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THESE

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Par

Elodie CARNEIRO

Optimization of GaN on Silicon technology for RF power applications

Optimisation de la technologie GaN sur Silicium pour les applications de puissance RF

Soutenance le 18 Juin 2024 devant la Commission d'examen :

Président du jury :	M. Katir ZIOUCHE	Professeur (Université de Lille)
Rapporteurs :	M. Andrei VESCAN	Professeur (Université de Aachen)
	M. Bertrand BOUDART	Professeur (Université de Caen Normandie)
Directeurs de thèse :	M. Farid MEDJDOUB	Chercheur CNRS, HDR (IEMN)
	M. Fabrice SEMOND	Directeur de recherches CNRS (CRHEA)
Examinateurs :	Mme Magali MORALES	Enseignant-chercheur (CIMAP-ENSICAEN)
	Mme Stéphanie RENNESSON	Ingénieur (EasyGaN)
	M. Philippe FELLON	Ingénieur (UMS)

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Abstract:

The advent of 5G and beyond telecommunications demands robust equipment capable of delivering superior output power density at high frequencies, particularly within the millimeter-wave spectrum ranging from 24 GHz to 94 GHz and beyond. This requires power amplifiers based on Gallium Nitride (GaN) instead of traditional Silicon (Si) and Gallium Arsenide (GaAs) employed in previous generations. GaN success in lighting and its potential in microLEDs, power electronics, and microwave technologies, including 5G networks, emphasizes its significance. SiC is generally the preferred substrate due to its high thermal conductivity, however not suitable for high volume applications because of the cost and low availability. Although more challenging from growth point of view, the use of cost effective Si substrate would solve the performance / reliability / cost balance. Usually, thick buffer layers (several µm) are used to minimize growth defect/dislocation density due to the large lattice mismatch between GaN and the Si substrate. However, thick buffer layers degrade the thermal dissipation and increase the epi-wafer cost. Therefore, the challenge lies in the hetero-integration of thin Nitride-based layers with Si substrates due to the growth complexity and material lattice mismatch. Despite two decades of research, mass-production of GaN-on-Si RF components remains elusive. To address this, a novel approach utilizing molecular beam epitaxy (MBE) on Si substrates is proposed, targeting the 5G market. This industrial Ph.D. collaboration between IEMN laboratory and EasyGaN aims to develop submicron GaN technology on Si for high-frequency applications up to W-band. The project focuses on creating a robust technology with superior performance while mitigating thermal and trapping effects. The thesis reminds the fundamentals of GaN-based HEMT for millimeter-wave applications, emphasizing growth techniques and device optimization. Methodologies for device fabrication and characterization, including high-frequency tests up to 40 GHz, are detailed. Optimization efforts include buffer and barrier layers, with a focus on enhancing power gain and transistor performance. In this work, the development of a total buffer thickness below 650 nm with Al-rich step-graded layers on Si substrate enables a unique combination of low electron trapping effects, low leakage current and extreme robustness under high electric field. Furthermore, the use of ultrathin AlN barrier combined with this innovative buffer allowed for high millimeter-wave power gain. This, in turn, enables excellent class AB bias operation at 40 GHz (up to $V_{DS} = 30$ V) for 140 nm gate lengths, promising RF reliability and potentially stable ultrathin AlN/GaN-on-Si HEMTs under high-power operation. Finally, a thermal management technique is introduced to enhance RF performances. These projects signify a crucial step towards realizing cost-effective GaN-on-Si technology, pivotal for advancing future electronic components in telecommunications applications.

Key words: GaN-on-Si, MBE, HEMT, Heterostructure, Millimeter-wave, High-frequency, Load-pull, Reliability

Résumé :

L’émergence des télécommunications 5G et au-delà exige des équipements robustes capables de fournir une densité de puissance de sortie supérieure à des fréquences élevées, particulièrement dans le spectre des ondes millimétriques allant de 24 GHz à 94 GHz et au-delà. Cela nécessite des amplificateurs de puissance basés sur le nitrure de gallium (GaN) plutôt que sur le silicium (Si) et l'arséniure de gallium (GaAs) traditionnellement utilisés dans les générations précédentes. Le succès du GaN dans l'éclairage et son potentiel dans les microLED, l'électronique de puissance et les technologies micro-ondes, y compris les réseaux 5G, soulignent son importance. Le SiC est généralement le substrat préféré en raison de sa haute conductivité thermique, cependant, il n'est pas adapté aux applications à grand volume en raison de son coût et de sa faible disponibilité. Bien que plus difficile d’un point de vue de la croissance, l'utilisation d'un substrat Si économique résoudrait l'équilibre entre performances / fiabilité / coût. Habituellement, des couches tampons épaisses (plusieurs µm) sont utilisées pour minimiser la densité de défauts de croissance / dislocations en raison du grand désaccord de réseau de maille entre le GaN et le substrat Si. Cependant, les couches tampons épaisses dégradent la dissipation thermique et augmentent le coût du wafer épitaxié. Par conséquent, le défi réside dans l'hétéro-intégration de couches minces à base de nitrure avec des substrats Si en raison de la complexité de croissance et du désaccord de réseau des matériaux. Malgré deux décennies de recherche, la production de masse de composants RF GaN-sur-Si reste évasive. Pour remédier à cela, une nouvelle approche utilisant l'épitaxie par jets moléculaires (MBE) sur des substrats Si est proposée, ciblant le marché 5G. Cette collaboration doctorale industrielle entre le laboratoire IEMN et EasyGaN vise à développer une technologie GaN submicronique sur Si pour des applications haute fréquence jusqu'à la bande W. Le projet vise à créer une technologie robuste avec des performances supérieures tout en minimisant les effets thermiques et de piégeage. La thèse rappelle les fondamentaux du HEMT à base de GaN pour les applications en gamme d'ondes millimétriques, en mettant l'accent sur les techniques de croissance et l'optimisation des dispositifs. Les méthodologies de fabrication et de caractérisation des composants, incluant les tests à haute fréquence jusqu'à 40 GHz, sont détaillées. Les efforts d'optimisation comprennent les couches tampons et la couche de barrière, en mettant l'accent sur l'amélioration du gain de puissance et des performances du transistor. Dans ce travail, le développement d'une épaisseur totale de couches tampon inférieure à 650 nm avec des couches graduées riches en Al sur un substrat Si a permis d’obtenir une combinaison unique de faibles effets de piégeage, de courant de fuite faible et une robustesse extrême sous champ électrique élevé. De plus, l'utilisation d'une barrière AlN ultramince combinée à ces couches tampons innovantes a permis de démontrer un gain de puissance élevé sur la gamme d’ondes millimétriques. Par conséquent, nous avons pu observer un excellent fonctionnement en polarisation de type classe AB à 40 GHz (jusqu'à V_{DS} = 30 V) pour une longueur de grille de 140 nm, une fiabilité RF prometteuse et une stabilité potentielle des HEMTs AlN/GaN-sur-Si ultraminces sous forte puissance. Enfin, une technique de gestion thermique est introduite dans le but d'améliorer les performances RF. Ce projet marque une étape cruciale vers la réalisation d'une technologie GaN-sur-Si bas coût, essentielle pour faire progresser les futurs composants électroniques dans les applications de télécommunications.

Mots clé : GaN-sur-Si, MBE, HEMT, Hétérostructure, Onde millimétriques, Haute fréquence, Load-pull, Fiabilité

Summary:

Introduction:

Telecom equipment for 5G and more (base stations and mobile devices) must be capable of operating at high frequency (millimeter waves) from 24 GHz up to 94 GHz and above. In order to deliver the power and frequency needed for equipment's antennas, the current trend followed by the vast majority of power amplifier manufacturers is to use Gallium Nitride (GaN) instead of Silicon and GaAs (Gallium Arsenide) used in 4G equipment.

GaN semiconductor has revolutionized the lighting industry in recent years with the production of highly efficient blue light-emitting diodes (LEDs). GaN will also play a major role in the fields of microLEDs, power electronics (conversion of electrical energy) and microwave electronics (5G and more telecommunications networks), which is the subject of this thesis. The active region of such a transistor is composed of GaN, AlN (aluminum nitride), and AlGaN alloys, all belonging to the nitride family and, ideally, deposited on a nitride substrate. In practice, the scarcity of such substrates has led to the use of alternative substrates, such as sapphire for LEDs and silicon carbide (SiC) or silicon for transistors. The core of these transistors is an electron gas of high density and high mobility at the interface between GaN channel and Al(Ga)(In)N barrier layer, generating high current densities.

For the deployment of 5G, high performance solutions based on GaN heterostructures grown on SiC substrates are available. However, these substrates are significantly more expensive than silicon (approximately 100 times) and thus not yet cost-effective for high volume applications. Currently, both industries and academics are investing in technologies based on silicon substrates to overcome these challenges. GaN-on-silicon technology is expected to become critical for future electronic components. Nevertheless, the development of GaN-on-Si technology has been limited by multiple challenges related to the growth complexity. On the one hand, the chemical reactions during deposition (usually via metal-organic chemical vapor deposition, known as MOCVD technology) of nitrides on silicon are challenging to control, and on the other hand, the large lattice and thermal expansion mismatch between these two completely different materials generate numerous defects. Despite intense academic research and sustained efforts by industrial players over the past 20 years, the growth of GaN on silicon remains difficult to master and reproduce, continually postponing the emergence of mass-produced GaN-on-Si RF components in the market. To address this issue, researchers have developed sophisticated intermediate layer structures, known as buffer layers, but at the expense of complexity and cost. Furthermore, they still do not meet the reliability expectations that semiconductor industry has become accustomed to with silicon-based devices.

In this context, we propose the development of a simple and thin structure grown on a silicon substrate using molecular beam epitaxy (MBE) growth technique, which targets 5G and above telecommunications market.

Within this framework, the present industrial Ph.D. between IEMN laboratory and the French industrial EasyGaN was initiated with the aim of developing a new GaN technology on Si substrates for Ka up to W-band frequency. This thesis work was supported by the French RENATECH network, and the French National grant GaNeXT ANR-11-LABX-0014.

The project organization consists in the device fabrication and electrical characterization at IEMN using various epitaxial structures grown by EasyGaN. The primary focus of the research conducted in this work regarding GaN technology development encompasses several key objectives: 1) create a robust technology that exhibits outstanding performance in terms of power density, current density and especially high power-added-efficiency for millimeter-wave applications while maintaining high operating voltages (V_{DS} > 20V). 2) reduce the impact of thermal and trapping effects. Subsequently, to evaluate the heterostructure and transistor performances, advanced characterizations are carried out, including: high voltage, DC, small signal, DC pulsed, large signal and temperature measurements as well as structural characterizations.

The objective of **chapter 1** is to establish the basics of GaN-based HEMT, which will be used throughout the manuscripts, and its promises for millimeter-wave applications, while also outlining the main industrial and academic players. Then, a justification of the chosen GaN heterostructure (compared to other materials such as Si, GaAs, InP, etc.) and the use of MBE growth technique rather than MOCVD will be provided. Next, growth aspects will be addressed. This section will detail the experimental process systematically applied throughout the project: epitaxy and structural characterization of the layers. Finally, the device design, fabrication, and optimization of millimeter-wave GaN-based HEMTs as well as the main figure of merit and related state-of-the art are presented.

Chapter 2 is devoted to the description of the adopted methodology for the study of GaN HEMTs. The adopted device fabrication steps and optimizations of GaN-based HEMT technology for high frequency will be described in this chapter. An overview of the test benches used in the frame of this thesis to carry out high voltage, static, small signal and DC pulsed, large signal up to 40 GHz, DCT and temperature characterization are described.

Chapter 3 presents the study of different sub-micron thick buffer on silicon and the optimization of the AlN nucleation layer. In this chapter, several batches of HEMT structures are studied in order to analyze various parameters affecting the device performances. In particular, the impact on breakdown field, electron confinement, electron trapping effects and robustness under high electric field has been extensively studied by means of high voltage, DC, pulsed and RF.

Chapter 4 focuses on the optimization of the barrier layer by using ultrathin Al-rich barrier layers with the aim of optimizing the GaN-based transistor performances as well as the power gain at high frequency. Power measurements up to 40 GHz are realized.

Chapter 5 provides an overview of the outlook of this work, presenting preliminary results after thermal management through substrate thinning and the use of a heat sink, such as copper, to enhance RF power performance**.**

Chapter 1: Introduction to GaN-based HEMT Technology

I. GaN technology: Advancements, applications, and impact on modern electronics

I.1. Overview

Semiconductors are presents in many forms in everyday life for both electronic and optoelectronic applications. Among these semiconductors, GaN-based components made their appearance in the 90s. Thanks to their outstanding properties such as a wide bandgap of 3.4 eV, a high thermal and chemical stability, a high breakdown field (3.3 MV/cm), and a high electron saturation velocity (2.5×10^7cm/s), GaN material is highly suitable for various optoelectronic, high-power, and high-frequency devices.

From a chronological standpoint, GaN was first used as a semiconductor in bright-light-emitting diodes. Then, its low sensitivity to ionizing radiation made it a suitable material for solar cell arrays on satellites. Furthermore, its stability in radiation environments also makes it advantageous for military and space applications. GaN material has also demonstrated its superiority in the realization of high electron mobility transistors (HEMTs) through numerous studies. This showcased the potential to achieve a unique combination of power, efficiency, higher bandwidth, and superior high-temperature stability compared to gallium arsenide (GaAs) or Silicon-based technologies, making them ideal power amplifiers for microwave frequencies. Some of these applications are illustrated in **Figure 1.1**.

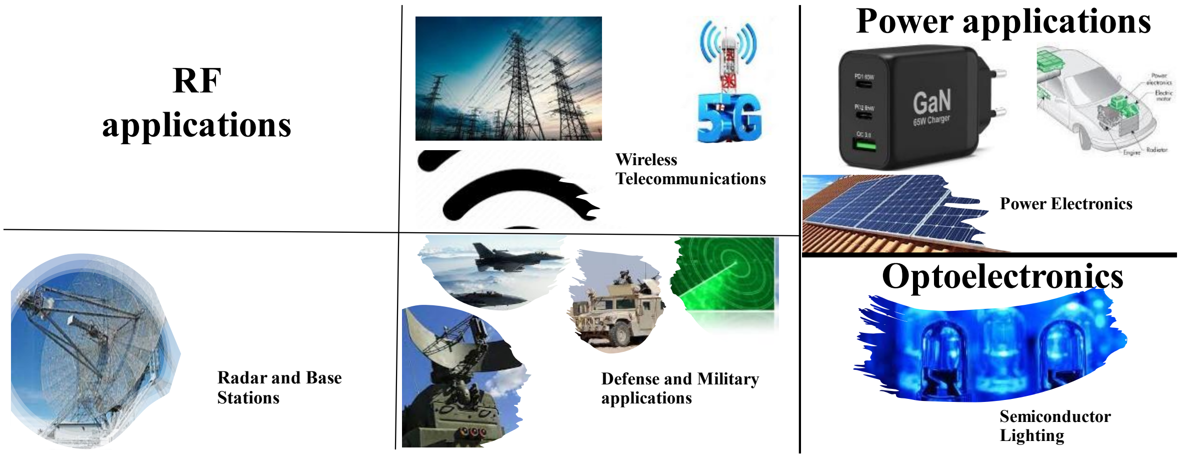


Figure 1.1.: Illustration of some applications for GaN HEMTs.

I.2. GaN-based HEMTs for millimeter-wave applications

In today's society, the processing, flow, and exchange of information have become crucial. Connectivity and mobility are two major factors in this context, both linked to the efficient flow and exchange of information. Hence, the growing interest in the millimeter-wave (mm-W) band (30-300 GHz) enabling shorter wavelengths and wide frequency bands, which allows the development of smaller components with improved performances. In addition, mm-W radiation is non-ionizing. **Figure 1.2** displays a diagram of the entire electromagnetic spectrum, with a focus on the microwave spectrum. In the past, early radio systems primarily utilized the lowest frequency bands for basic voice communication, which provided sufficient bandwidth for their needs. However, with in the progress of the technology and the expansion of wireless communication in terms of scale and complexity, there is a growing demand for greater bandwidth at higher frequencies. The exploration of the microwave spectrum began with the development of radar for military applications, where higher frequencies allowed for enhanced antenna resolution, serving vital purposes in military operations.

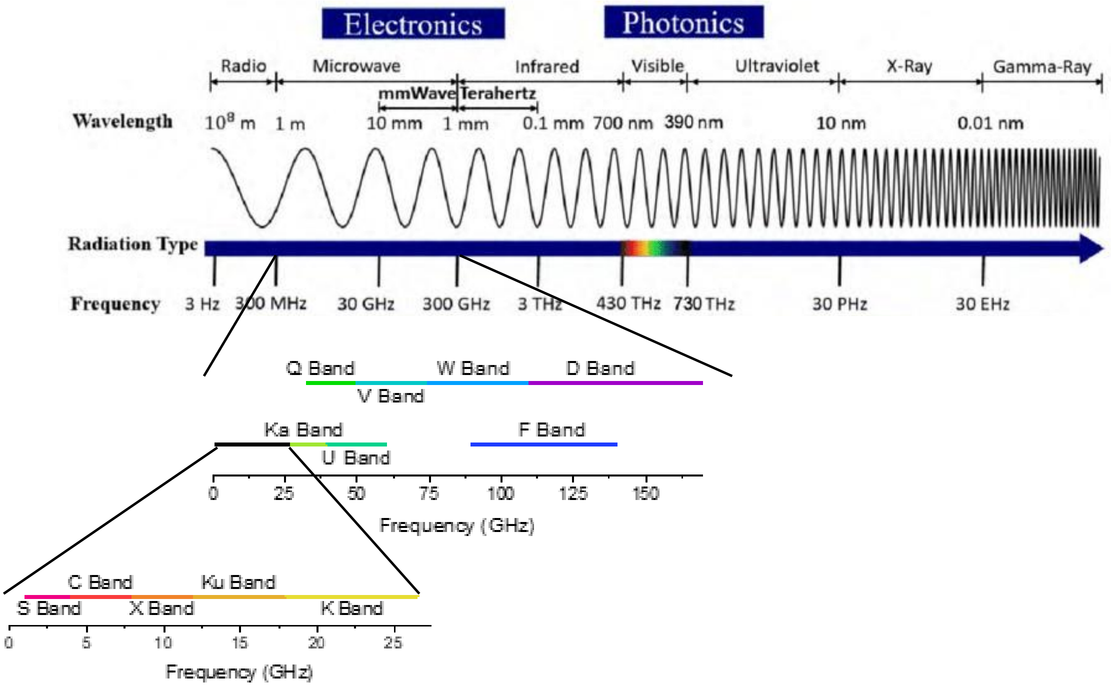


Figure 1.2.: The electromagnetic spectrum in wavelength and frequency [1].

As wireless communication systems expand to higher frequencies, system designers seek high bandwidth to support emerging applications. However, effectively utilizing the mm-W spectrum poses several challenges. Monolithic microwave integrated circuits (MMICs) based on III–V semiconductors play a crucial role in meeting the requirements of the mm-W range. High-frequency MMICs require a combination of high power/high efficiency, compact size, and cost-effectiveness. Currently, many MMICs in production, such as gallium arsenide (GaAs), silicon carbide (SiC), silicon (Si), indium phosphide (InP), etc., operate in the microwave and mm-W range, with modest breakdown voltages and limited power handling capabilities [2, 3]. However, the demand for higher power/frequency applications in the RF/microwave spectrum is steadily increasing. In this context, GaN material emerges as one of the most promising semiconductors, and its implementation in various applications has received a significant boost in recent years.

Indeed, the number of industrial and academic players has continuously increased over the last years. **Figure 1.3.a** shows a non exhaustive list of some industrial and academic players worldwide involved in the development of GaN technology. There are three major hubs on three different continents where GaN technology is industrially developed: USA, Japan, and Europe. In accordance, the total GaN RF market is predicted to double from $1.3B to more than $2.7B by 2028 in order to meet the needs of mm-W spectrum (**Figure 1.3.b**) [4]. Telecom infrastructure and defense are the main markets in 2022 and will keep covering the market with the corresponding increase of the demand. With a 10% increase of its resources, the telecom infrastructure will represent almost 45% of the total market.

In the field of telecom infrastructure, in the past year, wireless communications moved from the current fourth generation (4G) to the fifth generation (5G), opening the path for mm-W technology. GaN-based devices aim to tackle various challenges to meet the ever-increasing system level demands, particularly in terms of efficiency, power levels, and modulation bandwidth. The expected rise in bandwidth will further promote the deployment of GaN technology in the upcoming years.

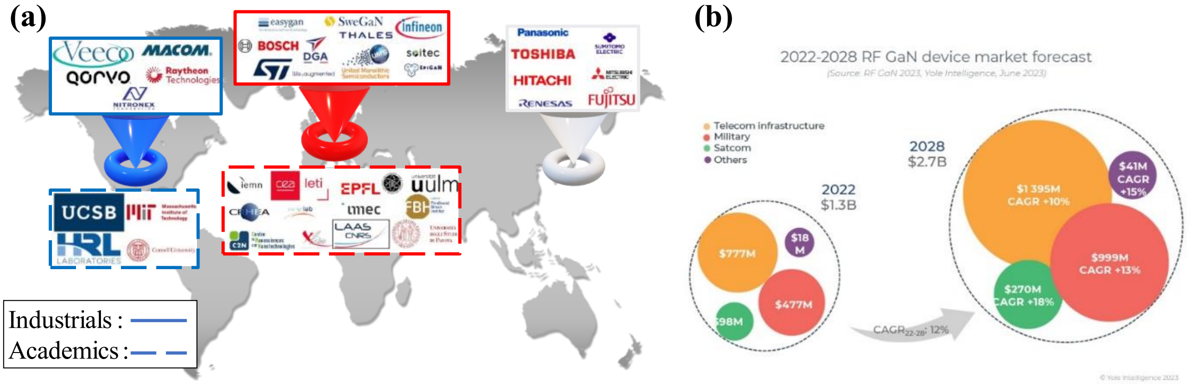


Figure 1.3.: (a) GaN technology's main industrial and academic players. (b) 2022-2028 RF GaN device market forecast Published by Yole Group - www.yolegroup.com[4].

I.3. Next generation wireless communication market

I.3.a. Brief history of wireless communication network

In 1895, the Italian inventor Marconi achieved a significant milestone by wirelessly transmitting Morse code signals using radio waves over a distance of 3.2 kilometers, marking the first-ever wireless transmission in the history of science. Since then, engineers and scientists have dedicated their efforts to efficiently communicate using radio frequency (RF) waves. **Figure 1.4** shows the constant evolution of the wireless communication network.

During the mid-20th century, the telephone gained popularity; however, its wired connection and limited mobility prompted engineers to seek alternatives. Consequently, they began developing a device that could transmit voice using radio waves, eliminating the need for a wired connection. In 1979, Nippon Telegraph and Telephone (NTT) in Japan pioneered the first generation (1G) of mobile telephony. Soon after, other carriers swiftly introduced their own systems. The 1G consisted essentially of an analogue telephone system. Nordic Mobile Telephone implemented 1G in 1981, while standards like Advance Mobile Phone System (AMPS) by Bell Labs in 1982 and C450 in Germany were widely adopted worldwide.

Second-generation (2G) mobile communication systems, which began in Finland in 1991, introduced a new digital technology called Global System for Mobile Communication (GSM). GSM technology served as the foundational standard for further advancements in wireless standards. It enabled up to 14.4 to 64 kbps data rate, which proved sufficient for SMS and email services. Additionally, during the mid-1990s, Code Division Multiple Access (CDMA) systems developed by Qualcomm were introduced and implemented. CDMA boasted several advantages over GSM, including improved spectral efficiency, support for more users, and higher data rates. Later developments of 2G encompassed features such as the inclusion of services like general packet radio service (GPRS) and Enhanced Data Rates for GSM Evolution (EDGE).

The launch of the third generation (3G) mobile communication started with the introduction of UMTS (Universal Mobile Terrestrial/Telecommunication Systems). This development coincided with the surge in internet users during the late 90s, which created a demand for users to access the web through their mobile phones. In response to this growing need, the 3rd Generation Partnership Project (3GPP) was formed in 1998, bringing together organizations from around the world to collaborate on developing protocols and standards for 3G. The result of this collective effort was the introduction of robust technologies such as

Wideband Code Division Multiple Access (WCDMA) and High-Speed Packet Access (HSPA), enabling high-speed and high-capacity web access. UMTS, with a data rate of 384 kbps, also supported video calling for the first time on mobile devices. Following the introduction of the 3G mobile communication system, smartphones became popular worldwide. Developers created specific applications for smartphones, enabling users to engage in multimedia chat, email, video calling, games, social media, and even healthcare services.

4G systems are an enhanced version of 3G networks developed by IEEE, offering higher data rates and the capability to handle more advanced multimedia services. Long-term Evolution (LTE) and LTE-Advanced wireless technologies are used in 4G systems, and they are compatible with previous versions, allowing for easier deployment and upgrade of their networks. With an LTE system, simultaneous transmission of voice and data is possible, resulting in a significant improvement in data rates. The use of complex modulation schemes and carrier aggregation allows for the multiplication of uplink and downlink capacity, further enhancing the performance of 4G networks.

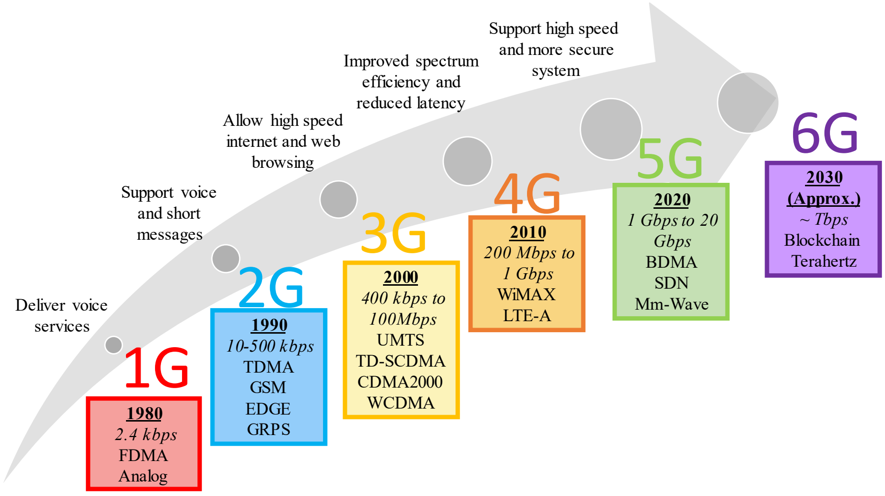


Figure 1.4.: Evolution of the mobile network technologies : 1G to 6G.

I.3.b. The transition from 4G to 5G: Challenges and opportunities in next-generation telecommunications

Since 2020, the wireless communication system has been shifting from the 4G to the 5G worldwide. Prominent international communication companies and manufacturers are engaged in a competitive race to showcase the capabilities and features of 5G technology. At the same time, they are paving the way for mm-W technology, which sets 5G apart from its predecessors in the realm of mobile telecommunications. The graphic of **Figure 1.5** gives an idea of bandwidth opportunity for 5G developers. 5G will mostly use the lower mm-W frequency band, somewhere between 24 GHz and 100 GHz. The 5G technology not only provides higher data rates but also brings about reduced latency, enhanced connectivity, and broader mobility and reliability. The scope of 5G encompasses broadband radio access and wireless networks, not only benefiting the telecommunication industry but also playing a transformative role in diverse sectors like robotics, automotive, factory automation, healthcare, and education. Specifically, the International Telecommunication Union (ITU) has initially defined three primary usage scenarios [5, 6]:

- **Ultra-reliable and Low Latency Communications (uRLLC):** to deal with highly reliable connectivity, low latencies (one millisecond or below), reliability and quickness of connection at low data rates.
- **Enhanced Mobile Broadband (eMBB):** to achieve high data rate peak speed of over 10 Gbps for high user density and very high traffic capacity.
- **Massive Machine-type Communications (mMTC):** for the Internet of Things (IoT) technologies requiring mass deployment of billions of low-cost, low powered consumption and low data rates devices with a very long battery life.

To realize this network performance, new features like a new waveform, Massive Input Massive Output (MIMO), beamforming (or special filtering), and mm-W technologies are essential for 5G. These advancements enable high efficiency, powerful Power Amplifier (PA) performance across a wide frequency range, resulting in cost-effective, broad bandwidth, and compact base-station systems.

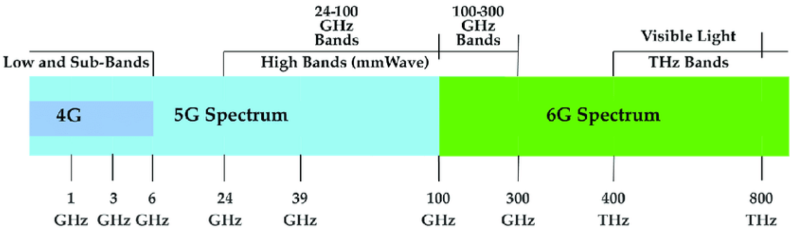


Figure 1.5.: The 4G, 5G and 6G spectrum in frequency [7].

I.3.c. From LDMOS to GaN HEMTs in telecom infrastructure

For the past three decades, Laterally Diffused Metal Oxide Semiconductor (LDMOS) has been the dominant technology for high-power transmit stages in wireless infrastructure, showcasing outstanding performance up to 3 GHz. Thanks to its cost advantage, stemming from fabrication on eight-inch Si substrates and full compatibility with standard Si process lines, LDMOS has been challenging to replace in the wireless base station market until the emergence of GaN HEMTs. Indeed, over the past two decades, GaN technology has emerged as a formidable contender to LDMOS in RF power applications, consistently demonstrating improved performance and reliability at a reduced cost. After making significant strides in the 4G-LTE telecom infrastructure market, GaN-on-SiC is expected to maintain a strong position in 5G sub-6 GHz RRH (Remote Radio Head) implementations (**Figure 1.6.a**). In the emerging domain of 5G sub-6 GHz AAS (Active Antenna Systems) with massive MIMO (mMIMO) deployments, the rivalry between GaN and LDMOS continues to evolve. According to **Figure 1.6.b** GaN technologies is aiming to reach half of the telecom infrastructure revenue by 2025 with the GaN-on-SiC technology being dominant. However, while GaN-on-SiC demonstrate remarkable bandwidth, PAE, and output power as compared to LDMOS, its cost-effectiveness remains to be improved. In this context, GaN-on-Si stands as a potential challenger and promises cost-efficient and integrated solutions. GaN-on-Si technology holds in particularly significant promise for telecom small cells that necessitate PAs with lower power requirements, making it a favorable option for 32T32R and 64T64R mMIMO base stations operating below 10W power range. GaN-on-Si is expected to enter the market by the end of 2023 with a foreseen gaining market share steadily in the forthcoming years (**Figure 1.6.b**).

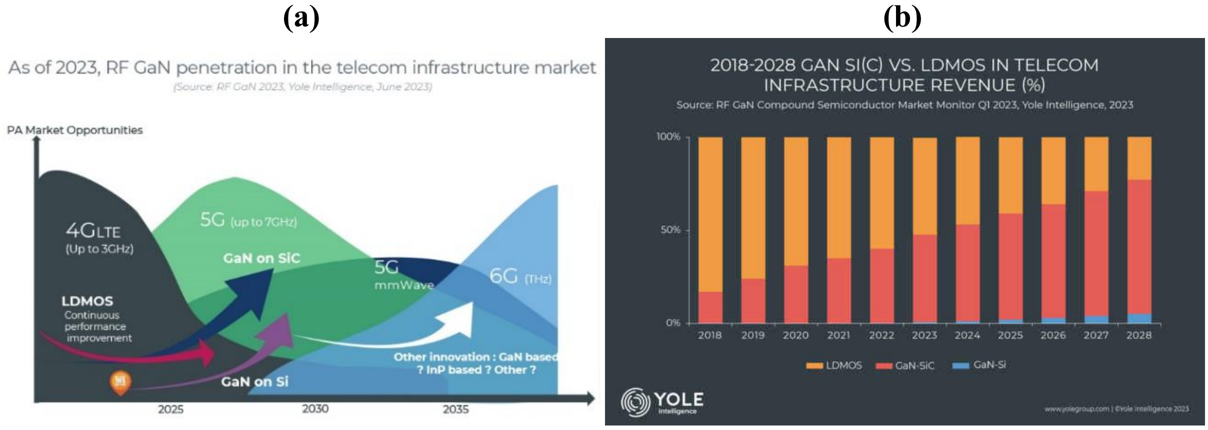


Figure 1.6.: (a) RF GaN penetration in the telecom infrastructure market. (b) 2018-2028 GaN-Si(C) vs LDMOS in telecom infrastructure revenue Published by Yole Group - www.yolegroup.com[8].

I.3.d. Future 6G: anticipating the next frontier of wireless communication

The growing number of new use cases, such as wireless backhaul, virtual reality (VR)/augmented reality (AR), the demands of a fully connected, intelligent digital world and space travel, raise questions about the ability of 5G wireless networks to satisfy emerging services and novel applications. This motivates the exploration of sixth-generation (6G) networks. In order to meet these demands, radically new communication technologies, network architectures, and deployment models will be needed [9]. In particular, it is projected that 6G wireless communication will be implemented approximately by 2030, with devices operating up to the terahertz range. The essential performance criteria for evaluating 6G wireless networks includes a peak data rate of 1 Tbps, which is 100 times that of 5G, a latency of 10–100 µs, and an energy efficiency that is 10–100 times better than 5G.

II. GaN material properties

II.1. Crystalline properties

Gallium nitride is a binary compound belonging to the group of III-nitrides, alongside aluminum nitride and indium nitride (AlN and InN). In the solid state, the elements in column III of the periodic table form covalent bonds with nitrogen. Nitrogen has a higher electronegativity than the elements in column III, making the III-N bond polar. The corresponding dipole moment is directed along the III-N bond, from the more electronegative element (nitrogen) to the less electronegative element (element III). The nitrides have a sp^3 hybridization state, where the atoms arrange themselves in a tetrahedral structure. Depending on the growth conditions and the substrate crystallographic orientations, III-N materials can crystallize into two structures: hexagonal (wurtzite) or cubic (zinc-blend). III-N materials can exist in the cubic zinc-blende phase under non-equilibrium conditions while the most common and thermodynamically stable form is the wurtzite phase. **Figure 1.7** represents the crystal structure of GaN in wurtzite form with two different orientations. It is characterized by two lattice parameters: a_0 and c_0, corresponding to the distance between two atoms of the same kind, neighboring in the hexagonal plane, and perpendicular to the hexagonal plane, respectively. **Table 1.1** summarizes the key properties of III-N elements. Since the GaN wurtzite structure has no inversion symmetry in the [0001] direction (c_0-axis) it can have a gallium or nitrogen polarity. Gallium polarity is associated with GaN oriented along the crystallographic axis [0001], while nitrogen polarity corresponds to GaN oriented along the axis $[000\bar{1}]$. These are referred to as Ga-face and N-face, respectively (**Figure 1.7**). All the samples developed during this thesis work are of gallium polarity.

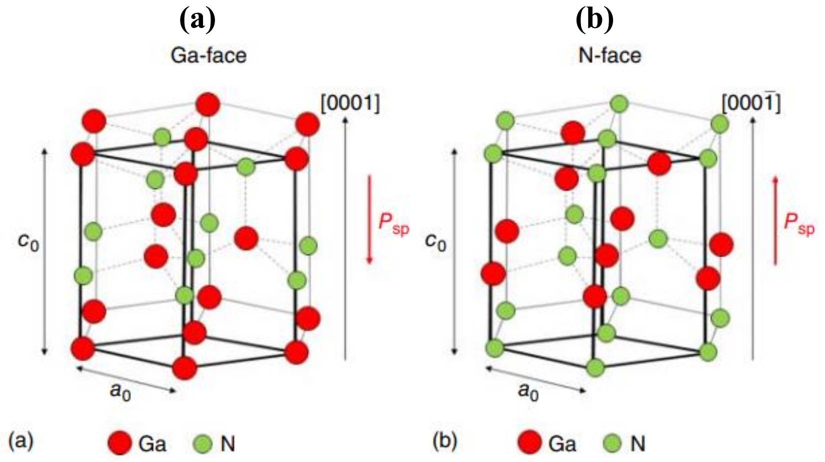


Figure 1.7.: Wurtzite (hexagonal) crystal structure of GaN (a) for the Ga-face and (b) for the N-face [10].

Furthermore, N-face crystals are more chemically active than Ga-face due to the crystallographic symmetry of GaN. They are characterized by a very rough surface morphology and a high doping concentration. On the other hand, Ga-face crystals have a much smoother surface morphology, lower doping concentration, higher electron transport properties, and are therefore preferred for power applications.

Wurtzite	**a_0 (Å)**	**c_0 (Å)**	**c_0/a_0**
GaN	3.189	5.185	1.627
AlN	3.112	4.982	1.601
InN	3.538	5.705	1.612

Table 1.1.: Lattice constants of III-N materials at room temperature (300 K)[11].

III-element nitrides can also be found in the form of ternary alloys: $Al_xGa_{1-x}N$, $In_xAl_{1-x}N$, and $In_xGa_{1-x}N$, where x represents the molar fraction. The lattice parameters of these alloys are typically obtained using a linear law (Vegard's law):

$$\gamma_{A_xB_{1-x}N} = \gamma_{AN}x + \gamma_{BN}(1-x) \qquad \textbf{Equation 1.1}$$

where γ represents either a_0 or c_0.

II.2. Polarization effects

Wurtzite crystals are considered ideal when it is composed of regular tetrahedra, which is the case when $c_0/a_0 = \sqrt{8/3} = 1.633$ [12, 13]. However, real wurtzite crystals are never ideal and are considered stable when $c_0/a_0 < 1.633$ which means that the tetrahedra in the wurtzite phase are not symmetrical but slightly distorted due to their environment. As a result, the sum of dipole moments within each tetrahedron do not cancel out, resulting in a nonzero dipole moment known as spontaneous polarization (P_{SP}). The induced internal electric field is oriented from the less electronegative charge (in this case, the III element) to the more electronegative charge (in this case, nitrogen), conventionally following the [0001] orientation or c_0-axis (see **Figure 1.7**). Consequently, as the c_0/a_0 ratio decreases, the P_{SP} increases. For example, due to its c_0/a_0 ratio of 1.601, the AlN crystal shows a higher P_{SP} of -0.081 C/m² compared to the GaN crystal, which has a higher c_0/a_0 ratio of 1.637 and a lower P_{SP} of -0.029 C/m² [13]. This also reveals the most important property of III-N materials: they are piezoelectric, meaning that deformation of the material from its initial state induces a polarization field called piezoelectric (P_{PE}) and, therefore, an electric field. The piezoelectric tensor of wurtzite in the group of III-nitrides has three independent components. Among them, e_{31} and e_{33} quantify the P_{PE} coefficient resulting from strain along the c-axis. The corresponding relationship is as follows [11]:

$$P_{PE} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \qquad \textbf{Equation 1.2}$$

where C_{13} and C_{33} are elastic constants [14]. The piezoelectric polarization is negative for tensile strain and positive for compressive strain.

Furthermore, in the case of a typical AlGaN/GaN heterostructure grown in the c_0-axis direction, the band diagram exhibits an energy discontinuity due to the varying energy gaps between the AlGaN film and GaN (**Figure 1.8.a**). Additionally, since the lattice constants $a_{0GaN} > a_{0AlGaN}$, a significant stress is induced on the AlGaN layer during growth. For an AlGaN/GaN heterostructure a tensile strain is induced and the orientation of the piezoelectric and the spontaneous polarization is parallel while for GaN/AlGaN heterostructure a compressive strain is formed and the orientation of the piezoelectric and the spontaneous polarization is antiparallel. For Ga-polar AlGaN/GaN heterostructure under tensile strain, the piezoelectric and spontaneous polarization point in the same direction toward the GaN substrate as shown in **Figure.1.8.b**. The value of the total polarization inside one layer is the sum of the piezoelectric and spontaneous polarization, $P = P_{PE} + P_{SP}$. The total polarization of both layers is directed towards the substrate for Ga-face and towards the surface for N-face polarity crystals. For each gradient of polarization, a polarization induced charge density is associated with the following definition:

$$\sigma = -\nabla P \qquad \textbf{Equation 1.3}$$

The polarization may either decrease or increase across the bilayer AlGaN/GaN, resulting in a fixed polarization charge density at the interface, which is defined by:

$$\left|\sigma\left(P_{Sp}+P_{PE}\right)\right| = |P(GaN)| - |P(AlGaN)| = |P_{SP}(GaN)| - |P_{SP}(AlGaN) + P_{PE}(AlGaN)|$$

Equation 1.4

As shown in **Figure 1.8.b**, for Ga-face and an AlGaN/GaN heterostructure, the polarization induced sheet charge is positive (+σ). In this case, free electrons will likely neutralize this charge, leading to the formation of a two-dimensional electron gas (2DEG) with a sheet carrier concentration, N_S, if the triangular quantum well at the interface will drop below the Fermi level as picture in **Figure 1.8.a**. Concerning N-face polarity a negative polarization induced sheet charge density (-σ) can form a two-dimensional hole gas (2DHG) if the valence band edge crosses the Fermi energy level at the interface of an AlGaN/GaN heterostructure.

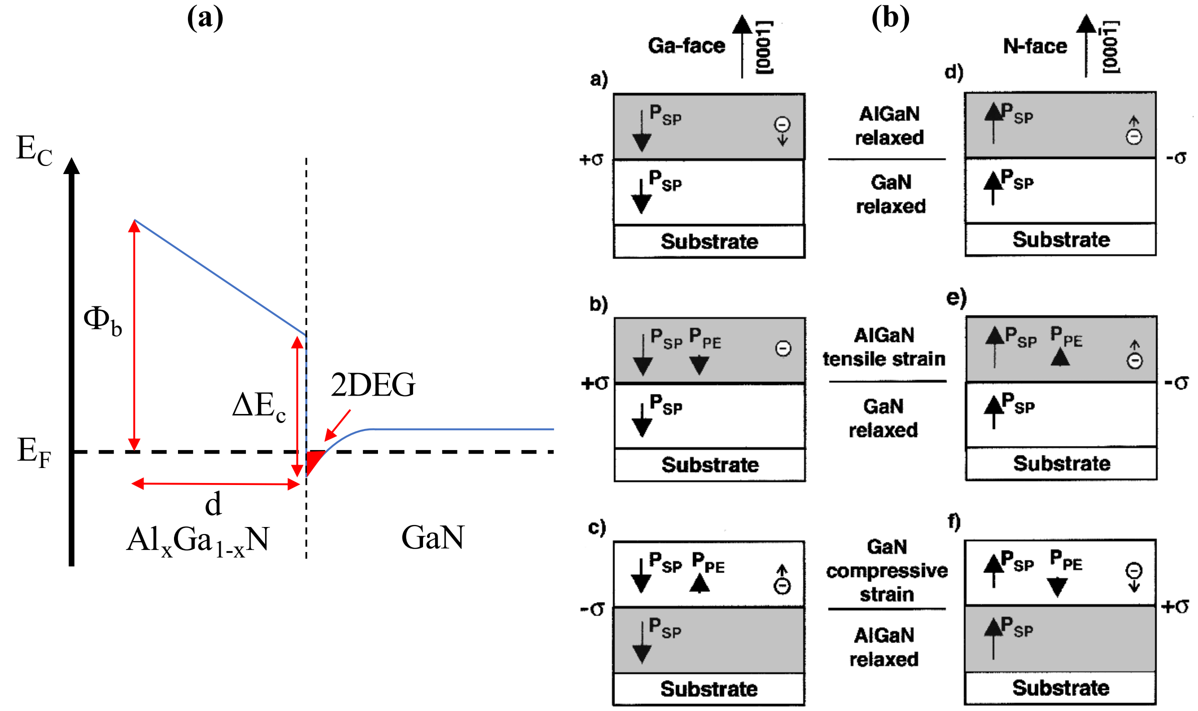


Figure 1.8.: (a) schematic band diagram of an Ga-face and AlGaN/GaN heterostructure. (b) Spontaneous and piezoelectric polarization in Ga-face and N-face strained and relaxed AlGaN/GaN heterostructures [14].

II.3. Sheet carrier concentration and mobility of 2DEGs

As mentioned before, a 2DEG can be formed at the interface of AlGaN/GaN heterostructure. The 2DEG electron concentration, N_S, can be calculated by using the following equation and the polarization induced sheet charge:

$$N_S = \frac{\sigma(x)}{e} - \left(\frac{\varepsilon_0 \varepsilon(x)}{de^2}\right)\left(e\Phi_b(x) + E_F(x) - \Delta E_C(x)\right)$$ **Equation 1.5**

where ε(x) and d are the relative dielectric constant and thickness of the AlGaN alloy layer, $e\Phi_b(x)$ is the effective Schottky barrier of the gate contact at the surface pinning the conduction band, $E_F(x)$ is the fermi level with respect to the GaN conduction-band-edge energy, and $\Delta E_C(x)$ is the conduction band offset at the AlGaN/GaN interface. **Equation 1.5** demonstrates that the value of N_S is dominated by the total polarization induced sheet charge which can be controlled by the alloy composition and the thickness of the AlGaN layer. The sheet carrier density of the 2DEG for a conventional AlGaN/GaN heterostructure is typically around 1×10^{13} cm^{-2}.

Furthermore, electron mobility (μ) is a quantity used to characterize the 2DEG. It is related to the average relaxation time of an electron between two collisions (diffusion). Diffusion mechanisms are partly related to the defects present in the AlGaN/GaN heterostructure. Two diffusion mechanisms can be distinguished:

- Elastic diffusion mechanisms: diffusion through impurities, interface roughness, alloy disorder, and charged dislocations,
- Inelastic diffusion mechanisms: operated by acoustic and optical phonons.

The total mobility can be expressed as follows:

$$\mu = \left(\frac{1}{\mu_{impurities}} + \frac{1}{\mu_{roughness}} + \frac{1}{\mu_{alloy}} + \frac{1}{\mu_{dislocation}} + \frac{1}{\mu_{phonons}}\right)^{-1}$$ **Equation 1.6**

Therefore, each parasitic contributions appearing in **Equation 1.6** can affect the overall 2DEG mobility. That is why the more perfect and defect-free the AlGaN/GaN heterostructure is, the higher the mobility. Typically, standard AlGaN/GaN heterostructures on silicon substrates exhibit an electron mobility up to 2000 cm²/V.s.

Finally, the last criteria to evaluate the 2DEG is the sheet resistance (R_{sh}), expressed in Ohms per square (Ω/sq). This quantity corresponds to the resistance of the 2DEG and depends on the electron density and the electron mobility of the 2DEG, as given by this formula:

$$R_{sh} = \frac{1}{eN_S\mu}$$ **Equation 1.7**

For proper transistor operation, a lowest possible sheet resistance is essential.

II.4. Physical and electronic properties

Table 1.2 shows some of the electronic properties of GaN as well as those of other III-N materials and other commonly used semiconductors such as GaAs, InP, Si, and SiC. GaN material exhibits a combination of exceptional electrical properties compared to other semiconductors. First, the wide band gap (WBG) of the material (E_{GAP} = 3.4 eV) induces a high critical electric field (E_{CR} = 3.3 MV/cm), which is the maximum field that the material can withstand without breakdown. It exceeds 3 times those of InP, GaAs and Si enabling higher breakdown voltage and higher operating voltage. Furthermore, although WBG materials are not known for delivering high electron mobility, GaN stands out prominently with a remarkably high saturation velocity (ν_{sat}) of 2.5×10^7 cm/s (three times higher than that of Si technology), which is crucial for high-frequency applications. The electron velocity is also linked to the current density, which is why GaN can generate substantial current at high voltages. It is worth mentioning that GaN material enables the use of heterostructures (In)(Al)GaN/GaN, resulting in a HEMT capable of achieving electron mobility exceeding 2000 cm²/V·s. The thermal conductivity of GaN is expected to vary in a certain range (1.3 − 2.1W/cm. K) depending on the defect density. These values are lower than those in SiC but much higher than GaAs or InP.

	III-N materials			**Other semiconductors**			
	InN	AlN	GaN	GaAs	InP	Si	SiC
Band gap energy E_{GAP} (eV)	0.7	6.2	3.4	1.42	1.34	1.12	3.3
Critical electric field E_{CR} (MV/cm)	1.2	8.4	3.3	0.4	0.5	0.3	3
Saturation velocity ν_{sat} ($\times 10^7$ cm/s)	1.4-1.8	1.7-2.1	1.5-2.5	1.3	1	1	2
Electron mobility μ (cm²/V.s)	3200	300	900 2000*	8500 10000**	5400 10000***	1500	900
Thermal conductivity λ (W/cm.K)	1.8	2	1.3-2.1	0.5	0.7	1.5	4.5

**AlGaN/GaN, **AlGaAs/GaAs, ***InAlAs/InGaAs heterostructures*

Table 1.2.: Main physical and electrionic properties of III-N materials and commonly used semiconductors at room temperature (300 K) [10, 15–18].

Figure 1.9 summarizes in a “radar chart” the electronic properties of GaN compared with those of GaAs, InP, Si and SiC. Utilizing GaN-based devices offers notable benefits due to the aforementioned properties, particularly in achieving high-voltage, high-frequency, and high-temperature operation capabilities. The graphic gives an idea of the great potential of this material in each domain.

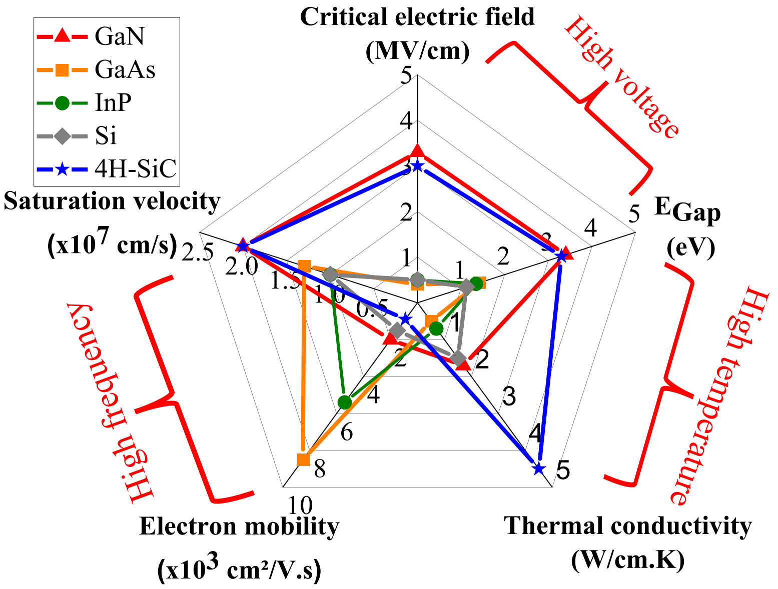


Figure 1.9.: Comparison of the physical and electronic properties of GaN semiconductors and commonly used semiconductors at room temperature (300 K).

For a better comparison of power and potentially achievable frequency performance using these various semiconductor materials, figures of merits have been proposed. The most commonly used in the field of power electronics and high frequency are: Johnson's Figure of Merit (JFM) and Baliga Figure of Merit (BFM). JFM extensively employed in RF devices, demonstrate the semiconductor material's capability to operate effectively at elevated frequency and power levels. It takes into consideration the critical electric field and electron saturation velocity and can be expressed as follows:

$$JFM = \left(\frac{v_{sat}E_{CR}}{2\pi}\right)^2$$ **Equation 1.8**

BFM evaluates the device's ability to withstand voltage and its resistive losses. It involves electron mobility, relative permittivity, as well as critical electric field:

$$BFM = \varepsilon\mu E_{CR}^3$$ **Equation 1.9**

Table 1.3 compiles the values of the main figure of merits normalized with respect to silicon. The potential of GaN is clear, as it presents a promising balance between high power and high frequency capabilities. Moreover, even though AlN shows even more promises than GaN, related research is not yet mature and still far from practical utilization of this material. Creating HEMT-type structures relying on AlN poses challenges due to considerable lattice mismatch with other III-V compounds. Nonetheless, there has been evidence indicating that incorporating an extremely thin AlN barrier layer in GaN-based heterostructures can significantly improve the 2DEG properties within the channel [19, 20]. Regarding GaN and SiC, they exhibit comparable figure of merits, offering significant advantages over traditional semiconductors. A considerable portion of ongoing research in RF devices is centered around GaN/SiC heterostructures, showing superior performance when compared to alternative technologies [21–23].

	Si	**InN**	**AlN**	**GaN**	**GaAs**	**InP**	**4H-SiC**
JFoM	1	41	2830	756	3	2.8	400
BFoM	1	0.2	3400	650	15.6	18	452

Table 1.3.: Main figure of merits for WBG semiconductors normalized with respect to silicon [24].

III. GaN-based HEMTs

III.1. GaN-based HEMT heterostructure

A HEMT structure is typically composed of the layer stack as described in **Figure 1.10**. The heterostructure is based on III-N materials grown on a substrate and composed as follows: a nucleation layer (NL), GaN-based buffer layers, a GaN channel layer, a spacer, a wide bandgap barrier layer (AlN, InAlN, InAlGaN or AlGaN), and finally an in-situ grown cap layer. The juxtaposition of a wide bandgap material (barrier) and a lower bandgap material (channel) creates a 2DEG at their interface.

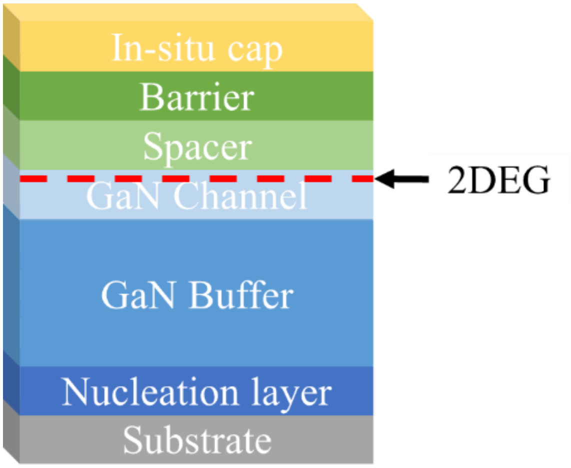


Figure 1.10.: Cross section of a typical GaN-based HEMT.

III.1.a. Substrate choice

Table 1.4 summarizes the properties of the main substrates used for GaN epitaxy: Sapphire, high resistive Si (111), 6H-SiC, bulk GaN and bulk AlN. The substrate, on which materials are grown, typically exhibits a relatively significant lattice mismatch with GaN. A substantial lattice mismatch, along with a high difference in thermal expansion coefficient, can lead to leakage paths under high electric field due to the dense dislocation density generated, and in extreme cases, could even result in cracks across the wafer.

	Sapphire (0001)	**Si (111)**	**6H-SiC**	**GaN (Bulk)**	**AlN (Bulk)**
Size	2”-6”	2”-12”	2”-6”	2”-4”	2”
Cost	-	--	+	++	+++
Resistivity ρ (Ω.cm)	> 10^{11}	> 10^{4}	> 10^{4}	> 10^{4}	10^{13}
Lattice constant a_0 (Å)	2.747	3.840	3.080	3.189	3.112
Thermal conductivity (W/cm.K)	0.5	1.5	5	1.5	2
Thermal expansion coefficient (× 10^{-6} K^{-1})	7.5	2.59	4.7	5.59	4.15
Difference in the lattice constant from GaN (%)	16.1 Compressive strain	-16.9 Tensile strain	3.5 Compressive strain	0	2.5 Compressive strain
Difference in the thermal expansion coefficient from GaN (%)	-25.5	115.8	18.9	0	34.7
Main application areas	Opto-electronics	High-Frequency and power electronics	High-Frequency electronics, opto-electronics	High-Frequency and power electronics, opto-electronics	High-Frequency and power electronics, opto-electronics

Table 1.4.: Properties of substrates used for GaN epitaxy [25].

Sapphire substrate is now the most commonly used because historically the first significant results for GaN growth were achieved on sapphire also due to its rather reduced cost [26].

However, its limited thermal conductivity hinders the manufacturing of power devices. Moreover, the difference in the lattice constant and heat expansion coefficient between GaN and sapphire result in substantial compression of the epitaxial GaN, leading to significant substrate curvature, dislocations and defects.

Newly published data provide confirmation that SiC stands out as the most appealing substrate for GaN millimeter-wave power devices. This preference is attributed to its exceptional physical properties, particularly its minimal lattice mismatch with GaN and high thermal conductivity, enabling unmatched power performance beyond the capabilities of other materials [21, 22]. Nonetheless, the primary constraint associated with SiC substrates pertains to their important cost and the limited availability of larger wafer sizes. It is also important to note that SiC has a lower thermal expansion coefficient compared to that of GaN results in tensile strain during cooling, which needs to be managed either by using relatively thin layers or by employing strain-adaptation layers.

In contrary compared to other substrates Si wafers are readily available at large-size (up to 12-inch) and can be acquired at a low cost. It also has a good thermal conductivity (though lower than that of SiC), making it a prime candidate for power components especially for mass production applications. Within this context, GaN-on-Si emerges as a prospective contender, offering the potential for cost-effective and integrated solutions as discussed in **section I.3.c**. However, silicon exhibits a substantial lattice mismatch and significant difference in thermal expansion coefficient with GaN. The tensile strain generated during cooling remains a critical concern for the growth of crack-free layers exceeding 3 μm in thickness.

Finally, the ideal scenario would involve the use of a GaN substrate that would enable near-perfect lattice matching. This would be particularly advantageous for GaN components with vertical transport. Bulk GaN substrates are also available commercially, exhibiting remarkably low dislocation densities (~10^7/cm²). However, its cost remains high with a size currently limited to 4-inch.

Within the framework, the investigated epitaxial structures are grown on Si substrates.

III.1.b. Nucleation and buffer layers design

The primary layer deposited on the substrate is the nucleation layer (NL), typically made of AlN in the case of Si due to its low lattice mismatch with GaN, which is only 2.5% (**Table 1.4**). A rather small thickness is enough to influence the entire structure by mitigating stresses and dislocations, thereby enhancing the quality of the active layers [27, 28]. Thus, the quality of the AlN NL ensures the integrity of the entire stack. The layer should possess the lowest possible dislocation density, minimal surface roughness, and good electrical quality with minimal trapping and ionized impurities to prevent leakage in the buffer and electron diffusion, which could adversely affect transport properties.

A set of GaN-based buffer layers is generally used, constituting a transition between the AlN NL and the GaN channel layer. GaN buffer layers need to be able to further decrease the dislocations reaching the channel while allowing a smooth surface of the barrier layer. **Figure 1.11** shows TEM images of structures with two different buffer and the reduced threading dislocations through the buffer all the way to the channel layer.

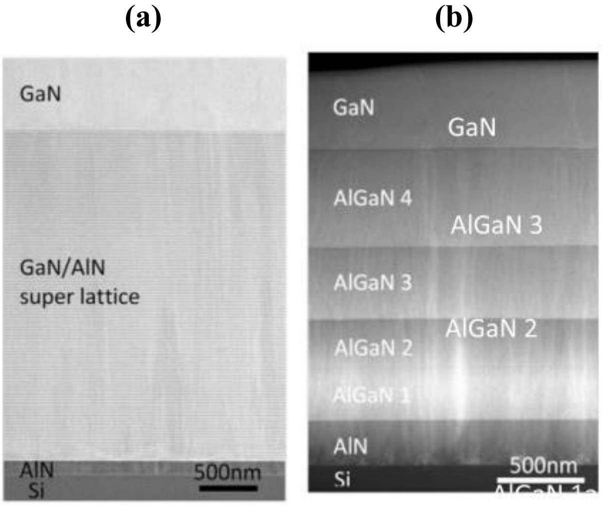


Figure 1.11.: TEM image of (a) a GaN/AlN superlattice buffer layer and (b) a step graded AlGaN buffer layer, both on Si substrates [29].

The buffer layer is also used to confine the electrons into the 2DEG under high electric field limiting short channel effects. Latest literature has demonstrated that for devices with poor electron confinement, the robustness is expected to decrease and high frequency performances cannot be achieved. Several configurations of buffers have been developed:

- ***Unintentionally doped GaN buffer:*** undoped GaN layer with a thickness exceeding one micrometer where residual n-type conductivity of the as-grown nitride layers are compensated by means of threading dislocations and/or carbon residual impurities for the formation of deep acceptor states [30]. It typically results in harmful short-channel effects, which degrades both the device's performance and long-term stability [31].
- ***Doped GaN buffer:*** Fe-doped or C-doped GaN are typically used to enhance the resistivity and thus enabling high breakdown voltage, which allows superior associated

output power density compared to unintentionally doped GaN buffers [30, 32–34]. However, while a heavily doped buffer enhances isolation and power performance, it also generally results in higher defect density and significant related scattering effects when dopants are introduced near the channel region leading to a strong current collapse [35, 36].

- ***$Al_xGa_{1-x}N$ buffer:*** this buffer involves incorporating AlGaN instead of GaN as buffer material to enhance the breakdown voltage sometimes at the expense of the mobility of the 2DEG, owing to AlGaN's wider bandgap and higher electric critical breakdown field [37]. The $Al_xGa_{1-x}N$ buffer layer acts as a back barrier, effectively improving the electron confinement in the 2DEG and significantly increasing the breakdown voltage of the devices. However, using a single layer of $Al_xGa_{1-x}N$ creates a significant lattice mismatch between the AlN NL or the GaN channel or both, depending on the Al content, thus impacting the quality of the 2DEG.

- ***Step-graded AlGaN buffer:*** sequence of AlGaN layers with decreasing Al content, ultimately leading to the GaN channel. This approach allows to take advantage of AlGaN alloys benefits, such as enhanced breakdown voltage and improved electron confinement, while gradually reducing the lattice mismatch between the AlN NL and the GaN channel [38–44]. However, the presence of AlGaN has a negative impact on thermal dissipation. The thermal conductivity of AlGaN decreases with increasing Al content [45]. Furthermore, the use of multilayers increases the number of interfaces and further degrades thermal dissipation [37].

- ***Compositionally graded AlGaN:*** in this case the composition is gradually changed from the AlN NL layer to the GaN channel layer [46–49]. Unlike step-graded buffer, the number of interfaces between each layer is decreased, thus reducing the poor thermal conductivity [37, 39].

- ***GaN/AlN superlattices:*** sequence of multiple Al(Ga)N/(Al)GaN layers, primarily enabling the growth of thick structures (greater than 1 µm) on Si without cracks. Through the iterative deposition of thin alternating layers of wide bandgap semiconductors characterized by excellent crystal quality (such as AlGaN, AlN, or GaN), the accumulation of internal strain is alleviated. This process yields a well-formed, highly insulating buffer with superior crystal quality, ultimately resulting in reduced buffer trapping effects [50–54].

The buffer is typically grown with thick layers (several µm) in order to decrease the dislocations reaching the channel layer while allowing a smooth surface for the barrier layer. However, a thick buffer degrades the thermal dissipation and increases the epi-wafer cost. Recent results showed that sub-micron thick with "buffer free" AlGaN/GaN HEMTs grown on SiC can deliver competitive RF performances [55, 56]. However, the large thermal expansion coefficient difference makes the growth on Si substrates even more challenging, and thus high performance with sub-micron thick GaN-on-Si HEMTs has not been proven yet to our knowledge.

Buffer optimization on Si was one of the main challenges of this work. In order to achieve this optimization, various sub-micron thick buffers inspired by the existing buffers cited above were studied.

III.1.c. Active layers: GaN channel, barrier and in-situ cap

The GaN channel, the spacer, the barrier, and the in-situ cap constitute the active layers of the HEMT heterostructure defining the 2DEG properties. The GaN channel is typically left undoped to facilitate high-quality electron transport. The selection of the GaN channel's thickness is crucial, as it directly impacts the electron confinement under high electric field for instance. A thicker GaN channel results in higher electron density and reduced trapping effects by pushing the doping compensation (if used) or the buffer layer interface away from the 2DEG. Nevertheless, when scaling devices with shorter gate lengths, a thinner GaN channel becomes necessary to mitigate short-channel effects reflected by the DIBL parameter, which could otherwise compromise device reliability and performance. As such, the choice regarding the GaN channel thickness relies on a balance between electron confinement and trapping effects for short GaN transistors.

In some heterostructure a spacer layer can be used. This layer is usually a thin AlN layer which enables overcoming diffusion due to alloy disorder and thus increasing the mobility of the 2DEG [57]. This can also be explained by the high bandgap of AlN (6.2 eV), which increases the conduction band discontinuity (> 1.7 eV) between the barrier and the channel. Moreover, this layer prevents the penetration of the 2DEG into the barrier. The optimal thickness is in the range of 1 nm for a spacer beneath an AlGaN barrier.

The channel and barrier layers enable the formation of the 2DEG at their interface as explained in **section II.2 and II.3**. The thickness of the barrier layer and its aluminum concentration are parameters that directly influence the N_s, μ, and R_{sh} of the 2DEG. The carrier density increases with the aluminum content. However, excessively high Al content in the barrier typically leads to an increase in leakage currents. This can indeed lead to a deterioration of piezoelectric properties due to relaxation phenomena, as well as the creation of leakage paths associated with defects. Various materials based on III-N semiconductors, including ternary and quaternary alloys, can be used as a barrier layer: AlGaN, AlN, InAlGaN, InAlN.

AlGaN/GaN HEMTs heterostructure is the most mature technology. An important aluminum content within the AlGaN barrier layer results in an enhanced spontaneous and piezoelectric polarizations, consequently leading to an increase in the 2DEG electron density, provided that a sufficiently thick barrier is maintained. However, achieving a pseudomorphic growth of high Al-content AlGaN on GaN presents challenges due to the large difference of their physical properties. This issue is reflected by AlGaN/GaN heterostructures exhibiting elevated dislocation levels as a result of tensile strain, particularly when employing thicker barrier layers close to the critical thickness [20]. Therefore, it becomes imperative to reduce the thickness of the AlGaN barrier in order to mitigate mechanical strains. A trade-off must be established between barrier thickness and Al content. Standard AlGaN barrier layers typically possess an Al composition ranging from 20% to 35%, along with a barrier thicknesses varying from 14 to 30 nm [58]. High Al-content and thick barrier within AlGaN/GaN structures result in larger mechanical strains. In contrary, adopting a lower Al-content along with a thinner barrier thickness leads to a reduction in the 2DEG density. Numerous investigations concerning AlGaN/GaN HEMTs have reported sheet carrier densities ranging from 5×10^{12} to 1×10^{13} cm^{-2}, delivering 2DEG electron mobilities reaching up to 2000 $cm^2/V.s$ [58]. These values are significantly influenced by the configuration of the AlGaN barrier layer. Moreover, below a certain critical barrier thickness, the energy of the donor level is higher than the energy of the Fermi level, the donor states are fully occupied, and the 2DEG is nonexistent. However, in order to enhance the performance of AlGaN/GaN HEMTs scaling down the barrier thickness is essential to uphold a substantial aspect ratio (gate length on gate to channel ratio L_G/a) and prevent undesirable short channel effects. Consequently, advanced epitaxial structure design, particularly in the selection of the barrier layer, are critical to fulfill the requirements for millimeter-wave applications.

The limitations posed by device design constraints arising from the lattice mismatch between AlGaN and GaN can be overcome through the substitution of AlGaN with either the ternary InAlN or the quaternary InAlGaN layers. In particular, InAlN demonstrates lattice matching with GaN at an indium composition of 17%, accompanied by notable attributes such as a substantial spontaneous polarization charge and a favorable band gap [59]. In the context of InAlN heterostructures, the significance of incorporating AlN spacer surpasses that of AlGaN heterostructures. This importance arises due to the considerably reduced electron mobility observed in InAlN/GaN heterostructures. InAlN/GaN HEMTs sheet carrier densities of 2×10^{13} cm^{-2}, with 2DEG electron mobility typically reaching up to 1300 $cm^2/V.s$ have been reported for sub-10 nm barrier thickness [60, 61].

In heterostructures containing quaternary layers, there exists a broad tunability of both spontaneous and electrical polarization. This flexibility enables the creation of both depletion and enhancement-mode transistors. In particular, it has been observed that the electron mobility within heterostructures incorporating quaternary InAlGaN layers surpasses that of InAlN/GaN heterostructures, even when the quaternary films have low concentrations of Ga [62, 63]. InAlGaN/GaN HEMTs sheet carrier densities ranging from 1.5×10^{13} to 1.8×10^{13} cm^{-2}, with 2DEG electron mobility reaching up to 2000 $cm^2/V.s$ has been reported for sub-10 nm barrier thickness [64]. Furthermore, the inclusion of quaternary layers in the devices resulted in reduced gate leakage, thereby further enhancing the transistor's performance when compared to transistor using InAlN layers [65]. While InAlN and InAlGaN/GaN-based HEMT devices show promise for millimeter-wave applications, they are not yet fully optimized and necessitate further research in terms of degradation mechanisms and parasitic effects that significantly influence the device reliability.

Another barrier widely used is the ultrathin AlN barrier due to its potential for significant scaling of the barrier layer (down to sub-5 nm), yielding larger polarization effects. Through the use of ultrathin AlN/GaN structures (sub-5 nm), the 2DEG density can still exceed 2×10^{13} cm^{-2}, coupled with an electron mobility of approximately 1000 $cm^2/V.s$ [19, 66, 67]. Additionally, the ultrathin AlN/GaN structure offers the advantage of mitigating short channel effects in highly scaled devices, owing to a favorable aspect ratio (L_G/a). These remarkable attributes position this material system as a prospective solution to meet the demands of GaN HEMTs for millimeter-wave applications. However, achieving high-quality growth of AlN/GaN remains challenging, particularly when employing thicker AlN barriers due to the substantial lattice mismatch between AlN and GaN. The strain, which increases significantly with AlN barrier thickness, elevates defect density within the barrier layer, thereby compromising the device robustness. Advances in the AlN/GaN structure have yielded impressive millimeter-wave performance [23]. Nevertheless, it's worth noting that a pure AlN barrier layer tends to exhibit higher contact resistance than an InAlGaN barrier layer although advanced and more expensive regrowth techniques can clear this issue [68].

Finally, the last layer that completes the HEMT is a passivation cap, typically a thin layer of GaN or SiN. One of the issues that can be encountered in GaN structures is related to surface states. It is important to emphasize that surface states are directly linked to the 2DEG and are accountable for several adverse effects on component performance. Surface charges lead to a localized depletion of the 2DEG [69–71]. Negatively charged surface states compensate for donor atoms, depleting the channel between the gate and drain, resulting in reduced dynamic current. This leads to a degradation of the component's performance and/or reliability. However, this issue has been more or less resolved, and one of the solutions is the use of a cap coupled with passivation (often SiN), which is deposited during the manufacturing process or even directly during growth. Moreover, apart from protecting the surface and passivating surface charges, it can also contribute to reducing the gate leakage current.

III.2. Growth techniques of a GaN-based HEMT heterostructure

The performance of HEMT devices is influenced by the growth methods employed for GaN-based heterostructures. Achieving high-quality and consistent epitaxial layer growth is heavily contingent on factors like temperature, pressure, and gas flow rate during the growth process. Molecular Beam Epitaxy (MBE) and Metal Organic Chemical Vapor Deposition (MOCVD) are the predominant and widely employed growth techniques, recognized for their popularity and common usage. **Table 1.5** offers an overview of the key features of these two methods.

	MBE	**MOCVD**
Growth pressure (Torr)	10^{-6}-10^{-4}	20-500
Substrate temperature (°C)	500-900	700-1200
Growth rate (µm/h)	0.1-1	0.2-5
Precursors	NH_3, N_2, solid metallic sources (Ga, Al, In)	NH_3, trimethyl-(Ga, Al, In)
Remarks	Regulating thickness and composition while managing interfaces Real-time growth management through in-situ monitoring (RHEED) Development stage	Rapid growth Multi-substrate wafer and large dimension substrates Industrial production

Table 1.5.: Key characteristics of growth techniques employed for the epitaxy of GaN-based HEMT.

III.2.a. MOCVD: Metal Organic Chemical Vapor Deposition

In today's semiconductor industry, the prevailing technique for manufacturing components in optoelectronics and power electronics is MOCVD or MOVPE (Metalorganic Vapor Phase Epitaxy). This method efficiently covers substantial surfaces while minimizing costs and time. The underlying principle of this growth approach involves the thermal decomposition of ammonia (NH_3), a nitrogen precursor, and an organometallic compound deposited onto the heated sample's surface. Commonly used organometallic compounds like trimethylgallium (TMGa), trimethylaluminum (TMAl), and trimethylindium (TMIn) are employed to introduce group III-elements. These compounds are introduced via a carrier gas (H_2 or N_2), and their pyrolysis on the surface of the heated sample releases the group III-element. The growth mode and quality of epitaxial layers will be especially affected by factors such as pressure, temperature, the V/III ratio, and the presence of hydrogen within the reactor. In particular, the interplay between pressure and temperature will exert a significant influence on the rates of both lateral and vertical growth. While this aspect holds less importance in MBE (owing to lower temperatures and reduced mobility of surface species), it assumes heightened significance in the growth of GaN featuring a low density of threading dislocations using the MOCVD technique. MOCVD facilitates rapid growth on sizable substrates (greater than 4") and multi-substrate wafers, leading to the formation of layers possessing acceptable crystalline quality. This technique stands out as the most widespread and well-matched method for producing substantial structures. In particular, it provides a versatile and cost-efficient approach that finds extensive use in today's semiconductor industry for crafting components such as LEDs, Heterojunction Bipolar Transistors (HBTs), HEMTs, Quantum Well Lasers, and more. The technique's advancement, encompassing the utilization of rather low epitaxial pressures and the incorporation of real-time in-situ growth monitoring methodologies (such as ellipsometry and reflectometry), presently enables precise control over layer thicknesses at the monolayer level, yielding minimal roughness and high-caliber interfaces. As a result, it becomes feasible to manufacture electronic or optoelectronic components using this approach, featuring structures with reduced dimensions.

III.2.b. MBE: Molecular Beam Epitaxy

MBE stands as an ultra-high vacuum growth technique: growth occurs within an extremely low residual pressure ($P \approx 10^{-11}$ Torr). This stringent condition is vital to prevent the integration of residual impurities and to ensure a sufficiently lengthy mean free path. MBE becomes feasible only when the mean free path of atoms surpasses the distance between the cell and substrate. This distinctive scenario permits atoms to reach the substrate surface without any interaction, hence the term "molecular beams”. In this procedure, atomic or molecular fluxes are introduced into a controlled chamber and interact upon a substrate, maintained at an optimal temperature for epitaxial growth. Effusion cells, housing group III-compounds (Ga, Al, In) slated for solid-state evaporation, are heated and strategically aligned toward the substrate (**Figure 1.12.a**). Sublimation of these compounds initiates the growth process. The nitrogen element is introduced either via a source generating chemically active N radicals from dinitrogen (N_2) through radiofrequency plasma, or by the thermal dissociation of NH_3 molecules at the substrate surface.

The growth process of MBE is influenced by a range of phenomena, all of which are governed by the specific growth conditions, such as temperature and atom fluxes. Upon reaching the surface, atoms undergo either physical adsorption (driven by attractive van der Waals forces) or chemical adsorption (involving electron transfer and subsequent chemical bond formation). In the former scenario, the weak binding energy between atoms and the surface promotes atom desorption. In the latter case, the stronger binding energies lead to atom integration onto the surface. Under appropriate temperature conditions, atoms may diffuse across the surface before becoming integrated into crystalline sites. This incorporation could occur along the edge of an atomic step or trigger the formation of an island on the surface. The atoms ability to settle into the most energetically favorable site plays a crucial role in ensuring high crystal quality, underscoring the importance of surface diffusion phenomena. Simultaneously, during growth, material decomposition can occur due to temperature effects or interactions with other species.

(a) **(b)**

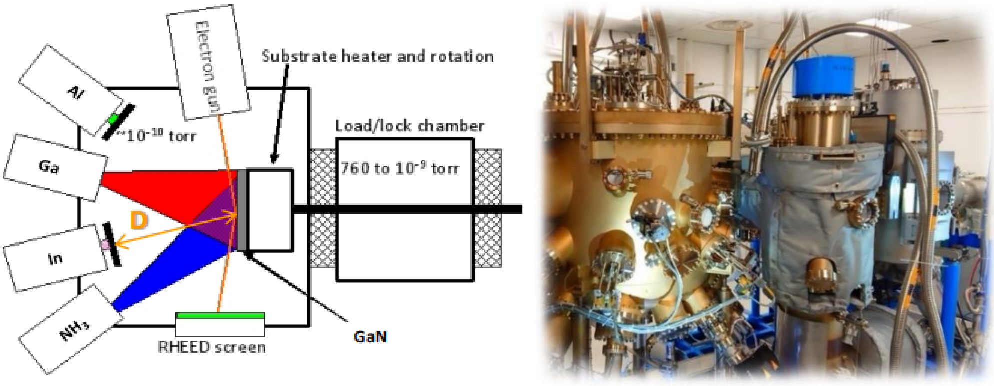


Figure 1.12.: (a) Schematic representation of an MBE growth reactor with ammonia source and (b) image of MBE 8-inch growth reactor at CRHEA.

When compared to other epitaxial methods, MBE provides a range of advantages:

- Swiftly interrupting flux using shutters positioned at the end of the cell allows for meticulous control over layer thickness and molecular-scale compositional adjustments.
- The use of comparatively lower temperatures (500-900°C) helps alleviate bulk diffusion effects and interdiffusion at interfaces. Moreover, these reduced growth temperatures diminish the strains resulting from disparities in thermal expansion coefficients between epitaxial layers and the substrate, thereby facilitating strain management.
- The slow growth rates (< 1 µm/h), in contrast to surface diffusion rates, namely offer precise management over the thickness of deposited layers and the achievement of sharp interfaces.
- The ultra-high vacuum setting allows the integration of diverse in-situ growth control methods and real-time monitoring of surface conditions like Reflection High Energy Electron Diffraction (RHEED) or tunneling microscopy, providing real-time insight into the ongoing growth process and the resultant crystalline quality.
- There is a minimal consumption of source materials, and safety measures are effectively managed.

Hence, MBE proves to be particularly well-suited for growing intricate multilayer structures, where elemental layers are exceedingly thin, and interfaces necessitate precision (HEMTs, quantum wells and dots, LEDs, lasers, etc.).

For this study, NH_3-MBE growth techniques was chosen for the growth of ultra-thin GaN based HEMT on Si and the multiple advantages listed previously. Two MBE reactors were primarily employed: an R&D reactor Riber Compact 21S, accepting up to 3” monowafer, and an industrial Riber MBE49 reactor with 3 x 4-inch configuration and up to 1x 8”. The reactors are located at CRHEA french laboratory (**Figure 1.12.b**).

III.3. Operating principle of HEMT transistors

Following the MEtal Semiconductor Field Effect Transistor (MESFET), the initial High electron mobility transistor (HEMT) emerged during the 1980s and quickly established themselves as leading components renowned for their low power consumption and minimal noise levels [72]. A HEMT is a heterojunction field-effect transistor. Its operating principle is based on the modulation of conductance between two ohmic contacts, the source (S) and drain (D), through the electrostatic action of a metallic control electrode known as the gate (G), with a length L_G and width W (**Figure 1.13.a**). The gate serves as the controlling electrode, enabling the adjustment of electron density within the 2DEG.

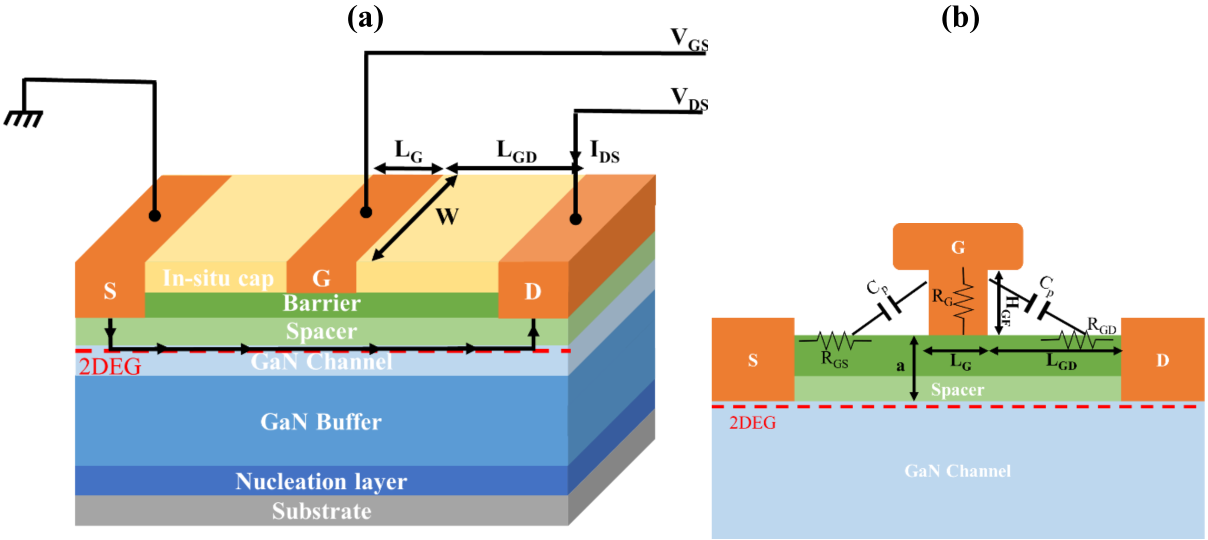


Figure 1.13.: (a) Operating principle of a HEMT transistor and (b) cross section of T-gate GaN HEMT.

Enhancement of high-frequency capabilities in millimeter-wave applications necessitates the scaling of GaN HEMT devices. These optimizations extend beyond the epitaxial structure and encompass various processing steps such as ohmic contacts and gate modules. Given that critical device dimensions are reaching the nanoscale, employing shorter gate lengths contributes to the reduction of electron transit time. Consequently, there is a need to decrease the thicknesses of HEMT epitaxial layers, particularly the barrier thickness. Nonetheless, it remains crucial to maintain a substantial aspect ratio (L_G/a) of over 15 [73]. Such a high aspect ratio is essential to counteract short channel effects while simultaneously enhancing the cut-off frequency/maximum oscillation frequency (F_t/F_{max}) ratio, which can be defined by the subsequent equations:

$$F_t = \frac{g_m}{2\pi(C_{GS}+C_{GD})}$$ **Equation 1.10**

$$F_{max} = \frac{F_t}{2(R_G+R_{DS})^{1/2}}$$ **Equation 1.11**

Where g_m represents the extrinsic transconductance, C_{GS} denotes the gate-to-source capacitance, C_{GD} refers to the gate-to-drain capacitance, and R_{DS} represents the drain-to-source resistance.

In order to achieve high frequency performances, it is necessary to minimize the electron transit time under the gate, maximize the intrinsic transconductance (hence minimize the barrier thickness), and reduce the gate length. Indeed, the primary factor for achieving strong RF performance is the optimization of the gate module. To achieve this, T-shaped gate structures are commonly employed. These structures serve to reduce parasitic capacitances and gate resistance as the gate length is minimized. Presently, the performance at higher frequencies is primarily restricted by short channel effects and parasitic components, which gain prominence as devices become shorter [73]. In **Figure 1.13.b**, a cross-sectional view of a GaN HEMT structure showcases the parasitic elements of the T-gate design. For improved F_{max}, a gate foot height (H_{GF}) exceeding 100 nm is necessary. Alternatively, enhancing F_t follows the guideline of reducing gate length (**Figure 1.14.a**) while ensuring a high L_G/a aspect ratio coupled with a substantial N_S. Moreover, the reduction of the source-to-drain distance, which effectively lowers the on-resistance, has proven to be successful in enhancing F_t/F_{max} and achieving a higher maximum drain current. As shown in **Figure 1.14.b**, after extensive endeavors within the research community and through the implementation of inventive device technologies, the most impressive achievements for F_t and F_{max} so far stand at 454 GHz and 582 GHz, respectively [74, 75].

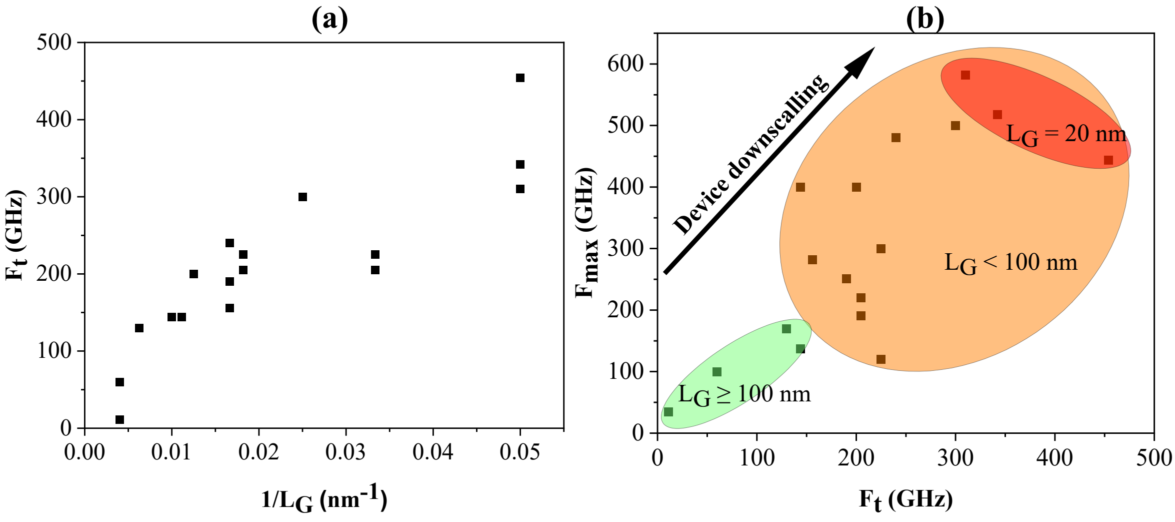


Figure 1.14.: (a) Scaling of cutoff frequency (Ft) of GaN HEMTs as a function of gate length (L_G) and (b) maximum oscillation frequency (F_{max}) as a function of F_t [74–85].

III.4. Figure of merit of GaN-based HEMTs

Within this thesis, the primary research emphasis lies in the creation of a high-performance GaN HEMT device intended for upcoming high-frequency power applications. To provide clearer insight into the thesis's objectives, it proves beneficial to delve into the key facets of GaN HEMTs functioning within the millimeter-wave spectrum. The sought-after achievements for high-frequency devices encompass the synthesis of elevated power and efficiency alongside high breakdown field.

III.4.a. Breakdown Field

Beyond a specific V_{DS} threshold, there is a sudden degradation of off-state leakage current, corresponding to the transistor breakdown, primarily attributed to the impact ionization phenomenon (if no other extrinsic cause such as material defects or processing contamination occur). The device breakdown appears when electrons, accelerated by the electric field within the channel, attain sufficient kinetic energy (greater than or equal to the bandgap). During a collision between a conduction band electron and a valence band electron, an electron-hole pair can form. Each charge is subsequently accelerated by the electric field and can, in turn, ionize another atom within the crystalline lattice. As a result, the drain current I_D experiences a sharp increase, and the lack of control over this effect can lead to irreversible transistor deterioration. The holes produced by these collisions can be collected by the gate or drain, captured by specific traps, or even recombine with the channel electrons.

While testing AlGaN/GaN-on-Si HEMTs intended for high voltage applications, a discovery has surfaced regarding their Breakdown Voltage (BV). This finding points to a critical limitation stemming from the vertical top-to-substrate "breakdown" phenomenon. The chase of enhanced vertical BV has led to the emergence of several potential solutions. Among these, thicker buffer layers [52] and the growth of AlGaN buffer layers with wider bandgaps [86] have taken center stage. Indeed, the deployment of highly resistive buffer layers has emerged as a crucial strategy. These layers exert their influence by leading to a reduction in background carrier concentration, thereby enhancing the OFF-state blocking voltage. Moreover, one of the main goal hinges on decreasing leakage current that manifest between the drain and substrate when these devices are held in high-voltage OFF-state conditions.

Exploring past research, the conduction mechanisms within the vertical stack have been meticulously examined. Insights gathered from these explorations highlight a significant finding: the vertical leakage current's trajectory is distinctly governed by Space Charge Limited conduction, a phenomenon driven by trap states embedded within the materials [87, 88]. Further enriching our understanding, a comprehensive analysis by Li et al. [89] shines a light on the conduction mechanisms through the nucleation layer that adorns the silicon substrate. This explanation reveals how imperfections, deep layers, and boundary states significantly affect the intricate flow of current through a naturally imperfect AlN layer.

III.4.b. Power added efficiency and output power density

GaN HEMT devices are expected to offer the ability to provide significant large signal gain, high efficiency, and a high output power density within the designated frequency range. The transistor's power gain (G_P) at the frequency of interest is characterized by the ratio between the absorbed high-frequency powers at its output (P_{RFOUT}) and input (P_{RFIN}). This value incorporates the input and output reflection coefficients of the transistor, providing a means to assess the genuine performance of the component under conditions of substantial signal magnitudes. G_P stands as the frequently employed power gain measure, and its mathematical representation is as follows:

$$G_P(dB) = 10\log_{10}\left(\frac{P_{RFOUT}}{P_{RFIN}}\right) \qquad \textbf{Equation 1.12}$$

The Power Added Efficiency (PAE), which is the ratio of the actual high-frequency power delivered by the active component (difference between the output power and the input absorbed power) to the DC power supplied for its operation, is expressed as follows:

$$PAE = \frac{P_{RFOUT}-P_{RFIN}}{P_{DC}} = \frac{P_{RFOUT}}{P_{DC}} \times \left(1-\frac{1}{G_P}\right) \qquad \textbf{Equation 1.13}$$

Where P_{DC} is the dissipated DC power density. This parameter reflects the efficiency of power conversion in the transistor. A high PAE reduces losses due to thermal dissipation. It also contributes to the long-term reliability of the transistor. The operational mode of a transistor dictates its polarization class. As illustrated in **Figure 1.15**, there exists a variety of polarization classes (A, AB, B...), with the primary focus in this study being on deep class AB. Within class AB, the quiescent drain current is calibrated to an optimal value, striking a balance between linearity and efficiency.

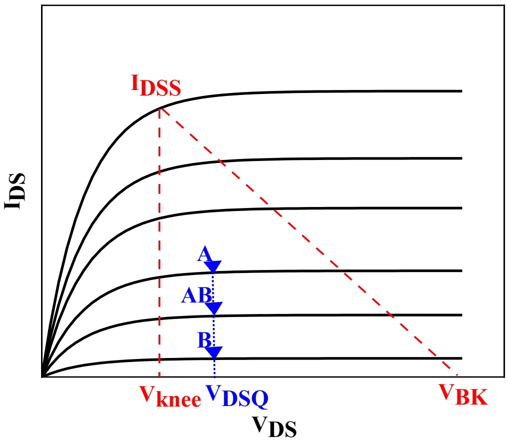


Figure 1.15.: $I_D(V_{DS})$ curve of GaN HEMT at different V_{GS} showing three different polarization types.

Finally, the output power density (P_{OUT}) can be defined as followed:

$$P_{OUT} = \frac{(V_{DSQ} - V_{knee}) \times I_{DSS}}{4}$$ **Equation 1.14**

Where V_{DSQ} represents the quiescent bias of drain-source voltage, V_{knee} stands for the knee voltage on the transistor's $I_{DS}(V_{DS})$ curve, and I_{DSS} denotes the saturated current density. A substantial breakdown voltage facilitates elevated quiescent operation of drain-source voltage, thereby enhancing the output power density.

The principal constraint on both the PAE and P_{OUT} arises from the interplay between DC-to-RF dispersion and thermal influences. The dispersion, often referred to as "current collapse", is attributed to traps, leading to reductions in P_{OUT} and PAE. Additionally, pronounced self-heating within the HEMT occurs under high drain voltage, substantially affecting PAE, primarily by diminishing electron mobility. Successfully managing dispersion while simultaneously delivering substantial large signal gain at high frequencies is one of the main targets within this study.

IV. State-of-the-art

IV.1. Review of the state-of-the art GaN-on-Si vertical buffer breakdown field

As discussed previously, one of the critical limitations of the breakdown voltage in GaN-based HEMTs arises from the vertical top-to-substrate "breakdown" phenomenon, also known as vertical buffer breakdown. **Figure 1.16.a** and **Figure 1.16.b** present a benchmark of vertical buffer breakdown voltage and vertical buffer breakdown field for GaN-on-Si heterostructures, respectively, as a function of the total stack thickness. In particular, achieving high breakdown voltage generally requires the use of thick heterostructures (> 1.5 µm) (**Figure 1.16.a**). The highest reported value for the vertical buffer breakdown field is 3 MV/cm, observed with a total stack thickness of 5 µm (**Figure 1.16.b**) [90]. However, employing a thick buffer degrades the thermal dissipation and increases the cost of the epi-wafer. It is important to highlight that despite the substantial total stack thickness and numerous buffer layer optimizations, the GaN material's intrinsic breakdown field has never been reached to the best of our knowledge.

In this study, one of the primary objectives was to optimize the buffer layer to achieve a high vertical buffer breakdown field while using a sub-micron thick GaN-on-Si HEMT heterostructure.

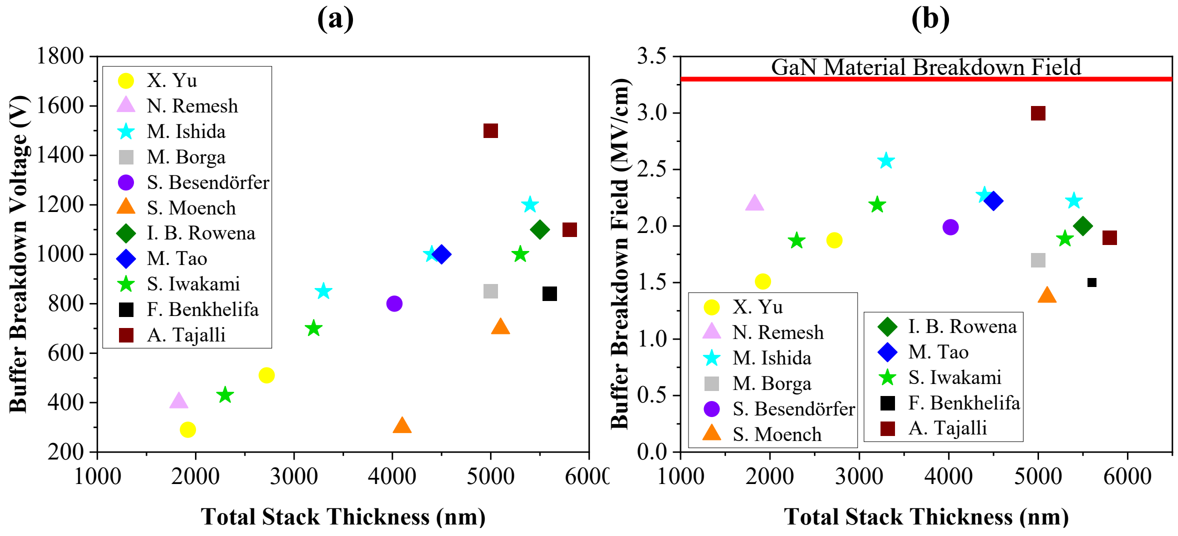


Figure 1.16.: GaN-on-Si HEMTS benchmark of (a) Buffer breakdown voltage and (b) Buffer Breakdown field as a function of the total stack thickness[90–100].

IV.2. State-of-the art of GaN-on-Si RF performances

Figure 1.17 illustrates a benchmark of PAE as a function of P_{OUT} for GaN-on-Si HEMTs within a frequency range from 2 GHz up to 90 GHz. In the sub-10 GHz range, S. Hoshi et al. reported a record P_{OUT} of 12.88 W/mm at 2 GHz using AlGaN/GaN HEMT technology with L_G = 500 nm, yielding a PAE of 64 % and a small signal gain of 19.15 dB [101]. Numerous sub-10 GHz results have been documented, featuring a P_{OUT} values exceeding 4 W/mm and an associated PAE surpassing 50 % are reported confirming the attractiveness of GaN-on-Si HEMTs for telecommunication networks such as 5G and more [101–108].

Additionally, in Ka-band R. AlKashlan recently demonstrated in CW mode AlGaN/GaN HEMTs delivering a PAE of 50 % and an associated P_{OUT} of 2.8 W/mm at 28 GHz and V_{DS} = 10 V [109]. Meanwhile, at 40 GHz, F. Medjdoub et al. obtained 2.5 W/mm and 18 % PAE using an ultrathin AlN/GaN on Si HEMTs [110].

Ongoing advanced research is pushing the boundaries to extend GaN devices to high frequency reaching W-band and beyond. These impressive RF achievements are attributed to innovative device scaling technologies. Extensive efforts have been devoted to meeting W-band requirements, including a short gate length (in the deep sub-100 nm range), high F_t/F_{max} ratio, and low contact resistances. In 2021, H.W. Then et al. presented the first W-band results for GaN-on-Si HEMTs, showcasing an output power density of 0.76 W/mm alongside a PAE of 23.6 % in CW mode at 76 GHz and an output power density of 0.4 W/mm associated with a PAE of 10.5 % in CW mode at 90 GHz [111].

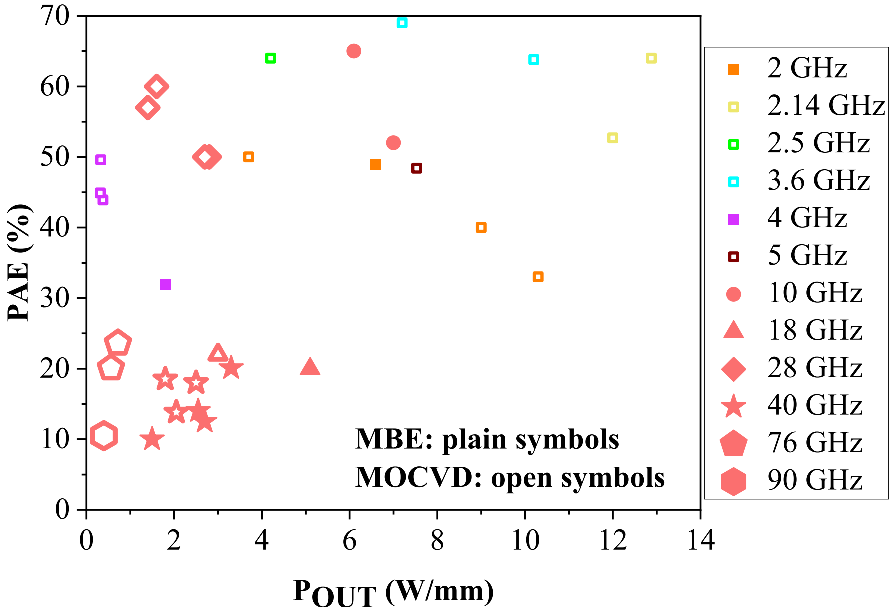


Figure 1.17.: Benchmark of state-of-the-art GaN-on-Si technologies grown by MBE vs MOCVD between 2 and 90 GHz at different operating voltages [101–122].

IV.3. Sub-micron thick GaN-based HEMT RF performances

In the last few years, sub-micron thick GaN-based HEMT have grown attention in order to improve the thermal dissipation and decrease the epi-wafer cost. Prior efforts involving a thin buffer layer have demonstrated a threading dislocation density that is twice as high [123], along with a reduced electron mobility [124, 125] when compared to a thicker buffer.

However, in 2021, J. Raychaudhuri et al. conducted a comparison between three different buffer layers with varying carbon doping concentrations for AlGaN/GaN HEMTs on SiC. Two of the buffers were thicker than 2 µm, while one was only 200 nm thick. Through their study, they discovered the possibility of achieving improved RF characteristics by using a thin buffer layer with the right composition of carbon doping optimization [126]. At the same time, Z. Liang et al. demonstrated an ultra-thin AlGaN/GaN HFET with a high breakdown voltage on sapphire substrates. They achieved a lateral breakdown voltage of 1700 V, thanks to the optimization of the buffer, which consists of a 35 nm AlN layer deposited using a physical vapor deposition (PVD) system, while the other layers were grown using MOCVD (**Figure 1.18.a**) [127]. Previously, in 2018, SweGaN demonstrated lateral and vertical breakdown voltages exceeding 1500 V for a sub-micron thick AlGaN/GaN HEMT grown on SiC using MOCVD with only an AlN back-barrier of 60 nm for the buffer (**Figure 1.18.b**) [128].

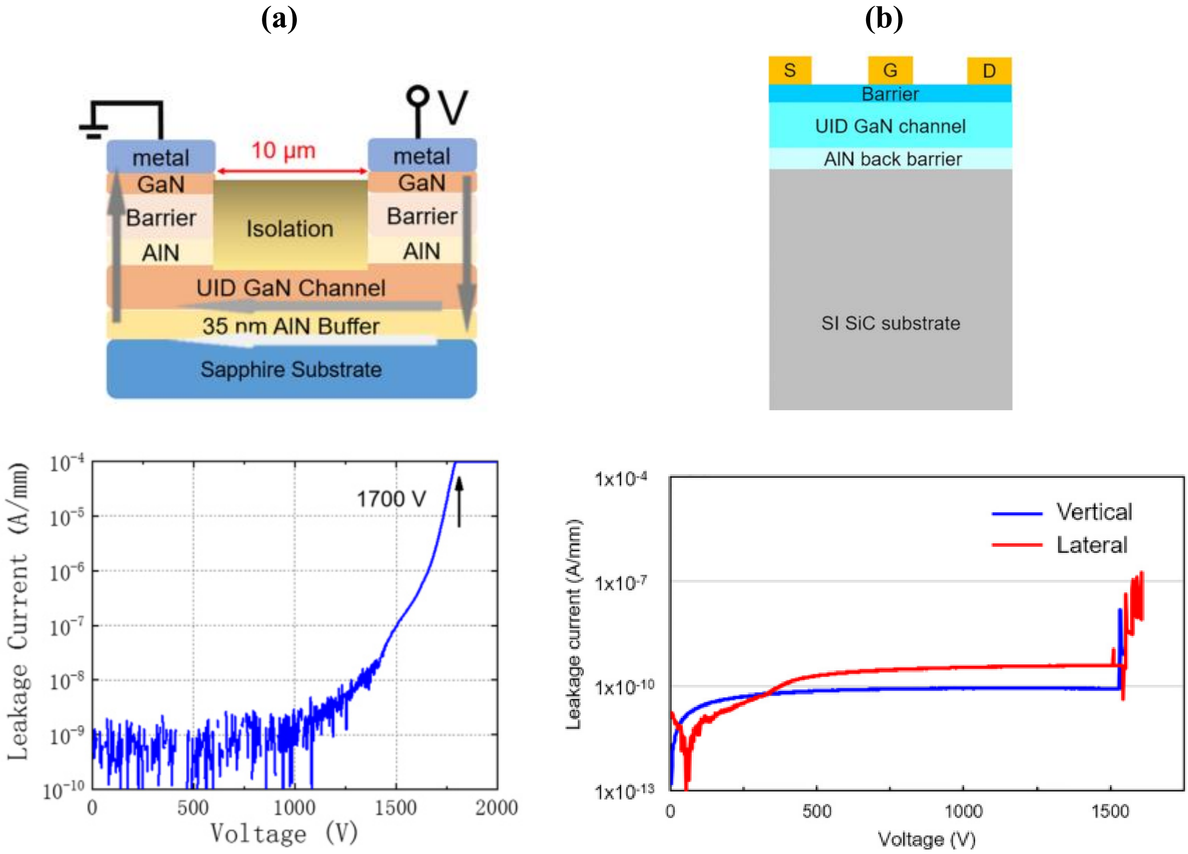
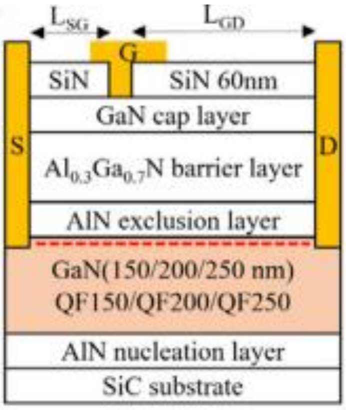


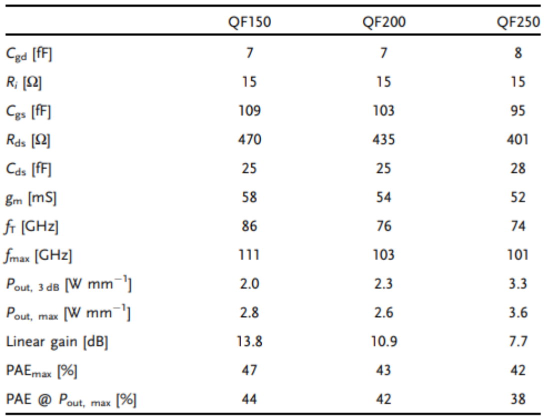
Figure 1.18.: (a) Schematic cross section of J. Raychaudhuri et al. thin AlGaN/GaN HEMT on Sapphire and associated lateral characteristic [127]. (b) Schematic cross section of the SweGaN thin AlGaN/GaN HEMT on SiC and associated vertical and lateral characteristics [128].

Moreover, more recently, SweGaN reported promising DC and RF performances of AlGaN/GaN HEMTs grown on SiC by MOCVD using their “buffer-free” or “QuanFINE” technology (**Figure 1.19.a**). With a total stack thickness of less than 1 µm and L_G = 70 nm, RF performances at 28 GHz were demonstrated, featuring a saturated P_{OUT} of 3.2 W/mm, along with a peak PAE of 40% at V_{DS} = 25 V (**Figure 1.19.c**). The improvement in this study lies in the good quality of the AlN NL, which serves both as a transition layer and back barrier, as well as the optimization of the channel thickness [55, 56].

(a)



(b)



	QF150	QF200	QF250
C_{gd} [fF]	7	7	8
R_i [Ω]	15	15	15
C_{gs} [fF]	109	103	95
R_{ds} [Ω]	470	435	401
C_{ds} [fF]	25	25	28
g_m [mS]	58	54	52
f_T [GHz]	86	76	74
f_{max} [GHz]	111	103	101
$P_{out,\ 3\,dB}$ [W mm^{-1}]	2.0	2.3	3.3
$P_{out,\ max}$ [W mm^{-1}]	2.8	2.6	3.6
Linear gain [dB]	13.8	10.9	7.7
PAE_{max} [%]	47	43	42
PAE @ $P_{out,\ max}$ [%]	44	42	38

(c)

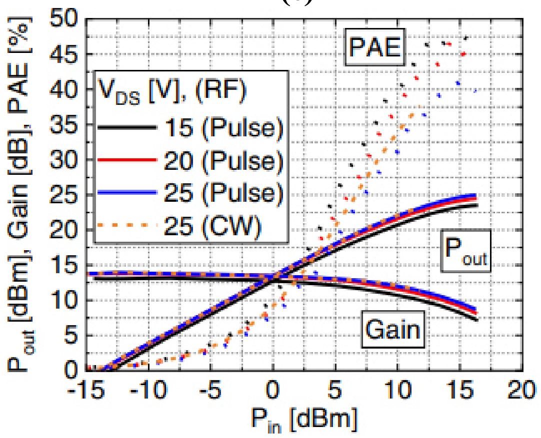


Figure 1.19.: (a) Schematic cross section of SweGaN AlGaN/GaN HEMTs grown on SiC by MOCVD with their "QuanFINE" technology and associated (b) small-Signal equivalent circuit parameters, f_T, f_{max}, and large-signal performance of HEMTs with an Lg of 70 nm and (c) load pull measurement at 28 GHz for different V_{DS} on QF150[56].

In this study, the main objective is to achieve good RF performances with sub-micron thick GaN-on-Si HEMTs. To the best of our knowledge, high RF performances achieved with sub-micron thick GaN HEMTs grown on Si substrate has never been demonstrated yet.

V. Conclusion

In this chapter, we have highlighted the exceptional potential of GaN material for high-power microwave applications. Indeed, the high bandgap coupled with good electron mobility make this material the ideal candidate for the realization of robust transistors and related integrated circuits. This paves the way for unprecedented performance in the millimeter-wave range. Furthermore, we have highlighted the presence of numerous global industrial and academic players creating an ecosystem focused on GaN technology. This clearly demonstrates the interest and significance of this material for high-frequency power applications. Subsequently, we have presented the figures of merit through the HEMT transistor and the corresponding state of the art. Nevertheless, limitations still exist, preventing the exploitation of the full potential that GaN could offer.

In this context, the main focus of this work is to develop sub-micron thick GaN HEMT devices on Si grown by MBE capable of delivering a combination of high power/high efficiency operating in the millimeter-wave range.

Chapter 2: Device fabrication and electrical characterization methods for GaN HEMTs

I. Introduction

In chapter 1 the intrinsic advantages associated with the use of GaN material and the limitations for the design and performance of GaN-based HEMTs were discussed. These advantages can be demonstrated through a proper selection of the heterostructure and technological parameters. **Figure 2.1** illustrates the challenges that must be addressed, spanning from epitaxial growth structure to device fabrication. In particular, at higher frequencies, the efficiency of GaN HEMTs remains limited, primarily due to the lack of power gain, enhanced trapping effects, and reduced electron confinement and self-heating when scaling down the device dimensions. Consequently, GaN HEMTs are improving owing to the optimization of epi-structure design and associated process technology. These optimizations are essential for mitigating issues related to dispersion and trapping effects, thereby enabling superior transistor performance.

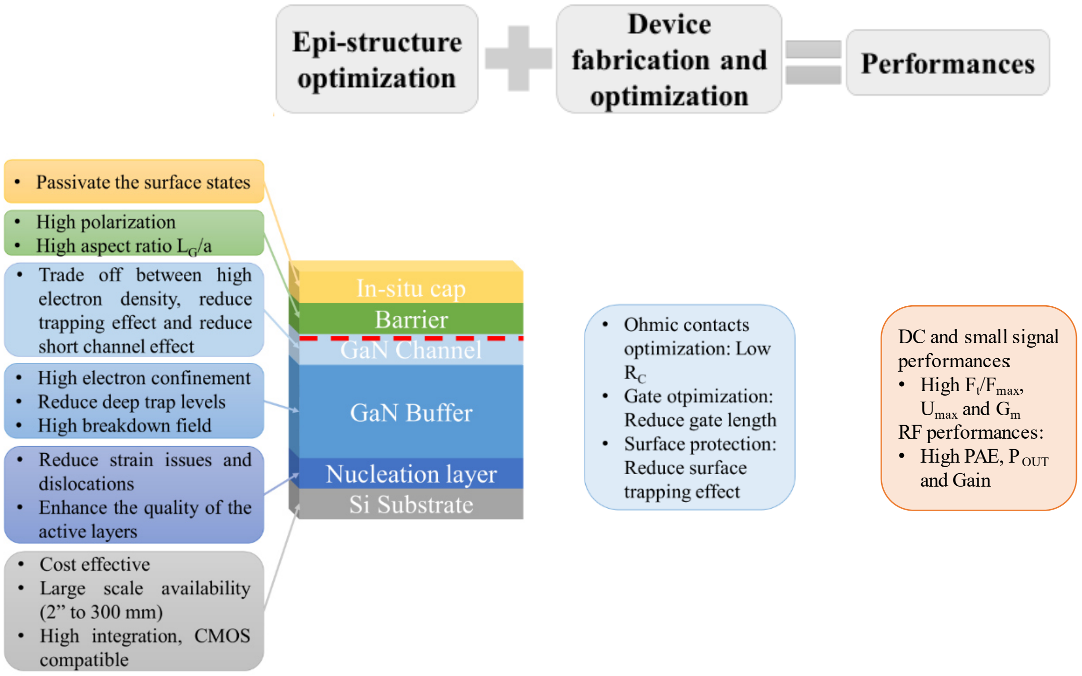


Figure 2.1.: Overcoming challenges from epitaxial structure to device fabrication for high performance achievement.

In the first part of this chapter, an overview of the essential technological steps for fabricating GaN-on-Si HEMTs for high-frequency operation are presented. The chapter will delve into processing development, the mask sets employed during device fabrication, and the characterization control monitoring during the fabrication. In the second part of this chapter, various electrical characterization techniques employed for assessing the main figures of merit are detailed. This section also covers the device characterization tools and measurement protocols established within this framework. It is worth noting that the processing and characterization of GaN HEMT devices were conducted at IEMN while epilayers have been grown by the company EasyGaN.

II. Technological process

The fabrication process of HEMTs took place in the cleanroom facilities from IEMN laboratory. While the epitaxial structures used were different, the fabrication process remained relatively consistent for each of them. The process flow is depicted in **Figure 2.2**. The optimization of some of the processing critical steps for high frequency operation are more detailed such as the fabrication of ohmic contacts and the gate module. The HEMTs investigated within the scope of this work use a standard configuration, featuring two gate fingers, two source contacts, and a drain contact, as illustrated in **Figure 2.2 (e)**.

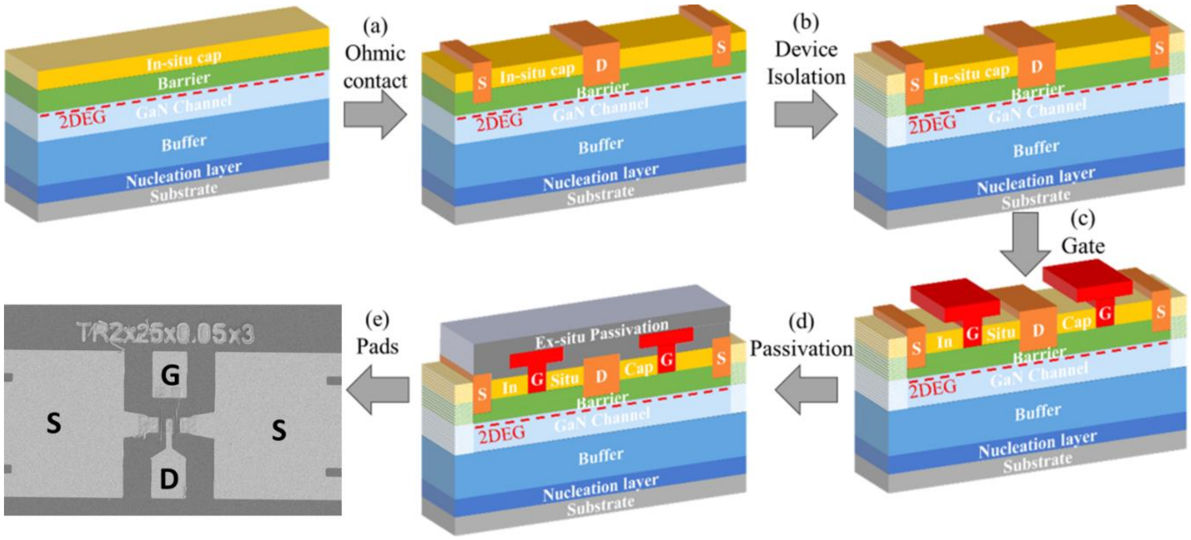


Figure 2.2.: (a-d) Process flow schematic of GaN transistor fabrication and (e) SEM image of the final transistor obtained using e-beam processes.

The fabrication of a complete HEMT device may involve six different processing steps as follow:

Alignment marks: Mark patterns play a crucial role enabling the alignment of various fabrication steps, given that each device typically involves multiple patterns or fabrication levels. The accurate alignment of patterns used in different lithography steps, which collectively constitute a single device, is vital to guarantee proper device operation. In the context of E-beam lithography-based HEMT fabrication, the process necessarily starts with the creation of alignment marks. These marks allow the precise positioning of the electron beam during the creation of various mask patterns for each step. The theoretical resolution of electron beam writing (E-beam) is in the order of 5 nm. The marks can be either etched or metallized. In our case, metallized marks were selected. Metallization is deposited by evaporation of a Mo/Ni/Mo metal stack (20/40/70 nm). Molybdenum (Mo), a refractory metal with a high melting point of 2617 °C, is chosen for this purpose. Mo is well-suited as it maintains sharp edges and low surface roughness throughout the fabrication process, ensuring precise alignment of the electron beam. An intermediate Nickel (Ni) layer (melting temperature of 1450 °C) is sandwiched between two Mo layers to mitigate the strain caused by Mo. Thicknesses have been optimized to achieve the necessary contrast between the mark surface and the sample surface, facilitating the accurate detection of alignment marks by the electron beam tool. **Figure 2.3** presents a SEM image of a metallized mark with 8 µm × 8 µm square patterns.

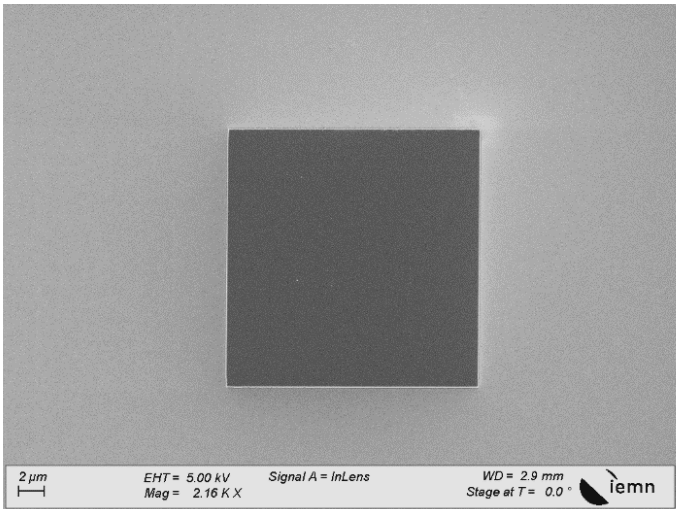


Figure 2.3.: SEM image of alignment mark with square patterns measuring 8 µm on each side..

(a) Ohmic contacts: In this step, low-resistance source and drain ohmic contacts with the 2DEG are formed. This ensures a high maximum drain current density, a reduced on-resistance and a high extrinsic transconductance enabling high F_t and F_{max}. However, establishing ohmic contacts on GaN-based materials can be quite challenging due to the wide bandgap, which naturally favors Schottky-type contacts. To attain high performance in GaN-based HEMTs, it is essential to minimize contact resistance (R_C) while maintaining low surface roughness and sharp edges. Factors like the work function and thickness of metal layers, the annealing temperature, the barrier layer etching, and more, play a crucial role in such optimization. The ohmic contacts are produced using a 'Lift-Off' process technique, commonly employed for III-V components. Once the patterns are defined, either via e-beam lithography or optical lithography, depending on the chosen process, the barrier layer is partially etched with a BCl_3/SF_6 plasma in an Inductively Coupled Plasma (ICP) reactor prior to metallization. Alternatively, the metal stack may be deposited directly on top of the barrier, depending on the barrier's thickness. Subsequently, a Ti/Al/Ni/Au stack is deposited via metallic evaporation, and any excess metal over the resist is removed via Lift-Off. A high-temperature annealing step is then performed to reduce the contact resistance. Further details on optimizing ohmic contacts will be provided in the following sections.

(b) Device isolation: Device isolation constitutes a crucial step in the HEMTs manufacturing process, properly defining the active area of each transistor, which serves as the ideal pathway for electron flow from the source to the drain. This process effectively isolates transistors, thereby reducing leakage currents between adjacent transistors. This boundary is established by insulating the 2DEG and the region below, typically few hundreds of nm. This can be carried out in two different methods: by deep etching using ICP (mesa technology) or by ion implantation using argon, nitrogen, helium or oxygen. Within the framework of this thesis, ion implantation using nitrogen atom was used. The energies and implantation doses were optimized in order to break the crystalline structure of the implanted material and to make the semiconductor amorphous thus preventing any parasitic conduction.

(c) Gate: Gate fabrication is essential to reach high-frequency transistor performances. Optical lithography is employed to define the large gate lengths (above 1 µm) for quick material evaluation, while e-beam lithography is used to define the short T-gate footprint. Following this, anisotropic SiN cap layer etching is conducted, followed by the deposition of a Ni/Au metal stack on top of the barrier layer to create a Schottky contact. The gates are then formed through a lift-Off process. Reducing the gate length leads to an increase of the transistor performances, in particular F_t and F_{max}. Therefore, it is imperative to achieve gate lengths below 100 nm in this project, making the optimization of the gate process technology, particularly the SiN cap etching, a critical requirement.

(d) Passivation: The presence of surface states in AlGaN and GaN materials has been pinpointed as the underlying cause of drain current collapse and related reliability issues, presenting a significant challenge in the manufacturing of high-performance AlGaN/GaN HEMTs. These surface states can originate from surface-bound dangling atomic bonds, surface growth defects, plasma-induced damage during processing, foreign contaminants, and more. Consequently, optimizing surface passivation is key to electrically deactivate these states and thereby alleviate their detrimental impact on device performance. In this study, a 200 nm Si_3N_4 passivation layer, deposited via Plasma Enhanced Chemical Vapor Deposition (PECVD), is employed.

(e) **Pads:** The final HEMTs fabrication process consists in thickening the pads, allowing electrical characterization of the device by providing access to the 3 terminals (gate, source and drain) for device characterization purposes. Optical lithography is employed to define the pads. Subsequently, the SiN passivation layer is etched using Reactive Ion Etching (RIE) SF_6 plasma. Following this, a Ti/Au metallization is deposited through evaporation, followed by a lift-Off process. A SEM image of both final optical and e-beam transistor is presented in **Figure 2.2.e**.

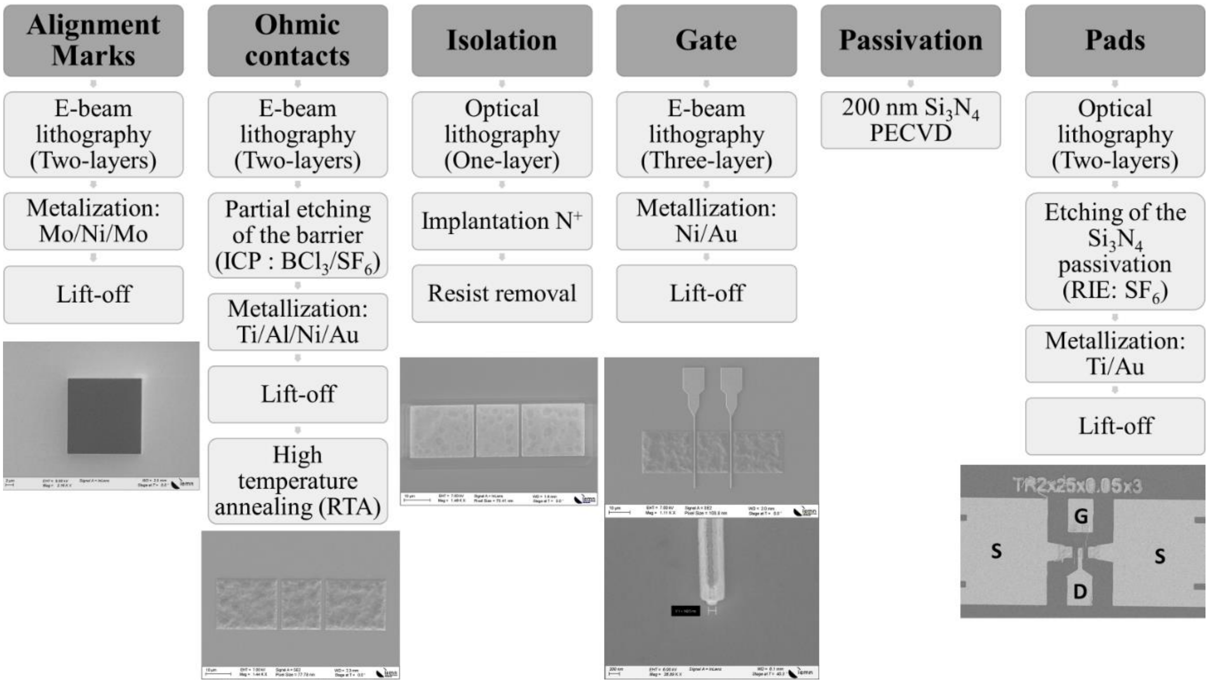


Figure 2.4.: E-beam process flow for GaN HEMTs.

II.1. Mask layouts description

The fabrication of transistors was organized into two stages. Initially, a quick evaluation loop of the epitaxial structures was required to determine their suitability for the fabrication of high-frequency short e-beam devices, which is both expensive and time-consuming. During this initial phase, various parameters, such as the 2DEG properties of the heterostructure (e.g., carrier concentration and mobility), DC characteristics (maximum drain current, threshold voltage, transconductance) and breakdown field (lateral and vertical breakdown, three-terminal off-state breakdown), were extracted through a similar, albeit quicker process, typically involving larger gate lengths (approximately 3 µm). This evaluation was conducted using an optical layout design known as "BreakUp" (**Figure 2.5**), which exclusively includes optical photolithography steps. This approach enabled the detection of issues related to the epitaxial structures that could significantly impact the device operation, such as excessive gate leakage or poor electron mobility.

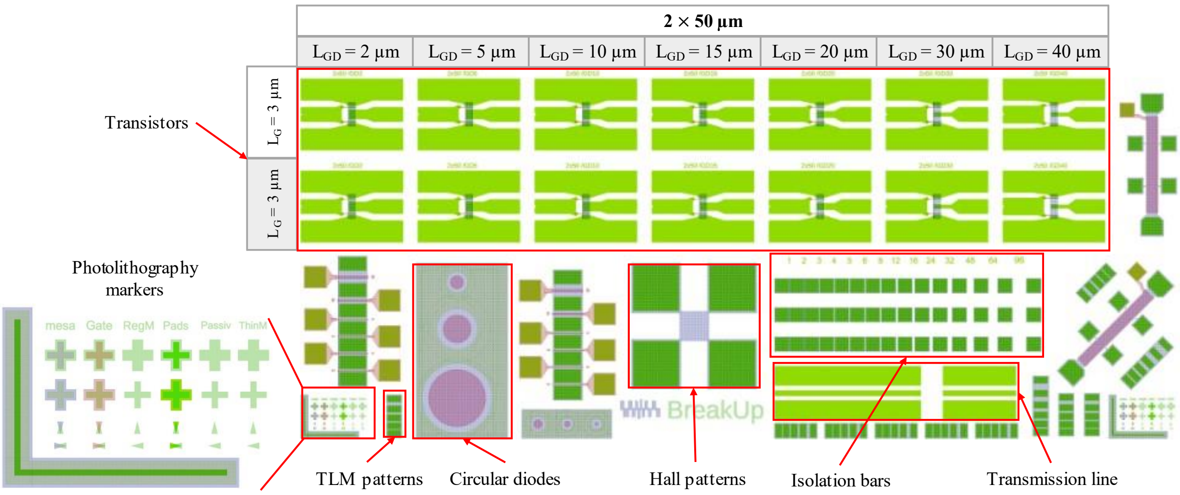


Figure 2.5.: Design layout of "BreakUp" for optical GaN HEMT fabrication.

Once the evaluation of the epitaxial structures yielded satisfactory results, these structures were then employed in the fabrication of high-frequency transistors, using a more advanced processing approach that involved electron-beam lithography as seen in **Figure 2.4**. **Figure 2.6** illustrates the complete transistor layout design, denoted as "GaN FAST," used in this work. This layout encompassed three e-beam lithography steps (alignment marks, ohmic contacts, and the gate module) and two optical photolithography steps (isolation and pads). The primary advantage of using e-beam lithography is the ability to achieve high-resolution patterns, allowing for sub-100 nm short gate lengths suitable for high-frequency operation. Nonetheless, it is worth noting that this technique presents some drawbacks, including high costs and a time-consuming processing timeline.

The "BreakUp" and "GaN FAST" layout exhibit similar designs, incorporating a collection of process control monitor patterns (PCMs), alignment marks, and transistors with diverse designs. In the lower section of both mask sets, a series of PCMs is featured, enabling the extraction of electrical parameters pertaining to the epitaxial structure and the monitoring of various processing steps. Transmission Line Measurement (TLM) patterns are employed to gauge the maximum current density and measure contact resistances. The Hall pattern serves to obtain the values of the 2DEG density, electron mobility, and sheet resistance within the heterostructures. Circular diodes reveal the quality of Schottky gate contacts, while simultaneously providing leakage current in reverse-biased diodes. The isolation process can be controlled and verified by measuring leakage current between two isolated contact bars with various distances. Lastly, transmission lines are utilized to assess the RF losses of the epitaxial structure.

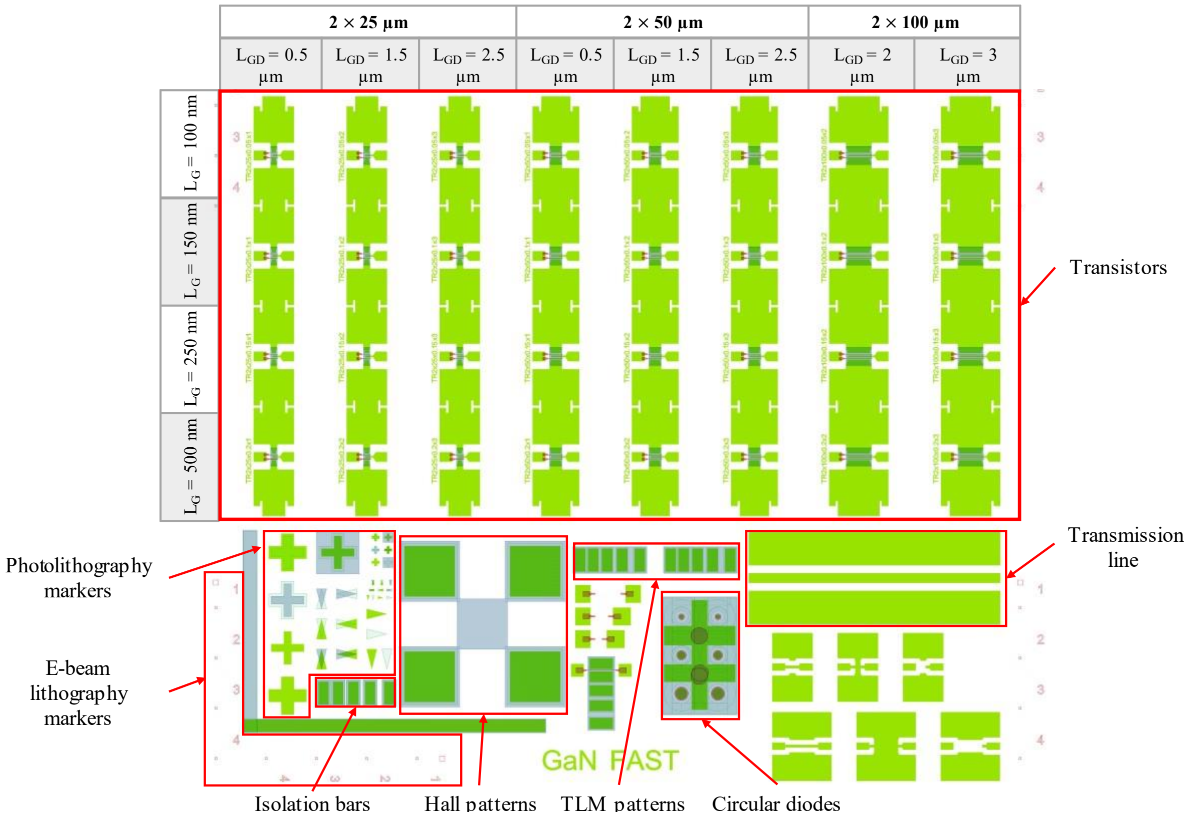


Figure 2.6.: Design layout of "GaN FAST" for e-beam GaN HEMT fabrication.

In the upper section of both layouts, various transistor designs can be found. In the "BreakUp" layout, two identical rows of transistors are available, with a variation of the gate-to-drain distance (L_{GD}) ranging from 2 µm to 40 µm, while maintaining a constant gate width (W_G) of 2×50 µm, gate length (L_G) of 3 µm, and gate-to-source distance (L_{GS}) of 0.5 µm, as depicted in **Figure 2.5**. In the case of the "GaN FAST" layout, there are eight columns of transistors, offering three different W_G options: 2×25 µm, 2×50 µm, and 2×100 µm, as shown in **Figure 2.6**. Within each column, there are four transistors, featuring two gate fingers and L_G ranging from 100 nm to 500 nm. L_{GD} varies between 0.5 µm, 1 µm, and 1.5 µm, while L_{GS} remains constant at 0.5 µm. It is important to note that L_G can be easily modified and adjusted in the mask layout of “GaN FAST” since this step is defined through e-beam lithography and not a hard mask.

II.2. Optimization of device processing technology

The fabrication process of GaN HEMTs necessitates the optimization of particular steps to enhance device performance in order to take full advantage of the benefits offered by the heterostructures. This section presents a comprehensive overview of the main adjustments, modifications, and improvements made during the process. The primary focus of optimization lies in the steps that entail the establishment of a metal-semiconductor contact, whether Schottky or ohmic. Schottky contacts naturally form at the metal-semiconductor interface and are commonly employed as gate contacts in GaN HEMTs. While the Schottky barrier height depends significantly on the metal's work function, GaN HEMTs typically require a high Schottky barrier. Additionally, in the GaN material system, a Schottky contact can transition into an ohmic contact after a high temperature annealing due to metal alloy inter-diffusion within the barrier layer. In such cases, metals with low Schottky barrier heights in the range of 0.4-0.5 eV are needed to create high-quality ohmic contacts.

II.2.a. Ohmic contact optimization

Reducing ohmic source and drain contact resistances with the 2DEG is of utmost importance, given its direct influence on the device's ON-state performance. An ohmic contact is defined as a metal / semiconductor contact exhibiting a linear and symmetric current-voltage (I-V) characteristic. This contact is considered ohmic when the metal's work function is higher than that of the semiconductor. It is necessary to achieve good ohmic contacts to minimize the value of access resistances, which can hinder the performance of high-frequency power components. The cumulative resistances contributing to the overall access resistances are outlined in **Figure 2.7**. A first contribution is related to the metal / barrier layer interface ($R_{CMetal/Barrier}$) and does not depend on the heterostructure properties. The two other components are correlated to the barrier thickness ($R_{CBarrier}$) and to the 2DEG properties (R_{C2DEG}). The total resistance between two contacts can be defined as follows [129]:

$$R_T = 2\frac{R_C}{W} + L\frac{R_{Sh}}{W}$$ **Equation 2.1**

Where R_C represents the contact resistance, W the contact length, L the distance between contacts, and R_{Sh} represents the sheet resistance.

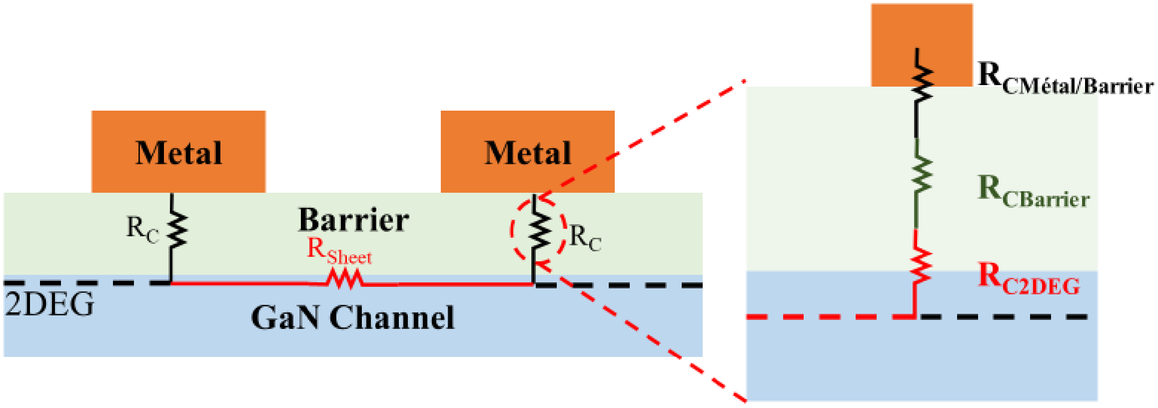


Figure 2.7.: Scematic illustration of the various resistances between two ohmic contacts in an AlGaN/GaN HEMT.

The optimization of the metal stack to achieve the lowest possible contact resistance on GaN-based heterostructures has been the subject of numerous studies [129–135]. This optimization has resulted in a metal stack, with thicknesses of 12/200/40/100 nm, composed of Ti/Al/Ni/Au, followed by a rapid thermal annealing (RTA) process that promotes alloy formation, thus reducing contact resistance [129, 136–138]. Titanium (Ti) serves as an adhesion layer and is responsible for the formation of the TiN alloy at the metal / semiconductor interface after RTA [130, 139–142]. This alloy possesses a lower work function than AlGaN, which facilitates the electron flow through thermionic emission. The formation of this alloy induces nitrogen vacancies within the AlGaN barrier, which behave as donors [143, 144]. The deposition of the aluminum (Al) layer results in the formation of a Ti-Al alloy, reducing reactivity between titanium and GaN [145–148]. This reduction limits the formation of voids at the interface caused by gallium migration, which would otherwise increase the contact resistance. To prevent the formation of compounds between the gold layer and aluminum that could make the contact brittle and cause short circuits, a nickel (Ni) layer is deposited. Finally, to evenly spread the current across the entire contact surface, a layer of gold (Au) with excellent electrical conductivity is applied, which also serves to prevent surface oxidation.

In the context of this thesis, two different barrier layers have been investigated: AlGaN and AlN. When dealing with an AlGaN barrier layer with a thickness ranging from 14 to 20 nm, a partial recess of ohmic contacts was performed prior to metallization using BCl_3/SF_6 plasma in an ICP reactor. This etching step is crucial for bringing the metal stack closer to the 2DEG without compromising the integrity of the GaN layer, as shown in **Figure 2.8.a** [129, 149]. As depicted in **Figure 2.8.b**, inadequate etching results in non-ohmic contacts. An optimal contact resistance is achieved when approximately 75% of the barrier layer is etched [150]. In contrast, when dealing with an AlN barrier layer with a thickness of less than 10 nm, ohmic contacts are directly formed on the barrier layer, as illustrated in **Figure 2.8.c**.

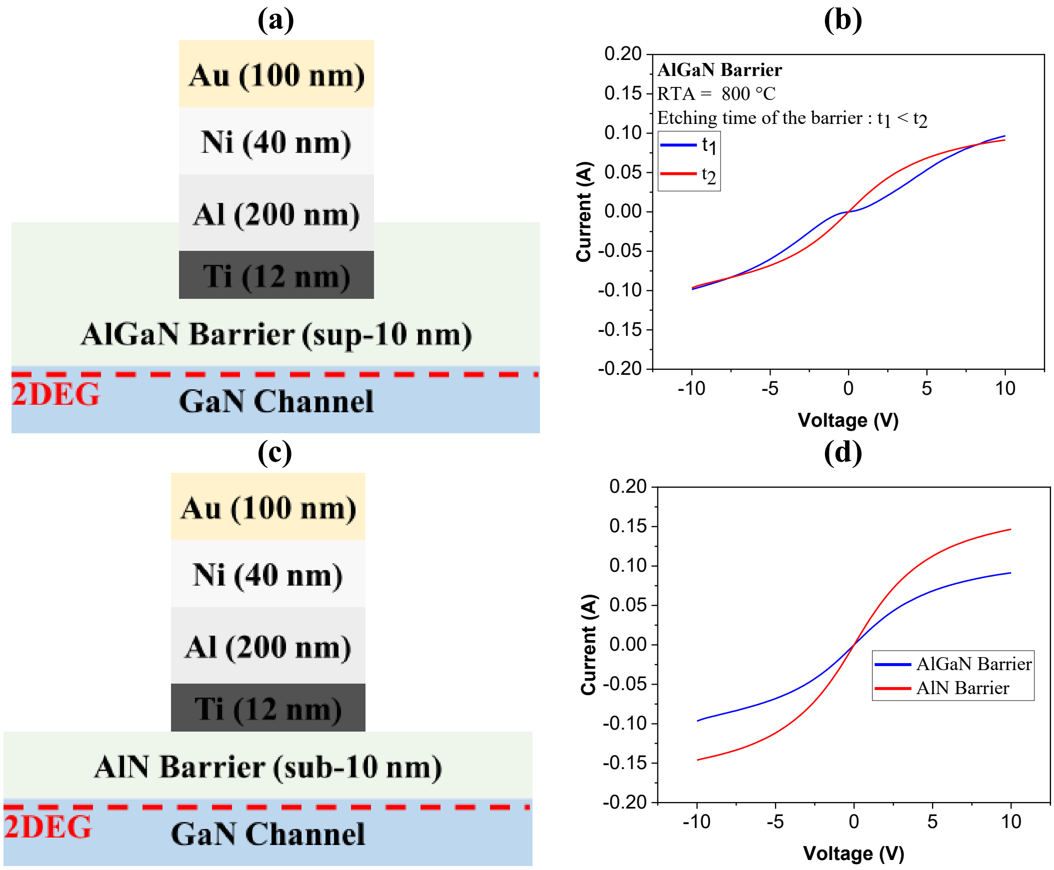


Figure 2.8.: (a) Partially recessed Ti/Al/Ni/Au ohmic contacts on AlGaN/GaN structures and (b) I-V measurements comparison of different etching time of AlGaN barrier layer. (c) Non-recessed Ti/Al/Ni/Au ohmic contacts on AlN/GaN structures and (d) I-V measurements comparison for AlGaN and AlN barrier.

The quality of ohmic contacts can be assessed through Transmission Line Method (TLM) test patterns, as depicted in **Figure 2.9.a**. These patterns consist of rectangular metal contacts with varying spacings of 2 µm, 5 µm, 10 µm, and 20 µm. In these patterns, W represents the contact width, and L represents the contact length. To assess the ohmic behavior of contacts, I-V characteristics are analyzed through a two-probes measurement, sweeping a voltage range from -10 V to +10 V. **Figure 2.9.b** illustrates the I-V characteristics for various contact spacings. The current density measured between two contacts separated by 5 µm for structures with AlN and AlGaN barriers is shown in **Figure 2.8.d**. The high current density measured for AlN barrier structures reflects the high electron density in the channel for these structures.

Furthermore, four-probe measurements enable the extraction of contact resistances. This measurement involves determining the total resistance between two adjacent contacts, with the current flowing through the semiconductor from one contact to another. Ohmic contact resistance and semiconductor sheet resistance can be extracted through linear regression analysis of the total resistance as a function of the contact spacing (d_x), as illustrated in **Figure 2.9.c**. The slope of the linear fit provides R_{Sh}, while the intercept with the y-axis yields R_C. Additionally, the current transfer length (L_T), obtained from the intersection with the x-axis, represents the average distance electrons (or holes) travel in the semiconductor beneath the contact before entering the contact.

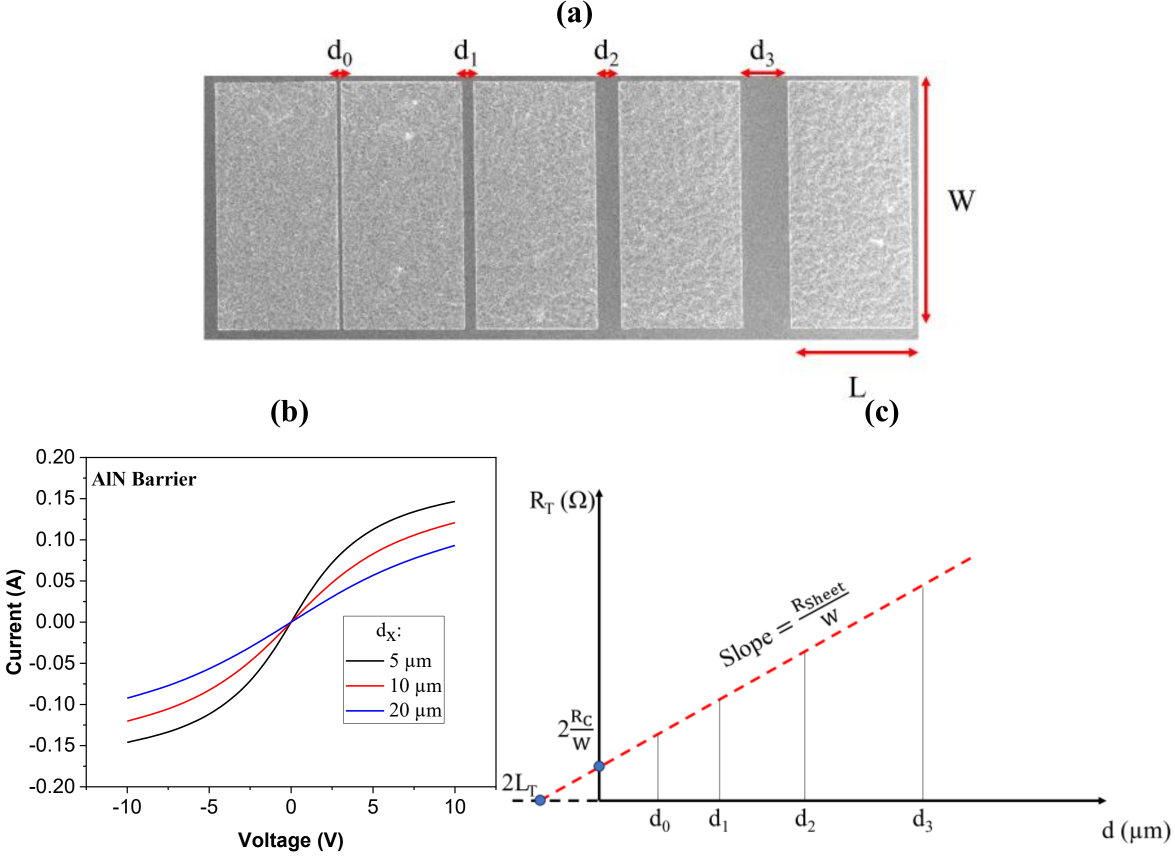


Figure 2.9.: (a) Transmission Line Method test pattern, (b) I-V measurement as a function of contact spacing d_x and (c) plot of total resistance as a function of contact spacing d_x.

Furthermore, it is important to specify that the annealing temperature is an essential parameter [129]. As shown in **Figure 2.10.a**, a set of I-V measurements between two TLM contacts spaced 5 µm apart is presented for various annealing temperatures within the same epitaxial structure. For a given stack and structure, an optimal temperature can be found corresponding to the minimum contact resistance as depicted in **Figure 2.10.b**.

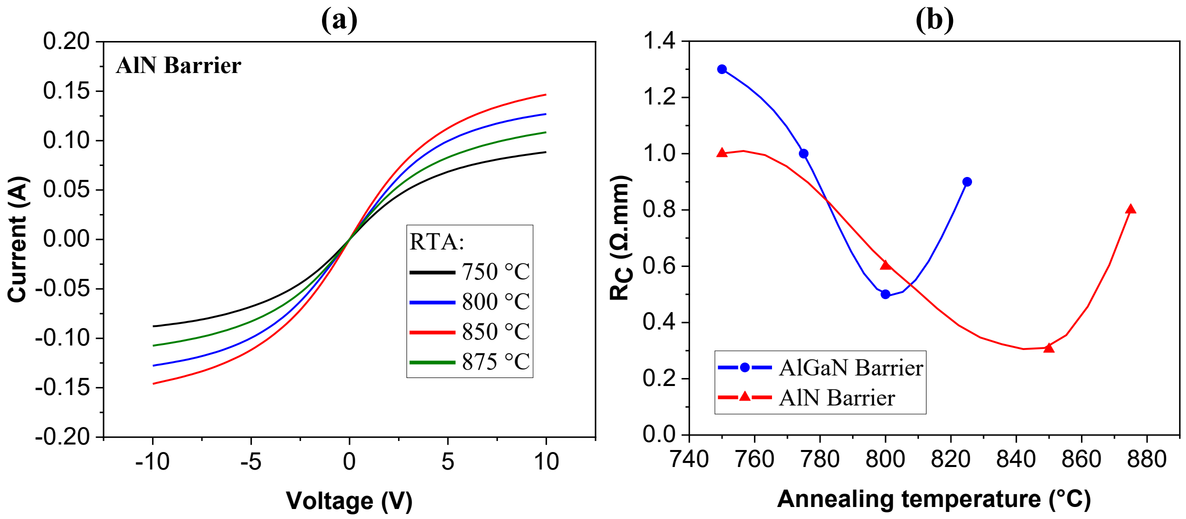


Figure 2.10.: (a) I-V characteristic between two TLM contacts spaced 5 µm apart and (b) contact resistance R_C as a function of the annealing temperature.

II.2.b. Gate Schottky realization

After completing the fabrication steps for ohmic contacts and device isolation, the critical and decisive phase of Schottky gate fabrication takes place. This phase is essential in achieving a component with robust electrical and high-frequency performance. A Schottky contact represents a metal / semiconductor junction where the semiconductor's work function is lower than that of the metal. In this work, the Schottky contact is formed using a Ni/Au metal stack. With a barrier height typically ranging from 0.66 to 1 eV, a Schottky contact is established through the direct deposition of Nickel (Ni) onto the semiconductor barrier. Nickel is selected for its strong adhesive properties and its ability to maintain a reasonable Schottky barrier height, while the subsequent deposition of gold further enhances the electrical contact.

Prior to metallization, a surface treatment is essential to deoxidize the barrier surface, guaranteeing the proper adhesion of Ni/Au. Moreover, in the context of our work, whether utilizing a GaN or SiN cap, a pre-passivation step involving the deposition of a 20 nm Si_3N_4 PECVD layer after creating ohmic contacts is carried out. This protective layer safeguards the surface and mitigates the surface leakage current or trapping effects. Consequently, SiN must be etched to enable the gate deposition on top of the barrier layer. To maintain short gate lengths while avoiding impurities at the gate/barrier interface, the chosen etching technique was optimized. To meet these demands, an ICP-RIE physical/chemical etching process that involves highly selective SF_6 plasma was developed. This technique produces an anisotropic SiN layer etching profile, ensuring reduced gate lengths while minimizing the implantation of fluorine ions during the etching process. ICP etching is exceptionally sensitive to external conditions, including chamber cleanliness and the type of support used during etching. Before SiN etching, the ICP chamber undergoes thorough cleaning and preconditioning to maintain a stable etch rate. To prevent the over-etching of the resist mask, a low RIE power etching method is used to reduce the physical etching, favoring a less damaging chemical etching process. Furthermore, an etching cycle process is performed to ensure uniform and controlled etching, thereby limiting the degradation of the surface state. It is important to point out that for the structures with a GaN cap, the gate is deposited directly on GaN.

Optical lithography is employed to define gate length L_G of 3 µm. As seen in **Figure 2.11**, the gate is positioned between the drain and source contacts. Breakdown voltage increases nonlinearly with L_{GD}. However, a shorter L_{GD} enables reaching higher current levels, as access resistances are inversely proportional to L_{GD}.

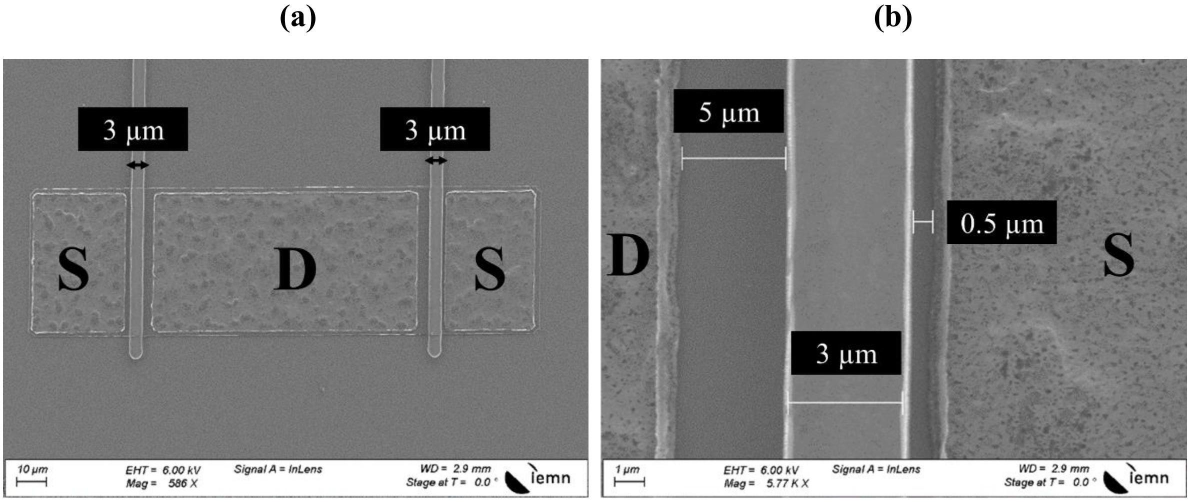


Figure 2.11.: SEM images of optical transistor with L_G =3 µm, L_{GD} = 5 µm and L_{GS} = 0.5 µm.

As explained previously, to achieve shorter gate lengths, T-shaped gates are employed with e-beam processing. As depicted in **Figure 2.12**, an e-beam lithography technique utilizing a PMMA-type three-layer resist is employed, followed by SiN PECVD layer etching to define the gate structure. Finally, the gate is metallized with a Ni/Au (20/400 nm) metal stack.

T-shaped gates are used in order to reduce both the gate resistance and parasitic capacitances especially when using shorter gate length. This technological process combined with high quality ohmic contacts leads to increased F_t/F_{max} and maximum drain current thus improving the device performance. Different gate lengths varying between 70 to 500 nm have been implemented in order to study the impact on the device performances. **Figure 2.13** shows a SEM tilted image of a 140 nm T-gate and the corresponding FIB cross section.

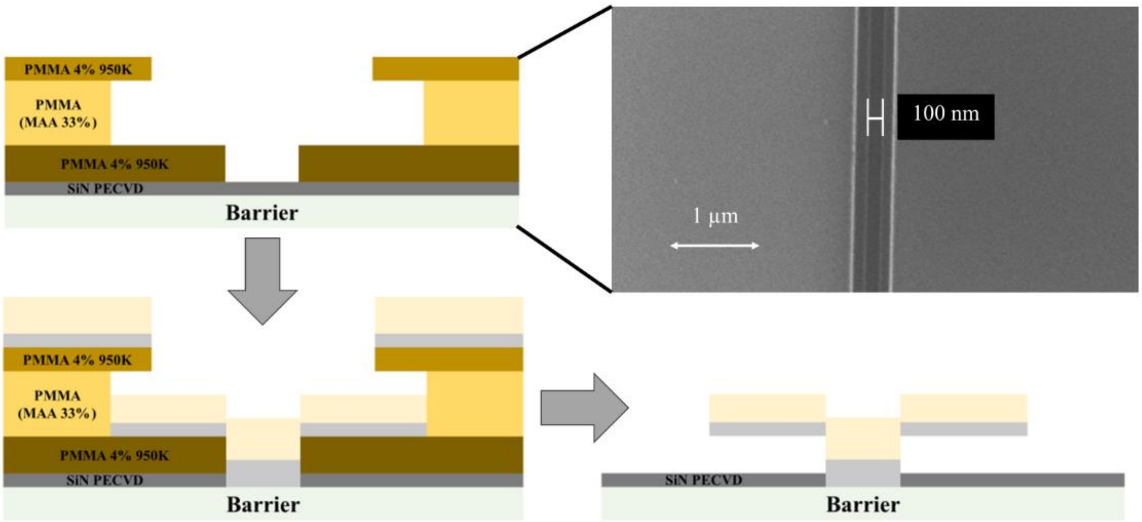


Figure 2.12.: Schematic representation of T-gate fabrication process with a SEM image top view of the tri-layer resist pattern opening.

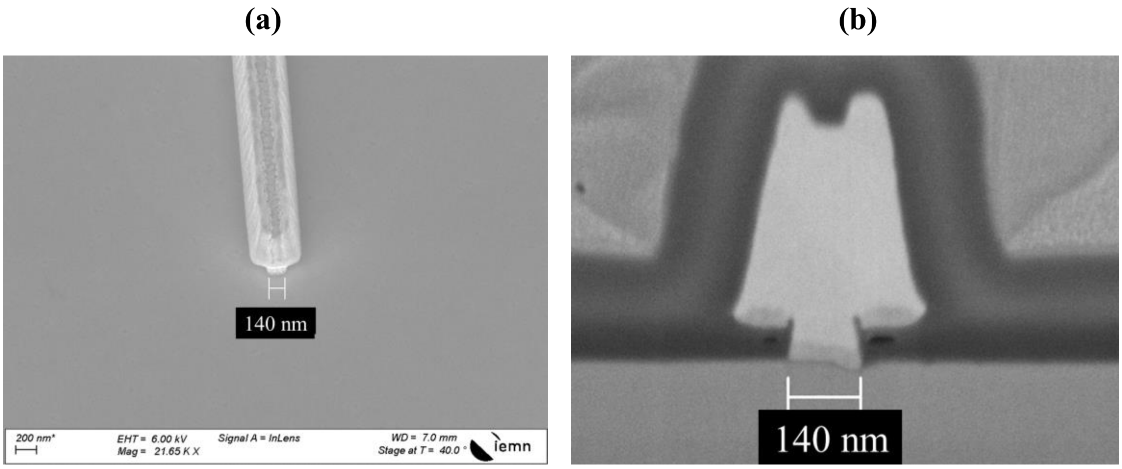
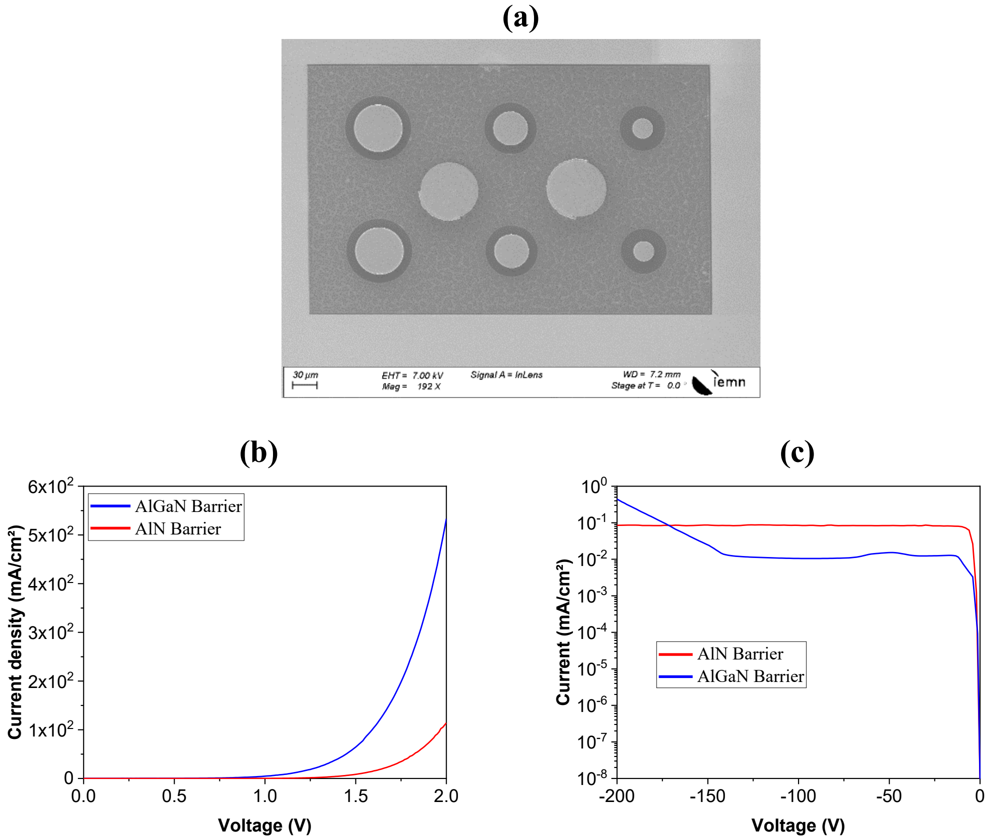

(a) **(b)**

Figure 2.13.: (a) SEM tilted image of T-gate and (b) corresponding FIB cross section image.

The quality of the Schottky contacts can be assessed through electrical characterizations of circular diodes. These measurements are used to evaluate the Schottky contacts and to detect any problems that could be caused by the fabrication process. **Figure 2.14** shows 30 µm diameter diode characteristics for structures with an AlN and AlGaN barrier layer. When a positive voltage is applied to the diode (diode-forward characteristics), the metal/semiconductor Schottky barrier is reduced, which results in an exponential increase of the current from a threshold voltage corresponding to the barrier height as shown in **Figure 2.14.b**. The threshold voltage of AlN/GaN structure (1.5 V) is usually higher than that of AlGaN/GaN (1 V) structures due to the higher Schottky barrier height with AlN barrier layer. Electrical characteristics of the reverse diodes are performed in order to detect any residues or contamination at the metal/semiconductor interface, which is reflected by the degradation of the reverse leakage current. **Figure 2.14.c** shows the leakage current of the reverse diodes for structures with an AlN and AlGaN barrier layer.


(a)

(b)

(c)

Figure 2.14.: (a) SEM image of circular diodes in optical and e-beam processing, (a) electrical characteristics of forward-diodes and (c) reverse diodes.

III. Electrical characterization of the devices

To evaluate and enhance the performance of HEMT devices, a series of characterization studies were conducted following a specific measurement protocol to extract key performance indicators. These tests utilized various equipment and benches provided by IEMN. The transistor characterization procedure depends on the process fabrication employed as shown in **Figure 2.15**. The transistor characterization procedure starts with the DC characterization in both cases. For optical transistors, DC, lateral and vertical breakdown voltage and pulsed characterizations are performed, while for e-beam transistor extensive small and large signal characterizations are carried out. The whole measurements have been carried out at IEMN characterization platform (CHOP) with the aim of evaluating the performances of transistors and identifying undesirable effects, which can be at the origin of issues such as short channel effects, robustness limitations as well as trapping effects. It can be pointed out that many types of other devices are measured with these benches and directly comparable.

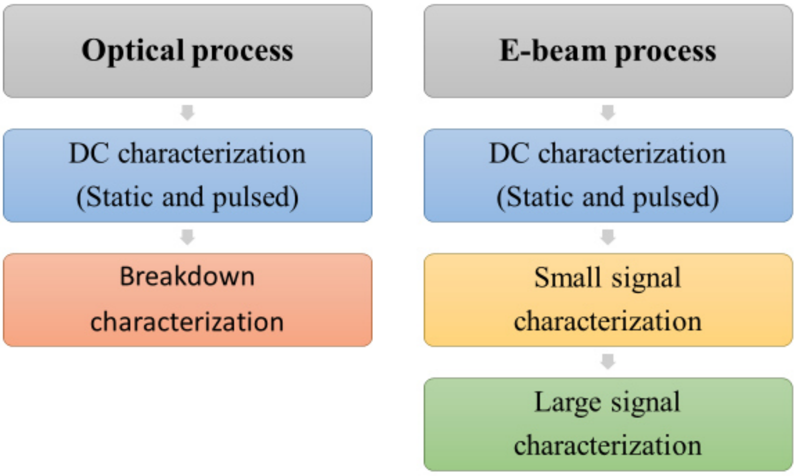


Figure 2.15.: *Transistor characterization procedure depending on the process fabrication.*

III.1. Breakdown voltage characterization

Breakdown voltage characterizations are performed using a Keysight B1505A high-voltage (HV) parameter analyzer bench available at IEMN (**Figure 2.16**). This bench allows voltage/current measurements up to 10kV/20A at room temperature. The electrical characteristics of the structures are examined through various types of measurements: lateral, vertical and three terminal off-state transistor. This specific measurement set-up was employed to evaluate and compare the various buffers during the optimization phase of the buffer study.

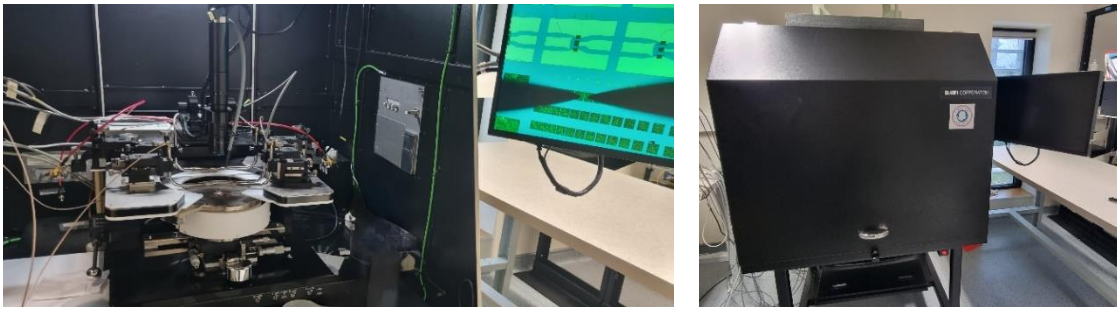


Figure 2.16.: *Photos of High-Voltage measurement bench at IEMN.*

III.1.a. Lateral breakdown voltage

The lateral breakdown voltage is measure between two isolated ohmic contact as depicted in **Figure 2.17.a**. Different spacing between two isolated contacts are used. In particular, on a silicon substrate, the breakdown voltage consistently saturates for wider contact spacing. Indeed, at a sufficiently high energy level, the space charge region reaches the silicon substrate, leading to parasitic conduction responsible for the breakdown [151]. With such spacings, the electric field propagates all the way down to the substrate so that any regions within the buffer layer can contribute. In the sub-micron thick structure study within this thesis, it has been observed that the breakdown voltage saturates for contact spacings as low as 5 µm (**Figure 2.17.b**).

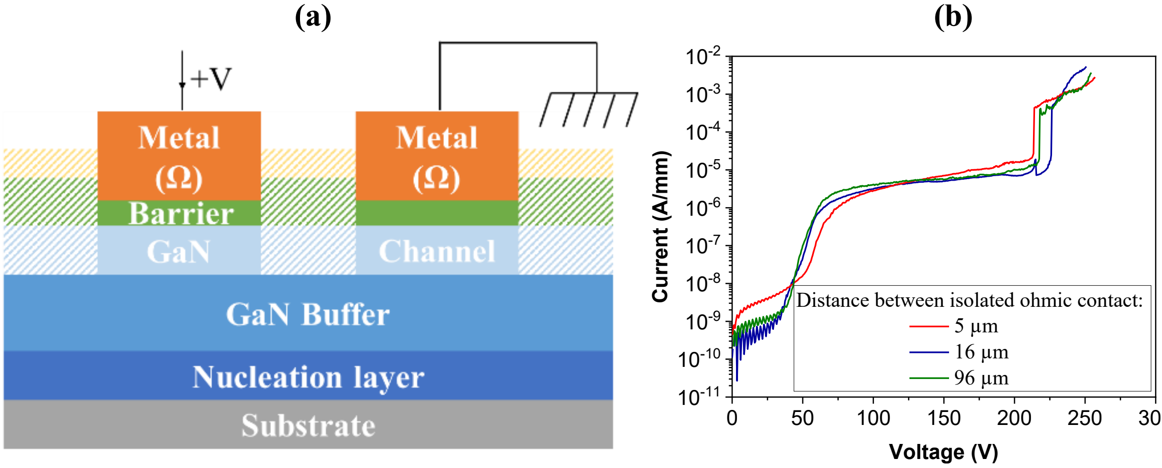


Figure 2.17.: (a) Schematic representation of lateral breakdown voltage measurements between two isolated ohmic contacts and (b) typical lateral breakdown voltages for various distances between isolated ohmic contacts in sub-micron thick GaN HEMTs.

III.1.b. Vertical breakdown voltage

The vertical breakdown voltage was measured with a grounded substrate and isolated ohmic contacts on the front side (**Figure 2.18**). The average vertical breakdown strength, representing the buffer's ability to block a specific vertical bias per unit buffer thickness, depends on the type and epitaxial growth parameters of the compensating buffer used to prevent lateral punch-through at high drain bias. Typically, the vertical breakdown voltage reflects the epitaxy quality, associated with defect density, for a given thickness. Additionally, normalizing the hard breakdown voltage with the total epi-stack thickness allows access to the vertical buffer breakdown field in MV/cm, enabling easy comparison between buffer with different thickness.

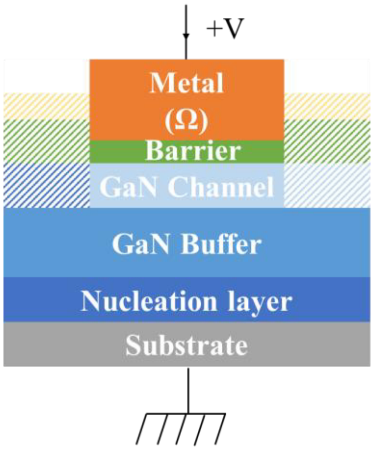


Figure 2.18.: Schematic representation of vertical breakdown voltage measurements on isolated ohmic contacts.

III.1.c. Three-terminal off-state transistor breakdown voltage

The three-terminal off-state transistor breakdown voltage is determined using source, drain, and gate contacts. As the name suggests, the gate is set at $V_{GS} < V_{th}$ to maintain an off-state condition. The breakdown voltage of GaN devices is often limited by various physical factors that need to be considered during the technology development. It is commonly measured as the voltage level where the drain current of pinched-off transistors exceeds a normalized value of 1 mA per millimeter of device width. Excessive gate or drain leakage currents, stemming from different epitaxial or technological factors, often restrict the maximum operational voltage. Within this thesis, when investigating sub-micron thick structures, it was noted that the three-terminal off-state transistor's breakdown voltage is not influenced by L_{GD}.

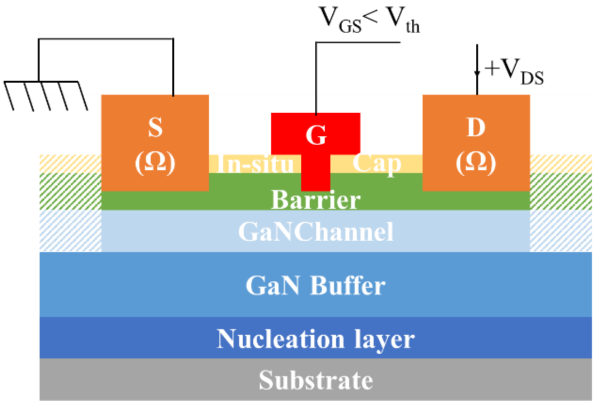


Figure 2.19.: Schematic representation of three-terminal off-state transistor breakdown voltage measurements.

III.2. DC characterization

One common electrical characterization applied to the final transistors, whether fabricated using optical or e-beam processing, involves DC measurements. This section details the DC characterization methods employed for the fabricated GaN HEMTs in this study. These measurements were carried out to evaluate the performance of transistors and detect any possible issues that might result in electrical abnormalities, including short channel effects, robustness, and trapping effects.

III.2.a. Static I-V characteristics

DC measurements are carried out with a Keysight A2902A static modular and source monitor, controlled by Keysight IC-CAP software. I-V electrical measurements of a transistor are the drain current expressed as a function of the gate or drain voltages as shown in **Figure 2.20**. The output characteristics I_D (V_{DS}) allow to extract the maximum on-state drain current

($I_{D,max}$) that the transistor can deliver while the transfer characteristics I_D (V_{GS}) allow to assess the following parameters:

- $I_{D,leak}$, the off-state drain leakage current of the transistor
- $I_{GS,leak}$, the gate leakage current of the transistor
- V_{th}, the HEMT threshold voltage
- $G_{m,max}$, the maximum extrinsic transconductance. That is obtained by the following derivation:

$$G_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)_{V_{DS}=Cste} \qquad \textbf{Equation 2.2}$$

- Drain Induced Barrier Lowering (DIBL), which is a short channel effect referring to a negative shift of the threshold voltage V_{th} at higher drain voltage.

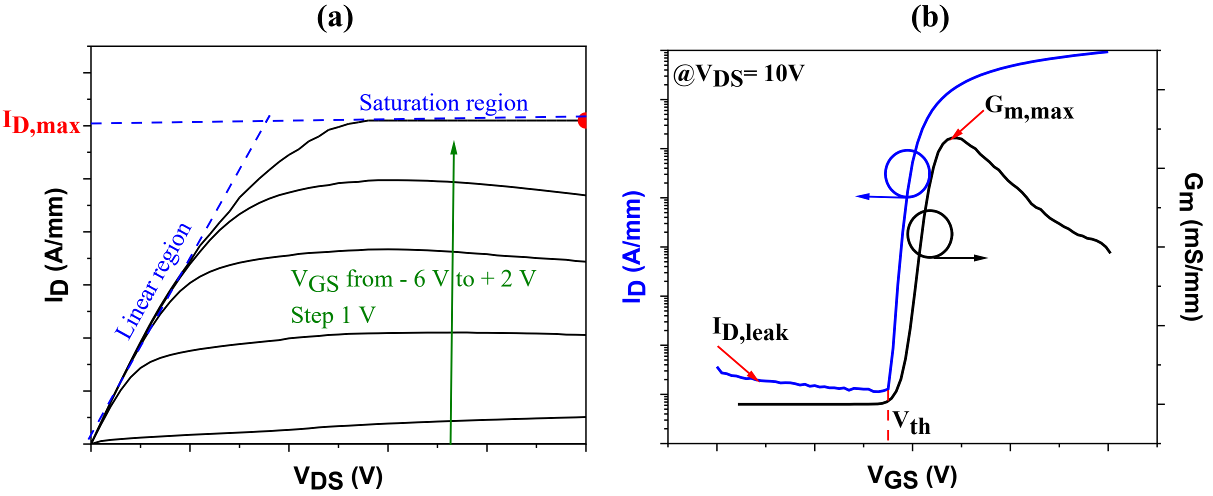


Figure 2.20.: Typical (a) output characteristics $I_D(V_{DS})$, (b) transfer characteristics $I_D(V_{GS})$ and extrinsic transconductance G_m of a GaN HEMT.

Figure 2.20.a displays the typical output characteristics $I_D(V_{DS})$ of the HEMT, identifying two operational regions: the linear region, where the drain current is proportional to the drain voltage, and the saturation region, where the drain current becomes independent on the drain voltage. The maximum drain current, $I_{D,max}$, is extracted from the output characteristics plot at $V_{GS} = +2$ V and $V_{DS} = 10$ V (in the saturation regime).

Figure 2.20.b illustrates typical transfer characteristics $I_D(V_{GS})$, which enable to determine the ON and OFF state drain current. The transistor's figure of merit is defined by a high I_{ON} / I_{OFF} ratio with low leakage current, essential for high-power performance. The threshold voltage is extracted graphically using the tangent extrapolation method, providing an

evaluation of the Schottky contact and gate length scaling. Furthermore, plotting G_m as a function of the gate voltage (V_{GS}) at a constant V_{DS} uncovers three operating areas:

- Off-state: $V_{GS} < V_{th}$, the channel becomes depleted, indicating the transistor is turned off.
- On-state: $V_{GS} > V_{th}$, the carrier density in the channel increases, leading to a rise in drain current relative to the gate voltage, up to an optimal operating V_{GS} where the transconductance reaches its maximum.
- Beyond the gate voltage corresponding to $G_{m,max}$, the transconductance drops as the channel opens due to thermal effects and an increase in parasitic elements with higher drain voltage.

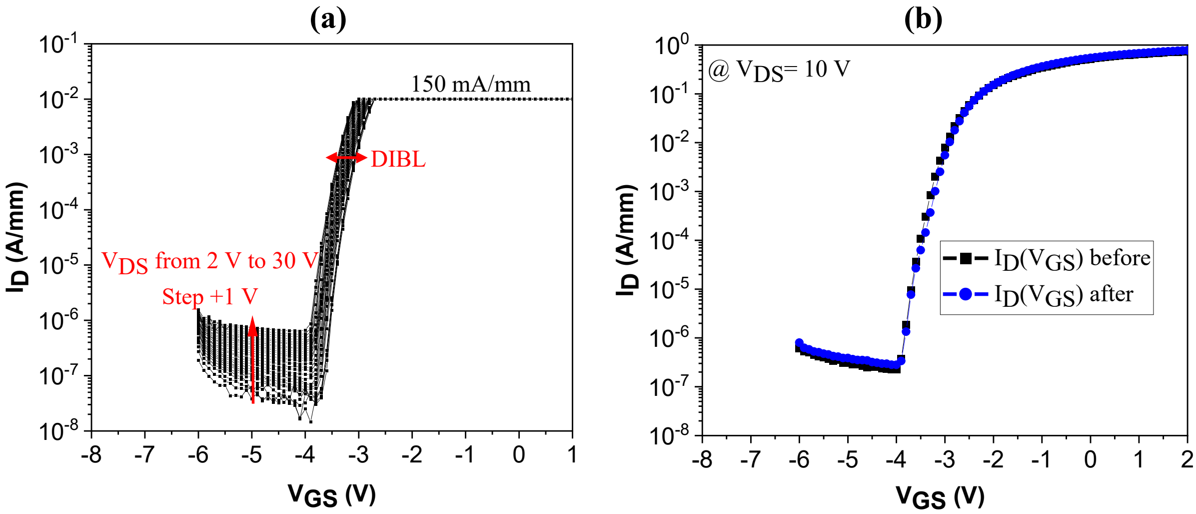


Figure 2.21.: (a) An example of semi-on robustness test with a compliance fixed at 150 mA/mm and swept from V_{DS} = 2V to 30V and (b) transfer characteristics $I_D(V_{GS})$ at V_{DS} = 10V performed before and after the semi-on robustness test .

The DIBL is extracted from a so-called "semi-on robustness test", which consists in limiting the drain current at 150 mA/mm during several transfer characteristics $I_D(V_{GS})$ sweeps from V_{DS} = 2 V up to V_{DS} = 30 V. Transfer characteristics $I_D(V_{GS})$ at V_{DS} = 10V are performed before and after the semi-on robustness test in order to evaluate the off-state current degradation (see **Figure 2.21**). This is a very efficient and quick test to highlight the material and processing quality as well as to define the safe operating area (to the first order). The DIBL value allows to evaluate the electron confinement within the structure. A higher DIBL can affect the device robustness. It can be expressed as follows:

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} \qquad \textbf{Equation 2.3}$$

III.2.b. Pulsed I-V characteristics

Trapping effects in semiconductor materials are responsible for short and long-term memory effects. These trapping effects can result from material defects, dislocations, lattice mismatch, impurities in the crystal lattice and existence of dangling bonds on the surface of transistors that act as trap centers for charge carriers flowing in conduction channel and causes current collapse. HEMT devices are deeply affected by trapping effects, which can prevent to benefit from their expected theoretical performances. Trapping phenomena is complex as it involves many potential sources within HEMT technology and thus cannot be solved rapidly. Pulsed I-V are the main measurements carried out during this work using different quiescent bias points in order to quantify the trapping effects, which may affect the transistor performances. From an electrical point of view when characterizing GaN HEMTs, the traps are separated into two types "Gate Lag" and "Drain Lag". They typically correspond to the electron trapping at the vicinity of the gate and within the overall structure (surface and buffer layers), respectively. The gate and the drain are pulsed from quiescent bias points (V_{GQ}, V_{DQ}) corresponding to a fixed trapping in the off-state duration time (t_{OFF}) and then the drain current is measured ($V_{D,meas}$) in the on-state duration time (t_{ON}) of the pulse as shown in **Figure 2.22**. The pulse width of the on-state duration time is chosen as small as possible (1µs) while the off-state duration time is much longer (99 µs) to prevent the self-heating effect and thus mostly investigating the trapping effect phenomena. The ratio between the pulse width and the period, known as duty cycle, must not be large in order to ensure fast and reliable data acquisition with averaging (duty cycle of 1% is used).

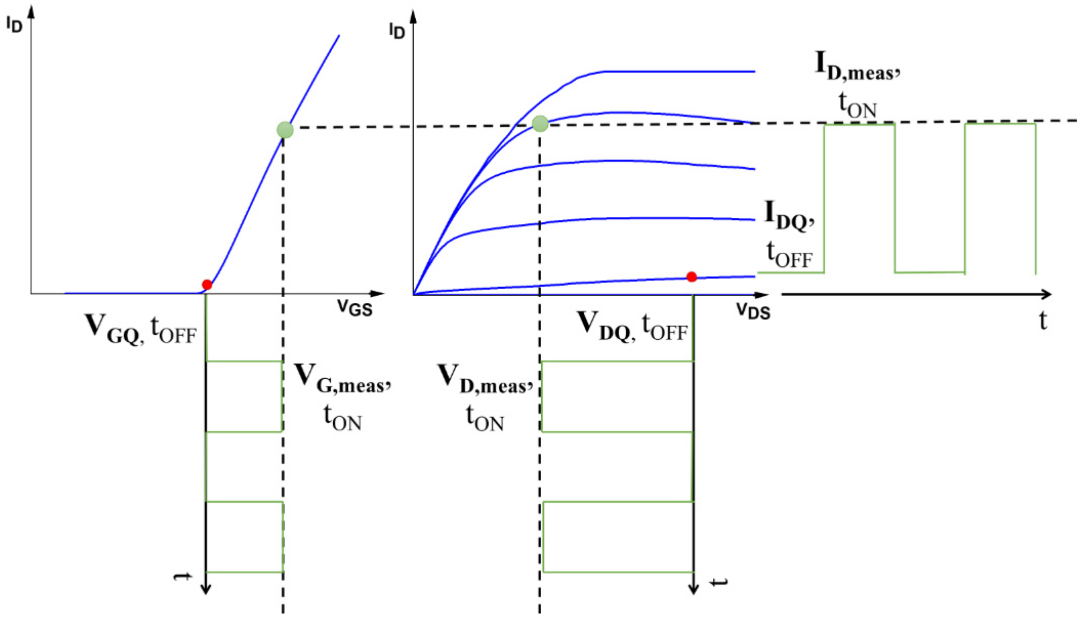


Figure 2.22.: Principle of I-V pulsed measurements

Figure 2.23 shows an example of pulsed I_D (V_{DS}) characteristics. A specific trapping pulsed I-V protocol based on I-V characteristics has been settled for different bias points in order to identify the trapping effects:

- Cold point: (V_{GQ}, V_{DQ}) = (0V, 0V) which corresponds to a measurement where the self-heating effect is excluded, and the electron trapping is negligible
- Gate-lag: (V_{GQ}, V_{DQ}) = (< V_{th}, 0V) which may favor the electron trapping under the gate region. V_{GQ} is chosen to be lower than the V_{th}
- Drain-lag: (V_{GQ}, V_{DQ}) = (< V_{th}, [10-20] V) which may favor the electron trapping under the gate-to-drain region along the space region

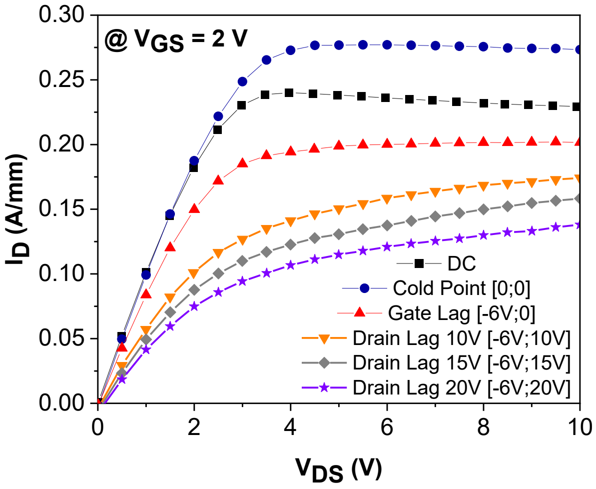


Figure 2.23.: An example of pulsed I-V characteristics showing strong trapping effects.

III.2.c. Drain current transient (DCT) measurements

A powerful method that can be added to directly evaluate the impact of charge trapping on drain current of HEMTs is Drain Current Transient (DCT) measurement. A DCT measurement bench has been recently developed in the framework of another PhD thesis from our research group. DCT measurements are executed in two phases (**Figure 2.24**):

- Trap-filling phase: the devices are kept for a flexible duration that can be short or long time (10 µs to 100 s) in off-state and various drain bias ($V_{GS,Fill}$; $V_{DS,Fill}$). During this phase, electrons are trapped under the gate and/or in the gate-drain access region (depending on the adopted bias point).

- Transient measurement phase: The devices are then switched to on-state ($V_{GS,ON}$;$V_{DS,ON}$), and the recovery of the drain current is measured during the whole duration of the de-trapping transient (typically from 1 µs to 100 s).

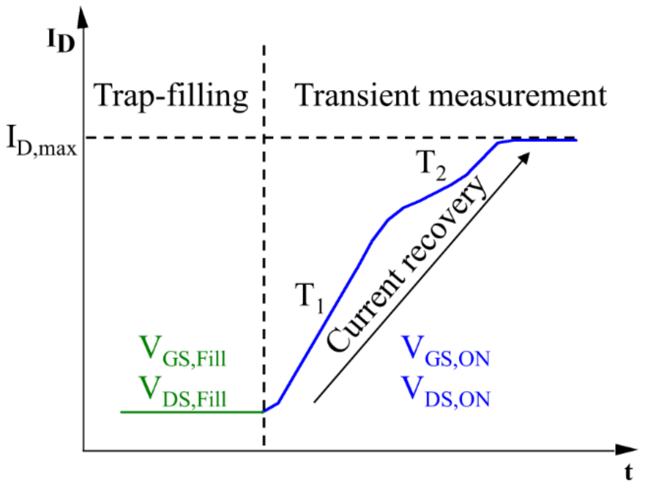


Figure 2.24.: Principle and example of DCT measurements.

Typical DCTs measured on GaN-HEMTs are plotted in **Figure 2.24**. The step-like behavior is due to the existence of two different electron emission processes, with different time constants (T_1 and T_2). A simple way to analyze the results of DCT measurements is to plot the derivative of the DCTs ($\delta I_D/\delta(\log(t))$, see **Figure 2.25.a**. Each positive peak represents an electron emission process; the time constant of the emission process is correlated to the position of the corresponding peak on the horizontal axis. By repeating the measurements at higher temperatures (**Figure 2.25.a**) it is possible to extrapolate the Arrhenius plot of the emission process and thus the activation energy (**Figure 2.25.b**).

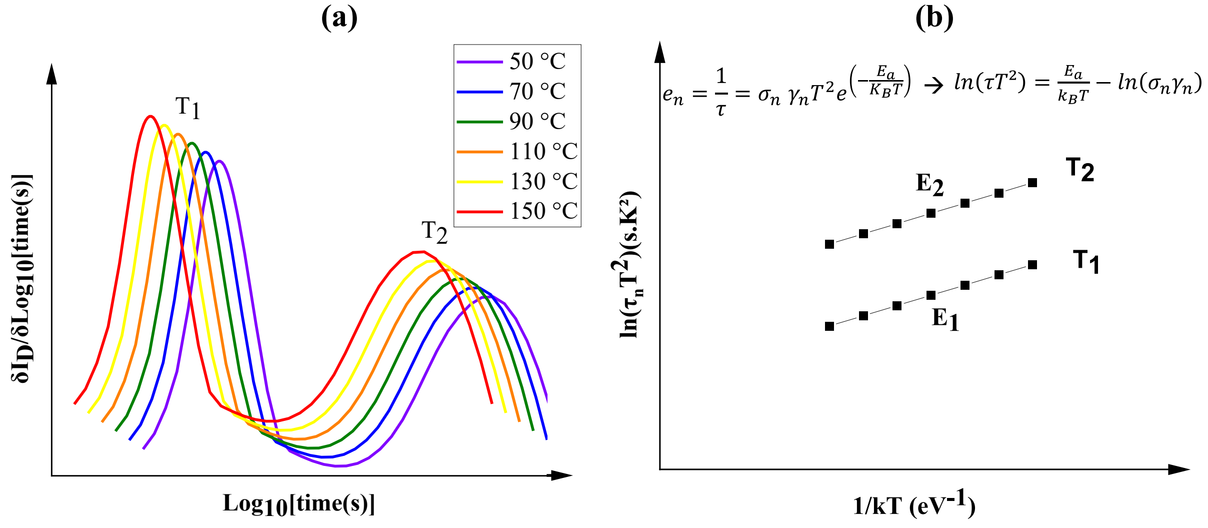


Figure 2.25.: (a) An exemple of time constant spectra (derivative of the drain current transients) measured versus temperature and (b) Arrhenius plot extrapolated from DCT measurements.

III.3. Small signal characterization

The small signal equivalent circuit of fabricated GaN HEMTs was derived using an Agilent PNA-67GHz (E8361A) network analyzer spanning 250 MHz to 67 GHz. This process aimed to evaluate the device's performance at higher frequencies. However, the precision of device measurements significantly relies on the calibration of the testing setup. Calibration is crucial to eliminate systematic errors across a range of measurements.

In small-signal operation, the transistor can be modelled as a quadrupole where an alternating voltage is applied (**Figure 2.26**). The load impedance, Z_c, is adjusted to determine the current gain $|H_{21}|$ and the unilateral gain U. Here, Z_s represents the source impedance.

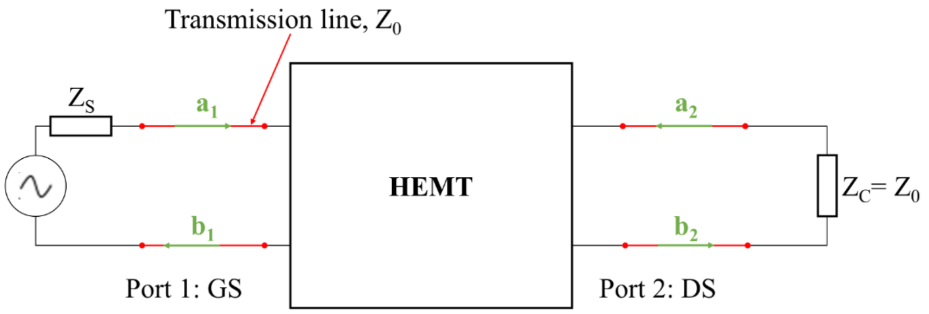


Figure 2.26.: Quadrupole representation of GaN HEMTs.

The incident and reflected power waves at the ports of the HEMT, denoted as a_i and b_i respectively, enable the determination of the scattering parameters S of the quadrupole through the following equations:

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad \textbf{Equation 2.4}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad \textbf{Equation 2.5}$$

Therefore, scattering parameters are complex wave ratios at a given frequency:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad \textbf{Equation 2.6}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0}$$

Hence, the current gain and unilateral gain are expressed as follows:

$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \quad \textbf{Equation 2.7}$$

$$U = \frac{1}{2}\frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{k\frac{S_{21}}{S_{12}}-Re\left(\frac{S_{21}}{S_{12}}\right)}$$ **Equation 2.8**

The illustration in F**igure 2.27** displays the small signal or linear model for HEMTs. This model comprises two distinct parameter types:

- The extrinsic parameters: it corresponds to the parasitic elements resulting from the access lines and metallization. It includes the pad capacitances C_{PG}, C_{PD} and C_{PGD}, the pad inductances L_G, L_D and L_S, and the gate and access resistances R_G, R_D, and R_S.
- The intrinsic parameters: it corresponds to gate-to-source, gate-to-drain, and drain-to-source capacitances (C_{GS}, C_{GD}, and C_{DS}), and drain-to-source resistance R_{DS}, which are bias dependent.

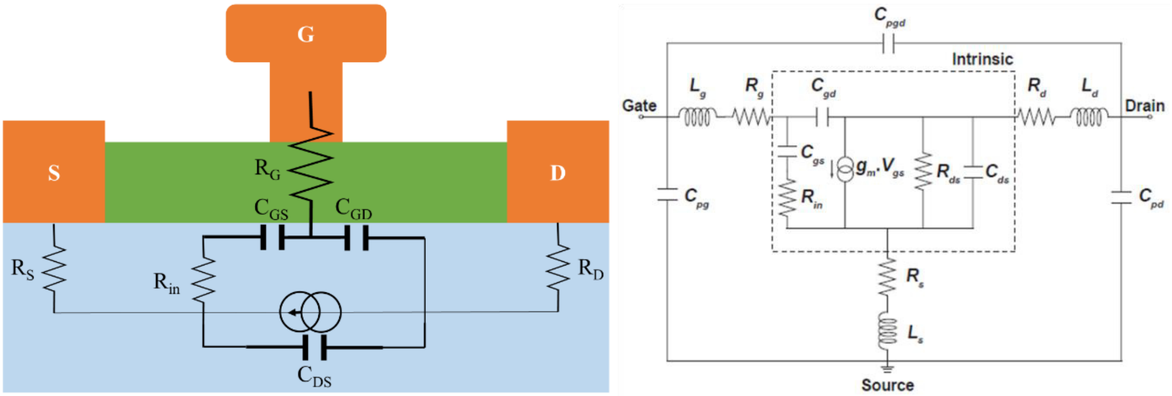


Figure 2.27.: Small signal equivalent circuit model of GaN HEMTs.

GaN HEMT high frequency performances are usually evaluated using two small signal figures of merit: the current gain cutoff frequency F_t and the maximum oscillation frequency F_{max}. The optimum gate polarization V_{GS} corresponds to the maximum transconductance $G_{m,max}$ while the drain voltage V_{DS} is increased from 10V up to 20V to evaluate the maximum oscillation frequency F_{max} of the transistor.

The transition frequency, also known as the current gain cutoff frequency F_t, marks the point where the current gain $|H_{21}|$ equals 0 dB. It is defined as a function involving the transconductance and the intrinsic characteristics within the equivalent circuit model:

$$F_t = \frac{G_m}{2\pi(C_{GS}+C_{GD})}$$ **Equation 2.9**

F_{max} serves as a crucial parameter in evaluating a transistor's capabilities for high-frequency operation. It denotes the frequency at which the unilateral power gain U reaches 0 dB. This parameter, f_{max}, is determined by a combination of the cutoff frequency, intrinsic, and extrinsic characteristics within the circuit model:

$$F_{max} = \frac{F_t}{2\left(R_g+R_{ds}\right)^{1/2}}$$

Equation 2.10

The cutoff frequency F_t and the maximum oscillation frequency F_{max} are extracted through extrapolation, employing the -20 dB/decade slope method. F_t represents the point where the -20 dB/decade tangent intersects the unity (0 dB) of the current gain H_{21}, while the maximum oscillation frequency is identified where the -20 dB/decade tangent intersects the unity of the power gain U, as illustrated in **Figure 2.28**.

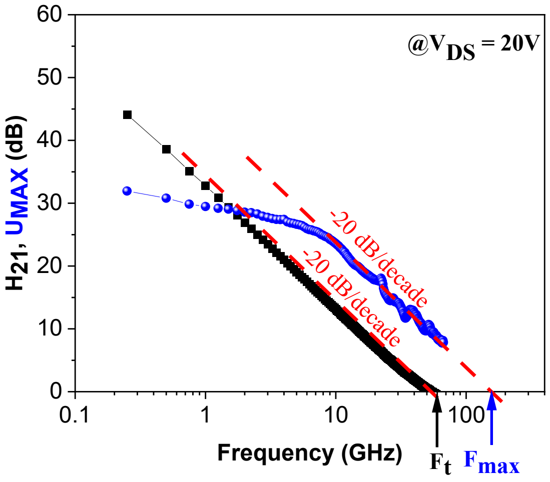


Figure 2.28.: An example of H_{21} and U curves used for the extraction of f_t and f_{max}.

III.4. Large signal characterization

GaN technology is acknowledged as an attractive solution for fulfilling the requirements of RF applications, where the combination of output power density and Power Added Efficiency (PAE) serves as a critical metric for evaluating device performance. In addition to addressing technological challenges, achieving an accurate non-linear characterization of transistors is an essential step to unlock the full potential of this emerging wide-band gap technology. However, conducting non-linear power device characterization is challenging due to factors such as losses, signal stability, and measurement time. To overcome these challenges, an active load-pull measurement bench was developed, enabling "Load-Pull" measurements up to 40 GHz in both continuous wave (CW) and pulsed mode. This development was part of a PhD thesis conducted by our research group in 2016 [152].

The NVNA setup uses a Nonlinear Vectorial Network Analyzer (Keysight N5245A-NVNA), allowing power measurements up to 40 GHz in both CW and pulsed mode. Within this framework, measurements at 10 and 40 GHz were conducted. **Figure 2.29** shows the power bench that has been optimized and the associated synoptic. The NVNA setup contains the following elements:

- Non-linear Vector Network Analyzer Keysight N5245A-NVNA
- 40 GHz Power Signal Generator (Agilent E8257D)
- Two 6-18 GHz amplifiers delivering 10W (CTT)
- Two 40-44 GHz amplifiers delivering 2W and 5W (Bonn Elektronik)
- A 40 GHz amplifier delivering up to 12W (TTi)
- A “Source Monitoring Unit” (SMU) delivering the DC power to the device under test (DUT) in CW mode (Agilent E5263A)
- Two pulse generators provide the DC power to the DUT in pulsed mode (HP-8110A & HP-8114A)
- Oscilloscope with voltage and current probes measures the voltage and current applied to the DUT in pulsed mode (Tektronix DPO7104)

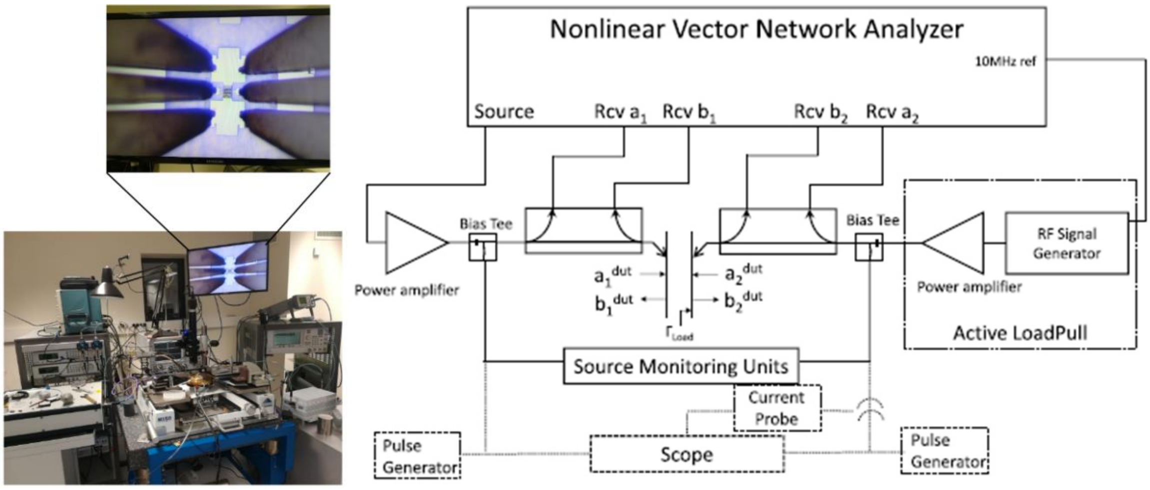


Figure 2.29.: Image of the load-pull bench up to 40 GHz and its optimized synoptic [152].

Load-pull measurements involve the incorporation of load impedances at the transistor output to determine the optimal load (≠ 50 Ω), thereby achieving the best power or PAE matching. This adjustment is crucial to prevent instability or oscillation issues that could lead to transistor degradation. The measurement process begins with biasing the transistor in the desired operating class. Power is then introduced at the transistor input to achieve saturation. Simultaneously, the load impedance is applied at the transistor output to achieve power or PAE matching. Throughout the load-pull measurements, the gate leakage current is monitored to ensure the transistor integrity.

Three approaches exist for load-pull measurements: passive, active, and hybrid load-pull. In this study, the focus was on the active load-pull method. Active load pull offers the advantage of reaching high values for the module, especially crucial when using smaller transistor sizes that typically result in high reflection coefficients.

Load-pull measurements are conducted through two excitation modes: Continuous Wave (CW) and pulsed mode. The CW mode is the conventional approach for nonlinear characterizations across various applications, involving a continuous polarization of the transistor throughout the measurement process. In contrast, the pulsed mode employs a pulsed polarization bias with a pulse width of 1 µs and a duty cycle of 1% in our case. This distinctive measurement technique at high frequencies enables the exploration of trapping effects under operational conditions, while simultaneously showcasing the devices complete potential by mitigating trapping and thermal effects.

Load-pull measurements are performed by varying the V_{DS} in both CW and pulsed modes, maintaining a constant drain current. During the load-pull sweeps, the gate current (I_G) is monitored as a function of the drain voltage V_{DS}, and a gate current degradation ($I_G > 100$ µA/mm) indicates device failure at the applied drain voltage.

Comparing results between CW and pulsed mode facilitates the assessment of trapping and thermal effects. However, it is essential to maintain consistent measurement conditions for both operational modes. A key performance metric for our transistors is achieving high efficiency. Therefore, a deep class AB has been selected to enhance PAE. The gate and drain bias as well as the optimal load at the transistor output are also chosen to maximize PAE. Notably, the optimal load may vary between CW and pulsed mode, as the S parameters of a transistor may differ due to the influence of trapping and thermal effects.

To avoid any oscillation or transistor degradation, it is imperative to identify the instability region on the Smith chart at 10 or 40 GHz for the transistors. This determination is carried out utilizing S-parameters and the Keysight-ADS tool (Advanced Design System) before starting load-pull measurements.

Figure 2.30 shows an example of large signal characteristics measured at 10 or 40 GHz. In order to evaluate the RF transistor performances at a particular frequency, there are three main figures of merit:

- The output power density P_{OUT}: which is the power density delivered by a transistor usually expressed in W/mm to compare the performance of a transistor regardless of its size. The transistor power density is evaluated through the saturated power P_{SAT} (the maximum power delivered by the transistor) and various compression points, which allows quantifying the linear behavior of the transistor.

- The power gain G_P: the transistor performances are characterized by the gain, which defines the capability to amplify an RF signal. A high gain contributes to high power density and PAE. It is given by the following form:

$$G_P\,(\text{dB}) = P_{RF,OUT} - P_{RF,IN} \qquad \textbf{Equation 2.11}$$

- The power added efficiency (PAE): PAE represents the ratio between the power gain and the dissipated power P_{DC}. A high PAE reduces the self-heating of the component and limits the energy consumption required by specific applications. It is given by:

$$PAE = \frac{P_{RF,OUT} - P_{RF,IN}}{P_{DC}} = \frac{P_{RF,OUT}}{P_{DC}} \times \left(1 - \frac{1}{G_P}\right) \qquad \textbf{Equation 2.12}$$

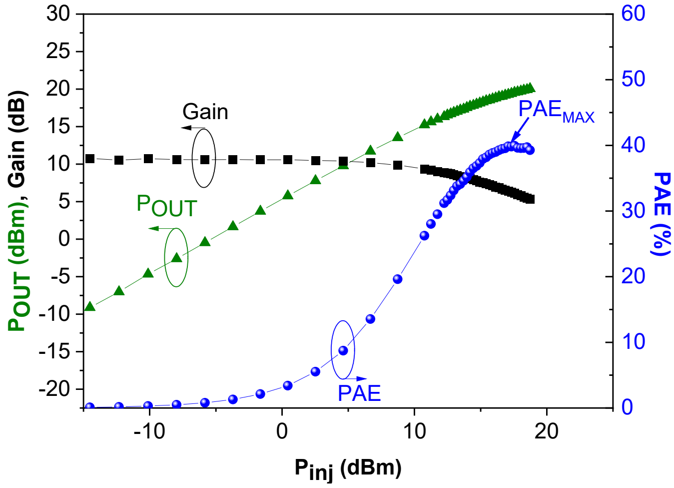


Figure 2.30.: An example of large signal characteristics showing the PAE, the P_{OUT} and the power gain at 10 or 40 GHz.

IV. Conclusion

Demonstrating the high-performance capabilities of GaN technology operating at high frequency requires the optimization not only of the epitaxial structures but also of the device processing and characterizations. This chapter outlines the fabrication process of GaN HEMTs designed for high-frequency operation, along with the device characterization tools.

The discussion begins with an overview of the mask sets and the development of the device processing. To enhance device performance, particular emphasis is placed on optimizing the fabrication process, especially with respect to ohmic and gate contacts. Achieving a reliable ohmic contact process with low contact resistances (R_c) is crucial for high-frequency performance of scaled devices. Simultaneously, gate fabrication for high-frequency operation undergoes critical development. A process enabling sub-100 nm gate lengths is introduced while maintaining low leakage current, low gate resistance, and parasitic capacitances.

Following this, the chapter delves into the bench and methods employed for breakdown voltage, small and large signal characterizations. The characterization campaigns at IEMN, incorporating different breakdown voltage, DC, pulsed, DCT, small and large signal characterizations are detailed. Finally, transistor characterization through load-pull benches at 10 and 40 GHz is described.

In the upcoming chapters, the electrical and structural characterization results of the various devices fabricated within this PhD will be elaborated.

Chapter 3: Optimization of Sub-micron thick Buffer on Silicon for High Buffer Breakdown Field

I. Introduction

The landscape of GaN for millimeter-wave power devices is currently undergoing a crucial debate regarding substrate choices. Recently published data proved SiC as the leading contender, given its outstanding physical properties, such as minimal lattice mismatch with GaN, low RF losses and high thermal conductivity, which unlock unprecedented power performance [21–23]. However, challenges arise due to the high cost and limited availability of larger wafer sizes for SiC substrates. On the other hand, Si substrates offer an appealing alternative, with large-size availability and cost-effectiveness up to 12 inches. Despite a significant lattice mismatch and thermal expansion coefficient difference with GaN, the potential for cost-effective and integrated solutions, especially in mass production applications, positions GaN-on-Si as a compelling prospect.

In the context of substrate development, the AlN nucleation layer (NL) and GaN-based buffer layers play a pivotal role, serving as a transition between the Si substrate and the GaN channel layer. The primary goal of the GaN buffer is to reduce dislocations reaching the channel layer and provide a smooth surface for the barrier layer. Additionally, the buffer layer is crucial for confining electrons to the 2DEG under a high electric field, limiting short channel effects. Recent literature emphasizes that devices lacking effective electron confinement exhibit reduced robustness and are unable to achieve high operating frequencies. Traditionally, these buffer layers are grown with substantial thickness (several µm) to minimize dislocations reaching the channel layer and ensure a smooth surface for the barrier layer. However, this approach comes with trade-offs, including degradation in thermal dissipation and an increase in the cost of epi-wafers. Moreover, commonly found in the literature are Carbon-doped GaN buffers. While a heavily doped buffer enhances isolation and power performance, it also leads to increased defect density and significant scattering effects when dopants are introduced near the channel region, resulting in current collapse [35, 36].

To address these challenges, this study focuses on the fabrication of a submicron buffer without intentional doping. Numerous investigations aim to optimize the buffer and nucleation layer, seeking superior electron confinement, minimized trapping effects under high electric field (i.e., high operating voltage) while maintaining a submicron total epi-thickness. This chapter presents the electrical and structural characterizations of the fabricated transistors within the framework of optimizing the nucleation and buffer layers. Measurement campaigns were conducted using various characterization tools, as described in **Chapter 2**, on fabricated transistors at IEMN.

II. Study of different submicron thick buffer configurations

In the first step, a buffer study was conducted, involving the epitaxial growth of a significant quantity of material using various types of buffers to identify the most effective one (such as overcoming the trade-off between the electron confinement under high electric field and trapping effects), as outlined in **Table 3.1**. The choice was made to exclusively utilize a combination of Al-rich AlGaN and/or AlN layers within the buffer due to the already poor thermal dissipation of the Si substrate. Consequently, intentional doping was omitted from the structure with the aim of minimizing trapping effects. For each buffer type, multiple wafers were produced with slight variations in parameters such as thickness and Al content. To achieve this, five buffer configurations with a total thickness below 1 µm were employed (see **Table 3.1**):

- AlGaN back barrier: a single layer of $Al_xGa_{1-x}N$ was employed below the GaN channel layer,
- Step-graded AlGaN: a sequence of three $Al_xGa_{1-x}N$ layers with decreasing Al content until the GaN channel was used,
- Superlattices: a sequence of multiple AlN/GaN layers were grown,
- Interlayer: an AlN layer was deposited between two distinct $Al_xGa_{1-x}N$ layers or between a GaN and $Al_xGa_{1-x}N$ layers.

Buffer	Number of wafers studied
Buffer-free	2
AlGaN back barrier	2
Step-graded AlGaN	6
Superlattices	5
Interlayer	3

Table 3.1.: Types and number of wafers studied for various submicron thick buffer configurations on Si.

Additionally, a structure without buffer layers, referred to as "Buffer-free," was developed where the GaN channel was directly deposited on top of a high-quality AlN NL. This structure was grown to enable a comparison of vertical and lateral breakdown with and without submicron buffer layers.

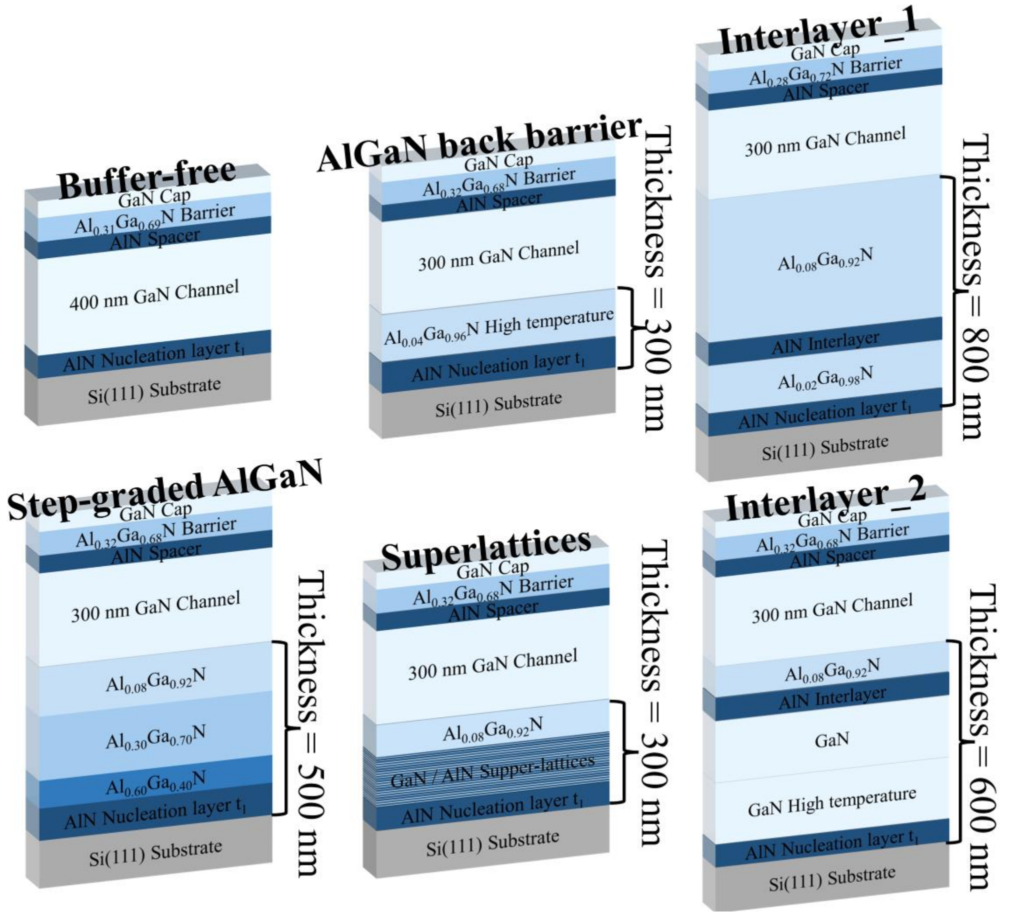


Figure 3.1.: Schematic cross section of various submicron thick buffer configurations used in the buffer optimization study.

In the following section, a comparison of six buffer configuration studies is presented. The growth of the structures was performed by NH_3-MBE on highly resistive Si (111) substrates (ρ > 5 kΩ.cm) of 3", 6", and 8". As illustrated in **Figure 3.1**, the structures consist of an AlN nucleation layer, with a thickness of less than 100 nm (t_1), followed by the buffer layers (thickness less than 1 µm), a 300 nm GaN channel, a 1 nm AlN spacer, and a 14 nm $Al_{0.28}Ga_{0.72}N$ barrier. Finally, the structure was capped with a 1 nm GaN layer. The distinctive feature of these structures is that they all have a buffer thickness of less than 1 µm. The six buffer studies are the following (more detailed in **Figure 3.1**): it starts with buffer free where the GaN was directly grown on the AlN nucleation layer; then an AlGaN back barrier to improve the 2DEG confinement refers as "AlGaN back-barrier" structure was added; The "Superlattices" structure consists of introducing an AlN/GaN SL in between the AlN nucleation layer and the AlGaN back-barrier, to increase the buffer resistivity; the “3 Step-graded AlGaN”, “Interlayer_1” and “Interlayer_2”. The “Interlayer_1” structure corresponds to the classic interlayer buffer while in “Interlayer_2” high temperature GaN in the buffer was introduced to further reduce the dislocation density.

The electrical properties, extracted through Hall Effect measurements at room temperature, are depicted in **Figure 3.2** for each buffer configuration. The structures “Buffer-free” and “Step-graded AlGaN” exhibit the best trade-off between high mobility and a substantial 2DEG concentration. Specifically, the “Buffer-free” structure achieves a mobility of 1470 cm^2/V.s and a N$_S$ of 1.1 × 10^{13} cm^{-2}, while the “Step-graded AlGaN” structure delivers a mobility of 1130 cm^2/V.s with a N$_S$ of 1.0 × 10^{13} cm^{-2}. In contrast, the N$_S$ of the four other structures is approximately 7-8 × 10^{12} cm^{-2}, albeit with good mobility: around 1100 cm^2/V.s for the “AlGaN back barrier” and “Super-lattices” structures, and 1700 cm^2/V.s for the “Interlayer_1” and “Interlayer_2” structures. The increased mobility observed in "Interlayer_1" and "Interlayer_2" is likely a result of the larger thickness of the buffer and the utilization of the AlN interlayer, which allows to decrease the dislocation density in the GaN channel.

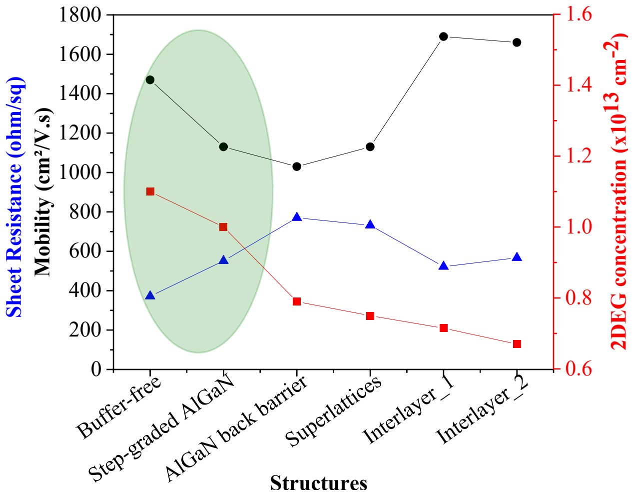


Figure 3.2.: 2DEG electrical properties for different submicron thick buffer configurations.

II.1. Device fabrication

This study has been carried out using the optical mask-set “BreakUp” in order to simplify the fabrication process and evaluate the epitaxial structures through breakdown voltage and DC characterizations. For each heterostructure a similar process was used. The source-drain ohmic contacts were formed by partially etching the AlGaN barrier layer with BCl$_3$/SF$_6$ plasma in an ICP reactor prior to the metallization. A Ti/Al/Ni/Au metal stack annealed at 750°C has been used to obtain a contact resistance < 1 Ω.mm. Then, Ti/Au gates of 3 µm length were defined by optical lithography. Finally, 150 nm PECVD SiN layer was deposited as final passivation prior to the Ti/Au pads deposition enabling electrical measurements.

II.2. Breakdown characterization of different submicron thick buffer

In **Figure 3.3**, the lateral breakdown characterizations of each structure is depicted for various distance between two isolated ohmic contacts, ranging from 5 µm to 96 µm with a floating substrate. However, due to the submicron thickness of the structures, the saturation regime is already observed for a distance between the contacts as low as 5 µm (**Figure 3.3.a**). The measurements were performed by immersing the samples in a Fluorinert solution to mitigate the risk of electrical arcing in air.

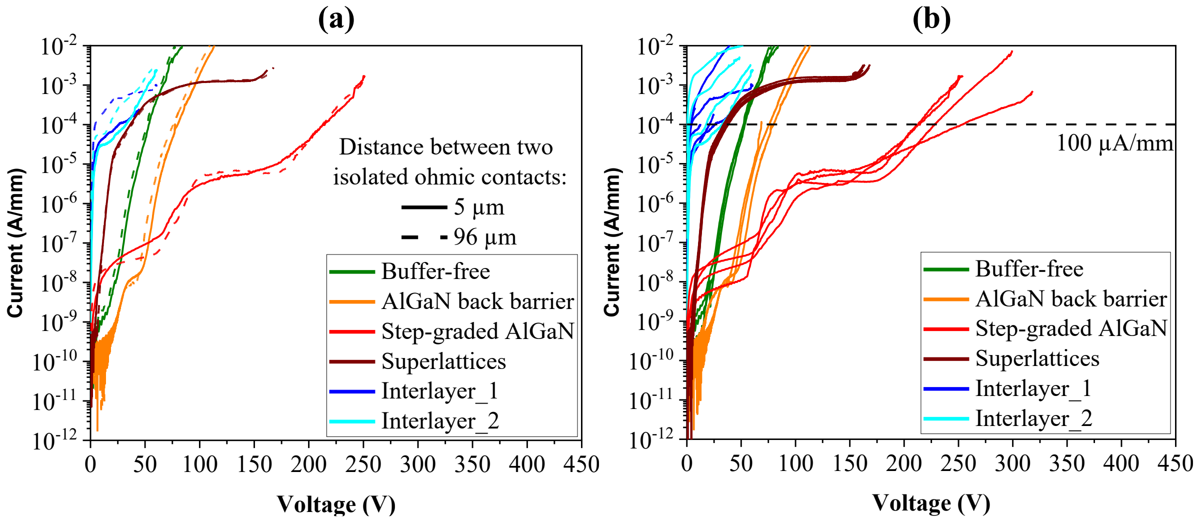


Figure 3.3.: Lateral breakdown characteristics of different submicron thick buffer configurations for (a) distances between two isolated ohmic contacts of 5 µm and 96 µm and (b) different locations across the samples.

The "Buffer-free" structure maintains a plateau up to 25 V before experiencing a drastic increase in leakage current, resulting in premature hard breakdown voltage at 80 V. In contrast, the "Interlayer_1" and "Interlayer_2" structures exhibit a high leakage current at low voltages, leading to a premature hard breakdown voltage around 50 V, which reveals the presence of a parasitic conduction inside the buffer. Similarly, the "Superlattices" structure lacks a plateau, with a leakage current increasing directly to 100 µA/mm at 40 V, despite a hard breakdown voltage at 170 V.

For the last two structures, "AlGaN back barrier" and "Step-graded AlGaN," the emergence of larger plateaus is observed. Indeed, both structures seem to share a common plateau up to 50 V. However, the "Step-graded AlGaN" structure exhibits a second plateau, maintaining a current below 100 µA/mm up to 200 V. Consequently, the "AlGaN back barrier" structure shows a hard breakdown voltage at 110 V, while the "Step-graded AlGaN" structure achieves an excellent breakdown voltage exceeding 250 V. This demonstrates that only one layer of $Al_xGa_{1-x}N$ with low Al content into the buffer is not sufficient to significantly increase the overall bandgap inside the structure.

Vertical breakdown voltage measurements were performed with a grounded substrate and isolated ohmic contacts on the front side for each structure (**Figure 3.4**). When examining the range between 0 V and 50 V, it becomes evident that the "Step-graded AlGaN" structure exhibits a dual plateau behavior (**Figure 3.4.b**). The first plateau maintains a current below 1×10^{-4} mA/cm² up to 80 V, while the second plateau sustains a current below 1 mA/cm² up to 500 V, facilitating a hard breakdown voltage around 550 V. In contrast, all other structures display leakage currents that increase at low operating voltages, resulting in leakage currents of 1 mA/cm² for voltages below 100 V, even though most of them exhibit a hard breakdown voltage higher than 500 V. The higher breakdown voltage at low leakage current observed in the "Step-graded AlGaN" structure is attributed to a higher effective bandgap compared to the other buffers. It can be pointed out that despite the submicron thickness of the epi-stack in each structure, the distribution of leakage current in vertical and lateral measurement is relatively uniform, indicating that a thick buffer is not mandatory to maintain high material quality close to the 2DEG (**Figure 3.3.b and Figure 3.4.b**) [153].

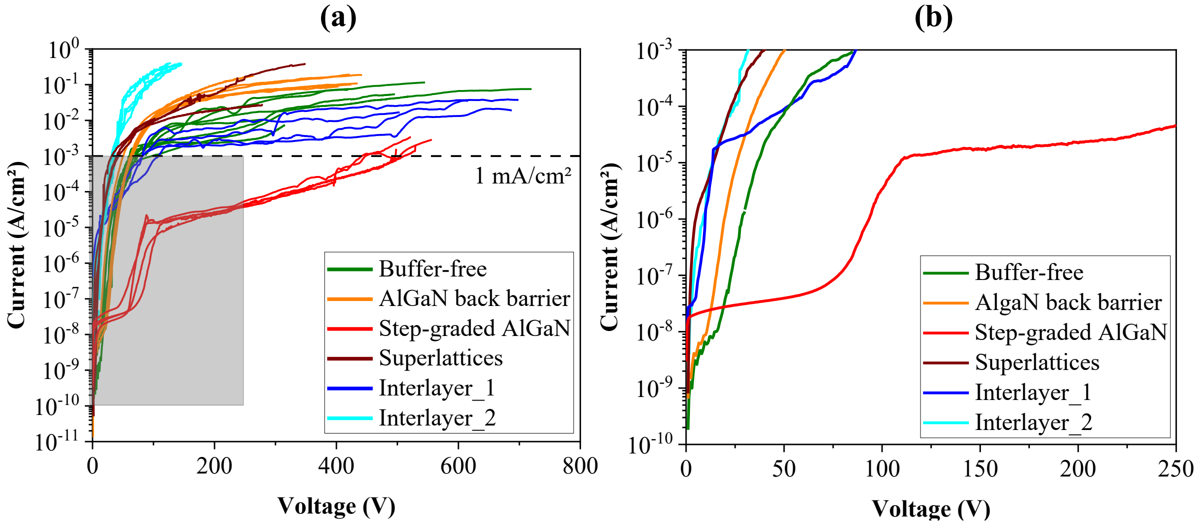


Figure 3.4.: Vertical breakdown characteristics of different submicron thick buffer configurations for different locations across the samples.

Three-terminal off-state breakdown voltage characterization were conducted on 2 × 50 µm transistors with L_G = 3 µm and L_{GD} = 5 µm at V_{GS} = -4 V for each buffer. As evident from both vertical and lateral breakdown characterizations, the "Step-graded AlGaN" structure demonstrates a superior three-terminal off-state breakdown voltage while maintaining a low drain current, well below 1 mA/mm up to V_{DS} = 250 V. In contrast, among the other structures, "Interlayer_2" exhibits high drain leakage current at low voltage operation. The "Superlattices" heterostructure reaches 1 mA/mm drain current at 50 V, and both "Interlayer_1" and "AlGaN back barrier" reach 1 mA/mm drain current at 100 V. The relatively high I_D observed in the "Interlayer_2" structure is likely attributed to the presence of a parasitic conduction between the GaN layer in the buffer and the AlN interlayer.

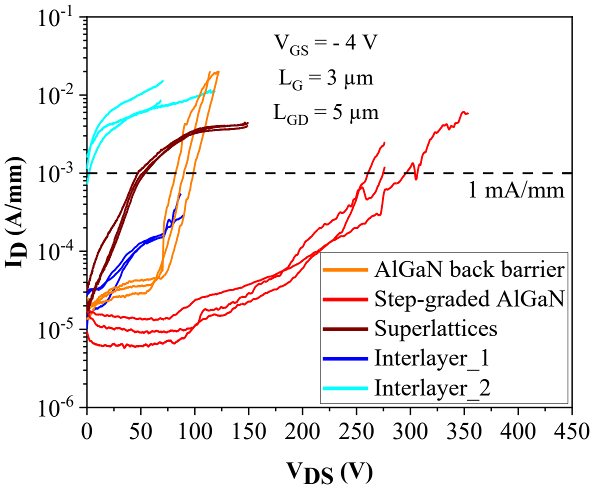


Figure 3.5.: Three-terminal off-state breakdown voltage of 2×50 µm transistor with L_G = 3 µm and L_{GD} of 5 µm at V_{GS} = -4 V of each submicron thick heterostructure.

II.3. RF losses

RF losses were extracted from S_{21} parameters through transmission lines up to 67 GHz as a key figure of merit in the investigation of various submicron buffers configurations (**Figure 3.6**). Significant RF losses of -1.6 dB/mm and -5.6 dB/mm are observed at 40 GHz for the "Interlayer_1" and "Interlayer_2" structures, respectively. This outcome distinctly indicates the presence of a parasitic conduction within the interlayer buffer type, particularly pronounced when undoped GaN is utilized within the buffer ("Interlayer_2"). **Figure 3.6.b** illustrates that for the three remaining structures, RF losses are maintained below -0.9 dB/mm up to 67 GHz. Notably, the "Step-graded AlGaN" buffer exhibits RF losses below -0.6 dB/mm up to 67 GHz. Nevertheless, these results remain relatively high when compared to structures grown on SiC or recent state-of-the-art results on Si and can be further improved [154]. Indeed, previous studies conducted by EasyGaN had already demonstrated the possibility of achieving RF losses as low as -0.3 dB/mm at 40 GHz for submicron GaN-on-Si heterostructures, as illustrated in **Figure 3.6.b**. The difference with the structures used in the buffer study results from the higher RF losses observed in the Si substrate lot delivering -0.5 dB/mm.

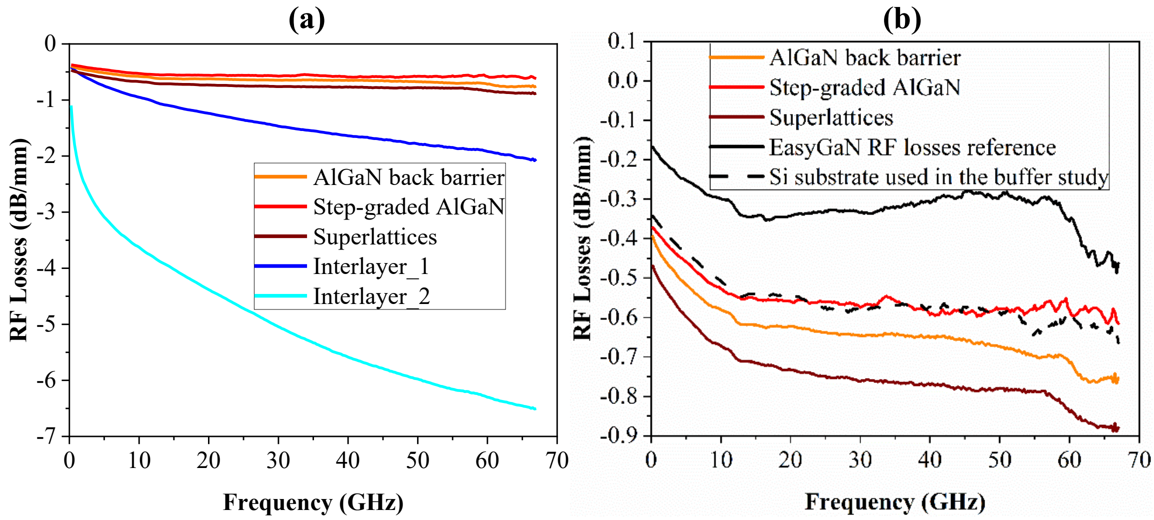


Figure 3.6.: RF Losses extracted from S_{21} parameters through transmission lines up to 67 GHz for the different submicron thick buffer configurations.

II.4. DC and DC pulsed characterization

Output characteristics of 2 × 50 µm transistors with L_G = 3 µm and L_{GD} = 5 µm on the structures with different submicron thick buffer are shown in **Figure 3.7**. The gate source voltage was swept from −6 to +2 V with a step size of 1 V. A maximum drain current $I_{D,max}$ varying between 0.4 and 0.5 A/mm for each structure has been measured mainly limited by the 2DEG electron mobility or N_S of these structures (see **Figure 3.2**).

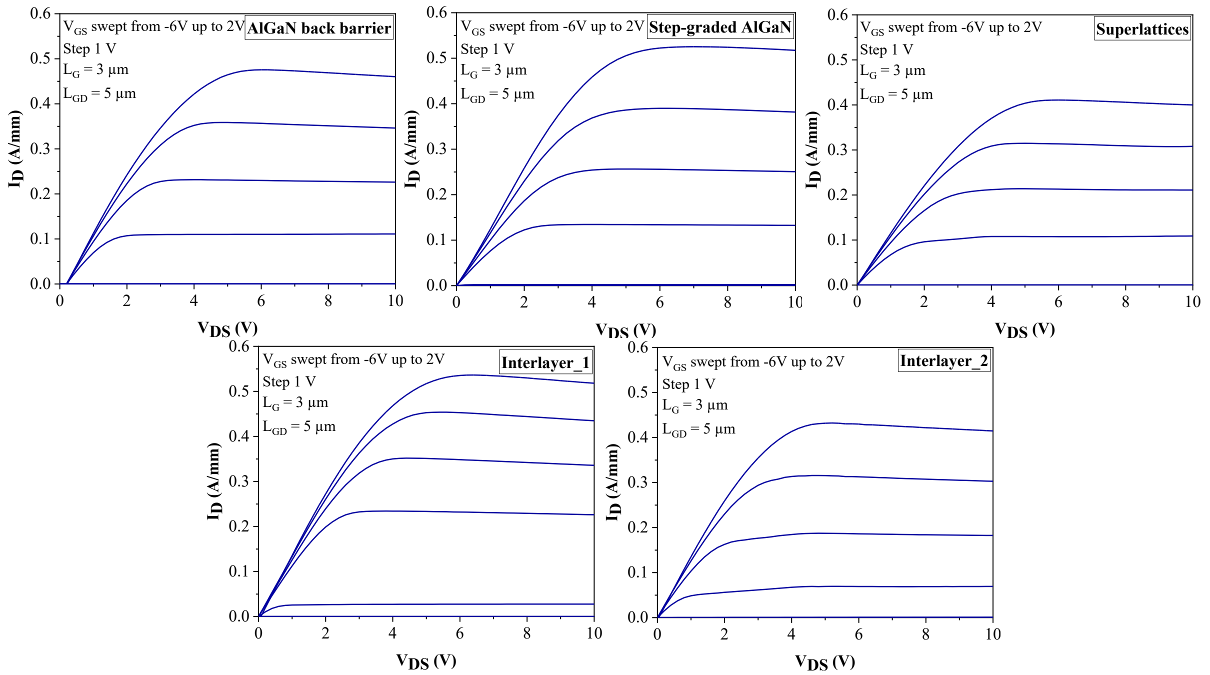


Figure 3.7.: Output characteristics of 2×50 µm transistors with L_G = 3 µm and L_{GD} = 5 µm of the structures with different submicron buffer configurations.

In **Figure 3.8**, transfer characteristics with a compliance fixed at 150 mA/mm and swept from V_{DS} = 2 to 20 V using a step of 1 V of 2 × 50 µm transistors with L_G = 3 µm and L_{GD} = 5 µm on the structures with different submicron thick buffer are shown. Although the DIBL for each structure is as anticipated satisfactory with the use of a 3 µm large gate length, the same cannot be said for the drain leakage current. Indeed, for the "Interlayer_2" structure, the off-state drain leakage current surpasses 100 µA/mm at low V_{DS}. In contrast, for "Interlayer_1" and "Superlattices" $I_{D,leak}$ remains below 100 µA/mm up to V_{DS} = 20 V. Similarly, for "AlGaN back barrier" and "Step-graded AlGaN," $I_{D,leak}$ is maintained below 10 µA/mm up to V_{DS} = 20 V.

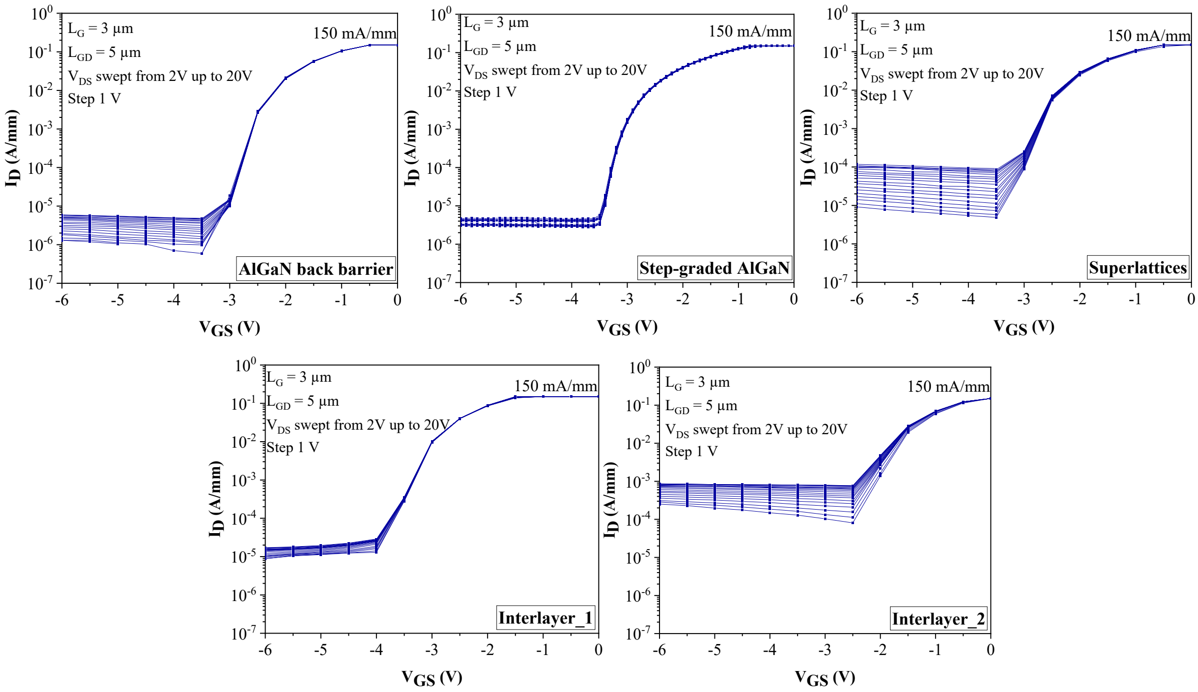


Figure 3.8.: Transfer characteristics of 2×50 µm transistors with a compliance fixed at 150 mA/mm and swept from V_{DS} = 2 to 20 V using a step of 1 V with L_G = 3 µm and L_{GD} = 5 µm of the structures with different submicron thick buffer configurations.

DC pulsed measurements were conducted on the various structures used in the submicron thick buffer optimization study at room temperature, with V_{GS} set at +2 V and different quiescent drain voltages. "Interlayer_1" demonstrates low gate lag and drain lag effects (less than 9% current collapse under drain lag conditions at 20 V), likely attributed to its larger thickness and the presence of the AlN interlayer, which enhances the filtration of dislocations. In contrast, the other structures exhibit low gate lag but notable drain lag. The "Superlattices" structure shows a current collapse of 20% under drain lag conditions at 20 V, while the remaining structures exhibit a current collapse around 30%. The observed current collapse may originate from either the buffer or the surface. Importantly, previous studies have indicated that the use of a GaN cap can introduce trapping effects onto the surface, a topic that will be further explored in **Section IV**.

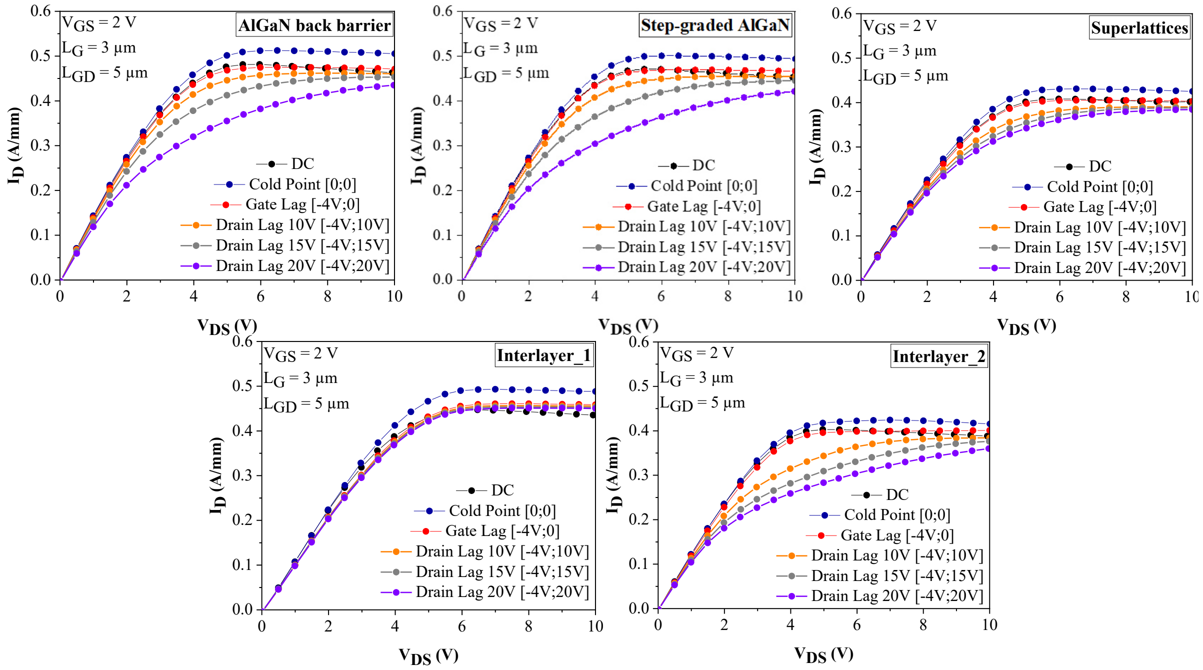


Figure 3.9.: Open channel pulsed I_D-V_{DS} output characteristics of 2×50 µm transistors with L_G = 3 µm and L_{GD} = 5 µm of the structures with different submicron thick buffer configurations.

	AlGaN	**Step-graded AlGaN**	**Superlattices**	**Interlayer_1**	**Interlayer_2**
Mobility	1030 cm^2/V.s	1130 cm^2/V.s	1130 cm^2/V.s	1700 cm^2/V.s	1700 cm^2/V.s
N_S	7.9×10^{12} cm^{-2}	1.1×10^{13} cm^{-2}	7.5×10^{12} cm^{-2}	7.1×10^{12} cm^{-2}	6.7×10^{12} cm^{-2}
Lateral breakdown @100µA/mm	75 V	200-250 V	35 V	10-30 V	10-30 V
Vertical breakdown @1 mA/cm²	60 V	450-500 V	45 V	90-100 V	30 V
Three terminal off-state breakdown @1 mA/mm	80-100 V	250-300 V	50 V	90 V	< 5 V
RF losses @40 GHz	-0.7 dB/mm	-0.6 dB/mm	-0.8 dB/mm	-5.6 dB/mm	-1.6 dB/mm
$I_{D,MaX}$	0.45 A/mm	0.5 A/mm	0.4 A/mm	0.5 A/mm	0.4 A/mm
$I_{D,leak}$	$1\times10^{-5} > I_{D,leak} > 1\times10^{-6}$ A/mm	$1\times10^{-5} > I_{D,leak} > 1\times10^{-6}$ A/mm	$1\times10^{-4} > I_{D,leak} > 1\times10^{-5}$ A/mm	$1\times10^{-4} > I_{D,leak} > 1\times10^{-5}$ A/mm	$1\times10^{-3} > I_{D,leak} > 1\times10^{-4}$ A/mm
Current collapse @drain lag 20 V	29 %	33 %	18 %	9 %	35 %

Table 3.2.: Summary of figure of merits for the various submicron thick buffer investigation.

Table 3.2 presents a summary of the main properties achieved for each submicron thick buffer study. The optimum buffer in this study corresponds to the one with three layers of AlGaN with a variation in the Al composition, known as "Step-graded AlGaN." This buffer showcases an impressive combination of vertical, lateral, and transistor breakdown voltage, while maintaining essential transistor properties such as off-state drain leakage current and low RF losses. The only drawback is the significant current collapse during pulsed DC measurements for this structure. However, it is important to note that the origin of trapping effects is not necessarily within the buffer. A thorough investigation of the traps in the structure will be presented in an upcoming section.

III. Impact of the nucleation layer thickness

Figure 3.10 shows the cross section of the HEMT structures used to study the impact of the nucleation layer thickness. Two different AlN NL with thickness 1 (t_1 < 100 nm) << thickness 2 (t_2 > 100 nm) have been grown by NH_3-MBE on highly resistive Si (111) substrates (ρ > 5 kΩ.cm) using a RIBER MBE49 growth reactor. The structure is then followed by three step-graded $Al_xGa_{1-x}N$ buffer layers ($Al_{0.60}Ga_{0.40}N$ /$Al_{0.30}Ga_{0.70}N$/ $Al_{0.08}Ga_{0.92}N$), a 150 nm thick GaN channel layer, a 1 nm thick AlN spacer and a 14 nm thick $Al_{0.32}Ga_{0.68}N$ barrier. Finally, the structure was capped with a GaN layer. The total stack thickness is less than 700 nm for the structure with AlN NL t_1 and the second structure has also a total thickness below 1 µm.

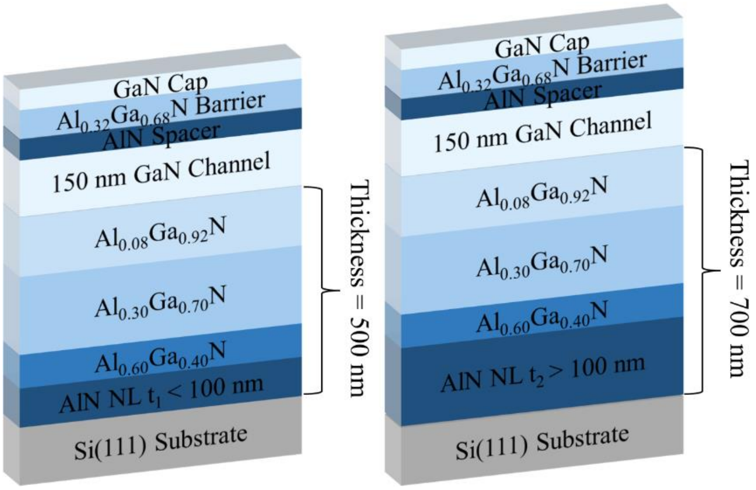


Figure 3.10.: Schematic cross section of two submicron thick AlGaN/GaN HEMT heterostructures grown on Si (111) with three step-graded $Al_xGa_{1-x}N$ buffer layers used in the nucleation layer thickness optimization study.

The 2DEG properties have been extracted at room temperature by Hall effect measurements and showed a charge density of 1.1×10^{13} cm^{-2} and 1.3×10^{13} cm^{-2} with an electron mobility of 1050 $cm^2/V.s$ and 1530 $cm^2/V.s$ for AlN NL t_1 and t_2, respectively (**Figure 3.11**). The AlN NL thickness indirectly impacts the electron mobility. Indeed, when increasing the thickness of the AlN, the crystalline quality is improved (with less dislocations and larger grains). In addition, the step-graded $Al_xGa_{1-x}N$ buffer layers on top and the GaN channel layer are more under compressive strain, which lead to an overall better crystalline quality, resulting in an increased electron mobility of the 2DEG.

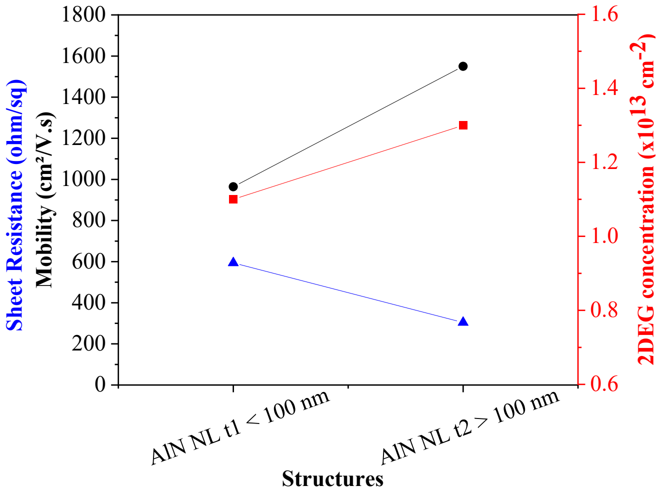


Figure 3.11.: 2DEG electrical properties for the AlGaN/GaN HEMT heterostructures grown on Si(111) using step-graded $Al_xGa_{1-x}N$ buffer layers and AlN NL t_1 < 100 nm or AlN NL t_2 > 100 nm.

III.1. Device fabrication

This study has been carried out using the optical mask-set "BreakUp" in order to simplify the fabrication process and evaluate the epitaxial structures mostly through breakdown voltage and DC characterizations. Device processing started with the formation of the source and drain ohmic contacts by partially etching the AlGaN barrier layer with BCl_3/SF_6 plasma in an ICP reactor prior to the metallization. A Ti/Al/Ni/Au metal stack was deposited and annealed at 800 °C. The contact resistance extracted by TLM method is about 0.6 Ω.mm for both structures. The devices were isolated using Nitrogen implantation. Then, Ni/Au gates of 3 µm length were defined by optical lithography. Finally, the devices were passivated with 150 nm PECVD SiN prior to the Ti/Au pads deposition enabling electrical measurements.

III.2. Breakdown characterization

Typical lateral leakage characteristics of the heterostructures at room temperature measured on several locations across the samples and between two isolated ohmic contacts of 5 µm distance are shown in **Figure 3.12.a**. Despite the submicron thick epi-stack, the distribution of the leakage current is rather uniform [153]. Additionally, it is observed that a leakage current below 100 µA/mm all the way to 225 V for the structure with AlN NL t_1 < 100 nm and up to 200 V for the one with AlN NL t_2 > 100 nm. Furthermore, the heterostructure with

AlN NL $t_1 < 100$ nm displays a plateau, maintaining the leakage below 10 µA/mm up to 225 V. However, this plateau is absent in the AlN NL $t_2 > 100$ nm heterostructure.

Figure 3.12.b shows typical vertical leakage characteristics of the heterostructures at room temperature measured on several locations across the samples. Despite the submicron thick epi-stack, the leakage current distribution is rather uniform showing that a thick buffer is not mandatory to maintain a high material quality close to the 2DEG. It can also be noticed that a leakage current below 1 mA/cm² is observed up to 400 V with a hard breakdown voltage of 500 V for AlN NL $t_1 < 100$ nm. This results in a remarkable vertical breakdown field higher than 6 MV/cm (calculated by normalizing the hard breakdown voltage with the total epi-stack thickness), which is significantly higher than the theoretical value of 3 MV/cm for GaN. On the other hand, it can be pointed out that an AlN NL t_2 thicker than t_1 using the same epi-stack results in a much larger leakage current. Indeed, a leakage current below 1 mA/cm² is observed at 250 V with a hard breakdown voltage of 400 V for AlN NL $t_2 > 100$ nm.

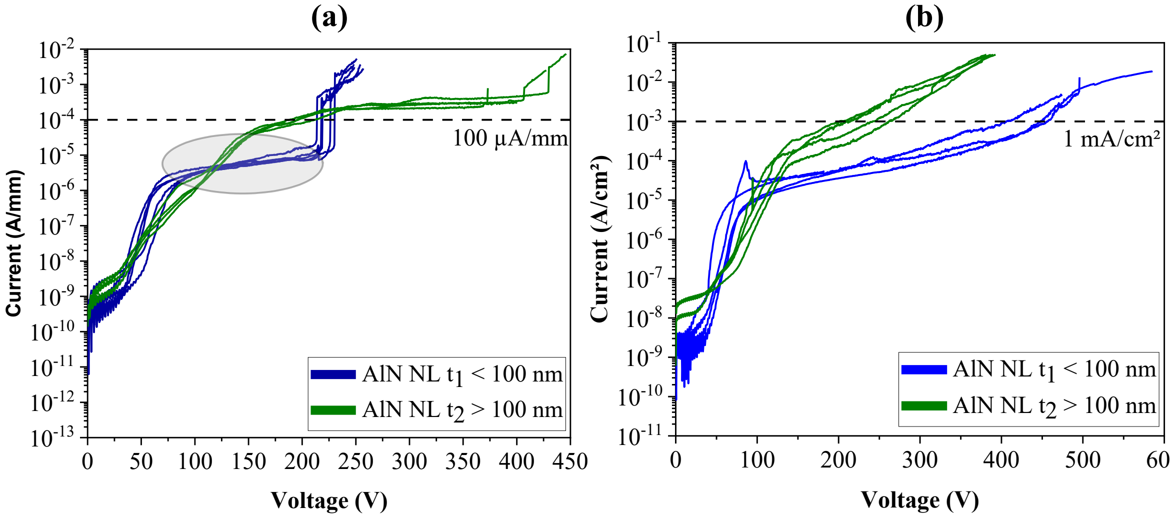


Figure 3.12.: (a) Lateral and (b) Vertical breakdown voltage characteristics of AlGaN/GaN HEMTs with submicron thick three step-graded $Al_xGa_{1-x}N$ buffer layers and AlN NL $t_1 <$ 100 nm or AlN NL $t_2 > 100$ nm.

The three-terminal off-state breakdown voltage has been measured with $L_G = 3$ µm at $V_{GS} = -4$ V for various gate to drain distance varying from 5 µm to 40 µm and for AlN NL t_1 and t_2 as shown in **Figure 3.13**. It can be noticed that a drain leakage current well below 100 µA/mm up to $V_{DS} = 200$ V is observed regardless of the device design for AlN NL $t_1 < 100$ nm while the AlN NL $t_2 > 100$ nm transistors deliver two orders of magnitude larger leakage current even at lower bias. For both thicknesses, the transistor breakdown voltage of about 250 V is independent of the gate to drain distance due to the thin heterostructure.

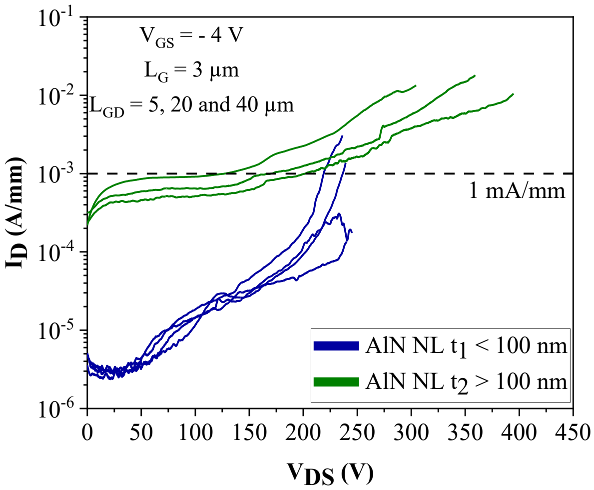
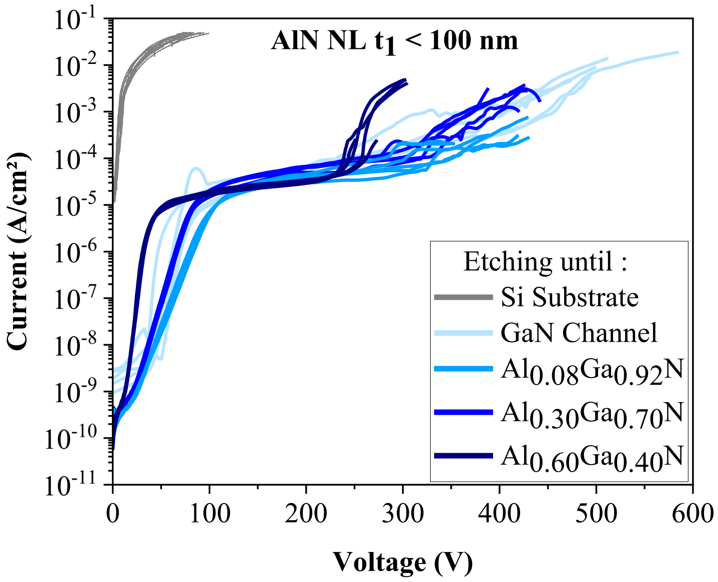


Figure 3.13.: Three terminal off-state breakdown voltage characteristics with L_G = 3 µm and L_{GD} = 5, 20 and 40 µm at V_{GS} = -4 V of 2×50 µm transistor AlGaN/GaN HEMTs with submicron thick three step-graded $Al_xGa_{1-x}N$ buffer layers and AlN NL t_1 < 100 nm or AlN NL t_2 > 100 nm.

III.3. Decomposition of the three step-graded $Al_xGa_{1-x}N$ buffer layers

To better understand the origin of the outstanding vertical breakdown characteristics, a decomposition study of the structure with AlN NL t_1 < 100 nm by etching several samples down to the different epilayers: GaN channel, $Al_{0.08}Ga_{0.92}N$, $Al_{0.30}Ga_{0.70}N$, $Al_{0.60}Ga_{0.40}N$ and Si substrate was performed (**Figure 3.14**). The structure was first etched down to the substrate, which shows a vertical breakdown voltage lower than 100 V. For all the other samples, this value was subtracted in order to remove the electrical contribution of the substrate on the vertical breakdown voltage. The full stack, as shown previously, exhibited a vertical breakdown voltage around 500 V, resulting in an excellent breakdown field of 6.3 MV/cm. The structure etched down to the first AlGaN buffer layer with 8 % Al contents showed an increase of the breakdown field of 9.6 MV/cm. Subsequently, the structure etched down to the second AlGaN buffer layer with 30 % Al content achieved 12 MV/cm breakdown field. Finally, the structure etched until the last layer of the AlGaN buffer layer with 60 % Al contents reached an impressive 15 MV/cm breakdown field. The vertical breakdown voltage of the different decomposed structures shows that the remarkable breakdown field is clearly attributed to the insertion of Al-rich AlGaN into the buffer layers combined with an optimized AlN NL offering outstanding breakdown strength of about 15 MV/cm, close to the theoretical value of AlN [155].



Channel	$Al_{0.08}Ga_{0.92}N$	$Al_{0.30}Ga_{0.70}N$	$Al_{0.60}Ga_{0.40}N$	
6.3	9.6	12.1	15	Breakdown Field (MV/cm)

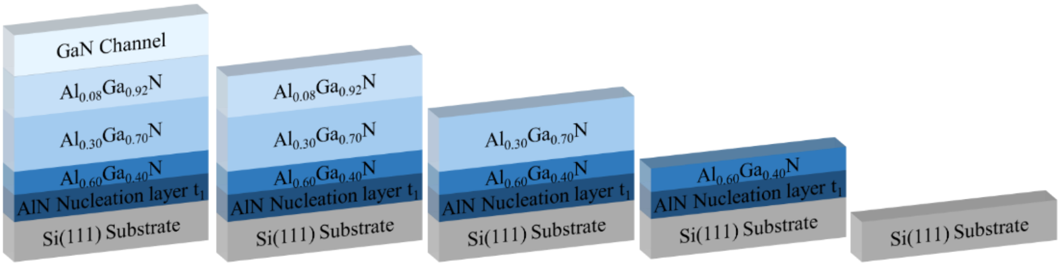


Figure 3.14.: Vertical breakdown voltage and breakdown field characteristics of the decomposed three step-graded $Al_xGa_{1-x}N$ buffer layers and the Si(111) substrate.

Figure 3.15 illustrates a benchmark of GaN on Si HEMTs buffer breakdown field as a function of the total stack thickness. Notably, the breakdown field found in the literature is typically lower compared to the breakdown field of pure GaN material. Historically, achieving a high breakdown voltage required the use of very thick structures, leading to a degradation of the overall thermal dissipation. However, in this study, state-of-the-art buffer breakdown field for submicron thick heterostructures was achieved. This accomplishment was made possible by introducing Al-rich AlGaN into the buffer layers, combined with an optimized AlN NL $t_1 < 100$ nm. The outcome is an exceptional breakdown strength of approximately 6.3 MV/cm, showcasing a remarkable improvement in the performance of the buffer compared to traditional approaches.

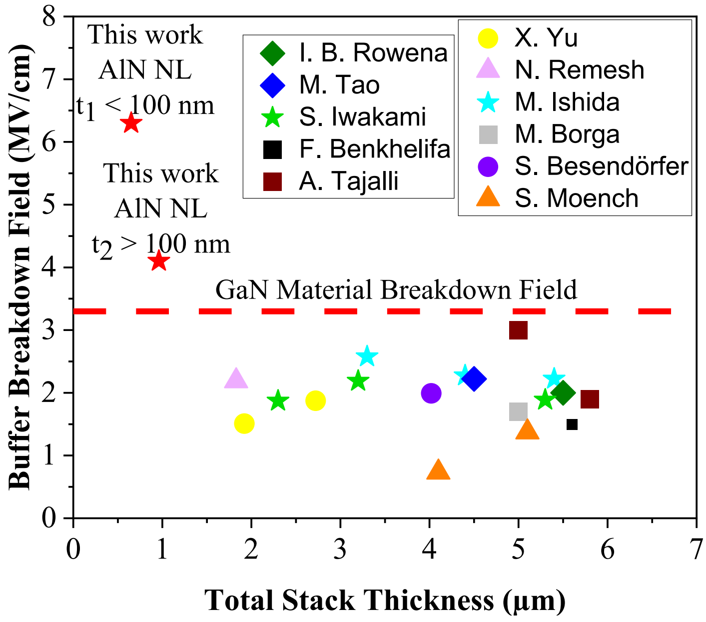


Figure 3.15.: Benchmark of GaN on Si HEMTs buffer breakdown field as a function of the total stack thickness[90–100].

IV. Impact of the in-situ surface passivation

In this section the importance of the in-situ surface passivation is highlighted. Indeed, as presented in **section II.4** one challenge that remains unresolved pertains to the presence of trapping effects within the structure. These effects may stem from either the buffer or the surface. Hence, an examination of heterostructures with an identical buffer but differing in surface passivation was undertaken in order to assess the full potential of the submicron thick buffer.

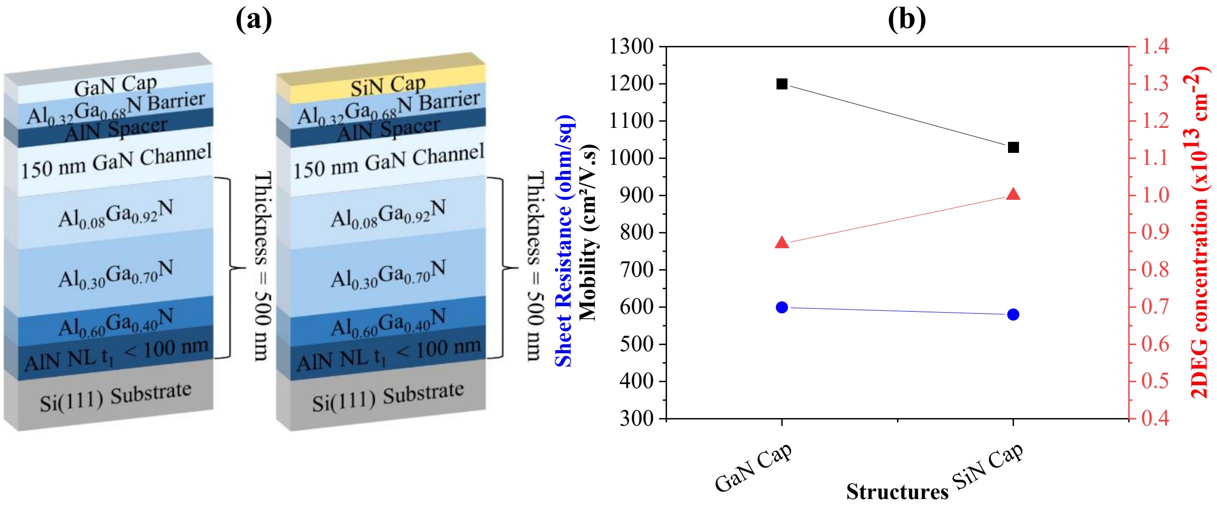


Figure 3.16.: (a) Schematic cross section and (b) 2DEG electrical properties for the two submicron thick AlGaN/GaN HEMTs used in the in-situ surface passivation study.

To achieve this, the optimized structure featuring submicron three step-graded AlGaN buffer layers and an AlN NL with $t_1 > 100$ nm was replicated and capped with less than 1 nm thick in-situ SiN passivation. Unlike MOCVD, MBE assisted by RHEED, allows for in-situ monitoring of the barrier/SiN interface formation. This capability facilitates the adjustment of growth parameters to optimize the interface and achieve high-quality in-situ SiN cap passivation with a thickness of less than 1 nm [156].The 2DEG properties were extracted at room temperature through Hall effect measurements, revealing a charge density of 0.9 × 10^{13} cm^{-2} and 1.0 × 10^{13} cm^{-2}, along with an electron mobility values of 1200 cm²/V.s and 1030 cm²/V.s for the GaN cap and SiN cap heterostructures, respectively (**Figure 3.16.b**).

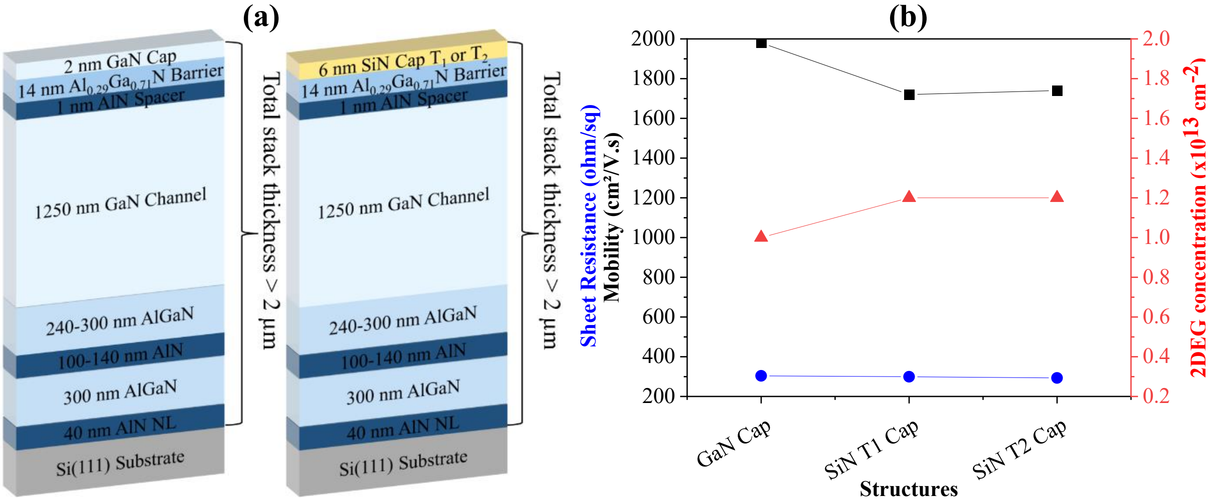


Figure 3.17.: (a) Schematic cross section and (b) 2DEG electrical properties of the AlGaN/GaN HEMTs provided by CRHEA for the in-situ surface passivation study.

Simultaneously, a parallel investigation was conducted on three additional heterostructures provided by CRHEA. This allowed for the examination of trapping effects with a conventional buffer with a total stack thickness exceeding 2 µm. Grown via NH_3-MBE on Si(111) substrates, these heterostructures consist of a 40 nm AlN NL, 300 nm AlGaN layer, 100-140 nm AlN interlayer, 240-300 nm AlGaN layer, 1250 nm GaN channel, 1 nm AlN spacer, and a 14 nm $Al_{0.29}Ga_{0.71}N$ barrier. One of the structures was capped with 2 nm GaN, while the other were capped with 6 nm SiN (**Figure 3.17.a**).

One of the SiN is deposited at the GaN growth temperature, which is 800°C (T_1). The other SiN is initially deposited at 800°C, and then the growth temperature was increased at T_2 > T_1. The 2DEG properties were extracted at room temperature through Hall effect measurements, revealing a charge density of 1.0 × 10^{13} cm^{-2} and 1.2 × 10^{13} cm^{-2}, along with electron mobility values of 1980 cm²/V.s and 1720 cm²/V.s for the GaN cap and both SiN cap heterostructures, respectively (**Figure 3.17.b**). This comprehensive approach enables a meticulous examination of trapping effects and their origins within distinct heterostructures, providing insights into the nuanced interplay between materials and passivation techniques.

IV.1. Device fabrication

This study utilized the optical mask-set "BreakUp" to streamline the fabrication process and assess epitaxial structures through DC and DC pulsed characterizations. The device processing commenced with the creation of source and drain ohmic contacts, achieved by partially etching the AlGaN barrier layer with BCl_3/SF_6 plasma in an ICP reactor prior to metallization. In the case of heterostructures with SiN cap, the cap underwent a local etching with SF_6 plasma in an RIE reactor. Subsequently, a Ti/Al/Ni/Au metal stack was deposited and annealed at 800 °C, yielding a contact resistance of approximately 0.6 $\Omega\cdot$mm, as extracted by the TLM method. Device isolation was accomplished through Nitrogen implantation. Following this, Ni/Au gates with a length of 3 µm were defined using optical lithography. The SiN beneath the gate was entirely removed via SF_6 plasma etching. Finally, the devices were passivated with a 150 nm PECVD SiN layer followed by the deposition of Ti/Au pads to facilitate electrical measurements.

IV.2. DC and DC pulsed characterization

Output and transfer characteristics of 2 × 50 µm transistors with L_G = 3 µm and L_{GD} = 5 µm on the heterostructures provided by CRHEA are shown in **Figure 3.18**. The gate source voltage was swept from −6 to +2 V with a step size of 1 V. A maximum drain current $I_{D,max}$ of 0.71 A/mm for the GaN cap and 0.77 A/mm for both SiN cap heterostructures have been measured (see **Figure 3.18.a**). **Figure 3.18.b** displays the transfer characteristics with a compliance fixed at 150 mA/mm and swept from V_{DS} = 2 to 20 V using a step of 1 V. A low threshold voltage shift as a function of V_{DS} is observed with a drain leakage current lower than 100 µA/mm on each heterostructures.

Pulsed I_D–V_{DS} characteristics revealing the charge trapping effects when using various quiescent bias points are depicted in **Figure 3.18.c**. The open channel DC pulsed measurements are shown at V_{GS} = +2 V with various quiescent drain voltages at room temperature. The structure with a GaN cap exhibits a pronounced gate lag. Specifically, the GaN cap structure shows a current collapse exceeding 40 % under drain lag conditions at 20 V, while the structure with a SiN cap T_1 exhibits a reduced gate lag with a current collapse around 10% under the same conditions. This indicates that the SiN T_1 cap efficiently passivate the surface states and significantly decrease the trapping effects. However, when comparing the two SiN caps, the influence of the growth temperature on traps becomes evident (**Figure 3.18.c**). Indeed, the drain lag varies significantly depending on the temperature. The heterostructure with the SiN T_2 cap shows an increase of the drain lag at 20V with a current collapse reaching 50 %. It can be inferred that the implementation of a SiN cap at an optimum growth temperature helps reducing surface traps and, consequently, mitigates gate lag and drain lag phenomena.

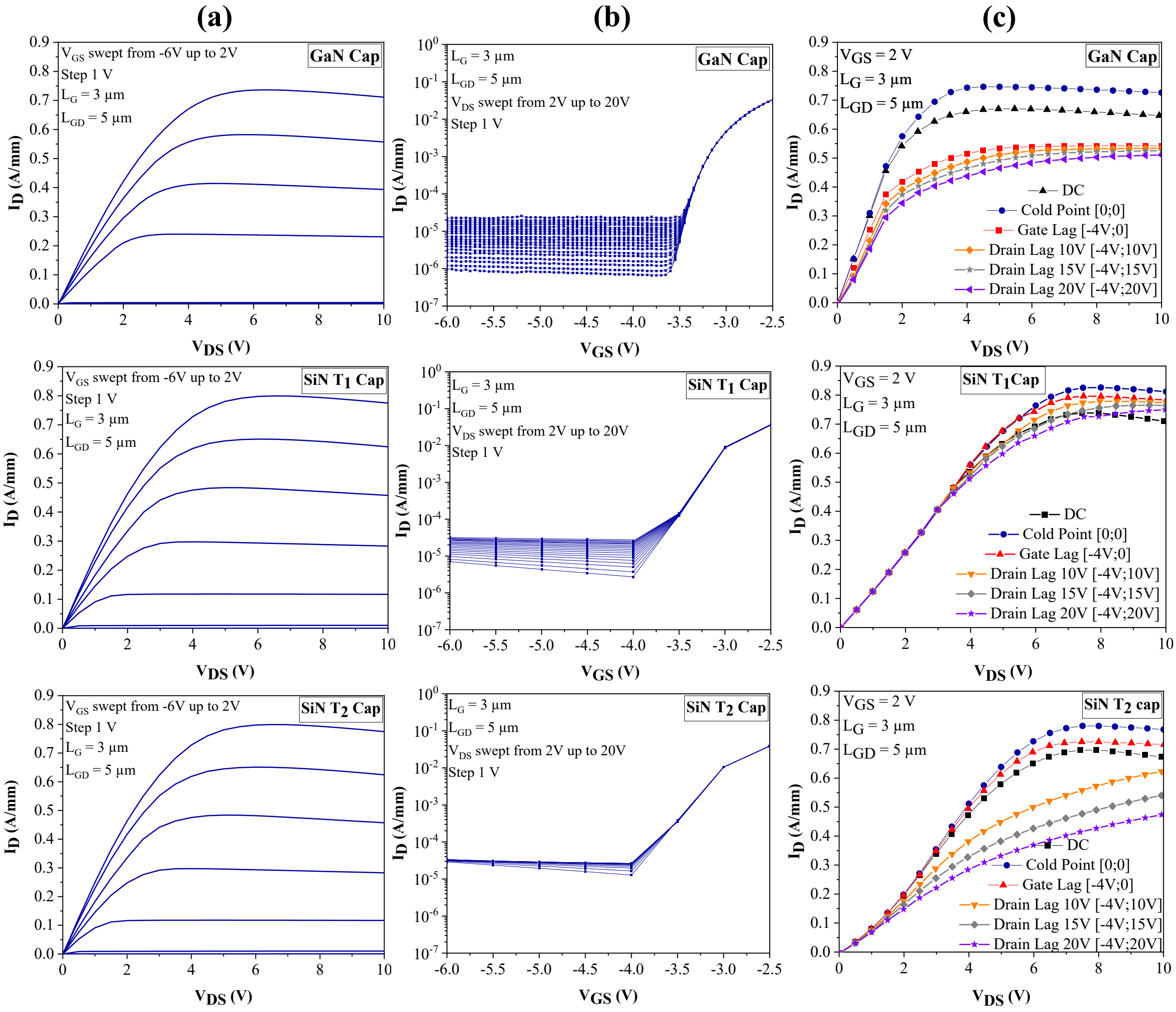


Figure 3.18.: (a) Output characteristics, (b) transfer characteristics, and (c) open channel pulsed I_D-V_{DS} output characteristics of a 2 × 50 µm AlGaN/GaN HEMT provided by CRHEA with L_{GD} = 5 µm and L_G = 3 µm.

The comparison of the DC and DC pulsed characteristics of the optimized submicron thick heterostructures with a GaN cap and SiN cap are shown in **Figure 3.19**. Output and transfer characteristics of 2 × 50 µm transistors with L_G = 3 µm and L_{GD} = 5 µm are shown in **Figure 3.19.a and b**. The gate source voltage was swept from −6 to +2 V with a step size of 1 V. A maximum drain current $I_{D,max}$ of 0.50 A/mm for the GaN cap heterostructure and 0.53 A/mm for the SiN cap heterostructure have been measured (see **Figure 3.19.a**). **Figure 3.19.b** displays the transfer characteristics with a compliance fixed at 150 mA/mm and swept from V_{DS} = 2 to 20 V using a step of 1 V. A low threshold voltage shift as a function of V_{DS} is observed with a drain leakage current lower than 10 µA/mm in both cases.

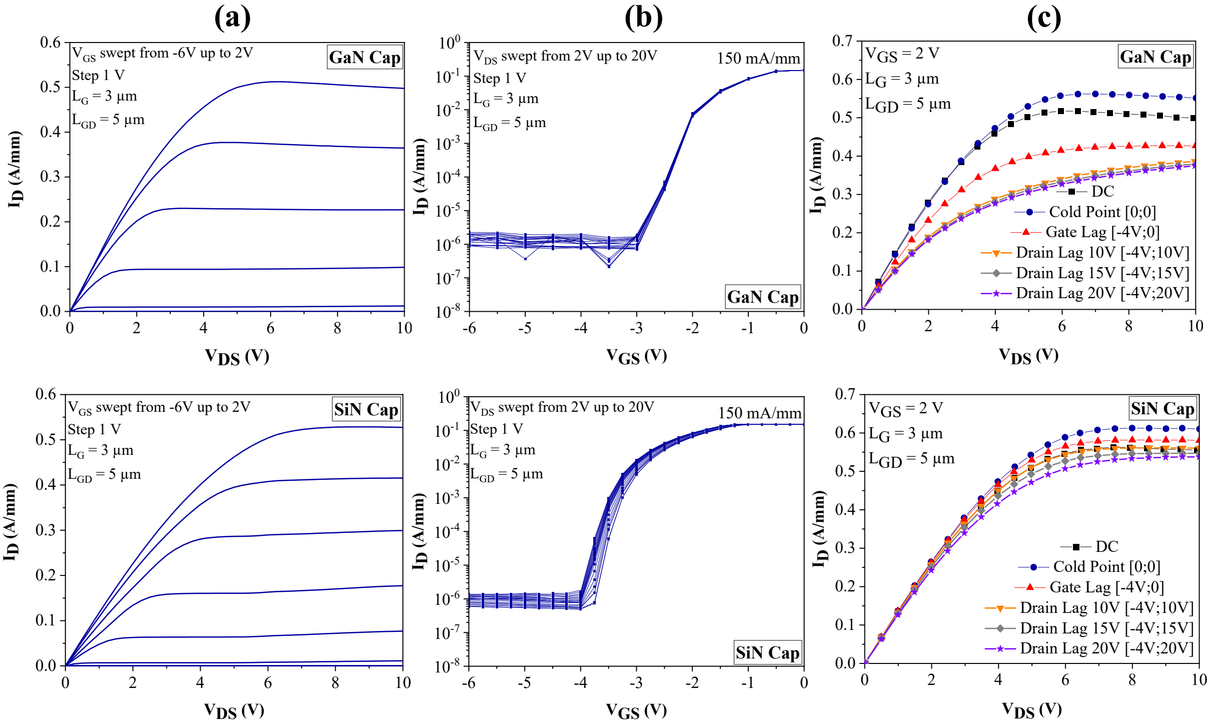


Figure 3.19.: (a) Output characteristics, (b) transfer characteristics, and (c) open channel pulsed I_D-V_{DS} output characteristics of the submicron thick 2 × 50 µm AlGaN/GaN HEMT with L_{GD} = 5 µm and L_G = 3 µm.

Pulsed I_D–V_{DS} characteristics revealing the charge trapping effects when using various quiescent bias points are depicted in **Figure 3.19.c**. The open channel DC pulsed measurements are shown at V_{GS} = +2 V with various quiescent drain voltages at room temperature. The structure with a GaN cap exhibits both high gate and drain lag. More precisely, the GaN cap structure shows a current collapse exceeding 40 % for a drain lag 20 V, while the structure with a SiN cap demonstrates a reduced gate and drain lag, resulting in a lower current collapse around 10% under drain lag at 20 V. This further confirms that the SiN cap deposited in-situ by MBE efficiently passivates the surface states and significantly decreases the trapping effects in our heterostructure.

V. Preliminary results under high electric field

The epitaxial structure, as illustrated in **Figure 3.20**, is designed with an optimized AlN nucleation layer thickness (t_1 < 100 nm) to accommodate the lattice mismatch between the buffer and the substrate. This is followed by the optimized buffer layers, comprising three-step-graded AlGaN buffer layers ($Al_{0.60}Ga_{0.40}N$, $Al_{0.30}Ga_{0.70}N$, $Al_{0.08}Ga_{0.92}N$), and then a 150 nm thick GaN channel. A 14 nm $Al_{0.32}Ga_{0.68}N$ barrier layer is subsequently grown. Finally, the structure is capped with an in-situ SiN layer to passivate the surface states. These HEMT epitaxial structures serve as a starting point for demonstrating a first combination of reduced trapping effects and proper electron confinement under high electric field. The electrical properties of the heterostructure were characterized using Hall effect measurements at room temperature, revealing a charge density of 1.0 × 10^{13} cm^{-2}, along with an electron mobility value of 1030 $cm^2/V.s$.

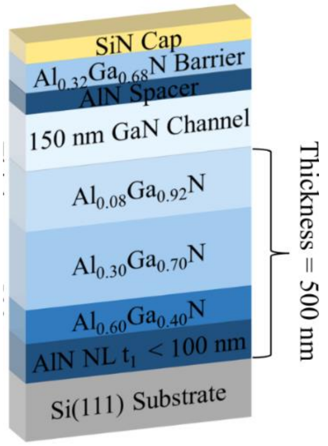


Figure 3.20.: Schematic cross-section of the ultrathin AlGaN/GaN HEMTs with an AlN NL t_1 < 100 nm, three step-graded $Al_xGa_{1-x}N$ buffer layers and in-situ SiN cap.

V.1. Device fabrication

In order to assess the full potential of the structure with the submicron three step-graded $Al_xGa_{1-x}N$ buffer, the AlN NL t_1 < 100 nm and capped with SiN the e-beam mask-set “GaN Fast” was used.

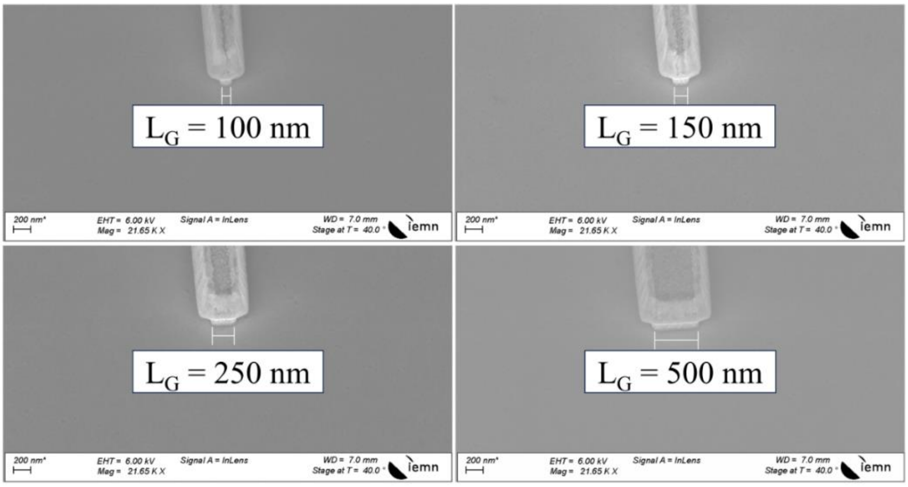


Figure 3.21.: SEM image of different gate lengths process by e-beam lithography.

A Ti/Al/Ni/Au metal stack annealed at 800°C has been used after partially etching the barrier with BCl_3/SF_6 plasma in an ICP reactor to form source-drain ohmic contacts. The contact resistance extracted by TLM method is about 0.6 Ω.mm. Ti/Au T-gates were defined by e-beam lithography. The SiN underneath the gate was fully removed using an SF_6 plasma etching through the e-beam lithography. **Figure 3.21** shows various gate lengths available in the mask-set varying from 500 nm to 100 nm enabling to evaluate the impact of the gate length (e.g. electric field) on the electron confinement. Finally, 200 nm PECVD SiN layer was deposited as final passivation prior to the deposition of Ti/Au pads to facilitate electrical measurements.

V.2. DC and small signal characterization

Figures 3.22 and 3.23 shows typical output and transfer characteristics of 2 × 50 µm transistors with L_{GD} = 500 nm and for various gate lengths, ranging from 500 nm to 100 nm. Transfer characteristics with a compliance fixed at 150 mA/mm and swept from V_{DS} = 2 V to 30 V using a step of 1 V, are depicted in **Figure 3.22**. Each gate length exhibits a minimal threshold voltage shift as a function of V_{DS} under high electric field up to 30 V. This observation confirms proper electron confinement within the 2DEG of the sub-micron step-graded $Al_xGa_{1-x}N$ buffer, as reflected by a low DIBL well below 50 mV/V for each gate length. Additionally, it is noteworthy that the off-state drain leakage current remains below 1 µA/mm up to V_{DS} = 30 V for each gate length.

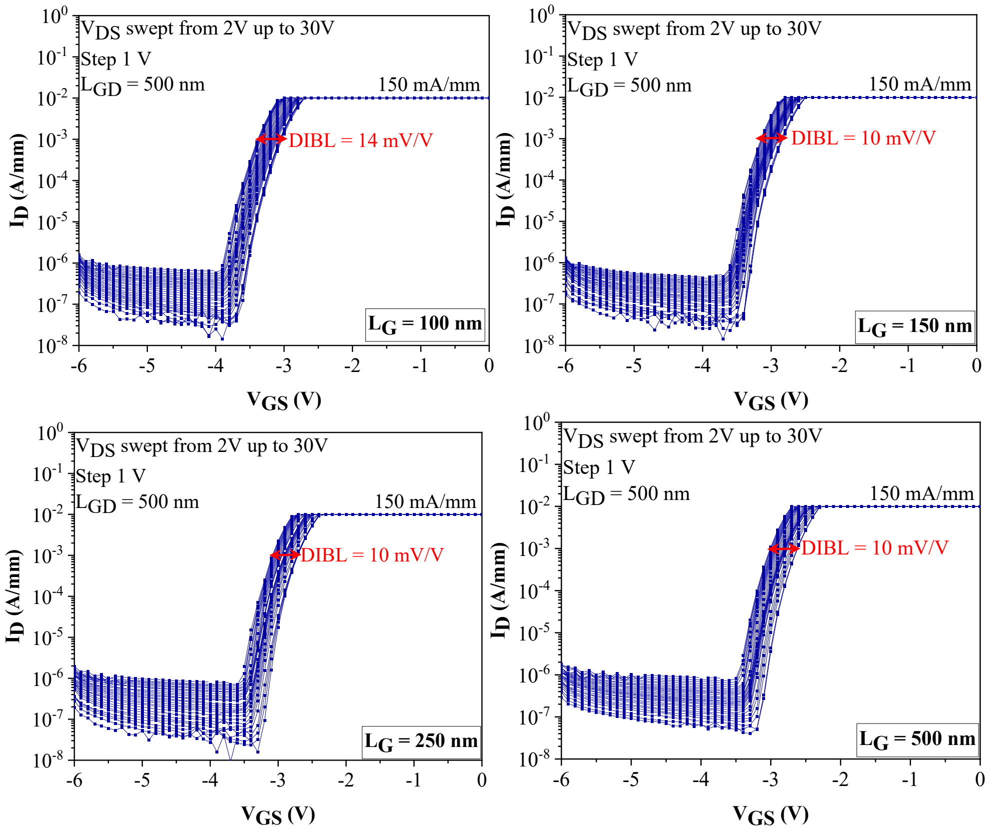


Figure 3.22.: Transfer characteristics of submicron thick 2 × 50 µm AlGaN/GaN HEMT with L_{GD} = 5 µm and L_G ranging from 500 nm to 100 nm.

Figure 3.23 shows some basic DC parameters as a function of the gate length for L_{GD} = 500 nm. As expected, an increase of $I_{D,max}$ and $G_{m,max}$ is observed by reducing the gate length (**Figure 3.23.a and 3.23.b**) . As mentioned previously, the leakage current shown in **Figure 3.23.c**, is well below 1 µA/mm at V_{DS} = 10 V for all gate lengths, which reflects the high material and processing quality of the structure. However, a drop of V_{TH} when the gate length is shrinked due to short channel effects is observed (**Figure 3.23.d**).

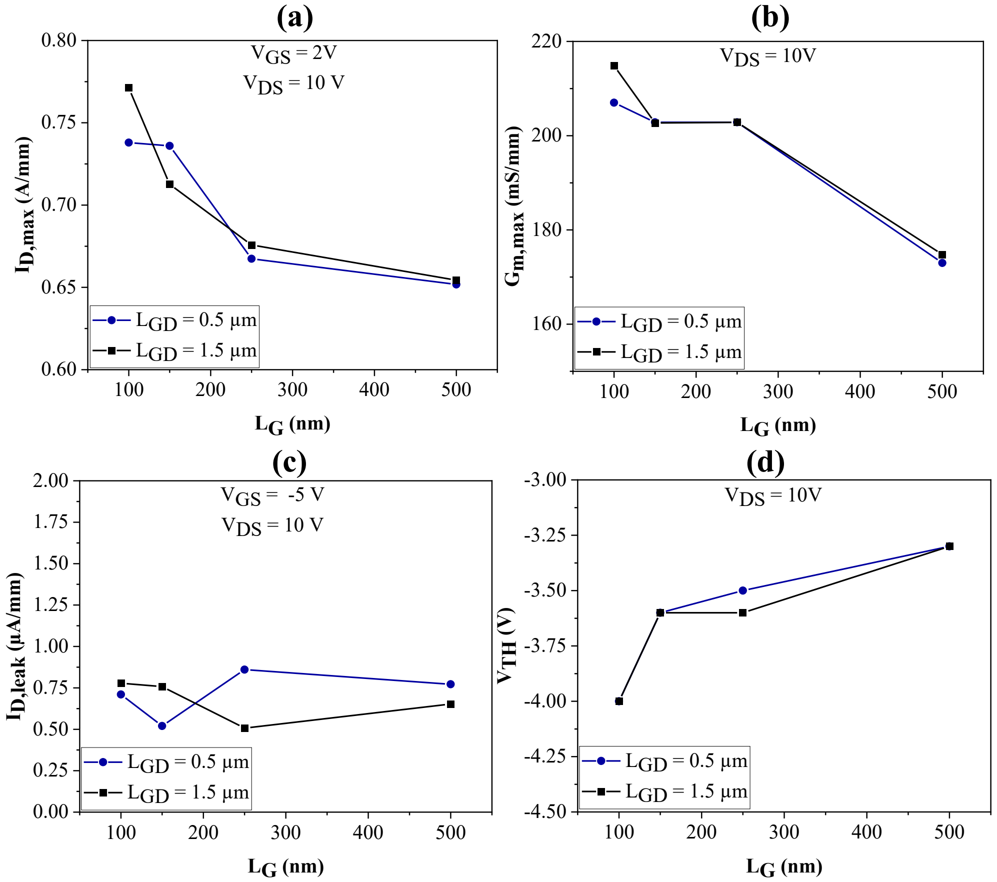


Figure 3.23.: (a) $I_{D,max}$, (b) $G_{m,max}$, (c) $I_{D,leak}$, and (d) V_{TH} as a function of gate length with L_{GD} = 500 nm of submicron thick 2 × 50 µm AlGaN/GaN HEMTs.

The S-parameters were measured from 250 MHz to 67 GHz for L_{GD} = 500 nm and various gate lengths, ranging from 500 nm to 100 nm, as illustrated in **Figure 3.24**. The current gain extrinsic cut-off frequency (F_T) is approximately 37 GHz for L_G = 100 nm but does not properly scale for short L_G (depicted in **Figure 3.24.a**) due to short channel effects resulting from an excessively thick barrier. The maximum oscillation frequency (F_{MAX}) increases with V_{DS} up to 153 GHz for L_G = 100 nm (**Figure 3.24.b**). An F_T/F_{MAX} ratio of 37/153 GHz is achieved at V_{DS} = 20 V with L_{GD} = 500 nm and L_G=100 nm (**Figure 3.24.d**). The F_{MAX}/F_T ratio is affected by the unfavorable aspect ratio: gate length / gate-to-channel distance. At 10 GHz a high maximum Gain (U_{MAX}) of 27 dB is achieved at V_{DS} = 20 V enabling large signal characterization at 10 GHz (**Figure 3.24.c**).

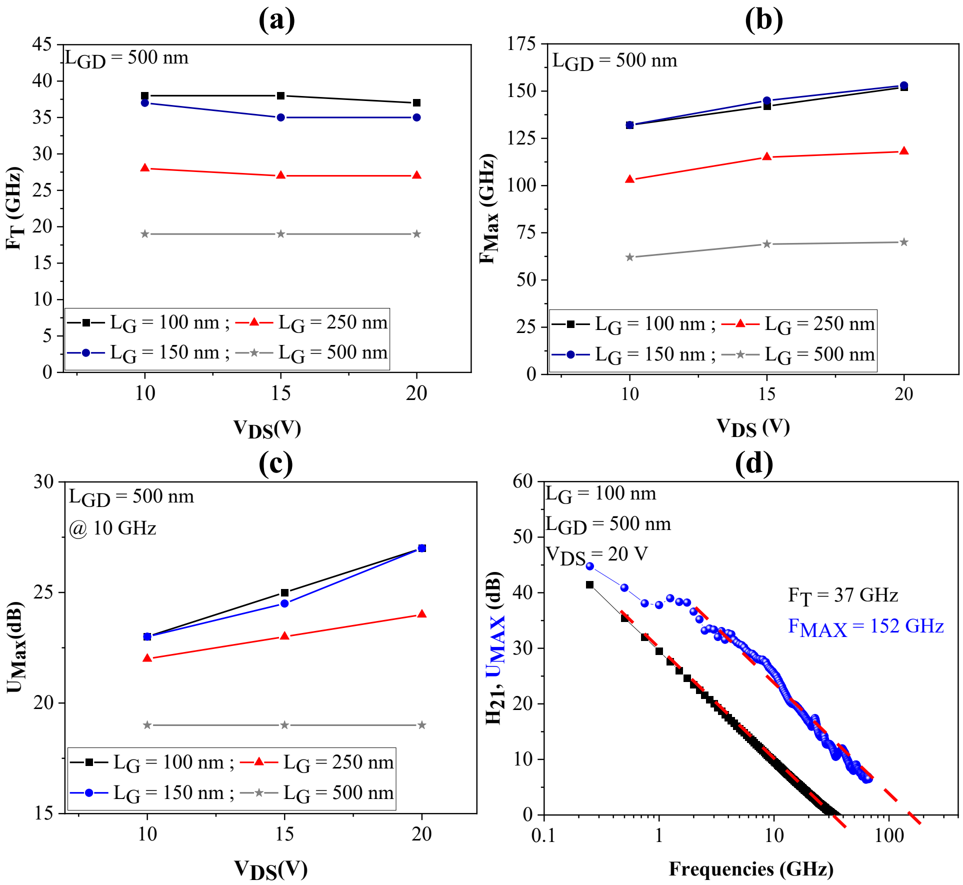


Figure 3.24.: (a) Current gain extrinsic cut-off frequency, (b) maximum oscillation frequency, (c) maximum gain and (d) small signal charcteristics of submicron thick 2 × 50 µm AlGaN/GaN HEMT with L_{GD} = 500 nm for various gate lengths.

V.3. Large signal characterization 10 GHz

Large signal characterizations have been carried out at 10 GHz. **Figures 3.25.a** and **Figure 3.25.b** show typical power performances of 2 × 50 µm transistors with L_{GD} = 500 nm and L_G = 100 nm at V_{DS} = 10 V and 35 V, respectively. A saturated output power density (P_{OUT}) of 0.6 W/mm associated to a power added efficiency (PAE) of 57.4 % at V_{DS} = 10 V is measured. For V_{DS} = 35 V, a P_{OUT} of 1.6 W/mm associated to a PAE of 30.9 % has been achieved. Moreover, after many Load-Pull sweeps, no degradation of the devices is observed up to V_{DS} = 35 V as seen in **Figure 3.25.c**. This proves that this heterostructure enables high voltage operation without degradation despite the use of a gate length as short as 100 nm. The promising robustness is attributed to the high quality of the submicron thick step-graded $Al_xGa_{1-x}N$ buffer layers. The rather limited output power density is explained by the low maximum drain current of this structure, which is related to the electron mobility that needs to be further enhanced. Finally, the drop of the PAE from V_{DS} = 10 V to 35 V is attributed to the poor thermal dissipation of the Si substrate. Therefore, further optimization of the structure, together with substrate thinning and use of a heat sink should significantly enhance the device's performance.

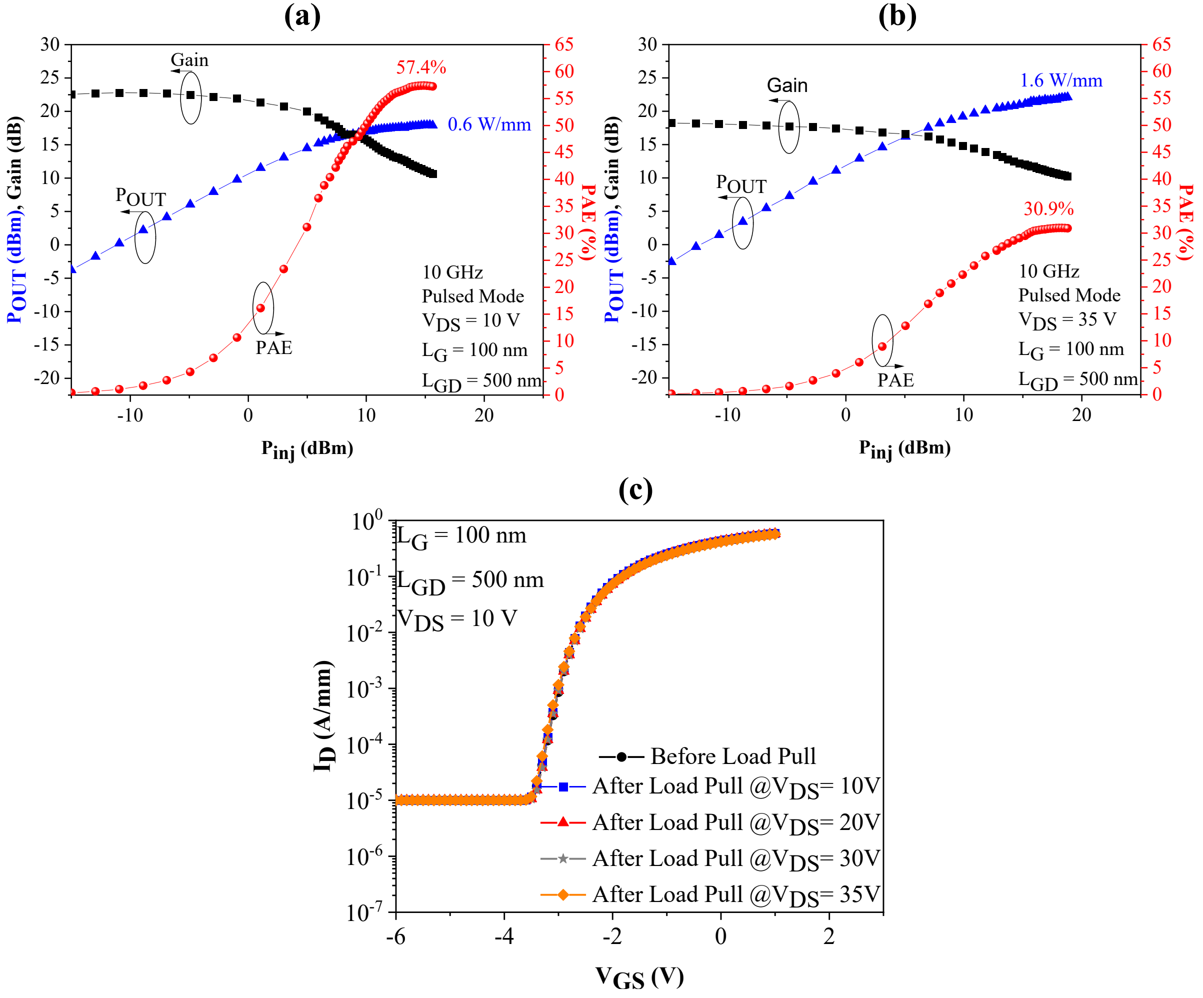


Figure 3.25.: Large signal performances at 10 GHz for a 2 × 50 µm transistor with L_{GD} = 500 nm and L_G = 100 nm at (a) V_{DS} = 10 V and (b) V_{DS}= 35 V. (c) Transfer characteristics after more than 40 Load Pull sweep up to V_{DS} = 35 V.

VI. Conclusion

In this chapter, an in-depth investigation was conducted on submicron thick AlGaN/GaN HEMTs grown on Si (111) substrates, featuring various buffers designed for high-frequency applications. The MBE grown heterostructure, including a total buffer thickness below 650 nm, containing Al-rich step-graded layers ($Al_{0.60}Ga_{0.40}N$, $Al_{0.30}Ga_{0.70}N$, $Al_{0.08}Ga_{0.92}N$), exhibited promising attributes such as an outstanding vertical, lateral, and three-terminal off-state breakdown voltage, along with low RF losses. The DC characteristics revealed fully functional transistors with minimal off-state leakage current.

The experimental analysis of the AlN nucleation layer thickness variation provided insights of its impact on electrical performance. Optimization of the submicron thick step-graded $Al_xGa_{1-x}N$ buffer layer, combined with an optimized AlN nucleation layer thickness, demonstrated a remarkable vertical breakdown field exceeding 6 MV/cm.

Moreover, DC pulsed characterizations were conducted to assess trapping effects, revealing the crucial role of the in-situ passivation. A direct comparison between heterostructures with and without an in-situ SiN cap showcased a significant difference in current collapse, 40% with a GaN cap compared to 10% with the SiN cap. Additionally, the growth temperature of the SiN cap was identified to play a crucial role. Importantly, this analysis underscored that the buffer exhibited low trapping effects, as expected, due to the absence of doping compensation, while maintaining high material quality.

Further investigations were performed on the submicron thick AlGaN/GaN HEMTs, featuring the Al-rich step-graded buffer layers, optimized AlN nucleation layer thickness, and an in-situ SiN cap, grown on Si (111) substrates for high-frequency applications. DC characteristics showed fully functional transistors with low off-state leakage current, even under high electric fields up to 30 V, despite a short gate length of 100 nm. This technology enables transistor operation under high drain bias at high frequencies, demonstrating enhanced robustness. Large signal measurements at 10 GHz were reliably achieved up to V_{DS} = 35 V, attributed to the optimization of the submicron thick step-graded $Al_xGa_{1-x}N$ buffer layer and the optimized AlN NL, enabling high electron confinement under high electric fields. However, small signal characteristics revealed the presence of short-channel effects, emphasizing the importance of reducing the barrier thickness to enhance the frequency performance. To address this, investigations of ultrathin Al-rich barrier layers for millimeter-wave devices were carried out, and the findings will be discussed in **Chapter 4**.

Chapter 4: Towards ultrathin AlN/GaN-on-Si HEMT for millimeter-wave devices

I. Introduction

Even though AlGaN/GaN-based HEMTs represent the most mature technology [85, 157–162], mitigating short-channel effects is imperative to enhance their frequency performance while scaling down device dimensions. Consequently, gate length scaling must be accompanied by a reduction in the gate-to-channel distance to avoid short-channel effects [73, 163]. Ultrathin AlN barriers emerge as preferable materials for the millimeter-wave range to avoid gate recess, a known factor contributing to device reliability degradation [164]. Additionally, the ultrathin barrier AlN/GaN heterostructure holds promise for the mm-wave range due to its potential for highly scalable epitaxial structures while maintaining high current density. This chapter presents a comprehensive comparison of device performances between ultrathin submicron-thick GaN-on-Si HEMT structures utilizing AlGaN and AlN barrier layers. Following this comparison, advanced structural and electrical characterizations of the AlN/GaN-on-Si HEMT are conducted.

II. Ultrathin AlGaN/GaN vs AlN/GaN HEMTs

The epitaxial layer structures are based on two submicron thick AlGaN/GaN and AlN/GaN heterostructures grown by NH_3-MBE on 4 inch high-resistivity Si (111) substrates ($\rho > 5$ kΩ.cm) using a RIBER MBE49 growth reactor. **Figure 4.1** shows the cross section of the HEMT structures. It consists of a high quality, lower than 100 nm, AlN NL, followed by a three step-graded $Al_xGa_{1-x}N$ buffer layers ($Al_{0.08}Ga_{0.92}N$/$Al_{0.30}Ga_{0.70}N$/ $Al_{0.60}Ga_{0.40}N$) and a 150 nm thick undoped GaN channel layer. Two different barrier layers of 14 nm thick $Al_{0.32}Ga_{0.68}N$ and 7 nm thick AlN have been used in order to check the impact on the device performances. The 7 nm thick AlN ultrathin barrier layer is used to benefit from both a high polarization and a high aspect ratio L_G/a. Finally, the structures were capped by less than 1 nm thick in-situ SiN layer. The total stack thickness is less than 650 nm in both structures.

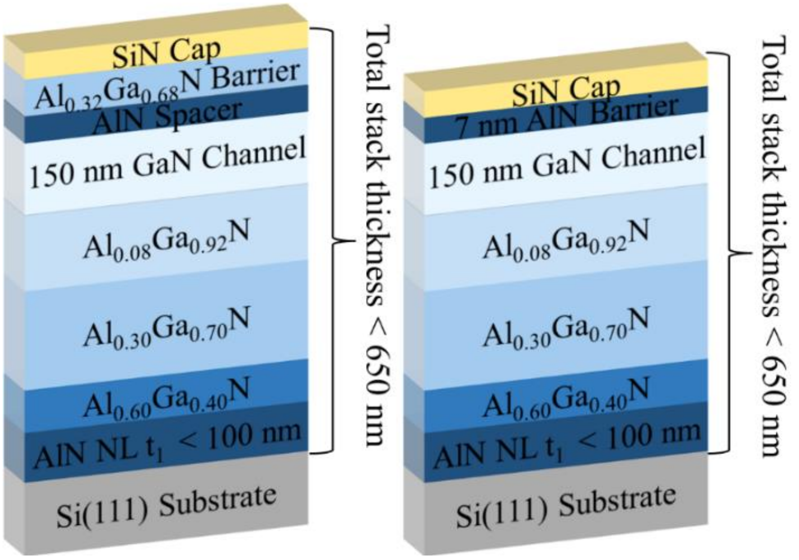


Figure 4.1.: Schematic cross section of submicron thick AlGaN/GaN and AlN/GaN HEMTs grown on Si(111) substrate using a step-graded $Al_xGa_{1-x}N$ buffer layers.

The 2DEG properties were extracted at room temperature through Hall effect measurements, revealing a charge density of 1.0 × 10^{13} cm^{-2} and 1.8 × 10^{13} cm^{-2}, along with electron mobility values of 1030 cm²/V.s and 745 cm²/V.s for the AlGaN/GaN and the AlN/GaN structures, respectively (**Figure 4.2**).

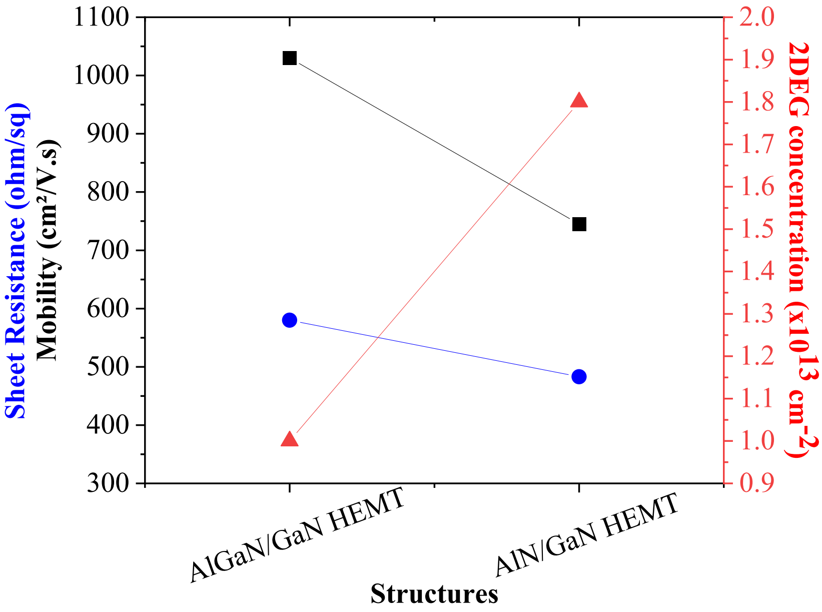


Figure 4.2.: 2DEG electrical properties of submicron thick AlGaN/GaN and AlN/GaN HEMTs grown on Si(111).

II.1. Device fabrication

The fabrication process has been carried out using the e-beam mask-set “GaN Fast”. Similar process has been applied on both structures for proper comparison. Device processing started with the formation of the source and drain ohmic contacts. The AlGaN barrier layer was partially etch with BCl_3/SF_6 plasma in an ICP reactor prior to the metallization while the contacts were directly deposit on the AlN barrier. A Ti/Al/Ni/Au metal stack was used and annealed at 800°C and 850°C yielding contact resistances of 0.6 Ω.mm and 0.4 Ω.mm for the AlGaN/GaN and the AlN/GaN structures, respectively. The devices were isolated using Nitrogen implantation. Then, Ni/Au T-gates ranging from 140 nm to 500 nm gate lengths were defined by e-beam lithography (**Figure 4.3**). The SiN underneath the gate was fully removed using an SF_6 plasma etching through the e-beam lithography. Finally, the devices were passivated with 200 nm PECVD Si_3N_4 prior to the Ti/Au pads deposition.

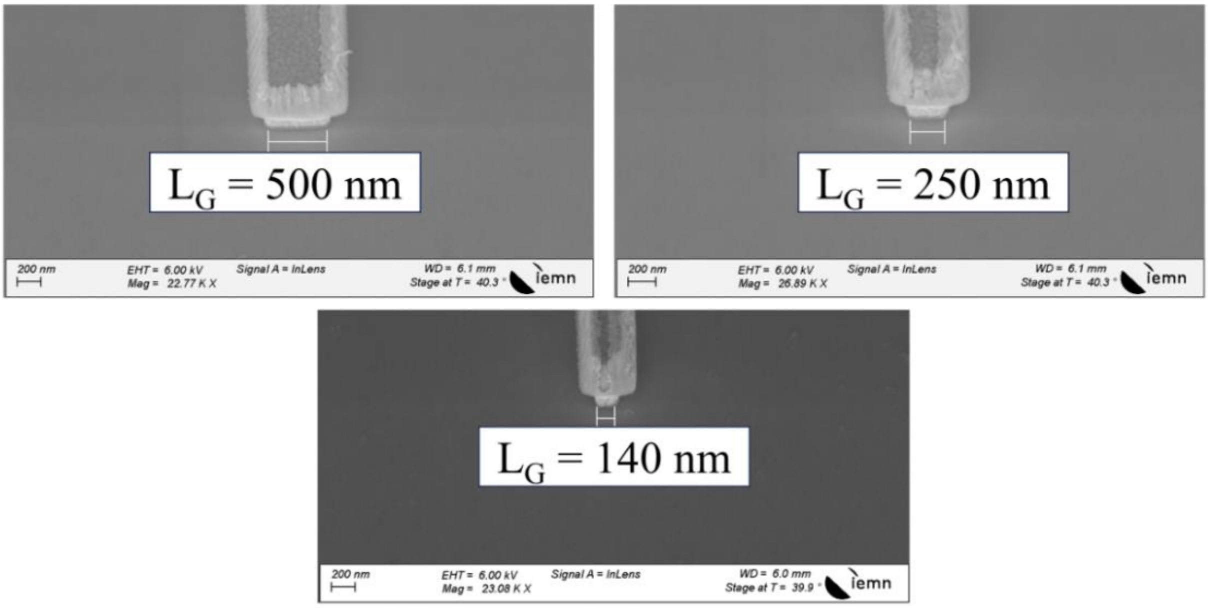


Figure 4.3.: SEM image of different gate lengths processed by e-beam lithography.

II.2. DC and small signal characterization

Figures 4.4 and 4.5 shows typical output and transfer characteristics of 2 × 50 µm transistors with L_G = 140 nm and L_{GD} = 500 nm. The gate source voltage was swept from −6 to +2 V with a step size of 1 V. A maximum drain current $I_{D,max}$ of about 0.74 A/mm and 1.0 A/mm have been measured for the AlGaN and AlN barrier, respectively (**Figure 4.4.a**) despite the rather limited electron mobility. A pinch-off voltage $V_{TH} = -3.4$ V for the AlGaN barrier and $V_{TH} = -2.2$ V for the AlN barrier (shown in **Figure 4.5.a and 4.5.b**) are observed with a drain leakage current lower than 10 µA/mm for both structures. A maximum extrinsic transconductance ($G_{m,max}$) of 200 mS/mm for the AlGaN barrier and 311 mS/mm for the AlN barrier have been measured (**Figure 4.4.b**). However, these values can be significantly increased by reducing the access resistances and improving the electron mobility.

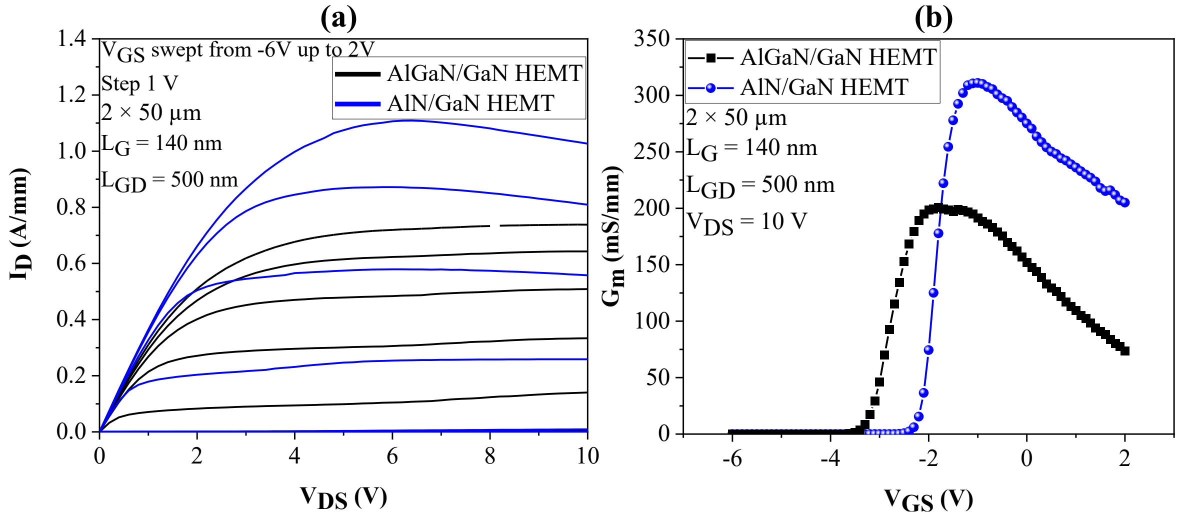


Figure 4.4.: (a) Output characteristics and (b) extrinsic transconductance characteristics at V_{DS} = 10 V of 2 × 50 µm AlGaN/GaN and AlN/GaN HEMTs with L_{GD} = 500 nm and L_G = 140 nm.

Figure 4.5.a and 4.5.b displays the transfer characteristics with a compliance fixed at 150 mA/mm and swept from V_{DS} = 2 to 30 V using a step of 1 V. A low threshold voltage shift as a function of V_{DS} are observed under high electric field up to 30 V, which confirms a proper electron confinement within the 2DEG owing to the proper buffer design (as discussed in the previous chapter) reflected by a low DIBL of 12 and 13 mV/V for the AlGaN and AlN barrier devices, respectively.

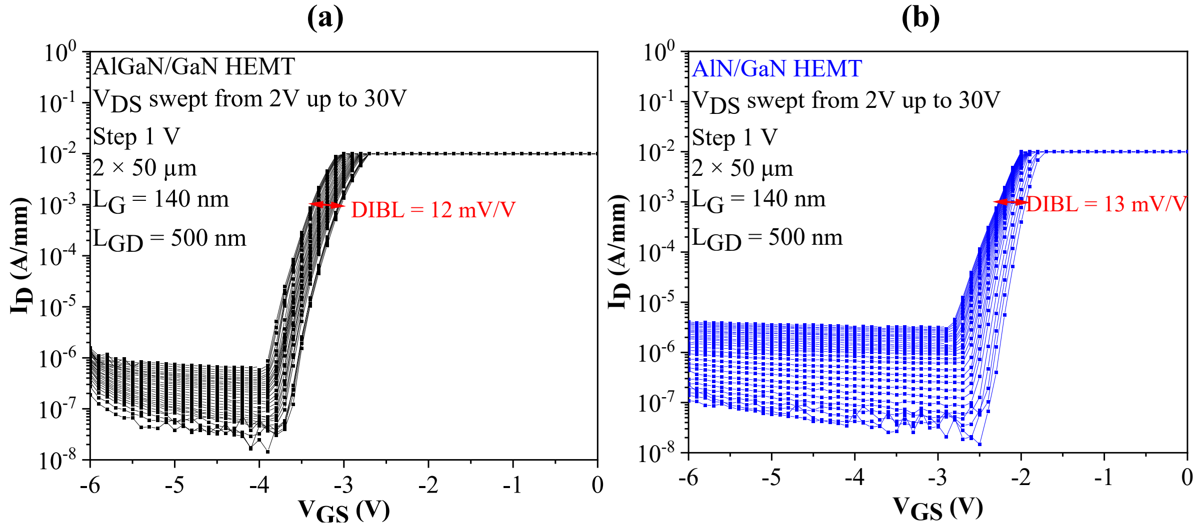


Figure 4.5.: Transfer characteristics of a submicron thick 2 × 50 µm (a) AlGaN/GaN HEMT and (b) AlN/GaN HEMT with L_{GD} = 500 nm and L_G = 140 nm up until V_{DS} = 30 V.

Figure 4.6 shows some basic DC parameters as a function of the gate length for L_{GD} = 500 nm. As expected, an increase of $I_{D,max}$ and $G_{m,max}$ are observed by reducing the gate length (**Figure 4.6.a and 4.6.b**) with about 50% improvement owing to the AlN barrier delivering higher polarization and offering reduced gate to channel distance. As mentioned previously, the leakage current shown in **Figure 4.6.c**, is well below 1 µA/mm at V_{DS} = 10 V for all gate lengths, which reflects the high material and processing quality of both structures. However, the AlGaN barrier shows a higher drop of V_{TH} when the gate length is shrinked due to short channel effects (**Figure 4.6.d**).

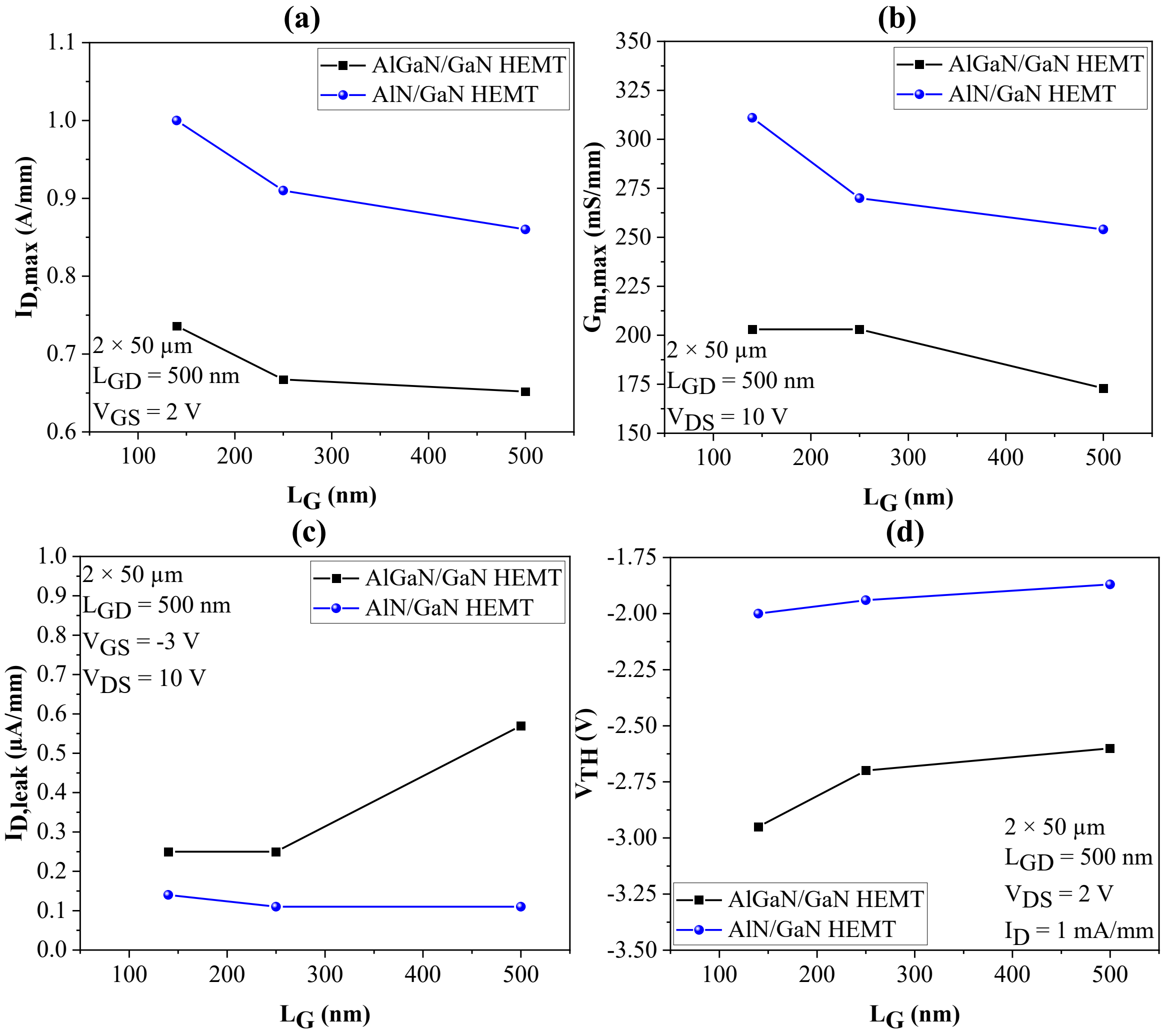


Figure 4.6.: (a) $I_{D,max}$, (b) $I_{D,leak}$, (c) V_{TH}, and (d) $G_{m,max}$ as a function of gate length with L_{GD} = 500 nm of submicron thick 2 × 50 µm AlGaN/GaN and AlN/GaN HEMTs.

Pulsed I_D–V_{DS} characteristics revealing the charge trapping effects when using various quiescent bias points are depicted in **Figure 4.7**. The open channel DC pulsed measurements are shown at V_{GS} = +2 V with various quiescent drain voltages at room temperature. 2 × 50 µm transistors with L_{GD} = 500 nm and L_G = 140 nm show low charge trapping effects despite the thin total growth thickness of both structures. Remarkably, a current collapse as low as 14 % and 12 % are observed under drain lag conditions at 20 V for the AlGaN/GaN HEMT and AlN/GaN HEMT, respectively. It can be noted that these current collapse level results in low impact on the RF device performance [165]. This is attributed to the high material quality, in particular the low impurity levels as seen in SIMS analysis (shown in the next section).

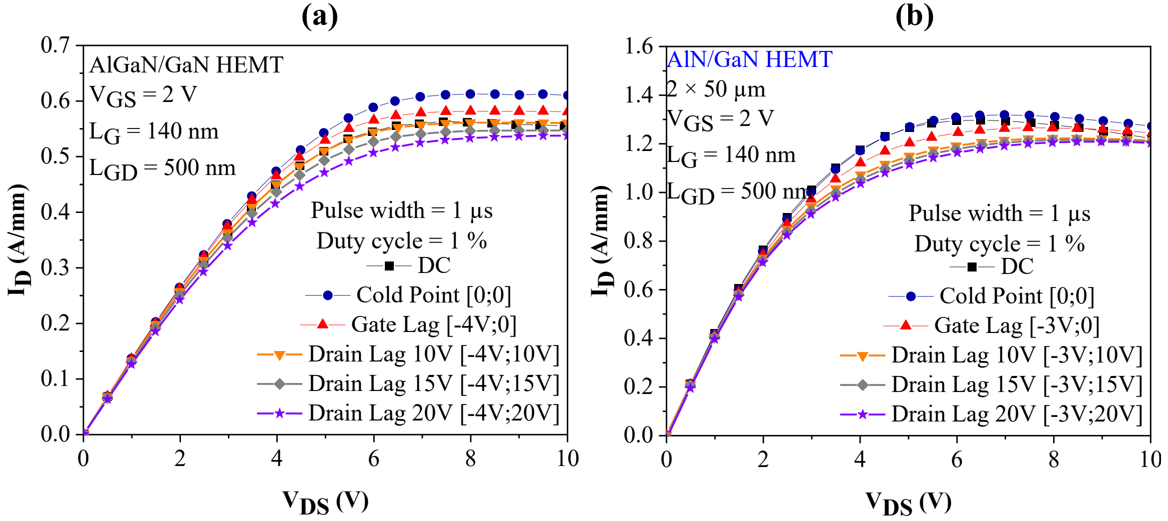


Figure 4.7.: Open channel pulsed I_D-V_{DS} output characteristics of submicron thick 2 × 50 µm (a) AlGaN/GaN HEMT and (b) AlN/GaN HEMT with L_{GD} = 500 nm and L_G = 140 nm.

The S-parameters have been measured from 250 MHz to 67 GHz as shown in **Figure 4.8**. The current gain extrinsic cut-off frequency (F_T) is not only higher in the case of AlN but also more scalable for short L_G (shown in **Figure 4.8.a**) owing to the reduced short channel effects enabled by the ultrathin barrier. The maximum oscillation frequency (F_{MAX}) increases as function of V_{DS} for both structures (**Figure 4.8.b**). F_T/F_{MAX} of 35/153 GHz and 50/175 GHz are achieved at V_{DS} = 20V with L_{GD} = 500 nm and L_G = 140 nm for the AlGaN and AlN barrier, respectively. The F_T/F_{MAX} ratio close to 3 for the AlN/GaN HEMT is attributed to the highly favorable aspect ratio: gate length / gate-to-channel distance.

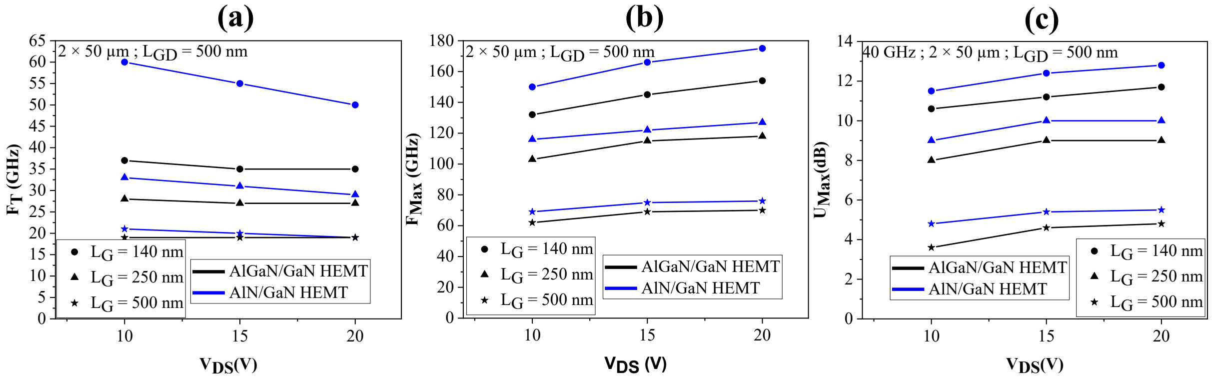


Figure 4.8.: (a) Current gain extrinsic cut-off frequency, (b) maximum oscillation frequency and (c) maximun gain at 40 GHz of a submicron thick 2 × 50 µm AlGaN/GaN HEMT and AlN/GaN HEMT with L_{GD} = 500 nm for various gate lengths.

II.3. Large signal characterization at 10 GHz

Pulsed large signal measurements at 10 GHz for V_{DS} = 10 and 30 V were conducted for both AlGaN/GaN HEMT and AlN/GaN HEMT devices, with L_G = 140 nm and L_{GD} = 500 nm, as illustrated in **Figure 4.9**. In **Figure 4.9.a**, the measurements at V_{DS} = 10 V are presented, showing the output power density, gain, and power-added efficiency as a function of the injected power. For the AlGaN barrier, a saturated P_{OUT} of 0.6 W/mm was obtained, corresponding to a peak PAE of 54%. In contrast, the AlN barrier exhibited a similar PAE of 54% but with a P_{OUT} of 1.1 W/mm, attributed to its superior polarization effects. This represents a P_{OUT} two times higher for the AlN barrier due to enhanced polarization characteristics.

Further load-pull measurements were conducted at V_{DS} = 30 V, revealing a saturated P_{OUT} of 1.3 W/mm with a peak PAE of 34.9% for the AlGaN barrier. Conversely, the AlN barrier demonstrated significantly enhanced performance, yielding a saturated P_{OUT} of 3.8 W/mm and a peak PAE of 46.6%. It can be pointed out that the P_{OUT} for the AlN barrier is three times higher, highlighting its superior capabilities. Additionally, a PAE gap exceeding 10 points between the two structures was observed, further confirming the advantages of the AlN barrier. Overall, the AlN barrier exhibited a superior power and PAE performance owing to its enhanced 2DEG properties and favorable gate-to-channel aspect ratio.

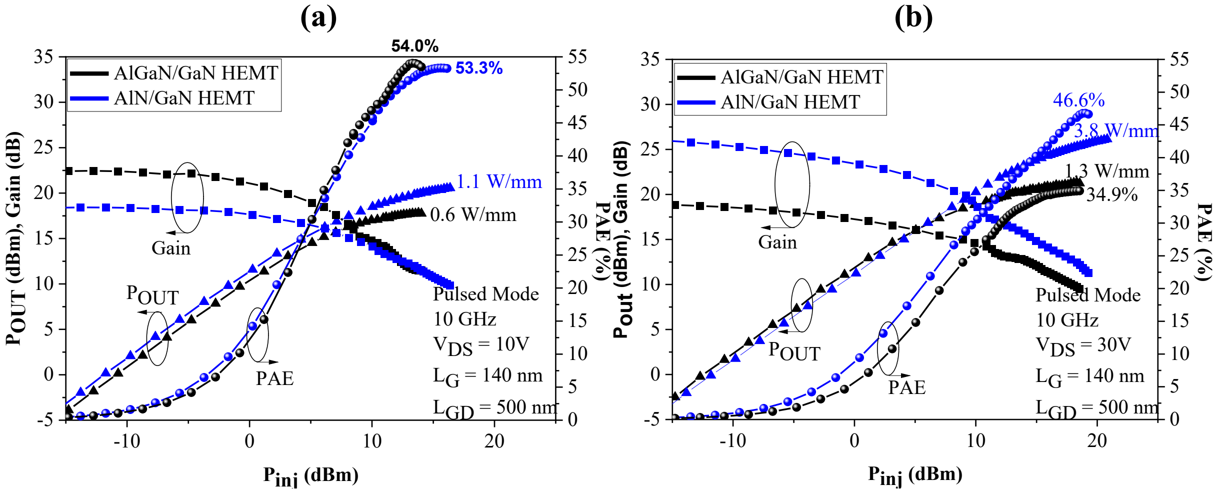


Figure 4.9.: Pulsed large signal performances at 10 GHz at (a) V_{DS} = 10 V and (b) V_{DS}= 30 V of a submicron thick 2 × 50 µm AlGaN/GaN HEMT and AlN/GaN HEMT with L_{GD} = 500 nm and L_G = 140 nm.

Figure 4.10 depicts typical pulsed PAE and P_{OUT} of 2 × 50 µm AlGaN/GaN HEMT and AlN/GaN HEMT with L_{GD} = 500 nm and L_G = 140 nm as a function of V_{DS} at 10 GHz. The drop of the PAE / P_{OUT} between pulsed and CW measurements is mainly attributed to the low thermal dissipation of the Si substrate as seen from the increasing CW/pulsed P_{OUT} gap that is more pronounced under higher output power.

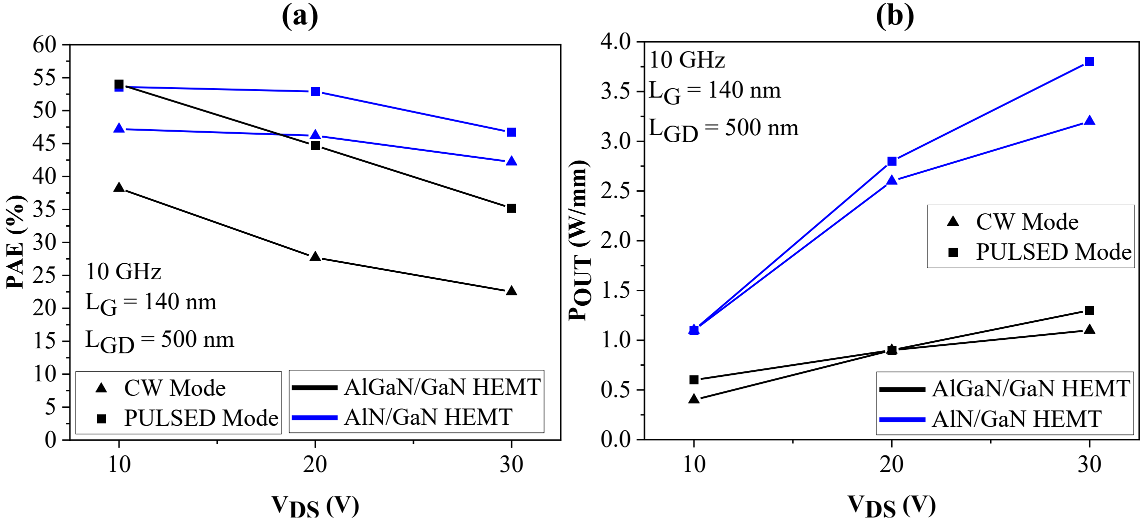


Figure 4.10.: (a) PAE and (b) P_{OUT} at 10 GHz as a function of V_{DS} of a submicron thick 2 × 50 µm AlGaN/GaN HEMT and AlN/GaN HEMT with L_{GD} = 500 nm and L_G = 140 nm.

III. Ultrathin AlN/GaN-on-Si HEMT technology

To our knowledge, the results presented in the previous section for the AlN/GaN-on-Si heterostructures represent the first successful fabrication of such ultrathin HEMTs using MBE for RF applications. Typically, AlN barriers grown via MBE exhibit high off-state leakage current even at low drain bias [19, 66, 166, 167]. Moreover, the only reports on AlN/GaN-on-Si HEMTs have utilized MOCVD growth technique [110, 168]. Most results for AlN/GaN are predominantly obtained through the MOCVD growth technique on SiC substrates [169, 170]. Furthermore, device fabrication of AlN/GaN HEMTs is challenging, particularly as the active region is located very close to the surface, rendering it more sensitive to any process steps.

In an effort to gain deeper insights into these results, various structural characterizations have been conducted on the material. Following process enhancements, further assessments aimed at pushing the technological boundaries of the AlN/GaN-on-Si HEMT, including DC temperature measurement, DCT assessment, large signal characterization at 40 GHz and short-term reliability at 40 GHz have been carried out.

III.1. Structural characterization

The structural quality of the AlN/GaN-on-Si heterostructures is evaluated using Atomic Force Microscopy (AFM), High Resolution Transmission Electron Microscopy (HRTEM) and Secondary-Ion Mass Spectrometry (SIMS).

III.1.a. Atomic force microscope (AFM)

The AFM analysis was performed on AlN/GaN-on-Si HEMTs by EasyGaN as illustrated in **Figure 4.11**. It exhibits a hillock -like morphology, typical of a GaN layer epitaxially grown by NH_3-MBE. The surface roughness measured is about 1 nm for a 5 µm x 5 µm scan. Most importantly the AlN/GaN-on-Si HEMT shows no microcracks due to the plastic relaxation of the AlN barrier (**Figure 4.11**). The emergence of dislocations at the surface is observed by the formation of a small depression which gives a small dark spot on the AFM images but we cannot precisely count the density of dislocations on these AFM images.

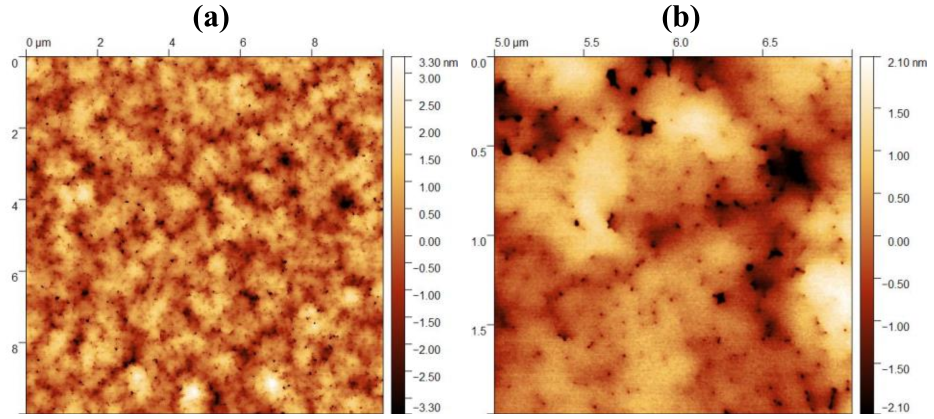


Figure 4.11.: AFM scan of a (a) 10 µm × 10 µm and (b) 5 µm × 5 µm AlN/GaN-on-Si HEMT epitaxial structure in topographic mode.

III.1.b. High Resolution Transmission Electron Microscopy (HRTEM)

In order to better understand such an outstanding electrical behavior High Resolution Transmission Electron Microscopy (HRTEM) structural characterization has been performed on the ultrathin AlN/GaN-on-Si HEMT. The thin lamella preparation for the TEM study was carried out at IEMN using Focused Ion Beam (FIB) method. The samples were then sent to CRHEA laboratory in order to perform TEM analysis.

The AlN/GaN-on-Si structure was investigated by Scanning Transmission Electron Microscopy (STEM). **Figure 4.12** shows high-angular annular dark field (HAADF) and Energy Dispersive X-ray (EDX) mapping images of the AlN/GaN structure. With this method, different epitaxial layers highlighted by various contrasts from the HAADF image are identified. The elemental composition of the material structure consists in Ga, Al, and Si atoms, which are homogeneously distributed as shown in the EDX mapping images.

Using MBE for AlN growth entails operating at lower temperatures compared to MOCVD, the predominant technique for GaN growth. This lower temperature process facilitates the formation of a sharp and crystalline AlN/Si interface, as depicted in **Figure 4.12**. The AlN nucleation layer culminates in a smooth surface devoid of pits and holes [171]. The exceptional quality of the AlN nucleation layer enables the growth of unprecedented structures, particularly those with a total stack thickness below 650 nm, while effectively filtering out dislocations, as evidenced by the HAADF image of the AlN/GaN structure. Indeed, it can be noticed that the dislocations are reduced inside the three step-graded $Al_xGa_{1-x}N$ buffer layers until the GaN channel (**Figure 4.12**) and have no obvious effects on the electrical properties of the heterostructure [153].

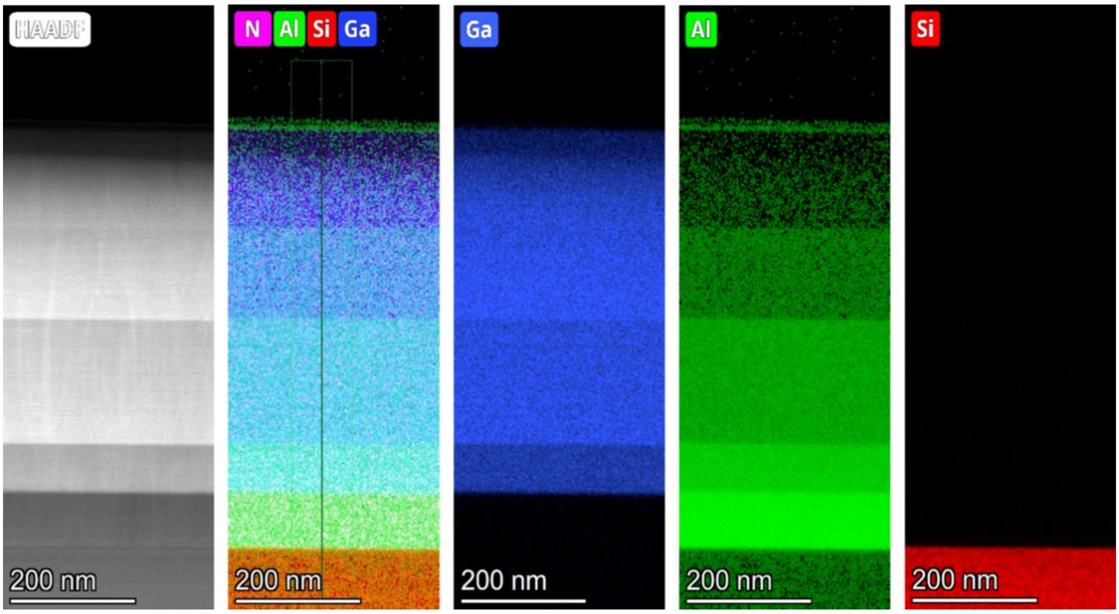


Figure 4.12.: Electron Dispersive Spectroscopy mapping of the Ga, Al and Si elements and the corresponding STEM-HAADF image of a selected area within the cross section prepared along the ultrathin AlN/GaN-on-Si HEMT.

The EDX images reveal an unexpected distribution of Al for the AlN barrier. Indeed, the structure exhibits a blurred interface, indicating an AlGaN transition region between the GaN channel and the AlN barrier layers. The corresponding EDX profiles are shown in **Figure 4.13**, with the y-axis representing the total atomic percentage of aluminum and gallium compounds. Three distinct regions can be distinguished from this plot: the region of the GaN channel with 100% gallium atoms, followed by the transition region with an average of 50% gallium, and finally, a nearly pure AlN barrier with approximately 90% aluminum and a low gallium content of approximately 5%. Consequently, the total thickness of the barrier layer in this case is close to 10 nm rather than the expected 7 nm.

From the literature, sharper interfaces can be found and were obtained by plasma-assisted MBE at very low growth temperatures [19, 66, 172]. Therefore, it can be expected that the use of lower temperature growth would generate sharper interface between the GaN channel and the AlN barrier. However, it should be noted that lower growth temperatures for the AlN barrier often result in high leakage current [66].

Moreover, the growth conditions of this AlN barrier exhibit a similar composition to that reported by Harrouche et al., who achieved a record performance at 40 GHz for a 3 nm AlN/GaN-on-SiC structure grown by MOCVD [173]. The transition layer is still considered sharp enough at the interface of the AlN/GaN structure, thus explaining the high performance of devices.

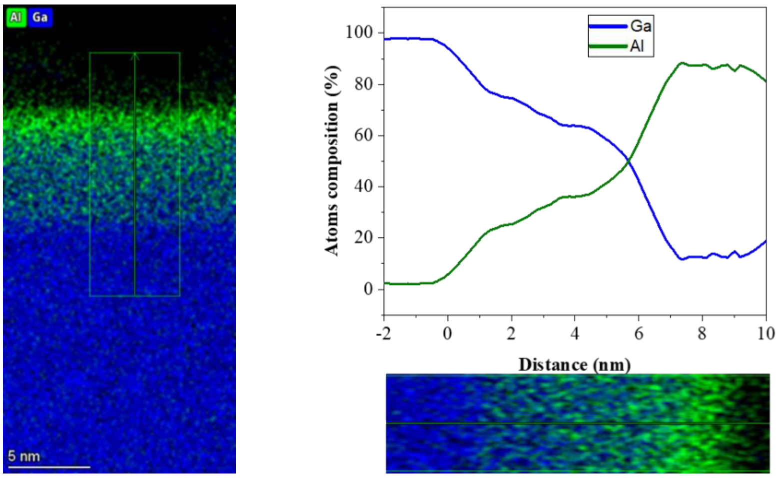


Figure 4.13.: Al and Ga-distribution within the AlN barrier / GaN channel layers.

III.1.c. Secondary-ion mass spectrometry (SIMS)

A key challenge in fabricating high-performance devices remains the uncontrollable background impurity levels in GaN crystals. Compensating GaN with various elements is a legitimate method of obtaining insulating material. However, the additional impurities can alter the properties of HEMTs and reduce the superior performance expected from intrinsic (ultra-pure) materials. Residual conductivity is often observed in GaN epitaxial structures [174, 175]. Oxygen has been identified as a primary source of unintentional background impurities leading to n-type conductivity [176, 177].

From an electrical quality perspective, Secondary-ion mass spectrometry (SIMS) analyses reveal the presence of impurities incorporated during growth, such as oxygen and carbon. **Figure 4.14** shows the results measured by SIMS performed along the AlN/GaN structure. The carbon and oxygen concentration are below 1 × 10^{17} atoms/cm^3 in both the step-graded $Al_xGa_{1-x}N$ buffer layers and the GaN channel. The relatively low unintentional carbon doping is considered satisfactory to avoid buffer trapping effects [165].

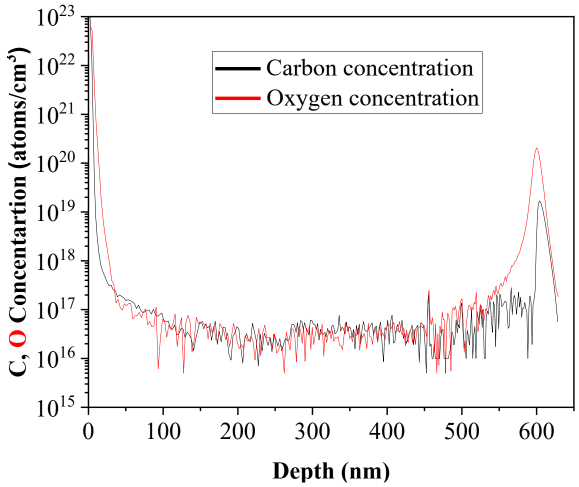


Figure 4.14.: Unintentional carbon and oxygen doping measure by secondary-ion mass spectrometry in the epi-stack AlN/GaN-on-Si.

III.2. Device fabrication

The cross section and FIB view of the HEMT structures with 140 nm T-gates are shown in **Figure 4.15**. It can be noticed that the total stack thickness is as low as 650 nm (**Figure 4.15**). The source and drain ohmic contacts were first fabricated. The contacts were directly deposited on top of the AlN barrier. A Ti/Al/Ni/Au metal stack was annealed at 850°C yielding contact resistances of 0.4 Ω.mm. Nitrogen implantation was used to isolate the devices. Then, Ni/Au T-gates of 140 nm, 250 nm and 500 nm gate lengths were defined by e-beam lithography and directly deposited on top of the thin in-situ SiN cap. Finally, 200 nm PECVD Si_3N_4 passivation layer was deposited prior to Ti/Au pads. Hall effect measurements at room temperature showed a charge density of 1.8×10^{13} cm^{-2} with an electron mobility of 745 cm²/V.s. The electron mobility can most probably be improved by further tuning the growth parameters and the hybrid barrier configuration [178].

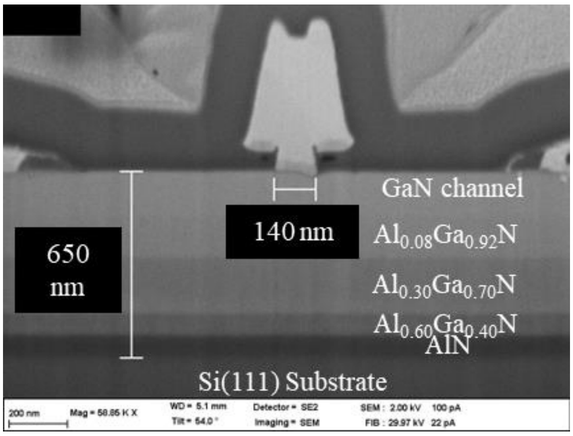


Figure 4.15.: FIB image of the sub-micron thick AlN/GaN HEMTs grown on Si(111) substrate by MBE and using a very thin step-graded AlxGa1-xN buffer layers.

III.3. Advanced electrical characterization

In the previous section it has been demonstrated that the AlN/GaN HEMT structure enables to combine an excellent electron confinement as reflected by the low drain-induced barrier lowering, a low leakage current below 10 µA/mm and low trapping effects up to a drain bias V_{DS} = 30 V while using sub-150 nm gate lengths. Consequently, further characterization, such as preliminary temperature-dependent DC measurements or drain current transient measurements have been performed.

III.3.a. Temperature dependent DC characteristics

DC measurement at a chuck temperature ranging from room temperature up to 150 °C have been performed on the AlN/GaN HEMT. Two sets of electrical tests have been used. The first measurement consists of studying the DIBL as a function of temperature from room temperature to 150°C in class AB (I_D = 1 mA/mm) (**Figure 4.16.a**). The DIBL remains lower than 60 mV/V and stable over a wide range of temperature.

For the second measurement, the transistor is biased in off-state (V_{GS} = -4 V) and the drain and gate currents are monitored for V_{DS} = 2 V up to 20V while increasing the temperature from room temperature to 150 °C (**Figure 4.16.b**). Both drain and gate off-state leakage currents remain lower than 10µA/mm and stable over a wide range of temperature. No permanent degradation subsequent to temperature measurements is observed indicating a proper isolation of the channel from the Si substrate under high electric field by the sub-micron thick buffer and thus an excellent electron confinement up to 150°C.

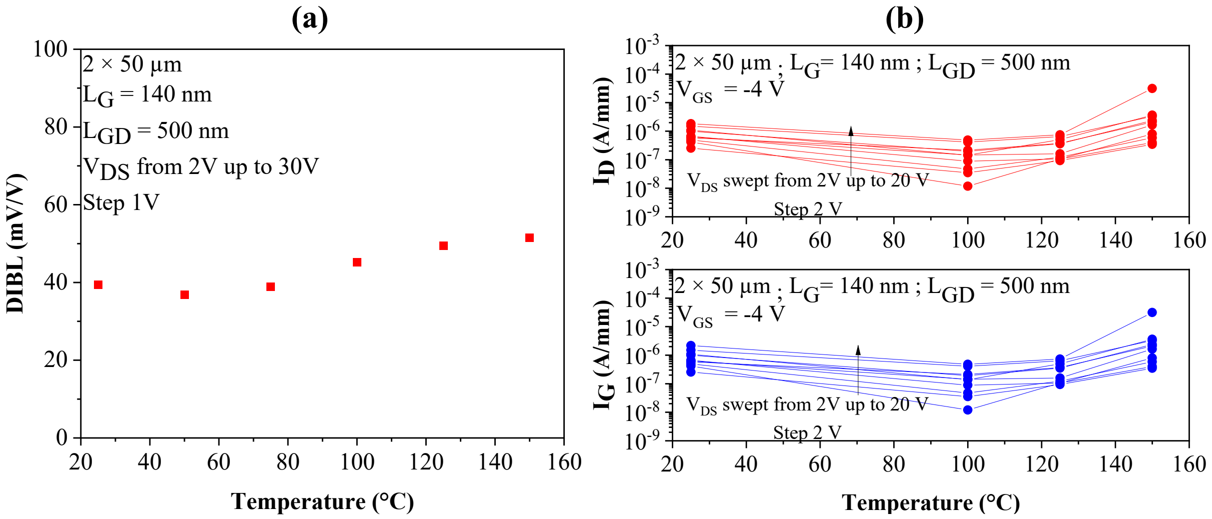


Figure 4.16.: (a) DIBL as a function of temperature and (b) I_D and I_G as a function of temperature for various V_{DS} at V_{GS} = -4 V of a submicron thick 2 × 50 µm AlGaN/GaN HEMT and AlN/GaN HEMT with L_{GD} = 500 nm and L_G = 140 nm.

III.3.b. Drain current transient (DCT) characteristics

Figure 4.17 illustrates the drain current transient (DCT) measurements conducted with trap filling times ranging from 100 µs to 100 s at $V_{DS,Fill}$ = 20 V and $V_{GS,Fill}$ = -4 V. It can be observed that less than 6% current collapse occurs for a filling time of 100 µs. Furthermore, it is evident that for filling times below 1 s, a consistently low level of current collapse (less than 5%) is observed, in agreement with standard DC pulsed assessments. Even with a filling time as long as 100 s, the current collapse remains approximately 12%, confirming minimal trapping effects despite the thin overall buffer thickness grown on a silicon substrate. The reduced trapping can be attributed to the low impurity concentration within the epitaxial stack such as carbon and oxygen, as observed from SIMS measurements, as well as high processing quality, including proper surface passivation.

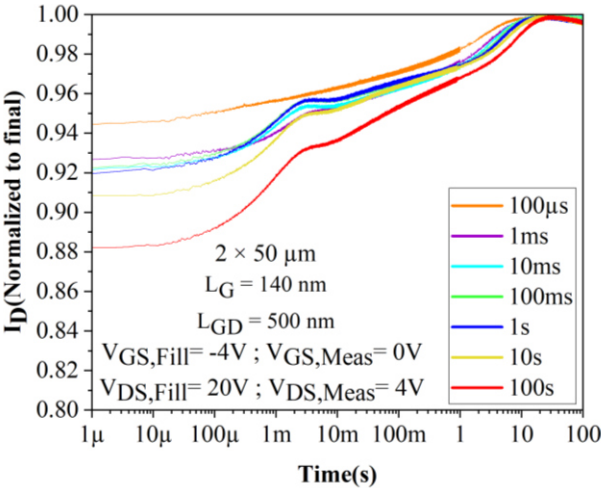


Figure 4.17.: Drain current transient characteristics for various filling time of a submicron thick 2 × 50 µm AlN/GaN HEMT with L_{GD} = 500 nm and L_G = 140 nm.

III.4. Large signal characterization at 40 GHz

Large signal characterizations have been carried out at 40 GHz. **Figures 4.18.a and 4.18.b** show typical CW and pulsed power performances at 40 GHz in deep class AB of 2 × 50 µm transistors with L_{GD} = 500 nm and L_G = 140 nm at V_{DS} = 10 V and 30 V, respectively. A saturated P_{OUT} of 1.1 W/mm associated to a PAE of 45.6 % and 35.5 % at V_{DS} = 10 V is measured in pulsed and CW mode, respectively. At V_{DS} = 30 V, a P_{OUT} of 3.1 W/mm and 2.3 W/mm with a PAE of 35.1 % and 25.2 % are observed in pulsed and CW, respectively. Moreover, it can be pointed out that following several tenths of CW Load-Pull sweeps under high gain compression (up to 10 dB), no major degradation of the devices up to V_{DS} = 30 V was observed (see **Figures 4.18.c**). This indicates an excellent robustness of this heterostructure handling extreme electric field and thus enabling high voltage operation without degradation while using a sub-150 nm gate length. The promising device reliability results from the combination of an excellent electron confinement and low trapping effects. 2

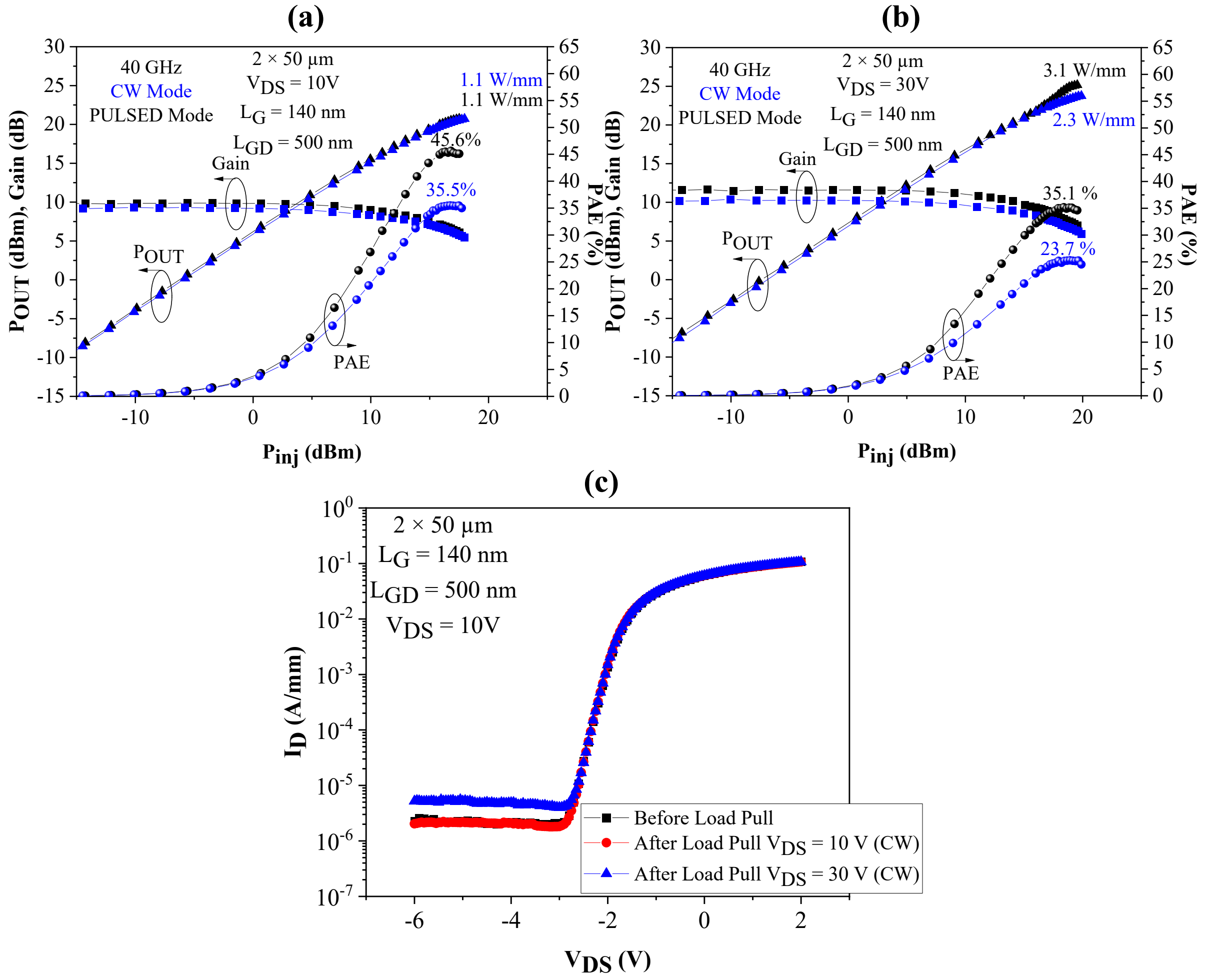


Figure 4.18.: CW and pulsed large signal performances at 40 GHz at (a) V_{DS} = 10 V and (b) V_{DS}= 30 V. (c) Transfer characteristics after more than 40 CW Load Pull sweeps in deep class AB under high compression up to V_{DS} = 30 V of a submicron thick 2 × 50 µm AlN/GaN HEMT with L_{GD} = 500 nm and L_G = 140 nm.

Figure 4.19 depicts typical pulsed PAE and P_{OUT} of 2×50 µm transistors with L_{GD} = 500 nm and L_G = 140 nm as a function of V_{DS} at 40 GHz. The drop of the PAE / P_{OUT} between pulsed and CW measurements is mainly attributed to the low thermal dissipation of the Si substrate as seen from the increasing CW/pulsed P_{OUT} gap that is more pronounced under higher output power. Therefore, further optimization of the structure to enhance the electron mobility and thus the power gain, combined with substrate thinning and related heat sink will certainly boost GaN-on-Si mm-wave device performances.

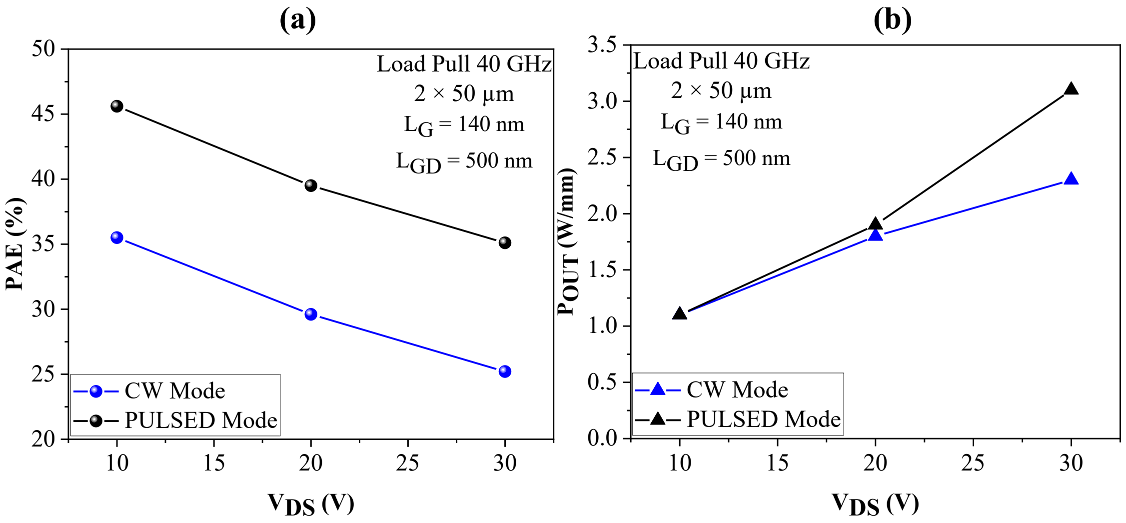


Figure 4.19.: CW and Pulsed (a) PAE and (b) P_{OUT} as a function of V_{DS} at 40 GHz with L_{GD} = 500 nm and L_G = 140 nm for 2 × 50 µm ultrathin AlN/GaN HEMTs.

Figure 4.20 shows a benchmark representing the PAE as a function of the output power density at 40 GHz in Ka-band. Both CW and pulsed RF performances of our AlN/GaN-on-Si devices at 40 GHz are favorably comparable to the state-of-the art with a combination PAE/P_{OUT} (35% / 3.1 W/mm at V_{DS} = 30 V) in pulsed mode. It is noteworthy that these results were achieved without employing specific thermal management techniques, such as substrate thinning or the subsequent use of a heat sink. The adoption of such techniques is expected to significantly enhance the RF performance beyond the current achievements and will be discussed in **Chapter 5**.

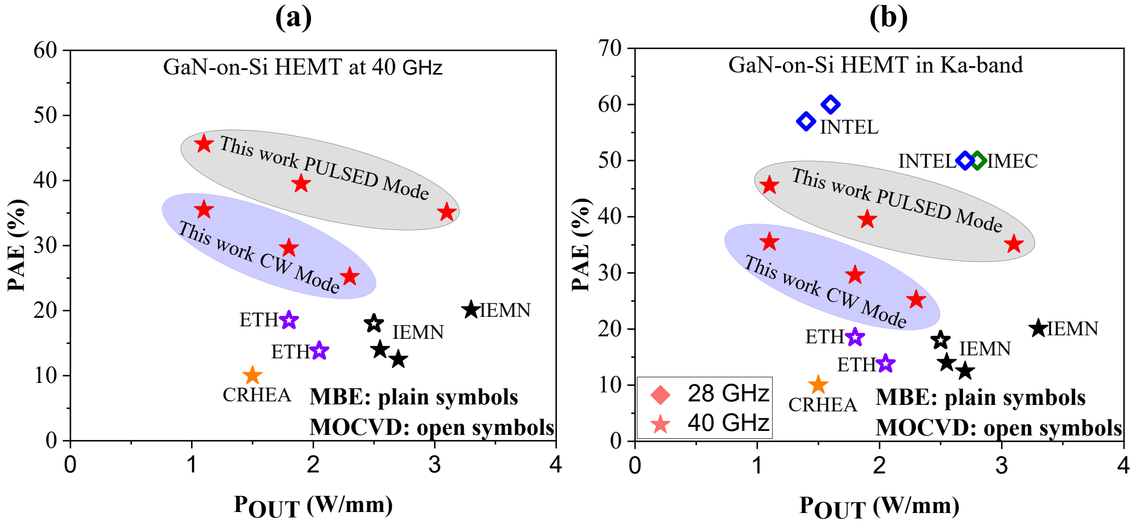


Figure 4.20.: Benchmark of GaN-on-Si HEMTs from the literature (a) at 40 GHz and (b) in ka-band [109–111, 114, 116, 118–120].

III.5. Ultrathin AlN/GaN-on-Si HEMT short term reliability at 40 GHz

In the past decade, significant strides have been made in GaN-based RF power devices, paving the way for new applications. High-frequency applications demand compact systems, where achieving high PAE coupled with a high P_{OUT} in the mm-wave spectrum stands as a paramount objective for GaN technology, alongside device linearity.

Reliability is a pivotal factor before GaN-based devices can enter the market, particularly for systems where maintenance during operation is unfeasible, such as satellites and military equipment. The reliability of these devices hinges on meticulous device design and fabrication processes. While several groups have demonstrated the unparalleled combination of high power and wide bandwidth achievable with GaN devices, stretching up to 94 GHz, short GaN devices with gate lengths below 150 nm face reliability hurdles due to electric field peaks and high junction temperatures under large drain bias. Consequently, few reports on mm-wave GaN device reliability are available in the literature, both for short and long-term assessments [107, 179–182].

Conventional packaging allows a maximum operating junction temperature of 150°C-230°C and consequently specific packages are needed to handle larger temperatures. In fact, the device lifetime is conventionally expressed in terms of mean time to failure (MTTF) at a defined junction temperature. This is typically obtained by means of temperature accelerated tests, usually performed in the range of 325-400°C. Considering a typical activation energy of 2 eV [179], it is easy to understand that meeting the reliability requirements for a lifetime of at least 20 years at a junction temperature of 300°C can be problematic. In contrast, reliability constraints can be met if a lower operating temperature is considered (e.g. [179]). Therefore, packaging and reliability constraints are the main reasons why the operating junction temperature of commercially available technology is around 150°C for GaN-on SiC and around 200°C for GaN-on-Si [179].

Short-term reliability assessments provide insights into device degradation or failure, offering valuable feedback for material quality adjustments before embarking on long-term reliability tests for final device applications. These assessments typically involve RF robustness evaluations at elevated temperatures over a few hours by increasing the base-plate temperature. However, short-term reliability assessments do not provide insights into degradation kinetics, activation energy, or mean time to failure, requiring long-term reliability testing to validate device reliability.

In this thesis, RF short-term robustness evaluations were conducted on the ultrathin AlN/GaN HEMT structure, through the development of a new test bench within the framework of another PhD thesis from our research group. **Figure 4.21** illustrates the High Temperature

Operating Lifetime (HTOL) measurements conducted over an 8-hour period at high junction temperature, subjected to RF stress in load pull conditions at 40 GHz. The measurements were performed on 2 × 50 µm transistors with L_{GD} = 1.5 µm and L_G = 140 nm. The chuck was heated to 150°C, and the 140 nm gate length device was operated in class AB mode with I_{DS} = 230 mA/mm and V_{DS} = 20V. The junction temperature is estimated to be above 250°C. Throughout the 8-hour duration, the measurements were conducted under large signal conditions and at peak PAE. At a chuck temperature of 150 °C, a reduction in peak PAE of 16.4% was observed, along with a saturated P_{OUT} of 1.4 W/mm. This decrease in PAE can be attributed to the thermal impact on electron mobility, which is the case for any compound semiconductors. It directly affects the gain and subsequently the PAE. However, the output power density remained stable thanks to adjustments in gate voltage to maintain the drain current at 230 mA/mm under the 150 °C chuck temperature.

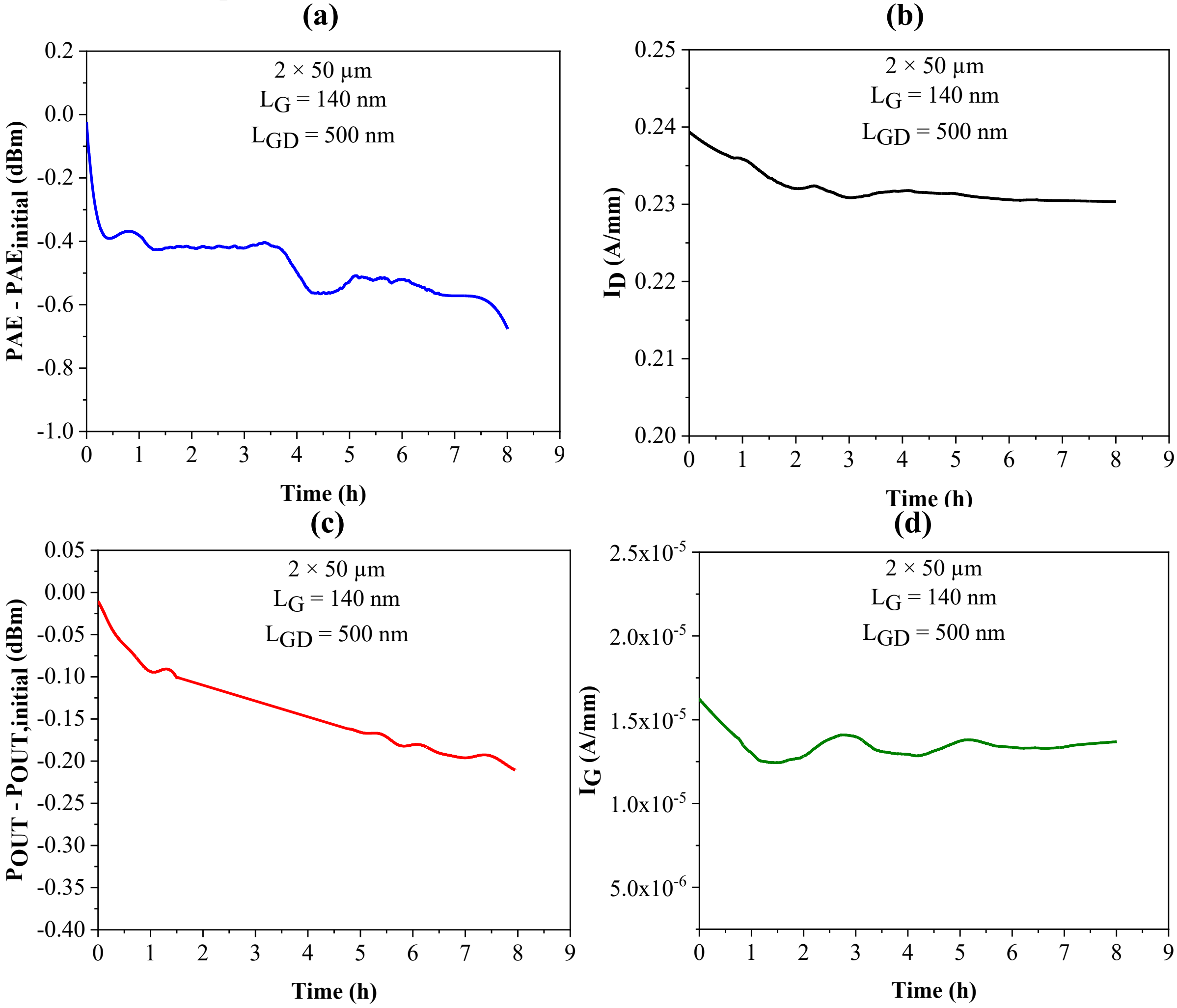


Figure 4.21.: Changes in (a) output power P_{OUT}, (b) PAE, (c) drain current and (d) gate leakage current during the 8 hours RF stress at V_{DS} = 20 V and chuck temperature 150°C of 2 × 50 µm ultrathin AlN/GaN-on-Si HEMT with L_G = 100 nm and L_{GD} = 500 nm.

Under such severe stress tests, an extremely low drop of output power and PAE are observed with no failure. Remarkably, the output power drop over time is as low as 0.2 dBm. The PAE drop over time, drain current, as well as gate leakage current variations are low, indicating that the very thin structure combined with an AlN barrier is very stable. The results demonstrate promising RF reliability and potentially stable ultrathin AlN/GaN-on-Si HEMTs under high-power operation.

Figure 4.22 shows the output, transfer and open channel pulsed I_D-V_{DS} output characteristics performed, on the 2 × 50 µm transistors with L_G = 140 nm and L_{GD} =1.5 µm, before and after 8 hours RF stress. No significant degradation of the on and off-state current is observed (**Figure 4.22.a and 4.22.b**) while the junction temperature (although not assessed yet) is expected to be well above 250°C (as compared to in-house GaN/SiC reference). Moreover, despite the low total epilayer thickness, no increase of the current collapse is observed after the RF stress (**Figure 4.22.c**). This reflects the high quality of both growth and device processing.

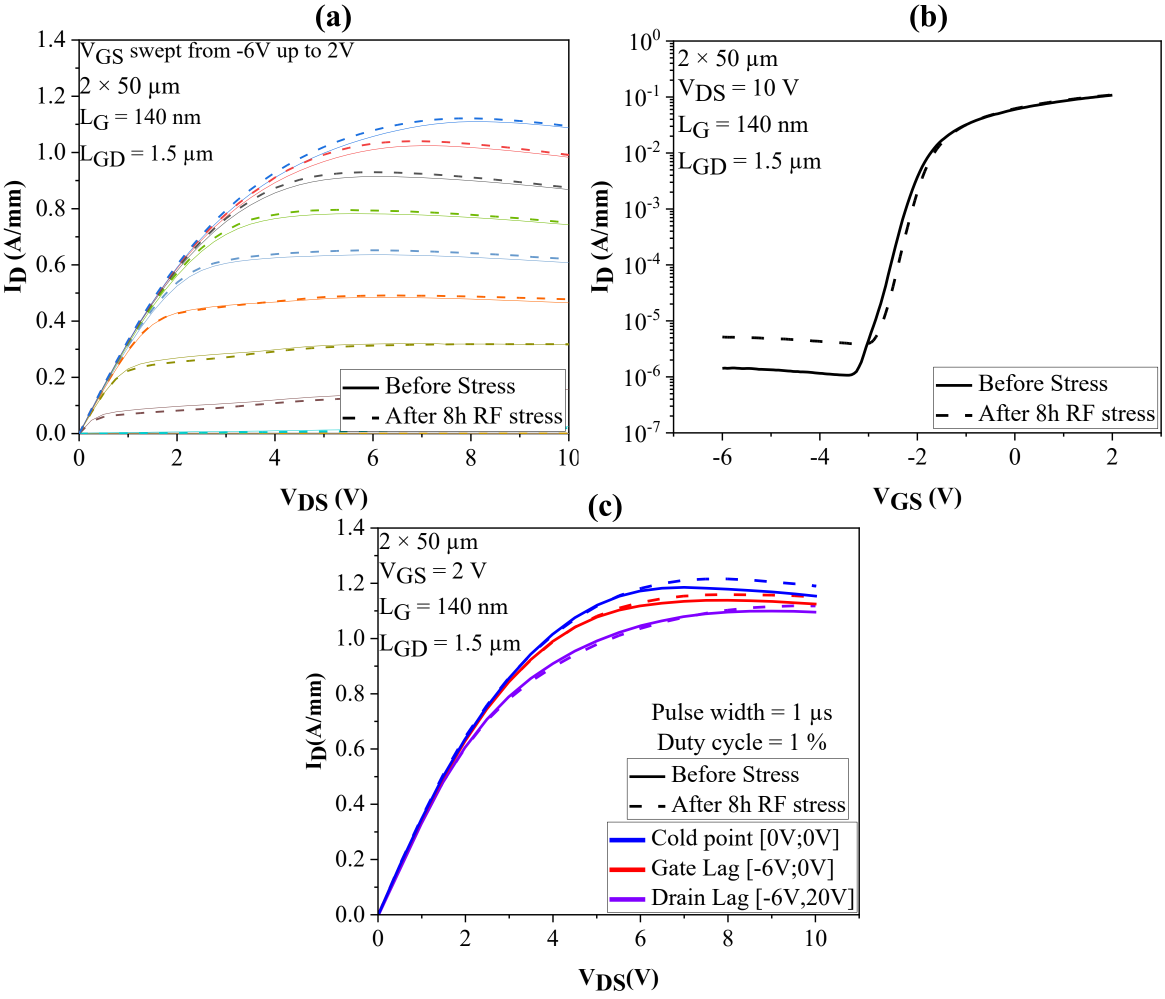


Figure 4.22.: (a) Output, (b) transfer and (c) open channel pulsed I_D-V_{DS} output characteristics before and after 8 hours RF stress.

IV. Conclusion

In this chapter, a comparison was made between sub-micron thick AlGaN/GaN and AlN/GaN HEMTs grown on Si (111) substrates for high-frequency applications. The thin heterostructures grown via NH_3-MBE exhibit promising and unique features, including low off-state leakage current under high electric fields up to 30 V for gate lengths of sub-150 nm, combined with high carrier density and low trapping effects. This achievement is attributed to the optimization of the sub-micron thick step-graded $Al_xGa_{1-x}N$ buffer layer, enabling high electron confinement under high electric field and proper surface passivation. Small-signal characteristics reveal the benefits of the thin AlN barrier in reducing short-channel effects and improving the frequency performance at 10 GHz.

Structural characterization demonstrates that the results achieved are due to a highly controlled growth technique offering reduced surface roughness. HRTEM structural characterization performed in collaboration with CRHEA Laboratory, revealed a transition layer at the AlN/GaN interface, while SIMS measurements confirmed the low concentration of impurities such as C and O inside the epi-stack.

Further characterization of the AlN/GaN-on-Si HEMT shows that DIBL and off-state leakage current remain low and stable over a wide range of temperatures from 25 to 150°C. No permanent degradation subsequent to temperature measurements is observed, indicating proper isolation of the channel from the Si substrate under high electric fields by the sub-micron thick buffer and thus excellent electron confinement up to 150°C. Moreover, DCT measurements confirm low trapping effects despite the thin total buffer thickness grown on the silicon substrate.

Consequently, unprecedented class AB bias operation (up to V_{DS} = 30 V) is achieved for 140 nm gate length ultrathin GaN-on-Si HEMTs. As a result, the proposed AlN/GaN-on-Si HEMT structure delivers high output power density together with state-of-the-art PAE of 45.6% / 35.1% at V_{DS} = 10 V / 30 V at 40 GHz, respectively. This achievement is attributed to the optimization of both materials, epitaxial design, and processing quality, enabling high electron confinement and reduced short-channel effects under high electric fields. These results demonstrate the potential of MBE to grow ultrathin, cost-effective AlN/GaN-on-Si HEMTs for millimeter-wave applications.

Furthermore, HTOL at high junction temperatures during 8 hours of RF stress was conducted at a chuck temperature of 150°C, V_{DS} = 20 V, and I_D = 230 mA/mm. Under such severe stress testing, an extremely low drop in output power and PAE was observed with no failures. Despite the proximity of the dislocation density at the substrate interface, no increase in current collapse was observed after the RF stress. These results demonstrate promising RF reliability and potentially stable ultrathin AlN/GaN-on-Si HEMTs under high-power operation.

However, one of the main drawbacks limiting the optimization of this structure is the self-heating. A significant decrease in RF performance at increased chuck temperature and high V_{DS} is observed with a larger gap between load-pull measurements at 40 GHz in pulsed and CW mode. Therefore, the main focus at the end of this PhD study was to improve the thermal management of the Si substrate by using substrate thinning and heat sinks to enhance the RF power performance. Preliminary results of this study are presented in **Chapter 5**.

Chapter 5: Thermal management in ultrathin AlN/GaN-on-Si HEMTs

I. Introduction

During the PhD, significant strides were made in optimizing the structure and processes, resulting in the development of a submicron thick AlN/GaN-on-Si HEMT with cutting-edge performance. However, a critical issue arises from the thermal impact of the Si substrate, limiting the device performance. It is well known that implementing thermal management on the backside could further enhance the performance. Indeed, GaN-based devices suffer from self-heating effects that reduce the drain current density and transconductance, thereby degrading the overall device performance. Literature indicates that this self-heating phenomenon and the subsequent rise in channel temperatures stem from the transfer of energy from electrons to the lattice [183–185]. As a result, electron mobility and saturation velocity decrease due to phonon scattering [186, 187]. Several approaches have been explored to enhance heat dissipation, including the use of highly thermally conductive materials such as SiC and diamond. However, the presence of metallic impurities in these materials leads to reduced thermal conductivity at higher temperatures, exacerbating the issue of phonon scattering [188]. Moreover, these substrates are currently not cost-effective or scalable. Alternative methods such as employing composite substrates and flip chip bonding techniques with epoxy under-fill have been attempted to reduce the thermal impedance across the entire wafers [189, 190]. Nonetheless, hot spots persist in the channel region. Prior research has explored reducing self-heating via substrate transfer [191, 192] and employing diamond nanostructures on device surfaces, albeit with moderate improvements [193, 194].

Although removing the Si substrate locally has been a common method to enhance heat dissipation, self-heating effects still persist [195, 196]. Additionally, efforts to deposit AlN on the backside of trench-etched AlGaN layers followed by Cu deposition have shown inferior thermal performance compared to Si substrate-based devices without trenches [197] due to the rather poor thermal conductivity of low temperature AlN material. Another approach by co-designing microfluidics and electronics within the same semiconductor substrate permitting to produce a monolithically integrated manifold microchannel cooling structure with good efficiency was also recently demonstrated [198]. Furthermore, filling trench structures with high thermally conductive metals like Cu has been proposed to enhance heat dissipation and device performance [199, 200]. A simulation study suggested an approach to improve heat dissipation and reduce junction temperature using Cu-filled via-holes under the active area of the device on a Si substrate [201]. Another simulation explored performance optimization through Cu-filled trench structures [202, 203]. Recent research has highlighted improvements in drain current saturation and transconductance in GaN/Si HEMTs by employing Cu-filled trenches or nanocrystalline diamond capping layers [204–208]. However, challenges remain such as potential cracking due to stress gradients resulting from lattice and thermal mismatch when transferring thick GaN layers grown on silicon [209, 210]. Ray-Hua Horng et al. have demonstrated that maintaining around 50 µm of Si substrate after thinning yields significant improvement when utilizing electroplated Cu [211]. This chapter presents preliminary results following the thinning of the Si substrate and the utilization of Cu as a heat sink.

II. Thermal management through backside processing

The objective of this study was to assess the enhancement of RF performance following thermal management of the Si substrate in the ultrathin AlN/GaN-on-Si HEMT. To achieve this, we chose to directly thin the entire substrate and employ metal deposition with high thermal conductivity.

II.1. Technological backside processing

Following the fabrication of front side devices, a backside process is initiated. The thermal management of the structures involves the following steps (**Figure 5.1**):

(a) Surface protection: Front side devices are protected to prevent degradation of electrical characteristics during backside processing. An optical resist layer is deposited onto the front side of the structure.

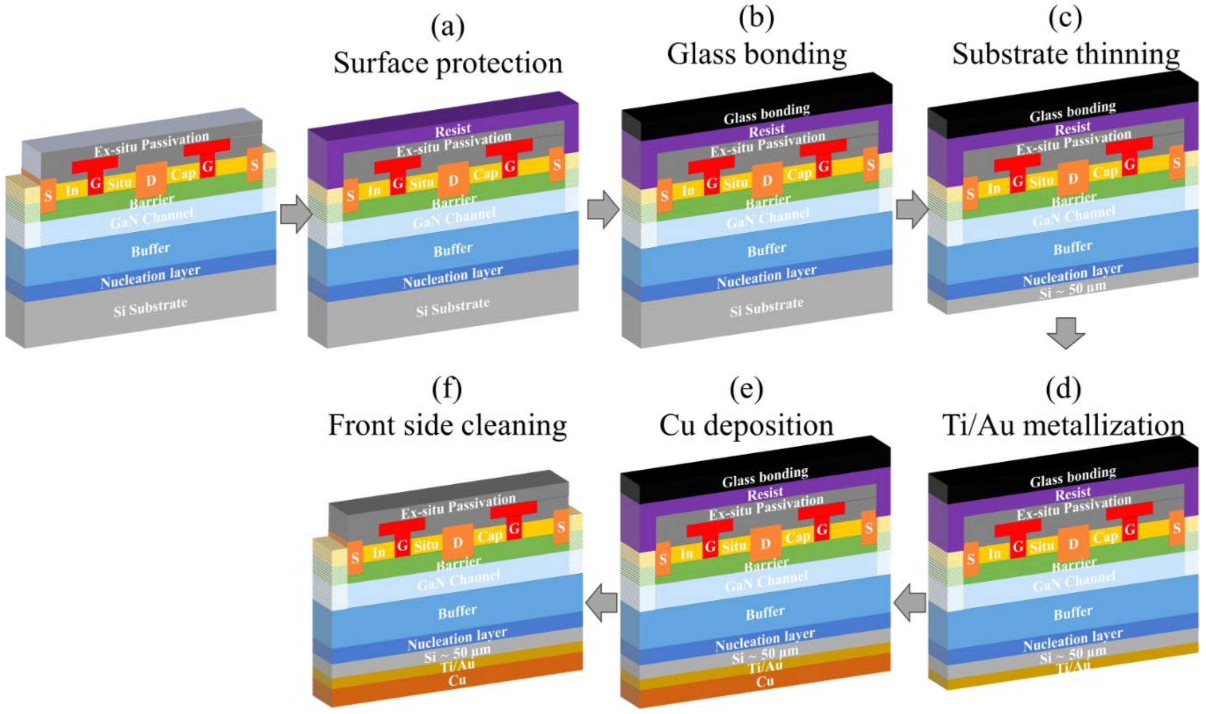
(b) Glass bonding: The sample is bonded to a glass carrier with wax. The advantage of the resist is that it allows for the complete removal of any wax residue after thinning.

(c) Substrate thinning: Thinning of the Si substrate is executed using a G&N MPS2 R300 D CS grinder, with a continuous water flow to cool and cleanse the treated surface, facilitating swift and controlled substrate removal.

(d) Ti/Au metallization: A seed layer of Ti/Au (20 / 300 nm) is deposited by evaporation. The Ti serves as an adhesion layer, while the Au is chosen for its excellent thermal and electrical conductivity while not prone to oxidation.

(e) **Cu deposition:** An electrochemical deposition of several tens of micrometers of Cu is employed as a heat sink, thus improving thermal dissipation.

(f) **Front side cleaning:** The sample is detached from the glass, and the removal of grease and resist is carried out chemically using a solution referred to as "orange juice". Finally, the samples were cleaned, rinsed and dried using a standard process to remove chemical residues.



(a) Surface protection

(b) Glass bonding

(c) Substrate thinning

(f) Front side cleaning

(e) Cu deposition

(d) Ti/Au metallization

Figure 5.1.: Schematics representation of the backside process.

II.2. Constraints and challenges in thinning the Si substrate

Initially, it was necessary to determine the extent to which the Si substrate would be thinned. According to the literature, thinning the Si substrate to at least 50 µm is required to observe a thermal improvement. During the optimization of the technological backside process, it was observed that the fragility of the samples was directly dependent on the remaining thickness of the Si substrate and the total thickness of the epitaxy. Indeed, the use of submicron thin epitaxy represents a risk of increasing mechanical stress on the sample. Therefore, attempts to thin the Si substrate below 50 µm were carried out to test the mechanical limitations of this process. **Figure 5.2** depicts ultrathin AlN/GaN heterostructures on Si (111) with optical processing carried out on the front side. The Si substrates with an initial thickness of 500 µm were thinned down to 80 µm, 50 µm, and 25 µm. Following the thinning step, no visible degradation of the samples was observed.

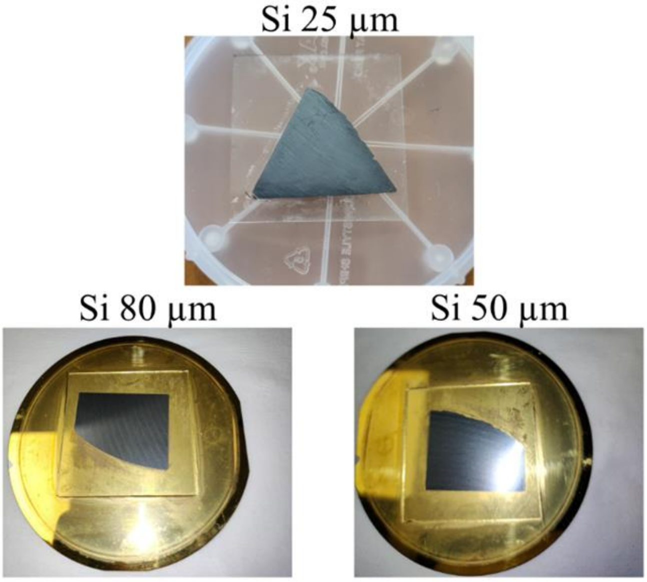


Figure 5.2.: Thinning evolution of Si substrate from backside perspective

Figure 5.3 illustrates the backside process on the sample with a Si substrate thinned down to 25 µm. Ti/Au and 100 µm Cu were deposited by evaporation and electrochemically, respectively. After removing the glass and resist, degradation of the sample was observed. Indeed, the sample exhibits a curvature, and cracks are visible after the backside process. As observed under the optical microscope, the structure eventually cracked during the process due to excessive mechanical stress exerted on the backside. As shown in the microscope images in **Figure 5.3**, these cracks irreversibly degraded the devices on the front side. Thinning to 25 µm is therefore not feasible and limiting the thinning to 50 µm was subsequently preferred in our case.

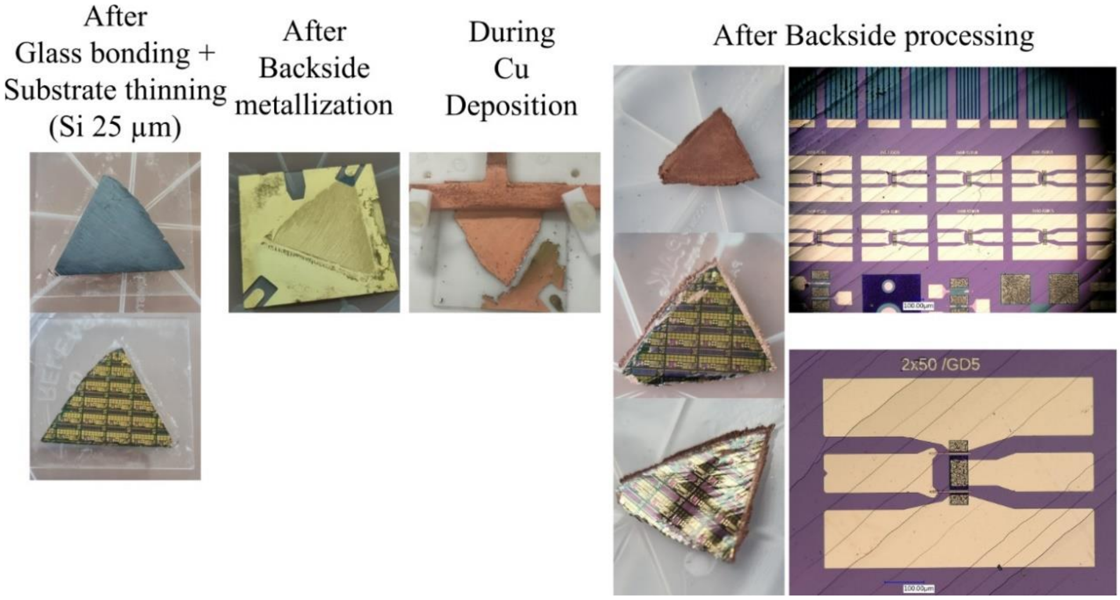


Figure 5.3.: Evolution of the backside process with 25 µm of Si substrate and 100 µm of deposited Cu resulting in cracking within the structure and extending into the device on the front side.

III. Thermal performance improvement of the ultrathin AlN/GaN-on-Si HEMT

In **Chapter 4**, the development of a submicron thick AlN/GaN-on-Si heterostructure was detailed. This structure was grown by NH_3-MBE on a Si (111) substrate, with a buffer thickness below 650 nm including Al-rich step-graded layers. The combination of low electron trapping effects, extreme robustness under high electric field, and high mm-wave power gain was facilitated by this advancement. Consequently, excellent class AB bias operation (up to V_{DS} = 30 V) for 140 nm gate lengths GaN-on-Si HEMTs was achieved.

However, it was emphasized that the performance of this HEMT was primarily limited by poor thermal dissipation, mainly attributed to the use of a Si substrate. Consequently, this same structure was chosen to undergo the first backside process with the aim of enhancing the thermal management. This step aimed to conduct an initial assessment of the RF performance potential improvement after implementing thermal management techniques for GaN-on-Si HEMTs.

III.1. Backside processing of the ultrathin AlN/GaN-on-Si HEMT

Figure 5.4 illustrates the evolution of the ultrathin AlN/GaN-on-Si HEMT sample throughout the backside processing. Initially, the surface was protected with a 2 µm thick optical resist. Then, the sample was bonded to glass. Subsequently, the Si (111) substrate was thinned down to about 50 µm without any noticeable degradation (**Figure 5.4**). Deposition of Ti/Au (20/300 nm) was conducted via evaporation. Electrochemical deposition of Cu was carried out, limited to 200 µm to avoid excessive mechanical stress. However, the deposition exhibited a rather high non-uniformity, with Cu thickness varying from 100 µm to 200 µm across the sample that can be certainly optimized. Subsequently, the sample was detached from the glass, and chemical removal of grease and resist was performed. Finally, the samples underwent a standard cleaning, rinsing, and drying process to eliminate chemical residues.

After completing the backside processing, two straight lines of cracks were observed across the sample, as depicted in **Figure 5.5.a**. It was determined that these cracks occurred due to the non-uniformity of the Cu deposition. Specifically, the 100 µm difference in Cu thickness created mechanical stress, resulting in two cracks extending to the front side of the structure and making this area non-usable (**Figure 5.5.b**). Therefore, ensuring further improvement in the uniformity of Cu deposition will be essential to prevent crack formation.

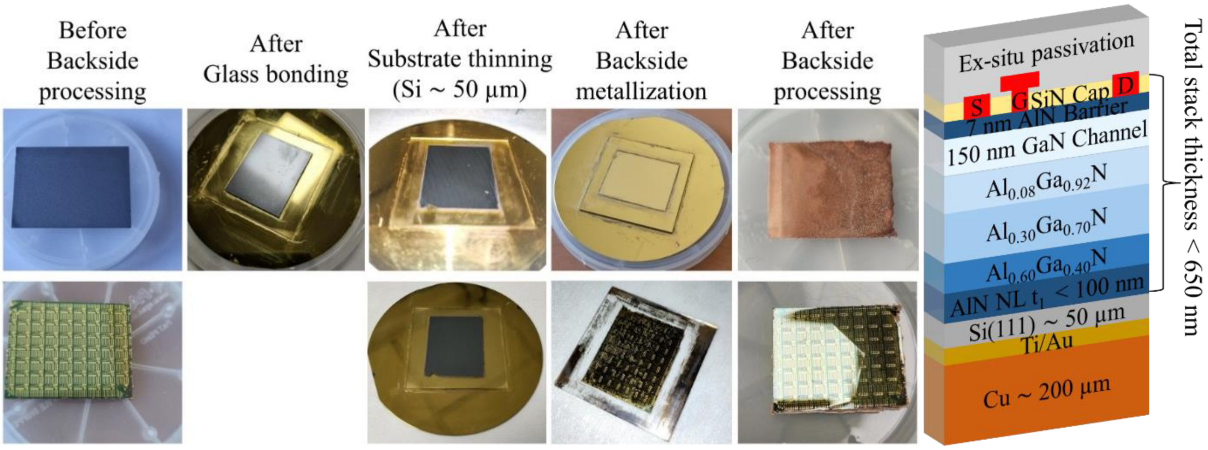


Figure 5.4.: (a) Evolution of the ultrathin AlN/GaN-on-Si HEMT sample during the backside processing and (b) schematic cross-section of the ultrathin AlN/GaN-on-Si HEMT after backside processing.

However, large area on the samples showed no signs of cracking after the backside processing (**Figure 5.5.a**). This prove that with optimization of the backside process an effective management of mechanical stress induced during the backside processing can be achieved. Specifically, maintaining the Si thickness at approximately 50 µm and adding an uniform Cu will ensured a smooth process. Furthermore, upon closer examination through SEM images, it was evident that the front side of the sample and the devices remained clean, with no evidence of residual resist or grease, as illustrated in **Figure 5.5.b.**

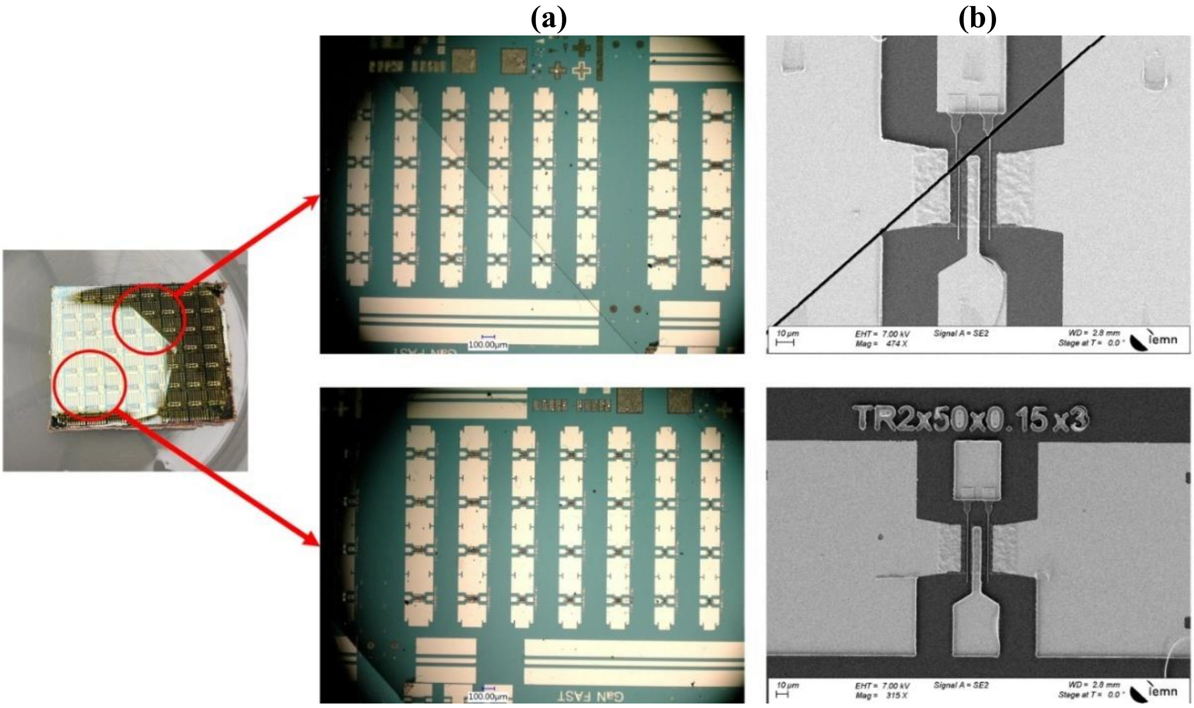


Figure 5.5.: (a) Microscope and (b) SEM images of the ultrathin AlN/GaN-on-Si devices after backside processing.

III.2. DC and small signal characterization

After completing the backside processing and confirming the absence of any physical device degradation, the transistors underwent the standard electrical characterization procedure. **Figure 5.6** and **Figure 5.7** presents the output, extrinsic transconductance, and transfer characteristics of 2 × 50 µm transistors with L_G = 140 nm and L_{GD} = 500 nm before and after the backside processing. Notably, all transistors remained functional after the backside processing.

In **Figure 5.6.a**, the output characteristic is illustrated, where the gate-source voltage was swept from -6 to +2 V with a step size of 1 V. As the channel temperature rises with increasing the gate voltage, electron mobility decreases, leading to a reduction of the current density. However, due to improved heat dissipation, the drain current density is increased compared to devices without backside processing. Nevertheless, it is observed that the improvement is still limited at higher V_{GS} (e.g., fully open channel), as the current density gap before and after backside processing drops significantly at V_{GS} = +2 V.

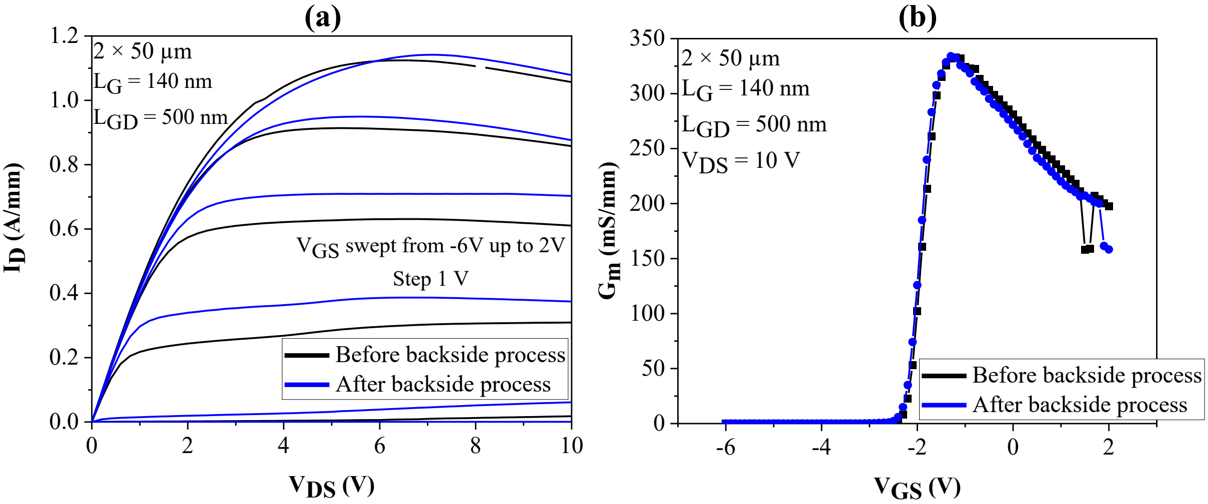


Figure 5.6.: Before and after backside processing: a) output characteristics, and (b) extrinsic transconductance of a submicron thick 2 × 50 µm AlN/GaN-on-Si HEMT with L_{GD} = 500 nm and L_G = 140 nm.

A pinch-off voltage $V_{TH} = -2.6$ V and $V_{TH} = -2.7$ V was observed before and after backside processing, respectively, as depicted in **Figure 5.7.a**. Additionally, the off-state drain leakage current remained lower than 10 µA/mm. Both before and after backside processing, the transistors exhibited a maximum extrinsic transconductance ($G_{m,max}$) of 330 mS/mm, as shown in **Figure 5.6.b**.

Figure 5.7.b illustrates the transfer characteristics, with a compliance fixed at 150 mA/mm, swept from V_{DS} = 2 to 30 V using a step of 1 V. It is noteworthy that a low threshold

voltage shift as a function of V_{DS} was maintained under high electric field up to 30 V before and after the backside process, which further confirms the absence of damage.

Figure 5.7.a depicts the transfer characteristics at V_{DS} = 10 V. Upon further observation, it can be observed that the channel is fully opened at V_{GS} = +2 V before backside processing. On the other hand, after backside process, the current density I_D continues to increase with V_{GS} while the threshold voltage is identical, indicating a thermal management improvement within the structure.

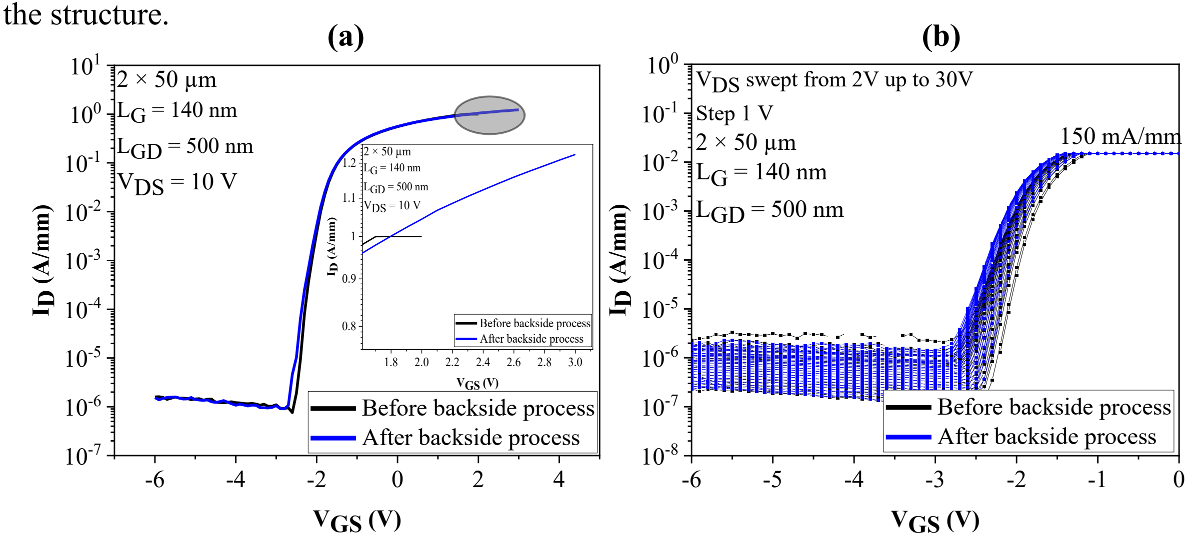


Figure 5.7.: Before and after backside processing: (a) Transfer characteristics at V_{DS} = 10 V, and (b) transfer characteristics with V_{DS} swept from 2 to 30 V of a submicron thick 2 × 50 µm AlN/GaN-on-Si HEMT with L_{GD} = 500 nm and L_G = 140 nm.

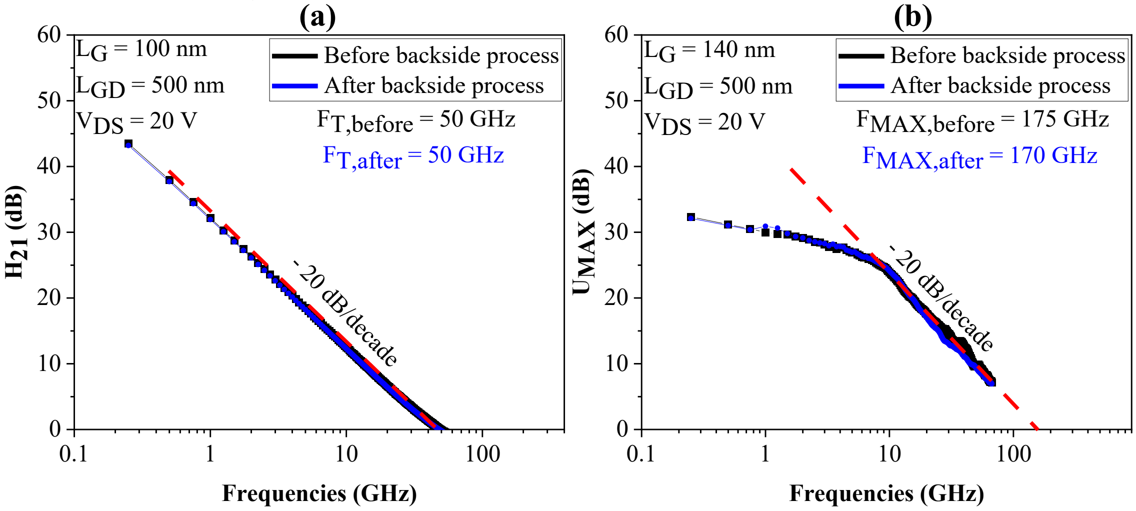


Figure 5.8.: Before and after backside processing: small signal charcteristics (a) H_{21} and (b) U_{MAX} of a submicron thick 2 × 50 µm AlN/GaN-on-Si HEMT at V_{DS} = 20 V with L_{GD} = 500 nm and L_G = 140 nm.

The S-parameters were measured from 250 MHz to 67 GHz, as illustrated in **Figure 5.8**. The current gain extrinsic cut-off frequency (F_T) remains unchanged before and after the backside process, with an F_T of 50 GHz at V_{DS} = 20 V, as shown in **Figure 5.8.a**. Likewise, the maximum oscillation frequency (F_{MAX}) remains consistent at around 170 GHz at V_{DS} = 20 V, as depicted in **Figure 5.8.b**.

RF losses were extracted from S_{21} parameters through transmission lines up to 67 GHz before and after backside process (**Figure 5.9**). Despite the significant thinning of the Si substrate RF losses are maintained lower than -0.6 dB/mm up to 67 GHz.

This set of DC and small signal measurements does not exhibit significant improvement in typical electrical characteristics, but it confirms the quality of the backside processing showing no degradation in the device RF performances.

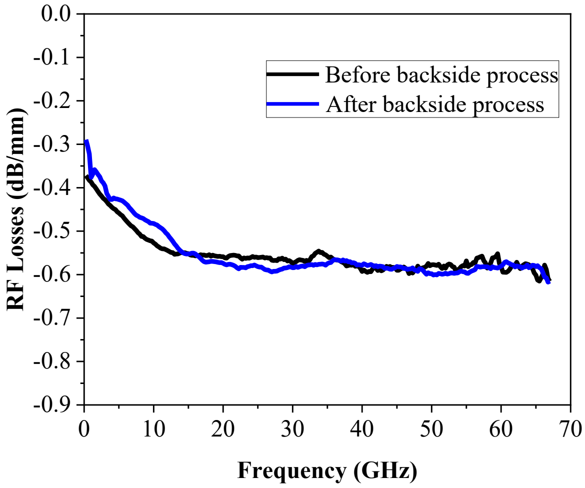


Figure 5.9.: RF Losses extracted from S_{21} parameters through transmission lines up to 67 GHz before and after backside processing.

III.3. DC pulsed and DCT characterization

To further verify the structural integrity following backside processing, trapping characterizations were conducted.

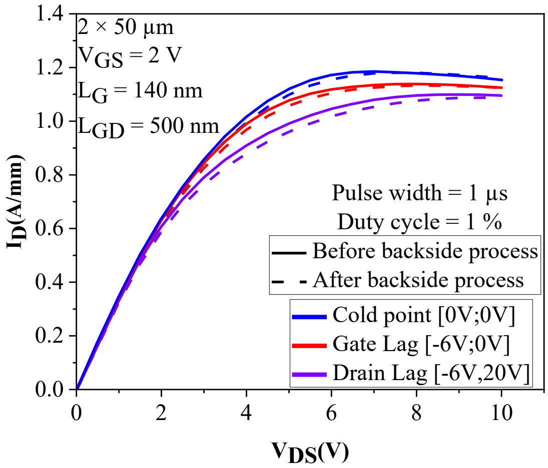


Figure 5.10.: Open channel pulsed I_D-V_{DS} output characteristics before and after backside processing.

Figure 5.10 illustrates Pulsed I_D–V_{DS} measurements. The charge trapping effects is observed at different quiescent bias points. Open-channel DC pulsed measurements were performed at room temperature with V_{GS} = +2 V. Transistors of 2 × 50 µm with L_{GD} = 500 nm and L_G = 140 nm showed no increase in current collapse post backside processing.

Figure 5.11 depicts drain current transient (DCT) measurements conducted with trap filling times of 100 µs and 100 s at $V_{DS,Fill}$ = 20 V and $V_{GS,Fill}$ = -4 V. It can be observed that for a filling time of 100 µs, less than 8% current collapse is maintained. Moreover, even with a filling time as high as 100 s, the current collapse remains below 15% showing no additional trap signature. This further validates the quality of the backside processing by showing no additional trapping effects within such thin epilayers, and despite the removal of most of the substrate and the use of very thick Cu on the backside. Consequently, the mechanical stress did not introduce any cracks into the structure that could potentially result in trapping effects.

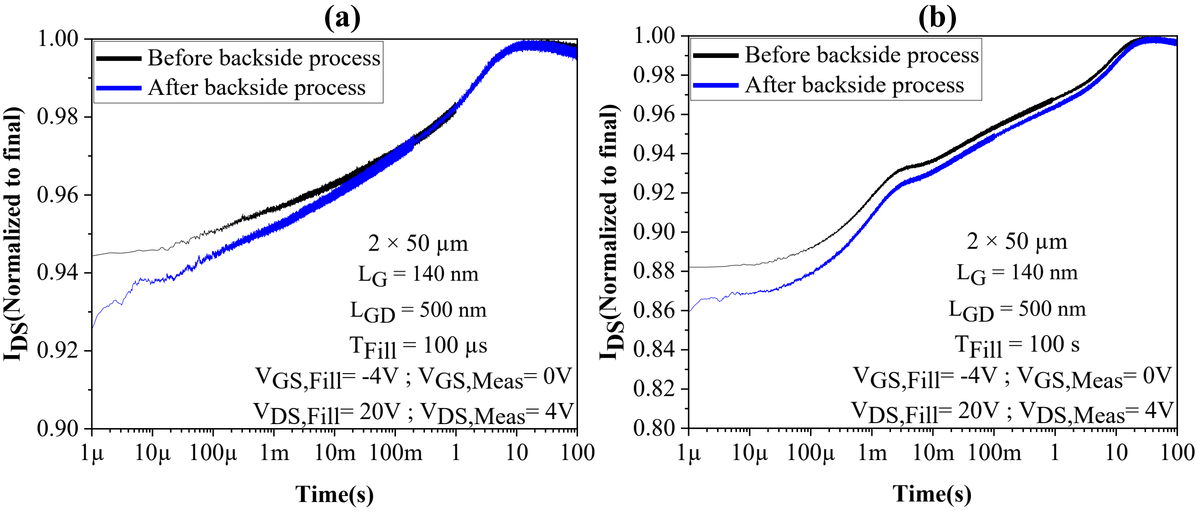


Figure 5.11.: Drain current transient characteristics for (a) 100 µs and (b) 100 s filling time with L_{GD} = 500 nm and L_G = 140 nm of a submicron thick 2 × 50 µm AlN/GaN-on-Si HEMT before and after backside process.

III.4. Large signal characterization at 40 GHz

Large signal characterizations were conducted at 40 GHz. **Figures 5.12.a and 5.12.b** illustrate the typical CW and pulsed power performances after the backside process at 40 GHz in deep class AB of 2 × 50 µm transistors with L_{GD} = 500 nm and L_G = 140 nm and V_{DS} = 10 V and 30 V, respectively. A saturated P_{OUT} of 1.1 W/mm and 1.0 W/mm associated with peak PAE values of 37.5% and 32.4% at V_{DS} = 10 V were measured in pulsed and CW mode, respectively. Meanwhile at V_{DS} = 30 V, a saturated P_{OUT} of 3.0 W/mm and 2.5 W/mm, with PAE values of 25% and 20% were measured in pulsed and CW mode, respectively. Additionally, it is worth noting that despite multiple CW Load-Pull sweeps under high gain compression (up to 10 dB), no degradation of the devices up to V_{DS} = 30 V was observed (see **Figures 5.12.c**). This emphasizes the excellent robustness of this heterostructure, which remained intact also after backside process.

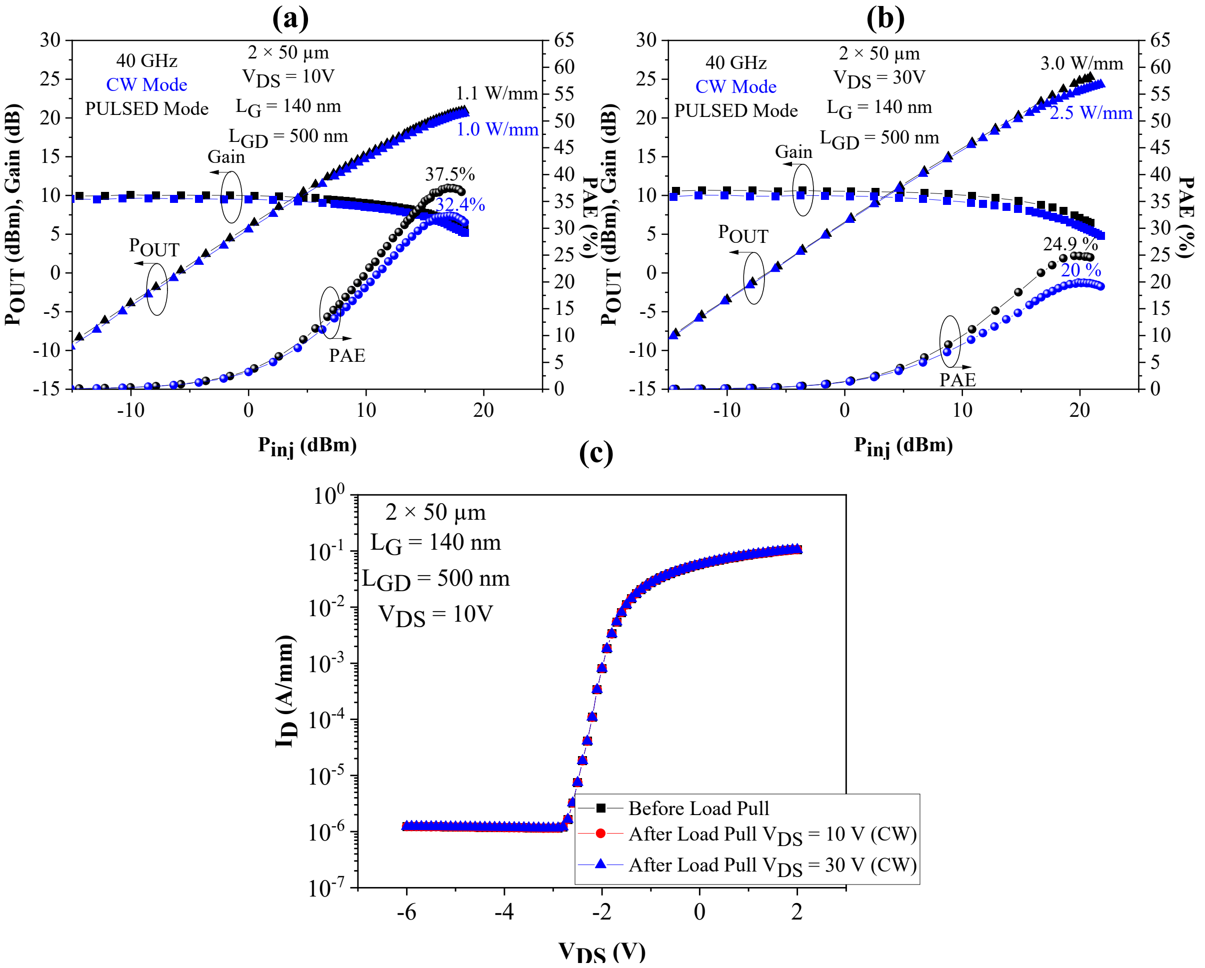


Figure 5.12.: CW and Pulsed large signal performances at 40 GHz at (a) V_{DS} = 10 V and (b) V_{DS}= 30 V. (c) Transfer characteristics after more than 40 CW Load Pull sweeps in deep class AB under high compression up to V_{DS} = 30 V with L_{GD} = 500 nm and L_G = 140 nm of a submicron thick 2 × 50 µm AlN/GaN-on-Si HEMT after backside process.

Figure 5.13 summarizes the typical pulsed and CW PAE / P_{OUT} of 2 × 50 µm transistors with L_{GD} = 500 nm and L_G = 140 nm as a function of V_{DS} at 40 GHz. The gap between the PAE in pulsed and CW measurements is rather low with approximately 5 points for a similar P_{OUT}. In contrast, prior to the backside process, a difference of around 10 points was observed between the PAE in pulsed and CW mode. Following the backside process, the power performances in both CW and pulsed mode are relatively similar, further indicating an enhanced thermal dissipation due to substrate thinning and implementation of a heat sink.

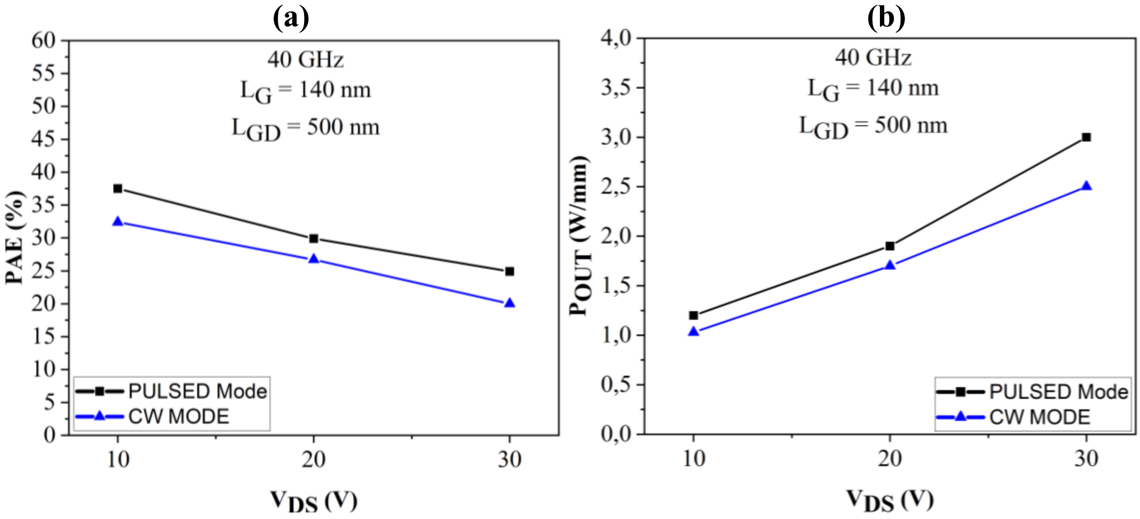


Figure 5.13.: CW and Pulsed (a) PAE and (b) P_{OUT} as a function of V_{DS} at 40 GHz with L_{GD} = 500 nm and L_G = 140 nm for 2 × 50 µm ultrathin AlN/GaN-on-Si HEMTs after backside process.

IV. Conclusion

In this chapter, initial results following the thinning of the Si substrate in ultrathin AlN/GaN-on-Si HEMT grown by NH_3-MBE together with the deposition of thick Cu as a heat sink were presented. Thinning the Si substrate requires careful control to end-up with a 50 µm thickness. It has been demonstrated that further thinning the substrate results in excessive strain and formation of cracks within the heterostructure.

The transistors after backside processing remains intact, exhibiting improved DC current and maintaining reduced trapping effects and small-signal RF performances. Consequently, class AB bias operation (up to V_{DS} = 30 V) in both pulsed and CW mode at 40 GHz yields similar results, with only a 5-point PAE difference for a gate length of 140 nm on the ultrathin GaN-on-Si HEMTs with backside processing. This outcome reflects the enhancement in thermal dissipation owing to substrate thinning and Cu heat sink deposition. Advanced techniques such as Raman spectroscopy or other methods will facilitate a more accurate quantification of this improvement.

Ultimately, further optimization of the Cu electrochemical deposition by improving the backside process quality will not only reduce the likelihood of structural cracking but also act as a better heat sink. Furthermore, optimizing the thermal management within the epitaxy is imperative to benefit even more from the advantages of employing a submicron thick heterostructure.

Conclusion:

The growing interest in millimeter-wave frequencies stems from their shorter wavelengths and broader frequency ranges, which facilitate the creation of smaller components with improved performances. Nonetheless, exploiting the millimeter-wave spectrum effectively poses various challenges. High-frequency devices must meet demanding performance criteria, including high power and efficiency, demonstrated reliability, compactness, and cost effectiveness. GaN-on-Si transistors emerge as a highly promising solution within this context.

In Chapter 1, significant advancements achieved in GaN-based HEMTs for high-frequency applications, especially in the millimeter-wave spectrum, have been outlined. It has been demonstrated that GaN exceptional properties, such as its high bandgap and electron mobility, make it an ideal material for robust transistors and integrated circuits, with potential for enhanced performances. Moreover, the thriving ecosystem of both industrial and academic players emphasizes the significance and interest in GaN technology for high-frequency power applications. Various configurations and specific material systems have been described for GaN HEMT structures in RF applications, emphasizing the importance of epitaxial structure optimization for enhanced device performance and reliability, particularly under high electric fields. Furthermore, despite progress, limitations persist, hindering the full exploitation of GaN potential. In this context, the main focus of this work was to develop submicron thick GaN HEMT devices on Si grown by MBE capable of delivering a combination of high power/high efficiency operating in the millimeter-wave range.

In Chapter 2, the process fabrication of GaN HEMTs and the essential technological steps required to achieve high performances at high frequency are addressed. Additionally, this chapter delves into the electrical characterization methods and tools employed within this context. The characterization efforts encompass various breakdown voltage characterization methods, as well as DC to large signal assessments, including drain current transient, static and pulsed I-V characterization methods. Subsequently, large signal characterization using an active load-pull approach at both 10 and 40 GHz was discussed.

In chapter 3 and 4, the electrical and structural characterizations of different structures carried out at IEMN were presented. First, an extensive examination of AlGaN/GaN HEMTs grown on Si (111) substrates, featuring various submicron thick buffers designed for high-frequency applications were presented. The heterostructure with a total buffer thickness below

650 nm and Al-rich step-graded layers, demonstrates outstanding breakdown voltage properties and low RF losses. DC characteristics reveal functional transistors with minimal off-state leakage current. Analysis of AlN nucleation layer thickness variation highlights its impact on electrical performance, together with the optimized buffer layers showcasing a remarkable vertical breakdown field exceeding 6 MV/cm. Moreover, investigations into trapping effects highlight the crucial role of in-situ passivation, with significant differences observed between heterostructures with and without an in-situ SiN cap. Further examinations on these HEMTs demonstrate their functionality under high electric fields, enabling operation at high frequencies with enhanced robustness. Afterward, a comparison was made between submicron thick AlGaN/GaN and AlN/GaN HEMTs grown on Si (111) substrates for high-frequency applications to underline the importance of thinner barriers in mitigating short-channel effects. The ultrathin AlN/GaN-on-Si HEMT heterostructures exhibit promising features, including low off-state leakage current under high electric fields up to 30 V for gate lengths of sub-150 nm, high carrier density, and low trapping effects. Structural characterization shows reduced surface roughness and dislocations within the buffer layers. DCT measurements confirm the low trapping effects, and fully stable class AB bias operation up to V_{DS} = 30 V is achieved for sub-150 nm gate length. As a result, the ultrathin AlN/GaN-on-Si HEMT structure delivers high output power density together with state-of-the-art PAE of 45.6% / 35.1% at V_{DS} = 10 V / 30 V at 40 GHz, respectively. Finally, RF short term high temperature operating reliability tests demonstrate stable ultrathin AlN/GaN-on-Si HEMTs under high-power operation.

. The last chapter discusses some preliminary results of thinning the Si substrate and introducing Cu as a heat sink. The ultrathin AlN/GaN-on-Si HEMT undergoes substrate thinning before Cu deposition, resulting in improved DC current while maintaining the initial RF characteristics. Class AB bias operation shows rather close performance in both pulsed and CW, reflecting the enhanced thermal dissipation.

Outlooks:

As discussed in Chapter 4, the ultrathin AlN/GaN-on-Si heterostructure have demonstrated high RF performances. However, there are still a few parameters limiting the full potential of this structure. Further optimization of both the structure and device fabrication, including the backside process, is necessary.

As observed in Chapters 3 and 4, the AlGaN/GaN and AlN/GaN structures have primarily exhibited limited 2DEG electron mobility (see **Figure 1.a**). This low mobility restricts the current density and, consequently, the output power density delivered during class AB bias operation. Optimization of the barrier thickness and the AlGaN transition layer, along with tuning the growth conditions of the in-situ SiN cap layer, should further enhance the electron mobility as demonstrated by A.Bairamis et al. (**Figure1.b**) [212].

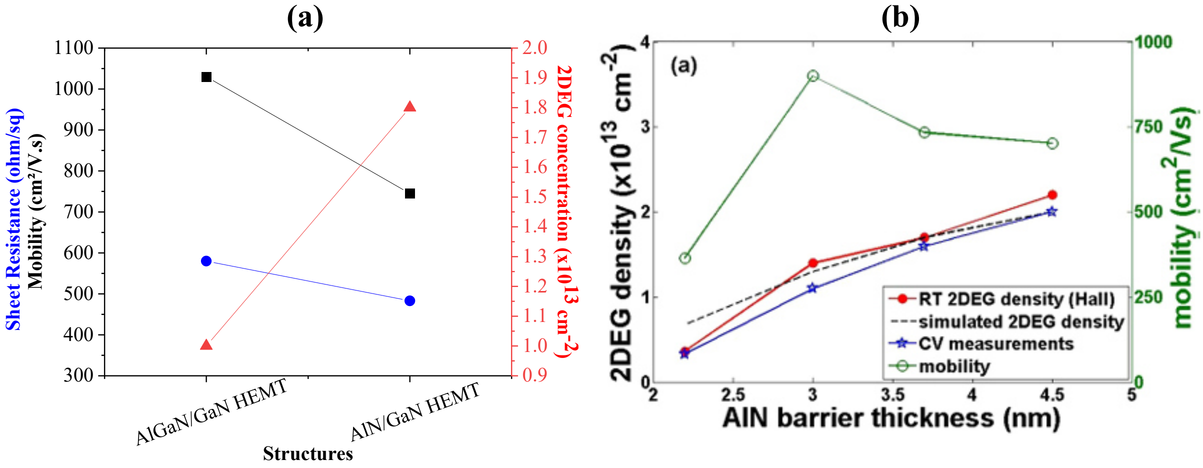


Figure 1.: (a) 2DEG electrical properties of submicron thick AlGaN/GaN and AlN/GaN HEMTs grown on Si(111) studied in this work and (b) 2DEG electrical properties as a function of AlN barrier thickness shown by A. Bairamis et al.[212].

In addition to the mobility enhancement, several process optimizations should be carried out to improve RF performances. The use of gate lengths below 140 nm is expected to yield higher performance levels. Fabrication of gate lengths below 100 nm at IEMN laboratory has already been demonstrated (see **Figure 2.a**). Implementing shorter gate lengths will certainly enhance small signal performance, thereby increasing overall RF performance. As illustrated in **Figure 2.b**, the F_t/F_{max} ratio is significantly enhanced with a reduction of the gate length. While downscaling the transistor dimensions, another key figure of merit to assess is the linearity, which is a prime parameter for many mm-wave applications.

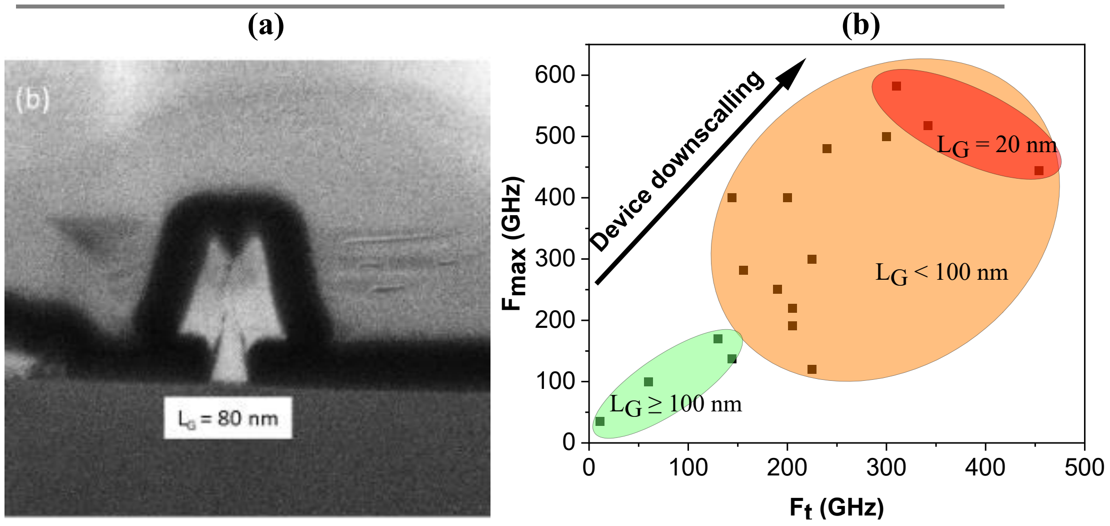


Figure 2.: (a) FIB image of a sub-100 nm T-gate gabricated at IEMN laboratory [173] and (b) maximum oscillation frequency (F_{max}) as a function of F_t with different gate length [74–85].

Moreover, the optimization of ohmic contacts conducted on the ultrathin AlN/GaN-on-Si HEMTs only allows to achieve a contact resistance of 0.4 Ω·mm. However, low contact resistance is essential for device performances, including output power, high efficiency, and high-frequency operation. A different approach, such as regrown ohmic contact technique, can lead to a drastic decrease in ohmic contact resistance. It is well-known that regrown ohmic contacts can yield a resistance as low as 0.1 Ω·mm, with the lowest reported contact resistances using MBE tool [68, 213–215].

As discussed in Chapter 5, thermal management of the structure plays a crucial role in RF performances. Preliminary results obtained with the initial thinning of the Si substrate and the use of Cu as a heat sink will pave the way for further backside process optimization. Initially, non-uniform deposition of Cu resulted in cracks in the structure. Consequently, an optimization of the electrochemical deposition of Cu will be carried out. Moreover, while the transistors remained intact after backside processing, exhibiting improved DC current, the RF performances remains similar. Therefore, advanced techniques such as Raman spectroscopy or other methods will be needed to facilitate a more precise quantification of this improvement. Additionally, novel configurations such as copper-filled trenches could be introduced. As illustrated in **Figure 3**, this configuration involves a local removal of the Si substrate and filling the trenches with Cu. This method allows local substrate removal etching down to few micrometers without generating detrimental mechanical strain that would cause sample cracking, as observed in Chapter 5 when attempting to thin the whole Si substrate below 50 µm.

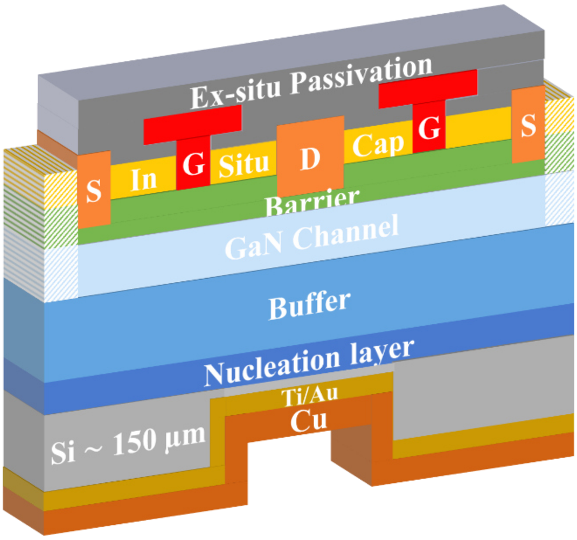


Figure 3.: Schematic cross-section of backside process with local removal of Si substarte and Cu trench fill.

As introduced in Chapter 5, a large number of techniques are often employed to enhanced thermal management of GaN HEMT. That is why, other entirely different configurations aimed at enhancing thermal management can be also explored. For example, GaN-on-diamond technology has emerged as a promising alternative for applications requiring the highest power density, owing to diamond thermal conductivity, which can be up to 6 times greater than that of SiC [216]. The longstanding challenge has been to develop a GaN-on-diamond technology that is both thermally relevant and commercially viable. The most promising approach involves employing an epitaxy transfer process technique. This technique has previously been utilized successfully for transferring GaN grown on SiC onto free-standing diamond substrate [217, 218]. Another completely different approach will consist of co-designing microfluidics and electronics within the same semiconductor substrate permitting to produce a monolithically integrated manifold microchannel cooling structure with good efficiency [198].

Finally, one of the main features of the proposed heterostructure was the submicron thickness. A major reason was the potential improvement of the thermal dissipation. Raman spectroscopy will confirm the thermal dissipation benefit with a direct comparison with a thicker structure on Si using the same growth condition and similar active layers (**Figure 4**).

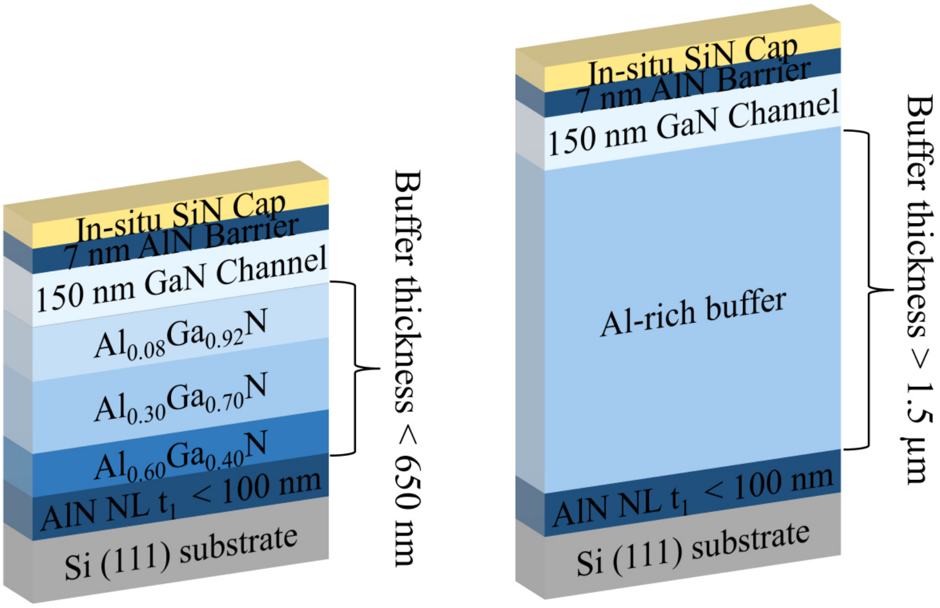


Figure 4.: Schematics cross-section of similar AlN/GAN HEMT with (a) submicron and (b) higher than 1.5 µm thick Al-rich buffer layers.

Publications related to this PhD thesis:

❖ Journals:

- E. Carneiro, S. Rennesson, S. Tamariz, K. Harrouche, F. Semond and F. Medjdoub, *Low Trapping Effects and High Blocking Voltage in Sub-Micron-Thick AlN/GaN Millimeter-Wave Transistors Grown by MBE on Silicon Substrate*, Electronics 2023, vol. 12, no. 13, 2974. https://doi.org/10.3390/electronics12132974

- E. Carneiro, S. Rennesson, S. Tamariz, K. Harrouche, F. Semond and F. Medjdoub, *Sub-Micron thick Step-Graded AlGaN Buffer on Silicon with a High Buffer Breakdown Field*, Physica status solidi A 2023, vol.220, no. 16, 202200846. https://doi.org/10.1002/pssa.202200846

- A. Bonnardot, E. Carneiro and S. Rennesson, Compound Semiconductor, 2023, vol.29, no. 5.

- K. Harrouche, W. Rili, E. Carneiro, J. Mehta, I. Abid, F. Medjdoub. *Preindustrial GaN devices developed at the nanofabrication center of IEMN*, Transducers 2021.

❖ International conferences:

- Compound Semiconductor Week (CSW) 2024 (June 3-6) at Lund (Sweden): *Short-term reliability assessment of sub-micron thick AlN/GaN-on-Silicon HEMTs grown by MBE for RF applications*, E. Carneiro, S. Rennesson, L. Ben Hammou, E. Okada, F. Semond and F. Medjdoub.

- The 14th International Conference on Nitride Semiconductors (ICNS-14) 2023 (November 12-17) at Fukuoka (Japan): *Sub-micron thick AlN/GaN-on-Si HEMTs grown by MBE with reduced trapping effects and superior blocking voltage for RF applications*, E. Carneiro, S. Rennesson, S. Tamariz, L. Ben Hammou, K. Harrouche, E. Okada, F. Semond and F. Medjdoub.

- Workshop Wocsdice Exmatec 2023 (May 21-25) at Palermo (Italy): *Comparison of Sub-Micron thick AlGaN/GaN and AlN/GaN HEMTs on Silicon for RF applications*, E. Carneiro, S. Rennesson, S. Tamariz, K. Harrouche, F. Semond and F. Medjdoub.

- International Workshop on Nitride Semiconductors (IWN) 2022 (October 9-14) at Berlin (Germany): *Sub-Micron thick Step-Graded AlGaN Buffer on Silicon with a Buffer Breakdown Field Higher Than 6 MV/cm*, E. Carneiro, S. Rennesson, S. Tamariz, F. Semond and F. Medjdoub.

- Workshop Wocsdice Exmatec 2022 (May 3-6) at Ponta Delgada (São Miguel Island – Azores (Portugal)): *Sub-Micron Thick GaN-on-Si HEMTs with More than 7.5 MV/cm Buffer Breakdown Field*, E. Carneiro, S. Rennesson, S. Tamariz, F. Semond and F. Medjdoub.

- The International Conference on Molecular Beam Epitaxy (ICMBE) 2022 (September) at Sheffield (United Kingdom): *From research to production: how MBE can unlock GaN-on-Si technology*, F. Semond, S. Rennesson, S. Tamariz, E. Carneiro, J. Mehta, and F. Medjdoub.

- 8th International Conference on Antennas and Electromagnetic Systems, AES 2022 (May) at Marrakesh, (Morocco): *Status and progress of millimeter-wave GaN transistors for next generation high-power radar systems*, K. Harrouche, S. S. Vankatachalam, E. Carneiro, F. Grandpierron, and F. Medjdoub.

❖ Awards:

- The 14th International Conference on Nitride Semiconductors (ICNS-14) 2023 (November 12-17) at Fukuoka (Japan): **“Best student award”**

- Workshop Wocsdice Exmatec 2023 (May 21-25) at Palermo (Italy): **“Best Student paper award”**

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