Substrate engineering and advanced epitaxial growth for the production of group IV semiconductor freestanding membranes

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Thèse de doctorat

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Ingénierie des substrats et la croissance épitaxiale avancée pour la production de membranes autoportantes de matériaux semi-conducteurs du groupe IV

Titre anglais

Substrate engineering and advanced epitaxial growth for the production of group IV semiconductor freestanding membranes

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“Báseň snese všechno. Čím větší pitomost, tím více lidí hledá v ní zrnko myšlenky, schopnost, neobyčejný talent, a tím více lidí uznává genialitu básníka.”

Jaroslav Hašek

Résumé

Les membranes autoportantes à base de semi-conducteurs (FSMs) sont récemment devenues cruciales pour l'expansion rapide de la nanoscience et de la technologie, représentant un domaine très prometteur de recherche avancée sur les matériaux. Les FSMs offrent un degré de liberté supplémentaire pour des mises en œuvre impossibles à obtenir par des méthodes conventionnelles telles que l'hétéroépitaxie de matériaux avec un désaccord de mailles cristallines très important. La fabrication de FSMs à partir de divers matériaux permet un empilement couche par couche, facilitant un couplage des propriétés physiques de matériaux différents. De plus, les structures FSMs offrent une légèreté et une flexibilité sans précédent par rapport aux substrats conventionnels. Cela démontre leur fort potentiel pour la fabrication de nouveaux dispositifs, notamment l'électronique sur la peau, les dispositifs empilés verticalement, l'optoélectronique flexible, etc., ainsi qu'une voie direct pour l'hétéro-intégration. De plus, l'utilisation de FSMs permet des économies significatives de coûts dans la production de dispositifs, en particulier pour des matériaux dont les prix sont plusieurs ordres de grandeur supérieurs à ceux du silicium, car seule une fraction du matériau est utilisée par rapport aux substrats conventionnels. Dans ce contexte, les FSMs de matériaux du groupe IV attirent beaucoup d'attention pour leurs applications dans l'optoélectronique haute performance et les dispositifs de télécommunication à haute vitesse tels que les guides d'ondes, les transmissions THz, les photodétecteurs et les lasers, ainsi que pour leur biocompatibilité et leur non-toxicité par rapport aux contreparties en matériaux III-V. Cependant, la fabrication de FSMs de haute qualité à partir des matériaux de groupe IV reste une tâche difficile.

Dans cette thèse, nous démontrons deux voies prometteuses pour produire des FSMs du groupe IV en développant les méthodes de l'ingénierie des substrats et de la croissance épitaxiale avancée. La première partie de ce travail se concentre sur l'épitaxie assistée par les matériaux 2D. Nous introduisons l'approche de nucléation par point d'ancrage permettant la croissance de FSM de haute qualité sur une surface recouverte de graphène. Grâce à un traitement au plasma, des défauts tels que des liaisons pendantes et des ouvertures nanometriques sont introduits dans la couche de graphène, agissant comme des sites de nucléation préférentiels lors de la croissance. Les données expérimentales

dévoilent la nature de ces défauts, leur rôle dans la nucléation et les mécanismes régissant cette technique. De plus, la microscopie électronique à transmission haute résolution combinée à une analyse de phase géométrique établit que les couches nouvellement formées sont parfaitement monocristallines, sans contraintes et orientées par le substrat sous la couche de graphène modifiée. Ces découvertes fournissent de nouvelles perspectives sur l'ingénierie du graphène par plasma et ouvrent une voie universelle pour l'hétéro-intégration de semi-conducteurs 3D de haute qualité sur le graphène, ainsi que la fabrication de FSMs.

La deuxième partie de ce travail se concentre sur une approche alternative pour la formation de FSMs en matériaux du groupe IV en utilisant des substrats nanostructurés. Tout d'abord, nous démontrons la formation de couches homogènes de germanium poreux (PGe) sur l'ensemble de la plaquette de 100 mm en utilisant une gravure électrochimique bipolaire, avec la possibilité de régler les propriétés physiques de la structure PGe par variation des paramètres de gravure. La nanostructure PGe maintient la nature cristalline et l'orientation du substrat de germanium (Ge), et présente une faible rugosité de surface, en faisant un substrat idéal pour l'épitaxie. La croissance à basse température permet de maintenir l'intégrité du PGe lors de la formation de FSM de haute qualité sur le dessus. La membrane peut être par la suite facilement détachée à travers l'interface poreuse et le substrat peut être nettoyé pour une réutilisation et la fabrication de plusieurs générations de FSMs à partir de même substrat. Ces découvertes offrent de nouvelles opportunités pour produire des dispositifs optoélectroniques légers et flexibles de haute performance basés sur les FSMs de Ge, tout en assurant une réduction à la fois des coûts et de la consommation de matériaux critiques.

Mots-clés: Membranes autoportantes, Matériaux du groupe IV, Germanium, Épitaxie assistée par matériaux 2D, semi-conducteurs poreux, détachement, réutilisation du substrat

Abstract

Semiconductor-based freestanding membranes (FSMs) have recently become central to the rapidly expanding frontiers of nanoscience and technology, and a highly promising area of advanced materials research. FSMs offer an extra degree of freedom for implementations that cannot be obtained by conventional methods such as heteroepitaxy, which often involves significant lattice mismatch in crystalline structures. Fabrication of FSMs from various materials allows for layer-by-layer stacking, enabling an easy coupling of the physical properties of dissimilar materials. Additionally, FSM structures offer unprecedented lightweight, and flexibility compared to conventional substrates. This demonstrates their high potential for the fabrication of novel applications, such as stretchable on-skin electronics or vertically stacked devices, flexible optoelectronics, etc., as well as a straightforward path for heterointegration. Furthermore, the use of FSMs provides significant cost savings in device production, especially for materials with orders of magnitude higher prices than that of silicon, as only a fraction of the material is being used when compared to conventional wafers. In this context, group IV materials FSM attract a lot of attention for their applications in high-performance optoelectronics and high-speed telecommunication, as well as for their biocompatibility and nontoxicity compared to III-V counterparts. However, the fabrication of high-quality group IV FSMs is still a challenging task.

In this thesis, we demonstrate two promising paths for production of group IV FSMs using substrate engineering and advanced epitaxial growth. The first part of this work focuses on 2D-assisted epitaxy. We introduce the Anchor Point Nucleation approach enabling the growth of high-quality FSMs over a graphene-covered surface. Through plasma treatment defects, such as dangling bonds and nanoholes, are introduced in the graphene layer, acting as preferential nucleation sites. The experimental data unravel the nature of these defects, their role in nucleation, and the mechanisms governing this technique. Additionally, high-resolution transmission electron microscopy combined with geometrical phase analysis established that the as-grown layers are perfectly single crystalline, stress-free, and oriented by the substrate underneath the engineered graphene layer. These findings provide new insights into graphene engineering by plasma and open

a universal pathway for the heterointegration of high-quality 3D semiconductors on graphene, and fabrication of FSMs.

The second part of this work focuses on an alternative approach to produce group IV FSMs using nanostructured substrates. First, we demonstrate the formation of homogenous porous germanium (PGe) layers across the entire 100 mm wafer using bipolar electrochemical etching, with the possibility to tune the physical properties of the PGe structure by variation of etching parameters. The PGe nanostructure maintains the crystalline nature and orientation of the Ge substrate, and presents low surface roughness, making it an ideal substrate for the epitaxy. The low-temperature growth allows maintaining the PGe's integrity during the formation of high-quality FSM on top. The membrane can then be easily detached through the porous interface and the substrate can be cleaned for reuse and fabrication of multiple FSMs generations. These findings provide new opportunities to produce lightweight and flexible, high-performance optoelectronics based on Ge FSMs, while also ensuring reduction of both costs and critical material consumption.

Keywords: Freestanding membranes, Group IV materials, 2D-assisted epitaxy, Germanium, Porous semiconductors, Lift-off, Substrate reuse

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First, I would like to thank Prof. Abderraouf Boucherif for providing me with the opportunity to pursue my Ph.D. thesis. Your trust in me and the freedom you provided to me in my research opened many opportunities I could not have taken otherwise.

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For these last few lines, I'm switching to my mother tongue. Although, I'm not as well versed as I once was, I want to avoid any unnecessary translations as they are meant for my family. V neposlední řadě bych chtěl poděkovat svým rodičům a rodině. Vaše neochvějná podpora mi umožnila vydat se na tuto dlouho cestu a překonat veškeré překážky, které mě na ní potkaly. A proto veškeré moje úspěchy jsou z nemalé části i vaší zásluhou.

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Table of Abbreviations

Abbreviation	Signification
2D	Two-dimensional
3D	Three-dimensional
AFM	Atomic force microscopy
AlAs	Aluminum arsenide
AlInP	Aluminum indium phosphide
AlN	Aluminum nitride
APN	Anchor point nucleation
As	Arsenic
BEE	Bipolar Electrochemical Etching
CBE	Chemical beam epitaxy
CCD	Charge-coupled device
CMP	Chemical mechanical polishing
COMS	Complementary metal-oxide-semiconductor
CPV	concentrated photovoltaics
CrN	Chromium nitride
Cu	Copper
CVD	Chemical vapor deposition
DIW	Deionized Water
EBSD	Electron Backscatter Diffraction
EE	Electrochemical etching
ELO	Epitaxial Lift-off
EtOH	Ethanol
FFT	Fast Fourier transform
FIB	Focused ion beam
FSM	Freestanding membrane
FWHM	Full width at half maximum
Ga	Gallium
Ga_2O_3	Gallium oxide
GaN	Gallium nitride
GaAs	Gallium arsenide
Ge	Germanium
GIXRD	Grazing incident X-ray diffraction
GoN	Germanium-on-Nothing
H_2O_2	Hydrogen peroxide
HAADF-STEM	High-angle annular dark-field STEM
hBN	Hexagonal boron nitride
HBr	Hydrobromic Acid

HCl	Hydrochloric acid
HF	Hydrofluoric acid
HRTEM	High-resolution Transmission electron microscopy
HRXRD	High-resolution X-ray diffraction
IFFT	Inverted Fast Fourier Transform
InAlAs	Indium aluminum arsenide
InGaAs	Indium gallium arsenide
InP	Indium phosphide
IPA	isopropyl alcohol
IR	Infrared
LED	Light-emitting diode
LLO	Laser lift-off
ML	Monolayer
Mo	Molybdenum
N_2	Nitrogen
Nb_2N	Niobium Nitride
O_2	Oxygen
O_3	Ozone
PDMS	Polydimethylsiloxane
PGe	Porous germanium
PMMA	polymethyl methacrylate
Pt	Platinum
PTEF	Polytetrafluoroethylene
QVdWE	Quasi-Van der Waals epitaxy
RE	Remote Epitaxy
RF	Radio frequency
RMS	Root Mean Square
SEM	Scanning electron microscopy
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon oxide
SLG	Single layer graphene
Sn	Tin
SOI	Silicon-on-Insulator
SoN	Silicon-on-Nothing
STEM	Scanning Transmission electron microscopy
TEM	Transmission electron microscopy
TPV	Thermophotovoltaics
VdW	Van der Waals
VdWE	Van der Waals epitaxy

XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
XRR	X-ray reflectivity
ZnO	Zinc oxide

Chapter I

1. Introduction

This chapter introduces the general context of the semiconductor freestanding membranes (FSMs) and their potential for future generations of electronics and main challenges in their fabrication. It also presents the context, objectives, original contributions, and an overview of this work.

1.1 Context and challenges

Semiconductor materials and devices are the fundamental components of modern electronics and optoelectronics. Ranging from individual LEDs (Light-emitting diodes), sensors, and lasers to computer clusters, LED displays, and solar panel arrays, semiconductors are ubiquitous in our daily lives and have a significant impact on our society. The progress in epitaxial growth and heterointegration technology has enabled the creation of high-quality layers and heterostructures on specific and suitable substrates. These structures are then transformed into functional devices like lasers, photodetectors, or transistors using conventional microfabrication processes. These devices can be then individually packaged and assembled into a final functional devices and systems.

In many cases, the host substrate is retained throughout the device fabrication or even plays an active role in the device structure. However, there is an increasing number of applications where the semiconductor layers need to be very thin (from tens of nm to a few μm), detached from the growth substrate, and transferred to a new one. One example of such application is near-field thermophotovoltaics (TPV) for heat-to-electricity conversion, where the initial thick growth substrate causes parasitic radiative coupling[1,2]. The use of membrane-based devices prevents this from happening, and it enables the use of backside reflectors, further improving the device efficiency.

Another area highly interested in membrane-based structures is advanced device fabrication and packaging. As an ever-expanding variety of materials needs to be integrated together and the device size slowly approaches its physical limits, both academia and industry focus on the development of new strategies for material heterointegration and nanofabrication. Today, heteroepitaxy is the most used technique for direct heterointegration of monocrystalline materials on top of each other, enabling the fabrication of high-quality crystalline heterostructures. However, the combination of materials accessible by this technique is very limited, due to the lattice mismatch and thermal expansion coefficient difference between the substrate and epitaxial layer, causing layer strain. Indeed, beyond a critical thickness, the epitaxial layer plastically relaxes, causing the formation of defects (mainly dislocations), which are detrimental to the electric and photonics performances of the final device. Currently, only a few materials are

industrially produced in the form of substrate wafers (Si, Ge, GaAs, GaP, GaSb, InP, InSb, InAs, SiC, GaN, AlN, CdS, sapphire), all the remaining monocrystalline semiconductor materials such as SiGe, GeSn, InGaAs, InAs, etc., are currently grown on top of these substrates by conventional heteroepitaxy. In contrast to conventional substrates, freestanding membranes (FSMs) offer an extra degree of freedom for implementations such as heterointegration of dissimilar materials with high lattice mismatch in crystalline structures, by allowing for various materials to be stacked on top of each other and enabling easy coupling of highly dissimilar material's properties. Layer stacking also has tremendous potential for vertical device architectures, further pushing the limits of miniaturization[3]. Additionally, layer transfer techniques enable simple path for 3D integration of various device components such as lasers, LEDs, detectors, solar cells, etc., on mature Si-based platform allowing the creation of novel complex high-performance devices, which could not be otherwise realized on a single substrate[4–6]. Moreover, the ability to FSMs from various materials can further broaden the selection of available substrates, including materials that can't be produced in bulk form.

The development of light and/or flexible devices stands as another significant driver for the necessity to create cost-effective techniques for layer and chip transfer. Flexible electronics possess a wide array of potential applications, including flexible or stretchable displays[7–20], flexible transistors[8–16], flexible solar cells[30–39], flexible sensors[40–47], wearable medical devices[48–52], and human–machine interfaces[53–56]. Although organic semiconductors are naturally well suited for producing flexible devices due to their compatibility with solution-based processes and conformal coatings on flexible substrates, they often exhibit compromises in device performance when compared to their inorganic counterparts. Conversely, inorganic semiconductors generally offer superior electron mobility, stability, and lifetime, but they cannot be directly grown on plastic substrates. This limitation is partly attributed to the incompatible processing conditions of inorganic semiconductors with flexible substrates. This, in turn, obstructs the direct fabrication of inorganic devices on plastic substrates since the processing temperature exceeds the thermal tolerance of flexible plastics. Consequently, a more feasible approach involves separating the fabrication of inorganic devices from the assembly process onto flexible substrates.

Finally, the use of FSMs provides significant cost savings for device production, especially for materials with 2-3 orders of magnitude higher prices than that of Si, compared to their bulk counterparts. Not only that the use of a few μm-thick FSM instead of a few hundreds μm-thick conventional substrates notably reduce the quantity of generally expensive materials such as III-V, III-N, Ge, but also layer transfer techniques usually offer the possibility to reuse the same substrate for production of multiple FSMs. Both those factors play an important role in the final substrate's price. By using membrane-based substrates this price could be significantly reduced, driving the overall cost of device production down.

The conventional methods for layer transfer are generally based on wafer bonding of the structure and substrate thinning either by mechanical[57–59], chemical[60,61], or dry etching methods. However, the main challenge of these methods is an accurate control of the membrane thickness and surface roughness, especially over large surfaces. The membranes produced by these methods cannot reach sub 10 μm threshold and often uses costly chemical-mechanical polishing to reduce the surface roughness. Moreover, most of the initial wafer's material is lost during the thinning process. To face these challenges a plethora of transfer techniques is being studied and developed, including sacrificial layer epitaxial lift-off techniques, 2D-assisted epitaxy and exfoliation, and mechanical release methods.

For instance, 2D-assisted epitaxy techniques such as Van der Waals epitaxy (VdWE) and remote epitaxy (RE), using 2D material interlayers, has shown tremendous potential for fabrication of III-N and III-V semiconductor compounds FSMs[62–64], as well as other materials such as various oxide compounds[65–78], perovskites[79], metals[80], and 2D materials[81–83]. This variety of applications makes 2D-assisted one of the most promising techniques for the development of highly mismatched heterostructures and FSMs. Nonetheless, its application for non-polar group IV materials such as Ge and its alloys there is very challenging due to the lack of interactions of the epilayer with the 2D interface and/or underlying bulk substrate. These materials are especially useful for applications in high-performance optoelectronics and high-speed telecommunication devices such as waveguides, THz transmission, photodetectors, biosensors, lasers, or

thermophotovoltaics. A variety of alternative techniques have been demonstrated to produce non-polar group IV material FSMs, namely epitaxial lift-off, mechanical spalling, and use of nanostructured substrates. Despite the progress made, their general adoption is still hindered by many obstacles including process complexity, high-cost, and substrates damage and/or contamination issues.

The focus of this thesis is on the development of novel techniques, using substrate engineering and epitaxial growth for fabrication of group IV material FSMs and their direct heterointegration with 2D materials. Namely, we introduce a novel technique for 2D-assisted epitaxy enabling growth of high-quality non-polar epilayers, and porosification lift-off process using wafer-scale porous Ge substrates for fabrication of FSMs and substrate reuse. This is a crucial steppingstone for the development of next-gen group IV FSM-based applications and devices (Figure 1-1).

Figure 1-1: Illustration of group IV semiconductor FSMs and their advantages.

1.2 Objectives

The objectives of this thesis can be subdivided into two principal development axes for fabrication of freestanding membranes through 2D-assisted epitaxy and porosification lift-off, respectively.

1.2.1 Development of 2D-assisted epitaxy method for non-polar materials

- Conceptualize a novel approach for 2D-assisted epitaxy of non-polar materials enabling growth of high-quality layers on graphene.
- Study of the graphene interlayer engineering by using plasma treatment.
- Identify the effects of various graphene defects on epitaxial nucleation and growth.
- Demonstrate high-quality epilayers grown on a non-polar substrate covered with engineered graphene.

1.2.2 Development of porosification lift-off for group IV semiconductor freestanding membrane fabrication and substrate reuse

- Establish the process of uniform porous germanium (PGe) layer formation at wafer-scale through electrochemical etching.
- Identify etching parameters that enable the modulation of the physical properties of the PGe.
- Develop non-destructive characterization methods to evaluate the uniformity of the PGe layers.
- Study the growth stages of Ge on PGe substrate.
- Demonstrate the fabrication of high-quality and large-scale Ge FSMs on PGe substrate.
- Implement a chemical treatment for substrate reconditioning after detachment.
- Demonstrate a successful substrate reuse.

1.3 Original contributions

The original contribution of the present research work is as follows:

- Application of Anchor Point Nucleation for Heterointegration on 2D materials and FSMs fabrication:
  - Implementation of graphene surface engineering through plasma treatment to create nanometric openings in the graphene lattice.
  - Understanding of the nucleation process on engineered graphene substrates, along with the through-hole crystal orientation transfer.
  - Demonstration of high-quality, monocrystalline Ge membranes over graphene-covered substrates.
- Implementation of Bipolar Electrochemical Etching (BEE) for Homogenous PGe Layers:
  - Identification and optimization of BEE parameters to mitigate lateral inhomogeneity of PGe layers.
  - Development of new porosification tools for edge-to-edge porosification of entire wafers.
  - Tuning of PGe layer properties, including layer thickness and porosity.
  - Application of fast feedback, non-destructive characterization methods to assess the homogeneity of PGe layers.
- Fabrication of Wafer-Scale Ge FSMs and Substrate Reuse:
  - Establishment of nucleation and growth mechanisms on PGe substrates.
  - Epitaxial growth of high-quality, monocrystalline Ge membranes at low temperatures on PGe substrates.
  - Successful detachment of wafer-scale Ge FSM.
  - Implementation of a chemical cleaning process to remove PGe residues, allowing the substrate reuse.
  - Reporosification of a cleaned and reconditioned substrate

1.4 Thesis overview

This thesis consists of seven chapters, each developing one of the research objectives. **Chapter I** introduces the general context of the research project, presenting the main advantages of semiconductor FSMs compared to traditional bulk structures. It highlights their potential for dissimilar material heterointegration and applications in flexible electronics, as well as the economic and sustainability benefits of using FSMs. The chapter also addresses the major limitations and challenges in the fabrication methods of semiconductor FSMs, especially for group IV materials. Additionally, it defines the objectives of the research work and emphasizes the originality of this research.

In **Chapter II**, a comprehensive state-of-the-art review introduces the ever-growing plethora of techniques employed for FSMs fabrication. This review positions our work within the broader research efforts in FSM development. The chapter introduces the concepts of 2D-assisted epitaxy techniques, relying on weak Van der Waals bonding between the 2D material-covered substrate and the FSM. Unique epitaxial challenges of heterointegration on 2D materials, particularly for non-polar materials such as Si, Ge, and GeSn, are identified, leading to the introduction of our approach called Anchor Point Epitaxy, using engineered 2D interface. This chapter also discusses alternative techniques for the production of group IV FSMs, employing nanostructured substrates, and highlights the major roadblocks in their widespread adoption. This underscores the significance of our work on the large-scale substrate nanostructuring process and the use of such substrates for the epitaxial growth of group IV FSMs.

Chapter III represents a research article published in the scientific journal *Small*, summarizing the work on the heterointegration of 3D materials on 2D substrates using Anchor Point Epitaxy. The article demonstrates the surface engineering of the graphene surface by plasma treatment, creating nanometric openings in the graphene lattice. These openings serve as preferential nucleation sites for epitaxial growth, efficiently anchoring the membrane on the substrate and orienting its crystalline structure. As a result, fully relaxed, defect-free, and dense membranes with monocrystalline quality are formed over graphene-covered substrates, showcasing the potential of the Anchor Point Epitaxy as a universal approach for heterointegration on 2D materials and for FSM fabrication.

Chapter IV represents research article published in *Advanced Materials Interfaces*, reporting on the large-surface formation of homogenous porous Ge layers and their fast feedback, non-destructive characterization. The optimized bipolar electrochemical etching process and newly developed porosification cells, introduced in this work, enable the formation of highly uniform edge-to-edge PGe structures over the entire 100 mm wafer, with the possibility to tailor their physical properties, such as porosity and thickness, for specific applications. Moreover, the characterization, using X-ray reflectivity and ellipsometry measurements, establishes a nondestructive quality control method for PGe substrates.

Chapter V presents a research article published in *Materials Today Advances*, which details our work on epitaxial growth on PGe substrates and the fabrication of 100 mm wafer-scale Ge FSM. The paper elucidates the initial growth stages on 3D porous substrates and the transition from island nucleation to the layer-by-layer growth regime. This enables the formation of high-quality membranes on top of unreconstructed PGe layers. The PGe nanostructure tuning then allows for easy detachment, resulting in large FSM. Additionally, the proposed chemical cleaning process, allows for efficient dissolution of the PGe residues on the parent substrate, preparing its surface for reuse and the production of multiple FSM.

Chapter VI showcases a research article published in *Sustainability*, presenting the optimized process of the Ge FSM fabrication with further reducing the Ge consumption. The publication details the cleaning process of the PGe residues, involving slow chemical etching of the nanometric crystals remaining on the substrate surface after the detachment as well as successful reporosification of the recovered substrate.

Finally, **Chapter VII** summarizes the results presented in this work and discusses the perspectives and opportunities for further development and applications of the processes introduced in this thesis.

Chapter II

2. State of the art on freestanding membrane fabrication

This Chapter provides an overview of various FSMs fabrication techniques, their principles, and most used materials. This includes techniques using conventional heteroepitaxy approach, 2D-assisted epitaxy, and substrate engineering as illustrated by Figure 2-1. It also positions the advancements achieved in this thesis into a larger context.

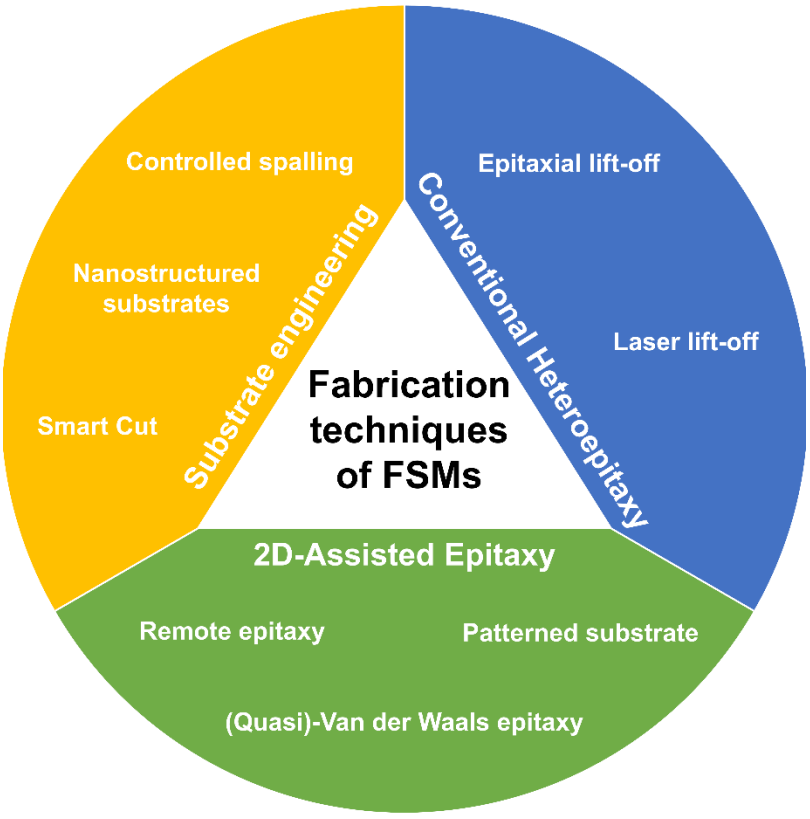

Figure 2-1: Illustration of different fabrication techniques of FSMs.

2.1 Membrane Production by Conventional Heteroepitaxy

Conventional heteroepitaxy is an instinctively apparent pathway for fabrication FSMs, as it is commonly used for the direct heterointegration of high-quality materials. To allow layer separation, sacrificial layers that can be selectively etched or decomposed without affecting the rest of the epitaxial stack are employed[84]. To achieve high-quality epilayers, fit for device applications, the sacrificial layer must be suitable for heteroepitaxial growth. The two primary parameters to consider achieving high-quality monolithic heteroepitaxy are lattice mismatch and expansion coefficient difference between the substrate (sacrificial layer in this case) and the epilayer. During heteroepitaxial growth, the chemical covalent bonding at heterointerface force the elastic deformation of the epilayer's lattice parameter to accommodate the difference with the substrate, causing the strain in the layer (Figure 2-2b)[85].

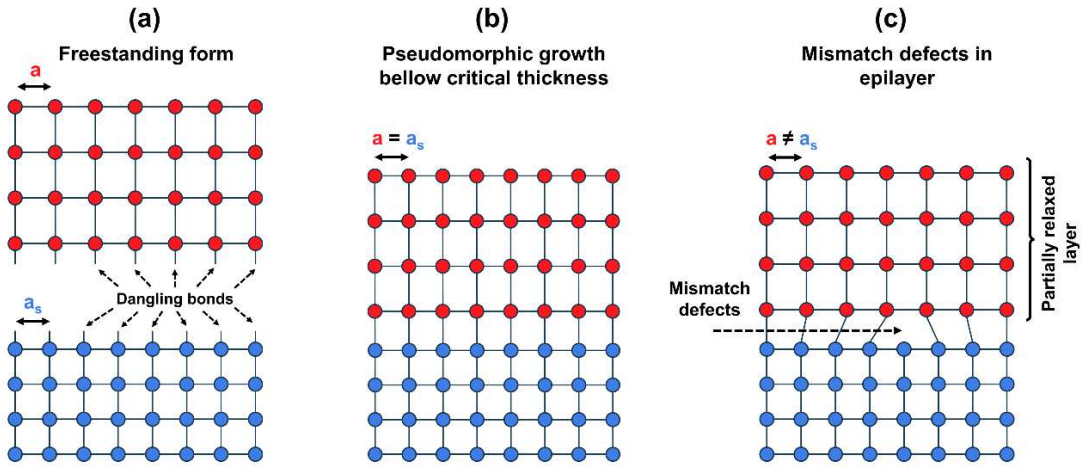

Figure 2-2: Schematic illustration of conventional heteroepitaxy, (a) freestanding form of the layer and substrate with their natural lattice parameters, (b) Pseudomorphic growth of strained epilayer below its critical thickness, (c) Partially relaxed epilayer with mismatch defects.

For systems with low lattice mismatch (<1%), the first layers of the growth allow this elastic deformation by strain, enabling the pseudomorphic growth. However, the accumulated strain in the epilayer increases with the thickness of the layer. Eventually, when the epilayer thickness exceeds the critical thickness, at which point, the system

cannot accommodate the strain and relaxes by formation of defects such as dislocations (Figure 2-2c). Similarly, for systems with high expansion coefficient difference between the growth substrate and epilayer, the layer stress is formed during the heating and cooling cycles due to the varying lattice expansion/contraction, causing the formation of the cracks in the structure when it is cooled at room temperature after the growth. In both cases the defects formed in the epilayer are detrimental for its electronic and optoelectronic performance.

These fundamental limitations of conventional heteroepitaxy then apply to epitaxial and laser lift-off techniques used for FSMs production, limiting their application to nearly lattice matched structures, and thus significantly reducing the variety of applicable materials. For this reason, epitaxial and laser lift-off techniques, using conventional heteroepitaxy for FSM fabrication, employs nearly lattice matched structures to avoid defect formation in the membrane.

2.1.1 Epitaxial Lift-Off

Epitaxial Lift-off (ELO) has been first introduced in the late ’80s as a means to produce thin GaAs (Gallium arsenide) membranes for applications in concentrated photovoltaics (CPV)[86]. Since then, this approach for layer transfer has received significant attention and has been applied to other III-V materials[87] as well as III-N[88,89] and II-VI[90] compounds, Ge[91,92], complex oxides[93], or metal films[94].

ELO relies on sacrificial layers introduced between the substrate and epilayer, which can be removed using chemical etching solutions to separate the epilayer from the substrate, while preserving their integrity (Figure 2-3). The main requirements for this technique are: (i) Growth compatibility of the epilayer with the sacrificial layer (ii) High etching selectivity of the sacrificial layer with respect to the substrate and epilayers.

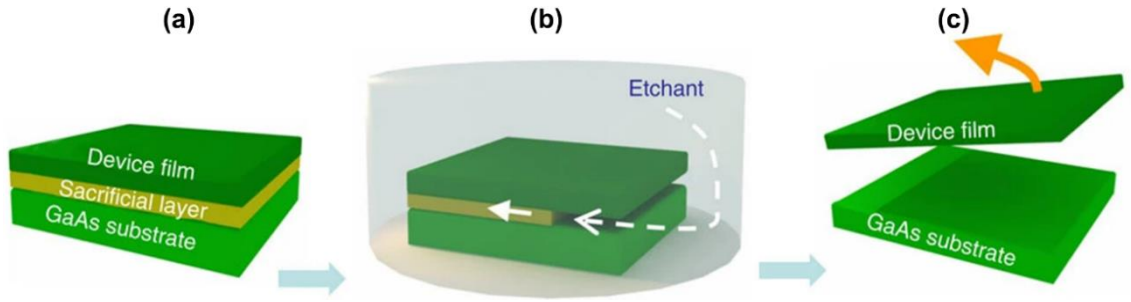

Figure 2-3: Schematic illustration of the ELO process: (a) Growth of the sacrificial layer and device membrane, (b) etching of the sacrificial layer, (c) release of the device membrane from the substrate[84].

This significantly limits the options for choice of the material stack as the sacrificial layer should be matched as closely as possible to the epilayer and the substrate, to avoid defect formation. For III-V semiconductors, lattice matched sacrificial layers such as AlAs (Aluminum arsenide) or AlInP (Aluminum indium phosphide) for GaAs[87], and InGaAs (Indium gallium arsenide) or InAlAs (Indium aluminum arsenide) for InP (Indium phosphide)[95], are commonly used, enabling high quality epilayer. In case of III-N materials, dissimilar sacrificial layers are generally employed since most lattice matched III-N alloys have very similar etching selectivity, making them unsuitable for ELO process. Layers such as ZnO (zinc oxide)[88,96], AlN (Aluminum nitride)[97,98], Ga_2O_3 (Gallium oxide)[99], SiO_2 (Silicon oxide)[100–102], and CrN (chromium nitride)[103] have been demonstrated for the successful release of GaN (Gallium nitride) epilayers. Although, this makes the growth of epi-stack more challenging and can cause the formation of defects in the epilayer, it enables the application of ELO for III-N semiconductors.

The second major criteria, for the choice of the sacrificial layer, is the etching selectivity. To successfully perform ELO, the sacrificial layer needs to manifest a significantly higher etching rate in the solution of choice compared to the epilayer and the substrate. This allows us to under-etch and release the epilayer from the substrate without its degradation. Thus, appropriate combination of sacrificial layer/etching solution needs to be identified. For example, both AlAs/HF (hydrofluoric acid) and AlInP/HCl (hydrochloric acid) sacrificial layer/etching solution combinations have been successfully used for ELO of GaAs-based FSMs. The use of AlAs/HF causes the formation of residues and high roughness of the

surface of the released membrane as well as the substrate. On the contrary, by using AlInP/HCl, a clean and smooth surface of the FSM and substrate can be obtained, enabling the prospect of the substrate reuse. Similarly, InP-based FSMs can be obtained using InGaAs sacrificial layer and either HF/H_2O_2 (Hydrofluoric acid/Hydrogen peroxide)[104] or H_3PO_4/H_2O_2 (Phosphoric acid/Hydrogen peroxide)[95] etching solutions. Alternatively, InAlAs can be used as the sacrificial layer, providing improved etching selectivity compared to InGaAs[105]. In every case, a suitable combination of sacrificial layer and etching solution is necessary to allow successful ELO process while preserving the quality of the FSM.

Another common challenge of the ELO is the long time necessary to chemically etch and release the epilayer. Although small samples can be released relatively quickly, at wafer-scale the lift-off process can take from a few hours to a few days, depending on the surface area and specific sacrificial layer. This imposes impractical limitations on the large-volume production and wide industrial adoption of ELO. To face this challenge several approaches are being developed.

To accelerate the chemical etching process, various micro/nanopatterned sacrificial layer structures can be used. These nano/microstructures are produced using various methods including selective area epitaxy, photolithography and dry etching or electrochemical etching[98,106–108]. The presence of the nano/microstructures in the sacrificial layer increases the surface area that can be etched and facilitates the wet etching of the sacrificial layer (Figure 2-4b-c). In some cases, the presence of the nano/microstructure can also improve the quality of the epilayer by reducing the quantity of dislocations, especially in case of growth on dissimilar materials, as it is the case for GaN.

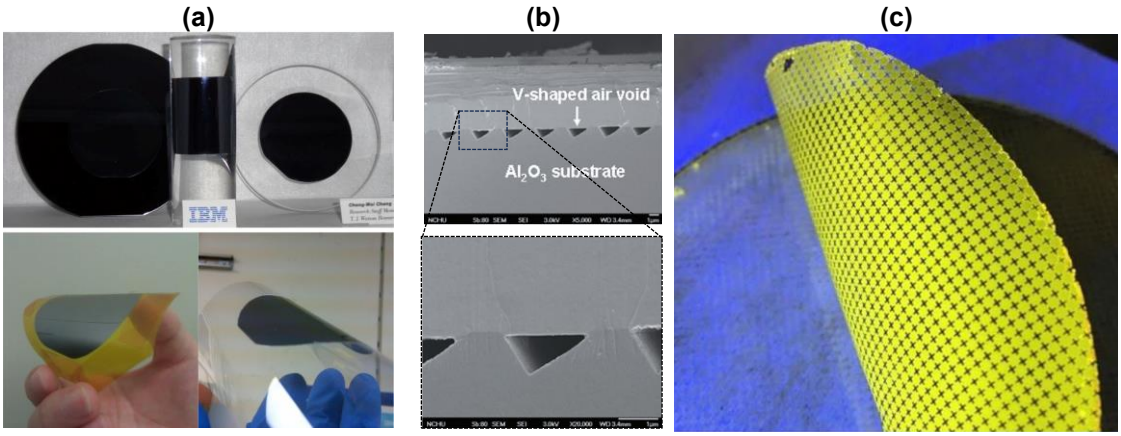

Figure 2-4: (a) (top) Demonstrations of the transferred GaAs thin films to the rigid substrate (from left, GaAs on 100 m Si wafer, GaAs on curved solid object, GaAs on glass) and (bottom) flexible substrates[84] (b) An LED epitaxial layer was grown on the patterned sapphire substrate with V-shaped air channels enabling faster layer under etching[98] (c) Photograph under UV illumination of full 100 mm GaN membrane release using ELO and layer perforation[106].

Alternatively, multiple stacks of sacrificial layer/epilayer can be grown on top of each other to produce multiple FSMs during single etching step[109]. Although, this approach increases the throughput of the method, it brings additional challenges such as the compatibility of the top epi-stack layer with growth of second sacrificial layer, as well as the FSM handling issues, since only the topmost epilayer of the stack can be bonded on the handle substrate before the lift-off process.

While ELO of various materials have been demonstrated, its wide adoption is still limited. For instance, the ELO of III-N compound semiconductors is still in the early stages of development and its commercial application has not been proven yet. In case of III-V semiconductor FSM, the ELO has been researched over many years, and it's now well developed for commercial applications, especially in high-efficiency III-V solar cells. However, it's still limited to niche markets, namely space photovoltaic, due to the high cost of the process. This is mainly due to slow FSM release by wet etching as well as expensive chemical mechanical polishing (CMP) of the substrates, necessary for their reuse and production of multiple FSMs.

Although, Ge has similar lattice parameters to GaAs and can be grown on top of the same AlAs sacrificial layer, these two materials are rarely grown in the same chamber, due to the cross contamination and residual doping between Ge and III-V layers. Moreover, Ge presents lower etching solution resistance and lower etching selectivity in acidic aqueous etching solutions[110–112] compared to GaAs. This is due to the presence of various unstable Ge suboxides, which can be easily etched even by water, causing partial dissolution of the Ge layer during the lift-off process. Consequently, this makes the obtention of high-quality and large surface Ge FSMs by ELO very challenging task, due to the long exposure to the etching solution.

2.1.2 Laser Lift-Off

In previous part, the ELO process has been discussed, showing its success especially for III-V materials. However, wet chemical etching, involved in ELO, often results in partial damage to the epilayer, which is being released. Finding a chemical etching solution that is completely non-reactive with the epilayer while maintaining a high etching rate for the sacrificial layer is an extremely challenging task. This is further made difficult by the extended etching duration of multiple hours required by ELO to release wafer-scale FSMs, imposing a limitation for fast production. Consequently, various “dry” lift-off techniques are explored to reduce the damage induced by wet etching and to accelerate the layer release. Like ELO, the laser lift-off (LLO) is based on monolithic heterointegration by epitaxy. However, instead of sacrificial layers and wet etching, LLO uses the difference in laser light absorption between the substrate and the epilayer. This generates localized heat at the interface, melting/decomposing the material near the interface, thereby separating the epilayer from the substrate (Figure 2-5)[113–116].

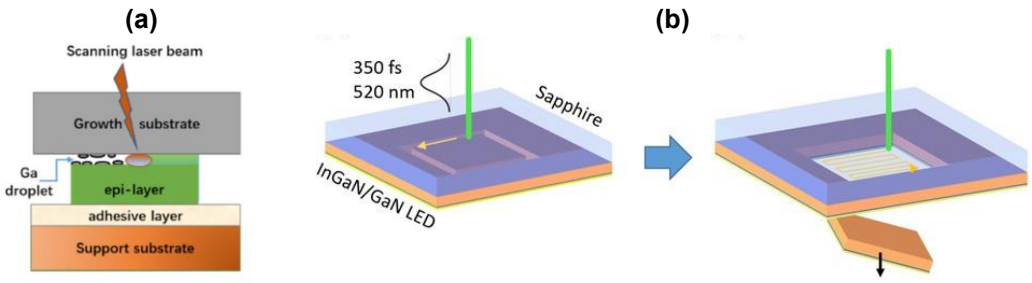

Figure 2-5: Schematic illustration of (a) laser lift-off process, and of (b) selective area membrane release by LLO[113,114].

A typical application of LLO is the release of GaN epi-structures grown on sapphire to support the substrate. GaN epilayer has a band gap of ~3.3 eV, compared to the sapphire's band gap of ~9.9 eV. This makes sapphire transparent to short-wavelength laser light, which is, on the other hand, absorbed by GaN epilayer generating heat. The localized heat at the interface sapphire/GaN causes the decomposition of the GaN into Ga droplets and nitrogen gas, enabling the release of the epilayer[117–120]. This membrane can be then transferred on various support substrates including Mo (molybdenum)[121], GaAs or flexible polydimethylsiloxane (PDMS)[122]. Initially this technique was limited to production of 50 mm GaN FSM wafers, but recently it was also demonstrated at 100 mm scale[123–125].

The major limiting factor of LLO on large surfaces is the formation of cracks in the epilayer, induced by thermal strain relaxation due to the local heating by laser. This effect can be reduced by using a heating plate during the LLO process to reduce the thermal strain and avoid the formation of cracks. Another important parameter affecting the laser-induced damage is laser spot size[123].

The LLO process can be used for local detachment of small devices as well as the entire 100 mm wafers, and the entire process of the release takes only a few seconds. However, to obtain defect-free FSM by LLO, the beam quality of the laser must be well controlled to avoid damage to the epilayer. Another disadvantage of the LLO is the overall cost of the tools limiting its availability for regular use. Finally, the necessary difference in optical

properties of the substrate and epilayer limits the use of LLO to only a few structures such as GaN on sapphire.

2.2 2D-assisted epitaxy and transfer techniques

Compared to conventional heteroepitaxy, during 2D-assisted epitaxy, only weak Van der Waals (VdW) bonding is formed between the substrate and the epilayer, due to the presence of the 2D material at the interface, creating a weak VdW gap at the heterointerface (Figure 2-6)[85]. This lack of covalent bonding between the epilayer and the substrate prevent the accumulation of the strain in the epilayer during the growth, and enables its elastic relaxation without the introduction of the defects[126], allowing the even growth of highly mismatched systems or layers with completely different lattice symmetries from the substrate[62]. Moreover, the VdW bonding provides a weak interface with low adhesion, which is ideal for the detachment. Applying force to the epistructure, grown by 2D-assisted epitaxy, causes the detachment of thin epilayer from the 2D material substrate, enabling the formation of semiconductor FSMs[127].

The weakly bonded VdW heterointerface also brings new challenges for the epitaxial growth. In general, 2D materials have a low surface energy, making the epitaxial nucleation process very difficult. Moreover, the lack of covalent bonding with the substrate complicates the crystal orientation of the epilayer, as it depends only on weak interactions in case of 2D-assisted growth. To harness the potential of this approach, two growth techniques called (Quasi-)Van der Waals epitaxy (VdWE) and remote epitaxy (RE) has been introduced[62,127].

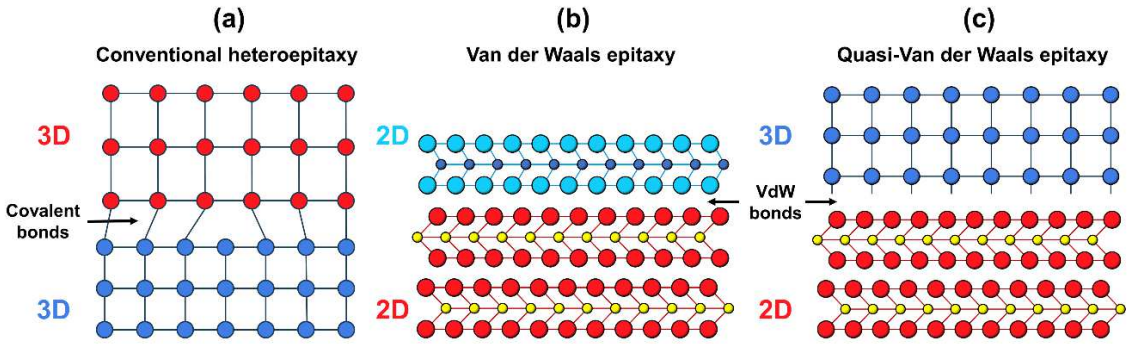

Figure 2-6: Schematic illustration of (a) conventional heteroepitaxy, (b) purely Van der Waals epitaxy 2D/2D, and (c) Quasi-Van der Waals epitaxy 3D/2D.

2.2.1 (Quasi-)Van der Waals epitaxy

The concept of VdWE has been first introduced in 80s by demonstrating the growth of crystalline MoS_2 on $NbSe_2$ using VdW interactions[128]. However, it gained lots of popularity last decade, thanks to the discovery and advancements in development of high-quality graphene and other 2D materials[81,129–133]. The VdWE provides a direct heterointegration road for fabrication of 2D/2D VdW heterostructures including highly mismatched materials. For example, previously mentioned epi-stack MoS_2 on $NbSe_2$ represent a lattice mismatch of around 10%, but still enables a high-quality growth of materials. However, this is true for the growth of 2D/2D heterostructures. The direct integration of 3D massif semiconductors on 2D substrates and vice versa, is more complex as the interactions at the heterointerface are not purely VdW and also involve the dangling bonds of the 3D material interacting with 2D VdW interface. In this case, we talk about Quasi-Van der Waals epitaxy (QVdWE). Despite this difference, the QVdWE structures maintain similarly weak VdW interface enabling the separation of the epilayer from the substrate.

Fabrication of 3D semiconductor FSMs using QVdWE has been demonstrated for the first time on AlGaN/GaN LED structures grown on single-crystal hexagonal Boron Nitride (hBN) interlayer[126]. The AlGaN buffer used as a seeding layer for growth of GaN on hBN (Figure 2-7a). The final GaN LED structure is then transferred on metallic indium sheet to fabricate first FSM-based LED as shown in Figure 2-7b. This process is later scaled

up to 50 mm wafer, thanks to the development of a large surface, high-quality hBN monolayer (ML) growth[134], and it is also demonstrated on other III-N materials[135]. The QVdWE has been also used for growth of various oxide compounds such as ZnO, MoO_2, $CoFe_2O_4$, Fe_3O_4, $PbZrTiO_3$, VO_2[67–73]. Similarly, an effort was made also to produce FSMs of III-V[136] and group IV[137,138] materials using QVdWE. Although, an improved nucleation on graphene surface either by initial adsorption of gallium (Ga)/arsenic (As) layer on the surface for growth of GaAs(Figure 2-7c), or ozone (O_3) treatment of the graphene for growth of Ge (Figure 2-7d), the final epilayers resulted in polycrystalline 3D structures due to the lack of interactions enabling uniform crystal orientation. This challenge has been later resolved for III-V materials by the introduction of remote epitaxy.

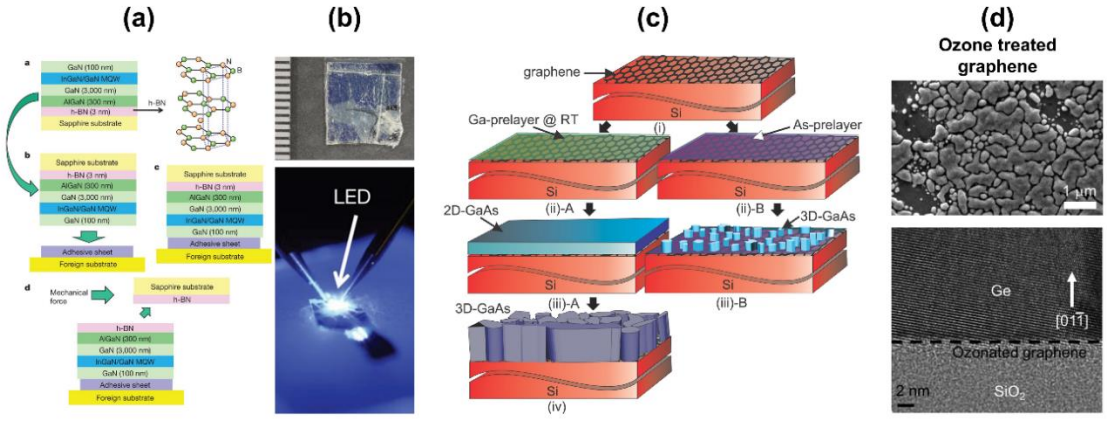

Figure 2-7: (a) Schematic illustration of the multiple quantum well LED materials design, release and transfer process[126], (b) optical image of the transferred structure (top) and of the transferred blue LED (bottom) produced by QVdWE[126] (c) Schematic illustration of the growth of GaAs on graphene covered Si via QVdWE[136] (d) SEM image of the Ge crystals grown on ozone treated graphene (top) and corresponding TEM image of the Ge crystal.

2.2.2 Remote epitaxy

Recently in 2017, a new technique called Remote Epitaxy (RE), based on QVdWE, has been introduced[62]. It was shown that single-layer graphene is transparent to the ionic field of the crystalline substrate underneath, which can be used for nucleation and orientation of the epilayer[63]. This allows maintaining a coherent interaction between the

epilayer and the substrate, enabling the growth of the substrate oriented, monocrystalline layer despite the presence of graphene interface. The growth by ionic interactions through graphene interlayer was first experimentally demonstrated on GaAs epilayer grown on graphene covered GaAs substrate (Figure 2-8a)[62]. These observations were later supported by theoretical simulations of the ionic interactions at the graphene surface[63]. Furthermore, recent studies have suggested that the presence of native oxides beneath the graphene can induce the formation of pinoles within the graphene interface, helping the orientation of the epilayer[139], in addition to remote polar interactions through the graphene.

RE has been demonstrated at wafer-scale, enabling the production of large single-crystalline FSMs. Since its discovery, the use of RE have been broadened to a variety of III-V (InP, GaP, etc.), III-N (AlN, GaN, etc.)[140] and complex oxide[66,141] materials (Figure 2-8b). Moreover, multiple substrate reuse[142,143] and high throughput multi-FSM stack production[143] have been investigated (Figure 2-8 c-d), making RE a promising alternative to ELO for production of III-V and III-N FSM.

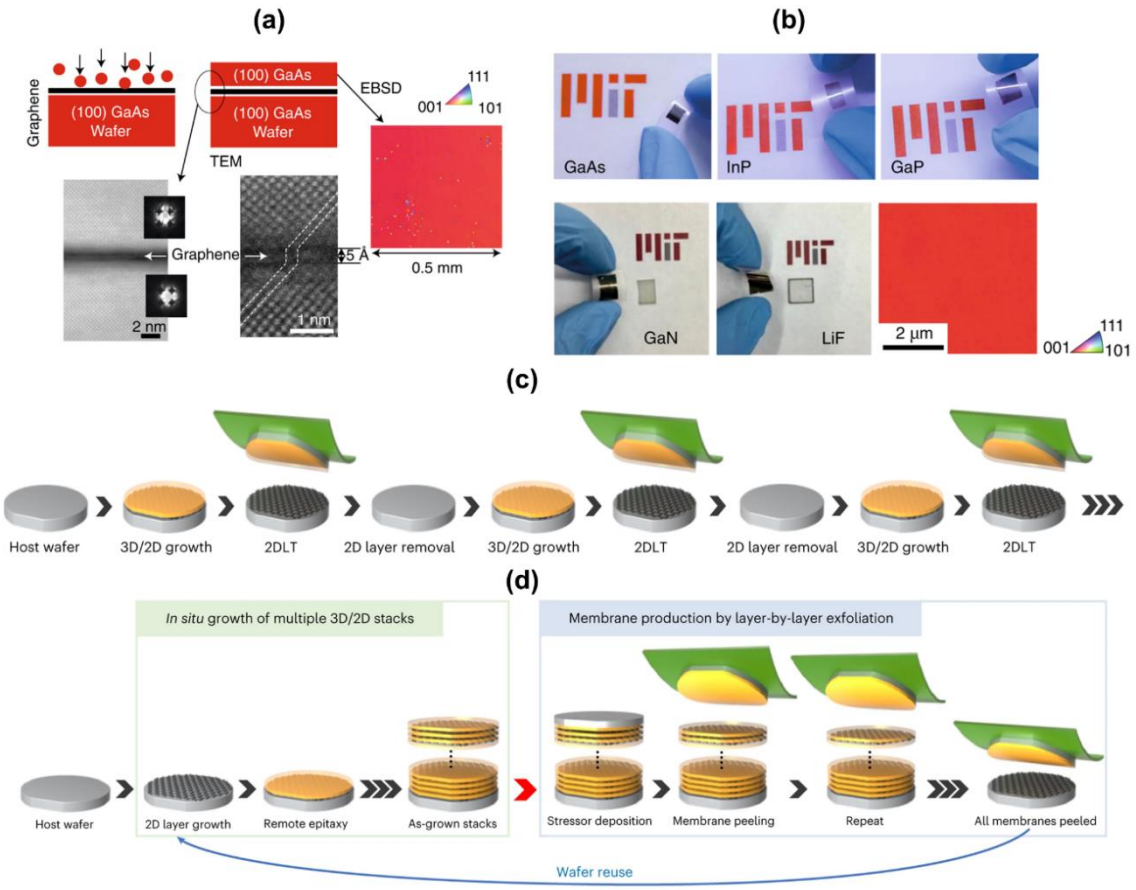

Figure 2-8: Remote epitaxy of different materials. (a) Schematic illustration of the RE growth, Transmission electron microscopy (TEM) image of the GaAs/Graphene/GaAs interface and Electron Backscatter Diffraction (EBSD) of the exfoliated GaAs surface. (b) Optical images of the FSM obtained by RE, including GaAs, INP, GaP, GaN and LiF, and typical EBDS of the transferred FSM showing monocrystalline nature of the membranes obtained by RE. (c) Schematic illustration of the substrate reuse after RE (d) Schematic illustration of the single-crystalline FSM production process using RE by direct growth of multiple stacks of 3D/2D layers and layer-by-layer exfoliation[143,144].

Nevertheless, the success of RE growth relies on the polarity of the substrate and the epilayer. Consequently, it is impractical for applications involving non-polar materials such as Si and/or Ge. Both growth of Ge/Si epilayers and growth on Ge/Si substrates using graphene interlayer have resulted in the formation of polycrystalline epilayer without any crystal alignment between the substrate and epilayer[63,145]. This is due to the lack of ionic interaction through graphene interface caused by the non-polar bonding nature of Ge and Si. The ionicity of the substrate is a crucial factor for good epitaxial growth by RE,

since it determines the thickness of the graphene interface through which the substrate can interact with the epilayer. For example, in case of GaAs (30% ionicity), GaN (50% ionicity) and LiF (90% ionicity) this thickness is 1, 2 and 3 ML of graphene respectively (Figure 2-9). This remains the main limiting factor of the RE and it is the reason why RE cannot be used for growth of non-polar materials such as Si, Ge and other group IV alloys.

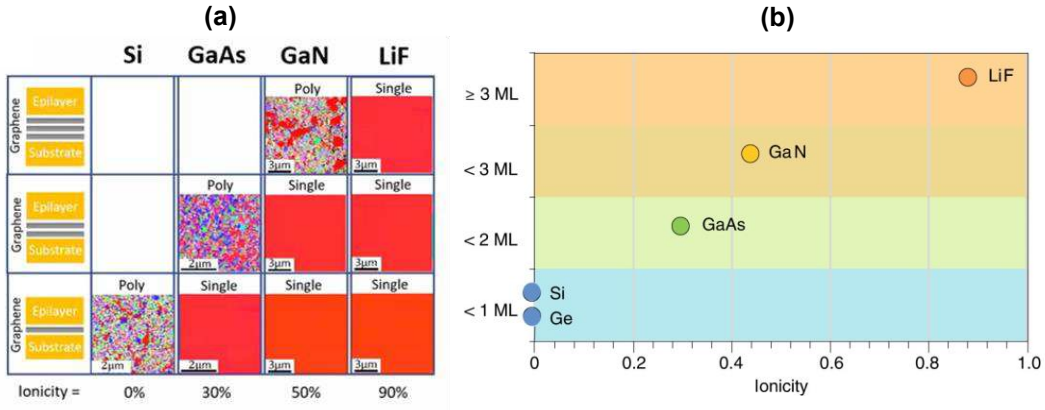

Figure 2-9: (a) EBSD characterization of various material FSM grown on increasingly thicker graphene interlayer. (b) Plot of graphene thickness vs. material ionicity, showing maximal thickness of the graphene interlayer for each material[144].

2.2.3 Remote epitaxy vs. Quasi-Van der Waals epitaxy

Although, RE and QVdWE have a lot in common, their main difference is the nature of the interactions defining the crystalline orientation of the epilayer. While the QVdWE depends mostly on the direct interaction between the 2D interface and the epilayer, the RE relies on the ionic interactions between the bulk substrate and epilayer through the 2D interface. This makes the choice of 2D interface for successful RE very important, as using ionic 2D materials such a crystalline hBN interfere with the ionic interactions between the bulk substrate and the epilayer[63]. Indeed, various studies on polar 2D materials such as hBN[126] or MoS_2[146], have shown that their polarity affects the crystalline orientation and the nucleation density of the 3D material during the growth.

The relation between the RE and the QVdWE has been further studied on GaN growth using increasingly thicker interlayers of hBN and graphene to elucidate the influence of the 2D interface[63]. Due to graphene's non-polar nature, it allows coherent ionic interactions

between the bulk substrate and epilayer through up to 2 ML thick interlayer (for GaN), resulting in monocrystalline substrate oriented epilayer (Figure 2-10a). For interlayers of 3 ML and thicker, these ionic interactions become too weak to orient the epilayer, causing difficult nucleation and random oriented seeds on the surface of the graphene, and leading to a polycrystalline epilayer. On the other hand, by using the polar hBN interlayer a competition between the ionic interactions of the bulk substrate and of the 2D interlayer results in polycrystalline epilayer (Figure 2-10b). As the thickness of hBN increases, the bulk substrate's interactions with epilayer get weaker, resulting in increasing orientation of the epilayer along the hBN interlayer. Eventually for hBN interlayers of 3 ML and thicker, the epilayer becomes perfectly monocrystalline, following hBN interlayer. These results show that both the bulk substrate's and 2D interlayer's nature as well as the thickness of the 2D interface play an important role in the final growth mode (QVdWE or RE). While polar substrates and non-polar interlayers promote RE growth mode, it can be easily hindered by the thickness of the 2D interlayer. In case of the QVdWE, a high nucleation density and good quality of the epilayer are promoted by increasing the polarity of the interlayer. Other aspects such as the quality of the 2D material can also play an important role during the growth on 2D interlayers. Any defect and contamination present on the 2D interface can result in random nucleation sites, leading to polycrystalline epilayers[145].

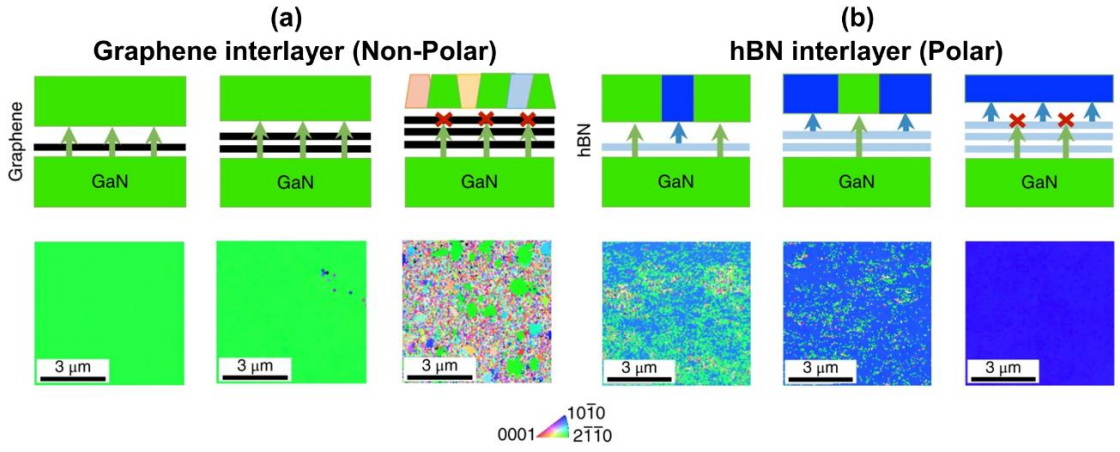

Figure 2-10: Schematic illustration (Top) and EBSD analysis (bottom) of the exfoliated GaN surface grown of varying numbers of monolayers (ML) of (a) hBN: 1 ML/h-BN (left), 2 ML/h-BN (middle) et 3 ML/h-BN (right), and (b) graphene: 1 ML/Graphene (left), 2 ML/Graphene (middle) et 3 ML/Graphene (right)[63].

Both VdWE and RE have shown tremendous potential for fabrication of FSMs and much of research is focused on better understanding and improvement of these methods. Today, they are mostly used for growth of high-quality 2D materials on semiconductor substrates and single crystal 3D membranes of polar materials. Their applications on non-polar 3D materials (e.g., Si and Ge) remain a challenge since the lack of interactions between the epilayer and 2D interlayer/substrate makes them incompatible with such materials.

To overcome this limitation, recent studies focus on defect engineering and nanopatterning of the 2D interface, enabling direct link between the substrate and epilayer, while maintaining most of the epilayer's surface weakly bonded to the 2D interface[139,147,148]. This solution to the limitations of 2D-assisted epitaxy is further explored in the Chapter III of this manuscript, focusing on the use of nanoengineering of the graphene interlayer to improve nucleation of non-polar 3D materials on top, while allowing the substrate orientation of the epilayer and growth of monolithic single crystalline FSMs of group IV semiconductors.

2.3 Mechanical layer release by substrate engineering

Alternatively, to both conventional and 2D-assisted epitaxial techniques, the formation of FSMs can be achieved through a variety of substrate engineering methods combined with mechanical release. These methods include controlled mechanical spalling, Smart cut technology, and nanostructured layer release. In all cases, the process is based on formation of mechanically weak interface below the surface of the substrate, enabling the layer separation of the membrane when mechanical force is applied.

2.3.1 Controlled mechanical spalling

Controlled mechanical spalling is a method to separate semiconductor membranes by inducing mechanical fractures in the substrate at room temperature. This is achieved by the deposition of a stressor layer on top of the substrate creating a crack at an equilibrium depth below the interface[149,150]. To achieve controllable fractures and uniform membrane transfer a flexible handle layer is attached on top of the stack. A small force is then applied on the handle, to mechanically guide and propagate the crack, resulting in separation of the portion of material from the substrate[149]. The entire process is illustrated by Figure 2-11a-c. Controlled spalling has been studied for many years and now it's possible to use it for wafer-scale transfer of variety of materials such as Si[151,152], Ge[153,154], GaAs[155], InP[156] and GaN[157]. The process can also be used for release of complete device structures, leading to a wide range of flexible devices, namely high efficiency solar cells[39,158–160], LEDs[161], CMOS[162,163], etc. Some examples of spalled membranes and examples of flexible circuits are shown in Figure 2-11d-g.

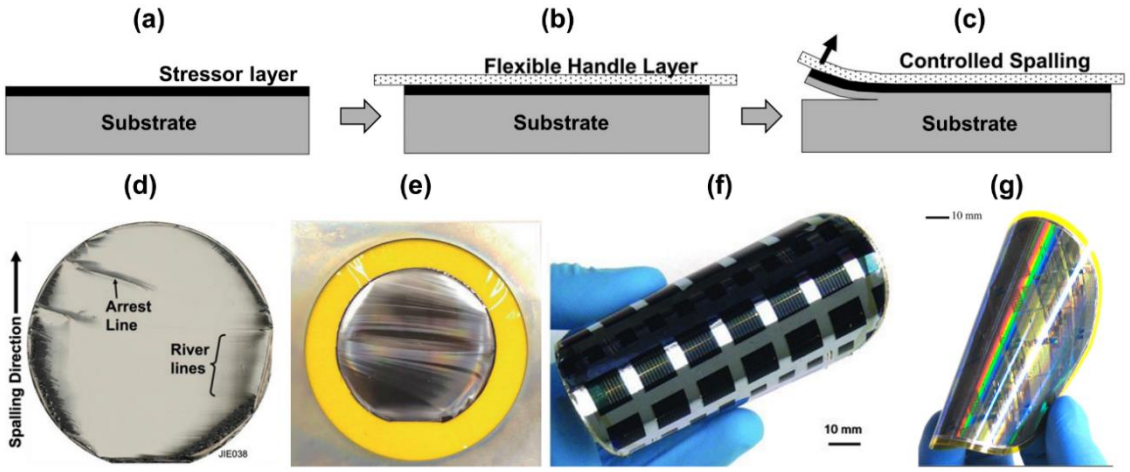

Figure 2-11: Schematic illustration of controlled spalling. (a) Deposition of the stressor layer with conditions avoiding spontaneous fractures, (b) Application of the flexible handle, (c) controlled propagation of the fracture using the handle[150]. Optical image of (d) 100 mm Ge membrane[160] and (e) 50 mm GaN membrane[161] obtained by controlled spalling. Photographs of post-spalling (f) 100 mm flexible InGaP/(In)GaAs tandem solar cells on plastic[158], and (g) thin SOI integrated electronic circuits[162].

One major disadvantage of controlled spalling is the fracture depth (thickness of transferred membrane). Although, it is possible to control the fracture depth by a variety of factors such as choice of stressor material and its thickness as well as the nature of the substrate materials. The accurate control of the final membrane remains a very challenging task[153]. Moreover, resulting membranes are in order of tens of microns thick, with the thinnest layers being around 10 µm. Another challenge for mechanical spalling is the fracture interface. In general, this interface is formed by crystal faceting with a height of few microns, causing high surface roughness as shown in Figure 2-12. The faceted surface is mainly concerning for the substrate reuse as the successful reconditioning necessitate either costly CMP treatment or chemical etching combined with epitaxial planarization to enable the formation of a new high-quality membrane from the same parent substrate[39,164]. While spalling offers an interesting pathway for the device detachment at wafer-scale and weight reduction, the high membrane thickness limits its use for the substrate production and device thinning.

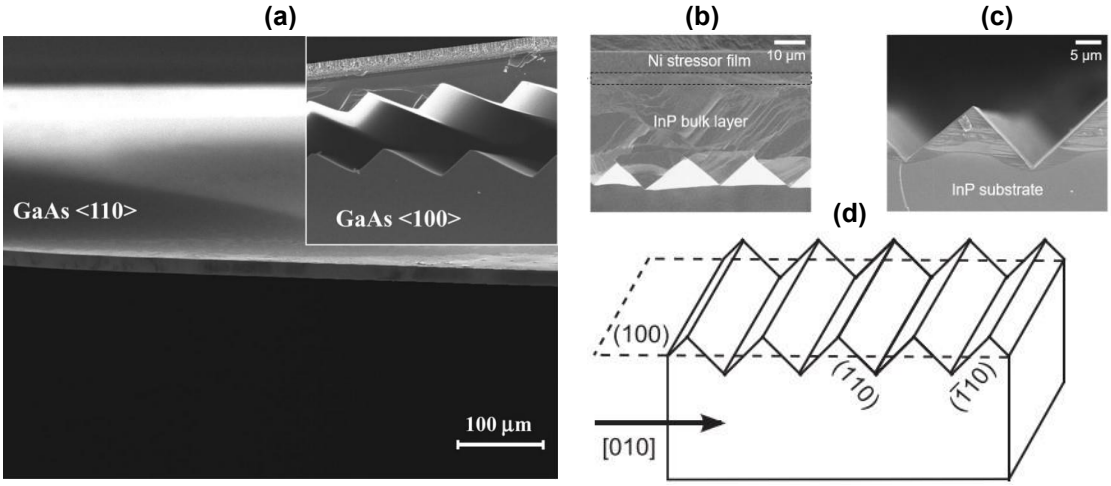

Figure 2-12: SEM micrographs of spalled (a) (110) and (100) GaAs surfaces and (b-c) InP surface[156]. (d) illustration of faceting after spalling of (100) InP and GaAs substrates[155].

2.3.2 Smart Cut process

The Smart Cut process technology is best known as a technique of manufacturing silicon-on-insulator (SOI) wafers (Figure 2-13), but later it was also adapted to other materials[165]. In this process, a thin membrane is transferred from the surface of a donor silicon substrate to another target silicon substrate. First, a silicon oxide (SiO_2) layer is formed on at least one of the silicon wafers. This layer will become the insulator separating the membrane from the substrate at the end of the process. The donor substrate is then submitted to implantation of hydrogen or helium ions. Both substrates are cleaned, mechanically bonded

by weak VdW forces and annealed[166]. During the annealing, a covalent bonding is formed between the surfaces, linking both substrates together. At the same time, microcavities are formed at implantation depth with highest ion concentration enabling to form splitting interface, during annealing of the structure, and separating the donor substrate from the SOI structure[167]. This substrate can be then repolished by CMP and reused for further production. Moreover, this process has been scaled at 200 mm and 300 mm wafer-scale, making it very lucrative for industrial applications.

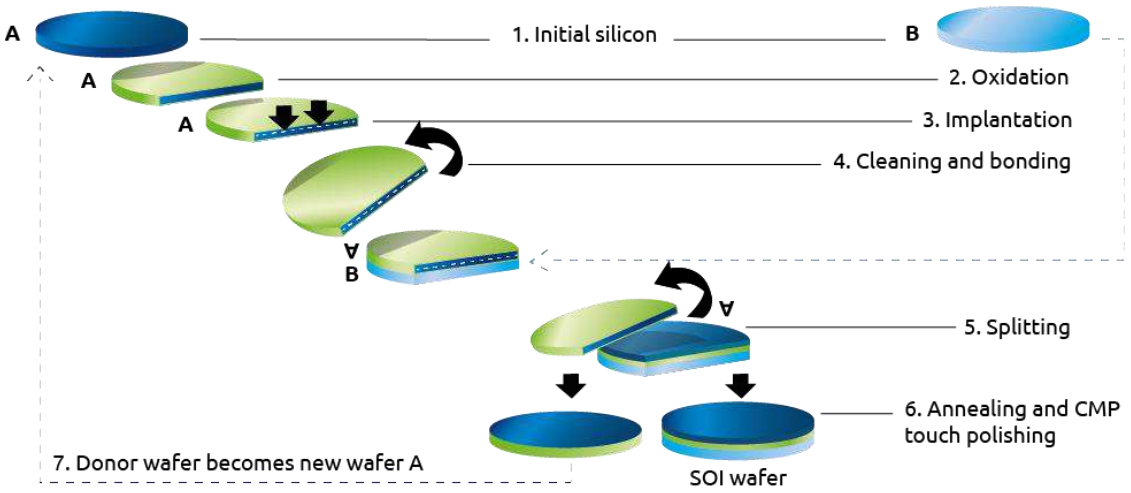

Figure 2-13: Schematic illustration of the SOI Smart cut process including wafer oxidation, ion implantation, cleaning and bonding to target substrate, releasing of the layer, polishing of the final layer and substrate reuse[168].

Similarly, Smart Cut technology has been adapted on a variety of materials such as GaAs[169], InP[165], Ge[170,171], SiC (Silicon Carbide)[172], GaN[173–176], or AlN[177], by switching the donor substrate to wafer of given material. Furthermore, the final properties of the membrane, e.g., crystalline orientation, doping, offcut, can be adjusted directly by choice of donor substrate. The membrane can also be transferred on a variety of other substrates than Si[178]. For example, InP have been already successfully transferred on GaAs, Sapphire, or Ge[165]. This offers the versatility of feasible structures.

Unlike Si, commercially available wafer sizes are much more limited for other materials. For instance, GaAs and InP are produced in maximal size of 150 mm and 100 mm, respectively, limiting the industrial scalability. To tackle this challenge a novel technique for pseudo-donor substrate has been developed. This approach is based on the preparation of smaller tiles from commercially available substrates. They are then fixed on the handle substrate in size of 200 mm or 300 mm to create a much larger pseudo-donor substrate, which can be then used for Smart Cut process (Figure 2-14a-b). This has been demonstrated on InP at 200 mm scale (Figure 2-14c-d).

In case of GaN, an alternative splitting method is being studied. Instead of ion implantation and annealing, an exposure to a laser beam is being used to induce micro

cavities in the substrate, enabling the separation of the membrane from the donor substrate. This is achieved on a similar promise as the LLO. A laser is shined at GaN layers causing a formation of microcavities, due to the GaN decomposition, enabling the formation of cracks and separation of the layer[179].

Smart Cut is a well established and commercialized process, allowing formation of membranes with thickness ranging from 0.2 µm to 1.0 µm. However, its successful application necessitates the availability of the material in substrate form, significantly limiting its application to few materials and reducing its potential as a universal transfer method of semiconductor membranes. Moreover, its substrate reuse relies on costly CMP process, raising the final price of the fabricated membrane. Nevertheless, Smart Cut technology has found an industrial/commercial success in case of materials such as Si, Ge, GaAs, InP, GaN and SiC.

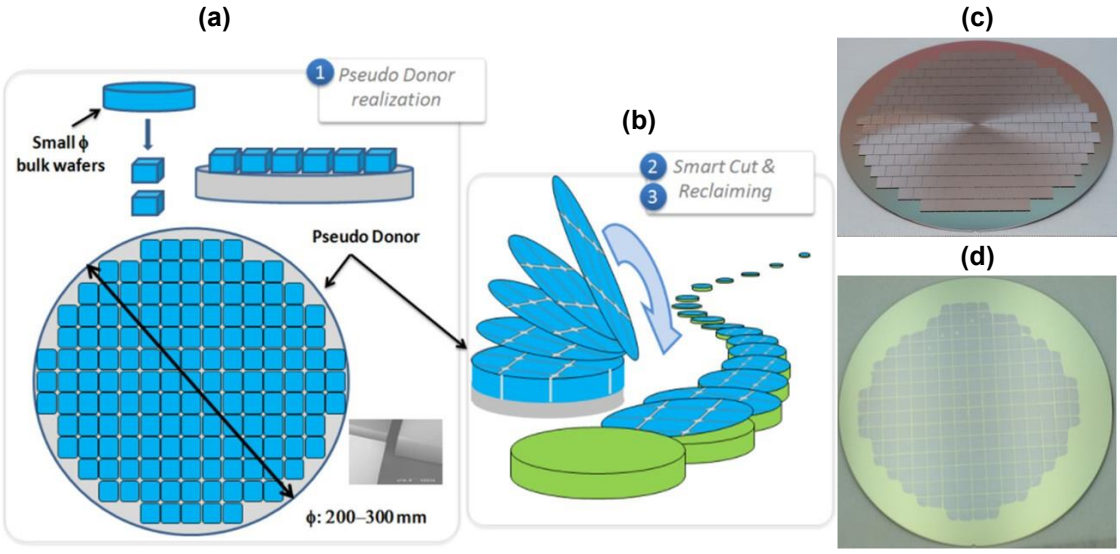

Figure 2-14: Schematic illustration (a) of the donor substrate preparation using tiling technique and (b) of its use in Smart Cut process. Optical images of (c) 200 mm InP tile pseudo-donor substrate and (d) its membrane transferred on Si substrate[165].

2.3.3 Layer release through nanostructured substrates

Another approach for FSMs fabrication is the use of nanostructured interface between the substrate and the membrane. This nanostructure serves as the membrane support during the fabrication process of devices, as well as a fragile interface facilitating the mechanical separation of the membrane from the substrate, thus limiting the formation of defects compared to mechanical spalling.

Silicon-on-Nothing (SoN) has been developed as an alternative to SOI produced by Smart Cut technology[180]. This SoN is based on the microstructure transformation of the Si to form large voids beneath the surface, enabling the detachment of the membrane (Figure 2-15)[180,181]. First an array of macropores is formed by lithography and dry etching. The voided layer underneath the surface is then obtained by high temperature annealing of the microstructure. Later, this technique has been adapted to Ge, allowing the production of Ge FSMs[182,183]. Although this approach enables perfect control of the microstructure, and it is easily scalable on large size wafers, the use of other nanostructuring techniques can reduce the complexity as well as the price of this FSM fabrication process. One such a technique is electrochemical etching (EE), enabling the formation of porous nanostructure on the surface of the semiconductor wafers.

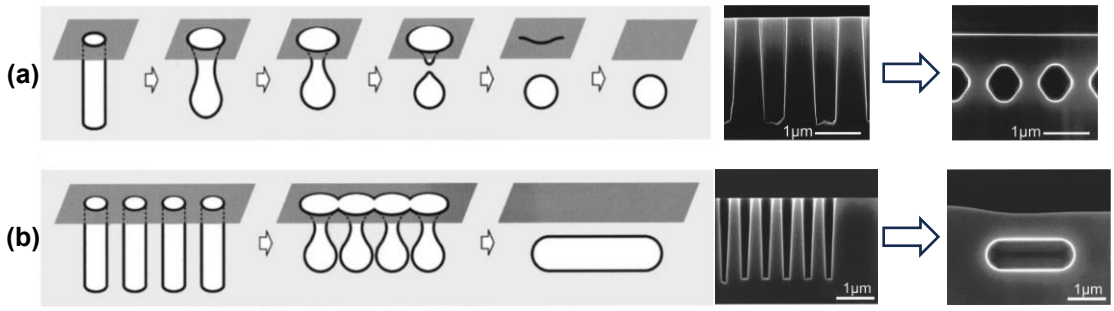

Figure 2-15: (a-b) Schematic illustration and SEM images of the thermal transformation of two different macropores structures in Si resulting in voids trapped beneath the surface[180].

Electrochemical porosification is a well-established method, and extensively studied the process in case of Si substrates. By applying an electrical bias on Si in electrolytic solution, pores are etched into the Si crystal. Formation of porous structures of other materials such

as GaAs[184–188], SiC[189–192], GaN[193–199], InP[200–202], Ge[203–205], etc., has also been demonstrated using EE. Although, the main principle of the porosification by EE remains the same, the specifics of the process vary depending on the material. For instance, in case of Ge the EE process is more complex than for Si, as the application of unipolar bias results in continuous dissolution of already formed PGe layer or even in complete dissolution of the Ge surface (e.g., Electro polishing) at current density[204]. In order to obtain porous structure in Ge, a bipolar EE (BEE) has to be used, where applications of the positive bias enable the etching of the PGe and the following negative bias forms a passivation layer around the pores, effectively protecting them from further dissolution[206–208]. Although, various PGe morphologies and double-layered structures have been demonstrated[205,209–213], the main challenge remains in fabrication of homogenous PGe layers over large surfaces. Moreover, destructive SEM observations are mainly used for the characterization of PGe structures, leaving space for the development of non-destructive quality control techniques. For these reasons, Chapter IV focus on fabrication of high-quality PGe layers, with tunable physical properties at wafer-scale. Additionally, fast feedback, non-destructive characterization techniques are introduced for quality control of produced PGe structures.

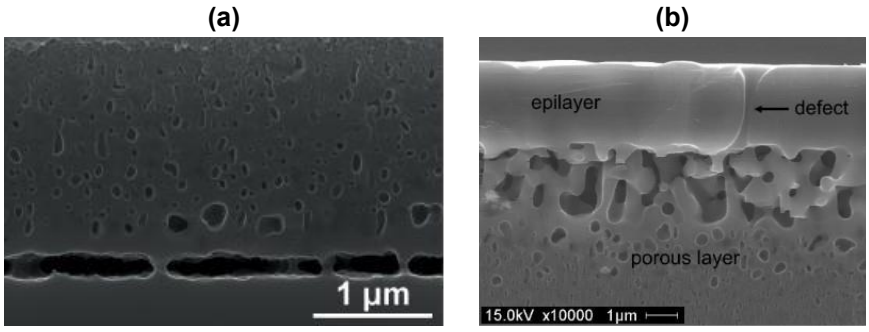

Figure 2-16: (a) SEM image of reconstructed double layered PGe structure after annealing[214] (b) SEM image of 4H-SiC epilayer grown directly on porous SiC substrate, demonstrating partial reconstruction[215].

Despite the challenges with the formation of uniform PGe, a successful formation of Ge membrane has been demonstrated[214,216]. Similarly to other materials, this is in general achieved by high temperature annealing of multilayered PGe structures, resulting in not

fully densified membranes with encapsulated voids inside (Figure 2-16a)[214,216–218]. Alternatively, the membrane can be grown directly on the porous substrate, producing high quality membrane, but usually also resulting in at least partial of the porous structure reconstruction into larger pillars (Figure 2-16b)[215,219–222]. The thermal stability of the porous substrates plays an important role as it needs to maintain its structure to enable the formation of the membrane on top, encapsulating the microstructure at the interface. This is particularly challenging in case of the PGe layers which demonstrate very low thermal stability and rapidly reconstruct at temperatures above 400 °C[223]. For this reason, The Chapter V explores the low temperature growth on non-reconstructed PGe substrates and discuss the growth mechanisms as well as the formation of fully densified, high-quality membranes.

Similarly to mechanical spalling and smart cut technology, the substrate recovery is also a challenging task in case of nanostructured substrates. After the detachment, the part of the nanostructured interface remains on the substrate's surface, causing high surface roughness and making it unsuitable for direct substrate reuse. To successfully reuse the substrate the reconditioning process is necessary to eliminate the remnants of the nanostructure on the surface. This can be accomplished using costly CMP techniques as in case of other mechanical release methods[224]. Alternatively, a wet chemical etching can be used, taking advantage of the anisotropic etching of the nanostructure features on the substrate's surface compared to the bulk material, which enables an efficient flattening of the surface[225,226]. This has been demonstrated on Si substrate reuse, using either KOH etching solution with etching rates of few µm/min. A single substrate has been reused up to 14 times before breaking[225]. However, in both cases an etching of a substantial thickness of the substrate (few µm) was necessary to flatten large features of the nanostructure remaining on the surface, wasting a non-negligible amount of the material, and reducing the possible number of reuses. Moreover, a slight degradation of the membrane's surface quality has been observed with each cycle. To tackle this issue, Chapter VI focus on the possibility to minimize the amount of etched material, while enabling an efficient reconditioning of the substrate by using unreconstructed PGe layers.

2.4 Conclusions

This chapter reviews the state of the art of techniques used for FSMs fabrication. It introduces their basic principles, advances, advantages, challenges, and opportunities. 2D-assisted epitaxy and layer release through nanostructured substrates are identified as promising techniques for fabrication of group IV semiconductor FSMs. 2D-assisted epitaxy presents a new but rapidly advancing branch of research on FSMs fabrication. However, it's one of its main limitations is the growth of non-polar materials due to the lack of interaction with the substrate. To face this issue Chapter III of this thesis introduces a novel approach based on substrate engineering of the 2D interface enabling the growth of non-polar materials by 2D-assisted epitaxy.

On the other hand, layer release through nanostructured substrates is relatively well-established method especially in case of the Si. However, its application on other materials, specifically Ge and its alloys are very limited. The challenges in formation of uniform PGe structures, direct growth of high-quality layers on unreconstructed PGe media, and low-cost substrate reconditioning for substrate reuse, are being the main obstacles for adoption of this technique. Chapters IV, V and VI of this manuscript address these challenges, respectively, offering a viable approach for sustainable Ge alloy FSMs production.

Chapter III

3. 2D-assisted epitaxy of group IV semiconductors using graphene engineering and Anchor Point Nucleation

This chapter focuses on the challenges of 2D-assisted epitaxy for non-polar group IV semiconductors. The chapter is in form of scientific article published in the journal *Small*. It introduces a novel approach of heterointegration of Ge layers on graphene through substrate engineering. A plasma treatment of the graphene covered substrate allows the formation of nanohole defects in the graphene lattice. These defects serve as preferential nucleation sites, enabling it to anchor the epitaxial layer on the graphene surface and to orients its crystalline structure. The full high-quality epitaxial layer is then formed through a lateral overgrowth on top of the graphene surface. This paves the way for 2D-assisted growth of non-polar semiconductors and fabrication of FSMs.

3.1 Foreword

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Contribution to the manuscript:

This article contributes to the thesis by demonstrating the heterointegration of non-polar Ge layers on graphene. It introduces a new original approach using substrate engineering of graphene and through-hole nucleation to obtain high-quality layers over graphene

covered substrate. This is an important step towards universal substrate for production of high-quality semiconductor FSMs.

3.2 French abstract

L'hétérointégration du graphène avec des matériaux semi-conducteurs et le développement de dispositifs hybrides fonctionnels à base de graphène dépendent fortement du contrôle de l'énergie de surface. Bien que la Remote Epitaxy (RE) offre l'une des techniques les plus attrayantes pour la mise en œuvre des hétérostructures 3D/2D, elle convient uniquement aux matériaux polaires et dépend énormément de la qualité de l'interface du graphène. Dans cette étude, nous avons démontré la croissance de couches de germanium (Ge) monocristallines sans défauts sur un substrat de Ge recouvert de graphène en introduisant une nouvelle approche appelée nucléation par point d'ancrage. Cette approche puissante basée sur l'ingénierie de surface du graphène permet la croissance de semi-conducteurs sur n'importe quel type de substrat recouvert de graphène. Grâce à un traitement au plasma, des défauts tels que des liaisons pendantes et des ouvertures nanométriques, qui agissent comme les sites de nucléation préférentiels, sont introduits dans la couche de graphène. Nos données expérimentales ont révélé la nature de ces défauts, leur rôle dans la nucléation et les mécanismes régissant cette technique. De plus, la microscopie électronique de transmission à haute résolution combinée à l'analyse de phase géométrique a établi que les couches formées sont parfaitement monocristallines, sans contrainte et orientées par le substrat situé sous la couche de graphène. Ces découvertes fournissent de nouvelles perspectives sur l'ingénierie du graphène par le plasma et ouvrent une voie universelle pour l'hétérointégration de semi-conducteurs 3D de haute qualité sur le graphène, et la fabrication des FSMs.

Unraveling the heterointegration of 3D semiconductors on graphene by Anchor Point Nucleation

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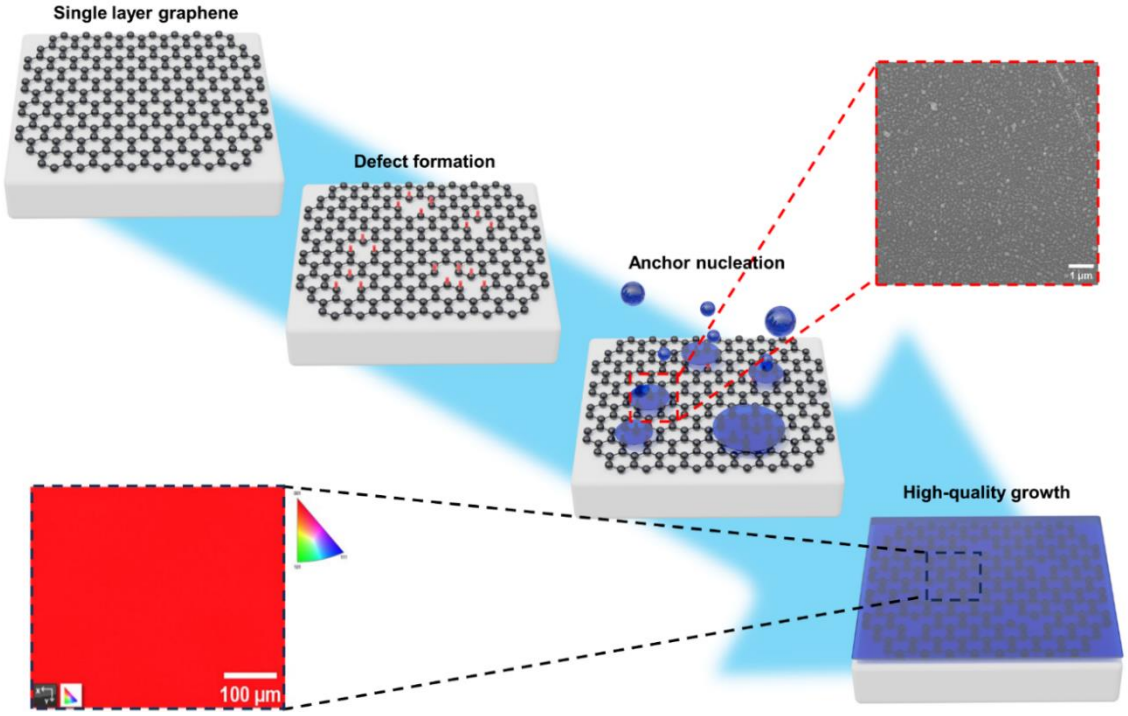
† Equal contribution

Keywords: Graphene, Heterointegration, Van der Waals epitaxy, Anchor Point Nucleation, Substrate engineering

3.3 Graphical abstract



3.4 Abstract

The heterointegration of graphene with semiconductor materials and the development of graphene-based hybrid functional devices are heavily bound to the control of surface energy. Although remote epitaxy offers one of the most appealing techniques for implementing 3D/2D heterostructures, it is only suitable for polar materials and is hugely dependent on the graphene interface quality. Here, we demonstrated the growth of defect-free single-crystalline germanium (Ge) layers on a graphene-coated Ge substrate by introducing a new approach named Anchor Point Nucleation. This powerful approach based on graphene surface engineering enables the growth of semiconductors on any type of substrate covered by graphene. Through plasma treatment, defects such as dangling bonds and nanoholes, which act as preferential nucleation sites, are introduced in the graphene layer. Our experimental data unraveled the nature of those defects, their role in nucleation, and the mechanisms governing this technique. Additionally, high-resolution transmission microscopy combined with geometrical phase analysis established that the as-grown layers are perfectly single crystalline, stress-free, and oriented by the substrate underneath the engineered graphene layer. These findings provide new insights on the

graphene engineering by plasma and open-up a universal pathway for the heterointegration of high-quality 3D semiconductors on graphene for disruptive hybrid devices.

3.5 Introduction

The monolithic heterointegration of three-dimensional (3D) bulk materials and 2D layered materials has sparked great interest, since their extraordinary intrinsic properties can be conjugated to obtain unique functionalities arising from the physical stacking of such materials[144,227]. Quasi-Van der Waals epitaxy (QVdWE) can theoretically enable epitaxial growth of crystalline 3D semiconductors on 2D materials, while circumventing the lattice and thermal mismatch issues, thereby extensively reducing defect density in the epilayers[85,228]. However, while the QVdWE of 2D/3D heterostructures[144] has been well established, the epitaxial growth of single-crystalline 3D on 2D heterostructures is an ongoing challenge[136,229–232]. This is mainly due to the dissimilar lattice structure of the substrate and epilayer, chemical bonding across the interfaces between 3D and 2D materials[233], but also due to the low surface energy of 2D materials[136].

Remote epitaxy (RE) has been proposed as a promising technique to circumvent these limitations and achieve high-quality single-crystalline layers[62]. In this approach, graphene is used as a non-polar interlayer. The epilayer's crystalline orientation is achieved via remote interactions that permeate through graphene. This technique has been applied for the growth of single-crystalline III-V, III-N semiconductors[62–64], and other materials including metals[80], complex oxides[141], halide perovskites[79], etc. In recent years, substantial advancements and significant progress in understanding the fundamental physics and principles governing RE[79,234,235], have solidified RE as a prospective method for the fabrication of freestanding membranes. Furthermore, recent studies have suggested that the presence of native oxides beneath the graphene can induce the formation of pinoles within the graphene interface, helping the orientation of the epilayer[139], in addition to remote polar interactions through the graphene. The quality of the graphene interface is a critical factor influencing the quality of the final membranes. The presence of residues, multilayers, wrinkles, or grain boundaries within the graphene can lead to the formation of polycrystalline layers[145]. To address these issues, several innovative solutions have been recently introduced, such as dry transfer techniques[145], or the

growth of high-quality graphene directly on semiconductor substrates[236,237]. Nonetheless, a significant challenge persists in the realm of RE. Given that the success of RE growth depends on the polarity of both the underlying substrate and the epilayer, this method is exclusively suitable for polar materials[234]. Consequently, it is impractical for applications involving non-polar materials like silicon (Si) and germanium (Ge). Hence, an alternative approach is imperative to alleviate these constraints and enable the growth of non-polar, single-crystalline layers while facilitating the production of freestanding membranes through 2D material-assisted epitaxy.

In this work, we propose a universal approach called anchor point nucleation (APN), based on controlled introduction of nanoholes in graphene interface by plasma treatment and epitaxial overgrowth, to monolithically grow single-crystalline semiconductors on graphene-terminated substrates (including non-polar materials). We demonstrated that by using plasma treatment, we can introduce defects in the graphene layer that improve its surface reactivity and adhesion with other materials. Those defects act as preferential nucleation sites for the epitaxial growth as a clear evidence was provided by in-situ TEM studies from our previous work[232]. Defect engineering using other methods has been previously reported for the epitaxial growth of 2D heterostructures[238,239]. However, this is the first time that such an approach is used for the growth of semiconductors on non-polar materials such as Ge. Moreover, the nature of the induced defects, their role in the epitaxial growth and the underlying mechanisms for such a technique are elucidated. Here, we find that the induced defects are mainly dangling bonds and nanoholes depending on the treatment duration. Our experimental data provide a clear corroboration for the role played by the induced defect during the nucleation process. We unveil that the APN approach is governed by the nucleation in the nanoholes followed by an overgrowth of a continuous layer. The combination of HRTEM measurements and strain mapping demonstrates that the APN method enables the epitaxial growth of single-crystalline Ge layers without any deformation or defects, caused by lateral overgrowth on graphene-terminated Ge substrate. Our findings demonstrate that the APN approach is a powerful technique that is suitable for the epitaxial growth of 3D semiconductors on graphene and is a promising solution to circumvent the limiting factors of QVdWE and RE.

3.6 Results and discussion

3.6.1 Anchor Point Nucleation approach

Figure 3-1 shows the schematic representation of the Anchor Point Nucleation (APN) processing steps that enhance the reactivity of graphene and enable the growth of monocrystalline layers on SLG. This approach is based on the controlled introduction of defects in the SLG, which will act as preferential nucleation sites allowing them to anchor adatoms on the graphene surface. The introduced nanoholes then serve as seeding sites to provide the crystal orientation to the epilayer, which is obtained by epitaxial overgrowth on SLG[139,147]. To achieve this, first, large-area SLG is transferred on the substrate using wet transfer technique (Figure 3-1a, see methods for more details). The substrate is then treated by plasma to introduce defects such as dangling bonds and nanoholes in the SLG (Figure 3-1b). These defects significantly enhance the surface energy of the graphene[240] and serve as preferential nucleation sites for the epitaxial growth. Moreover, the nanoholes provide a direct link between the substrate and epilayer enabling substrate-oriented growth even for elemental materials. It is worth mentioning that the use of plasma treatment is more advantageous compared to other patterning techniques such as photolithography and electrolithography[147,241], which are complex, expensive and uses photoresist. In contrast, the plasma-based technique is easy to use, cost-effective, simple without multistep processes and it enhances the cleaning of PMMA residues from wet transferred graphene[242–244], preventing random nucleation that will result in 3D growth. After the formation of dangling bonds and nanoholes by plasma treatment, we proceed with the nucleation of semiconductor islands that grow preferentially on the induced defects of the engineered graphene layer (Figure 3-1c). The nucleation on nanoholes allows the islands to be oriented by the underlying substrate. The nanohole mediated nucleation is then used as a seed layer to grow complete epitaxial layers trough the lateral overgrowth of the islands (Figure 3-1d). Compared to QVdWE and RE, the APN approach enables obtention of substrate oriented epilayers even for non-polar materials (e.g., Si and Ge), maintaining a significant portion of the weak bonding to the substrate, due to the epitaxial overgrowth on graphene interface. This is especially interesting for further exfoliation of the film.

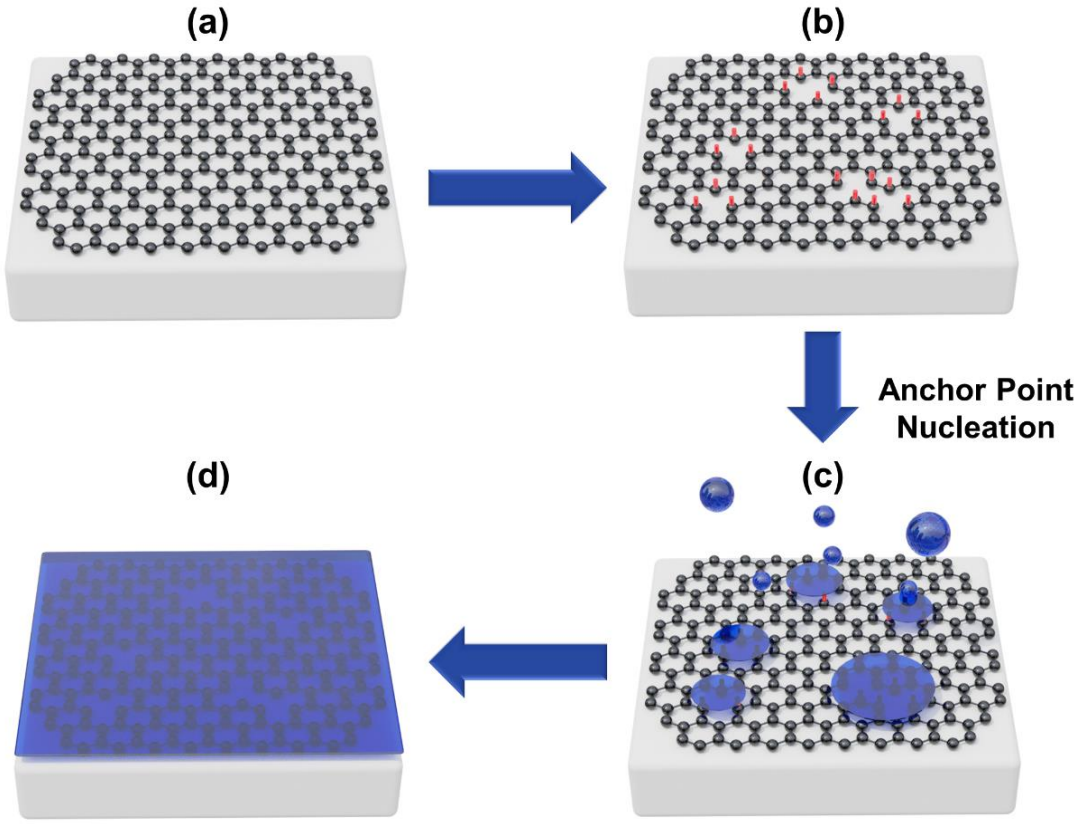


Figure 3-1: Schematic illustration of Anchor Point Nucleation approach enabling growth of monocrystalline layers on top of single layer graphene (SLG). (a) SLG is transferred on semiconductor substrate, (b) controlled introduction of defects in SLG by plasma treatment (c) Preferential nucleation on SLG (d) epitaxial growth of monocrystalline epilayers.

3.6.2 Effect of plasma treatment on SLG

A key challenge of the APN approach is to prevent a complete etching of the atomically thin SLG and introduce defects in a controlled manner. To this end, a balance between the duration and the power of the plasma must be established to slightly damage the SLG, while maintaining its nature and coverage on the substrate[147]. This is not an easy task since the graphene can be easily etched away by standard plasma etching techniques[245]. Indeed, our initial studies indicate that a very light plasma treatment in short burst must be used to avoid complete removal of the SLG on the surface (details can be found in Methods section). To further elaborate on these findings the effects of O_2 plasma etching (320 mTorr O_2 pressure, radio frequency power of 10 W and treatment duration varying between 0 s

and 30 s) on the SLG quality were thoroughly investigated by Raman spectroscopy and X-ray photoelectron spectroscopy (XPS) measurements.

Figure 3-2a shows Raman spectra of transferred SLG on Ge substrate for different duration of plasma treatment. The Raman spectra consist of a set of distinct peaks. The G band is related to C-C bond stretching in sp^2 carbon systems, the D band is related to defects and disorder, and the 2D band is the second order of the band D, but does not require a defect[246]. The non-treated SLG shows very sharp G and 2D bands with a very low D band, demonstrating the high-quality graphene layer with large crystallite sizes. Let's remember that the ratio of the D to G intensities (I_D/I_G) is inversely proportional to the crystallite size[247]. The apparition of D band and significant reduction of 2D band after the application of plasma treatment show a clear evidence of defect introduction inside the graphene layer. The I_D/I_G ratio as a function of treatment duration extracted from Figure 3-2a is shown in Figure 3-2b. A sharp initial rise of the D band is observed up to 6 s and then it decreases with increasing treatment duration. During the initial stages of the treatment, we believe that mainly dangling bonds and atomic vacancies are introduced in the SLG. As the duration increases larger nanoholes are formed in the SLG, causing a significant reduction in the graphene crystallite size. From Figure 3-2a and 3-2b, we concluded that up to 18 s of treatment, the SLG is being transformed from pristine graphene to nanocrystalline graphene with smaller crystallite size separated by small amorphous patches[248,249]. The annealing of the substrate during the epitaxial growth transforms the amorphous patches and nanosheets into crystalline graphene as demonstrated by Turchanin et al[250]. Such transformation is characterized by the appearance of the D-band and the increase of I_D/I_G and the broadening of all the peaks[249] (see Figure S3-1). Above 18 s of plasma treatment, the nanocrystalline graphene is transformed to low sp^3 amorphous carbon[248].

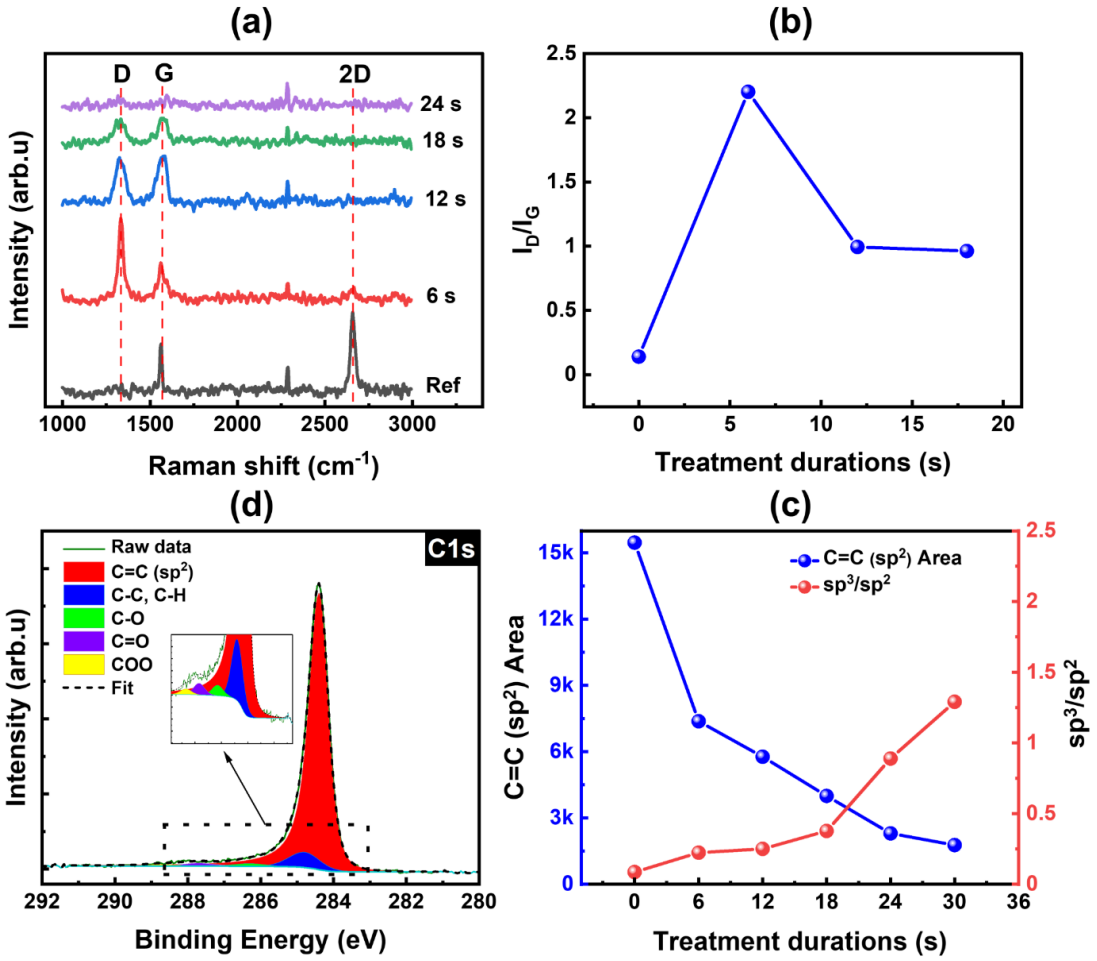


Figure 3-2: Analysis of the influence of plasma treatment duration during graphene surface engineering. (a) Raman spectra of single layer graphene for different durations, (b) I_D/I_G ratio extracted from the Raman measurements in (a), (c) High-resolution XPS spectrum of C1s of a non-treated SLG showing the sp^2 bonding of the graphene. (d) C=C sp^2 bond area (blue) and sp^3/sp^2 bond ratio (red) extracted from the XPS measurements of C1s orbital for the different treatments.

To further investigate the defect introduced in SLG, we performed XPS to measure spectra of C1s core level and to study the nature of chemical bonds in engineered graphene. Figure 3-2c shows the high-resolution C1s spectrum of a non-treated SLG. This spectrum contains mainly the sp^2 carbon peak centered at 284.4 eV. The analysis of the XPS spectra after the plasma treatment is presented in Figure 3-2d showing the C=C sp^2 bond area (blue) and the sp^3/sp^2 bond ratio (red) for different treatment duration. After, the plasma treatment, the FWHM of the C1s peak became broader (Figure S3-2). From Figure 3-2d,

we can see that the C=C sp^2 area decreases with the increase of treatment duration, while the ratio sp^3/sp^2 increases as more defects are generated in the SLG. This clearly demonstrates the introduction of defects in graphene. Initially the sp^2 area decreases rapidly due to the generation of dangling bonds. As the nanoholes start to grow by merging multiple atomic vacancies, the slope of the curve of sp^2 area decreases. These observations are in good agreement with the Raman spectroscopy measurement presented in Figure 3-2a and Figure 3-2b. More XPS analysis is presented in Figure S3-2 and Table S3-1.

3.6.3 Preferential nucleation induced by defects

To bring new insight on the influence of defects in SLG on epitaxial growth and to corroborate out above-mentioned hypothesis, we studied the impact of plasma treatment on epitaxial nucleation of few nm of Ge on the treated SLG. On pristine graphene, the formation of seeds is difficult due to the SLG's low surface energy, which makes epitaxial nucleation very challenging, because the adatoms barely stick to the surface and the nuclei can be easily desorbed before reaching the critical size[232]. Such nucleation results in a polycrystalline 3D growth mode as schematically illustrated by Figure 3-3a (see also Figure S3-3a). This is further confirmed by grazing incident X-ray diffraction (GIXRD) measurements (gray data set). As stated in the previous part, very short duration of plasma treatment introduces mainly dangling bonds and atomic vacancies, which help to increase the wettability of graphene and therefore significantly enhance its reactivity. This results in the increase of the Ge (111) orientation, which is the most favorable in case of QVdW growth of Ge on SLG[232], as shown by grazing incident X-ray (GIXRD) diffraction results shown in Figure S3-4. Even though those dangling bonds enhance the nucleation and crystal orientation of the epilayer on the SLG by acting as preferential nucleation sites as represented in Figure 3-3b, the resulting layer cannot be epitaxially oriented by the substrate underneath the graphene layer since there is no direct link between them. For treatment of 12 s and above, we observe the growth of seeds with crystal form, which is clear evidence of the nanohole formation in the SLG (Figure S3-3c). In contrast to dangling bonds, nanoholes provide a direct link with the substrate underneath the SLG, enabling direct epitaxial growth of substrate-oriented seeds (see Figure 3-3c). Similar observations have been reported[139] in nanoholes occurring during the underlying substrate

deoxidation. The nanoholes-mediated nucleation must be dominant to grow epitaxially monocrystalline layers on top of engineered graphene.

By increasing the duration of plasma treatment, more nanoholes are introduced in the SLG structure and their size increases. Figure 3-3d-f show SEM micrographs tracking the evolution of the nucleation of Ge on treated SLG at duration of 18 s, 24 s and 30 s, respectively. From these images, we can see that the density and the size of the seeds are increasing with treatment duration. The increase in the crystal size is attributed to the presence of larger nanoholes. For further understanding, we plotted the surface coverage by the seeds as a function of treatment duration shown in Figure 3-3g. We found that the surface coverage is proportional to the treatment duration. This can be explained by the fact that as the duration increases, larger regions not covered by graphene become available, enabling the nucleation of larger seeds directly on the substrate. When the SLG is totally etched away (above 30 s of treatment), the seeds form a continuous and homogenous layer. To successfully perform APN growth, the presence of the SLG is necessary, as it provides the surface with weak VdW bonding that facilitates the detachment of the epilayer. For this reason, the plasma treatment duration needs to remain below 30 s. It is also important to note that the increasing quantity of direct links between the epilayer and the substrate will increase the adhesion force of the film and make its exfoliation more difficult[147].

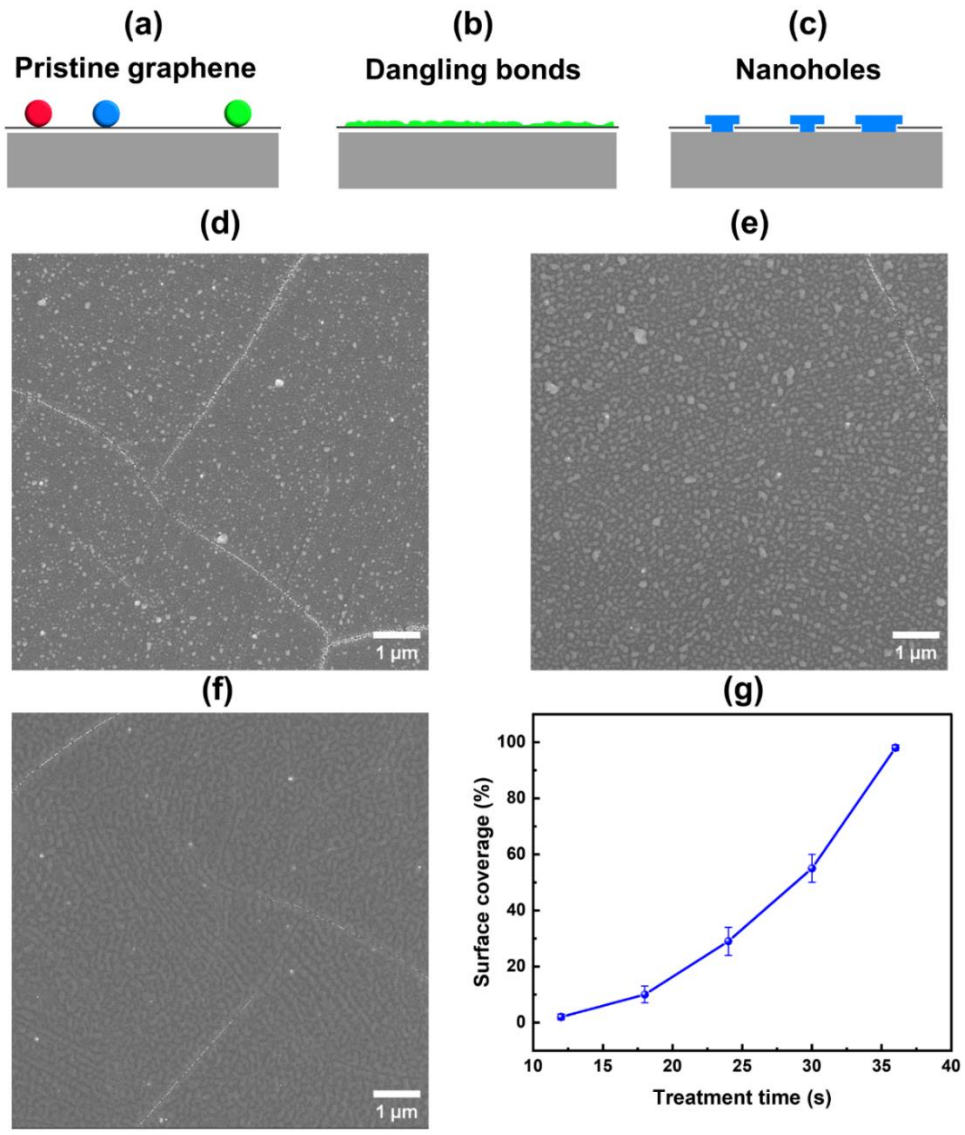


Figure 3-3: Study of the effect of plasma treatment duration on the nucleation of Ge by APN on engineered SLG on Ge substrate. (a), (b), (c) schematic illustration showing the different growth mechanisms on pristine graphene, induced by dangling bonds (<12 s of the plasma treatment) and via nanoholes (>12 s of plasma treatment), respectively. On the pristine graphene we have a 3D growth mode, while through the nanoholes we have a single-crystalline layer oriented by the underlying substrate. (d), (e), (f) SEM images tracking the evolution of the nucleation of Ge on treated SLG with duration of 18 s, 24 s and 30 s, respectively. For all the treatments presented in this figure, the growth temperature was 400 °C and the thickness is 5 nm. For short duration (up to 6 s), the APN is proceeded through dangling bonds and for longer durations through the nanoholes induced in the graphene layer. (g) evolution of the graphene surface coverage by Ge nuclei as a function of treatment duration extracted from the SEM images.

3.6.4 Growth of Ge on engineered graphene using APN approach

After unraveling the different mechanisms of nucleation involved in the APN approach, here we performed the epitaxial growth of Ge layers on the engineered SLG (18 s of O_2 plasma treatment) supported by Ge (100) substrate. Figure 3-4a and 3-4b show plan-view scanning electron micrographs (SEM) of the as grown epilayer. The SEM images reveal a homogenous and smooth surface of the 500 nm-thick Ge layers, confirming their high morphological quality. In Figure 3-4a, we can notice few defects, which we attributed to the poly-nucleation induced by the multilayer graphene. This can also be seen in the Figure 3-3 showing the SEM images of the early stages of the nucleation. However, without the multilayer of graphene the epilayer surface is quite homogenous (Figure 3-4b). The morphological quality of the epilayers was also investigated by AFM and the resulted image is displayed in Figure 3-4c. From this figure, we can notice a featureless and smooth surface with an RMS roughness ~2 nm. The electron backscattering diffraction (EBSD) map of the top surface presented in Figure 3-4d reveals that the Ge epilayers grown on the engineered SLG are perfectly single crystalline and have the same crystal orientation as the Ge (100) substrate. This demonstrates that the epilayer is oriented by the underneath substrate through the induced nanoholes. On pristine SLG, the as-grown layers are polycrystalline as previously reported in the literature[137,145,234,251], a result of spherical polycrystalline nucleation (Figure S3-5). In contrast, the APN approach, which is based on the controlled introduction of nanoholes in SLG and epitaxial overgrowth, has successfully demonstrated the growth of continuous and smooth layer on a non-polar substrate. So far, this is unachievable with the QVdWE or RE[62] since they are governed by the interactions with 2D interface or the substrate underneath the graphene[234].

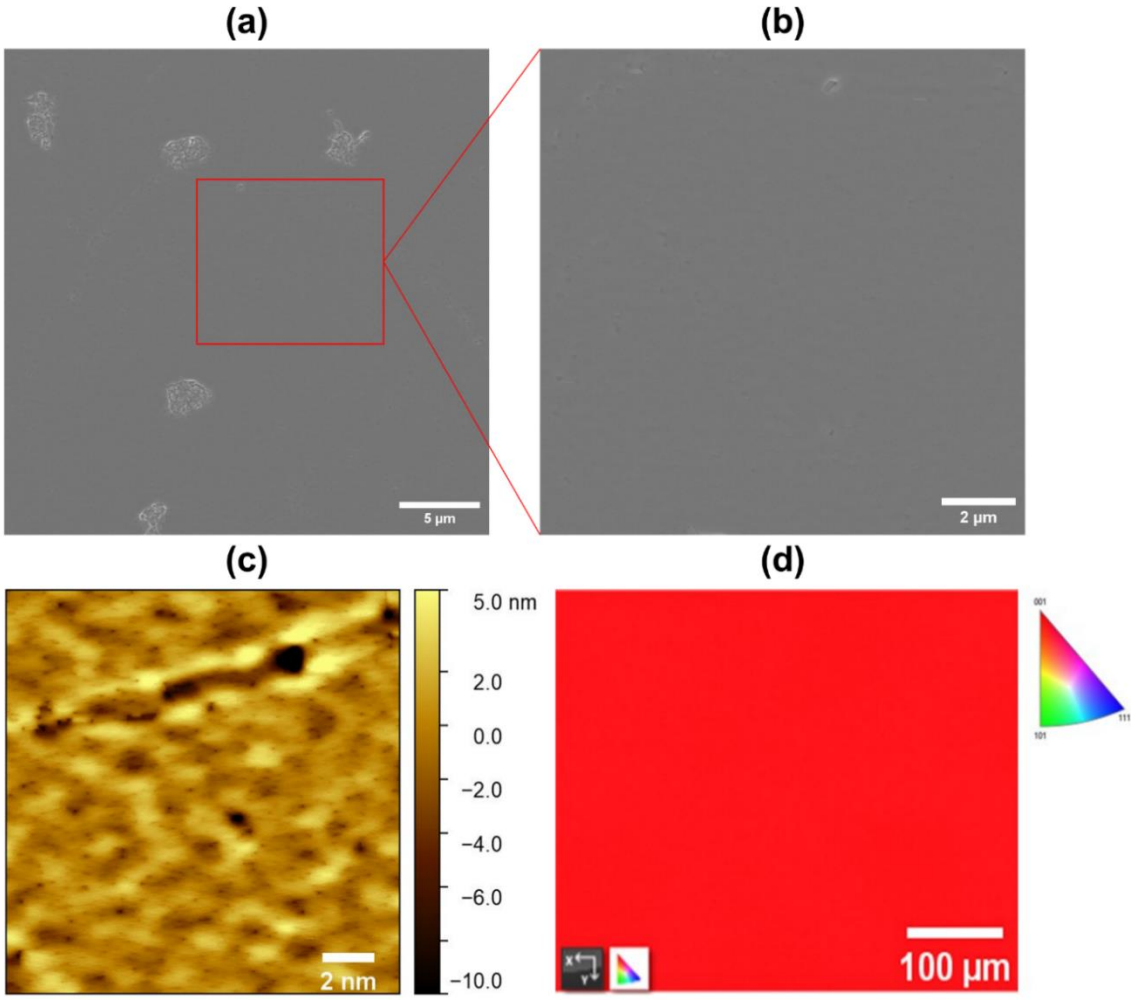


Figure 3-4: Growth of Ge layer (500 nm) on plasma treated (18 s) single layer graphene on Ge (100) substrate using the APN approach. (a) Low magnification plan-view SEM image showing homogenous surface with some defects induced by the nucleation on multilayer graphene, (b) SEM image of the red square on (a) showing a surface without any defect, (c) AFM image of a scan 5 × 5 µm^2 area showing smooth surface with an RMS roughness of 2 nm, (d) EBSD map of the layer showing single orientation, which demonstrates its single-crystalline nature.

To further investigate the crystalline quality of the as-grown layers by the APN approach, cross-sectional transmission electron microscopy (TEM) measurements were performed. Figure 3-5 shows the TEM analysis of Ge epilayers grown on engineered SLG. The cross-sectional high-angle annular dark-field STEM (HAADF-STEM) of the epitaxial structure is presented in Figure 3-5a. From this figure we can see that the epi structure is made of a continuous Ge epilayer, the engineered SLG interface and the Ge substrate. We

can also notice some small holes (Figure S3-6) highlighted by the red arrow, which we attributed to the overgrowth of Ge on the SLG once the nucleation is initiated within the nanoholes. This observation is in good agreement with our proposed mechanism for the APN approach presented in the previous sections. Figure 3-5b shows the cross-sectional high-resolution TEM image of the epitaxial structure where the SLG interface (dark contrast) can be observed clearly between the epilayer and the substrate. This HRTEM image was obtained with the zone axis <001>. Note that for a better view, the image was rotated by 90° with respect to the initial image. Through the dark interface representing the perfect graphene layer in Figure 3-5b, we can notice some small discontinuities (highlighted by yellow arrows) indicating the induced nanoholes. This observation confirms that the SLG still exists after the Ge growth, indicating that the graphene is not damaged under the used growth conditions and still maintains its nature. From this HRTEM image, there is clear evidence of the absence of structural defects in the epilayer, which demonstrates the high structural quality of the as-grown layers by APN. Figure 3-5c and 3-5d display the fast Fourier transform (FFT) patterns of the epilayer and the underlying substrate shown in Figure 3-5b, respectively. These FFT patterns display the family planes of (220) and (400) of the Ge diamond cubic lattice with d-spacing of ~ 0.2 nm and ~ 0.14 nm, respectively. We only observed those family planes due to the fact that the zone axis is <001>. We can notice that the FFT pattern for the substrate (Figure 3-5c) is similar and perfectly matches to the one for the epilayer (Figure 3-5d), indicating the same structure. This observation confirms the epitaxial relationship between the epilayer and the substrate and clearly demonstrates the single-crystalline nature of the as-grown layers. As mentioned previously, the epilayer is oriented by the underlying substrate because the nucleation through the nanoholes is dominant. Similar observations have been reported by Yu et al. during the growth of GaN on nitrogen plasma-treated graphene[251]. The Ge epilayer's and the substrate's structures are diamond cubic as shown in Figure 3-5e and 3-5f displaying the inverted fast Fourier transform (IFFT) images that show the (220) planes of the epilayer and the substrate, respectively, with a d-spacing of ~ 0.2 nm. Our results also demonstrated that some defects induced during the nucleation process due to multilayer graphene (see Figure 3-4a) can lead to the formation of a polycrystalline epilayer as shown in the Figure S3-6 of the supplementary materials. From this figure we

can clearly see that the epilayer have random diffraction spots with different orientations compared to the substrate and there is evidence of stacking faults and microstructure twinning. This suggests that the initial graphene layer should be uniform and of high quality prior to any treatment.

To clarify the mechanisms of how the epilayers relieve the deformations and the epitaxial stress, the strain state of the as-grown Ge layers on engineered SLG was studied by HRTEM (Figure 3-5b) combined with the geometrical phase analysis (GPA) method. The 2D strain and rotation maps of Ge/SLG/Ge are presented in Figure 3-5g-j. Note that the maps have been rotated by 90° with respect to the initial HRTEM image. The analysis of those maps provides clear evidence that there is no deformation and strains in the Ge epilayers in respect to the underlying substrate. This confirms that the growth is coherent without strain relaxation and comparable to homoepitaxy. From the in-plane map (E_{xx}), we can notice a very low negative out-of-plane deformation in the SLG interface that could be attributed to the nucleation on the graphene dangling bonds. However, in the regions we considered as nanoholes (Figure 3-5b), the in-plane deformation is zero ($E_{xx} = 0$). These observations perfectly corroborate the mechanisms governing the APN approach that we presented in the previous sections. The quality of such layers is suitable for high-performance hybrid devices.

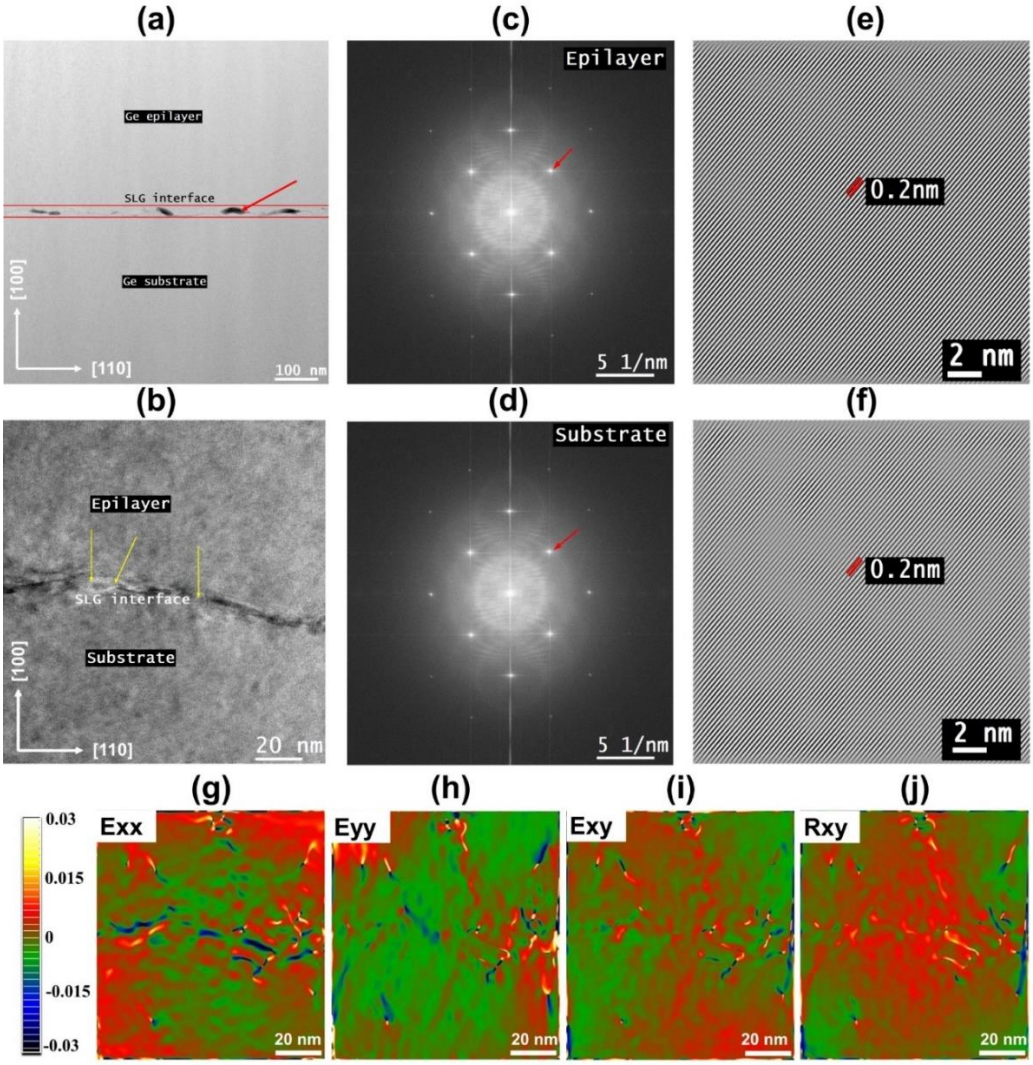


Figure 3-5: TEM analysis of as-grown Ge layer on plasma treated single layer graphene on Ge substrate using the APN approach. (a) Cross-sectional HAADF-STEM image of Ge epilayer grown on the engineered SLG on Ge. The SLG interface is marked off by the red lines and the red arrow shows a small hole at the interface induced by the overgrowth on the SLG, (b) cross section HRTEM image of a defect-free sample (similar region displayed in Figure 3-4b) showing the graphene interface between the substrate and the epilayer. The yellow arrows mark off the regions where nucleation occurred directly on the substrate through the nanoholes created by the plasma treatment, (c) and (d) FFT patterns of the epilayer and the substrate, respectively, showing the same diffraction spots demonstrating the epitaxial relationship between the substrate and the epilayer, and the monocrystalline nature of the as-grown epilayer, (e) and (f) IFFT images showing the Ge(220) planes of the layer and the substrate highlighted by red arrows in (c) and (d), respectively, with a d-spacing of ~ 0.2 nm, (g)-(j) Geometrical phase analysis (GPA) deformation maps of the Ge layers grown on engineered SLG on Ge substrate converted from (b).

In comparison to RE[62], which is governed by the polarity[234] of the substrate and QVdWE governed by interactions with 2D interface, the APN approach is a technique that can produce high-quality single-crystalline layers of semiconductors on any substrate including non-polar substrate. Our findings provide new insights on plasma-induced defects in SLG and open a new route for the growth of hybrid functional devices and fabrication of semiconductor freestanding membranes. Few recent works reported on a similar technique using lateral overgrowth, where the nucleation is induced by defects or nanopatterns in the graphene[139,147]. For instance, a selective area epitaxy of 2D hBN on graphene induced by defects and the epitaxial MoS_2 on hBN assisted by substrate defects has been reported[238,239]. Our work demonstrates that defect-induced anchor points are promising for the epitaxial growth of any 3D semiconductors (polar and non-polar) on a graphene-terminated non-polar substrate and alleviates the limitations of QVdWE and RE.

3.7 Conclusion

In this study, we report an original approach called anchor point nucleation for monolithic integration of 3D semiconductors on 2D materials. We demonstrated the epitaxial growth of defect-free single-crystalline Ge layers without any deformation on engineered SLG. Oxygen plasma treatment is used for surface engineering of the graphene, introducing defects such as dangling bonds and nanoholes in a uniform and controlled manner. These defects then act as preferential nucleation sites, enabling efficient and substrate-oriented nucleation for growth of high-quality epilayers. HRTEM and STEM results provide clear evidence that the layers on SLG are perfectly single crystalline and follow the underneath substrate orientation without any strain. Based on our experimental data, a growth model is proposed to elucidate the epitaxial growth mechanisms of Ge layers on engineered graphene. We demonstrated that the growth is governed by the nucleation through nanoholes followed by a lateral overgrowth of the nuclei anchored on the substrate and a coalescence of a continuous layer. These results lay the groundwork for advanced heterointegration of 3D/2D materials using engineered 2D substrates, for development of highly mismatched structures and semiconductor freestanding membranes, as well as their disruptive applications.

3.8 Methods

3.8.1 Graphene transfer

Commercially available SLG is used in this work. The SLG grown by CVD on copper substrate is initially transferred on polymer support using polymethyl methacrylate (PMMA) layer and dissolution of the copper substrate. To transfer the SLG on working substrate the received PMMA/SLG on polymer support stack is slowly immersed in deionized water (DIW) until the PMMA/SLG layer is released from its support and is floating on top of the DIW. Before the transfer, the Ge (001) substrate was previously deoxidized in HBr for 1 min and rinsed with DIW. In fact, it was demonstrated that HBr can effectively remove suboxides on Ge surfaces[237]. This deoxidized substrate is introduced into the DIW and is used to carefully scoop out the PMMA/SLG from below. The Ge substrate with PMMA/SLG is then dried for 30 min in ambient clean room air, followed by annealing on hot plate at 150 °C for 1h. The sample is then stored for 24h under the vacuum to avoid any detachment of the SLG and to remove all the residual moisture. Finally, to clean the SLG, the PMMA is dissolved in acetone and isopropyl alcohol (IPA) at 50 °C for 15 min in each. This part is crucial to obtains PMMA-free SLG surface, because any remaining polymer residue will result in unwanted nucleation leading to polycrystalline growth[232].

3.8.2 Plasma treatment

The SLG/Ge substrate is treated by oxygen (O_2) plasma process to introduce defects in the SLG. The O_2 plasma treatment is performed in a barrel type chamber, under a pressure of 320 mTorr and a radio frequency (RF) power of 10 W. The treatment duration varies between 6 s and 60 s. It is worth mentioning that increasing the RF power significantly accelerate the etching process, leading to complete destruction of the SLG. For example, at RF power equal to 20 W, the SLG was completely etched away after 12 s of the treatment. This aspect was carefully optimized during the experiments.

3.8.3 Epitaxial growth

Epitaxial Growth was carried out in VG Semicon VG90F CBE reactor, with liquid nitrogen cryopanel and with a thermocouple as a means of monitoring the temperature

during the growth. Prior to epitaxial growth, all samples were annealed at 600 °C during 10 min to thermally deoxidize the revealed parts of Ge substrate and to help eliminate any potential residues of PMMA from the transfer. The Ge was grown at 520 °C, at chamber pressure of ~$6E^{-6}$ Torr, using a solid source of Ge with a K-Cell temperature at 1250 °C.

3.8.4 Characterizations

Raman spectroscopy is performed using Horiba Raman spectrometer with a CCD detector and a laser with an excitation wavelength of 474 nm to analyze defects induced in SLG by plasma treatment. A 100× objective was used for the measurements, which results in a laser spot of ~1 µm in size. Before the data analysis, the background noise was subtracted. The D:G band ration was calculated directly from the maximum intensity of the bands.

X-ray photoemission spectroscopy is realized with Kratos Axis Ultra spectrometer using a monochromatic Al Kα source (hν = 1486.7 eV) and a charge neutralized system. Survey scans and high-resolution scans are performed with an analysis area of 300 µm × 700 µm. The samples were loaded in the chamber, right after the plasma treatment, to avoid contamination from ambient exposure. The XPS spectra are corrected to the main line of carbon 1s spectrum set to 284.8 eV. The data are analyzed using CasaXPS software. The Shirley background is subtracted from the XPS spectra, which is then fitted using a Voigt function.

The surface morphology of the nucleation and epitaxial layers is observed with a scanning electron microscope Zeiss LEO 1540 XB at 4.3 mm of working distance and 5 keV of acceleration voltage and with an atomic force microscope Veeco Dimension 3100 in tapping mode using SSS-NCHR silicon probe.

Prior to Scanning Transmission Electron Microscopy (STEM) and TEM imaging, the samples were prepared by focused ion beam (FIB) thinning and ion milling using a Zeiss NVision 40 Focused Ion Beam. The surface was protected by carbon coating to avoid the sputtering of the surface by the ion beam. The TEM and STEM observations were made in Titan Themis microscope operated at 200 kV and equipped with a CEOS probe corrector

and Ceta 16M camera from FEI. The data were treated using Gatan digital micrograph software, to evaluate the crystalline quality and strains of the layers.

The crystalline quality of the epilayers was also investigated by Rigaku smartlab HRXRD system with Cu Kα X-ray source in GIXRD configuration.

3.9 Author Contributions

Thierno Mamoudou Diallo and Tadeáš Hanuš contributed equally to this work. The manuscript was written through the contributions of all authors. All authors have given approval to the final version of the manuscript. **Thierno Mamoudou Diallo, Tadeáš Hanuš**: Conceptualization, Methodology, Investigation, Data curation, Original draft preparation, Review and Editing, Visualization. **Gilles Patriarche, Andreas Ruediger:** Investigation, Review and Editing. **Abderraouf Boucherif**: Conceptualization, Supervision, Review and Editing.

3.10 Acknowledgement

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3.11 Supplementary materials

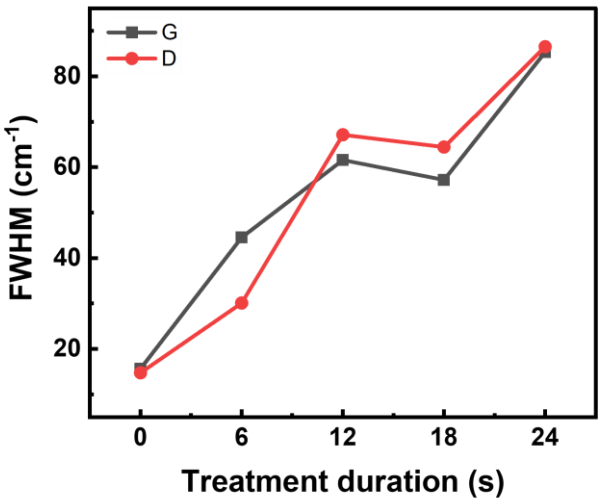

Figure S3-1: Influence of plasma treatment duration on full width half maximum (FWHM) of D and G bands in Raman spectra of the treated SLG. The broadening of the bands with increasing treatment duration signifies the transformation from pristine graphene to nanocrystalline graphene with smaller crystallite size.

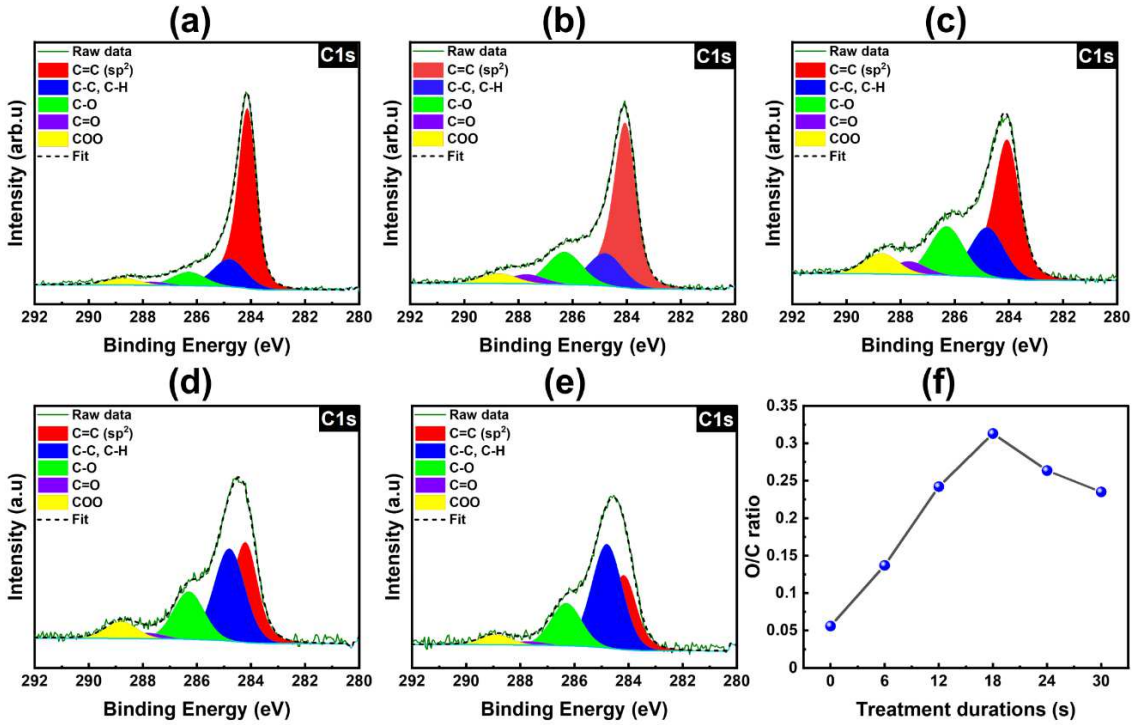

Figure S3-2: High-resolution XPS spectra of C1s of SLG treated with O_2 plasma for different durations: (a) 6 s, (b) 12 s, (c) 18 s, (d) 24 s, (e) 30 s. The spectra show the decrease of sp^2 bonding of the graphene with increasing treatment duration, and (f) O/C ratio evolution with plasma treatment duration extracted from the XPS spectra.

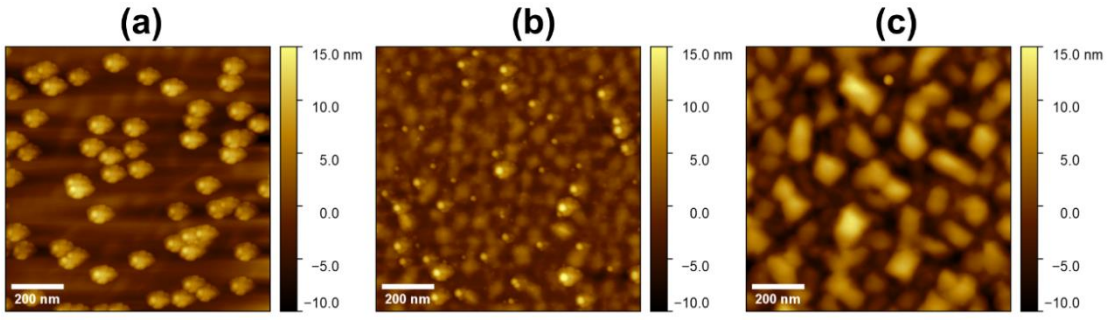

Figure S3-3: Typical AFM images of few nm Ge nucleation on (a) pristine graphene, seeds form spherical shapes on the surface due to the low surface energy of the SLG surface, (b) treated graphene with predominantly dangling bonds, the wettability of the surface is significantly improved, enabling the seed to laterally spread on the graphene, (c) treated graphene with nanoholes, the direct contact with the Ge substrate trough nanohole enables the formation of crystal shaped seeds.

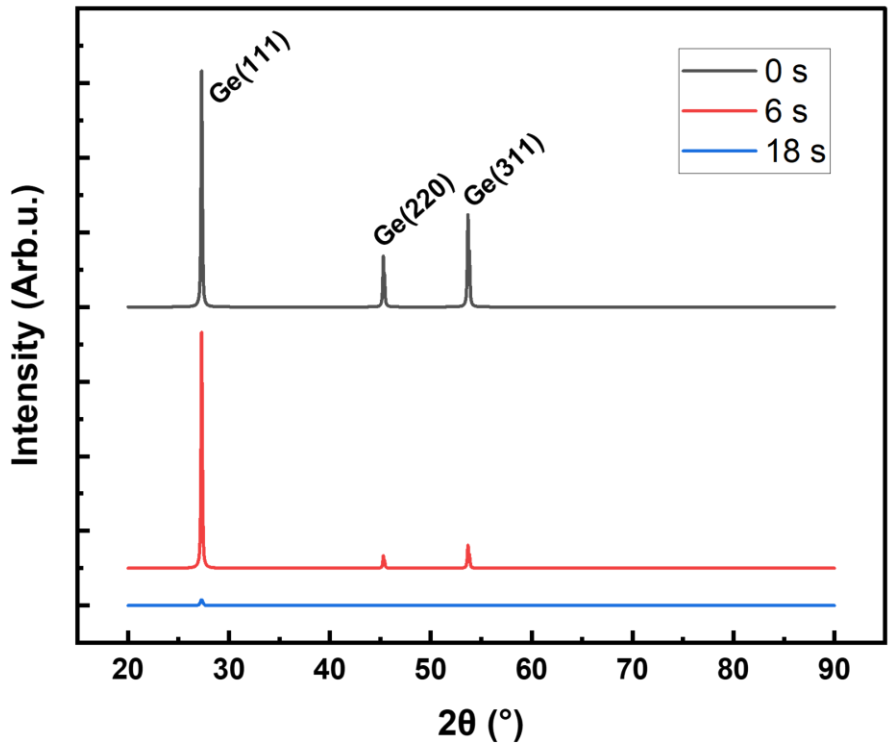

Figure S3-4: Grazing incident X-ray diffraction (GIXRD) data of Ge epilayer grown on SLG that has undergone 0 s (gray), 6 s (red) and 18 s (blue) of plasma treatment. Gray data set shows the polycrystalline nature of the Ge epilayer grown on pristine SLG, caused by its low surface energy. Red data set corresponds to Ge epilayer grown on engineered SLG with predominantly dangling bonds defect, improving SLG wettability. This results in preferential orientation of the layer along Ge (111) orientation, which is the most favorable for QVdW of Ge on SLG. The blue data set represents the Ge epilayer grown by APN with the remnant of the Ge (111) orientation (caused by the presence of wrinkles and multilayers in graphene), suggesting the Ge (001) orientation of the epilayer, obtained by through nanohole nucleation on Ge substrate. The Ge (001) orientation corresponding to the substrate does not show under GIXRD conditions.

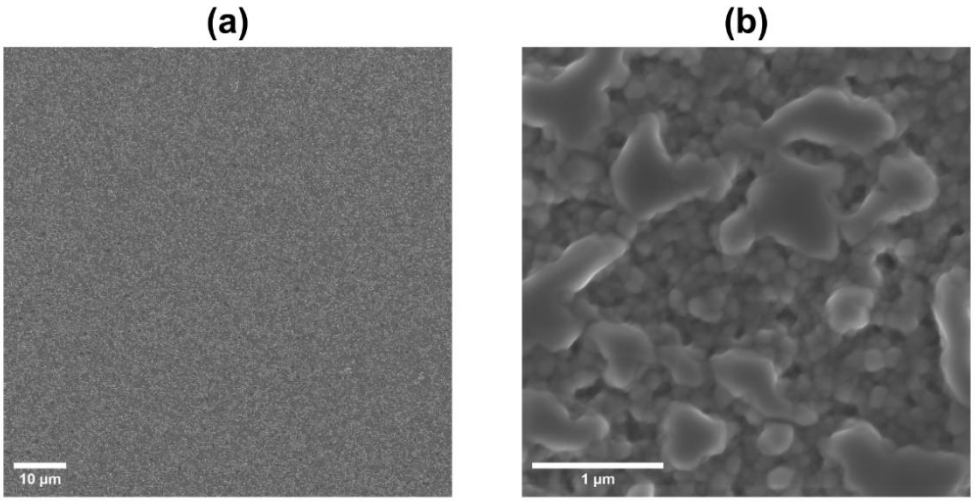

Figure S3-5: (a) SEM image of Ge layer grown on pristine graphene with inhomogeneous surface morphology due to the uncontrolled nucleation on the surface of SLG (b) Closer zoom of the SEM image in (a), showing that the layer is composed of a multitude of crystallites.

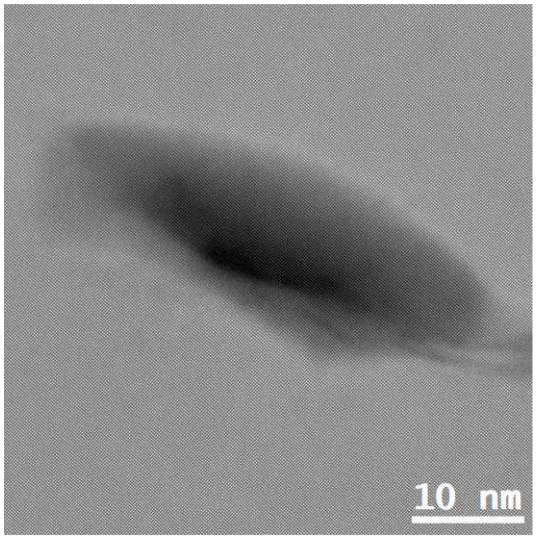

Figure S3-6: high magnification cross-sectional HAADF-STEM image of a small hole at the interface between the epilayer and the substrate shown in Figure 5a of the main manuscript.

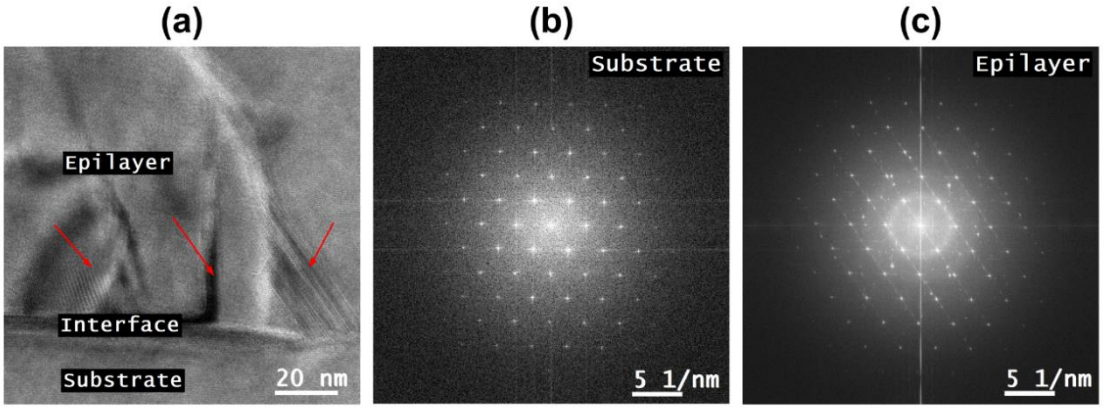

Figure S3-6: (a) Cross section HRTEM image taken at a defect similar to those displayed in Figure 4a in the main manuscript, showing the different crystalline planes and defects (highlighted by red arrows) in the epilayer, (b) and (c) FFT patterns of the layer and the substrate, respectively. In contrast to the substrate, the diffraction spots in the epilayer are random with different orientations, demonstrating the polycrystalline nature of the epilayer in those regions. Stacking faults and microstructure twinning can be seen in the epilayer.

Table S3-1: Area% evolution of different bonding species during different treatment duration of the SLG.

Bonding	**Area for different treatment duration (%)**				
	6 s	12 s	18 s	24 s	30 s
C=C	70.53	60.62	49.89	38.99	33.40
C-C, C-H	15.74	15.18	18.80	34.66	43.11
C-O	7.78	15.11	18.55	17.89	17.68
C=O	2.05	4.45	4.96	2.15	1.56
COO	3.90	4.64	7.80	6.31	4.25

Chapter IV

4. Formation of Uniform High-quality PGe layers at wafer-scale, and tailoring of their physical properties

This chapter focuses on formation of high-quality PGe layers further used as a substrate for growth of FSMs in chapters V and VI. The chapter is in form of scientific article published in the journal *Advanced Materials Interfaces*. It introduces BEE process allowing the formation of uniform PGe layers over a large surface. The combination of novel porosification tools and optimized etching process enables the formation of edge-to-edge PGe structures across 100 mm wafers with tunable thickness and porosity. Additionally, non-destructive fast feedback characterization techniques are explored to evaluate the PGe quality.

4.1 Foreword

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Journal: Advanced materials interfaces

Reference: [252]

French title: Formation à grande échelle de nanostructures poreuses et uniformes de Ge avec des propriétés physiques ajustables

Contribution to the manuscript:

This article contributes to the thesis by demonstration of high-quality PGe layer formation at 100 mm wafer-scale using BEE. The introduced technique enables the obtention of highly uniform PGe structures with tunable physical properties, while maintaining the original crystal orientation and low surface roughness. The PGe structures introduced in this article serve as a substrate for fabrication of FSMs developed in the following chapters.

4.2 French abstract

Les nanostructures poreuses de germanium (PGe) suscitent beaucoup d'attention en raison de leurs propriétés mécaniques et physicochimiques uniques, qui les rendent intéressantes pour diverses applications émergentes. En conséquence, il existe un besoin croissant de développer des méthodes de synthèse à faible cout pour assurer leur compatibilité avec une production à grande échelle. La gravure électrochimique bipolaire (BEE) est une solution à faible cout permettant de produire des couches poreuses de Ge. Cependant, l'absence de production contrôlable de couches uniformes de PGe à grande échelle est le principal facteur limitant pour les applications à grande échelle en industrie. Ce travail démontre la formation de couches homogènes de PGe à grande échelle en améliorant le processus de BEE. Les structures poreuses ainsi produites présentent une excellente homogénéité en termes d'épaisseur et de porosité, avec une variation relative inférieure à 2 % sur toute la plaquette de 100 mm. De plus, l'amélioration du processus BEE permet d'ajuster précisément les propriétés physiques de la couche de PGe en faisant varier les paramètres de gravure. Nous démontrons des structures de PGe avec une porosité allant de 40 % à 80 % et une épaisseur réglable de quelques nanomètres à plus de 4 μm, tout en préservant une faible rugosité de surface, offrant ainsi un large éventail de nanostructures de PGe répondant aux exigences pour des applications diverses. L'ellipsométrie et la réflectivité des rayons X ont été utilisées pour mesurer la porosité et l'épaisseur des couches de PGe, fournissant des méthodes de caractérisation rapides et non destructives. Ces découvertes posent les bases de la production à grande échelle de couches de PGe de haute qualité aux caractéristiques sur mesure.

Large-scale formation of uniform porous Ge nanostructures with tunable physical properties

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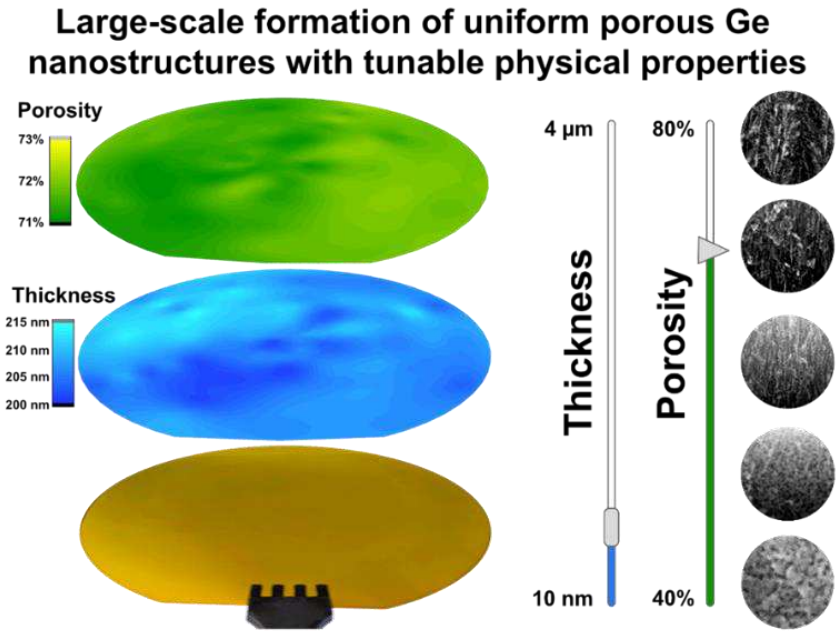
Keywords: Porous germanium, Nanostructures, Porous substrate, Wafer-scale, Electrochemical etching

4.3 Graphical abstract



4.4 Abstract

Porous germanium (PGe) nanostructures attract a lot of attention for various emerging applications due to their unique mechanical and physicochemical properties. Accordingly, there's an increasing need for the development of low-cost synthesis roots to ensure compatibility with large-scale production. Bipolar electrochemical etching (BEE) is a low-cost widely used solution to produce porous Ge layers. However, the lack of controllable production of large-scale uniform PGe layers is the main limiting factor for mainstream applications. This work demonstrates the formation of large-scale homogenous PGe layers by improving the BEE process. The produced porous structures, demonstrates excellent homogeneity in thickness and porosity with a relative variation below 2% over the entire 100 mm wafer. Furthermore, the improved BEE process enables accurate tuning of the physical properties of the PGe layer through the etching parameters variation. We demonstrate PGe structures with porosity ranging from 40% to 80% with an adjustable thickness from a few nm to over 4 µm, while preserving low surface roughness, giving access to a large variety of PGe nanostructures to fulfill the requirements of the widest possible range of applications. Ellipsometry and X-ray reflectivity have been employed to measure the porosity and thickness of PGe layers, providing fast and nondestructive

methods of characterization. These findings lay the groundwork for large-scale production of high-quality PGe layers with on-demand characteristics.

4.5 Introduction

Porous semiconductor materials have received an increasing interest for both fundamental research and advanced applications owing to their unique mechanical and physicochemical properties compared to their bulk material counterparts[221,253–255]. PGe in particular shows potential in a wide range of implementations such as energy storage systems[256–261], thermoelectric devices[262], sensors[263–265], optoelectronics[210,266] or synthesis of nanocomposite materials[267–269]. Moreover, PGe has recently been demonstrated as an efficient virtual substrate for epitaxial growth of detachable Ge membranes[182] and III-V heterostructures with high crystalline quality[214,216] paving the way to direct application in the development of lightweight and flexible photovoltaics and optoelectronics[183,270]. Nevertheless, to bring these applications to the real world, a large-scale formation of homogenous PGe layers with on-demand characteristics is necessary.

The fabrication of PGe nanostructures was demonstrated using techniques such as thermal reduction of GeO_2 nanoparticles[271], Oxidative Polymerization of the Deltahedral$[Ge_9]^{4-}$ Cluster[272], Spark processing[273], reduction–alloying–dealloying approach[274], ion implantation[275,276], growth by Molecular Beam epitaxy[266], coupled plasma chemical vapor deposition[277], metal-assisted chemical etching[278], lithography and dry etching[183], and electrochemical etching[203–205]. Some of the major challenges of the aforesaid techniques are confronted with the use of expensive precursors, high investment in equipment and labor, low yields, random crystallite orientation, low purity of PGe structures and intricate procedures making them nonviable for low-cost/large-scale production. The electrochemical etching is a simple and low-cost technique providing PGe layers with high material purity and densely packed nanocrystals. However, its wide-spreading application remains strongly dependent on the controllable production of homogenous PGe layer on large surfaces.

In the last two decades, the electrochemical porosification of Ge experienced major advancements. The BEE was introduced[208,279] to overcome the observed lateral

dissolution of the PGe[204] when applying a silicon-like unipolar anodic etching[280,281] on Ge substrate. Accordingly, adding a cathodization step allows passivating the porous layer formed during the previous anodization step. BEE produced PGe with various structures and morphologies has been reported by tuning BEE etching and passivation parameters[205,210,211]. Recently, the Fast BEE was introduced[203], allowing higher etching rates for thicker PGe layers production. Since then, this technique has been used to produce tubular and columnar morphologies[212], broadening the implementation of PGe as anode material for Li-ion batteries[282]. Despite the progress made in the fundamental understanding of the electrochemical etching of Ge[208,279,283] and the demonstrated suitability for various emerging applications, the formation of homogenous PGe layers on large surfaces and the control of its structural properties remain difficult to achieve because of the number of interfering factors during BEE. Indeed, parameters such as substrate characteristics, ratio etching/passivation pulse duration and current density or electrolyte composition have a strong impact on the final PGe properties (porosity, thickness, and morphology)[205,211]. Furthermore, PGe morphological characteristics (thickness and porosity) are often extracted using local and destructive techniques such as scanning electron microscopy (SEM), which are not suitable for large-scale assessment of the PGe homogeneity.

In this work, we demonstrate large-scale formation of homogenous PGe layers by a modified BEE. The proposed method allows fine-tuning and control of the porous layer thickness and porosity. Accordingly, widely tunable highly uniform PGe layer over full 100 mm wafers has been demonstrated. Additionally, we show that ellipsometry mapping and XRR are very accurate and nondestructive characterization techniques, to measure the PGe layer thickness and porosity.

4.6 Results and discussions

Ge electrochemical porosification requires the use of bipolar etching, where the anodic pulses enable effective etching, and the cathodic pulses protect the porous structure from dissolution during the etching step[208,279]. This additional complexity, compared to Si porosification, makes the formation of homogenous porous Ge layers by BEE very challenging. When applying standard symmetrical BBE process on a large surface, the

resulting layers exhibit inhomogeneous surface colors as demonstrated by Figure S4-1. A typical cross-sectional SEM image of porous Ge structures obtained by standard BEE process (Figure 4-1a) shows the lateral etching induced damages that locally alters the PGe layer's quality. The origin of this inhomogeneity can be attributed to an excessive formation of hydrogen gas during the BEE. The mechanism of Ge passivation step has already been described in previous works[203,211], showing that the formation of hydrogen terminations on the surface of the PGe structure, protects it against the dissolution during the subsequent etching step. As a by-product of this reaction, hydrogen gas is also formed inside the structure. The growth and evolution of H_2 bubbles generate a pressure on the pore walls inducing physical damages to the small and fragile PGe crystallites. Moreover, the large H_2 bubbles stuck inside the pores can isolate parts of the structure from the system, locally causing etching in lateral direction, which is detrimental for the porous layer homogeneity over the large surface. Figure 4-1b schematically illustrates the accumulation of the H_2 bubbles inside the porous structure and the consequent potential damage that may locally occur during the porous layer formation.

To overcome these undesirable passivation effects, we introduced some modifications to commonly used BEE conditions. Indeed, to reduce the quantity of produced H_2 gas, we employed a low passivation current density of 1 $mA \cdot cm^{-2}$. Additionally, a rest time has been introduced at the end of each etching/passivation cycle. The extra time after each cycle let the system reach the equilibrium potential as well as it enables the H_2 gas to escape from the porous structure as shown in Figure 4-1b. Moreover, the proportion of ethanol in the electrolyte is increased by 20% to reduce the surface tension of the solution[284]. This helps release the residual H_2 bubbles and facilitating the electrolyte penetration inside the nanoscale sized porous structure enabling an efficient diffusion of the ions towards the bottom of the pores. As a result, the introduced modifications increase the overall stability of the process, inhibiting the damage of the PGe layers during the etching while enabling homogenous PGe structures formation over large surfaces. Using this improved BEE recipe, well-defined PGe structure with good lateral and in-depth uniformity has been obtained as revealed by SEM micrograph (Figure 4-1c).

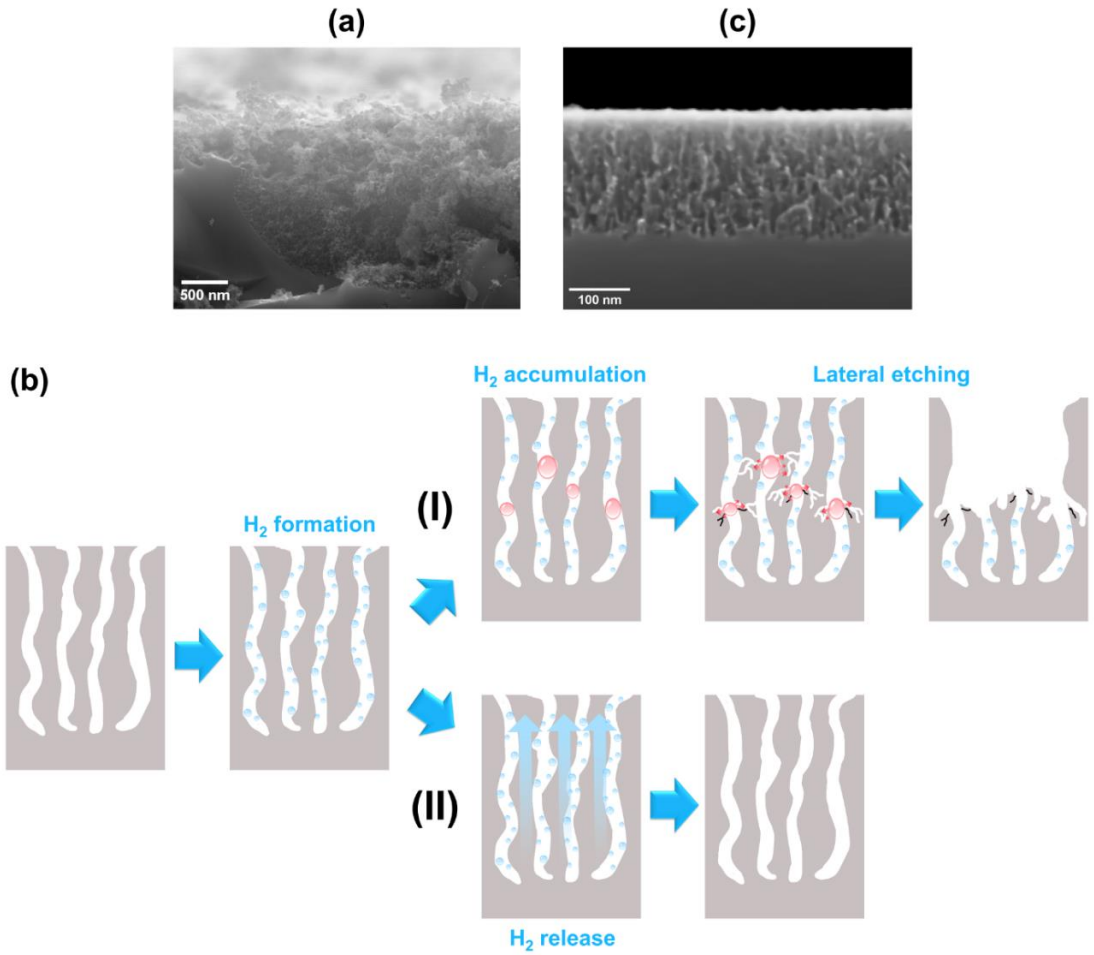


Figure 4-1: (a) Typical SEM micrograph of damaged PGe structure due to the lateral etching formed with 2 mA·cm^{-2} etching current density. (b) Schematic illustration of H_2 gas formation (I) accumulation of H_2 inside the porous structure and damage it causes due to the physical pressure and local insulation inside of pores causing lateral etching. (II) H_2 release during the rest time step in between etching cycles, preventing damage to the PGe structure. (c) SEM micrograph of well-defined PGe structure etched with improved BEE process and with 2 mA·cm^{-2} etching current density

To date conventional porosification cells for electrochemical etching of semiconductors employ a clamping mechanism to maintain the wafer inside the cell and to seal the reservoir for the electrolyte[204,285,286]. Figure 4-2a shows typical homogenous PGe layer produced in conventional 100 mm wafer porosification cell. Since the edge of the wafer is isolated from the electrolyte, it cannot be porosified leading to the formation of the rim of bulk material surrounding the porous structure. Moreover, the clamping mechanism causes

additional defects/inhomogeneities in the porous structure (as indicated by red arrows in Figure 4-2a) near the edges of the PGe layer. These combined effects reduce the effective usable surface of the wafer by over 25%, which is significant, especially in case of rare and expensive material such as Ge. Additionally, the interface between the bulk material and the porous structure can cause formation of defects, accumulation of materials and other problems for applications aiming for the use of full wafers such as epitaxial growth of heterostructures. To avoid these problems additional steps such as laser cutting or mechanical grinding to remove the rim[225] need to be undertaken, increasing the fabrication process's cost and complexity. Most industrial fabrication processes are developed to work with the whole wafers to ensure the highest possible efficiency. Consequently, any unusable parts of the substrate or additional steps will have a negative impact on the process throughput. To overcome this issue, we have developed custom design[287] of porosification cell enabling the porosification of the entire wafer's surface (edge included). Schematic illustration of this design is shown in Figure 4-2b along with the produced uniform edge-to-edge PGe layer on full 100 mm wafer (Figure 4-2c).

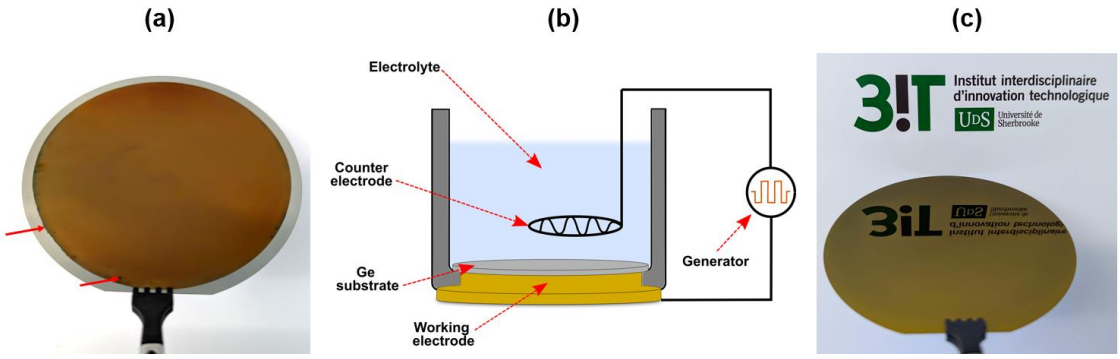


Figure 4-2: (a) 100 mm Ge wafer with homogenous PGe layer produced in conventional porosification cells. Red flashes indicate defects in PGe layer at the edges. (b) Schematic illustration of custom design porosification cell enabling edge-to-edge wafer porosification. (c) The edge-to-edge homogenous PGe layer with mirror finish produced in custom-made 100 mm cell.

To study the impact of the etching parameters on the PGe layer's uniformity, the etching current density was varied between 0.5 and 5.0 $mA \cdot cm^{-2}$. Indeed, as shown in Figure 4-3, the improved stability of the proposed BEE recipe enables the etching current density

variation while preserving the PGe layer's uniformity. Indeed, Figure 4-3a shows a linear increase of etching rate with etching current density. Compared to previously reported data[203], homogenous PGe layers can be produced even above 2.5 $mA \cdot cm^{-2}$ effectively avoiding the lateral dissolution at high etching current density. This allows for achieving high etching rates of above 40 nm/min, being previously reported only by fast BEE[203]. Moreover, for a given current density, the PGe layer thickness is found to increase linearly over time (Figure 4-3b). This testifies that the etching rate remains constant during the BEE process. This characteristic enables time-based thickness modulation of PGe layers from few nm up to 4 µm. Furthermore, the porosity can be successively tuned from 40 to 80% by varying the etching current density within the selected range, providing the formation of adjustable medium to high porosity (Figure 4-3c). Two main porosification regimes can be distinguished: (I) From 0.5 to 2.0 $mA \cdot cm^{-2}$, porosity exhibits high sensitivity to the etching current density, enabling a wide range of porosity variation between 40 and 70% (II). Meanwhile, for an etching current density ranging from 2.0 to 5.0 $mA \cdot cm^{-2}$, the porosity is found to vary only between 70 and 80% allowing very fine porosity modulation in this regime.

For all porosities the PGe structure is formed by interconnected mesopores, separated by Ge skeleton. Although the pores are disordered at a short range, a certain degree of ordering can be detected at a long range, particularly in the case of high porosities (Figure 4-3d-i). This shows that the PGe layers maintain its sponge-like morphology, regardless of the etching current density. This is possible thanks to the high degree of passivation. Other morphologies such as "pine-tree" and "fishbone", have been reported in the literature for lower degrees of passivation[211]. While the porosity of the PGe layer varies as a function of the etching current density, the pore size seems to remain the same as shown by the cross-sectional SEM images of PGe structures with porosities between 40% and 80% in Figure 4-3d-i. The image processing reveals an average pore diameter, around 5 ± 1 nm across all the porosities. This value is consistent with the observations by transmission electron microscopy (TEM) presented in Figure 4-5a as well as with the values indicated in literature[203,211]. The obtained average pore size classifies at the lower end of the mesoporous size domain. The provided flexibility in tuning of PGe structure's physical properties enables the possibility of on-demand porous layer

formation, depending on the desired characteristics. Many applications can take advantage of this kind of versatility such as energy storage systems[258], thermoelectric devices[262] or nanoengineered compliant substrates for epitaxial growth[183,214].

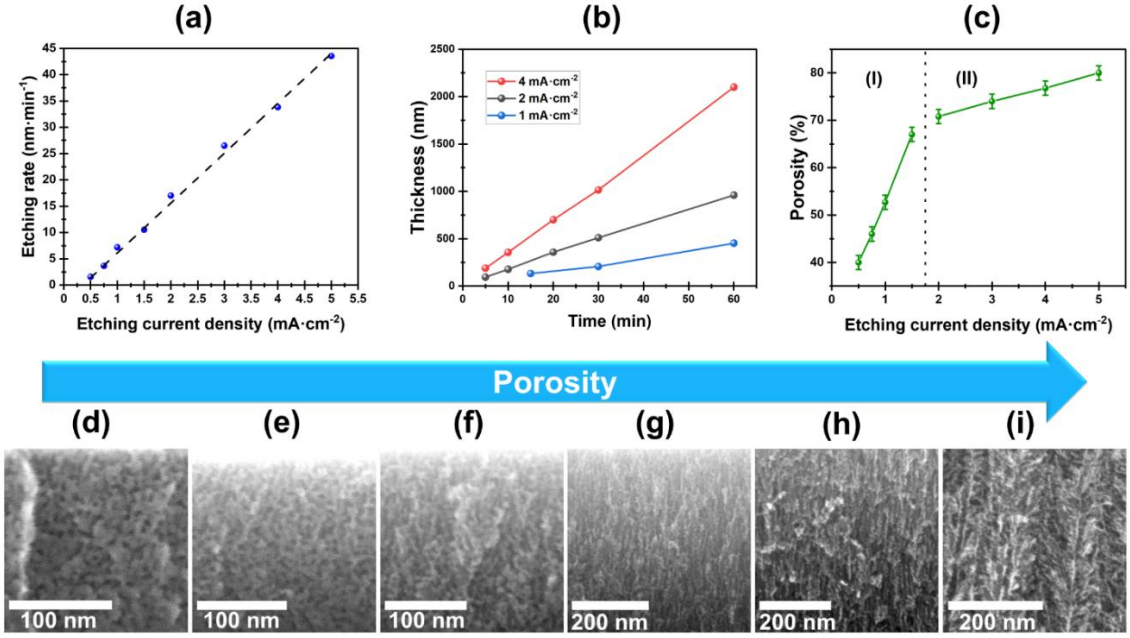


Figure 4-3: (a) Linear growth of etching rate of PGe layers with increasing current density. (b) Linear increase of PGe layer thickness over etching duration for 1, 2 and 4 mAc·m^{-2} etching current density. (c) Porosity of the PGe structure versus applied etching current density variation with (I) corresponding to the domain with fast porosity increase from medium to high porosity and (II) to slow progressive increase in high porosity domain. (d-i) Cross-sectional SEM micrographs of PGe structures etched with 0.50, 0.75, 1.00, 1.50, 2.00 and 5.00 mA·cm^{-2} corresponding to 40, 45, 53, 65, 71 and 80% porosity, respectively.

The demonstration of wafer-scale production and use of porous Ge substrates for various applications, comes with a crucial need to develop fast and nondestructive characterization methods easily applicable for post-production PGe wafers' quality assessment. To date, PGe layers are mainly characterized by SEM. Accordingly, we have employed this method on various locations along the PGe wafer's diameter as reference data to assess the accuracy of the nondestructive characterization techniques. Figure 4-1c shows a well-defined interface between the PGe layer with sponge-like morphology and bulk Ge material. The Figure 4-4a shows that the PGe layer thickness remains constant along the wafer's diameter with a mean value of 206 ± 4 nm (Figure 4-4b). SEM can also

be used to evaluate the porosity, using image treatment software, which is estimated in the present case to be 67 ± 12%. To assess this estimation using nondestructive technique, we first employed XRR measurement to precisely determine the porosity. Indeed, it allows for measuring the critical angle of porous layer, which is directly linked to the material's density and therefore its corresponding porosity. As the porosity of the layer increases the value of critical angle decreases. This enables the distinction between the critical angle of PGe layer (θ_{PGe}) and of the bulk Ge (θ_{Ge}) as shown in Figure 4-4b. The porosity can therefore be calculated using Eq. 1. Variation of PGe critical angle with porosity is shown in Figure S4-2 of supplementary materials. XRR enables non-destructive determination of porosity without relying on indirect image processing algorithms. Figure 4-4c shows radial profile of porosity of full wafer with an average value of 72 ± 2%. This result agrees with the estimation made by SEM images treatment. These methods give us good indication about the uniformity of the PGe layers, but they are still, not suitable for the fast feedback loop necessary for large-scale production.

Regardless of the precision and the accuracy of the provided information (layer's porosity, thickness, and homogeneity), SEM remains local and destructive method, which is non-representative of the whole PGe wafer's surface and unsuitable for quality control in production line. On the other hand, XRR is non-destructive and production-line compatible, but it doesn't offer reliable measurement of the PGe thickness. For this reason, we employed more complete fast and non-destructive ellipsometry measurements to access both thickness and porosity at the same time. Mapping with over 100 measurement points was performed to evaluate the uniformity of the PGe over the entire 100 mm wafer as shown in Figure 4-4d and 4-4e. The mean thickness of the PGe layer is evaluated to be 207 ± 3 nm (Figure 4-4d). In terms of porosity, the mean value is 72 ± 1% as shown in Figure 4-4e. These results demonstrate excellent uniformity of the PGe layer over the wafer's surface with a standard deviation below 2% for both thickness and porosity obtained by custom-designed porosification cell and optimized BEE recipe (similar results are obtained for medium porosity layers as shown in Figure S4-3). Moreover, the obtained data are consistent with both SEM and XRR measurements, making the ellipsometry mapping a fast, accurate and nondestructive technique suitable for fast feedback characterization of PGe layers.

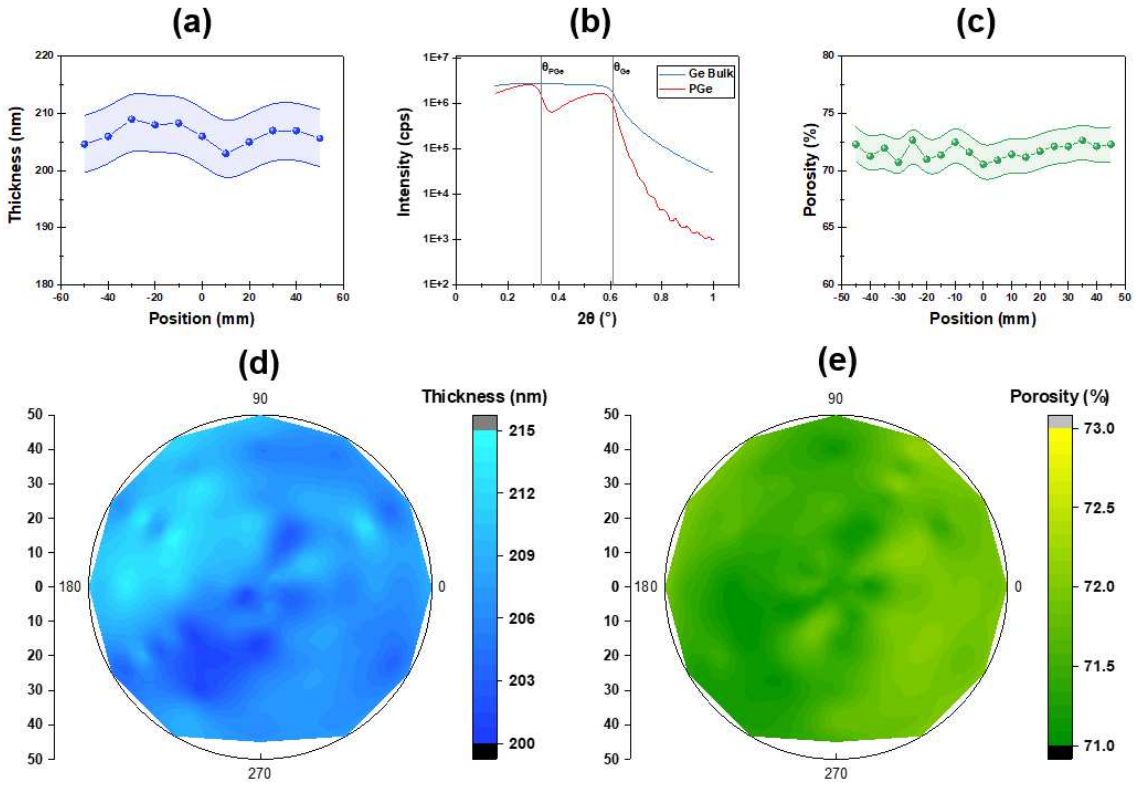


Figure 4-4: (a) Thickness variation of the PGe layer over the diameter of 100 mm wafer measured by SEM. (b) Typical XRR measurement of the Ge bulk substrate (Blue) and PGe layer (Red). (c) Porosity variation of the PGe layer over the diameter of the 100 mm wafer calculated from XRR measurements d) and e) mapping of the thickness and porosity of the PGe layer over the surface of 100 mm wafer measured by ellipsometry.

For applications such as epitaxial growth, the crystalline quality and surface morphology are crucial characteristics of the substrate. To further quality investigation of fabricated PGe layers HRTEM (High-Resolution Transmission Electron Microscopy), XRD and AFM are used. The HRTEM image of a typical PGe structure made by BEE (Figure 4-5a) shows Ge atoms oriented in crystalline structure without any observable presence of amorphous phase or oxides on the surface of the crystallites. To investigate if there is any bending of the crystallites in the PGe structure, a PGe layer with ~70% porosity and ~1 µm thickness is characterized by XRD, since the high porosity and thickness make this type of structure most keen to crystal bending and misorientation. Figure 4-5b shows 2θ out-of-plane XRD scan with only (004) and (002)[288] peaks of Ge, without signs of any other orientations. Combined, the HRTEM and XRD studies demonstrate the

crystalline nature of the porous structure, maintaining the substrate orientation without formation of any amorphous phase or crystal bending. Furthermore, Figure 4-5c shows a typical AFM scan of the PGe layer's surface topology of the sponge-like structure showing a smooth surface and low RMS (Root Mean Square) roughness below 3 nm. AFM scans for various PGe structures can be found in Figure S4-4 of supplementary materials. These surface characteristics were found to be the same for all the produced porous structures independently of their porosity as can be seen in Figure 4-5d. The high single oriented crystallinity combined with low surface roughness and good lateral uniformity make these PGe layers an excellent candidate as virtual substrate for wafer-scale epitaxy. Recently, it has been demonstrated that, as porosified PGe substrates allow epitaxial growth of monocrystalline Ge membranes[289]. It has been also showed that native oxides, which may be formed on PGe surface following a long storage time and/or longer period of exposure to the ambient atmosphere, can be easily removed by diluted acidic solutions such as HBr. Oxide-free PGe surface can be obtained, allowing monocrystalline Ge growth on top of it[290].

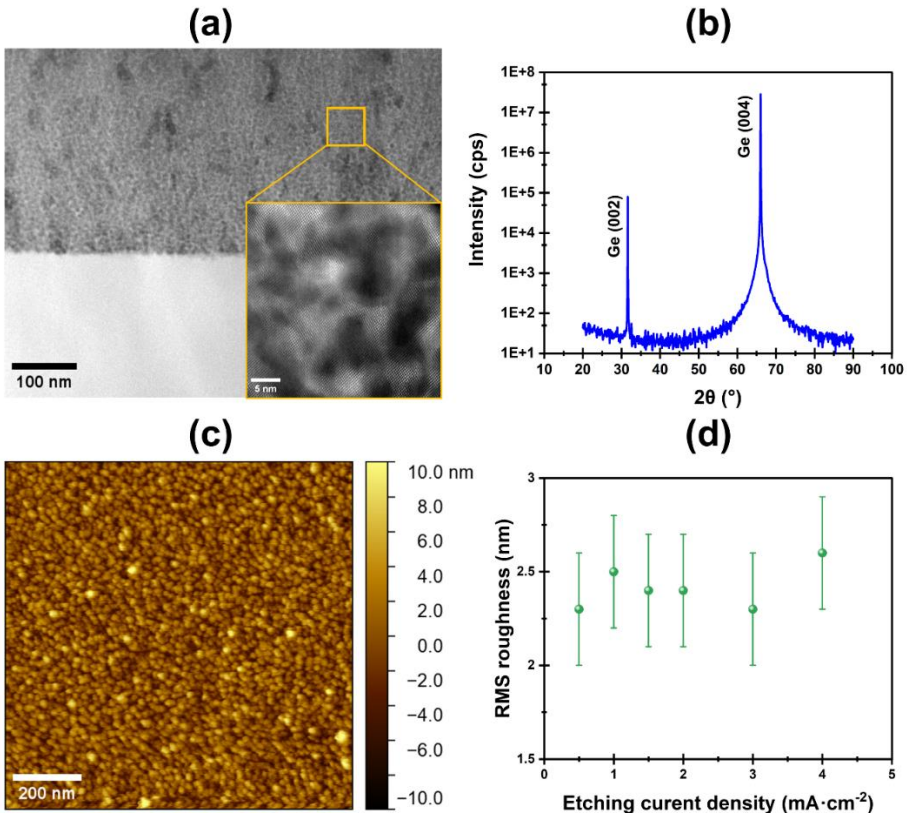


Figure 4-5: (a) HRTEM micrograph of high porosity structure showing the crystalline nature of the porous structure (b) 2θ out-of-plane XRD scan of the thick, high porosity PGe layer showing monocrystalline nature of the structure (c) AFM scan showing smooth surface morphology of the PGe layer. (d) Constant surface roughness of the PGe layers versus etching current density (Porosity).

4.7 Conclusion

We demonstrated the fabrication of edge-to-edge, 100 mm wafer-scale, homogenous and reproducible PGe layers. This is possible, thanks to a finely optimized BEE process with an additional rest time step to enable efficient evolution of H_2 produced during the passivation step. The edge-to-edge scale is enabled by custom designed porosification cell increasing the high-quality PGe surface by over 25% per 100 mm wafer compared to conventional porosification cells. Moreover, we show that the PGe structural properties such as thickness and porosity can be accurately tuned by varying the etching parameters to create PGe layers with on-demand characteristics depending on the desired application. The produced PGe layers' properties are easily assessable by production line compatible,

fast, and nondestructive techniques enabling the characterization of the entire surface. The resulting PGe layers present excellent homogeneity with less than 2% variation for both thickness and porosity. The HRTEM and XRD analysis shows that the PGe structure maintains the substrate crystalline nature, without any misorientation of the crystallites. Moreover, the porous substrates show a good surface topology with RMS roughness below 3 nm over the entire range of accessible porosities. This provides an opportunity for wafer-scale epitaxial growth of detachable III-V heterostructures for optoelectronics and photovoltaics applications. These results demonstrate the viability of BEE for large-scale production of high purity, crystalline PGe layers with on-demand characteristics and lay the groundwork for various applications of PGe structures.

4.8 Methods

4.8.1 Bipolar Electrochemical Etching

Electrochemical etching of Ge was performed in a custom-designed 100 mm electrochemical cell, composed of Teflon body, solid copper working electrode and platinum wire counter electrode. Gallium doped, p-type (100) oriented Ge wafers with 6° miscut towards (111) direction and resistivity of 8-30 mΩ·cm were used as a substrate. Prior to a Galvanostatic BEE, Ge wafers were deoxidized in the HF (49%) solution for 5 min, rinsed with EtOH (99%, Anhydrous) and dried under N_2 flow. The BEE was carried out in HF (49%): EtOH (99%, Anhydrous) (4:1, V:V) electrolyte using asymmetric anodic (etching), cathodic (passivation) pulses and 1 s rest time at the end of each cycle. The passivation pulses were fixed at 1 $mA \cdot cm^{-2}$ current density and 1 s pulse duration. The etching current density varied between 0.5 and 5.0 $mA \cdot cm^{-2}$ with pulse duration fixed at 1 s. Prior to BEE, a direct current was applied to initiate the formation of pores and to obtain their even distribution on the sample surface[203]. The total duration of BEE varied between 2 min and 1 h.

4.8.2 Materials Characterization

Cross-sectional profile of samples was observed by scanning electron microscopy (SEM) using Zeiss LEO 1540 XB at 4.3 mm of working distance and 20 keV of acceleration voltage, to measure the thickness of the layer. The roughness measurements

were performed, using the AFM Veeco Dimension 3100 in tapping mode with SSS-NCHR silicon probe and with a scan size of 5 × 5 and 1 × 1 μm^2. The X-ray diffraction (XRD) and X-ray reflectometry (XRR) measurements were performed using Rigaku Smartlab HRXRD system with Cu Kα X-ray source, Ge (220) × 2 monochromator and HYPIX-3000 hybrid pixel array 2D detector. The Powder XRD configuration was used to investigate the crystalline nature of the PGe layer. The XRR is used to measure the critical angle of PGe layers. The porosity (P) is then calculated using Equation 4-1 where θ_{PGe} and θ_{Ge} correspond to the critical angle of the PGe layer and of the bulk Ge, respectively[291,292].

$$P = (1 - (\frac{\theta_{PGe}}{\theta_{Ge}})^2) \times 100 \qquad \text{(Equation 4-1)}$$

Fast feedback characterization of 100 mm wafers of PGe was performed by ellipsometry using a J. A. Woollam Co. VASE® instrument, including mapping of the wafers. Spectral range from 500 nm to 900 nm and a model based on an Effective Material Approximation (EMA) using the Bruggerman analysis mode. This model uses a mix of Ge and air to represent the PGe layers on a Ge substrate[293], allowing thickness and porosity estimation. Ge material uses a Cody-Lorentz built-in function to model the dielectric model of Germanium as a wavelength-dependent oscillator[294,295], we used E_0 and E_g as 6 eV and 1 eV respectively.

4.9 Author Contributions

The manuscript was written through the contributions of all authors. All authors have given approval to the final version of the manuscript. **Tadeáš Hanuš**: Conceptualization, Methodology, Investigation, Data curation, Original draft preparation, Review and Editing, Visualization. **Javier Arias Zapata**: Investigation, Supervision, Validation, Review and Editing. **Bouraoui Ilahi**: Supervision, Validation, Review and Editing. **Philippe-Olivier Provost**: Conceptualization, Review and Editing. **Jinyoun Cho, Kristof Dessein**: Validation, Review and Editing. **Abderraouf Boucherif**: Supervision, Validation, Review and Editing.

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4.11 Supplementary materials

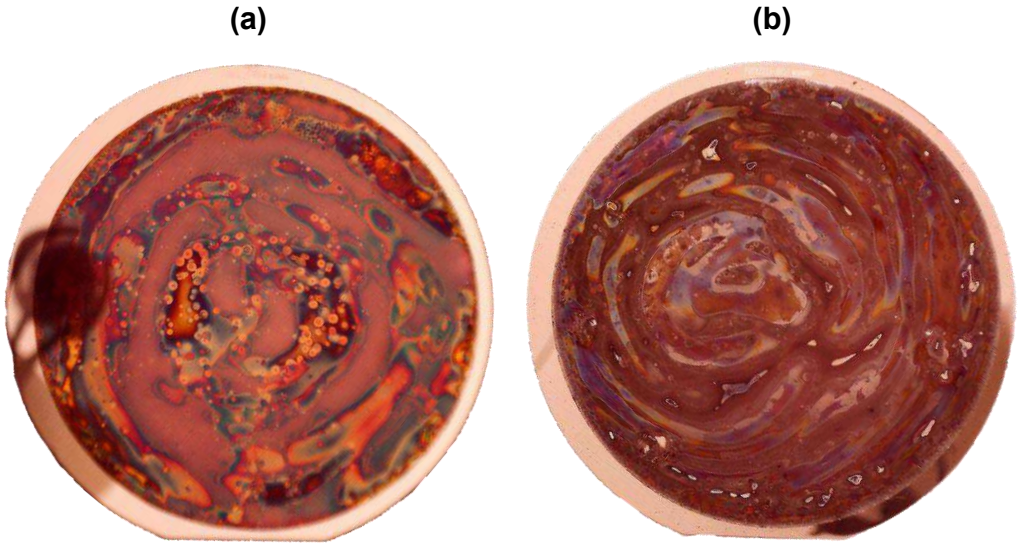

Figure S4-1: Optical image of PGe layers over 100 mm wafer using standard symmetrical BEE recipe with (a) 1.5 mA·cm^{-2} etching current density and (b) 2.0 mA·cm^{-2} etching current density. Both images show large inhomogeneous areas of the PGe layer.

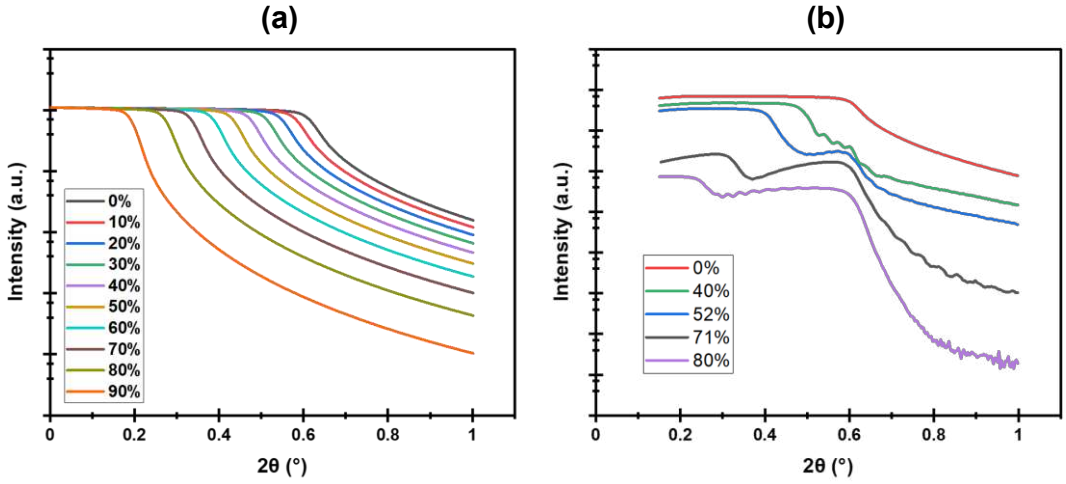

Figure S4-2: (a) Simulation of XRR for infinite PGe layers with porosities between 0-90%, showing decreasing critical angle with increasing porosity (b) XRR measurement of PGe layers with different porosities, showing constant critical angle of the substrate and critical angle of the PGe layer decreasing with increasing porosity of the layer.

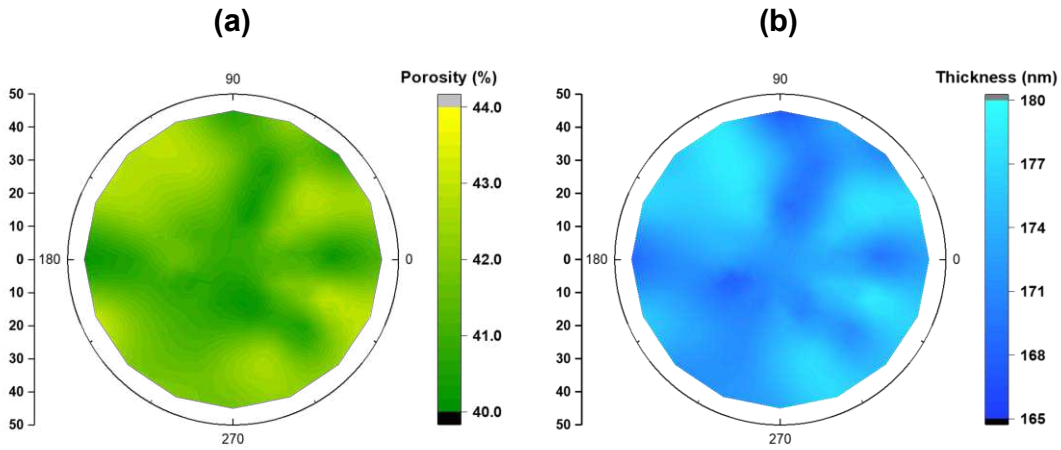

Figure S4-3: (a-b) mapping of the thickness and porosity of PGe layer, etched with 0.5 mA·cm^{-2} current density, over the surface of 100 mm wafer, measured with ellipsometr[290].

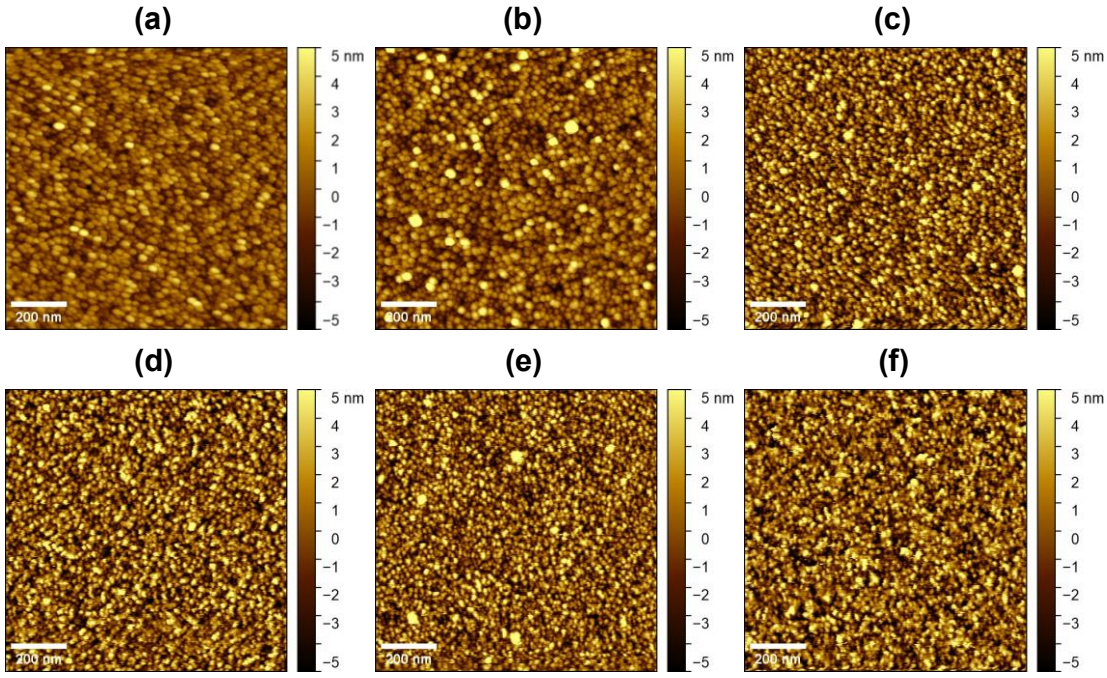

Figure S4-4: Surface topology AFM scans of PGe layers prepared with etching current density corresponding to (a) 0.50 mA·cm^{-2}, (b) 0.75 mA·cm^{-2}, (c) 1.00 mA·cm^{-2}, (d) 1.50 mA·cm^{-2}, (e) 2.00 mA·cm^{-2}, (f) 4.0 mA·cm^{-2}.

Chapter V

5. Growth on PGe Substrates and Fabrication of Monocrystalline Ge FSMs

This chapter focuses on epitaxial growth of Ge layers on PGe substrate and fabrication of Ge FSMs. The chapter is in form of scientific article published in the journal *Materials Today Advances*. It explores the initial stage of the growth on PGe interface and the evolution of the surface quality of the fully densified Ge layer. The low-temperature growth allows for high-quality growth, while avoiding the reconstruction of the PGe nanostructure. This facilitates both the formation of the FSMs by mechanical detachment, as well as the substrate reuse.

5.1 Foreword

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French title: Membranes autoportantes de Ge à l'échelle de la plaque de 100 mm pour l'optoélectronique léger et flexible

Contribution to the manuscript:

This article contributes to the thesis by introducing a novel approach for Ge FSMs fabrication and substrate reuse. To demonstrate a low temperature growth on PGe structures, allowing an easy detachment of the membrane and simple substrate cleaning process for its reuse. It also showcases the different growth stages on 3D porous substrate leading to the formation of the fully densified, high-quality membrane.

5.2 French abstract

Les membranes autoportantes (FSMs) à base de semi-conducteurs ont récemment émergé comme un domaine très prometteur de recherche sur les matériaux avancés. Leurs propriétés uniques, telles que leur légèreté et leur flexibilité, les rendent attrayantes pour une large gamme d'applications de dispositifs innovants. Cependant, la production de FSMs de haute qualité cristalline, en particulier à partir de matériaux élémentaires tels que le germanium (Ge), reste un défi important. Dans ce travail, nous rapportons la formation de FSMs de Ge facilement détachables de leur substrat à l'échelle de la plaquette, à l'aide du substrat poreux de Ge (PGe). La méthode proposée repose sur l'épitaxie du Ge à basse température sur une structure PGe, ce qui permet de préserver l'intégrité de la structure poreuse lors de la formation de la FSM et facilite le nettoyage du substrat après le détachement pour la réutilisation multiple. L'analyse de la morphologie de la surface en fonction de l'épaisseur de Ge déposée révèle que la formation de la FSM se produit en deux régimes distincts. Pendant le régime initial, la croissance du Ge est régie par la nucléation 3D à la surface supérieure du PGe. Lors de cette étape, des ilots en surface croissent, augmentant la rugosité de surface jusqu'à une épaisseur critique qui permet la coalescence complète des ilots en une couche épitaxiale 2D. Par la suite, la croissance continue en mode couche par couche. L'analyse de la morphologie de surface des membranes pour différentes épaisseurs montre une amélioration continue, atteignant une rugosité de surface subnanométrique. De plus, nous démontrons que ce processus de formation des FSMs est applicable, quelles que soient la porosité et l'épaisseur du substrat PGe, tout en offrant un reconditionnement facile et durable du substrat pour générer de multiples FSMs à partir du même substrat. Nos découvertes ouvrent de nouvelles opportunités pour la production des dispositifs optoélectroniques légers, flexibles et de haute performance basée sur des FSMs de Ge, tout en assurant une réduction à la fois des coûts et de la consommation de matériaux critiques.

Wafer-scale Ge freestanding membranes for lightweight and flexible optoelectronics

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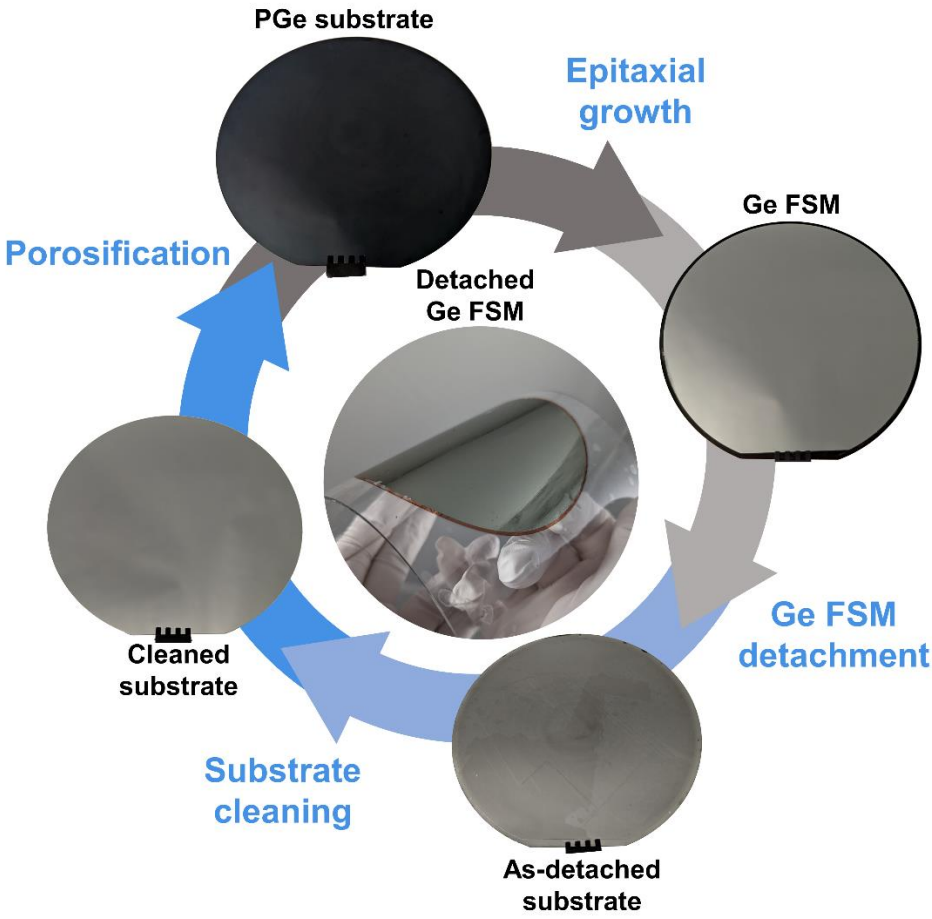
Keywords: Germanium, Porous substrate, Freestanding membranes, Epitaxial growth, Layer transfer, substrate reuse

5.3 Graphical abstract



5.4 Abstract

Semiconductor-based freestanding membranes (FSMs) have recently emerged as a highly promising area of advanced materials research. Their unique properties, such as lightweight and flexibility, make them attractive for a wide range of disruptive device applications. However, the production of high-quality, single-crystalline FSMs, especially from elemental materials such as germanium (Ge), remains a significant challenge. In this work, we report on the formation of easily detachable wafer-scale Ge FSM on porous Ge (PGe) substrate. The proposed method relies on low-temperature Ge epitaxy on a PGe structure, allowing for the preservation of the porous structure's integrity during the FSM formation allowing easy substrate preparation for multiple reuses. Analysis of the surface morphology as a function of the deposited Ge thickness reveals that the FSM formation occurs in two distinct regimes. During the initial epitaxial regime, the Ge growth is

governed by 3D nucleation on the PGe top surface. The nanoscale islands size increase, and consequent coalescence are found to increase the surface roughness up to a critical thickness, allowing full coalescence of islands into a 2D epilayer. The analysis of the membrane's surface morphology for various thicknesses shows continuous improvement, achieving sub nanometer surface roughness. Moreover, we demonstrate that the FSM formation process is applicable regardless of the PGe porosity and thickness, while offering facile and sustainable substrate reconditioning for multiple FSMs generation from the same substrate. Our findings open new opportunities to produce lightweight and flexible, high-performance optoelectronics based on Ge FSMs, while ensuring reduction of both cost and critical material consumption.

5.5 Introduction

In recent years, high-quality freestanding membranes (FSMs) made of functional materials have become central to the rapidly expanding frontiers of nanoscience and technology[297–302]. Group IV, III-V and III-N semiconducting membranes in particular have high potential for applications such as stretchable on-skin electronic[40,303], vertically stacked LEDs[3], and flexible photodetectors[304]. Indeed, FSMs offer an extra degree of freedom for implementations that cannot be obtained by conventional techniques such as heterointegration of dissimilar materials with high lattice mismatch in crystalline structures[305]. In addition to being lightweight and flexible, FSMs allow for various materials to be stacked on top of each other, enabling easy coupling of physical properties between dissimilar materials[306,307]. Furthermore, the use of FSMs provides significant cost savings for the device production, especially for materials with orders of magnitude higher prices than that of silicon, when compared to bulky wafers. In this context, germanium (Ge) FSMs particularly attract a lot of attention for their applications in high-performance optoelectronics and high-speed telecommunication devices such as wave guides[308,309], THz transmission[310], photodetectors[311–313] and lasers[314,315] as well as for their biocompatibility[316,317]. However, the fabrication of high-quality Ge FSM is still a challenging task.

For instance, remote epitaxy has shown tremendous potential for fabrication of III-N and III-V semiconductor compounds FSMs[318–320], and for other materials such as

complex oxides[65], perovskites[321], metals[80]. Nevertheless, this technique is based on ionic interaction between the epilayer and the underling substrate trough the graphene interface, prohibiting its application to non-polar materials such as Ge. To this date, a variety of lift-off techniques allowing the production of single-crystalline Ge FSMs and the reuse of wafers have already been reported, namely epitaxial lift-off (ELO)[322,323], mechanical spalling[160], smart cut method[324], growth on nanopatterned graphene[147], Germanium-on-nothing (GoN)[182,183] or porous lift-off[214,216,290]. Despite achieving significant advancements, the widespread adoption of Ge FSMs is still hindered by various obstacles including process complexity, high cost and substrates damage and/or contamination issues. Epitaxial growth on porous Ge (PGe) substrate has specially demonstrated high potential to produce lightweight solar cells[183,216]. The device detachment is achieved through the mechanically weak interface, formed by nano- to microscale-sized pillars[183,216,290]. After FSM detachment, the substrate surface contains broken pillars with various sizes whose reconditioning for multiple reuses require either conventional chemical mechanical polishing (CMP) treatment[224] or wet chemical etching over several microns[325]. Despite the significant improvement compared to the use of conventional wafers, these techniques still leave room for further reduction of both cost and Ge consumption during the reconditioning process.

Indeed, porous Ge (PGe) substrates offer a wide range of morphologies and physical properties[203,205,211,212], that can be directly used in the Ge FSM fabrication by epitaxial growth on an unreconstructed porous structure. Compared to the homoepitaxial growth on conventional substrate, where optimum 2D layer-by-layer growth can be easily reached, several challenges occur for nanostructured substrates. In fact, nanopores mediated epitaxial material diffusion[221] and porous reconstruction induced 3D micro-structuring[220] are among the encountered difficulties. These obstacles need to be overcome to ensure the epitaxial growth of FSM on PGe substrate. So far, successful epitaxy on PGe substrates is mainly based on high temperature annealing steps either before[182,183,214,216] or during the material deposition growth[290], triggering the thermal reconstruction of the porous layer. For instance, PGe with sponge-like morphology show a strong temperature dependence[223], inducing the formation of large pillars[290]

structures, while losing its intrinsic PGe properties and complicating the reconditioning process[325].

In this work, we demonstrate easily detachable wafer-scale Ge FSMs formation on PGe substrate by low temperature growth. The method, based on the preservation of the porous structure's integrity, is applicable regardless of the PGe porosity and thickness while ensuring easy substrate preparation for multiple reuses.

5.6 Results and discussions

The PGe substrates, used for epitaxial growth, are prepared by bipolar electrochemical etching (BEE) of the P-type Ge substrate, in the HF-based electrolyte. The process, which was reported in our previous work[252], enables fine-tuning of the PGe thickness and porosity, providing on-demand properties while ensuring a low surface roughness and a substrate oriented crystalline nature, making them a viable option for epitaxial growth. The produced PGe thickness and porosity demonstrate an overall variation standing below 2% across the wafer. Figure 5-1a depicts an optical image of a typical 100 mm Ge substrate, with homogenous porous layer on top, produced by BEE. To shed light on the initial stages of the Ge epitaxy on PGe nanostructures, we first consider 230 nm-thick uniform PGe layers (Figure 5-1c) over 100 mm Ge wafer with intermediate porosity around 54%, calculated from the critical angle measured by X-ray reflectivity[252] (Figure 5-1b), and having a surface RMS (root mean square) roughness below 2 nm (Figure S5-1). All the investigated samples have been grown at 300 ºC in Chemical beam epitaxy reactor (CBE) equipped with solid source Ge. The growth rate has been maintained constant throughout this study at 0.5 µm/h. Additionally, since our objective is to perform epitaxial growth of Ge on PGe structure, the growth temperature needs to be sufficiently low to avoid PGe reorganization as discussed further below.

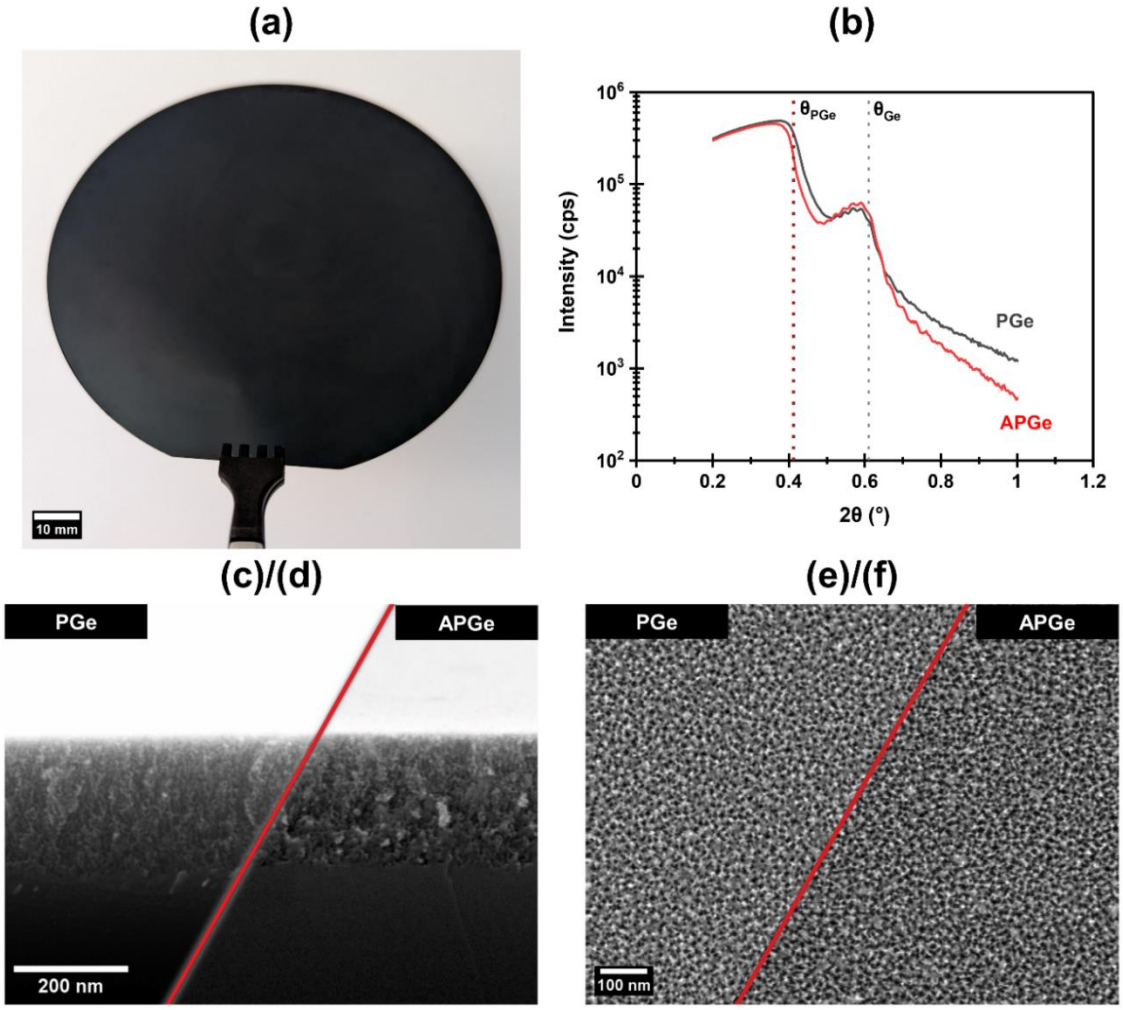


Figure 5-1: Evaluation of the PGe layer quality before and after the annealing at 300 °C during 30 min. (a) An optical image of a typical uniform PGe layer on 100 mm wafer. (b) XRR measures of PGe layer before and after annealing at 300 °C, the critical angles of both PGe layer(θ_{PGe}) and Ge substrate(θ_{Ge}) are indicated by dotted lines. (c)/(d) and (e)/(f) depict the top view and cross-sectional SEM micrographs of PGe layers before (PGe) and after annealing at 300 °C (APGe) respectively.

To evaluate the stability of the porous structure at the growth temperature, the PGe substrate has been first in-situ annealed at 300 °C for 30 min and characterized by XRR, scanning electron microscopy (SEM) and atomic force microscopy (AFM). Figure 5-1b shows XRR measurement of the porous Ge layer before and after annealing, with a negligible shift of the PGe layer critical angle (θ_{PGe}), from 0.414° to 0.410° (less than 1% increase of porosity), signifying that the porosity remains unchanged. Furthermore,

Figure 5-1 c-f depict cross-sectional and top-view SEM images, showing identical in-plane and in-depth porous morphologies before and after the annealing step. The surface RMS roughness does not undergo any major changes either, with only a slight increase from 1.1 nm to 1.6 nm. (Figure S5-1). Accordingly, Ge epitaxial growth can be performed on PGe substrate while preserving the porous structure integrity. For growth temperatures of 350 °C and above, morphological transformation of the PGe has been found to occur, making it unsuitable for the present work.

To study the initial growth stages and understand the Ge nucleation on PGe substrates, several samples have been prepared with deposited Ge nominal thicknesses ranging from 5 nm to 1 µm. The morphological evolution of the epilayers was systematically evaluated as a function of the nominal thickness of Ge on the PGe structure and characterized via SEM and AFM. Typical cross-sectional and top-view SEM images taken from samples with 5, 30, 60 and 100 nm deposited Ge thicknesses are shown by Figure 5-2a-d and Figure 5-2e-h respectively (Additional data are provided in Figure S5-2). The results reveal that the nucleation occurs on the top surface of the pore walls, forming nanoscale three-dimensional (3D) islands (Figure 5-2a and 5-2e). The combined low substrate temperature and small pores' size (below 10 nm) is likely to limit the adatoms diffusion into the porous structure[326] in favor of top surface nucleation. As more material is added, the 3D island's size increase, eventually coalescing to form a 2D Ge membrane (Figure 5-2b and 5-2f). Although, the densely packed nucleation enables continuous Ge membrane formation, the corresponding surface morphology remains rough as can be seen in Figure 5-2c and 5-2g). The observed behavior is also confirmed by AFM morphological investigations (Figure 5-3 and Figure S5-3). Indeed, the analysis of the RMS roughness indicates that the roughness rises first, with increasing Ge thickness up to 60 nm and then drops rapidly towards surfaces with sub nanometer roughness for membranes with thicknesses above 750 nm.

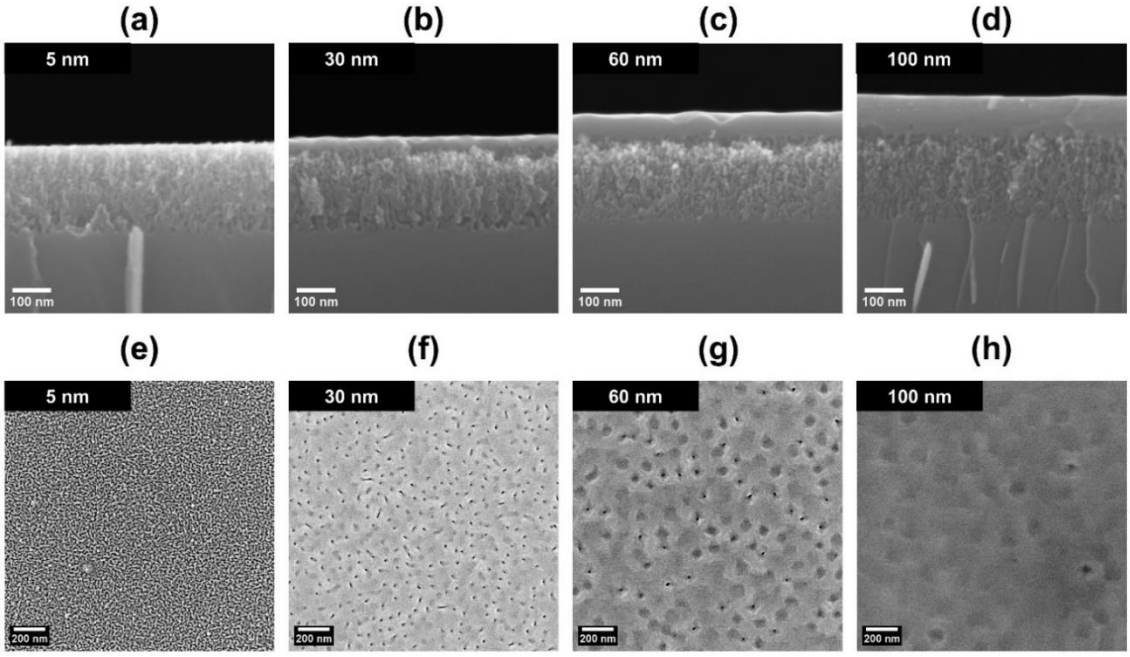


Figure 5-2: Initial growth stages of Ge on the PGe substrate (a-d) cross-sectional and (e-h) top view SEM micrograph of Ge layer at 5/30/60/100 nm of grown nominal thickness.

Additionally, during the Ge nucleation on PGe structure, the first islanding regime starting with 3D nucleation, considerably impacts the surface morphology through islands size increase and consequent seed island coalescence, leading to the observed RMS roughness increase. As shown by the Figure S5-3, the coalescence of the nanosized islands occurs for deposited Ge thicknesses higher than 10 nm giving rise to the appearance of pits. The islanding phase has been reported in case of low temperature growth of Ge on porous Si substrate[327]. However, in the latter case, the lattice mismatched strain and the differences in the thermal expansion coefficients have been shown to induce grain boundary formations that prohibits the full island coalescence into homogeneously dense epilayer. Moreover, similar behavior has already been reported at micrometer scale, where persistent separated microcrystals occur for Ge growth on Si micropillars[326], while good quality suspended Ge layers can be achieved by high temperature epitaxy/annealing on Ge micropillars[182]. Furthermore, the formation of a good quality dense epilayer has also been recently reported by GaN nucleation on porous GaN buffer on sapphire substrate[222], suggesting that the homoepitaxial growth is a key for obtention of fully coalesced layers on porous substrates at low temperature.

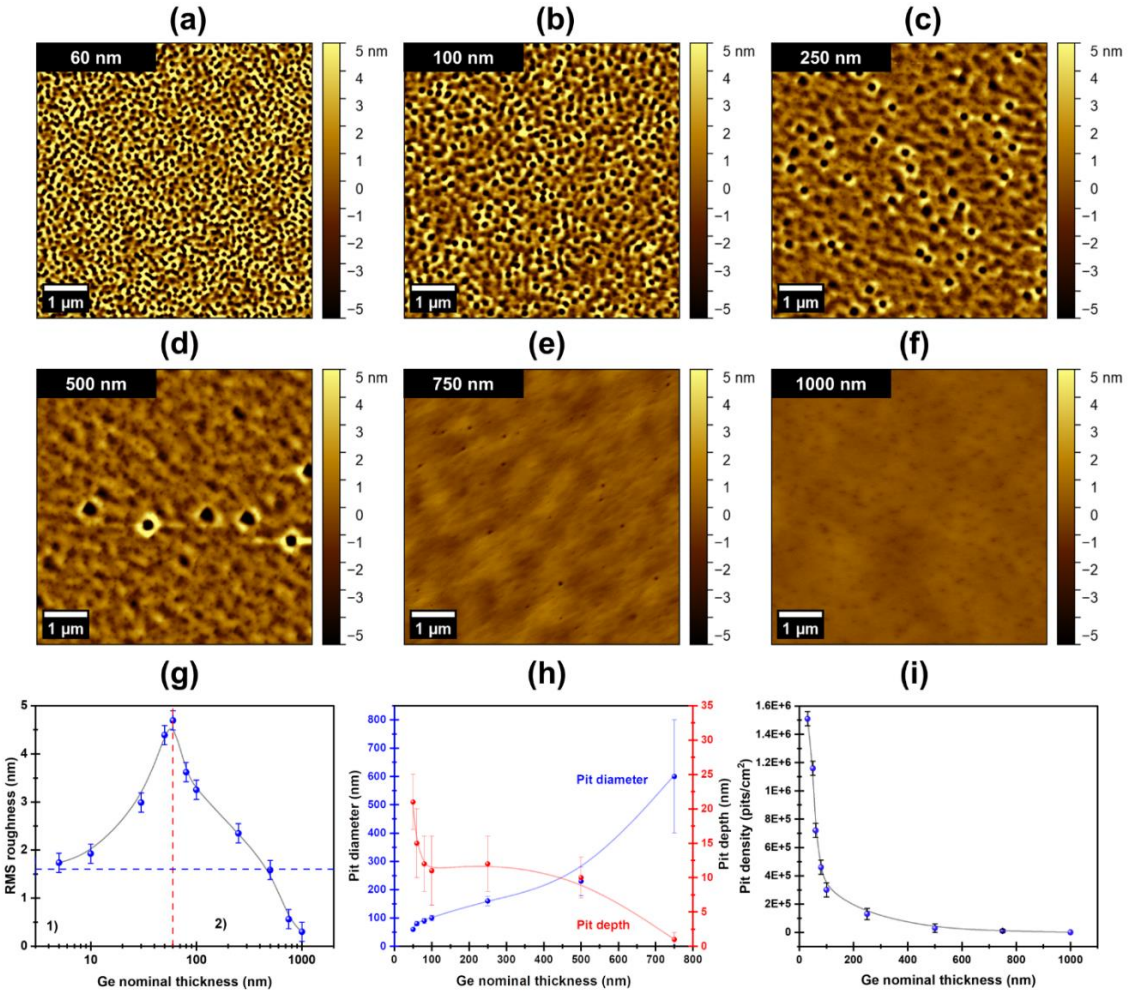


Figure 5-3: (a-f) 5 × 5 µm^2 AFM scans of the Ge membrane for various Ge epilayers thicknesses. (g) Evolution of the surface RMS roughness during all the growth stages, where the Red dashed line indicates the complete coalescence of the layer, and the blue one corresponds to the initial surface roughness of the PGe layer. (h) Surface pits' depth and size evolution as a function of the membrane thickness. (i) Pits surface density as a function of the membrane thickness.

While the island coalescence starts in an early nucleation stage, promoting initial pit formation, some deep pits crossing the membrane are still present up to a deposited Ge thickness of 50 nm (Figure S5-2e). Also considering the measured RMS roughness peak around 60 nm of deposited Ge (Figure 5-3g), this specific thickness appears as a critical one for the membrane formation process by homoepitaxial nucleation on PGe structure. Accordingly, we define the critical thickness (*Tc*), as the minimum thickness required to

ensure the full islands' coalescence into continuously dense membrane, without deep pits crossing the entire membrane. Once Tc is reached, the fully densified membrane can be further thickened, while improving the surface morphology as shown in Figure 5-3g-i. The pits start merging (Figure 5-3-f) and their depth gets continuously reduced as more Ge material is deposited (Figure 5-3h), while the surface pit density decreases until the obtention of perfectly flat surface seen in Figure 5-3i. As the thickness rises beyond Tc, the growth becomes basically dominated by 2D layer by layer mode. Consequently, the RMS roughness decreases exponentially testifying an improved membrane's surface morphology. After the deposition of a 750 nm thick Ge layer, a significant drop in the submicron scale pits' depth and increase of their diameter occur leading to their merging and flattening towards a smooth surface. Consequently, the large pits turn into surface ripples-like morphology making them strongly anisotropic and hardly quantifiable (Figure 5-3e and 5-3h). Despite the persistence of nanoscale sized pits residues (Figure 5-3e), the surface roughness is already well below 1 nm, testifying an excellent morphology suitable for further epitaxial growth. Indeed, as shown by the Figure 5-3d, imperfection free completely smooth surface with RMS roughness of 0.3 nm is obtained for a 1 µm thick membrane. The critical thickness for fully coalesced layer may vary depending on the PGe layer's properties, as the high porosity structure obviously requires more material to ensure the transition from 3D nucleation to 2D growth mode. These results demonstrate that once the deposited thickness exceeds Tc, and the membrane is fully densified, its surface morphology improves with more deposited material. All corresponding growth stages on porous substrates are schematically illustrated in Figure 5-4.

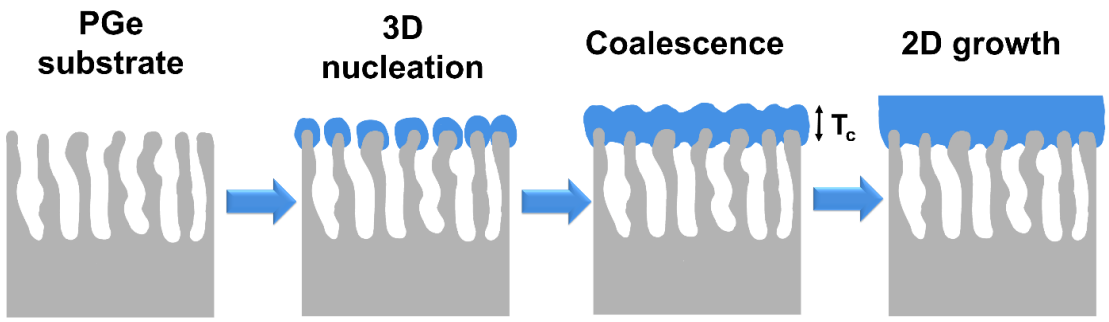


Figure 5-4: Schematic illustration of initial growth steps starting with PGe substrate, 3D island growth, coalescence of islands into Ge membrane, and thickening of the Ge membrane by 2D layer-by-layer growth.

To assess the feasibility of the proposed FSM growth process for different PGe thicknesses and porosity, 1 µm thick Ge membrane has been grown under the same conditions on 1 µm thick PGe layer with approximately 70% porosity. This represents an extreme case of thick and high porosity PGe substrate. Interestingly, fully densified Ge FSM has been successively fabricated at 100 mm wafer-scale (Figure 5-5a), while the high porosity layer remains unreconstructed (as shown later in the inset of the Figure 5-7a). The FSMs show RMS roughness of 1.2 nm, as illustrated by the AFM scan in Figure 5-5. Indeed, the surface still shows ripple-like morphology. Referring to the AFM analysis of the FSM thickness evolution for 54% porosity, such a surface state is likely to characterize fully coalesced pits with depth variation below 5 nm. This surface condition makes the layers comparable to membranes grown on 54% PGe substrate with a thickness between 500 nm and 750 nm. This phenomenon is actually predictable as the higher porosity generates sparser nucleation sites and eventually necessitate more material to form a fully coalesced layer and annihilate all the pits on the surface. The surface morphology can be further improved by the thickening of the membrane following the expected flattening trend.

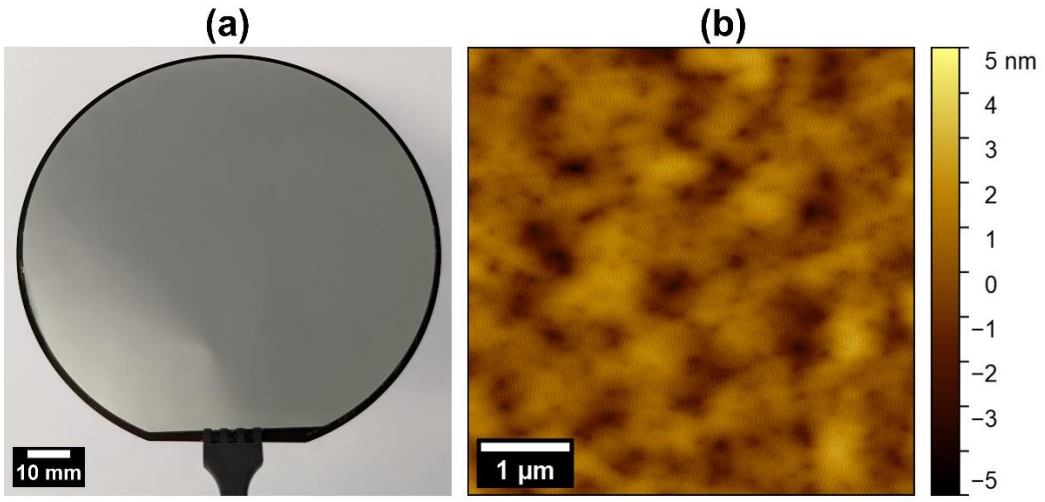


Figure 5-5: (a) Optical image of ~1 µm thick Ge membrane grown on top of 1 µm thick PGe layer with high porosity. (b) AFM scan of Ge membrane's surface grown on high porosity substrate.

To evaluate the crystalline quality of the membranes grown either on 70% or 54% PGe substrates, a comprehensive X-ray diffraction (XRD) analysis was conducted. The out-of-plane 2θ scans in Figure 5-6a reveal unique well-defined Ge (004) and (002)[288] peaks that correspond to the (001) substrate orientation indicating the monocrystalline nature of the FSM grown on both 54% and 70% PGe substrates. This is possible due to the substrate-oriented crystallites of the PGe layer[252], which transfer their orientation to the membrane during epitaxial growth. Furthermore, the in-plane configuration was used to ensure a low penetration depth of the beam, probing only the Ge membrane, thus discriminating its signal from that of the substrate. Interestingly, both in-plane pole figures of Ge (220), shown by the Figure 5-6b, depict four well-defined sharp peaks, with fourfold symmetry, corresponding to the cubic crystal structure of Ge, undoubtedly confirming the single-crystal quality of the Ge FSMs independently of the PGe's porosity used as the substrate.

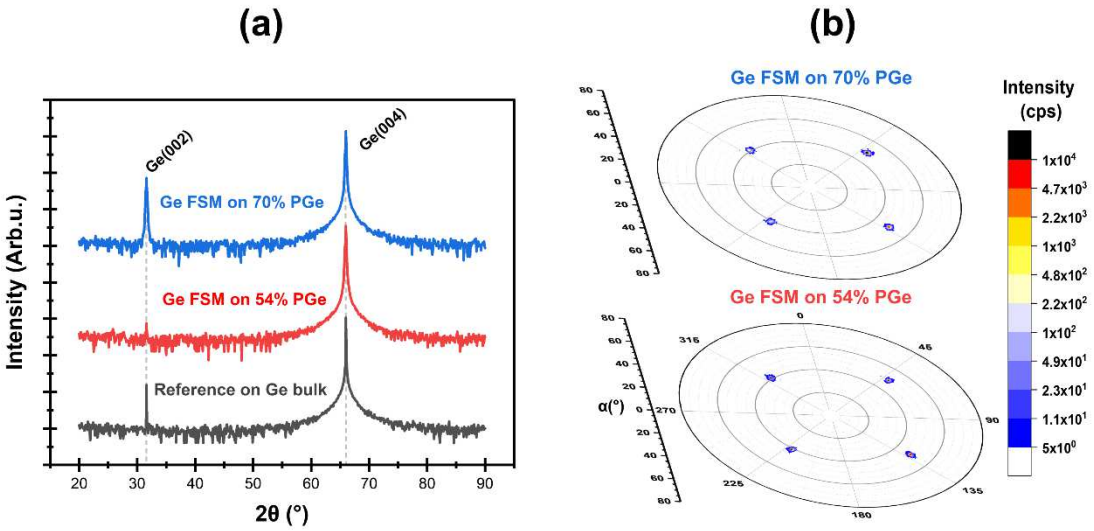


Figure 5-6: (a) 2θ out-of-plane XRD scan of the Ge membrane grown on 54% and 70% PGe substrates and of the Ge bulk substrate as a reference, with logarithmic scale on y-axis. (b) Ge(220) In-plane pole figure of the Ge membranes prepared on PGe substrates with 54% and 70% porosity.

The presence of unreconstructed PGe structure underneath the Ge FSM constitutes a well-adapted separation layer with nanostructured interface allowing for membrane lift-off. Indeed, the cross-sectional SEM image (Figure 5-7a) shows the easy fracture of the 70% porous interface between the Ge membrane and the bulk substrate. For demonstration purpose, we show a successful full 100 mm wafer Ge FSM release by simple adhesive polymer tape and transfer to a transparent, flexible plastic holder (Figure 5-7b).

Furthermore, the unreconstructed PGe separation layer also offers a unique opportunity for substrate reuse, as the bulk substrate material remains largely intact, with only PGe's residuals on the top surface as shown by the Figure 5-7c. Compared to the sub-micron[216,325] to micron scale[182,183] pillars formed by high-temperature annealing methods, in our case, the PGe crystallites are only a few nm in size[210] and have a high specific surface/volume of the Ge material ratio (in respect to Ge bulk material or large pillars). This allows to completely oxidize the majority of the PGe structure in H_2O_2 solution, and then dissolve it in HF with minimal bulk Ge material etching, compared to wet etching methods. This treatment results in a clean surface with RMS roughness ~0.72 nm (Figure 5-7d-e), which is suitable for additional cycles of porosification/epitaxial

growth/membrane release, as previously demonstrated[325]. This further highlights the advantages of using unreconstructed porous interface. The estimated Ge consumption is approximately 1 µm per cycle, since the bulk material stays intact during the substrate cleaning. This process has the potential to produce multiple Ge membranes from a single substrate with minimal material loss. Accordingly, a 175 µm thick Ge wafer could be reused around 30 times before reaching the thickness of 145 µm (Thinnest commercially available 100 mm Ge wafers) and being recycled. Giving the rarity and cost of Ge[328], this method has potential to significantly reduce the cost of Ge-based devices, while offering all the advantages of FSMs.

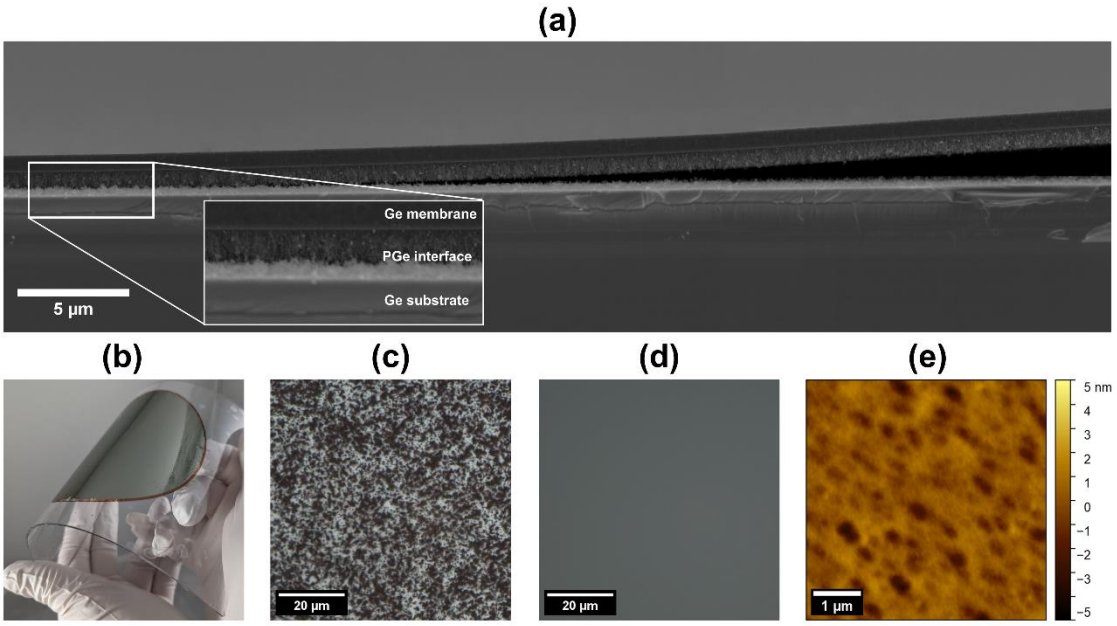


Figure 5-7: (a) Cross-sectional SEM micrograph of the Ge FSM on the weak porous interface illustrating the fracture of the nanostructured interface and the detachment of the membrane. The inset shows a zoom on the unreconstructed high porosity layer underneath the membrane. (b) Optical image of 100 mm Ge membrane transferred to flexible substrate using adhesive tape. (c) optical microscope image of the PGe remnants on the substrate after the detachment (d) and (e) Optical microscope image and AFM scan, respectively, of the Ge substrate after the cleaning

5.7 Conclusion

In summary, we demonstrate the growth of monocrystalline Ge membranes at 300 °C on PGe substrates, while leaving the porous structure of the substrate unchanged during the growth. The initial nucleation stages on porous structure have been experimentally investigated showing two growth regimes. Initially the growth is dominated by 3D nucleation on top of the pores and their coalescence. Once the Ge membrane reaches the critical thickness of coalescence, a dense membrane is formed, and the growth becomes governed by 2D layer-by-layer growth regime. At this stage, the remaining pits at the surface are being annihilated during the thickening of the membrane and good surface quality, with an RMS roughness below 1 nm, can be reached. The XRD analysis demonstrates the monocrystalline quality of the grown Ge membranes for all samples independently of their porosity and thickness. Our results show that PGe layers can be used to fabricate detachable wafer-scale Ge FSMs. Moreover, the nanometric crystallite size and high specific surface of the PGe remnants on the substrate surface, allow an easy cleaning process by oxidation and reuse of the substrate for production of multiple Ge FSMs. Furthermore, our finding also paves the way to the fabrication of wafer-scale FSMs from low temperature grown small bandgap materials for mid-IR optoelectronics such as Ge(Si)Sn.

5.8 Methods

5.8.1 Sample preparation

PGe layers were prepared by optimized BEE process[252] of Ga-doped, 100 mm (100) Ge wafers with 6° off-axis miscut towards (111) orientation and 8–30 mΩ·cm in resistivity, provided by Umicore. The BEE was performed in a custom-made 100 mm porosification cell[252], using SP-50 BioLogic generator. Prior to this process, Ge wafers were treated with HF (49%) solution for 5 min to dissolve any native oxides present on the surface, rinsed with EtOH(99%) and dried under N_2 flow. Samples were then introduced into the porosification cell with HF(49%):EtOH(99%) (4:1, V:V) electrolyte and etching and passivation pulses with 1 s duration and 1 s rest time at the end of each cycle were applied. The medium porosity (~54%) layers were formed using 1 $mA \cdot cm^{-2}$ symmetric etching/passivation current density. To produce high porosity layers (~70%), the etching

current density was increased to 2 $mA \cdot cm^{-2}$. At the end of BEE process substrates with PGe structure were rinsed with EtOH (99%), dried under N_2 flow, and introduced into the loading chamber of the CBE reactor.

Ge growth was carried-out in VG Semicon VG90H CBE reactor, with a load lock, transfer module maintained at ~6.10^{-9} Torr, and thermocouple as a means of monitoring the temperature during the growth. The solid source of Ge, with a K-Cell temperature at 1250 °C, was used to growth Ge with nominal growth rate of 500 $nm \cdot h^{-1}$. Samples were introduced to the growth chamber directly at 300 °C. Then various nominal thicknesses of Ge (5-1000 nm) was deposited on PGe substrates at 300 °Cat chamber pressure ~6.10^{-6} Torr.

After the detachment of the membrane with adhesive tape, the retrieved substrate was immersed in a concentrated H_2O_2(30%) solution for 1 min to fully oxidize the remains of the PGe structure. This is followed by deoxidation in concentrated HF (49%) prior to the reporosification.

5.8.2 Characterization

The top-view and cross-section of PGe layers and Ge/PGe structures were observed with a Zeiss LEO 1540 XB scanning electron microscope at 4.3 mm of working distance and 20 keV of acceleration voltage, to evaluate the thickness of deposited material and any morphological changes of the structure. The surface morphology of the membranes was evaluated using Veeco Dimension 3100, atomic force microscopy system, in tapping mode with SSS-NCHR silicon probe and scan resolution 512 × 512 pixels. The collected AFM profile data on various wafer locations were also used to evaluate the pits' size and depth evolution on the FSM's surface for various thicknesses. The structural properties of PGe and epitaxial layers were investigated using Rigaku smartlab HRXRD system with Cu Kα X-ray source, Ge (220)×2 monochromator on the incident beam, and HYPIX-3000 hybrid pixel array 2D detector. The XRR was used to determine the critical angle of PGe layers, which is directly linked to the porosity[252]. The out-of-plane and in-plane XRD configurations were used to identify the crystalline quality of the Ge membranes.

5.9 Author Contributions

The manuscript was written through the contributions of all authors. All authors have given approval to the final version of the manuscript. **Tadeáš Hanuš:** Conceptualization, Methodology, Investigation, Data curation, Original draft preparation, Review and Editing, Visualization. **Bouraoui Ilahi:** Conceptualization, Methodology, Supervision, Validation, Review and Editing. **Alexandre Chapotot:** Investigation, Review and Editing. **Hubert Pelletier:** Investigation, Validation, Review and Editing. **Jinyoun Cho, Kristof Dessein:** Validation, Review and Editing. **Abderraouf Boucherif:** Supervision, Validation, Review and Editing.

5.10 Acknowledgement

We thank Thierno Mamoudou Diallo and Raphaël Dawant for scientific discussions, Guillaume Bertrand, Philippe-Olivier Provost and all the technical staff of 3IT for the technical support. We thank Umicore, Saint-Augustin Canada Electric (Stace), Innovation en énergie électrique (InnovÉÉ), the Natural Sciences and Engineering Research Council of Canada (NSERC), Fonds de recherche du Québec (FRQNT), Mitacs, for the financial support. Abderraouf Boucherif is grateful for a Discovery grant supporting this work.

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5.11 Supplementary materials

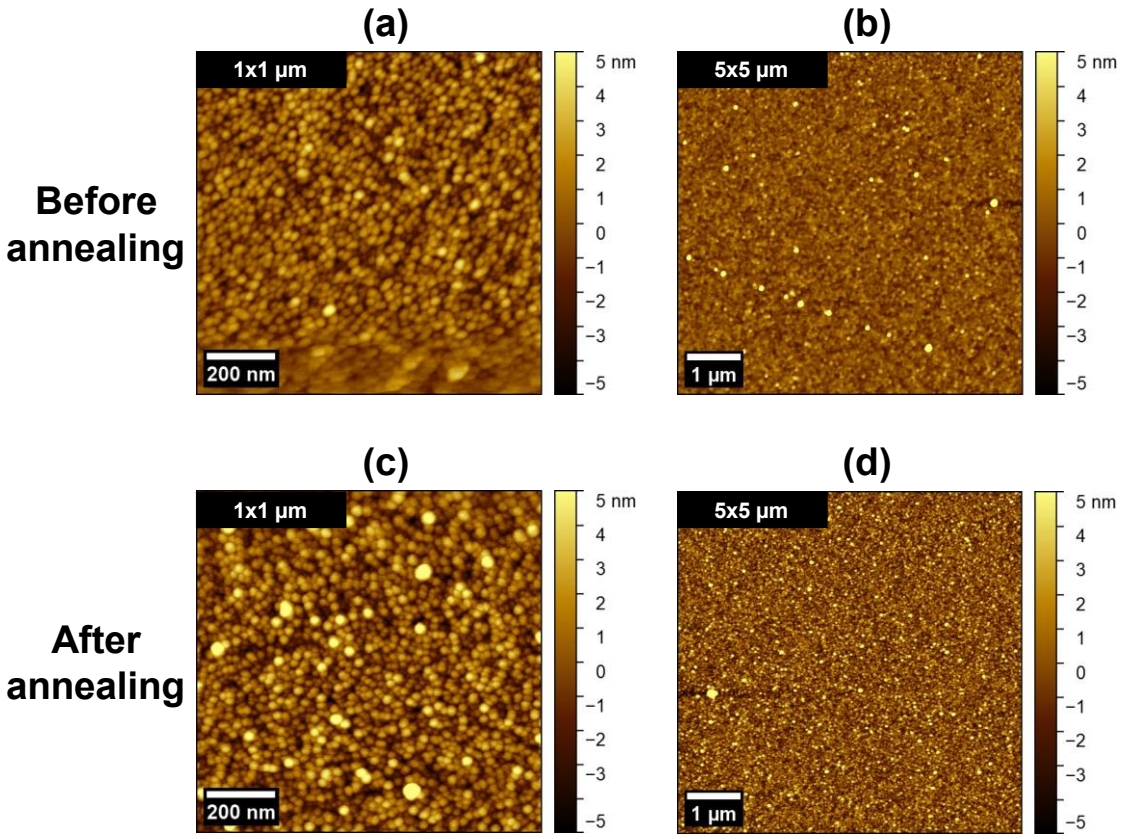

Figure S5-1: AFM scans of PGe layer (a-b) before and (c-d) after annealing at 300 °C showing no significant topological changes of the surface.

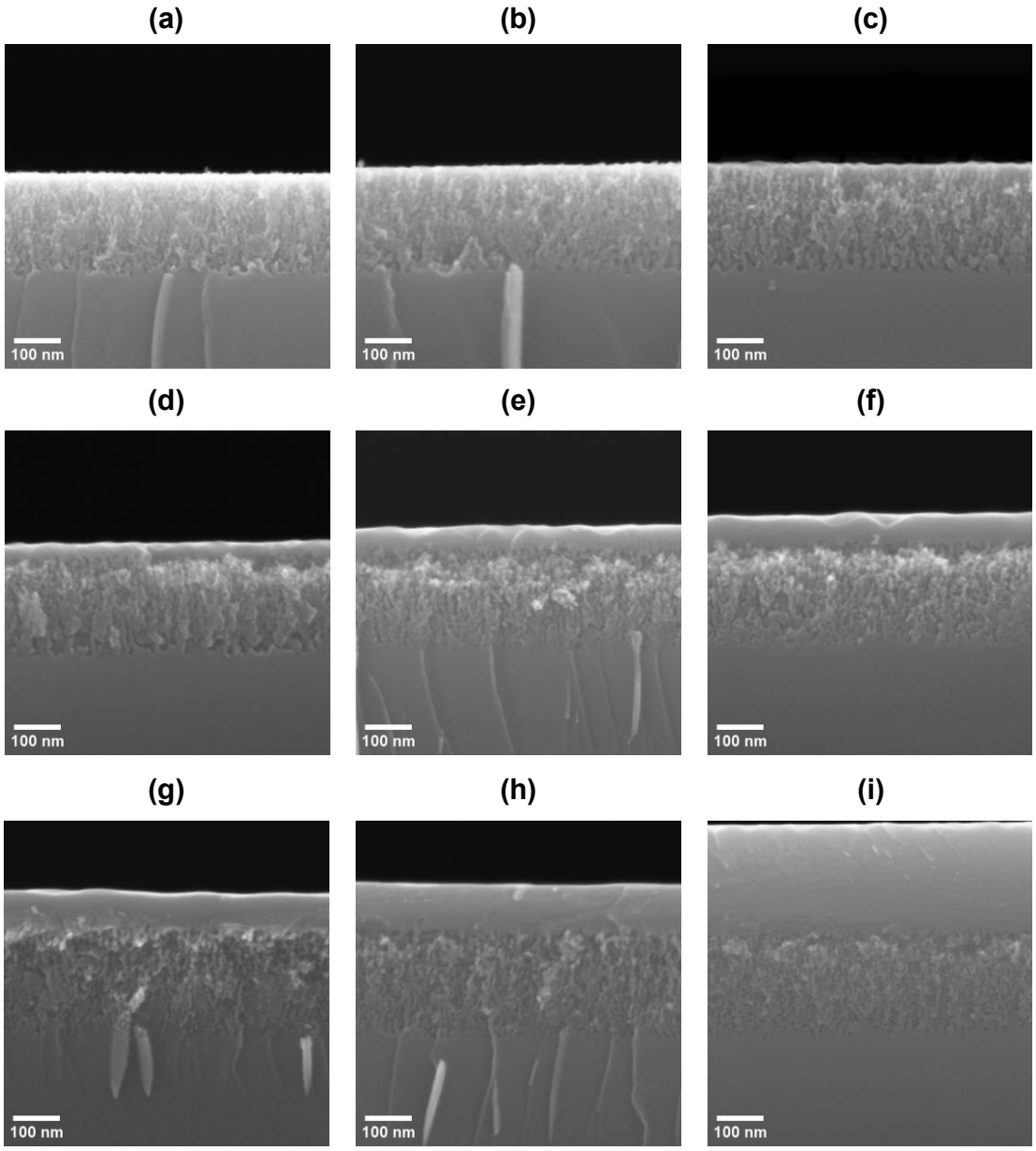

Figure S5-2: (a-i) Cross-sectional SEM micrographs showing the evolution of the layer grown on PGe substrates with increasing quantity of deposited material corresponding to 0/5/10/30/50/60/80/100/250 nm, respectively.

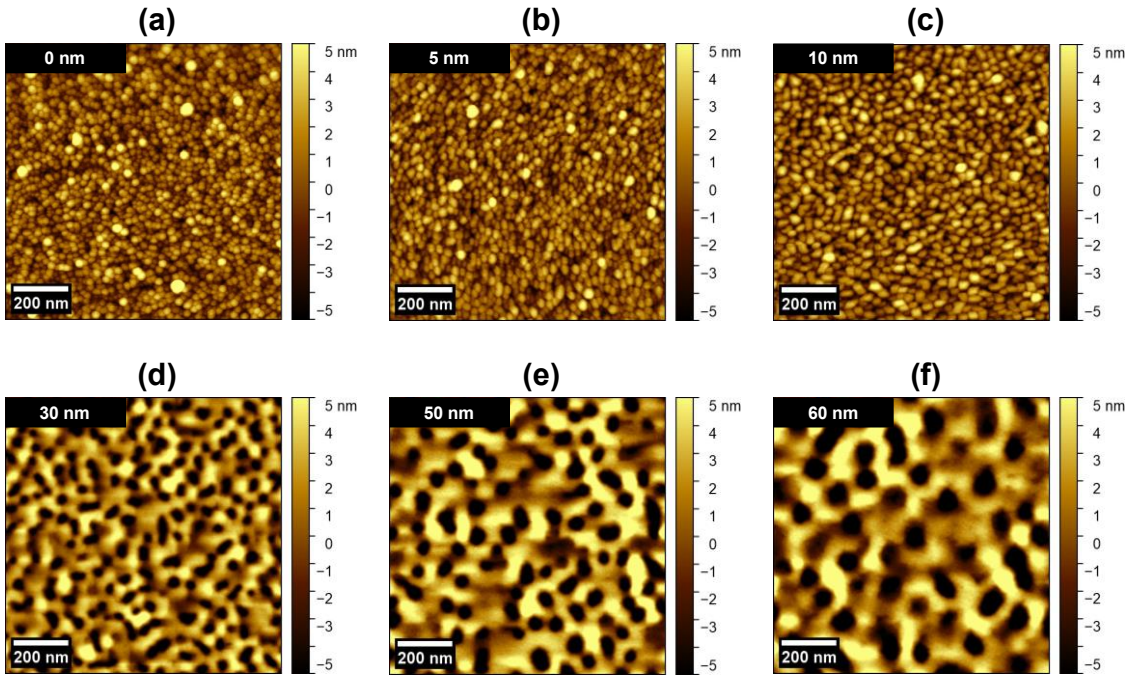

Figure S5-3: (a-f) AFM scans illustrating the evolution of the surface topology during the nucleation on pore walls, 3D seed growth and coalescence into the homogenous layer.

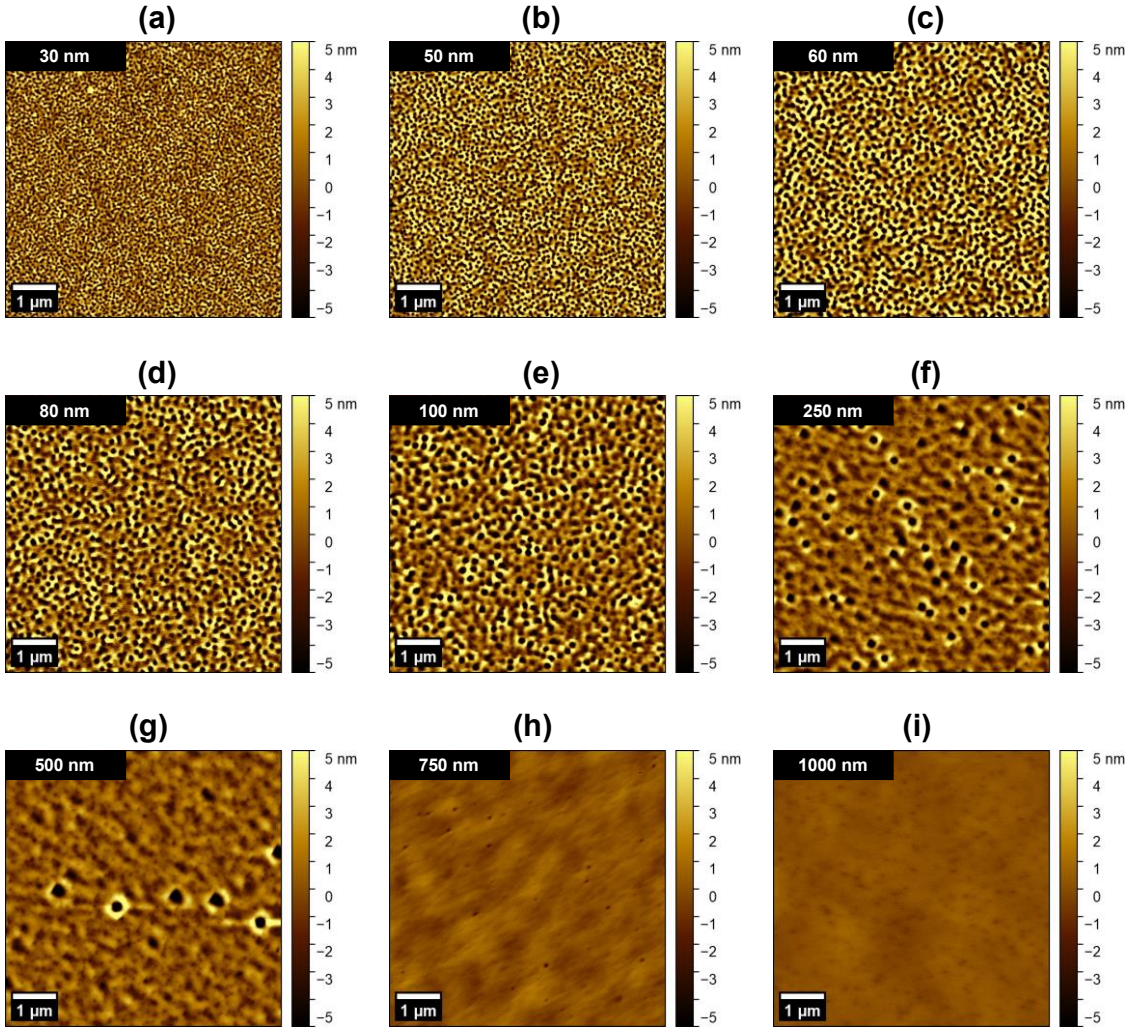

Figure S 5-4: (a-i) AFM scans depicting the evolution of the surface topology during the coalescence and effective thickening of the Ge membrane. The pits on the surface, caused by 3D nucleation, are being annihilated additional thickening of the layer.

Chapter VI

6. Substrate reuse and sustainable production of Ge FSMs

This chapter focuses on substrate cleaning after the Ge FSM detachment and its efficient reuse. The chapter is in form of scientific article published in the journal *Sustainability*. It describes the cleaning process of the PGe structure remaining on the substrate after the Ge FSM detachment and uniform reporosification of the reused substrate. Additionally, it introduces optimized PGe structure for Ge material consumption reduction.

6.1 Foreword

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French title: Production durable des membranes de Ge ultraminces et autoportantes

Contribution to the manuscript:

This article contributes to the thesis by further optimization of the process introduced in Chapter V. It deepens the understanding of the substrate cleaning process and demonstrate the high-quality and uniform PGe structure on recovered substrate. The optimized PGe layer then further improves the surface quality of the membrane and reduces the Ge consumption per fabrication cycle.

6.2 French abstract

Le germanium (Ge) est un matériau crucial pour des applications dans la photonique intégrée, l'imagerie infrarouge, la détection, les photovoltaïques et les photodétecteurs. Cependant, son prix et sa disponibilité limitée freinent son potentiel d'applications. L'utilisation de membranes autoportantes en Ge (FSMs) permet une réduction significative de la consommation de Ge pour la fabrication de dispositifs, tout en offrant des avantages supplémentaires tels qu'une forme légère et flexible pour de nouvelles applications. Dans ce travail, nous présentons un processus de production de FSMs en Ge impliquant la formation successive d'une structure poreuse, le dépôt de la membrane de Ge, le détachement, le nettoyage du substrat original et sa réutilisation. Cela permet la fabrication de multiples FSMs de haute qualité à partir du même substrat. Nous démontrons une réutilisation efficace du substrat grâce à une technique de nettoyage chimique simple du substrat. Des couches poreuses uniformes et de haute qualité sur le substrat nettoyé ont été démontrées. En évitant l'utilisation de polissage mécanico-chimique ou d'une gravure chimique humide substantielle, le processus réduit le cout et l'impact environnemental de la production des FSMs. Ce processus utilise des techniques de dépôt à basse température et à grande échelle, ouvrant la voie à une production durable des FSMs du groupe IV pour la prochaine génération d'optoélectronique flexible.

Sustainable production of ultrathin Ge freestanding membranes

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Keywords: Germanium, Porous lift-off, Freestanding membranes, Layer transfer, substrate reuse

6.3 Abstract

Germanium (Ge) is a critical material for applications in space solar cells, integrated photonics, infrared imaging, sensing, and photodetectors. However, the corresponding cost and limited availability hinder its potential for widespread applications. However, using Ge freestanding membranes (FSMs) allows for a significant reduction in the material consumption during device fabrication while offering additional advantages such as a lightweight and flexible form factor for novel applications. In this work, we present the Ge FSM production process involving sequential porous Ge (PGe) structure formation, Ge membrane epitaxial growth, detachment, substrate cleaning, and subsequent reuse. This process enables the fabrication of multiple high-quality monocrystalline Ge FSMs from the same substrate through efficient substrate reuse at a 100 mm wafer-scale by a simple and low-cost chemical cleaning process. A uniform high-quality PGe layer is produced on the entire recovered substrate. By circumventing the use of conventional high-cost chemical mechanical polishing or even substantial chemical wet etching, and by using an optimized PGe structure with reduced thickness, the developed process allows for both cost and an environmental impact reduction in Ge FSMs production, lowering the amount of Ge used per membrane fabrication. Moreover, this process employs large-scale compatible techniques paving the way for the sustainable production of group IV FSMs for next-generation flexible optoelectronics.

6.4 Introduction

Germanium (Ge) is at the forefront of many applications in optoelectronics and photonics including lasers[314,315], wave guides[308,309], photodetectors[311–313], THz transmission[310], thermophotovoltaic[330–332] and high-efficiency solar cells[333]. Moreover, thanks to the closely matching thermal and crystallographic properties of Ge and gallium arsenide (GaAs), Ge substrates provide a compelling alternative for epitaxial growth of III-V compounds, while offering wafer diameters up to 300 mm. For these reasons, Ge is considered a critical raw material[334,335]. However, its widespread adoption, outside high added-value markets without alternatives, is hindered by its continuously rising high cost due to the increasing demand for this rare material. Ge, representing a scant 0.00015% of Earth's crustal composition, is typically not encountered

in its free state. This element is predominantly sourced as a secondary product, being derived approximately 75% from zinc ore residues and 25% from the ashes of coal combustion[334,335]. It is estimated that around 30% of the world's total Ge production comes from recycling. However, it comes predominantly from new scraps generated during the manufacturing process of fiber-optic cables, infrared optics, and substrates, which are reclaimed and fed back to the production process[336,337]. Although the recycling of old scraps has increased during the past decade, it comes mainly from end-of-life fiber-optic cables and infrared optics, as the Ge recovery from electronic devices is a very complicated process that has not been demonstrated at an industrial scale[338,339].

Indeed, while conventional Ge substrates have a thickness of 140 µm, 225 µm, and 450 µm for diameters of 100 mm, 150 mm, and 200 mm[340], respectively, the efficiently required thickness for device operation generally does not exceed 10 µm. Thus, over 90% of the Ge material serves only as mechanical support without any added value to device functionality or performance. This unnecessarily increases the price of optoelectronic devices and increases the amount of hard-to-recover Ge in end-of-life products. A promising solution to this issue consists in using thin freestanding membranes (FSMs) instead of conventional thick substrates[296], to reduce the quantity of used material. Additionally, FSMs offer additional advantages such as being lightweight, flexible, and providing an extra degree of freedom for integration compared to conventional heterointegration techniques[3]. For instance, solar cells for space and vehicle applications are a perfect example of a sector that would benefit from the lightweight FSM, as the power-to-mass ratio is an important factor in this domain[341]. Similarly, the thin nature of the Ge FSMs bring added benefits for thermophotovoltaic applications as the presence of the thick substrate underneath the active layer results in an unwanted loss in efficiency due to the parasitic radiative coupling[1,2]. Additionally, the freestanding nature of the membranes allows for their direct integration on the structures incompatible with high-quality monocrystalline growth as well as for stacking of materials with large lattice mismatch, which is impossible with conventional heteroepitaxy[3]. The Ge FSMs have already proven their potential for thin high-efficiency solar cells[216,342–344], thermophotovoltaics[345], photodetectors[346,347], and biosensing applications[316,317]. The main domains and applications of Ge FSMs are illustrated in Figure 6-1.

Various techniques have been demonstrated for Ge FSMs fabrication, including substrate thinning[61], epitaxial lift-off[322,323], Smart cut technology[324], mechanical spalling[160], 2D-assisted epitaxy[147,148], and Germanium-on-Nothing[182,348]. Among them, the porosification lift-off technique has recently received significant attention and development thanks to its potentially high-throughput and cost-effective process[216,296]. This approach involves the formation of a uniform and tunable porous Ge (PGe) layer[252] using electrochemical etching[209,211,213,349], followed by the deposition of a Ge membrane on top of it. The membrane can then be detached from the parent substrate through the weak nanostructured interface, forming a thin Ge FSM. Moreover, this technique enables the reconditioning of the parent substrate by chemical etching and its reuse for the production of multiple Ge FSMs[226], further reducing the fabrication cost by avoiding the need for costly chemical mechanical polishing[224,350]. Overall porosification lift-off has shown its potential for large-scale production of Ge FSMs, with the significantly reduced consumption of Ge material than standard wafering techniques. Even with all the recent advancements this technique holds the potential to be improved and further reduce the quantity of Ge during the production of Ge FSMs.

Here, we present an optimized wafers-scale process enabling the Ge FSM fabrication using a porosification lift-off technique, involving the PGe structures with a reduced thickness and porosity, allowing for both reduced Ge consumption and improved Ge FSM surface quality. We demonstrate a successful cleaning of the entire 100 mm substrate after the detachment of the Ge FSM, using slow chemical etching of the PGe residues. The reporosification of the recovered substrate is achieved, resulting in a new high-quality uniform PGe suitable for the further production of Ge FSMs from the same substrate. These results highlight the potential of using Ge FSMs to reduce rare material consumption during optoelectronic device production, offering a sustainable pathway for the next-generation high-performance devices.

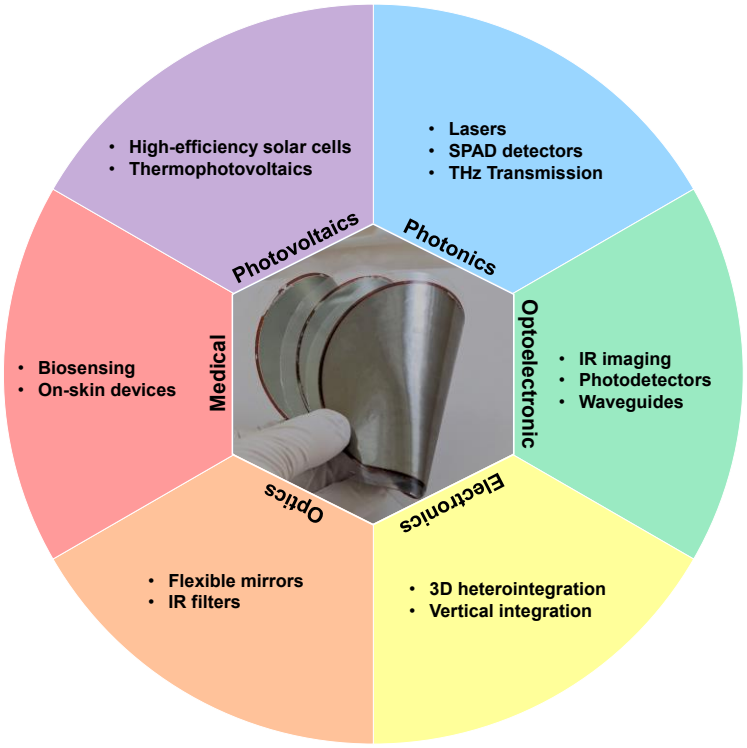

Figure 6-1: Illustration of Ge FSM applications. The central image depicts freestanding Ge membranes on a flexible holder obtained in this work.

6.5 Results and discussions

The fabrication process of Ge FSMs through the porosification lift-off technique consists of four main steps, as illustrated in Figure 6-2. First, a high-porosity (60-80%) porous germanium (PGe) layer is formed at the Ge substrate surface by electrochemical etching in HF:EtOH electrolytic solution. This is followed by a low-temperature deposition of the Ge membrane on top of the PGe layer. The membrane is then mechanically detached from the substrate, which is facilitated by the fragile nanostructured PGe interface between the Ge bulk substrate and the Ge FSM. After detachment, the PGe remnants at the surface of the recovered parent Ge substrate are oxidized using an H_2O_2 solution followed by their complete dissolution in HF and reuse of the parent Ge substrate for reporosification and repeating the process of Ge FSM fabrication. All steps were previously detailed in the Materials and Methods section, and the obtained results are discussed further below.

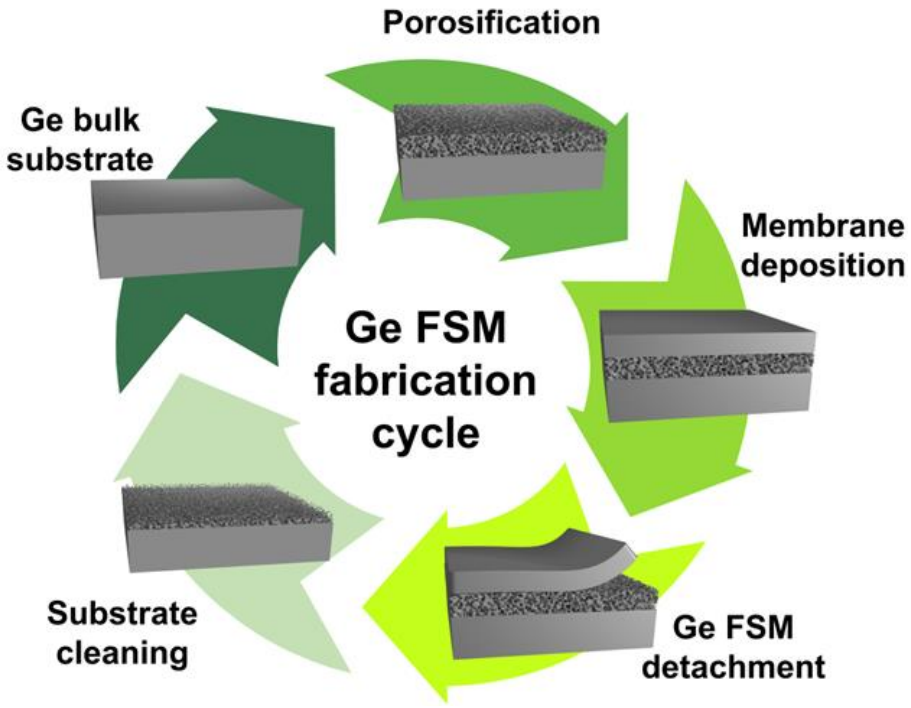

Figure 6-2: Schematic illustration of the Ge freestanding membrane fabrication and substrate reuse.

The Ge FSM fabrication cycle begins with the formation of a high-quality PGe layer on top of the Ge substrate. This is a crucial part of the process, as any major defects or inhomogeneities in the PGe structure can be further transferred to the Ge membrane, impacting its quality. Figure 6-3a shows a SEM cross-sectional micrograph of the PGe layer used in this work. The typical sponge-like porous structure shows a well-defined interface between the PGe layer and bulk material, with ~264 nm thickness and 63% porosity. Furthermore, the ellipsometry mapping of the 100 mm wafer, shown in Figure 6-3b and 6-3c, demonstrates the overall uniformity of the porous nanostructure in both the thickness and porosity with respective variations of ± 4 nm and ± 1% across the entire surface of the wafer. Moreover, the porous structure manifests a low surface roughness below 2 nm, as illustrated by Figure 6-3c. The closely packed crystallites of the high-porosity PGe layers (60-80%) make an excellent template for the growth of Ge membrane structures while enabling an easy detachment without additional annealing steps or deposition of the stressor layers to initiate the separation.

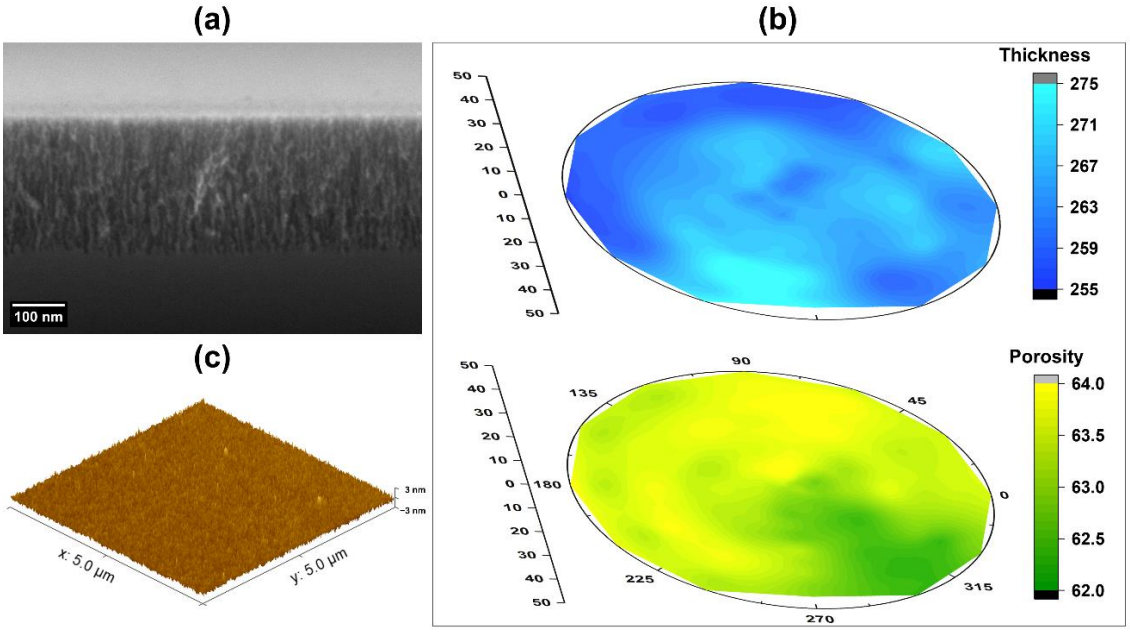

Figure 6-3: (a) Cross-sectional SEM micrograph of the PGe structure (b) Ellipsometry mapping of the 100 mm wafer showing the uniformity of the PGe layer in thickness (blue) and porosity (green) (c) 5×5 µm^2 AFM scan of the PGe surface.

A 1 µm thick Ge membrane is then grown, at 300 °C, on top of the PGe structure, resulting in a smooth surface with RMS roughness around 0.7 nm, as demonstrated by Figure 6-4a. A few shallow pits and undulations are still identifiable on the surface but can be annihilated by increasing the membrane's thickness. Depending on the targeted application the thickness of the membrane can be varied from ~100 nm to few µm. However, for membranes thinner than 1 µm the surface roughness can increase up to 5 nm for the thinnest membranes[296]. This way, the amount of Ge material used for device integration can be directly controlled to use only the quantity of Ge necessary for its function and hence limit the waste of material.

The crystalline quality of the membrane is verified using X-ray diffraction in the in-plane configuration, to limit the beam penetration. The resulting in-plane pole figure around the Ge (220) axis displays four sharp peaks with 90° rotational symmetry around their central axis as depicted by Figure 6-4b. This pattern corresponds to the diamond cubic crystal structure of Ge, confirming the high crystalline quality of the Ge membrane. Interestingly, the central axis of the sample demonstrates a 6° shift from the measurement

axis, as illustrated by the red arrow in Figure 6-4b. This shift is attributed to the parent substrate's 6° miscut from (100) orientation towards the (111) axis. Since the porous structure maintains the original substrate orientation, it can transfer even this characteristic to the Ge membrane, resulting in a monocrystalline epilayer with the same 6° off-cut as the parent substrate. The pole figure of the Ge membrane deposited on the on-axis substrate can be found in Figure S6-1.

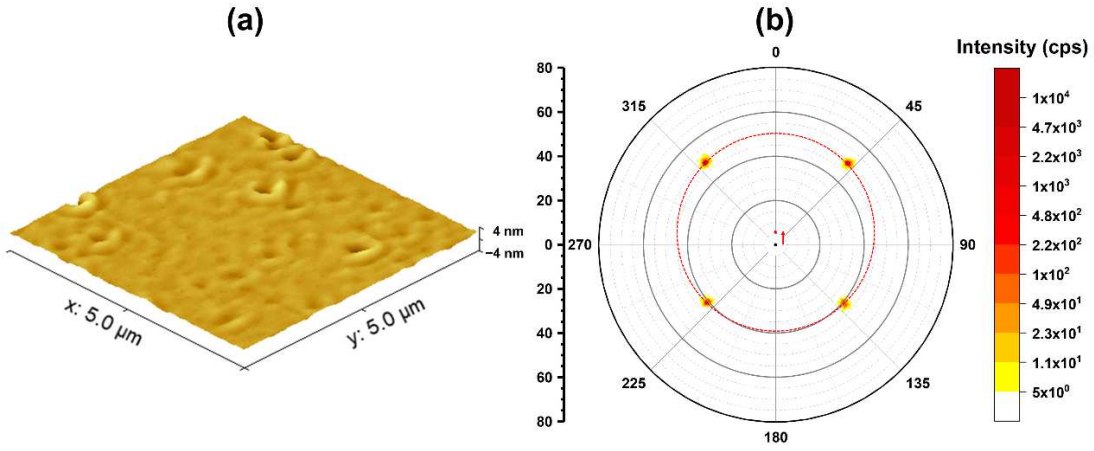

Figure 6-4: (a) 5 × 5 µm^2 AFM scan of the Ge membrane grown on PGe with surface roughness <1 nm (b) In-plane pole figure of the Ge FSM around Ge (220) axis, the red circle and arrow represent the 6° off-cut orientation of the membrane compared to normal axis.

Once the Ge membrane is formed, the high-porosity nanostructure underneath represents a perfect fragile interface allowing for easy detachment and transfer to the host substrate. Using an adhesive polymer tape, the Ge FSM can be separated from the parent substrate and transferred to a flexible PVC holder. After the detachment, irregular remnants of the porous structure are still present on the surface of both the substrate and membrane as illustrated by Figure 6-5a-c. To eliminate these porous residues, a simple chemical cleaning process is employed. The chemical etching of Ge in aqueous solutions functions on the principles of the formation and dissolution of the GeO_2, where H_2O_2 acts as an oxidizing agent which transforms the Ge surface in GeO_2[110,351]. At the same time, the reduction in the H_2O_2 at the surface of Ge provides the holes necessary for the dissolution of the oxide[61,352]. When the substrate is immersed in concentrated H_2O_2, the solution

transforms the remaining PGe structure's high specific surface area in GeO_2 and starts slowly etching it away[111]. This chemical etching of Ge can be described by Equation (6-1) and (6-2), where Equation (6-1) represents the formation of the GeO_2 on the Ge surface, and Equation (6-2) represents its dissolution into H_2GeO_2 a tetravalent form stable in aqueous solution with pH <8.5[110].

$$Ge + 2\,H_2O_2 \rightarrow GeO_2 + 2\,H_2O \qquad \text{(Equation 6-1)}$$

$$GeO_2 + H_2O \rightarrow H_2GeO_3 \qquad \text{(Equation 6-2)}$$

Compared to techniques involving high-temperature annealing and PGe reconstruction in crystallites with size superior to 100 nm[226,353], the high porosity nanostructure with significantly higher specific surface area and only 5-10 nm thick pore walls, allows for isotropic etching by H_2O_2 at a very slow rate (few nm/min). This avoids the substantial chemical etching of the substrate (few µm) necessary for the planarization of larger features while maintaining control over the etching process due to the slow etching rate. The remaining oxides on the substrate's surface are then dissolved in an HF solution during the deoxidation step prior to the reporosification. This results in a remnant-free surface as shown in Figure 6-5d-f.

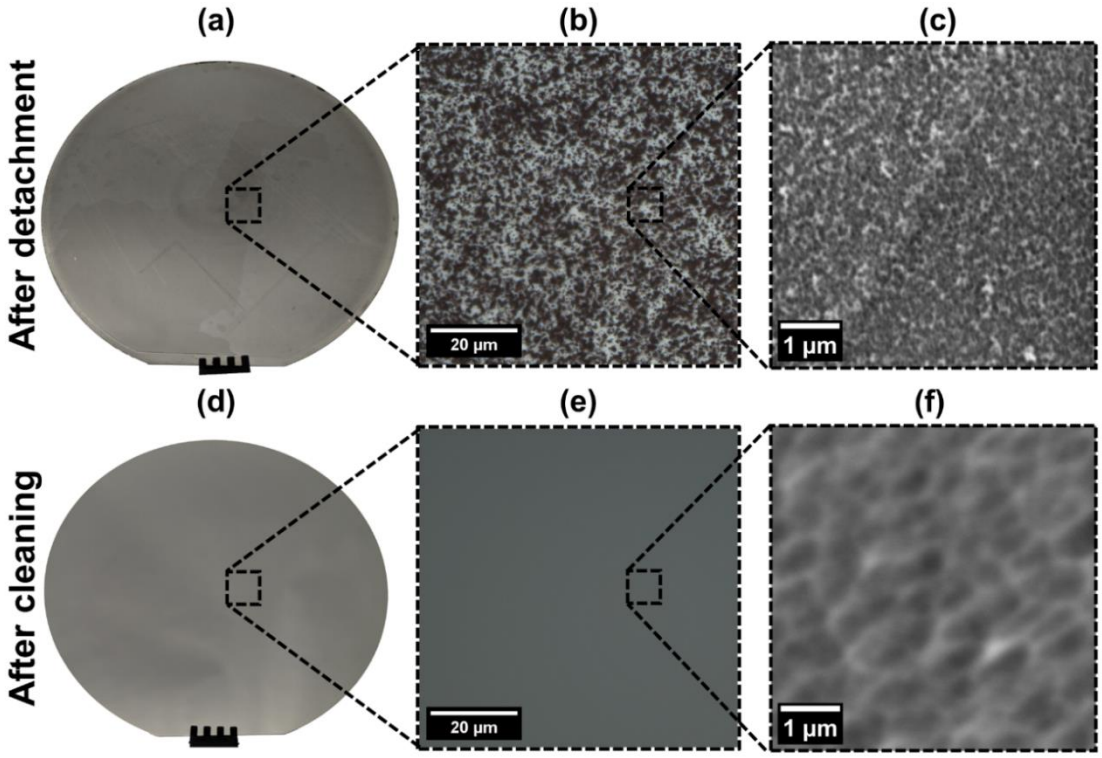

Figure 6-5: (a-c) Typical photo, optical microscope image, and SEM micrograph of the substrate with PGe remnants after the detachment, respectively (d-f) Typical photo, optical microscope image, and SEM micrograph of the substrate after cleaning

The entire chemical cleaning process is schematically illustrated in Figure 6-6a. The AFM scan of the recovered substrate in Figure 6-6b shows a flat surface with surface roughness below 1 nm. The apparent waving of the cleaned surface represents a slight variation in the initial Ge bulk/PGe interface formed during the BEE process, as the bottoms of the pores are not all perfectly aligned. This effect is then partially mitigated directly by the first anodic step of the BEE process during the formation of the new PGe layer[226,252].

The PGe remnants on the Ge FSM backside have the same nature as they are formed by the separation of the uniform PGe layer. This means that the same approach can also be used for membrane cleaning. However, its necessity should be evaluated depending on the Ge FSM use. In the case of applications where the Ge membrane does not play an active role in the final function and serves mainly as the crystalline substrate for the growth of epitaxial structures, membrane cleaning should not be necessary.

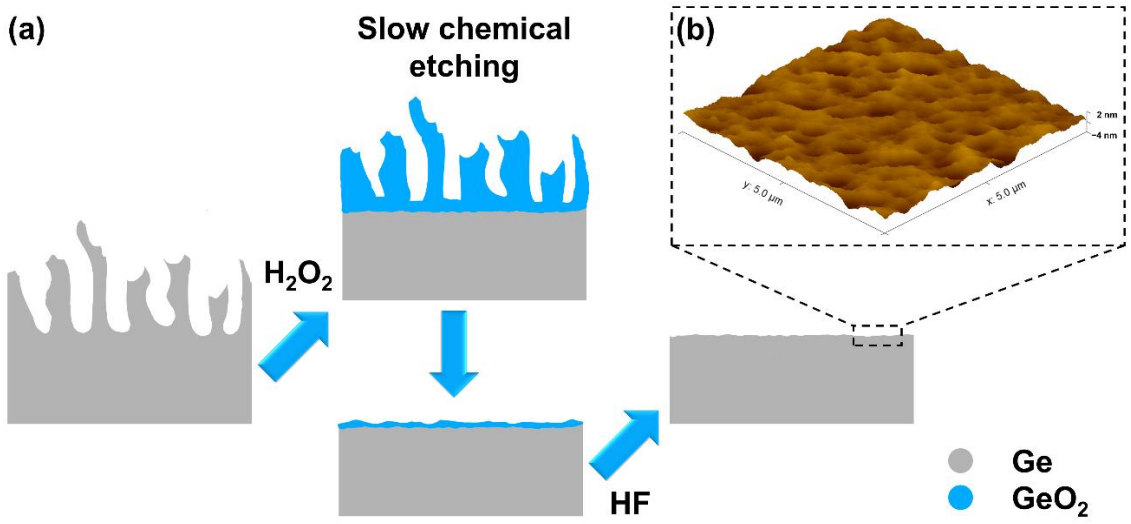

Figure 6-6: (a) Schematic illustration of the slow chemical etching cleaning process of the PGe remnants on the substrate's surface (b) 5×5 µm^2 AFM scan of the recovered Ge substrate after chemical cleaning with RMS roughness of 0.8 nm

To complete the cycle, the recovered parent substrate then undergoes a second porosification process to obtain a new PGe layer, presented in Figure 6-7a. For comparison, an optical image of the PGe layer on an epi-ready substrate can be found in Supplementary Materials Figure S6-2. The BEE conditions are identical to the ones previously used on the epi-ready substrate. It presents the same thickness and porosity with high uniformity across the entire 100 mm wafer as demonstrated by ellipsometry mapping present in Figure 6-7b-c. The new PGe layer presents a thickness of 265 ± 5 nm and a porosity of 63 ± 1%, both of these values are the same as on the original epi-ready substrate, demonstrating that the small surface undulations on the recovered substrate do not influence the BEE process. This new high-quality PGe structure then allows for new deposition of the Ge membrane and fabrication of multiple Ge FSMs from the same substrate, by repeating the process. This demonstrates that the Ge FSMs can be fabricated with the consumption of less than 300 nm of the original Ge substrate while allowing for easy substrate reuse without the involvement of expensive reconditioning techniques such as chemical mechanical polishing[224]. In the context of our previous study, the use of an optimized PGe layer enables improvements in both Ge FSM surface quality and material consumption of the substrate per cycle. The lower porosity allows for more closely packed nucleation sites,

resulting in a reduction in the membrane's surface roughness to 0.7 nm from 1.2 nm on 70% porosity PGe substrate[296]. Additionally, the reduced PGe thickness, further lowers the substrate consumption by over 70%, while maintaining the ease of detachability of the Ge FMS.

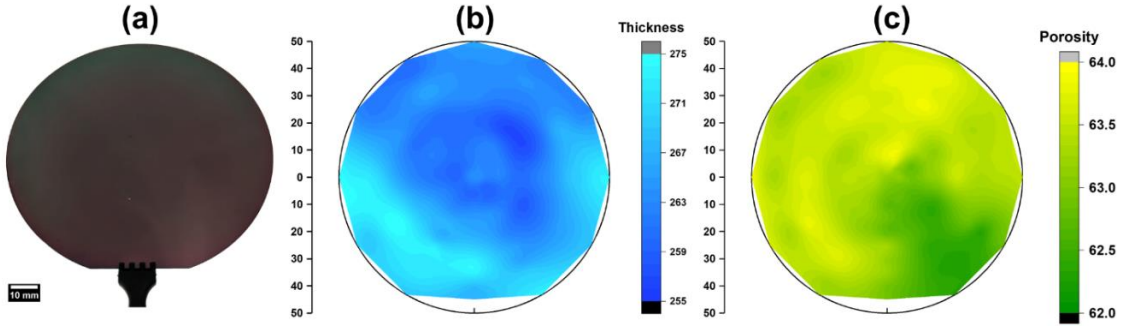

Figure 6-7: (a) Optical image of the PGe layer on recovered substrate. (b-c) Ellipsometry mapping of the 100 mm wafer showing the uniformity, in thickness and porosity of the PGe layer on recovered substrate, respectively.

In numbers, around 300 nm of the original substrate is consumed per produced membrane. This value includes the thickness of the PGe layer (~270 nm) and the front/back etching of the substrate during the cleaning process (~30 nm). By considering a conventional 100 mm, Ge wafer with a thickness of 175 µm and its thinnest commercially available counterpart with a thickness of 140 µm, around 35 µm of the substrate can be used for Ge FSM production before losing its structural integrity. This results in over 100 membranes produced from a single 100 mm wafer. The number of reuses can be further increased by the use of thicker substrates, which bring additional benefits such as a reduction in material lost during the sawing process of Ge wafers from a solid ingot grown by the Czochralski method[354–356]. Alternatively, the Ge substrate can be bonded on a holder (e.g., Si substrate) for mechanical support, allowing for the use of almost the entire substrate's thickness and enabling over 500 reuses. This number is expected to further grow with scaling on larger substrates, as larger diameter wafers are considerably thicker.

In comparison, techniques involving high-temperature annealing present large pillars with diameter superior to 100 nm, and cannot be reconditioned without the etching of substantial material quantity (few µm)[353] or the involvement of costly chemical

mechanical polishing (CMP)[182]. Considering single-sided chemical etching of 5 µm per reuse, this approach presents a more limited number of Ge FSMs fabricated from a single wafer. However, this approach holds its advantage for applications involving high processing temperatures (>400 °C) as the high specific area PGe structure cannot be maintained under these conditions.

2D-assisted epitaxy, in theory, could eventually offer infinite reuse of the substrate. However, it is still in relatively early research stages, especially in case of group IV materials such as Ge which was demonstrated for the first time in late 2022[147], using a new approach on local nucleation and lateral overgrowth on the 2D interface[139,148]. Moreover, other challenges such as large surface growth and the transfer of high-quality interfaces need to be resolved for its viable application[357].

Considering, the rarity of the Ge, the complexity of its recovery from end-of-life optoelectronic devices, and the recent geopolitical situation around this material, the Ge FSMs represent a sustainable alternative to conventional Ge substrates. It offers to significantly reduce the quantity of Ge material integrated into optoelectronic devices while allowing for cost reduction thanks to the limited Ge use and substrate recycling.

6.6 Conclusion

In conclusion, we demonstrated a successful substrate reuse and production of a highly uniform PGe layer on recovered Ge substrate, setting the milestone for the production of multiple Ge FSM from the same substrate. The reduced thickness of the PGe structure allows for a reduction in Ge consumption per cycle compared to previous studies, while still maintaining the capacity to easily detach and transfer the membrane. Additionally, the optimized porosity helps to improve the surface quality of the Ge FSM membrane. The substrate cleaning is achieved through slow chemical etching of the PGe remaining on the surface, enabling its complete dissolution and obtention of the surface with roughness below 1 nm, without the necessity of substantial etching of the substrate material. The recovered substrate enables the successful reporosification of the entire 100 mm wafer, resulting in a new high-quality PGe layer with physical properties identical to the one formed on the epi-ready surface. This allows for efficient substrate reuse, and the production of multiple Ge membranes, with minimal consumption of the Ge material, due

to the optimized PGe structure employed in this work. The Ge FSM production and substrate recovery open the way for a sustainable alternative to conventional Ge substrates while providing all the advantages of freestanding form for direct heterointegration and flexible electronics. It offers to significantly lower the quantity of Ge material integrated into optoelectronic devices, reducing the quantity of hard-to-recover material in end-of-life products. Furthermore, this approach presents a high potential for the fabrication of FSMs from other group IV materials such as Ge(Si)Sn alloys, presenting a small band gap ideal for near/mid-IR optoelectronic and photonic applications offering a nontoxic and low-cost alternative to III-V materials.

6.7 Methods

6.7.1 Sample preparation

PGe layers were formed using an optimized bipolar electrochemical etching (BEE) process[252] on top of Ge substrates. The p-type gallium (Ga) doped, 100 mm Ge wafers oriented along the (100) axis, with 6° off-axis miscut towards (111) orientation and resistivity of 8–30 mΩ·cm were used in this study. Before the PGe formation, the Ge substrate was deoxidized in a concentrated hydrofluoric acid (HF, wt%) solution for 5 min, followed by rinsing in anhydrous ethanol (EtOH, 99 wt%) and drying under nitrogen (N_2) flow. The BEE was carried out in a custom-built 100 mm porosification cell, consisting of a polytetrafluoroethylene (PTFE) body, copper (Cu) backside electrode, and platinum (Pt) wire working electrode, filled with 300 ml of electrolyte solution composed of HF(49 wt%):EtOH(99 wt%) in 4:1 (V:V) proportions. The SP-50 BioLogic generator was used to apply cyclic square 1 s pluses of etching and passivation with 1.5 and 1.0 $mA \cdot cm^{-2}$ current density, respectively. Each cycle was separated by 1 s rest time and 420 cycles were applied in total to produce the PGe layer. At the end of the process, PGe substrates were rinsed with EtOH (99 wt%), dried under N_2 flow, and subsequently placed into the loading chamber of the growth reactor under a vacuum. Further details on PGe formation can be found in our previous work[252].

The ~1 μm thick Ge membrane was grown in a VG Semicon VG90H CBE reactor at 300 °C, using a solid source of Ge heated at 1250 °C with a nominal deposition rate of 500 $nm \cdot h^{-1}$ as described previously[296].

After epitaxial growth, the Ge FSM is detached using an adhesive tape and transferred onto a flexible Polyvinyl Chloride (PVC) substrate. The recovered Ge substrate has been reconditioned by immersion in a concentrated hydrogen peroxide (H_2O_2, 30 wt%) solution for 1 min, at room temperature, to transform the remaining PGe crystallites at the surface in germanium dioxide (GeO_2) and etch them slowly away. The substrate has been subsequently deoxidized in concentrated HF (49 wt%) to dissolve the remaining Ge oxides on the surface and recover a flat surface. The reconditioned substrate is then reporosified, using the same BEE conditions as on the epi-ready substrate. The complete list of specifications of all the chemicals used in this study can be found in Table S6-1 of Supplementary Materials.

6.7.2 Characterization

The PGe thickness, porosity, and their uniformity over the 100 mm wafer were characterized using a J. A. Woollam Co. VASE instrument in the spectral range between 500 nm and 900 nm. The measuring points were radially paced every 30° with an in between point spacing of 5 mm along the radius of the wafer. The PGe thickness was also verified using SEM imaging of the PGe layer cross-section, also revealing the morphology of the nanostructure. The presence/lack of the PGe layer remnants on the substrate after the detachment and cleaning process was observed using optical microscopy (confocal microscope Keyence VK-X1100 with 150× lens) and SEM imaging of the substrate's plan view. All the SEM observations were performed at a 4.0 mm working distance with Thermo Fisher Scios 2 SEM using 20 keV acceleration voltage for the electron beam.

The Park system NX20, atomic force microscope (AFM) was used to evaluate the surface topology of the PGe layer, Ge membrane, and of the recovered substrate after cleaning. The AFM scans were performed in tapping mode using a super sharp silicon probe (SSS-NCHR) and a scan resolution of 512×512 pixels over a 5×5 μm^2 area. The scan data were then processed using Gwyddion software (Version 2.64) to obtain the root mean square (RMS) roughness values.

The investigation of the structural properties of Ge FSM was conducted using the Rigaku Smartlab high-resolution X-ray diffraction (XRD) system in the in-plane configuration equipped with Cu Kα X-ray source (wavelength λ(Cu Kα) = 1.5406 Å),

Ge (220)×2 monochromator on the incident beam, and a two-dimensional hybrid pixel array semiconductor X-ray detector (HYPIX-3000). The in-plane pole figure XRD measurements were employed to assess the crystalline quality of the Ge membranes while restricting the depth of beam penetration.

6.8 Author Contributions

The manuscript was written through the contributions of all authors. All authors have given approval to the final version of the manuscript. **Tadeáš Hanuš**: Conceptualization, Methodology, Investigation, Data curation, Original draft preparation, Review and Editing, Visualization. **Bouraoui Ilahi**: Conceptualization, Methodology, Supervision, Visualization, Investigation Review and Editing. **Jinyoun Cho, Kristof Dessein**: Review and Editing. **Abderraouf Boucherif**: Supervision, Funding acquisition, Review and Editing.

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6.10 Supplementary materials

Table S6-1: List of chemicals employed in porosification and chemical cleaning of the substrates.

Chemical name	Acronym	CAS number	Concentration (wt%)	Density (g/mL at 25 °C)
Hydrofluoric acid	HF	7664-39-3	49	1.15
Ethanol, anhydrous	EtOH	64-17-5	99	0.79
Hydrogen peroxide	H_2O_2	7722-84-1	30	1.45

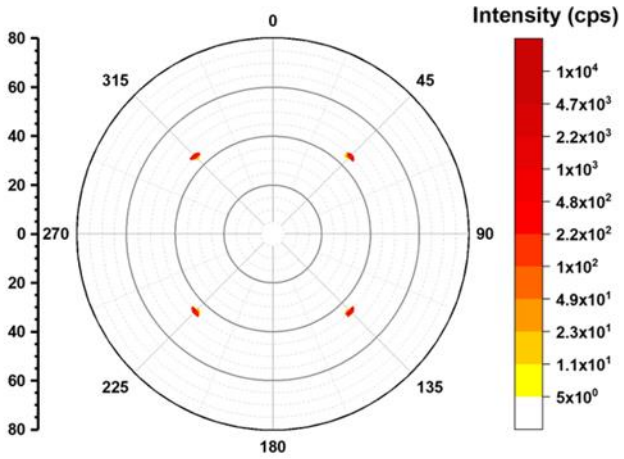

Figure S6-1: In-plane pole figure of the Ge FSM around Ge (220) axis deposited on the on-axis Ge substrate.

Figure S6-2: Optical image of uniform PGe layer on epi-ready substrate.

Chapter VII

7. Conclusions and perspectives

This chapter summarizes the advancements made in this work and proposes perspectives for further development of the introduced processes for fabrication of group IV materials FSMs.

7.1 Conclusions (Français)

Les membranes semi-conductrices autoportantes offrent de nombreux avantages, tels que la légèreté et la flexibilité, par rapport aux hétérostructures sur des substrats massifs conventionnels. De plus, leur degré de liberté supplémentaire ouvre de nombreuses possibilités pour le développement de procédés de fabrication innovants et de dispositifs novateurs grâce au transfert et/ou à l'empilement de membranes à base de divers matériaux. La fabrication de FSMs semi-conductrices offre une opportunité unique non seulement pour économiser des coûts et réduire l'utilisation de matériaux rares, mais aussi pour introduire et développer la prochaine génération de dispositifs microélectronique et optoélectronique à base de FSMs.

Cette thèse passe en revue les différentes approches possibles pour la fabrication de FSMs semi-conductrices, en résumant les avantages et les limites de chaque technique de fabrication de FSMs actuellement disponible. Cela nous montre que malgré tous les progrès réalisés, il reste encore un long chemin à parcourir pour que les FSM deviennent une solution industrielle viable et un remplacement pour les substrats conventionnels. Bien que la fabrication de FSMs de matériaux III-V et III-N ait démontré de nombreux progrès, les méthodes permettant la formation de membranes semi-conductrices du groupe IV sont très limitées. Dans cette thèse, nous nous concentrons sur le développement de nouvelles techniques d'ingénierie de substrats et de croissance épitaxiale permettant la fabrication de FSMs à base de matériaux du groupe IV en utilisant l'épitaxie assistée par les matériaux 2D et le décollement par porosification.

7.1.1 Épitaxie assistée par matériaux 2D

La première partie de ce travail (Chapitre III) se concentre à surmonter les défis de l'épitaxie assistée par matériaux 2D pour la croissance de matériaux non polaires qui ne peuvent pas être formés en utilisant les techniques RE ou QVdWE. Nous introduisons une nouvelle approche appelée nucléation par points d'ancrage permettant l'intégration monolithique de semi-conducteurs 3D non polaires sur des matériaux 2D et la fabrication des FSMs. Elle repose sur l'ingénierie de la couche de graphène, en introduisant des défauts tels que des liaisons pendantes et des ouvertures nanométriques de manière contrôlée et uniforme. Ces défauts agissent alors comme des sites de nucléation préférentielle,

permettant une nucléation efficace et orientée par rapport au substrat. La couche complète est ensuite obtenue par surcroissance épitaxiale et coalescence au-dessus du graphène, fournissant une interface VdW faiblement liée et adaptée au détachement de la membrane. Le traitement au plasma d'oxygène a été utilisé pour créer divers défauts dans le graphène, qui ont ensuite été caractérisés par la spectroscopie Raman et XPS. La nucléation subséquente a révélé que les ouvertures nanométriques sont nécessaires pour fournir des liens directs avec le substrat et former une couche de germination adaptée à la croissance. L'approche APN a été démontrée sur la croissance de couches de Ge monocristallines de haute qualité au-dessus du substrat recouvert de graphène modifié. Les résultats TEM ont fourni des preuves claires de la qualité cristalline des couches sans aucune contrainte.

Notons que la croissance épitaxiale assistée par graphène de couches non polaires sur substrats non polaires démontré dans ce travail représente un grand avancement dans le domaine. Malgré toutes les avancées dans ce domaine, ceci n'était jusqu'à maintenant pas possible. Ce travail a démontré non seulement mis au point cette nouvelle approche, mais aussi la haute qualité des couches qui en résultent qui peuvent être utilisées pour la fabrication des dispositifs de haute performance. De plus, le traitement plasma offre une solution rapide et économique pour l'ingénierie de l'interface 2D, qui peut être intégrée directement dans la chambre de croissance, comparant aux autres méthodes complexes comme la lithographie par faisceau électron. Nous ouvrons un boulevard d'opportunités de nouveaux matériaux et d'hétérostructures hybrides pour de nouvelles générations de dispositifs à haute performance qui répondent aux exigences de la nouvelle ère technologique. Cette découverte pourrait être la clé pour l'intégration efficace du silicium avec les semi-conducteurs III-V, sujet à débat depuis quatre décennies.

Ces résultats posent les bases pour le développement de nouveaux matériaux en forme de FSM, et de structures hétérogènes hybrides et fortement désaccordées pour la prochaine génération de dispositifs à haute performance.

Avancées scientifiques :

- Démonstration de couches non polaires de haute qualité sur substrat non polaire par épitaxie assistée par matériaux 2D.

- Mise en œuvre de l'ingénierie de surface du graphène par traitement plasma pour créer des ouvertures nanométriques dans le réseau de graphène.
- Compréhension du processus de nucléation sur des substrats de graphène modifié, et du transfert d'orientation cristalline à travers les ouvertures nanométriques.
- Démonstration de membranes de Ge monocristallines de haute qualité sur des substrats recouverts de graphène.

7.1.2 Décollement par porosification

La deuxième partie de cette thèse (Chapitres IV-VI) se concentre sur le développement d'un processus pour la fabrication des FSMs à base de semi-conducteurs du groupe IV, utilisant le décollement par porosification. Tout d'abord, nous démontrons la fabrication de couches de PGe uniformes de bord à bord à l'échelle de la plaque de 100 mm. Cela a été rendu possible par un processus BEE optimisé, qui introduit une étape de repos supplémentaire dans le cycle de gravure/passivation et utilise une solution électrolytique avec une tension de surface réduite et une densité de courant de passivation faible. Toutes ces optimisations limitent l'accumulation du gaz H_2 dans les pores, empêchant la formation de défauts et d'inhomogénéités dans la structure PGe. De plus, la modulation des propriétés physiques du PGe, telles que l'épaisseur et la porosité, est rendue possible par la variation de la densité du courant de gravure et du temps total de traitement, respectivement. Une cellule de porosification sur mesure a été réalisée pour permettre la formation de couches PGe de bord à bord, résultant en une augmentation de la surface utile de PGe de haute qualité de plus de 25 % par plaque de 100 mm par rapport aux cellules de porosification conventionnelles. Pour évaluer les caractéristiques des couches PGe, sans la nécessité de cliver l'échantillon, des techniques de caractérisation non destructives par XRR et ellipsométrie ont été mises au point. Elles fournissent une option de caractérisation rapide et non destructive, permettant l'évaluation de l'uniformité du PGe sur toute la surface. Les couches PGe résultantes ont démontré une excellente homogénéité avec une variation inférieure à 2 % en épaisseur et en porosité. L'analyse TEM et XRD a démontré que la structure PGe maintient l'orientation cristalline originale du substrat, sans aucune flexion ou désorientation des cristallites. Ensemble avec la rugosité de surface inférieure à 3 nm, cela rend les structures PGe produites un excellent substrat pour la croissance épitaxiale.

Ces résultats ouvrent les possibilités pour la fabrication de couches de PGe avec des propriétés adéquates et convenables pour la croissance épitaxiale et ainsi que d'autres applications.

Ensuite, ces structures de PGe ont été utilisées pour étudier les étapes initiales de nucléation de la croissance épitaxiale sur les substrats poreux à basse température, révélant expérimentalement deux régimes de croissance distincts. Initialement, la croissance est dominée par la nucléation 3D au-dessus des parois des pores, suivie par la coalescence des germes. Nous avons démontré qu'une fois que la membrane de Ge atteint l'épaisseur critique de coalescence, elle devient entièrement densifiée, le mode de croissance change en régime de croissance couche par couche. À ce stade, l'épaississement supplémentaire de la membrane de Ge aide à éliminer les éventuels puits à la surface, et à obtenir une faible rugosité en dessous de 1 nm. Nous avons montré que l'épaisseur critique de coalescence dépend de la porosité du substrat, les couches à haute porosité nécessitant plus de matériel pour former une membrane entièrement coalescée au-dessus. L'analyse XRD a démontré la nature monocristalline des membranes déposées, indépendamment de la porosité du substrat. La croissance à basse température ($T \leq 300$ °C) permet de maintenir la structure PGe inchangée pendant le processus, permettant même la croissance sur des substrats de haute porosité. De plus, l'utilisation de substrats de haute porosité avec des cristallites nanométriques fournit une couche de séparation idéale, permettant le détachement et la formation des FSMs. Ces découvertes ouvrent la voie à la croissance à basse température et à la fabrication des FSMs à partir de matériaux à petit band gap tel que les alliages Ge(Si)Sn pour des applications en optoélectronique et photonique de proche/moyen IR.

Enfin, les résidus de PGe, hautement poreux sur la surface du substrat après le détachement permettent un processus de nettoyage facile et la réutilisation du substrat pour la production de multiples FSMs. La récupération de l'ensemble du substrat de 100 mm a été réalisée par gravure chimique lente dans H_2O_2. Les cristallites nanométriques, avec une grande surface spécifique du PGe restant sur le substrat, permettent leur dissolution complète, sans la nécessité d'une gravure substantielle du matériel du substrat, et l'obtention d'une rugosité de surface en dessous de 1 nm. Cela rend possible la réutilisation réussie du substrat résultant en une nouvelle couche PGe hautement uniforme. Cela ouvre

les possibilités pour une multiréutilisation du substrat pour la production des FSMs avec une consommation d'environ 300 nm du substrat par cycle, réduisant considérablement la consommation de matériaux rares par rapport aux substrats conventionnels.

Dans l'ensemble, ce travail démontre le process de décollement par porosification pour la production des Ge FSMs de haute qualité et la réutilisation du substrat à l'échelle de plaque, avec le potentiel de son application pour autres matériaux du groupe IV comme les alliages Ge(Si)Sn. Ce process réduit significativement la consommation de matériaux couteux et rates comparant aux substrats conventionnels, ouvrant la voie à la fabrication économique d'optoélectronique légère et flexible.

Avancées scientifiques :

- Fabrication de couches PGe uniformes et de haute qualité par BEE.
- Développement de nouveaux outils de porosification pour des couches PGe (bord à bord) sur des wafers entiers.
- Modulation de l'épaisseur et de la porosité du PGe par variation du temps et de la densité de courant de gravure.
- Caractérisation non destructive et rapide des couches PGe pour l'évaluation de l'uniformité.
- Établissement des mécanismes de nucléation et de croissance sur PGe.
- Démonstration de la croissance de membranes monocristallines de Ge de haute qualité sur des substrats PGe à basse température.
- Détachement de FSM de Ge à l'échelle du wafer de 100 mm.
- Mise en œuvre d'un processus de reconditionnement chimique permettant la réutilisation du substrat.
- Reporosification du substrat reconditionné.

7.2 Perspectives

Les FSMs des matériaux IV présentent une technologie puissante qui peut révolutionner notre approche de l'hétérointégration et de la fabrication de la prochaine génération d'électronique et d'optoélectronique. Bien que ce travail ait apporté des avancées importantes pour l'épitaxie assistée par des matériaux 2D, l'ingénierie des substrats et la fabrication de FSMs en Ge, il reste encore beaucoup d'opportunités et de potentiel pour des améliorations et développements futurs. La partie suivante décrit une liste non exhaustive de perspectives pour les processus développés dans ce travail.

7.2.1 Épitaxie assistée par 2D

Le chapitre III de ce travail introduit la nucléation par points d'ancrage, une approche novatrice pour la croissance de membranes de semi-conducteurs non polaires par épitaxie assistée par 2D. Cela est réalisé par la formation de nanotrous dans le graphène par traitement plasma, créant des sites de nucléation préférentiels et des liens directs avec le substrat, permettant une surcroissance latérale sur la couche intermédiaire 2D restante, conduisant à une interface VdW faible. Cela permet la croissance de couches de haute qualité sans nécessité d'interactions ioniques à travers l'interface 2D. Pour améliorer et faire avancer cette technologie, les études suivantes peuvent être envisagées (dans un ordre quelconque) :

- **Qualité de l'interface 2D**

  La qualité de l'interface 2D joue un rôle crucial dans la croissance par épitaxie assistée par matériaux 2D[357]. Le principal défi du graphène transféré par voie humide (utilisé dans ce travail) est la présence de résidus de PMMA à la surface, créant des sites de nucléation indésirables pouvant entrainer des défauts dans la structure. Pour résoudre ce problème, une technique de transfert à sec peut être utilisée[142]. Alternativement, du graphène monocristallin de haute qualité peut être cru sur un substrat de Ge pour être utilisé dans l'épitaxie assistée par matériaux 2D.

- **Ingénierie des interfaces 2D amorphes**

  Pour permettre une interface 2D sans transfert sur une grande variété de substrats, des études récentes suggèrent qu'une monocouche de carbone amorphe peut être

utilisée comme interface 2D à la place du graphène[147]. Combinée à l'approche APN, cette option présente un fort potentiel pour une épitaxie assistée par 2D universelle.

- **Influence de la source de plasma**

  L'influence du traitement plasma sur la formation de défauts dans l'interface 2D doit être étudiée, car le contrôle précis de la formation des nanotrous est nécessaire pour l'approche APN. Des sources de plasma chimiquement inertes telles que l'argon ou l'hydrogène doivent être prises en considération, ainsi que le plasma d'azote qui peut également provoquer le dopage du graphène par insertion d'atomes de N dans le réseau.

- **Adaptation des sites de nucléation**

  L'influence de la densité et de la taille des nanotrous sur la force d'adhésion de la couche épitaxiée présente une voie importante pour le détachement contrôlé des FSMs et la modulation de l'adhésion pour divers procédés de fabrication de dispositifs.

- **Démonstration de l'APN pour d'autres matériaux**

  Des études futures devraient se concentrer sur la démonstration et l'application de l'approche APN à d'autres types de matériaux, notamment les matériaux III-V, III-N et divers alliages du groupe IV. Cela prouvera la nature universelle de l'approche pour la fabrication de FSMs de semi-conducteurs.

- **Hétérointégration sur Si par APN**

  L'hétérointégration de matériaux dissimilaires le Si est l'une des tâches les plus difficiles en épitaxie. L'approche APN a un fort potentiel pour accomplir cette tâche, car la nucléation locale permet d'orienter la couche épitaxiée le long du substrat Si non polaire, tandis que la surcroissance sur l'interface 2D permet la relaxation de la couche, évitant la formation de défauts dans le processus.

7.2.2 Porosification des substrats

Les résultats présentés dans ce travail, exposé dans le chapitre IV, ont démontré des avancées significatives dans la production de couches PGe uniformes de bord à bord sur des wafers de 100 mm, avec une épaisseur et une porosité réglable en utilisant des outils

de porosification innovants[287]. De plus, les techniques XRR et ellipsométrie ont été démontré pour la caractérisation non destructive des structures PGe, fournissant un retour rapide sur la qualité du PGe pour la production. Les développements futurs devraient se concentrer sur l'amélioration des techniques de caractérisation, l'augmentation de l'échelle de la fabrication de PGe, des processus BEE plus rapides, plus contrôlables et plus durables, ainsi que sur la fabrication de structures PGe complexes, stratifiées et/ou profondément gravées. Les objectifs de recherche suivants peuvent être envisagés :

- **Amélioration des mesures d'ellipsométrie**

  En utilisant le spectre IR moyen en plus du spectre visible et proche IR, les mesures d'ellipsométrie peuvent être considérablement améliorées, car le Ge est complètement transparent dans ce domaine. Cela peut être utilisé pour la caractérisation des structures PGe épaisses ou des multicouches de PGe. Des améliorations supplémentaires dans l'ajustement des mesures d'ellipsométrie peuvent ensuite conduire à une estimation de la rugosité de surface ou à l'identification de la présence d'oxyde due au vieillissement des couches PGe.
- **Formation des couches PGe uniformes à l'échelle de wafers de 200 et 300 mm**

  Comparés à d'autres substrats de matériaux rares, les wafers de Ge peuvent être produits même à une taille de 300 mm[340], représentant une surface presque 10 fois plus grande que les wafers de 100 mm utilisés dans ce travail. Cela constitue une réalisation importante à atteindre, offrant des rendements beaucoup plus élevés par wafer. Cependant, une augmentation de surface aussi importante peut révéler des variations ou des limitations du processus de porosification précédemment invisibles. Elle peut également induire la formation de défauts en raison d'un courant plus élevé impliqué dans le processus. Pour ces raisons, il est important d'étudier l'influence de la surface sur le processus BEE, en particulier pour les tailles de wafer au-delà de 100 mm.
- **Développement d'outils de porosification**

  Les outils de porosification utilisés dans ce travail permettent une porosification uniforme de bord à bord. Cependant, ils utilisent une électrode arrière en cuivre qui est sujette à l'oxydation et/ou à la corrosion de surface et nécessite un entretien régulier. De plus, le cuivre est considéré comme un élément

indésirable/contaminant pour de nombreux processus de fabrication de semi-conducteurs et doit donc être évité, même si le risque de contamination lors du processus BEE est minime et n'a pas été révélé lors des études actuelles. D'autres matériaux conducteurs similaires, offrant une meilleure résistance à la corrosion et à l'oxydation, devraient être étudiés et envisagés pour cet élément crucial. Alternativement, des cellules de gravure double face, impliquant un électrolyte des deux côtés du substrat de Ge. Cette approche présente un potentiel, notamment pour la formation de membranes PGe, car les deux côtés du wafer sont gravés simultanément[213]. Cependant, un mécanisme de fixation spéciale du wafer doit être développé pour permettre des couches PGe de bord à bord en utilisant cette technologie.

- **Suivi potentiométrique du processus BEE**

  Des études annexes (non incluses dans ce travail) ont montré que la réponse potentielle du système évolue au cours de la durée du BEE[209]. Les résultats montrent une variation importante de la réponse potentielle au cours du temps, particulièrement remarquable lors de l'étape de passivation. Cela suggère que le degré de passivation change au cours du processus, ce qui peut être la cause des difficultés de formation de couches PGe très épaisses (centaines de µm) à ce jour. Des études potentiométriques supplémentaires du processus, combinées à d'autres analyses in-situ, pourraient fournir une nouvelle compréhension fondamentale du processus et de sa cinétique, ainsi que révéler le lien manquant entre la BEE conventionnelle et rapide du Ge.

- **BEE potentiostatique**

  Le suivi potentiométrique du processus BEE galvanostatique conventionnel a également révélé que divers niveaux de réponse potentielle aboutissent à différentes structures de PGe[209]. Cela ouvre la possibilité de fabriquer des couches PGe avec diverses propriétés morphologiques, ainsi que la formation de structures PGe stratifiées en utilisant une approche BEE potentiostatique, qui était jusqu'à très récemment un territoire complètement inexploré pour la formation de couches PGe[209,349].

- **Composition de l'électrolyte**

  Les résultats présentés dans le chapitre IV ont montré que la composition de la solution électrolytique joue un rôle important dans la formation du PGe et son homogénéité. Bien que diverses études dans la littérature aient utilisé différentes solutions électrolytiques, leur influence sur les taux de gravure et la morphologie résultante du PGe n'a pas été étudiée et reste pour le moment inconnue.

- **Réutilisation de l'électrolyte**

  Actuellement, un électrolyte vierge est toujours utilisé pour la formation de PGe, ce qui entraine de grandes quantités de déchets d'électrolyte. De plus, il présente un mélange de solutions aqueuses hautement acides et de solvant hygroscopique nécessitant un traitement spécial pour séparer et neutraliser les deux composants. En considérant qu'une faible épaisseur du PGe (max quelques µm) est utilisée dans la plupart des applications, la solution électrolytique concentrée pourrait être réutilisée pour la production de plusieurs couches PGe. Cependant, l'influence des complexes de Ge dissouts dans la solution et de l'évaporation du solvant sur la formation du PGe doit être étudiée.

- **Porosification du Ge de type n**

  Le Ge de type n, qui a de nombreuses applications en électronique et optoélectronique, présente des opportunités uniques pour la formation de structures PGe, car il peut offrir une variété de structures morphologiques et potentiellement des taux de gravure plus élevés, mais aussi une forte photoactivation du processus BEE. Pour le moment, principalement la porosification du Ge de type p a été étudiée, donc le Ge de type n offre beaucoup à explorer.

7.2.3 Fabrication de FSMs du groupe IV

Le chapitre V introduit l'approche pour la fabrication de FSMs en Ge par croissance à basse température sur des substrats de PGe et pour le détachement ultérieur. La basse température permet de maintenir la structure PGe avec des nanocristallites non reconstruites, tout en permettant la formation d'une membrane de haute qualité. La couche PGe non reconstruite permet ensuite un détachement facile et une réutilisation du substrat.

Cela ouvre la voie à de nouveaux développements et applications de ce processus. Les objectifs de recherche suivants peuvent être envisagés :

- **Formation de membranes par d'autres techniques**

  Les membranes de Ge dans ce travail ont été formées par la croissance MBE à basse température. Ces conditions sont également adaptées à d'autres techniques de dépôt telles que la déposition chimique en phase vapeur, le dépôt par pulvérisation ou l'évaporation, qui sont plus courantes dans les applications industrielles. La formation de FSMs utilisant ces techniques doit être explorée pour mieux préparer le processus à un transfert industriel.

- **Influence des propriétés du PGe sur l'adhésion du FSM**

  Puisque dans le processus développé dans cette thèse, la couche PGe ne subit aucune transformation, l'adhésion de la membrane dépend uniquement des propriétés physiques de la couche PGe. En explorant la force d'adhésion de la membrane en fonction de l'épaisseur et de la porosité du PGe, elle peut être adaptée à divers processus de fabrication en fonction de l'application prévue.

- **Fabrication des FSMs d'alliages du groupe IV**

  Les conditions de basse température du processus ouvrent la possibilité de son application à d'autres alliages du groupe IV, en particulier les alliages Ge(Si)Sn, qui sont prometteurs dans les applications de proches/moyennes IR.

- **Développement de techniques de manipulation et de transfert adaptées**

  Les FSMs apportent de nouveaux défis en termes de manipulation par rapport aux substrats rigides traditionnels. Cela nécessite le développement de techniques de manipulation et de transfert adaptées pour faciliter le travail avec les FSMs.

- **Stabilisation du PGe pour la croissance à haute température**

  La structure PGe est très instable à haute température et subit une reconstruction thermique, limitant les applications du processus aux matériaux compatibles avec la croissance à basse température. Cependant, sur la base de nos résultats préliminaires, le PGe peut être stabilisé par le dépôt, par exemple, d'une fine couche de carbone à l'intérieur de la nanostructure, fournissant la stabilité nécessaire à haute température et permettant la croissance et la fabrication de FSMs III-V.

- **Application des FSMs dans la fabrication de dispositifs**

  L'étape la plus évidente pour ce processus est son application dans la fabrication d'un dispositif tel qu'une cellule TPV ou un détecteur IR.

7.4.4 Nettoyage et réutilisation des substrats

Les chapitres V et VI proposent et démontrent le processus de nettoyage de la structure PGe restante sur le substrat parent par gravure chimique lente. Cela permet la dissolution du PGe sans perte significative de matériau, tout en créant une surface lisse adaptée à la réutilisation du substrat. Les objectifs suivants peuvent être envisagés pour le développement futur de cet axe de recherche :

- **Évaluation d'autres solutions de gravure**

  La gravure chimique lente des résidus de PGe dans le H_2O_2 a montré des résultats prometteurs pour le nettoyage des substrats après le détachement de la membrane. Néanmoins, d'autres solutions telles que HNO_3, ou des solutions comprenant de faibles concentrations d'agents de gravure tels que HF, HCl ou H_2PO_3, peuvent être envisagées. Des agents supplémentaires comme l'acide acétique peuvent être ajoutés pour améliorer le mouillage du substrat avec la solution de gravure.
- **Influence des réutilisations multiples du substrat sur la qualité de surface**

  Le présent travail a démontré une réutilisation réussie du substrat sans influence significative sur la qualité du PGe. Pour valider davantage ce point, la qualité de surface du substrat doit être évaluée sur plusieurs cycles pour évaluer l'éventualité d'une augmentation de la rugosité de surface, ce qui nécessiterait un reconditionnement par la gravure plus profonde ou un processus CMP.

7.3 Conclusions (English)

Semiconductor freestanding membranes offer many advantages, such as lightweight and flexibility, compared to heterostructures on conventional bulk substrates. Moreover, their extra degree of liberty opens many possibilities for the development of innovative fabrication processes and novel devices empowered by membrane transfer and/or stacking. The fabrication of semiconducting FSMs offers a unique opportunity not only for cost saving and rare material use reduction, but also for the introduction and development of membrane-based next generation of microelectronics and optoelectronics.

This thesis reviews the various possible approaches for the fabrication of semiconductor FSMs, summarizing the advantages and limits of each currently available FSMs fabrication technique. This shows us that despite all the progress made, there is still a long way to go for FSMs to become industrially viable solution and replacement for conventional substrates. Although the fabrication of III-V and III-N FSMs has demonstrated huge advancements, the methods enabling formation of group IV semiconductor membranes are very limited. In this thesis, we focus on the development of novel substrate engineering and growth techniques enabling fabrication of group IV material FSMs using 2D-assisted epitaxy and porosification lift-off.

7.3.1 2D-assisted epitaxy

The first part of this work (Chapter III) focuses on overcoming the challenges of 2D-assisted epitaxy for the growth of non-polar materials which cannot be grown using RE or QVdW techniques. We introduce a novel APN approach enabling the monolithic integration of non-polar 3D semiconductors on 2D materials and fabrication of FSMs. It relies on the surface engineering of the graphene, introducing defects such as dangling bonds and nanoholes in a controlled and uniform way. These defects then act as preferential nucleation sites, allowing for efficient, substrate-oriented nucleation. The complete layer is then obtained by epitaxial overgrowth and coalescence on top of the graphene, providing weak VdW interface suitable for the detachment of the membrane. The oxygen plasma treatment was used to create various defects in the graphene, which were then characterized by Raman spectroscopy and XPS. Subsequent nucleation revealed that nanohole defects are necessary to provide direct links with the substrate and form seeding layer suitable for

growth. The APN approach was demonstrated on the growth of defect-free single-crystalline Ge layers on top of the engineered graphene covered substrate. The TEM results provided clear evidence of the crystalline quality of the layers without any strain.

It should be noted that graphene-assisted epitaxy of non-polar layers on non-polar substrates demonstrated in this work is a tremendous achievement in this domain. Despite all the advances in this area, this has not been possible until now. This work has demonstrated not only the proof-of-concept of this novel approach, but also the high quality of the resulting epilayers which can be used in the fabrication of high-performance devices. Moreover, the plasma treatment offers a fast and cost-effective solution for 2D interface engineering, which can be directly integrated in growth chambers, compared to other expensive techniques such as electrolithography. These results lay the groundwork for new FSM materials and hybrid and highly mismatched heterostructures for the next generation of high-performance devices.

Scientific advancements:

- Demonstration of high-quality non-polar layers on a non-polar substrate by 2D-assisted epitaxy.
- Implementation of graphene surface engineering by plasma treatment to create nanometric openings in the graphene lattice.
- Unraveling the nucleation process on engineered graphene substrates, along with the through-hole crystal orientation transfer.
- Demonstration of high-quality, monocrystalline Ge membranes over graphene-covered substrates.

7.3.2 Porosification lift-off

The second part of this thesis (Chapters IV-VI) concentrates on the development of a scalable process for fabrication of group IV semiconductor FSMs, using porosification lift-off. We have demonstrated the fabrication of edge-to-edge, uniform PGe layers at 100 mm wafer-scale. This was made possible by optimized BEE process that introduces additional rest time step into the etching/passivation cycle and uses an electrolyte solution with reduced surface tension and low passivation current density. All these optimizations limit

the accumulation of the H_2 gas in the pores, efficiently avoiding the formation of defects and inhomogeneities in the PGe structure. Moreover, the modulation of the PGe's physical properties, such as thickness and porosity, is enabled by variation of the etching current density and total process time, respectively. A custom porosification cell has been made to enable the formation of edge-to-edge PGe layers, resulting in the increase of the high-quality PGe surface by over 25% per 100 mm wafer compared to conventional porosification cells. To assess the characteristic of the PGe layers, without the necessity to cleave the sample, XRR and ellipsometry characterization techniques has been introduced. They provide the fast feedback, non-destructive characterization option, allowing the evaluation of the PGe uniformity over the entire surface. The resulting PGe layers demonstrated excellent homogeneity with variation inferior to 2% in both the thickness and porosity. The TEM and XRD analysis demonstrated that the PGe structure maintains the original crystal orientation of the substrate, without any bending or misorientation of the crystallites. With the addition of the surface roughness below 3 nm, this makes produced PGe structures an excellent substrate for epitaxial growth. These results open the possibilities for fabrication of PGe layers with on-demand properties for epitaxial growth and other applications.

Moreover, these PGe structures were then used to study initial nucleation stages of the growth on porous nanostructure at low temperatures, experimentally revealing two distinct growth regimes. Initially, the growth is dominated by 3D nucleation on top of the pore walls, followed by the coalescence of the seeds. We demonstrated that once the Ge membrane reaches the critical thickness of coalescence, a fully densified membrane is formed, and the growth becomes governed by 2D layer-by-layer regime. At this point, further thickening of the Ge membrane helps to annihilate any remaining pits on the surface, and to achieve low roughness below 1 nm. We have shown that the critical thickness of coalescence depends on the porosity of the substrate, as the high porosity layers necessitate more material to form a fully coalesced membrane on top. The XRD analysis has demonstrated the monocrystalline nature of grown membranes independently of the porosity of the substrate. The low temperature growth ($T \leq 300$ °C), allows for maintaining the PGe structure unchanged during the process, enabling the growth even on high porosity substrates. Moreover, the high porosity structure with nanometric crystallites

provides an ideal separation layer, enabling the detachment and formation of the Ge membrane. These findings pave the way for low-temperature growth and fabrication of FSMs from small bandgap materials such as Ge(Si)Sn alloys for applications in near/mid-IR optoelectronics and photonics.

Finally, the PGe remnants on the substrate surface after the detachment, allow an easy cleaning process by and reuse of the substrate for production of multiple Ge FSMs. The recovery of the entire 100 mm substrate has been achieved through slow chemical etching in H_2O_2. The nanometric crystallites with high specific area of the PGe remaining on the substrate, allow their complete dissolution, without the necessity of substantial etching of the substrate material, and obtention of the surface roughness below 1 nm. This makes possible the successful reuse of the substrate resulting in a new highly uniform PGe layer. This opens the possibilities for multi-reuse of the substrate for production of FSMs with consumption of only ~300 nm of the substrate per cycle, significantly reducing the consumption of rare materials compared to conventional substrates.

Overall, this work demonstrates a wafer-scale porosification lift-off process for production of high-quality Ge FSMs and substrate reuse, with high potential of its adoption for other group IV materials such as Ge(Si)Sn alloys. This process significantly reduces the consumption of rare and expensive materials compared to conventional bulk substrates, paving the way for cost-effective fabrication of light and flexible optoelectronics.

Scientific advancements:

- Fabrication of uniform high-quality PGe layers by BEE.
- Development of new porosification tools for edge-to-edge PGe layers on entire wafers.
- PGe thickness and porosity modulation by time and etching current density variation.
- Fast feedback, non-destructive characterization of PGe layers for uniformity assessment.
- Establishment of nucleation and growth mechanisms on PGe substrates.
- Demonstration of high-quality growth monocrystalline Ge membranes on PGe substrates at low temperatures.

- Detachment of 100 mm wafer-scale Ge FSM.
- Implementation of a chemical reconditioning process allowing the substrate reuse.
- Reporosification of reconditioned substrate.

7.4 Perspectives

The FSMs of IV materials present a powerful technology which can shake up the way how we approach the heterointegration and fabrication of the next generation of electronics and optoelectronics. Although this work has brought important milestones for 2D-assisted epitaxy, substrate engineering and Ge FSMs fabrication, there are still lots of opportunities and potential for further improvements and development. The following part describes a non-exhaustive list of perspectives for processes developed in this work.

7.4.1 2D-assisted epitaxy

The Chapter III of this work introduces Anchor Point Nucleation, a novel approach for growth of non-polar semiconductor membranes by 2D-assisted epitaxy. This is achieved through formation of nanoholes in the graphene by plasma treatment, creating preferential nucleation sites and direct links with the substrate, providing lateral overgrowth over remaining 2D interlayer, and leading to the weak VdW interface. This enables the growth of high-quality layer without the necessity of the ionic interactions through the 2D interface. To further improve and advance the technology following studies can be considered (in no particular order):

- **2D interface quality**

  Quality of the 2D interface plays a crucial role in the growth by 2D-assisted epitaxy[357]. The main challenge of the wet-transfer graphene (used in this work) is the presence of PMMA residues on the surface resulting causing unwanted nucleation sites which can result in defects in the structure. To resolve this issue, dry-transfer technique can be employed[142]. Alternatively, high-quality single crystalline graphene can be grown on top of Ge substrate to be further used for 2D-assisted epitaxy.

- **Engineering of amorphous 2D interfaces**

  Alternatively, to enable transfer-free 2D interface on a large variety of substrates, recent studies suggest that for RE and engineered 2D interface, an amorphous carbon monolayer can be used as the 2D interface instead of the graphene[147]. Combined with APN approach, this option presents a high potential for universal 2D-assisted epitaxy.

- **Influence of the plasma source**

  The plasma treatment influence on the defect formation in 2D interface should be further studied, as the precise control of the nanohole formation is necessary for APN approach. Chemically inert plasma sources such as Argon or Hydrogen should be taken into consideration as well as nitrogen plasma which can also cause the doping of the graphene by insertion of the N atoms in the lattice.

- **Tailoring of the nucleation sites**

  The influence of the nanohole density and size on the epilayer adhesion strength present an important pathway for the controlled detachment of the FSMs and modulation of the adhesion for various device processing methods.

- **Demonstration of APN for other materials**

  Further studies should focus on demonstrating and applying the APN approach for other types of materials, namely III-V, III-N, and various group IV alloys. This will prove the universal nature of the approach for the fabrication of semiconductor FSMs.

- **Heterointegration on Si through APN**

  Heterointegration of highly dissimilar materials on Si is one of the most challenging tasks in epitaxy. The APN approach has a high potential to achieve this task, as the local nucleation allows orienting the epilayer along the non-polar Si substrate while the overgrowth over the 2D interface enables the relaxation of the layer, avoiding the formation of defects in the process.

7.4.2 Substrate porosification

The results in this work, presented in Chapter IV, have demonstrated significant advancement in production of uniform edge-to-edge PGe layers over 100 mm wafers, with tunable thickness and porosity using innovative porosification tools[287]. Additionally, The XRR and ellipsometry techniques have proven useful for non-destructive characterization of PGe structures, providing fast feedback on PGe quality for production. The future development should focus on improvement of characterization techniques, further scale-up of PGe fabrication, faster, more controllable, and sustainable BEE process, as well as on fabrication of patterned, complex, layered, and/or deeply etched PGe structures. Following research objectives can be considered:

- **Improved ellipsometry measurements:**
  By using mid IR spectra in addition to the visible and near IR spectrum, the ellipsometry measurements can be vastly improved as the Ge is completely transparent in this domain. This can be then used for characterization of the deeply etched or layered PGe structures. Further improvements in the fitting of the ellipsometry measurements can then lead to surface roughness estimation or identification of the oxide presence due to the aging of the PGe layers.
- **Scale-up of the uniform PGe layers up to 300 mm wafer size:**
  Compared to other rare material substrate, Ge wafers can be produced even at 300 mm size[340], representing almost 10× larger surface compared to 100 mm wafers used in this work. This sets a significant milestone to achieve, offering much higher per wafer yields. However, such an important surface increase can uncover previously unseen PGe variations or limitations in porosification tools. It can also induce formation of defects due to a significantly higher current involved in the process. For these reasons it's important to study the influence of the surface area on BEE process, especially for wafer sizes beyond 100 mm.
- **Porosification tools development:**
  Porosification tools used in this work enable an edge-to-edge uniform porosification. However, they use Cu back electrode which is prone to surface oxidation and/or corrosion and necessitate regular maintenance. Moreover, Cu is

considered as an undesirable/contaminant element for many semiconductors fabrication processes and for this reason it should be avoided, even if the risk of contamination during BEE process is minimal and hasn't been uncovered during present studies. Other similarly conductive materials, offering better corrosion and oxidation resistance should be studied and considered for this crucial component. Alternatively, double sided etching cells, involving electrolyte on both sides of the Ge substrate[213]. This approach holds potential especially for PGe membranes formation as both sides of the wafer are etched simultaneously. However, a development of special wafer fixation mechanism needs to be developed to enable edge-to-edge PGe layers using this technology.

- **Potentiometric monitoring of BEE process**

  Annex studies (not included in this work) have demonstrated that the potential response of the system evolves over the duration of the BEE[209]. The results show an important variation in potential response over time, which is the most remarkable on passivation step. This suggests that the degree of passivation change over the duration of the process, which can by the cause of why the very thick PGe layers (hundreds of μm) have not been yet achieved. Further potentiometric studies of the process, combined with others in-situ analysis, could provide a new fundamental understanding of the process and its kinetics, as well as uncover the missing link between the conventional and fast BEE of Ge.

- **Potentiostatic BEE**

  Potentiometric monitoring of the conventional galvanostatic BEE process has also revealed that various levels of potential response results in different PGe structures[209]. This opens the possibility for fabrication of PGe layers with various morphological properties as well as formation of layered PGe structures using Potentiostatic BEE approach which was until very recently[209,349] completely uncharted territory for PGe layer formation.

- **Electrolyte composition**

  Results presented in Chapter IV have shown that the composition of the electrolyte solution plays an important role in PGe formation and its homogeneity. Although, various studies in literature have used different electrolyte solutions, their influence

on etching rates and resulting PGe morphology has not been studied and remains for the moment unknown.

- **Electrolyte reuse**

  Currently, a fresh electrolyte is always used for PGe formation, resulting in large quantities electrolyte waste. Moreover, it presents a mixture of highly acidic aqueous solution and hygroscopic solvent necessitating special treatment to separate and neutralize both components. Considering generally low PGe thickness (max few μm) for most of the applications, the concentrated electrolyte solution could be reused for production of multiple PGe layers. However, the influence of Ge complexes dissolved in the solution and solvent evaporation, on PGe formation should be studied.

- **Porosification of n-type Ge**

  The n-type Ge, which has many applications in electronic and optoelectronic, presents some unique opportunities for formation of PGe structures as it can offer a variety of morphological structures and potentially higher etching rates, but also high photoactivation of the BEE process. For the moment, mainly p-type Ge porosification has been studies, thus the n-type Ge offers a lot to explore.

7.4.3 Fabrication of group IV FSMs

Chapter V introduces the approach for Ge FSMs fabrication through low temperature growth on PGe substrates and subsequent detachment. The low temperature enables us to maintain the PGe structure with nanometric crystallites unreconstructed, while still allowing for the formation of high-quality membrane. The unreconstructed PGe layer then enables an easy detachment and substrate reuse. This paves the way for further development and applications of this process. Following research objectives can be considered:

- **Membrane formation by other techniques**

  The Ge membranes in this work were formed using MBE growth at low temperatures. These conditions are also suitable for other deposition techniques such as chemical vapor deposition, sputtering, or evaporation, which are more

common in industrial applications. The formation of FSMs using these techniques should be explored to better prepare the process for industrial transfer.

- **Influence of the PGe's properties on FSM adhesion**

  Since in the process developed in this thesis, the PGe layer does not undergo any transformation, the adhesion of the membrane is solely dependent on the physical properties of the PGe layer. By exploring the adhesion force of the membrane as the function of the PGe thickness and porosity, it can be adapted for various fabrication processes depending on the intended application.

- **Fabrication of group IV alloys FSMs**

  The low temperature condition of the process opens up the opportunity for its application on other group IV alloys, especially Ge(Si)Sn alloys, which are prominent in near/mid IR applications.

- **Development of adapted handling and transfer technique**

  FSMs bring new challenges in terms of handling compared to traditional rigid substrates. This necessitates the development of adapted handling and transfer techniques to facilitate the work with FSMs.

- **Stabilization of the PGe for high-temperature growth**

  The PGe structure by itself is very unstable at high temperatures and undergoes a thermal reconstruction, limiting the applications of the process to materials compatible with low temperature growth. However, based on our preliminary results the PGe can be stabilized by deposition of for example thin carbon layer inside the nanostructure, providing much-needed stability at high temperatures and enabling the growth and fabrication of III-V FSMs.

- **Application of FSMs in device fabrication**

  The most evident next step for this process is its application in fabrication of a device such as TPV cells or IR detectors.

7.4.4 Substrate cleaning and reuse

Chapters V and VI propose and demonstrate the cleaning process of the PGe structure remaining on the parent substrate using slow chemical etching. This enables the PGe dissolution without a significant loss of material, while creating a smooth surface suitable for substrate reuse. Following objectives may be considered for further development of this research axis:

- **Evaluation of other etching solutions**

  The slow chemical etching of PGe remnants in H_2O_2 has shown promising results for substrate cleaning after the membrane detachment. Nevertheless, other solutions such as HNO_3, or solutions including low concentrations of etching agents such as HF, HCl of H_2PO_3. Additional agents such as acetic acid can be added to improve the wetting of the substrate with the etching solution.

- **Influence of the multiple substrate reuses on surface quality**

  The present work has demonstrated a successful substrate reuse without any significant influence on the PGe quality. To further validate this point, the surface quality of the substrate should be evaluated over multiple cycles to evaluate the eventuality of the surface roughness increase, which would necessitate the reconditioning by removal of more material or CMP process.

Appendix

8. Scientific Contributions, Awards and Distinctions

8.1 Publications

8.1.1 Principal contribution

1) **Tadeáš Hanuš**, Bouraoui Ilahi, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif; Sustainable production of ultrathin Ge freestanding membranes, Sustainability; 2024, 16(4), 1444 (https://doi.org/10.3390/su16041444)
2) **Tadeáš Hanuš**, Laurie Mouchel, Arthur Dupuy, Bouraoui Ilahi, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif; Unraveling potentiometric monitoring during Ge electrochemical etching: Towards tunable double porosity layers, Electrochimica Acta; 2024; 474; 143529 (http://dx.doi.org/10.1016/j.electacta.2023.143529)
3) Thierno Mamoudou Diallo, **Tadeáš Hanuš**, Gilles Patriarche, Andreas Ruediger, Abderraouf Boucherif; Unraveling the heterointegration of 3D semiconductors on graphene by Anchor Point Nucleation; Small; 202, 20, 15, 2306038 (https://doi.org/10.1002/smll.202306038)
4) **Tadeáš Hanuš**, Bouraoui Ilahi, Alexandre Chapotot, Hubert Pelletier, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif Fabrication of wafer-scale freestanding monocrystalline Ge membranes; Materials Today Advances; 2023, 18, 100373 (https://doi.org/10.1016/j.mtadv.2023.100373)
5) **Tadeáš Hanuš**, Javier Arias-Zapata, Bouraoui Ilahi, Philippe-Olivier Provost, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif; Large-Scale Formation of Uniform Porous Ge Nanostructures with Tunable Physical Properties; Advanced Materials Interfaces; 2023, 10, 2202495 (https://doi.org/10.1002/admi.202202495)
6) Nicolas Paupy, Zakaria Oulad Elhmaidi, Alexandre Chapotot, **Tadeáš Hanuš**, Javier Arias-Zapata, Bouraoui Ilahi, Alexandre Heintz, Alex Brice Poungoué Mbeunmi, Roxana Arvinte, Mohammad Reza Aziziyan, Valentin Daniel, Gwenaëlle Hamon, Jérémie Chrétien, Firas Zouaghi, Ahmed Ayari, Laurie Mouchel, Jonathan Henriques, Loïc Demoulin, Thierno Mamoudou Diallo, Philippe-Olivier Provost, Hubert Pelletier, Maïté Volatier, Rufi Kurstjens, Jinyoun Cho, Guillaume Courtois, Kristof Dessein, Sébastien

Arcand, Chrientian Dubuc, Abdelatif Jaouad, Nicolas Quaegebeur, Ryan Gosselin, Denis Machon, Richard Arès, Maxime Darnon, Abderraouf Boucherif; Wafer-scale detachable monocrystalline Ge nanomembranes for the growth of III-V materials and substrate reuse; Nanoscale Advances; 2023, 5, 4696–4702 (https://doi.org/10.1039/D3NA00053B)

8.1.2 Coauthor

1) Ahmed Ayari, Firas Zouaghi, Bouraoui Ilahi, Tadeáš Hanuš, Jinyoun Cho, Kristof Dessein, Denis Machon, Nicolas Quaegebeur, Abderraouf Boucherif; Post-growth Adhesion strength tuning of Detachable Ge Membranes via Porous Ge Transformation; Materials Science in Semiconductor Processing; 2024, 180, 108563 (https://doi.org/10.1016/j.mssp.2024.108563)
2) Ahmed Ayari, Bouraoui Ilahi, Roxana Arvinte, **Tadeáš Hanuš**, Laurie Mouchel, Jinyoun Cho, Kristof Dessein, Denis Machon, Abderraouf Boucherif, Comprehensive investigation of Thermal Induced Reorganization of Porous-Ge structures; Thin Solid Films; 2024, 798, 140391 (https://doi.org/10.1016/j.tsf.2024.140391)
3) Jinyoun Cho, Valérie Depauw, Alexandre Chapotot, Waldemar Schreiber, Tadeáš Hanuš, Nicolas Paupy, Valentin Daniel, Guillaume Courtois, Bouraoui Ilahi, Abderraouf Boucherif, Clément Porret, Roger Loo, Jens Ohlmann, Stefan Janz, Kristof Dessein; Overview of Engineered Germanium Substrate Development for Affordable Large-Volume Multi-Junction Solar Cell; IEEE Journal of Photovoltaics; 2024, 14, 4, 623-628 (https://doi.org/10.1109/JPHOTOV.2024.3390846)
4) Alexandre Chapotot, Bouraoui Ilahi, **Tadeáš Hanuš**, Gwenaëlle Hamon, Jinyoun Cho, Kristof Dessein, Maxime Darnon, Abderraouf Boucherif; Sequential generation of multiple Ge nanomembranes from a Single Substrate: Towards Sustainable Recycling of Ge Wafers; Sustainable Materials and Technologies; 2024, 39, e00806 (https://doi.org/10.1016/j.susmat.2023.e00806)
5) Valentin Daniel, Thomas Bidaud, Jérémie Chretien, Nicolas Paupy, Ahmed Ayari, Thierno Mamoudou Diallo, **Tadeáš Hanuš**, Jonathan Henriques, Abdelatif Jaouad, Jean-François Lerat, Bouraoui Ilahi, Jinyoun Cho, Kristof Dessein, Christian Dubuc, Gwenaëlle Hamon, Abderraouf Boucherif, Maxime Darnon; High efficiency GaAs solar cells grown on porous germanium substrate with PEELER technology; Solar RRL; 2024, 8, 2300643 (http://doi.org/10.1002/solr.202300643)
6) Alexandre Chapotot, Bouraoui Ilahi, Javier Arias-Zapata, **Tadeáš Hanuš**, Ahmed Ayari, Gwenaëlle Hamon, Jinyoun Cho, Kristof Dessein, Maxime Darnon, Abderraouf Boucherif;

Wet chemical etching mechanism for germanium and its application for substrate reuse; Materials Science in Semiconductor Processing; 2023, 168, 107851 (https://doi.org/10.1016/j.mssp.2023.107851)

7) Nicolas Paupy, Ahmed Ayari, Bouraoui Ilahi, **Tadeáš Hanuš**, Jinyoun Cho, Kristof Dessein, Denis Machon, Richard Arès, Abderraouf Boucherif; Tailoring Ge membrane adhesion strength: impact of growth parameters and porous layer thickness; (Under review)

8.3 Awards and Distinctions

1) **La Preuve par l'Image**, Finalist – Acfas, 2024, Canada
2) **Popular Science Award** – Université de Sherbrooke, 2024, Sherbrooke, Canada
3) **Art Award** – Raith Micrograph Award 2023
4) **Médaille de Mérite Leonard de Vinci** – Faculty of Engineering, Université de Sherbrooke, 2023, Sherbrooke, Canada
5) **Young Researcher Award** – European Material Research Society Fall Meeting 2023, Warszawa, Poland
6) **Best Presentation Award**, Finalist – The 20th Canadian Semiconductor Science and Technology Conference, 2023, Montreal, Canada
7) **Best Poster Award**, 1st place – 3IT.Nano symposium, 2023, Jouvence, Canada
8) **Young Researcher Award** – European Material Research Society Spring Meeting 2023, Strasbourg, France
9) **Graduate Student Award** – European Material Research Society Fall Meeting 2022, Warszawa, Poland

8.4 Patents

1) Semiconductor Device and Method of Manufacturing Same; Thierno Mamoudou Diallo, **Tadeáš Hanuš**, Abderraouf Boucherif (Patent pending)
2) Computer System and Method for Manufacturing a Germanium Membrane; Abderraouf Boucherif, Bouraoui Ilahi, **Tadeáš Hanuš** (Patent pending)
3) Method and System for Manufacturing a Germanium-based Membrane, and Germanium Based Substrate; **Tadeáš Hanuš**, Bouraoui Ilahi, Abderraouf Boucherif (Patent pending)

8.5 Conference organization

1) Member of organization committee - The 7th Montreal Photonics Networking Event, Montreal, Canada (2023, December 1st)
2) Member of organization committee - The 8th Montreal Photonics Networking Event, Montreal, Canada (2024)

8.6 Scientific communications

1) **Tadeáš Hanuš**, Thierno Mamoudou Diallo, Gilles Patriarche, Andreas Ruediger, Abderraouf Boucherif; (2023, December 1st) 2D-assisted epitaxy: A method for the growth of group IV semiconductor freestanding membranes; (Poster presentation), The 7th Montreal Photonics Networking Event, Montreal, Canada
2) **Tadeáš Hanuš**, Bouraoui Ilahi, Javier Arias-Zapata, Alexandre Chapotot, Hubert Pelletier, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif; (2023, September 18-21) Lift-off process of monocrystalline Ge membranes and substrate reuse; (Oral presentation), European Material Research Society, Fall meeting, Warszawa, Poland
3) **Tadeáš Hanuš**, Bouraoui Ilahi, Philippe-Olivier Provost, Javier Arias-Zapata, Alexandre Chapotot, Hubert Pelletier, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif; (2023, August 21-25) Formation of Ge freestanding membranes and substrate reuse by homoepitaxial growth on porous Ge substrate (Oral presentation); The 20th Canadian Semiconductor Science and Technology Conference, Montreal, Canada
4) **Tadeáš Hanuš**, Bouraoui Ilahi, Philippe-Olivier Provost, Javier Arias-Zapata, Alexandre Chapotot, Hubert Pelletier, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif; (Poster presentation) La fabrication des membranes de germanium ultraminces et la réutilisation du substrat (2023, June 7) 3IT Nano Symposium, 2023, Jouvence, Canada
5) **Tadeáš Hanuš**, Bouraoui Ilahi, Philippe-Olivier Provost, Javier Arias-Zapata, Alexandre Chapotot, Hubert Pelletier, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif; (Poster presentation) La croissance des membranes autoportantes de germanium sur des substrats poreux (2023, June 9) Grande Conférence du Regroupement Québécois sur les Matériaux de Pointe, Sherbrooke, Canada
6) **Tadeáš Hanuš**, Bouraoui Ilahi, Alexandre Chapotot, Ahmed Ayari, Hubert Pelletier, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif (2023, May 29 to June 2), Growth of transferable germanium membranes on porous substrate for flexible optoelectronics (Oral presentation), European Material Research Society, Spring meeting, Strasbourg, France

7) **Tadeáš Hanuš**, Bouraoui Ilahi, Javier Arias-Zapata, Philippe-Olivier Provost, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif (2023, May 29 to June 2), Wafer-scale tunable porous Ge: Emerging engineered substrate for epitaxial growth of freestanding membranes (Oral presentation), European Material Research Society, Spring meeting, Strasbourg, France
8) **Tadeáš Hanuš**, Bouraoui Ilahi, Alexandre Chapotot, Ahmed Ayari, Hubert Pelletier, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif (2023, 22-25 May), Unraveling the growth stages on porous substrate and formation of thin detachable Ge membranes (Oral presentation), International Conference on Silicon epitaxy and Heterostructures – International SiGe technology and Device Meeting, Como, Italy
9) **Tadeáš Hanuš**, Bouraoui Ilahi, Javier Arias−Zapata, Alexandre Chapotot, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif (2022, 2 December). Fabrication of wafer-scale freestanding monocrystalline Ge membranes (poster presentation), the 6th Montreal Photonics Networking Event, Montreal, Canada
10) **Tadeáš Hanuš**, Thierno Mamoudou Diallo, Andreas Ruediger, Gilles Patriarche, Simon Fafard, Richard Arès, Abderraouf Boucherif (2022, 19-23 September). Unfolding the role of defect engineering in graphene during Van der Waals epitaxy of semiconductors (oral presentation), European Material Research Society, Fall meeting, Warszawa, Poland
11) **Tadeáš Hanuš**, Bouraoui Ilahi, Javier Arias−Zapata, Alexandre Chapotot, Jinyoun Cho, Kristof Dessein, Abderraouf Boucherif (2022, 19-23 September). Fabrication of wafer-scale freestanding monocrystalline Ge membranes (poster presentation), European Material Research Society, Fall meeting, Warszawa, Poland
12) **Tadeáš Hanuš**, Thierno Mamoudou Diallo, Andreas Ruediger, Gilles Patriarche, Simon Fafard, Richard Arès, Abderraouf Boucherif (2022, 10-16 September), Unraveling the influence of plasma induced defects in graphene on the Van der Waals epitaxy of semiconductors (oral presentation). 19th Conference on Gettering and Defect Engineering in Semiconductor Technology, Mondsee, Austria
13) **Tadeáš Hanuš**, Thierno Mamoudou Diallo, Andreas Ruediger, Gilles Patriarche, Simon Fafard, Richard Arès, Abderraouf Boucherif (2022, 4-9 September). Unraveling the influence of plasma induced defects in graphene on the Van der Waals epitaxy of semiconductors (oral presentation). International Conference on Molecular Beam Epitaxy, Sheffield, United Kingdom
14) **Tadeáš Hanuš**, Javier Arias-Zapata, Bouraoui Ilahi, Philippe-Olivier Provost, Alexandre Chapotot, Abderraouf Boucherif (2022, 18-20 July). Fabrication of ultrathin Ge template

for growth of high-performance III–V optoelectronic devices based on wafer-scale porous Ge (poster presentation), TOP-SET 2022 Summer School, Ottawa, Canada

15) **Tadeáš Hanuš**, Bouraoui Ilahi, Javier Arias-Zapata, Philippe-Olivier Provost, Alexandre Chapotot, Abderraouf Boucherif (2022, 6-8 July). Towards wafer-scale freestanding monocrystalline Ge membranes based on porous Ge substrate (poster presentation), Workshop on Advanced Epitaxy for Freestanding Membranes and 2D Materials, Cambridge, MA, USA, Massachusetts Institute of Technology (MIT)
16) **Tadeáš Hanuš**, Javier Arias-Zapata, Bouraoui Ilahi, Philippe-Olivier Provost, Alexandre Chapotot, Abderraouf Boucherif (2022, 5-10 June). Fabrication of ultrathin Ge template for growth of multijunction solar cells based on wafer-scale porous Ge (poster presentation), 49th IEEE Photovoltaic Specialists Conference, Philadelphia, PA, USA
17) **Tadeáš Hanuš**, Thierno Mamoudou Diallo, Abderraouf Boucherif (2022, 25-28 February), Graphene engineering by plasma enables the growth of single crystalline semiconductors (oral presentation), QCAM - 6th annual meeting 2022, Virtual Symposium.

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