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# Characterisation of 3.3kV IGCTs for Medium Power Applications

Silverio Alvarez E Hidalgo

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# THESE

Présentée  
pour obtenir le titre de

DOCTEUR DE L'INSTITUT NATIONAL POLYTECHNIQUE DE TOULOUSE  
Spécialité : Génie Electrique

Par

## Silverio ALVAREZ HIDALGO

Ingénieur ENSEEIHT – DEA Génie électrique

# Characterisation of 3.3kV IGCTs for Medium Power Applications

Soutenue le 3 novembre 2005 devant le jury composé de:

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# Abstract

The Low Voltage IGCT (3.3kV) is developed to provide a semiconductor able to work at high switching frequencies (>1kHz), preserving its "high current" capacity (4kA). The ultimate goal is to increase the dynamic performances of medium/high power converters, thus extending their application field.

To characterise the experimental samples of 3.3kV IGCTs, an opposition method based test bench was developed. This method allows the components to be evaluated at different test conditions in real operation without the need of several megawatt power supplies.

Once the samples were characterised, the applicability analysis of these components on specific applications related to the French railway network (SNCF) is performed.

Finally, a reactive power compensation application for single-phase systems is studied in detail and a 100kVAR IGCT based set up is built.

## *Keywords*

- 
- |                     |                  |                |
|---------------------|------------------|----------------|
| • 3.3 kV IGCT       | • Medium Voltage | • Medium Power |
| • Opposition Method | • STATCOM        | • AC Chopper   |
- 

# Résumé

Le développement des IGCT Basse Tension (3,3kV) vise un composant capable de travailler à fréquence élevée (>1 kHz) tout en gardant sa capacité "fort courant" (4kA). L'objectif final est d'augmenter les performances dynamiques des convertisseurs moyenne/forte puissance et d'étendre ainsi leur champ d'application.

Pour la caractérisation des échantillons expérimentaux des IGCT 3,3kV, un banc d'essais basé sur une méthode d'opposition a été développé. Cette méthode permet l'évaluation des composants sous différentes conditions d'essai en mode de fonctionnement réel sans nécessité de sources d'alimentation de plusieurs MW.

Une fois les échantillons caractérisés, l'analyse de l'applicabilité de ces composants dans des applications spécifiques aux réseaux ferroviaires SNCF est abordée.

Finalement, une application de compensation de puissance réactive pour des réseaux monophasés a été étudiée en détail et une maquette de 100kVAR à base de IGCTs a été réalisée.

## *Mots Clefs*

- 
- |                        |                         |                     |
|------------------------|-------------------------|---------------------|
| • IGCT 3.3kV           | • Moyenne Tension       | • Moyenne Puissance |
| • Méthode d'opposition | • Compensateur Statique | • Gradateur MLI     |
-

# Resumen

Los IGCT de Baja Tensión (3.3kV) se desarrollan para proporcionar un componente capaz de trabajar a frecuencia elevada (>1kHz) manteniendo su capacidad de "alta corriente" (4kA). El objetivo final es aumentar las prestaciones dinámicas de los convertidores de media/alta potencia y ampliar así su campo de aplicación.

Para caracterizar la muestras experimentales de IGCTs 3.3kV, se ha desarrollado un banco de ensayo basado en el método de oposición. Este método permite evaluar los componentes bajo diferentes condiciones de ensayo en modo de funcionamiento real sin necesidad de fuentes de alimentación de varios megavatios.

Una vez que las muestras han sido caracterizadas, se aborda el análisis de la aplicabilidad de estos componentes en aplicaciones específicas relacionadas con la red ferroviaria Francesa (SNCF).

Finalmente, se estudia en detalle una aplicación de compensación de potencia reactiva para redes monofásicas y se realiza una maqueta de 100kVAR con IGCTs.

## *Palabras Clave*

- 
- |                       |                 |                  |
|-----------------------|-----------------|------------------|
| • IGCT 3.3 kV         | • Media Tensión | • Media Potencia |
| • Método de oposición | • STATCOM       | • Chopper AC     |
-

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Con todo mi amor.*



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# Introduction

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At the end of the 90s, the evolution of the high power semiconductor properties, particularly the increase of the power semiconductors current and voltage ratings, stimulated the growth of the Medium Voltage/ Medium Power converters market ranging from several hundred kW to several MW in the kV voltage range. This evolution mainly influenced the field of industrial and traction applications but also had significant impact on electric energy generation, distribution and transmission applications. Nowadays, a wide range of applications apply medium and also high power electronic systems combining the latest developments on medium voltage semiconductors with advanced conversion topologies and control systems. For the applications where fully controlled semiconductors are required, mainly IGBTs and IGCTs are seriously considered. The IGBT, isolated gate bipolar transistor, is the favoured semiconductor for low and medium power applications, while the application field of IGCTs, turn-off thyristor type semiconductors, concerns mainly the medium and high power range (several tens MW).

In contrast to the actual trend of increasing the semiconductor blocking voltage (>6.5kV) to enlarge the converter power capacity, this work deals with the use of the experimental 3.3kV IGCTs developed by ABB Semiconductors. Although the 3.3kV market is already well covered by the commercially available IGBTs, the aim of the 3.3kV IGCT development is to provide a semiconductor able to work at high switching frequencies (>1kHz), preserving its "high current" capacity (>1kA). The ultimate goal is to increase the dynamic performances of the medium and high power converters, which consequently allows extending their application field (active filtering, sag compensation, reactive power compensation, etc.). This is possible starting from the standard asymmetric IGCT (4.5kV) structure, where the wafer thickness is decreased as well as its blocking voltage rating, leading to the significant reduction of the semiconductor on-state voltage and switching losses.

The main goals of the work presented in this dissertation concern the characterisation of the experimental 3.3kV IGCTs and the identification of the power electronic topologies and applications where the characteristics of these semiconductors can be efficiently exploited. The dissertation is organised in five chapters.

The first chapter provides an overview of the main medium voltage / high power semiconductors. Special attention is given to the operation principles, the implementation requirements and the future trends of IGCTs. Also a general comparison between the characteristics of the IGCTs and IGBTs is presented to show the differences between both technologies.

In the second chapter, the characterisation of the experimental samples of 3.3kV IGCTs and their associated freewheeling diodes is discussed. An opposition method based test bench is selected to evaluate the semiconductors in real operation under different test conditions, (DC bus (500V - 1.5kV), switched output DC current (0 - 2kA) and switching frequency (500Hz - 2kHz) at constant duty cycle,  $\alpha \approx 0.5$ ), without the need of several megawatt power supplies and loads. The test bench is mainly used to identify the semiconductors on-state and switching losses, but also other interesting parameters are measured, especially the gate unit power requirements and the clamp circuit power losses. A brief comparison between the obtained characterisation results with

the characteristics of the ABB commercially available 3.3kV IGBTs allows emphasising the properties offered by the experimental 3.3kV IGCTs.

With the characterisation results presented in the second chapter, the use of the 3.3 kV IGCTs in different applications and topologies is analysed in the third chapter. The semiconductor power losses calculation is used as the comparison element between the different conversion structures considered for each application. To perform these comparisons, a universal power losses evaluation tool for the semiconductors of a switching cell is developed and applied. The analysis is mainly focused on two applications related to the French railway network (SNCF), the active filtering for 1.5kV DC substations and the reactive power compensation for 25kV/50Hz single-phase substations.

The content of the fourth chapter is focused on a 3MVAR single-phase STATCOM based on step-down PWM AC Choppers equipped with 3.3kV IGCTs. First, the PWM AC Chopper topologies are briefly introduced. Then, a detailed design of the components, control strategy and switching pattern generation for a basic 1MVAR STATCOM module is treated.

Finally, in the fifth chapter, the experimental evaluation of the concepts developed in the fourth chapter is presented. Two set-ups are employed to demonstrate the feasibility of the solutions proposed to obtain stable and safe operation of the system. The low voltage/low power IGBT based set-up is used to validate the adopted switching pattern and control strategies, while the medium voltage 100kVAR IGCT based set-up is built to validate the use of the developed concepts when IGCTs are employed.

# Chapter 1

---

## IGCT, the Medium Voltage High Power Semiconductor

### 1.1 Introduction

From the very beginning, the development of power semiconductors has been looking for the ideal switch. Still these days, and thanks to the increasing demand of power electronics systems for different applications (industry and traction, generation, transmission and distribution, space, medicine, etc.), the search for the ideal switch goes on and will continue in the future. Different technologies and smart solutions in several disciplines (i.e. silicon technology, metallurgy and ceramics, electrical and mechanical engineering) have been applied to improve the characteristics of the semiconductors. The research and development efforts have been focused to minimise the on-state and switching losses, enlarge the semiconductors SOA (in both directions, current and voltage), operate at the highest possible switching frequency, use of simple and efficient driver circuits, increase the power dissipation capability, reliability and ruggedness of the components, etc. As silicon is reaching its physical limits, new materials as Silicon Carbide and diamond are being considered in order to realise the ideal switch.

In this chapter, first a brief summary of the basics of the main high power semiconductors is presented. Then, special attention is paid to the main topics referred to IGCTs, from basics of operation to future trends, including set up considerations in power electronics systems.

### 1.2 Medium Voltage High Power Semiconductors Overview

From the oldest semiconductor device, the p-n junction diode used since the 1940s, different power semiconductors have been used such as bipolar transistors, MOSFETs, Thyristors, GTOs, IGBTs, IGCTs, etc., most of them are silicon based devices, [KWO-95]. The first controllable high power semiconductor was the thyristor, which was first used in the 1960s for traction applications by means of line-commutated control [CAR-98] and for transmission applications with the first semiconductor based HVDC in 1970 [DAN-01]. Then, in the 1970s, fast thyristors and diodes allowed to expand the field of industrial and traction applications by means of self-commutated converters (choppers and inverters). During the 1980s the use of full-controlled semiconductors such as bipolar power transistors (Darlington), GTOs (Gate Turn-Off Thyristor and IGBTs (Insulated Gate Bipolar Transistor) enabled the rapid expansion of industrial motor drives. The transistor-based structures pushed the thyristor-based structures towards higher powers, and by the early 1990s GTOs had become very high power devices whereas the IGBTs and MOSFETs with their simple drive requirements (voltage control) were the main components of choice for low-voltage applications.

In the late 1990s, the emergence of the IGCT (Integrated Gate-Commutated Thyristor), [KLA-97], and the High Voltage-IGBT (HV-IGBT), [TAN-97], had given new impetus to the Medium Voltage - High Power semiconductor market. Nowadays, for high power applications, only these devices together with thyristors are under serious consideration for the present and the foreseeable future, since the GTO is destined to be replaced by the IGCT [CAR-98]. The IGBT seems to be the right component for low – medium power applications (from 100kW to 2-3 MW), whereas for medium – high power applications (1MW – 100MW) the IGCT seems to be the better option. However, the use of 6.5 kV IGBTs [GOT-99] and new developments using press pack IGBTs [DAN-01][BEG-03] and increasing the blocking voltage (8kV) [RAH-03], try to extend the IGBT power range. At the same time, new IGCT developments (10kV High Voltage [BER-03] and 3.3kV Low Voltage [ALV-04b]) try to expand their range of applications. Nowadays, 6.5kV/600A, 4.5kV/900A, 3.3kV/1.2kA are commercially available ratings for IGBTs, and 4.5kV/4kA and 6kV/3kA for IGCTs.

Prosperity of high power electronics systems in many application fields has been possible thanks to the development of all these high power semiconductors, although many other device structures have been investigated and discussed, Table 1-1. These devices can be divided in two families; Transistors and Thyristors, depending on the way they react to the control signal. Transistors act as “amplifiers” than can control the collector current and the switching speed by means of the control terminal voltage or current. Thyristors, however, behave as “binary current valves” where the gate signal has little, if any, influence to the collector current and on / off switching speed (mainly defined by external circuits).

THYRISTOR based semiconductors	TRANSISTOR based semiconductors
GTO (Gate Turn-Off Thyristor)	Bipolar Transistor (Darlington)
MCT (MOS-Controlled Thyristor)	MOSFET Transistor
FCTh (Field-Controlled Thyristor)	FCT (Field Controlled Transistor)
SITh (Static Induction Thyristor)	SIT (Static Induction Transistor)
MTO (MOS Turn-Off Thyristor)	<i>IGT</i> (Injection Enhanced Gate Transistor)
EST (Emitter-Switched Thyristor)	<b>IGBT</b> (Insulated Gate Bipolar Transistor)
ETO (Emitter Turn-Off thyristor)	
IGTT (Insulated Gate Turn-off Thyristor)	
IGT (Insulated Gate Thyristor)	
<b>IGCT</b> (Integrated Gate-Commutated Thyristor)	

Table 1-1.- Fully controlled semiconductor devices classification

Thyristors, GTOs, IGCTs and HV-IGBTs have already demonstrated their entire applicability in high power real systems. Of course, the fast recovery Diode must not be forgotten since it plays an important role in the transient behaviour of the other controlled semiconductors. The well known Thyristor, also called SCR (Silicon Controlled Rectifier) or PCT (Phase Controlled Thyristors) to be distinguished from Fast Thyristors, can only be turn on controlled which limits its use mainly to line-commutated frequency conversion. For other kinds of conversions, high frequency PWM is mainly used, which requires full-controlled semiconductors (turn-on and turn-off), also known as self-commutated devices. GTOs, IGCTs and HV-IGBTs are the preferred full-controlled devices.



## 1.2.1 Thyristors

A Thyristor is a 3 segment device (reversible voltage, unidirectional current) with a four-layer P<sup>+</sup>N<sup>-</sup>PN<sup>+</sup> structure, where the outermost N<sup>+</sup> and P<sup>+</sup> layers are electrically accessible by the terminals called Cathode and Anode respectively. Contact to the P base layer, the control terminal, is called Gate, Figure 1-1, [TEC-a], [KWO-95], [ABB-a]. In the forward direction (anode voltage positive with respect to cathode  $V_{AK}$ ) two distinct states exist, a low current - high voltage off state and a high current - low voltage on state. A positive gate current can trigger the change from the forward blocking state to the forward conducting state. However, a negative gate current is not effective to turn off the thyristor. In the reverse direction, only the off state is available.

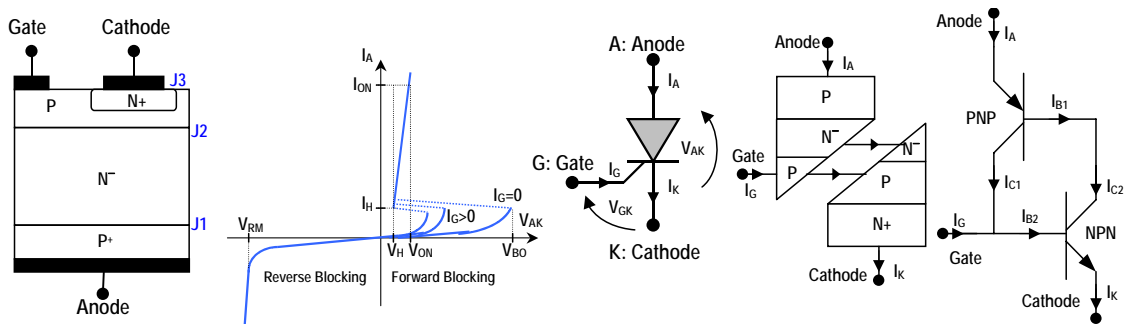


Figure 1-1.- Thyristor structure, static characteristic, symbol and two-transistor representation

- **Reverse blocking state:** In the reverse blocking mode ( $V_{AK} < 0$ ), junctions J1 and J3 are reverse biased, but most of the voltage drop is supported by the N<sup>-</sup> region. The breakdown voltage  $V_{RM}$  in this mode is mainly due to avalanche breakdown of J1.
- **Forward blocking state:** In the forward blocking mode ( $V_{AK} > 0$ ), only the junction J2 is reverse biased. There is a break-over voltage for  $V_{AK}$  above which the thyristor is automatically switched to the on state. This break-over voltage  $V_{BO}$  is a function of the gate current. With high gate current into the device  $V_{BO}$  is very low and the forward characteristics resemble to a PN junction characteristic. The  $V_{BO}$  level at zero gate current is usually very close to the reverse breakdown voltage  $V_{RM}$ .
- **Turn on:** The turn on mechanism of the thyristor can be easily explained with its four-layer structure divided in to a PNP and a NPN bipolar transistor with each base connected to the other's collector as depicted in Figure 1-1. Qualitatively, an initial small base current  $I_{B2}$  injected through the gate terminal produces a larger collector current  $I_{C2}$  which triggers the Thyristor. This  $I_{C2}$  is the base current for the PNP transistor,  $I_{B1}$ , and it is further amplified to give a still larger collector current  $I_{C1}$ . This  $I_{C1}$  adds to  $I_G$  and becomes the original base current  $I_{B2}$ . This effect represents a regenerative feedback that gives rise to switching on the thyristor (Eq. 1-1 to Eq. 1-4), it is said to be in the forward conducting state. Once the device has been latched on in this manner, external gate current is no longer required to maintain conduction, since the regeneration process is self-sustaining. The on state voltage  $V_{ON}$  is then the sum of one forward junction bias plus the  $V_{CE}$  saturation voltage of a bipolar transistor.

The required gate current level for switching on the thyristor is defined by the common base gain of the PNP and NPN transistors ( $\alpha_{PNP}$  and  $\alpha_{NPN}$ ) and the leakage currents due to the reverse-biased collector-base junctions of two transistors ( $I_{CB01}$  and  $I_{CB02}$ ). The main function of  $I_G$  for triggering is not to increase the numerator of Eq. 1-4 but to increase ( $\alpha_{PNP} + \alpha_{NPN}$ ) to meet the ignition condition ( $\alpha_{PNP} + \alpha_{NPN} = 1$ ).

$$I_{C2} = \alpha_{NPN} \cdot I_K + I_{CBO2} \quad \text{Eq. 1-1}$$

$$I_{B1} = (1 - \alpha_{PNP}) \cdot I_A - I_{CBO1} \quad \text{Eq. 1-2}$$

$$I_K = I_A + I_G \quad \text{Eq. 1-3}$$

$$I_A \approx \frac{I_G \cdot \alpha_{NPN} + (I_{CBO1} + I_{CBO2})}{1 - (\alpha_{NPN} + \alpha_{PNP})} \quad \text{Eq. 1-4}$$

The ignition of the thyristor can be also triggered by means of other mechanisms than the injection of a gate current. In fact, every injection mechanism of hole current enough to bias the gate – cathode junction above its threshold voltage limit  $V_{GT}$  is an ignition factor. For instance, the avalanche multiplication in the J2 junction due to high forward blocking voltage (voltage break-over), thermally derived J2 reverse current generation due to high junction temperature or even displacement current due to high  $V_{AK}$   $dV/dt$  are well known phenomena that can trigger the thyristor. To decrease the thyristors sensitivity to this non-desired ignition modes, small regions of  $N^+$  are left out in the cathode emitter layer and the corresponding P-type doping can reach the cathode metallised surface. These regions form an ohmic short-circuit across the P base-emitter junction (cathode shorts) and conduct a significant portion of the current at low current densities. This shunt resistance reduces the injection efficiency of the NPN transistor at low  $I_G$  levels, decreases its common base gain ( $\alpha_{NPN}$ ) and increases the value of the break-over voltage ( $V_{BO}$ ).

- **Blocking:** The transistor gain values in Thyristors make it impossible to turn off the device by extracting current through the gate. This is only possible with GTOs and IGCTs. The classical way to turn off a thyristor is by instantaneously decreasing the anode current. This inversion can be natural or externally generated by an auxiliary circuit. The polarity inversion has to be kept for a long enough time ( $t_Q$  turn off time) to allow the recombination of the base junctions stocked charges and to guarantee the return to the blocking state before a forward voltage is re-applied.

During the turn off sequence, it is very important that the voltage between anode and cathode remains inside the acceptable voltage limits. Normally, parallel RC snubbers have to be used to keep the blocking over-voltage under reasonable limits, Figure 3. This RC snubber also limits the  $dV/dt$  across the device.

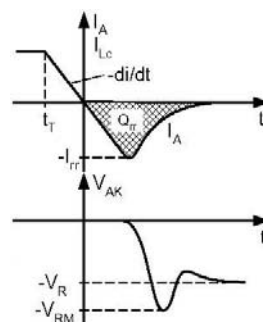


Figure 1-2.- Typical thyristor blocking waveforms

Different thyristor packages are commercially available (modules – discrete dies and press-packs – monolithic wafer, Figure 1-3), however, for high power application the press-pack package is preferred for its high power density and thermal capability (both sides cooling). In the press-pack package the so-called free-floating technology is generally applied, where a specific compression

force over the component is required to obtain good electrical contact between the external terminals (anode and cathode) and the silicon wafer.



Figure 1-3.-Thyristor packages, modules and press-pack

Recent developments in the field of high power thyristors have lead to new thyristor versions with specific functionalities adapted to specific applications (HVDC, SVC, etc) like the LTT (Light Triggered Thyristor, Eupec) or the BCT (Bi-directional Controlled Thyristor, ABB).

## 1.2.2 Gate Turn Off Thyristors (GTO)

As a member of the thyristor family, the Gate Turn Off thyristor (GTO) has also a four layer three junction regenerative ( $P^+N^-PN^+$ ) structure, Figure 1-1, therefore the ignition operation principle is the same as for thyristors [KWO-95], [ABB-b], [GRU-96a]. GTOs differ from conventional thyristors, in that they are designed to turn-off when a negative voltage is applied to the gate electrode, thereby causing a negative gate current. To achieve this goal, a more efficient gate-controlled turn-off is required, thus  $I_{B2}$  and  $I_{C1}$  have to be minimised during the on state. This demands higher gain for the NPN transistor and lower gain for the PNP transistor ( $\alpha_{NPN} \gg \alpha_{PNP}$ ), which normally is obtained by means of anode shorts, Figure 1-4. As result, a relatively high gate current is needed to turn off the device with typical turn-off gains (ratio of the anode current to the peak negative gate current) being in the range of 3 to 5, which implies several hundred amps to be extracted through the gate.

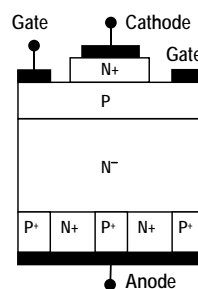


Figure 1-4.- Classic anode shorted GTO cross section

Another big difference with respect to Thyristors is the necessity of a highly interdigitated gate-cathode junction to optimise the current turn-off capability. In fact, the GTO has a thyristor structure with a finely divided cathode such that it may be considered as a large number of small thyristors on a common silicon substrate, having common anodes and gates but individual cathodes. The most popular design features multiple segments arranged in concentric rings around the device centre, Figure 1-5. This interdigitation contributes to the homogeneous blocking of the gate – cathode junction, which finally avoids uneven current distribution over the silicon wafer and hence local heating. The same consideration acts for the turn on process where a high amplitude and rise time of the gate trigger current also helps obtaining homogeneous switching transition.



Figure 1-5.- Interdigitated cathode example of a GTO thyristor

All the actions taken to obtain a controlled turn off have an adverse effect on the device's turn-on and conduction performance. Consequently, the resultant device is necessarily a compromise of turn-on, conduction and turn-off performance. This trade off requires the use of bulky RCD snubbers to limit the device  $dV/dt$  at turn off (typically  $1000 \text{ V}/\mu\text{s}$ ). In fact, the maximum turn-off current of a GTO depends on the snubber capacitance chosen, and on the stray inductance in the snubber network. Also,  $dI/dt$  limitation at turn on is required to avoid excessive recovery current on the associated free wheeling fast recovery diode (around  $500\text{A}/\mu\text{s}$ ). Figure 1-6 shows the typical GTO waveforms at turn on and off and the classical Undeland snubber circuit for GTO phase legs.

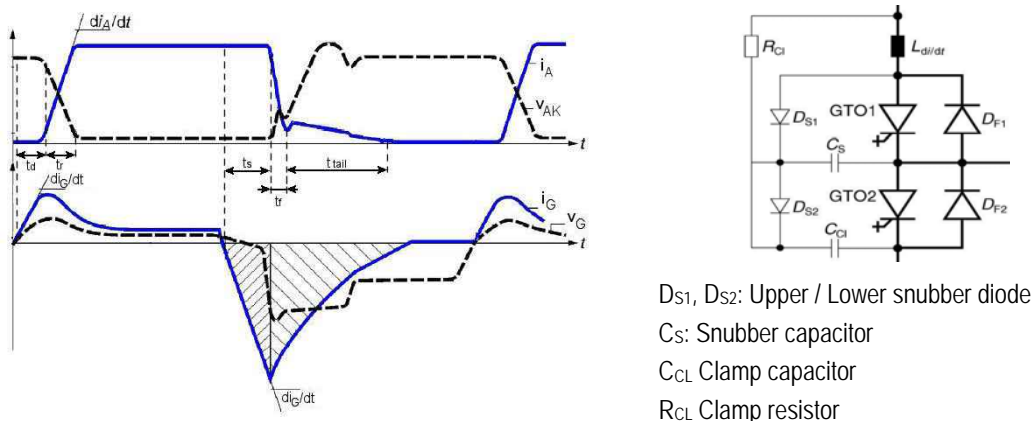


Figure 1-6.- GTO characteristic waveforms and classical Undeland snubber for a GTO phase leg

The switching frequency of GTOs is typically limited to a maximum value of about 300 Hz due to device and snubber losses. In general, the turn-on transient process of a GTO is almost identical with the one known from conventional thyristors; however, the main switching time constraints of GTOs appear especially at turn off. Large storage times,  $t_s$ , are required (typically around  $25\mu\text{s}$ ) to make the anode current start to fall after the gate current become negative. Then, after the fall time  $t_F$ , although the cathode current has ceased (NPN transistor blocked), anode to gate current continues to flow. This so-called "tail current" flows while the anode voltage is already high, which generates quite substantial power losses. The device regains its steady state blocking characteristics only when the tail current has completely disappeared.

The device current distribution during the switching transients can be in-homogeneous, which could lead to hot spots on the semiconductor and consequently a thermal avalanche. To avoid this phenomenon and to allow uniform junction temperature, minimum on-time ( $t_{ON\_MIN}$ ) an off-time ( $t_{OFF\_MIN}$ ) must be guaranteed (typically around  $100\mu\text{s}$ ).

Regardless of its limitations and costs, the GTO technology has found interesting applications and several different varieties of GTO are currently manufactured, all of them only available in press-pack packages. Devices with reverse blocking capability equal to their forward voltage ratings are the so-called symmetric GTOs. However, most products on the market today feature

an anode junction incapable of blocking reverse voltage, which are called asymmetric GTOs. Reverse conducting types constitute the third family of GTOs, where a GTO is integrated together with an antiparallel freewheeling diode onto the same silicon wafer.

### 1.2.3 Integrated Gate Commutated Thyristors (IGCT)

Many of the problems associated with the GTO turn off switching performances can be solved by using the Hard Driving principle, Figure 1-7, [ABB-b], [BER-96]. This principle relies on the application of a high gate current  $di_G/dt$ , enough to allow direct commutation of the total cathode current to the gate before a change in gate to anode voltage occurs. In this way, the NPN transistor of the four-layer thyristor structure is inactive, Figure 1-1, and the component turns off as a three-layer component (transistor mode turn off). Consequently, the device switching becomes homogeneous, eliminating the current filamentation problems inherent in conventional GTOs. The maximum turn off current will depend exclusively on the SOA capability of the device [STI-04] and not on external circuit elements (snubber capacitor value, stray inductances, etc.). Furthermore, the storage time  $t_s$  and fall time  $t_f$  are decreased remarkably, which leads to high reduction of the switching losses and simplification of the devices series connection.

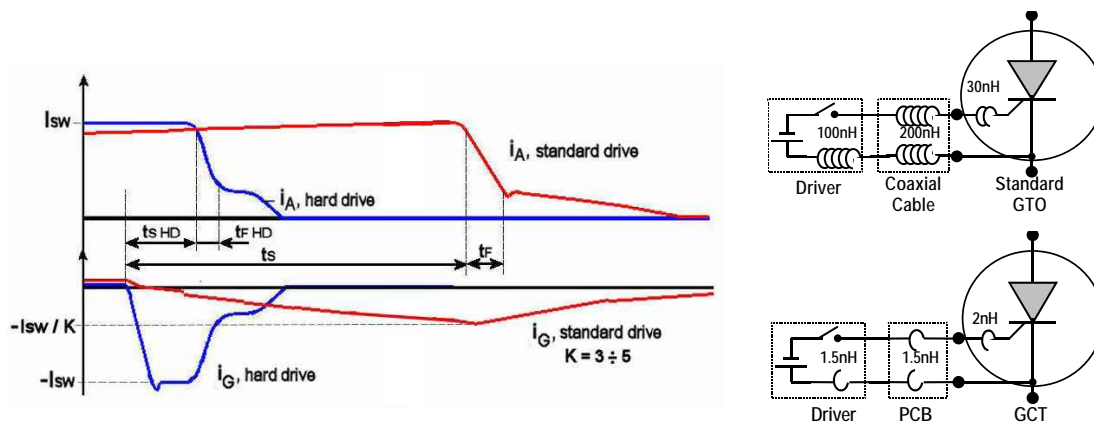


Figure 1-7.- GTO turn-off with hard and standard gate drive

Fast commutation of total GTO cathode current ( $di_G/dt > 3kA/\mu s$ ) depends basically on the gate parasitic inductance and voltage value. Using standard GTO housing, where the total gate inductance can be minimised to around 50nH acting over the gate driver and its cabling, gate voltages values of 200V are required. However, the use of such a gate voltage value can complicate the gate isolation and increase the gate driver power supply requirements.

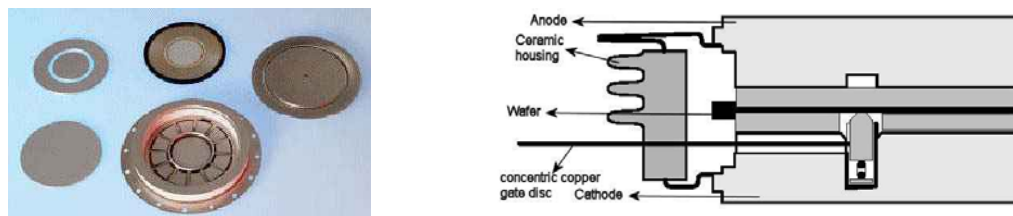


Figure 1-8.-IGCT low inductance gate contact

To avoid these problems, the most convenient voltage to use is 20V because the gate can withstand this voltage after turn-off. This means that the total gate inductance should be less than 5nH. To reach these figures, the following considerations were made. Firstly, the development of a coaxial GTO was considered and the GCT (Gate Controlled Thyristor) concept appeared,

Figure 1-8, which led to the minimisation of the inherent gate inductance of the component (around 2nH). Then, the interconnection of the gate driver with the GCT was optimised by using a printed circuit board coaxial configuration, leading to the so-called IGCT (Integrated Gate Controlled Thyristor).

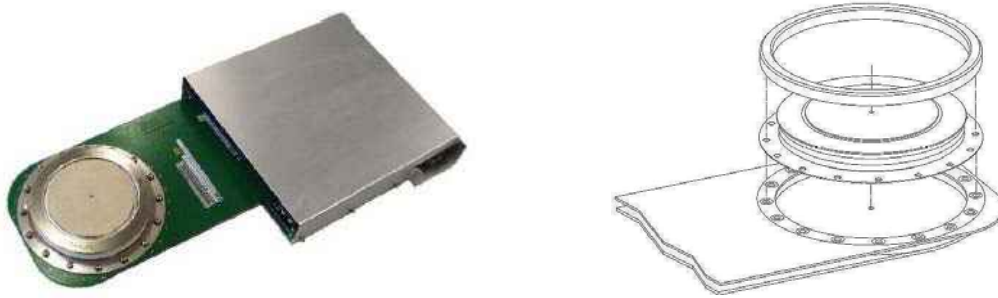


Figure 1-9.- IGCT, GCT low inductive connection to the driver by means of printed circuit boards

Such a development allows for have homogeneous current throughout the switching transitions but also avoids the need of snubber capacitors to limit the  $dV/dt$ , that is, the IGCTs can work in snubberless operation. Furthermore, due to the very low storage and fall times, the minimum on and off time can be reduced below  $10\mu\text{s}$  (compared to  $100\mu\text{s}$  for GTOs).

The turn-on characteristic by hard positive gate drive of the device is also improved and only the IGCT associated freewheeling diode is subject to turn-on  $di/dt$  limitations. Due to its thyristor nature, the GCT cannot provide such a  $di/dt$  control. Instead,  $di/dt$  control must be provided by means of an external inductor, which also requires a small low inductance clamp circuit (RCD circuit) for over-voltage limitation at IGCTs turn-off. Figure 1-10 shows the characteristic switching waveforms of an IGCT and the clamp circuit required to limit  $di/dt$  at turn-on (diode turn-off  $di/dt$  limitation) and over-voltage at turn off.

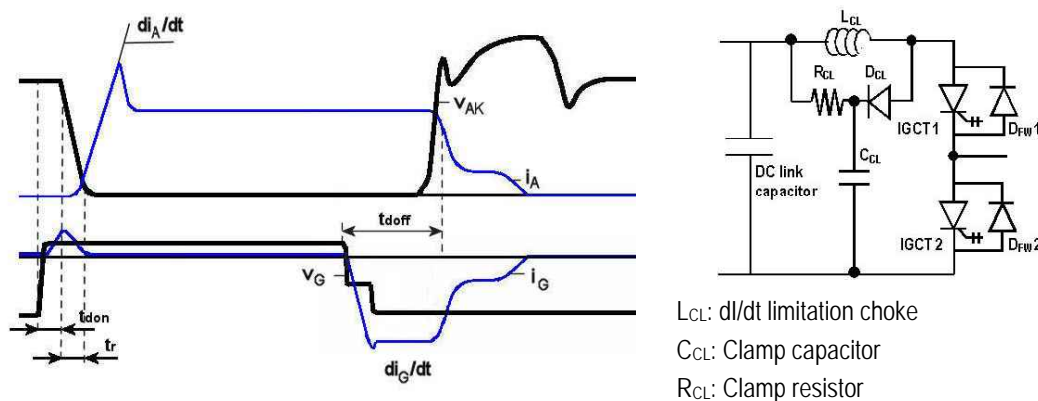


Figure 1-10.- IGCT characteristic waveforms and clamp circuit for free-wheeling diode  $di/dt$  turn-off limitation

Hard gate drive now allowed for significant wafer optimisation [GRU-96b]. Anode shorts were no longer needed and the thickness of the device could be reduced by 30% compared to GTOs with even higher capability to withstand cosmic radiation, thanks to the buffer layer combined with a transparent anode design. This technique allows also the reduction of on-state losses, switching off losses and on-state gate current, as well as the integration of an inverse diode in the same wafer without device performances deterioration. This helps to reduce the total inverter cost in many applications. Also, charge carrier lifetime tailoring (through electron and particle irradiation),

can be applied to obtain device trade-offs (turn off switching losses  $E_{OFF}$  versus on-state voltage drop  $V_T$ ) required for different applications, [STI-01]. Three main families can be distinguished:

- Low on-state losses (e.g. for DC or AC Solid State Breakers)
- Low switching losses for high frequency switching applications (e.g. for Medium Voltage Drives -MVD).
- Wide temperature range and low total losses (e.g. for Traction applications).

Considering the different GTO versions, symmetric, asymmetric and reverse conducting IGCTs are manufactured and commercially available.

With its proven high reliability, the IGCT is considered an optimal cost-efficient choice in many high power applications requiring turn-off devices and is currently used in large motor drive systems, traction power-supply and distribution systems, [GRU-97], [STE-97], [STE-00].

## 1.2.4 Insulated Gate Bipolar Transistors (IGBT)

The IGBT structure combines the MOS and bipolar transistor principles, which leads to a high speed, voltage easy controlled (MOS transistors) and low on-state voltage (bipolar transistors) device. Also it inherits some drawbacks from each technology such as its sensitivity to electrostatic charges (MOS) and the tail current at turn off (Bipolar), [SEM-a].

The structural design of the IGBT as well as the power MOSFET, Figure 1-12, consists of a silicon-micro-cellular structure of about 100,000 basic cells per  $\text{cm}^2$  (high-voltage-IGBTs) distributed over a chip surface that can vary between 0.3 and 1.5  $\text{cm}^2$ , Figure 1-11. As the current density is limited, the current capacity of the device can be increased by integration of several dies in a potential free power module (isolation of the base plate). Paralleling connection of chips is done by ultrasonic soldering of aluminium wire bonds to the chips metallisation. Dies are soldered on a Direct Copper Bonding (DCB) substrate consisting of a ceramic layer ( $\text{Al}_2\text{O}_3$  or  $\text{AlN}$ ) and two copper layers which are soldered on a copper or  $\text{AlSiC}$  base plate, [COQ-99a]. In addition to several transistor chips, these modules can contain adapted freewheeling diode chips and even passive components and other "intelligent" elements providing integrated functions such as temperature measurement, gate driving, protection, etc. In that way, the arrangement of devices on a module is very flexible and almost any desired structure can be built. However, in power modules only one-side cooling can be applied.

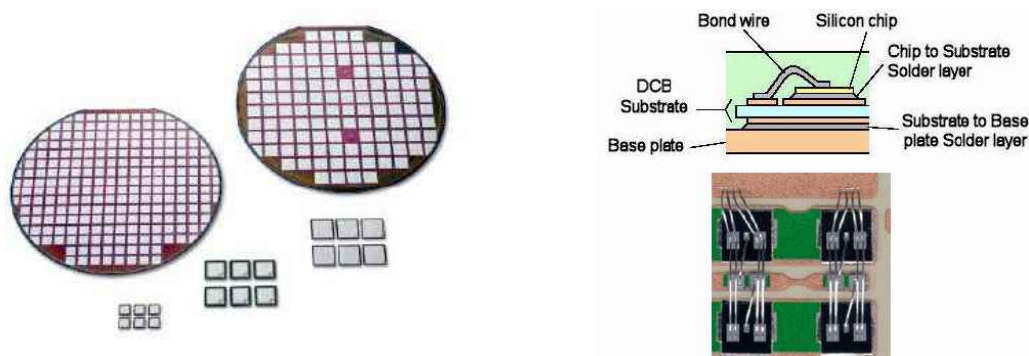


Figure 1-11.- IGBT and Diodes silicon chips. Integration of several dies on an isolated module

In a MOSFET, when a sufficient positive control voltage is applied between the gate and source, an inversion layer (N conducting channel) is generated in the  $\text{P}^+$  area below the gate, which represents a conducting channel for electrons, Figure 1-12. The electrons flowing in the electrical voltage field between drain and source ( $V_{DS} > 0$ ) are attracted by the drain connection, thus

absorbing the space charge zone. Consequently, the drain-source voltage will decrease and the main current (drain current) will be able to flow. Since the electrons are conducting current by 100% and are majority charge carriers in the  $N^-$  area, bipolar charge carriers will not flood the highly resistive  $N^-$  zone. Consequently the MOSFET is a unipolar component. In the blocking state the voltage drops in the wide low-doped MOSFET base ( $N^-$  region).

Due to its unipolar behaviour, the MOSFET is predominantly characterised in the on state by the  $N$  region resistance ( $R_{DS\ ON}$ ). For MOSFET voltage ratings above 600V (the  $N$  region thickness is increased), the on-state voltage drop is higher than for bipolar components and the current carrying capacity is lower. On the other hand, there are no storage effects because the majority charge carriers are exclusively responsible for charge transportation which leads to very short switching times, thus the switching frequency can be considerably high.

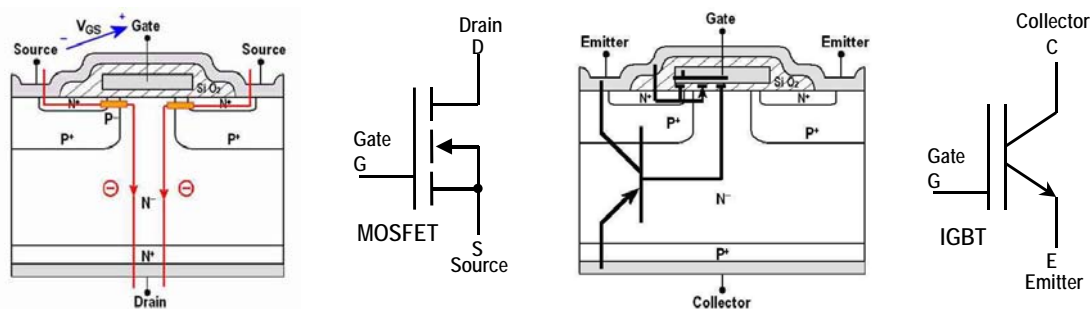


Figure 1-12.- MOSFET and IGBT basic cell structures and symbols.

To avoid the high resistance of MOSFETs for high voltage ratings, IGBTs are equipped with a  $P^+$  conductive area with connection to the collector below the  $N^-$  zone. The bipolar effect of charge transportation by diffusion is used. Compared to the pure ohmic on-state behaviour of the MOSFET, the IGBT has an additional threshold voltage due to the collector PN-junction layer, but the on-state voltage of high-voltage IGBTs (above 600V) is lower than that of MOSFETs because of the enhancement of minority carriers in the highly resistive  $N^-$  zone. Furthermore, IGBTs may be designed for considerably higher voltages and currents for similar chip surfaces. The main drawback compared to MOSFETs is the degradation of the switching transients due to the surplus  $P$  storage charge that has to be recombined in the  $N^-$  zone during turn-off once the collector voltage has increased (tail current).

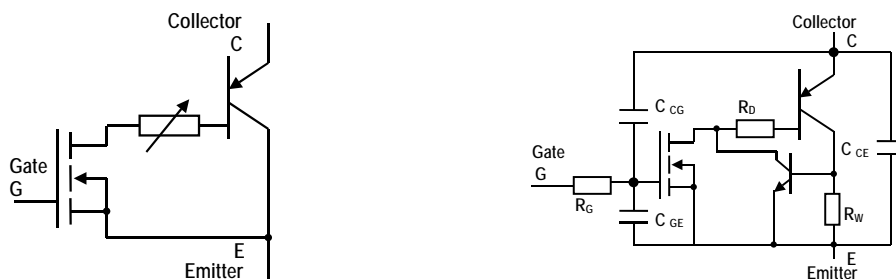


Figure 1-13.- IGBT equivalent circuit (simplified and with parasitic elements).

The basic operation principle of an IGBT can be easily explained by means of the simplified equivalent circuit shown in Figure 1-13. When the MOSFET is activated, a base current for the PNP bipolar transistor can be established and collector to emitter current can flow. A more detailed equivalent circuit (apart from internal capacitances and resistances) reveals the existence of a parasitic NPN transistor, which together with the PNP transistor represents a thyristor equivalent circuit. Latch-up of this parasitic thyristor will lead to a loss of controllability of



the IGBT and, therefore, to its destruction. The parasitic thyristor latch-up may happen during on state (when a critical current density is exceeded, which decreases with rising chip temperature) but it can also appear during turn-off (dynamic latch-up due to the increased hole current compared to on-state operation). In modern IGBTs, depending on the IGBT structure, different design precautions are applied to reliably prevent latch-up.

The static characteristic of an IGBT shows a 3 segment behaviour (current reversible and voltage unidirectional), however, the component forward operation characteristic optimisation results in a useless reverse characteristic, which means that the IGBT has to be considered as a 2 segment device, Figure 1-14. Therefore, if a third segment behaviour is required, combination with external diodes has to be applied. For instance, if reverse conducting capability is required, the extra diode must be connected in antiparallel with the IGBT. In turn, if reverse blocking capabilities are required the extra diode has to be series connected.

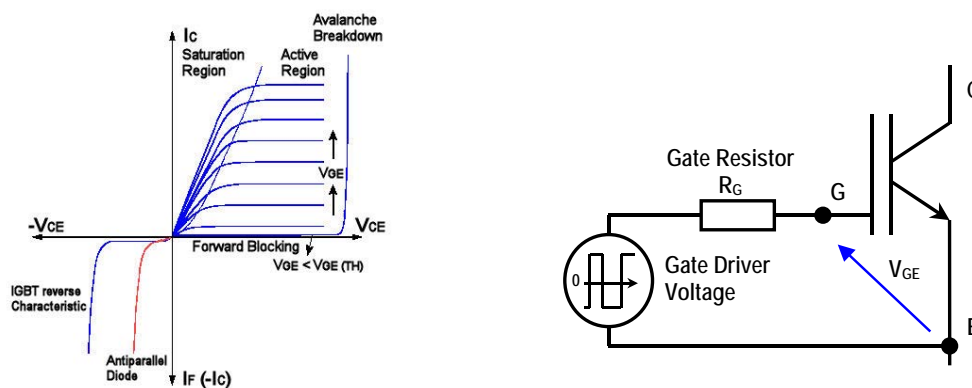


Figure 1-14.- IGBT static characteristic. Control by resistance principle

- Forward off state:** If the collector-emitter voltage  $V_{CE}$  is positive and the gate-emitter voltage  $V_{GE}$  is lower than the gate-emitter threshold voltage  $V_{GE (TH)}$ , a very small collector – emitter cut-off current is established. If  $V_{CE}$  increases, this current raises slightly till a certain maximum breakdown voltage  $V_{(BR) CES}$  where the avalanche breakdown phenomenon of the blocked junction appears. The multiplication current generated by the avalanche breakdown leads to the destruction of the IGBT.
- On-state:** The forward on-state characteristic of an IGBT can be subdivided in two regions. In the active region, the gate-emitter voltage  $V_{GE}$  slightly exceeds the threshold voltage  $V_{GE (TH)}$  and controls the collector current depending on its forward transconductance characteristic,  $g_{FS}$ , which defines the output characteristic of the component ( $dI_C/dV_{GE}$ ). In the saturation region, also called on-state when the IGBT is used in switching operation,  $V_{GE}$  is much larger than  $V_{GE (TH)}$  and consequently the saturation collector-emitter voltage  $V_{CE SAT}$  of the component is extremely small compared to the breakdown voltage  $V_{(BR) CES}$ .
- Switching behaviour:** The IGBT switching behaviour is determined by its internal capacitances (charges) and the internal and external gate resistances. Usually, IGBTs are driven by means of a controlled square voltage applied to the gate-emitter terminals through an external current limiting resistor, Figure 1-14. The value of the applied voltage and the gate resistors fix the extracting or injecting speed of the internal charges, which defines the speed and losses of the component's switching transient. In that way, the  $dI/dt$  at turn on and the  $dV/dt$  at turn off can be limited by adjusting the  $V_{GE}$  maximum and minimum values together with the gate resistor values (single gate resistor or two separate resistors for turn-on and turn-off).

Moreover, the commutation processes are affected by the parasitic connection inductances existing in the power layout and generated by connection of transistor chips in power modules; they induce transient over-voltages and may cause oscillations due to the circuit and transistor capacitances. The idealised hard switching waveforms can be observed in Figure 1-15. The IGBT bipolar effect at turn off (tail current) and the free-wheeling diode reverse recovery current  $I_{RR}$  reflected over the collector current  $I_C$  at turn on can be appreciated. Also, during both switching transients, the effect of the voltage drop (positive or negative) on the parasitic inductor of the switching loop is taken into account.

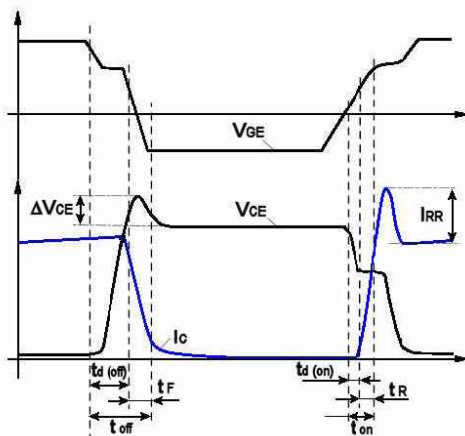


Figure 1-15.- IGBT idealised hard switching waveforms

- *Reverse state:* IGBT chips are designed mainly to comply with a high forward off-state voltage capability and optimised collector heat dissipation, which results in an ineffective reverse characteristic. So, the characteristics of the external diodes are exclusively responsible for the reverse on-state behaviour of IGBT modules.

Since the introduction of the IGBT, several structures have been considered, mainly planar structures. Promptly the “Non Punch Through” IGBT technology (homogeneous structure) dominated the original “Punch Through” concept based on Epitaxial technology, thanks to its easy paralleling ability provided by its on-state characteristic with positive temperature coefficient.

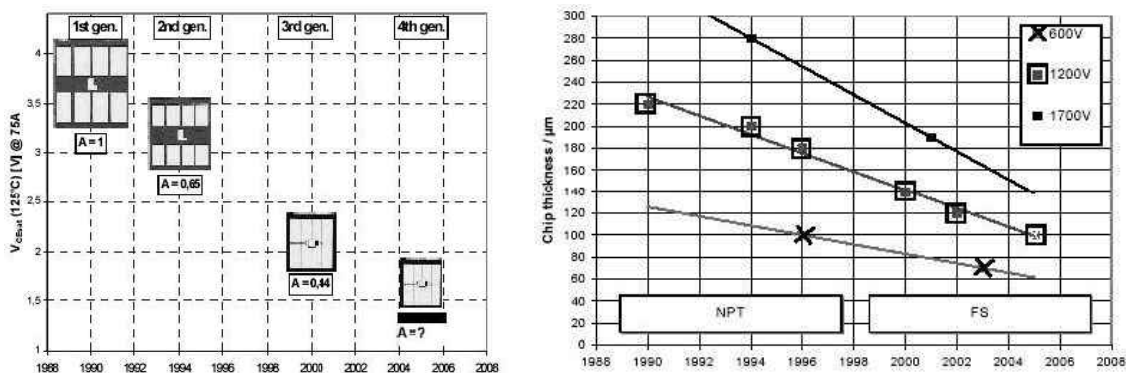


Figure 1-16.- Past and forecast 75A/1200V chip size and thickness evolution for NPT and Field-Stop IGBTs.

Nowadays, because of economic reasons, there is a strong demand for smaller chips with lower on-state and switching losses. A good indicator of the IGBTs evolution in terms of on-state and switching losses is the size and thickness evolution for a specific current / voltage die, as

depicted in Figure 1-16, [GUT-03]. As a consequence of smaller chip sizes, current densities are increased as well as the power dissipation density in combination with smaller silicon heat capacity. To combine these performances, new structures are being applied, even the consideration for vertical structures (Trench IGBTs). Among the structures now considered, the planar SPT (Soft-Punch-Through) and the vertical Trench-FS (Field Stop) technology offer the best performances, Figure 1-17. Both technologies show significant improvements over NPT-IGBTs, [LI-03].

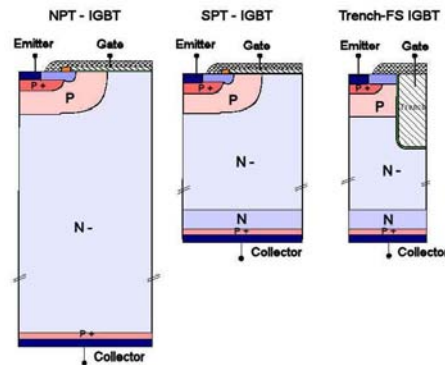


Figure 1-17.- NPT, SPT and Trench – FS IGBT structures

The switching behaviour of the SPT-IGBT is optimised to obtain linear voltage rise at turn off, low voltage overshoot, low and short tail current, and a smooth transition between fall and tail phase. Even the saturation voltage is improved with respect to the standard NPT-IGBT, while the chip area and consequently the thermal resistance remain almost unchanged. The Trench-FS technology leads to an improvement of the saturation voltage by more than 30% compared to NPT-IGBT, while the chip size is reduced to about 70%, thus the current density is higher. However, it has a higher thermal resistance as a side effect.

Thanks to all the different existing technologies, the component design can be adapted to the application requirements. IGBTs with switching losses, conduction losses or the total losses optimisation are commercially available.

## 1.2.5 Fast Recovery Diodes

The excellent switching performances offered by the existing controlled switches (IGBTs, GTOs and IGCTs) also requires adapted fast recovery diodes with low static and dynamic losses, enhanced Safe Operating Areas (SOA) and controlled (soft) recovery at very high  $di/dt$  and  $dV/dt$  levels. In most applications, the critical need to minimise stray inductance between the switch and the associated snubberless diode encourages fast diode commutation. Furthermore, these diodes can play different roles depending on their function on the circuit, (Snubber, Clamp, Free-Wheel Diode, inductive or resistive commutation), and often one single diode is not well adapted to be applied everywhere, [GAL-98]. For these reasons, semiconductor manufactures are developing new generations of diodes, trying to obtain lower reverse peak current  $I_{RR}$  together with "soft recovery" performances, keeping the diode switching losses as low as possible.

Two basic diode structures can be considered for fast power diodes, the Schottky and the PIN structure, [SEM-a]. The Schottky diode structure applies a metal-semiconductor junction as a blocking junction, which provides a very low on-state voltage and very low reverse recovery current. However, the Schottky structure application is only efficient for diodes with blocking voltage lower than 100V. Above 100V, PIN diodes, where the intrinsic zone (I) is obtained by means of  $N^-$  material, are the preferred structure. For voltages reaching 600V PIN-epitaxial diodes are used, whereas for higher voltage levels PIN-diffused diodes are produced, Figure

1-18. For high power fast recovery diodes, the on-state and dynamic losses trade-off and the adapted recovery behaviour is obtained combining the PIN structure with additional manufacturing techniques, (Controlled Axial Lifetime CAL diodes, [WEB-97], Emitter controlled EmCon diodes, [BIE-03]).

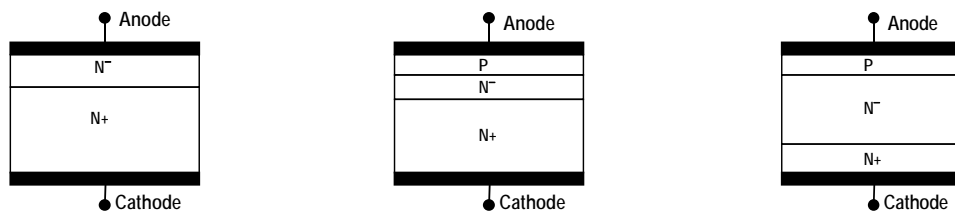


Figure 1-18.- Schottky structure, PIN-epitaxial structure and PIN-diffused structure

- Forward and blocking behaviour.* For a PIN diode structure, the diode voltage drop in the forward direction is defined by the voltage drop of the PN-junction ( $0.6 \div 0.8V$ ) and the resistance of the adjacent  $N^-$  zone. At the same time, the blocking voltage capacity of the diode (breakdown voltage  $V_{BD}$ ) depends directly on the thickness of the  $N^-$  zone. Consequently, for fast diodes with a blocking voltage of 600V and more the ohmic part prevails.
- Turn-on behaviour (forward recovery):* When the diode is turned on with high  $di/dt$ , the carrier gradient does not develop immediately, resulting in an overshoot voltage that decays with time to the normal forward voltage dc static level. The diode appears to be inductive; however, transit time and conductivity modulation, not only inductance, are responsible for this effect. This turn-on overshoot (dynamic) voltage appears generating turn-on losses. Usually the turn-on losses are neglected, however, for high power semiconductors and extremely high  $di/dt$ , the diode turn-on dynamic voltage can be relatively high (several hundred volts) and can alter the transient waveforms of adjacent switches.
- Turn-off behaviour.* The diode turn-off performance is mainly defined by its reverse-recovery characteristic. When diodes change from the on-state to the blocking state, as they are minority carrier devices, their internal storage charges have to be discharged. This results in a current flowing in reverse direction in the diode with a peak value called peak reverse recovery current  $I_{RRM}$ , Figure 1-19.

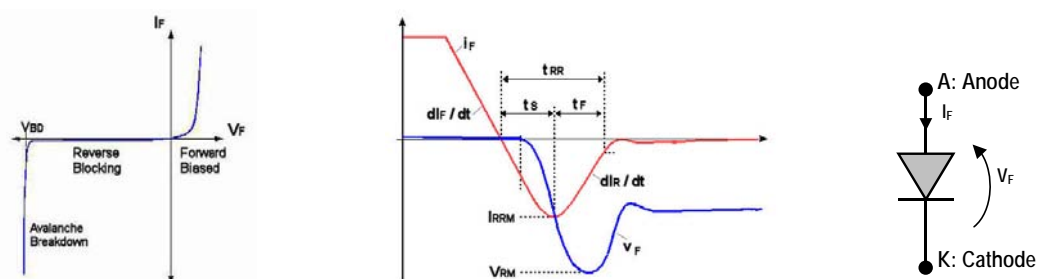


Figure 1-19.- Diode Static characteristic. Soft-recovery diode reverse recovery behaviour

This peak current changes with the diode on-state current value  $I_F$  (storage charges), the current decreasing ratio ( $di_F/dt$  negative) imposed by the external circuit (active or passively limited), the temperature of the component and also the diode operating voltage. With the negative reverse recovery current already established in the diode,

the diode starts to block (diode reverse voltage starts increasing) when the PN-junction in the diode is free of charge carriers. After that, the maximum peak reverse recovery current  $I_{RRM}$  is attained. Finally the current falls to the leakage current level depending solely on characteristic of the diode (diode recovery characteristic). If the current drops very steeply, this is called snappy recovery behaviour. If the current drops very softly, this is called soft recovery behaviour. The subdivision of the total reverse recovery time  $t_{RR}$  into  $t_F$  and  $t_S$  is used to define the qualitative behaviour of the diode through the Recovery factor  $s$  (Eq. 1-5). The bigger the  $s$  factor is the softer the diode recovery behaviour is.

$$s = \frac{t_F}{t_S} \quad \text{Eq. 1-5}$$

If the diode voltage is unclamped, for instance by means of the DC link capacitor in a voltage source inverter, a voltage overshoot is generated imposing the maximal reverse voltage  $V_{RM}$  that the diode has to withstand. This voltage overshoot depends on the diode characteristics (recovery current, parasitic capacitance) but also on the external circuit parasitic inductance. Furthermore, this over-voltage (together with the reverse recovery current) is hardly responsible for the turn-off losses of the diode and must be limited carefully.

High power diodes in module and press-pack packages are available to complement the converters using snubberless controlled switches. However, in many cases the operation mode of the controlled switches is limited by the behaviour of the fast recovery diodes (in terms of power losses and SOA), which must be seriously considered when selecting the correct diode.

## 1.3 IGCT Implementation

The safe utilisation of IGCTs requires the knowledge of several aspects that must be considered when designing IGCT based power converters. The following paragraphs point out and clarify these most critical aspects regarding electrical, mechanical and cooling issues.

### 1.3.1 Electrical Issues

First of all, IGCTs must be selected according to the intended application. For instance, three different ABB asymmetric IGCT versions are commercially available, specially tailored for specific applications (low turn off losses, low on-state losses and wide temperature range). Each version defines different operation restrictions to the component regarding its SOA capability, driver power consumption requirements and so on. Then, for these different versions, there are common electrical restrictions that must be adhered to (maximum switching frequency,  $di/dt$  limitation, etc.)

#### 1.3.1.1 SOA (Safe Operating Area)

The maximum controllable turn-off current limit,  $I_{TGOM}$ , of the IGCT SOA, varies with the component junction temperature (wide temperature range version) and with the permanent DC voltage (low turn-off losses version), Figure 1-20. For any specific application, the worst case must be considered, which can dramatically limit the switching current capacity of the component. Of course, the SOA characteristic assumes that the gate driver is able to commutate the total cathode current to the gate to avoid the IGCT turning off in GTO mode (gate current lower than cathode current), which will lead to the destruction of the component.

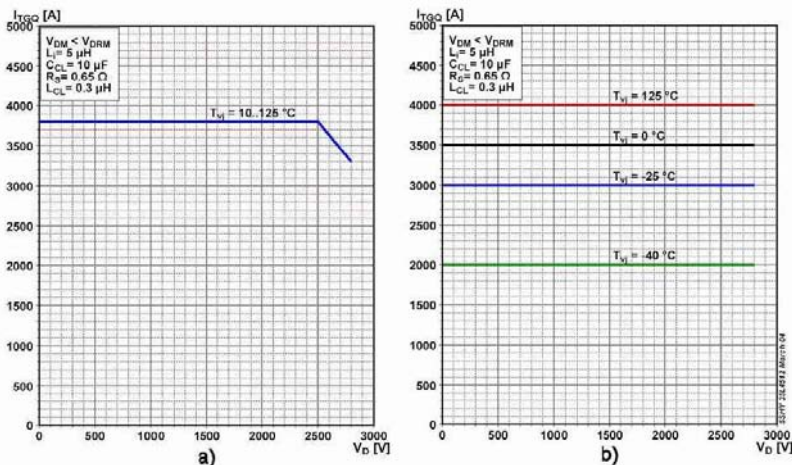


Figure 1-20.- ABB 4.5kV asymmetric IGCTs SOA. a) 5SHY35L4511, b) 5SHY35L4512

In terms of voltage, the SOA is not limited by maximum repetitive peak off-state voltage  $V_{DRM}$  that the component can withstand but by its cosmic radiation withstand rating. In the early 1990's, it was found that cosmic particles can lead to random destruction of power semiconductors exposed to high blocking voltages for long periods. Thus, the SOA voltage limit is fixed by the maximum permanent DC voltage that guarantees a failure rate of 100 FIT (1FIT represents 1 failure in  $10^9$  hours) due to cosmic radiation at sea level.

### 1.3.1.2 Gate driver

As its name denotes, in the IGCT (Integrated Gate Commutated Thyristor) the gate unit is provided together with the semiconductor (GCT). In that way the manufacturer can control parameters like the pulse amplitude of the gate-cathode turn-on and off voltage, the gate circuit inductance, the back-porch current (IGCT on-state gate current), etc., to allow safe operation of the semiconductor. The direct application of the semiconductor on a power converter is much more easy and only the driver power supply specification, control signal transfer and mechanical assembly has to be defined by the converter designer, Figure 1-21.

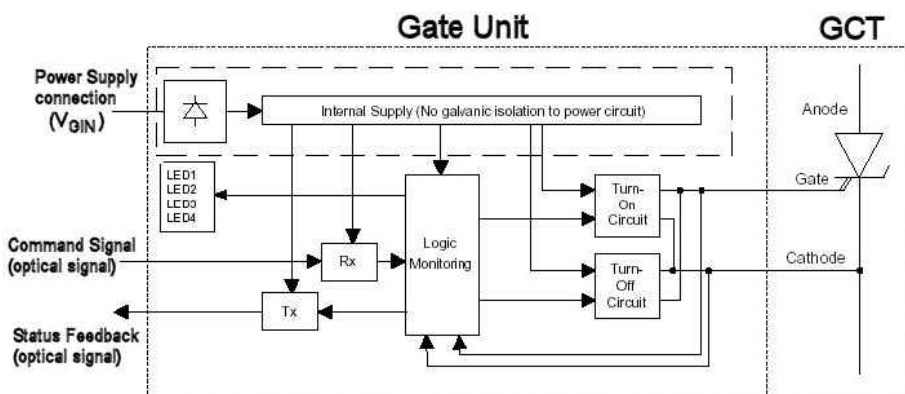


Figure 1-21.- IGCT gate unit synoptic

One of the most critical aspects to guarantee safe operation of the IGCT is the definition of the power consumption of the gate unit power supply. If the power rating of the gate unit power supply is not enough, the gate unit will not be able to block the IGCT safely. During the GCT turn-off process the gate driver capacity to commutate the cathode current will not be enough and it will switch into GTO mode (gate current lower than cathode current). As neither  $di/dt$  nor  $dV/dt$  snubbers are used (like in GTO circuits), the current distribution on the GCT will not be homogeneous and the destruction of the component will be induced.

The gate unit power consumption is directly influenced by the turn-off current, the switching frequency, the operating duty cycle, the chip temperature and the device technology (gate charge). That means that the definition of the gate unit power consumption is strongly application dependent. Information about the gate unit power consumption can be obtained from the component data sheet, Figure 1-22, however, not all the cases of operations are covered and approximate calculations have to be performed including a suitable safety margin. Of course, the power supply voltage and insulation has to be adapted to the selected IGCT and to the converter maximum operating voltage. Also gate unit internal component limitations must be considered (active and passive ratings, thermal limitations, etc.), which could limit the semiconductor work conditions to obtain the gate unit expected lifetime, Figure 1-23.

From a signal control point of view (mainly fiber optics are used to provide high insulation and immunity performances), several aspects have to be considered. In normal operation, minimum IGCT ON and OFF times ( $t_{ON\ MIN}$  and  $t_{OFF\ MIN}$ ) as well as a minimum switching period ( $t_{ON} + t_{OFF}$ ) defined on the component datasheet must be respected to guarantee safe component operation. The gate unit provides an internal minimum pulse width limitation (ON and OFF), but these minimum values are usually smaller than the values defined on the datasheet to allow single event protection sequences. Also, special care must be taken on the power up and down sequence of the control and the power stages. As the gate unit takes some time to become active, if control signals are sent during this sequence and voltage is applied across the GCT, high frequency operation can be generated leading to the destruction of the IGCT.

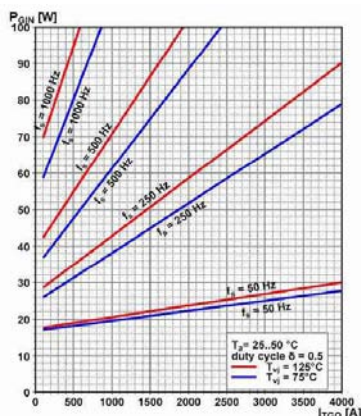


Figure 1-22.- ABB 5SHY35L4511 asymmetric IGCT (4.5kV) gate unit power consumption

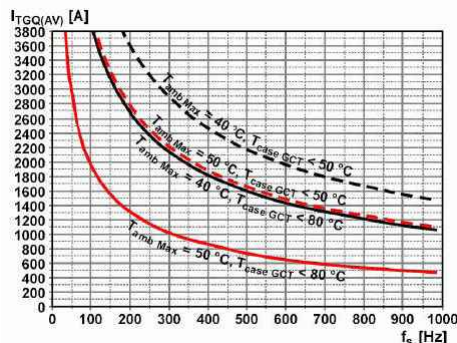


Figure 1-23.- ABB 5SHY35L4511 asymmetric IGCT (4.5kV) maximal turn-off current versus switching frequency for lifetime operation (20 years calculated lifetime of gate unit on-board electrolytic capacitors)

Special attention has to be paid in certain applications (voltage source inverters, soft switching converters) where load current sign changes quickly during the IGCT on-state. If this change induces the conduction change from the freewheeling diode to the GCT (negative to positive switch current), the thyristor regenerative effect has not been built in and the GCT is not yet ready for conduction. Inhomogeneous current distribution in the semiconductor can be established and device failure could be reached if this effect is reproduced in repetitive mode. If a critical rate of rise of the on-state current ( $di/dt_{CR}$ ) defined on the datasheet is exceeded, this failure mode can be attained. To provide safe operation over this working operation mode, an external re-trigger pulse has to be generated by the controller, which will require a more complicated driver to define the re-triggering pulse generation timing (gate-cathode voltage measurement, timing accuracy, etc.), [LUS-04].

IGCT status feedback is provided by the gate unit by means of an optical status signal that can be used to detect fault operations on the GCT and / or the gate unit (gate unit supply voltage

fault, gate-cathode short circuit / open circuit, etc.). Sometimes, additional visual feedback is provided by means of LED diodes.

### 1.3.1.3 di/dt limitation, clamp circuit

Even if IGCTs can be used in snubberless operation, as the gate signal has no influence to the collector current and switching speed, passive di/dt limitation at turn-on is required. This requirement is not imposed by the IGCT itself but by its associated freewheeling diode. di/dt values higher than the diode di/dt<sub>CRIT</sub> limit specified on its datasheet will led to excessive diode recovery current (out of its SOA), thus excessive peak power losses will be generated causing hot spots on the wafer and the destruction of the component. Depending on the IGCT version and its complementary free wheeling diodes, di/dt rates higher than 1kA/μs are not exceeded.

The IGCT di/dt limitation at turn-on (diode turn-off) is provided by means of a series inductor  $L_i$  between the DC link and the switching cell, Figure 1-24. As this inductor stores a certain amount of energy during the on-state of the switching cell, a voltage clamp circuit (RCD) is required to avoid its uncontrolled discharge generating destructive voltage spikes at IGCTs turn-off. The parasitic inductance  $L_{CL}$  between the RCD clamp circuit and the switching cell connection must be minimized to avoid uncontrolled voltage overshoots on the semiconductors and to minimise the turn-off losses.  $L_{CL}$  values around 300nH are acceptable.

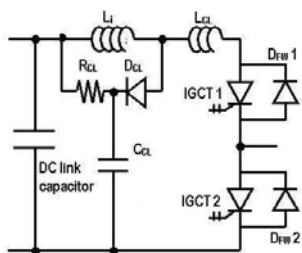


Figure 1-24.- IGCT di/dt limitation and clamp circuit

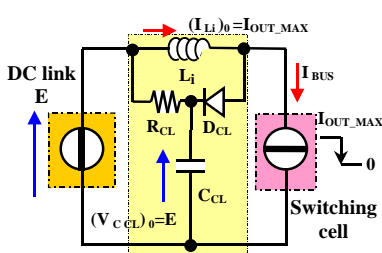


Figure 1-25.- Clamp simplified analysis circuit at IGCT turn off

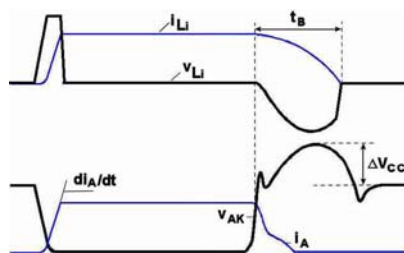


Figure 1-26.- di/dt limitation inductor  $L_i$  ideal waveforms

The values of the different di/dt limitations and clamp circuit components are selected with consideration of the converter and semiconductor worst case working conditions. Firstly, the minimum di/dt limitation inductor value  $L_i$  is selected considering the maximum DC link voltage and diode di/dt at turn off, Eq. 1-6.

$$L_{iMIN} = \frac{V_{DC LINK MAX}}{di/dt MAX} \tag{Eq. 1-6}$$

Then, the clamp capacitor  $C_{CL}$  and resistor  $R_{CL}$  values have to be selected to find a compromise between the transient blocking time  $t_B$  and the voltage overshoot over the semiconductors  $\Delta V_{C_{CL}}$  at IGCTs turn-off (existing due to the discharge of the energy stored on the di/dt limitation inductor  $L_i$ ), Figure 1-26. To evaluate  $t_B$  and  $\Delta V_{C_{CL}}$ , several simplification hypotheses are considered when analysing the resonant di/dt limitation and clamp circuit behaviour at IGCTs turn off, Figure 1-25:

1. The switching transition at IGCTs turn-off is modelled by an ideal current step function changing from the switching cell output current  $I_{OUT\_MAX}$  to zero.
2. No parasitic terms of the different components are taking into account, only ideal components are considered.



- The voltage and current initial conditions on the different components are fixed to the maximal working conditions defined by the converter characteristics.

Considering these simplifications, the  $t_B$  and  $\Delta V_{C_{CL}}$  maximum values expressions are obtained as function of the working conditions and the components values, Eq. 1-7 - Eq. 1-9.

$$(t_B)_{MAX} = 2 \cdot R_{CL} \cdot C_{CL} \cdot \sqrt{a} \cdot \left[ \pi - \arctan \left( \sqrt{\frac{1}{a}} \right) \right] \tag{Eq. 1-7}$$

$$(\Delta V_{C_{CL}})_{MAX} = 2 \cdot I_{OUT\ MAX} \cdot R_{CL} \cdot \sqrt{a} \cdot \sin \left[ \arctan \left( \sqrt{\frac{1}{a}} \right) \right] \cdot e^{-\left[ \sqrt{a} \cdot \arctan \left( \sqrt{\frac{1}{a}} \right) \right]} \tag{Eq. 1-8}$$

$$a = \frac{L_i}{4 \cdot R_{CL}^2 \cdot C_{CL} - L_i} \tag{Eq. 1-9}$$

The analysis of these expressions points out the multiple possible solutions for the selection of the couple  $R_{CL}$ - $C_{CL}$ . A graphical evaluation of these expressions for different commercially available capacitor values as a function of the resistor value is used to select the components. A safe over-voltage value is firstly defined and then the capacitance and resistance values are selected to obtain a reduced transient blocking time, Figure 1-27. When selecting the resistance and capacitor value, the designer must also consider the RC time constant and the resistor peak current due to the over-voltage on the  $C_{CL}$  (discharging phase to the DC link after  $t_B$  is finished).

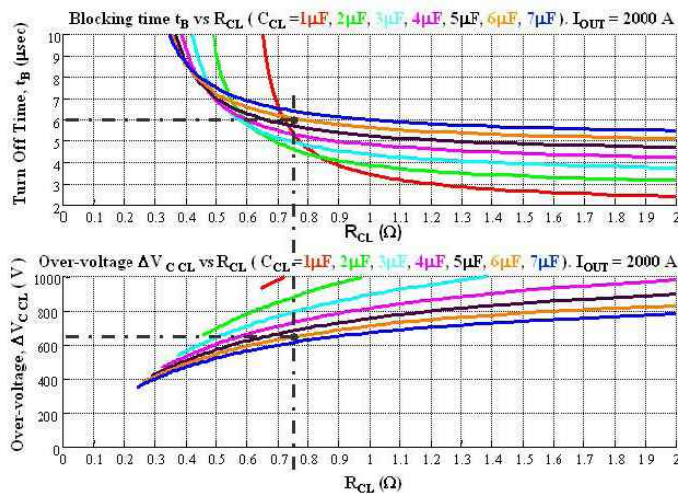


Figure 1-27.-  $t_B$  and  $\Delta V_{C_{CL}}$  Graphical evaluation fro  $R_{CL}$  and  $C_{CL}$  selection

The power and current ratings of each component is highly dependent on the application. Circuit simulations help to define these parameters.

Special attention must be paid when a single common  $di/dt$  limitation and clamp circuit is used for several switching cells (more than one). The switching timing must be adapted to allow effective  $di/dt$  limitation. In fact, even if the controller asks for IGCTs turn-on, no turn-on order has to be sent if the turn-off blocking process of the clamp circuit is not finished, otherwise the  $di/dt$  limitation will not be provided (the clamp circuit diode is conducting and the clamp circuit capacitor is connected in parallel with the switching cells) and the destruction of the free-wheeling diodes will be induced.

### 1.3.2 Mechanic and Cooling Issues

The use of press-pack semiconductors provides very good thermal evacuation capability thanks to the double-sided cooling characteristic of this technology. In general, the silicon wafer main contacts (anode and cathode) are electrically and thermally accessible by means of different metal interfaces, which are laterally coated by a ceramic housing. Molybdenum interfaces are used to provide high mechanical strength properties (low deformation) against thermal (dilatation) and compression efforts, and copper interfaces provide the external anode and cathode contacts. The gate electrode is arranged on the component cathode side and then externally accessibly through the ceramic housing. Finally, the package is filled with nitrogen and hermetically sealed to ensure long-term stability of both the blocking junction and contact interfaces, Figure 1-28. One specific characteristic of press pack components provided by its mechanical structure is the well known state after failure of the component, it always remains in short-circuit.

In most of the cases, press pack packages apply the Free Floating Silicon Technology [ABB-b], which basically means that the main elements of the component can slide freely over each other. This implies the need of an external specific compression force  $F_M$  across the press-pack semiconductor to establish good electrical and thermal contact with the silicon wafer. Even for the most basic device verifications with low-current, a minimum clamping force is required.

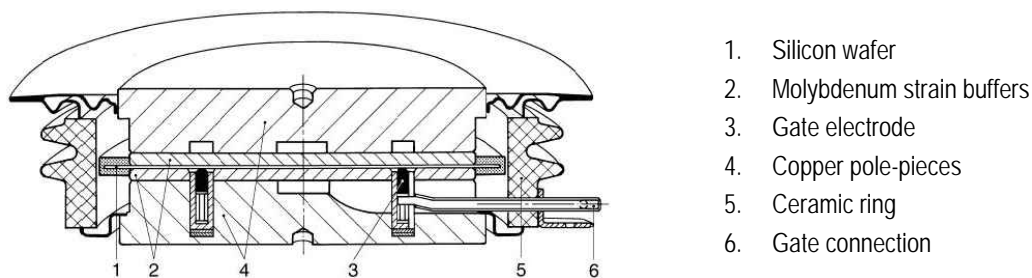


Figure 1-28.- GTO press-pack construction

The amplitude of the mounting force and how it is distributed over the entire wafer has foremost influence on the thermal resistance (impedance) and power dissipation of the component. An insufficient mounting force results in increased thermal resistance and could not provide good electrical contact with all cathode segments, which leads to the increase of the on-state voltage and current capacity limitation. In turn, an excessive mounting force leads to increased mechanical stress on the silicon wafer, which reduces life expectancy of the device and can lead to gate-to-cathode short circuits. To utilise the semiconductors' full potential, it is crucial to apply the force  $F_M$  predefined in the datasheet and to guarantee its homogeneous distribution over the entire semiconductor surface. For these reasons, a proper mechanical design of the complete assembly, including press-pack high power semiconductors, heat sinks, bus bars and other components, has to be applied. The different elements have to be designed considering thermal expansion, tolerances (surface roughness and flatness) and mechanical robustness to withstand high compression forces without deformation (even more than 40kN as nominal required force).

Ideally, the mounting force should be applied from a single point above the centre of the device, Figure 1-29, which can be obtained by using a spherical transmission force contact (spherical cup). To achieve good pressure uniformity, considering an ideal 90° force cone, Figure 1-30, a force spreader plate with a minimum thickness equal to half the pole-piece diameter of the device is recommended, [BAC-04].

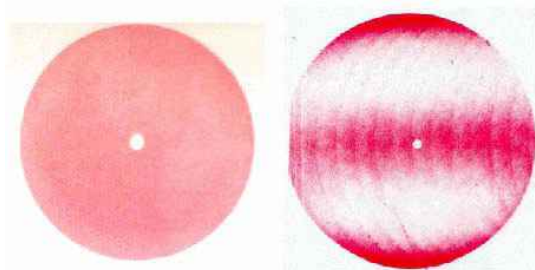
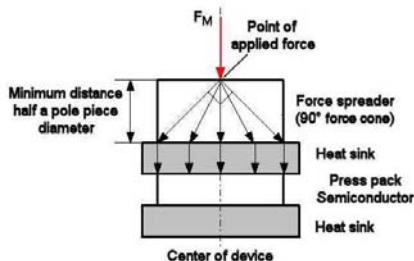


Figure 1-29.- Mounting force Ideal application    Figure 1-30.- Good and poor pressure distribution

### 1.3.2.1 The mechanical assembly

The main element of the clamping system is the mechanical clamp, Figure 1-31. It consists of two strong yokes (4, 8) joined together by means of two (or more) threaded rods (7). The upper yoke includes the applying force set which is attached by means of a blocking nut (1). This nut is used to calibrate the applying force and should not be unbolting once the calibration is performed (attachment of the stack components is provided acting over the nuts of the threaded rods). Below this blocking nut, a test washer (2) indicates that the pre-calibrated force is already applied when released. Then it can be fixed thanks to the positioning pin (3).

The force applying element consists of several spring rings already over pressure (5). Then, a spherical cup (6) is used to ensure that the force is correctly transmitted even if slight non-parallelism exists due to tolerances of the stack components. Once all the stack components are aligned by means of positioning pins, they are placed on the mechanical clamp and tightened by symmetrically screwing down the threaded rod screws (9). As can be seen in Figure 1-32, a single semiconductor stack components usually comprises the semiconductor, a heat sink on each side of the semiconductor, to force spreaders (one on each side of the stack), and the mechanical clamping system. Isolation between the top and bottom side of the stack is required and provided by insulation of the threaded rods and the mechanical contact between the upper force spreader and the spherical cup (the right materials and the right air and creepage distances must be utilised). Electrical contacts to the semiconductor are usually accessible through attaching terminals on the heatsinks. Flexible bus bars connections to the heatsinks are recommended to avoid uncontrolled external forces (heat expansion and contraction and mechanical tolerances), disturbing homogeneous pressure distribution within the stack.

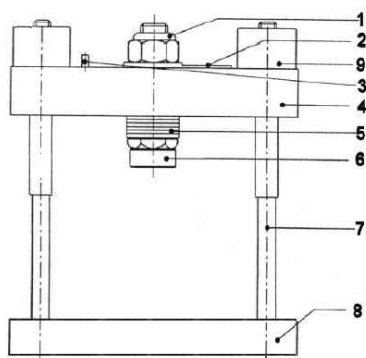


Figure 1-31.- Mechanical clamp drawing

Figure 1-32.- Press pack diode arrangement

If several semiconductors have to be stacked with the same mounting clamp, their rated mounting force should be the same to avoid over-stress or insufficient pressure for some of the devices in the stack, Figure 1-33. It is also advisable to use devices with the same pole piece

diameter to simplify the heat-sink design in order to achieve good pressure distribution on all devices. In cases of paralleling or anti paralleling devices, independent mounting clamps should be used, otherwise mechanical tolerances (height and parallelism) will create mechanical forces large enough to significantly reduce the lifetime of or even destroy the devices.

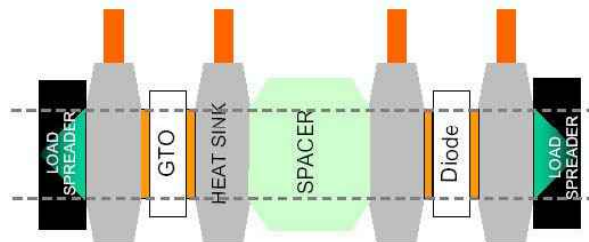


Figure 1-33.- Well designed stack with effective load spreaders and similar device diameters.

### 1.3.2.2 Heatsinks

Air or water-cooling heatsinks can be applied for double or single side press-pack cooling. In both cases the heatsinks must have adequate mechanical robustness to withstand the compression force and the adapted surface finish (flatness and roughness) to guarantee proper thermal resistance values.

When air-cooled heatsinks are used, proper air canalisation must be provided and adapted fans must be applied to allow enough airflow to overcome the pressure drop in the canalisation.

If water-cooled assemblies are used, since water is electrically conducting (around  $1\text{M}\Omega/\text{m}$ ) and the heat-sinks work under potential, a long enough tube length between heat-sinks with different potential has to be considered. De-ionised water should be used together with the water treatment equipment needed to remove conducting particles and to keep the water conductivity low. Very stiff tubes should not be used to avoid high mechanical forces caused by thermal expansion and contraction. Also, non-corroding materials (Teflon, PTFE, steel, etc) should be used to ensure a long lifetime of the water-cooling system. Regarding the water distribution possibilities, paralleling of heatsinks allows working with low pressure values to cope with the high pressure drops on the heat-sinks. However, high water flow rates are required. Heatsinks in a series arrangement require lower flow rates but high pressure requirements, which increase the risk of water leakages. Usually water pumps are used to obtain the required water distribution pressure and flow rates. Finally, heat exchangers (water to air or water to water) are required to remove the heat generated by the semiconductors from the water.

## 1.4 IGCT Future Trends

Nowadays, existing IGCTs (asymmetric, reverse conducting and reverse blocking) cover a huge range of application at medium voltage levels (Medium Voltage Drives, Static Circuit Breakers, DVRs, DUPs, SMES, BESS, Interties, etc.) with different conversion structures (Voltage Source Inverters, Current Source Inverters, series connection, soft switching, etc.), [CAR-01] [STE-00]. However, IGCTs of higher and lower voltage and current ratings could provide several benefits in specific applications. For this reason, further research and development efforts are carried on to improve the IGCTs performance and to expand their field of application.

Series connection of standard IGCTs without selections or adjustments using RCD snubbers [STE-96] or using simple a RC snubber and IGCT matching up [LYO-99] has already been successfully proven. However, to minimise the component part count of these solutions, serious

investigations about the 10kV IGCT are being held. Higher currents have already been realised up to 6 kA [OKA-03] and will become more common in the future for high power applications. For lower current and voltage ratings, purely commercial issues, market potentials and the “pros and cons” with respect to IGBTs will define their introduction on the market. A review of the most relevant IGCT trends and actual developments is presented in the next paragraphs.

### 1.4.1 10kV HV IGCTs

One clear technical trend of medium voltage pulse width modulated (PWM) converters is the increase of the converter voltage and power. Nowadays, 2.3, 3.3 and 4.16 kV<sub>RMS</sub> standard line voltages are reached, applying 3-level Neutral Point Clamped voltages source converter with a single semiconductor for switch position. For higher line voltages, 6.6–7.2 kV<sub>RMS</sub>, series connection of several semiconductors [NAG-01] or converters with higher number of levels [EIC-01] must be used, increasing the complexity, cost and reliability of the total system. Therefore, the research on 10kV IGCTs is motivated by the simplification of power converters dealing with 6.6–7.2 kV<sub>RMS</sub> line voltages for Medium Voltage Drives and Power Quality applications, [EIC-00]. The part count reduction (RC snubbers, semiconductors and gate drivers, etc.) will lead to lower cost, increased reliability, and simpler design and maintenance, [BER-03]. However, if compared to the series connection solution, the power dissipation of a 10kV device will be 50% lower than 2 series connected devices, which limits the power handling capacity of both the semiconductor and the power converter. Also switching limitations due to 10kV fast recovery diode could lead to semiconductor switching capacity limitation.

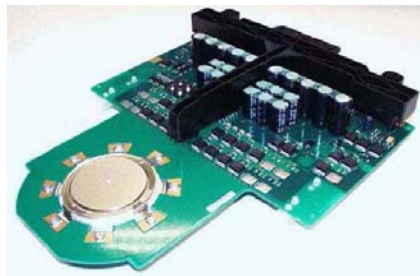


Figure 1-34.- 68mm 10 kV IGCT sample

10kV IGCT samples, Figure 1-34, have been successfully tested in single pulse operation at 7kV<sub>DC</sub> and 1kA turn off current, [BER-03]. Further investigations will demonstrate the potential ability of this component to be applied in practical products.

### 1.4.2 Dual Gate Turn-off Thyristor

The Dual Gate principle consists on the use of a second gate driver to control the IGCT gate-anode voltage (the base-emitter voltage of the PNP equivalent transistor in the thyristor type structure), Figure 1-35. This second gate driver will be able to eliminate the IGCT tail current at turn-off, considerably reducing the switching losses of the component, whereas using a symmetric structure can also provide a considerable reduction of the on-state losses [APE-01]. In addition, anode gate control may offer additional degrees of freedom for series connection and reduction of snubber requirements could be achieved, [APE-02]. The reduction of the switching losses provided by the dual gate principle, if applied to future 10kV IGCTs, could provide not only the required performances of the 6.6 – 7.2kV<sub>RMS</sub> medium voltage drives, but also reduce the cost per MW of the converter compared to a series connection solution. The main drawback comes from a control point of view, where the complexity and accuracy requirements are increased.

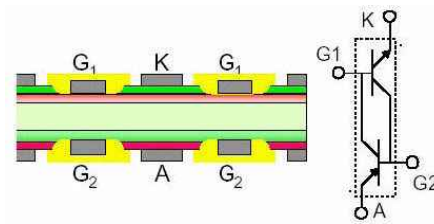


Figure 1-35.- Semiconductor structure of a "symmetrical" Dual Gate IGCT

### 1.4.3 SOA Improvement

The standard IGCT (4.5kV - 6kV) based converters power is limited by the semiconductor SOA capacity. Improvement of the SOA for large area IGCTs could extend the power rating of such converters. Several approaches (optimised gate-circuit, local SOA improvement applying optimised profiles, irradiation and compensation of lateral effects by means of irradiation) have been investigated and combined to obtain more than 30% SOA improvement in large area devices [STI-04], obtaining exceptional results reaching 1MW/cm<sup>2</sup> turn off capability for small devices (38mm), Figure 1-36. However practical application of all these combined technologies can increase the product cost drastically which will limit their use only accessible to very specific applications.



Figure 1-36.- 38mm IGCT sample with experimental gate unit for test purposes

### 1.4.4 3.3kV LV IGCTs

The experimental 3.3kV LV IGCT and their associated free wheeling diodes have been designed on the technology platform of the standard IGCT product line, Figure 1-37. Reduction of the silicon thickness and carefully adapted carrier lifetime engineering provides the required trade-off between the on-state and switching losses to increase the attainable switching frequency (500 - 2000 Hz) of the component, keeping its "high current" capacity (2 - 1kA), [ALV-04b]. Such a component contends for increasing the IGCT field of applications in medium voltage / medium power applications providing higher dynamic performances of the converter. Experimental results show the ability of these components to guarantee continuous hard switching operation at 1 kHz with a turn off capacity of 1.4kA (1.5kV<sub>DC</sub>,  $\alpha=0.5$ ), is limited only by the driver capacity (power supply). If the IGCT power losses are kept constant (around 4.4kW) and the switching frequency is increased to 2 kHz, turn off currents of 1kA over 1.8kV<sub>DC</sub> ( $\alpha=0.5$ ) are accessible. For applications with clear design goals, a further optimisation is possible and further analysis could result in defining such optimised target specifications. However, to reach these working conditions, the power consumption of the gate unit is increased and even further development on the gate unit design is necessary to provide the required internal components (electrolytic capacitors and MOSFETs) lifetime expectancy, which can increase the cost of the component.



Figure 1-37.- Experimental 3.3kV IGCT (5SHY 45L3300) and diodes (5SDF 10H2500)

## 1.5 IGCT vs. IGBT

Nowadays, despite the different technologies of IGCTs and IGBTs, their current and voltage ratings are similar, and for several applications and power converter ratings, both solutions can be applied. Therefore, the selection of the semiconductor has to be made according to relevant considerations like implementation issues, control simplicity, reliability, ruggedness, maintenance issues and of course market availability and cost.

For each application where particular requirements are imposed, a case by case analysis should be required to define the best solution. However, different priority criterions of different designers could lead to different results. For this reason, and trying to provide an objective point of view, the comparison presented here will point out the main advantages and drawbacks of both solutions.

### 1.5.1 Ratings and Mechanical Lay Out

Nowadays, the comparable IGCT and IGBT ratings available from different manufactures are shown in Table 1-2 and Table 1-3. For IGCTs, asymmetric and reverse conducting versions are taken into account. For the asymmetric IGCT, only the components optimised for medium frequency (1 kHz) and low turn-off losses are mentioned. It should be noted, for reverse conduction IGCTs, that the diode average current  $I_{FAV}$  is usually much lower than the IGCT average current  $I_{TAV}$ . The origin of this characteristic is the different section used in the wafer for the IGCT (outer region) and the diode (inner region) integration (separated by the gate contact ring).

All IGBTs are of module type, no press pack IGBTs are available commercially for more than 3.3kV. Components under development or foreseen for new releases are not mentioned.

IGCT					
Type	$V_{DRM}$ (V)	$V_{DC LINK}$ (V)	$I_{TQM}$ (A)	Manufacturer	
Asymmetric	4500	2800	3800	ABB	
	4500	3000	4000	Mitsubishi	
	6000	3600	3000	ABB	
	6000	3600	3500	Mitsubishi	
Type	$V_{DRM}$ (V)	$V_{DC LINK}$ (V)	$I_{TQM}$ (A)	$I_{TAV} / I_{FAV}$ (A)	Manufacturer
Reverse Conducting	4500	2800	340	130 / 85	ABB
			2200	1010 / 400	ABB
	5500	3300	280	110 / 65	ABB
			1800	840 / 340	ABB

Table 1-2.- IGCT available ratings (asymmetric and reverse conducting)

As a general rule, the IGCT switching capacity is higher for a given component adapted to a specific DC link voltage. Basically this is due to the lower on-state losses and higher power evacuation capability of IGCTs. However, the IGBT permanent switching frequency is, for the most part, only limited by its total thermal budget, while the IGCT maximum permanent switching frequency is limited to 1 kHz by the driver. The IGCT can operate at high switching frequency (16 kHz maximum) but only for a limited amount of time (burst mode).

IGBT			
$V_{CE}$ (V)	$V_{DC\ LINK}$ (V)	$I_c$ (A)	Manufacturer
3300	1800	1200 / 800	ABB
		1200 / 800 / 400	Eupec
		1200 / 800 / 400	Mitsubishi
		1200 / 800	Dynex
4500	2800	900 / 600 / 400	Mitsubishi
6500	3600	600	ABB
		600 / 400 / 200	Eupec
		600	Mitsubishi
		400	Dynex

Table 1-3.- IGBT available ratings

Regarding the mechanical lay out of both components, again the applied technologies are completely different. IGCTs require mechanical clamps to provide electrical and thermal contact to the component, Figure 1-38. As the connection interfaces to the press pack are under potential, insulation to ground has to be provided by means of external insulators. Creepage and clearance distances also have to be respected. This implies the adoption of complicated and expensive cooling systems, as is the case when de-ionised water-cooling systems are used. However, the inherent insulation of IGBT modules allows the direct fixation off several devices on the same heatsink, Figure 1-39, which simplifies the cooling system. Nevertheless, when high potential difference exists between these components (for example in multilevel converters) reinforced module insulation could be required.

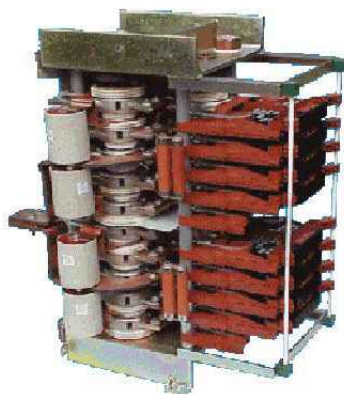


Figure 1-38.- ABB IGCT based Power Electronics Building Block

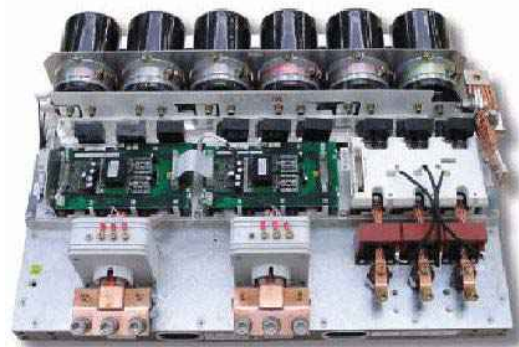


Figure 1-39.- ABB IGBT based Power Electronics Building Block

In terms of stray inductances, IGBTs need complicated laminated multi-layer bus-bar arrangements to minimise the switching loop and to constrain the turn-off voltage overshoot. That



is not necessary for IGCTs because a  $di/dt$  limiting inductor with an RCD clamp circuit is required as an intermediate stage between the DC link and the switching cell. However, it is recommended to minimise the existing stray inductance between the RCD circuit and the switching cell to limit the spike voltage over the IGCT and to minimise the turn-off losses (values around 300nH are acceptable).

When series connection of various semiconductors is required, the press pack package is advantageous because the mechanical arrangement is extremely simple, (the components to be series connected are stacked up on the same mechanical clamp). Also, the well known explosion free short circuit behaviour of press pack components, in case of device failure, can guarantee continuous operation of the system if redundancy components are used. Series connection of IGBT modules becomes much more difficult due to laminated bus bar connections and the unknown device state after failure. However, with IGBTs, the problem of high insulation power supplies is simplified because the gate drivers' power consumption is minimised.

## 1.5.2 Driver

The semiconductor performances are partly stipulated by the gate unit characteristics. This is especially the case for IGCTs, where the specially designed low inductance gate unit is required to safely switch the component in snubberless operation. Similar comments can be mentioned for IGBT drivers, which exert influence on the switching losses of the device ( $di/dt$  imposed by the control signal) and can also integrate protection functions (over current / short circuit protection and voltage active clamping).

The gate unit power supply has to provide the required power to the gate unit, but also static and dynamic insulation according to the device voltage rating. The power consumption for IGBT gates units is low (several watts), which in some cases allows the integration of the power supply together with the gate unit circuit. This is inconvenient in the IGCT case where several tens of watts (50 ÷ 100W) are required. This fact, together with the complexity of the IGCT gate unit, leads to higher cost of the device driving system compared with the IGBT solution. This is an important argument in favour of IGBTs when selecting a semiconductor technology for devices series association.

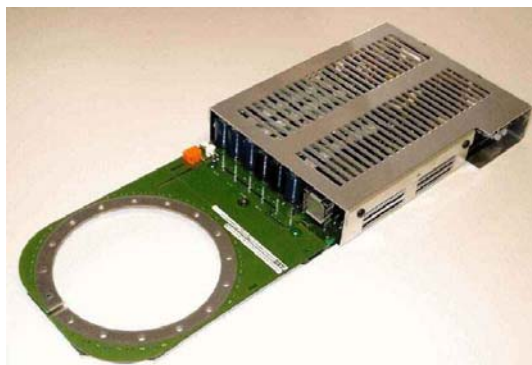


Figure 1-40.- IGCT gate driver



Figure 1-41.- IGBT gate driver

## 1.5.3 Cooling System

When considering the differences between the cooling system for IGBTs and IGCTs, the first important element to take into account is the insulation requirements. As IGCT heatsinks are under potential, additional insulation is required. If air cooling is used, insulated air ducts can be used, however, when water cooling systems are applied, much more expensive and maintenance

demanding equipment is needed (de-ionisation system). Insulation for IGBTs is directly provided by their package (modules), thus no additional insulation for the cooling system is required. However, when using water-cooling system for high voltage equipment, these systems are also used to provide extra insulating properties.

The second point to take into account when IGCTs are applied, is the presence of a  $di/dt$  limitation and clamp circuit. Besides its main function (free wheeling diode  $I_{RM}$  and turn-off over-voltage limitation), this circuit minimise IGCT turn on losses, which can be considered as an advantage because the semiconductor thermal budget is reduced. However, it also represents a drawback. Somehow, the IGCT turn-on losses are derived to the clamp circuit resistor, which also needs to be cooled.

The main advantage of the IGCT cooling properties (press pack) is its ability to use double side cooling, which allows higher heat transfer efficiency compared to IGBT modules.

Regarding the IGBT modules cooling properties, the heat distribution must be carefully taken into account when several modules share a common heatsink. In fact, the IGBT modules represent heat sources that can exert influence on adjacent modules if they are too close. Therefore, the IGBT modules must be spaced out across the large surfaced heat sink such that the lateral spread of the heat sink surface is optimally used and homogeneous transfer of heat is obtained.

## 1.5.4 Reliability

In the small signal electronic field, the failure rate of the different components can be officially obtained by using two databases: the CNET [RDF-93] and the Military Handbook 217 F. The data is even organised to provide failure rate evolution as a function of the device working conditions (junction temperature, blocking voltage, etc). This is not the case in the power electronics field, where only high power semiconductor reliability tests have been developed for thermal cycling strength characterisation [COQ-99b]. Data regarding the relationship between the power semiconductor failure rate and its working conditions is not available, maybe because of the high number of technological (components, cabling, insulation, etc.) and functional (conversion structure, switching mechanism, etc) parameters concerned. For instance, it is generally accepted that reduction of the semiconductor dynamic efforts provided by soft switching operation leads to the improvement of the converter reliability, even if the number of components is increased. However, this fact has never been quantified. Nowadays, only the reliability data provided by the power semiconductor manufacturers is available. The failure rate is given for operation condition with 50% of the current and voltage rated and for fixed ambient temperature, 40°C, [EUP-01], [ABB-b].

$$\lambda = \frac{r}{n \cdot t} \quad \text{Eq. 1-10}$$

$$\text{MTBF} = \frac{1}{\sum \lambda_i} \quad \text{Eq. 1-11}$$

A widely used reliability criterion in power electronics is the component hazard rate (or failure rate). The failure rate  $\lambda$  is defined as the number of occurred failures “ $r$ ” on a fixed number of components “ $n$ ” for a specific period of time “ $t$ ”, Eq. 1-10. The failure rate unity is a FIT (Failure In Time), which corresponds to a failure on  $10^9$  hours. The failure rate is then used to evaluate the Mean Time Before Failure (MTBF) of a total system assuming the individual failure rates of each component  $\lambda_i$ , Eq. 1-11

Regarding IGBTs and IGCTs reliability, the IGCT shows better properties because of the employed technologies (monolithic wafer compared to discrete die association) even if the IGBT technology is already mature, [BAS-02]. Figure 1-42 shows the previous years attainable failure rate evolution for IGBTs and IGCTs, but this evolution does not take into account the semiconductor operating conditions (switching mechanism, cabling quality, etc.). In this way, only an approximate power converter failure rate can be obtained. A more detailed converter reliability analysis requires some practical feedback information of the power converter in real working operation.

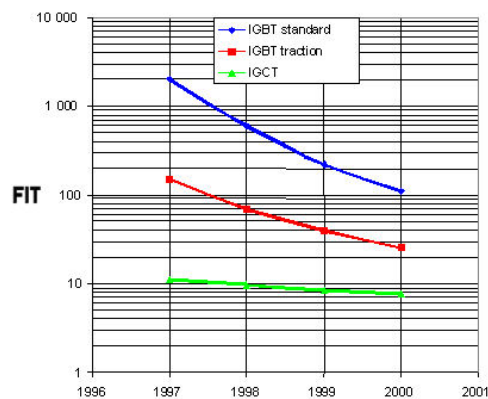


Figure 1-42.- IGBT and IGCT FIT evolution

As an example of converter FIT ratio evaluation, Table 1-4 presents the expected long-term reliability of an 8 MVA / 3-level water-cooled inverter. The data provided by ABB Industry [STE-01a] is based on 15 years of GTO experience, 5 years of IGCT experience and best estimates for future 4.5 kV press-packs.

8 MVA Inverter Type	No of Chips per Switch	Switch (FIT)	No of Chips per Diode	FW Diode (FIT)	Gate Driver (FIT)	N° Parallel Devices	Equivalent Discrete NPC Diode per Position (FIT)	Equivalent Clamp per Position (FIT)	Inverter Total (12 Positions) (FIT)	FIT Ratio to IGCT
IGCT	1	50	1	20	200	1	10	50	3'960	1.0
GTO	1	100	1	20	200	1	10	200	6'240	1.6
IGBT	24	120	12	60	150	2	10	50	9'120	2.3

Table 1-4.- Expected long term reliability of an 8 MVA / 3-level, water-cooled inverter

## 1.5.5 Power Semiconductor Main Failure Sources

Power semiconductor failures can be divided into failures related to the component design and manufacturing process (intrinsic failures) and the failures induced by static or dynamic overload events (electrical, mechanical, thermal) during the component lifetime or due to wrong component utilisation (extrinsic failures), [ABB-b]. From a power converter designer point of view, only the extrinsic failure rates can be affected, which always requires close technical cooperation with the component supplier. The following paragraphs comment briefly the main failure sources for IGBTs and IGCTs.

### 1.5.5.1 Thermal cycling

When successive thermal cycles are applied to power semiconductors, internal structural deformations can cause the device failure. IGCTs and IGBTs exhibit different thermal cycling aging mechanism due to the different technologies applied.

The IGCTs thermal cycling endurance is relatively high thanks to the simple press pack technology where the thermal and electrical contacts between the internal elements require high compressing forces, which limits their eventual deformation. Furthermore, the applied low dilation coefficient materials (Molybdenum) makes the component even less sensible to thermal dilatation. Only the junction temperature change  $\Delta T_J$  exerts influence on the thermal capability of the component.

That is not the case for IGBT modules where several elements (base plate, substrate, dies, bonding wires, solder layers, Figure 1-11), with materials of different deformation and thermal expansion and conduction coefficients are in contact. The thermal cycling effects over such a structure can end to fissures on the solder layers causing the failure of the device. Two types of failures are predominant, "solder fatigue" (deterioration of the solder layer between the base plate and the substrate) and "bond wire lift on" (loss of contact between the bond wires and the die). As a result, for IGBTs the junction temperature change  $\Delta T_J$  and the case temperature change  $\Delta T_C$  affect the thermal cycling capacity of the module.

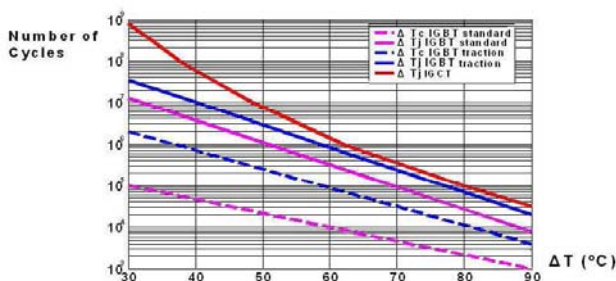


Figure 1-43.- IGBTs and IGCTs thermal cycling endurance versus junction temperature variation

Figure 1-43 shows the thermal cycling endurance of IGBTs and IGCTs considering the maximum junction temperature limited to 125°C [ALV-04a], concluding on higher IGCT reliability to thermal cycling.

### 1.5.5.2 Cosmic radiation

The cosmic radiation influence was discovered in the early 1990's when random destruction of the first 4.5kV GTOs was investigated. It was demonstrated that with higher electric fields on the component, the random failure rate was increased. Essentially, the cosmic neutron radiation was found to be responsible for this semiconductor failure mode. The neutron flow is dependent on the altitude, so the sea level cosmic radiation sensitivity is taken as reference and then increased with the altitude. To minimise this failure mode, semiconductor manufactures established design rules to reduce the electric field inside the device, conferring long term DC stability to their components.

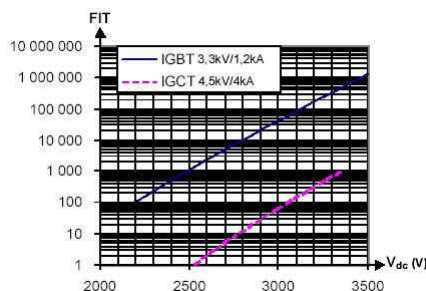


Figure 1-44.- Sea level cosmic endurance for IGCTs (4.5kV) and IGBTs (3.3kV)

In principle, IGBTs are more sensitive to cosmic radiation than IGCTs, Figure 1-44, [BAS-02], but new developments with higher current density and thinner dies could decrease their cosmic radiation sensitivity even more.

### 1.5.5.3 Partial discharges

This failure mode only directly affects the IGBT modules. In fact, the base plate in contact with the heatsink is electrically isolated. In this way, partial discharges can arise, leading to the following consequences:

- Generated electromagnetic interferences can induce perturbations on the control system causing the converter failure and its eventual destruction.
- The module reliability is reduced because of the degradation of the insulating silicone gel inside the modules. This can end in insulation failure and module destruction.

For IGBT modules, the electrical insulation is ensured by the ceramic substrate between the base-plate and the die, the silicone gel inside the module, and the plastic external coating of the module. To fulfil the International Electrotechnical Committee rules (IEC 1287), two basic tests have to be fulfilled; the insulation test and the partial discharge test. The insulation test validates the electrical insulation of the module, and the partial discharge test has to prove that charges below 10pC are released at the end of the test. Figure 1-45 shows the IEC 1287 voltage test profiles that apply for 6.5kV IGBTs.

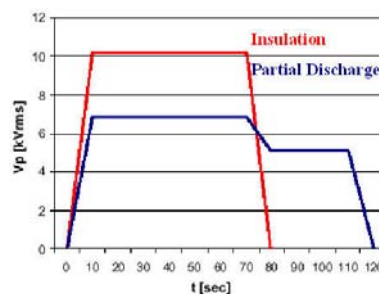


Figure 1-45.- IEC 1287 voltage test profiles for 6.5 kV IGBTs.

### 1.5.5.4 Gate unit failure

The driver of an IGCT is much more complex and requires more power consumption than an IGBT driver, so the gate unit of an IGCT has greater failure rates. In contrast, the difference is not so big if the use of fiber optics for transmission and reception of the control signal is considered, as is the case in most medium voltage and high power applications. In fact the optical transmitter and receiver failure rates are dominant when compared with the failure rates of the other electronic components of the gate unit, which leads to similar total failure rates for both the IGBT and IGCT gate units.

## 1.6 Conclusions

The recent evolution on high power semiconductors allows high power converters to be built in the kV range, applying very different technologies (IGBT, IGCTs) for many different application fields (industrial, traction, energy generation, distribution and transmission, etc.).

Even if the IGBT is getting closer to the IGCT ratings, the IGCT solution is still best suited for medium to high power applications. In the field of low to medium power applications, even if the

IGBT is the favoured component, a case to case analysis defining some priority design criterions (cost, reliability, maintenance, etc.) will be required to select the best solution. The examination in this chapter of the working principles, implementation requirements and future trends of IGCTs provides a clear glance at the advantages and drawbacks of this technology and the opportunities that such a component offers for Medium Voltage / Medium and High power applications.

## 3.3 kV IGCTs Characterisation

### 2.1 Introduction

When power semiconductors work in switching operation (hard or soft), the maximum switching frequency is practically limited by the total power losses and thermal properties of the device. However, the gate unit limits have also to be considered, (single pulse operation, burst mode, permanent switching operation).

For a given heat transfer capacity of the semiconductor and its cooling system, the distribution between the semiconductor on-state and switching losses impose the maximum on-state current and switching frequency that can be handled. Depending on the application, the maximum attainable values can be modified, either giving preference to one of these two parameters (maximisation of the on-state current or switching frequency) or looking for a suitable trade-off.

Currently, for standard 4.5kV asymmetric IGCTs (optimised for medium frequency and low turn-off losses) only switching frequencies below 1kHz are practically considered. If higher switching frequencies are needed, review of the IGCT ratings is required. In that way, based on the existing technology applied to the standard IGCT product line, ABB Semiconductors designed several experimental samples of 3.3kV LV IGCTs and their associated free wheeling diodes. The driver and package for 91mm wafers of the standard 4.5kV/4kA IGCT was used for the 3.3kV IGCT (5SHY 45L3300), whereas the 2.5kV (5SDF 10H2500) free wheeling diode was integrated into a 68mm wafer. Basically, the reduction of the silicon thickness and carefully adapted carrier lifetime engineering provided the required trade-off between the on-state and switching losses to increase the attainable switching frequency (500Hz – 2kHz) of the component retaining its “high current” capacity (2kA – 1kA).

In order to characterise these components, a test bench applying the Opposition Method was developed at the LEEI. The application of this method allows driving the semiconductors under nominal working conditions in PWM operation avoiding the use of multi-megawatt loads and power supplies. The test bench is designed to characterise the semiconductors in DC chopper mode under DC link voltages and DC output currents reaching 1.5kV<sub>DC</sub> and 2kA<sub>DC</sub> respectively. The switching frequency can also be selected (between 500Hz and 2kHz) maintaining the steady state duty cycle constant  $\alpha \approx 0.5$ .

In this chapter, a brief introduction of the standard semiconductor characterisation methods for the on-state and switching losses are given followed by the operation principle of the Opposition method test bench (power circuit and control strategy), its practical implementation and the 3.3kV IGCTs characterisation results.

## 2.2 High Power Semiconductors Characterisation

Semiconductor manufacturers apply the existing standards [JED] [EIA-79], to specify their semiconductor characteristics. To determine the device properties (electrical, mechanical, thermal), several characterisation tests are performed (static and dynamic). Often, test characterisation conditions (junction temperature, off voltage, on current,  $di/dt$  conditions, etc.) do not reflect the real operating conditions of semiconductors in power converters, so the power electronics designer must obtain an estimate of the semiconductor characteristics through extrapolation methods. That is the case with the device power losses (on-state and switching characteristic, mainly concerned in this analysis), which are very application dependent and essential for the definition of the semiconductor maximum current, voltage and switching frequency conditions as well as its cooling requisites [MAN-97]. For this reason, instead of using the standard characterisation methods (single / double pulse) to obtain the power losses characteristics of the 3.3kV IGCT and their free-wheeling diodes, the use of an Opposition Method [TUR-02] test bench that drives the semiconductors under real working conditions is proposed. Thanks to the Opposition Method operation principle, any semiconductor and converter operation mode could be reproduced, only the right conversion structure has to be applied, [BLO-99].

### 2.2.1 Power Losses Characterisation Standard Tests

Semiconductor standards define the conditions that need to be applied to semiconductors in order to perform the characterisation tests. Generally, the semiconductor junction temperature is defined as one of the imposed test parameters and the test itself should not affect the predefined value. The preferred solution to comply with this condition is to control the device junction temperature by external heating and then perform a pulse test, which allows obtaining the required electric characteristics. Normally, high-speed digital systems are used for measuring and treating of the test voltage and current waveforms.

A typical test circuit for pulse testing of IGCTs is shown in Figure 2-1, where  $L_i$ ,  $R_{CL}$ ,  $C_{CL}$  and  $D_{CL}$  form the  $di/dt$  limitation and clamp circuit required for the safe switching operation of the IGCT and its freewheeling diode. First the component is pressed to the rated force and heated externally to the test temperature during a certain amount of time to reach a homogeneous temperature distribution of the junction temperature. Then, the input capacitor is charged with the  $V_{DC}$  test voltage and the DUT (Device Under Test) is switched using a defined pattern until the test current  $I_{LOAD}$  and the desired switching conditions (turn-on and turn-off) are reached. Depending on the  $L_{LOAD}$  inductor value, the desired test voltage and current, the pulse test duration can last from several tens to several hundred  $\mu\text{sec}$ .

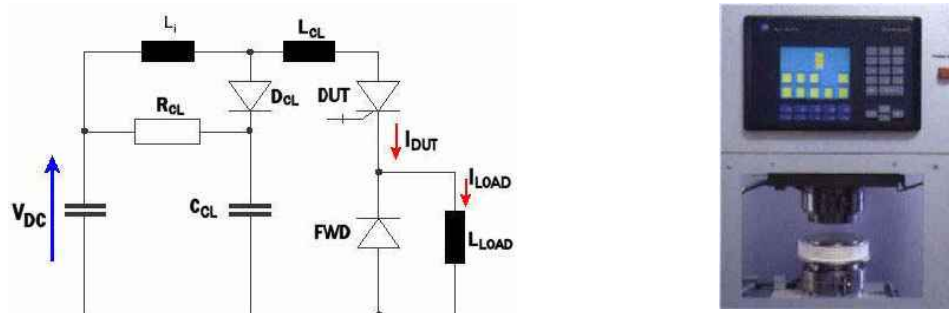


Figure 2-1.- IGCT test circuit. Pulse tester press clamping and heating system.



Depending on the desired characteristic (on state, turn-on or turn-off) and the component to be analysed (Free Wheeling Diode or IGCT), two basic pulse tests are considered, [LEM]. The single pulse test is mainly used to obtain the IGCT on-state and turn-off characteristics, Figure 2-2, whereas the double pulse test is used to obtain the IGCT turn-on and FWD turn-off characteristic, Figure 2-3.

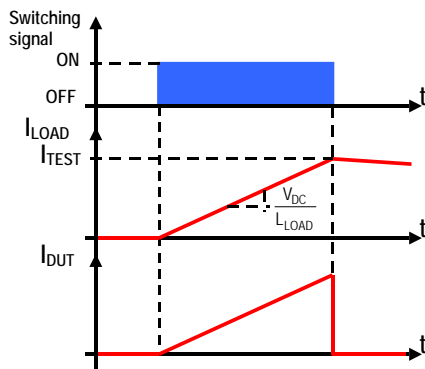


Figure 2-2.- Single pulse test pattern

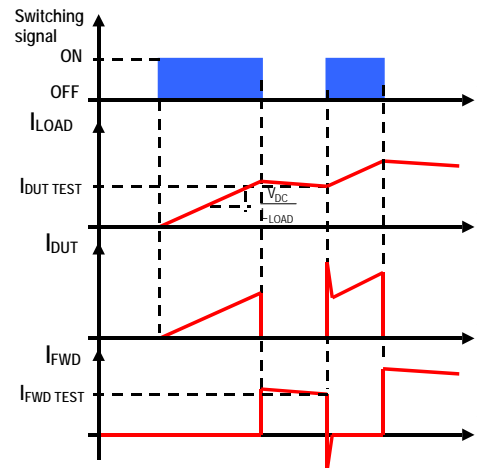


Figure 2-3.- Double pulse test pattern

To determine the on-state characteristic, the on-state current and the resulting voltage across the test device are measured. They are next represented graphically by the semiconductor  $I_T$  (on-state current) versus  $V_T$  (on-state voltage) curve. The on-state voltage is temperature sensitive and so the device thermal equilibrium should be achieved before the measurement is made. The manner in which the test device is triggered into the on-state is unimportant as long as the test current is near the rated value. The junction test temperature must always be mentioned.

Regarding the switching losses, diodes and controlled semiconductors should be characterised for the turn-on and turn-off switching transients. The parameters used for describing the switching losses ( $E_{OFF}$  and  $E_{ON}$ ) represent the energy dissipated in the device during the switching transients, they are given in joules per pulse. In the definition for the switching energy, Eq. 2-1, the instantaneous product  $v(t) \cdot i(t)$  represents the instantaneous power of the device, and times  $t_1$  and  $t_2$  define the limits of integration. The main condition to obtain an accurate evaluation of the switching losses is the use of digital systems with sampling times fast enough compared to the switching times. Also, the use of current and voltage probes with known delays that can be compensated are advisable.

$$E = \int_{t_1}^{t_2} v(t) \cdot i(t) \cdot dt \quad (\text{J}) \quad \text{Eq. 2-1}$$

When providing the switching losses defining parameters, elements and working conditions that influence their semiconductor performance need to be listed (switching voltage and current, circuit lay out, temperature, gate conditions, etc.).

## 2.2.2 Opposition Method Principle

The opposition method principle is described in [TUR-02]. This method provides good accuracy in measuring power losses for high power converters. Furthermore, the converters can be tested at

full power without using power supplies and loads adapted to their maximal ratings (even several megawatts), only the power losses of the system need to be provided by the power supply.

The principle of the opposition method consists of the use of two controllable voltage (current) sources that are linked by an inductor (capacitor). Both sources are controlled synchronously to impose the desired current (voltage) on the inductor (capacitor), Figure 2-4. Furthermore, the synchronisation control of both sources has to guarantee that the power generated by one source is going to be compensated by the other. In this way, the total power balance is reduced to the power losses on both sources and the inductor (capacitor).

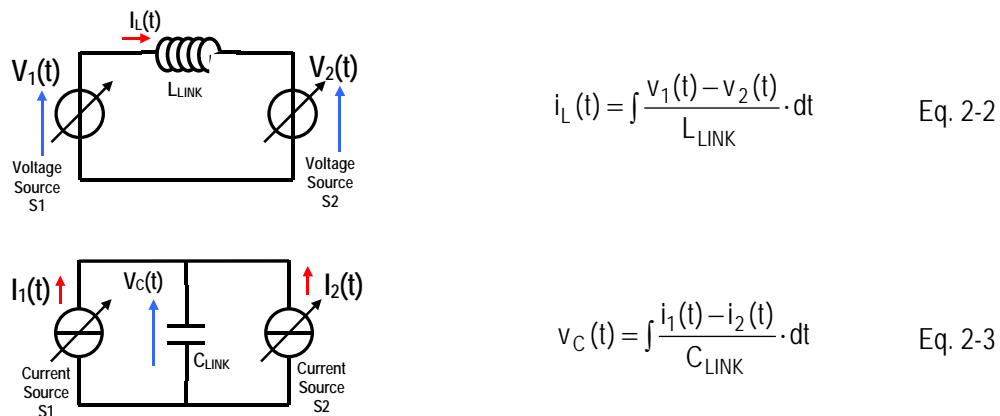


Figure 2-4.- Opposition Method operating principle

In power electronics systems, each source can be implemented by any kind of converter (from the basic switching cell to the most complicated converter), both connected to the same auxiliary power supply (DC or AC single - multi-phase), Figure 2-5. Both converters are controlled to manage the reactive power exchange generating the desired testing conditions for the converters, their semiconductors and even the link passive components (inductors and capacitors) or other auxiliary systems (cooling system, drivers, etc.). The auxiliary power supply must supply only the active power that represents the total losses of the system. Obviously, the power supply voltage rating must match with the operating conditions of the converters to be tested.

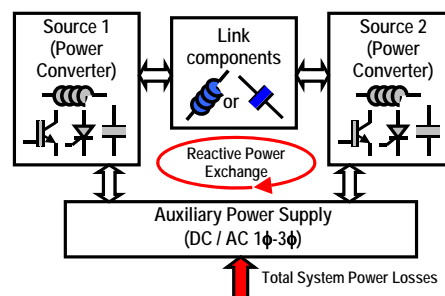


Figure 2-5.- Power converters in opposition method principle

## 2.3 Opposition Method Based Test Bench for 3.3kV IGBTs

The proposed Opposition Method test bench allows the characterisation of 3.3kV IGBTs and their associated free wheeling diodes in chopper mode operation (DC/DC conversion), [LAD-04]. The system is designed to allow the semiconductor PWM operation for switching frequencies between

500Hz and 2kHz at a constant duty cycle ( $\alpha=0.5$ ) under DC link voltages and DC output current values ranging from 500V to 1.5kV and from 0 to 2kA respectively. The input power necessary to drive the semiconductors under these working conditions is only 40kW, while the maximum controlled power is 3MW (1.5kV  $\times$  2kA). The test bench is equipped with electrical and thermal measurements systems (voltage and current probes, oscilloscopes, power analyser, temperature and flow meters) to obtain the concerned characteristics. Mainly water cooled components are utilised to minimise the size of the test bench and to get smaller thermal time constants that require lower time to reach the steady thermal state where the measurement is to be taken.

### 2.3.1 Test Bench Power Stage

The power stage of the test bench consists of two basic chopper switching cells (IGCT-Diode) arranged in the opposition configuration. The switching cells are controlled to manage the energy transfer between the input capacitor,  $C_{DC}$ , and the output inductor,  $L_s$ , Figure 2-6. A common  $di/dt$  inductor and RCD clamp circuit are used for both switching cells to limit the  $di/dt$  at turn-on and the over voltage at turn-off of the IGBTs. A fuse protects the test bench in the event of a switching cell short-circuit. In such a case, an input protection diode  $D_P$  is used to avoid the polarity change on the input power supply. The maximum ratings of the test bench are summarised in Table 2-1.

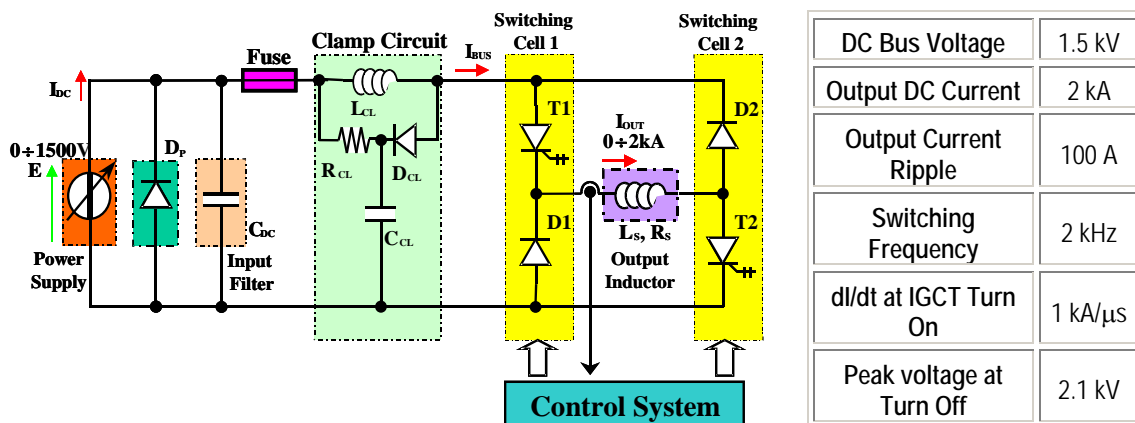


Figure 2-6.- Power stage circuit of the 3.3kV IGBTs Test Bench

Table 2-1.- Test Bench Maximum ratings

An adjustable electronic power supply is used to adjust the test DC input voltage between 0 and 1.5kV. Once the voltage is imposed, the control system is used to adjust the test output current between 0 and 2kA. The switching frequency can be also selected in the control system from 500Hz to 2kHz (500Hz, 750Hz, 1kHz, 1.25kHz, 1.5kHz, 2kHz). The  $di/dt$  circuit is designed to keep the IGBT  $di/dt$  at turn-on lower than 1kA/ $\mu$ s and the clamp-circuit to keep the maximum IGBT turn-off blocking voltage lower than 2.1kV.

### 2.3.2 Control Strategy

Applying the Opposition method principle, each switching cell is controlled independently. The first switching cell works in PWM mode controlled by the DC output current  $I_{OUT}$  control loop ( $\alpha_1 \approx 0.5$  in steady state), and the second switching cell works in open loop at constant duty cycle, ( $\alpha_2 = 0.5$ ). The gate signals of both switching cells are phase-shifted to minimise the output current ripple and the inductor value (its weight and volume). The phase shift angle between both gate signals  $\theta$  is carefully chosen to avoid the turn-on of an IGBT when the  $di/dt$  limitation inductor is still magnetised during a turn-off transient, Figure 2-7, which could lead to diode failure due to

uncontrolled  $di/dt$ . A minimum time between two switching orders must be guaranteed to provide safe operation of the semiconductors, at least two times the transient blocking time  $t_B$ . This switching pattern must be respected even during output current transients, which means that if the output current controller requires a certain duty cycle leading to simultaneous switching sequences of both switching cells (for example  $\alpha_1$  slightly lower than 0.5), a protection function must be applied to avoid this potential failure operating mode. This protection function is implemented on the modulator for both switching cells.

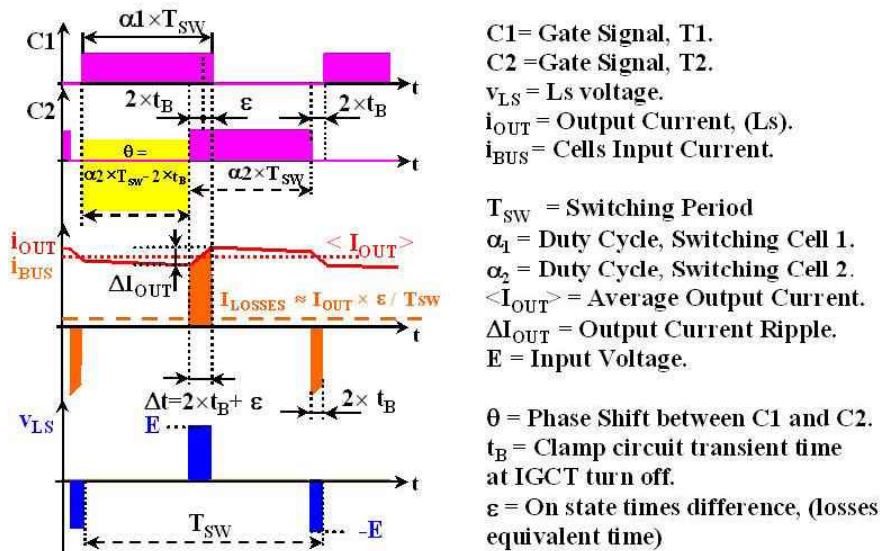


Figure 2-7.- Steady state idealised switching pattern and waveforms

Other secondary protection functions such as output over-current protection and power supply, auxiliary supplies, and cooling system monitoring are also implemented in the control system. The closed loop controller, PI type, is implemented analogically, and the PWM modulators as well as the secondary protection functions are implemented digitally on a FPGA.

### 2.3.2.1 Output current closed loop control

An analog control board containing the current ( $i_{LS}=i_{OUT}$ ) measuring interface (hall-effect current sensor output resistor), the reference generation (automatic or manual) and a PI controller (with inherent anti-windup function) is used. The duty cycle value generated by the controller is sent differentially (differential operational amplifiers) to the digital board containing A/D converters and a FPGA where the modulators for both switching cells are generated synchronously, Figure 2-8. The digital board provides the interface between the control system and the power circuit by means of fibre optic links. Optical fibre transmitters are used to send the gate signals to the IGBT drivers, and optical fibre receivers receive information about the status of the system (over-current, main and auxiliary power supply, cooling system). Start/Stop and Reset buttons are also installed on the FPGA based board to control the test bench operation.

The current measuring interface contains a high frequency filter to avoid high frequency noise generated by the semiconductors' switching transients. However, the current ripple at the switching frequency (between 500Hz and 2kHz) is not filtered. The PI generated duty cycle value ( $\alpha_1$ ) is converted into an 8-bit word at high sampling frequency piloted by the FPGA modulator (62.5kHz conversion rate for 16MHz FPGA clock speed). However, the modulator introduces a sample and hold function at the switching frequency rate to avoid uncontrolled switching frequency changes due to high frequency components on the duty cycle.

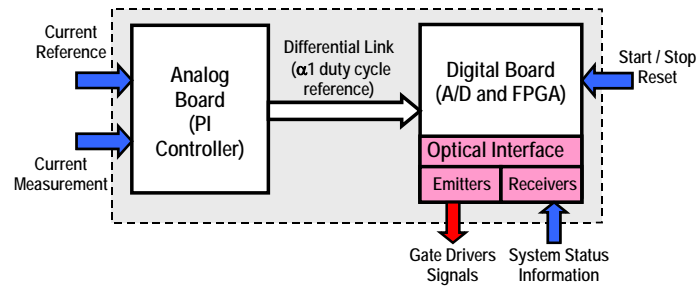


Figure 2-8.- Control System main boards

Taking into consideration all these elements, the PI controller parameters are tuned. As far as the voltage generated by the second switching cell can be considered as a constant perturbation with low influence over the steady state behaviour of the current control, the linear system model can be simplified to a pure inductor (the resistive term neglected). The modulator gain and delay as well as the current sensor gain are also considered in the model, Figure 2-9.

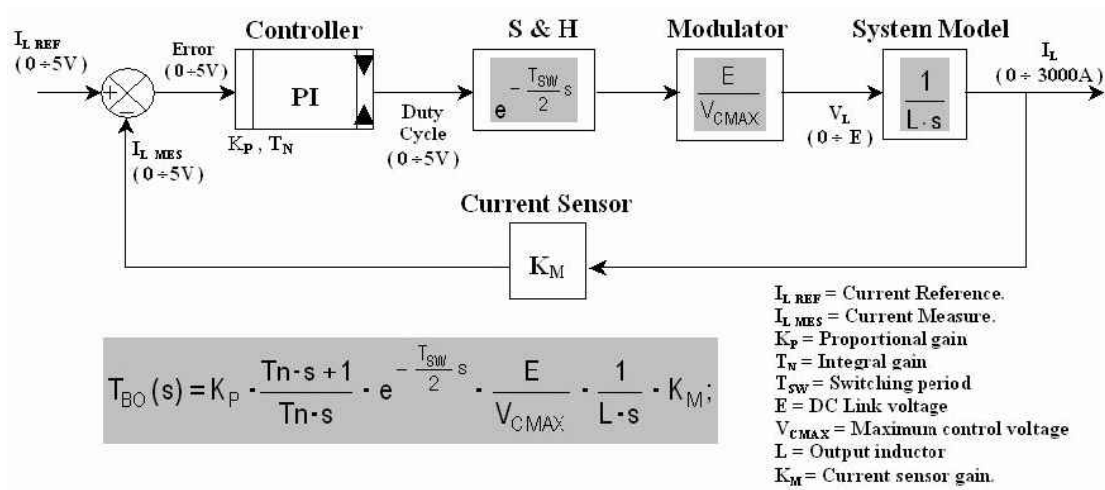


Figure 2-9.- Output current control loop linear model and open loop transfer function

The dynamic performance of the controller is not the main issue in this case because the system is intended for testing the components in steady state operation (DC operation). Thus, the controller parameters selection method can be mainly defined to guarantee stable operation and small steady state error of the control loop.

As the input voltage and switching frequency can vary depending on the test conditions, the proposed tuning strategy consists of the imposition of a margin phase big enough to guarantee stable operation for a given switching frequency in the whole voltage range (100V to 1.5kV). Under these conditions, if the controller parameters are kept constant, the controller bandwidth and phase margin change, which can be acceptable for this application. The adopted solution defines the controller parameters to obtain a 60° phase margin when the input voltage is E=750V and the cut-off frequency  $f_c$  is fixed to a value 10 times lower than the switching frequency  $f_{SW}$ . For the intended voltage range, the margin phase of the system is checked. The selected parameters are accepted if the worst phase margin value (lower input voltage) is above 35°. Figure 2-10 shows the Bode plot of the open loop transfer function at 500Hz under different input voltage levels.

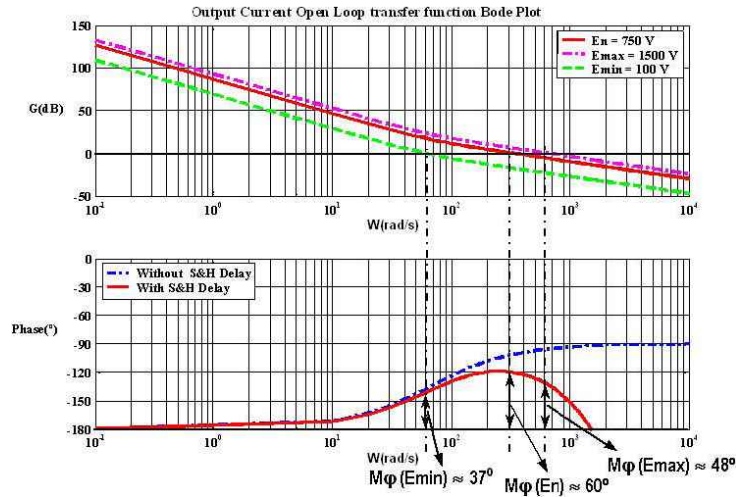


Figure 2-10.- Output current open loop transfer function Bode Plot ( E=100V, 750V, 1.5kV, f<sub>SW</sub>=500Hz)

For each switching frequency, change of the controller parameters (proportional K<sub>P</sub> and integral T<sub>N</sub>) is required according to the equations Eq. 2-4 and Eq. 2-5.

$$M\phi = 180^\circ + \angle T_{BO} |_{\omega_c} = \text{arc tag} \left( T_N \cdot \omega_c \right) - \frac{T_{SW}}{2} \cdot \omega_c; \Rightarrow T_N = \frac{\text{tag} \left( M\phi + \frac{f_c \cdot 180}{f_{SW}} \right)}{2 \cdot \pi \cdot f_c} \quad \text{Eq. 2-4}$$

$$|T_{BO} |_{\omega_c} = 1 = \frac{K_P}{L \cdot \omega_c} \cdot \frac{E}{V_{C_{MAX}}} \cdot K_M; \Rightarrow K_P = \frac{L \cdot \omega_c \cdot V_{C_{MAX}}}{E \cdot K_M} \quad \text{Eq. 2-5}$$

Mφ = Phase Margin (degrees)  
 f<sub>c</sub> = Cut-off frequency  
 f<sub>SW</sub> = Switching frequency

∠T<sub>BO</sub> = Open loop transfer function phase  
 |T<sub>BO</sub>| = Open loop transfer function gain

Table 2-2 show the selected controller parameters and the corresponding performances of the controller (bandwidth and phase margin) for 3 different switching frequencies depending on the DC link voltage value.

Switching frequency and Controller parameters	DC Link Voltage, E (V)	Phase Margin, Mφ (°)	Bandwidth, f <sub>c</sub> (Hz)
f <sub>SW</sub> = 500Hz K <sub>P</sub> = 0.502 T <sub>N</sub> = 14.97e <sup>-3</sup>	100	37	9.5
	750	60	50
	1500	48	100
f <sub>SW</sub> = 1kHz K <sub>P</sub> = 1.005 T <sub>N</sub> = 7.485e <sup>-3</sup>	100	37	21
	750	60	100
	1500	48	200
f <sub>SW</sub> = 2kHz K <sub>P</sub> = 2.01 T <sub>N</sub> = 3.743e <sup>-3</sup>	100	37	39
	750	60	200
	1500	48	400

Table 2-2.- Controller parameters and expected performances for different working conditions

Several non-linear compartments of the system are not considered when tuning the controller parameters (clamp circuit influence, modulator actuation for safe switching operation,  $t_B$  blocking transient time imposition). However, they have been introduced in transient simulations where the behaviour of the whole systems has shown stable operation. Figure 2-11 shows the stable current loop response under the most unfavourable voltage condition ( $E=100V$ ,  $M\phi = 37^\circ$ ) when the switching frequency is selected to be 500 Hz. At the beginning of the simulation it can be understood that there is no current on the output inductor because the duty cycle is so small that no energy is transferred to it. Once the controlled duty cycle  $\alpha_1$  is bigger than the constant duty cycle  $\alpha_2$ , energy starts flowing to the output inductor and the desired current can be established.

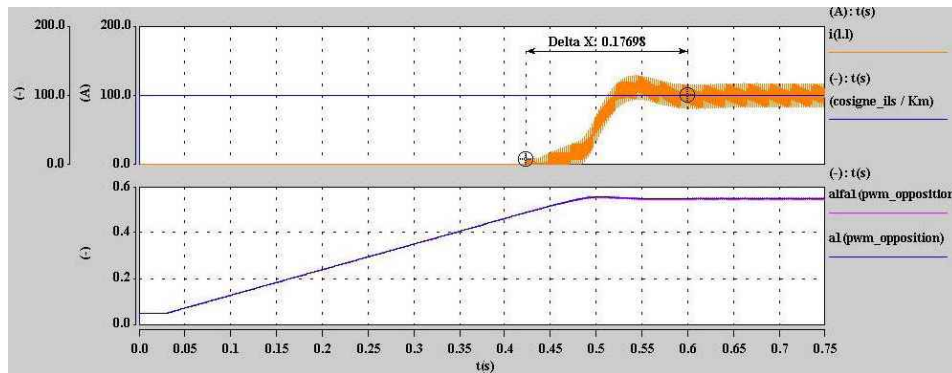


Figure 2-11.- Control system transient response ( $E=100V$ ,  $f_{SW}=500Hz$ ,  $I_{LREF}=100A$ )

### 2.3.2.2 FPGA functions

Several functions are implemented digitally on the FPGA board, from the modulator implementation to the state machine that controls the operation modes of the test bench. These functions are programmed in VHDL language and arranged in blocks (subprograms) that are then interconnected to build the full control program of the test bench as described in Figure 2-12. The functions of these subprograms are briefly explained in this section.

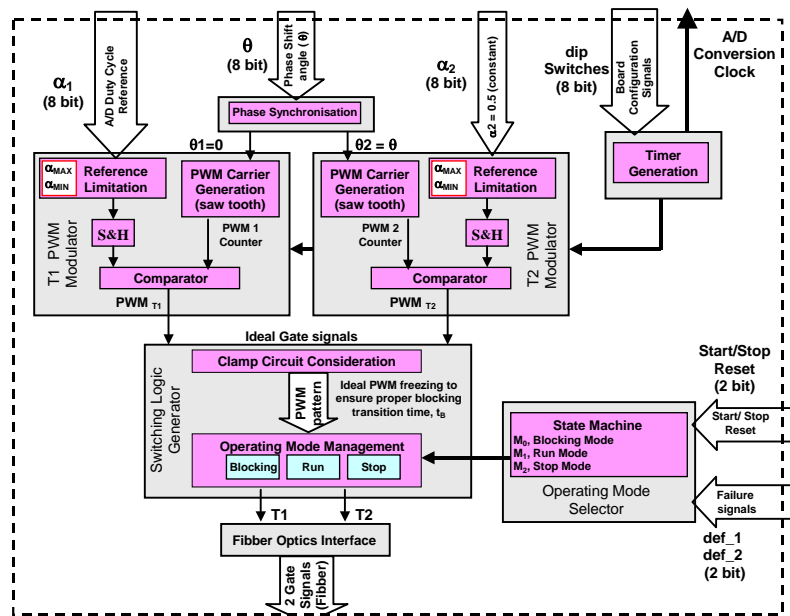


Figure 2-12.- FPGA program functional overview

### 2.3.2.2.1 PWM modulator

The PWM modulator is responsible of the ideal PWM pattern generation by comparing the duty cycle reference with the PWM carrier (saw tooth type). Also reference limitation and S&H functions in synchronism with the zero crossing of the PWM carrier are provided, which avoids measurement perturbation effects on the control loop due to commutation transitions. The switching frequency and other time dependent parameters (phase shift angle, blocking transient time generation, etc), can be selected by means of dip-switches. The most important quantities that can be directly affected with the selection of dip-switches are the switching frequency, the maximum and minimum on-state times, the phase shift angle between gate signals and the blocking transient time (ideal PWM pattern freezing time) that takes into account the existence of the clamp circuit.

### 2.3.2.2.2 Switching logic generator

The switching logic generator defines the correct switching sequence depending on the operation mode of the test bench (Blocking, Run, Stop) and the ideal PWM pattern for both switching cells. The first function that this block implements is the freezing of the ideal PWM pattern generated previously when an IGBT blocking signal arrives. The first signal takes action but the other gate signal remains frozen for a defined period of time that guarantee the end of the blocking transition on the clamp circuit, thus providing safe switching operation of the semiconductors.

The other main function of these elements is the management of the gate signals generation when the test bench changes from one operation mode to the other defined by the state machine that controls the operation of the test bench.

### 2.3.2.2.3 Operating mode selector (state machine)

The semiconductors of the test bench can be driven into three different operation modes ( $M_0$ ,  $M_1$ ,  $M_2$ ). A state machine is utilised to manage how the test bench move from one to another, Figure 2-13.

- $M_0$ , Blocking Mode: In this operating mode, all semiconductors are in the blocking state. From this operation mode (state 0), the Run Mode can be reached if the Start/Stop switch generates a start order (leading edge). To avoid sending signals to the IGBTs gate drivers during the power up of the control system, the Start/Stop switch has to be kept for a defined minimum time ( $t_{ON}$ ) on the Stop position, otherwise the state machine goes into a never ending loop (state 6) which requires the power down of the control system.
- $M_1$ , Run Mode: The IGBTs are controlled in PWM operation, with the first switching cell piloted from the analog control board, and the second switching cell working with constant duty cycle,  $\alpha_2=0.5$ . Also, a fixed phase shift angle between both gate signals is applied (close to half the switching period) which allows minimising the output current ripple.
- $M_2$ , Stop Mode: In this operating mode, a freewheeling sequence is generated to discharge safely the energy stored in the output inductor. Depending on the switching sequence previous to the Stop order, the free wheeling sequence is reached in a single commutation with either the upper or the lower switches, IGBT-Diode. Access to the Stop Mode can be accomplished by a normal operation stop order (lagging edge on the Start/Stop switch) or due to a fault signal generated because of output over current, power supply failure (main or auxiliary) or cooling system failure. All these faults are collected, coded and sent by a third control board (protection board)



to the FPGA control board by means of two fiber optic links, def\_2 and def\_1 (2 bit code). The test bench operation mode and error status are displayed by means of several LEDs as defined in Table 2-3.

def_2	def_1	Operating Mode	Lighting LED
1	1	Run Mode	GREEN
0	1	Output over current	RED 1
1	0	Power Supply failure (main or auxiliary supply)	RED 2
0	0	Cooling system failure	RED 3

Table 2-3.- Protection Board signals meaning

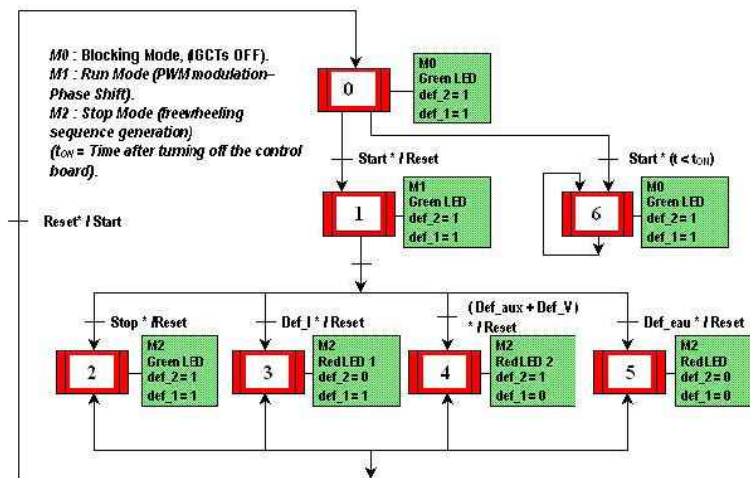


Figure 2-13.- Test bench control system state machine

### 2.3.3 Component Dimensioning

When applying the Opposition Method principle, the steady state working conditions and maximum current and voltage ratings of the components are mainly defined by the total power losses of the system. In the proposed 3.3kV IGBT characterisation test bench, as shown in Figure 2-7, the steady state duty cycle of the first switching cell,  $\alpha_1$ , is slightly higher than the constant duty cycle of the second switching cell ( $\alpha_2=0.5$ ). The difference between the on-state times of both switching cells ( $\varepsilon=(\alpha_1-\alpha_2)\times T_{SW}$ ) is only dependent on the active power that has to be supplied by the input power supply, that is the total power losses of the converter, Eq. 2-6. For this reason, the definition of the values and ratings of the components employed in the test bench (mainly passive components) need the previous estimation of the total power losses. For the components that have to be characterised (IGBTs and Diodes), the projected semiconductors data presented in [BAS-02] are used. For the other components, approximate data extrapolated from similar available components or empirical approximations are employed.

$$\text{Power Losses} = \frac{E \cdot I_{OUT} \cdot \varepsilon}{T_{SW}} \quad \text{Eq. 2-6}$$

Once the operation conditions and values of the components are defined through the total power losses estimation, simulation assisted dimensioning for the main components is performed.

### 2.3.3.1 Test bench power losses estimation

Before evaluating the total losses of the test bench, the proper semiconductor switching conditions need to be guaranteed. Considering the test bench working conditions and the switching condition limits of the 3.3kV IGCTs and their freewheeling diodes, the selection of the  $di/dt$  inductor and RCD clamp circuit components values are selected, Table 2-4 (see 1.3.1.3  $di/dt$  limitation, clamp circuit) and checked by simulation, Figure 2-14.

$E_{MAX}$ , maximum DC Link Voltage	1.5kV	$L_{CL MIN} = 1.5 \mu H$
$di/dt_{MAX}$ , maximum $di/dt$ at IGCTs turn on	1 kA/ $\mu s$	
$\Delta V_{CL MAX}$ , maximum semiconductors voltage overshoot	650V	$C_{CL} = 6 \mu F$
$t_{B MAX}$ , maximum blocking transition time	6.1 $\mu s$	$R_{CL} = 0.75 \Omega$

Table 2-4.- Components values of the  $di/dt$  inductor and RCD clamp circuit

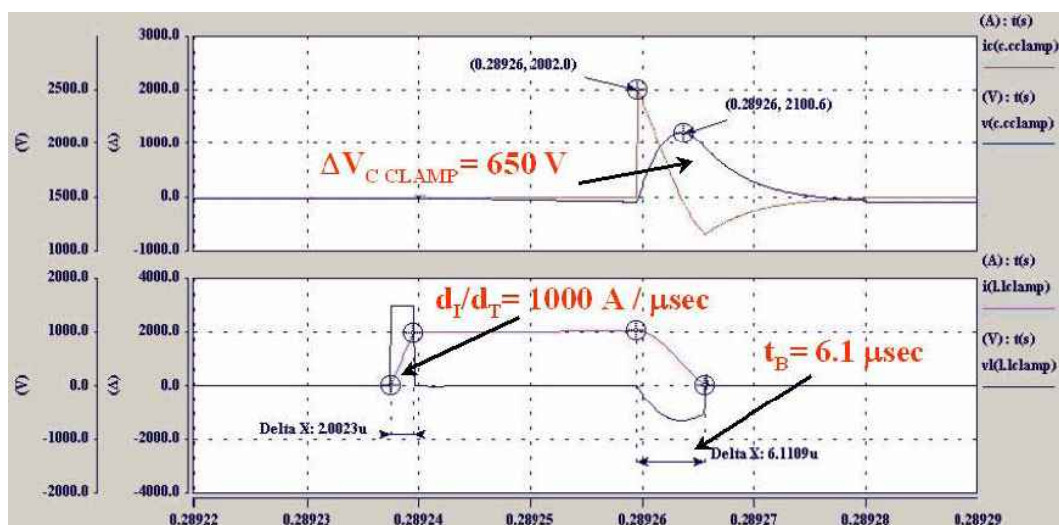


Figure 2-14.-  $di/dt$  inductor and RCD clamp circuit maximum operating conditions

With these values already fixed, the evaluation of the test bench total losses is performed, Table 2-5. The power losses are evaluated at the maximum test bench output current and DC link voltage ratings (2kA, 1.5kV) for three switching frequencies (500Hz, 1kHz and 2kHz). Three main power losses sources are considered in the estimation process,

- Semiconductors, (switching cells IGCTs and Diodes): On state losses and switching losses are evaluated taking into account the expected output current ripple,  $\Delta I_{LS MAX} = 100A$ , and a maximum duty cycle difference between both switching cells ( $\alpha_1 - \alpha_2$ ) lower than 0.025.
- Clamp resistor,  $R_{CL}$ : the energy stored on the clamp inductor  $L_{CL}$  is supposed to be evacuated completely over the clamp resistor. The frequency rate is twice the switching frequency (2 switching cells). The maximum output current (current ripple effect) is considered in the clamp resistor power losses evaluation.
- Output inductor parasitic resistor,  $R_s$ : The Joule effect power losses on the output inductor are taken into account. The parasitic resistor value is estimated to be around  $R_s = 1.25 m\Omega$ .

$I_{LS} = 2\text{kA}, E = 1.5\text{kV}, \Delta I_{LS} = 100\text{A}$				
$f_{sw}$		500Hz	1000Hz	2000Hz
IGCT 1 $\alpha 1 = 0.525$	On state	1712 W	1712 W	1712W
	Switching	1250 W	2500 W	5000 W
Diode 1 $1-\alpha 1 = 0.475$	On state	1862 W	1862 W	1862 W
	Switching	840 W	1680 W	3360 W
IGCT 2 $\alpha 2 = 0.5$	On state	1630 W	1630 W	1630 W
	Switching	1250 W	2500 W	5000 W
Diode 2 $1-\alpha 2 = 0.5$	On state	1960 W	1960 W	1960 W
	Switching	840 W	1680 W	3360 W
Semiconductor Total Losses	On state	7164W	7164W	7164W
	Switching	4180 W	8360 W	16720 W
	Total	11344W	15524W	23884W
CLAMP Losses ( $L_{CL} \cdot I_{LS \text{ MAX}}^2 \cdot f_{sw}$ )		3152W	6304W	12608 W
Output Inductor ( $R_s \cdot I_{LS \text{ DC}}^2$ )		5000 W	5000 W	5000 W
Total Losses		19496 W	26828 W	41492 W

Table 2-5.- Test bench power losses estimation

The estimation of power losses helps to define the power requirements of the input power supply, but also allows establishing the on state time difference between both switching cells  $\varepsilon$ , Eq. 2-6, which will be required for the definition of the test bench components. Table 2-6 shows the  $\varepsilon$  values for the three switching frequencies considered.

	$f_{sw} = 500\text{Hz}$	$f_{sw} = 1000\text{Hz}$	$f_{sw} = 2000\text{Hz}$
$\varepsilon = \frac{\text{Power Losses}}{E \cdot I_{OUT}} T_{SW}$	13 $\mu\text{s}$	8.94 $\mu\text{s}$	6.92 $\mu\text{s}$

Table 2-6.- On state time difference between switching cell 1 and 2

### 2.3.3.2 Output inductor, $L_s$

The use of a phase shift angle  $\theta$  between the gate signals of the switching cell 1 and 2 allows the minimisation of the output inductor value,  $L_s$ , which implies the minimisation of its weight and volume. However, the value of  $\theta$  is restricted by the existence of a single  $di/dt$  inductor and RCD clamp circuit for both switching cells. In steady state operation  $\theta$  is fixed to guarantee a minimum time between two consecutive switching transitions, at least twice the clamp imposed maximum blocking transition time, ( $2 \cdot t_{B \text{ MAX}}$ ) Eq. 2-7. Furthermore, for the safe operation of semiconductors in transient conditions, the modulator is designed to freeze the adjacent gate signals at each switching transition order to guarantee this minimum time between two successive commutations.

Under these operation restrictions, and imposing a maximum current ripple at the switching frequency lower than 5% of the maximum DC output current ( $\Delta I_{LS \text{ MAX}} \leq 100\text{A}$ ), the output inductor value is defined. The maximum input voltage pulse width  $\Delta t_{\text{MAX}}$  applied to the inductor when the input voltage is maximum and the current ripple limit impose the minimum value of  $L_s$ . The

maximum pulse width is subordinated to  $\varepsilon$ , Eq. 2-8, and occurs when the switching frequency is 500 Hz. Such considerations lead to an inductor value bigger than 382.5  $\mu\text{H}$ , Eq. 2-9.

$$\theta = \alpha_2 - 2 \cdot t_{B \text{ MAX}} \quad \text{Eq. 2-7}$$

$$\Delta t_{\text{MAX}} = \varepsilon_{\text{MAX}} + 2 \cdot t_{B \text{ MAX}} \quad \text{Eq. 2-8}$$

$$L_{S \text{ MIN}} > \frac{E_{\text{MAX}} \cdot \Delta t_{\text{MAX}}}{\Delta I_{L S \text{ MAX}}} = 382.5 \mu\text{H} \quad \text{Eq. 2-9}$$

Transient simulations help to define the output inductor dimensioning voltage and current ratings, Table 2-7. Special attention has to be paid to the voltage across the inductor. In Figure 2-15 it can be seen how the maximum voltage over the inductor is higher than the DC link input voltage due to the effect RCD clamp circuit, which has to be taken into account when defining the insulation properties of the component. Finally an  $L_S=400\mu\text{H}$  output inductor is specified and a water-cooled custom design solution is selected ( $L_S=400\mu\text{H} / 2\text{kA}$ , 450kg, 650mm  $\times$  500mm  $\times$  900mm, Boige & Vignal S.A.).

F <sub>SW</sub> = 500 Hz $\div$ 2000 Hz						
Component	I <sub>MAX</sub>	I <sub>RMS</sub>	I <sub>AV</sub>	$\Delta I$	$\Delta V$	V <sub>MAX</sub>
L <sub>S</sub> = 400 $\mu\text{H}$	2050 A	2000 A	2000A	100A	2200V	$\pm 2200\text{V}$

Table 2-7.- Output inductor dimensioning parameters

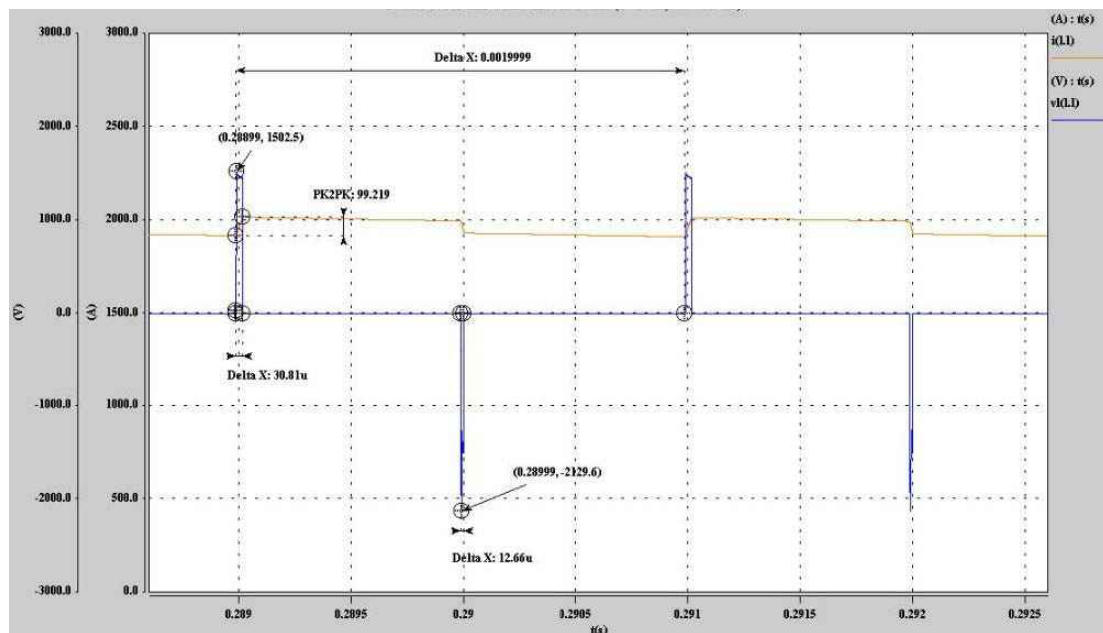


Figure 2-15.- Output inductor voltage and current steady state waveforms ( $E=1.5\text{kV}$ ,  $f_{\text{SW}}=500\text{Hz}$ )

### 2.3.3.3 Input capacitor, C<sub>DC</sub>

The value of the input capacitor is imposed by the maximum input voltage pulse width applied to the output inductor  $\Delta t_{\text{MAX}}$ , which also represents the maximum pulse width of the maximum output current circulating through the input capacitor. This consideration, together with the

maximum admissible switching frequency voltage ripple limited to less than 5% of the maximum input voltage ( $\Delta V_{C_{DC}} < 75V$ ), imposes the minimum value of the input capacitor, Eq. 2-10.

$$C_{DC\ MIN} > \frac{I_{OUT\ MAX} \cdot \Delta t_{MAX}}{\Delta V_{C_{DC}\ MAX}} = 680\mu F \tag{Eq. 2-10}$$

Regarding the current ratings of the capacitor, not only the RMS and peak current values are required. Also, the current spectrum is used by the capacitors manufacturer to determine the total dissipation of the component and its ability to withstand the working conditions. Figure 2-16 shows the capacitor steady state current and voltage waveforms as well as the capacitor current spectrum for the maximum DC output current (2kA) at 2kHz. The maximum peak current that the capacitor has to withstand is greater than the output current due to the effects of the clamp circuit.

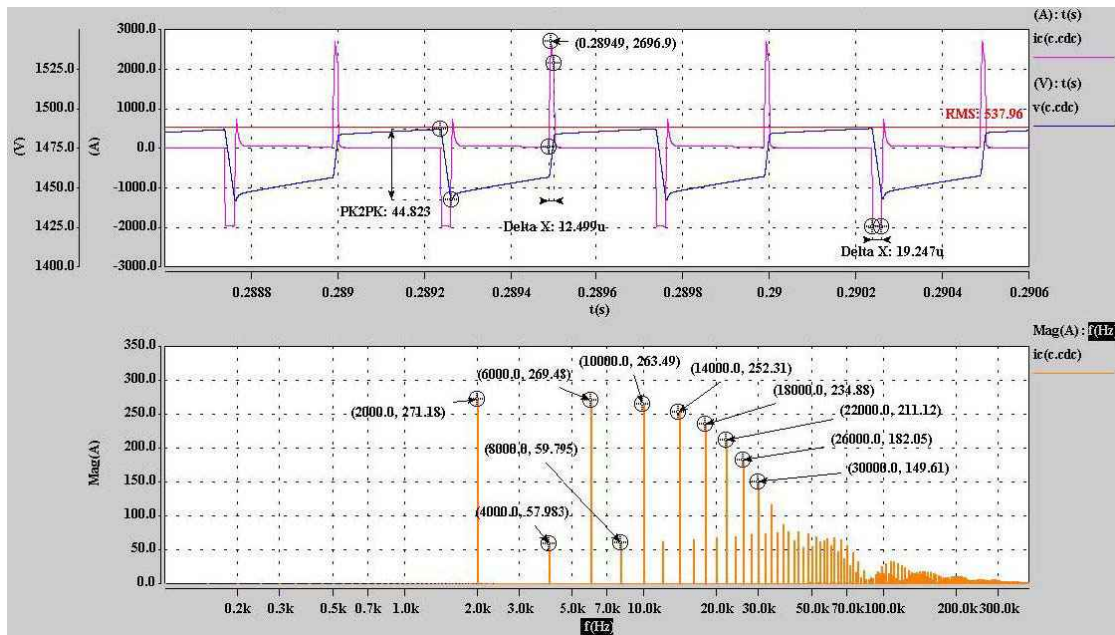


Figure 2-16.- Input capacitor steady state current and voltage waveforms ( $E=1.5kV$ ,  $I_{OUT}=2kHz$ ,  $f_{SW}=2kHz$ ). Capacitor current spectrum

The capacitor dimensioning parameters are given in Table 2-8. A commercially available  $3000\mu F / 600A_{RMS} / 2150V_{DC}$  capacitor (TRAFIM DKFTM266B3007, AVX) is finally utilised.

F <sub>SW</sub> = 500 Hz ÷ 2000 Hz						
Component	I <sub>MAX</sub>	I <sub>RMS</sub>	I <sub>AV</sub>	ΔI	ΔV	V <sub>MAX</sub>
C <sub>DC</sub> = 1000μF	2700 A	540 A	0 A	2700A	50V	1600 V

Table 2-8.- Input capacitor dimensioning parameters

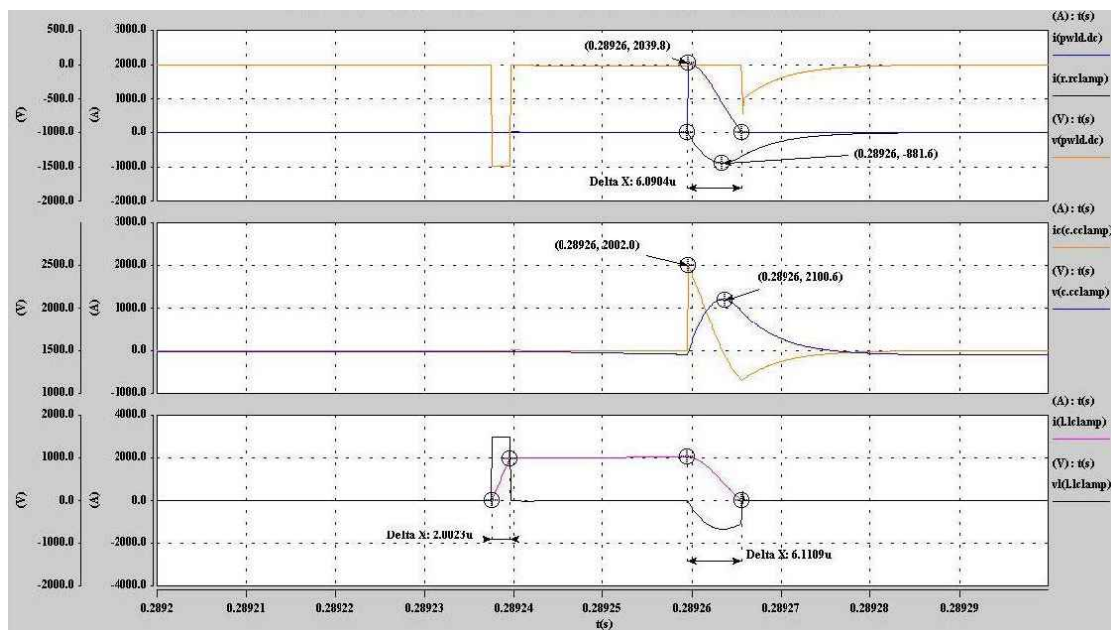
### 2.3.3.4 di/dt inductor and RCD clamp circuit components

The di/dt inductor and RCD clamp circuit components values being already selected, the dimensioning ratings in terms of voltage and current are obtained using idealised simulations. Table 2-9 summarises the dimensioning parameters for these components.

F <sub>SW</sub> = 500 Hz ÷ 2000 Hz						
Component	I <sub>MAX</sub>	I <sub>RMS</sub>	I <sub>AV</sub>	ΔI	ΔV	V <sub>MAX</sub>
L <sub>CL</sub> = 1.5μH	2050 A	510 A	60 A	2050 A	1600 V	1600 V
C <sub>CL</sub> = 6μF	2050 A	165 A	0 A	2050 A	650 V	2200 V
R <sub>CL</sub> = 0.75Ω	890 A	128 A	30 A	890 A	660V	660 V
D <sub>CL</sub>	2050 A	210 A	30 A	2050 A	1500 V	1500 V

Table 2-9.- di/dt inductor and clamp circuit components dimensioning parameters

Figure 2-17 shows the simulated waveforms (ideal components) for the di/dt inductor and RCD clamp circuit at maximum output current and input voltage for 2kHz operation.

Figure 2-17.- di/dt inductor and RCD clamp circuit waveforms (E=1.5kV, I<sub>OUT</sub>=2kHz, f<sub>SW</sub>=2kHz)

Except for the clamp diode (5SDF 03D4502, ABB), the components specifications impose the use of custom designed components or association of existing components. For the clamp inductor, an air-cored solution is preferred to avoid the change on the inductance value. A custom design solution is selected (1.7μH, 600A<sub>RMS</sub>, 150mm × 150mm × 305mm, Boige and Vignal). Regarding the clamp capacitor, three low inductive capacitors (2μF) with axial connections in parallel are used, (FPG86X0205J, AVX). Due to the high power dissipation of the clamp resistor (12.6kW), an arrangement of 24 non-inductive resistors in parallel (UXP600-18Ω / 600W, EBG) distributed over 3 water-cooled heatsinks (AAVID Thermalloy custom design) is adopted. Bus bar connections are used to minimise the parasitic inductance of the parallel arrangement. The interconnection between all these elements is carefully defined to minimise the switching path unclamped parasitic inductor and thus the voltage spike over the switching cell semiconductors.

### 2.3.4 Test Bench Lay-out

The disposition of the test bench components is selected to provide good access to the platform for the required measurements (electrical and thermal) and flexibility in the mounting and dismounting process of the component in case of necessity (failure, replacement of components). Also, special attention is paid to the semiconductor main switching loops, applying low inductive

bus bars where possible. Due to the high current values that are handled, some flexible current connections are provided to avoid mechanical stress over the semiconductors mechanical arrangements induced by thermal expansion. Also high surface contacts with several connecting points are utilised to provide good electric contact.

Regarding protection issues, besides the active protection functions implemented by the control system, the required electrical and mechanical protection means are provided. Electrically, the chassis of all the components are connected to the protection earth when they are not under voltage (output inductor, input capacitor, power supply, etc). If they are under voltage, the required insulation according to the voltage level is provided (water tubes length, bus bar isolation, mechanical clamps supporting base, etc). Also, when the test bench is not operative, the input capacitor is short-circuited by means of a discharging circuit to avoid dangerous remaining voltages on the test bench.

Mechanically, all the power stage components except the output inductor are installed on a chassis. This chassis is equipped with transparent polycarbonate plates for protecting people against any projected particles and allows visual supervision of the components. Also, isolated mechanical barriers are positioned between the control desk and the test bench to guarantee people safe insulation.

The test bench is equipped with the electrical and thermal probes and equipments required to accomplish the characterisation of the components. Figure 2-18 shows the general overview of the developed test bench. Other relevant details concerning different aspects of the test bench layout are shown in the following paragraphs.

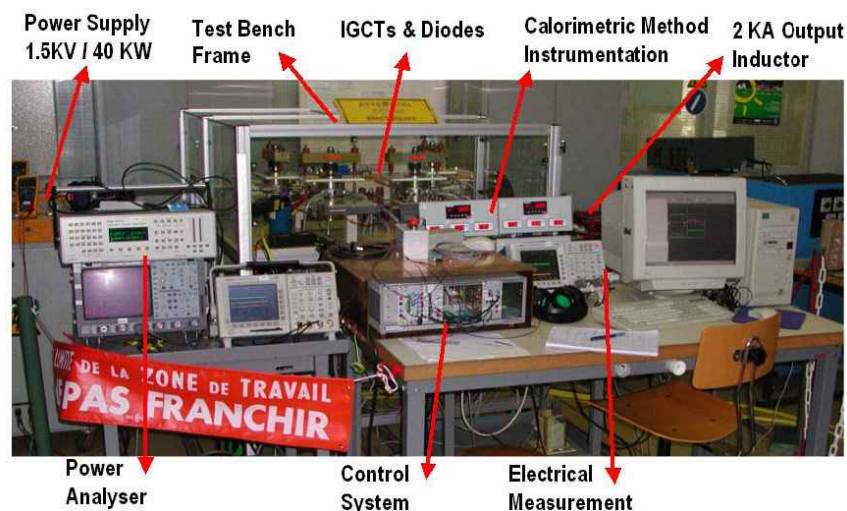


Figure 2-18.- 3.3kV IGCT characterisation test bench overview

### 2.3.4.1 Power stage components

The main feature of the test bench layout is the arrangement of the power semiconductors. In contrast to the classical stacked assembly of press pack components, here each semiconductor is fitted into an independent mechanical clamp with the required heat-sinks (ABB) and hardened steel made force spreaders, Figure 2-19. This disposition provides high flexibility degree for mounting and dismantling the semiconductors in case of failure and avoids thermal interaction between components, which guarantees well defined thermal measurements. Furthermore, this kind of layout allows the use of low inductive bus-bars to minimise the parasitic inductance of the switching path between the power semiconductors and the clamp circuit components.

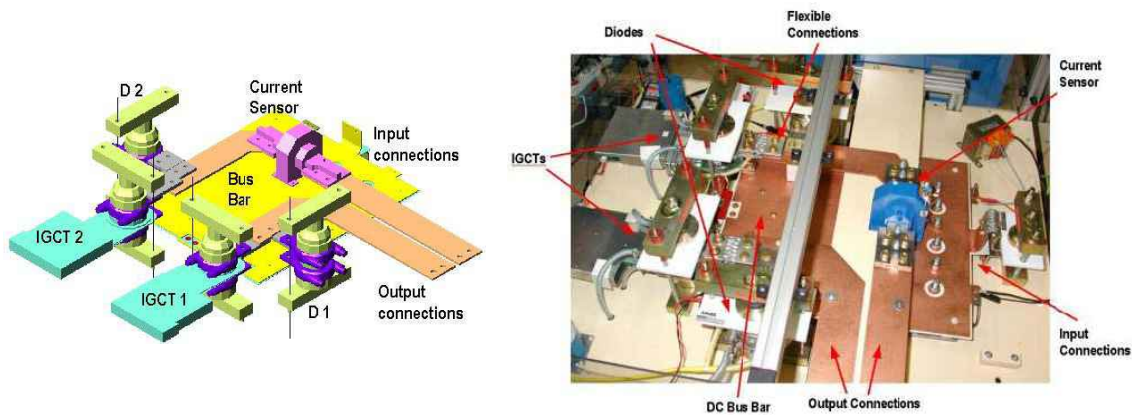


Figure 2-19.- Semiconductors arrangement for thermal and mechanical isolation

The main power circuit bus bar is divided in three plates. A top plate provides the connection between the switching cells semiconductors and the negative terminals of the input capacitor and clamp capacitor. An intermediate plate connects the positive terminal of the input capacitor to the protection fuses (two paralleled 400A<sub>RMS</sub> semiconductor protective fuses with lower I<sup>2</sup>t level than the used IGBTs and freewheeling diodes, 15URK93TTF0400, FERRAZ-SHAWMUT). A second bottom plate distributes the connections between the switching cell semiconductors, the di/dt inductor and the clamp diode, Figure 2-20. The required isolation between the top and bottom plates is guaranteed by two high insulating Nomex sheets (2x0.38mm). Additional plates are used to interconnect the clamp capacitor, the clamp diode and the clamp resistor. The input protection diode (5SDD51L2800, ABB), also mounted into an independent mechanical clamp but without heat-sinks, is connected to the bus bar input connections by flexible braids.

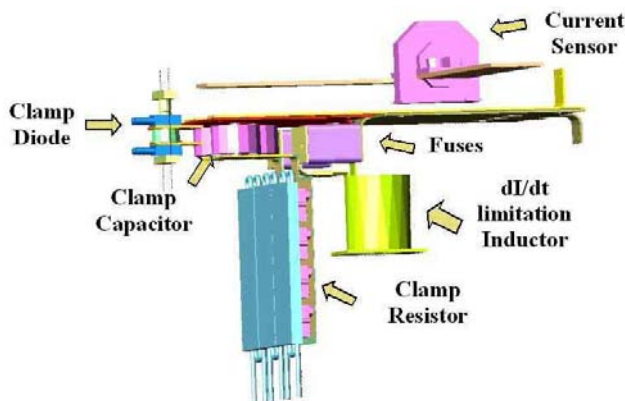


Figure 2-20.- Fuses, di/dt and RCD clamp components disposition view



Figure 2-21.- Custom designed di/dt inductor

The connections to the switching cell middle points are ensured by flexible braids (400mm<sup>2</sup> - 1000A, ERICO). Then, copper plates are used to connect the Hall Effect current transducer (LT2005-T/SP20, LEM) and to provide access to the power stage output connections. Connection between the power stage and the output inductor terminals is achieved by several flexible cables in parallel, Figure 2-23.

All the components, except the output inductor, are arranged on a wheeled aluminium profile based chassis (45mmx45mm, REXROTH BOSCH), Figure 2-22. Several insulating plates (PVC) are employed to position and to provide the required insulation for different elements (output connections, mechanical clamps, gate drivers and their power supplies (SW32-24A30G,



Ingenieurbüro Siebel), etc. The total supported weight is around 200kg. Also, the cooling circuit piping distribution is placed at the bottom side of the chassis, below the power semiconductors.

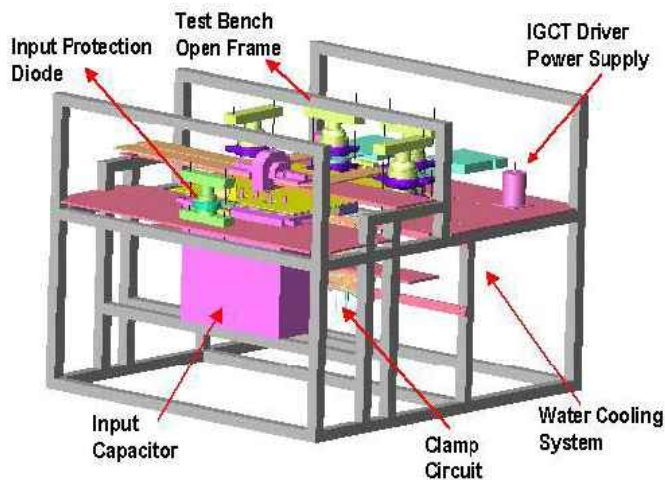
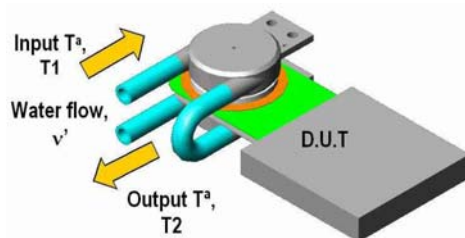


Figure 2-22.- Test bench mechanical assembly arrangement      Figure 2-23.- Output inductor disposition.

### 2.3.4.2 Water cooling system

Several water circuits are used to cool the different components of the test bench (power semiconductors, output inductor, clamp resistor) and also to assess the total power losses in each component by using the calorimetric method [BRO-96], Figure 2-24. To apply this method, several temperature and water flow measurements are integrated in the cooling systems.



$$P_{TOT\_X} = C_P \times \rho \times v' \times \Delta T$$

$P_{TOT\_X}$  = Total losses per component.

$\Delta T = T_1 - T_2$  (°C) (input – output  $T^a$  change).

$C_P$  = water specific heat - 4186 J/(Kg °C).

$\rho$  = water density (1Kg/ l).

$v'$  = Water flow (l/sec).

Eq. 2-11

Figure 2-24.- Power losses evaluation calorimetric principle

The switching cells semiconductors cooling circuit is shown in Figure 2-25. This circuit is divided into two branches, each one cooling the semiconductors of one switching cell. Each branch is equipped with a rotating-vane flow meter (DPL-060, Kobold), associated to a Counter/Rate Meter (PAXI 0010, Red Lion Control) and 3 high electric insulating PT100 temperature probes (CT22389, ManoThermo) together with their thermo-meters (EC3-161P012, Every Control). These components allow measuring the water temperature change associated with the losses of each semiconductor and the water flow rate of the branch, which are required to evaluate the total power losses of each component. Due to the pressure drop in the heatsinks ( $\Delta p = 2$  bar at 4 l/min), a water pump and their associated elements (water pump drive, reservoir, pressure gauge, etc.) are installed to increase the water pressure on the circuit and to obtain the desired flow rate (4 l/min maximum). Each branch is also equipped with a valve used to adjust the flow rate on the circuit. The cooling circuit of the output inductor and clamp circuit components is simpler but follows the same cooling structure Figure 2-26. However, to keep the components within their thermal limits (clamp resistors) higher flow rates are required (16 l/min) and therefore the flow meter range has to be adapted (DPL-250 Kobold).

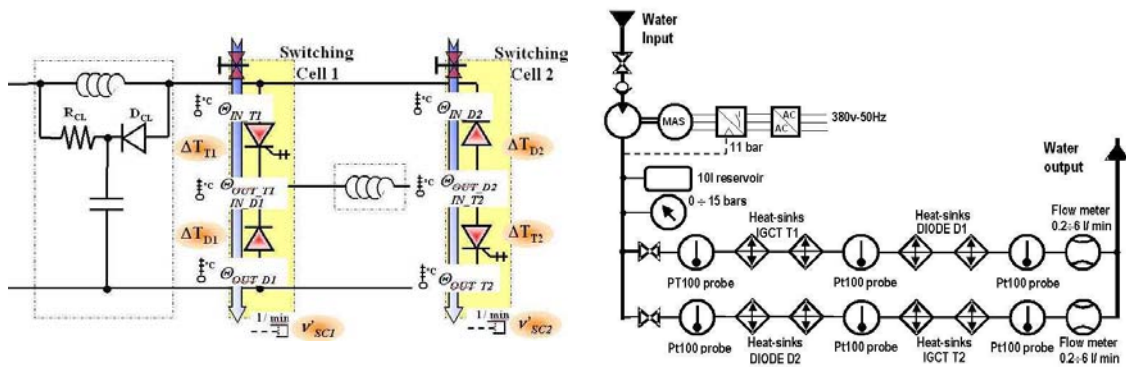


Figure 2-25.- Switching cell cooling circuit

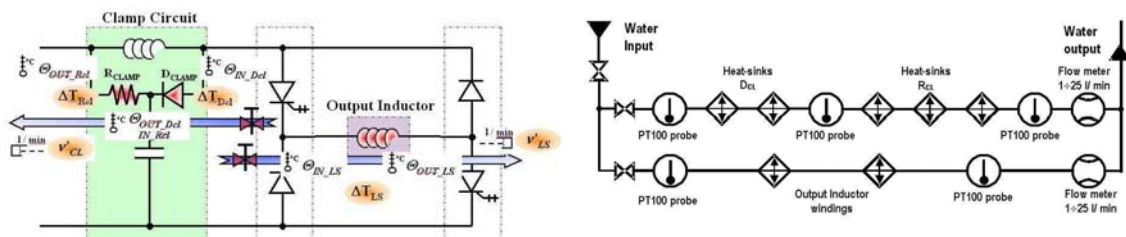


Figure 2-26.- Clamp circuit components and output inductor cooling circuit

## 2.4 3.3kV IGCTs Characterisation

The most relevant parameters obtained during the characterisation process of the 3.3kV IGCT and their associated freewheeling diodes are their switching and on-state losses. However, additional parameters are studied with the aim of defining the working limits and potential performance of the components. Aspects such as the driver power supply consumption and the clamp circuit losses have been also investigated, [ALV-04b].

The 3.3kV IGCT and Diode switching losses are obtained by means of oscillographic measurements (Tektronix oscilloscope TDS3014B, 4 channels, 100 MHz, 1.25Gsamples/s, 9 bits vertical resolution, 10kacquisition points per channel) using high bandwidth voltage probes (Tektronix differential voltage probe P5210, 4400 VRMS, 50 MHz) and high bandwidth current probes (PEM Rogowski AC current probe CWT30 6KA, 40kA/ $\mu$ s, 10 MHz). As the signal integrator of the Rogowski AC current probe eliminates the DC current term of the measured waveform, DC current term compensation is required to calculate the switching power and energy waveforms. Regarding the offset of the differential voltage probes, even if they are compensated by hardware at the beginning of each test, results show that voltage offset compensation is also needed due to the offset change depending on the measuring conditions. For this reason, data treatment of the measured signals is imperative. Firstly, the measured waveforms are transferred to a PC (Wavestar software for Tektronix oscilloscopes). Then, the waveforms are treated to remove their offset levels, and finally, the power and energy waveforms are calculated. As the gate voltage of the IGCTs is not accessible during the tests, the switching losses intervals are selected to separate the whole switching process from the on and blocking states according to the current and voltage waveforms. This procedure is graphically shown in Figure 2-27. Special attention was paid at IGCT and Diode Turn On where the very low losses level made it difficult to identify accurately the end of the switching process.

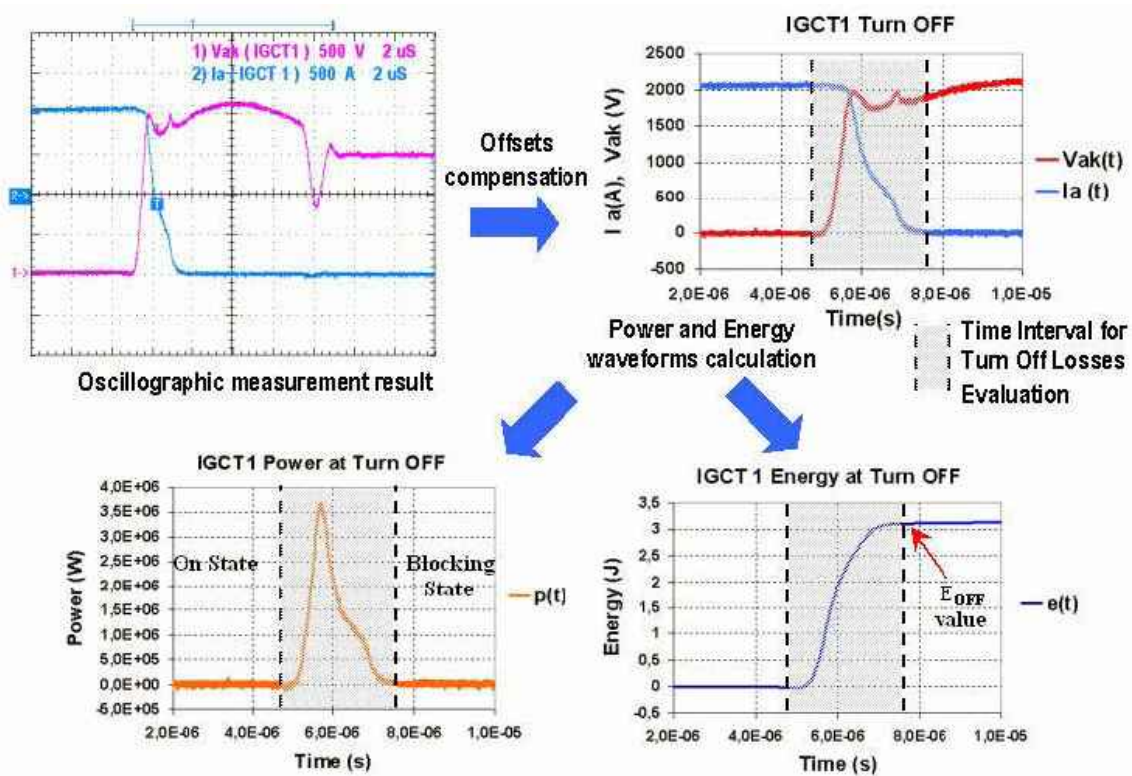


Figure 2-27.- Switching losses evaluation process at IGBT Turn-Off

This switching losses evaluation process is carried out for each switching transient of IGBT and Diodes under given working conditions (DC bus voltage, output DC current, switching frequency). Then, the results for the different working conditions are summarised and the switching characteristic curves of semiconductors are obtained. To complete the switching losses characterisation process, the defining coefficients of each characteristic curve are evaluated using mathematical curve fitting tools, Figure 2-28.

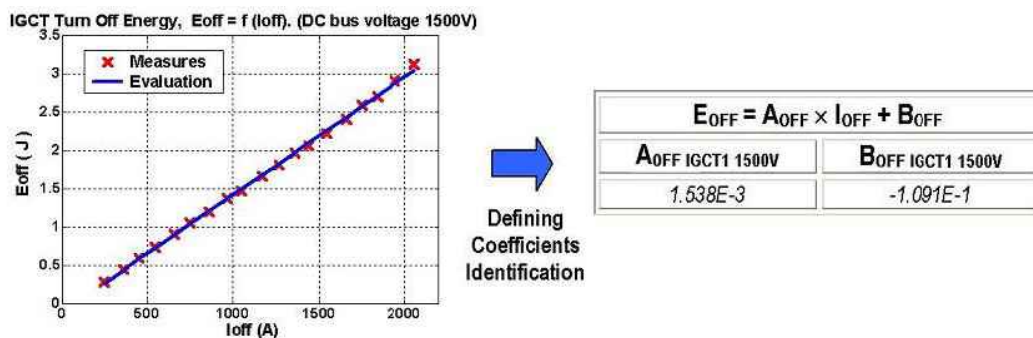


Figure 2-28.- Defining coefficients evaluation by mathematical curve fitting

To evaluate the on state losses, the calorimetric method for water-cooled components is applied, Figure 2-24. Measurement of the water input and output temperature and the water flow in the cooler allow obtaining the total semiconductor losses. This method is also applied to other water-cooled components to evaluate their power losses (output inductor, clamp circuit, etc.).

The values measured for each operating point and for each component are treated to evaluate the components total losses. Only values in thermal steady state are used. However, temperature

measurements are performed at variable flow rate to improve the accuracy of the power losses evaluation system at low output current (power losses) levels.

Once the total losses of a semiconductor are obtained, two evaluation methods can be used to determine the on state losses:

- On-state power losses evaluation by Electro-Thermal measurements (*DIRECT method*): The on state power losses are derived by subtracting the electrically measured switching losses from the total losses measured by means of the calorimetric method, Eq. 2-17.
- Switching / On-state power losses separation by calorimetric evaluation (*INDIRECT method*): The on state power losses are obtained by performing two tests at different switching frequencies with fixed DC input voltage and DC output current conditions. Since the on-state losses are constant and the switching losses are proportional to the switching frequency (the junction temperature change is neglected), the conduction losses can be mathematically separated from the switching losses, Eq. 2-12 to Eq. 2-17.

$$P_{X1}(f_{SW1}, E, I_{OUT}, \alpha) = P_{XCOND1} + K \cdot f_{SW1} \quad \text{Eq. 2-12}$$

$$P_{X2}(f_{SW2}, E, I_{OUT}, \alpha) = P_{XCOND2} + K \cdot f_{SW2} \quad \text{Eq. 2-13}$$

$$P_{XCOND1} \approx P_{XCOND2} \quad \text{Eq. 2-14}$$

$$K = \frac{P_{X2}(f_{SW2}, E, I_{OUT}, \alpha) - P_{X1}(f_{SW1}, E, I_{OUT}, \alpha)}{f_{SW2} - f_{SW1}} \quad \text{Eq. 2-15}$$

$$P_{XSW} = K \cdot f_{SW} \quad \text{Eq. 2-16}$$

$$P_{XCOND} = P_X - P_{XSW} \quad \text{Eq. 2-17}$$

$P_X$  = Component X total losses;  $P_{XSW}$  = Component X switching losses;  $P_{XCOND}$  = Component X on state losses;

The calculation is carried out for each working condition (DC bus voltage, output DC current, switching frequency). Then, the results of the different working conditions are summarised and the semiconductor on-state power loss curves are obtained. Likewise for the switching losses, the on-state defining coefficients of each characteristic curve are evaluated mathematically.

## 2.4.1 3.3kV IGCT Characterisation Results

Several tests were performed to obtain the on state and switching characteristics of 3.3kV IGCTs. For a given switching frequency (500Hz, 750Hz and 1KHz) and DC link input voltage (750V, 1kV, 1.2kV and 1.5kV) the output DC current was adjusted from 0 to 2kA (1.3kA at 1kHz). The measurements were taken always under electrical, Figure 2-29, and thermal steady state conditions. The following sections present the on-state and switching characteristics obtained in the characterisation process.

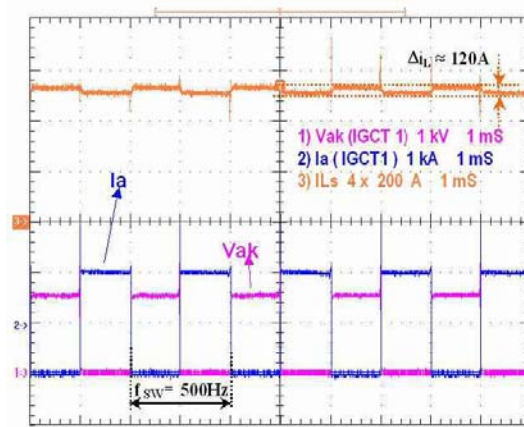


Figure 2-29.- Test bench steady state output current under continuous switching operation, ( $f_{sw}=500\text{Hz}$ ,  $E=1.5\text{kV}$ ,  $I_{OUT}=2\text{kA}$ )

### 2.4.1.1 IGCT switching losses

The IGCT switching characteristics presented in this section are subjected to the switching conditions imposed by the clamp circuit elements utilised in the test bench ( $L_{CL}=1.7\ \mu\text{H}$ ,  $C_{CL}=6\ \mu\text{F}$ ,  $R_{CL}=0.75\ \Omega$ ,  $D_{CL}=5\text{SDF } 03\text{D}4502$ , ABB). The junction temperature of the components is not fixed; it is imposed by the semiconductors losses and the cooling system (ABB water cooling plates, and flow rate between 0.5 l/min and 4 l/min). Figure 2-30 shows the turn on and turn off switching waveforms of the 3.3kV IGCTs under the maximum tested ratings,  $E=1.5\text{kV}$ ,  $I_{OUT}=2\text{kA}$ .

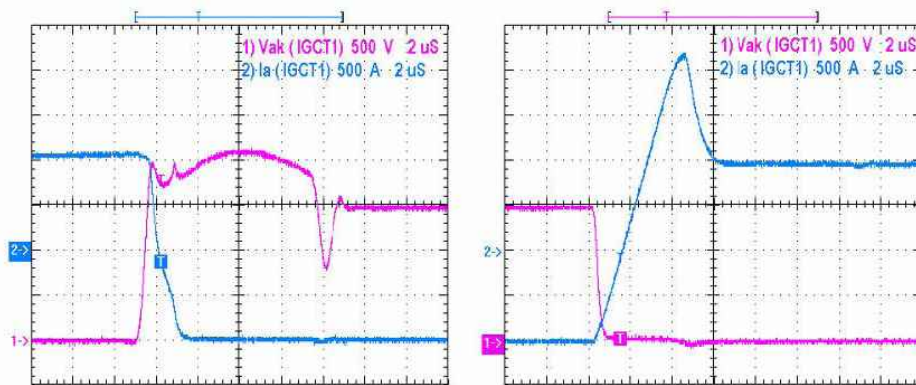


Figure 2-30.- 3.3kV IGCT Turn-Off and Turn-On waveforms, ( $E=1.5\text{kV}$ ,  $I_{OUT}=2\text{kA}$ )

Analysis of the different test results show that the switching characteristics of the IGCTs can be represented by the first order expressions Eq. 2-18, Eq. 2-19.

$$E_{\text{OFF\_IGCT}} = A_{\text{OFF\_IGCT}} \cdot I_{\text{OFF}} + B_{\text{OFF\_IGCT}} \quad \text{Eq. 2-18}$$

$$E_{\text{ON\_IGCT}} = A_{\text{ON\_IGCT}} \cdot I_{\text{ON}} + B_{\text{ON\_IGCT}} \quad \text{Eq. 2-19}$$

After mathematical treatment of the measurement data (by Least Squares Method), the characteristic coefficients of the IGCT switching losses and their representative curves are obtained. These parameters are presented in Table 2-10 for the turn off characteristic and in Table 2-11 for the turn on characteristic.

Switching frequency, $f_{sw}$	Voltage (V)	$A_{OFF\_IGCT\_500Hz}$	$B_{OFF\_IGCT\_500Hz}$	$E_{OFF\_IGCT\_500Hz}$ (J @ 2kA)
500 Hz	1500V	1,538E-03	-1,091E-01	3,129E+00
	1200V	1,314E-03	-8,253E-03	2,679E+00
	1000V	1,117E-03	6,008E-03	2,285E+00
	750 V	9,298E-04	-8,262E-03	1,909E+00
	Voltage (V)	$A_{OFF\_IGCT\_750Hz}$	$B_{OFF\_IGCT\_750Hz}$	$E_{OFF\_IGCT\_750Hz}$ (J @ 2kA)
750 Hz	1200V	1,352E-03	-3,387E-02	2,753E+00
	1000V	1,123E-03	1,935E-02	2,286E+00
	750 V	9,441E-04	-1,081E-02	1,934E+00

Table 2-10.- Coefficients of the 3.3kV IGCT turn-off switching losses characteristics

Switching frequency, $f_{sw}$	Voltage (V)	$A_{ON\_IGCT\_500Hz}$	$B_{ON\_IGCT\_500Hz}$	$E_{ON\_IGCT\_500Hz}$ (J @ 2kA)
500 Hz	1500V	1,056E-04	-9,582E-03	2,071E-01
	1200V	1,095E-04	-1,081E-02	2,007E-01
	1000V	8,788E-05	-8,520E-03	1,584E-01
	750 V	6,244E-05	-5,304E-03	1,222E-01
	Voltage (V)	$A_{ON\_IGCT\_750Hz}$	$B_{ON\_IGCT\_750Hz}$	$E_{ON\_IGCT\_750Hz}$ (J @ 2kA)
750 Hz	1200V	1,161E-04	-1,116E-02	2,438E-01
	1000V	9,130E-05	-8,465E-03	1,787E-01
	750 V	7,350E-05	-9,332E-03	1,425E-01

Table 2-11.- Coefficients of the 3.3kV IGCT turn-on switching losses characteristics

Figure 2-31 shows the 3.3kV IGCT turn-off losses under different working conditions. A slight change in the turn-off characteristic for the 500Hz and 750Hz operation can be noticed. This effect can be explained by the temperature dependence of the switching characteristics of the semiconductors. The higher the switching frequency, the higher are the switching power losses and therefore the junction temperature of the component increases for a given cooling condition. Working at higher junction temperature leads to the increase of the component turn-off losses. Also, generally, the higher the DC voltage the higher the turn-off power losses.

The main power losses of IGCTs at turn-off are generated by two different effects:

- High  $di/dt$  change in the current produces a high over voltage over the IGCT. This first spike Figure 2-30, depends on the dynamic behaviour of the IGCT (variable capacitance,  $di/dt$  at turn-off) and on the parasitic inductance between the clamp circuit and the switching cell. This process lasting several hundred nanoseconds (300ns-500ns depending on the switching current) but it generates the highest power peak value over the IGCT.
- The tail current of the IGCT along with the over voltage over the IGCT due to the clamp circuit produces a lower power peak that lasts longer (between 1.5 $\mu$ s and 2.5 $\mu$ s depending mainly on DC input voltage and the switching current).

To minimise the power losses at IGCT turn-off, special attention must be paid to the mechanical arrangement of the clamp circuit with respect to the switching cells. The use of Bus-Bars is advised to minimise the parasitic inductance of the switching cell.

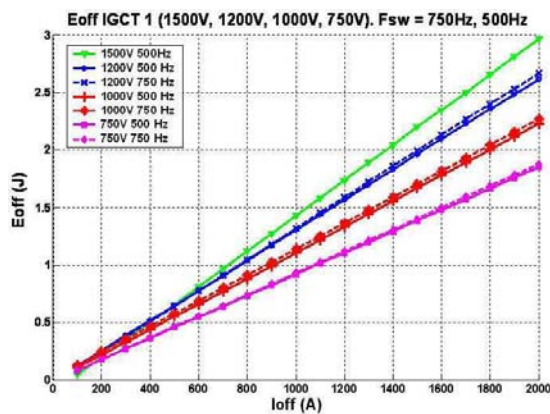


Figure 2-31.- 3.3kV IGCT Turn-Off switching energy per pulse versus Turn-Off current

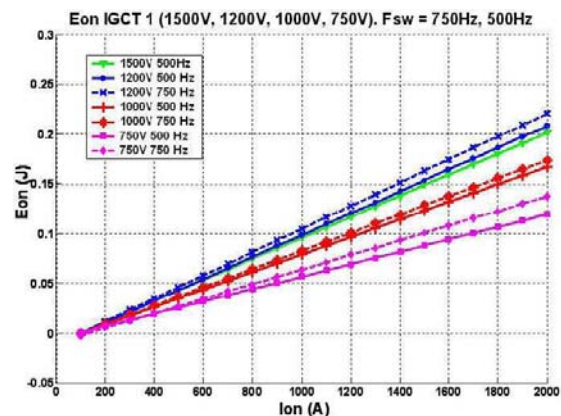


Figure 2-32.- 3.3kV IGCT Turn-On switching energy per pulse versus Turn-On current

The evolution of the IGCT turn-on characteristic is shown in Figure 2-32. Depending on the switching frequency, the same evolution as that obtained for the turn-off characteristic is noticed. It can be seen that the turn-on losses increase when the semiconductor junction temperature increases (higher switching frequency) at the same voltage level. Moreover, an unexpected evolution of the turn-on losses with the increasing DC input voltage was found. As the DC input voltage increases from 750V to 1.2kV the turn-on losses increase. However, in the next step (1.5kV), the turn-on losses decrease slightly. The reason for this evolution could be explained by the change in the turn-on  $di/dt$  with the DC input voltage. The higher the DC input voltage, the higher the  $di/dt$  at turn-on and therefore the switching time becomes shorter. Even if higher  $di/dt$  at turn-on leads to a higher diode recovery current, the evaluated losses in the defined integration interval could become smaller at high DC input voltage. Other measurements under these conditions could be performed to investigate the depicted evolution and reject the measuring errors hypothesis (delay compensation of the current and voltage probes, etc.).

#### 2.4.1.2 IGCT on state losses

In this section, IGCT on-state power losses evaluation results applying the Direct and Indirect methods are summarised and compared. The IGCT on-state characteristic defining coefficients ( $V_{T0}$  -threshold voltage and  $R_T$  - slope resistance) are derived by mathematical treatment (Least Squared Method) from the obtained on state power losses at IGCT working duty cycle ( $\alpha \approx 0.5$ ), Eq. 2-20. Finally, the IGCT on state voltage characteristic is calculated, Eq. 2-21.

$$P_{COND} = V_{T0} \cdot I_T \times \alpha + R_T \cdot I_T^2 \cdot \alpha \quad \text{Eq. 2-20}$$

$$V_T = V_{T0} + R_T \cdot I_T \quad \text{Eq. 2-21}$$

Table 2-12 shows the characteristic coefficients for the IGCT using the Direct and the Indirect method.

Test results show the expected negative temperature dependency of the IGCT on-state characteristic (at higher current it changes to positive). The higher the switching frequency, (and therefore the component power losses), the lower the  $V_T$  on-state voltage for a given DC input voltage. The same evolution is obtained by increasing the DC input Voltage (increasing IGCT

power losses) at given switching frequency. The higher the DC input voltage, the lower the  $V_T$  voltage.

Switching frequency, $f_{sw}$		Voltage (V)	$V_{T0\_IGCT\_500Hz}$ (V)	$R_{T\_IGCT\_500Hz}$ ( $\Omega$ )	$P_{COND\_IGCT\_500Hz}$ (2kA)	
Direct Method	500 Hz	1200V	0,8818 V	0,3290 E-03 $\Omega$	1526,91 W	
		1000V	0,9485 V	0,3290 E-03 $\Omega$	1629,20 W	
		750 V	0,9414 V	0,3470 E-03 $\Omega$	1609,02 W	
			Voltage (V)	$V_{T0\_IGCT\_750Hz}$ (V)	$R_{T\_IGCT\_750Hz}$ ( $\Omega$ )	$P_{COND\_IGCT\_750Hz}$ (2kA)
	750 Hz	1200V	0,868 V	0,320 E-03 $\Omega$	1508,00 W	
		1000V	0,850 V	0,381 E-03 $\Omega$	1612,00 W	
		750 V	0,913 V	0,3420 E-03 $\Omega$	1597,00 W	
			Voltage (V)	$V_{T0\_IGCT}$ (V)	$R_{T\_IGCT}$ ( $\Omega$ )	$P_{COND\_IGCT}$ (2kA)
	Indirect Method (500Hz - 750Hz)	1200V	1.0388 V	1.9918e-004 $\Omega$	1417.647 W	
1000V		1.0706 V	2.5133e-004 $\Omega$	1585.335 W		
750 V		1.0779 V	2.8323e-004 $\Omega$	1628.667 W		

Table 2-12.- Coefficients for the IGCT on-state characteristic (Direct Method and Indirect Method)

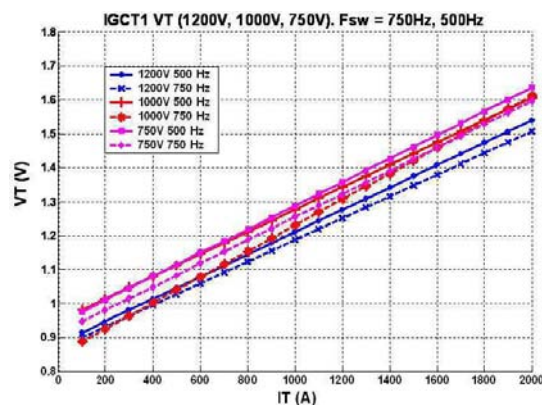


Figure 2-33.- 3.3kV IGCT1 On-State characteristics (Direct Method)

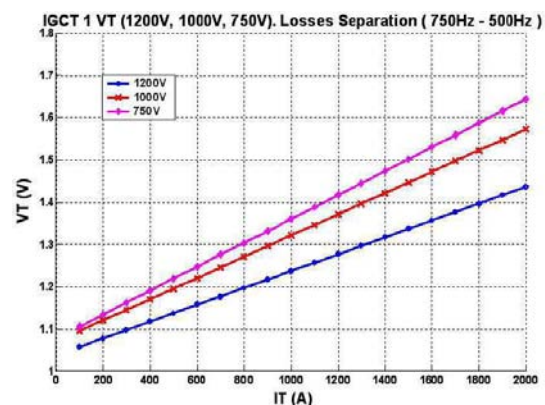


Figure 2-34.- 3.3kV IGCT1 On-State characteristics (Indirect Method)

In contrast to the expected results, a relatively high difference is found between the 2 proposed methods, which questions the accuracy of the measurements. ABB certification tests on 3.3kV IGCT indicates an on state voltage  $V_T=1.40V$  at on state current  $I_T=1kA$  and junction temperature  $T_{VJ}=125^\circ C$ . The results from the test bench are always below this value. IGCT operating conditions are not equivalent under different measurement conditions (lower junction temperature), but due to the negative temperature dependency of the IGCT on-state characteristic we should find a value higher than the one indicated by ABB. In the worst case we find a difference of 0.22V between the ABB value and our evaluated value. This  $V_T$  difference represents a power losses difference of 220W at  $\alpha=0.5$  and  $I_T=2kA$  (test bench working conditions) for 4kW of semiconductor total losses (5.5% error). Although this total power losses evaluation error (5.5%) can be considered as acceptable when standard measurement equipments are used, derivation of the on-state coefficients by the proposed methods leads to higher on-state voltage estimation errors (around 12%) More accurate thermal and flow measurements will be required to obtain better characterisation results. However the test method



shows its potential in being able to distinguish the temperature dependence on the IGBT characteristic.

To obtain accurate values for the IGBT on state characteristic, standard on state measurements were developed by ABB. The obtained characteristic coefficients obtained by curve fitting with the characteristics measured by ABB are shown in Table 2-13. These characteristics are shown in Figure 2-35.

Junction Temperature $T_{VJ}$ (°C)	$V_{T0\_IGBT}$ (V)	$R_{T\_IGBT}$ ( $\Omega$ )
25 °C	1.357 V	0.269 E-03 $\Omega$
125 °C	1.024 V	0.379 E-03 $\Omega$

Table 2-13.- 3.3kV IGBT on state characteristic coefficients, ABB measurement

Figure 2-36 shows the comparison between the characteristic obtained by the Direct method and the characteristic obtained in ABB. It is observed that the curves obtained by the Direct method follow the ABB characteristics evolution but with a certain offset (around 0.2V).

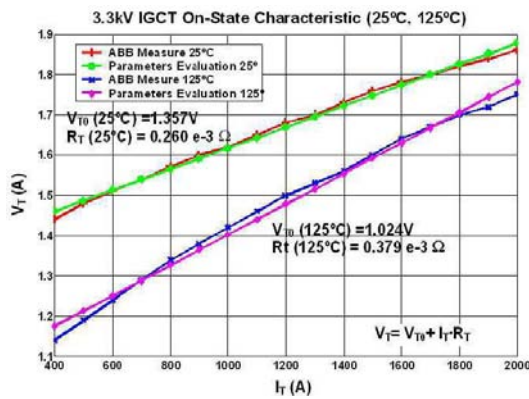


Figure 2-35.- 3.3kV IGBT1 On-State characteristics (ABB measure)

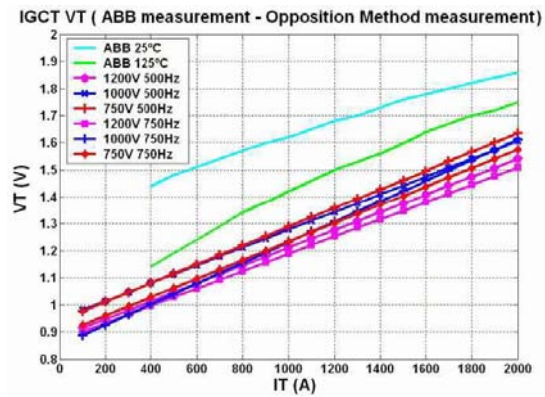


Figure 2-36.- On state characteristics comparison, (ABB - Direct Method)

## 2.4.2 FWD Characterisation Results

The characterisation of the freewheeling diodes FWD was performed at the same time as the IGBT, so the working conditions were exactly the same.

### 2.4.2.1 FWD switching losses

The first diode switching tests were performed taking into consideration only the turn-off switching characteristics. However, the latest tests were also focused on the turn-on characteristics of the diodes to identify their contribution to the power losses of the component. Figure 2-37 shows the turn of and turn off switching waveforms of the freewheeling diodes at  $E=1.5kV$ ,  $I_{OUT}=2kA$ .

$$E_{OFF\_DIODE} = A_{OFF\_DIODE} \cdot I_{OFF} + B_{OFF\_DIODE} \quad \text{Eq. 2-22}$$

$$E_{ON\_DIODE} = A_{ON\_DIODE} \cdot I_{ON}^2 + B_{ON\_DIODE} \cdot I_{ON} + C_{ON\_DIODE} \quad \text{Eq. 2-23}$$

Test results show that turn-off characteristics of the diodes can be represented by a first order expression, Eq. 2-22, and turn-on characteristics by a second order expression, Eq. 2-23. After

mathematical treatment of the measurement data, the coefficients of the Diode switching losses characteristics and their representative curves were obtained.

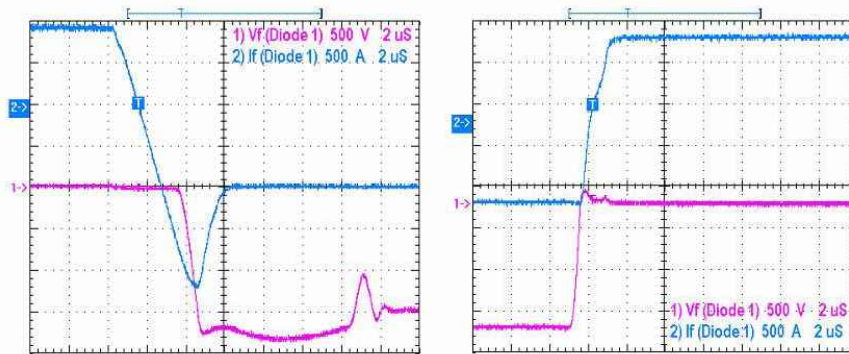


Figure 2-37.- FW Diode Turn-Off and Turn-On waveforms, ( $E=1.5kV$ ,  $I_{OUT}=2kA$ )

Table 2-14 shows the coefficients obtained for the diode turn of losses characteristics. These characteristics are depicted in Figure 2-38.

Voltage (V)	A <sub>OFF_DIODE</sub>	B <sub>OFF_DIODE</sub>	E <sub>OFF_DIODE</sub> (J @ 2kA)
1500V (500 Hz)	9,666E-04	2,311E-01	2,040E+00
1200V (750 Hz)	7,194E-04	2,483E-01	1,629E+00
1000V (750 Hz)	5,341E-04	2,028E-01	1,192E+00
750 V (750 Hz)	3,467E-04	1,428E-01	7,751E-01

Table 2-14.- Defining coefficients for diode turn-off switching losses (1.5kV, 1.2kV, 1kV, 750V)

Again, the parasitic inductance of the switching cell takes a relevant role in the diode power losses at turn-off. Special attention must be paid to the mechanical assembly between the clamp circuit and the switching cells. The parasitic inductance must be as low as possible to minimise the turn-off switching losses of the diode. Also, the dynamic behaviour of the diode (recovery time and current, parasitic capacitance) plays a very important role on its turn-off power losses. They should be selected correctly according to the intended operation mode.

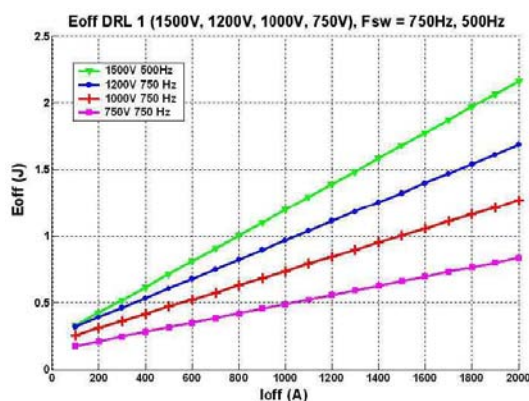


Figure 2-38.- Diode turn-off switching energy per pulse versus turn-off current

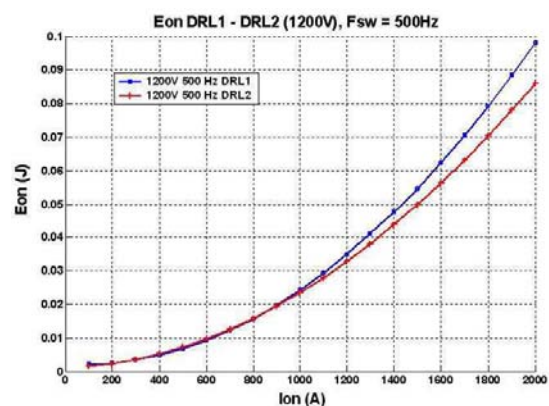


Figure 2-39. - Diode 1 & Diode 2 turn-on switching energy per pulse versus turn-on current

Figure 2-40 shows the non-linear evolution of the Diode recovery current  $I_{RRM}$  versus its turn-off current. However, an almost linear evolution of the  $I_{RRM}$  current with regard to the  $di/dt$  value can

be noticed. These effects are also noticed in Figure 2-41, where the recovery current over the turn-off current ratio versus the turn-off current is depicted.

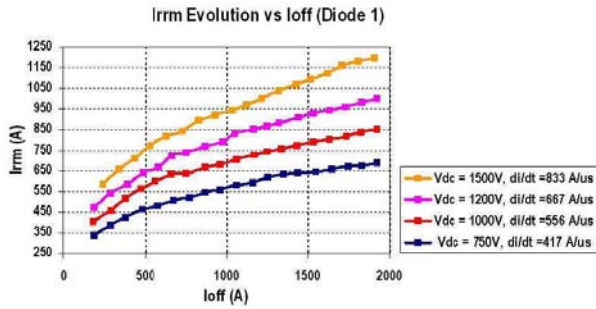


Figure 2-40.- Diode recovery current evolution versus turn-off current

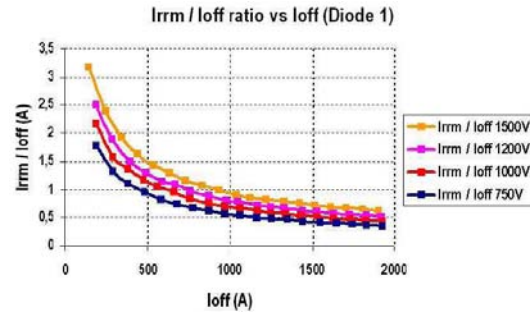


Figure 2-41.- Diode recovery current / turn-off current ratio versus turn-off current.

Two different turn-on switching characteristics of diodes were evaluated at DC input voltage  $E=1200\text{V}$  for a switching frequency of  $500\text{Hz}$ . The objective was to identify the contribution of diode turn-on losses to its total power losses.

The evaluated defining coefficients for both diodes turn-on characteristics are shown in Table 2-15.

$A_{\text{ON\_DIODE1}}$	$B_{\text{ON\_DIODE1}}$	$C_{\text{ON\_DIODE1}}$	$E_{\text{OFF\_DIODE1}} \text{ (J @ 2kA)}$
$2.594\text{e-}8$	$-4.004\text{e-}6$	$2.318\text{e-}3$	0.098
$A_{\text{ON\_DIODE2}}$	$B_{\text{ON\_DIODE2}}$	$C_{\text{ON\_DIODE2}}$	$E_{\text{OFF\_DIODE1}} \text{ (J @ 2kA)}$
$2.012\text{e-}8$	$2.173\text{e-}6$	$1.227\text{e-}3$	0.086

Table 2-15.- Defining coefficients for Diode1 & Diode2 turn-on switching losses (1200V, 500Hz)

For DC input voltage  $E=1.2\text{kV}$ , switching at  $500\text{Hz}$  with an output DC current of  $2\text{kA}$ , turn-on power losses of Diode1 are around  $50\text{W}$ . These losses represent only 6% of the Diode1 turn-off losses (electrical measurement) and the 3% of the total Diode1 losses (thermal measurement). The contribution of the Diode turn-on losses to the total losses increases at higher switching frequencies.

Figure 2-39 shows the comparison between the Diode 1 and Diode 2 turn on characteristics. A slight difference can be noticed at high turn-on current. This effect can be explained by the different dynamic characteristics of diodes and their associated IGCTs (diode forward on-voltage, IGCT tail current).

#### 2.4.2.2 FWD on state losses

On-state characteristics evaluation results of diode1 applying the Direct and Indirect method are summarised and compared in this section. The Diode on-state characteristic ( $V_F$ , on-state voltage) is defined by two coefficients ( $V_{F0}$  -threshold voltage and  $R_D$  - Dynamic resistance), Eq. 2-24. The on-state characteristic defining coefficients are obtained by mathematical treatment from the obtained on state power losses at diode working duty cycle ( $\alpha \approx 0.5$ ), Eq. 2-25.

The representative coefficients of the diode on state characteristics are given in Table 2-16. Both methods are considered, the Direct and Indirect methods. Figure 2-42 and Figure 2-43 show the corresponding characteristics.

$$P_{COND} = V_{F0} \cdot I_F \cdot \alpha + R_D \cdot I_F^2 \cdot \alpha \tag{Eq. 2-24}$$

$$V_F = V_{F0} + R_D \cdot I_F \tag{Eq. 2-25}$$

Test results applying the direct method show the positive temperature dependency of the Diode on-state characteristic, which corresponds with the expected behaviour. The higher the DC input voltage, the higher the  $V_F$  on-state voltage for a given switching frequency (junction temperature). However, the results obtained by the indirect method show a negative temperature dependency of this characteristic, which deviates from the expected results. Low calorimetric system accuracy can be the reason to this deviation.

	Voltage (V)	$V_{F0\_DIODE}$ (V)	$R_{D\_DIODE}$ ( $\Omega$ )	$P_{COND\_DIODE}$ (2kA)
Direct Method	1200 V	8,862E-01 V	3,842E-04 $\Omega$	1630,80 W
	1000 V	9,336E-01 V	3,336E-04 $\Omega$	1590,84 W
	750 V	8,858E-01 V	3,050E-04 $\Omega$	1473,18 W
	Voltage (V)	$V_{F0\_DIODE}$ (V)	$R_{D\_DIODE}$ ( $\Omega$ )	$P_{COND\_DIODE}$ (2kA)
Indirect Mode	1200V	0.6435 V	2.9477e-004 $\Omega$	1233.04 W
	1000V	0.6775 V	3.2846e-004 $\Omega$	1334.42 W
	750 V	0.6343 V	3.7871e-004 $\Omega$	1391.75 W

Table 2-16.- Defining coefficients for diode on-state characteristics (Direct and Indirect Methods)

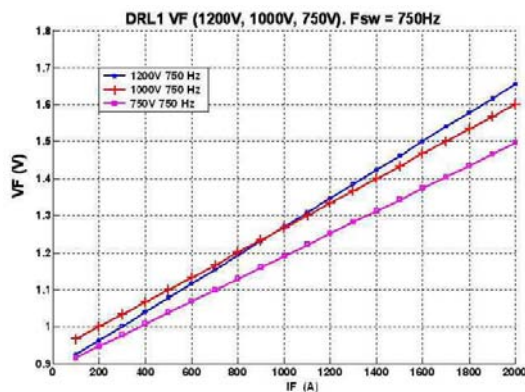


Figure 2-42.- Diode on-state characteristics (Direct Method)

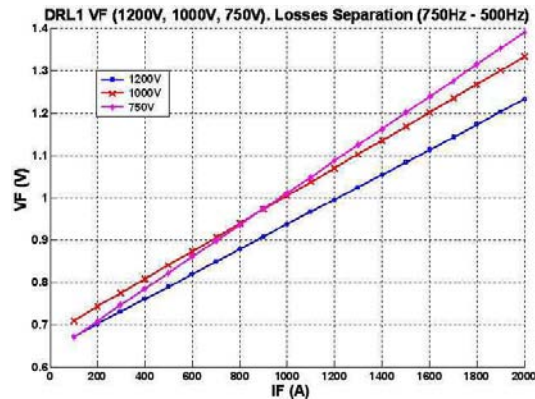


Figure 2-43.- Diode on-state characteristics (Indirect Method)

ABB certification test of Diodes indicates  $V_F$  ( $I_F=1kA$ )=1.20V and  $V_F$  ( $I_F=2kA$ )=1.48V for a junction temperature  $T_{VJ}=125^\circ C$ . With these values, an approximation of the diode on state characteristic defining parameters at  $125^\circ C$  are identified, Table 2-17.

Junction Temperature $T_{VJ}$ ( $^\circ C$ )	$V_{F0\_DIODE}$ (V)	$R_{D\_DIODE}$ ( $\Omega$ )
125 $^\circ C$	0.83 V	0.34 E-03 $\Omega$

Table 2-17.- Diode on state defining coefficients,  $T_{VJ}=125^\circ C$

### 2.4.3 Gate Unit Power Supply Requirements

The Siebel SW 32-24D20G power supply is used to supply the IGCT gate unit, Figure 2-44. The output current of the IGCT gate unit power supply is measured to identify its power requirements. Several measurements were performed at different DC link voltages, DC output currents and switching frequencies. The results show that only the IGCT turn off switching current and the switching frequency influence the power consumption of the driver power supply, no influence of the DC link voltage was perceived. Also the duty cycle should effect the gate unit power consumption due to the back-porch current during the IGCT on state, however these effects have not been analysed due to the fixed operation mode of the test bench (constant duty cycle  $\alpha=0.5$ ).



Figure 2-44.- Siebel SW 32-24D20G DC/DC power supply, (20V<sub>DC</sub> regulated, 80W)

Measurement results show that the driver output current evolution with the turn of switching current at fixed switching frequency can be represented by a first order expression Eq. 2-26, as shown in Figure 2-45.

$$I_{DR\_FSW} = A_{DR\_FSW} \cdot I_{OFF} + B_{DR\_FSW} \quad \text{Eq. 2-26}$$

$$I_{DR\_IOFF} = K1_{IOFF} + K2_{IOFF} \cdot f_{SW} \quad \text{Eq. 2-27}$$

The defining coefficients of the gate unit power supply consumption characteristic are identified for three different switching frequencies (500Hz, 750Hz and 1KHz), Table 2-18. The DC output test current was varied between 0 and 2kA when operating at 500Hz and 750Hz. However, it was limited to 1.3kA at 1kHz to avoid the destruction of the IGCT. In fact, operation between 1.5kA and 1.6kA was also tested but resulted in the destruction of the IGCT sample. The gate unit power supply consumption limit was reached and led to a non-homogeneous blocking process of the internal IGCT cells (GTO mode commutation), thus current focalisation and finally wafer perforation.

Switching frequency, $f_{SW}$	$A_{DR\_FSW}$	$B_{DR\_FSW}$	$I_{DRIVER} (2kA)$
1000 Hz	1.764e-3	1.2703	4.80 A
750 Hz	1.2234e-3	1.2247	3.67 A
500 Hz	8.1739e-4	9.7479e-1	2.61 A

Table 2-18.- Coefficients of the gate unit power supply output current - turn off current characteristic,  $I_{DR}=f(I_{OFF})$

The gate unit power supply limit (80W and paralleling operation not possible) restricted the use of the IGCT at higher switching frequencies under relevant DC output currents. To estimate the power requirements of the driver power supply at higher switching frequencies (until 2kHz), it is firstly verified that the gate unit current evolves proportionally with the switching frequency for a given turn-off switching current Figure 2-46, for example following Eq. 2-27. The coefficients K1

and K2 are evaluated for each turn-off switching current from 100A to 2KA and then the driver current is extrapolated at different switching frequencies. The output power of the power supply is finally calculated considering the power supply DC output voltage to be constant and equal to 20V. The estimated power consumption for the 3.3kV IGBT driver power supply is shown in Figure 2-47.

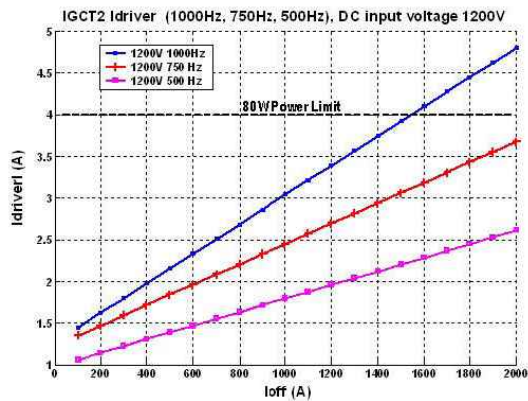


Figure 2-45.- Driver power supply output current vs. Turn-Off current ( $f_{sw} = 500\text{Hz}, 750\text{Hz}, 1\text{kHz}$ ).

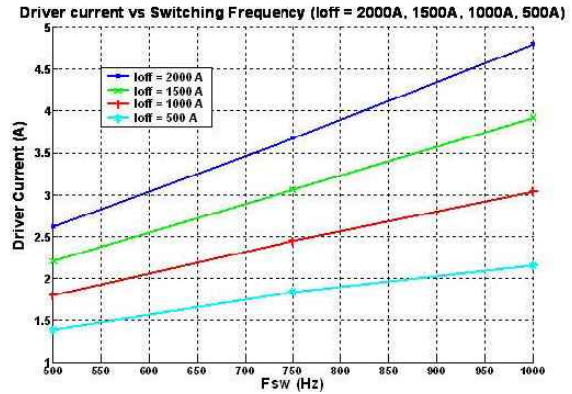


Figure 2-46.- Driver power supply current vs. switching frequency ( $I_{off} = 500\text{A}, 1\text{kA}, 1.5\text{kA}, 2\text{kA}$ )

The calculated results show how the limit of the utilised power supply (80W) is reached when operating the IGBT at 1kHz and 1.5kA (duty cycle  $\alpha=0.5$ ), which match with the failure mode that was obtained experimentally on the test bench.

Obviously, these results do not take into account the thermal limitations of the semiconductors and consider exclusively the power consumption demands of the gate unit. Also, one has to consider that the utilised gate unit is designed to operate at maximum IGBT switching frequencies of 1kHz. The operation at higher switching frequencies should also require hardware modifications on the gate unit to allow safe operation of their components (electrolytic capacitor, MOSFETs, etc.), thus the right operation of the IGBT.

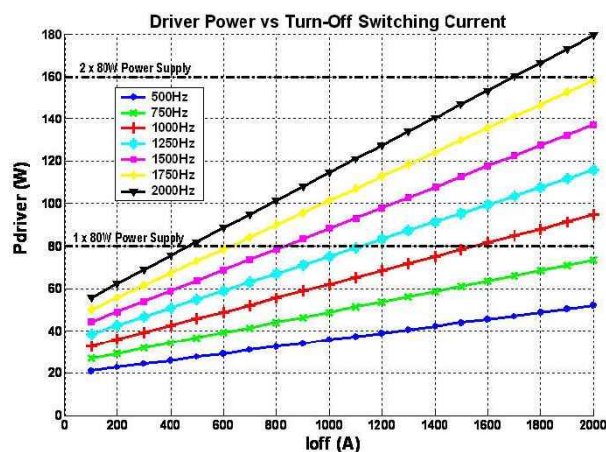


Figure 2-47.- Estimated power consumption for the 3.3KV IGBT gate unit power supply

### 2.4.4 Clamp Circuit Power Losses

Hard Switching IGBT switching cells must contain an IGBT turn-on inductor (snubber) to limit the diode turn-off  $di/dt$ . At IGBT turn-off, the energy stored in the inductor is discharged and clamped

by means of an RCD circuit, Figure 2-48. Not all of the magnetising energy is evacuated over the RCD circuit; certain amount of energy is dissipated on the semiconductors and restored to the input power supply.

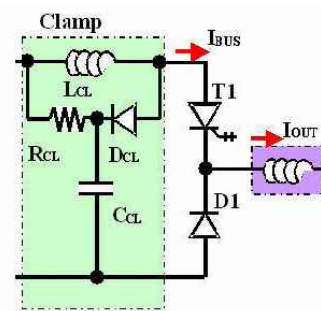


Figure 2-48. - IGBT Switching cell di/dt inductor and RCD clamp circuit

The clamp circuit power losses are evaluated to identify the amount of magnetising energy dissipated on the clamp circuit components.  $D_{CL}$  and  $R_{CL}$  power losses are evaluated by means of the calorimetric method. The clamp inductor and capacitor power losses are estimated from component data specifications (components parasitic resistors). The obtained results at 500Hz and 750Hz for several DC input voltages are compared with the theoretically calculated magnetising power generated by the di/dt inductor, Eq. 2-28. The comparison results are shown in Figure 2-49.

$$\text{Magnetising Power} = \frac{1}{2} \cdot L_{CL} \cdot I_{OUT}^2 \cdot f_{SW} \tag{Eq. 2-28}$$

Results show that the clamp circuit power losses increase with the DC input voltage for a given switching frequency. This fact can be explained by the IGBT turn-off behaviour change with the increasing DC input voltage. The higher the DC input voltage, the smaller the turn-off switching time and the higher the clamp circuit over voltage. Table 2-19 shows the measured turn-off times and clamp over voltage values at different DC input voltage levels. This fact means that with higher DC input voltage, the IGBT turn-off behaviour becomes more ideal and more energy is dissipated over the clamp circuit components.

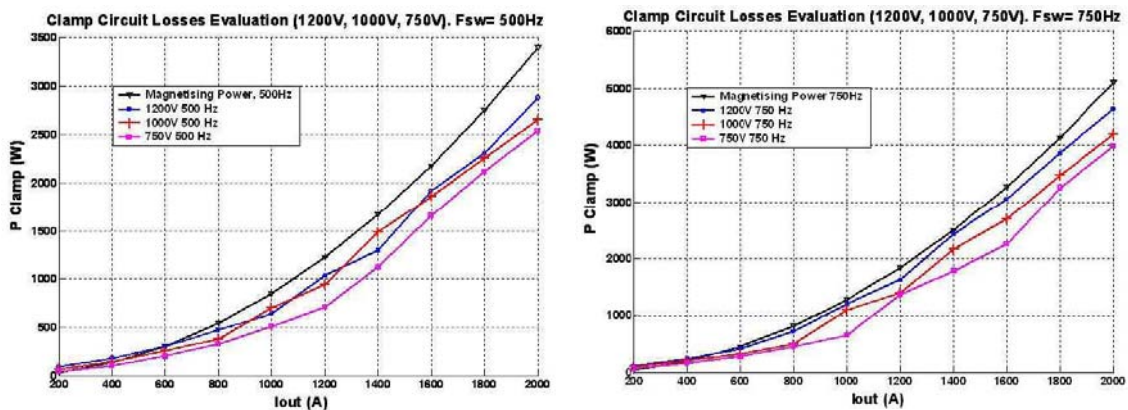


Figure 2-49.- Clamp circuit losses evaluation, fsw = 500Hz, 750Hz

Figure 2-50 shows the magnetising power percentage dissipated over the clamp circuit components at different switching frequencies for several DC input voltages.

Switching Frequency, $f_{sw}$ (Hz)	DC link Voltage (V)	$T_{OFF}$ ( $\mu s$ )	$\Delta V_{CL}$ (V)
500 Hz	750 V	3.72 $\mu s$	572 V
	1000 V	3.28 $\mu s$	585 V
	1200 V	2.96 $\mu s$	591 V
750 Hz	750 V	3.78 $\mu s$	577 V
	1000 V	3.35 $\mu s$	586 V
	1200 V	3.12 $\mu s$	606 V
	1500 V	2.45 $\mu s$	621 V

Table 2-19.- 3.3kV IGBT turn off switching times at different DC input voltage levels ( $I_{OFF}=2kA$ )

At 1.2kV DC input voltage, around the 85%-90% of the magnetising stored energy is dissipated over the clamp circuit components. At lower DC input voltages, 1000V and 750V, the dissipated energy is around 80%. At low output current the evaluation is not accurate enough, the calorimetric system for the clamp circuit is not adapted to measure low power losses due to the usage of a flow-meter with a large measurement range.

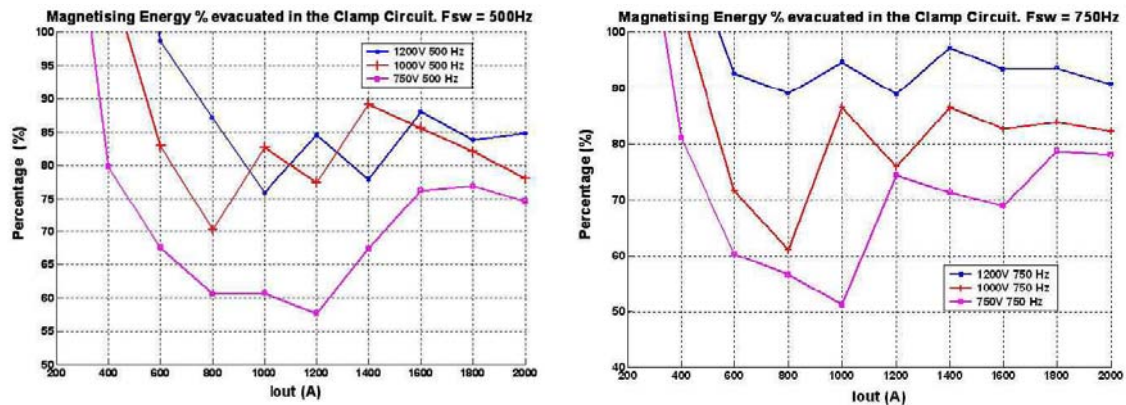


Figure 2-50.- Magnetising power % dissipated by the clamp circuit components,  $f_{sw} = 500Hz, 750Hz$

## 2.5 3.3kV IGBT – IGBT Comparison

The experimental 3.3kV IGBT can be considered as a competitor for the existing 3.3kV IGBT. Even if both technologies are very different and several technological considerations have to be taken into account when selecting the semiconductor to utilise, here only aspects related to the power handling capability of the component are considered. This section is intended to show the potential offered by the use of 3.3kV IGBTs. The IGBT selected to compare with the 3.3kV IGBT is the new ABB 3.3kV/1.2kA HiPak IGBT (5SNA 1200E330100).

Table 2-20 and Table 2-21 show the most relevant characteristics of IGBTs and IGBTs. IGBT and IGBT on-state values are given under the same working conditions ( $T_{VJ}=125^{\circ}C, I_C=1.2kA$ ). However, switching characteristics of IGBTs have been linearly extrapolated to compare both semiconductors at equivalent working conditions ( $V_{CC}=1.5kV, T_{VJ} = 80^{\circ}C, I_C=1.2kA$ ). It must be pointed out that the IGBT associated freewheeling diode is also integrated in the power module, representing one third of the surface available for semiconductors. If diode dies would be exchanged with IGBT dies, the IGBT current rating could be increased and its voltage drop decreased, however this product is not commercially available.



<b>Collector-Emitter Saturation Voltage, <math>V_{CE\ sat}</math></b>	$I_C = 1200\text{ A}, V_{GE} = 15\text{ V}, T_{VJ} = 125^\circ\text{C}$		3.8 V
<b>Turn-on switching energy, <math>E_{ON}</math></b>	$V_{CC}=1800\text{V}, I_C= 1200\text{A}, R_G=1.5\Omega,$ $V_{GE}=\pm 15\text{V}, L_\sigma=100\text{nH}$	$T_{VJ} = 25^\circ\text{C}$	1340 mJ
		$T_{VJ} = 125^\circ\text{C}$	1890 mJ
	Linear Extrapolation $V_{CC}=1500\text{V}, T_{VJ} = 80^\circ\text{C}$		1370 mJ
<b>Turn-off switching energy, <math>E_{OFF}</math></b>	$V_{CC}=1800\text{V}, I_C= 1200\text{A}, R_G=1.5\Omega,$ $V_{GE}=\pm 15\text{V}, L_\sigma=100\text{nH}$	$T_{VJ} = 25^\circ\text{C}$	1420 mJ
		$T_{VJ} = 125^\circ\text{C}$	1950 mJ
	Linear Extrapolation $V_{CC}=1500\text{V}, T_{VJ} = 80^\circ\text{C}$		1430 mJ

Table 2-20.- New ABB 3.3kV / 1.2kA (5SNA1200E330100) HiPak IGBT characteristics

LV IGBT (5SHY45L3300) Characteristics			
<b>On-state Voltage, <math>V_T</math></b>	$I_C = 1200\text{ A}, T_{VJ} = 125^\circ\text{C}$		1.42 V
<b>Turn-on energy per pulse, <math>E_{ON}</math></b>	$V_D=1500\text{V}, I_T= 1200\text{A}, R_{CL}=0.75\Omega,$ $C_{CL}= 6\mu\text{F}, L_{CL}=1.7\mu\text{H}, L_\sigma=100\text{nH}$	$T_{VJ} = 80^\circ\text{C}$	120 mJ
<b>Turn-off energy per pulse, <math>E_{OFF}</math></b>	$V_D=1500\text{V}, I_T= 1200\text{A}, R_{CL}=0.75\Omega,$ $C_{CL}= 6\mu\text{F}, L_{CL}=1.7\mu\text{H}, L_\sigma=100\text{nH}$	$T_{VJ} = 80^\circ\text{C}$	1740 mJ

Table 2-21.- ABB experimental 5SHY45L3300 3.3kV IGBT characteristics

The main difference between the two types of semiconductors appears in the on-state characteristic. The saturation voltage of the IGBT is more than 2.6 times greater than the IGBT on-state voltage (3.8V versus 1.42V). Regarding the switching losses, the IGBT has higher turn-off losses than the IGBT, but the turn-on losses are much lower due to the effect of the  $di/dt$  limiting inductor. Part of the energy losses is deviated from the IGBT to the clamp circuit.

To compare the losses on both components, a DC/DC chopper operation is selected. In that way, only the losses of the IGBT have influence on the thermal budget of the module, the freewheeling diode does not work. The working conditions consider the components operating at 1kHz with constant duty cycle  $\alpha=0.5$ , under a DC output current of 1.2kA and a DC input voltage of 1.5kV. The clamp circuit losses are included in the IGBT total switching losses budget to have a more realistic comparison between the IGBT and IGBT switching characteristics. Table 2-22 show the conduction and switching losses comparison between the experimental 3.3kV IGBT and the new 3.3 kV ABB IGBT.

	IGBT 3.3kV / 1.2kA	IGBT 3.3kV / 4kA
<b><math>P_{COND}</math></b>	2280 W ( $I_C=1.2\text{kA}, \alpha = 0.5, V_{CE\ sat} = 3.8\text{ V}$ )	852 W ( $I_T=1.2\text{kA}, \alpha = 0.5, V_T = 1.42\text{ V}$ )
<b><math>E_{OFF} / P_{SW\ OFF}</math></b>	1.43 J / 1430 W	1.74 J / 1740 W
<b><math>E_{ON} / P_{SW\ ON}</math></b>	1.37 J / 1370 W	0.12 J / 120 W
<b>Clamp Circuit</b>	0	1.22 J / 1220 W
<b><math>E_{TOT} / P_{SW\ TOT}</math></b>	2.80 J / 2800 W	3.08 J / 3080 W
<b><math>P_{TOT}</math></b>	5080 W	3932 W

Table 2-22.- 3.3kV IGBT – IGBT power losses evaluation ( $E=1.5\text{kV}, I_{OUT}=1.2\text{kA}, f_{SW}=1\text{kHz}, \alpha=0.5$ )

For this operation mode, the total switching losses difference between the two solutions is not relevant (280W more losses on the IGBT). However, the main difference is appreciated in the on-state losses, where the IGBT generates 1428W more than the IGCT (852W).

Once the power losses are evaluated, the thermal budget on the components has to be checked. In both cases, water-cooling has been considered with the same equivalent heatsink to water thermal resistance, which is technically available. Table 2-23 show the thermal parameters and the junction temperature estimated for both solutions. Attention must be paid to the power losses dissipated by IGCT, obviously the clamp circuit losses do not have to be taken into account. The water temperature is fixed at  $T_W=40^\circ\text{C}$ .

Parameter	3.3kV IGBT	3.3kV IGCT
Junction to case thermal resistance $R_{TH(J-C)}$	8.5 K/kW	8.5 K/kW
Case to heatsink thermal resistance $R_{TH(C-S)}$	9 K/kW (only IGBT) 6 K/kW (module)	3 K/kW (double side cooled)
Heatsink to water thermal resistance $R_{TH(S-W)}$	4 K/kW	4 K/kW
Power to dissipate	5080 W	2712 W
Junction Temperature, $T_{VJ}$ (water temperature $T_W=40^\circ\text{C}$ )	149.22 $^\circ\text{C}$	82.036 $^\circ\text{C}$

Table 2-23.- Thermal resistances for 3.3kV IGBTs and IGCTs (water cooling system)

It can be noticed that the IGBT is over its maximum junction operating temperature ( $T_{VJ}=125^\circ\text{C}$ ) and could not operate under these working conditions. However, the IGCT can operate safely under these working conditions thanks to a higher power dissipation capacity provided by the double sided cooling and lower power losses result of lower on-state losses and the existence of the clamp circuit.

If the junction temperature of the semiconductors is fixed to operate with a certain safe margin ( $T_{VJ}=110^\circ\text{C}$  and  $T_W=40^\circ\text{C}$ ), the maximum power that the IGBT could dissipate is 3250W, whereas the IGCT could dissipate more than 4400W, Table 2-24. Under these conditions, the IGBT module could handle output current slightly greater than 800A, while the IGCT could carry safely more than 1.6kA. That is, 2 IGBT modules in parallel would be needed to handle the same power that a single 3.3kV IGCT can handle.

	IGBT 3.3kV / 1.2kA (800A)	IGCT 3.3kV / 4kA (1.6kA)
$P_{COND}$	1280 W ( $I_C=800\text{A}$ , $\alpha = 0.5$ , $V_{CE sat} = 3.2\text{ V}$ )	1305 W ( $I_T=1.6\text{kA}$ , $\alpha = 0.5$ , $V_T = 1.63\text{ V}$ )
$E_{OFF} / P_{SW OFF}$	0.950J / 950 W	2.35J / 2350 W
$E_{ON} / P_{SW ON}$	0.910 J / 910 W	0.16 J / 160 W
$E_{TOT} / P_{SW TOT}$	1.86 J / 1860 W	2.51 J / 2510 W
$P_{TOT}$	3140 W	3815 W

Table 2-24.- 3.3kV IGCT (1.6kA) – IGBT (800A) power losses evaluation ( $E=1.5\text{kV}$ ,  $f_{SW}=1\text{kHz}$ ,  $\alpha=0.5$ )

The low on-state losses and high power losses evacuation properties of the 3.3kV IGCT open the possibilities to increase the operating frequency of the semiconductor keeping the switching current relatively high (over 1kA). Table 2-25 shows the estimated current limits of the 3.3kV IGCT operating at 2kHz. In this extrapolation the total power losses are kept constant (around

4.4kW), and then maximal switching current is derived (always considering chopper mode operation with duty cycle  $\alpha=0.5$ ). Depending on the DC input voltage, the DC output current could vary between 1kA and 1.4kA. In all cases the switching losses are dominant, with a switching losses to on-state losses ratio ranging from 3.6 to 6.

$f_{sw} = 2\text{KHz} (\alpha = 0.5)$					
Voltage (V)	$I_{OUT}$ (A)	$P_{SW}$ (W)	$P_{COND}$ (W)	$P_{TOT}$ (W)	$K = P_{SW} / P_{COND}$
1200 V	1400A	3530 W	976 W	4506 W	3.6
1500 V	1200A	3660 W	787.2 W	4447.2 W	4.83
1800 V	1000A	3710 W	620 W	4330 W	6.0

Table 2-25.- 2kHz LV IGCT extrapolated working conditions.

## 2.6 Conclusions

Practical characterisation results of experimental ABB 3.3kV IGCTs are presented in this chapter. The characterisation process is carried out on a specially developed test bench applying the so-called Opposition Method. This test bench allows operating and evaluating the performances of the semiconductors under real working conditions (continuous switching operation, cooling system, gate driver, etc.).

Characterisation results show the capability of the 3.3kV IGCTs to manage high currents at high switching frequencies in hard switching operation, keeping the power losses at acceptable levels. Experiments were performed at 1kHz and 1.3kA for a DC input voltage of 1.2kV (IGCT driver power supply limitation). The 3.3kV IGCTs were also driven to the maximum current and voltage ratings of the test bench (DC output current,  $I_{OUT}=2\text{kA}$  and DC input voltage  $E=1.5\text{kV} \Rightarrow 3\text{MW}$ ) with a switching frequency of  $f_{SW}=500\text{Hz}$ .

With the obtained characterisation results, a simple comparison in chopper mode operation show the ability of the 3.3kV IGCT to handle more than twice the power that a commercially available 3.3kV IGBT module is able to manage operating at 1kHz. Also, future prospects were extrapolated for operation at  $f_{SW}=2\text{kHz}$ , concluding with controlled currents higher than  $I_{OUT}=1\text{kA}$ . However, these prospects consider that the IGCT gate unit and its power supply are adapted for operation at 2kHz, which nowadays is limited to 1kHz.

## Potential Applications for 3.3 kV IGCTs

### 3.1 Introduction

The 3.3kV IGCT characterisation results demonstrate how the performance of this semiconductor can be used to complement and extend the existing Medium Power Converters application field, mainly providing a component that can handle higher currents (over 1kA) at high switching frequencies (over 1kHz). However, as the current market dealing with 3.3kV semiconductors is covered by the commercially available IGBTs and the IGCT technology is less popular for the greatest part of power converter manufacturers, the market introduction of the 3.3kV IGCTs depends only on commercial issues and market potentials. For these reasons, research efforts are dedicated to pointing out potential power converter topologies and applications where the use of 3.3kV IGCT utilisation could present interesting advantages.

The 3.3kV IGCT characteristic that must be mainly exploited is the low on-state losses of the component. Consequently, the best-suited applications for the use of such components are those where high currents have to be handled. Since the power losses budget of the component is mainly driven by the switching losses, for applications where relatively high switching frequencies are needed, topologies where the on-state losses are dominant should be favoured.

According to the previous considerations, the semiconductor's power losses distribution can be used as the first element to clear up which applications and topologies are convenient for the use of 3.3kV IGCTs. As the number of applications and topologies to analyse can be very vast, a Universal Power Losses Estimator for 3.3kV IGCTs switching cells is developed. The proposed estimator is based on the ideal switches simulation approach and can be applied in every converter where a generic switching cell (voltage unidirectional and current reversible) can be identified, which lightens the power losses evaluation process. Furthermore, the estimator is designed to consider relevant factors that influence the losses distribution on high power converters such as output current ripple, DC link voltage fluctuations, over-modulation and closed loop operation.

The applicability analysis of the 3.3kV IGCTs has been focused on specific medium power applications related to the French railway network (SNCF). Two particular applications have been considered, active filtering for the 1.5kV DC railway network substations, and reactive power compensation for the single-phase 25kV/50Hz railway network. For each application, different conversion structures and topologies have been analysed and briefly compared using the semiconductor power losses distribution as the main element of comparison. These analyses provide a detailed overview of the possibilities that the 3.3kV IGCTs can provide in distribution applications where high current and high switching frequency converters can be required.

## 3.2 Universal Power Losses Estimator

In most cases, any energy conversion function using static power converters (drives, power supplies, distributed power generation systems, active filtering, reactive power compensation, etc.) can be accomplished by means of several converter topologies using different semiconductor technologies. The selection of the conversion structure and semiconductors to be used is carried out mainly regarding the power of the system together with other features imposed by the application (static and dynamic performances, efficiency, ruggedness and reliability, volume and weight, cost, maintenance criteria, etc.). Last years developments in power semiconductors [CAR-98] (IGCT, HV IGBT, etc.) and topologies [MEY-98] (voltage or current source inverters, multilevel converters, AC/AC direct converters, soft switching converters, etc.) provide a wide spectrum of possibilities.

The power losses in semiconductors have a direct influence on the performances of the converter. In fact, it is normally the junction temperature of the semiconductors who limits the switching frequency, the output power of the converter, the cooling system and the number of components to use (parallel and/or series association). At the same time, the switching frequency imposes the bandwidth of the converter, the weight and size of passive components. Therefore, especially in medium and high power applications, the amount of power losses in the semiconductors can be considered as the first important criterion that allows highlighting the advantages and disadvantages of each technology / topology. It can be used as an interesting parameter to compare the suitability of the available different solutions for the concerned applications, helping to define which semiconductor technology / converter topology is best suited for a specific application. Nevertheless, the final adopted solution usually requires additional criteria depending in the case to case conditions (cost, development efforts, market relevance, etc.).

In our study, it is intended to find applications and topologies where the use of the experimental 3.3kV IGCT can improve the global performances of the system. Independently from the application, all power converters consist of several basic switching cells arranged to provide the desired energy conversion between two sources, [CHE-92]. As the number of concerned solutions can be immense, the evaluation of the semiconductor power losses on each conversion structure can be a hard task to complete. To simplify the task, a "universal" power losses evaluation tool for generic switching cells (unidirectional voltage and bi-directional current) is developed. This tool can be easily adapted to evaluate the semiconductor power losses when they are used in different topologies where a generic switching cell can be identified. Furthermore, the estimator takes into account the effect of output current ripple and the DC link voltage variations, which are relevant in high power converters. Also, closed loop operation and continuous conduction of the components for more than one switching period (hereafter called over-modulation operation) is taken into account.

### 3.2.1 State of the Art for Semiconductor Power Losses Estimation

The power semiconductor's losses estimation is a very important stage in the developing phase of a power converter. This estimation allows defining the requirements of the cooling system, but can be also used to optimise the semiconductor or topology selection depending on the dimensioning criteria imposed by the application such as higher efficiency or higher switching frequency (volume reduction, higher bandwidth, etc.). Several estimation approaches can be used, each one applying certain assumptions that define the accuracy of the power losses

estimation. A classification of the most commonly used techniques for power losses estimation is presented in the following paragraphs.

### 3.2.1.1 Analytic estimation

The analytic estimation technique makes use of analytic formulations to describe the switching and on-state averaged losses as well as the thermal conditions of the semiconductor, mainly in PWM operation [BER-95], [SCH-04]. The results are obtained instantaneously, which is useful to quickly change the working conditions of the converter (switching frequency, DC link voltage, output current, output frequency, modulation index, semiconductor characteristics and so on). Some semiconductor manufacturers provide free access to analytic estimation tools for classic 3-phase / 2-level voltage source inverter [ABB-c], [EUP-a] using directly the database containing the characteristics of their components. However, this kind of tools generally does not take into account the closed loop operation of the converter, the output current ripple or the DC link voltage fluctuations. They are mainly intended to make a quick pre-selection of the components adapted to a very specific application.

### 3.2.1.2 Estimation applying ideal switches simulation

The ideal switches simulation approach reproduces the power converter operation dealing with ideal models of semiconductors (binary resistor). Furthermore, the simulation integrates an estimation tool that uses the instantaneous currents and voltages generated by the simulated power converter to obtain the averaged power losses of the semiconductors. Sometimes, experimental evaluation test benches are developed to identify the on-state and switching losses parameters of semiconductors operating under specific working conditions (junction temperature, voltage, hard / soft switching, etc.), [MUN-00], [HIR-01]. These values are then used as input parameters for the estimation subsystem. Also, the thermal model of the component and its cooling system can be simulated to verify its functionality in case of complicated load profiles, overload conditions, etc.

The main advantage of this estimation technique is the use of the real input and output current and voltage waveforms of the converter (current ripple, closed loop effect, input voltage change, etc.). Moreover, the computation time and the size of the output files are quite acceptable. Such a kind of estimator does not usually consider the thermo-electric iteration of the semiconductor parameters.

### 3.2.1.3 Estimation applying real semiconductor models simulation

Finally, real semiconductor models can be used to simulate the real behaviour of semiconductors in a power converter (physical model, behavioural models, electro-thermal iteration models, etc.), [WON-96], [HEF-91], [MA-93], [HEF-93]. Using these models, the real and complex behaviour of the semiconductors is simulated, providing the instantaneous switching and on-state waveforms. Mathematical treatment of these waveforms leads to the instantaneous power and energy losses evaluation. The main difficulty of these models is the identification of the required parameters to run the simulation. Sometimes, the identification can be performed using the datasheets of the semiconductor [EVA-a], [LAU-a], other times it is the semiconductor manufacturer who provides directly the semiconductor physical model, [SIG-97]. Also, the external circuit parameters where the semiconductor is to be used (parasitic inductors, capacitors, etc.) need to be evaluated. The simulation results are accurate, however, the computation time and the size of the simulation files become too big when simulations of several tens of milliseconds are compulsory. Also, simulation

convergence problems can appear when the system complexity increase (number of real model components, non linear behaviour, etc.).

## 3.2.2 Description of the Proposed Universal Power Losses Estimator

The “universal” power losses estimator for 3.3kV IGCTs switching cells here proposed applies the ideal switches simulation approach. The estimator uses the experimental parameters obtained in the 3.3kV IGCT characterisation process presented in Chapter 2. However, the use of this estimator could be extended to any other controlled semiconductors (GTOs, IGBTs, MOSFETs, etc.) that can take part of a generic switching cell, only the defining coefficients of their on-state and switching losses characteristics are required.

Figure 3-1 shows the synoptic of the “universal” power losses estimator. The elementary unit considered for the power losses estimator is not just a single semiconductor but the whole generic switching cell. In that way, instead of directly using the discontinuous semiconductor current and voltage waveforms, the switching cell continuous output current  $i_{sc}(t)$  and input voltage  $e_{sc}(t)$  waveforms can be used. This avoids the uncertainty of the signals amplitude and time detection during the ideally simulated switching transients, which are very simulation time step dependent. Consequently, the control signals  $u_{T1}$  and  $u_{T1c}$  are required to obtain the switching transition times where the current and voltage values must be sampled to calculate the switching and on-state losses for each component (parameterised for each semiconductor IGCT – Diode). Finally, the average value of the semiconductor power losses is calculated at the end of each switching period in synchronisation with the PWM carrier by means of the signal  $T_{sw}$ .

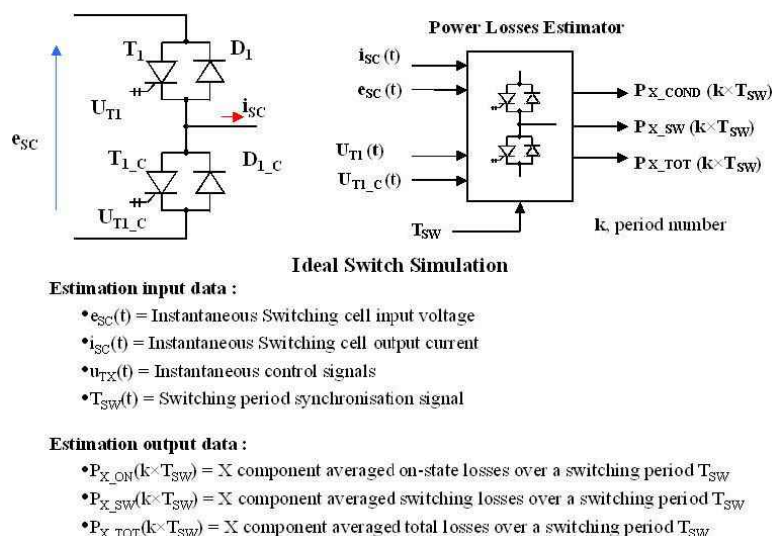


Figure 3-1.- Synoptic of the “Universal” power losses estimator.

Such a principle is applied in order to easily adapt the power losses estimator to any kind of topology where a generic switching cell (voltage unidirectional and current bi-directional) can be identified. Furthermore, this estimation structure allows considering the influence that the output current ripple, DC link voltage fluctuations, control loop and over-modulation operation can exert on the semiconductors power losses, which can be of relevance in medium and high power converters.

The simulation tool that has been used for the implementation of the “universal” power losses estimation is SABER. The use of its own programming language MAST, and particularly the use

of “state” type signals (continuous in amplitude but discrete in the time domain), allow to easily implant the proposed estimator.

### 3.2.2.1 Universal power losses estimator elements

To provide the “universal” nature to this tool, the entire estimation system is divided in 3 main parts, Figure 3-2. Specific functions of these 3 elements are explained in the following sections.

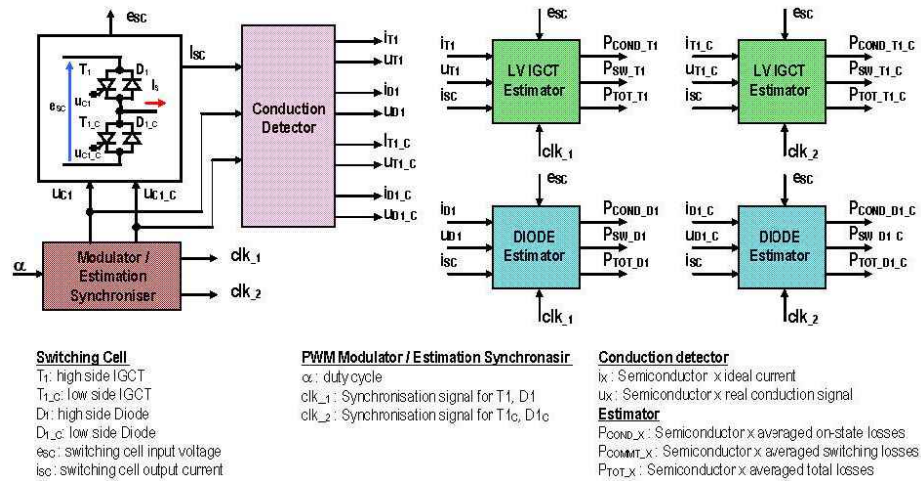


Figure 3-2.- Elements of the “universal” power losses estimator

#### 3.2.2.1.1 Modulator / estimation synchroniser

The “modulator / estimation synchroniser”, receives the duty cycle reference from the closed loop control system and provides the switching orders,  $u_{c1}$  and  $u_{c1,c}$ , to the ideal switches of the power converter. It also generates the synchronisation signals,  $clk_1$  and  $clk_2$ , which are used to perform the power losses averaging at the end of each switching period. These synchronisation signals are specially required for topologies where the components of the switching cell can remain in continuous conduction state for more than one switching period (over-modulation operation). Otherwise, the evaluation of the semiconductor on state current based on the switching transitions detection could induce relevant errors as depicted in Figure 3-3. Also, these synchronisation signals are useful when non-linear modulators are used, for example hysteresis controllers, because the switching period can vary.

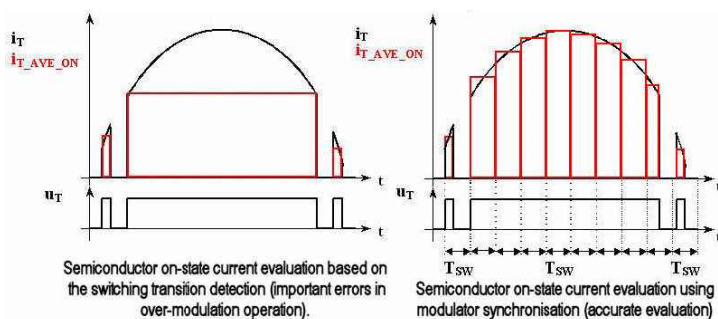


Figure 3-3.- Semiconductor on-state average current evaluation in over-modulation operation

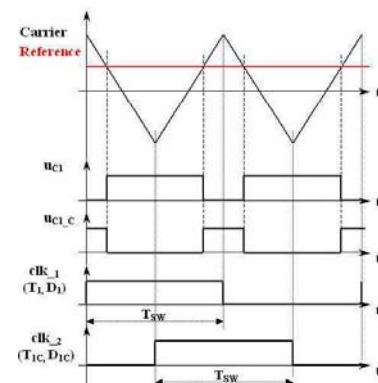


Figure 3-4.- Power losses estimator synchronisation signal generation



Each synchronisation signal is related to different switches for power losses averaging. The synchronisation signal  $clk_1$  is used for the power losses evaluation synchronisation of the high side semiconductors ( $T_1$  and  $D_1$ ) whereas the synchronisation signal  $clk_2$  is applied for their complementary low side semiconductors ( $T_{1\_C}$  and  $D_{1\_C}$ ). The generation of these signals is phase-shifted  $90^\circ$  to integrate on each estimation period both switching transitions (on and off) and the complete on-state of the component. Figure 3-4 shows the synchronisation signal generation when a classical PWM modulation patterns is used.

### 3.2.2.1.2 Conduction detector

The main function of the "conduction detector" is to derive from the switching cell current  $i_{sc}$  and the switching signals  $u_{c1}$  and  $u_{c1\_C}$  the real start / stop conduction times for each semiconductor. According to these signals, this block identify which component is really conducting, either the controlled switches or their associated antiparallel diodes. For each component, logic signals representing the state of the semiconductor ( $u_{TX}$ ,  $u_{DX}$ ,  $1 \Rightarrow$ conducting,  $0 \Rightarrow$  blocking) are generated according to the relations defined in Table 3-1. Furthermore, this block reproduces the ideal current waveforms of each switch ( $i_{TX}$ ,  $i_{DX}$ ). These signals are only used to verify the right operation of the "conduction detector" when compared with the simulated current obtained for each switch.

Conduction detector inputs			Conduction detector logical signals				Conductive element current
$i_{sc}$	$u_{c1}$	$u_{c1\_C}$	$u_{T1}$	$u_{D1}$	$u_{T1\_C}$	$u_{D1\_C}$	
$i_{sc} > 0$	0	0	0	0	0	1	$i_{D1\_C} = i_{sc}$
	0	1	0	0	0	1	$i_{D1\_C} = i_{sc}$
	1	0	1	0	0	0	$i_{T1} = i_{sc}$
	1	1	1	0	0	0	$i_{T1} = i_{sc}$
$i_{sc} < 0$	0	0	0	1	0	0	$i_{D1} = \text{abs}(i_{sc})$
	0	1	0	0	1	0	$i_{T1\_C} = \text{abs}(i_{sc})$
	1	0	0	1	0	0	$i_{D1} = \text{abs}(i_{sc})$
	1	1	0	0	1	0	$i_{T1\_C} = \text{abs}(i_{sc})$

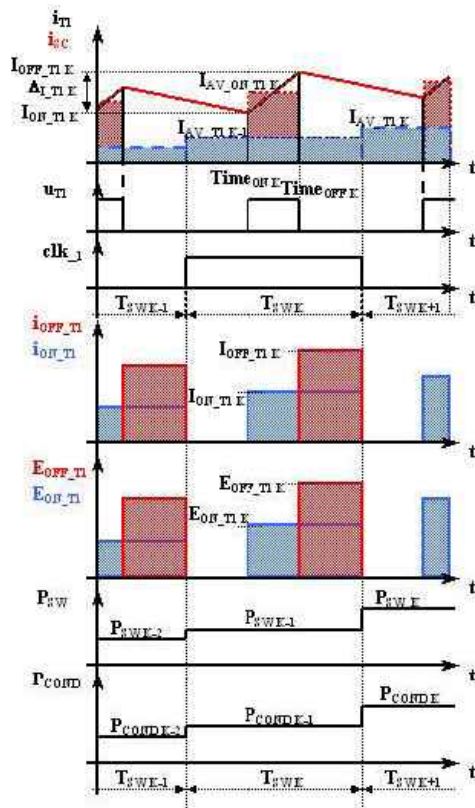
Table 3-1.- Semiconductor conduction status according to the switching cell current sign  $i_{sc}$  and the switching signals  $u_{c1}$  and  $u_{c1\_C}$

The block takes into account all the possible combinations that can be reached during the operation of the switching cell, from the dead time to the switching cell short-circuit. When a short-circuit order is generated ( $u_{c1}=1$  and  $u_{c1\_C}=1$ ), the estimator does not consider it as a default, but as a normal state of the converter where the sign of  $i_{sc}$  defines which controlled switch is conducting. Even if this operating mode is forbidden in most of the power converters, some topologies use this state consciously, that is why this state is taken into account.

### 3.2.2.1.3 Losses estimator

The "estimator" block performs the semiconductor power losses evaluation providing the on-state, switching and total power losses averaged at the switching period rate  $T_{sw}$ , ( $P_{CODN\_X}$ ,  $P_{SW\_X}$  and  $P_{TOT\_X}$ ). The estimator uses the rising and trailing edges of the conduction signals delivered by the "conduction detector" ( $u_{TX}$ ,  $u_{DX}$ ) to identify the component turn-on ( $time_{ON}$ ) and turn-off ( $time_{OFF}$ ) times. At these points, the switching cell current  $i_{sc}$  and voltage  $e_{sc}$  are sampled. At  $time_{ON}$  and  $time_{OFF}$ , the current at turn-on ( $i_{ON}$ ) and turn-off ( $i_{OFF}$ ) are assigned respectively

considering the absolute value of  $i_{sc}$ . Once this information is available, the on-state, switching and total losses calculation is performed according to the equations Eq. 3-1 to Eq. 3-10. The power losses evaluation results are obtained with a switching period delay.



$T_{SW}$ : Switching period

$\alpha$ : Semiconductor conduction time ratio

time<sub>OFF</sub>: Turn off switching time

time<sub>ON</sub>: Turn on switching time

$i_{AVE\_ON}$ : On-state averaged current

$i_{ON}$ : Current at turn on

$i_{OFF}$ : Current at turn off

$A_{ON}$ ,  $B_{ON}$ : Turn on switching losses parameters

$A_{OFF}$ ,  $B_{OFF}$ : Turn off switching losses parameters

$$E_{ON}(k) = A_{ON} \times i_{ON}(k) + B_{ON} \quad \text{Eq. 3-1}$$

$$E_{OFF}(k) = A_{OFF} \times i_{OFF}(k) + B_{OFF} \quad \text{Eq. 3-2}$$

$$P_{SW}(k) = \frac{E_{ON}(k) + E_{OFF}(k)}{T_{SW}} \quad \text{Eq. 3-3}$$

$$\alpha(k) = (\text{time}_{OFF} - \text{time}_{ON}) / T_{SW} \quad \text{Eq. 3-4}$$

$$i_{AVE\_ON}(t) = \frac{i_{ON}(k) + i_{OFF}(k)}{2} \quad \text{Eq. 3-5}$$

$$\Delta I(k) = i_{OFF}(k) - i_{ON}(k); \quad \text{Eq. 3-6}$$

$$i_{AVE}(k) = i_{AVE\_ON}(k) \times \alpha(k) \quad \text{Eq. 3-7}$$

$$[i_{RMS}(k)]^2 = \alpha(k) \times \left( [i_{AVE\_ON}(k)]^2 + \frac{[\Delta I(k)]^2}{12} \right) \quad \text{Eq. 3-8}$$

$$P_{COND}(k) = v_{X0} \times i_{AVE}(k) + r_X \times [i_{RMS}(k)]^2 \quad \text{Eq. 3-9}$$

$$P_{TOT}(k) = P_{SW}(k) + P_{COND}(k) \quad \text{Eq. 3-10}$$

$\Delta I$ : Switching current ripple

$i_{AVE}$ : Switching period averaged current

$i_{RMS}$ : Switching period RMS current

$v_{X0}$ : Semiconductor on-state threshold voltage

$r_X$ : Semiconductor on-state dynamic resistance

$P_{COND}$ : Switching period averaged on-state losses

$P_{SW}$ : Switching period averaged switching losses

$P_{TOT}$ : Switching period averaged total losses

Figure 3-5.- Power losses averaging each switching period  $T_{SW}$

The on-state losses are evaluated considering the effect of the current ripple over the component average and RMS current values.

The turn on and off switching losses are not only evaluated considering the switching current, they are also linearly extrapolated with respect to the switching voltage from several available switching energy characteristics  $E_X = f(i_X, e_{sc})$  as shown in Figure 3-6 and according to the equations Eq. 3-11 to Eq. 3-14. The turn-off and turn-on switching losses can be evaluated separately to evaluate the distribution of the switching losses on the components.

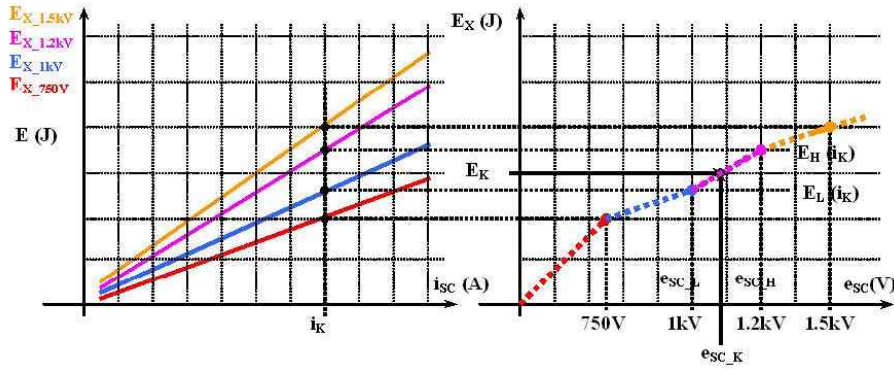


Figure 3-6.- Linear extrapolation of the switching losses energies according to the input voltage,  $e_{sc}$

$$E_H(i_k) = A_H \times i_k + B_H \tag{Eq. 3-11}$$

$$E_L(i_k) = A_L \times i_k + B_L \tag{Eq. 3-12}$$

$$m = \frac{E_H(i_k) - E_L(i_k)}{e_{sc\_H} - e_{sc\_L}} \tag{Eq. 3-13}$$

$$E_K(i_k) = E_L(i_k) + m \times (e_{sc\_K} - e_{sc\_L}) \tag{Eq. 3-14}$$

$i_k$ : Switched current at instant k (turn on or turn off)

$E_H(i_k)$ : Switching energy at voltage  $e_{sc\_H}$  and current  $i_k$ .

$e_{sc\_K}$ : Switched voltage at instant k (turn on or turn off)

$E_L(i_k)$ : Switching energy at voltage  $e_{sc\_L}$  and current  $i_k$ .

$A_H, B_H, A_L, B_L$ : Switching characteristics parameters of the component

$m$ : Semiconductor energy losses characteristic slope between  $e_{sc\_H}$  and  $e_{sc\_L}$  at  $i_k$ .

$e_{sc\_H}$ : High side closest voltage to  $e_{sc\_K}$  at which the switching characteristic is available

$E_K(i_k)$ : Extrapolated switching energy at transient k (turn on or turn off)

$e_{sc\_L}$ : Low side closest voltage to  $e_{sc\_K}$  at which the switching characteristic is available

### 3.2.2.2 Universal power losses estimator validation

To verify the proper operation and accuracy of the power losses estimator, the operation of the opposition method test bench for the characterisation of the experimental 3.3kV IGBTs presented in Chapter 2 is simulated, Figure 3-7.

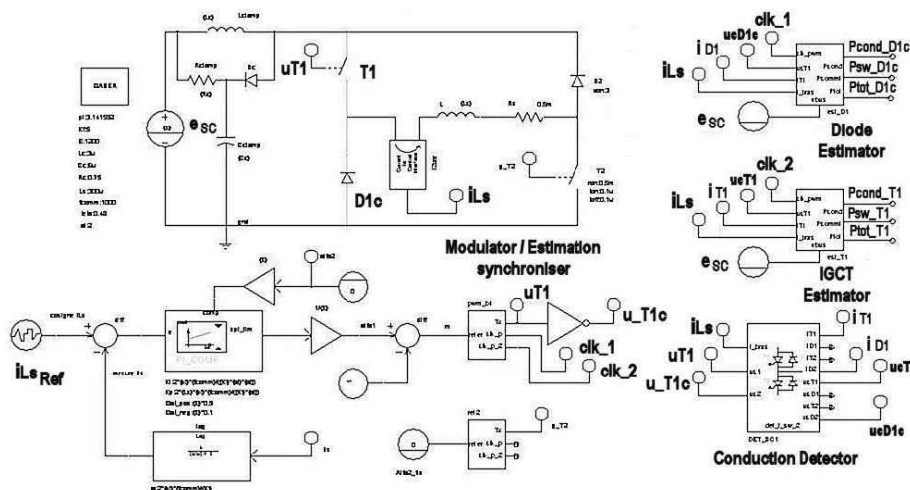


Figure 3-7.- Simulation of the characterisation test bench for 3.3kV IGBTs

The simulation considers the closed loop operation of the converter and the influence of the clamp circuit. The input voltage is modelled by an ideal voltage source. The power losses estimation is applied to the IGCT and the diode of the first switching cell, (T1 and D1c), which requires the generation of the switching control signals ( $u_{T1}$  and  $u_{D1c}$ ) even if there is no low side controlled switch, and both synchronisation signals ( $clk\_1$  for T1 and  $clk\_2$  for D1c). Figure 3-8 depicts the simulated power losses estimation results when the DC link voltage is 1.2kV, the output DC current reference is 1.2kA and the switching frequency is fixed to 1 kHz.

The first 3 signals of Figure 3-8 represent the synchronisation signal, the switch control signal, and the IGCT conduction detection signal. In this configuration, the control signal and the conduction detection signal are the same because the IGCT conducts as long as the control signal is activated, otherwise the diode of the switching cell conducts.

Note then the output current waveform (DC plus current ripple) over the current reference. Around these waveforms, the turn-on and turn-off current values used by the “universal” estimator for T1 are shown. At every step change on the conduction detection signal, the estimator acquires the switching current (and voltage) that is going to be used for evaluation of the switching losses as well as for the average and RMS current of the semiconductor. At the end of the synchronisation period (rising or trailing edge of the synchronisation signal) the average on-state, switching and total losses are calculated. Also, the estimator turn-on and turn-off currents become 0 to be ready for acquisition of the values in the next step.

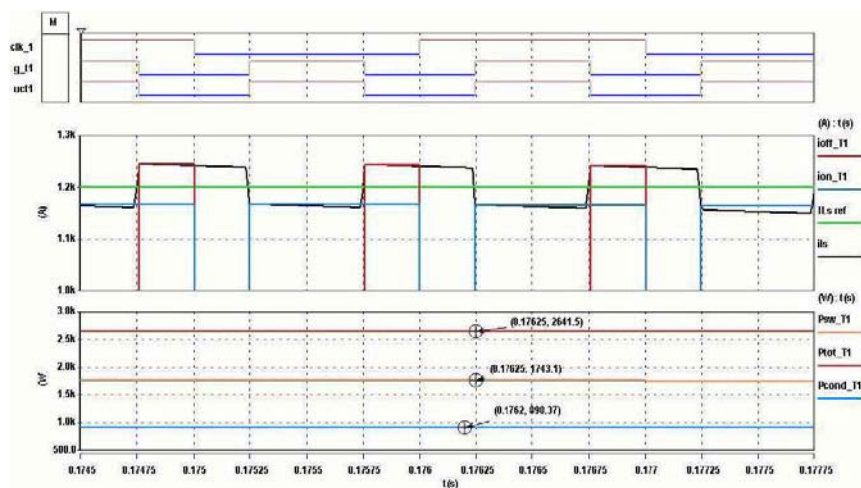


Figure 3-8.- Verification of the power losses estimator operation. Opposition method test bench ( $E=1.2\text{kV}$ ,  $I_{LS}=1.2\text{kA}$ ,  $f_{sw}=1\text{kHz}$ )

The 3 last waveforms show the values of the obtained on-state, switching losses and total losses for T1. At DC operation, the averaged effect over these waveforms is not noticed because of the very low difference between the losses from a switching period to the next one. The experimentally measured on-state and switching losses were 900W and 1680W respectively, whereas the simulated values are 898W and 1743 W. Only a slight mismatch on the switching losses is noticeable due to the different current ripples in real operation. These results show the functionality and accuracy of the developed estimator. The estimation system is therefore validated.

### 3.3 Potential Applications for 3.3kV IGCTs

High and Medium power electronics systems are used in a wide range of different applications where electric energy must be generated, transmitted, distributed, stored and utilised. The most

important application fields where the power electronics systems are applied are Industry, Traction and Energy Management.

In the High Power range, Industry and Utility applications are dominant. HVDC transmission systems in the range of several hundred MW to more than 1GW, Static VAR Compensators (SVC), large AC/AC cycloconverters for synchronous drives, arc furnaces and chlorine and aluminium electrolysis applications up to 100MW and more are some examples. All of these applications use line or load commutated converters based mainly on thyristors, which switch only once per network cycle. However, the development of power semiconductors has also enabled the use of Back to Back (BTB) configurations based on Voltage Source Inverters (VSI) for Interties and HVDC "Light" transmissions in the range of 100MW using IGCTs or IGBTs (usually in series / parallel connection) operating at switching frequencies up to 500Hz. Unified Power Flow controllers (UPFC), Active Filters for Power Conditioning and Storage system for several MW have been already installed punctually [AKA-01], [DAN-01], [CAR-98].

In the Medium Power Range, all application fields are concerned except Transmission. A big market in Medium Voltage Drives for industrial and traction applications is already established, with power ratings ranging from several hundred kW to several MW, [BER-00]. In the electric energy generation and distribution field, the interest on power electronics solutions has increased notably during the past few years thanks to the liberalisation of the Electric market and renovated environmental and power supply quality considerations. Terms such as "Distributed Generation" [ACK-01] and "Custom Power" [HIN-98] were introduced to classify the new emerging applications. In the generation market, the growth of wind turbines application is noticeable, with important quantities and power ratings reaching 3.5MW and planning to be increased. Other technologies such as solar plants, micro-turbines and fuel cells are also being considered, but its market introduction is still far from being massive for different reasons such as cost, reliability, etc. For the distribution market, multiple solutions such as Active Filters, Static VAR Compensators (STATCOMs), Dynamic Voltage Restorers (DVR), Solid State Breakers (SSB), Solid State Transfer Switches (SSTS), Dynamic Uninterruptible Power Supplies (DUPS), etc. have been applied successfully in field and keep improving their performances and reliability thanks to the research efforts being held. However, their use is limited to applications where other more basic solutions do not fulfil the specifications imposed by the actual standards or environmental issues (e.g. dynamic performances, volume, noise, etc.). The price and complexity of these systems are also big obstacles for their relevant market introduction, which in the near future can be overcome by the use of new technologies, equipments standardisation, etc. Also, the unstoppable increase on the electric energy consumption, the saturation of the actual electric system, the widespread introduction of distributed generation systems and future standards defined to modernise the electric system are the main arguments that will stimulate and support the use of these power electronics based systems.

In the Distribution field, and more specifically regarding the French Railways electric network, two potential applications for Power Electronics systems in the Medium Power range are identified:

- Harmonic currents compensation for 1.5kV DC substations.
- Reactive power compensation for 25kV / 50Hz single-phase substations

In these applications, the use of components handling high currents at high switching frequencies could provide competitive solutions to comply with the imposed requirements. Multiple solutions could be applied (i.e. semiconductors, topologies), but here the use of the most relevant solutions based on 3.3kV IGCTs are only considered to highlight the possibilities that this component offers in such applications.

### 3.3.1 Harmonic Currents Compensation for 1.5kV DC SNCF Substations

With the railway market liberalisation, the managing task of the French railways network was divided into two public institutions, SNCF (Société Nationale des Chemins de Fer) and RFF (Réseau Ferré de France). The train operation is managed by the SNCF while RFF is the owner of the railway infrastructure and manages it. The French railway network totals around 33000km rail tracks, of which approximately 13500km are electrically energised. Of these 13500km, around 6000km use 1.5kV DC lines and the rest use 25kV/50Hz single-phase lines, Figure 3-9. Although the number of kilometres for both voltage lines is similar, the number of DC substations is considerably high compared to the number of 25kV substations. This is due to the need for higher line current values (reaching 6kA in overload mode) when trains operate under a DC line, which generates higher voltage drops on the line that require shorter distances between substations (8 to 25km compared to 35km to 90km for 25kV lines) to keep the line voltage inside the operating voltage range of the trains.

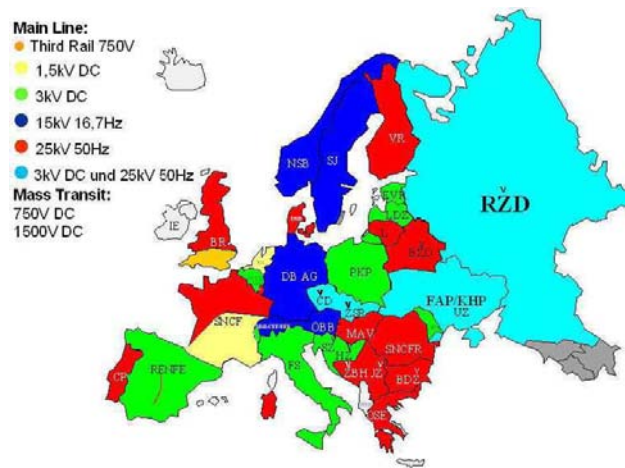


Figure 3-9.- Line voltages of the European railway networks

Not only is the voltage drop across the line a source of problems for the 1.5kV DC network, but the high harmonic current content generated on the rectifier based substations has to be limited to fulfil the standard imposed by the French public institutions for electric transmission (>63kV) RTE (Réseau de Transport d'Electricité) or electric distribution EDF (Electricité de France). In this section, the current harmonic problem on existing substations and several solutions are described and discussed.

#### 3.3.1.1 1.5kV DC SNCF Substations

The 1.5kV DC railway lines are supplied by substations usually connected to the 63kV or 90kV RTE transmission network. Internally, these substations consist basically of step-down transformers that adapt the voltage level and diode rectifiers to change the AC voltage into DC, which constitute the so-called "Traction Groups", Figure 3-10. The substations output lines are parallel connected with distances ranging from 8 to 25km depending on the train traffic and track profile.

Nowadays, the tendency for increasing the rail freight traffic (FRET) can require line current values up to 7kA, which can generate several hundred volt voltage drop between two substations and impede trains to work at their nominal rating. Under these circumstances, an intermediate substation can be installed. However, cost and environmental reasons complicate the access to

the 63kV or 90kV network and only connection to the 20kV network is available. This implies that the amount of current harmonics that will be generated must be taken into serious consideration.

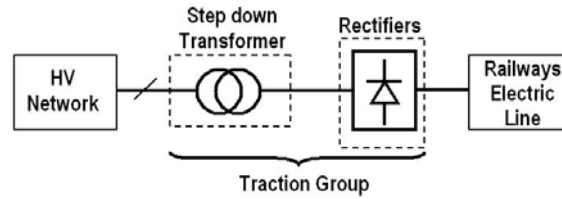


Figure 3-10.- SNCF 1.5kV DC substation synoptic

The current harmonic content must be limited to the specific values imposed by the electric transmission manager (RTE or EDF), otherwise penalties have to be suffered. For this application, the limits are well defined and better detailed in the low harmonic order range than in the IEEE 519 standard, "Recommended Practices and Requirements for Harmonic Control in Electric Power Systems".

Depending on the substation input voltage different regulations applies, [FAL-04]. Two voltage domains are concerned:

- HTA ( $1\text{kV} < U_{\text{HV}} < 20\text{kV}$ ): In this voltage domain, and for contracted powers  $P_{\text{REF}}$  higher than 100kVAR, the "n" order harmonic currents  $I_{\text{HV}_N}$  are limited according to the Table 3-2 and Eq. 3-15.

Even harmonics, n	2	4	>4	-	-
$K_N$	2	1	0.5	-	-
Odd harmonics, n	3	5 & 7	9	11 & 13	>13
$K_N$	4	5	2	3	2

Table 3-2.- Harmonic limits for the HTA voltage domain,  $P_{\text{REF}} > 100\text{kVAR}$

$$I_{\text{HV}_N} = K_N \cdot \frac{P_{\text{REF}}}{\sqrt{3} \cdot U_{\text{HV}}} \quad \text{Eq. 3-15}$$

$U_{\text{HV}}$ : Contracted Voltage;  $P_{\text{REF}}$ : Contracted Power;  $K_N$ : n order harmonic limit coefficient;

- HTB ( $U_{\text{HV}} > 20\text{kV}$ , usually 63kV and 90 kV): For the HTB domain the current harmonics limits are fixed by Table 3-3 and Eq. 3-16.

Even harmonics, n	2	4	>4	-	-
$K_N$	3	1.5	1	-	-
Odd harmonics, n	3	5 & 7	9	11 & 13	>13
$K_N$	6.5	8	3	5	3

Table 3-3.- Harmonic limits for the HTB voltage domain,  $P_{\text{REF}} > 100\text{kVAR}$

$$I_{\text{HV}_N} = K_N \cdot \frac{S_S}{\sqrt{3} \cdot U_{\text{HV}}} \quad \text{Eq. 3-16}$$

$U_{\text{HV}}$ : Contracted Voltage;  $S_S$ : Contracted Apparent Power;  $K_N$ : n order harmonic limit coefficient;

As the  $K_N$  harmonic current coefficients indicate, the tolerated harmonic currents are higher when the substation connection is made to the HTB domain. However, the cost of the connection to the HTB domain network is much more expensive than for the HTA (ratio close to 10), which makes

more attractive the use of network connections in the HTA domain. Also, the HTB networks are not always accessible where a substation is to be installed.

Considering the use of HTA network connections (20kV), a mean to allow higher harmonic current absolute values is increasing the contracted power. However, from an economic point of view, it is not acceptable to increase the contracted power in order to avoid penalties while the power consumption does not require such a contract. In that case, other solutions for harmonic current content reduction are required.

Regarding the existing step-down transformer and rectifier configuration, different arrangements are employed. The type of substation is identified by a three-character code defining the nominal power of the installation, the arrangement of the rectifiers and the diode housing, Table 3-4.

Substation Identifier					
1 <sup>st</sup> Identifier	Nominal Power	2 <sup>nd</sup> Identifier	Rectifier Configuration	3 <sup>rd</sup> Identifier	Diode Housing
A	3000 kW	1	Single bridge	v	Modules
B	5000 kW	2	Double bridge	p	Press pack
C	6600 kW	3	Double bridge - series	-	-
-	-	4	Double bridge - parallel	-	-

Table 3-4.- SNCF 1.5kV DC substations identification

The configuration mainly applied is the 12-pulse double bridge – series arrangement depicted in Figure 3-11. In that case the diodes of each 3-phase rectifier conduct the total load current  $I_L$  and the railways line voltage  $U_L$  is shared. To allow the safe series connection of both rectifiers, a six-phase system is generated by means of the star-triangle ( $\perp$ - $\Delta$ ) transformer secondary windings arrangement. The primary is usually arranged in star configuration. To share equally the output voltage on each rectifier, the transformation ratio between the primary and each secondary must be adapted according to Eq. 3-17. For a given high voltage side phase to phase input voltage  $U_{HV}$ , the average railways line voltage is defined by Eq. 3-18.

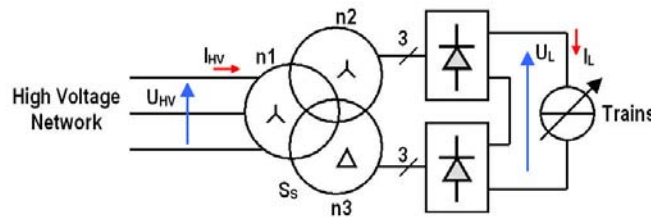


Figure 3-11.- Double bridge –series (12-pulse) rectifier configuration

$$m_{\Delta} = \sqrt{3} \cdot m_{\perp}; \quad m = m_{\perp}; \quad \text{Eq. 3-17}$$

$$U_{L\_AVE} = \frac{6 \cdot \sqrt{2} \cdot m \cdot U_{HV}}{\pi} \quad \text{Eq. 3-18}$$

$$m_{\perp} = \frac{n_2}{n_1}; \quad m_{\Delta} = \frac{n_3}{n_1}; \quad \begin{array}{l} U_{HV} = \text{High Voltage side phase to phase RMS voltage} \\ U_{L\_AVE} = \text{Railways electric line average voltage} \end{array}$$

Considering the ideal behaviour of the rectifier, the high voltage side phase current waveform is shown in Figure 3-12. In that case, the harmonic current content worst case is considered as described by Eq. 3-19. Only harmonics of order  $(12 \cdot K \pm 1)$  exist and their amplitude is inversely proportional to the order of the harmonic.



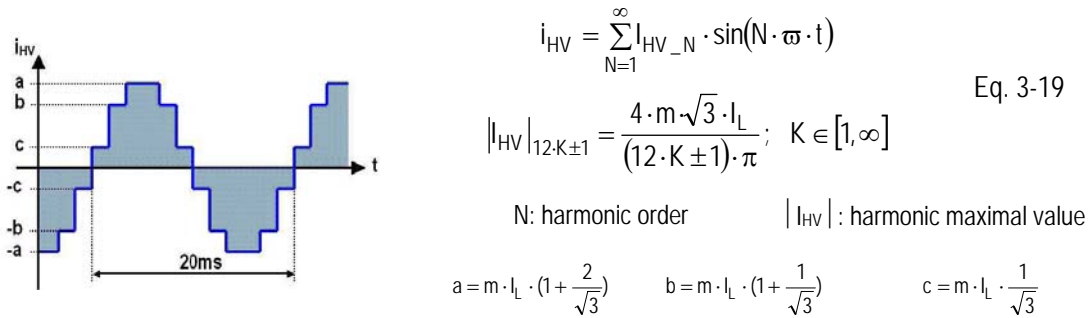


Figure 3-12.- High voltage side phase current waveform for 12-pulse rectifiers

For a contracted power of 8MVAR for a connection to the 20kV network, the evolution of the four first relevant harmonics (11<sup>th</sup>, 13<sup>th</sup>, 23<sup>rd</sup>, and 25<sup>th</sup>) with the load power consumption considering the rectifier ideal behaviour is shown in Figure 3-13. According to this figure, the imposed harmonic current limits are already exceeded for power consumption around 2.5MW.

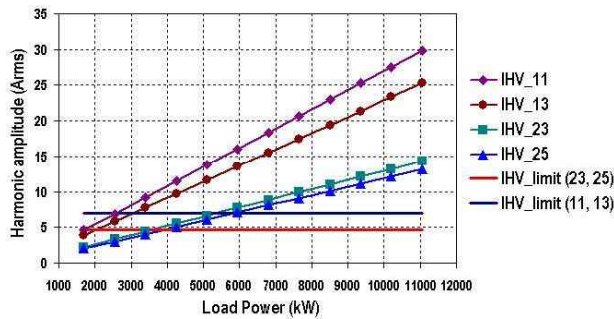


Figure 3-13.- DC substation input current 11<sup>th</sup>, 13<sup>th</sup>, 23<sup>rd</sup>, 25<sup>th</sup> harmonic evolution, (Ideal 12 pulse rectifier)

Compared to the idealised current steps of Figure 3-12, the current evolution is limited by the real diode commutation process on the rectifier, thus the current harmonic content is reduced. Because of this effect, the input current RMS value is also reduced and the reactive power consumption is increased. Analytical and simulation analyses demonstrate that the harmonic content reduction mainly depends on the rectifier switching impedances (mainly the network and transformer leakage inductance) and also on the load current value. Circuit simulations results that consider the rectifier real behaviour are shown in Figure 3-14, [FAL-04]. The harmonic current content is considerably reduced mainly at high load power values. However, the harmonic current limits are still exceeded for low power values (3MW) compared with the contracted power (8MVAR). It is important to point out that only the 11<sup>th</sup> and 13<sup>th</sup> harmonics exceed the imposed limits. The 23<sup>rd</sup> and 25<sup>th</sup> harmonics are always below their maximum limit.

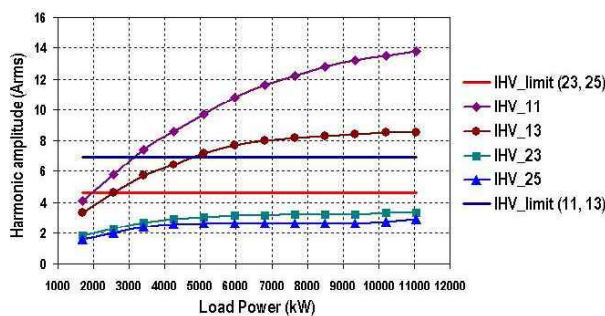
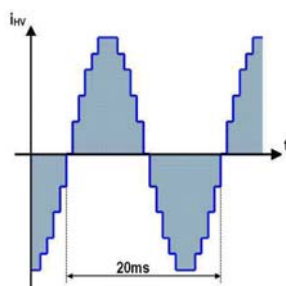


Figure 3-14.- DC substation input current 11<sup>th</sup>, 13<sup>th</sup>, 23<sup>rd</sup>, 25<sup>th</sup> harmonic evolution, (simulation results)

This analysis claims the need for harmonic filtering in the 1.5kV DC SNCF substations, which can be provided by several means. The classical solution consists of using bulky passive filters tuned at the harmonic frequency to be compensated. However, lower order filters are often required in order to prevent possible parallel and series resonance between the passive filter and the source impedance, which can be excited by source distortion or by load current residual non characteristic harmonics, [DBA-01]. Other possible power electronics based solutions are analysed in the following sections using the 3.3kV IGCT as the referred semiconductor. This analysis considers  $I_L=6\text{kA}$  as the maximum load current reachable in overload operation (10MW).

### 3.3.1.2 24-pulse diode rectifier

Applying the same philosophy of the 12-pulse rectifier with respect to the 6-pulse rectifier, increasing the number of pulses eliminates undesirable harmonics. In the case of a 24-pulse rectifier, only harmonics of order  $(24 \cdot K \pm 1)$  are generated, Eq. 3-20. Furthermore, the order of magnitude of the first relevant harmonics (23<sup>rd</sup> and 25<sup>th</sup>) is similar to these harmonics in the 12-pulse case (half the transformer turns ratio). In that way, the obstacle presented by the 12-pulse rectifier could be overcome as no additional filtering would be required.



$$i_{HV} = \sum_{N=1}^{\infty} I_{HV\_N} \cdot \sin(N \cdot \omega \cdot t) \quad \text{Eq. 3-20}$$

$$|I_{HV}|_{24 \cdot K \pm 1} = \frac{8 \cdot m \cdot \sqrt{3} \cdot I_L}{(24 \cdot K \pm 1) \cdot \pi}; \quad K \in [1, \infty]$$

N: harmonic order  
 $|I_{HV}|$ : harmonic maximal value  
 m:  $\perp$ - $\perp$  transformer turns ratio  
 $I_L$ : Load current

Figure 3-15.- High voltage side phase current waveform for 24-pulse rectifiers

To apply a 24-pulse rectifier, a 12-phase voltage system must be generated. That can be obtained by means of four times 3 phase transformers arranged to provide  $15^\circ$  phase shift between each three phase system reference. Several configurations of the four 3-phase rectifiers can be utilised, however the parallel configuration requires output inductors in the DC side to equilibrate the current sharing between each rectifiers, which favours the use of the series configuration.

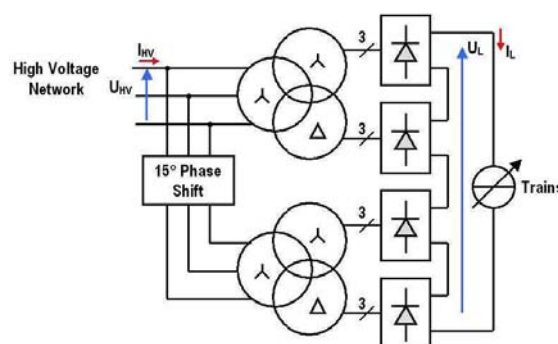


Figure 3-16.- Double bridge-series (12-pulse) rectifier configuration

For this solution, the main problem arises when the 12-phase system must be generated. The use of special secondary combinations (zig-zag, series connection, etc.) is required to obtain the desired  $15^\circ$  phase shift, which leads to transformer higher cost. Furthermore, the use of such a system in the existing installations will require replacing the full traction group, which is not

affordable in all cases. Therefore, this possibility could be interesting only for new installations. Moreover, the higher cost compared with the standard installations enable the chance of considering other more sophisticated solutions currently available, such as active filtering and active rectification.

### 3.3.1.3 Active filtering using 3.3kV IGCTs

The principle of active filtering for harmonic current compensation basically applies shunt structures where power electronic systems are connected to the network in parallel with a polluting load, Figure 3-18. The shunt-connected converter behaves as a controlled current source compensating the harmonic currents generated by the polluting non-linear load ( $\sum I_{hN}$ ).

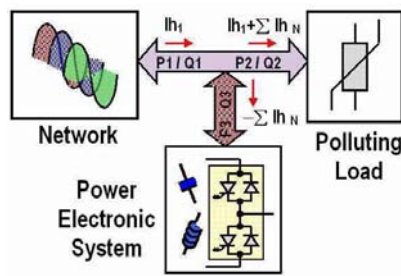


Figure 3-18.- Shunt compensation principle

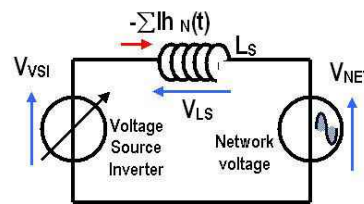


Figure 3-17.- Network current harmonic injection principle based on VSI

The current injected by the power converter to the network must be exactly the harmonic current generated by the non-linear load but in the opposed direction ( $-\sum I_{hN}$ ). In this way, the network will only provide the fundamental current term ( $I_{h1}$ ) demanded by the load. This action avoids the generation of harmonic voltages on the line, which could disturb other loads connected to the same line. Applying the same compensation principle, such a structure can also provide reactive power compensation functions. In such a case, the current generated by the power converter must compensate the load current term responsible of the reactive power demand. The main goal of such operation is the optimisation of the network utilisation by maximising the active power transfer and the control of the network voltage, avoiding effects such as flicker.

To obtain the controllable current source behaviour previously mentioned, mainly Voltage Source Inverters (VSI) are employed. The inverter voltage is controlled to impose the injection current on the link inductor  $L_S$  and thus on the network, Figure 3-17. The voltage drop on the inductor must be seriously considered, Eq. 3-21, because it will define the maximum inverter voltage required to compensate the concerned harmonic current. As the inductor impedance increases with the frequency, high harmonic current demands will result in high inverter voltage values, which are limited by the power semiconductor blocking capability. So, the inductor value must be chosen as small as possible. In turn, the inductor value should be as high as possible to limit the high frequency inductor current ripple induced by the switching mode operation of the converter. An appropriate trade off must be found depending on the applied topology and the harmonic current values to be compensated.

$$V_{VSI}(t) = V_{NET}(t) + \sum_{N=2}^{\infty} N \cdot L_S \cdot \omega \cdot I_{hN}(t) \quad \text{Eq. 3-21}$$

$\omega$ : network fundamental pulsation

For harmonic and reactive power compensation, as no active power consumption is demanded by the converter (except the power losses), no additional power source or storage element is needed, simply a DC capacitor is required. The capacitance value of the DC link capacitor must be specified to keep the voltage ripple under reasonable limits.

### 3.3.1.3.1 Active filtering structures for 12-pulse rectifiers

For a 12-pulse rectifier, the active filtering function could be applied either on the transformer primary side or on the secondary side. If compensation of the harmonics is performed on the secondary side, two compensation sets for three-phase systems will be required. Furthermore, each compensation system should handle currents with values equal to the load current (6kA) at low voltage levels and with higher harmonic contents. Therefore, from a converter design point of view, the best-suited compensation point is the primary side, Figure 3-19. The problem here is the need for a coupling transformer to adapt the 20kV network voltage to voltage levels that can be handled by the power semiconductors. However, the drawback of a coupling transformer can become an advantage if the additional degrees of freedom provided by the different transformer arrangements are exploited to obtain a better use of the power semiconductors.

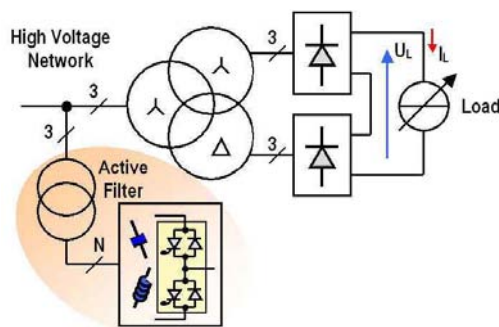


Figure 3-19.- Active filter position for a 12 pulse rectifier

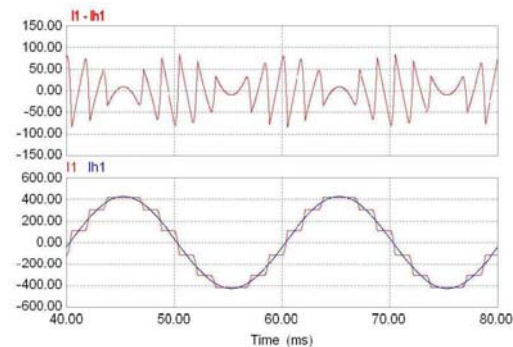


Figure 3-20.- Harmonic current waveform generated by a 12 pulse rectifier ( $U_{HV}=20\text{kV}$ ,  $I_L=6\text{kA}$ )

Regarding the performances of the power converter to be applied, an important requirement is "bandwidth", which is imposed by the harmonics to compensate, mainly the 11<sup>th</sup> and 13<sup>th</sup> in that case (550 and 650Hz respectively). Furthermore, high dynamic current changes present in the total harmonic current waveform are to be compensated, Figure 3-20, which increases the bandwidth requirements even more. This means that high "apparent" switching frequencies are required, typically between 3 and 10 times the bandwidth frequency.

If the application of classical 3-phase VSIs is considered, Figure 3-21, switching frequencies around 4kHz would be required to obtain enough dynamic performances. Furthermore, low inverter phase voltage levels would be obtained (for a DC bus of 1.8kV, maximum 600V<sub>RMS</sub>) and thus high current values would be necessary to provide the desired compensation. However, as the maximum inverter output current is limited by the inductance voltage drop for a given network voltage, paralleling of "n" inverters would be required to split the total harmonic current to be compensated. Parallel configuration of "n" inverters will require the use of "n" secondary windings and thus more complicated and costly arrangements.

If a classic three phase coupling transformer windings are decoupled and used as single-phase transformers, the use of 3 single-phase full bridge converters is possible, Figure 3-22. In this way, the inverter output voltage per phase can be doubled as well as the output apparent switching frequency if unipolar PWM modulation is used. With IGBTs operating at 2kHz, the apparent switching frequency will be 4kHz. Obviously, the number of switching cells to be used is also doubled.

Another interesting solution to increasing the harmonic current compensation capability and to increasing the apparent switching frequency without increasing the semiconductor switching frequency is the use of multi-cell converters, either series or parallel, [PCA-96] [DAV-97]. In these structures, the modulation carriers applied to generate the switching cells switching orders are

interleaved to increase the apparent output switching frequency and to generate multilevel (current or voltage) waveforms. These properties allow increasing the available converter bandwidth and reducing the amplitude of the switching frequency related harmonics generated by the inverter (passive filter reduction). Considering the high current handling ability of the 3.3kV IGCTs and the high current values to be compensated on this application, multi-cellular parallel structures are preferred, although series or mixed series-parallel structures could be also considered.

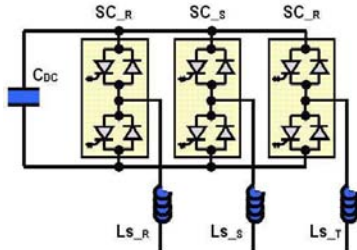


Figure 3-21.- Three-phase VSI

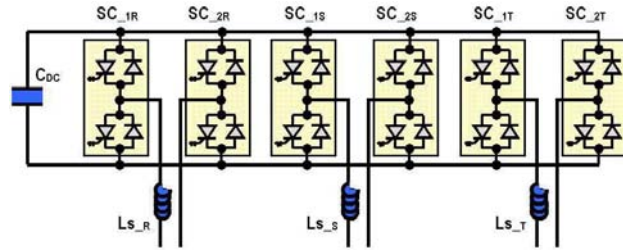
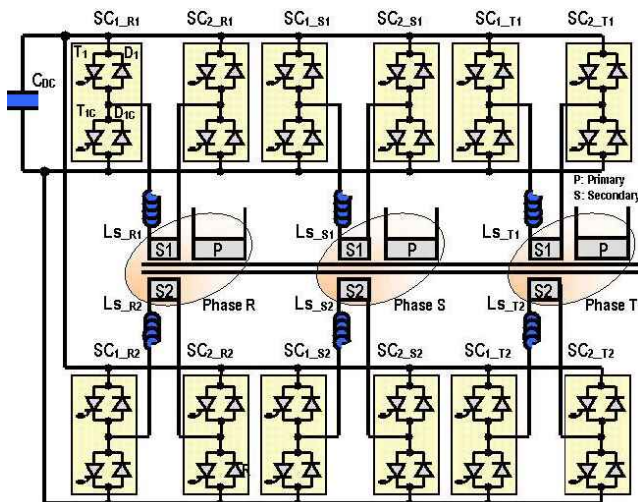


Figure 3-22.- 3xSingle-phase VSI

Other multiple structures with similar characteristics can be also considered (Neutral Point Clamped multilevel converters (NPC), Cascaded Inverters, Hybrid converters, etc., [MEY-98], [ROD-02], [STE-01b]). However, instead of considering all these relatively complex structures, it is interesting to value the use of the simple and well known parallel arrangement of “n” interleaved single-phase inverters, which is possible in this application thanks to the almost compulsory presence of the coupling transformer. Using “n” interleaved single-phase inverters for each network phase provides high bandwidth capability and also modularity properties to the conversion structure. In addition, the use of semiconductors with high current and high switching frequency capabilities, such as the 3.3kV IGCT, allows minimising the number of inverters to parallel.



$$\theta = \frac{\pi}{n} \quad \text{Eq. 3-22}$$

for even values of “n”

$$\theta = \frac{2 \cdot \pi}{n} \quad \text{Eq. 3-23}$$

for odd values of “n”

“n”: numbers of paralleled single-phase inverters per phase

$\theta$ : interleaving angle between carriers

Figure 3-23.- Conversion structure with “n” paralleled single-phase inverters per network phase, n=2

Each single-phase inverter requires its own secondary winding as it is shown in Figure 3-23 (n=2). A common DC link capacitor  $C_{DC}$  can be used for compensation of the three phases. A smoothing inductor for each single-phase inverter is also required, which will be submitted to an apparent switching frequency twice the switching cells switching frequency  $f_{sw}$ . Depending on the number of single-phase inverters to be paralleled, the interleaving carrier angle  $\theta$  must be

adapted according to Eq. 3-22 and Eq. 3-23. In that way the total apparent switching frequency will be “2·n” times  $f_{sw}$  on the primary side.

Applying the same conversion principle, an additional possibility that minimises the part count of the converter is to apply the harmonic compensation on the phase to phase voltages and not on each single-phase of the network. Obviously, this strategy is only effective if the three-phase system is equilibrated (network side and load side) and higher current values per inverter are feasible compared with the single-phase compensation solution. Also, the use of three-phase transformers is not possible, so two single-phase transformers with “n” secondary windings will be required, Figure 3-24.

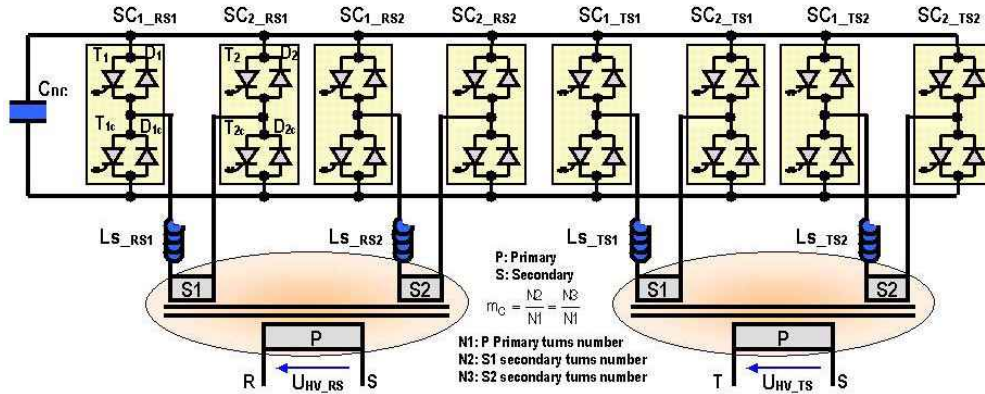


Figure 3-24.- Structure with “n=2” paralleled single-phase inverters for phase to phase compensation

### 3.3.1.3.2 “n” paralleled single-phase inverter solution (phase to phase)

If the use of 3.3kV IGBTs is considered, the maximal DC link voltage is limited to 1.8kV to guarantee a FIT (failure in time) rate of 100 due to the effects of cosmic rays. Therefore, using unipolar modulation, Figure 3-25, the maximum average voltage that can be generated by the inverter is around 1620V (1145  $V_{RMS}$ ) when the switching cell duty cycle is limited to  $\alpha_{MAX}=0.95$ , Eq. 3-26. For this maximum inverter voltage and to handle the harmonic compensation current values imposed by the application, a trade off between the compensation transformer turns ratio  $m_c$ , the smoothing inductor value  $L_s$  and the number of single-phase inverters to parallel “n” must be reached. The inverter maximum output voltage attainable guides the selection of these parameters.

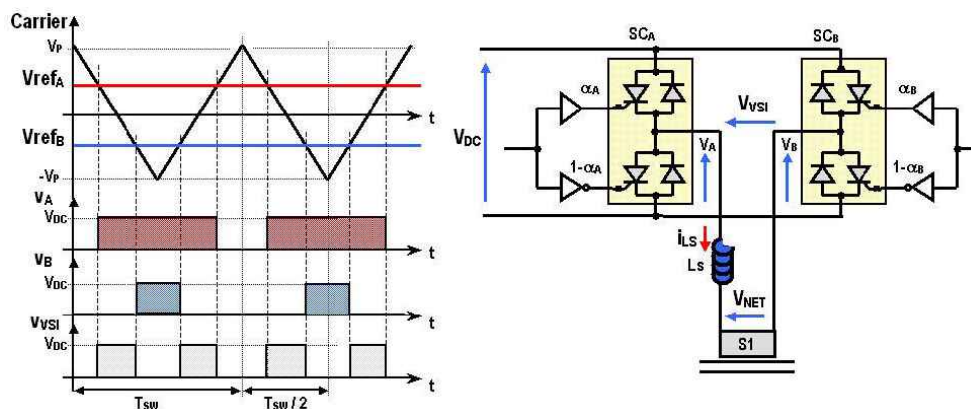


Figure 3-25.- Unipolar modulation for single-phase inverters,  $V_{VSI} > 0$

$$m_A = \frac{V_{refA}}{V_P}; \quad \alpha_A = \frac{1}{2} \cdot (1 + m_A); \quad <V_A> = V_{DC} \cdot \alpha_A \quad \text{Eq. 3-24}$$

$$m_B = \frac{V_{refB}}{V_P}; \quad \alpha_B = \frac{1}{2} \cdot (1 + m_B); \quad <V_B> = V_{DC} \cdot \alpha_B \quad \text{Eq. 3-25}$$

$$<V_{VSI}> = V_{DC} \cdot m_A = V_{DC} \cdot (2 \times \alpha_A - 1) \quad \text{Eq. 3-26}$$

$$V_{refA} = -V_{refB}; \quad m_A = -m_B; \quad \alpha_A = 1 - \alpha_B; \quad m_X \in \{-1, 1\}; \quad \alpha_X \in \{0, 1\};$$

For the selection of  $m_C$ ,  $L_S$  and “ $n$ ”, the harmonic currents maximum values must be considered. The steady state inverter voltage expressions are derived from Eq. 3-27 to Eq. 3-32 if only the 11<sup>th</sup> and 13<sup>th</sup> harmonics are considered. In this case, Figure 3-26 shows the voltage and current waveforms that the inverter must ideally generate to compensate completely the 11<sup>th</sup> and 13<sup>th</sup> harmonics generated by the 12-pulse rectifier.

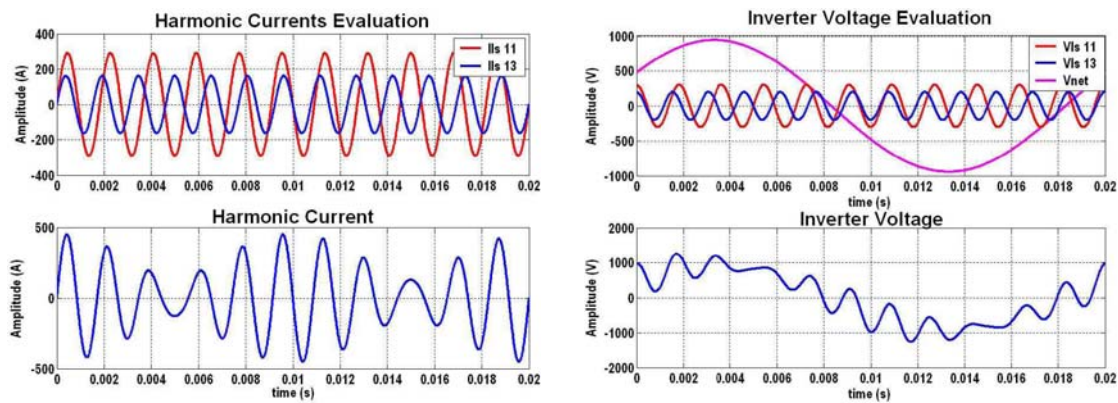


Figure 3-26.- Single-phase inverter steady state voltage and current for 11<sup>th</sup> and 13<sup>th</sup> harmonic compensation ( $V_{DC}=1.8\text{kV}$ ,  $m_C=1/30$ ,  $L_S=300\mu\text{H}$ ,  $n=2$ )

$$I_{LS\_11} = \frac{I_{HV\_11}}{n \cdot m_C} \cdot \sin(11 \cdot \omega \cdot t) \quad \text{Eq. 3-27}$$

$$I_{LS\_13} = \frac{I_{HV\_13}}{n \cdot m_C} \cdot \sin(13 \cdot \omega \cdot t) \quad \text{Eq. 3-28}$$

$$V_{LS\_11} = 11 \cdot L_S \cdot \omega \cdot \frac{I_{HV\_11}}{n \cdot m_C} \cdot \cos(11 \cdot \omega \cdot t) \quad \text{Eq. 3-29}$$

$$V_{LS\_13} = 13 \cdot L_S \cdot \omega \cdot \frac{I_{HV\_13}}{n \cdot m_C} \cdot \cos(13 \cdot \omega \cdot t) \quad \text{Eq. 3-30}$$

$$V_{NET} = U_{HV} \cdot m_C \cdot \sin(\omega \cdot t + \frac{\pi}{6}) \quad \text{Eq. 3-31}$$

$$V_{SI} = V_{LS\_11} + V_{LS\_13} + V_{NET} \quad \text{Eq. 3-32}$$

As multiple combinations of  $m_C$ ,  $L_S$  and “ $n$ ” can fulfil the compensation requirements, graphical evaluation of the maximum inverter voltage and current for different parameter combinations is used to determine a selection criterion. The first relevant conclusion of the analysis is that a solution with a minimum of  $n=2$  inverters is required. The use of only one inverter per phase will require higher DC voltages and the use of 3 inverters will increase considerably the part count of the structure. Figure 3-27 shows the analytically evaluated maximal inverter voltage and current values with different values of the transformer turns ratio  $m_C$  and the smoothing inductor  $L_S$  for an

arrangement with two single-phase inverters per phase to phase voltage,  $n=2$ . As it can be seen, several combinations allow the operation with voltage levels lower than the maximum inverter voltage available with a DC link of 1.8kV.

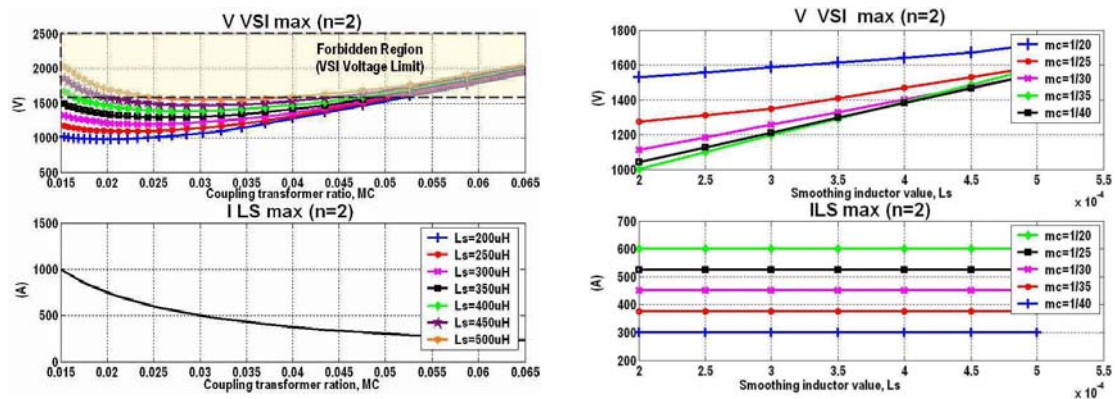


Figure 3-27.- Maximum inverter voltage and current evolution depending on  $m_c$  and  $L_s$  for “ $n=2$ ”

The next assertion that can be made when analysing the Figure 3-27 is that above a certain value of  $L_s$  ( $L_s \approx 500\mu\text{H}$ ), more than the maximum voltage provided by the inverter is required. Thus, the inductor voltage must be chosen lower than this value. Then, for any  $L_s$  under this value, minimisation of the maximum inverter current could be used as criteria for the selection of the transformer turns ratio  $m_c$ . However, the current ripple on the smoothing inductor and the controller closed loop operation are phenomena that exert influence on the selection of the transformer ratio and must be carefully considered.

- $\Delta I_{L_s}$ ,  $L_s$  current ripple: Several complications arise when dealing with high current ripples. Higher current ripples induce higher losses on different elements of the converter. Obviously, higher copper and magnetic losses will be generated on the inductor and transformer, but also on the power semiconductors (on-state and switching). Furthermore, unacceptable acoustic noise could be generated. For these reasons, it is convenient to minimise the current ripple value by increasing the inductor value for a defined switching frequency and DC link voltage. However, cost, weight and size issues have to be also taken into account when selecting the inductor value.

$$\Delta I_{L_s} = \frac{V_{DC}}{8 \cdot f_{SW} \cdot L} \quad \text{Eq. 3-33}$$

The classical expression derived from DC/DC choppers current ripple evaluation is usually applied to estimate the current ripple value under certain conditions, Eq. 3-33. However, this expression assumes that the low frequency output voltage and inductor current are constant throughout the switching period, which is not the case when switching frequencies close to the frequency of the signals generated by the inverter are employed. Inductor current and voltage low frequency terms influence on the current ripple is analysed analytically on Appendix 1, obtaining more accurate current ripple evaluation results. However, use of circuit simulation for validation of the analytical results show that the closed loop controller behaviour exerts also influence on the current ripple and should be taken into account.

- Closed loop controller: Ideally, the closed loop controller tries to reach the steady state operation condition of the system. However, when the steady state concerns waveforms with sudden changes, the controller response is limited by its inherent



bandwidth and by the limits of the steering magnitude that acts over the variable that is to be controlled (the inverter voltage in our case). If this magnitude reaches saturation limits, the controller can lose control and in the worst case run into instability. As consequence, a certain margin with respect to the steady state operation must be provided.

The previous considerations lead to the use of circuit simulations including the closed loop controller to select definitively the parameters to be used. Multiple and sophisticated control techniques can be employed for the harmonic content detection and controller function implementation, [DBA-01]. As these techniques are not the main interest of this study, here a simple harmonic detection system using second order filters, PI controllers with disturbance compensation (the network voltage in this case) and reference phase compensation (leading phase compensator) are employed, (see section 4.3.1.2). Only the current loop (smoothing inductor  $L_S$  current) is taken into account, considering the DC link voltage as an ideal voltage source (slow dynamics of the DC link voltage controller). Also, ideal switches simulation is applied considering the effects of practical modulators (switching cell dead time generation and controller signal sampling). The switching cells switching frequency is selected to be 2kHz.

Obviously, the first parameter selection is carried out taking into consideration the steady state characteristics shown in Figure 3-27. Firstly, an intermediate inductor value is selected trying to get a trade off between the current ripple and the size (volume and weight) of the inductor,  $L_S=300\mu\text{H}$ . Then several transformer turns ratio  $m_C$  values are simulated to check the system proper operation.

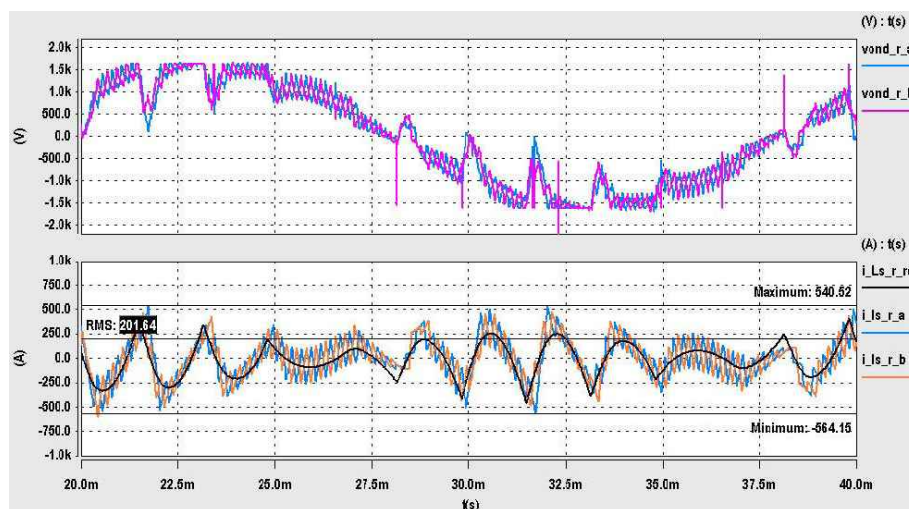


Figure 3-28.- Inverter compensation current reference, output current and controller output voltage ( $n=2$ ,  $L_S=300\mu\text{H}$ ,  $m_C=1/20$ )

Figure 3-28 shows the controller output signal (inverter voltage reference) sent to the modulator together with the inverter current reference ( $L_S$  inductor current) and both inverters output currents for a transformer turns ratio  $m_C=1/20$ . As it can be noticed, the voltage reference runs into saturation (1.62kV), which in principle does not disturb excessively the current control. Also, interleaving operation of the converters modulation can be noticed.

Figure 3-29 and Figure 3-30 show the simulation results for  $m_C=1/25$  and  $1/30$  respectively, both results proffering no controller saturation. The main quantitative difference between both operation conditions is the lower peak and RMS current values required at higher transformer turns ratio  $m_C=1/25$ . Table 3-5 compiles the simulation results regarding inductor peak and RMS currents.

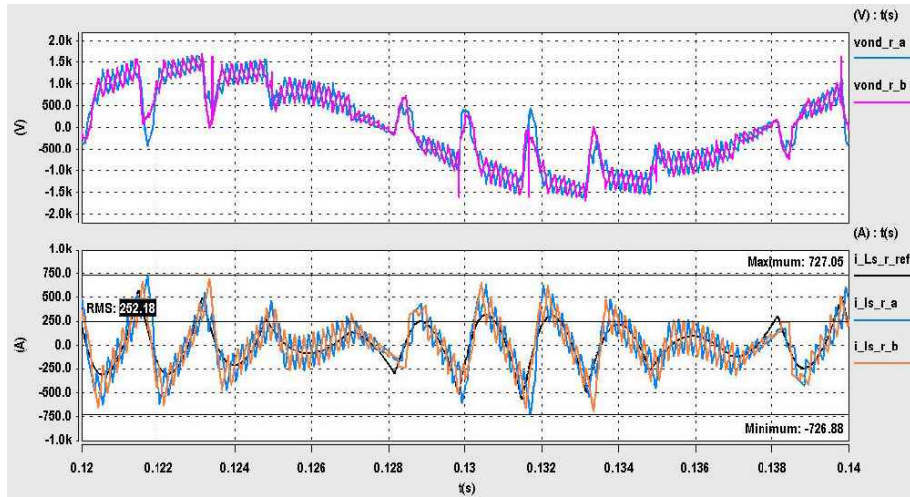


Figure 3-29.- Inverter current reference, current and controller output voltage ( $n=2$ ,  $L_s=300\mu\text{H}$ ,  $m_c=1/25$ )

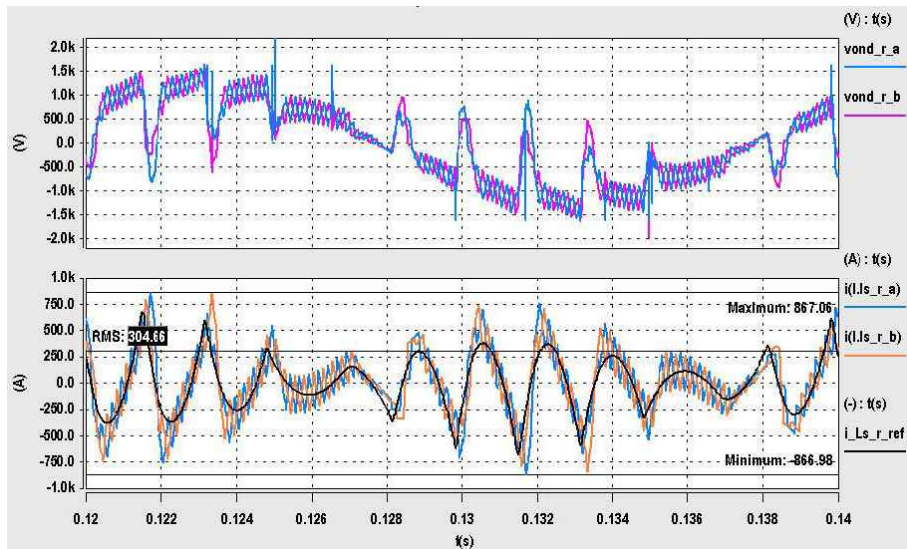


Figure 3-30.- Inverter current reference, current and controller output voltage ( $n=2$ ,  $L_s=300\mu\text{H}$ ,  $m_c=1/30$ )

Regarding the current ripple value, it is not easy to define a percentage ratio for quantitative comparison between each operating condition. However, qualitatively, if comparing defined current sections for each operation condition, slight reduction of the current ripple can be noticed at lower transformer turns ratio.

Transformer turns ratio, $m_c$	Primary Voltage (ph-ph)	Secondary Voltage	Inductor $L_s$ current	
			RMS	Peak
1 / 20	20 kV <sub>RMS</sub>	1 kV <sub>RMS</sub>	202A <sub>RMS</sub>	564A
1 / 25	20 kV <sub>RMS</sub>	800 V <sub>RMS</sub>	252A <sub>RMS</sub>	727A
1 / 30	20 kV <sub>RMS</sub>	666.6 V <sub>RMS</sub>	305A <sub>RMS</sub>	867A

Table 3-5.- Inductor  $L_s$  current values (RMS and peak) for  $m_c=1/20$ ,  $1/25$  and  $1/30$ .

As final result of the parameters selection process, the following values are retained favouring the current ripple minimisation:

$$L_s = 300\mu\text{H}$$

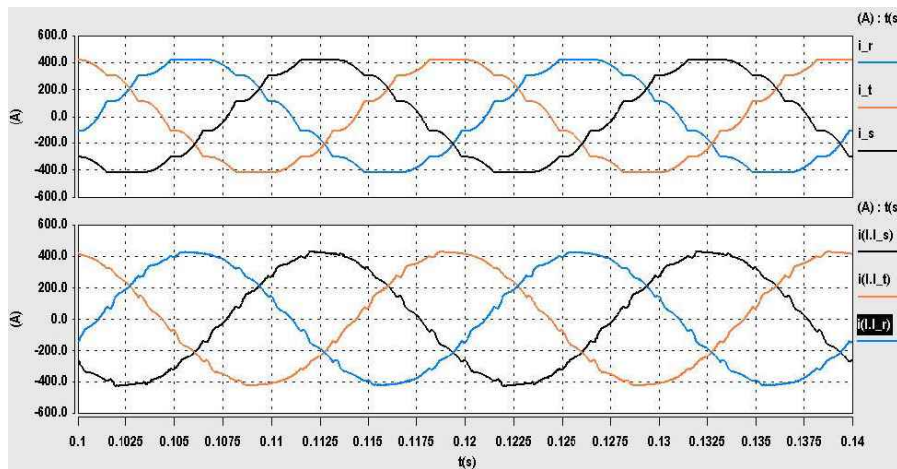
$$n = 2$$

$$m_c = 1/30$$

With these parameters, the harmonic compensation behaviour of the converter is checked. The parameters employed for the simulation of the entire system are given in Table 3-6. The harmonic compensation performance of the system is illustrated in Figure 3-31 with the network and traction group primary side current waveforms for a load current of 6kA. The spectrum of the network current shows the obtained harmonic reduction, basically for the 11<sup>th</sup> and 13<sup>th</sup> harmonics. The maximum harmonic value of the 11<sup>th</sup> harmonic is now 12.35dB (2.93A<sub>RMS</sub>), even lower than the 23<sup>rd</sup> and 25<sup>th</sup> harmonics (around 14dB, 3.54A<sub>RMS</sub>), which comply with the limits imposed by the regulations for a contracted power of 8MVAR, Figure 3-13.

Sub-system	Parameter Description	Parameter values
Traction Group	Transformer $\perp$ - $\perp$ - $\Delta$	N1=805, N2=26, N3=45
	Transformer leakage inductance and resistor, secondary side	$L_F = 23.7\mu\text{H}$ , $R_F = 1\text{m}\Omega$
	Network equivalent inductance and resistor	$L_{\text{NET}} = 2.5\text{mH}$ , $R_{\text{NET}} = 0.137\Omega$
	Phase to phase network voltage	$U_{\text{HV}} = 20\text{kV}_{\text{RMS}}$
	Load maximum current	$I_{\text{L MAX}} = 6\text{kA}_{\text{DC}}$
Active Filter	DC link voltage	$V_{\text{DC}} = 1.8\text{kV}$
	Semiconductor maximum peak current	$I_{\text{SW}} \approx 870\text{A}$
	Smoothing inductor	$L_S = 300\mu\text{H}$
	Switching frequency	$f_{\text{SW}} = 2\text{kHz}$
	Modulator sampling frequency	$f_{\text{SM}} = 4\text{kHz}$ (2 samples per switching period)
	Coupling transformer	$M_C = 1/30$
	Controller bandwidth	$f_{\text{BW}} = 750\text{Hz}$
	PI controller parameters	$K_P = 1.413$ , $K_I = 1/T_N = 108.2$
	Notch filter parameters for reference generation	$\omega_N = 314.1592$ , $\xi = 0.7$
	Reference leading phase compensator parameters	Numerator ( $b_1 = 320\mu$ , $b_0 = 0.475$ ) Denominator ( $a_1 = 114\mu$ , $b_0 = 0$ )

Table 3-6.- Active filter simulation parameters

Figure 3-31.- Traction group primary side and network currents after active filtering ( $I_L=6\text{kA}$ )

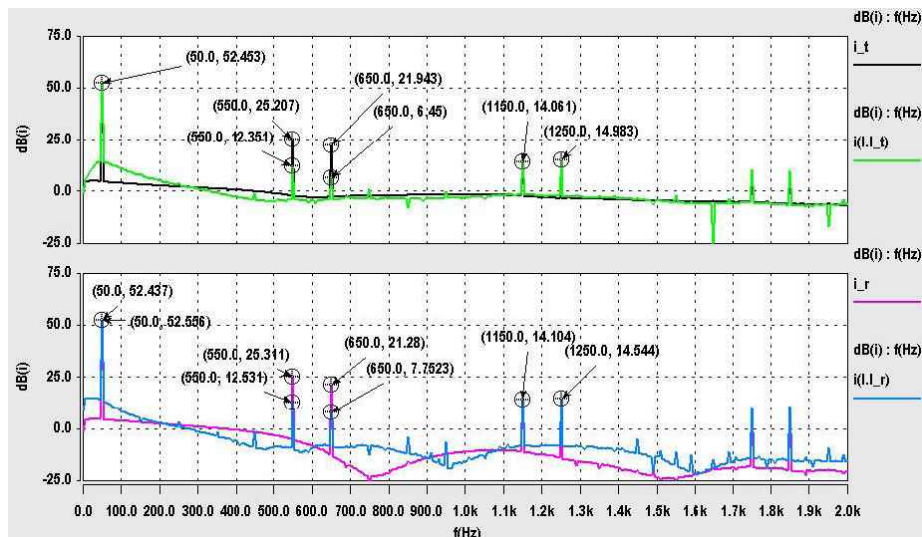


Figure 3-32.- Traction group primary side and network currents spectrum after active filtering ( $I_L=6\text{kA}$ )

Power losses evaluation of the semiconductors of an inverter is performed for several load current values applying the previously designed universal power losses estimator for 3.3kV IGCT switching cells. As it can be seen in Figure 3-33, the semiconductors are subjected to high power losses peaks (more than 4kW) corresponding with the maximum load current peaks. However, the average power losses throughout a network period are relatively low (560W). That means that in this application the semiconductor utilisation is mainly restricted for its SOA limits than for its thermal properties (a 3.3kV IGCT can dissipate more than 4kW permanently with the proper cooling system).

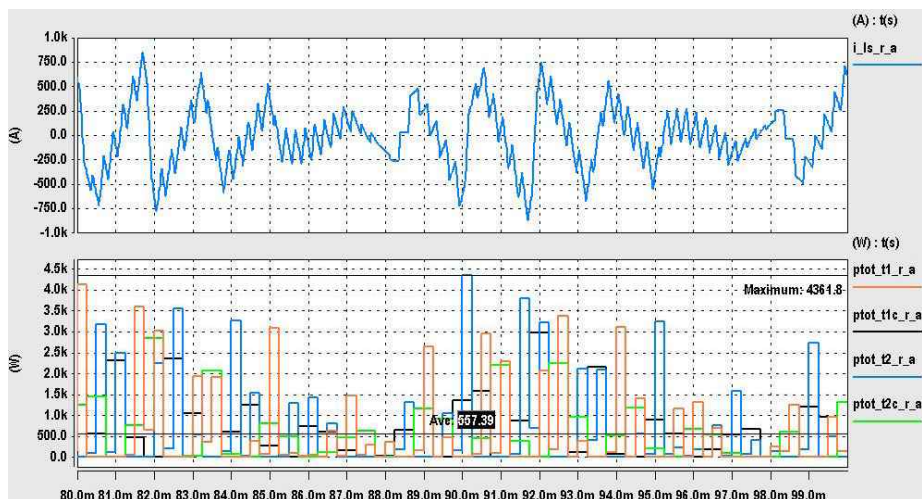


Figure 3-33.- Losses distribution on the IGCTs of an inverter throughout a network period, ( $I_L=6\text{kA}$ )

The following figures show the average semiconductor power losses distribution (switching, on-state and total) of an inverter as a function of the load current. The on-state losses are insignificant compared to the switching losses, which drive the total losses distribution. The switching cell topside IGCTs power losses are slightly greater than the losses on the bottom side IGCTs. Just the opposite behaviour is found for the diodes. The IGCTs power losses increase with the load current, whereas for the diodes this maximum is given at lower load currents and the losses remain almost constant in the whole load current range.

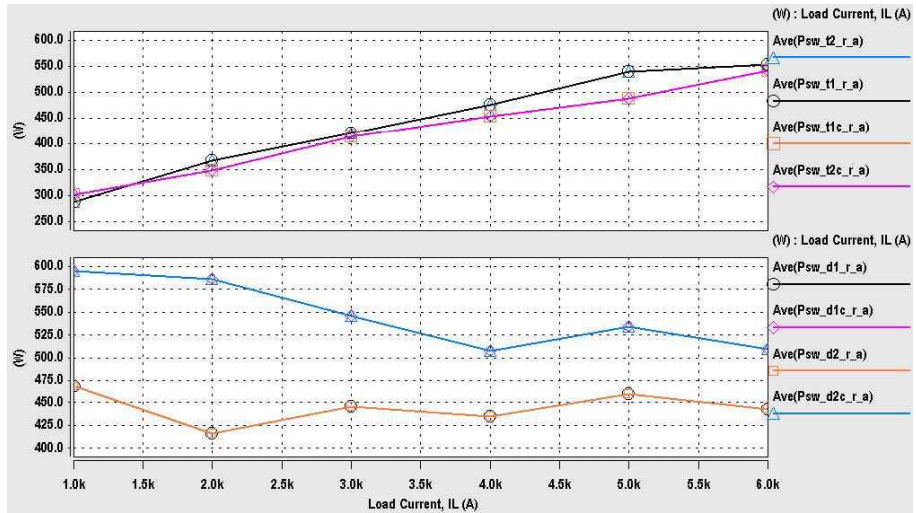


Figure 3-34.- VSI average switching losses distribution as a function of the load current,  $I_L$

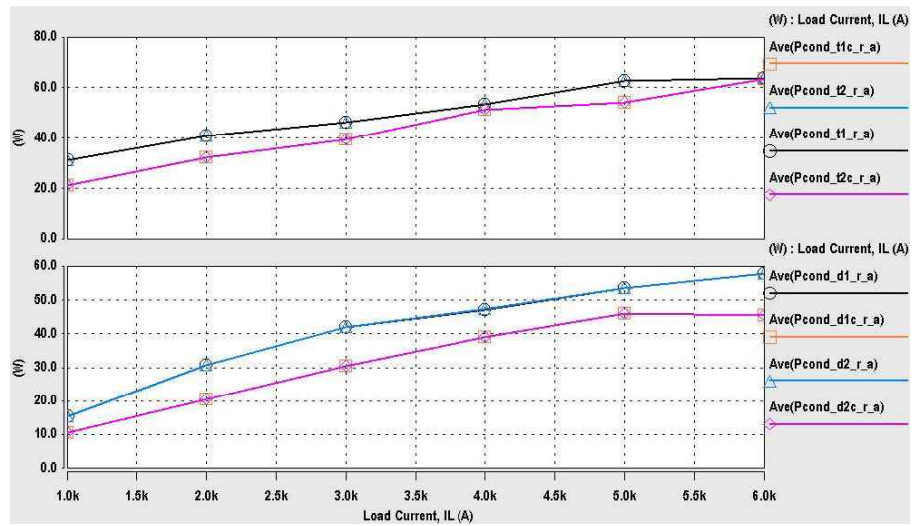


Figure 3-35.- VSI average on-state losses distribution as a function of the load current,  $I_L$

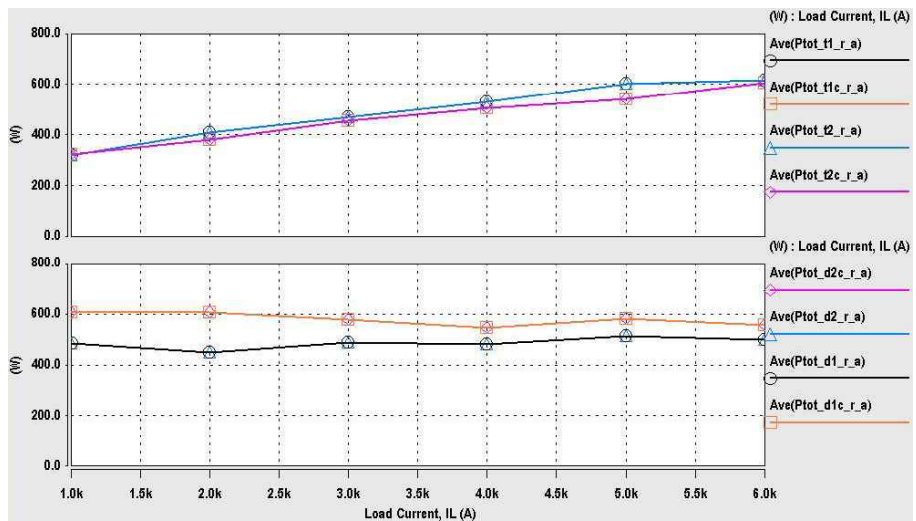


Figure 3-36.- VSI average total losses distribution as a function of the load current,  $I_L$

### 3.3.1.3.3 Active filtering solution discussion

Active filtering for SNCF 1.5kV DC substations can be accomplished by using multiple conversion structures. Here, the solution with  $n=2$  interleaved 3.3kV IGCT based single-phase inverters is analysed in detail and shows the ability of the components to handle the harmonic compensation requirements. The use of 2 single-phase inverters per phase to phase voltage is not imposed by the thermal or SOA limits of the IGCT but by the maximum voltage that can provide the converter. In such conditions the 3.3kV IGCT can be considered to be underused, but other arguments such as the use of air-cooling systems instead of using water-cooling systems could justify the use of this component. Obviously, lower semiconductor ratings could be affordable and other semiconductor technologies (3.3kV IGBT) could be also applied at the expense of higher losses per component.

If one wants better utilisation of the 3.3kV IGCT with the same dynamic performances, the use of a 3 level (multi-cell) single-phase inverter per phase to phase voltage could be used. In that way the maximum voltage level generated by the inverter is doubled and higher harmonic currents or higher transformer turns ratio  $m_c$  (higher secondary voltage) could be allowed. Also, only one inductor and secondary transformers will be required. Evidently, the number of semiconductors is the same as for the  $n=2$  proposed structure and other control (floating capacitor balance) and IGCT operation (clamp circuit) problems must be solved.

No matter which structure is used, the active filter solution guarantees the operation of the substation under the harmonics limits imposed by the regulations. Furthermore, this solution can be applied either in existing or in new substations with relatively low power requirements (less than 1MVAR at the transformer level considering the RMS current for 10MW load power). However, other issues such as cost, volume, reliability and maintenance must be taken into account when compared to other alternative solutions.

### 3.3.1.4 Active rectification using 3.3kV IGCTs

Another solution to comply with the regulations regarding the harmonic current content in the SNCF 1.5kV DC substation is to avoid the generation of harmonics. That can be accomplished by exchanging the existing 12-pulse diode rectifier, the source of harmonics, with an active rectifier with sinusoidal current consumption, Figure 3-37. The classical active rectifier solution consists of the connection of voltage source inverters between the network coupling transformer and the load to impose sinusoidal current consumption with power factor close to one. The presence of the network coupling transformer allows making similar considerations as in the previously analysed active filtering case (see 3.3.1.3.1).

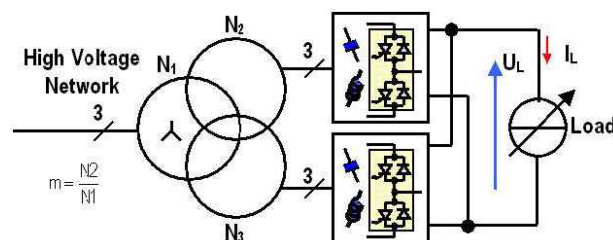


Figure 3-37.- Active rectification structure.

The solution evaluated here consists of keeping the same transformer structure of the DC substation (2 secondary windings per phase) and the use of a full bridge single-phase inverter per transformer secondary, (six single-phase inverters in total). Only the transformer turns ratio is modified,  $N_2=N_3$ . The converter is equivalent to the structure presented in Figure 3-23, but in this

case the load (trains) is connected to the DC link capacitor,  $C_{DC}$ . This solution is adopted to reach the required power ratings of the application (10MW in overload conditions), and to obtain the required bandwidth for operation with sinusoidal current consumption. Using unipolar modulation for each inverter and the interleaving strategy between the inverters related to the same primary phase, ( $n=2 \Rightarrow \theta=\pi/2$ ), a switching cell switching frequency  $f_{SW}=1\text{kHz}$  leads to a primary apparent switching frequency of 4kHz. This allows for a controller bandwidth  $f_{BW}$  around ten times bigger than the network frequency,  $f_{NET}=50\text{Hz}$ , which is enough to guarantee the expected sinusoidal current consumption.

The minimum DC link to feed the load is fixed by the nominal voltage of the substation,  $1.5\text{kV}_{DC}$ . Considering the maximum available duty cycle ( $\alpha_{MAX}=0.95$ ), the maximum inverter voltage reachable by each inverter is limited to  $1.35\text{kV}$ . Obviously, this maximum voltage should not be reached, otherwise saturation of the control system will arise and consequently current control loss. Therefore, for the selection of the smoothing inductor  $L_S$ , and the transformation ratio “m” this limit must be considered as shown in Figure 3-38.

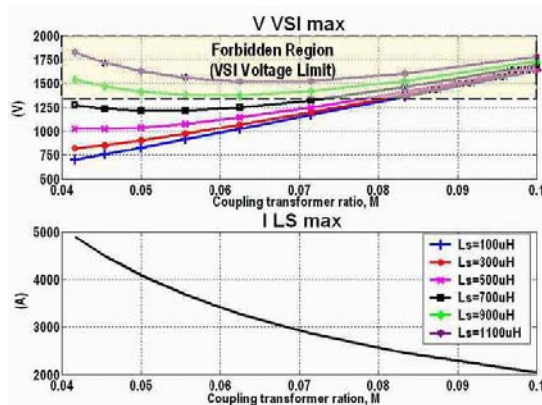


Figure 3-38.- Maximum inverter voltage and current evolution depending on  $m$  and  $L_S$  for active rectification

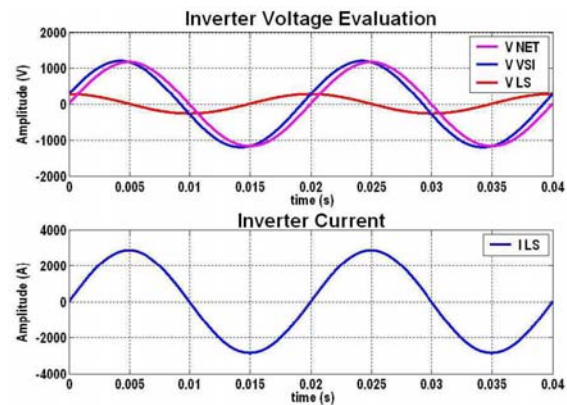


Figure 3-39.- Single-phase inverter steady state voltage and current for active rectification ( $V_{DC}=1.5\text{kV}$ ,  $m=1/14$ ,  $L_S=300\mu\text{H}$ )

For any  $L_S$  below a certain value ( $L_S \approx 700\mu\text{H}$ ) the selection of “m” is fixed by the maximum inverter current. Considering the influence of the control loop behaviour and the current ripple evaluation, a certain inverter voltage margin is required. Circuit simulation is used to select the final values employed on the performance analysis of the converter. Figure 3-39 shows the inverter voltage and current steady state waveforms with the selected parameters when 10MW are supplied to the load, ( $V_{DC}=1.5\text{kV}$ ,  $m=1/14$ ,  $L_S=300\mu\text{H}$ ).

With these parameters, the behaviour of the converter is checked by simulation. Only the current loop is simulated considering the output voltage as an ideal voltage source. The inverter current reference phase synchronisation is obtained by means of notch filters and the measure of the secondary voltage waveform, whereas the amplitude reference is derived from the secondary voltage RMS value and the power consumption to be simulated. The controller implemented is the classical PI with disturbance compensation (the secondary voltage). Table 3-7 shows the entire system simulation parameters.

Figure 3-40 shows the sinusoidal network currents obtained thanks to the active rectification for a DC link voltage of  $1.6\text{kV}$  and a load power of 10MW. The line currents are in phase with their respective line voltages providing a power factor close to 1. A slight switching current ripple derived by the switching operation can be noticed. The line currents spectrum, Figure 3-41, shows that this high frequency current ripple is located around 4kHz as expected. Also small low

frequency harmonics are generated (3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup>, etc.) due to the inverter imperfections (dead time, switching current effect on the control loop, etc.), which could be compensated by control. In all cases, the system operation complies with the current defined harmonic regulations.

Sub-system	Parameter Description	Parameter values
Active Rectifier based Traction Group	Transformer $\perp$ -(decoupled secondary windings, 2 per phase)	N1=840, N2=60,N3=60
	Network equivalent inductance and resistor	$L_{NET} = 2.5\text{mH}$ , $R_{NET} = 0.137\Omega$
	Phase to phase network voltage	$U_{HV} = 20\text{kV}_{RMS}$
	Load maximum current	$I_{L\ MAX} = 6\text{kA}_{DC}$
	DC link voltage	$V_{DC} = 1.6\text{kV}$
	Semiconductor maximum peak current	$I_{SW} \approx 3.2\text{kA}$
	Smoothing inductor	$L_S = 300\mu\text{H}$
	Switching frequency	$f_{SW} = 1\text{kHz}$
	Modulator sampling frequency	$f_{SM} = 2\text{kHz}$ (2 samples per switching period)
	Controller bandwidth	$f_{BW} = 600\text{Hz}$
	PI controller parameters	$K_P = 1.084$ , $K_I = 1/ T_{N} = 1116.7$
	Notch filter parameters for reference generation	$\omega_N = 314.1592$ , $\xi = 0.7$

Table 3-7.- Active rectifier simulation parameters

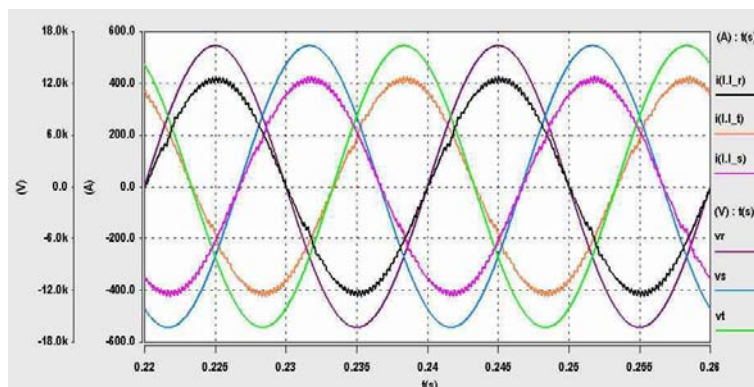


Figure 3-40.- Primary side line currents and phase to neutral voltages ( $V_{DC}=1.6\text{kV}$ ,  $P_L=10\text{MW}$ )

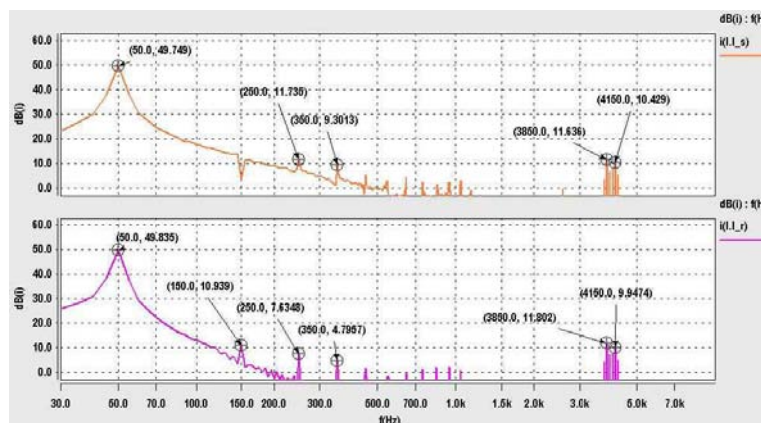


Figure 3-41.- Primary side line currents spectrum ( $V_{DC}=1.6\text{kV}$ ,  $P_L=10\text{MW}$ )



Figure 3-42 shows the inverters current waveforms when the maximum power is supplied (10MW). It can be seen that the interleaving operation of the two inverters is related to the same input voltage. A maximum peak current close to 3.2kA is attained, so the semiconductors have to admit such a peak current. Regarding the current ripple, maximum values around  $\Delta I_{LS} \approx 800A$  are identified, which in percentage is translated to be around 15% of the 50Hz current term.

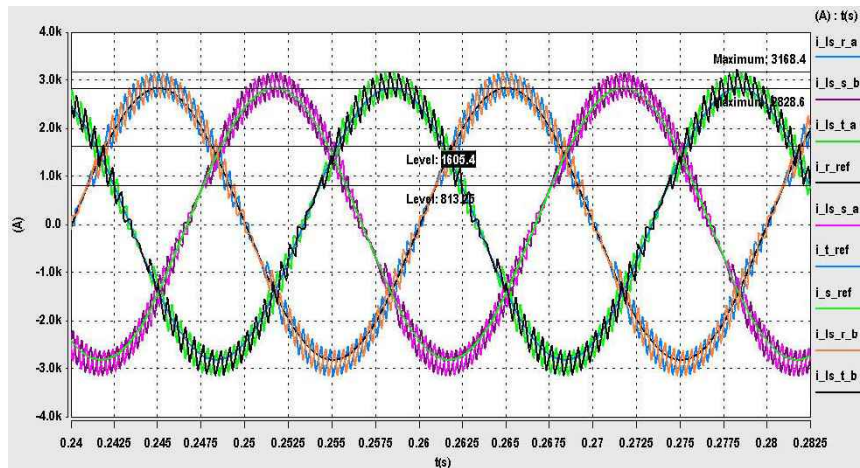


Figure 3-42.- Inverters current waveforms ( $V_{DC}=1.6kV$ ,  $P_L=10MW$ )

In such working conditions, the semiconductor power losses are evaluated to demonstrate the ability of the 3.3kV IGCTs to handle such amount of power (1.6MW per single-phase inverter). The simulation results show how the semiconductors are submitted to high power losses peaks (close to 8kW and 6kW for the diodes and IGCTs respectively) but with average power losses that can be handled by the component (around 2kW), Figure 3-43. Considering this operation mode, if the power load is increased, the SOA limit of the component will limit the maximum attainable output power.

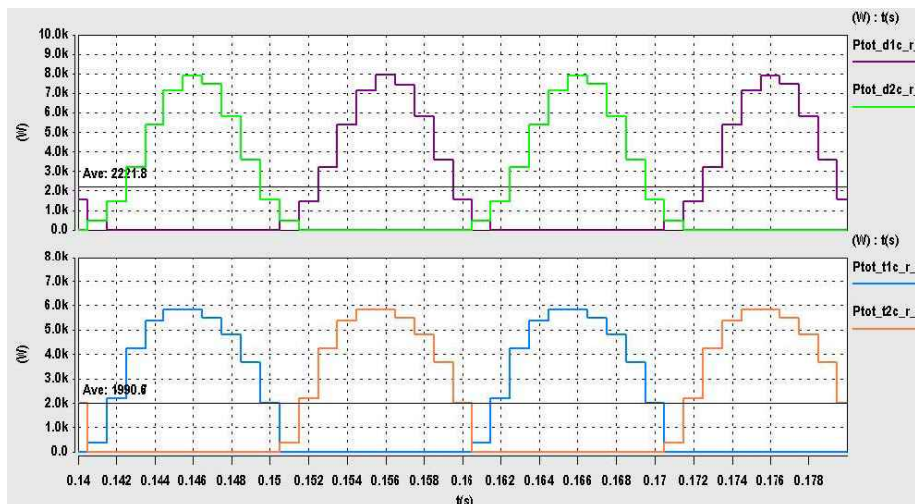


Figure 3-43.- Diodes and IGCTs power losses distribution ( $V_{DC}=1.6kV$ ,  $P_L=10MW$ )

The following figures show the evolution of the average power losses of the inverter semiconductors as a function of the inverter 50Hz RMS current, thus the output power. In all the components the power losses increase with the output power and a certain balance between the on-state losses and switching losses is obtained (slightly higher on-state losses at maximum

power). The total power losses are the same for both switching cells, with slight power losses differences between the top and bottom side semiconductors.

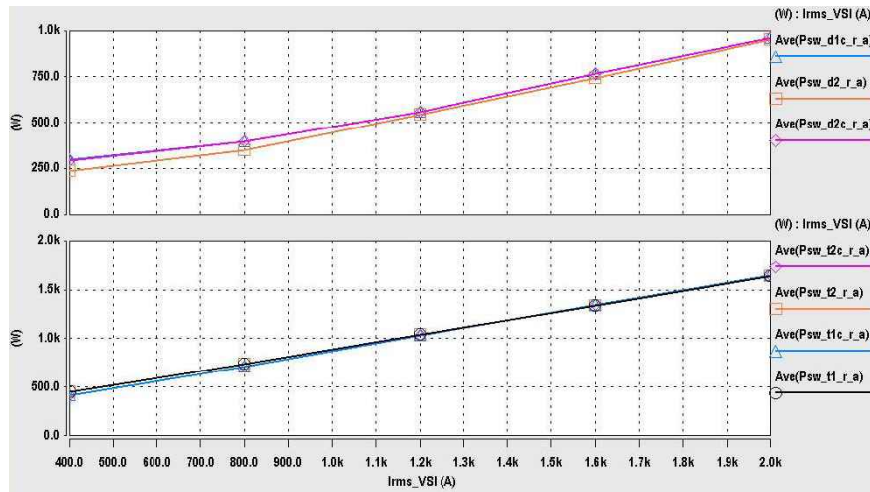


Figure 3-44.- Average switching losses distribution as a function of the inverter RMS current,  $I_{LS\ RMS}$

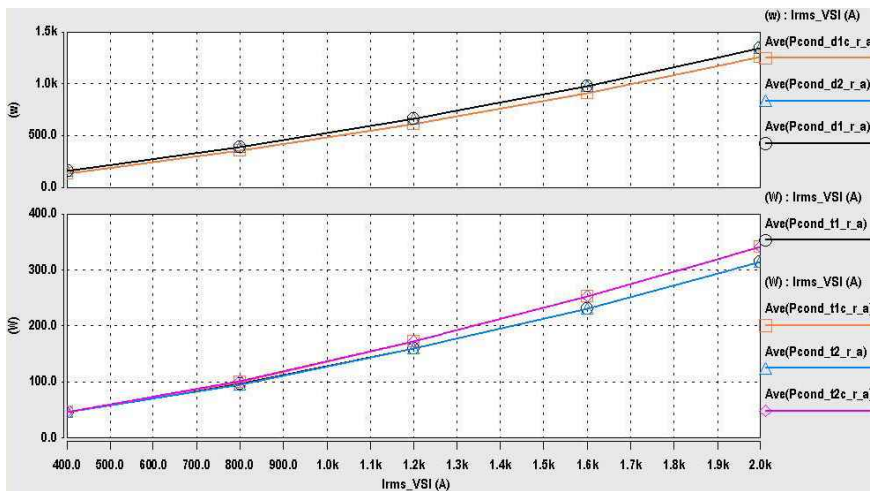


Figure 3-45.- Average on-state losses distribution as a function of the inverter RMS current,  $I_{LS\ RMS}$

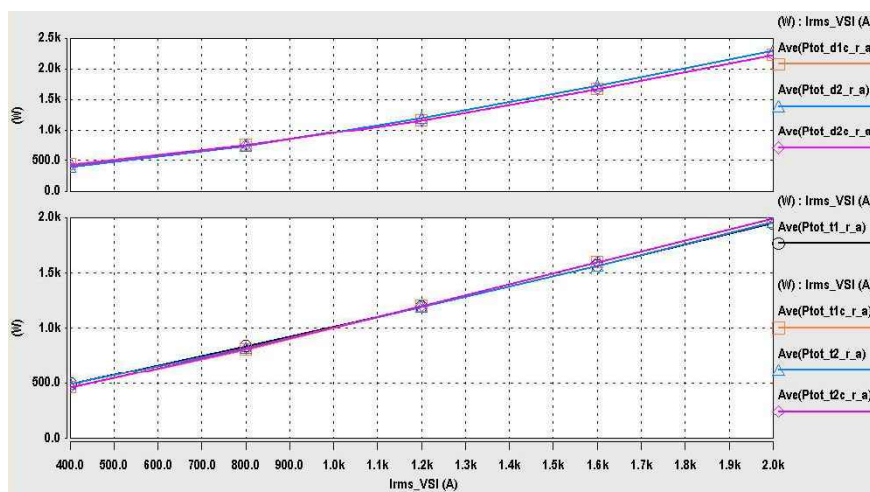


Figure 3-46.- Average total losses distribution as a function of the inverter RMS current,  $I_{LS\ RMS}$

#### 3.3.1.4.1 Active rectification solution discussion

The use of active rectifiers for a 1.5kV DC substation with maximum output power of 10MW ( $6kA_{DC}$ ) can be implemented by means of 6 single-phase 3.3kV IGCT based inverters. Such a configuration provides the dynamic characteristics required to comply with the harmonic current contents defined by the regulations, and even to answer to the sudden changes demanded by the load (the trains).

Other advantages of this structure are the properties of the converter to control the output voltage and to operate in energy devolution mode (regenerative mode). However, the most delicate issue with this solution is the behaviour of the converter when load short-circuit arises (not as uncommon on traction applications as desired). As the output of the converter behaves like a voltage source (DC link capacitor), the short-circuit current will be exclusively limited by the railway line impedance leading to huge short-circuit current that could damage firstly the DC link capacitor and then the semiconductors of the train and the substation. A possible solution to guarantee safe operation of the system is to add a two-quadrant DC/DC chopper (current reversible) at the output of the active rectifier providing two main functions, DC link voltage control and current limitation. However this additional converter will increase the complexity, cost and size of the system.

Such structure could be affordable exclusively for new installations because even if the transformer arrangement is the same as the one in the existing substations, the transformer turns ratio need to be adapted.

An alternative solution for active rectification providing output current limitation could be the use of Current Source Inverters. However, this solution requires semiconductors with reverse blocking characteristics and the ability to handle high currents and considerable switching frequencies, which nowadays are not available or have to be obtained by association of existing semiconductors (higher power losses, part count increase, etc).

#### 3.3.1.5 Harmonic currents compensation solution discussion

Several solutions applying 3.3kV IGCTs for harmonic currents compensation on SNCF 1.5kV DC substations have been analysed. Among these solutions, the use of active filters offers a flexible and relatively low effort demanding solution that can be applied either in new or in existing installations. Only the use of 24-pulse rectifiers could be a serious competitor for new installations, where cost, reliability and maintenance issues will define the adopted solution.

Regarding the active filtering solution, further investigations could be performed to find the best solution in terms of topology and semiconductors to use. Multi-cell and other multilevel solutions could provide system part count minimisation (passive components), thus lower cost, volume and heighten reliability.

### 3.3.2 Reactive Power Compensation for 25kV/50Hz Single-phase SNCF Substations

The 25kV/50Hz single-phase railway line is supplied from the electric transmission system at different voltage levels (63kV, 90kV, 200kV and 400kV). To accommodate the voltage level, the substation contains a transformer, which sometimes can be replaced by autotransformers statically adjusted to keep the voltage drop along the traction lines low. For protection and operation of the substation the installation is equipped with the adapted breakers, disconnecting switches and protective elements.

The simple configuration of the 25kV substations involves operation with relatively important voltage changes on the traction line (19kV÷27.5kV). These voltage changes are mainly related to the sudden high power changes of the load (the trains) and the high impedance of the substation transformers. To guarantee the operation of the system within its voltage limits, fixed capacitor stacks are often employed. These capacitor stacks act as power factor correctors compensating the reactive power consumption of the trains and optimising the use of the line. Nevertheless, when the line is unloaded, the voltage on the line can increase excessively. For this reason, the amount of fixed reactive power compensation on the substation is limited (6MVAR for the biggest stack).

As the power demand on the substations is increasing, mainly because of the freight traffic, the limit of using fixed capacitor stacks is being reached in some substations, and therefore penalties for reactive power consumption must be paid (especially in winter time where the railways reactive power consumption is more restricted). Moreover, future reductions on the reactive power limits that lead to penalties are expected, so the need for further reactive power compensation capabilities is required. With the use of power electronics based solutions for reactive power compensation the voltage drop in the substation transformer and along the railways line can be compensated dynamically according to the operating conditions. Consequently, the compensated reactive power can be increased, avoiding the penalties and increasing the capability of the line.

The first power electronic based solution applied on the SNCF network to increase the reactive power compensation capability was the use of the well known thyristor based Static VAR Compensator (SVC) structures [BAC-01]. This technology has been applied since decades and now high power applications are installed (more than 100MW). However, the low frequency operation of the thyristors generates low frequency harmonics that must be compensated, which implies the use of bulky filters tuned at the most relevant frequencies, Figure 3-47. Also, high levels of acoustic noise are generated, mainly on the passive components (especially on the inductor of the 3<sup>rd</sup> harmonic filter). Consequently, for substations located in urban zones such as the region of Paris where the French railways system is centralised, this solution is not convenient for size and acoustic pollution reasons.

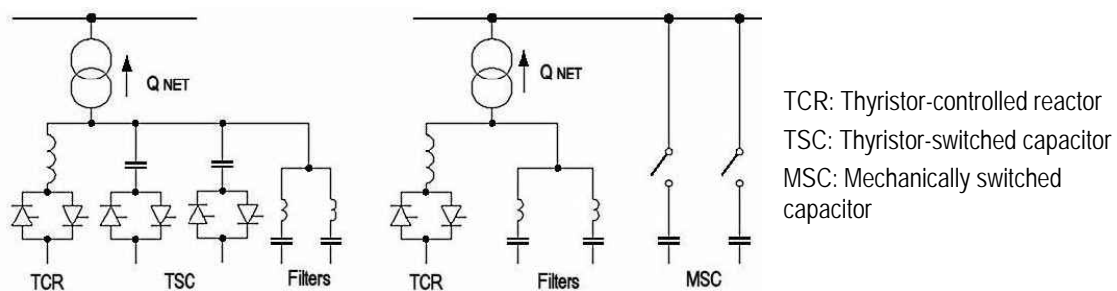


Figure 3-47.- Basic SVC structures

In addition, in the case of the railways network, the filtering of the harmonics is even more restrictive than in a classical distribution line. In fact, the lines utilised for the power transmission are also used for transmission of signalisation and communication signals, which impose extremely low harmonic limits at specific frequencies, Figure 3-48. Therefore, special attention must be paid to the harmonics generated by the entire power electronic system.

All the previous consideration leads to the use of STATCOM (Static VAR Compensator) solutions because they operate at high switching frequencies restricting the generation of low frequency harmonics and minimising the size and the acoustic noise of the reactive power compensator.

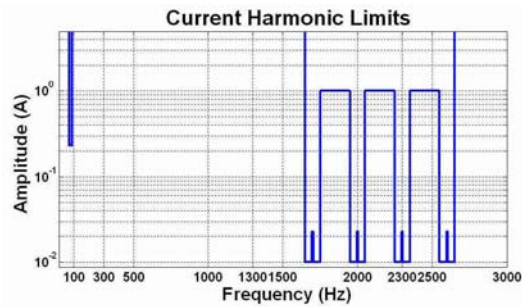


Figure 3-48.- 25kV line maximum harmonic current limits imposed by the signalisation system

In this case, the power of the basic single-phase STATCOM unit for the 25kV railways line is rated to 3MVAR, which can be combined with the existing fixed capacitor stacks to provide up to 9MVAR reactive power capability. Multiple conversion structures can be applied, however, particular solutions that inherently avoid the generation of harmonics in the railways signalisation frequency range are required. Based on the use of 3.3kV IGCTs, several solutions are analysed in the following sections, all of them applying the shunt compensation principle, Figure 3-18, and the use of a coupling transformer to adapt the 25kV voltage level to the semiconductors level.

### 3.3.2.1 Voltage source inverter based topologies

Within the voltage range of the Voltage Source Inverter  $V_{VSI}$ , the inverter current can be controlled to flow in any direction. For reactive power compensation, this means that the VSI can accommodate its output voltage to impose the network injected current  $i_{LS}$  either to compensate (capacitive) or generate (inductive) reactive power, Figure 3-49.

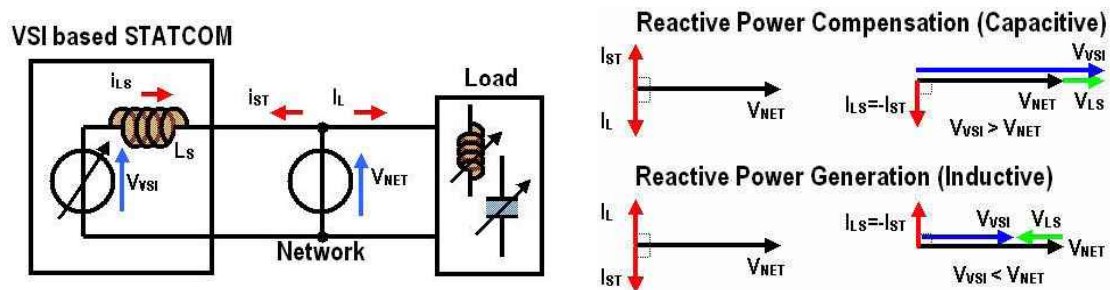


Figure 3-49.- VSI based STATCOM steady state vector diagrams (capacitive and inductive)

Regarding the VSI structure, multiple VSI topologies are now under serious consideration (2 level half and full bridge, multilevel NPC, Multi-cell, cascaded inverters, etc). For each topology, taking into consideration the ratings of the 3.3kV IGCTs (voltage and current) as well as current ripple considerations (switching frequency), the quest of the optimal component values (smoothing inductor  $L_S$ , coupling transformer ratio  $m_c$ ) for maximisation of the compensated reactive power could be found following similar procedures to those presented in section 3.3.1.4. However, the objective of the analysis here is to obtain a qualitative comparison between the most common VSI structures to determine the advantages and drawbacks of each solution for the intended application. Therefore, at first, the analysis of a single-phase full bridge 2 level and 3 level NPC and series multi-cell inverter is performed at defined 3.3kV IGCT maximum working conditions (blocking voltage 1.5kV, peak current 1.5kA and switching frequency 1kHz), and smoothing inductor value ( $L_S=500\mu\text{H}$ ). Only reactive power compensation (capacitive) is considered and obviously the coupling transformer turns ratio  $m_c$  is adapted to obtain as much reactive power compensation as possible. Under these conditions, the semiconductor power losses are

evaluated and the maximum compensated reactive power determined. Finally, the applicability of each solution on 3MVAR STATCOMs for the 25kV single-phase railways line is discussed.

For each topology, the DC link voltages are supposed to be controlled, so they are modelled as ideal voltage sources. Only a basic current loop controller (PI controller with disturbance compensation) is implemented and the current reference is ideally generated in synchronisation with the network voltage. Also, unipolar modulation for all topologies has been applied.

### 3.3.2.1.1 2-level voltage source inverter

The single-phase 2 level VSI structure and basic waveforms in STATCOM operation ( $V_{VSI}$   $90^\circ$  from the front with respect to  $I_{LS}$ ) are shown in Figure 3-50 and Figure 3-51.

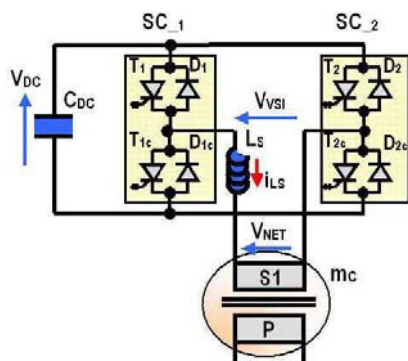


Figure 3-50.- Single-phase 2-level VSI based STATCOM

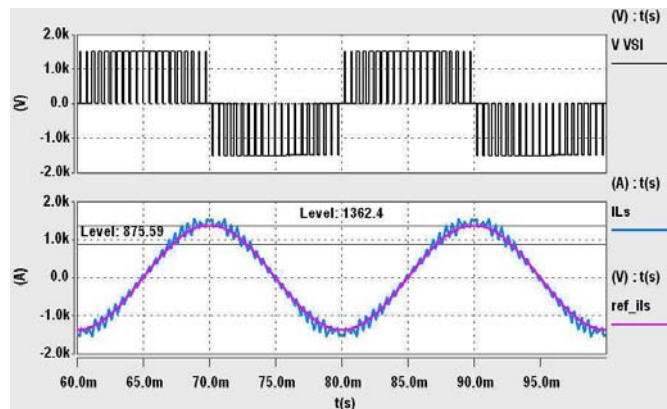


Figure 3-51.- 2-level VSI voltage and current for maximum reactive power compensation, 775kVAR

The maximum reactive power compensation for the simulated conditions defined in Table 3-8 is 775kVAR ( $V_{NET}=800V_{RMS}$ ,  $I_{LS\ 50Hz}=970A_{RMS}$ ). The inverter apparent switching frequency is twice the switching frequency ( $2 \cdot f_{SW}=2kHz$ ) due to the use of the unipolar modulation. Under these operation conditions, the maximum current ripple  $\Delta I_{LS}$  is close to 490A which represents around 18% of the peak to peak value of the  $I_{LS\ 50Hz}$  term.

Sub-system	Parameter Description	Parameter values
2 level VSI based STATCOM	Transformer turns ration ( $m_C=N_P / N_S$ )	$m_C=31.25$
	Railways line voltage (primary side) / Secondary side voltage	$U_{HV} = 25kV_{RMS} / V_{NET} = 800 V_{RMS}$
	Maximum compensation current, 50Hz	$I_{LS\ 50Hz} = 970A_{RMS}$
	Semiconductor DC blocking voltage	$V_{DC} = 1.5kV$
	Semiconductor maximum peak current	$I_{SW} \approx 1.5kA$
	Smoothing inductor	$L_S = 500\mu H$
	Switching frequency	$f_{SW} = 1kHz$
	Modulator sampling frequency	$f_{SM} = 2kHz$ (2 samples per switching period)
	Controller bandwidth	$f_{BW} = 250Hz$
	PI controller parameters	$K_P = 0.785, K_I = 1 / T_N = 206.8$

Table 3-8.- Simulation parameters for the single-phase 2-level VSI in STATCOM operation

The semiconductor power losses distribution of a switching cell of the VSI is obtained as a function of the fundamental output current ( $I_{LS\ 50\text{ Hz}}$ ) peak value. Simulation results depicted in Figure 3-52, Figure 3-53 and Figure 3-54 show equal losses distribution between the top and bottom side IGCTs and Diodes of the switching cell (slight difference at low compensation due to the effect of the ripple current) with higher losses on the IGCTs (1.1kW maximum). In this operation mode, the switching losses are dominant (more than twice the on-state losses).

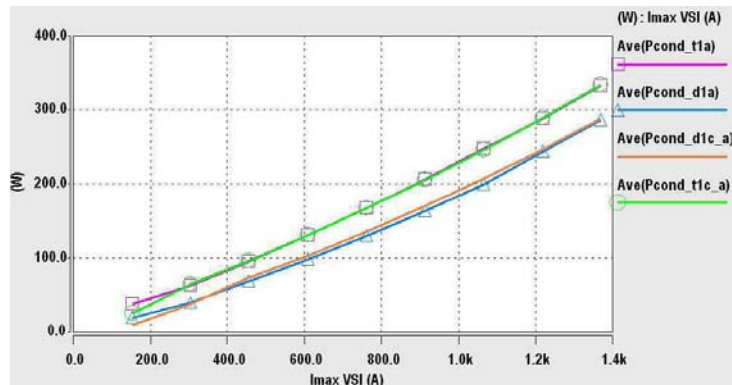


Figure 3-52.- 2-level VSI switching cell on-state losses distribution

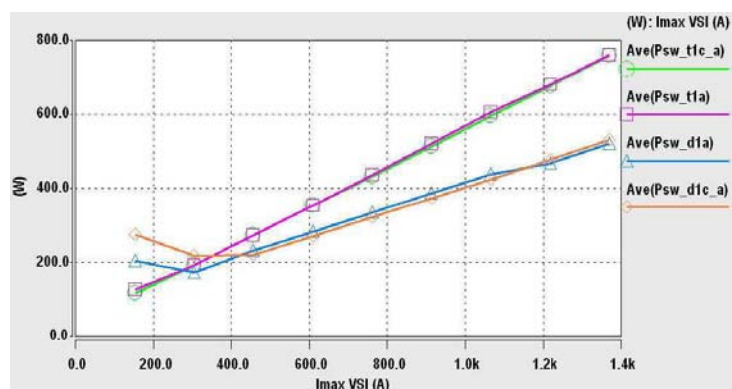


Figure 3-53.- 2-level VSI switching cell switching losses distribution

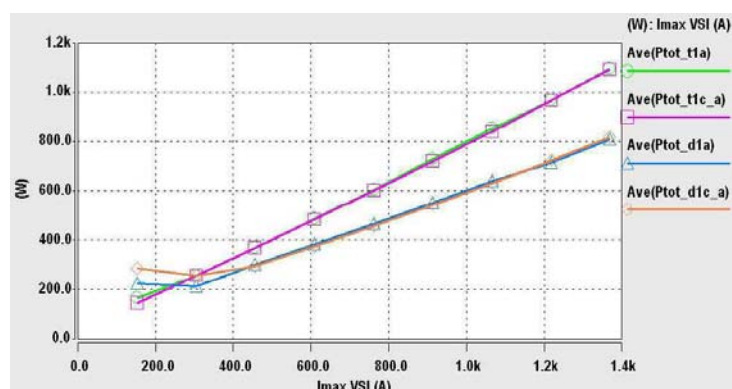


Figure 3-54.- 2-level VSI switching cell total losses distribution

### 3.3.2.1.2 3-level NPC voltage source inverter

Using a single-phase 3-level NPC VSI, Figure 3-55, the maximum reactive power compensation is increased to 1.55MVAR ( $V_{NET}=1.6kV_{RMS}$ ,  $I_{LS\ 50Hz}=970A_{RMS}$ ) thanks to a higher DC link voltage

(3kV<sub>DC</sub>). The inverter apparent switching frequency is twice the switching frequency ( $2 \cdot f_{sw} = 2\text{kHz}$ ) due to the use of the unipolar modulation, therefore the maximum current ripple  $\Delta I_{Ls}$  remains similar to the obtained with the 2-level inverter (around 475A), Figure 3-56.

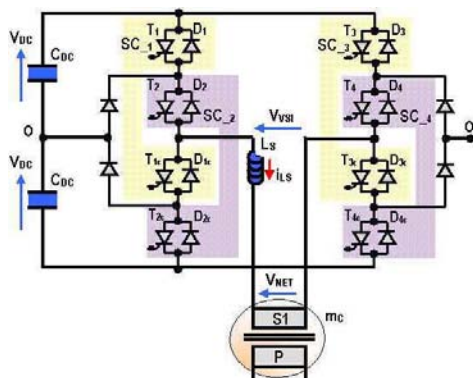


Figure 3-55.- Single-phase 3-level NPC VSI based STATCOM

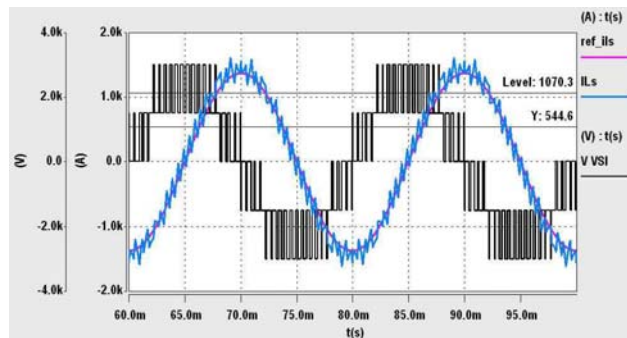


Figure 3-56.- 3-level NPC VSI voltage and current for maximum reactive power compensation, 1.55 MVAR

Compared with the 2-level inverter, the simulation parameters change only with respect to the transformer turns ratio ( $m_c = 15.625$ ) and the secondary side voltage ( $V_{NET} = 1.6\text{kV}_{RMS}$ ). Even the PI controller parameters remain the same.

Regarding the power losses distribution, there exists a relevant unbalance among the inverter leg semiconductor. The inner IGCTs ( $T_{1c}$  and  $T_2$ ) are subjected to higher on-state losses than the outer IGCTs ( $T_1$  and  $T_{2c}$ ) Figure 3-57, while the switching losses are similar for all of them (varying slightly due to the current ripple effect), Figure 3-58. In turn, for the freewheeling diodes the results show a balanced distribution on the on state losses and higher switching losses on the inner diodes ( $D_{1c}$  and  $D_2$ ).

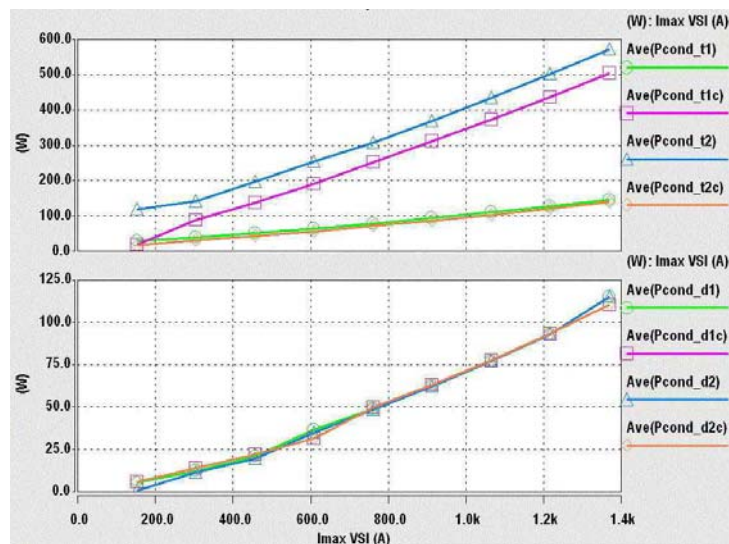


Figure 3-57.- 3-level NPC VSI switching cell on-state losses distribution

The NPC switching pattern (available semiconductor state combinations) is responsible for this unbalanced power losses distribution, ending in higher total losses for the inner semiconductor (IGCTs and Diodes). The unbalance is really noticeable for the IGCTs, with a total power losses difference around 550W between the  $T_2$  (1050W) and  $T_1$  (600W) IGCTs, Figure 3-59. The power



losses for the diodes are much lower than for the IGCTs, and the difference between diodes is also lower. The power losses on the clamp diodes are not considered.

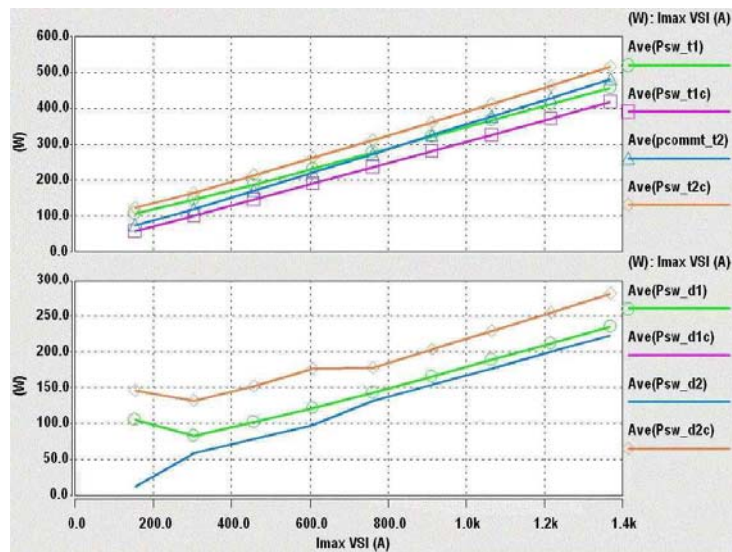


Figure 3-58.- 3-level NPC VSI switching cell switching losses distribution

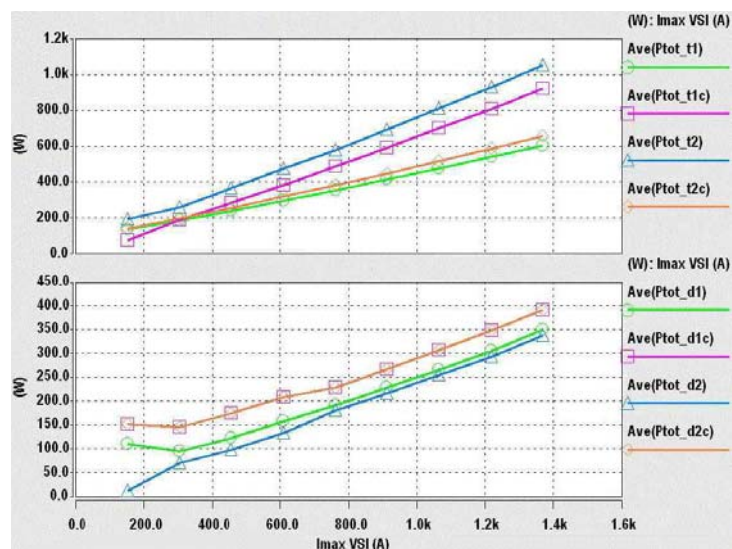


Figure 3-59.- 3-level NPC VSI switching cell total losses distribution

### 3.3.2.1.3 3-level Multi-cell voltage source inverter

The operation of the 3-level Multi-cell VSI offer a relevant reduction on the current ripple thanks to the increase of the apparent output switching frequency (four times de switching frequency instead of twice for the 2-level and 3-level NPC VSI), which can be also utilised to increase de bandwidth of the controller. This reduction (by a factor of two) is obtained thanks to the extra degrees of freedom proffered by redundant switches states available on this topology, Figure 3-60. For the single-phase 3-level Multi-cell VSI, the carriers related to each switching cell of an inverter leg are phase shifted  $180^\circ$ . The carriers for the switching cells of the adjacent leg are phase shifted  $90^\circ$  with respect to the switching cells of the other leg ( $SC_{1-SC_{3}}$ , and  $SC_{2-SC_{4}}$ ), which allows using the unipolar modulation strategy.

The single-phase 3-level Multi-cell VSI voltage and current waveforms for STATCOM operation are shown in Figure 3-61, where a maximum current ripple  $\Delta I_{LS}$  around 250A is obtained for a 50Hz current  $I_{LS\ 50Hz}=1kA_{RMS}$  and a secondary voltage  $V_{NET}=1.6kV_{RMS}$ , that is 1.6MVAR of reactive power compensation.

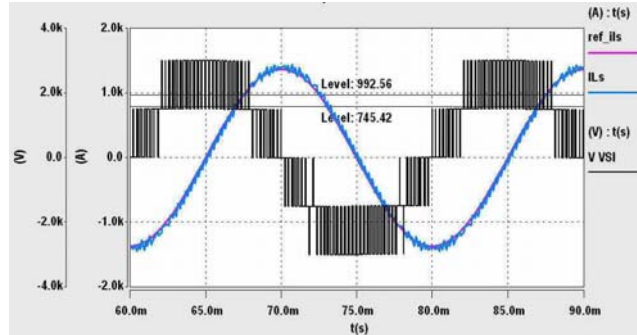
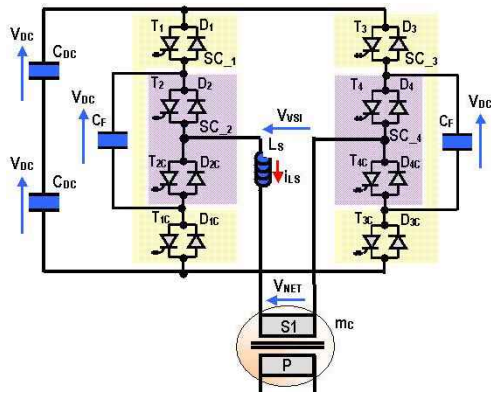


Figure 3-60.- Single-phase 3-level Multi-cell VSI based STATCOM

Figure 3-61.- 3-level Multi-cell VSI voltage and current for maximum reactive power compensation, 1.6 MVAR

The simulation parameters for the single-phase 3-level Multi-cell VSI in STATCOM operation are given in Table 3-9. The power losses evaluation on the semiconductors of an inverter leg (switching cells SC<sub>1</sub> and SC<sub>2</sub>) is obtained with these parameters as a function of the 50Hz compensation peak current.

Sub-system	Parameter Description	Parameter values
2-level VSI based STATCOM	Transformer turns ratio ( $m_C=N_P / N_S$ )	$m_C=15.625$
	Railways line voltage (primary side) / Secondary side voltage	$U_{HV} = 25kV_{RMS} / V_{NET} = 1.6kV_{RMS}$
	Maximum compensation current, 50Hz	$I_{LS\ 50Hz} = 1kA_{RMS}$
	Semiconductor DC blocking voltage	$V_{DC} = 1.5kV$
	Semiconductor maximum peak current	$I_{SW} \approx 1.5kA$
	Smoothing inductor	$L_S = 500\mu H$
	Switching frequency	$f_{SW} = 1kHz$
	Modulator sampling frequency	$f_{SM} = 2kHz$ (2 samples per switching period)
	Controller bandwidth	$f_{BW} = 250Hz$
	PI controller parameters	$K_P = 0.785, K_I = 1/ T_N = 1050$

Table 3-9.- Simulation parameters for the single-phase 3-level Multi-cell VSI in STATCOM operation

Figure 3-62 and Figure 3-63 show the IGCT and freewheeling diodes on-state and switching losses distribution. For the IGCTs as well as for the diodes, the switching losses are dominant with values twice greater than the on-state losses.

The total losses, Figure 3-64, shows a well-balanced distribution among all the IGCTs and diodes. Slight differences are noticed at low compensation values due mainly to the effect of the current ripple over the switching losses.

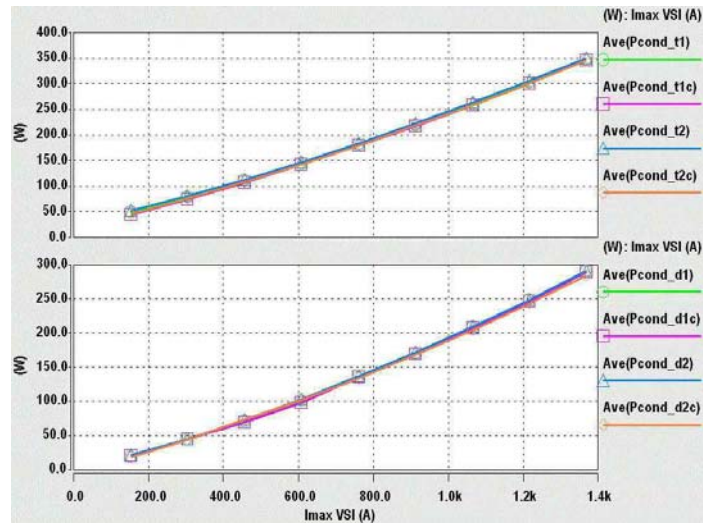


Figure 3-62.- 3-level Multi-cell VSI switching cell on-state losses distribution

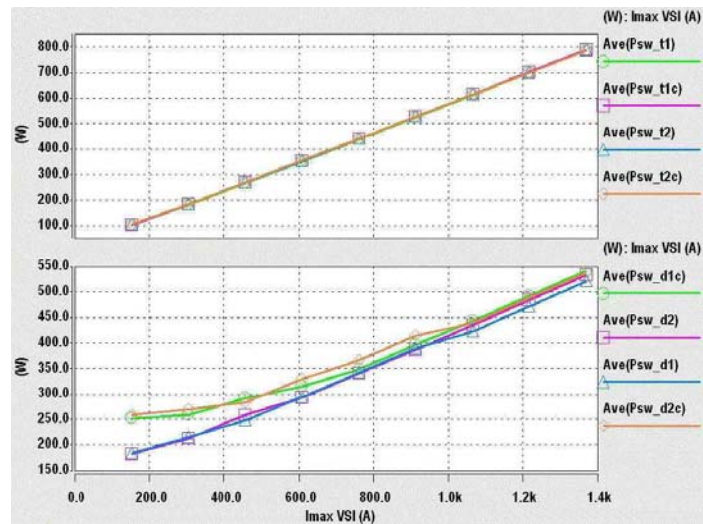


Figure 3-63.- 3-level Multi-cell VSI switching cell switching losses distribution

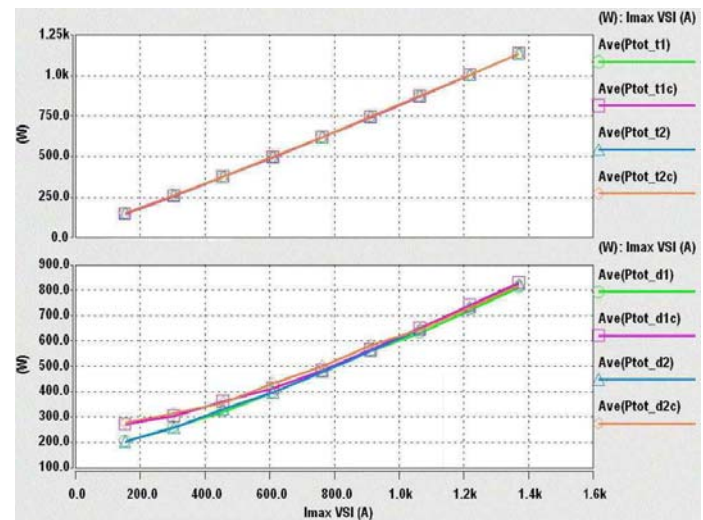


Figure 3-64.- 3-level Multi-cell VSI switching cell total losses distribution

### 3.3.2.1.4 VSI based STATCOM discussion

For the semiconductor maximum operation conditions imposed (blocking voltage 1.5kV, peak current 1.5kA and switching frequency 1kHz), no one of the single-phase VSI topologies provides the 3MVAR compensation capability, so paralleling of several VSI is required.

If the 2-level VSI solution is applied, four inverters are required to reach 3MVAR of reactive power compensation. Paralleling of the four inverters can be accomplished by using a transformer with 4 secondary windings or 4 single-phase transformers with the primary windings connected to the network. Interleaving the four modules will lead to an apparent switching frequency on the primary side of 8kHz, far enough from the forbidden current harmonics imposed by the railway line communication system (maximum 2.7kHz). Moreover, the inverter current ripple reflected to the primary side is divided by four. The required number of basic switching cells is eight.

Using the 3-level NPC VSI solution, only two inverters are required to provide 3MVAR of reactive power compensation. Two single-phase transformers or a two secondary windings transformer will be required. Interleaving both inverters will provide an apparent switching frequency on the primary side of 4kHz with a reduction of the inverter current ripple reflected to the primary side by two. Also eight switching cells are required.

In the same way, the 3-level Multi-cell VSI solution will require two inverters in parallel. Interleaving the inverters will provide an apparent switching frequency of 8kHz with a reduction of two on the inverter current reflected to the primary side. However, in this case the current ripple is half the current ripple of the 2-level and 3-level NPC current ripple. The required number of switching cells is also eight.

The previous considerations are summarised on Table 3-10 using as reference the parameters for the 2-level VSI solution (current ripple  $\Delta I_{LS}$  and transformer turns ration  $m_c$ ). From a high frequency current harmonics point of view all solutions avoid the generation of harmonics on the forbidden frequency range. The use of four single-phase 2-level inverters provides the best solution in terms of amplitude and first harmonic current frequency with the same number of switching cells. However, the number of transformers (or secondary windings), inductors, current sensors, etc. could penalise this solution. An intermediate option will be the use of the 3-level Multi-cell VSI, with 2 paralleled inverters and similar high frequency performance.

Topology	2-level	3-level NPC	3-level Multi-cell
VSI Apparent Switching frequency, $f_{sw\ vsi}$	2kHz	2kHz	4kHz
Inverter Current ripple, $\Delta I_{LS}$	$\Delta I_{LS}$	$\Delta I_{LS}$	$\Delta I_{LS} / 2$
Number of inverters in parallel, $n$	4	2	2
Number of Switching cells, $n_{sc}$	8	8	8
Primary apparent switching frequency, $f_{sw\ hv}$	8kHz	4kHz	8kHz
Transformer turns ratio	$m_c$	$m_c / 2$	$m_c / 2$
Primary side current ripple	$\Delta I_{LS} / (4 \cdot m_c)$	$\Delta I_{LS} / \cdot m_c$	$\Delta I_{LS} / (2 \cdot m_c)$
IGCT blocking Voltage, $V_{DC}=1.5kV$ IGCT peak switching current, $I_{sw}=1.5kA$	IGCT switching frequency, $f_{sw}=1kHz$ Smoothing inductor, $L_s=500\mu H$		

Table 3-10.- High frequency performance summary of different 3.3kV IGCT based VSI topologies for 3MVAR compensation (inverters paralleling).

Other important consideration that consolidates the choice of the 2-level or 3-level Multi-cell solution must be taken into account. In case of failure of one of the paralleled inverters, the system can operate without generating current harmonics in the forbidden frequency range (6kHz

for the 2-level and 4kHz for the 3-level Multi-cell). However the NPC solution will generate current harmonic exactly in the forbidden frequency range (2kHz). In this degraded operation mode, a possible solution to respect the harmonic current limits is modifying the switching frequency of the switching cell to 1.5kHz at the expense of switching losses augmentation and maybe power compensation limitation.

Regarding the power losses distribution, the NPC solution presents the best power losses budget (without counting the clamping diode losses). However, some of the semiconductors (the inner IGCTs) have similar power losses than the semiconductors of the 2-level and 3-level Multi-cell topology, which lead to similar cooling efforts in all these topologies.

In all cases, the semiconductors are not limited by their power losses or SOA limits, thus higher power compensation could be obtained increasing the inverter current and the switching frequency (decreasing the smoothing inductor value). However, practical limitations regarding the actual IGCT gate unit functionality or / and gate unit power supply could impede the operation under these conditions.

Concerning the capacitor of the DC link for all VSI topologies, its capacitance value must be high enough to keep the low frequency voltage ripple as low as possible. Neglecting the high frequency harmonics of the VSI voltage and current, Eq. 3-34 and Eq. 3-35 represent the 50Hz terms that take part on the reactive power compensation (capacitive) as depicted in the vectors diagram of Figure 3-49. Considering that no power is lost or stored on the converter, the converter instantaneous input power is equal to the instantaneous output power, Eq. 3-36. From this hypothesis, the low frequency capacitor current and voltage can be easily derived Eq. 3-37, Eq. 3-38, and finally the peak to peak value of the capacitor voltage ripple can be obtained, Eq. 3-39. The  $C_{DC}$  value must be selected to fix a maximum permissible voltage ripple (for example  $\Delta V_{CDC}=5\%$  of the DC link voltage, Eq. 3-40) to avoid the perturbation of the inverter current control and to minimise the capacitor power losses. In the 2-level case, the required DC link capacitor value is  $C_{DC}=22\text{mF}$  ( $\Delta V_{CDC}=5\%$ ,  $V_{DC0}=1.5\text{kV}$ ,  $Q_{VSI}=775\text{kVAR}$ )

$$v_{VSI} = V_{VSI} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \quad \text{Eq. 3-34}$$

$$i_{LS} = I_{LS} \cdot \sqrt{2} \cdot \sin(\omega \cdot t - \frac{\pi}{2}) \quad \text{Eq. 3-35}$$

$$V_{DC} \cdot i_{CDC} = (V_{DC0} + \Delta V_{CDC}) \cdot i_{CDC} = v_{VSI} \cdot i_{LS} \quad \text{Eq. 3-36}$$

$$i_{CDC} \approx \frac{v_{VSI} \cdot i_{LS}}{V_{DC0}} = \frac{V_{VSI} \cdot I_{LS} \cdot \sin(2 \cdot \omega \cdot t)}{V_{DC0}} \quad \text{Eq. 3-37}$$

$$\Delta V_{CDC} = \frac{1}{C_{DC}} \int i_{CDC} \cdot dt = \frac{-V_{VSI} \cdot I_{LS}}{V_{DC0} \cdot 2 \cdot \omega \cdot C_{DC}} \cdot \cos(2 \cdot \omega \cdot t) \quad \text{Eq. 3-38}$$

$$Q_{VSI} = V_{VSI} \cdot I_{LS} \quad \text{Eq. 3-39}$$

$$\Delta V_{CDC} = \frac{Q_{VSI}}{V_{DC0} \cdot \omega \cdot C_{DC}}$$

$$C_{DC} = \frac{Q_{VSI}}{0.05 \cdot V_{DC0}^2 \cdot \omega} \quad \text{Eq. 3-40}$$

For the 3-level VSI solutions, the DC link voltage is the double of the 2 level VSI, therefore, if the same relative voltage ripple (%) is considered half the capacitance value is required for double the VSI reactive power,  $Q_{VSI}$ . However, the energy stored on the capacitor for 3-level VSI is twice the energy of the 2-level VSI capacitor (half the capacitance and double the voltage), which could

lead to higher size and cost of the capacitor. Also, in 3-level VSI special capacitor arrangements (middle point) or even additional capacitors (floating capacitors) are required.

### 3.3.2.2 PWM AC chopper

The operation of AC Choppers provides a variable AC voltage from a constant AC voltage source, maintaining the output frequency constant equal to the input frequency. The classical AC choppers are based on phase-controlled thyristors but they generate high power factor fluctuation and harmonic currents. The use of PWM AC Choppers can overcome these problems thanks to their operation at high switching frequency.

At the beginning, classical PWM DC chopper topologies were directly transformed into PWM AC Choppers topologies using association of high frequency three-segment semiconductors to obtain a high frequency current and voltage reversible semiconductor (four segments semiconductors are required to interconnect the AC source and load) [CHO-89]. These converters offer some interesting advantages compared to the classical thyristor based phase-controlled solutions (mainly regarding power factor and harmonics), however other important technical drawbacks must be solved (safe switching of the reversible semiconductors, high conduction losses, etc). Then, PWM AC Choppers topologies using three segment classical semiconductors (current reversible, voltage unidirectional) are introduced. These topologies cover step up, down and up-down voltage transfer ratios (boost, buck and buck-boost type) not only for single-phase systems but also for three-phase systems [KWO-96], [SRI-95].

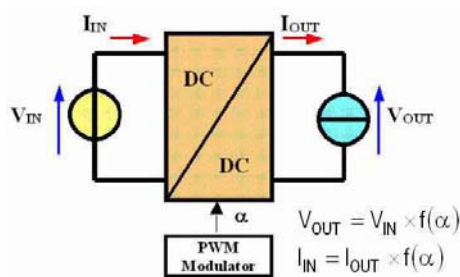


Figure 3-65.- PWM DC / DC Chopper operation principle

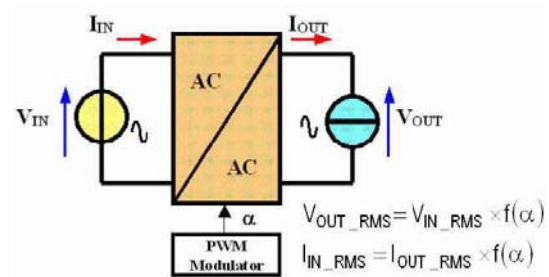


Figure 3-66.- PWM AC / AC Chopper operating principle

The AC Choppers operation principle is derived from the well-known operation of PWM DC choppers for DC/DC conversion, where the DC output voltage depends on the DC input voltage value and can be adjusted acting over the semiconductors duty cycle ( $\alpha$ ), Figure 3-65. For the AC Choppers, as the input voltage is changing in value and sign over the time, this conversion relation is true not for the DC value but for the RMS value provided that the switching frequency is high enough compared with the AC input frequency, Figure 3-66. The PWM AC Chopper conversion function in steady state, fundamental terms and ideal operation can be compared to a transformer where the transformer ratio is changed by action over the duty cycle.

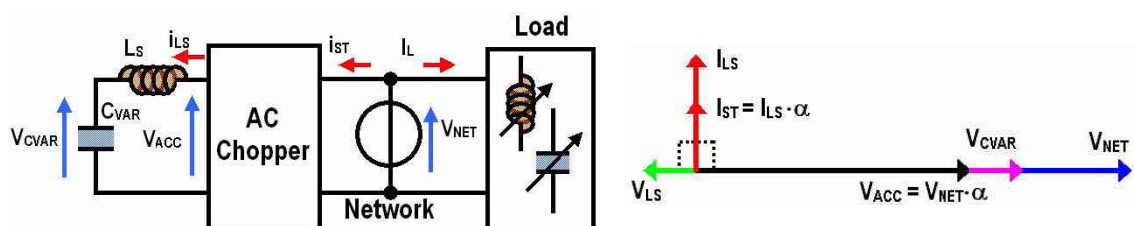


Figure 3-67.- AC Chopper based STATCOM steady state vector diagrams (capacitive compensation)

For reactive power compensation (capacitive) the AC chopper can be used to adapt the applied voltage over a fixed capacitor  $C_{VAR}$  obtaining the required variable capacitor function. Figure 3-67 shows the steady state vector diagram for a step-down (BUCK) AC Chopper operating as reactive power compensator. The smoothing inductor  $L_S$  is required to guarantee the current source behaviour of the load, however, at the line network frequency the load is capacitive.

Figure 3-68 shows the semiconductor arrangement of the single-phase step-down AC Chopper. The conversion structure is composed of 2 current reversible and voltage unidirectional switching cells, which are controlled according to the sign of the input voltage  $V_{NET}$ , (one switching cell is short-circuited alternatively on each input voltage semi-period while the other is PWM controlled). Also, an input capacitive filter  $C_F$  is added to filter the high frequency current generated by the switching operation of the AC Chopper.

The reactive power compensation characteristic of the step-down AC Chopper based STATCOM is duty cycle  $\alpha$  dependent as defined by Eq. 3-41 and shown in Figure 3-69. Detailed explanations about the operation and control of the converter are given in Chapter 4.

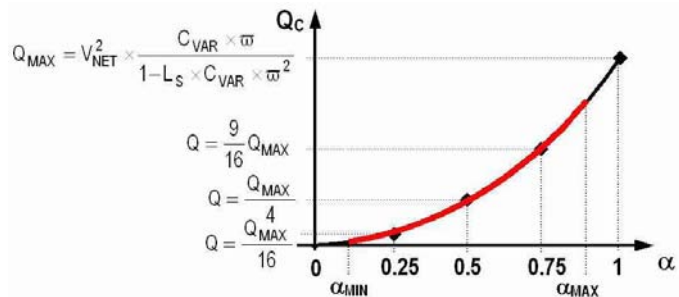
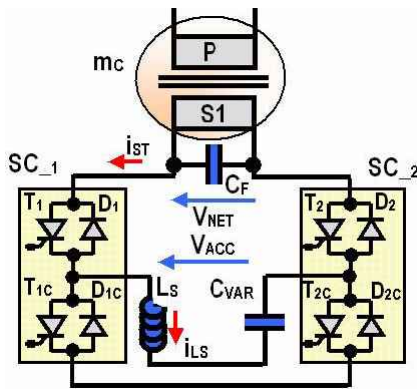


Figure 3-68.- Single-phase AC Chopper based STATCOM

Figure 3-69.- Reactive power compensation characteristic for a Buck AC Chopper.

$$\vec{V}_{ACC} = \vec{V}_{NET} \cdot \alpha = \vec{V}_{C_{VAR}} + \vec{V}_{L_S} = \frac{I_{L_S}}{C_{VAR} \cdot \omega} - L_S \cdot \omega \cdot I_{L_S};$$

$$Q = V_{ACC} \cdot I_{L_S} = V_{NET} \cdot \alpha \cdot \frac{V_{NET} \cdot \alpha}{\left(\frac{1 - L_S \cdot C_{VAR} \cdot \omega^2}{C_{VAR} \cdot \omega}\right)} = V_{NET}^2 \cdot \frac{C_{VAR} \cdot \omega}{(1 - L_S \cdot C_{VAR} \cdot \omega^2)} \cdot \alpha^2 \quad \text{Eq. 3-41}$$

$\alpha$  = duty cycle

$\omega$  = network pulsation (rad/s)

$V_{NET}$  = Input filter voltage

For an 3.3kV IGCT based AC Chopper for STATCOM operation, the same maximum voltage, current and switching frequency values as for the VSI solution are fixed (blocking voltage 1.5kV, switching current 1.5kA, switching frequency 1kHz). The maximum blocking voltage of the IGCTs imposes the transformer turn ratio ( $m_C=23.5$ ,  $V_{NET}=1.06kV_{RMS}$ ). Then, the load components ( $L_S=1mH$  and  $C_{VAR}=2.45mF$ ) are selected to obtain the maximum reactive power compensation without exceeding the maximum switching current for a maximum duty cycle  $\alpha_{MAX} = 0.95$ . Under these operating conditions, the maximum reactive power compensation reaches 1MVAR.

The AC Chopper output voltage  $V_{ACC}$  and current  $I_{L_S}$  waveforms operating at 1MVAR of reactive power compensation are shown in Figure 3-70. It can be seen how the sinusoidal input voltage is switched at 1kHz generating a current with a leading phase shift of  $90^\circ$  with respect to de voltage. Also the high frequency current ripple generated by the switching mode operation can be noticed.

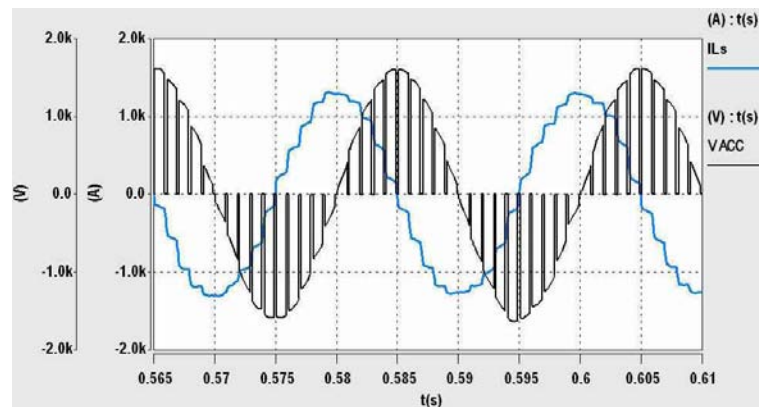


Figure 3-70.- AC Chopper voltage and current for maximum reactive power compensation, 1 MVAR

The use of the universal power losses estimator is applied to obtain the power losses distribution of the semiconductors on one switching cell of the AC Chopper. Obviously, the input voltage change, the short circuit operation of the switching cells according to the input voltage sign, the current ripple and the closed loop operation are taken into account. Simulation results for the on-state, switching and total power losses are depicted as a function of the maximum 50Hz component on the smoothing inductor  $L_s$  current in Figure 3-71, Figure 3-72 and Figure 3-73 respectively.

The most interesting property of the AC Chopper solution is that the on-state losses are dominant, which is well adapted for the use of IGCTs. The switching losses are low because the switching voltage and current change continuously and the maximum current /voltage is switched when the voltage/current is minimal.

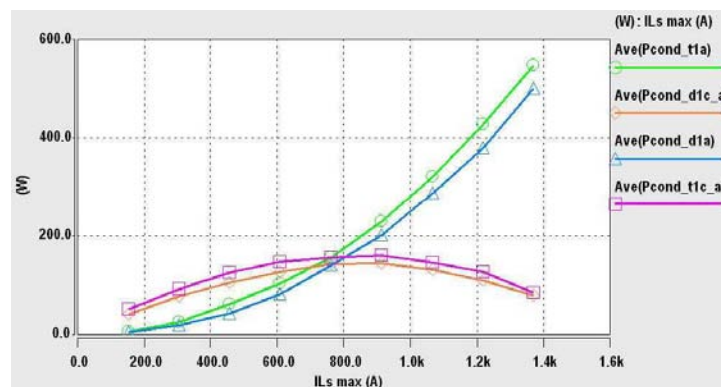


Figure 3-71.- AC Chopper switching cell on-state losses distribution

The total losses on the switching cell are not balanced, and the topside IGCTs and diodes ( $T_1$  and  $D_1$ ) are much more loaded than the bottom side semiconductors ( $T_{1c}$  and  $D_{1c}$ ). The power losses difference ratio between IGCTs and diodes of the same switching cell is greater than two. The power losses are balanced on an intermediate power compensation point. This point coincides with the operation at duty cycle  $\alpha=0.5$  where the top and bottom semiconductors are loaded equally.

In general, in this topology the total power losses are lower (lower than 800W in the worst case) and higher reactive power compensation (1MVAR) is obtained compared with the VSI solutions for the same semiconductor working conditions.



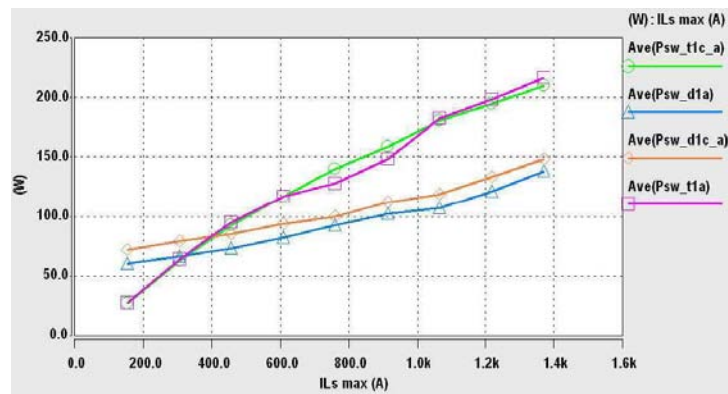


Figure 3-72.- AC Chopper switching cell switching losses distribution

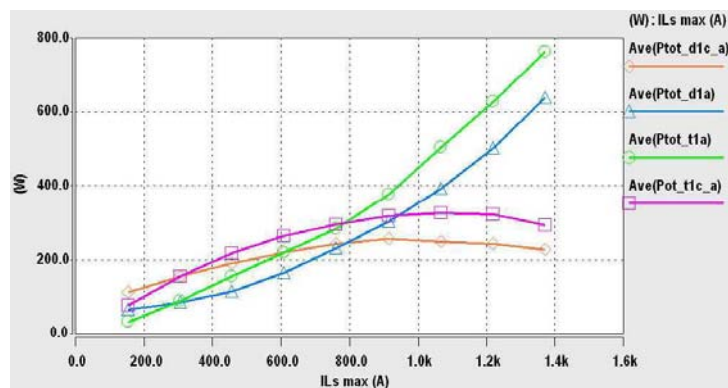


Figure 3-73.- AC Chopper switching cell total losses distribution

To obtain 3 MVAR of total reactive power compensation three single-phase AC Choppers operating in parallel by means of a single-phase transformer is required. Interleaving the three modules will generate on the low and high voltage side an apparent switching frequency of 3kHz, therefore the high frequency current harmonics will be out of the forbidden frequency range imposed by the SNCF communication system. Obviously, if one of the AC Choppers fails, current harmonics on the forbidden range will be generated. To avoid this operation in degraded mode, the AC Choppers can change to operation at 1.5kHz without very much compensation capability reduction because only the switching losses will be increased and they are not dominant in this case.

### 3.3.2.3 Reactive power compensation solution discussion

Several STATCOM solutions based on 3.3kV IGCTs for reactive power compensation of the single-phase 25kV/50Hz SNCF network have been analysed.

Among the classical Voltage Source Inverter solutions the use of single-phase 2-level or 3-level Multi-cell inverters are the best choice from a high frequency current pollution point of view. Both solutions have very similar power losses, in both cases much higher than the losses of the 3-level NPC solution. For the required compensation, relatively high DC link capacitance values are required.

Regarding the use of AC Choppers, the power losses results summarised on Table 3-11 show a relevant improvement compared to the VSI solution in terms of semiconductor use (lower number of switching cells to obtain 3MVAR) and power losses per module to be paralleled. However, from

a high frequency current harmonic generation point of view the VSI solutions offer better performance.

Topology	2-level VSI	3-level NPC VSI	3-level Multi-cell VSI	AC Chopper
Number of modules in parallel, n	4	2	2	3
Number of Switching cells, $n_{sc}$	8	8	8	6
Primary apparent switching frequency, $f_{sw\ HV}$	8kHz	4kHz	8kHz	3kHz
Maximum IGCT power losses	1.1kW	1.05kW	1.125kW	770W
Maximum Diode power losses	800W	380W	825kW	640
Maximum switching cell power losses	3.8kW	2.4kW	3.9kW	1.95kW
		2.3kW	3.9kW	
Maximum leg power losses	3.8kW	4.7kW	7.8kW	1.95kW
Maximum module power losses	7.6kW	9.4kW	15.6kW	3.9kW
Maximum total power losses	30.4kW	18.8kW	31.2kW	11.7kW
Maximum reactive power	3.1MVAR	3.1MVAR	3.2MVAR	3MVAR

Table 3-11.- Results summary for 3MVAR STATCOM topologies based on 3.3kV IGCT

In all cases, the SOA and thermal limits of the semiconductors are not attained. However, the gate unit and its power supply consumption at higher current and switching frequencies could limit the practical operation of the semiconductors under these conditions.

## 3.4 Conclusions

The universal power losses estimator developed for 3.3kV IGCT switching cells has demonstrated its flexibility to be used in different topologies for different applications under very different working conditions. Two main applications have been studied, the harmonic current compensation for SNCF 1.5kV DC substations and the reactive power compensation for SNCF 25kV/50Hz substations. For both applications their specific particularities have been introduced and several possible solutions have been proposed and analysed.

In the case of the 1.5kV DC substations, active filters based on single-phase inverters offer an effective solution that can be applied either in existing or in new installations with a relatively low power equipment (around 1MVAR) for load power levels reaching 10MW. Under these conditions, the 3.3kV IGCT can be considered to be underused and lower current rated semiconductors could be applied. Lower current 3.3kV IGCTs (if developed) or existing 3.3kV could be best suited for this application.

Regarding the single-phase 25kV substations, VSIs and AC Choppers have been analysed. If only reactive power compensation (capacitive) is required, the AC Chopper shows better performances in terms of power losses and utilisation of the semiconductors. However, concerning high frequency current harmonics generation, the VSI solutions offer better characteristics. Anyway, the AC chopper solution can fulfil the harmonic current requirements and must be considered as a serious candidate for this application using 3.3kV IGCTs. In contrast to the well know VSI, further research efforts on the AC Chopper must be carried out regarding the dimensioning of the components, IGCTs clamp circuits effect, control, modulation and operating modes of the topology, etc.

# Chapter 4

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## Single-phase STATCOM with 3.3kV IGCT based Step-Down PWM AC Choppers

### 4.1 Introduction

The use of direct AC/AC conversion PWM AC Choppers for single-phase reactive power compensation (capacitive operation) can provide an interesting alternative to the classical STATCOM solutions based on Voltage Source Inverters. Higher reactive power compensation capabilities at given semiconductor ratings, lower semiconductor power losses and smaller compensation capacitor are the main arguments offered by the PWM AC Choppers. However, the AC Choppers' control and switching pattern generation (PWM) is directly related to the AC input signal, which requires specific solutions dealing with the non-linear behaviour of these topologies.

This chapter is arranged as follows. First, the PWM AC Chopper topologies are briefly introduced to show their general characteristics. Then, the conversion structure for a 3MVAR single-phase STATCOM for the 25kV/50Hz SNCF substations based on step-down PWM AC Choppers equipped with 3.3kV IGCTs is proposed. The operation and design of a basic 1MVAR STATCOM module based on 3.3kV IGCTs and PWM AC Choppers is detailed in terms of components dimensioning, control strategy, etc.

### 4.2 Direct AC/AC Conversion with PWM AC Choppers

Multiple converter topologies can be applied to provide AC/AC conversion. Considering the number of conversion stages, they can be classified as either Direct or Indirect AC/AC converters, [BHO-93]. Indirect converters use intermediate links (DC or AC) using at least two different conversion stages, which generally require the use of storage elements. Direct converters provide a direct link between the source and the load without additional storage elements. Nevertheless, passive filters are always required to filter out the high frequency harmonics introduced at the input and output sides through the converter switching operation.

Among the AC/AC direct converters, the Cycloconverters and Matrix converters are distinguished by their ability to adjust the output frequency and voltage from a specific AC input voltage source. They also provide bi-directional power transfer capabilities, allowing the use of active loads (e.g. motors in regeneration mode).

On the other hand, the AC Chopper topologies, analogously to the well known DC choppers, provide direct AC/AC conversion only between two AC sources characterised by the same fundamental frequency, Figure 4-1. They can be treated as equivalent transformers where the

turns ratio can be electronically modified. Nevertheless, although they can provide instantaneously bi-directional power transfer, they allow the power transfer flow in one direction only according to the load's nature. The AC Choppers are normally designed to guarantee the power transfer between a fixed AC voltage source (e.g. the utility grid) and a passive AC load. The load voltage (i.e. its RMS value) can be adjusted to control the power demand, but the power exchange (either active or reactive) is only defined by the nature of the passive load (resistive, capacitive or inductive). For example, with an AC Chopper, an inductive load will never be able to operate as a capacitive load from the input side point of view. This is due to the fact that the phase of the AC voltage applied to the load cannot be modified. It is only defined by the input voltage and the transfer ratio of the AC Chopper.

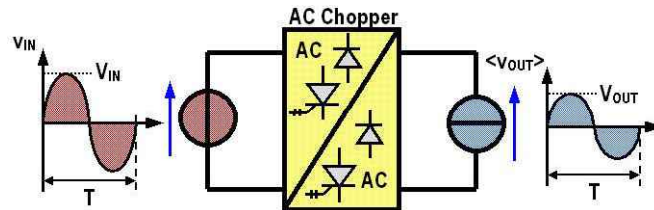


Figure 4-1.- Principle of AC Chopper direct AC/AC conversion

### 4.2.1 Overview of PWM AC Choppers Topologies

The concept of the AC Chopper is not new. Line frequency thyristor based direct AC/AC converters are widely used in AC power control applications such as industrial heating, lighting control, soft starting and speed controllers for induction motors, power conditioning, etc. In these applications, the load voltage is controlled by retardation of the thyristors' firing angle, which generates lagging power factor and significant current harmonics at the supply side, as well as relevant current and voltage harmonics at the output side.

The use of the PWM pattern generation was considered as a solution to improve the input power factor and to eliminate specific current harmonics of thyristor based direct AC/AC Converters, which led to the introduction of step-down PWM AC Choppers, [CHO-89], [CHO-95]. This topology is derived from the classical step-down PWM DC chopper, where the two segment semiconductors (unidirectional voltage and current) have been replaced by four segment turn-off semiconductors (voltage and current reversible), Figure 4-2.

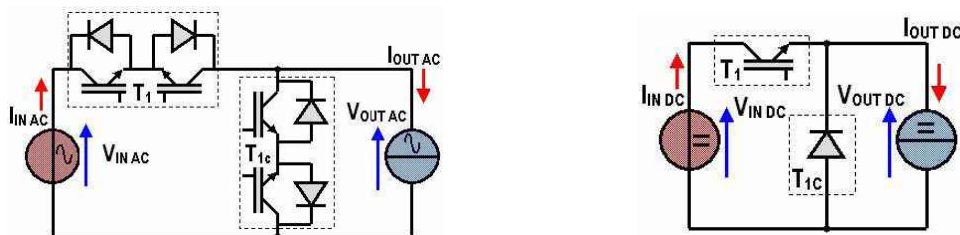


Figure 4-2.- Single-phase step-down PWM AC-chopper derived from the step-down DC-chopper

The output voltage is simply adjusted by alternating the two available semiconductors states inherent to this topology. During the active phase, the input voltage is applied to the load, and during the freewheeling phase a short-circuit path is provided to the load current, Figure 4-3. However, the practical application of this solution is limited by relevant technical drawbacks. Most significant problems are due to the need of bulky snubber circuits to provide safe switching conditions to the reversible semiconductors.

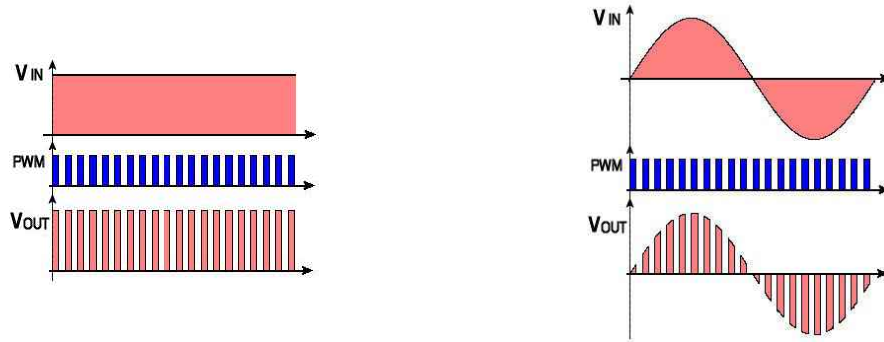


Figure 4-3.- Single-phase PWM DC and AC Chopper output voltage waveforms at constant duty cycle

Then, novel PWM AC Choppers topologies using three segment classical semiconductors (current reversible, voltage unidirectional) were introduced, [SRI-95]. These topologies use also the PWM DC Choppers as reference to derive PWM AC Choppers with step-up, down and up-down voltage transfer ratios (boost, buck and buck-boost type) for both single-phase and also for three-phase systems, (see Figure 4-4 and Figure 4-5 respectively).

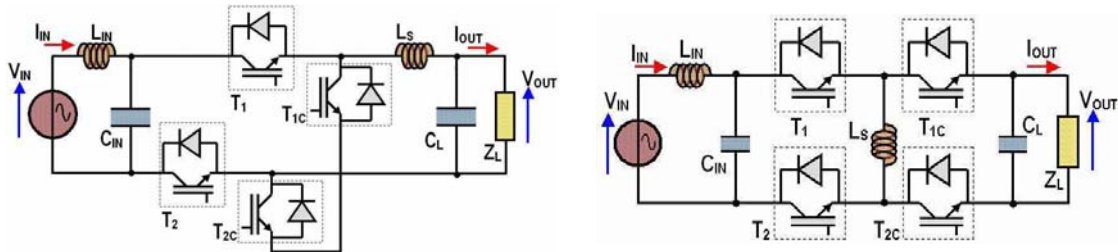


Figure 4-4.- Single-phase Buck and Buck-Boost PWM AC Choppers using 3 segment semiconductors

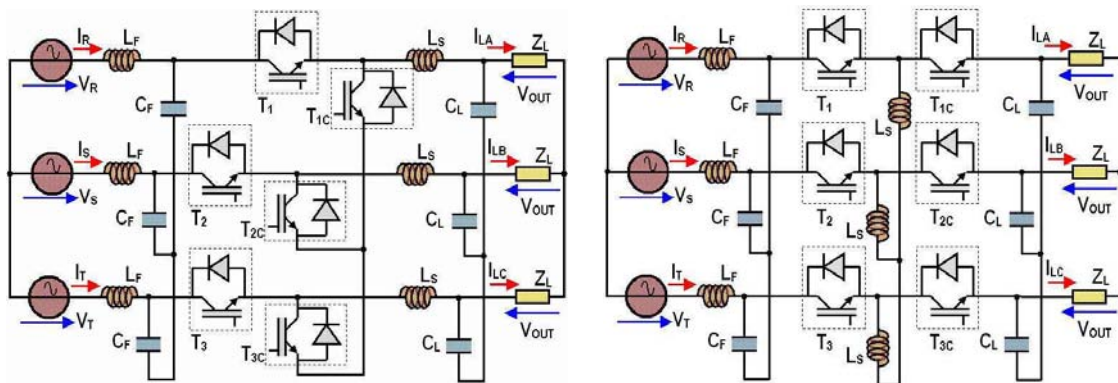


Figure 4-5.- Three-phase Buck and Buck-Boost PWM AC Choppers using 3 segment semiconductors

The use of classical three segment semiconductors arranged in switching cells ( $T_x$ - $T_{xc}$  complementarily controlled when operated in PWM) with decoupling capacitors and adapted PWM patterns allow the safe operation of the semiconductors, [KWO-96], [LEF-01]. In these conversion structures, the input and output voltage are connected differentially between two switching cells, which implies that, depending on the switching sequence, the load can be completely disconnected from the input (freewheeling phase). In some applications, for safety reasons, the neutral point of the load must be permanently connected to the input neutral point. In such cases, the so-called Non-Differential PWM AC Chopper structures can be applied for both single and poly-phase systems, [MEY-02], offering the same general behaviour as the differential structures. Figure 4-6 shows the basic structure of the single-phase step-down non-differential

AC Chopper. Characteristic for this structure is that the switching cell connected to the input is "broken" by the input voltage filter  $C_{IN}$ , which also acts as decoupling capacitor. The decoupling capacitor for the second switching cell is represented by  $C_D$ .

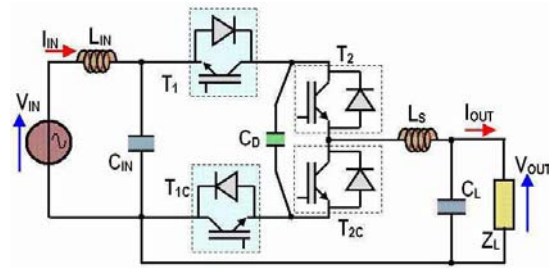


Figure 4-6.- Non differential step-down PWM AC Chopper

Finally, the PWM AC Chopper topology family is completed by the multi-cell PWM AC Chopper structures, [LEF-01]. Basically, since the PWM AC Chopper is made up of switching cells, extension of the multi-cell technique allows considering the multi-cell differential and non differential PWM AC Chopper structures. Nevertheless, in these structures the balancing problem of the floating capacitor  $C_{FL}$  is more complicated than in the VSI because the voltage has to change dynamically according to the input voltage waveform. Figure 4-7 and Figure 4-8 show the 3-level multi-cell structure of differential and non-differential step-down PWM AC Choppers respectively.

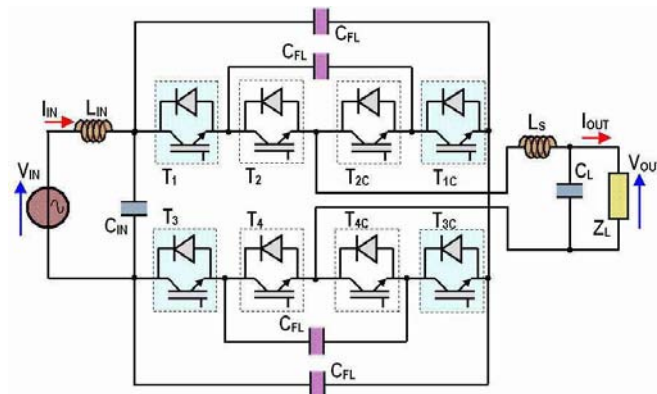


Figure 4-7.- 3-level multi-cell differential PWM AC Chopper (step-down)

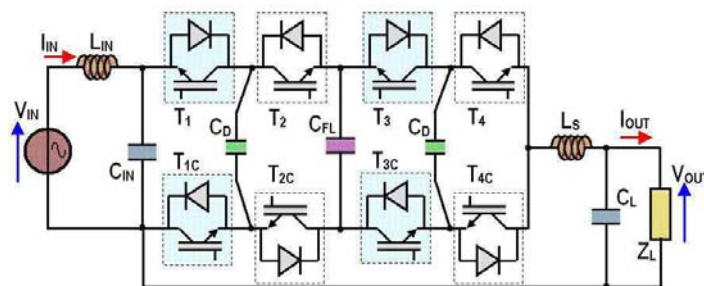


Figure 4-8.- 3-level multi-cell non-differential PWM AC Chopper (step-down)

Classical applications of PWM AC Choppers have been lighting control, soft starters for induction motors, industrial heating, etc. During the past few years, new applications considering PWM AC Choppers in the field of power conditioning such as power line conditioners, phase shift control in transmission lines, power electronic transformers, harmonic filters, series compensators, Flicker

controllers, etc, have been mentioned in the literature [VEN-97a], [LEF-01], [FED-02], [AEL-03]. Although these applications aim to be operated at medium and high power levels, most of the experimental set-ups have been demonstrated for low power only at high switching frequencies. Real application at medium and high power levels has not been reported yet.

## 4.2.2 Modulation of PWM AC Choppers

The PWM for AC Choppers with three segment semiconductors must be provided by a suitable switching pattern to obtain the desired voltage transfer ratio and also the safe switching operation of the semiconductors. Therefore, the PWM pattern must be adapted to the related AC chopper topology (single-phase, three-phase, etc.) and must take into account technical aspects that could lead to unsafe commutation of the semiconductors (switching times, operation sequences, measurement accuracy, etc.). The differential step-down PWM AC Chopper, Figure 4-9, is used to illustrate the key issues related to the modulation of the PWM AC Choppers.

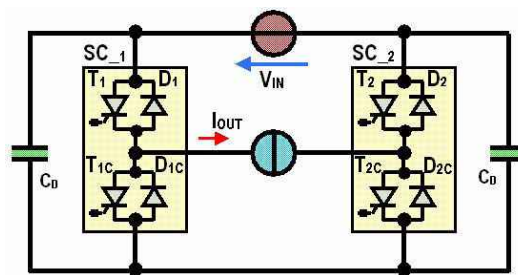


Figure 4-9.- Basic structure of the single-phase step-down PWM AC Chopper

Considering the influence of the switching cell decoupling capacitors  $C_D$  is essential for the definition of the converter operation sequences. Depending on the semiconductor gating signals and the polarity of the output current, the following three energy transfer phases can be distinguished:

- Active phase: The switching cell upper semiconductors connect directly the input voltage source  $V_{IN}$  to the output current source  $I_{OUT}$ , allowing the energy transfer between them, ( $T_1$ - $D_2$  for  $I_{OUT}>0$  and  $T_2$ - $D_1$  for  $I_{OUT}<0$ ), Figure 4-10.
- Freewheeling phase: The switching cell lower semiconductors provide a freewheeling path for the output current source  $I_{OUT}$ , ( $T_{1c}$ - $D_{2c}$  for  $I_{OUT}<0$  and  $T_{2c}$ - $D_{1c}$  for  $I_{OUT}>0$ ), Figure 4-11.
- Indirect exchange phase: When the switches of the converter form a diagonal between the two switching cells ( $T_1$ - $T_{2c}$  for  $I_{OUT}>0$  and  $T_2$ - $T_{1c}$  for  $I_{OUT}<0$ , or  $D_1$ - $D_{2c}$  for  $I_{OUT}>0$  and  $D_2$ - $D_{1c}$  for  $I_{OUT}<0$  when the controlled semiconductors are switched off), the decoupling capacitors participate in the energy transfer between the input voltage source and the output current source, Figure 4-12.

Although the indirect exchange phase could provide an additional degree of freedom to control the output voltage, there are no redundant switching states that allow to control at the same time the output voltage and the voltage of the decoupling capacitors as opposed to in multi-cell converters. As a consequence, only the active and freewheeling phases are useful. Note that attention has to be paid to the undesired application of the indirect phase during the dead time  $T_D$  imposed on the switching cells in order to avoid the input voltage source from being short-circuited.

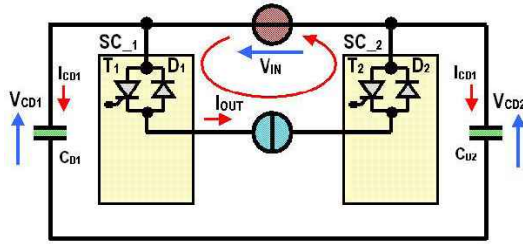


Figure 4-10.- Active energy exchange phase

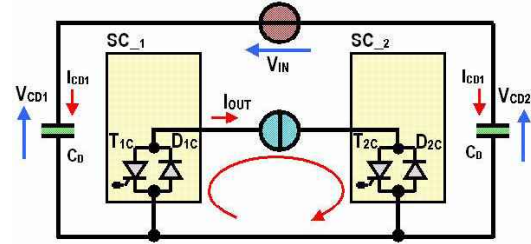


Figure 4-11.- Freewheeling phase

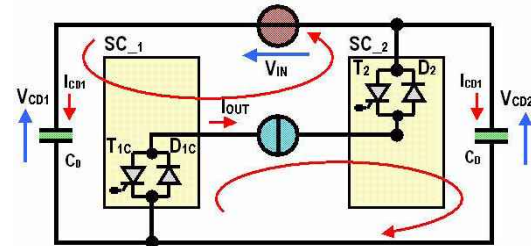
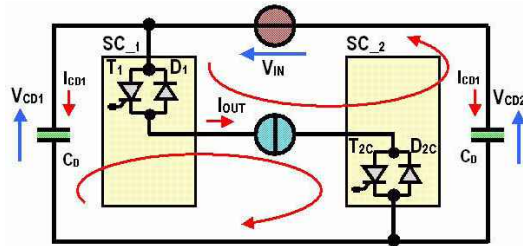


Figure 4-12.- Indirect energy exchange phases

During the indirect exchange phases generated by the switching cell dead times (all semiconductors off), the decoupling capacitors are charged by the output current source through the freewheeling diodes, Eq. 4-1, Eq. 4-2. Inversion of the output current polarity implies that the conducting diodes change from  $D_1$ - $D_{2C}$  ( $I_{OUT} < 0$ ) to  $D_2$ - $D_{1C}$  ( $I_{OUT} > 0$ ) and vice versa. As a result, the decoupling capacitors charging current during the dead times can be represented by the absolute value of the output source current (rectifier mode). This means that the voltage of the decoupling capacitor will be increased by a certain amount  $\Delta V_{CD1} = \Delta V_{CD2}$  on every dead time sequence, Eq. 4-3. This continuously charging process of the decoupling capacitors can not be allowed, therefore, adaptation of the switching pattern to avoid these effects and to guarantee the safe operation conditions of the semiconductors is required.

$$I_{CD1} = \frac{C_{D1}}{C_{D1} + C_{D2}} \cdot I_{OUT} \quad \text{Eq. 4-1}$$

$$I_{CD2} = \frac{C_{D2}}{C_{D1} + C_{D2}} \cdot I_{OUT} \quad \text{Eq. 4-2}$$

$$\Delta V_{CD1} = \Delta V_{CD2} = \frac{1}{C_{D1} + C_{D2}} \cdot \int_t^{t+T_D} |I_{OUT}(t)| \cdot dt \quad \text{Eq. 4-3}$$

Providing that only the Active and Freewheeling phases can be applied, the transition from one sequence to another must be assured avoiding the simultaneous conduction (input voltage short-circuit) or blocking (indirect exchange phase) of the four controlled semiconductors. Such operation requires additional information about which switching pattern has to be provided to guarantee the proper operation for each specific condition. Either detection of the input voltage or the output current sign can be used, [LEF-01]. However, since the output current ripple, introduced by the switching operation, is usually relatively higher than the input voltage ripple, accurate detection of the input voltage polarity is technically more feasible than detection of the output current polarity.

The switching strategy, adopting the input voltage polarity detection, consists in short-circuiting one of the switching cells according to the input voltage polarity, while the other switching cell operates in PWM mode with dead time generation. For example, if the input voltage  $V_{IN}$  is



positive, the switching cell  $SC_2$  is short-circuited and the switching cell  $SC_1$  operates in PWM, Figure 4-13. On the other hand, when  $V_{IN}$  is negative,  $SC_1$  is short-circuited and  $SC_2$  operates in PWM, Figure 4-14. This switching strategy respects the unidirectional voltage characteristic of the switching cells, limiting the voltage of the decoupling capacitors to the corresponding half cycle voltage of the input source. During the other half cycle, the switching cell voltage is zero.

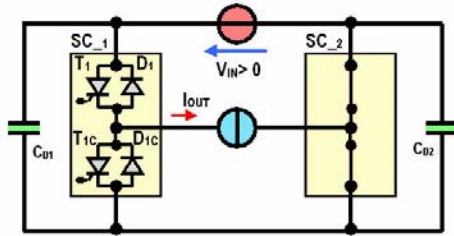


Figure 4-13.-  $V_{IN} > 0 \Rightarrow SC_2$  short-circuited,  $SC_1$  PWM operated

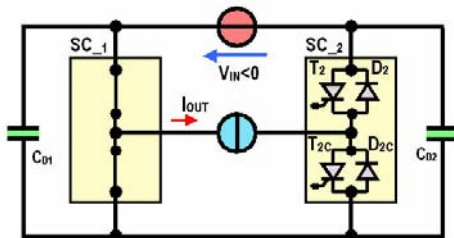


Figure 4-14.-  $V_{IN} < 0 \Rightarrow SC_1$  short-circuited,  $SC_2$  PWM operated

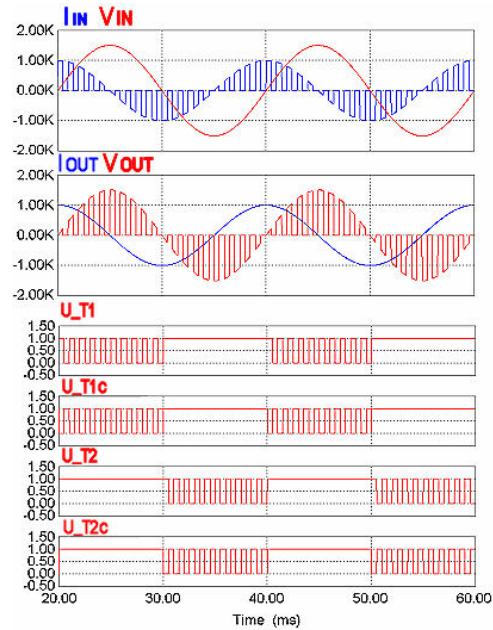


Figure 4-15.- Idealised PWM and waveforms for the differential step-down AC Chopper,  $\alpha=0.5$

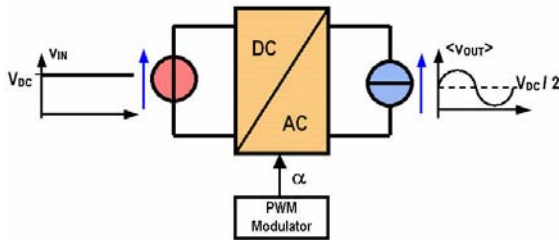
On each configuration, a reversible current buck converter can be identified, where the duty cycle  $\alpha$  defines the switching period averaged ratio between the input voltage  $V_{IN}$  and the output voltage  $V_{OUT}$ . The idealised PWM pattern, input and output current and voltage waveforms for the differential step-down AC Chopper in reactive power compensation are depicted in Figure 4-15.

The practical implementation of this kind of modulation must take into account the uncertainties on the input voltage zero crossing detection (polarity detection) introduced by the voltage sensor characteristics and the acquisition system (sensor accuracy, offset, speed, signal perturbation, etc.). Inaccuracy in the polarity detection could lead to erroneous sequence application resulting in an input voltage short circuit or an overcharge of the decoupling capacitors. To avoid these failure modes, the PWM operation can be stopped when the measured voltage signal is located inside a voltage band where the sign detection can be considered as inaccurate. In this region around the input voltage zero crossing, either the active phase or the freewheeling phase can be permanently applied. However, the change from the PWM operation to the fixed sequence generation around the zero crossing must be generated taking into consideration the semiconductors previous' state, while respecting their switching time restrictions. Obviously, this action disturbs the ideal output voltage characteristic of the converter, introducing an additional non-ideal behaviour of the system.

### 4.2.3 Modelling and Control of PWM AC Choppers

The ideal steady-state operation of the AC Choppers can be easily derived and explained by analogy with the well known PWM DC/DC choppers or DC/AC Voltage Source Inverters using averaging techniques. For instance, the ideal average output voltage of a VSI phase leg is proportional to the duty cycle. If the switching frequency is considerably high as compared with

the output fundamental frequency and the DC link voltage is constant, the duty cycle evolution has the same sinusoidal evolution as the desired phase voltage, Figure 4-16. In the step-down PWM AC chopper, the same principle can be applied. As the input voltage already has the desired output voltage waveform and the average output voltage is proportional to the duty cycle, the duty cycle is changed exclusively to modify the RMS amplitude of the output voltage, Figure 4-17.

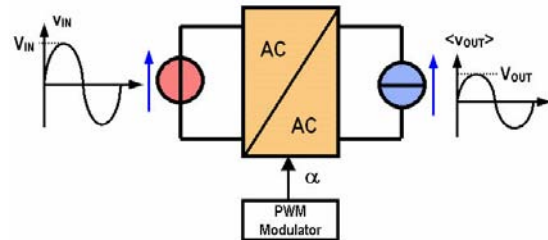


$$v_{IN} = V_{DC};$$

$$\langle v_{OUT} \rangle = \frac{V_{DC}}{2} + V_{OUT} \times \sin(\omega \times t);$$

$$\frac{\langle v_{OUT} \rangle}{\langle v_{IN} \rangle} = \frac{1}{2} + \frac{V_{OUT}}{V_{DC}} \times \sin(\omega \times t) = \alpha(t);$$

Figure 4-16.- Steady-state duty cycle for a VSI phase leg



$$v_{IN} = V_{IN} \cdot \sin(\omega \cdot t);$$

$$\langle v_{OUT} \rangle = V_{OUT} \cdot \sin(\omega \cdot t);$$

$$\frac{\langle v_{OUT} \rangle}{\langle v_{IN} \rangle} = \frac{V_{OUT}}{V_{IN}} = \alpha(t) = cte;$$

Figure 4-17.- Steady-state duty cycle for a single-phase step-down PWM AC Chopper

From a dynamic control point of view, classical linear averaging modelling techniques for PWM DC/DC converters have been successfully applied to several PWM AC Chopper topologies for different applications, [VEN-97b], [FED-01]. In these applications, the AC Choppers are designed to deal with low power values at high switching frequencies, aiming to cope with the modelling inaccuracies introduced by the assumptions of these techniques when they are applied to PWM AC Choppers, [KOR-01].

After averaging the model, a small-signal model is obtained by linearisation of the averaged system equations around a stable operation point. The small-signal model is valid only for small deviations around the operating point. However, PWM AC Choppers are excited with large levels of AC quantities and the effectiveness of this modelling technique is reduced significantly unless the sinusoidal voltage change is taken into account.

Another parameter that has a significant influence on the validity of the averaged model techniques, even for DC/DC converters, is the converter switching frequency. If the switching frequency is relatively low and the current and voltage switching ripples on the converter passive components are relatively high, the switching frequency terms can not be neglected and have influence on the average models. Several modelling solutions have been developed dealing with the influence of the switching frequency and the switching ripple effects, [KRE-90], [LEH-96a], [LEH-96b], [VER-99]. Most of the proposed solutions use complicated mathematical representations of the system, providing a better approximation of the converter behaviour reconstruction. However, their application for linear controllers' implementation is very restricted and they are mainly used to develop accurate simulation models with reduced computation time.

The non-linear characteristic operation of the AC Chopper (sinusoidal input voltage), together with the additional non-linear behaviour as with any other power converter (dead times, adapted switching patterns, etc), complicate the application of linear control strategies. Instantaneous compensation of the AC Chopper's non-linearity or use of non-linear control techniques (hysteresis controllers) can provide the required dynamic performance of the AC Choppers.

Obviously, due to the non-linear behaviour of PWM AC Choppers, which is emphasised when low switching frequencies are applied, imposes the use of computer-assisted verification of the proposed control solutions.

### 4.3 3MVAR PWM AC Chopper Based STATCOM for SNCF Single-Phase 25kV/50Hz Substations with 3.3kV IGCTs

The particularities of the reactive power compensation for the SNCF 25kV/50Hz substations arise mainly from the single-phase nature of the supply and the current harmonic generation restrictions imposed by the railway signalisation system in the frequency range between 1.6kHz and 2.7kHz. Also, additional characteristics of the reactive power compensation system such as size, acoustic noise, maintenance, reliability, etc., are arguments that favour the use of STATCOM systems in combination with the existing fixed capacitor stacks.

The variable reactive power capacity required for a single STATCOM system is rated to be 3MVAR. When combined with the maximum allowable fixed capacitor stacks already in use on the SNCF network (6MVAR) a maximum of 9MVAR of reactive power compensation can be totalised. Only reactive power compensation (capacitive behaviour) is required. A better use of the reactive compensation system can be obtained if a combination of two 3MVAR fixed capacitors stacks with a 3MVAR STATCOM is used, providing dynamic control of the compensated reactive power in the whole power range (from 0 to 9MVAR), Figure 4-18. The fixed capacitor stacks can be connected and disconnected (mechanical switches) according to the compensation requirements of the substation, while the 3MVAR STATCOM can control dynamically the compensation on each 3MVAR step range. The dynamic response time of the STATCOM is specified to be lower than 200ms.

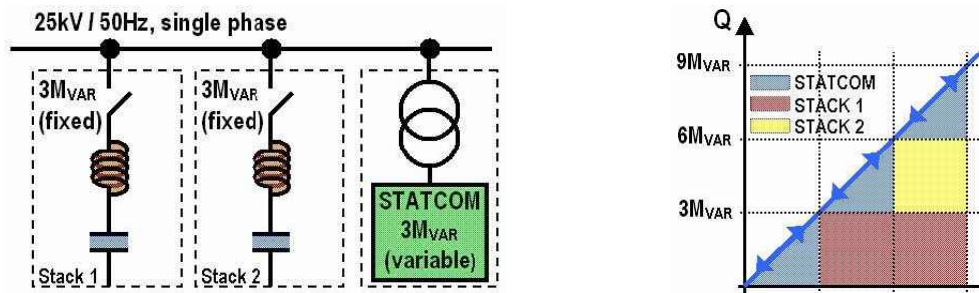


Figure 4-18.- Hybrid reactive power compensation system, ( passive 6MVAR - active 3MVAR)

The STATCOM solution presented here is based on single-phase step-down PWM AC Choppers using 3.3kV IGCTs. The required 3MVAR reactive power compensation capability is obtained by arranging three 1MVAR modules in parallel ( $n=3$ ), Figure 4-19. The modules are connected to a single input LC filter ( $L_F-C_F$ ) on the secondary side of a single-phase step-down transformer. The secondary nominal voltage of the transformer is  $V_{NET}=1.06kV_{RMS}$  ( $m_C \approx 23.6$ ), which imposes a maximum nominal voltage value of 1.5kV adapted to the IGCT ratings. The output load of each PWM AC Chopper consists of another LC circuit ( $L_S-C_V$ ) with capacitive behaviour at the network frequency to provide the desired reactive power compensation function. The smoothing inductor  $L_S$  is required to provide a current source behaviour for the load and to limit the switching current ripple. To guarantee the balanced operation of the 3 modules, each module has its own control loop and receives the same compensation reference.

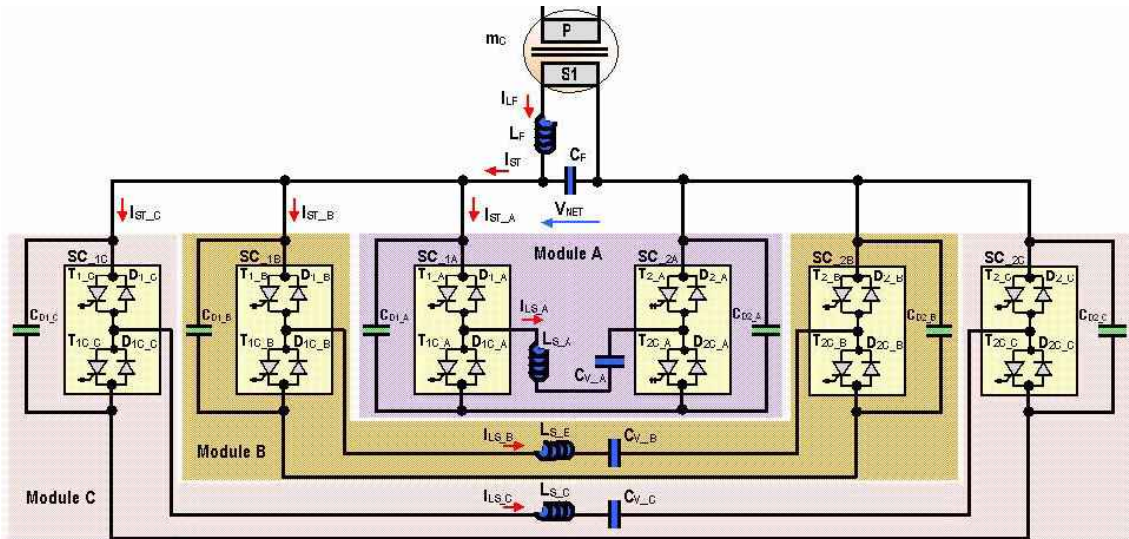


Figure 4-19.- 3 MVAR STATCOM based on step-down PWM AC Choppers with 3.3kV IGCTs (n=3)

Regarding the harmonic current generation of the STATCOM, the switching frequency of each module is fixed at  $f_{sw}=1\text{kHz}$  (maximum switching frequency imposed by standard IGCT gate units). Applying the interleaving strategy to the PWM carriers of the three modules ( $120^\circ$  phase shifted), Figure 4-20, the first relevant high frequency harmonics of the STATCOM input current  $I_{ST}$  are ideally generated at  $n \cdot f_{sw}=3\text{kHz}$  (multilevel current waveform), which is located above the upper frequency limit of the SNCF signalisation frequency range (2.7kHz). The input filter ( $L_F-C_F$ ) attenuates the high frequency current harmonics generated by the converter and must provide unity gain at the network frequency. Obviously, the input filter capacitor provides already a certain amount of fixed reactive power compensation. The use of the transformer leakage inductance, either entirely or partly, for the input filter inductor  $L_F$  must be considered.

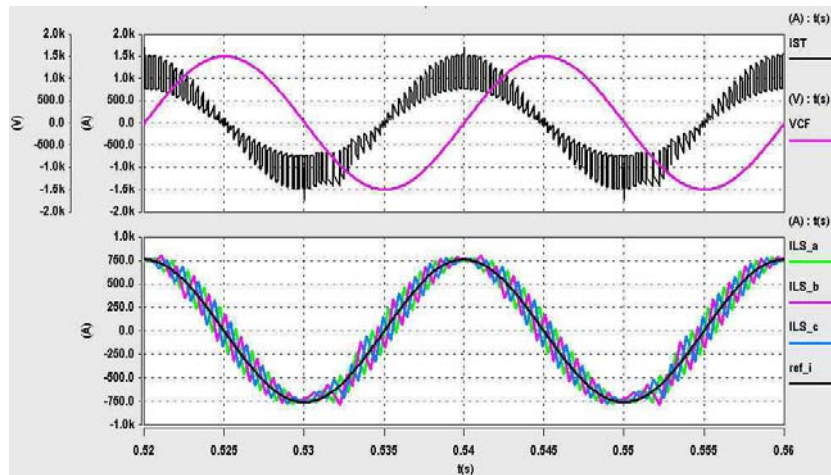


Figure 4-20.- Interleaving operation of the three PWM AC Chopper modules, ( $\alpha \approx 0.5$ )

Although the first high frequency harmonics are ideally displaced to the 3kHz range, the real behaviour of the converter (switching frequency side bands, output current ripple, dead times, control loop operation, PWM timing generation, etc.) can generate non-desired current harmonics within the forbidden frequency range imposed by the signalisation system of the SNCF (1.6kHz-2.7kHz). The input filter should provide the required attenuation to comply with the limit imposed by the SNCF standards. However, if the input filter is not sufficient enough to provide the required

attenuation, additional harmonic trap filters for the concerned frequency range can be used to reduce the current harmonics below the imposed limits (10mA in the worst case). Since the adopted modulation strategy tries to avoid the harmonics generation below 3kHz, the current rating of the trap filters will be very low compared to the reactive current compensation values. Figure 4-21 shows the simulated spectrum of the STATCOM current before filtering,  $I_{ST}$ , for operation of the PWM AC Chopper at duty cycle around  $\alpha \approx 0.5$ . As can be seen, peak current values of more than 10A are generated in the SNCF signalisation frequency range. To assure the harmonic current values below 10mA (worst case) on the 25kV/50Hz line, attenuation higher than 60dB could be required. In principle, this attenuation could be obtained only with the LC input filter (-40dB/dec) and the current gain introduced by the transformer turns ratio (-27.4dB). However, as the harmonic levels allowed are very low, only the behaviour of the compensation system installed in real field will allow taking into account all the possible interactions not considered in the simulations to definitively identify the need of additional filtering. Also, since low frequency harmonics are generated with relatively low amplitudes, attention must be paid to the resonant input filter excitation.

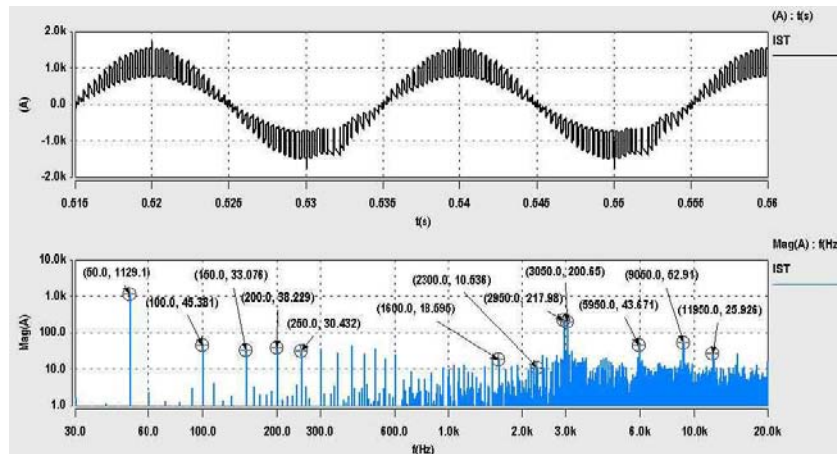


Figure 4-21.- Harmonic spectrum of the PWM AC CHOPPER based STATCOM current  $I_{ST}$ , ( $\alpha \approx 0.5$ )

### 4.3.1 Design of a 1MVAR Step-down PWM AC Chopper Module

The design of a basic 1MVAR step-down PWM AC Chopper Module concerns the selection of the components to be used, the definition of their operating conditions, and also the control and modulation strategies to be applied for stable, accurate and safe operation of the converter.

#### 4.3.1.1 Dimensioning of the power stage components

The use of 3.3kV IGCTs in PWM AC Choppers for reactive power compensation of the SNCF 25kV/50Hz substations has been reported previously in section 3.3.2.2, stating the ability to provide 1MVAR of reactive power compensation with the semiconductor steady-state maximum ratings reaching 1.5kV/ 1.5kA at  $f_{SW}=1$ kHz. Under these operating conditions, the maximum IGCT total losses are lower than 800W whereas the 1MVAR module semiconductor total losses (4 IGCTs and 4 diodes) are lower than 3.9kW, which could lead to the use of air-cooling instead of water-cooling. The dimensioning considerations for the remaining components of the power stage are presented in the next sections.

### 4.3.1.1.1 Output load components, $L_S - C_V$

The selection of the output load inductor  $L_S$  and capacitor  $C_V$  values is mainly determined by the amount of reactive power energy to be compensated. Nevertheless, multiple  $L_S$ - $C_V$  coupled values can provide the required compensation capability. Therefore, additional selection criteria must be considered to select the components values.

The reactive power compensation adjustable range of the STATCOM module can be derived by evaluation of the reactive power drawn by the load if ideal power transfer between the input and the output of the AC Chopper is considered and the influence of input filter is not taken into account, Figure 4-22. The maximum reactive power compensation  $Q_{MAX}$  is fixed by the maximum AC Chopper voltage ( $V_{ACC}$ ) and by the characteristic impedance ( $Z_{LC}$ ) of the  $L_S$ - $C_V$  load at the network frequency ( $\omega=2\cdot\pi\cdot f$ ), Eq. 4-7. The maximum AC Chopper voltage is given by the network voltage  $V_{NET}$  (transformer's secondary side) and by the maximum duty cycle achievable by the converter, ( $\alpha_{MAX}$  typically limited to 0.95). As a consequence, the maximum fundamental current of the load, that is, the maximum fundamental current switched by the semiconductors, is imposed, Eq. 4-6.

$$Z_{LC} = \frac{1-L_S \cdot C_V \cdot \omega^2}{C_V \cdot \omega} \tag{Eq. 4-4}$$

$$V_{ACC\_MAX} = V_{NET} \cdot \alpha_{MAX} \tag{Eq. 4-5}$$

$$I_{LS\_MAX} = \frac{V_{ACC\_MAX}}{Z_{LC}} = V_{NET} \cdot \alpha_{MAX} \cdot \frac{C_V \cdot \omega}{1-L_S \cdot C_V \cdot \omega^2} \tag{Eq. 4-6}$$

$$Q_{MAX} = V_{ACC\_MAX} \cdot I_{LS\_MAX} = V_{NET}^2 \cdot \alpha_{MAX}^2 \cdot \frac{C_V \cdot \omega}{1-L_S \cdot C_V \cdot \omega^2} \tag{Eq. 4-7}$$

$I_{LS\_MAX}$ = Maximum RMS current of  $L_S$  (50Hz)

Obviously, the LC load must have capacitive behaviour at the network frequency (50Hz) to provide reactive power compensation (capacitive). This implies that the capacitor impedance must be higher than the inductor impedance, leading to a  $L_S$ - $C_V$  load resonant frequency ( $f_R$ ) higher than the network frequency ( $f$ ), Figure 4-23.

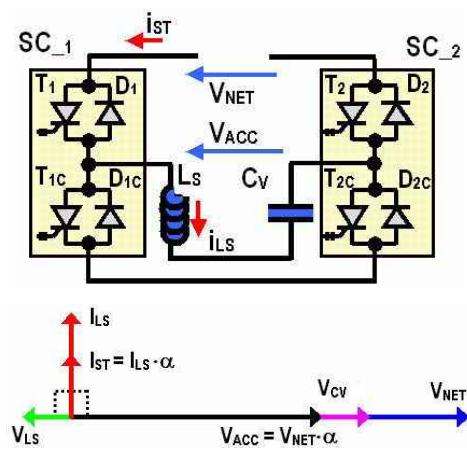


Figure 4-22.- AC Chopper based STATCOM steady-state vector diagram

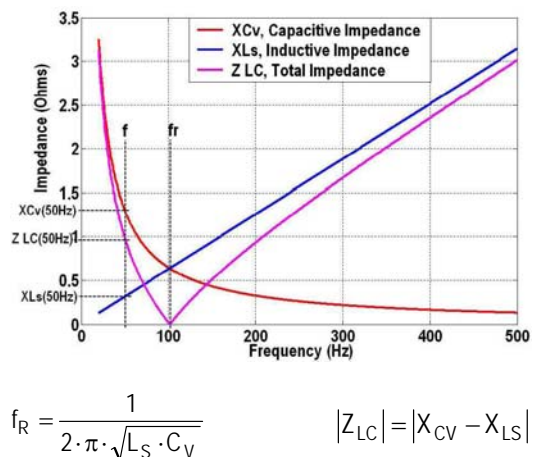


Figure 4-23.- Load  $L_S$ - $C_V$  impedance versus frequency

$$f_R = \frac{1}{2 \cdot \pi \cdot \sqrt{L_S \cdot C_V}} \quad |Z_{LC}| = |X_{Cv} - X_{Ls}|$$

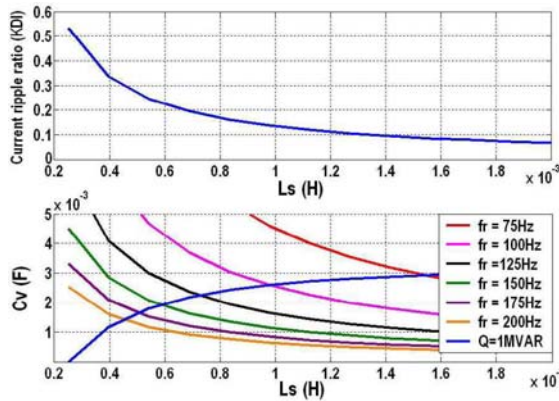
Additional considerations regarding the switching frequency  $f_{sw}$  involve the location of the load resonant frequency. The converter controller must have a bandwidth  $f_{BW}$  wide enough to

compensate eventual excitations of the resonant load and provide stable operation to the system. Consequently, the load resonant frequency must be within the converter bandwidth. As the converter bandwidth is directly related to the switching frequency, this consideration leads to a load resonant frequency much lower than the switching frequency ( $f < f_R < f_{SW}$ ).

From a high frequency point of view, the current ripple on the output inductor must be considered as relevant parameter for selection of the load component values. A trade off between the current ripple and the size of the inductor must be obtained. As the maximum current ripple expression shows, Eq. 4-8 (see Appendix 1), only the inductor value and the input maximum voltage exert influence on the current ripple value at a given switching frequency.

$$\Delta I_{LS_{MAX}} = \Delta I_{LS}(\alpha = 0.5) = \frac{V_{NET} \cdot \sqrt{2}}{4 \cdot L_S \cdot f_{SW}} \quad \text{Eq. 4-8}$$

Taking into account all the previously stated considerations, the following procedure has been applied to make the selection of the load component values. First, the current ripple ratio  $K_{\Delta I}$  is defined, Eq. 4-9, and evaluated for a certain range of the inductor values. Then, the capacitor values are evaluated for the considered inductor values to obtain a family of curves  $C_V$  versus  $L_S$  at constant resonant frequency  $f_R$ , Eq. 4-10. Finally, for the  $f_R$  range previously considered, the capacitor value is calculated, Eq. 4-11, to provide the maximum reactive power compensation  $Q_{MAX}$ , obtaining a  $C_V$  versus  $L_S$  curve at constant  $Q$ . The intersection points of the curve at constant  $Q$  superposed with the family of curves at constant  $f_R$  allows defining the capacitor value for a selected inductor value, Figure 4-24. This graphical method allows the designer to find quickly the values of  $C_V$ ,  $L_S$  for a specific trade off between  $f_R$  and  $K_{\Delta I}$  and the desired  $Q_{MAX}$ . The trade off between all these parameters must be defined by the designer, taking into account additional criteria such as cost and size of the inductor and capacitor, current ripple, etc. The resonant frequency range must be considered only between the network frequency and the maximum available bandwidth of the converter ( $f_{BW} \approx f_{SW}/5$ )



$$K_{\Delta I} = \frac{\Delta I_{LS\_MAX}}{2 \cdot \sqrt{2} \cdot I_{LS\_MAX}} = \frac{V_{NET}^2 \cdot \alpha_{MAX}}{8 \cdot L_S \cdot f_{SW} \cdot Q_{MAX}} \quad \text{Eq. 4-9}$$

$$C_V = \frac{1}{4 \cdot \pi^2 \cdot f_R^2 \cdot L_S} \quad \text{Eq. 4-10}$$

$$C_V = \frac{Q_{MAX}}{2 \cdot \pi \cdot f \cdot V_{NET}^2 \cdot \alpha_{MAX}^2} \cdot \frac{f_R^2 - f^2}{f_R^2} \quad \text{Eq. 4-11}$$

$I_{LS\_MAX}$  = Maximum RMS current of  $L_S$  (50Hz)  
 $V_{NET}$  = Nominal RMS secondary voltage (50Hz)

Figure 4-24.- Graphical evaluation of  $L_S$ ,  $C_V$  ( $f_R$  and  $K_{\Delta I}$  trade off for  $Q_{MAX}=1\text{MVAR}$ )

In this case,  $L_S$  is selected to be 1mH and  $C_V$  2.45mF imposing a resonant frequency  $f_R$  around 100Hz and a current ripple ratio  $K_{\Delta I}$  around 14%. Obviously, the maximum reactive power  $Q_{MAX}$  is 1MVAR. Table 4-1 summarises the selected parameters.

$Q_{MAX}$	$V_{NET}$	$I_{LS\_MAX}$	$L_S$	$C_V$	$K_{\Delta I}$	$f_R$
1MVAR	1.06kV <sub>RMS</sub>	995A <sub>RMS</sub>	1mH	2.45mF	0.14	101Hz

Table 4-1.- Load components values ( $Q_{MAX}=1\text{MVAR}$ )

### 4.3.1.1.2 Clamp Circuit components, $L_{CL}$ , $R_{CL}$ , $C_{CL}$ , $D_{CL}$

Safe switching of the IGCTs and their associated freewheeling diodes requires the use of a  $di/dt$  limitation inductor ( $L_{CL}$ ) at the IGCT turn-on (turn-off of the FWD). A RCD clamp circuit ( $R_{CL}$ ,  $C_{CL}$ ,  $D_{CL}$ ) is required to limit the IGCT turn-off over-voltage generated by the discharging of the energy stored by the  $di/dt$  limitation inductor in the previous on-state. In contrast to the topologies with DC links where a clamp circuit can be shared by more than one switching cell if the switching transitions are respected, each switching cell in the PWM AC choppers must be equipped with its own clamp circuit because the link to the power supply is not common, Figure 4-25. The clamp capacitors  $C_{CLX}$  play the role of the required decoupling capacitors of the switching cell.

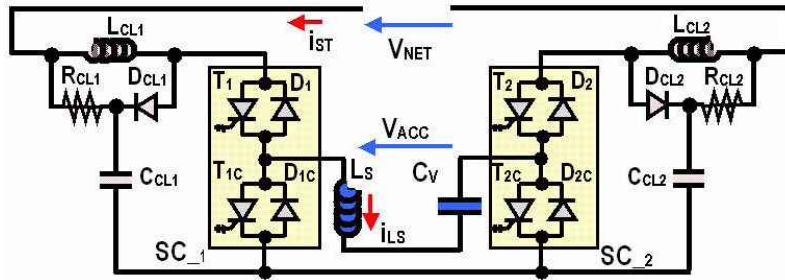


Figure 4-25.-  $di/dt$  and clamp circuit s of the step-down PWM AC Chopper switching cells

Although the switching cell voltage in the PWM AC Choppers, presents the sinusoidal evolution of one half cycle of the input voltage  $V_{NET}$ , the dimensioning of the clamp circuit is identical to that of the DC link topologies. The dimensioning must be performed for the maximum input voltage to limit the maximum  $di/dt$  at turn-on of the IGCTs. Obviously, as the switching cell voltage is changing according to the input voltage and the  $di/dt$  limitation inductor is fixed, the turn-on  $di/dt$  changes throughout the network period and so the turn-on transient time.

Considering the switching cell maximum voltage to be 1.8kV (the nominal voltage is 1.5kV), the maximum switching current 1.5kA and limiting the maximum  $di/dt$  to  $1\text{kA}/\mu\text{s}$ , selection of the  $di/dt$  limitation and clamp circuit components is performed (see 1.3.1.3).

$V_{NET\text{ MAX}}$ , Maximum Switching cell voltage	1.8kV	$L_{CL\text{ MIN}} = 1.8\mu\text{H}$
$di/dt_{\text{MAX}}$ , maximum $di/dt$ at IGCTs turn on	$1\text{kA}/\mu\text{s}$	
$\Delta V_{CL\text{ MAX}}$ , maximum semiconductors voltage overshoot	515V	$C_{CL} = 6\mu\text{F}$
$t_{B\text{ MAX}}$ , maximum blocking transition time	$6.86\mu\text{s}$	$R_{CL} = 0.75\Omega$

Table 4-2.- Clamp circuit parameters selection for the step-down PWM AC Chopper

Besides the normal operation of the clamp circuit along with the switching sequence of the PWM AC Chopper switching cell, additional transient current and voltages are induced on the switching cell semiconductors and clamp circuit during the switching cell short-circuit state. In fact, even if the switching cell is short-circuited, the switching operation of the adjacent switching cell generates current step changes that excite the short-circuited switching cell clamp circuit and  $di/dt$  limitation inductor. The excitation of this LCR resonant circuit generates a high frequency resonant current that is added to the load current seen by the short-circuited semiconductors (IGCTs or diodes). However, as the semiconductors are ideally in continuous on-state (no switching operation is being performed), this operation mode should not present any risk to the semiconductors. Also, a resonant voltage appears on the clamp capacitor and  $di/dt$  inductor, but the peak value of this voltage should not be harmful for the components because they are initially working at zero voltage and the resonant circuit is well damped by the clamp circuit resistors  $R_{CL}$ .



Even, this spike voltage cannot affect directly to the adjacent switching cell semiconductors because they are well protected by their own clamp circuit.

To verify the assumptions previously mentioned, analysis of the transient behaviour of the circuit is performed. Figure 4-26 shows the equivalent high-frequency (transient) circuit when the switching cell SC<sub>2</sub> is short-circuited and the switching cell SC<sub>1</sub> operates in switching mode. The switching operation of SC<sub>1</sub> is represented by a step current source and the SC<sub>2</sub> semiconductors are ideally represented by 0Ω resistors. The input voltage capacitor filter C<sub>F</sub> is supposed to behave as a short-circuit at high frequencies and several parasitic inductance are also considered (L<sub>LK</sub>, parasitic inductance between the input capacitor and the clamp circuits, L<sub>LK1</sub> and L<sub>LK2</sub> parasitic inductance of the switching cell switching paths). The reduced equivalent circuit of the system is shown in Figure 4-27, assuming that the clamp circuit diodes D<sub>CLX</sub> are blocked.

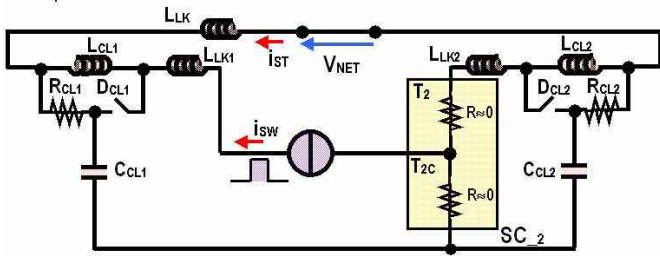


Figure 4-26.- High-frequency equivalent circuit for clamp circuit transient operation (SC<sub>2</sub> short-circuited)

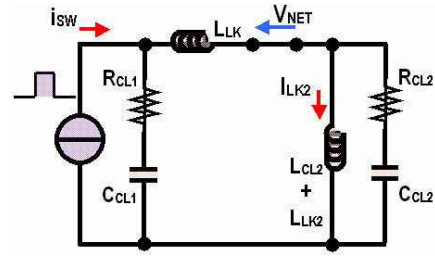
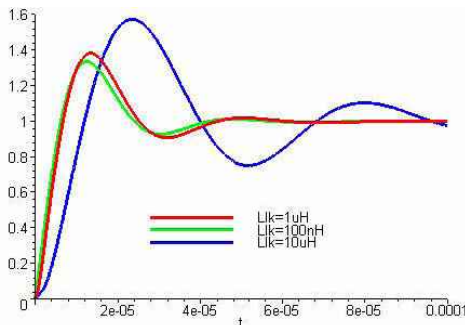


Figure 4-27.- Reduced high-frequency equivalent circuit SC<sub>2</sub> short-circuited)

Analysis of the transfer function between the parasitic inductor current I<sub>LK2</sub> and the SC<sub>1</sub> switched current I<sub>SW</sub>, Eq. 4-12, allows obtaining the characteristic resonant frequency (f<sub>TR</sub>) and damping factor (ξ<sub>TR</sub>) of the established resonant circuit as well as the transient peak current ratio with respect to the switched current, (ΔI<sub>TR</sub>/I<sub>SW</sub>). Obviously, to obtain numerical values, approximation of the parasitic inductor values must be considered.

$$\frac{I_{LK2}}{I_{SW}} = \frac{1}{\frac{(L_{CL2} + L_{LK2}) \cdot C_{CL2} \cdot s^2}{R_{CL2} \cdot C_{CL2} \cdot s + 1} + 1 + \frac{C_{CL1} \cdot s^2}{R_{CL1} \cdot C_{CL1} \cdot s + 1} \left[ L_{CL2} + L_{LK2} + L_{LK} \cdot \left( \frac{(L_{CL2} + L_{LK2}) \cdot C_{CL2} \cdot s^2}{R_{CL2} \cdot C_{CL2} \cdot s + 1} + 1 \right) \right]} \quad \text{Eq. 4-12}$$

Taking into account the selected clamp circuit values, and imposing the switching path parasitic inductors to L<sub>LK1</sub>=L<sub>LK2</sub>= 300nH (IGCT datasheet typical value), the influence of the parasitic inductance between the input filter capacitor and the switching cells L<sub>LK</sub> on the transient response is evaluated.



L <sub>LK</sub>	f <sub>TR</sub> , resonant frequency	ξ <sub>TR</sub> , damping ratio	ΔI <sub>TR</sub> / I <sub>SW</sub> , peak current ratio
100nH	28.2kHz	0.497	1.36
1μH	27.1kHz	0.464	1.39
10μH	17.7kHz	0.268	1.59

Figure 4-28.- Relative I<sub>LK2</sub> step transient response and characteristic parameters (I<sub>SW</sub>=1, L<sub>LK</sub>=100nH, 1μH and 10μH)

Figure 4-28 shows the step transient response of  $I_{LK2}$  (current on the short-circuited switching cell) for  $L_{LK}=100\text{nH}$ ,  $1\mu\text{H}$  and  $10\mu\text{H}$ . It can be noticed that the higher the  $L_{LK}$  value, the higher the semiconductors peak current (lower damping ratio), which leads to the conclusion that minimisation of the parasitic inductance between the capacitor of the input filter and the switching will lead to minimisation of the stress generated by the presence of the clamp circuit during the switching cell short-circuit state. Transient simulations considering ideally switched models are performed verifying the analytically derived previous results, Figure 4-29. In addition, the voltage waveform across the clamp capacitor  $C_{CL2}$  is obtained and identified to be lower than 200V. However, even if some parasitic elements have been taken into account in the analysis, the real behaviour of the semiconductors (parasitic inductors and capacitors, switching transients speed, etc) and additional parasitic elements could modify the transient response of the system, which requires practical verification in real operation.

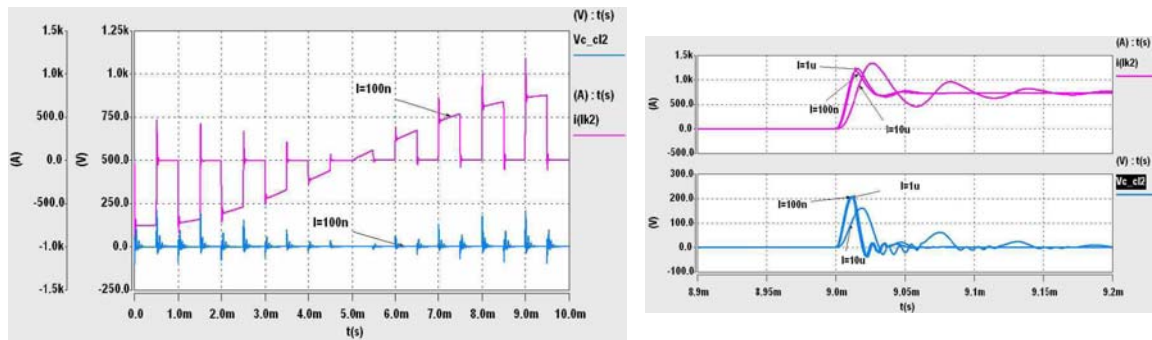
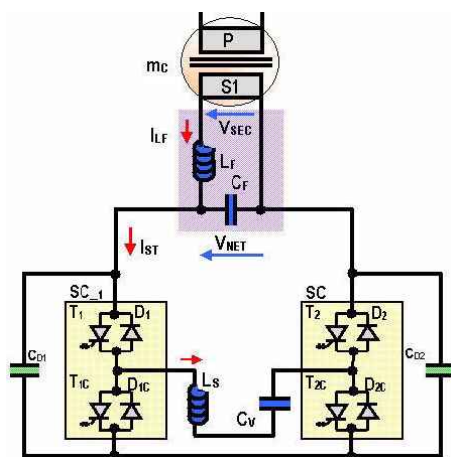


Figure 4-29.- Clamp circuit transient response ( $I_{LK2}$   $V_{C_{CL2}}$ ) at switching cell short circuit state

### 4.3.1.1.3 Input filter components, $L_F - C_F$

The input filter values, Figure 4-30, must be selected according to several low and high frequency criteria that allow obtaining proper operation of the system. However, the selection criteria must take into account the operation of the  $n=3$  PWM AC Chopper modules operating in parallel to obtain the required 3MVAR reactive power compensation and applying the interleaving strategy to reduce the high frequency harmonics introduced by the STATCOM switching operation.



$$f_{RF} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_F \cdot C_F}} \quad \text{Eq. 4-13}$$

Figure 4-30.-  $L_F, C_F$  PWM AC Chopper filter

The current harmonics generated by the AC Choppers must be attenuated to comply with the network standards, paying special attention to this application where the high frequency current harmonics have to be avoided according to the SNCF signalisation requirements as seen before.

The resonant frequency of the input filter  $f_{RF}$ , Eq. 4-13, defines the attenuation ratio provided by the filter with respect to the high frequency harmonics generated by the converter (second order filter, -40dB/dec). In addition, to provide stable operation of the control system and to avoid the excitation of the resonant  $L_F C_F$  input filter, the resonant frequency  $f_{RF}$  should be located above the bandwidth of the controller ( $f_{BW} \approx f_{SW}/5$ ).

Besides the current harmonic attenuation, the high frequency input voltage ripple introduced by the AC Chopper input switched current must be reduced as much as possible to avoid disturbing the stable operation of the converter (zero crossing detection, input voltage oscillation, etc.). The  $C_F$  current induced by the switching operation is the load output current  $I_{LS}$  during the PWM AC Chopper active state ( $0-\alpha \cdot T_{SW}$ ), and zero during the freewheeling state ( $\alpha \cdot T_{SW}-T_{SW}$ ). Considering the fundamental component of  $I_{LS}$  (current ripple omission), Eq. 4-14, the voltage ripple evolution for  $n$  modules is given by Eq. 4-15. As Eq. 4-16 shows, besides the influence of the input voltage  $V_{NET}$ , the output load impedance  $Z_{LC}$ , the input capacitor value  $C_F$  and the switching frequency  $f_{SW}$ , the maximum voltage ripple depends on the number "n" of modules to be paralleled. The higher the number of modules, the lower the voltage ripple, Figure 4-31.

$$I_{LS} = \frac{V_{NET} \cdot \sqrt{2}}{Z_{LC}} \cdot \alpha \cdot \cos(\omega \cdot t) \quad \text{Eq. 4-14}$$

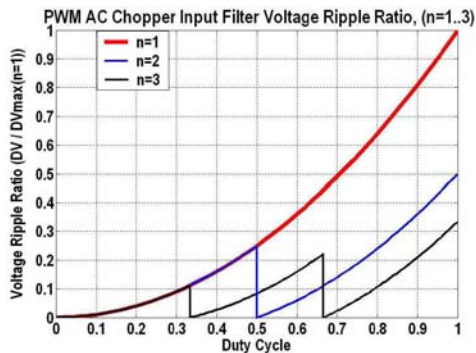
$$\Delta V_{CF} = \frac{V_{NET} \cdot \sqrt{2}}{Z_{LC} \cdot C_F \cdot f_{SW}} \cos(\omega \cdot t) \cdot \frac{\alpha}{n} \cdot (n \cdot \alpha - (SN-1)) \quad \text{Eq. 4-15}$$

$SN = 1, 2, \dots, n$  (duty cycle Sector Number according to the duty cycle value)

$$\frac{(SN-1) \cdot T_{SW}}{n} < \alpha < \frac{SN \cdot T_{SW}}{n};$$

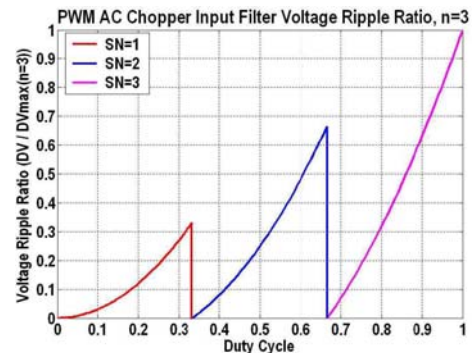
$$\Delta V_{CF\_MAX} (\alpha \approx 1) = \frac{V_{NET} \cdot \sqrt{2}}{Z_{LC} \cdot n \cdot C_F \cdot f_{SW}} \quad \text{Eq. 4-16}$$

Since the output load current amplitude increases with  $\alpha$  and the active phase time is also defined by  $\alpha$ , the voltage ripple shows a quadratic evolution with respect to  $\alpha$  where the maximum value occurs at  $\alpha \approx 1$ . The voltage ripple characteristic shows several discontinuities in the boundaries of each duty cycle sector number  $SN$  (function of the number of modules, Eq. 4-15) where zero voltage ripple is obtained. For  $n=3$ , the zero voltage ripple is obtained at  $\alpha=0$ ,  $1/3$ ,  $2/3$  and  $1$ , Figure 4-32. The voltage ripple ratio  $K_{\Delta V}$  between the high frequency and low frequency peak voltages is used to quantify relatively the input filter voltage ripple, Eq. 4-17.



$$\frac{\Delta V_{CF}}{\Delta V_{CF\_MAX}(n=1)}; \quad \Delta V_{CF\_MAX}(n=1) = \frac{V_{NET} \cdot \sqrt{2}}{Z_{LC} \cdot C_F \cdot f_{SW}}$$

Figure 4-31.-  $C_F$  voltage ripple evolution ( $n=1..3$ )



$$\frac{\Delta V_{CF}(n=3)}{\Delta V_{CF\_MAX}(n=3)}; \quad \Delta V_{CF\_MAX}(n=3) = \frac{V_{NET} \cdot \sqrt{2}}{Z_{LC} \cdot 3 \cdot C_F \cdot f_{SW}}$$

Figure 4-32.-  $C_F$  voltage ripple evolution,  $n=3$

$$K_{\Delta V} = \frac{\Delta V_{CF\_MAX}}{2 \cdot \sqrt{2} \cdot V_{NET}} = \frac{1}{6 \cdot Z_{LC} \cdot C_F \cdot f_{SW}} \quad \text{Eq. 4-17}$$

From a low frequency point of view, since the input filter resonant frequency  $f_{RF}$  must be greater than the network frequency  $f$ , the input filter acts as a constant capacitive load connected to the network ( $X_{LF}(50\text{Hz}) \ll X_{CF}(50\text{Hz})$ ). Therefore, a minimum fixed reactive compensation  $Q_{CF}$ , Eq. 4-18, is added to the adjustable reactive power compensation  $Q_{ADJ}$  (Eq. 4-19) of the STATCOM, Figure 4-33. Obviously, this fixed reactive power compensation should be as low as possible, which leads to the trend of  $C_F$  minimisation.

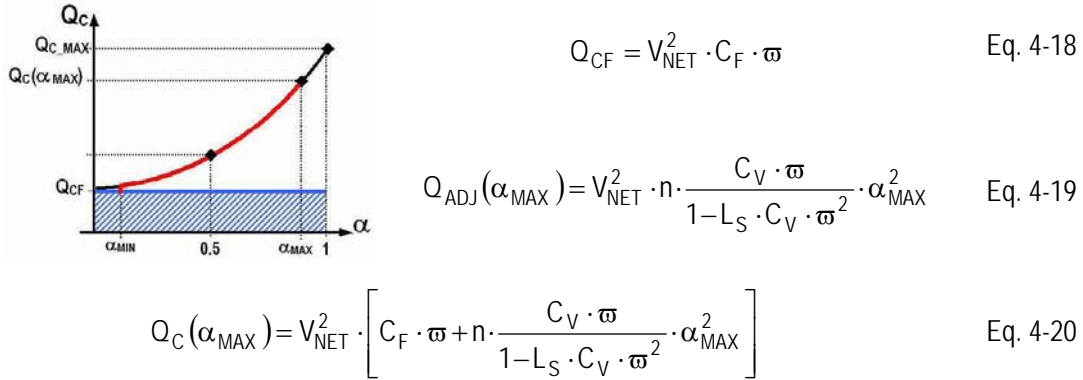


Figure 4-33.- PWM AC Chopper reactive power characteristic ( fixed  $Q_{CF}$ )

Regarding  $L_F$ , as shown in the vector diagram of Figure 4-34, its voltage drop is added to the secondary side voltage  $V_{SEC}$ . As a result, the voltage seen by the converters  $V_{NET}$  is higher than the secondary side voltage  $V_{SEC}$  and increases with the reactive power compensated by the STATCOM ( $\alpha^2$ ), Eq. 4-22. Obviously, the operation of the STATCOM must be restricted if the maximum allowable voltage of the semiconductors is reached ( $V_{NET}=1.27\text{kV}_{RMS}$  for 1.8kV maximum semiconductor voltage). Furthermore, this voltage drop across the inductor  $L_F$  reduces the total reactive power injected to the network for a given STATCOM input voltage  $V_{NET}$ , ( $Q_{SEC}$ , Eq. 4-23). For these reasons, the inductor value  $L_F$  must be selected as low as possible.



Figure 4-34.- System steady-state vector diagram considering the input filter  $L_F$ ,  $C_F$

$$I_{LF} = I_{CF} + I_{ST} \quad I_{LF} = V_{NET} \cdot \left[ C_F \cdot \omega + n \cdot \frac{C_V \cdot \omega}{1 - L_S \cdot C_V \cdot \omega^2} \cdot \alpha^2 \right] \quad \text{Eq. 4-21}$$

$$V_{NET} = V_{SEC} + L_F \cdot \omega \cdot I_{LF} \quad V_{NET} = V_{SEC} \cdot \frac{1}{1 - L_F \cdot \omega \cdot \left[ C_F \cdot \omega + n \cdot \frac{C_V \cdot \omega}{1 - L_S \cdot C_V \cdot \omega^2} \cdot \alpha^2 \right]} \quad \text{Eq. 4-22}$$

$$Q_{SEC} = V_{SEC} \cdot I_{LF} \quad Q_{SEC} = V_{NET}^2 \cdot (1 - L_F \cdot \omega \cdot Y_{EQ}) \cdot Y_{EQ} \quad \text{Eq. 4-23}$$

$$Y_{EQ} = C_F \cdot \omega + n \cdot \frac{C_V \cdot \omega}{1 - L_S \cdot C_V \cdot \omega^2} \cdot \alpha^2$$

A trade off between all these selection criteria must be defined to obtain the values of the components. Since the voltage ripple  $\Delta V_{CF}$  and the fixed reactive power  $Q_{CF}$  are directly dependent on the input capacitor value  $C_F$  (the rest of the parameters being already fixed), the solution here proposed consists of defining a trade off between these two parameters and derive then the lower inductor value  $L_F$  imposing a convenient resonant frequency  $f_{RF}$ , Figure 4-35. The selection of  $L_F$  is mainly driven by the minimisation of the resonant frequency  $f_{RF}$  to provide the maximum attenuation of the high frequency harmonics generated by the STATCOM. The restriction imposed by the maximum operating voltage of the converters  $V_{NET}$  imposes the maximum value of  $L_F$ , Eq. 4-24.

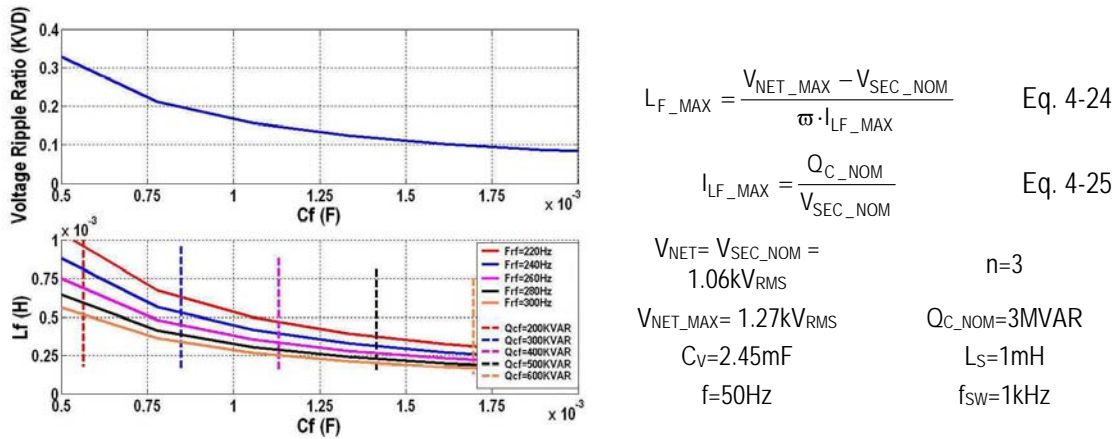


Figure 4-35.-  $K_{\Delta V}$ ,  $Q_{CF}$  and  $f_{RF}$  interrelation characteristics for  $L_F$  and  $C_F$  selection

$C_F$  is selected to be 1.8mF, which leads to a fixed reactive power compensation  $Q_{CF}=635kVAR$  (around 20% of the reactive power range,  $Q_{C\_NOM}= 3MVAR$ ) and a voltage ripple ratio  $K_{\Delta V}<0.10$  ( $\Delta V_{CF}=285V$ ) for  $V_{NET}=1.06kV_{RMS}$ . Selection of  $L_F=240\mu H$  fixes the resonant frequency to  $f_{RF}=240Hz$ . Later verification of the current harmonic amplitudes generated in the trains signalisation frequency range will clarify if additional filters (trap filter, etc) are required. Table 4-3 summarises the selected parameters.

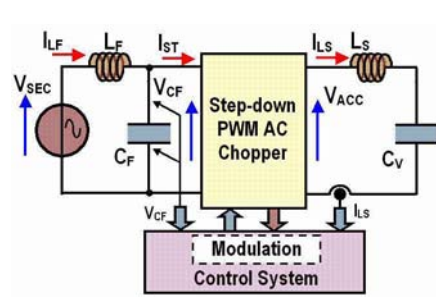
$Q_{CF}$	$V_{NET}$	$L_F$	$C_F$	$K_{\Delta V}$	$f_{RF}$	$n$
0.635MVAR	1.06kV <sub>RMS</sub>	240 $\mu$ H	1.8mF	0.10	240Hz	3

Table 4-3.- Input filter components values ( $n=3$ ,  $Q_{ADJ}= 3MVAR$ )

Notice that the transformer leakage inductance can be used as part of the  $L_F$  inductor. For a 3MVAR transformer with short-circuit impedance  $Z_{CC}=6\%$  and power factor  $\cos(\varphi_{CC})=0.8$ , the secondary side equivalent leakage inductance  $L_{LK\_TR}$  and resistor  $R_{LK\_TR}$  are around 40 $\mu$ H and 20m $\Omega$  respectively. The additional inductor to complete the  $L_F$  value is  $L_{F\_EXT}=200\mu H$

### 4.3.1.2 Control system of the step-down PWM AC Chopper

Ideally, the steady-state expressions relating the input and output variables of the step-down PWM AC Chopper, Eq. 4-26 - Eq. 4-29, can be employed to control the RMS values of current and voltage at the load side acting directly on the converter duty cycle,  $\alpha$ . For reactive power compensation control, modifying  $\alpha$  ideally allows controlling the RMS output voltage of the converter  $V_{ACC}$  and consequently the amount of reactive current demanded by the load  $I_{LS}$  and supplied to the input  $I_{ST}$ , Figure 4-36. However, the low damping factor of the LC load and input filter may easily lead to unstable operation of the system if only an open loop controller is applied.



$$V_{ACC} = V_{CF} \cdot \alpha \tag{Eq. 4-26}$$

$$I_{LS} = \frac{V_{ACC}}{Z_{LCC}} = \frac{V_{CF}}{Z_{LCC}} \cdot \alpha \tag{Eq. 4-27}$$

$$I_{ST} = I_{LS} \cdot \alpha = \frac{V_{CF}}{Z_{LCC}} \cdot \alpha^2 \tag{Eq. 4-28}$$

$$\alpha = \frac{T_{ON}}{T_{SW}} \tag{Eq. 4-29}$$

Figure 4-36.- Control synoptic of the step-down PWM AC-Chopper and corresponding transfer equations

For instance, the use of an open loop controller (feed forward) may lead to input filter and/or load instabilities depending on how the control signal is varied as illustrated in Figure 4-37. On one hand, if the duty cycle  $\alpha$  is changed slowly keeping the load current response  $I_{LS}$  acceptable, excitation of the input filter at its resonant frequency may occurs. On the other hand, if the AC Chopper voltage changes suddenly (e.g. due to a sudden change on the duty cycle or a drop in the input voltage), the load resonant circuit may start interacting with the input filter resulting in oscillatory behaviour of the system. Consequently, a closed loop control is required to guarantee stable operation of the system as a reactive power compensator.

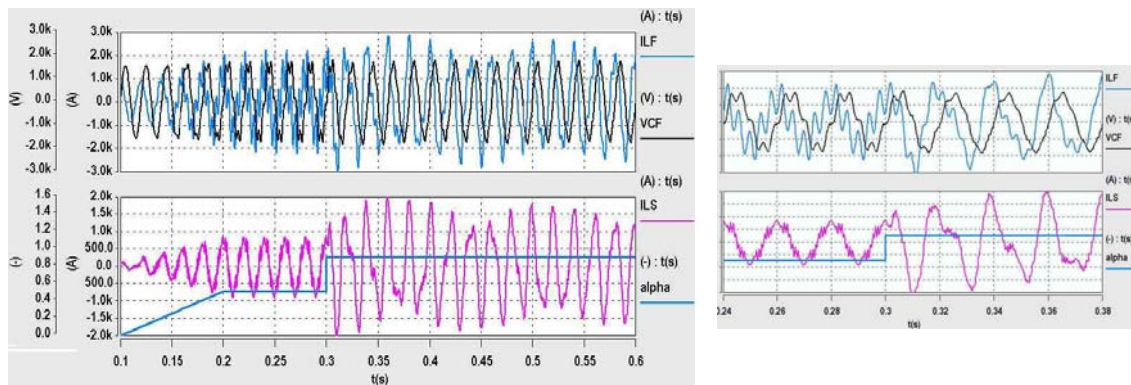


Figure 4-37.- Open loop response of the AC Chopper, (input filter excitation)

Although the aim of the system is to control the reactive power injected into the network  $I_{LF}$ , direct control of  $I_{ST}$  is barely effective because of its switched nature, Figure 4-15, and the non linear relationship with the control variable (Eq. 4-28,  $\alpha^2$  dependent). In contrast, control of the load current  $I_{LS}$  is a more straightforward solution due to the continuous evolution of the signal and the linear relationship with the input voltage and the control variable  $\alpha$ , Eq. 4-27. Control of the load current can provide stable steady-state operation to the converter damping the oscillatory nature of the LC input filter and load.

From a control point of view, the AC chopper can be considered as a non-linear system. Even the PWM AC Chopper step-down version where the switching period averaged ratio between the RMS input and output voltages is linear ( $\alpha$ ), Eq. 4-26, presents a non-linear behaviour due to the instantaneous sinusoidal waveform of the input voltage. Furthermore, the gains sign between the output voltage  $V_{ACC}$  and the output current  $I_{LS}$  changes with the switching configuration depending on the polarity of the input voltage. Two main approaches can be applied to control the system. The first approach consists of linearising the system and applying classical linear control techniques (PI regulator, etc). The second approach consists of applying non-linear controller techniques.

Although both approaches have been analysed, the use of non-linear control techniques (hysteresis controller) is here useless mainly due to the variable switching frequency inherent to this type of controller. Moreover, even if nearly constant switching frequencies can be achieved adapting the non linear controller (see Appendix 3), the impossibility to use interleaving operation of the modules and the excitation of the input filter due to the high bandwidth of the controller make the use of such a controller impractical. However, in other applications where the input filter damping ratio and the load behaviour is not so critical this kind of control systems could be used.

Consequently, the use of linear control systems is only considered. The following sections explain the required system linearisation and control actions required to provide stable operation of the system.

#### 4.3.1.2.1 Linear control system

The use of linear controllers for switching mode converters deals with linearised small-signal models of the converters obtained by applying averaging techniques [REC-96]. Nevertheless, in the PWM AC Chopper case the assumption of small-signal operation is not valid any longer since the input voltage is subjected to large AC fluctuations. Therefore, in order to use the small-signal model of the converter derived applying classical averaging techniques, compensation of the input voltage change is required.

The small-signal model and its corresponding characteristic transfer functions of the step-down PWM AC Chopper are given in Figure 4-38. The characteristics of the classical step-down DC/DC converter can be easily recognised showing the same control-to-output (Eq. 4-30) and line-to-output (Eq. 4-31) dynamic behaviour. The parasitics of the components (resistance of passive components, on-state voltage drop of semiconductors, etc.) are neglected assuming the second order system to be completely undamped, which corresponds with the worst case from a control point of view.

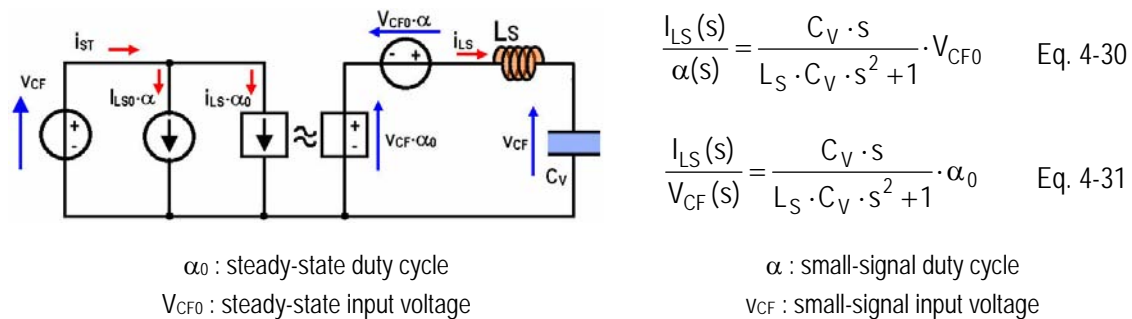


Figure 4-38.- PWM AC Chopper small-signal model and corresponding characteristic transfer functions

The main difference between the DC Chopper and the AC Chopper control to output model is the steady-state input voltage  $V_{CF0}$ . In the DC Chopper  $V_{CF0}$  is supposed to be constant, whereas in the AC Chopper this voltage is sinusoidal at the network frequency. Referring to Eq. 4-32, it is obvious that the changes in the input voltage cannot be considered as small, mainly when the switching frequency is relatively close to the network frequency ( $f=50\text{Hz}$ ,  $f_{sw}=1\text{kHz}$ ).

$$\frac{I_{LS}(s)}{\alpha(s)} = \frac{C_V \cdot s}{L_S \cdot C_V \cdot s^2 + 1} \cdot V_{CF0} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \quad \text{Eq. 4-32}$$

To compensate for the influence of the input voltage change on the transfer function, the intermediate use of the average relation between the AC Chopper voltage  $V_{ACC}$  and the input voltage  $V_{CF}$ , Eq. 4-26, can be used. Then the duty cycle can be derived by dividing the AC Chopper voltage signal with the instantaneous value of the input voltage. In such a way, the

small-signal transfer function between the output current and the AC chopper voltage defines the linear model of the converter, Eq. 4-33.

$$G(s) = \frac{I_{LS}(s)}{V_{ACC}(s)} = \frac{C_V \cdot s}{L_S \cdot C_V \cdot s^2 + 1} \quad \text{Eq. 4-33}$$

Taking into account the previous assumptions, a linear control structure based on feed-forward derived from the systems inverse model and a classical PI controller is selected. The feed-forward structure provides the steady-state control signal calculation (steady-state duty cycle  $\alpha_{ST}$ ), while the PI controller structure provides the dynamic correction (dynamic duty cycle  $\alpha_{DYN}$ ) required to compensate for the instantaneous current errors and the possible inverse model parameter changes ( $Z_{LC}=f(L_S, C_V, \omega)$ ).

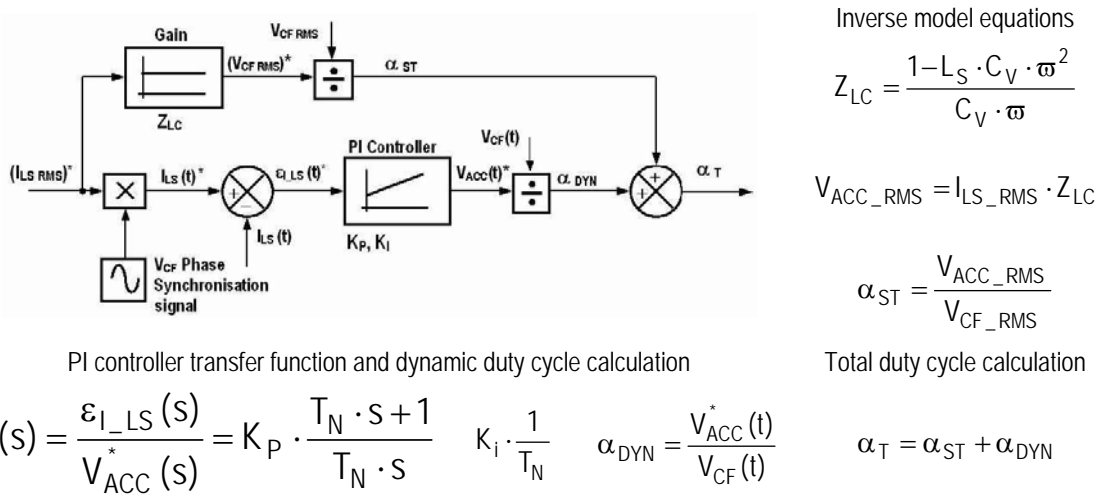


Figure 4-39.- Proposed control system structure (feed-forward and PI controller with input voltage compensation)

The static duty cycle reference  $\alpha_{ST}$  is calculated from the RMS reference value of the load current  $I_{LS}$ , the measured RMS value of the input voltage  $V_{CF}$  and the known impedance of the output load ( $L_S$  and  $C_V$  values). The instantaneous current reference is generated by multiplying the RMS reference value of  $I_{LS}$  with a sine wave of unity amplitude and  $90^\circ$  leading phase with respect to  $V_{CF}$ . This reference is compared with the measured output current  $I_{LS}(t)$ . The obtained error signal is fed to the PI controller, which outputs the AC Chopper voltage reference  $V_{ACC}^*$ . The dynamic duty cycle reference  $\alpha_{DYN}$  is then obtained by dividing the voltage reference  $V_{ACC}^*$  by the measured instantaneous input voltage measurement  $v_{CF}(t)$ . Finally, the total duty cycle value  $\alpha_T$  is obtained by adding the static and dynamic duty cycles ( $\alpha_T = \alpha_{ST} + \alpha_{DYN}$ ).

Tuning of the PI controller has been done taking into account the effect of the pure delay introduced by the PWM ( $e^{-s \cdot (T_{SW}/2)}$ ) to achieve a phase margin  $M\phi = 45^\circ$  at a cut-off frequency  $f_{BW} = f_{SW}/5 = 200\text{Hz}$ . The open loop transfer function  $TF_{OL}(s)$  of the system and the controller parameter expressions are given in Eq. 4-34 and Eq. 4-35 respectively.

$$TF_{OL}(s) = \frac{\epsilon_{I\_LS}}{V_{ACC}(s)} = K_P \cdot \frac{T_N \cdot s + 1}{T_N \cdot s} \cdot \frac{C_V \cdot s}{L_S \cdot C_V \cdot s^2 + 1} \cdot e^{-\frac{T_{SW} \cdot s}{2}} \quad \text{Eq. 4-34}$$



$$T_N = \frac{\tan\left(M_\varphi + \omega_{BW} \cdot \frac{T_{SW}}{2}\right)}{\omega_{BW}} \quad K_P = \frac{T_N \cdot \sqrt{\left(1 - L_S \cdot C_V \cdot \omega_{BW}^2\right)^2}}{\sqrt{1 + \left(T_N \cdot \omega_{BW}\right)^2}} \quad \text{Eq. 4-35}$$

The Bode plot of the open-loop transfer function clearly illustrates that the imposed tuning conditions are met, but reveals a lack of gain at low frequencies ( $K_P=0.92$ ,  $T_N=5\text{ms}$ ,  $K_I=200$ ). Nevertheless, the use of the additional feed-forward action compensates this lack of gain existing only in the low frequency range.

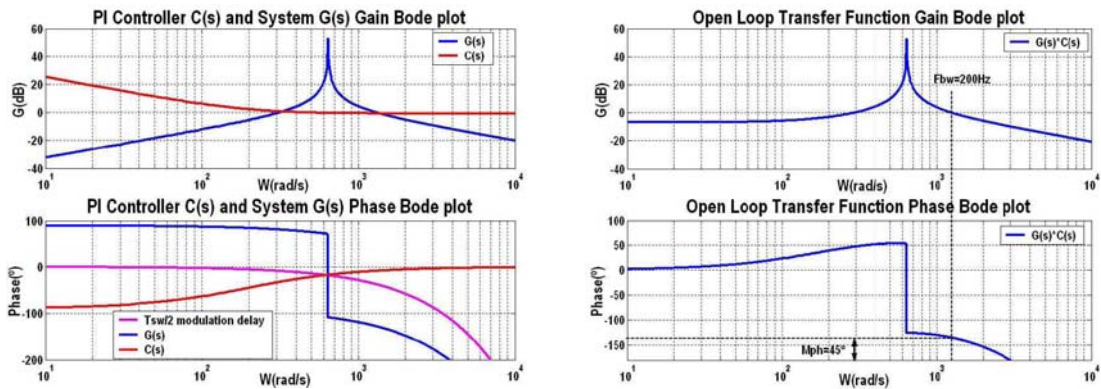


Figure 4-40.- Open-loop transfer function Bode plots ( $f_{BW}=200\text{Hz}$ ,  $M_\varphi=45^\circ$ ,  $K_P=0.92$ ,  $T_N=5\text{ms}$ ,  $K_I=200$ )

An additional non-linear function is added to the control system to assure stable operation under all operating conditions. Since the input voltage is sinusoidal, the division function providing the dynamic duty cycle  $\alpha_{DYN}$  results in an infinite value at the  $v_{CF}(t)$  zero voltage crossing. This disturbs the control system and excites the input filter as illustrated in Figure 4-41.

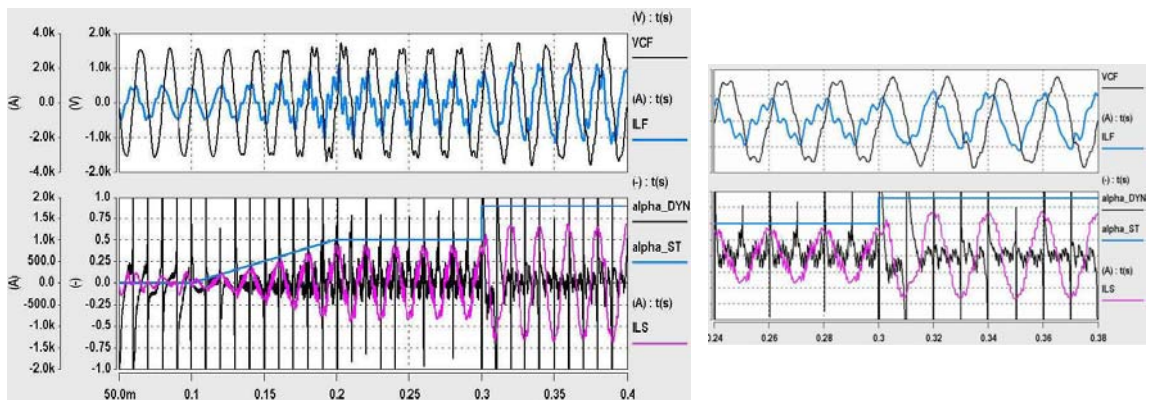


Figure 4-41.- Instable closed-loop response due to zero voltage division

To avoid the harmful effect of the PI controller at the zero crossing of the input voltage, an input voltage band ( $PI_{BLOCKING}$  level) is defined where only the static duty cycle is considered  $\alpha_{ST}$ . If the absolute value of the input voltage is higher than  $PI_{BLOCKING}$  the total duty cycle calculation considers both, the dynamic and the static duty cycle, Eq. 4-36. Otherwise, at the input voltage zero crossing, only the static duty cycle is considered, Eq. 4-37, (the PI controller keeps working, but its output signal is no further used). Therefore, at the zero crossing of the input voltage it can be said that the control system operates in open loop. Also, an anti-windup function to prevent the integral term divergence is foreseen in the PI controller structure to provide a faster dynamic response after the controller has been saturated.

$$|V_{CF}| > PI_{BL} \Rightarrow \alpha_T = \alpha_{ST} + \alpha_{DYN} \quad \text{Eq. 4-36}$$

$$|V_{CF}| < PI_{BL} \Rightarrow \alpha_T = \alpha_{ST} \quad \text{Eq. 4-37}$$

Simulation results for a single 1MVAR module with the proposed controller are shown in Figure 4-42. Stable operation of the output current control and the input filter is achieved, although the input filter current has representative low frequency harmonics. Furthermore, the dynamic response of the controller is demonstrated to be fast enough. Reaction in less than one network cycle is achieved even with a sudden change in the reference. Notice the evolution of the dynamic duty cycle  $\alpha_{DYN}$ , the current ripple is reflected on it only when the absolute value of the input voltage is above the defined voltage band  $PI_{BLOCKING}$ , at the zero crossing of the input voltage its value is zero. The value of  $PI_{BLOCKING}$  that assures stable operation of the controller is obtained empirically and its value is typically located around one third of the instantaneous maximum input voltage  $V_{CF\_MAX}$ .

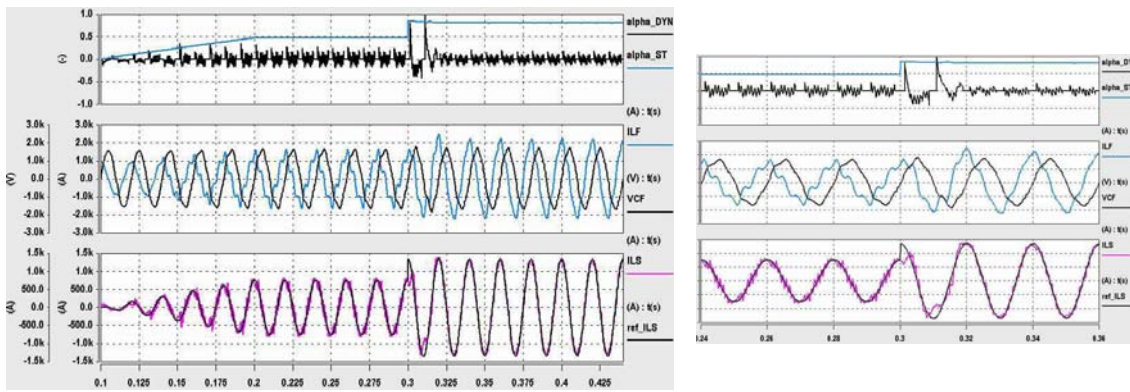


Figure 4-42.- Stable closed-loop response (avoiding zero voltage division)

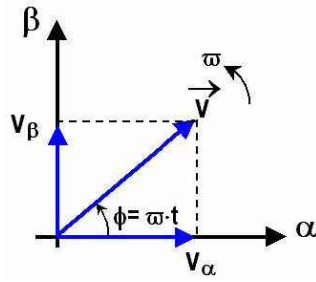
Obviously, the controller operation has been tested with the modulation adopted to assure safe switching operation of the semiconductors, which may play an important role in the stabilisation of the control system and the excitation of the input filter (see 4.3.1.3).

#### 4.3.1.2.2 Reference generation system

The generation of the reference output current  $I_{LS}^*$  must be synchronised with the input voltage  $V_{CF}$  to provide the  $90^\circ$  leading phase required to operate in reactive power compensation.

A classical solution to obtain the synchronisation with a sinusoidal waveform is the use of Phase-Locked Loop techniques (PLL), [HSI-96], a closed loop system that generates a signal with the same frequency and phase as the reference signal. The use of PLLs is widely applied for synchronisation in three-phase power systems where the application of the Clark and Park transformations allows controlling AC quantities by means of their DC representation on a D-Q reference frame. Extension of three-phase PLL techniques to single-phase systems can be performed by emulating a balanced three-phase system in which the single-phase voltage is associated with one of the frame axes of the virtual three-phase system representation, [MAG-01]. In general, the steady-state response of the PLL structures is very accurate and allows the correction of the system frequency change. The main drawbacks of PLLs are their limited dynamic response and their operation under distorted reference conditions, which may become unstable sometimes. Nevertheless, the use of advanced control techniques can be also applied to improve the dynamic performance of the PLL, [ALA-01].

Another possibility to obtain the synchronisation with a single-phase system is to make use of its representation by means of “instantaneous complex phasors” in a stationary  $\alpha$ - $\beta$  frame, Figure 4-43. Usually, this representation is implemented using digital or analog filters, [SAI-02], [BUR-01]. The accuracy, dynamic response and harmonics attenuation depend highly on the order of the filters employed, but generally they provide very stable operation. However, since the filters are tuned at a fixed frequency (the nominal single-phase system frequency), relevant phase errors may occur when relatively high frequency changes are common (higher when the order of the filter increases).



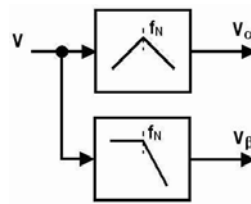
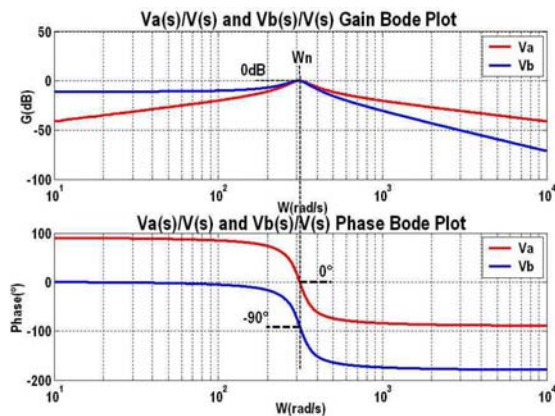
$$\vec{V} = \vec{V}_\alpha + \vec{V}_\beta = V \cdot e^{j\omega \cdot t} = V \cdot (\cos(\omega \cdot t) + j \cdot \sin(\omega \cdot t)) \quad \text{Eq. 4-38}$$

$$V_\alpha = V \cdot \cos(\omega \cdot t) \quad V_\beta = V \cdot \sin(\omega \cdot t) \quad \text{Eq. 4-39}$$

$$|V| = \sqrt{V_\alpha^2 + V_\beta^2} \quad \phi = \arctan \frac{V_\beta}{V_\alpha} \quad \text{Eq. 4-40}$$

Figure 4-43.- Complex phasor representation in the stationary  $\alpha$ - $\beta$  frame

The solution adopted here is to apply the “instantaneous complex phasors” technique using two second order filters (band-pass and low-pass filters) tuned at the network frequency. The second order transfer functions of the filters, Eq. 4-41 and Eq. 4-42, are selected to provide unity gain (0dB) at the considered frequency ( $\omega_N = 2 \cdot \pi \cdot f_N$ ) with the appropriated phase ( $0^\circ$  for  $V_\alpha$  and  $-90^\circ$  for  $V_\beta$ ), Figure 4-44. Once the characteristic frequency of the filters is fixed, the selection of the damping ratio  $\xi$  defines the dynamic characteristics of the  $V_\alpha$  and  $V_\beta$  generation system (see Appendix 2). On one hand, the attenuation of the input signal harmonics can be increased by lowering  $\xi$ , reducing also the frequency band around  $f_N$  with gain close to 0dB. On the other hand, the increase of  $\xi$  provides faster transient response times and less abrupt phase changes around  $f_N$ . A trade-off between all these considerations must be achieved depending on the network characteristics (i.e. harmonic content, frequency change) and the dynamic performance imposed by the application. The amplitude and phase synchronisation of the input signal can be derived by instantaneous computation of the magnitude  $|V|$  and angle  $\phi$  expressions, Eq. 4-40.



$$\frac{V_\alpha(s)}{V(s)} = \frac{2 \cdot \xi \cdot \omega_N \cdot s}{s^2 + 2 \cdot \xi \cdot \omega_N \cdot s + \omega_N^2} \quad \text{Eq. 4-41}$$

$$\frac{V_\beta(s)}{V(s)} = \frac{2 \cdot \xi \cdot \omega_N^2}{s^2 + 2 \cdot \xi \cdot \omega_N \cdot s + \omega_N^2} \quad \text{Eq. 4-42}$$

Figure 4-44.-  $V_\alpha$  and  $V_\beta$  generation by means of second order filters

In addition, the instantaneous complex vectors can be applied to the current values as well in order to compute in combination with the voltage vectors the instantaneous reactive and active powers of the system as defined by the Eq. 4-44 and Eq. 4-45 respectively.

$$S = P + j \cdot Q = \frac{1}{2} \cdot v \cdot i^* = \frac{1}{2} \cdot (v_\alpha + j \cdot v_\beta) \cdot (i_\alpha - j \cdot i_\beta) \quad \text{Eq. 4-43}$$

$$P = \frac{1}{2} \cdot (v_\alpha \cdot i_\alpha + v_\beta \cdot i_\beta) \quad \text{Eq. 4-44}$$

$$Q = \frac{1}{2} \cdot (v_\beta \cdot i_\alpha - v_\alpha \cdot i_\beta) \quad \text{Eq. 4-45}$$

For the reactive power compensation operation of the PWM AC Chopper STATCOM, the load current  $I_{LS}$  phase synchronisation with the PWM AC Chopper input voltage  $V_{CF}$  can be directly obtained from the instantaneous  $V_{CF\beta}$  complex vector. Only modification of the amplitude value of  $V_{CF\beta}$  by division with the  $V_{CF}$  maximum voltage and  $180^\circ$  phase shifted (-1 multiplication) are required to obtain the current waveform (unity amplitude)  $90^\circ$  leading with respect to the input voltage, Figure 4-45. The amplitude of the compensation current will be defined by the reactive power compensation manager system according to the network requirements.

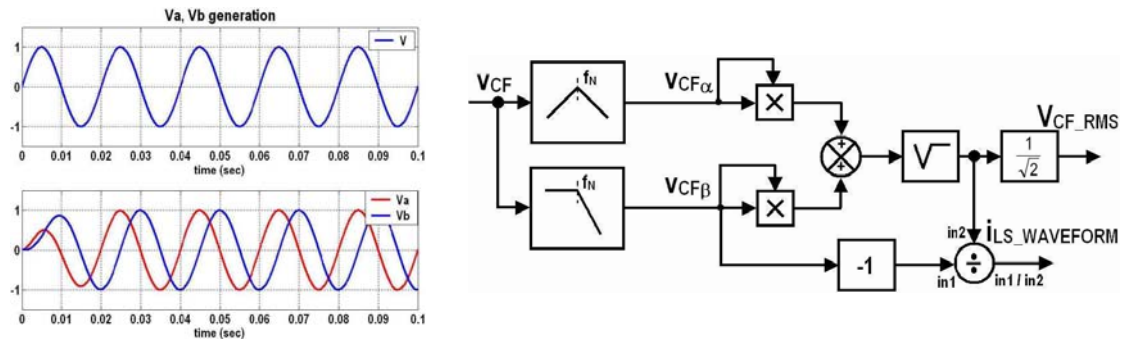


Figure 4-45.- STATCOM current reference synchronisation using  $V_{CF\alpha}$  -  $V_{CF\beta}$  complex phasors

### 4.3.1.3 AC Chopper PWM pattern generation

The modulator used by the AC Chopper has to consider the instantaneous working conditions of the input voltage  $V_{CF}$  in order to generate the correct switching sequence allowing the safe operation of the converter. The solution considering the input voltage polarity, Figure 4-15, to drive correctly the switches of the converter provides the best technical solution as stated in section 4.2.2. The main technical problem with the implementation of this solution is related to the correct detection of the input voltage polarity. Actually, the voltage sensor offset, accuracy and response time could lead to incorrect switching configurations causing a short-circuit of the input voltage. Furthermore, the dead time  $T_D$  for complementary safe commutation of the switching cell semiconductors and the minimum allowable pulses acceptable for the IGCTs ( $T_W = T_{ON(MIN)} = T_{OFF(MIN)}$  defined in the IGCT datasheets) have to be taken into account when generating the gating signals.

To avoid the uncertainty of the input voltage polarity around its zero crossing, either a freewheeling phase or an active phase can be permanently applied. Obviously, no switching events are generated then and the ideal PWM pattern is not applied, which may disturb the output and input signals. To keep the semiconductors in safe operation, it is essential to accommodate the gating signals at the input and output instants of this sequence considering the previous and the next states (carrier and duty cycle value) of the semiconductors. Special attention should be paid to respect the dead time  $T_D$  and minimum pulse time  $T_W$  generation. The modified PWM pattern strategy to guarantee the safe operation of the semiconductors is presented in Appendix 4. The application of a freewheeling phase during the zero crossing of the input voltage  $V_{CF}$  is given as a representative example of the proposed strategy.

### 4.3.2 Simulation of the PWM AC Chopper 3 MVAR STATCOM

The performance of the 3MVAR STATCOM based on PWM AC Choppers is analysed through simulation. The aim of this analysis is to investigate the behaviour of the complete system applying the solutions previously proposed in this chapter. The dimensioning of the system is verified and the controller and modulator operation and parameters are adjusted to obtain the best system performance with regard to the system control stability and input current harmonics generation. The parameters used in the simulations presented in this section are summarised in Table 4-4. The simulation is performed using ideal semiconductor switches and the IGCTs' clamp circuits are not considered.

Ideal transformer secondary voltage $V_{SEC}=1.060kV_{RMS}$ , ( $m_C=23.6$ , 3MVAR)						
Number of modules in parallel, $n=3$						
Input Filter	$L_F$ , input filter inductance	$C_F$ , input filter capacitance	$R_{LF}$ (transformer parasitic resistance)	-	-	-
	240 $\mu$ H	1.8mF	20m $\Omega$	-	-	-
1 MVAR Module output filter	$L_S$ , load inductance	$C_V$ , load capacitance	$R_{LS}$ (load inductor parasitic resistance)	-	-	-
	1mH	2.45mF	5m $\Omega$	-	-	-
PI Controller	$K_P$ , Proportional gain	$K_I$ , Integral term gain	Saturation limits ( $\alpha_{MAX}$ , $\alpha_{MIN}$ )	-	-	-
	1	500	0.95, 0.05	-	-	-
Modulator	$f_{sw}$ , switching frequency	$T_D$ , dead time	$T_W$ , minimum ON and OFF pulse	VALID_PI level	FW_level	$0^+$ and $0^-$ level
	1kHz	15 $\mu$ s	10 $\mu$ s	700V	100V	35V
Reference generation System	$f_N$ , 2 <sup>nd</sup> order filters frequency	$\xi$ , 2 <sup>nd</sup> order filters damping ratio	-	-	-	-
	50Hz	0.25	-	-	-	-

Table 4-4.- Simulation parameters for single-phase 3MVAR STATCOM based on PWM AC Choppers

Regarding the AC chopper modulation, the application of the free wheeling phase around the input voltage zero crossing is favoured since it performs better than the application of the active phase, mainly at low current reference values. Nevertheless, both solutions can be applied. During the freewheeling sequence, the load current on all the modules is freewheeling. Consequently, the input filter inductor current  $I_{LF}$  flows through the input capacitor filter  $C_F$  yielding a relatively high  $dV/dt$ . To optimise the performance of the system, the freewheeling phase length must be minimised. Considering practical measurement limitations, the polarity identification levels ( $0^+$  and  $0^-$ ) are selected to be ( $\pm$ ) 33.3V and the freewheeling limit is chosen to be three times larger,  $FW\_level=100V$ . The PI blocking level around the zero crossing is fixed at 700V.

From the controller point of view, it is important to disable the integration action of the PI controller during the stage around the input voltage zero crossing ( $\alpha_T=\alpha_{ST}$ ). This action is equivalent to the previously mentioned anti-windup function applied when the total duty cycle reaches its saturation limits ( $\alpha_{MAX}$ ,  $\alpha_{MIN}$ ), which provides better dynamic performance of the control system. Fine-tuning of the controller parameters has performed to provide better steady-state response in the whole current range, ( $K_P=1$ ,  $K_I=500$ ). This was necessary due to the non-linear nature of the system. Since no input voltage frequency changes are considered in the

simulation, the reference system generation parameters are selected mainly favouring dynamic and harmonic attenuation characteristics, ( $\xi=0.25$ ).

Once the control system parameters are selected the performance of the system can be analysed. Firstly, the reactive power compensation capability of the system has been verified. Figure 4-46 shows the AC Chopper input filter voltage  $V_{CF}$  and current  $I_{LF}$  waveforms for an output current reference (maximum value) changing from 0 to 760A and from 760 to 1.35kA with a time constant of 100ms (linear change). At the beginning of the simulation, the reactive power injected into the network  $Q_{SEC}=676\text{kVAR}$  is mainly imposed by the input filter. There is a slight difference between the reactive power injected into the network and the reactive power generated by the STATCOM ( $Q_C$ , input filter and AC Chopper modules) as a consequence of the reactive power reduction due to the input filter inductor. In this region, the AC Chopper operates in saturation at minimum duty cycle to track the zero current reference. Then, for  $I_{LS}=760\text{A}$ , the AC chopper operates with a duty cycle of around 0.5 injecting into the network a reactive power  $Q_{SEC}=1.45\text{MVAR}$  while the STATCOM generates  $Q_C=1.59\text{MVAR}$ . Finally, for a current reference of 1.35kA, the total power generated by the input filter and the AC Chopper is  $Q_C=3.61\text{MVAR}$  generating the desired network compensation of  $Q_{SEC}=3\text{MVAR}$ .

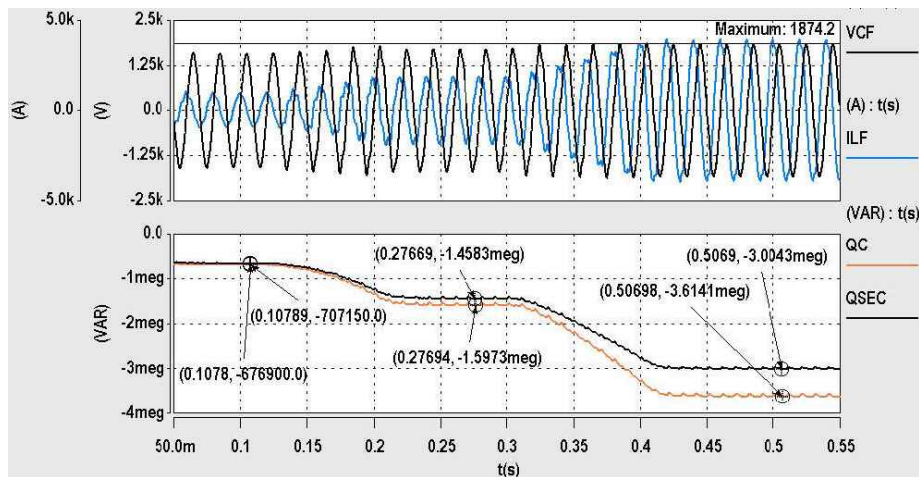


Figure 4-46.- Reactive power compensation response of the AC Chopper based 3MVAR STATCOM

Notice the stable response of the system during the changes in the reference, showing no significant current and voltage deviations. Notice also the increase on the voltage of the input filter capacitor related to the power compensation increase, showing maximum values slightly higher than the 1.8kV ( $1.27\text{kV}_{\text{RMS}}$ ) value, considered as the maximum blocking voltage for the semiconductor in the dimensioning procedure. This slight increase in voltage is not harmful for the semiconductors, and it is generated mainly by the distortion of the input voltage due to the AC Chopper operation as shown in Figure 4-47. The RMS voltage values correspond well with the expected value ( $1.273\text{kV}_{\text{RMS}}$ ).

Note also the increased change in  $dV/dt$  around the zero voltage of the input capacitor caused by the application of the freewheeling sequence. The three 1MVAR modules interleaved output currents ( $I_{LS\_A}$ ,  $I_{LS\_B}$ ,  $I_{LS\_C}$ ) are slightly distorted around the zero crossings of the input voltage, which is more accentuated after the output PI omission phase has ended in the generation of the total duty cycle ( $\alpha_T=\alpha_{ST}+\alpha_{DYN}$ ), disturbing slightly the input filter current  $I_{LF}$ . However, even if some low-frequency harmonics are generated at the input side, the load control behaves correctly. The steady-state duty cycle of the AC chopper at this operating condition is about  $\alpha_{ST}=0.78$ , still assuring some reactive power generation margin in case of lower network voltages.

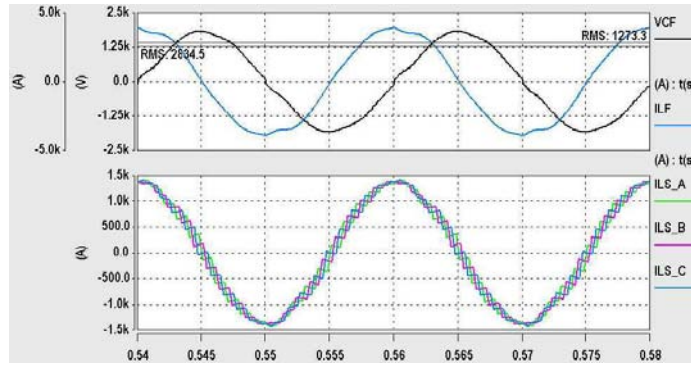


Figure 4-47.- STATCOM input filter current  $I_{LF}$  and voltage  $V_{CF}$  (top) and AC chopper 1MVAR modules' output current ( $I_{LS\_A}$ ,  $I_{LS\_B}$ ,  $I_{LS\_C}$ ) waveforms (bottom),  $Q_{SEC}=3MVAR$

The same comments apply also for the operation of the STATCOM at steady-state duty cycle around  $\alpha_{ST}=0.5$  ( $Q_{SEC}=1.45MVAR$ ). Nevertheless, a higher input current distortion can be identified, mainly as a consequence of the influence of the higher output inductors' current ripple, which has been found to be a maximum of 584A instead of the ideally estimated 375A. The influence of the control loop is responsible for this significant difference (190A), which has to be considered when selecting the component to be used.

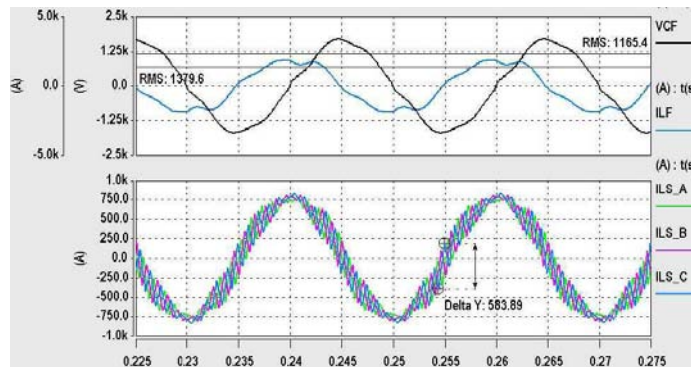


Figure 4-48.- STATCOM input filter current  $I_{LF}$  and voltage  $V_{CF}$  and AC chopper 1MVAR modules' output current ( $I_{LS\_A}$ ,  $I_{LS\_B}$ ,  $I_{LS\_C}$ ) waveforms,  $Q_{SEC}=1.45MVAR$

Regarding the harmonic content of the input filter current, operation at  $Q_{SEC}=3MVAR$  shows a total harmonic distortion  $THD=5.2\%$ , with the 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonics as the most significant low-frequency harmonics, Figure 4-49.

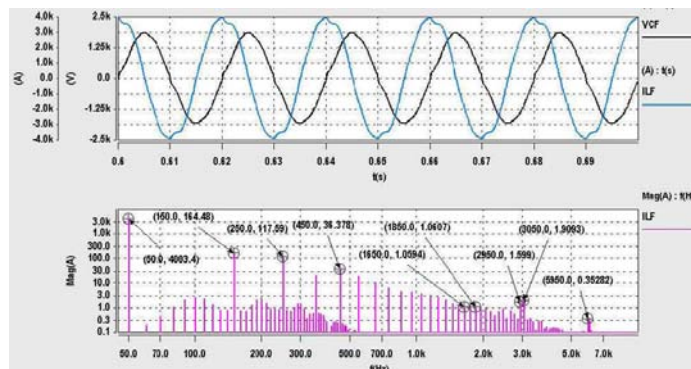


Figure 4-49.- STATCOM input filter current  $I_{LF}$  spectrum,  $Q_{SEC}=3MVAR$

From a high-frequency point of view, Figure 4-50, in the range between 1.6kHz and 2.7kHz (SNCF signalisation forbidden band), the maximum values of the current harmonics exceed slightly 1A. Considering the transformer turns ratio ( $m_c=23.6$ ), the RMS value of the current in the network does not exceed 32mA.

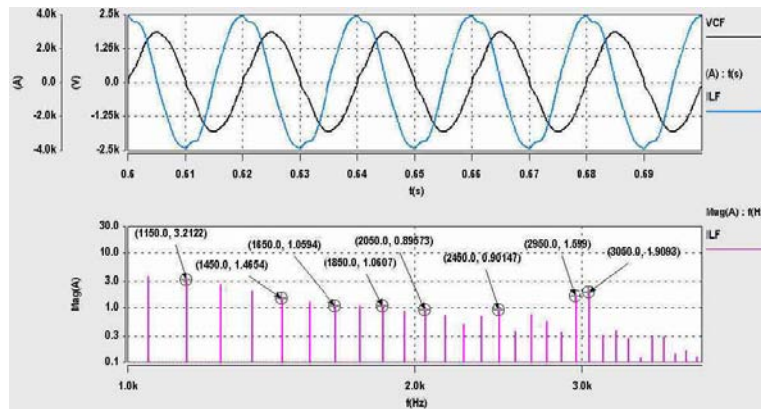


Figure 4-50.- STATCOM input filter current  $I_{LF}$  high-frequency spectrum detail,  $Q_{SEC}=3MVAR$

Although the SNCF current harmonic limits are slightly exceeded, Table 4-5, the use of small trap (EMI) filters in this frequency range can provide the additional attenuation (10dB) required to comply with the standards.

Frequency	$I_{LF\_MAX}$	$I_{LF\_RMS}$	$I_{LF\_RMS} / m_c$ (primary side harmonics)	SNCF harmonic limits
1550 Hz	1.25A	884 mA	37 mA	-
1650 Hz	1.06A	750 mA	32 mA	10mA
1750 Hz	1.06A	750 mA	32 mA	10mA
1850 Hz	1.06A	750 mA	32 mA	1A
1950 Hz	840 mA	594 mA	25 mA	10mA
2050 Hz	900 mA	636 mA	27 mA	10mA
2150 Hz	720 mA	509 mA	22 mA	1A
2250 Hz	480 mA	339 mA	14 mA	10mA
2350 Hz	700 mA	495 mA	21 mA	10mA
2450 Hz	900 mA	636 mA	27 mA	1A
2550 Hz	360 mA	255 mA	11 mA	10mA
2650 Hz	740 mA	523 mA	22 mA	10mA
2750 Hz	550 mA	389 mA	16 mA	-
2850 Hz	350 mA	247 mA	10 mA	-
2950 Hz	1.6A	1.131 A	48 mA	-
3050 Hz	1.9A	1.344 A	57 mA	-

Table 4-5.- STATCOM input current harmonics for  $Q_{SEC}=3MVAR$

When the STATCOM operates at  $Q_{SEC}=1.45MVAR$ , the current harmonic distortion (Figure 4-51) is increased to THD=13.3%, which may call for additional passive filters to comply with the network standards. Also, the increase of the input filter capacitor  $C_F$  could lead to the reduction of the input current harmonics providing a more stable operation of the AC chopper input voltage at



the expense of a lower adjustable reactive power compensation range. Otherwise, increasing the load output inductor  $L_s$  can be considered to reduce the current ripple and minimise its influence on the control loop, which is translated in larger size and consequently higher cost of the inductor. More advanced control techniques may be also investigated to obtain a better performance of the system (input current control, D-Q frame control, etc.), demanding for more accurate AC chopper models taking into account the non-linear behaviour of the converter.

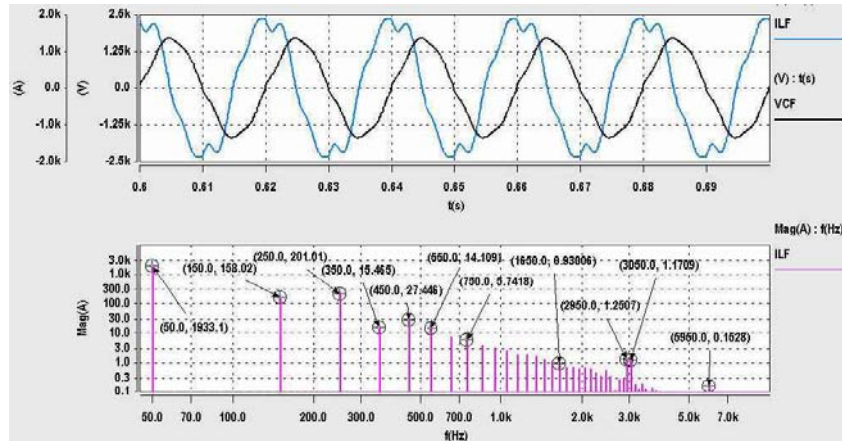


Figure 4-51.- STATCOM input filter current  $I_{LF}$  spectrum,  $Q_{SEC}=1.45\text{MVAR}$

In the high-frequency range, the harmonic content is even lower than for the operation at  $Q_{SEC}=3\text{MVAR}$ , Figure 4-52, which lead to the considerations previously mentioned.

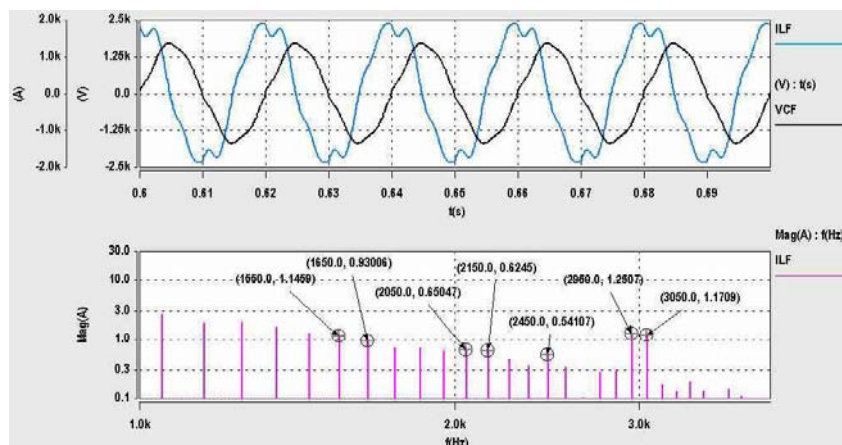


Figure 4-52.- STATCOM input filter current  $I_{LF}$  high-frequency spectrum detail,  $Q_{SEC}=1.45\text{MVAR}$

Another important phenomenon that has been verified through simulation is the behaviour of the STATCOM when the network voltage is significantly distorted. Figure 4-53 shows the reactive power compensation response provided by the system when a 3<sup>rd</sup> harmonic is injected into the network voltage (10% of the 50Hz nominal voltage,  $106V_{RMS}$ ). The current reference is kept the same as in the simulation example of Figure 4-46. Notice that the control system response is stable, but that the input voltage and filter current are highly distorted, presenting an input current distortion THD=19.8% and, what could be more harmful for the semiconductors, a peak voltage of 1.92kV. Also, the reactive power compensated to the network has been reduced significantly compared to the operation under non-distorted network conditions ( $Q_{SEC}=2.75\text{MVAR}$  instead of  $Q_{SEC}=3\text{MVAR}$ ).

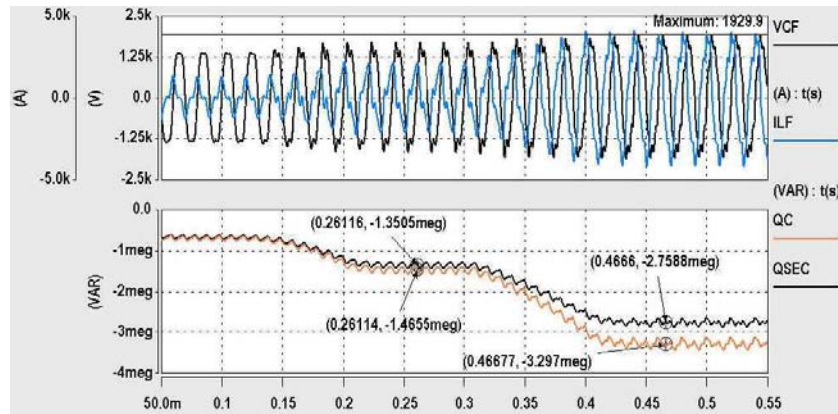


Figure 4-53.- Reactive power compensation response when a 3<sup>rd</sup> harmonic is injected in the network voltage (10% of the network nominal voltage)

This effect can be explained by the change of the load behaviour (from capacitive to inductive) when it is excited with frequencies above its resonant frequency,  $f_R=101\text{Hz}$  in this case. In fact, the current reference generation system rejects the 3<sup>rd</sup> harmonic content of the input voltage and provides an almost ideal 50Hz sinusoidal reference, REF\_ILS, Figure 4-54. The controller tries to track the reference, but the AC Chopper input voltage harmonic distortion which is not compensated by the controller introduces the corresponding current harmonics in the load current. Obviously, the harmonics above  $f_R$  are reflected at the input of the AC chopper, distorting the input current  $I_{LF}$  and acting as an inductive load, which decreases the total reactive power compensation of the system.

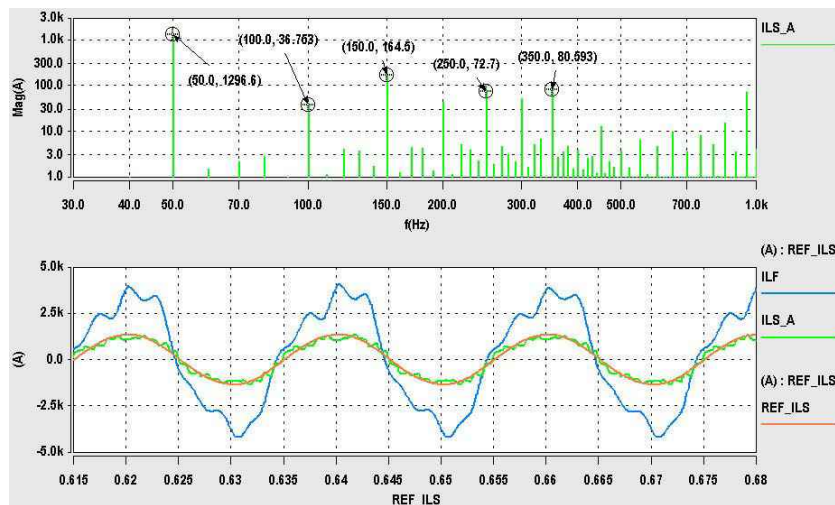


Figure 4-54.- Reactive power compensation response when a 3<sup>rd</sup> harmonic is injected in the network voltage (10% of the network nominal voltage)

To circumvent these effects, modification of the load current reference can be applied according to the input voltage harmonics in order to maintain the power compensation level and avoid the AC chopper input voltage to be highly distorted. To achieve this reference modification, identification of the harmonics and the load impedance at each harmonic frequency is required. Obviously, the bandwidth of the controller will limit the harmonics that can be taken into account.

The strategy here proposed to avoid the influence of the 3<sup>rd</sup> harmonic on the input voltage of the AC Choppers and to obtain the required compensation  $Q_{SEC}$  consists of the generation of a 3<sup>rd</sup> harmonic load current corresponding with the amplitude of the 3<sup>rd</sup> harmonic network voltage. That

means that the AC Chopper is controlled to operate as a variable inductor at the 3<sup>rd</sup> harmonic frequency depending on the value of reactive power  $Q_{SEC}$  to be compensated ( $\alpha_{ST}$ ). This operation implies that the STATCOM is going to inject a 3<sup>rd</sup> harmonic current to the network, which can be affordable depending on the amplitude of the voltage harmonics existing in the network and the impedance of the load.

Figure 4-55 shows the control structure that allows modifying the current load current reference  $I_{LS}(t)$  to take into account the occurrence of the input voltage 3<sup>rd</sup> harmonic. The amplitude and phase of the 3<sup>rd</sup> harmonic of the AC Chopper voltage  $V_{CF}$  is calculated applying the complex vector decomposition. The amplitude of the 3<sup>rd</sup> harmonic current reference ( $I_{LS\_RMS}$ )<sub>3·f<sub>N</sub></sub> is obtained from the steady-state duty cycle  $\alpha_{ST}$  defined to provide the desired reactive power compensation  $Q_{SEC}$  (Eq. 4-46), the 3<sup>rd</sup> harmonic voltage RMS value ( $V_{CF\_RMS}$ )<sub>3·f<sub>N</sub></sub> and the load impedance at the harmonic frequency ( $Z_{LC}$ )<sub>3·f<sub>N</sub></sub>, Eq. 4-47. The phase of the 3<sup>rd</sup> harmonic current reference is derived from the  $V_{CF\alpha\_3}$  signal, providing 90° of phase lag with respect to the 3<sup>rd</sup> harmonic voltage (inductive behaviour of the load at the 3<sup>rd</sup> harmonic frequency).

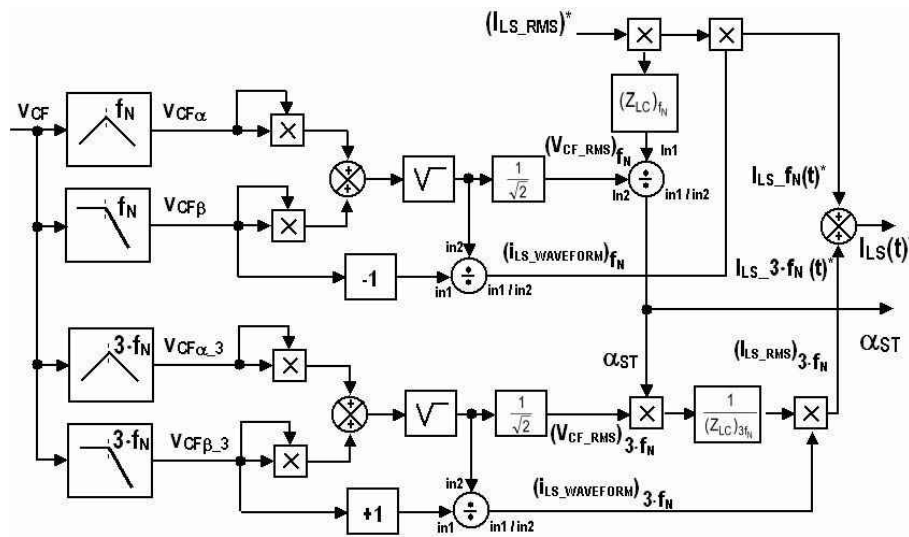


Figure 4-55.- Control structure to compensate for the influence of the 3<sup>rd</sup> harmonic voltage in the network voltage on the AC Chopper operation

$$\alpha_{ST} = \frac{(I_{LS\_RMS})^* \cdot (Z_{LC})_{fN}}{(V_{CF\_RMS})_{fN}} \quad \text{Eq. 4-46}$$

$$(I_{LS\_RMS})_{3 \cdot fN} = \frac{(V_{CF\_RMS})_{3 \cdot fN} \cdot \alpha_{ST}}{(Z_{LC})_{3 \cdot fN}} \quad \text{Eq. 4-47}$$

Figure 4-56 shows the reactive power compensation response when introducing 3<sup>rd</sup> harmonic load current reference. This correction allows to compensate for the desired reactive power  $Q_{SEC}=3\text{MVAR}$  while maintaining the current and input filter waveforms with reduced distortion. In this case, the maximum voltage applied to the semiconductors is 1.78kV, which is lower than in the case without input voltage 3<sup>rd</sup> harmonic (1.87kV). Notice at the beginning of the simulation the input filter current showing the 3<sup>rd</sup> harmonic characteristic current waveform of a passive load supplied by a 3<sup>rd</sup> harmonic voltage (the AC chopper is operating with zero current reference).

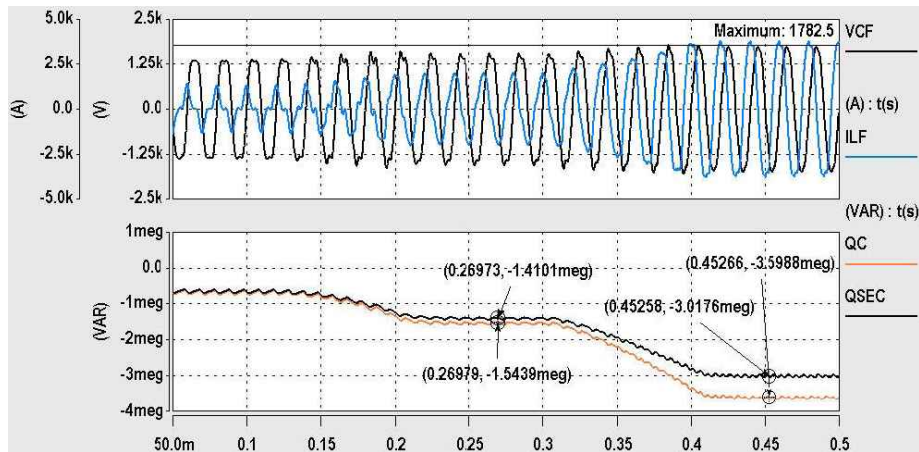


Figure 4-56.- Reactive power compensation response with correction of the 3<sup>rd</sup> harmonic network voltage influence (10% of the network nominal voltage)

The reference generation signals are shown in Figure 4-57, where the 3<sup>rd</sup> harmonic of the input voltage  $V_{SEC}$  can be noticed. To provide  $Q_{SEC}=3\text{MVAR}$ , the steady-state duty cycle is found to be around  $\alpha_{ST}=0.75$ , which generates a 3<sup>rd</sup> harmonic maximum current reference around 185A. The controller tracks accurately the current reference, providing the non-distorted operation of the input filter, which yields similar waveforms as the operation without network voltage 3<sup>rd</sup> harmonic.

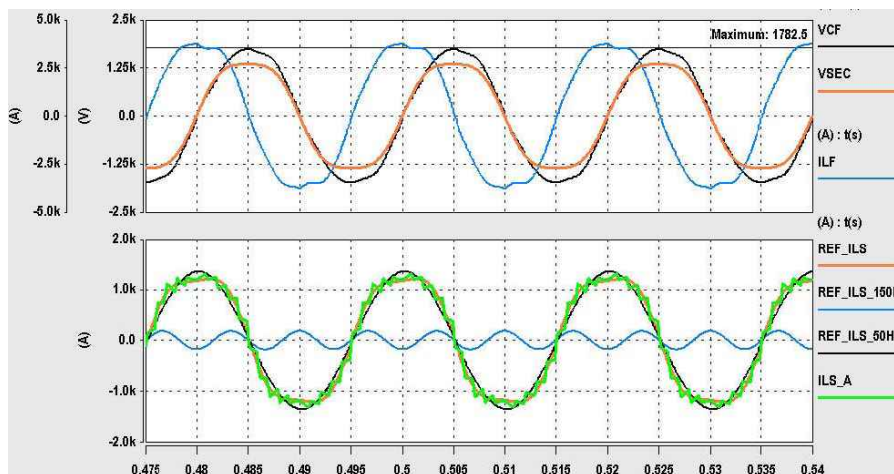


Figure 4-57.- Load current control reference generation (1<sup>st</sup> and 3<sup>rd</sup> harmonic components)

Obviously, besides the reactive power compensation  $Q_{SEC}$ , the STATCOM is seen by the network as a variable inductor at the 3<sup>rd</sup> harmonic, which increases the total harmonic distortion of the system to  $\text{THD}=8.8\%$ . Figure 4-58 shows the input harmonic spectrum of the input filter current  $I_{LF}$  under this operating condition. Notice the 3<sup>rd</sup> harmonic amplitude increase with respect to the STATCOM operation without network voltage 3<sup>rd</sup> harmonic (332A instead of 164A, Figure 4-49). This difference (168A) is the main reason why the THD is increased. To minimise the amount of the 3<sup>rd</sup> harmonic current injected by the STATCOM, the load resonant frequency  $f_R$  could be reduced to increase the load impedance at the harmonic frequency (increase of the load inductor  $L_s$  value). However, the reduction of this frequency is restricted by network frequency. Also increasing the input filter resonant frequency  $f_{RF}$  should be considered to minimise its contribution to the total 3<sup>rd</sup> harmonic current. However, this will increase the magnitude of the high frequency harmonics injected into the network.

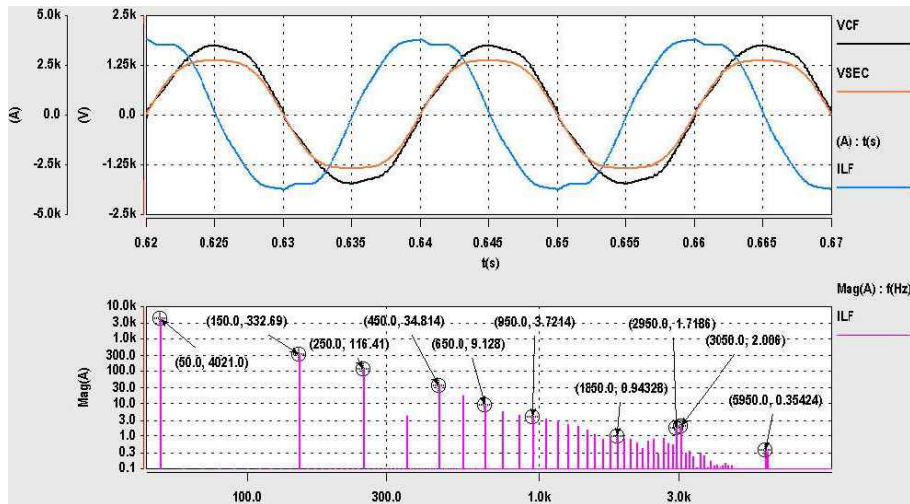


Figure 4-58.- STATCOM input filter current  $I_{LF}$  spectrum with 3<sup>rd</sup> harmonic injection,  $Q_{SEC}=3\text{MVAR}$

The high-frequency range of the input current spectrum is similar as compared to the one obtained without 3<sup>rd</sup> harmonic on the network voltage.

## 4.4 Conclusions

The STATCOM function is generally achieved using Voltage Source Inverters, which provides both possibilities, reactive power compensation (capacitive operation) and generation (inductive operation). However, other converter topologies can be also applied to provide this reactive power compensation. Among them and under certain conditions (only capacitive operation), the AC Chopper can provide higher reactive power compensation capabilities at given semiconductor ratings with lower semiconductor power losses and smaller compensation capacitors.

In this chapter, after a brief overview of the PWM AC Chopper topologies, the analysis of a 3MVAR single-phase STATCOM for the 25kV/50Hz SNCF network based on step-down PWM AC Choppers using 3.3kV IGCTS is presented. The proposed dimensioning procedures and criteria for the main passive components have been presented considering the specific conditions imposed by the SNCF network, mainly high frequency current harmonics limitation, and the IGCTs operating conditions. Special attention has been paid to the control system, providing the required solutions to obtain a stable operation of the system. Also, specific switching patterns complementing the PWM have been proposed to provide safe switching operation of the semiconductors around the zero crossing of the AC Chopper input voltage, where the uncertainties of voltage measurement could lead to the failure of the converter.

Finally, the proposed 3MVAR STATCOM structure is evaluated through simulation, demonstrating the validity of the design procedure previously presented and showing the performance of the system. The high-frequency current harmonic characteristic of the converter shows that the use of small trap or EMI filters will allow fulfilling the restrictions imposed by SNCF standards to protect its train signalisation system. The main drawback of the proposed solution lays in the low frequency harmonics generated at low power compensation level and the operation of the system under distorted network voltage. However, modification of the dimensioning criteria of the input filter and/or the load components and modification of the control system could lead to acceptable low frequency harmonic current ratios.

# Chapter 5

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## Practical Evaluation of Single-phase STATCOM based on Step-Down PWM AC Choppers

### 5.1 Introduction

The design and control concepts developed in Chapter 4 regarding the operation of the step-down PWM AC Choppers as single-phase STATCOM are practically evaluated and presented in this chapter. Furthermore, the operation sequences for safe start-up and shutdown of the system under normal or failure operation mode are introduced.

Two set-ups are built to demonstrate the feasibility of the proposed solutions. The first low voltage/power prototype (5kVAR) is based on the use of low voltage IGBTs operating at low switching frequency ( $f_{sw}=1\text{kHz}$ ). This small prototype is mainly developed to validate the control system operation (i.e. closed control loop, start-up and shutdown sequences, etc.) and the retained switching pattern providing safe switching operation to the semiconductors at the zero crossing of the input voltage. Once the control system is validated, a 100kVAR single-phase STATCOM based on step-down PWM AC Choppers with standard 4.5kV IGCTs is practically tested in reactive power generation (inductive) mode, validating the application of the developed concepts with the use of IGCTs. The maximum tested power is limited to 30kVAR due to the power limitation of the network connection point.

### 5.2 Start-up and Shutdown Sequences of the PWM AC Chopper

The synoptic representation of a single-phase PWM AC Chopper for reactive power compensation (capacitive operation) is shown in Figure 5-1. The network fuses and contactor/circuit breaker are used to supply and protect the system. A power transformer adapts the network voltage to the operating voltage of the semiconductors. The secondary winding of the transformer is protected by fuses. Then, an input filter ( $L_F-C_F$ ) is used to filter the switched current generated by the PWM AC Chopper. The PWM AC Chopper load consists of an LC filter ( $L_S-C_V$ ) whose cut-off frequency is selected to be higher than the network frequency. That means that the load has a capacitive behaviour at the network frequency. The Control System governs the semiconductors to control the reactive power injected into the network (capacitive reactive power) by controlling the load current ( $i_{LS}$ ) to impose a sinusoidal waveform with a  $90^\circ$  leading phase with respect to the input voltage ( $v_{NET}$ ). The input voltage has to be measured to generate the current reference for the output current control loop (phase and amplitude), and also to generate

the gate signals for the semiconductors according to the retained modulation strategy (see section 4.3.1.3).

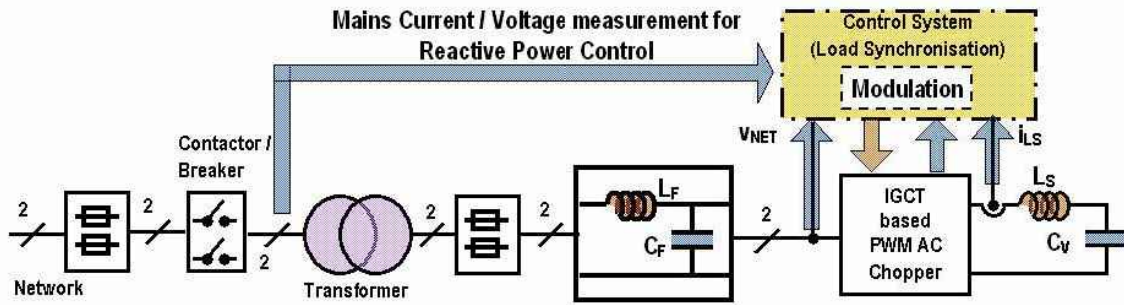


Figure 5-1.- Synoptic representation of a single-phase STATCOM based on PWM AC Choppers

Besides the special switching pattern generation of the PWM AC Chopper at the zero crossing of the input voltage and the reactive power compensation control, the control system must generate the suitable start-up and shutdown sequences of the converter to provide stable and safe working conditions for the components of the system. The particular working conditions of the AC Chopper during these sequences and the corresponding solutions proposed to obtain a proper operation of the system are presented in the following sections.

## 5.2.1 Network Connection

Considering all the switches of the AC Chopper to be blocked, when the contactor/breaker is switched on, a transient operation is started. The application of the network voltage excites the input filter of the PWM AC Chopper, which caused the input voltage ( $V_{NET}$ ) to be disturbed. In fact, the input voltage will have a fundamental component at the network frequency and a transient component at the cut-off frequency of the LC input filter. To allow the proper operation of the PWM AC Chopper, the switching sequences should not start before this transient operation is finished. The transient time of this operation depends on the input filter damped ratio, which depends mainly on the parasitic resistors of the transformer, the input filter inductor, and the capacitor. If the damping factor is too low, an extra damping resistor  $R_{DAMP}$  can be added when the network voltage is applied, which increases the damping ratio of the filter and limits the input filter capacitor charging current. Obviously, once steady state is reached, the extra damping resistor must be short-circuited by means of contactors or static switches to limit the power losses and the voltage drop on the component, Figure 5-2.

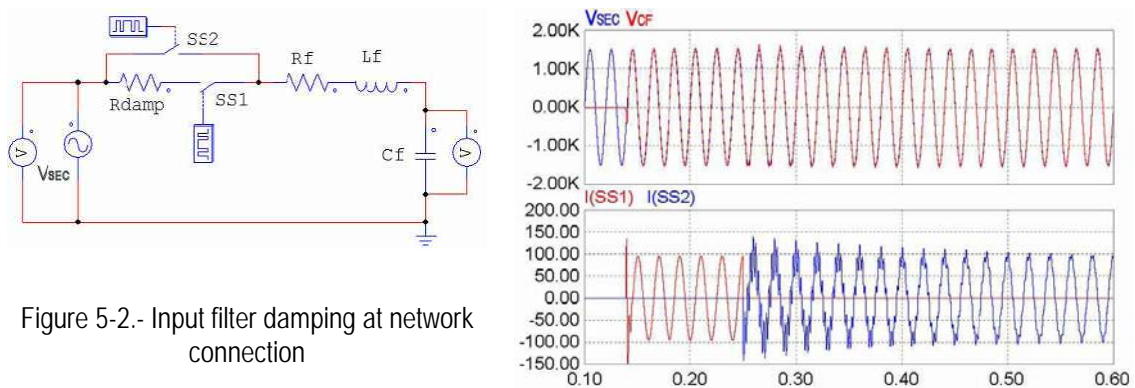


Figure 5-2.- Input filter damping at network connection

Short-circuiting the extra damping resistor will generate an additional transient operation due to the difference between the network voltage and the voltage of the input filter capacitor. However,

this transient operation is less important than the one generated if the network is directly connected to the filter due to the slight difference between the network and filter voltages.

Another available solution is the use of damped input filters as illustrated in Figure 5-3. The damping ratio is increased by adding additional resistors and capacitors or inductors arranged either in parallel or in series to minimise the power losses of the resistor in steady state operation. The filter attenuation and the cut-off frequency are slightly modified, whereas the quality factor of the filter is reduced; that is, the power losses in the whole input filter are increased. The power loss on the resistor is the main drawback of these damping solutions, which can be increased by the switched current demanded by the converter.

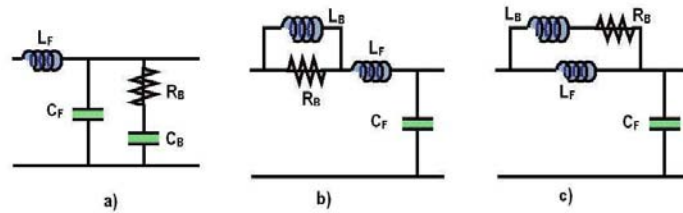


Figure 5-3.- Damping solutions for LC filters. a)  $R_B$ - $C_B$  parallel damping. b)  $R_B$ - $L_B$  series damping. c)  $R_B$ - $L_B$  parallel damping

## 5.2.2 Switching Operation Start-up synchronisation

Once the input filter voltage reaches steady state, the switching operation can start. However, the starting time for the switching operation must be selected to minimise the stress over the semiconductors of the PWM AC Chopper switching cells and their clamping and/or decoupling passive components.

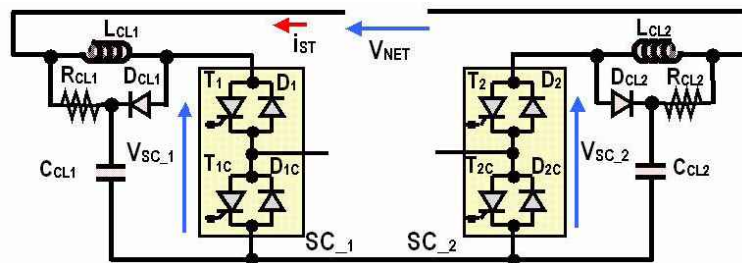


Figure 5-4.- Power stage of the IGCT based single-phase step-down PWM AC Chopper

The circuit in Figure 5-4 presents the main elements of the switching cells of an IGCT based single-phase step-down PWM AC Chopper (semiconductors of the IGCT switching cells and clamp circuit components). During the blocking state of the PWM AC Chopper, the semiconductors of both switching cells remain blocked. In this condition, the clamping capacitors  $C_{CL1}$  and  $C_{CL2}$  are connected to the input as a voltage divider through the clamp resistors  $R_{CL1}$  and  $R_{CL2}$  (series configuration), so the input voltage is equally shared in both capacitors (considering  $C_{CL1}=C_{CL2}$ ). Consequently, the voltages across the switching cells ( $V_{SC,1}$  and  $V_{SC,2}$ ) have the same waveform as the input voltage  $V_{NET}$  but they present a DC component equal to half the maximum value of the input voltage, Figure 5-5.

When the switching cells are going to start the switching operation, one of them must operate in short circuit according to the input voltage sign ( $V_{NET}>0$ ,  $T_2$  and  $T_{2C}$  switched on permanently,  $V_{NET}<0$ ,  $T_1$  and  $T_{1C}$  switched on permanently). When the switching cell is short circuited, the energy stored in the corresponding clamp capacitor  $C_{CL}$  is roughly discharged over the



semiconductors of the switching cell, only limited by the clamp circuit components. To minimise the stress over the components (current and voltage spikes, capacitor short-circuit, etc.), the first switching event should be synchronised to take place when the voltage across the switching cell that has to be short-circuited is close to zero. This time corresponds with the input voltage maximum value point (absolute value), Figure 5-6.

The starting-up synchronisation signal can be generated from the  $V_{NET}$  polarity detection system employed in the generation of the PWM AC Chopper switching pattern and a time delay. Simply a 5ms delay after the change of the  $V_{NET}$  polarity can provide a proper starting point for the start-up switching operation. Obviously, the start sequence must be subordinated to the start-up order coming from the general controller.

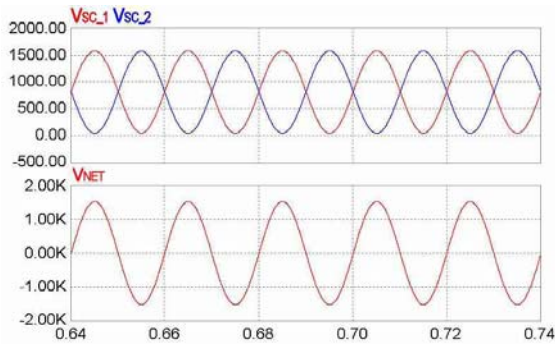


Figure 5-5.- Switching cell voltages equally shared in the blocking state of the PWM AC Chopper

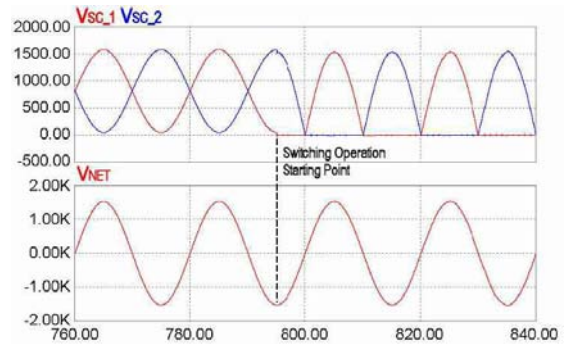


Figure 5-6.- Switching operation start time synchronised to be at switching cell zero voltage

### 5.2.3 Shutdown sequence

When the converter has to be stopped, it is recommended to progressively reduce the output current loop reference signal to zero. However, if the system has to be stopped urgently (emergency / protection stop), a defined sequence must be generated to discharge the energy stored in the output load ( $L_s$ ,  $C_v$ ). In such a case, blocking all the IGBTs will charge the clamp capacitors  $C_{LC}$  through the freewheeling diodes until the output inductor current decreases to zero and the freewheeling diodes are reverse blocked. This operation leads to the application of dangerous voltage to the blocked switching cells, which could cause the destruction of the semiconductors and even the passive components. In fact, this charging voltage is added to the input voltage as depicted in Figure 5-7, so the voltage seen by the switching cell could become more than two times bigger than the maximal voltage applied in switching operation.

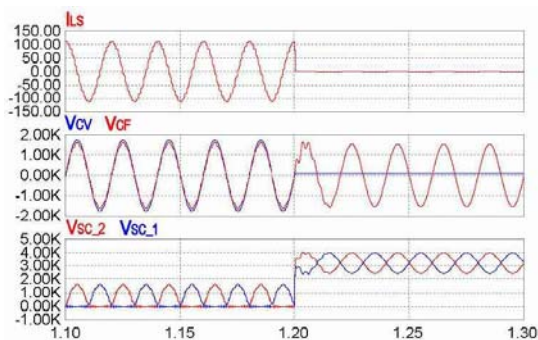


Figure 5-7.- All semiconductors blocking sequence at maximum load current

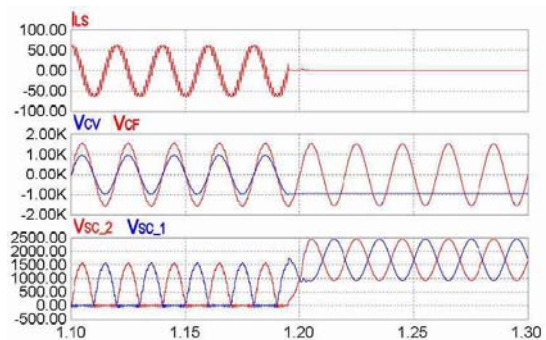


Figure 5-8.- All semiconductors blocking sequence around zero load current

A possible solution to avoid this problem is to block all the semiconductors when the output current is zero. However, the exact detection of the load current zero crossing is not practically accurate enough, mainly due to the high switching current ripple added the current fundamental term. Furthermore, the load capacitor  $C_V$  can remain charged even if its current is zero, Figure 5-8.

The proposed solution consists of providing a freewheeling path to discharge the energy stored in the load. The energy is discharged over the parasitic elements of the freewheeling path (parasitic resistance of the load components and on-state voltage of the semiconductors) in a softly manner. In fact, a damped resonance at the load circuit ( $L_S$ ,  $C_V$ ) cut-off frequency  $f_R$  is held, Figure 5-9. The energy discharging time will be defined depending on the damping ratio of the circuit (load parasitic resistors, and losses on the semiconductors). This sequence has to be launched any time the system is going to be stopped, (emergency or normal stop sequence), to insure that the energy stored on the load (capacitor and inductor) is really dissipated. Once the load energy is discharged, the blocking signal for all the semiconductors can be launched.

The freewheeling path is generated by turning-on both common potential IGCTs (T1c and T2c). This sequence is also used during the switching operation of the converter for a defined period of time (FW\_level) depending on the AC Chopper input voltage value at its zero crossing, (see section 4.3.1.3).

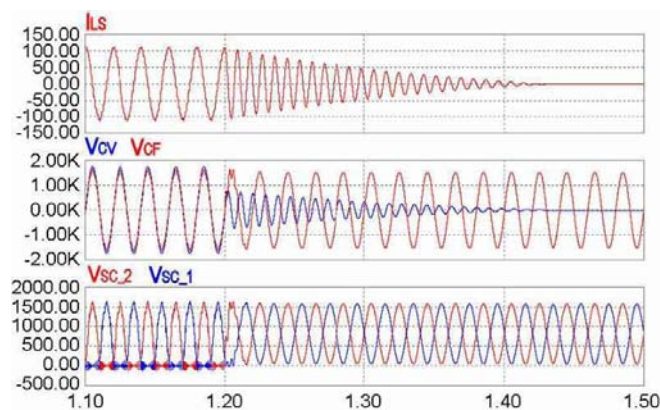


Figure 5-9.- Freewheeling sequence for discharging the energy stored on the load

Other solutions could be used to discharge the stored energy of the load in the shutdown sequence (short circuit of the load by means of an additional static switch); however, additional components will be required (bi-directional static switch, extra damping resistors, etc).

### 5.3 PWM AC Chopper Test Bench Control System

The PWM AC Chopper control system has been practically implemented using some modules (PowerPEC and PECMI boards) of the ABB's high performance control system, nowadays called AC 800PEC High Performance controller [ABB-d]. The control system combines the high-speed control requirements of power electronics applications with the low-speed control tasks of the process. In the PWM AC Chopper test platform, two control levels have been considered as represented in Figure 5-10, namely the "fast control" and the "High speed I/O control".

The "fast control" system contains the converter output current  $I_{LS}$  closed loop controller (reference generation, PI controller, etc), the human-machine interface (system monitoring and operation), and the interface with the "high speed I/O control" system (PWM modulator and failure system settings, duty cycle references generation, measurement levels adaptation and failure

values setting, etc). All these tasks are programmed by means of MATLAB<sup>®</sup>/SIMULINK<sup>®</sup> and are downloaded into the DSP of the PowerPEC control board by means of the Real-Time Workshop<sup>®</sup> (RTW) interface via the Ethernet TCP/IP communication protocol, which allows the modification of the system parameters in real-time. The cycle time of the “fast control routines” is selected to be  $T_{C\_FC}=150\mu s$  while the communication protocol time between the MATLAB/SIMULINK interface and the control board is fixed to 2.5ms.

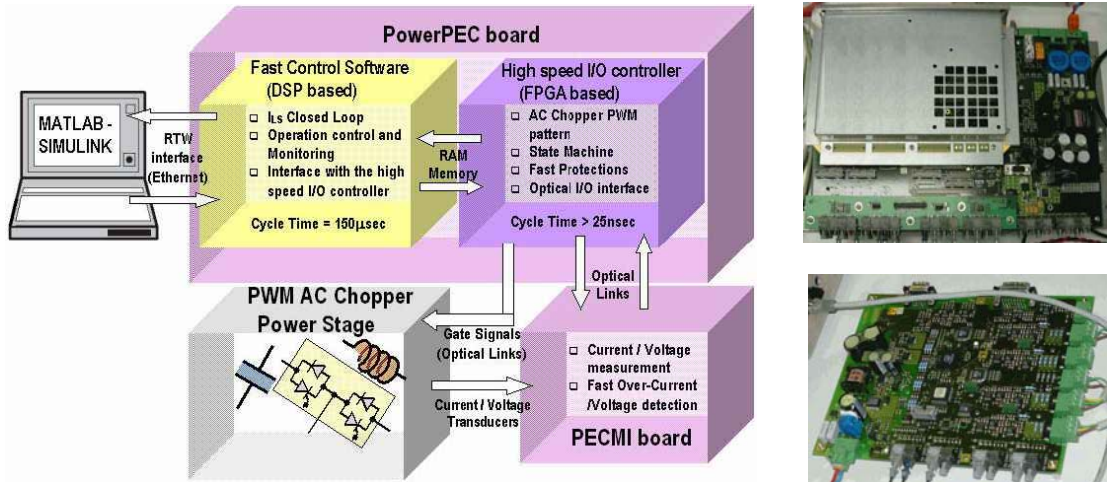


Figure 5-10.- PWM AC CHOPPER test bench control system structure

The “high speed I/O control” provides the highly time-critical functions required by the power electronics systems such as pulse-width modulators, pulse logic generation, very fast protection, fast acquisition and generation of analog and binary inputs and outputs, etc. These functions are programmed on the PowerPEC FPGA (Field programmable Gate Array) using VHDL (Very High Speed Integrated Circuit Hardware Description Language). The FPGA operates with a clock frequency of 40MHz, which provides a minimum cycle time of  $T_{CLK}=25ns$ .

In the “high speed I/O control” of the PWM AC Chopper test bench, the AC Chopper modulation pattern presented in section 4.3.1.3 is programmed to generate the semiconductor gate signals, which are sent to the AC Chopper semiconductors via optical links. In addition, a state-machine is implemented to manage the operation modes and sequences of the PWM AC Chopper (start-up, switching operation, shut-down, blocking, etc.).

The FPGA program is also responsible for the acquisition of the measurements performed on the power converter (input voltage  $V_{NET}$ , load inductor  $I_{LS}$ , and input filter inductor  $I_{LF}$  current) and provided by the measuring interface board (PECMI board with up to 8 measurement channels). The measurement signals provided by the current and voltage transducers are converted into digital values at the PECMI board level (also FPGA based). Then, the data of the different digitised measurements are sent to the PowerPEC board using a single optical link for all the measurement channels (ABB Powerlink protocol at 10Mbit/s) providing a sampling time of the signals of  $T_S=25\mu s$ . These signals can be transferred to the “Fast control” at its cycle time rate ( $T_{C\_FC}=150\mu s$ ) via a RAM memory accessible by the DSP and the FPGA of the PowerPEC board. An additional optical emitter of the PECMI board is used to send a fast failure signal to the PowerPEC board in case of over-current and/or over-voltage on the measured signals. In such a way, the PowerPEC board can react and apply the fast protection functions in less than  $2\mu s$ .

A general overview of the functions implemented on both control levels is presented in the following sections.

### 5.3.1 Overview of the FPGA Program functions

A general overview of the FPGA program functions for the single-phase STATCOM with PWM AC Choppers is shown in Figure 5-11. Each block represents a VHDL subprogram integrating a specific function. The description of the main functions is briefly introduced in the following paragraphs.

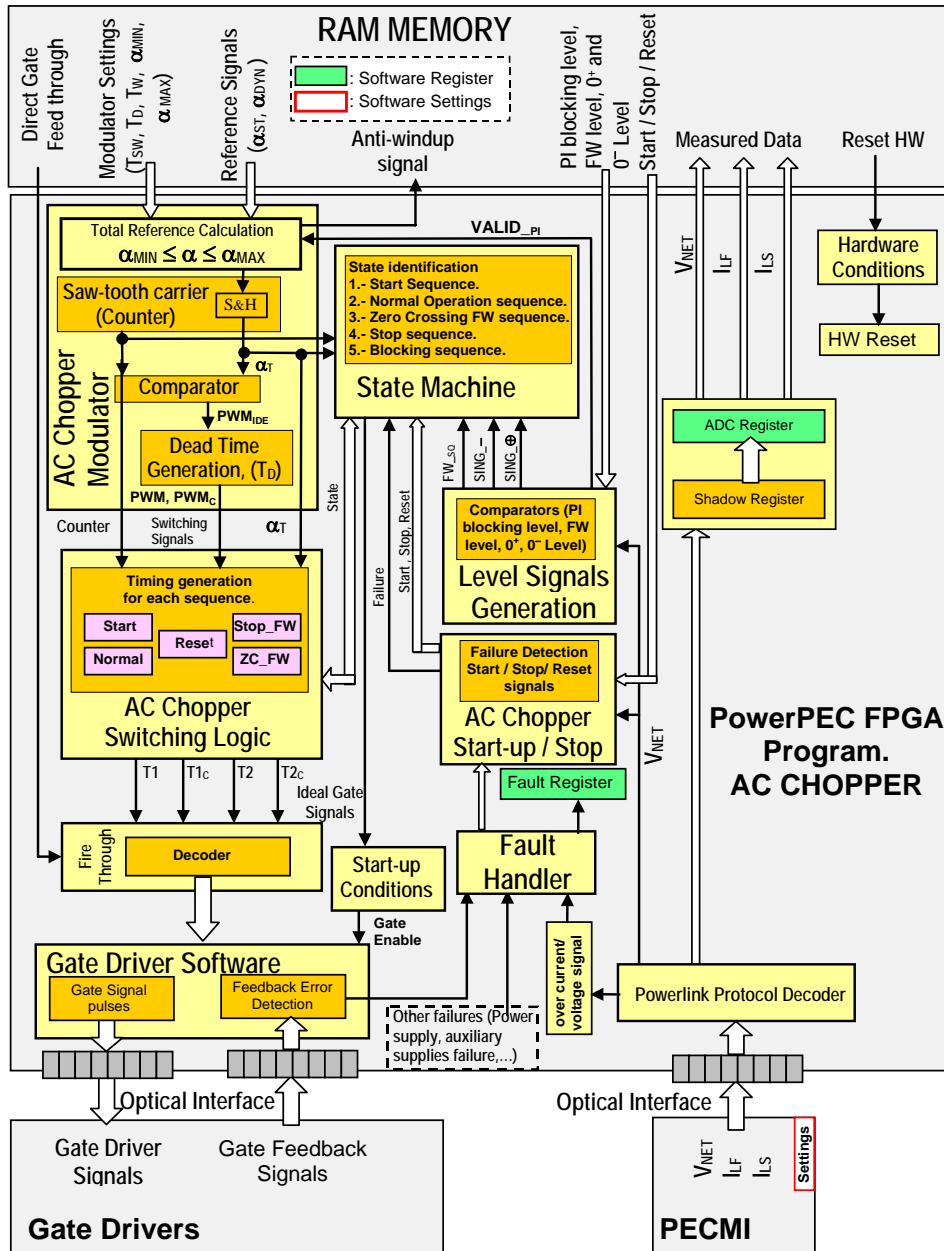


Figure 5-11.- Overview of the FPGA program functionality for the PWM AC Chopper

#### 5.3.1.1 AC Chopper PWM Modulator

The AC Chopper PWM Modulator generates the ideal PWM modulation switching pattern with dead time introduction  $T_D$  that will be applied when the switching cells of the PWM AC Chopper are in switching operation. Moreover, the total duty cycle  $\alpha_T$  evaluation is made according to the input voltage  $V_{NET}$  value (VALID\_PI signal) and the anti-windup signal for the PI controller is

generated. Also, the duty cycle applied on each switching period  $\alpha_{T\_SH}$  and the PWM carrier counter are sent to the PWM AC Chopper switching logic program to provide safe switching operation at the input voltage zero crossing (see 5.3.1.4). Figure 5-12 represents the functions implemented in the AC Chopper Modulator.

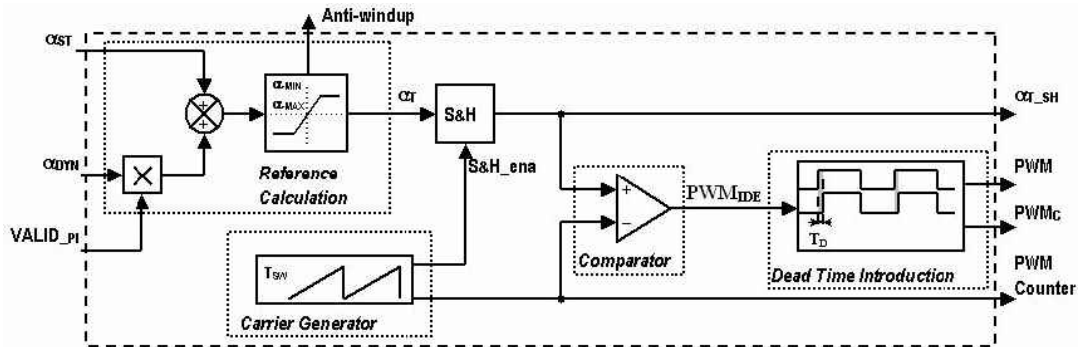


Figure 5-12.- Synoptic of the AC Chopper PWM Modulator functions

The total duty cycle reference  $\alpha_T$  is evaluated according to the  $VALID\_PI$  signal depending on input voltage value  $V_{NET}$  (see section 4.3.1.3) and the two reference signals provided by the DSP (MATLAB/Simulink program), namely  $\alpha_{ST}$  the feed forward duty cycle reference and  $\alpha_{DYN}$  the PI controller duty cycle reference. Around the zero voltage crossing of  $V_{NET}$ , the  $VALID\_PI$  signal is 0 and only the static duty cycle reference  $\alpha_{ST}$  is considered. When the  $VALID\_PI$  signal is 1, both duty cycle references are added to get the total duty cycle  $\alpha_T$ . The evaluated total duty cycle  $\alpha_T$  is compared and limited to the maximal and minimal allowable duty cycle (parameters  $\alpha_{MIN}$  and  $\alpha_{MAX}$  defined in the MATLAB/Simulink program). If the duty cycle limitation takes place, the Anti-windup signal is activated (0 value) and sent to the PI controller to block its integral action. The total duty cycle reference  $\alpha_T$  is sampled and held in synchronisation with the saw-tooth type PWM carrier. The sampling frequency is the switching frequency, whereas the sampling point is decided to take place at the end of the switching period where no switching actions happen (always the switching cell top switch is always in blocking state and the bottom switch is always in on-state). Finally, the comparison of the sampled duty cycle  $\alpha_{T\_SH}$  and the PWM carrier generates the ideal PWM pattern  $PWM_{IDE}$ . Using  $PWM_{IDE}$  as a reference, the PWM pattern with dead time introduction  $T_D$  for switching cell safe switching operation is obtained, Figure 5-13.

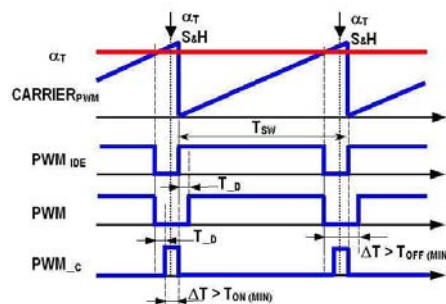


Figure 5-13.- PWM patter generation with dead time  $T_D$  introduction

### 5.3.1.2 Input voltage $V_{NET}$ level signals generation

The AC Chopper state machine and switching logic (see 5.3.1.3 and 5.3.1.4 respectively) require information about the AC Chopper input voltage  $V_{NET}$  value to generate the proper gate signals according to the modified switching pattern around its zero crossing (see section 4.3.1.3). The

input voltage level signals generation subprogram provides the required level detection signals ( $FW_{SQ}$ ,  $Sign_{-}$ ,  $Sign_{+}$ ,  $VALID_{PI}$ ). Basically, the subprogram compares the measured input voltage with the level limits ( $PI_{blocking}$  level,  $FW$  level,  $0^{+}$  level=  $-0^{-}$  level) defined in the MATLAB/Simulink program. Moreover, the input voltage measurement can be treated around its zero voltage crossing point to generate a signal that does not contain zero value ( $V_{NET\_NZ}$ ). This signal can be used in the division function integrated on the closed loop PI controller required to obtain the dynamic duty cycle reference  $\alpha_{DYN}$  (voltage reference / input voltage) avoiding zero division events, (see section 5.3.2).

### 5.3.1.3 PWM AC Chopper state machine

The PWM AC Chopper state machine identifies the power converter working operation state. This information (5 possible states) is sent to the AC Chopper switching logic (see next section), which generates the right gate signals according to the working state of the converter. Figure 5-14 shows the implemented PWM AC Chopper state machine.

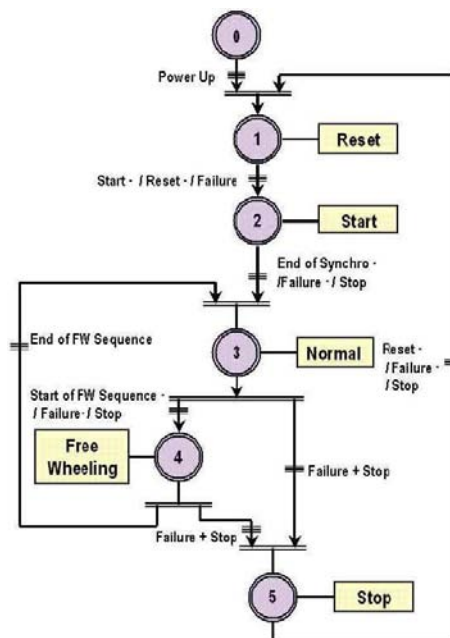


Figure 5-14.- PWM AC Chopper state machine

The converter state selection is driven by the logic combination of a set of signals coming either from other FPGA subprograms or from the MATLAB/Simulink program.

- The input voltage polarity detection signals  $Sign_{-}$  and  $Sign_{+}$  are employed to synchronise the beginning of the start switching operation at the maximum point (either positive or negative) of the input voltage (see section 5.2.2). When the synchronisation is finished (End of Synchro signal), the switching operation starts. Also, the total duty cycle  $\alpha_T$  and the PWM carrier Counter are employed to synchronise the first switching transition of the converter with the beginning of the switching period  $T_{SW}$ .
- The  $FW_{SQ}$  signal indicates the start and end points of the freewheeling sequence (Start and End of FW sequence signals) that must be launched on each input voltage zero crossing.

- The Start and Stop signals are employed to launch the start-up and shutdown sequences of the converter. The Start signal is manually activated from the MATLAB/Simulink program. The Stop order can be activated either manually from the MATLAB/Simulink program signal or from a fault signal provided by the fault handler.
- The Reset signal is used to block all the semiconductors of the AC Chopper after the shutdown sequence is finished (see 5.2.3).

The changes from one state to the other are restricted depending on the actual state and the working conditions. The "Start" state can be reached only from the "Reset" state (also considered as "Init" state) where all semiconductors are blocked. From the "Start" state the system changes directly to the "Normal" state when the input voltage is around its maximum point. In fact the "Start" state synchronises the converter's first switching transition with the input voltage maximum value (either positive or negative) by means of the input voltage polarity change detection and a 5ms timer. If the input voltage is higher than the freewheeling level, the system operates in the "Normal" state where the classical PWM switching operation is applied. From the "Normal" state, either the "Zero Crossing Free Wheeling" or the "Stop" state can be reached. In the "Zero Crossing Free Wheeling" state, the freewheeling sequence around the input voltage zero crossing is applied. When this sequence is finished (End of FW Sequence signal sent from the switching logic program to the state machine program), the system returns to the "Normal" state if no Failure or Stop signals are generated. In the "Stop" state, the shutdown sequence is generated providing a freewheeling sequence to discharge the energy of the load. From the "Stop" state only the "Reset" state is attainable if no Failure or Stop orders are held. The Reset signal (MATLAB/Simulink program) that allows the "Reset" state to be reached must be only activated if the energy of the load has already been discharged.

#### 5.3.1.4 PWM AC Chopper switching logic

The AC Chopper Switching logic generates the correct timing sequences for each switching state of the converter considering the working operation indicated by the AC chopper State machine and according to the switching pattern modification proposed in the section 4.3.1.3. Special attention is paid to the gate signals generation at the beginning and end of the "Zero Crossing Free Wheeling" state. Since these instants are random depending on the input voltage, the timing has to be defined to guarantee the dead time  $T_D$  generation and the minimum ON and OFF pulse width  $T_W$  allowed by the semiconductors (at least  $10\mu\text{s}$  for the IGBTs as defined in their datasheets).

The main output signals of the AC Chopper Switching Logic block are the Gate Signals that have to be applied to the AC Chopper semiconductors ( $T_1$ ,  $T_{1c}$ ,  $T_2$ ,  $T_{2c}$ ). Also, a state feedback signal is sent to the AC Chopper State Machine to indicate the end of the "Zero Crossing Free Wheeling" sequence at the zero crossing of the PWM AC Chopper input voltage.

#### 5.3.1.5 Gate driver software

The Gate Driver Software can convert the switching signal defined by the Switching Logic program or by the Matlab/Simulink program (Feed Through code) into a high frequency pulse train when the signal is high (1 logic). The signal remains at low value (0 logic) if the input signal value is low. The pulse frequency is adjustable to 1, 2 or 4 MHz with equal ON and OFF times. Otherwise, the Gate Driver Software simply sends the gate signals to the optical emitters. For the AC Chopper, no high frequency carrier is used and the input gate signals of the Gate Driver Software ( $T_1$ ,  $T_{1c}$ ,  $T_2$ ,  $T_{2c}$ ) are directly applied to the optical emitters.

If gate driver feedbacks are available, the gate driver software will provide the required logic to detect the working conditions of the semiconductors (On-state, Off-state, short-circuit, etc...). Since the selected IGCTs do not provide status feedback signals, this semiconductor detection program is not implemented.

### 5.3.1.6 Fault handler

The Fault Handler program is responsible for the detection and signalisation of the activation of any kind of failure signals. The main occurrences that will cause failure detection are:

- Input voltage RMS  $V_{NET\_RMS}$  value lower than the  $PI\_blocking$  level, which means that the input voltage is not big enough to make the semiconductors and converter operate in safe and stable conditions.
- Over-voltage / over-current signal sent by the measuring interface PECMI board ( $V_{NET}$  over-voltage,  $I_{LS}$  and  $I_{LF}$  over-current), detecting the over-load of the converter.

The over-voltage and over-current levels can be parameterised from the MATLAB/Simulink program. Also, the  $V_{NET\_RMS}$  value is evaluated in the MATLAB/Simulink program and sent to the FPGA program for failure detection

## 5.3.2 Overview of the MATLAB/Simulink program functions

The main MATLAB/Simulink diagram control block of the “Fast control” system for the single-phase step-down PWM AC Chopper in STATCOM operation is shown in Figure 5-15. The control system receives the measurement signals ( $V_{NET}$ ,  $I_{LS}$ ,  $I_{LF}$ ) and the anti-windup signal (1⇒integration enabled, 0⇒integration disabled) from the FPGA accessing the PowerPEC board RAM memory by means of the FPGA Input Interface block, which also contains the adapting gains to consider the binary conversion (16 bits) of the measuring board PECMI and the conversion ratios of the transducers.

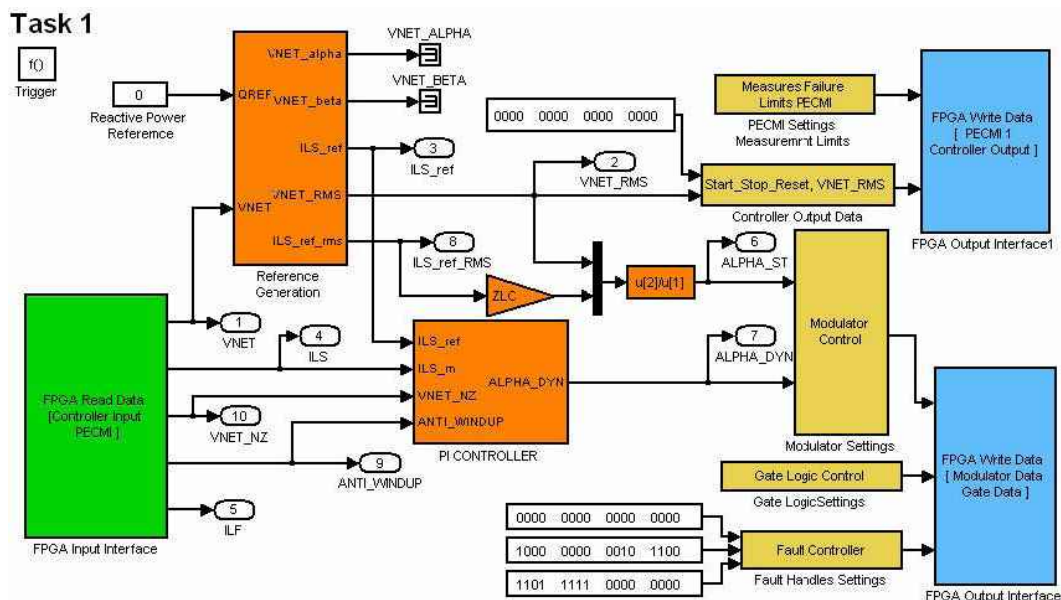


Figure 5-15.- Overview of the Matlab/Simulink control program for the single-phase AC Chopper STATCOM test bench



From the PWM AC Chopper input voltage  $V_{NET}$  measurement and the reactive power reference  $Q_{REF}$ , the instantaneous output current reference  $I_{LS\_REF}$  is obtained applying the “instantaneous complex vector” technique as reported in section 4.3.1.2.2, Figure 5-16. Also the RMS reference value of the output load current  $I_{LS\_REF\_RMS}$  and the RMS value of the input voltage  $V_{NET\_RMS}$  are obtained to derive the static duty cycle reference  $\alpha_{ST}$ , (see section 4.3.1.2.1). The impedance of the load circuit  $Z_{LC}$  is given as a fixed parameter depending on the fixed load of the converter.

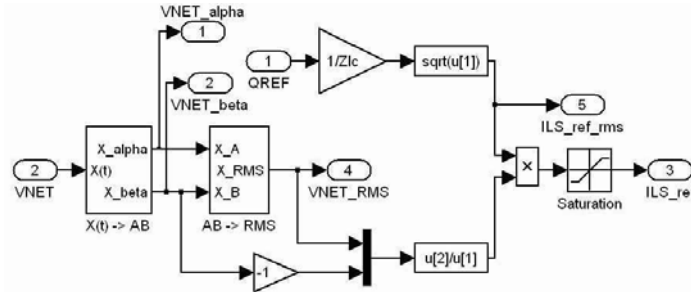


Figure 5-16.- PWM AC Chopper output current reference generation system

$I_{LS\_REF}$  is introduced into the PI Controller block where the dynamic duty cycle reference  $\alpha_{DYN}$  is going to be obtained, Figure 5-17. The proportional-integral separated actions structure of the PI is chosen to easily provide the anti-windup function to the controller. The PI output is then divided by the input voltage  $V_{NET\_NZ}$  (modified in the FPGA program to avoid the generation of 0 divisions at the zero crossing) and finally limited to vary between 1 and  $-1$ . Note that all the transfer functions, either in the PI controller block or in the reference generation block, are represented in the discrete time domain, which are directly derived from the continuous time domain transfer functions by digitalisation at the selected time cycle rate  $T_{C\_FC}=150\mu s$ .

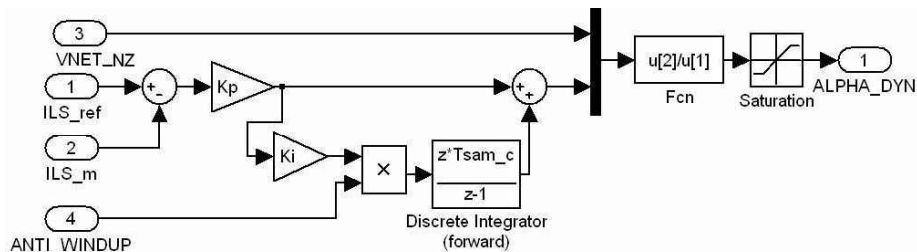


Figure 5-17.- PWM AC Chopper PI controller structure

The duty cycle references ( $\alpha_{ST}$  and  $\alpha_{DYN}$ ) are introduced into the Modulator Control block where the proper gains are applied to obtain the values that are going to be compared in the FPGA with the PWM carrier counter, Figure 5-15. The Modulator Settings (switching period  $T_{SW}$ , dead time  $T_D$ , IGCT acceptable minimum ON and Off times  $T_W$ , maximum and minimum duty cycle values  $\alpha_{MIN}$ ,  $\alpha_{MAX}$ , reference sample and hold parameters) and the level comparison values (PI\_blocking level, FW level and  $0^+$  and  $0^-$  levels) are also introduced in this block.

The operation of the converter is controlled by the Start, Stop and Reset bits of the Controller Output data block. Also, the  $V_{NET\_RMS}$  value is sent to the FPGA through this block. Other settings of the FPGA program such as the Gate Driver, Fault handler and PECMI board settings are also defined in the rest of the blocks.

The information sent from the MATLAB/Simulink program to the FPGA is made by means of the FPGA output interfaces, which write the data in defined RAM memory locations of the PowerPEC board.

## 5.4 Practical Evaluation of Single-phase step-down PWM AC Choppers in STATCOM operation

The practical evaluation of single-phase PWM AC Choppers in STATCOM operation is carried out in two different prototypes. Firstly, a low voltage/power single-phase IGBT based PWM AC Chopper prototype for reactive power compensation (capacitive) is built up to validate the proposed PWM pattern generation and control system. Then, after proposing a 100kVAR STATCOM (capacitive operation) set-up at Medium Voltage levels ( $\approx 1\text{kV}_{\text{RMS}}$ ) using an IGCT based PWM AC Chopper, the IGCT prototype is built and tested in reactive power generation (inductive) at 30kVAR due to the power limitation of the network connection point, which imposed the input filter design. The following sections describe these prototypes and show some representative waveforms of the operation of the converters.

### 5.4.1 Low Voltage/Power IGBT Based PWM AC Chopper

The main objective of the low voltage/power single-phase PWM AC Chopper prototype for reactive compensation (capacitive) is the validation of the proposed AC Chopper PWM modulation and control system. The set-up input voltage is limited to the standard low voltage network voltage (230V / 50Hz) and tests up to 5kVAR have been performed, Figure 5-18.

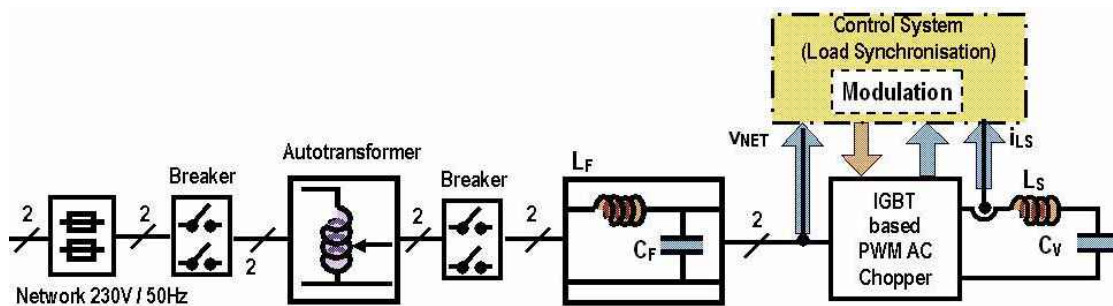


Figure 5-18.- Synoptic representation of the single-phase STATCOM set-up (capacitive operation) based on IGBT PWM AC Choppers

The characteristics of the main components employed in the set-up are summarised in Table 5-1. Figure 5-19 shows a general overview of the set-up.

Input voltage, $V_{\text{NET}}$	$V_{\text{NET}}=230\text{V}/50\text{Hz}$
Input Inductor ( $L_F$ ), Capacitor ( $C_F$ ). Resonant frequency, $f_{\text{RF}}$	$L_F=800\mu\text{H} / 40\text{A}$ , $C_F=250\mu\text{F} / 400\text{V}$ . $f_{\text{RF}}= 355\text{Hz}$
IGBT Modules (EUPEC). Natural convection cooling	FS300R12KE3 (1200V/300A)
IGBT Drivers (CONCEPT). Optical fibre gate signals	6SD106E
Decoupling Capacitors ( $C_D$ )	$C_D=0.22\mu\text{F}/1.6\text{kV}$
Switching frequency, $f_{\text{SW}}$	$f_{\text{SW}} = 1\text{kHz}$
Load Inductor ( $L_S$ ), Capacitor ( $C_V$ ). Resonant frequency $f_{\text{R}}$	$L_S=2\text{mH} / 115\text{A}$ , $C_V=250\mu\text{F} / 400\text{V}$ . $f_{\text{R}}= 225\text{Hz}$
Current sensor(LEM), $I_{L_S}$	LA55-P
Voltage sensor (ABB), $V_{\text{NET}}$	VS500B

Table 5-1.- Main components of the low voltage/power IGBT based PWM AC Chopper set-up

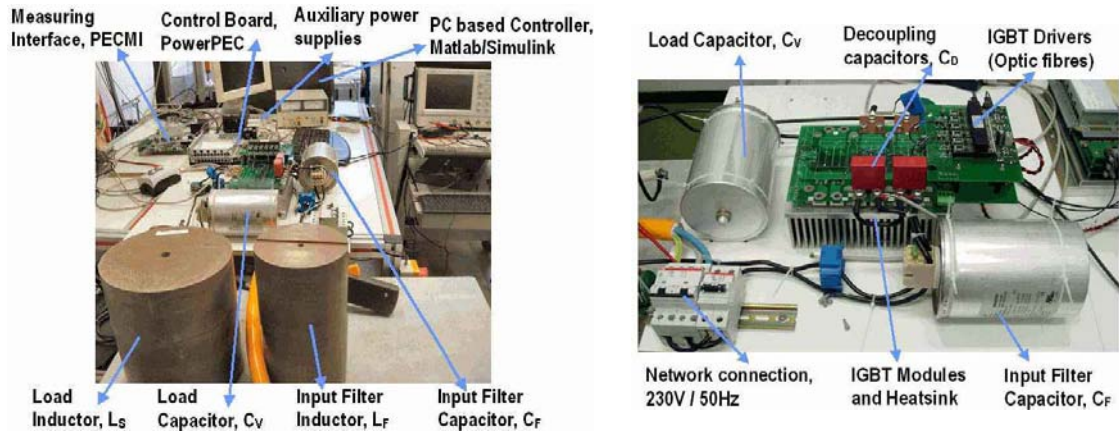


Figure 5-19.- Set-up overview of the low voltage/power IGBT based PWM AC Chopper

#### 5.4.1.1 Validation tests of the IGBT Based PWM AC Chopper

The PWM AC Chopper start-up, shutdown and switching sequences as well as the control system for reactive power compensation operation (capacitive) are successfully validated under the IGBT based PWM AC Chopper set-up.

Figure 5-20 shows the start-up sequence of the PWM AC Chopper. Before the switching operation starts (all semiconductors are blocked), the input voltage ( $V_{NET}$ , channel 3, 500V/div) is applied over the PWM AC Chopper sharing the voltage between both switching cells ( $V_{SC\_1}$  and  $V_{SC\_2}$ , channel 1 and channel 2 respectively, 200V/div). Obviously the load current ( $I_{LS}$ , channel 4) is zero. The switching operation is synchronised to start at the maximum voltage point of the input voltage  $V_{NET}$ . This avoids the high current spikes over the semiconductors of the switching cell that has to be short circuited according to the input voltage polarity due to the discharge of the decoupling capacitor  $C_D$ . At that point, the decoupling capacitor voltage of the switching cell to be short-circuited is zero.

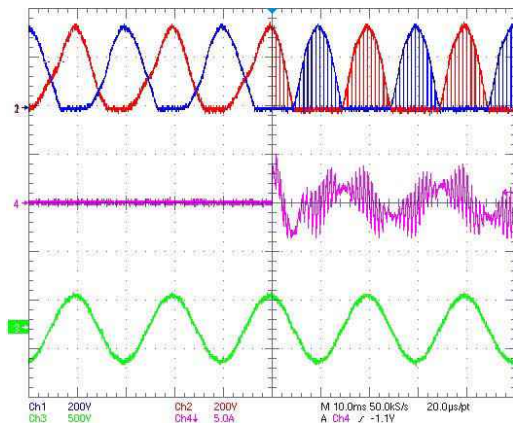


Figure 5-20.- IGBT based PWM AC Chopper start-up operation

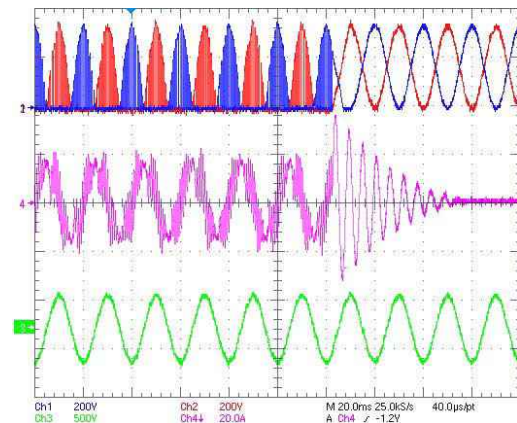


Figure 5-21.- IGBT based PWM AC Chopper shutdown operation

Figure 5-21 shows the shutdown sequence of the PWM AC Chopper. Once the shutdown signal is sent by the control system, the freewheeling state of the AC Chopper is permanently applied to discharge the energy stored in the load. The load energy is discharged over the parasitic elements of the freewheeling path (parasitic resistance of the load components and

semiconductors) generating a damped resonance at the load circuit ( $L_S$ ,  $C_V$ ) cut-off frequency  $f_R$ . Once the load energy is discharged, all semiconductors can be blocked.

In Figure 5-22 and Figure 5-23 the switching operation of the PWM AC Chopper is shown at static duty cycles  $\alpha_{ST}=0.3$  and  $\alpha_{ST}=0.5$  respectively. Notice the 90 degrees phase shift of the load current  $I_{LS}$  with respect to the input voltage  $V_{NET}$ , and the high current ripple value imposed by the low switching frequency (1kHz). The distortion on the input voltage caused by the current harmonics generated by the PWM AC Chopper operation can also be perceived.

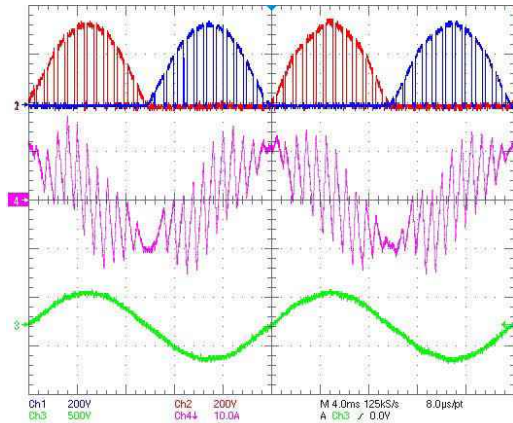


Figure 5-22.- IGBT based PWM AC Chopper switching operation at  $\alpha_{ST}=0.3$

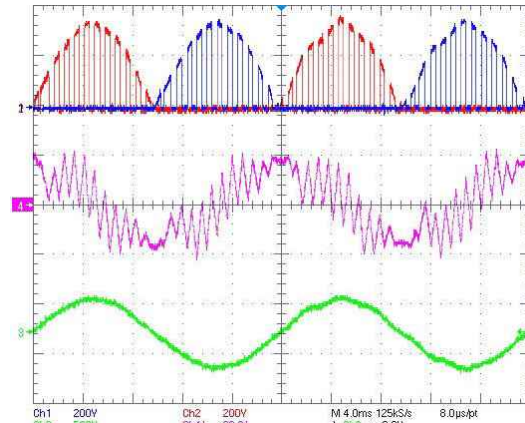


Figure 5-23.- IGBT based PWM AC Chopper switching operation at  $\alpha_{ST}=0.5$

## 5.4.2 Medium Voltage IGCT Based PWM AC Chopper

A Medium Voltage single-phase STATCOM set-up using PWM AC Choppers is built to validate the operation of the structure at higher power levels with IGCTs and their associated di/dt limitation and clamp circuits. The synoptic representation of the set-up is shown in Figure 5-24.

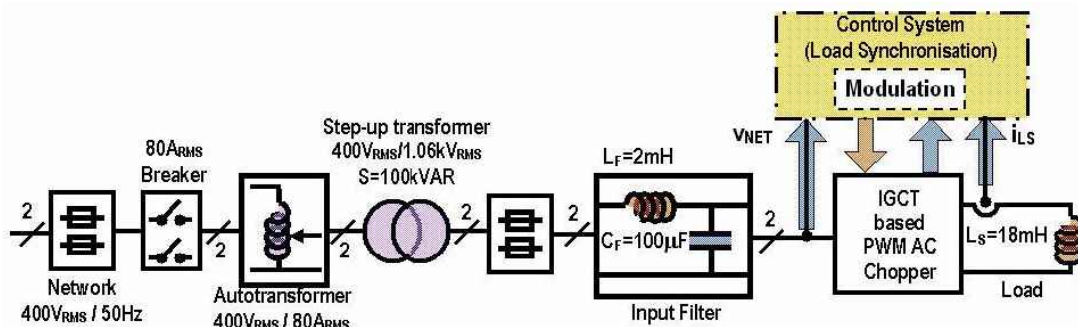


Figure 5-24.- Synoptic representation of the single-phase STATCOM set-up using an IGCT based PWM AC Chopper (inductive operation)

The AC Chopper nominal voltage is selected to be  $1.06kV_{RMS}$ , which is obtained by means of a step-up transformer supplied from the  $400V_{RMS}/50Hz$  phase to phase voltage of the three-phase standard network. An autotransformer is employed to adjust the AC Chopper input voltage  $V_{NET}$  and to slowly increase the input voltage in order to avoid the excitation of the resonant input filter ( $L_F$ ,  $C_F$ ). The autotransformer rating ( $S \approx 30kVAR$ ) limits the maximum power of the set-up. In fact, the input filter capacitor is selected to attain the autotransformer rated power ( $S \approx 30kVAR$ ) at the nominal input voltage ( $V_{NET}=1.06kV_{RMS}$ ) when the PWM AC Chopper does not operate. To allow the operation of the PWM AC Chopper as STATCOM, the load is selected to be simply an

inductor, which implies the operation of the AC Chopper as a reactive power generator (inductive operation). In this way, the power generated by the PWM AC Chopper compensates the fixed reactive power (capacitive) demanded by the input filter.

For the intended power, the smallest commercially available Reverse Conducting IGCTs are employed (ABB's 5SHX04D4502, 4.5kV/340A). Furthermore, water-cooling is adopted. Under these working conditions the semiconductors can be considered to be over-dimensioned. In this way, failure of the semiconductors can be considered to be only induced by inappropriate operation of the components and/or the proposed AC Chopper modulation. The switching frequency is fixed to  $f_{sw}=1\text{kHz}$ , the maximum admissible switching frequency reported in the datasheet of the IGCTs. Semiconductors fuses are employed to protect the IGCTs in case of short-circuit of both switching cells.

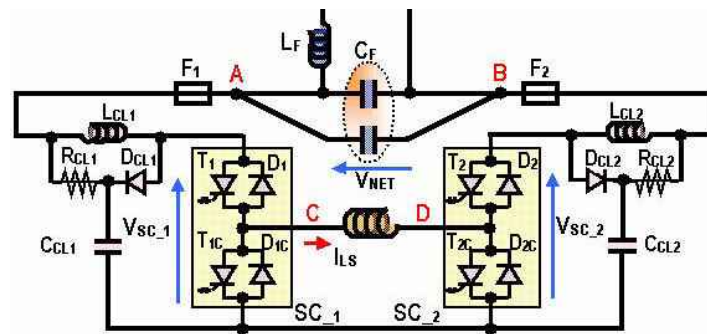


Figure 5-25.- Power stage circuit of the single-phase STATCOM set-up using IGCT based PWM AC Chopper (inductive operation)

Figure 5-25 shows the power stage circuit of the set-up and Table 5-2 shows the characteristics of the main components of the IGCT based PWM AC Chopper set-up.

Input voltage, $V_{NET}$	$V_{NET}=1.06\text{kV}_{RMS}/50\text{Hz}$
Input Inductor ( $L_F$ ), Capacitor ( $C_F$ ). Resonant frequency, $f_{RF}$	$L_F=2\text{mH} / 115\text{A}_{RMS}$ , $C_F=110\mu\text{F} / 1.5\text{kV}_{RMS}$ . $f_{RF}= 340\text{Hz}$
Reverse Conducting IGCT (ABB). Water cooling	5SHX04D450 (4.5 kV/340A)
di/dt and clamp circuit components	$L_{CL}= 12.5\mu\text{H}/100\text{A}_{RMS}$ , $C_{CL}=1\mu\text{F}/3.3\text{kV}_{DC}$ , $R_{CL}= 2\times 2\Omega/100\text{W}$ (4 $\Omega$ /200W), $D_{CL}=5\text{SDF03D4502}$ (ABB)
Fuses (Ferraz-Shawmut)	$F_1, F_2= 80\text{A}_{RMS}/ 1.25\text{kV}_{RMS} / 2.7\text{kA}^2\text{s}$ (12,5URD70TTF0080)
Switching frequency, $f_{sw}$	$f_{sw} = 1\text{kHz}$
Load Inductor ( $L_S$ ).	$L_S = 18\text{mH} / 115\text{A}_{RMS}$
Current sensor(LEM), $I_{LS}$	LF205-S/SP3
Voltage sensor (LEM), $V_{NET}$	AV 100-2000

Table 5-2.- Main components of the single-phase IGCT based PWM AC Chopper set-up

A single mechanical clamp solution is adopted to arrange the Reverse Conducting IGCTs that constitute the switching cells and the clamp circuit diodes. This solution avoids the use of additional mechanical clamps and minimises the parasitic inductor of the switching cells' switching paths, Figure 5-26. To allow the integration of all the components on a single mechanical clamp, several isolating parts are integrated in the stack (yellow parts in Figure 5-26). Notice also the arrangement of the switching cells' common point ( $T_{1C}$  and  $T_{2C}$  connection) where two heat sinks are stacked consecutively. This arrangement is used exclusively to provide enough

room for the IGCT drivers positioning. The switching cell output connections (point C and D) and the connection with the clamp circuit components are made by flexible copper sheets to avoid the application of externally generated mechanical efforts over the components of the stack. Electrical connections between the stack input (A and B points) and output (C and D points) connections are made using unipolar isolated cables ( $1\text{kV}_{\text{RMS}}$  isolation). The mechanical clamp is connected to ground for safety reasons. Figure 5-27 shows the stack arrangement already installed in the set-up.

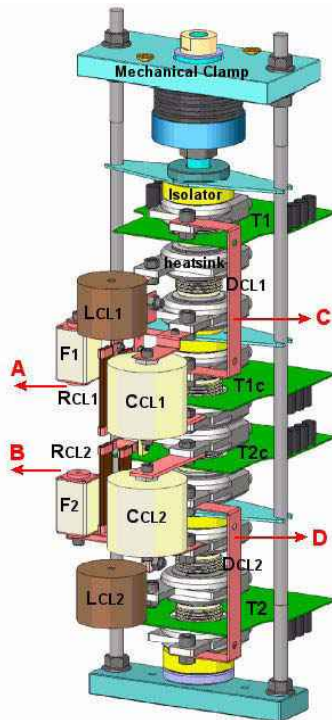


Figure 5-26.- Arrangement of the switching cells and clamp circuit components of the IGCT set-up

Figure 5-27.- Overview of the semiconductors stack and clamp circuit components of the IGCT set-up

The semiconductors stack and clamp circuit components are arranged on a cabinet together with the main passive components of the power stage. The heaviest components (input filter inductor  $L_F$  and load inductor  $L_S$  made up of several series connected  $2\text{mH}/115\text{A}_{\text{RMS}}$  inductors) are placed in the bottom side of the cabinet. The stack and the main capacitors are placed in the topside of the cabinet, Figure 5-28. The control board (PowerPEC), measuring interface (PECMI), and other additional elements (auxiliary power supplies, gate units power supplies, safety switch, water circuit input and output spreaders, etc.) are arranged over the different girders of the cabinet structure. It is also important to indicate the use of two decoupling capacitors ( $2 \times 5\mu\text{F}/3.3\text{kV}_{\text{DC}}$ ) taking part of the input filter capacitor  $C_F$  arranged as close as possible to the stack input connections (points A and B in Figure 5-26) to minimise the parasitic inductance between the input filter and the PWM AC Chopper semiconductors.

Figure 5-29 shows an overview of the set-up where the arrangement of the different components can be distinguished. Notice two additional inductors placed outside the cabinet to obtain the required  $18\text{mH}/115\text{A}_{\text{RMS}}$  load inductor  $L_S$ . Obviously, the supply of the set-up (autotransformer and step-up transformer) is not integrated on the cabinet and has to be operated remotely from the laboratory control desk outside of the Medium Voltage test zone. The metallic structure of the cabinet and the body of the rest of the components are connected to ground for safety reasons. When the system is not operated, the input filter capacitors are short-circuited and grounded by means of a safety switch.

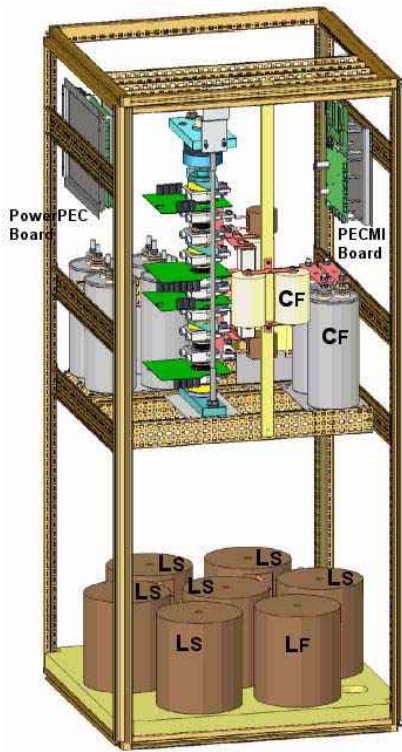


Figure 5-28.- Main components arrangement of the IGCT based PWM AC Chopper set-up



Figure 5-29.- Overview of the IGCT based PWM AC Chopper set-up

#### 5.4.2.1 Validation tests of the IGCT Based PWM AC Chopper

Basic validation tests are accomplished to assess the correct behaviour of the system, mainly regarding the different operation modes of the converter and the  $di/dt$  inductor and the influence of the clamp circuit components on the current waveforms of the IGCTs.

Figure 5-30 shows the PWM AC Chopper start-up process applied to the IGCT based set-up. Since all semiconductors are blocked before the load inductor current ( $I_{LS}$ , channel 2, 20A/div) starts increasing due to the switching operation of the converter, the input voltage ( $V_{NET}$ , channel 4, 1kV/div) is applied over the PWM AC Chopper sharing the voltage between both switching cells ( $V_{SC_1}$ , channel 3, 500V/div).

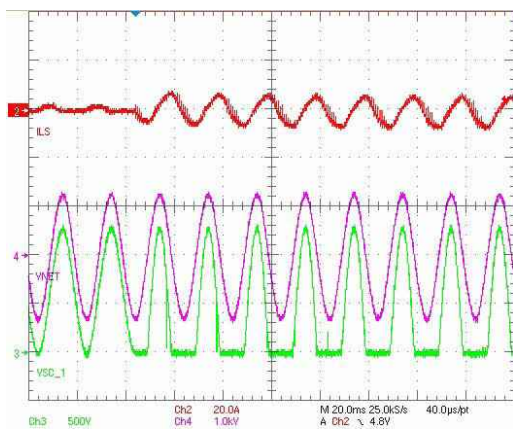


Figure 5-30.- IGCT based PWM AC Chopper start-up operation

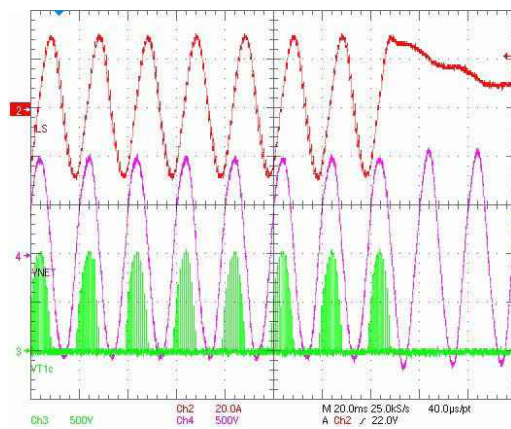


Figure 5-31.- IGCT based PWM AC Chopper shutdown operation

Once the switching operation starts, synchronised with the maximum voltage point of the input voltage  $V_{NET}$ , the switching cell voltages ( $V_{SC\_1}$  and  $V_{SC\_2}$ ) alternately present a zero value due to the switching cell short-circuit phase applied according to the PWM AC Chopper input voltage,  $V_{NET}$ .

Figure 5-31 shows the shutdown operation of the converter. During the shutdown sequence, the load is freewheeled by means of  $T_{1C}$  and  $T_{2C}$  and their respective freewheeling diodes. Since the load is an inductor ( $L_S$ ), the load current waveform ( $I_{LS}$ , channel 2, 20A/div) decays exponentially to zero. The time constant of the shutdown operation is imposed by the inductor value and the value of the parasitic resistors of the freewheeling path. Once the current of the load inductor is zero, all the semiconductors can be blocked and are consequently ready to start operating again.

Notice the increase on the PWM AC Chopper input voltage ( $V_{NET}$ , channel 4, 500V/div) when the switching operation is stopped ( $V_{T1C}$ , channel 3, 500V/div). As the PWM AC Chopper stops operating, the reactive power of the input filter is not compensated anymore causing the increase of the PWM AC Chopper input voltage  $V_{NET}$ .

The switching operation of the PWM AC Chopper can be shown in Figure 5-32. In can be noticed how the load inductor current ( $I_{LS}$ , channel 2, 50A/div,  $I_{LS\ RMS}=35A$ ) is controlled to be sinusoidal at the network frequency with 90 degrees of lagging phase shift with respect to the PWM AC Chopper input voltage ( $V_{NET}$ , channel 4, 1kV/div). Notice the switching current and voltage ripple in the load current as well as in the input voltage  $V_{NET}$  and consequently over the switching cell voltage, ( $V_{SC\_1}$ , channel 3, 500V/div).

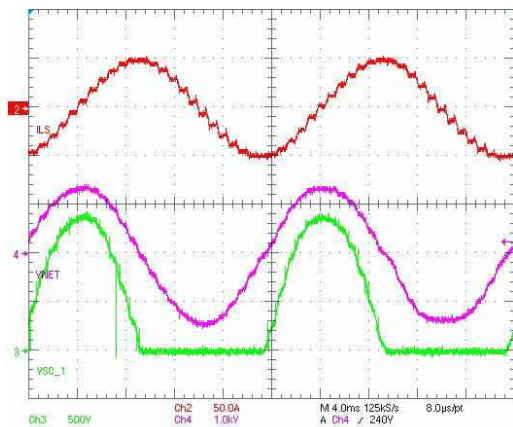


Figure 5-32.- IGCT based PWM AC Chopper switching operation ( $V_{NET}=1kV_{RMS}$ ,  $I_{LS}=35A_{RMS}$ )

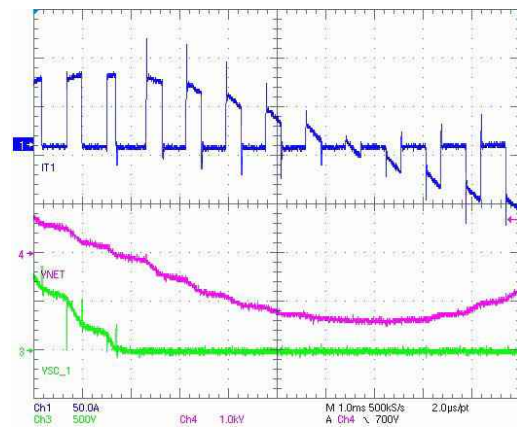


Figure 5-33.- Reverse Conducting IGCT ( $T_1, D_1$ ) switching operation ( $V_{NET}=1kV_{RMS}$ ,  $I_{LS}=35A_{RMS}$ )

Figure 5-33 shows the current  $I_{T1}$  (channel 1, 50A/div) of the reverse conducting IGCT  $T_1$  (IGCT  $T_1$  and freewheeling diode  $D_1$ ). During the switching operation of the switching cell  $SC_{-1}$ , when the switching cell voltage  $V_{SC\_1}$  (channel 3, 500V/div) is positive, no important current spikes appear in the semiconductor current. The small current spikes that can be noticed are generated by the recovery current of the freewheeling diode that has just been turned-off. Over the switching cell voltage  $V_{SC\_1}$ , it can be noticed that the zero voltage phases corresponding to the  $di/dt$  limitation at IGCT turn-on and the slight voltage spikes limited by the clamp circuit at IGCT turn-off.

During the switching cell short-circuit phase of  $SC_{-1}$  ( $V_{SC\_1}=0$ ), the excitation effects of its associated  $di/dt$  inductor and clamp circuit components by the switching operation of the adjacent switching cell  $SC_{-2}$  can be observed. Mainly the relatively important spikes in both polarities over the current of the semiconductor ( $I_{T1}$ ) are noticed (see section 4.3.1.1.2), although their values are well limited by the minimisation of the parasitic inductor between the input filter and the



switching cells by using decoupling capacitors connected as close as possible to the connection points of the switching cells (A and B points in Figure 5-26). These decoupling capacitors take part of the input filter capacitor and also provide some reactive power generation.

The increase of the reactive power generated (inductive) by the PWM AC Chopper shows the important influence of the input filter capacitor value over the behaviour of this topology. When the output current increases Figure 5-34 ( $I_{LS\text{ RMS}}=50\text{A}$ ), the input voltage  $V_{\text{NET}}$  (channel 4, 1kV/div) voltage ripple increases. Since the voltage ripple increases, the freewheeling phase length of the zero crossing point at the input voltage zero crossing can increase according to the adopted operation strategy (several zero crossing events can be detected due to the switching frequency voltage ripple). These freewheeling sequences at the input voltage zero crossing leads to zero current phases in the PWM AC Chopper input current, see  $I_{T1}$  (channel 1, 100A/div). The longer the PWM AC Chopper input current zero phases (longer than a switching period), the higher the low frequency harmonic content of the AC Chopper input current, which causes the input voltage  $V_{\text{NET}}$  distortion. Despite the well controlled load current  $I_{LS}$  (channel 2, 50A/div), the PWM AC Chopper generates relevant low frequency harmonics.

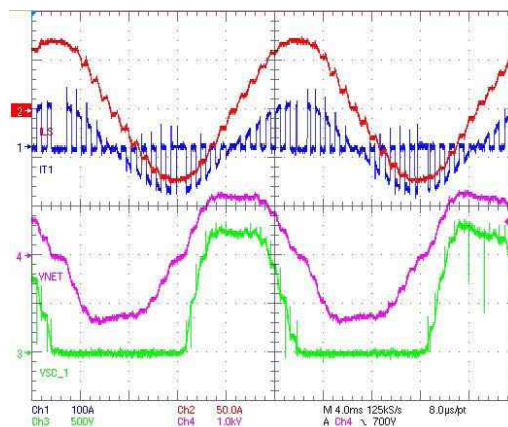


Figure 5-34.- IGCT based PWM AC Chopper switching operation ( $V_{\text{NET}}=1\text{kV}_{\text{RMS}}$ ,  $I_{\text{LS}}=50\text{A}_{\text{RMS}}$ )

The increase of the input filter capacitor  $C_F$  value (higher fixed reactive power compensation) and/or the use of additional control strategies considering the low frequency voltage harmonics in the PWM AC Chopper input filter could improve the behaviour of the AC Chopper. Obviously, the increase of the switching frequency and/or the use of several interleaved PWM AC Chopper modules reduce the PWM AC Chopper input voltage switching ripple and helps to ameliorate the system operation, see Chapter 4.

## 5.5 Conclusions

The practical evaluation of the single-phase step-down PWM AC Choppers in STATCOM operation (inductive and capacitive) is presented in this chapter. Firstly, the specific operating sequences of the PWM AC Chopper (network connection, start-up and shutdown) required to guarantee the stable and safe operation of the system are presented. Then, the control system common to the different set-ups tested is briefly described presenting the most important functions of the controller. Finally, the operation of the two different set-ups built to validate the design and control concepts analysed in Chapter 4 are presented. The first set-up is based on low voltage IGBTs and is mainly employed to validate the PWM modulation strategy adopted to provide safe operation of the PWM AC Chopper semiconductors and to validate the reactive power control system. The second set-up operating at Medium Voltage levels based on standard

Reverse Conducting IGCTs is mainly built to validate the feasibility of the PWM AC Choppers that use IGCTs and reach higher power levels (>30kVAR).

# Conclusion & Future Prospects

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The contributions of this dissertation are related to the use of high power / medium voltage semiconductors for medium power applications, and especially concerns the introduction of experimental 3.3kV IGCTs, the low voltage IGCT version derived from the standard asymmetric 4.5kV IGCTs.

After reviewing the most significant high power / medium voltage semiconductors and introducing the basic operation principles and implementation requirements of IGCT based power converters, an opposition method test bench was developed to achieve the characterisation of the experimental 3.3kV IGCTs. The system allowed testing the semiconductors in DC chopper operation mode in continuous switching operation at peak power values up to 3MW (switched current and voltage reaching 2kA and 1.5kV respectively). Although the test bench was intended to drive the 3.3kV IGCT at switching frequencies up to 2kHz, the need for more powerful gate unit power supplies and even the requirement of adapted gate units developed to operate at higher switching frequencies, limited the maximal test switching frequency to 1kHz. Extrapolation of the characterisation results was then employed to derive the operation limits (power losses) and driving requirements (gate unit power supply consumption) demanded by the 3.3kV IGCTs to reach operation at 2kHz.

The characterisation results showed the very low on-state voltage drop and acceptable switching losses of these components, which allows handling high current values (2kA - 1kA) at high switching frequencies (1kHz - 2kHz) with no need for component paralleling. In this way, power converters at medium voltage and medium power level with higher dynamic and reliability performances can be obtained. These arguments can be employed to favour the selection of 3.3kV IGCTs instead of the well market established 3.3kV IGBTs. However, the 3.3kV IGCT market introduction is restrained due to the fact that the use of the IGCT technology is less extended among the power converters manufacturer and to the lack of potential markets and other commercial arguments that could justify the investment on the production of these semiconductors. In the future, the increasing demand of power electronics systems in the electric distribution area related to the increase of electric power consumption could motivate such investments.

Several potential applications (active filtering and reactive power compensation) have been analysed that apply different conversion structures based on 3.3kV IGCTs. This analysis demonstrated the reduced part count required to comply with the system dynamic and static specifications imposed by the application. A universal power losses estimation tool for 3.3kV IGCT switching cells has been employed first to perform a general comparison among the considered solutions. This tool is specifically designed to take into account the relevant working conditions of medium power converters such as high current ripple, switching cell voltage change, over-modulation operation, etc. Furthermore, the use of this tool could be easily extended to other semiconductor technologies.

One of the interesting topologies, where the characteristics of the 3.3kV IGCTs can be better exploited, is the PWM AC Choppers. In these topologies, the on-state losses are dominant, which, under certain conditions allows handling higher power levels if compared to other

topologies. However, the field of application of the PWM AC Chopper is restricted to applications where a direct AC/AC conversion between two AC sources characterised by the same fundamental frequency is required. This reduces the benefit of using such topologies to certain specific applications.

An application where the use of PWM AC Choppers can be advantageous is the reactive power compensation of the distribution network. The control strategy, switching pattern and component dimensioning process for a 3MVAR single-phase STATCOM intended for its application in the SNCF 25kV/50Hz substations is proposed. The proposed conversion structure consists of three step-down PWM AC Chopper modules rated at 1MVAR driving the 3.3kV IGCTs at a switching frequency of 1kHz. Simulation results show the acceptable behaviour of the proposed solution under normal conditions, although certain restrictions regarding the harmonic generation of the converter must be taken into account. Higher switching frequencies and/or adapted control strategies can be considered to provide a solution to overcome these restrictions. The proposed control strategy and switching pattern generation have been validated at low voltage and medium voltage levels respectively over IGBT and IGCT set-ups operating in reactive power compensation (capacitive and inductive operation).

The most challenging future prospect that arises from this dissertation is the experimental evaluation of a real scale 3MVAR STATCOM prototype for the SNCF 25kV/50Hz substations. Such implementation requires a more detailed comparison among the possible solutions, not only considering technical aspects, but also economic and market potential aspects. Other conversion structures (PWM AC Chopper based or VSI based) and semiconductor technologies could also be considered to finally select the best solution. If the use of PWM AC Choppers is considered, a more exhaustive analysis of the interaction of the converter with the real network operating conditions (voltage harmonics, sags, etc.) is required. This analysis concerns mainly the control strategies required to guarantee the correct operation of the system. The control of the PWM AC Chopper input current instead of the control of the load current should be considered as a potential solution to improve the system performance, which requires additional research efforts for the application of advanced modelling and control strategies that allow for considering the highly non-linear behaviour of the topology. Other potential applications of PWM AC Choppers could also take advantage of such research efforts.

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# Appendix 1

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## 2-Level VSI and Step-down AC-Chopper Current Ripple Estimation for Single Phase Reactive Power Compensation

### 6.1 Introduction

The selection of the power converter inductors value is subjected to low frequency and high frequency considerations. The low frequency considerations (DC or AC) are mainly delimited by the maximum available power of the converter for specific semiconductor operating ratings (blocking voltage, switched current), which imposes the inductor maximum current and voltage drop. The high frequency considerations are mainly related to the converter high frequency harmonics generation and filtering (switching frequency, topology, etc.), where the inductor current ripple  $\Delta I_{LS}$  is the crucial parameter. Furthermore, the current ripple can also exert relevant influence on the power losses of the inductor and on the on-state and switching losses of semiconductors. Consequently, a trade-off between the low and high frequency considerations must be defined when selecting the inductors values for any specific application. Statement of such a trade-off requires the accurate evaluation of the current ripple.

In some cases, such as DC/DC converters, the evaluation of the current ripple is relatively simple and accurate. The operation with DC input and output voltages and with relatively high switching frequencies simplify the evaluation task. However, in cases where the low frequency current and voltages are changing (AC operation), and the switching frequency is relatively low compared to the frequency of the fundamental signals, the current ripple evaluation is not straightforward and must be carefully analysed. Analytical methods and circuit simulations offer wide possibilities to obtain an accurate evaluation of the current ripple.

### 6.2 Current Ripple Evaluation of a Full Bridge 2-level VSI

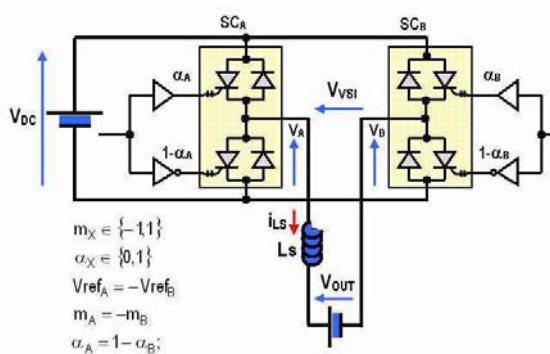
Classically, the evaluation of the current switching ripple of the full-bridge 2 level inverter in DC/DC operation is used as a reference to evaluate the current ripple when the inverter operates in DC/AC conversion. This approach is valid if two main conditions are respected:

- The switching frequency is much higher than the frequency of the AC signal to be reconstructed, and therefore, the output voltage can be considered constant throughout the switching period.
- The low frequency voltage drop on the inductor is negligible (0 in DC operation).

Otherwise, other approaches applying analytical methods or circuit simulation are required. The following sections present the classical  $\Delta I$  evaluation method for DC/DC operation, and shows the limitations of this method for DC/AC operation when the switching frequency is relatively low and the low frequency voltage drop is relatively high. Then, other analytical methods are proposed to evaluate the current ripple for DC/AC operation. The results obtained with these methods are compared with circuit simulation results to validate their applicability.

### 6.2.1 Current ripple evaluation in DC / DC operation

Considering the DC/DC operation of the VSI, the inverter voltage average value  $\langle V_{VSI} \rangle$  can be either positive or negative according to the modulation index ( $m = m_A = -m_B$ ), that is, according to the duty cycle of the switching cells  $SC_{-A}$  ( $\alpha_A$ ) and  $SC_{-B}$  ( $\alpha_B = 1 - \alpha_A$ ), Eq. 6-1 to Eq. 6-5.



$$m_A = \frac{V_{refA}}{V_p}; \alpha_A = \frac{1}{2} \cdot (1 + m_A) \quad \text{Eq. 6-1}$$

$$\langle V_A \rangle = V_{DC} \cdot \alpha_A \quad \text{Eq. 6-2}$$

$$m_B = \frac{V_{refB}}{V_p}; \alpha_B = \frac{1}{2} \cdot (1 + m_B) \quad \text{Eq. 6-3}$$

$$\langle V_B \rangle = V_{DC} \cdot \alpha_B \quad \text{Eq. 6-4}$$

$$\langle V_{VSI} \rangle = V_{DC} \cdot m_A = V_{DC} \cdot (2 \cdot \alpha_A - 1) \quad \text{Eq. 6-5}$$

Figure 6-1.- Full Bridge 2-level VSI in DC/DC operation

Applying the unipolar modulation, the switching patterns for both switching cells are generated comparing a triangular carrier at the switching frequency ( $f_{sw}$ ) with two reference signals with the same amplitude but opposite polarity ( $V_{refA} = -V_{refB}$ ), Figure 6-2. The semiconductors of each switching cell are controlled complementary. This strategy allows obtaining an apparent switching frequency at the VSI output twice the switching frequency.

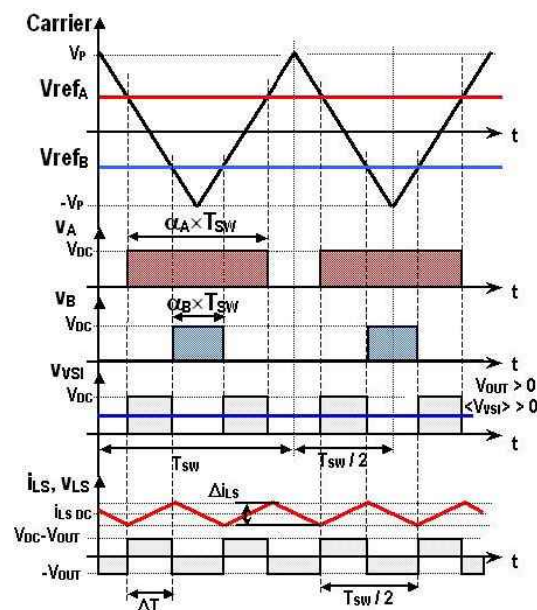


Figure 6-2.- Positive VSI average voltage generation ( $m_A > 0, 1 > \alpha_A > 0.5, \langle V_{VSI} \rangle > 0$ ).

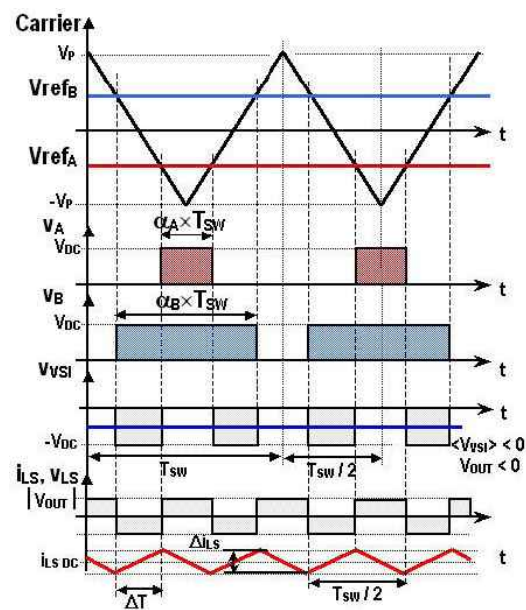


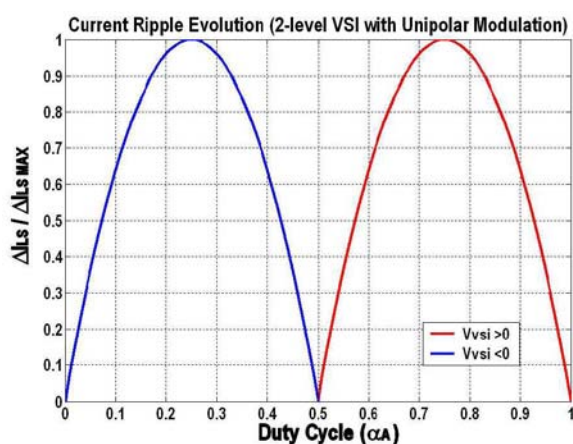
Figure 6-3.- Negative VSI average voltage generation ( $m_A < 0, 0 < \alpha_A < 0.5, \langle V_{VSI} \rangle < 0$ ).

Using the unipolar modulation, the positive average inverter voltage values ( $\langle V_{VSI} \rangle > 0 \Rightarrow 1 > \alpha_A > 0.5$  and  $0 < \alpha_B < 0.5$ ), is generated by voltage pulses changing from  $V_{DC}$  to 0, Figure 6-2. When negative values are needed ( $\langle V_{VSI} \rangle < 0 \Rightarrow 0 < \alpha_A < 0.5$  and  $1 > \alpha_B > 0.5$ ), the pulses change from 0 to  $-V_{DC}$ , Figure 6-3. In both cases, the current ripple evolution is driven by slightly different expressions. Therefore, analyses in both operation modes must be carried out.

In steady state, the VSI average voltage  $\langle V_{VSI} \rangle$  is equal to the output voltage  $V_{OUT}$ . In ideal conditions, the ideal inductor voltage amplitudes and pulse lengths ( $\Delta T$ ) are known, which allows estimating the current ripple  $\Delta I_{LS}$  expressions, (Eq. 6-8 for  $V_{VSI} > 0$  and Eq. 6-11 for  $V_{VSI} < 0$ ). Obviously, the current ripple along  $T_{SW}/2 - \Delta T$  is the same as the one evaluated along  $\Delta T$ , ( $\Delta I_{LS ON} = \Delta I_{LS OFF}$ ).

$\Delta I_{LS}$ expression for $V_{VSI} > 0$ ( $1 > \alpha_A > 0.5$ and $0 < \alpha_B < 0.5$ )		
	$\Delta T = \frac{T_{SW} \cdot (\alpha_A - \alpha_B)}{2} = (2\alpha_A - 1) \cdot \frac{T_{SW}}{2}$	Eq. 6-6
	$\Delta I_{LS} = \frac{v_{LS}(\Delta T)}{L_S} \cdot \Delta T = \frac{V_{DC} - V_{OUT}}{L_S} \cdot \Delta T = \frac{V_{DC} - V_{VSI}}{L_S} \cdot \Delta T = \frac{V_{DC} - V_{DC} \cdot (2\alpha_A - 1)}{L_S} \cdot \Delta T$	Eq. 6-7
	$\Delta I_{LS} = \left  \frac{V_{DC}}{L_S \cdot f_{SW}} \cdot (2\alpha_A - 1) \cdot (1 - \alpha_A) \right ; \quad 1 > \alpha_A > 0.5;$	Eq. 6-8
$\Delta I_{LS}$ expression for $V_{VSI} < 0$ ( $0 < \alpha_A < 0.5$ and $1 > \alpha_B > 0.5$ )		
	$\Delta T = \frac{T_{SW} \cdot (\alpha_B - \alpha_A)}{2} = (1 - 2\alpha_A) \cdot \frac{T_{SW}}{2}$	Eq. 6-9
	$\Delta I_{LS} = \frac{v_{LS}(\Delta T)}{L_S} \cdot \Delta T = \frac{-V_{DC} +  V_{OUT} }{L_S} \cdot \Delta T = \frac{-V_{DC} - V_{DC} \cdot (2\alpha_A - 1)}{L_S} \cdot \Delta T$	Eq. 6-10
	$\Delta I_{LS} = \left  \frac{V_{DC}}{L_S \cdot f_{SW}} \cdot (2\alpha_A - 1) \cdot \alpha_A \right ; \quad 0 < \alpha_A < 0.5$	Eq. 6-11

The maximum current ripple, Eq. 6-12, is obtained for  $\alpha_A = 0.25$  when the inverter voltage is negative, and for  $\alpha_A = 0.75$  when it is positive. Figure 6-4 shows the evolution of the current ripple as a function of the duty cycle  $\alpha_A$ .



$$\Delta I_{LS MAX} = \frac{V_{DC}}{8 \cdot L_S \cdot f_{SW}} \quad \text{Eq. 6-12}$$

Figure 6-4.- Current ripple evolution for a 2-level VSI with unipolar modulation (DC/DC operation)

## 6.2.2 Current ripple evaluation in DC / AC operation (reactive power compensation)

The operation of the 2-level VSI in DC/AC conversion implies the operation with variable duty cycle to obtain the desired AC output voltage. Since the current ripple changes with the duty cycle, AC operation implies change of the current ripple throughout the low frequency period ( $T=2\pi/\omega$ ). To illustrate this fact, the operation of the VSI as reactive power compensator is considered, Figure 3-49. In this operation mode, the steady state expressions relating the network injected current  $I_{LS}$ , the network voltage  $V_{NET}$  and the inverter voltage  $V_{VSI}$ , define the duty cycle evolution, Eq. 6-13 to Eq. 6-15.

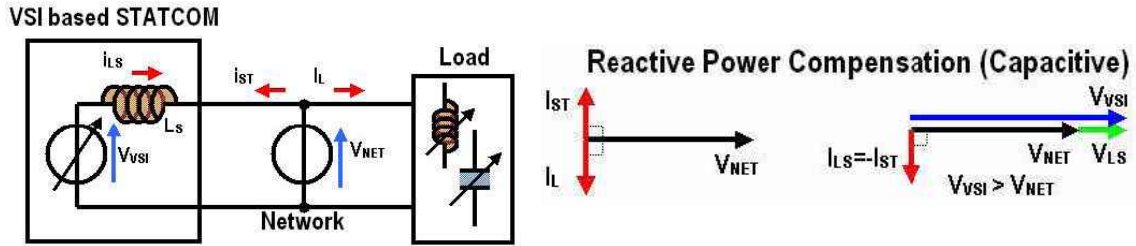


Figure 6-5.- VSI based STATCOM steady state vector diagrams (capacitive and inductive)

$$\vec{V}_{VSI} = \vec{V}_{NET} + \vec{V}_{LS}; \quad \text{Eq. 6-13}$$

$$V_{VSI}(t) = (V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2} \cdot \sin(\omega \cdot t)$$

$$m_A = -m_B = \frac{V_{VSI}}{V_{DC}} = \frac{(V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2} \cdot \sin(\omega \cdot t)}{V_{DC}} \quad \text{Eq. 6-14}$$

$$\alpha_A = 1 - \alpha_B = \frac{1}{2}(1 + m_A) = \frac{1}{2} + \frac{(V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2} \cdot \sin(\omega \cdot t)}{2 \cdot V_{DC}} \quad \text{Eq. 6-15}$$

If the evolution of  $\alpha_A$  (Eq. 6-15) and the voltage expression (Eq. 6-13) are put into the  $\Delta I_{LS}$  expression (Eq. 6-7), the evolution of the current ripple can be obtained for the DC/AC conversion operating mode, Eq. 6-17.

$$\Delta_T = (2\alpha_A - 1) \cdot \frac{T_{SW}}{2} = \frac{(V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2} \cdot \sin(\omega \cdot t)}{2 \cdot V_{DC} \cdot f_{SW}} \quad \text{Eq. 6-16}$$

$$\Delta_{ILS} = \frac{V_{LS}(\Delta_T)}{L_S} \cdot \Delta_T \quad \text{Eq. 6-17}$$

$$\Delta_{ILS} = \frac{V_{DC} - (V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2} \cdot \sin(\omega \cdot t)}{L_S} \cdot \frac{(V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2} \cdot \sin(\omega \cdot t)}{2 \cdot V_{DC} \cdot f_{SW}}$$

Evaluation of Eq. 6-17 throughout the network 50Hz positive half cycle ( $V_{VSI} > 0$ ) shows the idealised evolution of the inductor current ripple. For numerical evaluation, the switching frequency  $f_{SW}$  is fixed to 1kHz, the DC link voltage  $V_{DC}$  to 1.5kV and the network RMS voltage  $V_{NET}$  and injected current  $I_{LS}$  to 800V<sub>RMS</sub> and 970A<sub>RMS</sub> respectively. Figure 6-6 shows the current ripple evolution presenting a maximum of 375A when the duty cycle is  $\alpha_A = 0.75$ , which corresponds to the idealised value defined by Eq. 6-12.

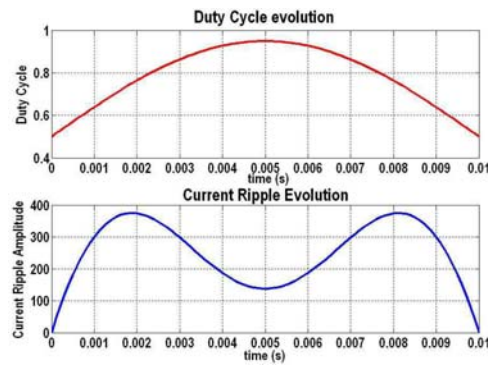


Figure 6-6.- 2-level VSI current ripple idealised evolution for reactive power operation ( $V_{VSI} > 0$ )

To check the validity of the analytical current ripple evaluation, circuit simulation of the VSI is performed using ideal switches. The simulation considers the inductor current loop, the modulator sampling and hold of the PI controller output at the switching frequency rate, the switching cell dead time generation, and inductor and semiconductor resistive terms. Figure 6-7 shows the inductor current and voltage waveforms together with the VSI voltage and the network voltage. The simulation results show that the evolution of the current ripple follows the expected evolution evaluated in Figure 6-6 but with a maximum current ripple around 486A instead of the ideal current ripple value of 375A, more than 110A of difference. It can be also noticed that the increasing current ripple ( $\Delta I_{LS\ ON}$ , positive  $di/dt$ ) is different from the decreasing current ripple ( $\Delta I_{LS\ OFF}$ , negative  $di/dt$ ), which confirms that under the considered operating conditions the expressions derived from the DC/DC operation of the VSI do not apply. The operation at low switching frequency (sampling of the modulation signal at the switching frequency) and the response of the current loop controller to compensate the VSI non ideal behaviour (dead times, power losses, etc) are found to be the main reasons to obtain higher current ripple.

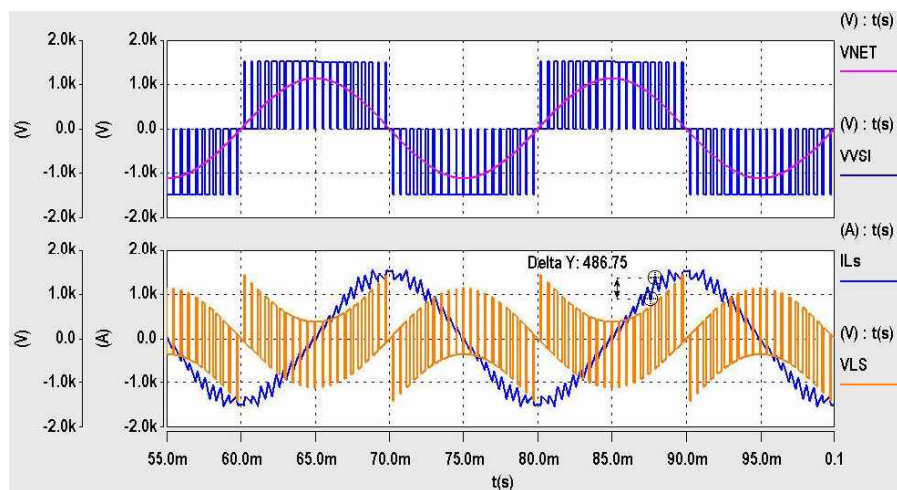


Figure 6-7.- Current ripple evaluation by circuit simulation

To obtain a more accurate current ripple evaluation, the influence of the switching frequency and sampling and hold of the modulation index can be taken into account. Considering the ideal current and voltage steady state vectors of the system, Figure 3-49, the modulation indexes ( $m_A$ ,  $m_B$ ) are derived and sampled at the switching frequency rate as depicted in Figure 6-8. Along the switching period, the modulation indexes remain constant and the network voltage and injected current change is not negligible. Therefore, they must be taken into account.

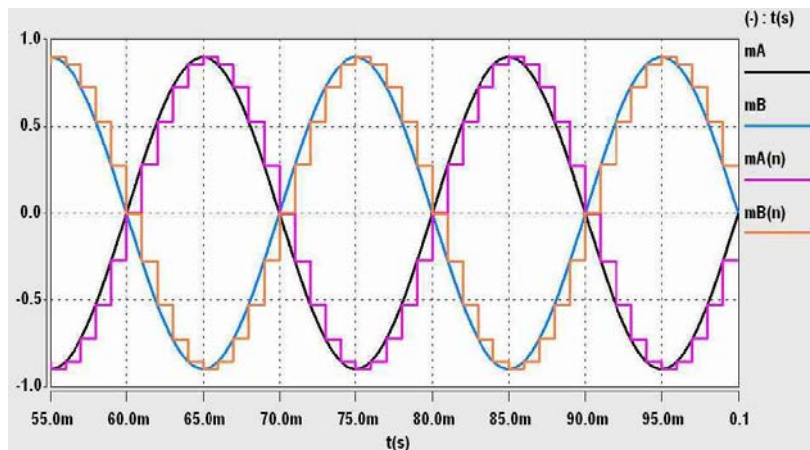
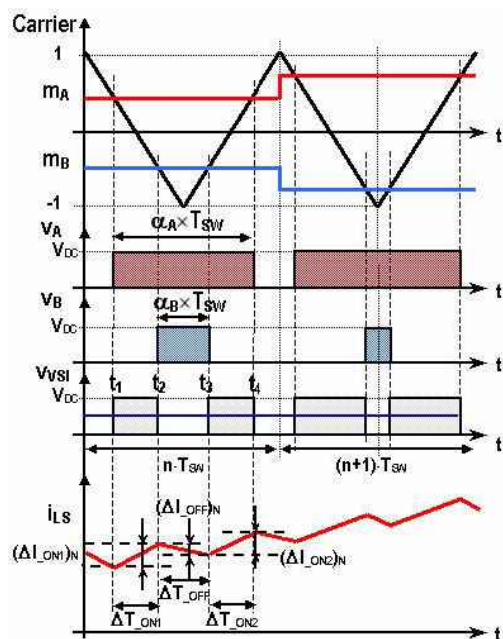


Figure 6-8.- Sampling and hold of the modulation indexes at the switching frequency rate

Considering the sampling of the PWM modulator, the discrete definition of the modulation index and duty cycles throughout the switching period "n" can be written, Eq. 6-18, Eq. 6-19. Comparison of the discrete modulation index with the PWM carrier allows defining the switching instants  $t_1$ ,  $t_2$ ,  $t_3$  and  $t_4$  for the corresponding switching period "n". Therefore, the pulse lengths of the voltage applied to the inductor can be obtained, Figure 6-9.

$$m_A = -m_B = \frac{(V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2}}{V_{DC}} \cdot \sin(\omega \cdot n \cdot T_{SW}) \quad \text{Eq. 6-18}$$

$$\alpha_A = 1 - \alpha_B = \frac{1}{2}(1 + m_A) = \frac{1}{2} + \frac{(V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2}}{2 \cdot V_{DC}} \cdot \sin(\omega \cdot n \cdot T_{SW}) \quad \text{Eq. 6-19}$$



$$t_1 = n \cdot T_{SW} + (1 - \alpha_A) \cdot \frac{T_{SW}}{2} \quad \text{Eq. 6-20}$$

$$t_2 = n \cdot T_{SW} + \alpha_A \cdot \frac{T_{SW}}{2} \quad \text{Eq. 6-21}$$

$$t_3 = n \cdot T_{SW} + (2 - \alpha_A) \cdot \frac{T_{SW}}{2} \quad \text{Eq. 6-22}$$

$$t_4 = n \cdot T_{SW} + (1 + \alpha_A) \cdot \frac{T_{SW}}{2} \quad \text{Eq. 6-23}$$

$$\Delta T_{OFF} = t_3 - t_2 = (1 - \alpha_A) \cdot T_{SW} \quad \text{Eq. 6-24}$$

$$\Delta T_{ON1} = t_2 - t_1 = (2 \cdot \alpha_A - 1) \cdot \frac{T_{SW}}{2} \quad \text{Eq. 6-25}$$

$$\Delta T_{ON2} = t_4 - t_3 = (2 \cdot \alpha_A - 1) \cdot \frac{T_{SW}}{2} \quad \text{Eq. 6-26}$$

Figure 6-9.- Switching times definition for the switching period "n".

The proposed method evaluates on each pulse length ( $\Delta T_{ON1}$ ,  $\Delta T_{ON2}$  and  $\Delta T_{OFF}$ ) the voltage applied to the inductor. Then, integration of the voltage expressions provides the inductor current expression on each time interval. The current ripple is obtained evaluating the inductor current expression on the times delimiting each time interval (e.g.  $t_1$  and  $t_2$  for  $\Delta T_{ON1}$ ). The following



equations present the switching current expressions for the 50Hz positive half cycle of the voltage network ( $1 > \alpha_A > 0.5$ ).

- $\Delta I_{LS\_ON1}$ , positive di/dt ( $0.5 < \alpha_A < 1$ ,  $n \in [0, T/(2 \cdot T_{SW})]$ )

$$\begin{aligned} v_{LS}(t) &= V_{DC} - (V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \\ i_{LS}(t) &= \int \frac{v_{LS}(t)}{L_S} dt = \int \left[ \frac{V_{DC}}{L_S} - \left( \frac{V_{NET}}{L_S} + \omega \cdot I_{LS} \right) \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \right] \cdot dt \\ i_{LS}(t) &= \frac{V_{DC}}{L_S} \cdot t + \left( \frac{V_{NET}}{L_S \cdot \omega} + I_{LS} \right) \cdot \sqrt{2} \cdot \cos(\omega \cdot t) \end{aligned} \quad \text{Eq. 6-27}$$

$$\begin{aligned} \Delta I_{LS\_ON1} &= |i_{LS}(t_2) - i_{LS}(t_1)| \\ \Delta I_{LS\_ON1} &= \frac{V_{DC}}{L_S} \cdot (2\alpha_A - 1) \cdot \frac{T_{SW}}{2} + \\ &+ \left( \frac{V_{NET}}{L_S \cdot \omega} + I_{LS} \right) \cdot \sqrt{2} \cdot \left[ \cos\left(\omega \cdot T_{SW} \cdot \left(n + \frac{\alpha_A}{2}\right)\right) - \cos\left(\omega \cdot T_{SW} \cdot \left(n + \frac{1 - \alpha_A}{2}\right)\right) \right] \end{aligned} \quad \text{Eq. 6-28}$$

$$\begin{aligned} \Delta I_{LS\_ON2} &= |i_{LS}(t_4) - i_{LS}(t_3)| \\ \Delta I_{LS\_ON2} &= \frac{V_{DC}}{L_S} \cdot (2\alpha_A - 1) \cdot \frac{T_{SW}}{2} + \\ &+ \left( \frac{V_{NET}}{L_S \cdot \omega} + I_{LS} \right) \cdot \sqrt{2} \cdot \left[ \cos\left(\omega \cdot T_{SW} \cdot \left(n + \frac{1 + \alpha_A}{2}\right)\right) - \cos\left(\omega \cdot T_{SW} \cdot \left(n + 1 - \frac{\alpha_A}{2}\right)\right) \right] \end{aligned} \quad \text{Eq. 6-29}$$

- $\Delta I_{LS\_OFF}$ , negative di/dt ( $0.5 < \alpha_A < 1$ ,  $n \in [0, T/(2 \cdot T_{SW})]$ )

$$\begin{aligned} v_{LS}(t) &= -(V_{NET} + L_S \cdot \omega \cdot I_{LS}) \cdot \sqrt{2} \cdot \sin(\omega \cdot t); \\ i_{LS}(t) &= \int \frac{v_{LS}(t)}{L_S} dt = \int \left[ -\left( \frac{V_{NET}}{L_S} + \omega \cdot I_{LS} \right) \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \right] \cdot dt = \left( \frac{V_{NET}}{L_S \cdot \omega} + I_{LS} \right) \cdot \sqrt{2} \cdot \cos(\omega \cdot t) \end{aligned} \quad \text{Eq. 6-30}$$

$$\begin{aligned} \Delta I_{LS\_OFF} &= |i_{LS}(t_3) - i_{LS}(t_2)| \\ \Delta I_{LS\_OFF} &= \left( \frac{V_{NET}}{L_S \cdot \omega} + I_{LS} \right) \cdot \sqrt{2} \cdot \left[ \cos\left(\omega \cdot T_{SW} \cdot \left(n + 1 - \frac{\alpha_A}{2}\right)\right) - \cos\left(\omega \cdot T_{SW} \cdot \left(n + \frac{\alpha_A}{2}\right)\right) \right] \end{aligned} \quad \text{Eq. 6-31}$$

Numerical evaluation of these expressions is shown in Figure 6-10. The evaluation results show that a maximum current ripple around 520A ( $\Delta I_{LS\_ON2}$ ) will be reached, which is much closer to the circuit simulation results (486A) than the idealised evaluation method (375A). Furthermore, the sample number with respect to the beginning of the 50Hz period where the maximum current ripple appears ( $n=8$ ) coincides with the circuit simulation result. However, no symmetry of the current ripple evolution is obtained, whereas in the circuit simulation this symmetry does exist. The proposed method can be considered more accurate than the idealised evaluation method, but still certain differences with respect to the circuit simulation are obtained. These differences are mainly due to the effect of the closed loop operation of the system when circuit simulation is applied. In fact, the steady state modulation index is modified by the control loop to compensate the non-linear behaviour of the converter (dead time, semiconductors voltage drop, etc.). Circuit simulation is therefore, the best solution to obtain an accurate evaluation of the current ripple of the converter inductor when dimensioning of the inductor is going to be performed. Nevertheless, for dimensioning of the converter, the sampling method here proposed could provide better current ripple estimation than the idealised method.

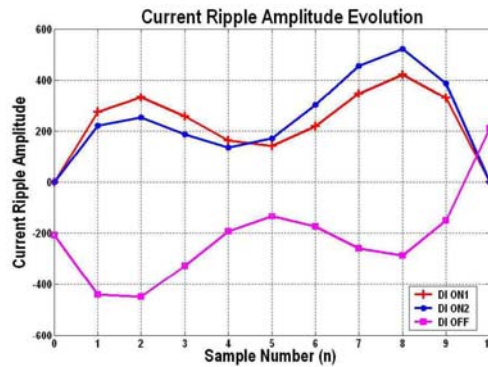


Figure 6-10.- Current ripple estimation considering the sampling of the modulation index

### 6.3 Current Ripple Evaluation of a Step-down PWM AC Chopper

The single-phase step-down AC Chopper principle for reactive power compensation is shown in Figure 3-67. The converter duty cycle ( $\alpha$ ) is modified to adjust the AC Chopper output voltage  $V_{ACC}$  and thus adjust the reactive power consumption of the load ( $C_{VAR}$ ,  $L_S$ ). The ideal relation between the network voltage  $V_{NET}$  and the AC Chopper output voltage  $V_{ACC}$  is defined by Eq. 6-32. The smoothing inductor  $L_S$  is required to guarantee the current source behaviour of the load, but the load has capacitive nature at the network frequency. Therefore, the operation of the AC Chopper allows modifying the load RMS voltage acting over the duty cycle, which makes the system ideally behave as a variable capacitor. The load current fundamental term is then defined by the duty cycle ( $\alpha$ ), the input voltage value  $V_{NET}$  and the load impedance  $Z_{LC}$  at the network frequency ( $\omega=2\cdot\pi\cdot f$ ), Eq. 6-33 and Eq. 6-34.

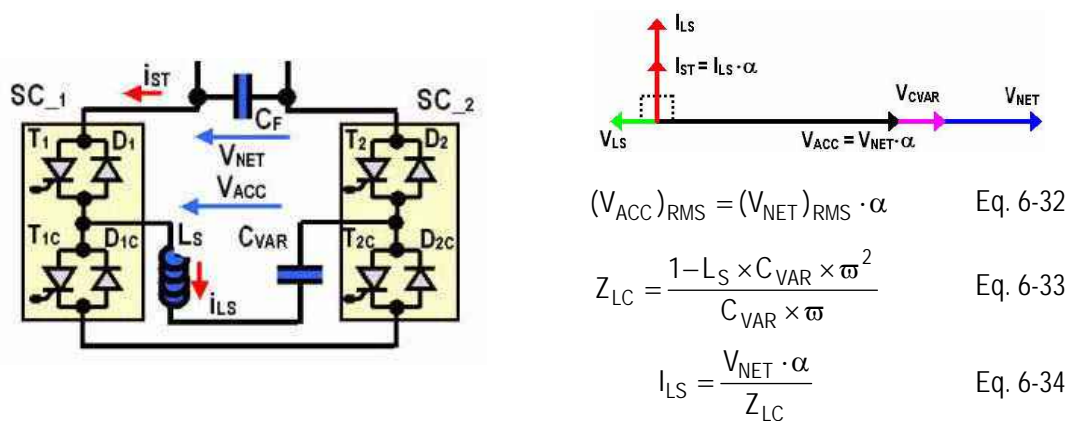


Figure 6-11.- AC Chopper based STATCOM steady state vector diagram

The current ripple on the smoothing inductors depends on the switching pattern employed by the AC Chopper. Also, the low frequency steady state current and voltage for reactive power compensation represented by the vector diagram of Figure 3-67 must be considered.

The pattern here considered is based on the polarity of the AC Chopper input voltage,  $V_{NET}$ . When  $V_{NET}$  is positive, the switching cell  $SC_2$  is short-circuited and the switching cell  $SC_1$  operates in PWM. On the other hand, when  $V_{NET}$  is negative,  $SC_2$  is PWM operated and  $SC_1$  is short-circuited.

According to the switching pattern, the AC chopper output voltage can adopt four different states. These four different values imply four  $\Delta I_{LS}$  expressions to be evaluated. The control signal  $u_s$  ( $u_s=1$ , switching cell upper switch ON, lower switch OFF;  $u_s=0$ , switching cell upper switch OFF, lower switch ON), together with the input voltage polarity are used to represent the different available states.

The first step to obtain the  $\Delta I_{LS}$  expressions is to evaluate the expressions of the output inductor voltage term at the switching frequency  $v_{LS\_HF}$  for each control signal  $u_s$  and input voltage polarity, Eq. 6-40. The high frequency voltage term of the output capacitor ( $v_{CVAR\_HF}$ ) can be neglected because the capacitor value  $C_{VAR}$  is selected to provide the required reactive power compensation. That is, its value is big enough to consider negligible the high frequency voltage ripple over the output capacitor.

$$v_{NET} = V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \quad \text{Eq. 6-35}$$

$$i_{LS} = i_{LS\_BF} + i_{LS\_HF} = I_{LS} \cdot \sqrt{2} \cdot \cos(\omega \cdot t) + i_{LS\_HF} \quad \text{Eq. 6-36}$$

$$v_{LS} = v_{LS\_BF} + v_{LS\_HF} = -I_{LS} \cdot L_S \cdot \omega \cdot \sqrt{2} \cdot \sin(\omega \cdot t) + v_{LS\_HF} \quad \text{Eq. 6-37}$$

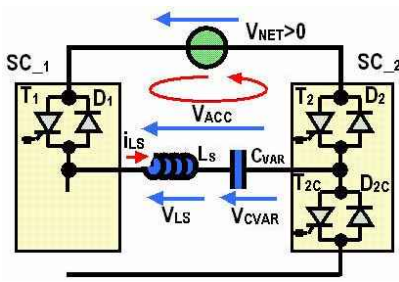
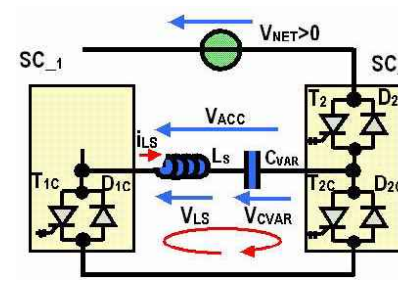
$$v_{CVAR} = v_{CVAR\_BF} + v_{CVAR\_HF} = \frac{I_{LS}}{C_{VAR} \cdot \omega} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) + v_{CVAR\_HF} \quad \text{Eq. 6-38}$$

$$v_{ACC\_BF} = V_{NET} \cdot \sqrt{2} \cdot \alpha \cdot \sin(\omega \cdot t) \quad \text{Eq. 6-39}$$

$$v_{CVAR\_HF} \approx 0 \quad \text{Eq. 6-40}$$

$$v_{LS\_HF}(u_s) \approx v_{ACC}(u_s) - v_{LS\_BF} - v_{CVAR\_BF}$$

The  $v_{LS\_HF}$  expressions for the four possible states are summarised in the table below, Table 6-1.

$V_{NET}(t) > 0, u_s = 1$ (Active Phase)	$V_{NET}(t) > 0, u_s = 0$ (Free wheeling Phase)
$v_{NET} = V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t); \quad \omega \cdot t \in [0, \pi];$ $i_{LS\_BF} = \frac{V_{NET} \cdot \alpha}{Z_{LC}} \cdot \sqrt{2} \cdot \cos(\omega \cdot t)$ $v_{LS\_BF} = -\frac{V_{NET} \cdot \alpha}{Z_{LC}} \cdot L_S \cdot \omega \cdot \sqrt{2} \cdot \sin(\omega \cdot t)$ $v_{CVAR\_BF} = \frac{V_{NET} \cdot \alpha}{Z_{LC}} \cdot \frac{1}{C_{VAR} \cdot \omega} \cdot \sqrt{2} \cdot \sin(\omega \cdot t)$	
	
$v_{ACC}(u_s) = v_{ACC}(1) = v_{NET} = V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t)$ $v_{LS\_HF}(u_s) = v_{ACC}(1) - v_{LS\_BF} - v_{CVAR\_BF}$ $v_{LS\_HF}(1) = V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot (1 - \alpha)$	$v_{ACC}(u_s) = v_{ACC}(0) = 0$ $v_{LS\_HF}(u_s) = v_{ACC}(0) - v_{LS\_BF} - v_{CVAR\_BF}$ $v_{LS\_HF}(0) = -V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot \alpha$

$V_{NET}(t) < 0, u_S=1$ (Active Phase)	$V_{NET}(t) < 0, u_S=0$ (Free wheeling Phase)
$v_{NET} = -V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t); \quad \omega \cdot t \in [0, \pi];$ $i_{LS\_BF} = -\frac{V_{NET} \cdot \alpha}{Z_{LC}} \cdot \sqrt{2} \cdot \cos(\omega \cdot t)$ $v_{LS\_BF} = \frac{V_{NET} \cdot \alpha}{Z_{LC}} \cdot L_S \cdot \omega \cdot \sqrt{2} \cdot \sin(\omega \cdot t)$ $v_{CVAR\_BF} = -\frac{V_{NET} \cdot \alpha}{Z_{LC}} \cdot \frac{1}{C_{VAR} \cdot \omega} \cdot \sqrt{2} \cdot \sin(\omega \cdot t)$	
$v_{ACC}(u_S) = v_{ACC}(1) = -V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t)$ $v_{LS\_HF}(u_S) = v_{ACC}(1) - v_{LS\_BF} - v_{CVAR\_BF}$ $v_{LS\_HF}(1) = -V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot (1 - \alpha)$	$v_{ACC}(u_S) = v_{ACC}(0) = 0$ $v_{LS\_HF}(u_S) = v_{ACC}(0) - v_{LS\_BF} - v_{CVAR\_BF}$ $v_{LS\_HF}(1) = V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot \alpha$

Table 6-1.- AC Chopper Switching states. Evaluation of the output inductor high frequency voltage term

Once the  $v_{LS\_HF}$  expressions are evaluated, the  $\Delta i_{LS}$  expressions can be obtained integrating it ( $di_{LS}/dt = v_{LS\_HF} / L_S$ ) over the switching state time ( $T_{ON}$  or  $T_{OFF}$ ), Table 6-2. As it can be seen, the current ripple expressions have the same absolute value for each switching state, only their polarity change depending on the input voltage polarity and the sort of phase applied (active or free wheeling).

$V_{NET}(t) > 0, u_S=1$ (Active Phase)	$V_{NET}(t) > 0, u_S=0$ (Free wheeling Phase)
$\Delta i_{LS} = \frac{v_{LS\_HF}(u_S = 1)}{L_S} \cdot T_{ON};$ $\Delta i_{LS} = \frac{V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot (1 - \alpha) \cdot \alpha}{L_S \cdot f_{SW}}$ <p style="text-align: right;">Eq. 6-41</p>	$\nabla i_{LS} = \frac{v_{LS\_HF}(u_S = 0)}{L_S} \cdot T_{OFF};$ $\nabla i_{LS} = \frac{-V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot \alpha \cdot (1 - \alpha)}{L_S \cdot f_{SW}}$ <p style="text-align: right;">Eq. 6-42</p>
$V_{NET}(t) < 0, u_S=1$ (Active Phase)	$V_{NET}(t) < 0, u_S=0$ (Free wheeling Phase)
$\Delta i_{LS} = \frac{v_{LS\_HF}(u_S = 1)}{L_S} \cdot T_{ON};$ $\Delta i_{LS} = \frac{-V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot (1 - \alpha) \cdot \alpha}{L_S \cdot f_{SW}}$ <p style="text-align: right;">Eq. 6-43</p>	$\nabla i_{LS} = \frac{v_{LS\_HF}(u_S = 0)}{L_S} \cdot T_{OFF};$ $\nabla i_{LS} = \frac{V_{NET} \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot \alpha \cdot (1 - \alpha)}{L_S \cdot f_{SW}}$ <p style="text-align: right;">Eq. 6-44</p>

Table 6-2.-  $\Delta i_{LS}$  expressions for the four AC Chopper switching states.

The switching ripple current evolution can be easily evaluated by simulation if considering the ideal operation of the AC Chopper at constant duty cycle. This can be done by the multiplication of the absolute value of the expressions obtained above with a triangular function that varies

between 0.5 and  $-0.5$ , (the slope is imposed by the duty cycle). The absolute value gives the amplitude of the current ripple and the triangular waveform provides its evolution. Figure 6-12 and Figure 6-13 show examples of the output current ripple evaluation of the AC Chopper for  $\alpha=0.5$  and  $\alpha=0.75$ . In these figures, different current ripple maximum amplitudes can be noticed. As expected, the operation at  $\alpha=0.5$  leads to higher current ripple than the operation at  $\alpha=0.75$ . In fact, the maximal current ripple is given at  $\alpha=0.5$ .

$$\Delta I_{LSMAX} = \Delta I_{LS}(\alpha = 0.5) = \frac{V_{NET} \cdot \sqrt{2} \cdot \sin(\varpi \cdot t)}{4 \cdot L_S \cdot f_{SW}} \quad \text{Eq. 6-45}$$

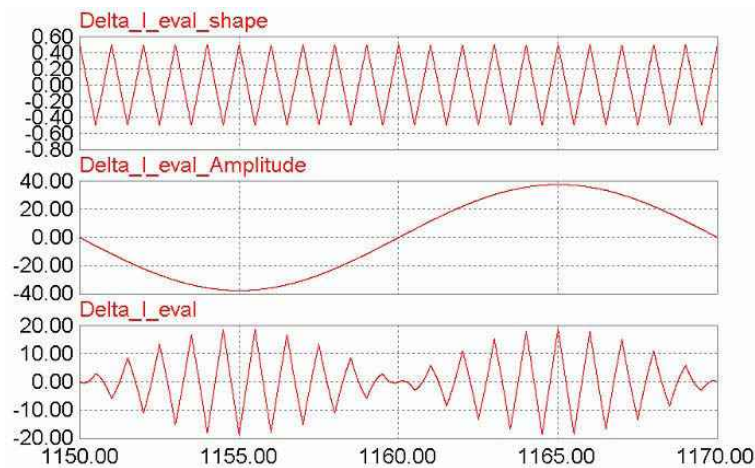


Figure 6-12.- AC Chopper output current ripple evaluation example,  $\alpha=0.5$ .

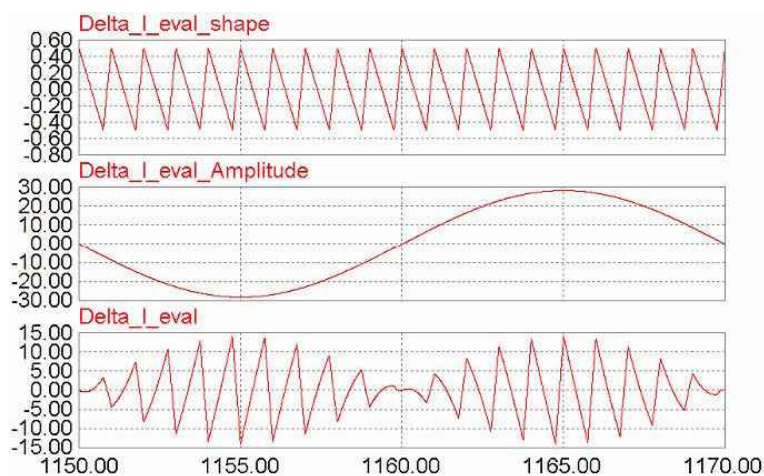


Figure 6-13.- AC Chopper output current ripple evaluation example,  $\alpha=0.75$ .

Comparison between the evaluated current ripple and the current obtained by ideal circuit simulation (switching operation) is performed. The aim of this simulation is to verify the validity of the method used to evaluate the current ripple evolution at constant duty cycle. Figure 6-14 shows the comparison result. A slight offset can be noticed between both simulated signals. This offset is due to the non-purely sinusoidal output current of the AC Chopper when working in open loop (the switched current ripple is calculated by subtraction of the inductor current and the ideal fundamental term). However, regarding the amplitude of the current ripple, the simulation results show that the evaluation method provides good results.

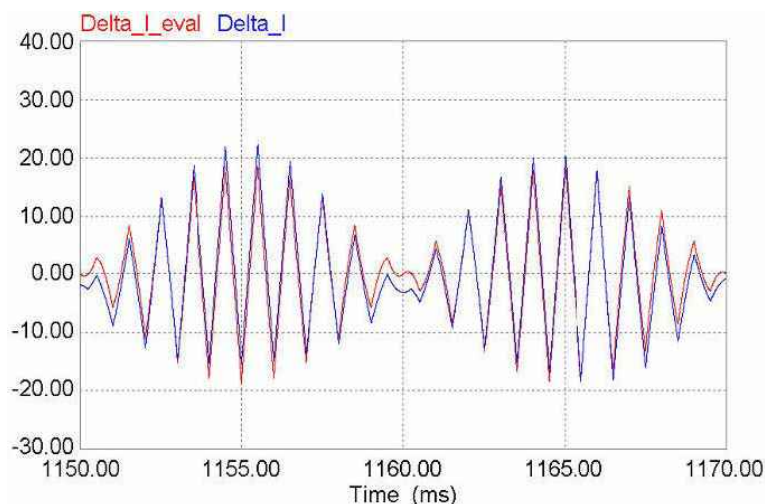


Figure 6-14.- AC Chopper output current ripple comparison (evaluation and switching operation),  $\alpha=0.5$

Nevertheless, this evaluation process considers the ideal behaviour of the AC Chopper. If the non-linear behaviour of the converter is taken into account, different maximum current ripple values are found. The modulation index sampling approach could be applied to obtain better evaluation results. However, since the AC Chopper duty cycle in steady state is constant, no big differences are found, Figure 6-15. Circuit simulation containing the non-ideal elements of the converter (input filter behaviour, dead times, semiconductor voltage drop, zero crossing detection, etc.) can provide more accurate evaluation of the inductor current ripple. The method developed here can be used as a first evaluation to perform the converter dimensioning.

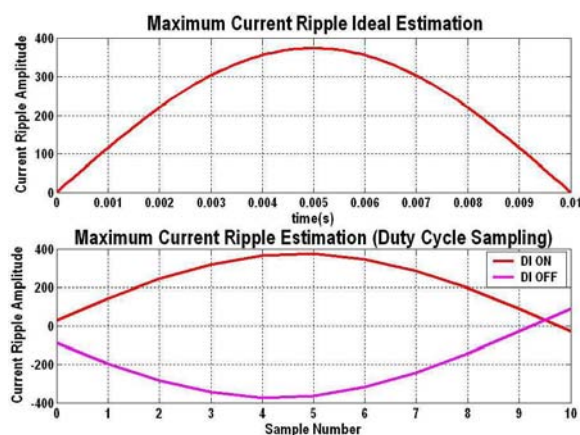


Figure 6-15.- AC Chopper maximum current ripple analytical evaluation (idealised and duty cycle sampling),  $\alpha=0.5$

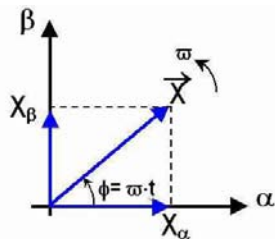
## 6.4 Conclusions

Several methods for evaluation of the inductor current ripple on different converters have been applied. It has been demonstrated that the use of the classical expression derived from DC/DC converters when low switching frequency is used leads to relevant evaluation errors. Consideration of the modulation index sampling and hold function of the modulator offer better evaluation results. However, the non-linear behaviour of the converter and the response of the closed control loop induce also errors in this evaluation method. Therefore, if accurate current ripple estimation must be obtained, the best solution is offered by the circuit simulation approach.

# Appendix 2

## $\alpha$ - $\beta$ Instantaneous Complex Phasors Representation of Single-phase Systems Using Second Order Filters. Dynamic Characteristics

The dynamic response of the single-phase system representation by means of "instantaneous complex phasors" in a stationary  $\alpha$ - $\beta$  frame, Figure 4-43, using second order filters is analysed in this appendix.



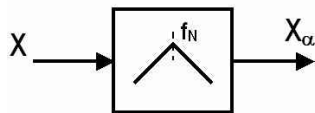
$$\vec{X} = X_{\alpha} + jX_{\beta} = X \cdot e^{j\omega \cdot t} = X \cdot (\cos(\omega \cdot t) + j \cdot \sin(\omega \cdot t)) \quad \text{Eq. 7-1}$$

$$X_{\alpha} = X \cdot \cos(\omega \cdot t) \quad \text{Eq. 7-2}$$

$$X_{\beta} = X \cdot \sin(\omega \cdot t) \quad \text{Eq. 7-3}$$

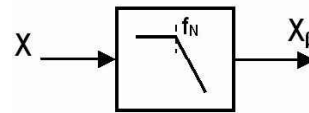
Figure 7-1.- Complex phasor representation in the stationary  $\alpha$ - $\beta$  frame

A second order band-pass filter is employed to generate the  $\alpha$  component ( $X_{\alpha}$ ) of the representation, providing unity gain (0dB) and  $0^{\circ}$  phase at the considered nominal frequency ( $\omega_N = 2 \cdot \pi \cdot f_N$ ) with respect to the signal to be represented ( $X$ ), Figure 7-2. The  $\beta$  component ( $X_{\beta}$ ) is obtained by means of a second order low-pass filter providing unity gain (0dB) and  $-90^{\circ}$  at  $\omega_N$ , Figure 7-3.



$$\frac{X_{\alpha}(s)}{X(s)} = \frac{2 \cdot \xi \cdot \omega_N \cdot s}{s^2 + 2 \cdot \xi \cdot \omega_N \cdot s + \omega_N^2}$$

Figure 7-2.-  $\alpha$  component generation filter.



$$\frac{X_{\beta}(s)}{X(s)} = \frac{2 \cdot \xi \cdot \omega_N^2}{s^2 + 2 \cdot \xi \cdot \omega_N \cdot s + \omega_N^2}$$

Figure 7-3.-  $\beta$  component generation filter.

The selection of the filters' characteristic frequency  $f_N$  to match the nominal frequency of the input signal  $X$  guarantee the steady state conditions required to obtain such representation. However, the dynamic response of the representation system is defined by the damping factor of the filters

( $\xi$ ). The time and frequency-domain characteristics of the transfer functions of the filters are analysed to derive the influence of  $\xi$  on the dynamic behaviour of the representation system.

The frequency domain characteristics of the filters are shown in Figure 7-4 and Figure 7-5. These characteristics show the higher attenuation of the input signal harmonics (at frequencies multiple of  $f_N$ ) when the damping factor  $\xi$  decreases. However, the higher the damping factor  $\xi$ , the higher the frequency band where the gain and phase of the filter stays near to the gain and phase at  $f_N$ . That is, the change of gain and phase around the characteristic frequency  $f_N$  of the filters is less abrupt when the damping ratio increases, which allows a higher tolerance to change in the nominal frequency on the input signal.

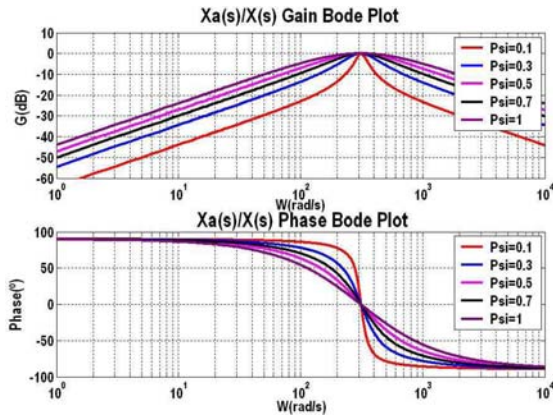


Figure 7-4.-  $X_\alpha(s)/X(s)$  bode plot vs.  $\xi$

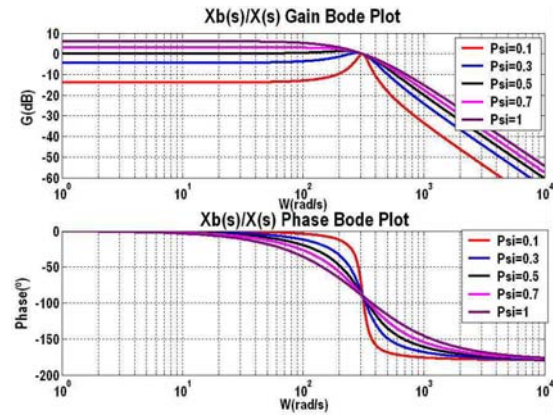


Figure 7-5.-  $X_\beta(s)/X(s)$  bode plot vs.  $\xi$

From a transient response point of view, the time evolution of the filters response is analysed when the input signal  $x(t)$  is an ideal sinus at the characteristic frequency of the filters  $f_N$ , Eq. 7-4. The transient response of the filters,  $x_\alpha(t)$  and  $x_\beta(t)$  (Eq. 7-7 and Eq. 7-9 respectively), contains an exponential term ( $e^{-\xi \cdot \omega_N \cdot t}$ ). The time constant ( $\tau=1/(\xi \cdot \omega_N)$ ) of this exponential term defines the response speed of the filter. A fast response speed of the filter requires a small time constant ( $\tau$ ) and therefore a high damping ratio ( $\xi$ ).

$$x(t) = \sin(\omega_N \cdot t) \quad \text{Eq. 7-4}$$

$$X(s) = \frac{\omega_N}{s^2 + \omega_N^2} \quad \text{Eq. 7-5}$$

$$X_\alpha(s) = \frac{2 \cdot \xi \cdot \omega_N \cdot s}{s^2 + 2 \cdot \xi \cdot \omega_N \cdot s + \omega_N^2} \cdot \frac{\omega_N}{s^2 + \omega_N^2} = \frac{-\omega_N}{s^2 + 2 \cdot \xi \cdot \omega_N \cdot s + \omega_N^2} + \frac{\omega_N}{s^2 + \omega_N^2} \quad \text{Eq. 7-6}$$

$$x_\alpha(t) = \sin(\omega_N \cdot t) - \frac{e^{-\xi \cdot \omega_N \cdot t}}{\sqrt{1-\xi^2}} \cdot \sin\left(\sqrt{1-\xi^2} \cdot \omega_N \cdot t\right) \quad \text{Eq. 7-7}$$

$$X_\beta(s) = \frac{2 \cdot \xi \cdot \omega_N^2}{s^2 + 2 \cdot \xi \cdot \omega_N \cdot s + \omega_N^2} \cdot \frac{\omega_N}{s^2 + \omega_N^2} = \frac{2 \cdot \xi \cdot \omega_N + s}{s^2 + 2 \cdot \xi \cdot \omega_N \cdot s + \omega_N^2} - \frac{s}{s^2 + \omega_N^2} \quad \text{Eq. 7-8}$$

$$x_\alpha(t) = \frac{e^{-\xi \cdot \omega_N \cdot t}}{\sqrt{1-\xi^2}} \cdot \left( 2 \cdot \xi \cdot \sin\left(\sqrt{1-\xi^2} \cdot \omega_N \cdot t\right) - \sin\left(\sqrt{1-\xi^2} \cdot \omega_N \cdot t + \phi\right) \right) e^{-\xi \cdot \omega_N \cdot t} - \cos(\omega_N \cdot t) \quad \text{Eq. 7-9}$$

$$\phi = \tan^{-1} \frac{\sqrt{1-\xi^2}}{\xi};$$



The evolution of the filters' transient responses for different damping ratios is shown in Figure 7-6 and Figure 7-7.

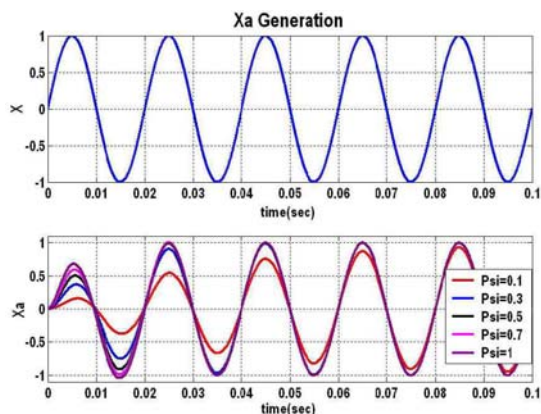


Figure 7-6.-  $x_{\alpha}(t)$  response for different  $\xi$  values

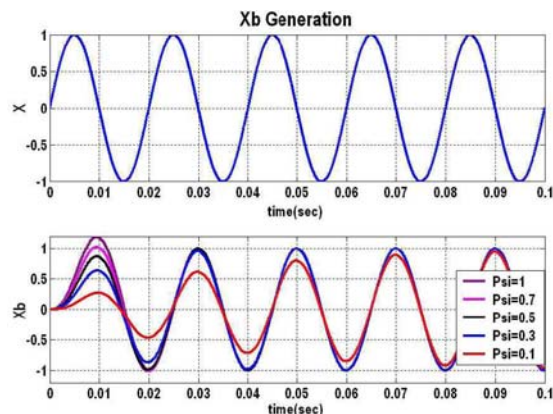


Figure 7-7.-  $x_{\beta}(t)$  response for different  $\xi$  values

Consequently, the selection of the filters' damping ratio  $\xi$  defines the dynamic characteristics of the  $X_{\alpha}$  and  $X_{\beta}$  generation system. On one hand, lowering the damping ratio of the filter  $\xi$  the attenuation of the input signal harmonics is increased. However, the response time to reach the steady state of the representation increases and the frequency band around  $f_N$  with gain close to 0dB is reduced, which implies that the frequency change in the input signal is more critical. On the other hand, the increase of  $\xi$  provides less abrupt phase changes around  $f_N$ . A trade-off in the selection of the damping ratio of the filter must be achieved considering the input signal characteristics (i.e. harmonic content, frequency change) and the representation dynamic performance required by the application.

# Appendix 3

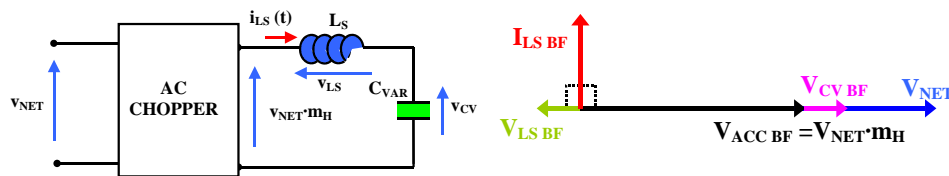
## Hysteresis Controller for the Step-down PWM AC Chopper

### 8.1 Introduction

Due to the highly non-linear behaviour of the PWM AC Chopper, a non-linear control system could be best suited for its correct operation. Here, the hysteresis controller is applied to a step-down PWM AC Chopper in reactive power compensation. Then, the operation of the hysteresis controlled at fixed switching frequency is derived.

### 8.2 Generic Hysteresis Controller for the Step-down PWM AC Chopper

To use a hysteresis controller and to obtain stable operation of the system, a first order relationship between the control variable and the variable to be controlled must exist.



$$V_{NET} = V_{NET} \cdot \sin(\omega \cdot t);$$

$$i_{LS} = i_{LSBF} + i_{LSHF} = I_{LS} \cdot \cos(\omega \cdot t) + i_{LSHF};$$

$$V_{LS} = V_{LSBF} + V_{LSHF} = -I_{LS} \cdot L_s \cdot \omega \cdot \sin(\omega \cdot t) + V_{LSHF};$$

$$V_{CV} = V_{CVBF} + V_{CVHF} = \frac{I_{LS}}{C_{VAR} \cdot \omega} \cdot \sin(\omega \cdot t) + V_{CVHF};$$

$$V_{ACCBF} = V_{NET} \cdot m_H \cdot \sin(\omega \cdot t);$$

$$I_{LSBF} = \frac{V_{NET} \cdot m_H}{Z_{LC}}; \quad m_H = \frac{V_{ACCRMS}}{V_{NETRMS}};$$

$$Z_{LC} = \frac{1 - L_s \cdot C_{VAR} \cdot \omega^2}{C_{VAR} \cdot \omega};$$

$$V_{CVHF} \approx 0;$$

$$V_{LSHF}(u_s) = V_{ACC}(u_s) - V_{LSBF} - V_{CVBF};$$

Figure 8-1.- PWM AC Chopper high frequency expressions derived from the low frequency steady state

For the step-down PWM AC Chopper in reactive power compensation, Figure 8-1, the considered control variable is the state of the switches defined by the control signal  $u_s$ , while the controlled variable is the load current ( $i_{LS}$ ). To verify whether a first order relationship exists between  $u_s$  and  $i_{LS}$ , the  $di_{LS}/dt$  sign must be analysed. The relationship exists if the  $di_{LS}/dt$  polarity changes only with the control signal  $u_s$  changes and not due to the change of other variables of the system.

Considering the stable operation of the system as reactive power compensator, vector diagram of Figure 8-1, the representative equations for each switch state can be obtained. The system variables are represented by a low frequency term ( $x_{BF}$ ) and a high frequency term ( $x_{HF}$ ). Analysing the high frequency term of the voltage applied to the inductor  $L_S$  ( $v_{LSHF}$ ), Table 8-1, the  $di_{LS}/dt$  expression for each switches state can be derived, Table 8-2.

$V_{NET}(t) > 0, u_s=1$ (Active Phase)	$V_{NET}(t) > 0, u_s=0$ (Free wheeling Phase)
$V_{NET} = V_{NET} \cdot \sin(\omega \cdot t); \quad \sin(\omega \cdot t) > 0; \quad \omega \cdot t \in [0, \pi];$ $i_{LSBF} = \frac{V_{NET} \cdot m_H}{Z_{LC}} \cdot \cos(\omega \cdot t);$	$V_{LSBF} = -\frac{V_{NET} \cdot m_H}{Z_{LC}} \cdot L_S \cdot \omega \cdot \sin(\omega \cdot t);$ $V_{CVBF} = \frac{V_{NET} \cdot m_H}{Z_{LC}} \cdot \frac{1}{C_{VAR} \cdot \omega} \cdot \sin(\omega \cdot t);$
$V_{ACC}(u_s) = V_{ACC}(1) = V_{NET} = V_{NET} \cdot \sin(\omega \cdot t);$ $V_{LSHF}(u_s) = V_{ACC}(u_s) - V_{LSBF} - V_{CVBF};$ $V_{LSHF}(1) = V_{NET} \cdot \sin(\omega \cdot t) \cdot (1 - m_H);$	$V_{ACC}(u_s) = V_{ACC}(0) = 0;$ $V_{LSHF}(u_s) = V_{ACC}(u_s) - V_{LSBF} - V_{CVBF};$ $V_{LSHF}(0) = -V_{NET} \cdot \sin(\omega \cdot t) \cdot m_H;$
$V_{NET}(t) < 0, u_s=1$ (Active Phase)	$V_{NET}(t) < 0, u_s=0$ (Free wheeling Phase)
$V_{NET} = -V_{NET} \cdot \sin(\omega \cdot t); \quad \sin(\omega \cdot t) > 0; \quad \omega \cdot t \in [0, \pi];$ $i_{LSBF} = \frac{-V_{NET} \cdot m_H}{Z_{LC}} \cdot \cos(\omega \cdot t);$	$V_{LSBF} = \frac{V_{NET} \cdot m_H}{Z_{LC}} \cdot L_S \cdot \omega \cdot \sin(\omega \cdot t);$ $V_{CVBF} = -\frac{V_{NET} \cdot m_H}{Z_{LC}} \cdot \frac{1}{C_{VAR} \cdot \omega} \cdot \sin(\omega \cdot t);$
$V_{ACC}(u_s) = V_{ACC}(1) = V_{NET} = -V_{NET} \cdot \sin(\omega \cdot t);$ $V_{LSHF}(u_s) = V_{ACC}(u_s) - V_{LSBF} - V_{CVBF};$ $V_{LSHF}(1) = -V_{NET} \cdot \sin(\omega \cdot t) \cdot (1 - m_H);$	$V_{ACC}(u_s) = V_{ACC}(0) = 0;$ $V_{LSHF}(u_s) = V_{ACC}(u_s) - V_{LSBF} - V_{CVBF};$ $V_{LSHF}(0) = V_{NET} \cdot \sin(\omega \cdot t) \cdot m_H;$

Table 8-1.- Switching states for the AC Chopper. Load inductor voltage  $v_{LSHF}$  evaluation

The low frequency relationship between the input voltage  $V_{NET}$  and the output voltage  $V_{ACC}$  of the step-down PWM AC Chopper is defined by the term " $m_H$ "  $\in [0,1]$ , which is equivalent to the duty cycle in PWM operation. The value of  $m_H$  depends on the desired current value  $I_{LS}$  (reactive power reference) and the impedance value of the load  $Z_{LC}$  for a given input voltage value  $V_{NET}$ .

The expressions for the high frequency value of the output inductor ( $v_{LS\ HF}$ ) can be derived from the system low frequency expressions as show in Table 8-1. The high frequency voltage term of the output capacitor ( $v_{CV\ HF}$ ) is neglected due to the big capacitor value  $C_{VAR}$  required to provide the reactive power compensation function. The states of the switching cells are defined by the control signal  $u_S$  and by the input voltage  $V_{NET}$  polarity. For the switching cell in switching operation (the adjacent switching cell being short-circuited), when  $u_S=1$ , the upper switch of the switching cell is in ON state and the lower switch is in OFF state, which corresponds to an active phase where the input voltage is applied to the load. Respectively, when  $u_S=0$ , the upper switch is in OFF state and the lower switch is in ON state, which corresponds to a freewheeling phase where the load is short-circuited.

	$u_S=1$ (Active Phase)	$u_S=0$ (Free wheeling Phase)
	$\Delta I_{LS} = \frac{v_{LSHF}(u_S = 1)}{L_S} \cdot T_{ON};$	$\nabla I_{LS} = \frac{v_{LSHF}(u_S = 0)}{L_S} \cdot T_{OFF};$
$V_{NET} > 0$	$\Delta I_{LS} = \frac{V_{NET} \cdot \sin(\omega \cdot t) \cdot (1 - m_H)}{L_S} \cdot T_{ON}; \Delta I_{LS} > 0;$	$\nabla I_{LS} = \frac{-V_{NET} \cdot \sin(\omega \cdot t) \cdot m_H}{L_S} \cdot T_{OFF}; \nabla I_{LS} < 0;$
$V_{NET} < 0$	$\Delta I_{LS} = \frac{-V_{NET} \cdot \sin(\omega \cdot t) \cdot (1 - m_H)}{L_S} \cdot T_{ON}; \Delta I_{LS} < 0;$	$\nabla I_{LS} = \frac{V_{NET} \cdot \sin(\omega \cdot t) \cdot m_H}{L_S} \cdot T_{OFF}; \nabla I_{LS} > 0;$

Table 8-2.-  $di_{LS}/dt$  polarity according to the switching states of the step-down PWM AC Chopper.

The  $v_{LS\ HF}$  expressions of Table 8-1 show that the polarity of this voltage does not change on each switching state, that is, the  $di_{LS}/dt$  polarity is constant on each switching state. However, for the same control signal value  $u_S$ , the  $di_{LS}/dt$  polarity changes depending on the input voltage polarity  $V_{NET}$ , Table 8-2. From these expressions, a first order relationship between the current load  $I_{LS}$  and the control signal  $u_S$  is identified. However, the relationships change depending on the input voltage polarity. This fact means that a classical hysteresis band controller cannot be directly used for this application. Nevertheless, it is possible to complement the behaviour of the classical hysteresis band controller adding a logic circuit that takes into account the input voltage polarity, as shown in the next paragraphs.

The classical characteristic of a hysteresis controller and its idealised implementation is shown in Figure 8-2. The control signal "u" changes when the error  $\epsilon_x$  attains the hysteresis band value H (respectively -H). The control signals will not change again until the error  $\epsilon_x$  reaches the opposed hysteresis band value -H (respectively H).

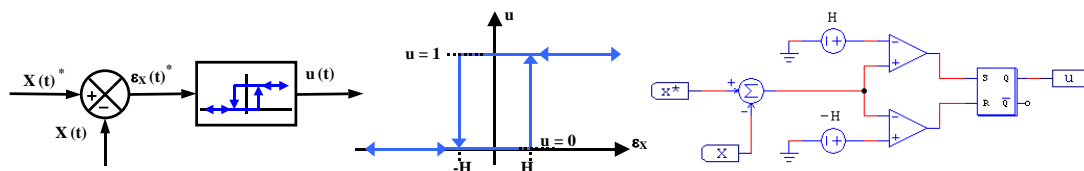


Figure 8-2.- Classical hysteresis band controller.

This characteristic can be directly applied to the PWM AC Chopper when the input voltage  $V_{NET}$  is positive. However, the value of the control signal "u" required when the input voltage  $V_{NET}$  changes to negative is just the opposite than the one provided by the classical hysteresis controller. Therefore, the PWM AC Chopper hysteresis controller is obtained using the classical hysteresis controller and modifying the output control signal "u" by means of a logical function according to the input voltage polarity. Table 8-3 is employed to obtain the relationship between

the gate signals of the step-down PWM AC Chopper, the hysteresis controller input  $\epsilon_x$  and the input voltage polarity.

Sign $V_E$	Error $\epsilon_x$	$u$	$di_{LS}/dt$	$u_s$	$U_{T1}$	$U_{T1c}$	$U_{T2}$	$U_{T2c}$
> 0	> H	1	> 0	1	1	0	1	1
> 0	< -H	0	< 0	0	0	1	1	1
< 0	> H	1	> 0	0	1	1	0	1
< 0	< -H	0	< 0	1	1	1	1	0

Table 8-3.- Hysteresis controller output values for a Buck AC Chopper (Input voltage sign dependent).

When the error valued  $\epsilon_x$  is positive (equal to H), the applied sequence must cause the increase of the load current ( $di_{LS}/dt > 0$ ). Respectively, when the error is negative (equal to -H), the new sequence must generate the reduction of the load current ( $di_{LS}/dt < 0$ ). The logic relationship depending on the input voltage polarity between the intermediate hysteresis controller output ( $u$ ) and the PWM AC Chopper control signal ( $u_s$ ) can be obtained by means of a XNOR logic gate, Figure 8-3. Then, the control signal  $u_s$  is used to drive the switching cells semiconductors during the switching mode operation phase, ( $u_s = T_X$  and  $/u_s = T_{XC}$  integrating a dead time). The input voltage polarity defines the short-circuit operation of each switching cell.

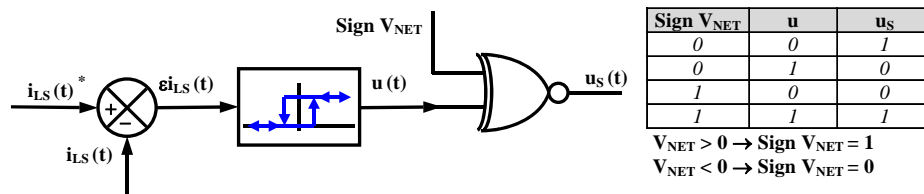


Figure 8-3.- Modified hysteresis controller for the step-down PWM AC Chopper.

Comment: Another solution, instead of using the XNOR function, could be the use of the signal ( $u$ ) to drive T1 and T2c, while the sign of the input voltage indicates when each switching cell must work in short-circuit operation.

The response of the single-phase step-down PWM AC Chopper using the proposed hysteresis controller is shown in Figure 8-4 and Figure 8-5 when no LC input filter is considered (an ideal sinusoidal voltage source is considered). It can be seen how the control response time is almost instantaneous, providing the well-known high-speed performance of hysteresis controllers.

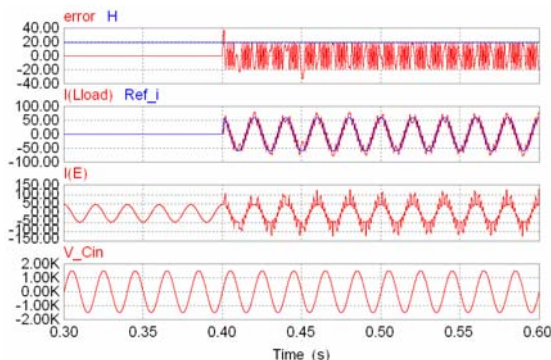


Figure 8-4.- Ideal hysteresis controller closed loop operation (step change in the current reference)

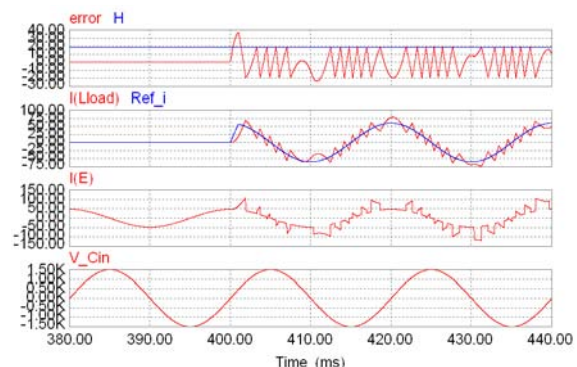


Figure 8-5.- Zoom of the ideal hysteresis controller closed loop operation

The error signal is normally limited to be inside the hysteresis band (between +H and -H value). However, in the simulation here presented the error signal exceeds the hysteresis band in some

points. This effect is due to the freewheeling sequence generated around the zero crossing of the input voltage to provide safe switching of the semiconductors.

When considering the LC input filter of the PWM AC Chopper, Figure 8-6 and Figure 8-7, the output current is still well regulated even if the input voltage is highly excited due to hysteresis controller fast response time. The PWM AC Chopper input voltage ( $V_{CIN}$ ) as well as the input filter input current ( $I_E$ ) contain harmonics at the resonance frequency of the input filter. This behaviour is an important drawback of the hysteresis controller. If the hysteresis controller is to be used, the use of a well-damped input filter (passively or actively) is compulsory to allow the non-polluting and stable operation of the converter.

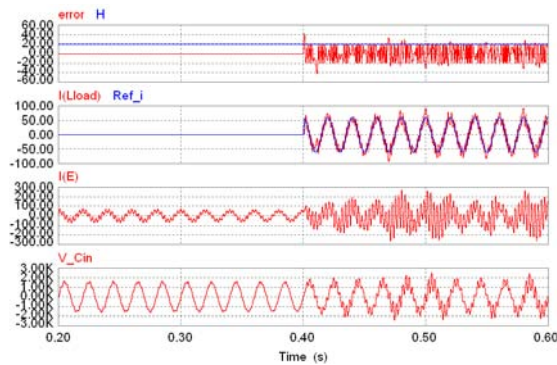


Figure 8-6.- Hysteresis controller closed loop operation, (Un-damped input filter)

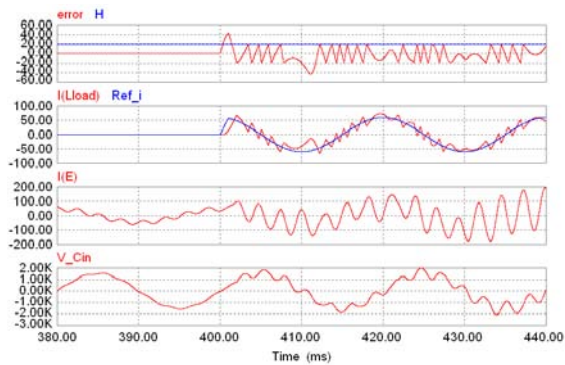


Figure 8-7.- Zoom of the hysteresis controller closed loop operation, (Un-damped input filter)

When the input filter is well damped, Figure 8-8 and Figure 8-9, here increasing the parasitic resistor and changing the resonance frequency of the input filter components (higher capacitor), the hysteresis controller response is acceptable.

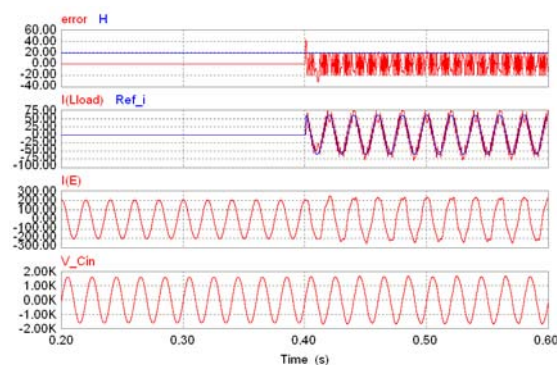


Figure 8-8.- Hysteresis controller closed loop operation, (Damped input filter)

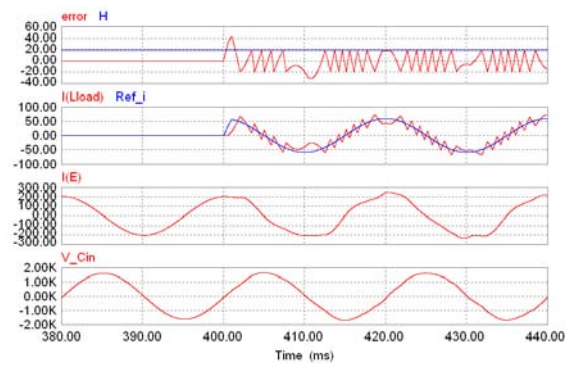


Figure 8-9.- Zoom of the hysteresis controller closed loop operation, (Damped input filter)

### 8.3 Modification of the Generic Hysteresis Controller to Obtain Fixed Switching Frequency operation

To make the hysteresis controller operate at fixed switching frequency, the hysteresis band has to be modulated over the time to take into account the change of the working conditions of the converter (input voltage, output current). The method proposed here consists of using the current ripple expression of the PWM AC Chopper when operates at fixed switching frequency ( $\Delta I = f(V_{NET}, t, I_{LS}^*, f_{SW})$ , see appendix 1) to derive the hysteresis band evolution ( $H = f(V_E, t, I_{LS}^*, f_{SW})$ ).

The hysteresis band has to simply follow the expression of the current ripple. The problem now consists of how to relate the hysteresis operation to the PWM operation, ( $H = f(t, \alpha)$ ).

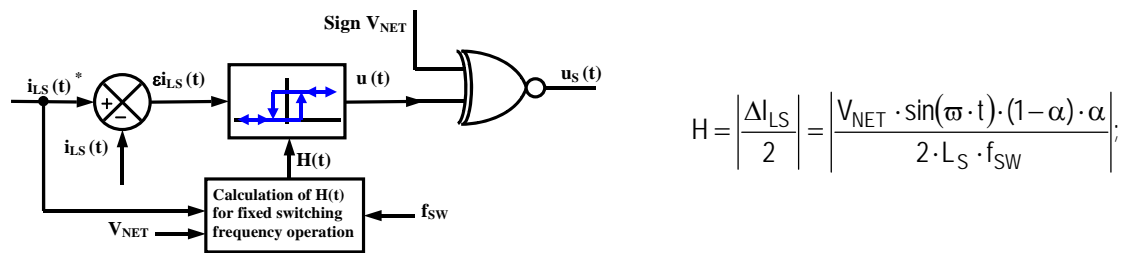


Figure 8-10.- Modified hysteresis controller to obtain fixed switching frequency operation of the step-down PWM AC Chopper

To obtain the evolution of the hysteresis band  $H(t)$ , Figure 8-10, the equivalent duty cycle value  $\alpha$  for the required reactive power compensation value must be calculated. To calculate  $\alpha$ , the relationship between the RMS value of the fundamental output current reference  $I_{LS}^*$  and input voltage  $V_{NET}$  must be measured. Also, the output load impedance  $Z_{LC}$  must be known. The calculation of  $\alpha$  is equivalent to the feed forward technique ( $\alpha_{ST}$ ) used in the linear regulation proposed in Chapter 4 (PI + feed forward).

$$I_{LS} = \frac{V_{ACC}}{Z_{LC}} = \frac{V_{NET} \cdot \alpha}{Z_{LC}}; \quad Z_{LC} = \frac{1 - L_S \cdot C_{VAR} \cdot \omega^2}{C_{VAR} \cdot \omega};$$

$$\alpha = \alpha_{ST} = \frac{|I_{LSREF}| \cdot Z_{LC}}{|V_{NET}|} = \frac{|I_{LSREF}| \cdot (1 - L_S \cdot C_{VAR} \cdot \omega^2)}{|V_{NET}| \cdot C_{VAR} \cdot \omega};$$

Only the sinusoidal (absolute value) evolution of  $H$  must be considered. As a first approximation, the amplitude and phase of the input voltage  $V_{NET}$  and the value of the output inductor  $L_S$  can be considered constant. Finally, the desired switching frequency  $f_{SW}$  must be selected.

To check the feasibility of the fixed switching frequency operation with the proposed hysteresis controller, several simulations are performed. Firstly, an idealised simulation was performed not taking into account the required input filter of the PWM AC Chopper. The simulation results are shown in Figure 8-11.

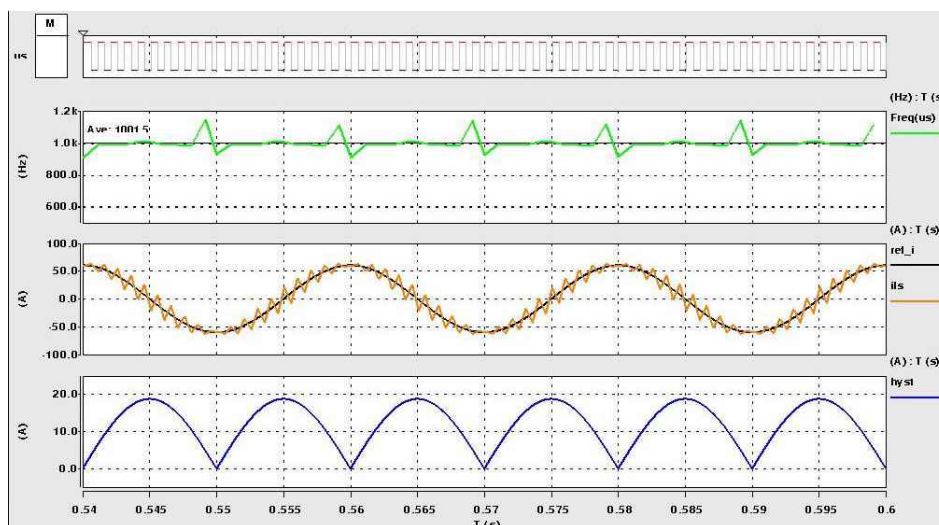


Figure 8-11.- Fixed switching frequency Hysteresis controller (ideal input voltage)

The simulation results show, as expected, an output current waveform very similar to the waveform obtained in PWM operation. The switching frequency varies slightly around the defined switching frequency ( $f_{sw} = 1\text{kHz}$ ), showing more important changes near the zero crossing point of the input voltage.

However, when introducing the input filter, Figure 8-12, again the excitation of the input filter is the main problem. The hysteresis controller behaviour excites the input filter, which induces distortion over the input voltage and consequently over the evolution of the hysteresis band. Although the load current evolution is well controlled (fundamental term and switching current ripple), the switching frequency change is increased due to the distorted evolution of the input voltage.

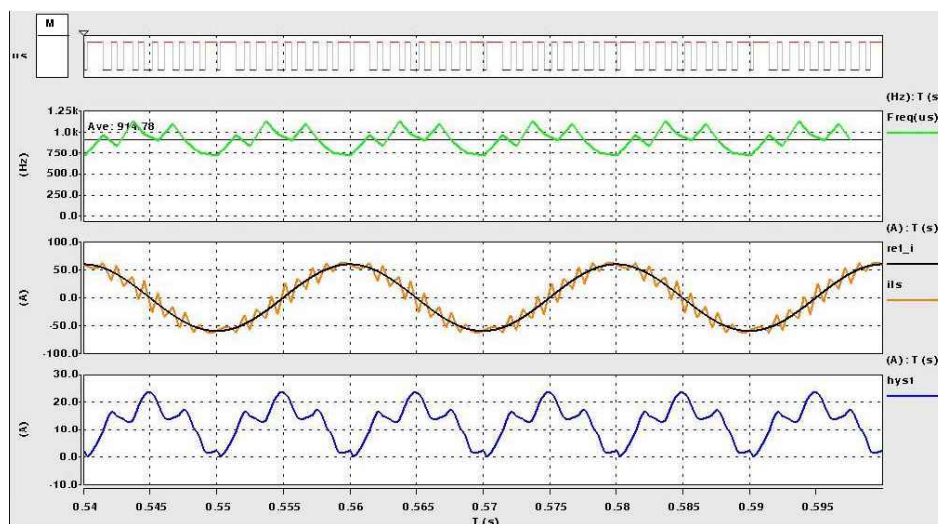


Figure 8-12.- Fixed switching frequency Hysteresis controller (input filter excitation)

## 8.4 Conclusion

The basic principles to use a non-linear hysteresis controller for the single-phase step-down PWM AC Chopper operating in reactive power compensation are presented in this appendix. Also, the controller modification to obtain almost fixed switching frequency operation has been derived. The main advantage of such a controller is the fast response time on the control system. However, the excitation of the input filter due to the high-speed response of such a controller arises, which leads to high amplitude low frequency current harmonics injected into the network. A highly damped input filter or additional control strategies to damp the input filter would be required to obtain a reasonable operation of the system.



# Appendix 4

## AC Chopper PWM pattern generation, freewheeling sequence at the input voltage zero crossing

The modified PWM pattern generation for PWM AC Choppers to guarantee the safe operation of the semiconductors is presented. The application of a freewheeling phase during the zero crossing of the input voltage  $V_{CF}$  is given as a representative example of the proposed strategy.

The introduction of the freewheeling region at the input voltage zero crossing requires the use of specific sequences that are generated according to the value of the PWM carrier and the duty cycle reference. First of all, an ideal PWM signal ( $PWM_{IDE}$ ) is generated by comparison of a PWM Carrier (saw-tooth or triangular waveform) with the duty cycle reference (only  $\alpha_{ST}$ , the PI generated reference is omitted, see section 4.3.1.2.1). The reference maximum and minimum values have to be limited to assure the correct pulse width lengths generation ( $T_{ON(MIN)}$  and  $T_{OFF(MIN)}$ ), Figure 9-1, Figure 9-2. Then, the dead time  $T_D$  is added, which is selected considering the switching times of the IGCTs as well as the influence of the clamp circuit on the switching transients.

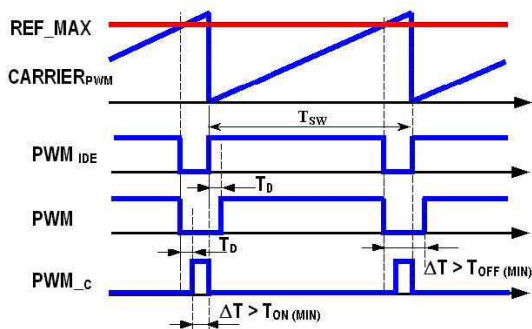


Figure 9-1.- PWM generation ( $\alpha_{MAX}$ )

$$\alpha_{MAX} = 1 - \frac{T_{ON(MIN)} + T_D}{T_{SW}}$$

$$\alpha_{MIN} = \frac{T_{ON(MIN)} + T_D}{T_{SW}}$$

$$T_{OFF(MIN)} = T_{ON(MIN)} + 2 \cdot T_D$$

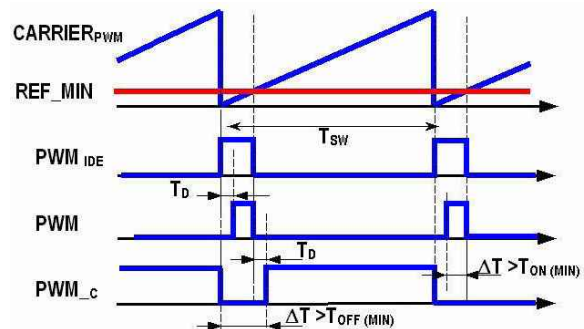


Figure 9-2.- PWM generation ( $\alpha_{MIN}$ )

$\alpha_{MAX}$  = Maximum duty cycle  $\rightarrow$  REF\_MAX

$\alpha_{MIN}$  = Minimum duty cycle  $\rightarrow$  REF\_MIN

$T_{ON(MIN)} = 10\mu\text{s}$ ;  $T_{ON(MIN)} = 10\mu\text{s}$ ; (Defined in the IGCT datasheet)

$T_D$  = Dead time;  $T_{SW}$  = Switching period;

The resulting signals (PWM and PWM\_C) are used to generate the final switching signals for the semiconductors according to the polarity of the input voltage. However, they are only used as

information during the freewheeling sequence, where the switching pattern is adapted to provide safe switching operation.

The adopted switching strategy considering the freewheeling sequence is explained here for the case where the input voltage value is positive and then becomes negative. The equations and sequences required for the generation of the switching signals (T1, T1c, T2, T2c, 1=On state, 0=Off state) during the freewheeling sequence are shown in Figure 9-3.

The duration of the freewheeling phase around the input voltage zero crossing region is defined by the comparison of the input voltage  $V_{CF}$  with a freewheeling level (FW Level). Also, to consider the inaccuracy introduced by the voltage measurement and to avoid the on-state operation of the four semiconductors at the same time (short circuit of the input voltage), two zero displacement levels are defined,  $0^+$  and  $0^-$ . On one hand, the  $Sign_{\oplus}$  signal is obtained by comparison between  $V_{CF}$  and the  $0^+$  level, indicating the region where the input voltage is assured to be positive. On the other hand, the  $Sign_{-}$  signal, obtained by comparison between  $V_{CF}$  and the  $0^-$  level, defines the region where the input voltage measurement guarantees the accurate negative polarity identification. Consequently, around the input voltage zero crossing, there is a region defined by the comparison levels  $0^+$  and  $0^-$  ( $Sign_{\oplus}$  and  $Sign_{-}$  are 0) where the polarity of the input voltage is not important because only a freewheeling sequence has to be generated.

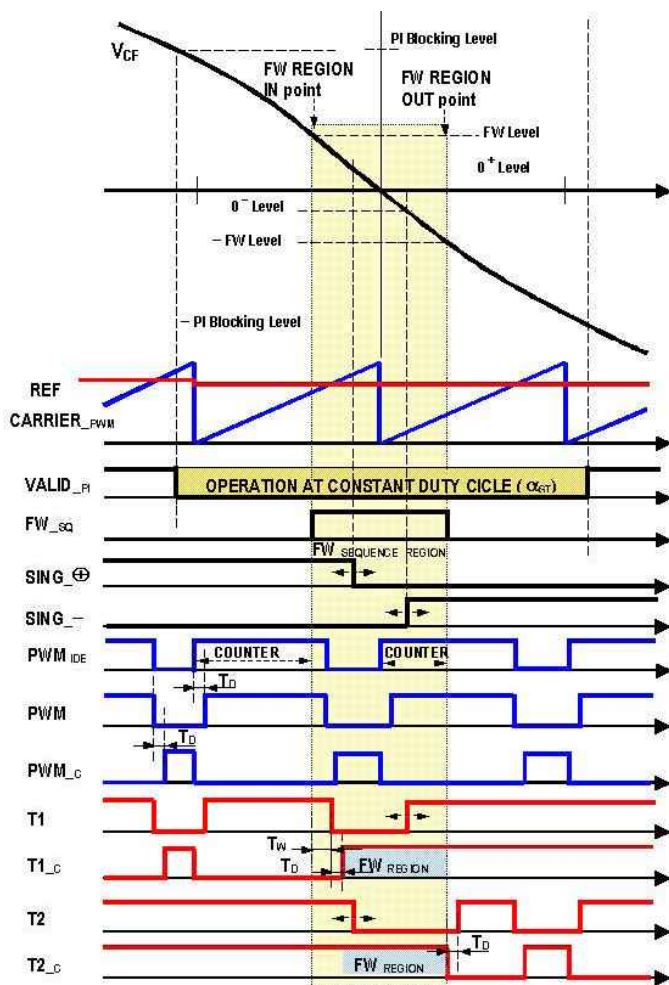


Figure 9-3.- PWM AC Chopper semiconductors' gate signals generation, (left). Freewheeling sequence generation for input voltage zero crossing from  $V_{CF} > 0$  to  $V_{CF} < 0$ , (right).

Signals generation at the IN point of the FW sequence:  $\hat{\uparrow}(FW_{sq} \cdot Sign_{\oplus})$

$$T2 = Sign_{\oplus} \quad T2C = 1$$

IN POINT	SEQUENCE					
	[PWM, PWMc]	[T1, T1c]	$\Delta t$	[T1, T1c]	$\Delta t$	[T1, T1c]
[0,0]	[0,0]	$T_D$	[0,1]	-	-	
[1,0]	If ( COUNTER < $T_D + T_W$ )					
	[1,0]	$T_W$	[0,0]	$T_D$	[0,1]	
[0,1]	If ( COUNTER > $T_D + T_W$ )					
	[0,0]	$T_D$	[0,1]	-	-	

Signals generation at the input voltage change:  $\hat{\uparrow}(Sign_{-})$

$$T1 = 1 \quad T1c = 1$$

$$T2 = 0 \quad T2c = 1$$

Signals generation at the OUT point of the FW Sequence:  $\hat{\downarrow}(FW_{sq} \cdot Sign_{-})$

$$T1 = 1 \quad T1c = 1$$

OUT POINT	SEQUENCE			
	[PWM, PWMc]	[T2, T2c]	$\Delta t$	[T2, T2c]
[0,0]	[0,0]	$T_D$	[PWM, PWMc]	
[1,0]	If ( $\alpha_T \cdot COUNTER > T_D + T_W$ )			
	[0,0]	$T_D$	[PWM, PWMc]	
[0,1]	If ( $\alpha_T \cdot COUNTER < T_D + T_W$ )			
	[0,0]	$T_D + T_W$	[PWM, PWMc]	

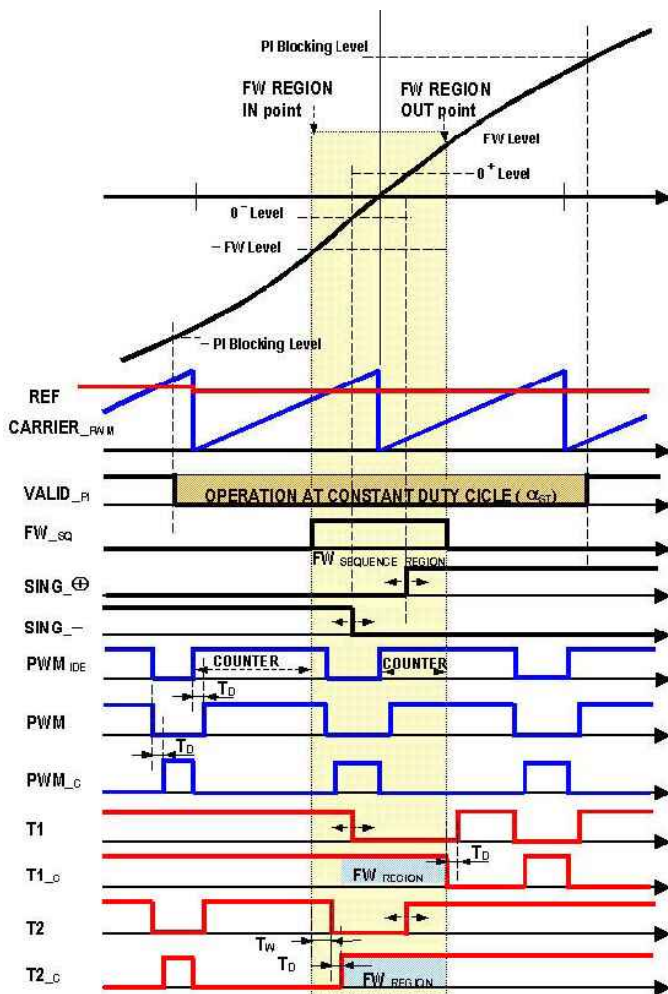
Signal generation before and after the Freewheeling Sequence

$$T1 = PWM + Sign_{-} \quad T1c = PWMc + Sign_{-}$$

$$T2 = PWM + Sign_{\oplus} \quad T2c = PWMc + Sign_{\oplus}$$

$T_D$ =Dead Time;  $T_W$ =Minimum pulse width time;

The signals  $Sign_{\oplus}$  and  $Sign_{-}$  are employed to generate the transitions of T1 and T2 during the freewheeling sequence. Therefore, the  $0^{+}$  and  $0^{-}$  levels have to be high enough to guarantee that T1 and T2 are not switched at the same time. A time interval where  $Sign_{\oplus}$  and  $Sign_{-}$  are both 0 must be guaranteed. Obviously, the FW level has to be higher than the polarity levels  $0^{+}$  and  $0^{-}$ , which means that the freewheeling sequence must be launched according to the of input voltage polarity and before the real zero crossing point of the input voltage has been reached.



Signals generation at the IN point of the FW sequence:  $\uparrow(FW_{SQ}, Sign_{-})$

T1=  $Sign_{-}$                       T1C= 1

IN POINT	SEQUENCE					
	[PWM,PWMC]	[T2,T2c]	$\Delta t$	[T2,T2c]	$\Delta t$	[T2,T2c]
[0,0]	[0,0]	$T_D$	[0,1]	-	-	-
[1,0]	If ( COUNTER < $T_D + T_W$ )					
	[1,0]	$T_W$	[0,0]	$T_D$	[0,1]	-
[1,0]	If ( COUNTER > $T_D + T_W$ )					
	[0,0]	$T_D$	[0,1]	-	-	-
[0,1]	[0,1]	-	-	-	-	-

Signals generation at the input voltage change:  $\uparrow(Sign_{\oplus})$

T1= 0                                      T1C= 1

T2= 1                                      T2C= 1

Signals generation at the OUT point of the FW Sequence:  $\downarrow(FW_{SQ}, Sign_{\oplus})$

T2= 1                                      T2C= 1

OUT POINT	SEQUENCE			
	[PWM,PWMC]	[T1,T1c]	$\Delta t$	[T1,T1c]
[0,0]	[0,0]	$T_D$	[PWM,PWMC]	-
[1,0]	If ( $\alpha_T - COUNTER > T_D + T_W$ )			
	[0,0]	$T_D$	[PWM,PWMC]	-
[1,0]	If ( $\alpha_T - COUNTER < T_D + T_W$ )			
	[0,0]	$T_D + T_W$	[PWM,PWMC]	-
[0,1]	[PWM,PWMC]	-	-	-

Signal generation before and after the Freewheeling Sequence

T1= $PWM + Sign_{-}$                       T1C= $PWMC + Sign_{-}$

T2= $PWM + Sign_{\oplus}$                       T2C= $PWMC + Sign_{\oplus}$

$T_D$ =Dead Time;  $T_W$ =Minimum pulse width time;

Figure 9-4.- PWM AC Chopper semiconductors' gate signals generation, (left). Freewheeling sequence generation for input voltage zero crossing from  $V_{CF}<0$  to  $V_{CF}>0$ , (right).

Note: Around the input voltage zero crossing, the duty cycle reference is kept constant. Only the static duty cycle value ( $\alpha_{ST}$ ) is used. The PI controller output value is ignored because it may lead to instability of the closed loop regulation (PI Blocking level).

During the freewheeling sequence, three successive switching transitions are generated. At the beginning of the sequence (rising edge on the  $FW_{SQ}$  signal,  $\uparrow FW_{SQ}$ ), the state of the PWM and  $PWMC$  signals and the PWM carrier (COUNTER) are checked, generating a switching sequence that respects the switching times ( $T_D$  and  $T_W$ ). Once this first phase is finished, the second is started providing the safe freewheeling path, ( $T1C=1$ ,  $T1C=2$ ). The third transition is activated by a falling edge on the  $FW_{SQ}$  signal ( $\downarrow FW_{SQ}$ ), which represents the end of the freewheeling sequence. In this phase, the gating signals are generated in a similar way as they are generated at the beginning of the FW sequence. The signals PWM and  $PWMC$ , the carrier COUNTER and

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the duty cycle value  $\alpha_{ST}$  are checked resulting in the generation of the suitable safe switching transition, completing the freewheeling sequence. Once the freewheeling sequence is finished, again the PWM and PWM<sub>C</sub> signals are employed to generate the gating signals (T1, T1<sub>C</sub>, T2, T2<sub>C</sub>) according to the polarity of the input voltage, (Sign<sub>⊕</sub> and Sign<sub>−</sub> signals).

Similarly, the equations and sequences when the input voltage value is negative and changes to a positive value are shown in Figure 9-4. Note that in this figure the PWM carrier is synchronised with the zero crossing of the input voltage. However, this situation is not easily achieved due to the uncertainties in detecting the voltage zero crossing. The switching patterns are defined taking into account the fact that the carrier is not synchronised with the zero crossings of the input voltage.