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Par
Loreine MAKKI

Differential Mode and Common Mode Modelling of Pulse Transformers for Gate-Driver Applications

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TABLE OF CONTENTS

GLOSSARY 5
ACKNOWLEDGMENTS 7
DEDICATION 10
RESUME EN FRANÇAIS 11
GENERAL INTRODUCTION 15
CHAPTER I: STATE-OF-THE-ART 18
A. POWER CONVERSION SYSTEMS' STRUCTURE 18
A.1 OVERVIEW 19
A.1.1 Power Conversion System Background 19
A.1.2 Switched-Mode Converters 20
A.1.3 Fundamentals of DC-AC Converters 21
A.2 POWER SEMICONDUCTOR DEVICES 22
A.2.1 State-of-the-Art: Power Semiconductors 22
A.2.2 Innovations in WBG Power Devices 23
A.2.2.1 SiC MOSFETs 25
B. GATE DRIVER TOPOLOGIES 27
B.1 FUNCTIONAL SPECIFICATIONS 27
B.2 GALVANIC ISOLATION REQUIREMENT 29
B.3 PLANAR TECHNOLOGY 31
B.3.1 Galvanic Isolation: Pulse Planar Transformers 32
B.3.2 Dielectric Material 33
C. ELECTROMAGNETIC COMPATIBILITY COMPLIANCE 34
C.1 INTERPRETATION OF EMC, EMI, EME AND EMS 34
C.2 CATEGORIZATION OF EMI IN POWER CONVERTERS 35
C.2.1 Conducted Signals in Electrical Circuits 37
C.2.1.1 Differential Mode Noise 37
C.2.1.2 Common Mode Noise 37
C.3 EMC CHALLENGE: PULSE TRANSFORMERS IN GATE DRIVERS 38
C.4 STANDARDS AND REGULATIONS 39
C.4.1 PCB Optimal Assembly 39
D. CM NOISE REDUCTION TECHNIQUES IN SMPS 41
D.1 OVERVIEW 41
D.2 FARADAY SHIELDING INSERTION MECHANISMS 42
D.2.1 Convenient Shielding Designs 42
D.2.1.1 Single or multi-Shield 42
D.2.1.2 Novel Shielding Designs 43
D.3 NUMERICAL ANALYSIS 45
E. CONCLUSIONS 46
CHAPTER II: NUMERICAL ANALYSIS APPROACH 47
A. EMC MODELLING 47
A.1 STATE-OF-THE-ART 47
A.1.1 Choke Modelling 48
A.1.1.1 Physical Model 48
A.1.1.2 Behavioral Model 48
A.1.2 Multiconductor Cable Modelling 48
A.1.3 Motor Modeling 49

A.1.4 HF Capacitor and Resistor Models *49*
A.1.5 PCB and Interconnects *49*
A.1.6 Power Semiconductor Models *50*
A.2 PARASITIC ANALYSIS FUNDAMENTALS 50
A.3 ELECTROMAGNETIC FORMULATION 51

B. PARASITIC EXTRACTION TOOL 52

B.1 ANSYS Q3D EXTRACTOR 52
B.2 FEM NUMERICAL ANALYSIS 53
B.3 PARASITIC CAPACITANCE COMPUTATION 54

C. ARTIFICIAL ANALYSIS 56

C.1 GEOMETRIC MODELLING 56
C.1.1 Computer-Aided Design *57*
C.2 AUTOMATED DESIGN SCHEME 58
C.2.1 Data Exchange Files *58*
C.2.2 AnsTranslator *59*
C.2.3 Generic Design Blueprint *59*

D. CASE STUDY: POWER TRANSFORMER ANALYSIS 61

D.1 ALTIUM DESIGNER 61
D.2 ANSYS SIWAVE 62
D.3 ANSYS Q3D EXTRACTOR 64
D.3.1 Identifying Nets *65*
D.3.2 Assign Excitations *65*
D.3.3 Defining Mesh Operations *66*
D.3.4 Specify a Solution Setup *67*
D.3.4.1 Frequency Sweep 68
D.3.5 Q3D Validation and Analysis *68*
D.3.6 Post Processing and Generating Reports *69*
D.3.7 Reducing Matrices *70*
D.3.7.1 Float Net 71
D.3.7.2 Ground Net 71
D.3.7.3 Float Terminal 71
D.3.7.4 Float at Infinity 71
D.3.7.5 Return Path 71
D.4 ANSYS CIRCUIT DESIGN 72

E. CONCLUSIONS 73

CHAPTER III: ENDORSEMENT OF SIMULATION MODELLING TECHNIQUE 75

A. GALVANICALLY ISOLATED GATE DRIVERS 75

B. PULSE PLANAR TRANSFORMER DESIGN 79

B.1 TRANSFORMER SCHEME 79
B.2 NORM CONFORMITY 81
B.3 SIGNAL TRANSMISSION AND ELECTRONIC CIRCUITRY 81

C. TRANSFORMER SCATTERING PARAMETERS 83

C.1 PULSE TRANSFORMER EFFICIENT FREQUENCY BAND 83
C.2 S PARAMETER ANALYSIS – ANSYS Q3D EXTRACTOR 85
C.2.1 Ansys Circuit Design Dynamic Link *88*
C.3 S PARAMETER EXPERIMENTAL VALIDATION 89

D. COMMON MODE TRANSIENT IMMUNITY 91

D.1 SUB-CIRCUIT DV/DT IMMUNITY TEST 91
D.2 EQUIVALENT CIRCUIT MODEL SUSCEPTIBILITY 93
D.2.1 Generic Corresponding Circuit Model *93*

D.2.2 Pulse Transformer Parameter Extraction *93*
D.2.3 Equivalent Model Susceptibility Test *95*
D.3 EXPERIMENTAL EXAMINATION 96
D.3.1 Experimental Circuit Arrangement *96*
D.3.2 dv/dt Immunity Results *97*

E. CONCLUSIONS 99

CHAPTER IV: SHIELDING STRUCTURE DESIGN FOR MULTI-LEVEL GATE DRIVER OF SIC MOSFETS 102

A. GATE DRIVERS FOR SIC MOSFETS 102

A.1 COMMERCIAL SIC MOSFET GATE DRIVERS 103
A.2 MULTI-LEVEL ACTIVE GATE DRIVER TOPOLOGY FOR SIC MOSFETS 105

B. RENOVATED PULSE TRANSFORMER SCHEME 106

B.1 COMPLIANCE TO STANDARDS 107
B.2 PULSE TRANSFORMER SYNOPSIS 107
B.2.1 Magnetic Core Specifications *107*
B.2.2 Winding Number of Turns *108*
B.2.3 Definite Transformer Scheme *108*
B.3 SHIELDING STRUCTURE DESIGNS 109

C. SHIELDING EFFECTIVENESS ON TRANSFORMERS' CMTI 113

C.1 S PARAMETER EXAMINATION 113
C.1.1 S Parameter Authentication *115*
C.2 ANSYS Q3D FIELD PLOT GENERATION 116
C.3 SHIELD EFFICACY ON CMTI – SUBCIRCUIT ANALYSIS 117
C.4 CM EQUIVALENT CIRCUIT MODEL 119
C.5 EXPERIMENTAL VALIDATION 122
C.5.1 Transformer Susceptibility Experimental Set-Up *122*
C.5.2 Shielded Transformers Susceptibility Test Results *124*

D. EXPLORATIONS AND PERSPECTIVES 126

D.1 DIELECTRIC MATERIAL SIGNIFICANCE 126
D.1.1 Dielectric Material Consequence on CMTI *127*

E. CONCLUSIONS 129

GENERAL CONCLUSION AND OUTLOOK 130

A. CONCLUSIONS AND CONTRIBUTIONS 130

A.1 SIMULATION ANALYSIS 130
A.2 PULSE TRANSFORMER MODELLING 131
A.3 SHIELDING STRUCTURE DESIGN 132
A.4 DIELECTRIC MATERIAL IMPORTANCE 133

B. RECOMMENDATIONS AND FUTURE WORK 133

REFERENCES 135

GLOSSARY

AC	Alternating Current
AGD	Active Gate Drivers
AEF	Active EMI Filters
BJT	Bipolar Junction Transistor
CAD	Computer-Aided Design
CAGR	Compound Annual Growth Rate
CM	Common Mode
CMR	Common Mode Rejection
CMTI	Common Mode Transient Immunity
CMTN	Common Mode Transient Noise
CMTV	Common Mode Transient Voltage
DC	Direct Current
DK	Dielectric Constant
DM	Differential Mode
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMS	Electromagnetic Susceptibility
ETO	Emitter Turnoff
EV	Electric Vehicle
FCC	Federal Communications Commission
FEM	Finite Element Method
GaN	Gallium Nitride
GTO	Gate Turn-off
HFET	Heterojunction Field Effect Transistors
HFPT	High Frequency Planar Transformers
HPDC	High-Power Density Converters
HTE	High Thermal Electronics

IEC	International Electrochemical Commission
IGBTs	Insulated Gate Bipolar Transistors
IGCT	Integrated Gate Commutated Thyristors
JFET	Junction-Gate Field-Effect Transistor
LNA	Linear Network Analysis
MoM	Method of Moments
MOSFETs	Metal Oxide Semiconductor Field Effect Transistors
PCB	Printed Circuit Board
PCSs	Power Conversion Systems
PE	Power Electronics
PGS	Patterned Grounded Shield
PPE	Personal Protective Equipment
PTFE	Polytetraflouorethylene
S Parameters	Scattering Parameters
SBD	Schottky Barrier Diodes
Si	Silicon
SiC	Silicon Carbide
SCR	Silicon-Controlled Rectifiers
SGS	Solid Ground Shields
SMD	Surface Mount Device
SOC	State of Charge
SMPS	Switch Mode Power Supplies
UVLO	Undervoltage-Lockout
UPS	Uninterrupted Power Supplies
VNA	Vector Network Analyzer
WBG	Wide Bandgap

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I dedicate this thesis to my parents Zeinab Youssef and Ali Makki, as an expression of gratitude and admiration, as this achievement would not have been possible without their cherished guidance

and never-ending support. No words could ever describe how grateful, thankful and blessed I am to have you by my side, everything I am is because of you. I heartily acknowledge my brother Dr. Issa Makki and his beloved wife Malak, and my dearest sisters Sandra and Sara for their encouragement, reinforcement and assurance.

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DEDICATION

To my parents,

Zeinab Youssef and Ali Makki

RESUME EN FRANÇAIS

Dans les années 1990, l'arrivée de composants de puissance à base de silicium (MOSFET, IGBT) a permis le développement de convertisseurs d'énergie électrique à forte densité de puissance. De nos jours, la mise en œuvre de composants à base de matériaux dits « grand gap » tels que le carbure de silicium (SiC) fait l'objet de nombreux travaux de recherche. Ces nouveaux matériaux autorisent le fonctionnement des convertisseurs à de plus hautes températures et à des tensions plus élevées, permettant un nouvel accroissement de la densité de puissance. De plus, la réduction drastique des durées de commutation (donc des pertes par commutation) des composants SiC permet d'envisager au moins deux scénarios. Le premier consiste à ne pas augmenter la fréquence de découpage des convertisseurs actuels ce qui a pour conséquence d'accroitre le rendement de ces derniers. Un deuxième scénario consiste à accroitre la fréquence de découpage des interrupteurs tout en conservant le rendement du convertisseur. Le gain est alors porté sur la discrétion de la compatibilité électromagnétique (CEM) du convertisseur. Ces dernières années, les industriels ont commercialisé des diodes et des transistors SiC sous la forme de modules de puissance de type MOSFET. Ces composants sont actuellement disponibles dans des boîtiers dédiés aux systèmes sur PCB ou sous la forme de modules pour des convertisseurs de moyenne puissance (> 10kVA) et basse tension (< 3kV).

L'augmentation de la densité de puissance s'appuie généralement sur l'augmentation de la tension d'alimentation des convertisseurs. La traction électrique est un exemple parmi d'autres où les réseaux s'échelonnent de quelques centaines de volts à plusieurs dizaines de kilovolts pour les applications à très fortes puissances. L'arrivée sur le marché de composants MOSFET SiC crée de nouvelles opportunités pour des domaines de l'électronique de puissance avides de densité de puissance toujours plus grande. Des recherches en cours pour fabriquer des puces SiC dont le calibre en tension de 3,3 kV permet d'imaginer des convertisseurs avec des réseaux d'alimentation proches de 2 kV.

L'utilisation optimale de ces composants passe par le développement d'un étage de commande rapprochée (nommé gate-driver) adapté et prenant en compte la spécificité de la technologie SiC. Les drivers de base assurent une fonction de pilotage en régime bloqué - passant du semi-conducteur. Les drivers plus évolués, dédiés aux composants équipant les convertisseurs de moyenne puissance, possèdent en plus des fonctions sécuritaires (essentiellement sous-tension d'alimentation et désaturation) qui indiquent la présence ou non d'un défaut de fonctionnement de la puce. Les informations échangées entre les étages au plus près du composant de puissance (étages secondaires) et l'étage primaire (relié directement au système de contrôle qui gère l'ensemble des commandes et la sécurité) sont transmises par l'intermédiaire de transformateurs d'impulsions ou de fibres optiques.

L'énergie électrique nécessaire aux voies de commande nécessite aussi une alimentation isolée galvaniquement. Pour les applications de moyenne puissance, cette dernière se fait systématiquement par un transformateur d'impulsions.

Les gate-drivers développés au laboratoire IETR mettent en œuvre 4 transformateurs d'impulsions : 2 sont dédiés à la transmission de l'énergie électrique du primaire aux voies de

commande, 2 autres sont dédiés à la transmission des ordres de commandes et sont aussi un canal de transmission de données. Pour garantir la sécurité des utilisateurs, des normes imposent des distances minimales à respecter entre l'étage primaire et les étages secondaires d'un gate-driver. Des travaux de recherche actuels au sein de l'IETR portent sur l'intégration de nouvelles fonctions de monitoring au sein des gate-drivers.

Ce projet de recherche traitera uniquement de la problématique de l'isolation galvanique des signaux de commande par l'intermédiaire de transformateurs d'impulsions, car leurs capacités à fonctionner à une fréquence élevée ont amené de nouveaux défis à résoudre tels que les problèmes d'interférence électromagnétique (EMI). De plus, l'augmentation de la vitesse de commutation des MOSFETs SiC entraîne des dv/dt de plus en plus élevés, ce qui induit des courants de mode commun traversant les capacités parasites du transformateur. Ces perturbations peuvent provoquer une transmission de commandes défectueuses au module de puissance et entraîner un court-circuit de bras.

L'objectif visé est l'amélioration du design du transformateur d'impulsion. Il est composé d'une ferrite et deux enroulements, un primaire et un secondaire. Au primaire comme au secondaire, des écrans électrostatiques (appelés aussi écrans de Faraday ou blindage) sont disposés. Chaque écran est relié au potentiel de référence des circuits électroniques auxquels ils sont associés. Ainsi, l'un est au potentiel de référence de l'électronique du primaire et l'autre au potentiel de référence de la voie de commande. Ils sont destinés à drainer les courants de mode commun vers un point particulier du circuit électronique afin de limiter les perturbations qu'ils induisent. Le design actuel de ces écrans ne repose sur aucune étude théorique, mais sur un savoir-faire et une expérience acquise depuis des années. Un des objectifs de la thèse est de définir le design de ces écrans électrostatiques par le biais de modèles et de simulations.

De même, le design de ces transformateurs d'impulsions est variable selon les habitudes des industriels ou des laboratoires de recherche. Le transformateur d'impulsion développé à l'IETR est de type planaire avec ces enroulements intégrés au PCB. Il possède également un écran électrostatique par enroulement.

Le but principal de cette thèse est de définir l'importance de ces écrans dans les transformateurs planaires. Le fil conducteur de ces travaux est le suivant : dessinés à partir du logiciel Altium Designer, les transformateurs sont ensuite modélisés avec l'outil Ansys Q3D Extractor et différents modèles sont obtenus. L'immunité des transformateurs est ensuite testée en simulation et les meilleurs designs de transformateurs sont sélectionnés. Les transformateurs sélectionnés sont ensuite fabriqués et des tests expérimentaux sont effectués afin de confirmer les simulations. Ainsi, le mémoire de thèse est constitué d'une introduction générale, quatre chapitres, une conclusion et des perspectives.

Au chapitre I, une introduction générale présente l'état de l'art de tous les aspects importants d'un système de convertisseur de puissance : introduction aux bases des systèmes de conversion de l'énergie électrique, aux bases des semi-conducteurs de puissance, à l'émergence des matériaux à large bande interdite et à leurs intégrations dans les applications de commande de grille. La topologie du gate-driver et de ces principales fonctions sont discutées. Ce chapitre met en évidence l'importance

du transformateur à technologie planaire et à son intégration dans les gate-drivers, en présentant les avantages et les inconvénients de cette technologie.

Les normes de compatibilité électromagnétique sont présentées et la catégorisation des interférences électromagnétiques dans les convertisseurs de puissance est expliquée. Enfin, les techniques de réduction du bruit en mode commun dans les systèmes de convertisseurs de puissance sont précisées et les techniques d'atténuation sont examinées. En particulier, les techniques d'insertion d'écrans de Faraday dans les transformateurs planaires sont présentées avec des aspects pratiques tout en discutant de l'importance de l'outil de simulation avant la phase de fabrication de prototypes.

Le chapitre II établit la chaîne complète de modélisation, avec plusieurs outils logiciels tels que Altium Designer, Ansys SIWAVE, Ansys Q3D Extractor et Ansys Cicuit Design. Le processus de modélisation est présenté à l'aide d'un exemple. L'étude en simulation de l'immunité du transformateur soumis à des forts dv/dt, tels que ceux rencontrés expérimentalement, permet de réduire le temps de conception des transformateurs et accroit la sureté de fonctionnement des gate-drivers.

Le processus de simulation décrit précédemment est exploité au chapitre 3. Des transformateurs planaires déjà fabriqués pour une précédente thèse et qui étaient destinés à piloter des MOSFET SiC 1,2 kV sont modélisés et simulés. La modélisation avec l'outil Ansys Q3D Extractor prend en compte le comportement du transformateur en mode différentiel et en mode commun. Elle intègre également une impédance de source et de charge connectées respectivement au primaire et au secondaire du transformateur. La validation de cette approche est effectuée en comparant des résultats de simulation à des mesures expérimentales. Un train d'impulsions d'amplitudes 1,4 kV avec un dv/dt égal à 125 kV/µs a été appliqué entre les 2 enroulements du transformateur et le niveau de bruit au niveau de l'étage secondaire a été mesuré et comparé aux simulations.

En parallèle, un modèle électrique équivalent pour le transformateur a été déduit. Dans un premier temps, une analyse spectrale de la forme des impulsions a été effectuée pour déterminer la bande de fréquences utiles. Dans un second temps, cette bande de fréquence est fournie à Ansys Circuit Design, ce qui permet d'obtenir les paramètres S du transformateur. Ces paramètres sont ensuite comparés à la mesure des paramètres S du transformateur 'réel'. La comparaison des paramètres S simulés avec ceux mesurés est satisfaisante. Dans un troisième temps, cette bande fréquentielle est ensuite paramétrée dans Ansys Q3D Extractor afin de déduire les paramètres électriques équivalents du transformateur. Ainsi, un modèle de type LTspice a été établi pour une fréquence définie de 50 MHz, cette fréquence étant choisie après l'analyse spectrale des impulsions. Puis ce modèle est simulé dans les conditions expérimentales précédentes. Les résultats de simulation et les mesures effectuées sont proches. En conclusion, la méthodologie mise en place pour modéliser des transformateurs mis en œuvre dans une précédente thèse est validée et est mise en œuvre au chapitre suivant pour concevoir de nouveaux designs de transformateurs intégrés dans des gate- drivers pilotant des modules MOSFETs SiC de 3,3 kV.

Dans le chapitre IV, des nouveaux écrans de Faraday sont dessinés et étudiés en simulation. L'immunité de ces nouveaux transformateurs soumis à des forts dv /dt est testé en simulation pour

différents paramètres géométriques. L'influence de la forme des écrans, de leur longueur, leur largeur et leur épaisseur est étudiée. Deux structures de blindage, solides et fragmentés, sont simulés. Le niveau de bruit au secondaire du transformateur est quantifié en simulation et les meilleurs designs de transformateurs sont sélectionnés. Les transformateurs sélectionnés sont ensuite fabriqués et des mesures expérimentales sont effectuées. La comparaison entre les mesures et les simulations valide l'approche effectuée. De plus, ce chapitre met en évidence l'effet du choix des matériaux diélectriques employés sur la variation de la susceptibilité des transformateurs d'impulsions.

Le chapitre V résume les travaux de recherche menés durant cette thèse et des perspectives de travaux futurs sont proposées.

GENERAL INTRODUCTION

Scientific exchange and collective contribution to the pool of knowledge is the primary objective of researching and economic growth. This research has been conducted under the framework of international thesis co-supervision. It is a mutually supervised doctoral program by the University of Nantes (UN), France and the Lebanese International University (LIU), Lebanon. In Lebanon, theoretical research was conducted and simulative analysis was performed. Moreover, financial support was granted upon performing research and instructing activities at the university. In France, simulation and experimental validation was conducted at IETR laboratory with the entire team. In addition, financial assistance and accommodation was granted during the research visit period.

For several years, the IETR laboratory team at University of Nantes conducted alternative researches encompassing gate driver circuit topologies. The established studies are always harmonized with the continual advancements of those topologies persevering substantial improvement in this domain. During the period in France, the research was conducted at IETR laboratory, Chantrerie site, accompanied with the ASIC team. Research and scientific exchange with scholars at the site, naming Antoine Laspeyres and Corentin Darbas, was very perceptive as intellectual cooperation is opportune for advanced and auspicious ideas. This thesis explicitly focuses on the common mode and differential mode modelling of pulse planar transformers integrated in gate driver applications, serving as the product of a previous thesis conducted at IETR laboratory and a complementary thesis to Antoine's prospective dissertation, which will be outlined thereafter.

In the 1990s, silicon-based power semiconductor devices (MOSFETs, IGBTs), piloted the development of high-power density converters. Moreover, continual advancements lead to the breakthrough of wide bandgap (WBG) semiconductor materials based on silicon carbide (SiC) and gallium nitride (GaN), permitting power electronic components to operate at higher temperatures, superior voltages, further power density attainments and realizing exceptional switching speeds. Adequately harnessing these capabilities, whilst safeguarding electromagnetic compatibility (EMC) standards, can lead to dramatic energy savings in diversified industrial applications. Recently, the market encountered a substantial commercialization of SiC diodes and MOSFET power modules. These components are currently serviceable as elements devoted for PCB system integration or as modules for medium power and low voltage converters.

The optimal exploitation of these distinctive devices is by means of PCB-integrated gate driver technologies. A gate driver circuit is an indispensable constituent of a power electronic system, it serves as an interface between microcontrollers that manage the switching operations (low voltage side) and the connected power module (high voltage side). This requires a galvanic isolation barrier that electrically isolates primary to secondary circuitry with discrete ground references. Gate drivers provide at least two operations, that include signal transmission and power supply. The fundamental concern of this thesis is the examination of switching order transmission through the galvanic isolation. Technologies such as optocouplers and pulse transformers are commonly recognized for

realizing the latter. For medium power applications, planar pulse transformers serve as the predominantly shared isolation technology amongst semiconductor manufacturers.

Nonetheless, this constructive blend of advanced technologies, originates severe alertness towards sustaining electromagnetic compatibility (EMC) standards. The realization of higher switching frequencies is worthwhile as long as it does not contribute to electromagnetic disturbances. However, an ample potential variation induces the development of common mode (CM) currents in gate driver circuits, which are mainly routed through interwinding capacitances of pulse planar transformers. This issue is alarming, as a faulty trigger of the semiconductor device originating from the unwanted pulsating currents can lead to hazardous results. Therefore, this highlights the necessity to mitigate CM current passage through the transformers by reducing the stray capacitance, renowned as the interwinding capacitance between the primary and the secondary windings. This dilemma can be resolved by acquiring proper installation of securely grounded electrostatic screens, which are acknowledged as faraday shielding layers. The actualized pulse planar transformers at IETR lab, which were integrated in a realized gate driver card intending to drive 1.2 kV SiC MOSFETs, were based on knowledge and expertise in the field; laying the foundation of this conducted thesis.

The main focus of this thesis is to groundwork the importance of faraday shielding insertion in pulse planar transformers by primarily modelling and analyzing the realized planar transformer prototypes via Ansys Q3D Extractor tool. Firstly, the objective is to set a theoretical and a simulative prospective that legitimize the formerly obtained experimental results. The agreeable results will affirm the dv/dt immunity of the transformers, hence, ensuring faraday shielding integration significance when responding to a steep potential variation applied between the primary and the secondary distinctive grounds. Moreover, novel ameliorated designs of the pulse transformer will be presented, examining alternative shielding design configurations, aiming to study the common mode transient immunity (CMTI) of the transformers and construct a corresponding equivalent circuit model that represents individual transformers. Accordingly, the thesis will be sectioned into four main chapters and a conclusion with perspectives.

Chapter I, a collective introduction, will present the state of the art of all prominent aspects of a power converter system. Initiating with basics of power conversion systems, fundamentals of power semiconductors, emergence of wide-band-gap material and the integration in gate driver applications. Moreover, challenges comprising the utilization of the latter technology will be presented, specifically regarding pulse transformers in gate driver applications, and means of mitigation techniques highlighted in literature will be reviewed.

Chapter II will accurately define the simulation methodology utilized with collective software tools, primarily Ansys Q3D Extractor, aiming to model, analyze and investigate the intended pulse planar transformer. The process will be explicitly and exceptionally presented in this thesis using a demonstrative example in this chapter.

Chapter III will verify the simulation process discussed in chapter II, by investigating already realized shielded pulse planar transformers that intended to drive 1.2 kV SiC MOSFETs. The latter will be simulated to duplicate an experimental realization and investigate the transformer's endurance to abrupt dv/dt application. Moreover, similar analysis will be implemented on a constructed equivalent circuit model of the transformers.

Chapter IV demonstrates an altered pulse planar transformer integrated into a distinctive gate driver card aiming to drive 3.3 kV SiC MOSFETs, where novel and ameliorated shielding designs will be investigated whilst evaluating the transformers' persistence to high switching transients. In addition, this section will also highlight the effect of dielectric material selection on the interwinding capacitance of the pulse transformers.

Finally, **Chapter V** concludes the thesis and briefly summarizes the main contributions and essential propositions. In addition, a forecast on possible future works is established.

CHAPTER I: STATE-OF-THE-ART

Power Electronics (PE) is a preeminent field of study in electrical engineering which acquires boundless areas of development and improvement, entitled as a "quiet revolution" [1]. As depicted in figure I-1, this field is enforced in wide ranges of electrical energy operations, granting it a multidisciplinary attribute.

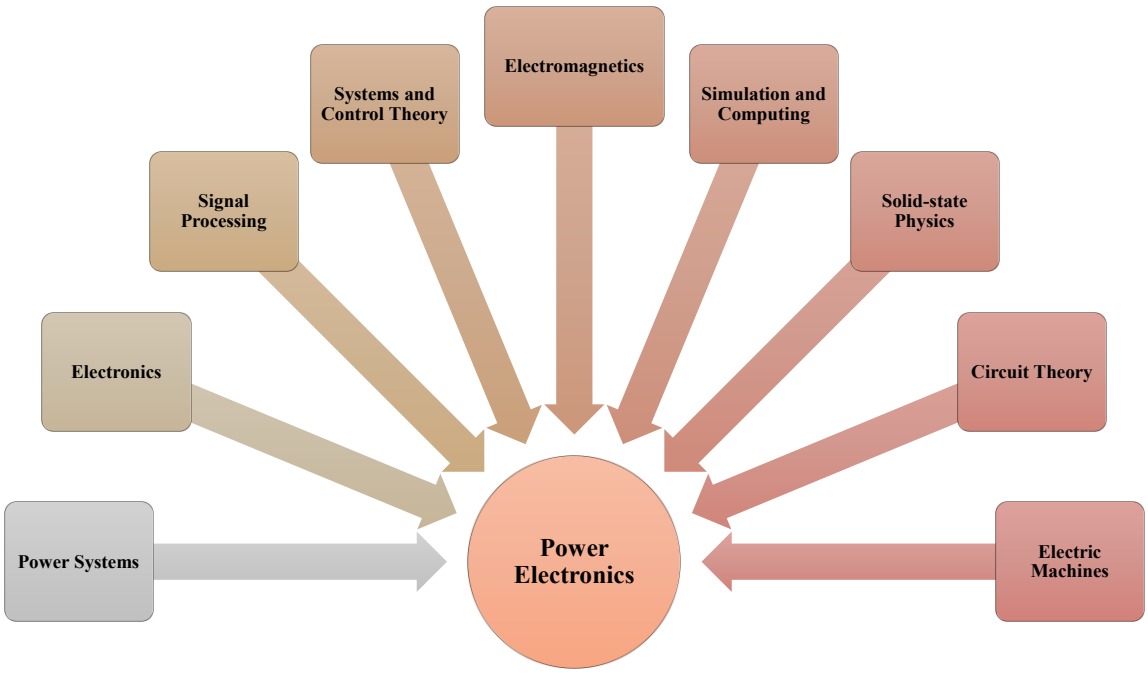


Figure I-1: Multidisciplinary attribute of Power Electronics

The evolution of electronic devices over the past few years has resulted in compelling impacts on the community and industry. Gradual technological leaps in the field of semiconductors and power devices are forecasted to structure the mechanized sector of the revolutionized globe [2], [3] . Robust power electronic systems are demanded in automotive, energy management, telecommunication, medical, and aeronautic applications [4]. Since 1970, the power density of power electronic converters in diverse operations has nearly doubled every ten years [5]. The primary agent of this trend was the proficiency to increase the switching frequency by a multiple of ten every decade, which was realized by the incessant improvement of power semiconductor device technologies [6]. This continual advancement of power density converters is portrayed by the demanded requirements for higher efficiency and reliability, volume reduction, lightweight materials, and cost effectiveness. Substantial research and examinations have been applied to different aspects of the aforementioned power converter system constituents to attain significant efficiency and power density objectives. However, optimization always comes with a cost; with every advancement, researchers and analysts are confronted with challenges and impediments to realize upgraded power converter designs.

A. POWER CONVERSION SYSTEMS' STRUCTURE

A.1 Overview

A.1.1 Power Conversion System Background

The fundamental objective of power electronic technology is to transform and regulate the flow of electrical energy aiming to supply optimum voltages and currents that fulfill user-defined requirements. Power Conversion Systems (PCSs) serve as an interconnection between incongruent types of electricity, such as alternating current (AC) sources with distinctive frequencies, direct current (DC) sources of dissimilar voltage magnitudes, AC and DC supplies, and a merger of all the latter as depicted in figure I-2. As observed, inverters and rectifiers are represented by a single-stage energy conversion model, whereas, AC/AC and DC/DC converters can additionally be realized by implementing two conversion stages using a DC and an AC link, respectively [7]. Formerly, sophisticated rather inefficient, electromechanical devices were used to attain such conversions, where the competency to interconnect two varied DC voltages was practically unattainable. This discloses the governance of AC technology for power transmission and distribution during that period. Currently, economical, competent and versatile power electronic converters are extensively used universally [8].

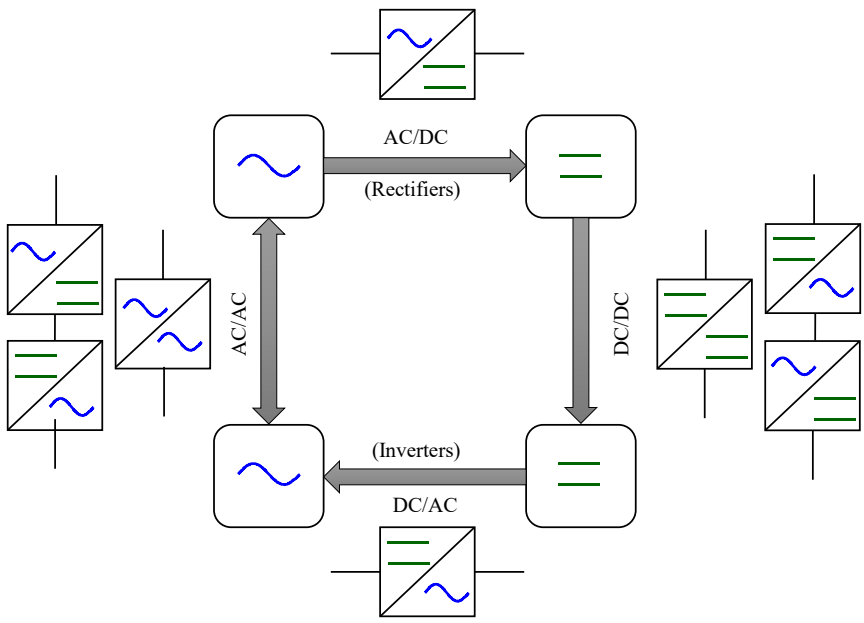


Figure I-2: Basic forms of power converters

A prevalent example is one's cellphone, which requires fixed and secured DC voltages for convenient functioning. This is achieved by converting the AC supply at the household to a compatible DC voltage using an AC/DC converter or rectifier. Furthermore, DC/DC converters are needed to convert the wavering DC voltage due to the battery's state of charge (SOC) into a steady DC voltage for the electronics. As for non-digital devices, motors that are driven directly from the AC grid acquire the grid's rotational frequency and their manufactured frequency, where it is beneficial to decouple these two frequencies. This is attained by using an AC/DC rectifier, followed by a DC to AC inverter at any relevant frequency, creating a variable speed drive (VSD) [8].

A.1.2 Switched-Mode Converters

Power electronic converters such as controlled rectifiers or choppers can be utilized to regulate the DC power for DC drives, contrarily, AC drives employ inverters to modify the voltage and frequency of the AC power. Switched-mode converters are DC-DC converters that supply DC loads with regulated output voltage that is either stepped up or stepped down, referred to as boost converter and buck converter, respectively. The chopper circuit is termed as a boost converter if the output voltage is greater than the input voltage, whereas a buck converter is identified when the output voltage is lower than the input voltage. Moreover, a buck-boost converter combines the functions of the latter in a single circuit and can be utilized in wide applications such as battery power systems. A fundamental DC-DC conversion solution is depicted in figure I-3 below, comprising switches S1 and S2 which represent at least one active device such as a power semiconductor and one passive component such as a diode, that operate in accordance to an external control signal. Thus, a 'control circuit' is utilized in all power converter applications as presented in figure I-4, to constantly monitor and compare the output voltage against an embedded 'reference voltage', initiating corrective action if the output drifts from its appointed value.

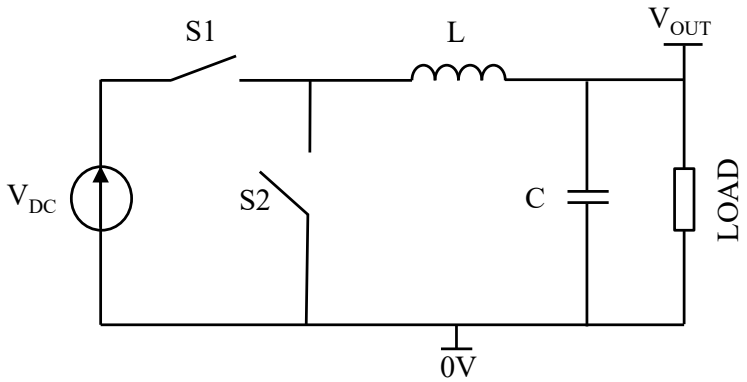


Figure I-3: Ideal DC-DC step-down converter circuit (buck converter)

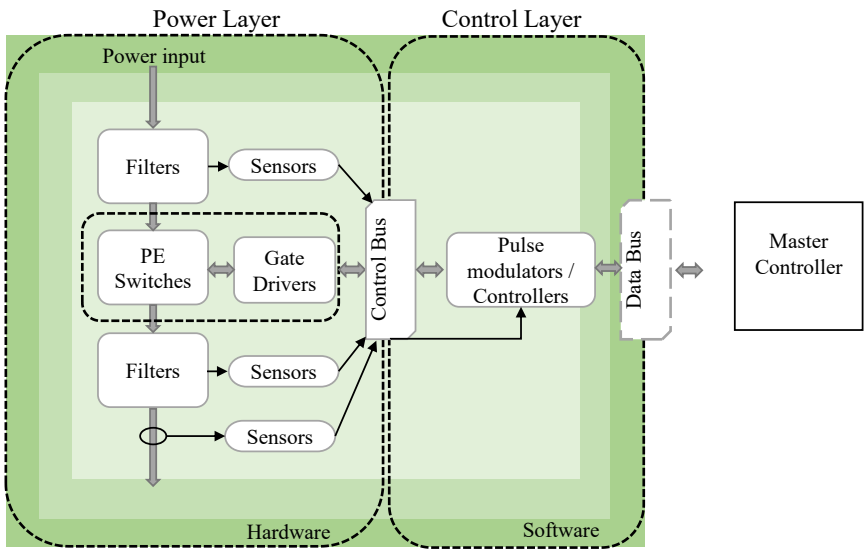


Figure I-4: Block diagram of power electronics arrangement

A.1.3 Fundamentals of DC-AC Converters

DC-AC converters are well-known as inverters, their role is to change a DC input voltage into a symmetric AC output voltage of intended magnitude and frequency. Applications such as adjustable-speed ac motor drives, uninterrupted power supplies (UPS), grid integration of renewable energy resources and electric vehicle battery charging systems demand the utilization of inverters [9]. Ideally, the output voltage waveforms of inverters are sinusoidal. However, practically, the waveforms are non-ideal and contain harmonics as shown in the exemplary of a full bridge inverter represented in figure I-5 thereafter.

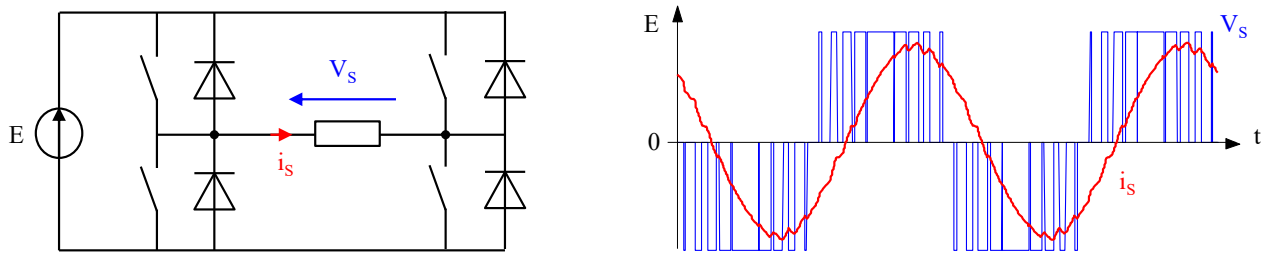


Figure I-5 : Single-phase full bridge inverter with associated waveforms

A full bridge inverter requires four diodes and four self-commutating switches which can be controlled (ON/OFF) using modulation signals. Each diode is connected in antiparallel to the switch. The useful power level application of such inverters ranges from 200 to 2000 VA. There are diverse contemporary and controllable power electronic switches that can be utilized such as relays, thyristors, Insulated Gate Bipolar Transistors (IGBTs) and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [10] . The output frequency of this type of inverter may be controlled by regulating the switch on and off times of the latter mentioned components. Figure I-6 represents an example of a half bridge switching cell, known as the vertical arm of a full bridge inverter, comprising two N-type MOSFETs that are unidirectional in voltage and bidirectional in current. The depiction highlights that the practical switching time of the MOSFETs are relatively prolonged with respect to the theoretical switching times, in addition to the inevitability of a galvanic isolation safeguarding independent transistor control [11]. It is imperative to protect the depicted switching cell against a short circuit occurrence [12]. Henceforth, it is common to integrate a time delay, termed as 'dead time', between the conducting and blocking phases of the transistors, to compensate for the difference between the conducting and blocking times. MOSFET transistors operate in the '1st quadrant' and '3rd quadrant' corresponding respectively to the phases where (V_{DS} >0, I_D>0) and (V_{DS} <0, I_D<0) as revealed in figure I-6.

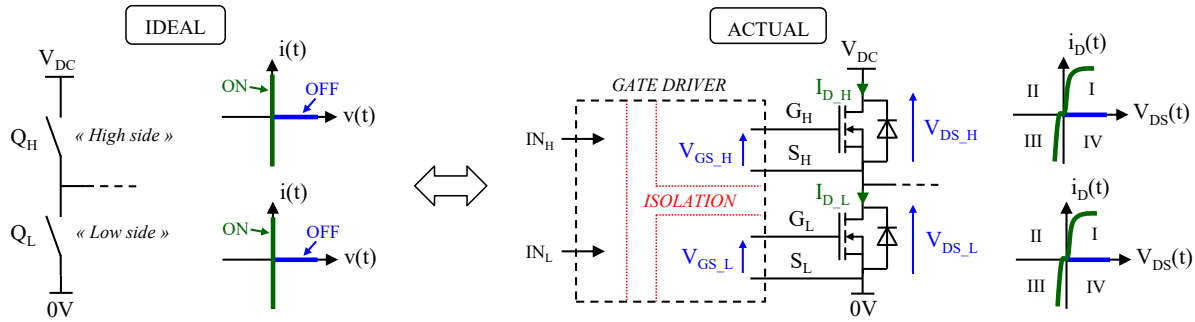


Figure I-6: Basic example of a switching arm with N-MOSFET transistors

A.2 Power Semiconductor Devices

A.2.1 State-of-the-Art: Power Semiconductors

Power semiconductor devices resemble the concrete foundation of power electronic systems. They play an indispensable role in determining the system's efficiency, size and cost. Originating from the invention and marketing of silicon (Si) bipolar junction transistor (BJT) sixty years ago, a considerable collection of Si power semiconductor devices have been promoted and commercialized, enabling power electronic systems to attain ultra-high efficiencies and power capacities required for various applications [13].

Currently, power converters are designed to envelope a broad range of power levels, from gigawatt in high-voltage direct current (HVDC) transmission systems to a few watts necessitated to function a mobile phone. As mentioned earlier, since power conversions can be processed various times before reaching the end-user, it is excessively crucial to realize high energy conversion efficiency in power electronic converters. This is associated to the amelioration of power semiconductor devices by the reduction of conduction and switching losses. In the last six decades, to meet high power density demands, more reliability, superior switching frequency levels whilst maintaining cost effectiveness, diversified current conduction mechanisms have been developed. The main innovation stimulant is to achieve power devices that can conduct more current for a defined chip area and breakdown voltage, hence improving the conductivity of the device when it is in the ON state, and the controllability of the alternating ON/OFF state occurrences.

A historical perspective of the latest development of power semiconductor devices is presented thenceforth in figure I-7 highlighting their augmentation and commercialization events.

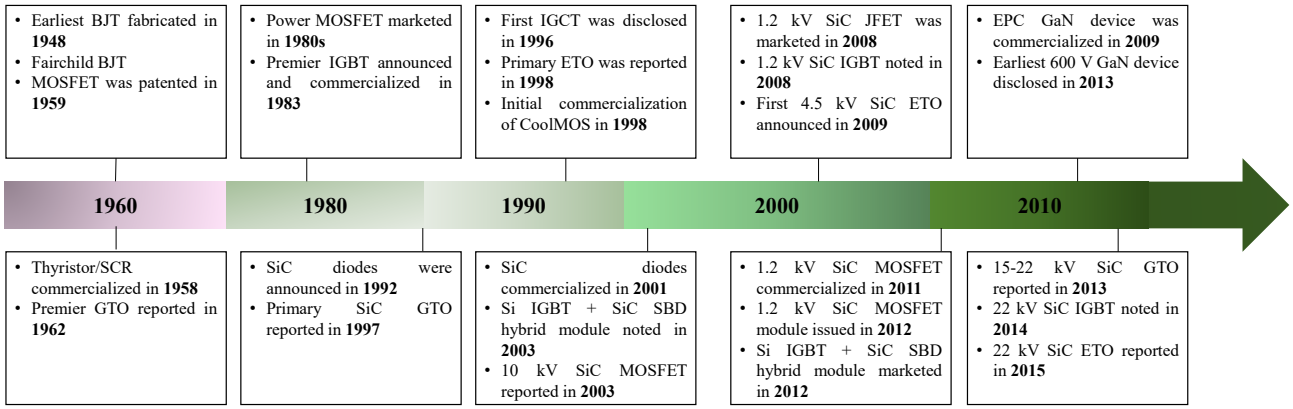


Figure I-7: Pivotal power semiconductor development and commercialization story line

As illustrated above, the inauguration of this technology with a transistor based on Germanium material took place at Bell Lab in 1948 [13]. Silicon bipolar junction transistor (BJT) and silicon-controlled rectifiers (SCR), or thyristors were marketed in 1958. Controlled three terminal switches such as BJTs and gate turn-off (GTO) thyristors were popularized in the 1960s and 1970s for power supply and motor drive applications [14]. In the 1980s, two popular inventions were developed that displaced the utilization of BJTs: MOSFETs which possesses exceptional static and dynamic performance and a gate control interface [15], and IGBTs [16] which profited from the power MOSFET fabrication process, however depended on a different physics where both electrons and holes contribute to current conduction, replacing GTO in most high power applications. In the mid-1990s, inventive super junction MOSFETs further reduced the conduction loss of power MOSFETs below the renowned 'silicon limit' [17]. The spotlight in the late 1990s was on integrated gate commutated thyristors (IGCT) and emitter turnoff (ETO) thyristors, which made high power GTOs feasible in ultra-high power converters [18], [19]. Subsequently, major innovative outbreaks occurred such as Schottky barrier diodes (SBD) [20], silicon carbide (SiC) MOSFETs [21] and heterojunction field effect transistors (HFET) based on gallium nitride (GaN) material [22].

A.2.2 Innovations in WBG Power Devices

Although Si-based IGBTs have been on the market for more than thirty years, they have reached their physical limits when confronted with the demand of high-power density converters (HPDC) and therefore higher switching frequencies [23]. The breakthrough of WBG device technology gained tremendous momentum serving as a pivotal enabler to achieve miniaturization of power electronic systems [24]–[30]. Furthermore, the emergence of commercial WBG semiconductor devices based on SiC- silicon combined with carbon-, GaN- gallium and nitrogen- and also diamond, prompted ample reduction in conduction losses due to their lower on-resistance. Moreover, they are featured with notable inferior gate capacitance, permitting them to operate at exceptional frequencies[31]. This technology farther lifted the borderline of power semiconductor devices to realize superior voltages, greater frequencies and higher temperatures as disclosed in figure I-8 below [32], [33]. Harnessing these capabilities, will allow WBG semiconductors to foreshadow intriguing innovations in power electronics, solid-state lighting and other various applications across numerous industrial and renewable energy sectors.

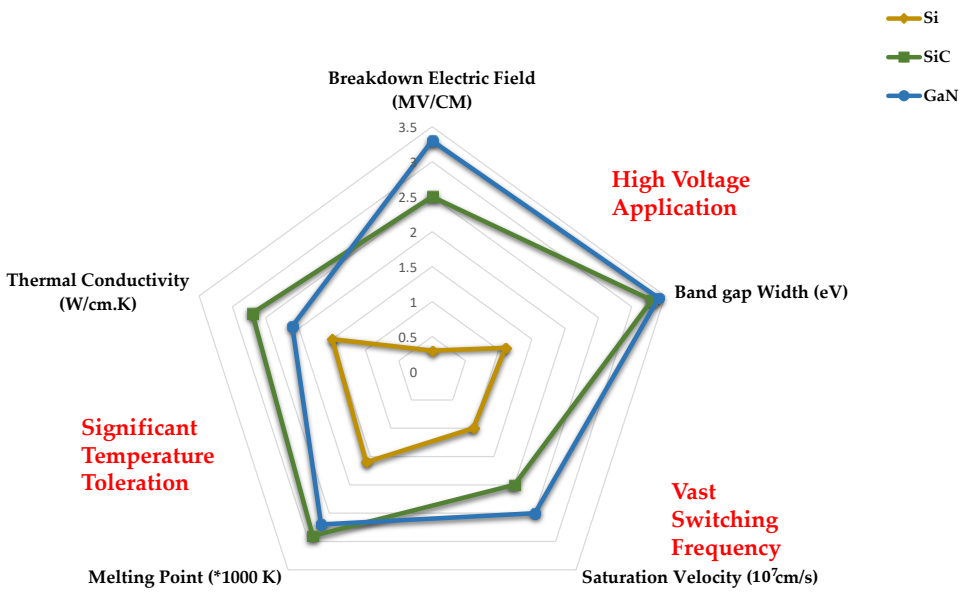


Figure I-8: Intrinsic properties of semiconductor materials: Si, SiC, GaN

The elemental agents that stirred the engagement and commercialization of SiC and GaN over their Si counterpart are their intrinsic material properties – bandgap, electric field and electron mobility, compared thereafter in table I-1.

Table I-1: Comparison of semiconductor material properties [34]

Parameter		**Si**	**GaN**	**SiC**
Band Gap	eV	1.12	3.4	3.2
Critical Electric Field	MV/cm	0.3	3.3	2.2
Electron Mobility	$cm^2/V.\ s$	1400	1800	950
Permittivity	ε_r	11.8	9	9.7
Thermal Conductivity	W/cm°C	1.5	1.3	4.9
Saturation Velocity	$10^7 \cdot cm/s$	1	2.7	2.7

As conferred, Si comprises a band gap just above an electron volt with a critical electric field of 0.3 MV/cm, differently, these specifications are much wider and greater for GaN and SiC revealing a tighter bond between the compositions of the material. The opportune realization of a high critical electric field, E_c, enables slimmer, more eminently doped voltage blocking layers in the devices, resulting in a considerable on-resistance reduction amounting to 1/10 in comparison to Si devices. To minimize conduction losses, high voltage Si MOSFETs are characterized with large chip areas, creating a high gate capacitance and notable losses at high switching frequencies. On the other hand, Si IGBTs exploit minority carriers and conductivity modulation, thus, acquire smaller die footprints than MOSFETs, yet the durability of minority carriers restrains the device's maximum switching frequency attainments. Accordingly, in correlation to a Si-based device, the integration of a high breakdown electric field, moderate conduction losses and short-term carrier lifetime, WBG materials can operate at a considerably higher frequency with a miniature footprint of 1/5 in comparison to Si

devices, using the same blocking voltage and on-resistance. The sparse intrinsic carrier concentration of these materials enables robust high-temperature operation due to low leakage currents [35].

SiC is leading in high voltage applications such as automotive, with massive growth in the electric vehicle sector (EV), information technology, grid infrastructure, electric motor drives and aerospace. Similarly, GaN is featured in applications such as DC/DC converters, motor drives and satellite electronics. Currently, SiC is considered to possess the best bargain regarding properties, commercialization, high power devices and high thermal electronics (HTE) [36]. Although GaN can offer superior frequency and voltage performances, however its thermal conductivity is lower than SiC, granting the latter better performance under high temperature conditions. Moreover, pure GaN is ten times more expensive than SiC, legitimizing the reason behind commercializing Si-substrate GaN instead of bulk GaN, which actually offers incomparable cost effectiveness over all other substrates including SiC.

As a concluding settlement of the tradeoff between SiC and GaN, the coexistence of both semiconductor material in the market is worthwhile in their respective categorized applications [37] as conferred in figure I-9 below. SiC devices grant higher breakdown voltage, greater temperature endurance and reliability. While, GaN present lower conduction losses (high power efficiency), lower cost and phenomenal performance at high frequencies [38].

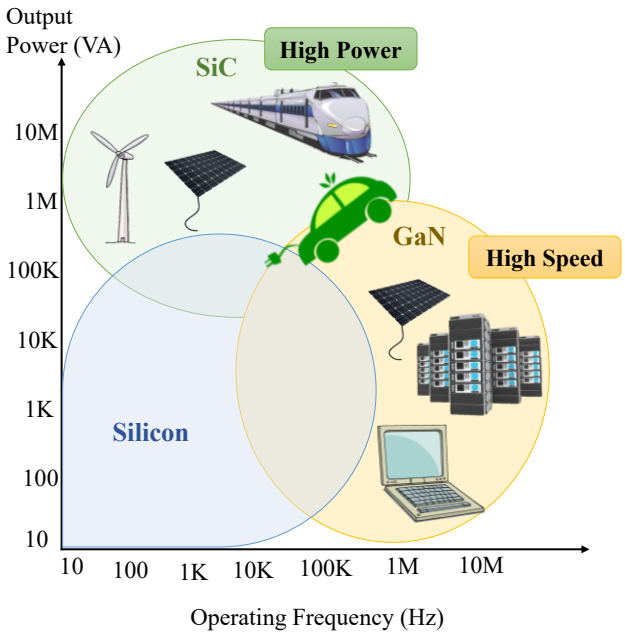


Figure I-9: Applications of SiC and GaN relative to operating frequency and output power

A.2.2.1 SiC MOSFETs

Over the past few years, accelerated endorsement of SiC devices played as a key trend in the power electronics industry [39], [40]. Figure I-10 below demonstrates the foretell of the compound annual growth rate (CAGR) and the application distribution of the power SiC market between 2019-2025 according to YOLE development.

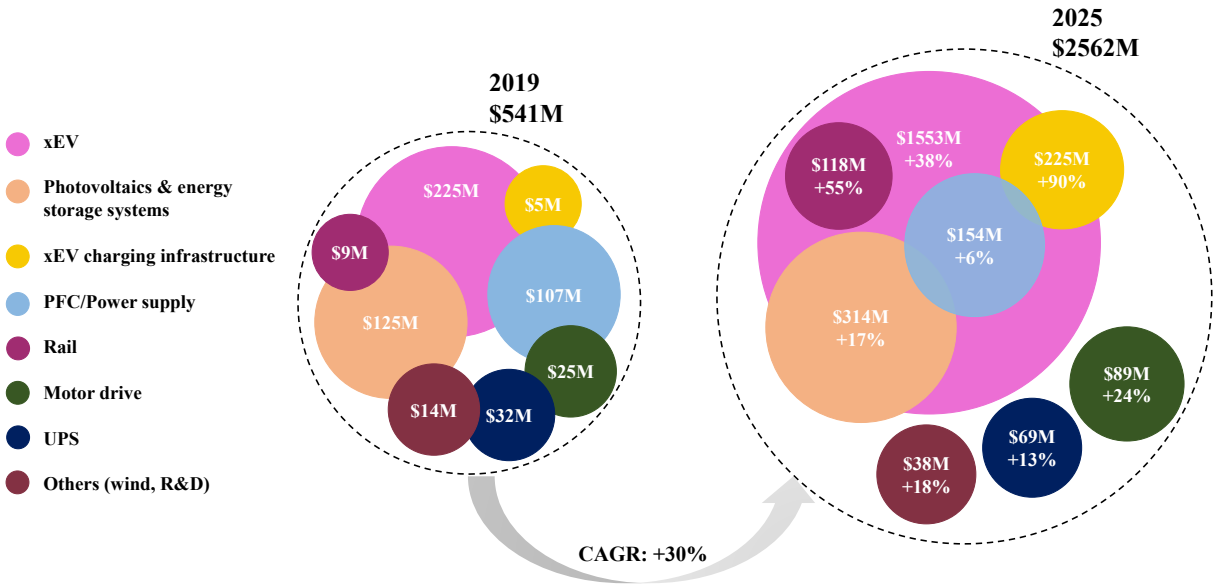


Figure I-10: Projection of power SiC market according to application by Yole Development[1]

MOSFETs are now employed in ubiquitous quantities in SiC-based power electronic systems. Compared with SiC JFET and BJT, they are the favored SiC three terminal switches. SiC MOSFETs are regarded as the upcoming generation of power switching devices for high power and high blocking voltage operations. It has been commercially popularized from 600 V to 1700 V reaching a new third generation of 3.3 kV with power loss and reverse current capacity improvement; in addition to higher current modules attaining 15 kV SiC MOSFETs have been prototyped and used in developing high-voltage-high-frequency solid state transformers [41], [42]. When compared to IGBT systems, a realization of one to two orders of magnitude incrementation in the operation frequency of SiC MOSFET based converters has been verified. Furthermore, a zero switching loss can also be actualized under precise conditions such as the operation of a 1.2 kV SiC module manufactured by Cree and integrated in a gate driver card at 3.38 MHz frequency is demonstrated in [43]. Considering their low conduction loss, they can also function in the third quadrant as a synchronous rectifier whilst reducing the third quadrant conduction loss and contributing to almost nil reverse recovery loss. The synchronous rectifier concept, despite being used with Si-MOSFET applications of less than 100 V, can now be applied to voltages ranging up to 3.3 kV with SiC MOSFETs.

As shown in figure I-11, there are two basic device architectures used in commercial SiC MOSFET compounds: a planar structure and a trench structure. It is imperative to declare that especially at lower voltages, there are three prospects that cannot be forsaken in a planar structure, which are: channel resistance, junction-gate field-effect transistor (JFET) resistance between the two P regions and the substrate resistance. Wafer slimming to less than 100 µm is efficient in reducing the substrate resistance, whereas improving the channel mobility meliorates the channel resistance. On the other hand, the superiority of the trench design is due to cell pitch reduction allowing channel density expansion hence reducing channel resistance as well as the eradication of the JFET region[44].

[1] https://s3.imicronews.com/uploads/2020/11/YDR20119_Power_SiC_Materials_Devices_Applications_2020_Sample.pdf

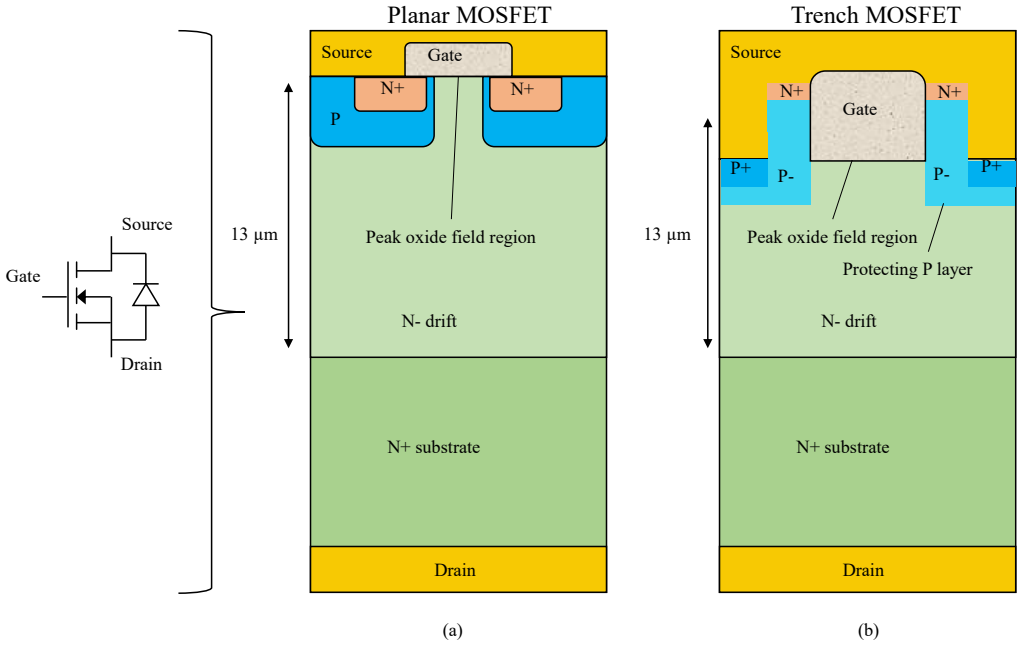


Figure I-11: Typical structure demonstration of a SiC MOSFET (a) planar; (b) trench

B. Gate Driver Topologies

B.1 Functional Specifications

Due to the sublime convenience of WBG devices, the market witnessed immense employment of this technology [45]. Nonetheless, to benefit from the technologies' distinguished performance, it is vital to upgrade its performance and system environment [46]. One of the imperative constituents of a power electronic system is a gate driver, as the terminology implies, it's the supply of a high current drive input for a gate of a high-power transistor such as a MOSFET. It serves as an interface between the low-voltage microcontroller and the high-voltage power modules (including MOSFETs, IGBTs, SiC MOSFETs, etc.). As illustrated in figure I-12, three basic classes of commercial IGBT/MOSFET gate drivers are available and categorized as follows:

- Driver ICs: From basic level shifters to completely molded integrated driver circuits including logic and isolation, this label encompasses a wide range of integrated circuits.
- Driver cores: On a larger range than a driver IC, a driver core provides all the functionalities for medium to high power applications. The entire circuit is manufactured on a printed circuit board (PCB) that can be further plugged or soldered on an alternative PCB, offering an adaptable design to fine-tune gate resistance and trip levels for peculiar modules. Moreover, isolation techniques are usually realized with pulse transformers and optocouplers permitting higher operating voltages and superior clearance/creepage distances. The aforementioned prospects will be further explained in the forthcoming section.
- Plug-and-play: These PCBs are designed to be instantly connected to a defined module housing. They are complete boards comprising all the features of a driver core, in addition

to equipped preconditioned gate resistors and structured components for a specific module type.

Integrated circuit drivers were commercialized by considerable manufacturers such as Texas Instruments, Infineon, On-semiconductor, Rohm semiconductor, Microchip, CISSOID, Power Integrations-Concept and Analog Devices. Moreover, the manufacturers that are prominent for high power applications are Wolfspeed-Cree, Semikron, Power Integrations-Concept and Infineon-Eupec.

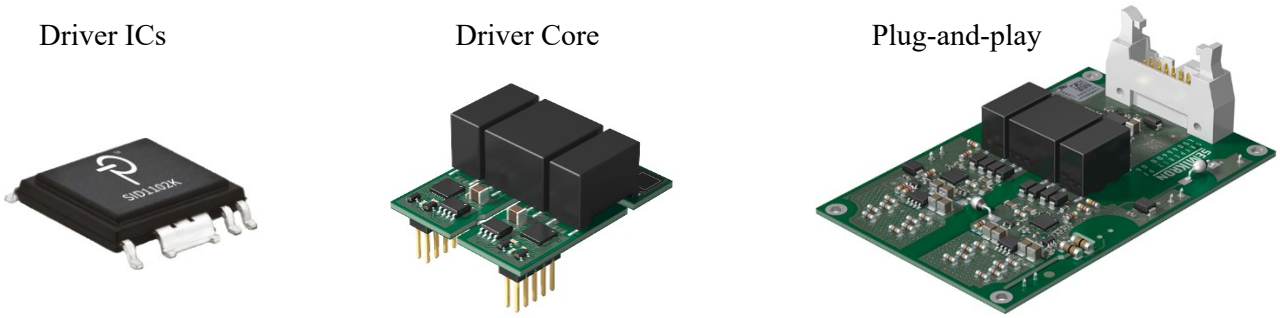


Figure I-12: Basic classes of gate drivers[2]

A conventional two-channel gate driver circuit is constructed in accordance to figure I-13, considering vital safety features and an apparent depiction of the isolation necessitated between the primary (low voltage) and secondary (high voltage) sides [47]. The controller cooperates with the primary side by transmitting control signals across the isolation barrier which is crucial to certify competent system functioning and user's safety [48]. Furthermore, an isolated power supply provided by a DC-DC converter, is essential to provide the potential needed to switch the power devices. Lastly, the secondary side is equipped with fast-acting protection and feedback schemes [49], [50]. It is imperative that the output stage, which allows signal buffering to drive the gate of the transistors, to be situated as close as possible to the power semiconductor devices. In case of a an application comprising SiC MOSFETs, to attain optimal switching the gate voltage required ranges from +20/-5 V for second generation modules and +15/-4 V for third generation components [51].

2 https://www.semikron.com

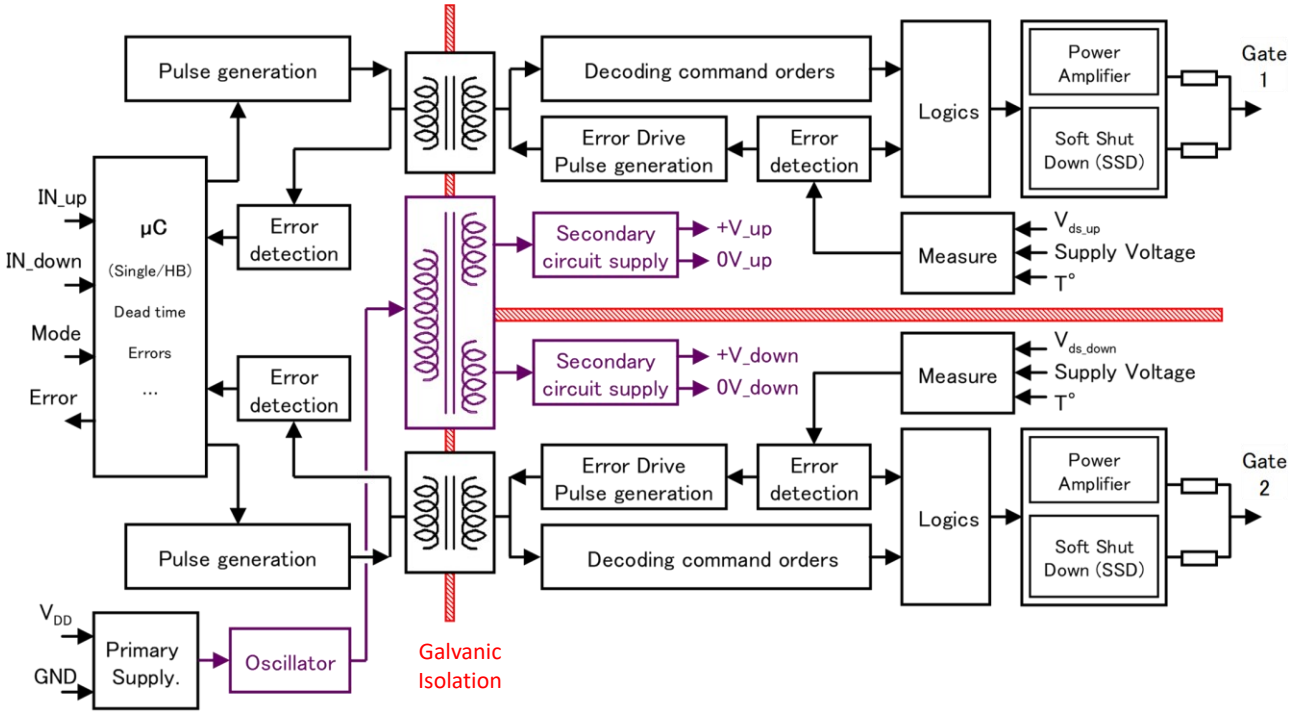


Figure I-13: Conventional gate driver circuit galvanically isolated using pulse transformers [47] [52]

B.2 Galvanic Isolation Requirement

Galvanic isolation, a prevailing gate driver characteristic used to provide optimal command orders for power devices, is an isolation barrier that electrically isolates primary to secondary circuitry, by founding segregated ground references. It concerns the isolation of the control signal transmission and the power supply circuit of the driver card. Gate drivers provide at least two functions that include signal transmission and power transmission as depicted in figure I-13 above. The power supply circuit is usually achieved by an isolated DC-DC converter, yet, the transmission of control signals or switching commands through the galvanic isolation barrier can be realized by the following technologies, appointed based on the voltage and power range of specific applications: optocoupler, transformer (with core/coreless), optical fiber, capacitive link and piezoelectric coupling [52]–[55]. Conventional isolators were obtained by means of optocouplers and/or discrete transformers[56]–[58]. However, these solutions are not adequate when it comes to expenses and restricted applications, respectively [59]–[61]. Presently, bulky and pricey methods are being replaced and dismissed by economical on-chip galvanically isolated modules [61], [62]. Table I-2 below compares some commonly used isolated gate driving solutions highlighting main parameters and features[60], [63].

Table I-2: Isolation solutions for gate driver systems [63]

Parameter	Optocoupler	Traditional Pulse Transformer	Isolated Gate-Driver IC (Coreless pulse transformer)	Digital Capacitive Isolator
Isolation Level	Reinforced, basic or functional	Reinforced, basic or functional	Reinforced, basic or functional	Reinforced, basic or functional
Propagation Delay	≥ 400 ns	≥ 35 ns	≈ 35 ns	≈ 50 ns
Stray Capacitance	≤ 2 pF	≥ 10 pF	≤ 2 pF	≤ 1 pF
CMTI	≤ 25 kV/µs	≥ 50 kV/µs	≥ 150 kV/µs	≥ 100 kV/µs

In high power applications, fiber optic isolators are seldom used due to their parasitic capacitances and complexities of incorporating fiber optic commands. Despite the extensive adoption of advantageous optocouplers in low to medium power applications, these devices suffer from aging, temperature drift and alternating current gain issues. In addition, they comprise significant parasitic capacitances which induce common mode (CM) current circulations between primary and secondary circuits, instigating electromagnetic disturbances. Modern gate drivers mainly employ digital isolators and pulse transformers. Digital capacitive isolators depend on high-voltage capacitors to withstand the required voltage rating and support isolation. Although they endure total immunity to magnetic fields, these devices have higher current consumption than transformer isolation. Moreover, a common consideration of capacitive isolators is their sensitivity to electric fields and common mode transients, originating common mode currents which can circulate through isolation capacitors and distort data transfer. Thus, an isolator's endurance and robustness to common mode transients is one of the essential parameters that determines an isolators' significance, this is demonstrated as the isolator's common mode rejection (CMR) or common mode transient immunity (CMTI) [64], [65]. It is measured by applying steep voltage pulses between two isolated ground references of the component, and it is defined by the maximal potential variation that the isolation can tolerate without impacting its data transfer efficiency. For optocouplers typical values for CMTI is less than 25 kV/µs, whereas capacitive isolators can attain up to 100 kV/µs considering their differential signaling.

Ultimately, magnetic isolators, particularly inductive ones as demonstrated in figure I-14, serve as the remarkably dispersed isolation technology among semiconductor manufacturers. This is exclusively attained with the expansion and progression of PCB-integrated gate driver technology, discussed thereafter.

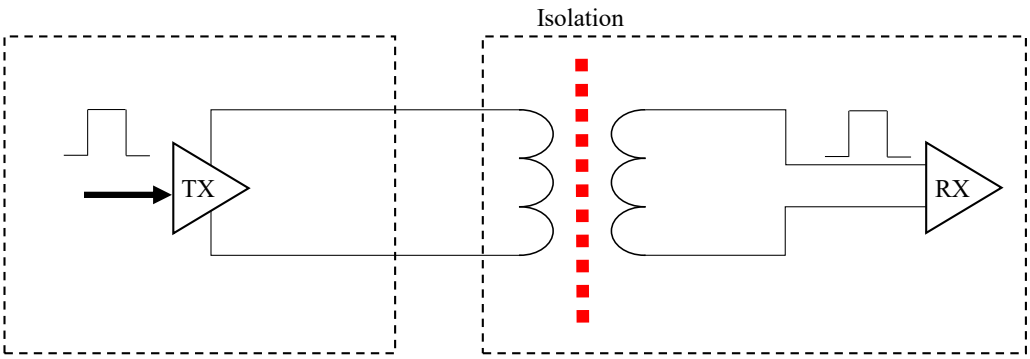
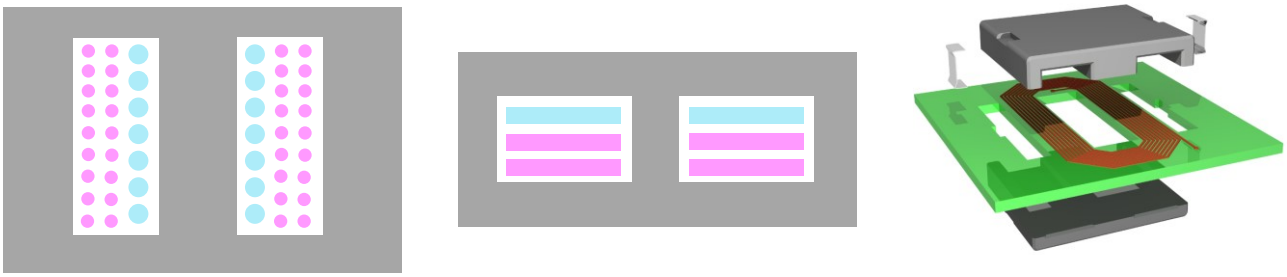


Figure I-14: Composition of an integrated inductive isolator

B.3 Planar Technology

The tendency toward high power density, high operating frequency, and low profile in power converters has disclosed a number of restraints in the employment of conventional wire-wound magnetic component structures. Favorable high switching frequency attainment becomes conflicting and challenging when considering the design of the magnetics which are the bulkiest components of power supplies. Nonetheless, at higher frequencies, skin and proximity effects increase leading to more winding losses and parasitic effects. Hence, to profit from the encouraging advancements, while inspecting the demerits, PCB-integrated gate drivers for WBG technology have been explored [66]. Electromagnetic compatibility (EMC) conformity is crucial when designing gate driver circuits amid preserving high power density and minimum isolation capacitance. This is attained by the utilization of planar transformers, which harmonize with the growing demand of slim-profile power supplies, and comprising low leakage inductance, repeatability and low thermal resistance [67], [68]. Research on the manufacturing of planar magnetic components has been investigated since the 1960s [69], mainly concentrating on thin film technology [70]. In the early 1990s, research relevant to planar magnetic components' design, modelling and optimization has emanated [71]. Recently, accelerated development of PCB technology and exploration of attaining miniature power converters with integrated PCB windings stirred far-reaching international attention and industrial and academic fields [72]–[75].

Planar wound structures are commonly manufactured by laminating planar copper windings and dielectric sheets into multilayer PCBs that are confined with a low-profile magnetically permeable core [76] as illustrated in figure I-15. These transformers are renowned for the following incentives: low profile, light weight, consistent manufacturing, high power density, distinguished repeatability, greater operating frequency in comparison to wire wound transformers and predictable parasitics [68], [77]. In opposition, planar magnetics encounter some restraints in terms of large surface area, low copper fill factor, limited number of turns and high winding capacitance.



(a) (b) (c)

Figure I-15: Comparison of magnetics: (a) conventional structure; (b) planar structure; (c) Unfastened view of a multi-layer PCB planar transformer

B.3.1 Galvanic Isolation: Pulse Planar Transformers

Integrated magnetics with planar cores and PCB technology verified to be efficient in improving dc-dc converter efficiency while reducing size, weight and cost. In particular, pulse planar transformers are commonly used in medium to high power applications, as they comprise low capacitive coupling between primary and secondary circuits, however, they require dedicated electronic schemes for shaping their transmitted pulses. Characterized with low profiles, 25-50% less than wire-wound transformers, makes them attractive in applications such as automotive and aerospace or aeronautics where volume and weight are superior discriminatory aspects [76]. Henceforth, pulse transformers where the preferred galvanic isolation providers in the gate driver card examined at IETR lab exemplified in figure I-16, as they are one of the prevailing solutions utilized to drive power semiconductors in half-bridge configurations. This is achieved by the passage of positive or negative pulses on the primary winding of the pulse planar transformer invoking either an activation or blockage of the connected power semiconductor devices, respectively.

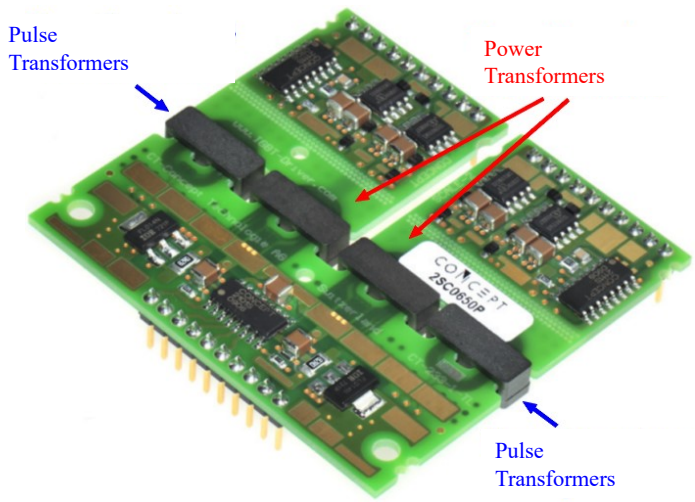
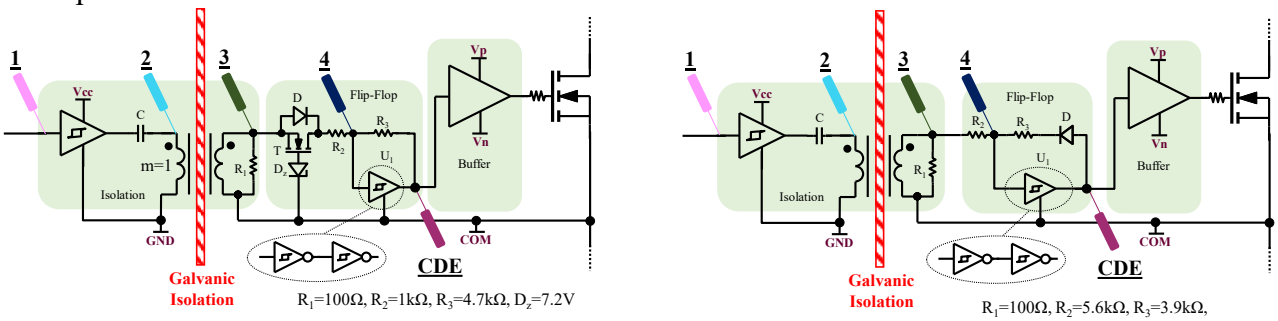


Figure I-16: Half bridge representation of a 2SC0650P gate driver card with pulse planar transformers

As reflected in figure I-16 above, for a half-bridge gate driver card regulating two semiconductor devices, there exists four planar transformers of which each channel comprises a transformer dedicated to excite the electronic circuitry and the other is committed to authorize the switching of power semiconductors by the transmission of triggering positive or negative impulses. An exemplary

of conventional pulse transmission through galvanic isolation circuits are depicted in figure I-17 below [47], [52]. A serial capacitance is connected to the primary side to prevent DC magnetic field in the pulse transformer which can lead to core saturation.



(a) (b)

Figure I-17: Conventional pulse transmission circuits: (a) Infineon 2ED300C17; (b) Semikron's SKYPER32RPRO [52]

B.3.2 Dielectric Material

Two planar layers of conductive windings are sandwiched and integrated in a dielectric material to provide proper insulation. This is because there are safety standards that impose minimum distance between windings. A typical dielectric material for PCB manufacturing is Flame-Retardant #4, known as FR4, a composite material produced from woven fiberglass bond with an epoxy resin. FR4 material standards display an electric strength (breakdown voltage) extending to 40 kV/mm. Consequently, for offline power converters at least 0.1 mm of distance between primary and secondary windings is enforced to meet safety standards. Therefore, the copper fill factor on a PCB board is highly associated with the dielectric material elected. This issue is ameliorated with the rapid progress and enhancement of dielectric materials. For example, copper on a thin flexible polymer substrate (2MV/mm dielectric strength) gives an exceptional fill factor, where dielectric thickness can be made as low as 13 µm. Hence, several single-layer flexible polymer substrates can be laminated together as a multiple-layer flexible PCB.

Moreover, a significant issue needs to be highlighted when discussing this aspect of a planar transformer. A dielectric material sandwiched by two conductive layers creates an embedded capacitor. High or low dielectric permittivity can then be selected as desired. FR4 substrate, is a common insulator material exploited in PCB manufacturing that is featured with a lower dielectric constant (DK). This material is relatively thick, leading to lower capacitance values. Lately, several companies such as 3M, Isola and Rogers supply high DK capacitive materials convenient for PCB manufacturing [76].

For the past few years, IETR laboratory has been concerned and involved with several researches and studies relating to the control of power semiconductor devices, specifically SiC MOSFETs, which has been the investigation of former realized theses and examinations [33], [50], [78], [79]. Pursuing the journey, and with an ultimate aim to advance gate driver topologies, this thesis will accentuate on vital and critical constituents of gate drivers; pulse transformers, intending to further investigate and ameliorate those components.

C. ELECTROMAGNETIC COMPATIBILITY COMPLIANCE

"Medical technicians taking a heart-attack victim to the hospital in 1992 attached her to a monitor/defibrillator. Unfortunately, the heart machine shut down every time the technicians turned on their radio transmitter to ask for advice, and as a result the woman died. Analysis showed that the monitor unit had been exposed to exceptionally high fields because the ambulance roof had been changed from metal to fiberglass and fitted with a long-range radio antenna. The reduced shielding from the vehicle combined with the strong radiated signal proved to be too much for the equipment" [80].

C.1 Interpretation of EMC, EMI, EME and EMS

With broad dispersion of electronic devices, it is essential that these devices can function adequately in a perplexing electromagnetic environment. Hence, EMC is a critical, significant characteristic of electronic devices. EMC, as defined according to International Electrochemical Commission (IEC) is "The ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment" [81]. Currently with the emergence of highly efficient switch mode power supplies (SMPS), adhering to EMC standards is a necessity. A competent electronic device is well known to be electromagnetically compliant; this is accurate when the component is fresh. However, with operating time, electronic components mature and degrade where aging problems might cause a considerable fluctuation of the EMC level [80].

Electromagnetic interference (EMI) is the deterioration of proper functioning of an equipment, transmission channel or system due to an electromagnetic disturbance. Electromagnetic signals can propagate in electrical and electronic systems by conduction or by electromagnetic field radiation. It is imperative to clarify that the term radiated interference includes two phenomena particularly, near field coupling and far field radiation. With the presence of EMI, there exists at least one source originating troublesome emissions (possible conducted, near field coupled or far field radiated) and perhaps, one or more EMI victim(s) which for several reasons is (are) sensitive to the emerged disturbance. Thus, electromagnetic emission (EME) is denoted by the electromagnetic energy originated from a source. Lastly, electromagnetic susceptibility (EMS) is the inefficiency of a device, circuit or system to operate without deterioration in the presence of electromagnetic disturbance. Susceptibility is interdependent to immunity, the latter defining to what degree EMI can be introduced to a system before deficiencies start to occur. Figure I-18 below demonstrates the common terminologies used in this field and their correlation [82]–[85].

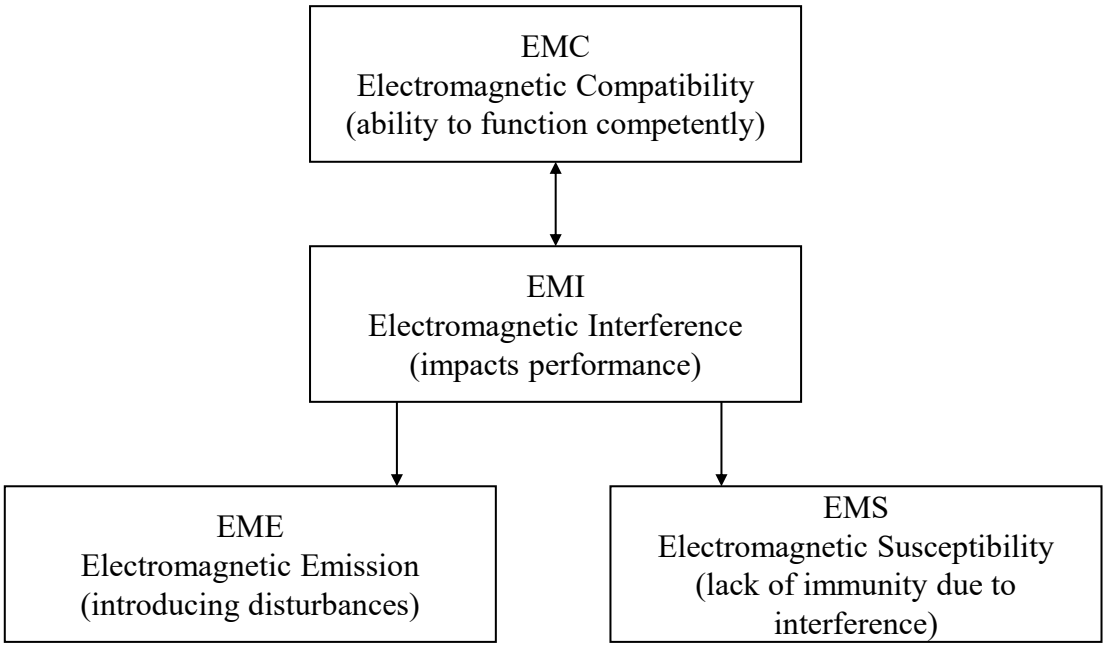


Figure I-18: EMC vocabulary and their interdependence

Additionally, as stated in the definition of EMC to "fiction satisfactorily" can be instinctive, thus the standard IEC 62132-1 proposed performance classes as presented in table I-3 to classify the performance of electronic equipment in immunity tests [86].

Table I-3: Performance classifications of an electronic system [86]

Class	Explanation
A	Normal performance within specification constraints
B	Momentary degradation or loss of function or performance which is self-reparable
C	Momentary degradation or loss of function or performance which compels operator intervention or system restart
D	Deterioration or loss of function due to damage or loss of data

C.2 Categorization of EMI in Power Converters

It is approximated that the supremacy of electricity generated in developed nations, namely 90% of generated power is being controlled through power electronic circuits before being sent to the utility [87], [88]. As previously stated in the introductory section, power converters, which are electronic circuits that fundamentally comprise power semiconductor switches, magnetic elements and energy storage components are the core of power conversion systems. Moreover, the urge to meet high power density demands merged with the evolution and commercialization of WBG semiconductor devices, permitted elevated operation of power converters at higher switching frequencies that are associated with their faster switching speeds [89], [90]. Nevertheless, the convenient aforementioned realizations become paradoxical when they reinforce the concern of

conductive EMI [34], [91]–[94]. This phenomenon can be a destructive agent of power converters. Figure I-19 reveals typical natural and man-made EMI sources [95].

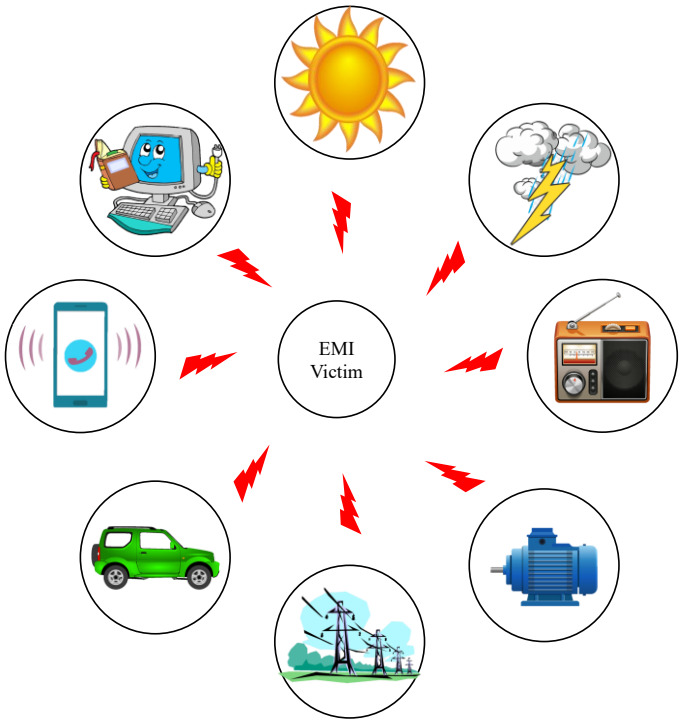


Figure I-19: Standard EMI sources

EMI disturbance in electrical circuits is classified as either radiated or conducted as portrayed in figure I-20 having alternative noise propagation paths. Moreover, the conducted EMI noise is further decoupled into common-mode (CM) noise and differential mode (DM) noise as categorized in figure I-21. Diversified methods have been discussed in literature to mitigate EMI sources and adhere to EMC standards, typical examples are: EMI filter, EMI shielding, soft switching, random modulation and chaotic PWM control [96], [97]. Radiated and conducted EMI are distinguished based on the operational frequency, EMI coupling route and electromagnetic field propagation.

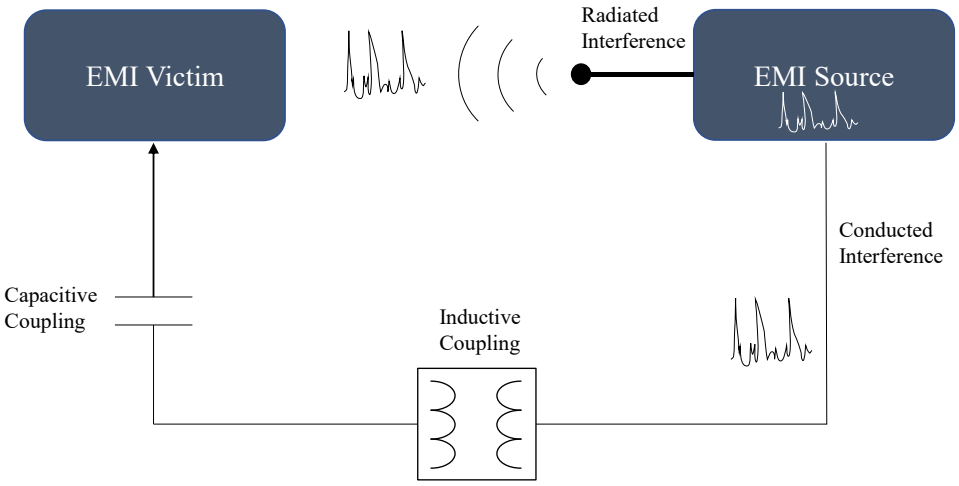


Figure I-20: A representation of EMI coupling path in electrical circuits

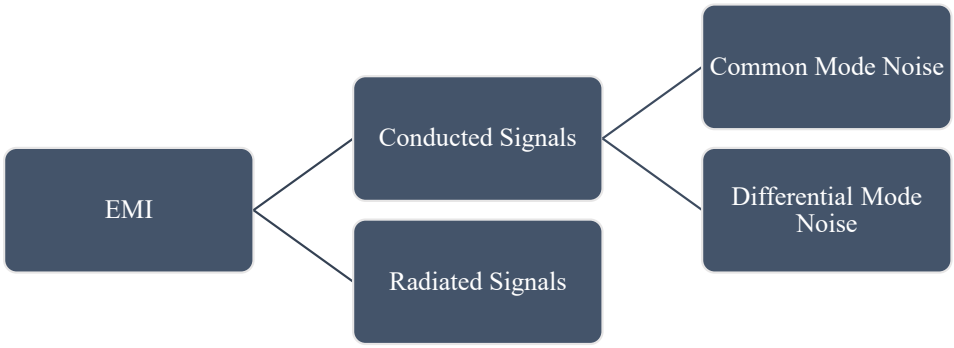


Figure I-21: Classification of EMI signals in electrical circuits

C.2.1 Conducted Signals in Electrical Circuits

The expected generation of signals for information transmission is not regarded as noise, even though it influences the overall EMC of electronic devices. The targeted concern of this thesis is on the unwanted conducted noise signals which are identified thereafter. Conducted emission is segregated into CM and DM according to noise propagation [98]–[100].

C.2.1.1 Differential Mode Noise

Noise can occur between any two lines of an electrical circuit, such as phase and neutral, two-phase lines and from plus to minus in DC systems. This noise is well-defined as DM noise or symmetrical noise. It appears on two conductors of a closed loop with equal and opposite polarity. It is a consequence of parasitic components in electrical circuits, such as equivalent series inductance or equivalent series resistance. It usually exists at lower frequencies in an electronic system, and is commonly relevant in SMPSs or motor drives.

C.2.1.2 Common Mode Noise

Noise can likewise be conducted from any line in an electrical circuit towards earth. Unlike DM noise, it flows in all lines in the same direction and then towards earth. CM noise mainly results due to the presence of stray or parasitic capacitances in an electrical system. Figure I-22 depicts a general representation of the propagation of DM and CM noise in an electrical circuit [100]. It is imperative to declare that the CM noise is sophisticated to suppress when compared to the DM noise, due to its complicated conduction paths impacted by stray inductive and capacitive parameters, and hence will be targeted in this dissertation.

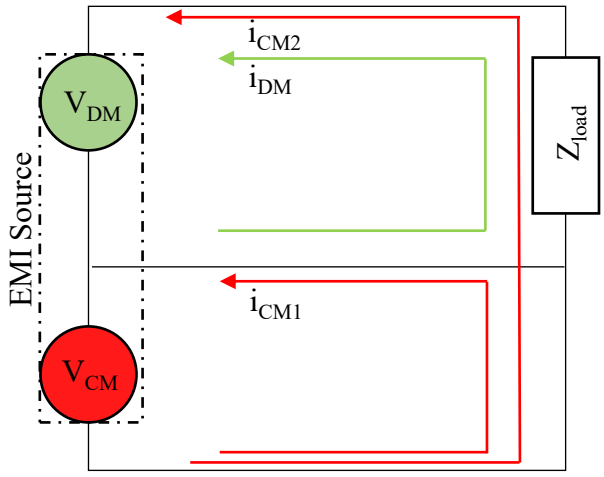


Figure I-22: Conducted DM and CM propagation in an electrical circuit

C.3 EMC Challenge: Pulse Transformers in Gate Drivers

The interpretation of EMI noise is essential to validate compliance with international and regional standards such as Federal Communications Commission (FCC), CISPR 11 [101] and CISPR 14 [102] that restrict the generated conducted emissions in the frequency range between 150 kHz and 30 MHz. With the prevailing research towards attaining high power density demands, the switching frequency of carrier signals stretch from several 100 kHz reaching several MHz. Furthermore, the fast switching transitions that are feasible with contemporary WBG semiconductors, generates consequential high-frequency spectral components [103], [104]. Hence, EMC conformity is crucial when designing gate driver circuits.

Applications which necessitate a blocking voltage of 1.2-10 kV are principally dominated by SiC MOSFETS featuring its small On-state resistance. Meanwhile, gate drivers are commercially available with a blocking voltage of 650-1700 V, there are scarcely any commercial gate drivers for 10 kV MOSFETs due to their accompanying challenges [105]. Beneficial high switching realizations become disturbing due to the occurrence of high switching transitions known as dv/dt, amounting to 100 kV/µs, which enforces a requirement for very nominal isolation capacitance in gate driver circuits [106], [107].

As mentioned earlier, gate drivers principally contribute to two functions which include signal transmission and power transmission. Signal transmission, utilized as an isolated pulse planar transformer in the gate driver at IETR lab which is a prevalent solution for galvanic isolation, is one of the most crucial aspects when composing a gate driver that controls SiC MOSFETs. Since, the existence of substantial potential variation due to switching, induces the passage of CM currents in gate driver circuits, mainly through interwinding capacitances of planar transformers [108]–[110], generating problematic electromagnetic disturbances that shall be firmly examined [111], [112]. The significant awareness targets pulse planar transformers, since the functionality of power transformers in gate driver circuits is to supply the electronic circuitry, thus, passage of CM currents through the latter does not impose unfavorable consequences on the reliability of the semiconductor device. However, pulse transformers are responsible for executing switching orders for exciting or blocking

power semiconductor transistors. Where, a steep dv/dt occurrence might provoke faulty or invalid switching orders due to the passage of CM currents as revealed in figure I-23, leading to adverse results such as the occurrence of a short circuit branch. Additionally, the gate driver placed adjacent to the power semiconductor devices, positions the driver to operate in a highly disturbed electromagnetic environment due to strong variations in current (di/dt), subjecting it to high electromagnetic stresses.

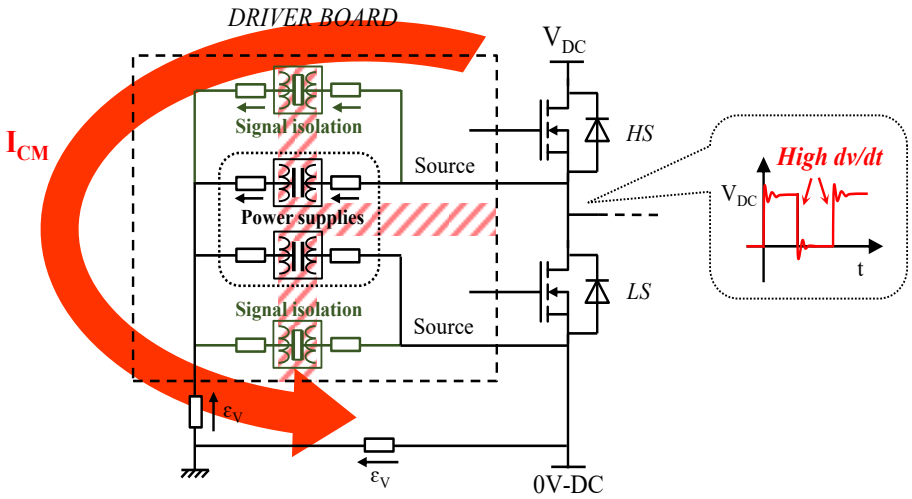


Figure I-23: Common mode current modelling through galvanic isolation of gate driver boards[78]

C.4 Standards and Regulations

To manufacture a functional and reliable PCB design there are steady standards to accomplish a favorable outcome. Abiding by IPC standards is the direction to a successful design. In 1957, the IPC was established and was known as the Institute of Printed Circuit, which currently encompasses manifold companies that are associated with PCB design supply chain.

IPC develops and preserves standards that serve as a shared guideline for PCB design manufacturing, molding, assessing and other areas of concern. Hence, PCB designers adhering to the designated IPC standards for PCB layouts plays an important role in the component's performance.

C.4.1 PCB Optimal Assembly

IPC has identified various standards that guarantee design reliability and fabrication guidelines. The prerequisite of designing a PCB, is the interpretation of IPC-2221 standard. This norm serves as a generic standard that comprises every aspect of a PCB design [113].

Among various PCB standards, one significant assortment governs creepage and clearance distances between adjacent conductors on a PCB. Thus, safeguarding the design and fabrication of electrostatically safe products, exclusively for those operating at high voltages.

Besides IPC-2221, there are several known standards that define clearance and creepage distances in a PCB such as IPC-9592B, UL-61010-1 and UL-60950-1 (second edition). Having the designated relative standards stated and characterized, it is time to prescribe and illustrate the difference between creepage and clearance distances on a PCB. As a definition, clearance distance is the shortest distance

through air between two conductive parts, whereas creepage distance refers to the shortest distance along the surface of a solid insulating material between two conductors [114], [115] as depicted in figure I-24 below.

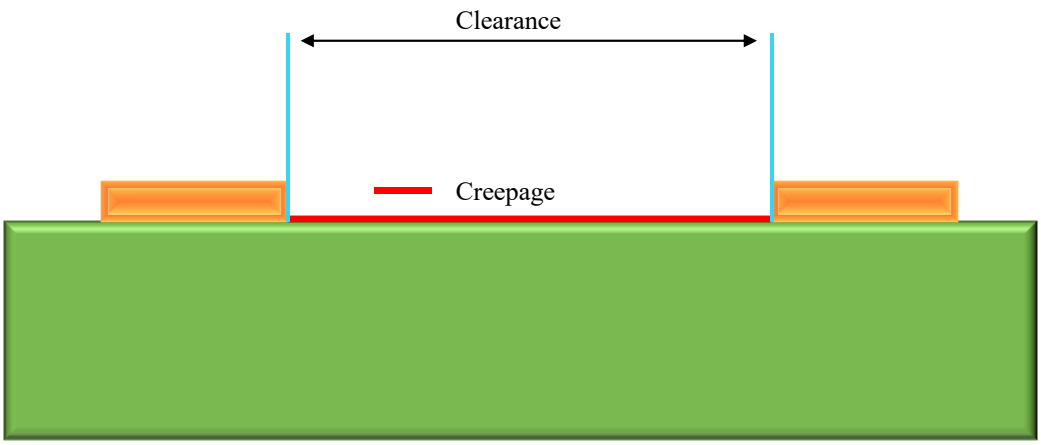


Figure I-24: Creepage and clearance distance identification on a circuit board

IPC2221A [116] is a collective standard that designates creepage and clearance distances, where the limits are further specified in IPC2221 and defined according to DC or AC peak voltage level as presented in figure 25, substrate material, limits for conductors on internal layers and the necessity of coating conductors on external layers. IPC-9592B is explicit in defining clearance and creepage trace requirements in power conversion devices operating above 100 V.

Voltage between conductors (DC or AC peaks)	Minimum spacing (mm)						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05	0.1	0.1	0.05	0.13	0.13	0.13
16-30	0.05	0.1	0.1	0.05	0.13	0.25	0.13
31-50	0.1	0.6	0.6	0.13	0.13	0.4	0.13
51-100	0.1	0.6	1.5	0.13	0.13	0.5	0.13
101-150	0.2	0.6	3.2	0.4	0.4	0.8	0.4
151-170	0.2	1.25	3.2	0.4	0.4	0.8	0.4
171-250	0.2	1.25	6.4	0.4	0.4	0.8	0.4
251-300	0.2	1.25	12.5	0.4	0.4	0.8	0.8
301-500	0.25	2.5	12.5	0.8	0.8	1.5	0.8
> 500 (mm/V)	0.0025	0.005	0.0025	0.00305	0.00305	0.00305	0.00305

- B1: Internal conductors
- B2: External conductors, uncoated, sea level to 3050 m
- B3: External conductors, uncoated over 3050 m
- B4: External conductors, with permanent polymer coating (any elevation)
- A5: External conductors, with conformal coating over assembly (any elevation)
- A6: External component lead/termination, uncoated, sea level to 3050 m
- A7: External component lead/termination, with conformal coating (any elevation)

Figure I-25: Minimum conductor spacing as a function of voltage[3]

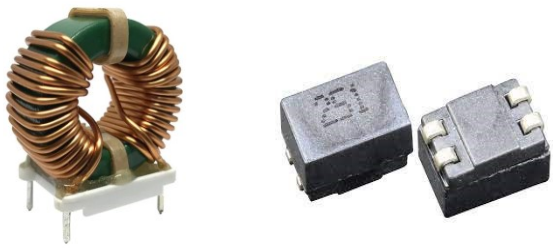
[3] https://resources.altium.com/p/using-an-ipc-2221-calculator-for-high-voltage-design

D. CM NOISE REDUCTION TECHNIQUES IN SMPS

D.1 Overview

The presence of CM noise contributes to significant EMI challenges that demand compelling awareness when designing highly efficient SMPS. An assortment of noise suppression strategies must be implemented in many power-supply designs to conform to EMC requirements. Literature reports several typical methods used to minimize CM noise in SMPS and are conferred hereafter.

The employment of CM noise filters is widely discussed and examined to mitigate CM noise. According to Shih and Chen [117], this is associated with prolonged designs which are conventionally used in SMPS. To attain sufficient EMI suppression, bulky CM noise filters are needed. Massive filters are not preferable nor profitable especially with the trend towards high power density demands. Damnjanovic et al. [118], [119], confirmed the significance of minimizing the size of the CM choke filter and suggested surface mount device (SMD) CM models [120]. Despite their miniature size, these devices are only effective above 1MHz, leaving the noise below this range unsuppressed. This frequency constraint is also shared with large CM chokes and Roc'h et al. highlight the importance of this issue [121], [122]. Moreover, active CM filter designs to further reduce CM noise were investigated by Mortensen and Venkataramanan [123]. In spite of the greater flexibility offered to fine-tune these filters, they are not easily designed and the gained bandwidth product is extremely restricted by the active components. Active EMI filters (AEF) are also examined in recent researches [124], [125]. Figure I-26 below exposes the difference between bulky CM chokes and SMD CM designs.



(a) (b)

Figure I-26: CM filters (a) Conventional bulky design; (b) SMD design

A diverse method is to diminish parasitic coupling capacitors from the primary to the secondary winding. This strategy leads to high leakage inductance and is inefficient [112]. Additionally, bypass capacitor connection across the primary and secondary sides was examined by Chen et al. in [126], where the impact of this Y-capacitor on CM noise conduction was assessed. However, this capacitance is restricted due to safety standards and cannot produce a reasonable impedance to avoid all of the routed CM noise current. Passive cancellation approaches or balance techniques can also be exploited to reduce CM noise, however, they require supplementary passive components and are very delicate to component and circuitry tolerance [127].

One of the most effective techniques to suppress CM noise is faraday shielding. This method requires proper installation and integration of grounded conductive sheets into the transformer as it

can be automatically embedded in a PCB assemblage process specifically if PCB winding is utilized, aiming to define a route for CM current [112], [128]–[135]. This technique holds remarkable significance to resolve the planar pulse transformer problematic which was previously discussed in section C.3, and will be thoroughly further discussed and examined subsequently in this thesis.

D.2 Faraday Shielding Insertion Mechanisms

An electrostatic screen, known as a faraday shield, is commonly used in planar transformers to counteract the capacitive coupling linking the primary and secondary windings, facilitating the path for CM current flow. This shield, a conductive element, is connected accurately to a defined reference potential, aiming to suspend or reduce the coupling capacitance between the windings and consequently the EMI, and define a path for the CM current circulation as portrayed in figure I-27 below [131].

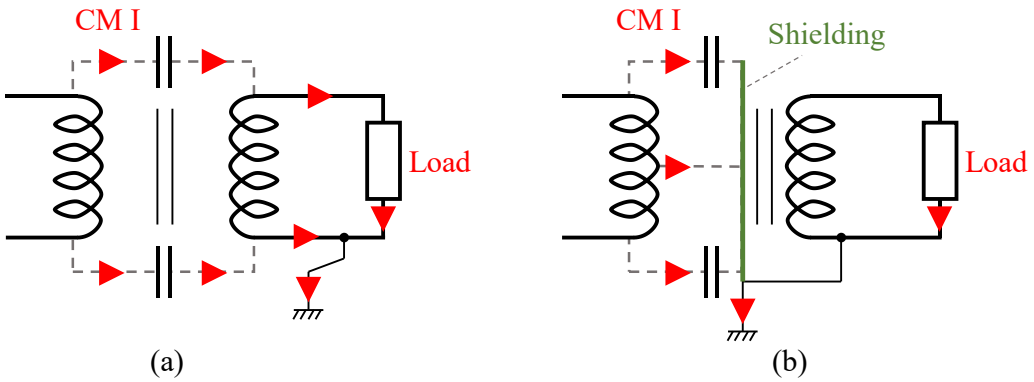


Figure I-27: CM current path in transformer (a) without shielding; (b) with grounded electrostatic shield

D.2.1 Convenient Shielding Designs

D.2.1.1 Single or multi-Shield

A single-shield isolation operates sufficiently to suppress CM interference on the primary side at low frequencies reaching 100 kHz by maintaining isolation of the order of 120-140 dB. However, this becomes problematic when dealing with DM interferences. The undesirable potential differences between any two current-carrying conductors can pervade the shielding as single shielded isolated transformers do not adequately suppress DM noise. With increasing frequency, exceeding 100 kHz, CM rejection decreases as the capacitive reactance between the primary and secondary windings decreases [136]. Therefore, multi-shield isolation transformers are utilized to suppress both conducted interferences, CM and DM noise, as illustrated in figure I-28. This implementation shall be handled with awareness whilst considering to sustain proper magnetization between the windings.

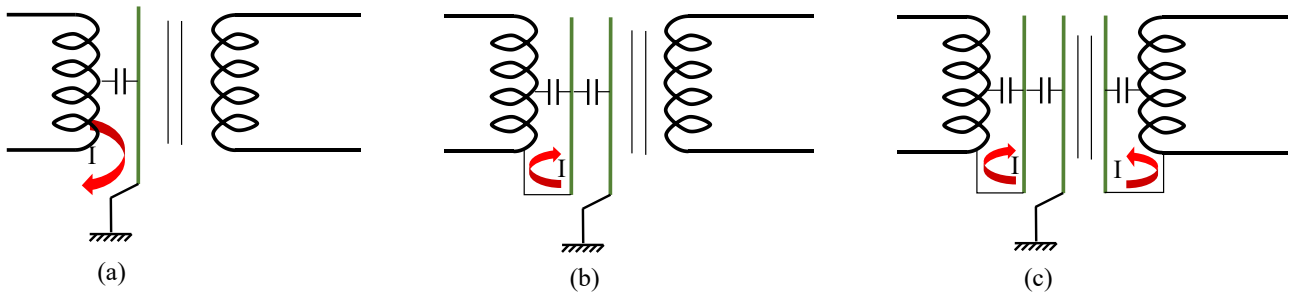


Figure I-28: Shielded isolation transformers (a) single-shield; (b) double-shield; (c) triple-shield

D.2.1.2 Novel Shielding Designs

Distinctive shielding designs were discussed in literature revealing different methods of shielding high frequency planar transformers (HFPT). A series shielding method was invented by Park [137], where the primary winding comprises three layers, whereas the secondary winding consists of one layer. The primary winding is divided into two parts, of which one part is normally winded P_1, P_2 and the other part P_3 is a shielding winding that is made identical with the secondary winding but connected in series with the primary winding. Hence, displacement current flows in the primary winding and does not contribute to CM noise as the shielding and secondary winding share the same voltage potential, assuming linear voltage distribution along the windings, as revealed in figure I-29. The limitation of this technique is that any misalignment will cause potential difference and its ineffective in mass production.

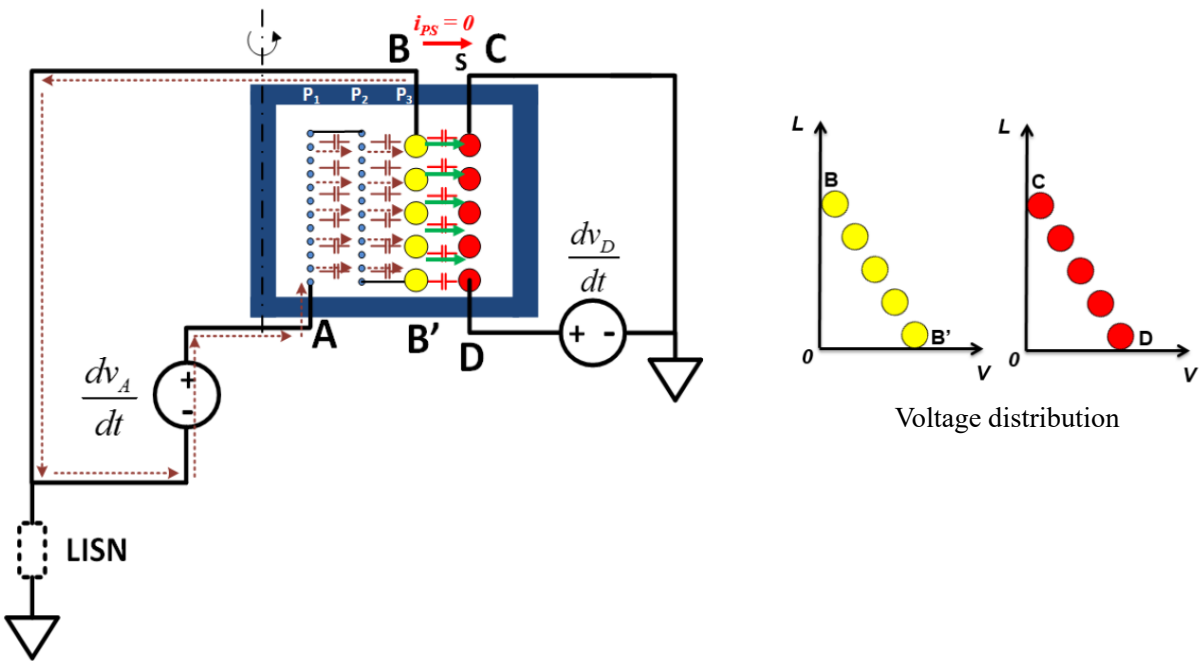


Figure I-29: Series shielding method [138]

A partial shielding method is also introduced in literature, where a section of the winding is shielded and the other is left unshielded, thus, reducing the shielding width as demonstrated in figure I-30 (a). Accordingly, in the unshielded sector, the voltage of the primary is greater than that of the secondary,

triggering the displacement current i_1 to travel from the primary to secondary. Similarly, but contrarily this occurs for displacement current i_2 flowing from the secondary to primary. This forms two parasitic capacitances C_{AC} and C_{BD} respectively, where the values can be modified by altering the length of the shielding with an objective to attain $i_1 = i_2$ as demonstrated in figure I-30 (b). Hence keeping this method confined to trial-and-error technique and is surely ineffective in mass production.

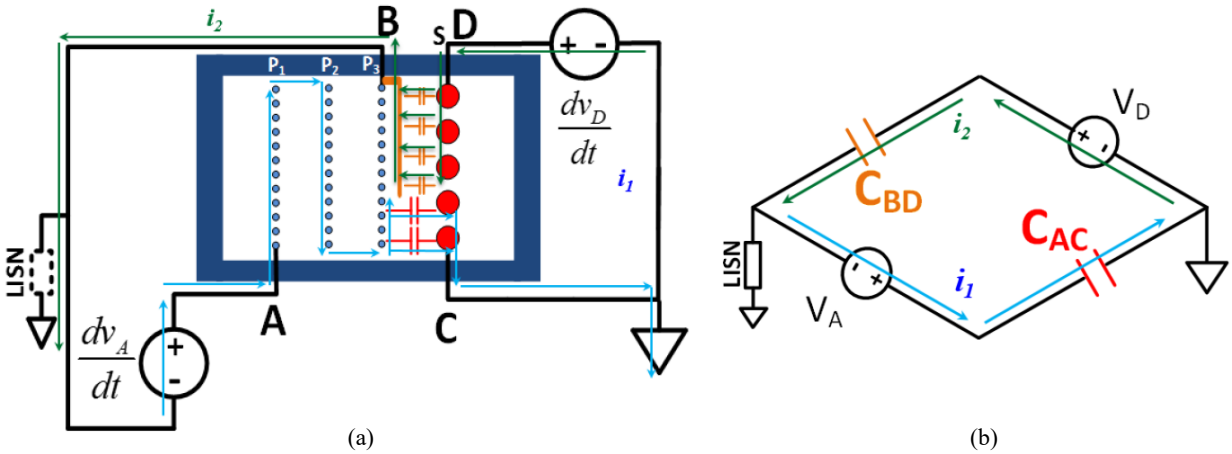


Figure I-30: Partial shielding method (a) configuration; (b) CM noise model [138]

Yang in [138], demonstrated a shielding technique where the shielding is connected to the primary side and aligned to the secondary with 180° rotation, making it easier to connect the shielding with the primary ground and avoiding the utilization of jumping wires. This method indicates that on one half the voltage of the secondary winding is higher than the shielding, and on the other half it is reversed as presented in figure I-31 below. Hence with two identical currents of opposite polarity, no CM noise current will flow across the windings.

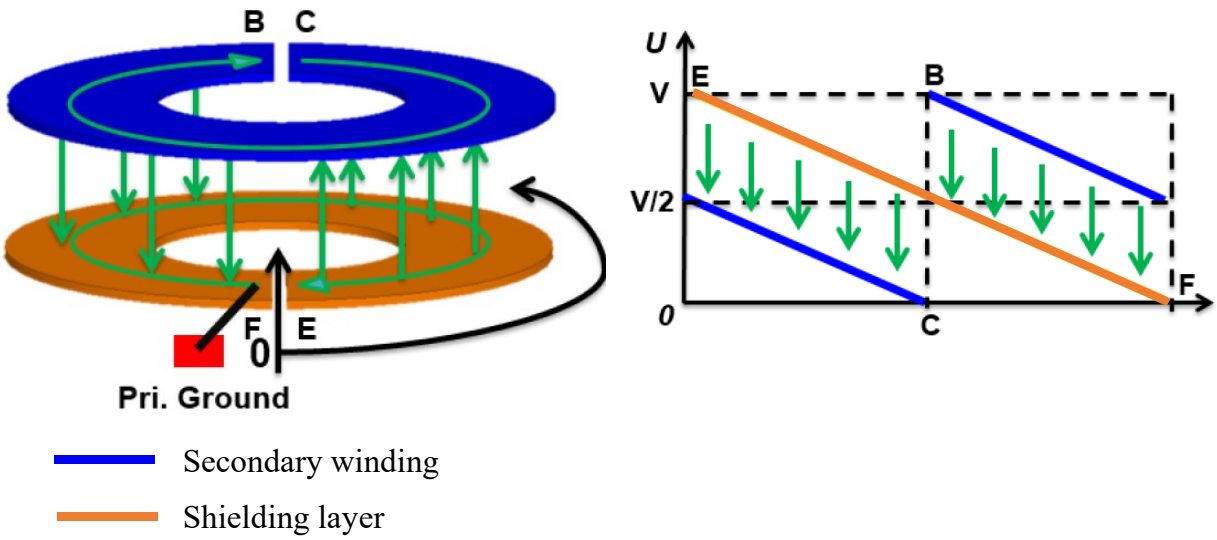
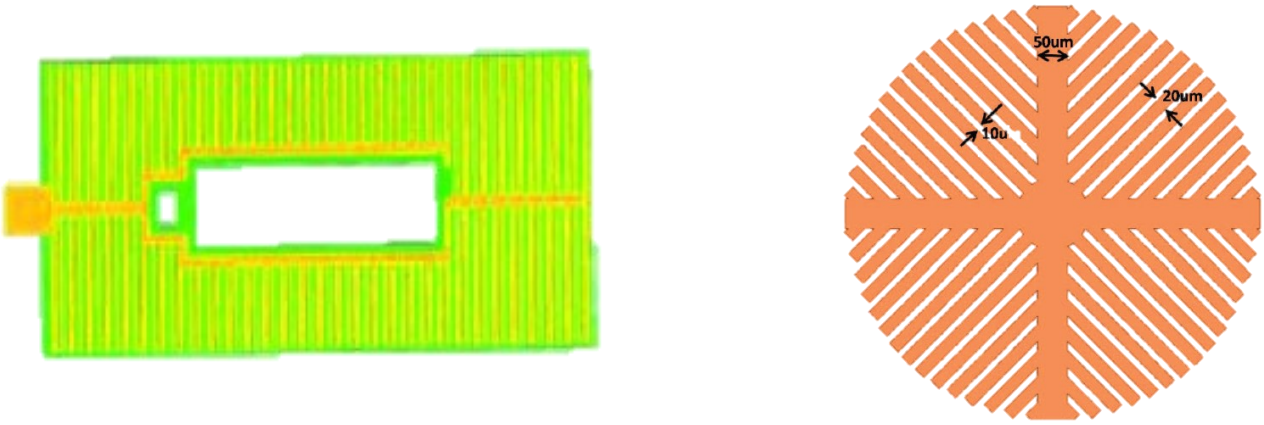


Figure I-31: Shielding layer aligned to secondary and rotated by 180 degrees [138]

With a similar concept, Fei et al. [132] demonstrated a shielding layer rotated at 270° and aligned to the secondary, intending to decrease the PCB footprint and minimize interference between primary windings and output terminals.

Moreover, intending to provide capacitive shielding whilst sustaining the magnitude of the magnetizing inductance, Lu et al. [136] and Wu et al. [135] have both discussed the advantages of implementing comb-shaped and patterned faraday shielding techniques, respectively, as depicted in figure I-32 below.



(a) (b)

Figure I-32: Novel faraday shield (a) comb-shaped [136]; (b) patterned [135]

D.3 Numerical Analysis

To estimate the performance of designed transformers, 1-D analytical methods are not relevant nowadays due to the efficiency and precision needed when modeling and analyzing these delicate devices. The certainty of 1-D analytical technique further decreases with complex geometrical structures. Essentially, most engineering problems are extremely complicated, and their resolution necessitates simplification and approximation. Thus, this will render to attain imprecise results that are not reliable. Formerly, this method was widely utilized du to the limitation of computational technology, where most of the transformer designs were based on manual calculations. Nevertheless, the advancement of computational technology, recurrent calculations and sophisticated computation processes can now be programmed, providing solutions in adequate intervals.

There are diversified numerical methods available in alternative fields and applications; of which Finite Element Method (FEM) is one of the most prominent numerical techniques incorporated with progressive computational technology. The FEM is a numerical method employed for solving partial differential equations and integral equations. In addition, its an effective tool when solving problems with many variables. The principle of behavior of the aforementioned tool is to segregate or partition the analyzed component into finite number of elements. Each element can be represented in diversified shapes, such as line, triangle, circular, rectangle, polygon etc. Moreover, each element will be appointed with a corresponding mathematical equation and boundary conditions prior to

analyzing the project. The eventual results are collected by computing the solutions of the overall global elements [139].

A Renowned collection of FEM tools will be utilized in this thesis to analyze, model and investigate the intended pulse planar transformer, and the process will be rigorously and unprecedentedly identified in Chapter II.

E. CONCLUSIONS

To accomplish upgraded power converter designs, researchers are always faced with challenges and obstacles as optimization is invariably valuable. The progressive upsurge in the field of power converters and semiconductor devices is the framework of the modern industrialized district. Thus, resilient power electronic systems are demanded in alternative fields of application. With a soaring urgence to attain high power density ratings, power semiconductor device technologies earned phenomenal progress, particularly in their switching frequency capabilities. This significant anticipation became effective with the emergence of WBG semiconductor materials, which qualified the devices to operate at exceptional frequencies. This realization gained immense publicity in the market, particularly in PCB-based gate driver applications of power electronic systems, which integrate upgraded planar technologies. To satisfy galvanic isolation requirements, pulse planar transformers in gate driver cards are renowned for competently driving power semiconductor switches, particularly SiC MOSFETs. Nevertheless, there is a tariff for optimization. The favorable rapid switching speed attainment by the utilization of WBG technology, leads to the occurrence of critical dispersed conducted electromagnetic disturbances, mainly classified as CM currents in gate driver circuits. This primarily demands accurate awareness when designing pulse transformers in gate driver cards as they are responsible to invoke semiconductor switching orders.

Various studies have been conducted to mitigate the CM noise occurrence in planar transformers, of which, the insertion of grounded electrostatic screens is certainly eminent and acknowledged amongst many researchers. This is necessary to safeguard EMC standards in the design of the whole gate driver card and ensure its reliable operation.

CHAPTER II: NUMERICAL ANALYSIS APPROACH

Examining and analyzing electromagnetic effects and occurrences to understand and interpret the efficiency of interconnects, integrated circuits and PCBs requires competent and dynamic software tools. As formerly stated in Chapter I, IETR laboratory team managed to design and fabricate, pulse planar transformers that integrated two adequately grounded faraday shielding layers based on their competency and proficiency in this field. The specifications of the transformers along with their shielding designs will be particularly presented in Chapter III conferring further analysis.

This chapter will set the course and trail that was conducted to lay a concrete foundation of the simulation analysis procedure pursued to validate and reinforce the earlier attained experimental results. The primary objective is to conserve time and expenses, whilst defining a roadway for impending developments. Thus, this chapter will accurately and unprecedentedly expose precise guidelines of the modelling chain utilized comprising collective software tools, originating from the creation of the design and finalized with an attainment of an equivalent circuit model of the designated pulse transformer.

A. EMC MODELLING

A.1 State-of-the-Art

EMC standards are regarded as the ethics of designing power converter systems and their respective constituents. Thus, vital consideration should be taken respecting the aforementioned standards at an early stage, especially, before fabrication. This is achievable by virtual prototyping of the design before reaching the physical manufacturing stage. The adherence to EMC standards is precisely relevant to the components arrangement and the parasitic elements of the designed model [140]. As previously stated, CM currents are generated as a result of the existence of parasitic capacitances and abrupt potential variations. Henceforth, the design and routing of components has a severe influence on the conducted emissions [141].

Competent and precise circuit models of power electronic components are essential for EMC simulations of power electronic systems. This section will reconsider the state-of-the-art in high-frequency modelling of all EMC-related power electronic constituents, such as chokes with non-linear magnetic cores, long cables, motors, resistors and capacitors, PCBs and construction and power semiconductors [142]. Some aspects are beyond the scope of this thesis, but will be concisely discussed to integrate the power electronic system, of which one explicit modelling technique will harmonize with the outlook of this dissertation.

Component modelling can be typically categorized into two broad types: physical or behavioral modelling [143], [144]. Physical modelling relies on elementary laws of physics, such as Maxwell equations. The dimension and electromagnetic characteristics of the component are necessitated permitting analytical or numerical techniques to formulate the equations and create an equivalent

circuit model. On the other hand, the behavioral modelling, does not require the aforementioned information and rather utilizes measured impedances of a component in alternative connection schemes to reproduce an equivalent circuit model that replicates its behavior.

A.1.1 Choke Modelling

Discussed earlier in Chapter I, EMI filters in power electronic systems constitute passive elements with inductors, termed chokes, aiming to reduce both CM and DM EMI disturbances. Since the frequency characteristics of chokes might be much different when operating at high frequencies due to parasitic parameters and leakage inductances, precise high frequency models are therefore critical when conducting EMC simulations.

A.1.1.1 Physical Model

Physical models rely on analytical and numerical approaches, or a merger of both, it exploits the geometry and the electromagnetic characteristics of the choke's windings and the core, which are feasible from datasheets or individually measured. Analytical equations aid in estimating the magnetic fields inside the magnetic core and in the air, in addition to the electric fields between windings and between windings and the core. These computations are employed to develop an equivalent circuit model of the choke [145]–[147], inclusive of leakage inductances [148], [149] and parasitic inter and intra winding capacitances [150]–[154]. These techniques can be sufficiently used to reform CM choke geometry and core materials [155].

Numerical methods depend on various numerical techniques to resolve Maxwell's equations for the whole choke model or elements of it. This technique includes Finite Element Method (FEM) [156], [157] or 3-D Partial Element Equivalent Circuit (PEEC) method linked with boundary integral method (BIM) [158]. This modelling technique is convenient for choke design and frequency-domain analysis.

A.1.1.2 Behavioral Model

Behavioral choke models can be additionally associated into two sub-divisions [144], [159]. The first classification comprises behavioral models of circuit schemes that reflect the physical effects inside the choke. The second sub-division is a black-box behavioral model, developing circuit topologies that are irrelevant to the choke's internal physical effects, however, precisely recreating the measured behavior at its terminals. A black box behavioral model can be attained using alternative connection strategies using spectrum analyzer [160], [161], impedance analyzer [162], or vector network analyzer (VNA) [163], [164]. The parameters of the equivalent circuit models (with either fixed or variable studies) are withdrawn from measurements by iterative analytical formulas, and/or optimization methods to conform the measured data, for example, rational function estimations [165], vector fitting [164], [166], [167], and transformative algorithms [143].

A.1.2 Multiconductor Cable Modelling

Power cables that are relatively long where their lengths significantly surpass the operating wavelength, can be modelled as multi-conductor transmission lines. This is because high consideration must be taken when handling many frequency-dependent characteristics, including parameters such as skin and proximity effect, dielectric losses and transmission line propagation [168].

A.1.3 Motor Modeling

Physical modeling of motors necessitates electromagnetic field analysis drawn from 2-D or 3-D FEM to construct equivalent circuit models [169]–[171]. This approach requires full information concerning geometry and material permitting definite EMC analysis and design of the motor. Differently, behavioral modeling requires real motor measurements to compose an equivalent circuit model that replicates the motor impedances. They are usually measured using an impedance analyzer placed on a motor in alternative connection schemes. The circuit elements are withdrawn from the measurements and constructed as per pre-determined equivalent circuit topologies mimicking the behavior of the motors [172]–[174], or general circuit layouts relying on function approximations [175] and vector fitting algorithm [176]. Moreover, an incorporation of FEM and behavioral modeling may also be implemented to enhance and calibrate the model parameters [177].

A.1.4 HF Capacitor and Resistor Models

A basic series RLC equivalent circuit can accurately represent impedance curves of roughly all types of capacitors. The RLC parameters can be realized from hardware measurements such as vector network analyzer, or software fitting tools such as Matlab Zfit. This analysis can be very beneficial when selecting capacitors, primarily to damp certain resonance occurrences [142].

A.1.5 PCB and Interconnects

The impact of PCBs and interconnects is very critical when analyzing EMC in power electronic circuits, especially when considering their parasitic effects [173], [178], [179]. This particular approach is the main objective of this thesis, as the PCB parasitic elements can facilitate the CM currents and thence, EMI disturbances, which will be further emphasized subsequently. The extraction of an equivalent circuit model from 3-D PCBs or interconnects is complicated and requires prolonged hours. Hence, accurate preparation of the CAD data can expedite the modeling process so that it can be incorporated with the EMC analysis process. Therefore, commercial design tools are expected to acquire the following features:

- Import the CAD data with programmed installation of component models, terminals, nets and ports.
- Extraction of models containing substantial number of ports.
- Constructing a Simulation Program with Integrated Circuit Emphasis (SPICE)-adaptable. output model.
- Providing a schematic-based interface allowing transient and frequency domain analysis.

Currently, there exists various commercial tools, permitting a full data process chain from CAD import to the extraction of an equivalent circuit model. A prominent tool is Ansys Q3D Extractor [180] which implements the entire design chain and will further be thoroughly discussed in this thesis.

A.1.6 Power Semiconductor Models

Power semiconductors in power electronic systems, undergo consecutive switching transitions which are considered the main originators of EMC noise. The noise spectrum is defined by the switching frequency assigned by the controller unit and the type of the semiconductors (IGBT, MOSFET, WBG semiconductors). As discussed earlier in chapter I, the increasing switching speed and frequency when utilizing WBG semiconductors, equivalently influences the EMI noise. Thus, accurate, semiconductor models are required when conducting EMC analysis. Briefly, various models are readily available in SPICE simulation tools' libraries, such as LTSpice or accessible on web pages of most manufacturers. Hence, modeling of power modules such as power diodes [181] and MOSFETs [182], [183] are well established. IGBTs are more complex to model, however a detailed overview of modelling approaches can be obtained in [184].

As a result, alternative methods for EMC modelling were presented. Amongst these methods, the numerical modelling is well refined and extensively promoted. The beneficial outcome of this methodology is the ability to quantify the parasitic parameters of intricate structures and geometries. The PEEC method is generally used in literature to model PCB interconnections [141]. This method allows the extraction of parasitic parameters (resistance, self-inductance and mutual inductance) of a designed model [185]. The aforementioned methods were based on utilizing InCa3D software tool. However, the limitation of this tool is that it only models resistive and inductive aspects via the PEEC method. Accordingly, capacitive elements, which are the most critical parameters and CM current promoters, are computed using analytical expressions [186]. This provoked the necessity to examine a suitable software tool that will consider all parasitic parameters and essentially the parasitic capacitances between conductive routings. Hence, Ansys Q3D Extractor tool was nominated to resolve this issue and will be consequently further discussed.

A.2 Parasitic Analysis Fundamentals

A basic example to introduce the importance of parasitic analysis is that the simplest passive electrical components, such as resistors, inductors and capacitors, are not real. These components comprise parasitic parameters that shall be considered when employing these devices. For example, a twisted resistor has inductance and capacitance, a winding bears resistance and capacitance, a capacitor includes series and parallel resistance, inductance etc. These derivatives are usually constructed as lumped electrical models consisting of classic R, L, C components.

The propagation momentum of electrical signals is in the order of speed of light, which is $3 \cdot 10^8$ m/s in vacuum. Furthermore, in power electronics, the employed frequencies are usually in the order ranging from 10-100 kHz attaining 10-100 MHz. This implies that the minimum wavelength (λ) measured in the meters range, is usually greater by at least one order of magnitude than the peculiar

length (L) of electrical circuits, namely, the linear dimensions of components or conductive parts. This ensues rapid propagation in the latter and justifies the competency of representing components or electronic devices as equivalent lumped electrical models. This rule of thumb is represented in accordance to the following mathematical expression (1).

$$L \leq 0.1 \cdot \lambda \tag{1}$$

This signifies that every component of an electrical circuit model acquires parasitic parameters. The challenge arouses when finding possibilities to be able to adequately extract the parameters and construct an equivalent model.

A.3 Electromagnetic Formulation

Computational electromagnetic modelling, classified in figure II-1, is a beneficial tool to investigate electronic and electrical components. Actual electromagnetic occurrences can be classified according to a time varying computation, where alternative mathematical equations are necessitated in accordance to the equivalent time varying conditions. In this dissertation a quasi-static software tool, Ansys Q3D Extractor, was elected to perform the analytical approach of extracting the parasitic parameters of the designated pulse planar transformer. Quasi-static approximation anticipates that the size of the analyzed structure is small in comparison to the wavelength at the maximum frequency of interest. The wavelength is inversely proportional to the frequency. In most PCB and Integrated circuit (IC) packaging, it is generally 15 cm at 1 GHz and 1.5 cm at 10 GHz. This hypothesis allows Q3D Extractor to evaluate sophisticated structures in a competent and effective way [187].

Following a quasi-static approximation, the correlation between magnetic and electric fields according to Maxwell's equations presented in the differential frequency-domain (2), (3) can be neglected [188]. These relate the electric field $\vec{E}$ to the magnetic field $\vec{H}$ in the existence of materials defined by electric permittivity ε, conductivity σ, and magnetic permeability μ. Hence, displacement currents are anticipated to be negligible when calculating inductances and resistances. Similarly, the capacitive charge storage is neglected during inductance computation. Likewise, when calculating capacitance and conductance parameters, the inductive voltage drops produced by time-varying magnetic fields are ignored.

$$\nabla \times \vec{E} = -j\omega\mu\vec{H} \tag{2}$$

$$\nabla \times \vec{H} = (\sigma + j\omega\varepsilon)\vec{E} \tag{3}$$

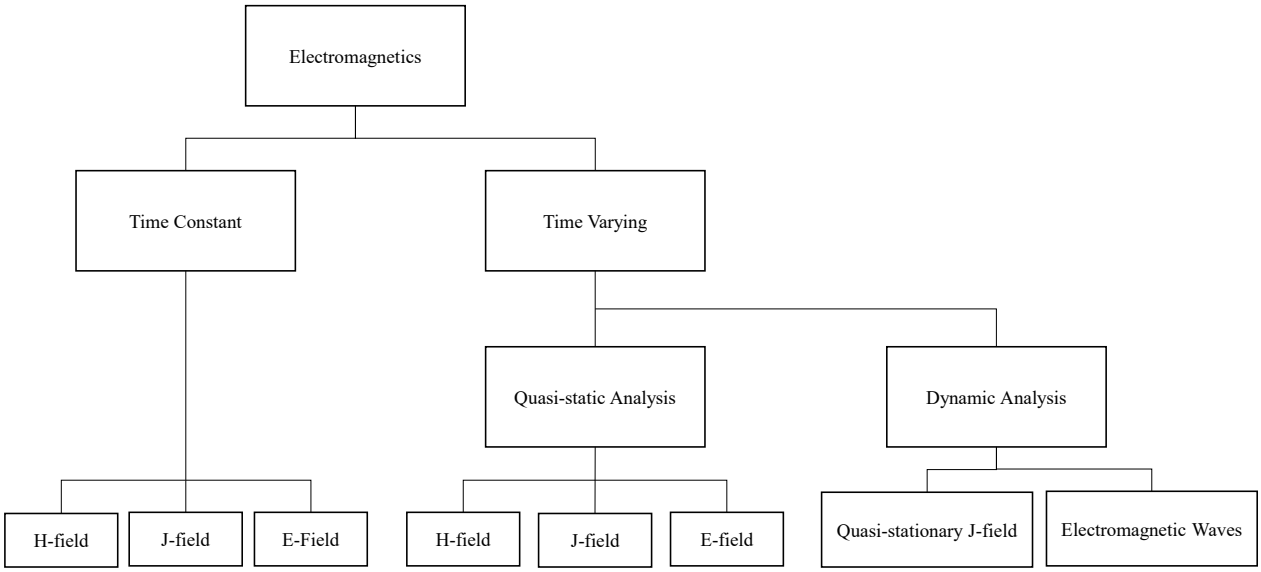


Figure II-1: Classification of electromagnetic formulation

B. PARASITIC EXTRACTION TOOL

B.1 Ansys Q3D Extractor

To reduce design and protype expenses, and govern electronic device behavior, Ansys Q3D Extractor, the leading parasitic extraction tool is commonly employed by power electronic engineers, both in academia and industry [189]–[191]. The competency of this tool when compared to other commercial 3D quasi-static EM solvers utilized for EM conformity analysis of power electronic systems, is its efficiency to extract resistance, conductance, partial inductance, and capacitance, known as RLGC parameters. Thus, it is the optimal tool for constructing models needed for power and signal integrity analysis. It allows better interpretation of high-speed electronic designs, principally multi-layered PCBs.

Furthermore, Ansys Q3D computes mutual inductive couplings between current paths, and capacitive couplings of conductive regions inside packages. Q3D Extractor relies on two numerical techniques: the FEM and the Method of Moments (MoM). This is achieved by either dividing the full problem space or surface of conductors into tetrahedral elements as illustrated in figure II-2 below, splitting the domain into smaller elementary sub-domains called finite elements. Furthermore, the modelling is positioned on dividing the solution into two parts. The low frequency (dc, $f < f_{dc}$) and high frequency (ac, $f > f_{ac}$). To attain the dc solution, current is uniformly distributed across the segments of conductors, which is anticipated and modelled using FEM, namely, skin depth is greater than the conductor thickness. Regarding the ac solution, it is presumed that the skin-effect is entirely developed, i.e., skin depth is approximately three times lower than the conductor thickness, and the currents are diffused only on the surface of conductors. The aforementioned solution is achieved using the MoM, which causes ac resistances to increase as $\sqrt{f}$. In the intermediate frequency range ($f_{dc} < f < f_{ac}$), the inductance and resistance interpretations are anticipated based on the dc and ac solutions [192]. It relies on the simplification of Maxwell's equations, termed quasistatic approximation by anticipating that the size of the analyzed design is diminutive compared to the

wavelength of maximum sought frequency where the coupling between magnetic and electric fields can be ignored [193]. Furthermore, it is essential to declare that Ansys Q3D Extractor can also be dynamically linked with other Ansys software tools to perform further analysis such as integrating the analyzed model in a customary electrical environment.

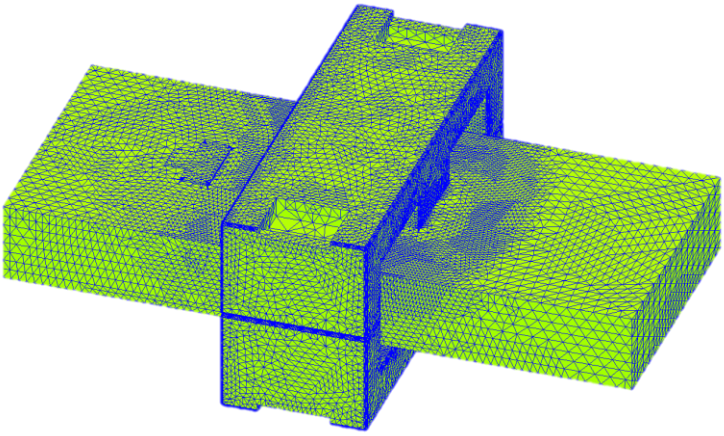


Figure II-2: Exemplary of a planar transformer simulated in Ansys Q3D Extractor

B.2 FEM Numerical Analysis

For high frequency (HF) magnetic analysis, for any random size electronic model, magnetic field and eddy current simulation techniques are necessitated. The solution of the simulation can be obtained in either frequency or time domain. 3D EM modelling methods can be utilized to find specific EM field information when analyzing a design. Thus, the EM field properties can be efficiently calculated spanning a wide frequency range (from kHz to MHz). Contrarily, conventional magnetic testing systems, only compute total power losses, insertion losses and leakage and magnetizing impedances. Currently, engineers can practically and accurately interpret EM field problems prematurely at the design and development stages.

Essentially, all of the electromagnetic phenomena are represented by Maxwell's equations, listed in a conventional form as revealed (4)-(7). Gauss's law (4) relates the propagation of electric flux density, $\boldsymbol{D}$, from the distribution of electric charge density, $\boldsymbol{\rho}$. It explains how electric field lines begin on positive electric charges and stop at negative charges. Gauss' law for magnetism (5), declares that the magnetic field, $\boldsymbol{B}$, does not start or end. Faraday's law of induction in (6), describes how a time varying magnetic field induces an electric field $\boldsymbol{E}$. Lastly, Ampere's law with Maxwell's addition (7) demonstrates that a magnetic flux density, $\boldsymbol{H}$, is originated in two ways, either by an electric current density, $\boldsymbol{J}$, or by the variation of electric flux density, $\boldsymbol{D}$.

$$\nabla \cdot D = \rho \tag{4}$$

$$\nabla \cdot B = 0 \tag{5}$$

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{6}$$

$$\nabla \times H = J + \frac{\partial D}{\partial t} \tag{7}$$

Regarding isotropic linear dielectrics and magnetic materials, the electric field $\boldsymbol{E}$ and magnetic field $\boldsymbol{H}$ are associated to the electric flux density $\boldsymbol{D}$ and magnetic flux density $\boldsymbol{B}$ as per (8) and (9).

$$D = \varepsilon E \tag{8}$$

$$B = \mu H \tag{9}$$

where ε, resembles the permittivity and μ the permeability. The hypothesis of isotropic materials is often used as it facilitates analytical derivations. This assumption is also employed in within each node/cell of the finite element approximation, however, material properties can be diversified throughout the domain [188].

B.3 Parasitic Capacitance Computation

When designing a planar transformer (PT), the stray capacitance cannot be neglected. The potential variation between turns, winding layers, and between windings and core generates these parasitic elements. The significance of this realization was previously highlighted, as stray capacitances considerably affect the magnetic device performance, where the current waveform on the excitation side becomes severely deformed reducing the overall efficiency of the converter. Moreover, under high voltage stresses, parasitic capacitances induce leakage currents and are the main originators of EMI disturbances [194].

Regarding the computation of parasitic capacitances with FEM, particularly when dealing with HF planar transformers, can be demonstrated by the theory of capacitances in a multi-conductor system [195], where the placement of the conductors is random and one of them might serve as the ground. Evidently, the presence of a charge on any of the conductors will affect the potential of all the rest. Therefore, based on the theory of conductors in a multiconductor system, the following set of N equations correlating the potentials of the N conductors to their designated charges is obtained (10).

$$\left\{\begin{array}{l} Q_1 = C_{11}V_1 + C_{12}V_2 + \cdots + C_{1N}V_N \\ Q_2 = C_{21}V_1 + C_{22}V_2 + \cdots + C_{2N}V_N \\ \quad\quad\quad\quad\quad\quad . \\ \quad\quad\quad\quad\quad\quad . \\ \quad\quad\quad\quad\quad\quad . \\ Q_N = C_{N1}V_1 + C_{N2}V_2 + \cdots + C_{NN}V_N \end{array}\right\} \tag{10}$$

The equation identifies the capacitance coefficients, denoted by C_{ii}, and the coefficients of induction, denoted by C_{ij} where ($i \neq j$). The condition of reciprocation ensures that $C_{ij} = C_{ji}$.

In accordance to Maxwell's theory, and in compliance with Poisson's equation, the alliance between potential and charge in a multiconductor system, can be defined by the electric scalar potential V (11).

$$-\nabla \cdot (\varepsilon \nabla V) = \rho \tag{11}$$

where ε, resembles the permittivity, and ρ is the space charge density.

The capacitance computation is resolved by utilizing FEM based numerical techniques. Galerkin's method is convenient to discretize the determined equation for two-dimensional problems. The representation of the capacitances in terms of static charge, representing the relationship between charges and voltages for the conductors is expressed as (12).

$$[S]\{V\} = \{Q\} \tag{12}$$

where [S] is the overall coefficient matrix and $\{Q\}$ is the charge matrix. By implementing the boundary condition defined placing a positive voltage on a conductor while leaving the other conductors grounded, induces positive charge to accumulate on the excited conductor, while a corresponding negative charge develops on the remaining conductors. This allows the computation of the capacitance Maxwell matrix. From the corresponding C_{ii} and C_{ij} coefficients, the capacitance from the *i'th* conductor to ground C_{i0} and the capacitance between the *i'th* and *j'th* conductor can be calculated [196].

A demonstrative example is illustrated in figure II-3 below between three conductors, where the net charge on each conductor is presented in (13).

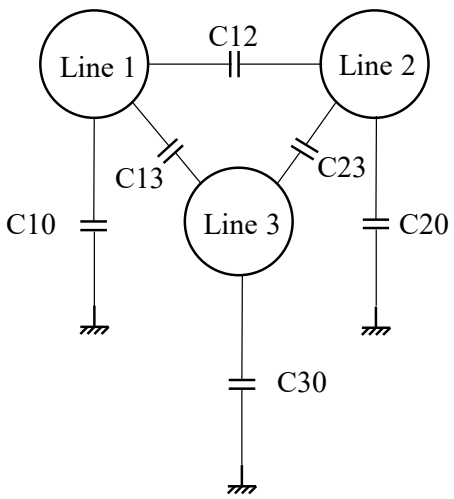


Figure II-3: Example of parasitic capacitance computation between three conductors

$$\begin{cases} Q_1 = C_{10}V_1 + C_{12}(V_1 - V_2) + C_{13}(V_1 - V_3) \\ Q_2 = C_{20}V_2 + C_{12}(V_2 - V_1) + C_{23}(V_2 - V_3) \\ Q_3 = C_{30}V_3 + C_{13}(V_3 - V_1) + C_{23}(V_3 - V_2) \end{cases} \tag{13}$$

In the case of a PT, two or more conductive sheets are sandwiched by a substrate or dielectric material with a specific dielectric permittivity. This represents a capacitance of a static plate capacitor that can easily be computed (14).

$$C = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{d} \tag{14}$$

Where ε_0 is the permittivity of free air space, ε_r represents the relative permittivity of the assigned dielectric material, A is the overlapping area of the conductive sheets and d is the distance between the conductive sheets as demonstrated in figure II-4.

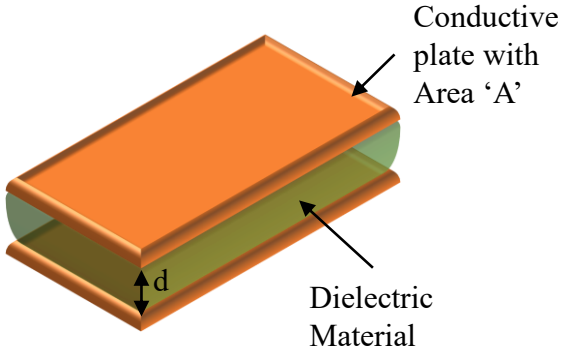


Figure II-4: Representation of a parallel plate capacitor

C. ARTIFICIAL ANALYSIS

C.1 Geometric Modelling

The initial step of analyzing a model in Ansys Q3D Extractor, is the actual implementation and definition of the geometrical design. FEM modelling can be achieved based on two different approaches: 2-D approach and 3-D approach. In the case of a transformer, 2-D simulations perform an analysis according to the transformer's symmetry axes. In this case, the simulation can be executed on the entire transformer cross section, or on only half of it, acknowledging its symmetry as illustrated in figure II-5. The benefit of this approach is that it requires limited computational time, however it can only partly consider the flux linkage in free air, as it cannot consider that the core geometry is limited.

3-D approach, which is the method conducted in this dissertation, is a FEM analysis that encompasses the entire transformer model. This analysis is remarkably accurate because it computes the transformer parameters taking into account all of the transformer composition, including those exposed to free air. Nevertheless, knowing that the entire geometry needs to be modelled with a fine mesh, this type of computation is prolonged. Furthermore, if a model comprises alternatively proportioned geometries, a mesh should be adequately identified to achieve a sufficient simulation [197].

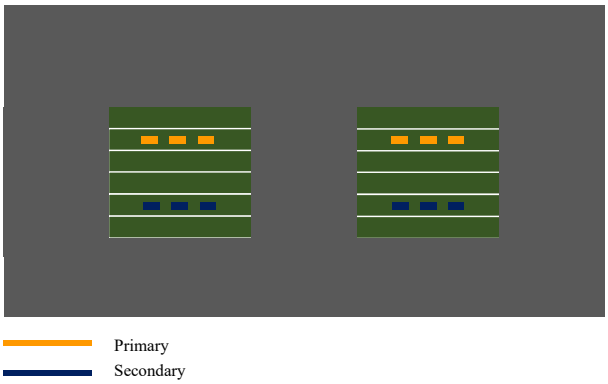


Figure II-5: Illustration of a 2-D planar transformer

C.1.1 Computer-Aided Design

There are several software tools that assist in the construction of a geometric model, namely Computer-Aided Design (CAD) software packages of different complexities can be utilized. The geometric models serve as both, the input data needed to perform the FEA simulations, and the foundation for physical fabrication of the component. For example, Ansys comprises a 3D CAD modelling software known as Ansys SpaceClaim. One can create 2-D or 3-D geometric models, or modify already existent models that are created by a distinctive CAD software tool. However, when a model is imported from an external software, sometimes the files are not translated properly by Ansys and hence the design requires modification to achieve successful analysis. This issue was challenging when conducting the analysis of the pulse planar transformers designed for gate-drivers developed at IETR laboratory as they were designed by an alternative software tool.

In gate drivers developed at IETR, planar transformers are modelled and designed using a notable complete CAD software system, known as Altium Designer. This is a distinct PCB design software allowing easier, faster, economical and efficient design processing. In addition, it serves as the groundwork for manufacturers to conveniently fabricate the modeled design. Figure II-6 below represents an example of a modelled power planar transformer using Altium Designer.

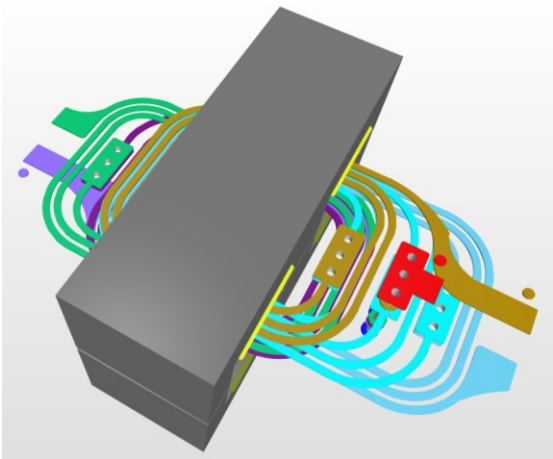


Figure II-6: Planar transformer design using Altium Designer

Therefore, the first stage of the process of analyzing the already realized pulse planar transformers, is to investigate the proper data exchange files that need to be exported from Altium Designer and authorized by Ansys Q3D Extractor tool, without modifying nor distorting the modelled design. The process will be generically demonstrated in section C.2 below.

C.2 Automated Design Scheme

The main objective of digital design is to reduce development time by restricting the number of fabricated physical prototypes. Concerning electronics, there is typically a relatively insufficient lead time of components and PCBs. This intrigues researchers and engineers to rapidly move to the experimental phase to examine a design. This is termed as a trial-and-error approach which was conducted at IETR lab when designing the pulse planar transformers. Nevertheless, if designs are constantly reviewed, lead times will accumulate. Furthermore, if a perplexing complication is encountered, it might be difficult to diagnose, measure and legitimize a solution.

A reliable and efficient automated design scheme is essential to be constructed before the actual fabrication of components. This will allow examiners to digitally review several designs and test different aspects. This will increase the researcher's observation on the overall electronic system and aid in identifying, resolving and anticipating challenges that might arouse in the design. Thence, if exploited properly, it permits the fabrication of a single physical prototype that conforms to the design specifications [188]. This section will identify a general simulation methodology process that was adopted to analyze the already realized and implemented pulse planar transformers.

C.2.1 Data Exchange Files

The physical planar transformers at IETR laboratory were designed using Altium Designer and fabricated based on this composition. To adopt this design structure, it was imperative to identify the specific data exchange files that need to be exported from Altium Designer and imported into Ansys Q3D Extractor. This initial step is vital to ensure that the imported model is compatible with the one implemented in Altium and was actually fabricated.

Gerber files and ODB++ files are one of the prominent formatted files that regard PCB designs' information such as circuit board objects, copper traces, vias, pads and solder masks. However, what makes ODB++ files superior to gerber files, is that the latter cannot define the layer stack-up of the PCB and the drill files cannot be included. On the other hand, ODB++, known as the more intelligent file can include a huge amount of data.

In Altium Designer, ODB++ files, which have become the dominant industry guidelines for configuring and transmitting PCB board data, are exploited to attain the initial step in the analysis process. ODB++ is a CAD-CAM data exchange format utilized in the design and fabrication of PCBs. They gained superior efficiency to Gerber format data exchange files. The format was initially developed by Valor Computerized Systems, LTd., as an open database that could provide further informative data exchange between PCB design software and Valor CAD-CAM software employed by PCB fabricators. Therefore, the proper transfer of the aforementioned files into Ansys software tool shall be sufficiently examined and tested before proceeding to simulation analysis.

C.2.2 AnsTranslator

ODB++ is an ASCII open-format produced by Mentor Graphics to seize CAD/EDA, assembly, and PCB manufacture information. It has become the industry possessor format for formatting and transferring PCB board data.

In Ansys software tool, Ansys ODB++ translator, named as AnsTranslator, allows the utilization of ODB++ and ANF file formats to perform analysis of PCBs. However, this is implemented in support of Ansys SIWAVE and Planar EM. Therefore, the direct import of the files into Ansys Q3D Extractor for example, might trigger some ODB++ issues, where the ODB++ file does not completely conform to the Valor ODB++ specifications as depicted in figure II-7 below. Thus, complications such as misalignment of geometries, overlapping of geometries and showing extra auxiliary geometries might occur. Hence, model corruption might take place due to certain file losses when performing the import. Moreover, this will cause the Mesh not to be properly defined and leads to a prolonged simulation that will terminate with failure messages. AnsTranslator takes the ODB++ input, and produces as output an Ansoft (ANF) file and an SIWAVE component file. Accordingly, the ODB++ data exchange files of the modelled design, should be exported from Altium Designer and primarily imported into Ansys SIWAVE that will accurately transform the model with all the related assignments and layer stack-up. However, attention shall be taken to always ascertain the layer stack up in Ansys SIWAVE. This will be further discussed in the upcoming sections. In Ansys SIWAVE, the model can be exported directly from an embedded link into Q3D Extractor where one can proceed with the desired analysis process, which will be generally identified in the upcoming section.

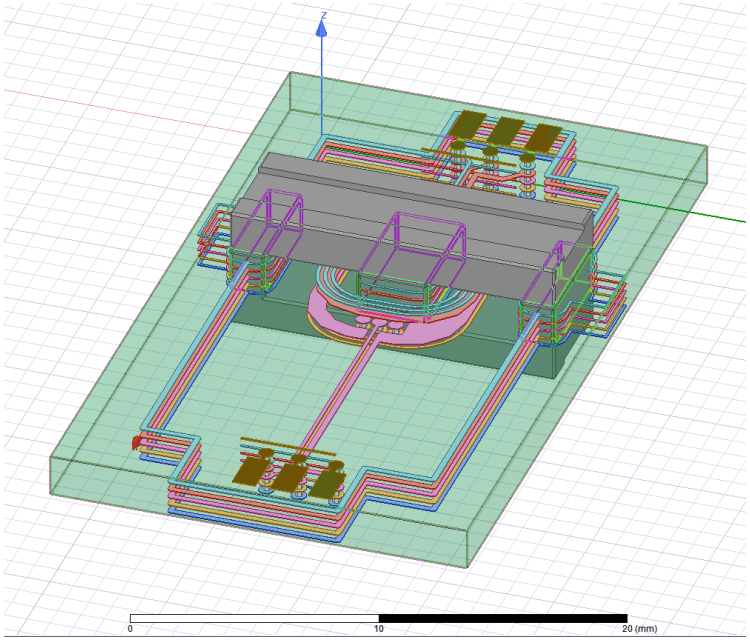


Figure II-7: Planar transformer ODB++ file imported directly into Q3D

C.2.3 Generic Design Blueprint

The definition of a digital design framework is economical and essential. Particularly, when the simulation process combines an assortment of associated tools that are needed to attain the intended end-result required by the user, or to test a specific critical occurrence, hence, preserving physical prototypes from any probable damage. In this case, it is to be able to implement a CM and DM model of the pulse planar transformer. This is advantageous since the simulation analysis is shared by collaborative tools, therefore, reducing computational time and complications. In addition, it is imperative to ensure that the exchange files or the import/export of the design is compatible amongst the alternative exploited software tools. A synopsis of the course of action taken and followed to attain sufficient simulation results is revealed in figure II-8.

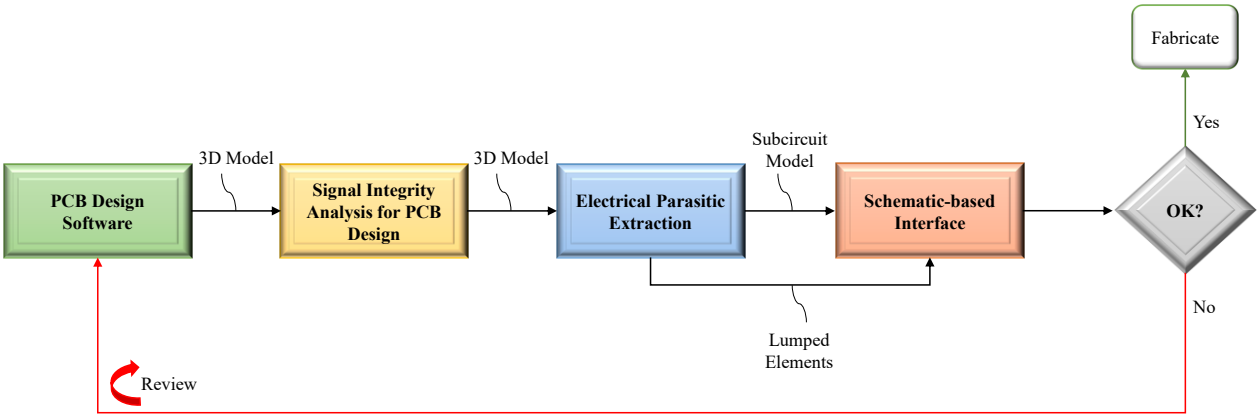


Figure II-8: Mechanism followed to simulate pulse transformer model

The previously displayed scheme is further expanded by revealing the designated assortment of software tools used, in addition to the input and output of each stage as depicted in figure II-9. The pulse planar transformer is modelled and designed in Altium Designer. Afterwards, the designated ODB++ data exchange files of the 3D model are exported and imported into Ansys SIWAVE. Ansys SIWAVE, which supports the imported files, is a specialized design platform for power integrity, signal integrity and EMI analysis of electronic packages and PCB. In this software tool, the layer-stack up of the imported model should be verified along with the materials appointed for every layer in the PCB model. After fulfilling this step, the 3D modelled transformer is selected and exported from within SIWAVE into Ansys Q3D Extractor using the embedded link in the software. The Q3D Ansys Electronic Desktop page will be invoked directly if the option was selected by the user or saved in the appointed designated folder. Henceforth, the precise model is now available in Q3D Extractor, for further simulation. In this software the model is analyzed after assigning the necessitated excitations for the conductors and defining an analysis setup, in addition to a frequency sweep. The step succeeding Q3D analysis, and after the extraction of the parasitic parameters, is the utilization of the extracted lumped elements or the equivalent subcircuit in a schematic-based interface. Q3D Extractor can be dynamically linked with Ansys Circuit Design which allows the simulation of a subcircuit with the project's original simulator to be aligned with the circuit simulator [198]. In addition, the availability of a schematic editor tool allows the creation of schematic circuit designs by adding and wiring electrical components. Furthermore, this software permits the execution of a transient and a frequency domain analysis that assists in deriving the intended results.

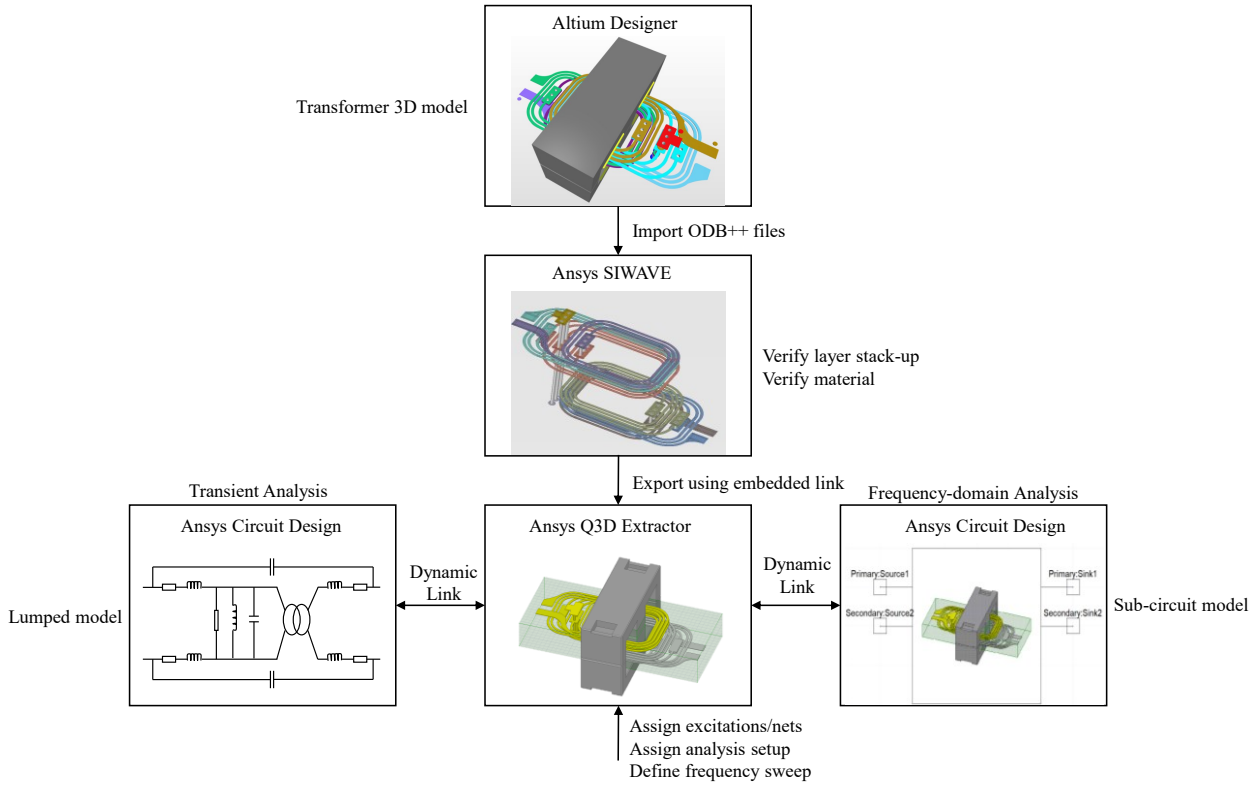


Figure II-9: Generic software scheme used to simulate planar transformers

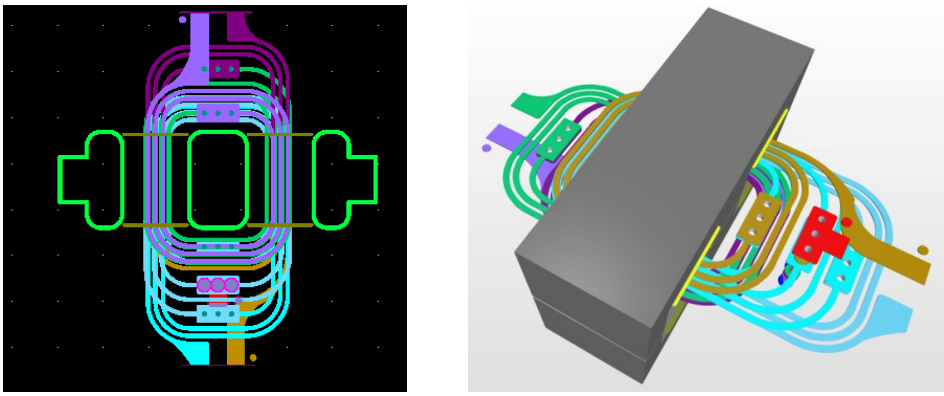
As illustrated in figure II-9 above the diverse software tools were utilized to perform the simulation analysis. This process is not well-defined in literature and was structured referring to Ansys software tool design manuals, extensive research and considerable design analysis evaluations. Therefore, the upcoming section will reveal in detail the exact steps performed in each of these software tools in order to reach the result.

D. Case Study: Power Transformer Analysis

A case study of a simulation analysis of a power planar transformer implemented in gate driver developed by Julien Weckbrodt [78] will be demonstrated in this section in order to explicitly present, and expand the capabilities of every software tool utilized. The objective of this section is to highlight the simulation process and develop the software sequential diagram highlighting fundamental steps that need to be implemented in every stage, commencing with Altium Designer and concluding with Ansys Circuit Design.

D.1 Altium Designer

A planar power transformer was designed and modelled in Altium designer. Once the design is finalized and a 3D model is created as revealed in figure II-10, the design can be exported from Altium Designer by exporting the appropriate ODB++ data exchange files. To access the files' location, the user should go to the fabrication outputs, and not the export button option as demonstrated in figure II-11 below.



(a) (b)

Figure II-10: Altium Designer power transformer model (a) 2-D representation; (b) 3-D representation

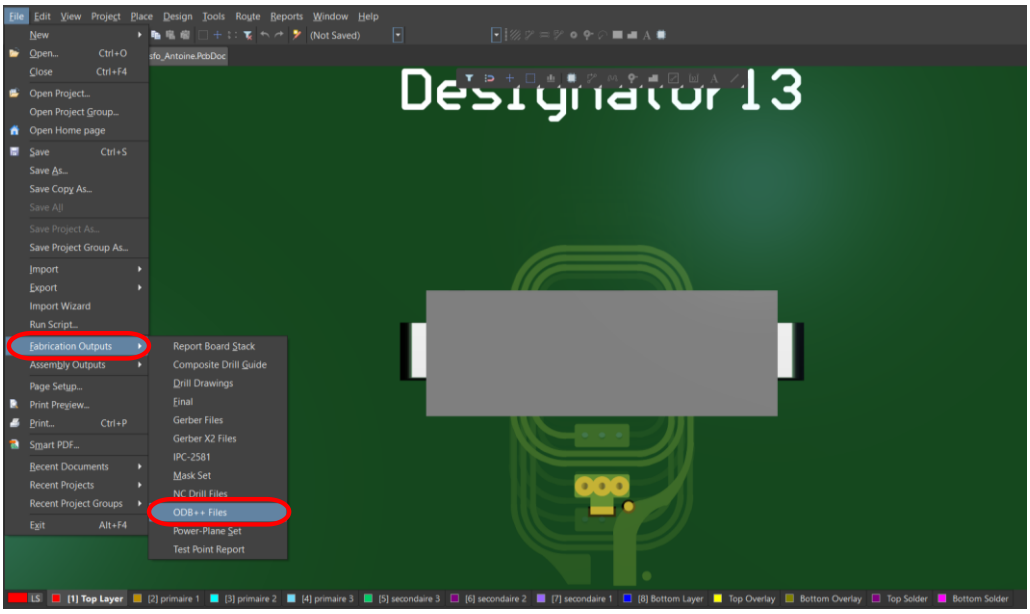


Figure II-11: Export ODB++ files from Altium Designer

The odb file will then be automatically updated in its designated folder and is now ready to be utilized in Ansys software tool.

D.2 Ansys SIWAVE

Ansys SIWAVE supports the exploitation of ODB++ files to perform studies on PCB board circuits. Thus, when this software tool is opened a welcoming pop-up box appears with an option to select to import ODB++ files as shown in figure II-12. Hence, the related ODB++ files of the power planar transformer were selected. The main objective of this tool is to verify the stack-up layer of the transformer by assuring the distance between the conductive layers to be compatible with the ones assigned in Altium Designer, as they may alter upon import. In addition, the user should ascertain the material selected for the conductors as well as the dielectric material. The verification of the layer stack-up is a process that automatically appears in SIWAVE, and is depicted in figure II-13. Therefore, the layers will automatically appear, the user should verify the thickness, where the unit

can be altered from this tab at the bottom. Moreover, the user can specify or modify the layer type and the dielectric material of each layer.

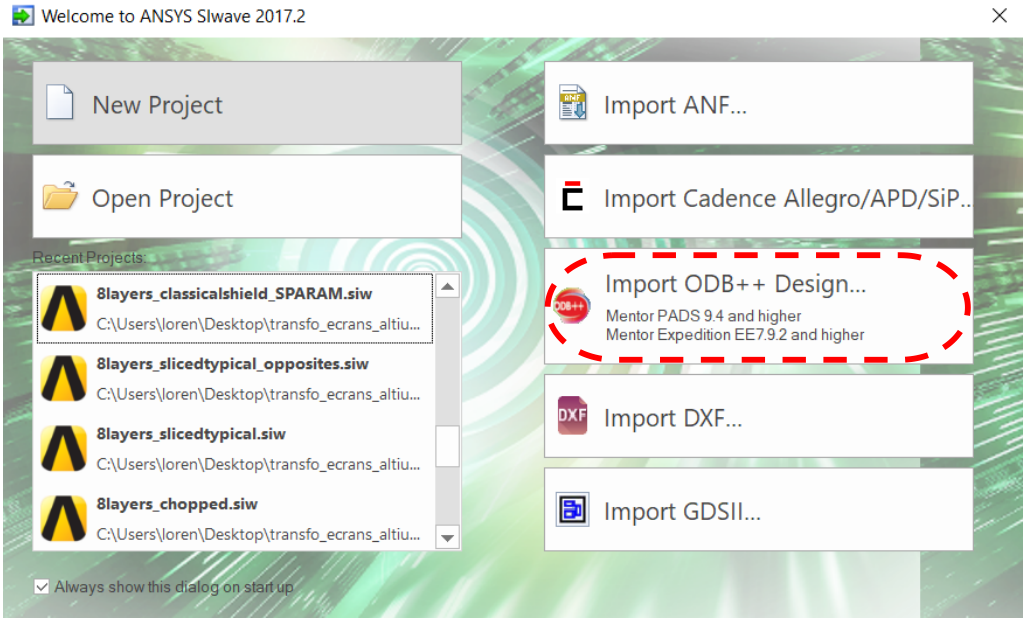
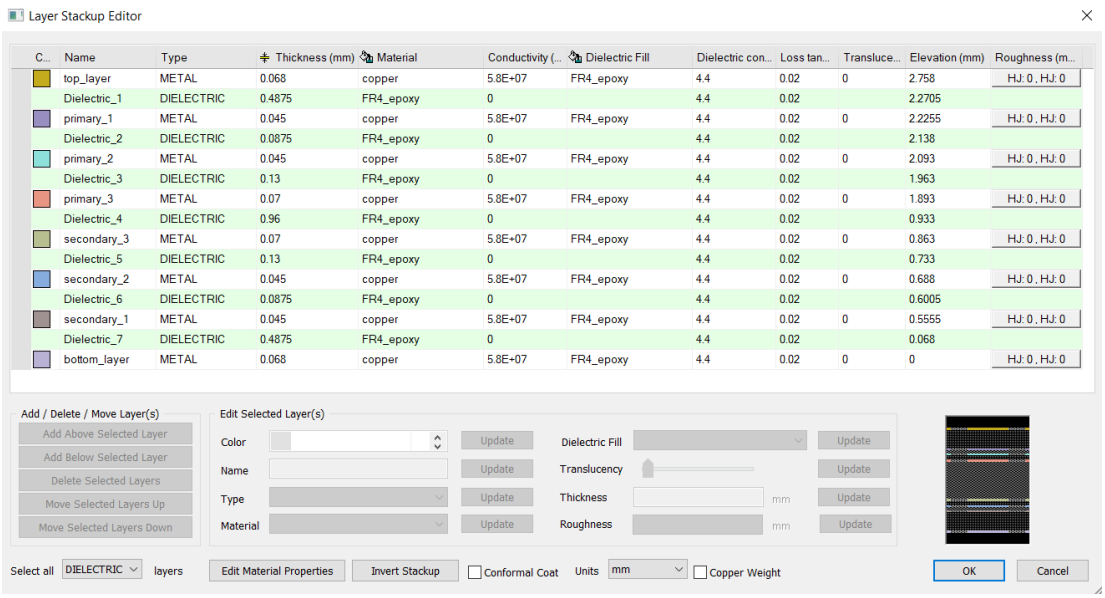


Figure II-12: Importing ODB++ files into Ansys SIWAVE



C...	Name	Type	Thickness (mm)	Material	Conductivity (...	Dielectric Fill	Dielectric con...	Loss tan...	Transluce...	Elevation (mm)	Roughness (m...
	top_layer	METAL	0.068	copper	5.8E+07	FR4_epoxy	4.4	0.02	0	2.758	HJ: 0 , HJ: 0
	Dielectric_1	DIELECTRIC	0.4875	FR4_epoxy	0		4.4	0.02		2.2705	
	primary_1	METAL	0.045	copper	5.8E+07	FR4_epoxy	4.4	0.02	0	2.2255	HJ: 0 , HJ: 0
	Dielectric_2	DIELECTRIC	0.0875	FR4_epoxy	0		4.4	0.02		2.138	
	primary_2	METAL	0.045	copper	5.8E+07	FR4_epoxy	4.4	0.02	0	2.093	HJ: 0 , HJ: 0
	Dielectric_3	DIELECTRIC	0.13	FR4_epoxy	0		4.4	0.02		1.963	
	primary_3	METAL	0.07	copper	5.8E+07	FR4_epoxy	4.4	0.02	0	1.893	HJ: 0 , HJ: 0
	Dielectric_4	DIELECTRIC	0.96	FR4_epoxy	0		4.4	0.02		0.933	
	secondary_3	METAL	0.07	copper	5.8E+07	FR4_epoxy	4.4	0.02	0	0.863	HJ: 0 , HJ: 0
	Dielectric_5	DIELECTRIC	0.13	FR4_epoxy	0		4.4	0.02		0.733	
	secondary_2	METAL	0.045	copper	5.8E+07	FR4_epoxy	4.4	0.02	0	0.688	HJ: 0 , HJ: 0
	Dielectric_6	DIELECTRIC	0.0875	FR4_epoxy	0		4.4	0.02		0.6005	
	secondary_1	METAL	0.045	copper	5.8E+07	FR4_epoxy	4.4	0.02	0	0.5555	HJ: 0 , HJ: 0
	Dielectric_7	DIELECTRIC	0.4875	FR4_epoxy	0		4.4	0.02		0.068	
	bottom_layer	METAL	0.068	copper	5.8E+07	FR4_epoxy	4.4	0.02	0	0	HJ: 0 , HJ: 0

Figure II-13: Transformer layer stack-up editor in Ansys SIWAVE

Once the layer stack up is defined, the design can be directly exported into Ansys Q3D Extractor from within SIWAVE tool export tab option as illustrated in figure II-14. The user is able to identify some Q3D export options if needed before attempting to perform this step, such as generating full nets or separating dielectrics. If selected by the user, this selection will automatically invoke an Ansys Q3D Extractor project to open comprising the planar transformer with the identified copper nets and dielectric material layer.

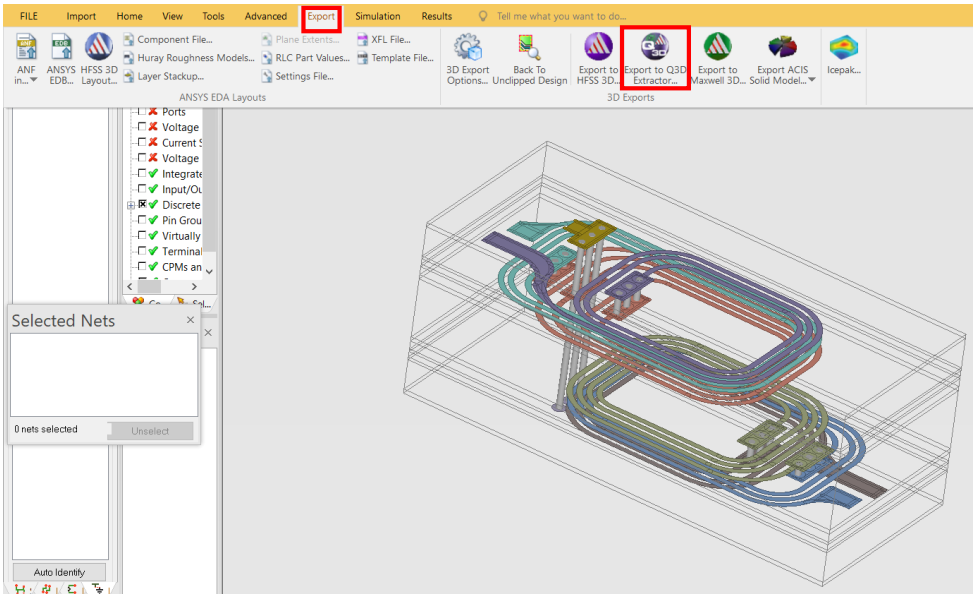


Figure II-14: Export to Q3D Extractor from Ansys SIWAVE

D.3 Ansys Q3D Extractor

The invoked Q3D project will present the properly identified planar transformer in its workspace where the component can be further analyzed. Firstly, the user needs to determine the model's unit of measurement by verifying the unit settings in Q3D under the modeler tab, which in this case is mm. On the left side of the workspace, the project manager tab allows the regulation of the modelled design by allowing the user to assign excitations, nets, mesh operations and an analysis setup. In addition, the material assignment of every component can be reviewed and edited under the model tab as revealed in figure II-15. It is imperative to declare that the material assignment and net identifications automatically appear in Q3D once the project is invoked from Ansys SIWAVE. The nets, which comprise all conductive parts of the project are only renamed by the user under the project manager tab for ease of identification in the matrices that will be later generated once an analysis setup is processed.

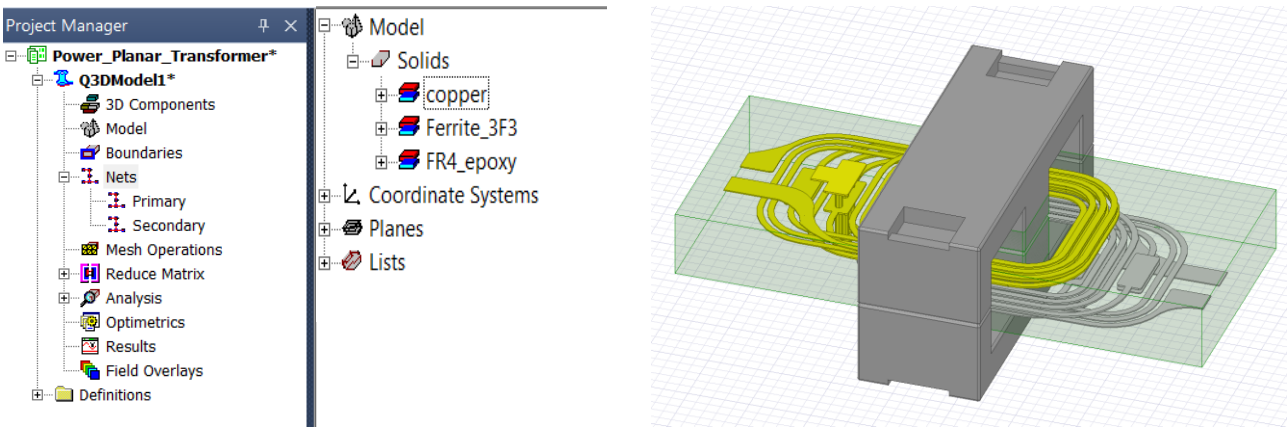


Figure II-15: Power planar transformer invoked in Ansys Q3D Extractor

D.3.1 Identifying Nets

It is essential to identify the nets of the model, as this allows the computation of the capacitance/conductance (CG) solution matrix. As previously declared, nets are usually auto-identified and are assigned only to conductive material. The nets will appear under their designated section in the project manager window. In this example the primary and secondary windings are the assigned nets as revealed in figure II-16.

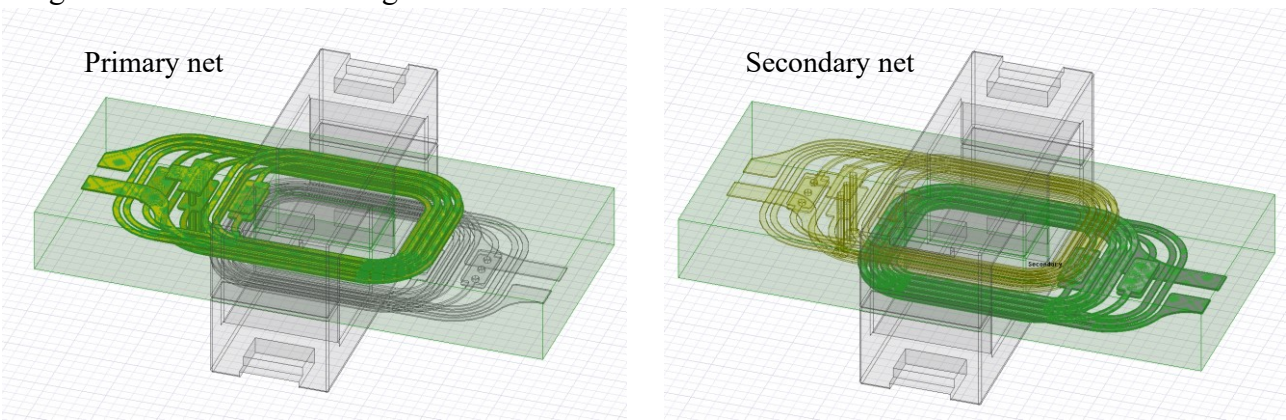


Figure II-16: Assigning the transformer nets in Ansys Q3D

D.3.2 Assign Excitations

In order to compute a resistive/inductive solution matrix, namely AC/DC RL solution in Q3D, assigning excitations to the nets is necessary. Any net should be identified with a single sink and at least one source. A source determines where the current enters a net and a sink identifies the exit path of the current. This can be achieved by right clicking on a face on the geometry section which is needed to be identified as a source or a sink and select assign excitation to the latter as depicted in figure II-17.

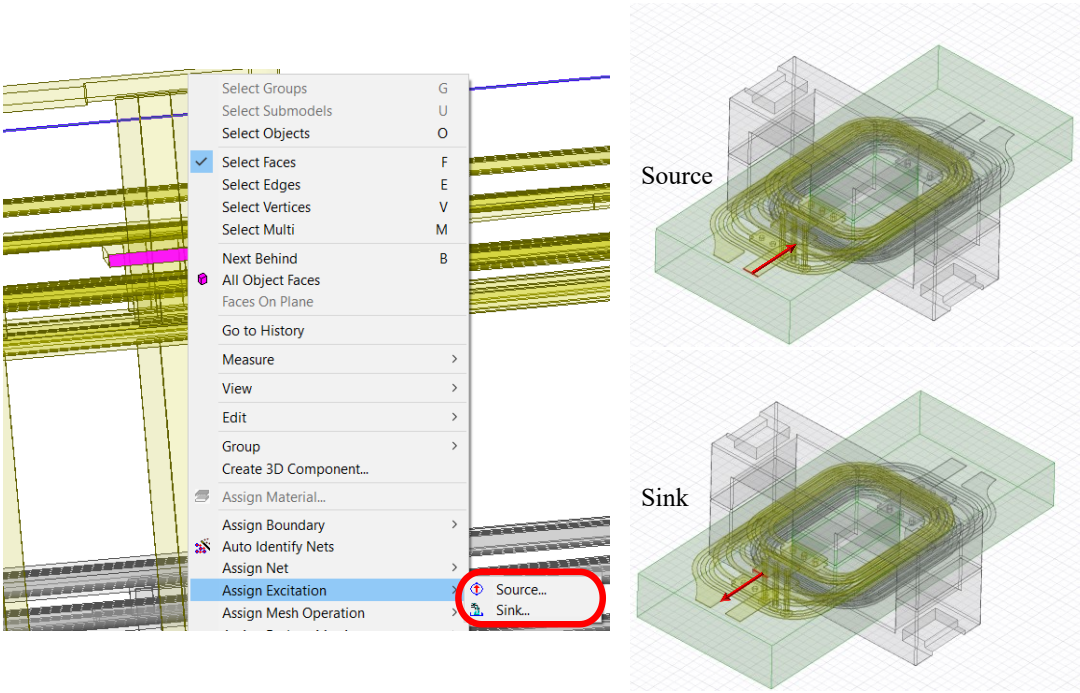


Figure II-17: Assigning excitations on planar transformer nets

D.3.3 Defining Mesh Operations

After identifying nets and excitations, the mesh operation is checked and defined. Under Mesh operations, the user shall select the initial mesh settings, where the mesh is auto-identified. The general tab will reveal selections for three mesh methods:

- Auto (default): the solver automatically selects the appropriate Mesher based on geometry. In most cases this will be a TAU mesh.
- TAU Mesh: Mainly used for complex geometries where a tolerant Mesher can create a mesh.
- Classic Mesh: Based on Ansoft 11 Mesher, might not be suitable for curved surfaces.

Under Curved Surface Meshing, the Use Slider or Manual Settings are available. The slider includes a visual representation of the resolution, one can choose an option ranging from coarse resolution with a small mesh size through a nine-position scale to a fine resolution with a large mesh size as illustrated in figure II-18, revealing the elected mesh for the power planar transformer analysis.

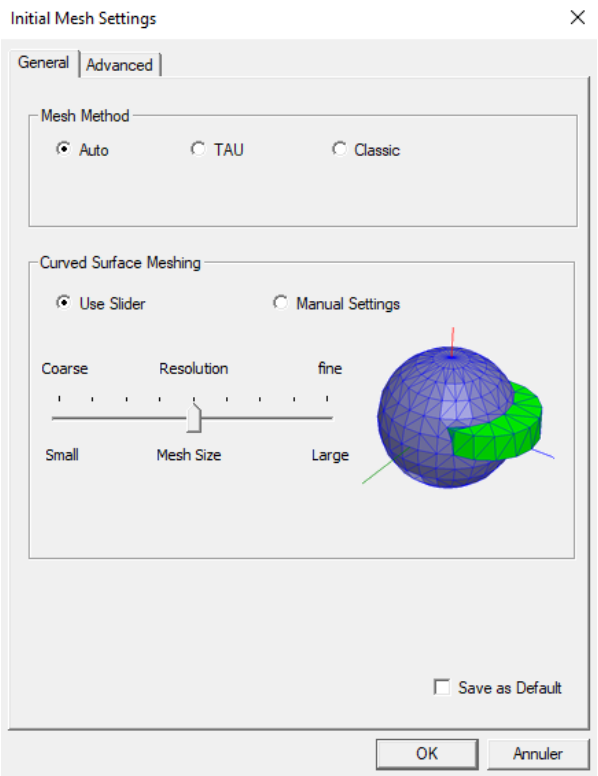


Figure II-18: Mesh operations defined for analyzing power transformer

D.3.4 Specify a Solution Setup

The specification of an analysis setup in Ansys Q3D Extractor is vital to compute CG and AC/DC RL parameters. This is performed by adding a solution setup as seen in figure II-19, where the user selects a specific analyzing frequency along with the designated solution selections. The save fields option is checked to enable field solutions post processing. Moreover, the user identifies a definitive adaptive solution criterion for each of the parameters where the default adaptive solution can be kept. The automatically increase solution order check box allows the solver to decide and increase the solution order. The solution order can be assigned as normal, high, higher, or highest. In the adaptive solution section, the maximum number of passes, minimum number of passes, minimum converged passes and percent error mark the stopping criteria. Q3D Extractor exits the adaptive loop as soon as one of these criteria is met. Regarding the percent refinement per pass, it designates what percentage of high-error triangle should be refined during each iteration.

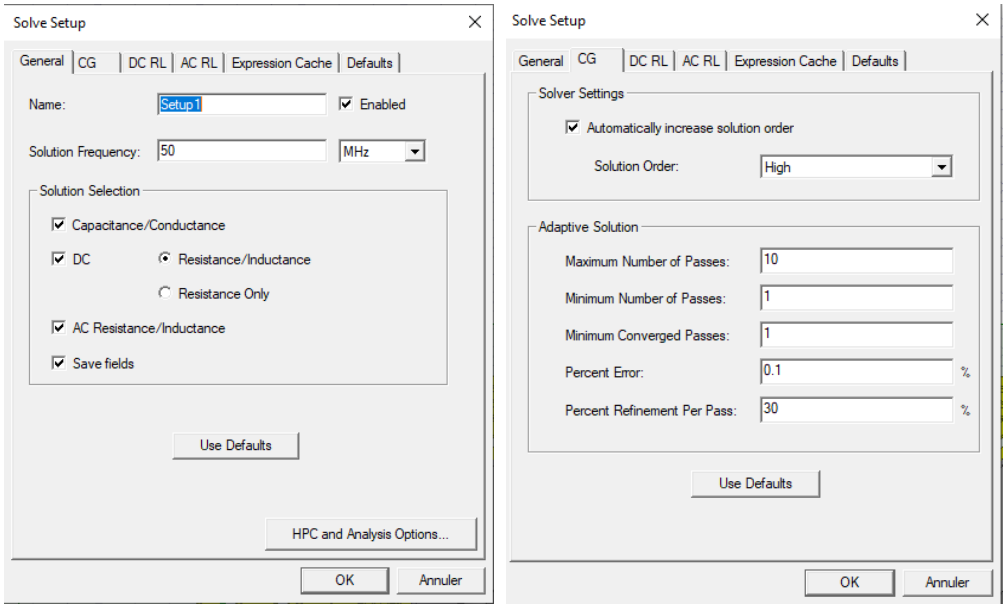


Figure II-19: Analysis setup identification

D.3.4.1 Frequency Sweep

A frequency sweep can be added to an existent analysis setup, which allows the generation of a solution across a range of frequencies after the adaptive solution is realized. This can be achieved by adding a frequency sweep to the analysis setup as shown in figure II-20. The sweep type can be either discrete or interpolating. A discrete sweep generates field solutions at specific frequency points in a frequency range, advantageous when only a few frequency points are necessary to accurately represent the results in a frequency range. Whereas, interpolating, estimates a solution for an entire frequency range, mainly when the range is wide and the frequency response is smooth. This feature is essential when it is intended to examine the component in Ansys Circuit Design in a frequency or transient domain analysis.

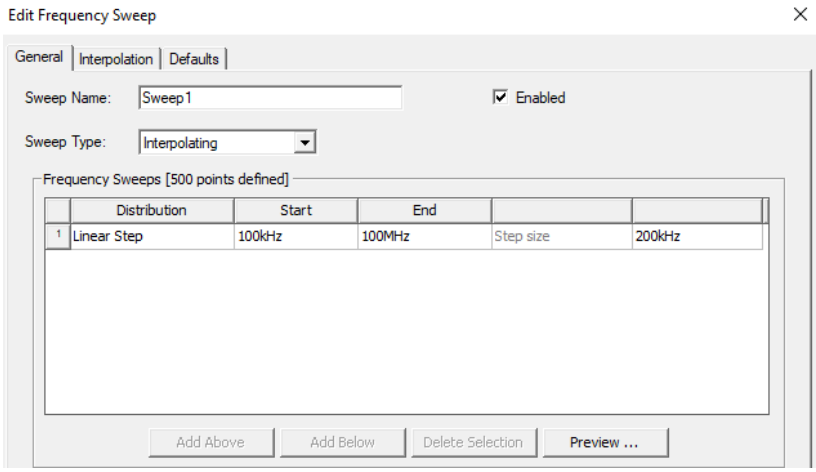


Figure II-20: Adding a frequency sweep to the analysis setup

D.3.5 Q3D Validation and Analysis

The final step to be implemented before analyzing the design, is performing a validation check. This will certify that the modelled design is ready for analysis as revealed in figure II-21. Accordingly, the user can analyze the design and monitor its progress.

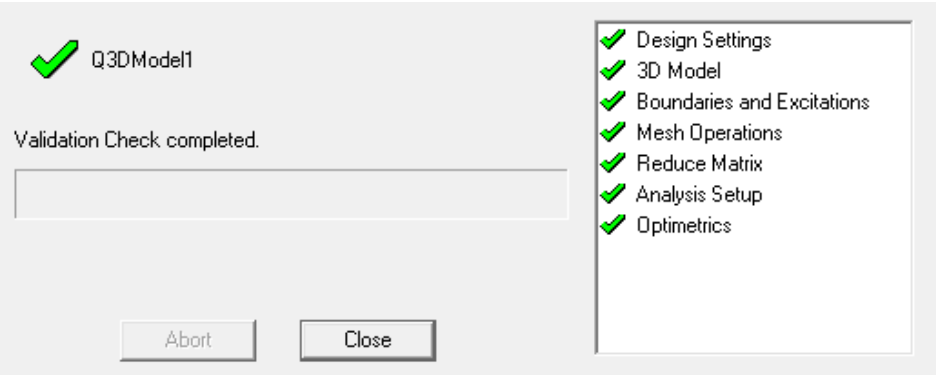
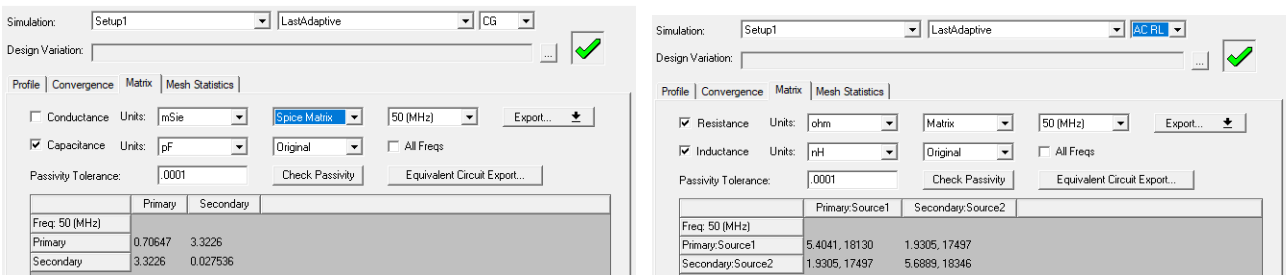


Figure II-21: Q3D validation check

D.3.6 Post Processing and Generating Reports

After the solution is complete, one can display and analyze results such as viewing solution data, creating 2D or 3D reports, plotting the finite element mesh or the field overlays of the objects. The solution data encompasses the RLGC solution matrices that can be accessible either during or post simulation analysis. The Matrix solution data displays the results of CG and AC/DC RL analysis at the designated frequencies as depicted in figure II-22. As illustrated, the capacitance matrix reveals the assigned nets, whereas the AC RL matrix displays the parameters in accordance to identified sources which is similar to the DC RL matrix. For the capacitance matrix, the diagonal matrix elements are called self-capacitances and the off-diagonal matrix elements are called mutual capacitances. This is similar for the inductance matrix, representing self-inductance of each signal line and mutual inductances between the lines.



(a) (b)

Figure II-22: Matrix solution data (a) capacitance matrix ; (b) AC RL matrix

When a spice sub-circuit is extracted from Ansys Q3D, an equivalent circuit is constructed using the parameters requested by the user. If the conductors have only one source terminal and one sink terminal, which is the case with the analyzed transformer, the system creates a balanced circuit model. This means that the circuit's impedance is the same regardless of the current flow. A basic example is demonstrated in figure II-23 below, of two conductors each comprising a single source and sink

terminal and its associated balanced circuit. Hence, the topology used for RLGC circuit models is based on quasi-static field solvers, an electrostatic solver is applied for capacitance (C), and a magneto-quasi-static solver for inductance (L) and resistance (R). The RLGC matrices are then unified into a circuit model to symbolize the overall behavior of the structure. Generally, the quasi-static model is a convenient approximation of the structure's full-wave response up to a frequency corresponding to ¼ wavelength.

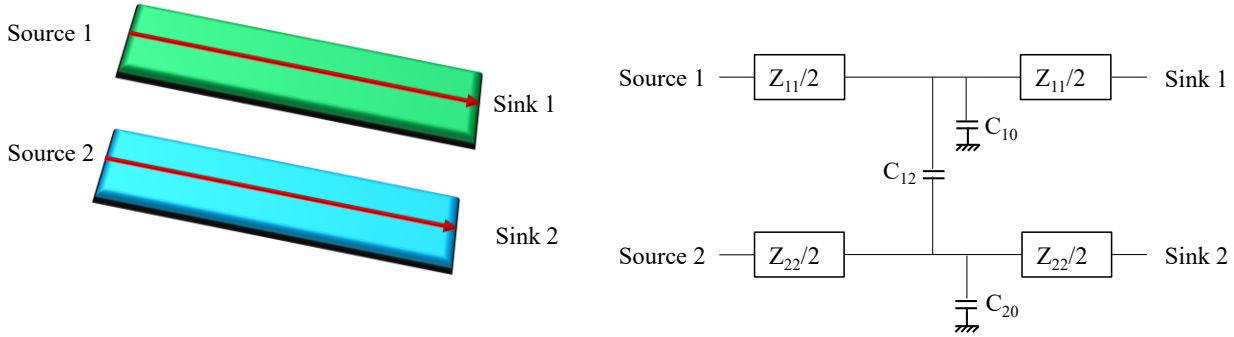


Figure II-23: Two excited conductors and their associated equivalent balanced circuit

D.3.7 Reducing Matrices

The reduce matrices option in Q3D allows to modify the existent original matrix by assigning selected conductors to appear in the solution which allows one to easily optimize ground assignments and generate a SPICE equivalent circuit. This feature is utilized to be able to extract RLGC parameters and construct the equivalent circuit model in Ansys Circuit Design. This beneficial option grants the user to do the following:

1. Simulate series and parallel connections between nets or terminals (sources/sinks).
2. Model floating nets and floating terminals in a model.
3. Investigate the effects of grounding different nets in a design.
4. For capacitance matrices, configure the case where the charge at infinity is zero (infinity is not maintained at zero potential).
5. For AC problems, compute the resistance at diverse frequencies.
6. For inductance and resistance matrices:
    a. Alter the location of current sink points inside conductors.
    b. Add current sink terminals to multi-terminal conductors.
    c. Designate a current return path through a conductor in the model.

Hence, reducing a model 's capacitance, inductance, and resistance matrices enables the examiner to rapidly and easily alter the excitations and connections of the conductors in the model without having to modify the conductor and source assignments and generate a new solution. Moreover, it allows modeling designs that cannot otherwise be simulated in Q3D Extractor, such as conductors connected in parallel or series. The available reduction methods include, move sink, add sink, join in series, join in parallel, join selected terminals, change frequency and other significant methods which will be summarized thereafter due to their relevance in constructing the equivalent circuit model by allowing the user to simulate an open circuit or a closed loop for example.

D.3.7.1 Float Net

This type of reduction allows the existence of floating conductors in a design. In inductance and resistance matrices, the total charge in a floating net is forced to zero amps. This simulates an open circuit occurrence. In a capacitance matrix, a floating net implies a total charge of zero. The net is considered as a perfect conductor as it is equipotential. The potential of the floating net relies between the potential of the adjacent sources and ground, depending on the excitations and the model's geometry.

D.3.7.2 Ground Net

This form of reduction grounds the specified nets in one's model. In capacitance matrices, grounded conductors endure a potential of zero volts. The ground reference at infinity is also considered to acquire zero potential. Grounded conductors in capacitance computations can be modeled in three means which are, utilizing matrix reduction, setting a conductor's voltage to zero, or by appointing a conductive material to an object and not proclaiming it as a conductor. For inductance and resistance matrices, when a conductor is grounded, its source terminals are linked to its sink terminal. Current can outflow in the newly created circuit due to fields induced by the surrounding conductors. The fields produced by this connection influence voltage drops observed in surrounding conductors. Thus, this will impact the inductance matrix of the remaining conductors.

D.3.7.3 Float Terminal

This application allows the shut off of the current in a particular source terminal. The effect on the inductance and resistance matrices is to exclude the row and column associated with the appointed source terminal. The other entries of the matrix are unaltered.

D.3.7.4 Float at Infinity

This function enables to model the case where the charge at infinity is zero, causing the potential at infinity to float, allowing the user to use a local ground as a reference. When computing capacitance, the Q3D Extractor employs the voltage at infinity as a reference, and presumes that this voltage is equal to zero. This signifies that the charge inside the problem region is balanced by the charge at infinity, i.e., a charge is generated at infinity. However, occasionally, if the ground net is intended to be the reference in the model, Q3D Extractor alters the capacitance values to demonstrate a local reference. The potential at infinity is not restricted to zero, and relies on the voltages inside the model.

D.3.7.5 Return Path

This reduction application permits to select a net to serve as a return path for current, allowing the approximation of the loop inductance of a closed conduction path. If a net is identified as a current

return path, the entire current exiting from the sink terminals on the remaining conductors returns inside the appointed conductor. The absolute current is compelled into the sink terminal of the return path conductor and arouses from the source terminal. This creates a closed current loop, resembling that the return conductor is connected via an ideal wire to the source conductor. Current flow in the particular return path conductor is automatically reversed. It is noted that this matrix reduction operation is adopted to model the inductance and resistance of a closed loop in Q3D Extractor (i.e., loop L, R). The software directly computes partial inductance and resistance matrices, which only comprise the effects of currents in the portion of the loop that is being modeled.

D.4 Ansys Circuit Design

Dynamically linking the analyzed model in Q3D into Ansys Circuit Design, allows the simulation of the subcircuit with the project original simulator to be aligned with the circuit simulator. Therefore, a static subcircuit, of the analyzed Q3D model with a defined set of solution data is convenient for further analysis, it will appear in the form of a touchstone N-port data. The number of ports appearing on the subcircuit, depends on the excitations assigned in Ansys Q3D Extractor. Circuit Design is a schematic-based interface, hence allowing the placement of ports, grounds, electrical components and wires.

The objective of utilizing this software is to implement a frequency or a transient domain analysis either with the four-port black box or by creating an equivalent circuit model of the planar transformer by utilizing the quantified values and reduce matrix option in Q3D Extractor. Once the planar transformer model is analyzed and finalized in Q3D, a Circuit Design project is added under the same Q3D project tree. The Q3D project can be simply dragged and dropped in the Circuit Design project, where it will appear as a four-port data subcircuit associated with the excitations appointed in Q3D, as revealed in figure II-24 below.

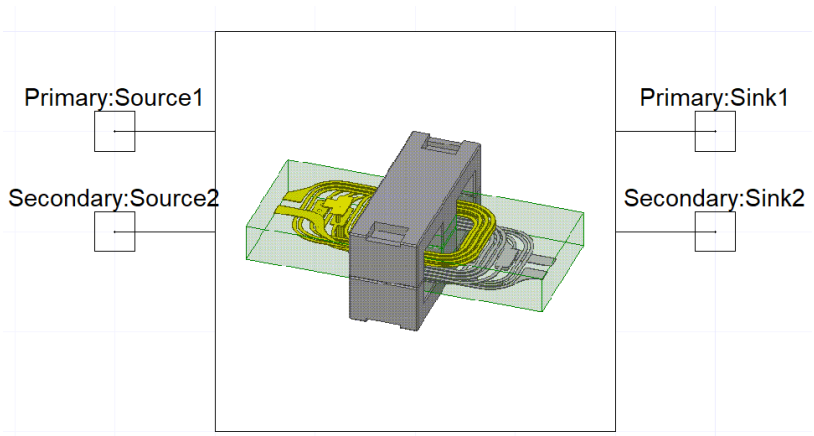


Figure II-24: Four-port subcircuit in Ansys Circuit Design

The frequency domain analysis performed in Ansys Circuit Design by assigning an analysis setup, is vital for the attainment of Scattering (S) parameter results that are needed to authenticate the simulation results and the solution data achieved by Q3D, with the experimental analysis. This is demonstrated in figure II-25, where 50-ohm ports were assigned to the sources and two distinctive grounds, named as global ports, where connected to the sink terminals. It is noted that if the normal

ground connector is utilized, it will be connected to all other grounds, i.e., sink 1 and sink 2 will be connected to each other. Hence, this is why a global port is used instead and is referenced in the port assigned to each source terminal. Moreover, it is imperative to declare that the link definition of the imported subcircuit model can be edited in circuit design. Therefore, the user is entitled to use the reduced matrices options that were performed in Q3D. For example, instead of using the original matrix, the user can link the simulation of the matrix with a grounded net, and perform the analysis in Circuit Design based on a grounded net in the model. This will be further clarified in Chapter three with the application of analyzing the CMTI of the shielded pulse planar transformer.

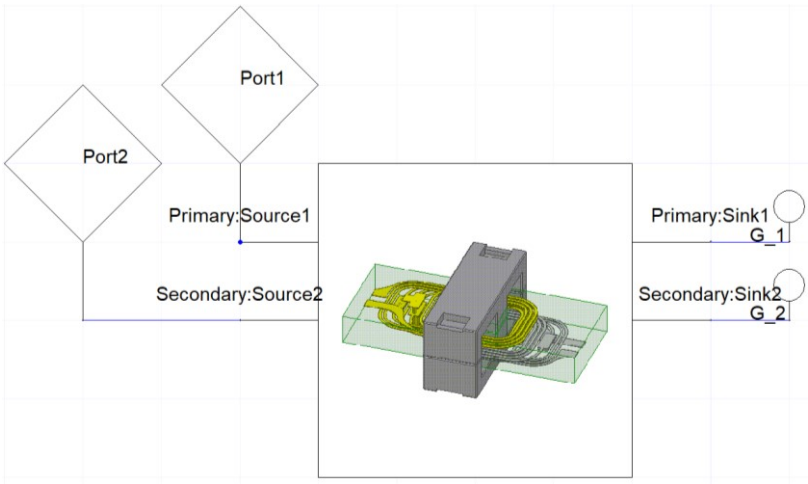


Figure II-25: S parameter analysis in Ansys Circuit Design

Regarding the transient domain analysis, it is setup after manually constructing an equivalent circuit model of the planar transformer using the schematic editor and setting up a designated time domain analysis.

E. CONCLUSIONS

Digital modelling is acquiring intensified recognition in the field of power electronic conversion systems. The conception is to utilize comprehensive simulations that precisely forecast the operation of the system, by permitting to rapidly improve the design, in opposition to fabricating several physical prototypes to examine system performance. The emergence of WBG semiconductors further increased the engagement of artificial analysis integration as the benefits of the rapid switching speed attainments are disregarded when achieved at the expense of EMC adherence.

Ansys Q3D Extractor is the most prominent FEM software tool, when contemplating to extract parasitic parameters of the designed model. This is vital, as the increase in switching transitions lead to high dv/dt occurrences that induce undesirable CM currents to pass through the parasitic parameters. Henceforth, the ability to construct an equivalent circuit model and analyze the design at an early stage will reduce expenses and allow early design renovations. This chapter presented an unprecedented modelling analysis chain that revealed the process of analyzing the design using collective software tools, where not only the examiner is able to analyze the design, but also adjust and incorporate the analysis to other software tools. This process will be the groundwork of verifying

the experimental analysis performed on the existent pulse planar transformers which will be reported thereafter in Chapter three.

CHAPTER III: ENDORSEMENT OF SIMULATION MODELLING TECHNIQUE

The former research conducted at IETR lab by Julien Weckbrodt in year 2020 [78], encompassed the importance of incorporating shielded pulse planar transformers in the gate driver card. The fabrication of the pulse transformers and the shielding examinations were solely based on an experimental approach. Accordingly, this procedure was the basis of constructing an equivalent circuit model of the pulse planar transformers and investigate their CMTI by applying an abrupt dv/dt between the primary and secondary distinctive grounds.

This chapter will interrogate the existent pulse planar transformers by applying the simulation process presented previously in Chapter II. The objective is to formulate a reliable and sufficient simulation methodology to authenticate the experimental results. Moreover, this will formulate the resourcefulness of this investigation to ensure safe operation of the components and determine behavior prediction of upcoming projected examinations. The transformer designs will be exported from Altium Designer and imported into Ansys SIWAVE, to be later analyzed in Ansys Q3D Extractor and dynamically linked with Ansys Circuit Design to perform the intended simulations of extracting the S parameter results and analyze the transformer's susceptibility to a high dv/dt application. The results will be compared to the realized experimental analysis to authenticate the feasibility of the adopted simulation modelling chain.

A. GALVANICALLY ISOLATED GATE DRIVERS

One of the imperative constituents of a power converter system, is the construction of an effective gate driver. A survey conducted by Wolfspeed/Cree on 19/05/2020 in a technical webinar, disclosed that power converter engineers are highly concerned about high dv/dt values than short circuit protection or negative voltage occurrence as reported in figure III-1 below [199].

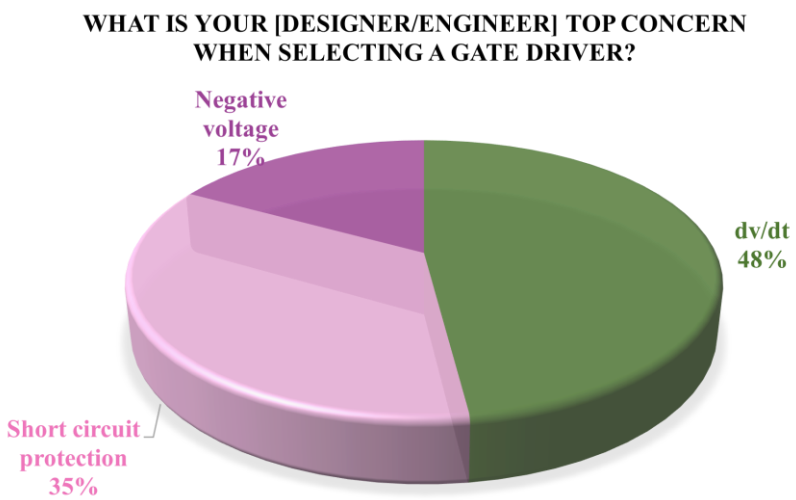


Figure III-1: Relevance of dv/dt phenomenon when selecting a gate driver for a reliable power converter system

The development of WBG semiconductors permitted an upsurge in the attainable blocking voltages of power semiconductors. Applications requiring blocking voltages from 1.2 kV to 10 kV are principally dominated by SiC MOSFETs, by virtue of its minimal on-state resistance [200]. Medium Voltage SiC MOSFETs acquire rapid switching speeds that can result in abrupt dv/dt occurrences amounting to 100 kV/µs. This phenomenon mandates a prerequisite of establishing a very low isolation capacitance in the gate driver circuit [105], [107]. In addition, intense dv/dt stresses shorten the lifetime of the insulation material [201]. High switching transients of SiC MOSFETs, create conflicting undesirable currents that arouse due to unwanted, yet imminent, parasitic capacitances and inductances in the power converter layout or circuitry. Therefore, this increases the vigilance towards EMI disturbances, which included new measures to be conducted when designing a power converter system [202].

In pulse transformer based isolated power converters, there are diversified coupling capacitances that provide a route for CM currents [203]–[205]. The CM currents that circulate in power converter systems can be split into two classifications: 1) CM currents that flow in the power part of the system, via power semiconductors and the ground [206], [207], and 2) circulation of the latter currents in the control through the isolation barriers of the power supplies and signal transmission of the gate drivers [208], [209]. The spotlight of this dissertation is on the second category, particularly the CM currents that circulate through the parasitic capacitances that originate from the signal transmission function of gate drivers [210]. The discussion will not include the parasitic capacitances introduced from the DC-DC power supply, as the latter does not impose direct jeopardization on the safe operation of the semiconductors. However, the pulse transformer utilized to send switching orders to the power modules possesses a very critical and decisive operation. Accordingly, CM current circulation through the interwinding capacitances of the latter might cause a faulty switching order to the power devices, provoking hazardous effects. Figure III-2, highlights in green the parasitic capacitances termed as C_{iso}, of the pulse transformers utilized for signal transmission. Therefore, this renders the gate driver to be an EMI victim in the power converter system as it comprises parasitic capacitances in the isolation barrier, prompting the necessitation of proper design and consideration to mitigate the isolation capacitances and implement EMI reduction techniques [202].

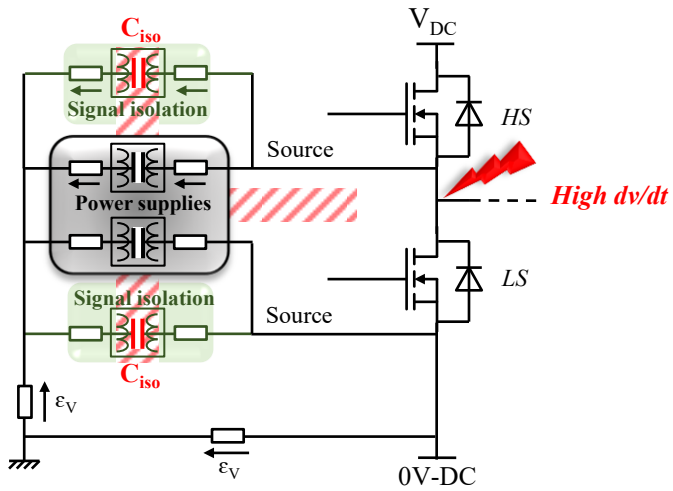


Figure III-2: Pulse transformer parasitic capacitances in a gate driver board

Pulse transformer based galvanically isolated gate drivers introduce interwinding capacitances, that are connected directly to the middle point of the power leg resembling the dv/dt source. Hence, the magnitude of the CM current I_{cm} is precisely affected by the high dv/dt source and the interwinding capacitance C_{iso}, as expressed in (1).

$$I_{cm} = C_{iso} \frac{dv}{dt} \tag{1}$$

Alternative interesting methods have been presented in literature to mitigate CM noise resulting from transformer's interwinding capacitances [211]–[214]. One of the most distinguished solutions is the integration of faraday shielding layers, which are adequately grounded conductive sheets that shunt CM noise current [215]–[218]. This method was implemented to the pulse planar transformers that were designed and fabricated at IETR lab. The objective of the shielding layers is to ensure a lower impedance routing for the CM current, henceforth improving CM performance. Furthermore, developing a definitive, elementary and efficient CM noise model of the pulse transformers is very valuable in the analysis, forecasting and reduction of CM noise. This is legitimate since the interwinding parasitic capacitance of the latter serves as the main route for CM noise [219], [220]. Figure III-3 below represents three configurations of a CM model of a transformer highlighting the necessity and effect of shielding layers on the routing of the latter current.

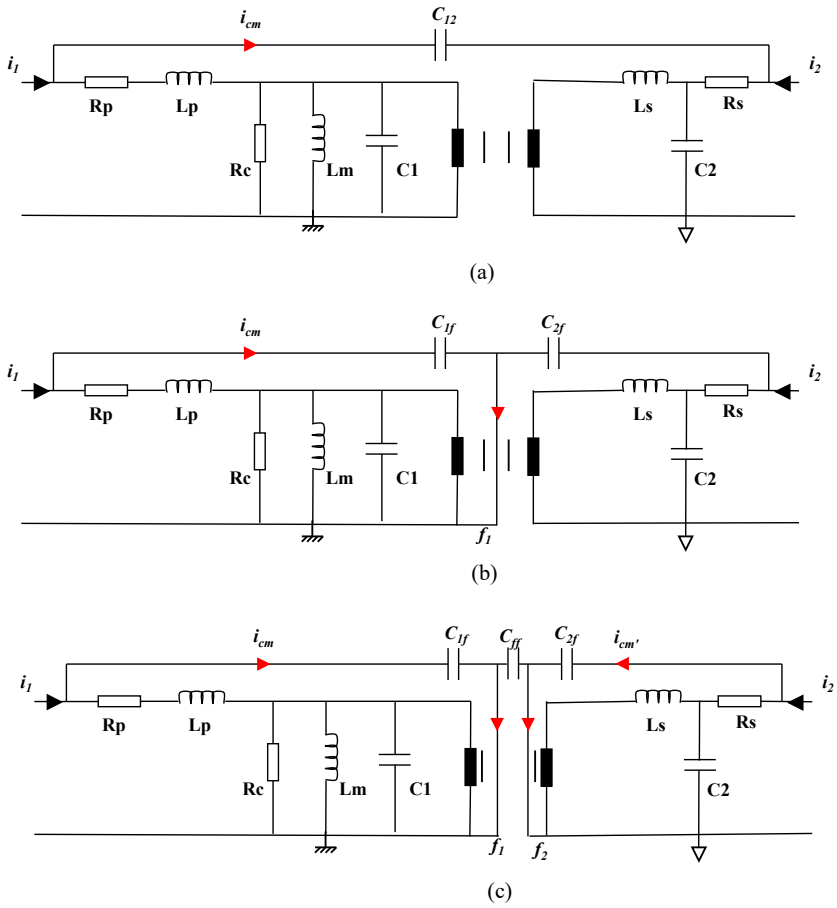


Figure III-3: CM model of a planar transformer (a) without shielding; (b) with one shield; (c) with two shielding layers

Three pulse planar transformers were designed, fabricated and experimentally tested at IETR lab, of which one was without shielding and the other two comprised two inserted shielding layers of typical and large width shields respectively as depicted in figure III-4. The typically shielded transformer covers the windings at the same width, hence at the exact periphery, whereas the large shield slightly surpasses the periphery of the windings. The pulse transformers' design and layout details will be presented in the upcoming section. Moreover, the simulation process will be implemented on the latter to test the transformers' S parameter results and their susceptibility to a high dv/dt amounting to 125 kV/µs which will conform the experimental results already attained and authenticate the proposed simulation process.

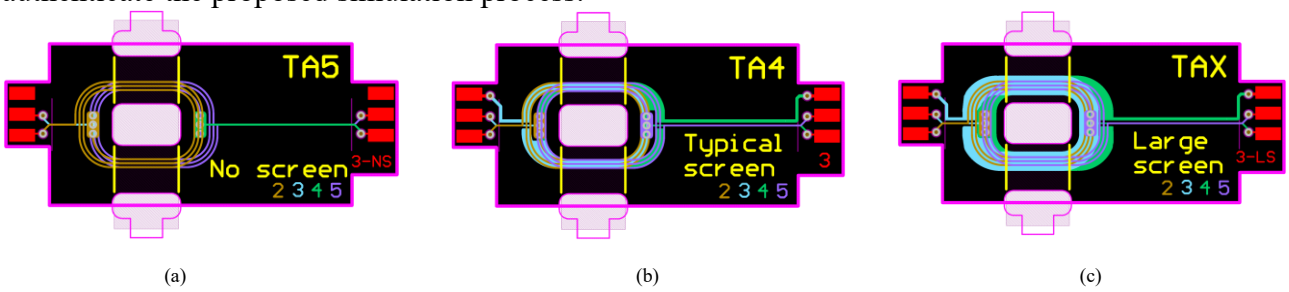


Figure III-4: Altium Designer overview of examined pulse planar transformers (a) without shield; (b) typical shield; (c) large shield

B. PULSE PLANAR TRANSFORMER DESIGN

In conventional gate drivers, only error messages in the event of problems such as short-circuit detection or low power-supply were sent back to the control unit on the primary side from the secondary side. However, in the case of transmission of switching command orders by pulse transformers, the error message returned is ensured by the pulse transformer itself. It is imperative to declare that the transmission of the error signal is carried out by the application of relatively long pulses to the secondary of the transformer as compared to the short period control pulses that command the switching operations. An exemplary of the implementation of this functionality is displayed in figure III-5. Thus, health monitoring of the power components also includes the necessity to consider the communication system which is adapted in a problematic power electronic environment. Thus, as revealed, the transient signal is applied to the pulse transformer, it is consequently decoded on the other side of the transformer. A serial capacitance is connected to the primary side to restrain DC magnetic field from saturating the core. Hence, a bidirectional communication is attainable by the application of longer pulses to the secondary winding, while error messages are sent by the latter so as not to increase the parasitic capacitance by including a devoted transmission line.

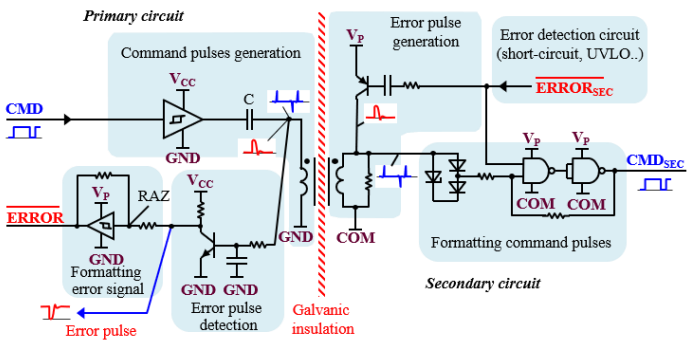


Figure III-5: Error pulse circuit configuration utilizing pulse transformer

B.1 Transformer Scheme

The fabricated pulse transformers, initially designed by Altium Designer, were of planar type, integrated in a six-layer PCB stack, electrically insulated by FR4 epoxy dielectric material and secured with 3F36 EI ferrite core. Four layers were designated for conductors, where the top and underlying conductors represent the primary and secondary windings, while the midst conductors represent the shielding layers. The insertion of two distinctively grounded electrostatic screens is easily achieved when utilizing planar technology. As discussed earlier, the objective of the faraday shielding integration between the winding layers assists in defining a grounded path for CM current flow as depicted in figure III-6. Thus, diminishing EMI disturbances, as they reduce the electrostatic field created by the pulsating currents, whilst securing pulse transmission as they are ineffectual to magnetic field.

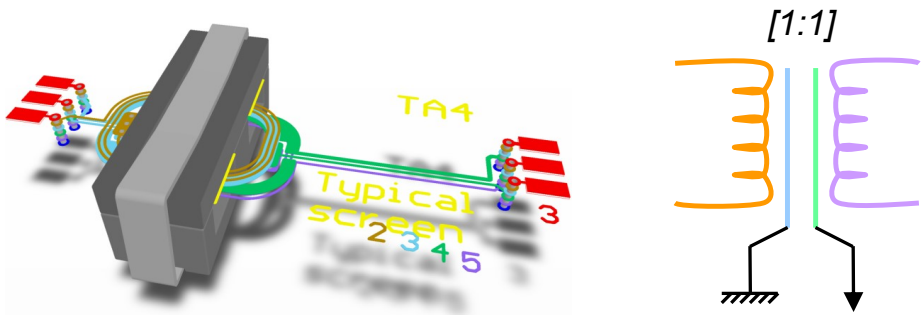


Figure III-6: Pulse planar transformer synopsis

The primary winding is composed of three turns of 150 µm track and shielded with a conductive layer distant at 210 µm, this is mirrored on the secondary side, realizing a turns ratio of 1, however separated by 500 µm of FR4 epoxy material to abide to standards as shown thereafter in figure III-7. Additionally, a nominal distance of minimum 1 mm was considered between the conductors and the ferrite core. The pulse transformers were designed to be integrated in an already existent gate driver card intended to drive two 1200 V SiC MOSFETs as illustrated in figure III-8, aiming to evaluate the merit of grounded electrostatic screens and test the transformer's immunity to sharp dv/dt application.

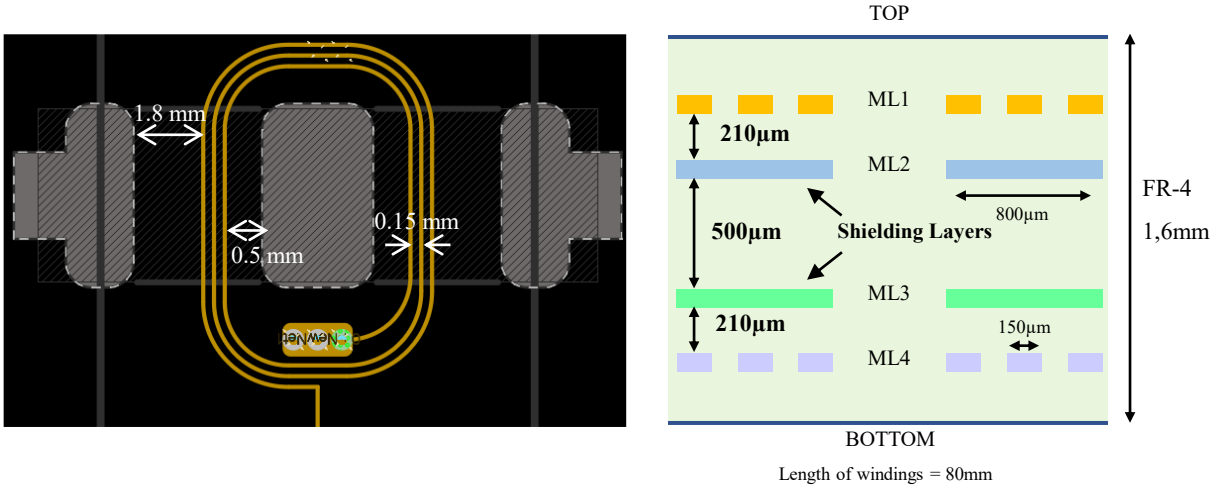


Figure III-7: Pulse transformer architecture and layer stack section view

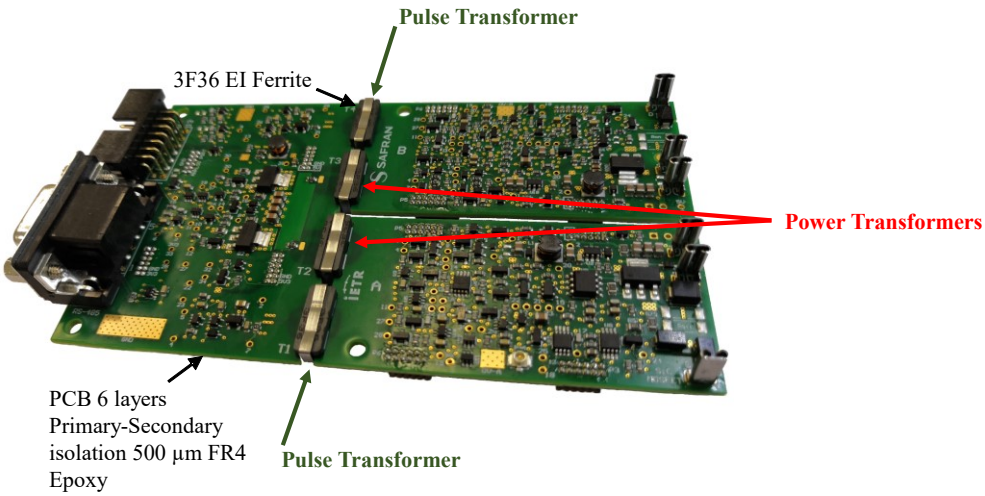


Figure III-8: Pulse transformers integrated in realized gate driver card [78]

B.2 Norm Conformity

Pulse transformers are preconditioned to provide galvanic isolation between the primary and secondary side of the transformer. Knowing that the secondary side is connected to the power module which can attain its maximum power potential. Thus, safeguarding personnel safety is an ultimate objective when designing the pulse planar transformer to adhere to electrical isolation standards. The integration of the pulse planar transformer in the gate driver card is achieved in compliance to the generic standard of PCB design, respecting electrical insulation standards renowned as IPC-2221 standards, regarding design and spacing constraints. Clearance and creepage distances, defining the shortest distance through air between two conductors and the shortest distance over an insulating surface between two conductors, respectively, were considered and measured when designing the pulse planar transformer [221]. Moreover, the insulating material between layer stacks or windings, known as solid isolation, is vital to ensure that conductors will not arc. However, this is not greatly restrictive due to the rigidity of FR4 epoxy dielectric material, which can tolerate 40kV/mm before breakdown. For example, the standards impose a thickness of 500 µm of FR4 for a DC bus voltage of the order of 1500 V which is applied in this design [222]. The norms are depicted in figure III-9 below.

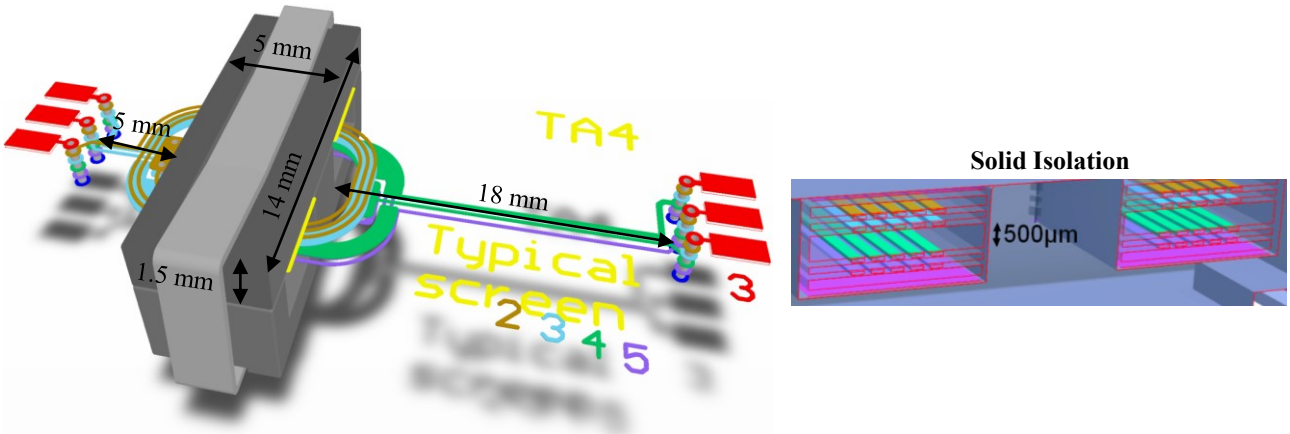


Figure III-9: Pulse transformer design in adherence to norms

B.3 Signal Transmission and Electronic Circuitry

In accordance to [78], Julien Weckbrodt has developed a system that permits the transmission of excitation and blocking orders and synchronous measurement requests to the SiC MOSFET from a single planar transformer. The latter is regulated by the microcontroller unit. This was achieved by implementing a programmed algorithm in an FPGA permitting to distinguish control commands from data pulses. The principle of operation of data and control signal transmission is illustrated in Figures III-10 and III-11 respectively. A positive impulse on the primary winding of the pulse transformer, enforcing power semiconductor activation, whereas a negative impulse invokes device blockage. The transmission of measurement requests has been carried out by the transmission of shortened square pulses of 25 ns duration. However, this requires noise control so that noise is not interpreted as a data.

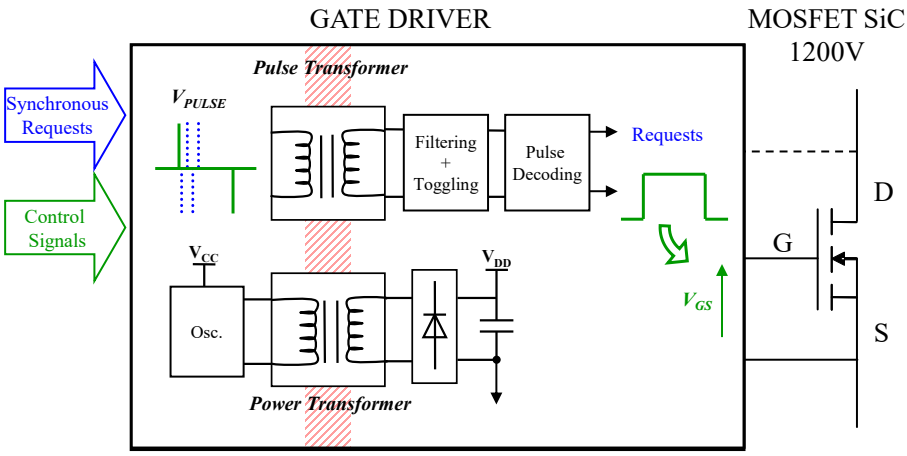


Figure III-10: Principle of operation of data signal transmission

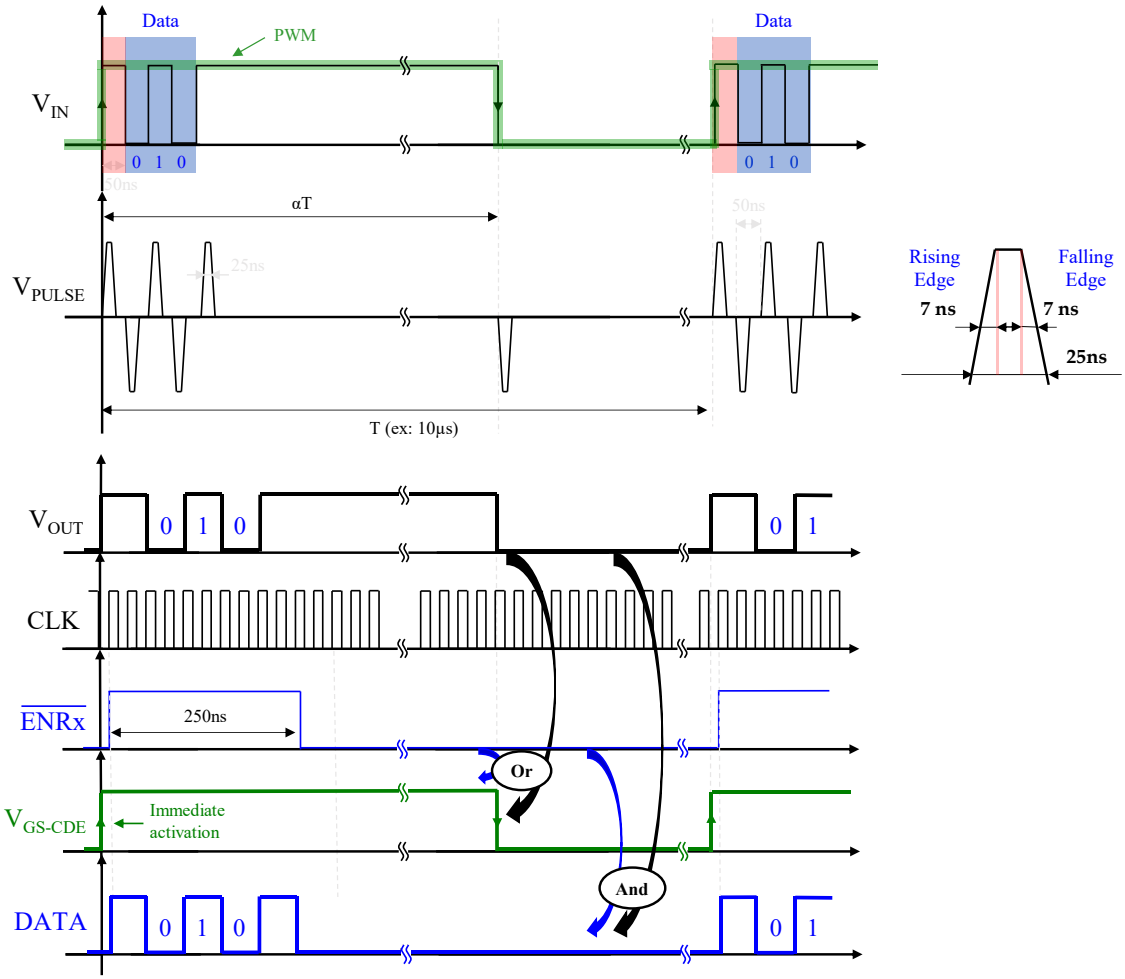


Figure III-11: Pulse transformer signal identification (V_{OUT} indicated in figure III-12)

The pulse generator's electronic circuitry responsible for transmitting switching orders to a power module, as well as data transmission is illustrated in figure III-12. It comprises two NAND logic gates that receive the input signal (V_{IN}) and its inverted equivalent, allowing the election of the rising or falling edge. This operation is based on a sequential logic circuit using a Set/Reset latch principle,

where a positive pulse renders a high logic, and a negative pulse delivers a low output signal. Moreover, the input signal is converted into a transient signal by the usage of the XNOR gate upon the occurrence of state variation. The transient signal duration is determined by the RC filter time response. Furthermore, the signal of 15 V amplitude is buffered to get transmitted through the transformer allowing the signal/noise ratio to be increased. Consequently, a pulse selection stage is essential to disparate between positive and negative pulses. A filter stage is situated to reduce the signal noise making them suitable for a 0-3.3 V logic output. Finally, an R-S flip-flop with a built in Schmitt trigger allows the original signal to be reconstructed from the series of pulses. This, this will guarantee the integrity of the signals in the presence of noise. As a result, any disturbances caused by high switching transients must not corrupt the control signals transmitted, explaining the utilization of low impedances on the secondary circuit.

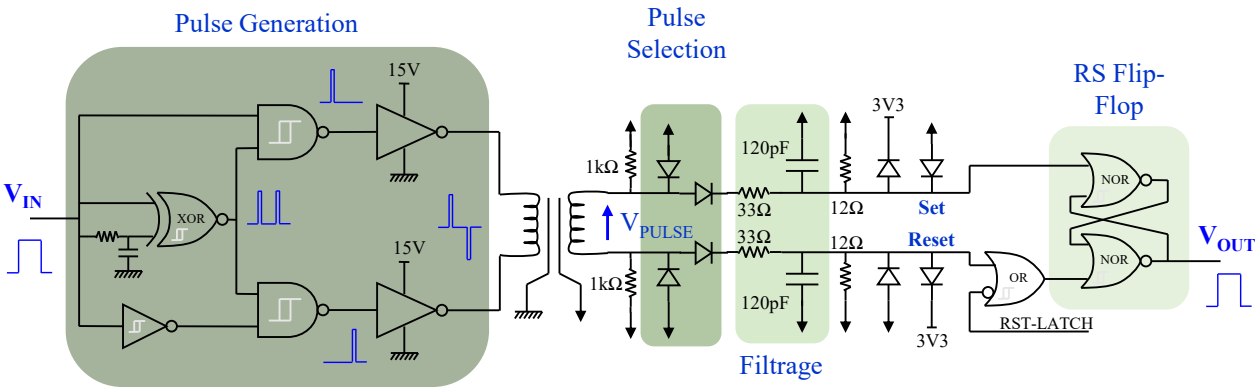


Figure III-12: Pulse transformer electronic circuitry

C. Transformer Scattering Parameters

The primary step of the simulation analysis performed in order to validate the experimental results realized by Julien Weckbrodt in [78] when constructing an equivalent circuit model of the pulse transformer and the examination of its susceptibility to high switching transitions was to conform to his initial utilized method. This was addressed by the questioning about the frequency behavior of the transformer's pulse signal. The method chosen was to measure the S parameters of the transformer over a wide frequency band ranging from 100 kHz to 100 MHz in order to deduce the frequency variation of the model's parameters. Accordingly, a model with constant parameters can be extracted based on adhering to two approaches. The first is based on the extraction of the model at a given frequency f_0 and the second model is obtained by averaging the values over the selected frequency band [f_1, f_2]. Therefore, addressing this issue where the efficient frequency band of the pulse transformer was the primary objective to commence with the simulation analysis process.

C.1 Pulse Transformer Efficient Frequency Band

As previously mentioned, the simulation analysis performed utilizing Ansys software tool requires a specific frequency or an application of an eligible frequency sweep. Therefore, a spectral analysis was performed to anticipate the frequency band of the short pulse transmissions. The employment of

WBG technology triggers the maximization of the gate driver's switching frequency by the usage of short pulses with a duration of 25 ns, elected in accordance to the pulse generator (UCC27517DBV) employed.

The signal was represented via MATLAB for a frequency bandwidth analysis using the Occupied bandwidth (obw) function, where the results of the trapezoidal pulse spectral analysis are revealed in figure III-13.

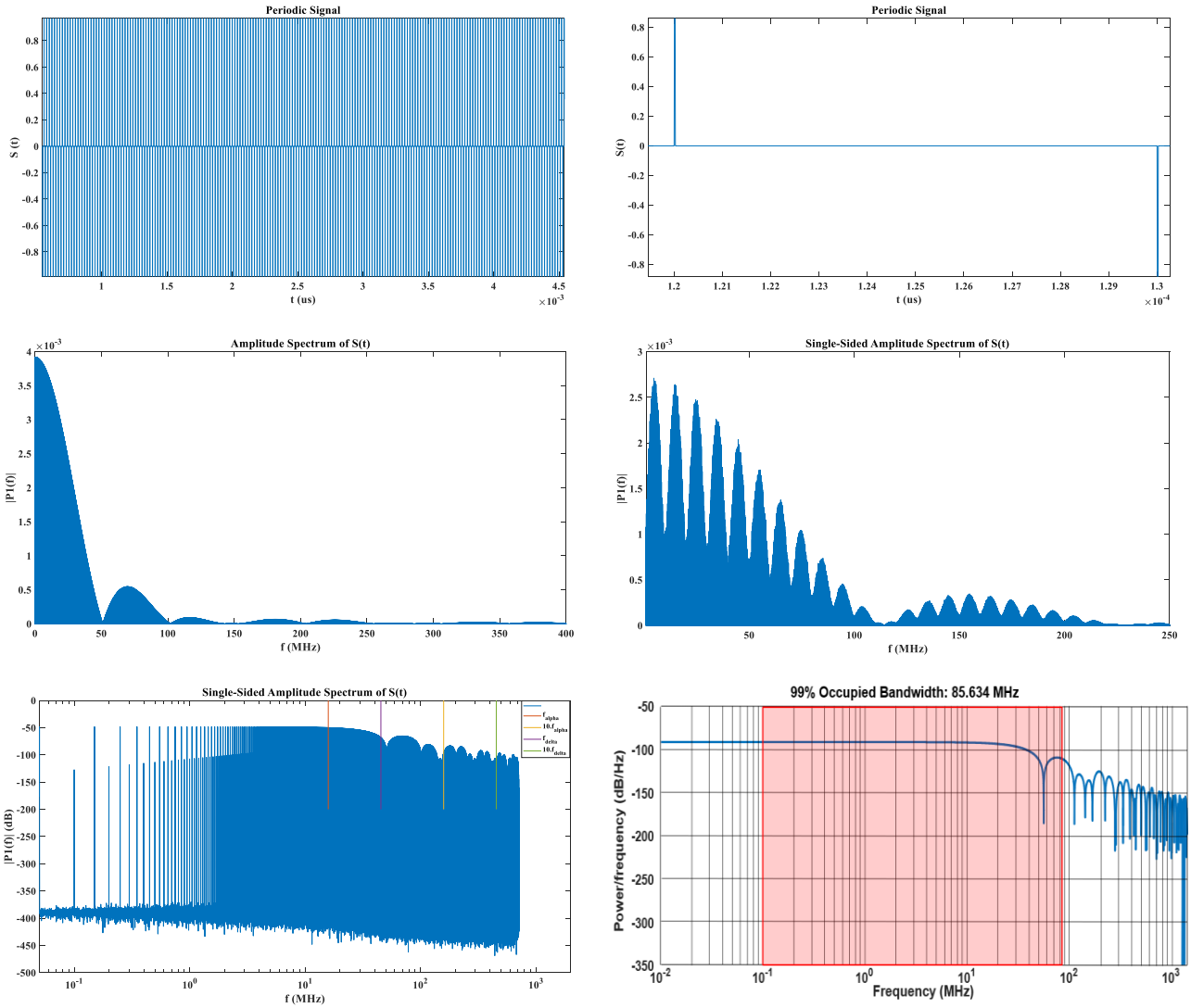


Figure III-13: Pulse signal spectral analysis

In observance to figure III-13, mainly to the obw function result, the analysis of a 100 kHz PWM with a 50% duty cycle and a sampling time of 0.7 ns, reveals that 99% of the occupied bandwidth ranges from approximately 100 kHz till 85.7 MHz, serving as the eligible applicable frequency band needed to be utilized in the executed simulations. Therefore, this frequency range will be used in Ansys software tool to examine the performance of the pulse planar transformer. The primary step implemented was to perform the simulations intending to extract the S parameters of the transformer and validate the results experimentally.

C.2 S Parameter Analysis – Ansys Q3D Extractor

In order to conduct the S parameter analysis and simulate the design in Ansys Q3D Extractor. The designed models were primarily exported from Altium designer and imported into Ansys SIWAVE, as described in the simulation process presented in chapter 2. This is illustrated in figure III-14 using the typically shielded pulse transformer, where a similar practice was conducted on the no shield and big shield transformers. It is noted that the ferrite core is not imported into Ansys, only the planar stack up of the transformer is identified in SIWAVE, hence, the EI ferrite core is separately designed in Ansys Q3D in accordance to ferroxcube datasheet specifications E/14/3.5/5/R as shown I figure III-15 [223].

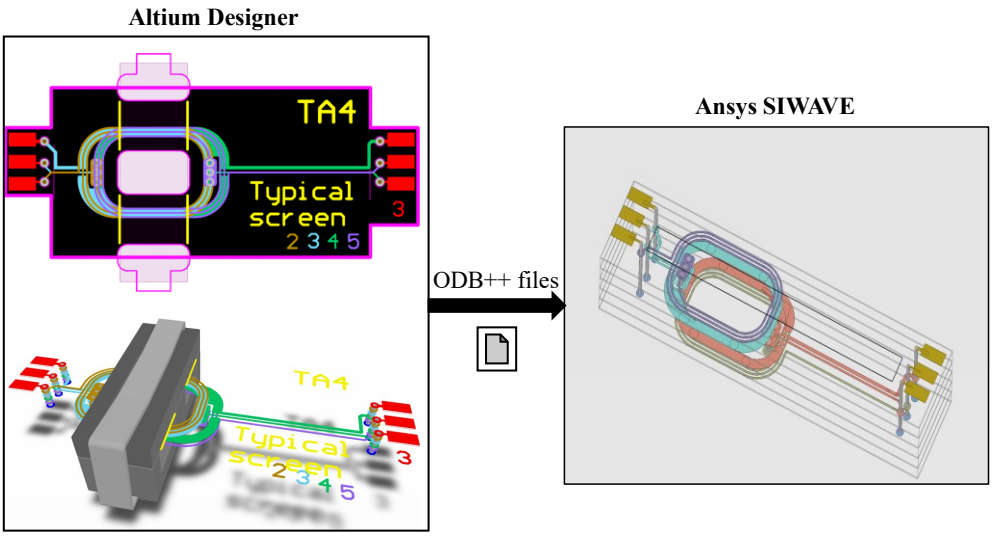


Figure III-14: Importing ODB++ files of Altium designed model into Ansys SIWAVE

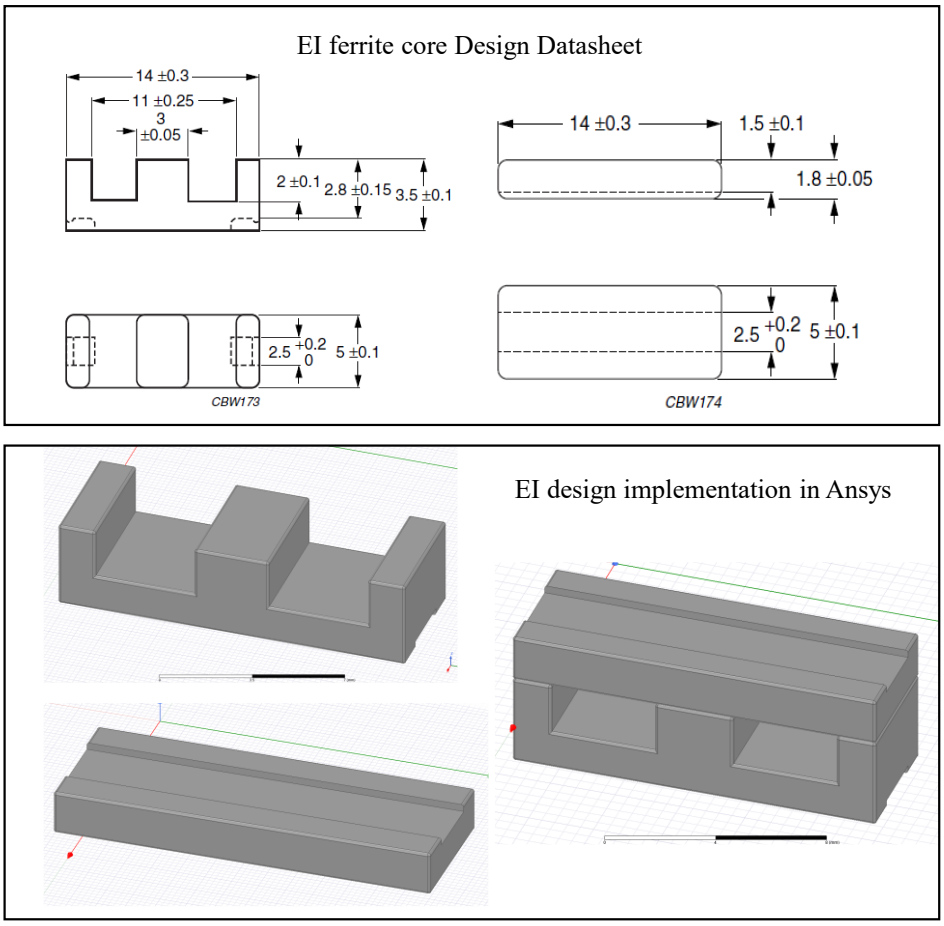


Figure III-15: EI ferrite core design specifications [223]

After specifying the layer stack up of the planar transformer in SIWAVE in accordance to the specified segregation distances formerly demonstrated in figure III-7, the model can be exported from within SIWAVE into Ansys Q3D Extractor for further analysis as represented in figure III-16 [224].

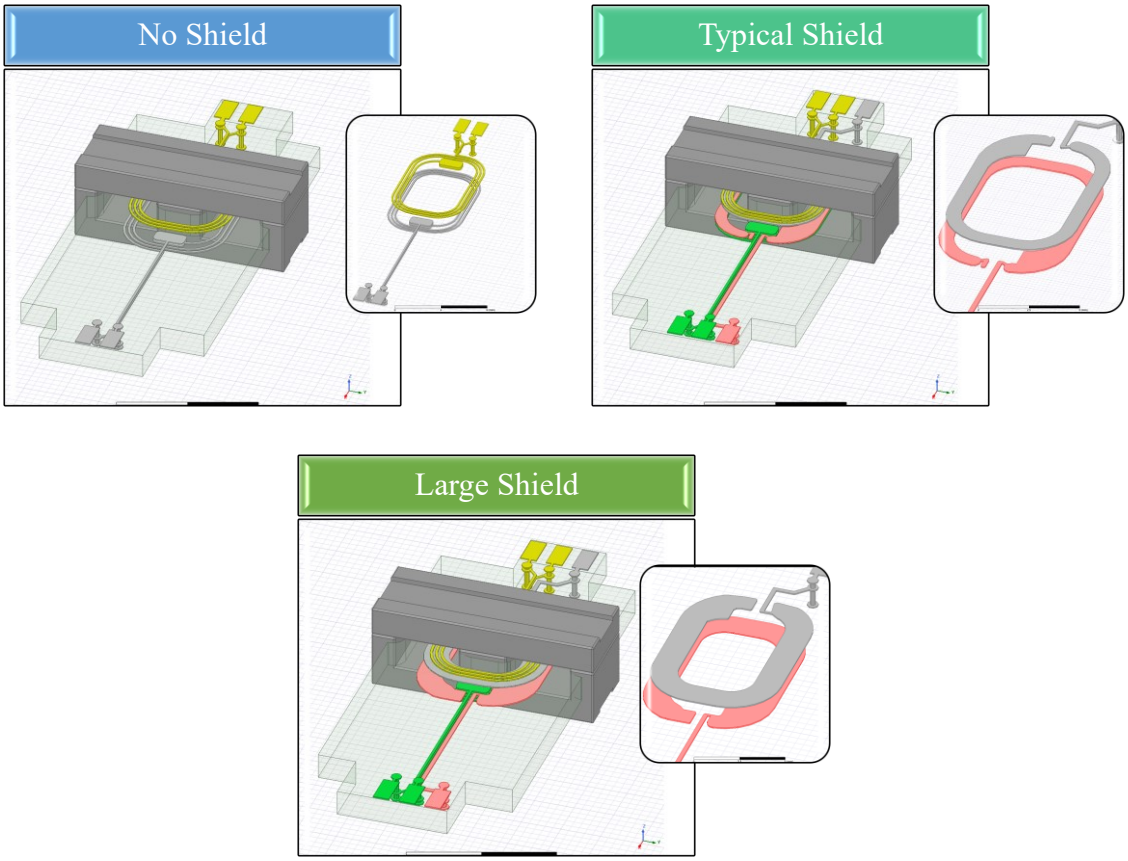


Figure III-16: No shield, typical shield and large shield pulse transformers in Ansys Q3D

S parameter simulation analysis was performed to examine and authenticate the electrical behavior of the pulse planar transformer. This was implemented by simulating the pulse planar transformer over the efficient frequency span ranging from 100 kHz till 85 MHz in Ansys Q3D Extractor after assigning the precise material, nets and excitations. Thus, the conductive layers were assigned as nets, and this step is vital to extract the CG matrix. Excitations, named as source and sink were assigned to the windings of the transformer, simulating where the current enters and exits the windings which will compute the AC RL and DC RL matrices. An illustration is depicted in figure III-17 identifying the nets and excitations. Moreover, a setup analysis is identified to compute all RLGC parameters and at this point the validated design is ready to be analyzed.

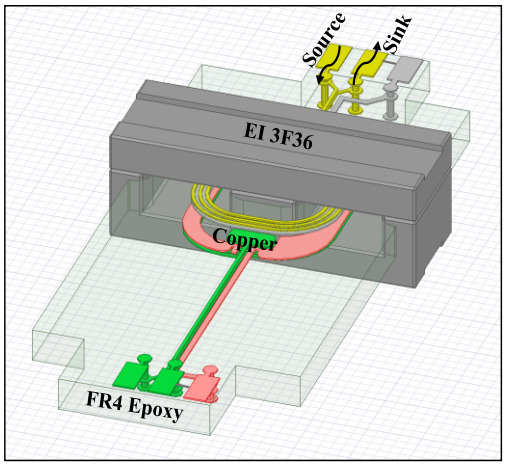


Figure III-17: Pulse transformer setup in Ansys Q3D Extractor

Upon the completion of the analysis, the transformer can be placed in a schematic-based interface to complete the simulation and acquire the simulated S parameter results in accordance to the implemented experimental analysis which was conducted using a Vector Network Analyzer (VNA).

C.2.1 Ansys Circuit Design Dynamic Link

The model is dynamically linked or inserted into Ansys Circuit Design by simply adding under the same project tree of Ansys Q3D an Ansys Circuit design project. The analyzed Q3D model project can be simply dragged and dropped into the Ansys Circuit Design project to perform further desired studies. The model will appear as a four port sub-circuit, in accordance to the assigned source and sink excitations for the primary and secondary windings in Ansys Q3D. Portraying an experimental analysis, two fifty-ohm impedance interface ports were associated to the source pins, as they represent the current entrance pins. Whereas two disparate grounds were connected to the sink pins which represent the current exit pins. It is noted that the two shielding windings are connected to the distinctive grounds of the primary and secondary windings. As concerning the analysis setup, the frequency domain scattering parameters are measured by realizing a frequency domain analysis through assigning a Linear Network Analysis (LNA) over the specified frequency span. The analyzed model in Ansys Circuit design is portrayed in figure III-18.

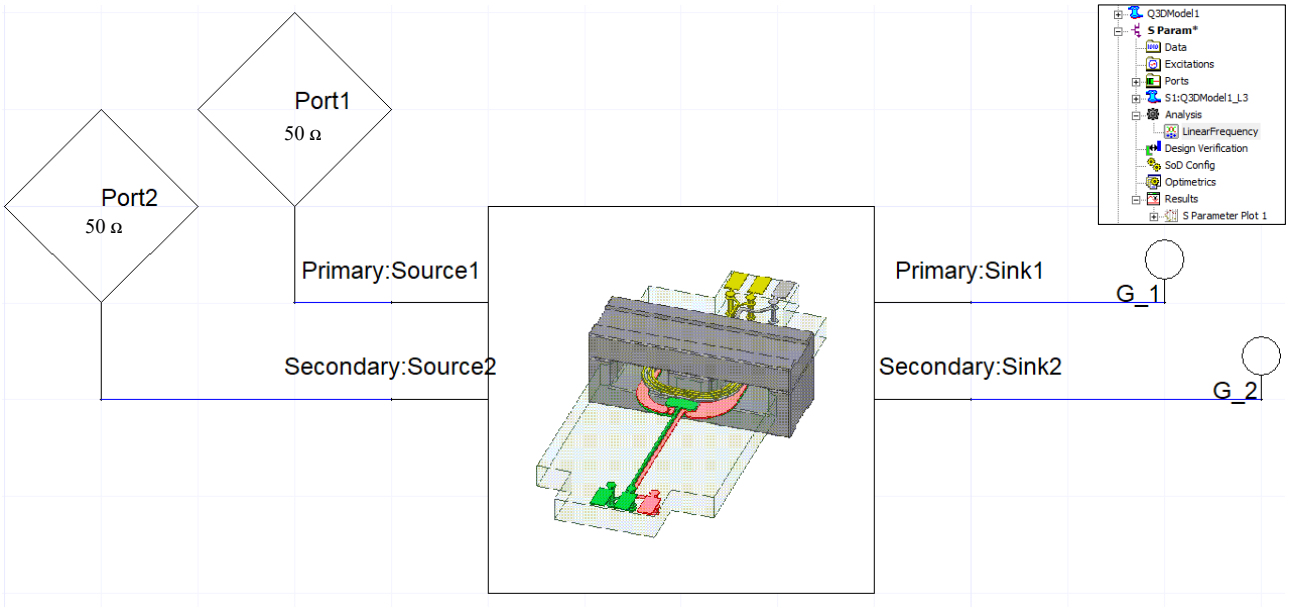


Figure III-18: S Parameter simulation analysis of dynamically linked model in Ansys Circuit Design

After the analysis is finalized, the S parameter results can be reported and extracted for comparison with experimental attainments which will be conferred in the subsequent section.

C.3 S Parameter Experimental Validation

The modelled pulse planar transformer was assembled in accordance with the design features previously stated, to endorse the simulated results. Hence, a fifty-ohm Vector Network Analyzer (VNA) was employed to observe the transformer's S parameter measurements as seen in figure III-19. The compliant S parameter results over the desired frequency range is displayed in figure III-20 for the three types of transformers analysed. The figures represent the adherence of the dashed simulation results to the experimental ones depicted by solid lines. S12 and S21 describe the transmission coefficients from ports 1 to 2 and 2 to 1 respectively and vice versa. Moreover, the reflection coefficients of ports 1 and 2 are termed as S11 and S22 accordingly [225]. Additionally, the unity of S11 and S22 and S12 and S21 in each of the simulation and experimental results is due to the symmetrical structure of the pulse planar transformer. The agreeable results attained justify the utilization of the all the involved software tools that will farther allow the investigation of the transformers' susceptibility to high switching transitions and the competency to construct their equivalent circuit model.

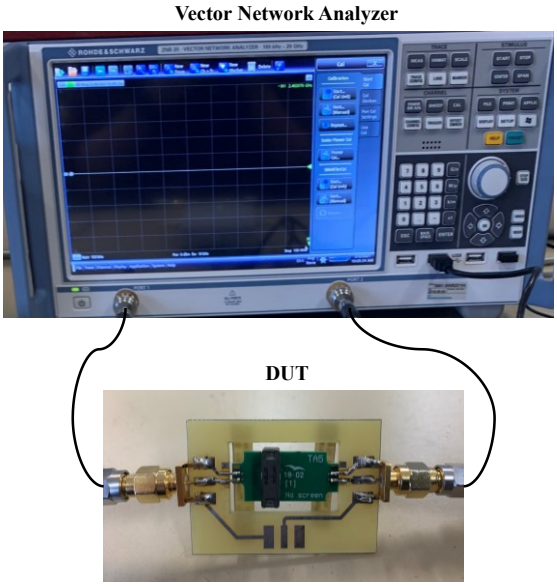


Figure III-19: S parameter experimental analysis using VNA

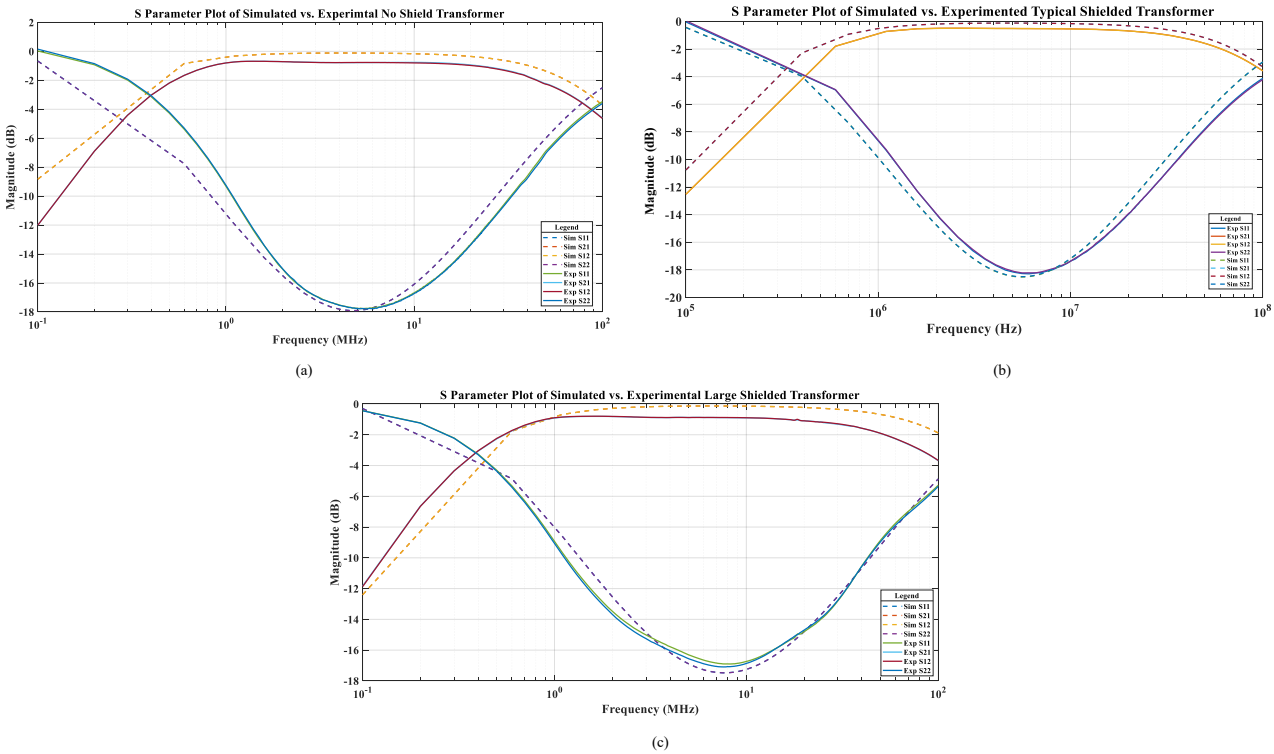


Figure III-20: Experimental authentication of S parameter results of pulse transformers (a) No shield; (b) Typical shield; (c) Large shield

It is imperative to proclaim that this experimental verification was performed to reveal result conformance which authorized reliable reliance on the simulation analysis implemented. Thus, reinforcing the ability to propose an equivalent circuit model of the planar transformers relying on ANSYS Q3D Extractor RLGC parameters conferred thereafter.

D. COMMON MODE TRANSIENT IMMUNITY

For authentic circuit simulations of power converters, a reliable electrical model of high frequency transformers is imperative especially when conducting a transient analysis [226]. Diversified techniques have been refined to simulate the behaviour of high-frequency transformers under different conditions. One of the methods is based on anticipating the equivalent model parameter values in correspondence to experimental analysis, such as curve fitting [227], [228] and evolutionary algorithms [229], [230]. An alternative approach is constructing a model based on physical characteristics including core and winding dimensions [68], [227]–[231]. This will permit the implementation of an equivalent circuit model based on lumped electrical parameters comprising of resistors, capacitors, and inductors.

This section will demonstrate the simulation and experimental validation of the transformers' CMTI when applying a high dv/dt application between the transformers' primary and secondary grounds. This will first be tested by the equivalent sub-circuit generated by Ansys Q3D Extractor and imported into Ansys Circuit Design, which will accordingly permit the construction of an equivalent circuit model-based susceptibility test. The results will be experimentally validated aiming to ensure the impact of inserting grounded electrostatic screens on the components' EMC compliance. The aim of the inserted faraday shielding layers which are connected to the reference of the primary and secondary circuits is to shunt the CM current passing through the transformers' parasitic capacitances to the ground plane intending to minimize EMI. However, the screen utilization can become counterintuitive if not properly grounded as this will introduce additional parasitic capacitance amidst the windings and therefore increase the EMC disturbances. Hence, the design and routing of these transformers shall be performed diligently as the geometry of the design possesses a considerable impact on the dv/dt immunity test of the transformer.

D.1 Sub-Circuit dv/dt Immunity Test

The first examination attempt of the pulse planar transformers' endurance to an application of a steep dv/dt amounting to 125 kV/µs, which simulates a severe switching condition of the power semiconductors. This was co-simulated in Ansys Circuit Design after finalizing the analysis of the transformers in Ansys Q3D Extractor. This was implemented to the no shield, typical shield and large shield transformers aiming to evaluate the merit of the insertion of the grounded electrostatic screens when driving 1200 V SiC MOSFETs using a 100 kHz frequency PWM signal and authenticate the simulation process proposed. Hence, the imported Q3D subcircuit with the identified ports in circuit design is constructed in accordance with the pulse transformer electronic circuitry previously presented and displayed thereafter in figure III-21. The imported circuit is linked, and the link definition is adjusted in Circuit Design by altering the original matrix to a ground net matrix. This means that the transformer will be tested by grounding the shielding layer integrated and not keeping it as an identified net. Hence, this will harmonize the experimental analysis and allow the check of the importance of the grounded electrostatic screens. A piecewise linear source was placed to simulate the exact application of the dv/dt source applied experimentally by a Haefely generator at IETR lab

by importing the potential variation into Ansys Circuit. Thus, this aims to originate a legitimate simulated framework, where the explicit 25 ns pulse signal and the dv/dt application are reproduced and applied on the transformer's primary side as demonstrated in the figure below. This exemplifies the typically shielded pulse transformer, however, a similar application was implemented on the remaining transformers.

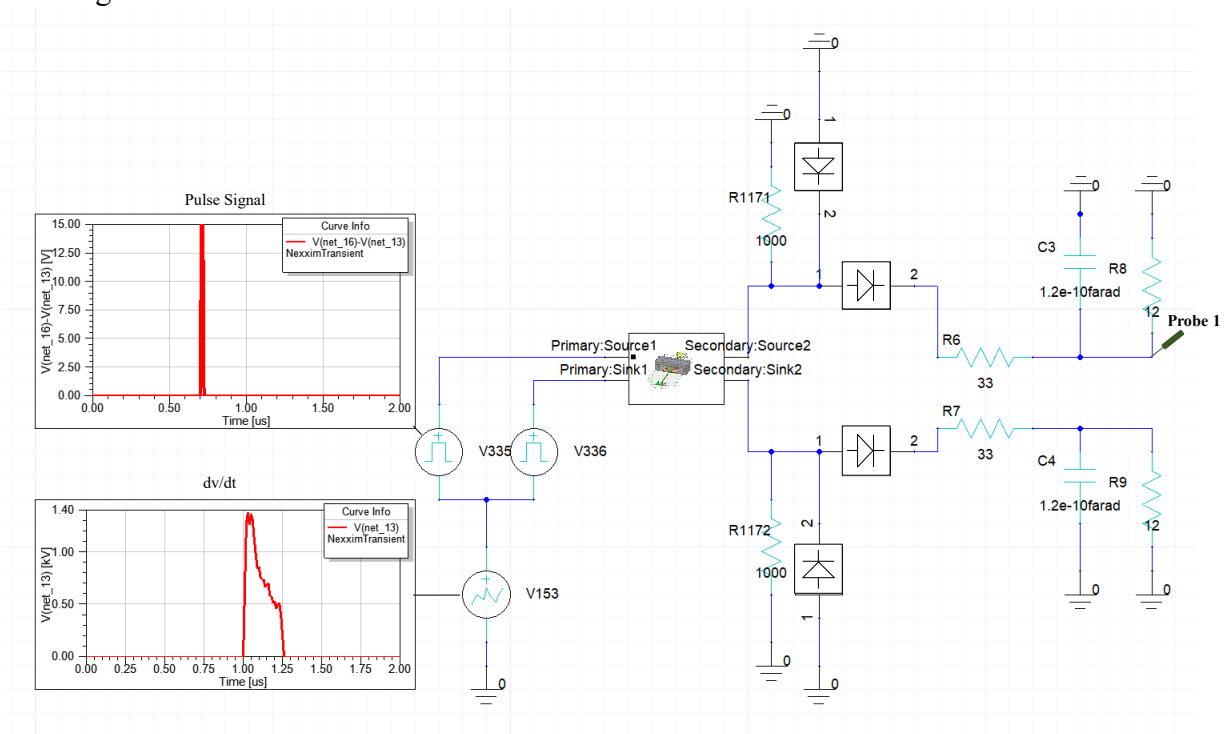


Figure III-21: dv/dt immunity test of pulse transformer's subcircuit in Ansys Circuit Design

A transient analysis setup was applied ranging between 0 µs and 2 µs, the 25 ns pulse signal was transmitted after 0.7 µs, and the application of the abrupt common mode transient voltage (CMTV) of 125 kV/µs between the primary and secondary grounds originated at t=1 µs. The output results representing the Common Mode Transient Noise (CMTN) of all the transformers, measured and identified at probe 1 are summarized in table III-1. The CMTN corresponds to the voltage level at the secondary measured after the application of a dv/dt between the primary and secondary separate grounds. It should be inspected as a maximum dv/dt application might cause dangerous CMTN results that surpass the identified voltage threshold rendering it incompliant to EMC standards. The promising results revealed the influence of the inserted grounded faraday shielding layers as the shielded designs produce mitigated CM noise in comparison to the unshielded transformer. Moreover, the experimental verification of the generated noise results attained at the output will be demonstrated consequently in section D.3.

Table III-1: Simulated dv/dt immunity test results

Transformer Type	CMTN (V)
No shield	0.8
Typical shield	0.6
Large shield	0.66

D.2 Equivalent Circuit Model Susceptibility

After performing the dv/dt immunity test to the transformer's equivalent circuit as a black box extracted from Ansys Q3D, the impending approach is to construct the CM equivalent circuit model of the transformer and implement a similar simulation on the entire characterized model. This will further reinforce the validity of the simulated results prior to achieving an experimental analysis. This section will demonstrate the process of constructing the equivalent circuit model at a defined frequency after extracting the parameters of the transformer on the entire eligible frequency range. The typically shielded pulse transformer will be demonstrated, acknowledging a similar process for the remaining transformers.

D.2.1 Generic Corresponding Circuit Model

A general and symmetrical CM current modelling of the pulse planar transformer is presented in figure III-22 below. The equivalent circuit model reveals the ideal transformer with a turn's ratio m, magnetizing inductance L_m, core resistance R_C, stray capacitances C_W, C_{mc1} and C_{mc2}, Leakage inductances L_P and L_S and winding resistances R_P and R_S. This model will be used to portray the transformer's behavior and test its susceptibility to a stressful switching transition which can be correlated to the formerly executed test utilizing the black box generated from Q3D Extractor.

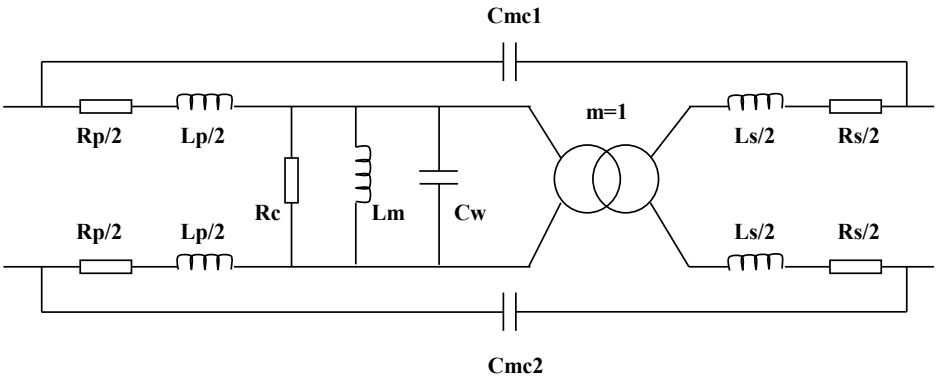


Figure III-22: Generic CM current model of the pulse planar transformer

D.2.2 Pulse Transformer Parameter Extraction

Aiming to quantify the previously displayed transformer generic model, Ansys Q3D Extractor was used to extract the displayed parasitic parameters. As previously stated, the model was setup for analysis in the software tool and an adequate frequency sweep was assigned ranging from 100 kHz till 85 MHz to extract the desired RLGC parameters. After a successful analysis, the reduce matrix element was used to quantify the model parameters by allowing the user to perform complementary floating, return path and grounding net matrices. The most influential parameter on the CMTI of the transformer and consequently, the CMTN voltage level is the interwinding capacitance between the primary and secondary windings. Hence, to be able to quantify C_{mc1}, the ground matrix was used to

ground the secondary shielding layer of the transformer. Similarly, to quantify C_{mc2}, the ground net matrix will be applied on the primary shield of the transformer. Therefore, when the export circuit is utilized, the user can alternate between the two distinctive reduced matrices in order to construct the equivalent circuit model.

After analysis completion over the acceptable defined frequency range in Q3D Extractor, from 100 kHz till 85 MHz, the RLC parameters were evaluated as shown in figure III-23, which demonstrates the stability of the parameters over the applied frequency band. The primary purpose of this realization is to perform a dv/dt susceptibility test of the equivalent model of the pulse transformer at a defined frequency.

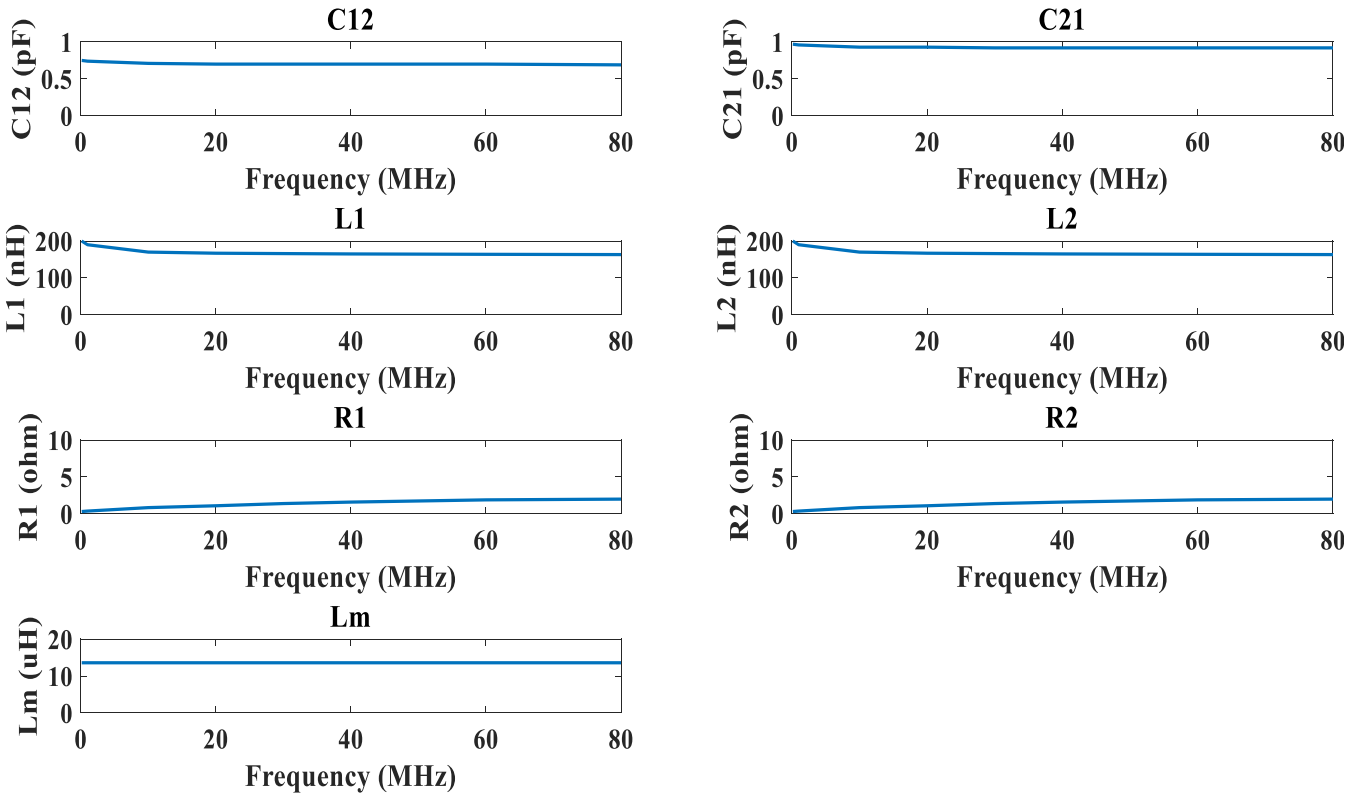


Figure III-23: Stability of RLC extracted parameters over frequency range

The quantification of the RLGC parameters determined over the implemented frequency span is demonstrated in table III-2 below. The steadiness of the parameters holds great convenience despite the negligible slight variation of RP and RS due to the occurrence of skin effect phenomenon.

Table III-2: Ansys Q3D Extractor RLC parameters of typically shielded transformer

Frequency (MHz)	C_{mc1} (pF)	C_{mc2} (pF)	R_P (Ω)	R_S (Ω)	L_P (nH)	L_S (nH)	L_m (µH)
0.1	0.75	0.97	0.32	0.32	200	200	13.6
1	0.74	0.96	0.38	0.38	190	190	13.6
10	0.71	0.93	0.85	0.85	170	170	13.6
20	0.7	0.93	1.1	1.1	167	167	13.6
30	0.7	0.92	1.4	1.4	166	166	13.6
40	0.7	0.92	1.6	1.6	165	165	13.6
50	0.7	0.92	1.7	1.7	164	164	13.6

60	0.7	0.92	1.9	1.9	164	164	13.6
70	0.7	0.92	1.92	1.92	163	163	13.6
80	0.69	0.92	2	2	163	163	13.6

Aiming to create a specific equivalent circuit model of the transformer irrespective of the assigned frequency, two approaches were executed. Initially, the values of the parameters were averaged over the applied frequency range. Furthermore, the second approach was performed by analyzing the design at two distinctive frequencies which are 10 MHz and 50 MHz to review the results. Correspondingly, both suggestions granted a congenial compliant result. Thus, an equivalent circuit model of the typically shielded pulse planar transformer at 50 MHz frequency is defined in figure III-24 below.

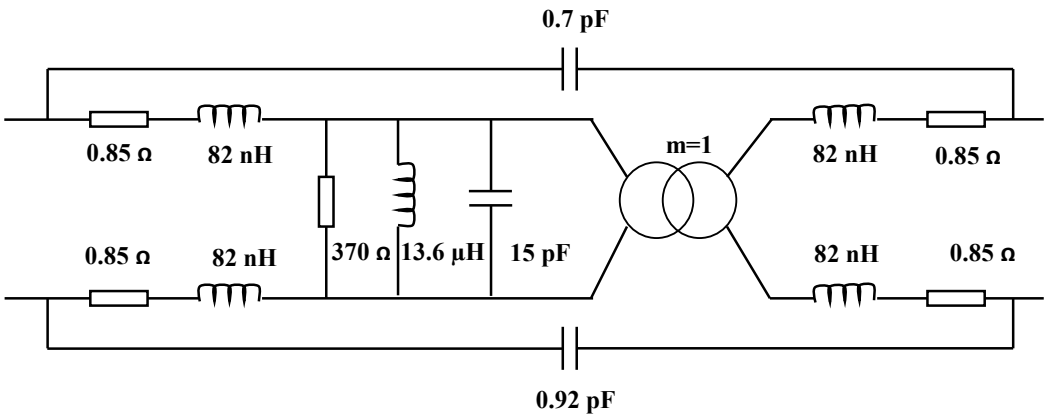


Figure III-24: Equivalent circuit model of typically shielded pulse transformer at 50 MHz

D.2.3 Equivalent Model Susceptibility Test

The constructed equivalent circuit model of the pulse planar transformer was also subjected to the high dv/dt of 125 kV/µs between the primary and secondary distinctive grounds in Ansys Circuit Design as revealed in figure III-25. The result attained was approximately 0.6 V, which corresponds to the result achieved when simulating the equivalent subcircuit model of the transformer.

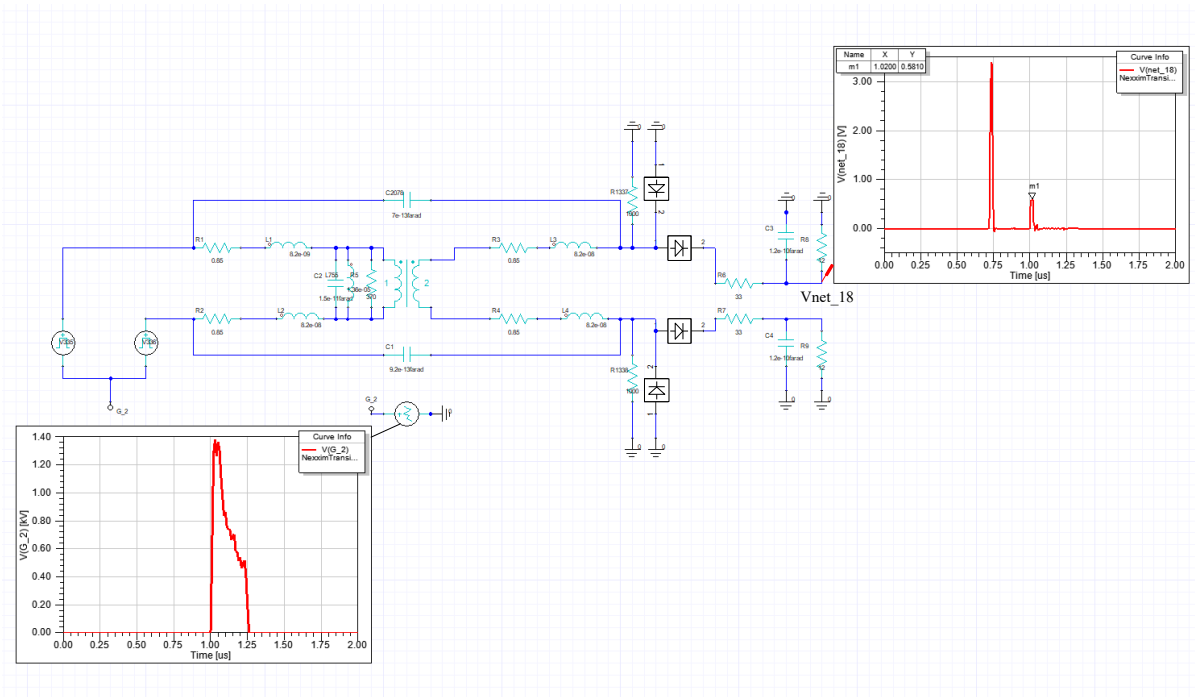


Figure III-25: CMTI simulation test results of equivalent circuit model of typically shielded pulse transformer

Similarly, the analysis was conducted on the remaining transformers and the attained results of the equivalent circuit models' CMTN is demonstrated in table III-3 below. As revealed, the results achieved are agreeable with the ones attained from the subcircuit analysis.

Table III-3: CMTN voltage level of pulse planar transformers' equivalent circuit models

Transformer Type	CMTN (V)
No shield	0.8
Typical shield	0.6
Large shield	0.6

D.3 Experimental Examination

D.3.1 Experimental Circuit Arrangement

The three pulse planar transformers that were already fabricated and tested at IETR lab were subjected to the testing conditions experimentally by the development of a structured experimental setup aiming to examine their dv/dt immunity. The obtained results will be compared to the simulated ones to verify the simulation process and organize a concrete foundation to construct and simulate ameliorated and optimized designs where the user will be able to alter diverse aspects of the model in a reliable testing platform.

The transformers' susceptibility to abrupt dv/dt occurrences was carried out under severe switching conditions to check the reliability of the transformers and the effectiveness of the inserted grounded faraday shielding layers. The generated switching disturbances amounted to 125 kV/µs. A function generator was utilized to deliver the pulse signals at 100 kHz with 0.5 duty cycle. The

recreation of a switching transition of a power semiconductor was applied between the primary and secondary distinctive grounds by using a Haefely generator. This specific dv/dt slope was implemented as it represents the maximum theoretical switching speed of the power module multiplied by a safety factor of four. The measurements of the relevant signals were performed using a battery-powered oscilloscope which was connected to the reference potential of the secondary (floating) circuit. It is imperative to wear personal protective equipment (PPE) during this testing procedure. The representation of the installed experimental setup is depicted in figure III-26 where the outcome result will be measured at channel 1 after applying a set signal.

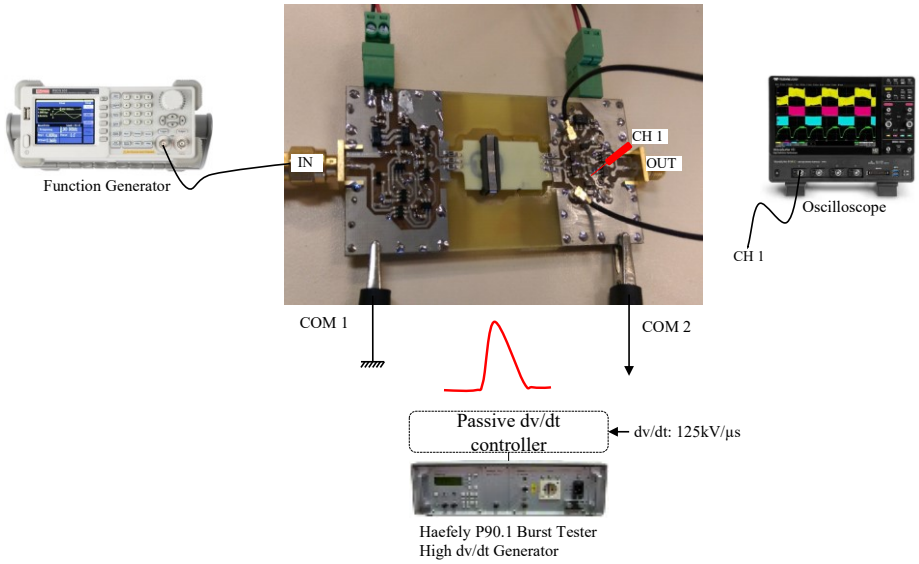


Figure III-26: Pulse planar transformer experimental setup for dv/dt immunity test

D.3.2 dv/dt Immunity Results

The rising common-mode voltage of the pulse planar transformer was monitored upon the application of a sharp dv/dt of 125 kV/µs, whilst ensuring that the input is tied to a low logic retaining the transistor to off state. This is very imperative as the occurrence of a faulty parasitic turn on can cause a critical short circuit incident. The examination was accomplished by transmitting a transient signal after 0.7 µs to invoke a switching on order, nonetheless, at 1 µs a common mode transient voltage (CMTV) of 125 kV/µs was applied between the primary and secondary disparate grounds. Fig. III-27 illustrates the correspondent simulated and experimented applied CMTV by the Haefely generator.

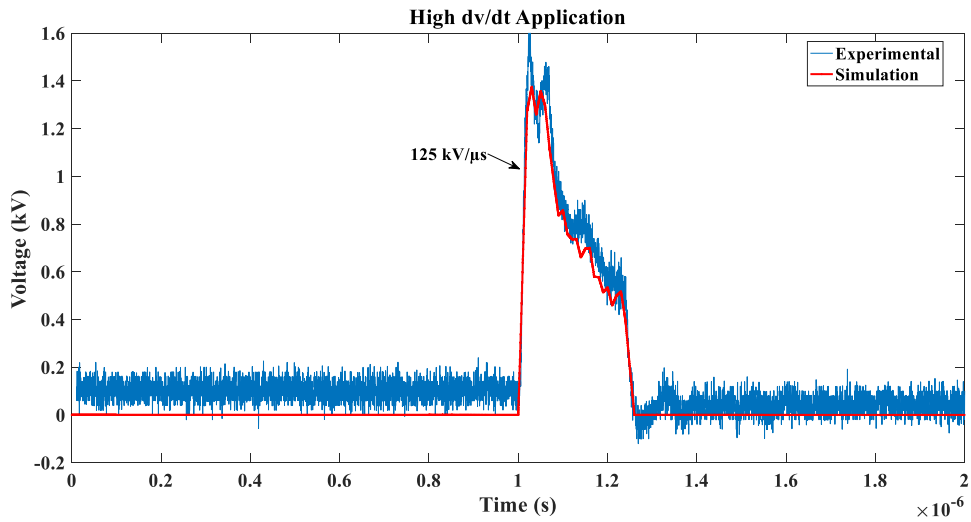


Figure III-27: Experimented vs. simulated abrupt dv/dt application

Succeeding an input signal transmission, the CMTI test of the typically shielded pulse planar transformer was measured at the set input of the NOR gate flip flop of the pulse transformer electronic circuitry. The simulated and experimented results are revealed in figure III-28 below, both displaying approximately 0.6 V of CMT parasitic voltage. It is noted that the comparison was performed with the subcircuit analysis in Ansys Circuit Design. The result is inconsequential corresponding to the threshold voltage of (VT+=1.88 V) of the applied Schmitt-trigger logic gate circuitry [232].

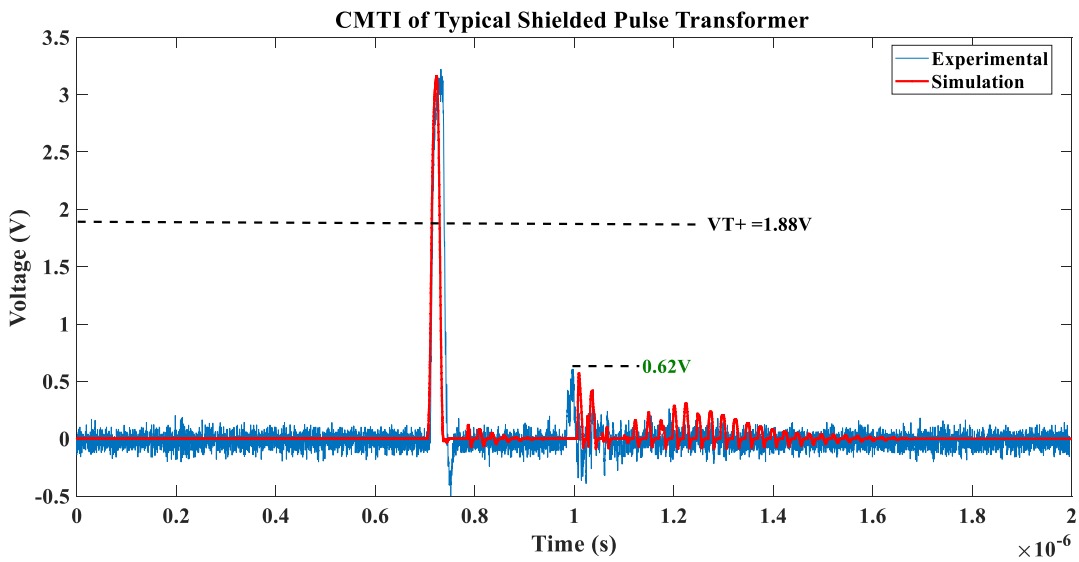
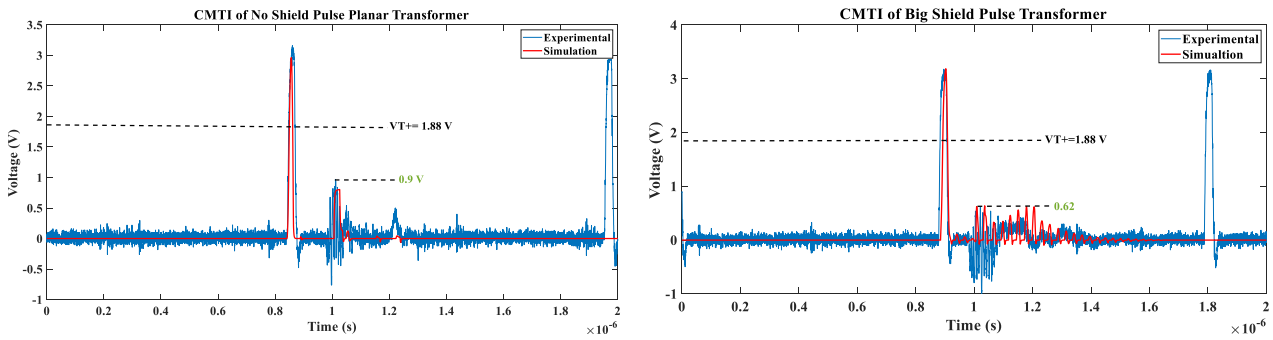


Figure III-28: CMTI test of typical shielded pulse planar transformer

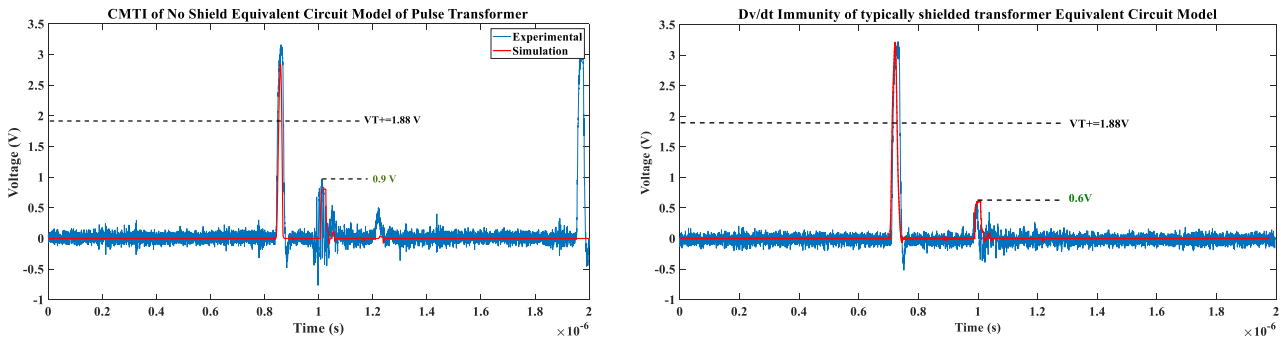
Similarly, the compatible experimental analysis of the no shield and large shield pulse planar transformers (figure III-16) were attained as revealed in figure III-29. The comparison of the no shield and shielded designs affirms the relevance of grounded electrostatic screen insertion on the enhancement of the transformer's immunity to EMI. This is justified by obtaining 0.9V CMTN for the no shield design and 0.6 V for the typical and big shield designs. This also indicates that the big shield arrangement which is wider than the winding periphery does not pose a major change or effect on the transformer's immunity. Furthermore, the results of the equivalent circuit model of each

transformer were also compared to the experimental results attained and the consenting outcomes are illustrated in figure III-30.

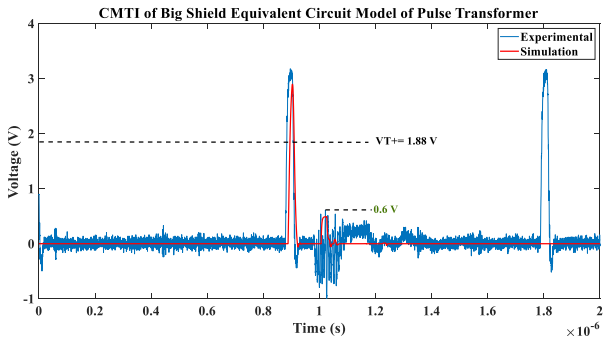


(a) (b)

Figure III-29: CMTI test of pulse transformers (a) No shield; (b) Large shield



(a) (b)



(c)

Figure III-30: Equivalent circuit model CMTI test of pulse transformers (a) No shield; (b) Typical shield; (c) Big shield

E. CONCLUSIONS

To accomplish upgraded power converter designs, researchers are always faced with challenges and obstacles as optimization is invariably valuable. The favourable rapid switching speed attainment by the utilization of WBG technology, leads to the occurrence of critical dispersed CM currents in gate driver cards. This primarily causes accurate awareness to be placed on pulse transformers in gate driver cards as they are responsible to invoke semiconductor switching orders, where a faulty parasitic turn on might instigate a short circuit occurrence.

This chapter revealed an original simulation method that was acquired to quantify the parasitic parameters of the pulse planar transformers integrated in a gate driver. The utilization of Altium Designer for modelling, and associated Ansys software tools for analysing and assessing the design were the foundation of this realization. Following the completion of a spectral analysis of the pulse signal applied, a sufficient frequency span was identified to simulate the evaluated transformer in Ansys Q3D Extractor, where the RLGC parameters were quantified, enabling the construction of equivalent circuit models. Moreover, the corresponding models were subjected to a high dv/dt, mimicking a switching transition, to examine the transformer's CMTI. Allied simulated and experimental results for all transformers; no shield, typical and big shield, namely 0.6 V of CMT parasitic voltage for the typical shielded transformer, demonstrates the authenticity of the simulation technique and EMC standard preservation. Therefore, the tools used which prompted validated results will permit the enhancement and examination of a pulse transformer design for a high voltage application and will found a sincere basis to perform further testing and amelioration of the modelled designs.

CHAPTER IV: SHIELDING STRUCTURE DESIGN FOR MULTI-LEVEL GATE DRIVER OF SIC MOSFETS

The realization and authentication of the applied simulation process presented in chapter 3, utilized to analyze the pulse planar transformer integrated in a gate driver card intended to operate 1.2 kV SiC MOSFETs, admits the feasibility of enhancement and renovation of the latter.

This chapter will present an ameliorated pulse planar transformer design, intended to be integrated in an innovative 3.3 kV SiC MOSFET gate driver card which will complement the dissertation study conducted by Antoine Laspeyres at IETR laboratory. The advanced layer stack-up representation will be illustrated, in addition to distinctive shielding designs which will be tested to attain further mitigated CMTN results.

Furthermore, the perspectives of this remodeling will reveal the influence of dielectric material election on the parasitic capacitance of the pulse transformer windings and consequently on the noise voltage level attained upon the application of a high dv/dt between the transformer's primary and secondary disparate grounds.

A. GATE DRIVERS FOR SIC MOSFETS

Remarkable gate driver techniques that are applied to Si IGBTs and MOSFETs can be achieved for SiC MOSFETs, considering differences related to parasitic elements, power supplies, higher frequency and speed transitions, voltage threshold, Miller stage and transconductance. Thus, many practices already applied to Si-based gate drivers have been conducted by SiC MOSFET applications, in addition to implementing new solutions [1].

Active gate drivers for SiC MOSFETs can be classified into five alternative circuits which are: open-loop, closed-loop, status feedback, overvoltage protection and crosstalk protection technique as illustrated in figure IV-1. Moreover, the conveniences and shortcomings of these classifications are presented in table IV-1 thereafter. Despite the establishment of various gate driver circuits, alternative challenges exist when developing the entire system. An efficiently executed gate driver comprises all of the described conceptions for a reliable operation.

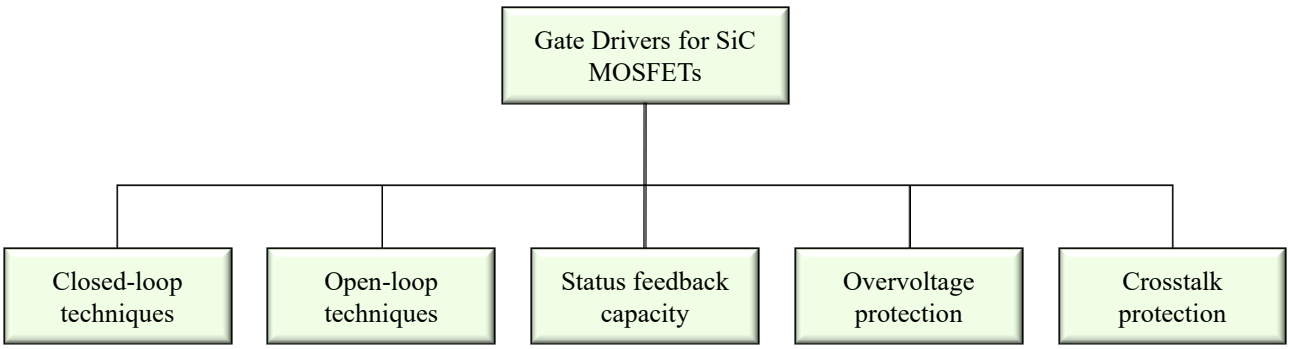


Figure IV-1:Categorization of gate driver circuits for SiC MOSFET devices

Table IV-1: Overview on active gate driver conceptions

Gate Driver Conception	Benefits	Shortcomings
Open loop	• Elementary • Easy to establish	• Inconsiderate of load variation and temperature • Fixed load profile
Closed loop	• Capable to mitigate and eliminate overshoot occurrences • Consider load and temperature variation	• Complex • Explicit applications • Complicated to program
Status feedback	• Flexible • Lessen and remove oscillations and overshoots • Efficient	• Complicated • Load should be acknowledged
Overvoltage and overcurrent protection	• Short-circuit protection • Increase durability	• Sophisticated • Requires additional circuits
Crosstalk protection	• Adequate to control crosstalk in two legs	• Complicated • Expensive

A.1 Commercial SiC MOSFET Gate Drivers

Alternative commercialized SiC MOSFET gate driver circuits can be found in the market, aiming to improve power semiconductor performance and the efficiency of the complete power converter system. Table IV-2 below identifies the entangled manufacturers in this field in addition to highlighting the resemblance and characteristics of the available models.

Table IV-2: Commercialized SiC MOSFET gate driver circuits

Manufacturer	Model	Characteristics	Benefits
Texas Instrument	UCC21710-Q1	• Single channel SiC/IGBT isolated gate driver • Modest propagation delay • Up to 1700 V • Rapid overcurrent and short circuit protection	• Low cost • Galvanic isolation • Easily manufactured
Texas Instrument	UCC21530	• Dual channel • Separate source and sink outputs • Application: 600 V/ 650 V/ 1200 V	• Galvanic isolation • High temperature toleration • Rapid • Enhanced protection modes

Infineon	1EDCxxI12AH 1EDCxxH12AH	• Single channel • Application: ≈ 1700 V	• Overcurrent and short circuit detection • Limited propagation delay
ROHM	BM61M41RFV-C	• Single channel isolated gate driver	• Overcurrent and short circuit detection • Limited propagation delay
Silicon Labs	Si823x	• Two completely isolated drivers in one package • Application: ≈ 1700 V •	• Galvanic isolation • Overcurrent and short circuit detection • Inexpensive • Easy to manufacture
AgileSwitch	EDEM3	• Single channel isolated gate driver • Up to 8MHz switching frequency	• High electromagnetic immunity • Overlap protection and programmable dead time
Microsemi	MSCSICMDD MSCSICSP3	• Adjustable -5 V to +20 V output gate driver • Galvanic isolation of more than 2000 V on both gate drivers • Capable of 6 W and 8W of gate driver power per side • Maximum switching frequency greater than 4000 kHz • Peak output current of up to 30 A	• Short circuit protection • Programmable dead time protection • Fault signaling • Under-voltage lockout protection
Cree/Wolfspeed	CDR-001	• Dual channel SiC isolated gate driver • 4000 kHz maximum switching frequency • +/- 100 kV/µs capability	• Galvanic Isolated • Advanced protections • Low Costs • Easy to implement
Cree/Wolfspeed	CGD12HBXMP	• Dual channel SiC isolated gate driver • 4000 kHz maximum switching frequency • +/- 100 kV/µs	• Galvanic Isolated • Advanced protections • Low Costs • Easy to implement
Cree/Wolfspeed	CGD15HB62P1	• Two output channels • Integrated power supply	• Short circuit and undervoltage

protection

As illustrated, despite the diversified gate driver circuits and solutions, the adaptation towards higher switching frequencies and advanced semiconductor devices, is a key factor for continuous improvement of the gate driver cards. Therefore, continuous exploration and progress in this field is a fundamental objective to attain highly efficient converters.

A.2 Multi-Level Active Gate Driver Topology for SiC MOSFETs

Active gate drivers (AGD) regulate a power device's switching waveforms during the switching transient by forming the gate voltage signal, in correlation to conventional gate drivers that apply a voltage step-function to the gate using a fixed resistance [2]. Active gate driving has been established with all type of MOS-gated Si devices, with the aspiration of controlling di/dt and dv/dt [3], by ultimately repelling EMI disturbances [4], [5]. Moreover, with the transition to WBG power devices, rapid and robust active gate drivers are necessitated. This is because, high switching speed attainments, cause large dv/dt slew rates that may cause high frequency noise through coupling with the heat sink or the gate driver galvanic isolation barrier components. It might also interact with the device's Miller capacitance, induce false turn-on, cross-talk noise and thereupon a shoot-through event [6]. Commonly, the most compelling method to retain EMI disturbance of SiC power devices, is to optimize the layout arrangement of the utilized PCB in a way to reduce or eliminate parasitic, mainly from power, isolation and gate loops [7]. Considering high voltage, EMI immunity is a prevailing concern over the switching speed and switching losses [8]. As a result of the above-mentioned problematics, third generation high-speed multi-level AGDs are being investigated. For example, multi-level turn-off approach has been proposed to control switching transients. One of the applications of the latter is driving high voltage SiC MOSFETs such as 10 kV SiC MOSFETs [9]. Some research examinations have proclaimed that the dv/dt of 10 kV SiC MOSFETs can attain greater than 140 kV/µs, which is much greater than the dv/dt immunity of most driver ICs. Thus, an effective multi-level AGD can be used to reduce dv/dt.

One of the most imperative features of gate driver circuits is the necessity of robust incorporation of galvanic isolation. Thus, the advancement of gate driver circuits and the tendency to operate the latter at higher voltages and higher switching frequencies necessitates the renovation of all constituents of the gate driver circuit including the galvanic isolation requirement. Thus, the upgrade towards engaging a 3.3 kV SiC MOSFET gate driver application at IETR lab mandated the remodeling of the pulse planar transformer involved, aiming to create a further immune and vigorous component, hence, assuring and reinforcing EMC standards, by achieving a reduced coupling capacitance to further enhance the noise immunity of the proposed 3.3 kV SiC MOSEFT gate driver to high dv/dt.

Since the isolated gate driver is essential to provide tolerable galvanic isolation and high CMTI for MV SiC MOSFET applications, the upcoming section will demonstrate the newly modelled pulse transformer and present the scheme of the latter in accordance to standard requirements. Moreover,

the updated transformer, intended to be integrated in the new upcoming gate driver circuit, will be tested upon incorporating alternative new shielding designs with different architecture, the designs will be simulated to inspect the transformer's susceptibility to an abrupt switching transition of 125 kV/µs to examine the influence of shielding designs on the transformer's immunity. The transformers will be fabricated and experimentally examined to verify the simulations.

B. Renovated Pulse Transformer Scheme

Pulse planar transformers are renowned to drive power components in half bridge configurations aiming to provide robust galvanic isolation between the microcontroller unit connected to the primary side and the power module connected to the secondary side. However, in some applications these transformers can be utilized as a DC supply to drive the power semiconductors. Contemporary gate drivers such as CMT-TIT8244 and CGD1700HB3P-HM3 primarily use a dedicated DC power supply to supply new features such as undervoltage-lockout (UVLO) or short circuit detection. Hence, in the mentioned applications, these transformers do not require DC supply and therefore, reduce the risk of magnetic saturation. The characteristics of planar transformers of acquiring a small footprint and remarkable reliability is mainly due to the isolation properties of integrating potent dielectric material such as FR4 epoxy.

The renovated design of the pulse transformer was mainly in the layer stack-up creation; however, the integration of the shielding layers was persistent due to the importance of their integration on EMC perseverance and CM noise mitigation attainments which were verified in chapter two. The inserted shields are grounded to the disparate grounds of the primary and secondary sides aiming to provide a conducted route for the CM currents that might occur due to high dv/dt occurrences. Hence, this will consequently lead to further decrease in the CMTN attained and ensure conformity to EMC standards. This is profitable in planar technology due to ease of integration of the electrostatic screens in the defined PCB layers. Figure IV-2 below demonstrates the pulse planar transformer synopsis designed in Altium Designer with the identification of the grounded shielding layers.

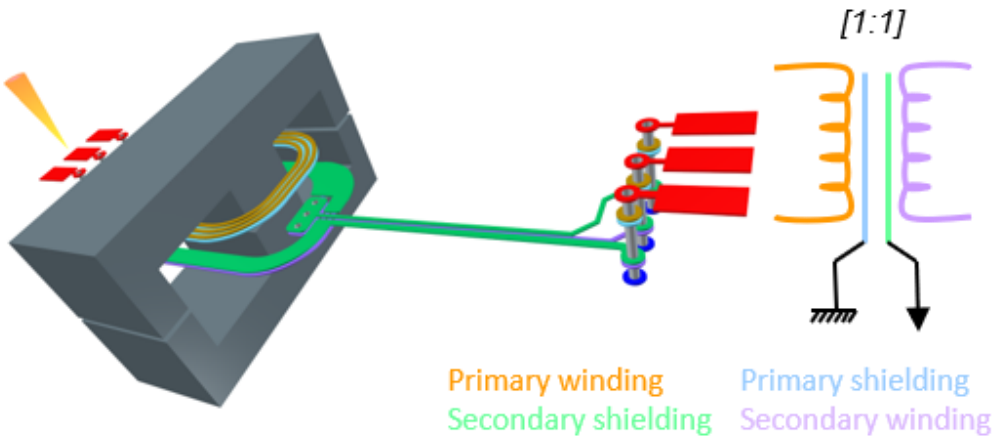


Figure IV-2: Remodeled pulse transformer design for 3.3 kV SiC MOSEFT

B.1 Compliance to Standards

As the examination of the pulse transformer, which is required to provide galvanic isolation between the primary and secondary side, which is accompanied to 3.3 kV SiC MOSFETs, people welfare shall be highly regarded as the potential can rise from 0 V to 2.5 kV being the maximum power component potential in this study. Therefore, the pulse transformer must adhere to electrical isolation standards. Three criterion which were previously addressed in chapter two, must be respected, clearance, creepage and solid isolation. As a recapitulation of the pre-identified norms, clearance is the shortest distance through air between two conductors, creepage is the shortest distance between two conductors along the PCB's insulation material. Ultimately, solid isolation considers the direct path between conductors, where the peak voltage of the isolator used, in this case FR4 epoxy, must endure to ensure conductors will not arc. The principles toward consenting to electric isolation standard requirement is illustrated in figure IV-3.

As previously mentioned, this pulse planar transformer is intended to drive a 3.3 kV SiC MOSFET power module, with an operating voltage of 2.5 kV. The transformer modelled is literally needed to be used in aeronautical applications. Accordingly, the European standard EN50178 is necessitated and required for this specific application [10] along with a vigorous isolation. Thus, 22.9 mm clearance and 25 mm creepage distances are allowed. Moreover, regarding the solid isolation, the latter must withstand 18.4 kV of impulse voltage. Thus, this justifies the utilization of MCL-E-679F (J) FR4 epoxy as the dielectric material of the pulse transformer as it acquires high dielectric strength of greater than 40 kV/mm. Consequently, this implies to maintain at least 460 µm solid isolation between the distinctive conductive sheets in the PCB.

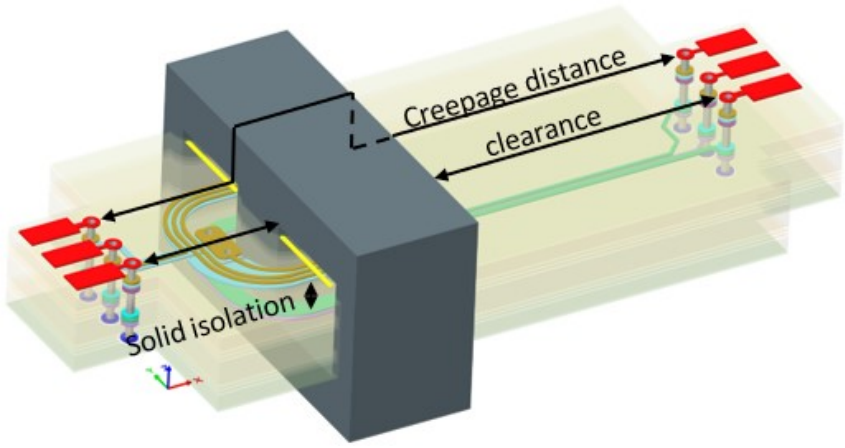


Figure IV-3: Pulse transformer configuration in compliance to electrical isolation standards

B.2 Pulse Transformer Synopsis

B.2.1 Magnetic Core Specifications

The pulse planar transformer receives quasi-rectangular pulse signals of 25 ns duration on their primary winding. Thus, if a voltage V is applied to a coil of N turns during a time Δt, a magnetic flux

density ΔB will concentrate. In order to prevent the magnetic core from saturating, the area of the core A must be selected in accordance to (1) [11].

$$V \cdot \Delta t = N \cdot A \cdot \Delta B \tag{1}$$

As a result, when applying 25 ns pulse signals of 15 V amplitude, and intending to substantially downsize the pulse transformer size, the nominal planar core form ferroxcube E14/3.5/5/R core was used of a minimum area of 10.9 mm^2. Targeting core loss reduction, a maximum flux density of ΔB= 50 mT is presumed, hence, resulting with a minimum number of turns of N=0.7.

B.2.2 Winding Number of Turns

The IEEE standardized equivalent circuit model of a pulse transformer is demonstrated in figure IV-4 [12]. In this interpreted model, two phenomena are principally considered, which are the overshoot and the rising time of the quasi-rectangular pulse signal. In reference to Bortis and al. in [13], in order to attain the rising time rapidly, leakage inductance must be insignificant. However, if the transformer's leakage inductance is inadequate, high voltage overshoot is predicted. Moreover, since leakage inductance is proportional to N^2, stabilization must be satisfied to retain rapid rising time while minimizing the probable overshoot occurrence. Alternative designs with N ∈ [1;5] were simulated in Ansys Q3D and the number of turns preferred was N=3.

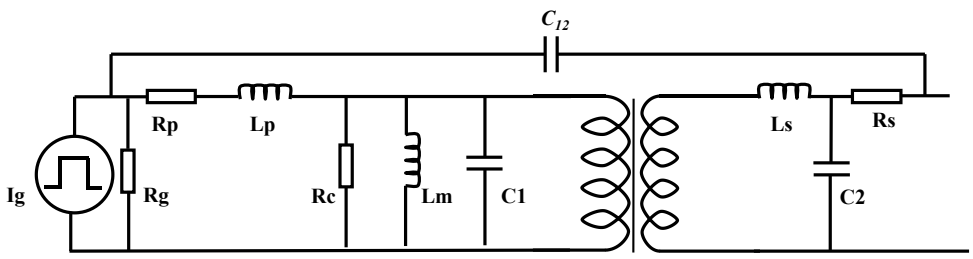


Figure IV-4: IEEE standardized equivalent circuit of pulse transformer

B.2.3 Definite Transformer Scheme

The definitive design of the pulse planar transformer consists of typically shielded three-turn primary and secondary windings, where the shield is placed 210 µm away from the primary side and the secondary side respectively. Therefore, this results with a turns ratio of 1 between the primary and secondary connection. Acknowledging the relevance of solid isolation in pulse planar transformers, in this design a twofold safety factor was considered on the resulting impulse factor. Therefore, the primary and secondary sides are separated by 1mm of FR4 epoxy to comply with standards. Moreover, a minimum distance of 1mm was also applied between the windings and the ferrite core. The pulse planar transformer scheme and design attributes is demonstrated in figure IV-5. This representation reveals an infrequent PCB thickness of 2.8 mm and not 1.6 mm safeguarding the twofold safety factor considered in this model, justifying the utilization of a double EE 3F36 ferrite core.

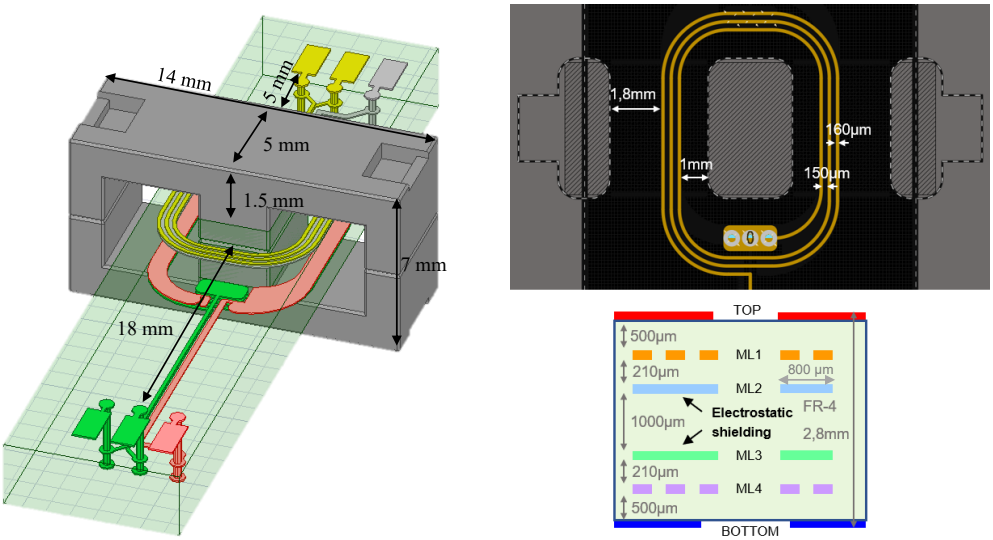


Figure IV-5: Pulse planar transformer synopsis

B.3 Shielding Structure Designs

The integrated shielding design model in the pulse planar transformer was constructed in alternative methods under the same synopsis presented in figure IV-5 above. Distinctive solid and patterned or chopped designs were implemented to test the influence of varying the shielding design in response to the application of a high dv/dt occurrence. The results will be compared to the transformer without integrating a shielding layer. All the implemented designs were simulated and examined to nominate the most efficient model in terms of transformer CMTI. Moreover, this will allow the examination of the influence of inserting a grounded faraday shield on the resultant CMTN. Moreover, the symmetrical application of the shielding structures was also respected for the majority of the implemented models, however, asymmetrical models were also demonstrated to assess the CM noise attained.

Several studies [15], [16], indicate the effectiveness of inserting solid ground shields (SGS) between the transformer windings as a method to mitigate the coupling capacitance between them by providing an excellent capacitive shielding. The studies assure the potency of inserting solid shielding layers on contributing to high dv/dt immunity capabilities. However, they also argue that SGS can achieve high immunity levels at the expense of sacrificing the inductances and voltage gain according to simulation analysis. The studies revealed the necessity of performing patterned or chopped shielding designs to conform to sufficient dv/dt immunity results while not sacrificing the magnetizing inductance of the transformer. Referring to Wu and al., a patterned grounded shield (PGS) was simulated where the results improved the dv/dt immunity by ten times when compared to SGS, without notably sacrificing the inductances. As a result, alternative structures of solid and patterned shielding structures were designed and simulated to check the isolation transformer's susceptibility to a high dv/dt. Moreover, the transformers were fabricated and experimentally tested to an application of 125 kV/µs to assure which design provides the utmost dv/dt immunity whilst considering the magnetizing inductance.

Prior to constructing and modelling the shielding structure, a simple representative design of the model was constructed in Ansys Q3D Extractor respecting the distance between layers and their length. The objective of this design is to use the optimetrics option in Ansys where the user can add parametric variation of all modelled designs. Since the shielding layer is the targeted examination, the optimetric option was applied on the shielding structure. Common mode noise (CMN) propagation in the transformer is as a result of the coupling between the primary and secondary windings. Hence, transformers with alternative shielding structures would result in different CM coupling performances [17]. Knowing that the interwinding capacitance between the primary and secondary windings holds a major influence on the common mode current and the attained CMTN, it was studied with respect to variations of the shielding structure. The optimum width and length of the shielding foil to realize minimum CMN by attaining the lowest coupling capacitance can be investigated using this feature. Therefore, a variation of the shielding width and length were simulated to study the effect on the capacitance between the primary and secondary windings respectively. The results attained are correspondingly demonstrated in figures IV-6 and IV-7 below. As illustrated in both examinations, after a certain width or length the value of the capacitance will become constant and unaffected by the variation of the mentioned variables. At approximately 7 mm width and 10 mm length is the representation of the typical winding structure developed. Therefore, distinctive structure designs were implemented based on the simulated findings intending to likewise study the effect of the shielding width and length with the aim to greatly minimize the coupling capacitance, and hence, the resultant CMTN.

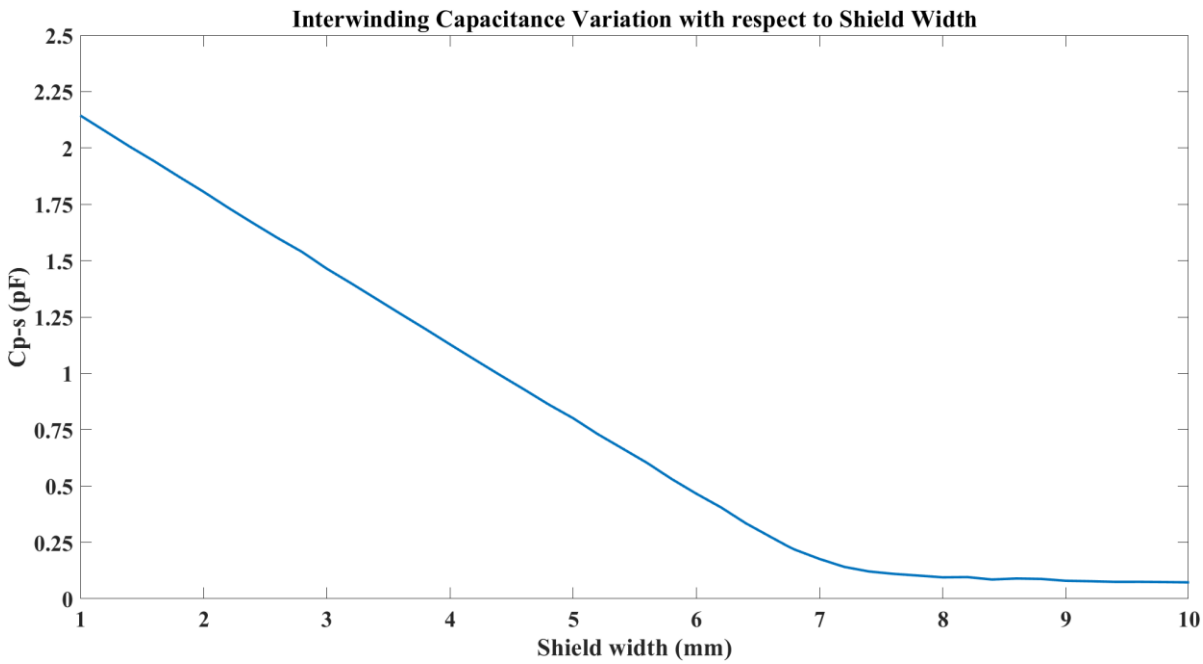


Figure IV-6: Interwinding capacitance variation according to shield width

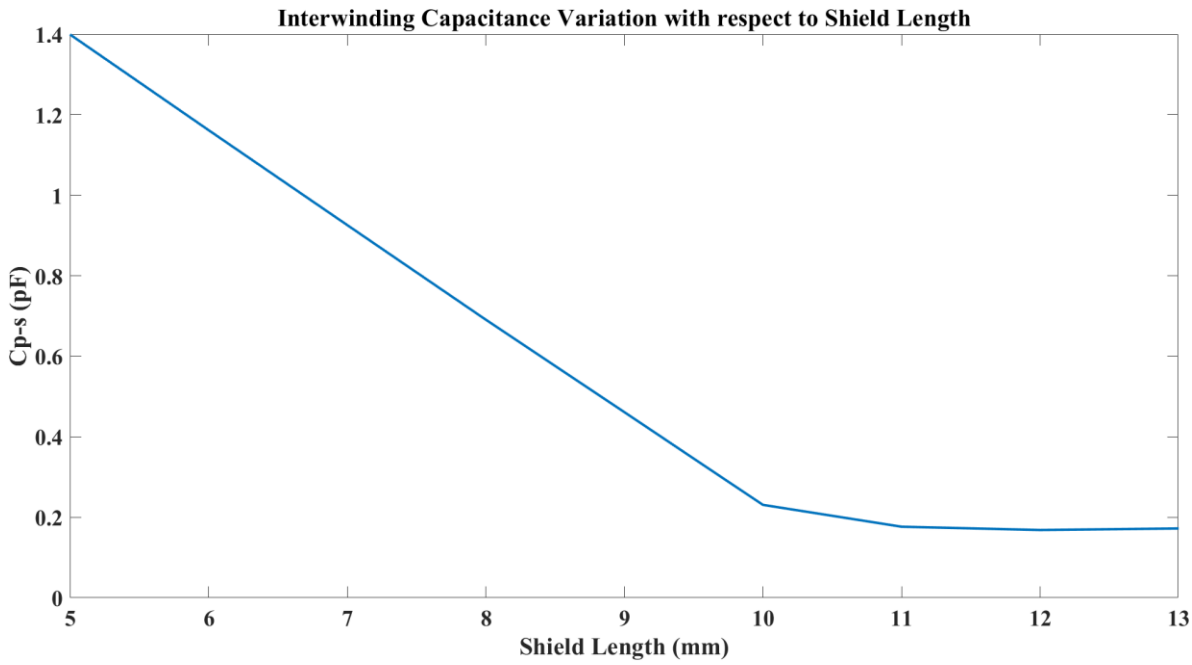


Figure IV-7: Interwinding capacitance variation according to shield length

In addition to the above, a variation of the shielding thickness with a feasible range was implemented to reveal no significant effect on the resultant capacitance presented thereafter in femtofarad between the windings, in figure IV-8.

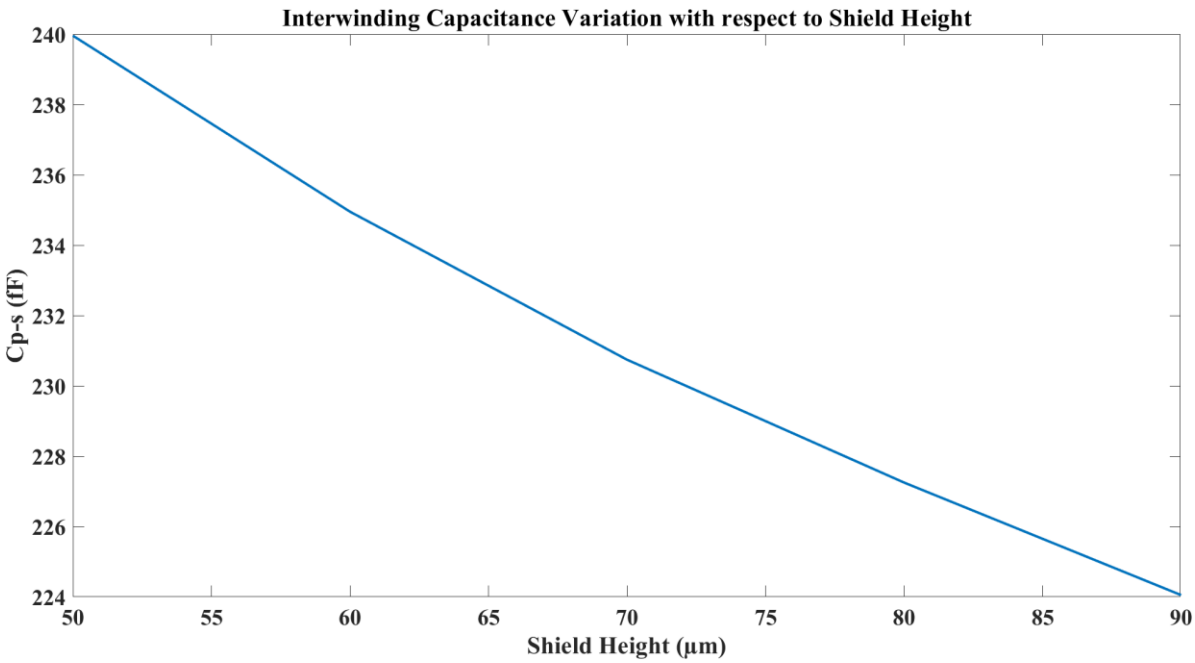


Figure IV-8: Interwinding capacitance variation according to shield height

The renovated pulse planar transformer integrated several structured shielding designs including no shield, fragmented shields and solid shields of different arrangements, as presented in figure IV-9 below. The shielding layers were shaped in Altium Designer before being exported into Ansys Q3D for simulation purposes.

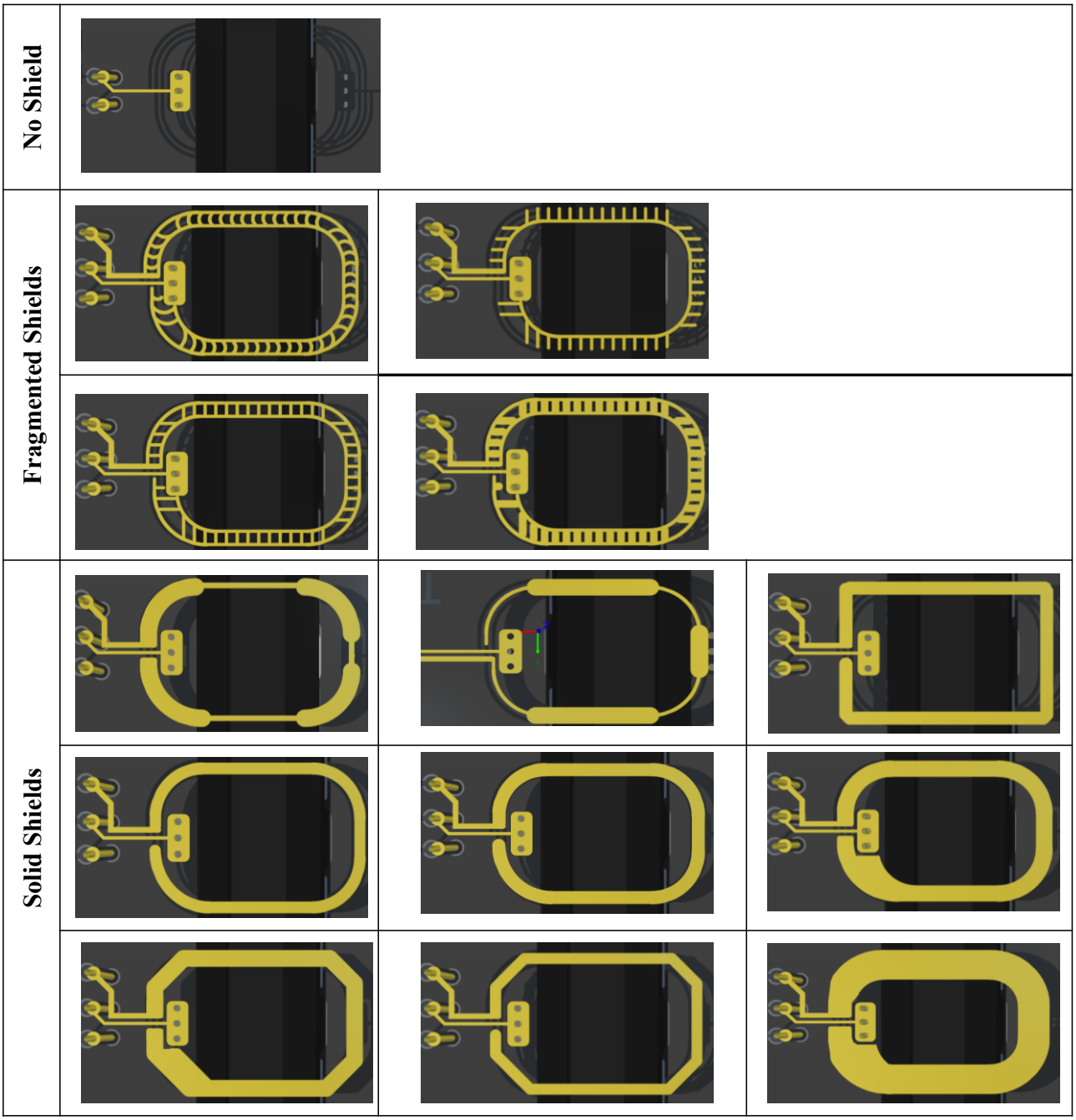


Figure IV-9: No shield, fragmented and solid shielding designs modelled in Altium Designer

The presented shielded transformers were imported into Ansys Q3D Extractor with a main objective of assessing their endurance to high dv/dt application of 125 kV/µs. This was achieved by exporting the necessitated ODB++ files into Ansys SIWAVE. Consequently, after verifying the layer stack-up and material in accordance with the new transformer scheme, the models were exported into Ansys Q3D Extractor for further simulations. Primarily, S parameter analysis results were conducted to authenticate the transformer simulation analysis for all the modelled transformers. This will be presented in the upcoming section by electing four shielded pulse planar transformers. The selection of the transformers was based on the finest, intermediate and inferior CMTV application simulation results that include solid and fragmented shields that were also experimentally verified and will be presented thereafter. The results will be compared to the unshielded transformer.

C. Shielding Effectiveness on Transformers' CMTI

C.1 S Parameter Examination

The same pulse generator presented in chapter 3, of 100 kHz PWM and 25 ns duration signal was also utilized for this application. Therefore, the eligible frequency bandwidth applied is from 100 kHz till 85.7 MHz based on the performed spectral analysis of the pulse signal. Furthermore, the simulation process initiating with Altium Designer and concluding with Ansys Circuit Design is respected and recapitulated as shown in figure IV-10.

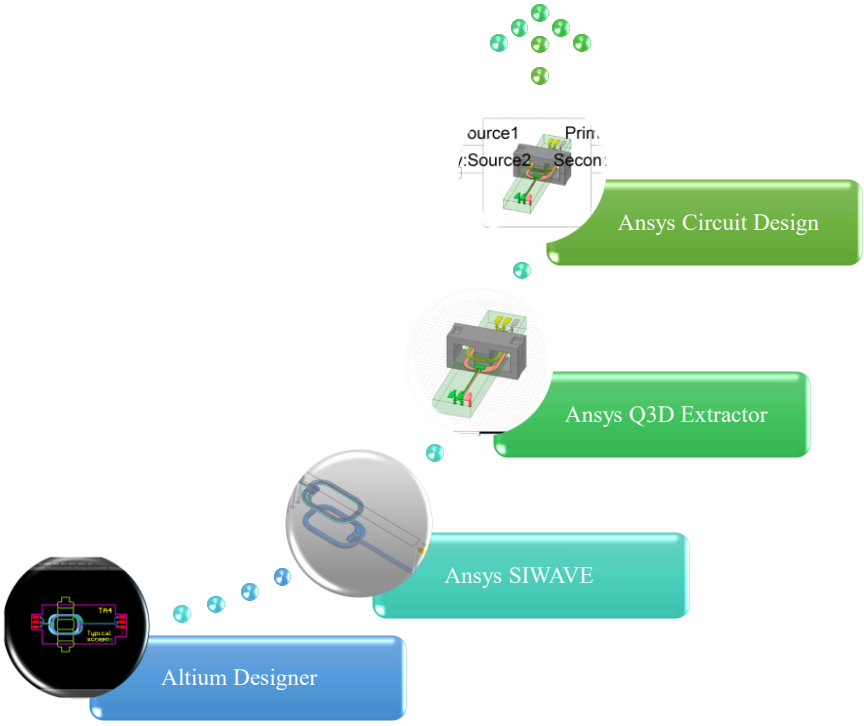


Figure IV-10: Simulation process maneuver recapitulation

After verifying the transformer stack-up in SIWAVE and exporting the latter into Ansys Q3D Extractor, the glued EE core was constructed in accordance to figure IV-11 [18]. Moreover, the analysis setup was identified after assigning the transformer's nets and related excitations. In addition, an effective frequency sweep was defined to simulate for all the RLGC parameters.

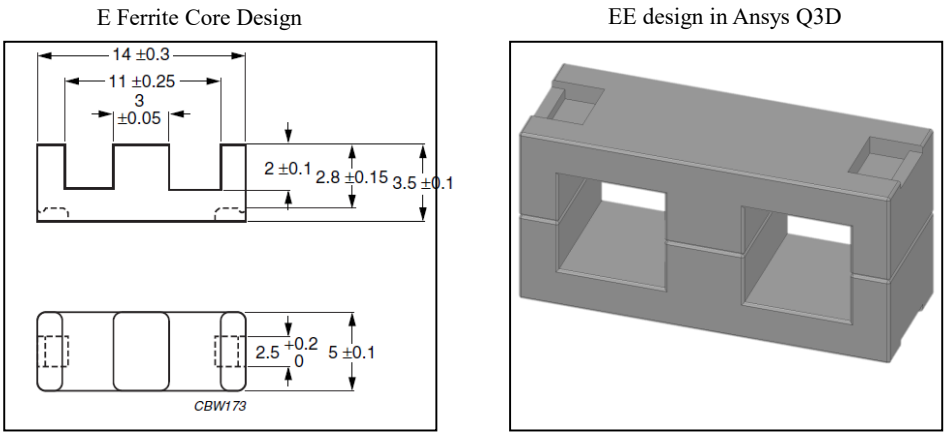


Figure IV-11: EE ferrite core design

The analyzed Q3D model is dynamically linked with Ansys Circuit Design, a demonstration is illustrated in figure IV-12 representing the typical shielded pulse transformer, however a similar analysis was conducted on all transformers. Knowing that some of the results were very close, it is noted that this chapter will demonstrate the most leading, fair and poorest results attained in terms of CMTI of the transformers, they are namely the typical shield (figure IV-12), thin-typical shield, chopped shield and asymmetrical shield are presented in figure IV-13. The results will be compared to the unshielded transformer.

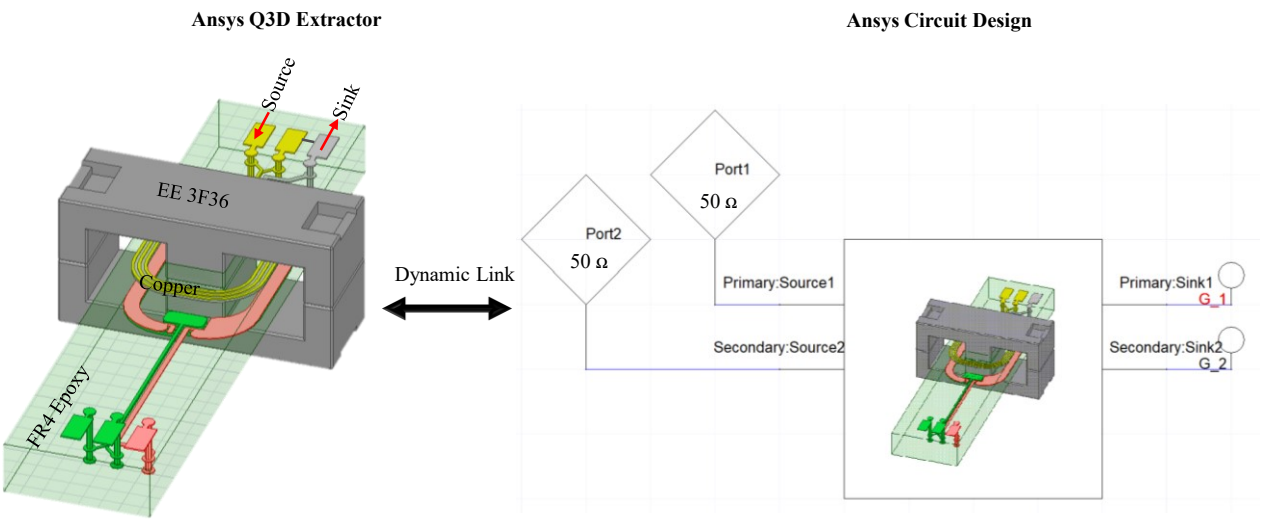


Figure IV-12: S parameter simulation analysis of typical shielded transformer

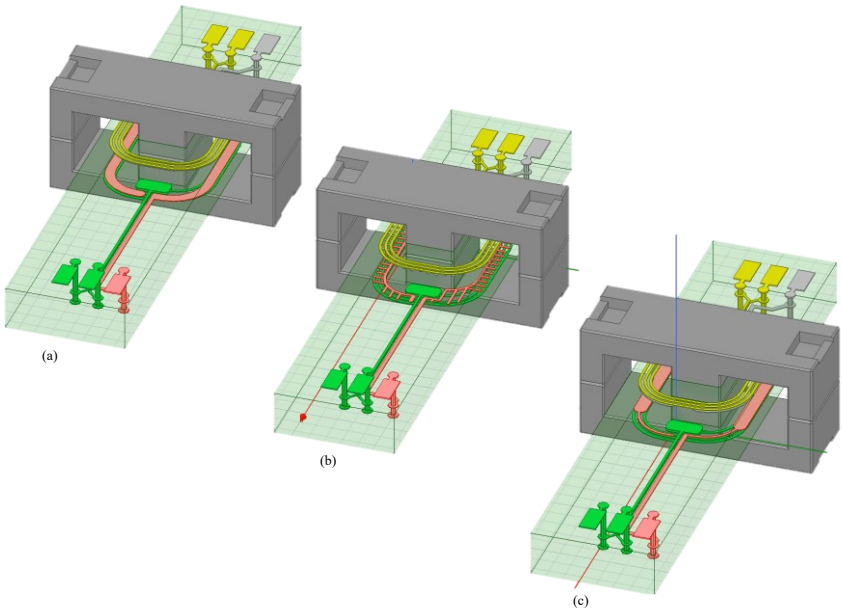


Figure IV-13: Renovated shielding structures (a) thin typical; (b) chopped; (c) asymmetrical

C.1.1 S Parameter Authentication

A fifty-ohm impedance VNA was utilized to examine the transformers' S parameters, to verify the simulated results. The device is calibrated on the applied frequency bandwidth and the power is set to 0 dBm. Consequently, the transformer is connected, and the S parameter results are traced as revealed in figure IV-14.

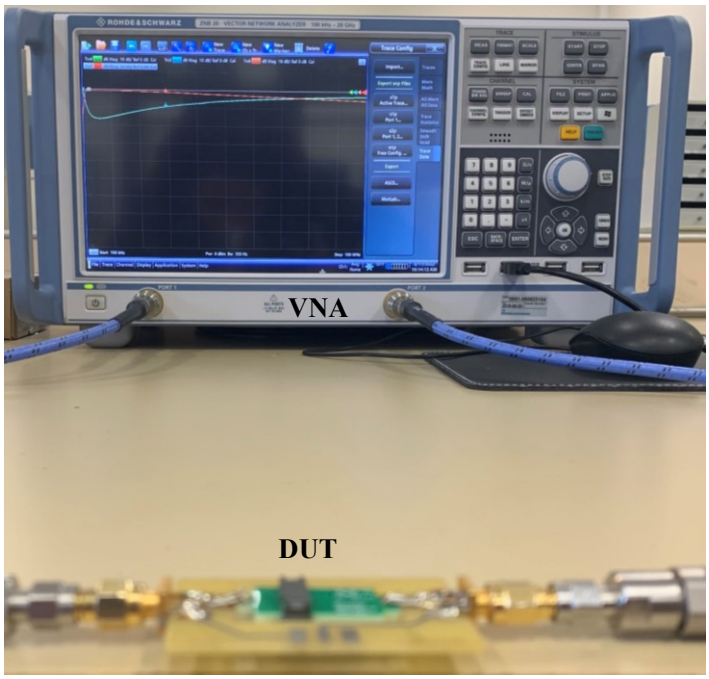


Figure IV-14: Experimental S parameter analysis

Figure IV-15 presents the satisfactory simulation versus experimental results of four distinctive shielded transformers which are termed as asymmetrical, chopped, thin typical, typical shielding. As

mentioned earlier, these transformers were appointed to be demonstrated due to the proximity of results attained which will be further presented in the upcoming section.

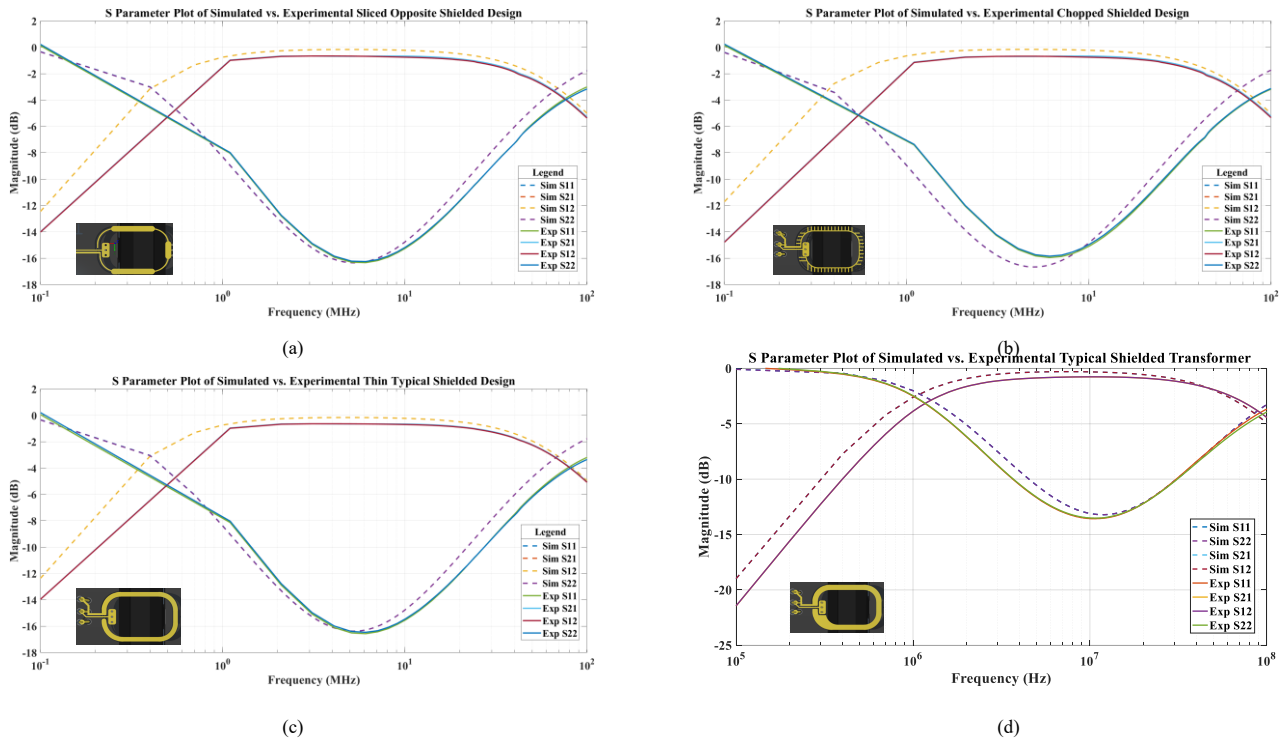


Figure IV-15: S parameter Plot for shielded transformers: (a)asymmetrical; (b) chopped; (c) thin typical; (d) typical

C.2 Ansys Q3D Field Plot Generation

A satisfactory analysis of the pulse transformers in Ansys Q3D Extractor allows the demonstration of the electrostatic fields of the pulse transformer. The electric charge surface density termed as the CG fields and the magnetic field strength named as the AC RL fields can be demonstrated on any identified geometry of the transformer.

The magnetic field strength of the ferrite core is presented in figure IV-16 in correspondence to the magnitude of the field and the surface vectors. It is noted that the size of the arrows was enlarged intentionally for observational purposes and hence appear exiting the ferrite core.

The electric charge density of the conductive layers of the unshielded and typically shielded transformers analyzed at a frequency of 100 kHz are demonstrated in figure IV-17 below. As the field sources were assigned on the primary windings of both transformers, the illustration reveals the effectiveness of the shield in blocking or resisting the charge density from penetrating and reaching the secondary side.

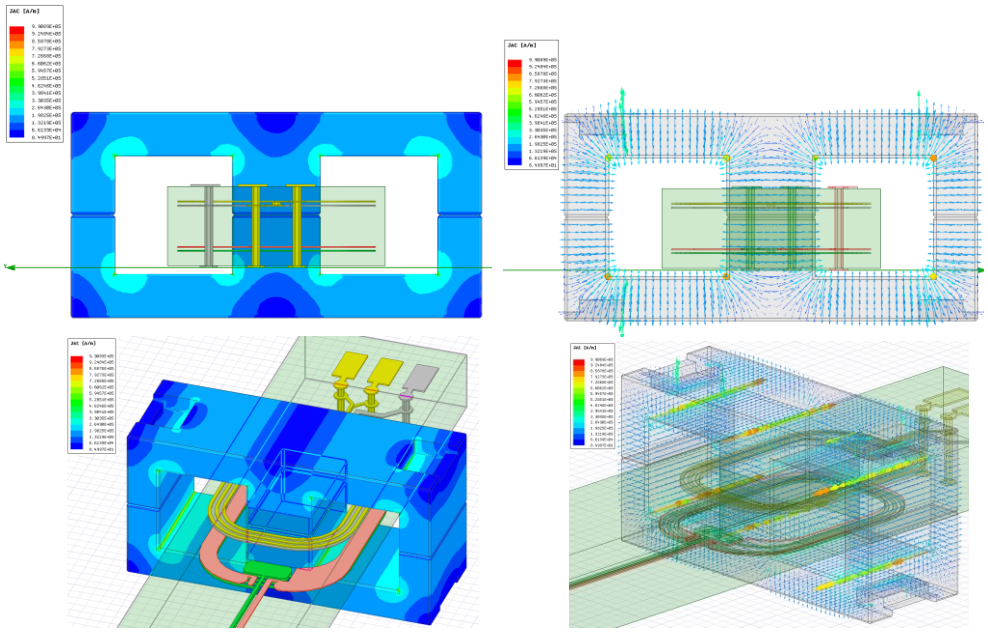
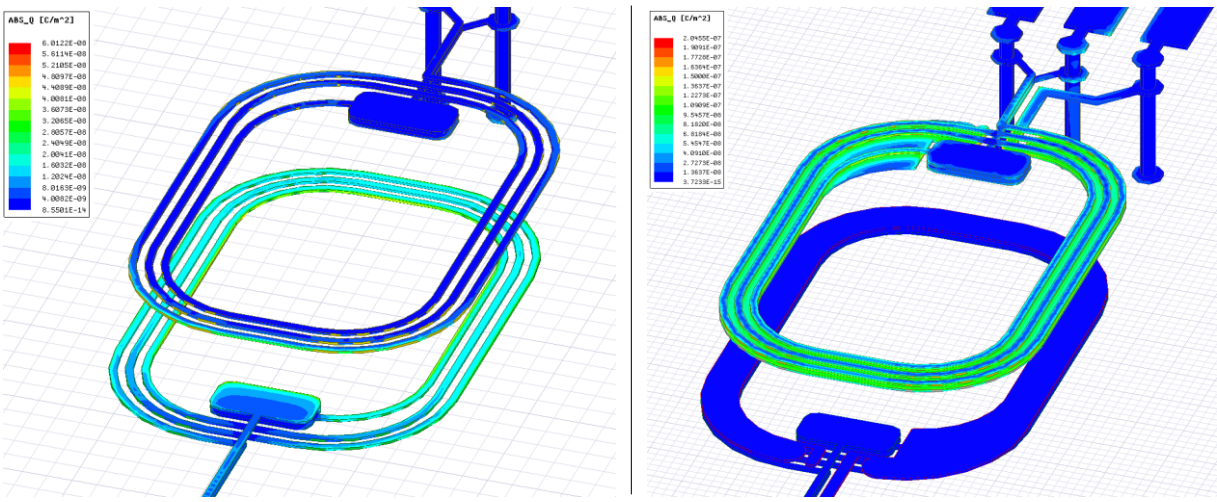


Figure IV-16: Magnetic field strength (magnitude and vector) demonstrated on the EE core of the typically shielded pulse transformer



(a) (b)

Figure IV-17: Electric charge density at 100 kHz for pulse transformer (a) Unshielded; (b) Typically shielded

C.3 Shield Efficacy on CMTI – Subcircuit Analysis

The efficiency of the inserted shielding structures was tested under an application of a high dv/dt to inspect the transformer's performance. Moreover, an assessment of the influence of solid and fragmented shielding structures on the outcome noise level was conducted. Therefore, after the satisfactory simulation analysis in Ansys Q3D, the transformers were dynamically linked to Ansys Circuit Design to implement the CMTI test for each transformer. It is noted that no changes were implemented on the pulse transformer electronic circuitry and the assigned pulse generator.

The sub-circuit of four-ports representing the excitation assignments of the transformer presented in Ansys Circuit, where all the electrical components were connected to construct the pulse

transformer's electronic circuitry, is presented in figure IV-18. This was conducted to examine the integrity of the shielding structure on the transformer's endurance to high dv/dt application of 125 kV/µs. Furthermore, since this transformer is intended to drive 3.3 kV SiC MOSFETs, it is imperative that the transformer develops minimal CMTN results. The figure below represents a typical experimental framework that will be consequently verified. The 25 ns, 15 V amplitude pulse generator is presented along with the applied dv/dt. The typical shielded transformer is depicted; however, the application was conducted on all the remaining transformers.

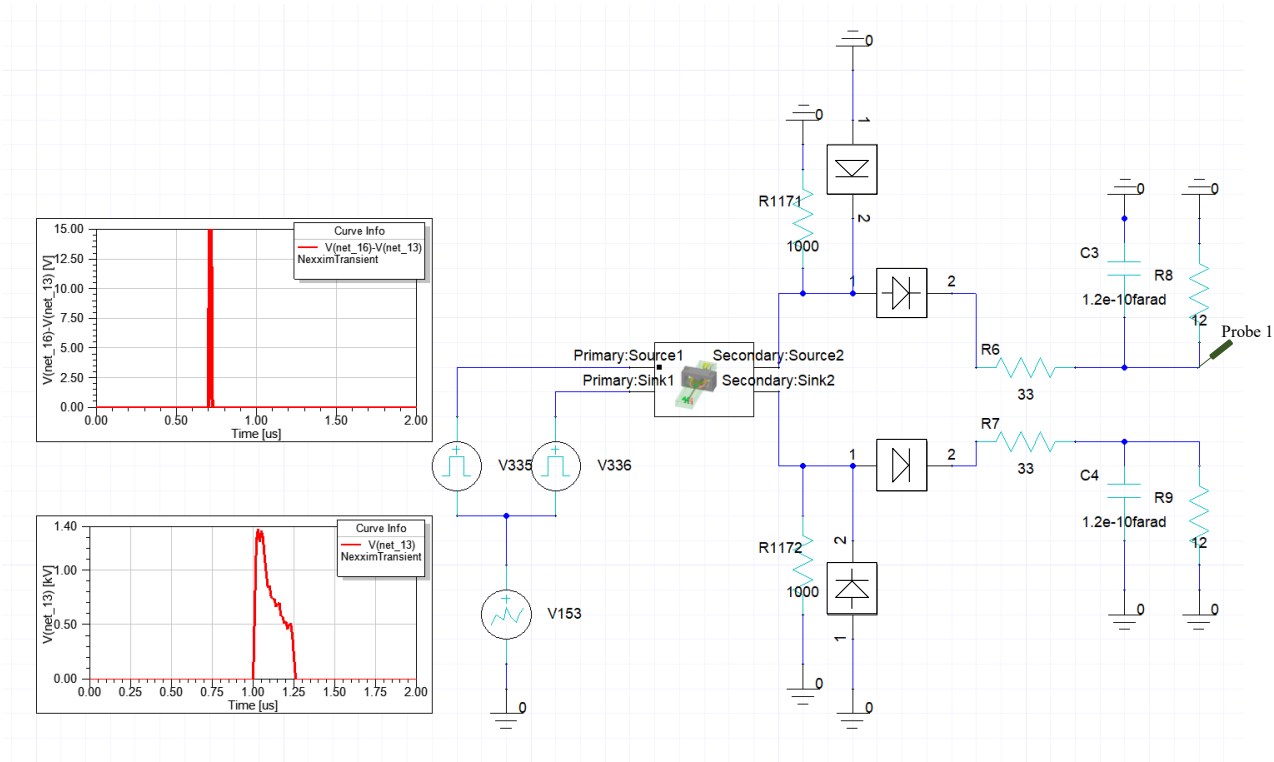


Figure IV-18: dv/dt immunity test on transformers' subcircuit in Ansys Circuit Design

Similar to an applied experimental setup, the transient analysis setup was added to simulate the design, ranging between 0 and 2000 ns. After transmitting a pulse signal, the arduous CMTV was applied at t=1 µs. The resultant CMTN inspected at probe 1 for all the transformers is summarized in table IV-3. The unshielded transformer resulted with 0.7 V noise. The results attained clearly highlight a considerable effect of the shielding structure design on the transformer's immunity. Peculiar transformers were elected to be experimentally tested to verify the attained results, namely, the best and most unfavorable results and those amidst both; this will be presented in section C.4.

Table IV-3: Simulated dv/dt immunity test results

Shield Structure	Type	CMTN (V)
Typical (800 µm)	Solid	0.4
Typical (600 µm)	Solid	0.46
Chopped (350 µm)	Fragmented	0.41

Rectangle	Solid	0.45
Partial Symmetrical	Solid	0.46
Octagonal (800 µm)	Solid	0.5
Octagonal (600 µm)	Solid	0.54
Chopped (150 µm)	Fragmented	0.6
Arc	Fragmented	0.9
Partial Asymmetrical	Solid	1.16

C.4 CM Equivalent Circuit Model

The representation of an equivalent circuit model of the pulse planar transformers was conducted by following a similar approach previously demonstrated in chapter 3 section D.2. The transformer is constructed at a specific appointed frequency after extracting the RLGC parameters over the entire desired frequency band. The typically shielded transformer will be demonstrated in this section, however a similar analysis was conducted on the remaining transformers.

In Ansys Q3D a frequency sweep ranging from 100 kHz till 85 MHz was assigned to quantify the RLGC parameters. Furthermore, after a satisfactory analysis the reduce matrix feature is used to evaluate the transformer's resistance and inductance and capacitance values. Therefore, this will allow the construction of the circuit model based on the generic model previously presented in chapter 3, figure III-22. The susceptibility of the equivalent circuit model to a high dv/dt application will be tested.

The quantified RLC parameters depicted in figure IV-19 below, reveal consistency along the frequency band, with an insignificant variation of R_P and R_S due to skin effect phenomenon. The precise measurements are illustrated in table IV-4, where a specific frequency will be appointed to construct an equivalent circuit model of the pulse transformer. The presented analysis represents the typical shielded planar transformer; however, a similar analysis was performed on the remaining transformers.

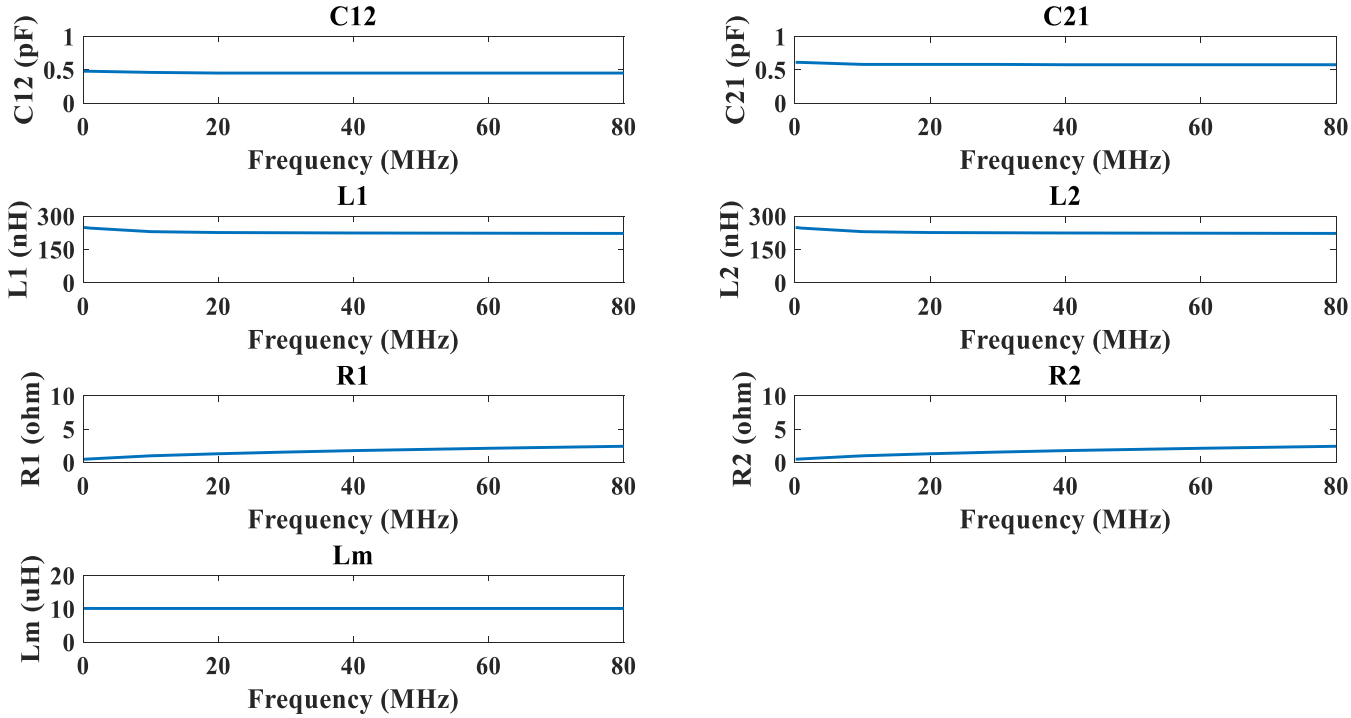


Figure IV-19: Steadiness of RLC extracted parameters over frequency bandwidth

Table IV-4: Ansys Q3D RLC parameters of typical shielded transformer

Frequency (MHz)	C_{mc1} (pF)	C_{mc2} (pF)	R_P (Ω)	R_S (Ω)	L_P (nH)	L_S (nH)	L_m (µH)
0.1	0.47	0.61	0.47	0.47	249	249	10.1
1	0.47	0.61	0.52	0.52	246	246	10.1
10	0.46	0.58	0.99	0.99	230	230	10.1
20	0.45	0.58	1.3	1.3	226	226	10.1
30	0.45	0.58	1.55	1.55	225	225	10.1
40	0.45	0.57	1.77	1.77	224	224	10.1
50	0.45	0.57	1.96	1.96	223	223	10.1
60	0.45	0.57	2.12	2.12	223	223	10.1
70	0.45	0.57	2.28	2.28	222	222	10.1
80	0.45	0.57	2.24	2.24	222	222	10.1

The equivalent circuit model of the transformer portrayed in figure IV-20 was constructed at a defined frequency of 50 MHz. The peculiar frequency was selected by conducting two approaches. The first was averaging the value of each parameter over the frequency span. Whereas the second approach was testing the model at two distinctive frequencies which are 10 MHz and 50 MHz. The results of both methods were in concession, allowing the construction of the equivalent circuit at a peculiar frequency.

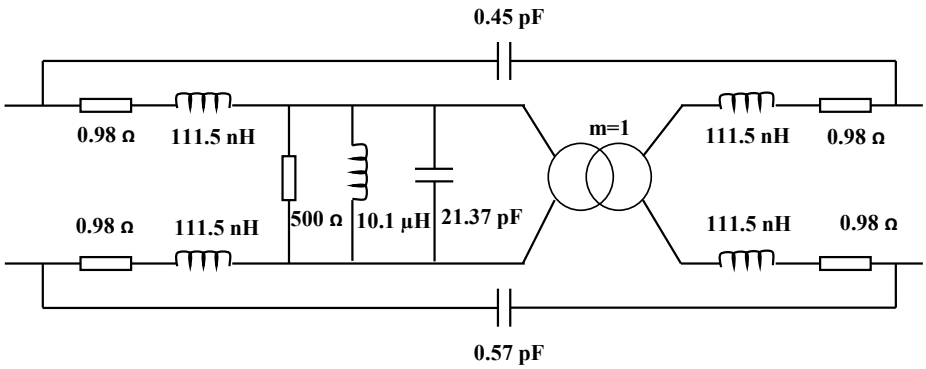
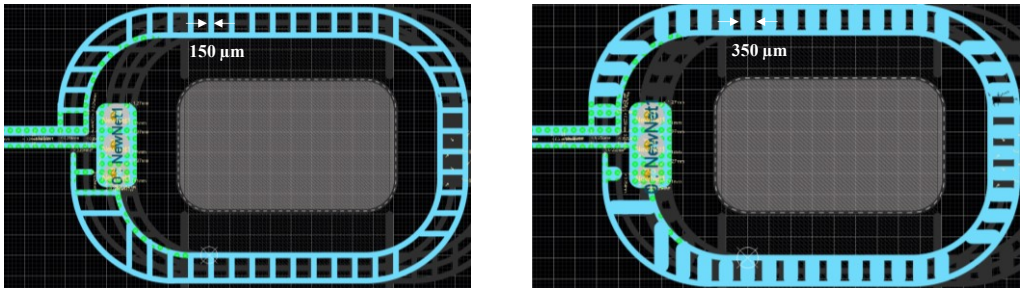


Figure IV-20: Equivalent circuit model of typical shielded transformer at 50 MHz

Table IV-5 below demonstrates the RLC parameters of appointed simulated and analyzed transformers extracted at F=50 MHz. These transformers were selected due to closeness of the CMTN results attained when simulating the dv/dt immunity test. The value in parentheses demonstrates the width of the shielding structure. Typical shielding layers of width 600 µm and 800 µm are of solid type shielding. Furthermore, the fragmented shielding structures were chopped into 150 µm and 350 µm dissections as illustrated in figure IV-21. This was performed to assess the effect of such structure on the RLC parameters, the magnetizing inductance and the transformer's susceptibility. In addition, this can allow the study of the effect of the density of dissections on the performance of the transformer under high dv/dt application. Finally, an asymmetrical design of the shielding was implemented to verify that an asymmetrical shielding design is expected to result in high CMTN. The results of their endurance to 125 kV/µs dv/dt will be presented in the upcoming section.

Table IV-5: Ansys Q3D RLC parameters of assorted shielded transformers

Frequency= 50 MHz							
Shield Structure	C_{mc1} (pF)	C_{mc2} (pF)	R_P (Ω)	R_S (Ω)	L_P (nH)	L_S (nH)	L_m (µH)
No Shield	0.933	0.933	1.51	1.51	232	232	9.8
Typical (600 µm)	0.59	0.7	1.82	1.82	226	226	10.1
Typical (800 µm)	0.5	0.6	1.96	1.96	223	223	10.1
Chopped (350 µm)	0.5	0.7	1.9	1.9	225	225	11.2
Chopped (150 µm)	1.1	0.9	1.72	1.72	230	230	10.9
Arc (150 µm)	1.38	0.84	1.9	1.9	227	227	11
Asymmetrical	1.6	1.6	1.76	1.76	226	226	10



(a) (b)

Figure IV-21: Fragmented shield structure of pulse transformer (a) 150 µm dissections; (b) 350 µm dissections

Lastly, the equivalent circuit model of the Haefely generator present at IETR laboratory, was also modelled as presented in figure IV-22, and applied in Ansys Circuit Design to further authenticate the examinations and attained results.

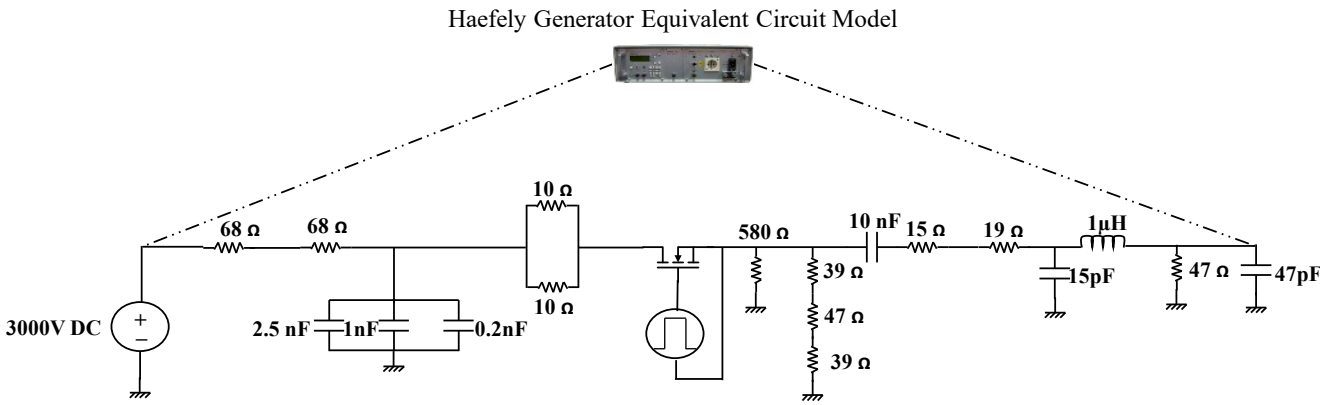


Figure IV-22: Equivalent circuit model of Haefely dv/dt generator

C.5 Experimental Validation

C.5.1 Transformer Susceptibility Experimental Set-Up

The pulse generator is constructed of two NAND gates serving as the receivers of the input signal and its inverted equivalent. This permits the selection of the rising or falling edge of the input impulse. The XNOR gate is utilized to transform the input signal into a transient signal when a change of the signal's state occurs. The transient signal duration is defined by the time response of the RC filter, τ=RC. Consequently, the signals are then transmitted through the pulse transformer. The electronic circuitry representation is depicted in figure IV-23.

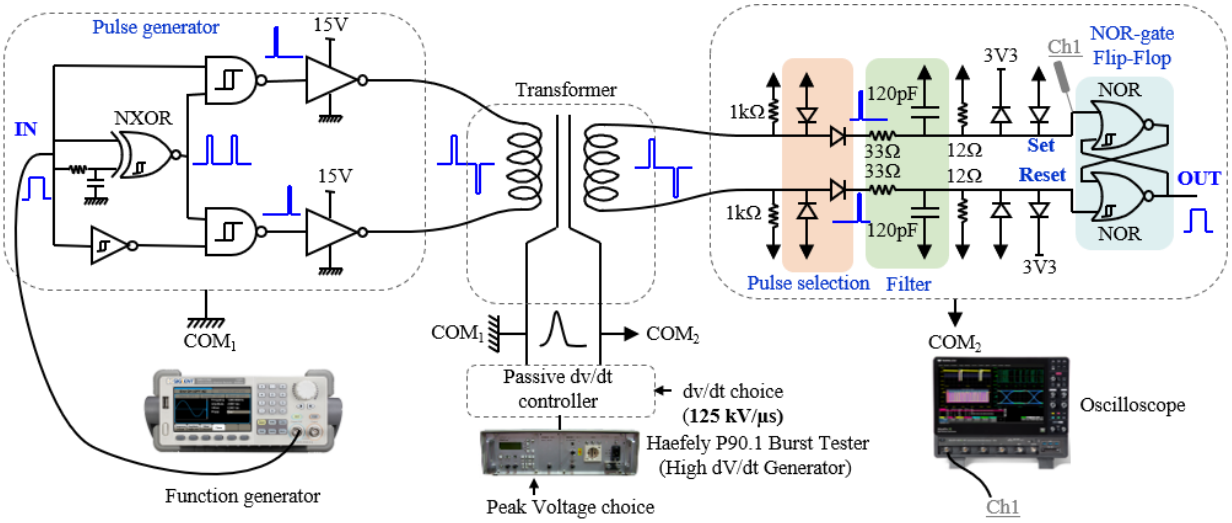


Figure IV-23: Pulse transformer susceptibility test circuitry to an application of 125 kV/µs between its disparate grounds

The simulated transformers were all tested at IETR laboratory in accordance with the circuit presented above. A 100 kHz PWM signal was generated by the function generator and is denoted as the IN signal. The Haefely generator, provoking a dv/dt occurrence, was connected to the transformer's distinctive corresponding primary and secondary grounds. A dv/dt of 125 kV/µs is transmitted in concurrence to a pulse signal transmission. This dv/dt slope was applied to reproduce the power module's superlative theoretical switching speed, amplified by a safety factor of four. Figure IV-24 embodies the establishment of the dv/dt station with the tested pulse transformer.

All the appointed simulated transformers were tested under the described conditions by interchanging the fabricated models of alternative shielding structures. The attained CMTN results measured at the set input of the NOR-gate flip-flop, as displayed in figure IV-23, will be demonstrated in the upcoming section.

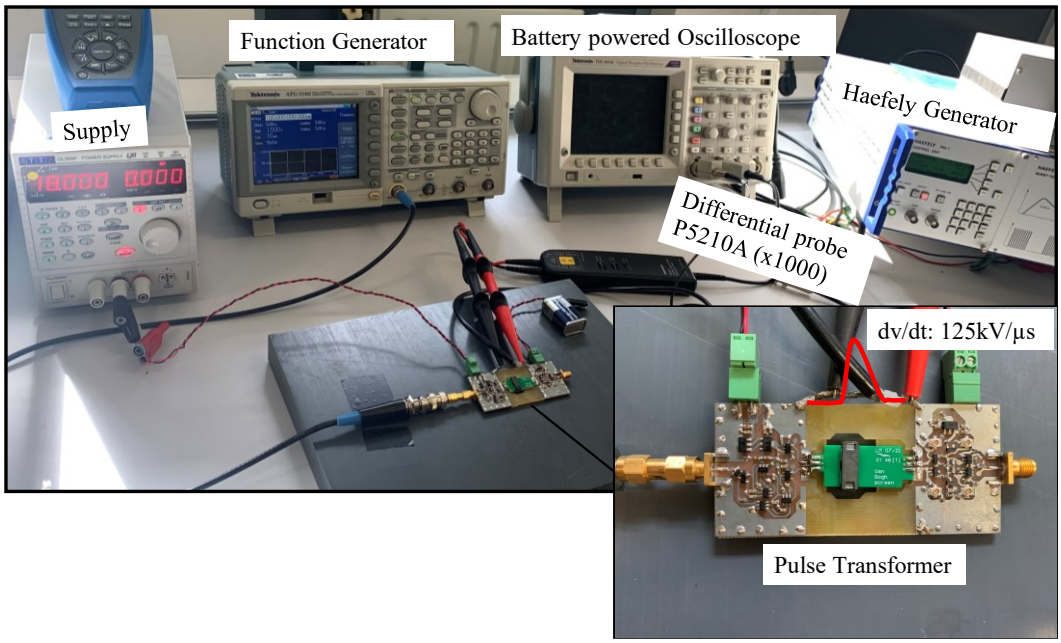


Figure IV-24: Installation of the experimental station to perform dv/dt immunity test of the pulse transformer

C.5.2 Shielded Transformers Susceptibility Test Results

The simulated equivalent circuit model of the transformers and the fabricated experimented model endured corresponding analysis set-ups. The application of a CMT waveform of 125 kV/µs was essential to determine the transformer's level of immunity, as a parasitic turn-on in high power gate drivers can lead to hazardous effects.

The CMTV was generated between the primary and the secondary distinctive grounds at a defined time of t=1µs, where the pulse signal was transmitted at an interval prior to the dv/dt application. The results of the simulated vs. experimental 125 kV/µs dv/dt application is displayed in figure IV-25 below.

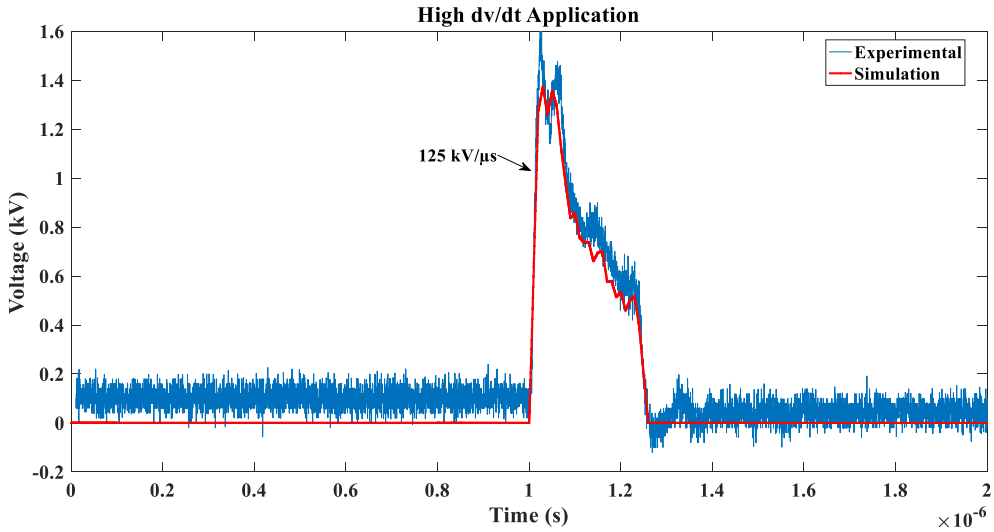


Figure IV-25: Simulated vs. Experimental high dv/dt application

The simulation vs. experimental results of the CMTI of selective solid, fragmented, and asymmetrical transformers is revealed in figure IV-26 below. As revealed, the convenient results show more immunity for the solid shielding designs than the distantly fragmented and asymmetrical models. A partial and asymmetrically shielded model, with an attained noise of approximately 1.2 V is greater by a factor of three than the typically solid shielded design. This justifies the effect of the width of the shielding on the resultant CMTN due to higher coupling capacitance with a partial shielding structure not fully covering the windings. In addition, and most importantly, this verifies the importance of symmetry application in terms of reducing or eliminating the coupling capacitance between windings. Moreover, symmetrically modelled transformers of similar or close widths such as 600 µm and 800 µm attained very close results in terms of immunity due to the consistency of the reduced coupling capacitance.

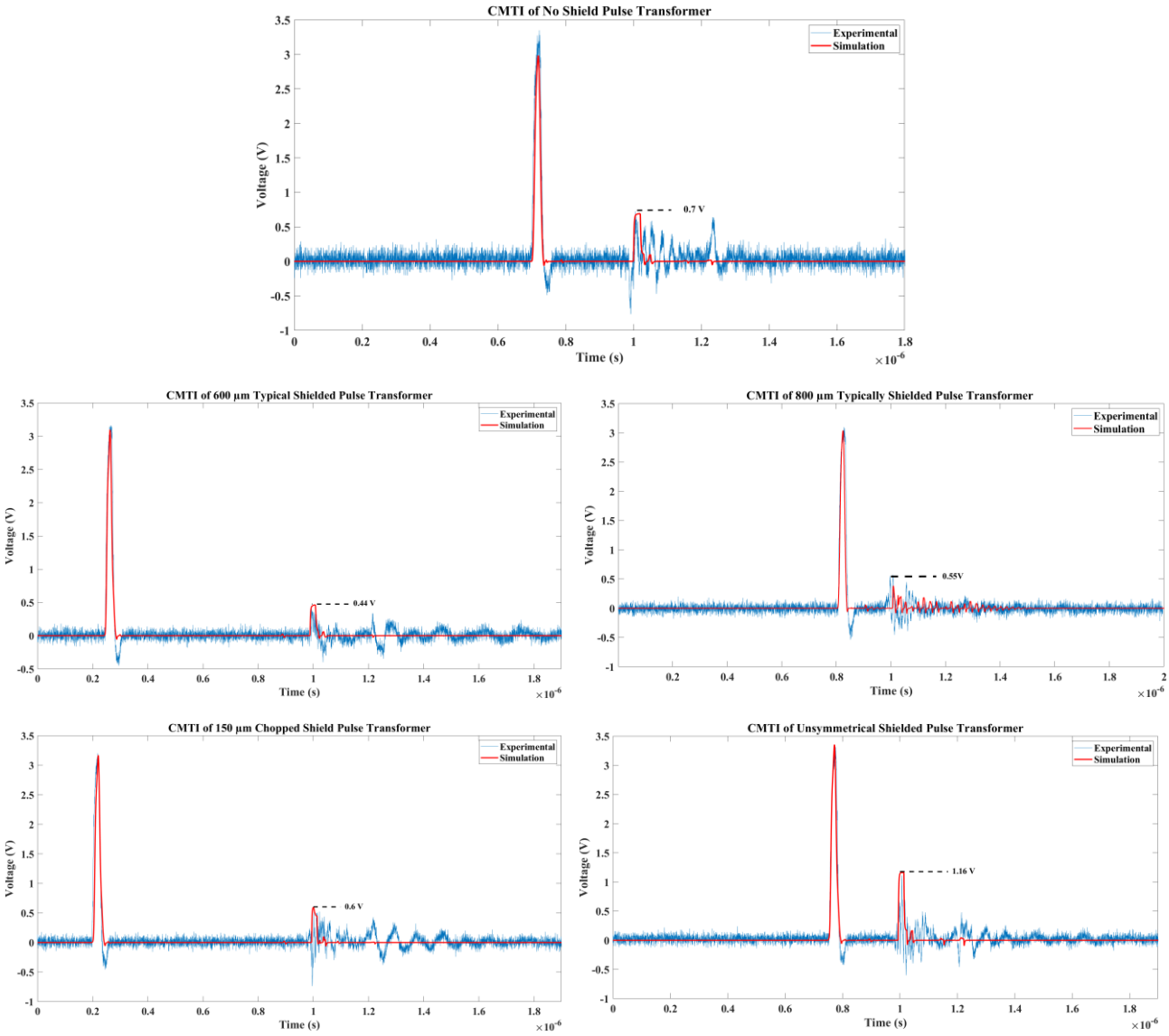


Figure IV-26: Simulation vs. experimental results of CMTI test of unshielded and distinctively shielded pulse transformers

The experimental results confirmed that a properly designed and shielded transformer can intensify a transformer's immunity to a high dv/dt application. However, the structure of the shielding design is very crucial in this matter, since as demonstrated, a poorly structured model can lead to inferior results, which are worse than the unshielded transformer. Primarily it is concluded that the shielding structure should cover the entire winding to suppress the CM currents resulting from parasitic capacitances and applied in a symmetrical. This was justified by the poor immunity of the asymmetrical structure with partial shielding of the windings.

Furthermore, fragmented designs are not always better than the solid designs in terms of dv/dt immunity. The model should be very densely chopped (almost solid) covering the primary and secondary windings to achieve high dv/dt resistivity. Indeed, a 10% greater magnetizing inductance value was achieved for chopped designs, however, the immunity of a densely fragmented structure is greater by 1.5 than a sparsely chopped shielding structure. The finest shielding designs that offer

better immunity are the ones that comprise a combination of high resistance and low capacitance parameters. This was verified with the results attained by the solid shielding designs such as the typical shielding acquiring lower parasitic capacitance in their equivalent model.

Lastly, most of the solid shielded designs demonstrated superior immunity to dv/dt application reaching to ameliorated immunity by a factor of three than the partially asymmetrical model for example, and a factor of two in comparison to the unshielded design.

D. EXPLORATIONS AND PERSPECTIVES

High frequency, planar PCB-transformers have been prominently examined and investigated in literature in terms of winding structure and placement aiming to reduce losses and/or parasitic capacitance [19], [20]. Most recent investigations targeted the minimization of the coupling capacitance within the insulation barrier in the transformer. This is because the coupling capacitor defines a path for noise current, or CM current, that is generated concurrently with high dv/dt switching occurrences of power modules. The fallout of minimizing the coupling capacitance is the reduction of the circulating current and consequently EMI disturbances.

This thesis proposed and investigated the relevant impact of adding an adequately structured and grounded electrostatic screen on the curtail of the parasitic capacitance of a planar PCB-transformer. However, several additional factors also impact the attainment of this minimization which will be explored in this section while considering the variables that can be adjusted while respecting the dimensions of the PCB planar transformer.

D.1 Dielectric Material Significance

Hosting conductive layers within a dielectric material-based assembly is essential to sustain required distance between windings and safeguard electric breakdown limits while considering the operative voltage level. Thus, the election of the proper dielectric material while considering its dielectric constant acts a decisive factor on affecting the value of the self and interwinding capacitance of the transformer. As the main objective of this dissertation is to minimize the coupling capacitance, and hence construct a more immune transformer to a high dv/dt application, further simulation analysis on convenient dielectric material was conducted. In a planar transformer, the coupling capacitance is approximated as a plate capacitor (2), where S is proportional to the conductive area, d, represents the thickness of the dielectric material, and $\varepsilon_0\ \varepsilon_r$, are given properties of the used dielectric material.

$$C = \frac{\varepsilon_0\ \varepsilon_r\, S}{d} \tag{2}$$

Air, acquiring a relative permittivity of almost 1, can be used as an insulation medium, especially in wireless power transfer setups. However, the inconvenience of this design's technique is the requirement for greater clearances, notably at higher isolation voltages. That is 50 mm for an operating voltage of 35 kV_{RMS} [21]. Nonetheless, to obtain compact transformers, solid or liquid insulation techniques should be used instead. Literature demonstrates PCB transformers using

insulation material such as polypropylene, polysterimide, polyimide or polytetraflouorethylene (PTFE) and FR4 Epoxy, with thickness ranging from 1-1.6mm.

The newly proposed transformer in this chapter, with an insulation thickness of 2.8 mm revealed better immunity to dv/dt application. It was constructed to be integrated in a gate driver card comprising a power transformer which was augmented in thickness to withstand higher potential of 3.3 kV SiC MOSFET modules. In addition to the transformer's topology, dielectric material governs the transformer's ability to withstand voltage. Therefore, the ideal properties of the dielectric material are to be nonmagnetic, acquire low permittivity, and tolerate high electric fields. Presuming a uniform distribution of electric field, the transformer's insulation voltage primarily depends on the material thickness, $h_{dielectric}$, and the superlative field the material can withstand E_{max} before breakdown. However, since the field is not perfectly uniform realistically, the actual breakdown voltage level is always lower than E_{max} (3).

$$V_{breakdown} \leq E_{max}\, h_{dielectric} \tag{3}$$

D.1.1 Dielectric Material Consequence on CMTI

As mentioned earlier, a direct effect of the dielectric material constant is ensued on the coupling capacitance of the transformer. Alternative simulations were conducted to an identical geometry of a shielded transformer comprising different dielectric material properties, presented thereafter in table IV-6. The objective is to study the effect of the latter on the transformer's immunity to an application of 125 kV/µs dv/dt. Air is added merely to demonstrate the effectiveness of using it in some suitable applications where Kapton tape can be used as an insulation. As for RO4350 material, it is supplied by Rogers among the RO4000 series of high frequency circuit materials. They are based on glass-reinforced hydrocarbon and ceramic and not PTFE.

In addition to the above, a hybrid configuration was also simulated including both FR4 Epoxy at the uppermost and bottom layers engulfing the conductors, and RO4350B dielectric in the area between the shielding layers as demonstrated in figure IV-27. This was implemented to study if the homogeneity of the material or its adverse comprise an effect on the immunity of the transformer.

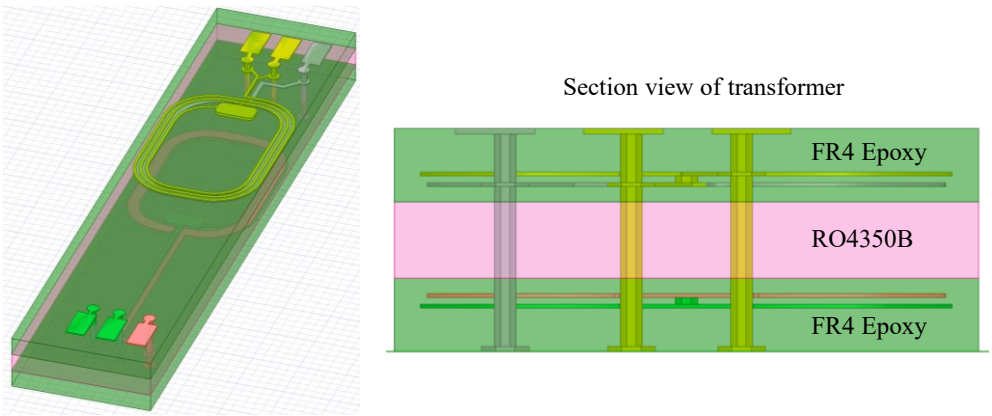


Figure IV-27: Hybrid dielectric material assignment in Ansys Q3D

The simulation of the application of a high dv/dt of 125 kV/µs to a 600 µm width typically shielded transformer was applied to the transformer to evaluate the effect of the different dielectric material compositions. Figure IV-28 below reveals the associated CMTN with each specified dielectric material. The results which are also numerically presented in table IV-6, affirm that there is a direct association between a transformer's dv/dt immunity and its dielectric material assignment. This is due to the reciprocity of the capacitance to the relative permittivity of the assigned material. In addition, a hybrid implementation revealed results close to a homogeneous application of the material engulfing the conductors, FR4 epoxy in this example. Therefore, efficient election of a robust dielectric material with regard to the application and operation of the transformer is also an imperative area to be studied and examined.

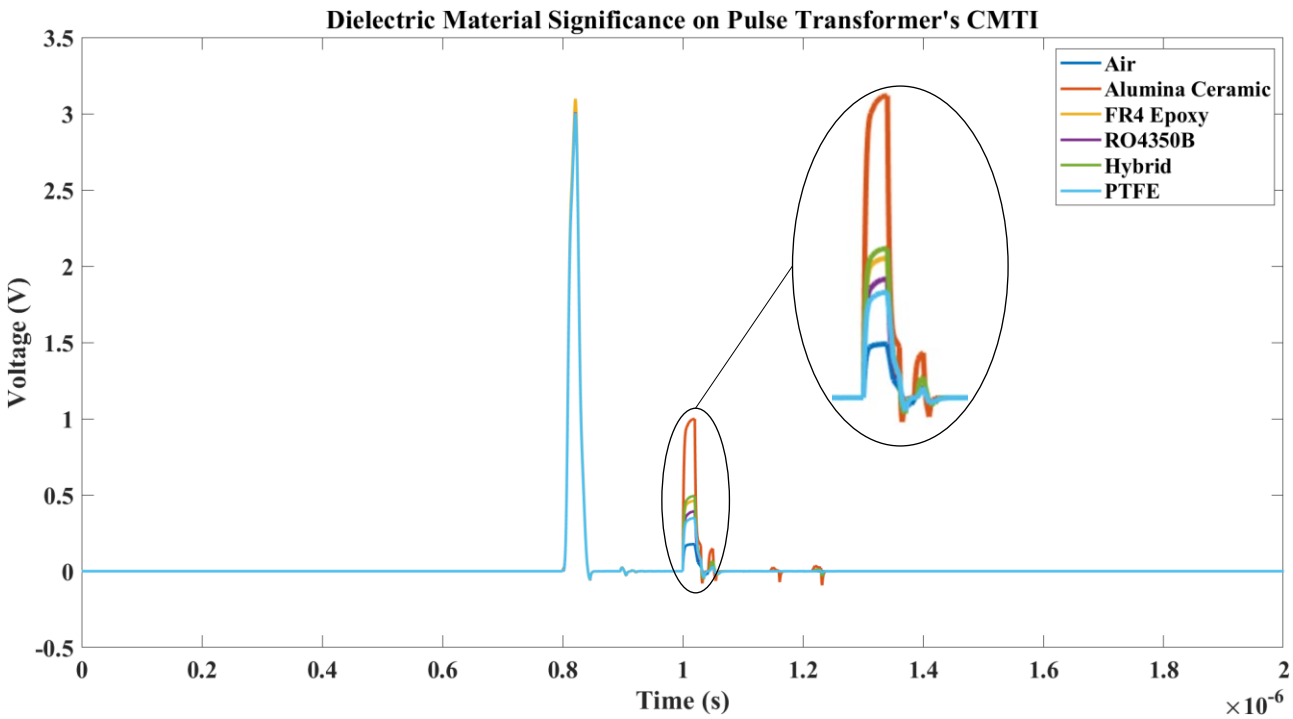


Figure IV-28: Dielectric material effect on transformer's CMTI

Table IV-6: Dielectric material properties used for simulating planar transformer

Dielectric Material	Dielectric Constant	Dielectric Strength	CMTN
Air	1	3 kV/mm	0.17 V
PTFE	2.1	≤ 24 kV/mm	0.35 V
RO4350B	3.66	30.7 kV/mm	0.4 V
FR4 Epoxy	4.4	≥40 kV/mm	0.46 V
Alumina Ceramic	9.8	≈ 31 kV/mm	1 V
Hybrid	-	-	0.49 V

E. CONCLUSIONS

Planar pulse transformers with alternative shielding designs were constructed for an application of 3.3 kV, respecting the European Standard EN 50178. The simulation analysis comprised an association of software tools including Altium Designer, Ansys Q3D Extractor, and its dynamic links. A spectral analysis was conducted on the utilized pulse signal of the pulse transformer to identify the eligible frequency band where the RLGC parasitic parameters were extracted and revealed consistent results. The study contributed to the establishment of an equivalent circuit model of the shielded transformers at an identified frequency, to investigate the shielding significance to a steep dv/dt application of 125 kV/µs, mimicking a power semiconductor's switching speed.

Divergent shielding designs were implemented, fabricated, and tested which are categorized under three main classifications. No shield, fragmented shield and solid shielding designs. The CM noise results attained after a dv/dt immunity test revealed a crucial interdependence on the shielding structure and design on the resultant outcome or the transformer's immunity. In addition, the significance of the shielding symmetry, width and length up to a certain limit was also presented and verified. After observing the results, an improper shielding design such as fragmented shields with large distance between the dissections or asymmetrical shields are insufficient and inferior. This is because, in comparison to an unshielded transformer these transformers were more susceptible and resulted with higher noise voltage. On the other hand, adequately grounded solid shielding designs revealed superior immunity up to a factor of two than the unshielded transformer. Moreover, this did not substantially affect the magnetizing inductance of the transformers. Densely chopped shielding structures as the ones demonstrated with 350 µm dissections, revealed a much better immunity result than the 150 µm fragmented shielding design. Furthermore, the magnetizing inductance of the densely fragmented shield revealed a 10% increase when compared to a solid shielded design structure with a favorable immunity outcome, however not as sufficient as a solid shielded structure.

Additionally, as a perspective investigation, the significance of the dielectric material composition on the transformer's immunity was also simulated to confirm direct reliance on the material's relative permittivity. The CMTN resulting from the utilization of Alumina Ceramic is greater by approximately a factor of two in correspondence to FR4 epoxy. This is interrelated to the relative permittivity of the mentioned materials.

Thus, despite being a miniature segment of the whole gate driver card, several factors in the construction, layout, and composition of the pulse transformer, impose a considerable impact on the performance, safety and EMC standard conservancy of the gate driver card.

GENERAL CONCLUSION AND OUTLOOK

A. CONCLUSIONS AND CONTRIBUTIONS

The realization of renovated power converter designs gained remarkable consideration in the industrial market, notably upon the evolution of WBG semiconductor devices. With a tendency to achieve high power density ratings, WBG-based semiconductors were explored as they allowed power converter devices to operate at exceptionally higher frequencies. This was greatly commercialized in PCB-based gate driver applications intending to drive the newly available fast-switching MV SiC semiconductors, namely, SiC MOSFETs. This development allowed the achievement of further efficient and compact MV converters, making them compelling to be used in numerous applications such as renewable energy collecting grids, high power electrical vehicle chargers and more electrical aircrafts.

However, power semiconductor devices are not lone components of a MV converter system. Passive components such as the pulse planar transformer, should be able to employ the full potential provided by the SiC power semiconductors. Pulse planar transformers, one of the fundamental building blocks of power converter systems, offer two critical functionalities: galvanic isolation and excitation of power semiconductor devices. Nevertheless, advantageous rapid switching speed attainments using this technology, causes high dv/dt occurrences, which make these devices prone to high EMI disturbances which can meet EMC standard confinements. Thus, DM and CM noise should be highly considered when designing pulse transformers in gate driver cards, especially that a faulty invoked switching order resultant from the passage of CM currents can lead to hazardous results. The transformer serves as the coupling between the primary circuit connected to the microcontroller unit and the secondary circuit connected to the power module. The coupling capacitance between the windings of the transformer serves as a permissive passage for CM currents which needs to be managed.

One of the most prominent CMN suppression techniques is shielding techniques. This is achieved by the insertion of adequately grounded electrostatic screens between the primary and secondary windings aiming to define a grounded route for the CM currents. Hence, intending to decrease the coupling capacitance between the latter. Thus, EMC standards are safeguarded in the gate driver card design which secures reliable operation and immunity of the transformer to high dv/dt application. As a result, the virtual prototyping of the design and its simulation before fabrication is a necessary and substantial process. Moreover, reliable equivalent circuit models of high frequency transformers acquiring lumped electrical parameters is essential to simulate their behaviour by constructing a model based on their physical characteristics and dimensions.

Accordingly, this dissertation concluded the following aspects:

A.1 Simulation Analysis

The importance of simulation before fabrication was highlighted in this dissertation. Constructing planar transformers based on a designed modelled will allow examiners to artificially review their

design and simulate alternative aspects before proceeding to fabrication. Hence, this allows the optimization of the design and increase the observations towards probable challenges that may arouse. Therefore, if adequately employed this will admit the fabrication of a particular revised version conforming to design specifications.

This dissertation presented an unprecedented simulation methodology, allowing the geometric modelling of a pulse planar transformer and analysing the latter in order to extract the parasitic parameters. The aim was to create an equivalent circuit model of the pulse transformer and examine the transformer's dv/dt immunity when applying 125 kV/µs between the transformer's disparate grounds. Therefore, this was achieved by using a collection of software tools, namely Ansys Q3D Extractor a prominent tool based on FEM noted in parasitic extraction. A simulation methodology chain was defined initiating from the modelling stage to the final steps of simulation analysis and results attainment. The simulation process included the design of the transformer in Altium Designer, where adequate data exchange files were exported and imported into Ansys SIWAVE. This step is vital to validate the layer stack up of the transformer and assign the material to each layer, as importing the ODB++ files directly into Ansys Q3D will not keep the stack up in the same format. Additionally, sometimes the design will lose some features due to incompatibility of AnsTranslator with the file, resulting in data losses or a resultant corrupted design. The model can be directly exported into Ansys Q3D from Ansys SIWAVE, where the simulation analysis occurs. Moreover, the design can be linked with Ansys Circuit Design, which is a schematic-based interface, that allows the user to add electrical parameters and perform an electronic circuitry simulation. Therefore, this permitted the simulation of a sub-circuit of the transformer to extract the S parameters and perform a dv/dt immunity test. Moreover, with the utilization of Ansys Q3D reduce matrix features, granted the construction of an equivalent circuit model of the transformer to check its susceptibility to high dv/dt stresses. Plus, the software permits the plotting of CG and AC RL fields, permitting to observe the charge density on the models. Finally, the use of the optimetrics feature allowed the assignment of variables, facilitating the ability to examine the variation of the shielding width, length and thickness.

A.2 Pulse Transformer Modelling

Constructing a reliable representation of the transformer as an equivalent circuit model is imperative to study the behavior of the transformer, primarily to investigate the parameters that highly affect the transformer's susceptibility to dv/dt application. This is imperative as the transformer intended to drive 1.2 kV SiC MOSFETs. Firstly, the spectral analysis of the pulse planar transformer was performed to determine an eligible frequency band to simulate the transformer. Furthermore, after analyzing the model in Ansys Q3D, the reduce matrix feature was used, where after attaining the original matrix, the user can simulate open and short circuit simulations to get the equivalent or lumped parameters of the primary and secondary windings. Moreover, the equivalent circuit export feature also allows the determination of the exact interwinding capacitance between the two windings upon grounding one of the nets. For example, to determine the capacitance between the primary and secondary when the secondary net is grounded, the user can ground the secondary shielding and extract the parasitic capacitance between the primary side and the secondary side. This is also

attainable when computing the capacitance between the secondary and primary when grounding the primary shield. This was further validated by extracting the model parameters by appointing two distinctive frequencies and by averaging the results over the entire frequency band. The outcome resulted in consistent values and similar result attainments. Therefore, an equivalent circuit model was constructed at a defined frequency of 50 MHz. It is noted that the realized simulated results confirmed the experimental analysis performed in the former thesis when utilizing an impedance analyzer and performing open and short circuit tests and to deduce the S parameters, ABCD parameters, and hence, the equivalent impedances or lumped electrical parameters of the transformer. Therefore, this can be attained easily using the defined simulation methodology after attaining an adequate simulation analysis of the designed model. Thus, in addition to validating the conformity of the transformer to a dv/dt application by using a subcircuit representation in Ansys Circuit Design. This further analysis allowed the creation of an equivalent circuit model and perform the same analysis where the results were conformed with the experimental ones. The eventuality of this analysis confirmed the necessity of inserting the grounded faraday shielding layers in mitigating the parasitic capacitance between the primary and secondary side, resulting in less CMTN upon the application of high dv/dt of 125 kV/µs.

A.3 Shielding Structure Design

The conclusion of the simulation analysis determined the fundamental significance of CMN suppression by the insertion of adequately grounded faraday shielding layers. This was highlighted by the mitigation of the noise upon dv/dt application between unshielded and shielded transformers. Moreover, the reliable reliance on the defined simulation process allowed the amelioration and renovation of the pulse planar transformer to be integrated in an ongoing construction and definition of a multi-level gate driver intending to driver two 3.3 kV SiC MOSFETs. Therefore, as the interwinding parasitic capacitance has a direct effect on the transformer's susceptibility, increasing the solid isolation from 500 µm to 1000 µm in the renovated design was essential for integration, which also further decreases the coupling capacitance between the layers. Moreover, despite providing a definite grounded path to the CM currents, the shielding structure design is a major key factor on the resultant coupling capacitance between the windings. Thus, not all shielding layers without exception can reduce the coupling capacitance, some poorly structured shields can render the transformer more susceptible to abrupt dv/dt stresses.

This was verified in chapter four by revealing the dependence of the coupling capacitance on the inserted shielding's structure, symmetry, length and width. Two shielding structures were constructed, solid and fragmented shields. The results attained were confirmed by simulation and experimental analysis, that there exists a convenient length and width of the shielding structure to mitigate the coupling capacitance. This was verified by applying an optimetric analysis in Ansys Q3D where the shielding length and width were assigned as variable and modified over an acceptable range to study the effect of the coupling capacitance. Accordingly, the designs of shielding structures were appointed based on the attained results to acquire the minimum coupling capacitance and CMN possible. Moreover, some poor designs were fabricated to verify that a poor shielding construction

can result in deficient CMN suppression in comparison to an unshielded transformer. This was confirmed with the asymmetrical structure, as a symmetrical structure with similar number of turns, single or multilayer, is requisite design fundamental to eliminate CM noise between windings. Another shielding structure aspect was approached by performing shield dissections, named fragmented shields, to assess the effect of such structure on the CMN and the magnetizing inductance. The results revealed that densely chopped shields are necessitated to attain favorable CMTI, at an expense of 10% increase in the magnetizing inductance in comparison to solid shield designs. It was also concluded that the variation of the thickness of the shielding does not impose a significant effect on the coupling capacitance. Moreover, the electric charge density field plots revealed how the existence of a shielding layer blocks the transfer of the charge to the secondary winding.

The attained simulation results of the equivalent circuit model undergoing a high dv/dt application, was physically constructed and experimentally applied at IETR lab. The results revealed conformity in terms of dv/dt application and CM noise results. EMC conservancy was established when using proper shielding structures.

A.4 Dielectric Material Importance

A supplementary exploration was conducted to study the effect of the elected dielectric material on the coupling capacitance of the transformer. Dielectric material such as Teflon and Rogers which comprise lower relative permittivity revealed less coupling capacitance and thus, lower CMTN. Therefore, the selection of a proper dielectric material is also essential to help decrease the planar transformer's susceptibility, depending on its dielectric strength and application necessity.

B. Recommendations and Future Work

In the framework of this thesis, it has been shown that MV SiC MOSFETs are permitting the realization of excessively efficient and compact isolated MV power converters and new gate driver topologies. However, it is apparent that there is no universal method that can eradicate alternative CM noise sources in planar transformers. Thus, although CM noise can be greatly mitigated, it remains a significant challenge that needs to be addressed. Relying on the results obtained in this thesis, different aspects could be further examined to improve the gate driver operation, and as a result the performance of the entire isolated MV converter, or other PCB-embedded applications.

- Alternative transformer concept: Different concepts of the utilized pulse planar transformer can be studied such as the coreless on chip transformer. They are especially convenient for applications acquiring SiC MOSFETs, since they are employed for robust isolation. These integrated transformers in gate driver applications allow greater operating limits in regards to core saturation, reinforced isolation, and satisfactory behavior at high temperature. Moreover, this will eliminate the overlap of the primary and secondary windings with the core, hence eliminating the parasitic capacitance between the core and earth which might return the current back to the windings. In addition, the possibility of an indirect coupling of the primary and secondary windings through the core will be nonexistent.

- Evaluate parasitic parameters in other aspects of the gate driver such as the SiC MOSFET half-bridge.
- Ansys Maxwell: Inspect and analyze the transformer in Ansys Maxwell, as it is an electromagnetic field solver allowing to inspect the time varying and frequency-domain magnetic and electric fields of the pulse planar transformer.
- Shielding Material: Inspect the utilization of alternative shielding material such as silver or brass instead of copper, and study the effect of different metallic material with different conductivity, on the evaluation of the pulse transformer.
- Embedded Passive Components (EPCs): The applied simulation methodology can be applied to PCB-embedded power dies [251]. Variable assignments of the arrangement can be applied to material, position, distance, thickness and other measures using the optimetrics analysis tool, where one can achieve an optimum design to attain minimum stray parameters.

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DOCTORAT BRETAGNE LOIRE / MATHSTIC

Nantes Université

Titre : Modélisation en Mode Différentiel et en Mode Commun des Transformateurs d'Impulsion pour les Applications Gate-Driver

Mots clés : Compatibilité Electromagnétique (CEM), Écrans Électrostatiques, Gate-driver, Mode commun (CM), Transformateurs d'impulsions, Wide-bandgap (WBG)

Résumé : L'accroissement de la vitesse de commutation des composants de puissance dits « grands gaps » tels que les MOSFETs à carbure de silicium (SiC) et leur capacité à fonctionner à une fréquence élevée ont amené de nouveaux défis à résoudre tels que les problèmes d'interférence électromagnétique (EMI). Les travaux de recherche présentés dans ce mémoire visent à améliorer le design des transformateurs d'impulsions intégrés dans les étages de commande rapprochée (nommé gate-driver). L'objectif visée était de limiter les capacités parasites de ces transformateurs qui sont à l'origine de courants de mode commun (CM). Une méthode permettant de concevoir et de simuler ces transformateurs d'impulsions avec différentes structures de blindage a été mise au point. Le transformateur est d'abord créé sous Altium Designer, tout en respectant la norme IPC-2221. Le design de ce transformateur est ensuite exporté vers ANSYS Q3D Extractor où un modèle électrique équivalent est extrait. En simulation, des impulsions d'amplitude 1,4 kV et présentant des dv/dt de 125 kV/µs ont été appliquées entre le primaire et le secondaire des transformateur, ce qui a permis de comparer la susceptibilité du transformateur avec différentes structures de blindage. L'influence de la forme de l'écran, des variations de sa longueur, sa largeur et son épaisseur est étudié. En parallèle de la simulation, les transformateurs étudiés ont été fabriqués et soumis aux mêmes dv/dt qu'en simulation. La comparaison des résultats expérimentaux avec les simulations ont permis de valider les modèles.

Title : Differential Mode and Common Mode Modelling of Pulse Transformers for Gate-Driver Applications

Keywords : Common Mode (CM), Electromagnetic Compatibility (EMC), Gate-driver, Pulse transformers, Shielding, Wide-bandgap (WBG)

Abstract : The higher switching speed attainments of WBG power devices such as silicon carbide (SiC) MOSFETs, and their ability to operate at higher switching frequencies, becomes conflicting when challenged with electromagnetic interference (EMI) issues. The objective of this dissertation is to improve the design of pulse transformers integrated in an intermediate stage of a power converter system, known as a gate-driver. The main goal is to mitigate the parasitic capacitances of these transformers, which are the source originators of common mode (CM) currents. A modelling and simulation scheme of pulse transformers with alternative shielding structures has been developed. The transformer is primarily designed using Altium Designer while respecting IPC-2221 standards. Its geometry is then exported into ANSYS Q3D Extractor, where an equivalent circuit model is extracted. The correlation of the susceptibility of pulse transformers comprising different shielding structures is simulated by applying pulses of 1.4 kV amplitude, representing a dv/dt of 125 kV/µs, between the primary and secondary distinctive grounds. The influence of the shielding configuration, and the variation of its length, width and thickness is explored. In addition to the applied simulation analysis, an equivalent experimental examination was conducted after manufacturing the studied transformers. The correspondence of the simulation and experimental results permitted the validation of the models.