Integrated circuits and systems for energy-efficient processing and advanced communication systems

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Université de Lille

Habilitation à Diriger des Recherches

Ecole Doctorale Sciences Pour l'Ingénieur

INTEGRATED CIRCUITS AND SYSTEMS FOR ENERGY-EFFICIENT PROCESSING AND ADVANCED COMMUNICATION SYSTEMS

CIRCUITS ET SYSTEMES INTEGRES POUR LE TRAITEMENT ENERGETIQUEMENT EFFICACE ET LES SYSTEMES DE COMMUNICATION AVANCES

Antoine FRAPPÉ

14 Juin 2019

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Antoine FRAPPÉ

June 14th 2019

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Associate Professor in Electrical Engineering
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EDUCATION

2007 **PhD in Microelectronics** University of Lille, France.
"All-digital RF signal generation using ΔΣ modulation for mobile communication terminals"

2004 **Master degree** - Microwave and Microtechnologies - Grade B - ranking 1st
University of Lille, France.

2004 **Engineering diploma -** Major in Microelectronics.
Institut Supérieur de l'Electronique et du Numérique (ISEN), Lille, France.

PROFESSIONAL EXPERIENCE

2009 - **Yncréa Hauts-de-France - ISEN Lille, France**
Associate Professor / Head of the Integrated Circuit Design Research Group

2008 - 2009 **Berkeley Wireless Research Center, University of California, Berkeley, CA**
Fulbright Visiting Postdoctoral Researcher

2007 - 2008 **IEMN – ISEN – STMicroelectronics, Lille, France**
Research Associate on RF circuit design

2004 - 2007 **ISEN, Lille, France**
Teaching Assistant in Electrical Engineering

LANGUAGES

French by mother tongue, Fluent **English,** Basics of **German**, **Spanish and Mandarin**

PUBLICATIONS

9 peer-reviewed journals / 29 international conferences / 3 book chapters / 320 citations / h-index: 8
Major publications:

- **A. Frappé**, A. Flament, B. Stefanelli, A. Kaiser, A. Cathelin, "An All-Digital RF Signal Generator Using High-Speed ΔΣ Modulators", IEEE Journal of Solid-State Circuits, vol.44, no. 10, pp. 2722-2732, Oct 2009
- C. Thakkar, L. Kong, K. Jung, **A. Frappé**, E. Alon, "A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS", IEEE Journal of Solid-State Circuits, vol.47, no. 4, pp. 952-968, Apr 2012
- A. Flament, **A. Frappé**, A. Kaiser, B. Stefanelli, A. Cathelin, H. Ezzeddine, "A 1.2 GHz Semi-Digital Reconfigurable FIR Bandpass Filter with Passive Power Combiner", Proceedings of the 34th European Solid-State Circuits Conference, ESSCIRC 2008, Edinburgh, Scotland, UK, September 15-19, 2008
- J. Muller, B. Stefanelli, **A. Frappé**, L. Ye, A. Cathelin, A. Niknejad, A. Kaiser, "A 7 -bit 18th order 9.6 GS/s FIR up-sampling filter for High Data Rate 60-GHz Wireless Transmitters", IEEE Journal of Solid-State Circuits, vol.47, no. 7, pp. 1743-1756, Jul 2012
- F. Gebreyohannes, **A. Frappé**, A. Kaiser, "A configurable transmitter architecture for IEEE 802.11ac and 802.11ad standards", IEEE Trans. Circuits Syst. II-Express Briefs, 63, 1, pp. 9-13, January 2016

GRANTS AND AWARDS

Best student project 16-17 Yncréa HDF, for a project on audio keyword recognition
Best research project 15-16 Yncréa HDF, for a project on electronic textiles
Best Student Paper Award IEEE VLSI 2011, Kyoto, Japan
Fulbright grant obtained in 2008-2009 as a postdoctoral researcher at UC Berkeley, CA

OTHER ACTIVITIES

TPC Member IEEE ESSCIRC (2015 – 2016), IEEE ICECS (2014 – 2018), IEEE RFIC (2018 -)
IEEE Senior Member – Secretary and Treasurer IEEE Circuits and Systems (CAS) Society France
Elected board member of Yncréa Hauts-de-France

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Thanks to all the persons I collaborated with. It is always a pleasure to meet you during conferences, project meetings or teleconference calls. Special thanks to Andreia for the long-lasting collaboration in the ST-IEMN common lab.

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I thank all my friends and family for their active support.

My warmest acknowledgment goes to my wife Louise, who accompanies me on a daily basis, and to my three children, Valentine, Jean and Raphaël, who are adorable and allow me to be multi-tasking. I love you.

How not to forget someone in this acknowledgement part? Please excuse me if I did and to catch up, I would be happy to discuss with you about electronic stuffs or lighter topics around a nice beer 😉.

Chapter 1 **Introduction**

This manuscript is the result of more than 10 years of research in the Integrated Circuit Design Research Group at ISEN, an engineering school in Lille, France. This research activity is also part of a research group at IEMN in Villeneuve d'Ascq, on the campus of the University of Lille, where we benefit from the equipment and laboratory environments. In addition, a common lab has been active between STMicroelectronics and IEMN since 2003 and provides a common settlement for the development of ambitious projects taking into account industry-related considerations and for access to the most advanced integration technology nodes for our demonstrations. This fertile environment is the ground that allowed me to develop interesting research topics, which are mainly discussed and detailed in this manuscript. The philosophy and essence of the work is to start by studying specific concepts and to develop systems that can prove the validity and utility of the proposed concept. We then move towards hardware demonstrations in the form of the design, fabrication and measurement of integrated circuits. In this manuscript, you will find an overview of the results of the research, where the selected contributions are detailed and placed in the appropriate context.

This manuscript is composed of 7 chapters and two annexes:

- After this introduction, the second chapter is entitled "Research directions" and is an attempt to trace the paths that led me to the research presented here.

- The technical contributions are presented in Chapter 3 and 4. They detail the contributions to digital RF transmitters and baseband circuits for mmW receivers, respectively. In the first chapter on digital transmitters, I have tried to highlight the many works thematically, drawing on the main challenges in digital RF transmitters, rather than a chronological description. I hope that the reader will find an interest in the concepts that are demonstrated and that it will open new ideas and research directions, whether for digital RF transmitters or applied to other areas of research, for example, optical links or body area communication systems. The next section on

baseband circuits highlights three research works on energy-efficient systems for high data-rate receivers. It is partly related to my postdoctoral experience at UC Berkeley and includes further work on the same topic.

- In Chapter 5, research perspectives are developed. I want to emphasize here that the focus is now on energy-efficient systems for smart embedded devices. In fact, the Internet of Things (IoT) connects devices and objects with built-in sensors and has to deal with tons of data to be transmitted, while artificial intelligence (AI) brings intelligence to machines. Behind the idea of near-sensor computing (also known as edge computing or AIoT for Artificial Intelligence of Things), we want to include analysis and decisions as close as possible to the source of sensed data, by developing an energy-efficient integrated hardware. Investigations include audio signal processing (for local tasks such as voice activity detection, speech recognition or event detection) and biological signal processing (ECG, ECoG, etc.) for body area networks. Implementation issues will also be addressed by examining body-coupled communications or connected textiles.

- Chapter 6 provides a detailed list of professional activities related to the research works. This includes student mentoring and supervision, teaching activities, involvement in the national and international academic context, such as project expertise, reviews, Ph.D. juries or membership in conferences, local administrative duties and collaborative projects.

- Finally, a general conclusion is drawn in Chapter 7.

- In the first Annex, I wanted to describe a gallery of chips, offering an overview of the diversity of the fabricated chips and a brief description of the technical details.

- The last Annex concerns scientific publications. A short summary is given at the beginning, followed by the complete list of publications and the reproduction of 8 selected publications for easy reference.

I hope you will like to read as much as I liked to write this manuscript!

Chapter 2 Research directions

Opportunities, fruitful encounters, and thoughtful choices trace a path in the research landscape. This chapter aims at relating my professional career path in relation to the research context and to expose the main research directions taken.

2.1. Passion for electronics

I have always been curious about electronic systems and how they work. My father injected me the virus of electronics at a very early age. He was CTO of a small local company delivering custom-made audio and video electronic products, like commutation matrices or PAL/NTSC conversion modules. I remember helping him assemble and weld PCB boards all day long on the production line. He even offered me a multimeter and soldering iron as a birthday gift.

Having spent my childhood in Dunkerque, it was natural for me to study electrical engineering at ISEN (Institut Supérieur d'Electronique et du Numérique) in Lille since it would fulfill my desire for technical deepness in this field. I discovered many domains, as diverse as telecommunication systems, computer science, quantum physics, cryptography, or acoustic modeling. I even ended up studying the details of a piezoelectric sensor design and simulating it with Finite Element Method (FEM)-based tools through a project and an internship in a start-up in Besançon that develops systems for non-intrusive defect detection.

As I wanted to dig further into microelectronic systems, I discussed with several professors at ISEN that described me advanced research projects and registered to the microwave and micro technologies Master program at the University of Lille 1, with the goal to attain a degree that would allow me to pursue my studies in a Ph.D. program. I have then chosen to do my research internship in Pr. Andreas Kaiser's integrated circuit design group, at the same time as 3 other colleagues, including my friend Axel Flament. Dimitri Galayko supervised my work on digital ΔΣ modulators. I got the engineering diploma from ISEN and the Master of Advanced Studies (Diplôme d'Etudes Approfondies–DEA) from the University of Lille 1 in 2004. Based on the results achieved in the DEA program, I received a research grant from

the Ministry of National Education, Higher Education, and Research to start a Ph.D. program supervised by Pr. Andreas Kaiser.

2.2. Ph.D. thesis on IC design and digital transmitters

During my research internship at Master level, I performed system-level studies in Matlab of ΔΣ-based transmitters and concretized that digital transmitters built upon these techniques would be a great research object for the Ph.D. thesis. At first, after compiling bibliographical data, one of the motivation point of this research was the publication in 2001 from Pr. Asbeck, Larson and Galton from UC San Diego entitled "Synergistic Design of DSP and Power Amplifiers for Wireless Communications" [1], in which they describe the potentiality of class-S amplifiers. In the conclusion, they derive future directions, reproduced below together with the associated figure.

> *As the speed of DSP advances, algorithms in which the DSP provides signals at RF can be envisioned (particularly for switching amplifiers, in which the inputs are inherently digital signals). An entirely digital implementation of the entire transmitter chain is shown in Fig. 13. Upconversion to RF and bandpass delta-sigma modulation is accomplished digitally. With a 1-bit digital output, the inaccuracies of high-resolution digital-to-analog converters at high frequency can be circumvented. In the scenario shown, the clock frequency of the DSP is 4× higher than the center frequency of the RF signal. The digital transmitter potentially offers many benefits, including programmability and reconfigurability, absence of tuning or aging problems, as well as easy integrability and testing. It can be an important element in a "software defined radio".*

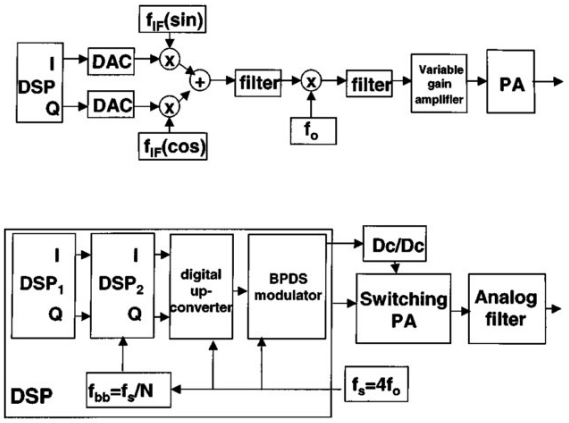

Fig. 13. Comparison of traditional wireless transmitter architecture, based on analog circuits, with a possible DSP-based architecture.

No need to explain that when I came to read these statements, the objectives of my research stand clear. I wanted to go there! My work focused on proposing solutions to generate RF signals with only digital components. Digital gates were available in design kits in 130 nm and 90 nm CMOS, but preliminary investigations on straight-forward structures showed speed limitations. So, I re-opened the bedside book from Jan Rabaey on digital integrated circuits [2] and designed my computation cells. Selecting an effective logic style was not enough, and I needed to think about the structural approach to the problem. During a visit to

the LIP6 laboratory in Paris, a short discussion about the issues I faced opened a large new panel of possibilities. I went on exchanging with Raphaël Daouphars about redundant arithmetic schemes and how to do the required operation from an arithmetic computational point of view. This is the beauty of inter-disciplinarity since this meeting was the turning point to bring about high-speed delta-sigma modulators (I would learn later that the straight-forward approach would be reachable in more advanced technology nodes). I built a first 3×1 mm² 96-pad 90 nm chip, in which we could only characterize the output stage since there were huge supply variations in the clock domain that prevent proper operation. I learned a lot in understanding the incorrect behavior and re-spun a second successful version, now sizing 4×0.8 mm², counting 103 pads and code-named Fulbert II. The obtained results on this prototype chip matched the expected ones and we published the work in the IEEE Journal of Solid-State Circuits [3], the premier journal covering integrated circuits.

The diversity of technical challenges and acquired experience is large as the Ph.D. work has included system-level behavioral modeling, integrated circuit design in advanced CMOS technologies, custom packaging, test, interfaces, PCB design, FPGA prototyping and programming, and hands-on lab measurements of the demonstrator. Even if I performed an academic thesis, the Nano 2008 program and STMicroelectronics – IEMN common lab supported the developments. I acknowledge the constant help of ST staff through regular meetings and training.

Though the digital signal produced by the delta-sigma modulator is of high fidelity in the considered band, the process of noise shaping pushes the noise outside the band of interest thus polluting the complete spectrum with large noise. In parallel to my investigations, Axel Flament studied means such as a passive power combination to boost the channel power and to include noise filtering using mixed-signal concepts such as semi-digital FIR filtering. This work showed enough originality to pave the way to further concepts.

We extended our work in the MOBILIS European project, in which larger demonstrators included the developed circuits to promote transmitter chains based on bulk acoustic waves (BAW) devices. We have then shown that BAW filters can solve the problem of noise filtering outside the band of interest and on the nearby receive bands.

Finally, as we continued the development of digital transmitters, Crépin Nsiala Nzéza, a post-doctoral researcher with a background on telecommunication systems, joined the group and we have investigated complex digital delta-sigma modulators in which the noise transfer function can be engineered to relax the filtering requirements in selected frequency bands.

2.3. A year of discoveries at UC Berkeley

I had the great opportunity to get selected by the Franco-American Fulbright Commission to pursue research for a year in an American institution. My application has focused on circuit design for future communication systems in a renowned group at UC Berkeley. The Fulbright grant not only offers a financial support for this stay but also a complete experience, through the Fulbright enrichment program and the fruitful meeting of people from different horizons and cultures. Throughout the stay, I also discovered how prestigious being a Fulbrighter is in the US.

I worked in Elad Alon's group at the Berkeley Wireless Research Center as a post-doctoral scholar through the Fulbright program from September 2008 to September 2009.

During my time in the lab, my research focused in two areas: (1) clock distribution for a wafer-scale radio using standing wave oscillators, and (2) on the architecture and implementation of an energy-efficient 10 Gb/s baseband for 60 GHz wireless communications. The second project resulted in a higher overall impact on the community.

The main motivation for this work was to reduce the power consumption of such 60GHz basebands to enable multi-Gb/s wireless links within mobile devices such as a cell-phone. Our approach breaks from traditional transceiver design paradigms, and rather than perform most of the high-speed signal processing in the digital domain, do so in the mixed-signal domain. The advantage of this approach is that at the dynamic ranges of interest in this system, analog processing requires less power than digital processing. Such a design still requires large digital processing to adapt and control the analog circuitry. The experimental results from the transceiver design (which dissipated ~50 mW at 10 Gb/s in a 65 nm process – an order of magnitude better than earlier designs) were published in the 2011 IEEE Symposium on VLSI Circuits in June 2011 [4], received the Best Student Paper Award and an extension appeared in the IEEE Journal of Solid-State Circuits in 2012 [5].

During the time I spent in UC Berkeley, Jonathan Muller started a CIFRE Ph.D. program with STMicroelectronics and IEMN and joined the Berkeley Wireless Research Center as a visiting student. I worked with him and encouraged his research towards ultra-high-speed signal processing for a 60 GHz transmitter baseband. His developments helped in understanding limits of high-speed operation in advanced CMOS technology.

2.4. Assistant Professor position at ISEN Lille

When I came back from the US in 2009, I got an Assistant Professor position in the electrical engineering department at ISEN Lille, under the responsibility of Andreas Kaiser. I joined the group I used to work with, so I knew the other professors and appreciated the context and research methods. As an Assistant Professor, I undertook 3 main objectives. The first duty concerned teaching responsibilities. I oversaw the introductory courses in analog and digital electronics for Computer Science students and more advanced courses related to electronic systems. Teaching involved diverse learning sequences, ranging from traditional lectures to codesign-based projects. The second mission concerned establishing a research activity within the group. The tasks went from defining potential impactful subjects, submitting applications to gather funding and support, supervising Master or Ph.D. students, and following technical advancement of granted projects. Developing industrial collaborations and contracts makes up the third direction.

The STMicroelectronics – IEMN common lab was established for many years and supported by the Nano 2012 national program. It offered a privileged link with ST staff and access to advanced CMOS technology. Thus, the research in integrated circuit design was positioned to leverage these digital technologies by showing the potential for analog and mixed-signal integrated systems.

I contributed to several already started projects. The TEROPP ANR project concerned the study RF terminals for opportunistic radio applications, while in the European MEDEA+ SIAM and QSTREAM projects, the focus was on silicon-based high data-rate communication systems in the mmW bands. In this context, we started two Ph.D. thesis: Arnaud Werquin studied digital RF power amplifiers (PA) and Baptiste Grave considered baseband systems for mmW applications. They both came up with very innovative ideas, such as a multi-rate multi-path approach to deal with image replicas in digital RF PA or subsampling methods to demodulate mmW signals.

In 2010, we collaborated for the launch of the ENIAC MIRANDELA project, which involved over 30 European partners. I was at first responsible for the work carried by ISEN Lille, but as our position evolved inside the project, I eventually led the cluster on mmW systems and sensors and co-animate the work-package on the full application demonstrator. This was rewarding and challenging since I coordinated the work from many institutes,

including researchers from CEA-Leti, Aalto (Finland), IEMN, STMicroelectronics, and ST-Ericsson.

Apart from a strong collaboration with STMicroelectronics, I started other industrial contracts with e2v, Thalès Alenia Space, and Alcatel-Lucent. e2v is a leader in high-speed high-resolution data converters and solicited us for a study on delta-sigma data converters. I worked with them on the Verilog-AMS modeling and simulation of an integrated high-speed converter with excessive in-loop delays. Thalès Alenia Space (TAS) considered our developments in digital RF transmitters and wanted to explore the architectural solutions for wideband signals (>250 MHz) in the Ku band (12 – 18 GHz). The collaboration with TAS started with a Master-level internship (Guillaume Rembert), followed by some specific studies on an in-depth understanding of LO leakage and image rejection due to IQ mismatch.

The collaboration with Alcatel-Lucent consisted in the study and design of a delta-sigma-based digital RF transmitter for base-station applications. We built a complete demonstrator composed of a 4.2×2 mm² 40 nm integrated circuit. The integrated delta-sigma digital quadrature modulators operated up to 8 GS/s and delivered a 4-bit output, compatible with the input of an RF PWM InP ASIC under development. I am glad to have led this very ambitious and successful project, which has been a collaborative work with my colleagues Axel Flament, Baptiste Grave and Bruno Stefanelli. Scientific publications on these industrial collaborations are lacking, but we produced many internal reports, listed in the publications list in Annex A.

2.5. ICD research group leadership

In late 2011, the ISEN Lille electrical engineering department has been re-organized and named SMART (as an acronym for Systèmes Microélectroniques, Automatique, Robotique, Telecommunications in French), supervised by Emmanuel Dubois. I took the responsibility of the integrated circuit design (ICD) research group. The missions involved managing and animating the group, defining the research directions, and dealing with financial, HR and administrative aspects of the research group. I was further responsible for finding contractual opportunities and executing current collaboration contracts. I took part in the ISEN Lille Research Council and Executive Committee-at-Large.

While the MIRANDELA project and industrial collaboration with Alcatel-Lucent on communication systems were running, I was eager to develop some new trends into our

research scope. Through an invited lecture at CMOS Emerging Technologies Symposium in Whistler, Canada, about digital transmitters, I attended a short presentation by Mariya Kurchuk, a former Ph.D. student in Yannis Tsividis' group at Columbia University on continuous-time digital signal processing (CT DSP) [6]. I found interest in these computation systems and the discussions I had with her showed all the potential and advantages of these solutions–and the associated challenges. Back in Lille, since we carried investigations on mmW baseband receiver architectures, the event-driven nature of the continuous-time digital signal processing seemed to offer great interest as it would remove the problems associated with the clock recovery and phase interpolation implementation. On top of this, digital CT filters proved competitive compared to analog implementations and envisioning an equalization scheme based on discrete events would be helpful for channels with long responses, such as 60 GHz channels. This has set the objectives of Ilias Sourikopoulos' thesis. His work contributed to the design of tunable digital delay cell that leverages the 28 nm FDSOI technology features and showed state-of-the-art performance.

Even though systems for communications in the 60 GHz band standardized, scenarios of deployment remained unclear and developments of circuit-level architectures for these bands stayed at a low level of maturity for integration into portable devices. With STMicroelectronics and IMS Bordeaux, we discussed the scenarios and a convergence of the WiFi (the emerging 802.11ac) and WiGig (802.11ad) systems into a configurable and shared structure sounded to be interesting to investigate. From an implementation point of view, the complexity of the interfaces was similar with a narrow bandwidth (20 to 40 MHz) and high resolution on one side, and a wide bandwidth (>1.5 GHz) and low resolution on the other side. We built the WENDY project that got accepted into the ANR INFRA program. This has led to the developments of Fikre Tsigabu Gebreyohannes' thesis on a configurable semi-digital filtering DAC (FIR-DAC), whose number of coefficients is adaptable and act as a reconstruction filter for the WiFi signals and as a channel filter for WiGig signals.

The STMicroelectronics – IEMN common lab renewed in the frame of the Nano 2017 program and I took an active part in this initiative as co-chair of the theme on Communication Systems (together with Andreia Cathelin from STMicroelectronics and Nathalie Rolland from CSAM group at IEMN). The work program targeted to show the potentiality of the 28 nm FDSOI technology, through ASIC design and integrated demonstrators. This created a favorable framework for new Ph.D. students: Cristian Marin investigated integrated digital transmitters and Matteo Causo started a research path on neuro-inspired computing architectures in collaboration with Jan Rabaey at UC Berkeley. Later, the same framework

helped in funding further Ph.D. subjects. Dipal Ghosh worked on multi-Gbps chip-to-chip communications as a collaborative effort between CSAM group and ours at IEMN, Angel Gonzalez pursued investigations on continuous-time DSP for feature extraction on audio signals and Robin Benarrouch started as a CIFRE Ph.D. student on integrated human body communications systems, again in collaboration with UC Berkeley. The ST – IEMN common lab creates a fertile ground on which we can aggregate competencies and attract complementary funding. I hope the support of future nation-wide programs for Microelectronics could sustain these efforts.

Since research funding is often very opportunistic, we got contacted by the Centre Européen des Textiles Innovants (CETI) in Tourcoing, who was building a consortium of companies, research centers, and academic groups to develop the future industrial sector on connected and autonomous textiles. This industrial project named AUTONOTEX emerged within a month and a half and got accepted to the PIAVE call from the BPI. I have never experienced such a fast build-up for a consortium involving 13 partners. A strong collaboration between the partners - Nicomatic (electrical connectors manufacturer), Percall (IoT solutions provider) and Mulliez-Flory (professional clothing company) - helped build a connected safety sheet for disoriented hospital patients. In this project, I want to point out the challenges related to inter-disciplinarity. Exchanging ideas and concepts on electronics and integrated systems with people specialized in textile dyeing or in polymer chemical analysis leads to a need for a non-negligible volume of pedagogy in explaining developments and agreeing on potential solutions. Meeting the project objectives entails understanding partners requests and constraints. This requires efforts but is valuable when achieved.

I want to close this part by mentioning that the research subjects we are carrying are evolving and that the focus is shifting towards low-power embedded systems for smart sensors. We have the competences to show novel integrated architectures to overcome the challenges of near-sensor computing. Benoit Larras joined as a new faculty in the group to build upon these new perspectives. He has a complementary education in the design of integrated silicon neural networks.

2.6. Conclusion

My experience as a researcher is personally very fruitful and I want as a conclusion to underline some rewarding activities. First, supervising students, so that they can eventually

defend their work and achieve their career goals, is a day-to-day challenge. This includes follow-ups and weekly meetings, as well as personalized support and coaching. I maintain an open-door policy so that the Ph.D. students are always welcome to come and discuss any matter with me. In Section 6.1, a list of M.Sc. students, Ph.D. students, and post-doctoral researchers I supervised details the position in industry or academia they are holding after graduation. I am very grateful to see that I was able to reveal the potential of the students I followed. I am convinced the HDR diploma will confirm my ability to lead a research group and supervise students.

Additionally, since the HDR also gives the opportunity to report on thesis works, I would be very happy to contribute to the evaluation of the research outcome of Ph.D. students from other laboratories in France. I have already been active in Ph.D. committees in other countries (detailed in Section 6.3.2). I served as an opponent at Chalmers University of Technology in Gothenburg, Sweden and as a preliminary examiner at Victoria University, Melbourne, Australia and at Aalto University, Helsinki, Finland. These were interesting and rewarding experiences.

Finally, I am regularly solicited for expertise works, reviews of journal papers and participation to technical program committees for several conferences. A complete list can be found in 6.3. This promotes the level of research I try to carry within my field of expertise and opens new horizons.

The story goes on…

2.7. Bibliography

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60 GHz Baseband in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 952–968, Apr. 2012.

[6] M. Kurchuk, C. Weltin-Wu, D. Morche, and Y. Tsividis, "GHz-range continuous-time programmable digital FIR with power dissipation that automatically adapts to signal activity," in *2011 IEEE International Solid-State Circuits Conference*, 2011, vol. 53, no. May 2010, pp. 232–234.

Chapter 3 Contributions to Digital RF Transmitters

This chapter will present research developments in the research group under my supervision around digital RF transmitters, from the origins of my PhD thesis work to recent demonstrations of integrated digital transmitters.

First, an introduction will explain why and how to move from traditional architectures to digital transmitters. An analysis of the existing concepts and architectures will be exposed, and this part will be concluded by presenting the key challenges. Then, the three subsections will develop specific research related to each challenge and show how our research has helped to address some of them. The structure of this chapter is not chronological. I chose to present the work thematically, using the many developments to illustrate the research carried out.

The first subsection will address the digital high-speed operation necessary to enable digital transmitters. It will consist of a description of my doctoral thesis work, focused on the digital generation of RF signals, followed by a more complete implementation of delta-sigma multi-bit modulators for base stations, in collaboration with Alcatel-Lucent. Time-interleaved delta-sigma modulation is then presented through a description of the work of Cristian Marin. Finally, high speed digital processing is pushed to its limit to reach bandwidths compatible with mmW frequency communications. Jonathan Muller has studied this last part.

The next subsection discusses output stage topologies for embedded transmitters. It will briefly cover the use of an inverter-based output stage with a passive network combination and the integrated switched-capacitor preamplifier as part of a digital RF transmitter demonstrated by Cristian Marin.

Last section deals with the management of out-of-band spurious emissions. Four contributions are identified here. The multi-rate multi-path approach for polar DPAs,

developed by Arnaud Werquin, is presented first. Then, techniques to deal with shaped quantization noise of delta-sigma modulators include the integration of analog bulk acoustic wave filters (MOBILIS project), the engineering of the noise transfer function (Crépin Nsiala Nzéza and Cristian Marin works) and finally the use of semi-digital FIR-DAC (Axel Flament, Fikre Tsigabu Gebreyohannes, Cristian Marin).

3.1. Introduction to digital RF transmitters

3.1.1. Traditional transmitters

A traditional analog direct conversion quadrature transmitter architecture is shown in Figure 3-1. The generated quadrature I and Q signals are converted in the analog domain by DACs at a f_{BB} rate and then low-pass filtered to remove unwanted image replicas at multiples of f_{BB}. The quadrature baseband signal is then converted to the local oscillator frequency f_c before being amplified by the power amplifier and eventually band-pass filtered.

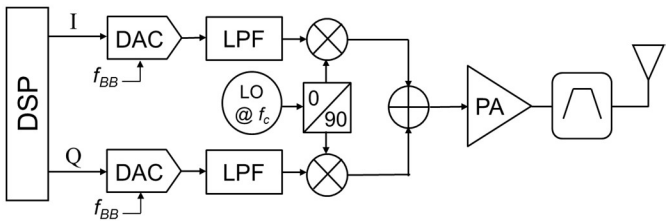


Figure 3-1 Traditional direct-conversion transmitter architecture including Digital Signal Processor (DSP), Digital-to-Analog Converters (DACs), Low-pass Filters (LPF), Local Oscillator (LO), and Power Amplifier (PA).

Environment-aware radios require the transmitters to reconfigure themselves and adapt their physical key settings to take into account, for example, a specific carrier frequency, signal bandwidth, dynamic range, or consumption target. A flexible transmitter, adjusted using the receiver's spectrum-sensed information, adds intelligence to the system [1], must meet existing wireless standards, and provide a scalable platform for future standards.

Single-chip multiband solutions have emerged and have proposed sharing the digital interface and most mixed-signal blocks, local oscillators, and mixers. However, many elements of the transmission and reception chain are still redundant, placed in parallel and activated on demand. In addition, the removal of external components, such as SAW filters, is in essential element of integrated transceivers. As an illustration, Skyworks highlighted at the ISSCC 2009 a 25 mm² 7-band 2G / 3G single-chip transceiver in 0.13 µm [2]. Figure 3-2 shows the block diagram of the transmitter system, in which 13 discrete components (7

duplexers / filters, 3 switches and 3 PA modules) are needed to meet the proposed standards and bands.

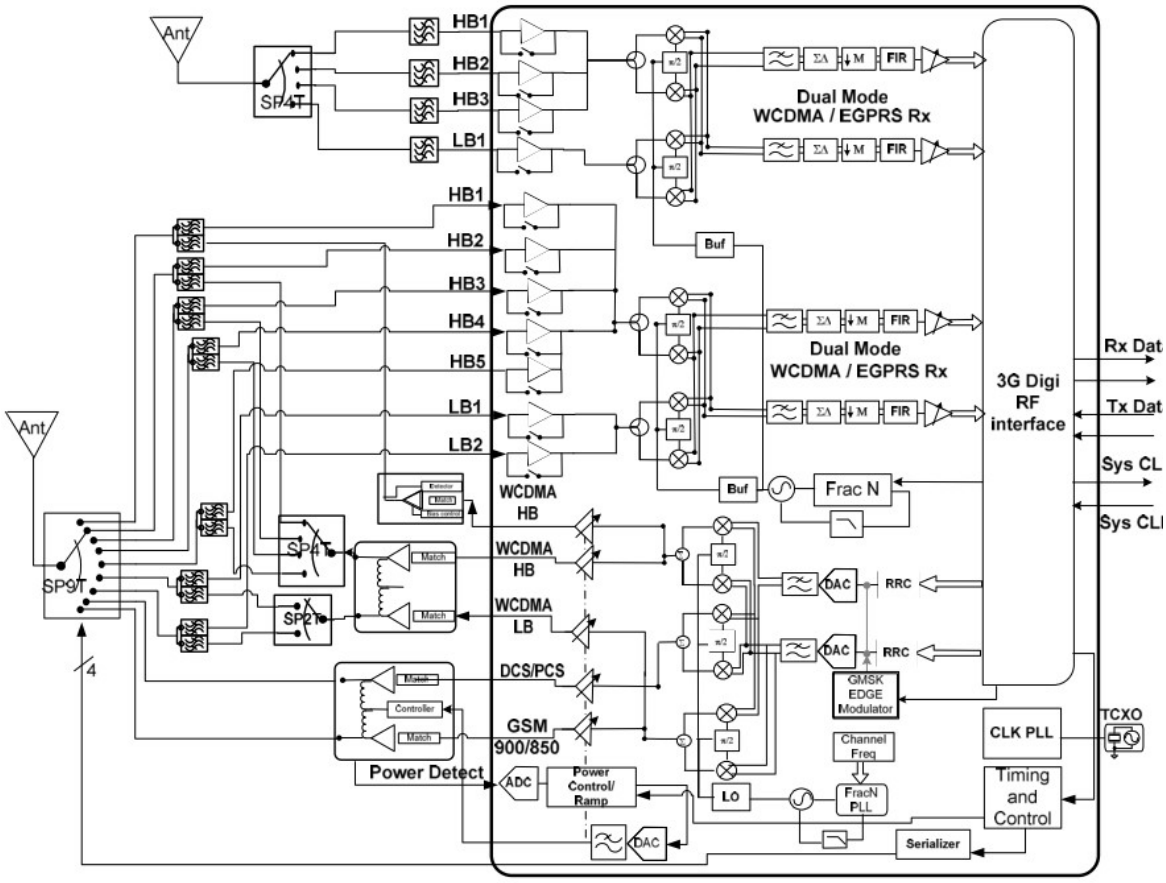


Figure 3-2 Block diagram of the multi-band single-chip transceiver presented in [2]

As advanced CMOS technologies are major drivers for digital signal processors, integrated radios have to deal with process scalability and major challenges of integrating radio-frequency (RF) functions into these digital intensive technologies [3]. In these technologies, the digital signal processing density scales with the technology, but performance and area of analog and RF components do not improve, and it becomes more difficult to meet the design specifications. Therefore, flexible RF front-end interfaces should rely primarily on digital-type circuits, while taking into account energy consumption, signal quality, and coexistence with other standards.

3.1.2. Switching to digital-intensive transmitters

a) Quadrature transmitters

In this context, there is a growing interest in digital-intensive RF transmitter solutions. Many topologies have emerged, from the simplest digital-to-RF converters to true digital

transmitters. This part offers an overview of each type of solution as well as the respective advantages and disadvantages.

A digital-to-RF converter (called DRFC, RF-DAC or DDRM in the literature) is a unique block that combines the digital-to-analog conversion and the upconverting mixing process. Such an architecture is shown in Figure 3-4(a). This greatly simplifies the implementation of the circuit and reduces the sources of non-linearity and noise. The main difference from traditional architectures is that the baseband low-pass filter needed to eliminate DAC replicas at multiples of the sampling rate is removed. This transfers the constraint to the output bandpass filter. A simple solution to the problem of the image is to oversample the digital signals and to digitally filter the images beforehand, as shown in Figure 3-4(a) with a factor M. The filters are well-known digital interpolation filters, in which there is a compromise between the quality of the signal in the band and the possible attenuation of the images. The oversampling process pushes the image replicas away from the carrier and attenuates them considerably, but the increase of the sampling rates entails a not insignificant cost, since the energy consumption increases linearly with the frequency of operation. Significant work has been done on the digital-to-RF conversion from Nokia, imec, MediaTek and Delft UT research groups [4]–[8] with DRFC resolution between 10 and 13 bits and moderate oversampling ratios.

To illustrate the image problem, Figure 3-3 details the output spectrum of the DRFC block when working at a f_S sample rate. The images are present in the spectrum at offsets equal to f_S around the carrier frequency f_C. They are attenuated by the frequency response of a zero-order hold (ZOH) function. Note that these images may be attenuated by other functions if a different output waveform is used in the digital-to-analog conversion process. The presence of images can be very troublesome for two reasons. First, adjacent and alternate channels of the same standard may be disturbed by close-band image replicas. This is exacerbated for broadband signals where attenuations are lower when f_S-f_0 approaches f_0. In [7], the implemented DRFC can handle channels up to 154 MHz wide. Nevertheless, the sampling frequency f_s is about 300 MHz. This involves high image levels that interfere with other channels. Secondly, other coexisting standards may suffer from out-of-band spurious emissions. For example, the coexistence of a Wi-Fi transmitter and a GPS receiver on the same chip represents a considerable challenge because the sensitivity levels of the GPS receiver are extremely low (< -174 dBm/Hz) and the Wi-Fi transmitter sends noise and spurs in these bands [9].

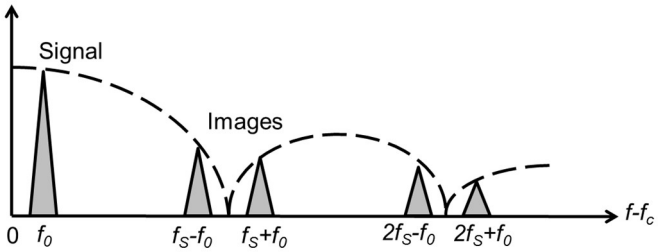


Figure 3-3 Single-sided spectrum of the signal at the output of the DRFC assuming zero-order hold (ZOH) behavior and with f_0, the center frequency of the signal, f_S the sampling clock frequency and f_C the carrier frequency of the local oscillator.

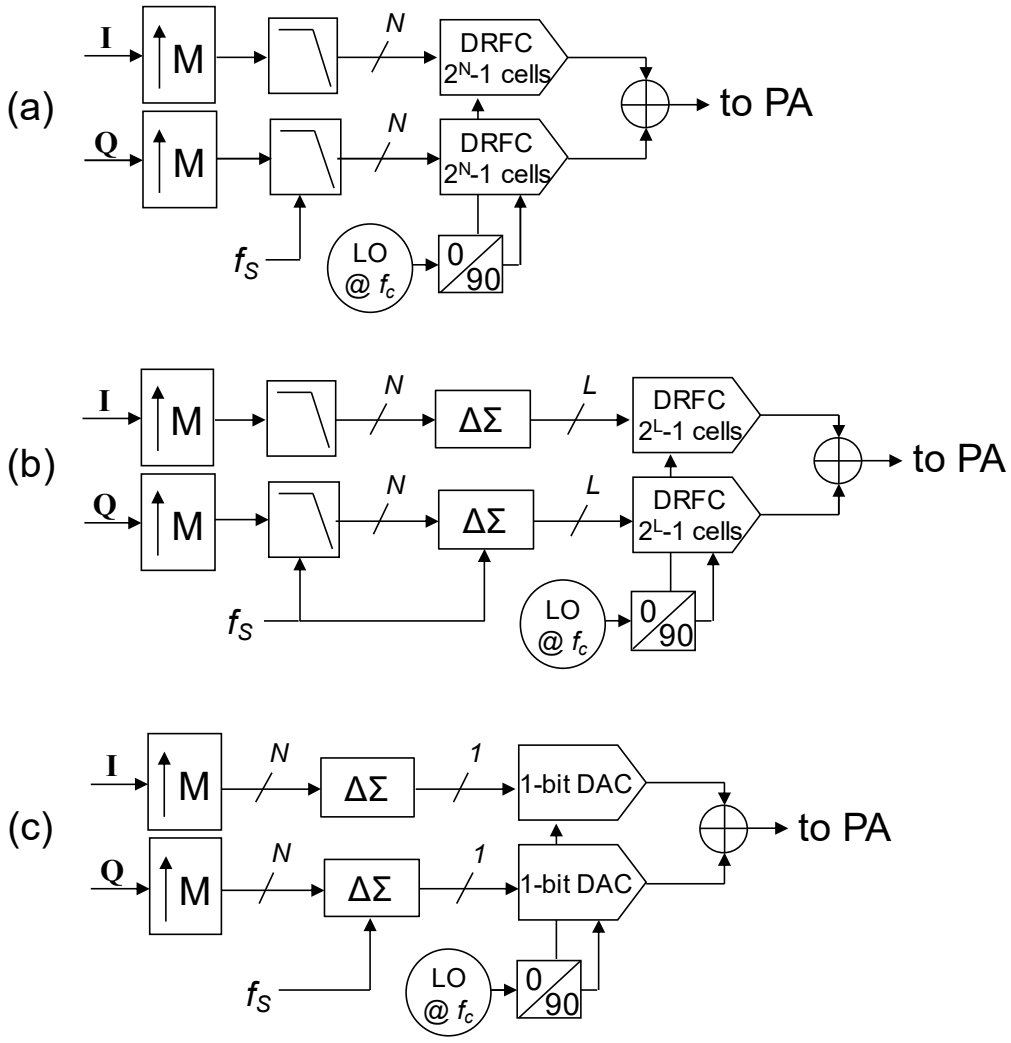


Figure 3-4 Comparison of different architectures for digital transmitters. (a) Oversampled DRFC requiring high-speed high-resolution DAC. (b) DRFC based on oversampled ΔΣ modulator with reduced resolution and shaped quantization noise (L<N). (c) Single-bit DAC based on oversampled single-bit ΔΣ modulator.

The design of high-resolution multi-bit linear digital-to-RF converters is a challenge and can be alleviated by reducing the number of bits from the converter to relax the linearity requirements. Since oversampling is mandatory for digital transmitters, ΔΣ modulation is a means of physically reducing the number of bits of the signal to be converted, while maintaining good performance and good resolution in a given bandwidth. In return, the quantization noise is increased outside this bandwidth. Thus, the ΔΣ modulation trades off linearity and flexibility for out-of-band quantization noise. This is sketched in Figure 3-4(b) and has been extensively explored by many groups in [10]–[18], with RF-DAC resolutions between 3 and 10 bits.

If the concept is pushed to the extreme case of single-bit ΔΣ modulators as in Figure 3-4(c), a highly digital implementation for the baseband can be considered, as well as the design of digital upconverting mixers and efficient switched power amplifiers. The input data I and Q are oversampled to f_S with a high oversampling ratio. It should be noted that the digital oversampling filter can be a simple ZOH process because the resulting images will in all cases be smaller than the quantization noise added by the ΔΣ modulation block. The data is quantized into a 1-bit high-speed data stream using low-pass ΔΣ modulation. The resulting spectrum contains the initial information in the given bandwidth and only shaped quantization noise outside this band. The upconversion of this digital signal to a carrier frequency f_C is performed by a digital image-reject mixer [19]. If this block is operated at 4 times f_C, its behavior is similar to that of a multiplexer between I and Q input streams, providing the output sequence {I, Q, -I, -Q}. The minus sign in this expression indicates the logical inverse of the I and Q 1-bit values. Note that there is an inherent integer relationship between f_C and f_S.

Another important aspect of providing a 1-bit digital RF signal to the power amplifier is to be able to increase the efficiency of the output stage. Switching mode PAs (such as class D) are known to provide very high efficiency [20]. An ideal class D PA has a 100% drain efficiency in the absence of conduction or switching losses. This becomes all the more relevant as the output power is high, as is the case for transmitters in base station applications, and thus the power consumption of the previous digital stages becomes negligible.

In early 2000, a research group at University of California at San Diego demonstrated the concept of bandpass ΔΣ modulation and class S amplification using a pattern generator and discrete NPN or FET transistors [21]–[23]. The first integrated demonstration in a 0.13 µm CMOS process was presented at ESSCIRC 2004 by researchers at the Helsinki University

of Technology [24]. The IC generated GSM and WCDMA signals at a sampling frequency of 700 MHz, reaching a carrier frequency of 175 MHz. In 2008, Arizona State University [25] showed a more complete system in 0.25 µm CMOS, including a 250 MS/s ΔΣ modulator and a digital-IF-to-RF converter based on an analog mixer and semi-digital filtering. Higher frequency of operation and larger bandwidths were obtained through investigations conducted as part of my Ph.D. works at the University of Lille in 2008 [26], [27]. I designed a 90 nm CMOS IC that generates RF modulated channels in a bandwidth of up to 50 MHz. The carrier frequency of these signals can be configured from 200 MHz to 3 GHz. Figure 3-5 shows an example of the output spectrum of such a digital RF signal generator. Nevertheless, the circuit is custom-designed in a 90 nm CMOS technology and the power budget is around 50 mW at full speed for the complete digital core. In more recent technologies, the ΔΣ modulator block can be designed using automated synthesis tools with a smaller power budget, as demonstrated in 2010 by Intel Labs in a 45 nm CMOS technology [28]. In 2016, researchers at Fudan University also integrated a single-bit ΔΣ-based digital modulator with a current-mode class-D power amplifier in a 65 nm CMOS process [29]. To complete the picture, NEC Corporation proposed an envelope ΔΣ modulation for the amplitude path and to multiply it digitally with a phase-modulated path, which can lead to a single-bit RF output with lower activity rate [30]. Apart from these works, no other significant circuit implementation has been reported for single-bit digital transmitters. Nevertheless, several proofs of concepts have been realized using FPGA and discrete components [31]–[33].

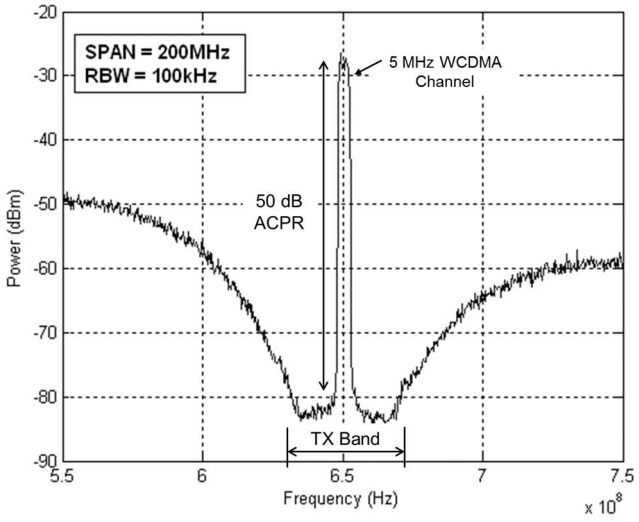


Figure 3-5 An example of a broadband output spectrum measured from a delta-sigma modulated 1-bit stream converted at a carrier frequency of 650 MHz. The channel is 5 MHz, while the total band is about 50 MHz. The adjacent channel power ratio (ACPR) is approximately 50 dB. We can clearly observe the shape of the noise provided by the delta-sigma modulators.

b) **Polar transmitters**

Significant work has also been done on polar transmitters, in which the signal is decomposed in phase and amplitude rather than in quadrature components. The digital phase signal is used to modulate a local oscillator that generates a square wave carrier. The amplitude path is either a multi-bit or quantized signal and, depending on the choice of implementation, modulates the supply of the digital PA, activates the corresponding number of cells, or is directly multiplied by the phase-modulated LO to provide bursts of bits to a switched mode PA. The circuits presented in [34] by KU Leuven and Infineon and [35] by KTH are very good examples of digital polar transmitters exploiting advanced CMOS technologies.

An advantage of polar modulators is the energy efficiency of the solution, especially when a switched-mode PA, such as class D or class E PAs, amplifies bursts of a square-wave phase-modulated carrier. However, polar modulators have certain disadvantages compared to quadrature transmitters. First, the bandwidths of the phase and amplitude signals are typically 3 to 6 times larger than the quadrature I and Q components, as shown in Figure 3-6, which poses problems for implementing the processing blocks. The recent CMOS technologies offer a high speed of operation of the transistors and contribute to the realization of efficient systems. Secondly, the processing in the amplitude and phase paths are essentially different, and it can be difficult to match their respective delays and synchronize the two paths when they are recombined. This limitation induces effects such as spectral regrowth [36] and raises architectural problems.

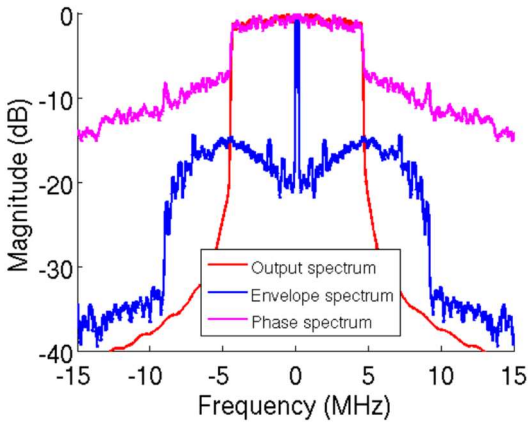


Figure 3-6 Envelope and phase spectra in polar representation

3.1.3. Challenges in digital RF transmitters

Examining the topologies in the previous section has shown some interesting potential for integrated digital transmitters, but challenges remain for creating robust, efficient, and

integrated digital RF transmitters. The main objective of this sub-section is to identify these challenges in order to position the work done in our group in the past 10 years in the study of potential solutions to overcome these challenges.

a) **High-speed operation**

Since most digital transmitter topologies require oversampling, they necessitate the use of high-speed operation of the digital logic. Fortunately, this is in line with the evolution of CMOS technologies and digital RF transmitters have a lot to gain from being integrated into very advanced nodes to benefit from speed and reduction of energy consumption per operation.

b) **Low voltage power supply in CMOS technology**

Advanced CMOS technologies offer supply voltages as low as 1 V. It is then very difficult to provide output powers in the order of 30 dBm, since this would require a low resistive load and a large current. Differential PA configurations are often used, as well as power combination schemes. This is probably the main limitation to extreme integration, since passive components such as inductors or transformers would often be needed.

c) **Out-of-band interference**

Flexible transmitters can produce and transmit data with many modulation schemes, data rates, carrier frequencies, and specific standards. They must comply with regulations on maximum emission in selected bands to allow the coexistence of several systems in the same neighborhood. This becomes particularly difficult with highly integrated digital transmitters because many spurious tones or noise are generated at the output. This includes spectral images and replicas, tones from clocks leaking from poorly isolated digital domains, or quantization noise produced by low-resolution coding schemes. Spurious out-of-band mitigation techniques take into account the reduction of all spurious and noises to an acceptable level or selective filtering in specific receive bands (such as very sensitive GPS bands).

3.2. High-speed digital operation

3.2.1. Generation of digital RF signals based on 1-bit delta-sigma modulation

As briefly described in the previous section, single-bit delta-sigma modulators push the digital-to-analog limit to the antenna. The advances and maturity of deep submicron CMOS technologies allow the DAC to achieve higher sample rates, reaching RF frequencies. Our team introduced the first 90 nm CMOS 1-bit ΔΣ RF signal generator suitable for integration into a complete transmitter chain [26]. A bandwidth of 50 MHz centered on 1 GHz can be obtained when the circuit is clocked at 4 GHz. Signals up to 3 GHz can be synthesized when using the first image band. The maximum output power into a differential 100 Ω load is 3.1 dBm with 53.6 dB SNDR. The digital core consumes 49 mW at the maximum clock rate. The active area is 0.15 mm^2. An overview of the signal generator chip is shown in Figure 3-7.

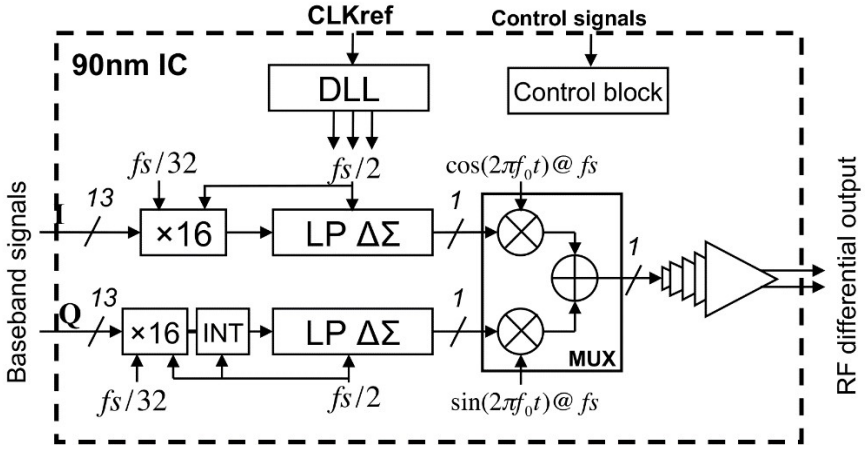


Figure 3-7 System view of the 1-bit ΔΣ RF signal generator (from [26])

After the off-chip baseband signal processing and the low-IF upconversion, the I and Q input channels are upsampled 16 times up to $f_s/2$. The ΔΣ modulators quantize the signals into 1-bit signals and shape the quantization noise with a third-order transfer function, including an optimized zeros placement. The 1-bit digital image-reject mixer replaces the conventional mixer and converts the I and Q signals into the desired RF carrier frequency before being pre-amplified by sized inverters. Note that a linear interpolation stage is inserted on the Q channel to reject the image channel.

The key innovation to achieve a clock frequency of 4 GHz is the development of a specific implementation of the core of the delta-sigma modulator. A redundant representation, named

borrow-save (BS), instead of the classical 2's complement representation has been proposed for the implementation of high-speed ΔΣ modulators [37]. This type of arithmetic allows additions without carry by simply calculating bit positions in parallel and saving carries in its representation, each bit position being doubled. Nevertheless, since output quantization cannot be easily calculated without reintroducing a carry propagation path, pre-computed non-exact quantization has been introduced. This output stage can be implemented with a digital (logic equations) or mixed-signal approach (sum of currents corresponding to the bit values). A patent covers the implementation of this type of architecture [38]. More details on the logical representation can be found in [37] or [39].

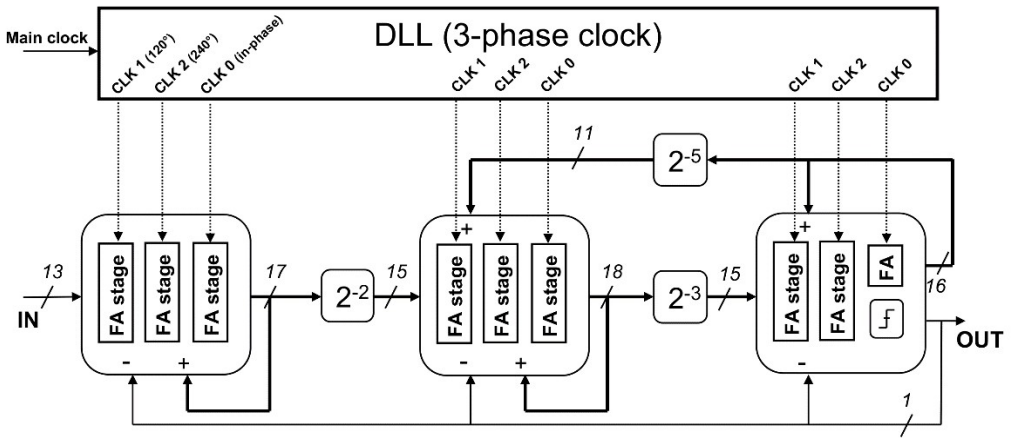


Figure 3-8 Third-order ΔΣ modulator with optimized zero placement (from [26])

A third-order 1-bit low-pass ΔΣ modulator with optimized zero placement was designed and successfully measured up to a sampling rate of 2 GS/s (Figure 3-8). It consists of 3 computation units, composed of 3 consecutive full-adder stages. To synchronize the operation, a 3-phase clock generated by a delay-locked loop (DLL) alternatively launches the calculation of each dynamic stage. A 90 nm CMOS integrated circuit, shown in Figure 3-9, was fabricated and tested to validate the concept. An SNDR of 72 dB over a bandwidth of 50 MHz was measured. However, the SNDR measured at the output of the chip degrades to 54 dB, due to the ringing of the supply voltage and the correlated jitter introduced into the output stage. This work is the first demonstration of a single-bit digital RF transmitter.

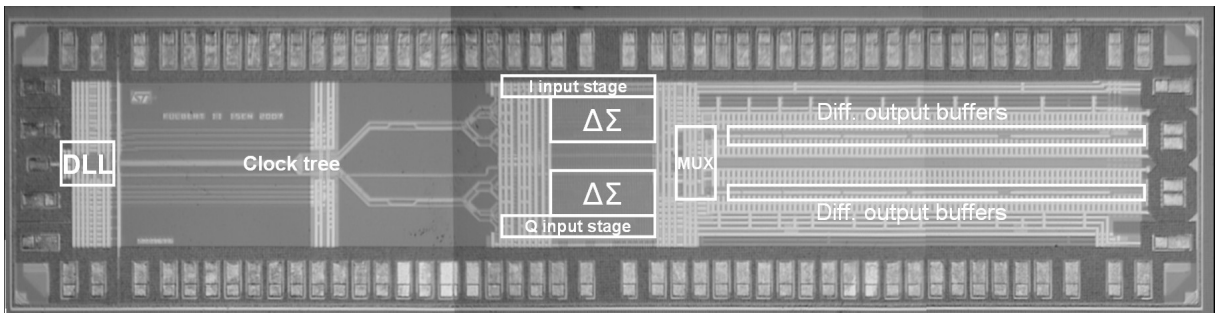


Figure 3-9 Integrated circuit microphotography of the 90 nm CMOS digital delta-sigma modulator (4 × 0.8 mm²)

As a result of this work, an ambitious collaborative project with Alcatel-Lucent focused on the use of baseband delta-sigma modulator for base stations. Some extracted performances describe the challenge. The system should offer instantaneous bandwidths of 200 MHz and modulated signals with high spectral quality (>70 dB ACLR and <6% EVM on the air). For low power consumption and heating problems, the spectral efficiency should be close to 90%. The proposed transmitter would consist of an FPGA generating digital baseband data at approximately 400 MS/s. It includes channeling, up-sampling and frequency shift. This signal is transmitted to a multi-chip module (MCM) built with a 4-bit 4 GS/s CMOS delta-sigma modulator and an RF PWM modulator and integrated drivers in InP technology, generating an output signal at 64 GS/s. Finally, a class S GaN power amplifier is integrated in another MCM with baluns and reconstruction filters. In this project, I supervised the development of the CMOS delta-sigma modulator chip.

A single-bit CMOS delta-sigma modulator cannot achieve the expected performance. Thus, a 4-bit solution has been proposed in conjunction with a digital PWM to transform this multi-bit signal into a 1-bit signal at a higher speed. Digital pre-distortion tables are integrated to achieve the targeted performance. Figure 3-10 shows the internal structure and the photograph of a 40 nm integrated circuit designed to produce a 4-bit high-speed data stream containing the modulated channels in a 500 MHz bandwidth. Design techniques, such as redundant arithmetic, are implemented to achieve GS/s operating frequencies. The circuit is fully functional up to an operating frequency of 8 GHz, that is, a 50 dB SNR is maintained in a 10 MHz bandwidth. The associated power consumption is shown in Figure 3-11. The circuit operates at a minimum voltage of 0.65 V at 3 GHz and 1.05 V for an 8 GHz clock. Measurements were made with a 50 MHz modulated channel and this shows that an ACPR of more than 53 dB is provided over a 500 MHz bandwidth (Figure 3-11). There is no publication associated with this work, but internal research and design reports have been produced as part of the collaboration with Alcatel-Lucent.

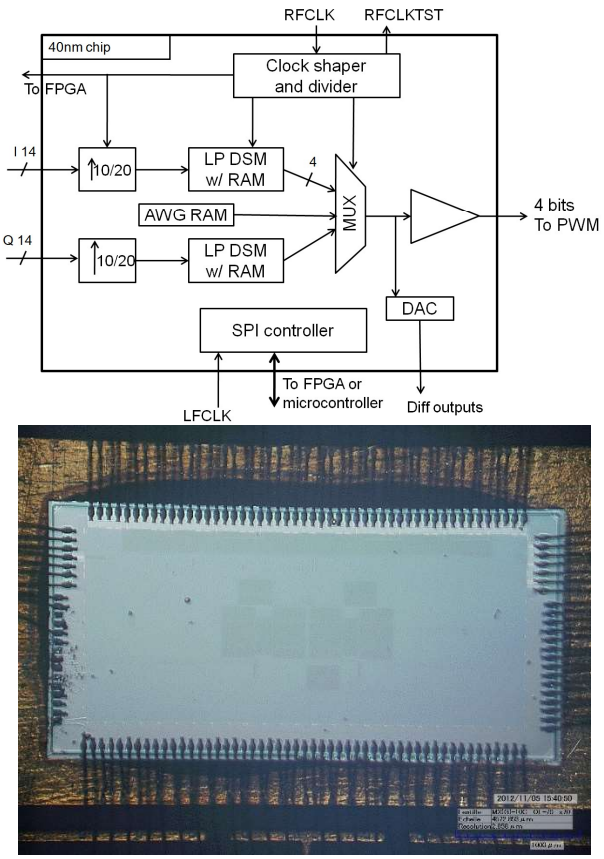


Figure 3-10 (left) Structure of the 40 nm integrated circuit based on 4th order ΔΣ modulators associated with the random access memories (for predistortion) (right) Microphotography of the 40 nm chip (4.2 × 2 mm²)

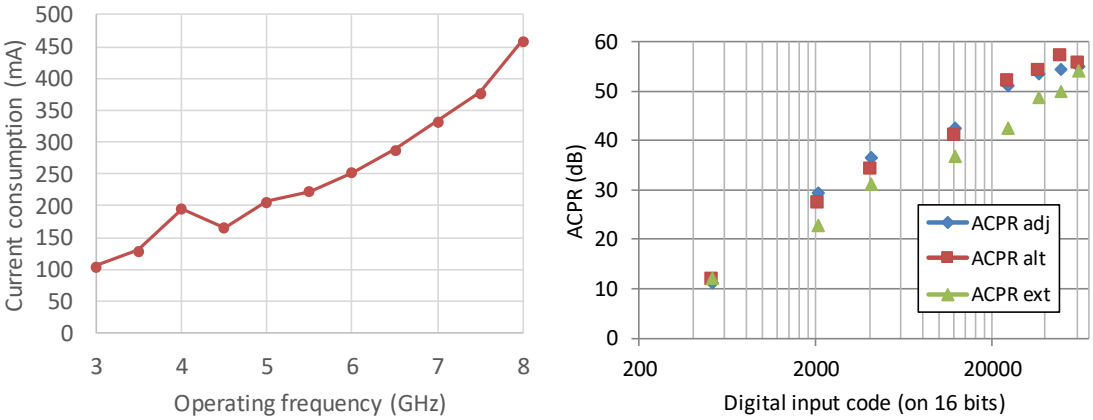


Figure 3-11 Measurement results of the integrated circuit: (left) Evaluation of the total consumption of the chip in relation to the operating frequency. For this plot, the VDD power supply is set at the minimum voltage that guarantees a measured SNR of 50 dB over a 10 MHz bandwidth; (right) Evaluation of the Adjacent Channel Power Ratio (ACPR) for a 50 MHz channel relative to the digital input code (directly related to the power of the output channel). The series represent the adjacent, alternate and extreme channel (measured at the edge of the 500 MHz total bandwidth).

3.2.2. Time-interleaving

A simple way to achieve a higher operating speed for the core of the digital processing is to parallelize the tasks in a time-interleaved (TI) pattern. This is not so obvious for delta-sigma modulators because internal states are stored in a structure that includes feedbacks. A solution has been presented in [28] on a 2nd order multi-stage noise shaping architecture (MASH) with 8 TI channels. This system operates at an effective sampling frequency of 2.5 GHz while consuming 6.9 mW. A thorough study of the critical path for a similar architecture is carried out in [40] in order to increase the sampling frequency up to 8 GHz, although the consumption is 10 times greater than in [28]. Nevertheless, the MASH architecture has a multi-bit output that requires the use of an additional Digital-to-Analog Converter (DAC) and does not allow the configurability of the bandwidth since all the zeros of the noise shaping function are on DC. Therefore, studies on error-feedback DSMs were conducted in the group by Cristian Marin and published in [41]. Time-interleaving methods in ΔΣ modulators (DSM) were compared in order to achieve a high sampling rate. These include a polyphase method [42] and a method based on node equations [43]. Careful analysis of the critical paths in error-feedback DSM revealed that the latter is more efficient, as illustrated in Figure 3-12. In addition, it has been demonstrated that a CIFB structure (cascade of integrators with feedbacks) leads to lower number of adders and computations in the critical path.

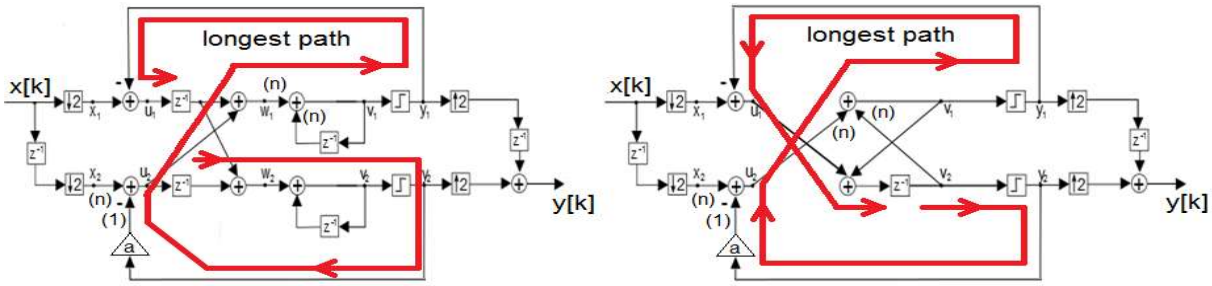
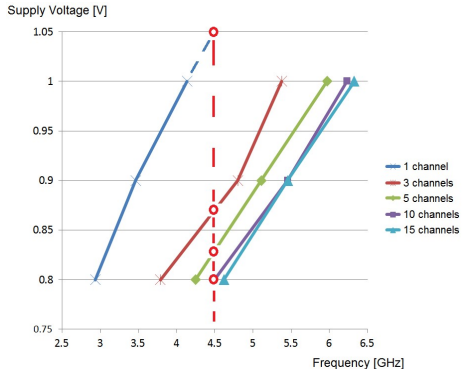


Figure 3-12 Evaluation of time-interleaved methods on a 1st order 2-channel DSM implementation: polyphase method (right) and node equation method (left)

Previous implementations of DSM in CMOS technologies have been custom-built to achieve high operating frequencies. With the availability of advanced CMOS technology nodes, such as the 28 nm FD-SOI, and time-interleaving techniques, it was interesting to consider automated synthesis tools. A 3rd-order CIFB DSM with configurable feedback was synthesized for different number of TI channels using STMicroelectronics 28 nm FD-SOI standard cells. The results presented in [41] were used to determine the maximum effective sampling frequency of modulators with respect to the supply voltage and number of TI

channels. This is shown in Figure 3-13. Increasing the number of TI-channels will allow for increased frequency operation, as the optimization introduced by the synthesizer may be more efficient for longer critical paths. For example, the maximum frequency for the 3-channel TI DSM is about 30% higher than its non-TI counterpart, which confirms the critical path study. However, increasing the number of TI channels above 10 does not improve the operating frequency while the complexity increases. In addition, if the application requires a lower operating frequency, time-interleaved modulators can operate at a reduced supply voltage to improve the power consumption. For example, in the case of a 10-channel TI DSM operating at 4.5 GHz, the supply voltage can be lowered to 0.8 V.

The power consumption compared to the number of TI channels for the operating frequency of 4.5 GHz and the different supply voltages is presented in the table of Figure 3-13. It can be seen that up to 5 channels, energy consumption remains around 6 to 7 mW, while a further increase in the number of channels will result in much higher energy consumption. Thus, a 5-channel TI DSM is an acceptable compromise for high-speed operation, low power consumption, and moderate silicon area.



TI-channels	Supply voltage	Power consumption	Total estimated Area
1	1.05 V	6.8 mW	1 700 µm²
3	0.9 V	7.4 mW	4 500 µm²
5	0.85 V	6.1 mW	6 400 µm²
10	0.8 V	9.6 mW	12 300 µm²
15	0.8 V	18.3 mW	17 600 µm²

Figure 3-13 (left) Frequency of operation versus supply voltage and number of time-interleaved channels for 3rd-order DSM synthesized in a 28 nm FD-SOI technology. (right) Minimum supply voltage, power consumption and estimated area for 4.5 GHz operation.

3.2.3. Up to higher sample rates (digital mmW transmitters)

Using the above techniques, addressing a bandwidth greater than 500 MHz is very difficult, given the oversampling ratio required for noise-shaping. In the evolution of mmW band communication standards, such as the 60 GHz band, the 2.5 GHz OFDM channels should be processed and generated. The use of digital-to-RF conversion (DRFC) concepts at mmW involves careful design of high-speed interpolation filters to avoid image replication. The work done by Jonathan Muller highlights a 4×-oversampled 18th-order 7-bit digital low-pass FIR up-sampling filter as shown in Figure 3-14 [44]. The up-sampling filter structure is

composed of two sections operating respectively at 5 GS/s and 10 GS/s. The design in a conventional 65 nm CMOS process relies on custom-designed complementary pass-transistor logic (CPL) and true single-phase clock flip-flops (TSPCFF).

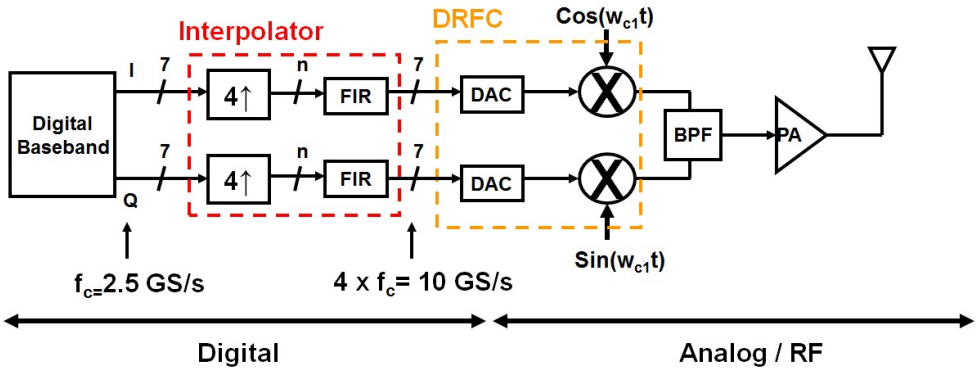


Figure 3-14 Architecture of the digital mmW transmitter proposed in [44].

The 65 nm CMOS chip prototype shown in Figure 3-15 was successfully measured up to an output frequency of 9.6 GS/s, which corresponds to the highest sampling frequency reported for a FIR filter at the date of publication of this work. In addition, the filter provides a bandwidth of 1.7 GHz and an attenuation of more than 40 dB at an offset frequency of 2.2 GHz, as shown in Figure 3-15.

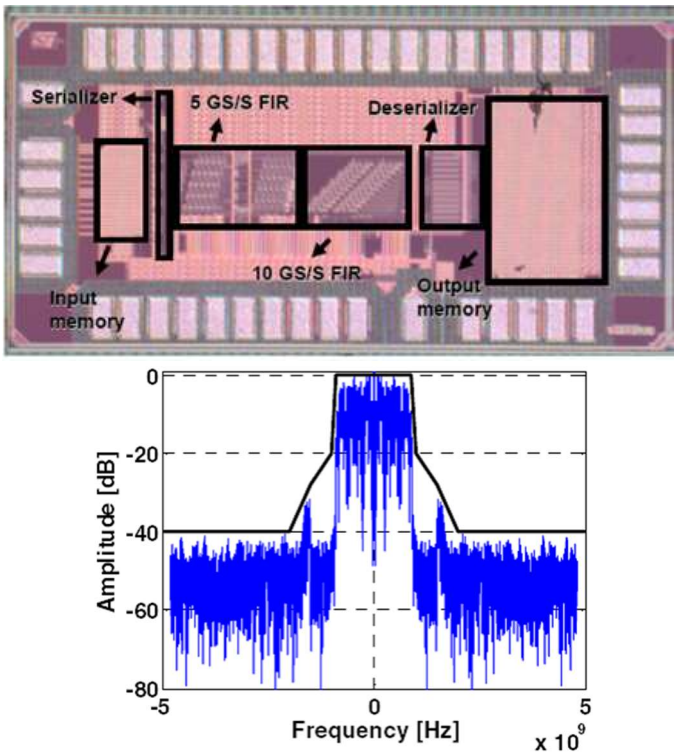


Figure 3-15 (left) 65 nm CMOS chip prototype. The dimensions are 1.5 x 0.9 mm². (right)1.7 GHz OFDM channel measured at the output. The attenuation provided by the integrated filter is greater than 40 dB and corresponds to the spectrum mask.

This work is an experiment of the very high-speed operation in CMOS and presents interesting conclusions. As can be seen for other high-speed circuits, operation up to a few GHz is compatible with the low power requirements of integrated systems. However, to operate at higher frequencies, we must pay the price of power consumption. This is illustrated in Figure 3-16, where the power consumption of the filter prototype is represented with respect to the operating frequency. The shape of the curve shows two sections. The left part is rather linear and is linked to an operation at 0.8 V. Above 4 GHz, there is a sharp increase in power consumption. This is due to an increase in the supply voltage to ensure error-free operation of the digital circuit. For example, in this demonstration, the supply voltage is increased to 1.4 V to achieve 9.6 GS/s operation. This needs to be taken into account during the design phase and poses some reliability issues, such as early physical degradation of the integrated system. It should be noted that the corner point is closely related to the technology and frequencies between 4 and 6 GHz can easily be obtained in more advanced technology nodes using automatic synthesis tools.

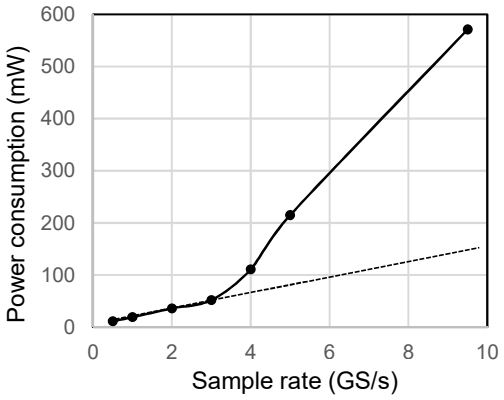


Figure 3-16 Power consumption of the 65 nm CMOS interpolation filter as a function of the output sampling frequency. The trend line shows the extrapolation of the consumption if the circuit operates at 0.8 V.

3.3. Output stage topologies for integrated transmitters

Small scale CMOS technologies allow very high-speed digital processing but are not suitable for mixed-signal and RF applications when power in the tens of dBm range is required. To illustrate this, Figure 3-17 shows the supply voltage and the optimal load when 30 dBm of output power is supplied to the load. The gate oxide becomes thinner and thinner and, as the breakdown voltage decreases, these technologies require lower supply voltages. The threshold voltage does not decrease in the same way, thus reducing the dynamic range at the output. Low impedance means high currents, which could also violate the electro-migration

rules of the process and complicate the design. The difficult question is how to generate power at very low output voltage.

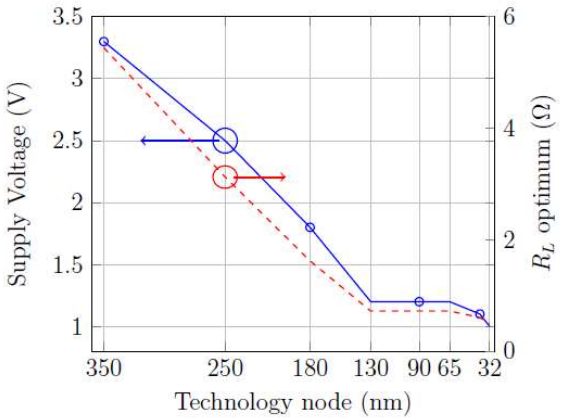


Figure 3-17 Evolution of supply voltage and optimum load when output power of 30 dBm is to be supplied (extracted from [45])

One of the possible solutions is to combine the generated outputs of several paths working in parallel. This can be done with elegance with transformers, especially for polar architectures [46]. This has been widely analyzed in the Ph.D. thesis of Arnaud Werquin [45] and I direct the reader to his manuscript for an in-depth view. Obviously, transformers integrated in dense CMOS nodes are impractical because of the large area required. Other techniques include (i) combining power with transmission lines [46], (ii) combining currents, as in current-steering DACs [47], or (iii) using switched-capacitor networks [48].

In the following subsections, the work done in the group will be detailed. The first subpart shows a power combining technique with discrete elements integrated in an IPD substrate, while a switched-capacitor power combining technique will be illustrated by the Cristian Marin's work on an integrated digital RF transmitter [49]. The current-steering approach will not be detailed here, but information on Fikre Gebreyohannes' work can be found in Section 3.4.4. It should be noted that the last two points (combination of currents and capacitors) are preferable in system architectures using a single-bit or low-resolution delta-sigma modulated signal, since this makes it possible to consider an appropriate switching scheme.

3.3.1. Power combination with passive networks

Switching-mode power amplifiers can theoretically achieve an efficiency of 100%. In a single-bit switching amplifier, the current is drawn from the power supply only for the signal components within the bandwidth, because the out-of-band components are rejected by the output bandpass filtering stage. The simplest voltage-mode switching power amplifier is a

simple CMOS inverter. This stage usually consists of a chain of CMOS inverters whose output can drive a low impedance load and behaves like an almost ideal voltage source (the resistance of the source can reach a few hundred mΩ depending on the last inverter width).

At low supply voltages, it is usually necessary to insert an impedance matching network between the power amplifier and the load to increase the output power. An alternative approach is to use multiple power amplifiers in parallel and combine the outputs in one way or another. For current output amplifiers, this is easily done by the sum of the currents on the output node. If voltage-mode amplifiers are used, the output power can be combined using transformers or transmission lines. Transformer-based techniques are mainly used because the ability to lower the impedance of these structures [50]. With respect to the transmission line-based power combination, the most common structure is the Wilkinson combiner which adds two signals so that their respective powers are added to the output node. Impedance transformation of transmission lines is, again, a key concept of power generation [51]. Note that the physical dimensions of the transmission lines are inversely proportional to their operating frequency, making them unsuitable for low frequency applications. However, at low frequencies, transmission lines can be replaced by equivalent stages of lumped element to save the chip area.

A network based on transmission lines has been proposed in [52] to combine the outputs of several inverter-based switching amplifiers. The power combiner consists of 5 channels driving a real load impedance RL, representing the antenna or the input of an antenna filter. This number of channels is limited only by the available area and can be extended to an N-channel configuration. In each channel a CMOS inverter drives a quarter-wavelength transmission line with a specific characteristic impedance. Figure 3-18 shows the topology of the 5-channel power combiner. The switched PAs are implemented in a 65 nm CMOS technology and the localized elements of the transmission line are integrated in an Integrated Passive Device (IPD) substrate, as shown in Figure 3-19. The output capacitance of the inverters and the value of inductance of the connection between the CMOS chip and the IPD were taken into account during the design of the LC networks. As will be described in a Section 3.4.4, the digital delay lines are used for implementing a finite impulse response (FIR) filter function on the combined signal.

We have demonstrated that there is a trade-off between power transfer and the rated output power by modifying the characteristic impedance of the transmission line depending on the application. Indeed, low characteristic impedance allows a high impedance transformation

ratio. When optimizing the power transfer (which tends towards unity thanks to a high characteristic impedance), power gain, defined as the ratio between output power delivered to the load when N channels are activated and the output power delivered to the load when 1 channel is activated, is a function of N^2, where N is the number of active channels. This can be seen in Figure 3-20, where 5 channels are activated, resulting in a power gain of 14dB. This is explained by the fact that N activated channels consist of N sources driving impedances N times smaller than the nominal impedance value. If output power has to be maximized, the power transfer decreases to 50% (ideal case) and the power gain remains a function of N^2. Special care must be taken to keep the output impedance of the inverter of the switched PA as low as possible. Ideally, these inverters represent short circuits, which turn into open circuits at the summing point, due to the quarter-wavelength transmission lines. This structure only works if the output impedance is very low, which keeps the transistors in the linear region. Otherwise, the output voltage would drop, and the impedance would become non-linear, which would degrade the power combination.

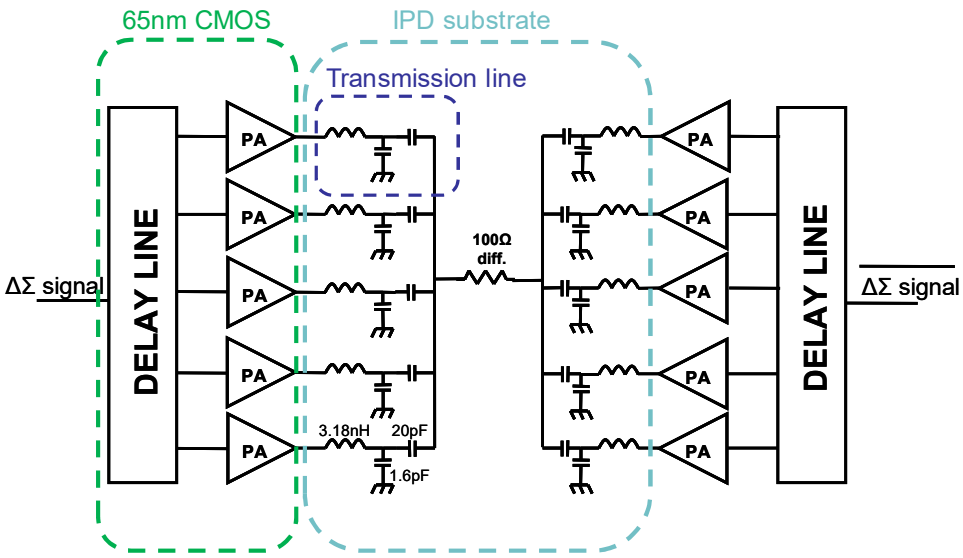


Figure 3-18 Architecture of the 5-channel power combiner, including digital delay lines.

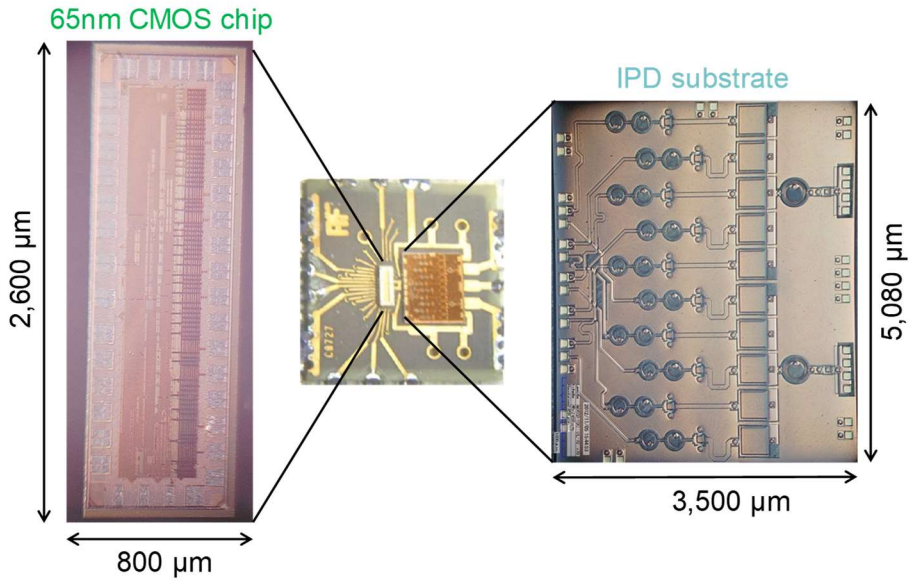


Figure 3-19 Assembly of 65 nm CMOS 5-channel switching amplifiers and transmission lines on IPD

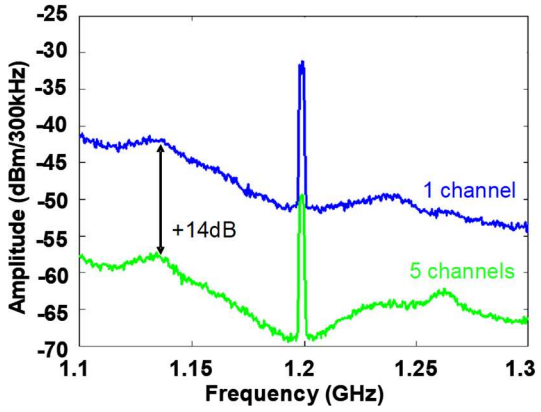


Figure 3-20 Spectrum of the modulated output of the circuits in the cases of 1 and 5 activated channels.

3.3.2. Switched-capacitor output stage

This subsection presents the concepts proposed by Cristian Marin during his doctoral thesis. Switching architectures based on low-resolution ΔΣ modulation (ΔΣM) [26], [53] have the potential to achieve high in-band performances and be effectively integrated into CMOS technologies, but they have to cope with significant out-of-band emissions that need to be mitigated to allow for the coexistence of different systems. This work proposes a hybrid digital transmitter architecture adapted to the GHz frequency bands. It combines a single-bit digital processing and a digital-to-RF mixer with 109-tap digital finite impulse response (FIR) filtering integrated into a pseudo-differential switched-capacitor (SC) RF digital-to-analog converter (DAC) implemented in 28nm FD-SOI CMOS technology.

The proposed all-digital RF transmitter architecture is illustrated in Figure 3-21. Two quadrature single-bit third-order ΔΣMs operate synchronously at twice the carrier frequency (f_c) while a digital-to-RF mixing stage (DRFM) operates at the final frequency of 4*f_c. Finally, the output is generated by a pseudo-differential SC RF DAC with integrated FIR filtering (FIR-DAC), and an RLC bandpass filter (BPF). The SC network in the output stage is based on a switching-mode (SM) class-D PA, as shown in Figure 3-22, while each unitary cell (switching element and capacitor) is used to create the coefficients of a digital 109-tap FIR filter. In addition, the capacitors used for switching are intrinsically part of an LC matching network at f_c, and serve two purposes, namely, digital-to-analog conversion and continuous-time filtering.

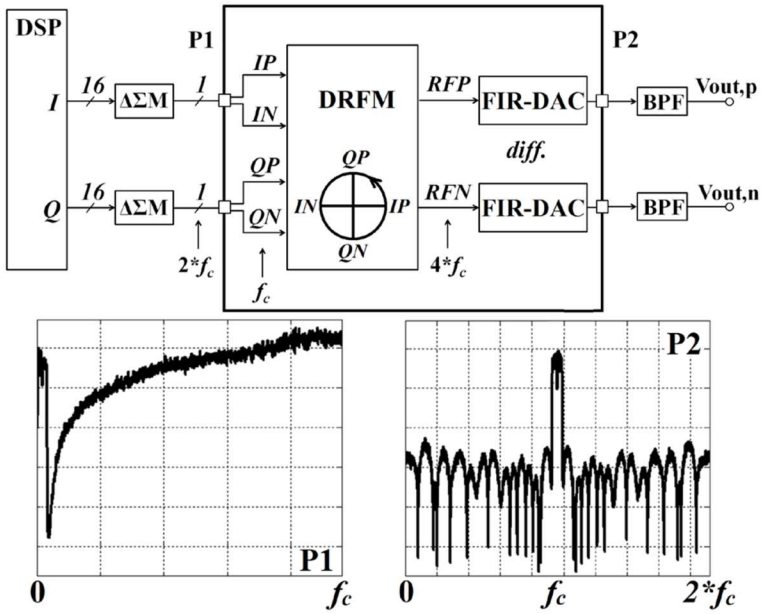


Figure 3-21 Proposed all-digital RF transmitter architecture and conceptual representation of the spectrum of the 1-bit digital input signal and the spectrum of the transmitter's analog output signal.

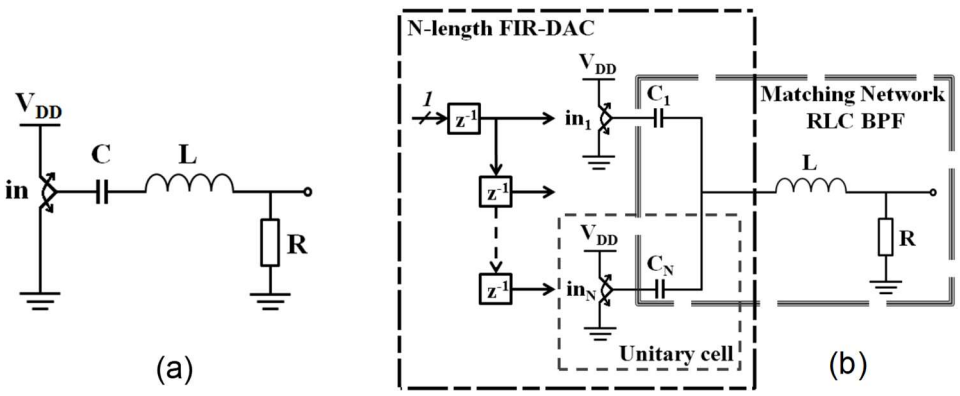


Figure 3-22 (a) Conceptual view of the switching cell (b) Proposed N-length FIR-DAC with class-D switching cells.

For the proposed application, the digital FIR filter should theoretically eliminate the out-of-band noise generated by the ΔΣM. However, such a filter requires a large number of high-

resolution coefficients and the integration of circuits becomes too complex. To facilitate integration, we proposed a two-step design optimization. First, the transfer function of the FIR filter is co-designed together with an output RLC bandpass filter, which reduces the coefficient quantization down to 5 bits. Second, we used the symmetry property of the FIR filter to suppress the unnecessary switching activity when the digital inputs to symmetric FIR coefficients RF_k and RF_{N-k+1} ($k = 1...54$) have opposite values. This is implemented with AND/NOR gates on the positive/negative sides of the FIR-DAC, resulting in a reduction in switching activity of about 20% and surface savings of about 50%. A notable consequence is that the three possible combinations of positive and negative drive signals result in a pseudo-differential configuration, which could lead to an increase in even-order harmonics due to the non-ideal differential to single mode conversion.

Full integration of the FIR-DAC under flip-chip (FC) RF pads is provided by a specific multi-layer structure in a 10 metal (Me) process, as shown in Figure 3-23. The unit cell occupies 1.6 x 1.8 µm^2 and includes a CMOS inverter built in Metal 1 (Me1), inter / intra-cell connections on Me2 to Me4, and a custom metal-oxide-metal (MOM) capacitor ($C_{MOM} \approx$ 1.7 fF) built on Me4 to Me8. The top plates of the capacitors are directly connected to the FC pad on Me10 and Alucap. Finally, the FIR-DAC has a total of 1152 unit cells, divided into a 32 by 36 matrix to fit under the FC pad.

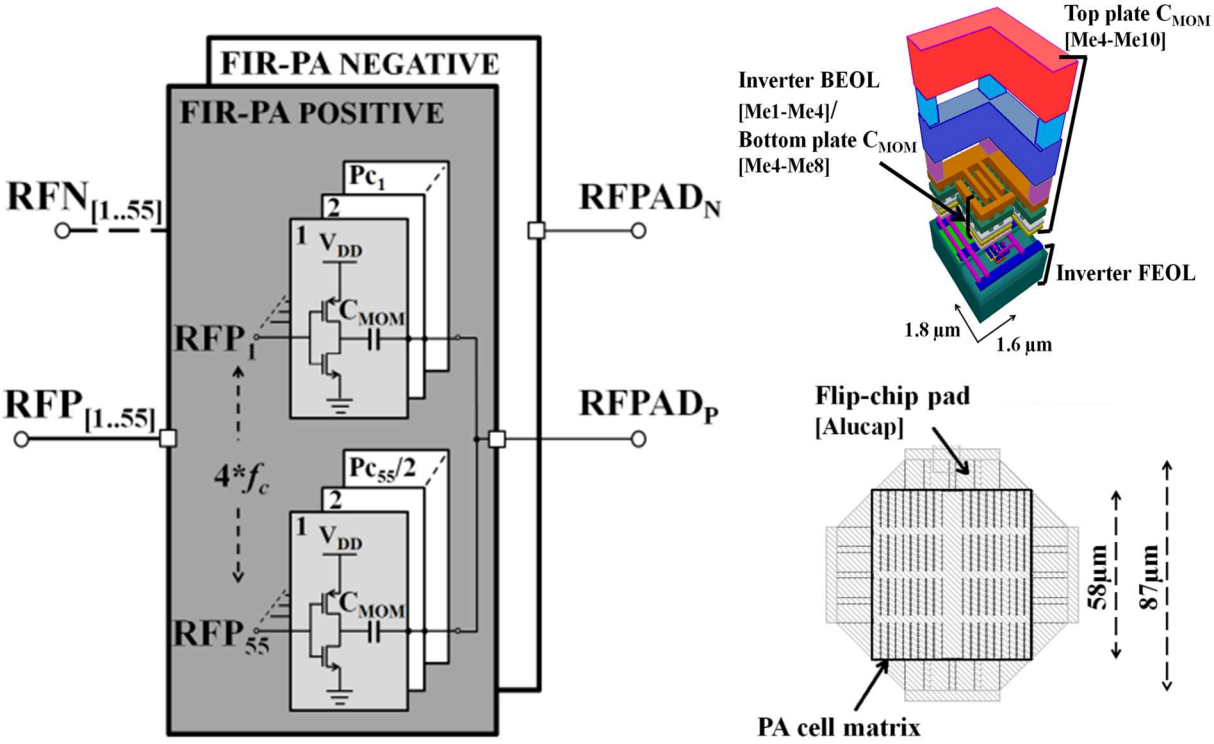


Figure 3-23 FIR-DAC implementation: schematic, unit cell (3D GDSII View) and RF pad integration.

The proposed circuit was manufactured in 28 nm FD-SOI CMOS and incorporates DRFM and SC FIR-DAC, with a total active area of 0.047mm^2 (Figure 3-24). The integrated circuit is mounted on a dedicated 5 x 5 mm^2 FC Ball Grid Array (BGA) which integrates RF inductors to create the LC matching network and decoupling capacitors.

In Figure 3-25, the measured output spectrum of a 3 MHz baseband (BB) tone at 6 dB of back-off related to the maximum output power of 4.6 dBm highlights the out-of-band attenuation provided by the FIR and RLC filtering. The carrier frequency is 900 MHz and the voltage supply is set to 1 V for an overall power consumption of 34.5 mW, with 8.3 mW for the front-end and 26.2 mW for the back-end, respectively.

In terms of out-of-band noise, it is found that the proposed architecture reaches -60 to -70 dBc at an offset frequency of -fc/3 = -300 MHz, when transmitting at the center frequency fc = 900 MHz, which is consistent with the study of the system for the given output power. In addition, the signal-to-noise ratio in the band (100 MHz) is about 61 dB, which corresponds to 10 effective number of bits (ENOB).

Furthermore, the FD-SOI body-biasing V_t tuning function, described in [54], has been used in the digital-to-RF mixer to adjust the operation of the CMOS transistors and reduce the non-idealities of switching, thus allowing additional control to balance the PMOS and NMOS switching and to find an optimal operating point. Thus, an improvement of the LO and image rejections was obtained to reach ~60 dBc.

The output power and ACLR performance for the transmitted LTE 10MHz (LTE10) and 20MHz (LTE20) signals are evaluated in Figure 3-26, highlighting the conformance of the spectral mask. The maximum output power and ACLR for LTE10 are -1.2 dBm and -33 / -43 dBc, while for LTE20 we have obtained -1.5 dBm and -34 / -43 dBc, respectively. The total power consumption is approximately 38 mW when the supply voltage is 1 V.

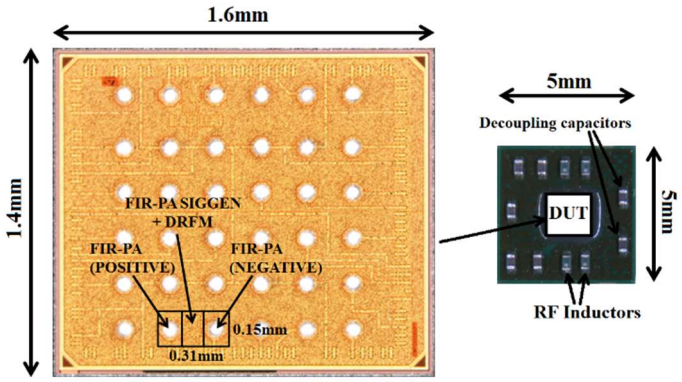


Figure 3-24 Microchip and flip-chip IC mounted on a BGA housing cavity. The cavity also includes SMD inductors and decoupling capacitors.

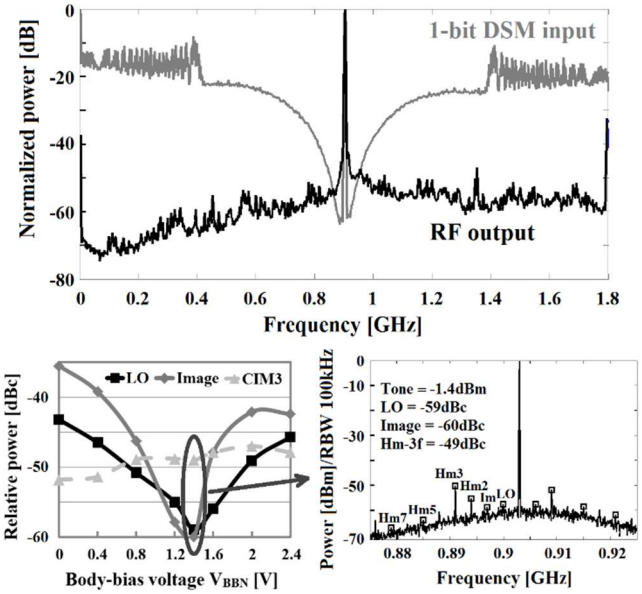


Figure 3-25 Spectrum measured for a 3 MHz BB tone at 6 dB back-off and evolution of LO leakage, image rejection and CIM3 relative to the FD-SOI body-bias voltage.

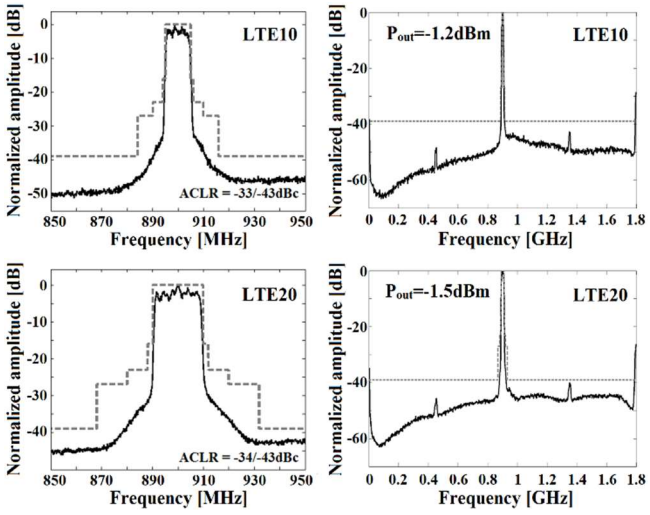


Figure 3-26 Spectra measured for the 10MHz and 20MHz LTE channels

	[Jin JSSC 17]	[Roverato JSSC 17]	[Paro Filho ISSCC 2016]		This work	
Architecture	Quadrature DRFC	10b ΔΣ + Mismatch Shaping 10b DAC	RQDAC + passive mixer		Digital Mixer + SC FIR-PA	
Carrier Frequency [MHz]	800	900	900	2400	900	
Supply voltage [V] Front-end / Back-end	1.1 / 1.1	1.5 / 0.9	0.9 / 1.1		1 / 1	
DAC Resolution [bits]	6 (physical)	10 (physical)	12 (physical)		1 (10 ENOB)	
Peak P_{out} [dBm]	13.9	1.2	3.5		4.6	
LO feedthrough [dBc]	-	-61	< -57		-59	
Image [dBc]	-	-36	< -42		-60	
CIM3 [dBc]	-	-67	< -50		-49	
Modulation signal	LTE10	LTE20	20MHz		LTE10	LTE20
Average P_{out} [dBm]	6.97	0.9	-3.5		-1.2	-1.5
ACLR [dBc]	-32.4 / -34.9	-60.7 / -61.6	-42 / -59	-47 / -59	-33 / -43	-34 / -43
Consumption [mW] Front-end / Back-end	CW: 60.7 / - LTE: 17.1 / -	LTE20: 75 / 22 (w/o ΔΣ)	20MHz: 11.1 / -	20MHz: 24.8 / -	CW: 12.3 / 26 LTE: 8.8 / 29	
Active area [mm²]	0.24	0.82	0.22		0.047	
Matching network	Off-chip	On-Chip	Off-chip		On BGA	
Technology	28nm	28nm	28nm		28nm FD-SOI	

Figure 3-27 Summary of performances and comparison with state-of-the-art ([55]–[57])

The performance of the 28nm FD-SOI RF transmission chain is summarized and compared with the digital-intensive architectures of Figure 3-27. At similar output power levels, the FIR-DAC (at 1 V) consumes 7 times less power than a 10-bit DSM-based DAC (at 1.5V) [56] and 25% less than a resistive 12-bit DAC (at 0.9V) [57]. The total active area is at least 4 times smaller than the previous smallest design, for the same technology node. Therefore, this work is characterized by low power consumption due to the single-bit core solution combined with band filtering and the low area obtained with a multi-layer FIR-DAC cell structure. It shows the transition from traditional analog transmitters to highly integrated, digital-intensive transmitters that target the future of mobile applications.

3.4. Out-of-band interference

This subsection deals with the management of spurious emissions, showing some investigations and ideas for properly sending a dedicated channel and not polluting the entire spectrum. There are two major contributions to spurious emissions that are concerned here. First, when a DRFC system is used, the sampling frequency of the baseband is generally moderately greater than the bandwidth, and replicas at multiples of the sampling frequency

are present in the spectrum. They are filtered only by the sinc function associated with the zero-order-hold at the output. This is particularly detrimental when broadband channels are taken into account. The first subsection presents a technique for attenuating images resulting from the digital-to-analog conversion using a multi-rate approach. The second out-of-band contribution is the quantization noise in systems where delta-sigma modulation is used. As noted in the previous sections, coexistence should be maintained, and the noise produced should be limited in specific bands. The following sections present several techniques to solve this problem, including experiments with BAW filtering, engineering of noise transfer functions, and study of integrated FIR-DAC approaches.

3.4.1. Multi-rate PA

We proposed to develop multi-rate systems in [58] to reduce spurious emissions due to image replicas without increasing the oversampling rate. Polar power amplifiers with digitally-controlled envelope (digital power amplifiers, DPA) are used in a power combination system to meet LTE standards. These power amplifiers function as digital-to-analog converters without filtering the image replicas for the amplitude path. The proposed improvement is to use different sampling rates (ideally in a non-integer ratio) for different paths as shown in Figure 3-28. This technique is effective so that the sampling images do not recombine, thus spreading their energy as illustrated in the spectrum measured in Figure 3-39. In this graph, the output spectrum of a 2-path system operating at different speeds is shown and compared to the same system but with an equal frequency for both paths. We can observe the split of the original image into 2 spurs of lower power. It should be noted that the useful signal constructively recombines. To demonstrate this concept, a 65 nm CMOS chip, comprising two DPAs, was designed and manufactured (Figure 3-30). This proof of concept can be extended to N-path structures, further increasing the supplied attenuation with a factor of $10 \cdot log$ (N).

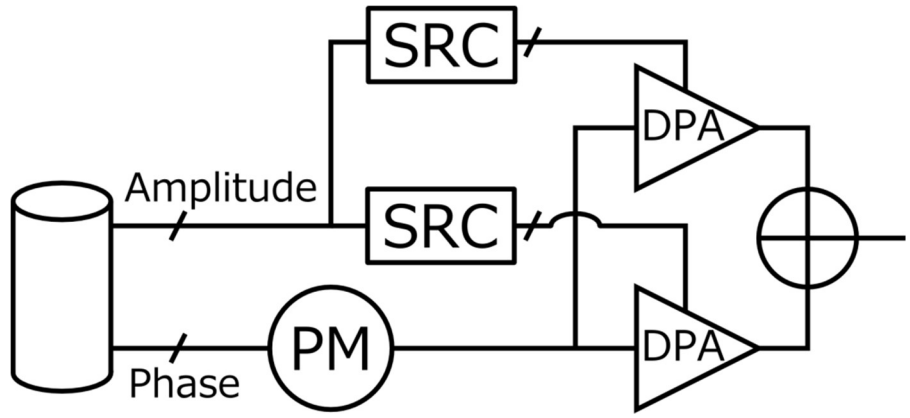


Figure 3-28 Block diagram of the proposed multi-rate digital power amplifier

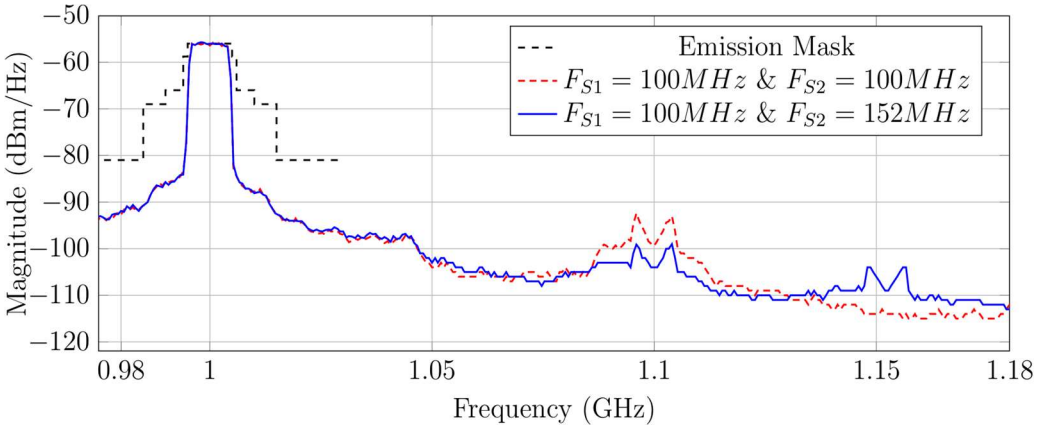


Figure 3-29 Measured output spectrum of a 2-channel 10 MHz LTE digital polar power amplifier with and without multi-rate paths (from [58]).

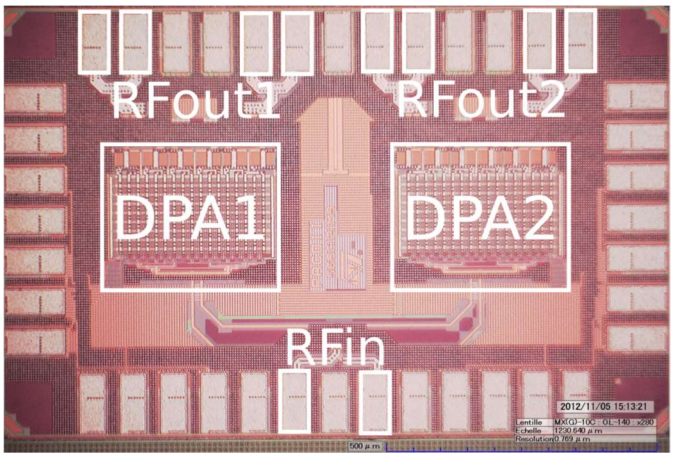


Figure 3-30 65 nm CMOS chip prototype for multi-rate DPA. The total area is 1.27 x 0.82 mm²

3.4.2. Analog BAW filtering

One possible solution for suppressing excessive out-of-band noise is to implement strong analog filtering using, for example, bulk acoustic wave (BAW) filters [59]. The designed BAW filters combine the advantages of the sharp passband-to-stopband transition of a ladder structure with the excellent stop-band rejection and low insertion losses of a lattice structure.

These filters provide high out-of-band attenuation and can be used as duplexers for frequency division duplex (FDD) standards, such as 3G UMTS. The other advantages of BAW technology are power handling and compatibility with Silicon processes. They are therefore ideally suited to provide the required attenuation of out-of-band quantization noise produced by delta-sigma modulators, when used in a lattice-ladder configuration.

a) Demonstration of quantization noise filtering

In the framework of the European project MOBILIS, BAW filters were studied [59] and tested together with the ΔΣ RF signal generator presented in Section 3.2.1. They were assembled on a tiny module, which is then mounted on a larger printed circuit board shown on Figure 3-31 [60]. The BAW filters were intended for the European UMTS 3G network, with a center frequency of 1.95 GHz and a bandwidth of 60 MHz. In order to demonstrate the filtering capabilities with a ΔΣ-modulated RF signal, the digital signal generator has been used in a mode in which the first image band is used in place of the fundamental frequency. In fact, the master clock frequency was set at 2.6 GHz, which led to a fundamental frequency of 650 MHz and a first image band around 1.95 GHz. This was done to demonstrate the functionality, but obviously the output power is greatly reduced by about 10 dB due to the attenuation of the sinc function at ¾ of the sampling frequency. The output spectrum of the ΔΣ RF chip is shown in the right part of Figure 3-31, in which we can see the fundamental band as well as the image band and the notch from the sinc function at 2.6GHz.

The matching network between the ΔΣ RF chip and the BAW filter is also made very simple. The output impedance of the ΔΣ RF chip is very low because the output is connected to wide inverters, while the BAW filter must see a diff. 50Ω impedance. Two 25Ω resistors were inserted between the two modules for demonstration purposes.

The measurement results show that the quantization noise near the band of interest was reduced below the noise level of the spectrum analyzer in this configuration, thus taking advantage of the high rejection of the BAW filter in the near-band. The far-band filtering is also effective. In the first image band, the measured ACLRs are 43 and 42 dB, respectively at offsets of 5 MHz and 10 MHz. The EVM is 3.7% and the measured channel power is -27 dBm (this low value is due to the use of the first image band and the loss in the series resistors). The following section will discuss the use of these circuits in a complete transmitter.

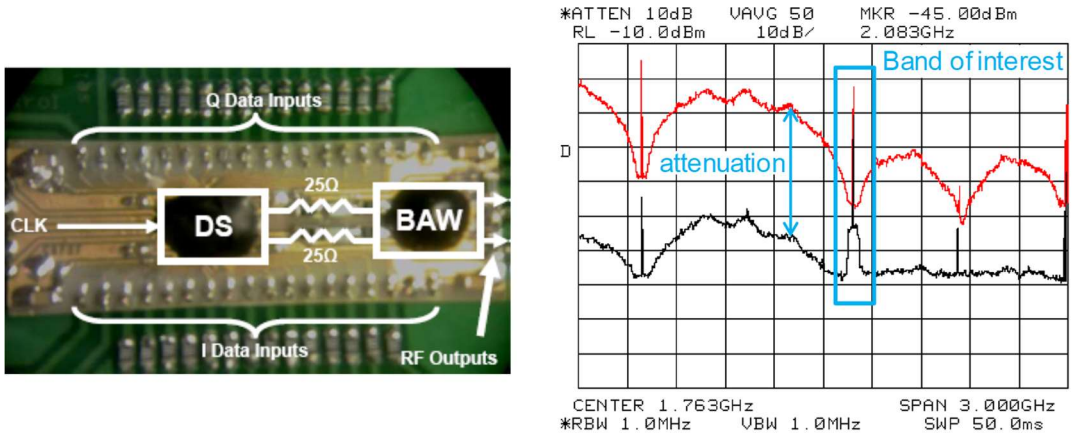


Figure 3-31 (left) Detail of the module carrying the ΔΣ RF signal generator and the medium-power BAW filter. (right) Output spectrum of the ΔΣ signal generator before and after BAW filtering.

b) Transmitter experiment with BAW filters and duplexers

In this proof of concept, the module presented in the previous subsection is coupled to a BiCMOS7RF power amplifier and a BAW duplexer, dedicated to filtering around the UMTS TX band and isolating the UMTS RX band (Figure 3-32). All these blocks were designed by partners of the European project MOBILIS [61]. The B7RF power amplifier has a gain of 10 dB and an output compression point of 27.5 dBm. The pre-power amplifier is an ad-hoc instrumentation amplifier, showing a gain of 30 dB around 2 GHz in a single-ended configuration. Its input power is 0 dBm and its very high output compression point does not degrade the overall linearity. This instrumentation amplifier is used to compensate for the low output channel power at the output of the ΔΣ signal generator module and the low gain of the output power amplifier.

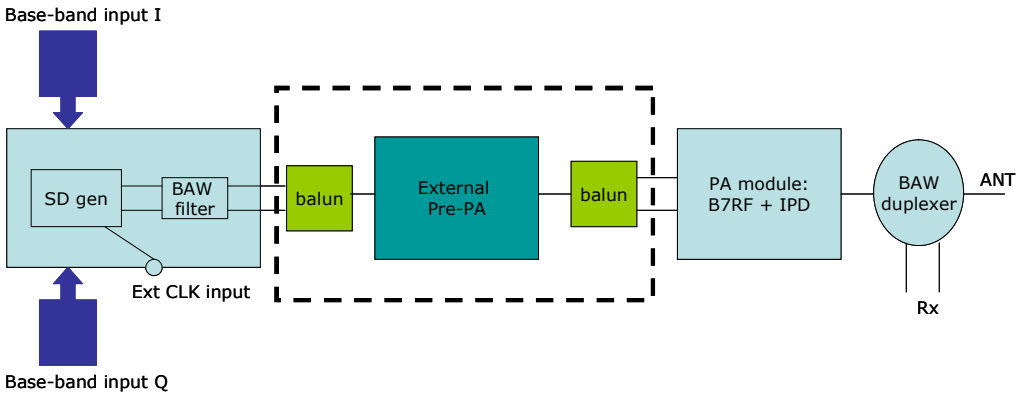


Figure 3-32 Test setup for the demonstration of a complete transmitter concept with external preamplifier

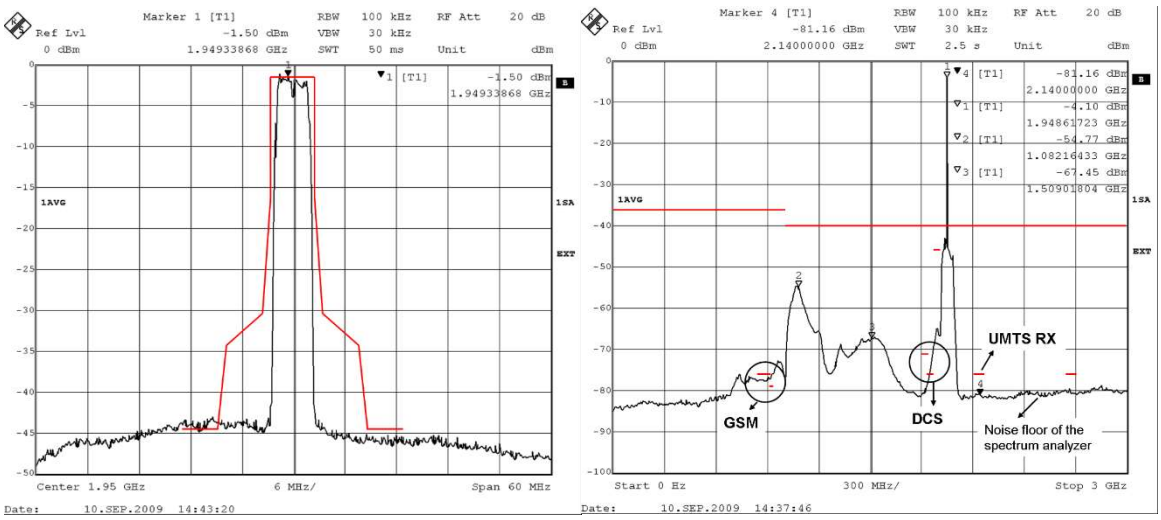


Figure 3-33 Output spectrum of the complete transmitter. (left) Zoom on the bandwidth and (right) full span.

The measurements of this transmitter are shown in Figure 3-33 with the standard emission mask for WCDMA, indicated in red for the global and specific bands (GSM, DCS, UMTS RX). The in-band emission meets the UMTS requirements and the measured ACLR are 42.5 dB and 44.5 dB, respectively for the 5 and 10 MHz offsets. The standard defines minimum ACLR as 33 and 43dB respectively. The measured EVM is less than 5%, well below the required 17.5% of the UMTS standard. The channel output power is 14.5 dBm. It can be seen that the system is compliant with regard to spurious emissions in most frequency bands and in particular in the constrained UMTS RX band. Nevertheless, the level of spurious emissions within the DCS and GSM bands is at the limit of what is required and needs further optimization.

3.4.3. Engineering of the Noise Transfer Function (NTF)

a) Complex noise transfer function

Another step towards the configurability and flexibility of the transmission chain is the ability to adapt the architecture to the chosen standard, especially to meet out-of-band noise requirements. These requirements depend on the application context and it is desirable to build a structure capable of reducing the noise generated at defined frequencies. To do this, we can design the noise transfer function of the delta-sigma modulator and introduce out-of-band notches by including a feedback in the architecture [62]. This is elegant but provides symmetrical notches around the center carrier frequency. In a quadrature modulator, it is therefore possible to create a complex transfer function, thus positioning independent notches on the left or right sides of the center frequency. To illustrate this, consider the first

order structure of Figure 3-34. Cross-coupling the quadrature paths, the frequency of the transmission zero then depends on the coefficients r and c [63]. This was implemented in [64] to create a 5th order delta-sigma modulator with optimized in-band zeros (placed at the edge of the transmission band) and two extra zeros placed on the DCS and UMTS RX sensitive bands (Figure 3-35).

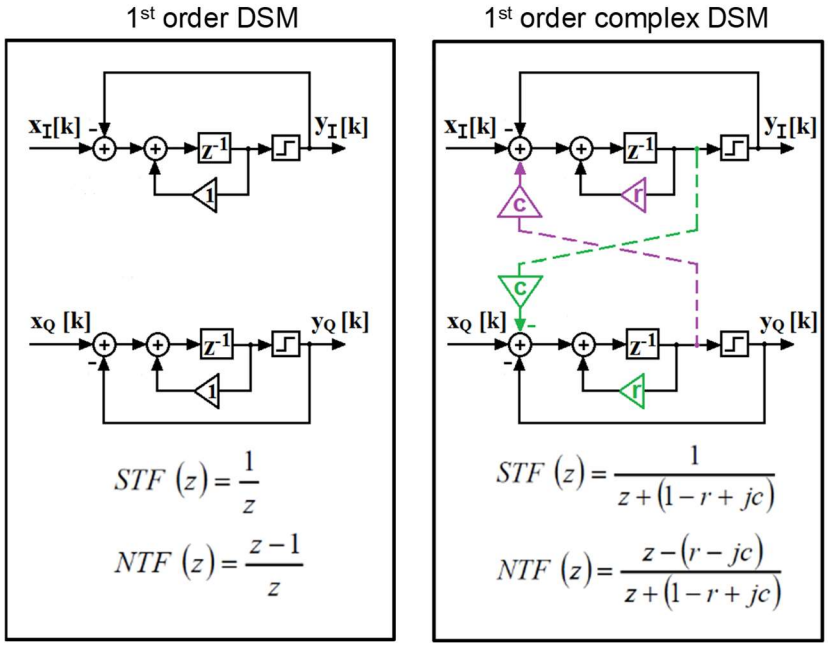


Figure 3-34 Description of a first order quadrature delta-sigma modulator (DSM) and additional cross-couplings required to build a complex DSM.

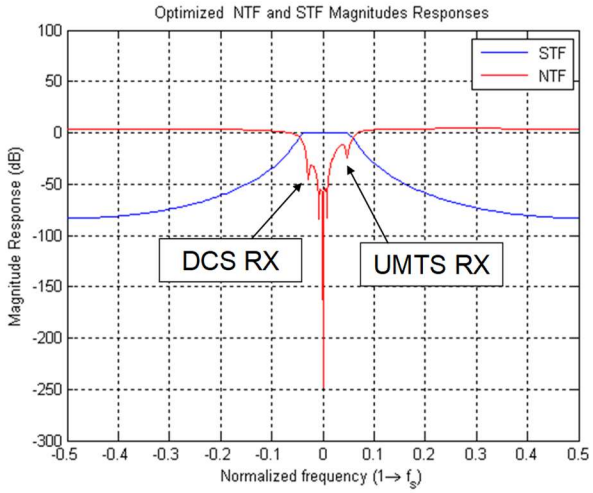
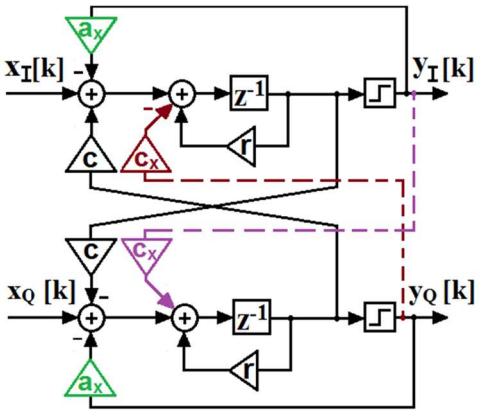


Figure 3-35 Example of signal and noise transfer functions of a fifth-order ΔΣ modulator with optimized zero positioning.

The configurability of the position of the notches allows a flexible architecture adapted to software defined radio systems. However, defining coefficients to create correct signal and noise transfer functions while ensuring stability in all conditions is a very delicate task and cannot rely on traditional generation tools such as the MATLAB Delta-Sigma Toolbox from R. Schreier for high-level design and simulation of delta-sigma modulators [65]. In view of

the above, the methodology presented in [63] proposes to include additional cross-couplings to restrict the dependence of the NTF numerator on r and c, as explained in Figure 3-36. The tools can now be used to optimize the intra-band properties of the modulator and the final stages will be integrated using the proposed cross-coupling scheme. This is illustrated in Figure 3-37, in which a 4th order delta-sigma modulator is created with automatic tools, then a stage is included to selectively create a notch in the GPS band or 3G RX band. Note that this is a preliminary step to reduce out-of-band noise, and that additional filtering is relaxed but still required. It has also been shown that this architecture allows coarse placement of the notch frequency with delays as well as precise placement using coefficient values, allowing a notch to be placed almost anywhere in the spectrum.



$$STF(z) = \frac{1}{z}$$

$$NTF(z) = \frac{z - (r - jc)}{z}$$

Figure 3-36 Cross-coupling technique proposed to create a 1st-order complex delta-sigma modulator

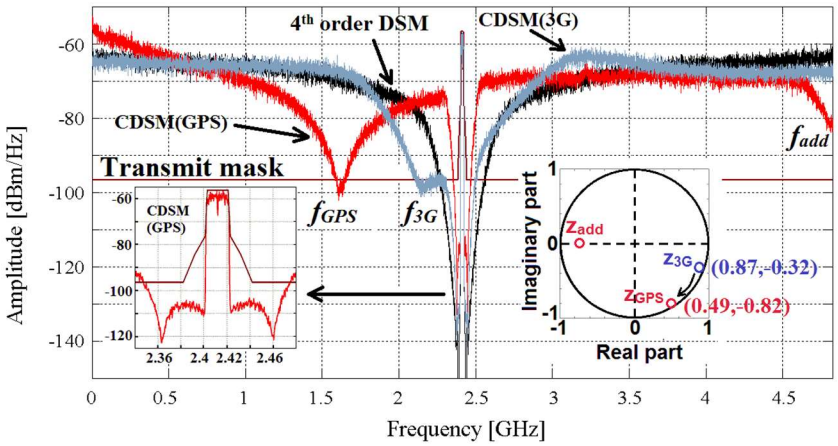


Figure 3-37 An illustration of a 4th order DSM and complex DSMs with specific notches placed in the GPS or 3G reception bands.

b) RF digital mixing with integrated FIR filter

Potential problems with the previous proposition arise when output stages are used to convert the 1-bit digital output signal into the analog world. Any discrepancy or mismatch on the

voltage or time references introduces a background noise that blurs the notches created in the transfer function. It is then necessary to take this into account during the design of the output stages. Alternatively, we proposed in [66] to integrate a FIR filter with a single tap directly on the digital output stage in order to create a specific notch during the recombination. This concept has already been used in [12] with 2 RFDACs, whose inputs are delayed. By construction, this notch will be deep and very tolerant to any noise or mismatch in the output stages. In the proposed implementation, a 1.5-bit digital output signal can be created as the sum of a single-bit delta-sigma output and a delayed version, as shown in Figure 3-38. The effect is visible in Figure 3-39, when compared to the output spectrum of a modulated signal with a single-bit or 1.5-bit delta-sigma modulator. We can observe that the out-of-band noise can be attenuated in specific bands, while being like a single-bit DSM in between. It should be noted that a 1.5-bit output stage can be implemented using pseudo-differential single-bit output stages and additional logic. Similarly, complex zeros can also be designed using this concept. More details are given in [66] on these aspects.

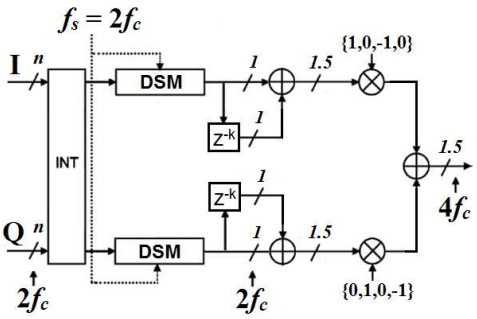


Figure 3-38 Digital-to-RF mixing, including a single-tap FIR filter.

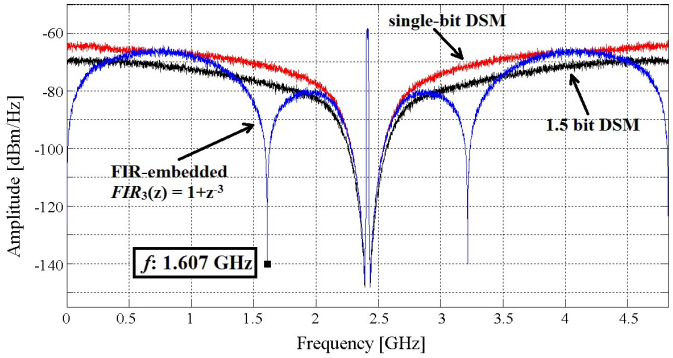


Figure 3-39 Simulated spectrum of a single-bit delta-sigma modulator, a 1.5-bit modulator and a structure incorporating an FIR filter.

3.4.4. FIR DAC

a) FIR-DAC principles

The principle of semi-digital FIR-DAC using the output of a 1-bit ΔΣ modulator comes from [67] for audio signals. A ΔΣ output stream feeds a digital delay line and the selected taps are summed in the analog domain (Figure 3-40). The main advantages are that 1-bit DACs are inherently linear and that mismatches of coefficients values only affect the transfer function and not the linearity, as in multibit DACs. Specifically, the random errors have a negligible effect in the bandwidth of the filter, but they limit the maximum attenuation of the stop band.

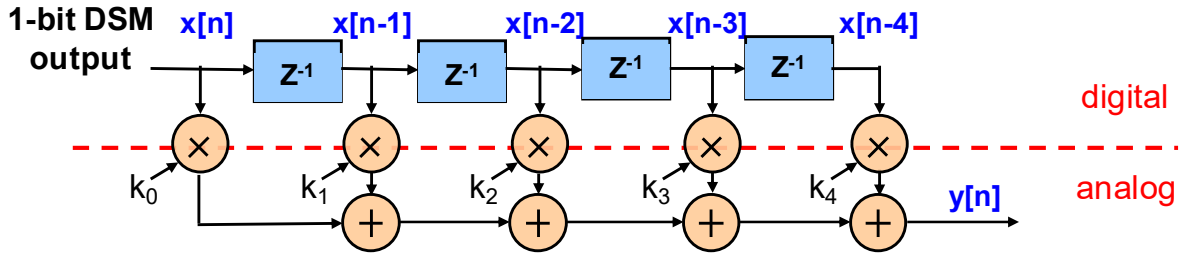


Figure 3-40 General principle of a semi-digital FIR DAC

In this subsection, some of our work using these concepts will be described. First, when implementing the transmitter described in Section 3.3.1, the power combining process is performed with transmission lines. The FIR structure can be activated by introducing a configurable delay line in front of each channel. The second implementation concerns the use of current sources to construct a reconstruction filter for broadband 802.11ac signals dedicated to an interleaved 2-path digital transmitter. Finally, the concept is also exploited in the switching capacitor circuit presented in Section 3.3.2 to provide out-of-band noise filtering in an integrated digital transmitter. This latter approach has been fully covered in the previous section.

b) Semi-digital RF frequency filtering

The power combiner architecture presented in Section 3.3.1 offers the possibility of implementing such a semi-digital filter at RF frequencies [52]. The shift registers are implemented in a 65 nm CMOS chip with fast flip-flops using True Single-Phase Clock (TSPC) dynamic logic and multiple cycles of the clock frequency are selectable with dedicated multiplexers. In this specific 5-channel demonstration, since it is not possible to weight the output inverters, all the coefficients are equal to ± 1, which gives transfer functions of the type $H(z^{-1}) = 1 \pm z^{-n_1} \pm z^{-n_2} \pm z^{-n_3} \pm z^{-n_4}$. The summation is done by

the transmission lines in the IPD substrate. The resulting functionality is shown in Figure 3-41, in which approximately 15 dB of attenuation is provided at specific frequencies when FIR filtering is enabled. This concept has also been extended in [5] for suppressing undesired quantization noise in selected frequency bands.

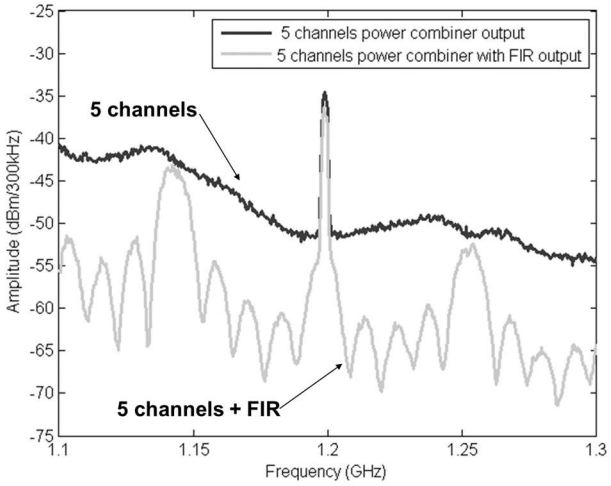


Figure 3-41 Output spectrum of a CMOS 5-channel power combiner using semi-digital FIR filtering. The input signal is a 1-bit delta-sigma modulated stream.

c) High-speed configurable FIR-DAC with a high number of taps

There have been numerous attempts to use a FIR-DAC for RF channels in the literature [5], [12], [68], [69], but most implementations rely on multi-bit DACs included in a filter with few coefficients, typically from 1 to 3. An implementation of high-speed FIR-DAC circuits with a high number of coefficients is proposed in [70]. In order to overcome image and quantization noise requirements, this work proposes a multi-mode low-power multi-standard transmitter based on a 1-bit semi-digital filtering DAC, configurable for both narrowband and broadband standards, while reusing the hardware optimally. As part of the ANR WENDY project, the goal was to develop hardware that can be shared to meet various standards such as 802.11ac (WiFi) and 802.11ad (WiGig). The baseband data rates and central frequencies are widely different. The bandwidths range from 20 and 160 MHz for the 802.11ac to 1.76 GHz for the 802.11.ad. The idea is to configure the semi-digital filter (i) to remove quantization noise and image replicas for standards such as 802.11ac or (ii) to shape the broadband channel according to the mask requirements for standards such as 802.11ad. This would advantageously replace a multi-bit DAC associated with an analog low-pass filter, while moderately increasing the complexity of the digital signal processing blocks.

For broadband WiGig 802.11ad signals, the architecture is presented in Figure 3-42. In this mode, the input signal is oversampled by two at a sample rate of 3.52 GS/s at the DAC input.

Interpolation filters which increase resolution are not required at this stage and oversampling can be directly implemented by zero-insertion or zero-order-hold (ZOH) processes. The sinc response of ZOH introduces a drop in the bandwidth that can degrade the EVM. Thus, an oversampling process with zero-insertion is chosen because it does not require any additional hardware and keeps the ripple of the bandwidth unchanged. The root-raised cosine channelization of the signal will be executed directly on this single-bit signal using the filter capabilities of the FIR DAC. A system-level study shows that 17 coefficients are needed for good channelization as illustrated in Figure 3-43. It should be noted that the architecture is very tolerant to the matching of current sources, allowing up to 14% of mismatch [71]. This architecture replaces the high-power, high-speed digital interpolation filters and the associated multi-bit DAC.

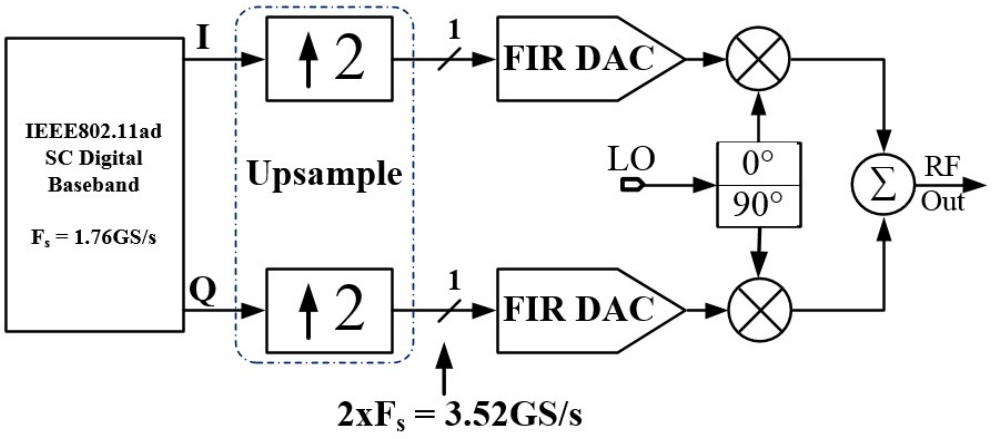


Figure 3-42 Proposed architecture for channel generation for WiGig 802.11ad

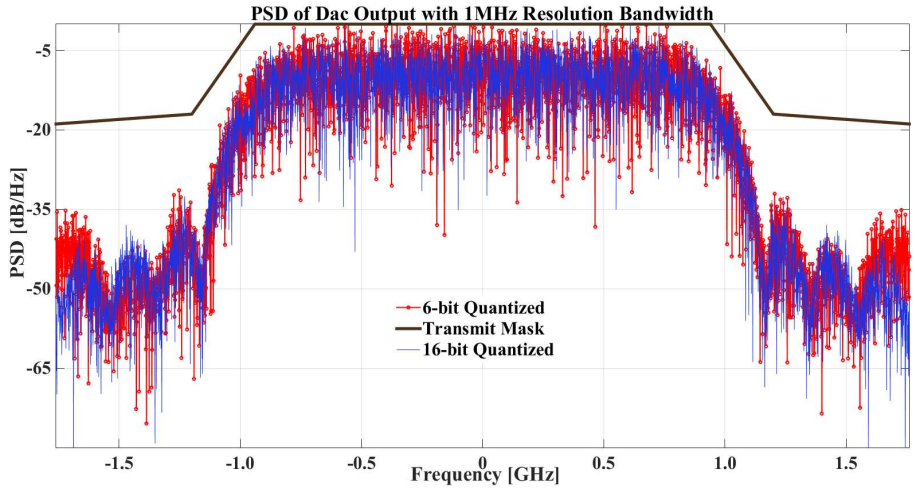


Figure 3-43 Spectrum of quadrature signals at the output of FIR DACs when a root-raised cosine filter with 17 coefficients is applied. This simulation also shows the effect of the resolution of the coefficients.

Figure 3-44 details the architecture of the 802.11ac system. The main difference lies in the signal processing path that includes a single-bit delta-sigma modulator. The input signal is an OFDM modulated channel with a bandwidth of up to 160 MHz. This signal is

oversampled by a factor of 22 to reach the final data rate of 3.52 GS/s. A first multiplier-less half-band filter increases the sampling rate by 2, then a simple zero-order hold is realized to reach the oversampled frequency. A 3rd-order 1-bit low-pass delta-sigma modulator quantizes the signal into a high-speed digital stream. The quantization noise of the delta-sigma modulator can be attenuated to below the requirements of the transmit mask by selecting a suitable set of coefficients in the semi-digital FIR DAC. The co-design of the delta-sigma modulator noise transfer function and the FIR-DAC response have shown that an FIR filter with 63 taps and 6-bit quantized coefficients is needed to obtain a proper out-of-band attenuation.

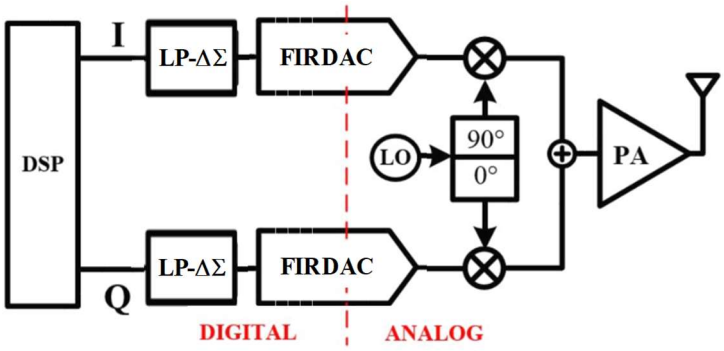


Figure 3-44 Proposed architecture for generating 802.11ac signals.

The system simulation for the 160 MHz mode is illustrated in Figure 3-45. It can be seen that the transition band of the FIR DAC filter cancels out the increasing quantization noise of the delta-sigma modulator. The resulting output noise is less than the required transmission mask (-40 dBr at its lowest level). An additional margin is considered to account for spurious emissions from the transmitter to a nearby receiver noise floor. An EVM value of -28.7 dB is obtained for the 160 MHz mode with 16-QAM OFDM input. This EVM contribution is manageable because it has a margin of 10 dB over the limits of the standard.

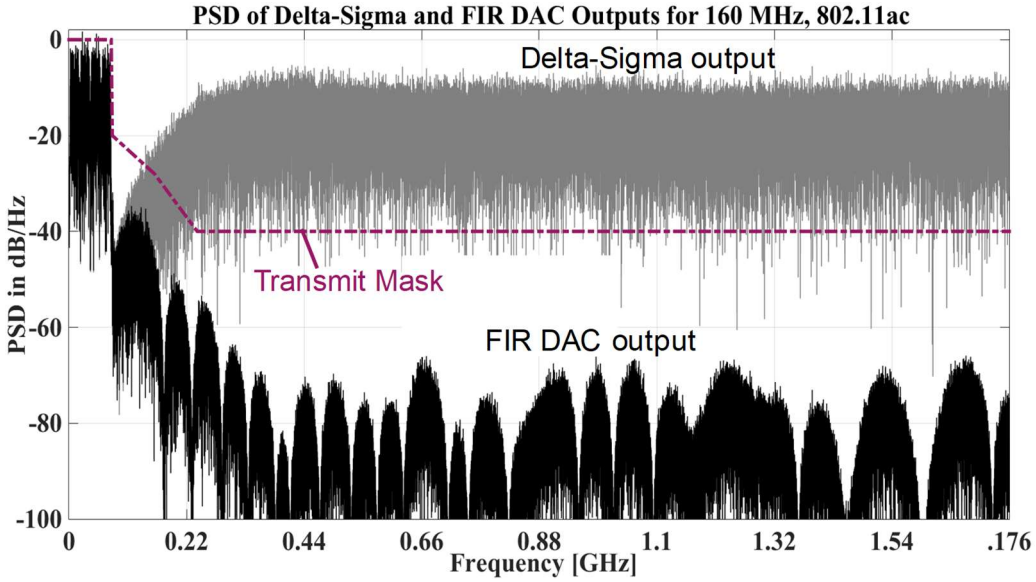


Figure 3-45 PSD of the delta-sigma modulator and FIR-DAC outputs with a 802.11ac 160 MHz signal.

d) Time-interleaved high-pass transmitter architecture

Digitizing the mixer is a very simple and well-known process as long as the sampling frequency is four times the carrier center frequency. Nevertheless, this poses a problem for the operating frequency of the circuits because they are related to the generally high carrier frequency. It has been demonstrated in [72]–[75] that L-path parallel DACs, clocked at 1/L of the input sample rate, can be used to suppress Nyquist images of a digital sampled input signal. In the particular case of two-path parallel DACs, their clocks are delayed 180° from each other and are at a frequency 1/2 of the input sampling frequency. Theoretically, all the images of the digital input signal in the second and third Nyquist zones are absent from the summed analog output. This principle was used in [76] to create the architecture of Figure 3-46 in order to lower the sampling rate required by a factor of 2, not just for the DACs, but for the overall architecture. The summed output consists in interleaved down-sampled streams. Each path processes odd and even samples respectively. A linear interpolation block estimates the missing samples to feed the input of low-pass delta-sigma modulators [26]. Baseband data is then up-converted with a simple scheme {+1, -1}. After aligning the clock with a half-cycle delay, the mixer outputs ({−I2, I4, ...} and {−Q1, Q3, ...}) are sent to the two parallel DACs, sampled with 180° phase-shifted clocks. All blocks of the architecture work at 2 fc, while generating a signal around fc without images. The included FIR-DAC implements a high-pass filter to eliminate the quantization noise of the delta-sigma modulators, as explained in the previous section. The transformation of the low-pass to the

high-pass is performed in the form of a simple inversion of the following stages in the flip-flop delay line.

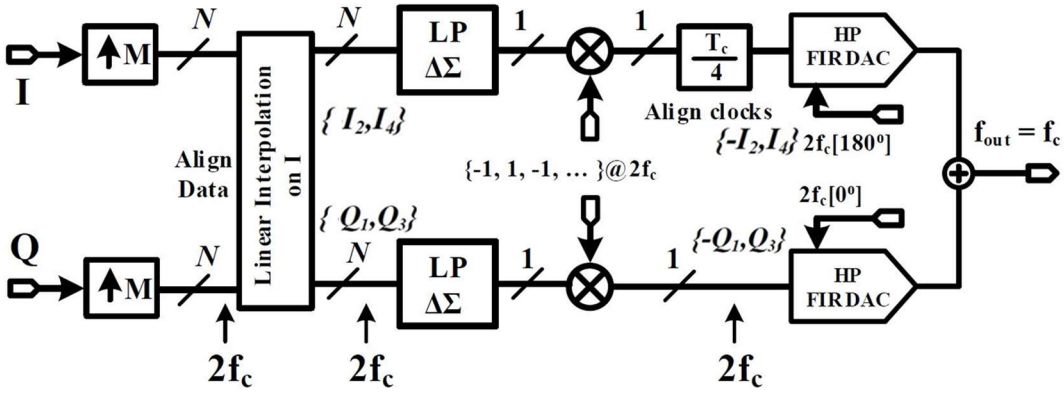


Figure 3-46 Proposed transmitter architecture based on 2-path parallel 1-bit HP FIR DACs

System-level architecture simulations were performed to validate the proposed quadrature modulator in a practical implementation. The simulation results for a sinusoidal signal and broadband 160 MHz 802.11ac OFDM signal are shown in Figure 3-47 and Figure 3-48, respectively. The two baseband signals are oversampled by 22 with half-band filter chosen as the interpolation filter of the first stage. A cascade-of-resonators, feedback form (CRFB) topology has been selected for the 4th-order, 1-bit LP DSM. The 1-bit HP FIR DAC has 8-bit resolution coefficients and is designed for a band ripple of less than 0.5 dB and a stopband rejection of 60 dBr.

The frequency response of Figure 3-47 illustrates the image cancellation process by time-interleaved DACs and shows rejection of the image down to the noise level. The increasing quantization noise is also canceled by the HP filtering in the DAC. The broadband nature of the system is represented in Figure 3-48 with a 160 MHz 802.11ac channel. The error vector magnitude (EVM) is simulated to be at -23 dB in the worst case (160 MHz 64-QAM signal with the distortion of the sinc function taken into account).

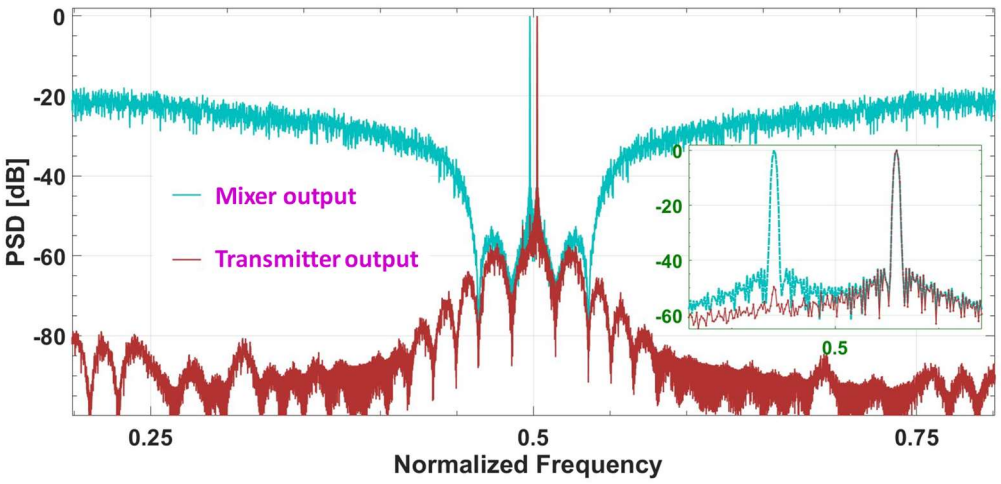


Figure 3-47 HP FIR-DAC simulations with a sinusoidal input. We can clearly see here the process of cancelling the image due to time interleaving. The image attenuation is 50 dB and is limited by the interpolator.

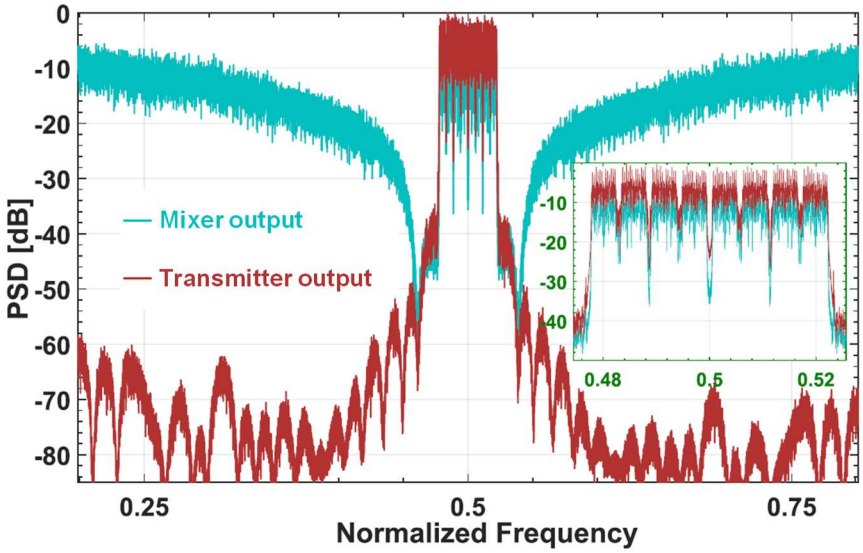


Figure 3-48 HP FIR-DAC simulations with a 160 MHz 802.11ac broadband channel.

A 28 nm FDSOI integrated circuit with a single HP FIR DAC using current sources was designed, manufactured and assembled in a QFN40 package (Figure 3-49). The 50 Ω output load resistors are formed inside an output probe head and the analog voltage is supplied directly from this probe. The bias voltage is 1.2 V while the digital circuits operate at a lower voltage. The total load current is 14.1 mA while the digital unit current cells (UCC) array, the delay line, the routing matrix, and all the clock and data buffers consume 19.4 mA at a clock frequency of 600 MHz. To determine the shape of the transfer function, the measurement is performed using a 1-bit PRBS data. The 1-bit random pattern was passed directly to the HP FIR DAC without digital processing and was clocked at a fraction of the FIR DAC update rate. The result of Figure 3-50(a) shows a stopband rejection of up to 50 dB. The background noise reaches -143 dBm/Hz at 200 MHz away from the center of the channel on the right side. It should be noted that the output of the chip is not externally filtered. Figure

3-50(b) shows the measured spectrum of the HP FIR-DAC output when a delta-sigma modulated baseband OFDM signal is applied. The rising quantization noise from the DSM is filtered up to 47 dB in the adjacent channel and more than 50 dB in the far spectrum. Although the filter maintains a flat passband, the effect of the zero-order hold clocking is visible in the difference between the attenuation of the upper and lower out-of-band noise components. Unfortunately, the digital circuits in the chip have a logic error that degrades the waveform and creates side lobes around the channel, as can be seen in the plots. The error has been modeled and the transfer function has been validated by retroactively simulating the output of the chip with the model. The results of the simulation are superimposed in the two spectra and they reveal that the measured results are very close to the simulated behavior.

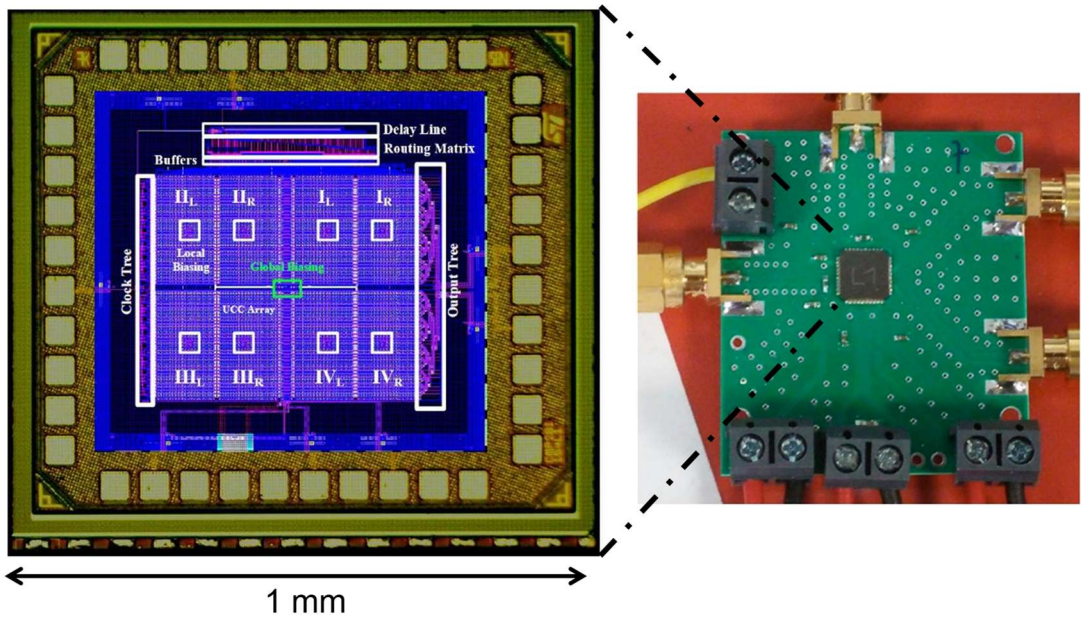


Figure 3-49 HP FIR-DAC 28 nm FDSOI chip microphotography and PCB test board with QFN40 package.

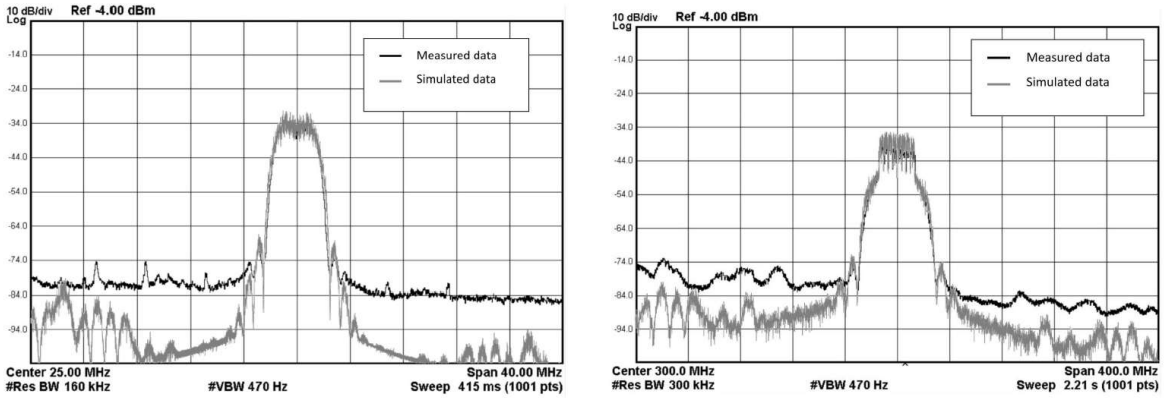


Figure 3-50 Experimental results of a 1-bit single-channel HP FIR DAC. (a) PRBS input clocked at fs /11, where fs is the FIR DAC update rate. (b) Wideband input with an oversampling rate of 22.

A comparison of the HP FIR-DAC chip performance with state-of-the-art DRFCs is found in [76]. In addition, to highlight the potential of the proposed solution, a qualitative comparison with existing transmitter architectures is reproduced in Figure 3-51. The main differences among existing solutions tend to be on the digital-to-analog conversion and the mixing stage. These two aspects are compared separately. The proposed architecture uses inherently linear 1-bit DACs and avoids problems associated with an upconverting circuit by integrating simple 1-bit mixers into the digital signal processing chain. The coexistence of the transmitter being important, the existing out-of-band noise filtering mechanisms are also compared. The proposed architecture provides a mixed-mode integrated filtering scheme that can be more compact than high-order analog reconstruction filtering and more efficient than simply relying on a sinc function. Unlike other architectures, the output frequency is only defined by the clock. A high carrier frequency can be achieved by up-conversion mixing with an LO. This may not be easily achieved in architectures where the clock and LO frequencies are closer together to compensate for the lack of a steep reconstruction filter. In summary, the table shows the compatibility of the HP FIR DAC-based architecture for advanced low-power CMOS implementation. They also demonstrate that the proposed architecture meets the requirements of broadband transmissions with low energy cost and silicon area.

	Architecture	DAC	OOB noise filter	Output Freq.	Mixing Stage
[JSSC 14]	Traditional analog	N-bit DAC at f_{CLK} §	Biquad + RC	f_{LO}	analog mixing with f_{LO}
[JSSC 07]	Quadrature DRFC	N-bit DAC at f_{CLK} §	Kth-order LC BP filter §	$f(f_{CLK}, f_{LO})$ †	analog mixing with f_{LO}
[JSSC 09]	All-digital	NA	No filtering	$f_c = f_{CLK}/4$	1-bit digital mixer at f_{CLK}
[JSSC 16]	TI RF-DAC	N-bit TI ΔΣ DAC at f_{CLK} §	$sinc(x)$	$f_c = f_{CLK}/2$	M-bit digital mixer at $2f_{CLK}$ §
[TCAS-II 16]	Traditional with FIR DAC	1-bit LP FIR DAC	Lth-order embedded FIR §	$f(f_{CLK}, f_{LO})$ ‡	analog mixing with f_{LO}
This work	2-path TI HP FIR DAC	1-bit HP FIR DAC	Lth-order embedded FIR§	$f_c = f_{CLK}/2$	Embedded in digital process

§ $N, K, M, L > 1$ † $f_c = f_{LO} \pm f_{CLK}/4 + \Delta f$, $\Delta f \ll f_{CLK}$ ‡ Due to ΔΣ, $f_{LO} = q * f_{CLK}$, $q \in \mathbb{N}$

Figure 3-51 Qualitative comparison of the proposed architecture with existing transmitter architectures (references refer to the following: [JSSC 14] is [77], [JSSC 07] is [11], [JSSC 09] is [26], [JSSC 16] is [17] and [TCAS-II 16] is [70]).

3.5. Summary and perspectives

After presenting the challenges associated with digital-intensive transmitters, this chapter has described some research topics to address some of them. In a first subsection, I described our investigations on the speed of operation to enable digital RF transmitters. The core of the work was based on digital delta-sigma modulation to digitally generate RF signals in advanced CMOS technologies and includes demonstrations through the design, fabrication

and measurements of integrated circuits. My Ph.D. thesis was a starting point that was derived in more complete systems. Time-interleaving of delta-sigma modulators has been found to be very effective in achieving high oversampling rates with moderate sampling frequencies, while being compatible with automatic circuit synthesis. Finally, we demonstrated the operation of a FIR filter at 10 GS/s. Thanks to this work, it has been shown that pushing the operating frequency is costly from an energy point of view.

The second part showed the use of transmission lines for combination of single-bit channels as well as a complete integrated solution based on the combination of a switched-capacitor network with a single-bit delta-sigma modulator. This demonstration showed the benefits of designing output stages with only inverters and capacitors in advanced technology nodes. In addition, a semi-digital filter has been co-designed with the output LC filter to allow for reduced complexity of the built-in filter.

The last part introduced ways to mitigate out-of-band interference generally present in digital transmitters and consisted of four parts. In a first subsection, a digital power amplifier achieved good performance while attenuating image replicas using a multi-rate approach. Then, experiments with BAW devices to filter out excessive quantization noise were presented. A third part showed several studies on the engineering of the noise transfer function of the delta-sigma modulator by introducing specific notches in complex architectures. Finally, the concept of FIR-DAC has been introduced and a configurable filter for narrowband and broadband communication channels has been described. A digital transmitter with time-interleaved high-pass FIR-DACs has been proposed as an application of these concepts.

The works presented offer interesting perspectives and two research paths are identified. First, the use of oversampling and noise-shaping concepts is required to allow fully-digital transmission in mobile applications but should be more relevant for moderate bandwidths and moderate carrier frequencies. Emerging Internet of Things (IoT) communication markets require wireless network standards that operate in the spectrum below 1 GHz, providing long-range and low-power operation, such as 802.11ah and 802.11af. In the 5G context, this is also noted as White-Fi or Super-WiFi. These emerging standards target licensed bands in TV white space spectrum in VHF and UHF bands (54 to 790 MHz) or unlicensed operation in the 900 MHz bands. Because it provides long-range and low-power operation, applications in sensor networks, IoT, machine-to-machine (M2M) communications and Human Body Communications (HBC) are envisioned. Since transmitters require a great deal

of flexibility to meet these specifications, solutions based on digital RF transmitters integrated in advanced technologies are of primary interest and constitute a research area with challenges such as extremely low power consumption, high integration (preferably with no passive external components) and improved configurability.

The second aspect concerns performance. To handle extreme bandwidths and multi-Gbps data rates, high-bandwidth high-speed RF DACs are required. They should rely on interleaved structures such as the work done in [78], in which a 50 dB SFDR is demonstrated for a 5.5 GHz signal. To improve linearity and increase the output frequency, all static and dynamic imperfections of the interleaved DACs must be compensated or calibrated. With the digital signal processing of advanced CMOS technologies, it is possible to consider techniques that achieve 70 dB of SFDR for output frequencies up to tens of GHz.

3.6. Bibliography

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Chapter 4 Contributions to baseband circuits for mmW receiver systems

This chapter details 3 distinct contributions in the field of baseband circuits for mmW receivers. The first work was done during my post-doctoral stay at UC Berkeley's Berkeley Wireless Research Center (BWRC). It addresses adaptive baseband circuits for 60 GHz communications capable of recovering GS/s signals with low power consumption in a context where echoes and reflections contribute greatly to interference. The second work highlighted is the study of a decision feedback equalizer utilizing digital signal processing concepts in continuous-time, such as a configurable digital delay line exploiting the functionalities of the 28 nm FD-SOI technology. Finally, the investigations around the subsampling of mmW signals will be detailed.

4.1. 60 GHz adaptive high data rate baseband receiver

4.1.1. Position of the problem

The first generation of products, targeting wireless communication in the 60 GHz band, appeared in 2015 to enter the consumer applications market. During the previous period, the impending need for integration with mobile devices imposes an incessant effort to reduce energy consumption. From the point of view of power consumption, the choice of modulation favors single-carrier (SC) schemes instead of using OFDM. This fact has been recognized by the IEEE 802.11ad standard, which specifies a low power physical layer using BPSK or QPSK. In addition, the 60 GHz propagation is characterized by a long delay spread, compared to the duration of the symbol (Figure 4-1), which imposes Inter-Symbol Interference (ISI) and requires the existence of an equalizer block in the communication chain. Choosing the extent of the 60 GHz channel delay spread considered for equalization is an important decision. It must support the usage model for the desired application, as well as the system deployment environment. Operation in Line-of-Sight (LOS) implies the equalization of a substantially shorter part of the multipath spread than a Non-Line-of-Sight

(NLOS) scenario. With regard to equalization techniques, frequency-domain equalization (FDE) is identified to be more power-demanding than time-domain equalization (TDE), due to the quantity and nature of operations involved.

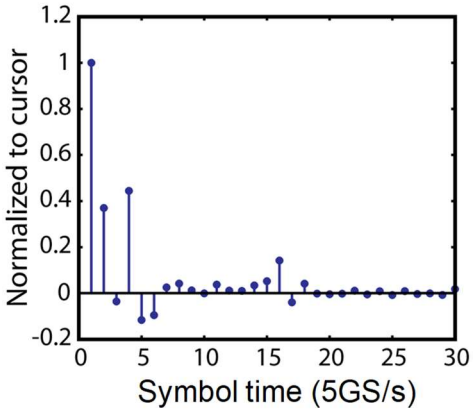


Figure 4-1 Example of a typical 60 GHz Line-of-Sight channel

Multi-GS/s data-converters and DSPs are reported to consume a large amount of power, making these designs unsuitable for handheld devices. A mixed-signal baseband with simple modulation (QPSK) – inspired by multi-Gb/s chip-to-chip links – is very attractive since it enables the use of energy-efficient low dynamic range analog signal processing. Previously presented mixed-signal solutions for 60GHz links have shown limited capability in equalization complexity [1], have relatively low data-rate [2], and/or require external adaptation and clock/carrier recovery. The proposed work [3], [4] presents a mixed-signal baseband receiver in 65nm CMOS capable of adaptively equalizing significantly longer multi-path interference profiles and automatically recovering both the TX/RX carrier as well as baseband clock phase/frequency differences. The design supports data-rates of up to 10Gb/s using QPSK modulation and consumes a total of at most 53mW, substantially easing the bottleneck of power consumption for 60GHz in mobile devices.

4.1.2. 60 GHz baseband receiver design

Even with significant directionality, at symbol rates of 5 GS/s a 60 GHz channel may exhibit 30-50 symbols of post-cursor inter-symbol interference (ISI) due to multi-path reflections. A mixed-signal decision feedback equalizer (DFE), such as presented in Figure 4-2, is a good candidate for efficiently removing this ISI [2]. However, it has been shown that due to self-loading caused by the capacitance of the current-steering switches, only a relatively limited number of taps can be realized before it becomes infeasible to achieve the bandwidth required for 5 GS/s operation, using conventional summation (Figure 4-3). This limitation can be

mitigated by noting that even though each tap must be able to handle the worst-case ISI over all possible channels, the total ISI for any given channel will always be less than the sum of the worst-case ISI at each tap. A cascode summation DFE can therefore enable substantially more taps by sizing the cascode to handle only the total ISI cancelation current (2x the cursor in this design). This reduces the capacitance at the summer's output and moves the capacitance of the switches to a lower impedance node, both of which relax the self-loading limitation. This is illustrated on Figure 4-3. Cascode summation enables 3 to 5 times more taps than direct summation at equal power and data-rate. This design implements 20 complex taps (20 direct and 20 cross-channel coefficients) on each (I and Q) channel.

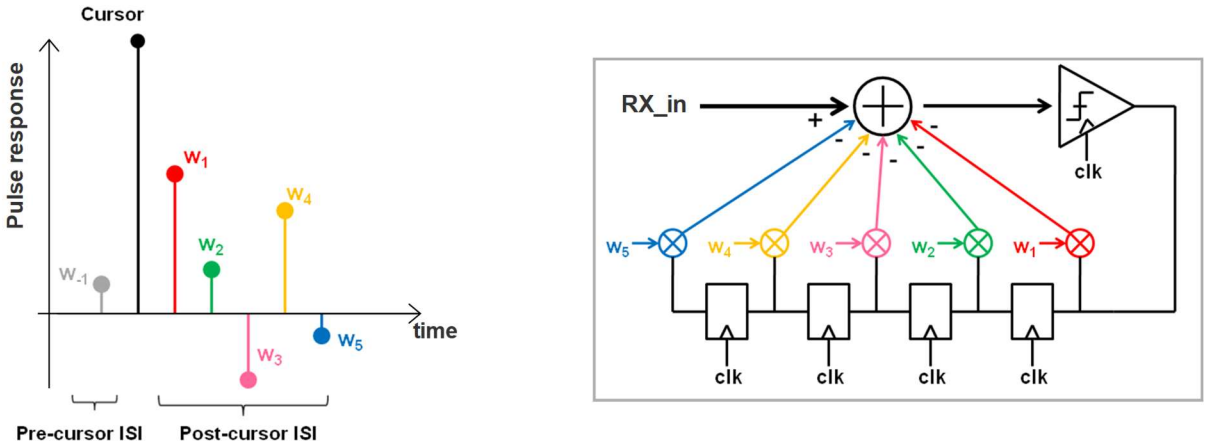


Figure 4-2 (left) Channel impulse response, including pre-cursor and post-cursor taps and (right) DFE structure to cancel post-cursor ISI. The colors correspond to the relative position of the taps.

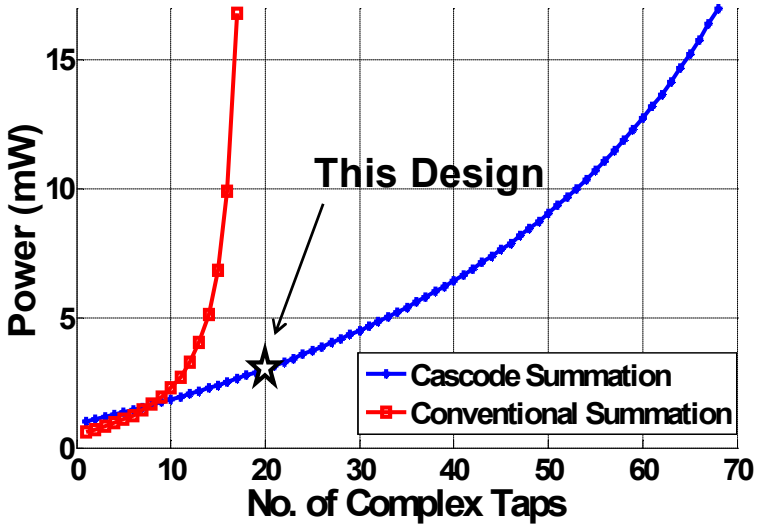


Figure 4-3 Required power versus the number of taps to cancel, using conventional summation and cascode summation. In this case, the total number of ISI is equal to 2 times the cursor value.

The proposed baseband receiver is shown in Figure 4-4. It is composed by a variable gain amplifier (VGA), phase rotators for carrier recovery, samplers that will act as slicers with an adjustable clock for phase and frequency alignment, and a DFE block to correct the channel-induced ISI. An adaptation engine is designed to run an adaptive algorithm to converge to the correct setting of all the parameters in the receiver chain, consisting of three distinct loops (tap adaptation, carrier recovery (CR) and clock/data recovery (CDR)).

In addition to the data sampler, the DFE uses an adaptive sampler that tracks the mean data eye level (dLev). Therefore, by driving the correlation between the sign of the errors around dLev and the data at previous instants to zero, a sign-sign least mean squares (LMS) algorithm [5] converges to the optimal weight of the taps, as illustrated in Figure 4-5. Carrier phase/frequency misalignment rotates the downconverted signal and causes errors about the mean data eye level (dLev). Therefore, by driving the correlation between the sign of the errors around dLevQ (dLevI) and the I-data (Q-data) to zero, the adaptive sampler required for DFE tap adaptation can be re-used (with no power overhead) to enable a sign-sign LMS loop for carrier recovery. This design uses a 2^{nd} order 500MHz digital loop filter and an analog phase rotator with average/worst-case phase steps of 5.5°/8.2° to close the CR loop. The CDR uses an additional edge sampler and a 2x oversampled bang-bang dual-loop architecture with a 2nd order digital loop filter.

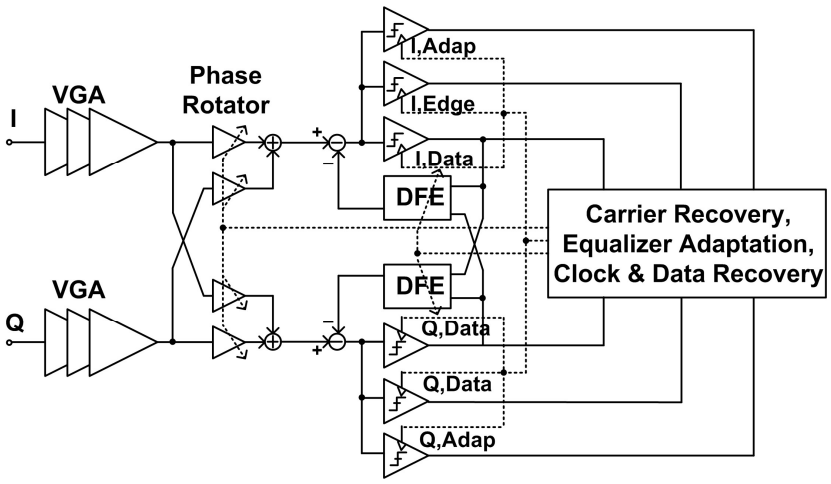
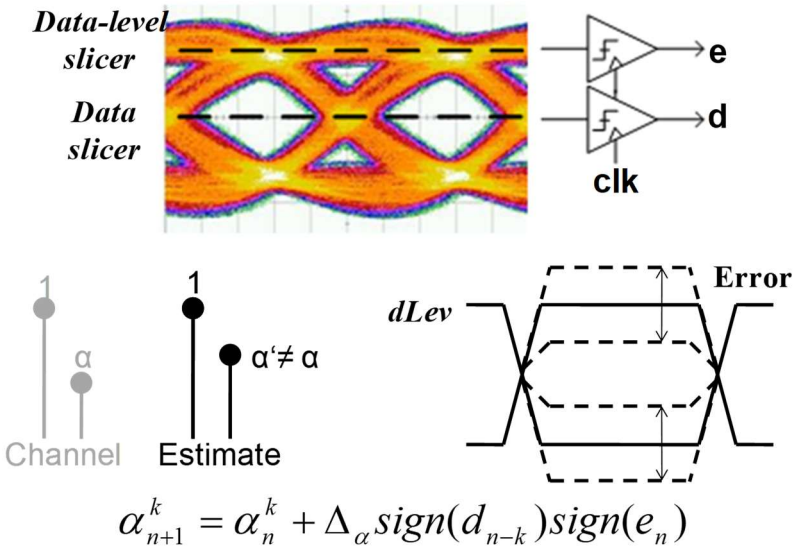


Figure 4-4 Proposed architecture for the 60 GHz baseband receiver



$$\alpha_{n+1}^{k} = \alpha_{n}^{k} + \Delta_{\alpha} sign(d_{n-k}) sign(e_{n})$$

Figure 4-5 Explanation of the sign-sign LMS algorithm to update the weight of each tap.

4.1.3. Chip measurement results

The fabricated receiver test-chip (Figure 4-6) was tested using a 5 GS/s 2-channel Arbitrary Waveform Generator (AWG). The AWG was programmed to mimic a 60 GHz multi-path channel with ISI and signal constellation rotation due to carrier frequency offset while generating 2^7-1 and 2^9-1 PRBS data on the I and Q channels. For up to ±50 ppm of carrier frequency offset, ±350 ppm of baseband CLK frequency offset, and ISI up to 2.5x the cursor (with the first tap handling 0.5x and the main DFE 2x) with all three on-chip adaptive loops (CR, CDR, and eq. tap) operating, the test-chip was able to receive 10 Gb/s QPSK data with BER $<10^{-12}$ (measured with an on-chip BERT, Figure 4-7). Post-convergence, the steady-state behavior of all loops (with 50 ppm carrier frequency offset) was measured as a histogram by scanning out the on-chip adaptation registers (Figure 4-8). The power breakdown appears on Figure 4-7.

A comparison is made to prior mixed-signal designs without adaptation in Table 4-1. This work achieves 8-13X improved power efficiency (4.5 pJ/bit) at 4-10X higher data-rate (10 Gb/s). Additionally, the system has been designed as complete as possible, with all the correction loops on-chip and since the achieved bit error rate is low, it does not require expensive error control coding.

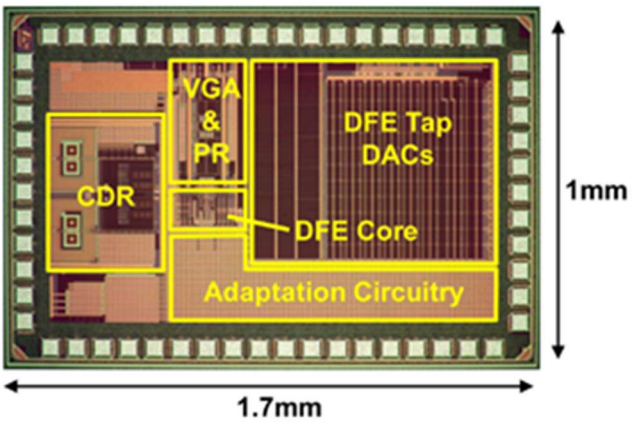


Figure 4-6 Chip microphotograph of the 65 nm baseband receiver chip

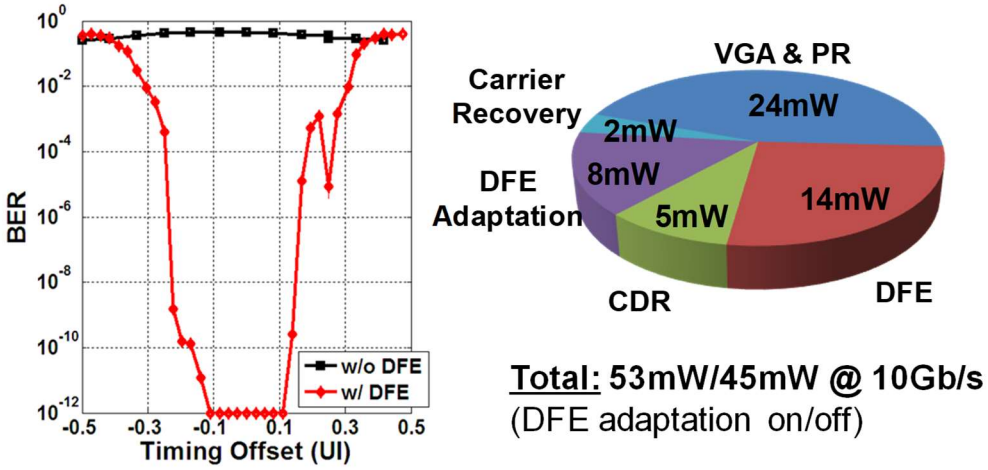


Figure 4-7 (left) Bathtub curve showing a BER lower than 10^{-12} when the DFE is activated and (right) power breakdown of the complete circuit.

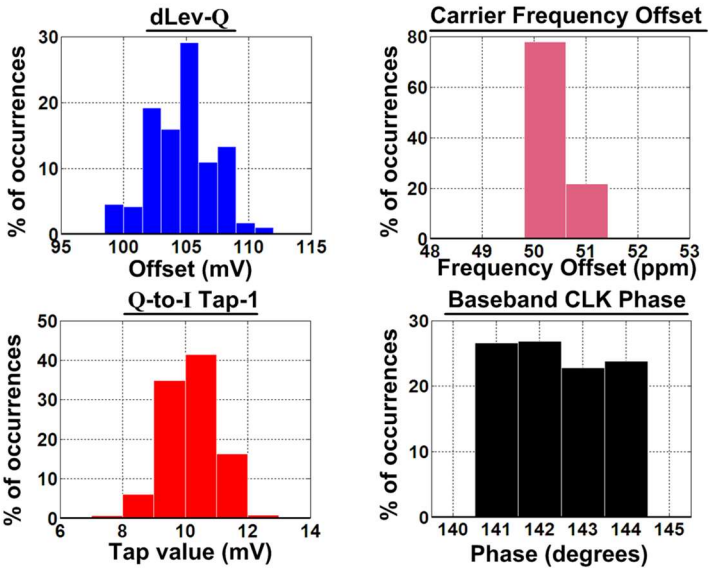


Figure 4-8 Histogram of on-chip post-convergence adapted settings with 50 ppm carrier frequency offset: dLev-Q – Q-channel adaptive sampler offset, Carrier recovery – phase rotator setting , DFE (Q-to-I tap-1 shown), and CDR – phase mixer setting.

		[Sobel JSSC 2009]	[Chen VLSI 2007]	This Work
Technology		90nm CMOS	90nm CMOS	**65nm CMOS**
VGA-PR	Gain	–	42dB	32dB
	Bandwidth	–	1.4GHz	2.2GHz
# of DFE Coefficients		16	–	**80**
Adaptation		–	CDR (CR not reqd.)	**CDR, CR, Equalizer**
Total Baseband Power		55mW	85mW	**45mW**
Minimum BER		< 1E-3 (sim.)	1E-9	**< 1E-12**
Data-Rate		1Gb/s	2.4Gb/s	**10Gb/s**
Power Efficiency		55pJ/bit	35.4pJ/bit	**4.5pJ/bit**

Table 4-1 Comparison table with previous works from [2] *and* [6]

4.2. Continuous-time digital signal processing for equalization

4.2.1. Introduction

In the context of high-speed receivers, mixed-signal systems that include decision feedback equalizers (DFE) are of high interest to equalize channels and provide low power consumption receivers, as demonstrated in the previous section. Continuous-time digital signal processing techniques are studied here to overcome the challenges imposed in this type of systems. This subsection will be composed of two parts. The first one will focus on the system-level architecture. It is demonstrated that continuous-time digital signal

processing techniques can lead to a decrease of the energy consumption of a DFE by at least a factor 4 [7]. A second part will focus on the design, integration and characterization of an essential block that is a configurable digital delay cell with coarse/fine tuning in 28nm FDSOI. This cell leverages the use of features of the FDSOI technology such as the back-gate control [8].

4.2.2. System-level architecture

In view of the work exposed in the previous section [4], consisting of enabling a large number of taps to be cancelled, the solution here is to support a critical-tap cancellation scheme, which will permit equalization of those multipath components that bear the highest contributions to ISI. The choice of integrating continuous-time delay lines, comprised of variable asynchronous digital delay elements, brings value as one considers the stringent timing constraints for the shortest loop in the clocked delay approach. This choice also obviates the power overhead involved with static signal routing and clock distribution. For example, in [9], DFE flip-flops, tap drivers and clock distribution consume about 50% of total power.

In this work, we outline the architecture of a mixed-signal DFE, for 60 GHz LOS communication, supporting a critical tap cancellation scheme. It features configurable continuous-time digital delay lines; a design choice, which results in a system that operates under channel-dependent power consumption.

a) Critical-tap cancellation

Bit Error Rate (BER) simulations prove that a 60 GHz LOS link could benefit from the equalization of a limited number of impulse response components, should it be feasible to equalize only the critical ones. Using the channel model, available from the IEEE 802.11ad working group, 100 impulse responses (IRs) were realized for the living-room scenario. A link distance of 5 m was chosen, along with 60° half-power beam width and no blocking of the 1st and 2nd order reflections. For the case of BPSK modulation and a rate of 1 Gbps, the BER was derived by zero-forcing critical components up to 20 ns. Figure 4-9 displays the BER as a function of the number of components canceled. Components are consecutively added to the equalization scheme based on their magnitude, starting with the strongest. Assuming constant signal-to-noise ratio (SNR) transmission, the results presented refer to the worst-case channel realizations of the set; namely IR28, IR6 and IR92. Based on these

results, the number of 5 components was chosen as a trade-off between complexity and performance.

The respective BER vs. SNR simulations including the non-equalized cases and the theoretical AWGN channel are presented in Figure 4-10. These provide the reference for system specification. The results demonstrate that for the entirety of the set, and under a 6 dB SNR, a BER better than 10^{-2} is expected. Such a minimum performance is considered sufficient for modern coding schemes.

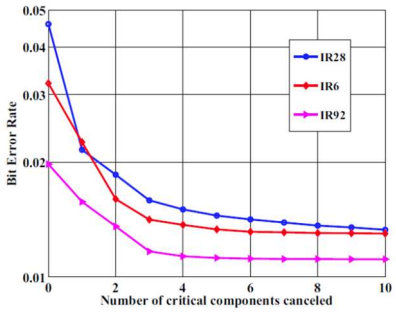


Figure 4-9 Worst-case BERs with an increasing number of critical impulse response components canceled, under Eb/N0=5 dB.

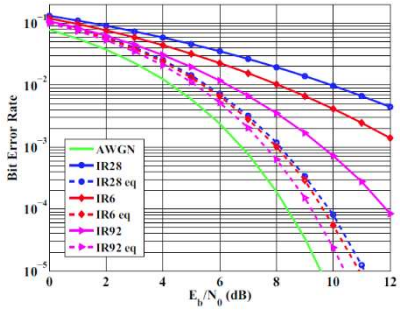


Figure 4-10 Worst-case BERs with (eq) and without equalization of 5 critical components compared to theoretical AWGN.

Based on the above results, the architecture of a 5-tap mixed-signal DFE is proposed. The analysis suggests that the taps must be able to be assigned in any delay arrangement up to 20 ns. Such a specification could be supported by a scheme such as the one in [2]. Assuming a targeted rate of 2 GS/s, a fixed-length clocked delay line of 40 delay elements would drive five 40:1 multiplexers. Introducing redundant delay elements could lead to simpler overhead routing, as in [10]. Nonetheless, all possible tap delay arrangements should be able to be addressed. A typical block diagram for a mixed-signal DFE is displayed in Figure 4-11. It requires a clocked comparator to follow the output of an analog summer, which is usually implemented in current mode for straightforward node summation. The DFE adaptable

coefficients can be realized as current-steering digital-to-analog converters, thus realizing tap magnitude and sign.

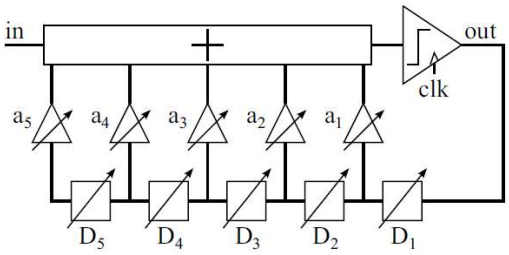


Figure 4-11 DFE block diagram.

b) Channel-dependent power consumption

Circuit simulations were carried out for an advanced CMOS technology node, in order to project system power consumption. This permitted as well, the comparison against the clocked delay line case. We assume a receiver scenario of BPSK demodulation and equalization on a rate of 2 Gbps. The target is to cover a 500 ps to 18 ns delay range for each equalizer tap, in multiples of 500 ps.

Minimum granular delay cannot exceed 500 ps, to avoid data loss at this rate. After accounting for a 20% margin against PVT variations, we have defined the range of variability for the granular delays to be from 200 ps to 400 ps. The valid control codes, as well as stage sizing itself, were chosen based on power consumption minimization. The optimization strategy aimed at approximating the consumption of a reference continuous-time delay line, comprised of fixed 500 ps delay elements. If this reference line is of selectable length, then consumption can be extrapolated as being linear and directly proportional to that length. Obviously, such a topology cannot be suggested, as it ignores sensitivity to process variations. However, it serves as an optimization reference (Figure 4-12) for the proposed configurable architecture. Figure 4-12 sums up all design decisions in terms of power consumption and represents a first perspective on the comparison with the discrete-time delay line approach. The energy consumption of a single clocked delay line can be approximated being directly proportional to the number of comprising flip-flops. Such consumption is static and equals the sum of energies dissipated by all flip-flops. In the case of the suggested continuous-time implementation, consumption is dynamic. It is not only the number of elements enabled, but also the granular delay value configured each time that determine the energy consumed. After observing that most IRs within our test-set does not exhibit an intra-cluster delay greater than 10 ns, the approximation was focused on providing

minimum power consumption for that part of the delay range. For this reason, the widest discontinuity appears only when enabling the last stage. Comparing the energy consumed by the delay element (within the 200 ps – 400 ps range) with the energy dissipated by a standard-cell D-flip-flop, we find an average 60% reduction. We have leveraged this improvement along with the fact that the energy consumed on the element varies almost linearly, but not directly proportionally to the delay value.

The suggested delay line topology exhibits dynamic power consumption that is dependent to tap assignment and therefore dependent to the channel realization meant for equalization. On the stacked histogram of Figure 4-13, this energy is presented along with the constant static consumption of the fully clocked counterpart as a normalized sum. The results of extrapolated power consumption for the set of 100 IRs yield an overall power reduction of 3 to 4 times when compared with the static approach. Obviously, the overall picture could be potentially more favorable. The comparisons reflect neither overhead multiplexing, nor clock driving to each flip-flop, which could exacerbate the power profile of the discrete-time case.

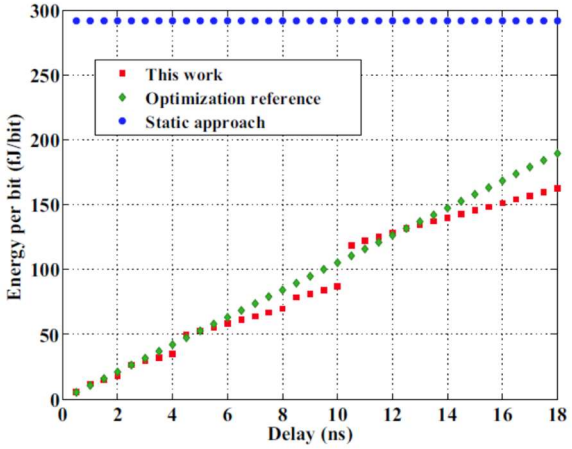


Figure 4-12 Power efficiency in the cases of discrete and continuous-time digital delay realizations versus tap delay value.

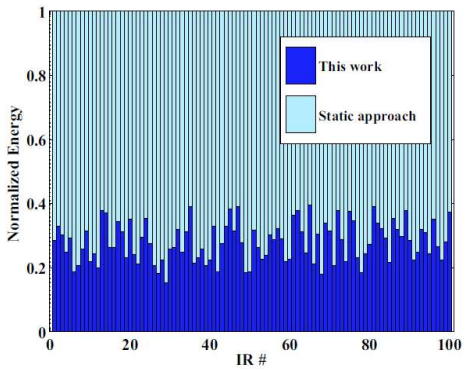


Figure 4-13 Consumption comparison between a static, single delay-line, discrete-time approach and the continuous-time configurable delay architecture presented here.

4.2.3. Digital Delay Line

a) Context and state-of-the-art

Delay controllability has always been the major concern for the reliable implementation of circuits whose purpose is timing. Depending on the application, the range and importance of accurately controlling a delay value differs. For instance, producing reliable timing signals usually comes along with employing elaborate delay-line systems in control-loop architectures.

One of the most proliferated techniques for building power-efficient, variable delay elements has been the thyristor-based [11]. It has received attention over the recent years [12] due to its capability in producing wide-range delays with low power consumption. The work in [13] increased configurability by controlling extra capacitances and [14] proposed techniques to reduce sub-threshold leakage and transient shunt currents.

In the purpose of our work, the implementation of a decision-feedback equalizer featuring continuous-time digital feedback has been suggested. The specification of such system calls for digital delays with: (i) fine granularity, in the order of picoseconds, to accommodate the GS/s throughputs for deployment of standards such as the 802.11ad and (ii) wide-range of configurability, in the order of nanoseconds, to meet the associated delay spreads. The delay line presented in this report is aimed for integration in such a system. The proposed granular delay element is based on a modification of the one in [15], which exhibits low power consumption in an advanced node. The work here extends functionality to provide fine-tuning through body biasing. Implemented in 28 nm UTBB FD-SOI (Ultra-Thin Body and Buried oxide Fully Depleted Silicon Over Insulator) CMOS technology, the transistor body terminal serves as a fine control knob which complements gate control. This way an unprecedented coarse/fine scheme is realized without any extra hardware.

b) Delay Element Design in FDSOI

The proposed thyristor cell topology is displayed in Figure 4-14 and three stages can be readily distinguished. The first stage is a current-starved inverter, whose output (V_C) is connected to a second, gated, inverter stage. The second stage produces a feedback signal, V_F, which controls the transistors in parallel with the ones implementing current-starving. Finally, a driving stage, generates the complementary output signals.

The circuit follows the typical thyristor operation. As it has been extensively presented in bibliography, we summarize operation: As input V_{IN} rises, V_C slowly discharges up to the point where the second stage inverter threshold is crossed. Through V_F, the parallel transistor is then activated and this effectively shorts the "starving" mechanism. So, the discharge of V_C is accelerated thus completing the switch.

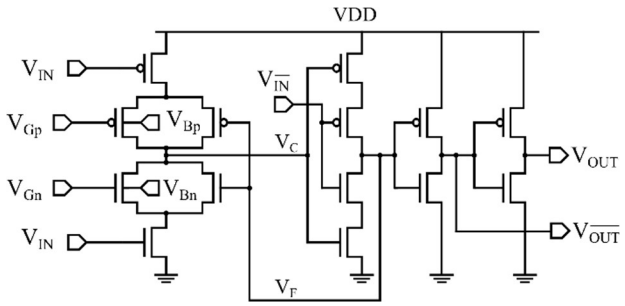


Figure 4-14 Proposed thyristor-type delay element featuring second stage gating and body biasing.

The element's consumption profile is dominated by the current-starved (dis-)charging interval which produces short-circuit currents during the slow switching of the second stage. To minimize the latter, the cell is designed with complementary inputs ensuring that the complemented $V_{\overline{IN}}$ signal precedes its complement. This is realized by cascading delay cells. Arriving directly on the second stage inverter, the input complement plays a preparatory role for the upcoming switch. When followed by V_{IN}, say in a high state, the complemented V_{IN} input $V_{\overline{IN}}$ is already driven low shutting the path to the ground. This action enables the slow second stage output to be raised high without short-circuit current losses.

For the proposed delay element, substrate control is suggested for current-starving. This is made possible thanks to FDSOI technology. As seen in Figure 4-15 (left), the transistor channels are implemented with a buried oxide layer underneath, which prevents source-bulk junction leakage. This ensures a body-tie voltage range which is much wider than in bulk CMOS (Figure 4-15, right). Also, the body coefficient is much more important in FDSOI (85 mV/V), than in the equivalent bulk node (40 mV/V).

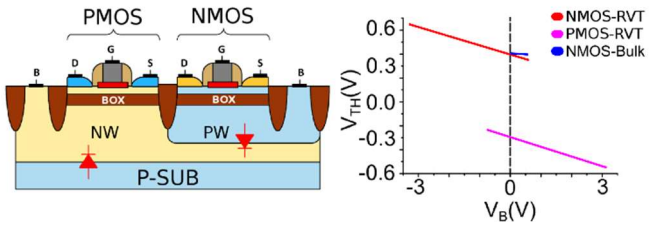


Figure 4-15 FDSOI transistor cross-section (left) and threshold voltage (V_{TH}) variation with body biasing (V_B) for regular Vt transistors (right).

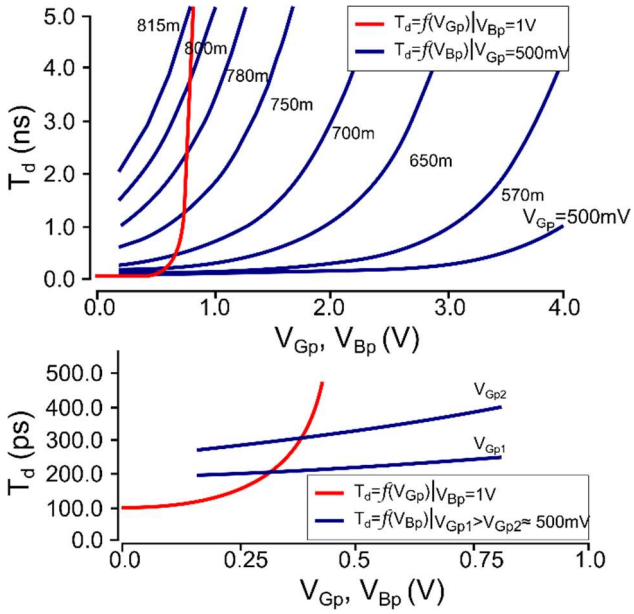


Figure 4-16 Simulations of falling edge delay time. Red curves: varying the gate while keeping body constant. Blue curves: varying the body while keeping the gate constant. Curves are presented on same x-axis to illustrate the evolution of delay, but are not coincident as they refer to different biasing conditions.

Regarding control of the drain current, body biasing is principally of the same nature as gate biasing. However, the electric field is applied through a thicker oxide and a more distant contact. One could easily predict that the effect on current modulation would be less profound. This is exactly the key observation for establishing an extra control knob to fine-tune the delay element.

The transistors of the circuit are sized to produce delays in the order of picoseconds. In Figure 4-16, on the top, we simulate the falling edge delay variation, T_d, against the control inputs. The NMOS starving transistor biases are fixed to V_{Gn}=500 mV for the gate, and V_{Bn}=0 for the body. The red curve refers to keeping the PMOS body as V_{Bp}=1 V and varying V_{Gp}. It is a typical exponential variation with a steep ascent as current is starved under conduction threshold. In blue, we plot a family of curves which refer to fixed values of V_{Gp}={500 mV, 570 mV…} and vary V_{Bp}. The results confirm the above observation and reveal another important effect: careful combination of gate/body biasing can lead to obtaining a segment of the delay range that refers to an almost linear part of the curve. To elaborate this, we can assume a gate voltage near 500 mV as seen in the bottom plot of Figure 4-16. For this setting, the delay versus the body bias variation provides a high correlation with a linear function, as well as a very fine-tuning capability.

c) Prototype delay line architecture

To fully investigate the topology and the control flexibility that body biasing offers, a prototype delay line was designed and fabricated. The regular-Vt transistors of the first stage current-starved inverter were laid out in twin and triple-well arrangements to ensure isolation. The imposed constraints of well spacing lead to an overall unit delay element area of 3 µm x 7 µm. The well arrangement is shown in Figure 4-17.

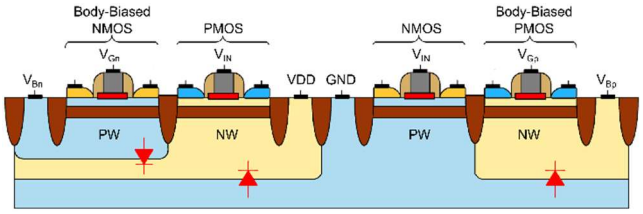


Figure 4-17 Well arrangement layout accommodating the body biasing stage.

The delay line design involves a cascade of granular cells organized in groups, as seen in Figure 4-18 (a). Group size was optimized based on the granular delay range to guarantee minimum overlap when programming a delay value. Each group is associated with a tap output to facilitate programmability. For this purpose, all tap output nodes are connected to a common bus. Control of the bus is carried out with an 11-bit thermometer-coded word that activates the selected output.

To minimize power consumption, a local power-down scheme is established for the delay groups that are not active for a given delay value. This is realized using Lead cells (indicated as L in Figure 4-18 (b)), which are placed between groups. Their function is to enable the output of the last active group and propagate a steady-state to the remaining ones. The logic is shown in Figure 4-18 (c).

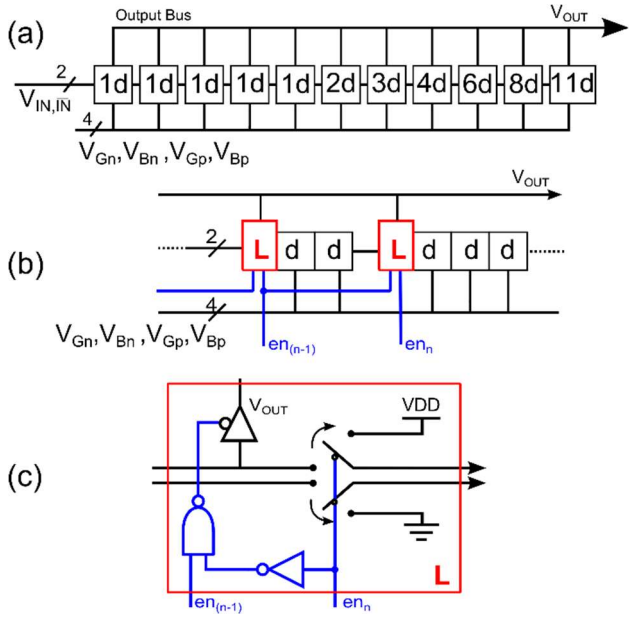


Figure 4-18 (a) Delay line architecture. (b) Inter-group transition and delay-line output is implemented with Lead cells. (c) Lead cell logic.

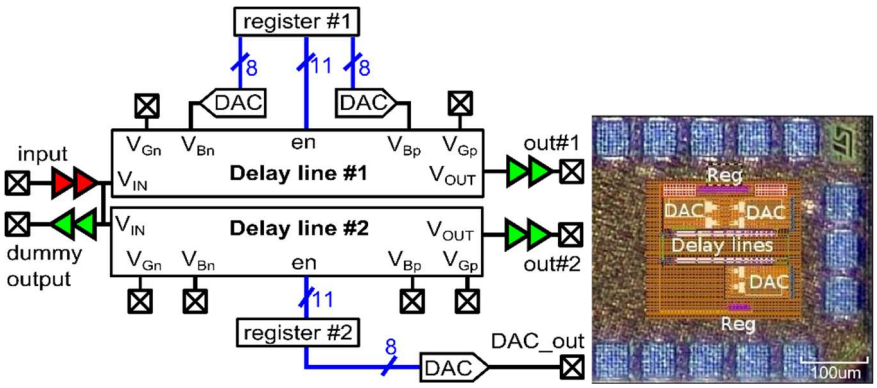


Figure 4-19 On-chip delay line test bench top level diagram (top) and chip photograph (bottom) with layout inset. Metal fill obscures metallization.

The prototype chip was fabricated in 28 nm FD-SOI technology from STMicroelectronics. The top-level block diagram and chip photograph are shown in Figure 4-19. It comprises two delay lines: one with external analog control of body biasing and one with digital, through on-chip 8-bit R-string DACs. A dummy output was used to de-embed the delays coming from pad drivers and external routing. The delay lines were designed with independent power supplies to permit direct power consumption measurements. The delay line control words and on-chip DAC inputs were provided from custom on-chip control registers. To perform the measurements, a test-bench was built with the die being wire-bonded on a PCB. The on-chip control registers as well as on-board DACs used for generating gate and body bias signals were programmed though the USB port of a PC, using a serial programming interface.

d) Measurement Results

The good functionality of the delay line under different control scenarios was verified. Various measurements of rising and falling edges were performed in different rates up to 2 GHz. Figure 4-20 presents the variation of delay for a fully active line with body biasing applied over a range of 1.6 V, both for rising and falling edges. The coarse/fine character is illustrated. Another scenario entailed activating consecutively the delay groups to characterize the complete line programmability. Rising edge delay range is measured under fixed gate biasing: V_{Gn}=400 mV, V_{Gp}=600 mV. Keeping V_{Bp}=1 V, this scenario involved activating stages incrementally and varying V_{Bn} body biasing between 0.2 V and 1 V. These are the limits between inter-well junction diode inversion and nominal supply. The delay versus the programming vector, up to activating all stages, is displayed in Figure 4-21.

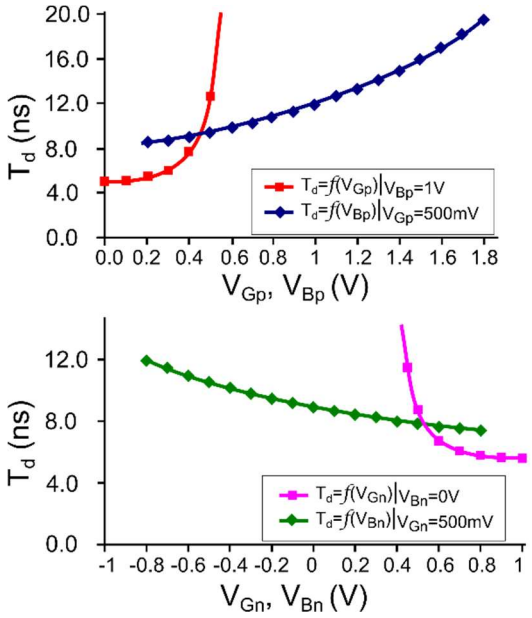


Figure 4-20 Falling (top) and rising (bottom) edge delay measurements. The fine control character of body biasing is verified.

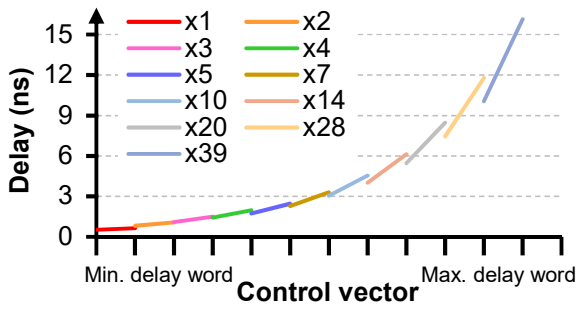


Figure 4-21 Rising delay of the delay elements vs. control vector (1 to 39 activated cells) at minimum and maximum values of body bias. The curve shape reflects group sizing.

The performance results are summarized in the second column of Table 4-2. “Minimum coarse sensitivity” refers to the minimum variation of delay achievable with enabling only the first group, while “minimum fine sensitivity” refers to varying body biasing at this setting. The “Maximum Delay” field refers to the general gate and body biasing extremes and verifies the known wide-spanning capabilities of a thyristor-type delay.

Moreover, granular delay characterization was pursued through multiple measurements of stage by stage activation to de-embed lead cells and output drivers. The results refer to a scenario of rising edge delays under V_{Gn}=V_{Bn}=500 mV, V_{Gp}=0 V and V_{Bp}=1 V. The measured control sensitivity is 50 fs/mV and energy efficiency 12.5 fJ/event. As delay range trades-off with sensitivity, even smaller sensitivity can be obtained if required by the application.

Comparison with the state of the art is done in Table 4-3. The advanced FDSOI CMOS node and the unique body control scheme mitigate the use of extra hardware, such as current sinks, which impose a static consumption overhead. This way the lowest reported power consumption is achieved.

Table 4-2 Performance summary

This work	**Delay line**	**Granular delay**
Nominal delay range (2 GHz input)	530 ps –16.13 ns	110 ps – 500 ps
Min. coarse sensitivity	120 ps/mV	600 fs/mV
Min. fine sensitivity	150 fs/mV	50 fs/mV
Max. delay	170 ns	4.5 ns
Efficiency	668 fJ/bit	12.5 fJ/bit
Area	980 um^2	21um^2

Table 4-3 Delay element comparison with the state of the art

Ref.	[14]	[12]	[15]	**This work**
Tech. node	0.35 µm	90 nm	65 nm	28 nm FDSOI
Supply	3.8 V	1 V	1 V	1 V
Delay range	4 µs - 22 ms	5 ns - 1 µs	95 ps - 250 ps	110 ps - 4.5 ns
Control	Current sink	Gate voltage	Current sink	Gate/Body (coarse/fine)
Minimum control sensitivity	100 kHz/µA (osc)	40 ps/mV (est.)	N/A	< 50 fs/mV
Power	< 120 pJ/event	50 fJ/event	40 fJ/event	12.5 fJ/event

4.2.4. Conclusion and perspectives

This subsection has presented the results of a study of decision feedback equalizers operating in continuous-time for what concerns the tap cancellation scheme. The conclusion is that energy can be gained from many reasons:

- Removing clock distribution networks and drivers
- Allocating taps where needed (5 taps are enough for correct bit error rate)
- Consuming only when the signal is active

A prototype chip has been designed, fabricated and measured. It has implemented a configurable digital delay line, that leverage the use of the 28nm FDSOI technology. The main outcome is that delays from 500 ps up to 16 ns can be created using coarse control for long delays and fine control through the back gate for precise resolution when required. This state-of-the-art result has been published in [8].

4.3. Subsampling of mmW signals

4.3.1. Introduction

60 GHz radio is the most promising candidate for high data rate short range wireless communications targeting the delivery of uncompressed high-definition video and fast downloading. The frequency plan used in the 802.11ad standard is composed of four channels of 1760 MHz bandwidth in the 8 GHz wide unlicensed band around 60 GHz. As integration into battery-operated mobile devices is targeted and power consumption is of concern, the low power version of the 802.11ad standard is addressed with a single carrier (SC) block transmission and modulation from binary phase-shift keying (BPSK) to quadrature phase-shift keying (QPSK).

To address this type of radio, the study presented here investigates the use of subsampling in 60 GHz receivers. A subsampling architecture has been proposed and a 28 nm LP CMOS chip has been designed and measured, demonstrating the potentialities of the approach.

This subsection will first draw the context and state-of-the art in a first part. A second part will quickly detail the demonstrator architecture, the chip implementation and the test setup. In the results and discussion part, measurements of the test chip are presented.

4.3.2. 60 GHz receiver architecture

Recent research on RF receivers in the low GHz range has focused on low cost, low power and reconfigurable solutions, using sub-sampling receivers as an attractive solution in terms of area and power consumption [16], [17]. Pushing these concepts for 60 GHz communication systems, a system-level study for a receiver including an IF subsampling stage has been proposed in [18] in which an arrangement of the frequency plan allows embedded anti-alias filtering. We then propose a 28 nm CMOS implementation of an IF subsampler suitable for heterodyne 60 GHz receivers. A simplified representation of the complete 60 GHz receiver including the proposed architecture is shown in Figure 4-22. First, the RF signal is amplified and down-converted to a fixed 21.12 GHz IF frequency. The signal is then demodulated and down-converted to baseband data using a 7.04 GHz subsampling clock frequency. In 60 GHz receiver state-of-the-art, heterodyne [19] and direct conversion [20] [21] radio architectures have been reported. They are referenced and compared in Table 4-4 at the end of this section.

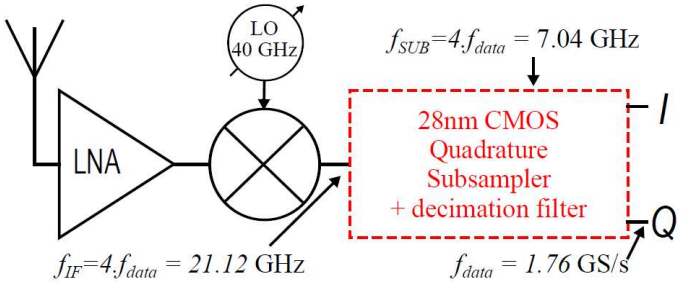


Figure 4-22 Complete 60 GHz receiver including the proposed implementation

4.3.3. Design of an IF subsampler for 60 GHz receivers

To demonstrate the proposed concept, an architecture for an IF subsampling receiver has been derived and a chip implementation has been done in 28 nm CMOS. The following parts describe this together with the measurement setup.

A schematic architecture of the proposed quadrature subsampler is shown in Figure 4-23. The reader is addressed to [18] for an extended justification of the architecture and detailed explanation of its operation. Each path (Quadrature or In phase) is composed of 4 paths (A through D, detailed in Figure 4-24) working in an interleaved scheme for continuous operation.

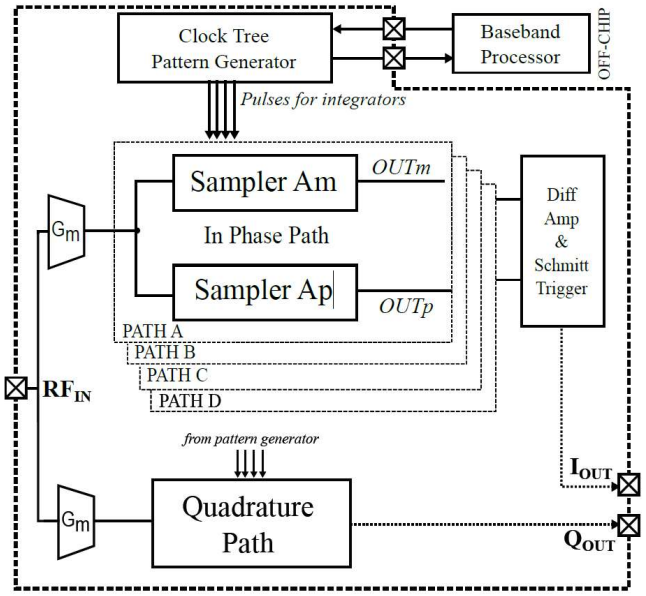


Figure 4-23 Global architecture of the proposed subsampler

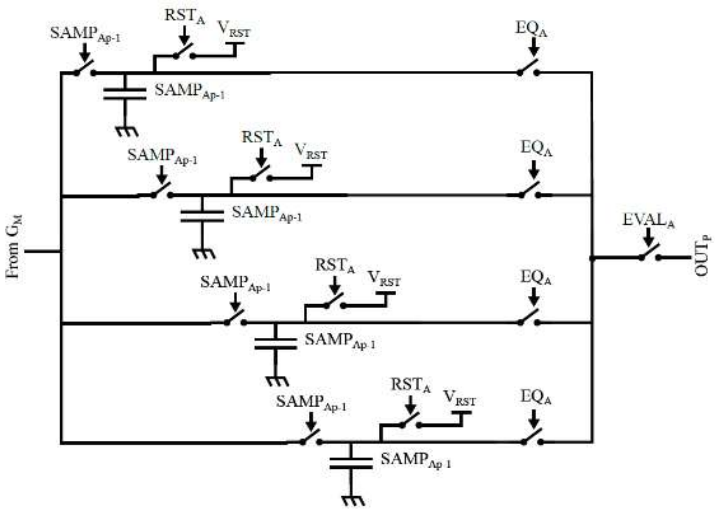


Figure 4-24 Detailed schematic of one sampler (Ap)

The integration process is performed in four phases. During the first phase, four successive samples are accumulated at the subsampling frequency (f_{SUB}) in charge domain on the positive side (sampler Ap) and four other samples are accumulated on the negative side (sampler Am). To avoid errors introduced by the finite output impedance of the Gm cell, each sample is acquired on a separate capacitor. The second phase consists of the averaging of the four values by turning the EQ switches on. During the third phase, the EV switch is activated and connects the sampling capacitors to the output differential amplifier. This amplifier acts as a buffer and introduces bandwidth limitations. When the sampling switches turn on and off, charges are injected and pumped onto the capacitors and create voltage glitches. As they appear as a common mode signal, the differential amplifier rejects these glitches. The four paths working in parallel ensure that capacitors are always connected to the differential amplifier input to avoid any undefined state. A Schmitt trigger extracts the

output data value. During the fourth and last phase, the RST switches reset the sampling capacitors.

The architecture of the clock tree is shown in Figure 4-25. The first block is common to both quadrature paths and is used for setting the global phase of the clock generator to sample the signal at the correct instant. The clock generator is divided into in-phase and quadrature phase paths to tune the parameters independently. A feedback loop allows automatic duty cycle adjustment. The delay between I and Q is finely tuned to a fourth of the period at IF frequency, based on the error rate detected by the baseband processor. Finally, coupled inverters perform the single-ended to differential conversion and feed the pattern generator which creates the correct pulses for the subsampler operation.

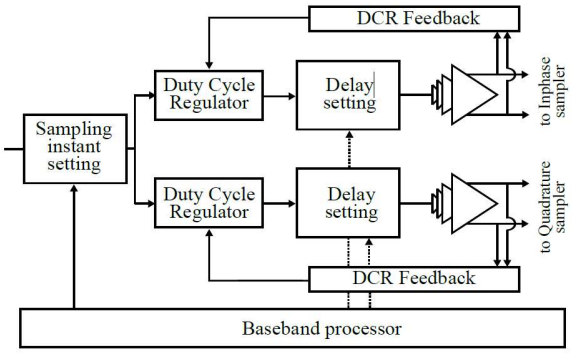
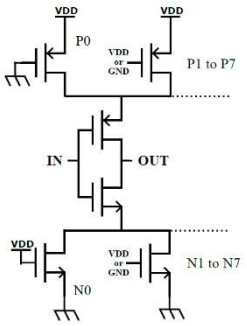


Figure 4-25 Architecture of the clock generator

In order to reach high sensitivity, the sampling instant should be set with a sub-picosecond precision [18]. This target cannot be reached simply by adding pairs of inverters because the delay of a simple loaded inverter is around 8 ps in the targeted technology. One solution is to work directly on the slew rate of the inverters by implementing digitally-controlled delay cells as shown in Figure 4-26. One path is always on because P_0 and N_0 are always active. This path defines the minimum slew rate. Activating $P_{1\text{-}7}$ or $N_{1\text{-}7}$ increases the slew rate for respectively the rising or the falling edge. After buffering, this results in a finely tunable delay. A unit delay cell is created with two slew-rate controlled inverters and is controlled by a 7-bit thermometer code. Simulations have shown that the delay increases linearly with a step of 0.47 ps in the typical corner. The steps are respectively 0.55 ps and 0.39 ps in Slow-Slow and Fast-Fast corners. In this work, three of these unit delay cells form the sampling instant setting block shown in Figure 4-25. Consequently, the ideal sampling instant can be finely reached just by modifying a digital control code on these delay cells.



Transistors sizes (L=28nm for all)

N_{INV} - P_{INV}	1u
N0 - P0	1u
N1 - P1	560n
N2 - P2	300n
N3 - P3	250n
N4 - P4	210n
N5 - P5	170n
N6 - P6	130n
N7 - P7	110n

Figure 4-26 Digitally controlled delay cells and corresponding transistor sizes

The duty cycle of the input clock should be set to 50% with a precision of 1% to create the correct sampling window. State of the art on duty cycle regulators (DCR) mainly focuses on high-speed locking solutions for low frequency clocks (up to 2 GHz). In this application, the clock frequency is higher, but the locking time is not critical. The proposed chip includes a DCR based on the slew-rate controlled inverters shown in Figure 4-26. After the clock tree, a simple RC circuit and comparators are used to monitor the time domain average of the clock signal which directly relates to the duty-cycle. Simulations have shown that the DCR can be locked with a 0.5% tolerance on the duty cycle.

4.3.4. Results and discussion

A 0.9 x 1.4 mm^2 test chip has been designed and fabricated in 28 nm CMOS process (Figure 4-27). However, the implemented test-chip is pad-limited, and the total active area is only 0.0162 mm^2. In the test setup, a BER tester generates the data streams for I and Q at f_{data} = 1.76 GS/s. A radio frequency mixer upconverts these quadrature signals and modulates them around f_{RF} = 21.12 GHz for the RF input of the system. A separate synchronized source generates the f_{SUB} = 7.04 GHz sampling clock for the system. As the output signal is a 1-bit digital stream instead of an analog baseband signal, classical measurements such as SNR or linearity cannot be done. BER measurements are performed instead.

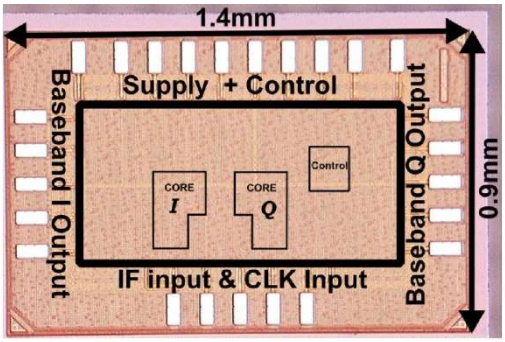


Figure 4-27 Subsampling receiver chip micrograph

Figure 4-28 shows the sensitivity of the system for BPSK and QPSK modulations. The targeted application requires a raw BER of 10^{-3}. In the BPSK test case, the BER is below 10^{-3} for input powers between -12 and 5 dBm. In the QPSK test case, the BER is below 10^{-3} for input powers between -10 and 5 dBm. The BER is limited to 10^{-4} because of interference between I and Q during the integration period.

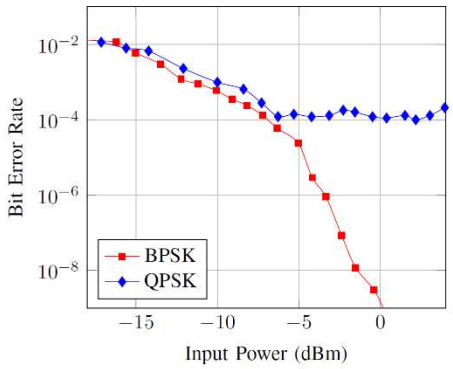


Figure 4-28 Bit Error Rate with BPSK and QPSK modulations assuming the ideal sampling instant vs input power

As described in the previous sections, the sampler should be synchronized with the RF input frequency. To do so, digitally controlled delay cells set the sampling instant. Figure 4-29 shows how this sampling instant affects the receiver's sensitivity for Pin = 0 dBm in the BPSK test case. With this configuration, 5 successive codes give a BER below 10^{-9}. Figure 4-30 shows the BER versus the sampling instant for low input powers: -12 dBm for BPSK and -10 dBm for QPSK. As expected, the sampling instant is more sensitive for the QPSK test case because I and Q leaks on each other when the sampling instant deviates from the ideal value.

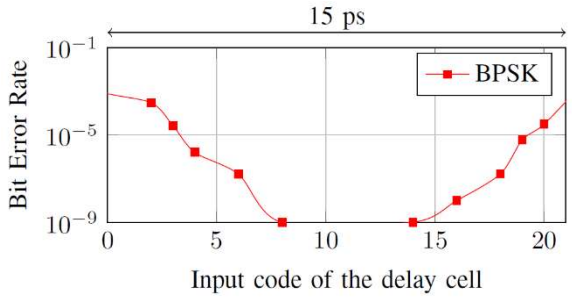


Figure 4-29 BER as a function of the sampling instant Pin = 0dBm

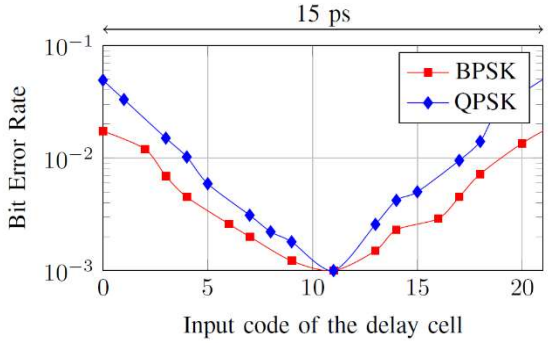


Figure 4-30 BER as a function of the sampling instant for a fixed input power (-12 dBm in BPSK and -10 dBm in QPSK)

To evaluate the immunity to blockers, the test setup is presented on Figure 4-31. The level for the channel of interest is -12 dBm providing a BER of 10^{-3}. A sine wave is added as a blocker. The power of this blocker is increased until the BER degrades to 10^{-2}. Figure 4-32 shows the allowable power for blocker frequencies from 14 to 21 GHz. It indicates the relative immunity of the system to blockers. It shows that out-of-band attenuation exists in the subsampler thanks to the charge domain subsampling and to the FIR filtering.

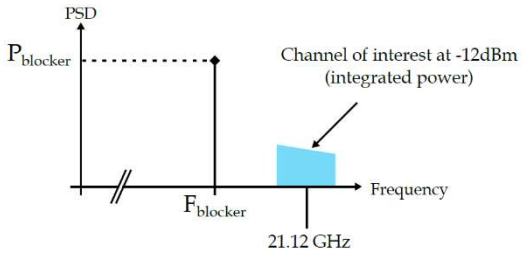


Figure 4-31 Channel of interest with a blocker

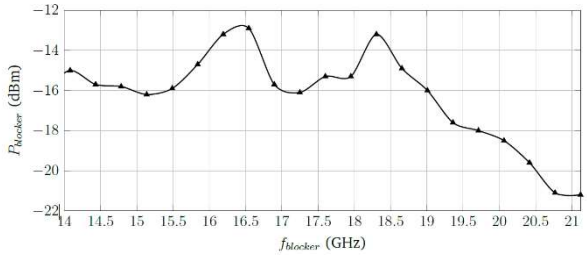


Figure 4-32 Maximum allowable power of a blocker for a 10^{-2} BER with an input signal power of -12 dBm

When demodulating data at 21.12 GHz, the power consumption of the whole system is 62 mW under 1.2 V voltage supply. The power is mainly consumed by clock buffers (52 mW) while the pattern generator and the transconductances respectively consume 6 mW and 4 mW. The power consumption is however scalable with the frequency of operation. The total power can go down to 15 mW under a 0.8 V power supply when demodulating 9 GHz input signal.

The performances of the circuit described cannot be directly compared to the state of the art because published solutions refer to complete systems from RF to analog DC while the proposed chip goes from IF at 21.12 GHz to digital baseband data after decoding. The frequency planning in [19] is similar to the one of the targeted system, and it seems therefore appropriate to use the blocks of [19] for a power consumption estimation of the complete 60 GHz receiver: 80 mW for the RF to IF part and 74 mW for the mmW PLL. The PLL in [22] is used as a reference for the low jitter clock generator at 7.04 GHz and consumes 36 mW. Consequently, for a fair comparison, the total estimated power consumption for a 60 GHz receiver integrating the proposed subsampler would reach 252 mW. Table 4-4 compares the proposed solution to complete receivers with different approaches for channel filtering: GmC in analog baseband [19], external Frequency Domain Equalizer (FDE) [20] and spatial filtering [21]. All these solutions require additional components. This work proposes to include channel filtering directly in the subsampling stage. This results in a complete system that is power efficient compared to reported receivers.

	This work	[SIL11]	[VID13]	[TSU13]
Topology	IF to DC subsampler + RF FE to IF [19] + RF PLL [22]	Heterodyne	Direct conversion	Direct conversion
Modulation	SC QPSK	OFDM 16QAM	SC QPSK	SC 16QAM
Channel Filtering	FIR + Sampler	GmC in ABB	External Equalizer	Spatial Filtering
Decoder	Integrated in sampler	8b external ADC	5b on-chip ADC	External ADC
Technology	28 nm	65 nm	90 nm (RF FE) 45 nm (FDE)	40 nm
Power Consumption	252 mW*	454 mW + ADC	274 mW (RF) + 710 mW (FDE)	584 mW + ADC (146 x 4 ant.)

Table 4-4 Comparison with different published approaches in CMOS [19]–[21].

4.4. Conclusion / Summary

This chapter has detailed the works done in targeting efficient baseband blocks for mmW receivers. The 65 nm CMOS adaptive baseband circuits designed for 60 GHz receivers can receive 10 Gb/s data with a 4.5 pJ/bit efficiency, while offering 80 DFE taps and CDR and CR adaptation loops. It opens the way to fully integrated solutions for high data-rate

receivers. Then, investigations on the use of continuous-time digital signal processing for high data rate receivers has shown that cancellation of selective taps in the DFE are sufficient to achieve decent error rates. A demonstrator comprising highly configurable delay lines has been built in 28 nm FDSOI and shows an unprecedented level of delay range and control sensitivity, combined with a very low power consumption. The last contribution concerns an experiment with direct subsampling of mmW signals. It has been shown, through a 28 nm chip, that subsampling of an IF signal at 20GHz is possible using charge subsampling techniques and that it facilitates integration of mmW receiver in advanced technology nodes, since the solution is energy-efficient and scalable.

4.5. Chapter bibliography

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Chapter 5 Perspectives and future directions

This chapter will present the future directions. It consists of two parts. The first one deals with near-sensor computing for audio processing to enable future embedded cloud-less solutions for voice activity detection and speech recognition. This is the framework on which some PhD work has been started and an ANR project called LEOPAR has been set up and will be led by Benoit Larras. The second part introduces longer-term research paths in the context of personal area networks. It extends the concepts of near-sensor computing and small-scale machine learning to body area networks and draw perspectives on human body communications, wake-up receiver concepts and integration of electronic elements in textiles.

5.1. Near-sensor computing for audio signals

5.1.1. Context

The emerging “Internet of Things” and ambient intelligence growth is faced with massive amounts of data to be transferred from connected portable devices to central computation units that process data from multiple sensors. Depending on the application, the devices communicate wirelessly the entirety of the data sets or embed generic computing resources to process them locally. Decreasing the energy consumption of the devices must be a priority to increase the battery lifetime. Since the communication interface or the embedded processor are the most energy-hungry parts of the sensor nodes, the “Near-Sensor Computing” concept aims at pre-processing the input data in order to limit either the amount of data to transmit or the number of computations in the processor.

We would like to address energy-limited embedded sensors and computation systems that address a large variety of applications. In the audio domain, applications such as voice activity detection in a noisy context, as well as more elaborate applications like vowels, words and

language recognition, can be targeted. In the healthcare domain, human-body signals (ECG, EEG, etc.) classification tasks are possible applications. Other domains, such as vibration monitoring or motion-triggered cameras can also be addressed.

A common way to achieve energy savings at the node level is to put the processing unit in standby mode most of the time and use a "wake-up" trigger signal to indicate the activity of the input signal. The system generating the "wake-up" signal is therefore active all the time but is usually composed of a simple threshold detection function and thus consumes very little energy. Consequently, the total energy consumption of the system is greatly decreased compared to the always-on case. Nevertheless, in this context, the threshold detection function reacts to the presence of any input signal, even if it does not contain useful information.

To address this problem and ensure the processor is only activated if a meaningful input is presented, a dedicated unit is inserted between the threshold detector and the processor, as illustrated in Figure 5-1. Upon activation by the threshold detector, this unit pre-processes the input signal and generates a second "wake-up" signal if the input signal contains relevant information. The pre-processor role is to extract features from the input signal and to classify them to determine their relevance. This structure is interesting as the pre-processor does specific processing, and thus consumes less energy than the main processor (or in the case of centralized computations, the amount of data to transfer through the communication interface is largely reduced). In both cases, the global energy consumption of the sensor node is reduced by many decades and is fitted to the real needs of a specific application.

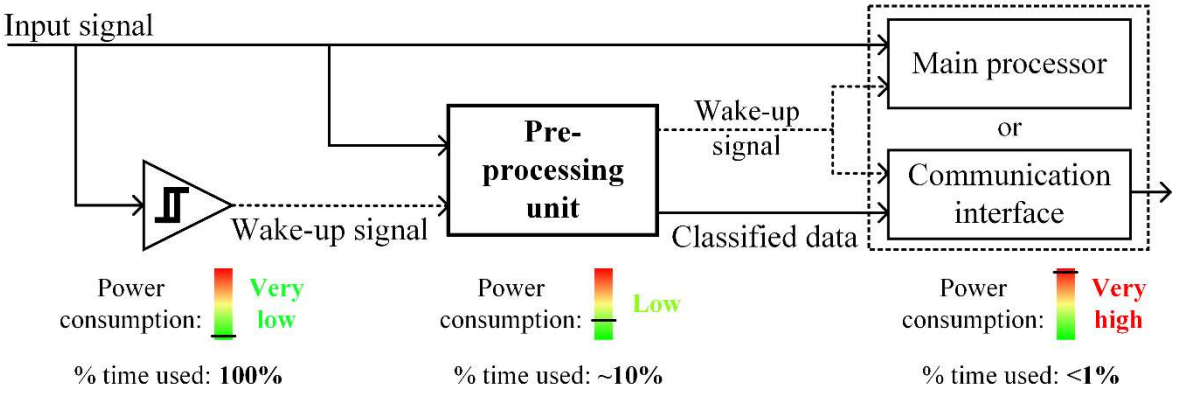

Figure 5-1 Block diagram of the 3-staged processing chain focusing on minimizing the global system energy consumption

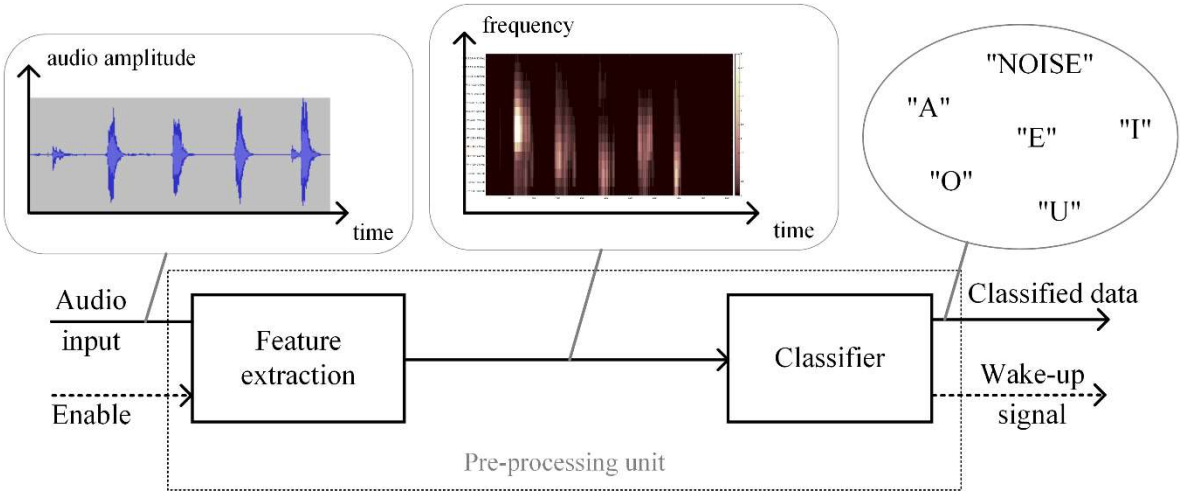

Figure 5-2 Block diagram explaining the different functions of the proposed pre-processing, applied to an audio application

In a first approach, audio applications seem to be the most promising vector of demonstrations. For these applications, the extracted features are the energy values of the frequency components of the input audio signal. By representing these features over time, a "time-frequency" diagram is formed, as shown in Figure 5-2. This diagram is specific to each input signal. The set of features is then input into a classifier, which determines if the input data belongs to a specific user-defined category. For audio applications, these categories can be "NOISE", "HUMAN VOICE", or vowel sounds, for example. Depending on the targeted application, a specific category output by the classifier can trigger a "wake-up" signal for a general-purpose processor, or it can be sent to another device.

5.1.2. State of the art in audio pre-processing units

The design of pre-processing units has been addressed in the state of the art for audio applications, as shown in Table 5. In 2016, Badami et al. propose a feature extraction block implemented by a bank of 16 analog band-pass filters [1]. The central frequencies of the filters are calibrated with the characteristic frequency compounds of the human voice. The energy in each band is extracted and a decision tree operates the feature classification. This solution achieves a power consumption of 6 µW but is not reconfigurable since the frequencies of the filters are fixed when the circuit is fabricated. Moreover, the proof-of-concept ASIC occupies a 2 mm² silicon area due to the integration of passive devices on-chip and is not scalable with the technology nodes, which is cumbersome for an embedded application. In 2018, Yang et al. propose a bank of 16 analog filters to extract audio features in [2]. The features are converted into events where the signal activity is proportional to the energy in the corresponding frequency band, allowing a decrease in power consumption down to 1 µW. The signals are then

fed into a digital binary-weighed Deep Neural Network (DNN), consuming 10 nJ to perform a classification. The corresponding ASIC occupies an area of 2.5 mm², out of which more than half is used for feature extraction. In order to bring flexibility and density in the system, feature extraction can be realized by the means of digital filters, as in the work of Wu et al. [3]. The proposed implementation integrates a bank of 72 digital filters in a chip of 0.67 mm², while allowing tuning the filter parameters. However, with a total power of 14 µW, the power per channel is higher to that in [2]. In 2013, Raychowdhury et al. implemented the pre-processing unit as a fully digital synchronous block in 32-nm CMOS technology [4]. A 512 pt FFT, followed by digital filters evaluate the energy in each of the audio bands. The system is highly configurable, but the downside is that the system digitizes the input at a high sample rate which increases the energy consumption of the system. Such a solution is therefore not suited for energy-constrained applications. Finally, a digital DNN solution is proposed for the classification in a voice-activity detection application by Price et al. in [5]. The system consumes 220 nJ per classification, i.e. 22 times more energy than in a binarized DNN for the same application. This justifies the need to decrease the system complexity, which is vital for embedded applications.

Table 5 Performance summary of state-of-the-art voice activity detection circuit implementations

	Feature extraction type	**Classifier type**	**Tech. node (nm)**	**Chip area (mm²)**	**System power (µW)**	**Energy/class. (nJ/class.)**
JSSC 2016 [1]	Analog / 16 BPF	Mixed-signal decision tree	90	2	6	-
ISSCC 2018 [2]	Analog-to-events / 16 BPF	Digital binarized DNN	180	2.5	1	10
ISSCC 2017 [3]	Digital / 4x18 BPF	-	65	0.67	14	-
JSSC 2013 [4]	Digital / 512 pt. FFT + Digital filters	Digital energy-based decision rule	32	-	300	9
JSSC 2018 [5]	-	Digital DNN	65	-	22.3	220

From this state of the art, three conclusions are drawn:

- From the comparison between the complexity of the implementations of [1]–[3], an analog-only feature extraction system lacks flexibility and is thus application-specific, and occupies a larger silicon area;
- The signal digitization increases the system power consumption since it is clocked at a higher sample rate, as shown by the comparison between the power consumption of [1], [2] and [3], [4];

- Simplifying the classification operation, e.g. replacing fixed-point weights with binary weights like in [2], allows significant decreases in both system complexity and energy consumption compared to an equivalent classifier as in [5], while keeping the system functional.

5.1.3. Proposed research directions

The proposed research directions aim at exploring innovative circuit structures in fine-pitch CMOS technologies, that leverage the benefits of both analog and digital signal processing for addressing the issues of combined configurability and silicon area occupation of the pre-processing unit while staying competitive in terms of energy consumption. The targeted hardware structure is depicted in Figure 5-3.

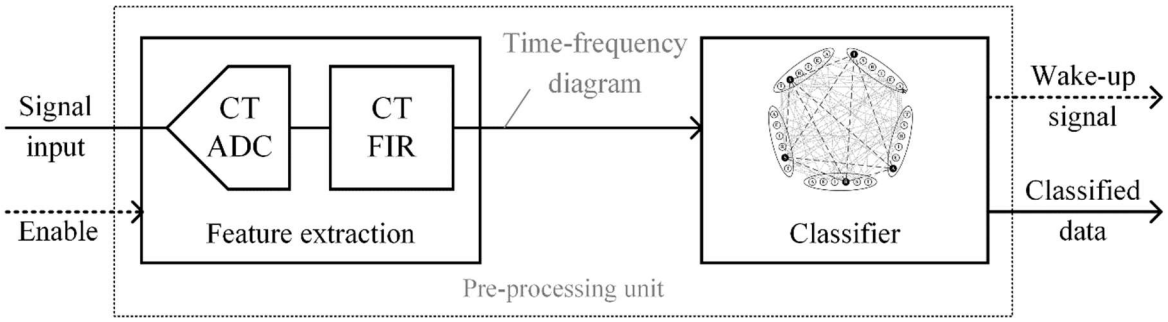

Figure 5-3 Block-diagram describing the envisioned system, in the example of an audio application

For *feature extraction*, we would like to investigate the possibility of using non-conventional event-driven digital computing. On the one hand, a digital unit would bring the flexibility and on-line configurability lacking in [1] and [2]. On the other hand, an event-driven system is clockless and its power consumption is signal-dependent, which is a key factor for signals in the kHz range like audio signals or biomedical signals. Despite event-driven systems offer the best of both analog and digital worlds, such systems are very challenging to handle and design, as it requires a different way to keep track of the signal timing. Nevertheless, fundamental building blocks such as Continuous-Time (CT) Analog-to-Digital Converter (ADC) [6] or simple Finite Impulse Response (FIR) filters [7] have been demonstrated to be integrated on-chip, while being extremely competitive in terms of silicon occupation and power consumption compared to state-of-the-art conventional designs. Moreover, configurable digital delay lines demonstrated in the research group [8] would bring the ability to propagate the signal at the right timing during the computation process, using the CMOS 28-nm FDSOI technology node. Finally, a system exploration has been started in the frame of the Ph.D. thesis of Angel Gonzalez

and a student project. It has already been shown in [9] that a reduced hardware is compatible with an accurate detection of features. An 8-bit ADC associated with an 8-filter bank and a 6-bit energy resolution provides a system-level accuracy of about 90%. The objective is to demonstrate a minimal-hardware event-driven solution to simple and efficient feature extraction of audio signals.

For *classification*, the effort will be made on studying highly-integrated specific neuro-inspired solutions. A first attempt with the work of Matteo Causo has led to an FPGA demonstration of an unsupervised learning with a Bayesian HMM (Hidden Markov Model) GMM (Gaussian Mixture Model) [10], but the implementation stage of specific blocks is very challenging to meet the ultra-low power requirements of this type of system. Next, neural networks with spiking-based neurons could be an interesting option, especially when implemented in recurrent neural networks. Neuron models, such as the one developed at IEMN [11], offer great opportunity for low-power operation (4 fJ/spike) and integration into advanced CMOS technologies. Finally, the recent arrival of Benoit Larras as an Associate Professor in the group opens some interesting research paths, notably supported by ANR JCJC (Jeunes Chercheurs - Jeunes Chercheuses) LEOPAR project. The LEOPAR project will explore the opportunity to use integrated associative memories. Previous works have demonstrated an energy-efficient clique-based neural network implementation [12]. It combines low-energy consumption brought by simple analog functions and the robustness of digital connections between the neurons. Network flexibility and energy consumption in the hundreds of picojoules range for the complete convergence of the system has been demonstrated in [13]. However, numerous challenges remain, such as designing the correct topology for the network, i.e. the adapted number of neurons needed, as well as the adapted activation function for the neurons. The final objective of the LEOPAR project would be the design and fabrication of a complete energy-efficient “wake-on-feature” demonstrator, including a pre-processing unit prototype ASIC in advanced CMOS technologies, able to prove the effectiveness of the global proposed scheme, i.e. real-time extraction of characteristic features of audio signals using non-conventional techniques such as event-driven digital processing and associative memories. The global focus is the decrease of the global energy consumption of a sensor node by several decades. Target numbers for the proposed groundbreaking integrated circuit structures are an average consumption lower than 1 µW, an energy consumption for a single classification of less than 1 nJ, a silicon area of less than 0.5 mm² and a latency of less than 1 ms while adding configurability to address many applications.

5.2. Circuits and Systems for Personal Area Networks

5.2.1. Context

Previous decades have seen the integration of many functions into smartphones. By centralizing these functions into a single device, it has provided large economies of scale and replaced many handheld devices, such as cameras, video recorders, portable music players, ebook readers, calculators, voice recorders, radios, GPS, flash lights, levellers, scanners, compasses, portable gaming devices, barcode scanners, alarm clocks, timers, guitar tuners and even compact mirrors. This list is not exhaustive, and many other devices can be thought about. The evolution of systems will rely on an increase in local computing power and ubiquity of over-the-air internet connections. Cloud computing, where the computations happen online instead of on a computer, will progressively be replaced with edge computing, since smaller and smaller devices will have greater and greater processing power. So, instead of smartphones in our pockets as our single, do-everything devices, we will have Personal Area Networks (PANs) in the form of clusters of devices worn on different parts of our bodies or around us. Distributed sensors in clothing, around the body or implanted in our bodies will continuously share information with central computation units in the form of tiny devices (watches, belts, coins, bracelets, frame of eyeglasses…). Voice seems to be an inevitable input to the system, as seen today with personal assistants, and displays would benefit from advances in augmented reality (AR) integrated in eyeglasses or contact lenses. Additionally, any connected object in the proximity of a person is considered a wearable device, and hence is an inherent part of the network.

This concept is introduced as the Human Intranet by Jan Rabaey at the Berkeley Wireless Research Center [14]. This is an “open scalable platform that seamlessly integrates an ever-increasing number of sensor, actuation, computation, storage, communication and energy nodes located on, in, or around the human body acting in symbiosis with the functions provided by the body itself. Like the Internet, the Intranet develops organically as a heterogeneous mesh of connected nodes (wired or wireless), collaborating to deliver services in a guaranteed way notwithstanding the stringent environmental, energy and size constraints.” The Human Intranet is part of a much wider concept described as the swarm in [15], which consists of more and more connected objects, where any item would be a source or a destination of information. It will make our environment smarter, offering new possibilities and applications to the end users,

enabled by the amount of data available, the different layers of computation implemented and the number of actuators accessible.

A major technological obstacle is battery life, so battery technology will need to improve, and in parallel, the power-consumption demands of the devices will need to become more efficient. So ultra-low power devices need to be designed and concepts such as wake-up receivers make a lot of sense in this environment. The topology of the network of nodes is also crucial to provide efficient sensing, computations, and communications. A flexible and hierarchical structure is preferred. At the sensor node, we need to offer local dedicated low-energy signal processing. At the local aggregation node (usually called hub), local data fusion and small-scale classification can be performed, while communication of the meaningful information or decision on an action to take or display information should happen at the master node. Contextual modelling and analysis of the network is mandatory to achieve system efficiency at the system-level and node-level. It is also required to offer flexibility, allowing to add (or remove) new devices to the network without having to reboot the entire system.

As integration of the nodes, the network topology, overall low power consumption and energy efficiency are key factors to reach the expectation of a potential end user, I want to establish here few research paths that have been identified and described these shortly.

5.2.2. Human body communications

Reliable and energy-efficient Human Body Communications (HBC) should be investigated. Using the body as a vector to propagate signals more efficiently is one of the target of Robin Benarrouch's CIFRE thesis in the frame of a collaboration with STMicroelectronics and UC Berkeley.

Body Coupled Communications (BCC) for PANs was described in [16]. Three main BCC mechanism are detailed in [17]. They consist in galvanic coupling, magnetic resonance and capacitive coupling. Magnetic resonance option was weeded out due to its bulkiness. Galvanic coupling suffers a greater attenuation, a limited data rate, this option was also crossed out. Capacitive coupling offers a few advantages to establish a communication over the body. It offers lower attenuation at higher frequency (compared to galvanic coupling) allowing wider bandwidth, higher data rate and longer range [17]. As an example, data rates of 80 Mb/s were achieved in [18] and [19]. Even if capacitive coupling benefits a lower attenuation at higher frequency than galvanic, all the research performed to this day stay below 200 MHz for

attenuation purposes. Our objective is to increase the bandwidth at a higher frequency to increase the overall data rate in order to improve the energy efficiency and shorten the communication duration. The mechanism is described in Figure 5-4. It works as follow: a "skin-electrode" is applied on (or in close proximity to) the skin and is the source of the signal. A second electrode, referred as the "ground electrode" is left floating, usually stacked on top of the skin-electrode. The excitation signal creates a non-directional electric field that propagates through the body. The receiver topology is similar to the transmitter. The circuit is closed by the "return path", capacitively coupling the ground electrode to a reference plane (usually the earth).

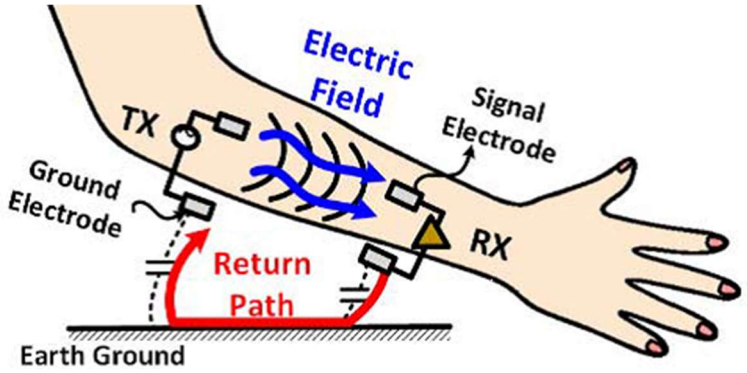

Figure 5-4 Capacitive coupling mechanism for BCC (from [17]*)*

Towards demonstrating a TX-RX efficient communication on the body, a first step will be to characterize the channel with in-situ measurements using dedicated sub-GHz radio boards and confirm the measurements with body-wide electro-magnetic simulations. Further on, integrated circuits comprising the main functions will be designed and fabricated in advanced CMOS technologies.

A way to improve energy efficiency from a system point of view is to introduce wake-up receivers. Its purpose is the detection of a wake-up beacon, allowing the main radio to stay in a deep sleep mode to lower its consumption. The efficiency of such an architecture lies in the difference of power consumption between the main radio and the wake-up receiver: the greater the better, as demonstrated in [20]. The wake-up receiver can be divided in two categories: Always-on wake-up receivers and duty-cycled wake-up receivers. The efficiency of the second approach is dependent on system parameters such as the duty cycle, the width of the listening window, the intensity of the traffic or the structure of the wake-up phase [20]. If a duty-cycled wake up receiver could be synchronized with the other nodes it communicates with, it would

become even more profitable. Unfortunately, the synchronization approach may cost more, in terms of energy required for the synchronization, than the benefits it brings.

Keeping in mind that this network is dedicated to and will be deployed on a human body, we identified the heart rate as being a global shared signal, potentially usable as a main activation clock for all nodes. It is available all over the body and its frequency follows the physical activity without any cost for the network. The details of such a synchronization mechanism is detailed in Figure 5-5. The timing diagram illustrates that all the nodes wake up simultaneously on a heartbeat event. A node selection is performed, allowing the others to go back to deep sleep mode, and the communication is established. We would like to investigate the added-value of such a mechanism, with regards to the power consumption of an analog front-end to detect the heart beat and generate a wake-up event, compared to the power of the main radio. In the literature, an analog front-end for heartbeat timing extraction implemented in 0.18 µm CMOS consumes 60 nW in [21]. In [22], arrhythmia monitoring is performed in a 65 nm CMOS chip using a 12.5 nW analog front-end (LNA + SAR ADC). These numbers are very relevant compared to the power of always-on wake-up receivers (>1 µW) and might be comparable to those of duty-cycling control systems while largely simplifying the connection process.

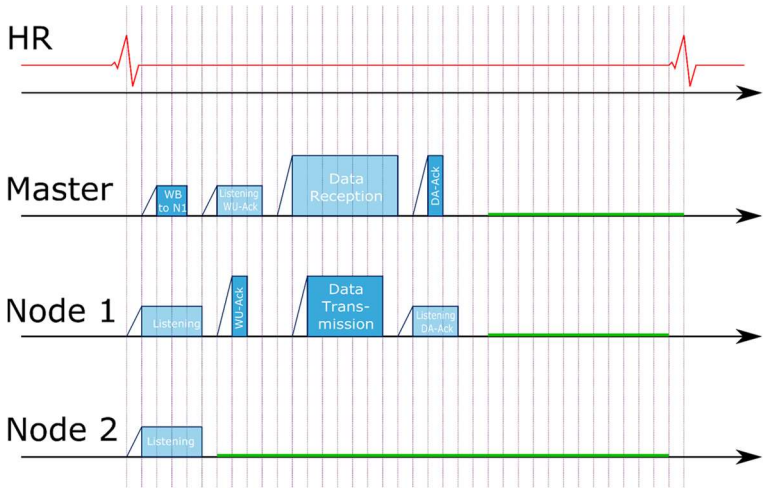

Figure 5-5 Timing diagram of a heartbeat driven communication between a master node and two slave nodes

Finally, privacy and security are mandatory in human body communications. We need to explore innovative ways of securing communications while keeping energy consumption at its lowest. For example, specific signatures from biological signals might be common at different spots over the body and might be used to encrypt the internal communication between nodes.

5.2.3. Near-sensor computing and machine learning for Body Area Networks

In this context of distributed sensors in personal area networks, designing smart nodes embedding energy-efficient communication, near-sensor processing and machine learning open the perspective to (i) extract meaningful and contextual information from the fusion of sensor signals, (ii) reduce considerably the communication overhead, thus improving the system efficiency and (iii) enhance privacy using local signal conditioning.

A first research path is to leverage FDSOI technology for the design of clock-less event-driven signal processing for specific types of sensors (audio, ECG, accelerometers, physiological, biological, humidity, tactile, pressure, contact, etc…). The concepts have been studied for audio signals in the frame of the PhD work of Angel Gonzalez but should be extended to other type of sensors. As an example, existing works on ECG sensors [23] show the advantage of event-driven ADC and QRS detection over traditional approaches. As well, a level-crossing ADC and asynchronous digital classifiers are introduced in [24] to create a wake-up circuit activated on a specific pattern.

The second research path deals with investigations on near-sensor small-scale fusion and classification unit using neuro-inspired architectures, such as clique-based networks, long short-term memories or binarized neural networks. We envision a modular demonstration platform for the integration of AI concepts directly at the sensor level, to be applied for many applications. Differentiating from centralized and energy-consuming machine learning algorithms, typically in the cloud, the goal here is to addresses edge computing for body area networks and aims to integrate efficient small-scale sensor fusion and classification engine into energy-limited sensor nodes using 28nm FDSOI technology.

5.2.4. Connected textiles

Integration of electronic devices in textiles seems to be of great interest for PANs, since everybody is wearing clothes most of the time. Many demonstrations have been made over the last few years, for example for sports or health-related monitoring, Using the textile threads as conductors, sensors or source of energy is a concept that we are investigating in a BPI-funded project called AUTONOTEX that plans to enable the future industrial sector in connected

textile in France. We are collaborating with fabric manufacturers, industrial textile groups such as Eminence or Mulliez-Flory, technical companies for interconnect solutions and IoT platform development, as well as academic research centers, to provide end-to-end solutions to enable the future of electronic-based textiles. Main challenges are in the miniaturization and flexibility of the electronic devices, the interconnections with the textile and the autonomy of connected textiles from sources such as piezoelectric-based multi-component fibers. As an illustration, flexible sensors have been developed to fit in a connected secure sheet for disoriented patients in hospital to track activity (Figure 5-6).

Figure 5-6 Example of a flexible sensor node developed in the AUTONOTEX project for integration into a secure sheet that tracks patient activity.

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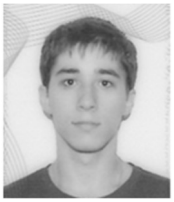
Chapter 6 Professional activities

6.1. Student mentoring

6.1.1. Supervision of M.Sc. students

The following students have made an internship in the ICD research group under my supervision:

Guillaume Rembert
"RF Digital-to-Analog Conversion for Space Applications"
Collaboration project with Thalès Alenia Space - 2010
Guillaume is now Director at Euryece Telecom, France



Răzvan Cristian Marin
"WiFi / WiGig configurable receiver back-end using subsampling demodulation"
Erasmus scholarship - 2013
Cristian has continued towards a Ph.D. degree obtained in 2017
Cristian is now Analog RF Design Engineer at Ericsson, Sweden

Other graduate students were hosted for short periods of time in the lab for specific projects:

- Florian Thorey has done a summer internship in 2009 on the optimization of a sample rate converter architecture and RTL design for FPGA implementation.
- Naoyuki Sakamoto from the University of Tokyo visited the lab for a month in 2014 for performing measurements and characterization of devices for the wireless drive of MEMS actuators. His work has been presented at Transducers 2015 [CI23].
- Mihai Marin from Politehnica Bucharest visited in 2015 for performing measurements on an integrated DAC that he designed in the frame of his Ph.D. work.

6.1.2. Supervision of Ph.D. students

Jonathan Muller
"60 GHz Transmitter with software defined radio capabilities"
STMicroelectronics CIFRE Ph.D. in collaboration with UC Berkeley, CA, USA
Defended September 20th, 2011, University of Lille.
Thesis director: Andreas Kaiser – Industrial supervision: Andreia Cathelin
Co-supervision: Ali Niknejad and Antoine Frappé
Jonathan is now Analog Designer at Semtech, Switzerland

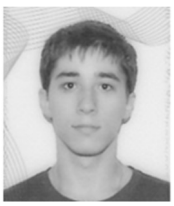
Arnaud Werquin
"Multiple rates multiple paths wideband digital transmitter with low spurious emissions applied to opportunistic radio"
Defended June 27th, 2013, University of Lille
Thesis director: Andreas Kaiser – co-supervision: Antoine Frappé
Arnaud was Engineer in Analog/IC Design at Samsung, UK in 2013 – 2014
Arnaud is now Senior Staff Engineer in RF Design at Mediatek, UK

Baptiste Grave
"Subsampling techniques applied to 60 GHz radio receivers in 28 nm CMOS technology"
Defended December 19th, 2013, University of Lille.
Thesis director: Andreas Kaiser – co-supervision: Antoine Frappé
Baptiste was Postdoctoral Scholar at Stanford University, CA, USA in 2014 – 2016
Baptiste is now Senior Engineer at Qualcomm, Ireland

Ilias Sourikopoulos
"Continuous-time digital processing techniques applied to channel equalization for low-power millimeter-wave communications"
Ph.D. co-funded by STMicroelectronics and IEMN
Defended December 14th, 2015, University of Lille.
Thesis directors: Andreas Kaiser and Laurent Clavier – co-supervision: Andreia Cathelin and Antoine Frappé
Ilias is now Postdoctoral Researcher at IRCICA, France

Fikre Tsigabu Gebreyohannes
"Scalable digital-to-RF processor for multi-standard and multi-band low power wireless transmitter in 5 GHz and 60 GHz"
Defended December 19th, 2016, University of Lille.
Thesis director: Andreas Kaiser– co-supervision: Philippe Cathelin, Antoine Frappé
Fikre is now Postdoctoral Researcher at LIP6, Sorbonne University, France

Matteo Causo
"Neuro-inspired energy-efficient computing platforms"
STMicroelectronics CIFRE Ph.D. in collaboration with UC Berkeley, CA, USA
Defended January 4th, 2017, University of Lille.
Thesis director: Andreas Kaiser – Industrial supervision: Andreia Cathelin
Co-supervision: Jan Rabaey and Antoine Frappé
Matteo is now a Postdoctoral Researcher at CEA-Leti, France



Răzvan Cristian Marin
"Highly parallel digital RF transmitter with switch-mode power amplifier and embedded band filter in 28 nm FD-SOI CMOS"
Ph.D. co-funded by STMicroelectronics and Région Hauts-de-France
Defended November 23rd, 2017, University of Lille.
Thesis director: Andreas Kaiser – co-supervision: Andreia Cathelin, Philippe Cathelin and Antoine Frappé
Cristian is now Analog RF Design Engineer at Ericsson, Sweden

Dipal Ghosh
"Low-power mm-wave wireless transceiver for high-speed inter-chip communications"
Thesis started in October 2015, University of Lille
Thesis director: Christophe Loyez – co-supervision: Antoine Frappé

Angel de Dios Gonzalez Santos
"Continuous-time digital signal processing in 28 nm FD-SOI CMOS"
Ph.D. co-funded by STMicroelectronics and Région Hauts-de-France / FEDER
Thesis started in January 2017, University of Lille
Thesis director: Andreas Kaiser – co-supervision: Philippe Cathelin and Antoine Frappé

Robin Benarrouch
"Wireless Hubs for the Human Intranet"
STMicroelectronics CIFRE Ph.D. in collaboration with UC Berkeley, CA, USA
Thesis started in August 2017, University of Lille
Thesis directors: Andreas Kaiser and Andreia Cathelin
Co-supervision: Jan Rabaey and Antoine Frappé

6.1.3. Supervision of post-doctoral researchers and research engineers

Pietro Maris Ferreira
"Design of digital-to-RF converters in CMOS 28 nm for 60 GHz applications"
ENIAC MIRANDELA Project 2012 – 2013
Pietro was Research Assistant at the University of Lille in 2013 – 2014
Pietro is now Associate Professor at CentraleSupelec, France

Stéphane Mebaley Ekome
"Estimation of 802.11ad 60 GHz Channels for Decision Feedback Equalization"
Joint project in IEMN Communication Systems Research Department 2013 - 2014
Stéphane is now Expert in Spectrum Engineering at ANFR, France

Walid Bourennane
"IoT and embedded electronics for connected textiles"
PIAVE AUTONOTEX Project 2016 – 2017
Walid is now R&D Engineer at Saint-Gobain Recherche, France

Julien Duforest
"Embedded electronics for connected textiles"
PIAVE AUTONOTEX Project 2018 –

6.2. Teaching

6.2.1. Delivered courses

During the Ph.D. program (2004 – 2007), I have taught many tutorial classes and labs in Analog and Digital Electronics at ISEN Lille engineering school. From 2009, I have taught regular classes as an Assistant Professor at ISEN Lille. ISEN Lille curriculum is composed of 5 years after the high school diploma, which are respectively denoted CSI1/CIR1, CSI2/CIR2, CSI3/CIR3, M1, and M2. The CSI undergraduate program (Cycle Sciences de l'Ingénieur) concerns the traditional preparatory classes leading to the engineering school, while the CIR undergraduate program (Cycle Informatique-Réseaux) is a parallel track with a major in computer science.

The *Introduction to Analog Electronics* and the *Introduction to Digital Electronics* courses are also delivered to L3 (undergraduate) students at the Catholic University of Lille. The *Integrated Circuit Design using Cadence* course is simultaneously delivered to M2 students at the University of Lille.

The total volume is calculated as an approximate count of the total number of face-to-face hours with students for all years taught.

Year	Course title	Type	Level	Volume (h)
2009 – 2016	Introduction to Analog Electronics	Lec / Tut / Lab	CIR2 & L3	250
2009 – 2016	Introduction to Digital Electronics	Lec / Tut / Lab	CIR2 & L3	250
2004 –	Analog and Digital Electronics	Tut / Pro	CSI3/CIR3	> 800
2009 – 2012	Digital Electronic Systems	Tut	CSI3/CIR3	50
2009 – 2012	Wireless Technologies and Applications	Tut	M1	12
2009 – 2012	Robotics	Pro	M2	80
2013 –	Mixed-signal Circuits for audio applications	Lec / Lab	M2	180
2015 –	Integrated Circuit Design using Cadence	Lab	M2	100

Lec = Lecture / Tut = Tutorial classes / Lab = Laboratory classes / Pro = Project-based classes

Additionally, a course on *RF Transmitter Architectures* has also been delivered at Telecom ParisTech as part of a continuing education program on Cognitive and Opportunistic Radios in 2013, 2015, 2017 and 2018.

6.2.2. Student Projects supervision

The following table details the projects supervised at ISEN Lille between 2009 and 2017.

Year	Description	Level	No. of students
2007	Implementation of a UMTS TX baseband in FPGA	M1	2
2009	High-speed Full Adder in 65nm CMOS	M2	2
	Optimization of a high-speed FIR Filter in 65nm CMOS	M2	2
	Reverse engineering of an iPhone (business model, hardware, and software evaluation)	CSI3	2 groups of 5
2010	Delta-Sigma Digital-to-Analog Converter	M2	2
	A radio-controlled vehicle using capacitive sensing touch screen	M1	2
	Rotating spherical LED Persistence of Vision (POV) system	M1	2 groups of 2
2011	Study of integrated adiabatic logic cells	M2	3
	LED-based POV systems	M1	2 groups of 2
2012	Development of a digital delta-sigma modulator on FPGA	M2	1
2013	LED-based POV systems	M1	2
2014	Design of a DLL-based multi-phase clock generator in 28nm FDSOI CMOS	M1	2
	LED-based POV systems for bike wheels	M1	2 groups of 2
2015	LED-based POV systems for bike wheels	M1	2
2016	AUTONOTEX: Development of an autonomous connected safety sheet	M2*	7
	Evaluation of a µ-controller for Bluetooth-enabled textile fabric	M1	1
2017	Energy harvesting from a piezoelectric textile fabric	M1	2
	Automatic feature extraction and classification tool for speech recognition. This project obtained the 1st prize in the 'Students' category of the Yncréa Hauts-de-France Remarkable Projects selection.	M1	2

* students from ISEN Lille (major in electronics) and HEI Lille (major in textile)

6.3. National and international outreach

6.3.1. Participation in national committees

- Selection Committee member for an Assistant Professor position (Maître de Conférences) in Section 63 at the University of Bordeaux in April 2012 (President R. Quere, XLIM Limoges, France)
- Individual follow-up committee member for the thesis of Saad Boutayeb, Université Grenoble-Alpes in 2017 and 2018.

6.3.2. Ph.D. committees

Year	Name	Ph.D. thesis title	University	Role
2011	Ulf Gustavsson	From Noise-Shaped Coding to Energy Efficiency – One bit at the time	Chalmers University of Technology, Goteborg, Sweden	Opponent
2013	Arnaud Werquin	Multiple Rates multiple Paths Wideband Digital Transmitter with low Spurious Emissions Applied to Opportunistic Radios	University of Lille, France	Supervisor
2013	Batiste Grave	Subsampling Techniques applied to 60 GHz radio receivers in 28 nm CMOS technology	University of Lille, France	Supervisor
2014	Robabeh Amirkhanzadeh	High-Resolution Integrated Passive Phase Shifters for Future Wireless Communications	Victoria University, Melbourne, Australia	Examiner
2015	Dajana Danilovic	Low-power RF receiver front-end evaluation in 28nm UTBB FDSOI CMOS	Télécom ParisTech, France	Examiner
2015	Mathieu Vallet	Millimeter waves frequency synthesizer for WiFi-WiGig convergence	University of Bordeaux, France	Examiner
2015	Ilias Sourikopoulos	Continuous-time digital processing techniques applied to channel equalization for low-power millimeter-wave communications	University of Lille, France	Supervisor
2016	Fikre Tsigabu Gebreyohannes	Scalable digital-to-RF processor for multi-standard and multi-band low power wireless transmitter in 5 GHz and 60 GH	University of Lille, France	Supervisor
2017	Matteo Causo	Neuro-Inspired Energy-Efficient Computing Platforms	University of Lille, France	Supervisor
2017	Enrico Roverato	Integrated High-Speed DSP for All-Digital RF Transmitters	Aalto University, Helsinki, Finland	Preliminary Examiner
2017	Răzvan Cristian Marin	Highly parallel digital RF transmitter with switch-mode power amplifier and embedded band filter in 28 nm FD-SOI CMOS	University of Lille, France	Supervisor

6.3.3. Expertise works

- French Research Agency (ANR) www.agence-nationale-recherche.fr
  Several reviews of projects submitted to the Generic Call for Proposals and defence-related calls (e.g. ASTRID)

- Research & Technology National Association (ANRT) www.anrt.asso.fr
  Review of CIFRE Ph.D. thesis proposals (industrial thesis)

- Flanders Research Foundation (FWO) www.fwo.be
  Review of research project proposals

- IDEX Université Grenoble Alpes www.communaute-univ-grenoble-alpes.fr
  Review of a project submitted to the Cross-Disciplinary Program

- CEA Eurotalents eurotalents.cea.fr
  Review of a research project submitted to the Outgoing CEA Fellowship

- Franco-American Fulbright Commission fulbright-france.org
  Review of proposals for the Student Program
  Review of proposals for the US Scholar Program

- European Microwave Association / Yole Développement www.yole.fr
  Contribution to a white paper on mmW communication systems

6.3.4. Reviews of scientific articles

I make regular reviews of papers submitted to the following journals:

Journal paper	CiteScore 2017 / Impact Factor	
IEEE Journal of Solid-State Circuits	5.03 / 4.08	From 2010
IEEE Transactions on Circuits and Systems I: Regular papers	3.68 / 2.82	From 2010
IEICE Transactions on Communications	0.93 / 1.09	From 2011
IEEE Transactions on Circuits and Systems II: Express Briefs	2.88 / 2.45	From 2012
IEEE Transactions on Microwave Theory and Techniques	3.59 / 3.18	From 2013
IEEE Microwave and Wireless Components Letters	2.50 / 2.17	From 2013
IEEE Journal of Microelectromechanical Systems	2.76 / 2.48	From 2014
IEEE Electron Device Letters	3.70 / 3.43	From 2018

6.3.5. Membership in conferences

Conference name	Date and place	Role
IEEE NEWCAS (International New Circuits and Systems Conference)	2010, Montréal, Canada	Reviewer
	2014, Trois-Rivières, Canada	Reviewer
	2018, Montréal, Canada	Reviewer
IEEE FTFC (Faible Tension Faible Consommation)	2012, Paris, France	Reviewer
	2013, Paris, France	Reviewer
IEEE ISCAS (International Symposium on Circuits and Systems)	2014, Melbourne, Australia	Reviewer
	2015, Lisbon, Portugal	Reviewer
	2016, Montréal, Canada	Reviewer
IEEE ICECS (International Conference on Electronics, Circuits, and Systems)	2014, Marseille, France	Technical Program Committee: - Track Chair: Analog and Mixed-Signal Circuits and Signal Processing - Session Chair: Circuits and Systems for Communications - Poster Session Chair
	2016, Monte Carlo, Monaco	Technical Program Committee: - Track Chair: Analog & Mixed-Signal Circuits - Session Chair: Sigma-Delta Converters - Special Session Organizer: Advanced Concepts for Future RF and mmW Transceivers
	2018, Bordeaux, France	Organizing Committee: - Special Sessions Chair
IEEE ITS (International Telecommunications Symposium)	2014, Sao Paulo, Brazil	Reviewer
IEEE ECCTD (European Conference on Circuit Theory and Design)	2015, Trondheim, Norway	Reviewer
IEEE ESSCIRC (European Solid-State Circuits Conference)	2016, Lausanne, Switzerland	Technical Program Committee: - Track Frequency Generation - Session Chair: Frequency Synthesis Techniques
IEEE SBCCI (Symposium on Integrated Circuits and Systems Design)	2016, Belo Horizonte, Brazil	Reviewer
IEEE PIMRC (Annual International Symposium on Personal, Indoor, and Mobile Radio Communications)	2016, Valencia, Spain	Reviewer
IEEE RFIC (Radio Frequency Integrated Circuits Symposium)	2019, Boston, MA, USA	Technical Program Committee: - Sub-committee: Analog and Mixed-signal and SoCs

6.3.6. Awards

- Fulbright Grant obtained for the academic year 2008-2009 to carry research as a postdoctoral scholar at the Berkeley Wireless Research Center (BWRC), UC Berkeley, CA, USA
- Best Student Paper Award received for the paper presented at IEEE VLSI 2011 in Kyoto, Japan [CI13].
- 1st prize of the Research Council of the Catholic University of Lille obtained by Baptiste Grave (Ph.D. student under my supervision) in 2013 for his thesis research on mmW receivers.
- Qualification for the 2014 regional final of « Ma thèse en 180 secondes » competition by Ilias Sourikopoulos (Ph.D. student under my supervision).
- Yncréa Hauts-de-France 2015-2016 Outstanding Research Project for the AUTONOTEX project
- Yncréa Hauts-de-France 2016-2017 Outstanding Student Project for the M1 project on the detection and classification of audio features (OK ISEN project)

6.3.7. Organization of technical seminars

- Jan Rabaey, Donald O. Pederson Distinguished Professor, University of California at Berkeley, USA, “A Roadmap to Long-Term Brain-Machine Interfaces”, sponsored by IEEE SSCS and IEMN Axis 4, IEMN, March 2015
- Jean-Paul Bardyn, CTO Semtech, Switzerland, “IoT: The Era of LPWAN is Starting Now”, ISEN Lille, October 2016
- Amin Arbabian, Assistant Professor, Stanford University, “Scalable High-Throughput mm-Wave “Wireless Fiber” Systems”, IEMN, October 2017
- Amin Arbabian, Assistant Professor, Stanford University, “Silicon Integrated Systems for Healthcare”, ISEN Lille, October 2017

6.3.8. Involvement in national and international instances

- Since 2016, IEMN contact point for the GDR SoC2 and involvement in the international working group of the GDR SoC2
- IEEE Senior Member since 2017 (IEEE Member since 2008)
- IEEE Circuits and Systems (CAS) France Section Officer: Secretary and Treasurer

6.4. Local administrative duties and management responsibilities

- Head of the Integrated Circuit Design Research Group (2011-)
- Research group representative in the scientific department 4 of IEMN (2011-)
- Member of the ISEN Lille Research Council (2011-)
- Member of the ISEN Lille Executive Committee-at-Large (2011-2015)
- Member of the ISEN Lille Steering Committee (2015-2017)
- Member of the ISEN Lille Management Committee (2015-)
- Member of the Yncréa HDF Steering Committee-at-Large (2015-)
- Elected representative member of the ISEN Lille and Yncréa HDF Governing Board (2017-)

6.5. Collaborative projects

Throughout the years, I participated to research projects or industrial contracts, with local responsibilities or coordination. Figure 6.1 chronologically traces back the projects I was involved in since 2006 and details are given on these projects in alphabetical order. I mainly participated in European, French or US projects before 2010, while I started involving myself into co-elaborating proposals and leading work packages and tasks within this type of projects after this date. As of industrial collaborations, I have always been involved in proposing work

plans corresponding to the partner needs and completely coordinating the projects when agreed upon.

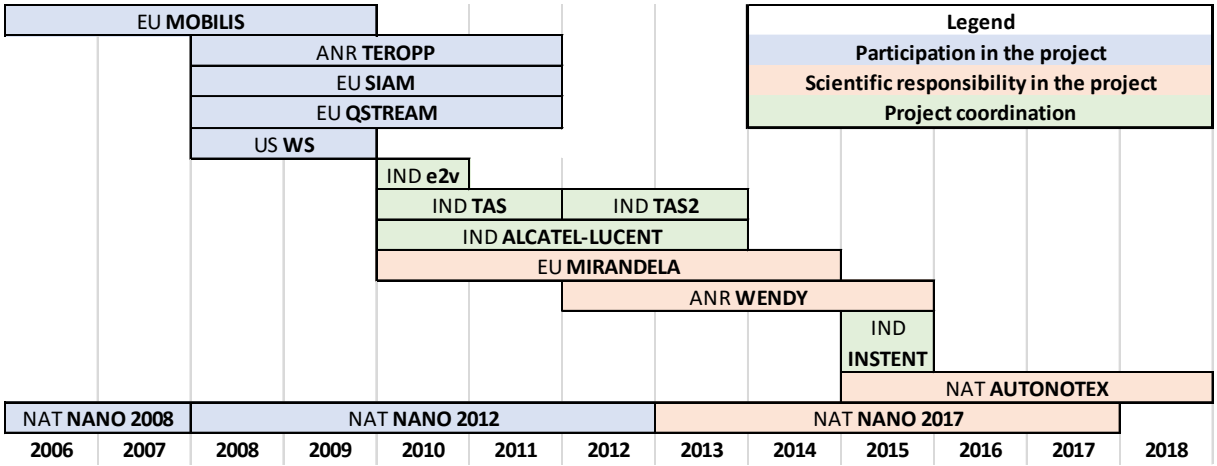


Figure 6.1 Chronology of the projects since 2006. The color code reveals the level of involvement in these projects. EU: project funded by the European Union; ANR: project funded by the French "Agence Nationale de la Recherche"; US: Project funded by the United States; IND: collaborative project with an industrial partner; NAT: project funded by French national funds.

Here is a list of the projects ordered alphabetically by acronym, including the title, partners, the type of project, my role in the project and the associated funding.

- ALCATEL-LUCENT

Title: CMOS integrated circuit design for the "Greenwave" project (Generalized Radio Emitter Enabling New Wireless Advantages Vis a vis Environment)
Type: Collaboration project ISEN / ALCATEL-LUCENT
Period: 2010 – 2013
Role: Project leader
Funding: 188 k€

- AUTONOTEX

Title: AUTONOmie énergétique des TEXtiles connectés
Type: BPI PIAVE Textile
Period: 2015 – 2018
Partners: Mulliez-Flory, Eminence, Arkema, TDV, Nicomatic, Percall, CETI, ENSAIT, IEMN, CANOE, ARMINES-ParisTech, ARMINES-Saint Etienne, IMT
Role: IEMN Partner co-leader, Work Package Leader
Funding: 412 k€ for IEMN partner

- e2v

Title: Simulation and system modeling of sigma-delta modulators
Type: Collaboration project ISEN / e2v
Period: 2010
Role: Project leader
Funding: 26.5 k€

- INSTENT

Title: Study of the integration of an ASIC on a medical stent
Type: Collaboration project ISEN / TRONICO – Instent
Period: 2015
Role: Project leader
Funding: 5 k€

- MIRANDELA

Title: Millimetre-wave and Radio-frequency integration in Nanoelectronics for Modern Wireless 5 A Communications
Type: Eniac Aeneas European project
Period: 2010 – 2014
Partners: STMicroelectronics FR (coord.), ACCM AU, Catena NL, CISC AU, IEMN France, CUAS AU, DICE AU, EPFL CH, Forth GR, Grenoble INP FR, Infineon AU, IMS FR, ISD GR, ISEN FR, CEA-LETI FR, Nokia FI, Politecnico Milano IT, Q-Free NO, SINTEF NO, ST-Ericsson BE, ST-Ericsson FI, ST-Ericsson FR, ST-Ericsson NL, ST-Ericsson UK, STMicroelectronics IT, TKK FI, TU Graz AU, UniMoRe IT, Univ Pavia IT, UPC ES, Univ Wuppertal DE, VTT FI
Role: IEMN Partner Leader, Work Package co-leader (Full Application Demonstrator), and Cluster Leader (mmW Systems and Sensors)
Funding: 243 k€ for ISEN partner

- MOBILIS

Title: Mixed SiP and SoC Integration of Power BAW Filters for Digital Wireless Transmissions
Type: FP6 IST STREP European project
Period: 2006 – 2009
Partners: IEMN France (coordination), STMicroelectronics France, EPCOS Germany, Aviza Technologies UK, CEA France, VTT Finland, UPM Spain, PUB Romania, XLIM France, IXL France, LAAS France
Role: Participant
Funding: 230 k€ for IEMN partner

- NANO 2008

Type: State support program for the STMicroelectronics – IEMN common lab
Period: 2004 – 2008
Role: Participant

- NANO 2012

Type: State support program for the STMicroelectronics – IEMN common lab
Period: 2008 – 2012
Role: Participant in the Work Package 2 on Communication Systems
Funding: 130 k€ for WP2

- NANO 2017

Type: State support program for the STMicroelectronics – IEMN common lab
Period: 2013 – 2017
Role: Co-Chair of the Work Package 2 on Communication Systems
Funding: 230 k€ for WP2

- QSTREAM

Title: Ultra-high Data-rate Wireless Communication
Type: MEDEA+ EUREKA project
Period: 2008 – 2011
Partners: NXP Semiconductors NL (coordination), IAF Germany, NXP Semiconductors Belgium, STMicroelectronics Italy, STMicroelectronics France, Technicolor France, NXP Semiconductors France, Signal Generix Cyprus, QPI Circuits NL, IMEC Belgium, Braunschweig UY Germany, TU/e NL, IMS France, IEMN France, LAAS France, ENST Brest France, TUKL Germany, CEA-LETI France
Role: Participant

- SIAM

Title: Silicon Analog to Millimeter-wave Technologies
Type: MEDEA+ EUREKA project
Period: 2008 – 2011
Partners: STMicroelectronics France (coordination), Philips Research NL, Ericsson Sweden, Signal Processing Devices Sweden, Catena NL, Acreo Sweden, CEA-LETI France, IMS France, IEMN France, Delft UT NL
Role: Participant
Funding: 430 k€ for IEMN partner

- TAS

Title: Radio Frequency Digital-to-Analog Conversion
Type: Collaboration project ISEN / Thalès Alenia Space
Period: 2010 – 2011
Role: Project leader
Funding: 20 k€

- TAS2

Title: Radio Frequency Digital-to-Analog Conversion: study on LO and image rejection
Type: Second phase of the collaboration project ISEN / Thalès Alenia Space
Period: 2012 – 2013
Role: Project leader
Funding: 5 k€

- TEROPP

Title: Technologies for terminals in opportunistic radio applications
Type: ANR P2IC (Programme Interne aux Instituts Carnot) project, 2008 - 2011
Partners: GET (coord.), CEA-LETI, CEA-LIST, C3S, IEMN, UTT
Role: Participant
Funding: 135 k€ for IEMN partner

- WENDY

Title: WiGig Flexible Transceiver Advanced System
Type: ANR INFRA (Infrastructures matérielles et logicielles pour la société numérique) project
Period : 2012 - 2015
Partners: STMicroelectronics, IEMN, IMS
Role: IEMN Partner Leader – Work Package Leader (Signal Processing and Frequency Generation TX)
Funding: 360 k€ for IEMN partner / 39k€ for ISEN Lille (preciput)

- WS

Title: Wafer Scale Distributed Radio
Type: United States DOD-AFRL (Air Force Research Lab) Grant
Period: 2008-2009
Role: Participant
Funding: $450,000 for Berkeley Wireless Research Center (BWRC)

6.6. Patents

The research carried out has been valorized through two patent applications. One is related to my Ph.D. work and has been granted and extended to the United States [P1]. A second one is related to the Ph.D. work of Arnaud Werquin and has been published internationally [P2].

Chapter 7 **Conclusion**

The closure of this manuscript is a complicated task and I would like to recall here the initial objective of the HDR diploma, as stated in the decree of 23 November 1988. The HDR "certifies the recognition of the scientific high level of the candidate, the original character of his approach in a field of science, his ability to master a research strategy in a sufficiently broad scientific or technological field and his ability to mentor young researchers".

I have tried to emphasize as much as possible these four conditions throughout the manuscript, by insisting on the novelty of the proposed technical concepts, the impact of the work, through publications in major journals and conferences in the field and actively supervising many young researchers. Evolution and scientific maturity has also been highlighted in the perspectives of my research and that of my future PhD students.

Analyzing research and actions carried in the last 15 years and writing a manuscript in a consistent way has been a great time, but the challenges are ahead of us and I want to see this work as a stepping stone to global research and a springboard to my future research projects.

Finally, one of the main results of this habilitation is the possibility of gaining greater autonomy by being able to supervise Ph.D. students as a thesis director. This is complemented by the opportunity to report on Ph.D. thesis, which is important in the academic context in France. I am very proud that I can soon contribute more intensively to the world of academic research.

Annex A **Chip gallery**

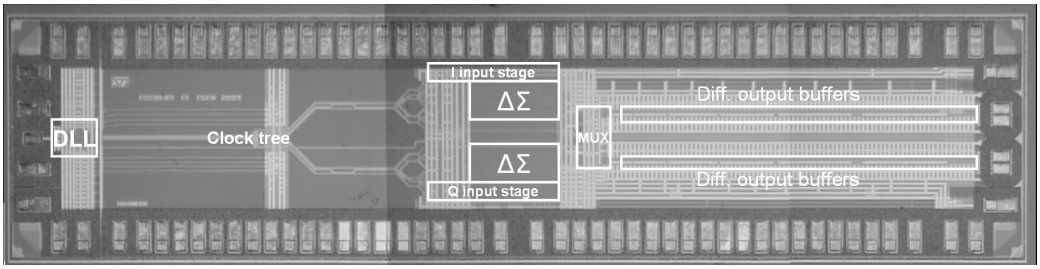
This section illustrates the integrated circuits designed, fabricated and tested within the research works described in this document. It includes a short description together with technological process, dimensions, and assembly type. A reference to the related main publication is also indicated.

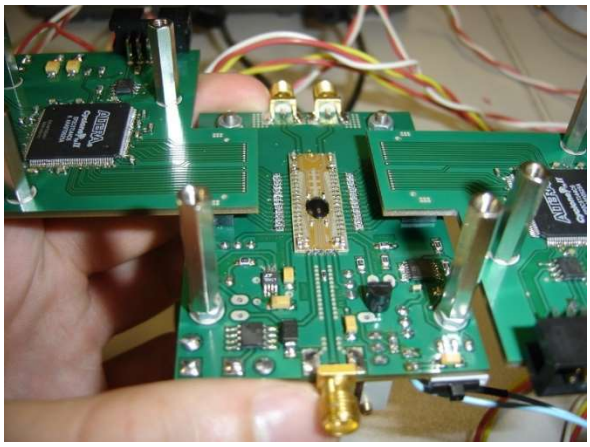
FULBERT II Digital RF signal generator based on delta-sigma modulation

STMicroelectronics 90 nm CMOS
4 x 0.8 mm²
Chip-on-board assembly on a dedicated substrate

A. Frappe, B. Stefanelli, A. Flament, A. Kaiser, and A. Cathelin, "A digital delta-sigma RF signal generator for mobile communication transmitters in 90nm CMOS," in *2008 IEEE Radio Frequency Integrated Circuits Symposium*, 2008, pp. 13–16.

Abstract: The presented digital RF signal generator in 90 nm CMOS uses 1-bit Delta-Sigma modulation and targets mobile communication terminals. A 50 MHz bandwidth centered on 1 GHz can be achieved when the circuit is clocked at 4 GHz. Signals up to 3 GHz can be synthesized when using the first image band. The peak output power into a 100 Ω diff. load is 3.1 dBm with 53.6 dB SNDR. The digital core employs redundant arithmetic, precomputed non-exact quantization and differential dynamic logic. The digital core consumes 49 mW at maximum clock frequency. Active area is 0.15 mm^2.





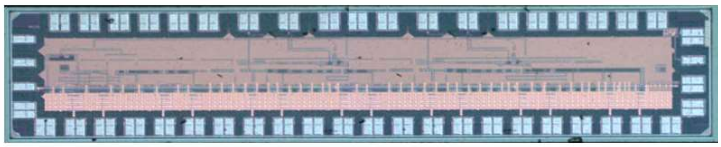
ROCCO Reconfigurable semi-digital RF-FIR filter with passive power combination

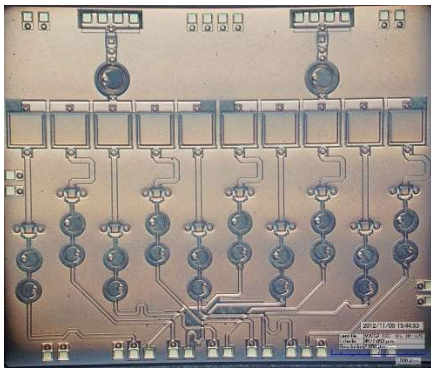
Chip:
STMicroelectronics 65 nm CMOS
2.6 x 0.8 mm²
Chip-on-board assembly on a module

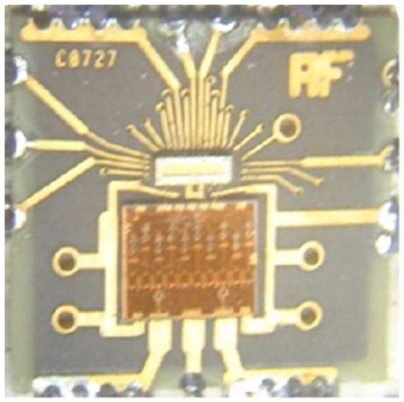
Power combiner:
STMicroelectronics IPD
3.5 x 5 mm²
Chip-on-board assembly on a module

A. Flament, A. Frappe, A. Kaiser, B. Stefanelli, A. Cathelin, and H. Ezzeddine, "A 1.2 GHz semi-digital reconfigurable FIR bandpass filter with passive power combiner," in *ESSCIRC 2008 - 34th European Solid-State Circuits Conference*, 2008, pp. 418–421.

Abstract: This paper presents a reconfigurable semi-digital RF-FIR filter suitable for digital transmitters using 1-bit ΔΣ signal generation. A transmission line based 5-channel power combiner allows both increase of output power and programmable filtering of the signal. A prototype has been built with 65nm CMOS and Integrated Passive Devices (IPD) technologies. The system exhibits a 14dB power gain for a peak power of 17dBm at 1.2GHz and an attenuation of out-of-band noise of up to 15dB. CMOS and IPD chip size are respectively 2.05mm² and 17.78mm².





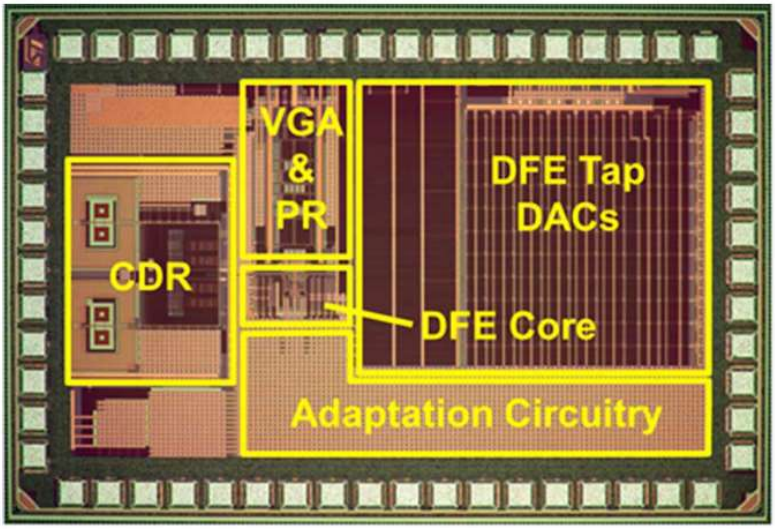


BB60 Adaptive baseband receiver for 60 GHz communication systems

STMicroelectronics 65 nm CMOS
1.7 x 1 mm²
Chip-on-board assembly

C. Thakkar, Lingkai Kong, Kwangmo Jung, A. Frappe, and E. Alon, “A 10Gb/s 45mW adaptive 60GHz baseband in 65nm CMOS,” in *2011 Symposium on VLSI Circuits - Digest of Technical Papers*, 2011, pp. 24–25.

Abstract: This paper presents a low-power adaptive 60GHz baseband in 65nm CMOS. The design integrates variable gain amplifiers, analog phase rotator, 40-coefficient I/Q decision feedback equalizers (DFEs), clock generation and data recovery circuits, and adaptation hardware. The baseband achieves 10Gb/s while consuming 53mW (DFE adaptation on)/45mW (DFE adaptation off), representing ~10X improvement in data-rate and power efficiency over prior art.

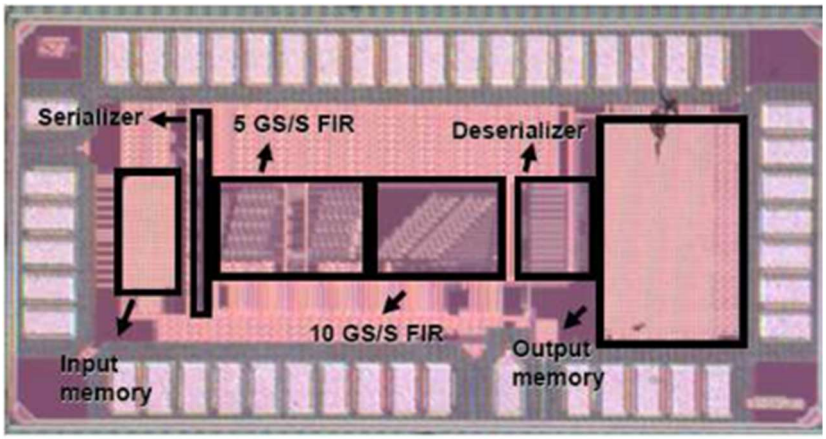


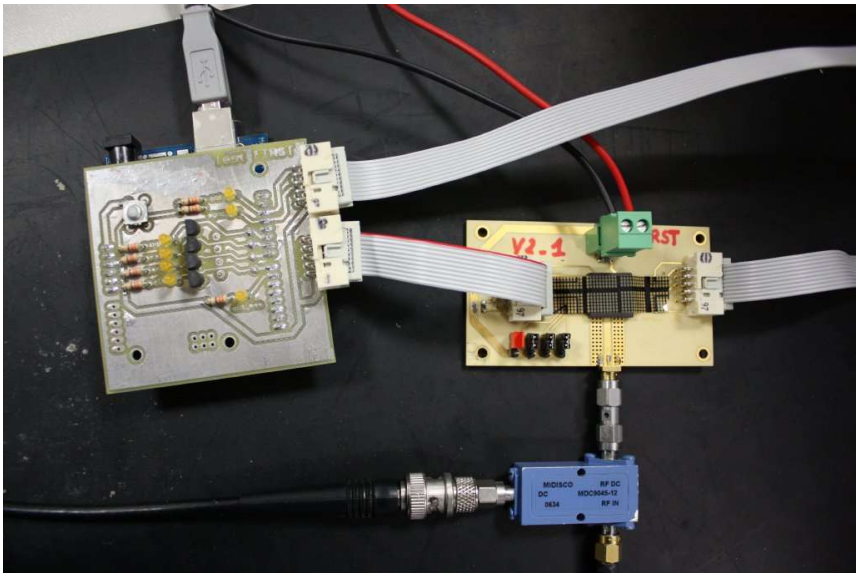
FIRST Digital up-sampling filter for 60 GHz communication systems

STMicroelectronics 65 nm CMOS
1.8 x 0.8 mm²
Chip-on-board assembly

J. Muller, B. Stefanelli, A. Frappé, L. Ye, A. Cathelin, A. Niknejad, A. Kaiser, "A 7-bit 18th order 9.6 GS/s FIR filter for high data rate 60-GHz wireless communications", Proceedings of 37th European Solid-State Circuits Conference, ESSCIRC 2011, Helsinki, Finland, September 12-16, 2011.

Abstract: This paper presents the design and measurements of a 4× oversampled 18th order digital low-pass FIR filter aimed at replacing all analog baseband filters in a 60 GHz high data-rate wireless communication transmitter. Pipeline CPL adders and TSPC flip-flops are used to enable a very high output sample rate. The filter area is 0.1mm2 in a standard 65nm CMOS process. The interpolator has been designed to work at 10 GS/s. Measurements can be performed up-to 9.6 GHz on a 1.4V supply voltage and the filter consumes 400 mW.

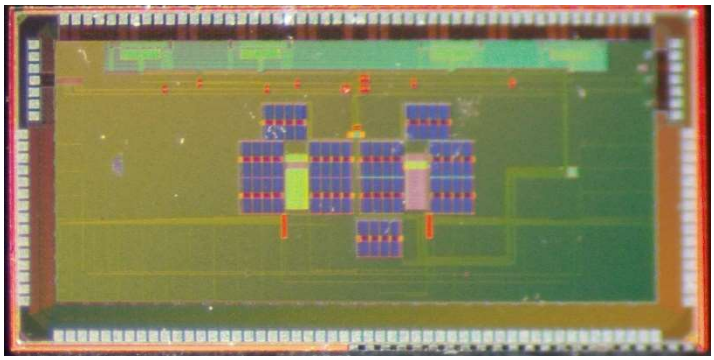


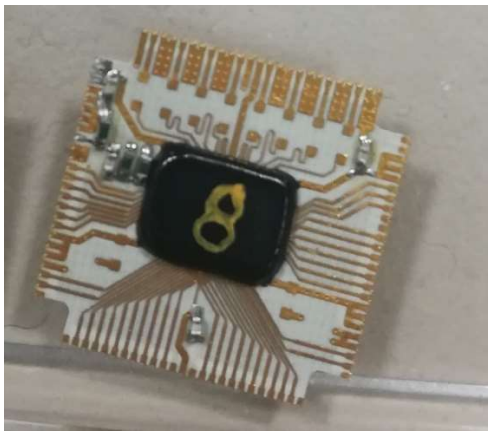


GARFIELD Digital delta-sigma modulator for digital RF signal generation in base stations

TSMC 40 nm CMOS
4.2 x 2 mm²
Chip-on-board assembly on a dedicated module

Internal report in the frame of a collaboration contract with Alcatel-Lucent:
A. Frappé, B. Stefanelli, « Report on measurement results », Programme de collaboration ISEN / Alcatel-Lucent, Livrable M5, 14 Mars 2013.



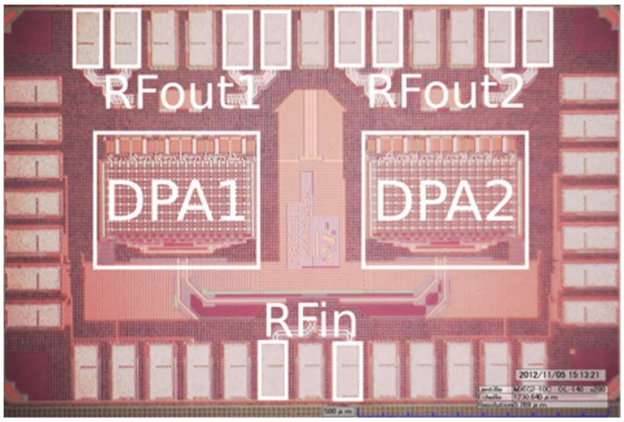


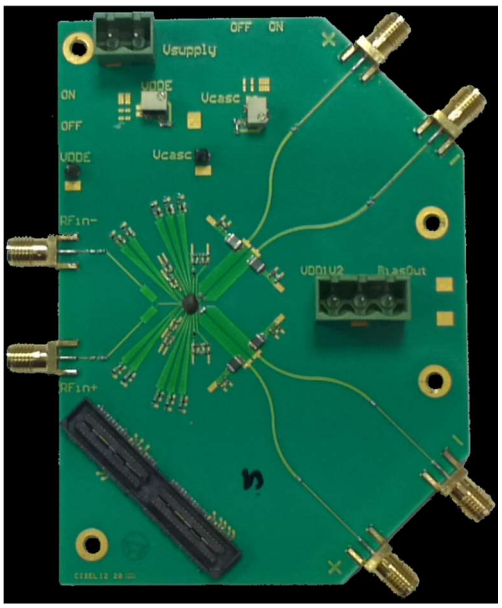
PACO II Digital power amplifier with multi-rate paths

STMicroelectronics 65 nm CMOS
1.2 x 0.8 mm²
Chip-on-board assembly

A. Werquin, A. Frappe, and A. Kaiser, “A multi-path multi-rate CMOS polar DPA for wideband multi-standard RF transmitters,” in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2013, pp. 327–330.

Abstract: A two-path digital power amplifier (DPA) in 1.2V 65nm CMOS is presented. This highly reconfigurable and frequency agile block is designed to be used as an envelope modulator in a wideband multi-standard polar transmitter. Each path is composed of a 12-bit DPA ensuring the modulation of the envelope of the RF signal. The DPAs are controlled by envelope code words (ECW) at different sample rates. This diversity strongly attenuates the images produced by the direct digital to RF conversion, avoiding passive filtering. The baseband sample rate conversion can easily be reconfigured. The proposed front-end can manage spurious emissions depending on the standard, the carrier frequency and the required power. The DPAs also integrate active input impedance compensation cells in order to limit the input impedance modulation when switching the DPA cells. The two-path DPA covers a 0.9-1.9 GHz bandwidth with 16.7dBm output 1dB compression point and 12.4% PAE. 64-QAM presents -28dB EVM while active area occupies 1x0.25mm2.



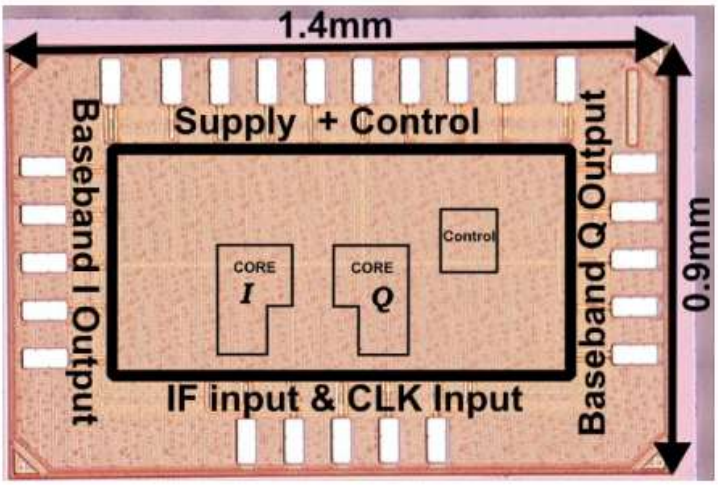


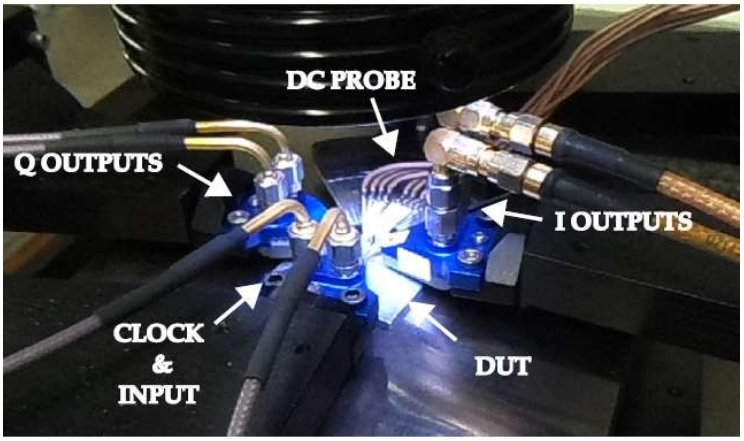
SYKING 60 GHz subsampling receiver

STMicroelectronics 28 nm CMOS
1.4 x 0.9 mm²
4-side probing

B. Grave, A. Frappe, and A. Kaiser, "Subsampling techniques applied to 60 GHz wireless receivers in 28 nm CMOS," in *2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS)*, 2014, pp. 365–368.

Abstract: This paper presents the architecture, the implementation details and the measurement results of an IF to DC subsampler for 60 GHz applications. The proposed subsampler performs down-conversion, IQ demodulation and out-of-band filtering within a unique operation. An 802.11ad (WiGig) channel at a fixed 21.12 GHz IF frequency is subsampled using a 7.04 GHz clock. The 1.76 GS/s analog to digital conversion is directly performed in baseband after FIR filtering and decimation. The charge domain subsampler and FIR filter provide additional immunity to perturbations at no extra hardware cost. Digitally controlled delay lines set the phase of the sampling clock to reach the best sampling instant. In conclusion, subsampling-based back-ends can be promising candidates for low power, low cost and digitally synchronized receiver architectures.



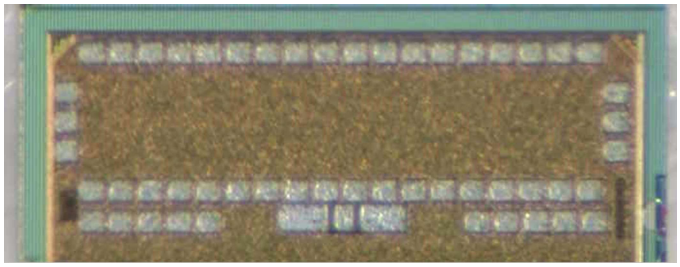


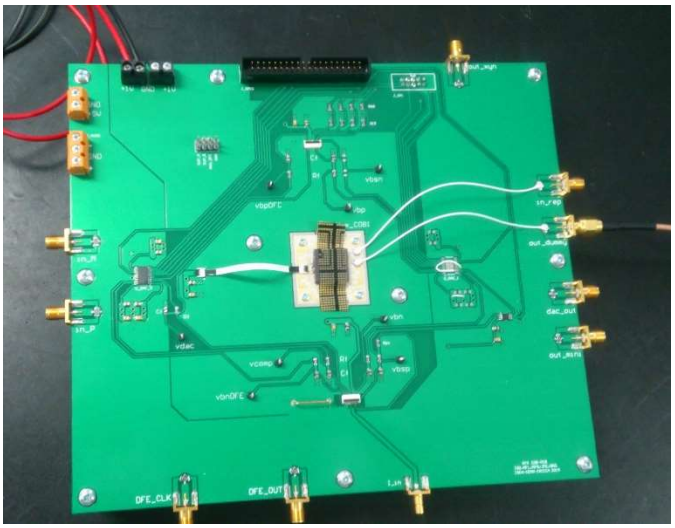
NYX Configurable digital delay line

STMicroelectronics 28 nm FDSOI
1 x 0.4 mm²
chip-on-board assembly on a substrate

I. Sourikopoulos, A. Frappe, A. Cathelin, L. Clavier, and A. Kaiser, “A digital delay line with coarse/fine tuning through gate/body biasing in 28nm FDSOI,” in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, 2016, pp. 145–148.

Abstract: This paper discusses the design and characterization of a programmable digital delay line. The core of the proposed architecture is a thyristor-type delay element featuring the capability for coarse/fine tuning without using any additional hardware. This is made possible by taking advantage of body biasing features available in 28nm FDSOI CMOS. Body biasing offers unique performance characteristics, notably a very low sensitivity to the biasing voltage. The prototype delay line was designed featuring thermometer-code multi-stage activation and gate/body biasing control. A delay range from 560ps to 16.13ns is exhibited for the delay line with a 2GS/s input stream. The unit delay cell exhibits fs/mV sensitivity combined with an order of magnitude larger delay dynamic range and an energy efficiency of only 12.5 fJ/event.



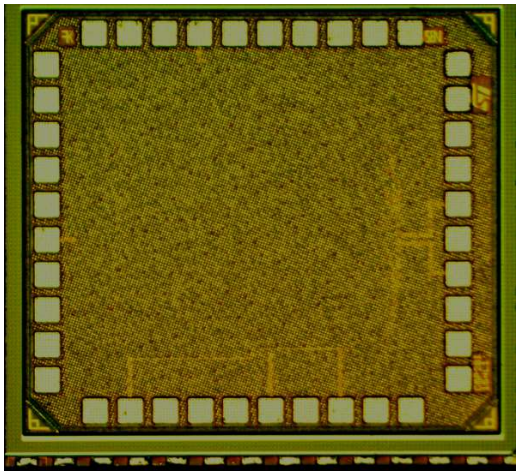


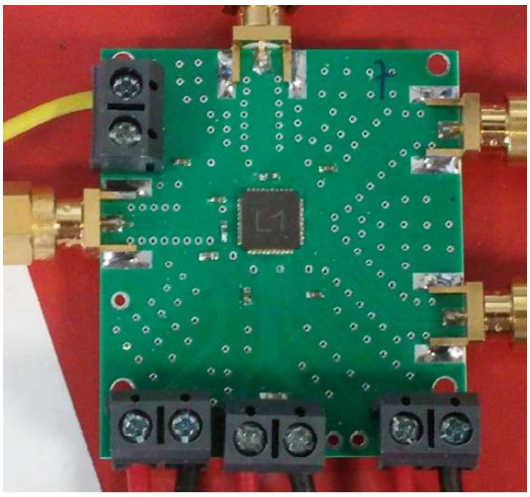
FIKRDAC Digital-to-analog converter with integrated finite impulse response filter (FIR-DAC)

STMicroelectronics 28 nm FDSOI
1 x 1 mm²
QFN40

F. T. Gebreyohannes, A. Frappe, P. Cathelin, A. Cathelin, and A. Kaiser, "All-Digital Transmitter Architecture Based on Two-Path Parallel 1-bit High Pass Filtering DACs," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. PP, pp. 1–14, 2018.

Abstract: This paper presents a novel transmitter architecture which is tailored for low power, all-digital, and high-speed implementation. It is based on two-path parallel digital-to-analog converters (DAC) which are driven by 180° phase-shifted clocks. The architecture operates in high pass mode and extends the output carrier frequency up to half the DAC clock rate. To decrease the number of analog unit current cells in the converter, a lowpass ΔΣ-modulator is used. Since the modulator also converts the input resolution to 1-bit, an inherently-linear digital-to-analog conversion is realized by embedding filtering in the DAC. Furthermore, the finite impulse response DAC transfer function is designed to cancel the ΔΣ-modulator quantization noise. Simulation results at system level demonstrate the robustness of the architecture against random coefficient mismatches, and its suitability for broadband transmissions. The error vector magnitude of the quadrature output is simulated for up to 15% random coefficient mismatch and it maintains a value below −22 dB even when the input signal bandwidths vary from 20 MHz (64-subcarrier OFDM) to 160 MHz (512-subcarrier OFDM). Experimental results are presented to discuss the validity of the proposed all-digital transmitter architecture and to highlight the challenges of implementing it in advanced CMOS nodes.



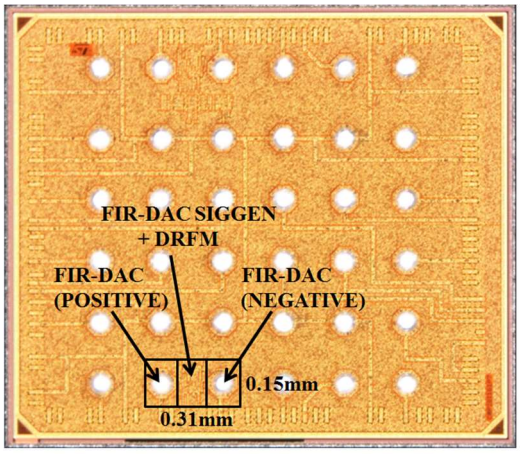


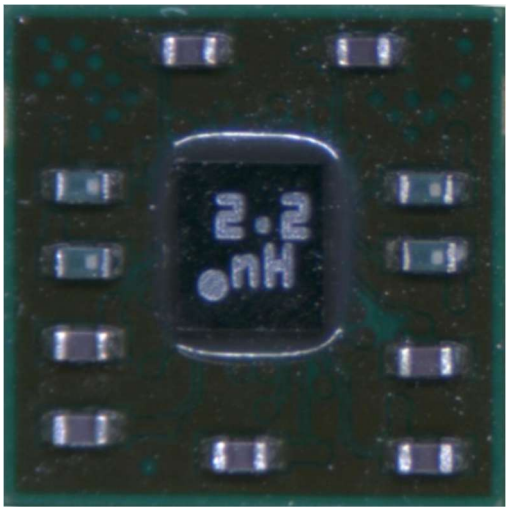
2PAD_WLANPA Digital RF Transmitter with Single-bit ΔΣM-driven Switched-capacitor RF DAC and Embedded Band Filter

STMicroelectronics 28 nm FDSOI
1.4 x 1.6 mm²
flip-chip on a dedicated BGA package

R.C. Marin, A. Frappé, B. Stefanelli, P. Cathelin, A. Cathelin, A. Kaiser, "Digital RF Transmitter with Single-bit ΔΣM-driven Switched-capacitor RF DAC and Embedded Band Filter in 28nm FD-SOI ", submitted to IEEE Transactions on Microwave Theory and Techniques.

Abstract: This paper presents a single-bit RF transmitter based on single-bit switched-capacitor RF digital-to-analog converters (DAC) embedded in a FIR filter (FIR-DAC). The transmitter system comprises a single-bit quadrature Delta-Sigma Modulator (ΔΣM), a digital mixer, and a 109-tap RF FIR-DAC stage with a single external inductor, combining D-A conversion with discrete and continuous time filtering. The on-chip part of the FIR-DAC is built exclusively with CMOS inverters and Metal-Oxide-Metal (MOM) capacitors implemented in the interconnect layers to propose a compact fully-digital solution, suitable for advanced CMOS nodes. A method for canceling redundant switching in the FIR-DAC is proposed to reduce its complexity and power consumption. Combining discrete and continuous-time filtering, the out-of-band quantization noise of the 1-bit RF signal is strongly attenuated below the level required by emission masks. The prototype RF FIR-DAC is integrated in 28nm FD-SOI CMOS technology with 10 metal layers and occupies a total active area of only 0.047mm^2. The resulting power consumption and surface make the proposed circuit particularly appropriate for use in emerging Internet of Things (IoT) applications. The overall power consumption is 38mW at 4.6dBm peak output power, 900MHz carrier frequency and 1V supply. Taking advantage of FD-SOI body-bias Vt tuning, carrier and image rejections of ~60dBc are measured.





Annex B Scientific publications

B.1. Bibliographical summary

The following tables give an overview of the scientific publications associated with this work from a quantitative and qualitative point of view.

Table 1 Quantitative summary of publications (as of Oct 2018)

Journal papers	9
Invited conferences	12
International conferences	29
National conferences	5
Other communications (no proceedings)	6
Book chapters	3
Patents	2

Table 2 Bibliometric indicators (as of Oct 2018). Data extracted from Google Scholar (http://scholar.google.com/).

Citation count	320
h-index	8
i10-index	7

Table 3 Qualitative description of the main publications as of Oct 2018. For the journal papers, the quality is derived from CiteScore and the Impact Factor published on the journal website. CiteScore measures average citations received per document published in the serial and can be found in the Scopus website (https://www.scopus.com/sources). For conference publications, only conferences with known impact in the domain are listed here and ranked following the ranking proposed by the GDR SOC2 (available at http://www.gdr-soc.cnrs.fr/conferences/)

Journal papers		**Number of documents**	**CiteScore 2017**	**Impact Factor**
IEEE Journal of Solid-State Circuits		3	5.03	4.08
IEEE Transactions on Circuits and Systems I: Regular papers		3	3.68	2.82
IEEE Transactions on Circuits and Systems II: Express briefs		1	2.88	2.45
Sensors and Actuators, A: Physical		1	2.79	2.31
International Journal of RF and Microwave Computer-Aided Engineering		1	1.14	1.31
Selected international conferences	**Acronym**	**Number of documents**	**Conference rank**	
IEEE International Symposium on Circuit and Systems	ISCAS	5	A	
IEEE Radio Frequency Integrated Circuits Symposium	RFIC	3		
IEEE European Solid-State Circuit Conference	ESSCIRC	3		
IEEE Symposium on VLSI Circuits	VLSI	1		
IEEE MTT-S International Microwave Symposium	IMS	1		
IEEE International New Circuits and Systems Conference	NEWCAS	6	B	
IEEE Int. Conference on Electronics, Circuits and Systems	ICECS	3		
IEEE International Wireless Symposium	IWS	2		
IEEE Biomedical Circuits and Systems Conference	BioCAS	1		

B.2. Publication list

B.2.1. Peer-reviewed international journals – Regular papers

[R1] A. Frappé, A. Flament, B. Stefanelli, A. Kaiser, A. Cathelin, "An All-Digital RF Signal Generator Using High-Speed ΔΣ Modulators", IEEE Journal of Solid-State Circuits, vol.44, no. 10, pp. 2722-2732, Oct 2009.
JIF = 3.151 [1]
Relative position of the journal (in the relevant WoS category): 4.5% [2]

[R2] A. Flament, A. Frappé, B. Stefanelli, A. Kaiser, A. Cathelin, S. Giraud, M. Chatras, S. Bila, D. Cros, J.B. David, L. Leyssenne, E. Kerhervé, "A complete UMTS transmitter using BAW filters and duplexer: A 90-nm CMOS digital RF signal generator and a 0.25-µm BiCMOS power amplifier", International Journal of RF and Microwave Computer-Aided Engineering, Volume 21, Issue 5, pages 466–476, Sep 2011.
JIF = 0.591
Relative position of the journal (in the relevant WoS category): 72.5%

[R3] C. Thakkar, L. Kong, K. Jung, A. Frappé, E. Alon, "A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS", IEEE Journal of Solid-State Circuits, vol.47, no. 4, pp. 952-968, Apr 2012.
JIF = 3.063
Relative position of the journal (in the relevant WoS category): 8.7%

[R4] J. Muller, B. Stefanelli, A. Frappé, L. Ye, A. Cathelin, A. Niknejad, A. Kaiser, "A 7 -bit 18th order 9.6 GS/s FIR up-sampling filter for High Data Rate 60-GHz Wireless Transmitters", IEEE Journal of Solid-State Circuits, vol.47, no. 7, pp. 1743-1756, Jul 2012.
JIF = 3.063
Relative position of the journal (in the relevant WoS category): 8.7%

[R5] B. Grave, A. Frappé, A. Kaiser, "A reconfigurable IF to DC sub-sampling receiver architecture with embedded channel filtering for 60 GHz applications", IEEE Trans. Circuits Syst. I-Regul. Pap., 60, 5, pp. 1220-1231, May 2013.
JIF = 2.303
Relative position of the journal (in the relevant WoS category): 18.6%

[R6] F. Gebreyohannes, A. Frappé, A. Kaiser, "A configurable transmitter architecture for IEEE 802.11ac and 802.11ad standards", IEEE Trans. Circuits Syst. II-Express Briefs, 63, 1, pp. 9-13, January 2016
JIF = 1.660
Relative position of the journal (in the relevant WoS category): 50.8%

[R7] R. C. Marin, A. Frappé, A. Kaiser, "Digital Complex Delta–Sigma Modulators with Highly Configurable Notches for Multi-Standard Coexistence in Wireless Transmitters," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, pp. 343-352, Jan. 2018.

[1] Source Journal Impact Factor (JIF): Journal Citation Reports ©Clarivate Analytics
[2] Source: https://publis.iemn.fr ©IEMN. This percentage relates the position of the journal in the Web Of Science (WoS) category in which it is ranked higher (most relevant category). This is to consider the specificity of each research domain. The lower the value, the better the ranking. More info can be found here: https://publis.iemn.fr/position-relative-du-journal.pdf

[R8] Y. Mita, N. Sakamoto, N. Usami, A. Frappé, A. Higo, B. Stefanelli, H. Shiomi, J. Bourgeois, A. Kaiser, "Microscale ultrahigh-frequency resonant wireless powering for capacitive and resistive MEMS actuators," Sensors and Actuators A: Physical, Volume 275, 1 June 2018, Pages 75-87.

[R9] F. T. Gebreyohannes, A. Frappe, P. Cathelin, A. Cathelin, and A. Kaiser, "All-Digital Transmitter Architecture Based on Two-Path Parallel 1-bit High Pass Filtering DACs," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 65, no. 11, pp. 3956–3969, 2018.

[R10] R.-C. Marin, A. Frappé, B. Stefanelli, P. Cathelin, A. Cathelin, A. Kaiser, "Digital RF Transmitter with Single-bit ΔΣM-driven Switched-capacitor RF DAC and Embedded Band Filter in 28nm FD-SOI," submitted to the IEEE Transactions on Microwave Theory and Techniques.

B.2.2. Invited conferences

[I1] A. Frappé, A. Flament, B. Stefanelli, A. Kaiser, *"Multimode Transmitters with ΔΣ-based All-Digital RF Signal Generation",* 18th Workshop on Advances in Analog Circuit Design, AACD 2009, Lund, Sweden, March 31-April 2, 2009.

[I2] A. Frappé, A. Kaiser, *"All-Digital RF Signal Generation",* CMOS Emerging Technologies Workshop, Whistler, BC, Canada, May 19-21, 2010.

[I3] A. Frappé, A. Kaiser, "*Digital RF signal generation for ultimate transmitters*", 61st IEEE MTT-S International Microwave Symposium, IMS 2013, Workshop WSD: Pushing the Ultimate Performance Limits of RF CMOS, Seattle, WA, USA, June 2-7, 2013, paper WSD-8.

[I4] A. Werquin, A. Frappé, "*Multi-path architectures for digital RF transmitters*", CMOS Emerging Technologies Research Conference, CMOSETR 2015, Vancouver, BC, Canada, May 20-22, 2015.

[I5] B. Grave, A. Frappé, "*Subsampling techniques applied to Gbps wireless communications*", CMOS Emerging Technologies Research Conference, CMOSETR 2015, Vancouver, BC, Canada, May 20-22, 2015.

[I6] A. Frappé, "*Digital radio frequency signal generation towards ultimate transmitters*", Proceedings of 2014 International Symposium on Fundamentals of Electrical Engineering, ISFEE 2014, Bucharest, Romania, November 28-29, 2014, session CIRC2 - Circuit Design, paper 219, 5 pages.

[I7] A. Frappé, F.T. Gebreyohannes, A. Kaiser*, "An 802.11ac/ad configurable transmitter architecture",* 4th IEEE MTT-S International Wireless Symposium, IWS 2016, Shanghai, China, March 14-16, 2016.

[I8] F. Gebreyohannes, A. Frappé, A. Kaiser, *"A configurable transmitter architecture for IEEE 802.11ac and 802.11ad standards",* IEEE International Symposium on Circuits and Systems, ISCAS 2016, Montreal, Canada, May 22-25, 2016.

[I9] C. Marin, A. Frappé, A. Kaiser, "*Delta-sigma based digital transmitters with low-complexity embedded-FIR digital to RF mixing*", Proceedings of 23rd IEEE International Conference on Electronics, Circuits and Systems, ICECS 2016, Monte Carlo, Monaco, December 11-14, 2016, Session A3L-C - Advanced Concepts for Future RF and mmW Transceivers, 237-240.

[I10] A. Frappé, *"Multi-standard RF and mmW transmitters based on semi-digital FIR-DAC",* 2017 IEEE Radio Frequency Integrated Circuits Symposium, RFIC 2017, Workshop WSD -

Advanced Concepts and Architectures for Future RF and mmW Transceivers in Nanoscale CMOS, Honolulu, HI, USA, June 4-6, 2017.

[I11] A. Kaiser, A. Frappé, "*Digital RF transmitter architectures exploiting FIRDACs in various configurations*", Proceedings of IEEE 12th International Conference on ASIC, ASICON 2017, Guiyang, China, October 25-28, 2017, Session SB8 - RF Design Techniques, paper SB8-1, 1094-1097.

[I12] R.C. Marin, A. Frappé, A. Kaiser, "*Digital Complex Delta-Sigma Modulators with Highly Configurable Notches for Multi-Standard Coexistence in Wireless Transmitters*", IEEE International Symposium on Circuits and Systems, ISCAS 2018, Florence, Italy, May 27-30, 2018.

B.2.3. International conferences

[CI1] A. Frappé, A. Flament, B. Stefanelli, A. Cathelin, A. Kaiser, "*All-digital RF signal generation for software-defined radios*", Proceedings of the 3rd IEEE International Conference on Circuits and Systems for Communications, ICCSC'06, Bucharest, Romania, July 6-7, 2006.

[CI2] A. Flament, A. Frappé, B. Stefanelli, A. Kaiser, A. Cathelin, « Convertisseur numérique analogique 1 bit à 7,8Gech/s pour émetteurs RF numériques en technologie CMOS 90nm », Actes du 7ème Colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications, TAISA'2006, Strasbourg, France, 19-20 Octobre, 2006.

[CI3] A. Frappé, A. Flament, B. Stefanelli, A. Kaiser, A. Cathelin, R. Daouphars, *"Design techniques for very high-speed digital delta-sigma modulators aimed at all-digital RF transmitters",* Proceedings of the 13th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2006, Nice, France, December 10-13, 2006.

[CI4] C. Nsiala Nzéza, J. Gorisse, A. Frappé, A. Flament, A. Kaiser, A. Cathelin, "*Reconfigurable digital delta-sigma modulator synthesis for digital wireless transmitters*", Proceedings of the 18th European Conference on Circuit Theory and Design, ECCTD'07, Sevilla, Spain, August 26-30, 2007.

[CI5] C. Nsiala Nzéza, A. Frappé, J. Gorisse, A. Flament, B. Stefanelli, A. Cathelin, A. Kaiser, "*Direct digital RF signal generation for Software-Defined Radio transmitters using reconfigurable Delta-Sigma modulators*", Proceedings of the 11th International Symposium on Microwave and Optical Technology, ISMOT-2007, Monte Porzio Catone, Italy, December 17-21, 2007.

[CI6] A. Frappé, B. Stefanelli, A. Flament, A. Kaiser, A. Cathelin, "*An all-digital delta-sigma RF signal generator for mobile communication transmitters in 90nm CMOS*", Proceedings of the 2008 IEEE Radio Frequency Integrated Circuits Symposium, IEEE RFIC 2008, Atlanta, GA, USA, June 15-17, 2008.

[CI7] C. Nsiala Nzéza, A. Flament, A. Frappé, A. Kaiser, A. Cathelin, J. Muller, "*Reconfigurable complex digital delta-sigma modulator synthesis for digital wireless transmitters*", Proceedings of the 4th European Conference on Circuits and Systems for Communications, ECCSC 2008, Bucharest, Romania, July 10-11, 2008.

[CI8] A. Frappé, A. Flament, B. Stefanelli, A. Cathelin, A. Kaiser, *"All-digital RF signal generation for software defined radio",* Proceedings of the 4th European Conference on Circuits and Systems for Communications, ECCSC 2008, Bucharest, Romania, July 10-11, 2008.

[CI9] A. Flament, A. Frappé, A. Kaiser, B. Stefanelli, A. Cathelin, H. Ezzeddine, "*A 1.2 GHz Semi-Digital Reconfigurable FIR Bandpass Filter with Passive Power Combiner*", Proceedings of the

34th European Solid-State Circuits Conference, ESSCIRC 2008, Edinburgh, Scotland, UK, September 15-19, 2008.

[CI10] A. Flament, S. Giraud, S. Bila, M. Chatras, A. Frappé, B. Stefanelli, A. Kaiser, A. Cathelin, "*Complete BAW filtered CMOS 90nm digital RF signal generator*", Proceedings of the 2009 Joint IEEE North-East Workshop on Circuits and Systems and TAISA Conference, NEWCAS-TAISA'09, Toulouse, France, June 28-July 1, 2009.

[CI11] A. Werquin, A. Frappé, A. Kaiser, "*Spurious Emissions Reduction using Multirate RF Transmitter",* Proceedings of the 2011 IEEE International Symposium on Circuits and Systems, ISCAS 2011, Rio de Janeiro, Brazil, 15-18 May 2011.

[CI12] A. Werquin, A. Frappé, J. Muller, A. Kaiser*, "Spectral regrowth analysis in wideband polar architectures applied to software defined radio",* Proceedings of 9th IEEE International New Circuits and Systems Conference, NEWCAS 2011, Bordeaux, France, June 26-29, 2011.

[CI13] C. Thakkar, L. Kong, K, Jung, A. Frappé, E. Alon, *"A 10Gb/s 45mW adaptive 60GHz baseband in 65nm CMOS",* 2011 Symposium on VLSI Circuits (VLSIC), pp. 24-25, Kyoto, Japan, June 2011 **(Best Student Paper).**

[CI14] J. Muller, B. Stefanelli, A. Frappé, L. Ye, A. Cathelin, A. Niknejad, A. Kaiser, *"A 7-bit 18th order 9.6 GS/s FIR filter for high data rate 60-GHz wireless communications",* Proceedings of 37th European Solid-State Circuits Conference, ESSCIRC 2011, Helsinki, Finland, September 12-16, 2011.

[CI15] B. Grave, A. Frappé, A. Kaiser, *"A Reconfigurable 60GHz Subsampling Receiver Architecture with Embedded Channel Filtering",* Proceedings of 2012 IEEE International Symposium on Circuits and Systems, ISCAS 2012, Seoul, Korea, May 20-23, 2012.

[CI16] A. Werquin, A. Frappé, A. Kaiser, *"A multi-path multi-rate CMOS polar DPA for wideband multi-standard RF transmitters",* Proceedings of 2013 IEEE Radio Frequency Integrated Circuits Symposium, IEEE RFIC 2013, Seattle, WA, USA, June 2-4, 2013, paper RTU2A-4, 327-330.

[CI17] I. Sourikopoulos, A. Frappé, A. Kaiser, L. Clavier, *"A decision feedback equalizer with channel-dependent power consumption for 60-GHz receiver",* Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS 2014, Melbourne, Australia, June 1-5, 2014.

[CI18] B. Grave, A. Frappé, A. Kaiser, *"Subsampling techniques applied to 60 GHz wireless receivers in 28 nm CMOS",* Proceedings of 12th IEEE International New Circuits and Systems Conference, NEWCAS 2014, Trois-Rivières, Canada, June 22-25, 2014.

[CI19] S. Mebaley-Ekome, L. Clavier, A. Frappé, E. Simon, I. Sourikopoulos, *"Estimation of 60-GHz channels based on energy detection",* Proceedings of 2014 IEEE International Conference on Ultra-Wideband, ICUWB 2014, Paris, France, September 1-3, 2014.

[CI20] R.C. Marin, A. Frappé, *"An adaptive synchronization scheme for 60 GHz subsampling receivers",* Proceedings of 2014 International Symposium on Fundamentals of Electrical Engineering, ISFEE 2014, Bucharest, Romania, November 28-29, 2014.

[CI21] R.C. Marin, A. Frappé, A. Kaiser, A. Cathelin, *"Considerations for high-speed configurable-bandwidth time-interleaved digital delta-sigma modulators and synthesis in 28 nm UTBB FDSOI",* Proceedings of 13th IEEE International Conference on New Circuits and Systems, NEWCAS 2015, Grenoble, France, June 7-10, 2015.

[CI22] F.T. Gebreyohannes, A Frappé, A Kaiser, *"Semi-digital FIR DAC for low power single carrier IEEE 802.11ad 60GHz transmitter",* Proceedings of 13th IEEE International Conference on New Circuits and Systems, NEWCAS 2015, Grenoble, France, June 7-10, 2015.

[CI23] N. Sakamoto, A. Frappé, B. Stefanelli, A. Kaiser, Y. Mita, *"Wireless drive of a MEMS ciliary motion actuator via coupled magnetic resonances using micro inductors",* Proceedings of 18th International Conference on Solid-State Sensors, Actuators and Microsystems, TRANSDUCERS 2015, Anchorage, AK, USA, June 21-25, 2015.

[CI24] F.T. Gebreyohannes, A. Frappé, A. Kaiser, "Multi-standard semi-digital FIR DAC: a design procedure", Proceedings of 4th IEEE MTT-S International Wireless Symposium, IWS 2016, Shanghai, China, March 14-16, 2016.

[CI25] I. Sourikopoulos, A. Frappé, A. Cathelin, L. Clavier, A. Kaiser, *"A digital delay line with coarse/fine tuning through gate/body biasing in 28nm FDSOI",* Proceedings 42nd European Solid-State Circuits Conference, ESSCIRC 2016, Lausanne, Switzerland, September 12-15, 2016.

[CI26] M. Causo, S. Benatti, A. Frappé, A. Cathelin, E. Farella, A. Kaiser, L. Benini, J.M. Rabaey, *"Sampling modulation: an energy efficient novel feature extraction for biosignal processing",* Proceedings of 12th IEEE Biomedical Circuits and Systems Conference, BioCAS 2016, Shanghai, China, October 17-19, 2016.

[CI27] D. Ghosh, A. Frappé, C. Loyez, A. Cathelin, "A bidirectional short-range low-power and high data rate W-band transceiver for network-on-chip", Proceedings of 16th IEEE International Conference on New Circuits and Systems, NEWCAS 2018, Montreal, Canada, June 24-27, 2018.

[CI28] F.T. Gebreyohannes, A. Frappé, P. Cathelin, A. Cathelin, A. Kaiser, "All-digital transmitter architecture based on two-path parallel 1-bit high pass filtering DACs," IEEE International Symposium on Integrated Circuits and Systems, ISICAS 2018, Taormina, Italy, Sep 2-3 2018.

[CI29] S. Lecoq, J. Le Bellego, A. Gonzalez, B. Larras, and A. Frappé, "Low-complexity feature extraction unit for 'Wake-on-Feature' speech processing,", accepted at IEEE International Conference on Electronics Circuits and Systems, Bordeaux, France, Dec 2018.

B.2.4. National conferences

[CN1] C. Nsiala-Nzéza, A. Frappé, J. Gorisse, A. Flament, B. Stefanelli, A. Kaiser, "Reconfigurable RF signal generation for software radio transmitters", Actes du 8ème Colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications, TAISA 2007, Lyon, France, 18-19 Octobre, 2007.

[CN2] B. Grave, A Frappé, A. Kaiser, "Low power configurable subsampling back-end with embedded filtering for 60 GHz receivers", Actes du 5ème Colloque du GDR SOC-SIP, Lyon, France, 15-17 Juin, 2011.

[CN3] Werquin, A. Frappé, A. Flament, B. Stefanelli, A. Kaiser, "Wideband image rejection in digital polar architectures", Actes du 5ème Colloque du GDR SOC-SIP, Lyon, France, 15-17 Juin, 2011.

[CN4] F.T. Gebreyohannes, A. Frappé, A. Kaiser, "Semi-digital FIR DAC for low power single carrier IEEE 802.11ad 60GHz transmitter", Actes des 18èmes Journées Nationales du Réseau Doctoral en Micro-nanoélectronique, JNRDM 2015, Bordeaux, France, 5-7 Mai, 2015.

[CN5] D. Ghosh, A. Frappé, C. Loyez, A. Cathelin, "An ultra low power mm-wave wireless transceiver design for high speed inter-chip communication above 100 GHz", Actes de la Journée Thématique du GT4 du GDR Ondes « Circuits et Systèmes Intégrés RF et Millimétriques », Grenoble, France, 10 Mars, 2017.

B.2.5. Other communications

[C1] A. Frappé, "*Digital RF Signal Generation for Ultimate Transmitters",* BIT's 1st Annual World Congress of Emerging InfoTech, WCEIT 2012, Dalian, China, August 28-30, 2012.

[C2] A. Frappé, *"Digital RF signal generation towards ultimate transmitters",* Victoria University IEEE Student Branch Technical Session, Melbourne, Australia, June 6, 2014.

[C3] A. Frappé, A. Werquin, *"Multi-rate multi-path wideband digital power amplifier for opportunistic radios",* Journée thématique AMS & RF du GDR SoC-SiP, 'L'éco-radio-intelligente', Bordeaux, France, 4 octobre, 2014.

[C4] A. Frappé, F.T. Gebreyohannes, A. Kaiser, *"An 802.11ac/ad configurable transmitter architecture",* Victoria University IEEE Student Branch Technical Session, Melbourne, Australia, October 26, 2016.

[C5] Frappé, B. Larras, A. Gonzalez, A. Kaiser, P. Cathelin, "Continuous-time digital signal processing for audio feature extraction integrated in 28nm FD-SOI CMOS", Journée Thématique du GDR SOC2 « Near Sensor Computing », Paris, France, 8 novembre, 2017

[C6] Gonzalez, A. Frappé, B. Larras, A. Kaiser, P. Cathelin, "Continuous-time digital signal processing for audio feature extraction integrated in 28nm FD-SOI CMOS", Journée Thématique conjointe IEEE-CAS et GDR/SOC2 « Analog to Information Sensing, Analog-to-Classification Sensing: New Principles to Extract Relevant Information », Paris, France, 12 décembre, 2017

B.2.6. Book chapters

[O1] A. Frappé, A. Flament, B. Stefanelli, A. Kaiser, A. Cathelin, *"Multimode Transmitters with SD-based All-Digital RF Signal Generation",* in *"Analog Circuit Design: Smart Data Converters, Filters on Chip, Multimode Transmitters",* edited by Arthur van Roermund; Herman Casier; Michiel Steyaert, Springer, 342 p., ISBN: 978-90-481-3082-5, Nov 2009.

[O2] A. Frappé, A. Flament, B. Stefanelli, A. Kaiser, A. Cathelin, *"All-digital RF signal generation"* in *"CMOS Nanoelectronics: Analog and RF VLSI Circuits",* edited by K. Iniewski, published by McGraw-Hill, ISBN 0071755659, August 2011.

[O3] M. Chatras, S. Bila, S. Giraud, L. Catherinot, J. Fan, D. Cros, M. Aubourg, A. Flament, A. Frappé, B. Stefanelli, A. Kaiser, A. Cathelin, J.B. David, A. Reinhardt, L. Leyssenne, E. Kerhervé, *"Modeling and design of BAW resonators and filters for integration in a UMTS transmitter"* in *"Modeling and measurement methods for acoustic waves and for acoustic microdevices",* Beghi M.G. (Ed), ISBN 978-953-51-1189-4, InTech (2013) chapter 14, 323-354.

B.2.7. Seminars

[S1] A. Kaiser, A. Frappé, *"Digital RF and mmW frontends",* 2nd Workshop University of Michigan - IEMN, Villeneuve d'Ascq, France, May 16-17, 2011.

[S2] C. Thakkar, L. Kong, K. Jung, A. Frappé, E. Alon, *"A 10Gb/s 45mW adaptive 60GHz baseband in 65nm CMOS",* BWRC Summer Retreat 2011, Berkeley, CA, USA, June 8, 2011.

[S3] A. Frappé, *« Les ADICODE® comme outils d'exploration de nouveaux usages pour les objets connectés »,* 10 ans de l'IRCICA, Villeneuve d'Ascq, France, 27 septembre, 2016 Frappé 10 ans IRCICA 2016

[S4] A. Frappé, B. Larras, *« Low-Energy On-chip Pre-processing for Activity Recognition (LEOPAR) »,* IEMN Flagship Workshop on Neuromorphic Technologies, Villeneuve d'Ascq, France, 06 November 2018.

B.2.8. Thesis

[T1] A. Frappé, *« Génération numérique de signaux RF pour les terminaux de communication mobile par modulation ΔΣ »,* Thèse de doctorat en Microondes et Microtechnologies, Université de Lille 1, 7 décembre 2007

B.2.9. Patents

[P1] *Procédé de traitement d'un signal numérique au sein d'un modulateur delta-sigma numérique, et modulateur delta-sigma correspondant*
Inventeurs : CATHELIN Andreia, FRAPPE Antoine, KAISER Andreas
Demandeur(s) : STMicroelectronics SA, CNRS
N° de brevet : FR2911455 (A1) 2008-07-18

Également publié en tant que :

- WO2008102091 (A2) 2008-08-28
- WO2008102091 (A3) 2008-10-09
- FR2911455 (B1) 2009-04-17
- US2010142641 (A1) 2010-06-10
- US8594226 (B2) 2013-11-26

[P2] *Procédé et dispositif de traitement d'un signal d'entrée pour augmenter le rapport signal sur bruit et convertisseur correspondant*
Inventeurs : WERQUIN Arnaud, KAISER Andreas, FRAPPE Antoine
Demandeur(s) : CNRS
N° de brevet : FR2973611(A1) 2012-10-05

Également publié en tant que :

- WO2012136729 (A1) 2012-10-11

B.2.10. Deliverables related to collaboration contracts

[RC1] A.C. Hladky-Hennion, A. Frappé, A. Flament, « Modélisation et réalisation de prototypes de matrice 3D » - Rapport final pour la société Sonaxis, 2003

[RC2] D. Galayko, A. Flament, A. Frappé, A. Kaiser, « Architectures d'émission pour la radio logicielle », Nano 2008 program, Activity report, December 2004.

[RC3] A. Frappé, A. Flament, B. Stefanelli, J.M. Capron, A. Kaiser, « Transmetteur numérique WCDMA », Nano 2008 program, Activity report, July 2005.

[RC4] A. Frappé, A. Flament, B. Stefanelli, J.M. Capron, A. Kaiser, « Transmetteur numérique WCDMA », Nano 2008 program, Activity report, December 2005.

[RC5] A. Frappé, A. Flament, C. Nsiala Nzéza, B. Stefanelli, J.M. Capron, A. Kaiser, « Transmetteur numérique WCDMA », Nano 2008 program, Activity report, July 2006.

[RC6] A. Frappé, A. Flament, J. Gorisse, C. Nsiala Nzéza, B. Stefanelli, J.M. Capron, A. Kaiser, « Transmetteur numérique WCDMA », Nano 2008 program, Activity report, December 2006.

[RC7] A. Frappé, A. Flament, J. Gorisse, C. Nsiala Nzéza, B. Stefanelli, J.M. Capron, A. Kaiser, « Conception de Nouvelles Architectures ou Circuits : Design avancé appliqué aux nouvelles architectures de communications mobiles», Nano 2008 program, Activity report, July 2007.

[RC8] A. Frappé, A. Flament, J. Gorisse, C. Nsiala Nzéza, J. Muller, B. Stefanelli, J.M. Capron, A. Kaiser, « Conception de Nouvelles Architectures ou Circuits : Design avancé appliqué aux nouvelles architectures de communications mobiles», Nano 2008 program, Activity report, December 2007

[RC9] A. Frappé, « ΣΔ Block diagram », Programme de collaboration ISEN / e2v, Livrable 4.2.1, 3 Mars 2010.

[RC10] A. Frappé, « Modélisation des blocs du modulateur delta-sigma », Programme de collaboration ISEN / e2v, Livrable 4.2.2, 26 Avril 2010.

[RC11] A. Frappé, « Modélisation des blocs avec un niveau de complexité croissant selon les parasites inclus dans le modèle », Programme de collaboration ISEN / e2v, Livrable 4.2.3, 15 Juin 2010.

[RC12] A. Frappé, B. Stefanelli, A. Flament, « Décision sur un choix de procédé technologique à utiliser », Programme de collaboration ISEN / Alcatel-Lucent, Livrable M1, 15 Mars 2011.

[RC13] A. Kaiser, A. Frappé, « Recherche d'architecture / Identification d'architectures potentielles – Etablissement des performances fonctionnelles », Programme de collaboration ISEN / Thalès Alenia Space, Livrable 1.1, 25 Mars 2011.

[RC14] A. Frappé, B. Stefanelli, A. Flament, « Rapport sur la faisabilité et l'architecture préliminaire du circuit », Programme de collaboration ISEN / Alcatel-Lucent, Livrable M2, 7 Avril 2011.

[RC15] A. Frappé, A. Flament, B. Grave, B. Stefanelli, « Rapport final d'architecture et de design », Programme de collaboration ISEN / Alcatel-Lucent, Livrable M3, 21 Octobre 2011.

[RC16] J. Gorisse, C. Dehos, C. Loyez, A. Frappé, "Report on system, architecture, and specifications for very low power mmW fast downloading applications", ENIAC MIRANDELA project, Deliverable D3.1.5, 18 Novembre 2011.

[RC17] A. Kaiser, A. Frappé, « Recherche d'architecture / Dimensionnement fonctionnel – Evaluation qualitative de la complexité – Sélection d'une solution unique pour la tache 2 », Programme de collaboration ISEN / Thalès Alenia Space, Livrable 1.2, 29 Février 2012.

[RC18] A. Kaiser, A Frappé, « Evaluation de complexité », Programme de collaboration ISEN / Thalès Alenia Space, Livrable 2, 24 Avril 2012.

[RC19] A. Werquin, A. Frappé, « Multirate wideband digital PA design », ENIAC MIRANDELA project, Report T2.3.1, 27 Avril 2012.

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[RC21] A. Flament, A. Kaiser, A. Frappé, « Etude et proposition de solutions de corrections de la fuite LO et mismatch IQ », Seconde phase du programme de collaboration ISEN / Thalès Alenia Space, Livrable 1, 18 Janvier 2013.

[RC22] A. Frappé, « Etude des réjections d'oscillateur local (OL) et de fréquence image d'un convertisseur numérique/analogique à signal de sortie radiofréquence / Définition d'un environnement de simulation pour tâches ultérieures », Seconde phase du programme de collaboration ISEN / Thalès Alenia Space, Livrable 2, 28 Janvier 2013.

[RC23] A. Frappé, B. Stefanelli, « Report on measurement results », Programme de collaboration ISEN / Alcatel-Lucent, Livrable M5, 14 Mars 2013.

[RC24] A. Frappé, M. Kärkkäinen, M. Varonen, C. Jany, C. Dehos, A. Siligaris, C. Loyez, "Report on the design (or redesign) of RF building blocks for mm-waves system for the second tape-out (if needed)", ENIAC MIRANDELA project, Deliverable D2.3.5, 6 Novembre 2013.

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[RC26] A. Frappé, "Report on design & evaluation of sub-sampling mmW receiver prototype circuit", ENIAC MIRANDELA project, Deliverable D4.1.2, 4 Décembre 2013.

[RC27] C. Loyez, A. Frappé, "Report on feasibility of passive imaging systems based on a synthetic aperture antenna technique", ENIAC MIRANDELA project, Deliverable D4.1.1, 7 Février 2014.

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[RC29] A. Flament, A. Frappé, « Etude de faisabilité de prototypes de circuits intégrés », Programme de collaboration ISEN / Tronico - Instent, 12 Mars 2015.

[RC30] A. Frappé, B. Grave, R.C. Marin, A. Kaiser, « Techniques de sous échantillonnage en gamme millimétrique - Récepteur hétérodyne 60 GHz à sous-échantillonnage - Architectures de récepteur optimisant l'interopérabilité des ressources WiGig et WiFi », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.1/SP2.4/SP2.8, 25 février 2016.

[RC31] A. Frappé, I. Sourikopoulos, A. Kaiser, L. Clavier, A. Cathelin, « Première démonstration de l'égalisation de canal ciblant la réduction de consommation - Egaliseur de canal numérique en

temps continu », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.2/SP2.6, 25 février 2016.

[RC32] F.T. Gebreyohannes, A. Frappé, « Architecture de transmetteur 60GHz à conversion numérique-vers-millimétrique », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.3, 25 février 2016.

[RC33] M. Causo, A. Frappé, A. Kaiser, A. Cathelin, J.M. Rabaey, « Première démonstration DSP neuro-inspiré 28FDSOI », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.7, 25 février 2016.

[RC34] F.T. Gebreyohannes, A. Frappé, « Architectures de transmetteur optimisant l'interopérabilité des ressources WiGig et WiFi », Programme de recherche & développement coopératif NANO 2017, Livrable SP211/SP2.16, 16 Février 2017.

[RC35] A. Frappé, M. Causo, « Démonstrateur final capteur faible consommation avec DSP neuro-inspiré », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.14, 10 Mars 2017.

[RC36] A. Frappé, W. Bourennane, U. Ismailov, « Impact des cas d'usage sur l'architecture des nœuds mobiles communicants et architecture préliminaire », PIAVE AUTONOTEX project, Livrable 5.1.1, 16 Mars 2017.

[RC37] P. Diener, M. Berthomé, A. Frappé, « Faisabilité et démonstration d'intégration de puces silicium dans une feuille plastique », PIAVE AUTONOTEX project, Livrable 5.2.1, 16 Mars 2017.

[RC38] A. Frappé, C. Loyez, D. Ghosh, A. Cathelin, « Architecture E/R très faible consommation pour communication inter-puce », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.5, 17 Mars 2017.

[RC39] A. Frappé, W. Bourennane, E. Bachié, « Démonstrateur de nœuds mobiles communicants standalone », PIAVE AUTONOTEX project, Livrable 5.1.2, 30 Juin 2017.

[RC40] A. Gonzalez Santos, A. Frappé, P. Cathelin, A. Kaiser, « Traitement du Signal en Temps Continu pour les signaux Audio », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.15, 27 Novembre 2017.

[RC41] A. Gonzalez Santos, A. Frappé, P. Cathelin, A. Kaiser, « Optimisation du traitement numérique en temps continu en 28nm FDSOI », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.19, 31 Janvier 2018.

[RC42] D. Ghosh, A. Frappé, C. Loyez, A. Cathelin, « E/R (28 mn DFSOI) pour test sans contact de circuits sur wafer», Programme de recherche & développement coopératif NANO 2017, Livrable SP2.21, 26 Mars 2018.

[RC43] A. Gonzalez Santos, A. Frappé, P. Cathelin, A. Kaiser, « Logarithmic CTDSP filter bank for speech and voice activity recognition », Programme de recherche & développement coopératif NANO 2017, Livrable SP2.20, 18 Juillet 2018.

[RC44] A. Frappé, E. Bachié, « Démonstration de nœud mobile communicant mécaniquement flexible », PIAVE AUTONOTEX project, Livrable 5.2.2, 8 Novembre 2018.

B.3. Reproduction of selected publications

Here after are reproduced some of the publications related to this work. The selection is composed by:

1. **A. Frappé**, A. Flament, B. Stefanelli, A. Kaiser, A. Cathelin, “An All-Digital RF Signal Generator Using High-Speed ΔΣ Modulators”, IEEE Journal of Solid-State Circuits, vol.44, no. 10, pp. 2722-2732, Oct 2009
2. C. Thakkar, L. Kong, K. Jung, **A. Frappé**, E. Alon, “A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS”, IEEE Journal of Solid-State Circuits, vol.47, no. 4, pp. 952-968, Apr 2012
3. J. Muller, B. Stefanelli, **A. Frappé**, L. Ye, A. Cathelin, A. Niknejad, A. Kaiser, “A 7 -bit 18th order 9.6 GS/s FIR up-sampling filter for High Data Rate 60-GHz Wireless Transmitters”, IEEE Journal of Solid-State Circuits, vol.47, no. 7, pp. 1743-1756, Jul 2012
4. B. Grave, **A. Frappé**, A. Kaiser, “A reconfigurable IF to DC sub-sampling receiver architecture with embedded channel filtering for 60 GHz applications”, IEEE Trans. Circuits Syst. I-Regul. Pap., 60, 5, pp. 1220-1231, May 2013.
5. A. Werquin, **A. Frappé**, A. Kaiser, “A multi-path multi-rate CMOS polar DPA for wideband multi-standard RF transmitters”, Proceedings of 2013 IEEE Radio Frequency Integrated Circuits Symposium, IEEE RFIC 2013, Seattle, WA, USA, June 2-4, 2013, paper RTU2A-4, 327-330.
6. I. Sourikopoulos, **A. Frappé**, A. Cathelin, L. Clavier, A. Kaiser, “A digital delay line with coarse/fine tuning through gate/body biasing in 28nm FDSOI”, Proceedings 42nd European Solid-State Circuits Conference, ESSCIRC 2016, Lausanne, Switzerland, September 12-15, 2016.
7. R. C. Marin, **A. Frappé**, A. Kaiser, "Digital Complex Delta–Sigma Modulators with Highly Configurable Notches for Multi-Standard Coexistence in Wireless Transmitters," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, pp. 343-352, Jan. 2018.
8. F. T. Gebreyohannes, **A. Frappé**, P. Cathelin, A. Cathelin, and A. Kaiser, “All-Digital Transmitter Architecture Based on Two-Path Parallel 1-bit High Pass Filtering DACs,” in IEEE Trans. Circuits Syst. I Regul. Pap., vol. 65, no. 11, pp. 3956–3969, 2018.

A. Frappé, A. Flament, B. Stefanelli, A. Kaiser, A. Cathelin, “An All-Digital RF Signal Generator Using High-Speed ΔΣ Modulators”, IEEE Journal of Solid-State Circuits, vol.44, no. 10, pp. 2722-2732, Oct 2009

An All-Digital RF Signal Generator Using High-Speed $\Delta\Sigma$ Modulators

Antoine Frappé, *Member, IEEE*, Axel Flament, Bruno Stefanelli, *Member, IEEE*, Andreas Kaiser, *Member, IEEE*, and Andreia Cathelin, *Member, IEEE*

***Abstract*—An all-digital RF signal generator using $\Delta\Sigma$ modulation and targeted at transmitters for mobile communication terminals has been implemented in 90 nm CMOS. Techniques such as redundant logic and non-exact quantization allow operation at up to 4 GHz sample rate, providing a 50 MHz bandwidth at a 1 GHz center frequency. The peak output power into a 100 Ω diff. load is 3.1 dBm with 53.6 dB SNDR. By adjusting the sample rate, carriers from 50 MHz to 1 GHz can be synthesized. RF signals up to 3 GHz can be synthesized when using the first image band. As an example, UMTS standard can be addressed by using a 2.6 GHz clock frequency. The measured ACPR is then 44 dB for a 5 MHz WCDMA channel at 1.95 GHz with output power of −16 dBm and 3.4% EVM. At 4 GHz clock frequency the total power consumption is 120 mW (49 mW for $\Delta\Sigma$ modulator core) on a 1 V supply voltage, total die area is 3.2 mm^2 (0.15 mm^2 for the active area).**

***Index Terms*—CMOS, delta-sigma modulator, digital quadrature upconverter, digital transmitter, delay-locked loop (DLL), non-exact quantization, redundant arithmetic, RF signal generator, RF transmitters.**

I. Introduction

THE increasing demand for a personal device to be able to communicate on several radio systems, with different carrier frequencies, bandwidths, data rates and dynamic ranges, leads to the design of sophisticated RF front-ends for mobile terminals with increasing functionality and integration while continuously reducing cost and power consumption.

The digital-to-analog conversion in the transmitter is typically performed at baseband or intermediate frequencies (IF) of not more than a few hundreds of MHz [1]. The analog radio frequency (RF) front-end then comprises mixers, filters and amplifiers. Due to the lack of configurability, several front-ends are usually placed in parallel for addressing multiple standards, thus increasing silicon area.

The vision of the software radio is to perform the digital-to-analog conversion in the transmit path as close as possible to the antenna, ideally just before the antenna. All the processing is pushed in the digital domain to ease reconfigurability. However, the design of high dynamic range DACs at RF frequencies remains a challenge if reasonable power consumption is targeted.

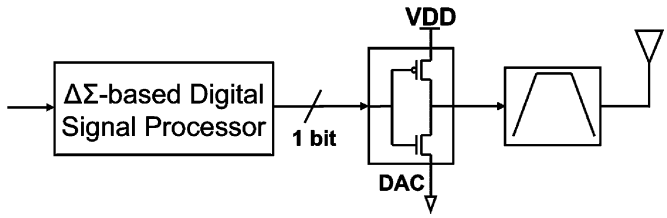

Fig. 1. Transmitter architecture based on 1-bit switched-mode power amplifier and $\Delta\Sigma$ modulation.

As an intermediate approach, [2]–[4] have introduced the concept of a digital RF transmitter using high-speed $\Delta\Sigma$ modulation associated with a class-S switched power amplifier acting as a single-bit DAC, as shown in Fig. 1. The $\Delta\Sigma$ modulator codes the input signal into a 1-bit sequence at a very high sampling rate (typically 4 times the carrier frequency), appropriate for driving the class-S power amplifier. The switched power amplifier has a theoretical 100% efficiency when working in voltage mode with an ideal filter. However, the low supply voltage of advanced CMOS processes limits the integration of a high-power class-S amplifier in a CMOS System-on-Chip (SoC) transmitter. The concept has however been used in [5] to implement a digital signal generator at IF frequencies.

More recently, multi-bit Digital-to-RF Converters (DRFC) have been introduced. The digital-to-analog converter and the mixer are merged into a single circuit. The digital input signal is upsampled and the number of bits reduced with a delta-sigma modulator [6]–[8]. The key advantage of that approach is the suppression of the analog baseband filter.

This paper describes the first fully integrated CMOS circuit implementing an all-digital signal generator based on a single-bit $\Delta\Sigma$ modulator directly at RF frequencies. The main goal is to demonstrate the feasibility of such an approach. For this purpose, a number of unconventional techniques have been used in the digital delta-sigma modulator to enable operation at clock frequencies of several GHz. While not able to deliver directly high power to the antenna, the circuit demonstrates that a complete transmitter up to the PPA could be implemented by an all-digital circuit. A passive filter, required at the output of the circuit to remove the quantization noise introduced by the delta-sigma modulator, and the PA would remain outside the CMOS SOC. An on-chip class-S PA would require high-voltage technology options. However, techniques such as

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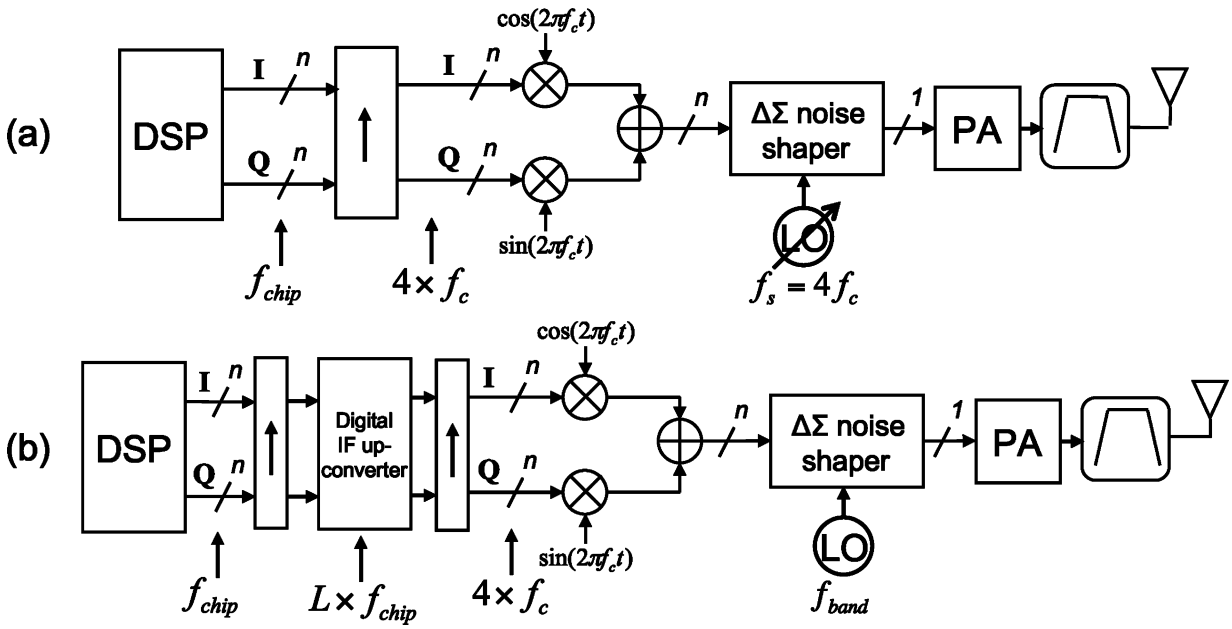

Fig. 2. Block diagram of (a) a direct upconversion and (b) a two-step upconversion ΔΣ-based transmitter.

power combining [9], [10] could allow reaching high power in low voltage processes. Moreover, as ΔΣ-modulated signals present a huge amount of quantization noise outside the band of interest, highly selective filtering is required at the output the class-S PA to meet the stringent requirements, especially to reduce spectral emission into the RX bands of the various communication standards.

This paper is organized as follows. Section II presents the digital RF transmitter architecture with an emphasis on architecture choices. The implementation of the ΔΣ modulator core is described in Section III. Its high-speed functionality has been achieved using design techniques such as redundant arithmetic and non-exact quantization. Section IV exposes the 90 nm digital RF signal generator chip design and Section V details the measurement results. Finally, other recent approaches to digital RF transmitters will be compared and discussed in Section VI, as well as means for relaxing the out-of-band filtering constraints.

II. ΔΣ-Based Digital RF Signal Generator

A. Architecture Description

The global function of the implemented digital signal generator is to convert a multi-bit digital I/Q baseband signal at baseband sampling rate (chip rate) into a single-bit digital RF signal at a very high sampling rate that can be converted to the analog domain. The underlying fundamental principles are oversampling and noise-shaping. ΔΣ modulators are used to shape the quantization noise in an appropriate way to move it out of the targeted transmit band.

The block diagram of a direct-conversion system is presented in Fig. 2(a). A digital signal processing block provides the signal to be transmitted, whatever the modulation scheme and the chip rate of the standard are. This digital signal will be oversampled up to 2 or 4 times the desired channel frequency before being mixed to RF frequencies and quantized to a 1-bit signal. An analog filter will be necessary at the output of the digital transmitter to remove the high out-of-band quantization noise from the ΔΣ modulation after amplification by a switched power or pre-power amplifier. Since the output filter will typically be a highly selective passive bandpass filter, covering the whole targeted standard's transmit band, the modulator must provide low quantization noise over the full transmit band. In a direct conversion approach, the useful frequency band of the modulators is centered on the desired channel. In order to assure low noise power over the full transmit band even for the channels at the lower and higher band edges, the ΔΣ modulator bandwidth must be twice the width of the transmit band [Fig. 3(a)].

To relax the noise shaper requirements, a two-step upconversion architecture has been adopted, as described in Fig. 2(b). The useful frequency band of the ΔΣ modulator remains now centered on the standard's transmit band frequency $f_{\rm band}$, regardless of the desired channel [Fig. 3(b)]. In the first step, the complex baseband signal is moderately oversampled and then upconverted to the desired IF channel by a digital multiplier. In the second step, the signal is oversampled up to the RF sampling frequency, transposed to RF and finally quantized with the 1-bit bandpass noise-shaper. Another advantage of fixed RF sampling frequency is relaxed phase-noise requirements on the RF sampling clock.

B. Oversampling Stages

In this two-step upconversion architecture, the oversampling process is divided in two blocks. A first oversampling stage brings the sampling rate up to, at least, two times the standard's bandwidth. This block should use half-band or similar digital filters. The second oversampling stage raises the sampling rate up to RF frequencies and is simply implemented as first-order

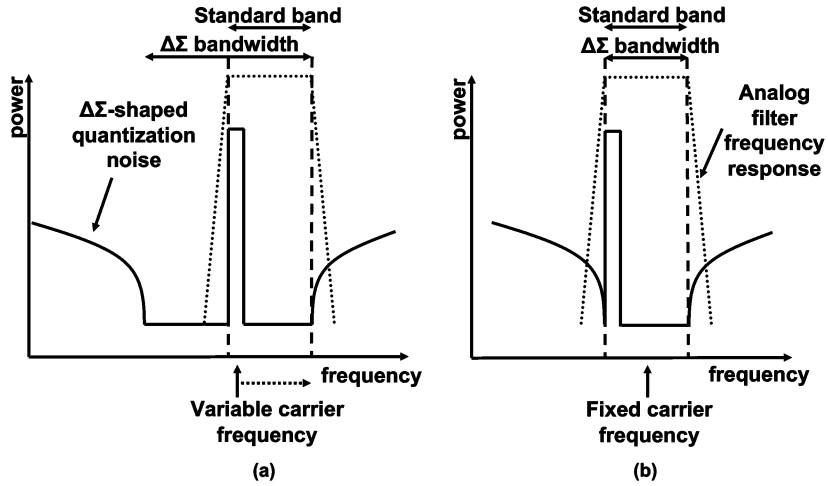

Fig. 3. $\Delta\Sigma$ modulator bandwidth requirements for (a) a direct upconversion architecture and (b) a two-step upconversion architecture.

hold interpolators. This is made possible because the resulting unattenuated images will be lower than the quantization noise brought by the $\Delta\Sigma$ modulation outside the useful band.

A major drawback in all-digital transmitters, in which the sampling clock is synchronized on the RF LO, is the fact that the ratio of the IF to the RF sampling frequencies is not necessarily integer, as one is related to the baseband chip rate and the other to the RF carrier frequency. The two ways to deal with this issue are, on one hand, to implement a non-integer sample rate conversion early in the baseband or, on the other hand, to slightly offset the RF sampling frequency to reach an integer ratio and to correct the channel center frequencies in baseband by the opposite amount. The second choice is easily implemented at no additional cost although it requires a margin on the modulator bandwidth.

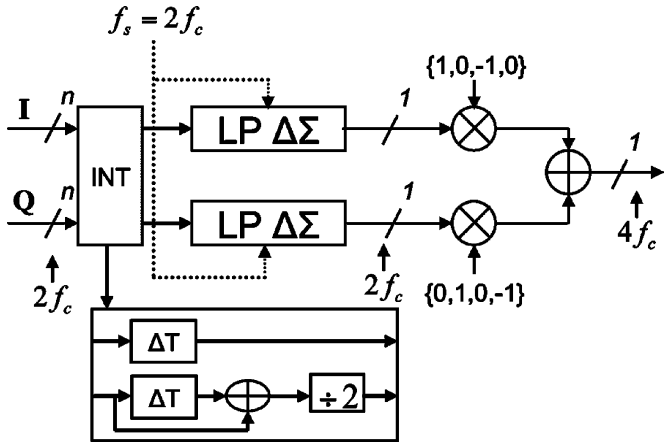

Fig. 4. Improved architecture using a 1-bit RF mixer, low-pass $\Delta\Sigma$ modulators and interpolation on Q channel to ensure good image rejection.

C. Mixer Stage

Upconversion of the digital IF signal to RF is achieved by a digital image-reject mixer [7], [11]. In the general case, two multipliers and a summer are required, all operating at the RF sampling frequency. By choosing the RF sampling frequency equal to 4 times the center frequency of the transmit band, the operation is however greatly simplified. In that case, the 90° phase shifted I and Q LO signals can be respectively represented by the digital sequences $[1, 0, -1, 0]$ and $[0, 1, 0, -1]$.

A simple multiplexer, selecting the I channel on odd periods and the Q channel on even periods, can replace the adder in the mixer. Furthermore, the multiplications are replaced by a simple change of the sign of the digital data, eliminating multipliers entirely. The digital RF output stream is then the following sequence:

$$RF_{\text{out}} = \{I(n), Q(n+1), -I(n+2), -Q(n+3)\}, \quad n = 0, 4, 8, 12, \ldots$$

D. Architecture Choices

Implementing two low-pass $\Delta\Sigma$ modulators and a 1-bit digital mixer is strictly equivalent to a n-bit digital mixer followed by a bandpass modulator. The first option offers the advantage of reducing the complexity of the mixer to a 1-bit multiplexer, as shown in Fig. 4, but two low-pass modulators must be implemented at the RF sampling rate. Nevertheless, it can be noticed that the input of the digital I/Q mixer actually samples only odd samples in I path and only even samples in Q path. If we do not produce the unnecessary samples, the effective sampling rate of the low-pass delta-sigma modulators in I and Q paths is only half of the RF sampling rate. This will not only halve the power consumption of the modulators but also relax the requirements on the digital logic in the modulators, as the cycle time is doubled.

The $\Delta\Sigma$ modulators should work in quadrature for proper operation. In practice, however, we would like to use the same sampling instants for the two low-pass $\Delta\Sigma$ modulators in I and Q paths. If we simply process only odd samples in both I and Q paths, an image of the transmit channel appears in the RF spectrum because of the slight phase shift of the Q path [12]. This is simply solved here by deriving the missing even Q samples from the odd ones through linear interpolation. As the oversampled I and Q input samples are identical for several periods, due to the previous first-order hold oversampling stage, only one out

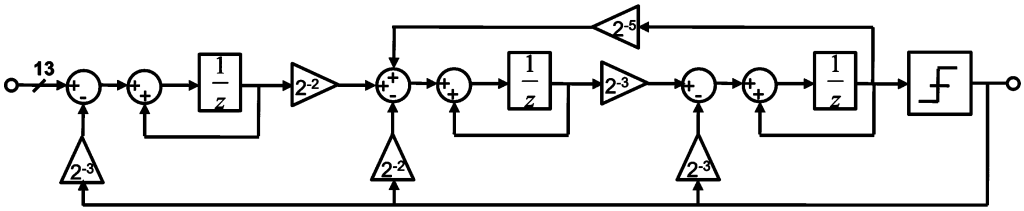

Fig. 5. Third-order ΔΣ modulator architecture.

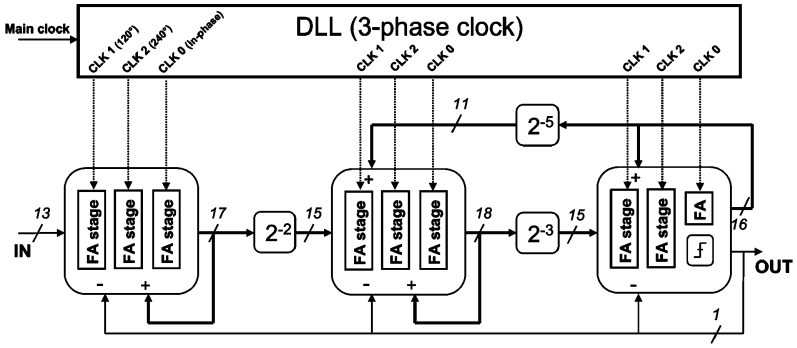

Fig. 6. ΔΣ modulator using Borrow-Save arithmetic, precomputed non-exact quantization and multiphase-clock produced by the DLL.

of 16 samples actually needs to be interpolated, leading to the architecture presented in Fig. 4.

III. Digital ΔΣ Modulator

A. ΔΣ Modulator Design

The low-pass ΔΣ modulator blocks will be designed to fulfill most standard requirements for in-band dynamic range. A third-order modulator with a 1-bit output data stream theoretically leads to approximately 80 dB of maximum SNR when an oversampling ratio of 40 is used. As the considered bandwidth is large, the noise has to remain almost flat in this band to keep performances constant over all channels. For this reason, zeros of the third-order noise transfer function have been placed at the edges of the desired band. The associated structure is presented in Fig. 5. and is made of integrators with a feedback from the output to the second integrator.

This architecture must be optimized to be suitable for a high-speed digital implementation. As an example, for UMTS systems, the required sampling frequency is 3.9 GHz, i.e., twice the 1.95 GHz center carrier frequency. That means the computations have to be done in the ~ 250 ps clock cycle, what is very stringent. First of all, all coefficients in the architecture are replaced by their closest power of two, becoming zero-delay right-shift operations. The word length for each signal has been determined from simulations of the architecture with typical input signals. The critical path is composed by the second integrator with input signals coming from the first integrator, the output and the local feedback. Dealing with the critical path requires the computation of several n-bit additions in a single clock cycle. No pipelining is allowed due to feedbacks that include right-shift operations. Ripple-carry adders, carry-select adders or carry-lookahead adders are not suitable here because the required number of successive Full-Adder (FA) cells remains large. We propose to use a redundant representation to overcome the 2's complement word-length dependent propagation delay [13]. The chosen borrow-save (BS) arithmetic enables carry-free additions by simply computing bit positions in parallel and saving carries in its representation, each bit position being doubled [14]. These latter ones can code either -1, 0 or 1 values for each weight. Moreover, the basic cells are signed-FA cells and are derived from classic FA cells by simply inverting one input and one output. A complete description of the computations with BS arithmetic can be found in [15]. The critical path is reduced to only three successive signed-FA cells as shown in Fig. 6.

A big issue associated with the BS representation is that the exact sign computation, inside the output quantizer, takes into account all bits, introducing again carry propagation along all bit positions. This introduces additional delay in the critical path at the output of the third integrator stage. We have demonstrated that non-exact quantization taking into account only a few most significant bits (MSBs) does not impact the dynamic performance of the ΔΣ modulator, due to the inherent error shaping function. This allowed computing the sign from only the three MSBs, reducing the output quantizer to a 3-input logic function [16]. Moreover, to further reduce latency, this block can be precomputed in parallel with the last full-adder cell of the third stage. This analysis is valid for this particular modulator. More or less complicated logic equations and precomputation schemes may be required for other architectures, depending on the robustness to the noise added by the non-exact quantizer. Nevertheless, borrow-save arithmetic and non-exact quantization techniques ease the implementation of very-high speed delta-sigma modulators.

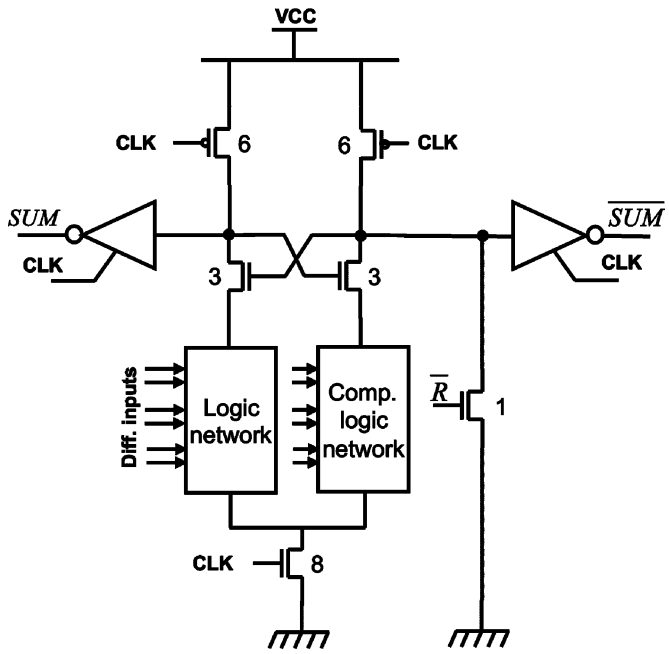

Fig. 7. Dynamic logic FA cell implementation with initialization circuitry. All lengths are minimal and indicated $W = 1$ refers to the minimum width.

B. FA Cell Transistor Implementation

Three FA stages have to be computed during a clock cycle inside each $\Delta\Sigma$ modulator stage. In a 90 nm technology, this is not so obviously realized and dynamic logic cells are designed to minimize propagation delays. No additional flip-flops are needed, as the storage function is implicitly implemented. However, each dynamic logic layer requires its own clock to be functional. Thus, for three logic layers, three clocks are needed, each delayed from the others by a third of the period. Fig. 6. illustrates the connection of the FA dynamic logic blocks. A DLL, detailed in a further section, generates the multiphase clock. Each differential dynamic logic layer will be evaluating the output in one third of a clock period.

Each dynamic logic block has two stages (Fig. 7): a precharge/evaluation stage followed by a hold/active clocked inverter (tri-state inverter). The structure is fully differential from a signal point of view, although each dynamic cell uses only a single phase clock. When the clock is low, intermediate nodes are precharged to the high state through the pMOS transistors and the outputs are high impedance. On the rising clock edge, outputs are made active and reflect the intermediate node evaluation. One of the intermediate nodes stays high, whereas the other one is discharged through the conducting FA nMOS logic and the clocked nMOS transistor. FA logic for sum and carry evaluation is not depicted here as it is simply a differential nMOS logic network.

If no care is taken, the two nodes of a differential signal could be equal when powering up the system. Then, as outputs are fed back to inputs, the non-differentiality of these signals keeps the circuit stable into this bad and non-operating state. So an initialization phase is needed. A reset transistor has been added on the complementary intermediate node. The reset transistor's width has been reduced in order to avoid conflicts when this node is precharged. The cross-coupled nMOS transistors have two purposes. The first one is to maintain a differential output signal whatever the inputs are. Only one side can discharge, as this automatically blocks the other side. Second, this structure acts as a latch, so it can operate at any frequency (of course limited by the worst case propagation delay). However, the addition of these cross-coupled transistors slightly slows down the operation, degrading the gate propagation delay from 50 ps to about 70 ps.

C. DLL-Based Multiphase Clock Generation

The three clock phases at 0°, 120° and 240° are generated by an on-chip Delay Locked Loop (DLL), detailed in Fig. 8. Its main component is a delay line in which delays depend on a control voltage. In this case, three identical delay elements are composed of an inverter with nMOS and pMOS transistors added in series in the main branch followed by a standard inverter. A phase detector drives a charge pump, which adjusts the control voltage in such a way that CLK0 will be exactly delayed by one period. CLK1 and CLK2 have then respectively a phase offset of 120° and 240°. Sample rates of inputs of the phase detector are divided by two to make succeeding stages uncritical.

In simulations with a 100 μA external current source for the charge pump, the calibration phase lasts between 50 and 100 ns for a few GHz clock. The locking error between CLK0 and the reference clock is around 5 ps, at 4 GHz clock frequency. Duty cycles are near 50% and rise and fall times are in the range of 20 to 40 ps. Three clock trees has been designed so as to equalize the insertion delays from the DLL to the dynamic cells of the $\Delta\Sigma$ modulator.

IV. Chip Implementation

The chip block diagram is shown in Fig. 9. Signal inputs are two 13-bit I and Q channels at a $f_s/32$ sample rate, f_s being equal to 4 times the chosen standard's center frequency. The chip comprises two 16-time first-order hold oversampling stages, including the image-reject interpolator on Q channel, two third-order low-pass $\Delta\Sigma$ modulators and the 1-bit digital mixer. The on-chip DLL creates the multi-phase $fs/2$ clocks from a clock signal provided by an external source.

The digital mixer is realized thanks to transmission gates and true single-phase clock flip-flops. Each transmission gate stage aims at choosing the appropriate I or Q signal or respective complementary signals to generate the sequence presented in Section II-C. The multiplexer outputs are synchronized on the main clock using flip-flops with matched setup times. This clock acts as the local oscillator when the output signal is interpreted in the analog domain.

The digital RF signal is buffered through sized CMOS inverters. The last one is made large enough to provide a 1 V drive into a 50 Ω load. It consequently acts as an almost ideal voltage source whose output impedance is approximately equal to 0.6 Ω. Its relative size is 24640/1 for the pMOS and 4500/1 for the NMOS, where 1 stands for the minimum feature size in

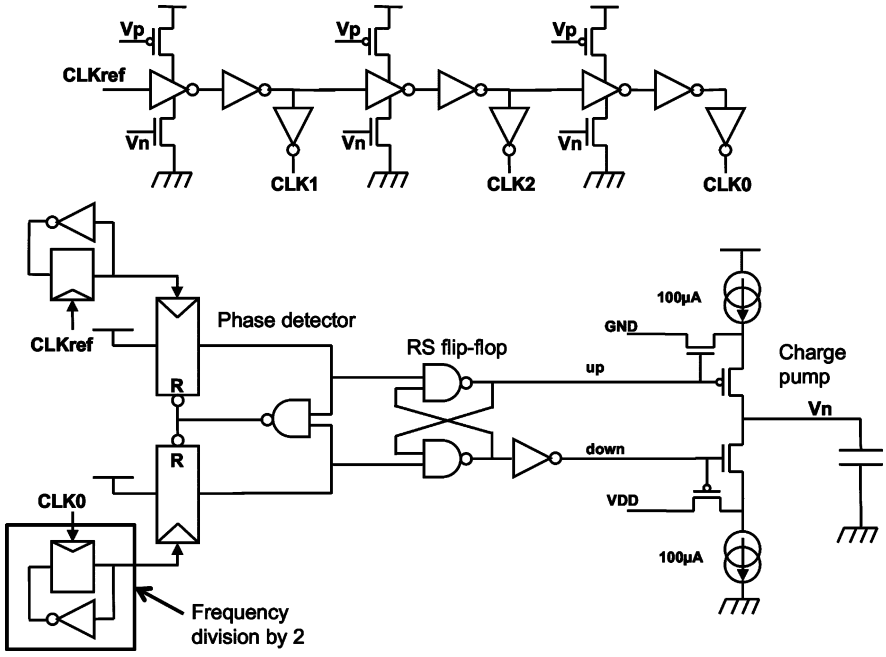

Fig. 8. DLL core implementation.

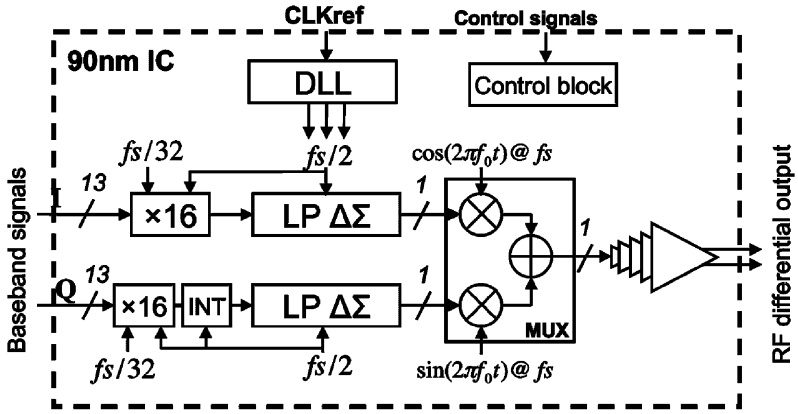

Fig. 9. System view of the designed 90 nm CMOS chip.

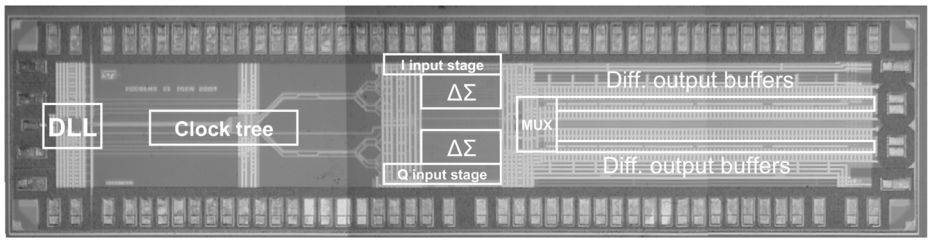

Fig. 10. Chip microphotograph.

CMOS 90 nm technology. The output structures are fully differential as this prevents inter-symbol interference.

The complete chip has 103 pads and occupies 4×0.8 mm^2 in STMicroelectronics 90 nm GP CMOS process [17]. However, the implemented test-chip is pad-limited and the total active area is only 0.15 mm^2. The die microphotograph is shown in Fig. 10.

V. Measurement Results

A. Single Carrier Measurements

The fabricated chip operates for clock frequencies up to 4 GHz, thus leading to an RF signal having a maximum bandwidth of 50 MHz at a 1 GHz center frequency. The measured RF output spectrum in the analog domain at maximum clock

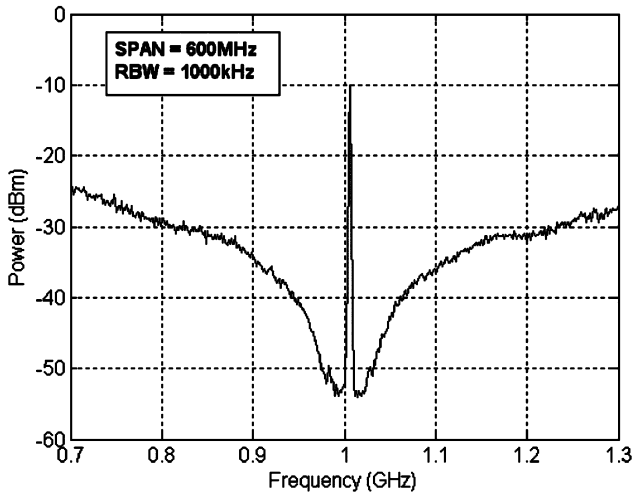

Fig. 11. Wideband output spectrum demonstrating the functionality for a 1 GHz carrier frequency (4 GS/s internal sampling frequency).

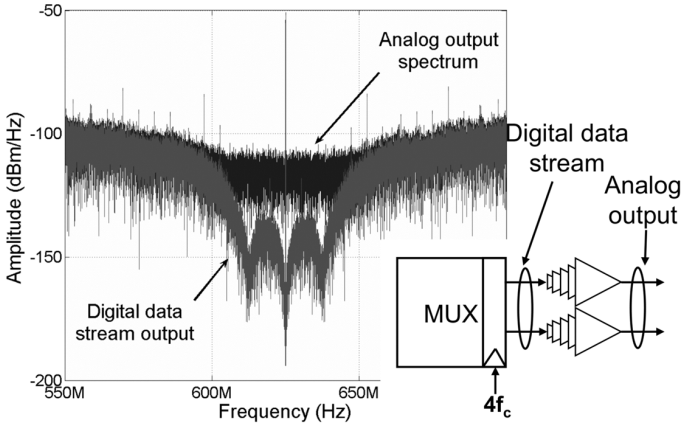

Fig. 12. Digital and analog spectrum measurements for a 2.5 GHz sampling clock. The digital data stream spectrum shows the desired $\Delta\Sigma$ noise shaping.

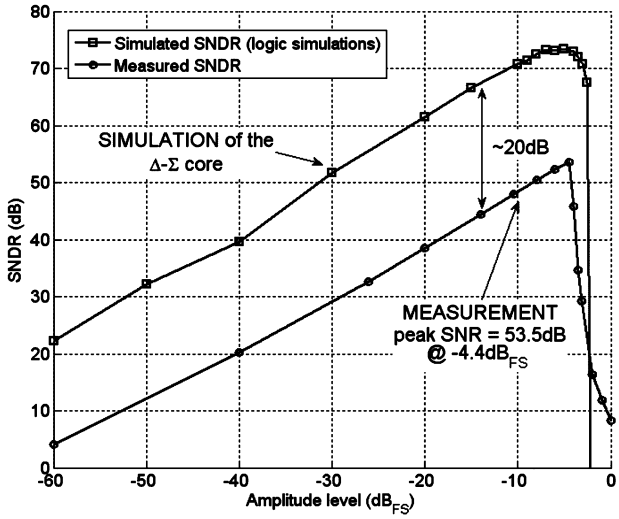

Fig. 13. In-band SNDR versus input amplitude for core simulation and measurement. 0 $\mathrm{dB_{FS}}$ refers to a full-scale sine wave.

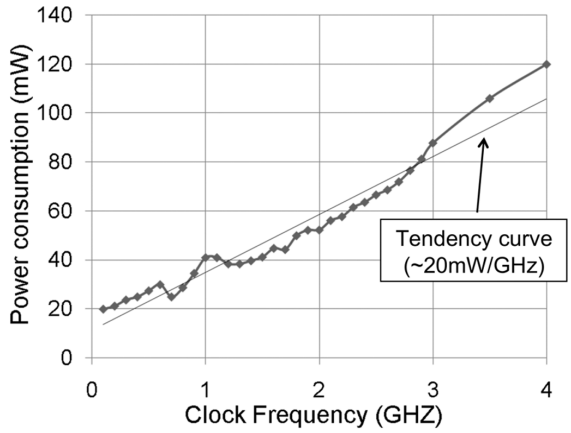

Fig. 14. Chip total power consumption as a function of the sampling clock frequency and tendency curve.

frequency is shown in Fig. 11. The noise transfer function can be clearly observed. However, noise transfer function zeros at the edges of the band are below the noise floor. Small peaks at 25 MHz offset from the carrier frequency are measurement artifacts due to the coupling between the baseband signal generation instrument and the chip itself.

The output signal has been acquired with a digitizing oscilloscope at 2.5 GHz sampling frequency, sampled and quantized as 1-bit values, deleting the effects of voltage variations, jitter and inter-symbol interferences introduced by the digital-to-analog conversion in the output stage. The spectra of the reconstructed digital output signal and the corresponding analog output signal are plotted in Fig. 12. The shaping of the quantization noise with zeros placed at either edge of the band can be clearly seen in the spectrum of the digital signal and corresponds precisely to the simulated core performance. The measured mean in-band noise floor is -146.5 dBm/Hz and the SNDR is 72.15 dB. However, the analog output signal exhibits higher noise in the band. The noise of the analog output signal can be related to supply voltage variations that cause variations of the threshold and delay of inverters in the output stages. Moreover, the clock input buffers are also very sensitive to voltage variations. This translates to uncorrelated jitter on the edges of the output signal and a higher noise floor in the signal band. The output jitter has been measured to be around 13 $\mathrm{ps_{RMS}}$, which is significantly higher than the expected value of 2 $\mathrm{ps_{RMS}}$. To quantify the degradation, the Signal-to-Noise and Distortion Ratio (SNDR) of the output signal has been measured for a digital sinusoidal input signal at 12 MHz, with amplitude ranging from -60 $\mathrm{dB_{FS}}$ to 0 $\mathrm{dB_{FS}}$. The measured noise floor is about 20 dB higher than expected from simulations of the $\Delta\Sigma$ core, as shown in Fig. 13, but these non-idealities would be reduced in future prototypes. Power consumption of this chip is plotted in Fig. 14. versus the clock frequency. With a 4 GHz main clock frequency, the total power consumption is 120 mW including output stages, while the core only consumes 49 mW. Measurement results are summarized in Table I.

B. UMTS Test Case Measurements

As the circuit is targeted at mobile communication applications, performance has been confronted to specifications of

TABLE I
EXPERIMENTAL RESULTS AT MAXIMUM FREQUENCY

Clock frequency	4GHz
Bandwidth	50MHz
Carrier frequency	1GHz
Analog output peak SNDR	53.5dB
Digital data peak SNDR	72.15dB
Core consumption	49mW

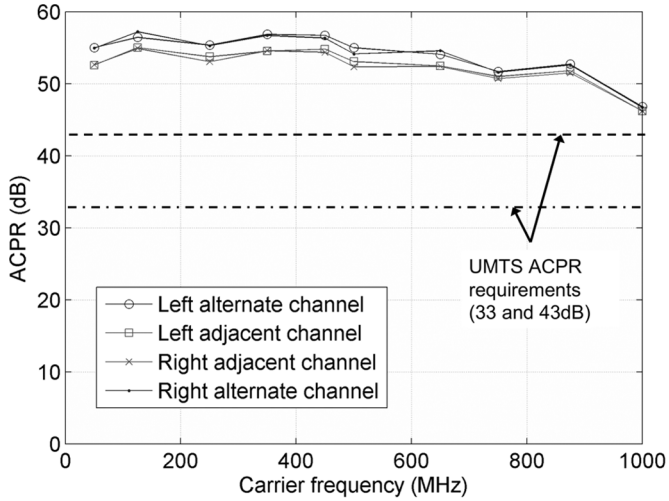

Fig. 15. ACPR versus carrier frequency for the fundamental band.

the European UMTS standard that implements WCDMA with 5 MHz channel spacing. ACPR requirements for adjacent and alternate channels are respectively 33 and 43 dB.

To demonstrate the configurability of this signal generator, the clock frequency has been swept to address carrier frequencies from 50 MHz up to 1 GHz. The ACPR has been measured for channel widths proportional to the carrier frequency, leading to the plot in Fig. 15, on which UMTS requirements have been plotted for reference. UMTS ACPR requirements are met for all carrier frequencies. However, the bandwidth is not adjustable and is proportional to the carrier frequency. Further improvements are needed to allow bandwidth reconfiguration through adaptive placement of poles and zeros in the ΔΣ modulator's noise transfer function.

The UMTS standard's principal transmit band is 60 MHz wide and centered at 1.95 GHz. This band can only be reached by using the first image band when operating the chip at 2.6 GHz clock frequency. The fundamental band is then at 650 MHz. The useful bandwidth, proportional to the sampling frequency, is reduced to 30 MHz in both the fundamental and the image band. Also, a 10 dB attenuation of the signal is observed in the image band, due to the sin_c shaping function, as shown in Fig. 16. The noise floor in the image band has been measured to be 3 dB lower than in the fundamental band, limiting the total degradation of the SNR to 7 dB.

Fig. 17 shows in-band spectra for a 5 MHz WCDMA QPSK channel at maximum power, for the fundamental and the image band. The input signal has 8.1 dB PAPR. The plot is centered on the channel of interest and the adjacent and alternate channels are shown on each side. The in-band noise floor dominates

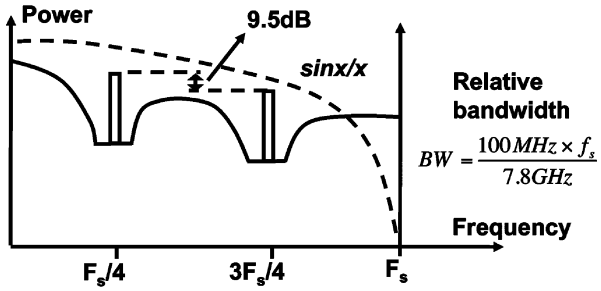

Fig. 16. Use of the first image band for UMTS test case.

the ACPR measurements. In the fundamental band, the measured ACPR is around 52 dB, while it degrades to 44 dB in the image band because of the lower SNR. The measured in-band power on a single-ended 50 Ω load is respectively −3.9 dBm and −15.8 dBm. The ACPR versus channel power is plotted in Fig. 18 for the 650 MHz and 1.95 GHz bands. The maximum ACPR is 53.6 dB and 44.3 dB, respectively. At maximum power, UMTS requirements are met even in the image band at 1.95 GHz.

At maximum power, error vector magnitude (EVM) for the 3.84 MS/s RRC filtered QPSK signal after downconversion is measured to be 1.24% in the 650 MHz band and 3.42% in the 1.95 GHz band (Fig. 19). For reference, the UMTS standard specifies EVM below 17.5% for output power at the antenna connector above −20 dBm. Typical performance of analog transmitters is 7 to 8%. Table II sums up the measurements related to the UMTS test case. The maximum sinusoidal differential output power on a 100 Ω load is respectively 3.1 dBm and −8.6 dBm for the fundamental and image band. The power consumption of the complete circuit is 69 mW for a 1 V supply voltage, each modulator core consuming less than 15 mW.

VI. DISCUSSION

This work is the first reported 1-bit digital RF signal generator using ΔΣ modulation, suitable for integration into a complete transmitter chain. Table III compares this work to recent approaches for highly digital RF transmitters in comparable CMOS technologies. The nearest implementation of a single-bit bandpass modulator is the one by Sommarek *et al.* in 2004 for IF frequencies [5]. However, only a single UMTS channel is covered at 175 MHz IF frequency.

Other authors use the recently introduced digital-to-RF conversion (DRFC) approach [18], where a multi-bit D/A converter is merged with an image-rejection mixer into the DRFC block. In [6], the UMTS I and Q channels are oversampled to a 10-bit 307.2 MS/s signals before being applied to the DRFC. In [7], a ΔΣ modulator is used to reduce the number of bits required in the DRFC to 3 bits. The ΔΣ modulator uses a second-order pipelined MASH structure and operates with a 2.625 GS/s sample rate. The circuit is targeted at the 5 GHz WLAN.

Finally, [8] presents a 65 nm CMOS transmitter for IEEE 802.11 b/g and 802.16e WLAN and WiMax standards in the 2.4–2.7 GHz band. It uses a pipelined MASH ΔΣ modulator to reduce the LSBs, creating a 6.15b signal (71-state word)

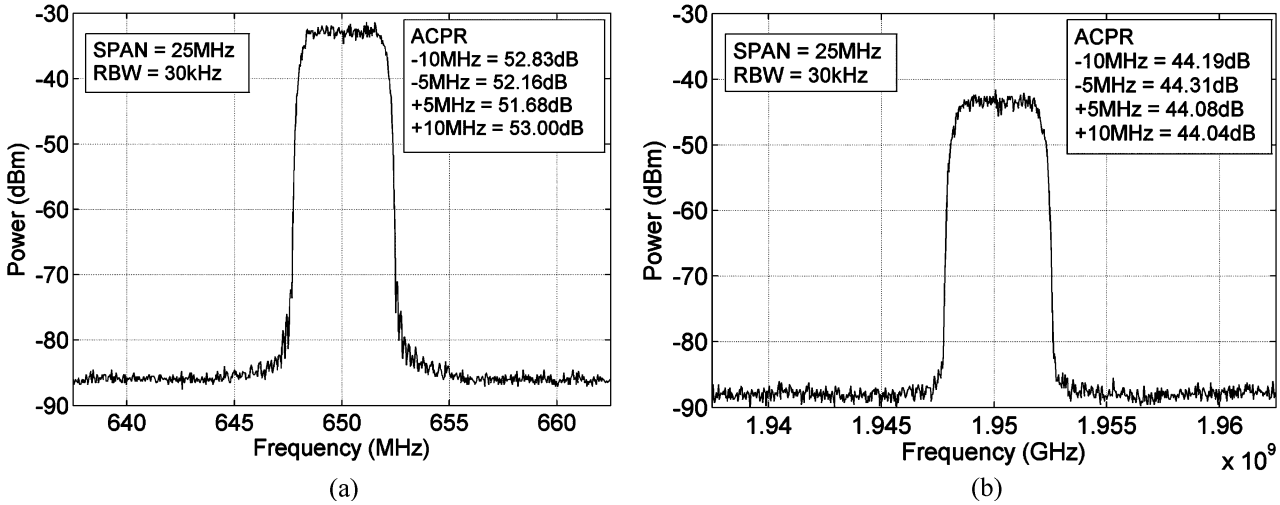

Fig. 17. In-band spectrum measurements for a 5 MHz WCDMA channel for the fundamental band (a) and the image band (b).

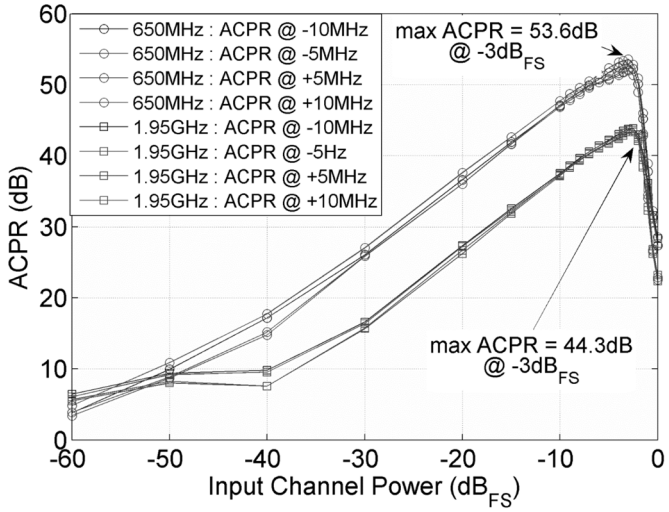

Fig. 18. ACPR versus channel power for adjacent and alternate channels in fundamental and image bands.

TABLE II
SUMMARY OF MEASUREMENTS AT A 2.6 GHZ CLOCK FREQUENCY

		650MHz band	1.95GHz image band
Max ACPR (5MHz wide channel)		53.6dB	44.3dB
Max Channel Power		-3.9dBm	-15.8dBm
EVM		1.24%	3.42%
Peak output power		3.1dBm	-8.6dBm
Power consumption	total	69mW (1V)	
	output stages	39mW	
	core	2 × 15mW	

at the RF-DAC input. The measured ACLR are 42.8/46.2 dB for 20 MHz channels at maximum power (2.6 dBm). EVM is around 2% and the transmitter offers a large 64 dB power control range. The current consumed at maximum power is 210 mA.

We can see from Table III that the DRFC approach offers similar performances. This is principally related to the use of current mode output, allowing the implementation of a multi-bit DAC, analog power control and good immunity to power supply noise in a differential structure. The single-bit voltage-mode approach, on the other hand, produces more out-of-band quantization noise, but is more flexible and inherently linear and gains high interest if efficient class-S power amplifiers become feasible.

A good choice for the output filter would be BAW filters, due to their high selectivity and good integration [19]. However, filtering requirements could be relaxed through semi-digital FIR RF filtering [9] or reconfigurable higher order complex $\Delta\Sigma$ modulator topologies [20], which could offer flexibility on the position of zeros in the noise transfer function, in order to tune the bandwidth and adaptively reduce quantization noise in critical bands such as the UMTS RX band or receive bands of other standards. This architecture becomes promising to replace existing analog approaches if the configurable signal generator, the PA and filter stages can be integrated together, what remains a challenge to be addressed.

VII. CONCLUSION

An all-digital RF signal generator using $\Delta\Sigma$ modulation and targeted at transmitters for mobile communication terminals has been implemented in 90 nm CMOS. Techniques such as redundant logic and non-exact quantization allow operation at up to 4 GHz sample rate, providing a 50 MHz bandwidth at a 1 GHz center frequency. The peak output power into a 100 Ω diff. load is 3.1 dBm with 53.6 dB SNDR. By adjusting the sample rate, carriers from 50 MHz to 1 GHz can be synthesized. RF signals up to 3 GHz can be synthesized when using the first image band. As an example, UMTS standard can be addressed by using a 2.6 GHz clock frequency. The measured ACPR is then 44 dB for a 5 MHz WCDMA channel at 1.95 GHz with output power of -16 dBm and 3.4% EVM. At 4 GHz clock frequency the total power consumption is 120 mW (49 mW for $\Delta\Sigma$ modulator core) on a 1 V supply voltage, total die area is 3.2 mm^2 (0.15 mm^2 for the active area). The power required for the digital signal generator is comparable to analog implementations

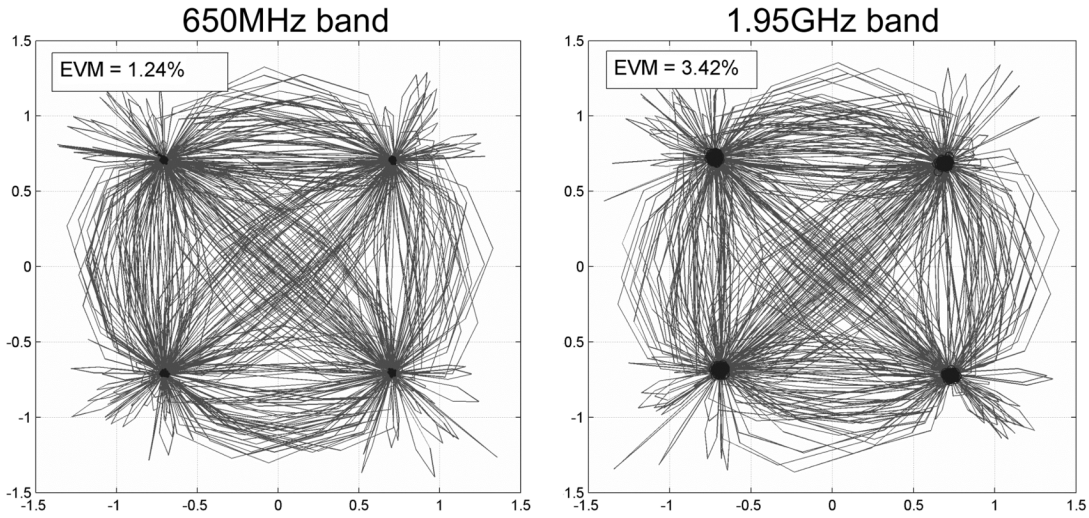

Fig. 19. IQ constellations for the fundamental (right) and image band (left).

TABLE III
COMPARISON TO STATE-OF-THE-ART

	This work	[5] 2004	[6] 2007	[7] 2007	[8] 2008
ΔΣ mod.	3rd order LP	4th order BP	-	2nd order MASH LP	3rd order MASH LP
DAC structure	1-bit	1-bit	10-bit DRFC	3-bit DRFC	6-bit DRFC
Sample rate	up to 4GS/s	700MS/s	307.2MS/s	2.625GS/s	5.4GS/s
Sample rate sync. on LO	yes	yes	no	no	yes
Carrier frequency	1GHz	175MHz	1.9GHz	5.25GHz	2.7GHz
Bandwidth	50MHz	5MHz	-	200MHz	-
ACPR	53.6dB	40.3dB (alt)	58dB (adj)	-	43dB (adj)
EVM	1.24%	-	<2%	-	2.1%
Output channel power	-4dBm	-	-2dBm	-	+2.6dBm
Max saturated output power	+3.1dBm	-	+1.9dBm	-8dBm	-
Power consumption	69mW @ 2.6GHz 120mW @ 4GHz	139mW	157mW	187mW	210mW
Area	0.15mm2	5.2mm2	1mm2	0.72mm2	0.35mm2
Process	90nm	130nm	130nm	130nm	65nm

in same technologies, but the digital approach offers reconfigurability, a large bandwidth and the possibility to use efficient output stages. This system is well suited for scalability. We can expect that a further technology shrink will result in even lower power consumption.

ACKNOWLEDGMENT

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A 10 Gb/s 45 mW Adaptive 60 GHz Baseband in 65 nm CMOS

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***Abstract*—This paper presents a low-power mixed-signal adaptive 60 GHz baseband in 65 nm CMOS. The design integrates variable gain amplifiers, analog phase rotator, 40-coefficient I/Q decision feedback equalizers (DFEs), clock generation and data recovery circuits, and adaptation hardware. The baseband achieves 10 Gb/s operation with BER $< 10^{-12}$ while consuming 53 mW (adaptation on)/45 mW (adaptation off), of which the core signal processing circuits consume only 29 mW.**

***Index Terms*—Carrier recovery, clock & data recovery (CDR), decision feedback equalizer (DFE), mixed-signal, phase rotator, sign-sign LMS, variable gain amplifier (VGA), 60 GHz.**

I. Introduction

THE 7 GHz of bandwidth available in the 60 GHz band [1] offers an opportunity to achieve multi-Gb/s wireless links. For this reason, ultra-high data-rate wireless communication over the 60 GHz band has gained increasing interest from both academic [2]–[4] and industrial groups [5]–[7]. Commercial transceiver solutions using the WirelessHD standard for applications such as home HDTV streaming are already available [8] and transceivers satisfying the WiGig [9] standard for multi-Gb/s wireless connectivity of electronic devices are expected to be available in the near future.

Despite operating at much higher carrier frequencies and bandwidths, today's 60 GHz radios often bear significant resemblance to lower frequency designs. For example, similar to today's 802.11a/b/g/n wireless LAN radios, current 60 GHz radios often rely on Orthogonal Frequency Division Multiplexing (OFDM). This choice of modulation scheme requires relatively high levels of circuit and signal processing complexity, and hence typical 60 GHz implementations utilize the traditional system partitioning shown in Fig. 1. The RF front-end provides directionality (typically using a phased array), and performs low-noise amplification followed by downconversion and (optionally) filtering, while the baseband comprises of the data-converters and digital signal processing (DSP). The DSP performs the requisite signal-conditioning to counter the non-idealities of wireless communication, such as OFDM

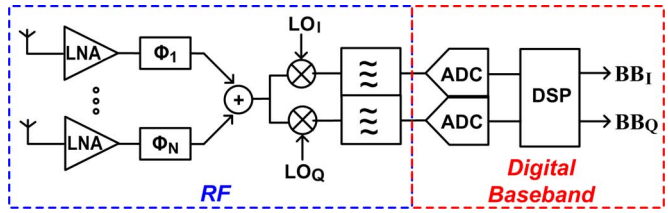

Fig. 1. Typical implementation of a wireless receiver.

de-modulation (or compensating inter-symbol interference in a single-carrier link), performing carrier phase/frequency recovery, clock/data recovery, and error-control coding/decoding.

Following this traditional radio implementation strategy, today's 60 GHz basebands dissipate roughly 1 W of power [10]—which is likely to limit the use of these designs in mobile/hand-held devices. Although at first glance one may assume that the multi-GS/s data converters are responsible for the majority of this power, recent advances in such data-converter designs [11]–[13] indicate that even a 5 GS/s ADC with ~5-bit resolution would dissipate well under 25 mW. A closer examination thus reveals that the power of a typical 60 GHz baseband is dominated by the various DSP blocks. The reasons for this can be illustrated by tallying the power required by highly optimized exemplary digital components with similar data-rates and functionality as the constituent signal processing blocks in a 60 GHz transceiver. For example, a 12-tap FIR filter in 90 nm CMOS demonstrated in [14] consumes 320 mW at 12 GS/s. Similarly, a 10GBASE-T ethernet low-density parity-check (LDPC) decoder implemented in 65 nm CMOS running at a 6.67 Gb/s throughput consumes 144 mW from a scaled (0.7 V) supply [15].

Since the DSP power required by OFDM and/or single-carrier frequency-domain equalization (SC-FDE)-based transceivers will likely be too high for mobile/hand-held devices, it is worthwhile examining alternative communication systems and implementations to seek inspiration for lower-power solutions. In particular, high-speed chip-to-chip electrical links have demonstrated that for high bandwidths and relatively low dynamic range (implying simple modulation such as 2-PAM), analog processing combined with a minimal number of comparators can be significantly more efficient than ADC/DSP-based solutions. Specifically, the energy-efficiency achieved by current state-of-the-art serial link designs using mostly analog processing is ~1 mW/Gb/s [16], [17] while operating at up to 12 Gb/s. For applications with even higher channel losses (25–35 dB) such as backplane-based transceivers

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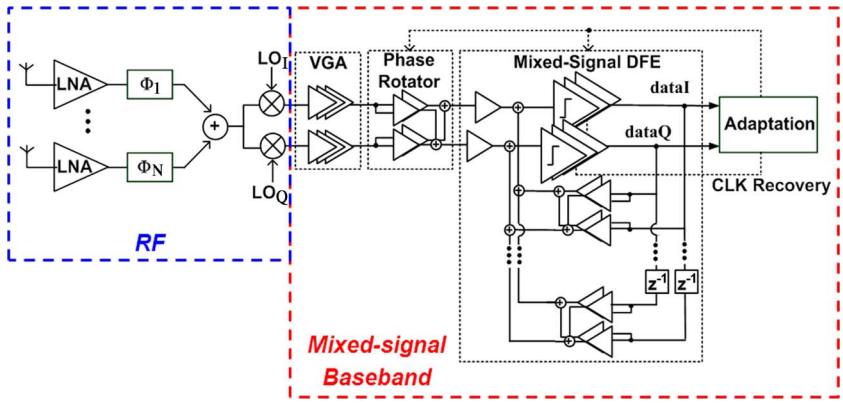

Fig. 2. 60 GHz mixed-signal receiver. This paper describes the design of the baseband.

requiring high transmit swings (0.6–1.2 V) and powerful equalizers (with as many as 14 taps of equalization), recent serial link designs [18], [19] have been able to achieve data-rates of 12–16 Gb/s with energy efficiencies of 8–15 mW/Gb/s. The key benefit offered by analog processing for moderate dynamic range (<6 bits) is that by using lower transistor width (and hence lower capacitance) per operation, analog processing consumes lower power than digital processing [20]. Note that serial links do use digital processing for certain high precision computations; however, since this processing is mostly limited to low-speed calibration/control circuitry, it does not incur a significant power penalty.

Noticing the potential advantages offered by analog/mixed-signal processing, previous works have demonstrated single-carrier mixed-signal baseband approaches suitable for ∼1–2 Gb/s 60 GHz links [21], [22]. Further work [2] enabled mixed-signal 60 GHz basebands operating at higher data-rates (up to ∼10 Gb/s), but with limited equalization capabilities and manual external control. This work (Fig. 2) therefore extends upon these previous designs by presenting a mixed-signal baseband RX in 65 nm CMOS capable of adaptively equalizing significantly longer delay spreads as well as automatically recovering both TX/RX carrier and baseband clock phase/frequency differences. The design supports data-rates up to 10 Gb/s using QPSK modulation and consumes a total of at most 53 mW, substantially easing the power consumption bottleneck for 60 GHz in mobile devices.

The first challenge facing any single-carrier 60 GHz baseband is the need to equalize against relatively long multi-path interference profiles. As will be described in the next section, this is particularly challenging in a mixed-signal design since traditional equalizer designs can only support a limited number of coefficients at a given data-rate. The next section therefore also describes the design of a cascode-summing decision feedback equalizer (DFE) that substantially increases the number of achievable coefficients. Section III then reviews equalizer coefficient adaptation, and clock/data recovery, before introducing an algorithm for performing carrier phase/frequency recovery using sign-sign LMS. The circuit design of the remaining baseband components—the VGA, phase rotator, and clock generation—is then described in Section IV. Finally, in order to experimentally verify the proposed techniques, Section V describes measured results from a 65 nm mixed-signal baseband test-chip.

II. Design of Mixed-Signal DFEs With Many Coefficients

A mixed-signal DFE that operates by summing current steering DACs [2], [21] is an excellent candidate for efficiently removing post-cursor inter-symbol interference (ISI). One of the challenges of using such a DFE for targeted symbol rates as high as 5 GS/s is that a 60 GHz channel may exhibit 30–50 complex taps of post-cursor ISI, even with a directional front-end [23]. Complex taps refers here to the presence of both in-phase and quadrature components. Therefore, in the context of an I/Q baseband, each complex tap consists of (a) a direct coefficient from I-to-I or Q-to-Q channels and (b) a cross-coefficient from I-to-Q or Q-to-I channels. In [21] Sobel and Brodersen described a mixed-signal equalizer for a 60 GHz channel covering 32 ns of multipath delay spread with 16 physical coefficients, but the design was limited to operating at only up to 1 Gb/s. While mixed-signal DFEs for wireline applications with up to 14 coefficients and data-rates as high as 16 Gb/s have been demonstrated [19], a 60 GHz channel requires even more coefficients. As will be shown shortly, when directly extended to 60 GHz, these DFEs prove to be inefficient in power consumption.

The fundamental limits of conventional current-steering mixed-signal DFEs can be understood by analyzing the design shown in Fig. 3. The circuit cancels post-cursor ISI by subtracting currents representing the ISI coefficients at a resistive load. The ISI cancelation currents are implemented by using current steering DACs, whose magnitude and sign represent the ISI magnitude and direction respectively. The summing node of this structure is loaded by the parasitic capacitance of the current-steering switches. At a given data-rate, since the DFE must satisfy a certain settling time requirement, this means that as the number of coefficients is increased, both the DFE cursor and coefficient currents must be increased. Scaling of these currents compensates for the increased loading and maintains a constant summing node bandwidth. As the number of coefficients gets even higher, the structure is self-loaded to

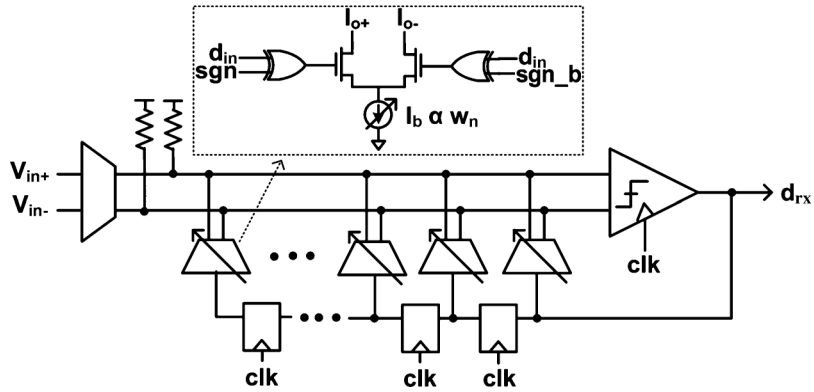

Fig. 3. Conventional mixed-signal DFE using current-steering DACs for ISI cancelation.

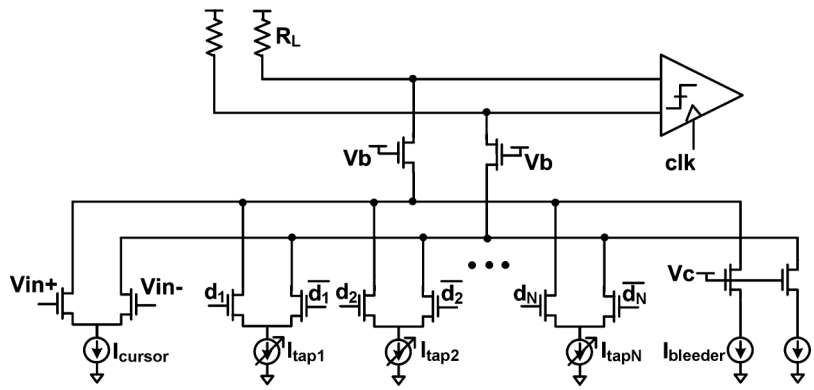

Fig. 4. Proposed cascode current-summing DFE (feedback shift registers not shown).

a limit where an infinitely large increase in current is required to add more taps.

To illustrate this formally, the power (P_{conv}) of such a conventional DFE (Appendix I) is given by

$$P_{conv} \propto \frac{I_{nom}}{1 - \frac{GBW}{\omega_{T,cursor}} \cdot \gamma \cdot \left(1 + k \cdot \frac{V_{in}}{V^*} \cdot \beta \cdot N_{coeff}\right)} \quad (1)$$

where $I_{nom} = C_L \cdot GBW \cdot V^*$ is the nominal current consumption of a class-A amplifier without self-loading, C_L is the external load capacitance, GBW is the DFE gain-bandwidth product, V^* is defined by $2I_D/g_m$ of the input transistors, γ is the ratio of drain to gate capacitance, V_{in} is the input voltage swing, $\beta = 2\omega_{T,cursor}/\omega_{T,coeff}$ and N_{coeff} is the number of DFE coefficients, each of which can cancel ISI up to a maximum amplitude of k times the cursor.

The two negative terms in the denominator of (1) represent the self-loading due to the cursor and equalizer coefficients respectively. As N_{coeff} becomes large (implying that the denominator approaches 0), the coefficient self-loading makes it infeasible (at any power) to achieve the bandwidth required for operation at a given rate. Therefore, in typical multi-GS/s DFE implementations, only a relatively limited number of coefficients can be implemented efficiently. Moreover, since the channel to be equalized is typically unknown ahead of time (or rather, for a wireless channel, it varies with time), the DFE needs to incorporate a certain amount of reconfigurability into each coefficient. Implementing such flexibility invariably involves an overdesign of the coefficients in terms of their current-handling capability (i.e., k becomes large), which exacerbates the self-loading of a conventional summing structure. As shown in Fig. 5, at the desired data-rate of 5 GS/s in a 65 nm CMOS technology, a conventional DFE structure, with each coefficient maximally able to cancel up to 0.5X of the cursor amplitude, can implement only ~10 complex taps efficiently.

A. Cascode Summation DFE

In order to significantly increase the number of taps that can be efficiently cancelled by a mixed-signal DFE, this work proposes to isolate the summation node from the final output of the structure through the addition of a cascode device, as shown in Fig. 4. To elucidate the benefits of this proposed structure, one must re-examine the constraints driving the design of a typical current-steering DFE.

In a current-steering DFE, the maximum magnitude of ISI to be canceled by each coefficient over any possible channel sets the width of the current steering switch associated with that coefficient. In other words, the current steering switch must be sized to handle this maximum ISI current. For example, if all coefficients have the same worst-case ISI, and the capacitive loading associated with handling this maximum ISI current is C_{par}, then the total loading at the summation node from N_{coeff} is $N_{coeff} \cdot C_{par}$. However, at any given time, no individual channel will have all ISI coefficients at their maximum magnitude simultaneously. Therefore, all coefficient currents will never be set to their maximum magnitudes at the same time. In other words,

$$I_{ISI,max} < N_{coeff} \cdot I_{max} \quad (2)$$

where I_{max} is the maximum current in each coefficient and $I_{ISI,max}$ is the maximum possible sum of currents in all coefficients. Thus, since the DFE will never actually handle this much current, loading the summation node with a capacitance of $N_{coeff} \cdot C_{par}$ is inefficient. In a conventional design, this inefficiency leads to a significant penalty in the number of coefficients that the mixed-signal DFE can implement at a given data-rate—especially at relatively high data-rates.

The proposed cascode current summation structure mitigates this penalty by summing all of the current through a cascode transistor, as shown in Fig. 4. The cascode transistor can be sized to handle only the bounded ISI current. The cascode transistor width is therefore much smaller than the sum of current steering switch widths, thus reducing the loading at the final output of the DFE and increasing the bandwidth of the output node. Similarly, the large capacitance of the current-steering switches is moved to the low-impedance cascode source, increasing the bandwidth of this node as well. In fact, in order to ensure high bandwidth at the cascode source, the cascode transconductance can be increased by flowing additional common-mode current. Increasing the achievable bandwidth of both nodes implies that the number of coefficients can be increased relative to a conventional design operating at the same data-rate.

To show this more formally, as derived in Appendix II, the power (P_{casc}) of a cascode-summing DFE is approximately as shown in equation (3) at the bottom of the page, where GBW_{casc} is the product of DFE gain and output node bandwidth, ω_T refers to the unity current-gain frequency, ω_{casc} is the cascode bandwidth, $k_{ISI,max}$ is the maximum possible total ISI amplitude with respect to the cursor, and $\beta = 2\omega_{T,cursor}/\omega_{T,coeff}$. It must be noted that since the cascode summing structure has two poles—one each at the output and the cascode source—in order to maintain the same effective bandwidth as a conventional DFE, both of these poles (and hence the GBW_{casc}, for equal gain) must be $\sim \sqrt{2}$ times higher than a conventional design. As a result, $I_{nom,casc} = \sqrt{2} \cdot I_{nom}$.

Compared to the power consumption of a conventional current summing structure (2), the self-loading term that is proportional to N_{coeff} is reduced by a factor of $(1/2\gamma) \cdot (\omega_{T,casc}/\omega_{casc})$. Intuitively, this benefit is proportional to $(\omega_{T,casc}/\omega_{casc})$ since the cascode bandwidth without external loading from the taps is $\omega_{T,casc}$. Due to the decreased self-loading from the current-steering switches, the cascode summation structure significantly extends the number of ISI coefficients that can be supported by the DFE. While (3) contains an additional fixed self-loading term proportional to $k_{ISI,max}$, for a large number of coefficients, the self-loading is dominated by the term proportional to N_{coeff}.

With representative 60 GHz channel models [9] for typical TX-RX separations (3–5 m) and moderately directional RF frontends, k and $k_{ISI,max}$ are ~0.5 and ~2 respectively. Under these conditions, the cascode summer can support 3–5 times more taps than conventional summation at equal power and data-rate (Fig. 5). Importantly, as long as $k_{ISI,max}$ is substantially smaller than $k \cdot N_{coeff}$, the cascode summer power is only weakly sensitive to $k_{ISI,max}$ (as shown in Fig. 5). The structure therefore facilitates energy-efficient mixed-signal equalization of a 60 GHz channel. The prototype described in this paper implements 20 complex taps (20 direct and 20 cross-channel coefficients) on each (I and Q) channel with the maximum ISI per coefficient and total ISI magnitude being 0.5X and 2X the cursor respectively. Each summing amplifier (including the 40 DFE coefficients) consumes only 1.5 mW of power from a 1.2 V supply (to meet headroom constraints) while supporting 5 GS/s operation.

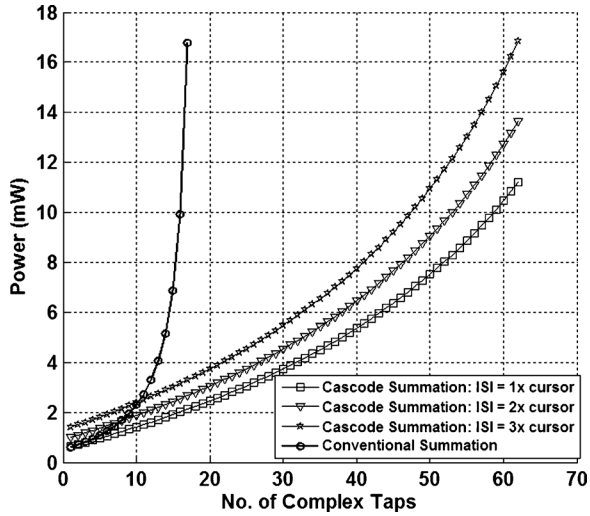

Fig. 5. Power versus number of complex taps for current-summing amplifiers: conventional and cascode summation.

B. Key Design Issues

While the cascode current summing structure can significantly extend the number of post-cursor ISI cancelation taps, several key circuit design issues must be addressed in order to implement data-rates of 5 GS/s with $\mathrm{BER} < 10^{-12}$. Fig. 6 shows the schematics of the 10 Gb/s 40-coefficient I/Q DFE prototype. In addition to the Data comparators, the DFE also includes Edge and Adaptive comparators for CDR and tap adaptation/carrier recovery respectively (further explained in Section III).

First-Tap Summation: Since the comparator must sample the input, resolve its value, and then subtract a signal proportional to that value from the input—all within in one symbol time (200 ps at 5 GS/s)—the first post-cursor tap of the DFE's feedback filter

$$P_{casc} \propto \frac{I_{nom,casc}}{1 - \frac{GBW_{casc}}{\omega_{T,cursor}} \cdot \gamma \cdot \left[1 + \frac{V_{in}}{V^*} \cdot \left\{2 \cdot k_{ISI,max} + k \cdot \beta \cdot N_{coeff} \cdot \left(2\gamma \cdot \frac{\omega_{casc}}{\omega_{T,casc}}\right)\right\}\right]} \tag{3}$$

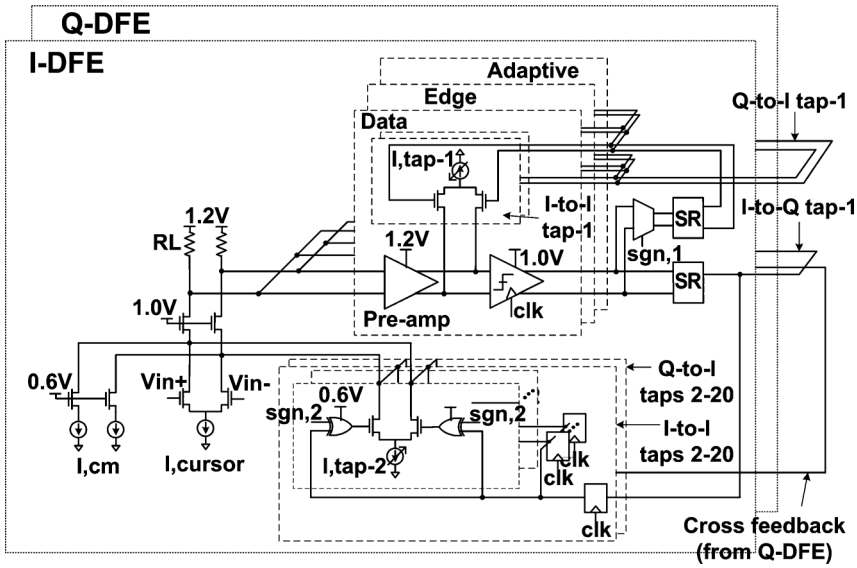

Fig. 6. Complex cascode current-summing DFE prototype with 40 coefficients.

is typically the most difficult to implement. For a cascode-summation DFE, if the first tap were to be subtracted at the cascode, the stringent timing constraint would force the summer bandwidth to be set very high. To efficiently relax this constraint and decouple it from the summer bandwidth, the first tap bypasses the summing amplifier altogether and is directly summed at the preamp output (similar to [24]). Since the preamp output self-loading is typically dominated by comparator offset cancelation current switches, the power overhead due to summing the first direct feedback and cross coefficients at the same node is small. The timing overhead of the first tap is further reduced by implementing the sign selection (XOR) in domino logic.

Tap-DAC Resolution and Low-Swing Drivers: Implementing as many as 20 complex (i.e., 40 coefficients per I/Q path) taps in the DFE can accrue sizeable quantization noise. To ensure that the quantization noise from summing 40 coefficients is below the thermal noise floor, each coefficient DAC requires 7 bits of resolution.[1] Due to matching requirements, such a high resolution necessitates a fairly large DAC size of $> 50\ \mu\text{m} \times 50\ \mu\text{m}$. To enable minimum loading on the high-speed timing paths, the DFE core must have a compact layout, and thus these large DACs (which are outside the high-speed feedback path) are physically located 100 s of μms of distance away from the DFE core (as shown in Fig. 15).

As a result of this physical separation and large device sizes, the tail-nodes of the tap switching pairs will be loaded by a large parasitic capacitance, creating a relatively low frequency pole (typically at a few hundred MHz). These slow-moving tail nodes are isolated from the amplifier output voltage variations by only the output impedance of the cascode transistor and the tap switches. The low intrinsic gain and output impedance of transistors in sub-micron technologies therefore requires that both the cascode and the tap switches be in saturation to ensure sufficient isolation. The resultant headroom constraints necessitate the use of low-swing drivers for the tap switches, as shown in Fig. 7. The driver inputs are full-swing (1 V) differential digital signals (din and $\overline{din}$) from the feedback shift registers, while the outputs are low-swing (0–0.6 V). The drivers implement XOR functionality for sign selection $(sgn, \overline{sgn})$, and additionally, ground the switch inputs to prevent unwanted coupling to the output when the coefficient is turned off (OFF = '1', $\overline{OFF}$ = '0').

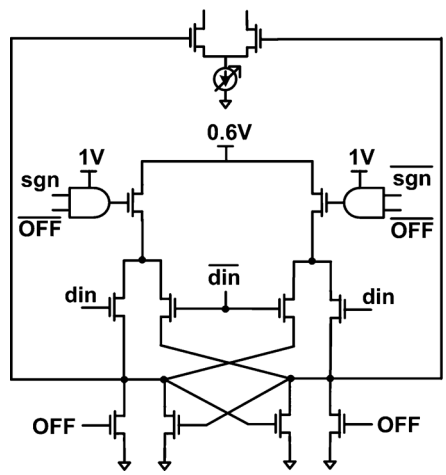

Fig. 7. Low-swing drivers for current steering switches, with embedded XOR and turn-off capability.

Infinite Impulse Response (IIR) Effects in DFE Currents: While the current-steering tap switches are driven differentially by the low-swing driver, imbalances are inevitably created whenever the gates of these switches are driven to steer current from one side to the other. As seen in Fig. 8, if the crossover point of the differential gate-drive signals is too high (low), the tail node glitches high (low). These glitches will eventually settle, but since the tail node is relatively slowly settling as compared to the symbol period (due to its large capacitance),

[1]This resolution requirement is computed with a signal amplitude of 120 mV (diff., p-p) at the comparator input and $\text{BER} < 10{-}12$, where the signal amplitude is set by a typical 60 GHz link budget for 3–5 m distances with a moderately directional RF front-end [31].

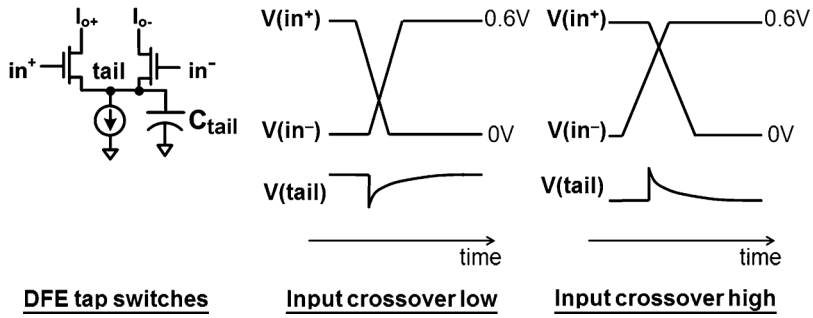

Fig. 8. Infinite impulse response (IIR) effects due to DFE tap switching.

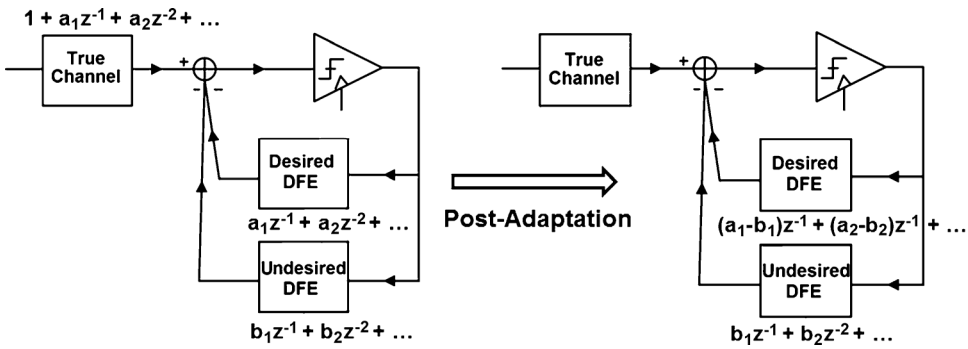

Fig. 9. Correction of DFE IIR effects by adaptation.

the glitch settles over multiple symbol periods as an infinite impulse response (IIR) filter.

The tail node glitches are roughly equal in magnitude about the equilibrium tail voltage, but their effect on the final DFE output are opposite in sign for the two directions of current steering. Since every data-bit change causes a glitch, the IIR phenomenon can be expressed as a convolution of the tap response (including the IIR effect) with $\varepsilon \cdot (1 - z^{-1})$ on the feedback path, where ε is the relative magnitude of the glitching error current with respect to the steady-state tap current. If the DFE taps were matched exactly to the ISI profile of the channel (referred to as the 'true channel' in Fig. 9), the IIR effects will cause a spurious component in the DFE feedback (referred to as 'undesired' DFE). Fortunately however, if the coefficients are adapted (e.g., with the adaptation algorithm explained in Section III) rather than hard-set, these undesired components can simply be corrected by appropriately adjusting the settings of the DFE itself.

These self-corrections in turn recursively create IIR effects which eventually decay below the LSB of the tap DACs. The IIR effects can therefore be mitigated by two methods: (1) Make the DFE longer (i.e., have more taps) than the actual channel delay spread, or (2) Prevent IIR effects in the final taps. This can be achieved by either (a) making the tail bandwidth high (which may be difficult as described earlier), or (b) intentionally making the tail bandwidth low by introducing additional capacitance so that the glitch results in a relatively static offset (relative to the longest run-length of '0' or '1' data-bits) that can be compensated by the offset-cancelation circuitry at the comparator input.

C. Simulation Results

Fig. 10 shows post-layout simulations of the DFE using a PRBS-7 input convolved with a representative 60 GHz channel. The output of the summing amplifier is free of all but the first tap of ISI, which is canceled separately at the input of the comparator. The comparator input eye highlights the difference in settling behavior of the first ISI tap cancelation current, which due to the delay of the comparators transitions later in the bit-time than the latter taps. The IIR effects of the tap currents are also apparent as a distinct drift in the voltage levels in the open part of the eye.

At 10 Gb/s, the prototype 40-coefficient complex cascode current-summing DFE has a total power consumption of 14 mW. From this total, 3 mW is consumed by the two summing amplifiers and taps, 4 mW by the six preamp/comparator pairs, while the other half (7 mW) is consumed by the feedback shift register chain of 80 flip-flops (40 each for I, Q DFEs). This power breakdown further highlights the power requirements of digital processing—even processing as simple as a delay line—at GS/s rates.

III. Adaptation Algorithms and Hardware

In order to track the variations in the 60 GHz wireless channel and any mismatch between the TX/RX, the RX baseband should be able to (a) adapt the equalizer coefficients to the channel, (b) adjust the phase and frequency of the baseband clock to sample the received data at the most suitable phase (i.e., CDR), and (c) correct for a phase/frequency mismatch between the TX and RX local oscillator (LO) signals (i.e., carrier recovery).

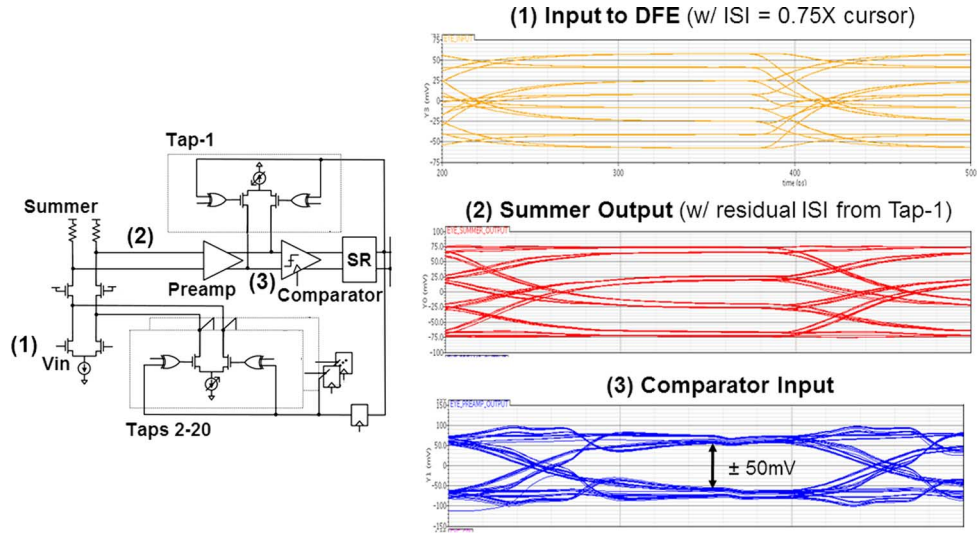

Fig. 10. Eye diagrams with 5 GS/s PRBS-7 input (post-layout simulation).

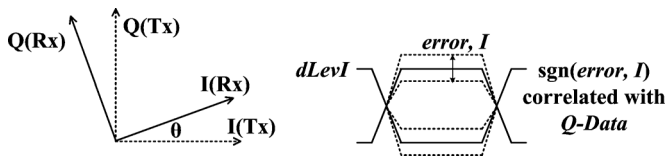

Fig. 11. Baseband constellation rotation: Errors on dLevI correlated with Q-Data.

In this prototype, equalizer coefficient adaptation is performed using sign-sign LMS by driving the correlation of errors about the data-level $(dLev)$ with previously received data-bits to zero [25]. $dLev$ is tracked by using an 'adaptive' sampler with a variable offset, clocked at the same phase as the data sampler. The logic implementing these tap and $dLev$ updates is estimated to consume 8 mW of power according to the digital synthesis report for the test-chip. CDR is performed by using an 'edge' sampler clocked at the opposite clock phase of the data/adaptive samplers in order to derive early/late information [26].

Given that they will be derived from physically independent frequency references, the TX and RX LO signals will initially be misaligned in both phase and frequency. Following the down-conversion mixer, this misalignment manifests as a rotation in the received signal constellation. As shown in Fig. 11, this effect is akin to crosstalk between the I and Q channels. This rotation can be compensated by using an analog phase rotator [2] on the baseband signal-path, as shown in Fig. 2.

With such a phase rotator in place to compensate for LO misalignment, the only remaining question is how to adaptively derive the control signals for this phase rotator. Constellation rotation causes errors about the mean $dLev$ on both the I and Q channels (termed $dLevI, dLevQ$ respectively). Therefore, in a manner essentially identical to equalizer coefficient adaptation, we propose to utilize a sign-sign LMS loop for carrier recovery by driving the correlation between the sign of the errors around $dLevQ$ $(dLevI)$ and the I-data (Q-data) to zero. Note that adaptive samplers to track $dLevI$ and $dLevQ$ would in any case be required for equalizer tap adaptation, and hence these samplers can be re-used with zero power or hardware overhead.

Specifically, a first-order update equation for the phase rotator angle φ_{rx} using the proposed sign-sign LMS for carrier phase recovery is

$$\begin{aligned}\varphi_{rx}[k+1] &= \varphi_{rx}[k] - \Delta\theta \cdot sign\left(eI[k]\right) \cdot dQ[k] \cdot I\left(dI[k]\right) \\ &\quad + \Delta\theta \cdot sign\left(eQ[k]\right) \cdot dI[k] \cdot I\left(dQ[k]\right) \\ I\left(d[k]\right) &= \begin{cases} 1, & d[k] == 1 \\ 0, & \text{otherwise} \end{cases}\end{aligned} \tag{4}$$

where suffixes I, Q denote the in-phase and quadrature-phase components respectively, the prefixes d and e denote the data-bit and error about $dLev$ respectively, and $\Delta\theta$ is the phase step size. Since LO phase misalignment fundamentally stems from frequency offsets between the TX and RX references, enhanced performance over the first-order loop in (4) can be obtained by estimating the frequency offset using an additional integral path in the LMS feedback loop. The corresponding second-order update equation utilized by the baseband described in this paper is

$$\begin{aligned}\varphi_{rx}[k+1] &= \varphi_{rx}[k] - \Delta\theta \cdot (updI[k] - updQ[k]) - \frac{2\pi}{\omega_s}\omega_{rx}[k] \\ \omega_{rx}[k+1] &= \Delta\omega \cdot \sum_{1}^{k} (updI[k] - updQ[k]) \\ updI[k] &= sign\left(eI[k]\right) \cdot dQ[k] \cdot I\left(dI[k]\right) \\ updQ[k] &= sign\left(eQ[k]\right) \cdot dI[k] \cdot I\left(dQ[k]\right)\end{aligned} \tag{5}$$

where ω_s is the angular sampling frequency of the loop and $\Delta\omega$ is the frequency step size. The logic implementing these carrier recovery updates in this baseband is estimated to consume 2 mW of power according to the digital synthesis report for the test-chip.

IV. Baseband Circuit Design

Beyond utilizing the previously described techniques for extended mixed-signal DFE design and carrier recovery, achieving a complete energy-efficient baseband required significant optimization of the circuit design and power consumption of the rest of the components as well. This section therefore describes

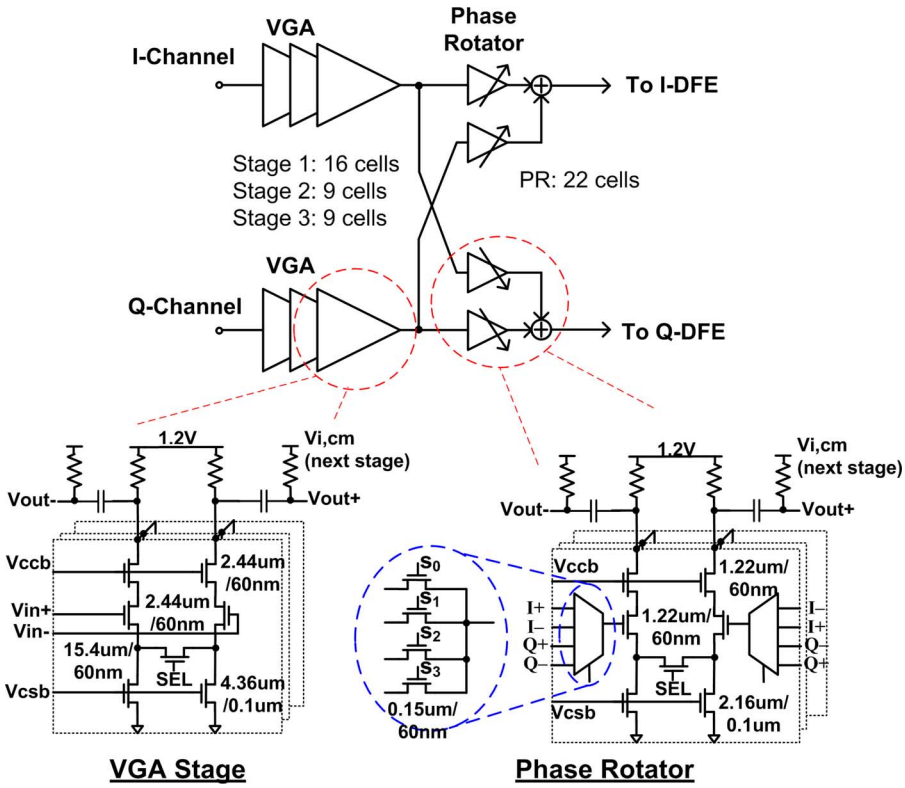

Fig. 12. (left) Variable gain amplifier (VGA) stage and (right) phase rotator (PR).

these optimizations to the variable gain amplifier, phase rotator, and clock/data-recovery circuitry.

A. Variable Gain Amplifier (VGA) & Phase Rotator (PR)

In order to meet the 60 GHz link budget for distances from $\sim$10 cm up to 5 m, the VGA-PR cascade was designed to provide 0–30 dB of voltage gain adjustment, with input referred noise $<$150 μV (rms) for the highest gain setting. Since the maximum data-rate is 5 GS/s, the bandwidth was initially targeted to be 2.5 GHz—i.e., the Nyquist frequency. This relatively high gain-bandwidth requirement necessitates the use of a multi-stage structure. To facilitate design optimization, each VGA stage was implemented as a simple common-source amplifier with resistive load. In order to achieve gain control, as shown in Fig. 12, each common-source gm-cell is partitioned into several unit cells, where a digitally-controlled shunting switch across the sources of the input devices turns each gm-cell on/off in differential-mode without affecting the common-mode bias point. Static voltage offset is rejected by using AC coupling capacitors between VGA stages.

The phase rotator (PR) rotates the signal constellation by summing the received I and Q baseband components weighted as per the required phase rotation [2]. A 4-to-1 analog multiplexer at the input of each PR unit cell implements I/Q signal and sign selection. As compared to the Gilbert-style selection in [2], this arrangement ensures that the PR DC-offset is independent of the rotation phase quadrant. As a balance between implementation complexity (and hence power) and phase quantization error, this design targets 6 bits (5.625°) of phase resolution. Since the PR is similar to a VGA stage, the VGA and PR were designed and optimized together as a multi-stage amplifier.

As a gain of $>$10 dB is difficult to obtain in a single stage while also meeting bandwidth constraints, the VGA-PR was implemented as a 4-stage amplifier, with the first 3 stages for signal amplification with variable gain, and the final stage for phase rotation with fixed gain. Leveraging the simplicity of the stages, a convex optimization framework [27] including technology and layout-dependent parameters was utilized to optimally allocate power consumption amongst the stages while ensuring that the complete design met its overall gain, bandwidth, and input-referred noise requirements. Since this optimization indicated that achieving the original target bandwidth of 2.5 GHz would require each stage to operate close to its intrinsic gain-bandwidth limits, the target bandwidth was reduced to 2.2 GHz in order to substantially reduce the VGA+PR power consumption. The marginal additional ISI produced by this reduced front-end bandwidth can be easily corrected by the DFE, and resulted in negligible decrease in signal energy even at 5 GS/s.

B. Clock and Data Recovery

The clock & data recovery (CDR) employs a dual-loop architecture with a second-order digital loop filter and a bang-bang phase detector [28]. Because a fully integrated transceiver would include a 60 GHz PLL, a divided version of the 60 GHz

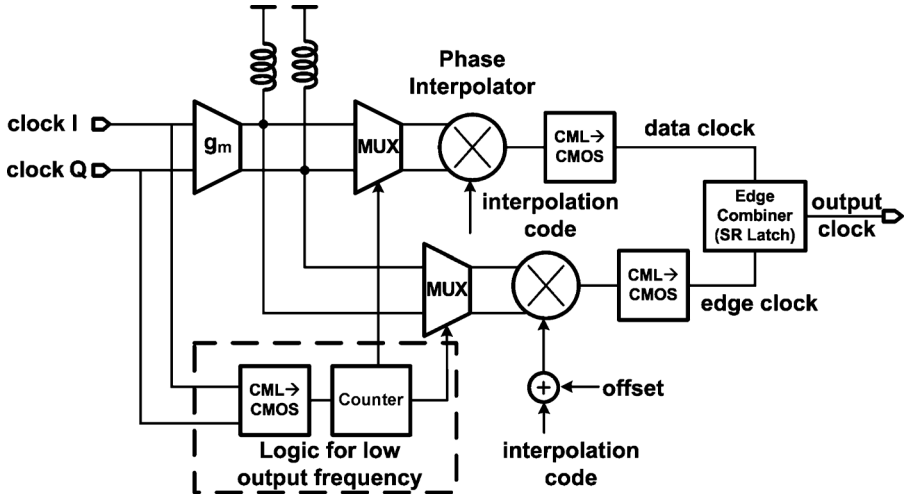

Fig. 13. Clock generation circuitry block diagram.

clock (obtained from the PLL divider chain) is used as a reference clock to eliminate the main PLL within the CDR, thus reducing design complexity and power consumption.

In utilizing this optimization, it is important to keep in mind however that one of the main purposes of the PLL in a dual-loop CDR architecture is to provide edge rate control for better phase interpolator linearity [28]. Therefore, as shown in Fig. 13, in this design a fixed frequency resonant buffer is used to shape the waveform at the input of the phase interpolator (PI) and to ensure PI linearity. Compared to an RC network whose 3 dB bandwidth is set to the clock frequency, even with a Q of only 1, an LC network resonating at the same frequency provides 3 dB more attenuation at the 3rd harmonic, which improves PI linearity by 0.5 dB. More importantly, since the inductor's value is determined by geometry and is hence largely insensitive to process variation, the resonance frequency is also less sensitive to process variation in comparison with its RC counterpart.

As the PI's inputs devices are kept small in order to minimize power consumption, the inductance required to resonate with the small input capacitance of the phase interpolator at 5 GHz is as high as 18 nH. To reduce area overhead, each inductor is implemented as a stacked multi-turn square utilizing metal 7 to metal 5 with 10 turns in each layer. The relaxed Q-factor requirement allows the metal traces within the inductors to be as narrow as 1 μm with 1 μm spacing. The resultant inductors each occupy only 30 μm $\times$ 30 μm.

Following the resonant buffer, two phase interpolators are employed to provide data and edge clock independently. Much like a fully balanced mixer, the phase interpolator is realized as two current-summed switching pairs controlled by two differential 6-bit current steered DACs, providing 7-bits of total phase control. The interpolated clock signals are then fed into CML-to-CMOS converters as well as edge combiners (similar to [29]) to ease the clock distribution for the comparators.

Although it is clear how the design described so far can robustly support a single baseband clock frequency by relying on LC edge-rate control, in general such a design would not support the multiple data-rates required for channel/throughput scalability and/or testing purposes. To overcome this drawback, this design incorporates a fractional divider into the PI (similar to [30]). The example shown in Fig. 14 demonstrates the generation of a 4 GHz clock from a 5 GHz reference. During the first period, the output clock is the interpolation of edge 1 of $clkI+$ and $clkQ+$; before the beginning of the next clock cycle, the coefficients for clock I and Q are swapped so that the output clock is an interpolation of edge 2 of $clkQ+$ and $clkI-$, thus generating an edge 250 ps away from the first one. In this design, the coefficient swapping is implemented with a double stack of switches in the phase interpolator (Fig. 14). In this manner, the proposed design can achieve a period resolution of 50 ps, thus creating output clock frequencies of 5 GHz, 4 GHz, 3.33 GHz, etc.

An interesting side effect of this fractional divider architecture is that the power consumption of the clock generation circuitry actually increases at lower output frequencies. Specifically, the resonant clock buffers and phase interpolators consume 2 mA from a 1 V supply while operating at 5 GHz, with an additional 1 mW consumed at lower output frequencies by the digital logic to generate phase-picking control signals. The CDR's second order digital loop filter operating at 500 MHz with a programmable bandwidth of 1 MHz to 10 MHz is estimated to consume 2.5 mW based on the synthesis report.

V. Measured Results

The baseband test-chip was fabricated in a standard 65 nm 1 V CMOS process. The die measures 1.7×1.0 mm^2 (Fig. 15) and was bonded in a chip-on-board configuration. The clock generation uses an external 10 GHz sinusoidal input, which in a fully integrated 60 GHz transceiver would be derived from the 60 GHz PLL divider chain. A 5 GS/s 2-channel Arbitrary Waveform Generator (AWG) was used to generate analog inputs to the test-chip. Using an AWG provides the flexibility to test the baseband operation for multiple 60 GHz channel conditions and TX/RX LO/clock mismatch.

As a first step, the PR was characterized (independent of the VGA) by feeding analog waveforms directly to the PR (by using multiplexer switches from the test-chip input pins). The PR constellation was measured by using a sinusoidal test-input to the

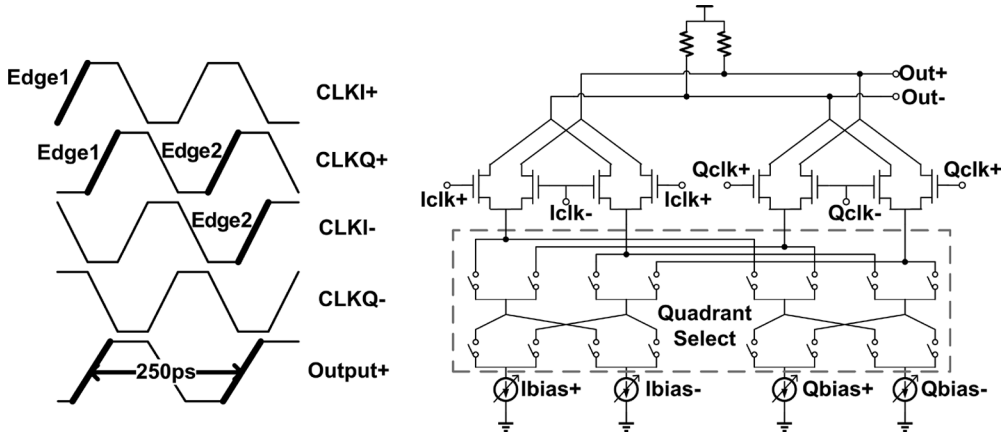

Fig. 14. Fractional divider: (left) operation principle, (right) phase interpolator implementation schematic.

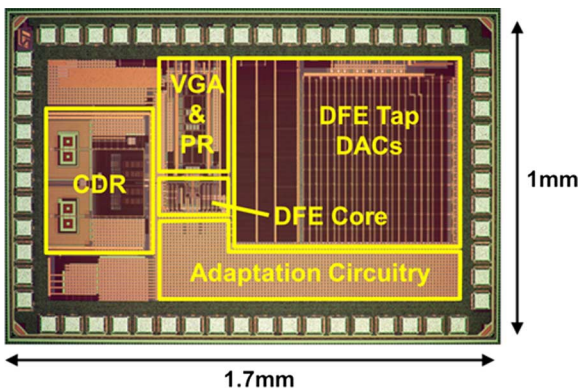

Fig. 15. Die micrograph.

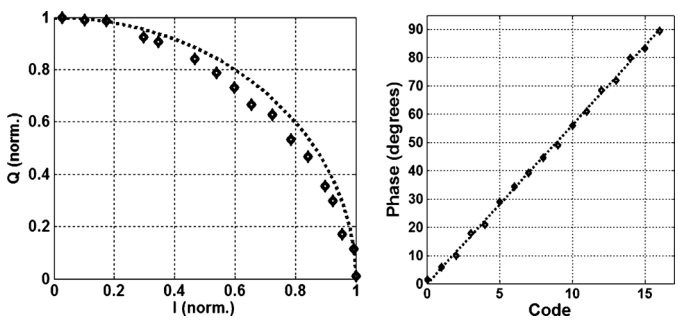

Fig. 16. Ideal (dotted line) and measured (diamonds) phase rotator characteristics: (left) Constellation, (right) Code versus Phase.

I-channel with no input to the Q-channel, thus rotating the signal into each quadrant. The resultant signal amplitude at the I/Q data samplers was measured by sweeping the offset voltage of the data comparator. The normalized signal constellation and rotation phase versus code is shown in Fig. 16. The PR has an average phase-step of 5.5° (designed phase step =5.625°), and a worst-case phase step of 8.05° (DNL = 0.43 LSB). The measured VGA-PR-DFE cascade bandwidth was 2.2 GHz, while the measured VGA+PR minimum to maximum gain ratio was 31 dB.

Next, the phase interpolator was characterized independently by driving its output off-chip through an integrated buffer.

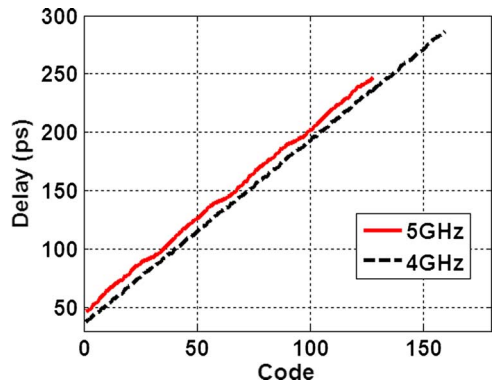

Fig. 17. Phase interpolator (PI) code versus measured delay for 5GHz and 4GHz clock outputs (spanning a delay of 200ps and 250ps respectively).

Fig. 17 shows the measured transfer curve of the phase interpolator delay versus digital code for both 5 GHz and (divided) 4 GHz clock outputs, with a delay span of 200 ps and 250 ps respectively. As seen in Fig. 18, the maximum phase step is <3 ps and <2.5 ps at 5 GHz and 4 GHz respectively.

In order to test the entire receiver, the AWG was programmed to mimic a line-of-sight (LOS) 60 GHz multi-path channel (similar to [23]) with ISI and signal constellation rotation due to carrier phase/frequency offset while generating 2^7-1 and 2^9-1 PRBS data on I and Q channels (Fig. 19). To match the link budget of a typical 60 GHz channel [31], the AWG amplitude and VGA gain were adjusted to receive a 120 mV (diff, p-p) signal at the sampler. For up to ± 50 ppm of carrier frequency offset, ± 350 ppm of baseband CLK frequency offset, and channel-induced ISI of up to 2.5X the cursor (with the first coefficient handling 0.5X and the main DFE 2X) with all three on-chip adaptive loops—carrier recovery (CR), CDR, and equalizer taps—operating, the test-chip was able to correct for all of these impairments and receive 10 Gb/s QPSK data with BER $< 10^{-12}$ (measured with an on-chip BERT). The recovered baseband clock jitter was measured to be <4 ps rms across the entire frequency locking range (Fig. 20). Post-convergence, the steady-state behavior of all loops was measured as a histogram by scanning out the on-chip adapted register values. The register readouts correspond to

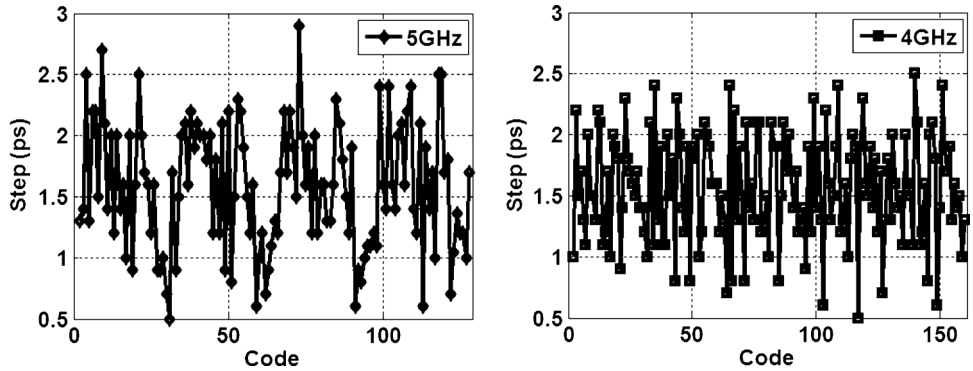

Fig. 18. Phase interpolator (PI) code versus measured delay-step for 5 GHz and 4 GHz clock outputs.

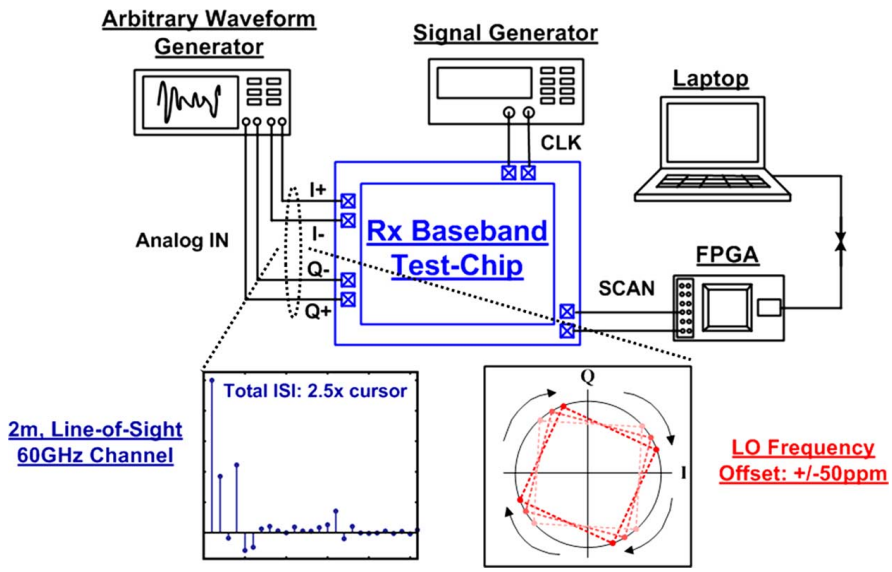

Fig. 19. Test setup.

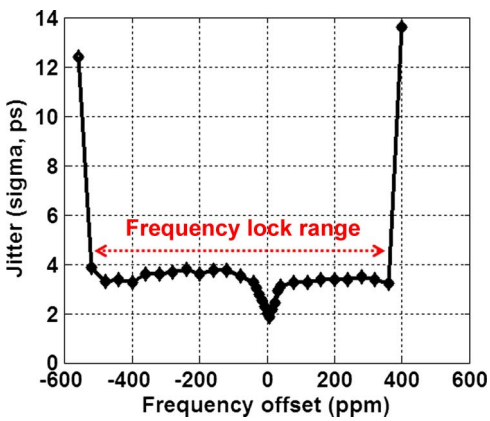

Fig. 20. Recovered clock jitter (σ, ps) versus frequency offset (ppm).

TABLE I
POWER BREAKDOWN

Block	Power
Variable Gain Amplifier (VGA)	16mW
Phase Rotator (PR)	8mW
Carrier Recovery (CR)	2mW
Decision Feedback Equalizer (DFE)	14mW
Equalizer Adaptation	8mW
Clock & Data Recovery (CDR)	5mW
Total	**53mW**

the channel non-idealities programmed into the AWG that are overlaid with the histograms shown in Fig. 21.

In order to estimate the timing margin on the received signal, the baseband clock phase was manually swept (while freezing the states of all other adapted values), and the variation of BER with phase (i.e., bathtub curve) was measured and is shown in Fig. 22. The baseband achieves a margin of 0.2 UI for BER of $< 10^{-12}$. Note that since the equalizer coefficients are not updated as the sampling phase is swept, the residual ISI increases once the sampling phase is moved away from its original position, and thus the shape of the bathtub curve is dominated by this effect (rather than by the recovered clock jitter). The on-chip adaptation rate (500 MS/s) was significantly faster than the rate at which the adapted vales could be read out externally using a scan chain (~24 MHz). In order to illustrate the dynamics of on-chip adaptation with sufficient time granularity, as an additional experiment, all of the adaptive loops with the exception

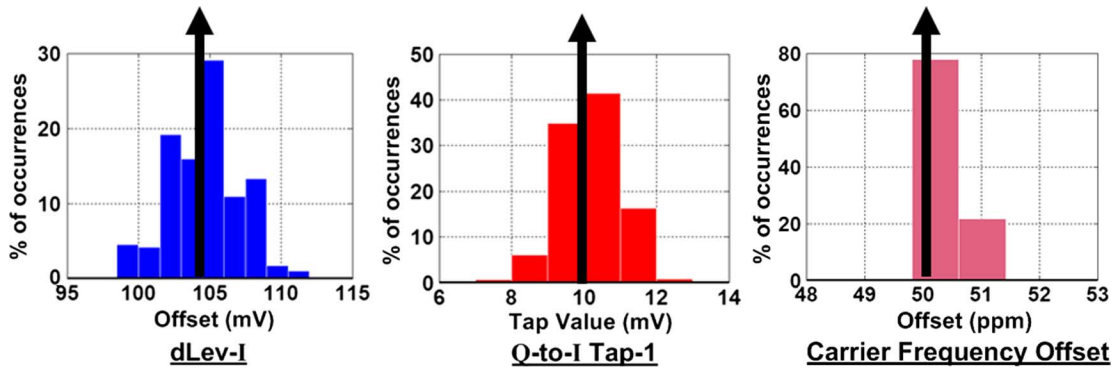

Fig. 21. On-chip adaptation results – expected (arrows) and measured (histograms).

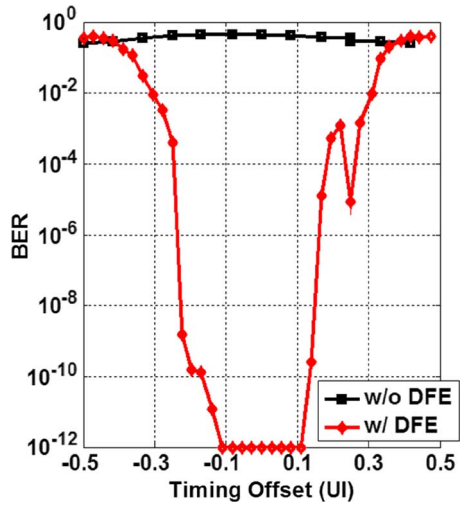

Fig. 22. Bathtub curve, measured before and after equalization.

of carrier and baseband frequency tracking were separately implemented on an FPGA that interacted with the baseband chip through the scan chain. Fig. 23 shows the simultaneous convergence (within $\sim 10^4$ symbols) of the multiple adaptive loops on the FPGA.

Table I shows the power breakdown of the baseband. The entire baseband (including 31 dB front-end gain) consumes only 45 mW at 10 Gb/s post-adaptation (with CR/CDR still running to track frequency offsets). Of this total, the core signal processing blocks—DFE, CDR, CR—consume only 29 mW. In comparison to previously presented mixed-signal designs without adaptation [21], [22] this work achieves 8–13X improved power efficiency at 4–10X higher data-rate (Table II).

VI. Conclusion

This paper demonstrates that high-speed wireline chip-to-chip circuit design-inspired techniques can offer energy-efficient baseband solutions for multi-Gb/s wireless communications in the 60 GHz band. As opposed to conventional wireless basebands relying on high dynamic range digital signal processing, the proposed design leverages relatively low dynamic range (implying simple modulation schemes) analog signal processing. By taking this approach, a prototype mixed-signal 60 GHz baseband in 65 nm CMOS demonstrates operation at up to 10 Gb/s using QPSK modulation in under 53 mW of total power.

In order to support the relatively long delay spreads of 60 GHz channels while retaining the power advantages of analog summation, a cascode summation DFE that supports 3–5X more coefficients at the same data-rate and power consumption as conventional current-steering designs is introduced. The prototype design includes a 40-coefficient I/Q cascode-summation DFE which consumes only 14 mW at 10 Gb/s. In addition to including known approaches for equalizer coefficient adaptation and CDR, this baseband demonstrates a proposed sign-sign LMS algorithm for carrier recovery that requires minimal hardware overhead due to its re-use of the high-speed samplers required for equalizer adaptation in any case. Finally, circuit-level optimizations of the VGA, analog phase rotator, and clock generation/recovery circuitry enable a total front-end gain range of 31 dB, bandwidth of 2.2 GHz, and power consumption of 24 mW (I/Q VGAs+PR)/4.5 mW (clock gen.+CDR).

For up to ~50 ppm of carrier frequency offset, ~350 ppm of baseband CLK frequency offset, and ISI in the channel up to 2.5X the cursor, all of the adaptive loops—equalizer adaptation, CDR, and carrier recovery—lock appropriately, and the baseband is demonstrated to receive data up to 10 Gb/s with a BER $< 10^{-12}$. The entire baseband consumes 53 mW of power (45 mW after DFE adaptation is completed), of which the core signal processing consumes only 29 mW. At this level of power consumption and demonstrated scalability to higher throughputs than existing 60 GHz standards [9], such a mixed-signal baseband appears to be an attractive enabler for embedding mm-wave transceivers into mobile devices.

Appendix I
Power versus Number of Taps for Conventional Current-Steering DFEs

Fig. 24 shows a conventional mixed-signal DFE summing amplifier structure along with its small-signal model. To simplify the analysis, transistor output resistances are ignored (i.e., assumed to be infinitely large). Throughout this analysis, we will assume that the input cursor amplitude (excluding the ISI) is V_{in}, that the summing amplifier has a DC gain of G_{dfe}, and that the DFE operates at a data-rate of f_s symbols/sec.

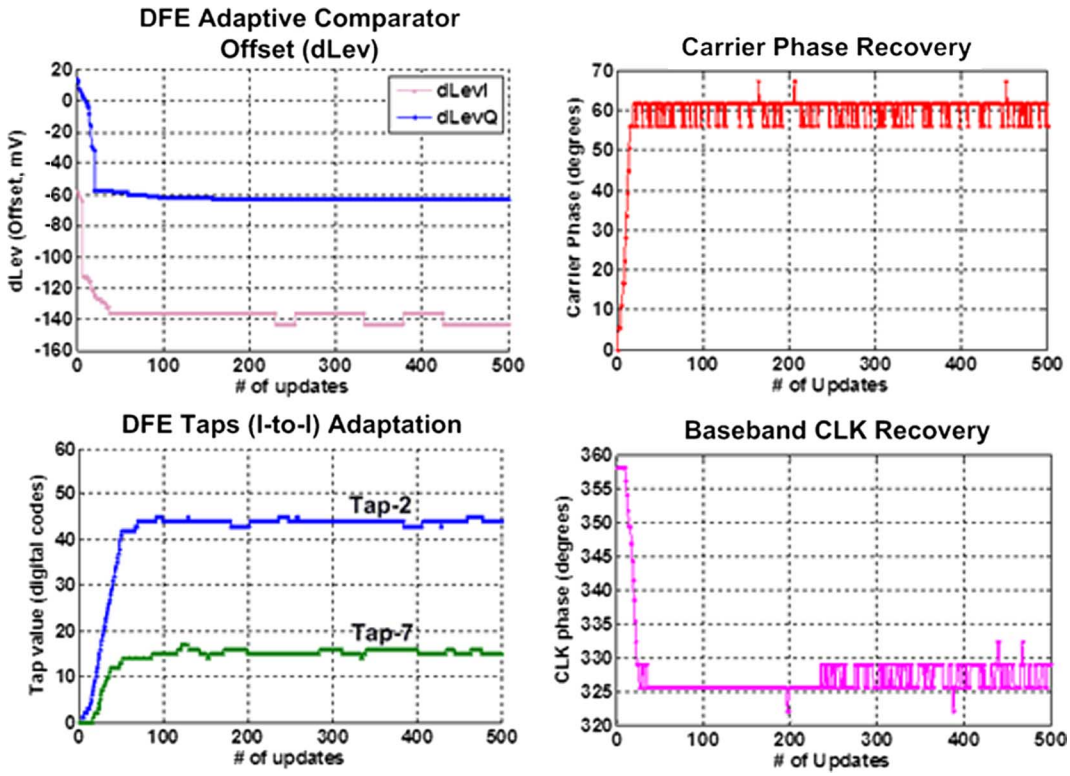

Fig. 23. Adaptation dynamics – measured using on-FPGA adaptation.

TABLE II
COMPARISON WITH MIXED-SIGNAL 60 GHz BASEBAND PRIOR ART

		[21]	[22]	This Work
Technology		90nm CMOS	90nm CMOS	**65nm CMOS**
VGA-PR	Gain	–	42dB	32dB
	Bandwidth	–	1.4GHz	2.2GHz
No. of DFE Coefficients		16	–	**80**
Adaptation		–	CDR (CR not required)	**CDR, CR, Equalizer**
Total Baseband Power		55mW	85mW	**45mW**
Minimum BER		$< 10^{-3}$ (simulated)	10^{-9}	**$< 10^{-12}$**
Data-Rate		1Gb/s	2.4Gb/s	**10Gb/s**
Power Efficiency		55pJ/bit	35.4pJ/bit	**4.5pJ/bit**

First, defining the V^* of a transistor as $V^* \equiv 2I_D/g_m$ and realizing that half of the tail current flows through each input device in a differential pair:

$$g_{m,cursor} = I_{cursor}/V^* \tag{6}$$

where I_{cursor} is the DC bias current of the input pair. The DC gain of the DFE is therefore given by

$$G_{dfe} = \frac{I_{cursor}}{V^*} \cdot R_L \tag{7}$$

A full-rate DFE has a time period of $1/f_s$ to settle each new summation value. This timing constraint can be partitioned into $(1-\alpha)/f_s$ for the flip-flop and XOR sign-selection delays (both digital), and α/f_s for the analog settling of the coefficient currents at the summation node. Thus, in order to ensure n_τ time constants of settling (with n_τ chosen to achieve a sufficiently accurately settled signal—e.g., 3 for 95% settling):

$$n_\tau \cdot \tau = \alpha/f_s \tag{8}$$

where τ is the time-constant of summation node. This time constant is given by the RC product:

$$\tau = R_L \cdot (C_L + C_{cursor} + N_{coeff} \cdot C_{coeff}) \tag{9}$$

where R_L is the load resistance, C_{cursor} and C_{coeff} are the drain capacitances of the input transistor and current steering tap switch respectively, C_L is the loading from the next stage

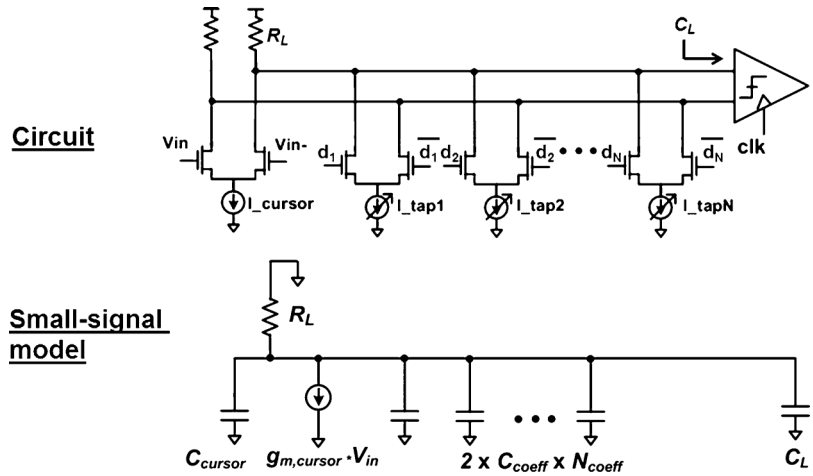

Fig. 24. Conventional DFE analysis.

(typically the comparator with a preamp to mitigate kickback). The DFE has N_{coeff} coefficients, each of which can cancel ISI up to a maximum amplitude of k times the cursor. Therefore, the maximum current required by each coefficient (I_{coeff}), is

$$I_{coeff} = k \cdot g_{m,cursor} \cdot V_{in} = k \cdot \frac{V_{in}}{V^*} \cdot I_{cursor} \tag{10}$$

As we will see shortly, one can combine (6) through (10) and predict the power consumed by the DFE simply by defining two more device/technology-dependent parameters. Of the three capacitors at the summation node, C_{cursor} and C_{tap} are attributed to the internal self-loading of the structure, and are therefore proportional to I_{cursor}. The internal capacitors can be expressed in terms of ω_T and γ (the gate-to-drain capacitance ratio):

$$C_{cursor} = \frac{\gamma}{\omega_{T,cursor}} \cdot \frac{I_{cursor}}{V^*} \tag{11}$$

$$N_{coeff} \cdot C_{coeff} = \frac{\gamma}{T,coeff} \cdot \frac{I_{cursor}}{V^*} \cdot \left(2k \cdot \frac{V_{in}}{V^*_{coeff}} \cdot N_{coeff} \right) \tag{12}$$

Using these parameters and combining (6)–(10) gives expression (13) (shown at the bottom of the page) for the cursor current (assuming $V^*_{coeff} = V^*$). In (13), $(n_\tau f_s/\alpha)$ is the bandwidth of the amplifier summing node. The product, $(n_\tau f_s/\alpha) \cdot G_{dfe}$, is therefore the amplifier gain-bandwidth (GBW). Furthermore, since $I_{coeff} \propto I_{cursor}$, the total power consumption of the conventional DFE summing amplifier, $P_{conv} \propto I_{cursor}$. By defining $\beta = 2\omega_{T,cursor}/\omega_{T,coeff}$, P_{conv} can be expressed as

$$P_{conv} \propto \frac{I_{nom}}{1 - \frac{GBW}{\omega_{T,cursor}} \cdot \gamma \cdot \left(1 + k \cdot \frac{V_{in}}{V^*} \cdot \beta \cdot N_{coeff}\right)} \tag{14}$$

where $I_{nom} = C_L \cdot GBW \cdot V^*$ is the nominal current of a class-A amplifier without self-loading.

Appendix II
Power versus Number of Taps for Cascode Summing DFE

Fig. 25 shows the small-signal model of the cascode current-summing structure in Fig. 4. The symbols used in the analysis, unless otherwise listed, have the same connotation as that for the conventional summing structure in Appendix I. The common-mode current added to each half of the differential circuit is I_{bleed}. The cascode transconductance $(g_{m,casc})$ is, therefore,

$$g_{m,casc} = \frac{2 \cdot \left(\frac{I_{cursor}}{2} + I_{bleed}\right)}{V^*_{casc}} \tag{15}$$

The cascode-based structure has two poles—one at the cascode source where all taps are summed (ω_{casc}), and another at the output node (ω_{out}). It is desirable to place both the poles at approximately the same frequency, since making one pole larger than the other has diminishing returns for the effective bandwidth of the summing stage in terms of power dissipation. To get an identical effective bandwidth as that of the conventional summing structure, both the poles should be at $\sim \sqrt{2}$ times higher frequency. Therefore, the analog settling constraint for the cascode summation DFE is

$$\sqrt{2} \cdot n_\tau \cdot \tau = \alpha \cdot (1/f_s) \tag{16}$$

$$I_{cursor} = \frac{C_L \cdot \left(\frac{n_\tau f_s}{\alpha}\right) \cdot G_{dfe} \cdot V^*}{1 - \left(\frac{n_\tau f_s}{\alpha}\right) \cdot G_{dfe} \cdot \frac{\gamma}{\omega_{T,cursor}} \cdot \left(1 + k \cdot \frac{V_{in}}{V^*} \cdot \frac{2\omega_{T,cursor}}{\omega_{T,coeff}} \cdot N_{coeff}\right)} \tag{13}$$

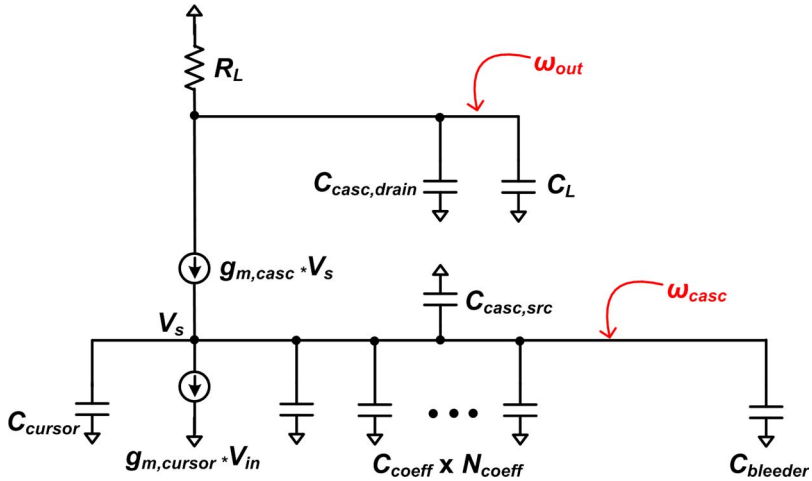

Fig. 25. Small-signal model of the cascode-summation (circuit schematic shown in Fig. 4).

The cascode and output poles are expressed in terms of their RC time-constants (τ_{casc} and τ_{out} respectively) as

$$\tau_{casc} = \frac{1}{g_{m,casc}} \cdot (C_{casc,src} + C_{bleed} + C_{cursor} + N_{coeff} \cdot C_{coeff}) \quad (17)$$

$$\tau_{out} = R_L \cdot (C_L + C_{casc,drain}) \quad (18)$$

where $C_{casc,src}, C_{casc,drain}$ are the cascode source and drain capacitances respectively, while C_{bleed} is the bleeder transistor drain capacitance. Furthermore, if the maximum possible total ISI amplitude is $k_{ISI,max}$ with respect to the cursor, the total maximum total ISI cancelation current ($I_{coeff,total}$) is

$$I_{coeff,total} = k_{ISI,max} \cdot \frac{I_{cursor}}{V^*} \cdot V_{in} \quad (19)$$

The intrinsic capacitors of the summing structure are again expressed in terms of ω_T and γ:

$$C_{bleed} = \frac{\gamma}{\omega_{T,bleed}} \cdot \frac{2I_{bleed}}{V^*_{bleed}} \quad (20)$$

$$C_{casc,src} = \frac{2}{\omega_{T,bleed} \cdot V^*_{casc}} \cdot \left(\frac{I_{cursor}}{2} + I_{bleed} \right) \quad (21)$$

$$C_{casc,drain} = \frac{2 \cdot \gamma}{\omega_{T,bleed} \cdot V^*_{casc}} \cdot \left(\frac{I_{cursor}}{2} + I_{bleed} \right) \quad (22)$$

Using these parameters and combining (15)–(19) results in (23) (shown at the bottom of the page), in which $BW = (\sqrt{2} n_\tau f_s / \alpha)$ is the bandwidth of both the cascode and output nodes. The product, $(\sqrt{2} n_\tau f_s / \alpha) \cdot G_{dfe}$, is referred to as the cascode gain-bandwidth (GBW_{casc}), even though strictly speaking, the effective amplifier bandwidth is $(n_\tau f_s / \alpha)$. Since both coefficient and bleeder currents scale with cursor current (i.e., $I_{coeff} \propto I_{cursor}$, $I_{bleed} \propto I_{cursor}$), the total power consumption of the cascode-summation DFE amplifier, $P_{casc} \propto I_{cursor}$. By again defining $\beta = 2\omega_{T,cursor} / \omega_{T,coeff}$, P_{casc} can be expressed as in (24), shown below, where $I_{nom,casc} = C_L \cdot GBW_{casc} \cdot V^*$.

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$$I_{cursor} \cong \frac{C_L \cdot BW \cdot G_{dfe} \cdot V^*}{1 - BW \cdot G_{dfe} V^* \frac{C_{d,Icursor}}{2} \cdot \left[1 + \frac{V_{in}}{V^*} \left\{ 2k_{ISI,max} + k \frac{2\omega_{T,curosr}}{\omega_{T,coeff}} N_{coeff} \cdot 2\gamma \cdot \frac{\omega_{casc}}{\omega_{T,casc}} \right\} \right]} \quad (23)$$

$$P_{casc} \propto \frac{I_{nom,casc}}{1 - \frac{GBW_{casc}}{\omega_{T,cursor}} \cdot \gamma \cdot \left[1 + \frac{V_{in}}{V^*} \cdot \left\{ 2 \cdot k_{ISI,max} + k \cdot \beta \cdot N_{coeff} \cdot \left(2\gamma \cdot \frac{\omega_{casc}}{\omega_{T,casc}} \right) \right\} \right]} \quad (24)$$

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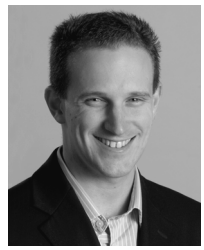

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J. Muller, B. Stefanelli, A. Frappé, L. Ye, A. Cathelin, A. Niknejad, A. Kaiser, “A 7-bit 18th order 9.6 GS/s FIR up-sampling filter for High Data Rate 60-GHz Wireless Transmitters”, IEEE Journal of Solid-State Circuits, vol.47, no. 7, pp. 1743-1756, Jul 2012

A 7-Bit 18th Order 9.6 GS/s FIR Up-Sampling Filter for High Data Rate 60-GHz Wireless Transmitters

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***Abstract*—This paper presents the design and measurement of a 4× oversampled 18th order digital low-pass FIR filter. It is a key building block in the proposed digitally enhanced transmitter architecture for 60 GHz wireless high-data rate links. Spectrum mask requirements are fully satisfied for OFDM modulated signals without requiring additional analog filtering. Pipelined CPL adders and TSPC flip-flops are used to enable a very high operation frequency. The core area is 0.1 mm^2 in a standard GP 65 nm CMOS process. Measured power consumption is 400 mW at 9.6 GS/s with a 1.4 V power supply voltage.**

***Index Terms*—Digital FIR Filter, millimeter waves, transmitter, CMOS.**

I. Introduction and Motivations

HIGH data-rate short-range wireless links are emerging as a replacement of existing cable connections such as HDMI video cables for example. To increase the data rate more bandwidth and more complex modulations are required. One possible solution is the UWB (ultra wide band) technology in the 3–10 GHz band, but it has been plagued by interference issues and lack of world-wide standardization. In 2001 the FCC (federal communications commission) released the 57–66 GHz band, introducing 9 GHz of unlicensed bandwidth and triggering a large effort to build low-cost radios suitable for consumer applications in this band. A standard has been defined (IEEE 802.15.3c) and several consortiums such as WiHDMI and WiGig are working towards supporting both OFDM and single carrier approaches [1]–[3].

Nanometer CMOS (and to a certain extent BiCMOS) processes opened the way to building 60 GHz radios in integrated silicon technologies [4]–[10] with commercial exploitation coming within reach. As an example, the authors in [11] have developed a complete 60 GHz band transceiver in 65 nm CMOS. The transmitter is composed of the analog baseband filters, the mixers and the quadrature LO generation and a PA. The proposed transceiver is fully compliant with the WiGig standard. It can perform both OFDM and single carrier modulations. The module occupies an area of 13.5×8.5 mm^2. It consumes 1.357 W in the transmit mode (357 mW for the transmitter and 1 W for the PA).

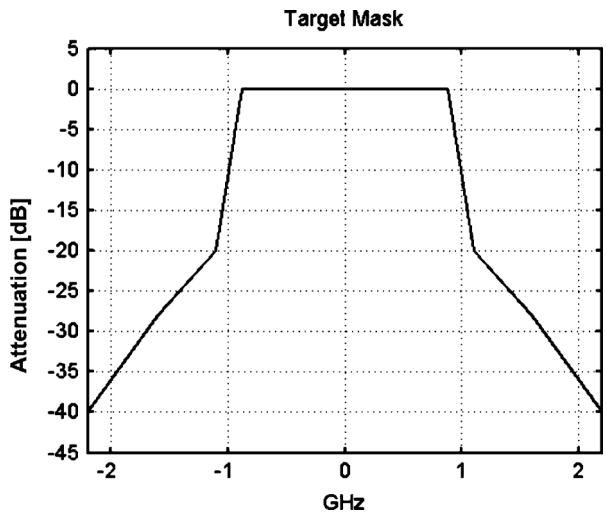

Fig. 1. IEEE 802.15.3.c channel spectrum mask.

Advances in CMOS technology primarily target performance increase of digital circuits in terms of speed, power consumption and area. Digital processing has therefore been largely introduced in RF transceivers for the low GHz frequency range. Approaches include all digital frequency synthesis combined with digital PA in a polar architecture [12], digital RF sigma-delta modulators [13] and direct digital-to-RF conversion [14], [15]. In the latter approach the digital baseband signal is first oversampled and then in one step converted to the analog domain and transposed to the RF carrier with a DRFC (Digital-to-RF converter). Image filtering is accomplished partly in the digital domain prior to conversion and partly at the RF output. The analog baseband filter disappears in this architecture. However, signal bandwidth in cellular or connectivity applications is 10 MHz or less. Transposing these techniques to the 60 GHz band is hindered by the large bandwidth, i.e., up to 1.7 GHz for one channel.

However, some digital capabilities have been introduced in 60 GHz transmitters with the works of [16]. The digital data is directly transposed to the 60 GHz carrier with a DRFC. Due to the direct QPSK modulation of the RF carrier, the signal occupies a bandwidth larger than prescribed by the standards. The transmit part consumes, with a 1.2 V supply, 170 mW while transmitting at a power level of 10 dBm. A data rate of 4 Gb/s has been achieved with a QPSK modulation over 1 m distance with less than 10^{-11} bit error rate (BER). In [17] a digital oversampled pulse-shaping filter for SC-QPSK combined with a 3.4 GS/s DAC is described. An alternative approach to filtering and

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Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (MHz)	Roll-Off Factor
A1	57.240	58.320	59.400	1728	0.25
A2	59.400	60.480	61.560	1728	0.25
A3	61.560	62.640	63.720	1728	0.25
A4	63.720	64.800	65.880	1728	0.25

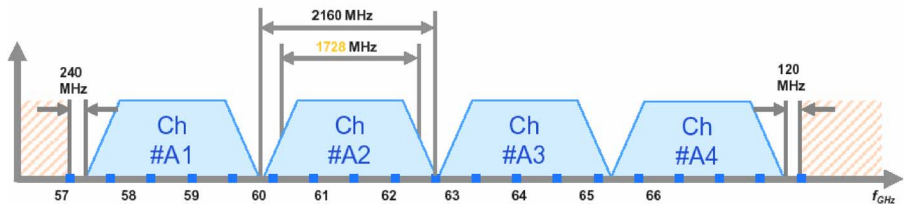

Fig. 2. 60 GHz radio channel map.

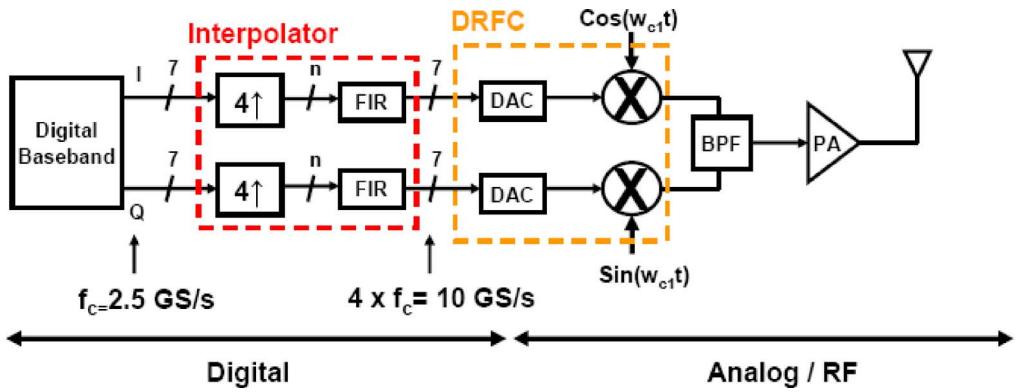

Fig. 3. Proposed digital transmitter architecture.

data conversion described in [18] introduces a semi-digital oversampling filter combining filter and DAC in a BiCMOS technology also targeted at single-carrier 60 GHz wireless communication systems.

The aim of this work is to transpose the DRFC concept to millimeter wave applications employing OFDM modulation with full compliance to the spectrum mask requirements imposed by the standards [19]. The proposed architecture is presented in the next section. The design of the interpolator filter at system level is described in Section III, while Sections IV and V describe the circuit and layout level implementation. Section VI presents the test methodology and chip assembly. Finally measurements are presented in Section VII.

II. Proposed 60 GHz Transmitter With Digital Capabilities

The circuit described in this paper is one of the first attempts to introduce digital processing beyond the baseband in wideband 60 GHz transmitters. The target is to propose an alternative to analog reconstruction filters by introducing digital oversampling filters combined with high speed DA converters. In a classical transmitter, the digital baseband signal is converted to the analog domain by a Nyquist rate DA converter followed by an analog filter to suppress spectral images. Such analog filters need to have a cut-off frequency of around 880 MHz (1.7 GHz useful channel bandwidth) and should be of order 4 or 5 to meet the spectrum mask requirements. Analog passive implementations with inductors and capacitors require very large silicon area and provide low quality factors. Appropriate active analog filters have also been shown recently in the context of a receiver [20]. Oversampling and filtering in the digital domain in combination with direct digital-to-RF conversion can push the analog filtering to higher frequencies and relax at the same time filtering requirements. Passive band-pass filters with smaller area can then achieve the required specifications. Furthermore, digital circuits can be made programmable offering increased flexibility.

The standard proposes to use either single carrier modulation or OFDM modulation. We focus our study on OFDM modulation. 4 channels of 1728 MHz bandwidth spaced by 2.16 GHz are available in the 57–65 GHz band. The OFDM signal contains 336 subcarriers of 5 MHz each and is sampled at the I and Q outputs of the digital signal processor at 2.5 GS/s. The spectrum mask requirements are shown in Fig. 1 and the radio channel map in Fig. 2.

Fig. 3 shows the proposed 60 GHz transmitter architecture. The D-to-A conversion is merged with the mixer into a so-called DRFC (digital-to-RF converter) as described in [16]. To avoid analog base-band filters, the digital data stream is oversampled prior to D-to-A conversion. In the oversampling process, images of the baseband spectrum appear at multiples of the initial sampling frequency and have to be filtered. To meet the spectrum mask requirements, a digital interpolation filter is needed. The design and implementation of this filter is reported in this paper. For the standard targeted here, signal-to-noise ratio and spectrum-mask specifications require 7 bit resolution.

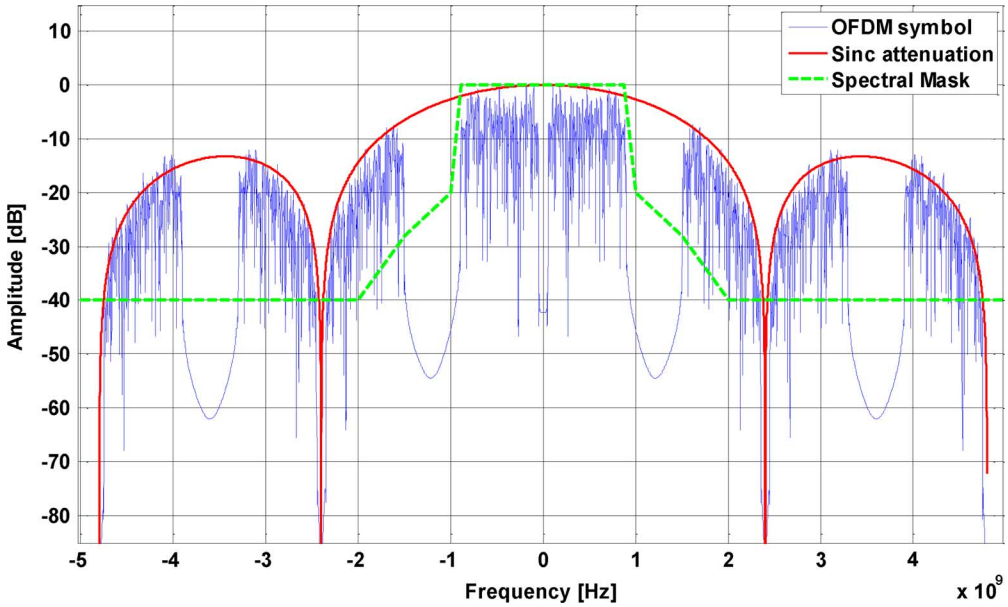

Fig. 4. OFDM signal up-sampled to 10 GS/s, attenuation of the images with the sinc function, and spectral mask.

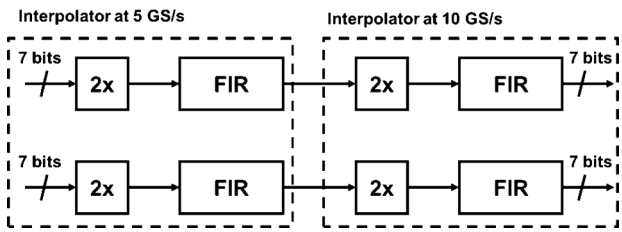

Fig. 5. Partitioned interpolator structure.

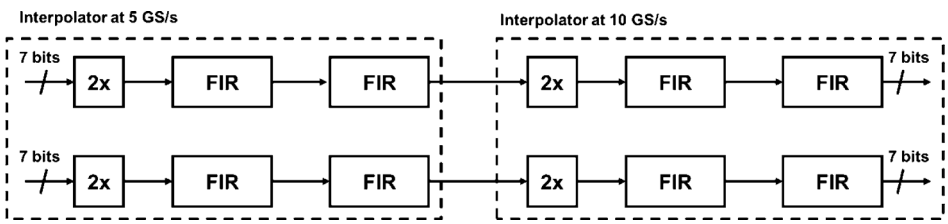

Fig. 6. Cascaded and partitioned interpolator.

After filtering and conversion to the analog domain, the first residual image appears at an offset equal to the sampling frequency. The worst case situation is when channels A1 (or A4) are used. To avoid that images appear in the channel on the other end of the RF band, the oversampling frequency must be greater than the standard's bandwidth, i.e., 8.64 GHz. At the same time, the oversampling frequency should be an integer multiple of the baseband sampling frequency. The closest frequency satisfying both criteria is 10 GHz, corresponding to a 4x oversampling of the base-band data. Thanks to the sample-and-hold function inherent to the D-to-A conversion, the first residual image is attenuated by 20 dB. Therefore it can be eliminated by the RF band filters present in the systems. Pushing the oversampling frequency to higher frequencies would relax the RF filtering requirements, but is not feasible with current CMOS technologies.

The spectrum of the QPSK-OFDM modulated digital signal after up-sampling to 10 GS/s is depicted in Fig. 4. Each sample is repeated 4 times. This introduces a sinc function that provides some attenuation of the images. Further attenuation by about 30dB is necessary in order to respect the spectrum mask.

III. Interpolator Design

This section focuses on the interpolator design from a system perspective. Basically an interpolator is the combination of an up-sampler and a digital filter to remove the images created by the up-sampling process. Due to the very high frequency operation, digital IIR filters containing feedback loops are not practical. A FIR filter is therefore used. Based on the filter specifications, it has been determined that a 22 coefficient filter is able to fulfill the requirements with acceptable attenuation at pass-band edges. However, even with a state of the art technology, the implementation of multipliers at 10 GS/s is not practical. Therefore, a modified filter architecture using only power-of-two coefficients has been implemented. Indeed, power-of-two coeffi-

TABLE I
QUANTIZED INTERPOLATOR COEFFICIENTS

	Number of coefficients	Coefficients	Adders
5GS/s FIR (2X)	6	$[-2^{-4}2^{-4}2^{-1}2^{-1}2^{-4}-2^{-4}]$	5
10GS/s FIR (2X)	3	$[2^{-2}2^{-1}2^{-2}]$	2

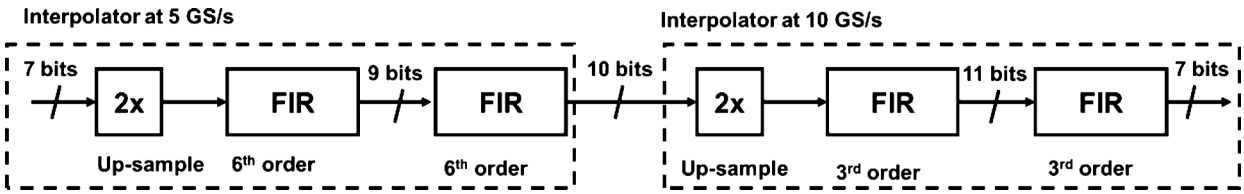

Fig. 7. Final internal architecture of the interpolator.

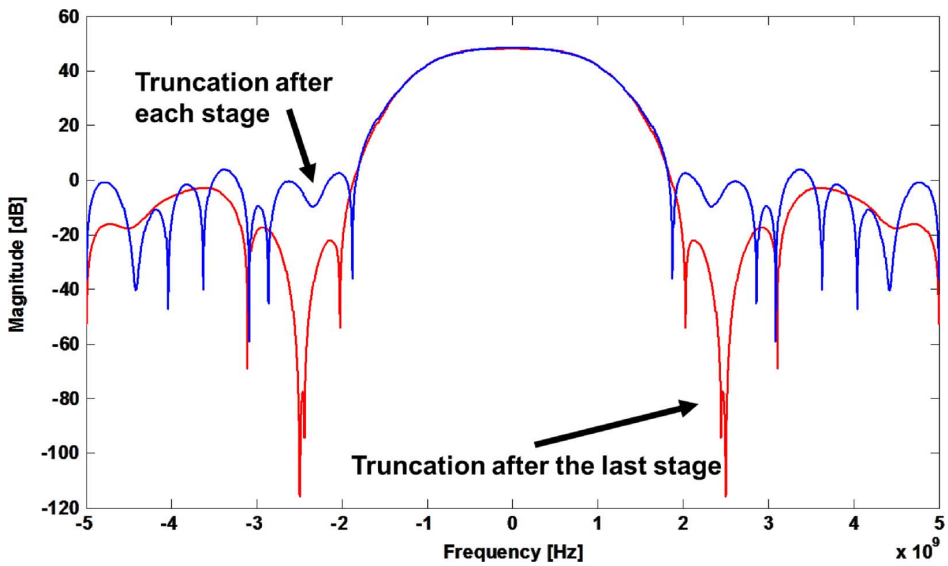

Fig. 8. Transfer function of the overall interpolator.

cients are realized by wired bit-shifts and don't require additional hardware.

Furthermore, it is not necessary to run the complete filter at 10 GS/s. To relax speed requirements, one could use parallel (poly-phase) architectures at a lower sample rate that are recombined into a high sample rate output data stream. However, the poly-phase structure introduces more complex routing and recombination of the output signals is also critical and involves several adder stages [21], [22]. Alternatively, it is possible to do the up-sampling in several steps, i.e., two steps in this case. In this way, only a small part of the filter actually works at the maximum sampling rate. This is the option taken here and is depicted in Fig. 5.

The next step is to determine a set of coefficients for the first and second interpolator, while trying to reduce complexity. In order to keep linear phase characteristics, the coefficient sets are supposed to be symmetric. At this point, filter synthesis tools have been used to find the required filter order. Finally, we explored a further simplification of the structure by dividing each of the FIR filters into a cascade of two identical filters as shown in Fig. 6.

As a final choice, each of the FIR filters at 5 GS/s has 6 coefficients, while each of the FIR filters at 10 GS/s has 3 coefficients. This minimizes the complexity of the filters at 10 GS/s while still meeting the specifications.

At this point coefficients are still floating point coefficients. Simple quantification of the coefficients does not produce satisfactory results. Instead, one can either do an exhaustive search over all possible quantified coefficient sets for the given structure, or use for example a genetic algorithm to find the optimum quantized coefficient set. The two criteria used for optimization are in-band ripple and out-of-band rejection. A genetic algorithm has been programmed to find an optimal set of powers of two coefficients with respect to these two criteria for the selected structure. The set of optimal coefficients is on a so-called Pareto front showing the optimal stop-band attenuation for a given pass-band ripple. The designer then chooses the most suitable compromise between the two criteria. Details on this algorithm can be found in [23] and [24]. Coefficients could be in the range from 2^0 to 2^{-6} given the 7 bit dynamic range. However, in practice the range used is from 2^{-1} to 2^{-4}. The coefficient sets selected are given in Table I.

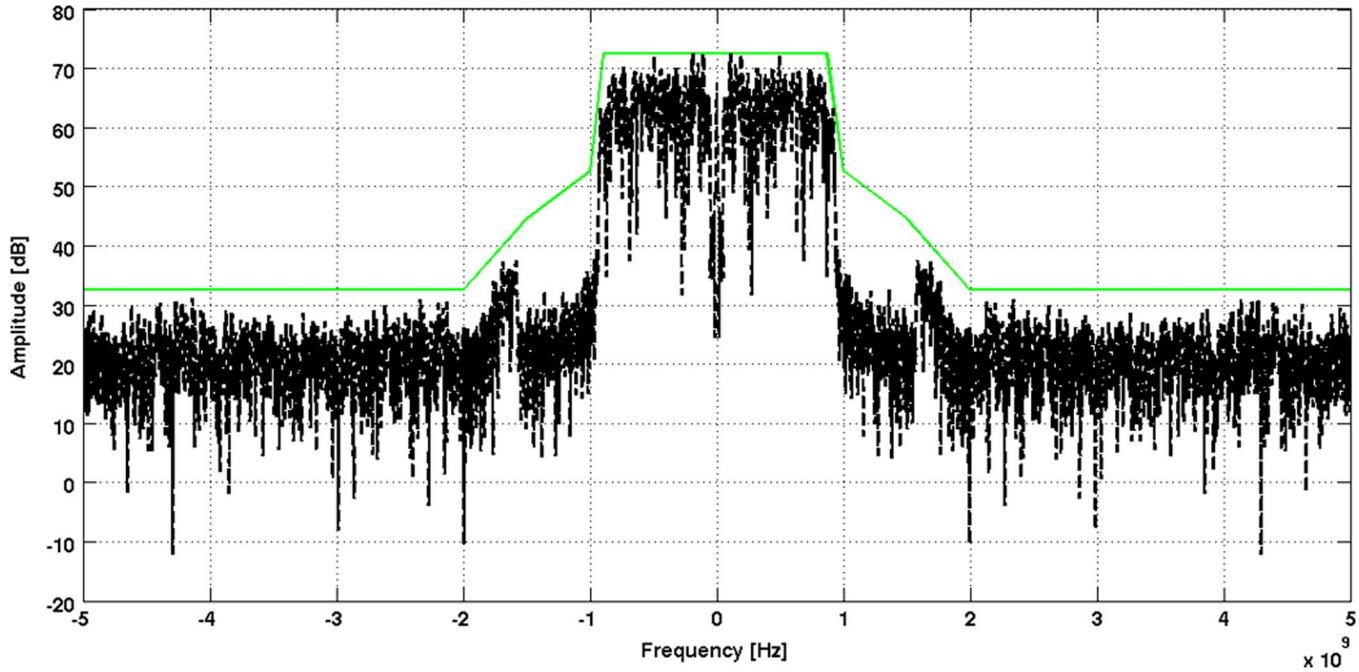

Fig. 9. OFDM signal filtered with final filter structure.

The final architecture, chosen for this work, is presented in Fig. 7. The filter output needs only 7 bit precision. To reduce the computational effort, each FIR output could have been truncated to 7 bits. However, the attenuation close to the band edge deteriorates significantly as shown in Fig. 8. The internal word length is therefore progressively extended up to 11 bits in order to avoid saturation and keep the maximum computational precision. Only the filter output is then truncated to 7 bits.

A global simulation of an OFDM symbol filtered with the chosen coefficients is shown in Fig. 9. Attenuation of signals in the pass band causes phase and amplitude errors in the constellation responsible for an increase of the error vector magnitude (EVM). The constellation of a random-data QPSK-modulated OFDM symbol at the interpolator output is represented on the I/Q chart in Fig. 10. Sub-carriers close to the band edge are attenuated with respect to the ones in the center of the band, which leads to this flower petal representation. The raw EVM before any equalization is 17.83% which is still compliant with the standard that requires an EVM $<19\%$ for class 2 devices.

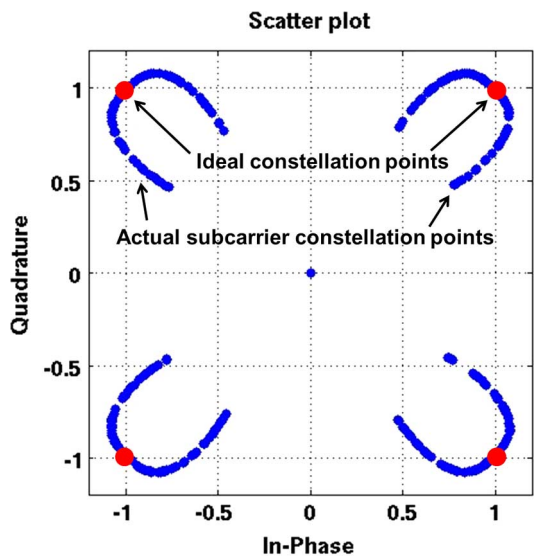

Fig. 10. Output constellation of QPSK modulated subcarriers.

IV. FIR Filter Design

The choice of the FIR filter hardware structure and the digital logic style is critical for high speed operation. Different structures exist to implement a FIR structure (direct, transposed, symmetric. . .). The transposed structure (Fig. 11) is chosen because the adders are spread over the filter and reduce the complexity of the critical path.

Only adders and delays (flip-flops) are needed, as the multiplications are implemented as hard wired shift operations. The critical path contains one adder and one flip-flop. This architecture can easily be pipelined as there are no feedback paths. The critical path has been evaluated with different logic styles for the adder in order to find the best implementation: combinational logic adder, transmission gate (TG) adder and complementary pass transistor (CPL) adder. The three different architectures have been designed in a 65 nm GP CMOS process. Simulations have been performed at nominal supply voltage and temperature set to 85° after extraction of resistance and parasitic capacitance from the physical layout.

TABLE II
Clock-to-Sum Delays of Different Adder Architectures

	CPL	TG	Combinational
Typical	40 ps	66 ps	50 ps
Fast	30 ps	46 ps	40 ps
Slow	48 ps	93 ps	66 ps

Table II shows for a 1-bit adder the Clock-to-Sum delays for different process corners at 1 V supply voltage. Similar results

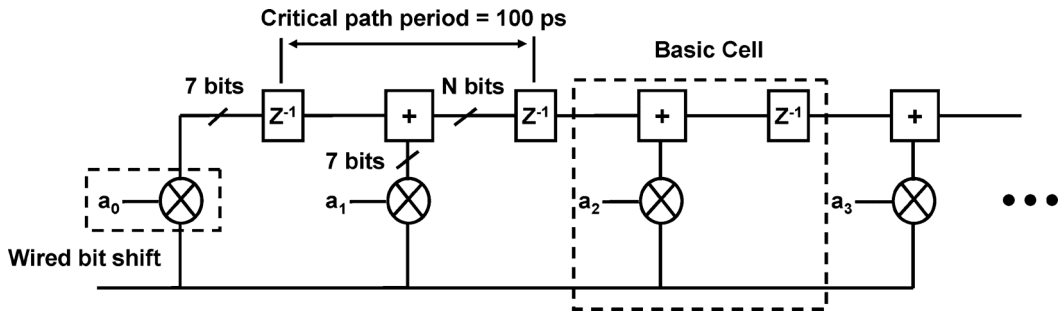

Fig. 11. Transposed FIR filter structure.

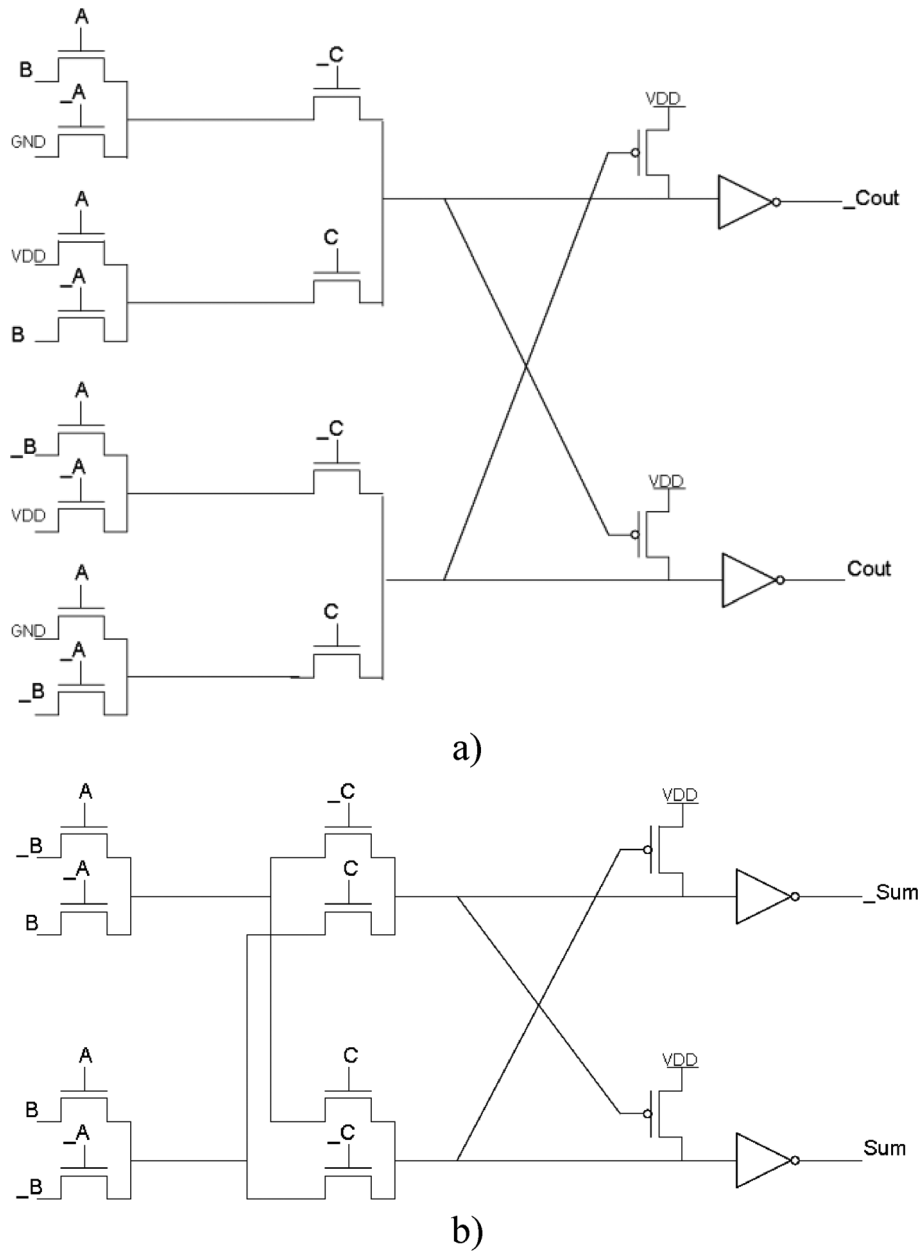

Fig. 12. CPL adder: (a) carry (b) sum.

have been obtained for the Clock-to-Carry delay. CPL logic is the fastest for all process corners. The drawbacks of CPL are a reduced noise margin, an increased number of wires to route in the physical layout and two times the number of flip-flops due to the complementary structure. The CPL adder, carry and sum, is presented in Fig. 12. The critical point in designing the CPL gates is the dimensioning of the level-restorer. The PMOS level restorer is a minimum size transistor while the NMOS transistors are two times the minimum size.

The True Single Phase Clock Flip-Flop (TSPCFF, Fig. 13) has been chosen as delay element [25]. It uses dynamic logic and has the advantage of requiring a single clock phase. Tran-

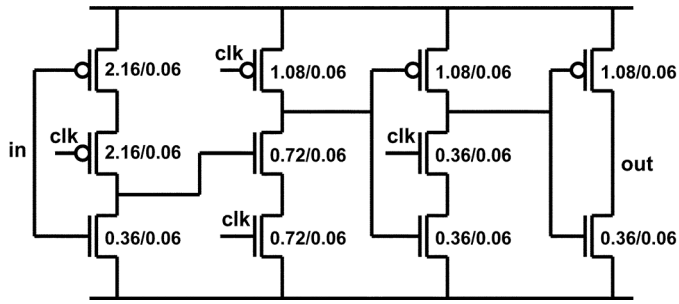

Fig. 13. True single phase clock flip-flop.

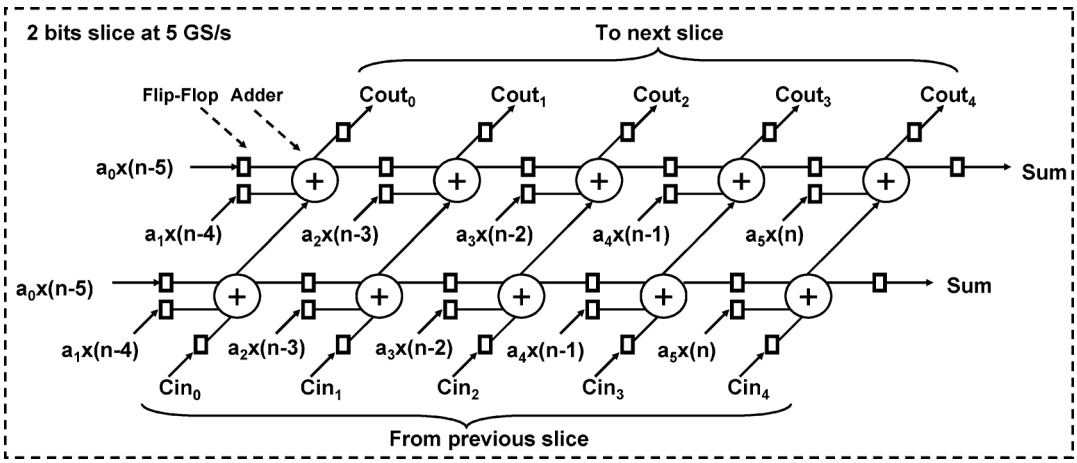

Fig. 14. FIR1 and FIR2-2 bit pipelined slice at 5 GS/s.

sistor sizes have been adjusted to provide symmetric rise and fall times at the output node. Simulations show a worst-case clock-to-output delay T_{CQ} of 42 ps and a setup time of 5 ps. The hold time of the flip-flop is close to zero.

The worst case critical path delay for a 1-bit implementation is therefore 95 ps. This means that operation at 10 GS/s is very close to the limit for this technology. Pipelined 1-bit slices are used for the 10 GS/s FIR filters, while 2-bit slices have been implemented for the 5 GS/s FIR filters. The 5 GS/s FIR filter could have been implemented as a 3-bit slice. However, the 2-bit slice version simplifies the interpolation from the 5 GS/s to the 10 GS/s parts. Figs. 14 and 15 show the block diagrams of one slice for each of the FIR filters. With exception of the carry input to the second adder in the 2-bit slice which is directly driven by the first adder, each adder input is driven by a flip-flop placed in its immediate vicinity. This avoids any excess delay due to interconnect. Due to the differential nature of the CPL structure, the actual implementation needs 10 flip-flops for a 2-bit adder stage and 6 flip-flops for a 1-bit adder stage.

The complete FIR architecture is presented in Fig. 16 for one slice from the input at 2.5 GS/s to the output at 10 GS/s. Extras flip-flops are needed to feed the pipeline at the input and to re-align the bits at the output. 4 and 5 extra flip-flops need to be inserted respectively for odd and even bits to provide the necessary inter-stage delays. The total count of flip-flops and adders is summarized in Table III.

Regarding the clock tree shown in Fig. 17, a combination of the mesh structure and the grid structure has been adopted in order to target a very low skew at the cost of slightly increased

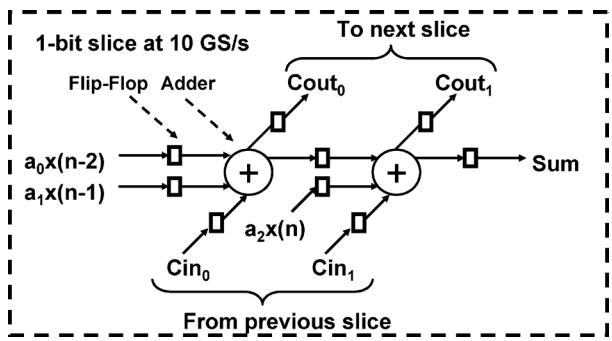

Fig. 15. FIR3 and FIR4-1 bit pipelined slice at 10 GS/s.

power consumption. A fan out of two has been chosen between each stage of the clock tree. The difficulty here is to provide a steep clock to the TSPCFF. A slow clock could turn both NMOS and PMOS on at the same time resulting in an undefined value.

V. Physical Layout

The circuit has been implemented in the 7 ML 65 nm GPLP CMOS process from STMicroelectronics. The filter core uses full custom layout in order to minimize line lengths and parasitic capacitances. The most critical signal is the carry out signal. Adjacent 1-bit and 2-bit bit slices are shifted in such a way as to minimize the length of this vertical connection.

Internal bit slice connections are in metal 2 and metal 3; the carry signals are routed using stacked metal 3 and metal 4. This

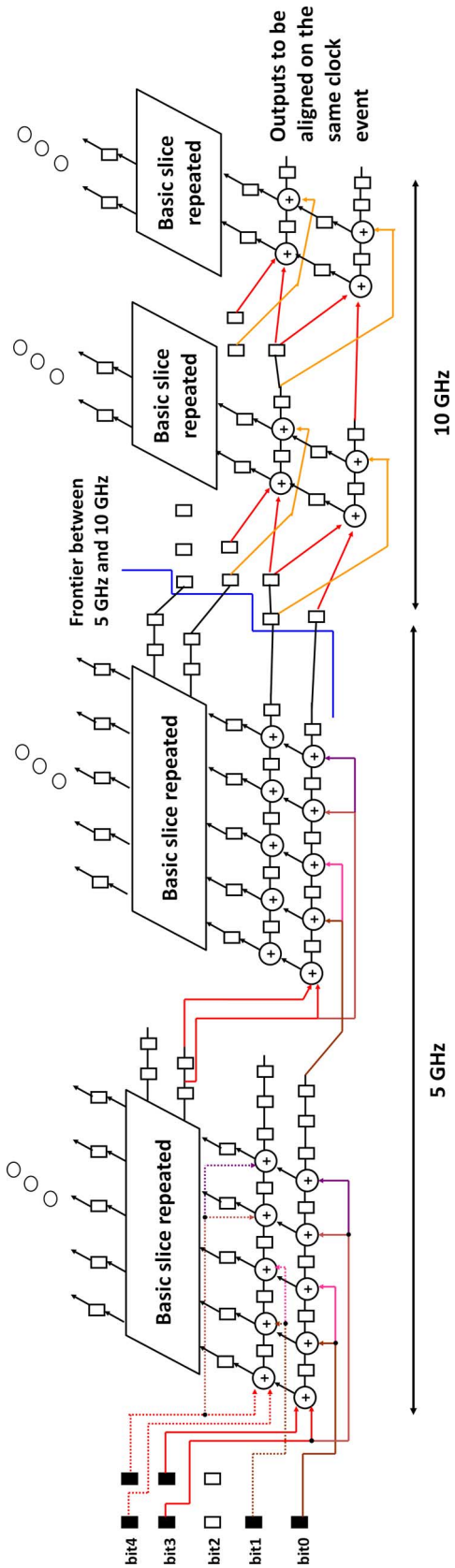

Fig. 16. Complete interpolator architecture (one slice).

slightly increases the global capacitance but decreases significantly the resistance of the line. The RC product and the propagation delay are thus decreased for the carry signal. VDD and GND are routed on the top metal layers. Additional flip-flops have been added directly at the input of each adder to isolate the adder from the interconnect delays. As dynamic flip-flops are vulnerable to noise, no signals are routed directly above flip-flop to avoid coupling with other signals and improve noise immunity. The layout of an elementary slice for a 5 GS/s filter is shown in Fig. 18. The same strategy has been used for the 10 GS/s slice depicted in Fig. 19.

TABLE III
TOTAL NUMBER OF ADDERS AND FLIP-FLOPS

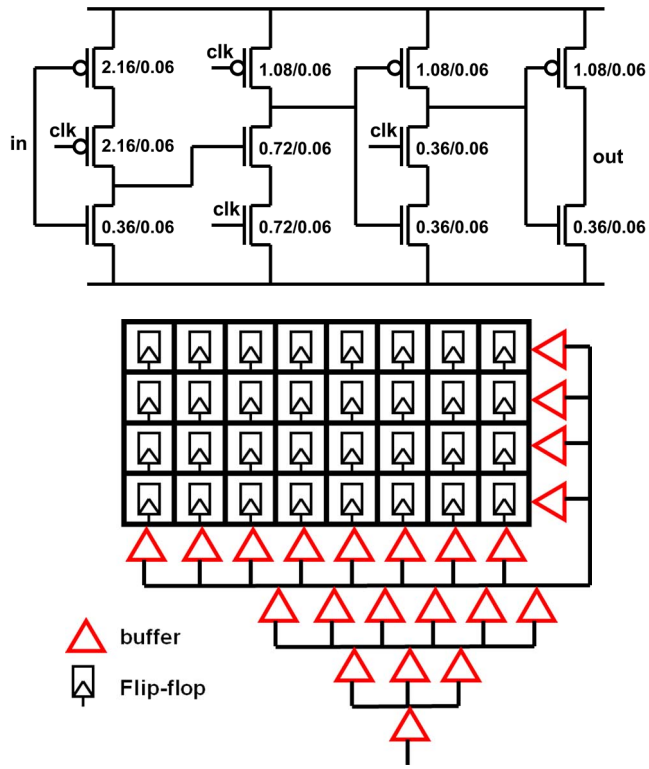

Fig. 17. Combined mesh and grid clock tree.

For the clock signal metals 4 and 5 are used. The hybrid clock tree is based on a grid. Metal 4 realized the vertical part of the grid and metal 5 realized the horizontal part of the grid. Buffers are inserted along the right vertical grid and along the horizontal grid. This topology can avoid setup violations as the clock "flow" goes from right to left while the data "flow" goes from left to right. TSPC flip-flops require fast clock edges for optimum performance. The final buffer stage is placed as close as possible to the TSPC flip-flops and a maximum of 12 TSPCFF are driven by a single buffer stage. Table IV summarizes the area occupied by the different blocks.

VI. Test Methodology and Chip Assembly

In order to test the circuit at full speed, 2×7 input bits need to be provided at a rate of 2.5 GS/s, and the same number of bits needs to be read at a rate of 10 GS/s. To avoid a large number of very high speed I/O pads, on-chip memories have been included in the test chip. This actually reduces the test chip size because of the lower number of pads. Furthermore, input and output memories can be written and read at low speed

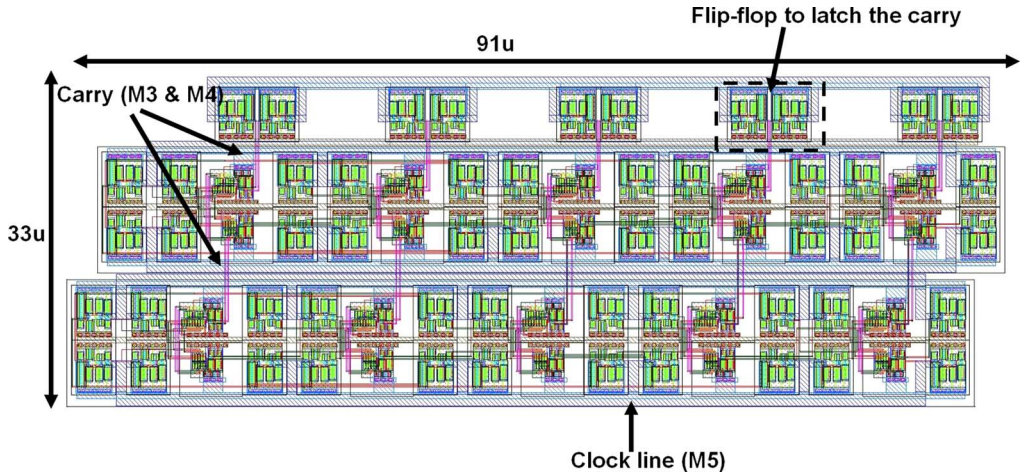

Fig. 18. Physical layout of a 5 GS/s filter slice.

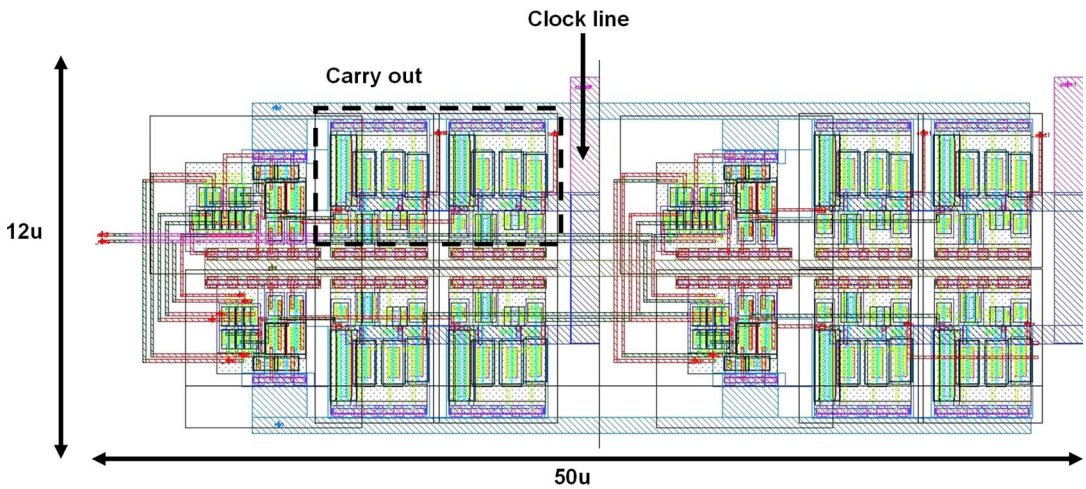

Fig. 19. Physical layout of a 10 GS/s filter slice.

TABLE IV
SUMMARY OF THE LAYOUT AREA OF THE DIFFERENT BLOCKS

Area	
Carry CPL area	4.7 x 3.8 um^2
Sum CPL area	4 x 4 um^2
TSPCFF area	5.4 x 4.5 um^2
5 GS/s slice area	91 x 13 um^2
10 GS/s slice area	50 x 12 um^2
5 GS/s FIR filter area	300 x 170 um^2
10 GS/s FIR filter area	295 x 170 um^2
Interpolator area	650 x 170 um^2

reducing dramatically the cost for the test setup. On the other hand, test vector depth is limited by the performance and size of the memory array.

The block diagram of the test chip is shown in Fig. 20. The input and output memories are realized with flip-flops as a shift register. To allow comprehensive testing, the input memory provides 7 bit data at 5 GS/s while the output memory is able to read 13 bit data at 10 GS/s. To simulate data at 2.5 GS/s as required for the targeted application, the input memory must be loaded with pairs of identical successive data. The depth of the output memory is two times larger than the depth of the input memory because of the higher sampling rate.

The input and output memories have been implemented with static flip-flops from the standard cell library. This is necessary to be able to write and read these memories in an asynchronous manner at very low speed. However, the maximum clock speed achievable for these shift registers is below 1 GHz. A 10-to-1 multiplexer (serializer) on each input bit and similarly, a 1-to-20 de-multiplexer (de-serializer) on each output bit allows parallel storage of the data in the memories at a data rate of 500 Ms/s.

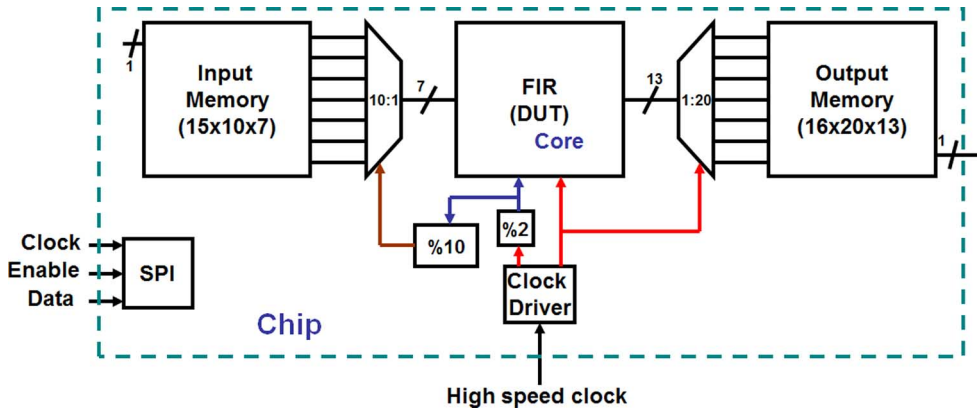

Fig. 20. Chip block diagram including test hardware.

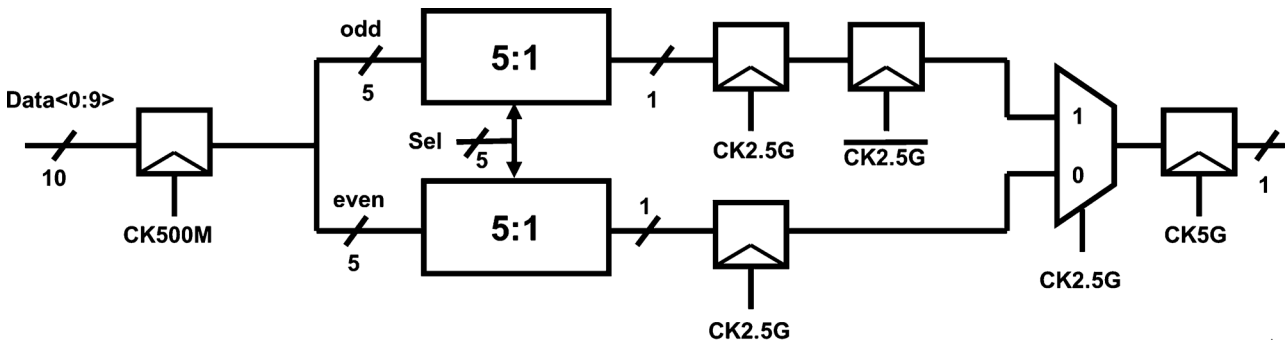

Fig. 21. Serializer architecture.

The implemented memory size is 10×15 7-bit words ($\sim$1 kbit) at the input and 20×16 13-bit words ($\sim$4 kbit) at the output. A loopback mode of the input memory allows for continuous full speed testing in order to measure the power consumption of the device.

An OFDM symbol is composed of 576 samples (512 data points $+64$ samples cyclic prefix) represented on 7 bits. Due to limited memory size, it cannot be loaded in a single test run. However, by using several consecutive test sequences with sufficient overlap in the input data to re-load the previous state into the interpolator the test setup allows the reconstruction of the response for a complete symbol. The input and output memory and the control logic have been synthesized from a VHDL RTL code but considering their high speed of operation the core, the serializer and deserializer are custom designs and layouts.

The serializer accepts 10 bits at 500 MS/s and serializes them to a 1 bit stream at 5 GS/s. The internal structure is illustrated in Fig. 21. The 10 bits are separated into odd and even data. The even and odd bits are separately serialized to 1-bit streams at 2.5 GS/s using transmission gate-based multiplexers with dedicated control signals. Finally, a multiplexer interleaves the two streams into one stream at 5 GS/s and resynchronizes them on the 5 GS/s clock. A deserializer architecture has been implemented at the output of the filter. In order to verify the core function all the bits (12 sum bits + 1 carry bit) are written in the output memory. The internal architecture of the deserializer as depicted in Fig. 22 is a 20-bit shift register at full clock speed connected to a 20-bit latch at memory clock speed.

Fig. 23 provides the implemented chip block diagram including the on-chip test hardware. 1.5 nF of gate oxide on-chip decoupling capacitance has been implemented in order to minimize supply voltage ringing. Fig. 23 shows a photomicrograph of the fabricated chip. The chip size including test hardware and pads is 800 μm $\times$ 1800 μm whereas the filter core occupies only 150 μm $\times$ 700 μm (0.1 mm^2).

VII. Measurements

Various test patterns have been used to verify functionality and correctness of the filter response by comparison to the model. Combinations of impulses are also used in order to test the dynamic functionality of the FIR. Furthermore the impulse response obtained is convoluted with OFDM symbols as shown in Fig. 24 in order to verify in the frequency domain that the spectrum mask requirements are met.

Measurements have been performed at different supply voltages and clock frequencies. A maximum operating frequency of 9.6 GHz is achieved at a supply voltage of 1.4 V. The supply current measured is 408 mA, resulting in a power consumption of 571 mW, including internal test hardware. The core however represents only 70% of the total power consumption, leading to an estimated current consumption of 285 mA (400 mW) at 9.6 GHz. A power penalty is due to the increase of the supply voltage. Table V compares the relative dynamic power consumption as a function of the supply voltage. The increase from 1 V to 1.4 V of the supply voltage roughly doubles the power

TABLE V
SUMMARY OF TOTAL MEASURED STATIC AND DYNAMIC POWER CONSUMPTION VERSUS SUPPLY VOLTAGE

VDD	Static supply current	Dynamic supply current per GHz clock frequency	Dynamic power consumption per GHz clock frequency	Power consumption per GHz clock frequency normalized to VDD = 1V	Maximum clock frequency
0.8V	5 mA	20 mA	16 mW	0,61	3 GHz
1V	7 mA	26 mA	26 mW	1	4 GHz
1.2V	9 mA	33 mA	40 mW	1,54	5 GHz
1.4V	12 mA	40 mA	56 mW	2,15	9.6 GHz

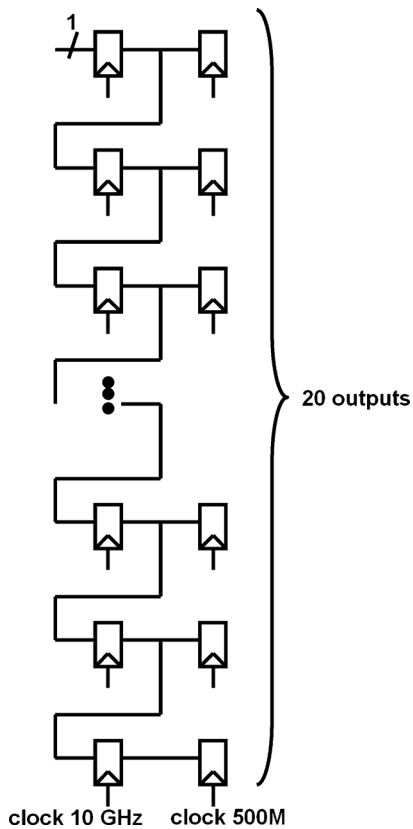

Fig. 22. Deserializer architecture.

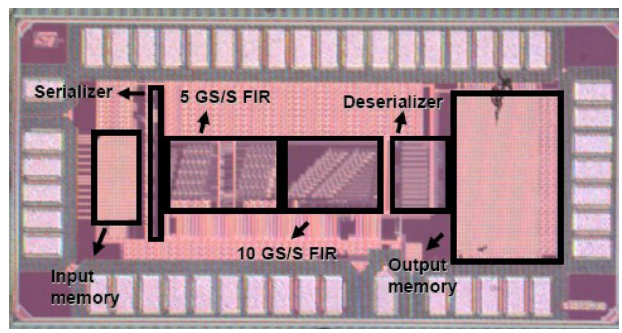

Fig. 23. Micrograph of the chip.

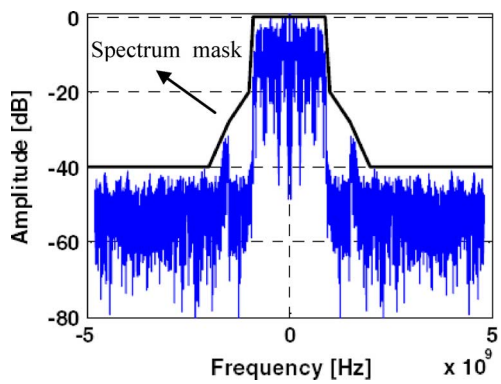

Fig. 24. OFDM symbols filtered by convolution with measured coefficients.

consumption at constant clock speed. It is however necessary to reach the targeted speed.

Fig. 25 presents the Shmoo diagram. 9.6 GHz is the maximum clock frequency that could be reached in measurements. Retro-simulations have shown that the limitations come from the clock driver and the clock tree interface. The clock driver shapes the input sine wave and provides the clock to the clock tree. The clock driver can however work up to 10 GHz by increasing the supply voltage beyond the nominal value up to 1.4 V. Nevertheless the clock provided to the clock tree is degraded and affects the global performance of the FIR.

The measured performance of the circuit is summarized in Table VI and compared to the semi-digital FIR described in [18]. Note that summing operations in [18] are done in the analog domain; the circuit can therefore not be used in conjunction with a DRFC. High speed digital designs in 65 nm CMOS technology have been reported in [26]–[28] It is however difficult to compare the circuits given the completely different architecture and function. Nevertheless, the presented circuit works close to the limits of this technology node.

An alternative implementation approach for interpolator FIR filters is the polyphase architecture using multipliers operating at low speed. Such a filter for a similar application is described in [17]. This 15-tap 8-way polyphase filter with an output data rate of 3.4 GS/s requires 68 product-sums (8.5 product-sums per output sample). For a specification equivalent to the filter described in this paper, a 25-tap 24-way polyphase filter would

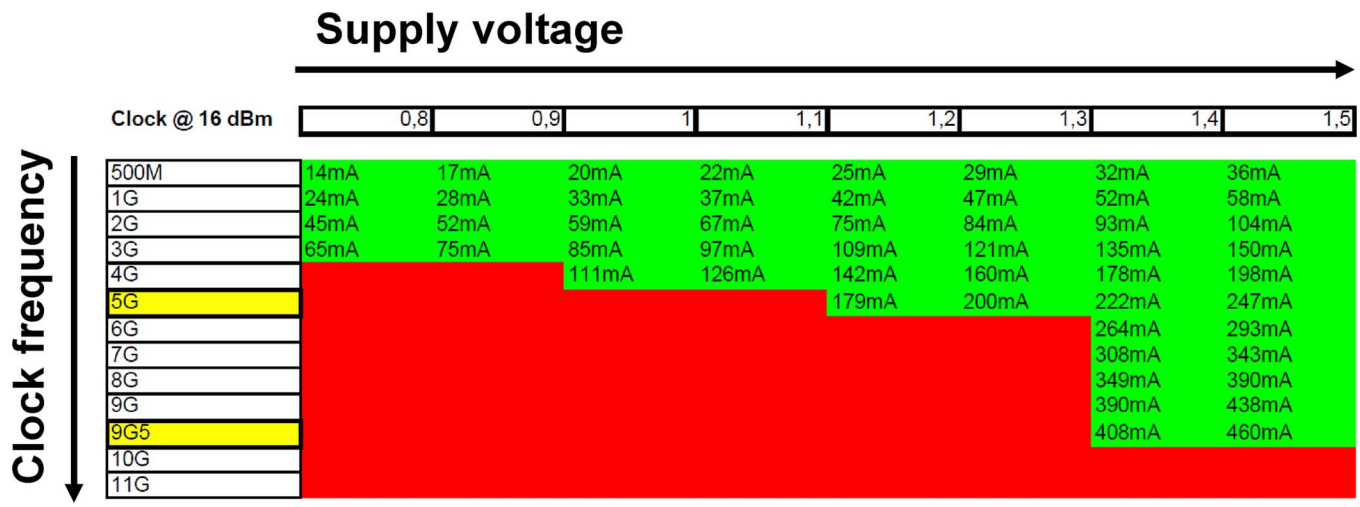

Fig. 25. Total power consumption for different combinations of clock frequency and supply voltage.

TABLE VI
PERFORMANCE SUMMARY AND COMPARISON TO STATE OF THE ART

	This work	[18]
Technology	65nm GP CMOS	0,25µm SiGe HBT
Sampling frequency	9.6 GHz	7 GHz
Number of FIR taps	18	17
Attenuation at mask edge	40dB @ 2.2GHz	19dB @ 2.2GHz
Power consumption	400 mW @ 1.4V	1W (including DAC)
Area	0.1 mm^2	~0.8 mm^2 (estimate)

be necessary requiring 168 product-sums (7 product-sums per output sample). The corresponding power consumption for such a filter extrapolated from [17] is roughly 100 mW not including the 7-bit 24-to-1 multiplexer operating at 10 Gs/s that is needed at the output. The total power consumption will again depend on the requirements of the fastest elements. For comparison, the computational effort for the implementation described in this paper is only 9 sums per output sample without any multiplication. However, due to the speed requirements some power penalty had to be paid. This penalty could be largely reduced in more advanced processes.

VIII. CONCLUSION

The design of a high-speed digital interpolator in a 65 nm CMOS technology has been presented. In order to achieve 10 GS/s output rate, careful optimisation at system, circuit and layout level was necessary.

Thanks to the 4× oversampling architecture, the circuit satisfies the IEEE 802.15.3c spectrum mask requirements over the full band of the standard without any analog filtering regardless of the channel used.

On-chip test pattern memories allow full speed testing of the circuit. Total core circuit power consumption is 400 mW, chip area 0.1 mm^2. It is expected that the power consumption of the digital interpolator could be largely reduced in more advanced CMOS technologies. Not only the power per operation would be lower, but faster technology would allow a different logic style not requiring complementary data, which reduces the number of flip-flops by a factor of two.

ACKNOWLEDGMENT

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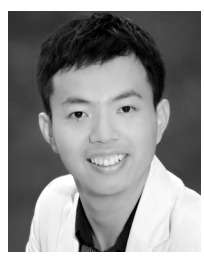

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A Reconfigurable IF to DC Sub-Sampling Receiver Architecture With Embedded Channel Filtering for 60 GHz Applications

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***Abstract*—This paper presents the theoretical analysis and simulation results of an IF to DC subsampler for 60 GHz heterodyne receivers architectures. A particular arrangement of the frequency plan allows embedded anti-alias filtering. Down-conversion, channel filtering and IQ demodulation are merged into a unique operation at no extra cost in terms of area and power consumption. The adjacent and alternate channel rejections for the 802.15.3.c are respectively more than 15 dBc and 23 dBc thanks to charge domain subsamplers. This paper presents solutions for the implementation of the system and its integration into a complete 60 GHz receiver. Advanced analysis is made for critical points of the architecture: generation of the integration windows, IQ demodulation, noise folding and effect of clock jitter. The proposed architecture is validated by simulations and complies with the requirements of the standards for 60 GHz wireless communications. The result of this study shows that sub-sampling is suitable for high bandwidth and high data-rate receiver systems.**

***Index Terms*—Sub-sampling, wireless receiver, 60 GHz.**

I. Introduction

SIXTY GigaHertz radio is the most promising candidate for high data rate short range wireless communications targeting the delivery of uncompressed high-definition video and fast downloading. The frequency plan used in the 802.15.3c standard [1] is composed of four channels of 1760 MHz bandwidth each in the unlicensed band around 60 GHz. These channels are centered respectively on 58.32, 60.48, 62.64 and 64.80 GHz. Other standardization groups such as ECMA-387, WirelessHD and the WiGig Alliance share the same frequency allocation for the four channels.

The context of this work is the study of a 60 GHz receiver with software defined radio (SDR) capabilities for ultra-high data rate communications. This work targets the 802.15.3c standard with a single carrier (SC) block transmission and a quadrature phase-shift keying (QPSK).

In state of the art of 60 GHz receivers, classical radio architectures have been reported: direct conversion or heterodyne [2]–[4]. Recent research on RF receivers in the low GHz range has focused on low cost, low power and reconfigurable solutions. Sub-sampling receivers are attractive in terms of area and power consumption [5]. The sub-sampler described in [6] targets the 800 MHz to 5.8 GHz band. For this target, the sampling frequency is up to 75 MS/s for a carrier frequency up to 5.8 GHz. After the sampler, the SNDR is 22.9 dB. In order to overcome the problem of noise folding due to the sub-sampling, digital processing such as averaging is introduced. This latter increases the final SNDR up to 73.1 dB which is large enough to reach the fastest data rate of the 802.11g standard. This baseband processing is possible because the data rate of this standard is 54 Mbps. However it is not a suitable solution for multi-Gbps data rate systems. Another sub-sampling solution has been presented in [7]. This system is a multi-standard RF heterodyne receiver. The RF signal is sampled by a first track and hold switch clocked at 761.8 MHz. The resulting IF frequency is between 145 and 185 MHz function depending on the handled band. A second track and hold switch down-converts the signal from this IF frequency to baseband. The simulation results of this system show that GSM, UMTS and 802.11g standards can be received by a single receiver because the SNR degradation due to the sub-sampling stage complies with the receiver requirements for all these standards. To the author's knowledge, no solution has been proposed for higher RF frequencies.

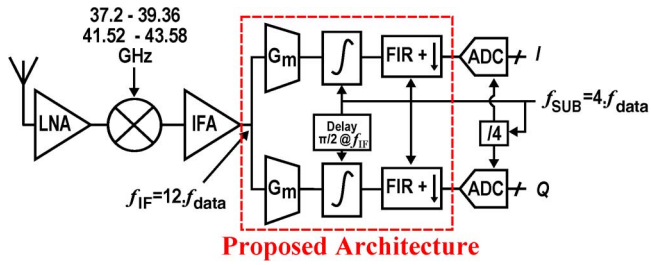

Fig. 1. Complete receiver architecture.

These architectures are hardly transposable for direct sub-sampling of signals around a 60 GHz carrier because of very stringent constraints on bandwidth, folded noise and clock jitter. A solution to relax these constraints is to perform sub-sampling at an intermediate frequency, creating a heterodyne receiver. This is the approach developed in this paper. Beyond relaxing the subsampler specifications, the heterodyne architecture allows synchronization of the base-band and RF sampling frequencies. Moreover a proper choice of the IF frequency and sampling interval introduces anti-aliasing filtering with no extra effort.

Fig. 1 shows the complete architecture of a 60 GHz heterodyne receiver integrating the proposed sub-sampler. This paper

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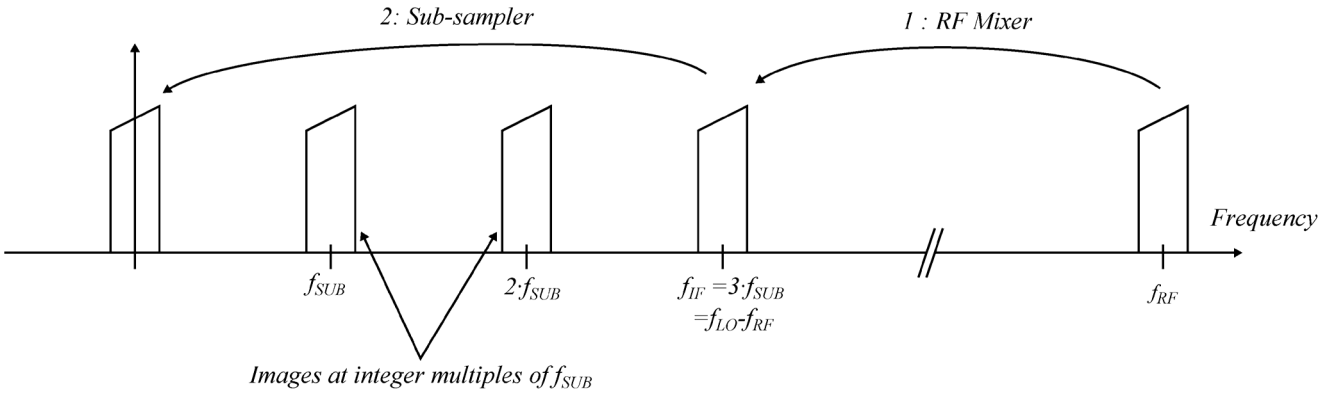


Fig. 2. Simplified representation of the successive down-conversion operations.

focuses on the second part of the receiver: from IF to analog baseband. First, transconductance stages (G_m) convert the IF input voltage into current. Then, charge-domain integrators perform down-conversion. Finally, Finite Impulse Response filters (FIR) down-sample the signal to the final data rate (f_{data}).

The IF is fixed for all RF channels and needs to be an integer multiple of the baseband data rate. The choice of the IF frequency is a trade-off between RF complexity and base-band timing constraints. For lower IF, the timing constraints in the back-end decrease while the local oscillator frequency increases. For heterodyne receivers such as the one reported in [2] the IF is typically chosen to be around 20 GHz to allow LO sharing for the first and second mixer stages. Thus, an IF frequency (f_{IF}) around 20 GHz would be compatible with existing RF front-ends.

The remainder of this paper is organized as follows: Section II introduces the theory of sub-sampling applied to this architecture. Section III details the IF-to-DC down-conversion block. Finally Section IV deals with the evaluated performances of the sub-sampling block.

II. Theory of Sub-Sampling Applied to the Proposed Architecture

A. Downconversion

Fig. 2 shows a simplified representation of the two successive operations performed in the system in order to down-convert the signal from the 60 GHz carrier f_{RF} down to DC. First, the RF mixer in the front end translates the signal from f_{RF} to f_{IF}. Second, the sub-sampler downconverts the IF signal around DC by sampling the signal at f_{SUB}. In order to be exactly around DC after the second operation, f_{IF} should be an entire multiple of f_{SUB}. Consequently a defined value of the LO frequency has to be chosen in order to put the desired channel around the fixed IF frequency.

B. Charge Domain Sub-Sampling Process

In sampling systems, there are two different ways to sample a signal: in voltage domain or in charge domain. In voltage domain the sample is taken at the sampling instant. In charge domain the signal is integrated during a defined period.

In voltage domain sampling, the value of the tracking capacitor and the on-resistance of the switches define the bandwidth of the sampler while in charge domain sampling, the bandwidth is defined by the integration window. The error due to the sampling clock jitter is reduced in charge domain sampling because the result depends on both rising and falling edge of the clock while in voltage domain, the sampling value only depends on the rising or falling edge. From a designer point of view, the voltage domain sampling only requires a sampling switch and sampling capacitor. The charge domain sampling is more complex because it requires in addition to the previous elements, a V-to-I converter, a reset system and a complex clock strategy.

Consequently, the voltage domain sampling is the best candidate for low-bandwidth systems because the implementation is simple. However, with the target of high frequency and high bandwidth systems, the charge domain sampling is the best candidate because of its reduced timing constraints. For this architecture the charge domain sub-sampling is the most suitable solution in terms of bandwidth and reconfigurability [8].

The charge sampler is composed of a transconductance stage (G_m) followed by a switch clocked at f_{SUB} and an integration/sampling capacitor C_s. Integration is done during an integration time T_i. The result of the integrated voltage on C_s is given by:

$$V_{OUT}(t) = \frac{1}{C_s}\int_0^{T_i} I_{IN}(t)dt \tag{1}$$

where V_{OUT} is the output voltage of the integrator and I_{IN} is the current flowing from the G_m stage. Considering this latter as the result of the conversion of the transconductance, the output voltage is a function of the voltage at the input of the transconductance V_{IN}

$$V_{OUT}(t) = \frac{G_m}{C_s}\int_0^{T_i} V_{IN}(t)dt \tag{2}$$

After Fourier transform of this expression, the frequency domain transfer function of the charge-domain integrator is given by:

$$|H(f)| = \frac{G_m}{C_s}\frac{|\sin(\pi f T_i)|}{\pi f} \tag{3}$$

The frequency dependent part of this transfer function only depends on T_i. Fig. 3 shows the result of the integration of a

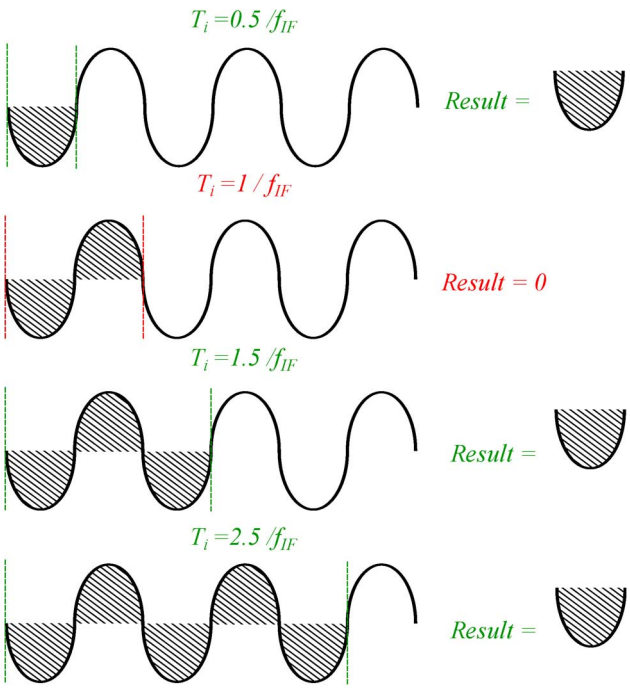


Fig. 3. Result of the integration of a sine wave at f_{IF} for several T_i.

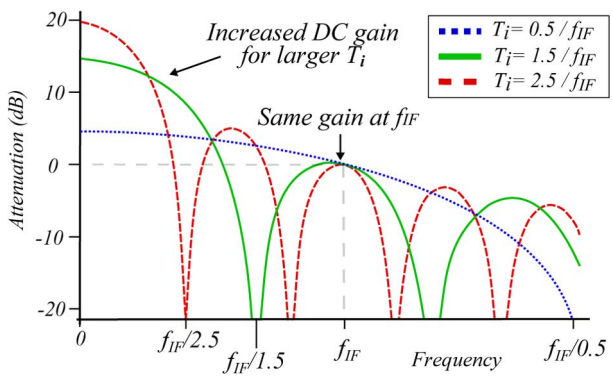


Fig. 4. Frequency response of the integrator for different N_{period}.

sine wave at f_{IF}, for given values of T_i. T_i has to be chosen such that $|H(f)|$ has a maximum for $f = f_{IF}$, which translates into the following requirements:

$$T_i = \frac{N_{period} + 0.5}{f_{IF}} \tag{4}$$

where N_{period} is an integer number. As shown in Fig. 4, for each value of N_{period}, a local maximum is found around f_{IF} and a notch is found every $1/T_i$. The main difference is DC gain: as T_i increases, the DC gain increases. This will influence noise folding as discussed in the next section.

C. Noise Folding

As sub-sampling receivers use aliasing of signals, they are consequently subject to noise folding. Fig. 5 shows how high frequency noise is aliased into the baseband. The total integrated noise over the entire band is:

$$P_{noise} = \int_{-\infty}^{\infty} V_{OUT}(f)^2 df = \int_{-\infty}^{\infty} V_{IN}^2 \left|H(f)\right|^2 df \tag{5}$$

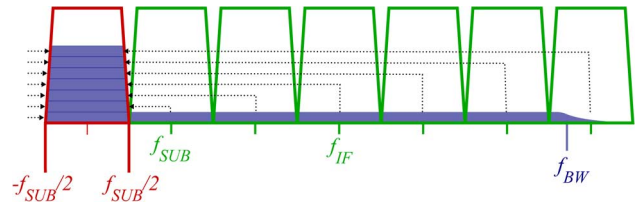


Fig. 5. Schematic representation of noise folding during the sub-sampling operation.

TABLE I
EFFECTS OF FILTERING ON FOLDED NOISE POWER

$T_i(ps)$	N_{period}	Noise Power w/o filtering (dBm)	Noise Power with filtering (dBm)
25	0	-28.2	-32.1
71	1	-23.5	-32.6
119	2	-21.2	-32.8
262	5	-17.8	-32.8

where V_{IN} is the input voltage at the antenna, $H(f)$ is the transfer function of the sampler defined in (3) and V_{OUT} is the output voltage, after the sampler. The input noise is considered being white over all the frequencies, so (5) is equivalent to:

$$P_{noise} = V_{IN}^2 \int_{-\infty}^{\infty} \left|H(f)\right|^2 df \tag{6}$$

Fortunately the bandwidth of the sampler is limited to f_{BW} thanks to the association of the sampling capacitor and the resistance introduced by the non ideal sampling switch. This limits the integrated noise power. It has been shown in [9] that the noise power is equal to:

$$P_{noise} = T_i \left(\frac{G_m}{C_s}\right)^2 \tag{7}$$

This represents the total theoretical noise power due to thermal noise on the antenna, integrated by the sampler. Regarding (7), low values of T_i seem to be the best choice because the total noise power at the output is lower. For f_{IF} around 20 GHz, the integration pulse width would be about 25 ps. For larger pulses, DC noise power increases. Equation (7) considers an infinite bandwidth for the elements of the receiver. The input noise at the antenna is constant for all frequencies. Knowing that frequency response of the sampler is a sinc shape, the most important part of the noise power is inside the first lobe. This first lobe is filtered while considering the actual limited bandwidth of the elements of the receiver. Each part of the receiver (Antenna, LNA, Mixer and IF amplifier) is considered as a 1st order high pass filter, mainly due to AC coupling between stages. Consequently the combination of all the front-end elements produces a 4th order high-pass filter shape. An assumption is made on the cut-off frequency of about 10 GHz for calculation purposes.

Table I shows the impact of the RF frequency selectivity on the noise power for different integration windows. These calculations consider thermal noise only. The other conditions are $G_m = 10$ mS, $C_s = 50$ fF, the gain of the front-end is 24 dB and the global noise factor is 5 dB. Considering (7) in the first

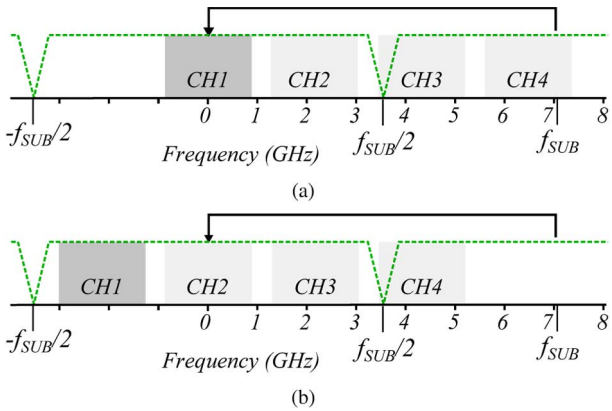


Fig. 6. Aliasing of channels while listening to the first/last channel (a) or the second/third channel (b).

column, the integrated noise power increases with T_i if no filtering is applied. While considering the limited bandwidth of each component of the receiver in the second column, the integrated noise power is roughly the same for all values of T_i. As a conclusion, N_{period} can be chosen independently of folded noise power considerations.

III. IF Sub-Sampling Architecture

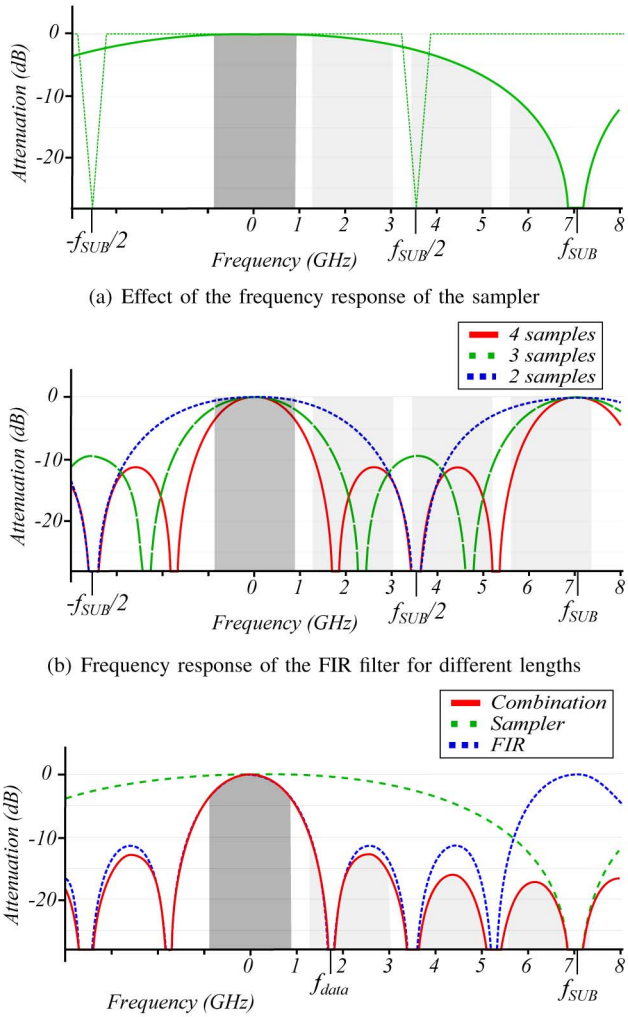
A. Frequency Planning

The baseband data rate defined by the 802.15.3c standard is 1.76 GS/s (f_{data}) in the single carrier case. Channel spacing is approximately 2 GHz and the total occupied bandwidth of the standard is therefore approximately 8 GHz. The sampling frequency f_{SUB} in the proposed architecture is chosen to be four times the baseband data rate, i.e. 7.04 GHz.

When using sampling frequencies lower than the standard's allocated bandwidth, in-band aliasing can occur. As shown in Fig. 6(b), when listening to the second or the third channel, the channels are aliased out of the band of interest. The critical situation appears when receiving the channels at the low or at the high end of the band because, as shown in Fig. 6(a), the channel at the other side of the standard's band produces in-band aliasing. By choosing an IF frequency of 3 times the sampling frequency ($f_{IF} = 21.12$ GHz) associated to a T_i of $1.5/f_{IF}$ ($N_{period} = 1$) the sampler provides notches at an offset frequency of 7.04 GHz from the IF frequency. These notches introduce effective anti-aliasing filtering for the critical case [10]. This is illustrated in Fig. 7(a).

Sampling the signal at four times the baseband data rate allows the implementation of a FIR filter. Fig. 7(b) shows the frequency response of averaging 2, 3 or 4 successive samples. The notch provided by the sampler filters the fourth channel in the critical case. The second and third channels could also be aliased onto the baseband. As shown in Fig. 7(b), the FIR filter which offers the best attenuation for the second and third channels is the averaging over 4 successive samples. This results in the transfer function of (8).

$$FIR(z) = 1 + z^{-1} + z^{-2} + z^{-3} \tag{8}$$



(a) Effect of the frequency response of the sampler

(b) Frequency response of the FIR filter for different lengths

(c) Effect of the frequency response of the sampler combined to the averaging of four successive samples

Fig. 7. Frequency planning. (a) Effect of the frequency response of the sampler; (b) Frequency response of the FIR filter for different lengths; (c) Effect of the frequency response of the sampler combined to the averaging of four successive samples.

TABLE II
Adjacent Channel Rejection

Channel	Rejection (dBc)
n+1	15.7
n+2	23.1
n+3	30.23

As shown in Fig. 7(c), the combination of both sampler and 4 coefficients FIR filter provides an efficient anti-aliasing filter for all adjacent channels of the 802.15.3c standard. Table II shows the simulated channel rejection when considering integrated power over the 1.76 GHz channel bandwidth.

The main advantage of the proposed architecture is the optimal use of the channel filtering capabilities in the down-conversion process.

B. Generation of the Integration Window

For direct detection of the I and Q values of the transmitted symbol, the beginning of the integration window needs to be

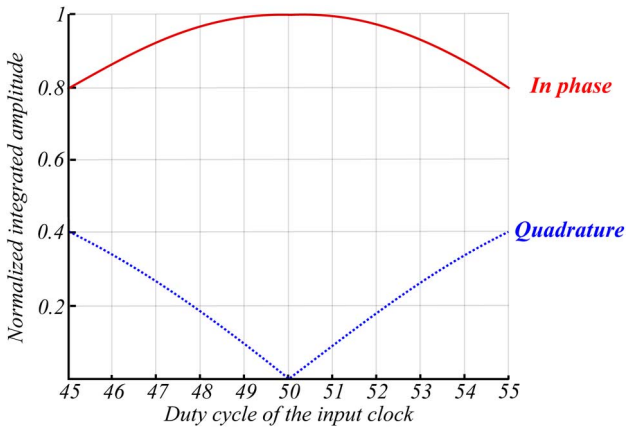


Fig. 8. Coupling between I and Q after integration.

synchronized with the beginning of the symbol. A continuously variable delay covering a full clock period of the sub-sampling clock at 7.04 GHz is needed for this adjustment in the main clock path. In the following, it is assumed that the sub-sampling clock is synchronized on the incoming data symbols. It is furthermore necessary to control adequately the duty-cycle and the I-Q delay as described in the following sections.

The input IQ signal is defined as:

$$V(t) = I \cdot \sin(2\pi f_{IF} t) + Q \cdot \cos(2\pi f_{IF} t) \tag{9}$$

Considering an integration interval from 0 to T_i, where T_i is defined in (4), the output corresponds to I value. If the integration time is delayed by a quarter of the period, then the output corresponds to the Q value. Considering an error on the integration time, a small part of the I (or Q) signal will leak onto the Q (or I) value and this will result in coupling between both values. Consequently the integration window width has to be monitored in order to maintain the sensitivity of the receiver.

The input frequency is $4 \cdot f_{data}$ and the needed integration window (T_i) is $1.5/f_{IF}$, as described earlier. The integration pulses can be directly created using the input clock by implementing a simple pattern generator. Consequently, the duty cycle of the reference clock should be strictly kept at 50% to ensure a correct constellation.

Fig. 8 shows how I and Q are coupled together as a function of the input clock duty cycle. This calculation considers an ideal sampling instant. For a duty cycle variation of 1%, the integrated value on the in-phase path is nearly equal to 1, but on the quadrature path, the value is 0.1. This means that there is a coupling noise that limits the SNR to 20 dB in this case.

State of the art on duty cycle correctors mainly focuses on high speed locking solutions for low frequency clocks (up to 2 GHz) [11], [12]. In the proposed application, the reference clock frequency is higher but the locking time is not critical. A simple RC circuit can be used to monitor the time domain average of the clock signal which directly relates to the duty-cycle. The duty cycle can be adjusted to bring the time domain average within given limits.

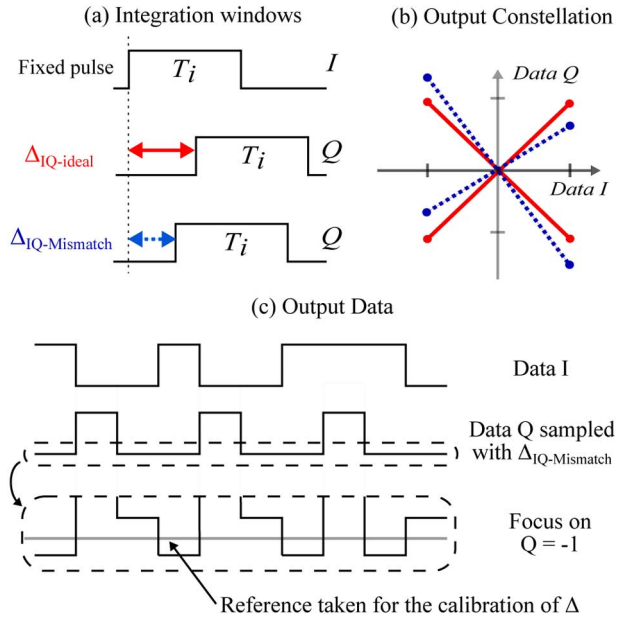


Fig. 9. Integration windows used for I-Q demodulation with $\Delta_{IQ-ideal}$ and with $\Delta_{IQ-Mismatch}$ (a), the resulting constellation (b) and the effect of the output value for Q(c).

C. IQ Coupling During Demodulation

I-Q data can be directly demodulated on two separate channels using a controllable delay. Considering an ideal integration window T_i and an ideal sampling instant for I, the integrated value for the Quadrature path is:

$$V_Q = \int_{\Delta}^{\Delta+T_i} V(t) \cdot dt \tag{10}$$

where $V(t)$ is the input signal defined in (9) and Δ is the I-Q delay. After integration (10) is equivalent to:

$$V_Q = -I \left[\frac{\cos(2\pi f_{IF} t)}{2\pi f_{IF}} \right]_{\Delta}^{\Delta+T_i} + Q \left[\frac{\sin(2\pi f_{IF} t)}{2\pi f_{IF}} \right]_{\Delta}^{\Delta+T_i} \tag{11}$$

This equation shows that the output value for the quadrature path is a combination of two contributions. The first one is function of I, the second one is function of Q. With an ideal sampling instant for the quadrature path, the first contribution is equal to zero so the output constellation is square (Fig. 9). The ideal delay between I and Q corresponds to a phase difference of $\pi/2$ at f_{IF}.

$$\Delta_{IQ-ideal} = \frac{1}{4 \cdot f_{IF}} = 11.8 \text{ ps} \tag{12}$$

When this I-Q delay differs from ideal value (12), coupling appears between I and Q as shown in Fig. 9. This coupling noise is given by the ratio of the two parts of V_Q:

$$IQ_{coupling} = \left[\frac{\cos(2\pi f_{IF} t)}{\sin(2\pi f_{IF} t)} \right]_{\Delta}^{\Delta+T_i} \tag{13}$$

Considering a maximal error of 10%, the previous equation gives that the maximum allowable deviation is 0.7 ps around the ideal value defined in (12).

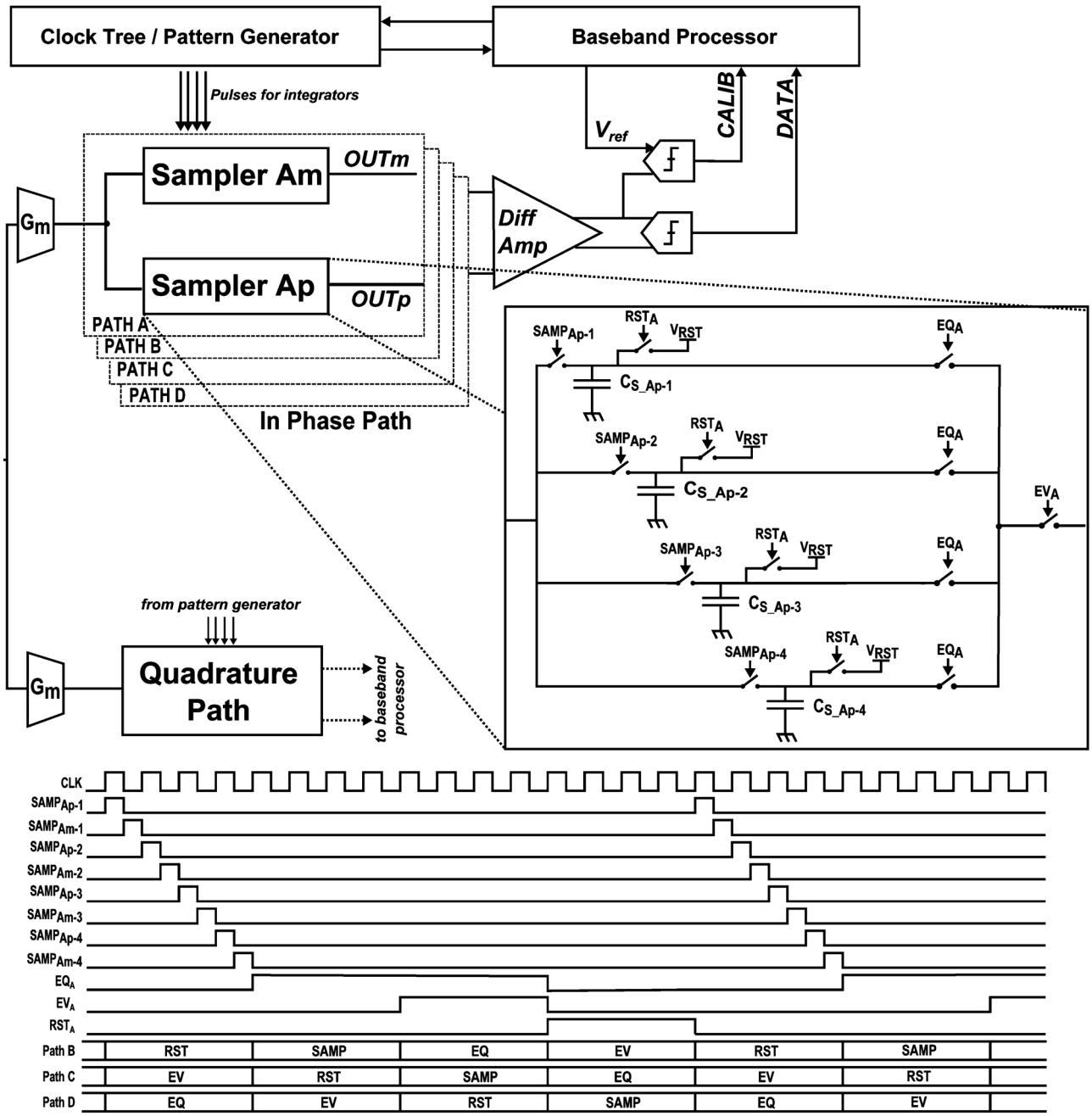


Fig. 10. Proposed sub-sampler implementation and timing diagram.

The adjustment of Δ_{IQ} is done by evaluating IQ coupling effect described in (13) and shown in Fig. 9(c). In presence of a delay error, V_Q for $\mathrm{Q} = -1$ has two different values for $\mathrm{I} = 1$ and for $\mathrm{I} = -1$. This difference can be detected by an appropriately set reference voltage and is then used to correct the delay error.

D. Sub-Sampler Implementation

The principle of operation of the proposed sampler and FIR is shown in Fig. 10. It is composed of 4 paths (A to D) working in an interleaved scheme. Each path comprises two parts: a positive one which samples the signal during a first T_i period and a negative one which samples the signal during the next T_i period, as described on the timing diagram of Fig. 10. The final result is the difference between both sides.

In the first phase, four successive samples are accumulated at f_{SUB}. In order to avoid errors introduced by the finite output impedance of the G_m cell, each sample is acquired on a separate capacitor.

The second phase is the averaging of the four values by turning the EQ switches on. All sampling capacitors are identical, so averaging of four successive samples implements the FIR filter function given by (8).

During the third phase, the EV switch is activated and connects the sampling capacitors to the output amplifier. This amplifier acts as a buffer and introduces bandwidth limitations.

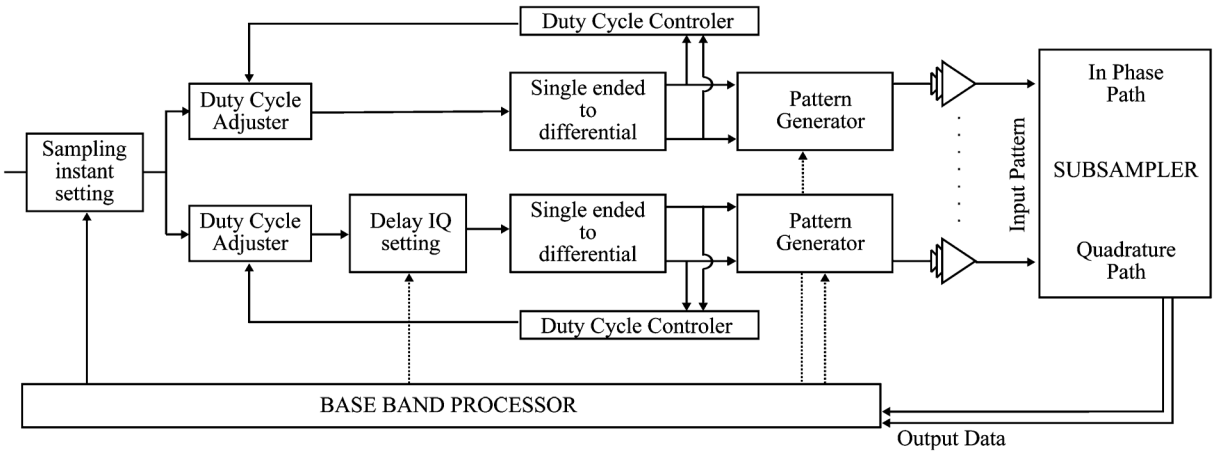


Fig. 11. Architecture of the clock generator in the proposed architecture.

When the switches turn on and off, charges are injected and pumped onto the capacitors and this results in voltage glitches. As they appear as a common mode signal, these glitches are rejected by the differential amplifier. The four paths working in parallel ensure that capacitors are always connected to the differential amplifier input in order to avoid an undefined state. The output data value is extracted by a Schmitt trigger. A second Schmitt trigger monitors the DC value just after the differential amplifier. This monitoring is used to perform equalization of the output constellation.

During the fourth phase, the sampling capacitors are reset.

E. Clock Generator of the Sub-Sampler

Fig. 11 represents a detailed block diagram of the clock generator for the proposed sub-sampler. The first block is common to both paths. It is used for setting the global phase of the whole clock generator in order to sample the signal at the correct instant. The clock generator is divided into in-phase and quadrature-phase paths to tune the parameters independently. A feedback loop allows duty cycle adjustment. The adjustment is performed according to the duty-cycle controller that monitors the clock quality on the leafs of the clock tree. The delay between I and Q is fine-tuned based on the error rate detected by the baseband processor. Finally, coupled inverters perform the single-ended to differential conversion and feed the pattern generator. The latter creates the correct pulses for the sub-sampler.

F. Frequency Planning of a Complete 60 GHz Receiver

The 802.15.3c standard defines four different channels [1]. Therefore, four distinct LO frequencies are needed to be able to down-convert any of these channels to the fixed IF.

Table III shows the channel center frequencies, the corresponding local oscillator frequency for a fixed IF and the ratio between this LO frequency and an 80 MHz reference frequency of the PLL. Only integer multiples of 80 MHz are needed for the LO frequencies. Moreover, the sub-sampling frequency (7.04 GHz) which is the input clock frequency of the proposed architecture is also an integer multiple (88 times) of the 80 MHz reference.

TABLE III
DIVIDER RATIOS OF THE PLL FOR EACH RF CHANNEL

RF Channel	Center Frequency (GHz)	LO Frequency (GHz)	$N = \frac{LO_{freq}}{80MHz}$
1	58.32	37.20	465
2	60.48	39.36	492
3	62.64	41.52	519
4	64.80	43.68	546

Due to the architecture of the PLLs, the phase noise power at the output goes up by N^2 [13], where N is the ratio between the reference frequency and the output frequency. In the proposed architecture, the reference frequency for the PLL could be 80 MHz, which is higher than the 36 MHz reference frequency used in [2] or [4].

The proposed 80 MHz reference frequency avoids using fractional dividers that could increase the effective phase noise [14]. This is interesting for the proposed architecture because the phase noise of the sampling clock contributes directly to the noise on the output.

IV. System Performance

A. Reference Architecture

For this study, the front-end published in [2] is taken as a reference for the characteristics of the RF front-end blocks: low noise amplifier, mixer and IF amplifier. The gain of the frontend is 24 dB and it has a 5 dB noise factor. Modulation is single carrier block transmission with QPSK constellation. In this mode, the minimum input signal power at the antenna is -53.9 dBm. Therefore, the minimum signal power at the transconductance input node is -30 dBm.

B. Dynamic Range

The signal transfer function is function of $1/C_s$ thanks to the integration. Most of the noise contributions are also functions of the sampling capacitor value. A simplified model of each component is used for calculating the noise contributions. As represented in Fig. 12, the antenna is modeled as a simple kT

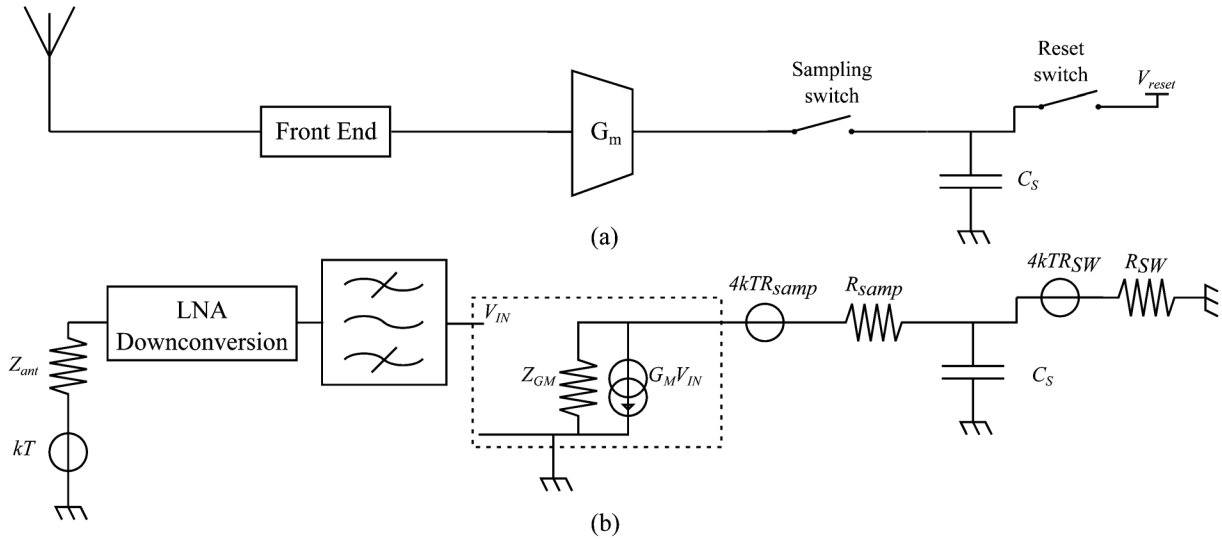


Fig. 12. Simplified chain of the receiver (a) and its equivalent model used for the noise analysis (b).

noise source and its corresponding impedance. The low noise amplifier and the mixer are considered as bandpass filters. Both sampling and reset switches are modeled as noisy resistors. The noise factor of the transconductance stage is not considered because of the very high gain of the low noise amplifier. The global noise factor considered is 5 dB, corresponding roughly to the noise factor of the LNA. The reset switch provides the well known sampling noise:

$$Pnoise_{RST} = \frac{kT}{C_s} \tag{14}$$

The sampling switch provides a less important noise contribution thanks to the output impedance of the transconductance stage:

$$Pnoise_{SAMP} = \frac{kT}{C_s}\frac{R_{samp}}{R_{samp}+R_{sw}} \tag{15}$$

The contribution of the thermal noise coming from the antenna consists in the integration of a thermal noise kT at -174 dBm/Hz over the effective bandwidth of the receiver. The antenna, the low noise amplifier and the mixer are all modeled in Matlab as ideal bandpass filters around the total bandwidth of the standard. As explained in Section II-C, the integrator and the FIR function add a contribution to the global transfer function. This contribution is considered by modeling the integrator in Matlab. The output noise contribution of the antenna is the result of the integration of the thermal noise shaped by the full system.

$$Pnoise_{ANT} = -293 + 10 \cdot log\left(\frac{G_m}{C_s}\right)^2 \tag{16}$$

The total output noise is the sum of these three major contributions (17).

$$Pnoise = Pnoise_{ANT} + Pnoise_{SAMP} + Pnoise_{RST} \tag{17}$$

Fig. 13 shows the total noise power as a function of the sampling capacitor. Output signal power is considered as the voltage

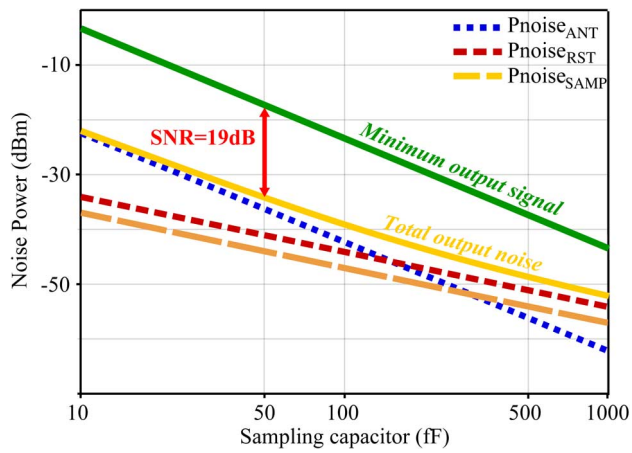


Fig. 13. Noise contributions as a function of the sampling capacitor.

of the sampling capacitor across a 50 Ω resistor. For these calculations, the output impedance of the transconductor was set to 2 kΩ and the sampling switch resistance is 2 kΩ. As a result, the signal-to-noise ratio is improved for low values of the sampling capacitor, and is obviously limited by the signal-to-noise ratio at the antenna.

For a sampling capacitor higher than 50 fF, noise contributions from switches become dominant, compared to input noise. Smaller values of the capacitor do not increase theoretical performance. However, reducing the value of the capacitor will increase sensitivity to parasitic capacitances and matching. Therefore, with a chosen value of 10 mS for the transconductance, a capacitor value of 50 fF seems to be a good trade-off. With these conditions, SNR is about 19 dB.

A system-level simulation of the bit error rate (BER) for given intput powers is presented in Fig. 14. The simulation includes the folded noise from the antenna and the noise contribution due to the sampling switch. The BER is below 10^{-12} for -54 dBm input power. Consequently, the input power can be reduced while keeping an acceptable BER. The sensitivity of the receiver is defined in [1] as the ability to receive a signal

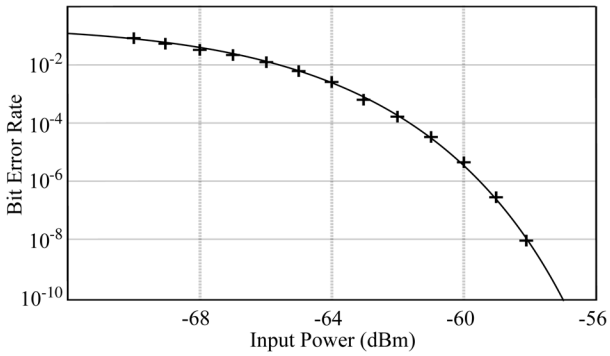


Fig. 14. Resulting bit error rate for a given input power at system level.

with a BER bellow 10^{-6} before corrections. Regarding Fig. 14, the sensitivity of the proposed architecture is -59 dBm. This result shows how the folded noise affects the sensitivity.

C. Effects of Sampling Jitter

The integration window is directly derived from the sampling clock. Hence the clock phase noise directly influences the phase of the demodulated data. Clock jitter is often a critical issue in sampling systems. The reference clock should be clean enough in order to limit its influence on the output SNR. Methods for jitter compensation have been recently described in [15]. However, a high resolution ADC is required which would translate in very high power consumption. Consequently, the sampling clock should be clean enough without any additional processing.

Reference [16] gives a relation between the RMS jitter and the output SNR for the voltage sampling. In the charge domain, the sampling operation considering jitter is modeled as follows:

$$V_{OUT} = \int_{a+\delta_0}^{a+T_i+\delta_1} V(t)dt \tag{18}$$

where $V(t)$ is the input IQ signal defined in (9), a is the sampling instant, T_i is the ideal sampling window, δ_0 and δ_1 are random variables representing the jitter of the sampling clock. I and Q are considered constant in the integration periods. This previous equation is divided in two parts which are the ideal integration window between a and $a + T_i$ called $V_{OUT-signal}$ and the noise contribution $V_{OUT-noise}$. Considering sampling in the In-Phase path, the ideal value is given for the sampling instant: $a = 0$. The standard deviation around the ideal sampling instant is considered short regarding the period of the input signal. Therefore, the following assumptions can be made on the input signal:

$$cos(2\pi f_{IF}\delta) = 1 \tag{19}$$

$$sin(2\pi f_{IF}\delta) = 0 + 2\pi f_{IF}\delta \tag{20}$$

Consequently, the result of the ideal integration is:

$$V_{OUT-signal} = \frac{-2 \cdot I}{2\pi f_{IF}} \tag{21}$$

where I is the in-phase data. The noise contribution is: With this consideration, the noise contribution of the output signal is:

$$V_{OUT-noise} = Q \cdot (-\delta_0 + \delta_1) \tag{22}$$

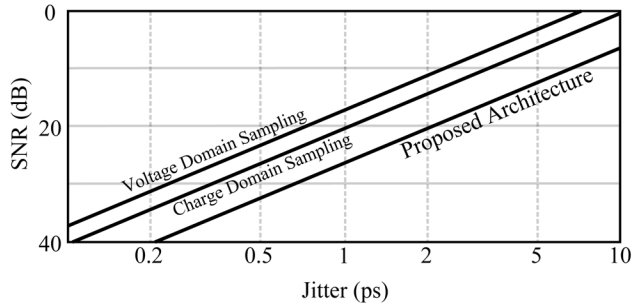


Fig. 15. Resulting SNR for the sampling of an IQ signal with a jitter on the sampling instant.

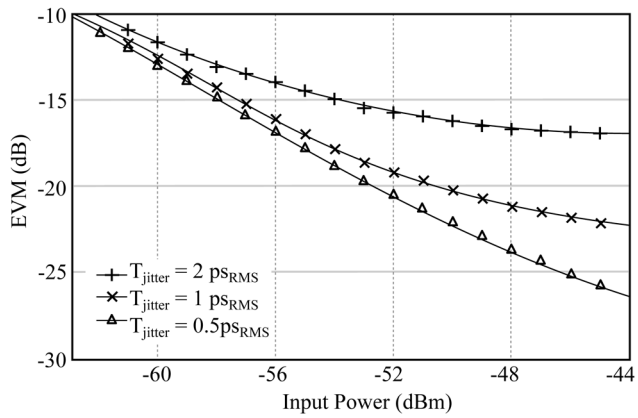


Fig. 16. EVM versus input power for several values of sampling clock jitter.

where Q is the quadrature data. Finally, the SNR for one sample taken in voltage domain is given by

$$SNR_{1-sample} = 20\log\left|2\pi f_{IF} \cdot \frac{(\delta_0 + \delta_1)}{2}\right| \tag{23}$$

The advantage of charge domain sampling with respect to voltage domain sampling is shown in (23) and in Fig. 15: the SNR resulting from the sampling instant jitter is reduced by $\sqrt{2}$ with an averaging of two random values. The proposed architecture has the advantage to take four successive values in charge domain. Consequently, the equivalent jitter contribution goes down by $\sqrt{8}$ in comparison to the voltage sampling technique.

$$SNR = 20\log\left(2\pi f_{IF}\frac{T_{jitter}}{\sqrt{8}}\right) \tag{24}$$

A system-level simulation has been performed in order to demonstrate the effect of uncertainty due to the sampling clock jitter. This simulation evaluates the error vector magnitude (EVM) as a function of the input power for several values of RMS jitter. The simulation includes the folded noise from the antenna, the noise contribution due to the sampling switch, the sampler with time uncertainty and the 4-coefficient FIR. The results are presented in Fig. 16. It shows that this jitter has a negligible effect at low input power as the noise is dominated by the folded thermal noise. Conversely, when the input power is high, the jitter effect is the most important contribution to the EVM. In order to keep the sensitivity of the receiver at -59 dBm, the RMS jitter should be below 1 ps.

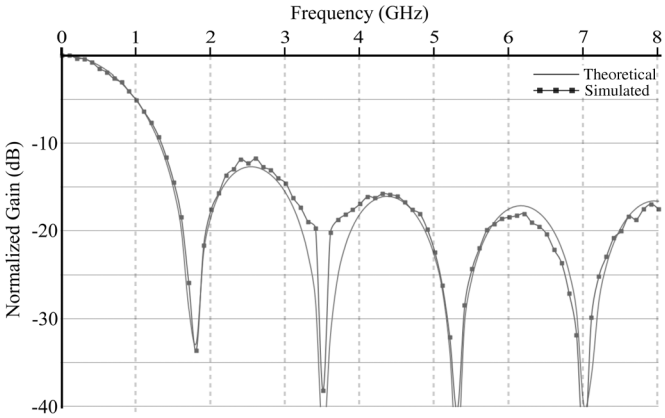


Fig. 17. Theoretical and simulated transfer function of the proposed architecture at transistor level.

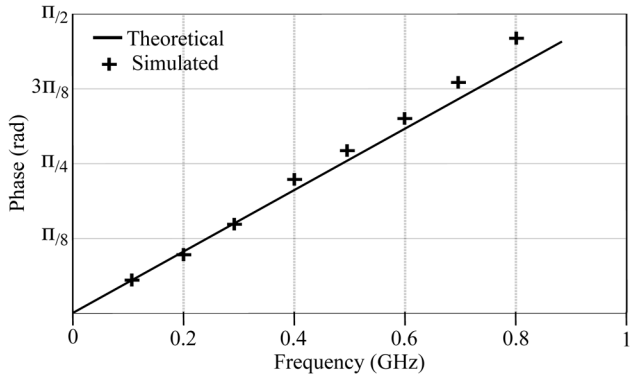


Fig. 18. Theoretical and simulated in-band phase response of the proposed architecture at transistor level.

Recent work on PLLs [17] has shown a low jitter oscillator with output frequency between 5.8 GHz and 8 GHz. Considering the phase noise given in [17] and a withe noise at -140 dBc/Hz between 40 MHz and $2 \cdot f_{SUB}$, the total RMS jitter complies with the previous requirement.

D. Transistor-Level Simulation Results

To check the feasibility of such an architecture in an advanced CMOS process, the most critical section, i.e. the switched capacitor section implementing the sampler and FIR filter, has been designed and simulated at transistor level with other sections implemented as ideal circuit elements. Transistor models for a 28 nm CMOS process [19] with high-K gate oxide and oxide thickness of respectively 1.4 nm and 1.7 nm for N-MOS and P-MOS transistors have been used. The process achieves a maximum ft of 300 GHz, minimum threshold voltages are 220 mV and maximum supply voltage is 1 V. Simulations include the pattern generator, the transconductances, the switches, the sampling capacitors, the differential amplifiers and the output analog-to-digital converters. The switch transistors are implemented as 1300 nm wide and 40 nm long PMOS transistors; each 47 fF sampling capacitor is a parallel connection of four 1500 nm wide and 350 nm long grounded NMOS transistors.

The transfer function of the system is obtained by sweeping a single tone sine wave at the input from 21.12 GHz to 29.12 GHz in 80 steps. The corresponding output values are shown in Fig. 17 and compared to the theoretical transfer function.

The simulation results and the theoretical values show the same behavior for the global shape and for the notches. The discrepancies between the simulated and the theoretical values are due to effects that have not been considered in the theoretical analysis such as capacitive coupling between signal lines, switch on-resistance and the charge injection of the switches.

The phase response of the channel bandwidth is shown in Fig. 18. The simulated phase response is close to the value predicted by theory.

The result of this transistor-level simulations shows that the system is possibly implementable in an advanced CMOS technology.

TABLE IV
ESTIMATED POWER CONSUMPTION OF A FULL 60 GHZ RECEIVER INCLUDING THE PROPOSED ARCHITECTURE

	Power Consumption (mW)
Front End RF to IF + RF PLL from [2]	74 + 80
Transconductances (estimated from [18])	14
Low jitter reference clock [17]	36
Channel Filtering & anti-aliasing filter	Included in the sampler
Total	204

E. Power Consumption

The power consumption of a complete 60 GHz receiver based on the proposed approach is estimated in Table IV. This estimation uses the power consumption of the front end and the RF PLL presented in [2]. [18] describes a 10 mS transconductance with 7 mW power consumption. Given that two transconductances are needed in this architecture, the total power consumption for the transconductances is estimated to be 14 mW. Furthermore, the PLL described in [17] complies with the requirements for this receiver architecture and is taken as a power estimate. With these front end considerations, the estimated power consumption is 204 mW for a receiver from RF to analog baseband excluding clock management and distribution. Each control parameter of this architecture can be further adjusted by automatic tuning schemes, such as the one presented in [20] for a reasonable additional power (8 mW for the adaptive equalization in the given reference).

Table V compares the proposed solution with the state-of-the-art 60 GHz solutions. A silicon implementation of the proposed architecture would have the advantage to include channel filtering at no extra power consumption. However, the proposed architecture would have a lower conversion gain than [2] (which affects sensitivity), but this could be counteracted by increasing the G_m value at the expense of a small increase of the power consumption. Regarding a direct-conversion receiver [4], the proposed architecture would offer a better conversion gain and would add channel filtering. Regarding a complete Si-Ge solution [3], the conversion gain would be lower but the channel rejection is equivalent for alternate channel and 2 dB lower for adjacent channels while the power consumption would be lower.

TABLE V
COMPARISON OF THE ESTIMATED PERFORMANCE OF THE PROPOSED ARCHITECTURE TO EXISTING 60 GHZ RECEIVER IMPLEMENTATIONS

	Proposed Arch.	**[2]**	**[3]**	**[4]**
Topology	RF to IF [2] + IF to DC Sub-sampling	Heterodyne	Heterodyne	Direct Conversion
Conversion Gain (dB)	36	32 to 41	69 to 70	4.7 to 17.3
Noise Factor (dB)	5	8 to 11	4.9 to 6.7	8
Channel Compatibility	all 4	all 4	all 4	CH1 & CH2
Modulation Scheme	SC QPSK	OFDM 16QAM	SC OOK, BPSK and MSK	SC BPSK to 16QAM
Filtering of Channels	FIR + Sampler	GmC in ABB	Active IF filters	No Filters
Adjacent Ch. Rejection (dBc)	15.7	N/A	18	N/A
Alternate Ch. Rejection (dBc)	23 to 30	N/A	more than 25	N/A
Technology	Simulations Only	65nm CMOS	SiGe BiCMOS 120nm	65nm CMOS
Power Cons. (mW)	204 (estimated)	454	573	172

This table shows that an IC implementation of the proposed solution included in a complete 60 GHz receiver could be competitive to the state of the art.

V. CONCLUSION

This paper presents a charge domain sub-sampling architecture for 60 GHz receivers, targeted at low power consumption. It includes down-conversion, IQ demodulation, and baseband filtering at minimal hardware costs. The charge sampler contributes to anti-alias filtering of the receiver allowing a sampling frequency of only 7.04 GHz. Regarding [2], the proposed architecture shows that it is possible to add the channel filtering for no extra cost in terms of power consumption. The system simulation shows that the system is suitable for implementation in an advanced CMOS technology. Future implementations would include an on-chip baseband processor in order to control all the settings of the system and could be integrated in a 802.15.3c single chip complete receiver.

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A Multi-path Multi-rate CMOS Polar DPA for Wideband Multi-standard RF Transmitters

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***Abstract*—A two-path digital power amplifier (DPA) in 1.2V 65nm CMOS is presented. This highly reconfigurable and frequency agile block is designed to be used as an envelope modulator in a wideband multi-standard polar transmitter. Each path is composed of a 12-bit DPA ensuring the modulation of the envelope of the RF signal. The DPAs are controlled by envelope code words (ECW) at different sample rates. This diversity strongly attenuates the images produced by the direct digital to RF conversion, avoiding passive filtering. The baseband sample rate conversion can easily be reconfigured. The proposed front-end can manage spurious emissions depending on the standard, the carrier frequency and the required power. The DPAs also integrate active input impedance compensation cells in order to limit the input impedance modulation when switching the DPA cells. The two-path DPA covers a 0.9-1.9 GHz bandwidth with 16.7dBm output 1dB compression point and 12.4% PAE. 64-QAM presents -28dB EVM while active area occupies 1x0.25mm^2.**

Keywords*—Multi-path, multi-rate, multi-standard, digital power amplifier (DPA), polar transmitter, software-defined radio (SDR), Lagrange interpolation, Cognitive Radio (CR).

I. Introduction

Front-ends of hand-held devices need to deal with several generations of standards like GSM/EDGE or UMTS, and new standards such as Long Term Evolution and WiMAX. Which tend to improve the spectral efficiency, but also introduce tough specifications. The Cognitive Radio (CR) approach is able to sense its environment and detect the spectral areas offering better communication efficiency. Then, the user's experience could be greatly improved if the front-end was able to reconfigure itself in order to take advantage of unused bands by switching from one standard to another, depending on usage. The traditional implementation of multi-standard front-end requires the use of several transmitters and power amplifiers designed for a single band [1]. Disadvantages are the lack of configurability and the cost and area increase with the number of frequencies to address. All-digital transmitters are good candidates for multi-standard and reconfigurable front-ends. The digital-to-RF conversion (DRFC) [2] and the digital power amplifier (DPA) architecture [3] [4] are two promising approaches extending the digital processing up to the antenna. However, the direct baseband digital signal to RF conversion suffers from the lack of anti-aliasing filters and leakage between the digital and RF blocks. The images are up-converted by the RF carrier and are located at multiples of the baseband sample rate and can violate the emission mask at many points. A straightforward solution would be to use a baseband signal sampled with high oversampling ratio (OSR), in order to shift the images out of the system bandwidth. This solution is easy to implement for narrow-band systems (around 500MHz), but becomes infeasible for wideband systems (e.g: 0.8-3GHz) in which the baseband signal needs to be sampled at a rate close to the carrier frequency. Besides the battery life aspect, the design of converters with such sample rates is highly constraining. The circuit presented in this paper introduces a multi-path multi-rate approach. The idea is to split the strong images into smaller ones [5] in order to meet the spurious emission level, as shown in Fig.1. The paper is organized as follows. First, the principle of the multi-rate approach will be explained in Section II. Then, the on-chip DPA and compensation cells will be detailed in Section III. Section IV will details the implemented system. Finally, Section V will present the measurement results obtained with the prototype.

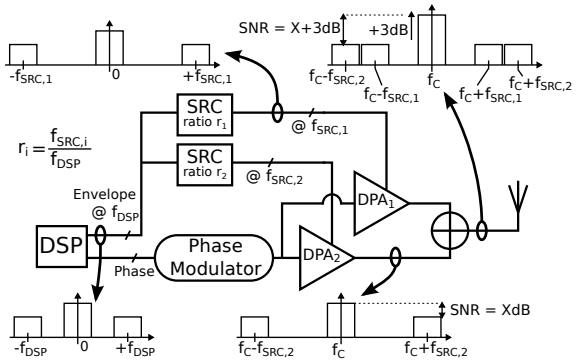

Fig. 1. Proposed polar multi-path multi-rate architecture

II. Multi-rate Architecture

Multi-path PA with power recombination, such as transformer-based combiner [6], have been used in advanced CMOS processes, due to the limited voltage supply and the need for high output power. The proposed architecture takes advantage of the multi-path approach and the high digital processing density of advanced technologies.

A. Multi-path approach principle

The images produced by the direct digital to RF conversion are related to the sample rate. In the architecture of Fig.1, each path comprises a sample rate converter (SRC) with a specific conversion ratio r_i. If all the conversion ratios are different, the images are not located at the same frequencies. Then, the images do not recombine while the fundamentals do. Fig.1 shows a 2-path polar architecture

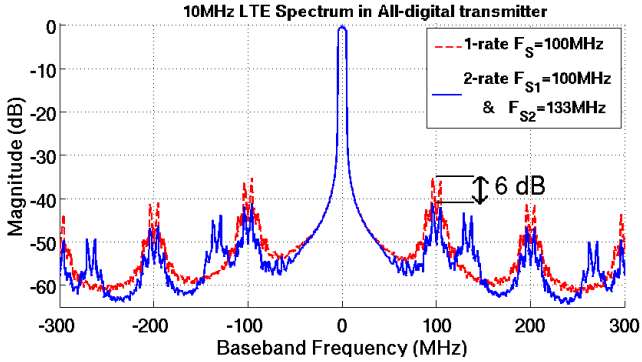

Fig. 2. Comparison standard all-digital Tx vs 2-rate architecture

with different sample rates. The fundamentals recombine at f_C, resulting in a 3dB gain at the transmitter output. On the contrary, the images keep the same magnitude. So, in a 2-path architecture, the SNR defined as the ratio between the fundamental and images is increased by 3dB, which is similar to an attenuation of 3dB of the images compared to a 1-rate transmitter. Finally, an architecture with N different sample rates will attenuate the images by:

$$Att(N) = 10 * \log(N) \quad (1)$$

B. Polar transmitter and impedance mismatch

Two additional aspects can help increase the images attenuation. First, polar transmitters perform different processes on the envelope and phase signals. The recombination of the filtered phase and envelope results in attenuated and distorted images as explained in [7]. This effect is represented in Fig.2 where a 2-rate polar system spectrum beside a standard 1-rate polar transmitter are shown. The second effect impacting the image attenuation comes from the impedance mismatch at the power combiner. In fact, the power combiner is designed to present the optimum impedance to all the RF modulators at the fundamental. But, the impedance presented to the RF modulators at image frequencies differs from the optimum. If only one path generates an image at one frequency, then the power combiner configuration can be approximated at this frequency as one active path while other paths are loaded by the output impedance of the RF modulators. In this case, the impedance presented to the power stage of the RF modulator is different from the optimum. Then, the power delivered to the power combiner is lower than the optimum case. In addition, the power is split between the antenna port and the other ports. To summarize, the total images attenuation depends on the number of images at the same frequency, the impedance mismatch and the power lost in inactive paths. Taking into account these three effects leads to the general approximation given in (2).

$$Att(N,K) = 10 * \log\left(\frac{P_{ANT}}{P_{ANTopt}}\right) = 20 * \log\left(\frac{K}{N}\right) \quad (2)$$

With N the total number of paths, and K the number of paths with images at the same frequency. Table I lists the total attenuation of images depending on N and K.

TABLE I. TOTAL IMAGES ATTENUATION

N\K	1	2	3	4	5	6
1	0					
2	-6.0	0				
3	-9.5	-3.5	0			
4	-12.0	-6.0	-2.5	0		
5	-14.0	-8.0	-4.4	-1.9	0	
6	-15.6	-9.5	-6.0	-3.5	-1.6	0

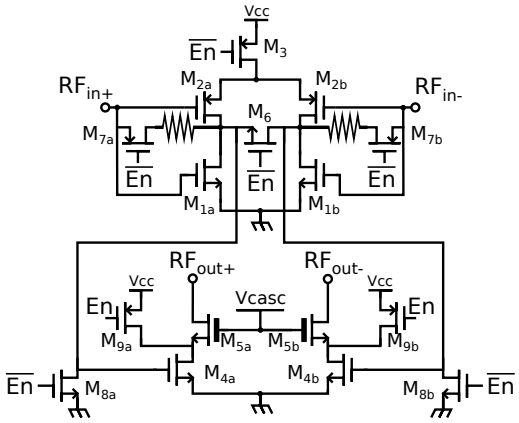

Fig. 3. Two-stage unit-amplifier cell

III. DIGITAL POWER AMPLIFIER

A dual DPA has been implemented in a 65nm CMOS process to cover a large frequency band and to support data rates up to 160Ms/s for the digital input. Architecture simulations show that a 12-bit resolution leaves enough margin for handling different modulation schemes, such as LTE, WCDMA or OFDM WLAN. The DPAs are implemented in a segmented form. The 4 LSBs drive a binary weighted matrix while the 8 MSBs control a 256 unit cells matrix. Fig.3 shows the schematic of a two-stage unit amplifier cell (UC) based on [4]. The first stage is a self-biased complementary common-source amplifier directly coupled to the output stage. This last stage is a Class-A amplifier with thick oxide cascode transistors which allow increasing the output swing to 4V. When the cell is ON, M_3 supplies the first stage and $M_{7a;b}$ allow self-biasing. Otherwise, when the cell is OFF, M_6 & $M_{8a;b}$ tie the last stage input to the ground while $M_{9a;b}$ reduce the leakage current and limit source voltage swing of the cascode transistors. The input impedance presented by a DPA is set by the input impedances of the UCs in parallel, and can be approximated by $Z_{IN} = (N_{ON} * Y_{ON} + N_{OFF} * Y_{OFF})^{-1}$, in which $\{N_{ON};\ N_{OFF}\}$ and $\{Y_{ON};Y_{OFF}\}$ represent the number of cells and the admittance presented by a UC in ON and OFF states. As explained in [4], the input differential capacitance can be supposed constant and equal to $C_{in} = N_{cell} * (C_{gs1a;b} + C_{gs2a;b})/2$. However, the switching of the self-biasing path introduces significant variations of the resistive input impedance. In order to limit the resulting signal distortions, a special compensation cell (CC) has been added to the DPA input. A CC is added every two columns of the MSB matrix and is controlled by the column activation signal as can

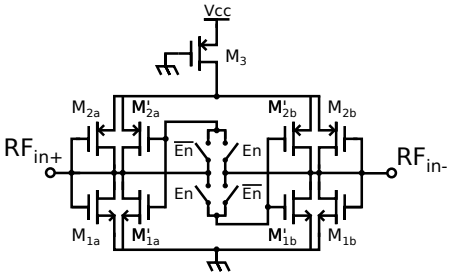

Fig. 4. Compensation cell

TABLE II. COMPENSATION CELL INPUT IMPEDANCES

State	Differential Mode	Common Mode
ON	$(2 * g_{ds1} + 2 * g_{ds2})^{-1}$	$(2 * g_{m1} + 2 * g_{m2})^{-1}$
OFF	$(2 * g_{m1} + 2 * g_{m2})^{-1}$	$(2 * g_{m1} + 2 * g_{m2})^{-1}$

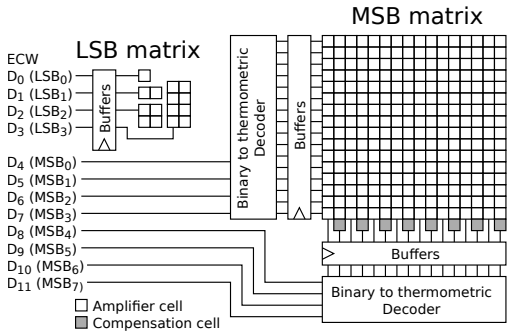

Fig. 5. DPA with Compensation cells

be seen in the DPA floorplan in Fig.5. One additional compensation cell is enabled for every 512 ECW step. Fig.4 shows the schematic of the compensation cell, which is matched to the input stage of the elementary amplifier cell. It is composed of two branches, $M_{1a;b}$ and $M_{2a;b}$ define the main branch, $M'_{1a;b}$ and $M'_{2a;b}$ the auxiliary branch. When the cell is enabled, the branches are in cross-coupled configuration. In differential mode (DM) , the transconductances $g_{m1a;b}$ and $g_{m2a;b}$ are cancelled by $g'_{m1a;b}$ and $g'_{m2a;b}$ while adding in common mode (CM) . On the contrary, in the off-state, branches are in parallel in both DM and CM. The resulting impedances presented between RF_{in+} and RF_{in-} are listed in Table II. Fig.5 shows the LSB and MSB matrix of the DPA with compensation cells beside the columns and rows controllers. Their differential resistive impedance variation is inversely proportional to the envelope code word, which compensates the one induced by the UC switching. Fig.6 shows the resistive input impedance variations as a function of the ECW. When no compensation cell is present, the input impedance strongly varies from $8K\Omega$ down to 32Ω. Adding the CC limits the impedance variation to less than 10Ω. The resistive impedance is always comprised between 27Ω and 38Ω. Furthermore, the CC have low CM impedance which stabilizes the DPA.

IV. Implemented System

In order to demonstrate the images attenuation in a multi-rate architecture, a 2-path digital polar PA was implemented in a 65nm CMOS process from ST Microelectronics. The die micrograph is represented on Fig.7. The circuit is pad limited. Thus, the 12-bit ECWs are serialized in a double data rate format on 3 bits in order to limit the number of pads dedicated to digital control, the resulting data clock speed is two times the sample rates and goes up to 320MHz. 20 pads are dedicated to power supplies, 10 to RF signals and 10 to digital signals. The active area occupies 0.25mm^2. The overall prototype setup is shown in Fig.8. Each symbol is separated into envelope and phase components. The phase signal modulates the carrier frequency thanks to a vector signal generator. The envelope signal is interpolated by an FPGA to two new signals at sample rates f_{S1} and f_{S2}. The SRC are based on highly reconfigurable Lagrange interpolators. Input and output impedance matching is performed on-board while single-ended to differential conversion and power combination are done with external components.

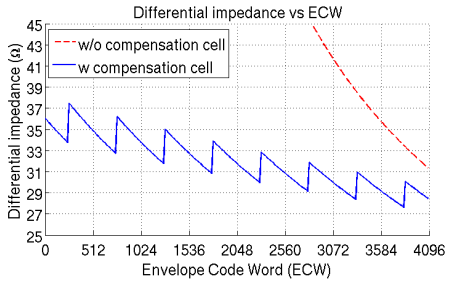

Fig. 6. Compensation cells impact on input impedance

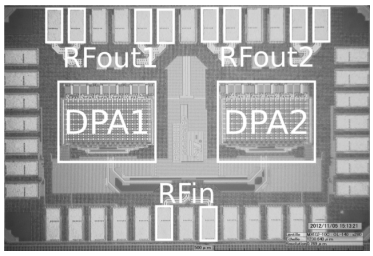

Fig. 7. Die micrograph

V. Measurements Results

Fig.9 shows the power characteristic of the amplifier when all the cells are enabled. Fig.12 represents the 1dB compression point output power and PAE over frequency after de-embedding of the on-board matching network and off-board power combiner for a one-tone signal, when both paths are enabled and set to the maximum ECW. The maximum output power is obtained at 1.1GHz and is equal to 16.7dBm with a maximum PAE of 12.4%. The circuit draws 130.2mA from the 2.5V supply and 39.3mA from the 1.2V supply. The logic interfaces and matrix buffers draw less than 5mA from the 1.2V supply. The amplifier was designed to cover a frequency band from 0.8 to 3GHz. However, the useful frequency range is limited by the on-board matching network to 0.9-1.9GHz. Fig.10 and 11 show the spectra for 10 MHz LTE channels when different couples of sample rates are chosen. The

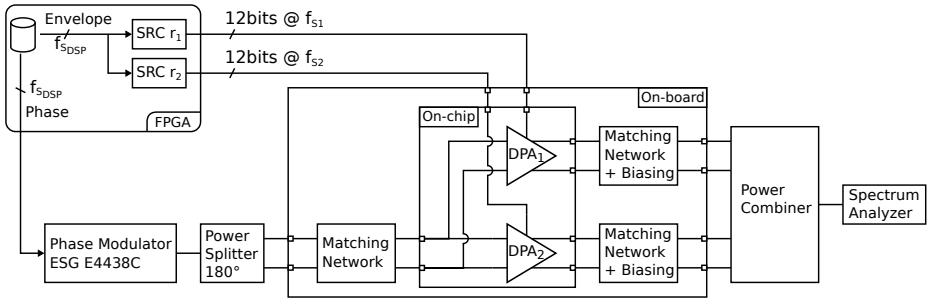

Fig. 8. Implemented System

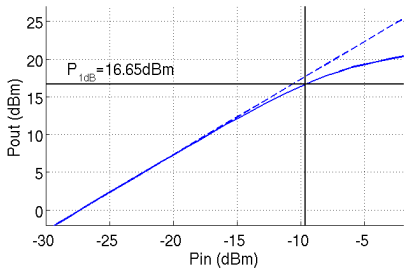

Fig. 9. P_{out} vs P_{in} for a 1.1GHz sine wave with full ECW

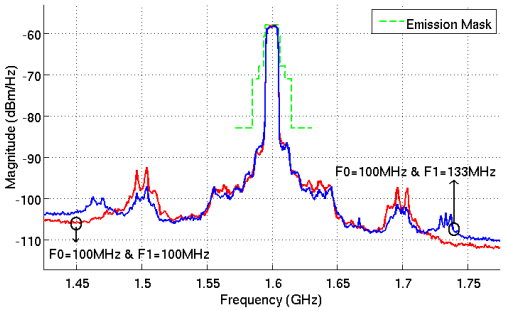

Fig. 10. Comparison between 1-rate and 2-rate spectrum

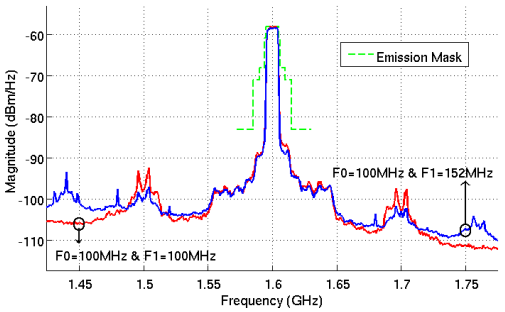

Fig. 11. Comparison between 1-rate and 2-rate spectrum

images are effectively reduced by 6 dB with the 2-path approach, and can be placed at arbitrary frequency offsets from the carrier. A -28dB EVM was measured for a 64-QAM modulation with a 10 MHz symbol rate and -10dBm input power corresponding to the input 1dB compression point, whatever the envelope sample rates.

VI. Conclusion

A wide-band digital polar amplifier based on a multi-path multi-rate approach has been demonstrated. The amplifier possesses two parallel DPAs controlled by two envelope signals with different reconfigurable sample rates. The amplifier delivers up to 16.7 dBm over a 0.9 - 1.9 GHz band while providing 12.4% PAE.

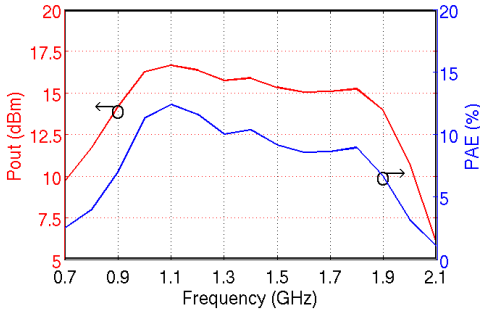

Fig. 12. P_{1dB} and PAE vs frequency

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I. Sourikopoulos, A. Frappé, A. Cathelin, L. Clavier, A. Kaiser, “A digital delay line with coarse/fine tuning through gate/body biasing in 28nm FDSOI”, Proceedings 42nd European Solid-State Circuits Conference, ESSCIRC 2016, Lausanne, Switzerland, September 12-15, 2016

A Digital Delay Line with Coarse/Fine tuning through Gate/Body biasing in 28nm FDSOI

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***Abstract*—This paper discusses the design and characterization of a programmable digital delay line. The core of the proposed architecture is a thyristor-type delay element featuring the capability for coarse/fine tuning without using any additional hardware. This is made possible by taking advantage of body biasing features available in 28nm FDSOI CMOS. Body biasing offers unique performance characteristics, notably a very low sensitivity to the biasing voltage. The prototype delay line was designed featuring thermometer-code multi-stage activation and gate/body biasing control. A delay range from 560ps to 16.13ns is exhibited for the delay line with a 2GS/s input stream. The unit delay cell exhibits fs/mV sensitivity combined with an order of magnitude larger delay dynamic range and an energy efficiency of only 12.5 fJ/event.**

Keywords—Delay element; FDSOI; body-biasing; digital delay line

I. INTRODUCTION

Delay controllability has always been the major concern for the reliable implementation of circuits whose purpose is timing. Depending on the application, the range and importance of accurately controlling a delay value differs. For instance, producing reliable timing signals usually comes along with employing elaborate delay-line systems in control-loop architectures.

One of the most proliferated techniques for building power-efficient, variable delay elements has been the thyristor-based [1]. It has received attention over the recent years [2], [3] due to its capability in producing wide-range delays with low power consumption. The work in [4] increased configurability by controlling extra capacitances and [5] proposed techniques to reduce sub-threshold leakage and transient shunt currents.

In another discussion, in [6], the implementation of a decision-feedback equalizer featuring continuous-time digital feedback has been suggested. The specification of such system calls for digital delays with: (i) fine granularity, in the order of picoseconds, to accommodate the GS/s throughputs for deployment of standards such as the 802.11ad and (ii) wide-range of configurability, in the order of nanoseconds, to meet the associated delay spreads. The delay line presented in this report is aimed for integration in such a system. The proposed granular delay element is based on a modification of the one in [7], which exhibits low power consumption in an advanced node. The work here extends functionality to provide fine-tuning through body biasing. Implemented in 28nm UTBB FDSOI (Ultra Thin Body and Buried oxide Fully Depleted Silicon Over Insulator) CMOS technology, the transistor's body terminal serves as a fine control knob which complements gate control. This way an unprecedented coarse/fine scheme is realized without any extra hardware.

The rest of the paper is organized as follows: In section II after a short technology introduction the granular delay element is presented by highlighting its tuning capabilities. In section III the prototype delay-line design is detailed. In section IV the focus turns to measurement results before concluding in section V.

II. DELAY ELEMENT DESIGN IN FDSOI

The proposed thyristor cell topology is displayed in Figure 1 and three stages can be readily distinguished. The first stage is a current-starved inverter, whose output (V_C) is connected to a second, gated, inverter stage. The second stage produces a feedback signal, V_F, which controls the transistors in parallel with the ones implementing current-starving. Finally, a driving stage, generates the complementary output signals.

The circuit follows the typical thyristor operation. As it has been extensively presented in bibliography, we summarize operation: As input V_{IN} rises, V_C slowly discharges up to the point where the second stage inverter threshold is crossed. Through V_F, the parallel transistor is then activated and this effectively shorts the "starving" mechanism. So, the discharge of V_C is accelerated thus completing the switch

The element's consumption profile is dominated by the current-starved (dis-)charging interval which produces short-

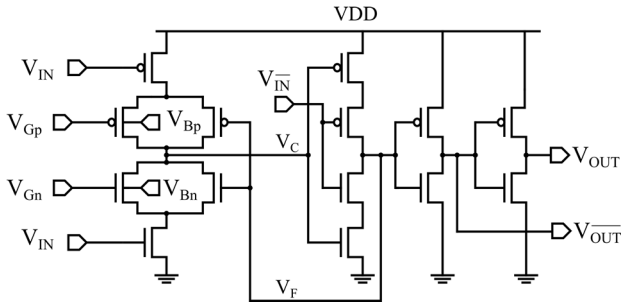

Fig. 1 Proposed thyristor-type delay element featuring second stage gating and body biasing.

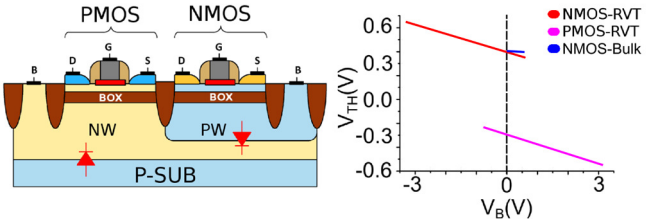

Fig. 2 FDSOI transistor cross-section (left) and threshold voltage (V_{TH}) variation with body biasing (V_B) for regular –Vt transistors (right).

-circuit currents during the slow switching of the second stage. In an attempt to minimize the latter, the cell is designed with complementary inputs ensuring that the $V_{\overline{IN}}$ signal *precedes* its complement. This is realized by cascading delay cells. Arriving directly on the second stage inverter, the input complement plays a preparatory role for the upcoming switch. When followed by V_{IN}, say in a high state, $V_{\overline{IN}}$ is already driven low shutting the path to the ground. This action enables the slow second stage output to be raised high without short-circuit current loss.

For the proposed delay element, substrate control is suggested for current-starving. This is made possible thanks to FDSOI technology. As seen in Figure 2 (right), the transistor channels are implemented with a buried oxide layer underneath, which prevents source-bulk junction leakage. This ensures a body-tie voltage range which is much wider than in bulk CMOS (Figure 2, left). Also, the body coefficient is much more important in FDSOI (85mV/V), than in the equivalent bulk node (40mV/V).

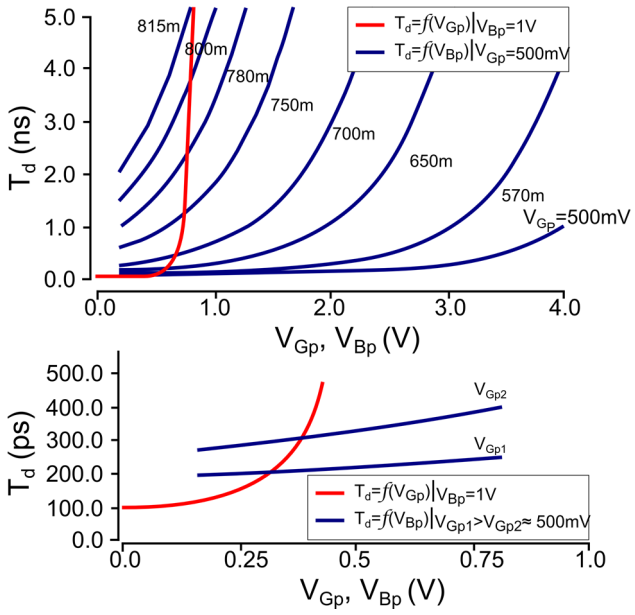

Fig. 3 Simulations of falling edge delay time. Red curves: varying the gate while keeping body constant. Blue curves: varying the body while keeping the gate constant. Curves are presented on same x-axis to illustrate the evolution of delay, but are not coincident as they refer to different biasing conditions.

Regarding control of the drain current, body biasing is principally of the same nature as gate biasing. However, the electric field is applied through a thicker oxide and a more distant contact. One could easily predict that the effect on current modulation would be less profound. This is exactly the key observation for establishing an extra control knob to fine-tune the delay element.

The transistors of the circuit are sized to produce delays in the order of picoseconds. In Figure 3, on the top, we simulate the *falling* edge delay variation, T_d, against the control inputs. The NMOS starving transistor biases are fixed to V_{Gn}=500mV for the gate, and V_{Bn}=0 for the body. The red curve refers to keeping the PMOS body as V_{Bp}=1V and varying V_{Gp}. It is a typical exponential variation with a steep ascent as current is starved under conduction threshold. In blue, we plot a family of curves which refer to fixed values of V_{Gp}={500mV, 570mV…} and vary V_{Bp}. The results confirm the above observation and reveal another important effect: careful combination of gate/body biasing can lead to obtaining a segment of the delay range that refers to an *almost linear* part of the curve. To elaborate this, we can assume a gate voltage in the vicinity of 500mV as seen in the bottom plot of Figure 3. For this setting, the delay versus the body bias variation provides a high correlation with a linear function, as well as a very fine tuning capability.

III. Prototype Delay Line Architecture

In an effort to fully investigate the topology and the control flexibility that body biasing offers, a prototype delay line was designed and fabricated. The regular-V_T transistors of the first stage current-starved inverter were laid out in twin and triple-well arrangements in order to ensure isolation. The imposed constraints of well spacing lead to an overall unit delay element area of 3 x 7 μm^2. The well arrangement is shown in Figure 4.

The delay line design involves a cascade of granular cells organized in groups, as seen in Figure 5-a. Group size was optimized based on the granular delay range in order to guarantee minimum overlap when programming a delay value. Each group is associated with a tap output to facilitate programmability. For this purpose, all tap output nodes are connected to a common bus. Control of the bus is carried out with an 11-bit thermometer-coded word that activates the selected output.

In order to minimize power consumption, a local power-down scheme is established for the delay groups that are

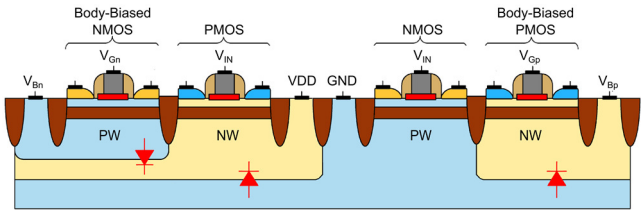

Fig. 4 Well arrangement layout accommodating the body biasing stage.

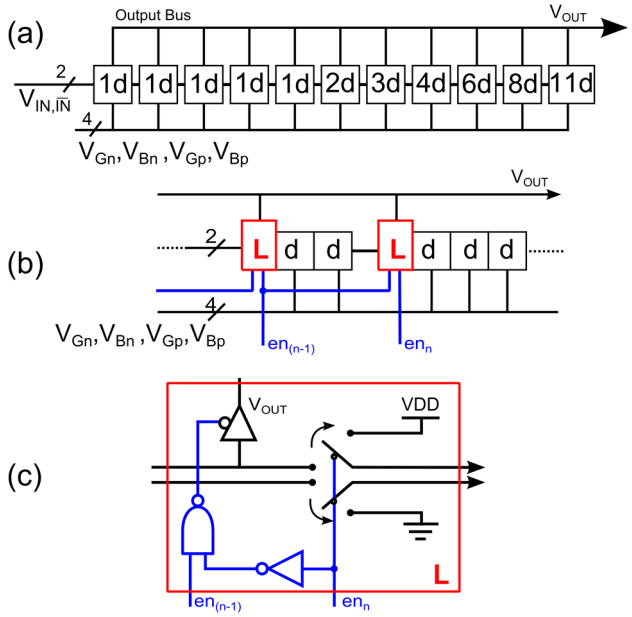

Fig. 5 (a) Delay line archtecture. (b) Inter-group transition and delay-line output is implemented with *Lead* cells . (c) *Lead* cell logic.

not active for a given delay value. This is realized through the use of *Lead* cells (indicated as *L* in Figure 5-b), which are placed between groups. Their function is to enable the output of the last active group and propagate a steady-state to the remaining ones. The logic is shown in Figure 5-c.

The prototype chip was fabricated in 28nm UTBB FDSOI CMOS technology by STMicroelectronics. The top level block diagram and chip photograph are shown in Figure 6.

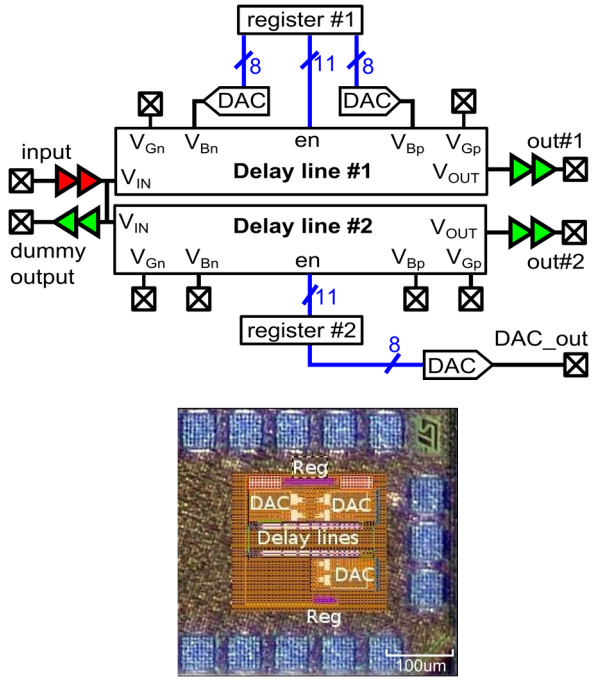

Fig. 6 On chip delay line testbench top level diagram (top) and chip photograph (bottom) with layout inset. Metal fill obscures metallization.

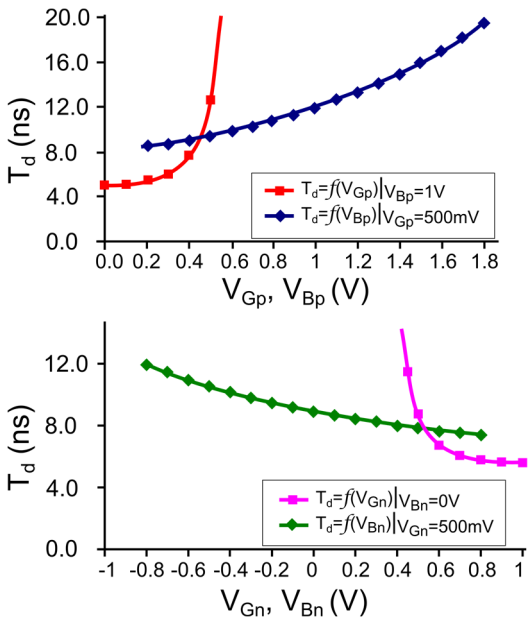

Fig. 7 Falling (top) and rising (bottom) edge delay measurements. The fine control character of body biasing is verified.

It comprises two delay lines: one with external analog control of body biasing and one with digital, through on-chip 8-bit R-string DACs. A dummy output was used to de-embed the delays coming from pad drivers and external routing. The delay lines were designed with independent power supplies to permit direct power consumption measurements. The delay line control words and on-chip DAC inputs were provided from custom on-chip control registers. In order to perform the measurements, a test-bench was built with the die being wire-bonded on a PCB. The on-chip control registers as well as on-board DACs used for generating gate and body bias signals were programmed though the USB port of a PC, using a serial programming interface.

IV. Measurement Results

The good functionality of the delay line under different control scenarios was verified. Various measurements of rising and falling edges were performed in different rates up to 2GHz. Figure 7 presents the variation of delay for a fully active line with body biasing applied over a range of 1.6V, both for rising and falling edges. The coarse/fine character is illustrated.

Another scenario entailed activating consecutively the delay groups to characterize the complete line programmability. Rising edge delay range is measured under fixed gate biasing: V_{Gn}=400mV, V_{Gp}=600mV. Keeping V_{Bp}=1V, this scenario involved activating stages incrementally and varying V_{Bn} body biasing between 0.2V and 1V. These are the limits between inter-well junction diode inversion and nominal supply. The delay versus the programming vector, up to activating all stages, is displayed in Figure 8.

The performance results are summarized in the second column of Table I. “Minimum coarse sensitivity” refers to the minimum variation of delay achievable with enabling only the

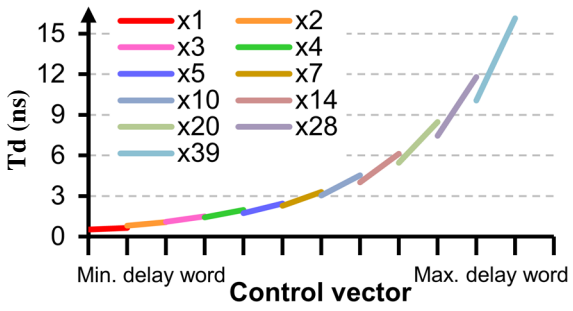

Fig. 8 Rising delay vs. control vector: 1-39 delay elements at minimum and maximum values of body bias. The curve shape reflects group sizing.

first group, while "minimum fine sensitivity" refers to varying body biasing at this setting. The "Maximum Delay" field refers to the general gate and body biasing extremes and verifies the known wide-spanning capabilities of a thyristor-type delay.

Moreover, granular delay characterization was pursued through multiple measurements of stage by stage activation to de-embed *lead* cells and output drivers. The results refer to a scenario of rising edge delays under V_{Gn}=V_{Bn}=500mV, V_{Gp}=0V and V_{Bp}=1V. The measured control sensitivity is 50fs/mV and energy efficiency 12.5 fJ/event. As delay range trades-off with sensitivity, even smaller sensitivity can be obtained if required by the application.

Comparison with the state of the art is done in Table II. The advanced FDSOI CMOS node and the unique body control scheme mitigate the use of extra hardware, such as current sinks, which impose a static consumption overhead. This way the lowest reported power consumption is achieved.

V. CONCLUSIONS

This report describes a delay line based on an FDSOI CMOS thyristor-type delay element. Power-savings are achieved through a complementary input scheme and body biasing is used for fine-tuning the output delay. A multi-stage delay line is fabricated featuring advanced programming flexibility and both rising and falling edge delay control. The measurement results confirm the precision control using the body terminal. This is achieved with no extra hardware cost as in comparable realizations. The capability of extending body biasing beyond the nominal supply voltage limit increases further the control range. With such fine-tuning and wide-controllability features, combined with a low-power consumption profile, the proposed design could readily serve in implementing precision timing functions.

TABLE I. PERFORMANCE SUMMARY

This work	Delay line	Granular delay
Nominal delay range (2GHz input)	530 ps –16.13 ns	110 ps – 500 ps
Min. coarse sensitivity	120 ps/mV	600 fs/mV
Min. fine sensitivity	150 fs/mV	50 fs/mV
Max. delay	170 ns	4.5 ns
Efficiency	668 fJ/bit	12.5 fJ/bit
Area	980 um^2	21um^2

TABLE II. DELAY ELEMENT STATE OF THE ART

Ref.	[5]	[3]	[7]	This work
Tech. Node	0.35um	90nm	65nm	28nm FDSOI
Supply	3.8V	1 V	1 V	1 V
Delay Range	4us-22ms	5ns -1µs	95ps-250ps	110 ps - 4.5 ns
Control	Current sink	Gate voltage	Current sink	Gate /Body (coarse/fine)
Minimum control sensitivity	100 kHz/µA (osc)	40ps/mV (est.)	N/A	<50 fs/mV
Power	<120 pJ/event	50fJ/event	40fJ/event	12.5 fJ/event

[7] reported consumption as per tap in a CT-DSP filter.

[5] reported a three-element oscillator consumption including a digital counter

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Digital Complex Delta–Sigma Modulators With Highly Configurable Notches for Multi-Standard Coexistence in Wireless Transmitters

Răzvan-Cristian Marin, *Student Member, IEEE*, Antoine Frappé, *Member, IEEE*, and Andreas Kaiser, *Senior Member, IEEE*

***Abstract*— This paper presents a complex delta–sigma modulator (CDSM) designed for integration in a digital transmitter chain targeting multi-standard coexistence with nearby receivers. The use of a DSM has the advantage of increased performance in terms of signal-to-noise-ratio in the band of interest. However, the resulting out-of-band noise becomes an issue for multi-standard coexistence, thus increasing the complexity of the subsequent filtering stage. This constraint could be relaxed in the DSM stage, by placing a complex zero near the frequency band, where a low noise level is needed. This is achieved by cross coupling the in-phase (I) and quadrature (Q) channels, thus obtaining a CDSM. A review of known design methods for CDSM revealed limitations regarding the poles/zeros optimization, and the configurability of the complex zeros placement. The proposed architecture introduces two additional cross couplings from the I and Q quantizers outputs in order to decorrelate the zeros placement and the poles optimization problem. Hence, the improved CDSM can be implemented using existing optimization tools, which reduces considerably the number of iterations and the computational effort. In addition, the resulting modulator can target different coexistence scenarios without the need of redesign, unlike other known methods. Simulation results show a noise level reduction of approximately 20–30-dB near specific frequency bands by the proposed CDSM scheme with respect to standard DSM. Finally, we show an efficient coarse/fine configurability mechanism, which is obtained when introducing additional delays in the cross-coupling paths.**

***Index Terms*— Delta sigma modulator (DSM), complex delta sigma modulator (CDSM), finite impulse response (FIR), multi-standard coexistence, digital transmitter.**

I. Introduction

RECENT progress in advanced CMOS integrated digital transmitter (TX) architectures [1], [2] has been focusing on reducing the power consumption and circuit area to follow the trend of increased data rates and signal bandwidths (*BW*) in communication standards, e.g. IEEE 802.11 standard.

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Furthermore, it is shown in [3] and [4] that low-complexity digital signal processing based on Delta-Sigma Modulators (DSM) can enable the use of highly-efficient power amplifier stages in a digital transmitter. Moreover, techniques such as time-interleaving (TI) [5] and multi-channel look-ahead [6] can be employed in order to overcome DSM integration challenges and increase the maximum operating frequency. As a result, it is shown in [6] that an FPGA implementation of a TI DSM-based all-digital transmitter can reach a maximum effective sampling frequency of 28 GHz and meet the transmit mask of IEEE 802.11a WLAN standard in the 5.2 GHz band.

However, there are still two important issues to be handled in digital transmitters, namely the image replicas and the out-of-band noise. First of all, image replicas can be seen very close to the signal when the sampling frequency (f_S) is not high enough. For instance, in [1], for a signal bandwidth of 154 MHz, image replicas will be very close, at ±300MHz from the center frequency (f_c).

Secondly, the out-of-band noise floor injected into a nearby receiver (RX) within another band can affect the coexistence of multiple radios on the same chip.

A. Out-of-Band Noise vs. Multi-Standard Coexistence

The most stringent noise specifications are found for the GPS band around 1575 MHz, due to the low typical power level of the GPS signal (~ -125 dBm). This issue has been highlighted in [2], where a noise floor of -130 dBm/Hz is measured in the GPS band when transmitting an 802.11g 54 Mbps signal on Channel 1 with a power of 16.35 dBm. In addition, the same noise requirements apply to the GLONASS (Global Navigation Satellite System) band around 1602 MHz (27 MHz away from GPS). Hence, the study of standard coexistence with GPS can be further extended to GLONASS.

In order to target advanced communication standards, [7] presents the design of a single-bit Delta-Sigma Modulator as part of a digital transmitter, focusing on time-interleaving to enable high-speed applications (up to 6 GS/s sample rate) and large signal bandwidths (up to 160 MHz).

A simple analysis regarding the two issues described before, shows that the performance of this DSM architecture is not affected by image replicas, thanks to the high sampling frequency. It is though affected by the out-of-band quantization

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noise, since the main function of the DSM is to reduce the in-band noise (increase SNR) by shaping it out-of-band. Hence, the amount of out-of-band quantization noise will determine the complexity of the succeeding filtering stage needed to meet stringent coexistence specifications with nearby receivers, in particular GPS/GLONASS.

One solution for the reduction of the out-of-band noise is to introduce analog filtering, which generally requires high-quality passive components in order to target one specific communication standard. For example, a 6-pole LC bandpass filter [8] with the center frequency $f_c = 2.4$ GHz and a bandwidth $BW = 300$ MHz can achieve an attenuation of around 40 dB around the GPS band.

However, for 1-bit high-speed DSMs, a FIR-DAC based mixed-signal stage, such as the one presented in [9], offers a good alternative to analog filters. Nevertheless, the designed filter requires a large number of signal taps, resulting in area and power consumption penalty due to the implementation of coefficient cells and control logic.

In this case, the digital filtering constraints could be further relaxed in the DSM stage, by placing complex zeros near the frequency bands, where low noise levels are needed, depending on the targeted application. Still, this assumes complex non-conjugated zeros, which lead to an asymmetric noise transfer function (NTF).

B. Known Implementation Methods of Asymmetric NTF

In order to obtain an asymmetric NTF, the In-phase (I) and Quadrature (Q) channels can be cross-coupled, resulting in a Complex Delta-Sigma Modulator (CDSM) as shown in [10], where a 5$^{\text{th}}$ order modulator is used to match both UMTS and DCS 1800 standards out-of-band spurious emissions.

The approach in [10] combines both linear algebra and control engineering theories in order to optimize the zeros and poles placement using the state matrix, whereas the modulator is assumed to be stable if i) all the zeros are placed on the unit circle (modulus equal 1) using additional integrator feedback coefficients, and ii) all the poles are inside the unit circle and equispaced on a smaller circle centered on $z_0 = 1$ and of constant radius $r_c < 1$.

Furthermore, [11] introduces an effective design tool used to synthesize the NTF for single-path and quadrature Delta-Sigma Modulators. For a quadrature configuration, the parameters considered for the optimization are the following: the order of the NTF, the oversampling ratio (OSR), the center frequency, the rms (root mean square) in-band noise gain, the rms image-band noise gain, and the number of image-band zeros. Thus, the design methodology is simplified by obtaining an optimum and stable architecture through an iterative process based on the requirements of the quadrature DSM. A detailed description of this tool and the associated functions can be found in [12].

However, both these methods introduce limitations regarding the design of CDSM. First of all, the approach in [10] is based on large computational effort in the optimization of poles and zeros, which makes it more difficult to apply to other communication scenarios. For example, for the 5$^{\text{th}}$ order CDSM, the characteristic polynomial has 18 different coefficients to be set, so that the five roots (poles) can meet the poles optimization relations.

Secondly, the method in [11] cannot be used to set zeros based on noise level requirements, because the zeros placement is limited to the image-band only, which is symmetric to the transmit band with respect to f_c.

In addition, complex transfer functions have been studied also for Sigma-Delta Modulator (SDM)-based ADCs, which can be used in the intermediate frequency (IF) stage of a receiver (RX). Reference [13] presents a 2$^{\text{nd}}$ order single-bit Complex SDM (CSDM) ADC to be used in a very low IF RX path in GSM/ GPRS/ EDGE phone applications for improved noise shaping (complex NTF), whereas only one integrator stage is complex. The coefficients of the architecture were obtained with a DSM specific design tool, because the custom complex zero is placed extremely close to the signal band ($z = -0.02j$), and has very little impact on the poles position.

Moreover, in [14] the SDM design concentrates on complex signal transfer functions (STF) with good stop-band attenuation, in order to reduce the image-band noise aliasing into the signal band. The algorithm is iterative and application-dependent, assuming the initial loss-pole (transmission zeros) placement derived in [15] and a minimum NTF magnitude at $\omega = \pi/OSR$.

Finally, [16] aims to reduce coefficients mismatch between the I and Q paths in a multi-bit CSDM. The method consists in adding feedback paths from the inputs and outputs of the CSDM to all the integrators inputs, which allows coefficients mismatch compensation (in digital domain) based on a matrix representation of mismatched complex operations.

The present paper details the simplification of the design method for digital CDSM architectures, using additional cross-couplings in order to cancel the complex coefficients in the characteristic polynomial. This allows the decorrelation of the poles optimization and the zeros placement, thus eliminating the aforementioned limitations, concerning the position of the zero, the high computational effort and the lack of configurability. The modified architecture can be obtained using automatic tools with flexible custom zeros placement, for optimized out-of-band noise performances.

Section II presents the model of a 1$^{\text{st}}$ order CDSM, as well as the proposed modified 1$^{\text{st}}$ order architecture, which is extended to a general approach for the design of higher order CDSM in Section III. Next, Section IV shows the flexibility of the CDSM scheme as part of a digital transmitter for multi-standard coexistence. Finally, Section V demonstrates a coarse/fine control mechanism with reduced overhead, thanks to additional delays introduced in the cross-coupling paths.

II. Complex Delta Sigma Modulator Model

A. General Architecture of 1st Order CDSM

A 1$^{\text{st}}$ order Complex Delta-Sigma Modulator is generally obtained from two standard 1$^{\text{st}}$ order DSMs in quadrature, by cross-coupling the I and Q paths in order to implement an asymmetric noise transfer function (Fig. 1).

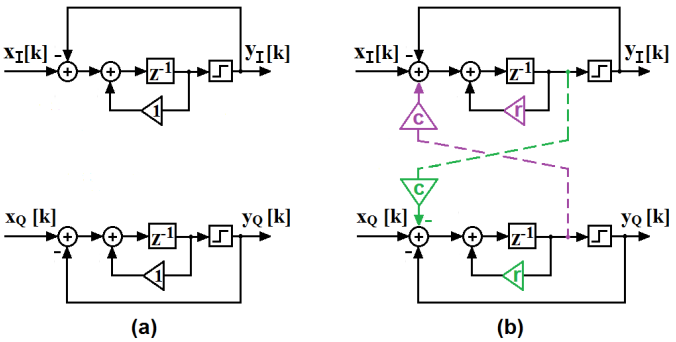

Fig. 1. Standard 1st order DSMs in quadrature (a); 1st order CDSM (b).

In order to ease the DSM analysis, the quantizer is often linearized by using an input-independent additive white noise model, with the quantization error sequence $e[k]$ [17]. Performing a z-domain analysis on the linear model, we obtain

$$Y_I(z) + jY_Q(z) = STF(z) \cdot \left(X_I(z) + jX_Q(z)\right) + NTF(z) \cdot \left(E_I(z) + jE_Q(z)\right) \quad (1)$$

where the STF and the NTF of the standard DSM are

$$STF_{D1}(z) = \frac{1}{z} \quad (2)$$

$$NTF_{D1}(z) = \frac{z-1}{z} \quad (3)$$

and the STF and the NTF of the CDSM are

$$STF_{CD1}(z) = \frac{1}{z + (1 - r + jc)} \quad (4)$$

$$NTF_{CD1}(z) = \frac{z - (r - jc)}{z + (1 - r + jc)} \quad (5)$$

Here, $X_I(z)$, $Y_I(z)$, $E_I(z)$ and $X_Q(z)$, $Y_Q(z)$, $E_Q(z)$ are the z-transforms of the input, output and quantization error for the I and Q paths, respectively.

The input signal is filtered by the signal transfer functions (STF_{D1} for DSM and STF_{CD1} for CDSM), whereas the quantization error is shaped by the noise transfer functions (NTF_{D1} for DSM and NTF_{CD1} for CDSM), in order to push the quantization noise outside the signal band. Furthermore, the NTF in (5) allows the placement of a complex zero, $z = r - jc \neq 0$, thus creating an asymmetric noise shaping based on the out-of-band noise requirements. The needed complex zero can be obtained by simply replacing the coefficients r and c from (5) with the values corresponding to the targeted normalized frequency (f_n), which can be obtained using the relationship between the z-transform and the Fourier transform in (6).

$$z = r - jc = Ae^{j2\pi f_n} \quad (6)$$

where A is the modulus of the complex number z.

Analyzing the NTF in (5), we notice a close link between the numerator and the denominator, namely the placement of a custom complex zero ($c \neq 0$) results in a characteristic polynomial with complex coefficients.

This is particularly problematic in the case of higher-order CDSM (for example 5th order in [10]), where the resulting transfer function with complex coefficients cannot be treated with design software, such as the Control System Designer toolbox in MATLAB.

Finally, this leads to two possible directions: we can either study the implementation of improved algorithms similar to [10], or propose a solution which can reduce the poles optimization to a known problem, thus allowing the use of existing design tools.

The second option, which will be further studied in this paper, suggests the decorrelation between the numerator and the denominator, by cancelling the r and c coefficients in the denominator.

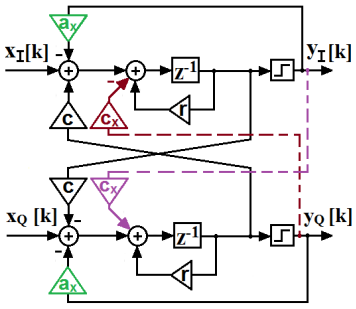

Fig. 2. Proposed 1st order CDSM.

B. Proposed 1st Order CDSM

In order to simplify the design of CDSM, we propose to reduce the characteristic polynomial to the known case of a 1st order DSM (Fig. 1a) without affecting the placement of the custom complex zero. We can indeed introduce additional feedback paths from the quantizers outputs to the inputs of the complex modulator. In particular, the direct feedback coefficient is modified from "1" to $a_x = r$ and a cross-coupling path with the coefficient $c_x = c$ is introduced in the modified CDSM architecture (Fig. 2).

Hence, we can obtain the STF and NTF of the proposed 1st order CDSM

$$STF_{p1}(z) = \frac{1}{z + (a_x - jc_x - r + jc)} = \frac{1}{z} \quad (7)$$

$$NTF_{p1}(z) = \frac{z - (r - jc)}{z + (a_x - jc_x - r + jc)} = \frac{z - (r - jc)}{z} \quad (8)$$

when setting $a_x = r$ and $c_x = c$.

Therefore, using this CDSM scheme, the denominator from (7-8) is reduced to a simple delay z^{-1} (independent of r and c, no complex coefficients), whereas the numerator in (8) remains identical to (5) and enables the placement of the custom complex zero according to (6).

Thanks to the decorrelation between the zeros placement and the characteristic polynomial, the proposed architecture has the advantage of increased configurability in targeting multiple communication scenarios. This is demonstrated in Fig. 3, where the STF, NTF and the associated pole-zero plots are shown for four different custom zeros, namely $z_1 = 0.25 + 0.97j$, $z_2 = 0.75 + 0.66j$, $z_3 = 0.75 - 0.66j$, $z_4 = 0.25 - 0.97j$.

First of all, we notice that the STF is the same for all the cases, as indicated in (7). Secondly, the sign of the

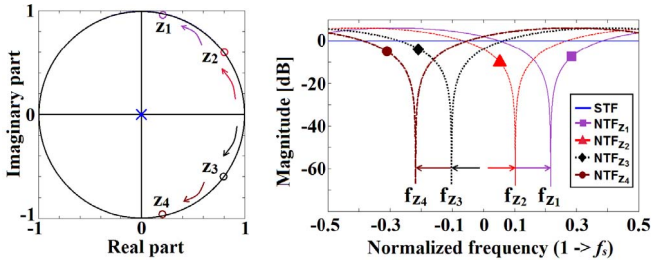

Fig. 3. Pole-zero plot (left); Signal and noise transfer functions (right).

imaginary part determines the position of the custom zero, namely if $Im(z) > 0$, then the normalized frequency is $f_z > 0$. Finally, the normalized frequency can be obtained using (6), for example in the case of $z_1 = 0.25 + 0.97j$, $f_{z1} \approx 0.21$.

In conclusion, this feature becomes very useful in the design of higher-order CDSM, because it allows configurable zeros placement while using existing DSM specific tools (NTF with real coefficients) for the poles optimization, which reduces considerably the number of design iterations and the computational effort.

III. Higher Order CDSM

The proposed 1st order CDSM scheme can be extended to higher order architectures in order to provide a general approach for the design of CDSMs. Thus, an n^{th} order CDSM can be built starting from $(n-k)$ real DSM stages, followed by k complex DSM stages, whereas k represents the number of custom complex non-conjugated zeros that need to be added, based on the targeted coexistence scenario.

This way, we can combine the advantages of both architectures, namely the increased SNR design margin thanks to the number of real stages $(n-k)$, and the custom complex zeros placement using complex stages, respectively.

In conclusion, we can identify two CDSM cases, namely higher order CDSM with one custom complex zero, and with multiple custom complex non-conjugated zeros.

A. CDSM With One Custom Complex Zero

Let us consider $n = 4$ and $k = 1$, namely three real stages in a Cascade-of-integrators feedback form (CIFB [11]), followed by the proposed complex integrator stage (Fig. 4).

In this case, the output in z-domain is the same as in (1), and the corresponding STF and NTF are given in (9) and (10)

$$STF_{p4}(z) = \frac{1}{den_4(z)} \tag{9}$$

$$NTF_{p4}(z) = \frac{(z-1)\cdot\left((z-1)^2+g_1\right)\cdot(z-(r-jc))}{den_4(z)} \tag{10}$$

$$den_4(z) = (z-r+a_x)\cdot(z-1)\cdot\left((z-1)^2+g_1\right) + a_3\cdot(z-1)^2 + a_2\cdot(z-1) + a_1 \tag{11}$$

Consequently, the characteristic polynomial $den_4(z)$ presents only real coefficients when $c = c_x$, whereas the influence of r can be cancelled by the a_x coefficient.

Thus, the decorrelation between the zeros placement and the characteristic polynomial allows the implementation of the

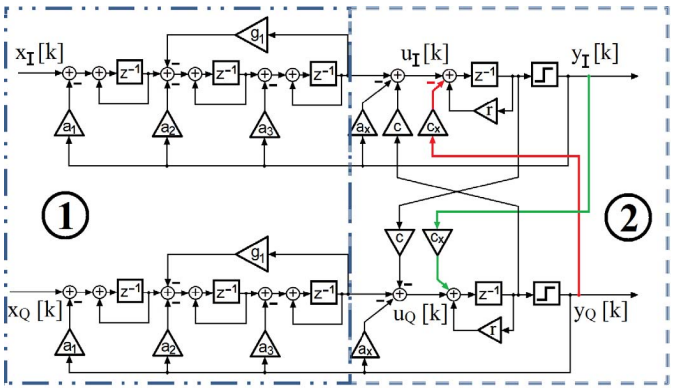

Fig. 4. 4th order CDSM: three real integrators (1); proposed complex stage (2).

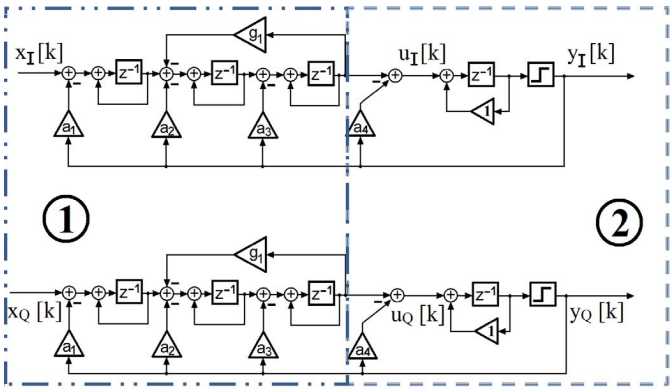

Fig. 5. 4th order DSM: three real integrators (1); standard real stage (2).

architecture based on the coefficient set $\{a_1, a_2, a_3, a_x, g_1\}$, resulting in a design which can be reduced to a known case of standard 4th order DSM (Fig. 5), as it can be seen from the STF and NTF

$$STF_{D4}(z) = \frac{1}{den_{D4}(z)} \tag{12}$$

$$NTF_{D4}(z) = \frac{(z-1)\cdot\left((z-1)^2+g_1\right)\cdot(z-1)}{den_{D4}(z)} \tag{13}$$

$$den_{D4}(z) = (z-1+a_4)\cdot(z-1)\cdot\left((z-1)^2+g_1\right) + a_3\cdot(z-1)^2 + a_2\cdot(z-1) + a_1 \tag{14}$$

The differences between the transfer functions of the two architectures (highlighted in Eq. (10-11) and (13-14)) show the transition from a DSM to a CDSM by moving a zero from DC $(z = 1)$ to a custom position $(z = r - jc)$, without affecting the optimization of the poles, i.e. the denominators of the STF and NTF are equivalent for $a_x = a_4 + r - 1$.

Hence, the proposed CDSM can be designed using existing optimization tools specific to DSM (obtain the coefficient set $\{a_1, a_2, a_3, a_x, g_1\}$), and can target different coexistence scenarios without the need of redesign, as in the case of [10] and [11]. Furthermore, the multi-standard coexistence depends now on only two coefficients, r and c, making it easier to provide a configurable solution.

This design simplification is demonstrated through simulation in MATLAB of a practical example and will be described next. First of all, using the Schreier Toolbox in MATLAB,

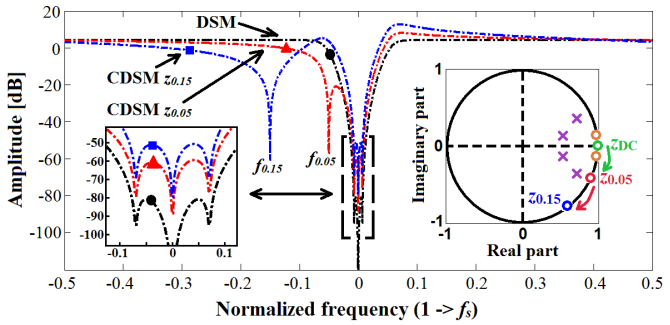

Fig. 6. 4th order DSM and CDSMs: NTFs, pole-zero plot, signal band (zoom).

we can obtain the coefficients of a 4th order DSM, with an oversampling ratio OSR = 100 (for high-speed applications) and a peak gain of the NTF equal to 1.6. The resulting values are $[a_1, a_2, a_3, a_4, g_1] = (0.01, 0.1, 0.41, 0.93, 0.002)$, and were used to obtain the associated noise transfer function (Fig. 6), where we can observe two zeros at DC and two complex conjugated zeros at the edges of the signal band.

Secondly, as it was mentioned before, the same set of coefficients obtained for the DSM can be used in the design of CDSM with configurable custom zeros placement. In order to verify this feature, let us consider two different frequency bands, $f_{0.05} = -0.05$ (close to the signal band) and $f_{0.15} = -0.15$ (out-of-band). Using (6) we can obtain the corresponding complex numbers $z_{0.05} = 0.95 - 0.31j$, and $z_{0.15} = 0.59 - 0.81j$.

These values are further introduced in Eq. (10-11) in order to obtain the NTFs shown in Fig. 6, whereas $a_{x,\,0.05} = 0.93 + 0.95 - 1 = 0.88$, and $a_{x,0.15} = 0.52$.

Hence, we notice that one of the zeros previously at DC is moving its position on the unit circle, depending on the values of r and c, without changing the position of the poles in all three cases (pole-zero plot in Fig. 6).

When compared to the 4th order DSM, the out-of-band noise integrated in the targeted frequency bands ($f_{0.05}$ and $f_{0.15}$) is considerably reduced in the CDSM case. However, the complex zeros placement will cause a noise redistribution leading to a degradation of SNR, which becomes larger with the distance between the position of the zeros and f_c.

This effect (highlighted in Fig. 6) is specific to CDSM architectures in general, and implies a design trade-off between a reduced noise level in a specific frequency band, and overall SNR performances. This type of situation is encountered in stringent multi-standard coexistence scenarios, e.g. in a mobile application an 802.11 transmitter working in the 2.4 GHz band coexisting with a GPS receiver working in the 1.6 GHz band on the same chipset. Hence, it is important to define the SNR requirements at the beginning of the design phase and choose the appropriate modulator order, oversampling ratio or out-of-band NTF gain, to provide adequate design margin and account for the SNR loss due to the complex zeros placement.

The proposed method can be applied independently of a particular value of the OSR, though reducing the OSR will inherently degrade the final SNR.

B. CDSM With Multiple Complex Non-Conjugated Zeros

The implementation of a NTF with multiple complex non-conjugated zeros can be useful in applications, such as the ones presented in [10], which target the matching of the UMTS and DCS 1800 standards out-of-band spurious emissions using a 5th order CDSM with two complex integrator stages and optimized poles.

This architecture can also be implemented using the proposed 1st order CDSM scheme for $n = 5$, and $k = 2$, resulting in three real integrators followed by two complex stages (Fig. 7). Furthermore, we note that both additional cross-couplings are introduced from the I and Q quantizers outputs, which ensures the cancellation of the complex coefficients of the characteristic polynomial without affecting the position of the custom zeros.

Next, we write the STF and the NTF

$$STF_{p5}(z) = \frac{1}{den_5(z)} \tag{15}$$

$$NTF_{p5}(z) = \frac{(z-1)\cdot((z-1)^2+g_1)\cdot(z-(r_1-jc_1))\cdot(z-(r_2-jc_2))}{den_5(z)} \tag{16}$$

$$den_5(z) = \left[(z - r_2 + a_y)\cdot(z - r_1) + c_1^2 + a_x\right]\cdot(z-1) \cdot\left((z-1)^2 + g_1\right) + a_3\cdot(z-1)^2 + a_2\cdot(z-1) + a_1 \tag{17}$$

A complete decorrelation between zeros placement and poles optimization is achieved when

$$\begin{cases} c_x = c_1\cdot(2 - a_5 - 2\cdot r_1) \\ c_y = c_1 + c_2 \end{cases} \tag{18}$$

$$\begin{cases} a_x = (a_5 + r_1 - 1)\cdot(r_1 - 1) + a_4 - c_1^2 \\ a_y = a_5 + r_1 + r_2 - 2 \end{cases} \tag{19}$$

where a_4 and a_5 are the coefficients of the two last stages of a 5th order DSM.

Again, using the Schreier Toolbox in MATLAB we can obtain the coefficient set $\{a_1, a_2, a_3, a_4, a_5, g_1\}$ for a 5th order DSM, with an oversampling ratio OSR = 100 and a peak gain of the NTF equal to 1.6, namely $[a_1, a_2, a_3, a_4, a_5, g_1] = (0.0015, 0.018, 0.113, 0.4215, 0.93, 0.01)$.

In order to compare the design methodology and architecture with [10], we will illustrate the functionality of the proposed higher order CDSM scheme with multiple custom complex zeros (5th order), considering the same application, i.e. UMTS and DCS 1800 standard coexistence.

In [10], for the UMTS case, the two complex non-conjugated zeros are placed in the DCS 1800 TX band at $f_c - 0.03$, and in the UMTS RX band at $f_c + 0.05$, whereas for the DCS 1800 case, the first zero is placed in the DCS RX band at $f_c + 0.03$, and the second in the UMTS RX band at $f_c + 0.06$, respectively. Furthermore, in both cases there are three zeros (one real and two complex-conjugated), which are placed in the signal band, at the center frequency (f_c) and at $f_c \pm 0.01$.

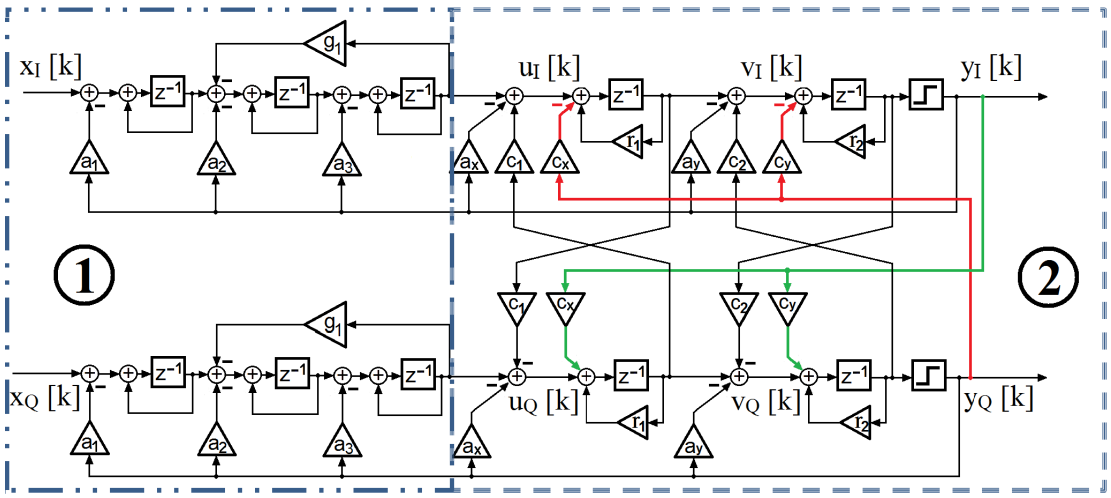

Fig. 7. Proposed 5th order CDSM with two complex integrator stages.

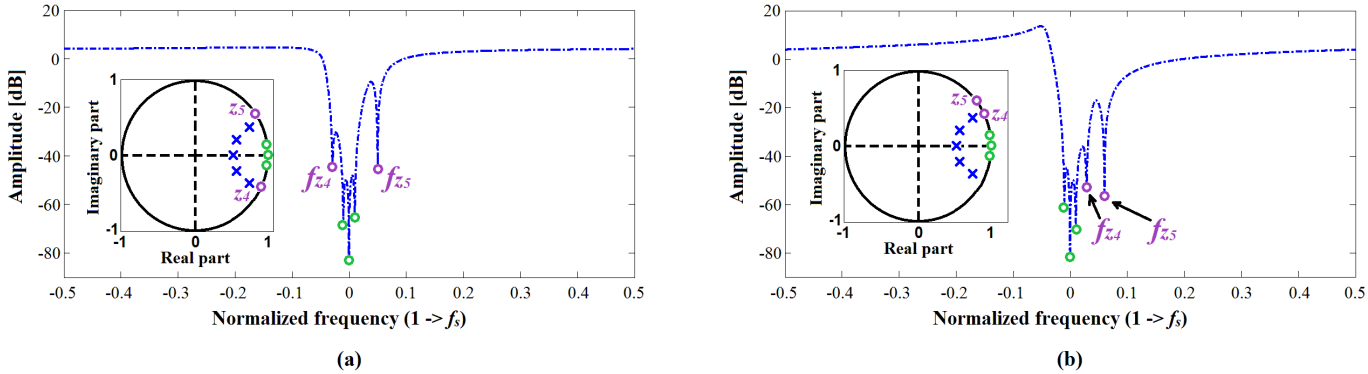

Fig. 8. NTF and pole-zero plot of proposed 5th order CDSM: a) UMTS case; b) DCS 1800 case.

By applying (6), we can obtain the complex numbers corresponding to these frequencies, namely in the UMTS case $[z_1, z_2, z_3, z_4, z_5]_{\text{UMTS}} = (1, 1 + 0.063j, 1 - 0.063j, 0.98 - 0.18j, 0.95 + 0.31j)$, and in the DCS 1800 case $[z_1, z_2, z_3, z_4, z_5]_{\text{DCS}} = (1, 1 + 0.063j, 1 - 0.063j, 0.98 + 0.18j, 0.93 + 0.37j)$. The complex non-conjugated zero pairs are $[r, c]_{\text{UMTS1}} = (0.98, 0.18)$, $[r, c]_{\text{UMTS2}} = (0.95, -0.31)$, $[r, c]_{\text{DCS1}} = (0.98, -0.18)$, $[r, c]_{\text{DCS2}} = (0.93, -0.37)$. Based on these values we can obtain the NTF and the pole-zero plots for the UMTS and DCS cases (Fig. 8), which are very similar with the results presented in [10].

We remark that the design of the proposed scheme is considerably easier to perform compared to [10], needing only the coefficient set of a DSM (obtained automatically using existing tools), and the custom zeros placement (obtained from the specifications of the out-of-band spurious emissions).

C. General CDSM Design Method

It was previously shown how an n^{th} order CDSM can be built out of $(n-k)$ real stages followed by k complex stages, where $k \geq 1$. The design of the proposed CDSM can be generally reduced to the following steps (Fig. 9): i) define the SNR requirements for the desired signal bandwidths and determine the number of real stages $(n-k)$, ii) identify the frequency bands with stringent noise requirements to obtain the number of complex stages (k) and the position of the custom complex non-conjugated zeros ($[r, c]$ coefficient pairs), and iii) obtain the initial values of coefficients for an n^{th} order DSM with existing design tools. A simple simulation can then be performed on the chosen CDSM to verify that the SNR requirements are met.

As described previously, there is a trade-off between the in-band SNR and the position of the notches relative to the center frequency. If the requirements are not fulfilled, then an additional margin is taken in the initial design phase and a new set of coefficients is generated and tested. This process requires in most application cases very few iterative steps.

Finally, we may state that the proposed method can in principle be applied to both digital (transmitter) and analog (receiver) DSM applications. Limitations remain those specific to the analog or digital domain. In the digital domain, the coefficients are subject to quantization, whereas in the analog domain the coefficients are impacted by mismatch. Mismatch between in-phase and quadrature paths can in particular be of concern in the analog implementation of complex DSMs (as shown in [16]).

IV. Application

This section details one application example in which the proposed method is used to design a 4th order CDSM as part of

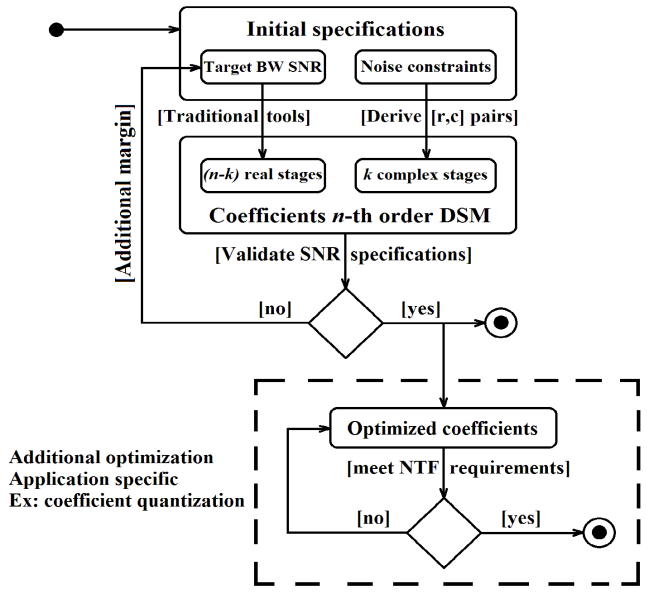

Fig. 9. Activity diagram of the proposed CDSM design method.

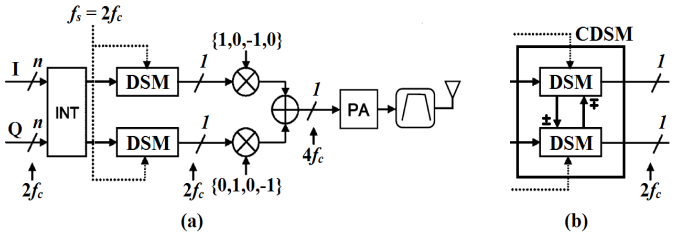

Fig. 10. Digital transmitter: (a) DSM-based [18]; (b) cross-coupled DSMs.

a highly-integrated WLAN digital transmitter chain, building upon delta-sigma modulation and efficient switching PA.

The block diagram of a DSM-based transmitter is shown in Fig. 10a, as introduced in [18]. This architecture is based on i) two single-bit DSMs working synchronously at $2^* f_c$, ii) a digital to RF mixing (D-RF) stage which ideally interleaves the I and Q paths at $4^* f_c$, and iii) a linear and highly efficient switching-mode power amplifier (PA). The digital implementation of the signal path up to the final PA eliminates potential I-Q mismatch and performance degradation due to this mismatch.

At the digital-to-RF mixer inputs, I and Q 1-bit samples are simultaneously available during a period $1/(2^* f_c)$ as illustrated in Fig. 11a. The interleaving operation results in the sequence composed of $\mathrm{I}(s_n)$ and $\mathrm{Q}(s_n)$, which translates to $\mathrm{I}(s_i)$ and $\mathrm{Q}(s_i)$ (s_n is the sampling instant at $2^* f_c$ and s_i at $4^* f_c$).

However, the samples required for the RF stream RF_{out} at $4^* f_c$ are $\mathrm{I}(s_i)$ and $\mathrm{Q}(s_i + 1)$ in order to achieve a correct quadrature operation. Therefore, an interpolator stage (INT) is introduced to derive the missing quadrature sample $\mathrm{Q}(s_i + 1)$, which is equivalent to $\mathrm{Q}(s_n + 1/2)$, where 1/2 represents the ratio between $2^* f_c$ and $4^* f_c$ (Fig. 11b).

A CDSM can be introduced in this architecture by cross-coupling the inner stages of quadrature DSMs (Fig. 10b), in order to place custom complex zeros and be able to target multi-standard coexistence with nearby receivers.

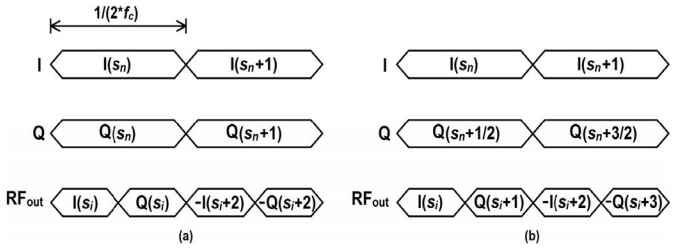

Fig. 11. D-RF stage sampling operation in [18]: (a) without INT (b) with INT.

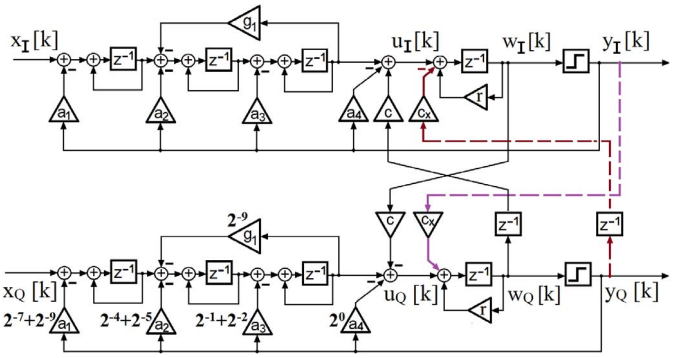

Fig. 12. Proposed 4th order CDSM as part of a digital TX chain.

Following the proposed CDSM design method, the first step is to define the specific SNR requirements for the targeted application, which determine the order of the CDSM. For instance, [7] describes the design of a 3rd order DSM targeting signal bandwidths from 20 MHz up to 160 MHz with an SNR larger than 67 dB.

Hence, we use three real stages followed by a complex stage to obtain a 4th order CDSM (Fig. 12) with competitive output SNR performances.

The structure is very similar to the one reported in Fig. 4, except for an additional delay of $1/(2^* f_c)$, introduced in the Q-paths from w_Q and y_Q to u_I, due to the synchronous operation of the I and Q paths of the CDSM. As explained earlier in the section, for the correct interleaving operation, the CDSM is working at half the final sampling frequency ($2^* f_c$), thus producing only half the samples on each path.

Adding this delay is mandatory to process the correct I and Q samples when performing the cross-coupling of the quadrature paths.

This would not be the case if the DSM operated at $4^* f_c$, yet this would imply higher power consumption and additional timing constraints as a result of the higher frequency clock.

The corresponding STF and NTF of the 4th order CDSM can be expressed as follows, for $c = c_x$

$$STF(z) = \frac{1}{den(z)} \tag{20}$$

$$NTF(z) = \frac{(z-1)\cdot\left((z-1)^2 + g_1\right)\cdot\left(z - \left(r - jc\cdot z^{-0.5}\right)\right)}{den(z)} \tag{21}$$

$$den(z) = a_1 + a_2\cdot(z-1) + a_3\cdot(z-1)^2 + (z - r + a_4) \cdot(z-1)\cdot\left((z-1)^2 + g_1\right) \tag{22}$$

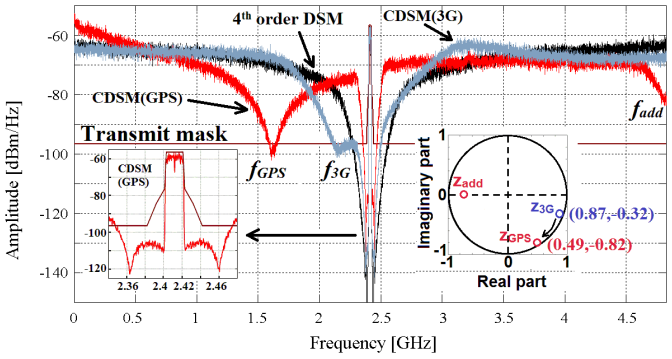

Fig. 13. Simulated output spectrum: 4th order DSM and CDSM; Complex zeros placement for 3G and GPS (zoom right).

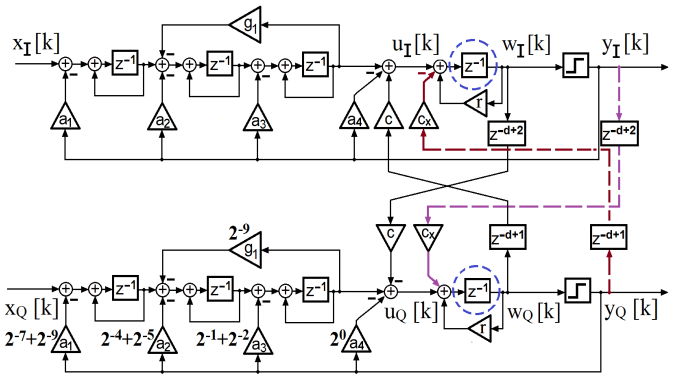

Fig. 14. CDSM with configurable delayed cross-coupling paths.

where a half-period delay ($z^{-0.5}$) is introduced in the equation due to the additional delay elements $1/(2^* f_c)$ in the Q paths, relative to the sampling period of $1/(4^* f_c)$.

Consequently, using the proposed CDSM scheme, the multi-standard coexistence can be made configurable and depends on only two coefficients, namely r and c, whereas the main architecture based on the coefficient set $\{a_1, a_2, a_3, a_4, g_1\}$ is the same as in the case of a real modulator. This feature is verified through simulations, for an input signal bandwidth $BW = 20$ MHz and $f_c = 2.412$ GHz (Fig. 13). Moreover, all the coefficients are quantized to sums of powers of two in order to simplify the digital implementation.

For the same general CDSM architecture, the complex zero is placed at $f_{GPS} \approx 1.6$ GHz (close to GPS and GLONASS bands) for $[r_{GPS}, c_{GPS}] = (2^{-5}, 2^{-1} + 2^{-2} + 2^{-3} + 2^{-4})$ in the first example, while it is placed at $f_{3G} \approx 2.17$ GHz (close to 3G communication bands) for $[r_{3G}, c_{3G}] = (2^{-1} + 2^{-2} + 2^{-4}, 2^{-2} + 2^{-4})$ in the second example, as highlighted in Fig. 13. We further observe that r has only a minor influence on the NTF. Hence, the dynamic coefficient a_x (used in Fig. 4 to compensate the real part of the complex zero in specific coexistence scenarios) can be replaced by the static coefficient a_4 of the 4th order DSM (a_4 is now used in Fig. 12 instead of a_x from Fig. 4).

When compared to the output of a 4th order DSM, the out-of-band noise integrated in the critical frequency bands (f_{GPS} and f_{3G}) is considerably reduced in the CDSM case, with ~20 dB at f_{3G} and ~30 dB at f_{GPS}. Moreover, we can notice that for the CDSM with $[r_{GPS}, c_{GPS}]$ (*CDSM(GPS)* in Fig. 13) there is an additional zero at $f_{add} = 2^* f_c$, which results from the second solution of the polynomial $(z - (r - jc \cdot z^{-0.5}))$ in (21), namely $z_{add} = -0.93$ (modulus almost equal to 1).

At the same time, as it was identified in a previous section, Fig. 13 reveals that the complex zeros placement leads to a relative degradation of the SNR, which is proportional to the distance between the position of the zero and f_c. This degradation can be partially compensated through an adequate choice of the SNR design margin and modulator's parameters. A complementary solution may be found in [19], which proposes a 1-bit multi-step look-ahead architecture to improve the input dynamic range and SNR compared to error-feedback structures, while maintaining a low complexity overhead for real-time operation.

Furthermore, it can be seen that the bandwidth of the CDSM (zoom signal band in Fig. 13) can be configured (g_1 coefficient in Fig. 12) to address (digitally) the three non-overlapping 20 MHz WLAN channels in the 2.4 GHz band, or to increase the signal bandwidth up to 40 MHz, thus meeting the near-band transmit mask in a worst-case scenario (GPS). Finally, in order to attenuate the noise outside the CDSM bandwidth, solutions such as analog filtering, or FIR filtering [9] can be employed.

V. Coarse/Fine Configurable CDSM

It was shown, that using the $[r, c]$ parameters we are able to configure the complex zeros placement, whereas the frequency step (granularity) depends on the number of coefficient pairs and quantization. For example, in order to achieve configurability in the frequency domain $[f_{3G}, f_{GPS}]$ (around 600 MHz range), we need to predefine as many $[r, c]$ coefficient pairs as possible, between $[2^{-5}, 2^{-1} + 2^{-2} + 2^{-4}]$ for r, and $[2^{-2} + 2^{-4}, 2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}]$ for c, respectively.

However, this would add large constraints to a real digital implementation, due to additional paths and increased number of operations.

In this case, the maximum operating frequency of the modulator may be reduced, thus limiting its performances (OSR, SNR, noise shaping) and application (limited f_c for the communication standard).

Consequently, we propose to minimize the number of $[r, c]$ coefficient pairs, and combine this with a coarse tuning mechanism for band selection using additional delays in the cross-coupling paths of the CDSM (Fig. 14), similar to the principle of asymmetric embedded FIR-filtering in [20].

A. CDSM With Delayed Cross-Coupling Paths

The noise shaping of the proposed 4th order CDSM is very similar to the asymmetric unbalanced embedded-FIR filtering presented in [20], which introduces additional delays in the cross-coupled I and Q paths between the DSM and mixer stages of a digital transmitter chain similar to [18].

Furthermore, [20] employs a different number of delays in the cross-coupling paths to compensate for the INT stage,

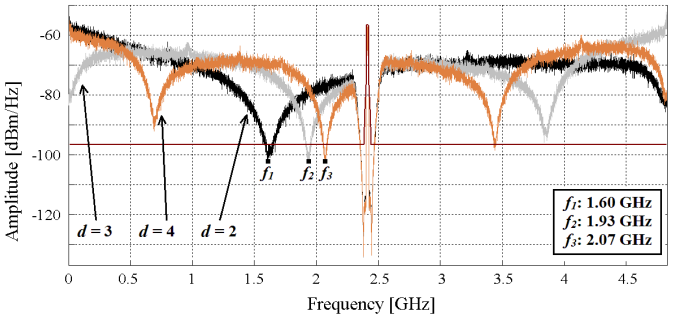

Fig. 15. Simulated output spectrum: CDSM with delayed cross-coupling paths.

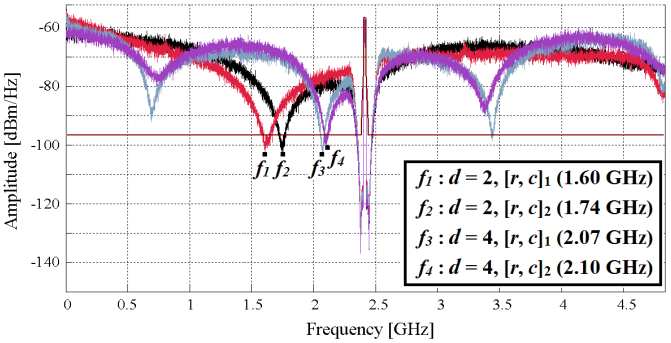

Fig. 16. Simulated output spectrum: CDSM with delayed cross-coupling paths.

namely $d-1$ for the I (z^{-d+1}) and d for the Q (z^{-d}) paths ([20] uses the notation k instead of d). The main advantage of the architecture in [20] is the introduction of configurable notches at specific frequencies (based on d) using simple digital logic, which can relax the filtering constraints of the system.

Hence, we propose to use the same principle of delayed cross-couplings between the inner stages of the CDSM (Fig. 14), to obtain NTF notches at different frequencies.

Simulation results for an input signal bandwidth $BW = 20$ MHz centered at $f_c = 2.412$ GHz, $[r_{GPS}, c_{GPS}]$, and different values of d (d equal 2, 3, and 4) show that the position of the complex zero changes with d (non-linearly) without affecting the noise shaping around the transmit band (Fig. 15), thus providing an additional mechanism for band selection in the zeros placement.

Moreover, increasing the number of delays in the cross-coupling paths has the advantage of introducing additional notches out-of-band which relax even more the succeeding filtering stage needed to meet the overall noise requirements.

B. Coarse/Fine Tuning Mechanism

Let us combine the two aforementioned effects, in order to obtain a coarse/fine tuning mechanism for multi-standard coexistence. The r and c coefficients are used for fine adjustment, and d is used to determine the coarse frequency band selection. In this case, using the same $[r, c]$ coefficient pairs, we can cover several frequency domains for different values of d.

Furthermore, we assume $N[r, c]$ coefficient pairs which correspond to N complex zeros placed in the frequency domain $[f_c - f_c/3,\ f_c - f_c/5]$ for $d = 2$. If we increase d, for example setting $d = 4$, we will retrieve the N complex zeros at locations which are proportional to the new frequency domain, $[f_c - f_c/7,\ f_c - f_c/9]$. This feature is highlighted in Fig. 16, for $d = \{2, 4\}$, $[r, c]_1 = (2^{-5}, 2^{-1}+2^{-2}+2^{-3}+2^{-4})$, $[r, c]_2 = (2^{-2} + 2^{-5}, 2^{-1} + 2^{-2} + 2^{-4})$, whereas $BW = 20$ MHz and $f_c = 2.412$ GHz.

Thus, the proposed coarse/fine tuning enables multi-standard coexistence in a digital CDSM-based TX chain over the frequency domain $[f_c - f_c/3,\ f_c]$ thanks to a reduced number of coefficient pairs combined with configurable band selection for improved performances and relaxed constraints.

In addition, this mechanism can also be applied for the symmetric frequency domain $[f_c,\ f_c + f_c/3]$ using only two digital inverter cells, namely for inverting the sign of the Q samples at the input of the CDSM, and again in the digital to RF mixing stage (as shown in Fig. 10).

In conclusion, the complete mechanism ensures zeros placement configurability over an extended frequency domain $[f_c - f_c/3,\ f_c + f_c/3]$ and greatly simplifies the final architecture implementation, i.e. less coefficient pairs, digital delays for band selection and inverter cells for symmetry.

VI. Conclusions

This paper describes an improved scheme for the 1st order Complex Delta-Sigma Modulator, which can be used in the design of higher order CDSMs with one or more custom complex non-conjugated zeros, using standard design and optimization tools specific to DSM.

Additional feedback paths allow the decorrelation between the placement of a complex zero and the characteristic polynomial. Hence, compared to other known methods [10], [11], the proposed CDSM can ease multi-standard coexistence using a generic well-known architecture and may achieve a noise level reduction at specific frequency bands of 20-30 dB.

Furthermore, we studied a complementary mechanism for zeros placement, by introducing additional delays in the cross-coupling paths of the CDSM block. Consequently, we obtain a coarse/fine control over the coexistence bandwidth, which simplifies the implementation, thanks to the reduced number of $[r, c]$ coefficient pairs.

Finally, the proposed configurable CDSM presents increased flexibility and a "true" single-bit output unlike the unbalanced embedded-FIR scheme in [20], thus allowing low overhead dynamic adjustment of the complex zeros at system level to protect the relevant receive channels in the coexistence scenario.

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All-Digital Transmitter Architecture Based on Two-Path Parallel 1-bit High Pass Filtering DACs

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***Abstract*— This paper presents a novel transmitter architecture which is tailored for low power, all-digital, and high speed implementation. It is based on two-path parallel digital-to-analog converters (DAC) which are driven by 180° phase-shifted clocks. The architecture operates in high pass mode and extends the output carrier frequency up to half the DAC clock rate. To decrease the number of analog unit current cells in the converter, a low-pass $\Delta\Sigma$-modulator is used. Since the modulator also converts the input resolution to 1-bit, an inherently-linear digital-to-analog conversion is realized by embedding filtering in the DAC. Furthermore, the finite impulse response DAC transfer function is designed to cancel the $\Delta\Sigma$-modulator quantization noise. Simulation results at system level demonstrate the robustness of the architecture against random coefficient mismatches, and its suitability for broadband transmissions. The error vector magnitude of the quadrature output is simulated for up to 15% random coefficient mismatch and it maintains a value below −22 dB even when the input signal bandwidths vary from 20 MHz (64-subcarrier OFDM) to 160 MHz (512-subcarrier OFDM). Experimental results are presented to discuss the validity of the proposed all-digital transmitter architecture and to highlight the challenges of implementing it in advanced CMOS nodes.**

***Index Terms*— Digital transmitter, high pass FIR DACs, time-interleaving, parallel DACs.**

I. Introduction

ALL-DIGITAL low power wireless transmitter implementations have employed the RF-DAC concept to merge both the digital-to-analog conversion and frequency translation in a direct digital-to-RF converter (DRFC) [1]. To ease matching requirements and facilitate high speed conversion, $\Delta\Sigma$-modulators are sometimes used to reduce the number of bits in the DAC at the cost of high sampling rates and large out-of-band quantization noise. The absence of any quantization noise filtering mechanism in the RF-DAC, other than $sinc(x)$, results in a transmitter which requires a high order analog filter in its output stage [2]. While the analog filter order can be lowered by operating the DRFC at a large oversampling ratio, without gain in useful data bandwidth, this comes at the cost of increased power consumption.

To solve the problem of filtering without using analog filters, one solution is to utilize a finite impulse response (FIR) DAC which embeds filtering in a DAC. A 1-bit FIR DAC is inherently linear. It is also robust against random coefficient mismatches as it only affects the stopband of the filter transfer function. A short-length FIR filter in a DAC can be designed to create isolated notches in the receive band [3] and it can be an effective mixed-domain solution to problems of transmitter coexistence [4]. High order, 1-bit FIR DAC can be used for effectively canceling rising quantization noise when it has high resolution coefficients. Reference [5] implements a mixing FIR RF-DAC which combines the strengths of the digital-IF transmitter architecture by implementing the quadrature modulation at low frequency in digital and that of a Band Pass (BP) $\Delta\Sigma$ modulator for lowering resolution bits with good in-band linearity. One weakness of a mixing FIR DAC architecture is that the length of the filter is limited by the magnitude of the DAC third-order intermodulation product. This results in low out-of-band attenuation by the embedded semi-digital filter as small number of taps have to be chosen to lessen effects of distortion. Naturally, a non-mixing FIR DAC can accommodate higher number of taps without increasing distortion due to finite current source output impedance. However, it requires a separate front-end analog mixing stage as in any classical transmitter architecture [6].

Another solution is to remove the $\Delta\Sigma$-modulator and instead use a high-resolution RF-DAC. Since the linearity of the DAC is significantly affected by mismatch, calibration circuitry is necessary. An all-digital I/Q RF-DAC implemented in [7] achieves quadrature summation by duty-cycled transmission of $-I, -Q, I, Q$ using four non-overlapping clocks. With this architecture, the quadrature output frequency is centered at the frequency of either of the phase-shifted clocks. Nevertheless, this architecture does not achieve high f_c/f_s ratio as the circuit operates at an effective sampling rate of four-times the output carrier frequency.

To reach carrier frequencies up to half the signal sampling frequency of the DAC, $f_c = f_s/2$, without including a mixing stage in the DAC, the work in [8] takes as an input a quadrature

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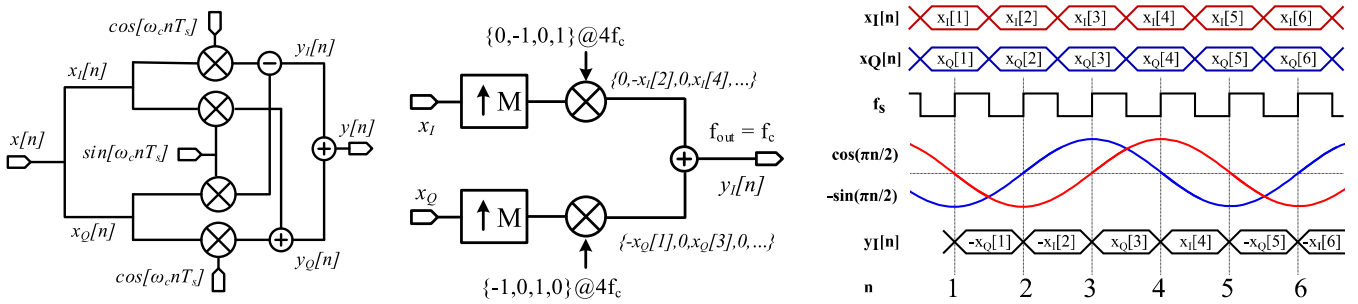

Fig. 1. Complex mixing in digital transmitter architecture. (a) Complex multiplier. (b) digital transmitter architecture, $f_c = f_s/4$. (c) Timing at the digital mixers.

output signal at $4f_c$ to a two-path interleaved architecture which has a cascade of a high pass (HP) $\Delta\Sigma$-modulator and a multi-bit DAC in each of its channel. Image rejection is obtained due to multi-phase clocking of the channels. It has strengths in that its all-digital structure can leverage technology scaling to enhance performance. Nonetheless, this architecture relies only on the zero-order-hold response, $sinc(x)$, of the DAC for far-out spectrum, quantization noise filtering. Moreover, the quadrature modulator which generates the DAC input signal still operates at twice the sampling frequency of the $\Delta\Sigma$-modulators and the DACs in the time interleaved (TI) structure.

To remedy the absence of inherent filtering in RF-DACs, this work proposes a transmitter architecture based on parallel HP FIR DACs. It reaches high output carrier frequency, $f_c = f_s/2$, while still avoiding problems associated with integrating a mixing stage in a conversion circuitry. Its performance benefits from implementation in advanced nodes as it has all-digital circuit blocks. It is also robust against random coefficient mismatches. In Section II, the proposed architecture is introduced starting with a discussion on basic digital transmission at $f_c = f_s/4$. This is further developed and is used for constructing a transmitter based on parallel DACs. The proposed architecture is further refined with the addition of a $\Delta\Sigma$-modulator and a HP FIR DAC. Validation of the architecture using system-level simulations were carried out and are presented in Section II. Wideband and sinusoidal input signals are employed to validate it. The most important non-idealities related to this architecture are discussed in Section III. Supporting data and simulation results are included to appraise their impact on the performance that can be achieved by the architecture. The challenges associated with circuit implementation of the proposed architecture are discussed in Section IV. In addition, in this section, circuit level issues are discussed using results from an implemented HP FIR DAC. Measured results of a single channel HP FIR DAC also make part of this section. The paper ends with a conclusion in Section V.

II. Proposed Transmitter Architecture

To realize frequency translation, Cartesian transmitters usually implement the real part of the output of a complete complex mixer shown in Figure 1a. Since it is helpful in explaining the proposed transmitter architecture, some equations related to this are briefly recalled below.

A. Digital Transmitter Architecture With $f_c = f_s/4$

Let $x_I[n]$ and $x_Q[n]$ be the real and imaginary components of an input signal $x[n]$, and output signal $y[n]$ is the product of complex multiplication of $x[n]$ and $e^{j\omega_c nT_s}$. $y[n]$ is a version of the input signal frequency-translated around the output frequency ω_c.

$$y[n] = x[n]e^{j\omega_c nT_s} \tag{1}$$

$$y[n] = \Big(x_I[n] + jx_Q[n]\Big)\Big(cos[\omega_c nT_s] + jsin[\omega_c nT_s]\Big) \tag{2}$$

Because the input signal $x[n]$ can be recovered with just the real part of the output signal at the receiver, the expression which produces $y_I[n]$ is what is implemented in a Cartesian transmitter.

$$y_I[n] = x_I[n]cos[\omega_c nT_s] - x_Q[n]sin[\omega_c nT_s] \tag{3}$$

To decrease the number of multipliers, resulting due to the fact that $x[n]$ has usually high resolution, and simplify their implementation, integer ratio is sought between the values of the output carrier frequency (f_c) and the sampling frequency (f_s) [9]. A popular choice is $f_c = \frac{f_s}{4}$:

$$y_I[n] = x_I cos\Big[\pi n/2\Big] - x_Q sin\Big[\pi n/2\Big] \tag{4}$$

$$y_I = -x_Q, -x_I, x_Q, x_I, \ldots \tag{5}$$

To obtain this output, two digital mixers can be added in both I and Q paths as depicted in Figure 1b. This arrangement allows for a simple implementation of the mixers. The timing diagram plots in Figure 1c show that a sequence of $0, -1, 0, 1$ and $-1, 0, 1, 0$ can be used in I and Q paths, respectively, to generate the right outputs. The final carrier frequency is one-fourth of the sampling frequency of the output stage.

This architecture has been implemented, for example, for a digital output using LP $\Delta\Sigma$-modulators and digital mixers in [10]; or in [11] using dedicated multi-bit converters for each of the negative and positive I and Q paths. It has also been used as a first-stage low-frequency mixer preceding a second-stage mixing RF-DAC [5].

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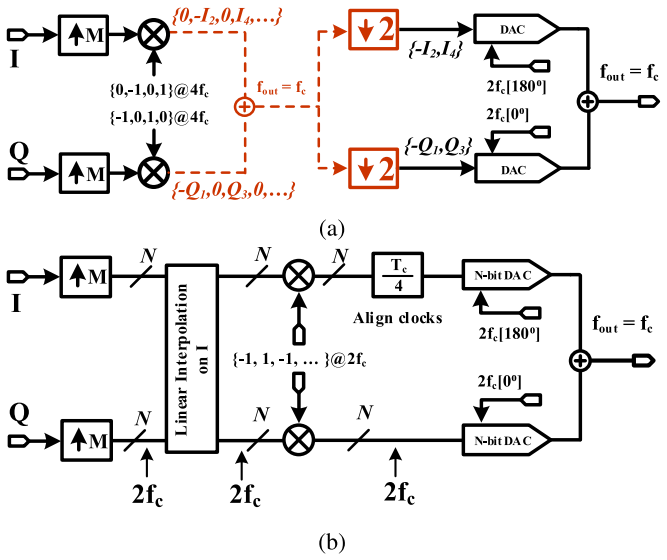

Fig. 2. a) Digital transmitter architecture with $f_c = f_s/4$ followed by 2-path data interleaving stage b) The basic structure of the proposed transmitter architecture.

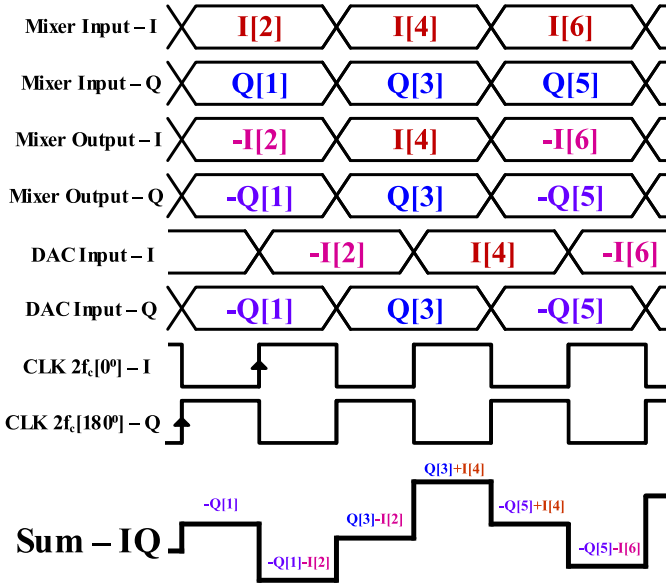

Fig. 3. Timing diagram in the proposed transmitter architecture.

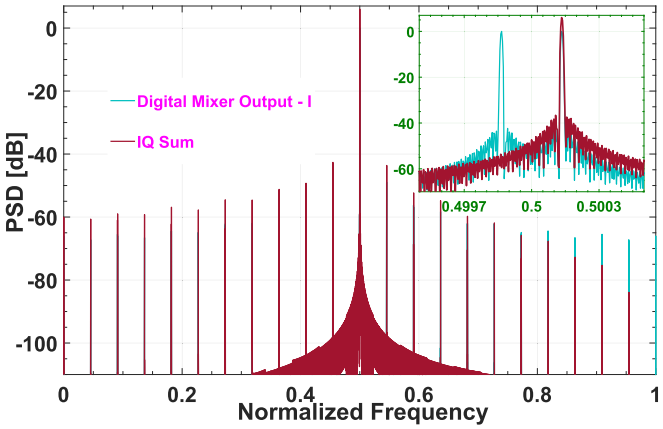

Fig. 4. frequency response of the basic architecture for a sinusoidal input.

B. Basic Structure of the Proposed Architecture

Equally, in the above architecture, the digital output sampled at $4f_c$ can be downsampled to drive parallel DACs operating at $2f_c$. This arrangement is shown in Figure 2a where a digital transmitter architecture whose output is at $fc = fs/4$ is followed by a data interleaving stage based on two-path parallel DACs. As has been demonstrated in [12]–[15], L-path parallel DACs, which are clocked at $1/L$ of the input sampling frequency, can be used to remove Nyquist images of a digital sampled input signal. In the special case of two-path parallel DACs, their clocks are 180° delayed from each other and are at a frequency $1/2$ of the input sampling frequency. Theoretically, all the images of the input digital signal in the second and third Nyquist zones are absent in the summed analog output. In the architecture in Figure 2a, although the DACs can run at twice the summed output carrier frequency without the need for a high-order filter, most of the digital circuits still operate at four times the carrier frequency. To lower the sampling rate—not just for the DACs, but for the whole architecture—the structure needs to be optimized.

The summed digital output after the digital mixers is downsampled by two as part of the data interleaving process. After clock alignment with a half clock cycle delay, the input data to the two parallel DACs are $-I_2, I_4, \ldots$ and $-Q_1, -Q_3, \ldots$ and these can be sampled by 180° phase-shifted clocks. These input data to the two DACs are similar to the corresponding data at the output of the digital mixers except for the missing zeros. These same data can be extracted directly from the output of the digital mixers by skipping the summation in digital and data interleaving blocks. This is done by scrapping each of the zero multiplication products from the output of the digital mixers. To accomplish this, all that has to be done at the clock side of the mixers is hold each of the -1 and 1 multiplication for one more clock cycle. For the digital blocks to the left of the digital mixer, it has been previously shown that they can operate at half the sample rate by using linear interpolation on the missing I/Q samples [10]. The optimized architecture of Figure 2b has both the DACs and the digital signal processing (DSP) blocks operating at $2f_c$.

The timing diagram in Figure 3 shows the propagation of an input data through the different blocks of the proposed architecture. Since the DSP blocks run on the same clock, I/Q inputs to the mixers have the same alignment. The $T_c/4$ delay block is equal to half DAC clock cycle. It can be implemented using latches that are clocked at $2f_c$ [16]. This $T_c/4$ delay block is inserted to align the clocks of the two paths. Due to the 180° phase-shift, the data instants at the outputs of I-path and Q-path DACs overlap for a time segment of $T_c/4$, where T_c is the period of the output signal. Therefore, the summed output signal has two distinct signal levels for each period of either of the DAC clocks. The basic structure of the proposed architecture in Figure 2b is simulated with a sinusoidal input. The outputs after digital mixing and the digital-to-analog conversion are shown in Figure 4. The IQ sum has a 6 dB increase in magnitude compared to the signal at the input of each DAC; its noise floor level similarly raises.

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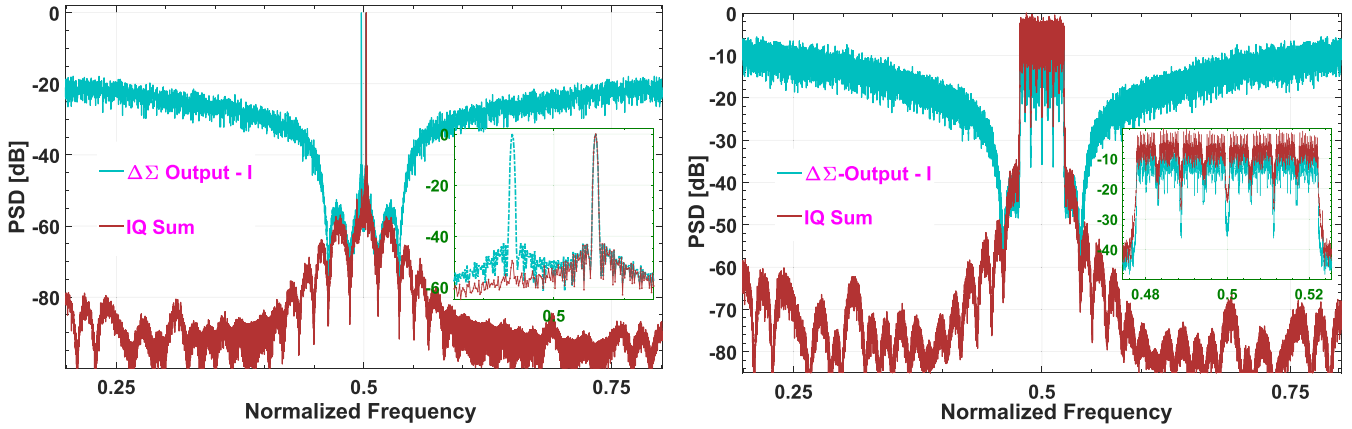

(a) (b)

Fig. 5. Simulation of the HP FIR DAC based proposed architecture with sinusoidal and wideband inputs. The I-path $\Delta\Sigma$ output and the IQ sum are shown in the plots. (a) Sinusoidal input. (b) Wideband input, $osr = 22$.

A close-up around the output carrier frequency, $f_c = f_s/2$, shows both the real signal and the quadrature sum.

C. Architecture Based on 2-Path Parallel 1-Bit HP FIR DACs

Although the basic structure of Figure 2b achieves two-fold sample rate reduction, and by association bandwidth improvement, for the whole architecture, some additional optimization are considered here to take advantage of those improvements.

The image rejection at the analog output is highly affected by timing mismatches and the gain imbalances in the two paths. Calibration circuitry can be added in each path to alleviate these problems. However, the size of these circuitry increases proportional to the effective resolution bits of the DACs. For example, in [8], two 3-bit parallel DACs require a 9-bit DAC for amplitude calibration and timing adjustment is done with 5-bit weighted current sources. Therefore, it is practical to lower resolution bits of the I and Q DACs.

To accomplish this, low-pass $\Delta\Sigma$-modulators can be inserted before the digital mixers. As the number of effective bits at the DACs decrease, the quantization noise increases as is the need for a filtering stage. All these requirements can be addressed adequately by embedding a filtering stage in a low resolution-bits DAC. A 1-bit FIR DAC is inherently linear and has an easy to design transfer function. These attributes make it an attractive choice for this architecture [17]. The other big advantage of the 1-bit FIR DAC is that its structure can be readily modified for quadrature operation by reusing coefficients for both I and Q paths. This is discussed in section IV. The optimized architecture which includes both LP $\Delta\Sigma$-modulators and 1-bit HP FIR DACs is shown in Figure 6.

D. Frequency Planning

In classic architectures where there is a dedicated mixing stage, the output carrier frequency can be translated to any desired band of a given standard by only varying the frequency of the local oscillator (LO). This may not be easily achieved in architectures where clock and LO frequency are closer to each other to compensate for an absence of a steep reconstruction filter [5], [8]. In the proposed architecture, the absence of a conventional frequency translation block demands a change in the frequency plan. This is because the sampling frequency is constrained by both the desired carrier frequency and the baseband sampling rate (f_{s_bb}). It has to be twice the output frequency while the oversampling ratio (OSR) of the interpolation blocks must be a natural number.

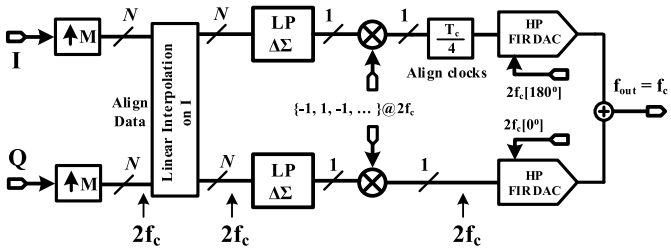

Fig. 6. Proposed transmitter architecture based on 2-path parallel 1-bit HP FIR DACs.

$$f_{s\_bb} = \left(2/osr\right) f_c, \quad osr \in \mathbb{N} \tag{6}$$

To further clarify this problem, the channel arrangement of the 20 MHz bands of the WiFi standard IEEE 802.11n standard will be used. For example, to reach the center frequency for the first channel at 2412 MHz, the DAC clock frequency has to be 4824 MHz. In the proposed architecture, the baseband has to be oversampled by a 241.2. One way to get around this problem is to employ sample-rate conversion in the DSP blocks preceding the LP $\Delta\Sigma$-modulators. Non-integer oversampling ratio between FIR DAC clock frequency and baseband sampling rate can be obtained by inserting fractional interpolator as the cubic Lagrange interpolation filter used in [18].

E. System Validation by Simulation

System-level simulation of the architecture in Figure 6 were carried out to validate the proposed quadrature modulator in a practical implementation. Simulation results for sinusoidal and

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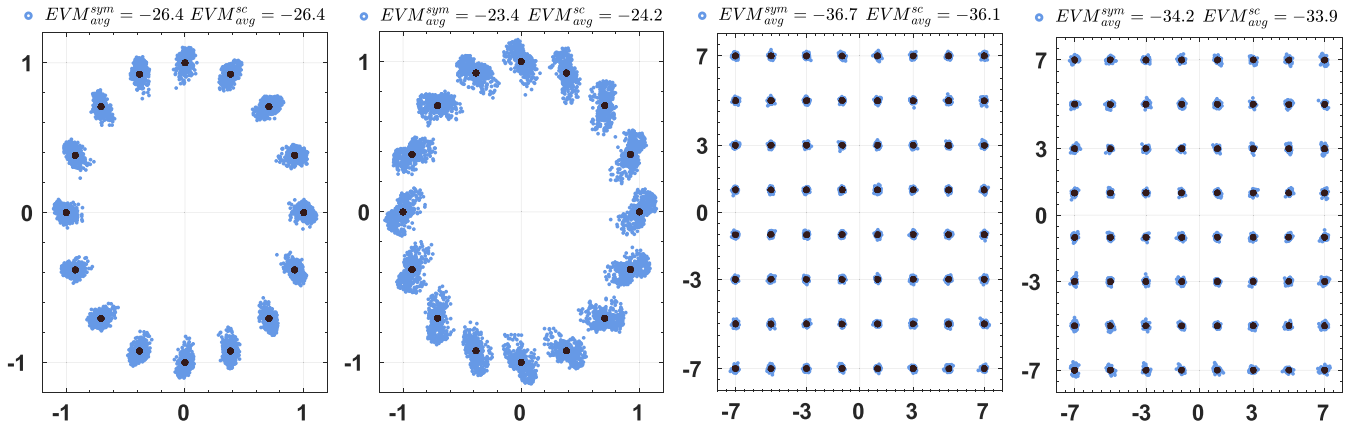
TABLE I

SIMULATED SYMBOL EVM VALUES FOR DIFFERENT MODULATION SCHEMES AND CHANNEL BANDWIDTHS

Channel Bandwidths	**Type of Modulation in the OFDM**					
	QPSK	16-PSK	16-QAM	64-QAM	16-PSK	64-QAM
	no *sinc* distortion				with *sinc* distortion	
20 MHz, osr = 176 64 subcarriers	-37.30 dB	-37.04 dB	-36.70 dB	-36.65 dB	-34.86 dB	-34.23 dB
40 MHz, osr = 88 128 subcarriers	-35.38 dB	-35.27 dB	-34.88 dB	-34.77 dB	-31.58 dB	-30.97 dB
80 MHz, osr = 44 256 subcarriers	-33.35 dB	-33.39 dB	-32.88 dB	-32.95 dB	-27.03 dB	-26.67 dB
160 MHz, osr = 22 512 subcarriers	-26.43 dB	-26.39 dB	-26.18 dB	-26.26 dB	-23.37 dB	-22.91 dB



(a) no sinc distortion (b) with sinc distortion (c) no sinc distortion (d) with sinc distortion

Fig. 7. Simulation of the proposed HP FIR DAC based architecture: (a) & (b) are simulated with 16-PSK–modulated 160 MHz channel bandwidth ($osr = 22$) 512-subcarrier OFDM input signal, and (c) & (d) are simulated with 64-QAM–modulated 20 MHz channel bandwidth ($osr = 176$) 64-subcarrier OFDM input signal.

wideband input signals are shown in Figure 5. The single-tone input signals are generated in Matlab® using readily available functions whereas IEEE 802.11ac WiFi baseband signals are used for wideband simulation. The simulation was carried out using OFDM wideband input signals; and the symbols are generated according to the spacing and placement of the subcarriers of the 160 MHz, IEEE 802.11ac standard. Design of the LP $\Delta\Sigma$-modulator and its simulation are based on the functions and modulator topologies from the Schreier Toolbox [19].

Both inputs in Figure 5 are oversampled by 22 with a half-band filter chosen as a first stage interpolation filter. A cascade-of-resonators, feedback form (CRFB) topology was selected for realizing the 4^{th}-order, 1-bit LP $\Delta\Sigma$-modulator. The 1-bit HP FIR DAC has 8-bit resolution coefficients and is designed for less than 0.5 dB in-band ripple and a 60 dBr stopband rejection.

The frequency response in Figure 5a is run in ideal case, with no gain mismatch between the two-paths, and it shows a rejection of the image to below the noise level. The rising quantization noise is also canceled by the HP filtering in the DAC. In the wideband case of Figure 5b, the signals at the input of the DAC in the I-path and at output of the DACs are shown. A zoom in the center of the band shows the difference in levels due to the summation operation at the output of the DACs. Moreover, it can be seen that the real signal has a symmetric spectrum unlike the quadrature output signal. Some computational techniques could be used to increase the rejection level, but the obtained results are enough to validate the proposed architecture at system-level.

Error vector magnitude (EVM) simulation results for four different modulation schemes (QPSK, 16-PSK, 16-QAM, and 64-QAM) and four different channel bandwidths of the IEEE 802.11ac WiFi standard (20 MHz, 40 MHz, 80 MHz and 160 MHz) are shown in Table I. To obtain accurate values, large number of simulations were run and the average EVM values of all symbols of a particular modulation scheme and channel bandwidth were calculated. For example, for the case of the 20 MHz channel bandwidth, 160 simulations were run for each of the values in the first row of Table I. The number of simulations were reduced for the other channel bandwiths in a ratio proportional to the number of subcarriers in their symbols. The constellation diagrams in Figure 7 are plotted by superimposing all the symbols of that particular run. Four different FIR DAC coefficient sets were used and each of them were designed for 8-bit coefficient resolution and 60 dBr stopband rejection. The DSP blocks were the same as in the previous simulations. The EVM simulation results show the capability of the architecture to transmit with high modulation accuracy. Example constellations are shown in Figures 7a and 7c. Both symbol EVM and subcarrier EVM are below -26 dB even for the case of the 160 MHz,

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TABLE II
SINC DISTORTION AT DIFFERENT CENTER FREQUENCIES

Parameters	Center frequency, f_c			
	$f_s/8$	$f_s/4$	$3f_s/8$	$f_s/2$
In-band ripple [dB] $bandwidth = f_s/22$	0.18	0.30	0.59	0.70
Power loss for a single-tone at f_c [dB]	-0.22	-0.91	-2.11	-3.92

512-subcarrier OFDM input signal. The IEEE 802.11ac standard requires a maximum EVM of -22 dB with a 64-QAM modulation scheme.

III. DISCUSSION ON NON-IDEALITIES

The proposed architecture has merits in that it reduces the required sampling rate for a desired output carrier frequency. The complete system is also amenable for an almost all-digital implementation. Nevertheless, those gains come with some drawbacks; they are be discussed in this section.

A. Sinc Distortion

The output frequency components of a non-return-to-zero (NRZ) DAC are attenuated by a sinc response which has nulls at multiples of the DAC sampling frequency. Table II gives attenuation values for four different center frequencies. Signals at $f_s/2$ experience higher output power losses compared to those at lower carrier frequency. Due to its importance in the HP operation, the effect of sinc distortion is simulated for different scenarios. For wideband input signals, sinc distortion results in a ripple across the passband. The ripple increases as the passband widens as in the case of a larger channel bandwidth. To quantify this effect, the in-band ripple experienced by the 160 MHz channel bandwidth for transmissions at different locations of the first Nyquist zone are tabulated in Table II. The difference in in-band ripple between a transmission at $f_c = f_s/4$ and $f_c = f_s/2$ is around 0.4 dB.

The impact of this increased in-band ripple on the value of the output quadrature signal constellation error of the proposed architecture was simulated for four different channel bandwidths and two different modulation schemes. The EVM values in Table I shown a degradation of more than 2 dB in all of the channel bandwidths and, as expected, a slight loss of modulation accuracy with the 64-QAM modulation scheme. Two example constellation plots which are simulated by considering the effect of sinc distortion are shown in Figures 7b and 7d. The EVM of 20 MHz channel loses 2.4 dB of accuracy in the 64-QAM modulation case while the 160 MHz channel bandwidth loses around 3.0 dB in the 16-PSK modulation scheme.

B. IQ Imbalance

Ideally, the gain difference and phase mismatch between the I and Q channels should be zero. Any imbalance in the two signal paths increases the power of image replicas. This is mostly worrisome in the HP operation as the desired signal and its image are close to each other; and filtering the undesired component in the absence of full rejection becomes difficult. Since attenuation of the replica below the noise level is not always achievable, calibration circuitry has to be added.

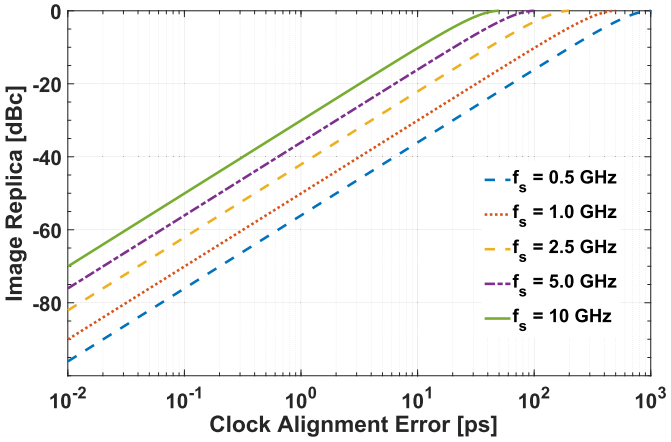

Fig. 8. Effect of timing errors on the magnitude of the image replica at different clock speeds.

One of the biggest source of phase mismatch between I and Q paths is the clock distribution circuitry. The two clocks are designed for a 180° phase separation. However, due to mismatch in routing, devices in driver circuits and other reasons, imperfection in clock alignment occurs. This timing error creates a cosine distortion. For a 2-path parallel DAC, the degradation in the nyquist image replica rejection can be calculated by the following ratio between the magnitudes of the image replica and the desired signal [12], [15]:

$$\frac{Image}{Desired\ \ Signal} = \left| cos\left(\pi \frac{\Delta T_e}{T_s}\right)\right| \tag{7}$$

Where T_s is the period of the clocks of the HP FIR DACs and $\Delta T_e/T_s$ is 0.5 when the clocks of the two DACs are perfectly aligned. The suppression of the image replica degrades to -16 dB, for example, if the alignment between the two clocks is $\pm 18°$ away from the desired phase difference of 180°; and the image can be reduced by more than -56 dB for smaller than 0.1% timing errors. Although a 0.1% timing error is a hard requirement at GHz clock speeds, this is in line with current developments [20]. For example, calibration down to 0.013% timing error at a clock rate of 2GS/s has been demonstrated in 130nm BiCMOS technology [8]. The same tuning resolution can be used at 4 GS/s clock speed with only 6 dB deterioration in the timing error limited SFDR. In Figure 8, the magnitude of the image spur that arises due to non-ideal clock alignment is plotted for different clock speeds. Moreover, the timing accuracy required to reach a certain linearity requirement can also be extracted from the figure. Hence, calibration circuitry can be added depending on the clock rate and SFDR requirements.

The other type of imbalance arises due to gain difference. In the proposed architecture, this non-ideality is simulated by dividing it into two components. One is a constant which represents the systematic difference between the two gain paths.

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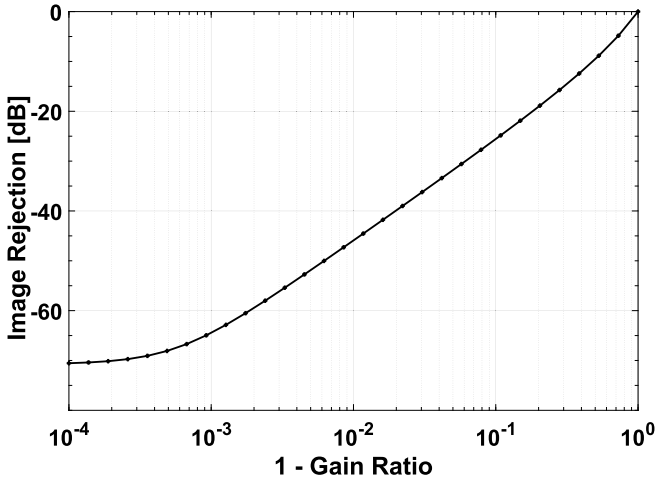

Fig. 9. Effect of gain difference in I and Q paths on image replica rejection. Gain ratio is equal to $gain_I/gain_Q$.

It is a non-zero scalar value equal to $gain_I/gain_Q$. The other is a random quantity that is caused by randomly-distributed variations within the gain elements of each channel.

The first type of gain imbalance is simulated for the basic architecture in Figure 2b as the impact of the LP $\Delta\Sigma$-modulator and the HP FIR DAC is non-consequential. The result is plotted in Figure 9. It shows that for $gain_I/gain_Q = 0.8$, the image replica is suppressed by close to -20 dB compared to the desired signal. Attenuation level of -70 dB is reached at less than 0.1% gain error.

C. Random Coefficient Mismatch

The main source for the random component of the gain error is the FIR DAC. It has gain elements, the coefficients, which normally are implemented using analog circuits. The values of these coefficients are prone to random mismatches [21] and [22]. To evaluate the impact of this type of mismatch on the performance of the transmitter, its effect on the FIR DAC response is first derived. An FIR filter output is given by the following equation:

$$y[n] = \sum_{k=0}^{N-1} c_k x[n-k] \tag{8}$$

Where c_k are the coefficients and N is the length of the filter. The filter transfer function for a general input $x[n] = e^{-j\omega n}$, where $-\infty < n < \infty$ is:

$$H(\omega) = \sum_{k=0}^{N-1} c_k e^{j\omega k} \tag{9}$$

If each c_k has a mismatch generated error ϵ_k, then the error transfer function can be written as:

$$H_e(\omega) = \sum_{k=0}^{N-1} \epsilon_k e^{j\omega k} \tag{10}$$

The filter magnitude response variation due to coefficient mismatch error is derived in [23] with the assumption that ϵ_k are uncorrelated Gaussian random variables which are identically distributed with zero mean and standard deviation σ_ϵ:

$$|H_e(\omega)| = \frac{\sqrt{\pi N}}{2}\sigma_\epsilon \tag{11}$$

While this equation is important in the characterization of FIR DAC coefficient mismatch errors, it is derived based on the coefficient being implemented as a lumped component. It fails to take into account that coefficients are usually implemented by replicating a single unit coefficient. For example, in a current-steering FIR DAC implementation, the larger coefficients are implemented as a integer sum of the unit coefficient. For coefficients larger than the unit coefficient, a standard deviation which is representative of the errors of all the coefficients should be taken. A slight modification can be applied to this equation to account for this difference that arises during implementation. If all the unit coefficients have errors that are uncorrelated Gaussian random variables which are identically distributed with zero mean and a standard deviation of σ_u, then a coefficient with a c_k unit coefficients has a standard deviation of $\sigma_u\sqrt{|c_k|}$. An average standard deviation of all the coefficients which are implemented with unit coefficients can be found from the pooled variance as:

$$\sigma_{ave} = \sqrt{\frac{\sigma_u^2|c_1| + \sigma_u^2|c_1| + \ldots + \sigma_u^2|c_N|}{N}} \tag{12}$$

The error on the magnitude response can then be modified to

$$|H_e(\omega)| = \frac{\sqrt{\pi N}}{2}\sigma_{ave} \tag{13}$$

A new formula for estimation of magnitude variation due to coefficient mismatch and more suitable to a current-steering FIR DAC implementation can then be found using:

$$|H_e(\omega)| = \frac{\sqrt{\pi \sum_{k=1}^{N} |c_k|}}{2}\sigma_u \tag{14}$$

This formula helps predict the passband and stopband ripples for a given standard deviation of the unit coefficient. It takes a circuit-level value and shows its effect on a system-level specification. If there is a specific transmit mask or an out-of-band noise profile that has to be respected, (14) can be used to estimate the random mismatch of unit coefficient required. It is also possible to simulate the impact of unit coefficient random mismatch errors on the quality of the final transmitted signal at the output of the proposed architecture in Figure 6 as opposed to their effect on the response of the embedded filter. This is carried out using a 512-subcarrier, 16-QAM modulated, 160 MHz OFDM input signal. Each of the coefficients in the 63-long filter are generated 800 times with a uniform distribution whose mean is the coefficient value in the original set and for a selected number of standard deviation values from $\sigma_u = 0.1\%$ to $\sigma_u = 15\%$. Hence, for one σ_u value, there are 800 coefficient sets. The modulation accuracy of the transmitter output for each of the coefficient sets are estimated by averaging over four OFDM symbols. The histogram in Figure 10 shows the EVM values for each value of the set for four different values of standard deviation. To decrease the likelihood of failure in the stability of the

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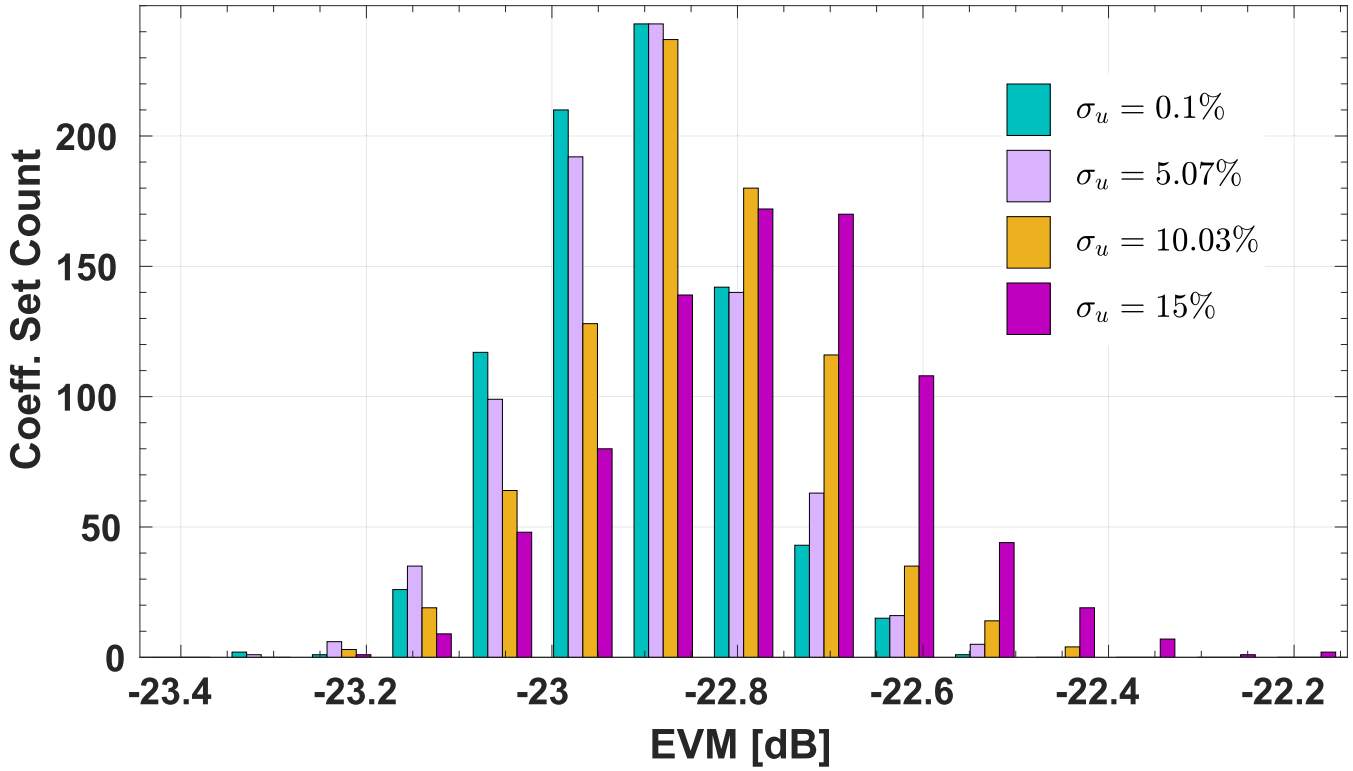

Fig. 10. Effect of coefficient mismatch on EVM for four different values of standard deviations. Simulation was carried out with 16-QAM–modulated 160 MHz channel bandwidth ($osr = 22$) 512-subcarrier OFDM input signal.

$\Delta\Sigma$ modulator, the peak amplitude of the input signals were reduced for this simulation. Hence, the general reduction of around 4 dB in the average EVM value compared with the result reported for 16-QAM modulated 160 MHz channel in Table I.

For each increment in σ_u value, the average EVM corresponding to that standard deviation degrades by a small margin. The bars, in Figure 10, corresponding to the higher standard deviation value increase as the EVM values decreases and those of the lower standard deviation increase as the EVM improves. Nonetheless, the difference of EVM of each coefficient set in each σ_u value from the average value of the group is not more than 0.5 dB. More importantly, as the random coefficient standard deviation varies from 0.1% to 15%, the EVM is degrading by only 1 dB.

It has been argued that the 1-bit FIR DAC has an inherent linearity against random coefficient mismatches because of the inherently-linear 1-bit DACs it realizes at each tap [22]. The coefficient errors merely result in changes in the stopband level of the FIR DAC transfer function with minimum ripple in the passband of the filter. The results in Figure 10 further solidify this strength of the 1-bit FIR DAC.

IV. Circuit Level Challenges

In the previous sections, the strength and drawbacks of the proposed transmitter architecture have been clearly analyzed with the support of system-level simulation results. In this part, the key blocks of the proposed architecture are examined from a circuit-level of abstraction.

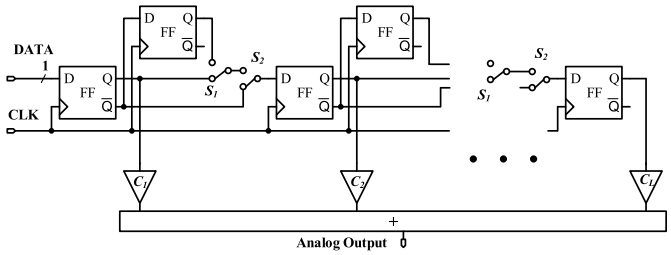

Fig. 11. Configurable delay line for FIR DAC center frequency translation.

A. HP FIR DAC Topologies

FIR DACs in communication circuits are designed such that: the stopband rejection can meet a desired out-of-band noise profile, as formulated in (14); the passband ripple would not be large enough to deteriorate the EVM; and the transition band would always be below the transmit mask of the standard. The designed FIR DAC coefficients are quantized such that each are integer multiple of the absolute value of the smallest coefficient. This is done to improve matching in layout because the smallest coefficient can be taken as a unit cell with which the other coefficients are implemented. Quantization level of the coefficients is an important parameter as it can considerably change the total silicon area required to implement the FIR DAC. Since it also degrades the stopband attenuation, the optimum level of quantization should be selected [22].

FIR DAC bandwidth is calculated from the ratio of f_s and osr. However, its center frequency can be at DC, low pass (LP); at $f_s/4$, bandpass (BP); or at $f_s/2$, HP. Once the frequency response is designed, the center frequency can

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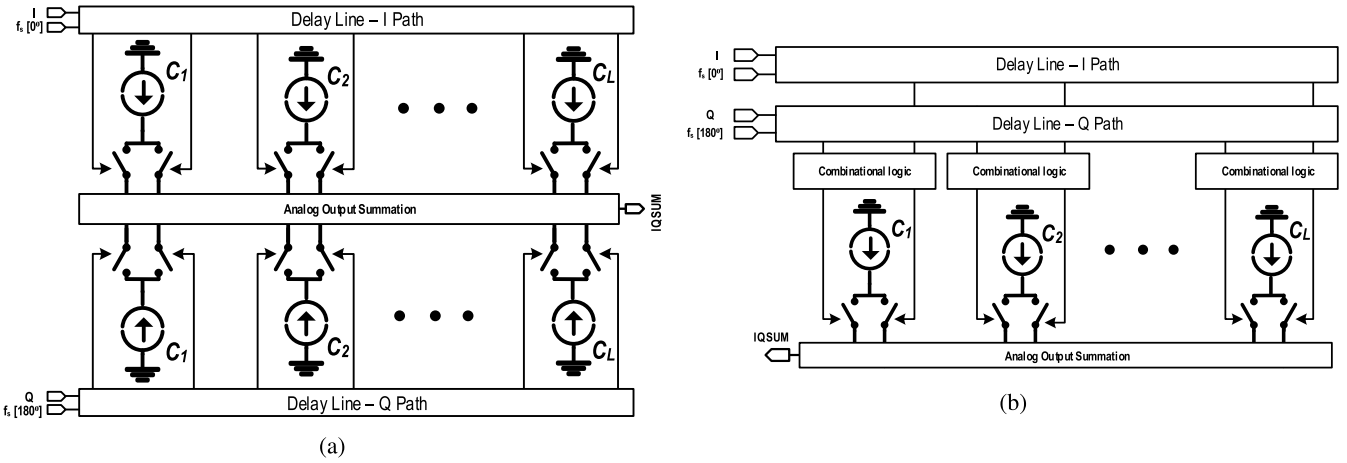

Fig. 12. Realization of the 1-bit FIR DAC blocks in the proposed architecture. (a) Two DACs. (b) Quadrature.

TABLE III

SWITCH STATES OF CONFIGURABLE DELAY LINE FOR TRANSLATION OF THE 1-bit FIR DAC CENTER FREQUENCY. POSITIONS OF THE SWITCHES IN FIGURE 11 ARE CONSIDERED AS 1

Frequency Response	**Switch,** S_1	**Switch,** S_2
LP FIR DAC	1	0
HP FIR DAC	X	1
BP FIR DAC	0	0

be translated using only the delay line of the FIR DAC. The configurable delay line shown in Figure 11 can be used to translate the frequency response of the coefficients by configuring it according to Table III.

The HP FIR DAC can be obtained by inverting the sign of every other coefficient of an LP FIR DAC. At circuit level, this transformation can be carried out for a 1-bit FIR DAC at the delay line by alternately propagating the inverted and non-inverted outputs, as shown in Figure 11. Naturally, each of the 1-bit HP FIR DACs in the proposed architecture can be implemented by using a single delay-line, and as many coefficients as the length of the embedded filter. The quadrature output is then obtained as a sum of the outputs of each DAC as in Figure 12a. However, they can also be optimized for a quadrature implementation by using a single set of coefficients as depicted in Figure 12b. In the latter case, the 1-bit signals at the output of the delay lines of each channel can be passed through a logic block to generate 1.5-bit control signals of a common coefficient set. These two realizations have difference in their power consumption, susceptibility to distortion, area and output power. The following qualitative comparison draws knowledge from a HP FIR DAC implementation whose experimental results are presented in the last section.

Concerning occupied area, the number of analog elements required for implementing the HP FIR DAC coefficients can be halved in the quadrature structure. However, to keep the same output power, the coefficients have to be implemented with twice the size of the coefficients in the two DACs structure. Still the required number of auxiliary components, for example drivers, can be halved in number. With respect to speed, the delay lines of each structure are clocked at $2f_c$ whereas the 1.5-bit control signals in the quadrature FIR DAC will effectively be sampled at four times the output carrier frequency. While the number of circuit elements will be higher in the two DACs approach, the speed of operation of most of the elements in the quadrature case will be doubled. Therefore, the total power consumption difference of the analog components between the two approaches may not be significant. Power consumption related to clock distribution network is minimized in the quadrature case owing to the fact that there are fewer switched current source elements (which implement the coefficients) and the clock speed need not change as both the rising and falling edges of the clock can be employed to resample the 1.5-bit control signals.

The quadrature implementations has lower gain imbalance over the two DACs implementation because the I and Q paths share the main gain elements. Similarly, the quadrature realization does not need power combining network unlike the two DACs realization of Figure 12a. Effect of random device mismatch errors are also reduced for the quadrature case for the fact that there are fewer elements and there is flexibility to design them with big area. Distortion caused by timing errors related to the 1.5-bit coefficient realization (for instance, a tri-state current source) will be significant in the quadrature structure [24], [25]. This distortion can be minimized if instead of turning off both switches at the same time, the third state is realized by simultaneous turning-on of both differential switches as the net output will still be zero. On the other hand, distortion caused by phase imbalance between the outputs of each DAC is higher in the two DACs topology. The delay between rising edges of the clock at different switches of the UCCs is likely to create some loss of linearity as the number of UCCs that it has to be distributed to increases. The two DACs topology suffers more from this than the quadrature. If calibration circuitry is to be employed, and it is a must to achieve high linearity at GHz carrier frequencies, it is likely

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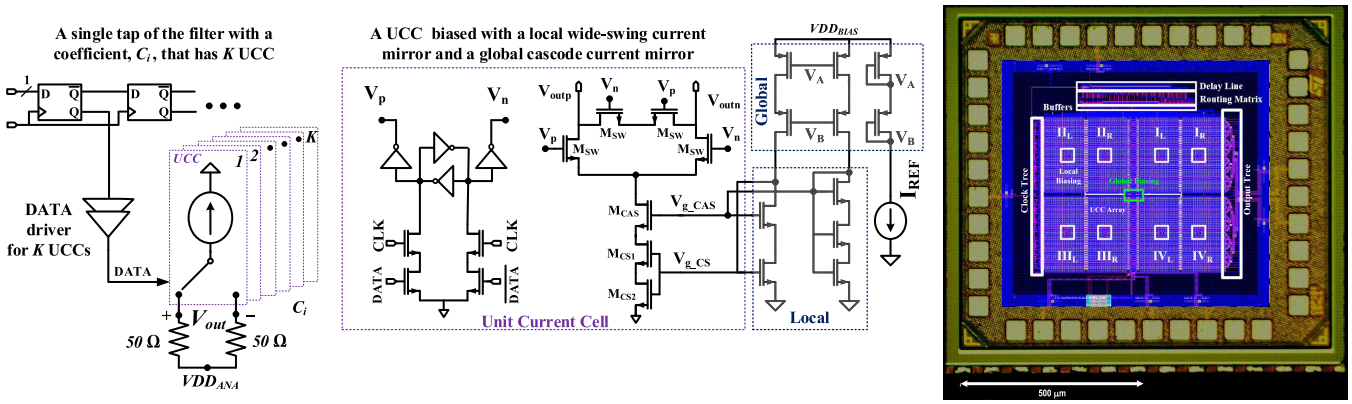

(a) (b)

Fig. 13. Implementation of the single-channel 1-bit HP FIR DAC in CMOS 28nm FDSOI. (a) A single-tap where coefficient C_i has K UCC. (b) Die Micrograph with the layout-view of the chip in-set.

to be implemented for each UCC. Thus, the reduced number of calibrated UCCs, which the quadrature topology offers, could overall be a better design choice than what the two DAC topology offers. At sub-GHz output frequencies where the need for complex timing calibration circuitry is minimal, the more linear UCC design in the two DAC topology can be employed to increase the output signal dynamic range.

B. Integration of the Proposed Transmitter Architecture

The proposed architecture is amenable for almost all-digital implementation. It can be used to implement low power, medium range wireless transmitter such as WiFi transmitters. To target bands of IEEE 802.11ac at around 5 GHz, the $\Delta\Sigma$ modulator and the HP FIR DAC need to function at least at a clock frequency of 10 GHz. This requirement is achievable at least for the digital parts of the architecture. There has been recent works on $\Delta\Sigma$ modulators which demonstrate those capabilities. In [26], operation up to 11 GS/s has been demonstrated for a time-interleaved $\Delta\Sigma$ DAC in 65nm CMOS technology.

Filtering DACs have not been commonly employed in high speed data conversion. There has been FIR DAC examples at medium speeds as in [27], or as a bandpass filter in a configurable transfer function power-DAC [28] or as part of an RF DAC in [5], but rarely a HP FIR DAC implementation. Therefore, there are not enough examples in literature that can be used to discuss the analog parts of the proposed architecture. To give an all-rounded perspective of the proposed architecture, some experimental results from a single-channel, 1-bit input HP FIR DAC implementation in 28nm CMOS FDSOI are included in the next subsection.

C. Experimental Results From a HP FIR DAC Implementation

Objectives of a current-steering FIR DAC design are reduction of static coefficient mismatches and dynamic switching errors. In such a long filter implementation, an additional challenge is to find a layout placement method that can mitigate timing errors and bandwidth limitations that result due to the relatively large area occupied by randomly-valued coefficients.

A pseudo double common centroid placement method is adopted [29]. The unit current cell (UCC) array is divided into four quadrants. As the filter has a symmetrical impulse response, the placement in each sub-quadrant is a mirror of its adjacent one. A binary clock tree of seven stages with a fan-out of four distributes clocks to the 64 row UCC array horizontally. A matching binary output tree is used to collect the differential output currents. To decrease IR-drop across UCC array, biasing is supplied at each sub-quadrant with a modified wide-swing current mirror and a global cascode current mirror circuits.

The UCC is implemented using a differentially-switched cascode current source shown in Figure 13a. To achieve lower timing errors, each UCC has a dedicated high speed latch for synchronization of data signals near the current source switches. To prevent simultaneous turn-off of current sources switches, high data crossing is achieved by adding an inverter to the low-crossing outputs of the latch [30]. Dummy switches are inserted to lower charge injection due-to gate-to-drain parasitic capacitance. Stabilization of supplies in the UCC is ensured with a local decoupling capacitor.

The 1 mm^2 HP FIR DAC chip is shown in Figure 13b. Active area is 0.3 mm^2. The die is mounted using a QFN40 open-cavity plastic package on a test board. The load resistors are off-chip and are connected to a 1.2 V analog supply voltage (VDD_{ANA}). The digital circuits can operate with, $0.6\ V \leq VDD_{DIG} \leq 1.325\ V$. The bias circuits require a minimum of 1.2 V voltage supply, VDD_{BIAS}, and it is provided separately. The results in Figure 14 are obtained with a digital supply voltage of 1 V. The total UCC load current is 14.1 mA while the digital parts of the UCC array, the delay line, routing matrix, and all the clock and data buffers consume 19.4 mA at a clock frequency of 600 MHz.

To determine the shape of the transfer function, measurement is carried using a 1-bit PRBS data which has a pattern cycle period of $2^{23}-1$ and a mark density of $1/2$ at multiple clock frequencies. The 1-bit random pattern was directly fed to the HP FIR DAC without any digital processing and was clocked at a fraction of the FIR DAC update rate. The result

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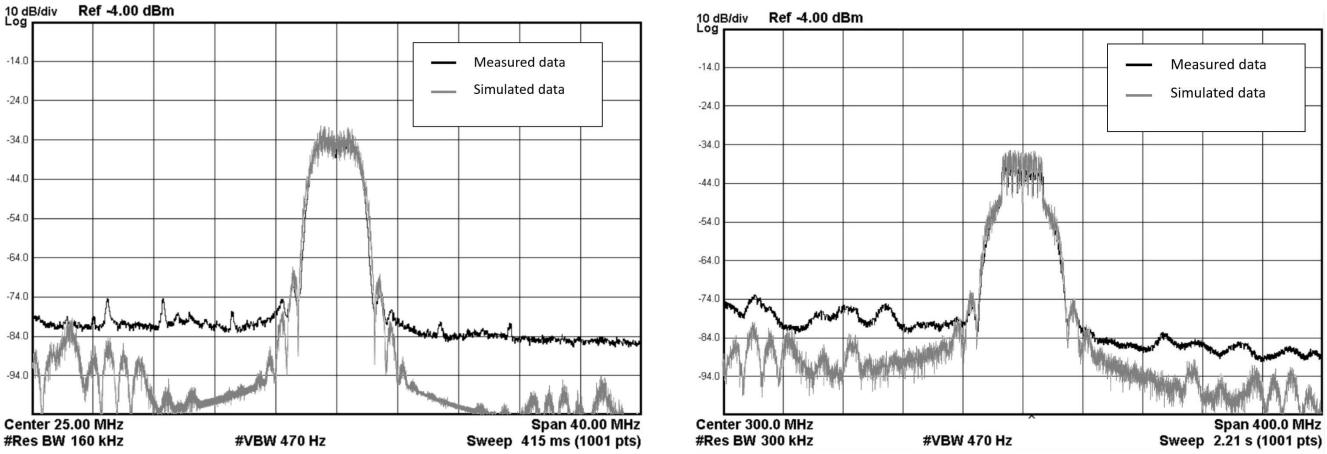

Fig. 14. Experimental results of a single-channel 1-bit HP FIR DAC. (a) PRBS input clocked at $f_s/11$, f_s being the FIR DAC update rate. (b) Wideband input, $osr = 22$.

TABLE IV
COMPARISON OF THE 1-bit HP FIR DAC WITH THE STATE-OF-THE-ART DRFCS

Parameters	Units	[1]	[31]	[32]	[33]	[5]	This Work
Clock Speed	MHz	200	245.7	NA	128	250	600
Bandwidth	MHz	16.6	5	20	18	15	27.3
Max. Output Power	dBm	NA	NA	6	8 ‡	NA	6
OOB Rejection ‖	dBc	-44 †	-64	-55	-47	NA	-50
Channel Power	dBm	-23@2.46GHz	NA	4@1.88GHz	1@1GHz	NA	-20@300MHz
Noise Floor	dBm/Hz	-139@20MHz	-158@240MHz ¶	-158@80MHz ¶	-155@45MHz	-126 †	-143@200MHz
from P_{out} of	dBm	-23	1	0	1	-5.4	-20
Power Consumption	mW	60.5	29.6 ‡	98	41.3 ‡	122	36.3
Active Area	mm^2	0.7	0.4	1.3	0.25	0.23	0.3
Supply Voltage	V	1.2	1.1/1.8	1.8	0.9/1.8	2.5	1/1.2
Process	nm	130	45	55	28	250	28
Type of DAC	–	8-bit DDRM	12-bit DAC §	10-bit DAC §	10-bit QDAC	1-bit FIR RF DAC	1-bit HP FIR DAC

† Estimated from plots ‡ Includes pre-power amplifier § Analog transmitter architecture

¶ With high-order baseband reconstruction filtering ‖ or the reported alternate ACPR

in Figure 14a shows a stopband rejection of up to 50 dB. The filter maintains a mean passband ripple of 4.2 dB up to 1.4 GHz clock frequency.

The noise spectral density is limited at lower frequencies by the combined performance of probes and measuring instrument. However, the noise floor reaches -143 dBm/Hz at 200 MHz away from the center of the channel in the right side. The plots in Figure 14 are not externally filtered as no off-chip filter is employed. The filter in the output signal measurement probes had a flat 0 dB passband up to around 7 GHz.

The baseband OFDM signals used for wideband measurement of Figure 14b is obtained from an IEEE 802.11ac waveform generator at an input sampling rate of 160 MHz. The input data are processed using the Matlab® model of Figure 6 and the pattern at the digital mixer output is used for testing. The rising quantization noise from the $\Delta\Sigma$ modulator is filtered by up to 47 dB in the adjacent channel and by more than 50 dB in the far-out spectrum. Although the filter maintains a flat passband, the effect of the zero-order hold clocking can be seen in the difference between the attenuation of the upper and lower out-of-band noise components. The chip has a logical error which degrades the waveform and creates sidelobes around the channel as can be seen in Figure 14b. The error was modeled and the transfer function has been validated by retro-simulating the chip output with the model. The simulation results are superimposed in both spectrums of Figure 14 and they reveal that the measured results are very close to the simulated behavior.

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TABLE V
COMPARISON OF THE PROPOSED ARCHITECTURE WITH EXISTING TRANSMITTER ARCHITECTURES

REF.	Architecture	DAC	OOB noise filter	Output Freq.	Mixing Stage
[32]	Traditional analog	N-bit DAC at f_{CLK} §	Biquad + RC	f_{LO}	analog mixing with f_{LO}
[2]	Quadrature DRFC	N-bit DAC at f_{CLK} §	Kth-order LC BP filter §	$f(f_{CLK}, f_{LO})$ †	analog mixing with f_{LO}
[10]	All-digital	NA	No filtering	$f_c = f_{CLK}/4$	1-bit digital mixer at f_{CLK}
[8]	TI RF-DAC	N-bit TI $\Delta\Sigma$ DAC at f_{CLK} §	$sinc(x)$	$f_c = f_{CLK}/2$	M-bit digital mixer at $2f_{CLK}$ §
[17]	Traditional with FIR DAC	1-bit LP FIR DAC	Lth-order embedded FIR §	$f(f_{CLK}, f_{LO})$ ‡	analog mixing with f_{LO}
Proposed	2-path TI HP FIR DAC	1-bit HP FIR DAC	Lth-order embedded FIR§	$f_c = f_{CLK}/2$	Embedded in digital process

§ $N, K, M, L > 1$ † $f_c = f_{LO} \pm f_{CLK}/4 + \Delta f$, $\Delta f \ll f_{CLK}$ ‡ Due to $\Delta\Sigma$, $f_{LO} = q * f_{CLK}$, $q \in \mathbb{N}$

D. Comparison With the State-of-the-Art

Since filtering DACs are not commonly used in transmitters, readers may find it difficult to find a place for the HP FIR DAC in the general spectrum of DRFCs. In Table IV, the 1-bit HP FIR DAC is compared to state-of-the-art DRFCs at moderate operating clock speeds. Works that implement both analog and digital transmitter architectures are selected. Furthermore, most of them have wireless communication standards as their target applications. Some performance metrics are not included since the measured chip is only single-channel HP FIR DAC. In addition, the values of some parameters, such as power consumption and area, are added without a caveat. Although the selected works implement I/Q modulators, the power consumption of the 1-bit FIR DAC is also not far from what the proposed modulator would consume if it were to be implemented in the quadrature DAC topology. The only difference would be the power consumption of the second delay line and the fact that the latches would switch at twice speed to drive 1.5-bit UCCs. However, the contribution of these to the reported 36.3 mW would be minimal as the delay line and the UCC latches consume a small percentage of the total. Similarly, the area of a quadrature topology HP FIR DAC would be almost equal to that of the 1-bit HP FIR DAC as an additional delay line occupies only a small percentage of the total active area.

In Table V, the proposed architecture is qualitatively compared with existing analog and digital transmitter architectures. The main differences among existing solutions tend to be on the digital-to-analog conversion and the mixing stage. These two are separately compared. The proposed architecture utilizes inherently linear 1-bit DACs and avoids problems associated with an up-conversion circuit by embedding simple 1-bit mixers in the digital signal processing chain. As transmitter co-existence is important, the existing OOB noise filtering mechanisms are also compared. The proposed architecture offers a mixed-mode embedded filtering scheme which can expected to be more compact than high-order analog reconstruction filtering and more effective than $sinc(x)$ filter. Unlike in other architectures, the output frequency is defined only by the clock. High carrier frequency can be reached by up-conversion mixing with an LO. This may not be easily achieved in architectures where clock and LO frequency are closer to each other to compensate for an absence of a steep reconstruction filter. In summary, the tables show the compatibility of the HP FIR DAC based architecture for low supply voltage advanced CMOS implementation. They also demonstrate that the proposed architecture is fit for broadband transmissions at optimum cost of power and silicon area.

V. CONCLUSION

This paper presents a novel all-digital transmitter architecture. It is based on two-path parallel digital-to-analog converters (DAC) which are driven by two 180° phase-shifted clocks. To decrease the number of analog unit current cells in the converter, a LP $\Delta\Sigma$-modulator is used. Since the modulator also converts the input resolution to 1-bit, an inherently-linear digital-to-analog conversion is realized by embedding filtering in the DAC. The FIR DAC transfer function is designed to cancel the $\Delta\Sigma$-modulator quantization noise. The architecture extends the output carrier frequency to half the DAC clock rate. Simulation results at system and circuit levels are used to validate the system. They demonstrate the robustness of the architecture against random coefficient mismatches and its suitability for broadband operation. Experimental results are also presented to discuss the validity of the proposed all-digital transmitter architecture at circuit level.

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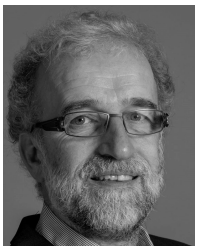

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Abstract

This manuscript provides an overview of the results of research conducted for over 10 years. It covers a selection of contributions to digital RF transmitters and baseband circuits for mmW receivers. Highlighting the main challenges of these topics leads to the description of concepts that are then demonstrated using integrated circuits and systems. The description of the various works is supported by a reproduction of publications in major journals and conferences of the field.

Following the description of the scientific contributions, some research perspectives are developed around energy-efficient circuits for smart embedded devices. Since artificial intelligence and the Internet of Things are about to merge, it is necessary to integrate the process of analysis and decision as close as possible to the source of data, by developing efficient and low-power hardware components. The proposal is to study event-driven circuits for near sensor computing to enable ultra-low-power always-on wake-on-feature system.

Finally, the manuscript also presents a more exhaustive vision of research, supervision, teaching and involvement in the academic and industrial context.

Résumé

Ce manuscrit offre un aperçu des résultats des recherches menées depuis plus de 10 ans. Il couvre une sélection de contributions aux émetteurs RF numériques et aux circuits en bande de base pour les récepteurs mmW. La mise en avant des principaux défis liés à ces sujets mène à la description de concepts qui sont ensuite démontrés à l'aide de circuits et systèmes intégrés. La description des différents travaux est étayée par une reproduction de publications dans des revues et conférences majeures du domaine.

Suivant la description des contributions scientifiques, certaines perspectives de recherche sont développées autour de circuits énergétiquement efficaces pour les systèmes intelligents embarqués. L'intelligence artificielle et l'Internet des objets étant sur le point de fusionner, il est nécessaire d'intégrer le processus d'analyse et de décision le plus près possible de la source des données, en développant des composants efficaces et peu consommateurs d'énergie. La proposition consiste à étudier les circuits pilotés par événements pour le calcul à proximité de capteurs afin de mettre en place un système de veille intelligent.

Enfin, le manuscrit présente également une vision plus exhaustive des activités de recherche, d'encadrement, d'enseignement et l'implication dans le contexte académique et industriel.