# Analysis and performance improvement in high frequency wide-band LNAs

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## In English

In this thesis three different approaches are presented in order to improve the performance of high frequency wide band LNAs. In the first approach, a new procedure for the design of multi stage LNAs with consideration of following stages noise is presented. This approach and its results has been previously published in [32]. In this approach, a new analytical solution for designing first stage of multi stage LNAs is presented. Conventional methodology for LNA design is to set source reflection coefficient of first stage equal to its $\Gamma_{opt}$ to achieve minimum possible NF. At RF and microwave frequencies, because of transistor's gain roll-off, to achieve the desired gain, multi-stage LNA is often required. In these cases, the design procedure is much more complicated due to following stage's noise factor and the effect of first stage's gain on overall-NF. To find optimized value for first stage's source admittance to achieve minimum overall-NF, optimum source impedance of first stage should be obtained by consideration of its gain and NF as well as the effect of following stages' noise. In this thesis, the analytical calculations for obtaining the optimum source impedance of first stage to achieve simultaneously noise and impedance matching as well as best gain and overall NF performance in multi stage LNAs is presented. By using these equations, numerical solution for optimum design of first stage in multi-stage LNAs can be obtained. This method can be used for optimization of gain and NF simultaneously. The analytical solution shows consideration of overall LNA in optimization of gain and NF, leads to improvement of its performance.
To validate the theoretical results and check the feasibility of proposed method and also its comparison to the traditional approach, two different LNAs with conventional and proposed approach have been designed using ADS. These LNAs are two stages LNAs. To be consistent, the second stage remains the same and the first one is optimized through traditional approach and the proposed one respectively. This stage is chosen to present relatively high NF to emphasize the effect of the change in $\Gamma_{opt}$ in multistage LNAs by considering the following stages' effect. The performance comparison is done according to momentum simulation in ADS and the results confirm the proposed method's perfor-

mance improvement in comparison to conventional design method. The designed LNA with proposed method shows lower NF and higher gain according to ADS momentum simulation in comparison to conventional method because it have better input impedance optimization. The LNA with better performance (proposed approach) is fabricated in order to confirm the validity of theoretical calculations. The results show the improvement in the performance of the proposed approach compared to conventional design method. It has been shown, despite slight increment in first stage's NF, the overall NF decreases due to higher first stage gain. Measurement results confirm the performance of designed LNA with proposed approach.

The second approach concerns about parallel amplifier usage for LNA design. The noise parameter is calculated and the procedure of achieving as low as possible NF with desirable input impedance matching, with high linearity LNA is described in this section. The analysis and design procedures of this part have been previously published in [33], [34]. Parallel amplifiers technique for achieving higher output power is a known method for power amplifier design, yet it has not been investigated as a practical topology for LNA design. Adding a parallel path demonstrates a number of virtues, including stability, higher output power, more tolerance to input signal power and better linearity, making it a reliable topology. Along with these advantages it also has drawbacks such as complexity of input power divider and output power combiner design. The loss of input divider increases the NF, and the loss of output power combiner decreases the gain of the LNA.

In this thesis, noise analysis results for parallel amplifier in general and in special case of two parallel IDCS in both coupled and uncoupled source inductors are represented. This analysis showed that the $R_n$ decreases in parallel amplifier which can lead to better NF with the same input impedance matching condition. To confirm proposed theory, two LNAs (single path and parallel amplifiers) are designed in 0.1-$\mu$ GaAs pHEMT process in both schematic and layout simulation. The parallel LNA in schematic design have the average gain of 10.5 dB along 8 to 11 GHz. The impedance matching in input and output are better than -10 dB and -14 dB respectively. The single stage IDCS LNA shows an average gain of 10 dB from 8 to 13 GHz and also the impedance matching in both input and output are better than -12 dB. In layout design, the parallel LNA exhibits the gain of 11 dB at 8 GHz with 3-dB gain bandwidth of 8-11.5 GHz, with input and output impedance matching better than -14 dB. In layout design also single stage IDCS LNA shows a gain of 9 dB at 8 GHz with 3-dB gain bandwidth of 8-13 GHz, with input and

output impedance matching better than -10 and -7 dB respectively. Output saturation power in both schematic and layout design improves 3dB because of parallel path, therefore this topology is considered as linear LNA. In this method input matching circuit design is simplified because of decrement in $R_n$. Simulation results show with no considerable change in $NF_{min}$ and similar input matching condition ($S_{11} < -10dB$), that NF in parallel topology is less than single path amplifier. As a result, even though the input divider and output combiner have losses and increase the NF slightly, the effect of $R_n$ decrement makes overall NF to be lowered in parallel amplifier.
The third design method presents a new approach in designing noise canceling common gate LNAs. In this part the condition of noise canceling are calculated and a design procedure is given to obtain low-NF, high gain, with appropriate impedance matching in common gate noise-canceling LNAs. The analytical design procedure and its results are also published in [35].
In this thesis, design procedure of new noise cancellation technique by using an IDCS stage instead of CS stage, is discussed. In spite of the conventional method which uses CS stage to cancel out the noise of CG, IDCS parallel with CG stage is used. The analytical calculation for achieving noise cancellation condition is calculated and MATLAB simulation is used to show the reduction of noise in proposed method in comparison to conventional one. To validate the theoretical analysis, two different LNAs with conventional method and proposed one are designed and compared using ADS with technology file of GaAs pHEMT 0.1 $\mu m$. The EM simulation results have shown that in proposed method the NF is decreased and better input impedance matching is obtained. It also shows that the NF decreases in the proposed approach and the gain is slightly improved. The $S_{11}$ of the proposed method is better than -12 dB while in conventional method, it is no more better than -8 dB. The output matching in both topologies have a narrow band behavior and at the center frequency the $S_{22}$ of both LNAs are better than -10 dB.

# En Français

Dans cette thèse, trois approches différentes sont présentées afin d'améliorer les performances des LNA hautes fréquences à large bande. Dans la première approche, une nouvelle procédure pour la conception de LNA à plusieurs étages en tenant compte des propriétés en bruit des étages suivants est présentée. La procédure de design ainsi que les principaux résultats obtenus ont été publiés dans [32]. Dans cette approche, une nouvelle solution

analytique pour la conception du premier étage des LNA à plusieurs étages est présentée. La méthodologie typiquement suivie pour la conception de tels amplificateurs consiste à imposer l'adaptation à l'entrée du premier étage sur son $\Gamma_{opt}$ afin de garantir la NF de ce premier étage la plus faible possible (i.e. $NF_{min}$). Aux fréquences RF et micro-ondes, en raison du compromis entre la maximisation du gain et de la minimisation de la figure de bruit, pour obtenir un gain répondant aux spécifications systèmes, il est souvent nécessaire de concevoir un LNA à plusieurs étages. Dans ce cas, la procédure de conception est beaucoup plus compliquée puisque le facteur de bruit global est aussi conditionné par le ratio entre le facteur de bruit de l'étage suivant et le gain du premier étage. L'admittance ramenée à la source du premier étage doit alors être optimisée pour présenter une figure de bruit minimum. Pour cela, il est impératif de prendre en considération non seulement le gain et le facteur de bruit du premier étage mais aussi le facteur de bruit des étages suivants.

Dans cette thèse, les calculs analytiques permettant de déterminer l'impédance de source optimale du premier étage afin de garantir simultanément le compromis entre adaptation en entrée, gain et figure de bruit globale dans les LNA à plusieurs étages sont présentés. En utilisant ces équations, une solution numérique pour une conception optimale du premier étage d'un LNA à plusieurs étages peut être obtenue. La solution analytique montre que la prise en compte de tous les étages du LNA pour l'optimisation globale du gain et de la figure de bruit, conduit à une amélioration globale de ses performances.

Pour valider les résultats théoriques et vérifier la pertinence de la méthode proposée comparativement à la méthode traditionnelle, deux amplificateurs LNA ont été conçus et optimisés à l'aide du logiciel ADS. Ces LNA sont constitués de deux étages dont le second est laissé identique dans les deux cas. Afin de mettre en évidence l'intérêt de cette méthode d'optimisation, le second étage est choisi pour présenter une figure de bruit relativement élevée tandis que le premier étage est optimisé dans un premier temps suivant la méthode traditionnelle puis celle proposée. La comparaison des performances est réalisée en nous appuyant sur des simulations électromagnétique 2,5D en utilisant le logiciel Momentum de la suite ADS. Les résultats obtenus confirment l'amélioration des performances globales obtenues par la méthode proposée. Ainsi, le LNA conçu avec cette nouvelle approche présente une figure de bruit plus faible conjointement avec un gain plus élevé (comparativement à celui conçu avec la méthode conventionnelle). Il présente, de plus, une meilleure adaptation en son entrée. Le LNA présentant les meilleures performances (méthode proposée) est fabriqué afin de valider pratiquement les calculs théoriques. Les

résultats montrent l'amélioration des performances de l'approche proposée par rapport à la méthode de conception conventionnelle. Malgré une légère augmentation du facteur de bruit du premier étage, le gain de ce dernier augmente. L'effet de masquage du facteur de bruit du second étage par ce gain est alors plus important et entraîne une amélioration globale du facteur bruit de l'ensemble.

La deuxième approche concerne l'utilisation d'amplificateurs parallèles pour la conception de LNA. Dans cette section, après avoir calculé le paramètre de bruit, la procédure de conception afin d'obtenir conjointement le plus faible facteur de bruit, la meilleure adaptation d'impédance en entrée ainsi que l'amélioration de la linéarité du LNA est décrite. Ces procédures d'analyse et de conception ont fait l'objet de publications [33] et [34]. L'utilisation d'une architecture parallèle pour augmenter la puissance de sortie disponible en sortie est une méthode connue pour la conception d'amplificateurs de puissance. Cependant son potentiel n'a pas, à l'heure actuelle, été exploité dans la conception d'amplificateurs faible bruit. L'ajout d'un chemin parallèle démontre un certain nombre de vertus, comme notamment une meilleure stabilité, une puissance de sortie plus élevée, une plus grande tolérance à la puissance du signal d'entrée et une meilleure linéarité. Outre ces avantages, il présente également des inconvénients tels que la complexité de conception du diviseur d'entrée et du sommateur de sortie. Les pertes du diviseur d'entrée augmentent le facteur de bruit, et les pertes du combineur de sortie diminuent ou en tout cas affectent le gain du LNA. Dans cette thèse, les résultats d'analyse du bruit pour l'amplificateur parallèle en général et dans le cas particulier de deux IDCS (Inductively degenerated common source) parallèles dans le cas où les inductances de source sont couplées puis non couplées sont représentés. L'analyse a montré que la résistance équivalente de bruit $R_n$ diminue pour l'amplificateur parallèle, ce qui peut conduire à une meilleure figure de bruit dans les mêmes conditions d'adaptation d'impédance d'entrée. Pour confirmer les théories proposées, deux LNA (amplificateurs à voie unique et amplificateurs parallèles) sont conçus en utilisant le design kit de la technologie pHEMT 0,1-$\mu m$ GaAs dans la simulation circuit (1D) et pour la simulation électromagnétique 2,5D.

Pour la simulation circuit, la structure LNA parallèle présente un gain moyen de 10,5dB entre 8 et 11GHz. L'adaptation en entrée et en sortie est, quant à elle, meilleure que -10dB et -14dB sur 8 et 11 GHz. Comparativement, la structure à un transistor (IDCS LNA) présente un gain moyen de 10dB sur la bande de 8 à 13GHz et une adaptation d'impédance en entrée et en sortie sur cette bande meilleure que -12dB. En ce qui concerne la simulation électromagnétique, le LNA à architecture parallèle présente un gain maximum de

11dB à 8GHz pour une bande passante à 3dB en gain couvrant 8 à 11,5GHz pour une adaptation d'impédance en entrée et en sortie meilleure que -14dB. L'amplificateur IDCS LNA, quant à lui, ne présente qu'un gain de 9dB à 8GHz pour une bande passante à 3dB en gain couvrant 8 à 13GHz. L'adaptation d'impédance en entrée et en sortie, dans ce cas, n'est alors que de -10 et -7dB respectivement.
Quel que soit le simulateur, une amélioration de l'ordre de 3dB est obtenue sur la puissance de saturation en faveur de la structure parallèle améliorant ainsi la linéarité du circuit. Dans cette méthode, la conception du circuit d'adaptation d'entrée est simplifiée en raison de la diminution de $R_n$. Les résultats de la simulation montrent que, sans changement considérable sur la $NF_{min}$ et pour des conditions d'adaptation d'entrée similaires ($S_{11} < -10dB$), la figure de bruit présentée par la topologie parallèle est inférieure à celle présentée par l'amplificateur seul. En conséquence, même si le diviseur d'entrée et l'additionneur de sortie des pertes qui pénalisent légèrement la NF, l'effet de la diminution de $R_n$ permet une diminution globale de la figure de bruit de la structure globale.
La troisième méthode de conception présente une nouvelle approche dans la conception de LNA à grille commune. Dans cette partie, les conditions de suppression de bruit sont calculées et la procédure de conception a permis de concevoir un amplificateur ayant un faible NF, un gain élevé, une adaptation d'impédance à l'état de l'art pour ce type de structure. La procédure de conception analytique et ses résultats ont également été publiés dans [35].
Dans cette thèse, la procédure de conception d'une nouvelle technique d'annulation du bruit en utilisant un étage IDCS au lieu d'un étage CS (Common Source) est discutée. La condition d'annulation du bruit est calculée analytiquement et une simulation MATLAB est utilisée pour démontrer la réduction effective du bruit par la méthode proposée par rapport à la méthode conventionnelle. Afin de valider l'analyse théorique, deux LNA différents avec la méthode conventionnelle et celle proposée sont conçus et comparés en utilisant ADS avec le design Kit de la technologie GaAs pHEMT 0,1 $\mu m$. Les résultats de la simulation EM ont montré que pour la méthode proposée, la NF est diminuée et une meilleure adaptation d'impédance d'entrée est obtenue. Le gain quant à lui augmente légèrement. Le coefficient de réflexion est ainsi meilleur que -12dB dans la bande passante alors qu'il n'est que de -8dB pour la méthode conventionnelle. L'adaptation d'impédance en sortie dans les deux topologies a un comportement à bande étroite et à la fréquence centrale, coefficient de réflexion de sortie S22 des deux LNA conçus restent inférieurs à -10dB.

# INTRODUCTION

The rapid extension of wireless networks in diverse areas increased the demand of efficient receivers with high reliability and minimum sensibility. Amplifiers are one of the key blocks in receivers whose characteristics greatly affect the overall specification of a receiver. Due to the low power level of the received signal and also the loss of first passive circuits, it is necessary to amplify the received signal as soon as possible without introducing extra noise: this is the main objective of low noise amplifiers (LNA). To maintain the signal integrity, the added noise should be as low as possible. Thus, the main characteristics of any LNA are its gain and noise figure (NF). In most receiver architectures, LNA is the first block, so it contributes most of the NF of a receiver. The most important parameters of an LNA, considering its application and required specification are its: NF, gain, bandwidth, power consumption, input and output return losses, Linearity and area on the chip. It is necessary to trade off between these parameters based on the application intended for the LNA.

## Crucial Parameters on an LNA

### Noise figure

Noise factor (F) in low-noise amplifiers is a factor that indicates the signal-to-noise ratio of the amplifier at the input to the output. Using this factor, the noise performance can be examined. [1]

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{S_{in}/N_{in}}{GS_{in}/G(N_{in}+N_{added})} = 1 + \frac{N_{added}}{N_{in}} \tag{1}$$

Most of time this noise Factor (F) is expressed in dB and is then called Noise Figure (NF). Sometimes these two definition are mistaken and Noise Figure is used inspite of Noise Factor. Nevertheless, this is commonly accepted as their definition are very close ($NF = 10\log_{10} F$).
There exists a minimum NF for each amplifier that can be achievable while the source

impedance of the LNA is equal to its optimum noise impedance. Assuming LNA as a two-port network, it can be shown that any of its noise sources can be transferred back at its input and represented by two main noise sources (Fig 1). According to this model $v_n$ is then an equivalent input voltage noise source and $i_n$ is equivalent input current noise source.

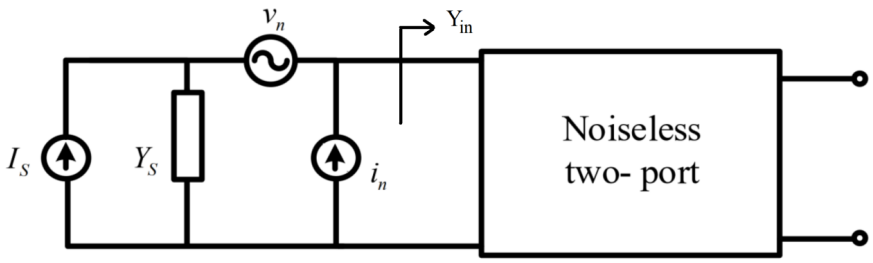



Figure 1 – Two-port noise model

Assuming that the amplifier is fed by a current source modeled through an ideal current source associated with its equivalent output impedance $Y_s = G_s + jB_s$, the input current of the noiseless amplifier can be calculated by the use of Eq (2).

$$i_i = I_s \frac{Y_{in}}{Y_{in} + Y_s} + i_n \frac{Y_{in}}{Y_{in} + Y_s} + v_n \frac{Y_{in}}{Y_{in} + Y_s} Y_s \tag{2}$$

The noise factor of the two-port can simply be calculated by use of Eq (3).

$$F = \frac{\overline{i_i^2}}{\overline{i_i^2}\big|_{i_n=0, v_n=0}} = 1 + \frac{\overline{(i_n + Y_s v_n)^2}}{{i_s}^2} \tag{3}$$

Since the two noise sources of $v_n$ and $i_n$ are not uncorrelated, it has been assumed that $i_n$ consists of two parts: $i_c$ which is correlated to $v_n$ by factor of correlation admittance of $Y_c$ ($i_c = Y_c v_n$) and $i_u$ which is the uncorrelated part. By considering $\overline{v_u^2} = 4kTR_n\Delta f$ and $\overline{i_u^2} = 4kTG_u\Delta f$, where $k$ is the Boltzmann constant and $T$ is the temperature and $R_n$ is noise equivalent resistance ($1/G_n$) and $G_u$ is equivalent uncorrelated noise conductance

and $\Delta f$ is the frequency range, Eq (3) can be written in form of Eq (4).

$$F = 1 + \frac{G_n}{G_s} + \frac{R_n}{G_s}|Y_c + Y_s|^2 = F_{min} + \frac{R_n}{G_s}|Y_s + Y_c|^2 \tag{4}$$

By derivation of F with respect to source admittance, the optimum admittance in which the minimum achievable F can be obtained.

$$B_{opt} = -B_c, G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \tag{5}$$

In this situation the minimum F would be [2]:

$$F_{min} = 1 + 2R_n\left(Y_{opt} + Y_c\right) = 1 + 2G_cR_n + 2\sqrt{R_nG_u + \left(R_nG_c\right)^2} \tag{6}$$

Therefore, the noise factor of a two port can also be represented in form of Eq (7) by use of reflection coefficients.

$$F = F_{\min} + \frac{4R_nY_0|\Gamma_{opt} - \Gamma_s|^2}{(1 - |\Gamma_s|^2)|1 + \Gamma_{opt}|^2} \tag{7}$$

By use of Eq (7), noise constant circles in smith chart can be shown in form of Eq (8).

$$\left|\Gamma_s - \frac{\Gamma_{opt}}{N+1}\right| = \frac{\sqrt{N(N+1-|\Gamma_{opt}|^2)}}{N+1} \tag{8}$$

while $N = \frac{F-F_{\min}}{4R_nY_0}|1 + \Gamma_{opt}|^2$. Concluding these equations, in an amplifier with specific noise parameters to achieve the desired noise factor, the source admittance should be optimized by use of constant noise circles in the smith-chart. However, the noise factor is not the only parameter to be achieved, some specifications could deal with gain or input impedance impedance matching. So one but not least challenge in LNA design is to find a specific point which realize the trade-off between all the specifications.

## Gain

LNA's gain is one of its most important characteristic. Achieving the highest possible gain without considerable changes in the frequency band is necessary in design optimization. Considering an amplifier as a two-port, its gain can be calculated through its reflection coefficient. Maximizing the gain of amplifier requires impedance matching in

the input and output and in case of multi-stage circuits, the impedance matching of inter-stages. The transfer gain of the amplifier can be calculated from Eq (9). In this regard, $P_{avs}$ is the maximum available power from the source. It should be noted this can be achieved in case of input impedance matching. $P_L$, is the power reached to the load.

$$G_T = \frac{P_L}{P_{avs}} = \frac{P_L}{P_{in}|_{\Gamma_s=\Gamma_{in}^*}} = \frac{\frac{|V_S|^2}{8Z_0}\frac{|S_{21}|^2(1-|\Gamma_L|^2)|1-\Gamma_s|^2}{|1-S_{22}\Gamma_L|^2|1-\Gamma_{in}\Gamma_s|^2}}{\frac{|V_S|^2}{8Z_0}\frac{|1-\Gamma_s|^2}{1-|\Gamma_s|^2}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_S\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} \quad (9)$$

In single-stage amplifiers, the noise optimum source admittance does not necessarily satisfy the input impedance matching condition. Therefore, it is not possible to achieve the maximum gain and minimum NF at the same time. Considering this, it is necessary to trade-off between the gain and NF of the amplifier. In multi-stage LNAs this trade-off is more challenging because in this case, not only the first stage need to have very low NF, but also due to the effect of first stage's gain on the overall NF, it has to have highest achievable gain.

In order to achieve the minimum NF and maximum gain, the LNA can be designed in a way that, the source impedance has to be equal to the optimal noise impedance ($Y_s = Y_{sopt}$) and on the other hand, the matching condition of input impedance is satisfied when $Y_s = Y_{in}^*$. In this case, by use of simultaneous noise and impedance matching, the optimal design can be obtained ($Y_{sopt} = Y_{in}^*$).

## Stability

By considering an amplifier as a two-port network, it is known that it is stable when the power of reflected signal is smaller than the incident signal in the input and output of the amplifier. Therefore when the amplifier is unilateral, it is unconditionally stable. In this case, with any magnitude in source and load impedance the circuit is stable. The scattering matrix of device can be also used to evaluate its stability. These conditions are :$|S_{11}| < 1$ and $|S_{22}| < 1$ which is almost the case for unilateral amplifier..

When the transistor is not unilateral, for evaluating the stability while the circuit is connected to any other magnitude of impedance in input and output by using its s-parameters the conditions of $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ should be met. It can be represented as Eq (10).

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \right| = 1 \quad (10)$$

Using Eq (10), the circle of stability in smith chart can be found. Its radius and center is represented in Eq (11).

$$r_L = \left| \frac{S_{21}S_{12}}{|S_{22}|^2 - |\Delta|^2} \right|, c_L = \left| \frac{(S_{22} - \Delta {S_{11}}^*)^*}{|S_{22}|^2 - |\Delta|^2} \right| \tag{11}$$

where $\Delta = S_{11}S_{22} - S_{21}S_{12}$, the stability condition can be easily estimated using the K stability factor and delta.

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}||S_{21}|} > 1,\ |\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{12}$$

While this test can evaluate the stability of a circuit, it can not represent the level of instability and it does not provide a way to compare the level of instability between two different circuits. Therefore, there is another test named $\mu$ test which can not only represents the stability but also specifies how stable or unstable a circuit is. This factor is represented in Eq (13).

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*\Delta| + |S_{12}S_{21}|} \tag{13}$$

In multi-stage circuits, the $\mu$ test is not sufficient for evaluation of stability of the circuit. It is also needed to analyze each stage separately to be sure that there is no oscillation in the circuit.

## Input and output impedance matching

One of the most important issues in LNA design is its impedance matching, which is done in order to transfer the signal properly by minimizing the reflected signal. Impedance matching at inputs and outputs are necessary because while connecting circuits, it is important that the output impedance of the first circuit and the input impedance of the second one, are matched so that they can transfer the maximum power between each other or from the first to the second one.

Impedance matching is typically done by passive elements of matching circuits. As the frequency response of transistors are mostly low-pass, to reach a flat gain over a specified bandwidth high-pass matching circuits with minimum losses with wide-band frequency response can help us to achieve the desired results.

The design of matching circuits is one of the most important issues in optimization of the

LNA specially for broadband amplifiers.

## Linearity

One of the specifications of any amplifier is its linearity. The linearity of the amplifier determines the range of input signal power in which the amplifier can amplify without distortion. One of the factors that determines an linearity of the amplifier is its 1 dB compression point (P-1dB). This point is actually a power indicator at which the gain of the amplifier deviates and decreases by 1 dB from the gain of the ideal linear region. In multi-stage amplifiers, the linearity of the amplifier is mostly dependent to the linearity of final stages because saturation of these stages occurs in lower power since the signal power is larger in the final stages.

Another factor for evaluating the linearity of a circuit is the third-order intercept point (IP3). It is based on the idea that the device non-linearity can be modeled using a low-order polynomial, derived by means of Taylor series expansion. IP-3 relates nonlinear products caused by the third harmonic non-linear term to the first harmonic signal. The intercept point is a purely mathematical concept and does not correspond to a practically occurring physical power level. In many cases, it lies far beyond the damage threshold of the device. IP-3 can be obtained by finding the intercept point of the output power versus the input power for first and third harmonic both on logarithmic scales. This point can be a representative for the non-linearity of the amplifier.

## Overview

The above mentioned factors are some of the most important specifications in design of an LNA. In different approaches and topologies for LNA design optimization method, it is essential to meet all required conditions with consideration of all trade-offs in the design. This thesis concerns about analytical approaches for wide-band high frequency LNA design methods and consists of three main ideas.
In the first section, a new optimization method based on analytical calculation for multi stage LNAs is presented. While numerical optimization methods for multi stage LNAs based on design of each stage as individual block have been previously developed [37]-

[41], the effect of following stage's noise has not been investigated previously. In this thesis, new design procedure in multi-stage LNAs is investigated. In spite of conventional method which emphasizes of first stage regardless to gain reduction from maximum available gain, this approach optimizes gain and NF simultaneously considering the effect of following stage's noise. Analytical calculation, for optimum multi-stage LNA design, show that the optimum noise impedance at the input of the first stage can differ. Using this new optimum input impedance can then lead to decrease the overall NF.
In the second section, parallel amplifier technique in LNA design is presented. Noise parameter have been calculated in order to achieve the best performance of this topology. The results show that the performance of the LNA can be improved and it can achieve higher gain, better input impedance matching, better linearity and robustness without any degradation in NF.
In the third section, a new noise cancellation topology in common-gate LNAs are presented. In this section, instead of common source stage for noise canceling stage, inductively degenerated common source stage is utilized which can lead to better simultaneously noise and impedance matching. The noise parameter calculations represent the required condition for noise cancellation. The obtained results show that using this approach, better NF, gain and input impedance matching can be obtained.

Chapter 1

# Literature Review

## 1.1 Introduction

The design of low noise amplifier is always associated with many challenges such as achieving to simultaneous optimum NF with desirable input impedance matching or optimal linearity with low power consumption while small area on chip is occupied in integrated circuits. In previous studies, different topologies as well as various design methods have been investigated in order to achieve appropriate gain and NF, or to have optimal input and output impedance matching, or to increase the linearity as well as reduction of the power consumption and LNA's occupied are on the chip. In these studies, the frequency band and bandwidth of the amplifier are a very important design factor. In microwave amplifiers, due to losses in transmission lines, and unavoidable reflections as well as transistor's gain roll-off, it is needed to focus more on topologies with the lowest possible NF [4]. In this chapter, two main topologies including common gate and common source LNAs will be examined. The approaches that have been proposed in these LNAs in order to improve their gain, NF, or impedance matching performance will be discussed with more details. The approaches for linearity improvement of LNAs are also investigated in this chapter.

## 1.2 Common Gate Topology

The common gate topology is considered as a broadband topology with a relatively low NF. Even though the input impedance matching condition is satisfied, the NF obtained remains much higher compared to the common source topology. This topology is mostly used because of its wideband behavior. The common gate topology is shown in Fig.1.1. In this circuit, the NF can be obtained by (1.1) [4], where $\gamma$ is a parameter for the thermal noise of the channel. ($\overline{i_{nd}^2} = 4kT\gamma g_m$ ).

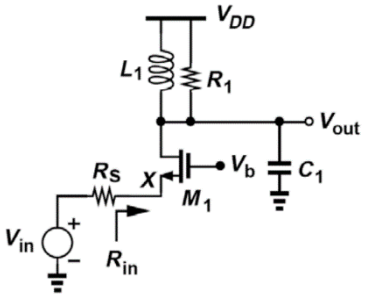



Figure 1.1 – Common gate topology [4]

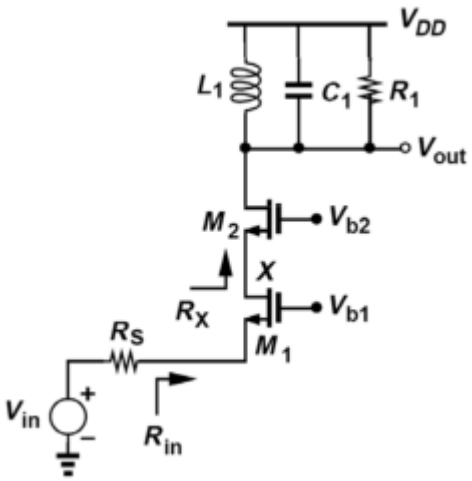



Figure 1.2 – Cascaded common gate [4]

$$NF = 1 + \frac{\gamma}{g_m R_s} + \frac{R_s}{R_1}(1 + g_m R_s)^2 \tag{1.1}$$

When the input impedance adaptation condition $g_m = 1/R_s$ is met, the NF is then $1+\gamma+\frac{4R_s}{R_1}$. Depending on the technology, this NF can be greater than 2 or 3, which is pretty much higher than the NF of the common source topology with the inductive degeneration with similar impedance matching conditions. Another problem of the common gate circuit is its dependence on the input impedance to the load resistor, which can be reduced by usage of cascaded common gate as represented in Fig.1.2. [4]. In this method, the input resistor is isolated from the load resistor. The noise from transistor M2 can increase the NF, which can become considerable at higher frequencies (the frequency at which node X is

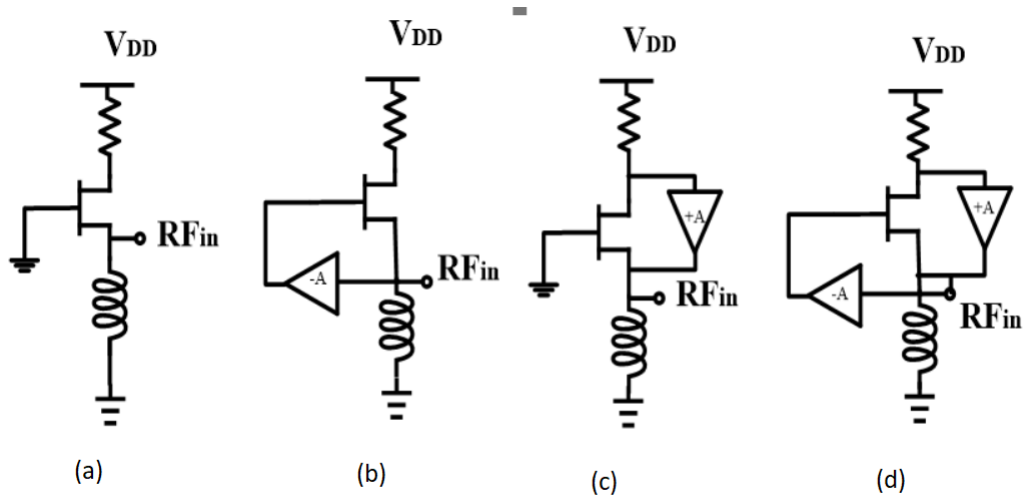



Figure 1.3 – Common gate topologies

AC-grounded). The common gate topology faces a major challenge of trading-off between its NF and the matching of the input impedance. Number of solutions to overcome this challenge have been previously proposed [5]-[9]. These methods are based on adding one or more feedback paths. Figure (1.3) shows different types of common gate topologies.
Figure (1.3-a) shows a simple common gate circuit whose main problem is high NF while its input impedance is fully matched. Using this method, by effectively increasing the $g_m$ of the transistor, the effect of channel noise at the output decreases and the input impedance matching conditions, the effect of noise is improved by a factor of $1 + A_{neg}$ (where $A_{neg}$ is the gain of the negative feedback path). One of the practical methods of this topology is the use of cross-coupled capacitors [6]. In this case, in addition to reducing the NF with an effective increase in $g_m$, the linearity is also improved by reducing the second-order distortion. The schematic of this topology is shown in Fig 1.4.

In this case, the coefficient of $A_{neg}$ will always be less than 1, so the input impedance is obtained from $Z_{in} = 1/(g_m(1 + A_{neg}))$ and the NF in the input impedance matching condition would be $1 + \frac{\gamma}{2} + \frac{4R_s}{R_1}$.
As we can see the NF is decreased using this approach compared to the previous method. Another topology is shown in Fig. (1.3-c). This approach investigated the use of a positive feedback between drain and source [7]. In this method, as shown in Fig.1.5. stability of the amplifier must be carefully considered because by use of positive feedback path, instability

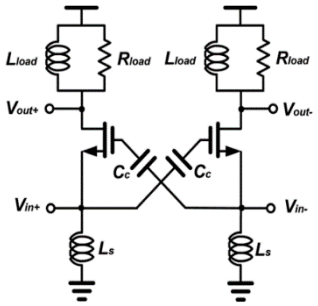



Figure 1.4 – Common gate with cross-coupled capacitors [6]

can occur.

According to this case the input impedance matching is calculated by $Z_{in} = 1/(g_m(1 - A_{pos}))$ and the NF can be obtained by Eq. (1.2)

$$NF = 1 + \frac{\gamma}{g_m R_s} + \gamma g_{m2} R_s + \frac{(1 + g_m R_s)^2}{{g_m}^2 R_s R_1} \tag{1.2}$$

In this method in case of input impedance matching ($R_s = Z_{in}^*$) the NF can be obtained by Eq (1.3) which is less than common gate topology (Eq (1.1)).

$$NF = 1 + \frac{\gamma}{2} + \gamma g_{m2} R_s + \frac{4R_s}{9R_1}. \tag{1.3}$$

Another way to improve NF in common gate topology is to use these two positive and negative feedbacks simultaneously, as shown in Figure (1.3-d). In this case, the input impedance will be $Z_{in} = 1/(g_m(1 + A_{neg})(1 - A_{pos}))$ and in the matching conditions, with $A_{neg} = 1$ and $A_{pos} = 0.5$ the NF can be calculated as:

$$NF = 1 + \frac{\gamma}{4} + \gamma g_{m2} R_s + \frac{4R_s}{9R_1} \tag{1.4}$$

It can be seen that by adding any of the feedback paths, the input matching conditions as well as the NF can be improved [5]. In another circuit shown in the Fig. 1.6, the simultaneous use of two feed-backs has improved the NF of common gate. In this method, the $G_m$ feedback path in fig.1.6 increases the transmittance while maintaining the broadband behavior of the input impedance matching [8]. In this circuit, the NF decreases with effective increase of $g_m$ while the input matching is fully matched. The simulation results represent that the effect of feedback path noise on the NF is negligible and this topology can decrease the overall NF. This method is used to design a low NF common gate dif-

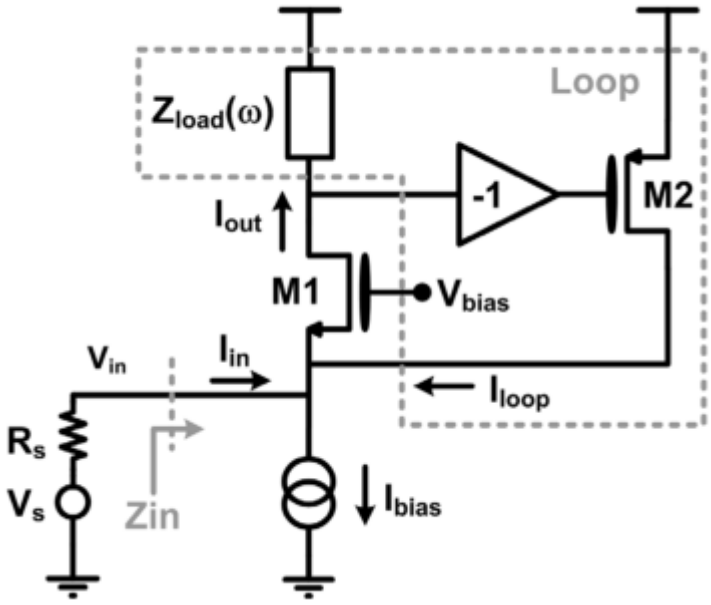



Figure 1.5 – Common gate with positive feedback between gate and drain [7]

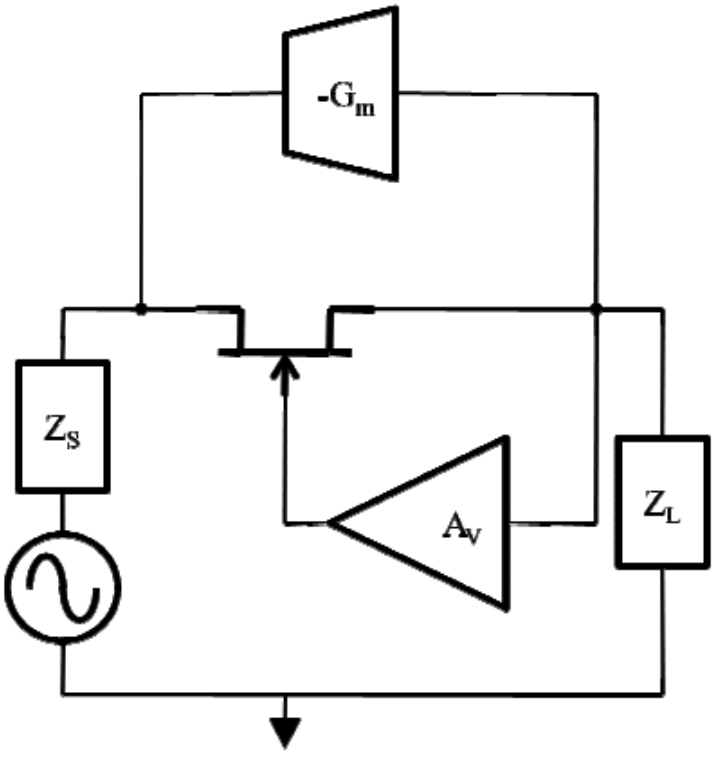



Figure 1.6 – Common gate with two feedbacks [8]

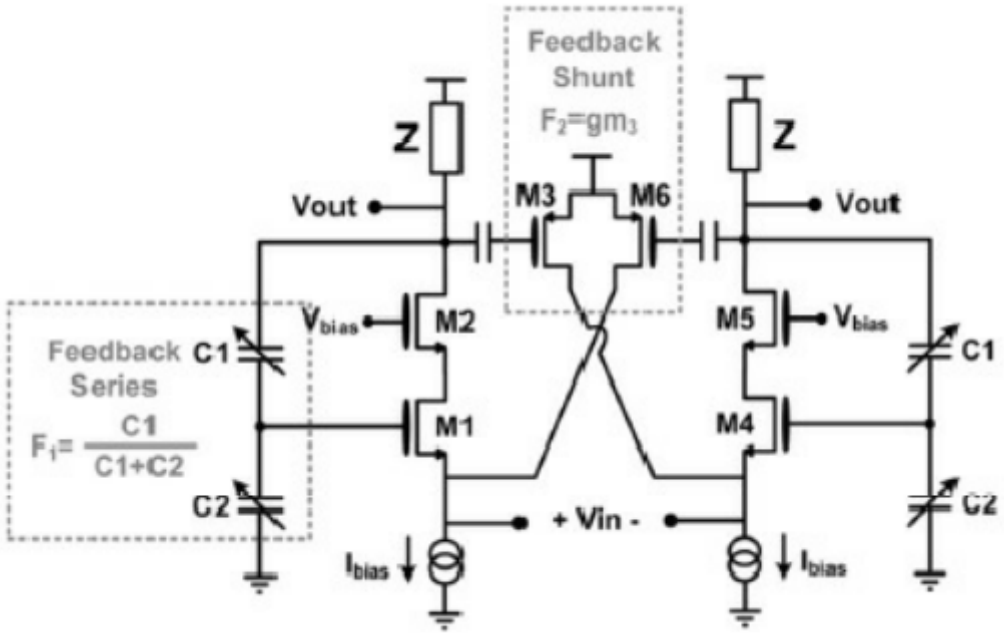



Figure 1.7 – Common gate with two differential feedbacks [8]

ferential LNA. Fig 1.7. represents the schematic design of this kind of circuit. The main issue will still be the conflict between the input impedance matching and the NF, this means that unlike inductively degenerated common source topology which can achieve simultaneous noise and impedance matching, these conditions cannot be met in common-gate topology at the same time. In two-stage LNAs with a common gate topology, the method of current-reusing can also be used to reduce power consumption. One sample of these method is shown in Fig.1.8. As it can be seen the two stages are connected using an LC matching circuit [9]. In this circuit, to eliminate interference, the matching circuits at the input and output are also used as filters to pass just the desired frequency so this method is narrow band method.

In similar works, the same topology of common gate with current reuse has been used for reducing power consumption in order to achieve gain and have input impedance matching in InP-HEMT technology in a wide frequency range from 68 to 110 GHz [10]. Noise cancellation method is another approach which is performed in common gate LNAs in order to improve the NF. In this topology a common source stage [11] as shown in Fig.1.9. is paralleled with common gate stage to cancel its channel's noise. The noise of common gate in the output would be equal to $\overline{V_{nout,M1}^2} = 4kT\gamma g_m \Delta f (\frac{R_1}{R_s} g_{m3} - g_{m4})^2 (R_s \parallel \frac{1}{g_m})^2$

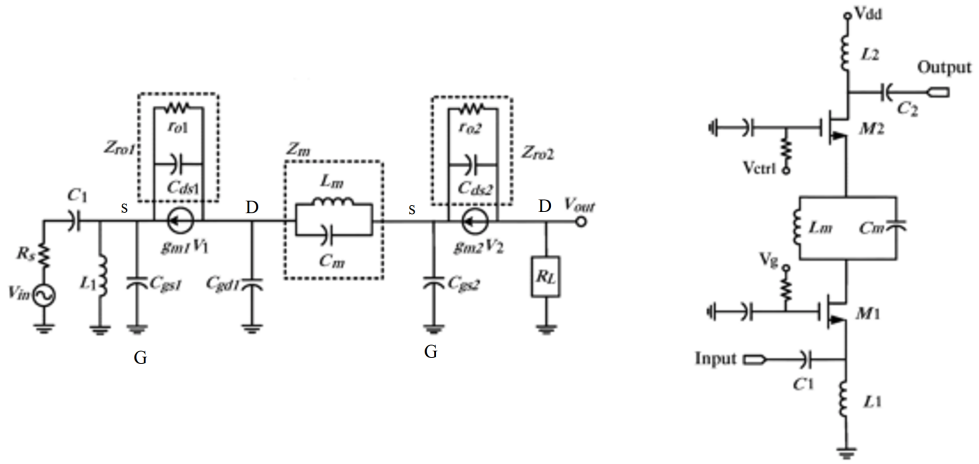



Figure 1.8 – Application of current-reuse with interference-rejection in common gate topology [9]

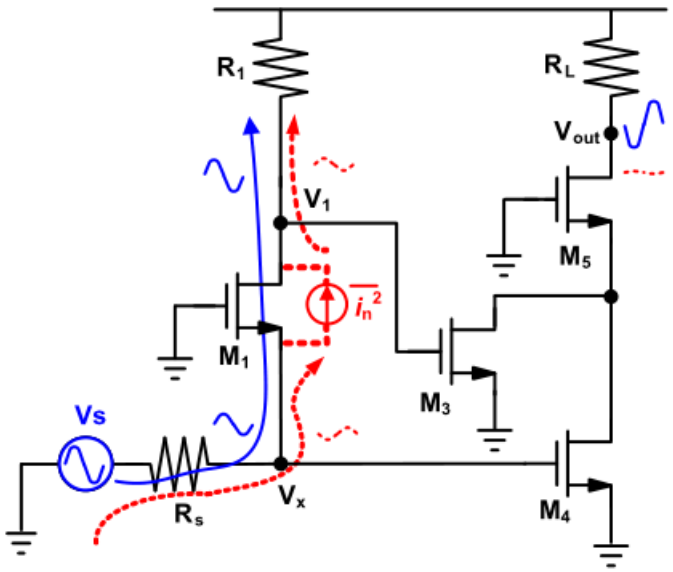



Figure 1.9 – Noise cancellation topology in common gate LNAs [11]

and by appropriate selection of circuit coefficients such as $g_{m3}$ and $g_{m4}$, it can be canceled out.

In the common gate topology, feedback paths are added to increase the degree of freedom to select the $g_m$ of transistor so that the input impedance matching condition and minimum NF can be met simultaneously. This topology has been widely used in broadband low noise amplifiers. Another topology that has been known in LNA design is the common source topology, which will be examined in the next section.

## 1.3 Common Source Topology

The common source topology is considered as a known topology in the design of low noise amplifiers. This topology is widely used in two different modes to be able to meet input impedance matching condition including: resistive feedback between gate and drain, and with inductive degeneration. In the case of resistive feedback, the noise behavior is degraded due to resistor noise. On the other hand, the amplifier exhibits a better linearity and wider frequency band. The other topology, common source with the inductive degeneration, can achieve simultaneous noise and input impedance matching. Even though this method is narrow-band, it is widely used due to its appropriate noise and input impedance performance [4]. The first topology studied in this section is the amplifier topology with feedback resistance.

### 1.3.1 Common Source Topology with Resistive Feedback

Fig.1.10 shows the small signal noise model of a common source stage with resistive feedback. The resistance $R_g$ indicates the gate noise and the noise source of $i_{nd}$ indicates the transistor channel noise. In designing a common source LNA with resistive feedback, it is important to choose the appropriate feedback resistor. In a preliminary calculation, regardless of the thermal noise of the gate ($R_g$), it can be considered that in order to have input impedance matching the $g_m$ of transistor should be equal to $1/R_s$ . In this case, the gain can be obtained from $A_v = \frac{1}{2}(1 - \frac{R_F}{R_s})$, assuming $R_F$ to be large, the gain magnitude would be $-\frac{R_F}{2R_s}$. In this case the NF can be calculated using Eq (1.5)

$$NF = 1 + \frac{4R_F}{R_S(1 - \frac{R_F}{R_S})^2} + \frac{\gamma g_m(R_F + R_S)^2}{R_S(1 - \frac{R_F}{R_S})^2} \approx 1 + \frac{4R_S}{R_F} + \gamma \tag{1.5}$$

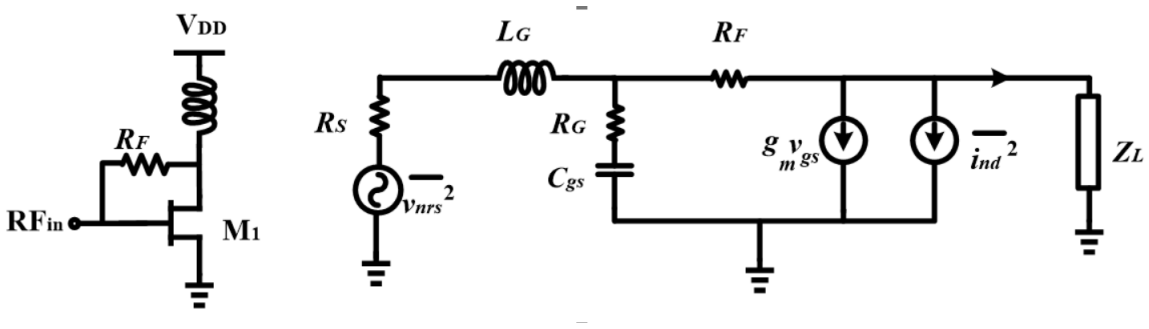



Figure 1.10 – Schematic and small signal noise model of resistive feedback topology

This topology has the NF larger than 2 or 3 dB depending on the process and the magnitude of $\gamma$. A closer look to the performance of this topology reveals that this resistor leads to decrement on sensitivity of this topology to the source impedance matching which can lead to wide-band amplifier design [12].

$$R_n = \frac{G_f + \gamma g_m + R_g {g_m}^2}{|Y_f - g_m|^2} \tag{1.6}$$

$$|Y_{opt}| = \sqrt{\frac{({g_m}^2 + {C_{gs}}^2\omega^2)(G_f + R_g {Y_f}^2) + \gamma g_m({G_f}^2 + {C_{gs}}^2\omega^2)}{G_f + \gamma g_m + R_g {g_m}^2}} \tag{1.7}$$

Using these equations in numerical analysis, by placing this $R_f$ resistor, the NF sensitivity to the input impedance matching can be reduced so the bandwidth of the circuit can be increased. In this topology, with increasing the resistance, the NF decreases and gain increases, but the effect of this resistance in the input impedance matching decreases so there is an optimal amplitude in which both desirable gain and NF can be achieved. The input impedance of this topology can be obtained using (1.8).

$$Z_{in} = \frac{Z_L/R_F + 1}{Z_L/R_F\,(C_{gs}s + g_m) + C_{gs}s + 1/R_F} \tag{1.8}$$

This topology is mostly used by some methods that can improve NF. One of these methods is noise-cancellation as represented in Fig.1.11. In this case by choosing $A_1 = (1 + \frac{R_F}{R_s})$the gain would be:

$$\frac{V_{out}}{V_x} = (1 - \frac{R_F}{R_s}) - A_1 = (1 - \frac{R_F}{R_s}) - (1 + \frac{R_F}{R_s}) \tag{1.9}$$

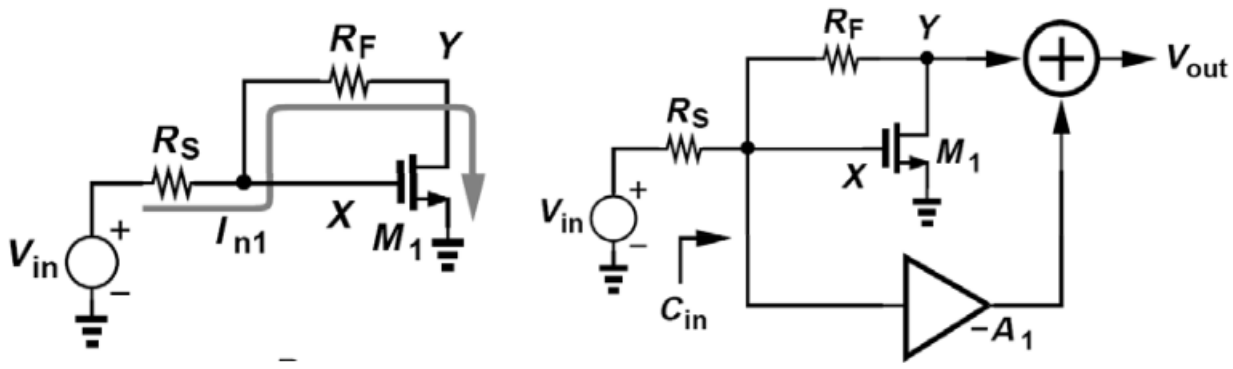



Figure 1.11 – Noise cancellation method in common source topology with resistive feedback [4]

In this case, the NF can be obtained from the Eq. (1.10) [4].

$$NF = 1 + \frac{R_s}{R_F} + \frac{\overline{V^2}_{nA1}}{4kTR_s}(1 + \frac{R_s}{R_F})^2 \tag{1.10}$$

### 1.3.2 Common Source Topology with Inductive Degeneration

The Inductively degenerated common source (IDCS) topology is one of the most widely used topologies in the design of low-noise amplifiers. This topology is used in the design of broadband circuits with very low NF [13], [14]. One of the best features of this topology is the possibility to achieve simultaneous noise and impedance matching. Fig.1.12. represents the schematic of this topology and its small-signal noise model. The resistance of $R_G$ indicates the gate's noise and the noise source of $i_{nd}$ indicates the transistor channel noise. For designing this circuit, two general approaches can be utilized. A more common and simpler method is to select the degenerate inductor to match the input impedance at the operating frequency and then calculate the circuit's NF. The obtained NF in this method will not necessarily be minimal. In the second method, which is called simultaneous noise and impedance matching (SNIM) by calculating the optimum noise impedance of the circuit ($Z_{sopt}$), it tries to achieve the condition of ${Z_{in}}^* = Z_{sopt}$ so that the minimum possible NF and high gain can be achievable. The input impedance of this circuit can be obtained by Eq. (1.11).

$$Z_{in} = R_G + (L_s + L_G)s + 1/C_{gs}s \ + \frac{g_m L_s}{C_{gs}} \tag{1.11}$$

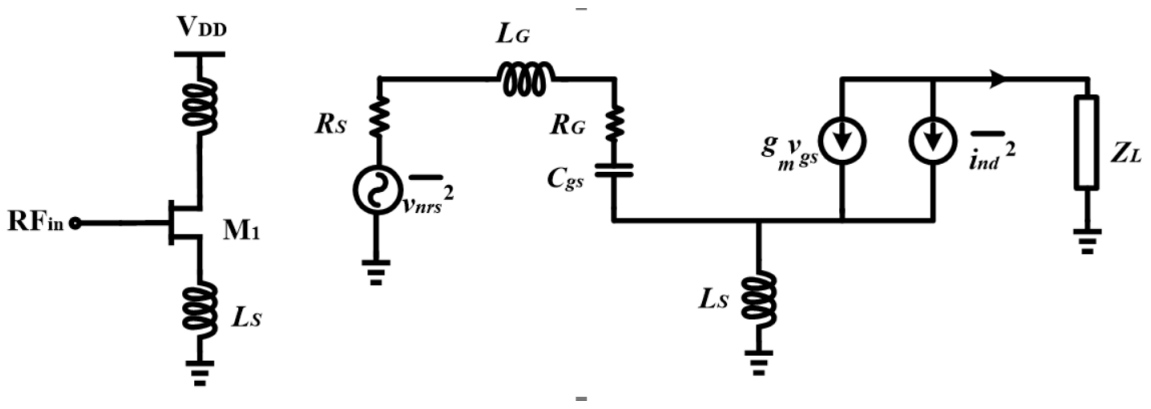



Figure 1.12 – Schematic and small signal noise model of IDCS stage

By placing $L_G$ in the input, input impedance can be achieve by setting $R_s = R_g + \frac{g_m L_s}{C_{gs}}$. In this case, the NF is obtained by neglecting the noise of $R_g$ as shown in Eq. (2.12).

$$NF = 1 + g_m R_s \gamma (\frac{\omega_0}{\omega_T})^2 \; (where\, \omega_T \approx \frac{g_m}{C_{gs}}) \tag{1.12}$$

To decrease the effect of the $C_{gd}$ cascading can be used as represented in Fig.1.13. In this approach, neglecting the noise of the cascaded transistor and considering the noise the load resistance the NF would be:

$$NF = 1 + g_m R_s \gamma (\frac{\omega_0}{\omega_T})^2 + \frac{4R_s}{R_1} (\frac{\omega_0}{\omega_T})^2 \; (where\, \omega_T \approx \frac{g_m}{C_{gs}}) \tag{1.13}$$

In similar researches, the same topology has been used by adding a switch to the re-configurable IDCS LNA in order to switch the frequency band as shown in Fig.1.14. [15].

IDCS stage is known as a topology capable of achieving simultaneous matching of noise and impedance (SNIM) [16]. To achieve minimum NF while input impedance is fully matched, further studies on this topology for SNIM condition is needed. The conditions for achieving SNIM have already been calculated with the CMOS noise model [17]. Here noise model of GaAs-pHEMT transistor has been investigated.. The reason for choosing this process is its suitable behavior for high frequency design. It is necessary to calculate the noise correlation matrix by obtaining the equivalent noise sources of the two-port so that the accurate noise parameters including minimum NF, source optimum noise impedance and $R_n$ can be obtained. The equivalent noise sources are represented in

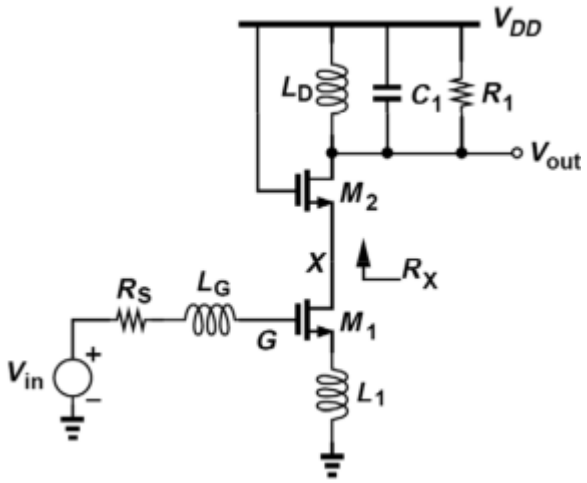



Figure 1.13 – Cascaded IDCS stage [4]

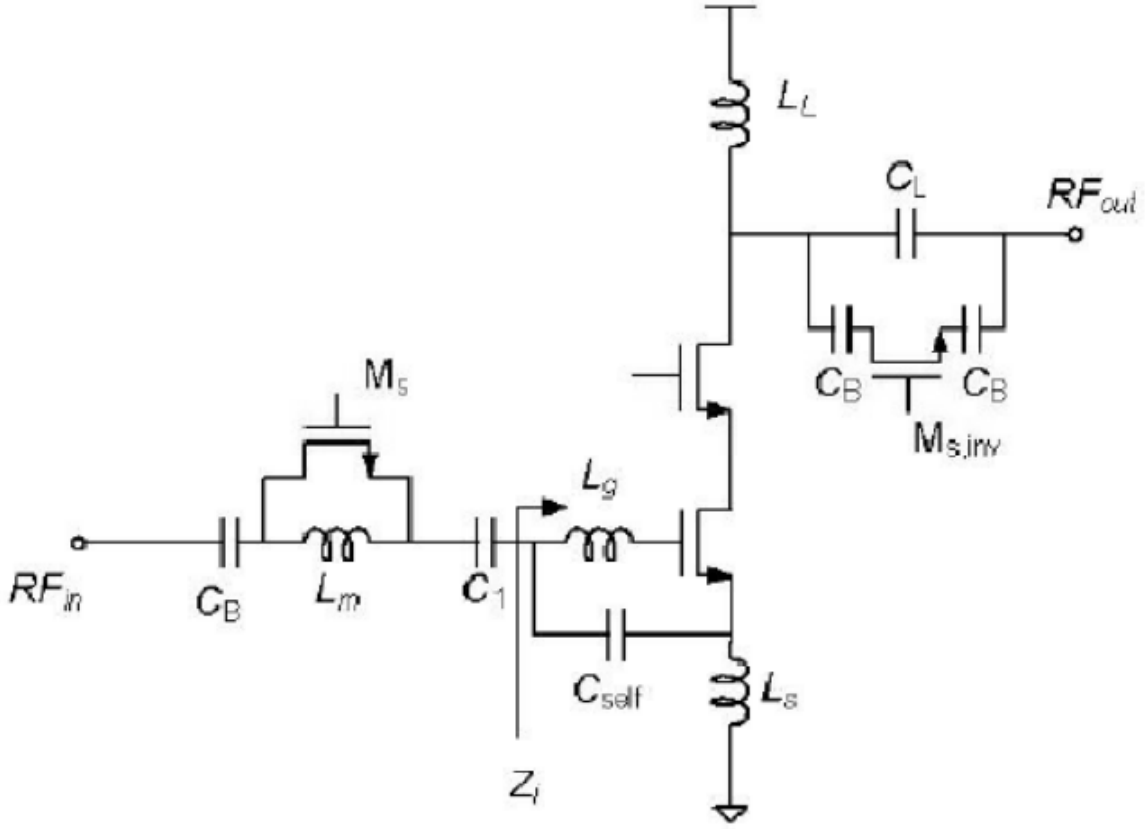



Figure 1.14 – Re-configurable multi-band LNA using a switch in gate [15]

Eq (1.14-1.15).

$$i_n = \frac{C_{gs}s}{g_m} i_{nd} \tag{1.14}$$

$$v_n = \frac{C_{gs}L_s s^2 + 1}{g_m} i_{nd} + v_{R_G} \tag{1.15}$$

Also the noise parameters can be calculated by Eq. (1.16)-(1.18).

$$R_n = R_g + \frac{\gamma}{g_m}(1 - L_s C_{gs}\omega^2)^2 \tag{1.16}$$

$$NF_{\min} = 1 + 2C_{gs}\omega\sqrt{\frac{\gamma R_g}{g_m}} \tag{1.17}$$

$$Z_{opt} = \frac{1}{C_{gs}\omega}(\sqrt{\frac{R_g g_m}{\gamma} + {R_g}^2 {C_{gs}}^2 \omega^2} + (1 - L_s C_{gs}\omega^2)j) \tag{1.18}$$

It can be seen that $R_n$ can be minimized at $\omega = \frac{1}{\sqrt{L_s C_{gs}}}$ so it can be expected to be able to design a circuit with low sensitivity to the source impedance around this frequency. To achieve SNIM, the condition ${Z_{opt}}^* = Z_{in}$ is needed.

$$Z_{in} = \frac{1 - L_s C_{gs}\omega^2}{C_{gs}\omega} j + \frac{g_m L_s}{C_{gs}} + R_g \tag{1.19}$$

Therefore:

$$L_s\omega = \sqrt{\frac{R_g}{\gamma g_m} + \frac{{R_g}^2 {C_{gs}}^2 \omega^2}{{g_m}^2}} + \frac{R_g C_{gs}}{g_m} \tag{1.20}$$

Therefore, in this topology, by properly choosing the source inductor, simultaneous noise and impedance matching can be achieved, and if our design is such that the frequency at which $R_n$ is minimized is the central frequency of our circuit, then we can achieve a wide-band design because around this frequency the sensitivity of the circuit to the optimal impedance change is minimized and thus the circuit NF will remain close to the minimum noise number.

One of the modifications that has been done in this topology to increase the bandwidth and improve the gain is the use of a coupled gate inductor to the source inductor [18]. In this circuit, as represented in Fig.1.15. and Fig.1.16. to reduce the power consumption, current-reuse method is utilized. The shared current path of these two stages would ultimately leads to a reduction in power consumption. The usage of this topology in newer

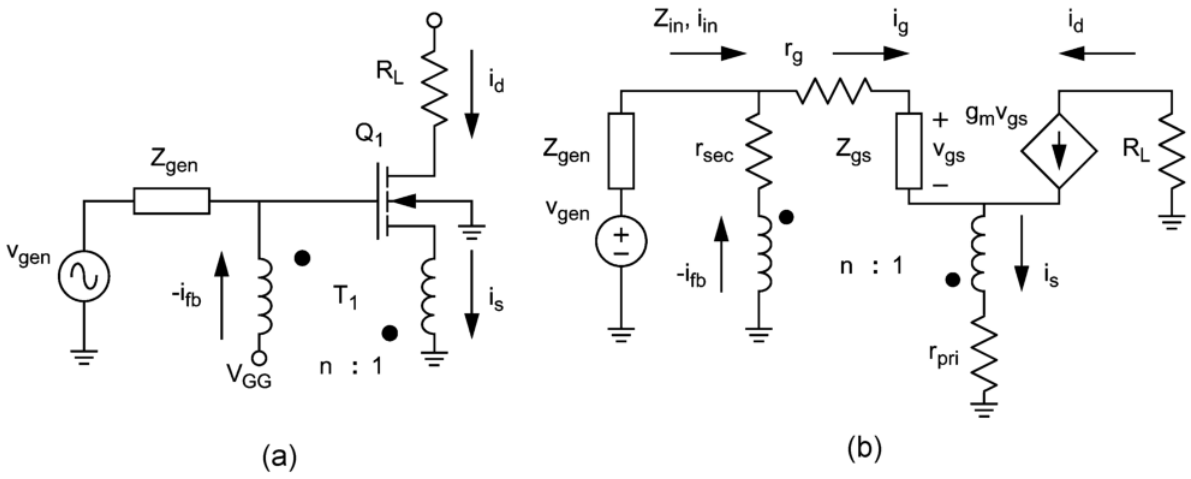



Figure 1.15 – Gate and source inductor coupling for performance improvement of IDCS stage [18]

technologies such as InP, which generally have lower NF, has also been considered, and ultimately has made it possible to achieve a very low NF in the wide-band LNA designs. In [19] as shown in Fig.1.17. a 5-stage LNA, by use of this topology in the first two stages has been designed in order to achieve the low NF. In the last three stages, common source topology with resistive feedback are used to achieve appropriate input and output impedance matching as well as smooth gain in the frequency range of 18 to 43 GHz.

In this section all used topologies in high frequency wide-band LNAs are investigated. These topologies can be used without or eventually with some improvement or with combination of different topologies in high frequency LNA circuits. Given that, the common gate topology is considered in the broadband impedance matching and relatively low NF. The topology of common source resistive feedback can be considered as linear amplifier with low sensitivity to source impedance and good input impedance matching while it has relatively high NF. Common source with inductive degeneration topology is widely used in applications with very low NF. In this topology, it is possible to achieve the lowest NF of transistor while matching the input impedance.

## 1.4 Linearization Techniques in LNAs

Linearity is one of the important parameters in LNA design which can greatly affect the performance of the receiver. The nonlinearity of the LNA is due to the intrinsic prop-

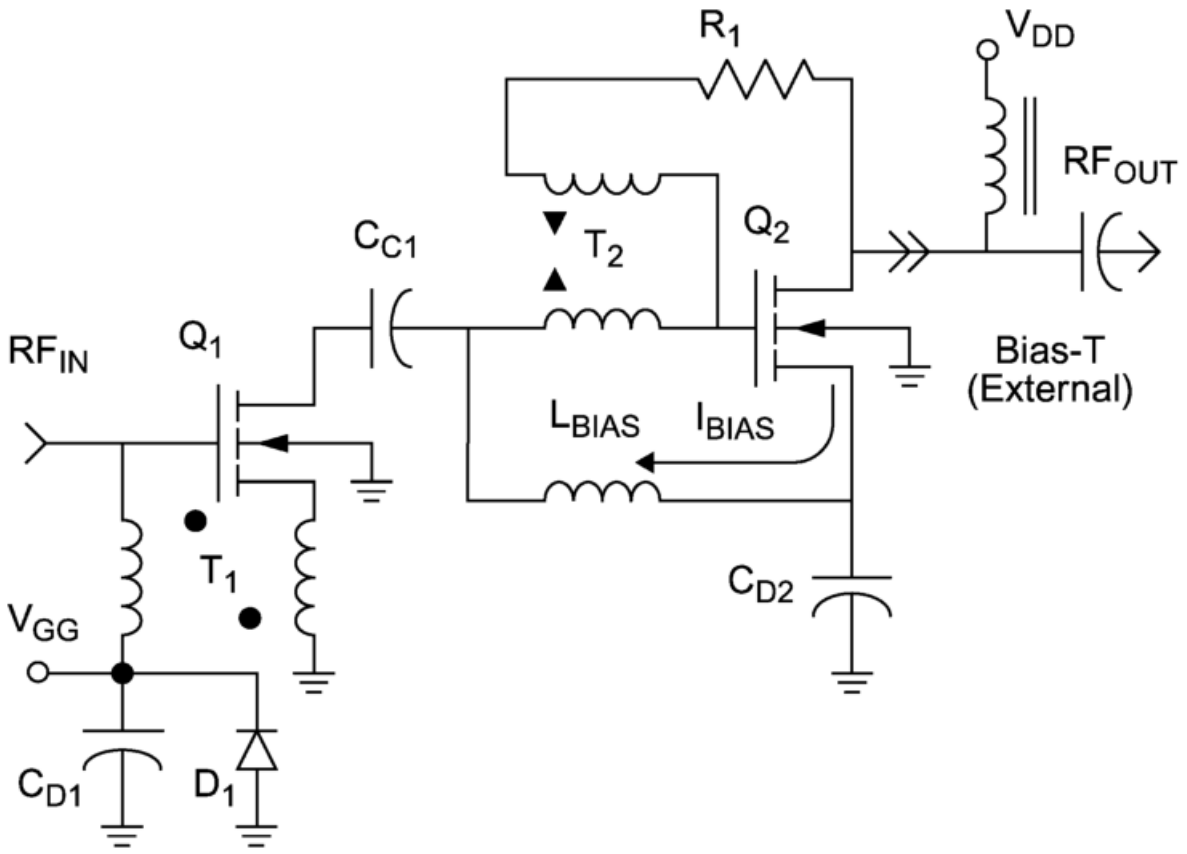



Figure 1.16 – Current reuse in gate and source inductor coupling for performance improvement of IDCS stage[18]

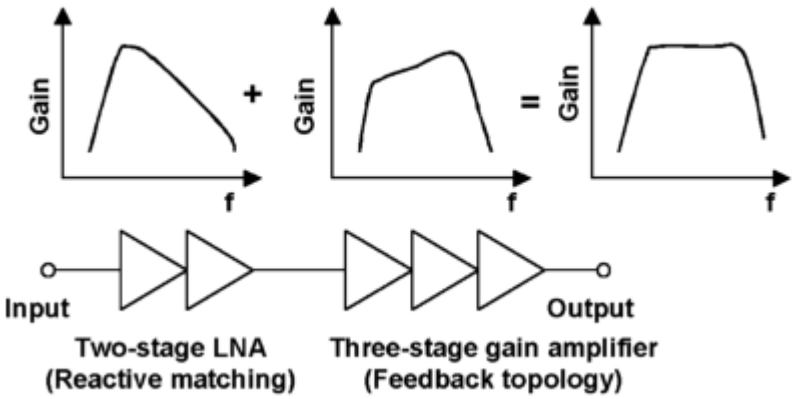



Figure 1.17 – Frequency behavior of different stages to achieve smooth gain in multistage amplifier with input IDCS stages [19]

erties of the transistor, which is mainly happens because of to two main reasons:[20]
1- Non-linearity due to the nonlinear behavior of $g_m$ that causes the input signal not to appear linearly at the output, which is called input non-linearity.
2-Non-linearity caused by a large signal in the output which is due to nonlinear behavior of $g_{ds}$ which is called output non-linearity. Linearization methods in amplifiers generally include the following approach:

- Feedback
- Harmonic termination
- Optimal Biasing
- Feed Forward
- Derivative Superposition
- Second order intermediation injection (IM2 Injection)
- Noise / distortion cancellation
- Post distortion
- EER (Envelope Elimination and Restoration)
- LINC (Linear amplification with Nonlinear Components)
- Pre distortion
- Linearization method based on specific architectures such as DOHERTY amplifier

EER and LINC methods are mostly being used in power amplifiers. The output signal of an amplifier can be modeled as polynomial such as $Y = g_1X + g_2X^2 + g_3X^3$ in which Y and X are output and input signal and $g1$ is the linear gain of the amplifier, and $g_2$, $g_3$ are weighting coefficient of the second and third order non linearity of the amplifier. Eq. (1.21) represents the nonlinear relationship between input and output of a transistor amplifier.

$$i_d = g_1(V_{gs} - V_s) + g_2(V_{gs} - V_s)^2 + g_3(V_{gs} - V_s)^3 \tag{1.21}$$

$$g_1 = \frac{\partial I_D}{\partial V_{gs}}; g_2 = \frac{1}{2}\frac{\partial^2 I_D}{\partial {V_{gs}}^2}; g_3 = \frac{1}{6}\frac{\partial^3 I_D}{\partial {V_{gs}}^3}. \tag{1.22}$$

One way to linearize the amplifier is to use the feedback path. With the presence of feedback as shown in Fig.1.18., the input-output relationship is calculated as follows [21]:

$$Y = b_1X + b_2X^2 + b_3X^3 \tag{1.23}$$

$$b_1 = \frac{g_1}{1+T}; b_2 = \frac{g_2}{(1+T)^3}; b_3 = \frac{g_3}{(1+T)^4}; (T = g_1\beta) \tag{1.24}$$

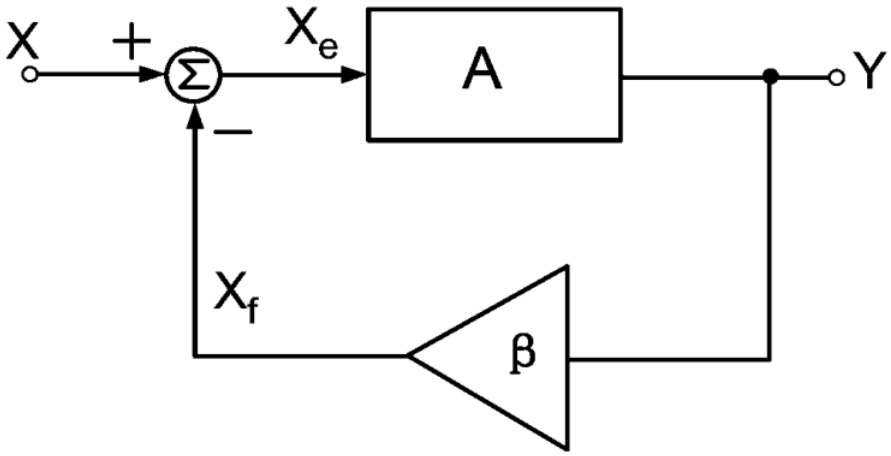



Figure 1.18 – Using feedback for linearization in LNAs [21]

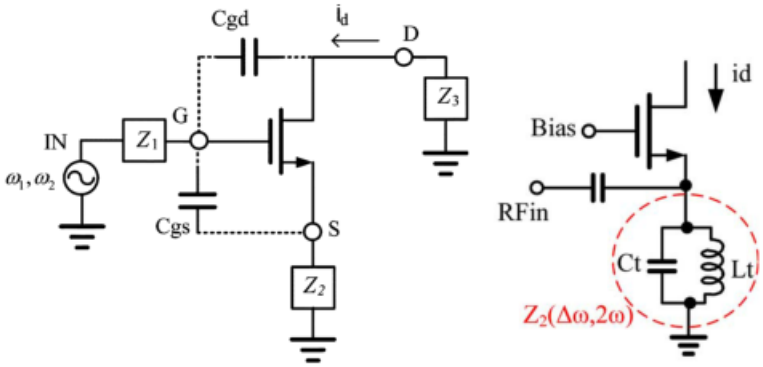



Figure 1.19 – Common source and common-gate LNA with harmonic termination [22]

where $\beta is the feedback gain in Fig. 1.18. Given that A_{Ip2} = \sqrt{\frac{g_1}{g_2}}$ and $A_{Ip3} = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|}$ [4], so $A_{Ip2}$ improves by the factor of $1 + T$ and $A_{Ip3}$ by the factor of $(1 + T)^{1.5}$. It should be noted that in this method, the loop-gain should be so small that its effect on the noise and gain should be negligible. The second method, shown in the Fig. 1.19. [22], is harmonics termination, in which a node of the circuit is grounded at a second-order intermodulation frequency, leading to no second-order intermodulation.

Another linearization method is biasing the transistor at its optimal point. In this method, the current in the transistor is plotted according to the gate-source voltage, then the second and third derivatives of this relation are also plotted. At the point where $g_3$

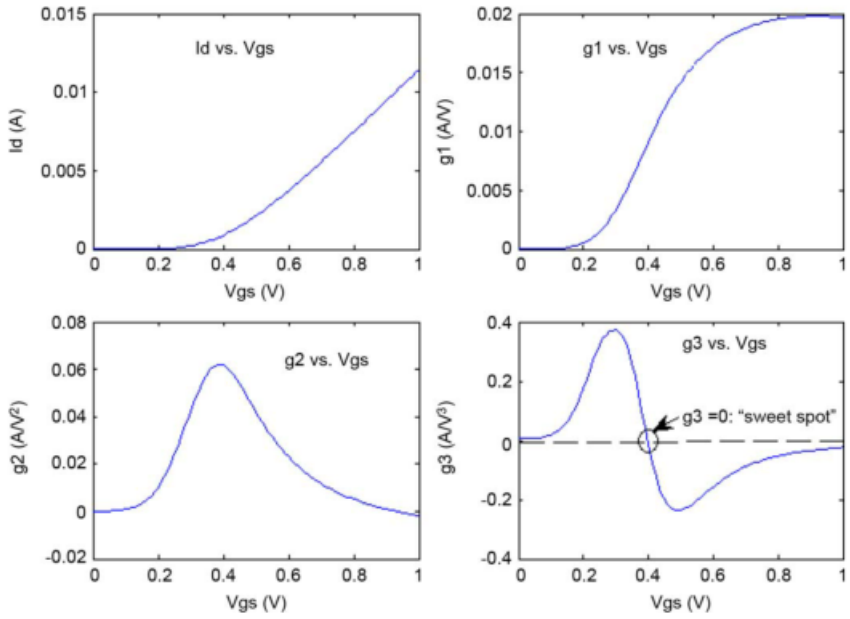



Figure 1.20 – linearization method by optimal biasing [23]

of the transistor equals zero, this bias point is selected for the transistor. This is shown in the Fig.1.20. for an NMOS transistor in the 90nm process with $\frac{w}{l} = 20/.08$ and with $v_{ds} = 1V$. This bias point is called the sweet spot [23].

In order to eliminate non-linear elements of $g_2$ and $g_3$ with the least effect on $g_2$, a higher degree of freedom is needed. Therefore, an auxiliary path from input to output consist of an auxiliary amplifier can be used. By controlling its gain and linearity, the linearity of overall amplifier can be improved. In this method as shown in Fig. 1.21. , by selecting the appropriate magnitude for the coefficient of b and n, the linearity of amplifier can be controlled. The equations associated with this method is represented in Eq. 1.25-1.27. Although in this method the gain is slightly reduced, but nonlinear parameters are further reduced which leads to more linear amplifier [24].

$$Y_{main} = g_1 X + g_2 X^2 + g_3 X^3 \tag{1.25}$$

$$Y_{aux} = (g_1(bX) + g_2(bX)^2 + g_3(bX)^3)\frac{1}{b^n} \tag{1.26}$$

$$Y_{tot} = g_1 X(1 - \frac{1}{b^{n-1}}) + g_2 X^2(1 - \frac{1}{b^{n-2}}) + g_3 X^3(1 - \frac{1}{b^{n-3}}) \tag{1.27}$$

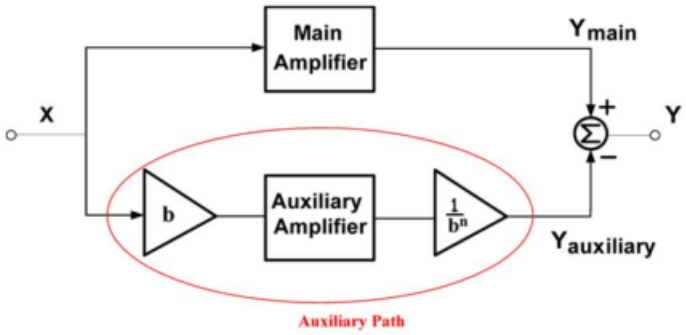



Figure 1.21 – Linearization method using an auxiliary path in amplifier [24]

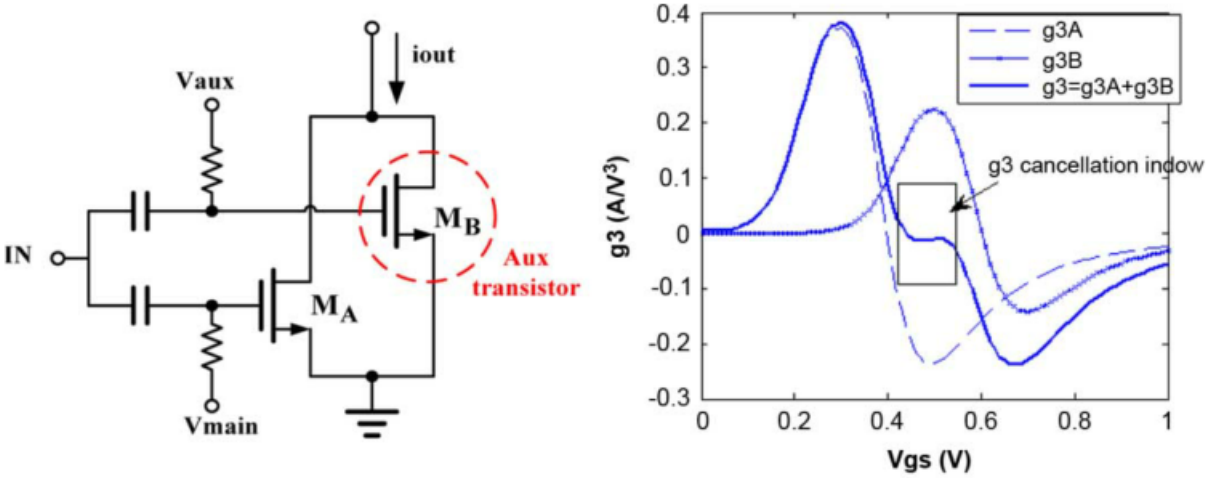



Figure 1.22 – Derivative Superposition technique to linearize amplifier [20]

Another method is the Derivative Superposition method, which is a special case of the above mentioned method. In this technique, b = 1 is selected. The main difference is that the two amplifiers does not exhibit the same behavior. For example, in CMOS technology, the two transistors are not biased at the same biasing point. Choosing appropriate biasing can lead to a more linear amplifier through the combination of these two transistors. As represented in Fig. 1.22. it can be seen that, this method is called derivative superposition because the third-order derivative of overall amplifier is the summation of two main and additional amplifiers so it can eliminate the non-linearity of main amplifier [20].
Another linearization method is the second-order intermodulation injection. As can be seen in Fig. 1.23. a new parallel path composed of a mixer will generate $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ components by multiplying the input signal with the second order intermod-

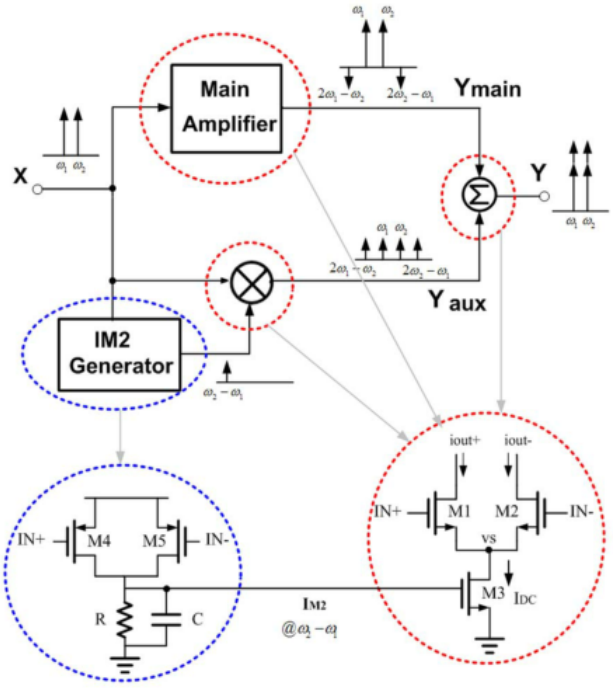



Figure 1.23 – Linearization technique using second order intermodulation injection [25]

ulation with a negative magnitude. Therefore, by choosing appropriate coefficients, the nonlinear components of the main amplifier can be eliminated [25].

Another method is noise and distortion cancellation in which common gate and the common source stages are parallelized. Since the output of common gate is in phase with the input and output of common source is in opposite phase to the input, the parameters of the two stages can be selected in such way that the noise and distortion can be canceled. The idea is represented in Fig.1.24 for a differential output on the left [26] and a single output [27] on the right.

The final method is to use the post-distortion method in which similar to Derivative Superposition method, the non-linearity behavior of the main amplifier is eliminated by the nonlinear behavior of the additional amplifier. It has two advantages in comparison to that: it has less effect on the impedance matching, and since all transistors are in the saturation region, it is a more reliable method. In this method as shown in Fig.1.25, the output of the two main and auxiliary amplifiers will be as Eq. 1.28-1.30, in which the input voltage of the auxiliary amplifier is dependent to the voltage of the first amplifier.

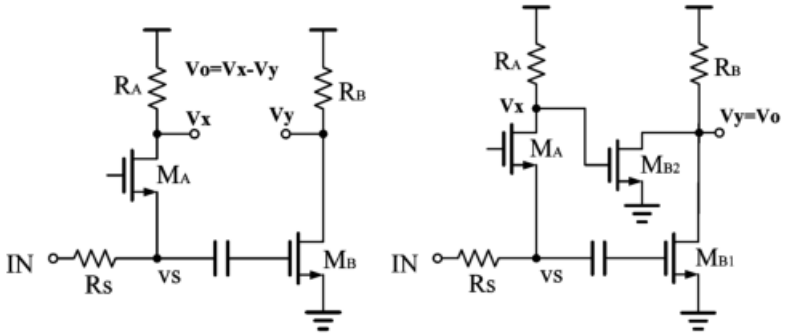



Figure 1.24 – Noise and distortion cancellation technique for LNA linearization [26]-[27]

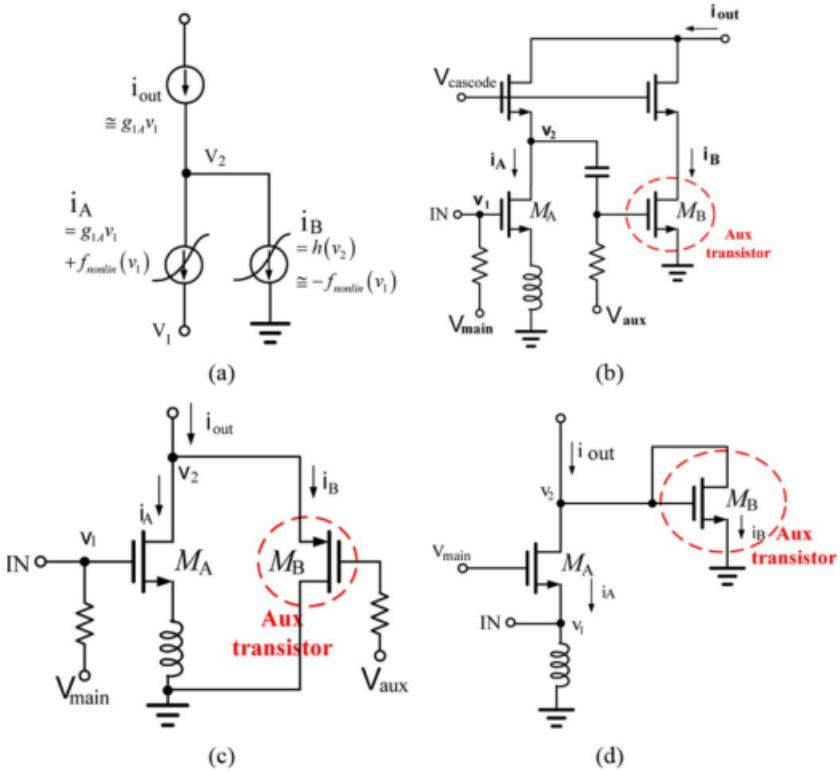



Figure 1.25 – Post-distortion linearization and implementation in a [28], b [29] and c [30]

$$i_A = g_{1A}v_1 + g_{2A}{v_1}^2 + g_{3A}{v_1}^3 \tag{1.28}$$

$$i_B = g_{1B}v_2 + g_{2B}{v_2}^2 + g_{3B}{v_2}^3 \tag{1.29}$$

$$v_2 = -b_1v_1 - b_2{v_1}^2 - b_3{v_1}^3 \tag{1.30}$$

In this way, the output relation to the input is obtained as Eq.1.31, which makes the overall amplifier be more linear by minimizig the coefficient of the second and third order distortions.

$$i_{out} = (g_{1A}-b_1g_{1B})v_1+(g_{2A}-{b_1}^2g_{2B}-b_2g_{1B}){v_1}^2+(g_{3A}-{b_1}^3g_{3B}-b_3g_{1B}-2b_1b_2g_{2B}){v_1}^3 \tag{1.31}$$

## 1.5 Study of Different Technologies for Implementation of RF circuits

The ever-increasing growth of high-frequency wireless technologies has created a broad possibility for making efficient, cost-effective circuits as well as a reasonable complexity of the manufacturing process.
This has led to a variety of technologies ranging from low-cost CMOS technology with rather poor performance to third and fourth generation technologies to be considered according to the required performance in the designing of RF circuits. There is a great variety of manufacturing technologies each of which meet part of required constrains.
CMOS technology, as one of the most available technologies is a low-cost, high-yield technology with a large wafer surface. It also enjoys benefits of the vast experience gained in this technology over decades in the construction of circuits. Despite the fact that this technology has been widely used for digital integration, due to its poor noise performance and hard integration of passive elements, it is associated with a great challenges in designing RF circuits. Therefore, it is not a good option in the construction of low-noise RF circuits [31].
In this technology, as the size of the transistors decreases, the high frequency behavior is improved and also the power consumption is reduced, but all these happen at the expense of worsening the noise behavior.
Other technologies are SiGe-BiCMOS and SiGe-HBTs that have relatively balanced the construction cost, performance and manufacturing complexity. The process of making SiGe-BiCMOS is only slightly more complex than conventional CMOS. The new SiGe-HBT process has the same working frequency as the GaAs, which is the first choice in

the construction of integrated microwave circuits. However, GaAs behave better in the integration of passive and high power elements. In general, SiGe will be a good choice whenever we want good high frequency behavior with good noise performance at a moderate to high cost. GaAs technology can be considered as the first choice in the design of microwave circuits due to its very good performance. The progress of this process and the increasing use of pHEMT has made the performance of this process even better. Thus, GaAs technology even with its higher cost is preferred among technologies available at high power and low noise application at higher frequencies.
In addition to this, in newer and more expensive manufacturing processes, it is possible to achieve lower noise and better high frequency behavior. For example, SOI technology, due to an insulating layer, causes the circuit elements to be isolated from each other, which improves noise behavior vastly[31]. To conclude according to what has been said, among all the available technologies for IC design, in this thesis, based on the required specifications which are to achieve the minimum possible NF and high output power at high frequencies, GaAs-pHEMT 0.1$\mu$m technology is chosen. The noise model for this process is detailed in the following chapters. In this section, an overall literature review to LNA design is presented. Considering the previous works, three different method for performance improvement in high frequency wide band LNAs are proposed in this thesis. The following three chapters will have a detailed discussion on these three approaches.

Chapter 2

# First Approach: Optimization Of LNA's First Stage To Reduce Overall Noise Figure in Multi-Stage LNAs

## 2.1 Introduction

In the previous chapter, we have defined all critical parameters for LNA design. We have shown the importance of the technology as well as the topology of mounted LNAs. So, in a first approach, the consideration of following stages noise for designing a multistage LNAs is looked forward. In this approach, a new procedure for design of multi stage LNAs with consideration of following stages noise is presented. This approach and its result previously published in [32].

At RF and microwave frequencies, to meet the required gain specification, usually more than one stage is needed. While analytical solution for design method of a single stage LNA is previously presented [36], optimization for a multi-stage LNAs and specially its first stage has not been investigated thoroughly yet. Designing a multi-stage LNAs are considered more complicated than single stage LNAs according to the importance of specifying the number of stages to achieve required gain as well as optimal design of each stage based on its constant-noise factor (F), available gain and input return circles in the $\Gamma_S$ plane. Therefore, all the consideration on the trade-off between these constrains to meet the required specifications should be taken into account.
Conventional methods in different topologies and approaches for LNA design with optimized NF consist of specifying the number of stages to achieve the required gain in the desired bandwidth and designing each stage based on:

- constant-noise factor (F)

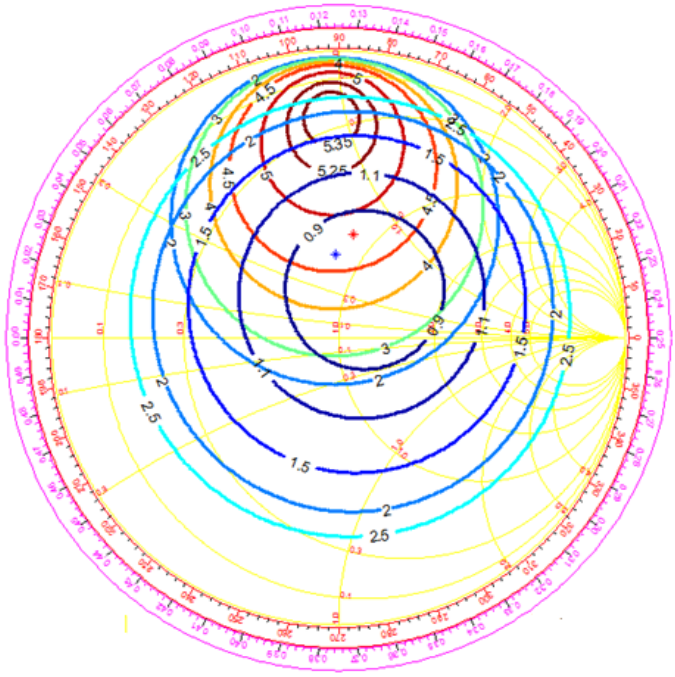



Figure 2.1 – Gain and NF contours for optimal conventional design

- constant-available gain ($G_{av}$)circles in the source reflection coefficient plane ($\Gamma_s$ plane)
- constant-input return loss ($RL_{in}$) circles in the source reflection coefficient plane ($\Gamma_s$ plane)

In order to meet the required specifications, it is crucial to have a trade-off between these constraints. For example, the trade-off between gain and NF in $\Gamma_S$ plane is shown in Fig. 2.1. In most cases the first stage is designed with lowest possible NF according the well-known Friis' formula [1] But, if the first stage presents a limited gain, the noise contribution of the second stage could become significant. Therefore optimizing the first stage of LNA in order to have optimum noise factor as well as higher gain is very essential.

Different methods for multi stage design with focus on the input and output matching are previously presented. Using noise-measure (NM) parameter for designing multi stage LNAs to obtain perfect matching in input and output sections is investigated in [24]. This methodology relies on the use of the NM, first defined by Haus and Adler [37]-[38], as a design parameter able to simultaneously account for the device noise [39], [40], [41] and gain performance. This method presents an optimization that finds appropriate $\Gamma_s$ in which NM factor ($NM = \frac{F-1}{1-(1/G)}$) is minimized. In this method noise factor and gain of

an LNA are considered simultaneously to achieve both low NF and high gain. While NM factor optimization, optimizes gain and NF for best performance simultaneously, it does not consider the effect of following stage's noise in change of optimum noise impedance. Constant mismatch circles in designing input and output matching circuits are also investigated in [41]. This method is used to obtain a suitable simultaneous match at both ports in multi stage LNAs by analyzing the role of the output termination when the source termination is fixed. The aim was to achieve a suitable noise condition while comply with other requirements.

While the above mentioned approaches in different topologies and methods, tried to provide an optimal point in the design of LNA, they did not thoroughly investigate the effect of change in optimum source impedance in multi stage LNAs due to the effect of adjacent stages. Setting the first stage at its minimum NF can lead to reduction of its associated gain. Therefore, the effect of following stage's noise can be strengthened and then degrades the overall NF [3]. Anyway, this variation on the overall NF can be negligible but remains considerably depending on the sensitivity and topology of the first stage as well as the following ones.

In this thesis, design method of the first stage in multi-stage LNAs with consideration of the effect of following stage's noise, is discussed. In spite of conventional method which emphasizes minimizing NF of first stage regardless to gain reduction from maximum available gain, this approach optimizes overall-NF considering first stage's gain and NF simultaneously as well as the effect of following stage's noise.

This section is arranged in two main parts. In the first section, analytical calculation of overall NF of an amplifier using S-parameters is presented. In this section, the contours of overall-NF of a multi-stage LNA are depicted in $\Gamma_s$ Smith-chart. In the second section, two different circuits have been designed in discrete version using ATF13136 transistor. The circuits are designed according to two different versions which are conventional method and the proposed one. Simulation results confirm the performance improvement of proposed optimization method. The proposed circuit has been fabricated and measurement approve the simulation results.

## 2.2 Noise Analysis

The noise factor of an LNA, as a two-port circuit, is dependent to its $F_{min}$ (minimum noise factor of LNA), $\Gamma_{opt}$ (optimum source admittance) and $R_n$ (the noise resistance that

shows the dependency of $F$ to difference of $\Gamma_s$ and $\Gamma_{opt}$) [21]. This noise factor expression is recalled according to the following Eq (2.1).

$$F = F_{min} + \frac{4R_n Y_0}{|1+\Gamma_{opt}|^2} \frac{|\Gamma_{opt} - \Gamma_s|^2}{1-|\Gamma_s|^2} \tag{2.1}$$

Conventional methodology for LNA design is to set source reflection coefficient equal to its $\Gamma_{opt}$ to achieve minimum possible NF. At RF and microwave frequencies, because of transistor's gain roll-off, to achieve the desired gain, multi-stage LNA is often required. In these cases, the design procedure is much more complicated due to following stage's noise factor and the effect of first stage's gain on overall-NF. To find optimized value for first stage's source admittance to achieve minimum overall-NF, gain and NF of first stage should be considered as well as following stage's noise. According to Friis's law, for a multi-stage LNA, overall noise factor can be calculated using (2.2),

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots \ . \tag{2.2}$$

According to (2.2) noise factor is strongly dependent on the first stage's noise factor as well as its gain. Overall optimization includes determination of source admittance of each stage in such a way that leads to overall-NF minimization. That means the NF and the gain of each stage should be optimized simultaneously. One of the known methods is to draw NF and gain circles in $\Gamma_s$-plane and use the graphical method to find where two appropriate circle of NF and gain meet in the $\Gamma_s$ plane. NF circles can be represented with center of $C_N$ and radius of $R_N$ according to Eq (2.3).

$$\begin{aligned} C_N &= \frac{\Gamma_{opt}}{N+1} \\ R_N &= \frac{\sqrt{N(N+1-|\Gamma_{opt}|^2)}}{N+1} \\ N &= \frac{F - F_{min}}{4R_n Y_0} |1+\Gamma_{opt}|^2 \end{aligned} \tag{2.3}$$

The transducer gain can be calculated by (2.4) using its S-parameters [2].

$$G_T = \frac{|S_{21}|^2 \left(1-|\Gamma_s|^2\right)\left(1-|\Gamma_L|^2\right)}{|1-S_{22}\Gamma_L|^2 (1-\Gamma_{in}\Gamma_s)^2} \tag{2.4}$$

where $\Gamma_s$, $\Gamma_L$, $\Gamma_{in}$ are the reflection coefficient correspond to source, load and LNA's input impedance respectively. $\Gamma_{in}$ of the first stage is calculated by (2.5) considering its input impedance to be fully matched ($\Gamma_{in} = \Gamma_s^*$). The assumption is that the load is chosen in such a way that input impedance is matched. Since $\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}$:

$$\Gamma_L = \frac{{\Gamma_s}^* - S_{11}}{{\Gamma_s}^* S_{22} - \Delta} \; (where\; \Delta = S_{11}S_{22} - S_{21}S_{12}) \tag{2.5}$$

Source fully matched gain circles is calculated through (2.6). The center and radius are $C_G$ and $R_G$ respectively.

$$\begin{aligned} C_G &= \frac{S_{22}\Delta^* - {S_{11}}^*}{(|S_{22}|^2 - 1)(M+1)} \\ R_G &= \frac{\sqrt{M^2 + (|S_{12}|^2|S_{21}|^2(1+\frac{1}{M}) - |S_{22}\Delta^* - {S_{11}}^*|^2 + 1)M}}{(M+1)(|S_{22}|^2 - 1)} \\ M &= G|S_{12}|^2. \end{aligned} \tag{2.6}$$

Considering the fact that the optimization goal is to calculate the $\Gamma_s$ in which the overall NF is minimized, and also the condition in which the gain is calculated (with input impedance matching according to (2.5)) we can obtain simultaneously noise and impedance matching in this design procedure . The overall noise factor is evaluated according to (2.7). It should be mentioned that, it is considered the effect of following stages is seen through the consideration of an equivalent "second stage". It is assumed that the LNA is designed separately of first stage and its NF is then independent from first stage's noise behavior.

$$\begin{aligned} F &= F_{\min} + K_1\frac{|\Gamma_{opt} - \Gamma_s|^2}{1 - |\Gamma_s|^2} \\ &+ K_2\frac{\left(1 - |\Gamma_s|^2\right)}{\left(\left|\Gamma_s - \underbrace{\frac{S_{22}\Delta^* - {S_{11}}^*}{(|S_{22}|^2 - 1)}}_{\Gamma_x}\right|^2 - \underbrace{\frac{|S_{12}|^2|S_{21}|^2}{\left||S_{22}|^2 - 1\right|^2}}_{X}\right)} \\ &= F_{\min} + K_1\frac{|\Gamma_{opt} - \Gamma_s|^2}{1 - |\Gamma_s|^2} + K_2\frac{\left(1 - |\Gamma_s|^2\right)}{\left(|\Gamma_s - \Gamma_x|^2 - X^2\right)} \end{aligned} \tag{2.7}$$

(2.8)

where $K_1$ and $K_2$ are defined by (2.9).

$$\begin{aligned} K_1 &= \frac{4R_nY_0}{|1+\Gamma_{opt}|^2} \\ K_2 &= (F_2-1)\,|S_{12}|^2 \end{aligned} \tag{2.9}$$

To find an approximate answer for optimum overall NF, the contribution of first stage and effect of following stage's noise can be considered individually. Assuming $F = N$ while $N = F_{min} + N_i + M$ where $F_1 = F_{min} + N_i$ is the noise contribution of the first stage and $F_2 = M$ is for the second stage. They can also be represented as:

$$N_i = K_1\frac{|\Gamma_{opt}-\Gamma_s|^2}{1-|\Gamma_s|^2} \tag{2.10}$$

$$M = K_2\frac{\left(1-|\Gamma_s|^2\right)}{\left(|\Gamma_s-\Gamma_x|^2-X^2\right)} = N - F_{\min} - N_i \tag{2.11}$$

The overall NF is the summation of the effect of these two stages and by choosing appropriate $N_i$ and $M$ the overall NF can be minimized. In order to find the NF locus in $\Gamma_s$ plane, the constrains shown in Eq (2.12) should met. This equation is calculated by some math derivation from Eq (2.7-2.11).

$$\begin{aligned} \left|\Gamma_s - \underbrace{\frac{K_1}{(K_1+N_i)}\Gamma_{opt}}_{\alpha}\right|^2 &- \underbrace{\frac{{K_1}^2|\Gamma_{opt}|^2+N_iK_1+{N_i}^2}{(K_1+N_i)^2}}_{A^2} = 0 \\ \left|\Gamma_s - \underbrace{\frac{M}{(M+K_2)}\Gamma_x}_{\beta}\right|^2 &- \underbrace{\frac{{K_2}^2+MK_2(1-|\Gamma_x|^2)}{(M+K_2)^2}}_{B^2} = 0. \end{aligned} \tag{2.12}$$

Since both these condition should met simultaneously, the overall noise factor locus is where these two circles meet.

$$\left|\frac{K_1}{(K_1+N_i)}\Gamma_{opt} - \frac{M}{(M+K_2)}\Gamma_x\right| =$$

$$\frac{\sqrt{{K_1}^2|\Gamma_{opt}|^2 + N_i K_1 + {N_i}^2}}{(K_1 + N_i)} + \frac{\sqrt{{K_2}^2 + MK_2(1-|\Gamma_x|^2)}}{(M+K_2)} \tag{2.13}$$

For calculation of exact optimum $\Gamma_s$, the derivative of overall NF with respect to $\Gamma_s$ is needed.

$$\begin{aligned} F &= F_{\min} + N_i + M \\ \frac{\partial F}{\partial \Gamma_s} &= \frac{\partial N_i}{\partial \Gamma_s} + \frac{\partial M}{\partial \Gamma_s} = 0 \\ \frac{\partial N_i}{\partial \Gamma_s} &= -\frac{\partial M}{\partial \Gamma_s} \end{aligned} \tag{2.14}$$

The exact magnitude of $\Gamma_{sopt,new}$ (optimum source reflection coefficient of first stage) is calculated by the solution of (2.15). While analytical solution for the equations is time consuming, a MATLAB optimization code is generated for finding optimum noise impedance of first stage with consideration of following stage's NF. In this method the overall NF is minimized with consideration of first stage's S-parameters, $\Gamma_{opt}$, $R_n$ and also following stage's NF while the load impedance is calculated in the way that input impedance is fully matched using (2.6). In this code, the stability is also checked and the search for $\Gamma_{opt,new}$ in $\Gamma_s$-plane is only done in stable area. To have a better perspective of proposed optimization method in table 2.1, with use of MATLAB numerical calculations, magnitude of the $\Gamma_{Soptnew1}$ (optimum source reflection coefficient of first stage using proposed approach) and $\Gamma_{Loptnew1}$ (optimum load reflection coefficient of first stage using proposed approach) in some scattering and noise parameters with different NF of second stage is calculated. This table shows that the proposed design method suggests that according to first stage's Scattering and noise parameters along with second stage's NF, the optimum magnitude for $\Gamma_S$ and $\Gamma_L$ of first stage changes for best performance of noise and gain.

$$\frac{\left(1-|\Gamma_s|^2\right)^2\left[\left(2\,|\Gamma_s|\,|\Gamma_s-\Gamma_X|^2(|\Gamma_s|-|\Gamma_s-\Gamma_X|)+2\,|\Gamma_s|\,X^2-2\,|\Gamma_s-\Gamma_X|\right)\right]}{\left(|\Gamma_s-\Gamma_X|^2-X^2\right)^2\left[2\,|\Gamma_{opt}-\Gamma_s|\,(1-|\Gamma_s|\,(|\Gamma_{opt}-\Gamma_s|-|\Gamma_s|))\right]} = \frac{K_1}{K_2} \tag{2.15}$$

Using MATLAB, the NF contours at the input for a single stage LNA and overall-NF contours for a multi-stage LNA with 3-dB NF for the following stage are drawn and depicted in Fig. 2.2. These contours show that considering following stage's noise leads

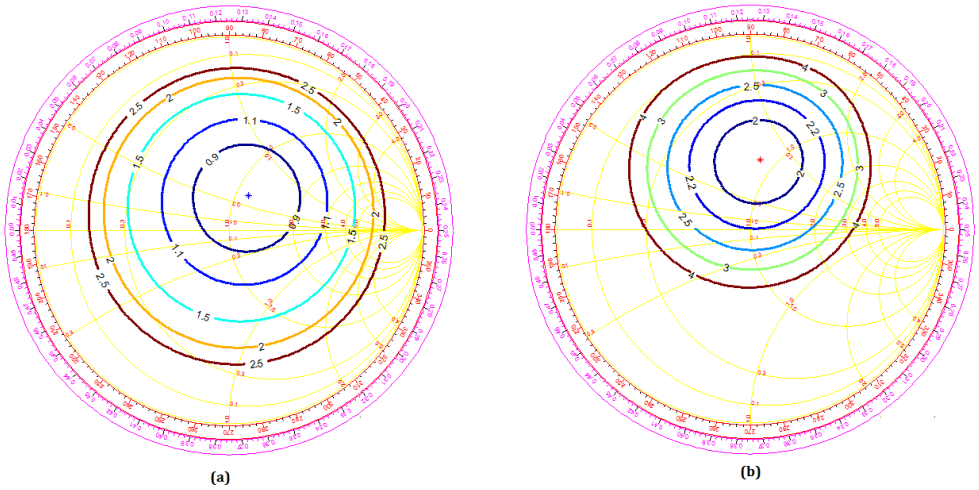



Figure 2.2 – (a) NF contours, (b) overall-NF contours

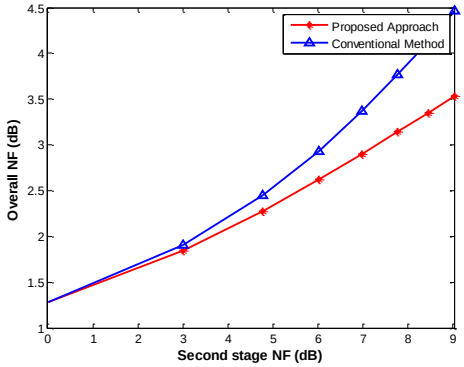



Figure 2.3 – Effect of second stage's NF in overall NF

to location of $\Gamma_{opt}$ (which minimizes overall-NF) slides and changes the design procedure for multi stage LNAs. To have a better insight for effect of second stage's NF in overall NF, simulation results in terms of Overall NF depending on NF of the second stage is presented in Fig. 2.3. It can be seen that using proposed method leads to better overall NF. In low NF cases the improvement is marginal while in high NF second stages the overall NF decrement can be considerable.

Table 2.1 – Change of $\Gamma_{opt}$ in Multistage LNAs

| $S_{11_1}$ | $S_{12_1}$ | $S_{21_1}$ | $S_{22_1}$ | $NF_{min1}$ | $\Gamma_{opt1}$ | $R_{n1}$ | $NF_2$ | $\Gamma_{Soptnew1}$ | $\Gamma_{Loptnew1}$ | $MAG(dB)$ |
|---|---|---|---|---|---|---|---|---|---|---|
| $0.54\angle 174$ | $0.031\angle 139$ | $1.65\angle 143$ | $0.45\angle -105$ | 1.22 | $0.30\angle -177$ | 2.85 | 2 | $0.40\angle -159$ | $0.30\angle 105$ | 6.59 |
| $0.54\angle 174$ | $0.031\angle 139$ | $1.65\angle 143$ | $0.45\angle -105$ | 1.22 | $0.30\angle -177$ | 2.85 | 10 | $0.61\angle -148$ | $0.45\angle 155$ | 6.59 |
| $0.67\angle 105$ | $0.035\angle 103$ | $2.85\angle 160$ | $.77\angle -47$ | 1.23 | $0.40\angle -132$ | 10.3 | 2 | $0.39\angle -130$ | $0.30\angle 3.8$ | 10.8 |
| $0.67\angle 105$ | $0.035\angle 103$ | $2.85\angle 160$ | $.77\angle -47$ | 1.23 | $0.40\angle -132$ | 25 | 2 | $0.40\angle -131$ | $0.30\angle 2.6$ | 10.8 |
| $0.67\angle 105$ | $0.035\angle 103$ | $2.85\angle 160$ | $.77\angle -47$ | 1.23 | $0.40\angle -132$ | 25 | 10 | $0.38\angle -128$ | $0.29\angle 6.3$ | 10.8 |

## 2.3 Circuit design with proposed approach in discrete mode

To validate the theoretical results and check the feasibility of proposed method and also its comparison to the traditional approach, two different LNAs with conventional and proposed approach have been designed using ADS. These LNAs are composed of two stages with the same second stage. This stage has relatively high NF to emphasize the effect of the change in $\Gamma_{opt}$ and the first stage is optimized according to the proposed and the conventional approaches respectively. The design methodology consists of five steps:
1- Finding the S-parameters of the transistor in specified biasing and frequency.
2- Calculating the $\Gamma_s$ according to (2.15).
3- Calculating the $\Gamma_L$ using (2.5).
4- Designing input and output matching according to calculated magnitude of optimum $\Gamma$ in center frequency.
5- Fine-tuning the elements for better performance considering the layout effect.
While realizing in IC mode is not available, discrete circuit is chosen to validate the theoretical approach. Transistor ATF13136 as a high performance gallium arsenide Schottky-barrier-gate field effect transistor with $f_T = 40GHz$ is chosen. Its premium NF makes it appropriate for use in LNA's first stage in 2-16 GHz frequency range.
The first circuit is designed in a the way that in the first stage $\Gamma_{source} = \Gamma_{opt}$ where $\Gamma_{opt}$ is the optimum impedance in which minimum NF of first stage is achievable. The second

circuit is designed in such a way that $\Gamma_{source} = \Gamma_{opt-overall}$ in which $\Gamma_{opt-overall}$ is the optimum impedance for overall NF of the LNA.
The difference between $\Gamma_{opt1}$ and $\Gamma_{opt-overall}$ is calculated using the MATLAB code developed for numerical solution of new optimization method which uses first stage's S-parameter, $\Gamma_{opt}$, $NF_{min}$, $R_n$ as well as second stage's NF.
S-parameters of transistor is obtained in accordance with its biasing point using the data sheet provided by the manufacturer company. The $V_{ds} = 2.5V$ and $I_{ds} = 20mA$ was chosen according to data sheet for best NF performance. The S parameters and noise parameters in this condition is represented in Eq (2.16-2.17).

$$\begin{aligned} S_{11} &= 0.84\angle -85 \\ S_{21} &= 3.28\angle 93 \\ S_{12} &= 0.077\angle 31 \\ S_{22} &= 0.53\angle -54 \end{aligned}$$

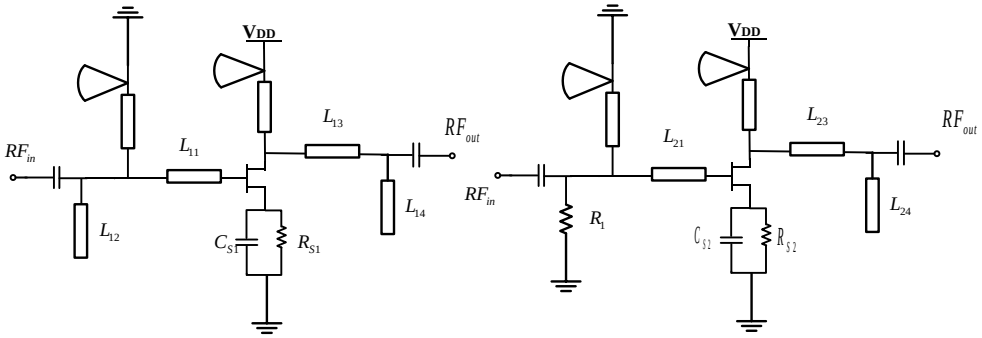
$$\Gamma_{opt} = 0.58\angle 87;\ NF_{min} = 0.5dB \tag{2.16}$$

As shown in Fig. 2.4. for both first and second stage common source stage are used. The transistor is biased using self-biasing resistor and its noise has been eliminated at the operating frequency by a parallel capacitor. For DC feed a quarter wavelength transmission line with micro-strip radial stub is used and optimized at the frequency of 4 GHz and the optimized matching circuits of each design are realized using micro-strip lines. It should be mentioned Both conventional and proposed LNAs have same schematic with different line length.
The second stage LNA is designed with rather high NF of $7dB$ for emphasizing the effect of proposed optimization method. The magnitude of line lengths for the matching circuits for both designs are gathered in table 2.2.

The performance comparison is done according to momentum simulation in ADS and LNA with better performance (proposed approach) is fabricated in order to show feasibility of theoretical calculations. Simulation results show the improvement of performance of proposed approach in comparison to conventional design method. Fig. 2.5-2.6 shows S-parameters and NF of both LNAs. The simulation results show despite slight increment in first stage's NF, the overall NF decreases due to better gain. The PCB of proposed first stage and second stage were made on the substrate with $\epsilon_r = 2.55$, $t_\delta = .0022$ and thickness of $1.35mm$.

Table 2.2 – Elements of designed LNAs

| **Proposed first stage** | **Conventional first stage** | **Second stage** |
|---|---|---|
| $L_{11} = 8.7mm$ | $L_{21} = 10mm$ | $L_{21} = 17mm$ |
| $L_{12} = 8mm$ | $L_{22} = 11.1mm$ | $R_1 = 35ohm$ |
| $L_{13} = 10.8mm$ | $L_{23} = 15.2mm$ | $L_{23} = 11.5mm$ |
| $L_{14} = 3.8mm$ | $L_{24} = 18.9mm$ | $L_{24} = 18mm$ |




First stage Schematic

Second stage Schematic

Figure 2.4 – Schematic of designed LNAs

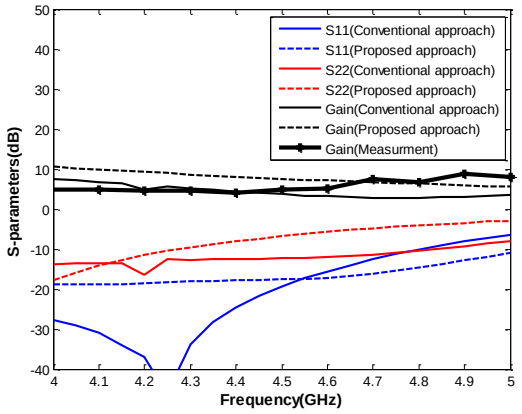



Figure 2.5 – S-parameter comparison of two LNAs

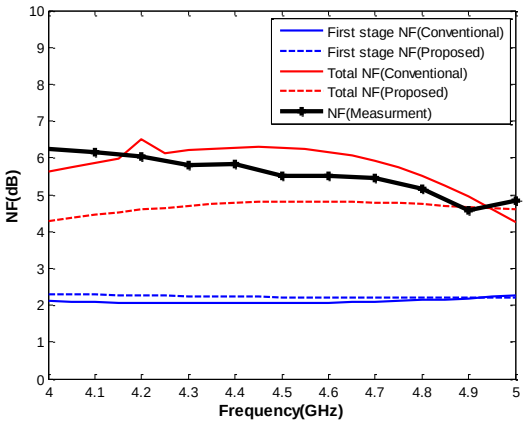



Figure 2.6 – Overall NF and first stage NF comparison of two LNAs

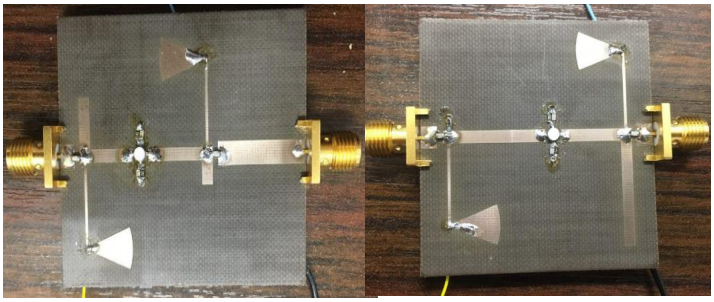


Figure 2.7 – PCB of designed LNAs: Proposed first stage and Second stage

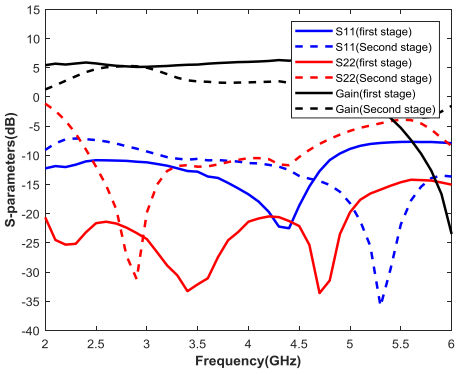



Figure 2.8 – Measurement S-parameters of each stage

Pictures of these LNAs are represented in Fig. 2.7.
Measurement results confirm the performance of designed LNA and show that the proposed approach achieves NF of 4.5 dB and Gain of 8 dB Compared to the conventional

approach which are NF of 6 dB and gain of 6 dB. The difference between simulated results and measured data happens because of process variation of transistors and also the effect of SMA connector's non ideality and losses caused by soldering effect.
The data sheet states that the pinch-off voltage can vary from -4 V to -0.5 V and the saturated drain current $I_{DSS}$ also vary from 40 to 90 mA. The process variation in transistors changes their biasing point and respectively their S-parameter and this change affects the obtained gain and also NF.
The non ideality of connector and soldering effect in input and output port leads to increment in NF and change of input and output impedance matching and also it affects the connection of first and second stage which changes the frequency response of designed LNA. The non ideality of soldering changes the frequency response of the circuit due to the added parasitic inductors and resistors in some sensitive nodes like transistor gates. These effects lead to the increase in NF and decrease in gain and also the change of frequency response. It should be mentioned that even with measurement effects the NF of LNA designed with the conventional method is higher than the LNA designed with proposed method.
The S-parameters of each stage individually are measured and depicted in Fig. 2.8.
The designed circuit with proposed approach achieves the P1-dB of 0 dBm compared to -2 dBm for conventional LNA with the same power consumption of 50mW for the first stage.
To have a better comparison between both circuits their performance are compared using $FOM = \frac{G*BW*P1B}{NF*S_{11}*S_{22}*Power-Consumption}$. The LNA with proposed approach has a FOM of 4.5 compared to conventional one with FOM of 1 shows an improvement which means a better performance.

## 2.4 Design method of Inductively degenerated common source stage with proposed method

Inductively degenerated common source stage (IDCS) due to the capability of simultaneously impedance and noise matching is commonly used in high frequency wide-band LNAs. In this topology, source inductor is calculated in way that noise optimum source impedance to be equal to conjugate of input impedance to achieve minimum NF and input impedance matching. This method is based on narrow-band numerical optimization of single stage LNA by use of source inductive degeneration and gate inductor for

input impedance matching in a specific frequency. While analytical solution for design procedure of a single stage IDCS LNA is previously presented [16], the effect of following stage's noise has not been investigated. Although the phenomenon of first stage's source input optimum noise impedance in multi-stage LNAs has previously presented in [12], the numerical calculation of IDCS stage as a known topology in high-frequency LNAs is not proposed. Here the analytical approach and numerical analysis for optimal design of IDCS stage in multi-stage LNAs are presented. In this section, design procedure of first stage in multi-stage for a IDCS stage as first stage is investigated. In the proposed approach instead of design optimization of a single stage LNA for its best performance, it is considered as a part of the block and is optimized by consideration of the noise of all stages in the multi-stage LNA in order to achieve the best performance of the overall circuit.
First the IDCS amplifier and optimization of its source impedance while considering next stage's noise has been discussed. In the second part, to validate theoretical analysis design and optimization procedure of a LNA designed on a 0.1-$\mu$m GaAs pHEMT process are presented. Simulation results confirms performance improvement of proposed optimization method.

### 2.4.1 Design analysis and calculations

In the optimization of an LNA conventionally source admittance is set equal to $Z_{opt}$ (source optimum noise impedance) to achieve minimum possible NF. At higher frequencies, the gain roll-off of transistor causes some difficulty in achieving required gain. This leads to the need for designing multi-stage LNAs. In these LNAs, the effect of following stage's noise affect the overall NF and this effect can vary depending on the gain of gain of first stage. According to Friis law, overall NF can be represented by (2.2) and as it shows it is dependent to first stage's gain. Therefore, the design procedure becomes more complicated because not only should it achieve simultaneously noise and impedance matching, but it should also considers the effect of following stage noise on the overall NF by optimization first stages gain to minimize this effect.

Noise optimization of a IDCS stage in two different methods of optimization consist of consideration and neglecting of following stage's noise are performed. Noise model of transistor is given in Fig. 2.9. Neglecting noise of $R_d$ and $R_s$ (transistors parasitic resistors in drain and source) transistor's noise sources would be the noise of $v_{ng}$ which represents

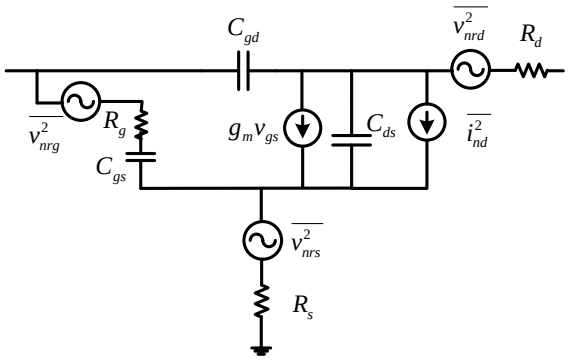



Figure 2.9 – Noise model of transistor

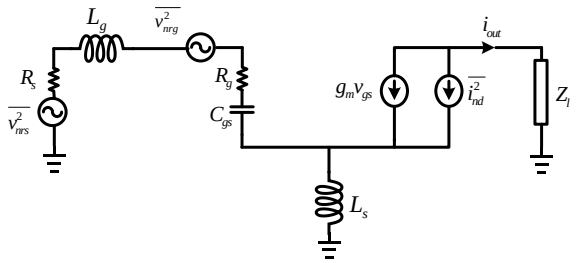



Figure 2.10 – Small signal model of IDCS LNA

the noise source of gate's resistor $R_g$ and drain channel's noise shown by means of $i_{nd}$.

$$\begin{aligned} \overline{i_{nd}^2} &= 4kTg_m\gamma f \\ \overline{v_{Rg}^2} &= 4kTR_g f \end{aligned} \tag{2.17}$$

Small signal model of IDCS LNA is shown in Fig. 2.10. The effect $C_{gd}$ and $C_{ds}$ is neglected for simplicity and their negligible effect on analyses. $L_g$ represents the input matching circuit. For wide-band LNAs much more complicated matching circuit is needed meanwhile this inductor can be used for matching circuit requirement calculation in narrow-band analysis. Noise factor of this topology is calculated. The transfer function of each noise sources is represented in (2.19)-(2.21).

$$\frac{i_{out}}{i_{nd}} = \frac{\left(C_{gs}(L_g + L_s)\right) s^2 + \left(R_g + R_s\right) C_{gs} s + 1}{\left(C_{gs}(L_g + L_s)\right) s^2 + \left(g_m L_s + R_s C_{gs}\right) s + 1} \tag{2.18}$$

$$\frac{i_{out}}{v_{nrg}} = \frac{g_m}{(C_{gs}(L_g + L_s))\, s^2 + (g_m L_s + R_s C_{gs})\, s + 1} \tag{2.19}$$

$$\frac{i_{out}}{vs} = \frac{g_m}{(C_{gs}(L_g + L_s))\, s^2 + (g_m L_s + R_s C_{gs})\, s + 1} \tag{2.20}$$

Noise factor is represented in (2.22) and the optimum source impedance is calculated by derivation relative to $R_s$ and $L_g$ and shown in (2.23).

$$NF = 1 + \frac{R_g}{R_s} + \frac{|C_{gs}\,(L_g + L_s)\, s^2 + C_{gs}(\ R_s + R_g)s + 1|^2 \gamma}{R_s\ g_m} \tag{2.21}$$

$$\begin{aligned} L_g\omega &= \frac{(1 - L_s C_{gs}\omega^2)}{C_{gs}\omega} \\ R_s &= \frac{1}{C_{gs}\omega}\sqrt{R_g^2 C_{gs}^2 \omega^2 + \frac{g_m R_g}{\gamma}} \end{aligned} \tag{2.22}$$

Consideration of following stage causes the gain of IDCS stage to affect overall noise factor. Gain and total noise factor is represented in (2.24), (2.25) respectively.

$$\frac{v_{out}}{vs} = \frac{g_m Z_l}{(C_{gs}(L_g + L_s))\, s^2 + (g_m L_s + R_s C_{gs})\, s + 1} \tag{2.23}$$

The effect of next stage's noise is represented by its equivalent noise voltage $\overline{v_n^2}$. Overall noise factor of IDCS is calculated in [1](2.26) and for simplicity $N = \frac{\overline{v_{n2}^2}}{4kTR_s}$.

$$F_{tot} = F_1 + \frac{\overline{v_{n2}^2}}{4kTR_s A_{v1}^2} \tag{2.24}$$

$$\begin{aligned} F_{tot} &= (\frac{\gamma}{g_m R_s} + \frac{N}{g_m^2 Z_l^2})(C_{gs}(L_g + L_s))^2 \omega^4 \\ &+(N\ \frac{(C_{gs}(R_g + R_s) + g_m L_s)^2}{g_m^2 Z_l^2} - 2N\ \frac{C_{gs}(L_g + L_s)}{g_m^2 Z_l^2} \\ &+\frac{\gamma}{g_m R_s}(2\,(C_{gs}(L_g + L_s)) - (C_{gs}(R_g + R_s))^2))\omega^2 \\ &+\frac{N}{g_m^2 Z_l^2} + \frac{R_g}{R_s} + \frac{\gamma}{g_m R_s} + 1 \end{aligned} \tag{2.25}$$

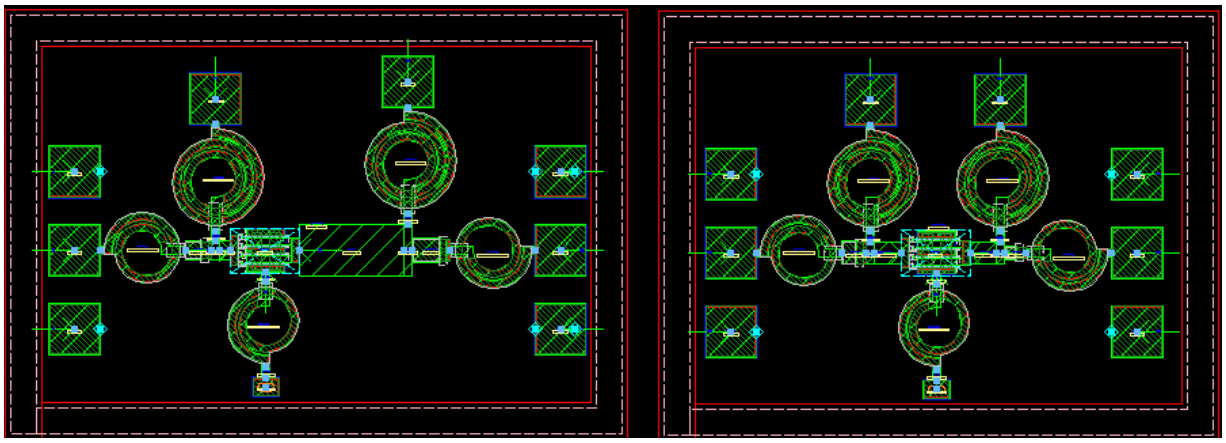


Figure 2.11 – Layout micrograph of (a) multi-stage optimized LNA (b) single-stage optimized LNA

Numerical value of $L_g$ and $R_s$ is calculable by (2.27) and (2.28).

$$L_g\omega = \frac{(1 - L_s C_{gs}\omega^2)}{C_{gs}\omega} \tag{2.26}$$

$$2NR_s^3 \ + (\gamma \ Z_l^2 + 2N\frac{R_g}{g_m} + \frac{2NL_s}{C_{gs}})R_s^2 g_m = {Z_l}^2 g_m^2 R_g(\frac{1}{C_{gs}^2\omega^2} + \frac{\gamma R_g}{g_m} \ ) \tag{2.27}$$

Considering following stage's noise changes optimum source impedance of first stage and decreases overall-NF. This design methodology suggests gain improvement of first stage with expense of slight degradation of NF which improves overall-NF in multi-stage LNAs. This approach reaches higher gain in a specified LNA in comparison to conventional method without drawbacks in NF by finding source optimum impedance. In the next section, to compare these approaches two LNAs with different optimization methodology is designed and their post-layout simulation results are compared.

### 2.4.2 Simulation Results

To validate theoretical analyses, a single stage LNA is designed in two different optimization method. First LNA optimized considering the effect of following stage's noise and second one optimized for its own minimum NF. The results are compared while these LNAs set for first stage of a receiver in which following stage's have NF of 3 dB.

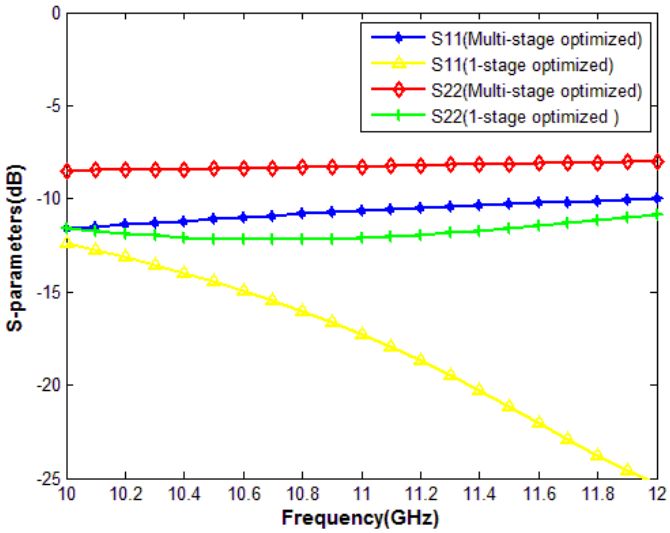



Figure 2.12 – S-parameter of LNAs

The designed amplifier is simulated in a GaAs pHEMT process with 0.1-$\mu$m gate length. The thickness of the substrate is 50 $\mu$m. The unity gain frequency $f_T$ and the maximum oscillation frequency $f_{max}$ of the process are 130 and 180 GHz, respectively [16]. The processes have two metal layers with 1 $\mu$m and 2 $\mu$m thickness, air bridges and ground back-vias. Moreover, the other passive components of this process include the metal-insulator-metal (MIM) capacitors with a capacitance density of 400 $pF/mm^2$ as well as thin film and mesa resistors with sheet resistances of 50 and 140 $^{\Omega}/.$ $g_m$ of transistors maximizes at the gate–source voltage of about -0.4 V. The minimum NF of transistors decreases by reduction of the gate–source bias voltage and almost fixes in the gate-source voltage less than -0.4 V. Based on these considerations, the transistors are biased at the gate–source voltage of -0.4 V to achieve good gain and NF. The layout micrograph of LNAs are depicted in Fig. 2.11. First LNA is optimized considering following stages noise and second LNA is single stage optimized. EM simulation is performed and S-parameters of both LNAs are represented in Fig. 2.12. Input matching of both LNAs are better than -10 dB and output matching is -8 dB for multi-stage optimized LNA and -12 for second LNA. NF of LNAs are shown in Fig. 2.13. Difference between $NF_{min}$ of LNAs are negligible while NF of multi-stage optimized LNA is 0.7 dB better than single-stage optimized LNA. First LNA is designed based on $\Gamma_s$ optimization of first stage considering the effect of following stage's noise. Therefore, the matching components are different and optimized

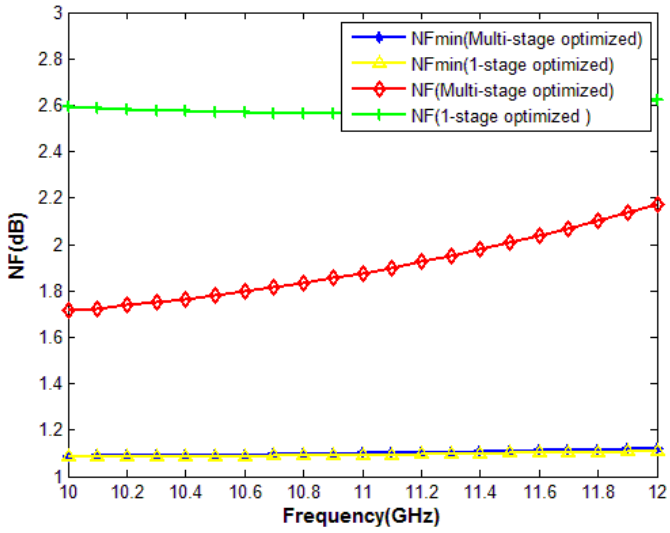



Figure 2.13 – NF of LNAs

for best performance of LNA. Gain of LNAs are shown in Fig. 2.14. Both LNAs achieve $S_{21}$ between 7 dB and 8.5 dB and the difference between them are negligible. It represents that with consideration of overall-NF circles, $\Gamma_s$ can be chosen in way that better NF is achievable without any degradation in gain. NF of first stage of LNA is represented in Fig. 2.15. This figure represents despite that first stage's NF has increased slightly, significant decrement in overall-NF is seen.

The designed circuit with proposed approach achieves the P1-dB of 6.6 dBm compared to 4.4 dBm for conventional LNA with the same power consumption of 60mW.

To have a better comparison between both circuits their performance are compared using $FOM = \frac{G*BW*P1B}{NF*S_{11}*S_{22}*Power-Consumption}$. The LNA with proposed approach has a FOM of 67.6 compared to conventional one with FOM of 62.8 shows an improvement which means a better performance.

### 2.4.3 Conclusion

In this paper, new approach for optimization of first stage of LNA with IDCS topology is presented. This method considers not only the gain and NF of first stage but also takes the effect of following stage's noise into account in order to optimize of $\Gamma_s$ of LNA. The numerical solution for IDCS LNA in order to have minimum overall NF based on its noise model as well as following stage's noise for a multi-stage LNA is represented. EM-

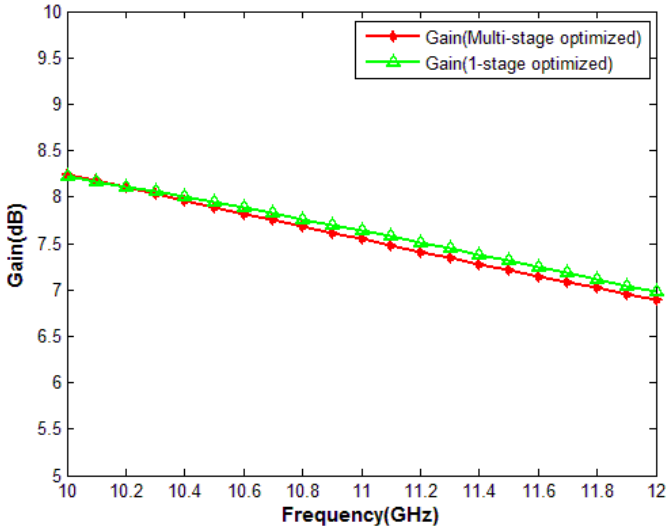



Figure 2.14 – Gain of LNAs

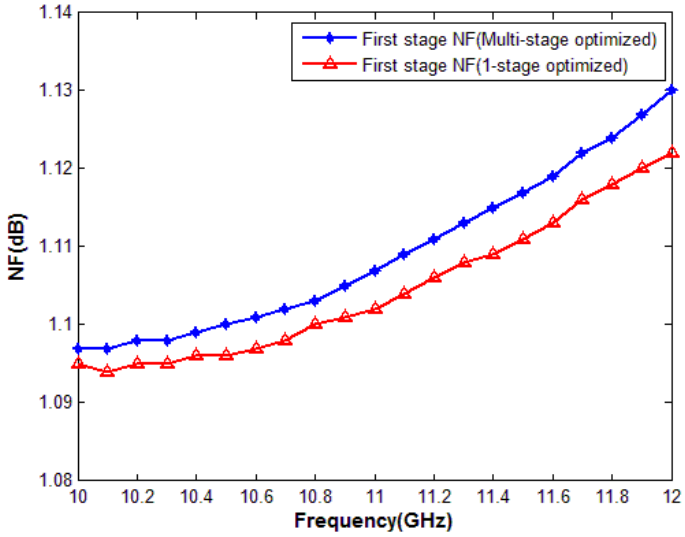



Figure 2.15 – First stage's NF of LNAs

simulation results of both LNA's layout are represented for two different conventional and proposed approaches. As represented in comparison of these methods It can be seen that slight degradation in first stage's NF, leads to improvement of the gain which can decreases the following stages noise effect hence it improves the overall NF performance.

Chapter 3

# Second Approach: Parallel Amplifier Design Technique

## 3.1 Introduction

The second approach concerns about parallel amplifier usage for LNA design. The noise parameter is calculated and the procedure of low NF with desirable input impedance matching, with high linearity LNA is described in this section. The analysis and design procedures of this part have been previously published in [33], [34].
Parallel amplifiers technique for achieving higher output power is a known method for power amplifier design [42], yet it has not been investigated as a practical topology for LNA design. Adding a parallel path, demonstrates a number of virtues, including stability, higher output power, more tolerance to input signal power and better linearity, making it a reliable topology. For instance, a single device failure will cause a parallel amplifier gain to drop rather than catastrophic failure depending on the broken state of the transistor. Different realization techniques for linearity enhancement of LNAs including the use of feedback path [21], harmonic termination [43], feed-forward path [44], post-distortion [45]- [46] have been reported previously. Demand for highly linear receivers has increased recent interest to design linear LNAs [20]. Even though recent reported techniques focus on narrow band applications and principally improve only the third-order intercept point (IIP3), parallel amplifier technique improves output 1-dB compression point. Along with these advantages it also has drawbacks such as complexity of input power divider and output power combiner design. The loss of input divider increases the NF, and the loss of output power combiner decreases the gain of the LNA. It should be ensured that each path's amplifier should achieve minimum possible NF along with maximum gain. Different typologies like common source and common gate are used before to achieve minimum noise figure and desired input impedance matching in high frequency LNAs [12]-[13],[47]-[53]. CG LNA is known as broad-band topology, but it has high NF while its input impedance

is matched [47], [48].
Inductively degenerated CS (IDCS) is a common topology in high frequency LNAs due to its capacity for satisfying simultaneously noise and input impedance matching [12]. In this topology, source inductor is used to achieve minimum NF as well as input impedance matching by equalization of noise optimum source impedance with conjugate of input impedance [13], [51]. Considering input and output losses to achieve higher gain and less NF, IDCS topology is selected for each path in parallel amplifier. This chapter is arranged in three section. In the first part, the noise parameters of each path's amplifier are calculated. The second section concerns the basic phenomena of parallel amplifiers. In the third section, simulation results to compare the proposed approach with conventional IDCS LNA is presented with the 0.1-µm pHEMT GaAs model.

## 3.2 Noise Analysis

The Noise model of a two-port can be presented in Fig. 3.1. $v_n$ and $i_n$ are the input voltage and current equivalent noise sources. The correlation matrix of noise is written by calculating its equivalent noise sources and its noise parameters consist of $NF_{min}$ (minimum noise figure), $Y_{sopt}$ (optimum noise admittance) and $R_n$ (equivalent noise resistance), can be calculated using $C_A$ matrix [3].

$$C_A = \frac{1}{2\Delta F}\begin{bmatrix} C_{vv^*} & C_{vi^*} \\ C_{iv^*} & C_{ii^*} \end{bmatrix} = 2k\begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt} \\ \frac{F_{min}-1}{2} - R_n Y_{opt}^* & R_n Y_{opt}^2 \end{bmatrix} \tag{3.1}$$

$$F = F_{min} + \frac{R_n}{G_s}(Y_s - Y_{opt})^2 \tag{3.2}$$

To acquire the noise model of the parallel network, $C_Y$ and Y-parameters of each network is used. Using (3.3-3.4) the noise correlation matrix of the parallel network is obtained.

$$C_{Ai} = \begin{bmatrix} R_{ni} & \frac{F_{\min i}-1}{2} - R_{ni} {Y_{opti}}^* \\ \frac{F_{\min i}-1}{2} - R_{ni} Y_{opti} & R_{ni}|Y_{opti}|^2 \end{bmatrix} (for\ i = 1, 2.) \tag{3.3}$$

$$C_{Yi} = \begin{bmatrix} -y_{11,i} & 1 \\ -y_{21,i} & 0 \end{bmatrix} C_{Ai} \begin{bmatrix} -{y_{11,i}}^* & -{y_{21,i}}^* \\ 1 & 0 \end{bmatrix} (for\ i = 1, 2.) \tag{3.4}$$

$$C_{Atot} = C_{Y1} + C_{Y2} = \frac{1}{|y_{21,1} + y_{21,2}|^2} \begin{bmatrix} 0 & -1 \\ 1 & -(y_{11,1} + y_{11,2}) \end{bmatrix} C_{Ytot} \begin{bmatrix} 0 & 1 \\ -1 & -(y_{11,1} + y_{11,2})^* \end{bmatrix} \tag{3.5}$$

Using Eq. 3.5, the parameters of parallel network correlation matrix can be represented by Eq. 3.6-3.8.

$$C_{11,tot} = \frac{R_{n1}|y_{21,1}|^2 + R_{n2}|y_{21,2}|^2}{|y_{21,1} + y_{21,2}|^2} \tag{3.6}$$

$$\begin{aligned} C_{12,tot} &= R_{n1}\left(\frac{|y_{21,1}|^2(y_{11,2} - y_{opt,1}) - {y_{21,1}}^* y_{21,2}(y_{11,1} + y_{opt,1})}{|y_{21,1} + y_{21,2}|^2}\right) \\ &+ R_{n2}\left(\frac{|y_{21,2}|^2(y_{11,1} - y_{opt,2}) - y_{21,1}{y_{21,2}}^*(y_{11,2} + y_{opt,2})^*}{|y_{21,1} + y_{21,2}|^2}\right) \\ &+ \frac{{y_{21,1}}^*\left(\frac{F_{\min 1}-1}{2}\right) + {y_{21,2}}^*\left(\frac{F_{\min 2}-1}{2}\right)}{|y_{21,1} + y_{21,2}|^2}(y_{21,1} + y_{21,2}) \end{aligned} \tag{3.7}$$

$$\begin{aligned} C_{22,tot} &= R_{n1}\left(\frac{|(y_{opt,1} + y_{11,1})(y_{21,1} + y_{21,2}) - y_{21,1}(y_{11,1} + y_{11,2})|^2}{|y_{21,1} + y_{21,2}|^2}\right) \\ &+ R_{n2}\left(\frac{|(y_{opt,2} + y_{11,2})(y_{21,1} + y_{21,2}) - y_{21,2}(y_{11,1} + y_{11,2})|^2}{|y_{21,1} + y_{21,2}|^2}\right) \\ &+ Re\left(\frac{y_{21,1}(y_{11,1} + y_{11,2})}{(y_{21,1} + y_{21,2})} + \frac{y_{11,1}}{|y_{21,1} + y_{21,2}|^2}\right)(F_{min1} - 1) \\ &+ Re\left(\frac{y_{21,2}(y_{11,1} + y_{11,2})}{(y_{21,1} + y_{21,2})} + \frac{y_{11,2}}{|y_{21,1} + y_{21,2}|^2}\right)(F_{min2} - 1) \end{aligned} \tag{3.8}$$

These equations can be used for any parallel two-port to calculate its noise parameters. In this thesis the topology to investigate its parallel network behavior is inductively degenerated common source (IDCS) due to its ability to achieve simultaneously noise and impedance matching in high frequency LNAs. Noise model of transistor is given in Fig. 3.2. Due to the small magnitude of the parasitic resistors of drain and source ($R_d$ and $R_s$), their noise sources are neglected. Therefore, the transistor's noise sources would be the noise of $v_{nrg}$ (noise source of gate's resistor $R_g$) explained according to Eq (3.10) and drain channel's noise which is shown by means of $i_{nd}$ relies to Eq (3.9) [3].

$$\overline{i_{nd}^2} = 4kTg_m\gamma\Delta f \tag{3.9}$$

$$\overline{v_{nrg}^2} = 4kTR_g\Delta f \tag{3.10}$$

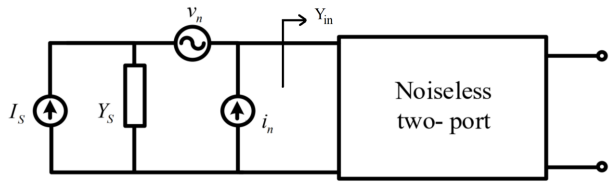



Figure 3.1 – Two-port noise model.

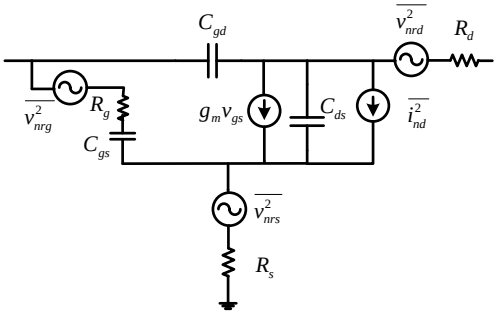



Figure 3.2 – GaAs-pHEMT transistor noise model.

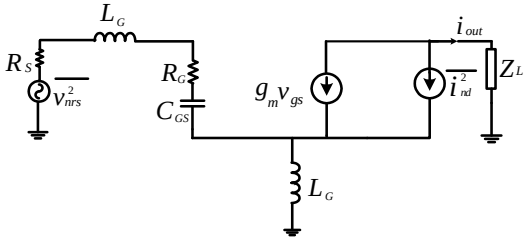



Figure 3.3 – Noise model of single path LNA

While working with Eq. (3.6-3.8) can be time consuming and complicated, the transfer function of each noise source is calculated in order to investigate the parallel network's noise behavior. Neglecting $C_{ds}$ and $C_{gd}$ for simplicity because of its negligible effect on the equations, the noise model of each path is shown in Fig. 3.3. The transfer function of output current to noise sources is shown in Eq (3.11-3.13).

$$\frac{i_{out}}{i_{nd}} = \frac{\left(C_{gs}(L_g + L_s)\right) s^2 + \left(R_g + R_s\right) C_{gs} s + 1}{\left(C_{gs}(L_g + L_s)\right) s^2 + \left(g_m L_s + R_s C_{gs}\right) s + 1} \tag{3.11}$$

$$\frac{i_{out}}{v_{nrg}} = \frac{g_m}{(C_{gs}(L_g + L_s))\, s^2 + (g_m L_s + R_s C_{gs})\, s + 1} \tag{3.12}$$

$$\frac{i_{out}}{v_s} = \frac{g_m}{(C_{gs}(L_g + L_s))\, s^2 + (g_m L_s + R_s C_{gs})\, s + 1} \tag{3.13}$$

where $v_s$ is the source voltage. Therefore, NF can be easily calculated in the form of (3.14).

$$NF = 1 + \frac{R_g}{R_s} + \frac{|C_{gs}\,(L_g + L_s)\, s^2 + C_{gs}(\ R_s + R_g)s + 1|^2 \gamma}{R_s\ g_m} \tag{3.14}$$

To have minimum NF, optimum source impedance of amplifier can be calculated by derivation of NF with respect to Rs and Lg. Noise parameters including $Z_{opt}$, $R_n$, $NF_{min}$ are represented in (3.15)-(3.17).

$$NF_{\min} = 1 + 2C_{gs}\omega\sqrt{\frac{\gamma R_g}{g_m}} \tag{3.15}$$

$$R_n = R_g + \frac{\gamma}{g_m}(1 - L_s C_{gs}\omega^2)^2 \tag{3.16}$$

$$Z_{opt} = \frac{1}{C_{gs}\omega}\sqrt{{R_g}^2 {C_{gs}}^2 \omega^2 + \frac{g_m R_g}{\gamma}} + (\frac{1}{C_{gs}\omega^2} - L_s)\omega j \tag{3.17}$$

To achieve $NF_{min}$, $R_s$ and $L_g\omega$ should be equal to real part and imaginary part of $Z_{opt}$ respectively. For broad band LNA design $R_n$ parameter should be minimized so that optimum noise impedance mismatch does not increase NF greatly.

## 3.3 Noise Analysis of parallel path

Noise model of parallel amplifier which has an IDCS amplifier in each path is shown in Fig. 3.4. The noise sources of each amplifier contribute in outputs noise current. Overall NF is calculated by using of the noise sources' transfer function. Assuming source inductors are not coupled ($M = 0$) and neglecting $C_{ds}$ and $C_{gd}$, transfer function of each noise source is calculated.

$$\frac{i_o}{ind_1} = 1 - \frac{L_{s1} g_{m1} k_2 s + (C_{gs2} L_{s1} g_{m1} - C_{gs1} L_{s1} g_{m2}) Z_s s}{k_1 k_2 + (C_{gs2} k_1 + C_{gs2} k_2) Z_s s}$$

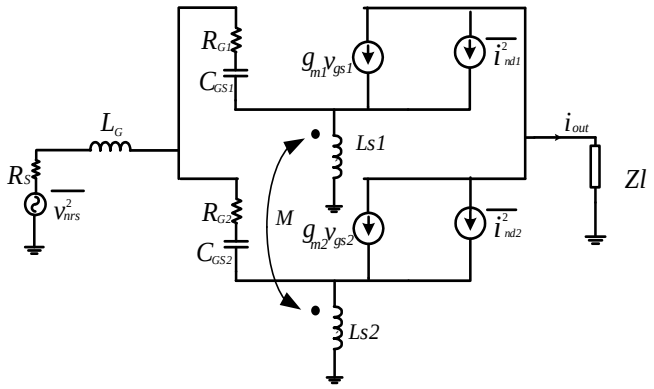



Figure 3.4 – Parallel amplifiers noise model

$$\frac{i_o}{ind_2} = 1 - \frac{L_{s2}g_{m2}k_1 s + (C_{gs2}L_{s2}g_{m1} - C_{gs1}L_{s2}g_{m2})Z_s s}{k_1k_2 + (C_{gs2}k_1 + C_{gs2}k_2)Z_s s} \tag{3.18}$$

$$\frac{i_o}{vrg_1} = -\frac{g_{m1}k_2 + (C_{gs2}g_{m1} - C_{gs1}g_{m2})Z_s}{k_1k_2 + (C_{gs2}k_1 + C_{gs2}k_2)Z_s s} \tag{3.19}$$

$$\frac{i_o}{vrg_1} = -\frac{g_{m1}k_2 + (C_{gs2}g_{m1} - C_{gs1}g_{m2})Z_s}{k_1k_2 + (C_{gs2}k_1 + C_{gs2}k_2)Z_s s} \tag{3.20}$$

$$\frac{i_o}{vrg_1} = -\frac{g_{m1}k_2 + (C_{gs2}g_{m1} - C_{gs1}g_{m2})Z_s}{k_1k_2 + (C_{gs2}k_1 + C_{gs2}k_2)Z_s s} \tag{3.21}$$

Where $k_i = (g_{mi} + C_{gsi}s)L_{si}s + R_{gi}C_{gsi}s + 1$ (for $i = 1, 2$). The overall $G_m$ of amplifier is also calculated and shown in Eq. (3.22).

$$G_m = \frac{i_o}{v_s} = -\frac{g_{m2}k_1 + g_{m1}k_2}{k_1k_2 + (C_{gs2}k_1 + C_{gs2}k_2)Z_s s} \tag{3.22}$$

For simplicity, it is assumed that the two parallel paths are similar. In this case NF can be written in the form of (3.23).

$$\begin{aligned} NF_{parallel} &= 1 + \frac{\gamma {C_{gs}}^2(R_g + 2R_s) - 2C_{gs}\gamma(2L_g + L_s)}{2g_mR_s}\omega^2 \\ &+ \frac{R_g}{2R_s} + \frac{\gamma}{2g_mR_s} + \frac{(2L_g + L_s)^2\gamma {C_{gs}}^2}{2g_mR_s}\omega^4 \end{aligned} \tag{3.23}$$

$R_n$ and $Z_{sopt}$ are also shown in (3.24)-(3.25) respectively. $R_{n-p}$ represents the equivalent

noise resistant factor for parallel amplifier while $R_{n-s}$ is for single path amplifier.

$$R_{n-p} = \frac{1}{2}R_{n-s} = R_g + \frac{\gamma}{g_m}(1 - L_s C_{gs}\omega^2)^2 \tag{3.24}$$

$$Z_{sopt} = \frac{1}{2C_{gs}\omega}\sqrt{{R_g}^2{C_{gs}}^2\omega^2 + \frac{g_m R_g}{\gamma}} + \frac{1}{2}(\frac{1}{C_{gs}\omega^2} - L_s)\omega j \tag{3.25}$$

It can be seen that by equating source impedance with optimum source impedance in NF equation, $NF_{min}$ does not change. Equation (3.24) shows that $R_n$ of two parallel amplifiers is equal to half of single path amplifier. Therefore, the sensitivity of amplifier to optimal source admittance decreases and simplifies matching circuit's design. In this topology, decrement of sensitivity parameter leads to broadband amplifiers. The effect of source inductor's coupling is also considered due to the non-ideality of layout effects which leads to source inductors of parallel paths to be coupled. For $M \neq 0$, $NF_{min}$, $Z_{sopt}$ are calculated and shown in (3.26)-(3.27).

$$\begin{aligned} NF_{min} &= 1 + \frac{2\gamma R_g {C_{gs}}^2\omega^2}{g_m} - 2\gamma C_{gs} M\omega^2 \\ &+ \frac{4\gamma {C_{gs}}^2\omega^2}{g_m}\sqrt{\frac{{R_g}^2}{4} + \frac{M^2{g_m}^2}{4{C_{gs}}^2} + \frac{g_m R_g}{4{C_{gs}}^2\omega^2} - M\frac{g_m R_g}{2C_{gs}}} \end{aligned} \tag{3.26}$$

$$\begin{aligned} Z_{sopt} &= \sqrt{\frac{{R_g}^2}{4} + \frac{M^2{g_m}^2}{4{C_{gs}}^2} + \frac{g_m R_g}{4{C_{gs}}^2\omega^2} - M\frac{g_m R_g}{2C_{gs}}} \\ &+ \frac{1}{2}(\frac{1}{C_{gs}\omega^2} - L_s + M)j\omega \end{aligned} \tag{3.27}$$

In this case, $Z_{sopt}$ and $NF_{min}$ are changed. Therefore with appropriate M, $NF_{min}$ can be reduced. Parallel amplifier technique for LNA design associated with IDCS topology is considered for both coupled and uncoupled source inductors. This technique as well as being practical for enhancement of the linearity can also be useful for low sensitivity LNAs. It can be assumed that its broadband characteristic makes this approach interesting for the design of wideband LNAs. In practice we should consider that the circuit design of low loss power divider and combiner in input and output of the LNA respectively, are

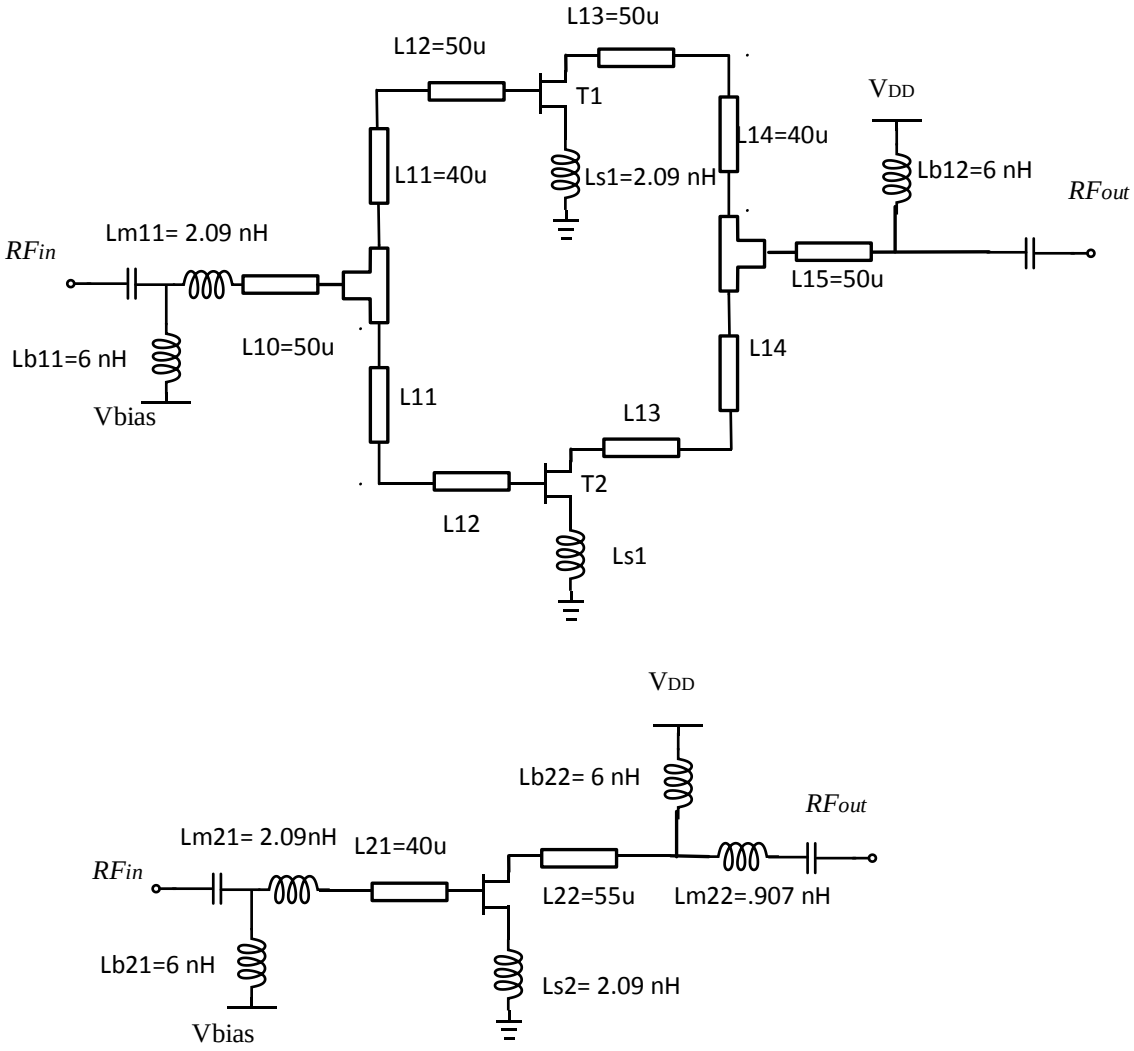



Figure 3.5 – Schematic of designed parallel and single path LNAs

the main issues in this topology. Loss of input divider increases NF directly and must be negligible in comparison to LNAs NF. The following part represents and discusses the simulation results of proposed topology.

## 3.4 Simulation Results

The designed amplifier is implemented in a GaAs pHEMT process with 0.1-$\mu$ gate length.

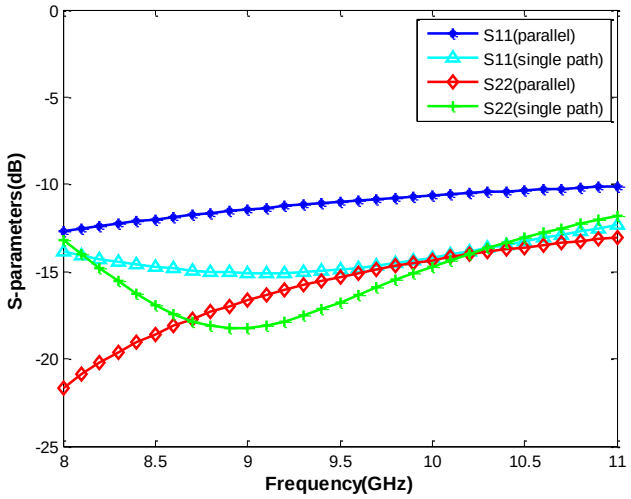



Figure 3.6 – S-parameter of both LNAs

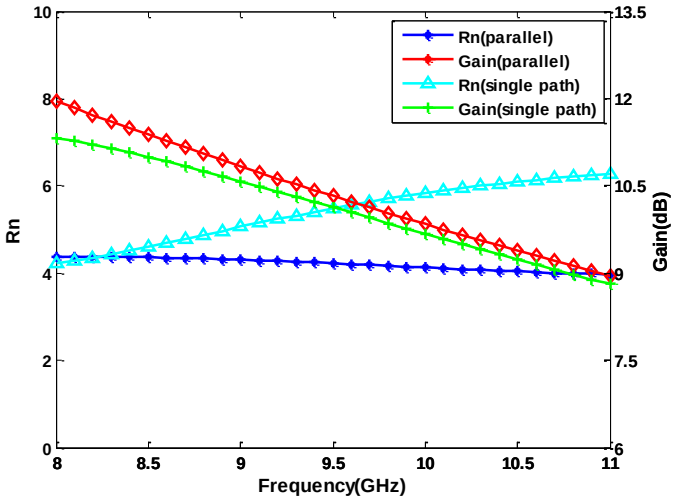



Figure 3.7 – $R_n$ and gain of both LNAs

Fig. 3.5. represents the schematic of designed amplifiers. The values of circuit elements is also shown in this figure. Simulation is done in order to compare single path with parallel amplifier performance. To validate the theoretical calculations a parallel amplifier is compared with a single path LNA. The goal is to design LNAs with a matching better than -10 dB in both input and output and a gain higher than 10 dB.

Input and output matching of single path and parallel LNA are shown in Fig. 3.6. It shows that the parallel amplifier have better $S_{11}$ and $S_{22}$ in comparison to single path LNA. This

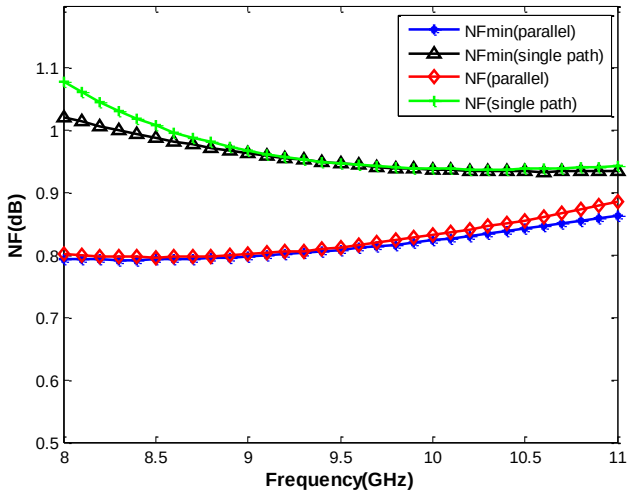



Figure 3.8 – NF and $NF_{min}$ of both LNAs

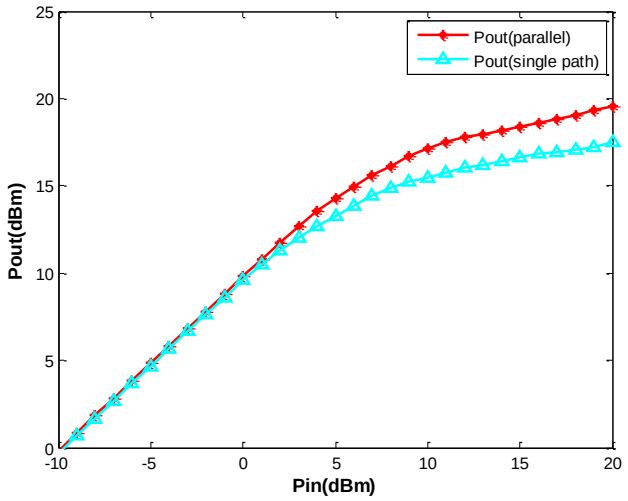



Figure 3.9 – Output power versus input power for both LNAs

fact leads to gain improvement of proposed topology in comparison to conventional IDCS amplifier as shown in Fig 3.7.

$R_n$ of amplifiers is represented in Fig. 3.7. The parallel amplifier's $R_n$ is lower than the other one and this causes its NF to be lower.

Fig. 3.8. shows that the parallel technique enhances NF of amplifier due to second order effect of $R_n$. Even though this improvement is marginal, the results show that the proposed topology can decrease the NF and also improves the input impedance matching. The

decrement of $R_n$ makes this kind of amplifier to be less sensitive to source impedance. Output versus input power of amplifier at $f = 10GHz$ is shown in Fig. 3.9. and parallel amplifier have 3-dB higher P-1dB than single path LNA.

## 3.5 Layout Results

To have a better insight on this design approach, the layout of both LNAs are also designed and compared. The layouts are also implemented in a GaAs pHEMT process with 0.1-$\mu$ gate length. The thickness of the substrate is 50 $\mu$m. The unity gain frequency $f_T$ and the maximum oscillation frequency $f_{max}$ of the process are 130 and 180 GHz. The process offers two metal layers with 1- and 2- $\mu$ thickness, air bridges, and ground back-vias. Moreover the other passive components of this process include the metal-insulator-metal (MIM) capacitors with a capacitance density of 400 $pF/mm^2$, and thin film and mesa resistors with sheet resistances of 50 and 140 $^{\Omega}/square$.
Two different LNAs are designed with bandwidth of 2 GHz for input and output matching better that -10 dB. These two LNAs exhibit a gain of about 8dB along the defined bandwidth. First LNA is a single path amplifier and second one is a parallel amplifier with two similar paths. The layout graph of both LNAs are depicted in Fig. 3.10.
Input and output matching of single path and parallel LNA are shown in Fig. 3.11. It shows that the $S_{11}$ and $S_{22}$ of parallel amplifier are better than single path LNA. This fact leads to gain improvement of proposed topology in comparison to conventional IDCS amplifier as shown in Fig. 3.12.
Fig. 3.12. also shows that $R_n$ of parallel amplifier is less than single path and it causes NF of this amplifier to be lower. Fig. 3.13. shows that parallel LNA topology can improve NF because of a second order factor. $R_n$ minimization causes amplifier to have less sensitivity to source impedance and decreases LNA's dependency to input matching circuit. The output power versus input power behavior of both amplifiers is represented in Fig. 3.14. It shows that p-1dB of parallel amplifier is 3-dB better than single path LNA as previously shown according to schematic simulations.

The designed circuit with proposed approach achieves the P1-dB of 3 dBm while consumes 76 mW compared to 0 dBm for conventional LNA with the power consumption of 58 mW.

To have a better comparison between both circuits their performance are compared using $FOM = \frac{G*BW*P1B}{NF*S_{11}*S_{22}*Power-Consumption}$. The LNA with proposed approach has a FOM

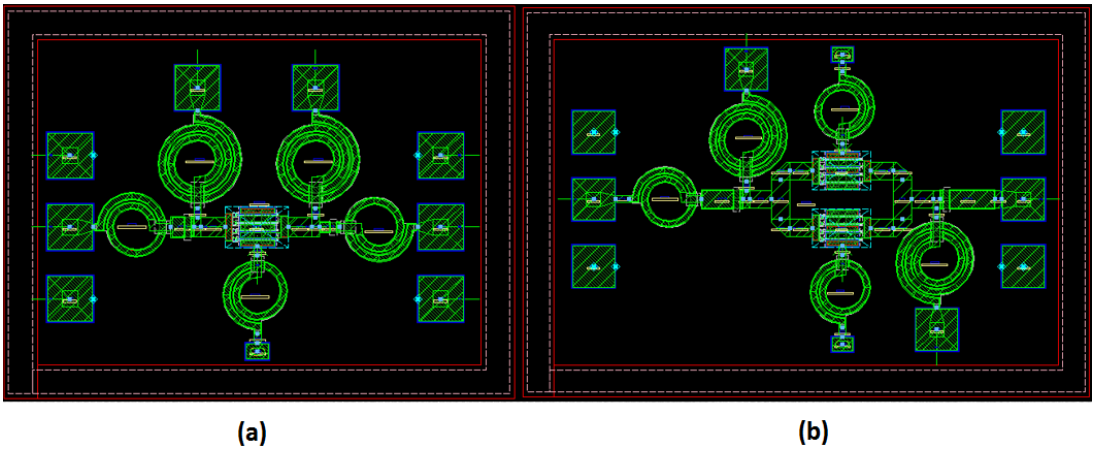



Figure 3.10 – Layout micrography of LNAs (a) Single stage LNA (b) Parallel LNA

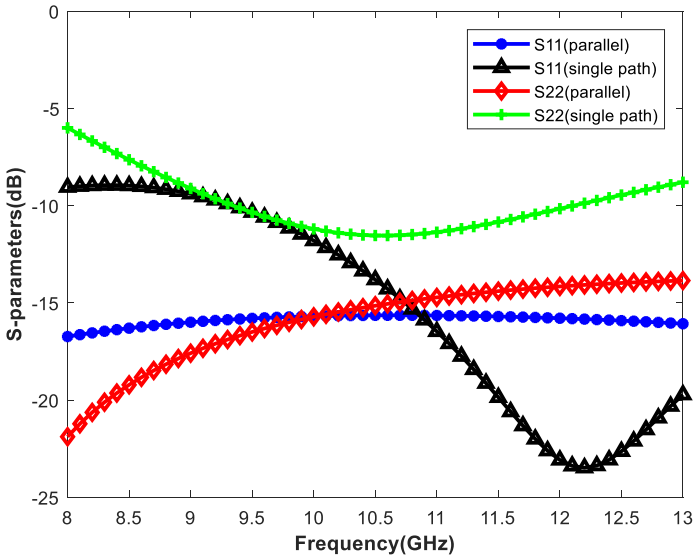



Figure 3.11 – S-parameter of both LNAs

of 145 compared to conventional one with FOM of 8 shows an improvement which means a better performance.

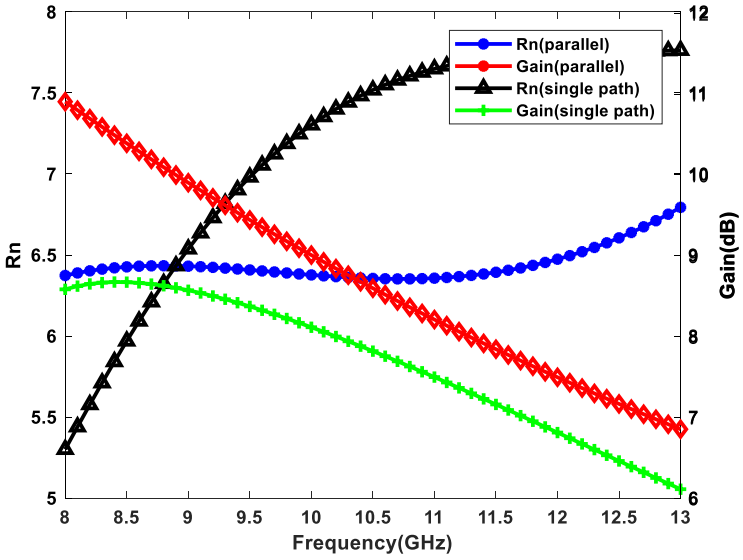



Figure 3.12 – $R_n$ and gain of both LNAs

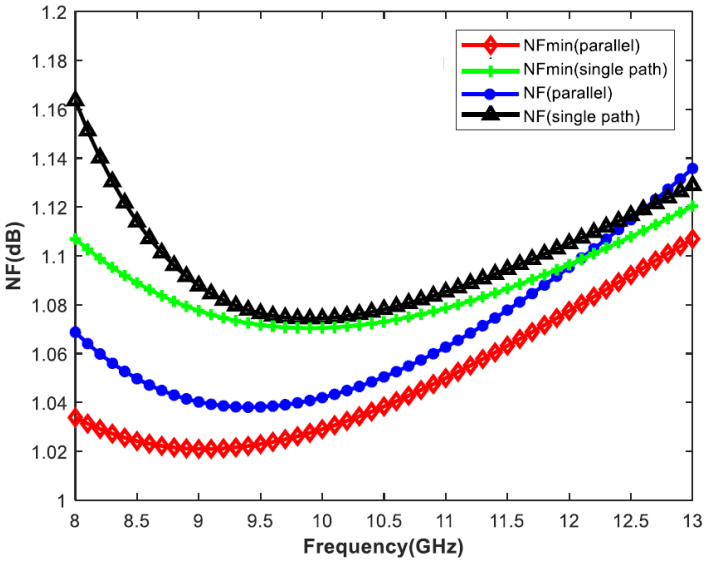



Figure 3.13 – NF and $NF_{min}$ of both LNAs

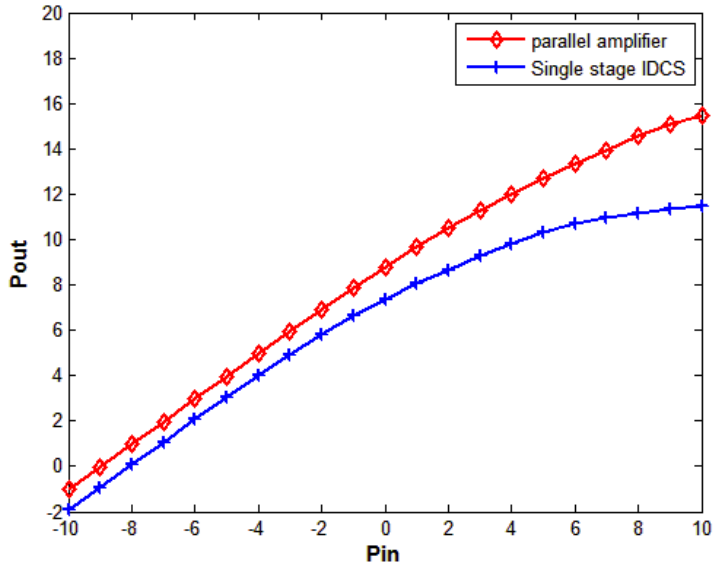



Figure 3.14 – Output power versus input power for both LNAs

Chapter 4

# Third Approach: New Noise Cancellation Topology In Common-gate LNAs

## 4.1 Introduction

The third design method presents a new approach in designing noise canceling common gate LNAs. In this part the condition of noise canceling is calculated and a design procedure is defined to obtain to have low-NF, high gain, with appropriate impedance matching in common gate noise-canceling LNAs. The analytical design procedure and its results are also published in [35]. In this method, in order to cancel the common gate's noise instead of a simple common source stage, IDCS is used and the constrains for achieving noise-cancellation are calculated based on analytical design.

Designing an LNA is based on several trade-offs. To achieve the lowest possible noise figure (NF) and return loss with high gain over the desired bandwidth several topologies in low noise amplifiers (LNAs) design have been investigated. A frequent approach is common gate (CG) amplifier which provides wideband input matching due to its input impedance of 1 over $g_m$. The basic topology of CG is shown in Fig. 4.1 (a). In this topology NF can be calculated as in Eq. 4.1.

$$NF = 1 + \frac{\gamma}{g_m R_s} + \frac{R_s}{R_l}(1 + g_m R_s)^2 \tag{4.1}$$

$R_s$ and $R_l$ are the source and load resistance respectively and $\gamma$ is the coefficient for the thermal noise of transistor. In matching condition this topology can achieve to a NF of $1+\gamma+\frac{4R_s}{R_1}$. Therefore, even if the input return loss remains in acceptable range over the frequency bandwidth, the NF is relatively high [4]. In this topology, different modifications have been previously proposed to decrease the NF of LNA in input matching conditions.

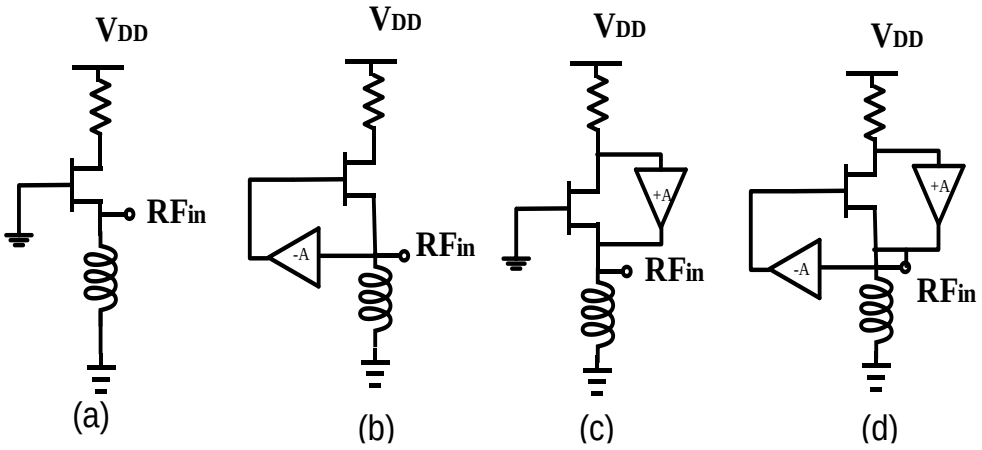



Figure 4.1 – Different common gate LNAs

These methods had the cost of extra parasitic elements that limit the frequency range of the LNA [5]-[54]. The Fig. 4.1 (b) represents utilization of feedback element to improve the NF of this topology. According to this method by increasing the effective $g_m$, the NF decreases due to the reduction of channel noise effect [3]. The positive feedback have been also previously used in [6] in order to decrease the NF of LNA in input impedance matching. Using both positive and negative feedback is also investigated in [7] which can improve the NF in input matching condition. Noise cancellation technique is the other approach used to improve the performance of CG stage[26],[55]-[56]. In this method a common source (CS) stage is used in parallel with CG stage to cancel its noise in expense of a limitation on the bandwidth of the LNA due to its capacitive input impedance. Moreover, the CS topology, itself has relatively high NF. Another low noise LNA with similar behavior to CS topology that can cancel out the noise of CG is inductively degenerated common source (IDCS). This topology is very common in high frequency LNAs with a very low noise behavior because of its capability of simultaneous impedance and noise matching (SNIM) for achieving minimum possible NF along with maximum gain [13], [16], [67]-[62]. In this topology, an inductor is added at the source terminal of the CS stage to achieve noise and impedance matching condition simultaneously by setting $\Gamma_{opt} = \Gamma_{in}^{*}$ [17], [57]-[58], [62]. In this section, design procedure of new noise cancellation technique by using an IDCS stage instead of CS stage, is discussed. In spite of conventional method which uses CS stage to cancel out the noise of CG, IDCS parallel with CG

stage is used. The analytical calculation for achieving noise cancellation condition is calculated. MATLAB simulation is used to show the reduction of noise in proposed method in comparison to conventional method. To validate the theoretical analysis, two different LNAs with conventional method and proposed one are designed and compared using ADS (Advanced Design System) with technology file of GaAs pHEMT 0.1 $\mu m$. This section is arranged in two main parts. In the first section, analytical calculation of overall NF and noise cancellation condition are presented. In next section, the noise behavior of two noise cancellation methods are compared using MATLAB simulation. In the third section two different circuits have been designed and compared using Electromagnetic simulation with utilization of GaAs pHEMT 0.1 $\mu m$ process model. The designed circuit's simulation results confirm the performance improvement of proposed topology.

## 4.2 Noise Analysis

To calculate the noise factor of the LNA, transfer function of each noise sources have been calculated. The topology of proposed LNA which uses an IDCS stage instead of CS is presented in fig. 4.2. The noise model of transistor is also shown in fig. 4.3. Due to their inconsiderable effect, noise of $R_d$ and $R_s$ (parasitic resistors in the drain and source) are neglected. Also the effect of the output resistance of the transistor $r_o$, gate noise resistor $R_g$, gate-drain capacitance $C_{gd}$ and drain-source capacitance $C_{ds}$ is neglected in this analysis for simplicity. Considering $i_{nd}$ which represents the noise current in the drain, transfer function of the output voltage with respect to noise sources is calculated. $i_{nd1}$ and $i_{nd2}$ are the drain noise source of common gate and common source stage, respectively and $V_{out} = V_{out_+} - Vout_-$.

$$\overline{i_{nd}^2} = 4kTg_m\gamma\Delta f \tag{4.2}$$

To reach real value for input impedance of IDCS stage, the source inductor is selected in a way that $C_{gs2}L_s\omega^2 = 1$. Therefore, to obtain input impedance matching condition, Eq. (4.3) should be met:

$$\begin{gathered} g_{m1} + \frac{C_{gs2}}{g_{m2}L_s} = \frac{1}{R_s} \Rightarrow \\ g_{m2}L_s g_{m1}R_s + C_{gs2}R_s = g_{m2}L_s \end{gathered} \tag{4.3}$$

Considering these constraints and $Z_1 = R_1$ (The impedance located in drain of common gate stage as shown in Fig. 4.2) , the transfer function of CG and IDCS stage's noise

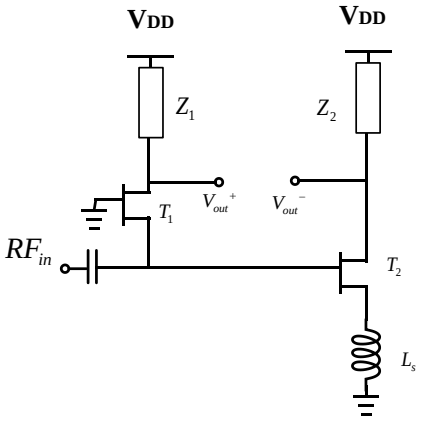



Figure 4.2 – Schematic of new noise cancellation technique

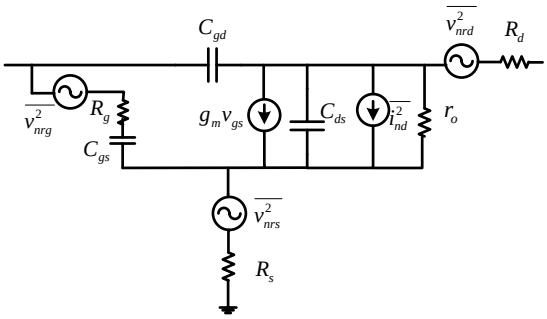



Figure 4.3 – Noise model of transistor

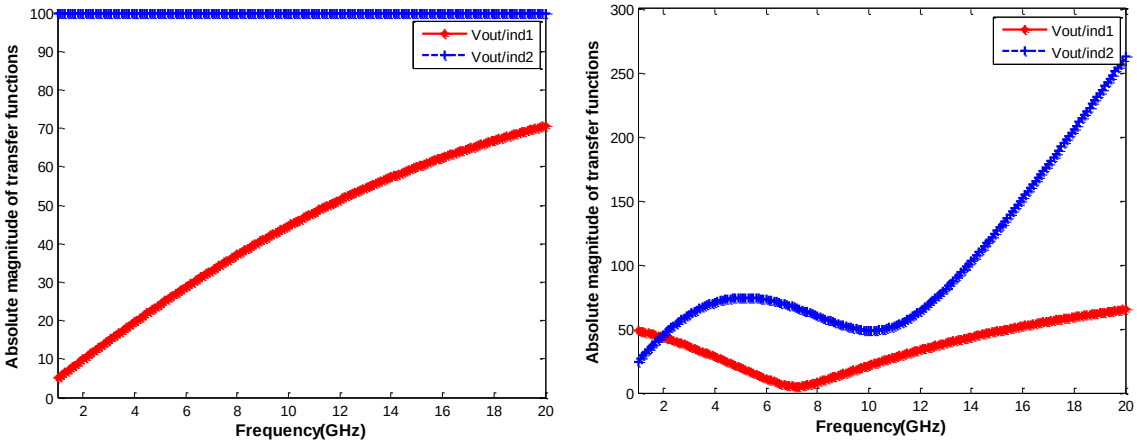



Figure 4.4 – Absolute magnitude of transfer functions: (a) Conventional method (b) Proposed method

sources are calculated in Eq. (4.4-4.5). The transfer function of source voltage is also shown in Eq. (4.6).

$$A = \frac{V_{out}}{i_{nd1}} = \frac{(R_1 C_{gs2} R_s + L_s R_1 g_{m2})s - Z_2 g_{m2} R_s)}{2 L_s g_{m2} s} \tag{4.4}$$

$$B = \frac{V_{out}}{i_{nd2}} = C_{gs2} R_s \frac{R_1 g_{m1} L s + Z_2}{(L_{ss} g_{m2}(1 + R_s g_{m1}) + C_{gs2} R_s)} \tag{4.5}$$

$$C = \frac{V_{out}}{v_{ns}} = g_{m2} R_s \frac{(R_1 g_{m1} L_s s + Z_2 g_{m2})}{(L_s g_{m2}(1 + R_s g_{m1}) + C_{gs2} R_s)} \tag{4.6}$$

Finally the overall NF can be calculated using the following equation:

$$NF = 1 + \gamma g_{m1} \frac{|A|^2}{|C|^2} + \gamma g_{m2} \frac{|B|^2}{|C|^2} \tag{4.7}$$

To have the noise cancellation condition, it is known that the transfer function of CG stage's noise source should be equal to zero. This condition is met using Eq. (4.8).

$$|A|^2 = \left|\frac{V_{out}}{i_{nd1}}\right|^2 = \left|\frac{(R_1 C_{gs2} R_s + L_s R_1 g_{m2})s - Z_2 g_{m2} R_s)}{(L_s g_{m2}(1 + R_s g_{m1}) + C_{gs2} R_s)s}\right|^2 = 0 \tag{4.8}$$

This equation shows that the load of IDCS stage should be inductive and its inductor value can be calculated using Eq. (4.9).

$$\begin{aligned} R_1 C_{gs2} R_s + L_s R_1 g_{m2} - L_2 g_{m2} R_s = 0 \\ L_2 = \tfrac{R_1 C_{gs2}}{g_{m2}} + \tfrac{L_s R_1}{R_s} \end{aligned} \tag{4.9}$$

Under these circumstances, this topology can be used as a CG noise cancellation method which can decrease the NF in comparison to conventional approach. To have a better look on this topology, we used MATLAB code to show the transfer function of each stage in both conventional and proposed topology in frequency range visually.
As Fig. 2.26. shows due to the effect of considering $C_{gs}$ in calculations, the transfer function of $v_{out}/i_{nd1}$ in conventional method is not exactly equal to zero. These two LNAs are designed to have noise cancellation condition at $f = 10GHz$ as well as input impedance matching. Due to derived equations, the value of source inductance of IDCS stage is calculated. The transfer function of each noise sources are shown in Fig. 4.4. in both methods. The results show that the magnitude of transfer function of noise sources can

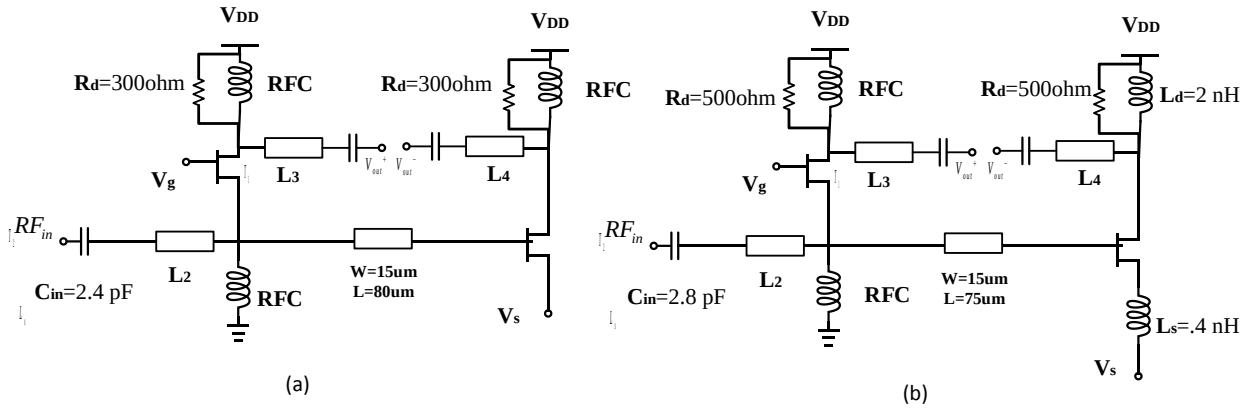



Figure 4.5 – Schematic of designed LNAs: (a) Conventional method (b) Proposed method

be reduced in proposed method over the designed frequency band which can lead to reduction in NF.

## 4.3 Circuit Design

To validate the theoretical and simulation results, two different noise canceling CG LNA with conventional approach and proposed approach have been designed using ADS. These two LNAs have been optimized and designed using GaAs pHEMT .1 $\mu m$ process model. In this process the thickness of the substrate is 50 $\mu$m. This process offers two metal layers with 1- and 2- $\mu$m thickness, air bridges, and ground back-vias. The unity gain frequency $f_T$ and the maximum oscillation frequency $f_{max}$ of the process are 130 and 180 GHz. Other passive components of this process include the metal-insulator-metal (MIM) capacitors with a capacitance density of 400 $pF/mm^2$, and thin film and mesa resistors with sheet resistances of 50 and 140 $^{\Omega}/square$ respectively.

The LNAs are designed in X-band. The first LNA is optimized considering the conventional noise cancellation technique by using CS stage and the second LNA is designed by using an IDCS stage. The transistors in this process have relatively higher $g_m$ than 20mS. This makes it harder for the conventional approach to have good input matching but it has rather low NF. On the other hand the proposed approach due to real value of the input impedance in IDCS stage can have better input matching.

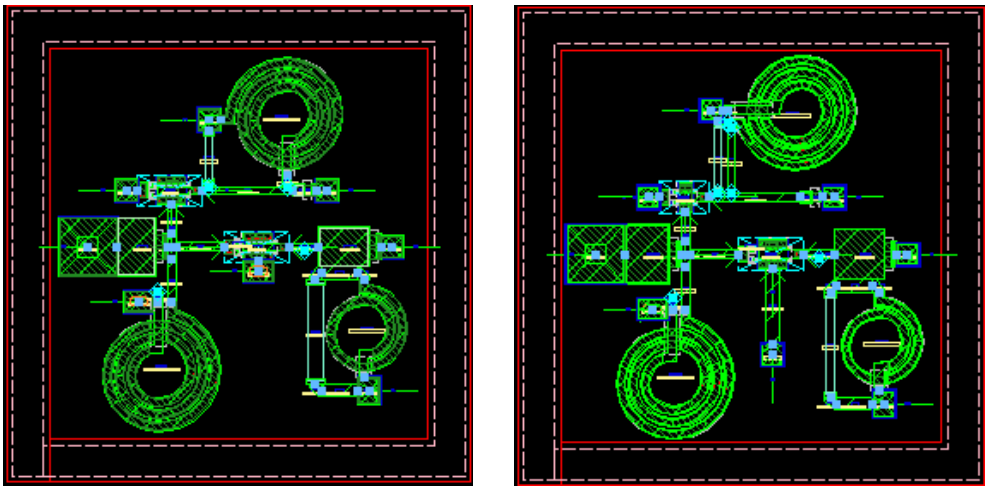


Figure 4.6 – Layout micro-graph of designed LNAs: (a) Conventional method (b) Proposed method

The schematic of both LNAs are depicted in Fig. 4.5. The output matching of each stage is designed to meet its own load requirement. As it can be seen in this figure, for the placement issues there is a need to have a line in the gate of the common source stage which can have an adverse effect on the performance of the circuit due to the delay in the signal path. However, in the frequency band of this circuit according to the size of this line, this effect is negligible and did not affect the performance of the circuit but it should be considered in higher frequency applications. In the proposed method by adding a degree of freedom with source inductor the noise cancellation condition can happens with lower $g_{m2}$ in comparison to conventional method. This can lead to less power consumption. In the designed LNAs, the proposed method can achieve less power consumption. The size of common gate transistors are chosen to be $2 * 50\mu m$ and size of transistors in common source stages are chosen to be $2 * 50\mu m$ and $2 * 30\mu m$ in both conventional and proposed method respectively. The preliminary value of design parameters are calculated using MATLAB simulation. In order to achieve best matching in both input and output of both LNAs, ADS optimization is also done to choose the appropriate values for circuit elements. In this case, simulation results show the performance improvement of proposed approach in comparison to conventional design method. To consider the high frequency effects of elements, electromagnetic momentum simulation is done for both LNAs. The layout micro-graph of both LNAs are represented in Fig. 4.6. The NF and gain performance of both LNAs are represented in Fig. 4.7. It can be seen that the NF decreases in the proposed approach and the gain have a slight increment. The S-parameters of both LNAs

Table 4.1 – Performance comparison of LNAs with similar design approach and bandwidth

| Ref | Technology | BW (GHz) | Power (mW) | Gain (dB) | $S_{22}$ (dB) | $S_{11}$ (dB) | NF (dB) | P-1dB (dBm) | FOM |
|---|---|---|---|---|---|---|---|---|---|
| [63] | .18um CMOS | 2.4-9 | – | 24 | -10 | -7.5 | 3.16 | - | - |
| [64] | .18um CMOS | 1.2-11.9 | 20 | 9.7 | -11 | -10 | 4.5 | -17 | 3.24 |
| [65] | .18um CMOS | 1.25-11.34 | 5.8 | 11 | -11 | – | 2.4 | - | - |
| [66] | .18um CMOS | 3.1-10.6 | 12.5 | 13.4 | -10 | -10 | 4.5 | -16 | 3.58 |
| [67] | .13um CMOS | 3.1-10.6 | 9.13 | 15.33 | -10 | -10 | 3.45 | -16.8 | 5 |
| This | 100nm GaAs | 9.8-11 | 56.6 | 6.5 | -11 | -10 | 2.25 | 4 | 17.5 |
| **This** | **100 nm GaAs** | **10-12** | **43.5** | **7** | **-8** | **-11** | **1.75** | **2** | **41.5** |

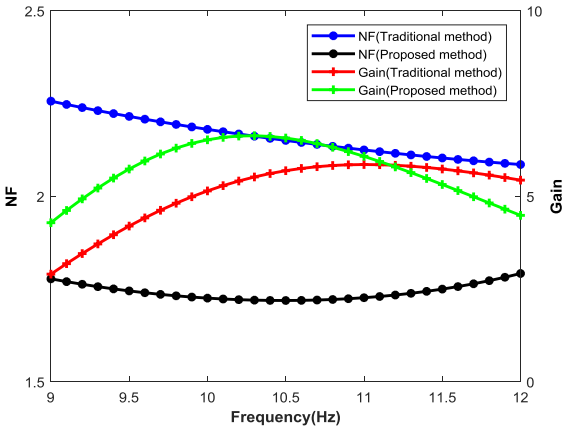



Figure 4.7 – NF and Gain of both LNAs

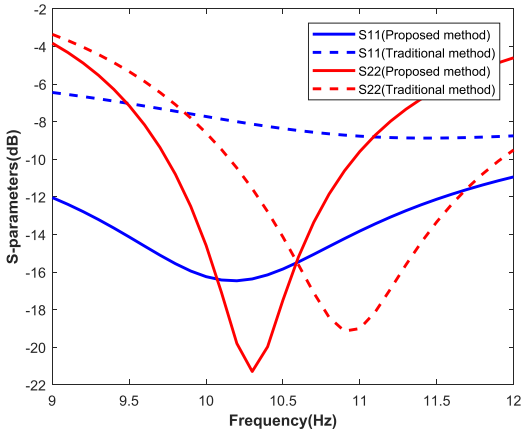



Figure 4.8 – S-parameters of both LNAs

are depicted in Fig. 4.8. The $S_{11}$ of the proposed method is better than -12 dB while the input matching condition in conventional method is better than -8 dB. The output matching in both topologies have a narrow band behavior and at the center frequency the $S_{22}$ of both LNAs are better than -10 dB.
The designed LNAs are compared with similar works with different technology files in table 4.1. As it can be seen in this table, the designed LNA can achieve the lowest NF and the best input impedance matching among all presented works. The designed circuit with proposed approach achieves the P1-dB of 2 dBm while consumes 43.5 mW compared to 4 dBm for conventional LNA with the power consumption of 56.6 mW.

To have a better comparison between circuits their performance are compared using $FOM = \frac{G*BW*P1B}{NF*S_{11}*S_{22}*Power-Consumption}$. The LNA with proposed approach has a FOM of 41.5 compared to conventional one with FOM of 17.5 shows an improvement which means a better performance. It also has a better FOM compared to previous works. The comparison between power consumption of these LNAs shows that the presented work, consumes higher power than CMOS LNAs due to its different process. On the other hand the proposed approach consumes less power in comparison to conventional noise cancellation technique in same process.

# CONCLUSION

In this thesis, three different approaches for performance improvement of high frequency wide-band LNAs are proposed. In all these approaches, analytical calculations are done in order to find the optimum design. Based on analytical design in each method, two different LNAs using proposed and conventional method are designed and compared in order to represent the effectiveness of proposed approaches. The conclusion of each method are given in this chapter.

### 4.3.1 First Approach: Optimization Of LNA's First Stage To Reduce Overall Noise Figure in Multi-Stage LNAs

In this method, a new methodology for optimization of first stage of multistage LNA is presented. This method has investigated the effect of following stage's noise in optimization of $\Gamma_s$ of LNA. Analytical calculations prove that overall-NF contours are different from constant NF circles in $\Gamma_s$ Smith-chart and $\Gamma_{opt}$ changes while considering following stage's noise. This method can be used for optimization of gain and NF simultaneously. The analytical solution shows that consideration of overall LNA in optimization of gain and NF, leads to improvement of its performance. The results of EM-simulation of LNA's layout are given for both conventional and proposed method. This result shows the feasibility of proposed design approach. Also comparing this method with conventionally used approach shows that with slight degradation in first stage's NF, its gain can be improved in way that overall-NF decreases.
To prove the theoretical and simulation results a discrete multi stage LNA has been designed with ATF13136 transistor and the results confirm the proposed method's performance improvement in comparison to conventional design method. The designed LNA with proposed method shows lower NF and higher gain with ADS momentum simulation in comparison to conventional method because it have better input matching optimization.

### 4.3.2 Second Approach: Parallel Amplifier Design Technique

In this method theoretical analysis results for parallel amplifier are presented and for the special case of two IDCS amplifiers in both coupled and uncoupled source inductors the noise parameters are calculated. The analytical results in both cases represent that using this topology can decrease $R_n$ which leads to better input impedance matching as well as less sensitivity of NF to input impedance. To confirm proposed theories, two LNAs (single path and parallel amplifiers) are designed in 0.1-$\mu$ GaAs pHEMT process in both schematic and layout simulation. The parallel LNA in schematic design have the average gain of 10.5 dB at 8-11 GHz. The impedance matching in input and output are better than -10 dB and -14 dB respectively while single stage IDCS LNA shows an average gain of 10 dB at 8-13 GHz and also the impedance matching in both input and output are better than -12 dB. In layout design, the parallel LNA exhibits the gain of 11 dB at 8 GHz with 3-dB gain bandwidth of 8-11.5 GHz, with input and output impedance matching better than -14 dB while single stage IDCS LNA shows a gain of 9 dB at 8 GHz with 3-dB gain bandwidth of 8-13 GHz, with input and output impedance matching better than -10 and -7 dB respectively. Output saturation power in both schematic and layout design improves 3dB because of parallel path, therefore this topology is considered as linear LNA. In this method input matching circuit design is simplified because of decrement in $R_n$. Simulation results show with no considerable change in $NF_{min}$ and similar input matching condition ($S_{11} < -10dB$) parallel topology NF is less than single path amplifier. As a result, even though the input divider and output combiner have losses and increase the NF slightly, the effect of $R_n$ decrement makes overall NF to be lower in parallel amplifier.

### 4.3.3 Third Approach: New Noise Cancellation Topology In Common-gate LNAs

In this method a new methodology for designing noise cancellation CG LNAs is proposed. In this approach instead of a CS stage for canceling CG stages' noise an IDCS stage is utilized. The analytical calculations including matching, NF, gain, noise cancellation conditions are presented in order to calculate design parameters of this topology. Using MATLAB simulation the analytical analysis of proposed and conventional method are compared in term of the behavior of noise sources' transfer functions. The results have shown that according to proposed topology the absolute magnitude of transfer function of noise sources decreases in comparison to conventional noise canceling technique which

leads to better NF performance. To validate the theoretical analysis, two different noise canceling LNAs are designed. The first LNA is designed using a CS stage in parallel with CG stage and the second one is designed using IDCS instead of CS stage. The EM simulation results have shown that in proposed method the NF is decreased and better input impedance matching is obtained. The obtained analytical and simulation results of this topology represent that the proposed method can have a better performance compared with the conventional method and can be used in wide-band low-NF CG LNAs.

### 4.3.4 Limitation of the research

In this study, due to the lack of access to the integrated circuits, the proposed ideas were analyzed and verified in the form of integrated circuit simulations.
The first idea of the circuit was made as a discrete circuit and tested.
Regarding the second and third ideas and their comparison with the conventional method, this issue has not been possible due to the following limitations:

- In the second idea, we need two similar stages to be able to compare their performance with a single-circuit exactly the same transistor properties. This problem is much more pregnant for discrete transistors where their performances are directly linked with the process changes.
- There is also the issue of transistors being not identical for comparison in the third method. This is important because the ideas presented have been analyzed with the aim of improving conventional design methods and should be performed under exactly the same conditions. This hypothesis could be more easily performed for integrated circuit amplifiers.

### 4.3.5 Perspectives for future works

In the continuation of this research, it is suggested that the ideas proposed at higher frequencies and in the integrated circuit have to be constructed and examined.
In the following, the first method seems to be very helpful in designing single stage low-noise amplifier circuits in the receiver, after which there is high noise in the rest of the receiver circuit, and it seems that in such conditions this optimization method can be used for optimal design.
In the second method, the use of noise matrix analysis could be generalized in an optimal way to analyze and improve the performances of amplifier with parallel path. That is to

say, by adding a auxiliary parallel path to an amplifier and optimizing its noise matrix parameters, the noise parameters of overall amplifier can be optimized in order to ameliorate the noise performance of overall amplifier.
In the third method, due to the proper performance of this circuit in the simulation, it is possible to use this topology due to its broadband behavior with low noise and proper input matching as a suitable topology to replace the common gate circuit to cancel its noise. The future works can utilize this approach in different processes in order to achieve both wide-band behavior of common gate LNAs as well as low NF of inductively degenerated common source stage.

# BIBLIOGRAPHY


[1] I. J. Bahl, Fundamentals of RF and Microwave Transistor Amplifiers, John Wiley and Sons, Inc. Publication, 2009.

[2] T. H. Lee, Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits, Cambridge university press, 2004.

[3] D.M.Pozar, Microwave and RF Design of Wireless Systems, John Wiley and Sons, Inc., 2001.

[4] B.Razavi, RF microelectronics, Prentice Hall, 1998.

[5] J.Kim, S.Hoyos and J.S.Martinez, "Wideband Common-Gate CMOS LNA Employing Dual Negetive Feedback With Simultanous Noise, Gain, and Bandwidth Optimization," IEEE Transactions on Microwave and Techniques, vol. 58, pp. 2334-2351, 2010.

[6] H.G.Han, D.H.Jung and T.W.Kim, "A 2.88 mW +9.06 dBm IIP3 Common-Gate LNA With Dual Cross-Coupled Capacitive Feedback," IEEE Transactions on Microwave Theory and Techniques, vol. 63, pp. 1019-1025, 2015.

[7] A.Liscidini, M.Brandolini, D.sanzogni and R.Castello, "A 0.13 um CMOS Front-End for DCS1800/UMTS/802.11b-g with Multi-Band Positive Feedback Low Noise Amplifier," in Symposium on VLSI Circuits Digest of Technical Papers, 2005.

[8] A. Liscidini, G. Martini, D. Mastantuono and R. Castello, "Analysis and Design of Configurable LNAs in Feedback Common-Gate Topologies," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 55, pp. 733-737.

[9] W. Chen, S. Chang and G. Huang, "A Ku-Band Interference-Rejection CMOS Low-Noise Amplifier Using Current-Reused Stacked Common-Gate Topology," IEEE Microwave And Wireless Component Letters, vol. 17, pp. 718-120, 2007.

[10] M. Sato, T. Takahash and T. Hirose, "68–110-GHz-Band Low-Noise Amplifier Using Current Reuse Topology," IEEE Transactions on Microwave Theory and Techniques, vol. 58, pp. 1910-1917, 2010.

[11] W. H. Chen, "Designs of Broadband Highly Linear CMOS LNAs for Multiradio Multimode Applications," ph.D thesis on Electrical Engineering and Computer Sciences University of California at Berkeley, California, 2009.

[12] M. Sabzi, A. Medi, "Analysis and design of multi-stage wideband LNA using simultaneously noise and impedance matching method," in *Microelectronics Journal*, Vol. 86, pp. 97–104, 2019.

[13] L. Belostotski and J. W. Haslett, "Noise Figure Optimization of Inductively Degenerated CMOS LNAs With Integrated Gate Inductors," IEEE Transaction On Circuits and Systems, vol. 53, pp. 1409-1422, 2006.

[14] S. Weng, C. Lin, H. Chang and C. Chiong, "Q-band Low Noise Amplifiers Using a 0.15-μm MHEMT Process for Broadband Communication and Radio Astronomy Applications," IEEE Microwave Theory and techniques, International Microwave Symposium Digest, pp. 455-459, 2008.

[15] S. Yoo and H. Yoo, " Compact Reconfigurable LNA for Single Path Multistandard Receiver," IEEE Conference on Electron Devices and Solid-State Circuits, pp. 461-464, 2007.

[16] D. Shaeffer, "A 1.5 V 1.5 GHz CMOS Low Noise Amplifier," IEEE Journal of Solid-State Circuits, vol. 32, 1997.

[17] T. Nguyen, C. Kim, G. Ihm, M. Yang and S. Lee, "CMOS Low-Noise Amplifier Design Optimization Techniques," IEEE Transactions On Microwave Theory And Techniques, vol. 52, pp. 1433-1443, 2004.

[18] M. T. Reiha and J. R. Long, "A 1.2 V Reactive Feedback 3.1–10.6 GHz Low-Noise Amplifier in 0.13 um CMOS," IEEE Journal Of Solid State Circuits, vol. 42, pp. 1023-1033, 2006.

[19] S. Masuda, T. Ohki and T. Hirose, "Very Compact High-Gain Broadband Low-Noise Amplifier in InP HEMT Technology," IEEE Transactions On Microwave Theory And Techniques , vol. 54, pp. 4565-4572, 2006.

[20] H. Zhang and E. Sánchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," IEEE Transaction on Circuits and Systems, vol. 58, pp. 22-37, 2011.

[21] S. Narayanan, "Application of Volterra series to intermodulation distortion analysis of transistor feedback amplifies," IEEE TransAction Circuit Theory, vol. 17, pp. 518-527, 2004.

[22] T. W. Kim, B. Kim and K. Lee, "Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors," IEEE Journal of Solid-State Circuits, vol. 39, pp. 223-229, 2004.

[23] B. Toole, C. Plett and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETS," IEEE Transactions on Circuits and Systems, vol. 51, pp. 319-328, 2004.

[24] Y. Ding and R. Harjani, "A +18 dBm IIP3 LNA in .35 um CMOS,"," in IEEE International Solidstate Circuits Conference, 2001.

[25] S. Lou and H. C. Luong, "A linearization technique for RF receiver front-end using second-order-intermodulation injection," IEEE Journal of Solid-State Circuits, vol. 43, pp. 2402-2412, 2008.

[26] J. Jussila and P. Sivonen, "A 1.2-V highly linear balanced noise-cancelling LNA in 0.13-um CMOS," IEEE Journal of Solid-State Circuits, vol. 43, pp. 579-587, 2008.

[27] W. Chen, G. Liu, B. Zdravko and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," IEEE Journal of Solid-State Circuits, vol. 43, pp. 1164-1176, 2008.

[28] N. Kim, V. Aparin, K. Barnett, C and Persico, "“Acellular-bandCDMA 0.25 um CMOS LNA linearized using active post-distortion," IEEE Journal f Solid-State Circuits, vol. 41, pp. 1530-1534, 2006.

[29] T. S. Kim and B. S. Kim, "Post-linearization of cascode CMOS LNA using folded PMOS IMD sinker," IEEE Microwave Wireless Component Letters, vol. 16, pp. 182-184, 2006.

[30] H. Zhang, X. Fan and E. Sánchez-Sinencio, "A low-power, linearized,ultra-wideband LNA design technique," IEEE Journal of Solid-State Circuits, vol. 44, pp. 320-330, 2009.

[31] G.Breed, "A Comparison of RFIC Fabrication Technologies," Summit Technical Media, 2006.

[32] M. Sabzi, M. Kamarei, T. Razban, Y. Mahe,' Optimization of LNA's first stage to reduce overall noise figure in multi-stage LNAs', AEU - International Journal of Electronics and Communications, Volume 123, 2020, 153300/

[33] M.Sabzi, M. Kamarei, T. Razban, Y. Mahé, 'Parallel Amplifiers Technique for LNA Design. Fifth Sino-French Workshop on Information and Communication Technologies (SIFWICT 2019)', Jun 2019, Nantes, France.

[34] M. Sabzi, M. Kamarei, T. R. Haghighi and Y. Mahe, "Analysis and Design of X-Band LNA Using Parallel Technique," 2020 28th Iranian Conference on Electrical Engineering (ICEE), Tabriz, Iran, 2020, pp. 1-5, doi: 10.1109/ICEE50131.2020.9260604.

[35] M. Sabzi, M. Kamarei, T. Razban, Y. Mahe, 'New noise cancellation topology in common-gate LNAs', Microelectronics Journal, Volume 100, 2020, 104800.

[36] W. Ciccognani, E. Limiti, P. Longhi, M. Renvoise, "MMIC LNAs for radioastronomy applications using advanced industrial 70 nm metamorphic technology", IEEE J. Solid-State Circuits 45 (2010), 2008-2015

[37] H. A. Haus, R. B. Adler, "Optimal noise performance of linear amplifiers", Proc. IRE 46 (1958), 1517-1533

[38] R. B. Adler, H. A. Haus, "Network realization of optimum amplifier noise performance", IRE Trans. Circuit Theory 5 (1958), 156-161

[39] H. Rothe, W. Dahlke, "Theory of noisy four poles", Proc. IRE 44 (1956), 811-818

[40] H. A. Haus, "Representation of noise in linear twoports", Proc. IRE 48 (1960), 69-74

[41] W. Ciccognani, P. Longhi, S. Colangeli, E. Limiti, "Constant mismatch circles and application to low-noise microwave amplifier design", IEEE Trans. Microwave Theory Tech. 61 (2013), 4154-4167

[42] K. Kim and C. Nguyen, "A V-Band Power Amplifier With Integrated Wilkinson Power Dividers-Combiners and Transformers in 0.18- $\mu$ m SiGe BiCMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 3, pp. 337-341, March 2019.

[43] T. W. Kim, "A Common-Gate Amplifier With Transconductance Nonlinearity Cancellation and Its High-Frequency Analysis Using the Volterra Series," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 6, pp. 1461-1469, June 2009.

[44] C. Li, S. Chou, C. Lai, C. Hsieh, J. Y. Liu and P. Huang, "A feedforward noise and distortion cancellation technique for CMOS broadband LNA-mixer," in 2014 IEEE Asian Solid-State Circuits Conference (A-SSCC), KaoHsiung, 2014, pp. 337-340.

[45] A. Zokaei, A. Amirabadi and M. Ghasemzadeh, "A 130 nm wideband fully differential linear low noise amplifier," in 2015 22nd International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), Torun, 2015, pp. 229-233.

[46] B. Guo and X. Li, "A 1.6–9.7 GHz CMOS LNA Linearized by Post Distortion Technique," in IEEE Microwave and Wireless Components Letters, vol. 23, no. 11, pp. 608-610, Nov. 2013.

[47] M. Parvizi, K. Allidina and M. N. El-Gamal, "An Ultra-Low-Power Wideband Inductorless CMOS LNA With Tunable Active Shunt-Feedback," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 6, pp. 1843-1853, June 2016.

[48] T. Stucke, N. Christoffers, R. Kokozinski, S. Kolnsberg and B. J. Hosticka, "Graphical Optimization of Common-Gate LNA," in 2006 Ph.D. Research in Microelectronics and Electronics, Otranto, 2006, pp. 453-456.

[49] M. Khurram and S. M. R. Hasan, "A 3–5 GHz Current-Reuse $g_m$-Boosted CG LNA for Ultrawideband in 130 nm CMOS," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 3, pp. 400-409, March 2012.

[50] E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari and E. Sanchez-Sinencio, "A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback," in IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 12, pp. 3154-3161, Dec. 2011.

[51] Y. Hsiao, C. Meng and C. Yang, "Design Optimization of Single-/Dual-Band FET LNAs Using Noise Transformation Matrix," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 2, pp. 519-532, Feb. 2016.

[52] P. Mahmoudidaryan and A. Medi, "Codesign of Ka-Band Integrated Limiter and Low Noise Amplifier," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 9, pp. 2843-2852, Sept. 2016.

[53] V. Papageorgiou and S. Vlassis, "CMOS LNA optimization techniques: Comparative study," 2010 17th IEEE International Conference on Electronics, Circuits and Systems, Athens, 2010, pp. 82-85.

[54] W. Sanghyun, K. Woonyun, and J. Laskar, "A 3.6 mW differential common-gate CMOS LNA with positive-negative feedback," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Paper (ISSCC) (2009), 218-219

[55] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," IEEE J. Solid-State Circuits 43 (2008) 1341–1350.

[56] K. H. Chen and S.-I. Liu, "Inductorless wideband CMOS low-noise amplifiers using noise-canceling technique," IEEE Trans. Circuits Syst. I, Reg. Papers, 59 (2012) 305–314.

[57] B. Aja, M. Seelmann-Eggebert, A. Leuther, H. Massler, M. Schlechtweg, J. D. Gallego, I. Lopez-Fernandez, C. Diez, I. Malo, E. Villa, E. Artal, '4-12 and 25-34 GHz

Cryogenic mHEMT MMIC Low-Noise Amplifiers', IEEE Trans. Microw. Theory Tech. 60 (2012), 4080–4088.

[58] C. Fu, C. Kuo, S. Taylor, Low noise amplifier design with dual reactive feedback for broadband simultaneous noise and impedance matching, IEEE Trans. Microw. Theory Tech. 58 (2010), 795–806.

[59] M. Daoud, R. Aloulou, H. Mnif, M. Ghorbel, 'Inductive degeneration low noise amplifier for IR-UWB receiver for biomedical implant', IEEE Int. Conf. on Microelectronics (ICM) (2015), 95–98.

[60] S. Bhaumik, D. Kettle, Broadband X-band low noise amplifier based on 70 nm GaAs metamorphic high electron mobility transistor technology for deep space and satellite communication networks and oscillation issues, IET Microwaves, Antennas and Propagation 4 (2010), 1208–1215.

[61] M. S. Heins, J. M. Carrol, M. KAO, J. Delaney, C. F. Campbell, 'X-band GaAs mHEMT LNAs with 0.5 dB NF', Microwave Symp. Digest. 1 (2004), 149–152.

[62] C. Feng, X. P. Yu, Z. H. Lu, W. M. Lim, W. Q. Sui, 3-10 GHz self-biased resistive-feedback LNA with inductive source degeneration, Electronic Letters 49 (2013), 387–388.

[63] M. Anwar, S. Azeemuddin, and M. Zafar Ali Khan. 'Design and Analysis of a Novel Noise Cancelling Topology for Common Gate UWB LNAs.' VLSI Design and Test, (2013), 169–176.

[64] C. F. Liao and S. I. Liu, 'A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers,' IEEE J.Solid-State Circuits, 42 (2007), 329—339.

[65] A. Jamalkhah, A. Hakimi, 'An ultra-wideband common gate LNA with gm-boosted and noise cancelling techniques', In 21st Iranian Conference on Electrical Engineering (ICEE), 2013, Iran , 1–5.

[66] J. Liu ,G. Chen , R. Zhang, 'Design of a noise-canceling differential CMOS LNA for 3.1–10.6 GHz UWB receivers'. In: IEEE 8th International Conference on ASIC, ASICON 09, October 20–23, 2009. p. 1169.

[67] L. W. Chen, W. Ro-Min, H. Ren–Yuan, Ch. Shih-Kai, 'A 1.3 V noise-cancelling low noise amplifier for ultra wideband applications.' In 2016 IEEE 5th Global Conference on Consumer Electronics, 2016, p. 1–2.

DOCTORAT BRETAGNE LOIRE / MATHSTIC

UNIVERSITÉ DE NANTES

**Titre :** Analyse et amélioration des performances dans les LNA large bande haute fréquence

**Mot clés :** LNA, haute fréquence, large bande, NF, gain, adaptation d'impédance

**Résumé :** Dans cette thèse, 3 approches différentes pour l'amélioration des performances des LNA large bande haute fréquence sont présentées. Dans la première section, une nouvelle méthode d'optimisation basée sur le calcul analytique pour les LNA à plusieurs étages est présentée. Cette approche optimise le gain et la NF en considérant simultanément l'effet du bruit de l'étage suivant. Les résultats de la simulation et du circuit fabriqué montrent qu'en utilisant cette méthode d'optimisation, la NF globale des LNA à plusieurs étages peut être réduite. Dans la deuxième approche, la technique d'amplification parallèle dans la conception LNA est étudiée pour obtenir les meilleures performances de cette topologie. En utilisant cette méthode, les performances du LNA peuvent s'améliorer pour obtenir un gain plus élevé, une meilleure adaptation d'impédance d'entrée, une meilleure linéarité et une meilleure robustesse sans dégradation de la NF. Dans la troisième section, une nouvelle topologie d'annulation de bruit dans les LNA à porte commune pour améliorer les performances de ces topologies est présentée. Pour l'étage de suppression de bruit, un étage de source commune à dégénérescence inductive est utilisé, ce qui peut conduire à une meilleure adaptation simultanée du bruit et de l'impédance. Les calculs des paramètres de bruit représentent la condition d'annulation de bruit requise. Les résultats obtenus montrent qu'en utilisant cette approche, une meilleure correspondance de NF, de gain et d'impédance d'entrée peut être obtenue.

**Title:** Analysis and performance improvement in high frequency wide-band LNAs

**Keywords:** LNAs, high-frequency, wide-band, NF, Gain, Impedance matching

**Abstract:** In this thesis, 3 different approaches for performance improvement of high-frequency wide-band LNAs are presented. In the first section, a new optimization method based on analytical calculation for multi stage LNAs is presented. This approach optimizes gain and NF simultaneously considering the effect of following stage's noise. The simulation and fabricated circuit results represents that by using this optimization method, overall NF of multi-stage LNAs can be reduced. In the second approach, parallel amplifier technique in LNA design is investigated to achieve the best performance of this topology. By using this method the performance of the LNA can improve to achieve higher gain, better input impedance matching, better linearity and robustness without degradation in NF. In the third section, a new noise cancellation topology in common-gate LNAs for improvement of this topologies' performance is presented. For noise canceling stage, inductively degenerated common source stage is utilized which can leads to better simultaneously noise and impedance matching. The noise parameter calculations represents the required noise cancellation condition. The obtained results show that using this approach, better NF, gain and input impedance matching can be obtained.