



**HAL**  
open science

# Circuit-level approaches to mitigate the process variability and soft errors in FinFET logic cells

Alexandra Lackmann Zimpeck

► **To cite this version:**

Alexandra Lackmann Zimpeck. Circuit-level approaches to mitigate the process variability and soft errors in FinFET logic cells. Micro and nanotechnologies/Microelectronics. Institut Supérieur de l'Aéronautique et de l'Espace (ISAE); Universidade Federal do Rio Grande do Sul (Brésil), 2019. English. NNT: . tel-02890418

**HAL Id: tel-02890418**

**<https://hal.science/tel-02890418v1>**

Submitted on 6 Jul 2020

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



# THÈSE

**En vue de l'obtention du**

## **DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE**

**Délivré par :**

Institut Supérieur de l'Aéronautique et de l'Espace

Universidade Federal do Rio Grande do Sul (Brésil)

---

**Présentée et soutenue par :**  
**Alexandra LACKMANN ZIMPECK**

**le** mardi 24 septembre 2019

**Titre :**

Circuit-level approaches to mitigate the process variability and soft errors in FinFET logic cells

Approches au niveau du circuit pour atténuer la variabilité de fabrication et les soft errors dans les cellules logiques FinFET

---

**École doctorale et discipline ou spécialité :**

ED GEET : Micro et nanosystèmes

**Unité de recherche :**

Équipe d'accueil ISAE-ONERA OLIMPES

**Directeur(s) de Thèse :**

M. Ricardo REIS (directeur de thèse)  
M. Laurent ARTOLA (co-directeur de thèse)

**Jury :**

Mme Lirida NAVINER, Professeur Télécom Paris - Rapporteur, Présidente  
M. Ricardo REIS, Professeur UFRGS Brésil - Directeur de thèse  
M. Laurent ARTOLA, Ingénieur de Recherche ONERA - Co-directeur de thèse  
M. Remi BARBIER, Professeur ISAE-SUPAERO  
Mme Karine COULIÉ, Maître de Conférences Université Aix-Marseille - Rapporteur  
M. Marc GALLARDIN, Ingénieur CEA  
M. Paul LEROUX, Professeur KU Leuven Belgique  
Mme Cecilia MEZZOMO, Ingénieur Thales Alenia Space

# Acknowledgments

---

I would like to start by thanking my parents, Alexandre and Dulcinara, for the study encouragements since the earliest stages of my life, for all support provided me to achieve my goals, and for never letting me give up on my dreams. I thank my brother, Lucas, for unconditional love even though sometimes he didn't understand the reasons for the distance between us. Thank you for always been close to me, even when I have been a few thousand kilometers away from you. I also thank my husband, André Furlan, for your patience, support to achieve my goals and mainly, for accompanying me during my internship in Toulouse. I take the opportunity also to thank all my family and friends who always sent positive vibes for me and understood the several important moments when I could not be present.

I would like to thank my colleagues from UFRGS, Gracieli Posser, Calebe Micael, Tania Ferla, Jucemar Monteiro, Felipe Rosa, Walter Calienes, Vitor Bandeira, Geancarlo Abich, Mateus Fogaça, Lucas de Paris, Louise Etcheverry, Vladimir Afonso, Leonardo Brendler, Leonardo Moraes, Pablo Silva, for the friendship, confidence and the countless hours discussing a variety of subjects. My thanks to all my colleagues from ONERA, especially to Raphael Vieira and Neil Rostand for sharing studies, knowledge, and ideas, and Virnigie Inguibert for helping me understand better the French language. I would thank especially Prof. Cristina Meinhardt for all support in my scientific research since 2010, for the professional partnership on most varied subjects and her friendship during all these years.

I want to thank my advisor, Prof. Ricardo Reis, for always believing in my potential and for encouraging me to be better every day. I thank so much Prof. Fernanda Kastensmidt for her collaborations, discussions, and all support given for this work. I also thank Laurent Artola and Guillaume Hubert for the research opportunity and for all knowledge obtained inside of ONERA as well as for providing me a fantastic internship in France. Finally, I would like to thank all the supernatural forces that make us go forward until the end.

To all of you, my sincere thanks.

# Abstract

---

Process variability mitigation and radiation hardness are relevant reliability requirements as chip manufacturing advances more in-depth into the nanometer regime. The parameter yield loss and critical failures on system behavior are the major consequences of these issues. Some related works explore the influence of process variability and single event transients (SET) on the circuits based on FinFET technologies, but there is a lack of approaches to mitigate the effects caused by them. For these reasons, from a design standpoint, considerable efforts should be made to understand and reduce the impacts introduced by reliability challenges. In this regard, the main contributions of this Ph.D. thesis are: 1) to investigate the behavior of FinFET logic cells under process variations and radiation effects; 2) to evaluate four circuit-level approaches to attenuate the impact caused by work-function fluctuations (WFF) and soft errors (SE); 3) to provide an overall comparison between all techniques applied in this work; 4) to trace a trade-off between the gains and penalties of each approach regarding performance, power, area, and SET cross-section. Transistor reordering, decoupling cells, Schmitt Trigger, and sleep transistor are the four circuit-level mitigation techniques explored in this work. The potential of each one to make the logic cells more robust to the process variability and radiation-induced soft errors are assessed comparing the standard version results with the design using each approach. This Ph.D. thesis also establishes the mitigation tendency when different levels of variation, transistor sizing, and radiation particles characteristics such as linear energy transfer (LET) are applied in the design with these techniques. The process variability is evaluated through Monte Carlo (MC) simulations with the WFF modeled as a Gaussian function using SPICE simulations. The SE susceptibility is estimated using the radiation event generator tool MUSCA SEP3 (developed at ONERA), also based on an MC method, which deals both with radiation environment characteristics, layout features and the electrical properties of devices. In general, the proposed approaches improve the state-of-the-art by providing circuit-level options to reduce the process variability effects and SE susceptibility, at fewer penalties and design complexity. The transistor reordering technique can increase the



robustness of logic cells under process variations up to 8%, but this method is not favorable for SE mitigation. The insertion of decoupling cells shows interesting outcomes for power variability control with levels of variation above 4%, and it can attenuate until 10% the delay variability considering manufacturing process with 3% of WFF. Depending on the LET, the design with decoupling cells can decrease until 10% of SE susceptibility of logic cells. The use of Schmitt Triggers in the output of FinFET cells can improve the variability sensitivity by up to 50%. The sleep transistor approach improves the power variability reaching around 12% for WFF of 5%, but the advantages of this method to delay variability depends how the transistors are arranged with the sleep transistor in the pull-down network. The addition of a sleep transistor become all logic cells studied free of faults even at the near-threshold regime. In this way, the best approach to mitigate the process variability is the use of Schmitt Triggers, as well as the sleep transistor technique, is the most efficient for the SE mitigation. However, the Schmitt Trigger technique presents the highest penalties in area, performance, and power. Therefore, depending on the application, the sleep transistor or decoupling cells technique can be the most appropriate to mitigate the process variability effects.

# Resumo

---

A variabilidade de processo e a resistência a radiação são requisitos de confiabilidade relevantes à medida que a fabricação de *chips* avança mais a fundo no regime nanométrico. A perda de rendimento paramétrico e as falhas críticas no comportamento do sistema são as principais consequências destes problemas. Alguns trabalhos relacionados exploram a influência da variabilidade de processo e dos eventos transientes únicos (SET) nos circuitos projetados nas tecnologias FinFET, mas existe uma ausência de abordagens para mitigar eles. Por estas razões, do ponto de vista de projeto, esforços consideráveis devem ser feitos para entender e reduzir os impactos introduzidos pelos desafios de confiabilidade. Dessa forma, as principais contribuições desta tese de doutorado são: 1) investigar o comportamento de células lógicas FinFET sob variações de processo e efeitos de radiação; 2) avaliar quatro abordagens em nível de circuito para atenuar o impacto causado por flutuações na função trabalho (WFF) and *soft errors* (SE); 3) fornecer uma comparação global entre todas as técnicas aplicadas neste trabalho; 4) Traçar um balanceamento entre os ganhos e as penalidades de cada abordagem em relação ao desempenho, potência, área, seção transversal SET e largura de pulso SET. Reordenamento de transistores, e o uso de *decoupling cells*, *Schmitt Triggers* e *sleep transistors* são as quatro técnicas de mitigação em nível de circuito exploradas neste trabalho. O potencial de cada uma delas para tornar as células lógicas mais robustas à variabilidade de processo e aos *soft errors* induzidos pela radiação são avaliados comparando os resultados da versão padrão com o projeto usando cada uma das técnicas. Esta tese também estabelece a tendência de mitigação quando diferentes níveis de variação, dimensionamento de transistores e características das partículas de radiação, tais como a transferência linear de energia (LET), são aplicados no projeto com estas técnicas. A variabilidade de processo é avaliada através de simulações Monte Carlo (MC) com a WFF modelada como uma função Gaussiana usando simulações SPICE enquanto a susceptibilidade à SE é estimada usando a ferramenta gerado de eventos de radiação MUSCA SEP3 (desenvolvida na ONERA) também baseada em um método MC que lida com as características do ambiente de radiação, os recursos de leiaute e as

propriedades elétricas dos dispositivos. De modo geral, as técnicas propostas melhoram o estado da arte, fornecendo opções à nível de circuito para reduzir os efeitos da variabilidade de processo e a susceptibilidade à SE, com menos penalidades e complexidade de projeto. A técnica de reordenamento de transistores pode aumentar a robustez das células lógicas sob variação de processo até 8%, mas este método não é favorável para a mitigação de SE. A inserção de *decoupling cells* mostra resultados interessantes para o controle da variabilidade de potência com níveis de variação acima de 4%, e esta técnica pode atenuar até 10% a variabilidade de atraso considerando um processo de manufatura com 3% de WFF. Dependendo do LET, o projeto com *decoupling cells* pode diminuir até 10% a susceptibilidade à SE das células lógicas. O uso de *Schmitt Triggers* na saída das células FinFET podem melhorar a sensibilidade à variabilidade até 50%. A abordagem com *sleep transistors* melhora a variabilidade de potência em torno de 12% para 5% de WFF, mas as vantagens desse método para o atraso dependem de como os transistores estão posicionados em relação ao *sleep transistor* na rede *pull-down*. A adição de um *sleep transistor* torna todas as células lógicas estudadas livre de falhas mesmo no regime quase limiar. Neste contexto, a melhor abordagem para mitigar a variabilidade de processo é o uso de *Schmitt Triggers*, bem como a técnica de *sleep transistor* é a mais eficiente para a mitigação de SE. No entanto, a técnica de *Schmitt Triggers* apresenta as maiores penalidades de área, desempenho e potência. Sendo assim, dependendo da aplicação, a técnica de *sleep transistors* pode ser a mais apropriada para mitigar os efeitos da variabilidade de processo.

# Résumé

---

## 1. INTRODUCTION GENERALE

De nouveaux matériaux et de nouvelles architectures de dispositifs ont dû être mis en œuvre dans les circuits intégrés pour assurer la mise à l'échelle de la technologie (PRADHAN; SAHU; RANJAN, 2016). L'adoption des appareils FinFET présentait plusieurs avantages, en maintenant le rythme des performances, en réduisant la consommation d'énergie et en augmentant la densité. Cependant, les petits motifs géométriques imposés par les nœuds technologiques avancés soulèvent des questions essentielles liées à la fiabilité des systèmes électroniques. L'utilisation de technologies inférieures à 22nm entraîne une complexité de conception accrue avec davantage de sources potentielles de variabilité ainsi qu'une densité plus élevée permettant à une seule particule énergétique d'affecter plusieurs nœuds adjacents (ENDO et al., 2009) (BHUVA et al., 2015).

La variation de fabrication représente un écart aléatoire par rapport aux spécifications de conception typiques, qui stimule la dégradation du circuit, la consommation électrique anormale et la divergence des performances (TASSIS et al., 2014). Les principales sources de variations de processus sont la longueur d'onde adoptée dans l'étape de la lithographie, qui ne suit pas le rythme de la mise à l'échelle du dispositif et l'utilisation de diélectriques à  $k$  élevé pour améliorer le contrôle de grille sur la région du canal. Bien que l'utilisation de métal comme matériau de grille soit utile pour contrôler certains défis, elle modifie les orientations du grain en générant différentes fonctions de travail alignées de manière aléatoire, ce qui implique des fluctuations plus élevées de la fonction de travail (DADGOUR et al., 2010).

Le *soft error* (SE) provient de l'interaction de particules énergétiques provenant de l'espace et de radiations terrestres avec le silicium. En général, les technologies nanométriques plus approfondies sont plus sensibles à la SE en raison de tensions d'alimentation faibles, de capacités intrinsèques réduites et d'un fonctionnement à fréquence plus élevée (BAUMANN, 2005). Cependant, la structure 3D de FinFET minimise le volume de silicium exposé au mécanisme de collecte de charge et, par conséquent, diminue la susceptibilité du SE sur ces dispositifs (SEIFERT et al., 2015). Cependant, les effets ne peuvent pas encore être considérés comme négligeables car la variabilité de fabrication peut modifier le seuil de transfert d'énergie linéaire (LET) pour induire un *soft error*.

## MOTIVATION

La réduction de la variabilité des processus et la dureté du rayonnement sont des exigences de fiabilité pertinentes alors que la fabrication de puces progresse plus en profondeur dans le

régime nanométrique. Les circuits intégrés à variabilité de fabrication peuvent ne pas satisfaire à certains critères de performance ou de consommation électrique, ce qui augmente la perte de rendement paramétrique et la nécessité de plusieurs étapes de la refonte. Les erreurs logicielles induites par les radiations peuvent provoquer une perte temporaire de données, entraînant des défaillances critiques du comportement du système, même au niveau du sol. La feuille de route des industries des semi-conducteurs les plus renommées souligne encore l'utilisation de dispositifs FinFET pour la prochaine génération de nanotechnologies. En outre, un kit prédictif de conception de processus (PDK) FinFET 7-nm est devenu disponible pour une utilisation académique, ce qui permet une recherche approfondie au niveau de la structure (CLARK et al., 2016). Du point de vue de la conception, ces défis nécessitent des estimations précises du comportement du circuit, en soulignant l'importance d'indiquer de nouvelles directives de conception capables de gérer ces controverses tout en préservant l'avancée technologique.

Plusieurs travaux ont étudié l'impact de la variabilité des processus et des effets du rayonnement sur les technologies FinFET, principalement au niveau des dispositifs et de l'électricité, mais beaucoup moins de connaissances ont été acquises au niveau de la disposition. De plus, seuls quelques travaux ont proposé des solutions pour atténuer les effets causés par celles-ci. Les approches les plus efficaces dans la littérature pour atténuer les variations de processus et les défauts transitoires sont généralement liées à l'utilisation d'une structure et d'un matériau différents au cours du processus de fabrication, ou de la réplification matérielle, respectivement. Cependant, les modifications de fabrication ont un coût élevé et une complexité de conception accrue, ainsi que la redondance matérielle, entraînent des frais généraux importants.

## **OBJECTIFS DE THESE**

Les techniques d'atténuation au niveau du circuit qui modifient la conception des cellules logiques au niveau de la disposition constituent des alternatives potentielles pour parvenir à des solutions plus robustes et plus précises, avec un coût de mise en œuvre moins élevé et moins de pénalités. De cette manière, les objectifs principaux de cette thèse sont :

1. étudier le comportement des cellules logiques FinFET sous les variations de processus et les effets de rayonnement ;
2. Évaluer quatre approches au niveau du circuit pour atténuer l'impact causé par les fluctuations du travail et les erreurs logicielles.
3. Fournir une comparaison globale entre toutes les techniques appliquées dans ce travail ;
4. Tracez un compromis entre les gains et les pénalités de chaque approche concernant la surface, les performances, la consommation d'énergie, la durée d'impulsion SET et la section transversale SET.

Les quatre approches d'atténuation au niveau du circuit explorées dans ce travail sont le *transistor reordering*, *decoupling cells*, *Schmitt Trigger* et *sleep transistor*. Le *transistor reordering* est basée sur l'optimisation des dispositions des transistors. L'utilisation de *decoupling cells* est une méthode capacitive. Schmitt Trigger agit en tant que mécanisme de retour afin de minimiser la dégradation de la sortie. Le *sleep transistor* est une stratégie de *power-gating*. Tout d'abord, la version standard des cellules logiques FinFET, c'est-à-dire sans aucune technique au niveau du circuit, a été mise en œuvre dans des scénarios de variabilité de fabrication et de rayonnement à des fins de comparaison. Ensuite, le potentiel de chaque approche pour rendre les cellules logiques FinFET plus robustes aux fluctuations de la fonction de travail et aux erreurs logicielles est évalué en comparant la version standard à la conception adoptant chaque technique selon des métriques prédéfinies bien connues.

Ce travail établit également la tendance à l'atténuation lorsque différents niveaux de variation de processus, de dimensionnement de transistor et de caractéristiques de particule de rayonnement, tels que le LET, sont appliqués dans la conception utilisant ces techniques. Cette thèse contribue à l'avancement de l'état de la technique en fournissant des options au niveau du circuit pour atténuer la variabilité des processus et la susceptibilité aux *soft errors* dans une technologie FinFET avec moins d'inconvénients techniques et une mise en œuvre plus simple, si on la compare aux autres approches disponibles dans la littérature. De plus, l'ensemble des informations fournies dans ce travail aide les concepteurs à choisir le schéma de présentation le plus approprié pour une application donnée, en connaissant tous les avantages et les inconvénients de son adoption.

## **2. FONDEMENT THEORIQUE**

Ce chapitre présente les concepts fondamentaux liés aux technologies FinFET, tels que la structure, le mode de fonctionnement et les propriétés des transistors FinFET, une analyse de l'évolution technologique dans l'industrie des semi-conducteurs ainsi que des informations sur le schéma de configuration, les modèles prédictifs et les kits de conception de processus.

Le dispositif FinFET se compose d'ailettes de silicium verticales pour former la région de canal et pour connecter les régions de source et de drain à chaque extrémité. Ces ailettes verticales enveloppent la région de la porte et des canaux MOS sont formés sur les deux parois latérales et sur le dessus de l'aileron. Les principaux paramètres géométriques d'un FinFET selon la figure 1 sont la longueur de la porte ( $L_G$ ), la hauteur de l'ailette ( $H_{FIN}$ ), l'épaisseur de l'aile ( $T_{SI}/T_{FIN}/W_{FIN}$ ) et l'épaisseur de l'oxyde ( $T_{OX}$ ). Les structures à porte courte (SG) et à porte indépendante (IG) sont les deux principaux types de dispositifs FinFET. Ce travail adopte le modèle SG dans un substrat en vrac tel que la porte arrière et la porte avant soient liées ensemble, physiquement court-circuitées. Dans ce mode, les deux portes fournissent une commande de porte maximale assurant le contrôle électrostatique du canal. Cependant, le

courant à l'arrêt est plus élevé car il n'est pas possible de réguler la tension de seuil de l'appareil ( $V_{TH}$ ) électriquement.

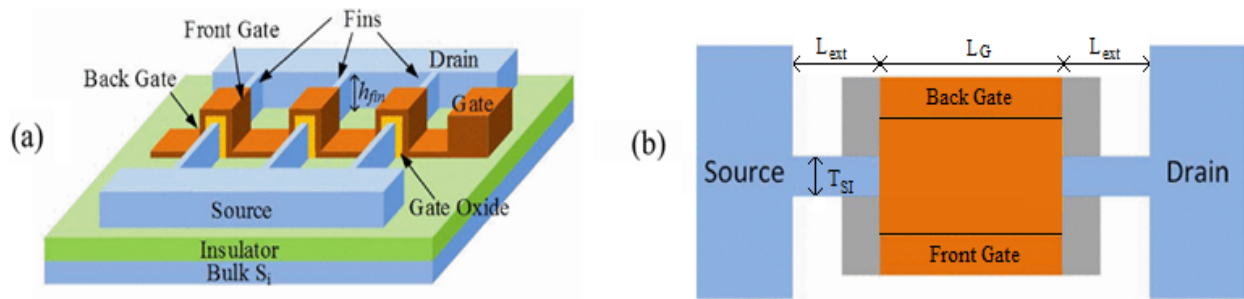


Figure 1 : Structure SG FinFET dans (a) une vue en perspective et (b) une vue de dessus (GUPTA; ROY, 2013)

Le prix élevé des équipements de recherche, de développement et de fabrication a entraîné une réduction du nombre d'industries de semi-conducteurs qui investissent dans des nœuds technologiques avancés. De nos jours, la course aux puces plus compactes et technologiques se produit principalement parmi les sociétés Intel, Samsung et TSMC (HIBBEN, 2018).

La conception FinFET est composée de rangées d'ailettes reliant les régions de source et de drain, avec des barrettes de grille orthogonales. Les portes simples violent généralement les règles de conception des technologies FinFET. Ainsi, la conception d'un seul FinFET comporte trois portes car chaque transistor doit être terminé avec des portes factices de chaque côté. De plus, il n'est pas possible de couper la diffusion en terminant simplement le polygone comme dans les dispositifs plans.

Actuellement, le modèle de technologie FinFET le plus précis pour les simulations SPICE est le PTM-MG développé par ASU (SINHA et al., 2012) (PTM, 2018). D'autre part, le PDK ASAP7 développé par ASU en partenariat avec ARM Ltd se démarque car il admet des conjectures de conception réalistes concernant l'étape de lithographie et les compétences technologiques actuelles (CLARK et al., 2016).

### 3. DEFIS TECHNOLOGIQUES FINFET

Ce chapitre présente un aperçu général des problèmes rencontrés dans les appareils FinFET. De plus, il présente en détail les deux défis de fiabilité évalués dans ce travail : la variabilité de fabrication et les erreurs logicielles induites par le rayonnement. La dernière sous-section de ce chapitre décrit les quatre techniques d'atténuation au niveau du circuit étudiées et comment chacune d'elles a été mise en œuvre.

## VARIABILITE DE FABRICATION

Les technologies FinFET sont plus susceptibles de subir des variations de processus telles que la rugosité de bord de ligne (LER) et la granularité de grille métallique (MGG). La variabilité de fabrication représente une déviation aléatoire qui modifie la structure du transistor et, par conséquent, modifie les propriétés électriques d'un circuit. De cette manière, les spécifications de conception typiques subissent des modifications stimulant la dégradation du circuit, une consommation électrique anormale et une divergence de performances, augmentant la perte de rendement paramétrique. Généralement, l'étape de lithographie au cours du processus de fabrication utilise une lumière ultraviolette pour transférer les motifs géométriques sur les tranches minces de silicium. Les technologies FinFET ont essayé d'adopter une technologie ultraviolette extrême (EUV) pour toutes les couches afin de fournir des conceptions simples et rentables. Cependant, la longueur d'onde n'a pas suivi le rythme de la mise à l'échelle du dispositif et de multiples approches de modélisation doivent être adoptées (RIEGER, 2012). Tous ces facteurs contribuent au LER, ce qui signifie une déviation des bords du transistor par rapport à la forme attendue.

Les imperfections de la région de la porte sont classées comme rugosité du bord de la porte (GER), tandis que les variations de la surface des ailettes sont appelées rugosités du bord de la fin (FER), comme le montre la Figure 2. Le MGG a pris de l'importance depuis l'adoption des diélectriques à améliorer le contrôle de porte sur la région de canal dans les technologies inférieures à 45 nm. La différence d'énergie entre le niveau de vide et le niveau de Fermi d'un solide s'appelle la fonction de travail (WF). L'orientation du grain de la porte en métal provoque une déviation de la fonction de travail de la porte. Dans le processus de fabrication, les dispositifs à grille en métal sont généralement fabriqués en utilisant des métaux avec différentes fonctions de travail ( $\phi_m$ ) alignées de manière aléatoire, ce qui implique des fluctuations de fonction de travail plus élevées (WFF) (DADGOUR; DE; BANERJEE, 2008). Des recherches antérieures indiquent que la fluctuation des fonctions de travail est la principale source de variabilité des dispositifs FinFET (MEINHARDT; ZIMPECK; REIS, 2014b).



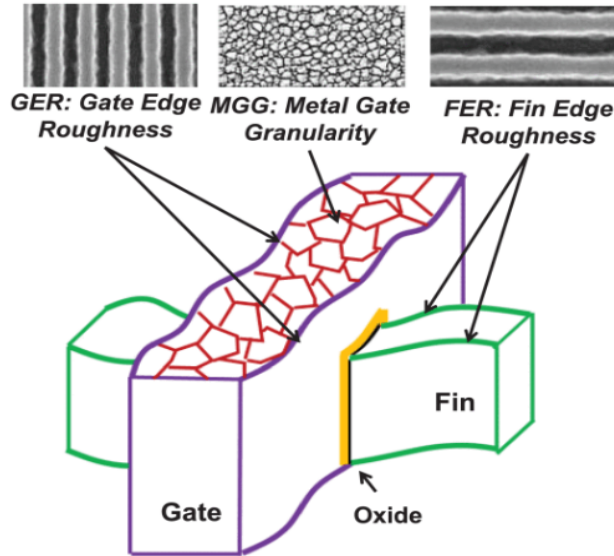


Figure 2 : Principales sources de variation aléatoire dans le FinFET: GER, MGG, and FER (JIANG et al., 2016)

## EFFETS DE RAYONNEMENT NATUREL

Une autre préoccupation liée à la fiabilité des nœuds technologiques avancés est la susceptibilité aux environnements de rayonnement naturel. Initialement, les effets des radiations dans les systèmes électroniques n'étaient considérés comme pertinents que dans les cas de conception militaire, avionique ou spatiale. Néanmoins, avec l'avancement de la microélectronique, des défauts induits par les radiations peuvent se produire même au niveau de la mer (DODD et al., 2010). Au cours de l'ère de la CMOS, la dose ionisante totale (TID) était la principale source de défauts de radiation entraînant des dommages fonctionnels permanents et irréversibles. À mesure que la technologie évoluait, les événements transitoires à événement unique (SEE) gagnaient en importance et devenaient de plus en plus importants pour les systèmes électroniques aux niveaux spatial et terrestre. SEE se produit en raison de l'interaction de particules énergétiques avec le silicium (tels que neutrons, électrons, protons, particules alpha et ions lourds) dans les drains sensibles des transistors, provenant de rayonnements spatiaux et terrestres. La charge déposée par une seule particule ionisante peut produire une déviation temporaire sur un court intervalle de temps qui peut altérer ou non le comportement du système. Les effets non destructifs les plus connus sont les événements uniques (SEU) et les événements transitoires (SET). Le SEU se produit lorsqu'une particule énergétique frappe un circuit séquentiel, tel qu'un verrou ou une bascule, en modifiant le bit stocké. Sinon, le SET se produit lorsque la particule rencontre un circuit combinatoire, tel que des portes de base ou des additionneurs complets, générant une impulsion transitoire, qui peut ou non être capturée par un élément de mémoire.

En général, les technologies nanométriques diminuent la charge minimale requise pour induire un SET en raison de faibles tensions d'alimentation et de capacités intrinsèques réduites (SEIFERT et al., 2015). Le fonctionnement en fréquence supérieure augmente également la probabilité qu'un élément de mémoire verrouillant un SET généré dans la logique combinatoire ainsi que le phénomène de partage de charge deviennent plus fréquents dans les circuits intégrés à densité supérieure. Cependant, la nature perturbatrice des FinFET minimise le volume de silicium exposé au mécanisme de collecte de charge, comme illustré à la figure 3, ce qui diminue la susceptibilité aux soft errors sur ces dispositifs. La controverse est la variabilité de fabrication qui peut changer le transfert d'énergie linéaire (LET) pour induire un soft error. De cette manière, même si la structure 3D des dispositifs FinFET est moins sensible aux erreurs logiques, les autres problèmes de fiabilité ne permettent pas que les effets du rayonnement puissent être négligeables.

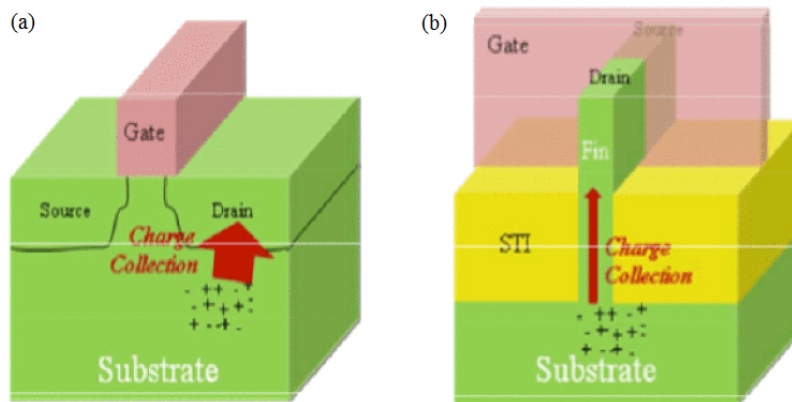


Figure 3: Mécanisme de collecte de charges dans des dispositifs (a) plans et (b) FinFET (LEE et al., 2015)

## APPROCHES DES DURCISSEMENT AU NIVEAU DU CIRCUIT

Plusieurs techniques peuvent être appliquées à différents niveaux d'abstraction pour améliorer la fiabilité des circuits intégrés. Habituellement, des techniques d'atténuation basées sur l'utilisation de différents dispositifs, matériaux ou profils de dopage estiment votre efficacité à l'aide de simulations TCAD. Bien que ce niveau d'abstraction présente des résultats très précis, il nécessite un temps de calcul plus long pour les conceptions VLSI. Une solution consiste donc à étudier des approches au niveau du circuit qui modifient la conception des cellules logiques afin d'obtenir des solutions plus robustes. Les ajustements de conception peuvent être liés à l'insertion de composants ou d'éléments de filtrage, à l'exploration de différents arrangements de transistors, à l'optimisation de grille, au repliement de transistors, à la redondance matérielle, à l'augmentation de la capacité des nœuds les plus sensibles et à l'utilisation de la conception à plusieurs niveaux cellules complexes. Les quatre approches

d'atténuation au niveau du circuit explorées dans ce travail sont le *transistor reordering*, *decoupling cells*, *Schmitt Trigger* et *sleep transistor*.

## TRANSISTOR REORDERING

L'optimisation de la disposition des transistors est une méthode généralement utilisée pour concevoir des circuits plus rapides, pour réduire les courants de fuite ou pour traiter les effets d'instabilité de la température de polarisation (BTI); (SILVA; REIS; RIBAS, 2009) (BUTZEN et al., 2010) ( CHUN; CHEN, 2016). Le principe de cette technique est de modifier les agencements de transistors en conservant la même fonction logique pour toutes les topologies. Les possibilités peuvent être obtenues en utilisant différents styles logiques tels que CMOS complémentaires, logique pondérée et logique passe-transistor, ou par *transistor reordering*. La réorganisation du transistor modifie les caractéristiques électriques et physiques des cellules logiques et, par conséquent, la susceptibilité à la variation de fabrication et aux erreurs logiques est également modifiée.

La figure 4 montre deux topologies alternatives pour la cellule AOI21 qui sont logiquement équivalentes. Dans le réseau de réception, le transistor série (signal d'entrée A) peut être placé à proximité ou à distance de la sortie de la cellule. Certaines portes logiques, telles que AOI221 et OAI221, peuvent également explorer un emplacement intermédiaire entre les associations parallèles pour placer le transistor en série. La topologie de fermeture est définie comme la version standard de ce travail car elle est la plus utilisée dans les bibliothèques de cellules standard. Lorsque les transistors du réseau complémentaire n'ont qu'une association parallèle, le réarrangement n'est pas nécessaire car il n'influence pas les résultats tels que la consommation d'énergie et les performances. L'absence de pénalité de surface est le principal avantage de cette technique.

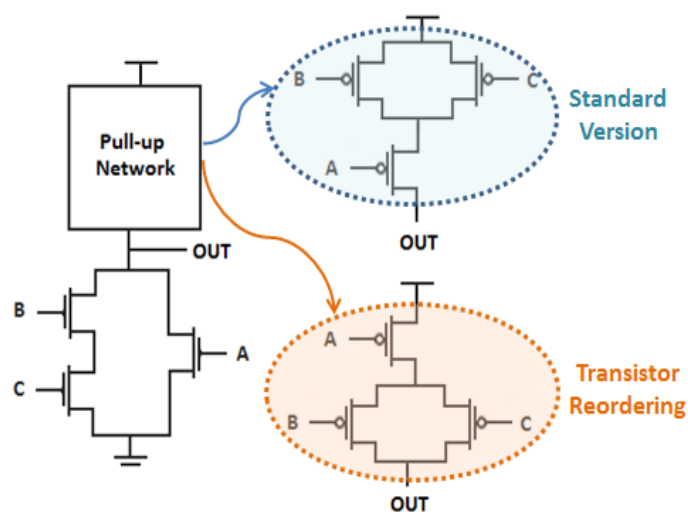


Figure 4 : Version standard de la cellule logique AOI21 et avec le transistor reordering

## DECOUPLING CELLS

L'ajout de cellules de découplage est une méthode capacitive couramment utilisée dans plusieurs conceptions industrielles pour assurer une plus grande immunité au bruit sur les rails d'alimentation et les lignes de signaux (EVANS et al., 2002) (SU et al., 2003). Les *decoupling cells* sont connectées à la sortie de grille et sont composées de deux transistors agencés en mode de couplage croisé, comme illustré à la figure 5 pour la cellule AOI21. Ces cellules augmentent la capacité totale dans le noeud de sortie, augmentant la charge critique pour produire une impulsion SET et rendant ce noeud moins sensible à l'impact des particules énergétiques. Dans (ANDJELKOVIC et al., 2018), cette technique a été utilisée pour filtrer les impulsions SET générées par des particules de basse énergie dans un ensemble de portes logiques conçues à l'aide de la bibliothèque numérique CMOS en masse de l'IHP de 130 nm avec l'injection de défaut via le double courant exponentiel au niveau de SPICE.

De plus, les *decoupling cells* fournissent du courant aux portes lors de la commutation, protégeant les circuits des perturbations causées par les variations de processus. Pour obtenir de meilleurs résultats en ce qui concerne l'atténuation, il est recommandé d'utiliser deux cellules de découplage de telle sorte qu'une cellule soit connectée entre la sortie et le rail d'alimentation, tandis que l'autre est placée entre le rail de sortie et le sol. Comme l'insertion de *decoupling cells* est une méthode capacitive, les cellules de découplage plus grandes contribuent encore plus à l'atténuation de la variabilité de fabrication et des *soft errors* induites par le rayonnement. L'inconvénient est la superficie et les frais généraux de consommation d'énergie dus à l'ajout de quatre transistors supplémentaires dans la conception.

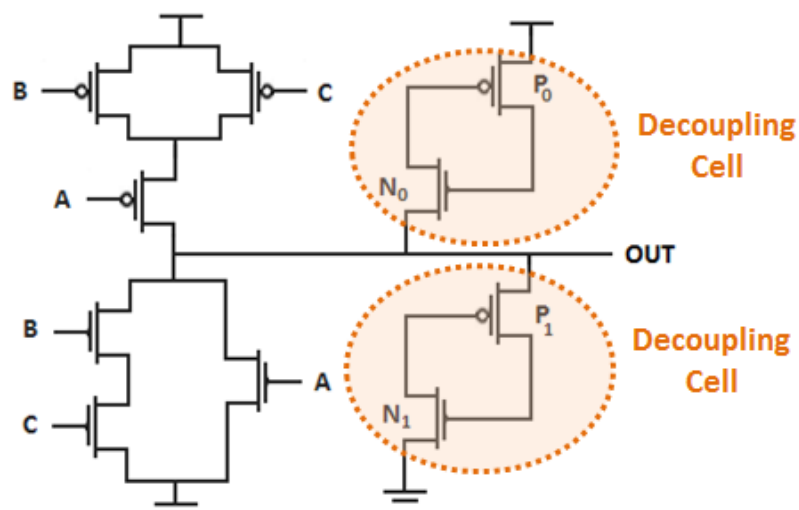


Figure 5 : Conception de la cellule logique AOI21 reliant les decoupling cells en sorti

## SCHMITT TRIGGER

Les *Schmitt Triggers* ont une propriété d'hystérésis inhérente couramment utilisée pour améliorer la stabilité du signal et une immunité élevée au bruit. Ce travail explore une topologie bien connue de *Schmitt Trigger* où la principale différence par rapport aux versions les plus courantes est la présence de dispositifs  $P_F$  et  $N_F$  qui sont responsables d'un système de rétroaction, comme le montre la figure 6 (LOTZE; MANOLI, 2017). Par exemple, si la sortie est à un niveau haut, le transistor  $N_F$  est activé, entraînant le noeud X à un potentiel élevé, forçant la tension drain-source du transistor  $N_1$  presque nulle et sa tension grille-source dans la région négative. Ce type de topologie réduit le courant de fuite dans  $N_1$  de façon exponentielle, en augmentant le rapport de courant  $I_{ON}/I_{OFF}$  et en minimisant la dégradation de la sortie.

Le principal effet de la variabilité de fabrication est un décalage de la courbe de transfert de tension (VTC) dû à la variation de la tension de seuil. L'impact de variabilité sur le VTC est réduit dans le déclencheur de Schmitt en raison de la forte influence de la tension grille-source des transistors internes ( $N_1$  et  $P_1$ ) sur son point de commutation. Le remplacement des onduleurs traditionnels par Schmitt Triggers sur des additionneurs complets s'avère être une alternative attrayante pour atténuer les effets des variations de fabrication sur les technologies planaires (DOKANIA; ISLAM, 2015) (TOLEDO et al., 2018) ainsi que pour une technologie FinFET (MORAES et al., 2018). L'inconvénient principal de cette technique est également la surcharge en surface et en puissance due à l'ajout de six transistors supplémentaires dans le circuit.

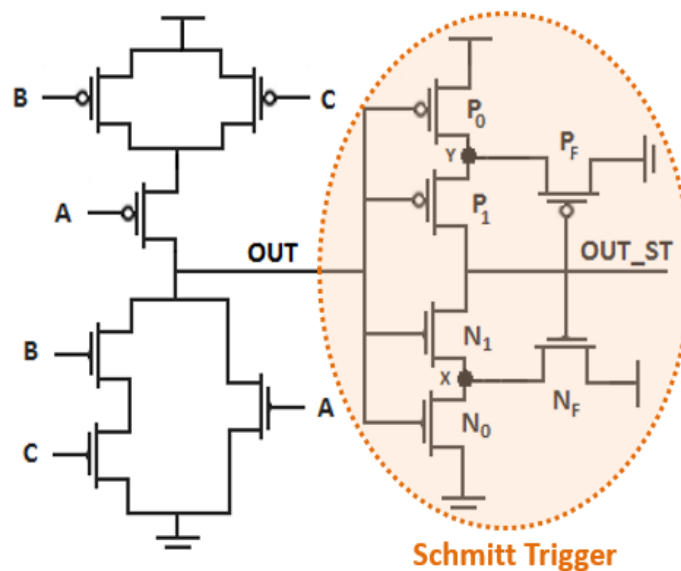


Figure 6 : Conception de la cellule logique AOI21 reliant un Schmitt Trigger à la sortie

## SLEEP TRANSISTOR

Le *power-gating* est une stratégie largement utilisée dans les conceptions de faible puissance pour couper les blocs de circuit qui ne sont pas utilisés, améliorant ainsi la puissance globale d'une puce (CALIMERA et al., 2015). La différence entre les conceptions à commande de puissance réside dans la granularité des blocs. Ce travail se concentre sur un modèle à grain fin dans lequel un *sleep transistor* est ajouté à chaque cellule. Cependant, pour les circuits plus importants, le style à blocs est plus indiqué pour éviter la surcharge. La figure 7 illustre la cellule AOI21 avec un *sleep transistor* placé entre le réseau de tirage et le rail de masse. Le signal de veille permet de contrôler les états "actif" (veille = 0) et "inactif" (veille = 1) du transistor.

Lorsque le transistor de veille est en mode actif, il garantit une connexion typique de la cellule logique au rail de masse, agissant en tant que régulateur de tension d'alimentation. En mode veille, le transistor de veille est désactivé, déconnectant ainsi la terre virtuelle ( $V_{GND}$ ) de la terre physique. Ce comportement vise à réduire les courants de fuite, les défauts transitoires et les effets BTI. De plus, l'ajout de transistors de sommeil s'est avéré très efficace pour atténuer l'impact des variations de processus dans les technologies planaires (REIS; CAO; WIRTH, 2015). Cependant, pour appliquer avec succès la technique du transistor veille, il faut considérer deux points fondamentaux: 1) le contrôle correct du signal de veille; et 2) l'adoption d'un dimensionnement approprié. Le principal inconvénient de cette technique est la dégradation des performances lorsque le transistor de veille est en mode actif, ce qui en fait le retard dans le pire des cas pour les cellules logiques.

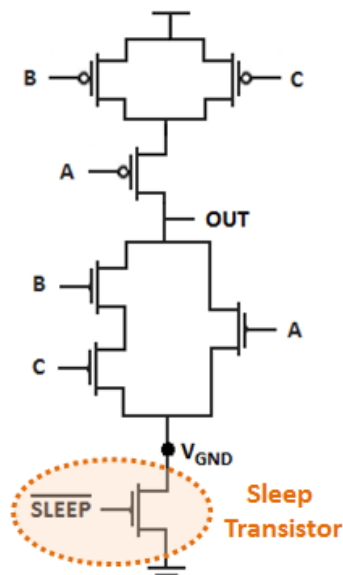


Figure 7 : Conception de la cellule logique AOI21 utilisant un sleep transistor

## 4. METHODOLOGIE D'ÉVALUATION

Ce chapitre explique la méthodologie utilisée dans ce travail depuis la conception de FinFET jusqu'à l'évaluation de la variabilité de fabrication et de la susceptibilité aux radiations. Il présente également le comportement typique des cellules logiques FinFET à des fins de comparaison, c'est-à-dire sans appliquer d'approche au niveau du circuit pour atténuer les effets des variations de WF et des *soft errors*. Premièrement, le flux de conception a été effectué en tenant compte de la version standard des cellules à des fins de comparaison, puis le schéma de chaque cellule a été modifié à l'aide des approches au niveau du circuit décrites dans la section 3.3 afin d'obtenir des circuits plus fiables.

Les cellules logiques passent par trois étapes élémentaires : conception physique, flux de vérification et extraction parasite. Dans la conception physique, le schéma, la présentation et le symbole de toutes les cellules logiques ont été implémentés à l'aide de l'outil Virtuoso de Cadence. Ensuite, chaque mise en page a été soumise au flux de vérification composé des étapes de vérification des règles de conception (DRC) et de mise en forme par rapport au schéma (LVS).

Dans ce travail, les étapes DRC et LVS sont basées sur les règles technologiques du PDK FinFET à 7 nm appelé ASAP7 développé par ASU en collaboration avec ARM Ltd (CLARK et al., 2016). Ce PDK implémente le modèle à porte courte, dans lequel une cellule TAP est utilisée pour connecter la porte arrière à la porte avant, garantissant ainsi le bon fonctionnement des transistors. Enfin, les résistances et capacités parasites (RC) des fils sont extraites de la structure. Une nouvelle liste de circuits est générée de telle sorte que chaque réseau possède un sous-système avec l'arborescence RC et les connexions entre les réseaux parasites. Les outils Calibre de Mentor, ainsi que Virtuoso, ont été utilisés pour exécuter les étapes de flux de vérification et d'extraction parasite. Le flux de données géométriques (GDS) est un fichier généré par l'outil Virtuoso qui représente toutes les formes géométriques de la présentation au format binaire. Ce fichier peut être utilisé pour reconstruire tout ou partie d'une mise en page, pour transférer la mise en page entre différents outils ou pour créer des photomasques pour le processus de fabrication.

### ÉVALUATION DE LA VARIABILITE DE FABRICATION

Cette thèse considère deux simulations MC effectuées dans SPECTRE à partir de Cadence pour estimer le comportement des cellules logiques FinFET sous des variations de fabrication (ALIOTO; CONSOLI; PALUMBO, 2015). Comme la fonction de travail (WF) est le paramètre le plus impacté par la variabilité de fabrication dans les technologies FinFET, la WF est modélisée comme une fonction gaussienne, en supposant un écart de 3-sigma ( $\sigma$ ). Toutes les cellules logiques ont été évaluées en utilisant des niveaux de WFF variant de 1% à 5% en raison du manque d'informations de l'industrie sur les niveaux de WFF dans les technologies FinFET

actuelles. Ces variations ont été adoptées en tant que référence aux valeurs nominales du modèle de tension de seuil régulière (RVT) de ASAP7.

La base de données sur la variabilité fournit un résumé des résultats statistiques des simulations MC, telles que les valeurs minimale (minimale) et maximale (maximale), la moyenne ( $\mu$ ) et l'écart type ( $\sigma$ ) pour tous les arcs de synchronisation ainsi que pour la consommation d'énergie. Malgré les données fournies par la base de données de variabilité pour les mesures de délai et de puissance, ce travail a également retenu deux valeurs de mérite pour permettre une comparaison plus détaillée: 1) l'écart type normalisé ( $\sigma/\mu$ ) pour indiquer la sensibilité des cellules logiques au WF les fluctuations; et 2) la relation delta ( $\Delta$ ) pour spécifier l'ampleur du changement de sensibilité aux variations de processus lorsque les cellules logiques sont conçues en utilisant une approche d'atténuation au niveau du circuit au lieu de la version standard.

### **ESTIMATION DES *SOFT ERRORS***

La susceptibilité aux erreurs logiques des cellules logiques FinFET a été estimée à l'aide de l'outil MUSCA SEP3 développé par l'ONERA, le laboratoire aérospatial français (HUBERT et al., 2009) (ARTOLA et al., 2013). MUSCA SEP3 est un outil générateur d'événements de rayonnement, basé également sur la méthode de Monte Carlo, qui modélise toutes les étapes depuis l'introduction d'une particule énergétique dans la matière jusqu'à la manifestation d'une impulsion transitoire sur les circuits. Les particules de rayonnement disponibles pour l'analyse sont les neutrons, les protons, les ions lourds, les muons et les particules alpha. Cet outil prend en compte l'environnement de rayonnement ciblé (espace, avionique, sol), les caractéristiques de rayonnement (LET, angle d'incidence, type de particule énergétique), les mécanismes de transport dynamique et de collecte de charges, la tension de polarisation, les caractéristiques de tracé, le circuit électrique réponse, l'oxyde de STI et les détails du processus de fabrication

Les frais de collecte de chaque transistor sont calculés en fonction de la structure de l'appareil, qui peut être extraite à partir d'une ingénierie inverse ou à l'aide du rapport FEOL du fichier GDSII. Le transport de modélisation et la collecte des porteurs libres dans le silicium sont effectués à l'aide de modèles analytiques 3D, via les informations BEOL, qui adoptent les mécanismes suivants: diffusion ambipolaire, collecte dynamique, amplification bipolaire à collections multiples pour évaluer le partage de charge et le phénomène d'extinction d'impulsion, recombinaison et dépendance de biais. L'impact de la température (jusqu'à 50K) est pris en compte pour tous les modèles physiques et électriques utilisés pour le transport et la collecte de charge dans les semi-conducteurs. Le modèle mis en œuvre pour l'amplification bipolaire dépend de deux aspects. Premièrement, le modèle utilise les résistances d'accès équivalentes du dispositif multi-états pour déterminer le déclenchement du transistor



bipolaire. En outre, le modèle considère la variabilité de l'amplification de la collecte de charges en fonction de la technologie LET due aux technologies FinFET.

La base de données SET générée par l'outil est très précise car elle prend en compte toutes les caractéristiques présentées ci-dessus. Une nouvelle base de données SET est créée pour chaque configuration différente. Une fois cela fait, il est composé d'un ensemble de sources de courant à injecter dans les noeuds sensibles, c'est-à-dire le drain des transistors. L'injection de faute est effectuée automatiquement à l'aide d'un script associé à SPECTRE de Cadence. Après, les résultats sont évalués pour déterminer la susceptibilité de *soft error* des circuits.

Ce travail explore l'irradiation par des ions lourds sous un angle d'incidence normal, à la température ambiante (27°C) et avec une tension d'alimentation variant de la valeur nominale (0,7V) au régime proche du seuil (0,3V). Les cellules logiques NOR2, NAND2 et AOI21 ont été évaluées sous faible LET, c'est-à-dire moins de  $15\text{MeV.cm}^2.\text{mg}^{-1}$  ce qui correspond aux particules secondaires représentatives induites par des neutrons ou des protons dans les applications avioniques et terrestres. La susceptibilité à la SE a également été étudiée dans des LET plus élevés (30 et  $58\text{MeV.cm}^2.\text{mg}^{-1}$ ) représentant l'environnement spatial. Pour obtenir une estimation plus précise, la base de données SET a été simulée pour tous les vecteurs d'entrée. De plus, la sortie de chaque cellule est connectée à une chaîne de quatre inverseurs, permettant l'évaluation des effets de propagation. Un défaut est comptabilisé si l'amplitude de tension du noeud de sortie dépasse la tension de seuil de grille ( $V_{DD}/2$ ). Ce travail adopte la section transversale ( $\sigma_{cs}$ ) comme facteur de mérite central pour estimer la susceptibilité des cellules logiques à la SE.

## **COMPORTEMENT TYPIQUE DES CELLULES LOGIQUES FINFET**

### **SENSIBILITE A VARIABILITE DE FABRICATION**

La caractérisation des dispositifs adoptant le modèle électrique fourni par ASAP7 est cohérente avec ceux obtenus à l'aide d'autres technologies multi-serveurs (MEINHARDT; ZIMPECK; REIS, 2014a). Les fluctuations de la fonction de travail dominant l'impact sur les courants  $I_{ON}/I_{OFF}$  des appareils FinFET. L'augmentation du nombre d'ailettes est un moyen de protéger les dispositifs contre les variations géométriques, mais cette méthodologie ne permet pas d'atténuer les effets de fluctuation de la WF. Pour cette raison, désormais, cette thèse adopte toujours les fluctuations du travail pour toutes les évaluations de la variabilité de fabrication.

Les fluctuations WF sur les périphériques FinFET peuvent générer de la puissance et retarder les écarts. Ces écarts sont estimés à l'aide de l'écart type normalisé (relation  $\sigma/\mu$ ). Dans ce travail, nous adoptons les termes « variabilité de puissance » et « variabilité de délai » pour indiquer les écarts de puissance et de retard dus aux fluctuations de la WF, respectivement.

Comme prévu, la sensibilité des cellules logiques à la variation de processus ( $\sigma/\mu$ ) augmente lorsque des niveaux plus élevés de fluctuations de la WF ont été explorés pour les deux métriques. Les cellules logiques avec un plus grand nombre d'entrées sont moins robustes aux fluctuations de WF. Par exemple, le NAND4 est au moins 9,2% et 20,6% plus sensible que le NAND2 à la variabilité du délai et de la puissance, respectivement.

En comparant la sensibilité des cellules de base, les variations de processus affectent davantage les cellules NOR que les cellules NAND. En ce qui concerne les cellules complexes, les cellules AOI21 et OAI211 sont plus robustes pour retarder la variabilité que les cellules OAI21 et AOI211. Le comportement de ces cellules est similaire à celui de la variabilité de puissance, sauf lorsque la cellule AOI21 présente une déviation de 1 à 3% et que la cellule OAI211 présente une variation de 5% par rapport aux valeurs nominales. En général, les cellules logiques FinFET sont plus sensibles à la variabilité de retard pour des déviations jusqu'à 4%, mais un comportement opposé peut être vérifié pour des variations de 5%, c'est-à-dire que les cellules logiques deviennent plus sensibles à la variabilité de puissance. De plus, des variations de 5% triplent presque la sensibilité des cellules logiques à la variabilité de puissance par rapport à 4% d'écart. La moyenne ( $\mu$ ) des simulations de MC en version standard est considérée ultérieurement pour estimer les pénalités imposées par les techniques d'atténuation au niveau du circuit.

### **SENSIBILITE AUX *SOFT ERRORS***

Les *soft errors* sont des événements transitoires à court intervalle de temps induits par des particules énergétiques provenant de radiations terrestres et spatiales. Les erreurs logicielles induites par les radiations peuvent entraîner des défaillances critiques du comportement du système, pouvant entraîner des pertes de vies humaines ou financières. Cette section évalue l'impact des erreurs logicielles dans trois cellules logiques FinFET sous des valeurs LET faibles, c'est-à-dire inférieures à  $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ . Ces valeurs de LET ont été ciblées car correspondent à des particules secondaires induites par des neutrons dans les applications avioniques et terrestres. La métrique utilisée pour l'évaluation des erreurs logicielles est la section transversale SET en considérant le vecteur d'entrée le plus sensible ainsi que la moyenne de tous les vecteurs d'entrée. La figure 8 montre la sensibilité de *soft error* des cellules NAND2, NOR2 et AOI21 à un régime proche du seuil (0,3 V) en considérant le vecteur d'entrée le plus sensible. Pour toutes les technologies LET étudiées, les trois portes logiques sont exemptes de défauts à 0,6V et de tension principale. La cellule AOI21 est exempte de défauts avec une LET de  $5\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , et des erreurs logicielles ne sont observées que dans les cellules NAND2 et NOR2 en sortie à 0,3V. Par ailleurs, il est possible d'observer certaines failles à 0,4V et à 0,5V lorsqu'on étudie une valeur LET plus élevée ( $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ). La réduction du nombre de défauts est due à la nature FinFET qui augmente la charge minimale requise pour induire une impulsion SET.

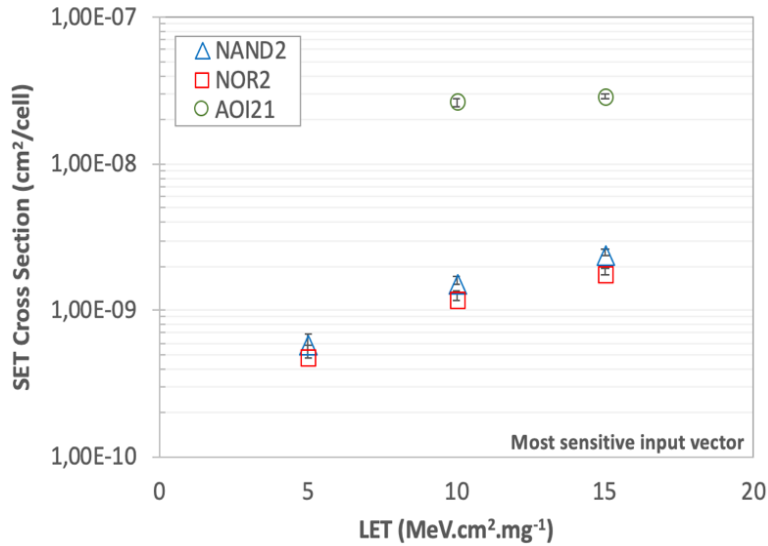


Figure 8 : SET section transversale de cellules logiques fonctionnant à un régime proche du seuil en tenant compte du vecteur d'entrée le plus sensible

## 5. ATTENUATION DE LA VARIABILITE DE FABRICATION E DES *SOFT ERRORS*

Ce chapitre évalue l'utilisation d'approches au niveau du circuit dans la conception des cellules logiques FinFET afin d'améliorer les effets de la variabilité des processus et la susceptibilité aux *soft errors*. En plus des avantages de chaque technique, ce chapitre présente également la tendance à l'atténuation lorsque différents niveaux de fluctuations de WF, de dimensionnement et de valeurs de LET ont été utilisés. Les résultats présentés dans ce chapitre cherchent à: 1) prouver l'efficacité des quatre approches d'atténuation au niveau du circuit étudiées dans cette thèse en considérant différents scénarios de test, 2) indiquer les avantages et les inconvénients de l'adoption de chacune d'elles, et 3) fournir une comparaison globale pour permettre aux concepteurs de choisir la meilleure technique en fonction de l'application cible.

Les cellules logiques peuvent être soumises à des fluctuations élevées (5%), moyennes (3%) ou faibles (1%), de sorte que ces variations peuvent avoir une incidence sur la puissance, les retards de propagation ou les deux. La sensibilité des cellules logiques aux variations du processus est mesurée par l'écart type normalisé (relation  $\sigma/\mu$ ). Comme précédemment présenté, les déviations de puissance et de propagation dues aux variations de processus sont dénommées dans ce travail par variabilité de puissance et de retard.

La figure 9 montre l'impact d'un processus de fabrication avec un écart de 5% lorsque les approches d'atténuation de version standard ou au niveau du circuit sont adoptées dans la conception. La meilleure technique pour atténuer l'impact sur la variabilité de la puissance est basée sur l'insertion de *Schmitt Triggers*. Même pour les écarts les plus faibles, l'ajout de Schmitt Trigger reste le plus avantageux. Après cela, la technique la plus indiquée pour atténuer

la variabilité consiste à insérer des *sleep transistors* ou des *decoupling cells*. Pour les conceptions avec 5% d'écart, l'amélioration des deux techniques est similaire. Toutefois, pour les faibles niveaux de fluctuation de WF (1-4%), l'approche par *sleep transistor* est la deuxième meilleure option. Enfin, la technique avec moins d'atténuation de la variabilité d'énergie est le *transistor reordering*.

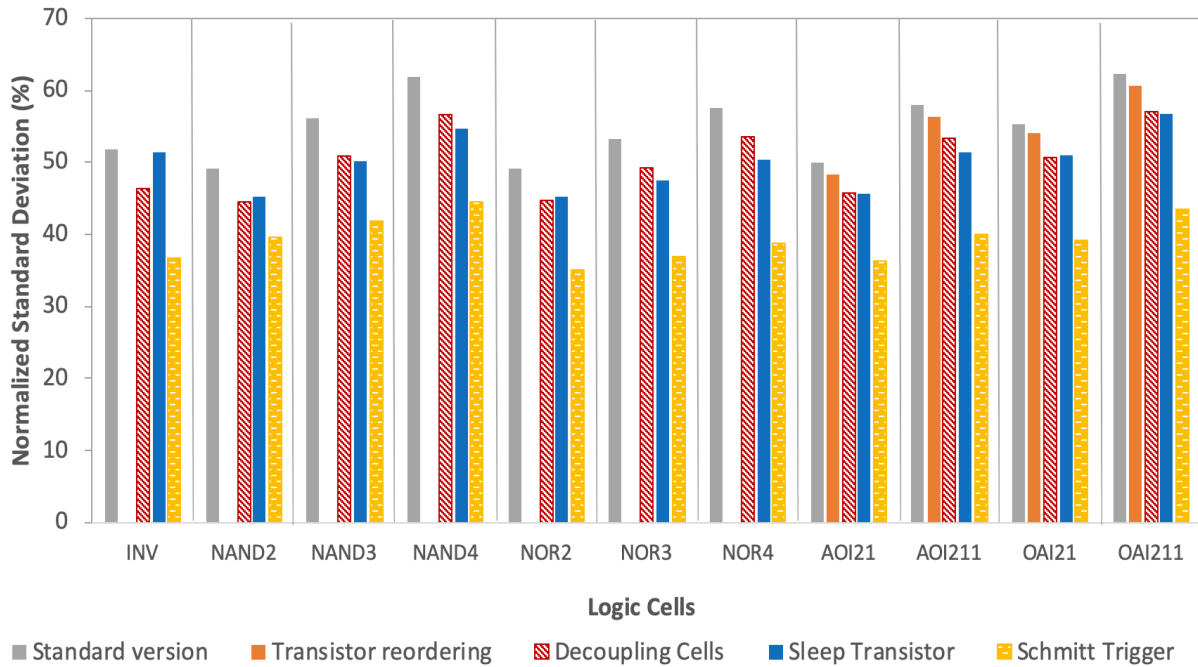


Figure 9 : Variabilité d'énergie utilisant des approches d'atténuation au niveau du circuit

Pour atténuer la variabilité du délai, il est plus difficile de dégager une tendance générale pour toutes les cellules logiques évaluées, comme le montre la figure 10. À l'exception des cellules AOI21 et OAI21, l'insertion de *Schmitt Trigger* est la meilleure technique pour améliorer la variabilité du délai. La seconde alternative varie également en fonction des cellules logiques. Par exemple, l'adoption d'un *sleep transistor* est préférable au *decoupling cells* pour les cellules NAND et OAI211, mais l'inverse se produit pour les cellules INV, NOR et AOI211. Pour les cellules AOI21 et OAI21, la première meilleure option consiste à utiliser les *sleep transistors*. Après, le *Schmitt Trigger* est plus indiqué. La technique de *transistor reordering* n'a apporté que des avantages significatifs en termes d'atténuation de la variabilité de performance pour la cellule OAI211. Pour des niveaux inférieurs de fluctuations de WF (1-4%), la même tendance a été observée pour toutes les cellules logiques.

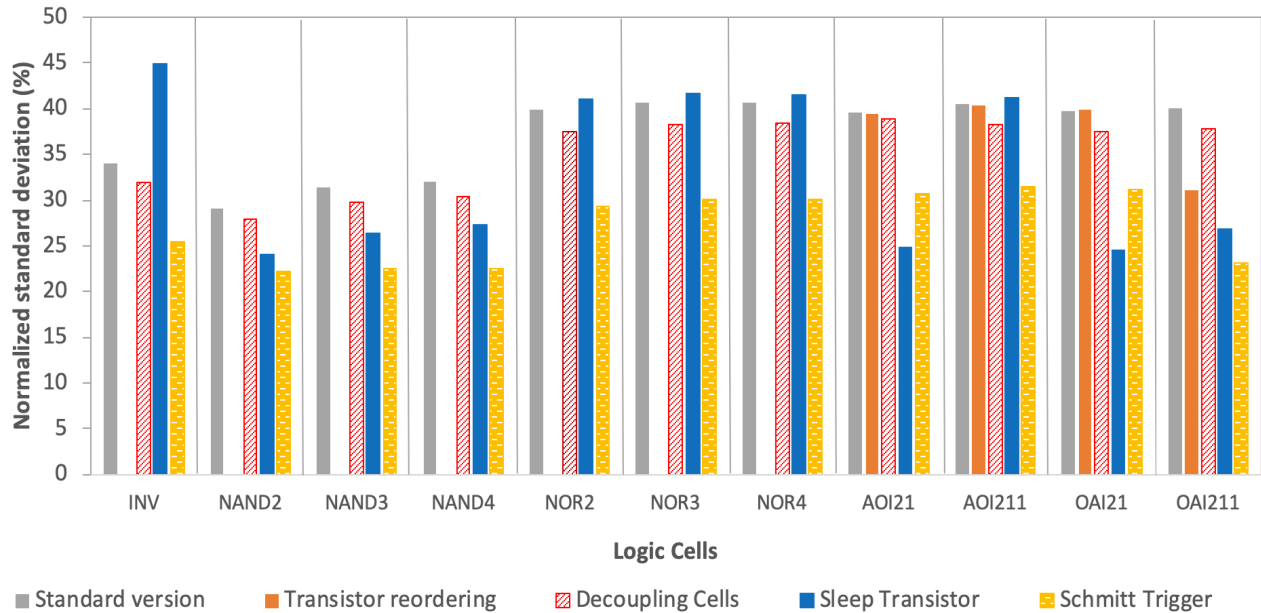


Figure 10 : Variabilité de performance en utilisant des approches d'atténuation au niveau du circuit

Les quatre techniques utilisées pour atténuer les effets des variations de processus et des erreurs commises induites par un rayonnement ont entraîné certaines pénalités en termes de surface, de consommation électrique et de performances. La technique de *transistor reordering* n'entraîne aucune pénalité de zone et son impact sur la puissance et les performances est faible. Cependant, cette technique n'a pas apporté d'améliorations significatives aux effets causés par les variations de processus sur des cellules complexes. De plus, la réorganisation des transistors devient la cellule logique plus sensible aux *soft errors*.

La connexion de *Schmitt Trigger* à la sortie des cellules logiques est le meilleur moyen de réduire considérablement l'impact des variations de fabrication et d'obtenir des cellules logiques exemptes de défauts, même à un régime proche du seuil. Cependant, des pénalités plus élevées sont observées, principalement en ce qui concerne la consommation d'énergie et les performances. L'insertion de *decoupling cells* a la même pénalité en surface que la technique de *Schmitt Trigger*, mais les inconvénients en termes de consommation d'énergie et de performances sont divisés par deux. De plus, une conception avec *decoupling cells* diminue la susceptibilité aux *soft errors* des cellules logiques. L'approche des *sleep transistor* a introduit des pénalités de faible surface et des cellules logiques exemptes de pannes, même à un régime proche du seuil, mais l'impact sur la consommation et les performances est considérable. Pour la plupart des techniques et des cellules logiques analysées, les pénalités sont plus lourdes lorsque les fluctuations de WF sont faibles.

Les *decoupling cells* avec un plus grand nombre d'ailettes augmente, voire plus, la robustesse des cellules logiques. Cependant, les pénalités augmentent en même temps que le nombre

d'ailerons. Mais pour cette technique, les pénalités introduites sont encore agréables. De la même manière, des *Schmitt Trigger* plus importants dans la conception augmentent l'atténuation de la variabilité d'énergie, mais les inconvénients techniques de la consommation et des performances sont inacceptables. D'autre part, les transistors de sommeil avec un plus grand nombre d'ailettes ne minimisent pas la sensibilité des cellules logiques de manière significative. Pour cette raison, les grands *sleep transistors* ne sont pas conseillés en raison des pénalités élevées introduites.

En général, en considérant les résultats moyens des cellules logiques obtenues pour toutes les approches d'atténuation au niveau du circuit ainsi qu'une évaluation globale de tous les sujets et scénarios de test présentés dans ce travail, il est possible de conclure que :

1. Schmitt Trigger est la meilleure technique si les concepteurs ne font qu'améliorer l'impact de la variabilité, sans aucune exigence de domaine, de performance ou de puissance ;

2. Le *sleep transistor* est la meilleure option si les concepteurs s'attachent à accroître la robustesse de la variabilité de fabrication, mais qu'ils ont des restrictions de zone ;

3. Les *decoupling cells* sont indiquées si l'objectif des concepteurs est d'améliorer l'impact de la variabilité, mais qu'elles ont des exigences en matière de puissance ou de performances ;

4. Les *sleep transistors* ou *Schmitt Triggers* sont les meilleurs choix si les concepteurs se concentrent uniquement sur la susceptibilité aux *soft errors* ;

5. Les *sleep transistors* sont plus indiqués si les concepteurs s'attachent principalement à atténuer l'impact des *soft errors*, mais qu'ils ont des contraintes de zone ;

6. Les *decoupling cells* sont la meilleure alternative si les concepteurs s'attachent à améliorer les effets de la variabilité de fabrication et à devenir un circuit plus robuste aux défauts transitoires, avec des pénalités acceptables en termes de surface, de performances et de consommation d'énergie.

## **6. CONCLUSIONS**

Les dispositifs FinFET ont été largement adoptés par l'industrie des semi-conducteurs pour les nœuds technologiques de moins de 22 nm, soulevant des questions essentielles liées à la fiabilité des systèmes électroniques. Les petites configurations géométriques imposées par les technologies avancées intensifient les variations de processus, ainsi que la densité plus élevée permettant à une seule particule énergétique d'affecter plusieurs nœuds adjacents. Les principales conséquences de ces défis sont la perte de rendement paramétrique et les défaillances critiques du comportement du système, qui peuvent entraîner des pertes en vies humaines ou financières. L'impact de la variabilité des processus continue d'augmenter à chaque nouveau nœud technologique, et il est de plus en plus difficile de limiter la technologie à l'échelle utilisant des dispositifs FinFET. Du point de vue de la conception, les variations de processus et les erreurs réduites induites par le rayonnement dans les nœuds FinFET

nécessitent une estimation précise ainsi que de nouvelles méthodologies de conception capables de réduire les effets causés par celles-ci.

Selon la revue de la littérature, peu de travaux proposent des techniques permettant d'atténuer l'impact des variations de processus et des erreurs logicielles, en particulier pour les technologies FinFET. En outre, il n'existe pas d'approches d'atténuation au niveau des circuits permettant d'examiner les modifications de la conception afin d'obtenir des solutions plus robustes. De cette manière, cette thèse fait progresser l'état de la technique en fournissant:

1. L'évaluation des cellules logiques FinFET sous variabilité de fabrication et effets de rayonnement à l'aide d'un kit de conception de processus prédictif FinFET à 7-nm;
2. La conception de cellules logiques utilisant quatre approches différentes au niveau du circuit pour atténuer l'impact causé par les fluctuations du travail et les erreurs logicielles.
3. un compromis entre les gains et les pénalités de chaque approche concernant la surface, les performances, la consommation d'énergie, la durée d'impulsion SET et la section transversale SET;
4. La tendance d'atténuation des techniques au niveau du circuit lorsque différents niveaux de variation de processus, de dimensionnement de transistor et de LET ont été appliqués dans la conception.

Les approches d'atténuation au niveau du circuit explorées dans cette thèse étaient la réorganisation des transistors et l'insertion de cellules de découplage, de déclencheurs de Schmitt et de transistors de sommeil.

En général, toutes ces techniques réduisent les effets de variabilité de fabrication et la susceptibilité aux *soft errors*, introduisant moins de pénalités, de coûts de mise en œuvre et de complexité de conception par rapport aux rares solutions disponibles dans la littérature.

La technique de réordonnancement des transistors peut augmenter jusqu'à 8% la robustesse des cellules complexes sous des variations de processus (5% d'écart). Cependant, cette méthode n'est pas favorable à l'atténuation des erreurs logicielles, augmentant la sensibilité des cellules complexes jusqu'à 20% pour les faibles LET. Parmi toutes les techniques évaluées, le réordonnancement des transistors présentait moins de frais généraux de puissance et de performances, de plus, il ne comporte aucune pénalité de surface.

L'adoption de *decoupling cells* montre des résultats intéressants pour le contrôle de la variabilité de puissance sous des niveaux de variation supérieurs à 4%. D'autre part, cette technique est efficace pour la réduction de la variabilité du délai indépendamment des niveaux de variation. Les améliorations les plus importantes de la variabilité du délai peuvent être constatées pour des niveaux de variation plus faibles (1 à 3%). La conception avec cellules de découplage diminue la susceptibilité à la *soft error* d'environ 10% pour une valeur LET élevée ( $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ). Les gains avec des LET inférieurs peuvent atteindre un maximum de 4%.

Cette technique présentait une surcharge de zone importante, mais un impact moindre sur les métriques de puissance et de performance.

La meilleure approche pour contrôler les variations de fabrication consiste à connecter un *Schmitt Trigger* à la sortie des cellules FinFET. Cette technique peut améliorer la variabilité des retards jusqu'à 50%, principalement pour les processus de fabrication avec 2 à 4% d'écart WF. Pour la variabilité de puissance, une robustesse plus élevée a été obtenue avec des niveaux de variation plus élevés (4-5%). De plus, toutes les cellules logiques étudiées sont exemptes de défauts, même au régime proche du seuil (0,3V) et sous l'influence d'une forte LET ( $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ). Cependant, comme cette technique ajoute six transistors supplémentaires, elle introduit des pénalités plus sévères en termes de surface et de puissance.

L'insertion d'un *sleep transistor* entre le réseau déroulant et le rail de masse est avantageuse principalement pour le contrôle de la variabilité de la puissance. Les améliorations pour certaines cellules dépassent 10% pour des niveaux de variation plus élevés (4-5%). D'autre part, l'efficacité de cette méthode pour la réduction de la variabilité du retard dépend de la manière dont les transistors sont disposés avec le *sleep transistor* dans le réseau déroulant. Cette technique est également exempte de défauts, même au régime proche du seuil (0,3V) et sous l'influence d'une forte LET ( $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ). La disposition avec un transistor de veille introduit une petite surface supplémentaire, mais l'impact sur les métriques de puissance et de performance est très important.

Une conception avec de plus grandes *decoupling cells* (quatre ou cinq ailettes) est avantageuse pour atténuer la variabilité des processus, avec une augmentation acceptable des frais généraux. Le *Schmitt Trigger* avec un plus grand nombre d'ailettes améliore également la sensibilité aux fluctuations de la WF, mais les inconvénients techniques impliqués sont inacceptables. D'autre part, l'augmentation du dimensionnement du *sleep transistor* ne modifie pas de manière significative la sensibilité à la variabilité de fabrication.

Le choix de la technique la plus appropriée dépend de l'application cible et de ses exigences en matière de zone, de consommation électrique et de performances. La technique de Schmitt Trigger a présenté les meilleurs résultats pour l'atténuation de la variabilité de fabrication et la dureté du rayonnement. Cependant, cette approche introduit des pénalités critiques sur la surface, les retards et la consommation d'énergie. De cette manière, si un concepteur souhaite améliorer la fiabilité du circuit en introduisant des pénalités plus acceptables, une conception avec des *decoupling cells* est plus indiquée pour contrôler la variabilité du retard. D'autre part, pour obtenir une réduction de la variabilité de puissance et de la susceptibilité aux *soft errors*, la meilleure option consiste à utiliser la technique du *sleep transistor*.

Enfin, cette thèse fournit un ensemble d'informations utiles pour aider: 1) l'industrie des semi-conducteurs à obtenir des améliorations de rendement paramétriques en évitant les



nombreuses étapes de la reconception; 2) les concepteurs introduisent une technique d'atténuation au niveau de la disposition pour une application donnée, connaissant tous les avantages et les inconvénients de son adoption; et 3) l'industrie aérospatiale telle que l'ONERA, le laboratoire aérospatial français, à concevoir des systèmes plus fiables pour la prochaine génération de constellations de nano-satellites.

## **TRAVAUX FUTURS**

Il existe plusieurs possibilités de nouvelles expériences et scénarios de test pouvant être réalisés à partir de cette thèse. Premièrement, il est possible d'étendre cette recherche en explorant deux autres approches potentielles pour améliorer la robustesse des cellules logiques FinFET : la conception à plusieurs doigts (FORERO et al., 2017) et le pitch à double porte (MARELLA et al., 2015). Les deux techniques doivent être mises en œuvre au niveau de la mise en page.

Une étude approfondie peut être réalisée pour déterminer les meilleurs endroits pour placer ces cellules dans une chaîne de portes, de sorte qu'il n'est pas pratique d'appliquer des *decoupling cells*, *Schmitt Trigger* ou des *sleep transistors* dans toutes les cellules logiques de circuits intégrés. En outre, il est crucial de mieux comprendre car chaque technique contribue à atténuer les effets des variations de fabrication et des *soft errors* induites par les radiations. De plus, certains moyens de réduire les inconvénients techniques (surface, puissance, délai) imposés par les approches d'atténuation au niveau du circuit explorées dans ce travail doivent être examinés.

Une autre possibilité de travail futur est l'évaluation des fluctuations de la WF et des erreurs logicielles, en considérant le cas le plus défavorable de défaillances pour introduire les variations de processus sur les circuits. En outre, l'impact des variations de processus peut également être estimé en utilisant comme métrique le produit de délai-énergie (PDP), qui offre un compromis précis entre les résultats de variabilité de puissance et de délai. Enfin, depuis cette thèse, une bibliothèque de cellules pour les conceptions numériques peut être développée, se concentrant sur des questions de fiabilité, telles que l'atténuation de la variabilité des processus et la dureté du rayonnement.

## Table of Contents

<b>Chapter 1: Introduction</b> .....	32
1.1 Motivation.....	33
1.2 Objectives.....	34
1.3 Work Organization.....	35
<b>Chapter 2: Theoretical Foundation</b> .....	37
2.1 Multigate Devices.....	37
2.2 General Background of FinFET Technology.....	42
2.3 The Advancement in the Semiconductor Industry.....	44
2.4 Layout Design using FinFET Devices.....	47
2.5 FinFET Predictive Models.....	51
2.5.1 Technology models for SPICE simulations.....	51
2.5.2. Process Design Kit (PDK) .....	53
<b>Chapter 3: FinFET Technology Challenges</b> .....	58
3.1 Process Variability.....	60
3.1.1 Sources of Process Variability.....	63
3.1.1.1. Line Edge Roughness.....	64
3.1.1.2 Metal Gate Granularity.....	67
3.1.1.3 Random Dopant Fluctuation.....	67
3.1.2 Literature review about process variability.....	68
3.1.2.1 General Background.....	68
3.1.2.2 State-of-the-art works.....	69
3.2 Radiation-Induced Soft Errors.....	76
3.2.1 Radiation environment.....	76

3.2.2 Radiation effects on devices.....	77
3.2.3 Fault masking.....	79
3.2.4 Charge collection mechanism in FinFET devices.....	82
3.2.5 Literature review about radiation effects.....	84
3.2.5.1 General background.....	84
3.2.5.2 State-of-the-art works.....	86
3.3 Circuit-Level Mitigation Techniques.....	93
3.3.1 Transistor reordering.....	94
3.3.2 Decoupling cells.....	95
3.3.3 Schmitt Trigger.....	96
3.3.4 Sleep Transistor.....	97
<b>Chapter 4: Evaluation Methodology.....</b>	<b>98</b>
4.1 Process Variability Evaluation.....	101
4.2 Soft Error Estimation.....	102
4.3 Typical Behavior of FinFET Logic Cells.....	105
4.3.1 Effects of process variability.....	105
4.3.1.1 Characterization of devices from ASAP7 under process variations.....	105
4.3.1.2 Sensitivity to process variations.....	109
4.3.2 Susceptibility to Soft Errors.....	111
<b>Chapter 5: Process Variability and Soft Error Mitigation.....</b>	<b>114</b>
5.1 Design with Circuit-Level Mitigation Approaches .....	114
5.1.1 Transistor reordering.....	114
5.1.1.1 Soft error susceptibility.....	117
5.1.2 Decoupling cells.....	120

5.1.2.1 Impact of different levels of WF fluctuations.....	122
5.1.2.2 Sizing influence.....	124
5.1.2.3 Exploring decoupling cells with transistor reordering.....	124
5.1.2.4 Soft error susceptibility.....	126
5.1.3. Schmitt Trigger.....	128
5.1.3.1 Impact of different levels of WF fluctuations.....	130
5.1.3.2 Sizing influence.....	131
5.1.3.3 Soft error susceptibility.....	131
5.1.4. Sleep Transistors.....	132
5.1.4.1 Impact of different levels of WF fluctuations.....	134
5.1.4.2 Sizing influence.....	135
5.1.4.3 Soft error susceptibility.....	136
5.2 Technique Drawbacks .....	136
5.2.1 Area.....	137
5.2.2 Power Consumption.....	138
5.2.3 Performance.....	141
5.3 Overall Comparison.....	143
<b>Chapter 6: Conclusions.....</b>	<b>148</b>
6.1 Future Works.....	150
<b>References.....</b>	<b>152</b>

# Chapter 1: Introduction

---

Novel materials and new device architectures had to be implemented in the integrated circuits to ensure the technology scaling sub-22nm (PRADHAN; SAHU; RANJAN, 2016). The 3D structure and the lightly doped channel of FinFET devices imply in a significant reduction of leakage currents, superior immunity to the short channel effects (SCE), the increase of carrier mobility and a decrease of random dopant fluctuations (RDF) (KING, 2005) (AGOSTINELLI et al., 2010). All these characteristics helped to enhance the electrostatic control of the channel, one of the main challenges faced during the planar scaling. In this way, the adoption of FinFET devices brought several benefits for the semiconductor industry, maintaining the pace of less power consumption, better performance, and higher density.

On the other hand, the small geometric patterns imposed by the advanced technology nodes raise essential topics related to the reliability of electronic systems. At nanometer regime, there are more potential sources of variability (COLLINS, 2014), the lower supply voltages increase the sensitivity to the external noise as well as the higher density allows that a single energetic particle affects multiple adjacent nodes (ENDO et al., 2009) (BHUVA et al., 2015). These factors can compromise entire blocks of logic cells because they can modify the transistor structure and/or alter the electrical properties, decreasing the integrated circuits robustness.

The process variability represents a random deviation from the typical design specifications that stimulates the circuit degradation, abnormal power consumption, and performance divergence (TASSIS et al., 2014). FinFET technologies are more prone to the process variations due to the wavelength adopted in the lithography step and the use of high-k dielectrics to improve the gate control on the channel region (DESHMUKH et al., 2015). In the first case, as the wavelength has not kept pace with the technology scaling, the transfer of small geometric standards to the substrate surface results in a deviation in the device structure after the manufacturing process. On the other hand, the use of metal as gate material modifies the

orientation of the grains, generating different work-functions (WF) aligned randomly that implies in higher work-function fluctuations (DADGOUR et al., 2010).

The soft error (SE) arises from the interaction of energetic particles with the silicon, coming from space and terrestrial radiations. In general, nanometer technologies decrease the minimum charge required to induce a single event transient (SET) pulse. This happens due to reduced nodal capacitances, low supply voltages, and also due to the higher frequency operations, which increases the probability of a memory element latching a SET generated in the combinational logic (BAUMANN, 2005). However, the FinFET disruptive nature is favorable to reduce the SE susceptibility. The connection between the transistor channel and the substrate occurs through a narrow region surrounded by isolation oxides, decreasing the volume of silicon exposed to the charge collection process. This modifies the sensitive areas, and consequently, it limits the increase of soft errors in the FinFET technologies (SEIFERT et al., 2015).

Although the FinFET devices present attractive properties to control the radiation-induced soft errors, other reliability challenges, such as the process variability, can modify the linear energy transfer (LET) threshold to induce a soft error. In this way, process variability mitigation and radiation hardness became two relevant reliability requirements as chip manufacturing advances more in-depth into the nanometer regime.

## **1.1. Motivation**

Integrated circuits with process variations can fail to meet some performance or power consumption criteria, leading to the parametric yield loss and demanding several redesign steps. Radiation-induced soft errors can provoke temporary data loss inducing to critical failures on system behavior even at the ground level. Depending on the target application, soft errors also can result in human life losses. These consequences emphasize the importance of creating new design guidelines able to deal with the challenges imposed by sub-22nm technologies.

The roadmap of most renowned semiconductor industries still points out the use of FinFET devices for the next generation of nanotechnologies. Additionally, a predictive 7-nm FinFET

process design kit (PDK) became available for the academic use allowing in-depth research at the layout level (CLARK et al., 2016). From a design standpoint, these challenges require a detailed and accurate evaluation considering several tests scenarios and verifying all the unwanted effects caused on FinFET circuits. Furthermore, the exploration of mitigation approaches and the development of electronic design automation (EDA) tools are essential since the early steps of design to obtain more reliable circuits.

Several techniques can be applied in different abstraction levels for enhancing the reliability of circuits. On the literature, some works investigated the impact of process variability and the radiation effects on FinFET technologies, mainly at the device and electrical levels, but much less understand has been gained at the layout level. Moreover, only a few works proposed solutions to attenuate the effects caused by them. The most effective approaches in the literature for mitigating the process variations and transient faults are commonly related to the use of a different structure and/or material during the fabrication process, or hardware replication, respectively. However, manufacturing changes have an expensive cost with higher complexity involved, besides the hardware redundancy introduces large overheads. Circuit-level approaches that modify the circuit design can be interesting alternatives to achieve more robust solutions, with smaller cost of implementation and fewer penalties.

## **1.2. Objectives**

Some researches adopt circuit-level approaches to increase the robustness or to optimize the performance and power consumption of circuits. However, to the best of our acknowledgment, only a few works indicate the influence of circuit-level techniques to reduce the process variability and radiation effects on FinFET technologies. In this way, the overall purpose of this thesis is to analyze potential methods at circuit-level to mitigate the impact caused by these challenges, knowing all the pros and cons of adopting it. This thesis is divided into the following steps to reach this objective:

1. To investigate the behavior of FinFET logic cells designed at the layout level under process variations and radiation effects;

2. To evaluate the effectiveness of four circuit-level techniques to mitigate the impact caused by work-function fluctuations and soft errors;
3. To demonstrate the mitigation tendency when different levels of process variation, transistor sizing, and radiation particle characteristics, such as LET, are applied in the design using the circuit-level techniques;
4. To trace a trade-off between the gains and penalties of each approach regarding the area, performance, power consumption, SET pulse width, and SET cross-section;
5. To provide an overall comparison between all techniques applied in this work and those available in the literature.

The circuit-level techniques explored in this work are the transistor reordering, and the insertion of decoupling cells, Schmitt Triggers, and sleep transistors in the design. Transistor reordering is based on the optimization of the transistor arrangements. The use of decoupling cells is a capacitive method. The Schmitt Trigger acts as a feedback scheme to minimize the output degradation. The addition of sleep transistors is a power-gating strategy. The potential of each method to make FinFET logic cells more robust to work-function fluctuations and soft errors are assessed comparing the well-known predefined metrics of the standard design with the design adopting each technique.

As a differential factor from most of the related studies, this thesis considers the ASAP7 PDK allowing the design exploration at the 7-nm node, that is the same technological node explored by the renowned semiconductor industries currently. Moreover, this work adopts a soft error prediction tool, MUSCA SEP3, which considers layout features coupled with radiation-induced currents modeled by the tool, and the electrical simulations (HUBERT et al., 2009).

### **1.3. Work Organization**

This thesis is organized as follows. Chapter 2 introduces the theoretical foundation of FinFET devices. It contains the description of FinFET operation, a review of the technological evolution for the manufacture, and also discusses some points about the layout design and predictive models. Chapter 3 describes in detail the two reliability challenges evaluated in this work: process variability and radiation-induced soft errors. Moreover, this chapter presents the



four circuit-level mitigation techniques investigated in this work and how each one was implemented.

Chapter 4 explains the methodology used in this work from the FinFET design to the evaluation of process variability and radiation susceptibility. This chapter also presents the typical behavior of FinFET logic cells for comparison purpose, i.e., without applying any circuit-level approach to mitigate the effects of WF variations and soft errors. Chapter 5 demonstrates the potential of each circuit-level technique applied in FinFET logic cells and technical drawbacks of each one. It also contains an overall comparison among the proposed techniques as well as a comparison with the related works. Chapter 6 shows the conclusions, which reinforce the main contributions of this thesis and point out some future works.

# Chapter 2: Theoretical Foundation

---

This chapter explains the advantages in replacing planar devices by multigate devices to keep the technology scaling as well as the basic concepts related to FinFET technologies such as structure/properties of devices, advancement in the semiconductor industry, design rules for layout generation, predictive models, and process design kit information. This chapter helps to reinforce that FinFET devices are still extensively studied in academia and applied to industrial manufacturing processes, considering different test scenarios.

## 2.1 Multigate Devices

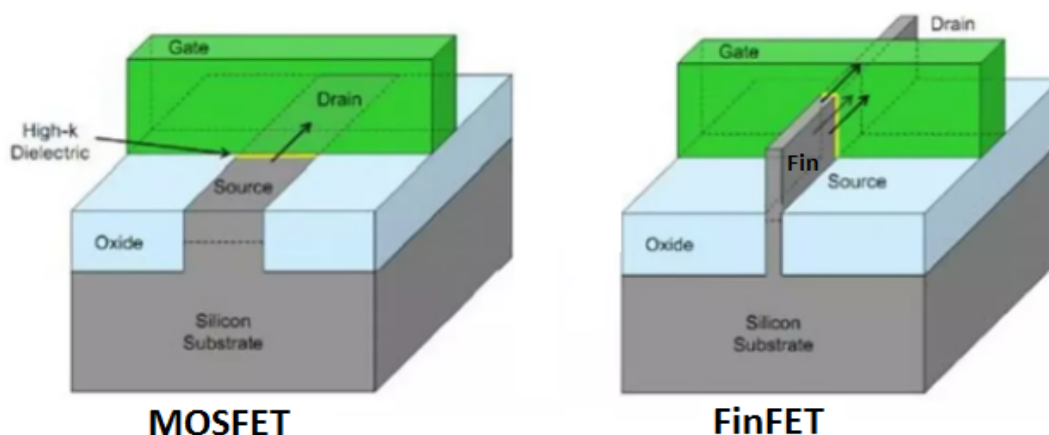
The integrated circuits (IC) increase the transistor count in a same chip as the technology scaling down according to Moore's Law, satisfying the demand for higher density, lower cost, more functionalities, superior clock frequency, and reduced power consumption (ANGHEL et al., 2007). Nevertheless, in each new technology node, it is harder to maintain the exponential growth rate incurring in higher design efforts and longer time to market. The high integration factor and the technology evolution brought new challenges for Very Large-Scale Integration (VLSI) designs.

For several decades, the planar CMOS technology was the main core of integrated circuits, but the metal-oxide-semiconductor field-effect transistor (MOSFET) reached the physical limits (FRANK et al., 2001) (SAHA; BHOWMICK; BAISHYA, 2017). The control of the gate over the channel region suffers changes as the gate electrode is reduced. MOSFET devices required high channel doping to control the SCE such that it reflected in the mobility degradation and a significant increase of the leakage currents, affecting the transistor performance directly (ITRS, 2011). For ensure the advancement of microelectronics in sub-22nm nodes, novel materials, and new device architectures need to be adopted able to deal with the electrostatic control of the channel, reduction of leakage currents, decrease of the sub-threshold slope, and parametric yield loss (PRADHAN; SAHU; RANJAN, 2016).

Multigate devices gained prominence for presenting better SCE control, reduced leakage currents, high driving capability, and a better yield (MISHRA; MUTTREJA; JHA, 2011). Hence, the International Technology Roadmap for Semiconductors (ITRS) pointed them as the most attractive choice to overcome obstacles and keep scaling down (KING, 2005) (ITRS, 2011). There are a variety of multigate devices available reported in the literature such as the  $\pi$ -gate (PARK; COLINGE; DIAZ, 2001),  $\Omega$ -gate (YANG et al., 2002), gate-all-around (GAA) (SINGH et al., 2006), FlexFET (WILSON et al., 2007), and Trigate (CARTWRIGHT, 2011) (JAMES, 2012). However, the fin-shaped field effect transistor (FinFET) was predominantly adopted by the semiconductor industry mainly due to the similarity of the manufacturing process with conventional planar technologies.

Figure 2.1 shows a basic comparison between the planar and FinFET structures. A FinFET device consists of a vertical silicon fin to form the channel region and to connect the source and drain regions at each end. The vertical fin wraps the gate region, and a MOS channel is formed at the two sidewalls plus top-side of the fin. The fin-like geometry implies in no free charge carriers available, making the suppression of SCE possible (KING, 2005). Unlike the MOSFET devices, FinFET channels have lower doping ensuring better mobility of the carries and consequently, better performance.

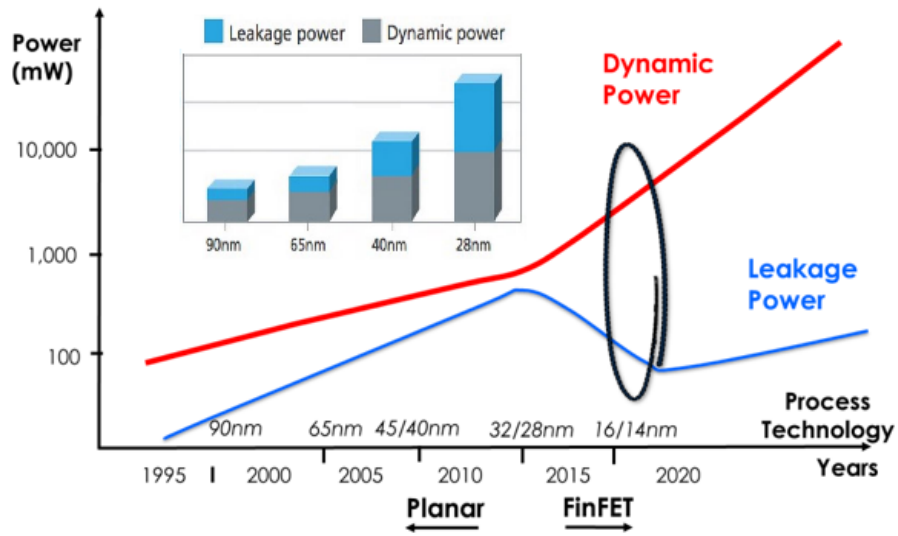
Figure 2.1: The structural differences between MOSFET and FinFET devices



Source: Adapted from (KAWA, 2012)

The adoption of FinFET devices to keep the microelectronic advancements also improves the leakage power significantly in FinFET-based circuits, as shown in Figure 2.2. A little increase of leakage power in sub-10nm FinFET nodes can be observed due to further challenges of technology scaling, but the dynamic power dissipation keeps growing as more transistors being packed together ensuring the best performance for the circuits (RANJAN, 2015). In general, FinFET devices offer interesting power-delay tradeoffs with advantageous characteristics for both low power and high-performance applications (MISHRA; MUTTREJA; JHA, 2011).

Figure 2.2: Planar CMOS and FinFET power consumption trends



Source: Adapted from (MENTOR, 2014) and (RANJAN, 2015)

FinFETs include additional properties to describe the fin configurations besides the length and width typical measures. The key geometric parameters for a FinFET are the gate length ( $L_G$ ), the fin height ( $H_{FIN}$ ), fin thickness ( $T_{Si}/T_{FIN}/W_{FIN}$ ) and oxide thickness ( $T_{OX}$ ), according to Figure 2.3 (a) and (b). Fin engineering (balancing the fin height, fin thickness, oxide thickness, and the channel length) is essential to minimize the leakage current,  $I_{OFF}$ , and maximize the on-state current,  $I_{ON}$  (SWAHN; HASSOUN, 2006). Higher values of fin height can result in structural instability that impacts the manufacturing process and the SCE control. On the other hand, smaller fin height offers more flexibility, but this leads to more silicon area due to the need of

multiple fins (BHATTACHARYA; JHA, 2014). The effective channel length ( $L_{EFF}$ ) and width ( $W_{EFF}$ ) of a single FinFET double-gate transistor are given by Equation 2.1 and Equation 2.2, respectively,

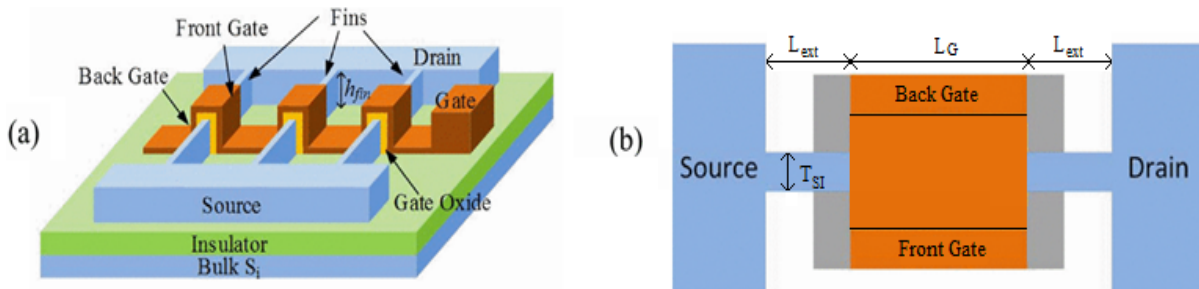
$$L_{EFF} = L_G + 2 \cdot L_{EXT} \quad (2.1)$$

$$W_{EFF} = T_{SI} + W_{MIN} \quad (2.2)$$

where the  $L_{EXT}$  corresponds to the full extension of the source and drain regions, and the  $W_{MIN}$  of a FinFET device is approximately equal to  $2 \cdot H_{FIN}$ . In planar technologies, the transistor channel width can receive arbitrary values as long as it obeys the design constraints. For FinFETs, the channel width has a quantization characteristic using a discrete sizing (NOWAK et al., 2004). For scaling the effective channel width ( $W > W_{MIN}$ ) it is necessary to increase the number of fins connected in parallel, which are sharing a common lateral diffusion, as shown in Figure 2.3 (a). The width of a FinFET with multiple fins is given by Equation 2.3, where  $N_{FIN}$  is the number of fins.

$$W = N_{FIN} \cdot W_{MIN} \quad (2.3)$$

Figure 2.3: The key geometric parameters of FinFET devices



Source: Adapted from (GUPTA; ROY, 2013)

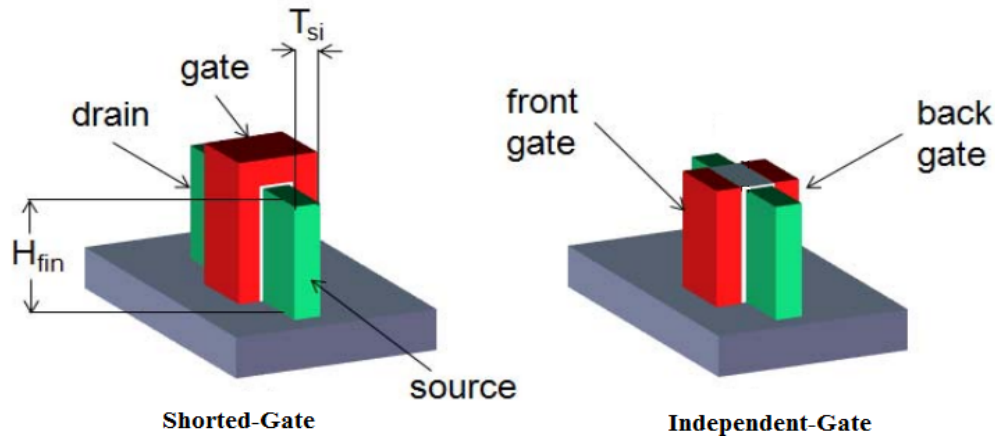
FinFET devices can be designed using different configurations for the gates and also for the substrate. In relation to the gates, FinFETs can be classified as shorted-gate (SG) or independent-gate (IG) (MISHRA; MUTTREJA; JHA, 2011). In the first case, the back-gate (BG)

and the front-gate (FG) are tied together, physically shorted. The SG structure is very similar to MOSFET devices, with three terminals (3T) controlling the transistor operation. In this mode, both gates providing maximum gate drive making a favorable electrostatic control of the channel. However, the off-current is more elevated because it is not possible to regulate the device threshold voltage ( $V_{TH}$ ) electrically.

The IG FinFET modifies the concept previously presented. The top part of the gate is etched out, generating two independent gates to control the channel. This format allows each gate to have a different input signal, generating a four-terminal (4T) transistor (BHATTACHARYA; JHA, 2014). Typically, back-gates are used to control the threshold voltage of front-gates to obtain even smaller leakage currents. Moreover, this configuration offers the designers more flexibility to create low-power circuits (ROSTAMI; MOHANRAM, 2011). The structural differences between SG and IG FinFET devices are shown in Figure 2.4.

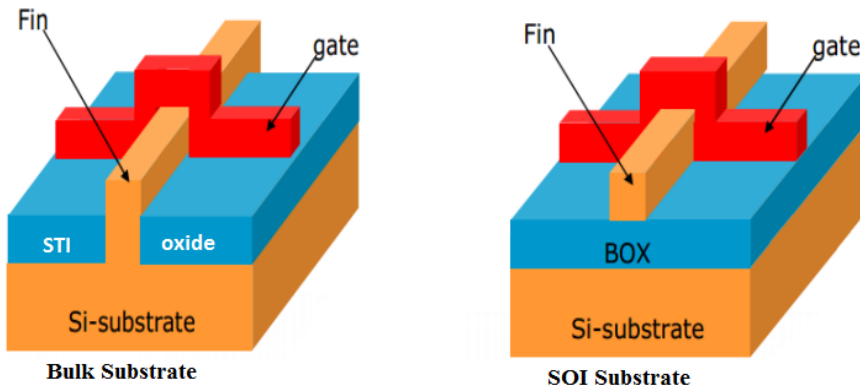
FinFET devices can be fabricated on conventional bulk or in silicon on insulator (SOI) substrates, as illustrated in Figure 2.5. In bulk FinFETs, all fins share a common silicon substrate, and the Shallow Trench Isolation (STI) oxide provides the insulation between the adjacent fins (BHATTACHARYA; JHA, 2014). On the other hand, the SOI FinFET has a thin layer of oxide ( $SiO_2$ ), and the devices are manufactured on the top of the buried oxide (BOX). Bulk FinFETs present a set of benefits such as less expansive wafers, low defect density, less back-gate bias effect, better immunity to heat transfer problems, low NBTI stress, and similarity with the planar fabrication processes (POLJAK; JOVANOVIC; SULIGOJ, 2008) (AUTRAN; MUNTEANU, 2015). The disadvantage is the fin formation that happens by a timed etch process more prone to process variations. Moreover, this kind of substrate requires stronger doping that impact on the leakage currents causing mobility degradation. In SOI FinFETs, the fin structure is formed through a natural process, which stops when it reaches the buried oxide layer, reducing the impact of process variations (SWINNEN; DUNCAN, 2013). Furthermore, SOI substrates minimize parasitic capacitances and improve the current drive, circuit speed, and power consumption (COLLINGE, 2008).

Figure 2.3: FinFET devices with different gate configurations: shorted-gate and independent-gate



Source: Adapted from (SIMSIR; BHOJ; JHA, 2010)

Figure 2.4: FinFETs fabricated with different substrates: bulk and SOI



Source: Adapted from (CONLEY, 2014)

## 2.2. General Background of FinFET Technology

The idea of transistors with multiple gates to attenuate the SCE was first announced by Sekigawa and Hayashi in 1984 (SEKIGAWA; HAYASHI, 1984). Some years later, a novel multigate device called DELTA with vertical ultra-thin structure provided better channel controllability, higher transconductance, and minimized subthreshold swing (HISAMOTO et al., 1989). The first FinFET with an SOI substrate was investigated in (HISAMOTO et al., 2000). They observed that for reducing the parasitic resistances, the devices need to be self-aligned to each other and with the source/drain terminals. The first experimental evidence using FinFET devices was a

four-stage inverter chain (RAINEY et al., 2002), and a static random-access memory (SRAM) cell (NOWAK et al., 2002). Since then, FinFET devices have been widely explored in the last decades.

The benefits in adopting FinFET devices to keep scaling and the comparison between MOSFET and multigate structures were discussed in (FRANK et al., 2001) (SOLOMON et al., 2003) (NOWAK et al., 2004) (SKOTNICKI et al., 2005) (HU, 2011) (KUHN, 2011) (DORIS, 2013). An explanation about the improvements of SCE in FinFET devices over traditional MOSFETs can be encountered in (HISAMOTO et al., 2000) (TANG et al., 2001) (YU et al., 2002) (SAIRAM et al., 2007) (GU et al., 2008). The circuit design considerations for FinFETs and how it impacts on performance, power consumption and area were explored in (KING, 2005) (ZHAO; CAO, 2006) (COLINGE, 2008) (MISHRA; MUTTREJA; JHA, 2011) (BHATTACHARYA; JHA, 2014). The electrical device characteristics such as threshold voltage analysis,  $I_D \times V_G$  curves, power and performance estimates were done in (ROY et al., 2005) (TRIVEDI et al., 2007) (GUILLORN et al., 2008) (CHANG et al., 2011) (BOUKORTT et al., 2016).

The advantages and drawbacks of SG and IG FinFET devices can be encountered in (SUBRAMANIANA et al., 2005) (AMBACQ et al., 2006) (BORREMANS et al., 2008). Novel circuit styles using SG and IG FinFETs for low-power design and leakage current suppression were studied in (WEIMIN et al., 2005) (MUTTREJA; AGARWAL; JHA, 2007) (AGOSTINELLI et al., 2009) (ROSTAMI; MOHANRAM, 2011). Sizing techniques to improve performance, area and power consumption in FinFET circuits were evaluated in (SWAHN; HASSOUN, 2006) (GU et al., 2008) (POSSER et al., 2014). Some geometric restrictions imposed by standard cell methodologies were presented in (ALIOTO, 2010) (ZHANG; PAN, 2012) (CHAUDHURI; MISHRA; JHA, 2012) (KLEEBERGER; GRAEB; SCHLICHTMANN, 2013).

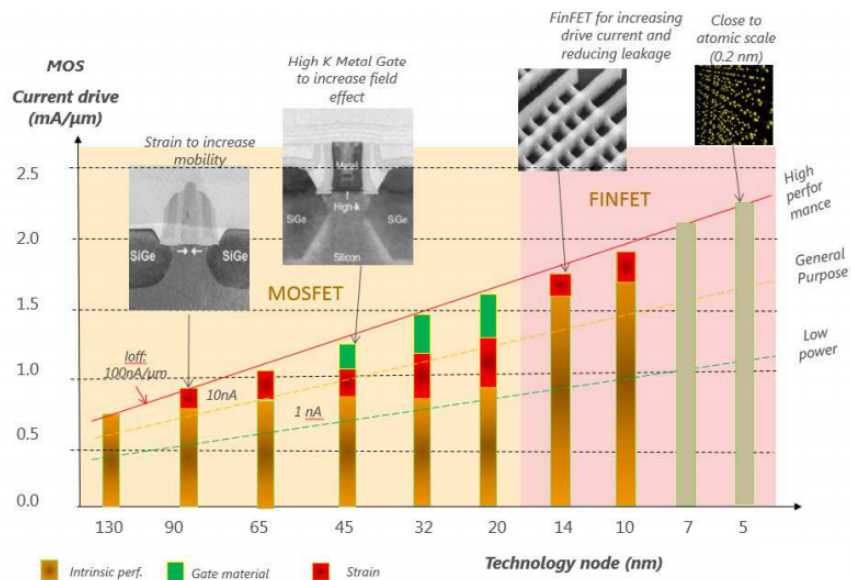
Sequential circuits and SRAM memories occupy a large fraction of the chip area in most of the designs. The behavior of them when adopting FinFET technologies were analyzed in (GUO et al., 2005) (JOSHI et al., 2010) (KANG et al., 2010) (ENDO et al., 2011) (SACHID; HU, 2012). The behavior of the FinFET digital circuits under aging effects such as BTI and HCI was investigated in (WANG; COTOFANA; LIANG, 2012) (KHALID; MASTRANDREA; OLIVIERI, 2015) (RAMEY et al., 2015) (SOOTKANEUNG; HOWIMANPORN; CHOOKAEW, 2017) (HUANG et al., 2018) (HSU et al., 2018).



## 2.3. The Advancement in the Semiconductor Industry

In 1965, Gordon E. Moore proposed the Moore's Law. He predicted that the number of transistors on a chip doubles every two years with the same cost and improvements in the transistor performance (MOORE, 1965). Until now, the semiconductor industry adopts this prediction as a guide and from it set targets for research and development. Figure 2.6 illustrates the advancement of the nanometer regime as well as some techniques and materials used to keep scaling over the last few years. The high price of research, development, and manufacturing equipment led to a reduction in the number of semiconductor industries investing in advanced technological nodes. As an example, the GlobalFoundries recently decided to stop the design of chips at 7-nm FinFET technology. Nowadays, the race for more compact and technological chips happens mainly among the Intel, Samsung, and TSMC companies (HIBBEN, 2018).

Figure 2.6: Advancements of the nanometer regime in the last few years



Source: (SICARD, 2017)

The Intel Corporation was the first company to produce microprocessors using FinFET technology (AUTH, 2012). Both mobile models as the desktop processors adopted the 22-nm node and became available in the market in 2012. Ivy Bridge is the name used to represent all

the first generation of Intel Core processors based on FinFET technology. Other semiconductor industries introduced FinFET circuits in the market since 2014.

TSMC started the volume production of 16-nm FinFET node in 2014, obtaining circuits 50% faster, with 60% less power consumption. Shortly after, Intel introduced the 14-nm FinFET node. Compared with the first node, the fins of transistors are taller, thinner, and more closely spaced for improving the density, and decrease capacitances (SEIFERT et al., 2015). Still, in 2014, the Exynos7 was introduced in the market as the first mobile processor developed by Samsung on 14-nm FinFET technology offering about 20% more performance, and 35% power reduction than existing nodes.

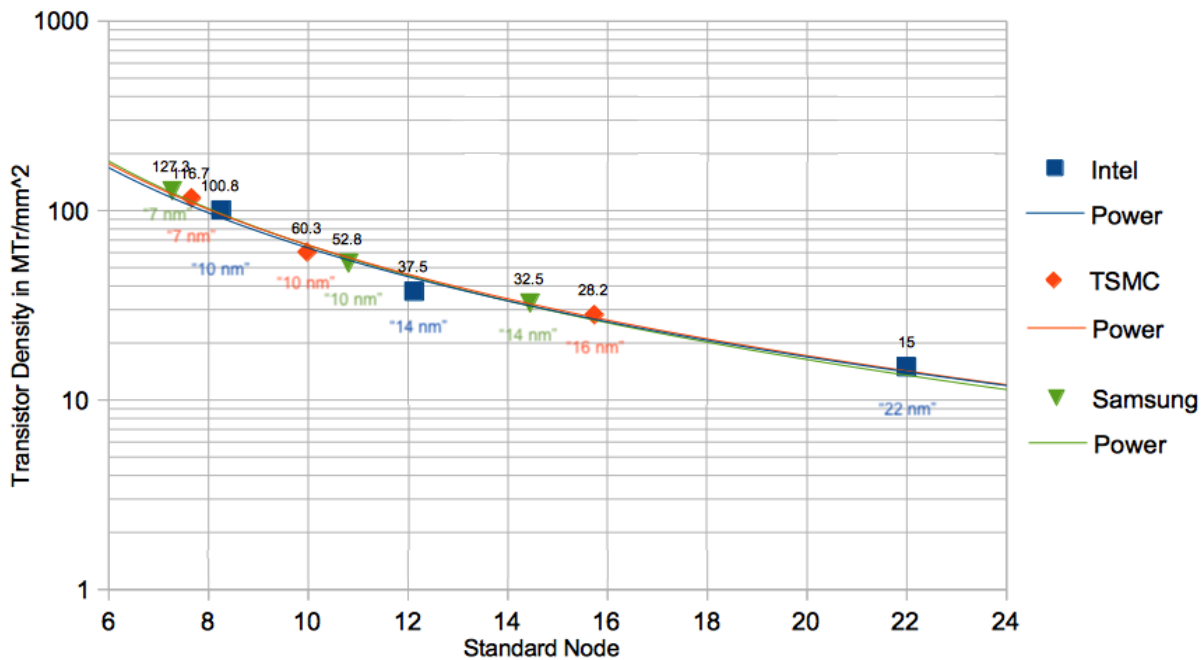
In 2016, Samsung, Intel, and TSMC announced the 10-nm FinFET node in the consumer market. Samsung devices improved 30% the area efficiency increasing the performance by 27% and reducing the power consumption by 40% (SAMSUNG, 2017). Intel Corporation presented circuits with 25% better performance and 45% lower power consumption (INTEL, 2017). For TSMC, the new node provided an improvement of 2X logic density along with 15% faster speed and 35% less power consumption. In 2017, the second generation of the 10-nm FinFET nodes with even more benefits was made available by Intel and Samsung.

The mass production of 7-nm devices began in 2018. The TSMC launched 7-nm devices for mobile and also for high-performance computing applications with improvements of 1.6X logic density, 20% of higher speed and 40% of power reduction. In October, Samsung announced the beginning of wafer production using the 7-nm process using multiple patterning for selected layers. This technology enables a 40% area reduction along with 50% lower power and 20% higher performance when compared to the 10-nm process. For technology nodes below 10-nm, the most important metric is the transistor density. Thus, the 7-nm process offered by Samsung and TSMC is roughly equivalent to the 10-nm provided by Intel (ED SPERLING, 2017). Figure 2.7 reinforces this statement and illustrates the transistor density comparison between the three more relevant semiconductor industries.

In 2019, Samsung informed that a 5-nm FinFET technology is ready for customer's samples. This node reduces the mask layers presenting 25% logic area efficiency, and 20% lower power or 10% higher performance. TSMC has plans to start the risk production in 5-nm FinFET node at

the end of 2019, and the mass production in 2020. However, the scaling benefits are questionable for these 5-nm FinFET nodes. They are considered half-nodes because they do not provide the double density and significant improvements in power and performance metrics.

Figure 2.7: Transistor density regarding the technology scaling in commercial FinFET technologies



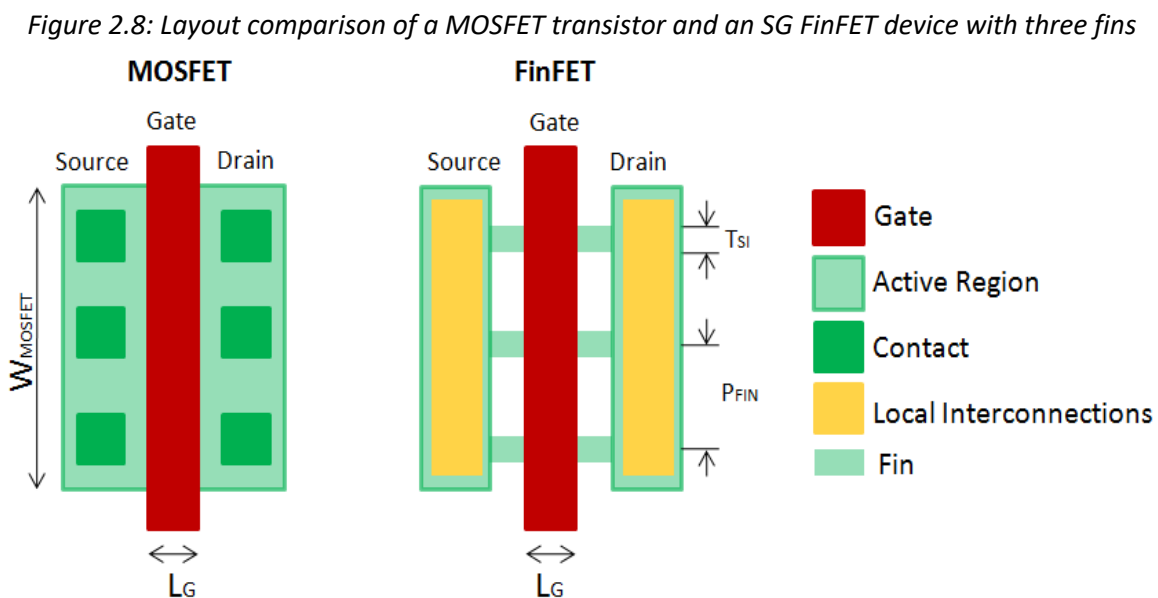
Source: Adapted from (HIBBEN, 2018)

According to the consumer’s point of view, they wish a product that offers better performance for the lowest price with a reliable roadmap for future generations. For chips to get denser, the chipmakers have two options: try to extend FinFETs to 3-nm or migrate to gate-all-around (GAA) devices. The thinner geometric patterns imposed to each new FinFET node increase the probability of phenomenon like LER and MGG that modifies the ideal shape and features of the transistor channel preventing the transistors from working as desired. The deviation in the structure due to the process variability impacts mainly the performance of a transistor. For this reason, to continue the scaling with FinFET devices, it is necessary to mitigate the effects of process variability or to find a performance booster able to control the weak electrostatic of the channel.

On the other hand, the adoption of GAA devices implies in technical and cost challenges. The manufacturing process of these devices requires an extra step that involves extreme ultraviolet lithography (EUV) with a high level of complexity and multiple reliability issues. However, the implementation demands huge funding putting the technology out of reach for many consumer applications. With all these drawbacks in mind, the introduction of another node or the switching to an alternative device may be delayed beyond the target date of 2021. But the fewer modifications required the fewer problems that potentially can affect yield and time to market.

## 2.4. Layout Design using FinFET Devices

In general, the essential difference in the FinFET manufacturing process is the existence of fins. However, from a physical point of view, the procedure of fin formation is not a trivial task and requires high aspect ratio etches and higher stress for mobility enhancements imposing challenges in the design (KAWA, 2012). Figure 2.8 highlights the differences between the layout of a transistor designed using MOSFET and FinFET technologies.



Source: Adapted from (CUI et al., 2014)

In FinFET layouts, the conducting channel between the source and drain terminals is formed through the fins with local interconnect layers. The area occupied by fins in an SG FinFET device is given by Equation 2.4

$$A_{FIN} = (N_{FIN} - 1) \cdot P_{FIN} \quad (2.4)$$

where  $P_{FIN}$  is the fin pitch, which corresponds to the distance between the middle section of two parallel fins. The disadvantage at the layout level for IG FinFET devices is the area needed for placing the two separated contacts of the gates. Hereafter, some experimental results are presented exploring the fundamental concepts of FinFETs at the layout level as well as methods to improve the layout density.

According to Equation 2.4, there are two ways to improve the FinFET transistor area: reducing the fin pitch or the number of fins. The fin pitch can be defined through the lithography-defined and spacer-defined methodologies (ANIL, 2003) (ALIOTO, 2010). In the first case, the minimum value of the fin pitch is set by the adopted technology node. Otherwise, in spacer-defined technique, the fin pitch can be halved due to an additional lithography step. The replacement of  $W_{MIN}$  by  $2 \cdot H_{FIN}$  in Equation 2.3 indicates that the number of fins can be reduced by increasing the fin height. However, the increase of  $H_{FIN}$  is restricted due to practical considerations. The acceptable ratio of  $H_{FIN}/T_{SI}$  in FinFETs should be around 2 (COLLINGE, 2008).

Datta et al. (2007) presented the layout of an inverter with the IG model to estimate the area occupied of a 4T device considering a 45-nm technology node. They represent the area of the cell concerning the minimum spacing requirement ( $\lambda$ ) proposed by Nowak et al. (2004). The area of inverter suffers an increase of 9.1% with IG structure due to the additional back-gate contact. Similar area penalty can also be observed in the NAND2 and NOR2 logic cells. However, in merged cells, the reduction in the number of transistors provoked an area contraction when compared to SG devices mainly in low-power circuit design. For ISCAS85 benchmark circuits, the IG devices obtained around 8.5% of area economy and 18% of power-saving over the SG structure with no performance penalty.

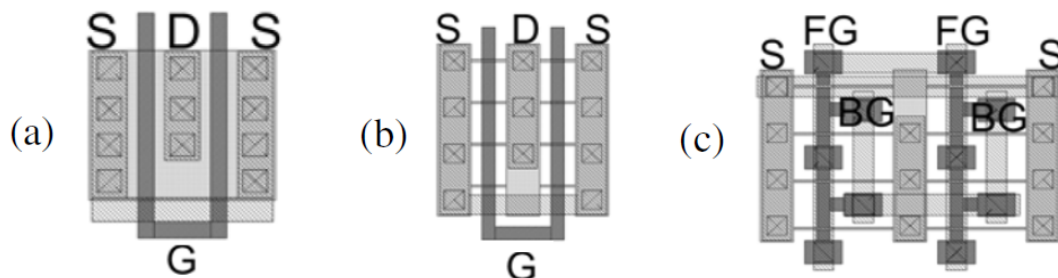
Kumar and Kirubaraj (2010) investigated four FinFET logic design styles such as shorted-gate, independent-gate, low-power (LP) and hybrid (IG/LP) for a NAND2 cell. Moreover, rectangular

and fin-shaped diffusion approaches were considered for all FinFET modes presented above. Power dissipation and performance were analyzed for each design style considering different supply voltages. The results were compared with the NAND2 cell implemented using traditional planar technology. In general, they conclude that power dissipation is smaller in the FinFETs logic design and even better when a fin-shaped diffusion is used. However, the average delay of all design styles using FinFET devices is more prominent than traditional planar technologies.

Alioto (2010) compared the lithography-defined and spacer-defined methods in 3T devices and the dependence of layout density with the fin height considering geometric constraints imposed by the standard cell library. The layout density of FinFET is better than planar CMOS even for moderately tall fins. The lithography-defined (spacer-defined) FinFET cells exhibits an average area reduction by a factor of  $0.95/0.58 = 1.64$  ( $0.68/0.52 = 1.31$ ) when increasing  $H_{FIN}$  from  $T_{SI}$  to  $4T_{SI}$ . Hence, fin height is considered a powerful knob to improve the layout density in FinFET cells.

Alioto (2011) compared the layout density of 3T, 4T, and mixed 3T-4T FinFET devices. His results demonstrated that 3T and MT devices in standard cell format have the same layout density compared to planar CMOS cells for low values of fin height. The results were even better when moderate fin height was applied. Instead, 4T devices have an unfavorable layout density due to the separated contacts of the front and back-gates. Hence, the fin pitch must be higher than the minimum value allowed by the technology. The multi-finger layout structure used to implement very wide transistors also was evaluated. The two-finger 3T transistor has a 15% lower area ratio compared with the traditional devices with  $H_{FIN}/T_{SI} = 2$ . Figure 2.9 shows the two-finger structure for planar CMOS, 3T, and 4T FinFET layouts.

Figure 2.9: Two-finger structure for (a) bulk CMOS devices, (b) 3T FinFET devices and (c) 4T FinFET devices

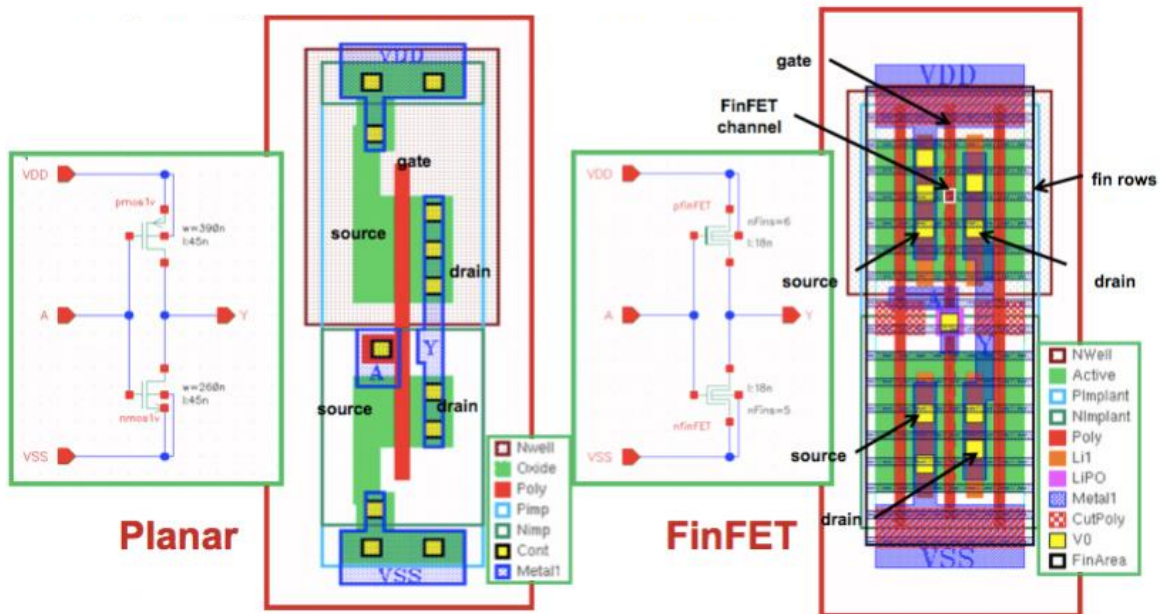


Source: (ALIOTO, 2011)

Wimer (2012) proposed an algorithm for converting planar transistors in multigate devices maximizing the number of fins in the target cell. This algorithm is also applicable from multigate source layout to multigate target layout for future technology nodes. He used a hard-IP reuse technique to ensure the migration of a physical layout of an existing chip into a new target technology with the same functionality and preserving all layout design rules. The place and route maintain the relative positions as in the source layout. The conversion flow has been successfully tested on full adders and sequential circuits.

McLellan (2014) presented a detailed comparison between the layout of an inverter designed in planar CMOS and FinFET technologies, as shown in Figure 2.10. The transistors have a number of fins equal to five. The FinFET design is composed of rows of source/drain with gate strips orthogonally. Single gates usually violate the design rules of FinFET technologies. Thus, the FinFET inverter has three gates (red) because every transistor must be finished with dummy gates on either side. It is not possible to cut off the diffusion by just ending the polygon as in the planar devices. The red hashed area in the middle of the FinFET inverter is the cut mask that separates the PFET and NFET transistors.

Figure 2.10: Planar to FinFET layout differences



Source: (McLELLAN, 2014)

Cui et al. (2014) built a standard cell library in 7-nm FinFET technology, choosing an adequate number of fins for the complementary networks of all logic cells. The standard cell library contains ten combinational logic cells with different drive strengths and three sequential logic cells activated on the positive-edge. The  $\lambda$ -based layout design represents the characterization of each cell with the same height. The power density report was made, including near-threshold and super-threshold operation for different ISCAS benchmarks. Results show that the power density of each 7-nm FinFET circuit is at least 10 to 20 times larger than the same circuit in 45-nm planar CMOS technology. Therefore, they conclude that careful thermal management is necessary for the FinFET technology nodes.

## **2.5 FinFET Predictive Models**

### **2.5.1. Technology models for SPICE simulations**

With the continuous advancement of technology, predictive models are essential in circuit designs to identify design requirements, explore challenges and possible solutions (SINHA et al., 2012). The basic idea is to consider previous results to develop a representative model that can be used to predict future outcomes. Multigate transistors have been extensively evaluated through TCAD simulation tools providing high precision. However, the simulation time for VLSI circuits can be huge. Electrical models for SPICE simulations require shorter computational time compared to 3D models, providing an alternative to aid circuit designers (MEINHARDT, 2014).

Some predictive models based on SPICE simulations were developed for FinFET technologies (ZHAO; CAO, 2006) (ZHANG, 2014). However, these models do not represent an accurate behavior of the transistors needing some adjustments to be widely adopted. In 2012, a new generation of predictive technology model (PTM) for FinFET devices in sub-20nm technology nodes called PTM-MG was developed by Arizona State University (ASU) (SINHA et al., 2012) (PTM, 2018). These models provide high-performance (HP) and low standby power (LSTP) versions, where the main difference is the threshold voltage adopted. The flow to generate the predictive models was based on Technology Computer-Aided Design (TCAD) model where the main parameters were scaled considering the ITRS trends. The reference values of geometric parameters and doping information for a set of predictive nodes from PTM are shown in Table 2.1. The main disadvantage of PTM is not allowing the simulation of



FinFETs in the IG structure. Another model based on PTM-MG was proposed to fill this gap allowing the circuit simulation with different voltage in the front-gate and back-gate terminals (ZAREI, 2013).

In 2016, another predictive model called ASAP7 developed by ASU in partnership with ARM Ltd became available to estimate the trends of the 7-nm FinFET technology (CLARK et al., 2016). This model is considered more accurate than the previous one because it considers realistic conjectures from the semiconductor industry. The ASAP7 provides the typical (TT), fast-fast (FF) and slow-slow (SS) process models for the designers. However, the FF and SS models affect the  $I_{ON}/I_{OFF}$  currents considerably. Table 2.2 shows a summary of the main geometric parameters and the doping characteristics in the simulations using the ASAP7 model.

Table 2.1: Geometric parameters and doping information of PTM-MG models

Parameters		20-nm	16-nm	14-nm	10-nm	7-nm	
Supply voltage (V)		0.90	0.85	0.80	0.75	0.70	
Gate length(nm)		24	20	18	14	11	
Fin height (nm)		28	26	23	21	18	
Fin thickness (nm)		15	12	10	8	6.5	
Oxide thickness (nm)		1.40	1.35	1.30	1.20	1.15	
Channel Doping ( $m^{-3}$ )		$5 \times 10^{23}$	$1 \times 10^{23}$	$5 \times 10^{22}$	$2.5 \times 10^{22}$	$1 \times 10^{22}$	
Source-Drain Doping ( $m^{-3}$ )		$3 \times 10^{26}$	$3 \times 10^{26}$	$3 \times 10^{26}$	$3 \times 10^{26}$	$3 \times 10^{26}$	
Work-function (eV)	HP	NFET	4.38	4.41	4.42	4.42	4.42
		PFET	4.80	4.76	4.75	4.75	4.74
	LSTP	NFET	4.56	4.58	4.60	4.60	4.61
		PFET	4.62	4.59	4.57	4.56	4.56

Source: (SINHA et al., 2012)

Table 2.2: Geometric parameters and doping information of ASAP7 models

Parameters	TT	FF	SS
Supply voltage (V)	0.7		
Gate length (nm)	21		
Fin height (nm)	32	34	30
Fin thickness (nm)	6.5	7	6
Oxide thickness (nm)	2.1		
Channel Doping ( $m^{-3}$ )	$1 \times 10^{22}$		
Source-Drain Doping ( $m^{-3}$ )	$2 \times 10^{26}$		
Work-function (eV)	NFET	4.37	
	PFET	4.81	

Source: (CLARK et al., 2016)

Both PTM and ASAP7 models allow the simulation of different FinFET structures (double-gate, triple-gate or quadruple-gate) as well as the substrate mode (bulk or SOI). For this, it is necessary to set the *geomode* and *bulkmode* parameters correctly in the technology file according to Table 2.3.

Table 2.3: Setup for different structures and substrate

	<i>Geomode</i>	<i>Bulkmode</i>
0	Double-gate	SOI
1	Triple-gate	Bulk
2	Quadruple-gate	-

Source: (CHAUHAN et al., 2015)

## 2.5.2 Process Design Kit (PDK)

The FinFET PDK, cell libraries, and design flow used by the semiconductor industries are not available for academic use. In this way, the North Carolina State University (NCSU) and the ASU in collaboration with ARM Ltd proposed free and predictive PDKs exploring the 15-nm and 7-nm nodes, respectively (BHANUSHALI; DAVIS, 2015) (CLARK et al., 2016). Both PDKs are not tied to any specific foundry. This thesis focuses on the ASAP7 PDK because it allows design exploration at the 7-nm node that is the current technology used in the manufacturing process of the largest semiconductor industries. Moreover, the developers considered realistic design conjectures regarding lithography steps and the current technology competencies of commercial nodes. Table 2.4 shows a summary of the widths and pitches beside the kind of lithography adopted for all layers from ASAP7 PDK.

The lithography step uses ultra-violet light to transfer the geometric patterns to the thin wafers of silicon. FinFET technologies tried to adopt single exposure (SE) and extreme ultra-violet (EUV) for all layers to provide simple and cost-effectiveness designs. However, the wavelength has not kept pace with the device scaling, introducing challenges to print the small standards required when the technology nodes reach to 14-nm and beyond (RIEGER, 2012). Multiple patterning (MP) is the method used to overcome some lithography limitations and ensure enough resolution in the manufacturing process (LI; LIU, 2016). Different types of multiple patterning can be requested, depending on the circumstances. The implementation of MP can be through double, or quadruple patterning. Double patterning involves two lithographic exposures and etches steps processed separately where the final shapes are combined at the end to create a single layer (GHAI DA et al., 2013). The litho-etch-litho-etch (LELE) and self-aligned double-patterning (SADP) are the most common ways to implements the double patterning. The SADP has a significant advantage in the overlay tolerance if compared with LELE. The

self-aligned quadruple patterning (SAQP) is a natural extension of SADP such that the only difference is one more step of spacer deposition (DING; CHU; MAK, 2015). Intel and TSMC already incorporated the SAQP methodology in their most recent technology nodes.

*Table 2.4: Key layer lithography assumptions, widths, and pitches*

Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54 <sup>b</sup>
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25 <sup>a</sup>
M1-M3	EUV	18/18	36
M4-M5	SADP	24/24	48
VIA4-VIA5	LELE	24/24	34 <sup>a</sup>
M6-M7	SADP	32/32	64
VIA6-VIA7	LELE	32/32	45 <sup>a</sup>
M8-M9	SE	40/40	80
VIA8	SE	40/40	57 <sup>a</sup>

<sup>a</sup> Corner to corner spacing as drawn      <sup>b</sup> horizontal only

Source: (CLARK et al., 2016)

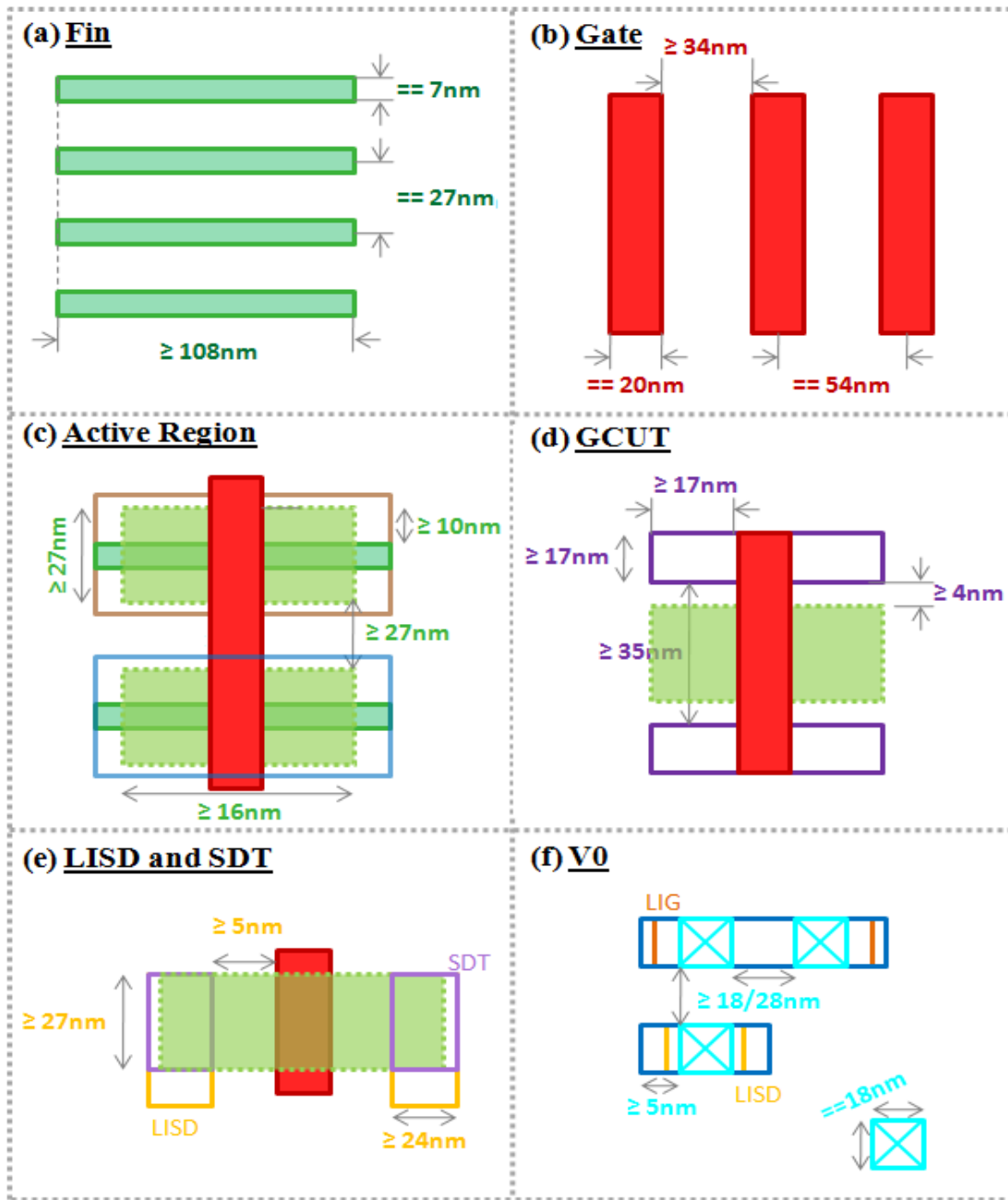
The manufacturing process of FinFET technologies is divided into three categories: front-end-of-line (FEOL), middle-of-line (MOL) and back-end-of-line (BEOL). The first group includes the production of wells and transistors, with the essential elements as the active region, fins, gate, and diffusions. The BEOL considers the contacts by via layer and the metallic layers from metal 1 (M1) to the top metal (M9). This stage is responsible for short connections and overall cell routing. The connection between FEOL and BEOL steps happen in the MOL stage. For example, the source-drain trench (SDT) layer connects the active area to the local interconnect source-drain (LISD) layer as well as the LISD joins the source and drain terminals of transistors. LISD is above SDT in the MOL stack. The local interconnect gate (LIG) is used for the contacts of the gate terminal. The purpose of V0 is to join the LIG and LISD to the BEOL layers.

Figure 2.11 shows the basic design rules of ASAP7 PDK. There is a set of details to be considered in the FinFET layout design. The fins need to be uniformly aligned respecting the fixed fin pitch, and the exact vertical fin width. Moreover, all fin layer polygons should have an equal length along the horizontal axis, and they cannot be bended. The FinFET fabrication process uses two dummy gates at each end of the cells, not allowing single gates in the design. The gate layer with bends is also not supported. Each gate must have an exact fin pitch and a fixed horizontal gate width. All gate polygons must have an equal vertical length if they are not cut by GCUT. The vertical edge of the GCUT layer cannot lie inside or coincide with the gate layer, and it also cannot interact with the active region. The GCUT layer cannot exist without the gate layer.

The n- or p-select must always enclose the active region. The horizontal distance between two active areas varies if the diffusions have different or equal voltages. The SDT layer must always be inside the LISD layer, and it cannot be entirely outside of the active region. V0 should exactly be the same width as the M1 layer, and it needs to be uniformly aligned for all vertical and horizontal directions. V0 must always interact with M1 layers and LISD/LIG. Moreover, this PDK requires a TAP cell in all layout designs to ensure proper functionality of circuits. The TAP cell is responsible for connecting the back-gate of FinFET transistors. For FinFETs designed in an SG model, the back-gate has the same signal of the front-gate.

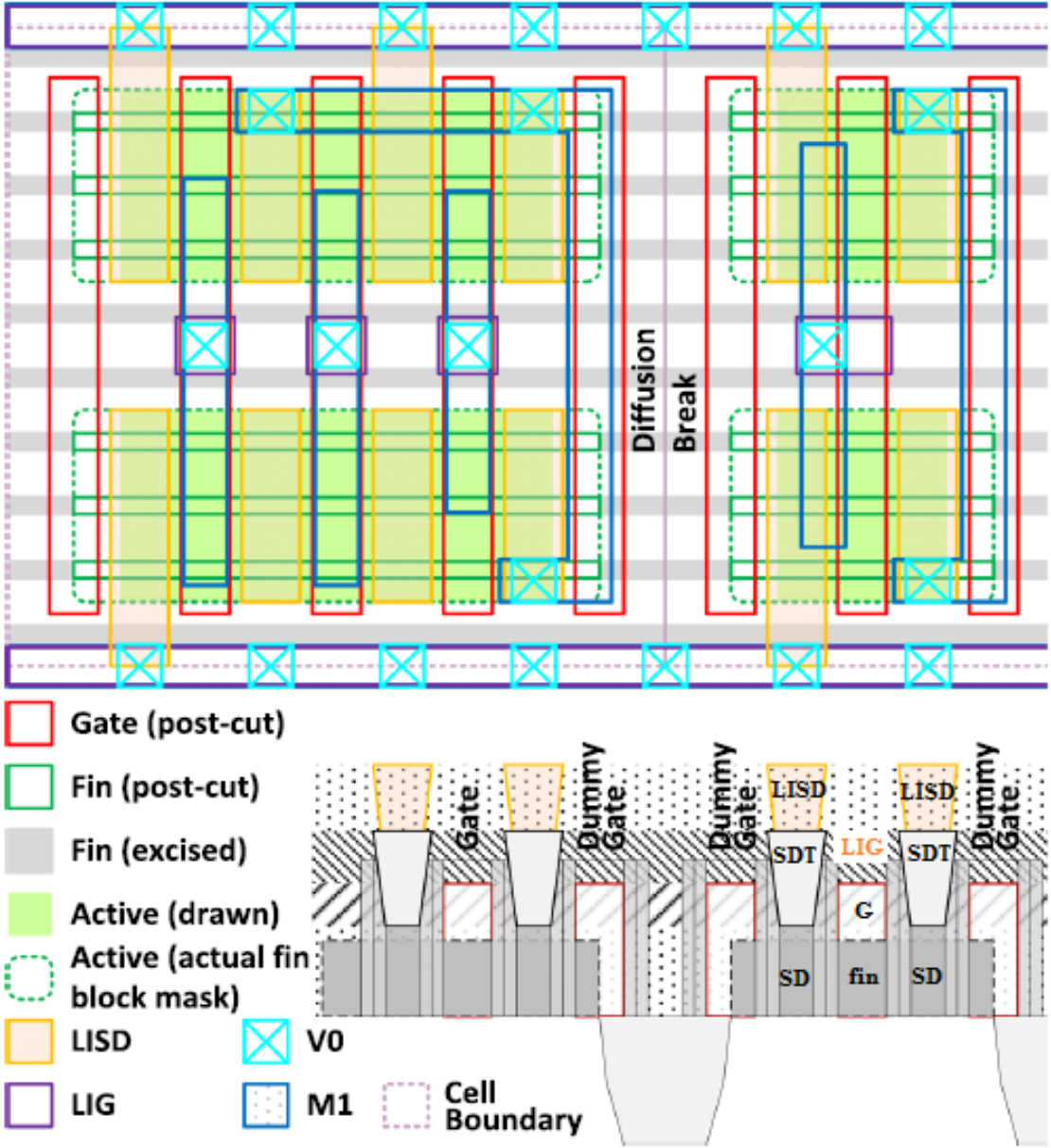
For exemplifying all information presented in this sub-section, Figure 2.12 shows the layout of a NAND3 and an inverter based on the standard cell template using the design rules from ASAP7 PDK. Although the layout presents ten fins along the vertical axis, the transistors have only three fins. The excised fins rails represented in light gray, two between the active regions and two near to power, are necessary due to constraints imposed by FinFET technologies, but they are not taken into account for the transistor sizing. The diffusions are connected using M1 and V0 contacts. As there is a diffusion break, active regions of each cell require a gate at either side (dummy gates). On the bottom of Figure 2.12, the cross-section view of cells is presented with detailed information about FEOL, MOL, and BEOL steps.

Figure 2.11: Basic design rules of ASAP7 process design kit



Source: From the author

Figure 2.12: The NAND3 and an inverter designed in the 7-nm FinFET technology on the standard cell template



Source: Adapted from (CLARK et al., 2016)

# Chapter 3: FinFET Technology Challenges

---

This chapter introduces the main reliability challenges in FinFET technologies and the consequences of them in the integrated circuits. Moreover, the most relevant state-of-the-art works are presented, with a focus on evaluating or attenuating the reliability challenges in nanometer technologies. Four circuit-level techniques to mitigate the effects caused by process variability and radiation-induced soft errors also are discussed in this chapter.

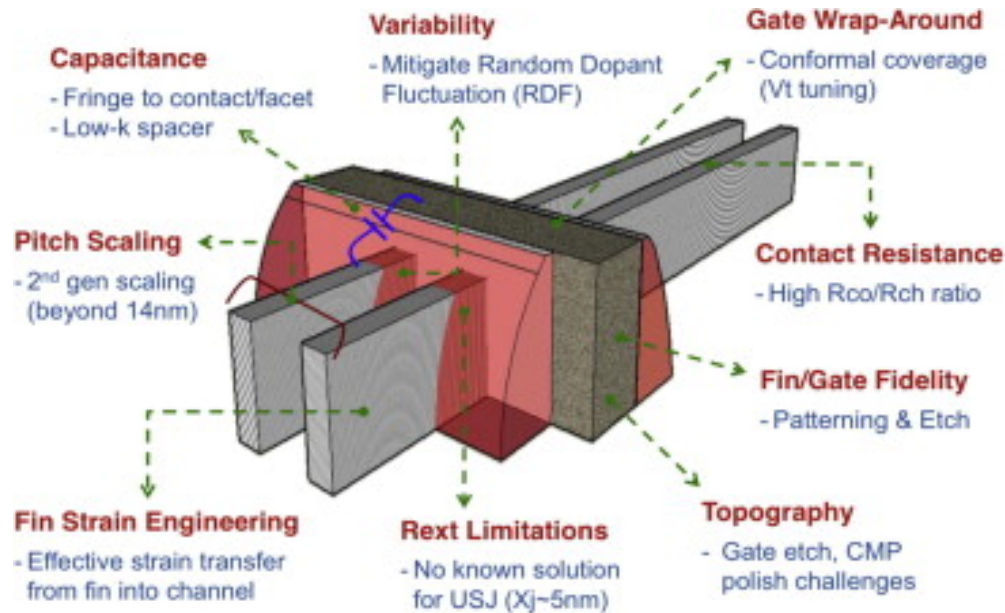
The technology scaling regarding the adoption of FinFET devices brought several benefits, but some challenges also were introduced. The quantization feature to increase the transistor width imposed restrictions at the layout level because the circuits need to be always designed into a grid reducing the design flexibility. FinFET devices require a careful resistances and capacitances modeling with satisfactory tools to realize the RC extraction, avoiding inappropriate device characterization and circuit performance degradation. The Miller effect influences the reliability of the circuit and reinforces the need for power and timing analysis accurately (McLELLAN, 2014). Moreover, the circuits become more susceptible to transient faults coming from space and terrestrial radiations, and also to permanent events.

Examples of most common FinFET problems are shown in Figure 3.1 such as the fringe capacitance to contact/facet, low-k spacer, fin/gate fidelity, contact resistances, chemical-mechanical planarization (CMP) polish, threshold voltage tuning, susceptibility to process variability, quantization feature to transistor sizing and the surface orientation (HENDERSON, 2013). All these factors raise essential topics related to the reliability of electronic systems that need to be better investigated.

According to Borkar (2009), the reliability in FinFET technologies can be divided into static and dynamic sources, as Figure 3.2 illustrates. Static sources are usually random, permanent in time, and immediately noticeable after the manufacturing process. Examples of static variation sources are random dopant fluctuation (RDF), line edge roughness (LER), and metal gate granularity (MGG). On the other hand, dynamic sources are time-varying suffering modifications according to operating conditions like temperature oscillation, supply voltage

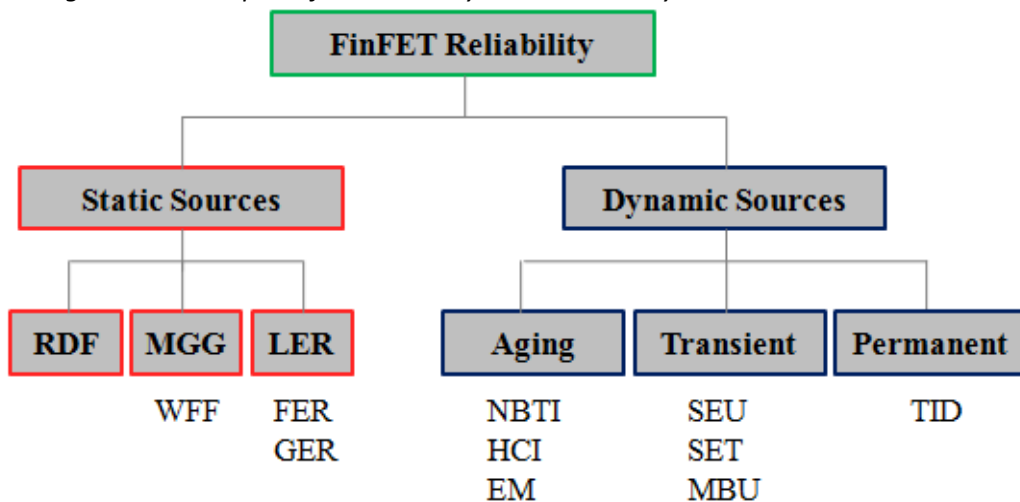
drop, switching activity, environmental noise, and radiation exposure. Examples of dynamic sources are the aging effects (e.g., Bias Temperature Instability (BTI), Hot-Carrier Injection (HCI), Electromigration (EM)), transient faults (e.g., Single Event Upset (SEU), Single Event Transient (SET), Multiple Bit Upset (MBU)), and permanent events (e.g., Total Ionizing Dose (TID)).

Figure 3.1: Some challenges for FinFET technologies



Source: (HENDERSON, 2013)

Figure 3.2: Examples of static and dynamic variability sources in FinFET devices



Source: From the author



Currently, process variability and radiation-induced soft errors are considered the major reliability challenges for commercial electronic systems manufactured in FinFET technologies. From a design standpoint, considerable efforts should be made to reduce the impacts introduced by these issues (SAHA, 2010) (NSENGIYUMVA et al., 2017). In this way, this thesis focuses on evaluating a set of FinFET logic cells under process variability and soft errors as well as propose potential reliability-oriented approaches to mitigate the effects caused by them. The next sub-sections are dedicated to explaining in detail these topics.

### 3.1. Process Variability

Variability is related to the random deviation, which causes an increase or decrease of typical design specifications (SAHA, 2010). The main issue associated with variability is the uncertainty about the correct circuit operation because there is no guarantee that a circuit will behave as expected after the manufacturing process. Due to the variability, each circuit can present a different electrical behavior such as abnormal power consumption and performance deviation. The unexpected behavior due to variations can stimulate the circuit degradation besides making it inappropriate for their initial purpose (ORSHANSKY; NASSIF; BONING, 2008). The variability sources can be divided into three main categories: environmental, reliability, and physical (NASSIF, 2008). The first two categories are dynamic (time-varying), while the last one is static occurring during the manufacturing process.

Environmental factors are deviations in the operating conditions during the circuit lifetime due to architectural and operational decisions such as power lines design and cells placement. The most common examples of this category are the oscillations in switching frequency, temperature, supply voltage, and environmental noise. The supply voltage is variable in a chip, and voltage drops occur mainly due to non-zero resistances in the power supply networks (MEINHARDT, 2014). Supply voltage ( $V_{DD}$ ) has a quadratic relationship with dynamic power, according to Equation 3.1,

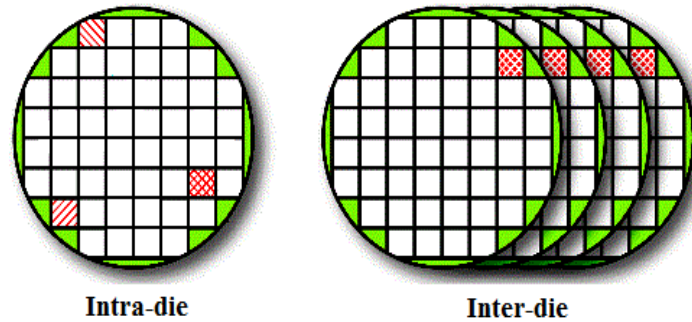
$$P_{\text{dynamic}} = f \cdot C \cdot V_{DD}^2 \quad (3.1)$$

where  $f$  is the switching frequency and  $C$  is the capacitance between the output nodes. This relation becomes an attractive solution for low power applications, but it has to be used carefully because the clock frequency is reduced significantly. Moreover, the supply voltage deviation also affects the propagation delays due to the relation with the transistor saturation current. This association is exponential for a wide voltage range. Temperature oscillations can compromise interconnections and the behavior of electronic components in a chip. Higher heat flux results in higher temperature, creating hot spots, which in turn generate temperature variations across the die. At high temperature, devices may not meet performance requirements due to threshold voltage drift, higher leakage currents, and propagation delay. Moreover, temperature variations across communicating blocks on the same chip may cause logic or functional failures (BORKAR, 2009). However, the structure of multigate devices has diminished the thermal conductivity due to the small and confined dimensions of the fin (ZHANG et al., 2016) (KUMAR; RAO, 2016).

Reliability factors are related to the transistor aging due to the raising electrical fields through the oxide thickness presented in modern circuits. NBTI, hot carrier injection (HCI) and electromigration are classical problems in this category. NBTI is a degradation factor that negatively affects the performance and noise margins because the electrical fields generate interface traps in p-type devices which results in the unwanted increase in the threshold voltage (KHALID; MASTRANDRE; OLIVIERI, 2015). HCI is another degradation mechanism, and it arises from the heating inside the channel during the circuit operation. Electromigration causes shorts and opens in metal interconnects, leading to interconnection failures decreasing the mean-time to failure (MTTF) of the chip at sub-45nm nodes (POSSER; SAPATNEKAR; REIS, 2017). Physical factors are associated with structural variations after the manufacturing process. They can be classified into inter-die and intra-die variations (MUTLU; RAHMAN, 2005), as shown in Figure 3.3. The inter-die variations are characterized by lot-to-lot, wafer-to-wafer, or die-to-die fluctuations, i.e., the same devices at different wafers are manufactured differently. On the other hand, the intra-die variations are random deviations occurring at distinct locations within the same wafer. Process variability is classified as an intra-die variation that can be originated

from the dopant density or by the small geometric patterns imposed by nanometer technologies.

*Figure 3.3: Intra-die and inter-die variations*

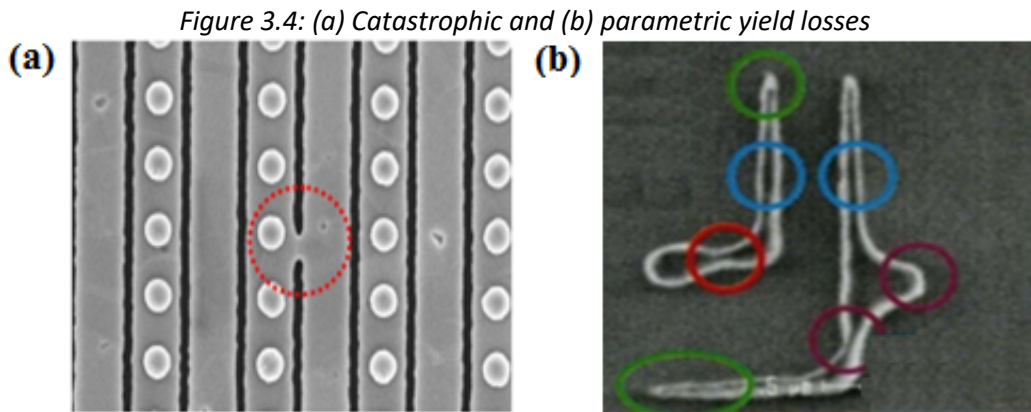


*Source: Adapted from (MENTOR, 2018)*

Integrated circuits with manufacturing defects or deviations from initial specification should be discarded. The yield loss in the semiconductor industry can be divided into catastrophic and parametric (GUPTA; PAPADOPOULOU, 2011). The former is related to functional failures such as open trails or short circuits, which make the circuit does not work correctly. Figure 3.4 (a) shows an example where a bridging fault on metal 3 occurs, changing the behavior of the circuit. On the other hand, the parametric yield loss is caused by process variations where a chip is functionally correct, but it fails to meet some power or performance criteria. Figure 3.5 (b) shows a poly layer with some geometric deviations. The high costs of the manufacturing process are directly related to the variability effects due to the many redesign steps required until the expected behavior is achieved. For example, a chip designed in planar CMOS technology was modified around four times before reaching the production volume (SHERLEKAR, 2004), but this number is more critical for designs that employ sub-22nm technologies.

The manufacturing process introduces the variability at each stage. Once ready, a chip is also susceptible to several natural changes caused by the environment over its lifetime. Environmental factors increase the dynamic variability, as well as the process variations intensify the static variability. In this way, dealing with variability is an increasingly complex problem. The challenges imposed by variability require new design methodologies and new

EDA tools to predict and to minimize their effects on the integrated circuits. Moreover, researches highlight that it is no longer sufficient to focus only on the deviations of the threshold voltage in the design development considering FinFET technologies. Also, it is necessary to evaluate all deviations in the electrical characteristics such as  $I_{ON}/I_{OFF}$  currents, power consumption, and performance.



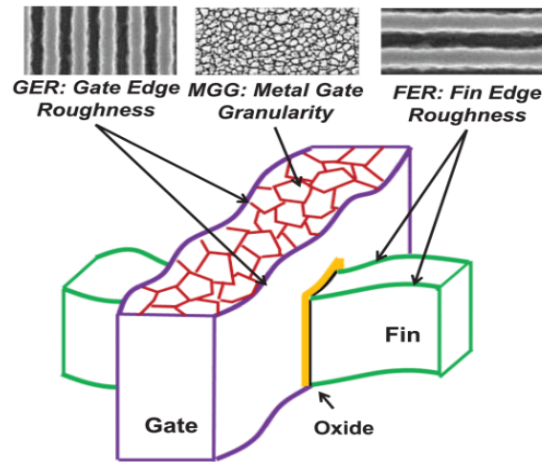
*Source: Adapted from (KLEIN, 2008) and (GUPTA; PAPADOPOULOU, 2011)*

### 3.1.1. Sources of Process Variability

The technology scaling to maintain the pace of performance and density gains results in an increase of design complexity with more potential sources of variability. In this way, technology nodes sub-22nm tend to be more susceptible to process variability effects. The process variability arises from the inaccuracy wavelength used to transfer the small geometric patterns to the wafer, the use of high-k dielectrics to improve the gate control on the channel region or due to the alteration in the doping density.

The most significant sources of process variability are the line edge roughness (LER), metal gate granularity (MGG), and random dopant fluctuation (RDF). The LER can be subdivided in fin edge roughness (FER) and gate edge roughness (GER). Figure 3.5 shows an overview of how and where these sources modify the transistor structure during the manufacturing process. These variations can compromise entire blocks of cells besides reducing the performance and energy efficiency of the chip. The individual contributions of each source are process dependent. The combined effect of them can impact even more the device behavior and the parametric yield loss (AGARWAL et al., 2013). More detailed information about the sources of variability in FinFET devices will be explored in the next subsections.

Figure 3.5: Major random variation sources in FinFETs: GER, MGG, and FER

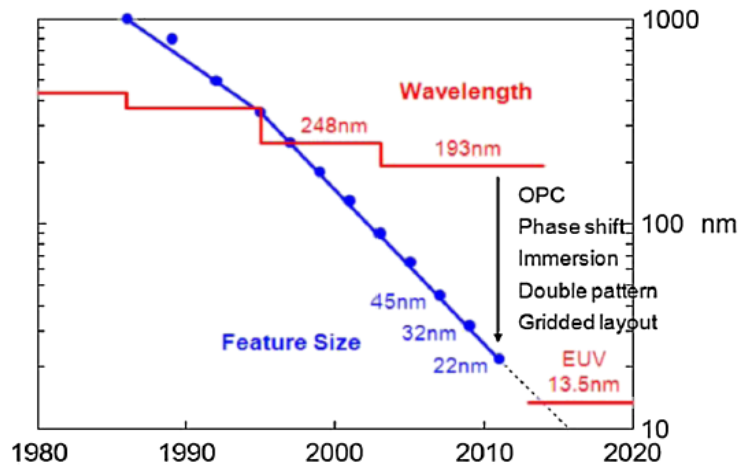


Source: (JIANG et al., 2016)

### 3.1.1.1. Line Edge Roughness

Typically, the lithography step in the fabrication process uses ultraviolet light to transfer geometric shapes to the thin slices of silicon. However, the wavelength is a property of the light source that not kept pace with the devices scaling. The transition of light wavelength from 193nm to 13.5nm is a slow procedure, as shown in Figure 3.6, becoming harder the use of 193nm lithography as chip manufacturing advances more in-depth into the nanometer regime due to the circuit design complexity, increased clock frequency, and edge placement errors (BAKSHI, 2018).

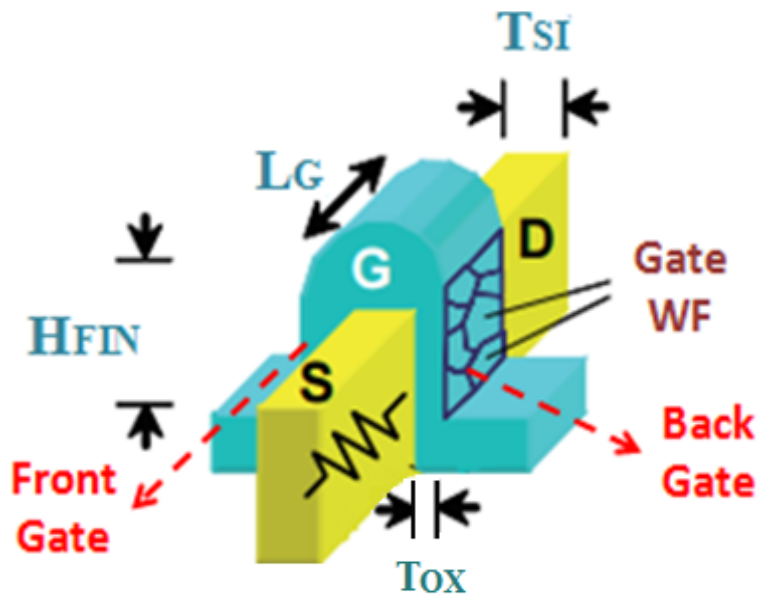
Figure 3.6: Technology scaling and the wavelength adopted in the lithography step



Source: (RIEGER, 2012)

In this way, circuits designed in FinFET technologies are more prone to suffer with LER phenomenon due to the small standards imposed by sub-22nm nodes. Line edge roughness corresponds to a deviation in the transistor edge position if compared with the best fit-line of ideal shape. The imperfections caused by the optical performance loss can influence the fin height ( $H_{FIN}$ ), fin thickness ( $T_{SI}$ ), the gate length ( $L_G$ ) and oxide thickness ( $T_{OX}$ ), as shown in Figure 3.7 (ENDO et al., 2009). The deviations in the gate region are classified as GER while the variations in the fin area are called FER. Gate length, fin thickness, and oxide thickness were pointed as the main sources of threshold voltage variability for FinFET devices (ENDO et al., 2009). FER deviations introduced higher variability on the on-state current since FER affects the channel and also the source/drain resistances (WANG et al., 2011). The impact on  $I_{ON}$  is a little more meaningful when the fin height suffers deviations instead of the fin thickness. The off-state current suffers more deviations when the gate length is modified during the fabrication process (MEINHARDT; ZIMPECK; REIS, 2014a). The impact of oxide thickness variations in FinFET devices can be considered negligible when on- and off-state currents were observed (ZIMPECK; MEINHARDT; REIS, 2014).

Figure 3.7: Geometric parameters for FinFET devices



Source: Adapted from (ENDO et al., 2009)

For reduce the LER, the lithographers use many approaches to bypass the features much smaller than were allowed by the resolution criteria of 193nm lithography such as optical proximity correction. Moreover, some layers replaced the single exposure by multiple patterning methodologies to provide enough resolution in the integrated circuits. Figure 3.8 shows the sub-45nm technology advancement regarding the use of single, double, and quadruple patterning for the main layers. Usually, the fin layers are implemented using quadruple patterning such as SAQP method (CLARK et. al, 2016). The complexity of multiple patterning is because the regular mask is broken up into four incremental mask levels (or two in case of double patterning) where each one of them has process variations which do not correlate with each other. After, it is necessary to align the mask layers of additional exposures accurately on top of each other for better patterning quality, obeying the overlay requirements. Furthermore, multiple patterning methodologies impose new physical verifications at the layout level.

Figure 3.8: Single, double and quadruple patterning applied in the layers of advanced technology nodes

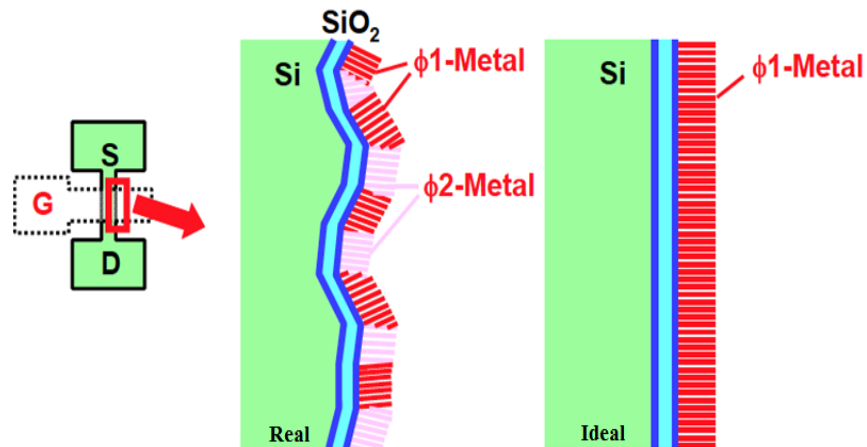


Source: (BRAIN, 2017)

### 3.1.1.2. Metal Gate Granularity

MGG gained prominence since the adoption of high-k dielectrics to improve the gate control on the channel region in sub-45nm technologies. The energy difference between the vacuum level and the Fermi level of a solid is called work-function (WF). The metal WF is the minimum energy required to move an electron from the Fermi level to the vacuum level, and it depends on the type of metal used. MGG refers to the random orientation of the different metal grains leading to variations in the gate work-function. According to Figure 3.9 in the ideal fabrication process, metal gate devices have the gates produced with a unique metal uniformly aligned. Nevertheless, in the real fabrication process, metal gate devices are generally produced using metals with different work-functions ( $\phi_m$ ) randomly aligned, that implies in higher work-function fluctuation (WFF) (DADGOUR; DE; BANERJEE, 2008). Wang et al. (2011) highlight the high correlation between the variability in the on-state current and threshold voltage under metal gate granularity. In general, multigate devices exhibit higher MGG variability compared to other process variability phenomena like LER and RDF. Previous research indicates that work-function fluctuation is the main source of variability in FinFET devices (MEINHARDT; ZIMPECK; REIS, 2014b).

Figure 3.9: Metal gate alignment in a real and ideal manufacturing process



Source: Adapted from (ORSHANSKY; NASSIF; BONING, 2008)

### 3.1.1.3. Random Dopant Fluctuation

RDF arises from the variation in the implanted impurity concentration modifying the discreteness of dopant atoms in the transistor channel (BORKAR, 2005). The change in the number or placement of dopants atoms results in threshold voltage deviations that affect the transistor properties directly. The



variation in the source/drain resistance due to doping alterations dominates the RDF variability incurring in the absence of channel doping (WANG et al., 2011). Since the RDF is a local form of physical variability, neighboring transistors can present different dopant concentrations. The technology scaling down has been adjusting the channel doping to meet the targeted threshold voltage, on- and off-state current expectations. Moreover, to control the leakage currents and other challenges in bulk CMOS technologies, the total number of channel dopants increased significantly, resulting in a larger variety of dopant atoms. For this reason, the RDF was considered the major source of variability in planar technologies (NAWAZ; MALLIK, 2016). As the fin thickness is reduced, the FinFET becomes fully depleted, and the channel can be lightly doped, which provides a significant reduction in the threshold voltage fluctuations due to RDF. It implies that FinFET devices suffer less from dopant-induced variations (ABU-RAHMA; ANIS, 2013) (JIANG et al., 2016), improving the manufacturing yield.

### **3.1.2. Literature review about process variability**

This sub-section summarizes the main related works about process variability in FinFET technologies available in the literature.

#### **3.1.2.1. General Background**

A case study of Gold Standard Simulation (GSS) simulated some sources of variability in a 3D FinFET model. The experiments evaluated the impact of process variations on the  $V_{TH}$ ,  $I_{ON}$ , and  $I_{OFF}$  analyzing the electrical behavior in sub-threshold and saturation regions (GSS, 2010). Basic concepts, characterization, and challenges of process variability in digital circuits and systems were presented in (BORKAR, 2005) (DADGOUR; DE; BANERJEE, 2008) (NASSIF, 2008) (ENDO et al., 2009) (SAHA, 2010) (WANG et al., 2011). The effects of random variations on the performance of FinFET circuits using the analytical models were evaluated in (CAO; CLARK, 2005) (RAHMA-ABU; ANIS, 2008) (THAKKER et al., 2010) (WANG et al., 2013) as well as the performance estimation using response surface methodology was studied in (HARISH; BHAT; PATIL, 2007) (JUNG-HWAN; MURTHY; ROY, 2007).

Artificial neural networks have been widely used as a CAD tool for circuit design using both microelectronic and microwave devices (AVCI; BABAC; YILDIRIM, 2005) (JANAKIRAMAN et al., 2010). In (MUTLU; RAHMAN, 2005), a similar technique has been utilized to develop the

statistical performance model for a ring oscillator. The impact of process variations on the oscillation frequency of a bulk CMOS VCO was investigated in (GHAI; MOHANTY; KOUGIANOS, 2009) using Monte Carlo analysis. The behavior of SRAM cells and flip-flops under process variability was explored in (NEUBERGER; WIRTH; REIS, 2008) (RASOULI; ENDO; BANERJEE, 2009) (FAN et al., 2010). Mitigation techniques for environmental and reliability variations in FinFET devices were proposed in (ISLAM; AKRAM; HASAN, 2011) (WANG; COTOFANA; FANG, 2012). A method to model the effects of work-function variations in a transistor with a high-k metal gate was presented in (AGARWAL et al., 2013).

The quantitative evaluation of the contribution of different sources of statistical variability is provided in (CATHIGNOL et al., 2008) for a low-power bulk NFET. In (SWAHN; HASSOUN, 2006), FinFET gate sizing was formulated as a power minimization subject to delay, considering the operating temperature and weighting factors as constraints. One methodology to find the optimal sizing of FinFET circuits under process variations optimizing the worst-case cost for a given yield requirement was presented in (KLEEBERGER; GRAEB; SCHLICHTMANN, 2013). In (SWAHN et al., 2005), the sizing problem is formulated as a mixed-integer non-linear program (MINLP) to minimize the area of FinFET devices.

### **3.1.2.2. State-of-the-art works**

The influence of process variability on  $I_{ON}$  and  $I_{OFF}$  currents of PFET and NFET transistors were analyzed for a set of predictive FinFET technologies from 20nm to 7nm (MEINHARDT; ZIMPECK; REIS, 2014a). Results showed that fin height has a small standard deviation while gate length and fin thickness have a considerable difference from nominal conditions. However, for all setups evaluated, work-function fluctuation showed to be the most impacted parameter under the process variability effects with large standard deviation results.

An additional research was done in (ZIMPECK; MEINHARDT; REIS, 2014), focusing on analyzing the impact of temperature variations on 20-nm FinFET devices. LSTP devices are more sensitive to temperature oscillations. PFET devices are more impacted by the temperature, with an increase of  $7.27\mu\text{A}$  and  $7.82\mu\text{A}$  in the  $I_{ON}$  to HP and LSTP devices, respectively. LSTP devices

are up to 25% more susceptible to temperature variations. Another point is that PFET devices are approximately 30% more sensitive to temperature effects.

An evaluation of PVT variations impact on total/static power and timing in a set of cells was done in (MEINHARDT; ZIMPECK; REIS, 2014b) and (ZIMPECK; MEINHARDT; REIS, 2015a). Under voltage variations, some cells presented up to 70% of power-delay-product (PDP) reduction. However, voltage reduction provokes a timing increase by more than three times. Total power consumption is the principal parameter impacted by the temperature increase. At higher temperatures, the power increase can reach results of around five times the nominal values. Finally, WFF variation has a significant impact on  $I_{OFF}$  and consequently, on the static power consumption of standard cells. For cells with a similar function, but with the different number of inputs, it is possible to note a decreasing WFF sensibility as the number of inputs rises.

The impact of PVT variations and NBTI/PBTI aging on the write noise margins are measured and compared for a set of MOSFET and FinFET flip-flops (KHALID; MASTRANDREA; OLIVIERI, 2015). The authors adopted the 16-nm FinFET predictive technology from PTM to obtain the results. The smaller standard deviation in FinFET cells results in better performance for write failure probability at a given input voltage noise. Supply voltage dependence of noise margins tends to be always linear and poorly affected by aging. On the other hand, the temperature dependence of noise margins is linear, with opposite behavior in MOSFET and FinFET cells.

Different sources of process variability and their impact on FinFET-based logic cells were explored in (KARAPETYAN; KLEEBERGER; SCHILICHTMANN, 2015). Both TCAD and PTM device models were used and compared concerning the performance metrics of the NAND2 and NOR2 gates adopting the 14-nm technology node. They conclude that LER and MGG are the dominating local variability sources affecting the gate delay while the RDF has a negligible role. Otherwise, since the threshold voltage is highly sensitive to RDF, it has a dominant impact on leakage power variation along with the LER. There is a threshold voltage difference between the device models, and then, the deviations are of an order of magnitude higher for PTM.

The impact of fin shape variability on the short channel effect control is investigated through TCAD simulations both with 14-nm and 10-nm FinFET nodes (TOMIDA et al., 2015). This work reveals that fin height and fin thickness variations besides the taper angle have a

significant effect on the electrostatics of the device. Results showed a PFET transistor under these three fins shape variation and verified the impact in the  $I_{ON}/I_{OFF}$  currents. Compared to the nominal case, the higher, narrower and more tapered fins show less deviation on  $I_{OFF}$  currents. Especially in advanced nodes, they suggested that the suppression of the fin thickness and angle variability would be essential to guarantee the variability robustness.

The impact of PVT variations on performance and power consumption considering different transistor sizing techniques applied to a fixed subset of gates was presented in (ZIMPECK et al., 2015b) and (ZIMPECK et al., 2016a). The transistor sizing techniques analyzed were minimum transistor sizing (MTS), which corresponds to all cells with the number of fins equal to 1; logical effort (LE); and optimized transistor sizing (OTS) using the sizing presented in (POSSER et al., 2014). Results point out that transistor sizing regarding the process variability is not a trivial choice. The most indicated technique is the OTS for FinFET cells, but it presents large area overhead.

A novel FinFET structure with body spacers was proposed to improve the FER variation produced during the manufacturing process (WEI et al., 2016). The effective  $H_{FIN}$  with body spacers are precisely controlled because it only depends on the silicon epitaxy layer thickness. Device simulation using Sentaurus TCAD demonstrated an improvement from 33.46% to 8.05% in the  $I_{ON}$  current variation when the body spacers are applied in 10-nm bulk n-FinFET transistors. The gain is even more significant for devices when higher body spacer heights were used. Moreover, manufacturing FinFET with body spacers needs no extra lithography step becoming a promising mitigation technique for the industrial community.

A report about the impact of device scaling on the performance of a FinFET device due to gate work-function fluctuation and random dopant fluctuation was done in (NAWAZ; MALLIK, 2016). 3D device simulation considering the technology nodes of 14-nm, 10-nm, and 7-nm were performed. The WFF and RDF variations (observing standard deviation) of both threshold voltage and subthreshold swing are significant. Their investigation reveals that the impact of RDF can be reduced without to alter the channel doping, but meeting the targeted  $V_{TH}/I_{OFF}/I_{ON}$ . However, the negative side is the increase of the relative impact of WFF as the technology scaling down.

The threshold voltage variability induced by WFF for different grain sizes (10, 7, and 5-nm) in 14-nm FinFET technology is analyzed using 3D simulations (RATHORE; SHARMA; RANA, 2016). They observed that with a reduction in grain size, the threshold voltage variations decrease linearly. They have seen that the different fin shapes have around of 6% shift in the threshold voltage where there is approximately 16% improvement in the standard deviation of the  $V_{TH}$ . Further, on reducing the average grain size from 10-nm down to 5-nm results in an approximately 45% reduction in variability induced by WFF.

A detailed set of predictive data about FinFET and Trigate devices behavior considering process variability effects in  $I_{ON}$  and  $I_{OFF}$  currents were provided in (ZIMPECK et al., 2016b) and (ZIMPECK et al. 2017). Process variations analysis considers the individual contribution of the main geometric parameters of the devices using the predictive sub-22nm technologies from PTM-MG. Individually,  $L_G$ ,  $H_{FIN}$ , and  $W_{FIN}$  parameters slightly affect the  $I_{ON}$  currents considering geometric deviations in the range of 5% to 20%. On the other hand, the  $I_{OFF}$  suffers the higher impact of geometric variability, mainly on FinFET devices. PFET devices and the LSTP model are also more sensitive than NFET devices and high-performance models. Results highlight that Trigate devices are up to 10% less sensitive to gate length variations.

A simple device-level characterization approach to quantitatively evaluate the impacts of different random variation sources in FinFETs is proposed in (JIANG et al., 2017). The variations of threshold voltage induced by LER and MGG are theoretically decomposed based on the distinction in physical mechanisms and their influences on different electrical characteristics. The effectiveness of the proposed method was confirmed through both TCAD simulations and experimental results. There is a considerable increase when  $L_G$  shrinks, while for MGG variations,  $V_{TH}$  remains consistent. This work can provide helpful guidelines for variation-aware technology development.

Two-step FinFET devices with different fin material (Si and Ge) were analyzed under WFF and geometric variations and compared to conventional FinFET (SAHA; BHOWMICK; BAISHYA, 2017). The parametric analysis showed that Si step-FinFET is more immune to subthreshold swing (SS), drain induced barrier lowering (DIBL) and threshold voltage while Ge step-FinFET has higher  $I_{ON}/I_{OFF}$  ratio, lower intrinsic delay at different length and oxide thickness. When the

gate metal work-function fluctuation is inserted, Si step-FinFET presented a minor variation in the threshold voltage and subthreshold swing, but a higher variation in the  $I_{ON}/I_{OFF}$  ratio than in conventional FinFET. The proposed device performs better in low power applications.

Temperature dependence is of utmost importance for the performance and power dissipation analysis. The temperature dependence of bulk double-gate FinFET and Trigate MOSFET devices is investigated in (AGUIAR et al., 2017a). Additionally, it is also evaluated the analysis for the Zero Temperature Coefficient (ZTC) condition. The results indicate that the increase in leakage current can reach more than 40X when compared to the nominal temperature for high-performance applications. Trigate devices have shown to be more sensitive to these variations with a difference of up to 19.7% in  $I_{OFF}$  current when compared to FinFETs.

The impact of oxide thickness on threshold voltage variation induced by WFF in multigate devices was investigated using 3D simulation (LEE; SHIN, 2017). The WFF-induced threshold voltage variation does not significantly vary with dielectric material but increases with decreasing physical oxide thickness. The electric field tends to be locally concentrated, causing a considerable deviation of electrostatic potential as  $T_{OX}$  becomes thinner. They conclude that it is possible to alleviate the WFF-induced  $V_{TH}$  variation without significant performance degradation if the gate dielectric layer becomes thicker with appropriately adopted higher-k engineering.

The effects of fin thickness scaling of p- and n-type 10-nm FinFET and the correlation of the WFF with the electrical performance of the devices were investigated in (OTHMAN; HATTA; SOIN, 2017). They observed that the transfer characteristics are increased drain current in the linear region towards increased  $T_{SI}$  for both p- and n-FinFET. The threshold voltage is shifted to the right for p-type as the work function is increased. Oppositely for n-type, they shifted to the left as the work function reduced. The  $I_{ON}/I_{OFF}$  ratio for the low-performance device shows the magnitude drops to 63% and 82% in n- and p-type, respectively, when the fin width is changed from 4nm to 8nm.

A 3D simulation study to evaluate the threshold voltage variability induced by statistical parameters fluctuations in 14-nm bulk and SOI FinFET structures was done in (RATHORE; RANA;

SHARMA, 2017). They have studied and explored the influence of various statistical variability sources such as RDF, oxide thickness variation, and WFF on threshold voltage performance for both bulk and SOI FinFET structures. The simulation results suggest that the threshold voltage variability in SOI FinFET structure shows ~32% improvement as compared to bulk FinFET structure.

In (DAS; BAISHYA, 2017), they studied the effects of two essential variation sources such as work-function fluctuation of the gate material and the temperature, on the behavior of FinFET device. The investigation was carried out on a Germanium-based FinFET device. The working device showed improvements on the current drivability in terms of high ON current ( $I_{ON}$ ), less leakage current ( $I_{OFF}$ ), a high value of  $I_{ON}/I_{OFF}$  ratio, and have reasonable control on short channel effects. Moreover, the analysis carried out reveals that a high work-function gate material with optimum temperature show a good electrostatic behavior

One way to reduce the impact generated by WFF variations on full-adders (FA) is the replacement of internal inverters by Schmitt Triggers (ST) (MORAES et al., 2018). Four FAs were analyzed in nominal voltage and near-threshold regime at the layout level using the 7-nm FinFET node from ASAP7. In general, the ST technique presented considerable robustness improvements overall full-adders. The power robustness variability using the ST technique can be up to 37.3% and 66.6% better than traditional architectures operating at the nominal and near-threshold regime, respectively. The main disadvantage is the area penalty highlighting the need for new design techniques at the layout level to address variability.

The evaluation of process variability and SET masking on a set of complex logic gates considering different transistor topologies is explored in (BRENDLER et al., 2018a) using the 7-nm FinFET electrical model from ASAP7. A comparison is made between complex logic gates in their traditional versions and a multi-level of basic logic gates that implement the same function using only NAND2, only NOR2, and NAND2/NOR2/INV cells. The functions were converted using De Morgan's theorem. Results show that although complex cells present better timing and power results, multi-level circuits are up to 28% less sensible to radiation faults and about 40% more stable under process variability.

According to the best results encountered in the previous work, a new study was done at the layout level using ASAP7 technology (BRENDLER et al., 2018b). Seven logic cells were designed using complex logic gate and using only NAND2 gates (providing a multi-level cell design). At nominal conditions, the complex gate topology presents the best results, but under the effects of transient faults or process variability, multi-level arrangements are the best option. Despite the area impact, NAND2 topology mitigate at least 50% of the effect on delay due to process variability effects reaching, on average, more than 85% of improvement compared to complex gates. Moreover, NAND2 topology improves over 45% on average the fault coverage evaluation from SET effects for these layouts.

Schmitt Triggers are promising circuits for variability effects mitigation and enhancement of noise immunity being widely applied on critical applications with reliability constraints. In (MORAES et al., 2019), Schmitt Triggers were evaluated over multiple scenarios considering several levels of process variability, supply voltages, transistor sizing, and clock frequencies, prioritizing better energy consumption and the attenuation of process variability effects using the ASAP7 PDK. The hysteresis intervals showed attractive advantages of up to 10.8% and 25.3% when a higher number of fins and supply voltages were tested, respectively, bringing noise immunity improvements. It could be observed up to 16% and 44.7% maximum increase and decrease in the clock frequency, respectively, with differences between variability impact in the layouts, rising alongside the supply voltage values. The set of data in this paper can provide relevant information for VLSI designers, and also for the design of low power applications that need to manage the process variability impact.

All my own works presented in this subsection are not part of the thesis results. These researches evaluate the process variability impact considering the electrical models from PTM-MG besides not analyzing any mitigation techniques.



## **3.2. Radiation-Induced Soft Errors**

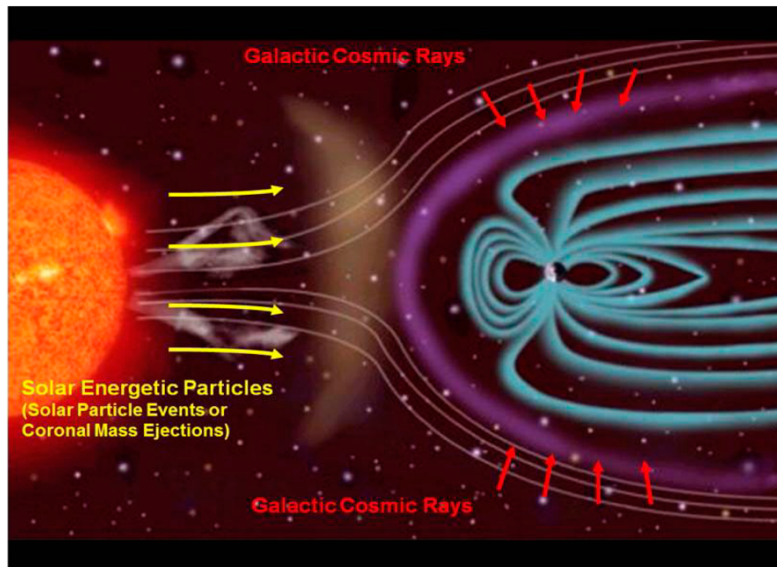
Another key reliability concern at advanced technology nodes is the susceptibility to natural radiation environments. Initially, the radiation effects in electronic systems were only considered relevant in cases of military, avionic, or spatial designs. However, with microelectronics advancement and using low supply voltages, transient event errors can occur even at sea level and may bring critical consequences (DODD et al., 2010). This chapter explores the radiation environment and its characteristics, the effects caused by radiation on circuits, the charge collection mechanism in FinFET devices, and the state-of-the-art works.

### **3.2.1. Radiation Environment**

The natural radiation can be divided into spatial and atmospheric environments. The three main sources of spatial radiation are solar, galaxy cosmic ray, and belt radiations (BARTH, 1997), as shown in Figure 3.10. The solar radiation depends on the sun activity. Typically, in a period of high solar activity, few neutrons are detected, but in a period of lower solar activity, the Earth's magnetic field traps particles that can be absorbed by the atmosphere. The cosmic radiation arises from stellar flares, supernova explosions and other cosmic activities and it consists mainly of protons. Finally, the Van Allen belts are the space areas closest to the Earth with a large number of protons and electrons. These protons are especially dangerous for spacecraft following the Low Earth Orbit (LEO).

The Earth is protected by a magnetic field that acts as a radioactive filter, blocking a large quantity of radiation coming from space (solar flares, solar winds, cosmic rays). However, high energetic particles arising from cosmic radiation are not trapped by this filter, and then, they can interact with the atmosphere via direct ionization or by nuclear reactions. The nuclear reactions produce every kind of secondary radiation (BARTH et al., 2003). The result of the cosmic-ray shower is a set of energetic particles such as protons, electrons, neutrons, heavy ions, muons, and pions. The type of secondary radiation and the intensity depend on the altitude, the geomagnetic latitude, and the Sun's activity. At sea level, the radiation levels are smaller due to the loss of energy generated by the successive collisions. Currently, muons are the energetic particles most numerous at ground level (HUBERT; ARTOLA; REGIS, 2015).

Figure 3.10: Spatial radiation environment



Source: (CHANCELLOR; SCOTT; SUTTON, 2014)

### 3.2.2. Radiation effects on devices

The radiation effects that affect the integrated circuits can be classified into three categories: displacement damage (DD), total ionizing dose (TID), and single event effects (SEE). Displacement damage refers to the dislodging of atoms of the crystalline structure of a material due to non-ionizing energy loss (NIEL) of the incident particles. NIEL depends on the material being irradiated, the particle type, and the particle energy (SROUR; PALKO, 2013). DD degrades the minority carrier lifetime, the carrier mobility and the net doping level due to the introduction of new energy levels in the semiconductor bandgap. TID is a cumulative effect that happens due to long-term silicon exposure to radiation, and it can damage a circuit permanently. The total accumulated dose depends on orbit altitude, orientation, and time. TID is measured concerning radiation absorbed dose (rad). The trapped charges in the STI oxide and at its interface with silicon affect the electrical characteristics (VELAZCO; FOUILLAT; REIS, 2007). Irradiated circuits for a long-term can cause threshold voltage shifts, increased leakage currents, timing changes, mobility degradation, and loss of circuit functionality. Planar technologies needed hardening by design (HBD) techniques like enclosed layout transistor (ELT) or guard rings, to become the integrated circuits almost free from the TID effects (FACCIO,

2007). However, the 3D structure and the oxides used in the FinFET manufacturing process are favorable to attenuate the impact of TID.

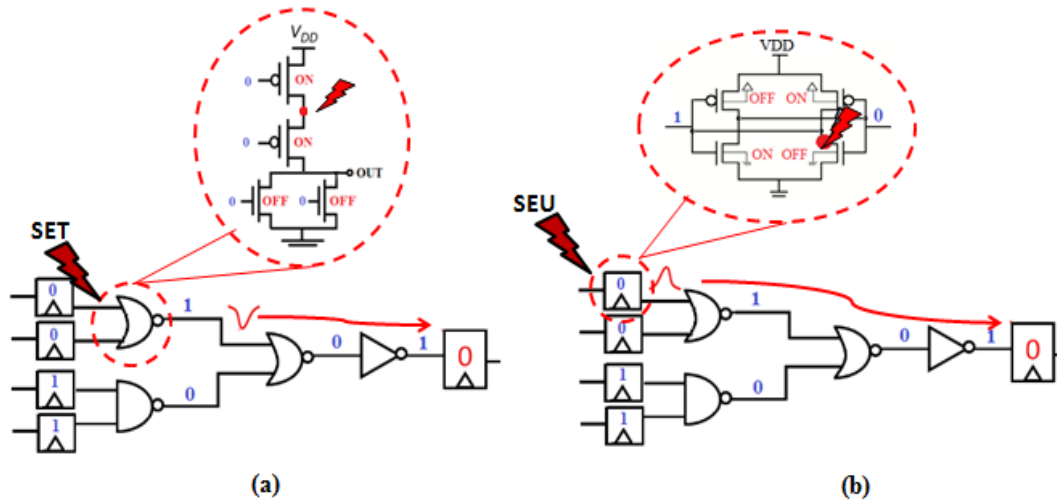
Single event effects occur due to the interaction of energetic particles, coming from space and atmospheric radiations, with the silicon. For older technologies, a transient pulse only happens if the collected charge ( $Q_{\text{coll}}$ ) exceeds the critical charge ( $Q_{\text{crit}}$ ) of the nodes. However, nanometer technologies increase the proximity of devices, such that a single hit can diffuse the charge to the adjacent nodes introducing the concept of charge sharing (TOURÉ et al., 2011). The charge deposited by a single ionizing particle can produce a wide range of effects that can be classified as destructive and non-destructive. Destructive effects cause permanent and irreversible functional damages (SEXTON, 2003). The most known destructive effects are: Single Event Latchup (SEL) where, exclusively in CMOS devices, a low resistance path is created between power supply and ground rails; Single Event Burnout (SEB) when the particle reaches the source region of the transistor creating a conductive path between the source and the drain; Single Event Gate Rupture (SEGR) where the gate dielectric isolating the gate and channel regions fails; Single Hard Errors (SHE) when the deposition of large charges affects the state transitions of the devices.

Non-destructive effects, also named as soft errors, induce a temporary deviation where the data are corrupted for a short time interval (O'BRYAN, 2000). The most well-known non-destructive effects are: Single Event Upset (SEU) when an energetic particle hits a sequential circuit, such as latches or flip-flops, causing the change of the stored bit; Single Event Transient (SET) when the particle strikes a combinational circuit, such as basic gates or full-adders, generating a transient pulse that may or may not be captured by a memory element. The interaction of radiation with devices is usually quantified by the linear energy transfer (LET), which is a measure of the average energy deposited by a particle per unit path length (SCHRIMPF et al., 2012).

Figure 3.11 exemplifies the non-destructive effects: (a) SET and (b) SEU. First, a SET occurs in a sensitive node of a NOR2 logic gate, and it generates a pulse at the stroke node. This pulse was propagated, and it reached the sequential logic to the right, which stored the incorrect value '0'. Memory cells have two stable states, one that represents a stored value '0' and one

that represents a stored value '1'. In each state, there are two transistors in on-state and two transistors in off-state. In the second case, an energetic particle hits the sequential circuit in one of the two sensitive nodes. So, a bit-flip happens, and it affects the rest of the circuit because the incorrect value also is captured by the sequential element on the right.

Figure 3.11: (a) Single Event Transient and (b) Single Event Upset on a circuit



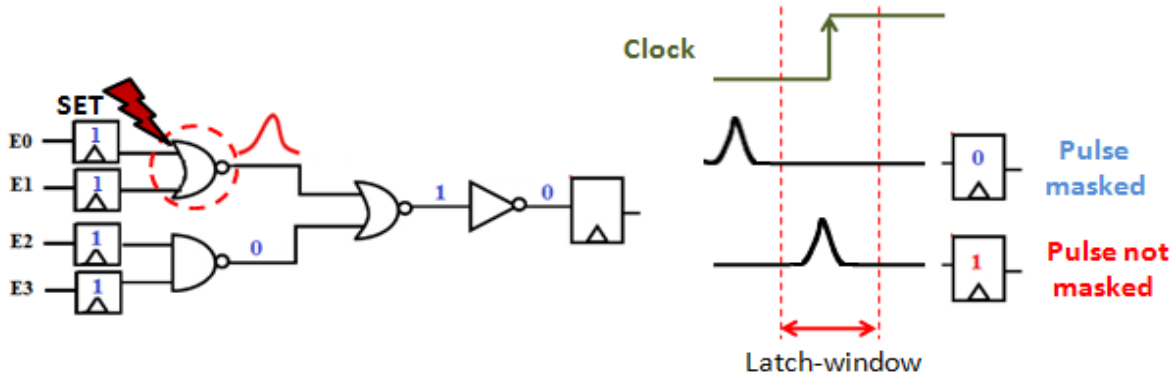
Source: From the author

### 3.2.3. Fault Masking

There are some cases where a transient pulse will be masked, and the sequential elements will not capture it. In this case, the fault will not lead to errors or failures visible to the user. Moreover, the circuit keeps a correct value in the output because the faults are masked still in origin. There are three kinds of masking observed in logic blocks: logical masking, electrical masking, and latch window masking (LIDEN et al., 1994) (SHIVAKUMAR, 2002). The logical masking happens when a particle affects a portion of the circuit, but the hit node is not relevant to determine the final output. In this way, the output can be determined only by inputs not affected by radiation effects. For example, the first input of a NAND2 logic gate in Figure 3.12 is '0', and then, the second input is not important because the final result will always be '1'. So, if a particle impacts one of the inputs, the error will not be seen in the final output. According to the truth table, the same happens with a NOR2 logic gate. If one input is equal to '1', the final result will always be '0'.



Figure 3.14: Latch-window masking in a combinational circuit



Source: From the author

In the scientific community, the two radiation effects most relevant is the total ionizing dose and single event effects (CLEMENS, 2012). Some years ago, TID was considered a major source of faults in integrated circuits. However, as technology has advanced, SEE gained more prominence and becomes a significant reliability concern for electronic systems in space as well as ground level. The TID effects were reduced due to the thinner oxides of modern deep submicron processes (FACCIO, 2007). On the other hand, transistors with shrinking geometry, higher speed, and logic density increase the SEE sensitivity. Moreover, as the supply voltage decreases, the charge stored at circuit nodes reduces according to Equation 3.2, such that the critical charge can be larger than the collected charge more often. Consequently, soft errors susceptibility increases due to advanced technology nodes.

$$Q_{\text{node}} = C_{\text{node}} \cdot V_{\text{DD}} \quad (3.2)$$

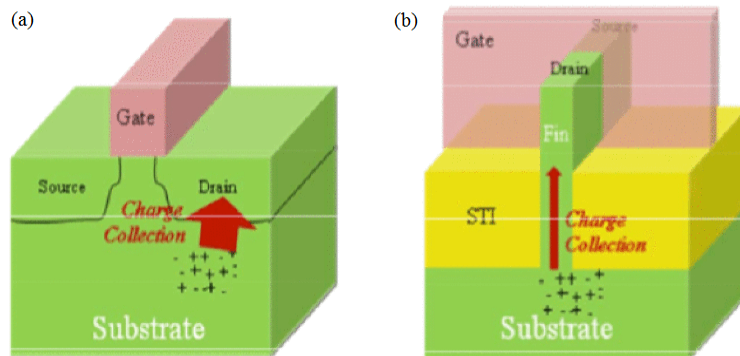
The 3D structure of FinFETs presents attractive properties to control the increase of the radiation-induced soft errors compared to the bulk counterpart (EL MAMOUNI, 2011). However, the change in device structure from planar to FinFET modifies the sensitive area and the charge collection mechanisms after an energetic particle hits the silicon (NSENGIYUMVA et al., 2016). In this way, the improvement of the reliability in sub-22nm technologies also requires the accurate understanding, predicting, and mitigating of the single event effects on FinFET based-circuits.

### 3.2.4 Charge collection mechanism in FinFET devices

The collision of energetic particles causes a strong electric field perturbation due to the direct ionization, a primary mechanism of charge deposition caused by the incidence of alpha particles or heavy ions. As an energetic particle hits in the silicon, it loses energy and forms a track of electron-hole pairs. If the ionization track transverses the depletion region, the electric field collects the carriers generating a transient current pulse at the node. The charge generated by the impact of particles varies depending on the ion type, incident angle, and impact site.

In traditional planar devices, charges associated with the ion tracks colliding the silicon substrate are deposited in the drain directly and then, and then diffuse to the drain, as shown in Figure 3.15 (a). Otherwise, the thin fin region and the narrow connection to the substrate of the bulk FinFETs reduce the volume of silicon available for the charge collection when compared with planar devices. Thus, a smaller amount of deposited charges can be expected to diffuse the FinFET drain, as illustrates Figure 3.15 (b) (FANG; OATES, 2011). For these reasons, the FinFET devices are considered less sensitive to soft errors.

Figure 3.15: Comparison of charge collection mechanism of (a) planar and (b) FinFET devices

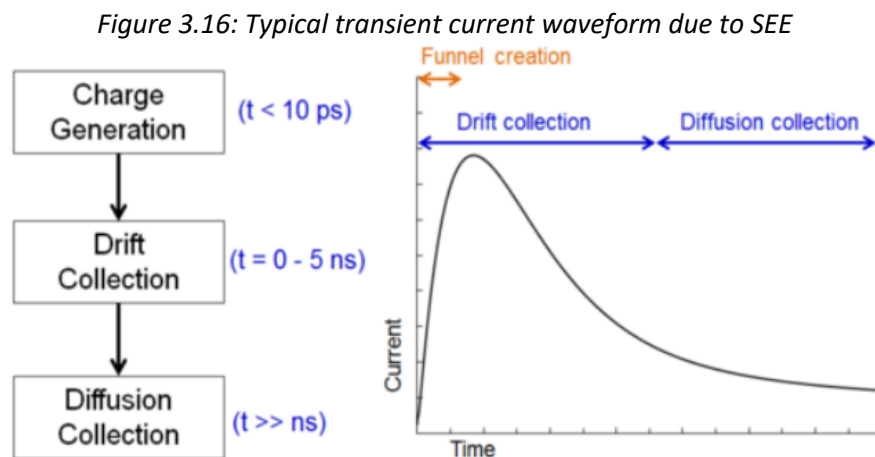


Source: (LEE et al., 2015)

The disturbance caused for the impact of energetic particles depends on the energy lost per unit track length and it is known as linear energy transfer (LET). For every 3.6eV (electron volts) of energy loss by the particle, one electron-hole pair is created in the silicon substrate (HARTMANN, 2009). The LET depends on the mass/energy of the particle and the material in which it is traveling. The highest LET values are obtained when more massive and energetic

particles impact denser materials (BAUMANN, 2005). In this way, the pulse width is dependent on the particle energy, the charge stored at a node, and the charge collection in the affected junction.

After the silicon particle ionization, the process of charge collection proceeds through two mechanisms: drift and diffusion (MUNTEANU; AUTRAN, 2008). When the resultant ionization track traverses the depletion region, carriers are rapidly collected by the high electric field. This charge collection is known as drift. The crossing of particles through the depletion region is responsible for temporary deformation in a funnel shape. This effect is called funneling, and it causes an increase in the collected charge efficiency due to the increase of the depletion region area (BAUMANN, 2005). Finally, the diffusion process collects all the other carries generated besides the depletion layer. The typical transient current waveform resulting from the additional collect charge induced by particle incidence can be seen in Figure 3.16. The funnel creation and drift mechanism are high-speed processes. They are responsible for controlling the almost instantaneous rise of the transient current due to deformation of the electric field of the junction. In the diffusion mechanism, a longer time is needed to collect the charge and, then, the transient pulse has a slower fall time.



Source: (CUMMINGS, 2010)

Charge deposition mechanism proposed in (MESSENGER, 1982) is widely used to form a current source whose behavior is modeled as a double exponential. The modeling of the



transient current is given by Equation 3.3, Equation 3.4, and Equation 3.5, where:  $Q_{coll}$  is the collected charge due to a radiation particle strike,  $\tau\alpha$  is the collection time constant of the junction and  $\tau\beta$  is the ion track establishment time constant and  $L$  is the charge collection depth that decreases with the technology scaling. In bulk silicon, a typical charge collection depth for a heavy-ion is approximately  $2\mu\text{m}$ . For every  $1\text{MeV}\cdot\text{cm}^2/\text{mg}$ , an ionizing particle deposits about  $10.8\text{fC}$  of electron-hole pairs along each micron of its track (MAVIS et al., 2002). For sub-22nm nanometer technologies, especially for LETs higher than 10 MeV, the typical transient current waveform tends to suffer some modifications presenting a behavior similar to "plateau" (SAYIL, 2016). However, double exponential current sources still are considered the most reasonable first-order estimate, and it is widely adopted as a base model for SEE analysis (WROBEL et al., 2014).

$$I_p(t) = I_0 \cdot (e^{-t/\tau\alpha} - e^{-t/\tau\beta}) \quad (3.3)$$

$$I_0 = Q_{coll}/(\tau\alpha - \tau\beta) \quad (3.4)$$

$$Q_{coll} = 10.8 \cdot L \cdot \text{LET} \quad (3.5)$$

### 3.2.5. Literature review about radiation effects

This sub-section summarizes the main related works about radiation effects in FinFET technologies available in the literature.

#### 3.2.5.1. General background

A theoretical overview of the several ways that FinFET circuits can be affected due to radiation was discussed in (SCHRIMPF et al., 2012). In general, the sensitivity of technology to SEE increases as device dimensions decrease. The susceptibility of the SOI and bulk FinFETs to total ionizing dose and single event effects were compared in (ALLES et al., 2011). Similar research was done in (ROCHE et al., 2013) reporting the radiation experiments in UTBB FDSOI 28-nm for the first time. In general, bulk FinFETs tends to collect more charge than SOI FinFETs due to substrate considerations.

The fault models for FinFET circuits were discussed in (LIU; XU, 2012) including fin stuck-on, stuck-open, and gate oxide short. One single defect may affect multiple gates that are

correlated due to the configuration of FinFET. The effects of the single event latchup in bulk FinFETs and planar technologies were investigated by (DAI et al., 2017). The small fin structure seems to be harmful to latchup immunity due to the increased parasitic resistance and the reduced guard ring efficiency. However, FinFET circuits with a higher supply voltage have a higher risk of latchup effects.

The FinFET structure modifies the charge collection mechanism on a device. A charge collection mechanism for FinFETs using through-wafer two-photon absorption and ion beam experiments were analyzed in (EL MAMOUNI et al., 2011). In (ARTOLA et al., 2015), the behavior of FinFET devices under radiation effects was investigated as well as the modeling of the SET pulse at advanced technology nodes. In (MONGA et al., 2016) was presented a charge collection model for accurate prediction of SER in FinFETs. The model proposed is scalable and includes the effects of variation of FinFET technology and layout parameters.

In (SEIFERT et al., 2012), the radiation-induced soft error rates (SER) of memory and logic devices designed in 22-nm Trigate technology was reported. Comparison with the 32-nm planar devices showed a SER reduction of 1.5x - 4x for cosmic radiation. An overview of the impact of terrestrial radiation on soft error sensitivity considering bulk, FDSOI, and FinFET technologies was done in (HUBERT; ARTOLA; REGIS, 2015). According to the results, the muon is the main particle to provoke an increase of SER in sub-22nm technologies.

A Multi-Scales Single Event Phenomena Predictive Platform (MUSCA SEP3) was developed by (HUBERT et al. 2009). This platform is dedicated to SEE prediction based on a Monte Carlo method which allows a full simulation from the radiation environment definition down to the occurrence of the soft error in the integrated circuit. The analysis confirms that MUSCA SEP3 agrees very well with TCAD simulations and SEU/SET irradiation testing while reducing the computational effort by several orders of magnitude. The details of the Monte Carlo radiation tool used in this work will be presented in the next sub-section.

In planar technologies, a set of layout techniques were proposed to attenuate the radiation-induced soft errors. Although the FinFET structure is different from the planar one, some approaches can be tested to mitigate transient faults in FinFETs. A layout approach via pulse quenching was investigated by (ATKINSON et al., 2011). For this technique, one extra

drain diffusion is inserted into a cell output is inserted to intentionally promote charge sharing between transistors and quench the voltage pulse on the output. TCAD simulations demonstrated a reduction of 60% and 70% in the sensitive area and the pulse width, respectively.

A set of n-well contact schemes were investigated to verify the influence on the pulse width of SETs in (ALBHIN et al., 2011). Results showed a strong relationship between the SET pulse width and the percentage of the n-well area contacted contradicting the theory that the cross-section of a logic gate is based entirely on the drain regions of transistors. A multi-finger layout technique for N-hit SET mitigation is discussed in (CHEN et al., 2012a) for the standard cell design. TCAD simulations with heavy ions experiments show that SET pulse widths are efficiently reduced with the multi-finger approach. Moreover, the method presented an area penalty acceptable, and the performance of circuits remains almost unchanged. Multi-finger is preferred over the traditional arrangement in the radiation hardened integrated circuit design. Similarly, according to (CHEN et al., 2012b), a source isolation technique is used for the P-hit SET mitigation.

Another layout technique for SET mitigation based on dummy transistors was proposed in (CHEN et al., 2013). The approach calls for the addition of an off-state idle PMOS and NMOS transistor to the circuit connected to the sensitive region. The performance of cells that uses the proposed layout almost does not change as well as it is generated a smaller area penalty.

### **3.2.5.2. State-of-the-art works**

The behavior of FinFET circuits under the total ionizing dose effects was explored in (CHATTERJEE et al., 2014), (HUGHES et al., 2015), (KING et al., 2017) and (ZHANG et al., 2017a). The TID response of bulk FinFETs is investigated under geometric variations (CHATTERJEE et al., 2014). Transistors with more extended channels ( $L_G$ ) degrade less than those with shorter channels. On the other hand, devices with large fin pitch degrade more, compared to those with narrow fin pitch. The TID-induced degradation increases with decreasing of the fin thickness ( $T_{SI}$ ). TID radiation effects on 14-nm bulk and SOI FinFET technologies were analyzed by (HUGHES et al., 2015). The replacement of MOSFET by FinFET device generates an increase

in TID sensitivity due to the trapped charge in the STI oxide. Moreover, irradiation resulted in significant changes in the threshold voltage for SOI devices and significant deviations in the  $I_{OFF}$  current for bulk FinFETs.

In (KING et al., 2017), a near-threshold operation is presented as a methodology for reducing the increases in leakage currents caused by radiation. Results indicate devices with high channel stop doping as the most robust response to TID, allowing stable operation of ring oscillators and the SRAM bit-cell with a little shift in critical operating characteristics. The TID response was evaluated with strained Ge pMOS FinFETs varying the fin length, fin thickness, and gate length in (ZHANG et al., 2017a). Modest threshold voltage shifts, small transconductance degradation, and minimal changes in  $I_{ON}/I_{OFF}$  ratios are observed. In comparison with planar Ge pMOS, the improvements in Ge pMOS FinFETs happen due to the material quality, reductions in the STI thickness in areas of relevance to transistor operation, and better gate control.

Hardening techniques to attenuate the effects of radiation-induced soft errors were investigated in (CALOMARDE et al., 2014), (NARASIMHAM et al., 2017) and (ALGHAREB et al., 2017). A novel design style which reduces the impact of radiation-induced single event transient on logic circuits, and enhances the robustness in noisy environments through the strengthening of the sensitive nodes using a technique similar to feedback was presented in (CALOMARDE et al., 2014) The results were compared with other techniques for hardening radiation at the transistor level using 7-nm FinFET technology. Strengthening presents the best immunity in a noisy environment.

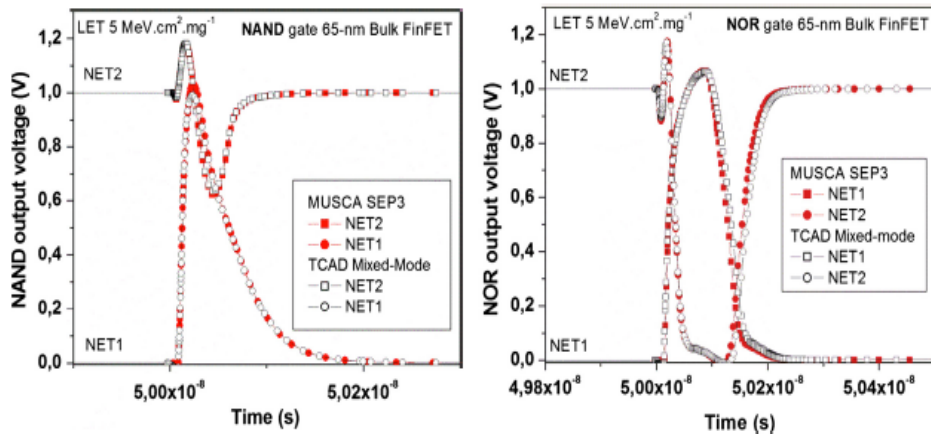
A charge-steering based latch hardening technique with significant SEU hardness was proposed in (NARASIMHAM et al., 2017). TCAD simulations showed the effect of charge steering in 16-nm bulk FinFET devices for reducing the amount of collected charge at the critical sensitive nodes considering alpha, proton, and heavy ions. The trade-offs regarding the area, performance, and power penalties are much lower compared to the other hardening approaches already proposed in the literature.

A set of techniques to mask SET and SEU using spatial, temporal, and hybrid redundancy were investigated by (ALGHAREB et al., 2017). The performance and energy impact of each

method is quantified at the near-threshold operation. A comparison between 45-nm planar and 16-nm FinFET technologies was made to investigate the effects of technology scaling. Temporal redundancy provides higher energy saving, but it requires consideration of the SET pulse duration.

The variability along with SET in FinFETs was explored in (ARTOLA; HUBERT; ALIOTO, 2014), (SEIFERT et al., 2015), (AGUIAR et al., 2017b) and (AGUIAR; MEINHARDT; REIS, 2017). The soft error evaluation of logic gates in FinFET technologies considering the prediction tool MUSCA SEP3 coupled with electrical simulations of the gate was presented in (ARTOLA; HUBERT; ALIOTO, 2014). First, a comparison of this tool with the TCAS mixed-mode simulation for an ion with LET equal to  $5\text{MeV cm}^2 \text{mg}^{-1}$  was made obtaining a good agreement between them as shown in Figure 3.17 Only a small divergence can be observed in the NOR2 logic gate when the output voltage of NET1 and NET2 come back to their initial logic state.

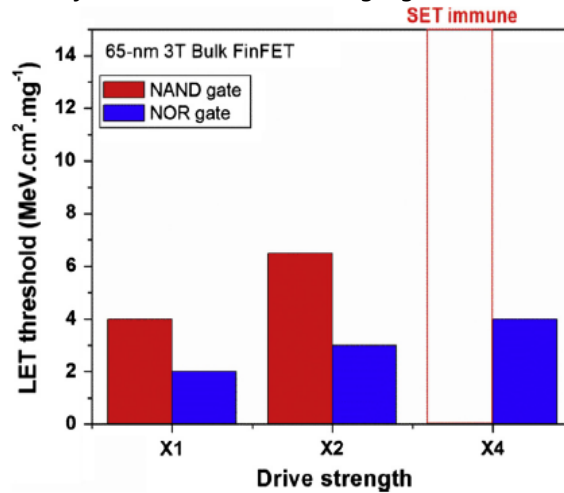
Figure 3.17: Comparison of the transient response of 65-nm NAND2 and NOR2 logic gates using MUSCA SEP3 and TCAS mixed-mode



Source: (ARTOLA; HUBERT; ALIOTO, 2014)

After, two soft errors reduction techniques were explored in NAND2 and NOR2 FinFET logic gates: supply voltage variation and the drive strength. The higher supply voltage diminishes the SET susceptibility of both logic gates as discussed previously in this chapter. Using a larger channel width in FinFETs, i.e., higher drive strength, the SET sensitivity of both logic gates decreases, as shown in Figure 3.18 The NAND2 cell is immune to SETs induced by atmospheric neutrons when the X4 drive strength is used.

Figure 3.18: LET threshold for NAND2 and NOR2 logic gates with a range of drive strength



Source: (ARTOLA; HUBERT; ALIOTO, 2014)

The SER of memory and logic devices manufactured in a 14-nm FinFET technology was measured in (SEIFERT et al., 2015). Results showed that SER is dominated by high-energy neutron-induced upset rates (77%), while thermal neutron and alpha-particle contribute around 16% and 7%, respectively. Moreover, there is a SER reduction when the 14-nm node is adopted instead of 22-nm technology. This reduction happens due to the fin dimensions, little scaling, and a decrease in charge collection efficiency per fin.

A comparative analysis of two majority voters based on NOR and NAND gates designed in 7-nm FinFET technology to estimate the SER was explored by (AGUIAR et al., 2017b) at the layout level. In general, NOR voter is less sensitive to soft errors than the NAND voter as it provides lower soft error rate. However, NOR voter presented a larger SET pulse width. At nominal supply voltage, no event has been observed for alpha and atmospheric environment.

In (AGUIAR; MEINHARDT; REIS, 2017), different XOR topologies under radiation effects were implemented using two multigate devices: double-gate FinFET and Trigate. Trigate-based circuits demonstrated to be more robust than FinFET with improvement percentage from 6.2% up to 12.6% in the threshold LET. Furthermore, voltage deviation can reduce the threshold LET up to 20.8%, increasing the fault susceptibility of the analyzed circuits.

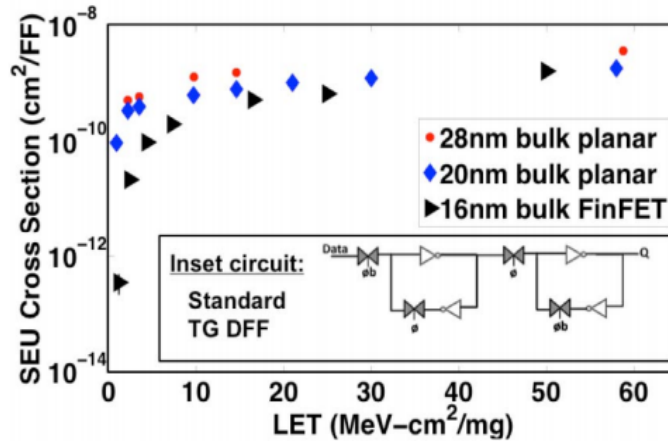
The SEU susceptibility in FinFETs in sequential circuits was verified in (KIAMEHR et al., 2014), (NARASIMHAM et al., 2015), (UEMURA et al., 2016), (NSENGIYUMVA et al., 2016),

(UEMURA et al., 2017), (NSENGIYUMVA et al., 2017) and (ZHANG et al., 2017b). A detailed analysis of radiation-induced soft errors of SRAMs designed in SOI FinFET technology was presented by (KIAMEHR et al., 2014). The authors considered the effects of supply voltage and process variations on the soft error rate of SRAM memory arrays. They conclude that SER is higher for lower supply voltages, MBU/SEU ratio is relatively higher for alpha radiation compared to that for protons, and neglecting the impact of process variation leads to an under-estimation of SER.

The SEU cross-section over an extensive supply voltage range for D flip-flops designed in 16-nm FinFET technology was evaluated in (NARASIMHAM et al., 2015). Also, comparisons between planar and FinFET devices sensitivity to SEU were made. The cross-section increases with a reduction in bias for low-LET particles as alpha particles and low-energy protons. Results reinforce that SEU rates are influenced by the supply voltage and the operating environment.

Characterization of the soft error rate through of the alpha irradiations considering combinational cells, SRAM, and flip-flops manufactured in 14-nm FinFET technology was presented by (UEMURA et al., 2016). The main factor that contributes to the increase of SEU is the charge collection on NMOS transistors due to low-LET incidence. Design schemes for low-power have little impact on the SER. An extension of this work was published in (UEMURA et al., 2017) where the 10-nm FinFET technology was evaluated. A comparison of SEU trends among 16-nm bulk FinFET, 20-nm bulk planar, and 28-nm bulk planar were made in (NSENGIYUMVA et al., 2016) considering D flip-flop. For LETs lower than  $10 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ , 16-nm FinFET flip-flops presented a considerably smaller SEU cross-section compared with the planar technologies. However, the cross-section of the 16-nm FinFET flip-flop for high LET particles is very similar to planar nodes analyzed, as shown in Figure 3.19. The SET pulse width is reduced in FinFET technology for low as well as high LETs. Moreover, the SET pulse width decreases when the supply voltage is increased. FinFET technology has a lower critical charge than that of planar nodes such that 3D simulations demonstrated a more considerable difference between them than experiments after the fabrication process.

Figure 3.19: SEU cross section versus LET for FinFET and planar technologies



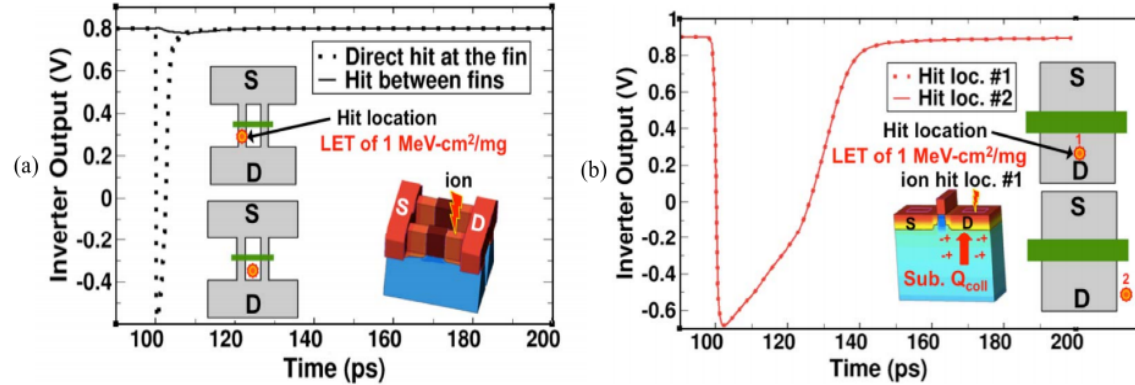
Source: (NSENGIYUMVA et al., 2016)

After, in (NSENGIYUMVA et al., 2017), the authors investigated the FinFET structural effects on the SE cross-section. Results showed that an ion strike direct at the fin produces an observable SET while an ion strike between two fins results in a minimum voltage perturbation according to Figure 3.20. For the planar technology, independently of the hit location, a SET pulse was observed at the inverter output for low LET particles. For strikes by energetic particles with high-LET, no dependence was observed to either device technologies, as shown in Figure 3.21.

An evaluation of the angular effects of incident heavy ions on the SEU cross-section of D flip-flop designed in a 16-nm bulk FinFET was made in (ZHANG et al., 2017b). Incident direction included normal incidence, West-East (tilt angle), and North-South (roll angle) incidences. Similar to planar technologies, the SEU cross-section increases along with tilt angles. Otherwise, an increase in roll angle in FinFET technologies decreases the charge track length in the active silicon region due to the fin structure, resulting in a decreased SEU cross-section. The effects of the threshold voltage and frequency variations on the SEU response of D flip-flops and logic circuits designed in 16-nm FinFET and 20-nm planar technologies were studied in (ZHANG et al., 2017c). Results showed that an increase in the  $V_{TH}$  is directly related to the rise of the SEU cross-section for the FinFET technology while the planar technology showed the opposite  $V_{TH}$  dependence. An increase in the clock frequency leads to higher SEU cross-section for both devices.

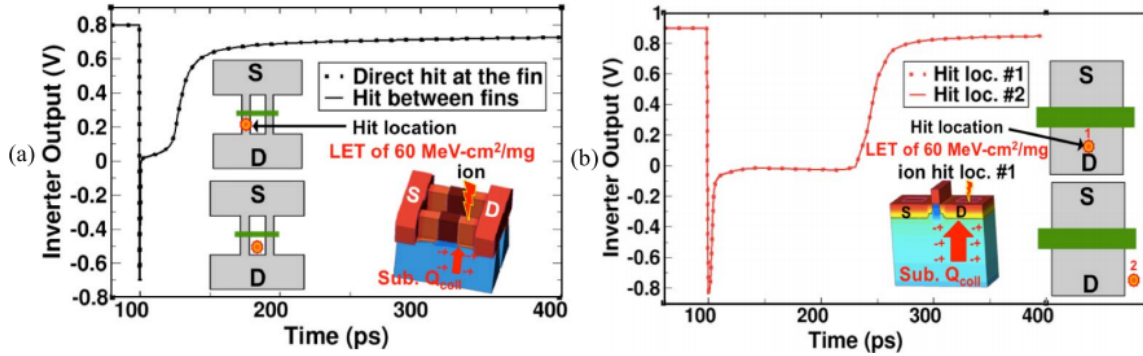


Figure 3.20: Impact of transistor structure on low-LET for (a) 16-nm FinFET and (b) 28-nm planar technologies using 3D TCAD simulations



Source: (NENGIYUMVA et al., 2017)

Figure 3.21: Impact of transistor structure on high-LET for (a) 16-nm FinFET and (b) 28-nm planar technologies using 3D TCAD simulations



Source: (NENGIYUMVA et al., 2017)

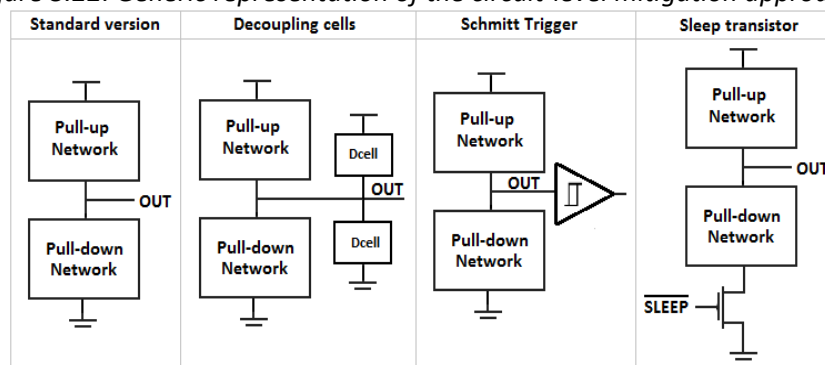
Finally, the impact of multiple bit upsets in FinFET circuits was analyzed in (BHUYA et al., 2015) and (EBRAHIMI et al., 2016). A comparison of the SRAM sensitivity to multiple bit upsets considering 28-nm bulk planar and 16-nm bulk FinFET technologies over a wide range of LET values and supply voltage was made in (BHUYA et al., 2015). FinFET-based SRAM decreased the percentage of MBU errors compared to the planar one for the same particle LET values. For both technologies, MBUs due to high-LET particles dominate the overall rates. A set of benchmark circuits were synthesized to 45-nm planar and 15-nm FinFET technologies in (EBRAHIMI et al., 2016), and the probability of MBUs was evaluated with different LETs. The results reveal that the average number of upset cells by a single particle strike doubles from 45-nm to 15-nm. As the particle energy is increased, the average of the affected cells also increases.

### 3.3. Circuit-Level Mitigation Approaches

Several techniques can be applied in different abstraction levels for enhancing the reliability of integrated circuits. Usually, mitigation techniques based on the usage of different devices, materials, or doping profiles estimate your effectiveness using TCAD simulations. Although this abstraction level presents very accurate results, it demands larger computational time for VLSI designs. So, one alternative is to investigate circuit-level approaches to achieve more robust solutions. Design adjustments can be related to the insertion of components or filtering elements, the exploration of different transistor arrangements, gate upsizing, transistor folding, hardware redundancy, increase of the capacitance of the most susceptible nodes, and the use of multi-level design instead of complex cells.

The four circuit-level mitigation approaches explored in this work are the transistor reordering, and the insertion of decoupling cells, Schmitt Triggers, and sleep transistors. All these methods were previously evaluated in the literature but focusing on improving other reliability challenges or using planar CMOS technologies. Considering that these techniques were beneficial for other reliability purposes and the effectiveness of them can change for FinFET technologies, they were chosen to be evaluated in this thesis. Figure 3.22 shows the generic representation of each of them in the design, with exception to the transistor reordering technique since your modifications happen inside of pull-up or pull-down networks. The main characteristics, advantages, drawbacks, and how are the implementations of each of them are presented in the subsections, adopting the AOI21 logic cell as an example.

Figure 3.22: Generic representation of the circuit-level mitigation approaches



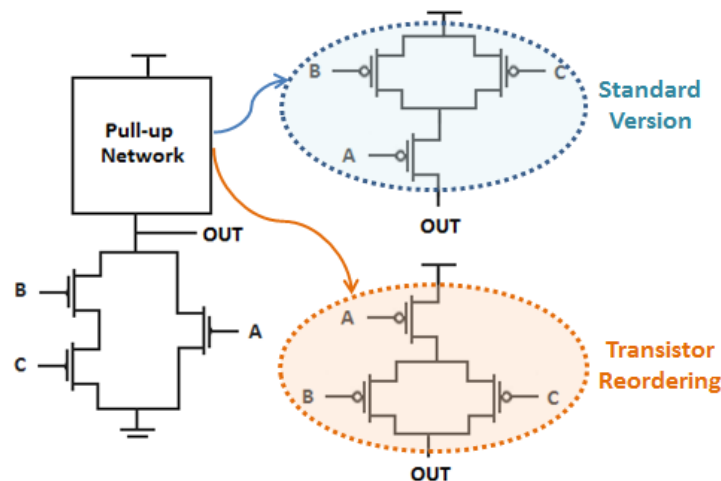
Source: From the author

### 3.3.1. Transistor Reordering

The optimization of the transistor arrangements is a method typically used to design faster circuits, to reduce the leakage currents or to deal with bias temperature instability (BTI) effects (SILVA; REIS; RIBAS, 2009) (BUTZEN et al., 2010) (CHUN; CHEN, 2016). The principle of this technique is to modify the transistor arrangements keeping the same logic function for all topologies. The possibilities can be obtained by using different logic styles such as complementary CMOS, ratioed logic and pass-transistor logic, or by transistor reordering. The transistor reordering changes the electrical and physical characteristics of the logic cells, and consequently, the susceptibility to process variation and soft errors also is modified.

Figure 3.23 shows two alternative topologies for the AOI21 cell that are logically equivalent. In the pull-up network, the serial transistor (input signal A) can be placed close or far to the cell output. Some logic gates, such as AOI221 and OAI221, can also explore an intermediate place between the parallel associations to put the serial transistor. The close topology is defined as the standard version in this work because it is the most used in the standard cell libraries. When the transistors of the complementary network have only parallel associations, as shown in Figure 3.23, the rearrangement is not necessary because it does not influence the results like power consumption and performance. The absence of area penalty is the main advantage of transistor reordering technique.

Figure 3.23: Standard version of AOI21 logic cell and applying transistor reordering



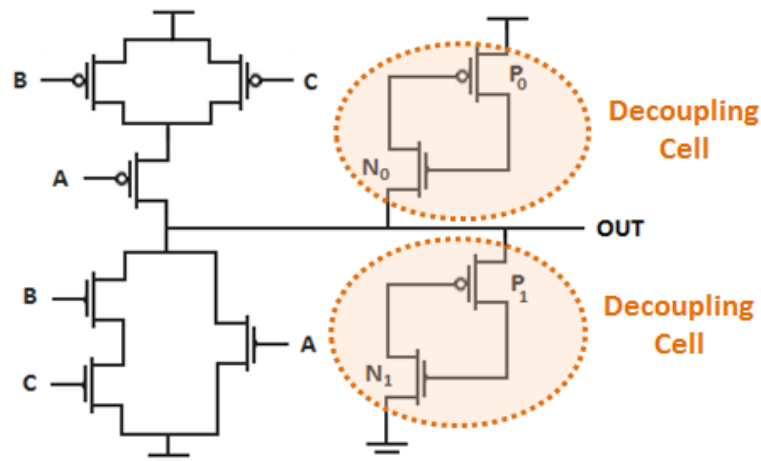
Source: From the author

### 3.3.2. Decoupling Cells

The addition of decoupling cells is a capacitive method commonly used in several industrial designs to ensure higher noise immunity on the supply rails and signal lines (EVANS et al., 2002) (SU et al., 2003). Decoupling cells are connected in the gate output, and they are composed of two transistors arranged in the cross-coupled mode, as shown in Figure 3.24 for the AOI21 cell. These cells increase the total capacitance in the output node, increasing the critical charge to produce a SET pulse, and making this node less susceptible to the impact of energetic particles. In (ANDJELKOVIC et al., 2018), this technique was used to filter SET pulses generated by low energy particles in a set of logic gates designed using the IHP's 130-nm bulk CMOS digital library with the fault injection through the double-exponential current at SPICE level.

Moreover, decoupling cells deliver current to the gates during the switching, protecting the circuits of the disturbances caused by process variations. For obtaining better results in relation to the mitigation, two decoupling cells are recommended in the design such that one cell is connected between the output and the supply rail while the other is placed between the output and ground rail. As the insertion of decoupling cells is a capacitive method, larger decoupling cells contribute even more for the attenuation of process variability and radiation-induced soft errors. The disadvantage involved is the area, and power consumption overheads due to the addition of four more transistors in the design.

Figure 3.24: Design of the AOI21 logic cell connecting decoupling cells in the output



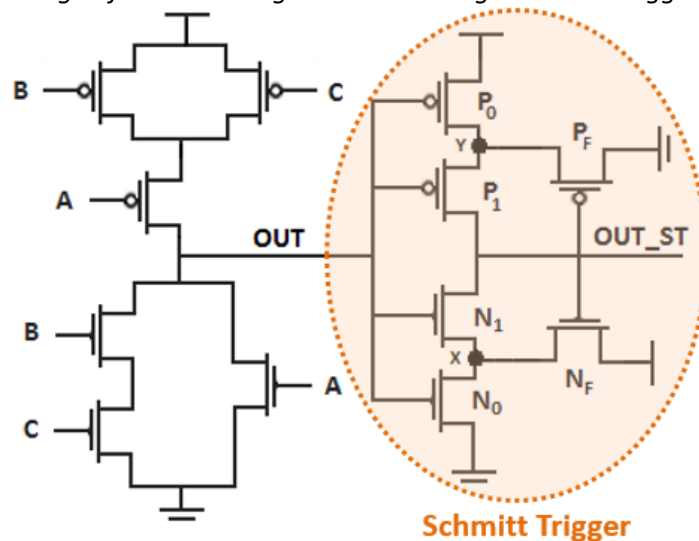
Source: From the author

### 3.3.3. Schmitt Trigger

Schmitt Triggers have an inherent hysteresis property commonly used to enhance signal stability and high noise immunity. This work explores a well-known topology of Schmitt Trigger where the main difference from the most common versions is the presence of  $P_F$  and  $N_F$  devices that are responsible for a feedback scheme, as shown in Figure 3.25 (LOTZE; MANOLI, 2017). For example, if the output is in a high level, the  $N_F$  transistor is on, pulling the node X to a high potential, forcing the drain-source voltage of transistor  $N_1$  almost zero, and its gate-source voltage into the negative region. This kind of topology reduces the leakage current in  $N_1$  exponentially, increasing the  $I_{ON}$ -to- $I_{OFF}$  current ratio, and minimizing the output degradation.

The main effect of process variability is a shift in the voltage transfer curve (VTC) due to the threshold voltage variation. The variability impact on VTC is reduced in the Schmitt Trigger as a result of the strong influence of the gate-source voltage of the inner transistors ( $N_1$  and  $P_1$ ) over its switching point. The replacement of traditional inverters by Schmitt Triggers on full-adders shows to be an attractive alternative to mitigate the effects of process variations on planar technologies (DOKANIA; ISLAM, 2015) (TOLEDO et al., 2018) and also for a FinFET technology (MORAES et al., 2018). The main drawback of this technique also is the area and power overheads due to the addition of six more transistors in the circuit.

Figure 3.25: Design of the AOI21 logic cell connecting a Schmitt Trigger in the output



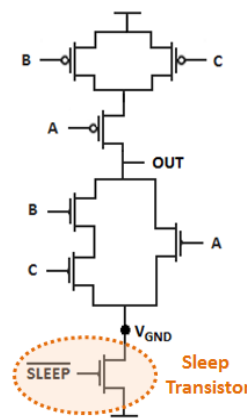
Source: From the author

### 3.3.4. Sleep Transistor

The power-gating is one strategy widely employed in low power designs to shut off circuit blocks that are not in use, improving the overall power on a chip (CALIMERA et al., 2015). The difference among the power-gating designs is the granularity of the blocks. This work focuses on a fine-grained model where a sleep transistor is added to every cell. However, for larger circuits, the block-grained style is more indicated to avoid the area overhead. Figure 3.26 illustrates the AOI21 cell with a sleep transistor placed between the pull-down network and the ground rail.

The sleep signal is used to control the ‘active’ (sleep = 0) and ‘idle’ (sleep = 1) states of the transistor. When the sleep transistor is in active mode, it guarantees a typical connection from the logic cell to the ground rail, acting as a supply voltage regulator. In the standby mode, the sleep transistor is turned off, disconnecting the virtual ground ( $V_{GND}$ ) from the physical ground. This behavior aims to reduce leakage currents, transient faults, and NBTI effects. Moreover, the addition of sleep transistors proved to be very efficient to mitigate the impact of process variations in planar technologies (REIS; CAO; WIRTH, 2015). However, two fundamental points must be considered to the sleep transistor technique to be successfully applied: 1) the correct control of the sleep signal; and 2) the adoption of proper sizing. The main disadvantage of this technique is the performance degradation when the sleep transistor is in the active mode, leading this path to become the worst-case delay of logic cells.

Figure 3.26: Design of the AOI21 logic cell using a sleep transistor



Source: From the author

# Chapter 4: Evaluation Methodology

---

The general objectives of this thesis are to evaluate the impact of process variability and soft errors at the physical level in FinFET logic cells besides to investigate circuit-level approaches to mitigate the effects caused by them. This chapter presents the methodological flow to achieve these goals. Moreover, the typical behavior of FinFET logic cells under process variability and soft errors, without any mitigation technique, also is discussed in this chapter.

The set of basic and complex cells evaluated in this work are INV, NAND2, NAND3, NAND4, NOR2, NOR3, NOR4, AOI21, OAI21, AOI211, and OAI211. The complex cells are defined as ones that have both serial and parallel transistor networks. The AND-OR-Inverter (AOI) are two-level of logic functions composed by one or more AND gates precede a NOR gate. The complementary of AOI cells is the OR-AND-Inverter (OAI) such that a NAND gate follows the OR gates. This set of logic gates was chosen for representing the most common cells among the standard libraries. More detailed information about them can be seen in Table 4.1.

*Table 4.1: Information about the FinFET logic cells*

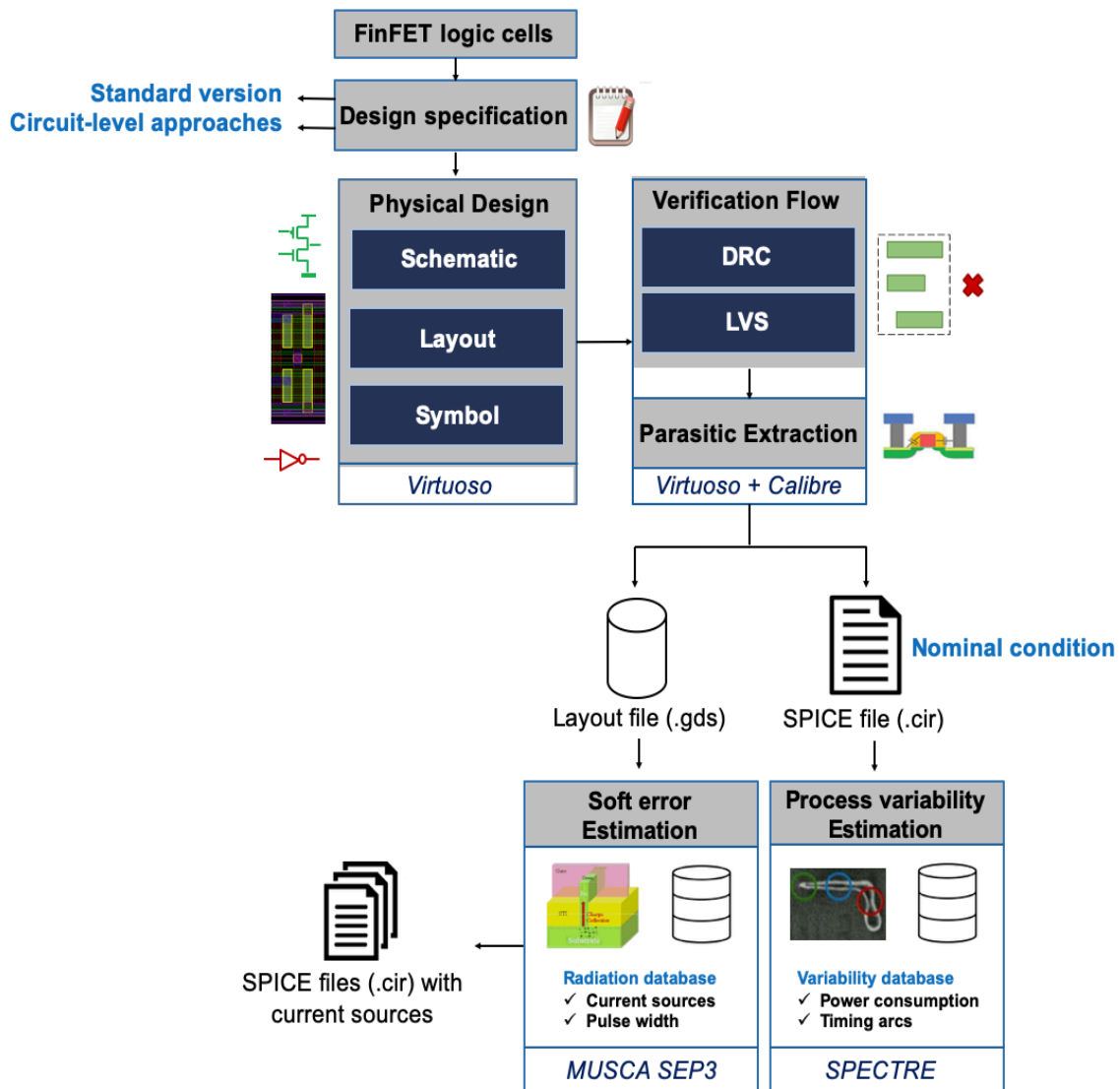
Gates	Number of Inputs	Number of Transistors	Area (nm <sup>2</sup> )
INV	1	2	50.9
NAND2	2	4	67.8
NAND3	3	6	84.8
NAND4	4	8	101.7
NOR2	2	4	67.8
NOR3	3	6	84.8
NOR4	4	8	101.7
AOI21	3	6	84.8
AOI211	4	8	101.7
OAI21	3	6	84.8
OAI211	4	8	101.7

*Source: From the author*

The design flow used in this work is presented in Figure 4.1. First, this design flow was performed considering the standard version of cells for comparison purpose, and after, the

schematic of each cell was changed using the circuit-level approaches described in Section 3.3 to obtain more reliable circuits. The standard version of complex cells considers the serial transistors close to the gate output according to most of the standard cell libraries. This work considers the same transistor sizing (three fins) for all transistors of the logic gates to avoid overly difficult routing or poor density (VASHISHTHA et al., 2017). The variation of transistor sizing (three to five fins) is only applied in the extra transistors imposed by decoupling cells, Schmitt Trigger, and sleep transistor techniques.

Figure 4.1: Design flow adopted in this work



Source: From the author



The logic cells pass by three elementary steps: physical design, verification flow, and parasitic extraction. In the physical design, the schematic, layout, and symbol of all logic cells were implemented using the Virtuoso tool from Cadence. Since logic cells are used several times in the same integrated circuit, a cell library is a way to save time and avoid errors in the physical design. The height of logic cells was set as 7.5, 9, and 10.5 tracks of metal 2 (M2) when transistors with three, four, and five fins are used in the design, respectively. This work follows this design pattern to allow the future development of a cell library focused on reliability issues.

After, each layout was submitted to the verification flow composed by a design rule check (DRC) and layout versus schematic (LVS) steps. DRC checks if the layout satisfies the design rules as width, pitch, spacing, area, overlap, and enclosure, required for the layers of a given technology. On the other hand, the LVS compares devices and connectivity presented in the schematic with those of the layout. In this work, DRC and LVS steps are based on the technology rules of the 7-nm FinFET PDK called ASAP7 developed by ASU in collaboration with ARM Ltd (CLARK et al., 2016). This PDK implements the shorted-gate model, where a TAP cell is used to connect the back-gate to the front-gate, ensuring proper functionality to transistors.

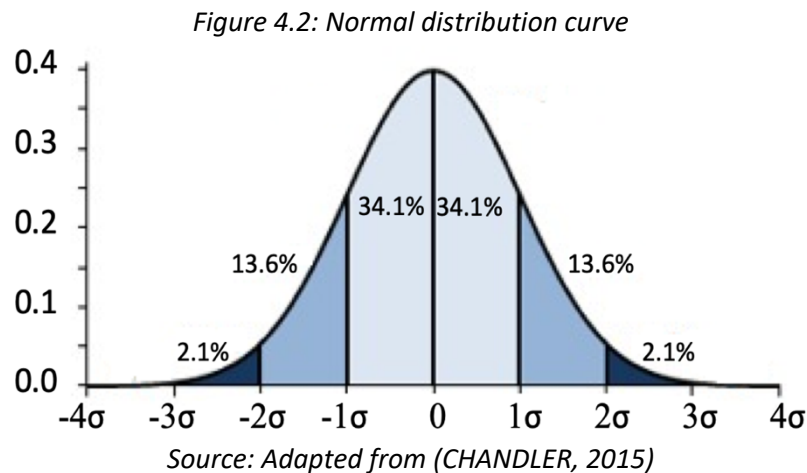
The layer information and the basic design rules of this PDK were summarized in Table 2.2 and Table 2.4. Finally, the parasitic wire resistances and capacitances (RC) are extracted from the layout. A new circuit netlist is generated such that each net has one subckt with the RC tree structure and the connections between the parasitic networks. Calibre tool from Mentor along with Virtuoso tool, were used to perform the verification flow and parasitic extraction steps. The geometric data stream (GDS) is a file generated by Virtuoso that represents all the geometric shapes of layout design in the binary format. This file can be used to reconstruct all or part of a layout, to transfer the layout between different tools, or to create photomasks for the fabrication process.

A SPICE file was created with all details to perform electrical simulations such as input waves, supply voltage, all metrics to be measure (power, propagation delays, currents), technological model and the new netlist coming from the parasitic extraction step. This work considers FinFETs in a bulk substrate for all experiments. For a more realistic assessment, all logic cells drive a fan-out 4 (FO4). Moreover, two inverters are connected to each input to

represent a load. The SPICE file is simulated to verify the nominal conditions, i.e., the behavior of each cell without process variability or radiation effects. All the electrical simulations were carried out using SPECTRE from Cadence. The details about process variability insertion and radiation analysis will be discussed in the next subsections.

## 4.1 Process Variability Evaluation

Monte Carlo (MC) is the most common method used to model the probability of different outcomes that cannot easily be predicted due to the many random variables involved. According to (ALIOTO; CONSOLI; PALUMBO, 2015), two thousand MC simulations is enough to obtain accurate results in the variability analysis. For these reasons, this thesis considers two thousand MC simulations performed in SPECTRE from Cadence to estimate the behavior of FinFET logic cells under process variations. As presented in Chapter 3, work-function (WF) is the most impacted parameter by process variability in FinFET technologies. In this work, the WF is modeled as a Gaussian function, assuming 3-sigma ( $\sigma$ ) deviation, which represents 99.7% of the normal distribution curve, as shown in Figure 4.2.



All logic cells were evaluated using levels of WFF varying from 1% to 5% due to the lack of information from industry about the levels of WFF in current FinFET technologies. These variations were adopted as a reference to the nominal values of regular threshold voltage (RVT) model from ASAP7 at typical (TT) configuration. The geometric parameters and doping

information of this model can be seen in Table 2.2. The variability database provides a summary of statistical results from MC simulations such as the minimum (min), and maximum (max) values, mean ( $\mu$ ) and standard deviation ( $\sigma$ ) for all timing arcs and also for power consumption.

The standard deviation quantifies the variation of a set of data from the nominal conditions. A low standard deviation indicates that the data is closer to the mean. Despite the data provided by the variability database for delay and power metrics, this work also adopted two figures of merit to allow a more detailed comparison: 1) the normalized standard deviation ( $\sigma/\mu$ ) to indicate the sensitivity of logic cells to the WF fluctuations; and 2) the delta relation ( $\Delta$ ) to specify how much the sensitivity to process variation changes when logic cells are designed using a circuit-level mitigation approach instead of the standard version.

The  $\sigma/\mu$  relation was calculated for all timing arcs. From this, there are two ways to evaluate the delay variability. First, the higher  $\sigma/\mu$  relation among all timing arcs is considered, and after, the  $\sigma/\mu$  relation of the worst-case delay is used as a reference (the propagation delay with the largest mean). This thesis presents the results of delay variability considering both methodologies. The relative deviations in power and delay metrics are estimated comparing the nominal values (without any variation) with the mean values of Monte Carlo simulations.

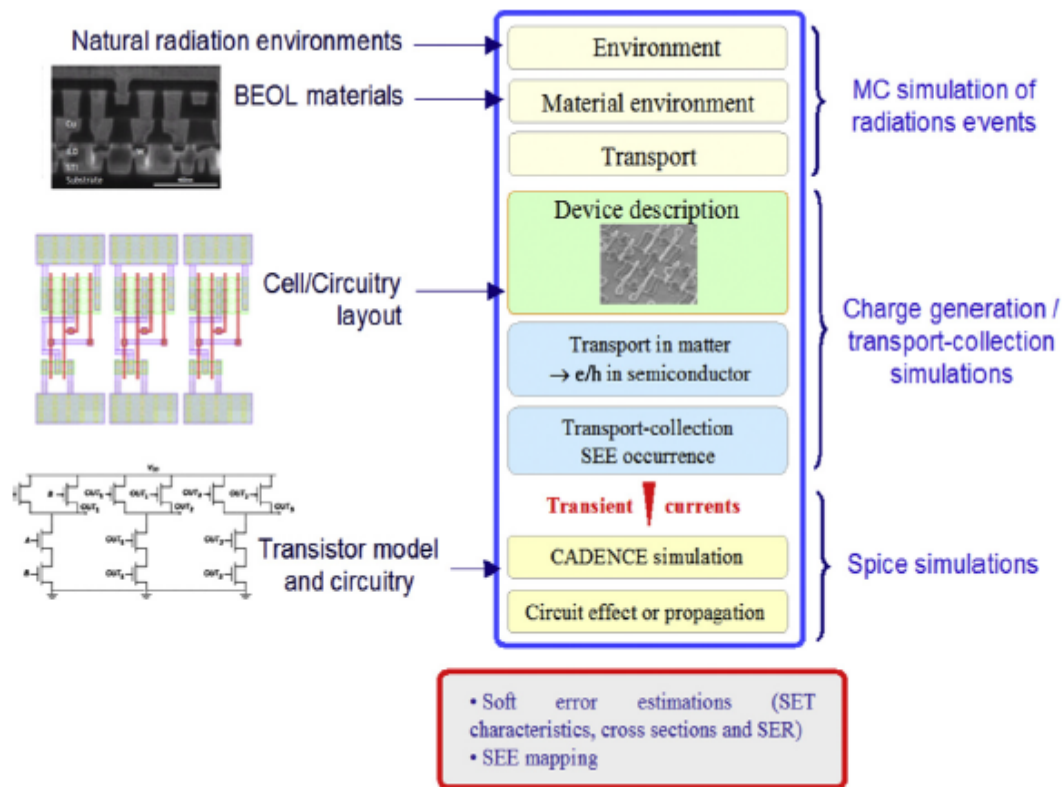
For example, the AOI21 logic cell was designed considering the standard version, and also adopting the four circuit-level techniques presented in Chapter 5. Each design has a different  $\sigma/\mu$  relation for delay and power metrics. A design is pointed out as the best choice to mitigate the delay or power variability if it has the lowest value for the  $\sigma/\mu$  relation. On the other hand, the delta relation compares the  $\sigma/\mu$  relation of the standard version with each of those obtained using circuit-level approaches. A technique is classified as favorable to power or delay variability mitigation if the delta relation has positive values. The same idea was followed to evaluate the other logic cells.

## 4.2. Soft Error Estimation

The soft error susceptibility of FinFET logic cells was estimated using the MUSCA SEP3 tool developed by ONERA, the French Aerospace Lab (HUBERT et al., 2009) (ARTOLA et al., 2013). MUSCA SEP3 is a radiation event generator tool, also based on the Monte Carlo method, which

models all stages since the strike of an energetic particle into the matter, until the manifestation of a transient pulse on the circuits. The radiation particles available for analysis are the neutrons, protons, heavy-ions, muons, and alpha particles. This tool takes into account the targeted radiation environment (space, avionics, ground), radiation features (LET, angle of incidence, type of energetic particle), dynamic transport and charge collection mechanisms, the bias voltage, the layout characteristics, the circuit electrical response, the STI oxide, and the details of manufacturing process. Figure 4.3 summarizes the design flow executed by the MUSCA SEP3 tool.

Figure 4.3: MUSCA SEP3 prediction flow for FinFET technology nodes



Source: (ARTOLA; HUBERT; ALIOTO, 2014)

The collection charge of each transistor is calculated based on the layout of the device, which can be extracted from a reverse engineering or using the FEOL report from the GDSII file. The modeling transport and the collection of free carriers in the silicon are performed using 3D analytical models, through the BEOL information, that adopts the following mechanisms:

ambipolar diffusion, dynamic collection, multi-collection bipolar amplification to evaluate the charge sharing and pulse quenching phenomenon, recombination, and bias dependence. The impact of the temperature (down to 50K) is considered to all the physical and electrical models used for the transport and collection of charge in the semiconductors. The model implemented for the bipolar amplification depends of two aspects. First, the model uses the equivalent access resistances of the multigate device to determine the triggering of the bipolar transistor. Also, the model considers the variability of the amplification of charge collection as a function of LET due to the FinFET technologies.

The SET database generated by the tool is very accurate since it considers all characteristics presented above. To each different setup, a new SET database is created. Once done, it is composed of a set of current sources to be injected in the sensitive nodes, i.e., the drain of transistors. The fault injection is performed automatically using a script along with SPECTRE from Cadence. After, the results are evaluated to determine the soft error susceptibility of the circuits.

This work explores the heavy-ion irradiation at a normal angle of incidence, room temperature (27°C), and with the supply voltage varying from the nominal value (0.7V) down to the near-threshold regime (0.3V). NOR2, NAND2, and AOI21 logic cells were evaluated under low LET, i.e., less than  $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , which corresponds to the representative secondary particles induced by neutrons or protons in avionics and ground applications. The SE susceptibility also was investigated under higher LETs (30 and 58  $\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ) representing the space environment. For obtain a more accurate estimation, the SET database was simulated for all input vectors. Moreover, the output of each cell is connected to a chain of four inverters, allowing the evaluation of propagation effects. A fault is accounted if the voltage amplitude of the output node exceeds the gate threshold voltage ( $V_{DD}/2$ ). This work adopts the cross-section ( $\sigma_{cs}$ ) as the central figure of merit to estimate the SE susceptibility of logic cells. This metric quantifies the probability of an energetic particle crossing the area of  $1\text{cm}^2$  and to produce a transient event. The relation between the SE susceptibility and the SET pulse width also were analyzed in this work.

## 4.3. Typical Behavior of FinFET Logic Cells

This section explores the behavior of FinFET logic cells at nominal conditions, and also under the effects of process variability and radiation-induced soft errors. In this analysis, the standard version of logic cells was evaluated without any circuit-level mitigation technique. The results presented in this chapter seek: 1) to reinforce that process variations and soft errors can modify the behavior of logic cells significantly, and consequently, 2) to highlight the importance of proposing techniques able to mitigate the effects caused by these challenges. Moreover, the results of this section will be used as a reference point to estimate how much the adoption of circuit-level approaches in the design improves the robustness of logic cells.

### 4.3.1. Effects of process variability

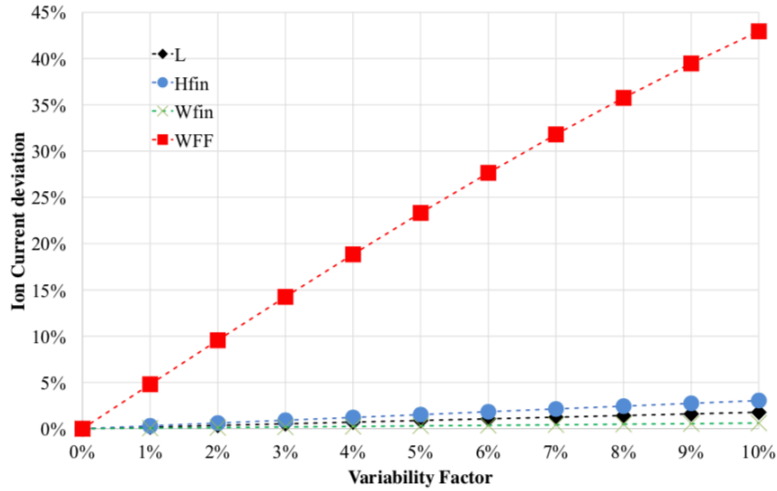
Process variability is a random deviation in the device structure, which causes an increase or decrease of typical design specifications. These deviations can affect the reliability of circuits because it modifies the  $I_{ON}/I_{OFF}$  currents, the power consumption, the performance, the threshold voltage, and the LET threshold to induce a soft error. First, this section presents an overview of the impact of LER and MGG variations on the  $I_{ON}/I_{OFF}$  currents of FinFET devices. After, the power consumption and propagation delay metrics of FinFET logic cells are evaluated under WF fluctuations.

#### 4.3.1.1. Characterization of devices from ASAP7 under process variations

The influence of deviations in the gate length ( $L_G$ ), fin height ( $H_{FIN}$ ), fin width ( $W_{FIN}$ ), and work-function (WF) due to LER and MGG variabilities were evaluated, focusing on the  $I_{ON}/I_{OFF}$  currents of PFET and NFET devices from ASAP7.

Figure 4.4 illustrates the impact of process variations on the  $I_{ON}$  current of NFET devices with the minimum transistor sizing (1 fin). For the geometric parameters, even considering 10% of deviation from nominal conditions, the impact on  $I_{ON}$  current is small, i.e., less than 5%. On the other hand, low levels of WF fluctuations already introduces at least 5% of deviation on the  $I_{ON}$  current. The impact of WF fluctuations on the  $I_{ON}$  current grows linearly with the increase in the levels of variation.

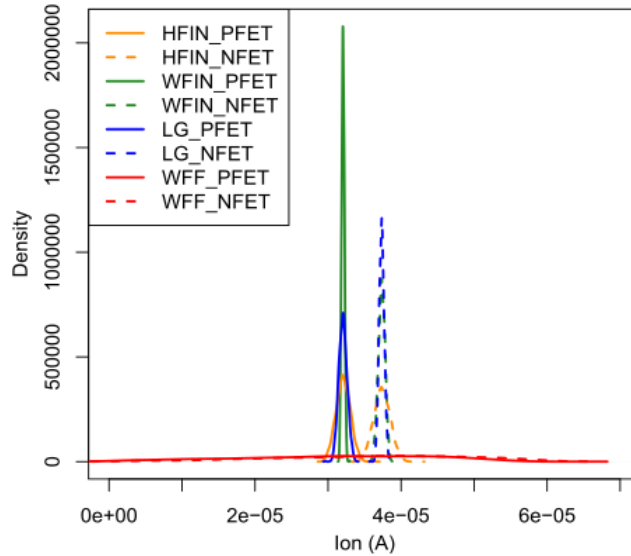
Figure 4.4: Impact of geometric and WF variations on the  $I_{ON}$  current



Source: Adapted from (BRENDLER et al., 2019)

The density curves for the Monte Carlo simulations of each individual parameter, considering 10% of process variation, are shown in Figure 4.5, for the  $I_{ON}$  current. It is possible to observe that geometric parameters present denser results due to the small deviations. PFET devices are less dense than NFET devices, such that the data is further to the mean. However, WF fluctuations show a significant deviation, with the impact on the  $I_{ON}$  current ranging from nano to micro-amperes.

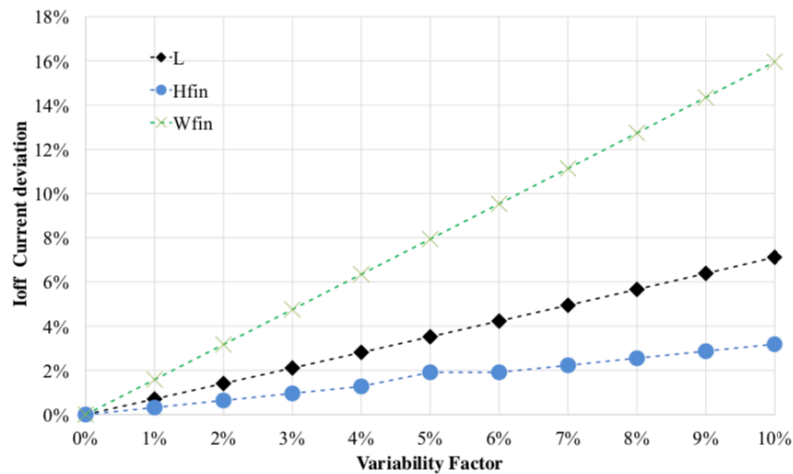
Figure 4.5: Density curves of the  $I_{ON}$  current under process variations



Source: Adapted from (BRENDLER et al., 2019)

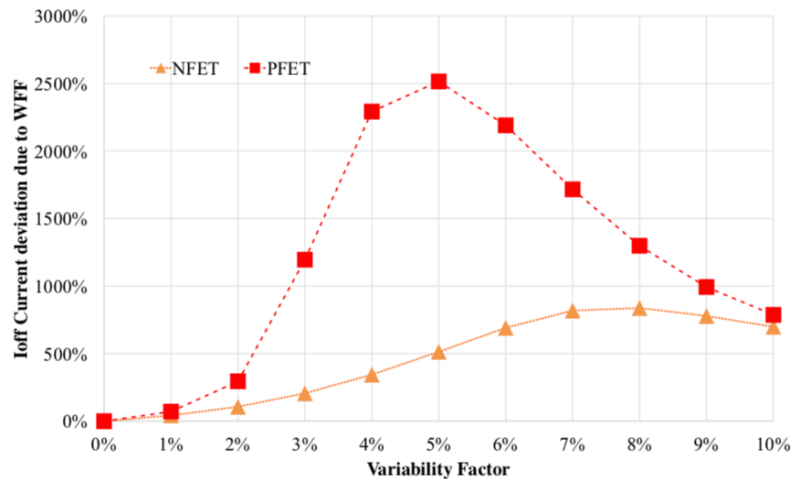
Among the statistical variability on the geometric parameters, the deviation of  $H_{FIN}$  and  $L_G$  modifies the  $I_{OFF}$  current up to 3% and 7%, respectively, as shown in Figure 4.6. However, the roughness in the  $W_{FIN}$  may provoke more than 10% of deviation if the fabrication process introduces more than 5% of process variation. Figure 4.7 shows the influence of WF fluctuations on the  $I_{OFF}$  current for PFET and NFET devices. The WF fluctuations produce  $I_{OFF}$  currents drastically higher than the nominal behavior, mainly for PFET devices. Some of these highest values can be considered inaccurate because they are very similar to the  $I_{ON}$  currents, but regardless, the WF already was pointed out as the most impacted parameter by process variations in FinFET technologies.

Figure 4.6: Impact of geometric variations on the  $I_{OFF}$  current



Source: Adapted from (BRENDLER et al., 2019)

Figure 4.7: Impact of work-function fluctuations on the  $I_{OFF}$  current

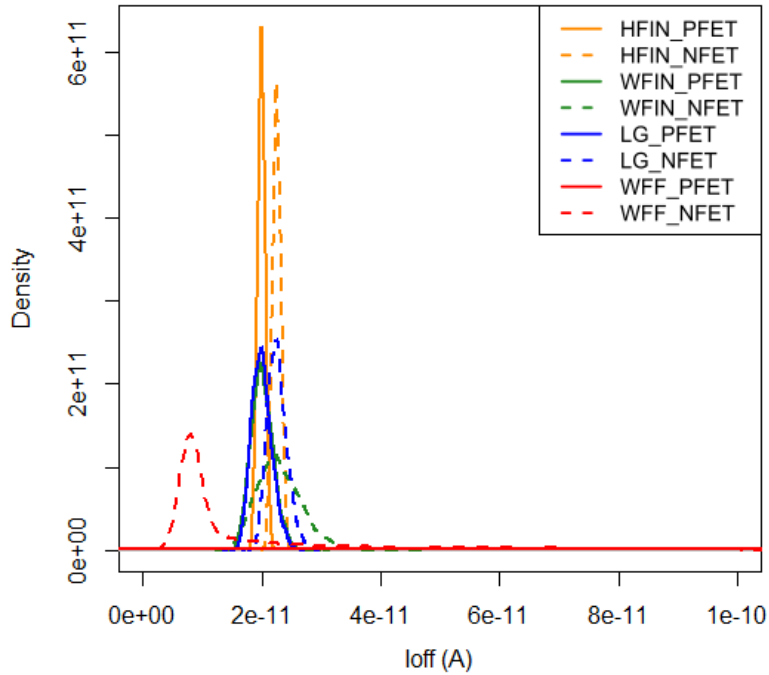


Source: Adapted from (BRENDLER et al., 2019)



The density curves for the  $I_{OFF}$  current under process variations are presented in Figure 4.8 for both devices. Geometric parameters, such as gate length and fin width, demonstrate a reduction on the density for PFET devices while the fin height becomes denser. However, NFET devices are more impacted by the fin width variations, presenting a wider density curve. The WF fluctuations show large deviation mainly for PFET devices, even at small levels of variation.

Figure 4.8: Density curves for the  $I_{OFF}$  current under process variation



Source: From the author

The characterization of devices adopting the electrical model provided by ASAP7 is consistent with those obtained using other multigate technologies (MEINHARDT; ZIMPECK; REIS, 2014a). The work-function fluctuations dominate the impact on the  $I_{ON}/I_{OFF}$  currents of FinFET devices. The increase in the number of fins is a way to protect the devices against geometric variations, but this methodology not work to attenuate the WF fluctuation effects. For this reason, henceforward, this thesis always adopts the work-function fluctuations for all process variability assessments.

### 4.3.1.2. Sensitivity to process variations

The WF fluctuations on FinFET devices can generate power and delay deviations. These deviations are estimated using the normalized standard deviation ( $\sigma/\mu$  relation). In this work, we adopt the terminology ‘power variability’ and ‘delay variability’ to indicate the deviations on power and delay due to WF fluctuations, respectively.

Table 4.2 and Table 4.3 show the typical values for the propagation delay ( $\sigma/\mu$  relation of worst-case) and power consumption of each gate, respectively, at nominal conditions (nom) and under WF fluctuations from 1% to 5%. As expected, there is an increase in the sensitivity of logic cells to the process variation ( $\sigma/\mu$ ) when higher levels of WF fluctuations were explored for both metrics. Logic cells with a larger number of inputs are less robust to WF fluctuations. For example, the NAND4 is at least 9.2% and 20.6% more sensitive than NAND2 to the delay and power variability, respectively.

Comparing the sensitivity of basic cells, the NOR cells are more impacted by process variations than NAND cells. In relation to the complex cells, the AOI21 and OAI211 cells are more robust to delay variability than OAI21 and AOI211 cells. These cells have a similar behavior to the power variability, except when the AOI21 cell suffers 1-3% of deviation, and the OAI211 cell has 5% of variation from nominal values. In general, FinFET logic cells are more sensitive to delay variability for deviations up to 4%, but an opposite behavior can be verified for variations from 5%, i.e., the logic cells become more susceptible to power variability. Moreover, variations of 5% almost triple the sensitivity of logic cells to power variability when compared with 4% of deviation. The mean ( $\mu$ ) of MC simulations at standard version is considered later to estimate the penalties imposed by circuit-level mitigation techniques.

The impact of delay variability also can be evaluated using the higher  $\sigma/\mu$  relation among the timing arcs of each logic cell. As shown in Table 4.4, except for the inverter, the sensibility of all logic cells become bigger. Moreover, the mean of MC simulations is smaller. This happens because the higher  $\sigma/\mu$  relation among the timing arcs normally not corresponds to the worst-case delay. However, the most statements previously presented using the  $\sigma/\mu$  relation of worst-

case delay may still be considered. The main difference is that AOI21 cell is less sensitive than OAI21 only with 1% of deviation.

*Table 4.2: Propagation delay at nominal conditions and under WF fluctuations adopting as metric the  $\sigma/\mu$  relation of worst-case delay*

Gates	nom (ps)	1%		2%		3%		4%		5%	
		$\mu$ (ps)	$\sigma/\mu$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)
INV	6.3	6.3	4.42	6.4	10.46	6.6	18.01	6.9	25.58	7.2	34.02
NAND2	9.6	9.6	4.02	9.8	9.25	10.0	15.93	10.4	22.51	10.7	29.10
NAND3	14.2	14.2	4.43	14.5	11.12	14.9	18.26	15.4	24.76	16.0	31.35
NAND4	19.2	19.3	4.86	19.7	12.45	20.4	19.44	21.1	25.65	21.8	32.05
NOR2	12.6	12.8	6.79	13.2	16.21	13.7	23.68	14.2	30.91	14.8	39.90
NOR3	19.9	20.3	9.32	21.1	18.06	21.8	24.70	22.5	31.64	23.4	40.64
NOR4	28.1	28.9	10.74	29.9	18.34	30.8	24.64	31.7	31.54	32.9	40.60
AOI21	14.1	14.2	6.87	14.7	15.83	15.2	23.10	15.7	30.35	16.4	39.53
AOI211	21.9	22.4	9.10	23.2	17.48	23.9	24.12	24.7	31.19	25.6	40.45
OAI21	14.2	14.3	6.99	14.8	15.97	15.3	23.25	15.8	30.55	16.5	39.80
OAI211	15.7	15.8	7.33	16.4	16.08	16.9	23.23	17.4	30.58	18.1	40.02

*Source: From the author*

*Table 4.3: Power consumption at nominal conditions and under WF fluctuations*

Gates	nom (nW)	1%		2%		3%		4%		5%	
		$\mu$ (nW)	$\sigma/\mu$ (%)	$\mu$ (nW)	$\sigma/\mu$ (%)	$\mu$ (nW)	$\sigma/\mu$ (%)	$\mu$ (nW)	$\sigma/\mu$ (%)	$\mu$ (nW)	$\sigma/\mu$ (%)
INV	427	431	3.39	434	7.07	442	11.92	455	20.84	485	51.83
NAND2	540	534	2.92	539	6.13	547	10.22	562	18.26	596	49.19
NAND3	591	607	3.56	613	7.42	624	12.18	643	21.28	689	56.05
NAND4	663	668	4.09	676	8.45	689	13.79	714	23.95	769	61.97
NOR2	532	543	3.38	548	6.77	556	10.95	571	18.98	606	49.20
NOR3	626	628	3.98	634	8.21	645	13.20	666	22.05	711	53.28
NOR4	691	698	4.64	707	9.52	722	15.24	747	24.90	803	57.51
AOI21	615	642	3.34	648	6.58	658	10.79	676	18.90	718	49.89
AOI211	649	651	3.93	658	8.10	670	13.22	692	22.77	743	58.03
OAI21	575	576	3.21	580	6.37	589	10.52	606	19.32	646	55.40
OAI211	605	606	3.35	611	6.92	621	11.50	640	21.46	689	62.20

*Source: Adapted from (ZIMPECK et al., 2019a)*

Table 4.4: Propagation delay at nominal conditions and under WF fluctuations adopting as metric the higher  $\sigma/\mu$  relation

Gates	nom (ps)	1%		2%		3%		4%		5%	
		$\mu$ (ps)	$\sigma/\mu$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)
INV	6.3	6.3	4.42	6.4	10.46	6.6	18.01	6.9	25.58	7.2	34.02
NAND2	7.1	7.1	4.61	7.2	10.83	7.4	18.15	7.7	25.50	8.0	33.98
NAND3	12.4	12.5	4.88	12.8	12.23	13.2	20.06	13.7	27.05	14.3	34.49
NAND4	15.9	16.0	5.58	16.5	14.43	17.2	22.42	17.8	29.33	18.6	36.38
NOR2	11.8	11.9	6.79	12.4	17.14	12.9	24.94	13.4	32.42	14.0	41.70
NOR3	17.5	18.0	10.36	18.8	19.96	19.5	27.11	20.2	34.53	21.1	44.16
NOR4	23.5	24.4	12.51	25.4	21.12	26.2	28.11	26.2	35.71	28.3	45.70
AOI21	11.8	11.9	7.30	12.4	17.17	12.9	24.97	13.4	32.45	14.0	41.75
AOI211	17.6	18.0	10.38	18.8	19.98	19.5	27.13	20.2	34.55	21.1	44.17
OAI21	13.4	13.5	7.35	14.0	16.77	14.5	24.35	15.0	31.89	15.6	41.45
OAI211	15.2	15.0	7.67	15.5	16.81	16.1	24.22	16.6	31.80	17.3	41.54

Source: Adapted from (ZIMPECK et al., 2019a)

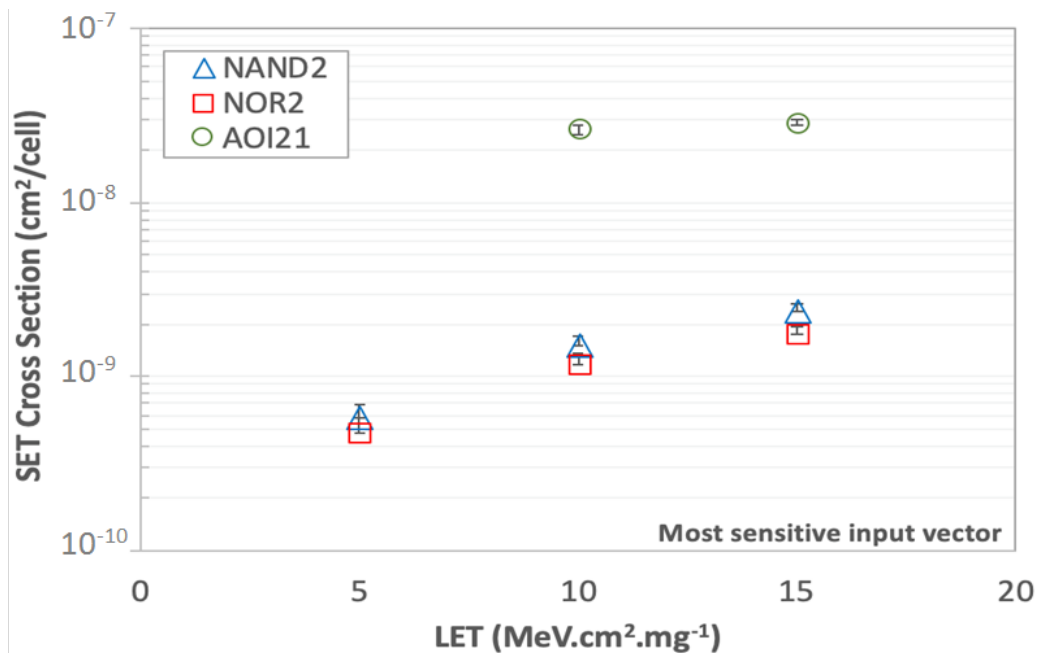
### 4.3.2. Susceptibility to Soft Errors

Soft errors are transient events with a short time interval induced by energetic particles coming from terrestrial and space radiations. Radiation-induced soft errors may cause critical failures on system behavior, which can lead to financial or human life losses. This section evaluates the impact of soft errors in three FinFET logic cells under low LET values, i.e., less than  $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ . These LET values have been targeted because correspond to secondary particles induced by neutrons at avionic and ground applications. The metric for soft error evaluation is the SET cross section considering the most sensitive input vector and also the mean of all input vectors.

Figure 4.9 shows the soft error susceptibility of NAND2, NOR2, and AOI21 cells at near-threshold regime (0.3V) considering the most sensitive input vector. For all LETs investigated, the three logic gates are free of faults at 0.6V and core voltage. The AOI21 cell is free of faults with a LET of  $5\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , and soft errors are only seen in the output of NAND2 and NOR2 cells at 0.3V. On the other hand, it is possible to observe some faults at 0.4V and 0.5V when higher LET ( $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ) was investigated. The reduction of number of faults happens due

to the FinFET disruptive nature that increase the minimum charge required to induce a SET pulse. Moreover, this behavior is consistent with the previous work obtained for the same technology on majority voters (AGUIAR et al., 2017).

Figure 4.9: SET cross section of logic cells operating at near-threshold regime considering the most sensitive input vector



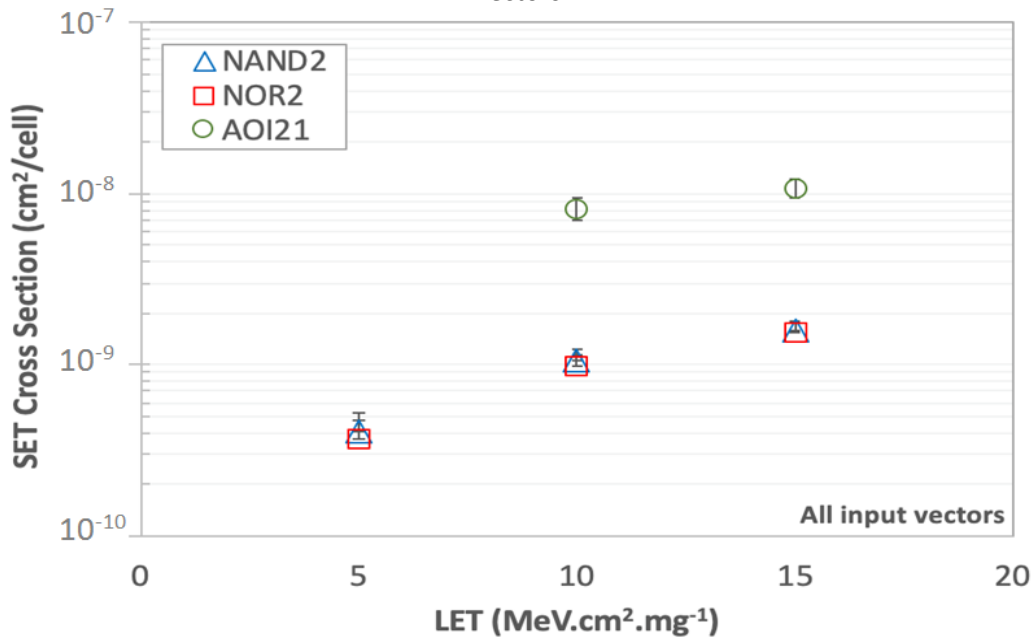
Source: From the author

The logic cell more susceptible to soft errors is the AOI21 because most of the current sources from the SET database generated visible faults at the output. However, the increase of the LET from 10 to 15MeV.cm<sup>2</sup>.mg<sup>-1</sup> does not impact significantly the cross section. On the other hand, the increase of the cross section of basic cells is almost linear to the increase of LET according to Figure 4.9. The simulations indicate a higher SET cross section to the NAND2 cell, such that it also agrees with the previous work that uses the ASAP7 model (AGUIAR et al., 2017). The NOR2 cell is around 17.4%, 21.7%, and 25.5% more robust than NAND2 cell to soft error impact for LETs equal to 5, 10, and 15MeV.cm<sup>2</sup>.mg<sup>-1</sup>, respectively.

Figure 4.10 demonstrates the same analysis, but the cross section was calculated using the mean of faults for all input vectors. It is possible to note that the susceptibility of basic cells to

soft error is very similar when all input vectors were considered. Moreover, the SET cross section of AOI21 cell decreases around 65% for both LETs because the other input vectors manifested fewer faults compared to the most sensitive input vector. The error bars in all SET cross section graphs are defined as one divided by the square root of the number of SETs representing the statistical error induced by Monte Carlo simulations (HUBERT; ARTOLA, 2013).

Figure 4.10: SET cross section of logic cells operating at near-threshold regime considering all input vectors



Source: From the author

# Chapter 5: Process Variability and Soft Error Mitigation

---

This chapter evaluates the use of circuit-level approaches in the design of FinFET logic cells to improve the process variability effects and the soft error susceptibility. In addition to the benefits of each technique, this chapter also presents the mitigation tendency when different levels of WF fluctuations, transistor sizing, and LET values were used. The results presented in this chapter seek: 1) to prove the efficiency of the four circuit-level mitigation approaches investigated in this thesis considering different test scenarios, 2) to indicate the pros and cons in adopting each one of them, and 3) to provide an overall comparison to allow the designers to choose the best technique depending on the target application.

## 5.1. Design with Circuit-Level Design Approaches

Transistor reordering and the adoption of decoupling cells, Schmitt Triggers, and sleep transistors are the four circuit-level techniques explored in the next subsections. In general, all approaches demonstrate interesting results to control the process variation and the soft error susceptibility. Furthermore, this work also provides a trade-off evaluation considering power consumption, performance, and area penalties.

### 5.1.1. Transistor Reordering

Transistor reordering is a simple technique based on rearranged transistor networks keeping the same logic function. Different transistor combinations change the electrical and physical characteristics of logic cells, and consequently, it also modifies the susceptibility to process variations and radiation-induced soft errors. As an example, Figure 5.1 shows the schematic and the layout of the two possible FinFET implementations of AOI21 cell with three fins. The reordering of transistor 'A' maintains the same layout width, just increasing the amount of metal 1 (M1) to do the new connections correctly. The reordering of transistors 'B' and 'C' is not necessary because it does not change the electrical behavior of AOI21 logic cell. In this way, we did the same reordering for other complex cells, such as OAI21, AOI211, and OAI211. Both implementation versions of these logic cells also keep the same layout width.

Figure 5.1: Schematic and layout of AOI21 cell implemented at standard version and using the transistor reordering technique

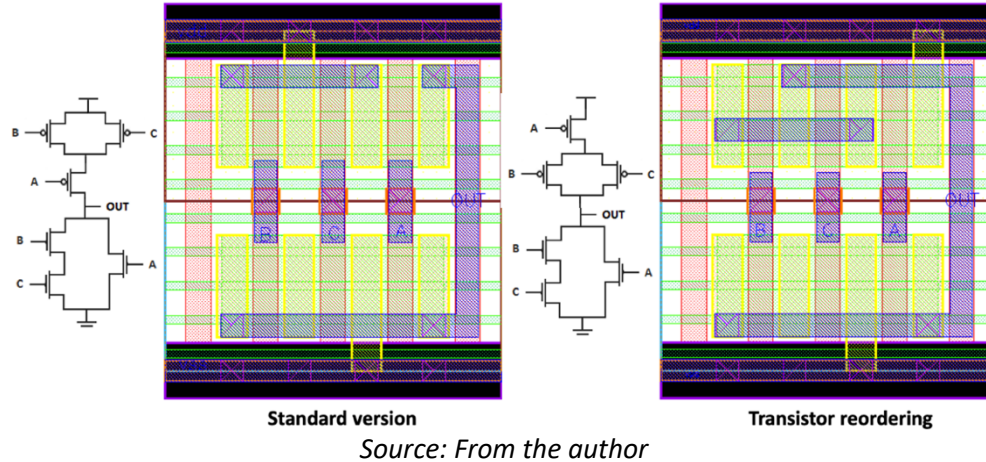
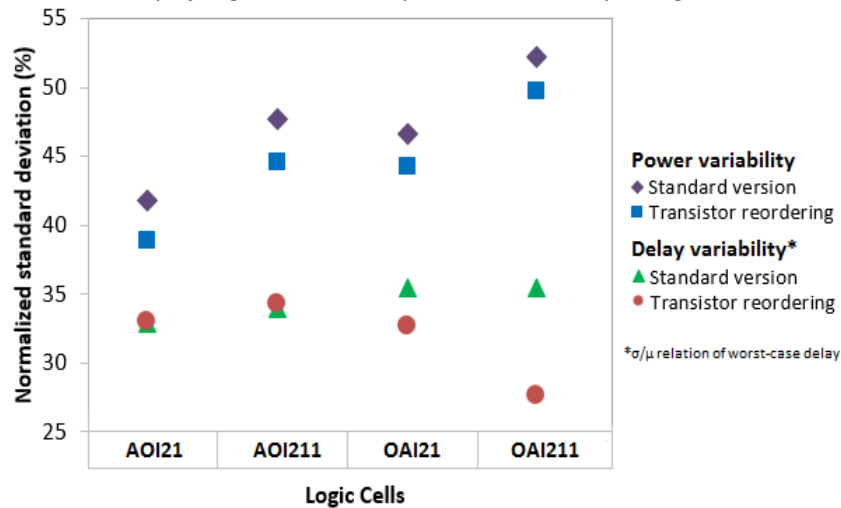


Figure 5.2 shows the sensitivity of logic cells designed at standard version and using the transistor reordering technique, under 5% of WF deviation from nominal conditions. For the delay variability, the metric used was the  $\sigma/\mu$  relation of worst-case delay. The placement of serial transistors as far as possible to the cell output (like the version presented in the right of Figure 5.1) improves at least 4.9% the robustness of logic cells to the power variability, reaching 7% for the AOI21 cell. On the other hand, the attenuation of delay variability is only achieved if the transistor reordering is applied on the OAI cells. The transistor reordering enhanced the delay variability robustness around 8% and 22.1% for the OAI21 and OAI211 cells, respectively.

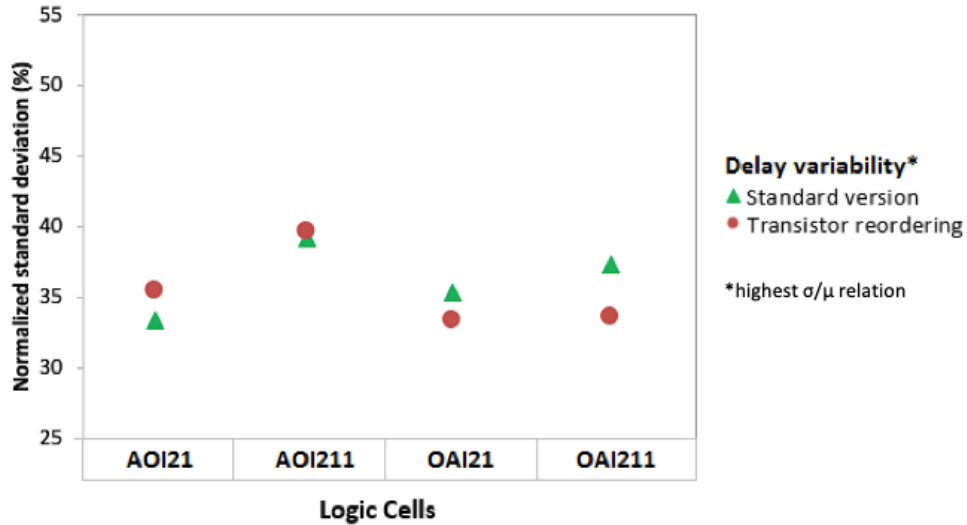
Figure 5.2: Sensitivity of logic cells to the process variability using transistor reordering





The delay variability also can be measured using the highest  $\sigma/\mu$  relation among all timing arcs of each logic cell, as illustrates the Figure 5.3. The tendency of sensitivity is the same, the transistor reordering remains disadvantageous for attenuate the delay variability of AOI cells. However, the robustness gain in adopting the transistor reordering technique is smaller, around 5.6% for the OAI21 logic cell and 10% for the OAI211 logic cell.

Figure 5.3: Sensitivity of logic cells to the delay variability using transistor reordering



Source: From the author

The influence of transistor reordering technique to the process variability mitigation was published in (ZIMPECK et al., 2018). The results are obtained adopting the HSPICE from Synopsys and the first version of ASAP7 PDK. As all other techniques evaluated in this thesis used the SPECTRE from Cadence as well as the last version of ASAP7 PDK, the experiments were re-simulated to ensure a fair comparison. For these reasons, there are some differences between the values presented here and, in the paper, but the design flow is the same.

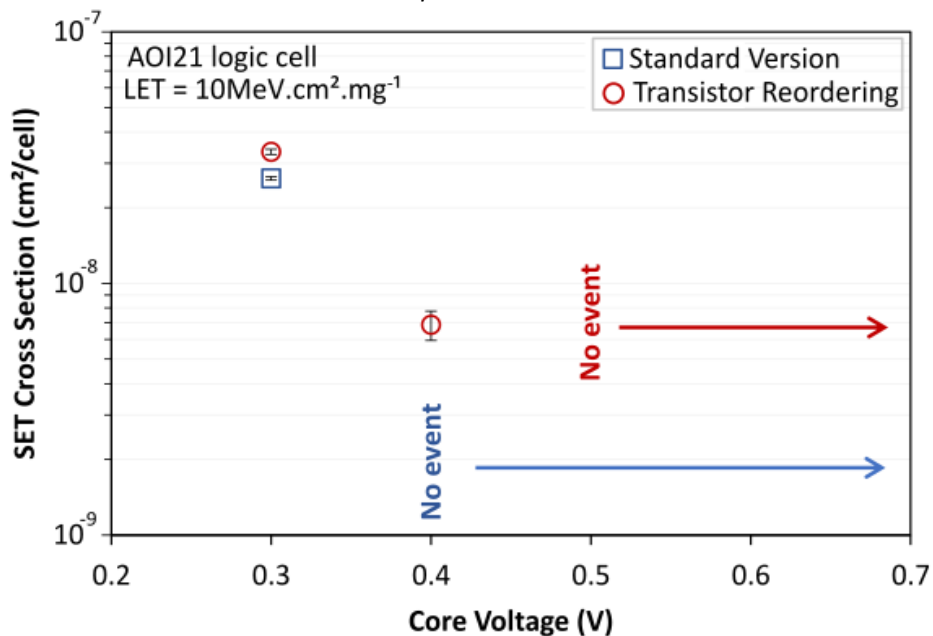
The transistor reordering technique does not add any extra transistor, such that all modifications happen in the transistors themselves from the standard version. For this reason, the influence of the number of fins has not been evaluated. Moreover, when this technique was evaluated with levels of WF fluctuations varying from 1% to 4%, the improvements in power and delay variability were less than 2%. Thus, as statistically is not advantageous to apply this technique for these levels of variation, the results are not presented in this thesis.

### 5.1.1.1. Soft Error Susceptibility

A comparison between the SET cross section of AOI21 cell considering the standard version and the transistor reordering technique is shown in Figure 5.4 for most sensitive input vector and a LET of  $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ . For this LET, both topologies show none events on the range from 0.5V to the nominal voltage (0.7V). Consequently, the choice of different transistor arrangements in the AOI21 cell for these supply voltages does not influence its susceptibility to soft errors.

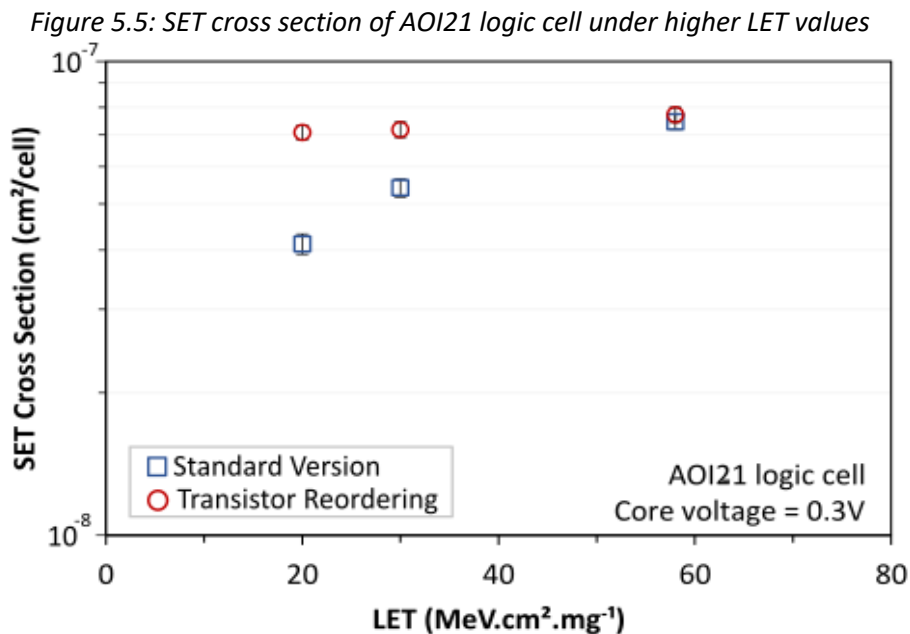
At near-threshold regime (0.3V-0.4V), the transistor reordering putting the serial transistors as far as possible to the output is not favorable to mitigate the soft error susceptibility. The AOI21 cell is 20% more robust to soft errors if the standard version is kept in the design. For LETs below to  $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , both topologies are free of faults independently of the core voltage. The results for  $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$  are omitted due to the similarity with the  $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ .

Figure 5.4: SET cross section of AOI21 cell under a LET of  $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$  considering most sensitive input vector



Source: Adapted from (ZIMPECK et. al, 2019b)

Figure 5.5 shows the cross section for the AOI21 cell operating at near-threshold regime (0.3V) as a function of LETs up to 58  $\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ . First, it is important to note that the standard version continues to be less sensitive than the design with transistor reordering for all levels of LET investigated. The soft error susceptibility using the standard version is smaller by around 37%, 24% and 5% for LETs equal to 20, 30 and 58  $\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , respectively. Another interesting factor is that the advantage in using the standard version decreases for higher LETs. Both topologies under higher LET values also were tested considering the core voltage varying from 0.4V to 0.7V, but no events were detected in the output of AOI21 cell. In summary, the transistor reordering is not a favorable technique for soft error mitigation.

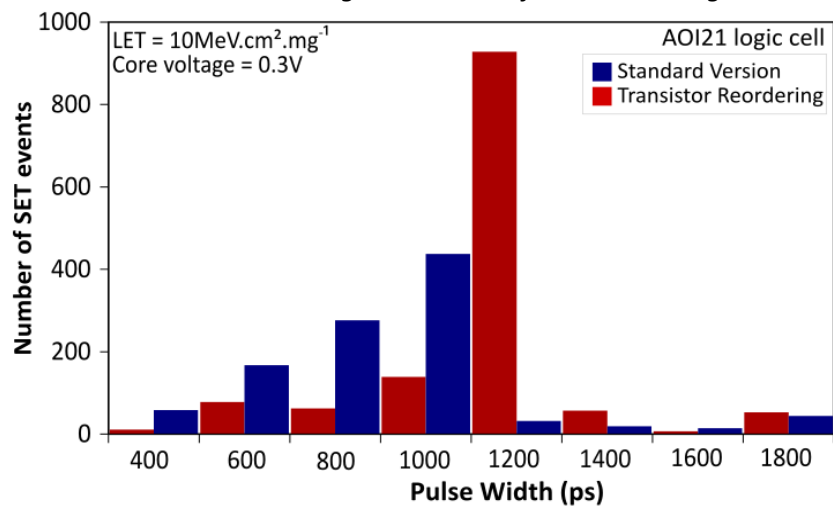


Source: Adapted from (ZIMPECK et. al, 2019b)

The histograms of SET pulse width for both topologies are shown in Figure 5.6 and Figure 5.7 for the AOI21 cell under a LET of 10  $\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$  and 58  $\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , respectively. The range of SET pulse width measured for low LET is between 267-1800ps while for high LET dose is between 120-600ns. As expected, the SET pulse widths have a wide distribution and increase significantly for higher LET levels.

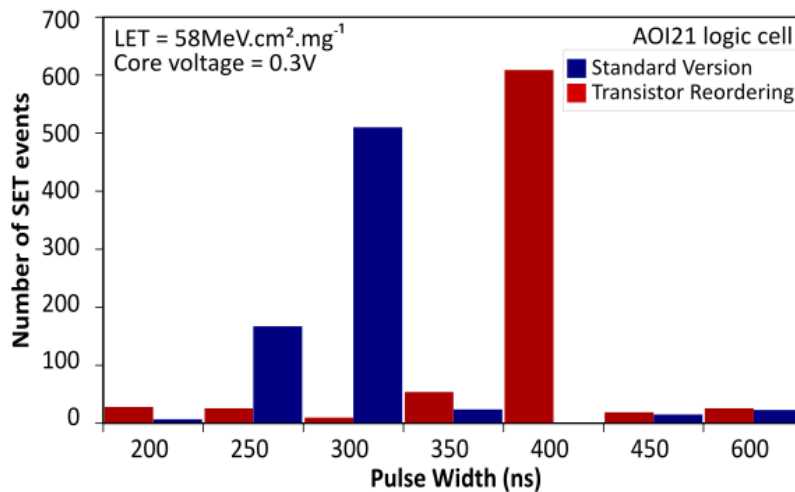
The standard version generates predominantly smaller SET pulse widths when compared with the full distribution of pulses in both LETs investigated. For a LET of  $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , most of SET pulse widths (around 90%) are smaller than 1000ps. The opposite happens with a design using the transistor reordering technique, such that 78% of the SET pulse widths are larger than 1000ps. For a LET of  $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , a similar tendency can be observed. The transistor reordering results in 92% of the SET pulse widths larger than 350ps.

Figure 5.6: SET pulse width distribution for the AOI21 gate designed in the standard version and using the transistor reordering under a LET of  $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$



Source: Adapted from (ZIMPECK et. al, 2019b)

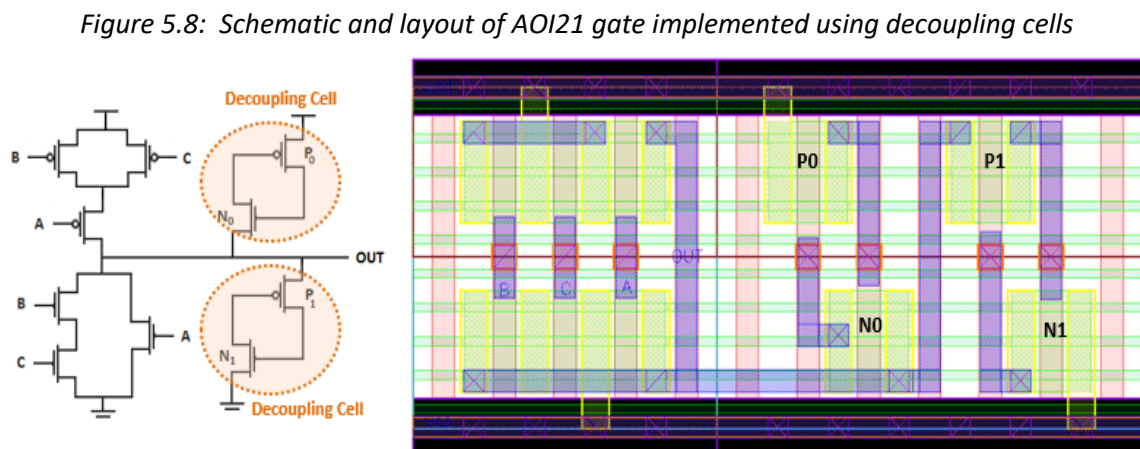
Figure 5.7: SET pulse width distribution for the AOI21 gate designed in the standard version and using the transistor reordering under a LET of  $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$



Source: Adapted from (ZIMPECK et. al, 2019b)

## 5.1.2. Decoupling Cells

The insertion of decoupling cells is a capacitive method that increases the critical charge of the node that is connected to them. Moreover, the transistors in cross-coupled mode help to ensure better signal integrity, decreasing the impact caused by process variations. Considering that, for the logic gates investigated, the output node is most vulnerable to soft errors and the sensitivity of gates to process variability is measured using the output signal, the decoupling cells were connected to the output node. Figure 5.8 shows the schematic and the layout of AOI21 logic gate using decoupling cells with sizing equal to three fins. This technique demands four extra transistors, increasing the layout width, and consequently, the area of AOI21 gate around 1.4x.



*Source: From the author*

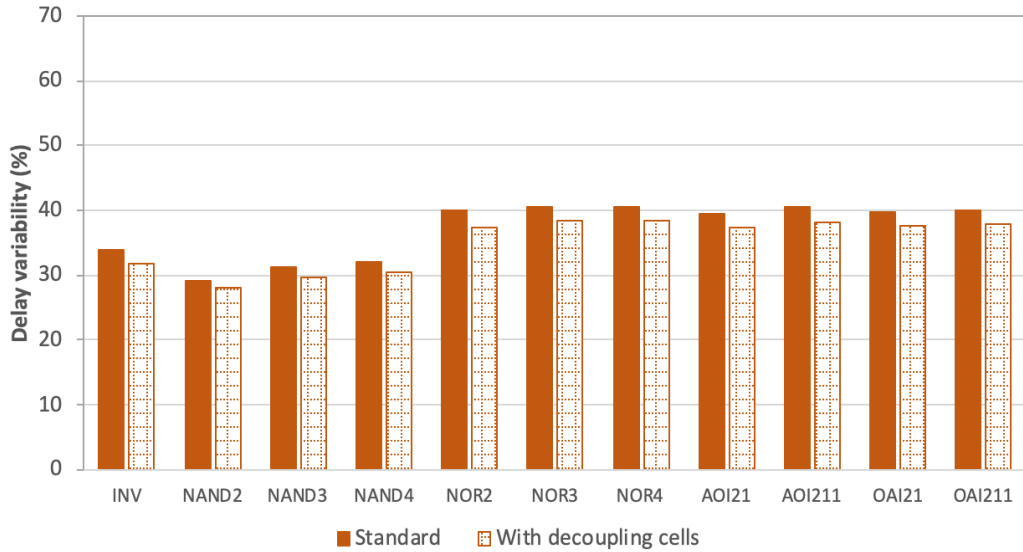
The delay and power variability of all logic gates in the standard version and using decoupling cells is shown in Figure 5.9 and Figure 5.10, respectively, considering 5% of deviation from nominal values and the  $\sigma/\mu$  relation of the worst-case delay. According to the results, the adoption of decoupling cells is an effective approach to obtain logic gates more robust to process variations, presenting more significant reductions for power variability.

On average, a design with decoupling cells decreases the delay variability of logic gates around 5.1%, if compared with the standard version. The improvements for the NAND and AOI gates increase as the number of inputs also increase, but the opposite behavior was verified for

the NOR and OAI gates, with a drop in the gains. Except for AOI21 gate, all the other presented a minimal improvement of 4% in the delay variability.

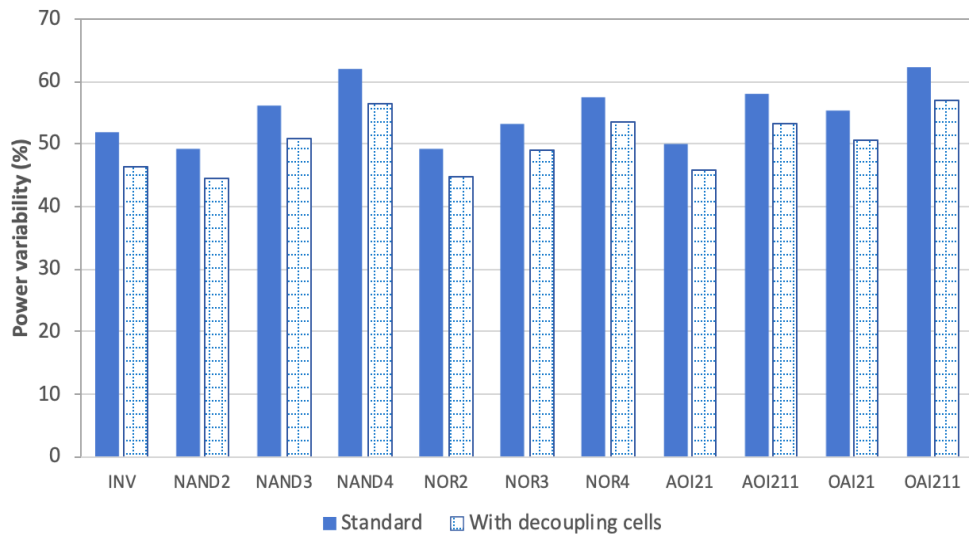
The gains on power variability using decoupling cells are 8.6%, on average. Logic gates with a smaller number of inputs presented higher power variability mitigation. Among all logic gates evaluated, the NAND2 presented the highest gain (9.4%) in the power variability while the lowest improvement is equal to 7%, obtained by the NOR4 logic gate.

Figure 5.9: Delay variability using decoupling cells



Source: From the author

Figure 5.10: Power variability using decoupling cells



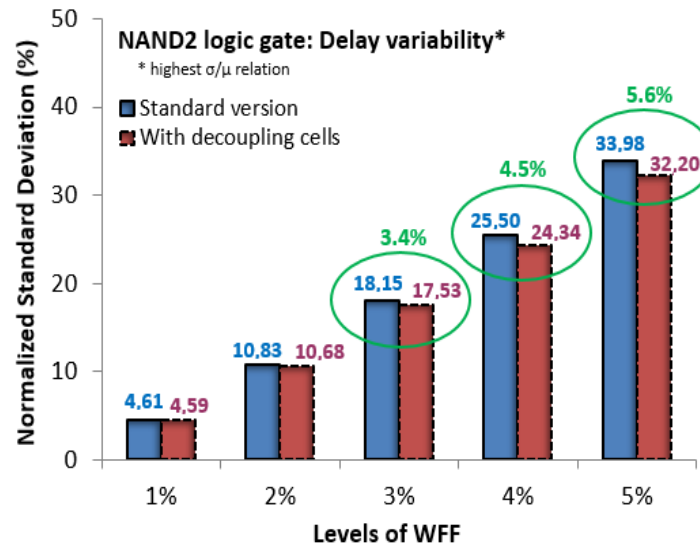
Source: From the author

### 5.1.2.1. Impact of different levels of WF fluctuations

The design of each logic gate using decoupling cells was evaluated under different levels of WF fluctuations. As an example, Figure 5.11 shows the delay variability of NAND2 gate with process variations from 1% to 5% adopting the highest  $\sigma/\mu$  relation. The insertion of decoupling cells become advantageous for fabrication processes with WF fluctuations above 2%. The same behavior was observed for all logic gates studied in this work.

The gains for the NAND2 gate increase as the percentage of variation also increases, reaching up to 5.6% with 5% of WFF, as can be seen in the values highlighted above the circles. This tendency also was verified for the INV, and NAND3 cells. However, the opposite happens for all the other gates, such that the variations of 3% instead of 5% presented the most robust results. According to Figure 5.12, it is possible to analyze the delay variability of NAND2 gate considering the  $\sigma/\mu$  relation of worst-case delay. Although the trend for all logic gates remains the same, the gains in adopting the decoupling cells technique become smaller.

Figure 5.11: Delay variability of NAND2 gate with different levels of WFF considering the highest  $\sigma/\mu$  relation



Source: Adapted from (ZIMPECK et. al, 2019a)

On the other hand, a design with decoupling cells is only advantageous for power variability if the variation from nominal conditions is above 4%, as highlighted in Figure 5.13. If

the NAND2 logic gate suffers a deviation of 5%, the use of decoupling cells brings an improvement of around 9.4%. Except for the inverter, all the other logic gates presented the same tendency to process variability mitigation. Depending on the levels of WFF, a design with decoupling cells introduced gains in the delay and power variability up to 10.3% and 10.7%, respectively.

Figure 5.12: Delay variability of NAND2 gate with different levels of WFF considering the  $\sigma/\mu$  relation of worst-case delay

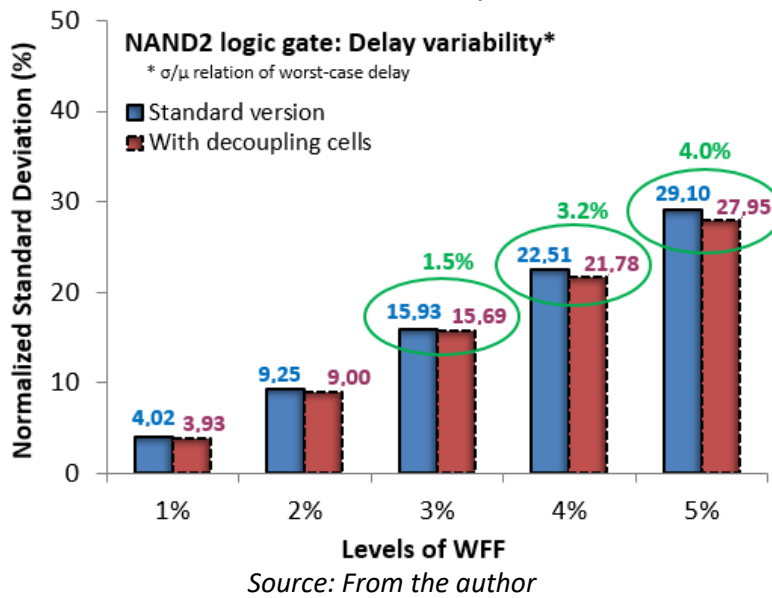
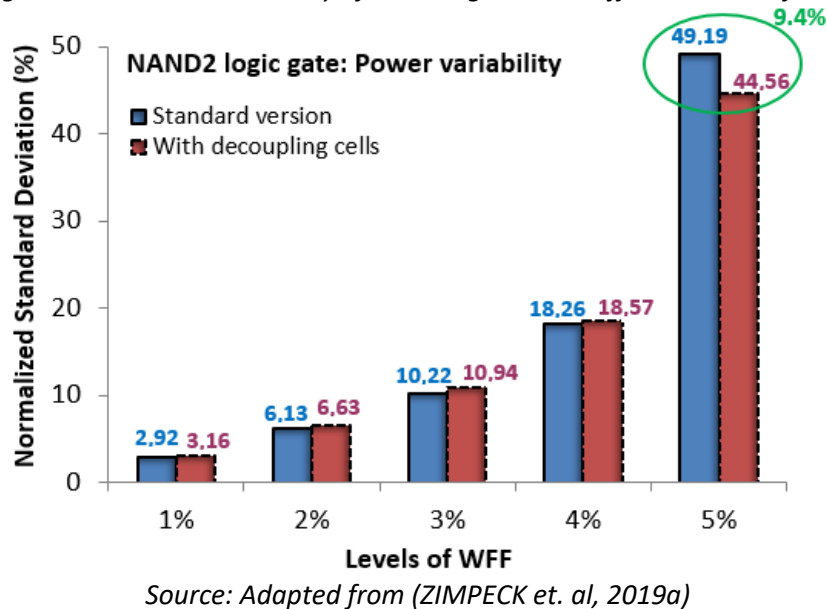


Figure 5.13: Power variability of NAND2 gate with different levels of WFF

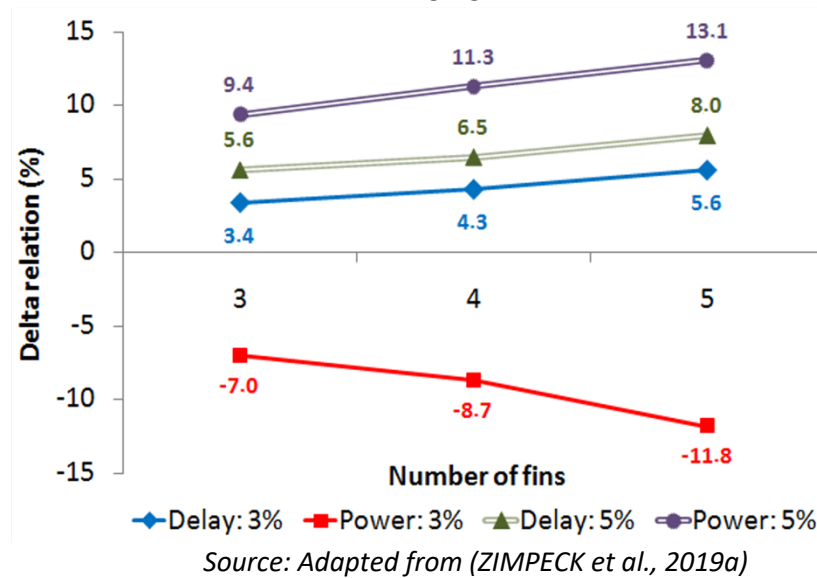




### 5.1.2.2. Sizing Influence

The total capacitance in the output of each gate depends on the transistor sizing of decoupling cells. As FinFET devices have a discrete sizing, it is possible to place multiple fins in parallel to obtain wider FinFETs. The gains of a NAND2 logic gate with decoupling cells exploring a different number of fins can be seen in Figure 5.14. Process variability robustness increases even more when larger decoupling cells are used. For example, considering the process variations of 5% WFF, the adoption of decoupling cells with five fins reduces the sensitivity of power and delay variability in 3.7% and 2.4% when compared with a layout with three fins, respectively. On the other hand, the adoption of decoupling cells with 3% of WF variations from nominal values generates a worsening in the sensitivity of power variability. This behavior intensifies when larger decoupling cells are used in the design. The behavioral trend for the other logic gates remains the same.

Figure 5.14: Improvements in connecting decoupling cells with different number of fins in the output of NAND2 logic gate

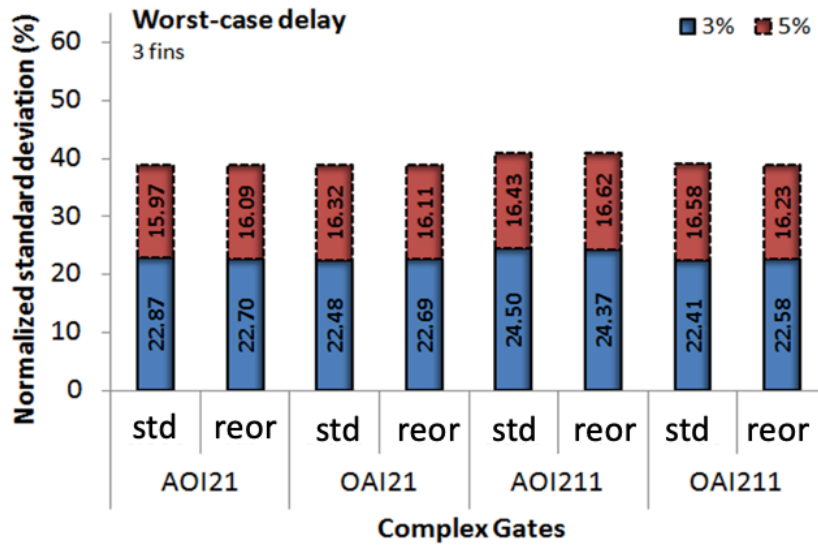


### 5.1.2.3. Exploring decoupling cells with transistor reordering

The effectiveness of applying the transistor reordering technique with the insertion of decoupling cells is presented in Figure 5.15 and Figure 5.16 for the delay and power variability, respectively. In this case, the transistor reordering (reor) presents the lowest values in most of

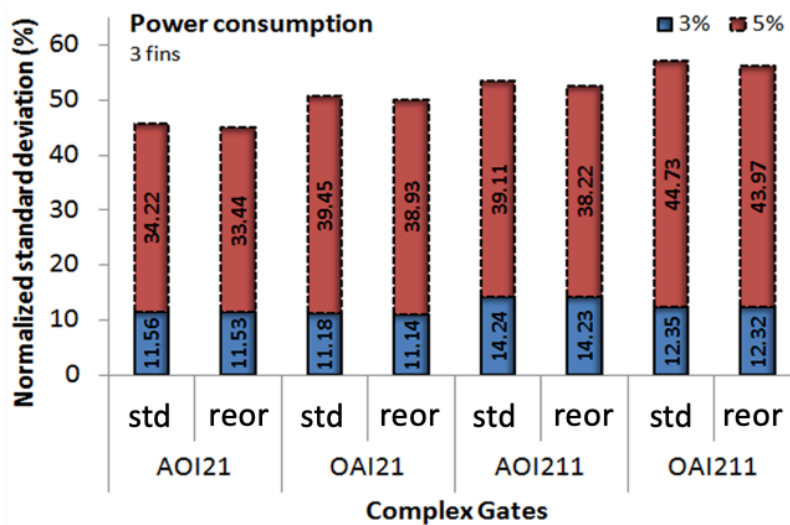
the cases observing the  $\sigma/\mu$  relation. The standard topology (std) has a little advantage for the OAI gates under 3% of WFF for delay analysis, and, also for AOI211 complex gate exposed to 5% of WFF. However, in general, the results differ less than 2%, signaling a not statistically significant difference in the deviation. Thus, the influence of the transistor arrangement does not show a direct relation to increasing the process variability robustness when the decoupling cells are used in the design.

Figure 5.15: Delay variability exploring decoupling cells with transistor reordering



Source: Adapted from (ZIMPECK et al., 2019a)

Figure 5.16: Power variability exploring decoupling cells with transistor reordering



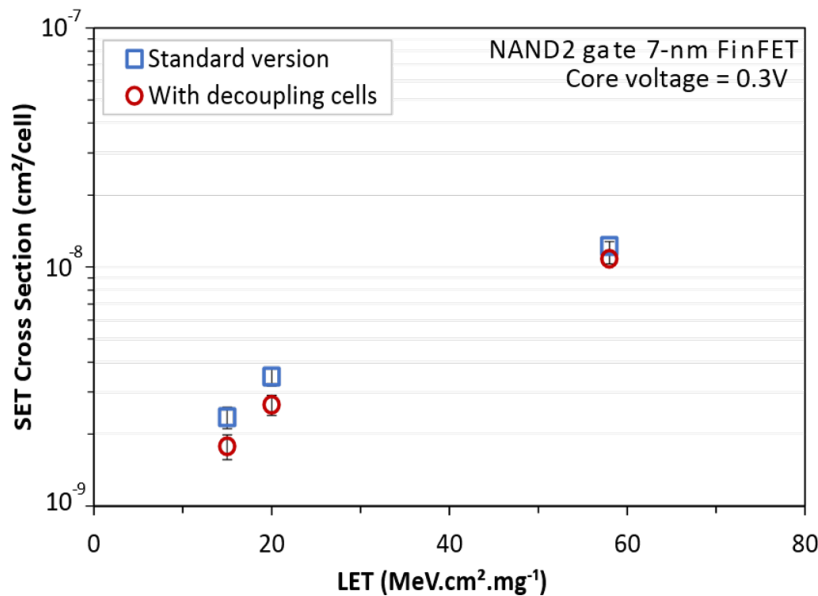
Source: (ZIMPECK et al., 2019a)

#### 5.1.2.4. Soft Error Susceptibility

The SE susceptibility of the NAND2 gate was investigated considering the standard version and connecting decoupling cells in the output with the core voltage varying from 0.7V down to 0.3V. From nominal voltage until 0.5V, the NAND2 gate is free of faults for both design possibilities. Few faults were observed in the output at 0.4V, i.e., less than 6% of current sources from the SET database considering all LETs evaluated.

Nevertheless, the design using decoupling cells presented a little improvement in the SET vulnerability. The comparison between the SET cross section of the NAND2 gate in the standard version and with the decoupling cells connected in the output at near-threshold regime (0.3V) is presented in Figure 5.17. The results showed that the SE vulnerability decreases around 24.5%, 23.7%, and 11.4% for LETs equal to 15, 20, and 58 MeV.cm<sup>2</sup>.mg<sup>-1</sup> when decoupling cells are adopted in the design. Like the previous technique, the use of decoupling cells is more advantageous for lower LETs.

Figure 5.17: SET cross section of NAND2 gate using decoupling cells

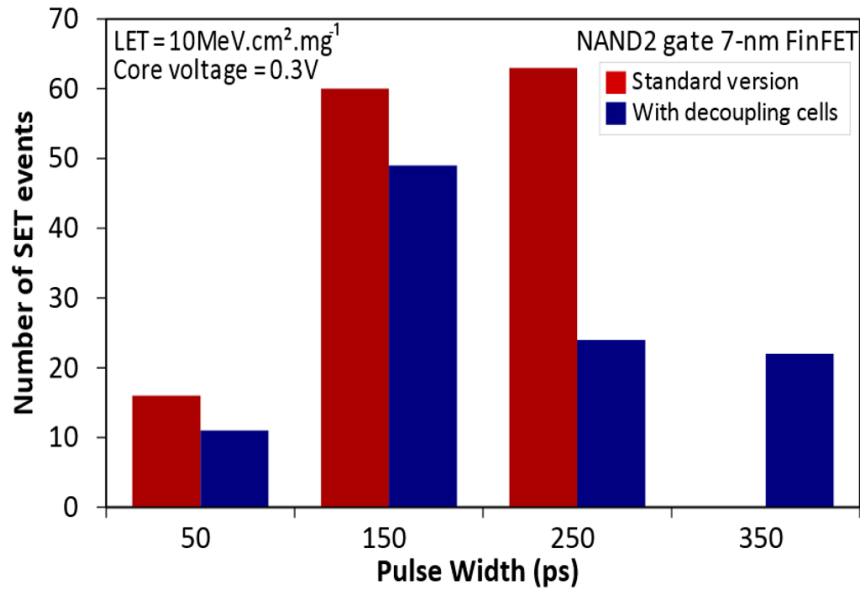


Source: (ZIMPECK et. al, 2019b)

The SET pulse width distribution to the NAND2 gate in the standard version and using decoupling cells for a LET of 15 and 58 MeV.cm<sup>2</sup>.mg<sup>-1</sup> can be shown in Figure 5.18 and Figure

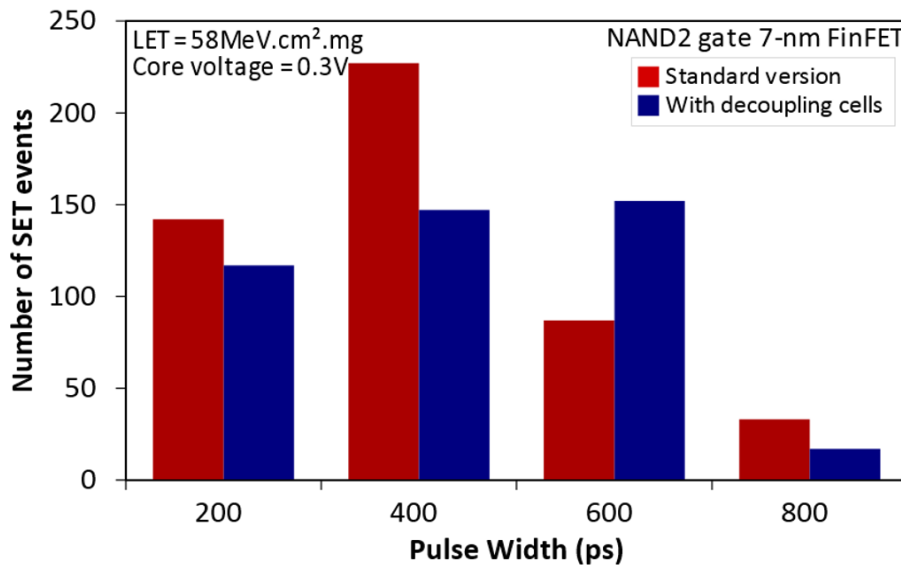
5.19, respectively. Although the design of FinFET gates connecting decoupling cells in the output is better to improve the SE susceptibility, larger SET pulses were verified mainly under higher LET levels.

Figure 5.18: SET pulse width distribution for the NAND2 gate designed with and without decoupling cells under a LET of  $20\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$



Source: (ZIMPECK et. al, 2019b)

Figure 5.19: SET pulse width distribution for the NAND2 gate designed with and without decoupling cells under a LET of  $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$

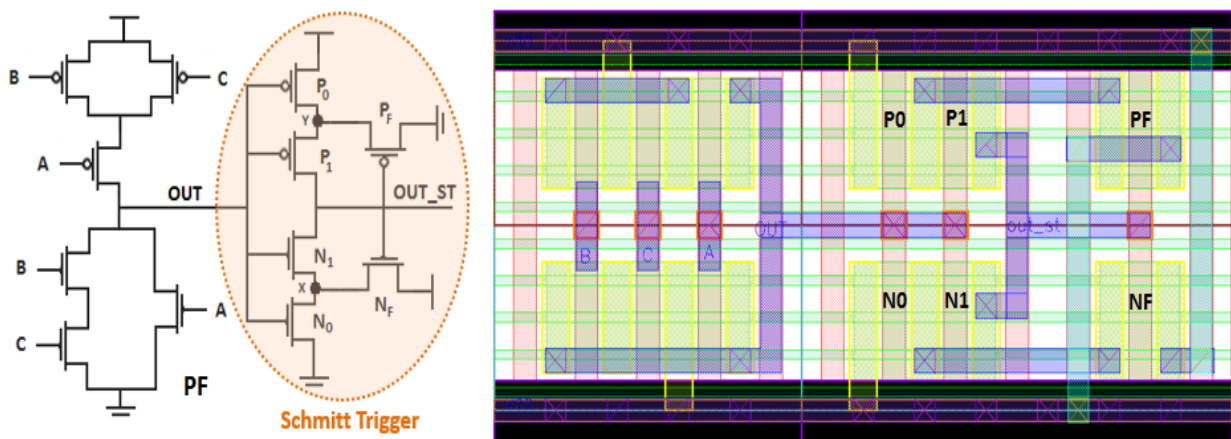


Source: (ZIMPECK et. al, 2019b)

### 5.1.3. Schmitt Trigger

The use of Schmitt Triggers is an effective method for increasing the  $I_{ON}$ -to- $I_{OFF}$  current ratio, and consequently, for minimizing the output degradation. Moreover, the design with Schmitt Trigger increases the capacitance of the output node of logic cells. These features help to mitigate the process variability effects and the soft error susceptibility. Figure 5.20 illustrates the schematic and layout of the AOI21 cell with a Schmitt Trigger of three fins connected in the output. The six extra transistors imposed by this technique alter the layout width, increasing the area of AOI21 cell around 1.4x. Among all methods evaluated, the layout of the Schmitt Trigger is unique to use M2 rails for connecting the source terminals of  $P_F$  and  $N_F$  transistors.

Figure 5.20: Schematic and layout of AOI21 logic cell implemented using Schmitt Trigger

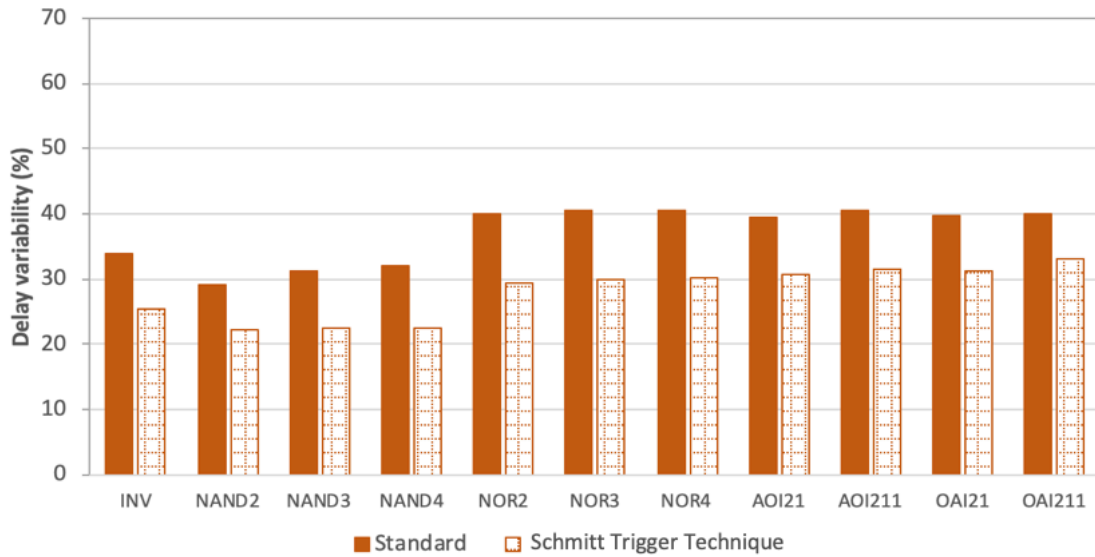


Source: From the author

The sensitivity of logic cells to process variations decreases considerably connecting Schmitt Trigger in the output node. The attenuation in the delay and power variability using this approach can be seen in Figure 5.21 and Figure 5.22, respectively, with fabrication process deviation of 5%. On average, the delay variability of logic cells has an improvement of around 26.6%. The NAND4 is the most benefited cell with the Schmitt Trigger technique, reaching 29.6% of delay variability mitigation.

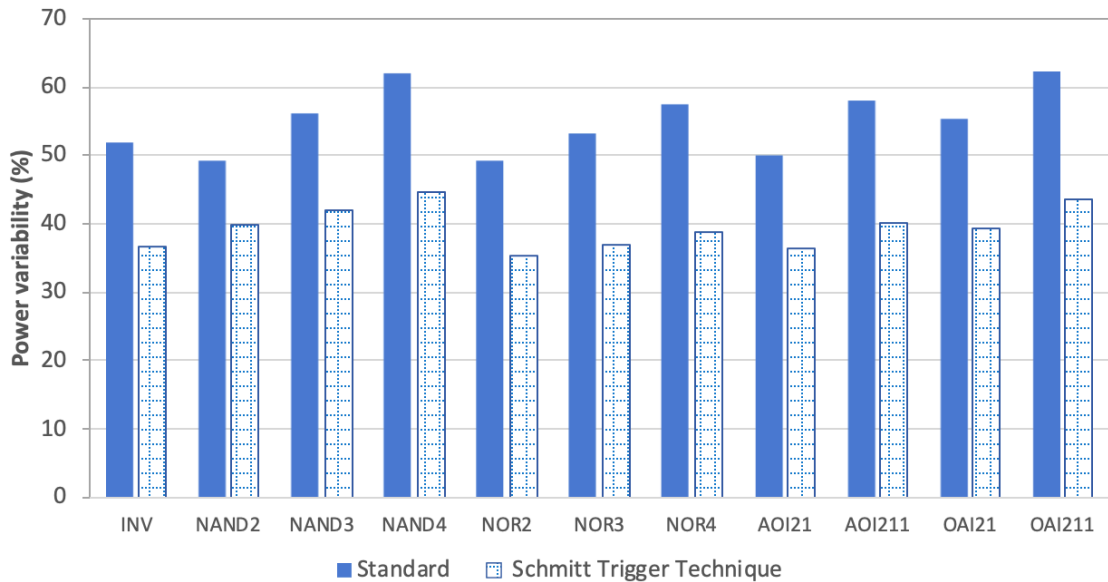
The design with a Schmitt Trigger provides the power variability mitigation of 28.3%, on average. More improvements can be found for logic cells with a larger number of inputs. However, the minimum gain (19.3%) in power variability adopting this approach is already considerable value.

Figure 5.21: Delay variability mitigation using Schmitt Trigger



Source: From the author

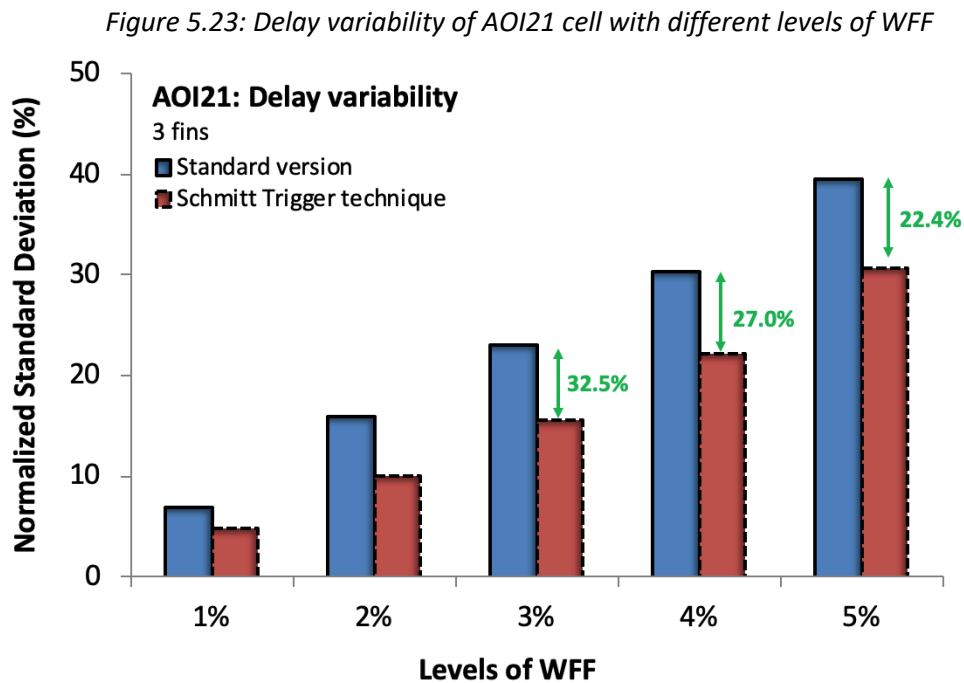
Figure 5.22: Power variability mitigation using Schmitt Trigger



Source: From the author

### 5.1.3.1. Impact of different levels of WF fluctuations

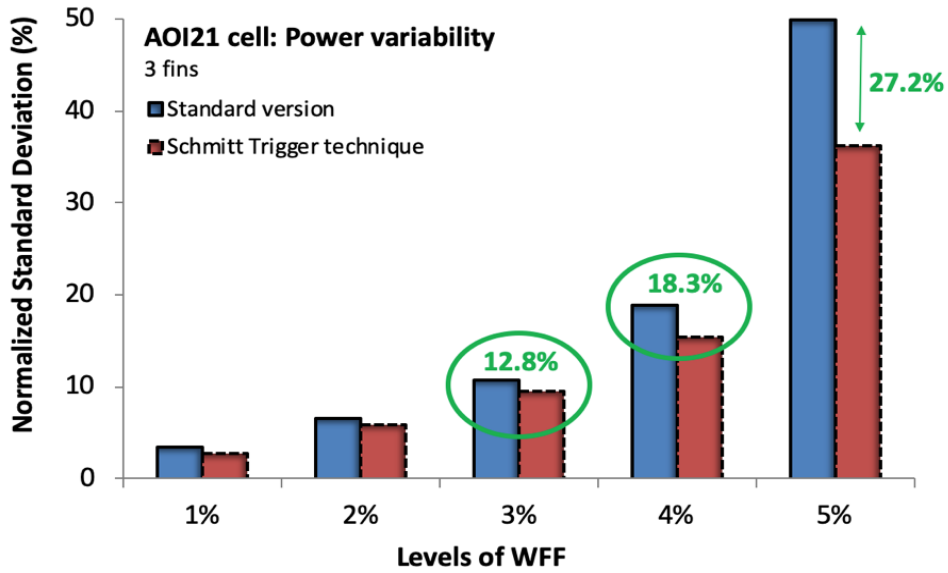
The advantages in adopting the Schmitt Trigger change according to the level of WF fluctuation that a logic cell is exposed. For exemplify this statement, Figure 5.23 shows the impact of the process variations on the delay variability of AOI21 cell. Lower levels of WF fluctuations improve even more the delay variability. However, logic cells under 1% and 2% of deviation do not follow this trend. This behavior is verified for all logic cells investigated in this work.



Source: From the author

Figure 5.24 illustrates the tendency of power variability mitigation when the AOI21 cell connected to a Schmitt Trigger was analyzed under different levels of WF fluctuation. It is possible to verify an opposite behavior of delay variability, such that more improvements in the power variability are achieved with higher levels of deviation. This conclusion for the AOI21 cell also can be applied to all logic cells. On average, the Schmitt Trigger technique provides power variability mitigation of 18% and 22.3% for 3% and 4% of deviation from nominal conditions.

Figure 5.24: Power variability of AOI21 cell with different levels of WFF



Source: From the author

### 5.1.3.2. Sizing Influence

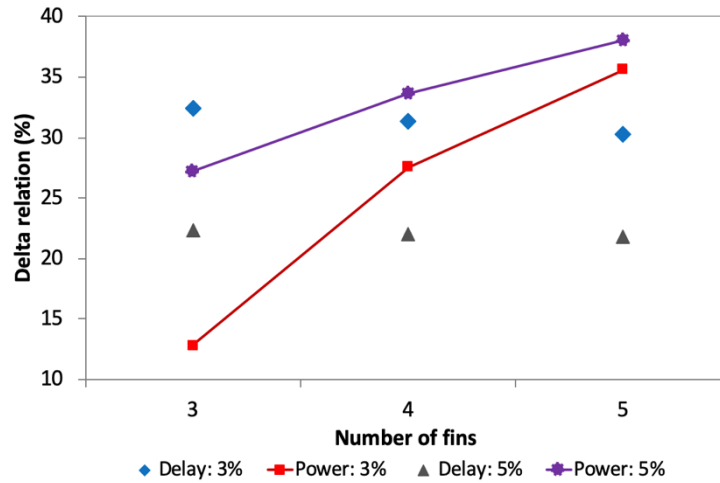
The influence in connecting a Schmitt Trigger with a different number of fins in the output of AOI21 cell was verified in Figure 5.25. Larger Schmitt Triggers decrease the impact on power variability considerably. For example, considering the process variations of 3% and 5%, the use of Schmitt Trigger with five fins improves the sensitivity of power variability in 22.8% and 10.8% if compared with a layout with three fins, respectively. On the other hand, the increase in the number of fins contributes less than 2% for delay variability mitigation, independently of the levels of WF fluctuation. In this way, investing in larger Schmitt Triggers is only advantageous to attenuate power variability.

### 5.1.3.3. Soft Error Susceptibility

The soft error susceptibility of NAND2, NOR2, and AOI21 logic cells was analyzed under low and higher LETs, varying from 5 to 58MeV.cm<sup>2</sup>.mg<sup>-1</sup>. Moreover, all input vectors were tested as well as the core voltage was modified until the near-threshold regime (0.3V). The results show that a design using a Schmitt Trigger is very promising for soft error mitigation. The three logic cells become free of faults (no events seen at gate output) using this technique, independently of the LET, input vector or core voltage employed in the design.



Figure 5.25: Improvements in connecting a Schmitt Trigger with different number of fins in the output of AOI21 logic cell

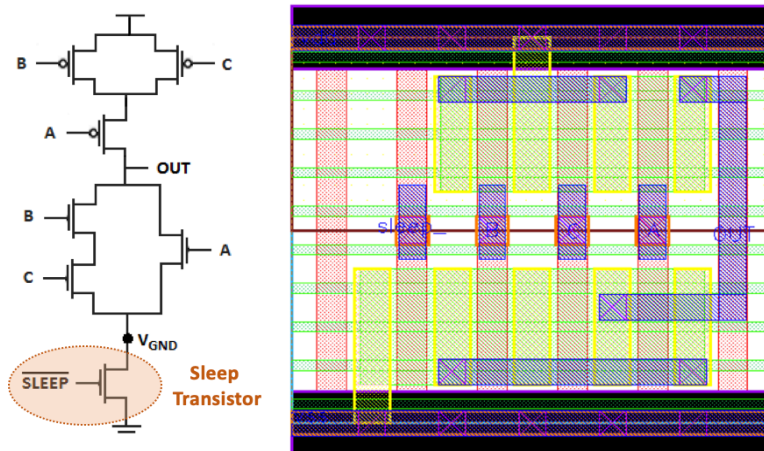


Source: From the author

### 5.1.4. Sleep Transistor

A design with sleep transistor helps to reduce the leakage currents, transient faults, process variations, and NBTI effects. For all logic gates investigated, a sleep transistor was inserted between the pull-down network, and the ground rail. As an example, Figure 5.26 shows the schematic and layout of AOI21 cell using a sleep transistor with transistor sizing equal to three fins. The extra transistor modifies the layout width, increasing the area of AOI21 cell around 0.3x.

Figure 5.26: Schematic and layout of AOI21 cell implemented using sleep transistor

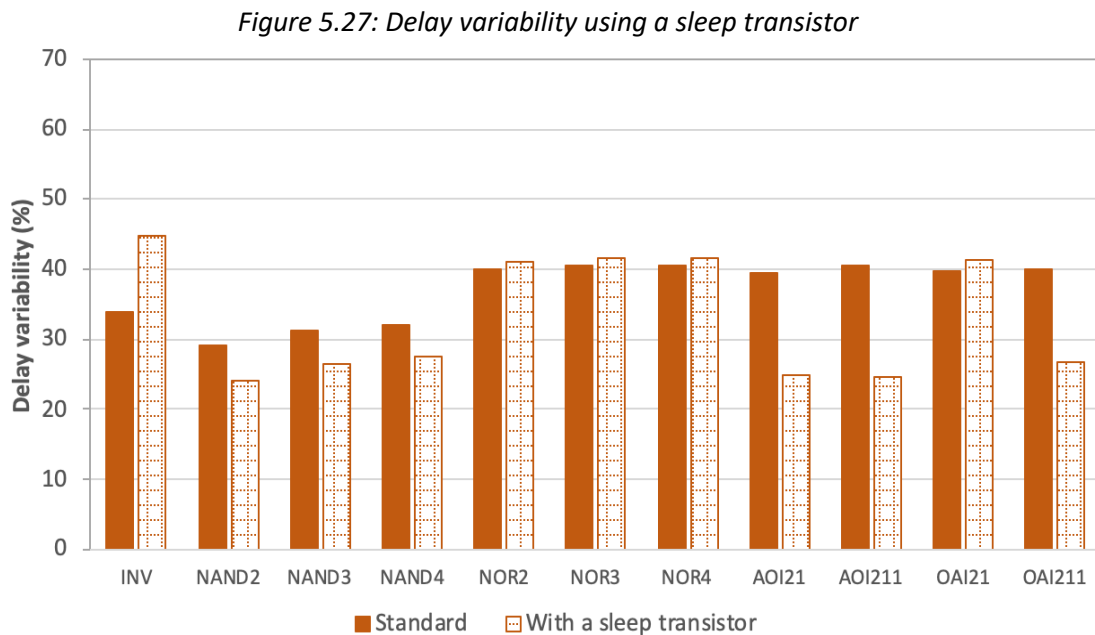


Source: From the author

Figure 5.27 and Figure 5.28 show the sensibility of logic gates to the delay and power variability, respectively, when a sleep transistor with three fins is added in the design with 5% of WF fluctuation. The results confirm the efficiency of this technique to mitigate the effects of process variation because the  $\sigma/\mu$  relation of logic cells is reduced in most of the cases.

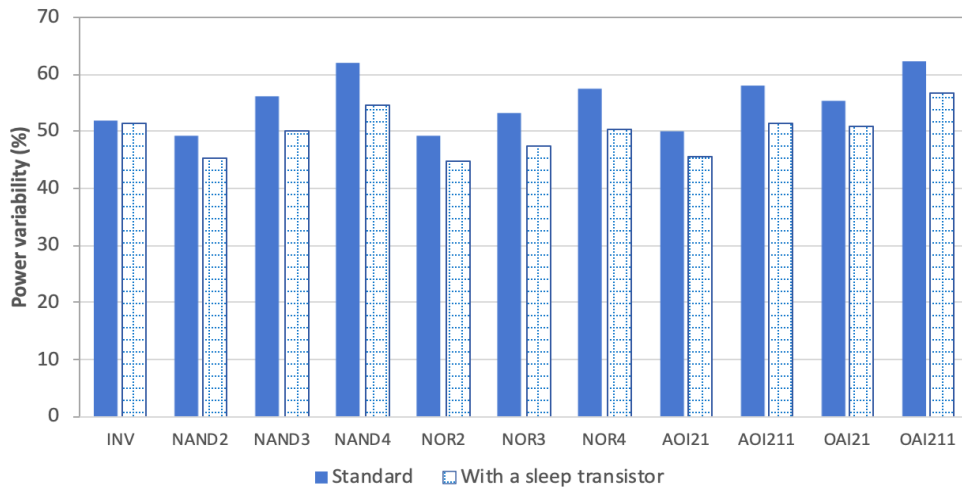
The NAND2 cell obtained 17.1% of attenuation in the delay variability. Fewer gains were observed for the NAND cell with three (15.8%) and four (13.7%) inputs. The most significant improvement in the delay variability can be observed in the AOI21 and OAI cells, where the mitigation is 36.4%, on average, for 5% of WF deviation. Nevertheless, the sleep transistor is not advantageous to control the delay variability for the inverter, AOI211, and NOR cells. This worsening is related to how the transistors in the pull-down network are arranged along with the sleep transistor.

On the other hand, a design with a sleep transistor is favorable to mitigate the power variability of all logic gates. Except for the inverter, the gains adopting this technique vary from 7.9% to 12.4%, considering 5% of deviation. Moreover, the basic (NAND/NOR) and complex (AOI/OAI) cells with a larger number of inputs present more benefits regarding power variability reduction.



*Source: From the author*

Figure 5.28: Power variability using a sleep transistor

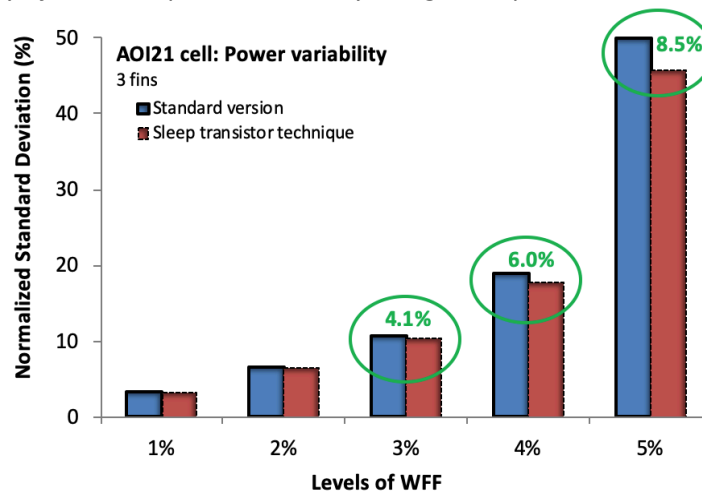


Source: From the author

### 5.1.4.1. Impact of different levels of WF fluctuations

The design of each logic cell using a sleep transistor was evaluated under different levels of WF fluctuations (1-5%). Higher levels of WF variations intensify the power variability mitigation, as shown in Figure 5.29, for the AOI21 logic cell. According to the values in green, the gains of AOI21 cell with the sleep transistor technique reach up to 8.5% with 5% of WFF. The same behavior was verified for most of the logic gates, except for INV, NOR2, and OAI211 cells. On average, the power variability is improved around 6.5%, and 9.2% for 3%, and 5% of deviation from nominal conditions.

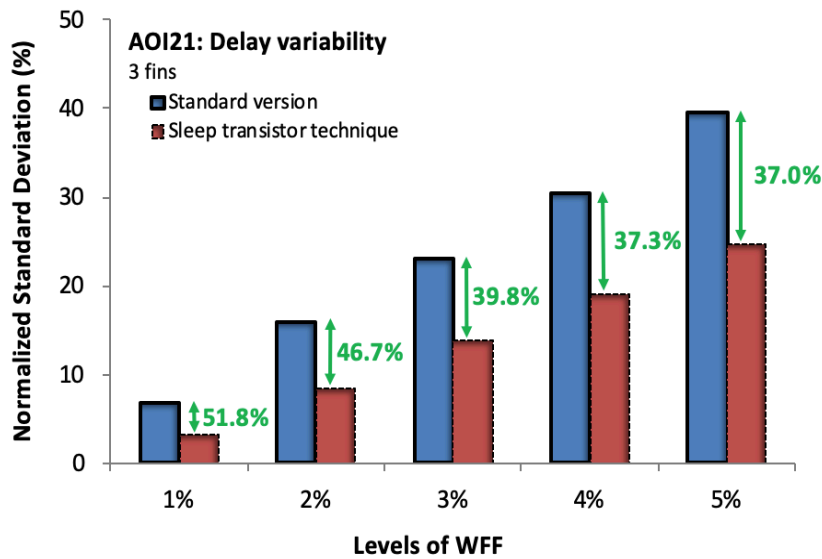
Figure 5.29: Sensitivity of AOI21 to power variability using a sleep transistor with different levels of WFF



Source: From the author

The opposite behavior was verified for the delay variability, such that low levels of WF fluctuations provide better mitigation results for the AOI21 cell, as shown the green values in Figure 5.30. The sleep transistor technique improves the delay variability around 51.8% for process variation with 1% of deviation from nominal values. This trend is in agreement with those observed for the Schmitt Trigger technique. However, it is important to highlight that for the sleep transistor technique, this tendency behavior is not valid for all the logic cells studied in this work. Moreover, the addition of a sleep transistor in the design is disadvantageous to mitigate the delay variability of NOR cells and AOI211 cell.

Figure 5.30: Sensitivity of AOI21 to delay variability using a sleep transistor with different levels of WFF

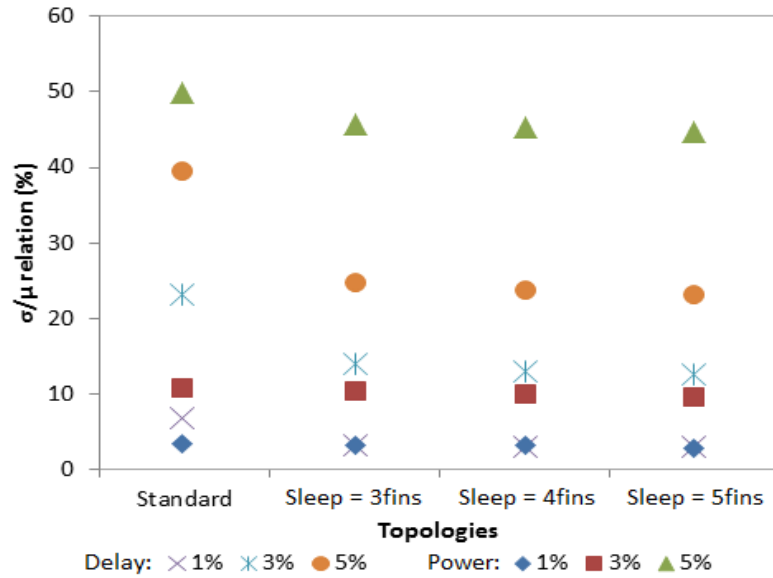


Source: From the author

### 5.1.4.2. Sizing Influence

The influence of different sleep transistor sizes to the process variability mitigation is shown in Figure 5.31, using the AOI21 cell as an example. Independently of the levels of variation, larger sleep transistors contribute less than 2% both for power and delay mitigation, if compared with the smaller version (3 fins). This behavior is similar to all the other logic cells adopting different transistor sizing. In this way, the best alternative is to use a smaller sleep transistor, ensuring favorable process variability mitigation, avoiding even more penalties in performance, power consumption, and area.

Figure 5.31: Impact of sleep transistor sizing in the process variability mitigation of AOI21 gate



Source: (ZIMPECK et. al, 2019c)

### 5.1.4.3. Soft Error Susceptibility

The soft error susceptibility of NAND2, NOR2, and AOI21 logic cells was analyzed under low and higher LETs, varying from 5 to 58MeV.cm<sup>2</sup>.mg<sup>-1</sup>. Moreover, all input vectors were tested as well as the core voltage was modified until the near-threshold regime (0.3V). The results show that a design using a sleep transistor is also very promising for soft error mitigation. The three logic cells become free of faults (no events seen at gate output) using this technique, independently of the LET, input vector or core voltage employed in the design.

## 5.2. Technique Drawbacks

The use of circuit-level techniques brought several benefits regarding the mitigation of process variability and soft errors. However, some approaches add extra transistors in the design that, consequently, increases the area, power consumption, and performance of logic cells when compared with the standard version. Moreover, even that the transistor reordering keeps the same number of transistors in the design, this approach modifies the electrical behavior, introducing some penalties in the metrics. This section is dedicated to discussing the penalties involved in the adoption of each proposed mitigation technique.

## 5.2.1. Area

All transistors of the logic cells were designed using the same sizing, but the extra transistors imposed by some approaches were evaluated using different sizing to verify the mitigation capability. The number of extra transistors, as well as the area of the logic cells using each technique, are shown in Table 5.1.

In terms of area occupied, the transistor reordering is the best technique, because it has no area penalties. The addition of decoupling cells or Schmitt Triggers in the cell output introduces a different number of extra transistors, but the area penalty for both is the same. This happens because the signal in the gate terminal is different for the pair of transistors in the cross-coupled mode. Since the ASAP7 PDK does not allow the gate layer break, more area is demanded in the layout of decoupling cells to adjust each input (see Figure 5.8). The increase of area can vary between 2.2x and 4.5x, depending on the number of inputs and the sizing of extra transistors.

*Table 5.1: Area penalties in adopting each circuit-level mitigation techniques*

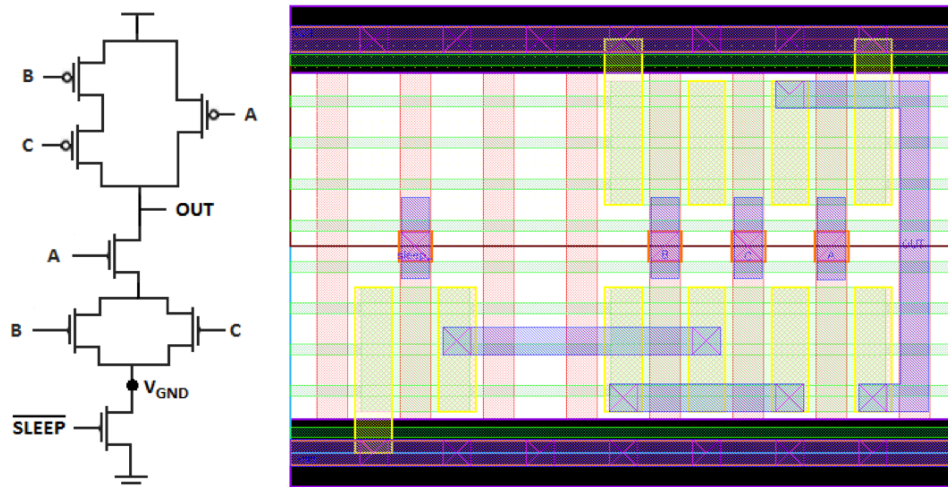
Techniques	Extra transistors	Sizing	Area of logic cells (nm <sup>2</sup> )			
			1 input	2 inputs	3 inputs	4 inputs
Standard version	-	3 fins	50.9	67.8	84.8	101.7
Transistor reordering	0	3 fins	-	-	84.8	101.7
Decoupling cells	4	3 fins	169.6	186.5	203.5	220.4
		4 fins	198.7	218.6	238.5	258.3
		5 fins	227.9	250.7	273.5	296.2
Schmitt Trigger	6	3 fins	169.6	186.5	203.5	220.4
		4 fins	198.7	218.6	238.5	258.3
		5 fins	227.9	250.7	273.5	296.2
Sleep transistor	1	3 fins	67.8	84.8	*101.7	*118.7
		4 fins	79.5	99.4	*119.2	*139.1
		5 fins	91.2	113.9	*136.7	*159.5

*\* These values change for the OAI logic cells.*

*Source: From the author*

The insertion of a sleep transistor generates a small increase in the area of logic cells that vary from 1.2x to 1.8x in most of the cases. However, there is an exception to the OAI21 and OAI211 logic cells. As shown in Figure 5.32 for the OAI21 cell, a diffusion break was required to make the connections between the standard design and the sleep transistor correctly. For each diffusion break, the ASAP7 PDK demands two dummy gates at each end. This constraint increases the estimated area in Table 5.1 around 33% and 28% for OAI21 and OAI211 cells designed with sleep transistors, respectively.

Figure 5.32: Diffusion break to connect the sleep transistor to the standard design of OAI21 cell



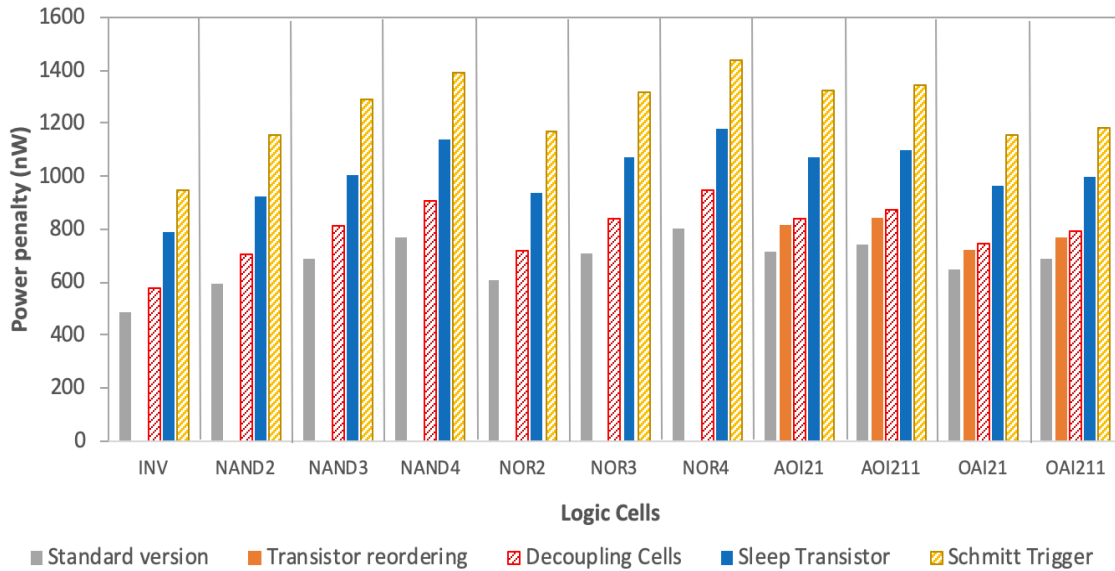
Source: From the author

## 5.2.2. Power Consumption

The four circuit-level mitigation techniques explored in this work also introduced penalties in the power consumption of the logic cells. As expected, approaches that add extra transistors bring a higher impact over the power consumption, as shown in Figure 5.33, considering 5% of deviation and the extra transistor sizing equal to three fins. In this way, a design with Schmitt Trigger connected to the cell output suffers the higher average impact on power (84.6%). The insertion of decoupling cells has four additional transistors. The advantage is that transistors in the cross-coupled mode consume less power. For this reason, the average impact on power due to the addition of decoupling cells is around 17.6%. Although the sleep transistor presented the fewer area penalty, this device connected to the pull-down network introduces a considerable

power overhead of 50.4%, on average. Finally, the impact of the transistor reordering approach on power consumption is around 11.1%.

Figure 5.33: Power penalty of using circuit-level mitigation approaches



Source: From the author

The power penalties increase even more for low levels of WF fluctuations, as shown in Table 5.2. This behavior can be seen for all mitigation techniques, but the growth is not so significant for the designs using a sleep transistor. On average, a design with decoupling cells under 1% of deviation from nominal conditions suffer 12.3% more penalties in the power consumption if compared with 5% of deviation. The use of Schmitt Trigger remains the approach that most impacts the power of logic cells, independently of the level of WF fluctuations.

The extra devices imposed by decoupling cells, sleep transistor, and Schmitt Trigger techniques were evaluated under different number of fins. As expected, larger devices increase the power penalties, as demonstrates Table 5.3 considering 5% of deviation. Decoupling cells with four and five fins generate an increase in the power consumption around 5% and 11%, respectively, when compared with the three fins version. This percentage of penalty does not rise to lower levels of variation (1-4%).



Table 5.2: Power penalty of using circuit-level mitigation approaches with different levels of WF fluctuations

Gates	Power penalties (%) – 3 fins								
	Decoupling cells			Sleep transistor			Schmitt Trigger		
	1%	3%	5%	1%	3%	5%	1%	3%	5%
INV	31.6	19.7	18.6	60.8	61.3	62.1	99.1	94.1	95.3
NAND2	19.7	19.4	18.8	55.8	54.7	54.7	99.1	94.3	94.0
NAND3	43.7	18.9	18.1	53.2	52.9	45.7	95.1	92.1	87.2
NAND4	29.8	18.4	17.8	50.6	50.2	48.4	90.6	87.2	81.1
NOR2	31.3	19.6	19.0	55.8	55.6	54.5	98.9	96.8	92.7
NOR3	30.1	18.9	18.3	51.9	52.1	50.4	93.8	91.0	85.4
NOR4	29.7	18.4	18.1	49.6	48.9	47.1	89.4	85.5	79.0
AOI21	29.3	17.6	16.9	51.4	50.9	49.7	89.6	88.6	84.8
AOI211	29.2	17.9	17.2	50.7	50.7	48.3	88.0	86.6	80.9
OAI21	27.8	16.3	15.6	50.3	49.9	48.9	83.5	82.7	78.6
OAI211	26.6	15.3	14.8	46.9	46.5	45.1	78.2	77.1	72.1
<b>Average</b>	<b>29.9</b>	<b>18.2</b>	<b>17.6</b>	<b>52.5</b>	<b>52.2</b>	<b>50.4</b>	<b>91.4</b>	<b>88.7</b>	<b>84.6</b>

Source: From the author

Table 5.3: Power penalty of using circuit-level mitigation approaches with different number of fins and 5% of deviation

Techniques	Power penalties (%) – 4 and 5 fins					
	Decoupling cells		Sleep Transistor		Schmitt Trigger	
Sizing	4 fins	5 fins	4 fins	5 fins	4 fins	5fins
INV	24.1	30.5	62.3	63.7	114.6	136.7
NAND2	24.2	30.5	54.7	54.7	114.1	136.6
NAND3	23.7	30.0	51.8	52.5	106.5	127.9
NAND4	23.0	29.3	48.4	48.8	99.7	120.4
NOR2	24.4	31.0	54.6	55.9	113.5	136.3
NOR3	23.8	30.1	50.4	51.6	105.8	127.7
NOR4	23.4	29.6	47.1	48.2	98.8	120.3
AOI21	21.9	27.9	49.7	51.0	103.8	124.4
AOI211	20.3	25.7	48.7	49.1	100.0	120.9
OAI21	22.3	28.4	48.8	50.0	96.0	114.9
OAI211	19.2	24.4	45.6	46.2	88.4	106.1
<b>Average</b>	<b>22.7</b>	<b>28.9</b>	<b>51.1</b>	<b>52.0</b>	<b>103.7</b>	<b>124.7</b>

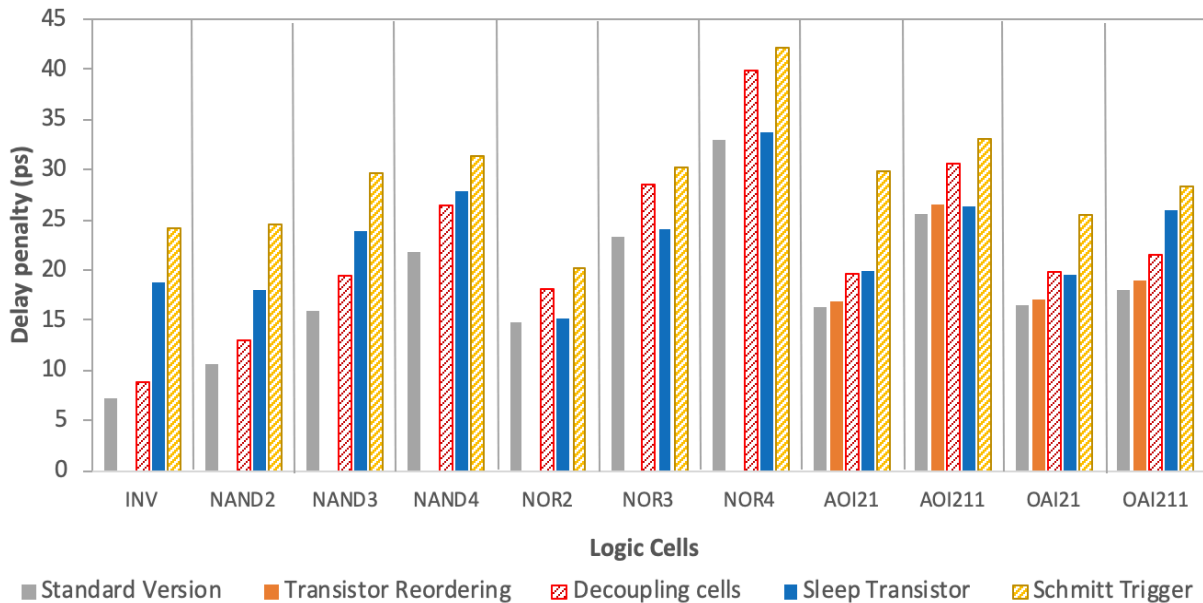
Source: From the author

For the sleep transistor technique, independently of the transistor sizing and the levels of WF fluctuations, the impact on power consumption is almost the same, around 50-53%. The critical case is related to the addition of larger Schmitt Trigger. Each fin adds in the design generates a worsening of 20% in the power consumption of logic cells, on average. More disadvantages can be seen when lower levels of deviation (1-4%) were investigated.

### 5.2.3. Performance

The extra transistors of the circuit-level mitigation approach also introduced a performance drop in the logic cells. Figure 5.34 illustrates the delay penalty of all logic cells under 5% of deviation using each technique. The connection of Schmitt Triggers with three fins in the cell output generates an increase of 74.6% in the delay metric, on average. Also observing the average, the impact on the delay halved (36.3%) when sleep transistors were adopted instead of the Schmitt Trigger technique. The delay overhead introduced by using decoupling cells is around 21.2%, such that the delay is much less impacted than the power metric. Finally, the transistor reordering technique modifies the performance of complex cells around 3.5%.

Figure 5.34: Delay penalty of using circuit-level mitigation approaches



Source: From the author

With the exception of decoupling cells technique, the penalties on delay decrease for low levels of WF fluctuation, on average, as shown in Table 5.4. For the AOI211 and NOR cells, the adoption of a sleep transistor introduced a little impact on delay. On the other hand, the insertion of decoupling cells can be more interesting for INV, AOI21, OAI21, and NAND cells to reduce the impact on delay. Independently of the levels of WF fluctuations, the Schmitt Trigger remains the approach that most impact the performance. Larger sleep transistors decrease the impact on delay, as shown in Table 5.5, considering 5% of deviation. However, if decoupling cells or Schmitt Triggers are connected to the output, the influence on the delay grows as the sizing increases.

*Table 5.4: Delay penalty of using circuit-level mitigation approaches with different levels of WF fluctuations*

Gates	Delay penalties (%) – 3 fins								
	Decoupling cells			Sleep transistor			Schmitt Trigger		
	1%	3%	5%	1%	3%	5%	1%	3%	5%
INV	24.6	24.2	22.2	125.4	142.4	159.7	212.7	233.3	234.7
NAND2	21.6	23.0	22.4	66.0	69.0	68.2	107.2	124.0	129.0
NAND3	37.3	22.8	21.3	48.6	49.7	49.4	78.2	85.2	85.6
NAND4	21.8	22.1	21.6	32.1	32.8	28.0	39.9	43.6	44.0
NOR2	24.2	24.1	23.0	1.6	2.2	2.7	23.4	32.1	36.5
NOR3	23.6	22.9	22.2	2.0	2.3	2.6	27.1	28.9	29.1
NOR4	20.4	21.8	21.3	1.7	1.9	2.4	30.4	29.9	28.0
AOI21	22.5	21.7	20.1	26.8	23.7	22.0	78.9	82.2	81.7
AOI211	25.4	20.9	19.9	1.8	2.5	2.7	28.1	29.7	29.3
OAI21	22.4	21.6	20.0	23.1	20.3	18.8	47.6	52.9	54.5
OAI211	20.3	19.5	18.8	45.6	43.8	43.1	51.9	55.6	56.9
<b>Average</b>	<b>24.0</b>	<b>22.2</b>	<b>21.2</b>	<b>34.0</b>	<b>35.5</b>	<b>36.3</b>	<b>65.9</b>	<b>72.5</b>	<b>73.6</b>

*Source: From the author*

Table 5.5: Delay penalty of using circuit-level mitigation approaches with different number of fins and 5% of deviation

Techniques	Power penalties (%) – 4 and 5 fins					
	Decoupling cells		Sleep Transistor		Schmitt Trigger	
Sizing	4 fins	5 fins	4 fins	5 fins	4 fins	5fins
INV	29.2	37.5	138.9	140.3	243.9	252.9
NAND2	29.0	36.4	58.9	53.3	137.9	146.9
NAND3	28.1	35.6	41.9	37.5	94.4	103.8
NAND4	27.5	35.3	32.6	29.4	54.1	61.9
NOR2	29.1	37.8	2.0	2.0	45.7	55.1
NOR3	28.2	36.3	2.1	2.1	38.0	47.4
NOR4	27.1	35.0	2.1	1.8	36.5	45.6
AOI21	26.2	34.1	15.2	11.0	86.9	93.9
AOI211	25.8	33.2	2.3	2.0	37.5	49.8
OAI21	26.1	33.9	12.1	7.9	70.9	83.0
OAI211	24.3	31.5	35.9	32.0	68.0	72.4
<b>Average</b>	<b>27.3</b>	<b>35.2</b>	<b>31.3</b>	<b>29.0</b>	<b>83.1</b>	<b>92.1</b>

Source: From the author

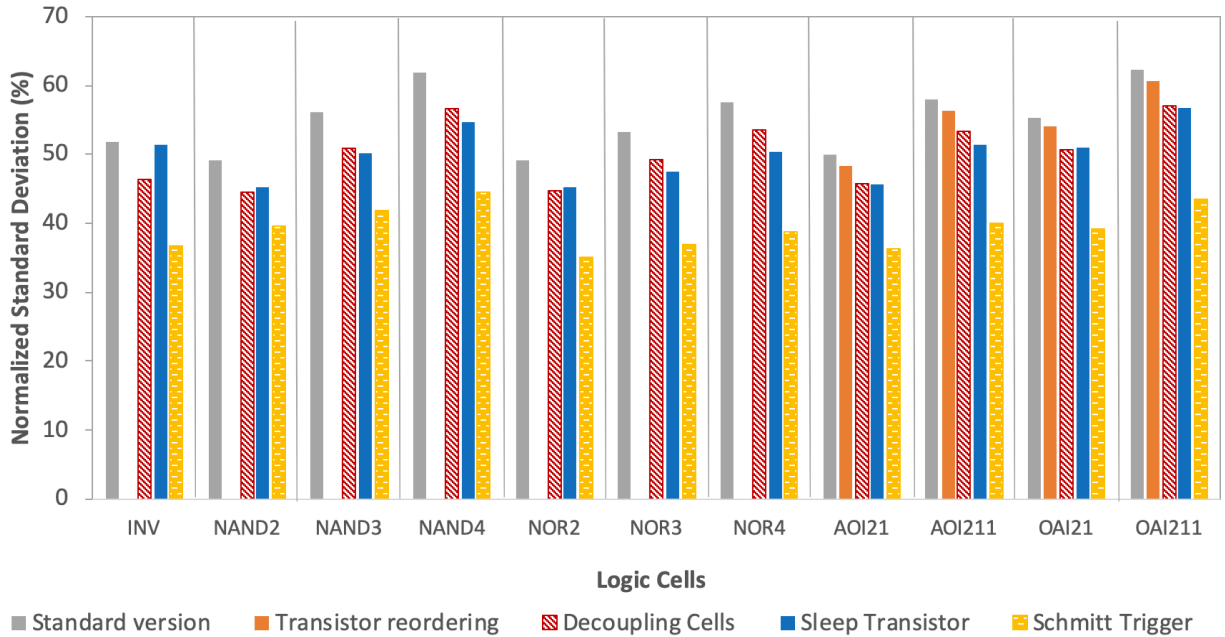
### 5.3. Overall Comparison

This subsection summarizes all conclusions obtained in this thesis and point out the best circuit-level mitigation technique depending on the target application. Logic cells can be submitted to high (5%), medium (3%), or low (1%) levels of WF fluctuations, such that these variations can impact the power, propagation delays or both. The sensitivity of logic cells to the process variations is measured through the normalized standard deviation ( $\sigma/\mu$  relation). As previously presented, the deviation on power and propagation delays due to the process variations are denominated in this work as power and delay variability.

Figure 5.35 shows the impact of a fabrication process with 5% of deviation when the standard version or circuit-level mitigation approaches are adopted in the design. The best technique to attenuate the impact on power variability is based on the insertion of Schmitt Triggers. Even for lower levels of deviation, the addition of Schmitt Trigger remains the most advantageous. After that, the most indicated technique to power variability mitigation is the insertion of sleep transistors or decoupling cells. For designs with 5% of deviation, the

improvement of both techniques is similar. However, for lower levels of WF fluctuation (1-4%), the sleep transistor approach is the second best option. Finally, the technique with fewer gains on power variability attenuation is the transistor reordering.

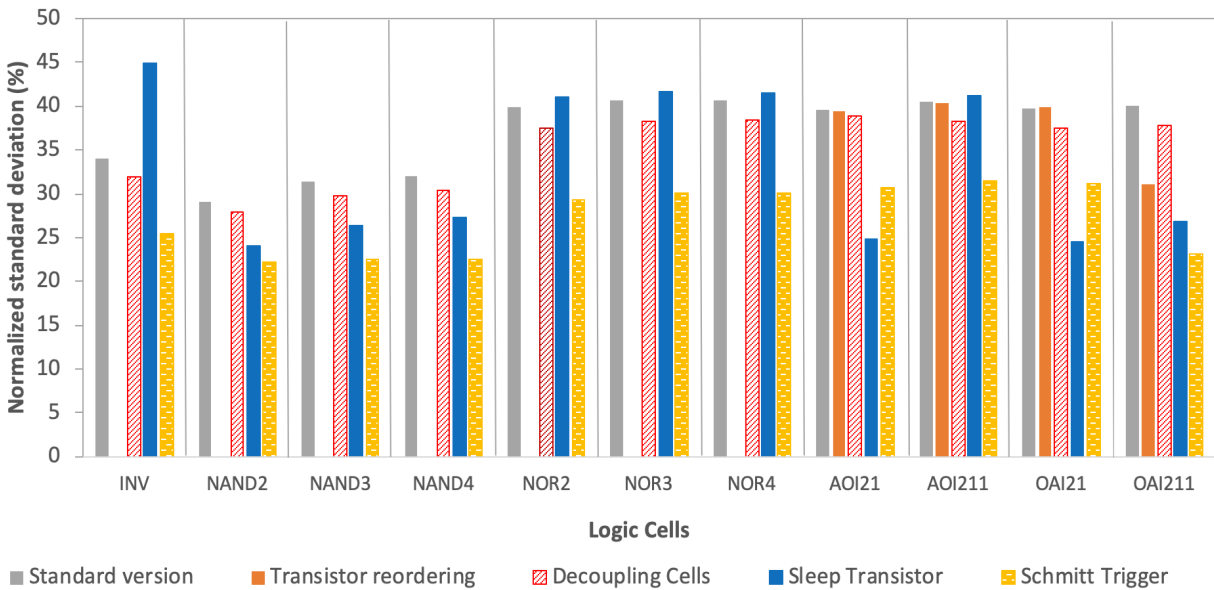
Figure 5.35: Power variability using circuit-level mitigation approaches



Source: From the author

For the delay variability mitigation, it is harder to find a general trend for all logic cells evaluated, as shown in Figure 5.36. Except for the AOI21 and OAI21 cells, the insertion of a Schmitt Trigger is the best technique to improve the delay variability. The second alternative also varies according to the logic cells. For example, the adoption of a sleep transistor is better than decoupling cells for the NAND and OAI211 cells, but the opposite happens for the INV, NOR, and AOI211 cells. For the AOI21 and OAI21 cells, the first best option is using the sleep transistors, and after, the Schmitt Trigger transistor is more indicated. The transistor reordering technique only brought significant advantages of delay variability mitigation for the OAI211 cell. For lower levels of WF fluctuations (1-4%), the same tendency was observed for all logic cells.

Figure 5.36: Delay variability using circuit-level mitigation approaches



Source: From the author

The four techniques used to mitigate the effects of process variations and radiation-induced soft errors introduced some penalties regarding area, power consumption, and performance. Transistor reordering technique has no area penalties, and the impact on power and performance is small. However, this technique not presented significant improvements to the effects caused by process variations on complex cells. Moreover, the reordering of transistors becomes the logic cells more sensitive to soft errors.

The connection of Schmitt Trigger in the output of logic cells is the best way to decrease the impact of process variations significantly and also to obtain logic cells free of faults even at the near-threshold regime. However, higher penalties are observed, mainly regarding power consumption and performance. The insertion of decoupling cells has the same area penalty of Schmitt Trigger technique, but the drawbacks in power consumption and performance are halved. Moreover, a design with decoupling cells decreases the soft error susceptibility of logic gates. The sleep transistor approach introduced low area penalties and logic cells free of faults even at near-threshold regime, but the impact on power consumption and performance is considerable. For most of techniques and logic cells analyzed, the penalties are higher with lower levels of WF fluctuation.

Decoupling cells with a larger number of fins increases, even more, the robustness of logic cells. However, the penalties increase as the number of fins also increases. But for this technique, the penalties introduced are still agreeable. In the same way, larger Schmitt Triggers in the design increases the power variability mitigation, but the technique drawbacks on power consumption and performance are unacceptable. On the other hand, sleep transistors with a larger number of fins does not minimize the sensitivity of logic cells significantly. For this reason, larger sleep transistors are not advised due to the high penalties involved.

In general, considering the average results of logic cells obtained for all circuit-level mitigation approaches as well as an overall evaluation about all topics and test scenarios presented in this work, it is possible to conclude that:

1. Schmitt Trigger is the best technique if the focus of designers is only improving the impact of variability, without any area, performance or power requirements;
2. Sleep transistor is the best option if the focus of designers is in increasing the process variability robustness, but they have some area restrictions;
3. Decoupling cells are indicated if the focus of designers is in improving the impact of variability, but they have some power or performance requirements;
4. Sleep transistor or Schmitt Trigger are the best choices if the focus of designers in only decrease the soft error susceptibility;
5. Sleep transistor is more indicated if the focus of designers is attenuate the impact of soft errors, but they have some area constraints;
6. Decoupling cells is the best alternative if the focus of designers is in improving the process variability effects and also become a circuit more robust to transient faults, with acceptable penalties on area, performance, and power consumption.

As previously mentioned in the introduction, few works are exploring circuit-level approaches to mitigate the effects of process variability and soft error in FinFET technologies. Currently, there are four works available in the literature directly related to the subject of this thesis.

In (MORAES et al., 2018), the traditional inverters of FinFET full adders were replaced by Schmitt Triggers at the layout level, and the process variability sensitivity of these circuits was

verified. For the most cases evaluated, the adoption of Schmitt Triggers improves the power and delay variability, but with significative overhead, mainly on the area. The results obtained in (MORAES et al., 2018) are in agreement with those presented in this thesis. However, all overheads are more prominent due to the insertion of more than one Schmitt Trigger in the design of full adders.

In (BRENDLER et al., 2018b), different complex cells were designed at the layout level using the multi-level design (only with NAND gates). The process variability and soft error sensitivity were analyzed considering both topologies. Despite the area impact, the multi-level design mitigates at least 50% the delay variability when compared with the version of complex gates. Moreover, the multi-level version improves over 45%, on average, the fault coverage evaluation from SET effects. The improvements obtained in (BRENDLER et al., 2018b) are similar to the Schmitt Trigger technique applied in this thesis, but the penalties on area, delay, and power are higher. The comparison among the soft error results is not fare, because in (BRENDLER et al., 2018b), the fault injection happens though the double-exponential current using SPICE simulations.

In (CALOMARDE et al., 2014) and (ALGHAREB et al., 2017), circuit-level techniques based on the strengthening and redundancy were applied in FinFET circuits to enhance the soft error susceptibility, respectively. Although both approaches demonstrated very promising outcomes regarding soft error robustness, the experiments consider the estimation using the double exponential and are not considering the layout features. In this way, the comparison with this thesis also does not suitable.



# Chapter 6: Conclusions

---

FinFET devices were widely adopted by the semiconductor industry for technology nodes sub-22nm, raising essential topics related to the reliability of electronic systems. The small geometric patterns imposed by advanced technologies intensify the process variations as well as the higher density allows that a single energetic particle affects multiple adjacent nodes. The main consequences of these challenges are the parametric yield loss, and the critical failures on system behavior, which can lead to financial or human life losses. The impact of process variability continues to increase at each new technology node, becoming harder to keep the technology scaling down using FinFET devices. From a design standpoint, process variations and radiation-induced soft errors in FinFET nodes require an accurate estimative, besides new design methodologies able to reduce the effects caused by them.

According to the literature review, there are few works proposing techniques to attenuate the impact of the process variations and soft errors, specifically for FinFET technologies. Moreover, there is a lack of circuit-level mitigation approaches exploring changes in the design to achieve more robust solutions. In this way, this thesis advances the state-of-the-art providing:

1. The evaluation of FinFET logic cells under process variability and radiation effects using a 7-nm FinFET predictive process design kit (PDK);
2. The design of logic cells using four different circuit-level approaches to mitigate the impact caused by work-function fluctuations and soft errors;
3. A trade-off between the gains and penalties of each approach regarding the area, performance, power consumption, SET pulse width, and SET cross-section;
4. The mitigation tendency of the circuit-level techniques when different levels of the process variation, transistor sizing, and LET were applied in the design.

The circuit-level mitigation approaches explored in this thesis were the transistor reordering, and the insertion of decoupling cells, Schmitt Triggers, and sleep transistors.

In general, all these techniques reduce the process variability effects and the soft error susceptibility, introducing fewer penalties, implementation cost, and design complexity when compared with the few alternatives available in the literature.

The transistor reordering technique can increase up to 8% the robustness of complex cells under process variations (5% of deviation). However, this method is not favorable to soft error mitigation, increasing the susceptibility of complex cells up to 20% for low LETs. Among all technique evaluated, the transistor reordering presented fewer power and performance overheads, besides it has no area penalties.

The adopting of decoupling cells shows interesting outcomes for power variability control under levels of variation above 4%. On the other hand, this technique is efficient for the reduction of delay variability independently of the levels of variation. The higher improvements in the delay variability can be seen for lower levels of variation (1-3%). The design with decoupling cells decreases the soft error susceptibility around 10% for a high LET ( $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ). The gains with lower LETs can reach a maximum of 4%. This technique presented a large area overhead, but a smaller impact on power and performance metrics.

The best approach to control the process variations is the connection of a Schmitt Trigger in the output of FinFET cells. This technique can improve the delay variability up to 50%, mainly for manufacturing process with 2-4% of WF deviations. For the power variability, higher robustness was obtained with higher levels of variations (4-5%). Moreover, all logic cells investigated are free of faults, even at the near-threshold regime (0.3V) and under the influence of a high LET ( $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ). However, as this technique adds six extra transistors, it introduces higher penalties in area and power.

The insertion of a sleep transistor between the pull-down network and the ground rail is advantageous mainly for power variability control. The improvements for some cells exceed 10% for higher levels of variation (4-5%). On the other hand, the efficiency of this method for delay variability reduction depends on how the transistors are arranged with the sleep transistor in the pull-down network. This technique is also free of faults, even at the near-threshold regime (0.3V) and under the influence of a high LET ( $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ). The layout

with a sleep transistor introduces a small area overhead, but the impact in power and performance metrics is very significant.

A design with larger decoupling cells (four or five fins) is advantageous for process variability mitigation, with an acceptable increase on overheads. The Schmitt Trigger with a larger number of fins also improves the sensibility to WF fluctuations, but the technical drawbacks involved are unacceptable. On the other hand, increasing the sizing of the sleep transistor not change the sensitivity to process variability significantly.

The choice of the more appropriate technique depends on the target application, and its requirements regarding area, power consumption, and performance. The Schmitt Trigger technique presented the best results for process variability mitigation and radiation hardness. However, this approach introduces critical penalties on area, delay, and power consumption. In this way, if a designer wants to improve the reliability of the circuit introducing more acceptable penalties, a design with decoupling cells is more indicated to control the delay variability. On the other hand, for obtain a reduction in the power variability and soft error susceptibility, the best option is to use the sleep transistor technique.

Finally, this thesis provides a set of information useful to help: 1) the semiconductor industry to obtain a parametric yield improvements avoiding the many stages of redesign; 2) the designers to introduce a mitigation technique at the layout level for a given application knowing all the pros and cons of adopting it; and 3) the aerospace industry such as ONERA, the French Aerospace Lab, to design more reliable systems for the next generation of nano-satellite constellations.

## **6.1. Future Works**

There are several possibilities of new experiments and test scenarios that can be done from this thesis. First, it is possible to extend this research exploring two more potential approaches for improving the robustness of FinFET logic cells: multi-finger design (FORERO et al., 2017) and dual-gate pitch (MARELLA et al., 2015). Both techniques should be implemented at the layout level.

An in-depth study can be done to discover the best places to put these cells in a chain of gates, such that it is not practical to apply decoupling cells, Schmitt Triggers, or sleep transistors in all logic cells of integrated circuits. Also, it is crucial to understand better as each technique contributed to attenuate the effects of process variations and radiation-induced soft errors. Moreover, some ways to reduce the technique drawbacks (area, power, delay) imposed by the circuit-level mitigation approaches explored in this work need to be investigated.

Another possibility of future work is the evaluation of WF fluctuations and the soft errors together, considering the worst-case scenario of faults to introduce the process variations on circuits. Furthermore, the impact of the process variations also can be estimated using as metric the power-delay-product (PDP), which offers an accurate trade-off between the results of power and delay variability. Finally, a cell library for digital designs can be developed focusing on reliability issues, such as process variability mitigation and radiation hardness.

# References

---

- AGARWAL, S. et al., *Ab initio* Study of Metal Grain Orientation-Dependent Work Function and its Impact on FinFET Variability, **IEEE Transactions on Electron Devices**, vol. 60, n. 9, 2013.
- AGOSTINELLI, M.; ALIOTO, M.; ESSENI, D.; SELMI, L., Design and evaluation of mixed 3T-4T FinFET stacks for leakage reduction, **Integrated Circuit and System Design**, p. 31-41, 2009.
- AGUIAR, Y.; ZIMPECK, A. L.; MEINHARDT, C.; REIS, R., Temperature dependence and ZTC bias point evaluation of sub 20nm bulk multigate devices, **IEEE International Conference on Electronics Circuits and Systems (ICECS)**, 2017a.
- AGUIAR, Y. et al., Evaluation of radiation-induced soft error in majority voters designed in 7 nm finfet technology, **Microelectronics Reliability**, vol. 76-77, p. 660-664, Elsevier, 2017b.
- AGUIAR, Y.; MEINHARDT, C.; REIS, R. A. Radiation sensitivity of xor topologies in multigate technologies under voltage variability, **IEEE Latin American Symposium on Circuits & Systems (LASCAS)**, p. 1–4, 2017.
- AHLBIN, J. R. et al., Influence of N-Well Contact Area on the Pulse Width of Single-Event Transients, **IEEE Transactions on Nuclear Science**, vol. 58, n. 6, 2011.
- ALGHAREB, F. S. et al., Energy and Delay Tradeoffs of Soft-Error Masking for 16-nm FinFET Logic Paths: Survey and Impact of Process Variation in the Near-Threshold Region, **IEEE Transactions on Circuits and Systems**, vol. 64, n.6, 2017.
- ALIOTO, M., Analysis of Layout Density in FinFET Standard Cells and Impact of Fin Technology. **IEEE International Symposium on Circuits and Systems (ISCAS)**, p. 3204-3207, 2010.
- ALIOTO, M. Comparative Evaluation of Layout Density in 3T, 4T and MT FinFET Standard Cells. **IEEE Trans. On Very Large Scale Integration (VLSI) Systems**, v.19, n.5, May, 2011.
- ALIOTO, M.; CONSOLI, E.; PALUMBO, G., Variations in nanometer CMOS flip-flops: Part I - Impact of process variations on timing, **IEEE Transactions on Circuits and Systems**, vol. 62, no. 8, p. 2035-2043, 2015.
- ALLES, M. L. et al., Radiation hardness of FDSOI and FinFET technologies, **IEEE International SOI Conference**, 2011.
- ALLES, M. L. et al., Total-Ionizing-Dose Response of Narrow Long Channel 45 nm PDSOI Transistors, **IEEE Transactions on Nuclear Science**, vol. 61, no. 6, pp. 2945, 2014.
- AMBACQ, P. et al., Analog and RF circuits in 45 nm CMOS and below: planar bulk versus FinFET, **Proc eur solid-state device research conf**, p. 54-57, 2006.
- ANDJELKOVIC, M. et al., Use of decoupling cells for mitigation of SET effects in CMOS combinational gates, **IEEE International Conference on Electronics, Circuits and Systems (ICECS)**, pp. 361-364, 2018.
- ANGHEL, L.; REBAUDENGO, M.; REORDA, M. S.; VIOLANTE, M., Multi-level Fault Effects Evaluation. In: VELAZCO, R.; FOUILLAT, P.; REIS, R. (Ed.). **Radiations Effects on Embedded Systems**. Springer, p.69 – 88, 2007.
- ANIL, K.G.; HENSON, K.; BIESEMANS, S.; COLLAERT, N., Layout density analysis of FinFETs. **Proceedings of the Conference on European Solid-State Device Research**, p. 139-142, 2003.

ARTOLA, L.; HUBERT, G; ALIOTO, M., Comparative Soft Error Evaluation of Layout Cells in FinFET Technology, **Microelectronics Reliability**, vol. 54, issues 9-10, p. 2300-2305, Elsevier, 2014.

ARTOLA, L. et al. Modeling single event transients in advanced devices and ics. **IEEE Transactions on Nuclear Science**, v. 62, n. 4, p. 1528–1539, 2015.

ATKINSON, N. M. et al., Layout technique for single-event transient mitigation via pulse quenching, **IEEE Transactions on Nuclear Science**, vol. 58, n. 3, 2011.

AUTH, C., 22-nm fully-depleted tri-gate CMOS transistors, **Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)**, pp. 1-6, 2012.

AUTRAN, J-L; MUNTEANU, D., Soft Errors: From Particles to Circuits, CRC Press, 2015.

AVCI, M., M.Y. BABAC, AND T. YILDIRIM. Neural network-based MOSFET channel length and width decision method for analog integrated circuits. **International Journal of Electronics**, [S.l: s.n.], v.92, p.281–293, May 2005.

BAILEY, G. E. et al, Double pattern solutions for 32nm hp and beyond, **Design for Manufacturability through design-process integration, Proceedings of the SPIE**, vol. 6521, 2007.

BARRAUD, S. et al., "Performance and Design Considerations for Gate-All-Around Stacked-NanoWires FETs", **IEEE International Electron Devices Meeting**, 2017.

BARTH, J. L. et al., Space, atmospheric, and terrestrial radiation environments, **IEEE Trans. Nucl. Sci.**, 50(3), p. 466-482, 2003.

BAUMANN, R. C., Radiation-induced soft errors in advanced semiconductor technologies. In: IEEE Transaction on Device and Materials Reliability, 2005. **Proceedings...** [S.l]: IEEE, 2005, p. 305-316.

BHATTACHARYA, D.; JHA, N. K., Finfets: From devices to architectures. **Advances in Electronics**, Hindawi Publishing Corporation, v. 2014, 2014.

BHOJ, A. N.; JHA, N. K., Design of logic gates and flip-flops in high-performance FinFET technology, **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, vol. 21, no. 11, p. 1975–1988, 2013.

BHUNIA et al., Arbitrary Two-Pattern Delay Testing Using a Low-Overhead Supply Gating Technique, **Journal of Electronic Testing**, vol. 24, n. 6, p. 577-590, 2008.

BHUVA, B. L. et al., Multi-Cell Soft Errors at Advanced Technology Nodes, **IEEE Transactions on Nuclear Science**, vol. 62, n. 6, 2015.

BLESFORD, K., Let's Get Physical. Available in: <https://blogs.synopsys.com/letsgetphysical/2014/09/26/how-do-finfects-impact-physical-verification-drclvs/>, 2014. Access in: May, 2018.

BORKAR, S., Designing reliable systems from unreliable components: the challenges of transistor variability and degradation, **IEEE Micro**, vol. 25, n. 6, 2005.

BORKAR, S., Design perspectives on 22nm CMOS and beyond, **Design Automation Conference (DAC)**, 46, 2009. ACM/IEEE, 2009, p. 93-94.

BORREMAN, J. et al. Perspective of RF design in future planar and FinFET CMOS, **IEEE radio freq integrated circuits symp**, Atlanta, USA, p. 75–78, 2008.

BOUKORTT et al., Silicon: Electrical Characteristics of 8-nm SOI n-FinFETs, **Silicon Journal**, vol. 8, no. 4, p. 497-503, Springer, 2016.

BRAIN, R., 14nm technology leadership, **Technology and Manufacturing Day**, Intel. Available in: <https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2017/03/Ruth-Brain-2017-Manufacturing.pdf>, 2017. Access in: Jul, 2018.

BRENDLER, L. H. et al, Evaluating the impact of process variability and radiation effects on different transistor arrangements, to be published in **IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)**, 2018.

BRENDLER, L. H. et al, Exploring multi-level design to mitigate variability and radiation effects on 7nm FinFET logic cells, **IEEE International Conference on Electronics Circuits and Systems (ICECS)**, pp. 581-584, 2018.

BUTZEN, P. F. et al., Transistor network restructuring against NBTI degradation, **Microelectronics Reliability**, vol. 50, p. 1298-1303, 2010.

CALOMARDE et al., SET and noise fault tolerant circuit design techniques: application to 7nm FinFET, **Microelectronics Reliability**, vol. 54, p. 738-745, 2014.

CAO, Y.; CLARK, L. T., Mapping statistical process variations toward circuit performance variability: an analytical modeling approach, **Design Automation Conference (DAC)**, p. 658-663, 2005.

CARTWRIGHT, J.; Intel enters the third dimension, **Nature International Weekly Journal of Science**. Available in: <https://www.nature.com/news/2011/110506/full/news.2011.274.html>, 2011. Access in: Apr, 2011.

CATHIGNOL, A. et al., Quantitative evaluation of statistical variability sources in a 45-nm technological node LP N-MOSFET, **IEEE Electron Device Letters**, vol. 29, n. 6, 2008.

CHANCELLOR, J. C. et al., Space Radiation: the Number One Risk to Astronaut Health beyond Low Earth Orbit, Special Issue: Response of Terrestrial Life to Space Conditions, vol. 4, pp. 491-510, 2014.

CHANDLER, D. L., MIT News Office. Available in: <http://news.mit.edu/2012/explained-sigma-0209>, 2012. Access in: Jun, 2018.

CHANG, J. B. et al., Scaling of SOI FinFETs down to fin width of 4nm for the 10nm technology node, **Proceedings of the Symposium on VLSI Technology, Systems and Applications**, p. 12-13, 2011.

CHANG, K. et al., Full-chip monolithic 3D IC design and power performance analysis with ASAP7 library, **IEEE/ACM International Conference on Computer-Aided Design (ICCAD)**, 2017.

CHATTERJEE, I. et al., Length and fin number dependence of ionizing radiation-induced degradation in bulk FinFETs, **IEEE International Reliability Physics Symposium (IRPS)**, 2013.

CHATTERJEE, I. et al., Geometry dependence of total-dose effects in bulk FinFETs, **IEEE Transactions on Nuclear Science**, vol. 61, n. 6, 2014.

CHATZIKYRIAKOU E.; MORGAN, K.; GROOT, C. H. K., Total Ionizing Dose Hardened and Mitigation Strategies in Deep Submicrometer CMOS and Beyond, **IEEE Transactions on Electron Devices**, vol. 65, n. 3, 2018.

CHAUDHURI, S.; MISHRA, P.; JHA, N. K., Accurate leakage estimation for FinFET standard cells using the response surface methodology, **Proceedings of the International Conference on VLSI Design (VLSID)**, p. 238–244, 2012.

CHAUHAN et al., FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard, Elsevier, 2015.

CHAVA, B. et al. Standard cell design in n7: Euv vs. immersion, **Proc. SPIE**. v. 9427, p. 94270E–94270E, 2015.

CHEN, J. et al., Novel layout technique for N-hit single-event transient mitigation via source-extension, **IEEE Transactions on Nuclear Science**, vol. 59, n. 6, 2012a.

CHEN, J. et al., Simulation Study of the Layout Technique for P-hit Single-Event Transient Mitigation via the Source Isolation, **IEEE Transactions on Device and Materials Reliability**, vol. 12, n. 2, 2012b.

CHEN, J. et al., Novel layout technique for single-event transient mitigation using dummy transistor, **IEEE Transactions on Devices and Materials Reliability**, vol. 13, n. 1, 2013.

CHUN, J. W.; CHEN, C. Y., Transistor and pin reordering for leakage reduction in CMOS circuits, **Microelectronics Journal**, vol. 53, p. 25-34, 2016.

CLARK, L. T. et al., ASAP7: A 7-nm FinFET Predictive Process Design Kit, **Microelectronics Reliability**, vol. 53, pp. 105-115, Elsevier, 2016.

CLEMENS, M. A; Energy Deposition Mechanisms for Proton-and-neutron-induced single event upsets, Thesis (PhD) — Vanderbilt University, 2012.

COLLINGE, J.-P. FinFET and Other Multi-Gate Transistors, Springer, Berlin, 2008.

COLLINS, L. FinFET Variability Issues Challenges Advantages of New Process. Available in: [http://www.techdesignforums.com/blog/2014/04/16/finfet-variability\\_challenges-advantages/](http://www.techdesignforums.com/blog/2014/04/16/finfet-variability_challenges-advantages/), 2014. Access in: Nov, 2016.

CONLEY, A., FinFET vs. FD-SOI: Key Advantages & Disadvantages, Technical Marketing, ChipEx. Available in: [http://www.chipex.co.il/\\_Uploads/dbsAttachedFiles/ChipExAMAT.pdf](http://www.chipex.co.il/_Uploads/dbsAttachedFiles/ChipExAMAT.pdf), 2014. Access in: Mar, 2018.

CUI, T. et al., 7nm FinFET standard cell layout characterization and power density prediction in near- and super-threshold voltage regimes, **IEEE International Green Computing Conference**, 2014.

CUMMINGS, D. J. Enhancements in CMOS device simulation for single-event effects. Thesis (PhD) — University of Florida, 2010.

DADGOUR, H.F., DE, V. K., BARNERJEE, K., "Statistical Modeling of Metal-Gate Work-Function Variability in Emerging Device Technologies and Implications for Circuit Design, **ICCAD**, 2008.

DADGOUR, H.F.; ENDO, K.; DE, V. K.; BANERJEE K., Grain-Oriented Induced Work Function Variation in Nanoscale Metal-Gate Transistors - Part I - Modeling, Analysis and Experimental Validation, **IEEE Tran. on Elec. Dev.**, vol. 57, pp. 2504-2514, 2010.

DAI et al., Latchup in bulk FinFET technologies, **IEEE International Reliability Physics Symposium (IRPS)**, 2017

DAS, R.; BAISHYA, S., Investigation of work function and temperature of germanium FinFETs, **International Conference on Electron Devices and Solid-State Circuits (EDSSC)**, 2017.



DATTA, A et al., Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices, **IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems**, v.26, n.11, p. 1957-1966, 2007.

DESHMUKH, R. et al., Comparing FinFETs: SOI Vs Bulk: Process variability, process cost, and device performance, **International Conference on Computer, Communication and Control (IC4)**, 2015.

DING, Y.; CHU, C.; MAK, W-K., Detailed routing for Spacer-Is-Metal type Self-Aligned Double/Quadruple Patterning Lithography, **ACM/EDAC/IEEE Design Automation Conference (DAC)**, 2015.

DODD, P. E. et al., Current and future challenges in radiation effects on CMOS electronics, **IEEE Transactions on Nuclear Science**, vol. 57, n. 4, p. 1747–1763, 2010.

DOKANIA, V.; ISLAM, A., Circuit-level design technique to mitigate impact of process, voltage and temperature variations in complementary metal-oxide semiconductor full adder cells, **IET Circuits, Devices & Systems**, vol. 9, n. 3, p. 204-212, 2015.

DORIS, B. et al., Device design considerations for next generation CMOS technology: planar FDSOI and FinFET (invited), **Proceedings of the International Symposium on VLSI technology, Systems and Applications (VLSI-TSA)**, p. 1-2, 2013.

EBRAHIMI, M. et al., Layout-Based Modeling and Mitigation of Multiple Event Transients, **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, vol. 35, n. 3, 2016.

ENDO, K. et al., Variation analysis of TiN FinFETs, **International Semiconductor Device Research Symposium (ISDRS)**, 2009.

ENDO, K. et al., Independent double-gate FinFET SRAM technology, **Proceedings of the IEEE International Nanoelectronics Conference (INEC)**, p. 1–2, 2011.

EL MAMOUNI, F. et al., Laser and heavy ion-induced charge collection in bulk FinFETs, **IEEE Transactions on Nuclear Science**, vol. 58 (6), pp. 2563-2569, 2011.

FACCIO, F., Design Hardening Methodologies for ASICs. Radiation Effects on Embedded Systems, p. 143–160, 2007.

FAN, M., WU, Y., HU, V.P.-H., SU, P. CHUANG, C. Investigation of Cell Stability and Write Ability of FinFET Subthreshold SRAM Using Analytical SNM Model. **IEEE Transactions on Electron Devices**, vol.57, no.6, pp.1375,1381, June 2010.

FANG, Y-P; OATES, A. S., Neutron-Induced Charge Collection Simulation of Bulk FinFET SRAMs Compared With Conventional Planar SRAMs, **IEEE Transactions on Device and Materials Reliability**, vol. 11, n. 4, 2011.

FORERO et al., Analysis of short defects in FinFET based logic cells, **IEEE Latin American Test Symposium (LATS)**, 2017.

FRANK, D. J.; DENNARD, R. H.; NOWARK, E., SOLOMON, P. M.; TAUR, Y.; WONG, H-S. P., Device Scaling Limits of Si MOSFETs and their Application Dependencies, **Proceedings of the IEEE**, 89(3):259–288, Mar. 2001.

GHAI, D., MOHANTY, S.P., KOUGIANOS, E. Design of Parasitic and Process- Variation Aware Nano-CMOS RF Circuits: A VCO Case Study. **IEEE Transaction**

**VLSI Systems**, v.17, p.1339–1342, Sep. 2009

GHAIDA, R. S. et al., Layout decomposition and legalization for double-patterning technology, **IEEE Transactions on Computer-Aided design of Integrated Circuits and Systems**, vol. 32, no. 2, 2013.

GSS – Gold Standard Simulations Ltd. Case Study: Statistical Variability in an Example

22nm FinFET. 2010. Available in: [http://www.goldstandardsimulations.com/GSS\\_22nm\\_FinFET\\_case\\_study.pdf](http://www.goldstandardsimulations.com/GSS_22nm_FinFET_case_study.pdf). Access in: May, 2018.

GU, J.; KEANE, J.; SAPATNEKAR, S.; KIM, C. H., Statistical leakage estimation of double gate FinFET devices considering the width quantization property, **IEEE Transactions on Very Large Scale Integration Systems**, vol. 16, n. 2, pp. 206-209, 2008.

GUILLORN, M. et al., FinFET performance advantage at 22nm: an AC perspective, **Proceedings of the Symposium in VLSI Digest of Technical Papers**, p. 12-13, 2008.

GUO, Z. et al., FinFET-based SRAM design, **Proceedings of the International Symposium on Low Power Electronics and Design**, pp. 2–7, 2005.

GUPTA, P.; PAPADOPOULOU, E., Yield analysis and optimization, **The Handbook of Algorithms for VLSI Physical Design Automation**. RC Press, 2011.

GUPTA, S. K.; ROY, K., Device-circuit co-optimization for robust design of finfet-based srams. **IEEE Design & Test**, v. 30, n. 6, pp. 29–39, Dec 2013.

HARISH B.P., N. BHAT, AND M.B. PATIL. On a Generalized Framework for Modeling the Effects of Process Variations on Circuit Delay Performance Using Response Surface Methodology, **IEEE Transactions on CADICS**, v.26, p.606–614, Mar. 2007.

HARTMANN, F., Silicon Detectors. Available in: [http://isapp.ba.infn.it/2009karlsruhe/www.kceta.kit.edu/downloads/Hartmann\\_Si-Detectors.pdf](http://isapp.ba.infn.it/2009karlsruhe/www.kceta.kit.edu/downloads/Hartmann_Si-Detectors.pdf). Access in: Jul, 2018.

HENDERSON, C. L., Failure analysis techniques for a 3D world, **Microelectronics Reliability**, Vol. 53, i. 9-11, pp. 1171-1178, Elsevier, 2013.

HIBBEN, N., TSMC, not Intel, has the lead in Semiconductor processes. Available in: <https://seekingalpha.com/article/4151376-tsmc-intel-lead-semiconductor-processes>, 2018. Access in: Jun, 2018.

HISAMOTO, D., KAGA, T., KAWAMOTO, Y., TAKEDA, E., A fully depleted lean channel transistor (DELTA) - a novel vertical ultra thin SOI MOSFET. **Technical Digest of IEDM**, 833, 1989.

HISAMOTO, D., et al., FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. **IEEE Transactions on Electron Devices**, pp. 47-12 , 2320, 2000.

HSU, C.-L. et al., Layout-dependent aging mitigation for critical path timing, **Asia and South Pacific Design Automation Conference (ASP-DAC)**, 2018.

HU, C., New sub-20nm transistors: why and how, **Proceedings of the Design Automation Conference (DAC)**, p. 460-463, 2011.

HUANG, D. S. et al., Comprehensive device and product level reliability studies on advanced CMOS technologies featuring 7nm high-k metal gate FinFET transistors, **IEEE International Reliability Physics Symposium (IRPS)**, 2018.

HUBERT, G. et al., Operational SER calculations on the sac-c orbit using the multi-scales single event phenomena predictive platform (MUSCA SEP3), **IEEE Transactions on Nuclear Science**, v. 56, n. 6, p. 3032–3042, 2009.

HUBERT, G.; ARTOLA, L.; REGIS, D. Impact of scaling on the soft error sensitivity of bulk, fdsoi and finfet technologies due to atmospheric radiation. **Integration, the VLSI journal, Elsevier**, v. 50, p. 39–47, 2015.

HUGHES, H. et al., Total ionizing dose radiation effects on 14nm FinFET and SOI UTBB technologies, **IEEE Radiation Effects Data Workshop (REDW)**, 2015.

INTEL, Intel's 10nm Technology: Delivering the Highest Logic Transistor Density in the Industry Through the Use of Hyper Scaling, Available in: <https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2017/09/10-nm-icf-fact-sheet.pdf>, 2017. Access in: May, 2018.

ISLAM, A.; AKRAM, M. W.; HASAN, M., Variability immune FinFET-based full adder design in subthreshold region, **International Conference on Devices and Communications (ICDeCom)**, p. 1-5, 2011.

ITRS. The International Technology Roadmap for Semiconductors. Available in: <http://www.itrs2.net/2011-itrs.html>, 2011. Access in: May, 2018.

JAMES, D., Intel to present on 22-nm Tri-gate Technology at VLSI Symposium. Available in: [https://electroi.com/chipworks\\_real\\_chips\\_blog/2012/04/12/intel-to-present-on-22-nm-tri-gate-technology-at-vlsi-symposium/](https://electroi.com/chipworks_real_chips_blog/2012/04/12/intel-to-present-on-22-nm-tri-gate-technology-at-vlsi-symposium/), 2012. Access in: Jul, 2018.

JANAKIRAMAN, V., BHARADWAJ, A.; VISVANATHAN, V., Voltage and Temperature Aware Statistical Leakage Analysis Framework Using Artificial Neural Networks. **IEEE Transaction on CADICS**, v.29, p.1056–1069, Jul. 2010.

JIANG, X. et al., Device-level characterization approach to quantify the impacts of different random variation sources in FinFET technology, **IEEE Electron Device Letters**, vol. 37, n. 8, 2016.

JOSHI, R.; KIM, K.; KANJ, R., FinFET SRAM design, **Proceedings of the International Conference on VLSI Design (VLSID)**, p. 440–445, 2010.

JUNG-HWAN, C.; MURTHY, J.; ROY, K., The effect of process variation on device temperature in FinFET circuits, **IEEE/ACM International Conference on Computer-Aided Design**, p. 747-751, 2007.

KANG, M. et al., FinFET SRAM optimization with fin thickness and surface orientation, **IEEE Transactions on Electron Devices**, vol. 57, no. 11, p. 2785–2793, 2010.

KARAPETYAN, S.; KLEEBERGER, V.; SCHLICHTMANN, U., FinFET-based product performance: Modeling and evaluation of standard cells in FinFET technologies, **Microelectronics Reliability**, vol. 61, p. 30-34, 2015.

KAWA, J., FinFET Design Manufacturability, and Reliability, Synopsys Design Aware Technical Bulletin, 2013.

KHALID, U.; MASTRANDREA, A.; OLIVIERI, M., Effect of NBTI/PBTI aging and process variations on write failures in MOSFET and FinFET flip-flops, **Microelectronics Reliability**, vol. 55, p. 2614-2626, 2015.

KIAMEHR, S. et al., Radiation-Induced Soft Error Analysis of SRAMs in SOI FinFET Technology: A Device to Circuit Approach, **Design Automation Conference (DAC)**, 2014.

KIM, S-D et al., "Performance Trade-offs in FinFET and Gate-All-Around Devices Architectures for 7nm-node and Beyond", **IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference**, 2015.

KING, T.-J. FinFETs for Nanoscale CMOS Digital Integrated Circuits, **International Conference. on Computer-Aided Design (ICCAD)**, v. 1, n. 1, p. 207–210, 2005.

KING, M. P. et al., Analysis of TID Process, Geometry, and Bias Condition Dependence in 14nm FinFETs and Implications for RF and SRAM Performance, **IEEE Transaction on Nuclear Science**, vol. 64, n.1, p. 285-292, 2017.

KLEEBERGER, V.B.; GRAEB, H.; SCHLICHTMANN, U. Predicting future product performance: Modeling and evaluation of standard cells in FinFET technologies, **Proceedings of the Design Automation Conference (DAC)**, 2013.

KLEIN, R., Overview of process variability, **Proc. ISSCC Microprocessor Forum F6: Transistor Variability Nanometer-Scale Technol.**, p. A1-A24, 2008.

KUHN, K. J. et al. Process technology variation. **IEEE Transactions on Electron Devices**, v. 58, n. 8, p. 2197–2208, 2011.

KUMAR, V. R., KIRUBARAJ, A. A., Submicron 70nm CMOS Logic Design with FinFETs, **International Journal of Engineering Science and Technology**, v.2, n.9, p. 4751-4758, 2010.

KUMAR, U. S.; RAO, V. R, Thermal performance of nano-scale soi and bulk finfets, **IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)**, p. 1566–1571, 2016.

LEE, S. et al., Radiation-induced soft error rate analyses for 14nm FinFET SRAM devices, **IEEE International Reliability Physics Symposium**, 2015.

LEE, Y.; SHIN, C., Impact of equivalent oxide thickness on threshold voltage variation induced by work-function variation in multigate devices, **IEEE Transactions on Electron Devices**, vol. 64, n. 5, 2017.

LIDEN, P., DAHLGREN, P., JOHANSSON, R., KARLSSON, J., On Latching Probability of Particle Induced Transient in Combinational Networks. In: 24th Symposium on Fault-tolerant Computing (FTCS), 1994. IEEE, 1994, p. 340-349.

LIU, Y.; XU, Q., On modeling faults in FinFET logic circuits, **IEEE International Test Conference**, 2012.

MALLIK, A. et al, Tease: A systematic analysis framework for early evaluation of finfet-based advanced technology nodes, **Design Automation Conference (DAC)**, 2013.

MARELLA et al., Optimization of FinFET-based circuits using a dual gate pitch technique, **IEEE/ACM International Conference on Computer-Aided Design (ICCAD)**, 2015.

MARKOFF, J., IBM Discloses Working Version of a Much Higher-Capacity Chip, available in: <https://www.nytimes.com/2015/07/09/technology/ibm-announces-computer-chips-more-powerful-than-any-in-existence.html>, 2015. Access in: May, 2018.

MAVIS, D. G.; EATON, P. H., Soft Error Rate Mitigation Techniques for Modern Microcircuits. In: Proc. 40th Annual Reliability Physics Symposium, 2002. IEEE, 2002, p. 216-225.

MEINHARDT, C., **Variabilidade em FinFETs**, Thesis (Doutorado em Ciência da Computação) – Instituto de Informática, UFRGS, Porto Alegre, 2014.

MEINHARDT, C., ZIMPECK, A. L., REIS, R., Predictive evaluation of electrical characteristics of sub-22nm FinFET technologies under device geometry variations, **Microelectronics Reliability**, vol. 54, n. 9-10, 2014a.

MEINHARDT, C., ZIMPECK, A. L., REIS, R., Impact of gate workfunction fluctuation on FinFET standard cells, **IEEE International Conference on Electronics, Circuits and Systems (ICECS)**, 2014b.

MENTOR GRAPHICS, As nodes advance, so must power analysis. Available in: <https://semiengineering.com/as-nodes-advance-so-must-power-analysis/>, 2014. Access in: Oct, 2018.

MENTOR GRAPHICS, The design and verification challenge for the next decade. Available in: [http://low-powerdesign.com/fosler\\_designandverify.htm](http://low-powerdesign.com/fosler_designandverify.htm). Access in: Jul, 2018.

MESSENGER, G. Collection of charge on junction nodes from ion tracks. **IEEE Transaction on Nuclear Science**, v. 29, n. 6, p. 2024–2031, 1982.

MISHRA, P.; MUTTREJA, A; JHA, N, FinFET Circuit Design. In: JHA, N., CHEN, D., Nanoelectronic Circuit Design. New York: Springer, 2011.

MONGA, U. et al., Charge-collection modeling for SER simulation in FinFETs, **Simulation of Semiconductor Processes and Devices**, 2016.

MOORE, G. E., Cramming more Components onto Integrated Circuits, **Electronics**, vol. 38, n. 8, pp. 114-117, 1965.

MORAES, L. B. et al., Evaluation of variability using Schmitt trigger on full adders layout, **Microelectronics Reliability**, vol. 88-90, pp. 116-121, 2018.

MORAES, L. B. et al., Minimum energy FinFET Schmitt Trigger design considering process variability, to be published in **IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-Soc)**, 2019.

MUNTEANU, D.; AUTRAN, J.-L., Modeling and simulation of single-event effects in digital devices and ics. **IEEE Transactions on Nuclear science**, 55(4):1854–1878, 2008.

MUTLU, A. A.; RAHMAN, M., Statistical Methods for the Estimation of Process Variation Effects on Circuit Operation, **IEEE Transaction on CADICS**, v.28, p.364–375, 2005.

MUTTREJA, A.; AGARWAL, N.; JHA, N. K., CMOS logic design with independent-gate FinFETs, **Proceedings of the IEEE International Conference on Computer Design (ICCD)**, p. 560–567, 2007.

NAGY et al., FinFET versus gate-all-around nanowire FET: Performance, scaling, and variability, **Journal of the Electron Devices Society**, vol. 6, 2018.

NARASIMHAM et al., Charge-Steering latch design in 16nm FinFET technology for improved soft error hardness, **IEEE Transactions on Nuclear Science**, vol. 64, n. 1, p. 353-358, 2017.

NASSIF, S. R., Design for variability in DSM technologies [deep submicron technologies], **IEEE First Int. Symp. on Quality Electronic Design (ISQED)**, Proceedings... [S.l:s.n.], p.451-454, 2000.

NASSIF, S. R., Process variability at the 65nm node and beyond. In: IEEE Custom Integrated Circuits Conference, 2008. p.1-8.

NAWAZ, S. M.; MALLIK, A., Effects of device scaling on the performance of junctionless FinFETs due to gate-metal work function variability and random dopant fluctuations, **IEEE Electron Device Letters**, vol. 37, n. 8, 2016.

NEUBERGER, G., G. WIRTH, R. REIS. Protecting Against Flip-Flop Hold Time Violations Due to Process Variations, **Latin-American Test Workshop (LATW)**. Proceedings..., p. 1-4, 2008.

NOWAK, E. J. et al, A functional FinFET-DGCMOS SRAM cell, **International Electron Devices Meeting, (IEDM)**, pp. 411-414, 2002.

NOWAK, E. J. et al., Turning silicon on its edge [double gate CMOS/FinFET technology], **IEEE Circuits and Devices Magazine**, vol. 20, n. 1, p. 20-31, 2004.

NSENGIYUMVA, P. et al., A comparison of the SEU response of planar and FinFET D flip-flop at advanced technology nodes, **IEEE Transactions on Nuclear Science**, vol. 63, n. 1, p. 266-272, 2016.

NSENGIYUMVA, P. et al. Analysis of Bulk FinFET Structural Effects on Single-Event Cross Sections, **IEEE Transactions on Nuclear Science**, v. 64, n. 1, p. 441–448, 2017.

O'BRYAN, M. V., Radiation Effects & Analysis - Single Event Effects. Nov. 2000. Available in: <<http://radhome.gsfc.nasa.gov/radhome/see.htm>>. Access in: May. 2018.

ORSHANSKY, M.; NASSIF, S.; BONING, D., **Design for Manufacturability and Statistical Design**. Springer, 2008.

OTHMAN, N. A. F.; HATTA, S. F. W. M.; SOIN, N., Impacts of fin width scaling on the electrical characteristics of 10-nm FinFET at different metal gate work function, **IEEE Regional Symposium on Micro and Nanoelectronics (RSM)**, 2017.

PANDEY et al., A modified method of Logical effort for FinFET circuits considering impact of fin-extension effects, **International Symposium on Quality Electronic Design (ISQED)**, 2018.

PARK, J. T.; COLINGE, J.-P.; DIAZ, C. H., Pi-gate SOI MOSFET, **IEEE Electron Device Letters**, vol. 22, no. 8, pp. 405-406, 2001.

POLJAK, M.; JOVANOVIC, V.; SULIGOJ, T., SOI vs. Bulk FinFET: Body Doping and Corner Effects Influence on Device Characteristics, **IEEE Mediterranean Electrotechnical Conference (MELECON)**, 2008.

POSSER, G. BELOMO, J.; MEINHARDT, C.; REIS, R. Performance Improvement with Dedicated Transistor Sizing for MOSFET and FinFET Devices, **IEEE Computer Society Annual Symposium on VLSI (ISVLSI)**, p.418-423, 2014.

POSSER, G.; SAPATNEKAR, S. S.; REIS, R., Electromigration inside logic cells: modeling, analyzing and mitigating signal electromigration in NanoCMOS, Springer, 2017.

PRADHAN, K.; SAHU, P. K., RANJAN, R., Investigation on asymmetric dual-k spacer (ads) trigate wavy finfet: A novel device. **IEEE International Conference on Devices, Circuits and Systems (ICDCS)**, p. 137–140, 2016.

PTM - Predictive Technological Model. Available in: <<http://ptm.asu.edu/>>, 2012. Access in: Jul. 2018.

RANJAN, A., Micro-Architectural Exploration for Low Power Design. Available in: <http://semiengineering.com/micro-architectural-exploration-for-low-power-design/>, 2015. Access in: Nov. 2017.

RAHMA-ABU, M.H., ANIS, M. A Statistical Design-Oriented Delay Variation Model Accounting for Within-Die Variations, **IEEE Transaction on CADICS**, v.27, p.1983-1995, Nov. 2008.

RAINEY, B. A. et al., Demonstration of FinFET CMOS circuits, **Digest Device Research Conference Proceedings...**, p. 47-48, 2002.

RAMAY, S. et al., Aging model challenges in deeply scaled tri-gate technologies, **IEEE International Integrated Reliability Workshop (IIRW)**, 2015.

RASOULI, S. H.; ENDO, K.; BANERJEE, K., Variability analysis of FinFET-based devices and circuits considering electrical confinement and width quantization, **IEEE/ACM International Conference on Computer-Aided Design - Digest of Technical Papers**, p. 505-512, 2009.

RATHORE, R. S.; SHARMA, R.; RANA, A. K., Impact of work function fluctuations on threshold voltage variability in nanoscale FinFETs, **IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, 2016.

RATHORE, R. S.; RANA, A. K.; SHARMA, R., Threshold voltage variability induced by statistical parameters fluctuations in nanoscale bulk and SOI FinFETs, **International Conference on Signal Processing, Computing and Control (ISPCC)**, 2017.

REIS, R.; CAO, Y.; WIRTH, G., **Circuit Design for Reliability**. Springer, 2015. 274 p., 2015, ISBN 978-1-4614-4077-2. DOI 10.1007/978-1-4614-4078-9

RIEGER, M. L., Communication theory in optical lithography, **Journal of Micro/ Nanolithography**, MEMS and MOEMS, 11(1), 2012.

ROCHE, P. et al., Technology Downscaling Worsening Radiation Effects in Bulk: SOI to the Rescue, **IEEE International Electron Devices Meeting**, 2013.

ROSA, L. S. et al., Switch level optimization of digital CMOS gate networks, **IEEE International Symposium on Quality Electronic Design (ISQED)**, 2009.

ROSTAMI, M; MOHANRAM, K., Dual- $V_{th}$  Independent-Gate FinFETs for Low Power Logic Circuits. **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, v.30, n.3, p.337-349, Mar. 2011.

ROY et al., Double-gate SOI devices for low-power and high-performance applications, **Proceedings Int. Conf. on Computer-Aided-Design**, p. 217-224, 2005.

SACHID, A. B.; HU, C., Denser and more stable SRAM using FinFETs with multiple fin heights, **IEEE Transactions on Electron Devices**, vol. 59, no. 8, p. 2037–2041, 2012.

SAHA, S.K., Modeling Process Variability in Scaled CMOS Technology, **IEEE Design and Test of Computers**, Vol.27, p.8–16, 2010.

SAHA, R.; BHOWNICK, B.; BAISHYA, S., Si and Ge step-FinFETs Work function variability, optimization and electrical parameters, **Superlattices and Microstructures Journal**, vol. 107, p. 5-16, 2017.

SAIRAM, T.; ZHAO, W.; CAO, Y., Optimizing FinFET technology for high-speed and low-power design, **Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI)**, p. 73-77, 2007.

SAMSUNG, Samsung Launches Premium Exynos 9 Series Processor Built on the World's First 10nm FinFET Process Technology. Available in: <https://news.samsung.com/global/samsung-launches->

premium-exynos-9-series-processor-built-on-the-worlds-first-10nm-finfet-process-technology, 2017. Access in: Aug. 2017.

SAYIL, S. Soft error mechanisms, modeling and mitigation. Springer, 2016.

SCHRIMPF, R. D. et al., Soft errors in advanced CMOS technologies, **IEEE International Conference on Solid-State and Integrated Circuit Technology**, 2012.

SEIFERT, N. et al., Soft Error Susceptibilities of 22 nm Tri-Gate Devices, **IEEE Transactions on Nuclear Science**, vol. 59, n. 6, 2012.

SEIFERT, N. et al., Soft error rate improvements in 14-nm technology featuring second-generation 3D tri-gate transistors, **IEEE Transactions on Nuclear Science**, vol. 62, no. 6, 2015.

SEKIGAWA, T.; HAYASHI, Y. Calculated threshold-voltage characteristics of an xmos transistor having an additional bottom gate. **Solid State Electronics**, v. 27, p. 827–828, sep. 1984.

SEXTON, F. W., Destructive single-event effects in semiconductor devices and ICs, **IEEE Transactions on Nuclear Science**, vol. 50, n. 3, p. 603-621, 2003.

SHERLEKAR, D., Design Considerations for Regular Fabrics, **International symposium on Physical design (ISPD)**, Proceedings... Phoenix, 2004. p. 97-102.

SHIVAKUMAR, P. et al., Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic. In: International Conference on Dependable Systems and Networks, 2002. IEEE, 2002, p. 389-398.

SICARD, E., Introducing 14-nm FinFET technology in Microwind, **Microwind Application Note**. Available in: <https://hal.archives-ouvertes.fr/hal-01541171/document>, 2017. Access in: Jun, 2018.

SILVA, D. N.; REIS, A. I.; RIBAS, R. P., CMOS logic gate performance variability related to transistor network arrangements, **Microelectronics Reliability**, vol. 49, pp. 977-981, 2009.

SIMOEN et al., Radiation Effects in Advanced Multiple Gate and Silicon-on-Insulator Transistors, **IEEE Transactions on Nuclear Science**, vol. 60, n. 3, 2013.

SIMSIR, M. O.; BHOJ, A; JHA, N. K., Fault Modeling for FinFET Circuits, **IEEE/ACM Symposium on Nanoscale Architecture**, 2010.

SINGH, N. et al., High-Performance fully depleted Silicon Nanowire Gate-All-Around CMOS devices, **IEEE Electron Device Letters**. 27 (5): 383–386, 2006.

SINHA, S. et al., Exploring sub-20nm FinFET design with predictive technology model, **ACM/EDAC/IEEE Design Automation Conference (DAC)**, 2012. p. 283-288.

SKOTNICKI, T. et al., The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance, **IEEE Circuits and Devices Magazine**, vol. 21, n. 1, p. 16-26, 2005.

SOLOMON, P. M. et al., Two gates are better than one, **IEEE Circuits and Devices Magazine**, vol. 19, n. 1, p. 48-62, 2003.

SOOTKANEUNG, W.; HOWIMANPORN, S.; CHOOKAEW, S., Thermal effect on performance, power, and BTI aging in FinFET-based design, **Euromicro Conference on Digital System Design (DSD)**, 2017.



SROUR, J. R.; PALKO, J. W., Displacement damage effects in irradiated semiconductor devices, **IEEE Transactions on Nuclear Science**, vol. 60, n. 3, p. 1740-1766, 2013.

SUBRAMANIANA, V. et al., Device and circuit-level analog performance trade-offs: a comparative study of planar bulk FETs versus FinFETs, **IEEE International Electron Devices Meeting (IEDM)**, 2005.

SWAHN, B.; HASSOUN, S., Gate Sizing: FinFETs vs 32nm bulk MOSFETs, **Design Automation Conference (DAC)**, pp. 528-531, 2006.

SWAHN, B.; HASSOUN, S.; ALAM, S.; BOTHA, D., VIDYARTHI, A., Thermal analysis of finfets and its application to gate sizing, **ACM/IEEE International Workshop on Timing Issues**, 2005.

SWINNEN, M.; DUNCAN, R., Physical Verification of FinFET and FD-SOI Devices. Available in: <http://www.techdesignforums.com/practice/technique/physical-verification-design-finfet-fd-soi/>, 2013. Access in: Apr, 2018.

TANG, S. et al., FinFET - a quasiplanar double-gate MOSFET, **Proceedings of International of Solid-State Circuits Conference**, p. 118-119, 2001.

TASSIS, D. H.; FASARAKIS, N.; DIMITRIADIS, A; GHIBAUDO, G., Variability analysis – prediction method for nanoscale triple gate FinFETs, **International Semiconductor Conference Dresden - Grenoble (ISCDG)**, 2014.

THAKKER, R.A.; SATHE, C.; BAGHINI, M.S.; PATIL, M.B. A Table-Based Approach to Study the Impact of Process Variations on FinFET Circuit Performance. **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, vol.29, no.4, pp.627,631, 2010.

TOLEDO, S. P. et al., Pros and Cons of schmitt trigger inverters to mitigate PVT variability on full adders, **IEEE International Symposium on Circuits and Systems (ISCAS)**, 2018.

TOMIDA et al., Impact of fin shape variability on device performance towards 10nm node, **IEEE International Conference on IC Design & Technology (ICICDT)**, 2015.

TOURÉ, G. et al., Simulation of Single and Multi-Node Collection: Impact on SEU Occurrence in Nanometric SRAM cells, **IEEE Transaction on Nuclear Science**, vol. 58, no.3, pp. 862-869, 2011.

TRIVEDI, V. P.; FOSSUM, J. G.; ZHANG, W., Threshold voltage and bulk inversion effects in nonclassical CMOS devices with undoped ultra thin devices, **Solid State Electronic**, p. 170-178, 2007.

UEMURA, T. et al., Investigation of Logic Circuit Soft Error Rate (SER) in 14nm FinFET Technology, **IEEE International Reliability Physics Symposium (IRPS)**, 2016.

UEMURA, T. et al., Investigation of logic soft error and scaling effect in 10nm FinFET technology, **IEEE International Reliability Physics Symposium (IRPS)**, 2017.

VELAZCO, R.; FOUILLAT, P.; REIS, R. (eds.), **Radiation Effects on Embedded Systems**. Springer, 2007.

WANG, X.; BROWN, A. R.; CHENGL, B.; ASENOV, A., Statistical Variability and Reliability in Nanoscale FinFETs, **International Electron Devices Meeting**, 2011.

WANG, Y.; COTOFANA, S. D.; LIANG, F., Statistical reliability analysis of NBTI impact on FinFET SRAMs and mitigation technique using independent-gate devices, **IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)**, p. 109–115, 2012.

WANG, X et al., Unified compact modeling strategies for process and statistical variability in 14-nm node DG FinFETs, **International Conference on Simulation of Semiconductor Processes and Devices**. 2013.

WEI et al., Bulk FinFETs with body spacers for improving fin height variation, **Solid-State Electronics Journal**, vol. 122, p. 45-51, 2016.

WEIMIN, Z.; FOSSUM, J.G.; MATHEW, L.; YANG, D., Physical insights regarding design and performance of independent-gate FinFETs, **IEEE Transactions on Electron Devices**, vol. 52, no. 10, p. 2198–2205, 2005.

WILSON, D. et al., Flexfet: Independently-Double-Gated SOI Transistor With Variable  $V_t$  and 0.5V Operation Achieving Near Ideal Subthreshold Slope, **IEEE International SOI Conference**, 2007.

WIMER, S., Planar CMOS to multi-gate layout conversion for maximal fin utilization, **Integration, the VLSI Journal**, vol. 47, p. 115-122, Elsevier, 2012.

WROBEL, F. et al. Determining realistic parameters for the double exponential law that models transient current pulses. **IEEE Transactions on Nuclear Science**, v. 61, n. 4, p. 1813–1818, Aug 2014.

YANG, F.-L. et al., 25 nm CMOS Omega FETs, **Digest. International Electron Devices Meeting**, (2002): 255-258.

YU, B. et al., FinFET scaling to 10nm gate length, **Proceedings of IEEE International Devices Meeting**, p. 251-254, 2002.

ZAREI, M. Y., et al. Modeling symmetrical independent gate FinFET using predictive technology model. **ACM international conference on Great lakes symposium on VLSI (GLSVLSI)**, p. 299-304, 2013.

ZHANG, B., PAN, D., FinFET standard cell optimization for performance and manufacturability, 2012. Dissertation - Faculty of the Graduate School of the University of Texas at Austin.

ZHANG, E. X. et al., Total Ionizing Dose Effects on Strained Ge pMOS FinFETs on Bulk Si, **IEEE Transactions Electronic Devices**, v.64, p. 226-232, 2017a.

ZHANG, H. et al. Temperature dependence of soft-error rates for FF designs in 20-nm bulk planar and 16-nm bulk finfet technologies, **IEEE International Reliability Physics Symposium (IRPS)**, [S.l.], p. 5C–3, 2016.

ZHANG, H. et al., Angular Effects of Heavy-Ion Strikes on Single-Event Upset Response of Flip-Flop Designs in 16nm Bulk FinFET Technology, **IEEE Transactions on Nuclear Science**, vol. 64, n. 1, 2017b.

ZHANG, H. et al., Effects of Threshold Voltage Variations on Single-Event Upset Response of Sequential Circuits at Advanced Technology Nodes, **IEEE Transaction on Nuclear Science**, vol. 64, n. 1, 2017c.

ZHANG, H. et al., Effects of Total Ionizing Dose Irradiation on Single-Event Response for Flip-Flop Designs at a 14-/16-nm bulk FinFET Technology Node, **IEEE Transactions on Nuclear Science**, vol. 65, n. 8, p. 1928-1934, 2018.

ZHAO, W., CAO, Y., New Generation of Predictive Technology Model for Sub-45nm Early Design Exploration. **IEEE Transactions Electronic Devices**, v.53, p. 2816–2823, Nov. 2006.

ZIMPECK, A. L; MEINHARDT, C.; REIS, R., Evaluating the Impact of Environment and Physical Variability on the  $I_{ON}$  current of 20nm FinFET Devices, **International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)**, p. 1-8, 2014.

ZIMPECK, A. L; MEINHARDT, C.; REIS, R., Impact of PVT Variability on 20nm FinFET Standard Cells, **Microelectronics Reliability**, v. 55, n. 9-10, 2015a.

ZIMPECK, A. L; MEINHARDT, C.; POSSER, G.; REIS, R., Process Variability in FinFET Standard Cells with Different Transistor Sizing Techniques, **IEEE International Conference on Electronics Circuits and Systems (ICECS)**, 2015b.

ZIMPECK, A. L; MEINHARDT, C.; POSSER, G.; REIS, R., FinFET Cells with Different Transistor Sizing Techniques against PVT variations, **IEEE International Symposium on Circuits and Systems (ISCAS)**, 2016a.

ZIMPECK, A. L; AGUIAR, Y. Q.; MEINHARDT, C.; REIS, R., Geometric variability impact on 7nm trigate combinational cells, **IEEE International Conference on Electronics Circuits and Systems (ICECS)**, 2016b.

ZIMPECK, A. L; AGUIAR, Y. Q.; MEINHARDT, C.; REIS, R., Robustness of sub-22nm multigate devices against physical variability, **IEEE International Symposium on Circuits and Systems (ISCAS)**, 2017.

ZIMPECK, A. L. et al., Impact of different transistor arrangements on gate variability, **Microelectronics Reliability**, vol. 88-90, pp. 111-115, 2018.

ZIMPECK, A. L. et al., Mitigation of process variability effects using decoupling cells, **Microelectronics Reliability**, 113446, ISSN 0026-2714, 2019a.

ZIMPECK, A. L. et al., Circuit-level hardening techniques to mitigate soft errors in FinFET logic gates, to be published in **European Conference on Radiation and its Effects on Components and Systems (RADECS)**, 2019b.

ZIMPECK, A. L. et al., Sleep transistors to improve the process variability and soft error susceptibility, to be published in **IEEE International Conference on Electronics Circuits and Systems (ICECS)**, 2019c.