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Deep electrical characterization and modeling of parasitic effects and degradation mechanisms of AlGa_N/Ga_N HEMTs on SiC substrate

Mehdi Rzin

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Par Mehdi RZIN

Deep electrical characterization and modeling of parasitic effects and degradation mechanisms of AlGaIn/GaN HEMTs on SiC substrates

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Introduction

The AlGaIn/GaN high electron mobility transistors (HEMTs) hold tremendous promise for radio-frequency (RF) power amplifier applications and for wireless base stations. This is due essentially to the interesting features of the AlGaIn/GaN heterostructure such as high density of the two dimensional electron gas (2-DEG), high breakdown electric field, high electron mobility and good thermal conductivity in addition to the high thermal conductivity of SiC substrate.

The optimization of the performances of AlGaIn/GaN HEMTs has been challenging for designers over the last decade. Many materials have been tested and studied for passivation with different deposition techniques to reduce the leakage current and increase the output power and the transconductance. The optimization of the topology and geometry of field-plates in the structure has been used to reduce the high vertical field in the vicinity of the gate. The thickness, doping and alloy composition of Al_xGa_{1-x}N layer are also crucial parameters in design and optimization of GaN based HEMTs.

The fabrication processes of GaN based HEMTs technologies are generally well controlled but there are still some issues that are hampering the power performances and the electrical reliability like the leakage current that might increase during operation. A deep characterization and understanding of the parasitic effects and the degradation mechanisms that are limiting the performances of these devices are needed.

The studied AlGaIn/GaN HEMTs are provided by the society United Monolithic Semiconductor (UMS) from the GH50 and GH25 that were qualified during this thesis. Many devices from these two GaN processes were submitted to high temperature accelerated life tests by UMS and characterized electrically at IMS laboratory to study the parasitic effects and degradations mechanisms.

This work has taken place at the Integration of Materials to Systems (IMS) laboratory, University of Bordeaux, in the framework of two projects:

- ReAGaN (Reliability Analysis of GaN technologies - Development of an innovative methodology for physical and electrical analysis at the device scale) funded by the ANR (Agence Nationale de Recherche),
- Extreme GaN – GaN technology pushed to extreme conditions for missile application funded by THALES Optronique (TOSA).

This thesis is divided into three chapters and is organized as follows:

The first chapter gives an overview of the basics of GaN based high electron mobility transistors (HEMTs). Gallium Nitride material features are reviewed as well as substrates suited for GaN based devices. GaN market in Europe and the main industrial actors are listed. Furthermore, the structure and operation of GaN based HEMTs are described. In the last part, the two UMS GaN processes are described.

The second chapter presents the life tests that are used for reliability studies. State of the art of parasitic effects and degradation mechanisms of AlGaIn/GaN HEMTs is given.

Furthermore, the ReAGaN project in which the main part of this thesis is involved is described. The electrical characterization techniques used at IMS during this thesis are presented.

The third chapter is divided to four case studies; three case studies are in the framework of ReAGaN project and the fourth one in the Extreme GaN project. In the first case study, we investigate the conduction mechanisms inducing the leakage current in AlGaIn/GaN HEMTs issued from GH50 process. The second case study is dedicated to the study of an electrical parasitic effect that appears on the Schottky diode forward characteristic after temperature accelerated life tests. In the third case study, we study the influence of Al mole fraction on the DC electrical parameters of AlGaIn/GaN HEMTs with strained AlGaIn layer. The last case study consists in the determination of the limits and safe operating area (SOA) of UMS GH25 GaN HEMTs by carrying out the two and three terminal breakdown voltages measurements.

Chapitre 1: Basics of AlGa_N/Ga_N HEMTs

In this chapter, we present the basics of high electron mobility transistors (HEMTs) based on AlGa_N/Ga_N heterostructure. First, an overview of the gallium nitride (Ga_N) material crystal structure and crystal polarities is given. Furthermore, an insight about Ga_N market by presenting the opportunities and outlook up to the next five years is reported. Ga_N epitaxy and development of substrates suited to Ga_N based devices are introduced. The main Ga_N industrial actors are listed and the European challenge to own an independent Ga_N technology and Ga_N supply chain in Europe is described.

In the second section of this chapter, we describe the AlGa_N/Ga_N HEMT structure by presenting the AlGa_N/Ga_N heterostructure, the formation of 2-DEG and different improvements in the device design to reduce degradation mechanisms. In addition, the device operation is explained.

In the third section, the devices under test are shown, by introducing the two UMS Ga_N technological processes: GH50 and GH25. Finally, the circuit applications and performances of Ga_N based devices are summarized.

1.1 Gallium Nitride material

The need of radio frequency (RF) electronics market for high power, high frequency, high efficiency, high linearity and low-cost monolithic amplifiers for radar and wireless communication systems is driving the development of competitive semiconductor devices.

The basic element of RF systems is high-speed transistor that operates at high frequencies. The invention of the bipolar junction transistor (BJT) in 1947 allowed the development of the first transistor based on Germanium (Ge) operating around 1GHz in the late 1950s. Silicon (Si) and Gallium Arsenide (GaAs) showed later great interest for high-frequency applications and became the dominating materials for fabrication of transistors (HBT, IGBT, MESFET and HEMT) in RF electronics.

In the early 1990s, gallium nitride (GaN) was considered an excellent semiconductor material for microwave and power electronics applications thanks to its large bandgap, high electron mobility and high breakdown voltage. As a result, the benefits of these parameter values are high operating temperature, high maximum current and high breakdown strength. Figure 1 shows a comparison between GaN parameters and Si and GaAs ones and their advantages in RF and power supply circuits. It is obvious that GaN is a good competitor over the RF market dominating materials and would bring more advantages to new systems, provided that the reliability concerns are fixed.

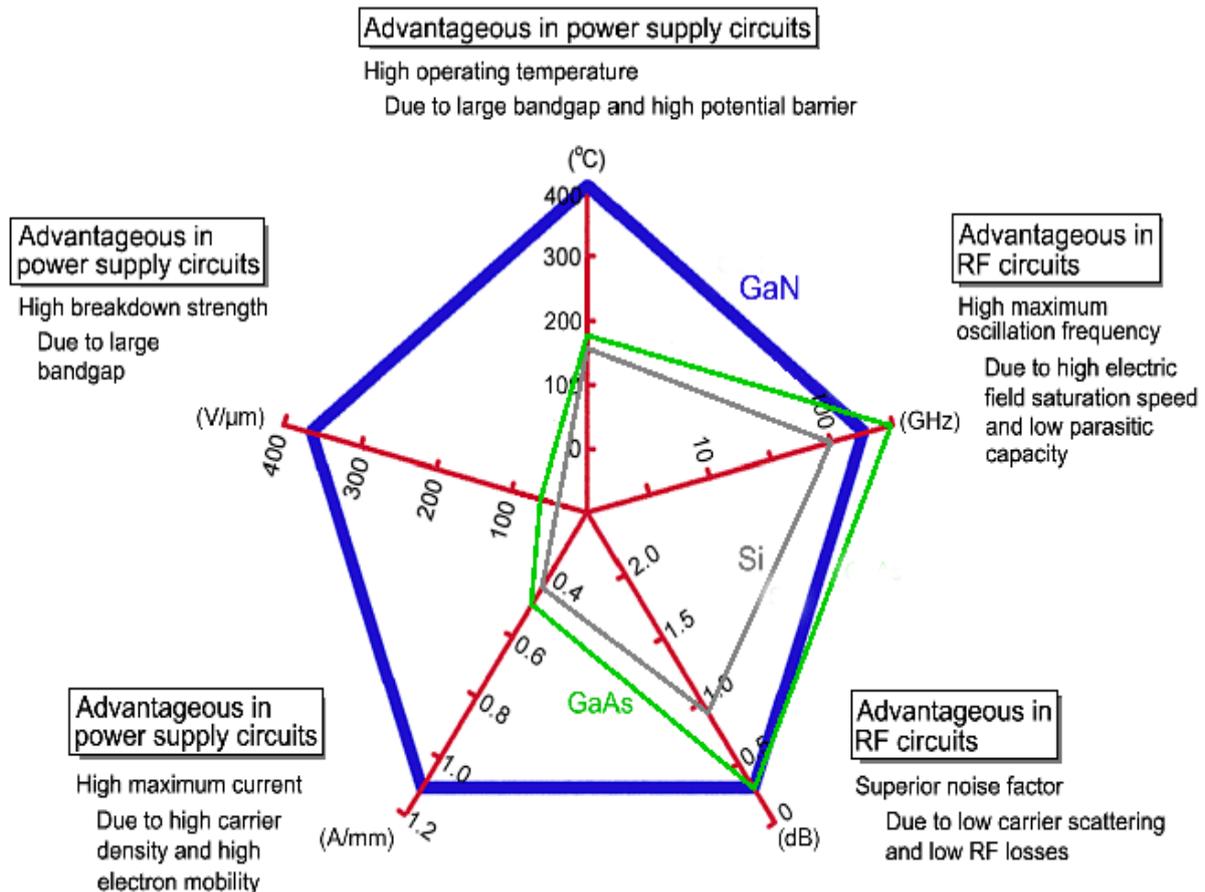


Figure 1. GaN material compared to Si and GaAs [GaNsystems]

1.1.1 Gallium Nitride Crystal structure

Group III nitrides and particularly GaN based semiconductors exist under three crystalline structures depending on the growth conditions: the wurtzite (Wz), zinc blende (Zb), and rock salt (RS) [Morkoc 2008].

At ambient pressure conditions, GaN usually tends to crystallize in the Wz structure, whereas Zb GaN is formed during film preparation process, while RS GaN only appears under ultrahigh pressures.

It is well established that Wz structure transforms to RS structure under high pressures [Perlin 1992] [Cui 2002] [Halsall 2004] [Xiao 2008] [Dong 2010]. It was reported that the competition between phonon and elastic instabilities plays an important role in the reconstructive phase transition from Wz to RS structure [Yao 2013]. The RS structure is typical of ionic bonds [Karas 2005] and presents less interest for device applications.

The zinc blende structure is the thermodynamically metastable polytype of GaN. It has a cubic unit cell, containing four Ga atoms and four N atoms. The Zb structure has several advantages for device applications, including easy cleavage, smaller band-gap and high carrier mobilities [Ploog 1997]. The Zb structure can be used for applications that need high cut-off frequency. This is due to the high electron drift mobility and lower effective mass compared to Wz structure [Arabshahi 2008].

The wurtzite structure has a hexagonal unit cell. It contains six atoms of Ga and six atoms of N. The Wz structure consists of two interpenetrating hexagonal close-packed sublattices. Hence it is defined by the edge length a of the basal hexagonal, the height c of the hexagonal prism, and an internal parameter u defined as the anion-cation bond length along $[0001]$ axis in units of c .

The wurtzite structure is more stable than Zb structure and most of GaN based transistors are grown on the Wz phase. Main focus will be on the Wz structure farther.

1.1.2 Wurtzite GaN crystal polarities

The Wurtzite GaN crystal is tetrahedrally coordinated semiconductor and lacks inversion plane symmetry along the c -axis.

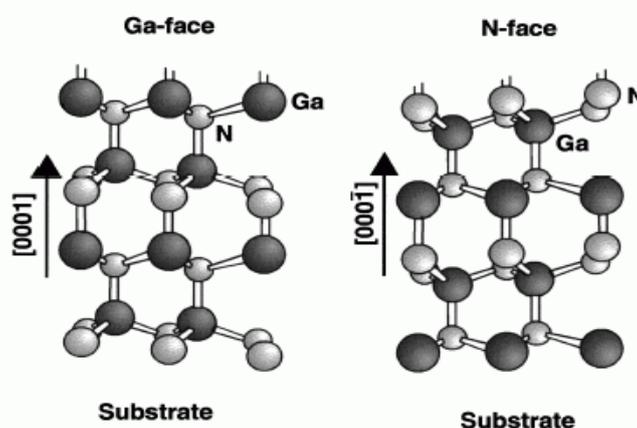


Figure 2. Wurtzite crystal GaN: Ga-face polarity (left) and N-face polarity (right)

The Ga and N atoms are arranged in bilayers. These bilayers consist of two closely spaced hexagonal layers, one formed by cations and the other one by anions, leading to polar faces. A basal surface could be either cation-face (Ga-face) or anion-face (N-face) corresponding to either Ga or N atoms on the top layer [Li 2000].

The polarity of GaN crystal depends on the position of the bonds along the [0001] axis that is by convention +z direction. The Ga-face polarity is when the bond points from the substrate to the surface while the N-face polarity is when the polarization points to the substrate (figure 2).

GaN wurtzite crystal structure and high degree of ionicity of the Ga-N covalent bonds result in significant polarization effects: spontaneous and piezoelectric polarization effects [Yu 1999]. Experimental and theoretical investigations revealed their great interest in the understanding of the physical properties of nitride heterostructures that will be discussed farther.

GaN Wurtzite crystal structure exhibits polarization at zero strain that is large in all nitrides [Bernardini 1997]. This polarization that occurs in the absence of an external electric field is called spontaneous polarization. The ionicity of the covalent bonds and the low symmetry in GaN Wz crystal generate the spontaneous polarization. Moreover, the non-ideality of the crystal lattice creates molecular dipoles in the material that build up the polarization field. The spontaneous polarization, P_{SP} , is defined as a vector pointing from Ga atom toward N atom. Therefore the direction of the spontaneous polarization depends on the face polarity of GaN material (Ga-face or N-face).

1.2 AlGaIn/GaN HEMT

The high electron mobility transistor (HEMT) is also called modulation doped field effect transistor (MODFET), two dimensional electron gas field effect transistor (TEGFET), and selectively doped heterojunction transistor (SDHT). Initially, the HEMT was based on AlGaAs/GaAs heterostructure and it was first reported by Mimura et al. at Fujitsu laboratories in Japan [Mimura 1980] and by Delagebeaudeuf et al. at Thomson-CSF laboratories in France [Delagebeaudeuf 1980], in 1980. The GaN material demonstrated more advantages over GaAs material, and the first report on the fabrication of AlGaIn/GaN HEMT was by Khan et al. in 1993 [Khan 1993].

1.2.1 HEMT structure

a- Basic structure

The AlGaIn/GaN HEMT structure is based on multiple epilayers grown on each other with different thicknesses and alloy compositions and three contacts connected to the active layer surface. Figure 3 shows the basic cross section of AlGaIn/GaN HEMT.

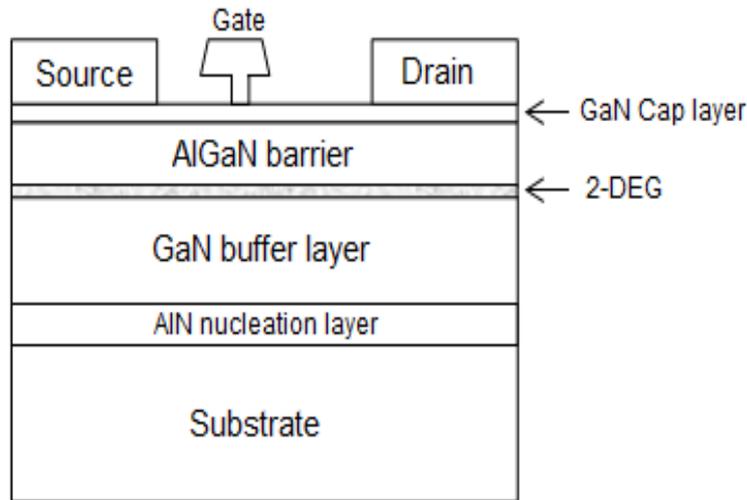


Figure 3. Basic AlGaN/GaN HEMT structure

The structure of AlGaN/GaN HEMT is as follows:

- Substrate: The growth of the structure is realized on semi-insulating substrate. The most used substrates for GaN based devices are SiC, Sapphire (Al_2O_3) or Si. The choice of the substrate depends on the application of the GaN based device, the allowed mismatch with GaN and the price as well as the wafer size. More details on the substrate are given farther.
- Nucleation layer: it is an intermediate buffer layer between GaN and the substrate. The use of AlN as nucleation layer may reduce the tensile strain of GaN due to the mismatch with the substrate that may lead to the formation of cracks.
- GaN buffer layer: This unintentionally doped or undoped layer is grown on the substrate directly or on the nucleation layer. The buffer is composed of the narrow-band-gap material that acts as active layer at which the 2-DEG heterointerface channel is formed. The material quality of this layer is very crucial especially because of traps and deep levels that degrade the device RF performances.
- AlGaN barrier: unintentionally doped layer is formed by the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ wide band-gap material, where x is the aluminum mole fraction. This layer forms the Schottky contact with the gate metal contact and supplies electrons for current conduction in the channel. The thickness and alloy composition of this layer are crucial to determine the mechanical stress and hence the piezoelectric polarization in the structure.
- GaN cap layer: It is an undoped or lightly doped thin GaN layer to protect the active layer, and to reduce the contact and channel resistance. Its purpose is also to limit the leakage current.

In addition, three contacts: gate, source and drain are deposited on the AlGaN layer. The drain and source are low-resistance ohmic contacts to minimize the access resistances. The gate contact forms with the AlGaN barrier a Schottky contact to modulate the carrier transport in the channel.

The basic structure showed above is not sufficient to limit some degradation mechanisms or dispersion of RF performances. Thus, some modifications might be applied like adding a field-plate structure or depositing a passivation layer.

b- Field plate (FP)

The role of a FP is to modify the electric field profile and to decrease its peak value on the drain side of the gate edge, hence reducing high-field trapping effects and increasing breakdown voltage.

GaN based HEMT demonstrated promising performances for high power and high frequency applications. However, until not long ago, there were some important issues that needed to be addressed. Current collapse phenomenon has been one of the most important concerns as it limits the output power, hence RF performances compared to what is expected from DC characterization. Generally, the presence of defects or traps at AlGaIn barrier surface on the drain side of the gate [Vetury 2001], AlGaIn/GaN heterointerface [Osvald 2010], and GaN bulk or substrate [Jogai 2003] [Horio 2005] are known to cause this phenomenon. Significant RF performance improvements are obtained by using field plate (FP) technique. The increased trapping effects limiting device RF performances can undermines its reliability [Jungwoo 2011]. The achievement of power densities more than 40W/mm [Wu 2006] and breakdown voltages more than 1000V [Xing 2004] is due essentially to the introduction of the FP to the device structure. Both gate connected FP (GFP) and source connected FP (SFP) allowed the dynamic performance improvement by suppressing the peak electric field and reshaping the electric field distribution in the channel [Boutros 2009] [Saito 2007]. However, the GFP configuration adds gate-to-drain capacitance (C_{gd}) that causes the reduction in current gain and power gain cut-off frequencies [Wu 2005]. With the SFP, the drawback of the added C_{gd} by the FP is eliminated.

c- Passivation

The introduction of dielectric thin films as passivation layers revealed improvements of RF power and breakdown voltage by reducing surface states. Many passivant materials have been investigated with different deposition techniques. In the early 2000s, the addition of Si_3N_4 [Green 2000] or SiN [Tilak 2000] passivation layers to undoped AlGaIn/GaN HEMTs resulted in the increase of the saturated output power by more than 75% and the breakdown voltage by 25% compared to values before passivation. Increase of carrier density in the channel (2-DEG) and the transconductance after passivation were also reported [Shealy 2003] [Wang 2006]. SiN passivation by using catalytic or plasma-enhanced chemical vapor deposition (cat-CVD or PECVD) showed that cat-CVD SiN passivation is more effective in increasing the 2-DEG density and reducing the AlGaIn potential barrier height [Onojima 2007]. Moreover, Si_3N_4 passivation by using low pressure chemical vapor deposition (LPCVD) was demonstrated to reduce drastically the surface depletion of 2-DEG by compensating the negative surface polarization charge with fixed positive charge in the silicon nitride [Shealy 2003]. In addition to the passivant material and the deposition techniques, the permittivity and the thickness of the insulator are crucial parameters to improve the breakdown voltage. The off-state breakdown voltage has been shown to increase

by increasing the permittivity (ϵ_r) or the thickness (d) of the passivation layer, thus AlGaIn/GaN HEMTs with high-k and thick passivation layer will have high breakdown voltage [Hanawa 2014]. Recent researches are ongoing to improve and optimize PECVD silicon nitride passivation to improve 2-DEG density and electric field [Gatabi 2013]. However, the change of transport properties of the 2-DEG due to SiN_x passivation has been shown to vary with the stress in the SiN_x layer from tensile to compressive [Fehlberg 2011]. Thus, even with the same passivation layer and deposition technique, the deposition conditions must be considered to obtain the optimum performances of AlGaIn/GaN HEMTs.

1.2.2 Device operation

a- AlGaIn/GaN heterostructure

Generally, a heterostructure or heterojunction is a junction between two semiconductors with different energy band gap. The lattice matching between epi layers has been considered as the most crucial point in the growth of heterostructures. Therefore, the development of epitaxy growth techniques (MBE and MOCVD) in the late 1970s made heterostructures, quantum wells and superlattices more accessible [Zse 2007]. The growth of heterostructures with important crystal mismatch causes dislocations at the interface, and degrades the performances of the device based on the heterostructure. Thus, the focus was more on the growth of crystals with the same lattice constant or small lattice mismatch. First, the mobility enhancement behavior in the AlGaAs/GaAs modulation doped superlattice was demonstrated by Dingle et al. at Bell laboratories, Murray Hill, NJ [Dingle 1978] and revealed the existence of a two-dimensional electron gas (2-DEG). In this work, the carrier mobility in the 2-DEG was demonstrated much higher than in the GaAs bulk.

The main characteristic of the AlGaAs/GaAs HEMT is the heterostructure consisting of doped wide bandgap material (AlGaAs) and undoped narrow bandgap material (GaAs). The doping modulation induces mobility enhancement as the impurity scattering is reduced because the channel carriers are spatially separated from donor ions. Initially, the Fermi level of the AlGaIn and GaIn materials do not coincide as shown in figure 4.

The AlGaIn/GaN heterostructure at thermodynamic equilibrium must have constant Fermi level throughout the structure according to the Anderson rules. The difference of the two materials electron affinities and the continuity of the vacuum level have as consequence that conduction and valence bands show discontinuities at the interface between the two materials.

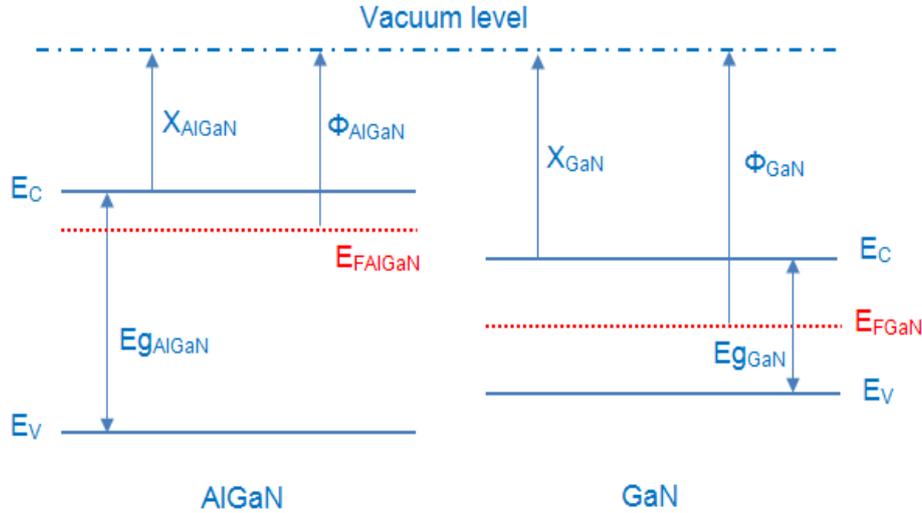


Figure 4. Energy band diagram of AlGaIn and GaN materials

A band-bending appears at the AlGaIn/GaN heterostructure as shown in figure 5 that is strongly affected by the mechanical strain.

The mechanical strain in the heterostructure depends on the thickness of $Al_xGa_{1-x}N$ layer and the Al mole fraction.

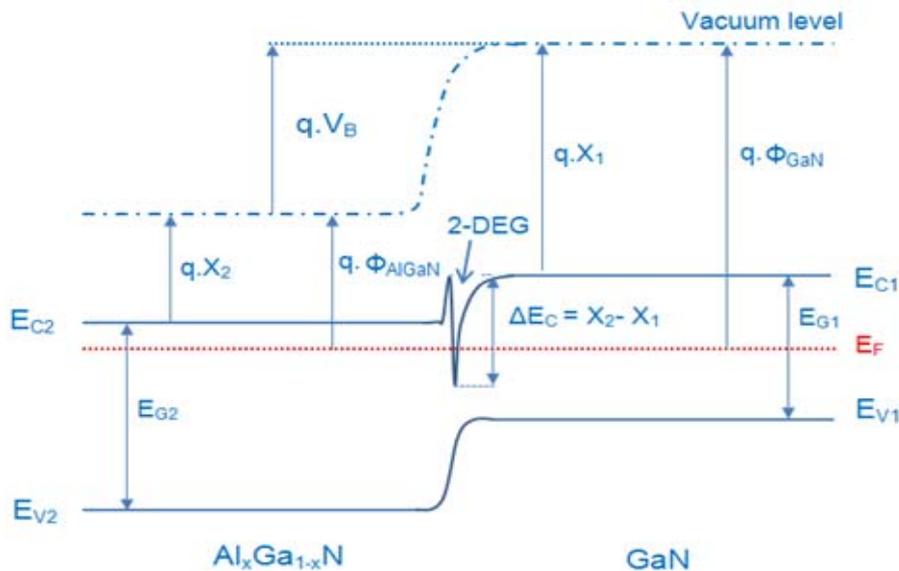


Figure 5. Energy band diagram of AlGaIn/GaN heterostructure

b- 2-DEG formation due to polarizations

In the AlGaIn/GaN heterostructure, the 2-DEG is induced by the piezoelectric charge effect without doping. Thus, the “piezoelectric doping” technique avoids the defects due to the introduced dopants [Shur 1999].

The polarization of GaN crystal is able to change under external stress or strain along the c axis due to the non-ideality of the equilibrium lattice parameters (a_0 and c_0). These

parameters will change to accommodate the stress. The generation of an electric polarization field in a crystal, which is under strain is called piezoelectric polarization (P_{PE}).

At a microscopic level, a strain parallel or perpendicular to the c axis induces an internal displacement of the metal sublattice with respect to the nitrogen ones. Hence, it is causing a variation of the parameter u (the anion-cation bond length along the (0001) axis) of the Wz structure [Ambacher 2000]. The piezoelectric polarization is due to the change of the lattice constants.

The piezoelectric polarization P_{PE} can be expressed via the piezoelectric constants e_{33} and e_{13} as [Li 2000] [Ambacher 2000]:

$$P_{PE} = e_{33}\varepsilon_z + e_{13}(\varepsilon_x + \varepsilon_y) \quad (1.1)$$

Where $\varepsilon_z = (c - c_0)/c_0$ is the strain along the c axis and the in-plane strains $\varepsilon_x = \varepsilon_y = (a - a_0)/a_0$ are assumed to be isotropic, e_{33} , e_{13} are the piezoelectric coefficients, and a and c are the lattice constants of the strained layer.

The different strains in the lattice are given by:

$$\varepsilon_z = -2 \cdot \frac{C_{13}}{C_{33}} \cdot \varepsilon_x \quad (1.2)$$

Where C_{13} and C_{33} are elastic constants. Eq1 and Eq2 can be combined to obtain the following equation:

$$P_{PE} = 2 \cdot \frac{a-a_0}{a_0} \cdot \left[e_{13} - e_{33} \frac{C_{13}}{C_{33}} \right] \quad (1.3)$$

Since $(e_{13} - e_{33} \frac{C_{13}}{C_{33}})$ is assumed to be always negative in the III-nitrides wurtzite structures, the direction of the piezoelectric polarization depends on the sign of $(a - a_0)$. P_{PE} is always negative for layers under tensile stress ($a > a_0$) and positive for layers under compressive stress ($a < a_0$). As spontaneous polarization in III-nitrides is always negative, spontaneous and piezoelectric polarizations are parallel to each other for layers under tensile stress, and are anti-parallel for layers under compressive stress.

The piezoelectric polarization for GaN is known to be zero as the bulk is strain-free. The AlGaN is a polar and piezoelectric material and for Ga-face it is used under tensile strain. Hence, the P_{SP} and P_{PE} polarizations have the same sign as shown in figure 6.

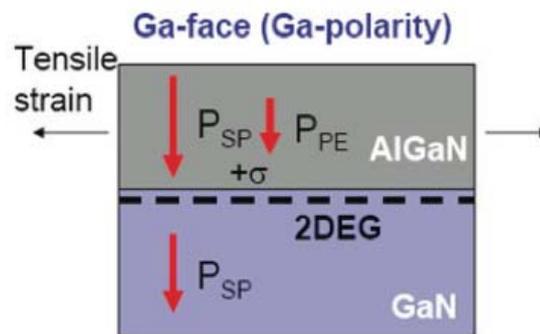


Figure 6. P_{SP} and P_{PE} Polarizations of Ga-face AlGaN/GaN heterostructure

The AlGaIn/GaN interface polarization is given as follows:

$$P_{AlGaIn/GaN} = P_{SP(AlGaIn)} + P_{PE(AlGaIn)} + P_{SP(GaN)} \quad (1.4)$$

The electrons transfer from AlGaIn into GaN and get confined in the emerged triangular quantum well. The charge density is called two dimensional electron gas (2-DEG) due to the two-dimensional distribution of electrons in the channel.

Under the complete charge depletion, the 2-DEG carrier density is governed by the following equation [Rashmi 2002]:

$$n_s = \frac{\epsilon(x)}{qd} (V_{GS} - V_{TH} - E_F) \quad (1.5)$$

Where x is the Al mole fraction in the AlGaIn barrier, $\epsilon(x)$ is the dielectric constant of AlGaIn, d is the AlGaIn thickness, V_{GS} is the applied gate bias and V_{TH} is the threshold voltage.

c- 2-DEG modulation control by the gate bias

The AlGaIn/GaN HEMT is based on 2-DEG induced by the piezoelectric field created by piezoelectric polarization. The application of a voltage between the source and the drain contacts induce an electric field that increases the current flow in the channel. The Schottky gate contact modulates this current flow by the electric field induced by the gate bias. Most of GaN based HEMTs are normally-on, which means that at $V_{GS} = 0V$, the channel is not depleted and the current can flow in the channel. In order to operate in off-state, the gate bias should be below the threshold voltage $V_{TH} < 0V$ that is the value of V_{GS} at which the 2-DEG channel is open. Figure 7 shows the energy band diagram under the Schottky gate contact.

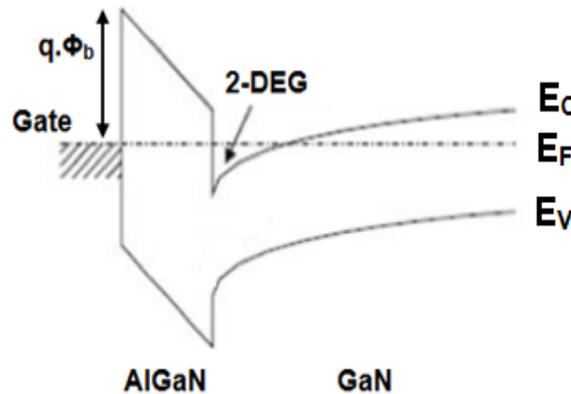


Figure 7. Energy band diagram under the gate at $V_{GS} = 0V$

1.2.3 Schottky contacts

The gate contact of the AlGaIn/GaN HEMT is a Schottky contact formed by a junction between a metal stack and AlGaIn layer. The most important parameter in the Schottky contact is the barrier height ($q\Phi_B$) that is a potential energy barrier. The Schottky barrier height $q\Phi_B$ is defined as the difference between the interfacial conduction band energy E_C and the Fermi level E_F . Low leakage current and low resistivity are required for the gate contact.

Several schemes of metals with high metal work functions including Titanium (Ti) ($\Phi_m = 4.33$ eV), Platinum (Pt) ($\Phi_m = 5.65$ eV), gold (Au) ($\Phi_m = 5.1$ eV) and Nickel (Ni) ($\Phi_m = 5.15$ eV) are used for GaN based HEMTs.

The Schottky contact multilayers on GaN formed by Ni/Au, Pt/Au, and Mo/Au are fairly thermally stable and no “gate-sinking” has been reported [Meneghesso 2008]. However, the barrier height has been reported to increase after thermal treatments or accelerated life test [Zhao 2010].

The introduction of Pt in Ni/Au multilayer (Ni/Pt/Au) has been reported to improve the characteristics of the Schottky contact after short-term annealing but causes important degradation after annealing at 500°C for 8 hours due to the diffusion of Ni into the Pt layer which results in the lowering of the Schottky barrier height [Ofuonye 2014].

1.2.4 Ohmic contacts

High quality ohmic contacts are required for AlGaIn/GaN HEMTs. Generally, it is assumed that the sheet resistance (R_{SH}) of the layer under the ohmic contacts is the same as between the contacts. As R_{SH} of GaN based HEMTs is low, increasing the ohmic contact resistance would degrade the performances of the device as the extrinsic gain and limit the current density in the 2-DEG. The source and drain access resistances must be reduced in order to improve the frequency performances of GaN based HEMT [Nidhi 2006].

The most common ohmic contacts used for AlGaIn/GaN HEMTs are based on metal stack of Titanium (Ti) and Aluminium (Al) used as the base of the multilayer. To obtain ohmic behavior of this multilayer, a rapid thermal annealing (RTA) in the temperature range of 800 – 900°C is applied [Fay 2008]. Other metals are added to Ti/Al metal stack as Molybden (Mo), Gold (Au), Nickel (Ni) or Platinum (Pt) to form different metal schemes : Ti/Al/Mo/Au [Selvanathan 2002] [Wang 2007], Ti/Al/Ni/Au [Crespo 2003] [Iucolano 2013], Ti/Al/Ti/Au [Wang 2001], Au/Pt/Al/Ti [Fay 2008].

The transition from rectifying to ohmic contact is attributed to diffusion of Ti or Au into AlGaIn layer after RTA that can cause n-type doping or the formation of an interfacial TiN layer. It induces Nitrogen (N) depletion in the AlGaIn layer that could be considered as n-type doping [Bright 2001].

1.3 Devices under test – UMS technology

UMS has developed two GaN based processes (GH50 and GH25) to provide foundry and services to European defense and space industries that need GaN technology to develop and improve their products. These two processes are based on AlGaIn/GaN heterostructure on SiC substrate. There are crucial differences of epitaxial layers, geometry, and gate length between the two processes.

1.3.1 GH50

The GH50 process is dedicated to manufacture power discrete transistors up to C band and was fully qualified in 2012. This process is intended for high power commercial and defense applications like base stations and ground radars [Lambert2012].

The GH50 process with a $0.5\mu\text{m}$ Au based gate metal is based on epitaxy of GaN and AlGaN layers by MOCVD on $100\mu\text{m}$ thick semi insulating (SI) SiC substrate, to form the active region of diodes and transistors. The wafer diameter is 3" while 4" wafers are intended for the next generation. A metal stack is deposited by evaporation after a deposition and etching of a photo resist and then structured by thermal annealing to form source and drain contacts. A SiN passivation layer is deposited on the whole wafer to passivate the AlGaN barrier layer and to protect it during the next fabrication process steps. Inter device insulation (transistors, diodes and GaN resistor) is made by Argon implantation. A gate trench in the passivation is defined by electron beam lithography and opened by reactive ion etching. Windows opening in the first SiN passivation are patterned. The structure of the Schottky gate is defined by optical lithography and the gate metallization is deposited by evaporation. A second passivation layer is deposited to protect the gate. A metal interconnection windows opening in both passivation layers is patterned by optical lithography and opened by reactive ion etching. To improve the interconnections robustness and to form the field plate (FP) a metal stack is formed on top of the contacts. A photo resist is deposited to realize contact between the FP metal and the air bridge two ends. SiN passivation is deposited on the whole wafer to protect the surface and the air bridges. The front of the wafer is protected and fixed on glass substrate then the back is thinned until $100\mu\text{m}$. The back of SiC substrate is covered with Al layer where the via-hole connections are defined by contact lithography, and then a metal stack is sprayed on the SiC substrate. A deposit of gold is added to reinforce the back metallization. At the end, the wafer is detached from the glass substrate and washed. The final AlGaN/GaN HEMT structure is shown in figure 8.

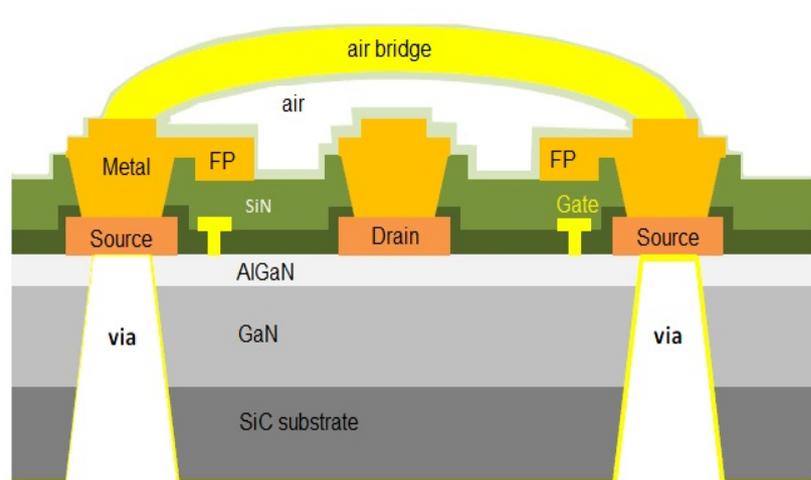


Figure 8. Schematic of UMS AlGaN/GaN HEMT structure [Brunel 2014]

1.3.2 GH25

The GH25 technology is based on an AlGaN/GaN epitaxy on SiC substrate with a 0.25 μ m Au based gate metal. The AlGaN layer is around 20 nm thick and a moderate Al content is used in order to contribute to the reduction of the reverse gate leakage current.

This technology intends to cover high power and wide band frequency range applications up to Ku band for telecom and defense markets. Studied AlGaN/GaN HEMTs present 8x125 μ m- gate finger topology, standard ohmic contacts, a silicon nitride passivation and a source terminated field plate.

1.4 GaN for power and RF applications

1.4.1 GaN market: opportunities and outlook

The gallium nitride (GaN) semiconductor market was valued at US \$380 million in 2012 according to [Transparency market research]. It is forecasted to reach \$ 2.2 billion by 2019, growing at a compound annual growth rate (CAGR) of 24.6 percent from 2013 to 2019. Apart from power semiconductor, GaN is predominantly used in optosemiconductor, for LEDs and laser diodes. In 2012, optosemiconductor was the major product type and accounted for 96.6 percent of the global GaN semiconductors in military, aerospace, defense and consumer electronics sectors.

Among the different applications, the military defense and aerospace sectors held the highest market share and were valued at \$82 million in 2012. With the markets for pulsed RF power semiconductor devices set to top \$250million by 2018, the future for GaN in defense electronics applications looks very healthy [Abi Research]. Consumer electronics was the second largest application segment followed by information and communication technology (ICT) and automotive sectors.

The introduction of 4G wireless system including Long Term Evolution (LTE) to meet the increasing requirements of high data rate and high efficiency will raise the demand for high power transistors and base stations. The GaN RF power transistor, due to its high efficiency and high power density, is the best candidate for supporting the next-generation RF power device applications. Hence, the demand for GaN power semiconductors in ICT is expected to grow faster.

The GaN based devices were used primarily for low frequency L, S and C-band applications but the raising demand for high frequency, with high output power and high efficiency have been a great challenge for design engineers to develop power amplifiers in X and Ku band applications such as radars [Damian 2012].

X-band radars systems – such as the US Sea Based X-band Radar, which is claimed to be the world’s largest phased array X-band radar carried aboard a mobile, ocean-going semi-submersible oil platform – are increasingly using GaN RF devices [CS-Jan2014].

Growing application areas as well as increased demand from military is the major driving force for the growth of GaN semiconductor devices market.

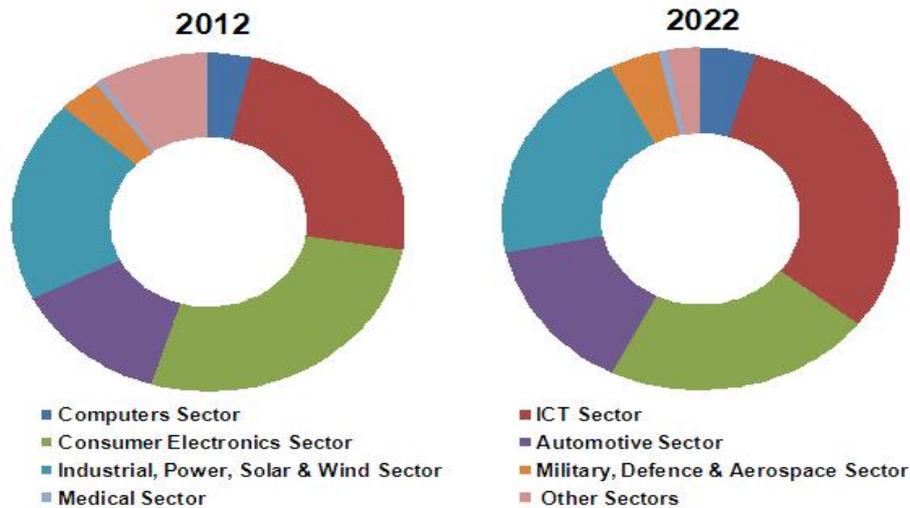


Figure 9. GaN semiconductor market revenue shares by application sector (2012 – 2022)
[Markets and Markets]

1.4.2 GaN epitaxy and substrates

During the past decade, rapid progress has been made in the US and Japan in the research and development toward qualification and commercialization of GaN based devices [Blanck 2009]. Until 2008, the only available GaN foundries were based in the US. The US monopoly over the industrial GaN supply chain options made it difficult for European defense industries to have independent technology or to be competitive in some strategic areas. Therefore, many projects (KORRIGAN [Gauthier 2006], GREAT² [Barnes 2012], EuSIC [Waltereit 2013], MANGA [Mikulla 2011]...) were initiated by European institutions to support and accelerate the development of GaN technology in Europe. This is by covering substrates fabrication and epitaxy development to process foundry and a focus on the reliability improvement through advanced failure analysis. The support was not only financial but also with the contribution of ministries of defense (MoD) of the European countries involved in the projects to ensure the success and keep an overall view on the European roadmap.

In the RF industrial GaN supply chain, the first activity to focus in is the substrate and particularly SiC substrates. More details about the choice of SiC will be given farther. The major SiC substrates manufacturers in the world are: Cree and II-VI in the US, Tankeblue and Nippon in Asia as well as SiCrystal and Norstel in Europe. SiC substrates of these last two manufacturers are available in 2” and 3” diameter and are grown by using conventional Physical Vapor Transport (PVT) and High Temperature Chemical Vapor Deposition (HTCVD) [Mikulla 2011]. Recent works are focusing on Si substrates to reduce cost and increase wafer dimensions but reliability concerns are still under research.

Substrates

The crystal growth techniques such as Czochralski and Bridgman were applied to produce crystals large enough to manufacture large and low price wafers. However, GaN based devices manufacturers have to choose between a far-from perfect 2” GaN substrate that

is very pricey and some other alternatives for larger and foreign substrates that have the drawback of leading to inferior material quality and thus the performances are below the theoretically predicted ones. GaN substrate is mandatory for laser diodes makers, because they must work with very high quality material. However, LED and power electronics industries are adopting sapphire (Al_2O_3), silicon (Si) and silicon carbide (SiC) as GaN is considered too expensive. An average 6" Si wafer costs about \$12, a 2" sapphire substrate is available at only \$8 to 10\$, but 2" GaN substrate retails for \$2000 at least [CS2 January 2014]. The prices of commercially available 4" SiC substrates range from \$2153 to \$5382 [Oshita 2013]. The substrates indicated above have all a mismatch with GaN that leads to a large number of crystal defects and dislocations causing the degradation of device performances and lifetime.

In recent years, many researches were carried out to find out new materials that would be in good agreement with GaN relative to their lattices, thermal and electrical properties for GaN based devices epitaxy. In general, the mismatch parameter is the key criterion to select a substrate. However, the structure of the crystal material, treatment of a surface, composition, reactivity of the surface, as well as, chemical, thermodynamic and electric properties of the material used are very important for selecting materials for preparation of the substrate [Kukushkin 2008]. Table 1 resumes a wide range of applicants to substrates for GaN with their crystal structures and lattice constants.

Indeed, the substrate determines the crystal orientation and polarity (Ga or N-face polarity for AlGaIn/GaN transistors). In addition, the substrate thinning induces residual strain in the heterostructure that would increase the electron sheet density and the mobility up to a critical thickness beyond which relaxation occurs and induces cracks in the AlGaIn/GaN surface [Azize 2010].

Material	Structure	Lattice constants (nm)	
		a	c
W-GaN	Wurtzite	0.31885	0.5185
Zb-GaN	Zinc-Blende	0.4511	
RS-GaN	Rock-Salt	0.422	
W-AlN	Wurtzite	0.31106	0.49795
Zb-AlN	Zinc-Blende	0.438	
RS-AlN	Rock-Salt	0.404	
SiC	4H (W)	0.3073	1.0053
SiC	6H (W)	0.30806	1.51173
GaAs	Zinc-Blende	0.56533	
Si	Diamond	0.54310	

Table 1. Properties of some used substrates for GaN [Kukushkin 2008]

The most used substrate for the growth of GaN was sapphire. Its important lattice mismatch (~16%) with GaN results in high concentration of dislocations ($10^{10}/\text{cm}^2$) that leads to decrease in mobility of charge carriers. In addition, the poor thermal conductivity

coefficient ($0.25\text{W}\cdot\text{cm}^{-1}\cdot\text{K}^{-1}$) manifests in a poor dissipation of heat in the structure [Kukushkin 2008]. Furthermore, the dielectric characteristics of sapphire substrate added to the above cons makes it inadequate for high frequency applications.

SiC substrate is more interesting than sapphire for GaN growth. The low lattice mismatch with GaN ($\sim 3\%$), the high thermal conductivity ($3.8\text{W}\cdot\text{cm}^{-1}\cdot\text{K}^{-1}$), whereas doping SiC, hence increasing the electrical conductivity makes SiC an excellent choice for high RF power applications. This is in spite of the high price and some process complexity of etching off the material. There are two polar SiC substrates: C-polar and Si-polar substrates [Hellman 1998]. Nowadays, Si-polar SiC substrates are more preferable, as growing GaN films on them results in top-quality [Kukushkin 2008]. There are more than 250 polytypes of SiC substrates but only two polytypes, 4H and 6H, are commercially available substrates of high quality

Silicon is very attractive as substrate for GaN device makers due the low cost, high crystal quality and large wafer sizes. In addition, the possibility to combine GaN devices with Si microelectronics ones in the same wafer is attractive. However, the large lattice mismatch with GaN and moderate thermal conductivity makes it difficult for Si based devices to achieve the same RF performances as SiC based devices.

1.4.3 Circuit performances and applications

A large expertise and know-how about the epitaxy have been developed in the last decade at different research laboratories: III-V lab (France), IAF and FBH (Germany), and Linköping University (Sweden) and commercial companies like EpiGaN (Belgium) incorporated in 2010 as a spin-off of IMEC (Belgium) and a “pure-play” epitaxy supplier, as well as QinetiQ (England) that announced exit from all semiconductor activities in 2010. The main actors of GaN foundries in the world are led by (FUJITSU, NEC, and Matsushita Electric Industrial) in Japan, (TRIQUINT, RFMD, CREE, RAYTHEON, HRL, and NORTHROP GRUMMAN...) in the US and (UMS, SELEX SI) in Europe.

The necessity of a European industrial source for GaAs/GaN RF manufacturing gave rise to the creation of UMS by gathering THALES and EADS MMICs activities. This is to respond to defense and space stakeholders needs to improve European technology. Two GaN technologies have been qualified for power and MMIC applications. The European defense and space industries interested by GaN technology to improve and develop their products are: Thales (France), SAAB (Sweden), EADS (European), MBDA (European), ESA (European), TESAT (Germany) and Roke (UK).

The circuit designs are usually based on the performances and also cost of the used semiconductor material. GaN based HEMTs are considered to be the best candidates for achieving high performances in high power amplifiers (HPA) such as high linearity and wide bandwidth operation with low power consumption. C-band HPAs are used for most of weather radars in the 5.25 – 5.75 GHz frequency band and used by TV stations. The saturated output power per die area of a GaN HPA is a key criterion to make it economically more attractive. Florian et al. realized two C-band HPAs by using UMS $0.25\mu\text{m}$ GaN process: one with a maximum output power of 20W and an output power density of $1.2\text{W}/\text{mm}^2$ [Florian 2012] and an other one with a maximum output power of 40W and an output power density

of $1.8\text{W}/\text{mm}^2$ [Florian 2013]. Jeong et al. [Joeong 2014] realized a C-band HPA by using $0.25\ \mu\text{m}$ Cree GaN process with a maximum output power of 50W and an output power density of $3.2\ \text{W}/\text{mm}^2$. Van Wanum et al. [Van Wanum 2013] demonstrated a 50W C-band HPA with $3.6\ \text{W}/\text{mm}^2$ by using UMS GH25 GaN process. Most of these HPAs are used for space based synthetic aperture radars (SARs) that are used by satellite earth observation.

Most of space applications are using the vacuum tube based traveling wave tube amplifiers (TWTA) because of a high power added efficiency (PAE). However, the most critical issues of vacuum device power amplifiers are the high voltage power supply and the tube itself. The reliability of TWTA is considered a major concern as the lifetime is limited due to the hot electrons in the vacuum tube [Ishida 2011]. Recently, solid state power amplifier (SSPA) is developed to replace TWTA by taking advantage of the GaN based HEMT high output power, high frequency and low noise performances [Casto 2011]. L-band HPA are applicable for use in base station amplifiers suitable for the cellular phone network [Ishida 2011]. X-band MMIC GaN HEMT based amplifiers have been developed to operate for X-band radar applications like the SBX-1 sea based X-band radar [MDA], and as microwave rectifiers used in wireless power transmission [Litchfield 2014]. GaN SSPA at UHF bands have been demonstrated by Katz et al. [Katz 2013] for the transmission of wideband code division multiple access (WCDMA) used in government and communications satellites. Colangeli et al. [Colangeli 2013] presented broadband and narrowband low noise amplifiers (LNA) based on AlGaN/GaN HEMTs that operates in the frequency range 2-18 GHz.

1.4 Conclusions chapter 1

In the first part of this chapter, the GaN material crystal structure and polarities have been discussed. The attracting interest to GaN material for optoelectronic, high power and high frequency applications is due essentially to the interesting features of this III-V material : high breakdown voltage, high band gap and high electron mobility. The spontaneous and piezoelectric polarizations due to the high ionicity of GaN are of great interest for devices based on this material like HEMTs. An insight about the GaN semiconductor devices market and the opportunities offered by the growing demand especially for military applications has been discussed. Furthermore, the GaN supply chain in Europe has been resumed.

The AlGaIn/GaN HEMT based on AlGaIn/GaN heterostructure and the piezoelectric field induced by piezoelectric polarization enhances the carrier mobility in the 2-DEG. The basic structure of GaN based HEMT is based on different epi layers with different thicknesses and alloy compositions that each plays a great role in the performances of the device. However, adding a field plate structure or passivation to the basic HEMT structure is essential to reduce RF performances dispersion or degradation mechanisms related to trapping effects. The 2" pricey GaN substrates oblige LED and power transistors makers to choose larger and foreign substrates that leads to inferior material quality, due to the lattice mismatch with GaN material. The low ohmic contacts access resistance is required for GaN based HEMT to improve frequency performances, while the most used metals for Schottky contact must have high metal work function. Furthermore, the GaN based HEMT operation has been explained.

In the last section of this chapter, the devices under test based on two GaN processes of UMS have been described. In addition, the fabrication processes of UMS AlGaIn/GaN HEMT have been detailed. Many works have demonstrated the performances of GaN based HEMT for radars, satellites and wireless applications.

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Chapter 2: Degradation mechanisms and reliability of AlGa_N/Ga_N HEMTs

The tremendous promise of AlGa_N/Ga_N HEMTs for radio-frequency power amplifier applications and for wireless base station is due essentially to the interesting features of the AlGa_N/Ga_N heterostructure. The fabrication process of the Ga_N based HEMTs technology has been improved during the last decade and is generally well controlled but still there are some issues that are hampering the power performances and the electrical reliability that should be fixed to improve the performance and the efficiency of Ga_N HEMT devices.

In this chapter, we discuss the life tests that are widely used for the reliability evaluation of Ga_N based HEMTs. First, the reliability and the “bathtub” curve that describes the failure rate over time are defined. Moreover, some of the used accelerated life tests that allows the quantification and understanding of degradation or failure mechanisms that occur at normal use conditions are presented. In the last part of this section, three of the most used lifetime distributions (exponential, lognormal and Weibull) are resumed. Furthermore, the Arrhenius life stress model is illustrated and the equations that allow obtaining the activation energy of the failure mechanism are detailed.

In the second section of this chapter, we give a summary of the state of the art of parasitic effects and degradation mechanisms that are hampering the electrical performances and the reliability of AlGa_N/Ga_N HEMTs.

In the third section, the ReAGa_N project in which this thesis is involved is described. First the objectives of the project are presented, and then the methodology and the different techniques that have been used to achieve the expected results are resumed. In the last part of this section, two types of failure analysis for defect localization (non-destructive and destructive) are discussed.

In the last section of this chapter, the technical characterization procedure used at IMS laboratory for ReAGa_N project is illustrated and the electrical characterization techniques are detailed.

2.1 Life tests for reliability evaluation

Reliability is defined as the probability that a system performs an intended function under specified conditions for a stated period of time without failure or degradation. For GaN based HEMTs, the functionality of the devices in final circuits whether for space, telecom or military applications under which electrical, thermal, or environmental conditions is important for the reliability study. For example, study of radiation effects on AlGaIn/GaN HEMTs by X-rays, protons, neutrons (Single event Effects), and/or heavy ion irradiations is crucial for space applications in radiative environments [Ionascut-Nedelcescu 2002]. A sufficient number of samples should be considered to be confident about the results. The voltage, current and temperature values at which the study is performed can induce different failures or accelerate degradations localized in different areas of the device, hence reducing the lifetime.

The reliability of semiconductor devices is associated to the failure rate over time described by the known “bathtub” curve. This curve is divided into three regions: Early failures, useful life and wear-out as shown in figure 10.

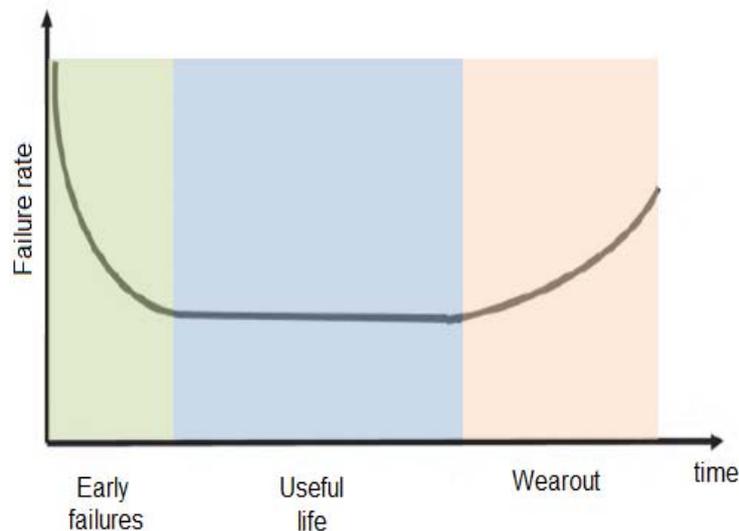


Figure 10. Failure rate with time

The failure rate is initially high due to early failures or infant mortality. This is caused by the defects that occur during the fabrication process such as contaminating particles that leads to premature device failure. The failure rate decreases to the lowest value and becomes constant during the useful life phase that corresponds to the working life of devices. Failures are induced by external conditions that are related to lighting or electrostatic discharging, hence they are unpredictable. Finally, the failure rate increases due to the wear out of the device related to intrinsic reasons [Marcon PhD thesis]. In order to reduce the failure rate and improve the reliability in the first region of the bathtub curve, burn-in might be applied to eliminate the external reasons causing defects. However, it is difficult to measure wearout directly, as the failure happens in time much longer than the useful life of the device. Thus

the method to forecast the device lifetime is based on accelerated life tests at a fixed current and/or voltage values under different temperatures.

Lifetime measurement includes Mean Time to Failure (MTTF) that is used to describe the expected time to failure for non-repairable devices once they fail. MTTF is defined by:

$$MTTF = \int_0^{\infty} tf(t)dt \quad (2.1)$$

Where $f(t)$ is the density function of time until failure

2.1.1 Accelerated life tests

In order to analyze the lifetime of a product or a semiconductor device particularly, time to failure data must be analyzed under optimal operating conditions. Nowadays, the maturity and advanced technological fabrication process make it difficult to obtain device lifetime data under normal operating conditions. The GaN HEMT industrial competition is rude and the time between the design definition and the final product release should be as small as possible. The accelerated life tests allow the quantification and understanding of degradation or failure mechanisms that occur at normal use conditions. The main purpose of accelerated life tests is to accelerate the failure modes and not to introduce failures to the studied structure; hence much attention must be given to the stress conditions.

There are physical defects that are activated under various DC or RF conditions, electric field, environmental, and mechanical stresses and most of GaN HEMT degradations and wear-out mechanisms can be accelerated by thermal (high temperature) stresses.

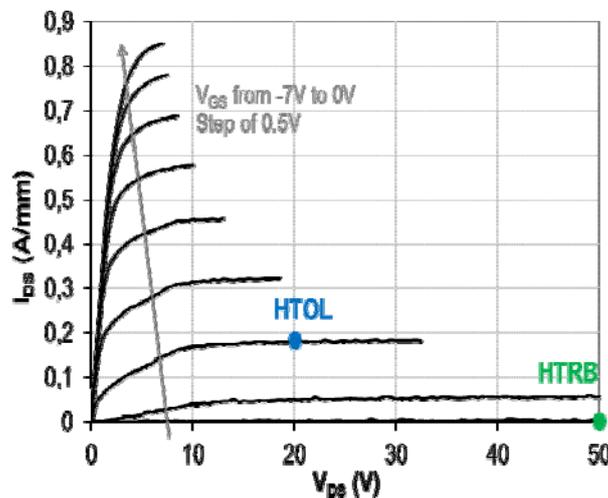


Figure 11. $I_{DS} - V_{DS}$ characteristic with possible bias points of ageing tests HTOL and HTRB used during this work

2.1.1.1 High Temperature Operating Life (HTOL) test

High temperature operating life test (HTOL) is performed to identify the effects of electrical bias and temperature on GaN HEMTs over long periods of stress during which degradation mechanisms or failures are accelerated. HTOL is used for process qualification before the product release and manufacturing for commercialization. A short duration HTOL test known as “burn-in” is used for screening devices with high early failure and infant

mortality rate. The stress conditions are similar to HTOL but usually the stress time is much shorter for burn-in. HTOL is particularly used to assess the wearout mechanism of GaN HEMTs process. It is performed at three to six temperatures generally between 250°C and 310°C with the devices biased at nominal V_{DS} and low I_{DS} . HTOL allows extracting t_{50} that is quite often used instead of MTTF, which is the time when 50% of the devices has failed.

2.1.1.2 High Temperature Reverse Bias (HTRB) test

High temperature reverse bias (HTRB) test is performed to study the robustness of the Schottky contact and to evaluate the HEMT long term stability under high drain-source bias.

During this test, the devices are biased under high V_{DS} , deep pinch-off condition ($V_{GS} \ll V_{TH}$) and high temperature

As the devices under HTRB test are under pinch-off condition where no current is flowing in the channel, the channel temperature is about the same as the case temperature.

The channel temperature can be estimated by using the following equation:

$$T_{CH} = T_C + (R_{TH} \times P_{diss}) \quad (2.2)$$

Where T_{CH} is the channel temperature, T_C the stress case temperature, R_{TH} is the device thermal resistance and P_{diss} is the dissipated power of the device.

2.1.1.3 Step stress

The step stress accelerated test is operated at a fixed temperature, in which parameters like voltage, current or RF power are stepped with time either monotonically or with a recovery period in between [Cheney 2012].

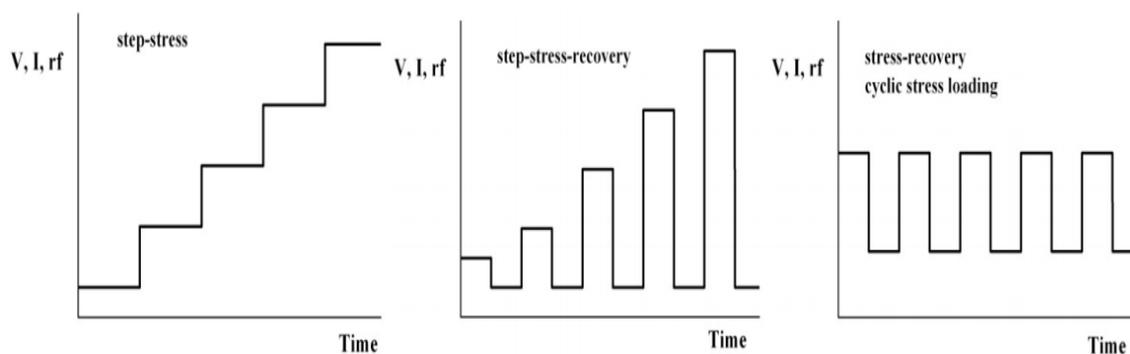


Figure 12. Step stress [Cheney 2012]

The step stress is time dependent; the devices are subjected to a stress that varies with time where the stress remains constant for a short period of time and then is stepped or ramped into a different stress level. The electrical parameters are recorded during the period of stress. If no degradation is noticed, the devices are stressed for another amount of time until important degradations are revealed. This experiment allows inducing cumulative failures during a period of stress without degrading the studied devices in a short time.

The reverse bias step stress is performed by applying a negative bias to the gate while the source and the drain are grounded ($V_{DS} = 0V$). The gate bias is stepped to a very negative value or until device failure and the duration of each step is 1 or 2 minutes [Joh 2008] [Marcon 2010] [Meneghini 2012] [Cullen 2013].

2.1.2 Life time distribution

After performing the appropriate life test, data should be analyzed by an underlying lifetime distribution that describes the GaN based HEMT evolution at different stress levels and a life stress model to quantify the change that occurs to the lifetime distribution during the stress. Generally, the lifetime distributions used for electronic devices include the Weibull, exponential and lognormal distributions. In addition, the Arrhenius life stress model is commonly used.

2.1.2.1 Exponential distribution

The exponential distribution is used to quantify components or systems time to failure with a constant failure rate. It is interesting for its simplicity. The exponential failure function is given by:

$$F(t) = 1 - e^{-\lambda(t-\gamma)} \quad (2.3)$$

Where λ is the failure rate per unit of time and γ is the location parameter. The MTTF is the inverse of the exponential distribution failure rate when $\gamma = 0$. Hence, the reliability function is a 2-parameter exponential distribution function. The feature of the exponential distribution is the constant failure rate λ .

2.1.2.2 Weibull distribution

The Weibull distribution is a general reliability distribution used to model time to failure of electronic components. The Weibull distribution function, called also 3-parameters cumulative density function is given by:

$$F(t) = 1 - e^{-\left(\frac{t-\gamma}{\alpha}\right)^\beta} \quad (2.4)$$

Where t is the time and α , β , and γ are the three parameters of the Weibull distribution function that represents respectively the scale parameter, the shape parameter, and the location parameter.

The main feature of the Weibull distribution for which it is widely used is its versatility. The whole range of electronic devices lifetime behaviors can be modeled by the Weibull distribution function, depending on the values of the three parameters α , β , and γ .

The Weibull parameter β determines the failure rate characteristics by considering the value of β ($\beta < 1$ or $\beta = 0$ or $\beta > 1$). The three bathtub curve regions can be modeled with the Weibull distribution function by changing the value of β .

Marcon et al. [Marcon 2013] have demonstrated that the time to breakdown (t_{BD}) data of time dependent breakdown (TDB) experiments of GaN based HEMTs can be fitted by a

Weibull distribution function. Moreover, Bahl et al. [Bahl 2013] have shown that the breakdown voltage of GaN based HEMTs are Weibull distributed.

2.1.2.3 Lognormal distribution

The lognormal distribution is a reliability distribution of a random variable which natural logarithm of the failure to time is normally distributed. A variable can be modeled as lognormal when it results from many independent random variables.

The lognormal distribution function is given by [lognormal]:

$$F(t) = F(t, \mu, \sigma) = \frac{1}{t\sigma\sqrt{2\pi}} e^{-\frac{(\ln(t)-\mu)^2}{2\sigma^2}} \quad (2.5)$$

Where μ and σ are respectively the mean and the standard deviation of the natural logarithm of the time to failure and t is the time.

Different works showed that the time to failure (TTF) statistics of GaN based HEMTs from different foundries followed a lognormal distribution [Singhal 2005] [Singhal 2007] [Gajewski 2011] [Lee 2013].

Stoffels et al. [Stoffels 2013] showed that the cross section for single events switching (SES) of AlGaIn/GaN MISHEMTs under heavy ion irradiation exhibited a lognormal distribution with a median value in the range of the gate area, and the capture cross section exhibited slight voltage dependence.

2.1.2.4 Arrhenius life-stress model

The Arrhenius life stress model is the most common life stress relationship used in accelerated life testing. It is widely used when one acceleration stress factor is the temperature. It is based on Arrhenius reaction rate equation proposed by the Swedish physical chemist Svante Arrhenius in 1887 given by:

$$R(T) = Ae^{-\frac{E_a}{k_B T}} \quad (2.6)$$

Where R is the reaction rate, A is a non-thermal constant, E_a is the activation energy, k_B is the Boltzmann's constant and T is the temperature.

The Arrhenius life stress model is formulated by assuming that lifetime is inversely proportional to the reaction rate of process to failure. Thus, equation (2.6) can be rewritten as:

$$L_T = Ce^{\frac{E_a}{k_B T}} \quad (2.7)$$

Where L_T is the component lifetime, such as mean lifetime, and C is a constant estimated from the lifetime data [Kececioglu 1984].

The lifetime L_{Tu} at operational temperature T_u and accelerated temperature T_a are given by:

$$L_{Tu} = Ce^{\frac{E_a}{k_B T_u}} \quad (2.8)$$

$$L_{Ta} = C e^{\frac{E_a}{k_B T_a}} \quad (2.9)$$

Consequently, the ratio of lives at use and accelerated conditions is:

$$\frac{L_{Tu}}{L_{Ta}} = e^{\left[\frac{E_a}{k_B} \left(\frac{1}{T_u} - \frac{1}{T_a} \right) \right]} \quad (2.10)$$

The acceleration factor in accelerated life tests is given by:

$$A_F = \frac{L_{Tu}}{L_{Ta}} = e^{\left[\frac{E_a}{k_B} \left(\frac{1}{T_u} - \frac{1}{T_a} \right) \right]} \quad [\text{Kececioglu 1984}] \quad (2.11)$$

The activation energy (E_a) of a failure mechanism is determined by performing an accelerated life test at a minimum of three accelerated temperatures. The ageing tests will provide the lifetime of the devices at each temperature. From equation (2.11), the activation energy is obtained as follows:

$$E_a = k_B \left(\frac{\ln(L_{Tu}) - \ln(L_{Ta})}{\frac{1}{T_u} - \frac{1}{T_a}} \right) \quad (2.12)$$

The end of life mechanism of the GH50 UMS GaN process was assessed by performing HTOL test at various temperatures between 270 °C and 310 °C. The good agreement to the Arrhenius law showed a T_{50} of 3×10^7 hours at a junction temperature of 175 °C with an associated activation energy of 1.82 eV (figure 13) [Lambert 2012].

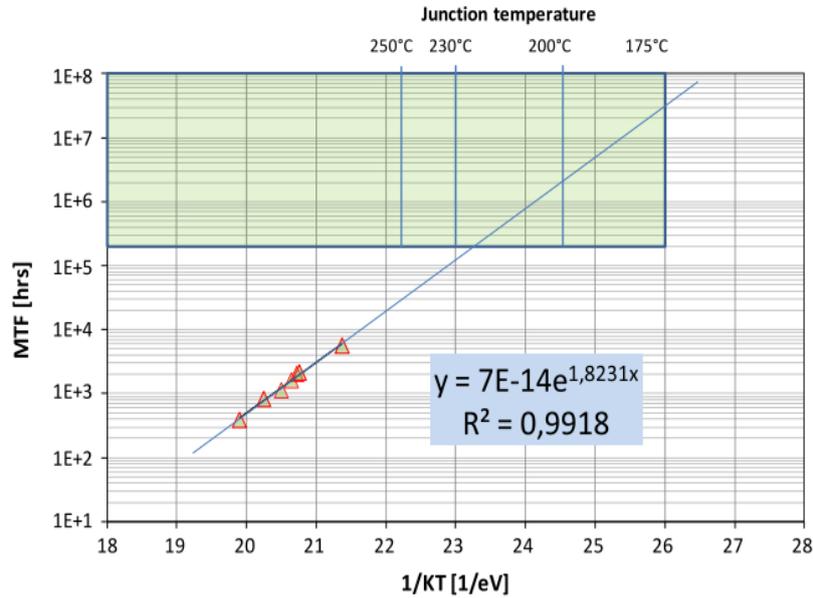


Figure 13. T_{50} vs temperature for three temperature HTOL test performed at $V_{DS} = 50V$ and $I_{DS} = 100 \text{ mA/mm}$ [Lambert 2012]

2.2 Parasitic effects and degradation mechanisms

The parasitic effects are the undesirable effects that appear on the I-V characteristics of fresh devices and reduce the electrical performances without impacting the lifetime of the device. The slow drain current transient that is observed when the gate or the drain bias is

changed abruptly is problematic in circuit applications. The decrease of the drain current at high electric field and open channel conditions accompanied by an abrupt increase of the drain conductance known as the kink effect is causing the device instability during operation. Another harmful parasitic effect in GaN based HEMTs is trapping effects that occur at different places of the device.

Degradation mechanisms are the processes that occur in the device structure during an accelerated life test or operational life and decrease the electrical performances and the reliability, thus the lifetime of devices. The devices might be submitted to ageing tests at high temperatures or high reverse electric field for characterization and modeling of the degradation mechanisms, that could induce damages, cracks, pits, grooves in the device layers or migration of metals from a layer to another. The degradation mechanisms might be irreversible and reduce drastically the lifetime of the device. An example of the most cited degradation mechanisms of GaN based HEMTs are: gate contact degradation that is critical as it limits the control of the Schottky gate of the channel [Zanoni 2013] and the inverse piezoelectric effect causes the permanent increase of the gate leakage current which reduces the efficiency of the device and hence induces the onset of the device breakdown [Bahat-Treidel 2012].

2.2.1 Trapping effects

Trapping effects have been always considered as a critical issue for AlGaIn/GaN HEMTs technology as they occur at different locations of the device structure such as at the surface of the AlGaIn layer near the gate edges or at the metal/AlGaIn interface, inside the AlGaIn or GaN layers or at AlGaIn/GaN interface. The trapping phenomena are responsible of the degradation of RF performances known as RF dispersion, current collapse or power slump.

A typical matter of concern for high voltage switching transistors is the fact that trapping and/or degradation effects might give rise to a large increase of the dynamic on-state resistance (R_{ON}). This means that during switching the effective on-state resistance is much higher than suggested by DC-characterization only. It is strongly dependent on internal field distribution in the device and can be irreversible if a technology related device threshold electrical field is exceeded [Saito 2011].

The model or the concept of the virtual gate has been introduced by Vetury et al [Vetury 2001] to explain how traps cause a reduction of the output power. By considering that electrons from the metal gate get trapped at the AlGaIn surface, the positive charge present at the AlGaIn layer is reduced and the surface potential is made negative. Thus, this leads to the depletion of electrons of the channel and to the extension of the gate depletion region. The surface negative charge acts as a negatively biased metal gate. Thus, there are now two gates on the surface, between the source and drain, connected in series as shown in figure 14. The potential on the metal gate is controlled by the applied gate bias while the potential on the second gate, is controlled by the total amount of trapped charges in the gate drain access region. This second gate is referred to as the virtual gate. By considering the virtual gate model, the output drain current is controlled by the mechanism that supplies charges to, and

removes charges from the virtual gate, in addition to the applied gate bias. The trapping/de-trapping mechanisms control the frequency response of the device.

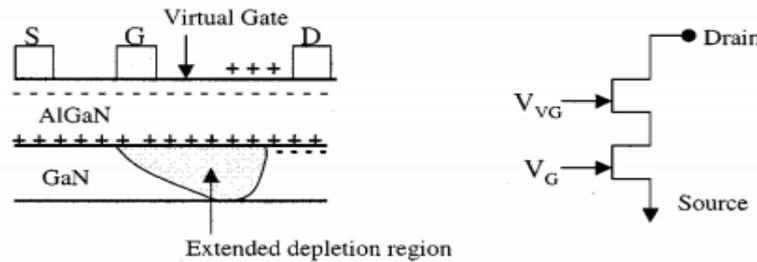


Figure 14. Schematic of the model of the virtual gate [Vetry 2001]

2.2.2 Kink effect

The kink effect has been observed and analyzed for different transistors: silicon MOSFET's [Hafez 1990], GaAs MESFETs [Horio 1995], SiGe HBT's [Peter 1999] and GaAs based HEMTs [Mazzanti 2002], including GaN based HEMTs [Lin 2005] [Xu 2013] [Wang 2011] [Meneghesso 2009] [Killat 2013] [Kaushik 2013].

The kink effect is characterized by an increase of the drain current I_{DS} in the output characteristic at $4V < V_{DS} < 8V$ (V_{DSkink}) (figure 15). As a consequence, the output conductance G_d in the saturation regime is maximum at V_{DSkink} .

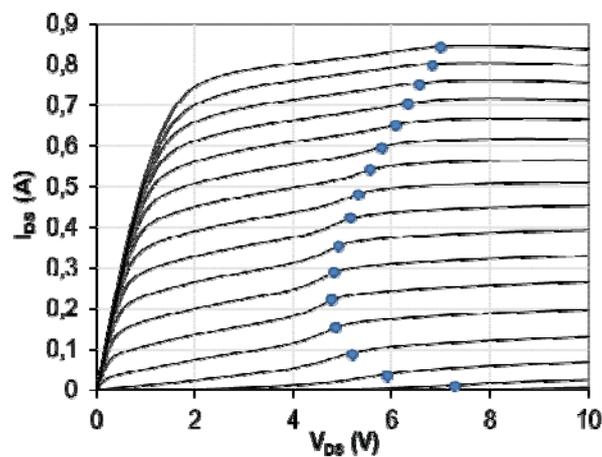


Figure 15. $I_D - V_{DS}$ with a V_{GS} from 0 to -4V with a step of -0.2V. Blue circles correspond to the kink region (V_{KINK}).

In GaN based HEMTs, the kink effect has been attributed to different mechanisms. Lin et al. [Lin 2005] proposed that kink effect, in Si_3N_4 passivated GaN based HEMT, was activated by trapping effect at cryogenic temperature. Xu et al. [Xu 2013] have reported that kink effect in AlGaN/GaN HEMTs can be decreased by using Al_2O_3 passivation replacing Si_3N_4 . Wang et al. [Wang 2011] have suggested that kink effect is probably induced by hot electron trapping and field dependent detrapping of electrons from donorlike buffer traps. Meneghesso et al. [Meneghesso 2009] suggested that the kink effect could be induced by interband impact ionization of electrons by slow traps in the epitaxial layers under the gate, possibly in the GaN buffer.

2.2.3 Current collapse

Current collapse is a phenomenon of particular concern in AlGaIn/GaN HEMTs, as it reduces the device output power, and degrades the power switching efficiency. Current collapse is observed at high drain-source voltage of the dc I-V characteristic, which results in a decreased drain current with an increase in the knee voltage as showed in figure 16.

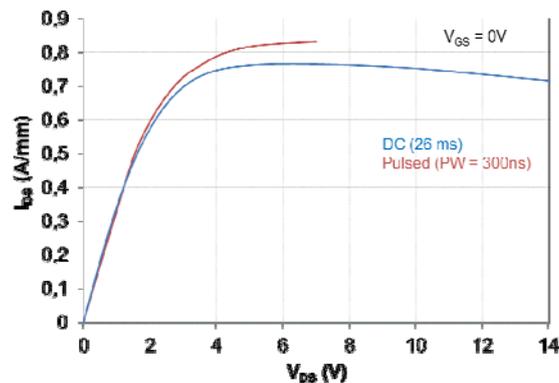


Figure 16. DC and pulsed I_{DS} - V_{DS} characteristics at $V_{GS} = 0V$

Klein et al. [Klein 2001] attributed the current collapse to the deep traps in the high resistive GaN buffer layer that are introduced by carbon doping. The deep trap incorporation causing current collapse was correlated with the growth pressure of GaN buffer layer by the metal organic vapor phase epitaxy (MOVPE). Current collapse causes the increase of the on-state resistance; Saito et al. [Saito 2014] showed the importance of optimization of the field plate design and GaN-layer crystal quality to suppress current collapse. Kawanago et al. [Kawanago 2014] studied the gate metal contribution to the current collapse in the AlGaIn/GaN HEMTs. They suggested the involvement of electron trapping on the defects in the AlGaIn layer caused by gate metal under the gate. Also, the nitrogen vacancies in the AlGaIn layer were pointed out to be responsible for electron trapping in AlGaIn layer.

2.2.7 Belly shape

The “belly shape” effect is an electrical parasitic effect that appears on the gate-source and gate-drain diodes forward bias I-V characteristics of AlGaIn/GaN HEMTs after HTRB [Brunel 2013] or HTOL [Ando 2013] ageing tests as shown in figure 17.

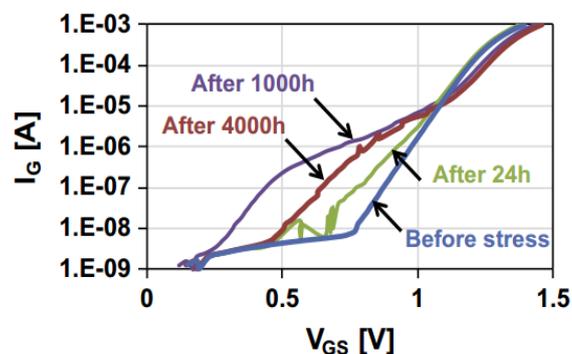


Figure 17. Evolution of the Schottky diode forward characteristic at $V_{DS} = 0V$ during HTRB test [Brunel 2013]

Brunel et al. [Brunel 2013] detected the “belly shape” effect on GaN based HEMTs that were stressed by HTRB stress carried out at 175°C up to 4000 hours. This parasitic effect has been attributed to lateral surface conduction and correlated with EL signature under diode forward biasing conditions but not under transistor pinch-off biasing conditions. Then, physical analyses have pointed out the formation and growing over time of pits and cracks at the gate edge on the drain side that could not be correlated with “belly shape” effect. Ando et al. [Ando 2013] detected the “belly shape” effect on GaN based HEMTs that were stressed by HTOL test for 1 hour: $V_{DS} = 50V$ and $I_D = 87.5mA/mm$ and a channel temperature $T_{CH} = 270$ °C. This effect was correlated with the thinning or partial vanishment of GaN cap layer and void formation in the gate edges.

2.2.8 Inverse piezoelectric effect

The piezoelectric nature of GaN and AlGaIn materials makes that a vertical electric field induces mechanical stress inside these materials. Joh [Joh 2006] and Del Alamo [Del Alamo 2009] have investigated the electrical reliability of AlGaIn/GaN HEMTs. They have explained the sudden and non-reversible increase in the gate leakage current during reverse bias stress of the gate Schottky of GaN based HEMTs by excessive stress associated with inverse piezoelectric effect. Indeed, AlGaIn layer on GaN is typically under significant tensile strain due to the lattice mismatch between the AlGaIn layer and the buffer layer and therefore a sizable amount of elastic energy is stored in the barrier layer, even without applying a bias. By applying a reverse bias to an AlGaIn/GaN HEMT, the electric field increases sharply to achieve a high peak at the drain side edge of the gate, thus the tensile strain and the elastic energy increases in the gate edge where the electric field achieves its highest value. Once a critical value of the elastic energy is achieved, crystallographic defects are formed. These defects can cause the degradation of the electrical characteristics as they are activated electrically through traps for example.

Micro-Raman spectroscopy was used by Sarua et al [Sarua 2006] to study piezoelectric strain in AlGaIn/GaN HEMTs under bias. The measurements were made through the transparent SiC substrate. The strain in GaN was found to be related to the electric field component normal to the surface and was particularly located in the gate-drain gap and in the area underneath the drain contact. Micro-Raman spectroscopy was also used to study inverse piezoelectric effect in undoped and Fe-doped AlGaIn/GaN HEMTs with different substrate types [Sarua 2010]. A considerable strain/stress was found in undoped samples, on the other hand, the Fe doping causes confinement of the strain/stress in the AlGaIn/GaN interface near the electron channel.

2.3 Objectives of this study within ReAGaN project

ReAGaN which means Reliability Analysis of GaN technologies – Development of an innovative methodology for physical and electrical analysis at the device scale – is the title of the project in which my thesis is involved. The main purpose of this project is to develop a toolbox with different techniques for the characterization of transport mechanisms and structural defects of GaN based HEMTs. These defects induce degradations and are hampering the performances and the reliability of these devices. Emphasis was placed on

deep characterization of physical and structural parameters of GaN and AlGaIn epitaxial layers that forms the AlGaIn/GaN heterostructure. In addition to the strain of the AlGaIn layer due to the piezoelectric field and Aluminum alloy composition, the polarization field of GaN layer is a crucial parameter to understand the problems that occur in the heterostructure.

2.3.1 Methodology and techniques

In order to meet the target of the project efficiently, analysis techniques should have been developed or adapted from previous experiences with other technologies to be dedicated to structures based on wide-band gap semiconductors and particularly to GaN based HEMTs. As described in figure 18, these techniques include Opto-Electrical characterization (task 3) and advanced physical analysis (task 4).

The innovative approach of ReAGaN is the correlation between physical analyses used to localize defects at the nanometric scale and opto-electrical analysis performed at the device scale. This would allow deep understanding of electrical and optical signatures of GaN based HEMTs defects and their physical origin.

The complementarity of the developed techniques and the scientific and technical expertise of the project partners aimed to contribute in the development of GH50 and GH25 UMS GaN technology processes. This has been possible by defining and establishing an efficient failure analysis methodology to understand in depth the degradation mechanisms of GaN based HEMT technology.

ReAGaN project is funded by ANR (Agence Nationale de la Recherche) with the contribution of three French industrials and three French laboratories that belong to the CNRS (Centre National de la Recherche Scientifique):

- United Monolithic Semiconductor (UMS) – Villeneuve-sur-Yvettes (France)
- THALES Research and Technology (TRT) – Palaiseau (France)
- SERMA technologies – Grenoble (France)
- LAAS – UPR CNRS, Toulouse (France)
- LEPMI – UMR CNRS 5279, Grenoble (France)
- IMS – UMR CNRS 5218, Bordeaux (France)

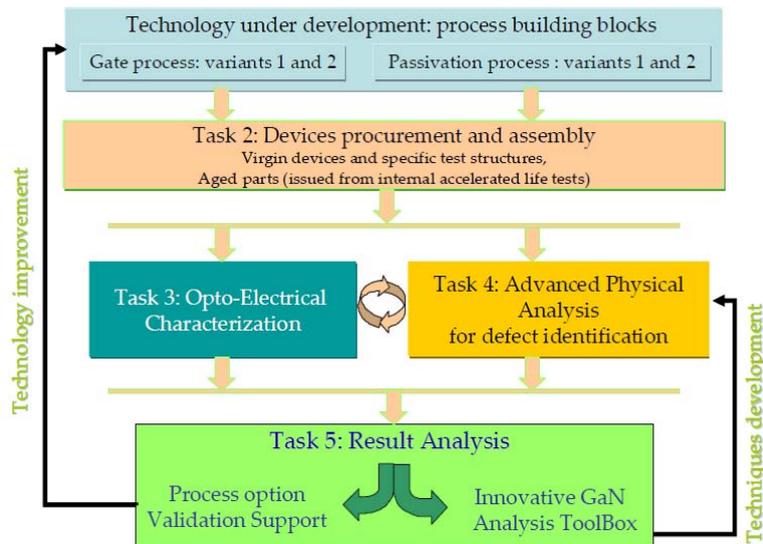


Figure 18. ReAGaN project structure [ReAGaN]

2.3.2 Failure analysis for defect localization

Failure analysis is used to determine the cause of a failure in a circuit or a system. The failure analysis process in ReAGaN project relies on collecting devices with atypical behavior or degraded samples after an accelerated life test or samples issued from the same process with variants of gate metallization or Al alloy composition of the AlGaIn layer.

The electrical characterization of AlGaIn/GaN HEMTs studied in this thesis is part of the third task of ReAGaN project: Opto-Electrical characterization (figure 18). In the third task are also involved L.A.A.S. laboratory and Thales Research and Technology (TRT) society. Complementary electrical characterization with IMS laboratory and low frequency noise measurements are performed by L.A.A.S., while the optical analysis (Emission microscopy, OBIRCH technique and electroluminescence) were conducted by TRT. The task 4 of ReAGaN project gathers the work of SERMA about failure analysis (TEM, EDX) and LEPMI laboratory that performed Raman spectroscopy.

2.4 Electrical characterization procedure at IMS for ReAGaN project

At the IMS laboratory, we investigate electrical parasitic effects of AlGaIn/GaN HEMTs by using DC, pulsed I-V and transient electrical characterizations. The purpose is to understand the conduction mechanisms and the degradation mechanisms that are hampering the GaN based HEMT technology.

2.4.1 DC measurements

The DC I-V measurement is performed by using the standard method of four-point probes or Kelvin measurements that yields accurate results compared to the two probe measurements. The measurement system is composed of an HP4142 DC source-monitor that is a computer controlled DC parametric instrument using ICCAP Agilent software. The measurements are performed by using TTPX Lakeshore probe station (shown in figure 19)

which test fixture was adapted to UMS devices. The I_G - V_{GS} , I_D - V_{GS} and I_D - V_{DS} characteristics were carried out for temperature from 100K to 400K to evaluate and analyze the temperature influence on the Schottky contact and on the key parameters of the GaN based transistors.

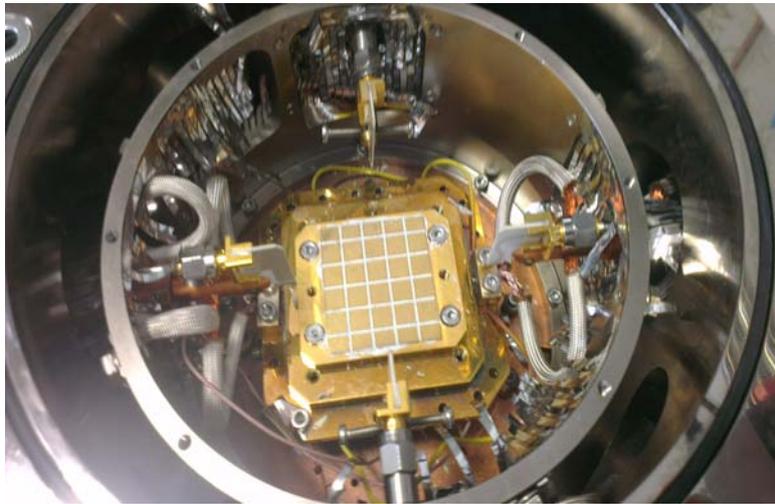


Figure 19. TTPX Lakeshore cryogenic probe station

2.4.2 Pulsed measurements

The pulsed I-V measurements allow studying thermal and trapping effects in power microwave transistors like GaN HEMTs.

The measurement system was designed by MC². It is supplied with two pulsed heads, one dedicated for high voltage and high current suitable for the drain (APMS-HPM) and the second one designed to reach high accuracy in lower voltage and current suitable for the gate (APMS-LPM). Two external power supplies are needed (figure 20)

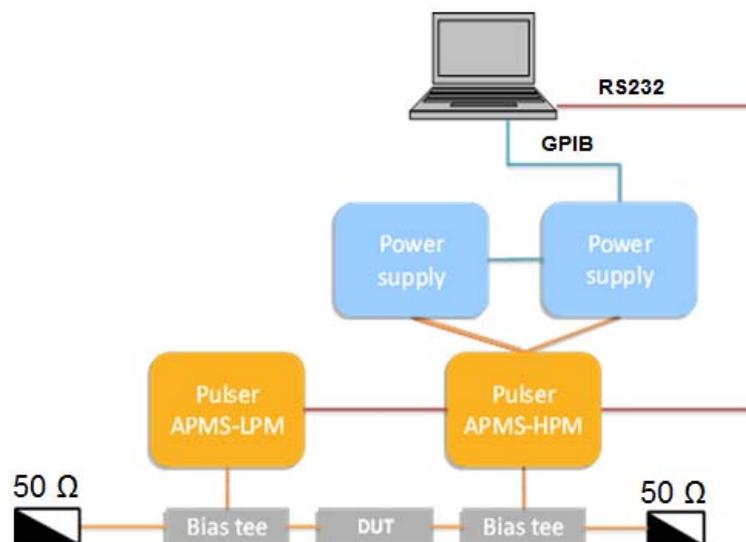


Figure 20. Pulsed I-V measurement setup

The bias tees are generally used to measure the S-parameters in pulsed mode and also to stabilize the component by avoiding oscillations. We have studied the influence of the bias tees on the pulsed I-V measurements. The used bias tee is a KEYSIGHT 11612A that operates in the frequency range of 45 MHz-26.5 GHz.

The pulsed I-V measurements were carried out at different quiescent bias (QB) conditions (V_{GS0} , V_{DS0}) to quantify the gate and drain lag phenomena. The waveforms $V_{DS}(t)$ and $I_{DS}(t)$ were extracted to verify the stability of the quiescent and instantaneous biases of the device; as a consequence, it is ensured that instantaneous measurements are performed in the time window within which $V_{DS}(t)$ and $I_{DS}(t)$ are stable. A pulse width (PW) of 300 ns is used to study the lag phenomena and the dynamic resistance R_{ON} .

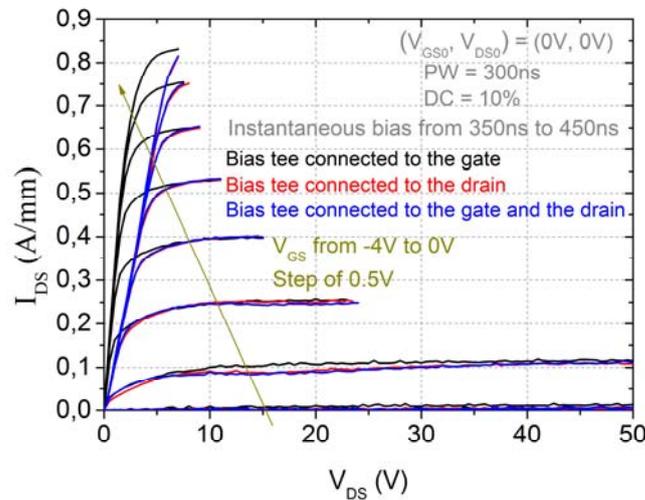


Figure 21. Pulsed I-V measurements at $(V_{GS0}, V_{DS0}) = (0V, 0V)$, connecting the bias tee on the gate (black line) or the drain (red line) or both (blue line).

Figure 21 shows 300 ns pulsed I-V measurements of a representative fresh device using the quiescent bias condition $(V_{GS0}, V_{DS0}) = (0V, 0V)$ with a duty cycle of 10% while connecting a bias tee on the gate or the drain or both electrodes. To minimize noise and enhance measurement accuracy, an average of 1024 measurements is performed.

Figure 22 shows a typical $I_{DS}(t)$ waveform by using the quiescent bias condition $(V_{GS0}, V_{DS0}) = (0V, 0V)$ at $V_{GS} = 0V$ for V_{DS} from 0 to 7V.

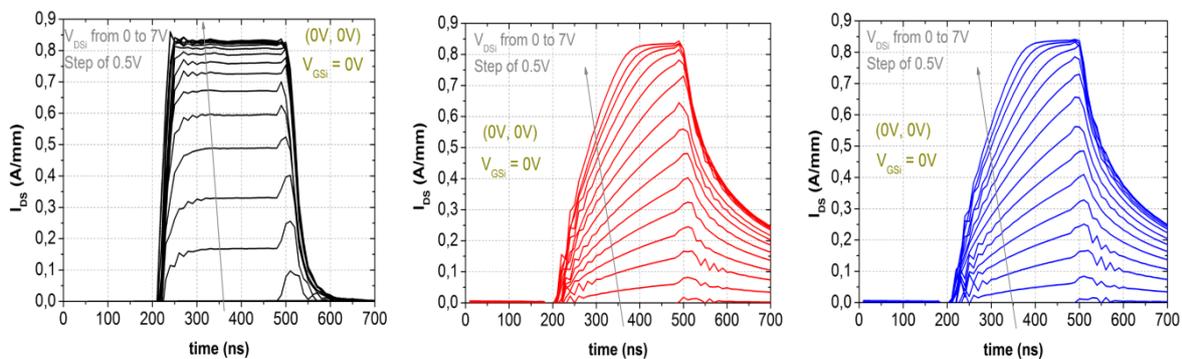


Figure 22. $I_{DS}(t)$ waveform measured by pulsed I-V measurement setup at $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and pulse width (PW) of 300 ns and duty cycle (DC) of 10% connecting the bias tee on the gate (black line) or the drain (red line) or both (blue line)

The quiescent bias is measured from 50 ns to 150 ns, and the instantaneous bias is measured from 350 ns to 450 ns. When the bias tee is connected only on the gate, the $I_{DS}(t)$ waveform is steady in the instantaneous bias window for the whole instantaneous bias V_{DSi} range. On the other hand, when the bias tee is connected to the drain, the $I_{DS}(t)$ waveforms are not steady in the instantaneous bias window. Thus, the noticeable increase of R_{ON} in figure 21 is due essentially to capacitive and inductive effects of the bias tee.

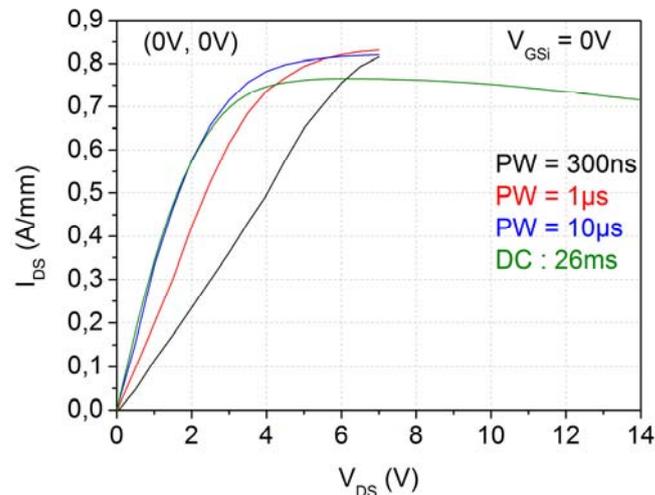


Figure 23. Pulsed I-V measurements at $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and PW of 300 ns, 1 μ s and 10 μ s and DC of 10% connecting the bias tees on both the gate and the drain and DC I-V measurement at $V_{GS} = 0V$

Figure 23 shows pulsed I-V measurements at $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and pulse width of 300 ns, 1 μ s and 10 μ s and a duty cycle of 10% at $V_{GSi} = 0V$ with the bias tees connected on the gate and the drain and dc I-V measurement at $V_{GS} = 0V$. The slope of pulsed I_D vs. V_{DS} increases by increasing the pulse width from 300 ns to 10 μ s. Thus, R_{ON} decreases by increasing the pulse width to achieve the value of R_{DS} at PW = 10 μ s.

Jin and Del Alamo ([Jin 2012] and [Jin 2013]) have reported on the rise of the slope of I_D vs. V_{DS} by increasing the pulse width from 200 ns to 1 ms. They showed that during off-to-on transients, dynamic R_{ON} is enhanced up to several times of its original dc value, particularly as the off-state voltage increases and that the increase of R_{ON} is reversible.

The $I_{DS}(t)$ waveforms at $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and pulse widths of 300ns, 1 μ s and 10 μ s with the bias tees connected on the gate and on the drain are plotted in figure 24. The $I_D(t)$ waveforms show that the bias tees act as filters at frequencies higher than 0.1 MHz and their influence get reduced by increasing the pulse width PW. Hence, R_{ON} is low in these measurement conditions and achieves the value of R_{DS} measured with PW of 10 μ s.

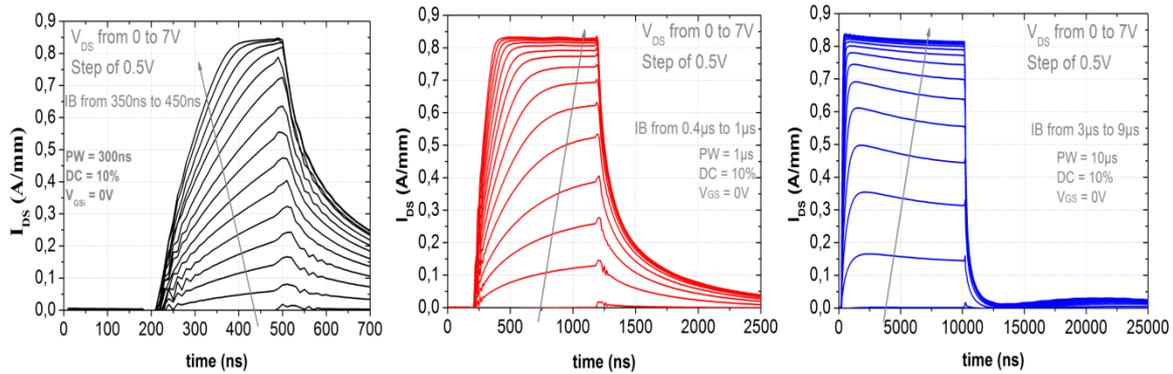


Figure 24. $I_{DS}(t)$ waveforms measured by pulsed I-V measurement setup at $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and pulse width (PW) of 300ns, 1 μ s, 10 μ s and duty cycle (DC) of 10% with a bias tee connected on the gate and on the drain.

The verification of $I_{DS}(t)$ waveform is important for the validity of the pulsed I-V measurements before the analysis of the pulsed I-V characteristics.

2.4.3 Transient measurements

The trapping/detrapping processes associated to deep traps were studied by drain current transient spectroscopy (DCTS). This method is based on the analysis of the drain current transients and their evolution with temperature.

The principle of the measurement, as shown in figure 25, is to measure the drain current transient response by applying a voltage pulse with a period T on the gate while the HEMT is biased in saturation mode. The test bench is composed of a pulse generator (HP8116A) and a digital multimeter (HP34401A) connected to a resistor of 1 Ω in order to obtain a direct image of the drain current. The HP 8116A operates over the frequency range 1 mHz to 50 MHz and is capable of driving a 16 V peak-to-peak amplitude output signal into a 50 Ω load. The acquisition time of each measurement to observe emission or capture phenomena is 50 s with a step of 7 ms.

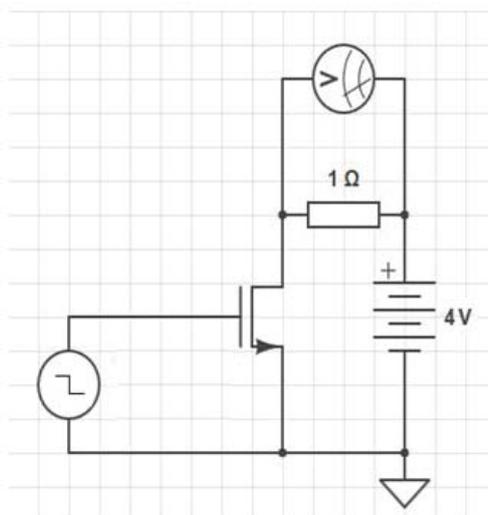


Figure 25. Principle of the DCTS measurement

The square pulse that is applied to the gate with a period T has a high level (HL) and a low level (LL). This signal is applied while the HEMT is biased in saturation regime by

maintaining the bias V_{DD} in a steady state during the measurement. The evolution of the drain current with time is measured when the square pulse changes from HL to LL during half of the signal period T . Each measurement is performed 10 times then averaged to increase the signal to noise ratio. Traps charge or discharge mechanisms are inducing capture and emission phenomena. The transients follow exponential law and allow identifying both capture and emission mechanisms as shown in figure 26. Measured drain current transients are then normalized to the final value of the current at equilibrium state [Brunel 2012].

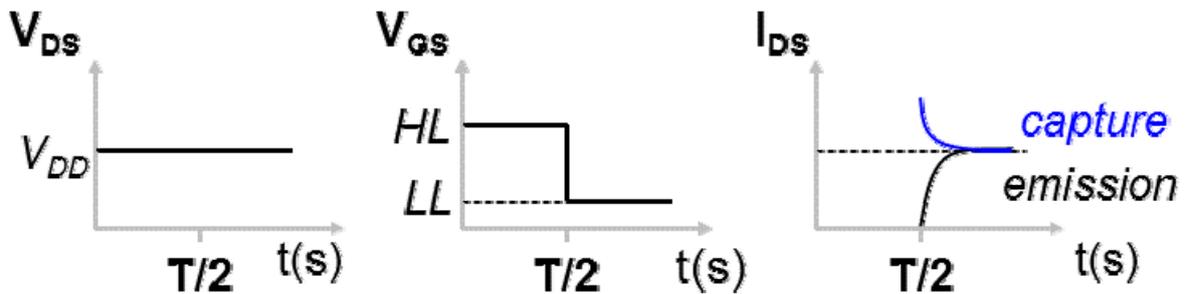


Figure 26. Principle of the DCTS measurement

2.4.4 Low frequency noise measurements

The test bench of the low frequency noise associated to gate current is illustrated in figure 27. It contains a transimpedance amplifier EG&G 5182 connected to the gate bias circuit. The gate current is measured through the DC output of the transimpedance amplifier. A signal analyzer HP3562A is connected to measure the noise spectra. Moreover, a digital multimeter is connected to the DC output of the transimpedance to measure and to fix the bias voltage of the gate. A Faraday cage contains the cryostat where the device under test (DUT) is connected, the trans-impedance amplifier, the multimeter and the biasing circuit.

Gate current low frequency noise (LFN) measurements are used as a tool to study the fluctuations of the gate current as well as the transport properties that are strongly influenced by crystalline defaults and/or trapping effects.

The test bench can be used to measure the low frequency noise associated with the drain current by changing the transimpedance amplifier by the voltage amplifier EG&G 5184.

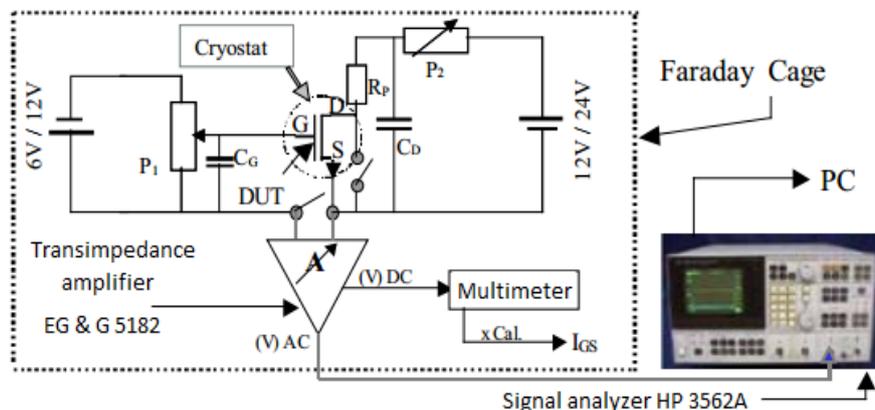


Figure 27. Principle of the test bench configured for the measurement of the low frequency noise gate current [Curutchet 2005]

2.5 Conclusions: Objectives of ReAGaN project and thesis

In the first part of this chapter, a general definition and state of the art of the reliability of GaN based HEMTs have been discussed. In order to define the lifetime of a device, time to failure data should be analyzed correctly. The use of accelerated life tests allows the quantification and understanding of degradation or failure mechanisms that occur at normal use conditions. The accelerated life tests under high temperature or high reverse bias are the most used in the qualification of industrial process. Three of the most used lifetime distributions (exponential, lognormal and Weibull) have been illustrated. Furthermore, the Arrhenius life stress model and the equations that allow obtaining the activation energy have been detailed.

The parasitic effects and the degradation mechanisms that are limiting the performances and the reliability of GaN based HEMTs have been introduced and discussed.

Then, the ReAGaN project which this thesis is involved is described. The description involves the definition of the objectives of the project, and then the methodology and the different techniques used to provide answers to questions about reliability and correlation of electrical degradations to physical failures have been resumed. In the last part of this section, two types of failures analysis for defect localization (non-destructive and destructive) have been discussed.

In the last section of this chapter, the technical characterization procedure used at IMS laboratory for ReAGaN project is illustrated and the characterization techniques are detailed.

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Chapter 3: Electrical characterization and degradation mechanisms of AlGaIn/GaN HEMTs

This chapter is divided into four case studies, three case studies that have been investigated in the frame of ReAGaN project and the fourth one in the Extreme GaN project.

The purpose of the first case study is to investigate the conduction mechanisms inducing the leakage current in AlGaIn/GaN HEMTs provided from GH50 process. DC and transient measurements were performed from 80K to 420K and pulsed measurements at room temperature to study subthreshold leakage current and the trapping effects. After the on-wafer electrical characterization, components were shared in two categories depending on the gate leakage current level: “leaky”-”L” and “non-leaky”-”NL”. The components are considered leaky if I_G is higher than $200\mu\text{A}/\text{mm}$ at $V_{DS} = 50\text{V}$ and $V_{GS} = -7\text{V}$. The positive and negative dependence of the gate and drain subthreshold leakage current with temperature from 300K to 400K were investigated by DC and transient measurements to identify trap effects.

The purpose of the second case study is to characterize an electrical parasitic effect that is detected on the gate-source and gate-drain diodes forward current characteristics after temperature accelerated life tests. Virgin and aged devices from the GH25 UMS GaN process have been characterized electrically. HEMTs have been aged by 20V High Temperature Operating Life (HTOL) stress carried out at $T_{CH} = 155^\circ\text{C}$ and $I_{DS} = 210\text{mA}/\text{mm}$ during 7000 hours. DC, pulsed, transient measurements and low frequency noise associated with gate current have been used to characterize the parasitic effect.

The purpose of the third case study is to study the influence of the Aluminum (Al) mole fraction on the DC electrical parameters of AlGaIn/GaN HEMTs with strained AlGaIn layer. Virgin and aged devices from the GH25 UMS GaN process have been characterized electrically. A High Temperature Reverse Bias (HTRB) stress has been carried out on four devices from two lots at $V_{GS} = -7\text{V}$ and $V_{DS} = 30\text{V}$ during 2200 hours with a base plate temperature of 175°C to evaluate the Schottky contact stability over time as a function of Al mole fraction.

The aim of the last case study is to determine the limits of operation of the GH25 GaN process. This work consisted in the quantification of the dispersion of the electrical parameters of devices issued from GH25_10 UMS GaN process and the determination of the safe operating area (SOA) of this technology by studying the Schottky diode and off-state breakdown voltages at room temperature and at high temperature from 50°C to 150°C .

3.1. Case study 1: Subthreshold leakage current

3.1.1 Purpose of the case study

The purpose of this case study is to understand the conduction mechanisms inducing the leakage current in AlGaIn/GaN HEMTs. Virgin GaN based HEMTs from the GH50 UMS GaN process have been characterized. After the on-wafer electrical characterization some devices have shown higher gate and drain leakage currents than the UMS acceptance criterion of the leakage current. The components were shared in two categories depending on the leakage current level: “leaky”-“L” and “non-leaky”-“NL”. The components are considered leaky if I_G is higher than $200\mu\text{A}/\text{mm}$ at $V_{DS} = 50\text{V}$ and $V_{GS} = -7\text{V}$.

3.1.2 DC I-V characteristics

3.1.2.1 Gate Schottky diode characteristics: $I_G - V_{GS}$

The input $I_G - V_G$ characteristics were measured at $V_{DS} = 0\text{V}$ in forward and reverse modes from 100K to 400K with a step of 20K for two representative “NL” devices (A4 and A5) and two representative “L” devices (A17 and A26) issued from the same wafer.

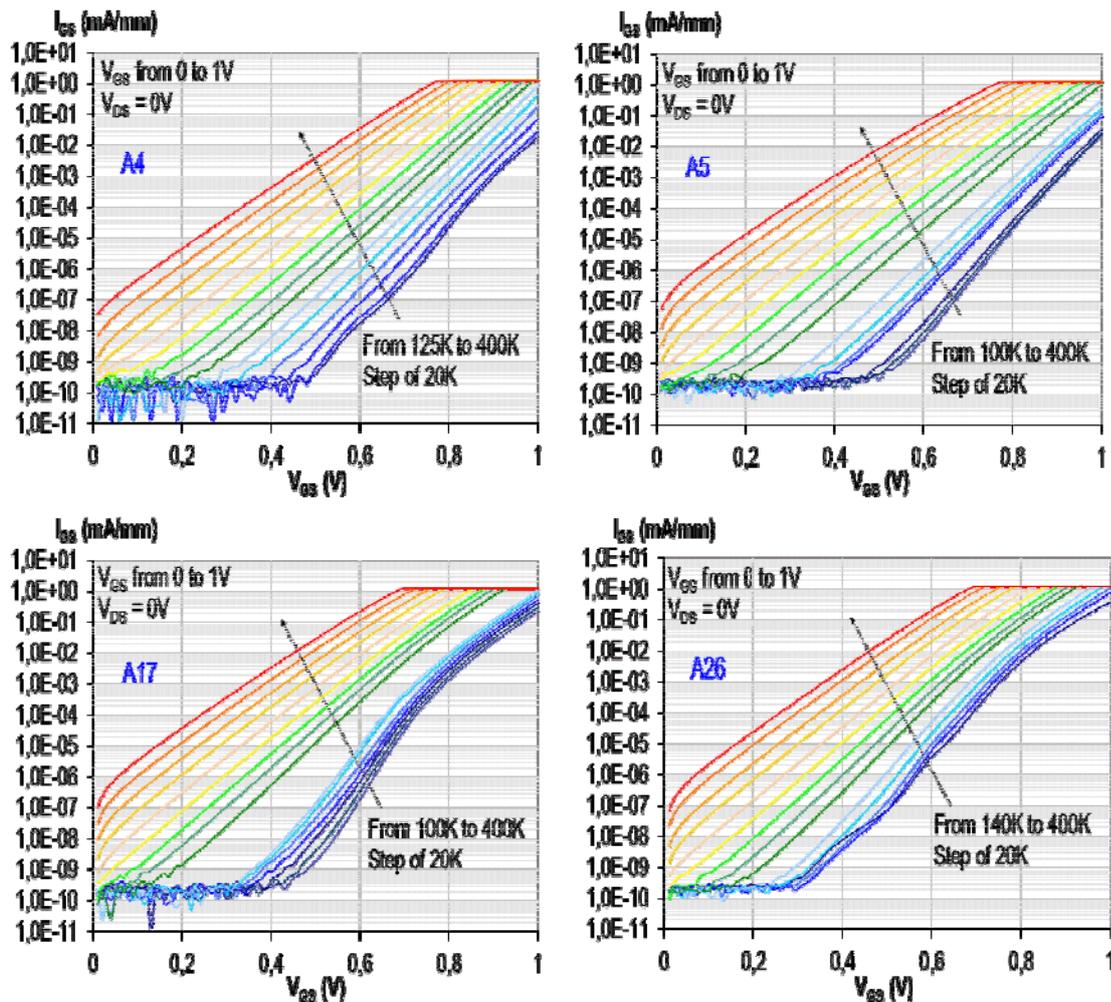


Figure 28. $I_G - V_{GS}$ measurements at $V_{DS} = 0\text{V}$ in forward bias for A4, A5, A17 and A26 for temperature from 100K to 400K

In forward mode (figure 28), the thermionic mechanism is dominant from 300K to 400K for all devices. On the other hand, from 100K to 220K we notice an unusual behavior of the Schottky diode characteristics more pronounced for the leaky devices, which highlights the influence of other transport mechanisms. Chikhaoui et al. [Chikhaoui 2011] explained this mechanism by multiple Schottky barriers associated to energies lower than the barrier height identified for the thermionic mechanism, and through which the carrier transport would be enhanced.

The forward I_G - V_{GS} characteristics might be analyzed using the standard thermionic emission relation (1) for electron transport from the semiconductor to the metal, given by,

$$I_G = I_S \left\{ \exp \left[\frac{q(V_{GS} - R_S I_G)}{nk_B T} \right] - 1 \right\} \quad (3.1)$$

That can be reduced to the following equation, if $V_{GS} \gg R_S I_G$,

$$I_G = I_S \exp \left(\frac{qV_{GS}}{nk_B T} \right) \quad (3.2)$$

Where V_{GS} is the applied voltage, n is the ideality factor, T is the temperature, k_B is the Boltzmann constant (1.38×10^{-23} J/K.s²), q is the elementary electric charge (1.602×10^{-19} C) and I_S is the reverse saturation current derived from the straight line intercept of the current at zero bias given by Eq. (3)

$$I_S = AA^* T^2 \exp \left(\frac{-q\phi_B}{k_B T} \right) \quad (3.3)$$

Where A is the diode area and A^* is the effective Richardson constant ($28.86 \text{ A.cm}^{-2}.\text{K}^{-2}$ for $\text{Al}_{0.18}\text{Ga}_{0.82}\text{N}$) that can be given in an experimental way by measuring the current as a function of the temperature and in theoretical way according to Eq. (4),

$$A^* = \frac{4\pi m_e^* q k_B^2}{h^3} \quad (3.4)$$

Where m_e^* is the effective mass for $\text{Al}_{0.18}\text{Ga}_{0.82}\text{N}$ ($m_e^* = 2.184 \times 10^{-31}$ kg), calculated by the following formula where m_0 is the electron effective mass,

$$m_{e,\text{AlGa}}^*(x) = (0.22 + 0.13x)m_0 \text{ [Arnaud 2005]}, \quad m_0 = 9.1 \cdot 10^{-31} \text{ kg}$$

h is Planck's constant ($h = 6.62 \times 10^{-34}$ J.s) and Φ_B is the effective barrier height from the metal to the semiconductor. From equations (1) and (2), the barrier height, Φ_B , and the ideality factor, n , can be written respectively as,

$$\phi_B = \frac{k_B T}{q} \ln \left(\frac{AA^* T^2}{I_S} \right) \quad (3.5)$$

$$n = \frac{q}{k_B T} \left(\frac{dV_{GS}}{d(\ln I_G)} \right) \quad (3.6)$$

With $V_T = \frac{k_B T}{q}$ is the thermal potential. $V_T = 25.8mV @ 300K$.

The relationship between the gate current I_G and temperature in order to verify the thermionic mechanism is obtained by matching equations (2) and (3):

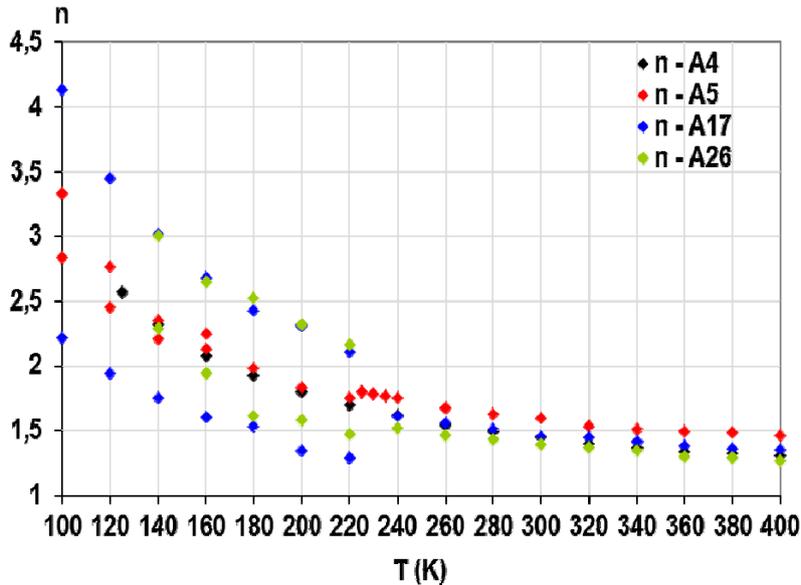
$$I_G = AA^* T^2 \exp\left(\frac{-q\phi_B}{k_B T}\right) \exp\left(\frac{qV_{GS}}{nk_B T}\right) \rightarrow I_G = AA^* T^2 \exp\left(\frac{q(V_{GS} - n\phi_B)}{nk_B T}\right) \quad (3.7)$$

$$\ln\left(\frac{I_G}{T^2}\right) = \frac{q(V_{GS} - n\phi_B)}{nk_B T} + \ln(AA^*) \quad (3.8)$$

Extracting I_S from the linear part of the $\log(I) - V$ plot in forward bias, a Richardson plot can be created by plotting $\ln(I_S/AA^* T^2)$ versus $1/kT$. The linear behavior means that TE is the dominant process throughout the temperature range of the measurements and that Φ_B does not depend on the voltage bias

$$\ln\left(\frac{I_S}{AA^* T^2}\right) = \frac{-q\phi_B}{k_B T} \rightarrow \ln\left(\frac{I_S}{AT^2}\right) = \frac{-q\phi_B}{k_B T} + \ln A^* \quad (3.9)$$

The ideality factor and the Schottky barrier height were extracted as a function of temperature in forward bias mode as showed in figure 29. The ideality factor is about 1.5 from 240K to 400K for all devices. This means that another mechanism adds up to the thermionic mechanism. At low temperatures, the double barrier model allows to extract two values of the ideality factor and the barrier height for three components out of four. On the contrary, the gate-source/drain diode of the “NL” A4 device is correctly modelled by a unique barrier in the whole temperature range.



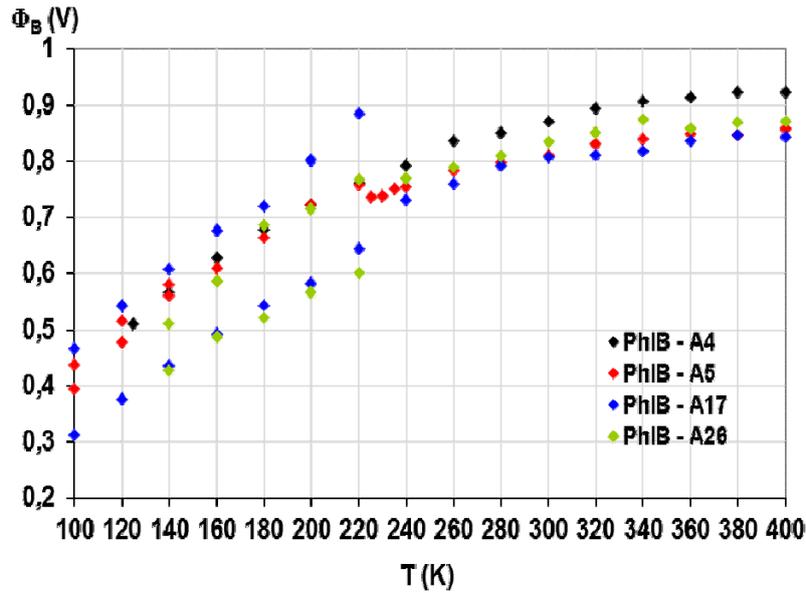


Figure 29. The ideality factor n and the Schottky barrier height Φ_B evolution with temperature for A4, A5, A17 and A26.

The DC I-V characteristics in reverse mode show that the gate leakage current of the “L” devices is higher than the “NL” ones (figure 30).

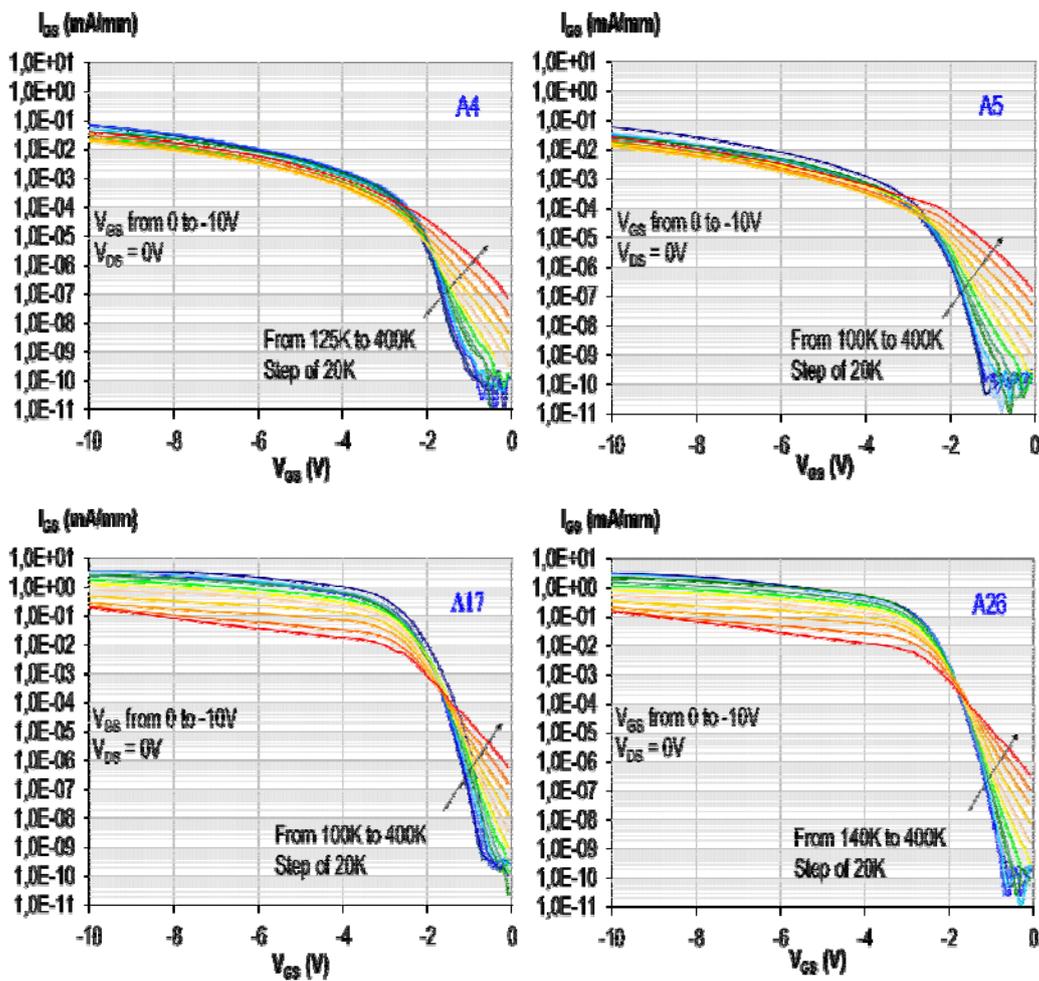


Figure 30. I_G - V_{GS} at $V_{DS} = 0V$ in reverse bias for A4, A5, A17 and A26 from 100K to 400K

The evolution with temperature is similar for $-2V < V_{GS} < 0V$ for NL and L devices and correspond to the thermionic mechanism. For V_{GS} below $-2V$, which is nearly the transistor threshold voltage, there is a change in the evolution of the current that is inversed with temperature.

Given the large barrier heights typical for Schottky contacts to GaN and $Al_xGa_{1-x}N$, we assume that thermionic emission over the Schottky barrier makes only a negligible contribution to reverse-bias current flow. When the reverse-bias leakage current is nearly nondependent on temperature, it suggests that tunneling is the dominant mechanism of current flow. As the electric-field profile within the AlGaN/GaN HFET structure differs from that in a conventional Schottky contact to an n-type semiconductor, we describe the current density as a function of the electric field in the barrier, which is then calculated as a function of bias voltage [Turuvekere 2013]. In this approach, the current density is given by the Fowler-Nordheim tunneling expression,

$$J_{FN} = AE_b^2 \exp\left(-\frac{B}{E_b}\right) \quad (3.10)$$

$$A = \frac{q^2(m_0/m_e^*)}{8\pi\hbar\phi_B} = 1.54 \times 10^{-6} \frac{(m_0/m_e^*)}{\phi_B} \left(\frac{A}{V^2}\right) \quad (3.11)$$

$$B = \frac{8\pi\sqrt{2m_e^*(q\phi_B)^3}}{3qh} = 6.83 \times 10^7 \sqrt{(m_e^*/m_0)(q\phi_B)^3} \left(\frac{V}{cm}\right) \quad (3.12)$$

Where E_b is the electric field in the semiconductor barrier, it depends on the 2DEG density in function of the applied bias V . The relation between $n(V)$ and E_b is derived from solving Poisson's equation,

$$E_b = \frac{q(\sigma - n(V))}{\epsilon_0\epsilon_r} \quad (3.13)$$

$$\sigma(x) = P_{PS,GaN} - (P_{PS,Al_xGa_{1-x}N} + P_{PZ,Al_xGa_{1-x}N}) \quad (3.14)$$

$$P_{PS,Al_xGa_{1-x}N}(x) = -0.052x - 0.029(C/m^2) \quad (3.15)$$

$$P_{PZ,Al_xGa_{1-x}N}(x) = [-0.0525x + 0.0282x(1-x)](C/m^2) \quad (3.16)$$

Where $n(V)$ is the 2-DEG concentration at the hetero-interface and σ is the bound charge at the hetero-interface, which is the sum of the piezoelectric polarization charge in the barrier and the difference between spontaneous polarization charge in the barrier and the buffer.

From Eq. (9), according to Fowler Nordheim tunnelling model, the slope of $\log\frac{J_{FN}}{E_b^2}$ vs.

$\frac{1}{E_b}$ should be nondependent on temperature and proportional to $\sqrt{m_e^*\phi_B^3}$.

$$\ln\left(\frac{J_{FN}}{E_b^2}\right) = -\frac{B}{E_b} + \ln A \quad (3.17)$$

However, the observed dependence of the current densities on electric field and their very weak dependence on temperature indicate that tunneling is in fact, the dominant mechanism of current transport at low temperatures.

In case of current density depends on both electric field and temperature, we observe a linear dependence of $\log \frac{J}{E_b}$ on $\sqrt{E_b}$, where J is the current density and E_b electric field at semiconductor surface. J would increase rapidly with increasing temperature. The transport model that would satisfy these criteria among others would be Poole-Frenkel emission. This mechanism refers to electric-field-enhanced thermal emission from a trap state into a continuum of electronic states. The current density associated with Frenkel-Poole emission is given by

$$J_{PF} = CE_b \exp\left[-\frac{q\left(\phi_t - \sqrt{\frac{qE_b}{\pi\epsilon_0\epsilon_r}}\right)}{k_B T}\right] \quad (3.18)$$

Where E_b is the electric field in the semiconductor barrier at the metal-semiconductor interface, Φ_t is the barrier height for electron emission from the trap state, ϵ_r is the relative dielectric permittivity at high frequency, T is temperature, ϵ_0 is the permittivity of free space, and k_B is Boltzmann's constant. Because the electrons emitted from the trap states do not polarize the surrounding atoms, the relevant dielectric constant is that at high frequency, rather than the static dielectric constant.

$$\epsilon_r = \epsilon_{GaN} + 0.5\chi \quad (3.19)$$

From eq. (16) we see that, for current transport by Frenkel-Poole emission $\log \frac{J}{E_b}$ should be a linear function of $\sqrt{E_b}$, i.e.

$$\ln\left(\frac{J_{PF}}{E_b}\right) = \frac{q}{kT} \sqrt{\frac{qE_b}{\pi\epsilon_0\epsilon_r}} - \frac{q\phi_t}{k_B T} + \ln C = K(T)\sqrt{E_b} + L(T) \quad (18)$$

$$K(T) = \frac{q}{kT} \sqrt{\frac{q}{\pi\epsilon_0\epsilon_r}} \quad (3.20)$$

$$L(T) = -\frac{q\phi_t}{k_B T} + \ln C \quad (3.21)$$

3.1.2.2 HEMT characteristics: $I_{DS} - V_{DS}$

Figure 31 shows I_D versus V_{DS} at $V_{GS} = 0V$ for A4 and A5 (non-leaky devices) and A17 (leaky device) for temperature range 100K – 400K. The devices A5 and 17 have the same DC output power for all studied temperatures on the contrary to A4 that has less output power.

The drain current decreases with temperature and the static resistance R_{DS} in ohmic regime increases with temperature for all devices.

Although A5 and A17 have different leakage current values, they have the same DC output power. Therefore, it can be supposed that the leakage path is not located in the channel.

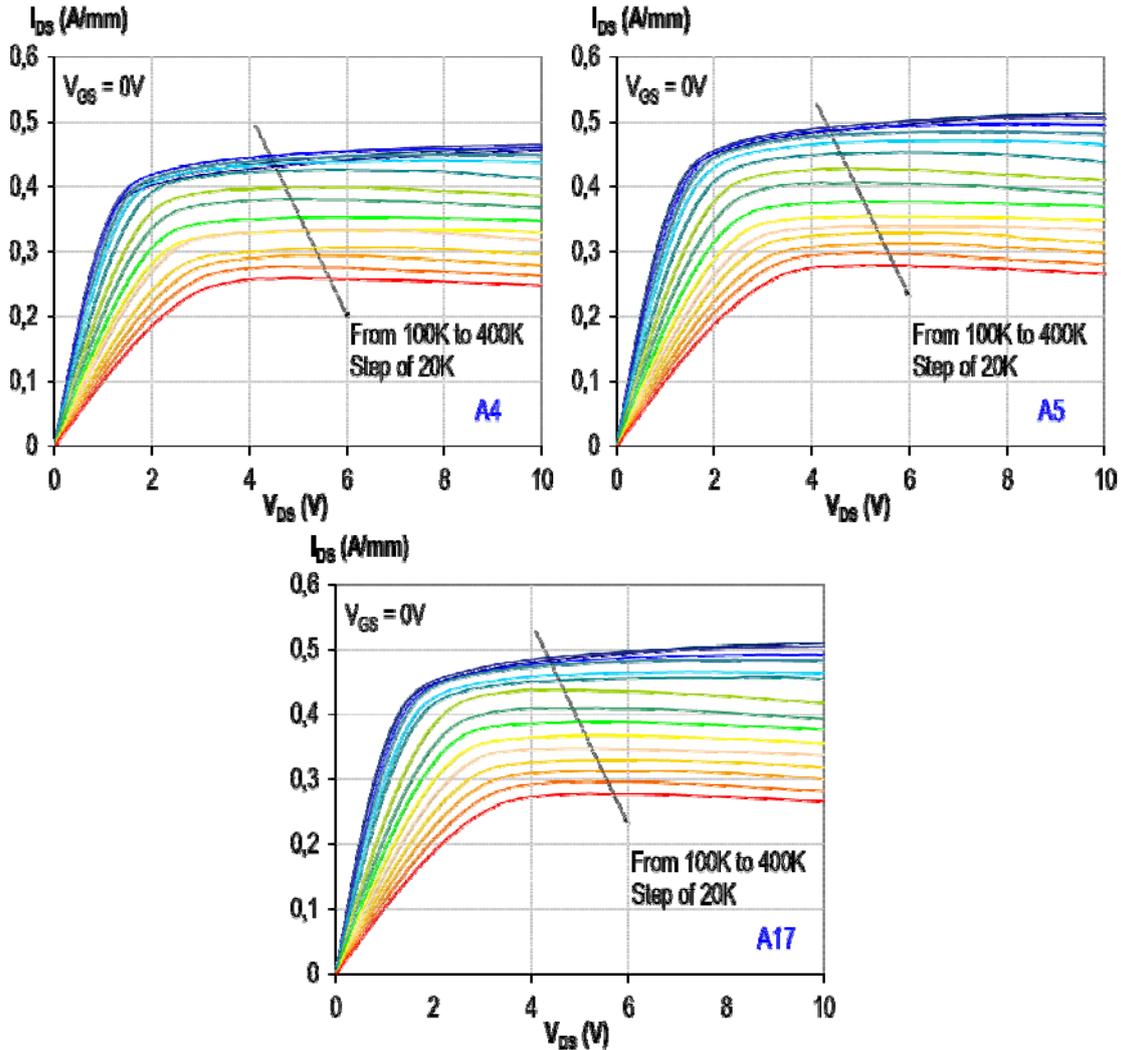


Figure 31. I_{DS} - V_{DS} measurements at $V_{GS} = 0V$ for A4, A5 and A17 for temperature from 100K to 400K

Moreover, the extracted static resistance in ohmic regime R_{DS} at $V_{GS} = 0V$ and V_{DS} from 0V to 0.4V with temperature is shown in figure 32. The evolution of R_{DS} with temperature is superimposed for “NL” and “L” devices. Hence, it is confirmed that the leakage path is not located in the channel.

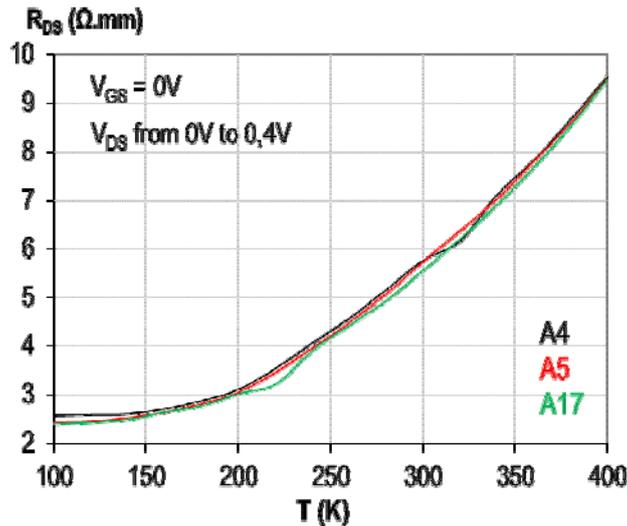


Figure 32. R_{DS} versus temperature for A4, A5 and A17 in ohmic regime at $V_{GS} = 0V$ and V_{DS} from 0V to 0.4V

Figure 33 shows the transistor gate current as a function of the gate-source voltage V_{GS} at a drain-source voltage V_{DS} of 1V for a typical non-leaky HEMT and a typical leaky one issued from the same wafer for temperature range 300K - 400K.

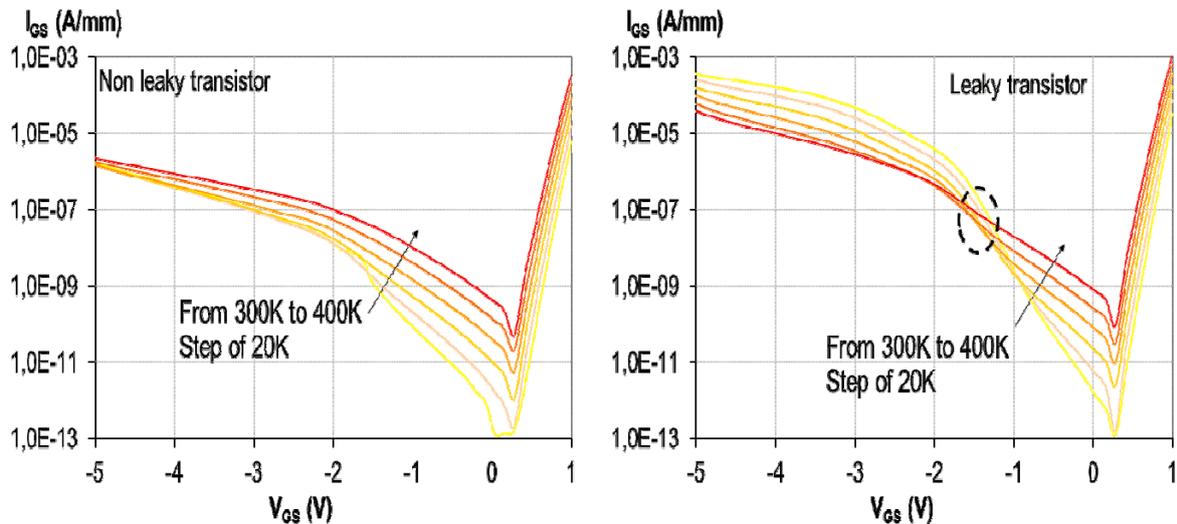


Figure 33. DC gate current versus V_{GS} characteristics at $V_{DS} = 1V$ for a non-leaky transistor and a leaky one for temperature range 300-400K

The temperature dependence of the forward gate current is approximately similar for both representative devices. The reverse gate current of the non-leaky transistor increases with temperature as was reported by some authors [Hashizume 2004] [Sathaiya 2006] and it is reported as the normal temperature dependence of reverse gate leakage current in AlGaIn/GaN HEMTs [Kaushik 2013]. The reverse gate current dependence on temperature for the leaky transistor is different below $V_{GS} = -2V$. Indeed, the transistor threshold voltage is about -2V. This inverse temperature dependence of the reverse gate current with temperature has also been reported in [Lu 2008] [Hasegawa 2009] [Ha 2012] and explained in [Kaushik 2013] using a virtual gate-trap-assisted tunneling model that assumes the presence of defect states at the AlGaIn/SiN interface close to gate metal and bulk traps in the AlGaIn layer of the HEMT.

Figure 34 shows the static drain current as a function of the gate-source voltage V_{GS} at a drain-source voltage V_{DS} of 1V for non-leaky and leaky transistors for temperature range 300K - 400K. The transfer characteristics of the non-leaky and the leaky transistors are similar above $V_{GS} = -2V$ and we notice a curve cross at about $V_{GS} = -1.6V$; it corresponds to the expected evolution with temperature of the threshold voltage. Hence, the threshold voltage of the studied devices is about $V_{GS} = -2V$. In subthreshold regime, the drain current of the non-leaky transistor increases with temperature which is considered to be normal.

On the contrary, for the leaky transistor a second curve cross occurs at $V_{GS} = -2.6V$ showing an inverse temperature dependence of the drain leakage current as observed for the gate leakage current. Interestingly, it is observed an increase of the drain leakage current in subthreshold regime while V_{GS} is more negative. It was reported in [Bahat-Treidel 2012] that there are two dominant subthreshold leakage current mechanisms: the bulk subthreshold leakage current and the Schottky-gate reverse bias tunneling leakage current.

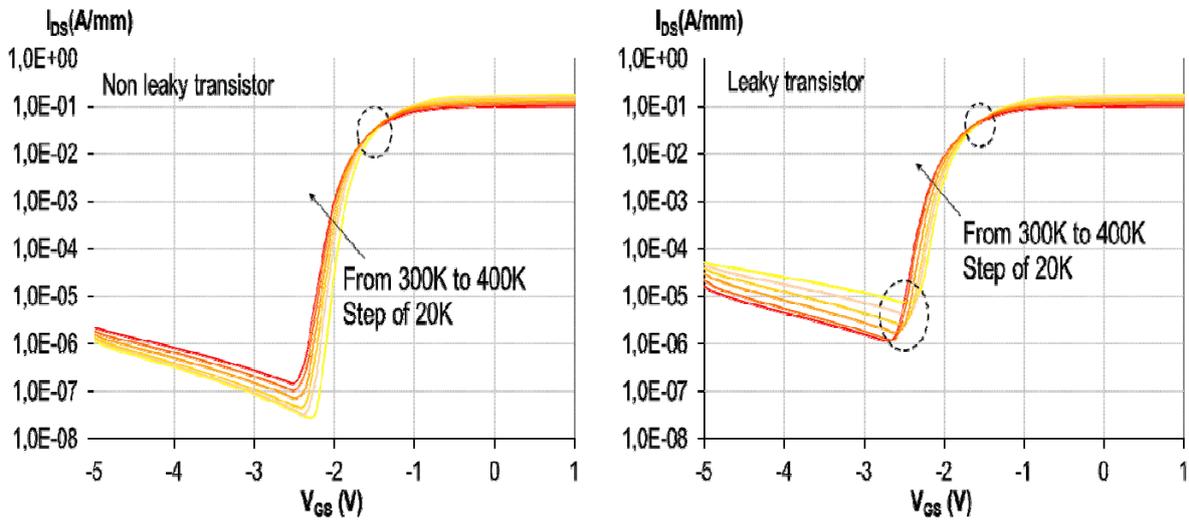


Figure 34. DC drain current versus V_{GS} characteristics at $V_{DS} = 1V$ for a non-leaky transistor and a leaky one for temperature range 300-400K

Figure 35 shows the evolution of the drain leakage current I_{DS} as a function of the temperature from 100K to 400K at $V_{DS} = 1V$ and $V_{GS} = -3V, -2V, -1V$ and $1V$.

At $V_{GS} = -3V$, in subthreshold regime (as the threshold voltage is $V_{TH} = -2V$), the leakage current of the HEMT I_{DS} is negligible for A4 and A5 devices compared to the one of A17. At $V_{GS} = -2V$, a value near the threshold voltage, the leakage currents I_{DS} of A5 and A17 are equal and weakly higher than the one of A4 which threshold voltage is $-1.7V$.

At $V_{GS} = -1V$, the channel is open and the drain current has the same evolution for all devices. When the channel is open and for example at $V_{GS} = 1V$, the drain current is superimposed for all devices.

These results show that the main difference between AlGaIn/GaN HEMTs with different leakage current occurs at subthreshold regime for $V_{GS} < V_{TH}$. Note that V_{TH} at $I_{DS} = 1\% I_{DSPLS}$ (I_{DS} at $V_{GS} = 1V$ and $V_{DS} = 10V$) is $-2.0V$ for A4, $-2.3V$ for A5 and $-2.2V$ for A17.

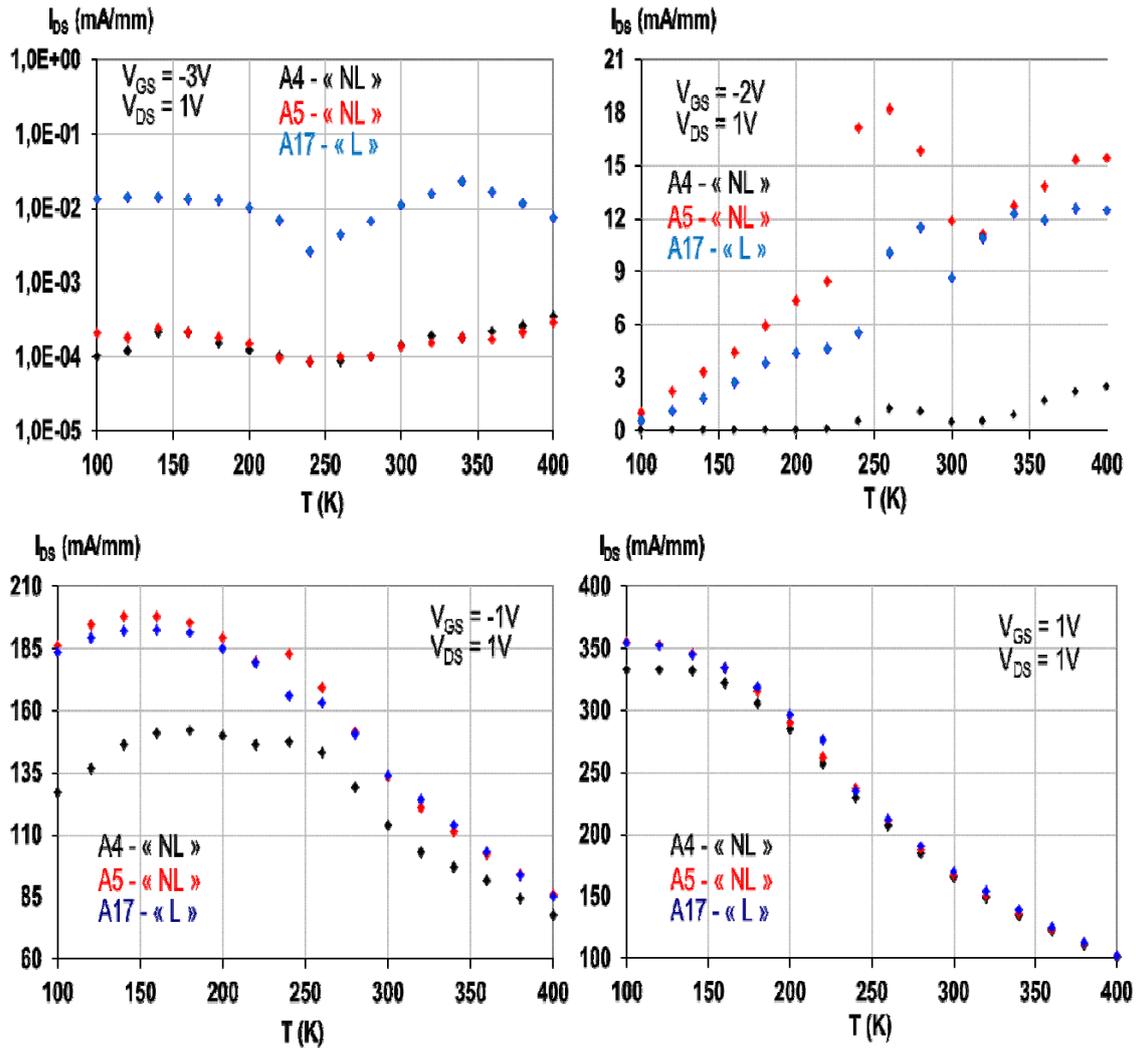


Figure 35. I_{DS} versus temperature at $V_{DS} = 1V$ for $V_{GS} = -3V, -2V, -1V$ and $1V$ for A4, A5 and A17 for 100K – 400K temperature range (note that V_{TH} at $I_{DS} = 1\% I_{DSPLS}$ is $-2.0V$ for A4, $-2.3V$ for A5 and $-2.2V$ for A17)

Figure 36 shows the comparison of the gate and drain leakage currents at subthreshold regime for non-leaky and leaky devices for 120K – 400K temperature range.

The gate and drain leakage currents for the non-leaky transistors decrease from 120K to 240K and increase from 260K to 400K. At $V_{GS} = -3V$, the gate and the drain leakage currents are equal, but more V_{GS} becomes negative, higher the difference between the drain and the gate leakage currents while having the same evolution with temperature.

For the leaky transistor, the gate and the drain leakage currents decrease with temperature in the whole range. There is a large difference between the gate and drain leakage currents unlike for the non-leaky devices. A deep insight analysis should be focused in the range of temperature where the two devices have different dependences with temperature from 300K to 400K.

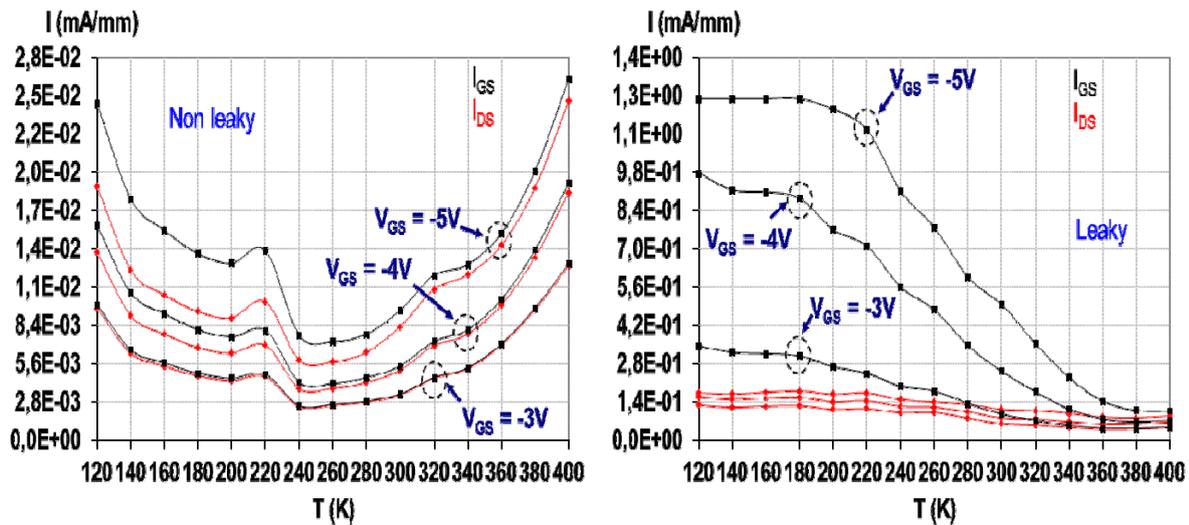
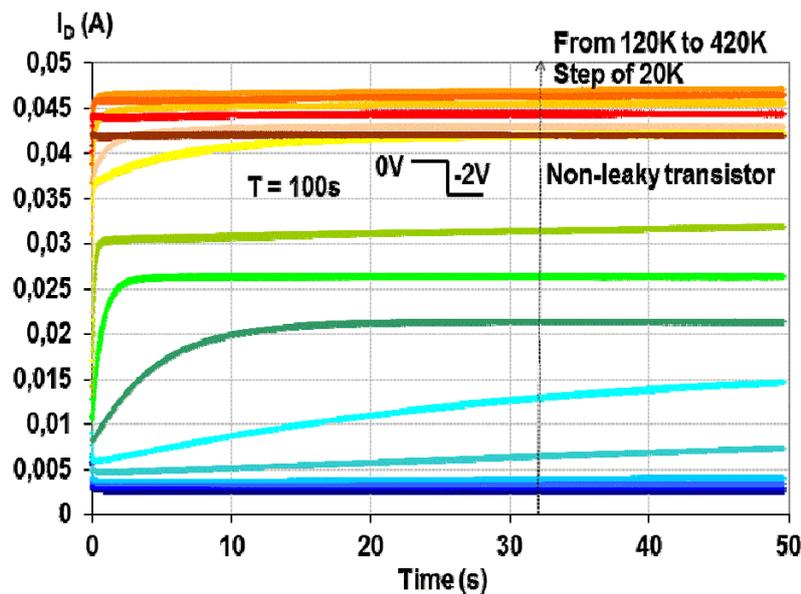


Figure 36. I_{DS} & $I_{GS} = f(V_{DS})$ measurements at $V_{DS} = 8V$ at subthreshold voltage ($V_{GS} = -3V, -4V$ and $-5V$) for non-leaky and leaky AlGaIn/GaN HEMTs for temperature range 100K-400K

3.1.3 Traps characterization

The drain current transient evolution is presented in Figure 37 from 120K to 400K for non-leaky and leaky transistors. The period of the gate-source voltage pulse is of 100 s and its duty cycle of 50%. As we intend to study the trapping effects independently of the thermal ones, we measure isothermal transients of the drain leakage currents; the pulse is defined from 0 to V_{GS} lower than the threshold voltage of the transistor, namely $-2V$. The drain current transients of the leaky and non-leaky devices present emission and capture processes depending on the temperature range.



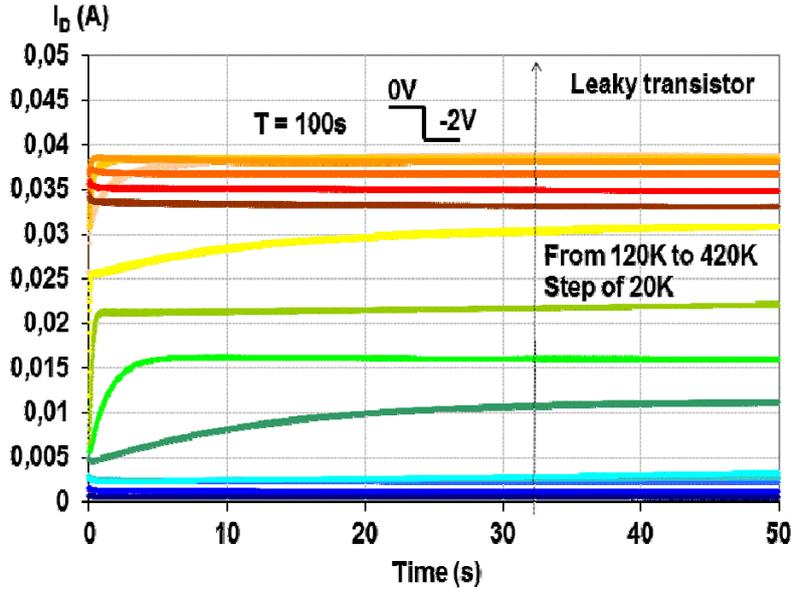


Figure 37. Drain current transients for a period of 100s for V_{GS} pulse from 0V to -2V from 120K to 400K for a non-leaky and a leaky AlGaIn/GaN HEMTs

The drain current transients amplitudes are higher for the non-leaky devices than for the leaky ones for all the temperature range but their evolution with temperature showing emission or capture processes are similar for all devices. Electron capture process occurs from 120K to 180K, while a transition from electron capture to emission occurs between 200K and 220K. An electron emission process is clearly detected from 240K to 340K for the leaky device while it continues until 360K for the non-leaky device. A capture process appears for the leaky devices from 360K to 420K while it is not so visible for the non-leaky ones.

The transients are then decomposed into a sum of exponential components as follows:

$$I_D = I_0 + \sum_{i=1}^m a_i e^{-\frac{t}{\tau_i}} \quad (3.22)$$

With I_0 the current value at equilibrium state, τ_i the time constant and a_i the amplitude associated to each detected trap. For emission traps, the traps signature is identified from the time emission constant $\tau_i = 1/e_n$ as a function of temperature.

The probability of emission (e_n) of electrons by traps is given by the following expression [Saysset 1996]:

$$e_n = v_n \sigma_n N_C e^{\frac{-E_a}{k_B T}} \quad (3.23)$$

Where T is the temperature, σ_n the trap cross-section, N_C the effective state density in the conduction band given by equation (3) and v_n the thermal velocity of electrons expressed by equation (4).

$$N_C = 2 \left(\frac{2\pi m_e^* k_B T}{h^2} \right)^{\frac{3}{2}} \quad (3.24)$$

$$v_n = \sqrt{\frac{3kT}{m_e^*}} \quad (3.25)$$

m_e^* is the electron effective mass, k_B the Boltzmann constant and h the Planck constant.

The equation (1) is used to fit the emission and/or capture kinetics at each temperature. The amplitude a_i of each exponential component decreases with temperature while its time emission/capture constant τ_i increases.

Figure 38 shows the Arrhenius plots of $\tau_i.T^2$ versus $1000/T$ obtained from DCTS measurements carried out on a non-leaky transistor (A5) and a leaky one (A17). For the calculation of the cross-section, we use the effective mass of the AlGaN layer assuming that all traps are located in this layer for a comparison purpose.

In order to get correlation with the trapping effects responsible for the positive and negative temperature dependences of the reverse gate current which occur in the temperature range of 300K-400K, we have focused the result extraction in this temperature range in the analysis of the Arrhenius plots.

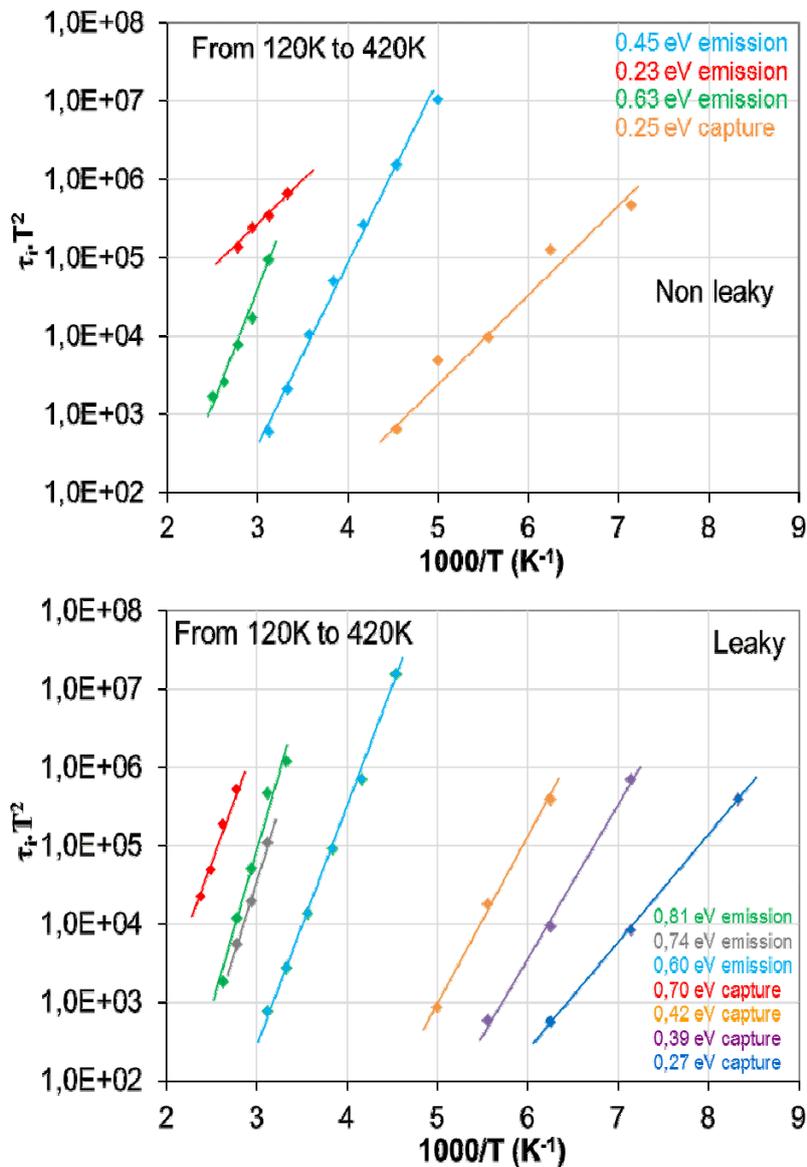


Figure 38. Drain current transients for a period of 100s for V_{GS} pulse from 0V to -2V from 120K to 400K for a non-leaky and a leaky AlGaN/GaN HEMTs

For the non-leaky transistor, these plots point out the presence of two prominent emission trap levels with activation energy of 0.45 ± 0.04 eV and 0.63 ± 0.05 eV and respective cross section of 1.43×10^{-19} cm² and 3.19×10^{-16} cm².

For the leaky transistor, a capture process with activation energy of 0.70 eV and cross section of 2.13×10^{-15} cm² is identified in addition to the emission mechanisms; these emission mechanisms are characterized by two traps with activation energy of 0.81 ± 0.02 eV and 0.74 ± 0.02 eV and respective cross section of 1.28×10^{-13} cm² and 2.55×10^{-15} cm².

Numerous trapping/detrapping mechanisms have been previously reported by other authors. Traps with activation energy around 0.5 eV were identified in [Sozza 2005] for stressed and unstressed samples suggesting the same physical origin and were associated with surface traps. It was reported in [Mizutani 2003] that traps with activation energy of 0.6 eV correspond to electron traps originating from a defect level located in the GaN layer.

Trapping process having an activation energy of about 0.74 eV in the temperature range of 340K-380K has been reported in [Joh 2011] and associated to electron injection from the gate and trapping either inside the AlGaN layer or at the surface close to the gate. This mechanism might correspond to the capture process that we have only identified in the leaky transistor and in the temperature range of 340K-380K. The same authors have also reported on detrapping process from the AlGaN barrier exhibiting activation energy of 0.57 eV. This type of emission traps has been found in this study for the non-leaky transistor.

3.1.4 Pulsed I-V characteristics

The pulsed I-V measurements are carried out at different quiescent bias (QB) conditions (V_{GS0} , V_{DS0}) in order to quantify the gate and drain lag phenomena. The waveforms $V_{DS}(t)$ and $I_{DS}(t)$ are extracted to verify the stability of the quiescent and instantaneous biases of the transistor; as a consequence, it is ensured that instantaneous measurements are performed in the time window within which $V_{DS}(t)$ and $I_{DS}(t)$ are stable. A pulse width PW1 of 0.3μs and PW2 of 10μs are used to study the influence of this parameter on the lag phenomena and on the dynamic resistance (R_{ON}). A duty cycle of 10% is fixed for the two pulse width conditions.

Figure 39 shows I_{DS} - V_{DS} 0.3μs pulsed characteristic of a non-leaky HEMT (A4) using the quiescent bias conditions (V_{GS0} , V_{DS0}) = (0V, 0V) and (-7V, 0V) and figure 41 shows its I_{DS} - V_{DS} 0.3μs pulsed characteristic using the quiescent bias conditions (V_{GS0} , V_{DS0}) = (-7V, 30V) and (-7V, 50V). Figures 40 and 42 show $I_{DS}(t)$ waveforms of four chosen points A, B, C and D corresponding to different values of instantaneous measurement conditions V_{GSi} and V_{DSi} . For a pulse width of 0.3μs, the quiescent bias measurement is done from 50 ns to 150 ns and the instantaneous drain current is measured from 350 ns to 450 ns.

Therefore, for the points A, B, C and D, the instantaneous drain current is measured during the pulse in steady state conditions. This verification is necessary to validate the pulsed I-V characteristics of the device under test and the quantification of the gate lag and drain-lag ratios presented below.

Figure 43 shows I_{DS} - V_{DS} 10 μs pulsed characteristic of the same non-leaky HEMT (A4) using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and $(-7V, 0V)$ and figure 44 shows its I_{DS} - V_{DS} 10 μs pulsed characteristic using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (-7V, 30V)$ and $(-7V, 50V)$. As there is no significant difference between the measurements performed with PW of 0.3 and 10 μs , it can be concluded that there is not any activation of new transient effects with time constants between 0.3 μs and 10 μs .

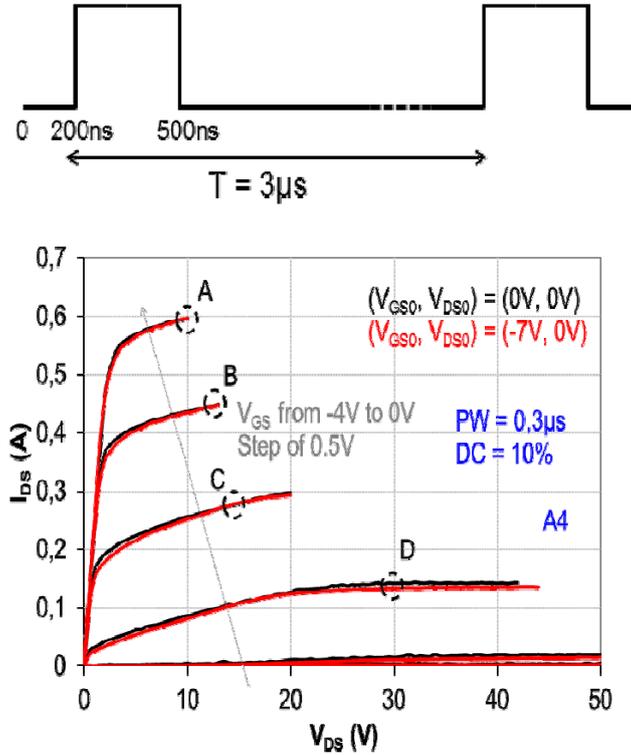
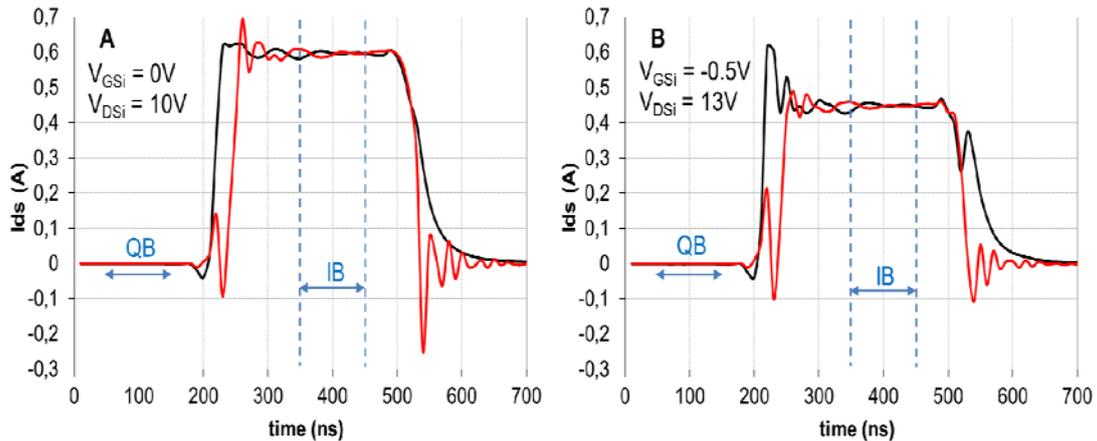


Figure 39. 0.3 μs pulsed I-V measurements of a non-leaky HEMT using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and $(-7V, 0V)$



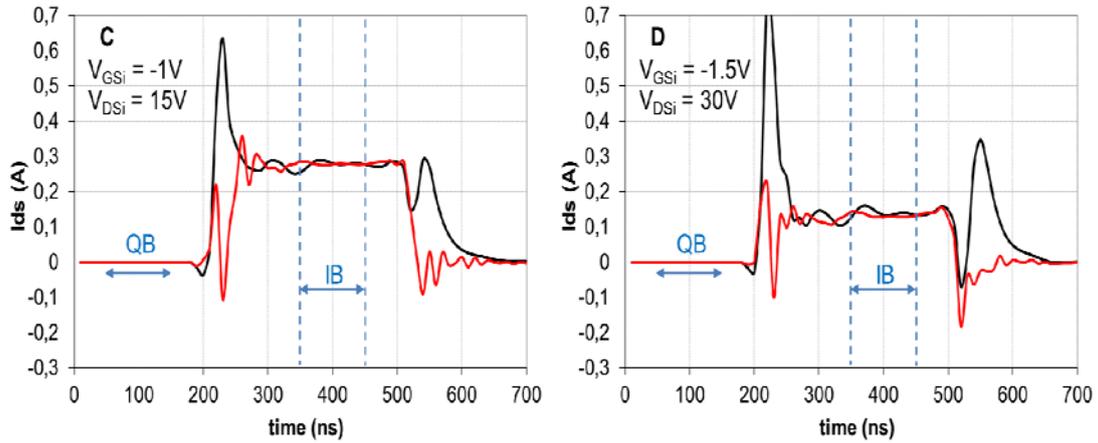


Figure 40. $I_{DS}(t)$ waveforms corresponding to the instantaneous bias points A, B, C and D

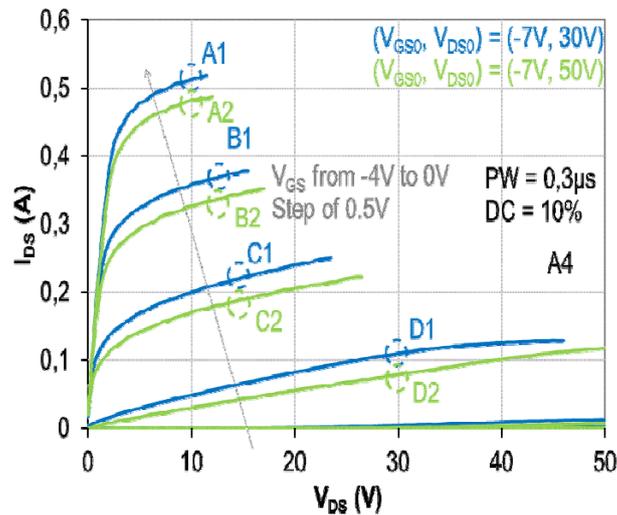
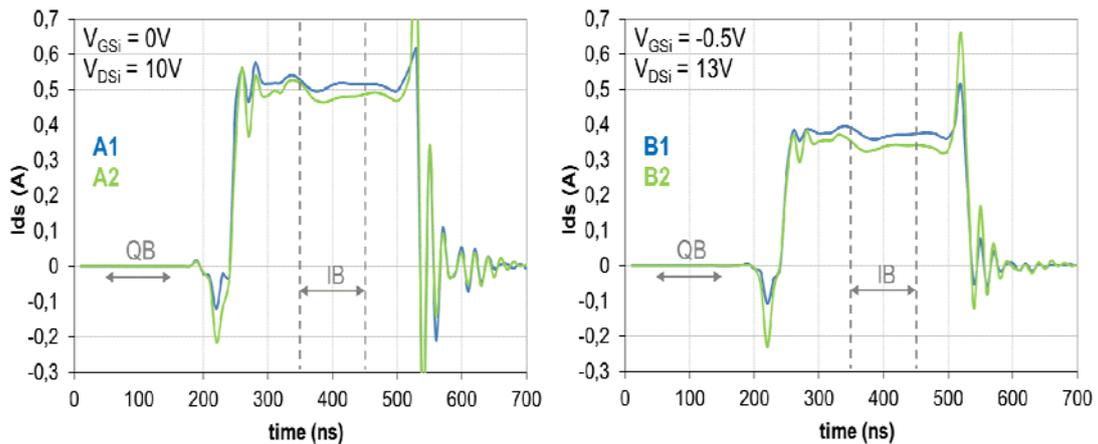


Figure 41. $0.3\mu\text{s}$ pulsed I-V measurements of a non-leaky HEMT using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (-7\text{V}, 30\text{V}), (-7\text{V}, 50\text{V})$



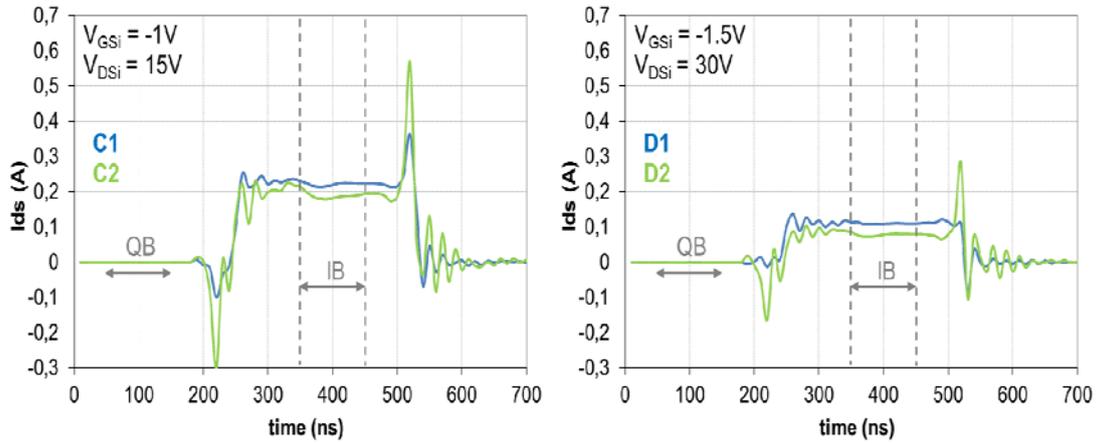


Figure 42. $I_{DS}(t)$ waveforms corresponding to the instantaneous bias points A, B, C and D

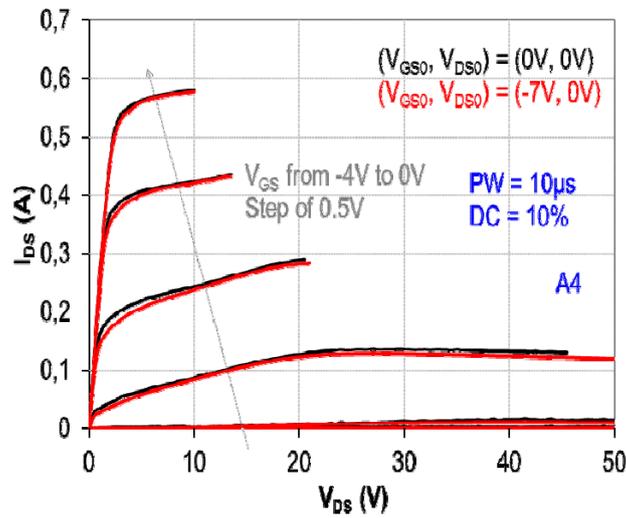


Figure 43. $10\ \mu\text{s}$ pulsed I-V measurements of a non-leaky HEMT using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (0\text{V}, 0\text{V}), (-7\text{V}, 0\text{V})$

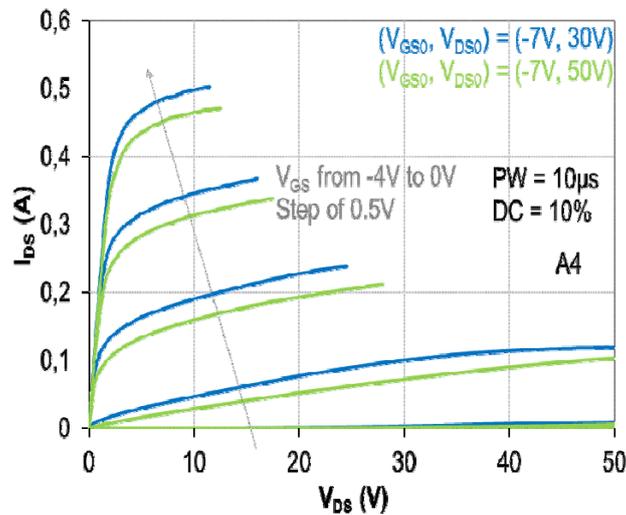


Figure 44. $10\ \mu\text{s}$ pulsed I-V measurements of a non-leaky HEMT using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (-7\text{V}, 30\text{V}), (-7\text{V}, 50\text{V})$

3.1.4.1 Gate-lag effect

The gate-lag (GL) is a delayed response of the drain current with respect to the gate voltage variation. Figure 45 shows 0.3 μ s pulsed I-V measurements of two non-leaky and a leaky HEMTs using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and $(-7V, 0V)$. We notice that the difference between the I-V characteristics for both quiescent bias conditions in all the V_{DS} range is negligible for the non-leaky devices and is more pronounced for the leaky one. As reported in table 2, it is obvious that the non-leaky HEMTs presents a gate-lag ratio lower than the one of the leaky device, which can hamper the large gate voltage variations under class A amplification. This higher gate-lag effect for the leaky device is attributed to traps with time constants higher than 0.3 μ s (that is the pulse width), and lower than the period duration of 3 μ s. A. Nakajima et al [Nakajima 2009] reported that when V_{GS} becomes negative, electrons in the channel can be injected into the buffer layer. These electrons are captured by the deep donors, and hence the gate-lag arises.

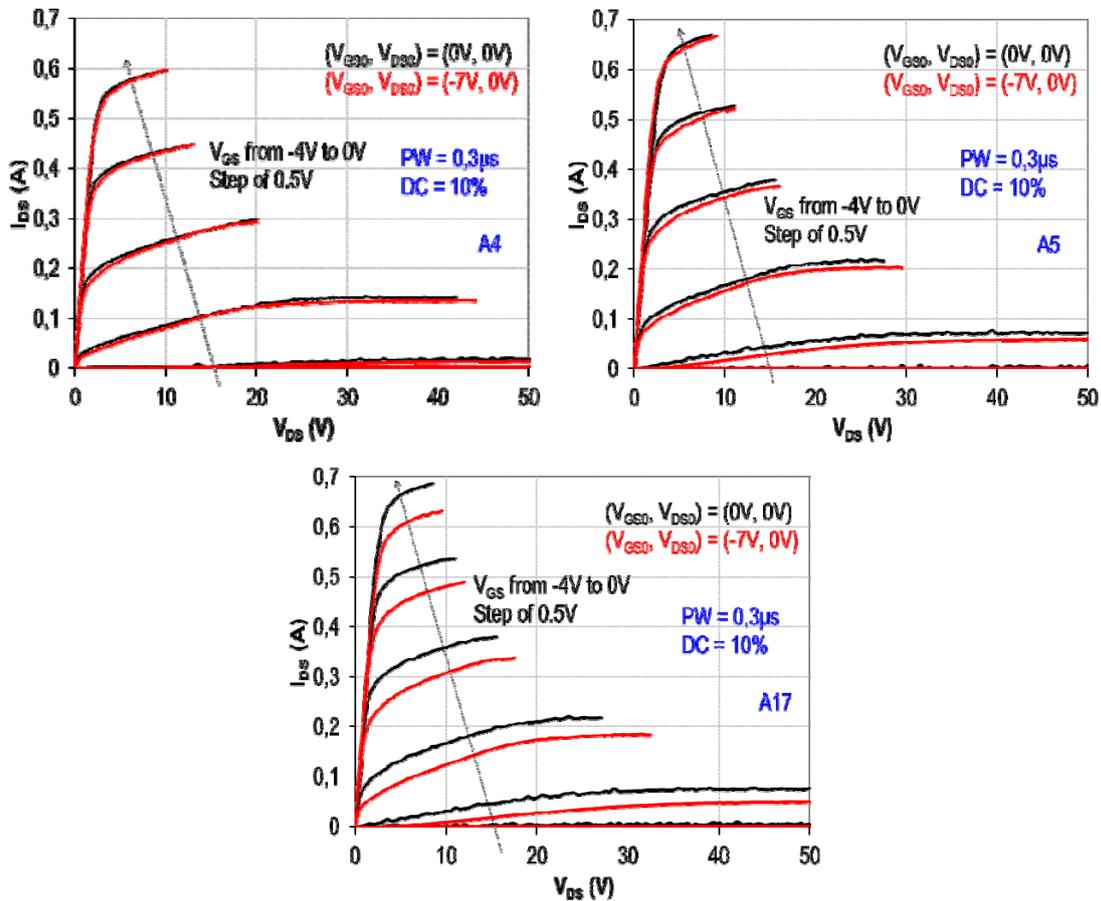


Figure 45. 0.3 μ s pulsed I-V measurements of A4 and A5 (non-leaky HEMTs) and A17 (leaky HEMT) using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (0V, 0V)$ and $(-7V, 0V)$

V_{GS} (V)	GL_A4 (%)	GL_A5 (%)	GL_A17 (%)
-1.5	7.19	7.31	28.78
-1	1.82	4.41	15.06
-0.5	0.53	1.47	10.36
0	0.28	0.95	8.40

Table 2. Gate-lag (GL) rate of A4 and A5 (non-leaky HEMTs) and A17 (leaky HEMT)

3.1.4.2 Drain lag-effect

The drain-lag (DL) is a delayed response of the drain current with respect to the drain voltage variation. Figure 46 shows 0.3 μ s pulsed I-V measurements of two non-leaky and a leaky HEMTs using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (-7V, 30V)$ and $(-7V, 50V)$. Here $\Delta V_{DS0} = 20V$.

We notice that for a constant gate voltage and $\Delta V_{DS0} = 20V$, the non-leaky and the leaky HEMTs present approximately the same evolution of the drain-lag ratio over the V_{DS} measurement range. As reported in table 3, the drain-lag ratio is lower than 10% at $V_{GSi} = 0V$ and is increasing with more negative V_{GS} . Moreover, the magnitude of the drain-lag is approximately identical for the leaky and non-leaky devices as it differs from less than 3% over the V_{DS} and V_{GS} investigated ranges.

Figures 47 and 48 show 0.3 μ s pulsed I-V measurements of two non-leaky and a leaky HEMTs using the quiescent bias conditions respectively:

$(V_{GS0}, V_{DS0}) = (-7V, 0V)$ and $(-7V, 30V)$. Here $\Delta V_{DS0} = 30V$.

$(V_{GS0}, V_{DS0}) = (-7V, 0V)$ and $(-7V, 50V)$. Here $\Delta V_{DS0} = 50V$.

As expected, the drain-lag ratios of leaky and non-leaky HEMTs increase with ΔV_{DS0} and are approximately of the same magnitude for the two sets of devices (tables 4 and 5).

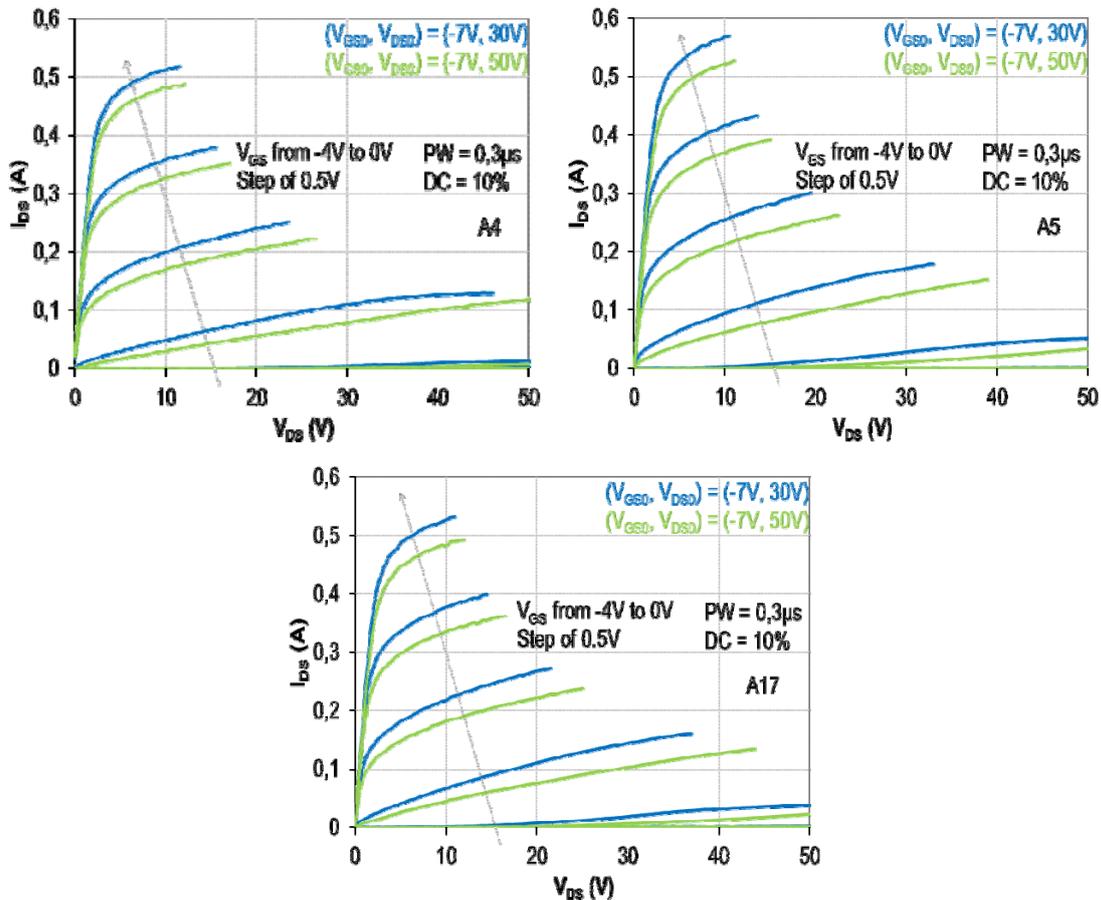


Figure 46. 0.3 μ s pulsed I-V measurements of A4 and A5 (non-leaky HEMTs) and A17 (leaky HEMT) using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (-7V, 30V)$ and $(-7V, 50V)$

V_{GS} (V)	DL_A4 (%)	DL_A5 (%)	DL_A17 (%)
-1.5	38.56	34.70	34.23
-1	15.01	16.81	17.00
-0.5	9.44	10.77	11.28
0	6.24	8.15	7.58

Table 3. Drain-lag (DL) rate of A4 and A5 (non-leaky HEMTs) and A17 (leaky HEMT) for 0.3 μ s pulse and $\Delta V_{DS0} = 20V$

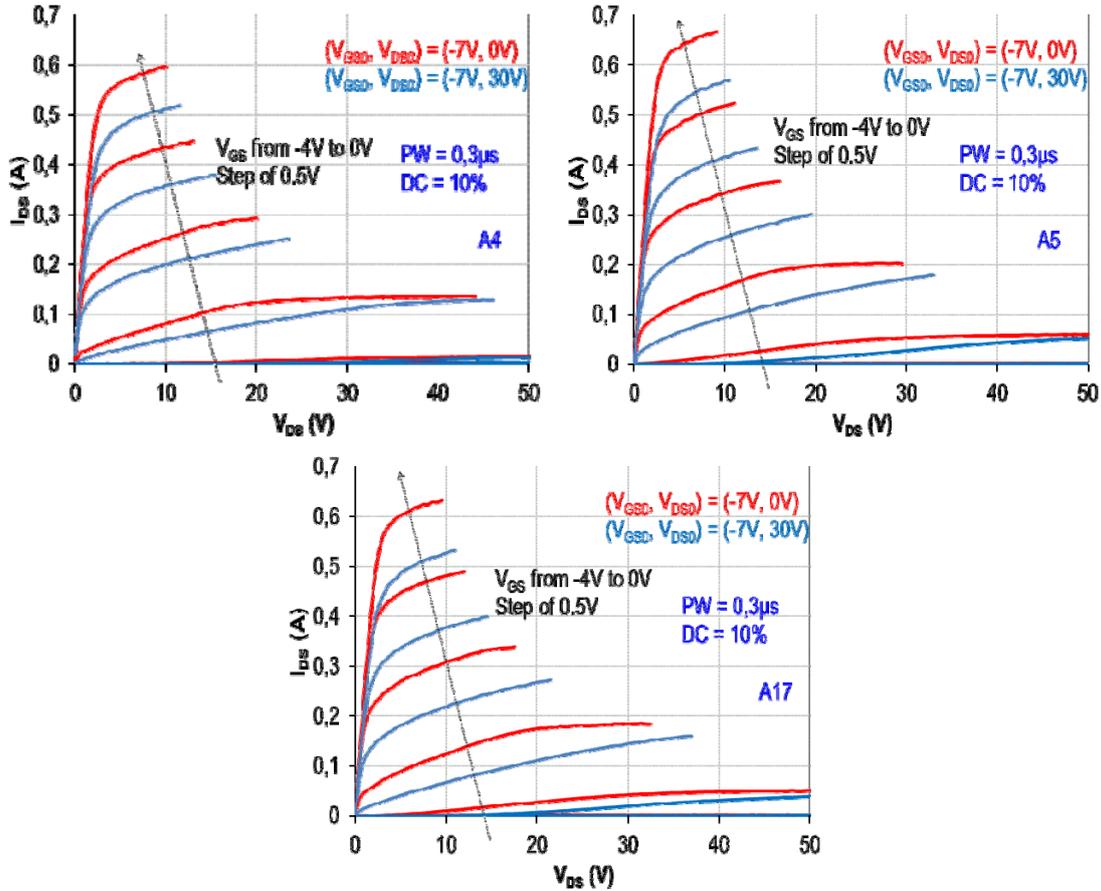


Figure 47. 0.3 μ s pulsed I-V measurements of A4 and A5 (non-leaky HEMTs) and A17 (leaky HEMT) using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (-7V, 0V)$ and $(-7V, 30V)$

V_{GS} (V)	DL_A4 (%)	DL_A5 (%)	DL_A17 (%)
-1.5	40.19	41.07	47.00
-1	20.64	26.53	29.29
-0.5	17.78	20.46	22.24
0	14.28	15.71	17.25

Table 4. Drain-lag (DL) rate of A4 and A5 (non-leaky HEMTs) and A17 (leaky HEMT) for 0.3 μ s pulse and $\Delta V_{DS0} = 30V$

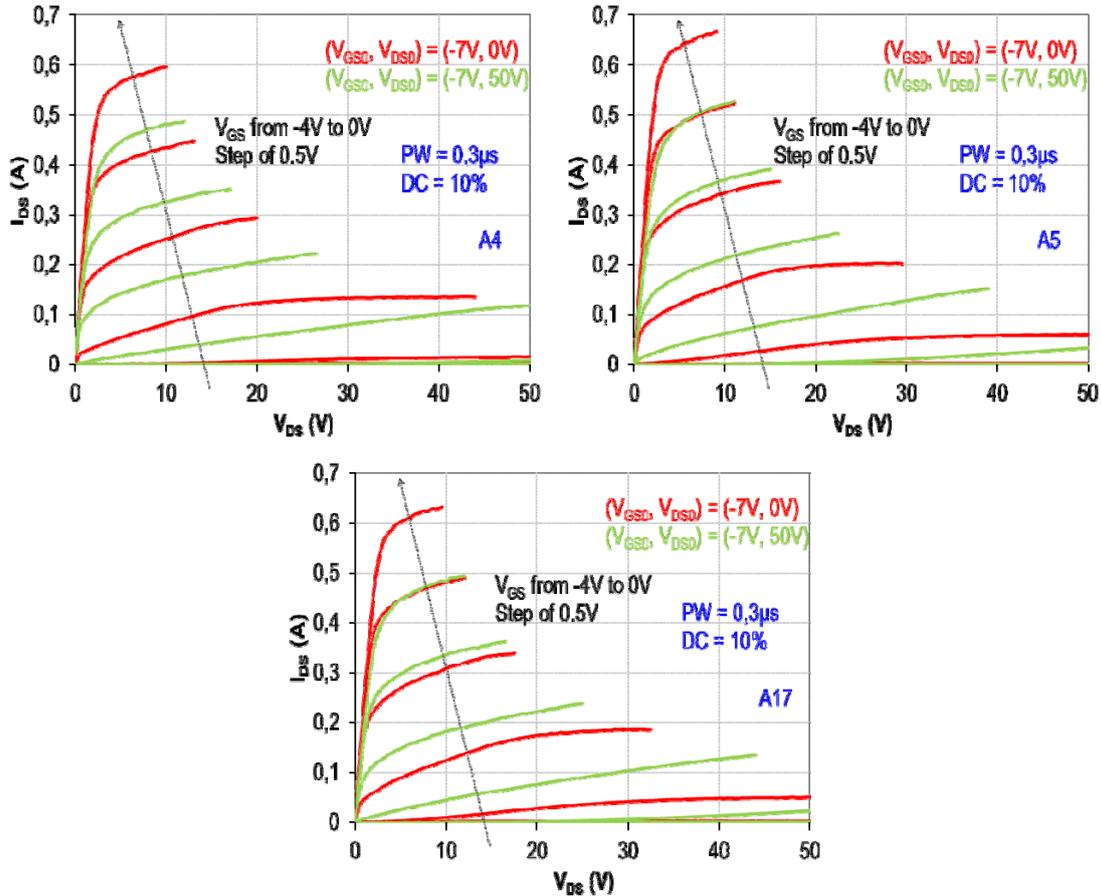


Figure 48. 0.3 μ s pulsed I-V measurements of A4 and A5 (non-leaky HEMTs) and A17 (leaky HEMT) using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (-7V, 0V)$ and $(-7V, 50V)$

V_{GS} (V)	DL_A4 (%)	DL_A5 (%)	DL_A17 (%)
-1.5	63.25	61.52	65.15
-1	32.55	38.88	41.32
-0.5	25.54	29.03	31.01
0	19.63	22.58	23.52

Table 5. Drain-lag (DL) rate of A4 and A5 (non-leaky HEMTs) and A17 (leaky HEMT) for 0.3 μ s pulse and $\Delta V_{DS0} = 50V$

3.1.4.3 Dynamic on-state resistance

The dynamic on-resistance R_{ON} is extracted from the slope of the output characteristic in the linear regime for different pulse widths. Figures 49 and 50 show pulsed I-V measurements of AlGaIn/GaN HEMT with a duty cycle of 10% and a pulse width of 0.3 μ s (black) and 10 μ s (red), respectively for a non-leaky and a leaky device. We notice that there is no current dispersion in ohmic regime and a weak one in saturation regime.

Therefore, the GH50_10 technology does not suffer from dispersion of the dynamic on-resistance which is known to affect high-voltage switching performances. Indeed, the most critical parameter for high voltage switching is the increase of the dynamic on-resistance that can be multifold for high switching frequency. It has been reported in [Würlf 2011] that the

lowest on-state resistance increase is obtained for non-doped buffer structures and that incorporation of high C-concentration in the buffer leads to a pronounced increase of R_{ON} .

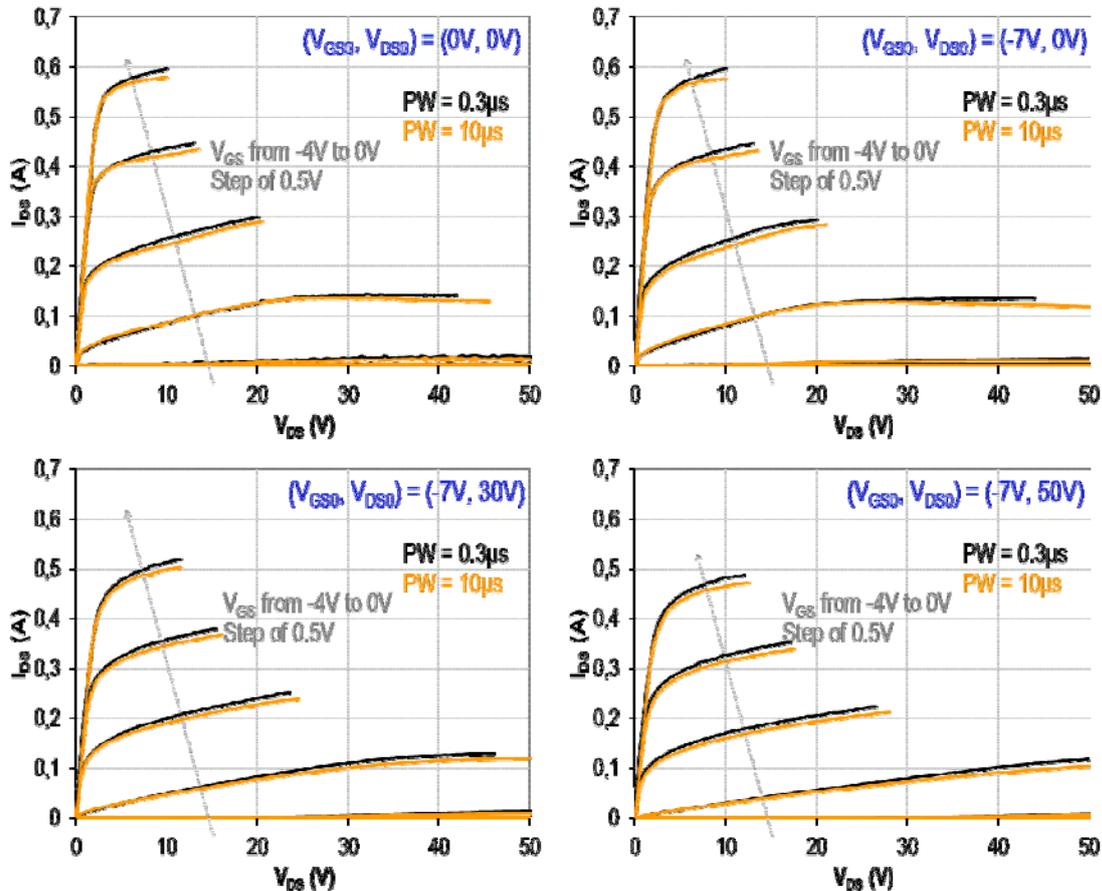


Figure 49. 0.3 μs and 10 μs pulsed I-V measurements of A4 (non-leaky HEMT) using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (0\text{V}, 0\text{V}), (-7\text{V}, 0\text{V}), (-7\text{V}, 30\text{V})$ and $(-7\text{V}, 50\text{V})$

Saito et al. [Saito 2011] investigated different combinations of field plates for GaN based HEMT for high voltage switching. They found that field plate design variations influence the maximum electric field in the device and that devices with non-optimum field plates still allowing for very high internal fields are prone to excessive dynamic on-state resistance increase once the device is operated at high voltage. The increase of dynamic on-state resistance is partly reversible. However, depending on maximum field the device has encountered during stressing, also persistent degradation occurs. This can be attributed to the accumulation of charges with time (under much localized zones where high electrical field occurs), that can recover or not depending on the stress period.

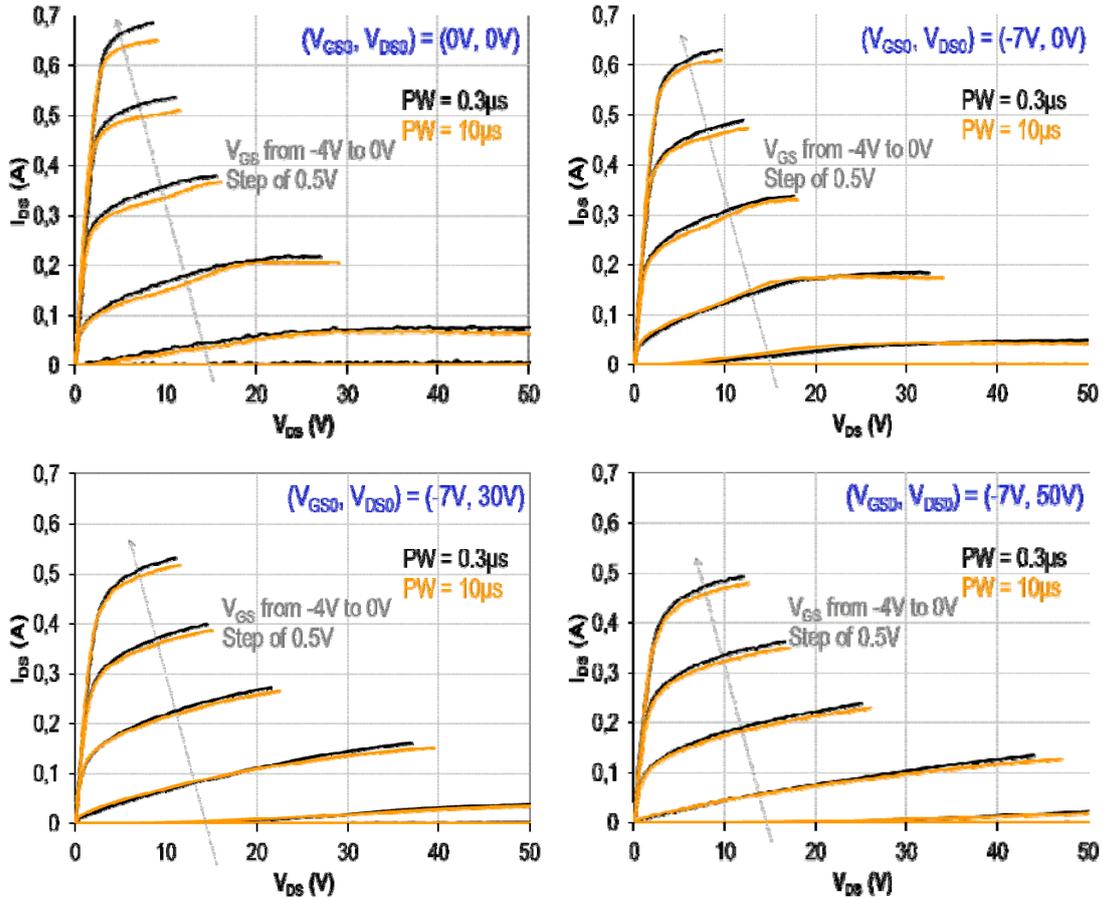


Figure 50. $0.3 \mu s$ and $10 \mu s$ pulsed I-V measurements of A17 (leaky HEMT) using the quiescent bias conditions $(V_{GS0}, V_{DS0}) = (0V, 0V), (-7V, 0V), (-7V, 30V)$ and $(-7V, 50V)$

Würfl et al.[Würfl 2013] have reported that a strong impact of buffer epitaxy on dynamic properties can be seen whereas the influence of the gate technology (normally-off p-GaN gate compared to Schottky gates) is of minor influence. In this comparison, devices with AlGaN buffer layers show the lowest increase in dynamic on-state behavior followed by GaN-on-Si devices with a proprietary buffer design. In contrast, devices with C-doped buffer layers are prone to increase dynamic on-state resistance. On the other hand, C-doped buffer structures show much larger breakdown strength as compared to AlGaN back-barrier design. For a practical device application this means that the required gate-drain distance for a given lateral breakdown voltage is much smaller for C-doped GaN as compared to AlGaN back-barrier buffer structures. Thus, devices fabricated on C-doped buffers show a smaller static on-state resistance. This means that there is a trade-off between the static and the dynamic on-state resistance that has to be considered when optimizing device performance.

In short time scale, the R_{ON} transient is dominated by a temperature independent release of electrons, most likely detrapping through a tunneling process. These traps can be charged in the off-state through the gate current and in the high-power state through hot electrons from the channel.

A most likely origin for these traps that is consistent with all observations is interface states at the AlGaN/AlN interface. This interface is known to harbor interface states. Traps that are physically located inside a barrier but very close to the channel and that release their

electrons through a tunneling process are known as border traps. The longer thermally-activated time transients are associated with conventional traps at the surface or inside the AlGa_N barrier. These are accessible from the gate in the off-state but not from the channel in the high-power state because of the energy barrier associated with the AlGa_N. To some extent, these traps can be engineered through proper growth procedures [Joh 2011].

Conclusion of case study 1: “link” with ReAGaN project

The electrical characterization of the GH50 devices has been performed following a test plan. This is to understand the origin of the high subthreshold leakage current that is one of the major factors still hampering the power performances and the electrical reliability of AlGa_N/Ga_N HEMTs.

Three electrical characterization techniques have been used for this case study: DC, pulsed and drain current transient characterization for a temperature range between 100K and 400K.

The analysis of the gate current in forward bias with temperature showed a unique barrier height for non-leaky “NL” devices unlike the leaky “L” devices for which we noticed a double barrier height at low temperatures. The evolution of gate current in reverse bias is different between the studied devices: the leakage current is higher for leaky devices than for non-leaky ones for all the studied temperature range. The output characteristics showed no difference between the “NL” and “L” devices, as well as the static resistance R_{DS} that is superimposed for all studied devices for temperature range of 100K-400K. This highlights that the leakage path is not located in the channel.

Another different feature of the leaky devices compared to the non-leaky ones is the negative dependence of the drain subthreshold leakage current with temperature from 300K to 400K.

The gate and drain leakage currents of the non-leaky transistor versus gate-source voltage increases with temperature, which is reported as the normal behavior. The drain and gate leakage current dependence with temperature for the leaky transistor is inverse to the non-leaky one in subthreshold regime below $V_{GS} = -2V$. Indeed both gate and drain currents present an inverse dependence on temperature in subthreshold regime but they have the same dependence on V_{GS} below $-2.6V$. This was investigated by drain current transient measurements that showed three dominant traps for the leaky transistor with activation energies between 0.7 eV and 0.9 eV. Traps with activation energies in this range were reported in literature to be associated with electron injection from the gate and trapping either inside the AlGa_N layer or at the surface close to the gate.

The inverse temperature dependence of the reverse gate current with temperature has also been explained in [Kaushik 2013] using a virtual gate-trap-assisted tunneling model that assumes the presence of surface states at the AlGa_N/Si_N interface close to gate metal and bulk traps in the AlGa_N layer of the HEMT. As already reported, the leakage currents of Ga_N based HEMT might be reduced by accurate engineering of the buffer layer and of the AlGa_N/Si_N interface in the vicinity of the gate.

Electrical pulsed measurements have been given special attention by making sure that the time profile of the drain current and gate and drain voltages are well established and in a steady state in the instantaneous and quiescent bias time. This is to make sure that the measurements are correct.

Low gate-lag is found on non-leaky devices (lower than 7% near pinch-off conditions, close to zero near open channel condition). Leaky devices present a gate lag ratio more than 3 times higher than non-leaky devices. However, the drain-lag is similar for all the studied devices which mean that traps are rather located in the gate area.

We noticed that there is no current dispersion in ohmic regime and a weak one in saturation regime. Therefore, the GH50_10 technology does not suffer from dispersion of the dynamic on-resistance which is known to affect high-voltage switching performances.

The pulsed measurement results were correlated in the frame of ReAGaN project with low frequency noise measurements provided by LAAS laboratory and were published in [Karboyan 2013]. The identification of the different mechanisms and the localization of leakage path are investigated by physical analysis in the Task 4 of the project ANR ReAGaN [Lambert 2012].

3.2. Case study 2: Belly Shape parasitic effect

3.2.1 Purpose of the case study: data from ageing test

The purpose of this case study is to characterize an electrical parasitic effect that is detected on the gate-source and gate-drain diodes forward current characteristics after accelerated life tests. Virgin and aged devices from the GH25 UMS GaN process have been compared at UMS. Twelve devices with eight gate fingers of 125 μm width (1 mm total gate periphery) are studied. HEMTs have been aged by 20 V high temperature operating lifetime (HTOL) stress carried out at a case temperature $T_C = 155\text{ }^\circ\text{C}$ and a junction temperature $T_J = 255\text{ }^\circ\text{C}$ and $I_{DS} = 210\text{ mA/mm}$ during 7000 hrs. They are divided in two lots of six devices (one used as reference and five aged ones) issued from different wafers.

3.2.2 Monitoring of the electrical parameters during HTOL test

The HTOL test is performed in nominal operating conditions until achieving 50% of failures in order to determine the lifetime of the devices.

The failure criteria are defined either by drift of one or several electrical parameters down or up to defined limits during the ageing test or the burnout of the device. The evolution of the electrical parameters during the ageing test must be recorded in order to be able to identify the start of the failure.

The test bench allows monitoring the stress conditions during the ageing test. Therefore, the time to failure can be defined precisely when a drift of a parameter occurs. Relevant parameters such as I_{DSPLS} , I_{GLHV} , V_{G100} and G_{mmax} as described in table 6 are extracted from the recovery measurements done at different steps of the ageing test.

Parameter	Conditions	Criteria of failure
I_{DSPLS}	$V_{DS} = 10\text{V}$ and $V_{GS} = 1\text{V}$	$\pm 20\%$
I_{GLHV}	$V_{GS} = -7\text{V}$ and $V_{DS} = 30\text{V}$	$> 200\mu\text{A/mm}$
V_{G100}	$V_{DS} = 10\text{V}$ and $I_{DS} = I_{DSS}/100$	$\pm 20\%$
G_{mmax}	$V_{DS} = 10\text{V}$	$\pm 20\%$

Table 6. Main electrical parameters and criteria of failure of GH25 UMS GaN process[PhD Brunel]

Figure 51 illustrates the evolution of the electrical parameters I_{DSPLS} , I_{GLHV} , V_{G100} and G_{mmax} of the reference devices (black lines), aged devices of the A lot (red lines) and the D lot (blue lines) during HTOL test.

The first recovery measurement performed after 18 hours of HTOL test reveals a positive shift of the threshold voltage V_{G100} of 4% and 4.5% respectively for A and D aged devices. As a consequence, I_{DSPLS} decreases by 3.5% and 3.1% respectively for A and D devices. Furthermore, G_{mmax} decreases by 2.2% and by 1.9% for both lots respectively. The drift of the above parameters is similar to all the aged devices independently of the “belly shape” effect. On the other hand, the drift of the gate leakage current I_{GLHV} is very important for the aged devices with the “belly shape” effect than for the others. The dozen of the recovery measurements that were operated during the HTOL test up to 7000 hours show that the drift of the electrical parameters continue to increase with time and that there is always a

correlation between the drift of I_{DSPLS} , V_{G100} and G_{mmax} . Moreover, in spite of the ups and downs of the drift of I_{GLHV} , the leakage current remains higher for the devices with the “belly shape” effect as well as its drift.

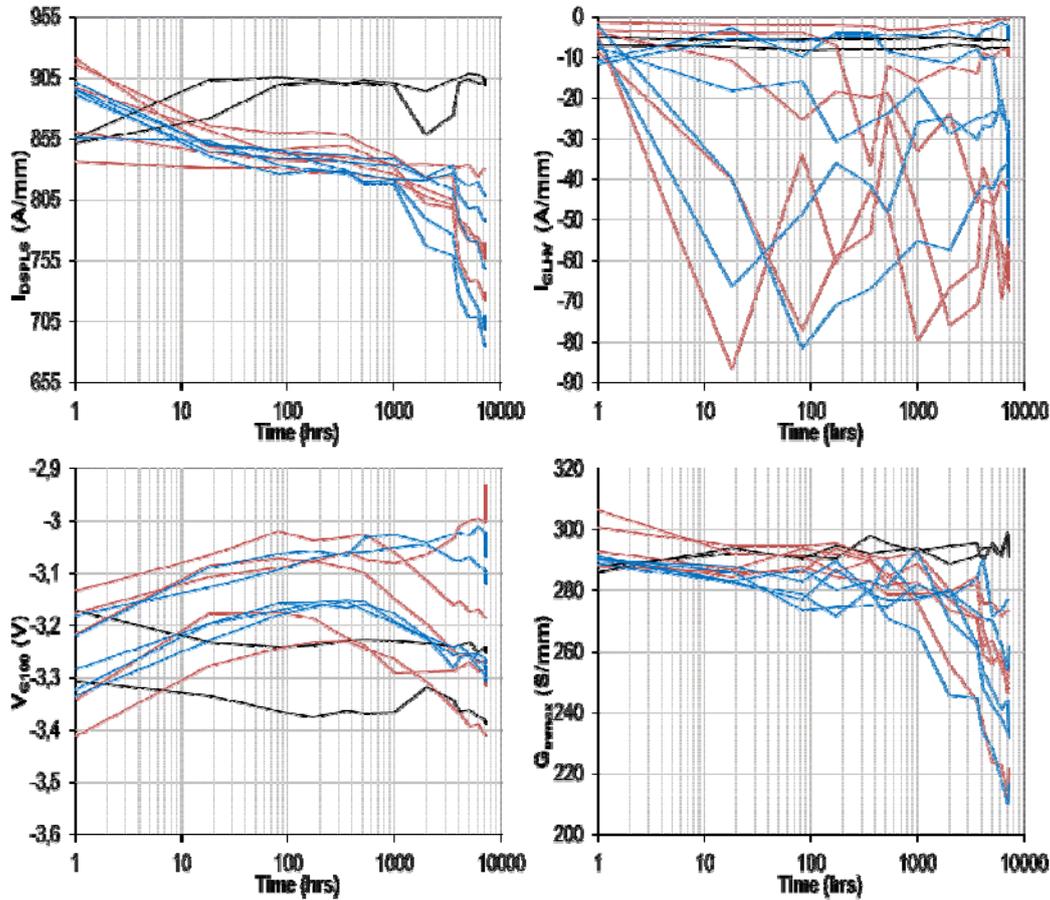


Figure 51. Evolution of I_{DSPLS} , G_{mmax} , V_{G100} , I_{GLHV} of two lots of aged devices (A: red and D: blue) and reference (black) ones during HTOL test; $V_{DS} = 20$ V ; $I_{DS} = 210$ mA/mm ; $T_C = 155$ °C ; $T_J = 255$ °C

3.2.2 DC I-V characteristics of virgin and aged devices at room temperature

3.2.2.1 Schottky diode characteristics

The input I_G - V_{GS} characteristics of the gate - source diode with open drain and at $V_{DS} = 0$ V were measured in forward and reverse modes at 300K for two reference and ten aged devices. Figure 52 shows the Schottky diode forward characteristics of 3 representative devices: two reference devices, and eight aged devices exhibiting the electrical parasitic effect named “Belly Shape” (BS) [Brunel 2013], and two aged ones without BS (NBS).

The BS effect is characterized by higher gate current on the Schottky gate characteristic in forward bias that appears after ageing test compared to the virgin devices for V_{GS} below 1.2V. The trap assisted thermionic emission model is not efficient to fit the forward gate current. The aged devices with BS exhibit an unpredictable behaviour from device to device as the I_G - V_G characteristics are not superimposed. This variation from device to device does

not appear at V_{GS} above 1.4V where the Schottky gate characteristic is influenced by the series resistance of the gate-source diode.

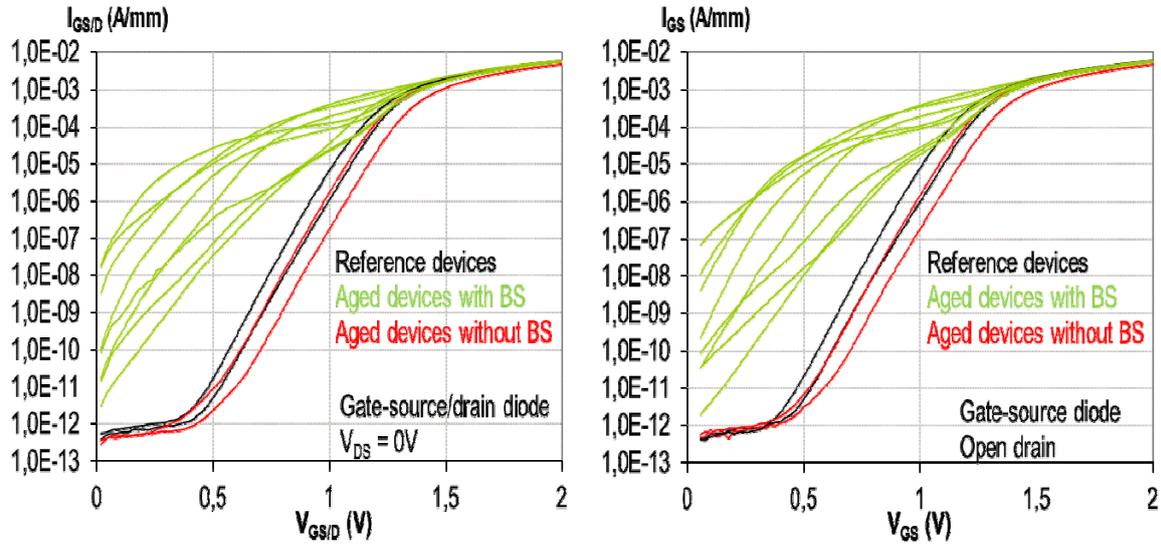


Figure 52. Forward gate current characteristics of reference and aged devices with and without BS for gate-source diode with $V_{DS} = 0V$ and open drain

Few studies have reported on this parasitic effect ([Ando 2013] and [Brunel 2012]) so that it is important to investigate its origin and impact on the lifetime and the reliability of GaN based HEMTs. The Schottky diode reverse characteristics are shown in figure 53 The reverse gate current for devices with BS is higher compared to the reference devices and the aged ones without BS by one or two decades for $V_{GS} < -3V$, while it is higher by 3 decades for $-3V < V_{GS} < 0V$. A high gate leakage current can be correlated with the electrical signature of the “belly shape” effect.

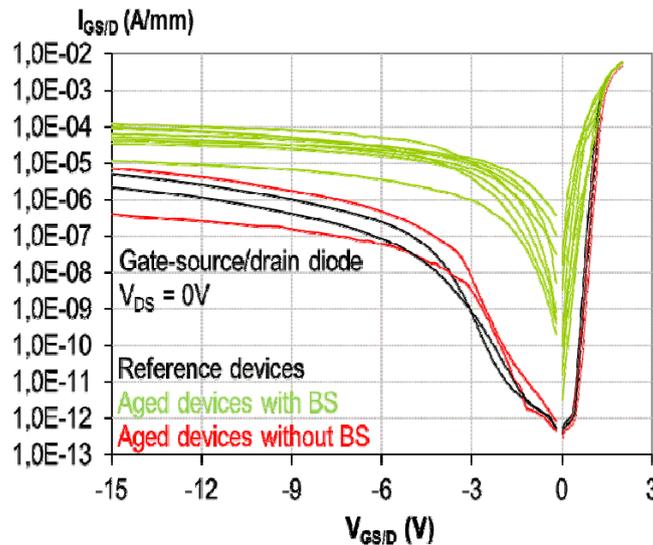


Figure 53. Reverse gate current characteristics of reference and aged devices with and without BS of the gate diode with $V_{DS} = 0V$ and open drain

3.2.2.2 Drain current output characteristics

The BS effect appears on the gate current characteristics as seen above. In order to evaluate the impact of this effect on the electrical performances of GaN based HEMTs, the

output characteristics have been measured to study the influence of the BS on the channel and the carrier transport properties.

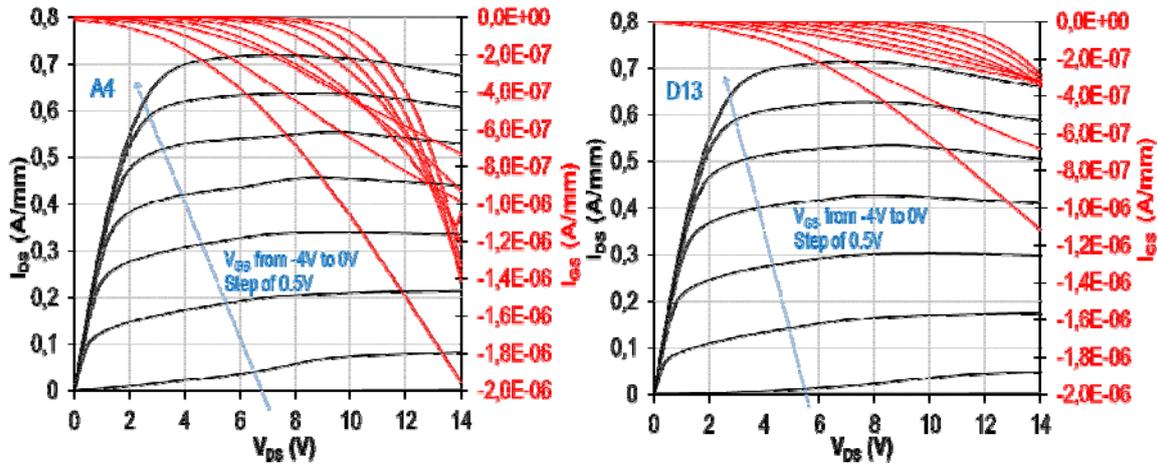


Figure 54. I_{DS} - V_{DS} and I_{GS} - V_{DS} characteristics of reference devices

The figure 54 shows I_{DS} - V_{DS} and I_{GS} - V_{DS} characteristics of the reference devices of the two lots. The saturation current I_{DSS} (I_{DS} at $V_{DS} = 10V$ and $V_{GS} = 0V$) is $0.7A/mm$ for both devices, and the calculated static drain-source resistance R_{DS} (at $V_{GS} = 0V$ and for V_{DS} from 0 to $0.4V$) is $2.8 \Omega.mm$. The R_{DS} parameter results from the contribution of the ohmic contacts resistance and carrier transport properties in the channel, mainly electron mobility. We observe an increase of the gate current with the increase of V_{DS} up to $10V$ for V_{GS} from $0V$ to $-4V$. Then, a curve cross is noticed at higher values of V_{DS} for V_{GS} higher than the threshold voltage, consequently the gate current becomes much higher when V_{GS} is approaching $0V$. This phenomenon named “runaway” was identified as a mechanism of end of life of the GH50_10 technology [Lambert 2012] and will not be detailed in this case study. It has also been characterized and explained in the PhD report of Laurent Brunel [Brunel 2013].

The measured I_{DS} - V_{DS} characteristics of the aged devices without the “belly shape” effect A10 and D5 are shown in figure 55. In this figure, we notice the effect of the ageing test on the aged devices without the parasitic effect. The aged devices were received after the end of 7000 hours of HTOL test and were not characterized at different steps of the stress. The comparison of the electrical parameters of the aged devices is performed with the ones of the reference devices. I_{DSS} is respectively $0.60 A/mm$ and $0.67 A/mm$ for the A and D aged devices. It is lower compared to the one of the reference devices. I_{DSS} of A10 and D5 have been degraded respectively by 8% and 23% after HTOL test. The calculated R_{DS} value is $3 \Omega.mm$ for both devices. The degradation of I_{DSS} suggests a possible decrease of the charge density in the 2-DEG channel caused by the thermal stress [Vitobello 2012] or hot electron effects occurring during the HTOL test. The phenomenon of the runaway does not appear on the characteristics of the gate current, an indication that it has disappeared or it has been delayed to higher values of V_{DS} . In transistor mode, the gate leakage current is about ten times lower than for reference devices. Chini et al [Chini 2014] have reported on the decrease of the gate leakage current after RF stress, and explained this by a density increase of an acceptor trap located beneath the gate contact and in the AlGaIn layer.

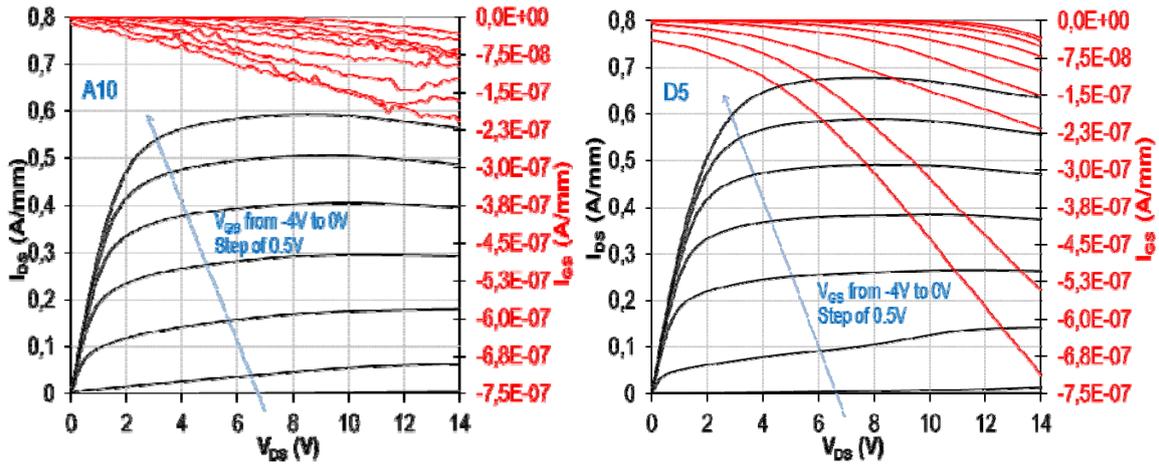
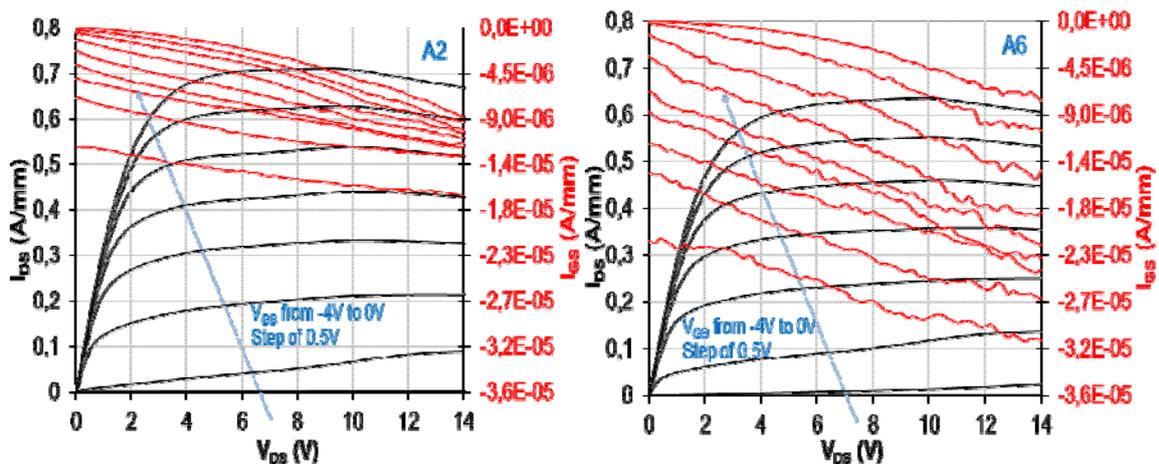
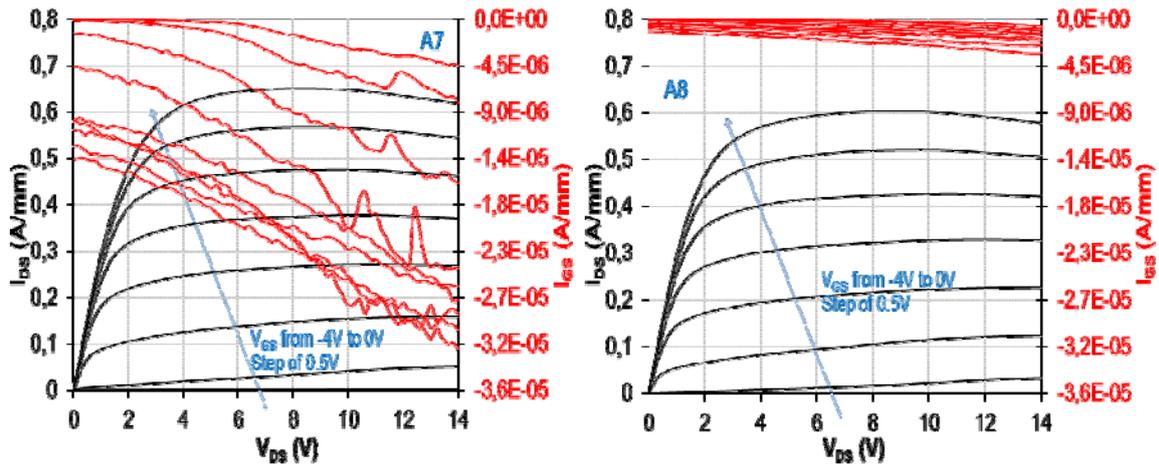
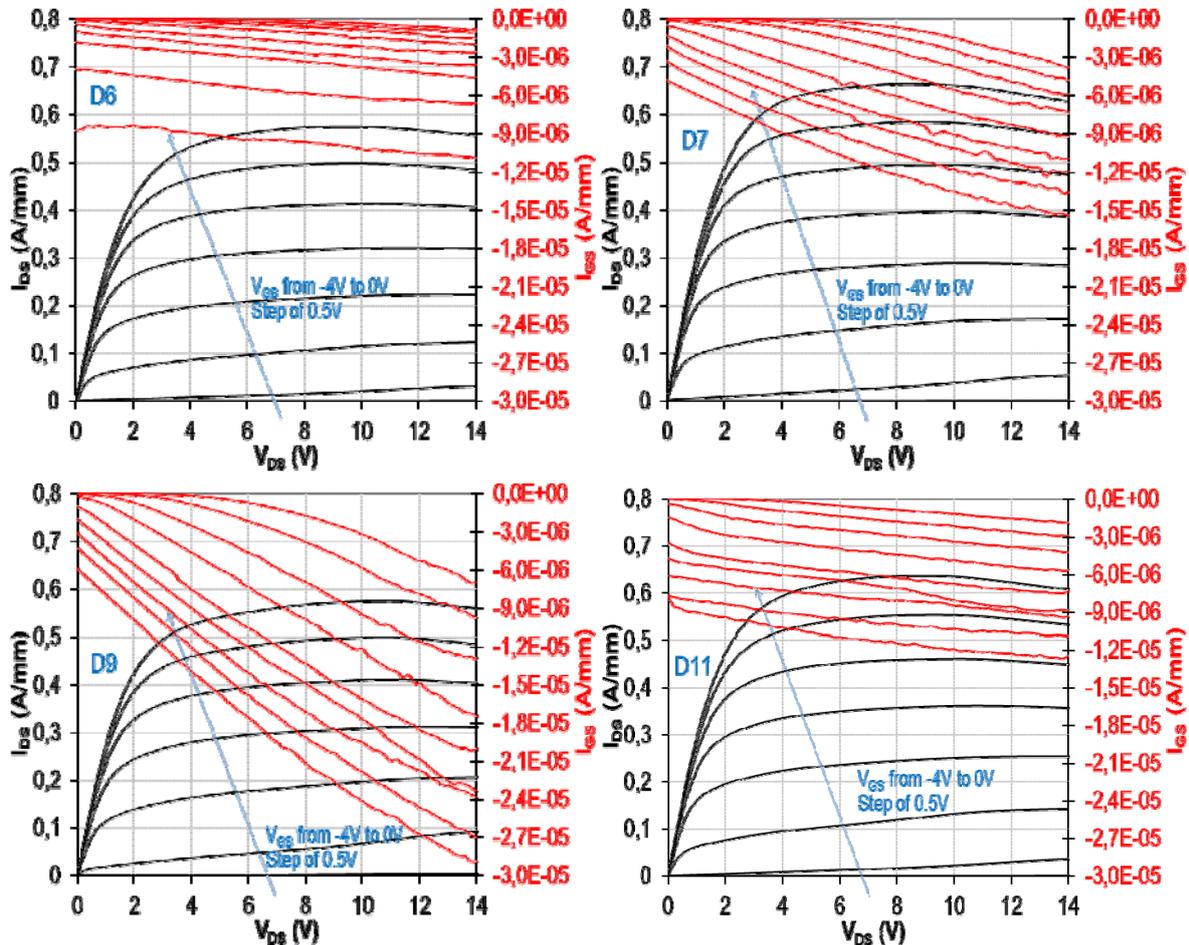


Figure 55. I_{DS} - V_{DS} and I_{GS} - V_{DS} characteristics of aged devices without Belly Shape

The measured I_{DS} - V_{DS} characteristics of the aged devices with the “belly shape” effect from the lots “A” and “D” are shown respectively in figures 56 and 57. I_{DSS} is between 0.57 A/mm and 0.70 A/mm and by referring to degradation between 10% and 20% of I_{DSS} after the ageing test, it is clear that the decrease of I_{DSS} is due to the ageing test. Moreover, it occurs for all the aged devices independently of the “belly shape” effect. Therefore, the “belly shape” effect does not impact the channel and carrier transport properties.

As the features of the “belly shape” effect are unpredictable and not superimposed in the I_{GS} - V_{GS} characteristics, the same applies to the gate leakage current characteristics but the electrical signature is similar. The gate leakage current is not as low at $V_{DS} = 0V$ for $V_{GS} > -3V$. For example at $V_{DS} = 0V$ and $V_{GS} = 0V$, the gate leakage current varies from 2 $\mu A/mm$ to 10 $\mu A/mm$ from device to another which are high values for a leakage current. The phenomenon of the runaway does not appear on the characteristics of the gate current, an indication that it has disappeared or it has been delayed to higher values of V_{DS} . The runaway phenomenon has been detailed in chapter 2.




 Figure 56. I_{DS} - V_{DS} and I_{GS} - V_{DS} characteristics of “A” aged devices with Belly Shape

 Figure 57. I_{DS} - V_{DS} and I_{GS} - V_{DS} characteristics of “D” aged devices with Belly Shape

The gate leakage current in diode or transistor characteristics of the aged devices with the “belly shape” effect is much higher than other devices under study. The path of the leakage current is created during the ageing test through cracks or pits [Brunel 2012] or can be due to the thinning or partial vanishment of GaN cap layer as reported by Ando et al. [Ando 2013] for AlGaIn/GaN HEMTs on Si substrate after HTOL test.

3.2.2.3 Transfer and transconductance characteristics

In this section, the transfer characteristics ($I_{DS} - V_{GS}$) are analyzed in order to extract the threshold voltage (V_{TH}), the transconductance (G_m) and to study the correlation between the gate and the drain subthreshold leakage currents for devices with and without “belly shape” effect.

The measured I_{DS} (I_{GS})- V_{GS} characteristics of the reference devices are plotted in logarithmic scale are shown in figure 58.

The threshold voltage at $V_{DS} = 1V$ of the A and D devices is respectively $V_{TH} = -2.82V$ and $-2.75V$. In the subthreshold regime ($V_{GS} < -4V$), the gate and drain leakage currents increase with V_{DS} and the gate leakage current is slightly higher than the drain one. At $V_{GS} = -10V$ and $V_{DS} = 10V$, the drain leakage is about $3\mu A/mm$ for both reference devices.

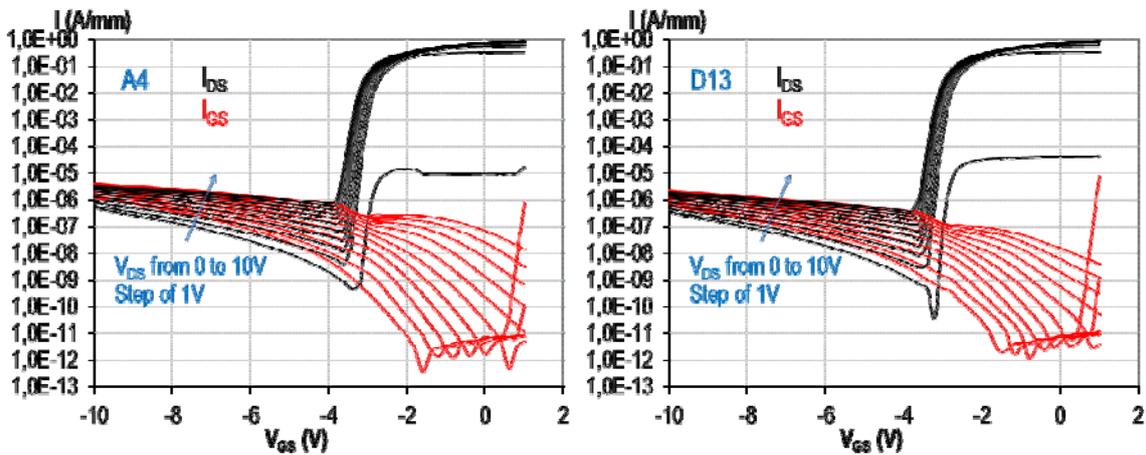


Figure 58. I_{DS} - V_{GS} and I_{GS} - V_{GS} characteristics of reference devices

The measured I_{DS} - V_{GS} characteristics of the aged devices without “belly shape” effect are shown in figure 59. The threshold voltage at $V_{DS} = 1V$ of the A and D devices is respectively $V_{TH} = -2.3V$ and $-2.65V$. The average value of the threshold voltage measured at UMS named V_{G100} ($V_{DS} = 10V$ and $I_{DS} = 1\%$ of I_{DSS}) before the ageing test is $-3.2V$ for the studied devices, which means that V_{TH} of the devices showed in figure 9 have been shifted to positive values after HTOL test. The gate and the drain subthreshold leakage currents of the A10 device are superimposed and they are between $0.1\mu A/mm$ and $0.4\mu A/mm$ at $V_{GS} = -10V$ for V_{DS} from 0 to 10V. The subthreshold leakage currents of the D5 device are not superimposed. Indeed, the gate current is higher than the drain one. The characteristics of the two aged devices without “belly shape” effect are not similar; hence it is not possible to conclude on the effect of the ageing test on the drain and gate leakage currents.

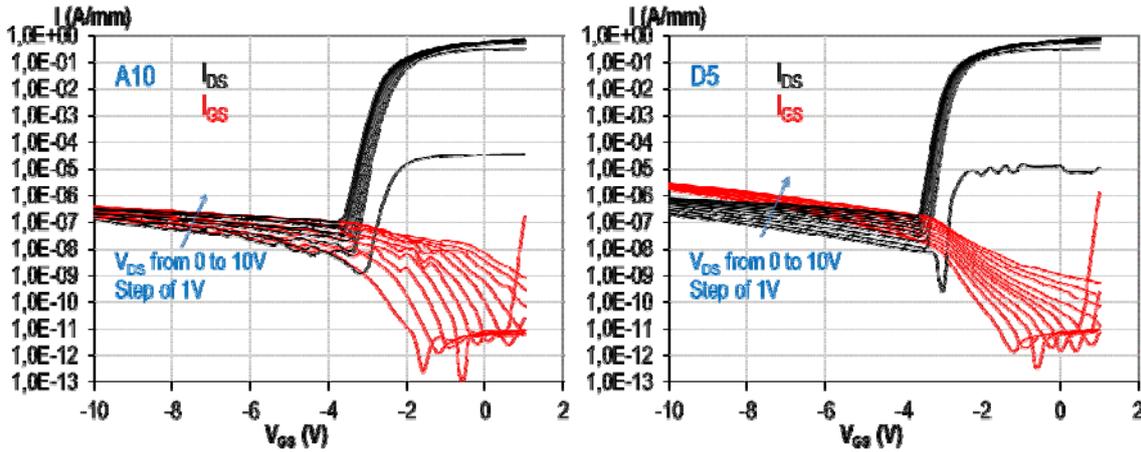


Figure 59. I_{DS} - V_{GS} and I_{GS} - V_{GS} characteristics of aged devices without Belly Shape

The measured I_{DS} - V_{GS} characteristics of the aged devices with “belly shape” effect of the A and D devices are respectively illustrated in figures 60 and 61. The gate subthreshold leakage current is higher than the drain one by one decade or two for some devices except for the D9 device for which the gate and drain leakage currents are superimposed. In spite of the fact that the dependence of the subthreshold leakage current with V_{DS} or V_{GS} differs from a device to another, there are common behavior that characterize the devices with “belly shape” effect. Indeed, the gate subthreshold leakage current of devices with BS effect is between $10\mu A/mm$ and $100\mu A/mm$ at $V_{GS} = -10V$ and tends to not depend on V_{DS} .

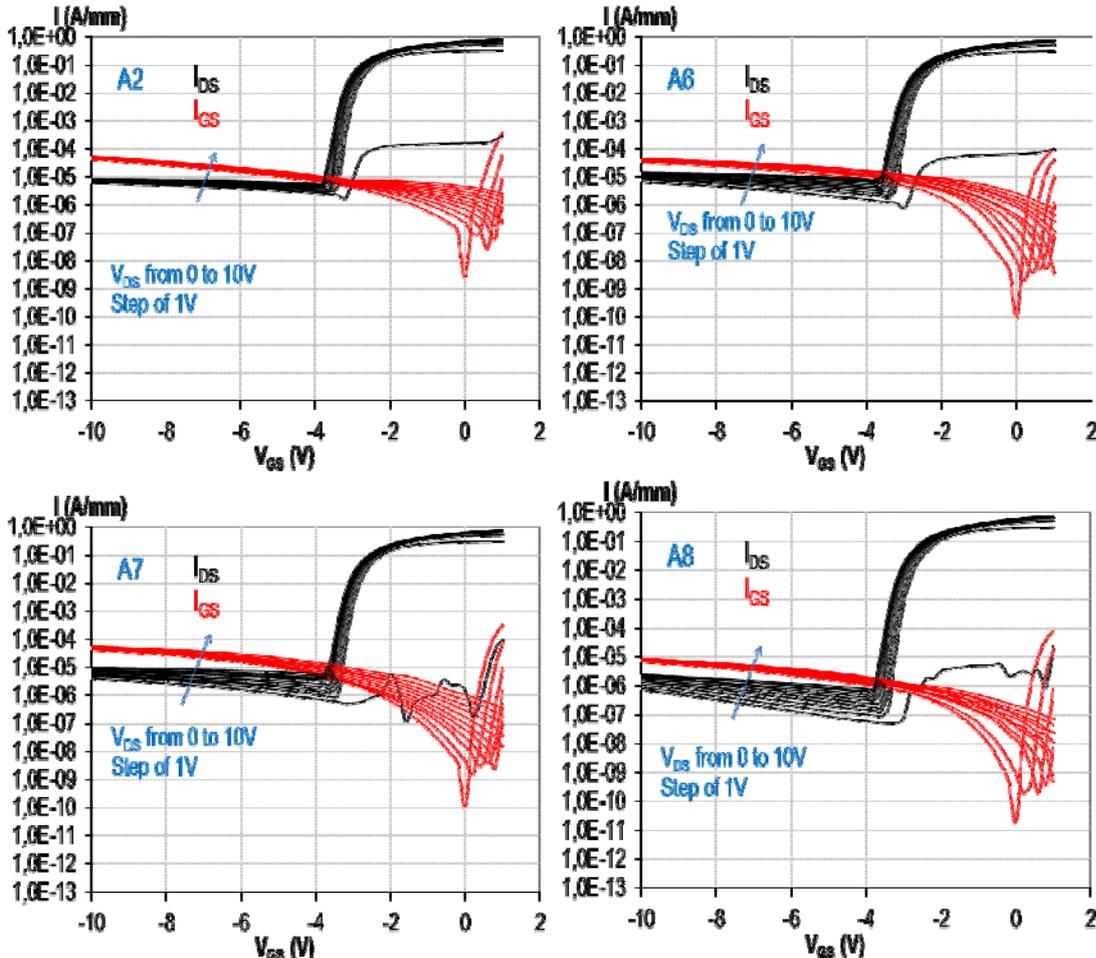


Figure 60. I_{DS} - V_{GS} and I_{GS} - V_{GS} characteristics of “A” aged devices with Belly Shape

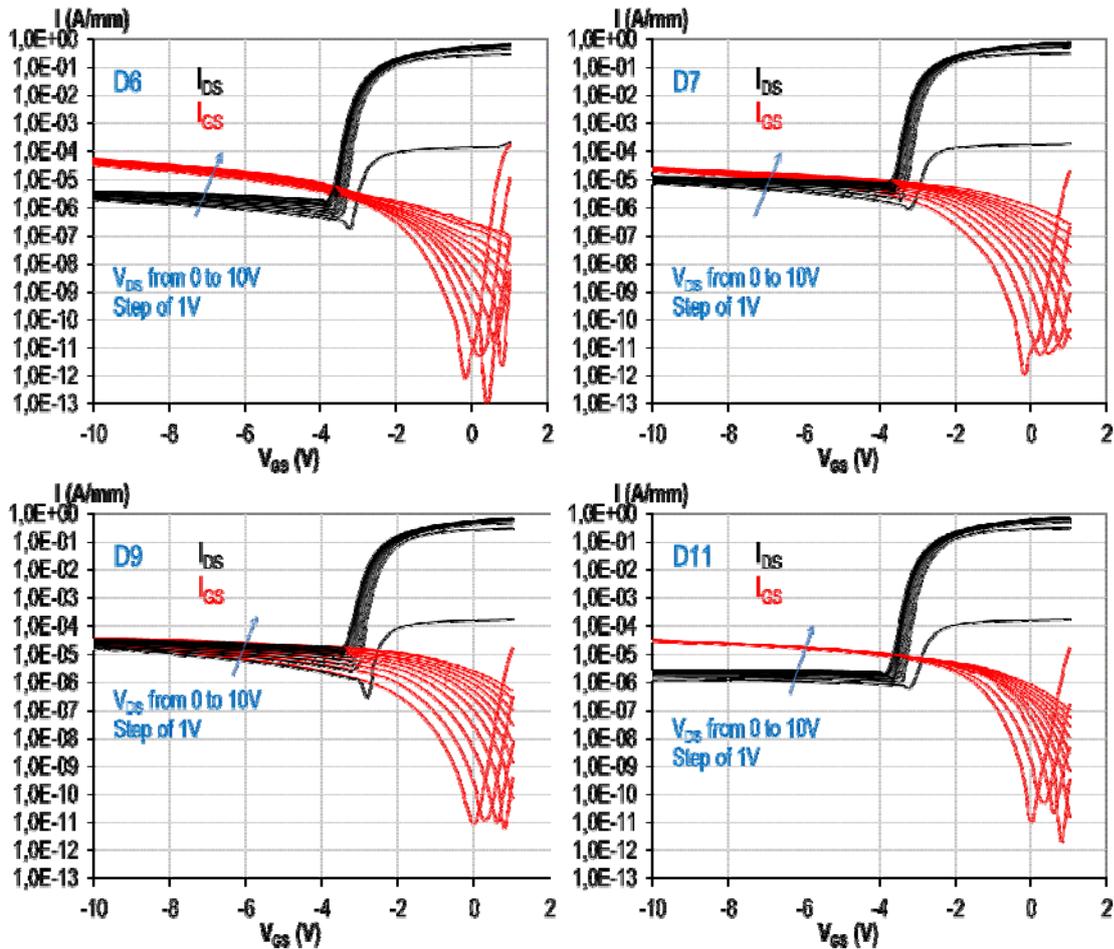


Figure 61. I_{DS} - V_{GS} and I_{GS} - V_{GS} characteristics of “D” aged devices with Belly Shape

The drain current and the transconductance dependence with V_{GS} at $V_{DS} = 6V$ are shown in figure 62. The drain current I_{DS} at $V_{GS} = 1V$ of the aged devices is lower than the one of the two reference devices. The maximum transconductance G_{mmax} of the aged devices is lower than the one of the reference devices, as well as the positive shift of the threshold voltage of the aged devices compared to the reference ones. The decrease of these parameters as was seen in the monitoring of the HTOL test is due to the ageing test independently of the “belly shape” effect.

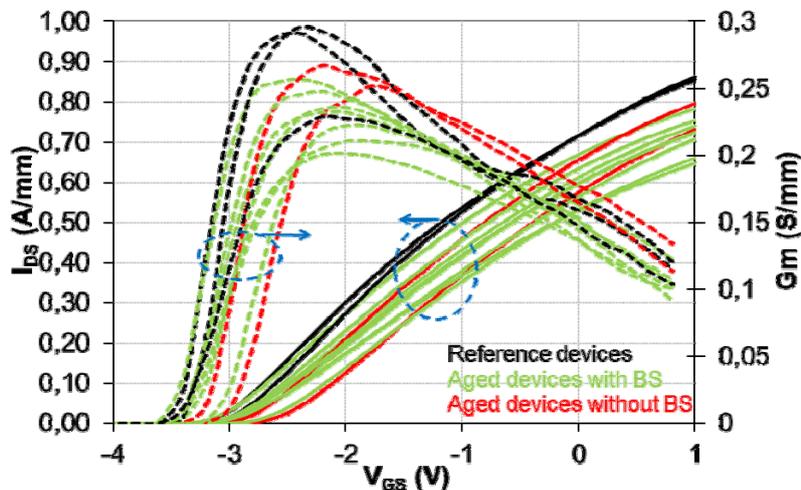


Figure 62. I_{DS} & G_m vs. V_{GS} at $V_{DS} = 6V$

3.2.2.4 Subthreshold leakage current

The purpose of this paragraph is to study the correlation between the gate and drain subthreshold leakage currents. The gate subthreshold leakage current evolution with V_{DS} at $V_{GS} = -10V, -8V, -6V$ and $-4V$ for three typical devices is shown in figure 63. The gate leakage current increases with both V_{GS} and V_{DS} for the reference device and the aged one without the “belly shape” effect. On the other hand, the gate leakage current presents a resistive behavior with V_{DS} for the aged device with the “belly shape” effect and the leakage current is higher by at least a decade compared to the other devices.

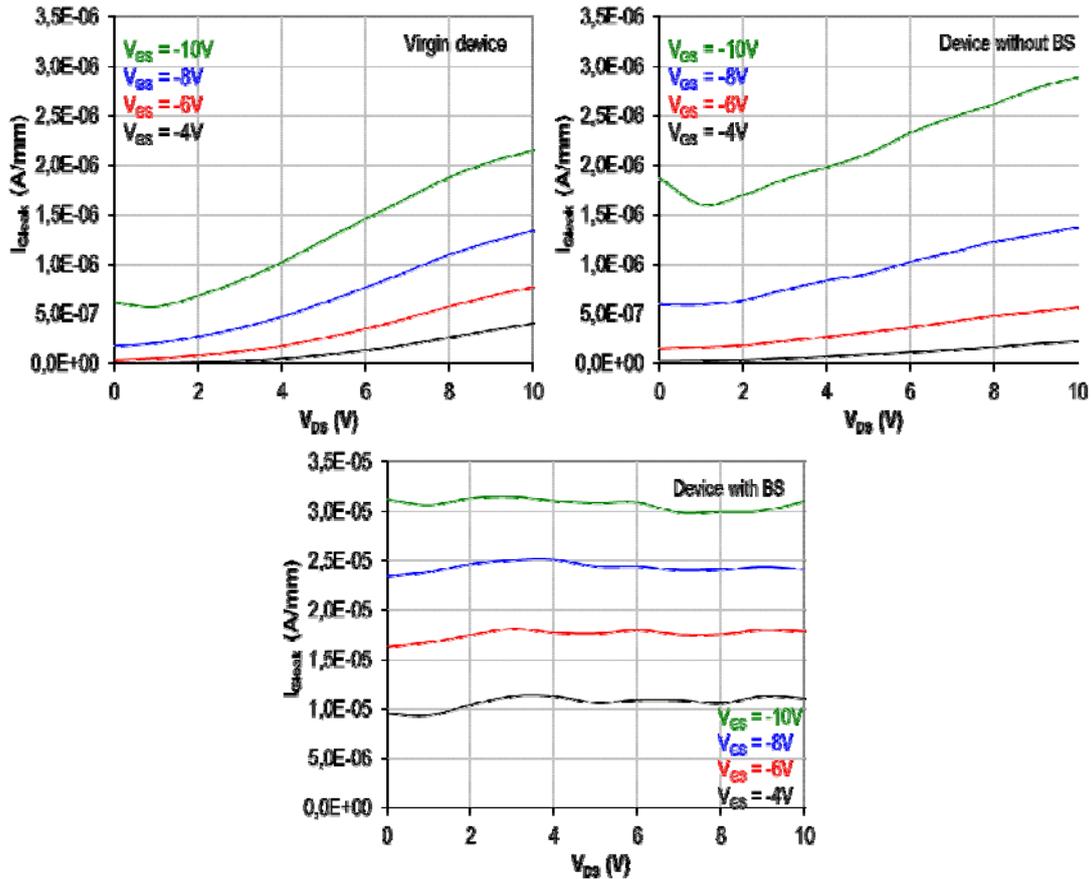


Figure 63. I_{Gleak} - V_{DS} of reference and aged devices with and without Belly Shape

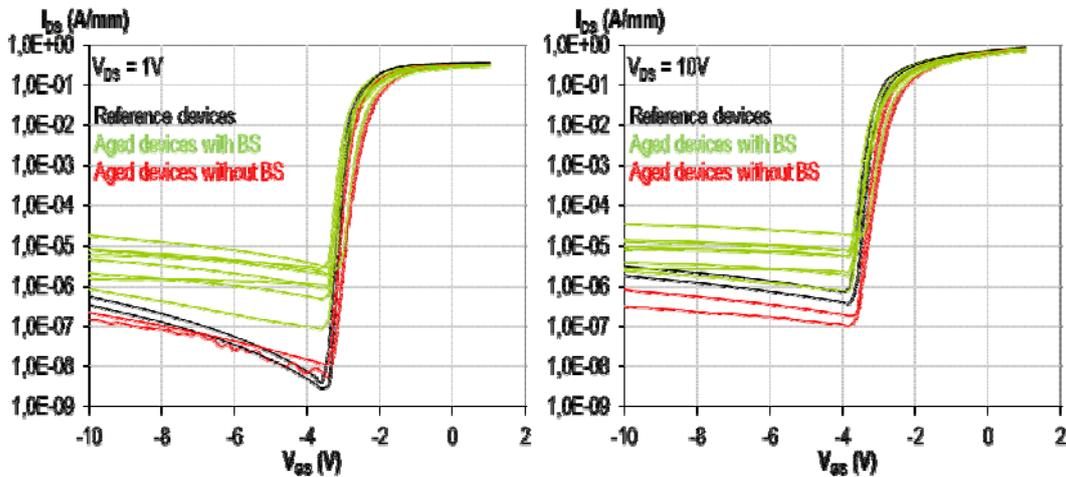


Figure 64. I_{DS} vs. V_{GS} at $V_{DS} = 1V$ & $10V$

The transfer characteristics of all the studied samples presented in logarithmic scale at $V_{DS} = 1V$ and $V_{DS} = 10V$ are illustrated in figure 64. The drain subthreshold leakage current is higher for the aged devices with “BS” than for the other devices for both values of V_{DS} . The gate leakage current of all the studied devices have been plotted in logarithmic scale versus the drain leakage current at $V_{DS} = 1V$ and $10V$ to correlate both leakage currents as shown in figure 65. The green line indicates when both leakage currents are equal. The gate leakage current is always higher than the drain one for all devices. Both leakage currents are approximately equal at $V_{DS} = 1V$ and $10V$ for the reference devices. Moreover, the leakage current of the aged devices without the “BS” are equal for a device and not for the second one. Furthermore, the gate leakage current is always higher than the drain one for the aged devices with “BS”.

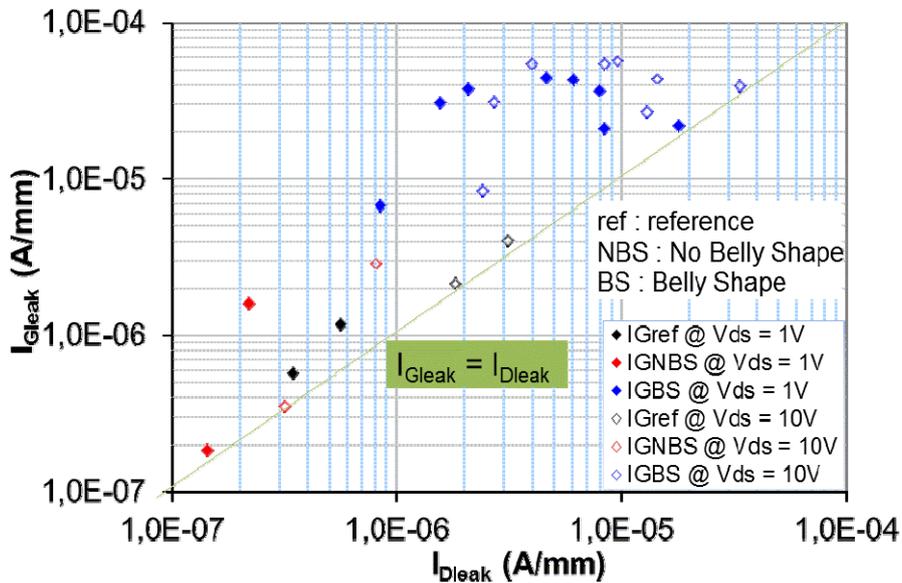


Figure 65. Subthreshold leakage current

The main electrical parameters I_{DSS} , R_{DS} , I_{DSPLS} and V_{TH} of the studied devices are summarized in table 7.

	Device	I_{DSS} (mA/mm)	R_{DS} (Ω .mm)	I_{DSPLS} (mA/mm)	V_{TH} (V)
Ref	A4	711	2,81	843	-2.82
	D13	701	2,78	834	-2.75
Aged NBS	A10	590	3,02	729	-2.3
	D5	671	2,95	801	-2.65
Aged BS	A2	708	2,85	833	-2.9
	A6	634	3,12	764	-2.66
	A7	647	3,09	777	-2.78
	A8	601	3,07	732	-2.66
	D6	574	3,31	690	-2.8
	D7	660	3,04	790	-2.75
	D9	574	3,21	699	-2.45
	D11	635	3,05	765	-2.75

Table 7. Summary of the main electrical parameters

3.2.4 Low frequency gate current noise

Gate current low frequency noise (LFN) measurements are used as a tool to study the fluctuations of the gate current as well as the carrier transport properties that are strongly influenced by crystalline defaults and/or trapping effects.

The studied devices were biased in a common-source configuration at $V_{DS} = 0V$. The gate current noise measurements are performed by sweeping the gate voltage from the value corresponding to a gate current of 100 nA/mm up to $V_{GS/D} = 1.48V$. The noise spectra were measured at room temperature in the frequency range of 1Hz to 100 kHz. The low noise current preamplifier has a bandwidth of 25 kHz on its most sensitive range used for $10 \text{ nA} < I_{GS/D} < 100 \text{ nA}$ and a bandwidth of 1 MHz on its least sensitive range.

In Figure 66, LF gate current noise spectra densities are measured in the belly-shape region, for $V_{GS/D}$ below 1.2 V. The LFN spectra of the reference devices have $1/f^\gamma$ noise behavior with γ close to 1 in the 1 Hz – 10 kHz frequency range. The LFN spectra of the aged devices without BS effect present pure $1/f^\gamma$ noise or $1/f^\gamma$ noise with superimposed generation-recombination

(g-r) noise components for $V_{GS/D} < 1V$. On the contrary, all noise spectra of aged devices with BS effect exhibit g-r noise components.

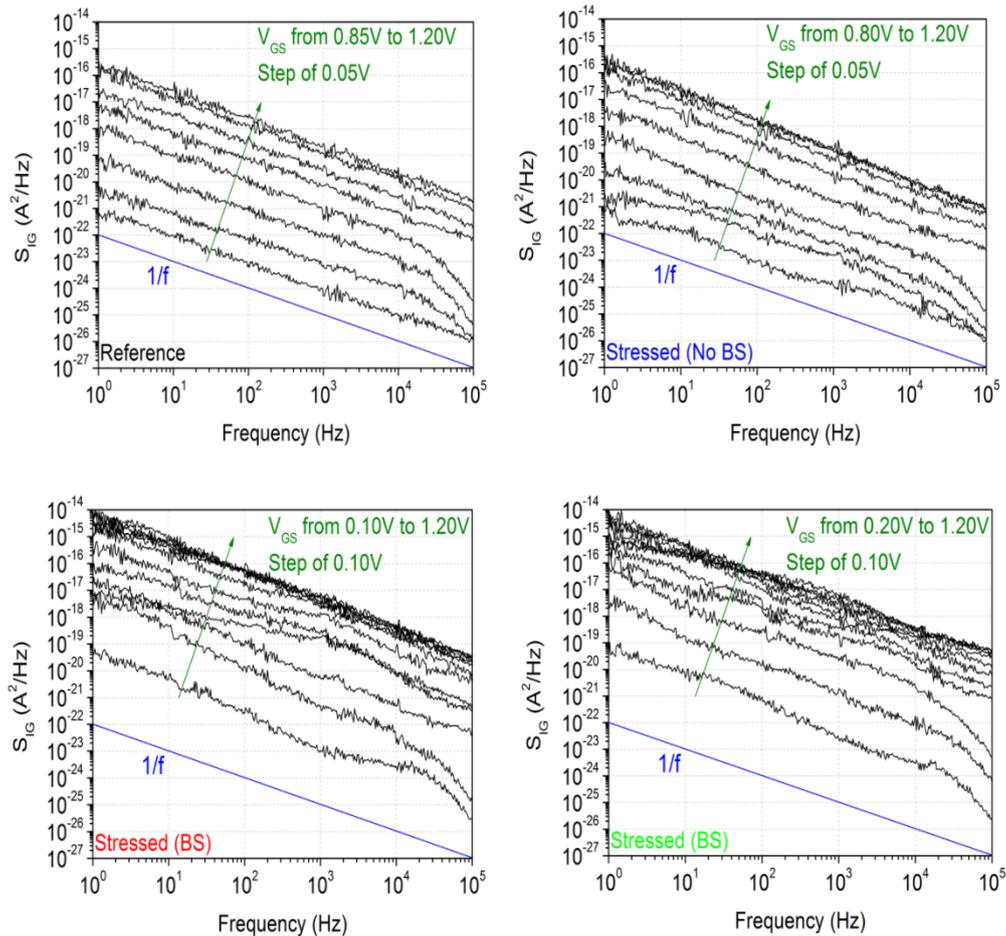


Figure 66. Gate current noise spectra S_{IG} evolution with V_{GS} lower than 1.2V in the BS effect region for a reference device and a stressed one without belly-shape effect and 2 stressed devices

with belly-shape effect at $V_{DS} = 0V$. The solid blue line is the theoretical $1/f$ noise law

Overall, the LFN of aged devices with BS is higher compared to the one of reference and aged devices without BS effect. A deep analysis of this comparison is given farther.

Gate current LFN has been measured for gate bias voltage higher than the region where the “BS” effect appears, i.e. for $V_{GS/D}$ from 1.2V to 1.48V. Gate current LFN for $V_{GS/D} > 1.2V$ are shown in figures 67 and 68. For all devices under study, the gate current LF noise decreases by at least a decade for $V_{GS/D}$ varying from 1.2V to 1.48V. $1/f^y$ noise is dominant for $V_{GS/D} > 1.2V$, with some g-r noise components that appear for the aged devices with BS effect.

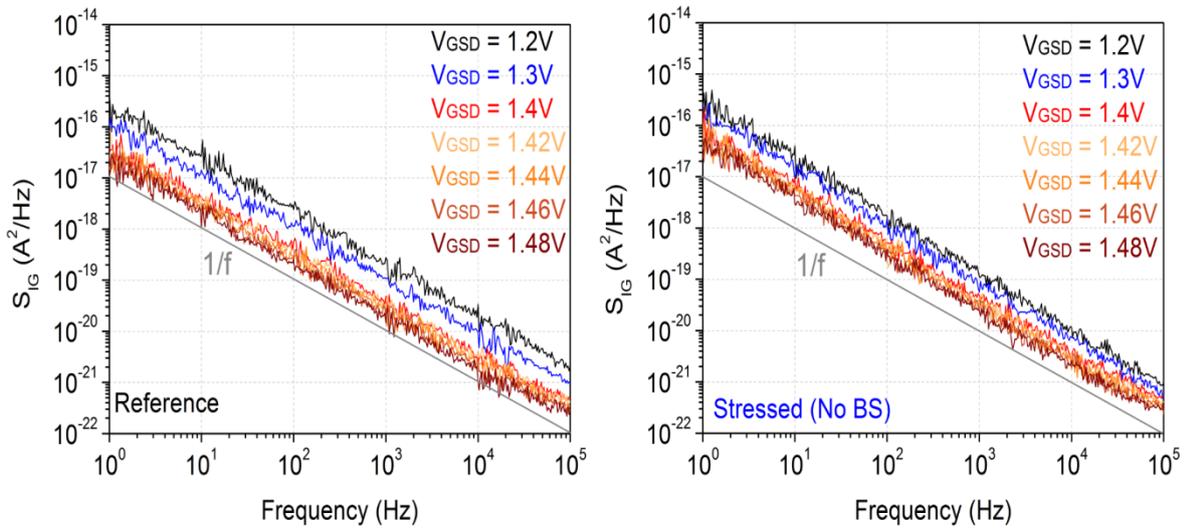


Figure 67. Gate current noise spectra S_{IG} evolution with V_{GS} varying from 1.2V to 1.48V at $V_{DS} = 0V$ in the diode series resistance region for a reference device and a stressed one without belly-shape effect.

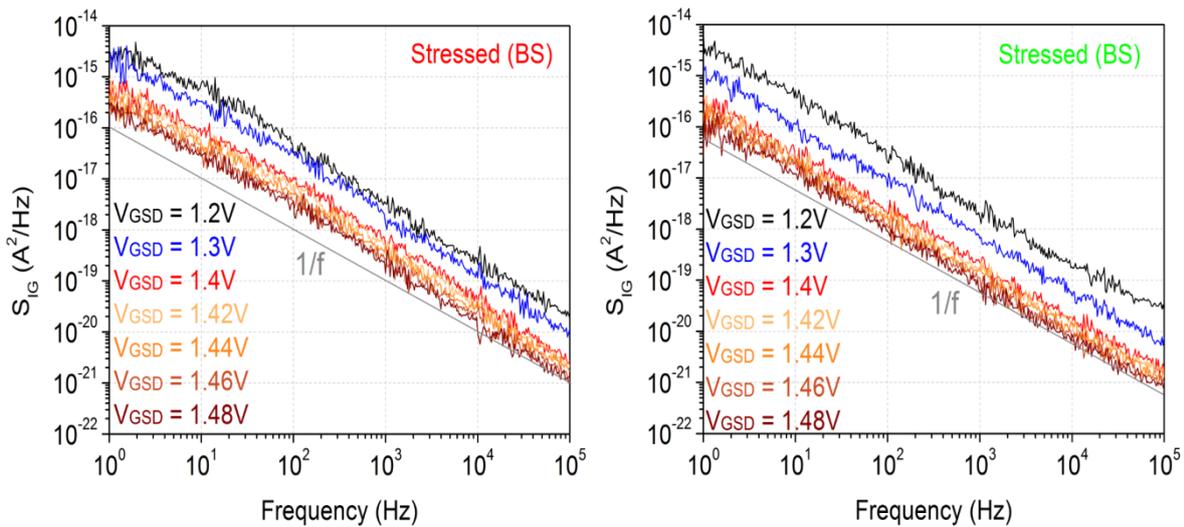


Figure 68. Gate current noise spectra S_{IG} evolution with V_{GS} varying from 1.2V to 1.48V in the diode series resistance region for two stressed devices with belly-shape effect.

Another gate current fluctuation mechanism is detected for $V_{GS/D} > 1.2$ V at $V_{DS} = 0$ V that is not necessarily related to the ageing test. Indeed, virgin devices as well as aged devices present the same behavior. This noise component is even replacing the g-r noise in the aged devices with BS effect.

3.2.4.1 1/f low frequency noise

The $1/f^\gamma$ (with $\gamma = 1$) noise component of S_{IG} is extracted from the noise spectra of the reference device for $V_{GS/D}$ from 0.85 to 1.48V and plotted as a function of forward gate current $I_{GS/D}$. S_{IG} is found proportional to square of I_G for $V_{GS/D} < 1.2$ V (Figure 69).

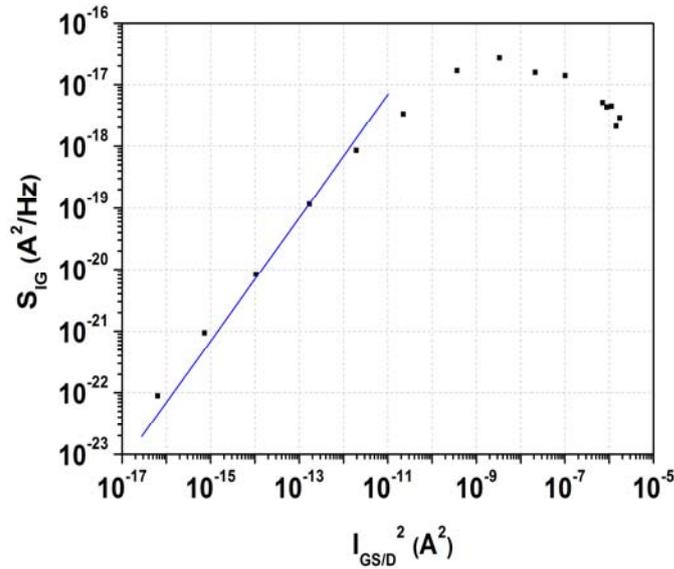


Figure 69. Gate current noise as function of square of gate current. Points are the measured values and solid line indicates the best fit dependence $S_{IG} \propto I_G^2$

S_{IG} dependence on I_G^2 has been reported and is known to be related to trap density fluctuations in the space charge region of the Schottky junction [Rao 2009]. The $1/f$ noise component, detected on the reference and aged devices without BS effect, is reproducible.

For $V_{GS/D} > 1.2$ V, S_{IG} is as expected no more dependent on I_G^2 . It is related to fluctuation mechanisms occurring in the gate-source and gate-drain series resistance.

3.2.4.2 Relative gate current noise: comparison of virgin and aged devices

Figure 70 shows the relative gate current LFN at $V_{GS/D} < 1.2$ V and $V_{GS/D} > 1.2$ V respectively corresponding to the region with and without BS effect. The relative LF gate current noise is higher for aged devices with BS effect than for reference ones.

For $V_{GS/D} < 1.2$ V, the virgin and aged devices without BS effect exhibit $1/f^\gamma$ noise which is proportional to the square of $I_{GS/D}$, while the aged devices with BS effect exhibit Lorentzian noise that is non-repeatable when measured at different times under identical biasing

conditions [Rao 2009]. It has also been observed that the amplitude of the BS effect can vary in the dc characteristics when measured several times.

For $V_{GS/D} > 1.2V$, $1/f'$ noise is dominant as the gate current is governed by diode series resistances.

The comparison of the gate current LF noise at a fixed gate current allows quantifying the noise of the aged devices with and without BS effect in the same operating area. However, the LF noise of aged devices with BS effect for $V_{GS/D} < 1.2V$ is temporally unstable and not all the time repeatable.

We assume that the BS effect is a transient effect related to trapping mechanisms located beneath the gate in the gate/cap GaN interface or at the gate edges induced by HTOL test.

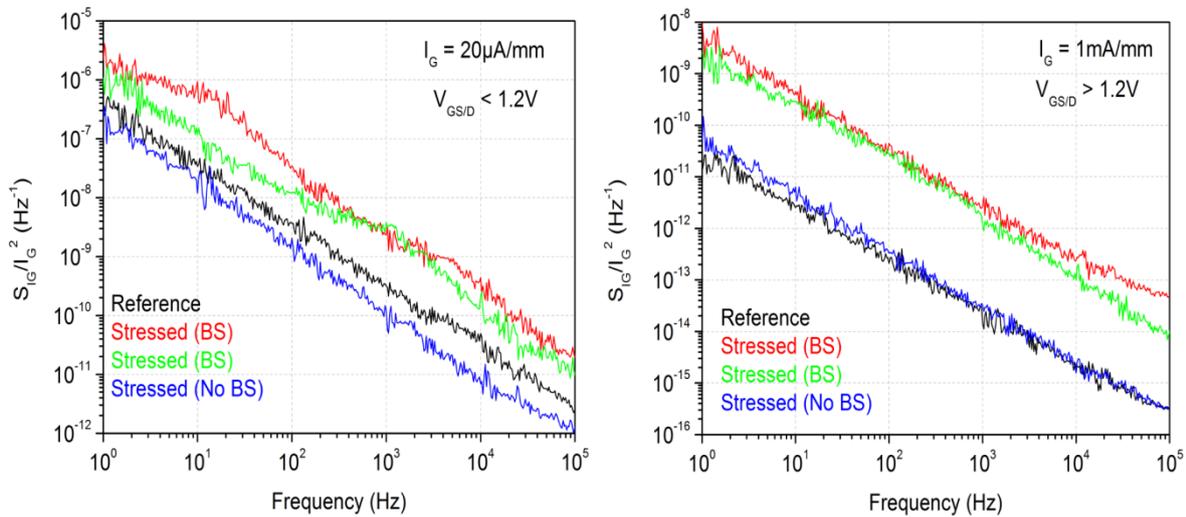


Figure 70. Normalized low frequency noise S_{I_G}/I_G^2 spectra at $I_G = 20\mu A/mm$ and at $I_G = 1mA/mm$

Conclusion of case study 2: “link” with ReAGaN project

High temperature operating life (HTOL) test has been performed to ten devices from two lots of the GH25 UMS GaN process during 7000 hours. The analysis of the electrical characteristics revealed a parasitic effect named “belly shape” effect that appears on the Schottky gate current characteristics in forward bias. The “BS” effect is characterized by higher gate current on the Schottky gate characteristic in forward bias that appears after ageing test for some devices but not all of them. Deep electrical characterization has been operated to investigate this parasitic effect, its signatures and its possible impact on the reliability and the lifetime of the studied devices.

The monitoring of the electrical parameters during the ageing test reveals a degradation of the drain current I_{DSPLS} and the maximal transconductance G_{mmax} as well as a positive shift of the threshold voltage V_{TH} . The above parameters drift happens for all the aged devices independently of the “BS” effect. On the other hand the important drift of the gate leakage current I_{GLHV} occurs only for the aged devices with “BS”.

The drift of the drain current I_{DS} occurs for all the aged devices independently of the “BS” effect which means that the parasitic effect does not impact the life time of the devices. Moreover, only the increase of the gate and drain subthreshold leakage currents is correlated with the “BS” effect.

In summary, an electrical parasitic effect in AlGaIn/GaN HEMTs that appears on the gate current dc characteristic in forward bias after HTOL ageing test is characterized by dc and LFN measurements. The “Belly-Shape” effect is characterized by higher gate current for $V_{GS/D}$ below 1.2V compared to the one of devices without BS effect.

The drift of main dc parameters recorded during HTOL test is similar for all aged devices including the ones with BS effect, which means that the belly-shape effect does not affect the life time of the devices. However, higher gate leakage current after HTOL test is part of the electrical signature of the BS effect as it was noticed for all aged devices featuring this parasitic effect.

The gate current LFN spectra of reference device present $1/f^{\gamma}$ noise, which is proportional to the square of I_G for $V_{GS/D} < 1.2V$. For $V_{GS/D} > 1.2 V$, S_{IG} is as expected no more dependent on I_G^2 . It is found to be related to the Schottky diode series resistances.

Gate current LFN spectra of aged devices without BS effect for $V_{GS/D} < 1.2 V$ exhibit a combination of $1/f^{\gamma}$ and g-r noise components. On the contrary, devices with BS effect exhibit Lorentzian noise that is often non-repeatable even when measured with the same bias conditions as well as the belly shape parasitic effect in the dc characteristics.

The belly shape effect is assumed to be a transient effect related to trapping mechanisms located beneath the gate in the gate/cap GaN interface or at the gate edges.

3.3. Case study 3: Al mole fraction

3.3.1 Purpose of the case study: data from ageing test

The optimization of the performances of AlGaIn/GaN HEMTs has been challenging for designers over the last decade. Many materials have been tested and studied for passivation with different deposition techniques [Fehlberg 2011] to reduce the leakage current and increase the output power and the transconductance. The optimization of the topology and geometry of field-plates in the structure [Ando 2012] [Palankovski 2006] and [Wu 2006] has been used to reduce the high vertical field in the vicinity of the gate. The thickness, doping and alloy composition of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer are crucial parameters in design and optimization of GaN based HEMTs, but the main factor that controls 2DEG density in the channel is the aluminum mole fraction. At given aluminum mole concentration in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer, there is a critical barrier layer thickness beyond which the strain due to mismatch in the layer decreases. For thickness of 20 to 40 nm, the barrier layer is expected to be fully strained for $0 \leq x \leq 0.38$, partially relaxed for $0.38 \leq x \leq 0.67$ and fully relaxed for $0.67 \leq x \leq 1$ [Ambacher 2000]. Ha et al. [Ha 2012] investigated on the electrical characteristics of various Schottky contacts on AlGaIn/GaN heterostructure with a wide range of Al mole fractions and reported that the Schottky Barrier Diode (SBD) increases linearly as the metal work function increases but independently of the Al mole fraction. The 2-DEG electron mobility decreases for high Al mole fraction (>30%). The increase in non-ideal behavior of AlGaIn/GaN-based SBDs with high Al mole fraction was attributed to the increase of un-intentionally incorporated oxygen donors and energy band bending at the surface, resulting in the increase of the tunneling current through the thin, heavily doped Schottky barrier. The increase of 2DEG electron mobility up to the Al mole fraction of 26% and the significant decrease for higher Al content of AlGaIn barrier has also been reported [Guojian 2010]. The main disadvantage of high Al content is the interface defects due to relaxed crystal growth of AlGaIn over GaN causing the degradation of mobility in the 2DEG channel.

The purpose of this case study is to evaluate the influence of the Aluminum (Al) mole fraction of the strained undoped AlGaIn layer on the electrical parameters of virgin and aged AlGaIn/GaN HEMTs in the temperature range of 100K to 400K. Virgin and aged devices from the GH25 UMS GaN process have been characterized. Studied devices present $8 \times 125 \mu\text{m}$ gate finger topology with two Al contents. Two sets of virgin samples were used as control or reference devices: Set A of three devices with 23.5% Al content and set B of five samples with 25% Al mole fraction. A High Temperature Reverse Bias (HTRB) stress has been carried out on four A devices and three B devices at $V_{\text{GS}} = -7\text{V}$ and $V_{\text{DS}} = 30\text{V}$ during 2200 hours with a base plate temperature of 175°C to evaluate the Schottky contact stability over time as a function of Al mole fraction.

3.3.2 DC characteristics of virgin devices at room temperature

3.3.2.1 Schottky diode characteristics

The Schottky diode forward characteristics of the two sets of virgin samples with 23.5% (set J in black) and 25% (set I in red) of Al content in the AlGa_N layer are shown in figure 71. The forward gate current of A devices is higher than the one of the B devices from $V_{GS} = 1V$ until 1.5V. The ideality factor and the Schottky barrier height (SBH) are extracted by using the standard thermionic emission model.

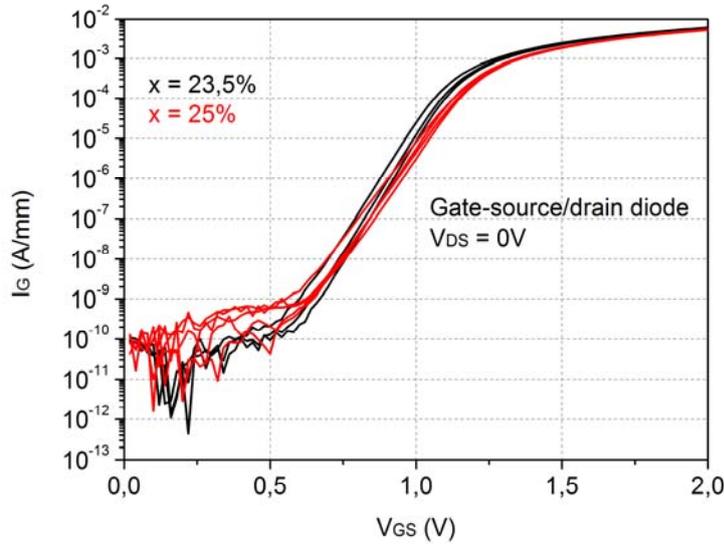


Figure 71. I_G - V_{GS} in forward bias for virgin samples with Al mole fraction (x) of 23.5% (set J) and 25% (set I)

The ideality factor (n) of samples with 25% Al content is slightly higher than the one of the samples with 23.5% of Al mole fraction. The Schottky barrier height (Φ_B) is approximately equal between the two sets of devices. This is due to the fact that the saturation current derived from the straight line intercept of the current at zero bias (I_s) is approximately equal for all devices.

Table 8. The ideality factor and SBH for J devices (23.5% Al) and I devices (25% Al)

devices	J5	J8	J9	I1	I8	I9	I11	I13
n	1.46	1.38	1.42	1.64	1.58	1.76	1.54	1.53
Φ_B (eV)	1.01	1.07	1.04	0.98	1.01	0.92	1.01	1.01

Figure 72 shows the Schottky diode reverse bias characteristics of the two sets of virgin samples with 23.5% (in black) and 25% (in red) of Al content in the AlGa_N layer.

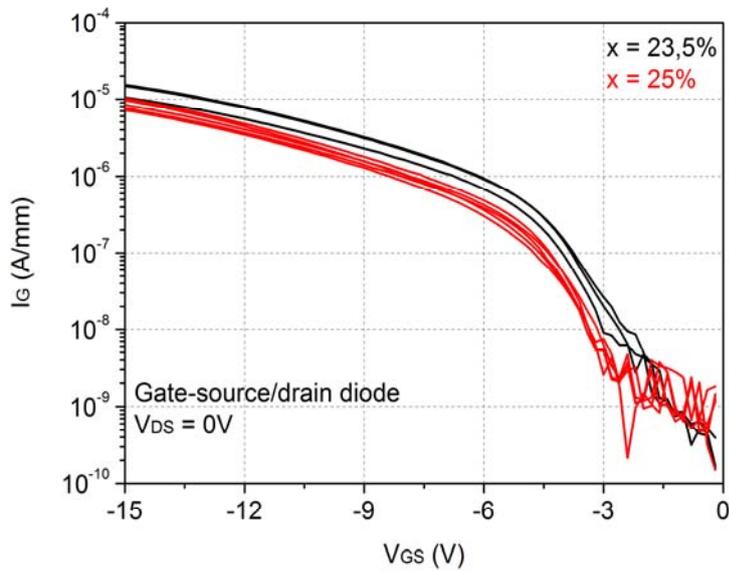


Figure 72. I_G - V_{GS} in reverse bias for virgin samples with Al mole fraction (x) of 23.5% and 25%

The gate leakage current of devices with 23.5% Al content is higher compared to the one of devices with 25%. It was reported [Ha 2012] that more Al mole fraction increases, more the leakage current increases, and this is true for partially or fully relaxed AlGaIn layer. Furthermore for strained AlGaIn layer, it is still possible to increase the Al mole fraction to a critical value to decrease the gate leakage current.

3.3.2.2 Drain current output characteristics

The measured I_{DS} - V_{DS} output characteristics of two sets of virgin samples with 23.5% (black) and 25% (red) of Al content in the AlGaIn layer are shown in figure 73. The gate was biased from -4V to 0V with a step of 0.5V. Both sets of samples exhibited high current drive capability. The drain-source current is similar between A and B samples for $V_{GS} > -1V$ where it is lower for devices with 23.5% Al content compared to devices with 25% Al content for $V_{GS} < -1V$. This is due to the threshold voltage that depends on the Al mole fraction x . The mean maximum drain current I_{DSS} at $V_{GS} = 0V$ and $V_{DS} = 10V$ is 750 mA/mm. Furthermore a slight decrease of R_{DS} is noticed when the Al content increases.

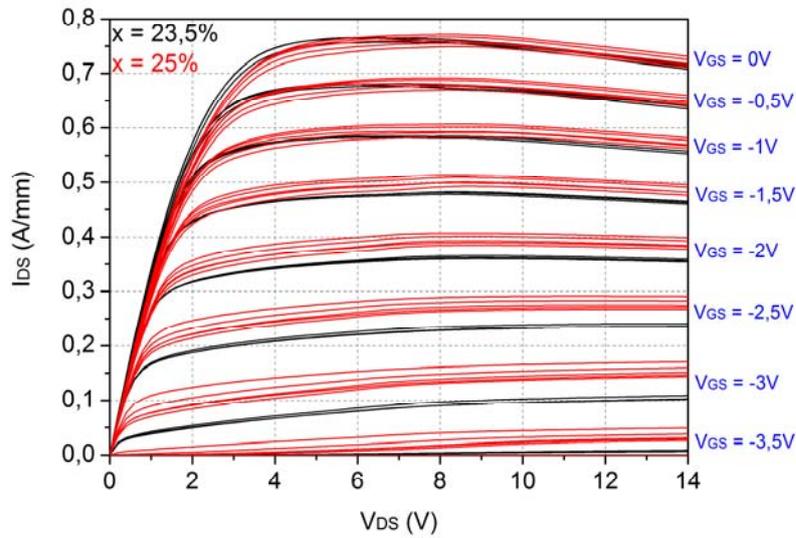


Figure 73. I_{DS} - V_{DS} for virgin samples with Al mole fraction (x) of 23.5% and 25%

The static drain-source resistance R_{DS} and the maximal current I_{DSS} ($V_{GS} = 0V$ and $V_{DS} = 10V$) of the studied samples are summarized in table 9. The R_{DS} of the devices with Al mole fraction of 25% is slightly higher than the one of the other devices. Moreover, the I_{DSS} is similar for both values of Al mole fractions.

Device	R_{DS} (Ω .mm)	I_{DSS} (mA/mm)
I1	3,00	759
I8	3,03	750
I9	3,03	763
I11	3,00	748
I13	3,12	742
J5	2,77	744
J8	2,85	747
J9	2,76	751

Table 9. R_{DS} and I_{DSS} parameters for virgin devices for $x = 23.5\%$ and 25%

The gate leakage current extracted from I_{DS} - V_{DS} characteristics of devices with two Al mole fractions (x): 23.5% and 25% at $V_{GS} = -4V$ and 0V is illustrated in figure 74.

At $V_{GS} = 0V$ (open channel) and at $V_{GS} = -4V$ (subthreshold regime) the gate leakage current of devices from wafer J with Al mole fraction of 23.5% is higher than the one of the devices from wafer I with 25% Al content. The curves for $-4 < V_{GS} < 0V$ were not added to the plot of figure 49 to make it more easy to analyze the difference between devices with different Al contents.

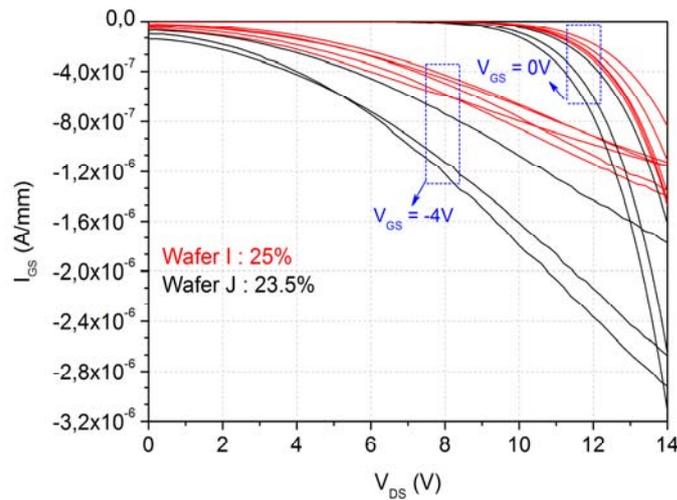
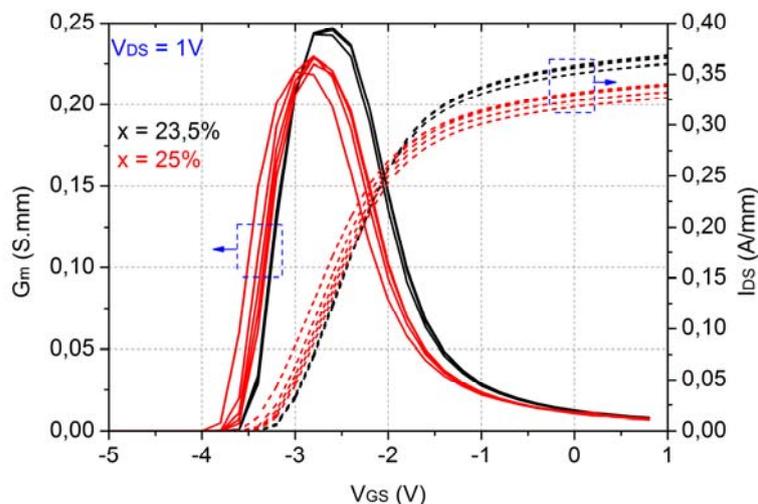


Figure 74. I_{GS} - V_{DS} of virgin AlGaIn/GaN HEMTs with Al mole fraction (x) of 23.5% and 25% at $V_{GS} = -4V$ and $0V$

3.3.2.3 Transfer and transconductance characteristics

The drain-source current and the transconductance characteristics with the gate-source voltage at $V_{DS} = 1V$ and $V_{DS} = 10V$ for $x = 23.5\%$ and 25% are shown in figure 75.

The threshold voltage of J devices at $V_{DS} = 1V$ is $-3.1V$ and for I devices is around $-3.3V$. The higher the Al content of AlGaIn layer is, the more negative the threshold voltage is [Chattopadhyay 2006]. The drain current at $V_{DS} = 1V$ at open channel is higher for J devices with 23.5% of Al content as well as the transconductance G_{mmax} that is $243mS/mm$ for J devices and $230mS/mm$ for I devices. At $V_{DS} = 10V$ and $V_{GS} = 1V$, there is no difference in the drain current that is around $890 mA/mm$ for all samples and in the G_m peak that is about $290 mS/mm$. The G_m peak at high drain-source voltage is not sensitive to the small difference in Al content of the AlGaIn barrier.



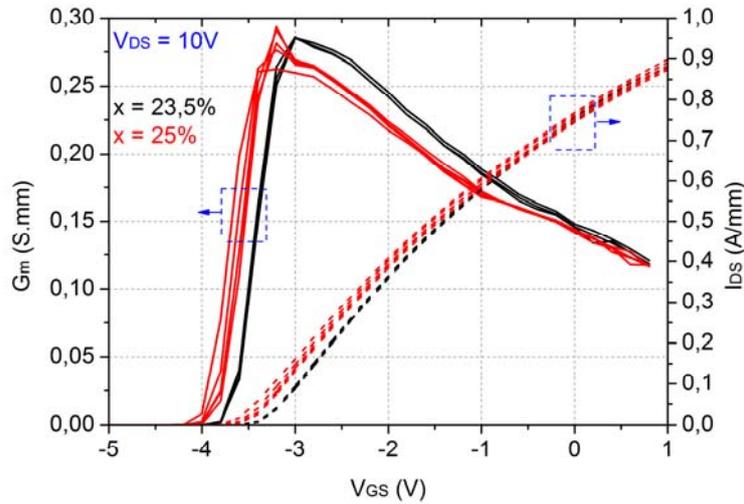


Figure 75. I_{DS} - V_{GS} and G_m - V_{GS} at $V_{DS} = 1V$ and $10V$ for virgin samples with Al mole fraction (x) of 23.5% and 25%

3.3.2.4 Subthreshold leakage current

The subthreshold drain current characteristics are plotted in logarithmic scale vs. the gate-source voltage at $V_{DS} = 1V$ for Al mole fraction of 23.5% (black) and 25% (red) in figure 76. The subthreshold drain leakage current increases in the subthreshold regime for all samples. It is higher for devices with Al content of 23.5% than for devices with 25% of Al content in AlGa_N barrier. For example at $V_{GS} = -10V$, $I_{DSleak} = 0.78 \mu\text{m}/\text{mm}$ for J devices and $I_{DSleak} = 0.35 \mu\text{m}/\text{mm}$ for I devices.

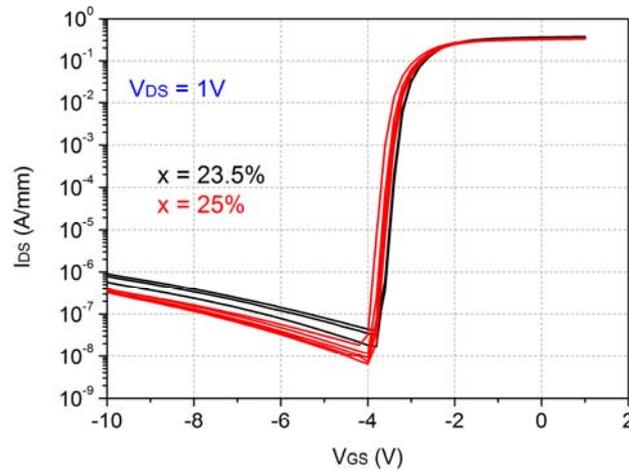


Figure 76. The drain current in logarithmic scale vs gate-source voltage (x) for virgin devices with Al mole fraction of 23.5% and 25%

3.3.3 Study of virgin samples with temperature

Typical samples of the two sets with Al mole fractions of 23.5% and 25% were characterized for temperature range 105K-405K to study the influence of temperature on the strained AlGa_N layer with different Al contents.

3.3.3.1 Schottky diode characteristics

The input I_G - V_{GS} characteristics were measured at $V_{DS} = 0V$ in forward and reverse modes from 105K to 420K with a step of 25K for two representative devices with 23.5% and 25% Al contents. Figure 77 illustrates the measured gate characteristics in forward bias.

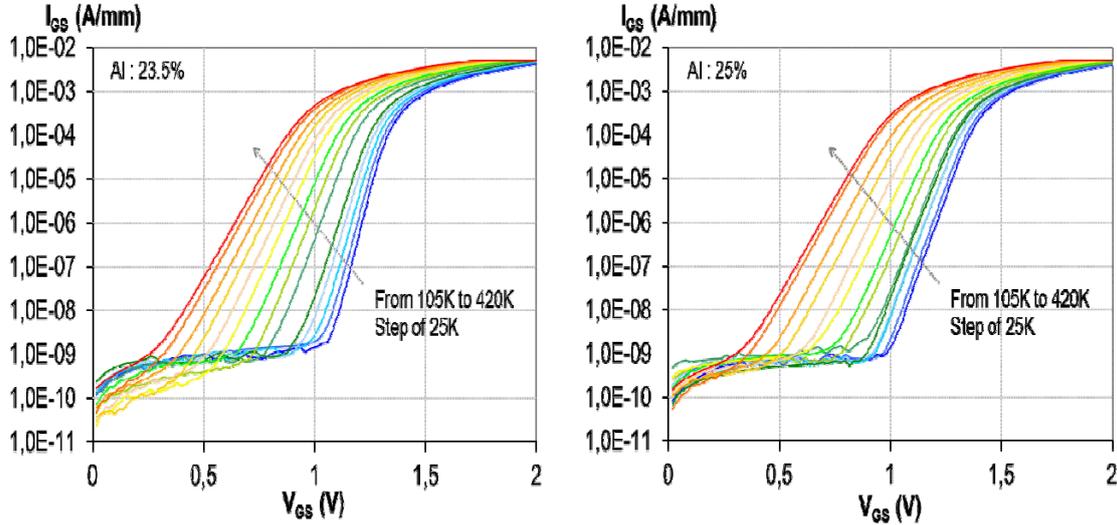


Figure 77. I_G - V_{GS} at $V_{DS} = 0V$ in forward bias for virgin samples with Al mole fraction (x) of 23.5% and 25% for temperature range 105K – 420K

The ideality factor and the Schottky barrier height extracted over two decades for a gate current from $0.1\mu\text{m}/\text{mm}$ to $10\mu\text{m}/\text{mm}$ with Al mole fraction of 23.5% and 25% for temperature range of 105K-405K is shown in figure 78.

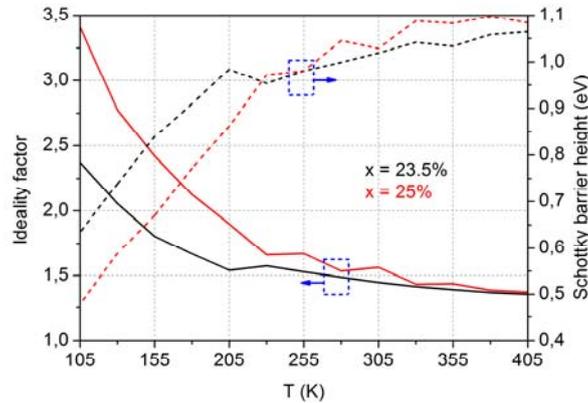


Figure 78. Ideality factor and Schottky barrier height for virgin devices with Al mole fraction (x) of 23.5% and 25% for temperature range 105K-405K

For temperature range 105K-230K, the ideality factor of the sample with 25% of Al content is higher than the one with 23.5% of Al content, where the Schottky barrier height is lower for the first sample compared to the second one which is consistent with the evolution of the ideality factor. The ideality factor and the SBH are weakly dependent on x from 255K to 405K.

The measured I_G - V_{GS} characteristics at $V_{DS} = 0V$ in reverse bias from 105K to 420K of two representative devices of wafers I and J are shown in figure 79. The gate reverse current of the gate-source/drain diodes remains higher for the studied temperature range for the device with 23.5% of Al content than the one with 25% as was seen at ambient temperature. The reverse bias leakage current is nearly independent of temperature from 105K to 205K for the device with $x = 23.5\%$, and up to 180K for the second device, which suggests that tunneling is the dominant source of current transport at low temperatures. The current density of AlGaN/GaN HEMT diode is described as function of the electric field in the barrier, which is then calculated as a function of the bias voltage. In this approach, the current density model is known as Fowler-Nordheim tunneling model.

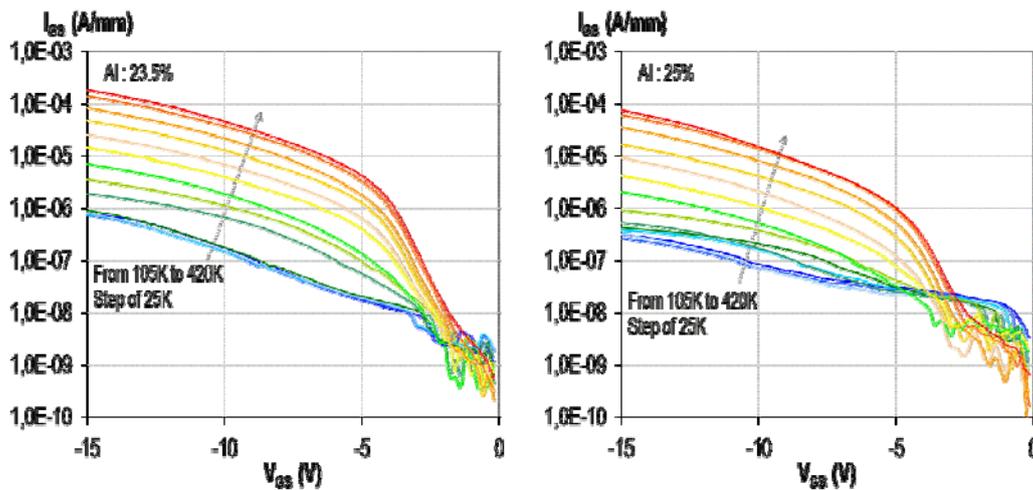


Figure 79. I_G - V_{GS} at $V_{DS} = 0V$ in reverse bias for virgin samples with Al mole fraction (x) of 23.5% and 25% for temperature range 105K – 420K

In case of current density depends on both electric field and temperature, the transport model that would satisfy these criteria among others would be Poole-Frenkel emission. This mechanism refers to electric-field-enhanced thermal emission from a trap state into a continuum of electronic states.

3.3.3.2 Drain current output characteristics

The measured I_{DS} - V_{DS} characteristics for the temperature range of 105K – 405K with two sweeps of V_{DS} from 0 to 14V and from 14V to 0V revealed that the kink effect appears on the characteristics at low temperatures and it disappears as much as the temperature increases as shown in figure 80. The kink effect appears for all the values of V_{GS} at 105K except for $V_{GS} = 0V$, and higher the temperature, more negative is the V_{GS} value at which the kink effect appears. By increasing the temperature, an overshoot as well appears for values of V_{GS} for which the kink effect has disappeared. At 405K, the I_{DS} - V_{DS} characteristics for the two sweeps of V_{DS} tend to be superimposed and both the kink and the overshoot effects disappear.

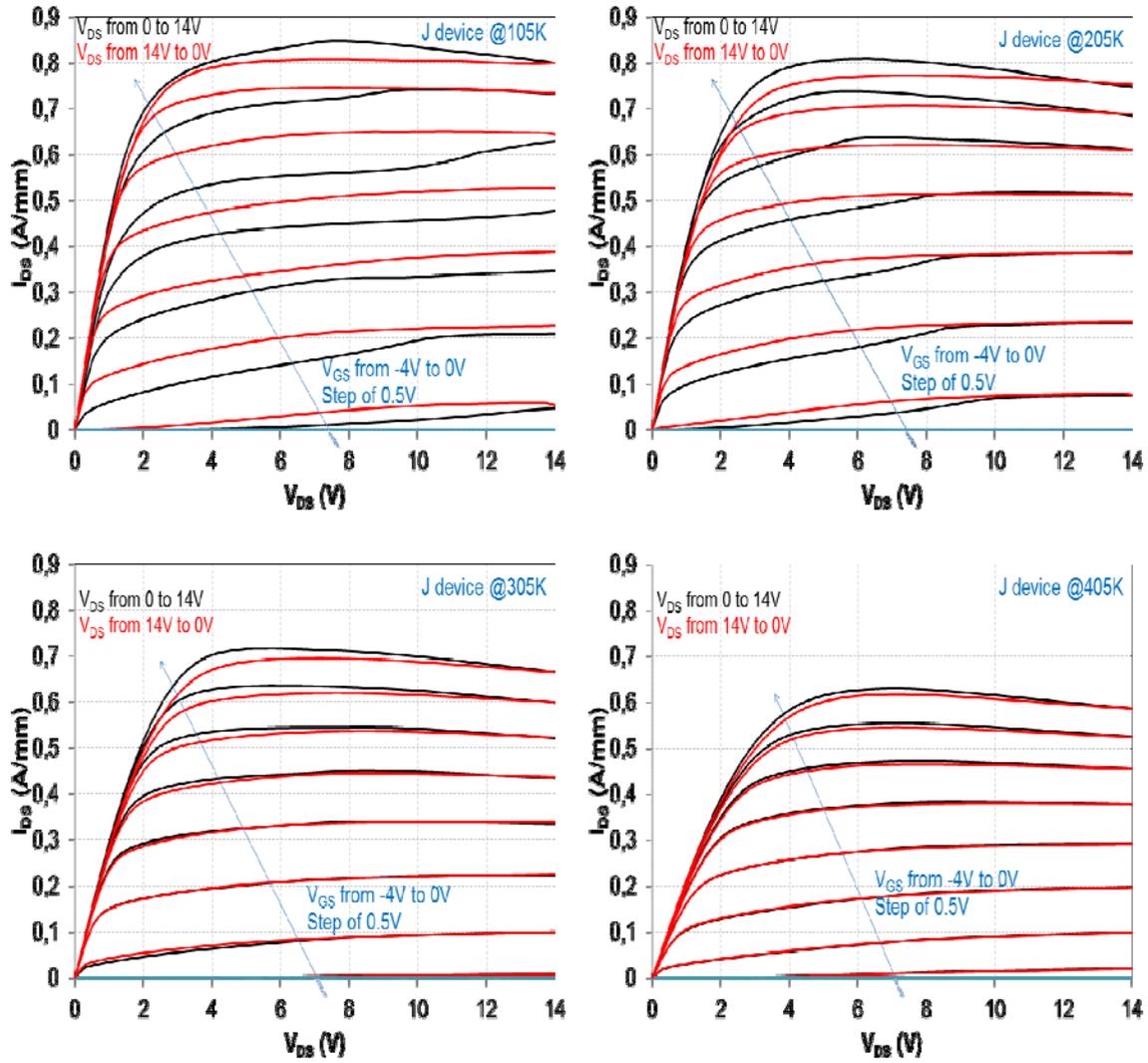


Figure 80. $I_{DS} - V_{DS}$ of J device ($x = 23.5\%$) for two sweeps increasing or decreasing of V_{DS} at 105K, 205K, 305K and 405K

The kink size of the I device at low temperatures increases at more negative values of V_{GS} where it extends to higher V_{DS} as shown in figure 81.

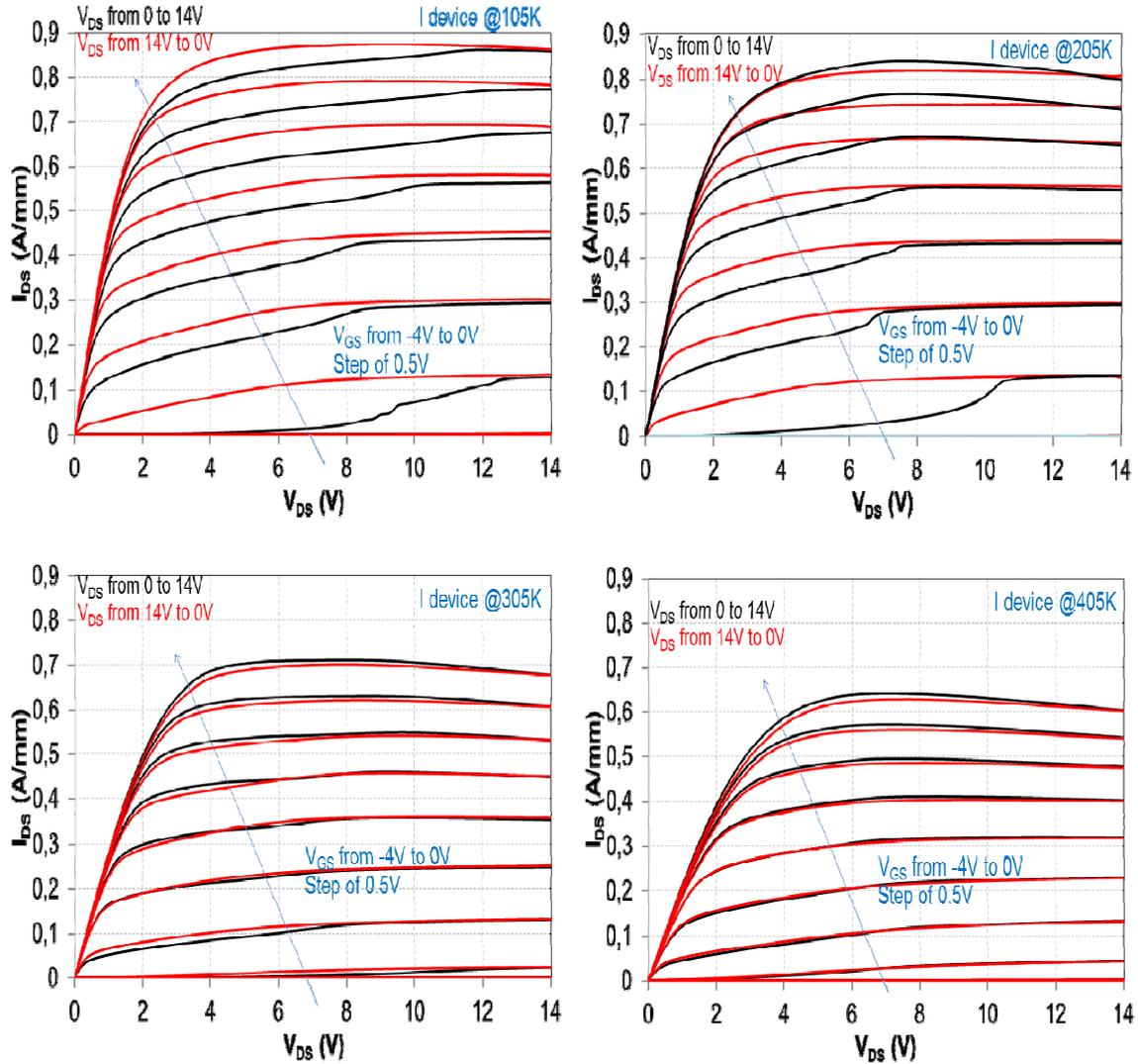


Figure 81. $I_{DS} - V_{DS}$ of representative virgin I device ($x = 25\%$) for two sweeps of V_{DS} at 105K, 205K, 305K and 405K

The kink effect disappears for both I and J devices at high temperatures. The evolution with temperature from 105K to 405K of the maximum drain current I_{DSS} at $V_{GS} = 0V$ and $V_{DS} = 10V$ and the drain-source resistance R_{DS} extracted for V_{DS} from 0V to 0.5V for two sweeps of V_{DS} from 0V to 14V and from 14V to 0V is shown in figure 82. I_{DSS} decreases and R_{DS} increases for whole temperature range for both devices. For the temperature range of 105K-280K, I_{DSS} is higher for the device with the highest Al content for the two sweeps of V_{DS} , while R_{DS} is weakly dependent on the change of Al content. Furthermore, for higher temperatures, I_{DSS} and R_{DS} of both samples do not depend much on the variation of Al mole fraction. This means that at low temperatures a small increase of Al content x of AlGaN barrier induces a significant variation of discontinuity in the conduction band and of the piezoelectric polarization; this increase in x increases the concentration of 2-DEG in the channel, while it is weakly influent at high temperatures.

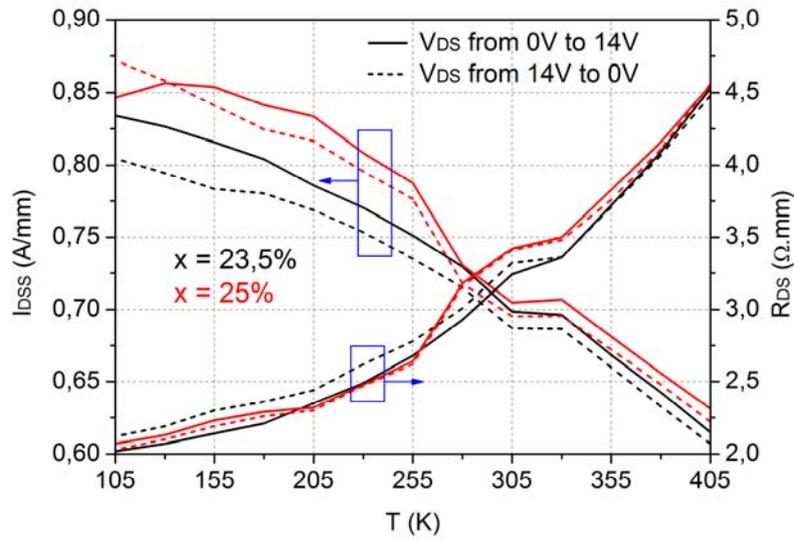


Figure 82. I_{DSS} and R_{DS} evolution with temperature for two sweeps of V_{DS} for virgin devices with Al mole fraction (x) of 23.5% and 25%

3.3.3.3 Transfer and transconductance characteristics

Figure 83 illustrates the measured drain current vs. V_{GS} and the extracted transconductance G_m curves at $V_{DS} = 1V$ from 105K to 405K for representative devices with Al mole contents of 23.5% and 25%. We notice similar changes with temperature for both devices: a negative shift of the threshold voltage (V_{TH}), a decrease of the G_m peak (G_{mmax}) and a uniform decrease of G_m at high V_{GS} . The drain current and transconductance decrease with temperature is uniform at high V_{GS} . The drain current and the transconductance evolution with V_{GS} are similar for both devices from 305K to 405K. On the other hand, the drain current and the transconductance are higher at low temperatures for the device with Al content of 25%. The concentration of the 2-DEG in the channel is influenced by a small variation of the Al content of the AlGaN barrier at low temperatures.

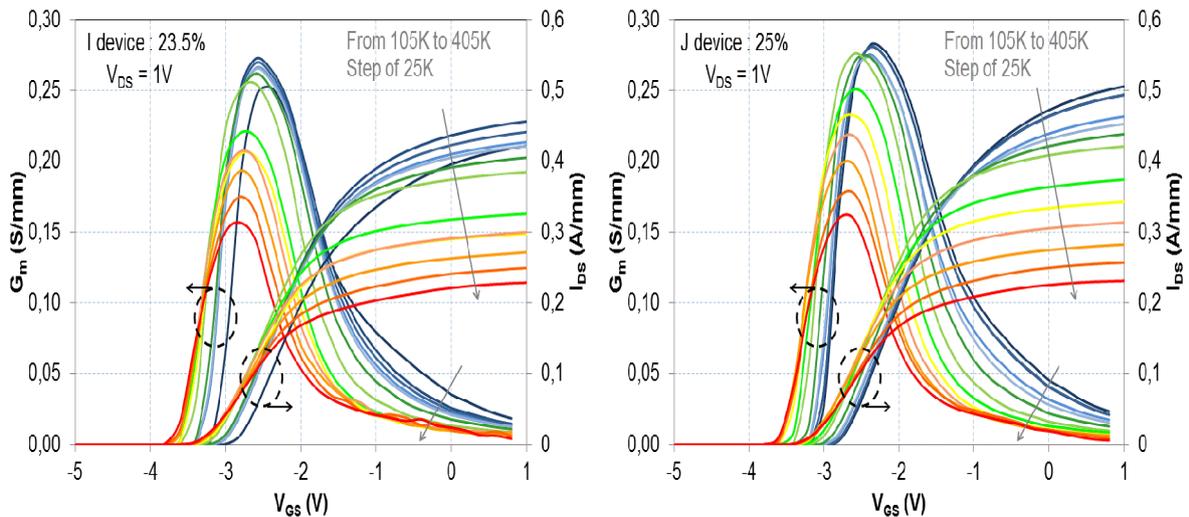


Figure 83. I_{DS} and G_m vs. V_{GS} at $V_{DS} = 1V$ from 105K to 405K for two representative virgin devices with Al mole content of 23.5% and 25%

3.3.3.4 Subthreshold leakage current

Figure 84 shows I_{DS} vs V_{GS} at $V_{DS} = 1V$ from 105K to 405K in logarithmic scale.

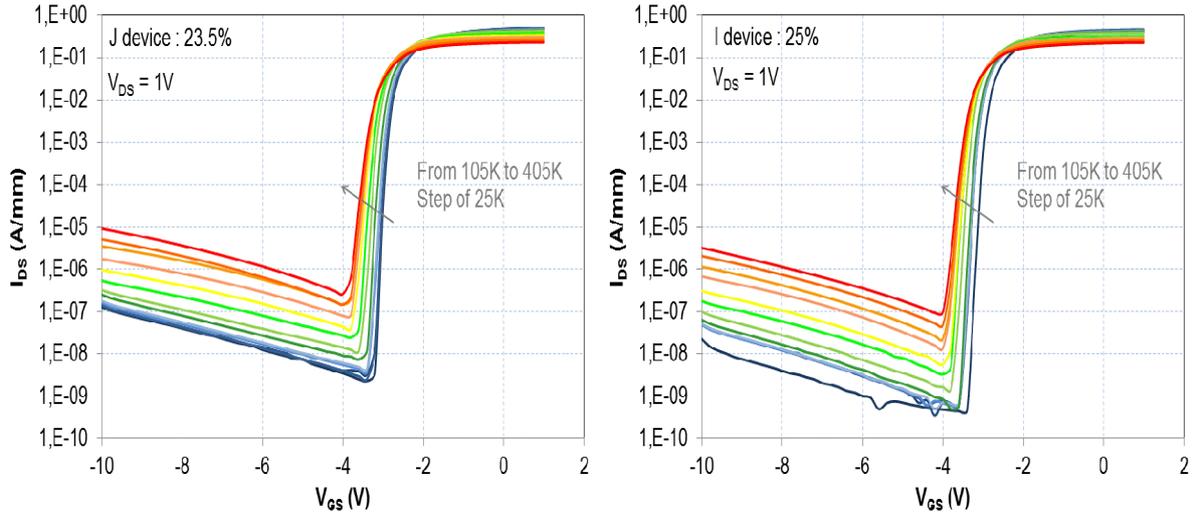


Figure 84. I_{DS} vs. V_{GS} at $V_{DS} = 1V$ from 105K to 405K

The drain subthreshold leakage current increases with temperature for both devices. On the other hand, the drain subthreshold leakage current of the device with 25% Al content remains higher than the one of the device with Al mole fraction of 23.5% in all the temperature range.

3.3.4 Comparison of aged devices with virgin ones at room temperature

For the two AlGaIn compositions, i.e., $x = 23.5\%$ and 25% , HTRB stress have been applied to samples to compare their degradation mechanisms.

3.3.4.1 Monitoring of the electrical parameters with HTRB test

Figure 85 illustrates the evolution of the electrical parameters of devices with Al mole fraction of 23.5% (red lines) and 25% (black lines) during 2200 hours of HTRB test: $V_{DS} = 30V$, $V_{GS} = -7V$, $T_C = 175^\circ C$.

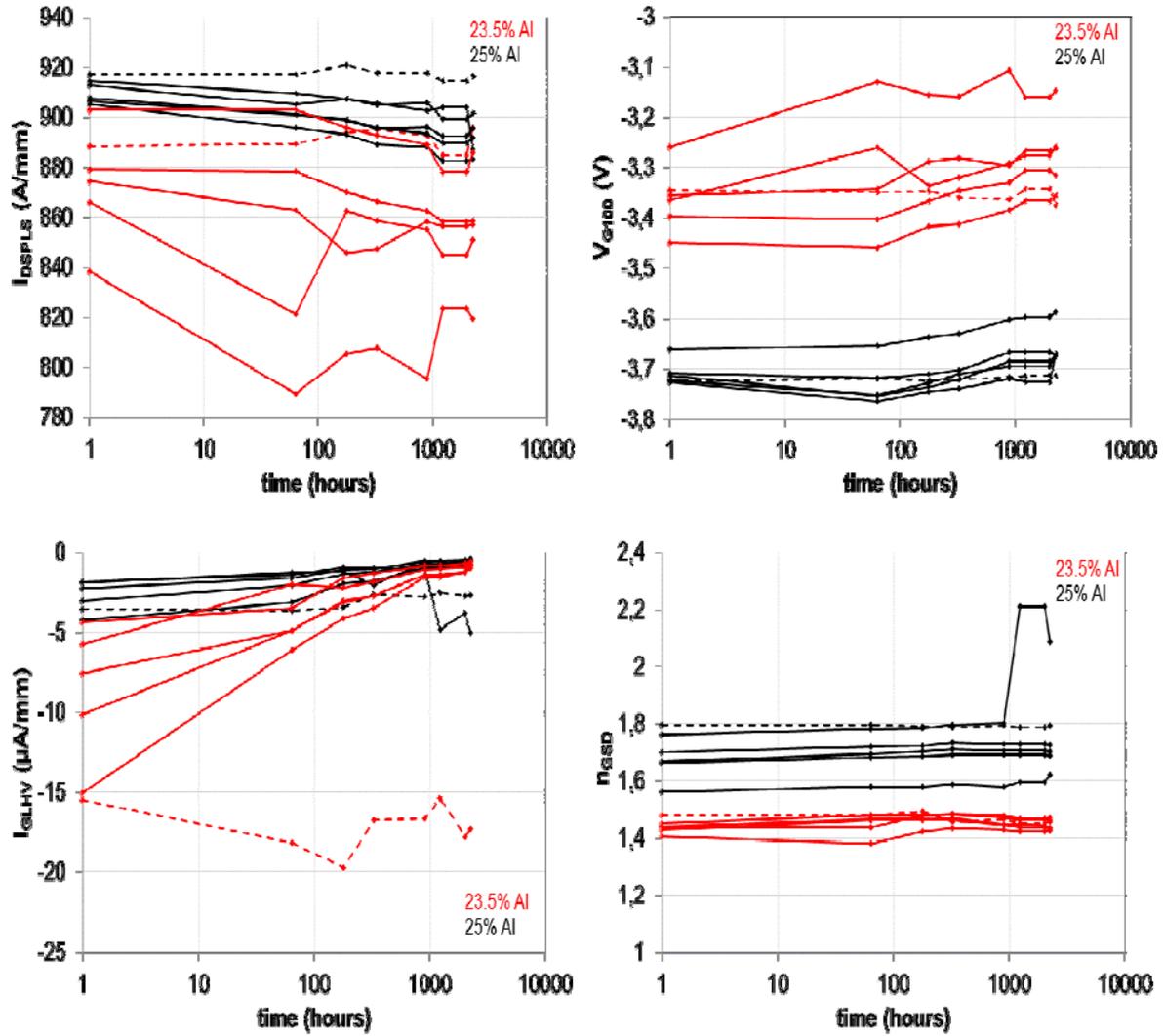


Figure 85. Evolution of I_{DSPLS} , V_{G100} , I_{GLHV} and n_{GSD} of reference (dashed line) and aged devices (continued line) of devices with 23.5% (red line) and 25% (black line) of Al content during HTRB test; $V_{DS} = 50V$; $V_{GS} = -7V$; $T_C = 175^\circ C$ during 2200 hours

Before ageing, we notice main differences between devices with 23.5% and 25% Al contents. By increasing the Al content of AlGaN layer there is an increase of I_{DSPLS} . The threshold voltage (V_{G100}) becomes more negative, the gate leakage current (I_{GLHV}) decreases and the ideality factor n_{GSD} of the Schottky diode increases.

The first recovery measurement done after 64 hours of HTRB test shows a slight decrease of I_{DSPLS} of all devices, while there is no major drift of V_{G100} and n_{GSD} . On the other hand, I_{GLHV} of devices with 23.5% of Al content decreased significantly, but its initial value was significantly higher than the one of devices with 25% of Al content.

The decrease of I_{GLHV} continues up to the end of the test to achieve values of less than $1\mu A/mm$ except for one device. The ideality factor of this atypical device increased from 1.8 at 900 hours of test to 2.5 at the end of the test. Moreover, the drift of I_{DSPLS} and V_{G100} is similar for devices for all the test time.

3.3.4.1 Schottky diode characteristics after HTRB stress

The Schottky diode characteristics in forward bias of the two sets I and J of virgin and aged samples with 23.5% and 25% of Al contents in the AlGa_N layer are shown in figure 86. The forward gate current of aged devices is lower compared to the reference one for both sets of devices. This is due to the ageing test independently of the Al mole fraction in the AlGa_N layer as shown in figure 85. The “belly shape” effect appears in the forward gate characteristic of one of the aged I devices.

The ideality factor and the Schottky barrier height (SBH) of the aged devices were extracted on two decades of I_G from $0.1\mu\text{A}/\text{mm}$ to $10\mu\text{A}/\text{mm}$ by using the thermionic emission model.

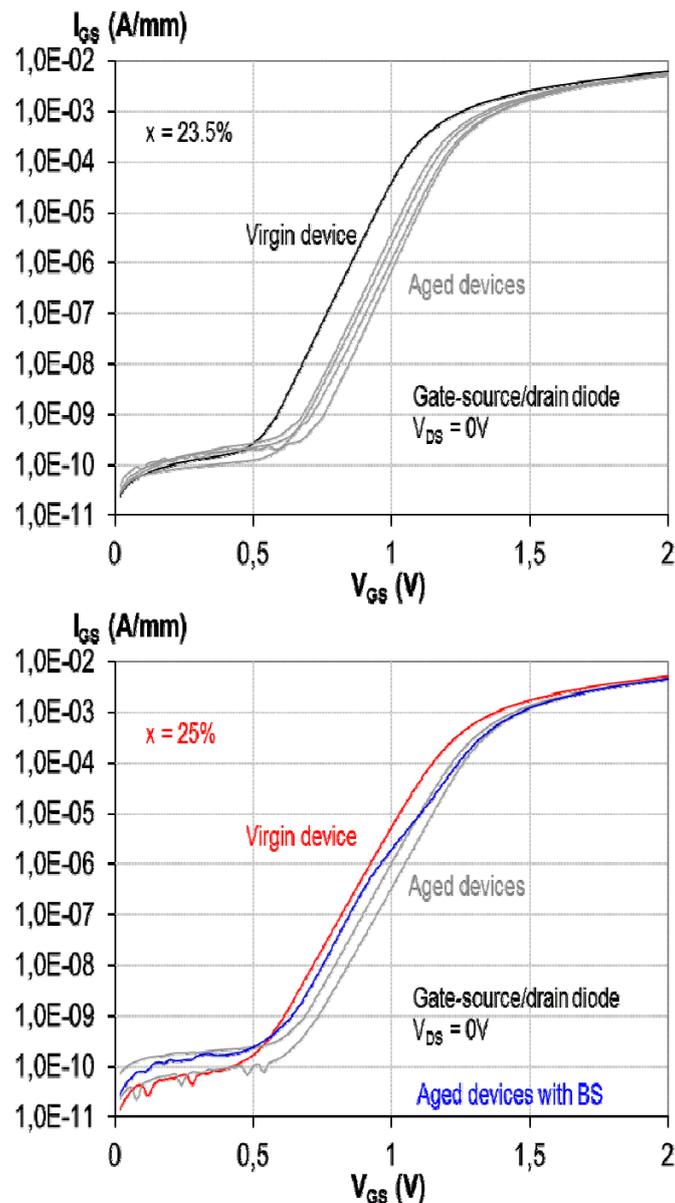


Figure 86. The Schottky gate current characteristics in forward bias vs gate-source voltage of reference and aged devices with (x) of 23.5% and 25%

The Schottky gate current characteristics in reverse bias of reference and HTRB aged devices with Al content of 23.5% and 25% are illustrated in figure 87. The gate leakage

current of the aged devices is lower to the virgin ones independently of the Al mole fraction except for the device with the “belly shape” effect. This result is independent of the Al content of AlGaN barrier.

We notice the same electrical signature of the “belly shape” effect on the atypical device of this case study compared to the studied samples aged by HTOL test of the previous case study. The gate reverse current is higher by two or three decades than the virgin one for V_{GS} between 0 and -3V and the gate current is higher for more negative V_{GS} than the one of devices without “belly shape” effect.

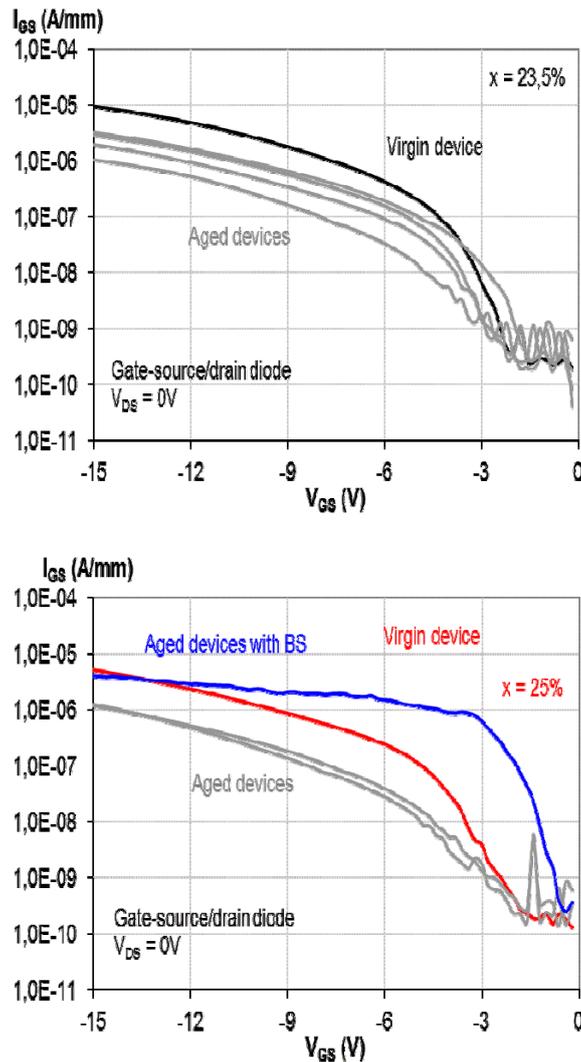


Figure 87. The Schottky gate current characteristics in reverse bias vs gate-source voltage of reference and aged devices with (x) of 23.5% and 25%

3.3.4.2 Drain current output characteristics

The drain current output characteristics and the gate leakage current of virgin and HTRB aged devices with Al content of 23.5% and 25% at $V_{GS} = 0V$ are shown in figure 88. The HTRB ageing test induced a decrease of the drain current I_{DSS} of devices with both Al contents as well as a decrease of the gate leakage current. The “runaway” phenomenon has been suppressed or delayed to higher values of V_{DS} after HTRB test. The device with “belly

shape” effect has the same maximum drain current I_{DSS} to the other aged devices. However, the gate leakage current of the device with “belly shape” effect is higher compared to the one of the other aged devices.

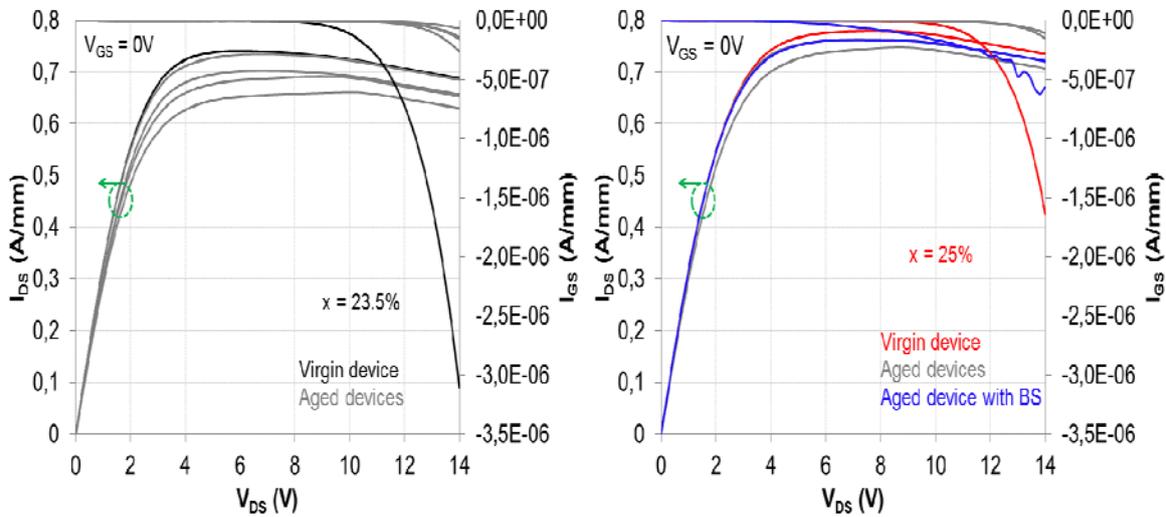


Figure 88. I_{DS} - V_{DS} and I_{GS} - V_{DS} of virgin and HTRB aged devices at $V_{GS} = 0V$ with Al content of 23.5% and 25%

3.3.4.3 Transfer and transconductance characteristics

The transfer characteristics (I_{DS} - V_{GS}) in logarithmic scale at $V_{DS} = 1V$ of virgin and HTRB aged devices with Al content of 23.5% and 25% are shown in figure 89. The HTRB stress induced a decrease of the drain subthreshold leakage current and a slight shift of the threshold voltage. An exception is for the device with “belly shape” effect for which the drain subthreshold leakage current is higher even than the one of the virgin devices.

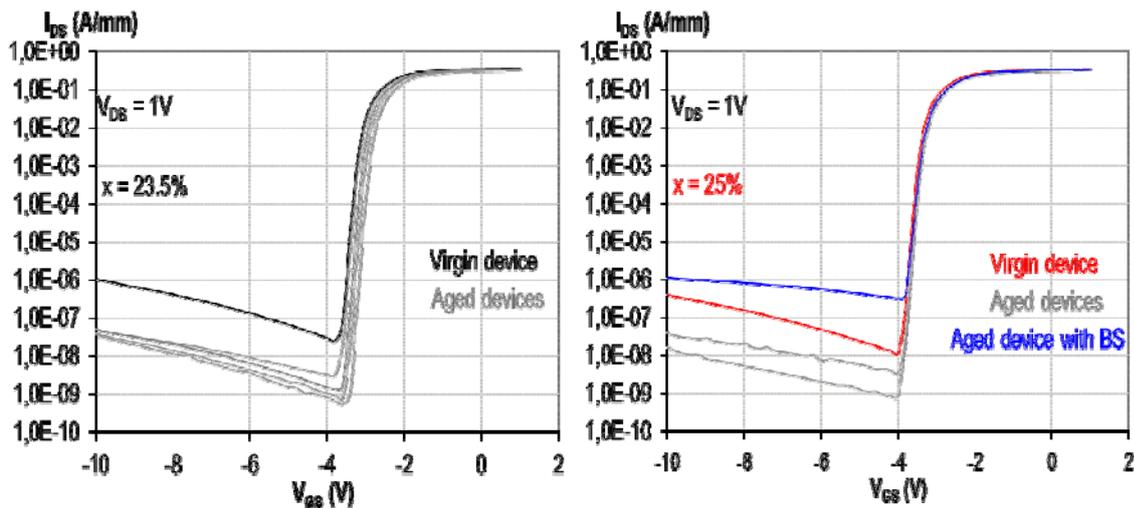


Figure 89. I_{DS} - V_{GS} of virgin and HTRB aged devices at $V_{DS} = 1V$ with Al content of 23.5% and 25%

I_{DS} - V_{GS} and G_m - V_{GS} at $V_{DS} = 1V$ of virgin and HTRB aged devices with Al mole fraction of 23.5% and 25% are shown in figure 90. We notice that the drain current of aged devices is lower than the one of virgin devices. Furthermore, the maximum transconductance

G_{mmax} of aged devices is lower than the one of virgin devices and the threshold voltage of aged devices is slightly shifted to positive values compared to the one of reference devices.

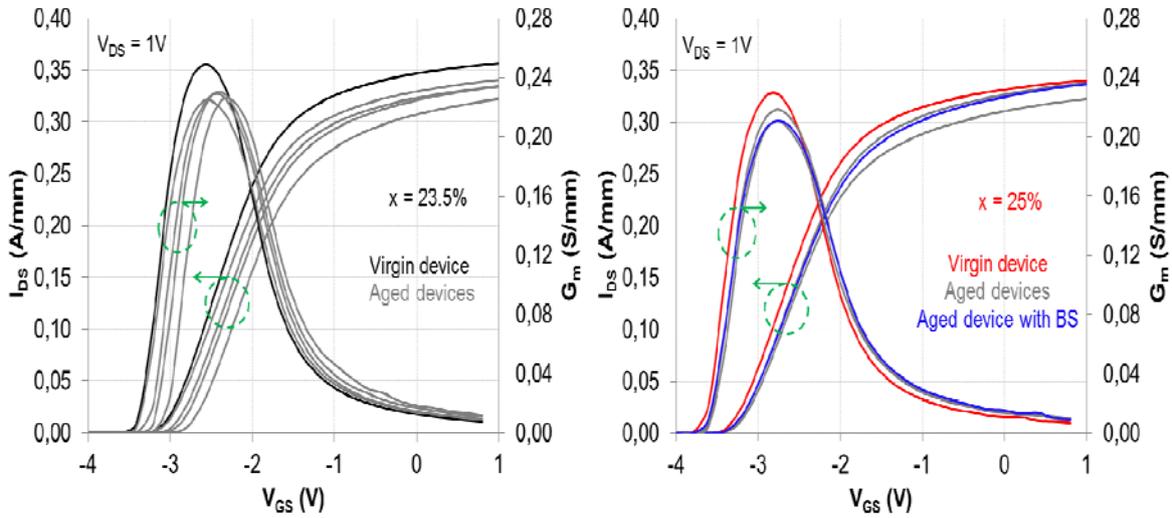


Figure 90. I_{DS} - V_{GS} and G_m - V_{GS} of virgin and HTRB aged devices at $V_{DS} = 1V$ with Al content of 23.5% and 25%

3.3.4.4 Gate and drain subthreshold leakage currents

Figure 91 shows the gate and the drain subthreshold leakage currents at $V_{GS} = -10V$ and $V_{DS} = 1V$ and $10V$ for virgin and aged devices with Al content of 23.5% and 25%. The drain-source current output characteristics and the transfer characteristics of aged devices show no significant degradation neither for the maximum drain current I_{DSS} , nor for drain-source resistance R_{DS} , nor for the threshold voltage V_{TH} . On the other hand, the subthreshold gate and drain leakage currents are lower for aged devices compared to virgin ones. The leakage current of samples with 25% of Al content remain lower than the one of samples with 23.5% of Al content except for the device with the “Belly-Shape”. The gate leakage current is higher than the drain leakage current for all virgin and aged devices. This proves that the variation of Al mole fraction has no incidence on the life time of the strained AlGaIn layer of AlGaIn/GaN HEMTs.

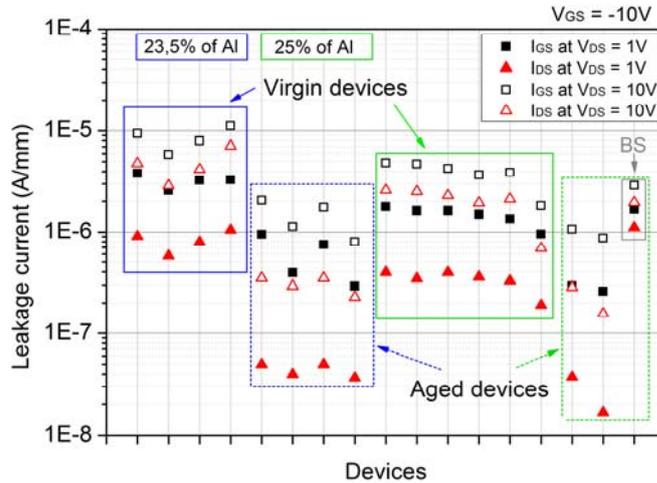


Figure 91. Gate and drain leakage current at $V_{GS} = -10V$ and $V_{DS} = 1V$ and $10V$ with Al mole fraction (x) of 23.5% and 25%

3.3.5 Dynamic on-state resistance (R_{ON}) investigation before and after HTRB test with pulsed I-V measurements

In this section, the dynamic on-state resistance (R_{ON}) in AlGaIn/GaN HEMTs is investigated by pulsed measurements. The study is done on virgin and aged devices with Al content of 25%. The reason behind this choice is that the HTRB ageing test has the same impact on devices independently of the Al content. All the pulsed I-V measurements were performed without using the bias tees.

3.3.5.1 Analysis on fresh devices

The pulsed I-V measurements at pulse widths of 300 ns and 10 μ s are superimposed, thus R_{ON} is not sensitive to time transients lower than 10 μ s as shown in figure 92.

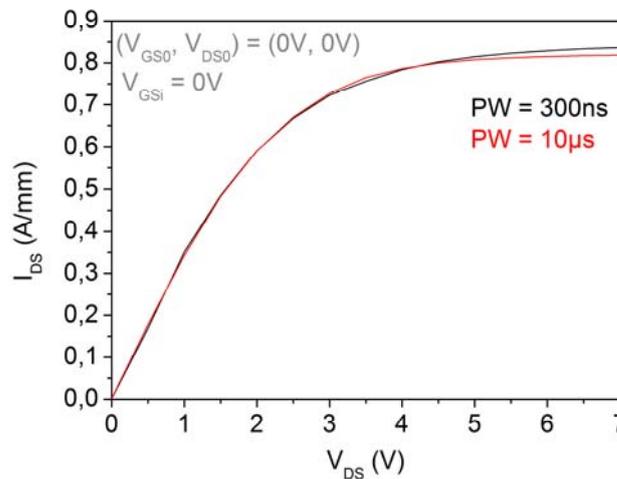


Figure 92. Pulsed I-V measurements at $(V_{GS0}, V_{DS0}) = (0V, 0V)$, PW of 300ns and 10 μ s, and duty cycle of 10%.

Figure 93 shows the measured pulsed I_{DS} - V_{DS} and G_m - V_{GS} characteristics and $I_{DS}(t)$ waveforms with PW of 300 ns and duty cycle of 10% at four quiescent bias conditions:

- (1) $(V_{GS0}, V_{DS0}) = (0V, 0V)$
- (2) $(V_{GS0}, V_{DS0}) = (-7V, 0V)$
- (3) $(V_{GS0}, V_{DS0}) = (-7V, 30V)$
- (4) $(V_{GS0}, V_{DS0}) = (-7V, 50V)$.

The pulsed I-V characteristics are plotted with the $I_{DS}(t)$ waveforms at $V_{GSi} = 0V$ and $V_{DSi} = 5V$ for each quiescent bias condition. The quiescent bias (QB) measurement is performed from 50 ns to 150 ns, while the instantaneous bias (IB) is measured from 350 ns to 450 ns. $I_{DS}(t)$ waveforms are steady in the QB and IB measurement time window. Furthermore, the pulsed I-V characteristics indicate that the studied sample is sensitive to the gate-lag and to the drain-lag with the latter effect more pronounced at high V_{DS0} .

R_{ON} is higher by 11% for $(V_{GS0}, V_{DS0}) = (-7V, 0V)$ than for $(-0V, 0V)$. As well, R_{ON} is higher by about 50% for $(V_{GS0}, V_{DS0}) = (-7V, 30V)$ than for $(-7V, 0V)$ and it is doubled for $(V_{GS0}, V_{DS0}) = (-7V, 50V)$ compared to its value at $(-7V, 0V)$.

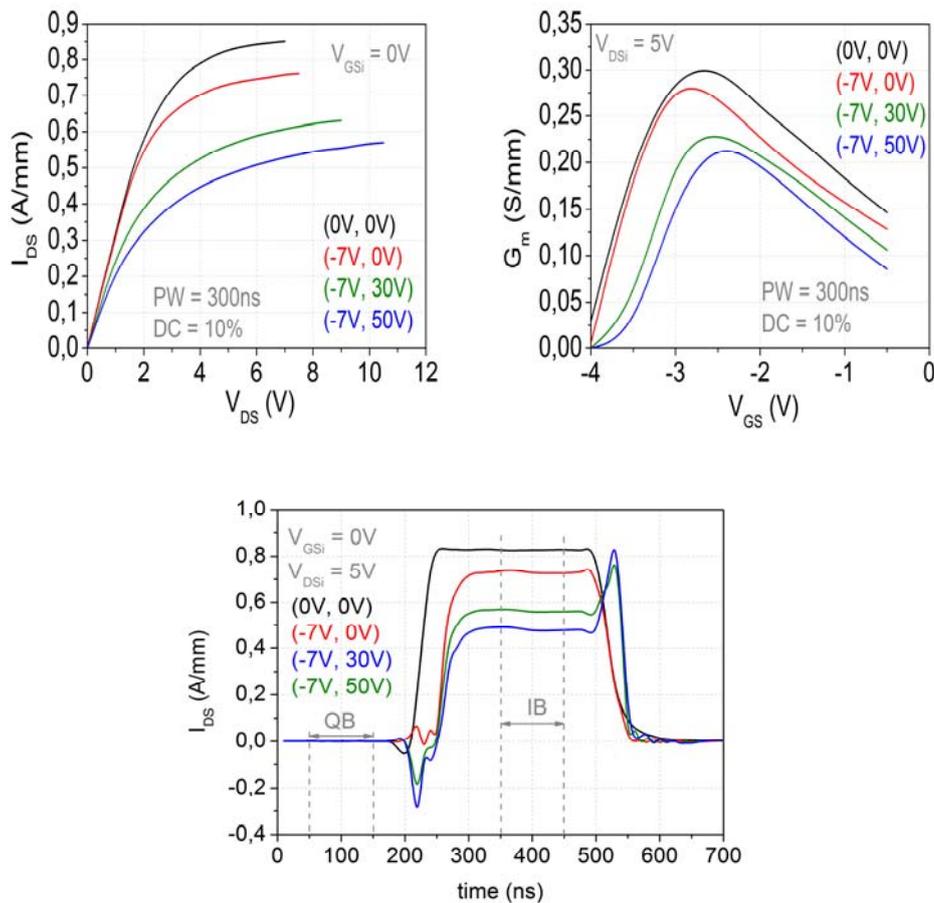


Figure 93. (a) Pulsed I-V measurements at $(V_{GS0}, V_{DS0}) = (0V, 0V)$, $(-7V, 0V)$, $(-7V, 30V)$ and $(-7V, 50V)$ at PW = 300ns & $V_{GSi} = 0V$ (b) $I_{DS}(t)$ waveforms at $V_{GSi} = 0V$ & $V_{DSi} = 5V$

The comparison of the transconductance (G_m) vs. V_{GS} measured in conditions (1) and (2) shows that: the threshold voltage V_{TH} under both conditions is superimposed, G_m peak and G_m at high V_{GS} are lower for condition 2 ($(V_{GS0}, V_{DS0}) = (-7V, 0V)$).

Moreover, we notice a higher value of V_{TH} and a lower G_m peak and G_m at high V_{GS} for conditions (3) and (4) compared to condition (2).

The variation of R_{ON} in the quiescent bias condition of $(V_{GS_OFF}, V_{DS_HIGH})$ has been reported by Meneghini et al. [Meneghini 2014] to be related to traps in the access region as no variation on V_{TH} has been noticed. In our case, both variations of R_{ON} and V_{TH} under $(V_{GS_OFF}, V_{DS_HIGH})$ conditions are noticed which suggests that the increase of R_{ON} is related to traps beneath the gate or in the vicinity of the gate.

3.3.5.2 Analysis on HTRB aged devices

As the higher V_{DS0} for the condition (V_{GS_OFF}, V_{DS0}) , the higher R_{ON} , HTRB ageing test at $V_{DS} = 30V$ and $V_{GS} = -7V$ carried out during 2200 hours is supposed to give more insight on the physical location of trapping effects causing R_{ON} variation. Four typical devices were submitted to HTRB test.

Figure 94 illustrates pulsed I_{DS} - V_{DS} characteristics of a reference and aged devices at $V_{GSi} = 0V$ and $(V_{GS0}, V_{DS0}) = (0V, 0V)$, $(-7V, 0V)$, $(-7V, 30V)$ and $(-7V, 50V)$, PW of 300ns and duty cycle of 10%. The aged devices present significant gate-lag and drain-lag effects. A current collapse is noticed for aged devices under the four studied conditions.

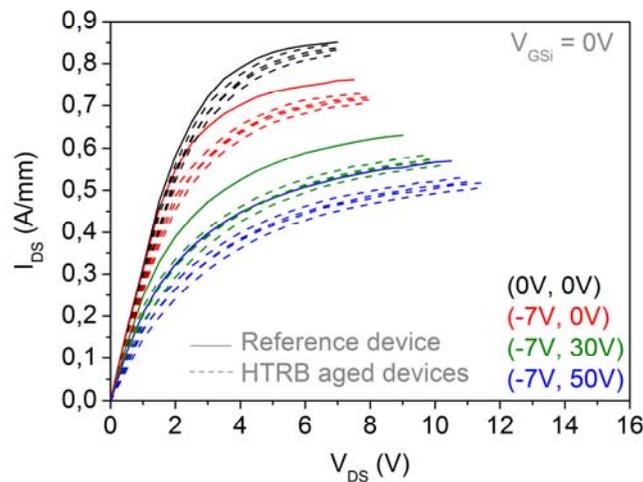


Figure 94. Pulsed I-V curves of reference and HTRB aged devices at $(V_{GS0}, V_{DS0}) = (0V, 0V)$, $(-7V, 0V)$, $(-7V, 30V)$ and $(-7V, 50V)$, PW of 300ns, and DC of 10% and $V_{GSi} = 0V$.

The extracted R_{ON} with the mean values and standard deviation of aged devices are reported in figure 95. The mean R_{ON} of aged devices compared to the reference one is higher by 10% with a deviation of $\pm 5\%$ at condition (1). For the condition (2), the mean R_{ON} is above the one of the reference device by 14% with a deviation of $\pm 6\%$. In the conditions (3) and (4), the mean R_{ON} compared to the reference one is higher by 22% with a standard deviation of $\pm 17\%$.

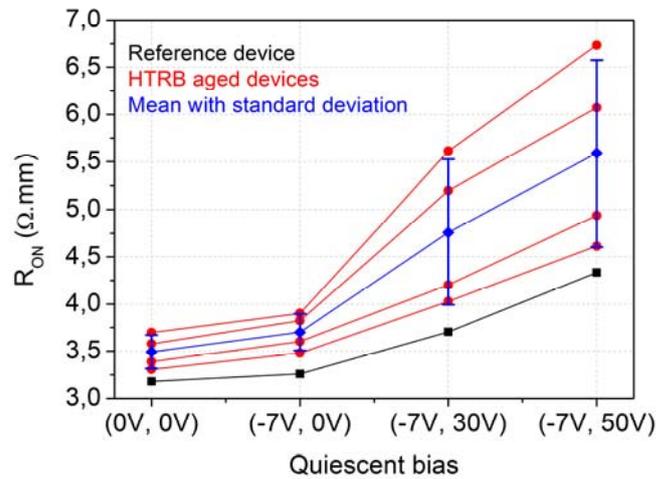


Figure 95. Dynamic on-state resistance of reference and HTRB aged devices at $(V_{GS0}, V_{DS0}) = (0V, 0V), (-7V, 0V), (-7V, 30V)$ and $(-7V, 50V)$, PW of 300ns, and DC of 10%

As HTRB test is basically operated to evaluate the stability and the quality of the Schottky contact, we assume that the increase of R_{ON} in off-state condition with higher V_{DS} is related to traps and/or defects located in the vicinity of the gate.

The pulsed G_m vs. V_{GS} characteristics of reference and aged devices at $V_{DS} = 5V$ at the studied quiescent bias conditions are reported in figure 96. The G_m vs. V_{GS} characteristics of the aged devices have the same evolution with (V_{GS0}, V_{DS0}) as the reference device. A slight decrease of G_m peak is noticed at $(0V, 0V)$, while a significant drop of G_m peak is recorded at $V_{GS0} = -7V$ and V_{DS0} of 0, 30 and 50V. On the contrary to R_{ON} dispersion of aged devices shown in figure 94, V_{TH} has the same value for all aged devices.

As the threshold voltage V_{TH} of aged devices has not shifted during the HTRB ageing test, trapping effects responsible for the increase of R_{ON} are rather more located in the gate-source and drain-source access regions than under the gate.

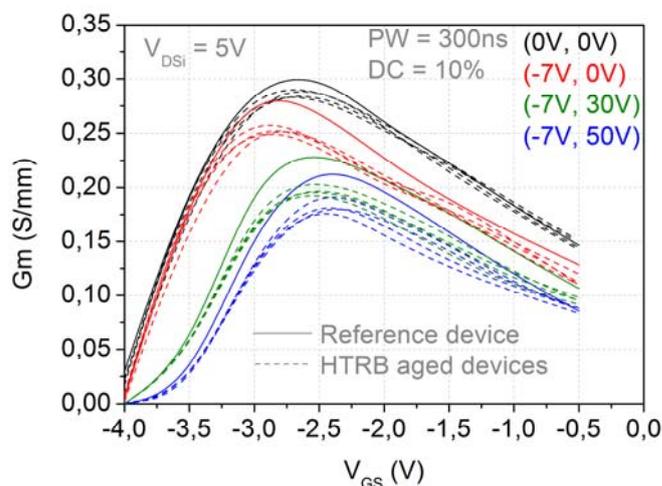


Figure 96. Pulsed G_m characteristics at $V_{DS} = 5V$, PW = 300ns, at $(V_{GS0}, V_{DS0}) = (-0V, 0V), (-7V, 0V), (-7V, 30V)$ and $(-7V, 50V)$, PW of 300ns, and DC of 10%

Conclusion of case study 3: link with ReAGaN project

AlGaIn/GaN HEMTs with strained AlGaIn layer of 23.5% and 25% Al content have been characterized at room temperature and for temperature range 105K – 405K. The variation of the Al content from 23.5% to 25% at 300K increases the ideality factor but decreases the gate and the drain subthreshold leakage currents and the threshold voltage becomes more negative.

For low temperatures, samples with 25% Al content present higher maximum drain current I_{DSS} than the one with 23.5% of Al mole fraction, but I_{DSS} is weakly dependent of the Al content at high temperature.

Al content	300K		From 105K to 405K	
	23.5%	25%	23.5%	25%
Ideality factor	-	higher	-	Higher from 105K to 305K similar from 325K to 405K
Barrier height	similar	similar	Higher from 105K to 255K similar from 280K to 405K	-
Subthreshold leakage current	higher	-	higher	-
I_{DSS}	similar	similar	-	Higher from 105K to 280K similar from 305K to 405K
G_{mmax}	similar	similar	similar	similar
V_{TH}	-	More negative	-	More negative

Table 10. Comparison of parameters of devices with 23.5% and 25% Al content at room temperature and from 105K to 405K

The 2200 hours HTRB test applied on both I and J lots of devices has induced identical degradation independently of the Al mole fraction in AlGaIn layer. Indeed, the decrease of the forward gate current, and of the gate and drain subthreshold leakage currents occur for all aged devices. It has been observed that the Al mole fraction has no impact on the lifetime of the devices.

R_{ON} is higher by 11% for $(V_{GS0}, V_{DS0}) = (-7V, 0V)$ than for $(0V, 0V)$. As well, R_{ON} is higher by about 50% for $(V_{GS0}, V_{DS0}) = (-7V, 30V)$ than for $(-7V, 0V)$ and it is doubled for $(V_{GS0}, V_{DS0}) = (-7V, 50V)$ compared to its value at $(-7V, 0V)$. As both variations of R_{ON} and V_{TH} under $(V_{GS_OFF}, V_{DS_HIGH})$ conditions are noticed, the increase of R_{ON} is related to traps beneath the gate or in the vicinity of the gate.

The threshold voltage V_{TH} of aged devices has not shifted during the HTRB ageing test carried out during 2200 hours. Therefore, trapping effects responsible for the increase of R_{ON} are rather more located in the gate-source and drain-source access regions than under the gate.

3.4. Case study 4: Breakdown voltage mechanisms

3.4.1 Purpose of the case study

The purpose of this case study is to investigate the voltage operation limits of the UMS GH25_10 GaN technology. This work consisted in studying the electrical behavior and the dispersion of the electrical parameters of the studied transistors, also to assess the two and three terminal breakdown mechanisms at room and at high temperatures. This work is performed in the frame of the Extreme GaN project that aims to investigate and define the capability of the GH25_10 GaN technology to operate in extreme conditions for missile application.

GaN based HEMTs from the GH25_10 UMS GaN technology have been characterized by dc I-V measurements as well as two and three terminal breakdown measurements at room temperature and from 50°C to 150°C. The devices present two gate geometries of $0.25\mu\text{m} \times W_G$, with $W_G = 1\text{mm}$ and 1.2mm .

3.4.2 DC I-V characteristics at room temperature

Figure 97 shows Schottky gate forward characteristics of AlGaIn/GaN HEMTs with three different integration times. The integration time which can be small ($S = 4\text{ ms}$), medium ($M = 26\text{ ms}$) or large ($L = 320\text{ ms}$), does not induce any change on the forward characteristics. The ideality factor is about 1.8 and the Schottky barrier height is about 0.88 eV.

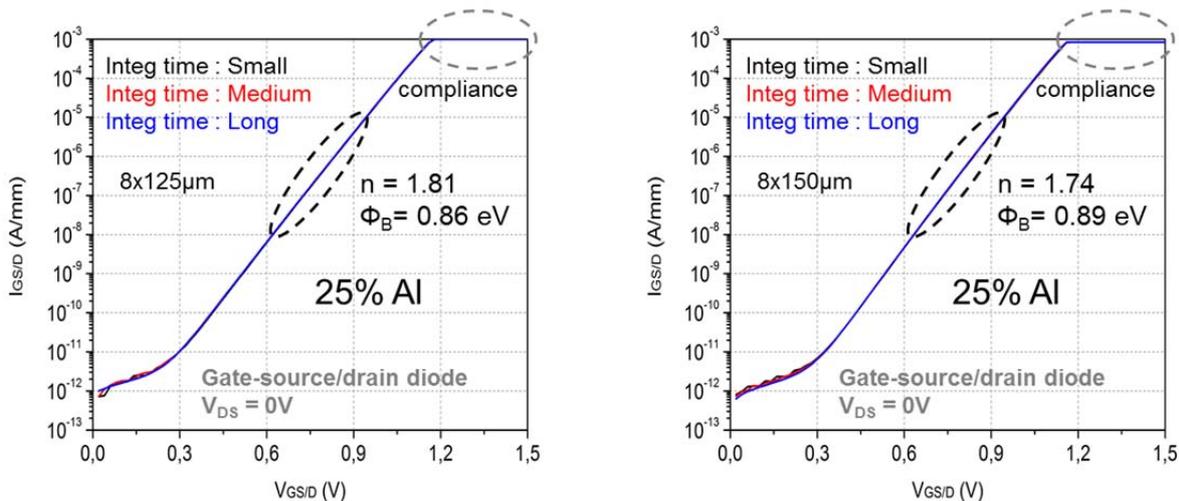


Figure 97. Forward I_G - V_{GS} characteristics of 1 mm and 1.2 mm gate width HEMTs measured with different integration times

Figure 98 shows the Schottky gate forward characteristics of gate-source diode, gate-drain diode and both diodes in parallel for the two geometries with integration time Large (L). The characteristics for the three configurations are superimposed.

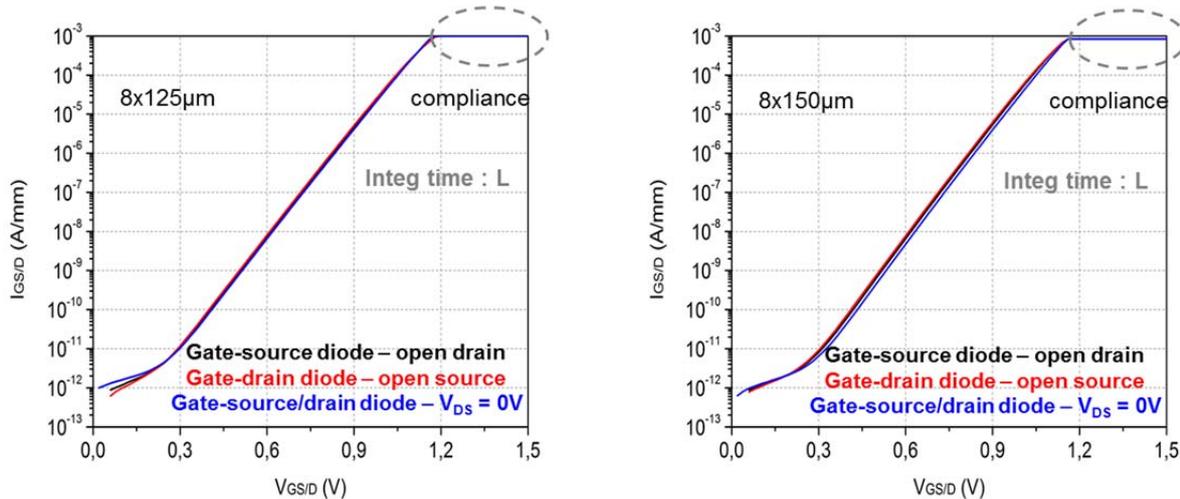


Figure 98. Forward I_G - V_{GS} characteristics of gate-source diode, gate-drain diode and both diodes in parallel of 1mm and 1.2mm gate width HEMTs.

Figure 99 shows Schottky gate reverse characteristics of the 1 mm gate geometry with three different integration times. The characteristics are shown for two sweeps of V_{GS} : from 0V to -15V and from -15V to 0V. The integration time, small (S = 4ms), medium (M = 26ms) or large (L = 320ms) does not impact on the reverse characteristics. On the other hand a shift of the zero of the reverse characteristics is noticed for V_{GS} sweep from -15V to 0V.

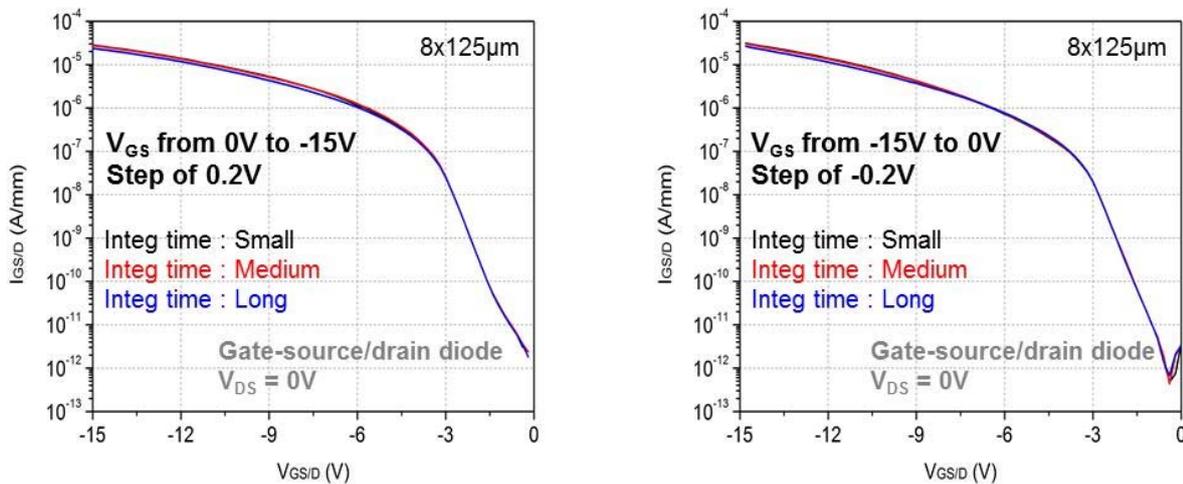


Figure 99. Reverse I_G - V_{GS} characteristics of 1mm and 1.2mm gate width HEMTs with different integration times and for two sweeps of V_{GS} .

Figure 100 shows the Schottky gate reverse characteristics of gate-source diode, gate-drain diode and both diodes in parallel. The gate leakage current of gate-drain diode is higher than the one of the gate-source diode.

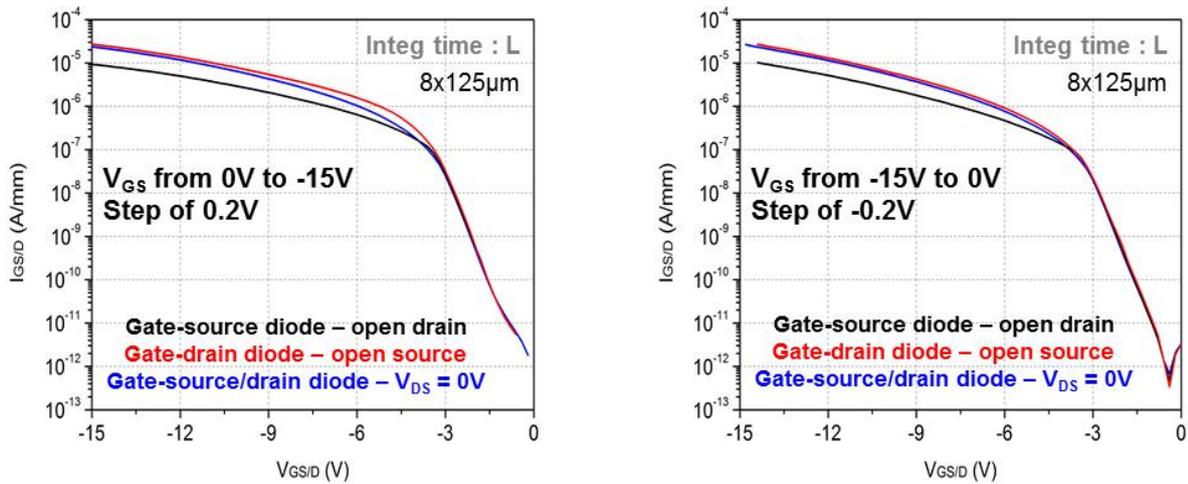


Figure 100. Reverse I_G - V_{GS} characteristics of gate-source diode, gate-drain diode and both diodes in parallel of 1mm gate width HEMTs for two sweeps of V_{GS} .

Figure 101 shows I_{DS} - V_{DS} output characteristics of two gate width devices with two sweeps of V_{DS} from 0 to 14V and from 14V to 0 and for V_{GS} from -4V to 0V. A small kink effect is noticed for the device of 1mm gate width. The average saturation drain current I_{DSS} is 700 mA/mm.

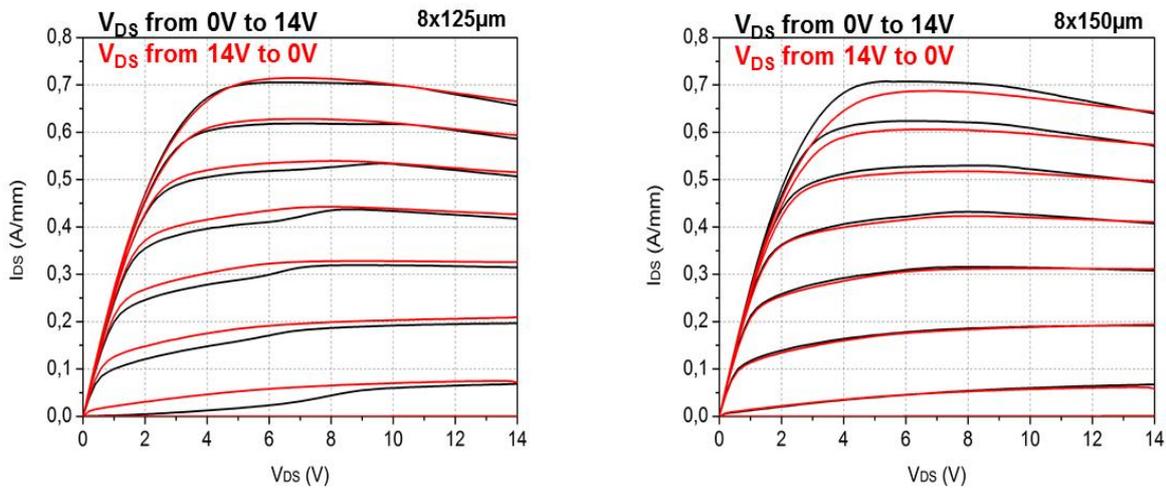


Figure 101. I_{DS} - V_{DS} characteristics up to $V_{DS} = 14V$ for V_{GS} from -4V to 0V for two sweeps of V_{DS}

Figure 102 shows I_{DS} - V_{DS} output characteristics of the two geometries with two sweeps of V_{DS} from 0 to 40V and from 40V to 0V and for V_{GS} near the threshold voltage from -4V to -2.5V. A kink effect is noticed for both samples. The drain-source voltage applied is limited by the maximum compliance of the measurement set-up. Indeed I_{DS} cannot exceed 350 mA for drain-source voltage up to 40V.

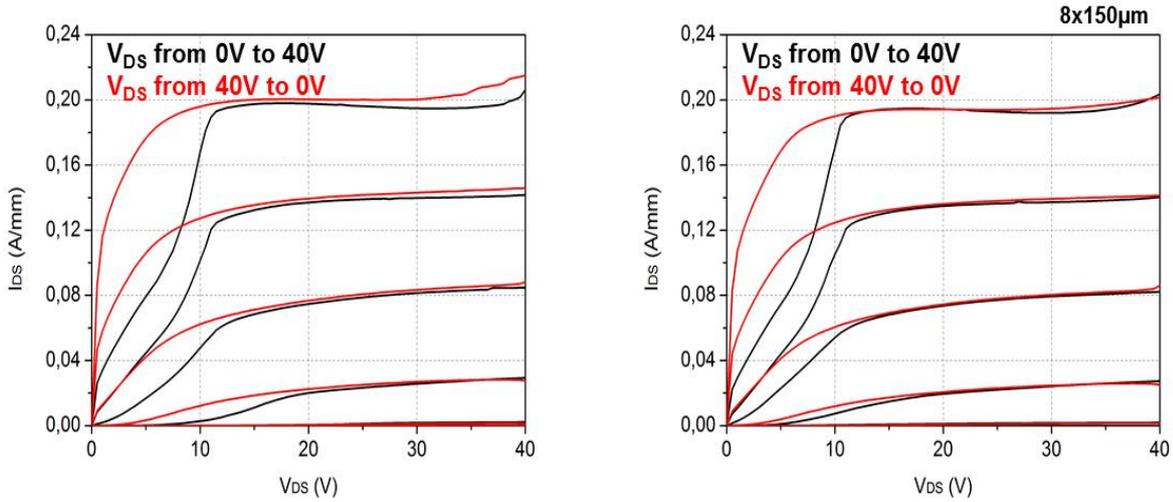


Figure 102. I_{DS} - V_{DS} characteristics up to $V_{DS} = 40V$ for V_{GS} from $-4V$ to $-2.5V$ for two sweeps of V_{DS}

Figure 103 shows I_{DS} - V_{DS} output characteristics of two gate width HEMTs with two sweeps of V_{DS} from 0 to 50V and from 50V to 0V and for V_{GS} near the threshold voltage from $-3.5V$ to $-3V$. A kink effect is noticed for both samples. The drain-source voltage applied is limited by the maximum compliance of the measurement equipment. Indeed I_{DS} cannot exceed 125mA for drain-source voltage up to 50V.

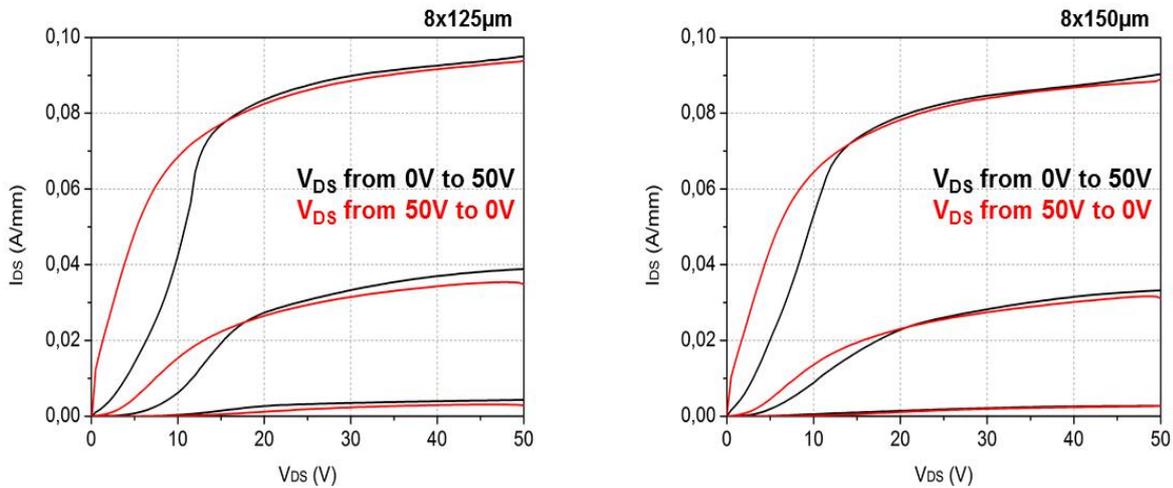


Figure 103. I_{DS} - V_{DS} characteristics up to $V_{DS} = 50V$ for V_{GS} from $-3.5V$ to $-3V$ for two sweeps of V_{DS}

3.4.2.1 Dispersion of electrical parameters

Figure 104 shows Schottky gate forward and reverse characteristics of four samples of two gate widths. The forward and reverse characteristics of the 1 mm samples are superimposed while the characteristics of the four 1.2mm samples are similar two by two.

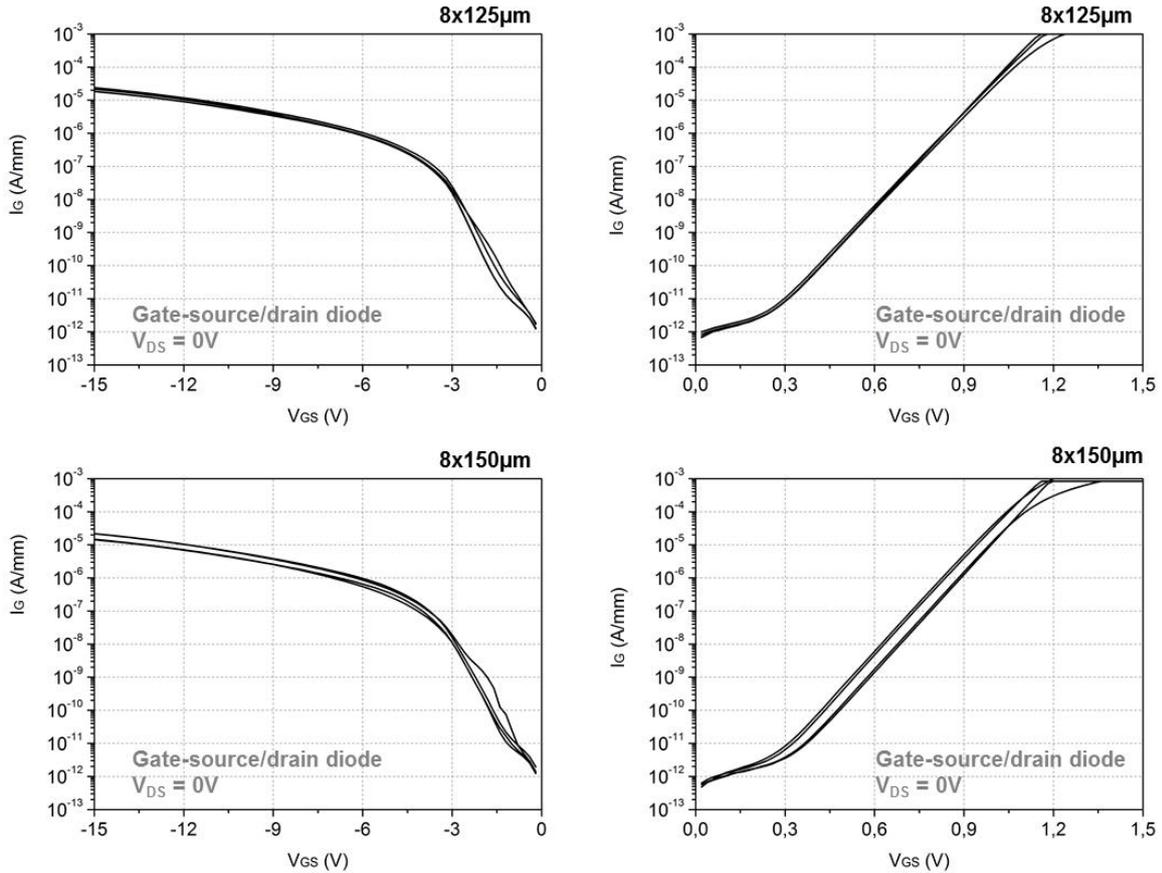


Figure 104. I_G - V_{GS} characteristics in forward and reverse bias of four samples from each geometry

Figure 105 shows I_{DS} - V_{DS} output characteristics up to $V_{DS} = 14V$ of four samples of each geometry for V_{GS} from $-4V$ to $0V$. No dispersion is noticed for the 1mm devices while a small dispersion is noticed for the 1.2mm devices.

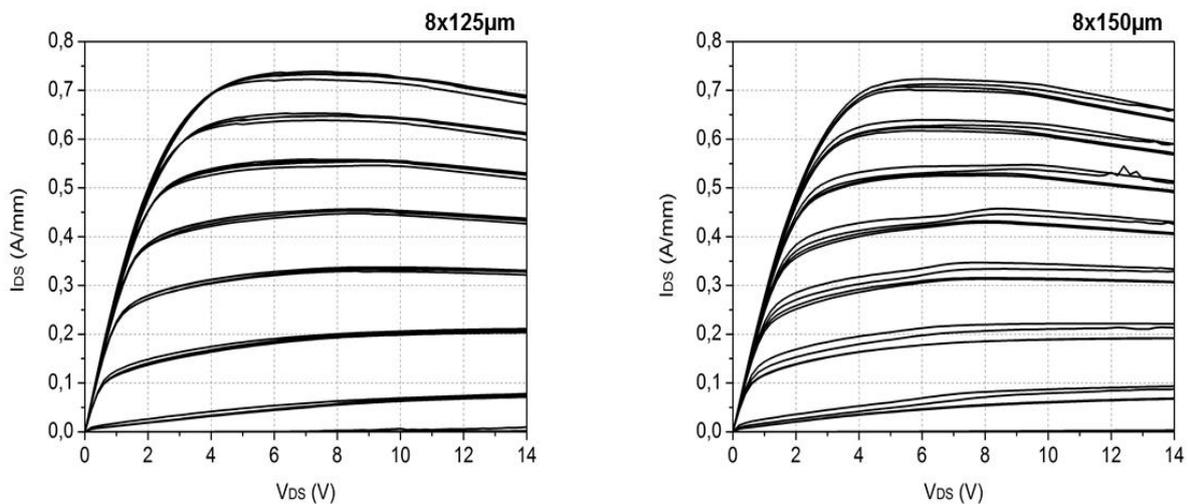


Figure 105. I_{DS} - V_{DS} characteristics up to $V_{DS} = 14V$ of four samples of each geometry

Figure 106 shows transfer characteristics in logarithmic scale at $V_{DS} = 1V$ and $10V$ of two gate width HEMTs.

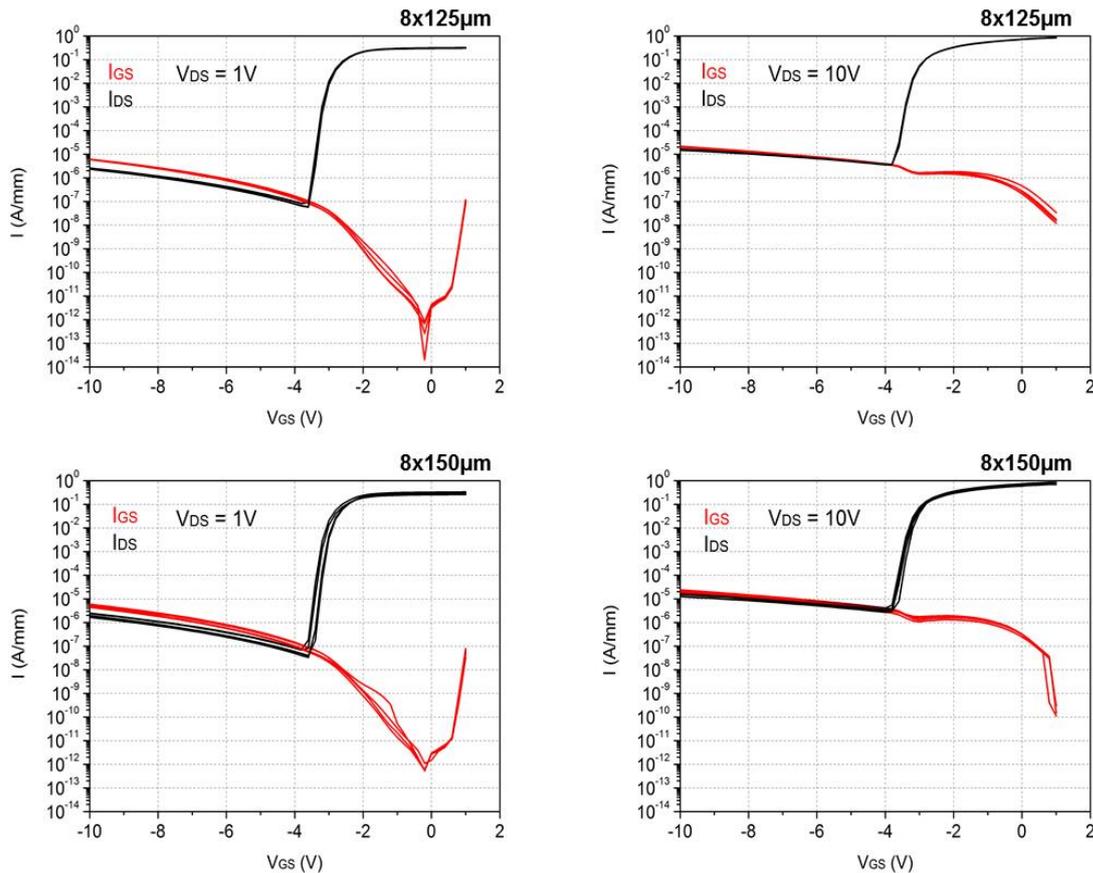


Figure 106. I_{DS} - V_{GS} and I_{GS} - V_{GS} characteristics of four samples from each gate width device at $V_{DS} = 1V$ and $10V$

All the DC characteristics of the 1mm samples are superimposed while the characteristics of the four 1.2mm samples are similar two by two.

3.4.2.2 DC I-V characteristics from 50°C to 150°C

Two samples with identical gate width were extracted from the set of eight samples that have been characterized at room temperature and have been characterized from 50°C to 150°C.

Figure 107 to 111 show the following characteristics measured from 50°C to 150°C:

- Schottky gate forward characteristics of two gate width HEMTs from. The gate forward current increases with temperature.
- Schottky gate reverse characteristics
- Drain and gate current versus V_{DS} at $V_{GS} = 0V$. The drain current decreases with temperature while it is the opposite for the gate leakage current.
- Transfer characteristics in linear scale and transconductance at $V_{DS} = 1V$ and $10V$
- Transfer characteristics in logarithmic scale at $V_{DS} = 1V$ and $10V$.

Table 11 summarizes the evolution with temperature of the main electrical DC parameters of two samples of 1 mm and 1.2 mm geometries: R_{DS} (for V_{DS} from 0 to 0.5V at

$V_{GS} = 0V$), I_{DSS} (at $V_{GS} = 0V$ and $V_{DS} = 10V$) and I_{GSS} (at $V_{GS} = 0V$ and $V_{DS} = 10V$) from $50^{\circ}C$ to $150^{\circ}C$.

Geometry	8x125 μ m						8x150 μ m					
Device	TZ1S0B100_Y89			TZ1S0B100A_Y89			TZ1S0B120_075			TZ1S0B120A_075		
T ($^{\circ}C$)	R_{DS} (Ω .mm)	I_{DSS} (mA/mm)	I_{GSS} (mA/mm)	R_{DS} (Ω .mm)	I_{DSS} (mA/mm)	I_{GSS} (mA/mm)	R_{DS} (Ω .mm)	I_{DSS} (mA/mm)	I_{GSS} (mA/mm)	R_{DS} (Ω .mm)	I_{DSS} (mA/mm)	I_{GSS} (mA/mm)
50	3.80	695	-5.67E-07	3.87	693	-1.04E-06	3.94	677	-2.44E-06	3.97	670	-1.72E-06
75	4.21	669	-1.15E-06	4.24	665	-2.49E-06	4.39	657	-3.78E-06	4.40	647	-3.86E-06
100	4.66	646	-2.14E-06	4.75	636	-5.55E-06	4.98	628	-6.43E-06	4.95	624	-7.36E-06
125	5.19	619	-3.98E-06	5.30	617	-7.89E-06	5.37	608	-8.61E-06	5.42	602	-1.32E-05
150	5.78	599	-5.26E-06	5.64	592	-1.27E-05	5.87	584	-1.40E-05	5.87	581	-9.45E-06

Table 11. R_{DS} , I_{DSS} and I_{GSS} from $50^{\circ}C$ to $150^{\circ}C$

There is no dispersion between the value of the DC parameters extracted as well as on their respective evolution with the temperature.

The drain-source resistance R_{DS} increases with the temperature by 50% whereas I_{DSS} decreases by 14% between $50^{\circ}C$ and $150^{\circ}C$.

The gate leakage current in transistor mode increases by one order of magnitude for 1mm gate width devices and by a factor 4.5 for 1.2 mm devices characterized versus temperature present a higher leakage current than the 1 mm ones.

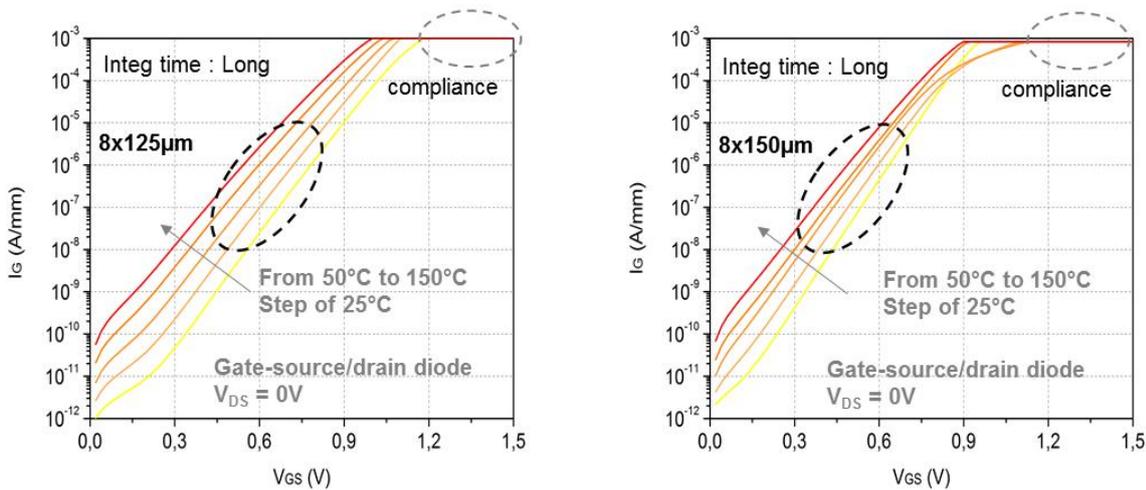


Figure 107. Forward I_G - V_{GS} characteristics of 1mm and 1.2mm gate width HEMTs from $50^{\circ}C$ to $150^{\circ}C$

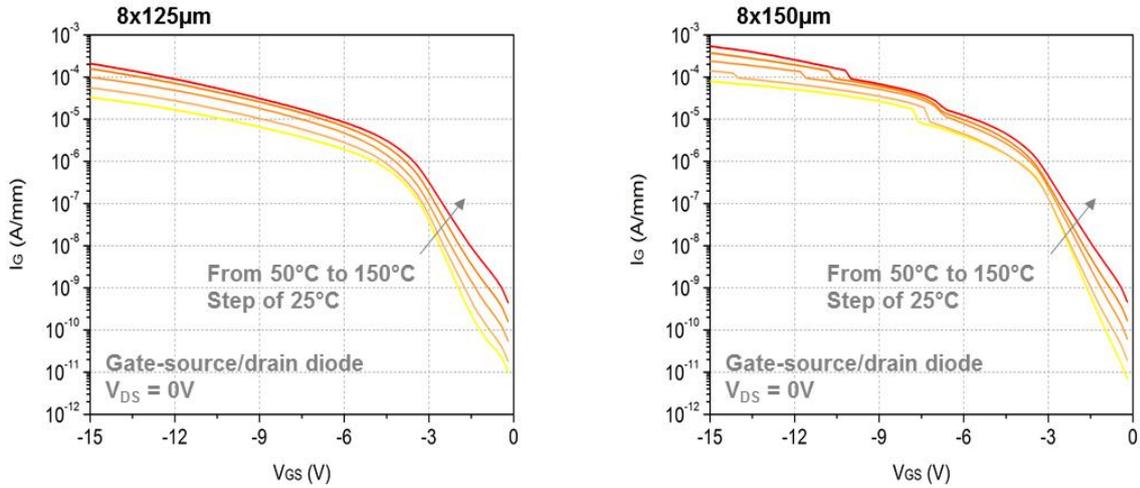


Figure 108. Reverse I_G - V_{GS} characteristics of 1mm and 1.2mm gate width HEMTs from 50°C to 150°C

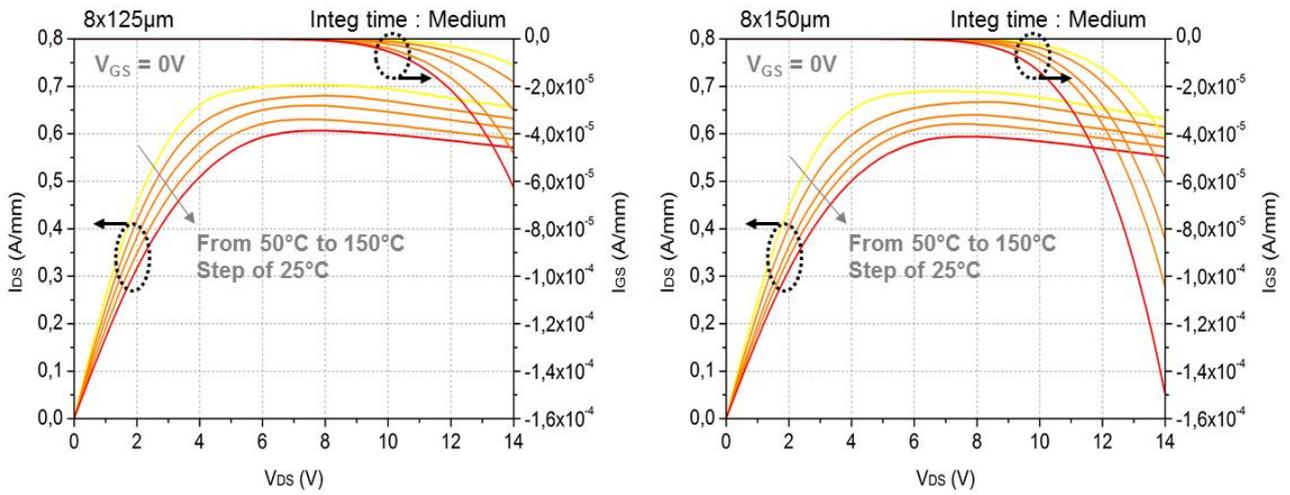


Figure 109. Drain and gate currents versus V_{DS} from 50°C to 150°C at $V_{GS} = 0V$

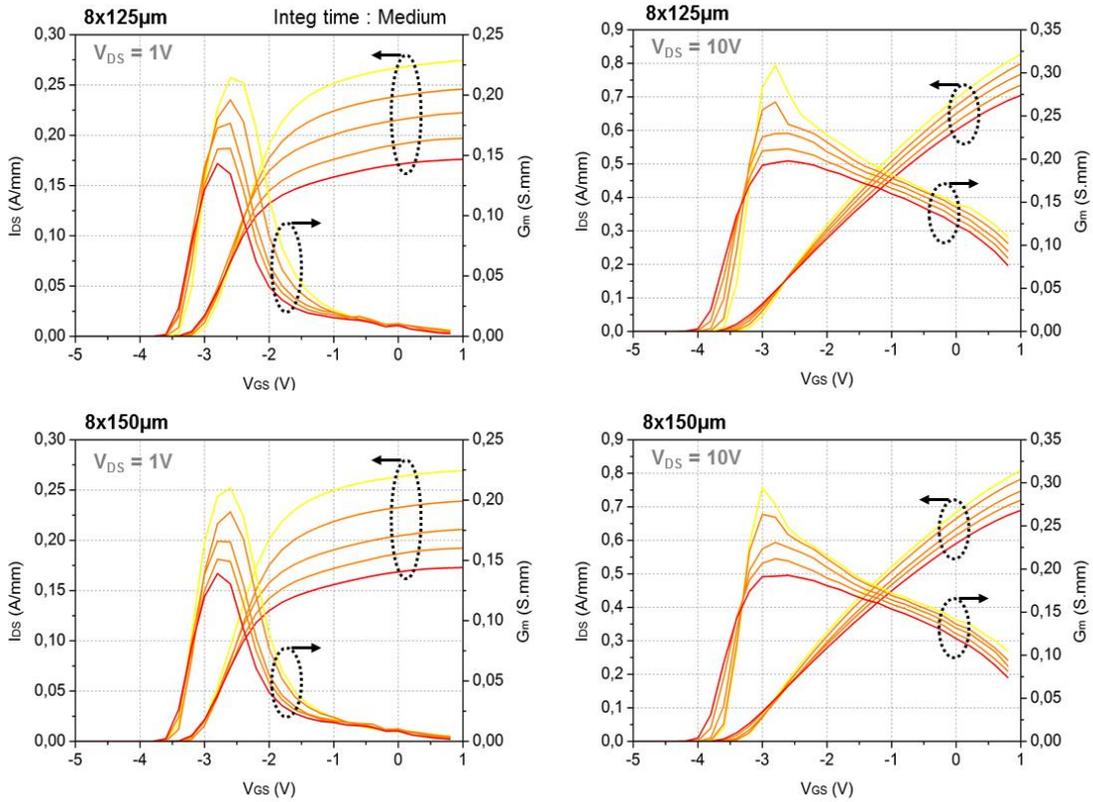


Figure 110. I_{DS} - V_{GS} and G_m - V_{GS} of 1 mm and 1.2 mm gate width HEMTs at $V_{DS} = 1V$ and $10V$ from $50^\circ C$ to $150^\circ C$

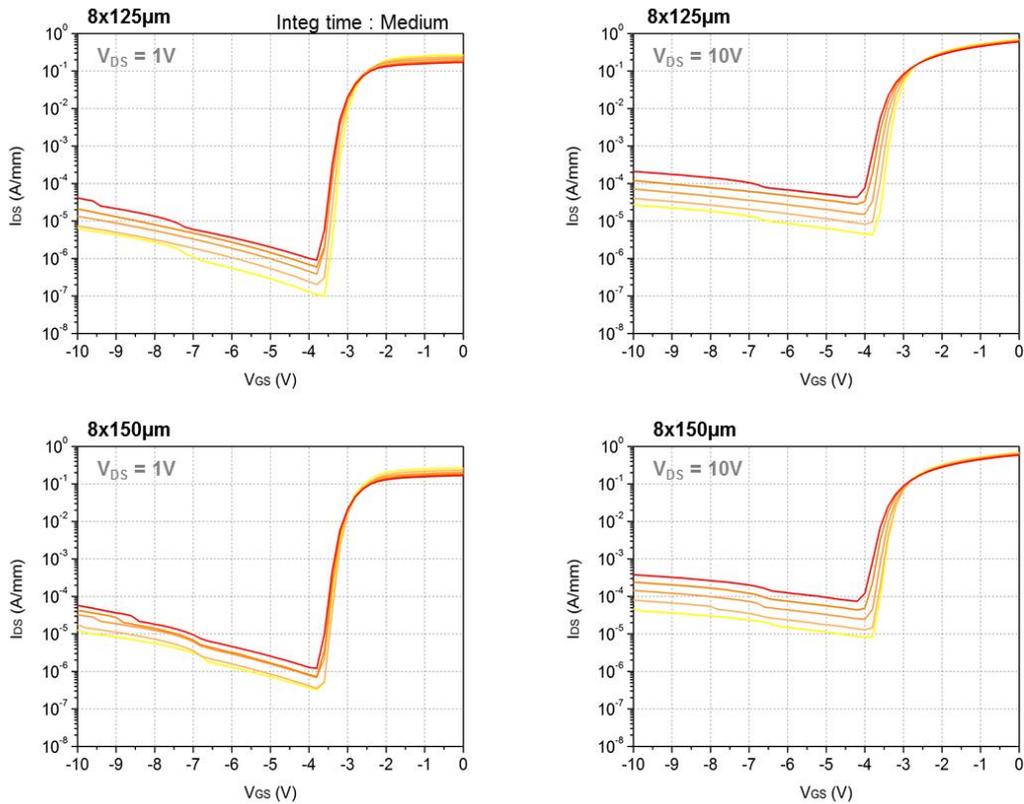


Figure 111. I_{DS} - V_{GS} in logarithmic scale of 1 mm and 1.2 mm gate width HEMTs at $V_{DS} = 1V$ and $10V$ from $50^\circ C$ to $150^\circ C$

3.4.3 Breakdown measurement

The off-state breakdown voltage, V_{br} , is an important parameter determining the limits of the applied voltage and current of the studied technology and hence determining the safe operating area (SOA) under conditions of high power and high drain voltage operation. It is crucial information about the used technology in order to achieve the maximum power in optimum conditions without achieving the burnout or catastrophic failure of the sample.

In the GaN based HEMTs, the two components of electric field, vertical and longitudinal must be considered in the evaluation of the breakdown voltage. The vertical one is maximal under the gate while the longitudinal one is related to the drain-source voltage applied to the channel. The breakdown mechanism can then occur either in the junction of one of the gate-drain or gate-source diodes or both or in the channel. Two setups are used to study the breakdown voltage: diode mode and transistor mode.

3.4.3.1 Gate-source and gate-drain diodes breakdown

3.4.3.1.1 at room temperature

The breakdown voltage measurement in the diode mode is used to evaluate the maximum voltage that can be applied to the Schottky diodes without degradation or burnout of the GaN HEMT. In the first experiment, gate-source and gate-drain reverse current characteristics are measured up to $-20V$. Then, the voltage is increased by step of $-10V$ up to $-100V$ with a compliance of $1mA/mm$ on the gate current. As the threshold voltage V_T of this technology is $-3V$, the breakdown measurements are performed in the subthreshold regime where the leakage current I_G is also supposed to increase with the voltage. The leakage current might hide the breakdown voltage as it increases. Figure 112 shows breakdown voltage measurements of gate-source (left) and gate-drain (right) Schottky diodes of four samples with $8 \times 125 \mu m$ gate width up to gate-source and gate-drain voltages of $-100V$. The gate current compliance is fixed at $1mA/mm$. The four characterized samples show no significant dispersion in the I_G-V_G characteristics. It is not explained why the gate-drain leakage current of the $1mm$ devices is higher than the gate-source one as the gate-source distance is lower than the gate-drain one. However, the field plate is connected to the source and this could be a crucial parameter to explain the difference noticed in the leakage currents.

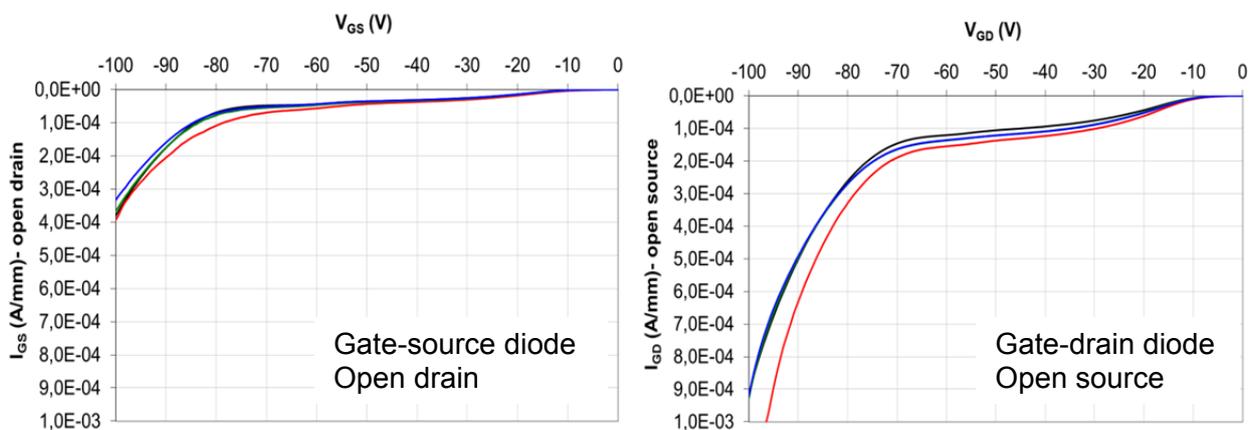


Figure 112. Breakdown measurements of Schottky diodes of four samples with $W_G = 8 \times 125 \mu m$

The gate-drain breakdown voltage at 24°C is estimated at 70-80V. On the other hand the gate-source breakdown voltage is estimated more than 100V.

3.4.3.1.1 for temperature range of 50°C to 150°C

Two terminal breakdown voltage measurements were performed from 50°C to 150°C to determine the gate-source and gate-drain diodes breakdown voltage respectively BV_{GS} and BV_{GD} .

The gate-source and the gate-drain current reverse characteristics of a representative device with 1mm gate geometry with temperature are shown in figure 113. The gate-drain diode leakage current increases with temperature and exceeds 1 mA/mm without achieving the breakdown voltage. Usually, the value of 1 mA/mm is the tolerated limit of the leakage current beyond which the sample can be degraded or can burn-out. For this set, the leakage current of the studied four samples exceeds 2 mA/mm without achieving the breakdown voltage. The leakage current in this case hides the breakdown voltage especially for high temperatures.

Each graph of the figure 88 is divided into two regions: leakage and breakdown regions. In the first one, the leakage current is the preeminent mechanism before achieving the breakdown voltage, whereas the breakdown voltage onset is shown in the second region.

Due to the high value of the leakage current, setting a criterion on the leakage current to determine the breakdown voltage of the gate-drain diode is difficult. At 50°C and 75°C, the knee of the characteristic allows determining the breakdown voltage around 80V. At higher temperature, it is not possible to enter the breakdown region in the measured current range.

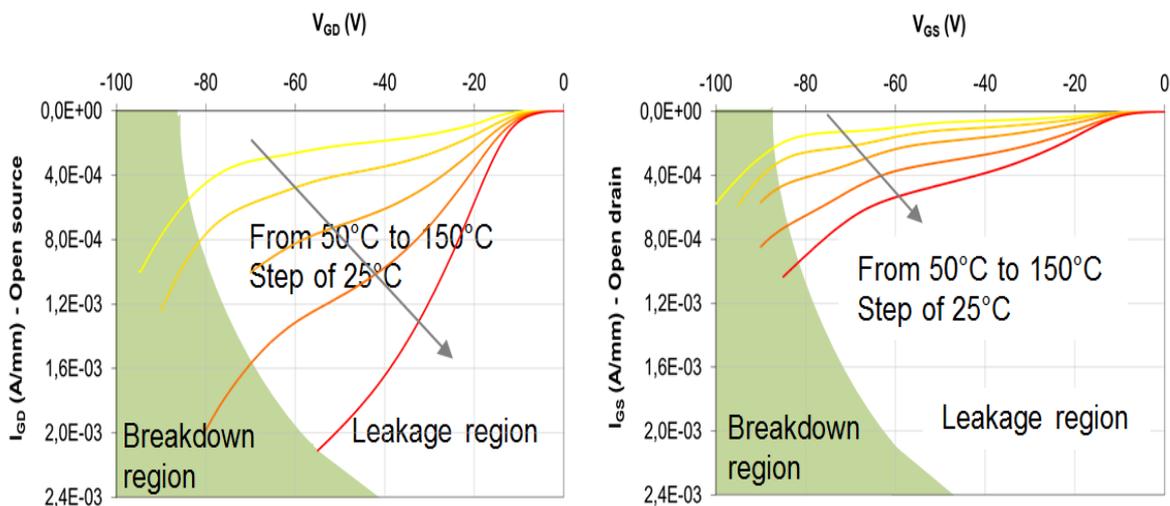


Figure 113. Gate-source and gate-drain diodes breakdown voltage measurements from 50°C to 150°C

As it is difficult to define a criterion on the leakage current to determine a diodes breakdown, we compare the leakage current at a fixed $V_{GS/D}$ to show the evolution of the gate leakage current with temperature. Figure 114 shows the evolution of the gate leakage current with temperature at $V_{GS/D} = -50V$. The gate-drain leakage current remains higher with temperature. The value of the gate-drain leakage current is 0.25mA/mm at 50°C and achieves

2mA/mm at 150°C whereas the gate-source leakage current remains below 0.5mA/mm in the studied temperature range.

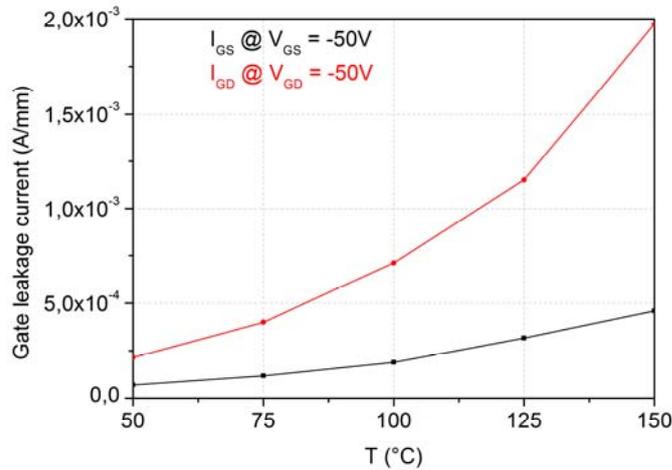


Figure 114. Gate leakage current of gate-source and gate-drain diodes at $V_{GSD} = -50V$ from 50°C to 150°C.

3.4.3.2. Off-state breakdown

The off-state breakdown voltage is determined by measuring the gate, source and drain currents by sweeping the drain-source voltage at fixed gate-source voltages in the subthreshold regime. V_{DS} is swept until 180V for V_{GS} from -6V to -30V as shown in figure 115 at room temperature for a representative device of the set of 8 samples under study. The value of 1mA/mm of the drain leakage current is not achieved under the chosen measurement conditions. A new criterion should be determined based on the characteristics.

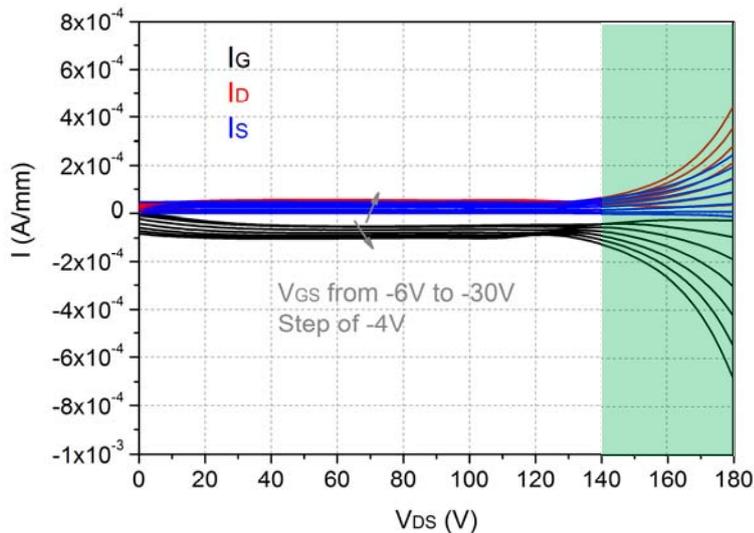


Figure 115. Off-state breakdown measurements at room temperature

3.4.3.2.1 at room temperature

In order to understand the off-state breakdown mechanisms that occur in the device, the characteristics are studied at a fixed V_{GS} . At $V_{GS} = -6V$, as shown in figure 116, the source current is negligible up to 140V while the gate and the drain currents are opposite and symmetrically equal. It means that up to $V_{DS} = 140V$, the breakdown is induced by the leakage current of the gate-drain diode.

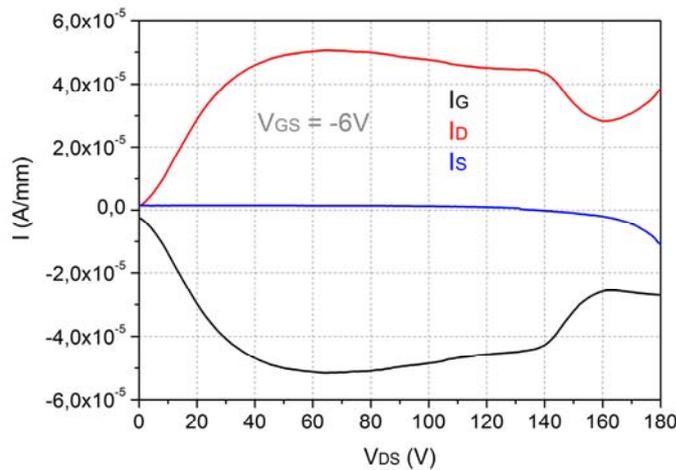


Figure 116. Off-state breakdown measurements in transistor mode at $V_{GS} = -6V$

For V_{DS} from 140V to 160V, a decrease of the drain current appears and from $V_{DS} = 160V$ to 180V, the drain current increase is accompanied by a decrease of the source current. The positive drain current accompanied with negative source current indicates that the leakage current is flowing in the channel.

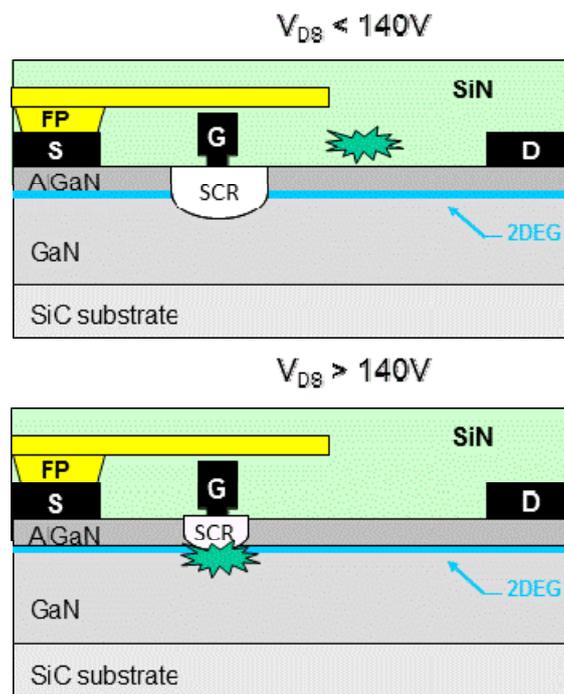


Figure 117. Off-state breakdown mechanisms at $V_{GS} = -6V$

The breakdown mechanisms for $V_{GS} = -6V$ are illustrated in figure 117. The breakdown mechanism is governed by the gate-drain diode up to 140V and by channel breakdown from 160V to 180V, while for V_{DS} from 140V to 160V; there is a transition between the two breakdown mechanisms.

Figure 118 shows the off-state breakdown at $V_{GS} = -30V$ at room temperature.

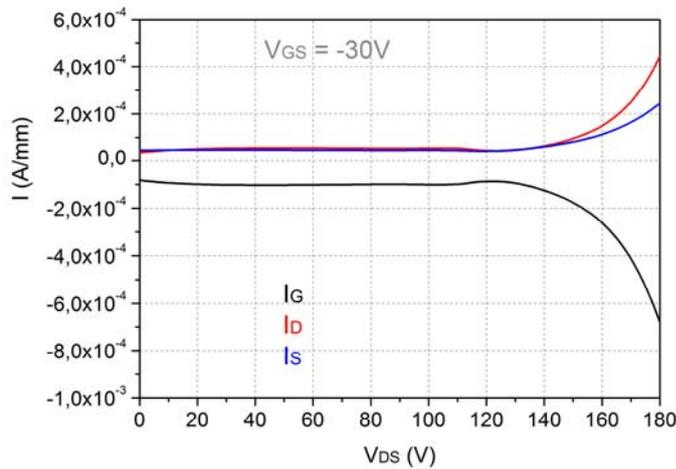


Figure 118. Off-state breakdown at $V_{GS} = -30V$

The same evolution of the gate, drain and source currents with V_{DS} was observed for V_{GS} from -14V to -30V. At V_{GS} from -14V to -30V, the drain and source currents are positive and superimposed while the gate current is negative. This means that the breakdown mechanism is due to the leakage of the gate-source and drain-source diodes as shown in figure 119.

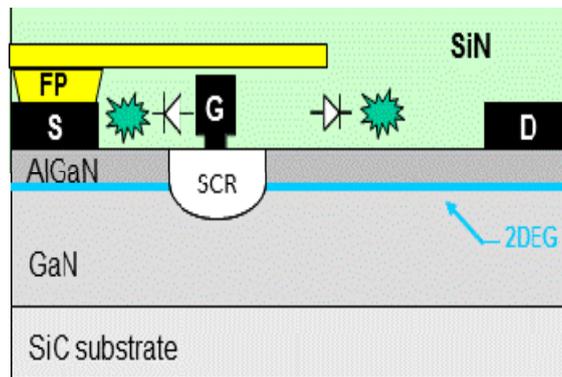


Figure 119. Off-state breakdown mechanism at $V_{GS} = -30V$

A criterion is chosen at $I_D = 0.1mA/mm$ to determine the off-state breakdown voltage (figure 120). The off-state breakdown voltage is $V_{BD} = 152V$ at $V_{GS} = -30V$ and achieves 172V at $V_{GS} = -14V$.

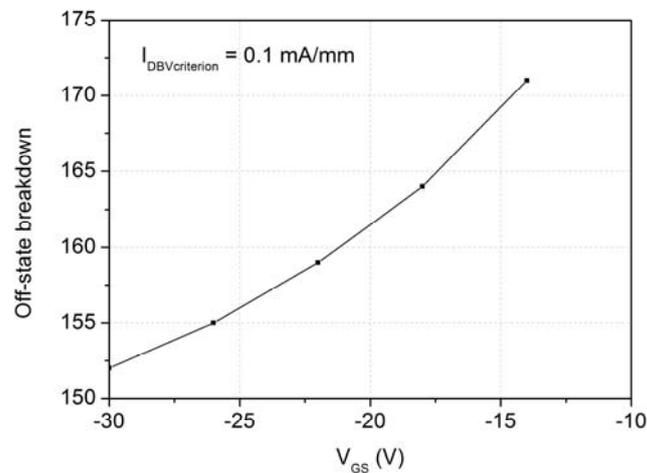


Figure 120. Off-state breakdown vs V_{GS} at criterion of $I_D = 0.1$ mA/mm

As expected, the breakdown voltage V_{BD} decreases as V_{GS} is more negative. Indeed, the breakdown voltage is comprised between 155V and 165V at $V_{GS}=-20$ V, and between 145V and 155V at $V_{GS}=-30$ V with the I_D criterion of 0.1 mA/mm.

3.4.3.2.2 for temperature from 50°C to 150°C

Off-state breakdown voltage measurements were performed from 50°C to 150°C to determine the off-state breakdown and to verify the determined criterion ($I_D = 0.1$ mA/mm) at room temperature. Figure 121 shows the drain, gate and source currents evolution with drain-source voltage for V_{GS} from -10V to -30V from 50°C to 150°C.

By increasing the temperature from 50°C to 150°C the drain, gate and source subthreshold leakage currents increase. The compliance of 1 mA/mm that was not achieved at room temperature for all the range of V_{GS} values is achieved at 125°C at $V_{GS} = -20$ V and at 150°C at $V_{GS} = -10$ V.

The breakdown mechanisms shown at room temperature remain the same as with temperature from 50°C to 150°C, except the leakage current and the breakdown voltage that increase.

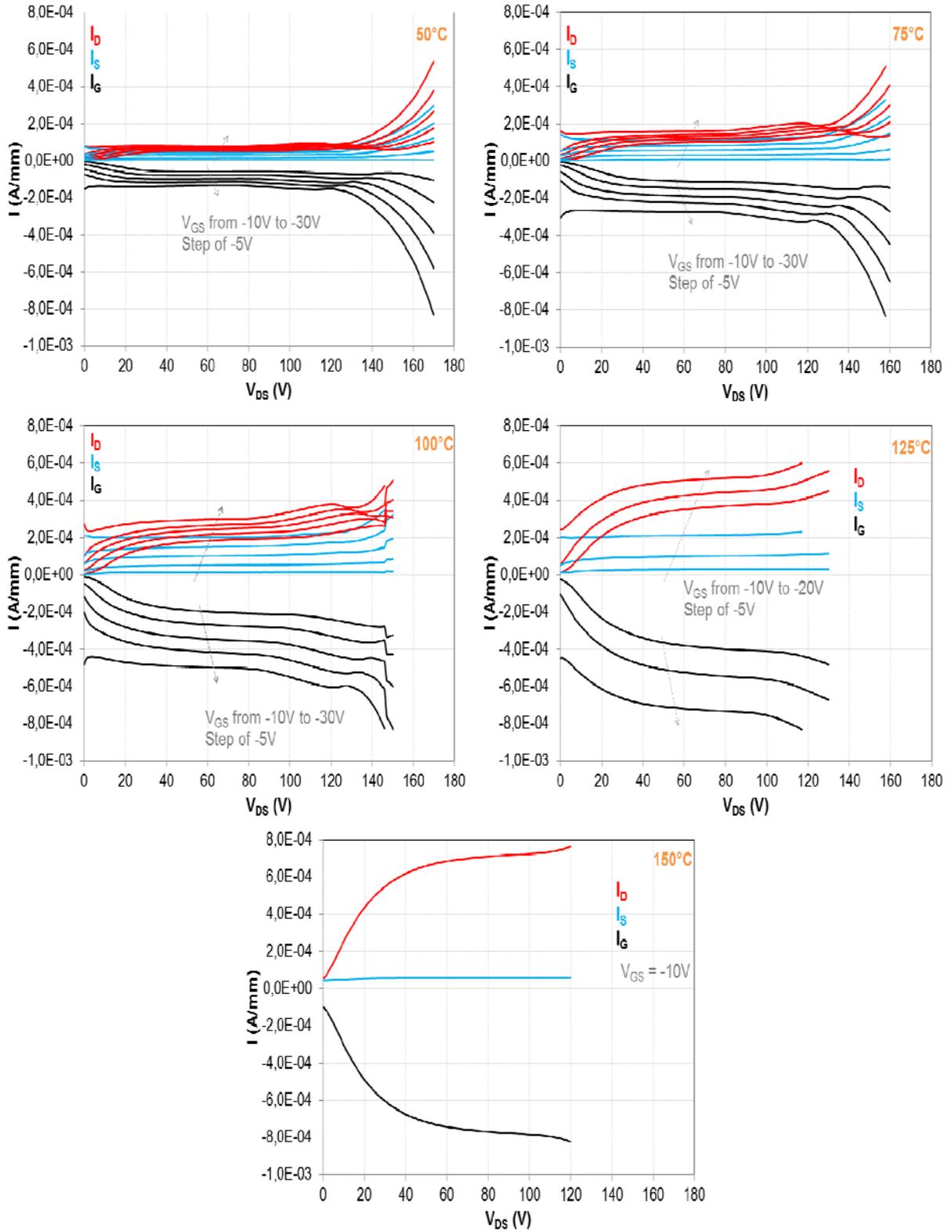


Figure 121. Off-state breakdown measurements from 50°C to 150°C

Figure 122 illustrates the off-state breakdown at $I_D = 0.1\text{mA/mm}$ from 25°C to 150°C with a step of 25°C .

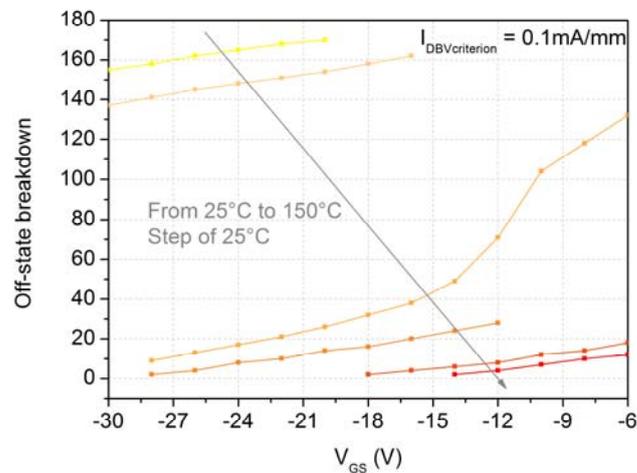


Figure 122. Off-state breakdown vs V_{GS} at criterion of $I_D = 0.1 \text{ mA/mm}$

The value of $I_D = 0.1 \text{ mA/mm}$ is achieved at low values of V_{DS} at high temperatures. This criterion is reliable only at temperatures of 25°C and 50°C where the leakage currents are lower.

Conclusion of case study 4: “link” with Extreme GaN project

AlGaIn/GaN HEMT’s Schottky diode and off-state breakdown have been investigated at room temperature and at high temperature by using voltage injection technique to determine the breakdown at high current values.

The gate-drain breakdown voltage is estimated between 70-80V, while the gate-source breakdown voltage is higher than 100V at room temperature. At high temperatures, the leakage current exceeds 1mA/mm without achieving the breakdown area.

In low pinch-off conditions, the breakdown mechanism is located in the gate-drain region up to 140V while it is located in the channel from 160V to 180V. Furthermore, in deep pinch-off conditions, the breakdown mechanism occurs in the gate-source and gate-drain regions up to 180V.

The criterion of $I_D = 0.1 \text{ mA/mm}$ has been used to determine off-state breakdown at room temperature but it is difficult to use it at high temperatures as the leakage current increases significantly.

No degradation has been noticed after the two-terminal and three terminal breakdown measurements.

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Conclusion

The conduction mechanisms inducing the leakage current in GaN based HEMTs have been studied on virgin devices issued from GH50 GaN process. “Leaky” device (I_G is higher than $200\mu\text{A}/\text{mm}$ at $V_{DS} = 50\text{V}$ and $V_{GS} = -7\text{V}$) have a double barrier height at low temperatures. The output characteristics showed no difference between the “Non Leaky” and “Leaky” devices, as well as the static resistance R_{DS} that is superimposed for all studied devices for temperature range of 100K to 400K. This highlights that the leakage path is not located in the channel. The “leaky” devices subthreshold leakage current has a negative dependence with temperature from 300K to 400K which is an unexpected behavior. The drain current transient measurements showed three dominant traps for the “leaky” transistor with activation energies between 0.7 eV and 0.9 eV. Traps with activation energies in this range were reported in literature to be associated with electron injection from the gate and trapping either inside the AlGaN layer or at the surface close to the gate. Leaky devices present a gate lag ratio more than 3 times higher than non-leaky devices. The leakage currents of GaN based HEMTs might be reduced by accurate engineering of the buffer layer and optimizing the residual strain at the AlGaN/SiN interface in the vicinity of the gate.

An electrical parasitic effect (Belly Shape: BS) in AlGaN/GaN HEMTs that appears on the gate current DC characteristic in forward bias after HTOL ageing test is characterized by dc and gate current low frequency noise (LFN) measurements. The “Belly Shape” (BS) effect is characterized by higher gate forward current for $V_{GS/D}$ below 1.2V compared to the one of devices without BS effect. The “Belly Shape” effect does not affect the life time of the devices as the drift of the drain current and the threshold voltage during HTOL test is similar for aged devices with or without BS effect. Devices with BS effect have higher leakage current compared to the devices without BS effect.

The gate current LFN spectra of reference device present $1/f^{\gamma}$ noise, which is proportional to the square of I_G for $V_{GS/D} < 1.2\text{V}$. Gate current low frequency noise spectra of aged devices with BS effect in the BS bias region present a combination of $1/f$ and generation-recombination noise components. Devices with BS effect exhibit Lorentzian noise that is often non-repeatable even when measured with the same bias conditions as well as the belly shape effect in the dc characteristics. In the bias region of the diode controlled by its series resistance, S_{IG} is not dependent on I_G^2 and it is found to be related to the fluctuations occurring in diode series resistances. The belly shape effect is then assumed to be a transient effect related to trapping mechanisms located beneath the gate in the gate/cap GaN interface or at the gate edges.

The variation of the Al content from 23.5% to 25% at 300K increases the ideality factor and decreases the gate and the drain subthreshold leakage currents and the threshold voltage becomes more negative. The maximum drain current I_{DSS} is weakly dependent on the variation of Al content at open channel condition. For temperature from 105K to 305K, the ideality factor of the device with 25% of Al content is higher, the Schottky barrier height is lower and the maximum drain current I_{DSS} is higher. On the contrary, the variation of Al content from 23.5% to 25%, has no impact on the electrical parameters in the temperature

range from 330K to 405K. The 2200 hours HTRB test applied on devices with Al content of 23.5% and 25% has induced identical degradation of DC parameters independently of the Al mole fraction in AlGa_N layer.

The gate-drain breakdown voltage of AlGa_N/Ga_N HEMTs issued GH25 process is estimated at about 70 to 80V, while the gate-source breakdown voltage is higher than 100V at room temperature. At high temperatures, the leakage current exceeds 1mA/mm without achieving the breakdown area. In low pinch-off conditions, the breakdown mechanism is located in the gate-drain region up to 140V while it is located in the channel from 160V to 180V. Furthermore, in deep pinch-off conditions, the breakdown mechanism occurs in the gate-source and gate-drain regions up to 180V.

The usual criterion of 1mA/mm used to define the breakdown voltage in GaAs based HEMTs can not be used for Ga_N based HEMTs due to the low leakage current level of AlGa_N/Ga_N HEMTs. The criterion of $I_D = 0.1\text{mA/mm}$ has been used to determine off-state breakdown at room temperature but it is difficult to use it at high temperatures as the leakage current increases significantly.

We have used drain and gate voltage injection technique to measure the breakdown voltage of Ga_N HEMTs instead of gate and drain current injection technique in order to be able to achieve the breakdown voltage area at high leakage current level ($I_D = 0.1\text{mA/mm}$). The limitation of the used technique is that the device might burn-out if we achieve the run-way mechanism area.

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