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Amit Kumar Sahoo

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THESE

PRESENTEE A

L'UNIVERSITE BORDEAUX I

ECOLE DOCTORALE DE SCIENCES PHYSIQUES ET DE L'INGENIEUR

Par **Amit Kumar SAHOO**

POUR OBTENIR LE GRADE DE
DOCTEUR

SPECIALITE: **ELECTRONIQUE**

Electro-thermal Characterizations, Compact Modeling and TCAD based Device Simulations of advanced SiGe:C BiCMOS HBTs and of nanometric CMOS FET

Soutenance prévue le : 13th Juillet 2012

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Electro-thermal Characterizations, Compact Modeling and TCAD based
Device Simulations of advanced SiGe:C BiCMOS HBTs and of
nanometric CMOS FET

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*To Pubali
To my Parents Janakibala and
Abhoy Narayan Sahoo*

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Abstract

An extensive evaluation of different techniques for transient and dynamic electro-thermal behavior of microwave SiGe:C BiCMOS hetero-junction bipolar transistors (HBT) and nano-scale metal-oxide-semiconductor field-effect transistors (MOSFETs) have been presented. In particular, new and simple approach to accurately characterize the transient self-heating effect, based on pulse measurements, is demonstrated. The methodology is verified by static measurements at different ambient temperatures, s-parameter measurements at low frequency region and transient thermal simulations. Three dimensional thermal TCAD simulations are performed on different geometries of the submicron SiGe:C BiCMOS HBTs with f_T and f_{max} of 230 GHz and 290 GHz, respectively. A comprehensive evaluation of device self-heating in time and frequency domain has been investigated. A generalized expression for the frequency-domain thermal impedance has been formulated and that is used to extract device thermal impedance below thermal cut-off frequency. The thermal parameters are extracted through transistor compact model simulations connecting electro-thermal network at temperature node. Theoretical works for thermal impedance modeling using different networks, developed until date, have been verified with our experimental results. We report for the first time the experimental verification of the distributed electrothermal model for thermal impedance using a nodal and recursive network. It has been shown that, the conventional single pole thermal network is not sufficient to accurately model the transient thermal spreading behavior and therefore a recursive network needs to be used. Recursive network is verified with device simulations as well as measurements and found to be in excellent agreement. Therefore, finally a scalable electro-thermal model using this recursive network is developed. The scalability has been verified through numerical simulations as well as by low frequency measurements and excellent conformity has been found in for various device geometries.

Key words: Hetero-junction bipolar transistors (HBTs), MOSFET, electrothermal effects, thermal resistance, thermal capacitance, thermal impedance, semiconductor device characterizations, pulse measurements, semiconductor device modeling, thermal TCAD simulation, scalable electrothermal model.

Résumé

Ce travail de thèse présente une évaluation approfondie des différentes techniques de mesure transitoire et dynamique pour l'évaluation du comportement électro-thermique des transistors bipolaires à hétérojonctions HBT SiGe:C de la technologie BiCMOS et des transistors Métal-Oxyde-Semiconducteur à effet de champ (MOSFET) de la technologie CMOS 45nm. En particulier, je propose une nouvelle approche pour caractériser avec précision le régime transitoire d'auto-échauffement, basée sur des mesures impulsionnelles. La méthodologie a été vérifiée par des mesures statiques à différentes températures ambiantes, des mesures de paramètres S à basses fréquences et des simulations thermiques transitoires. Des simulations thermiques par éléments finis (TCAD) en trois dimensions ont été réalisées sur les transistors HBTs de la technologie submicroniques SiGe: C BiCMOS. Cette technologie est caractérisée par une fréquence de transition f_T de 230 GHz et une fréquence maximum d'oscillation f_{MAX} de 290 GHz. Par ailleurs, cette étude a été réalisée sur les différentes géométries de transistor. Une évaluation complète des mécanismes d'auto-échauffement dans les domaines temporels et fréquentiels a été réalisée. Une expression généralisée de l'impédance thermique dans le domaine fréquentiel a été formulée et a été utilisée pour extraire cette impédance en deçà de la fréquence de coupure thermique. Les paramètres thermiques ont été extraits par des simulations compactes grâce au modèle compact de transistors auquel un modèle électro-thermique a été ajouté via le nœud de température. Les travaux théoriques développés à ce jour pour la modélisation d'impédance thermique ont été vérifiés avec nos résultats expérimentaux. Il a été montré que, le réseau thermique classique utilisant un pôle unique n'est pas suffisant pour modéliser avec précision le comportement thermique transitoire et donc qu'un réseau plus complexe doit être utilisé. Ainsi, nous validons expérimentalement pour la première fois, le modèle distribué électrothermique de l'impédance thermique utilisant un réseau nodal récursif. Le réseau récursif a été vérifié par des simulations TCAD, ainsi que par des mesures et celles-ci se sont révélées en excellent accord. Par conséquent, un modèle électro-thermique multi-géométries basé sur le réseau récursif a été développé. Le modèle a été vérifié par des simulations numériques ainsi que par des mesures de paramètre S à basse fréquence et finalement la conformité est excellente quelque soit la géométrie des dispositifs.

Mots-clefs : Hétéro-transistors bipolaires (HBT), MOSFETs, effets électrothermiques, résistance thermique, capacité thermique, impédance thermique, caractérisations de semi-conducteurs, des mesures impulsionnelles, la modélisation de dispositifs semi-conducteurs, de simulation thermique TCAD, modèle électrothermique multi-géométries.

Glossary

Acronym and abbreviations:

ITRS	International Technology Roadmap for Semiconductors
WiHDMI	Wireless High-Definition Multimedia Interface
CMOS	Complementary metal–oxide–semiconductor
FET	Field Effect Transistor
MOSFET	Metal-Oxide Semiconductor Field Effect transistor
HBT	Heterojunction Bipolar transistor
SiGe	Silicon-Germanium
HEMT	High electron mobility transistor
WLAN	Wireless local area network
TEM	Transmission electron microscopy
HICUM	High Current Model
RF	Radio Frequency
TCAD	Technology Computer-Aided Design
NQS	Non-quasi-static
SMU	Source/monitor unit
PMU	Pulse measurement units
GSG	Ground – Signal – Ground
SOLT	Short-Open-Load-Thru
VNA	Vector network analyzer

General notations:

λ	wavelength
f_{\max}	Maximum frequency of oscillation
f_T	Transit frequency
L_G	Gate length
Z_{TH}	Thermal impedance
R_{TH}	Thermal resistance
C_{TH}	Thermal capacitance
A_E	Emitter contact area
L_E	Emitter contact length
W_E	Emitter contact width
α	Current Gain in common base configuration
β	Current Gain in common emitter configuration
BV_{CB0}	Base-collector breakdown voltage in common base configuration
BV_{CE0}	Base-collector breakdown voltage in common emitter configuration
BV_{EB0}	Emitter-base junction breakdown voltage
C_{BC}	Base-collector capacitance
C_{BE}	Base-emitter capacitance
E_C	Energy of conduction band

E_G	Energy gap between valance band and conduction band
E_V	Valance band energy
g_m	Transconductance
I_B	Base current
I_C	Collector current
I_E	Emitter current
J_C	Collector current density
J_{CKirk}	Collector current density due to the Kirk effect
k	Boltzmann constant
m_e	Effective mass of electron
N_{ab}	Doping concentration in the base
n	Ideality factor of base-emitter junction
N_{dc}	Doping concentration in collector
N_{de}	Doping concentration in the base
R_B	Base resistance
R_C	Collector resistance
R_E	Emitter resistance
SCR	Space charge region
τ_B	Transit time in the base
τ_C	Transit time in the collector
τ_F	Transit time in the base-collector
τ_{F0}	Base-collector transit time at zero current
V_{BE}	Applied base-emitter voltage
V_{CB}	Applied base-collector voltage
V_{Cbi}	Intrinsic base-collector voltage
V_{CE}	Collector-emitter voltage
v_{sat}	Saturation velocity of electron
v_T	Electron thermal velocity
T_j	Junction temperature
T_{sub}	Substrate temperature
P_{diss}	Power dissipation
ΔT	Temperature rise
λ_{th}	Specific heat conductance
T_{amb}	Ambient temperature
$\tau_{Thermal}$	Thermal time constant
$f_{Thermal}$	Thermal cut-off frequency
p	Laplace variable
T_B	Base-plate temperatures
L_{Cable}	Coaxial cable inductance
C_{Cable}	Coaxial cable capacitance

R_{cable}	Coaxial cable resistance
$ Z _{Cable}$	Coaxial cable characteristic impedance
$I_C(t)$	Transient collector current
I_{C-ISO}	Isothermal collector current
Z_{trans}	Transient state thermal impedance
V_{GS}	Gate-source voltage
V_{DS}	Drain-source voltage
I_D	Drain current
T_{CH}	Channel temperature
κ	Thermal conductivity
c_L	Lattice heat capacity
ϕ_n and ϕ_p	Electron and hole quasi-Fermi potentials
μ_n and μ_p	Electron and hole mobilities
$T_{Lattice}$	Lattice temperature
F_{Heat}	Heat flux



General introduction

Lower production cost and higher product complexity are key factors for the success of semiconductor and system integration companies. Volume market domination is more than ever related to low cost, high performance, and reliable products with very short development and production cycle time. Thus, a high level of innovation is mandatory if we want to succeed in this highly evolving and competitive world.



A. Millimeter to THz waves and its application

Millimeter and terahertz waves are the electro-magnetic waves like microwaves, radio waves, visible and infrared light (*Figure I*). Millimeter waves lie in the frequency region from 30–300 GHz ($\lambda = 1–10$ mm) and the terahertz waves, sometimes called sub-millimeter waves, lie in the region from 300 GHz to 3 THz ($\lambda = 100 \mu\text{m}$ to 1 mm) [1]. However, in the context of wireless communication, the term Millimeter waves generally corresponds to a few bands of spectrum near 38, 60 and 94 GHz, and more recently to a band between 70 GHz and 90 GHz (also referred to as E-Band), that have been allocated for the purpose of wireless communication in the public domain [2].

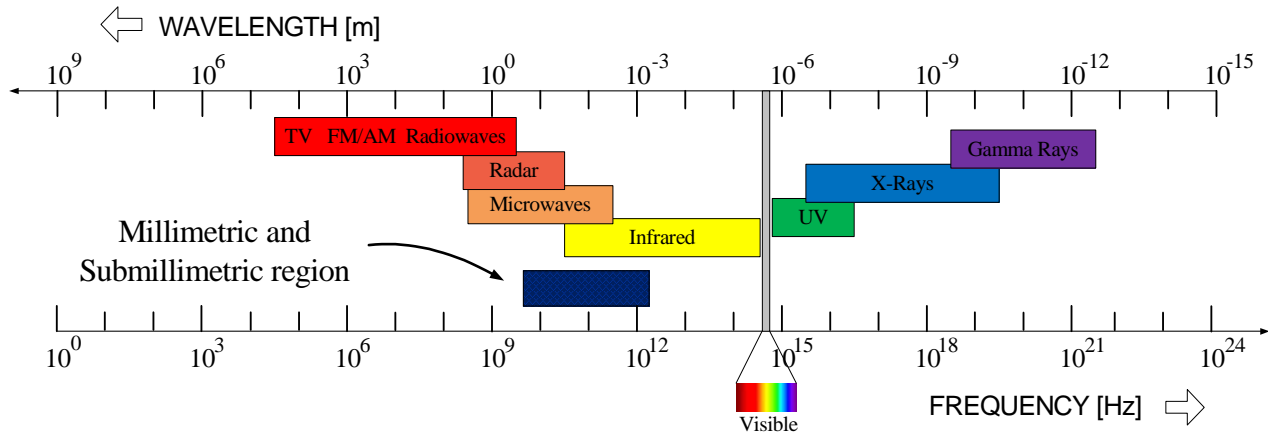


Figure I: Millimeter and sub-millimeter wave range

The electromagnetic waves up to and including microwaves that have relatively low frequencies are generally unaffected by atmospheric effects. This has made them suitable for long-range radio communications such as television and radio broadcasting. In comparison, millimeter and terahertz waves suffer from attenuation caused by rain and resonant absorption in oxygen and water molecules, so they are unsuitable for long-range radio communications. However, their short wavelengths prove to be an advantage in the transmission of large amounts of data at one time. Millimeter and terahertz waves also provide high spatial resolution in imaging applications, in contrast to the low definition of microwave imaging. Moreover, in the terahertz region, it may be possible to detect molecular networks through weak inter molecule coupling, which could lead to the application of terahertz waves to protein analysis and drug discovery [1].

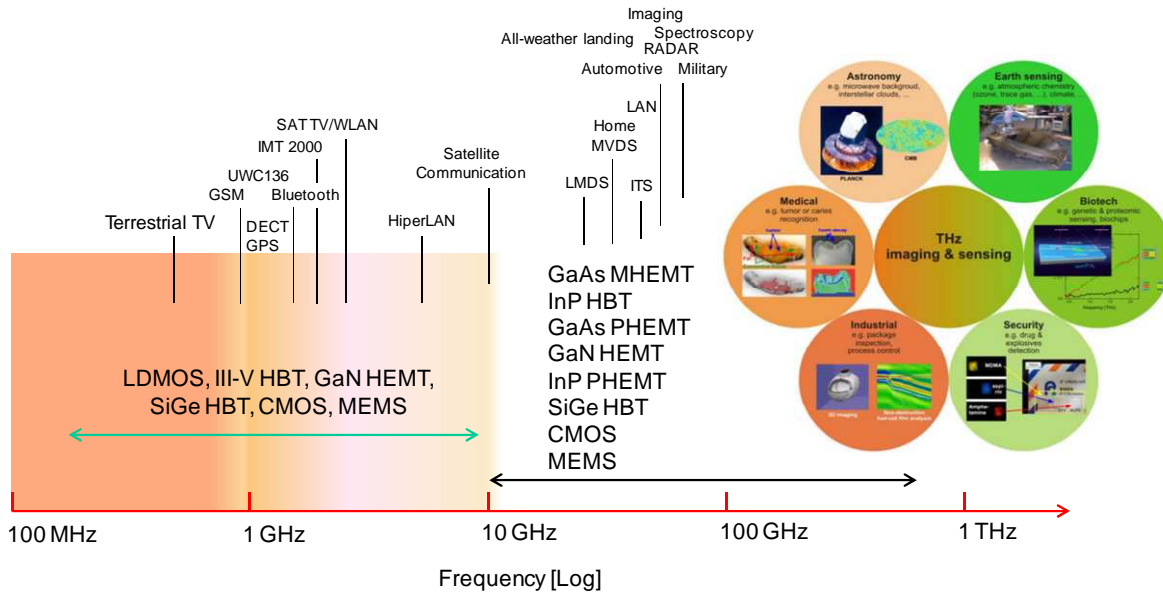


Figure II: Millimeter wave to THz frequency application; source[3], [4].

The evolution of these technologies is based on the ability of transistors to increase their performance. This is achieved by reducing the size of device and circuit which implies an increase in computing speeds. In modern integration technology, the down scaling of electronic device dimensions has been expected to be the main way to achieve better high frequency performance as seen by the International Technology Roadmap for Semiconductors (ITRS). The faster growth of RF wireless communications market requires the necessity of high performance device at low cost, because transistors fabricated on silicon offer ultra-large-scale integration capability and a high cut-off frequency. The requirement of high speed circuit performance has been addressed by miniaturization of device geometries and increased packaging densities. All these developments are opening up a wide spectrum of applications, from radar to automotive (77 GHz), wireless broad band network, WiHDMI (60 GHz) and range beyond 100 GHz [5]. This implies transistors capable of operating up to 0.5 THz. The applications being referred many of astronomy to biotechnology (biochip) in through the medical (identification of tumors or cavities) or safety (detection drugs or explosives). Over the past decades this downscaling has allowed the semiconductor industry to gain significant progress in high speed and also new circuit applications such as automotive radar, terahertz imaging, 100Gb/s data transfer etc. As seen by the technology roadmap, geometry scaling is anticipated to be the key technique to carry on this tendency.

B. High frequency state of the art

Since the revolutionary invention of the transistor at Bell Laboratories in 1947, the progress made in the field of semiconductor technology have a constant increase in performance according to Moore' law which states that the number of transistors per chip doubles every 2 years [6]. Early 1950s, the transistors were made from germanium. However, the germanium-based transistor is not very reliable and does not work at very high temperature. Everything changed in 1954 when Texas Instruments announced the first silicon transistor. Ten years later, a silicon chip containing over 2000 transistors was fabricated. Today, the Quad Core Intel Itanium contains more than 1 billion transistors. This is an amazing and revolutionary progress of silicon technology.

Figure III and Figure IV show the roadmap prescribed by the ITRS in terms of transit frequency (f_T) and maximum oscillation frequency (f_{max}) by comparing the silicon components (CMOS and SiGe HBT) and III-V (InP HEMT, InP HBT, GaAs and GaAs PHEMT and MHEMT).

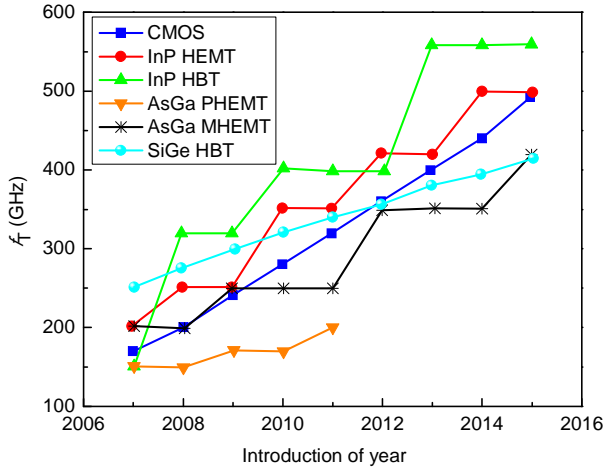


Figure III: Evolution of transit frequency f_T with introduction of year for silicon and III-V technology; source [7], [8].

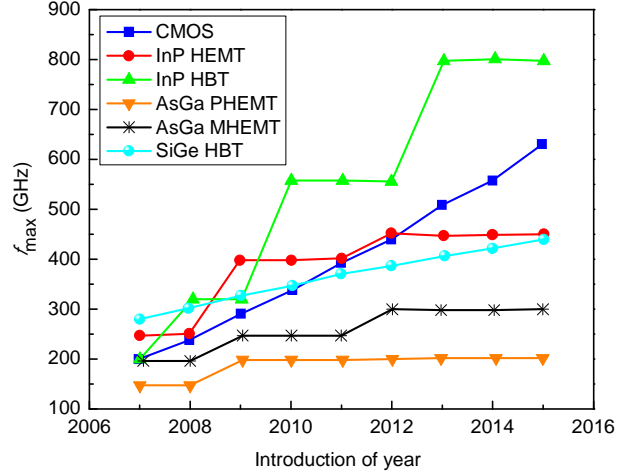


Figure IV: Evolution of maximum oscillation frequency f_{max} with introduction of year for silicon and III-V technology; source [7], [8].

In millimeter wave applications, the III-V technologies have dominated the silicon technologies for many years. Performances of silicon technologies are still lower than GaAs, PHEMT, InP and InP HBT HEMT. The electron mobility of silicon is lower, which limits the performance of the technology. However, advancement in silicon technology driven by high

performance digital applications offer advantages to the mm-wave designer [9]. Performance, quantified by f_T and f_{max} has dramatically increased with geometry scaling and technology enhancements in both CMOS and SiGe HBTs. Both CMOS and BiCMOS technologies have been used to demonstrate circuit functioning at frequencies in and above the K-band. Now, these silicon technologies are, by virtue of nanometer-scale design rules, able to implement staggering amounts of digital logic in a given area thereby enabling the on-chip integration of sophisticated control logic for performance tuning and/or digital signal processing [9]. Furthermore, the worldwide manufacturing capacity of silicon technologies driven by consumer applications like gaming and personal electronic appliances assures low-cost. This will certainly provide a boost for the evolution of mm-wave consumer applications. The combination of mm-scale wavelengths, low cost and the ability to integrate begs the consideration of array-based transceiver topologies being implemented on a single die or package.

Silicon HBT offer some advantages compared to CMOS devices such as lower $1/f_{noise}$, higher output resistance and higher voltage capability for a given speed [10]. The range of technologies on the market today offers HBTs with $f_T > 200\text{GHz}$ and sometimes $f_{max} > 300\text{GHz}$. In 2006, the state of the art frequency performance ranged beyond 300 GHz. Indeed, Intel presented frequencies transition record of 360 GHz and 420 GHz f_T and f_{max} [11]. In 2005, IBM presented a transistor on SOI nFET with 290 and 450 GHz f_T and f_{max} [12] respectively. In 2010, IHP invented an HBT with a maximum oscillation frequency of 500GHz under DOTFIVE project which is considered as the highest for SiGe devices till date. The follow up project DOTSEVEN is targeting the development of SiGe:C HBTs technologies with cut off frequencies f_{max} of around 700 GHz. This opens the door for terahertz (THz) applications.

Thus, the context of this thesis is part of the recent progress of millimeter range of components such as silicon MOSFETs on solid substrate ("bulk") and hetero-junction bipolar transistors (HBT) based SiGe: C.

i. MOSFET technology

Micro and nano technologies tend towards the miniaturization of device to reach ultimate higher performances. The progress has been driven by the downscaling of the components in large-scale-integration. Since last 20 years CMOS became the technology of choice for general-

purpose integrated circuit applications. Advantages of CMOS technology are low static power consumption, simple laws of scalability, stability of operation and not only for digital circuits but also for analog and RF circuits. A large part of the success of the MOS transistor is due to the fact that it can be scaled to smaller dimensions, which results in higher performance. The ability to improve performance consistently while decreasing power consumption has made CMOS architecture the dominant technology for integrated circuits. The scaling of the CMOS transistor has been the primary factor driving improvements in microprocessor performance. Transistor delay times have decreased by more than 30% per technology generation resulting in a doubling of microprocessor performance every two years [13], [14]. In order to maintain this rapid rate of improvement, aggressive engineering of the source/drain and well regions is required. In *Figure V* Intel’s commercial process technology is shown which employed 90 nm MOSFET in 2003 and recently reaches to below 32 nm dimension in 2011.

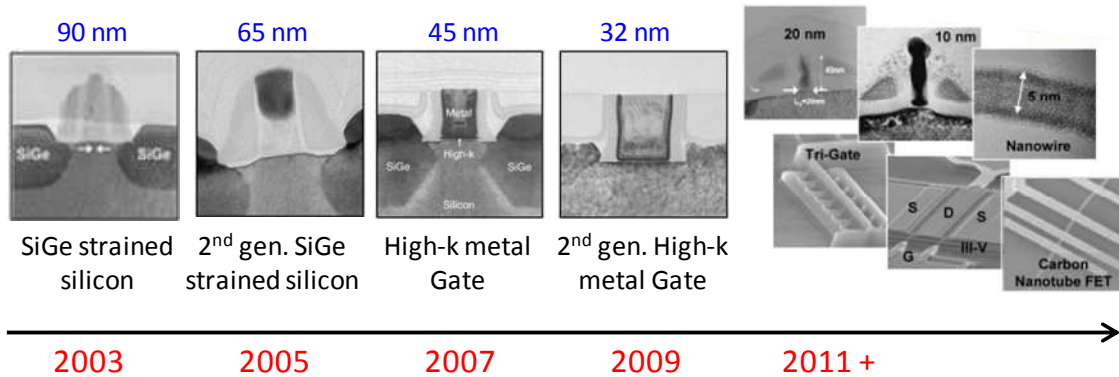


Figure V: Device scaling as projected by Intel; source [15], [16]

CMOS transistors follow the well-known Moore’s Law of scaling, thus leading to always increasing functional integration. The physical gate length is reduced to shrink the CMOS device. For MOS device, $f_T \propto 1/L_G$ (L_G = gate length) and as a first order approximation, is independent of the gate oxide thickness [17]. f_T as high as above 350GHz are reached in the 65nm node of Intel’s high power (HP) devices. Collected f_T data with L_G scaling from several major semiconductor foundries show good conformity with the ITRS road map as shown in *Figure VI*.

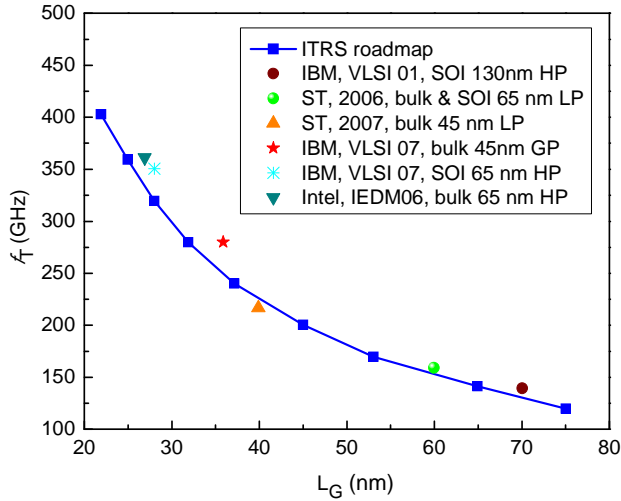


Figure VI: f_T with gate length L_G - ITRS road-map and several foundries' performances; source [9].

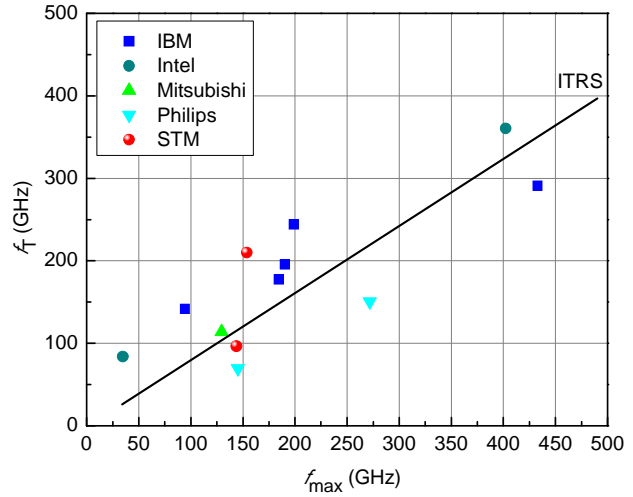


Figure VII: $f_T - f_{max}$: ITRS road-map and several foundries' performances; source [7], [8].

ii. SiGe BiCMOS technology

High-performance silicon-germanium (SiGe) technology already addresses the demands of high frequency transceivers for millimeter wave applications [18]. The rapid technology development has made SiGe being a feasible alternative to III-V compound semiconductors for many microwave and millimeter-wave applications [19]. The development of SiGe Heterojunction bipolar transistor (HBT) has progressed rapidly in recent years. In terms of f_T and f_{max} , SiGe HBTs have advanced from 100 GHz of a few years ago to today's 300 GHz and beyond in several research laboratories as described in *Figure VIII*.

BiCMOS technology is the combination of Bipolar and CMOS technology [20], [21]. Bipolar technology provides high switching speed and good noise performance. On the other hand, CMOS technology offers less power dissipation and higher packaging density. Following both bipolar and CMOS technology, BiCMOS technology achieve improved speed over CMOS and lower power dissipation than bipolar. The introduction of Silicon-Germanium (SiGe) in the base region of silicon-based bipolar transistors offers improved overall performance at higher operating frequencies. SiGe BiCMOS technology features important advantages such as [22]:

- (i) inherently high forward current gain,
- (ii) homogeneous high integration of bipolar transistors and CMOS,

- (iii) power saving due to a higher transit frequency (f_T) allowing a lower bias current for a given gain at a given frequency, and
- (iv) lower noise figure and high linearity.

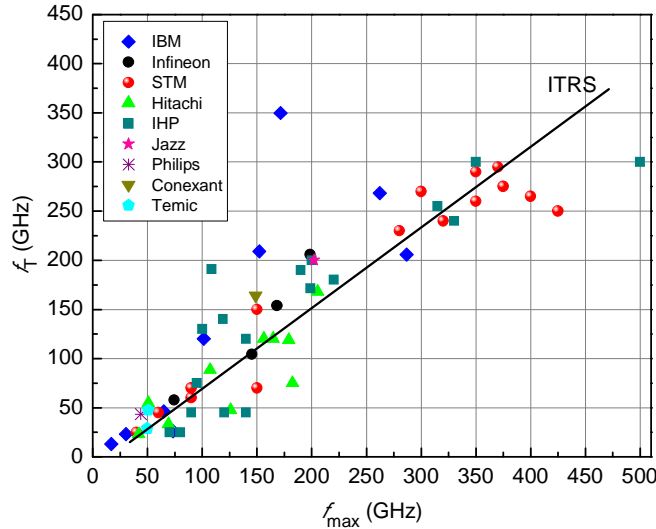


Figure VIII: f_{max} and the associated f_T data for selected SiGe HBT vendors; source [19].

The first STMicroelectronics technology capable of addressing the mm-wave domain was BiCMOS9 [23]. The 120-nm SiGe BiCMOS9 process offers a quasi self-aligned (QSA) 160 GHz f_T/f_{max} Si/SiGeC HBT, dual V_T (high performance / low leakage) and dual gate oxide (1.2 V / 2.5 V) 120-nm CMOS devices, passives and a 6-level copper back-end. This BiCMOS9 technology was mainly developed for optical networking and wireless applications up to 40 Gb/s - 40 GHz, and is the most advanced high-speed SiGe BiCMOS technology currently in production at STMicroelectronics. However, higher device performance is required to meet the needs of circuits operating at frequencies > 50 GHz and targeting 77 GHz automotive radars, 60 GHz WLAN, 100 Gb/s optical communications or non-intrusive imaging technologies [24], [25]. A new technology of STMicroelectronics, 120-nm SiGe BiCMOS9MW [26], is dedicated to millimeter-wave applications. The SiGe BiCMOS9MW has a 230-GHz f_T / 280-GHz f_{max} HBT, which is achieved with a fully self-aligned (FSA) architecture using selective epitaxial growth of the base. The device features record low minimum noise figures: NF_{min} of 1.2 dB at 40 GHz and 1.6 dB at 60 GHz. This BiCMOS9MW technology is mainly intended for 60-GHz WLAN, 77-

GHz automotive radars and 80-Gb/s optical communications. The main characteristics of the technology are summarized in *TABLE I*.

TABLE I

ST Microelectronics 120-nm high-speed SiGe BiCMOS technologies; source: [26]

Technology Targets	BiCMOS9		BiCMOS9MW	
CMOS	$T_{OX} = 20 \text{ nm (GO1)} / T_{OX} = 50 \text{ nm (GO2)}$			
(NMOS & PMOS)	High & Low V_T (mV)			
N: 120nm/1.2V (GO1)	450	340	450	340
P: 120nm/1.2V (GO1)	395	300	395	300
N: 280nm/2.5V (GO2)	430	140	430	140
P: 280nm/2.5V (GO2)	485	180	485	180
Si/SiGe:C HBT	QSA structure ($W_E=170 \text{ nm}$)		FSA structure ($W_E=120 \text{ nm}$)	
f_T (GHz)	160		230	
f_{max} (GHz)	160		280	
BV_{CEO} (V)	1.8		1.6	
BEOL (Cu)	6ML + Al		6ML + Al	
<i>thin / thick Cu layers</i>	5 / 1		3 / 3	
$\alpha @ 80\text{GHz}$ (dB/mm)	1.2		0.5	

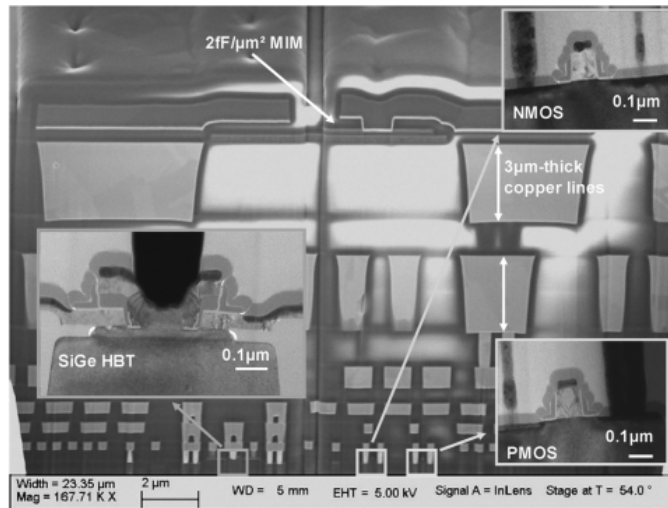


Figure IX: SEM cross-section of the technology (BiCMOS process and device features) with thick-copper back-end, MIM capacitor and TEM pictures of the HBT and MOSFETs; source: [27], [28].

STMicroelectronics developments within DOTFIVE project [29] are based on a state-of-the-art 130nm SiGe BiCMOS technology optimized for very high frequency applications [27]. As shown in *Figure IX*, this technology includes a dedicated copper metallization scheme with two 3 μ m thick levels to minimize signal attenuation at mm-wave frequencies ($\alpha \sim 0.6\text{dB/mm}$ at 80GHz). Figure shows a cross-sectional view of the technology showing the three active devices, the MIM capacitor and the back-end interconnections.

In *Figure X*, the roadmap of ST BiCMOS process technologies is shown. *Figure X (b)* summarizes the various steps in the optimization of high speed SiGe HBT performances from BiCMOS9MW (230-GHz f_T / 280-GHz f_{max}) to B3T (260-GHz f_T / 350-GHz f_{max}) and B4T (265-GHz f_T / 400-GHz f_{max}) [27].

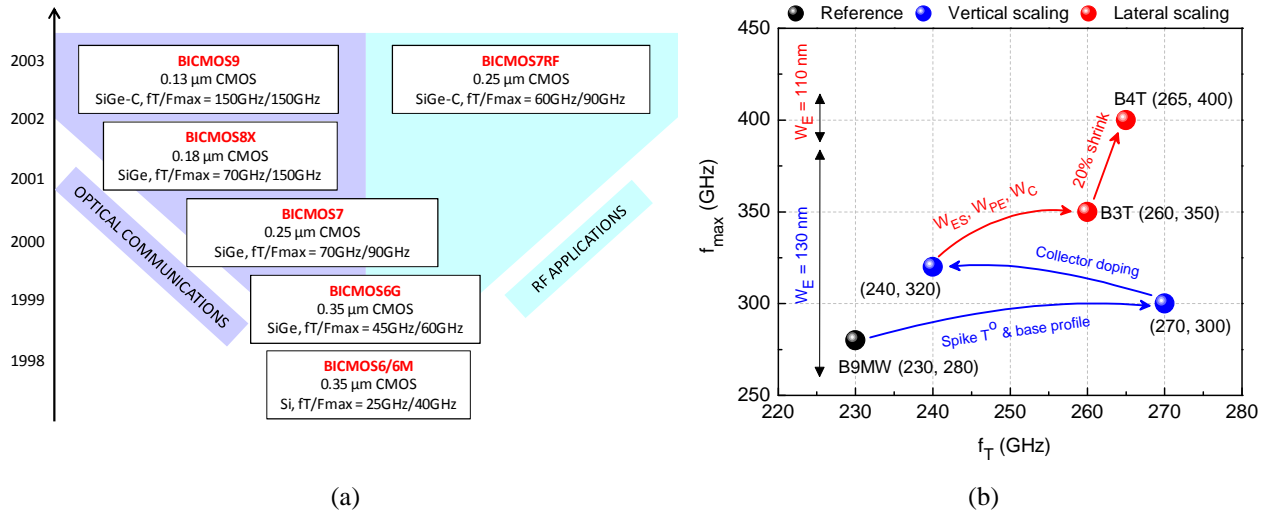


Figure X: Different BiCMOS process technology developed by ST microelectronics – (a) roadmap of ST BiCMOS process; source [30], (b) from BiCMOS9MW to B3T and B4T technology; source [27].

C. Power density and thermal phenomena

Ever increasing demand for faster microprocessors and the continuous trend to pack more transistors on a single chip (*Figure XI*) have resulted in an unprecedented level of power dissipation [16]. Moreover, power density of the transistor increases noteworthy due to the geometry shrinking. In *Figure XII*, the evolution of power density with critical device dimension of Intel’s transistor is shown.

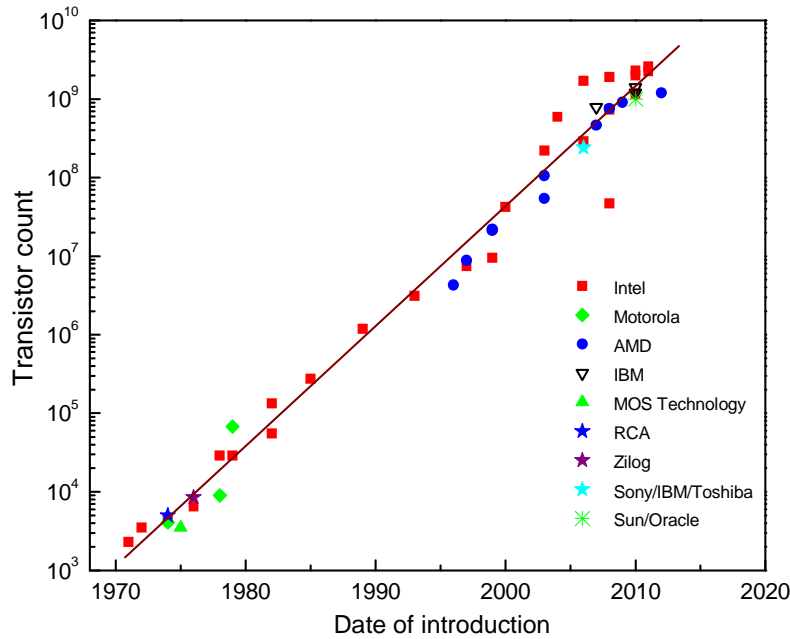


Figure XI: Transistor count per chip with introduction of year; source [7], [16].

The following well-known Moore’s law, the improved device integration pursued in order to support high current capability, has led to a steady increase in power density [31–34]. This significantly contributes to even higher device and system operational temperature. Thermal phenomena influence the electrical functionality and performance of semiconductor devices and also adversely affect their reliability. The major thermally-induced reliability concerns for transistors are [16]:

- (i) degradation of device electrical characteristics due to heating effects,
- (ii) stresses due to different rates of thermal expansion of transistor constituents, and

- (iii) failure of metallic interconnects due to diffusion or flows of atoms along a metal interconnect in the presence of a bias current, known as the electro-migration phenomenon.

Self-heating of the device reduces electron mobility and results in a poor performance of these devices.

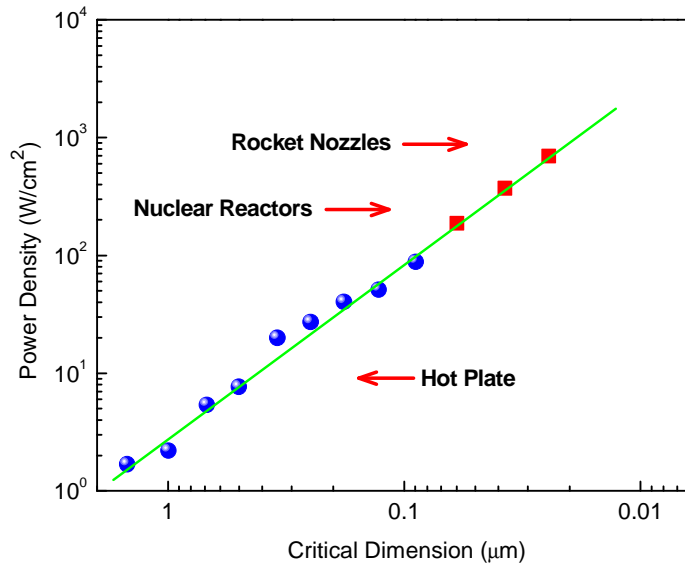


Figure XII: Evolution of the average power with critical dimension of device; source [16], [49], [50].

In microwave applications, SiGe Heterojunction Bipolar Transistors (HBTs) play an important role due to their high linearity and ability to operate at high current densities. Advanced device performance is mainly achieved with shrinking of device dimensions and by improving the device architecture. The high performances bipolar technology requires good device isolation. Structural innovation has contributed to reduce the parasitic elements and to decrease the transit time by introducing shallow trench, deep trench and other technological process steps [35–37]. The major improvements are: (i) parasitic capacitances are reduced by introducing deep trench and shallow trench isolation. The drawback is that, due to lower thermal conductivity of SiO₂ trench wall, the heat flow is confined and resulting larger thermal impedance (Z_{TH}) [38–46]. (ii) In order to boost the transit frequency, a lot of attention is paid to a careful design of the BC junction and the EPI-collector. It permits to push the Kirk-effect to higher current densities leading to higher transit frequency f_T on the one hand, but on the other hand to lower breakdown voltages with a minimum value of above 1V for ultimately scaled

devices [47]. Finally, it shifts the operating point to higher current densities [48]. Therefore temperature rise induced by the power consumption of devices increase significantly in high power application and thus heat dissipation, the source of heat increase, becomes a major issue to confront. Both aspects for the increase of device performances result in a more pronounced self-heating effect. In a bipolar transistor self-heating occurs mainly in the base-collector depletion region, where both the current and field are high. This can produce negative output impedance, a shift in DC characteristic, as well as concerns about device stability and reliability.

In bipolar technology, a device operating point is essential due to the thermal reliability issue. A transistor Safe Operating Area (SOA) is limited by various breakdown mechanisms [34], [51–54]. According to the *Figure XIII*, the first breakdown is caused by avalanche multiplication that is the multiplication of the carriers in the space charge region. The second breakdown is caused by electro-thermal effects and impact ionization. Following the *Figure XIII*, maximum device temperature (T_{max}) boundary is limited by SOA. This SOA is minimized with increase of current density i.e., device down-scaling. The increase in power density leads to higher operating temperature. The temperature rise ΔT in a bipolar device can be given by,

$$\Delta T = R_{TH} \cdot A_E \cdot J_C \cdot V_{CE} \tag{Eq. 1}$$

where, R_{TH} , A_E , J_C and V_{CE} are the thermal resistance, emitter area, current density and collector-emitter voltage respectively. Following the *Eq. 1*, the higher current density due to down scaling issue is the cause of device temperature increase.

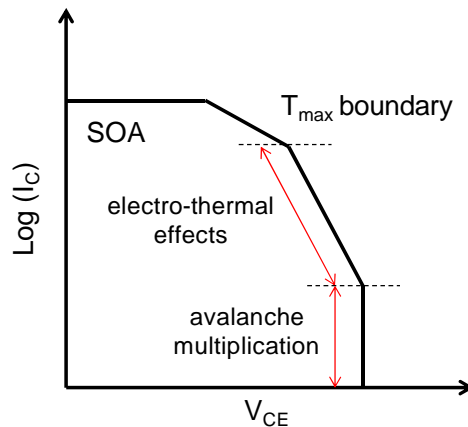


Figure XIII: Transistor safe operating area due to avalanche multiplication and electro-thermal effect; source [34].

D. Motivation

Thermal issue is one of the key factors limiting the performance and reliability of the devices and integrated circuits. Consequently, realistic thermal compact modeling is strongly mandatory in order to obtain accurate simulation results taking into account the intrinsic operating temperatures. The excessive temperature has underscored the need of thermal effect characterization in device compact models. An accurate determination of the device thermal impedance is required to specify operating temperature. Characterization of thermal phenomena is necessary for thermal stability and reliability analysis for modern bipolar circuits design. Moreover, the thermal compact model must also be valid up to the RF range. The electrical behavior is also influenced by the dynamic variations of junction temperature [55] which can have significant impact on third-order intermodulation products generated near the thermal time constant due to the nonlinearity of the device [56]. Therefore, the characterization and modeling of self-heating in electronic devices remains a major research issue associated with the advancement of technology.

It is obvious from the previous discussion that, the self-heating can cause major changes in the device operation when there are considerable temperature rise. In general the extractions of compact model parameters are usually based on steady-state measurements at a single ambient temperature. But, transistor junction (HBT) or channel (MOSFET) temperature rises due to self-heating during the measurements. The resulting steady-state measurements compose a temperature dependent characterization. Therefore, the predictive ability of the compact model could be restricted if the final operating point and thermal environment differ from the one in which the device was characterized. Also, the unphysical nature of extracted parameters can make it difficult to develop a scalable model. The absence of such a scalable model is a significant restriction in the development of analog circuits. Not only the self-heating is important to integrated circuit designers, but it is also dominant concern for the reliability engineers because device operation at high temperatures results a shorter device lifetime. The knowledge of self-heating is needed to extrapolate the statistical estimation of device lifetime.

E. Thesis organization

The thesis is organized as follows:

Chapter 1: Self-heating and device compact modeling - This chapter demonstrates a general overview of self-heating effect in electronic device and a short description on different analytical models, presented in literatures. Transistor compact model has been discussed in brief. The compact model has been verified by static and dynamic measurements.

Chapter 2: Characterization of SiGe:C BiCMOS HBTs - This chapter provides an extensive evaluation of self-heating in microwave SiGe:C BiCMOS HBTs through DC, pulse and low frequency s-parameter measurements. Different methodologies have been applied in order to evaluate steady state, transient and dynamic thermal behavior of the device. Thermal parameters are extracted with HiCuM L2 simulations using different electro-thermal networks at temperature node.

Chapter 3: Characterization of nano-metric MOSFETs - In this chapter, we present the self-heating characterization of nano-metric CMOS technology through DC measurements, pulse measurements and, DC and pulse RF measurements.

Chapter 4: 3D thermal TCAD simulations - This chapter discussed about 3D thermal simulations. TCAD simulations are performed in order to investigate the transient and the dynamic behavior of the device temperature in dependence of the device architecture and material properties. The structure of the transistors is same as the measured one, submicron SiGe:C BiCMOS HBTs.

Chapter 5: Results validations, scalable approach and applications - This chapter presents a comparison of thermal parameters extracted from different measurements and device simulations. A scalable model has been proposed for transient self-heating modeling in trench isolated Si-Ge HBTs. This model has been verified through numerical simulations as well as low frequency s-parameter measurements and found to be in excellent agreement for various device geometries.

F. Project description

This work is the part of DOTFIVE project (BiCMOS HBT) and MIRENDELA project (45 nm CMOS).

DOTFIVE [4], [57]: This is an ambitious three-year (2008 to 2010) European project supported by the European Commission through the Seventh Framework Program for Research and Technological Development, focused on advanced Research, Technology, and Development activities necessary to move the SiGe-HBT into the operating frequency range of 0.5 THz (500 GHz). This high frequency performance is currently only possible with more expensive technology based on III-V semiconductors, making high integration and functionality for large volume consumer applications difficult. The new transistors developed by DOTFIVE will be used for designing circuits enabling power efficient millimeter-wave applications such as automotive radar (77 GHz) or WLAN communications systems (60 GHz –Wireless Local Area Network). In addition to these already evolving markets, DOTFIVE technology sets out to be a key enabler for silicon based millimeter-wave circuits with applications in the security, medical and scientific areas. A higher operating speed can open up new application areas at very high frequencies, or can be traded for lower power dissipation, or can help to reduce the impact of process, voltage and temperature. The project involves 15 partners (University of Naples-Italy, ST Microelectronics-France, IMEC Microelectronics-Belgium, IMS-University of Bordeaux 1-France and Bundeswehr University Munich-Germany.) from industry and academia in five countries teaming up for research and development work on silicon-based transistor architectures, device modeling, and circuit design.

MIRANDELA [58], [59]: This is a research project within the ENIAC - Technology Platform. The project aims to the **MI**llimetre-wave and **R**adio-frequency integr**A**tion in **N**anoelectronics **C**MOs Platforms for **MoDE**rn **WireLess** **5A** Communications. Starting from core CMOS nodes, specific works will be conducted in order to offer a silicon technology platform adequate for the development of modern wireless communication applications. They can be “labeled” as **5A** communications: **A**nanything to be transferred from/to **A**n**y**body located **A**n**y**where at **A**n**y**time using the most appropriate physical path from **A**n**y**-path available between the sender and the recipient based on performance and/or economical considerations. A significant effort will be devoted to the architecture of RF and millimeter-wave functions. In addition to traditional analog

RF design, there are several new ideas that will be eventually deployed in such a technology node: millimeter-wave design in pure CMOS, RF design at very low power consumption, auto calibration of RF functions, etc. The capability of these technologies will be demonstrated through the development of mixed signal very low power RF circuits to be used for autonomous reconfiguration and communication nodes supporting for multiple RF air interface protocols.

Starting from a standard CMOS technology node (e.g. 32nm to be shrunk to 28nm), the project intend to derive a technology and design platform for the integration of analog, RF and MMW components, blocks and functions together with the digital base-band on a same chip in order to address the very promising mobile communication market as indicated by the evolution of the smart phone sales. Our view of the next generations of mobiles phone is on one hand the low cost market of emerging countries and the evolution to very sophisticated smart phone able to replace PC, TV, video recorder, video storage and much more devices all in a pocket. To address such markets we need to integrate more function on the same chip for production cost consideration for low end products that will anyway propose more communication paths (2G, Bluetooth) or for high end products where High Data Rates are mandatory for large file transfers (picture, personal or commercial video for instance).

G. Technology under analysis

In this work, transistors with two different technologies are taken for self-heating analysis.

❖ *SiGe BiCMOS9MW HBT*

The analyzed device is SiGe NPN HBTs. The transistors are fabricated within the ST Microelectronics with SiGe BiCMOS9MW technology, which is a quasi self-aligned trench isolated technology. The key figures of this technology are: breakdown voltage, $BV_{CEO} = 1.6$ V, $BV_{CBO} = 5.5$ V, transit frequency (f_T) = 230 GHz and maximum oscillation frequency (f_{max}) = 290 GHz. A TEM cross-section of the BiCMOS9MW HBT is shown in *Figure XIV*.

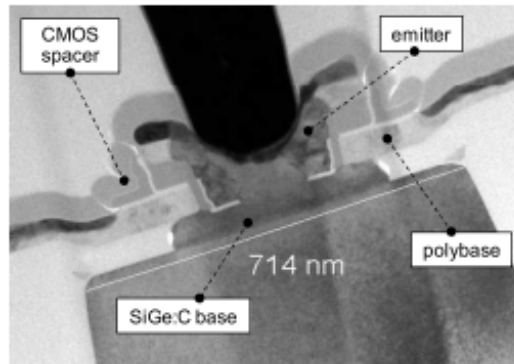


Figure XIV: TEM picture of BiCMOS9MW self-aligned SiGe HBT; source: [27].

The device (taken for characterization) specification: (i) the maximum safe operating range: collector – emitter voltage (V_{CE}) = 1.5 V and base – emitter voltage (V_{BE}) = 0.05 V; (ii) the dimensions of the drawn emitter window: $L_E \times W_E$ (μm^2) = 3 x 0.27, 5 x 0.27, 10 x 0.27, 15 x 0.27, 10 x 0.54, 10 x 0.84 and 10 x 1.08; and (iii) transistor configuration: CBE (1 emitter, 1 base and 1 collector) and CBEBC (1 emitter, 2 base and 2 collector).

❖ *CMOS 045 MOSFET*

In this work, CMOS045 (SVT25 / SVTLP) RF MOS technologies are characterized. The device specification: (i) the maximum safe operating range: for SVT25 RF MOS, drain – source voltage (V_{DS}) = 2.5 V and gate – source voltage (V_{GS}) = 2.5 V; for SVTLP RF MOS, $V_{DS} = 1.2$ V and $V_{GS} = 1.2$ V (ii) transistor configuration: SVT25 transistors are with 10 fingers (finger width = 3 μm) with 4 MOS parallel and SVTLP transistors are with 10 fingers (finger width = 2

μm) with 6 MOS parallel. The total gate width (W_G) = 120 μm for both SVT25 and SVTLP. The transit frequency f_T with L_G is given in *Figure XV*. The f_T is extracted at 10 GHz frequency (not deembedded).

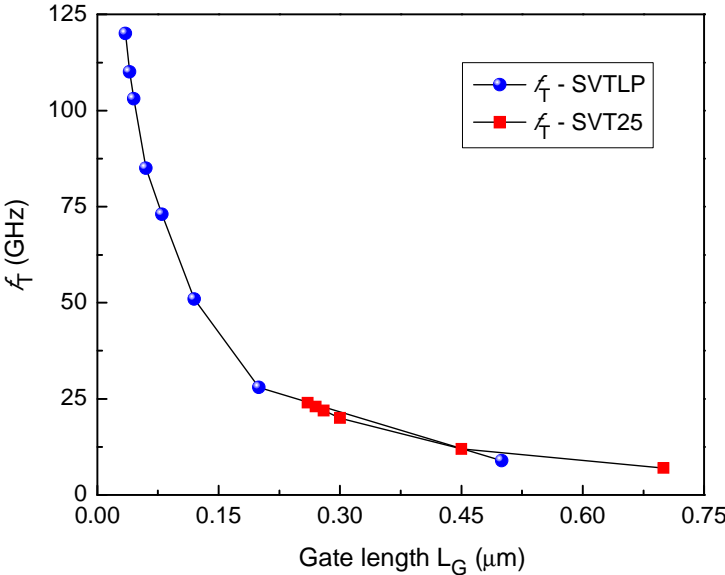


Figure XV: Measured (extracted at 10 GHz frequency) f_T with gate length L_G .

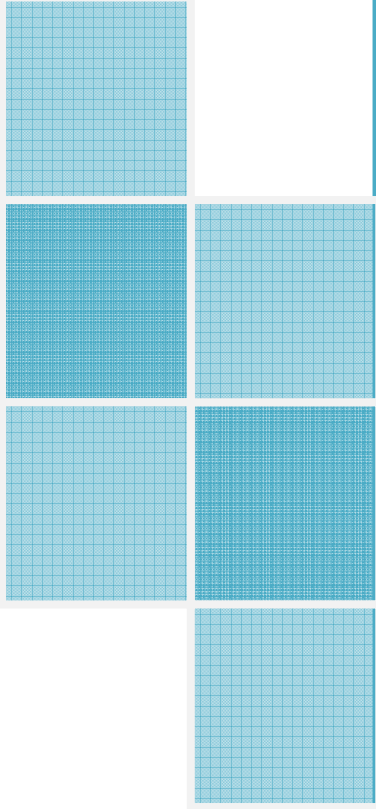
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A decorative graphic on the left side of the page, consisting of a grid of blue squares. The grid is arranged in a cross-like shape, with a vertical column of four squares and a horizontal row of three squares, overlapping in the middle. The squares have a fine grid pattern.

Self-heating and device compact modeling

This chapter demonstrates a general overview of self-heating effect in electronic device and a short description on different analytical models, presented in literatures. Transistor compact model has been discussed in brief. The compact model has been verified by static and dynamic measurements.



1.1 Introduction

The temperature rise in a chip is mainly due to three different mechanisms; (i) self-heating in the device because of power dissipation, (ii) thermal coupling between neighboring device and (iii) chip to package and package to ambient thermal impedance. This thesis concentrates to investigate the first effect, the thermal phenomena inside the device, as it has a major impact on analog circuits.

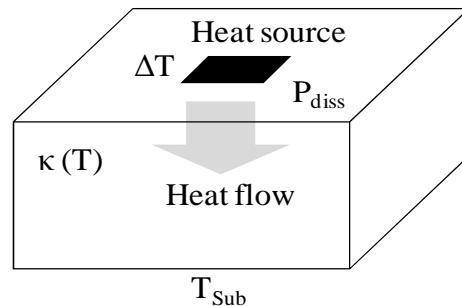


Figure 1-1: A semiconductor device with a heat source of power dissipation P_{diss} : the heat flow coupled with substrate thermal conductivity $\kappa(T)$ results in a temperature rise of heat source ΔT .

The self-heating is the process by which power dissipation of the device alters its temperature. Heat is generated only in a localized portion of the transistor and conduction of heat away from this region into the surroundings is limited due to several reasons and, therefore, device temperature rises. In general, this temperature rise is non uniform. The device operation is a time-average power dissipation, which results in a heat flow from the heat source to the backside of the substrate. The backside of the substrate is considered to be controlled by the external environment to a substrate temperature T_{sub} . The heat flow to the backside of the wafer, coupled with the thermal conductivity of the semiconductor wafer on which the device is fabricated, results in a temperature rise of the device above the ambient temperature. The heat flow from the thermal source to the top of the device via the interconnect metallization is usually assumed to be negligible. In many cases it is necessary to account for the temperature dependence of the thermal conductivity and also the possibility for the power dissipation. The temperature dependent power dissipation causes electro-thermal feedback. Solution of the equations describing the non-linear system illustrated in *Figure 1-1* gives the temperature distribution throughout the device under study; it is this temperature rise that is a direct result of self-heating.

1.1.1 Electrical representation of thermal system

The propagation of heat in a medium can take place in three different ways, convection, radiation and conduction. The electronic components generally have only the heat conduction. In a homogeneous isotropic material medium it is described by a parabolic partial differential equation,

$$\frac{\partial^2 T}{\partial x^2} = \frac{c\rho}{\lambda_{th}} \frac{\partial T}{\partial t} \quad \text{Eq. 1-1}$$

In the above equation, λ_{th} stands for the specific heat conductance, c for the specific thermal capacitance and the ρ for the density of the material. T describes the temperature and x the coordinates in the direction of heat propagation.

In order to investigate for an electrical analog model, the comparison with a transmission line comes contiguous [1]. The transmission line equation describes all the properties for a wave such as reflection, standing wave etc. which is expressed by a much more complex form,

$$\frac{\partial^2 U}{\partial x^2} = C'L' \frac{\partial^2 U}{\partial t^2} + (C'R' + G'L') \frac{\partial U}{\partial t} + G'R'U \quad \text{Eq. 1-2}$$

Here C' is the capacitance per unit length, R' the resistance per unit length, G' the transverse conductance per unit length and L' the impedance per unit length.

It is considered that, in the field of heat conduction in solid, there is no direct comparison for electrical term of inductance, because a volume element cannot cool itself [1]. This can be described by $L'=0$ and $G'=0$. Therefore the transmission line equation is reduced to

$$\frac{\partial^2 U}{\partial x^2} = C'R' \frac{\partial U}{\partial t} \quad \text{Eq. 1-3}$$

The structure of the *Eq. 1-3* is same as *Eq. 1-1*. In 1845 Kirchhoff stated that, “two different forms of energy behave identically when the basic differential equations which describe them have the same form and the initial and boundary conditions are identical”.

According to the *Eq. 1-1* and *Eq. 1-3* heat conduction process can be modeled by transmission line equivalent circuit diagram which consist of resistance R and capacitance C elements. The analogy between electrical and the thermal quantities are: voltage at a node of an

equivalent circuit (U in V) is the temperature in the device (T in K), current (I in A) is the heat flux (P in W), resistances (R in V/A) and capacitances (C in As/V) are thermal resistances (K/W) and thermal capacitances (Ws/K) respectively.

1.1.2 Thermal modeling of electronic system

In order to characterize the self-heating effect, it is necessary to understand the way in which increases to the operating temperature at the device will subsequently alter device performance. The thermal behavior of a homogeneous isotropic volume element containing no internal heat source is governed by heat equation. In Cartesian coordinate it is described by,

$$\nabla^2 T = \frac{c\rho}{\lambda_{th}} \frac{\partial T}{\partial t} \quad \text{Eq. 1-4}$$

In the above equation, λ_{th} stands for the specific heat conductance in W/m°C, c for the specific thermal capacitance in J/Kg°C and the ρ for the density of the material in Kg/m³. For most material, thermal conductivity is a nonlinear function of temperature, which greatly complicates the problem. In general, it cannot be solved even for very simple geometries, using numerical techniques and thus simplifications and approximations are required to process analytical solution of the problem. With proper initial and final boundary conditions, the temperature can determined as a function of time (t) and position (r) within the conducting media.

The thermal resistance, R_{TH} can be expressed in the terms of the ratio of the final value of the temperature at a given position and the dissipated power, P_{diss} from the heat source as:

$$R_{TH}(r) = \frac{T(r, t = \infty) - T(r, t = 0)}{P_{diss}} = \frac{\Delta T(r)}{P_{diss}} \quad \text{Eq. 1-5}$$

Even the R_{TH} is a function of r , it is conventional to represent R_{TH} as the thermal resistance at the region inside the device with the maximum temperature, called the junction temperature T_j . R_{TH} of a device can be extracted from the relation between the T_j and the P_{diss} . Such a relation is generally obtained by exploiting the temperature dependence of an electrical parameter of the device, in which the electrical parameter is measured at various power levels and then converted into temperature variations by a careful calibration. Hence, the following spatial independent formula is widely accepted:

$$R_{TH} = \frac{T_j - T_{amb}}{P_{diss}} \quad Eq. 1-6$$

where T_{amb} is the temperature in the absence of power dissipation or the ambient temperature. P_{diss} in the device is calculated using the following formula,

$$P_{diss} = I_C \cdot V_{CE} + I_B \cdot V_{BE} \quad Eq. 1-7$$

where I_C and I_B are the collector current and base current respectively, and V_{CE} and V_{BE} are the collector-emitter voltage and base-emitter voltage respectively.

The R_{TH} is sufficient to describe the relationship between temperature and dissipated power for steady state conditions. However, for transient behavior, the concept of thermal capacitance C_{TH} is used. The general expression for the C_{TH} in a solid is given by,

$$C_{TH} = \rho \cdot c \cdot V \quad Eq. 1-8$$

where c is the specific heat capacity, ρ is density and V is the volume to be heated. The assumption is made here that the temperature is uniform throughout the volume V . But, for practical device structures a thermal gradient always exists inside the device. Also the volume, V , is not clearly defined since the substrate around the device is partially heated. In such cases C_{TH} evaluated from *Eq. 1-8* will lead to incorrect results. The way to prevent this is to estimate C_{TH} from time response of the T_j to the P_{diss} .

1.1.3 One dimensional modeling approach

In electronic device like bipolar transistors or MOSFET, the heat diffusion phenomena from the heat source to heat sink can be modeled with the transmission line equivalent circuit diagram. In this case, the electrical power source $P(t)$ represents the power dissipation P_{diss} (heat flow) occurring in the device in thermal equivalent. In physical reality, the parameters of the transmission line equivalent circuit exhibits one-dimensional heat flow. Therefore, the thermal resistance and capacitance per unit length need to be considered for exact characterization of the thermal properties of a component. However, for simplicity, it is useful and acceptable to combine single volume elements in lumped equivalent elements [1]. In this approach the segmentation of the complete device structure is considered as a sum of partial volume elements. The assumptions state that:

- The graduation of layer thickness should be chosen so that progressively larger thermal time constants ($\tau_{\text{Thermal}} = R_{\text{THi}} C_{\text{THi}}$) are produced in the direction of heat propagation.
- If the heat inducing area (heat source) is smaller than the heat conducting material cross section, the heat spreading region can be assume by a spreading angle α (Figure 1-2)
- Unlike the division of layers through which heat is conducted, the size of each volume element in which heat is produced must be determined exactly, because in transient power dissipation, its heat capacity has a decisive influence on the thermal impedance.

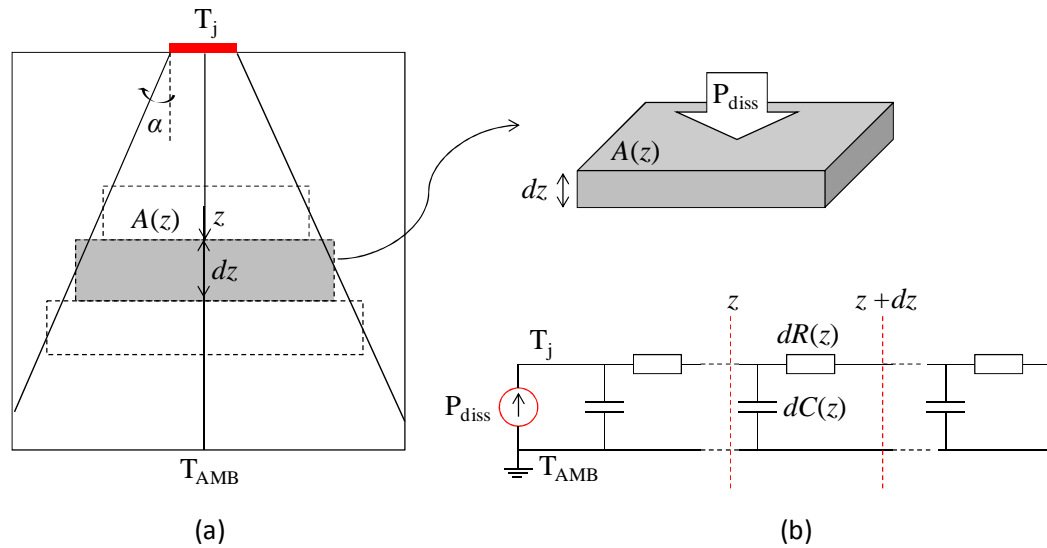


Figure 1-2: (a) Heat diffusion within spreading angle α in a simple structure (b) electrical transmission line equivalent circuit diagram.

Let us consider heat is dissipating from a rectangular heat source towards substrate region of the device. The substrate material is characterized by a thermal conductivity κ and a specific heat per volume unit C_v . While the heat is flowing in the z direction it spreads out under an angle α in both x and y directions as shown in Figure 1-2 (a). It is well known that the time-dependent diffusion of heat can be modeled by a distributed RC-network [2]. An elementary horizontal slice at depth z with thickness dz can be characterized by resistance $R(z)dz$ and a capacitance $C(z)dz$ as follows (Figure 1-2 (b)):

$$dR(z) = \frac{1}{\kappa A(z)} dz, \quad dC(z) = C_v A(z) dz \quad \text{Eq. 1-9}$$

where $A(z)$ is the cross-section area of the heat flow path at a distance z from heat source. Following the Eq. 1-9, the thermal equivalent elements of the *Figure 1-2 (b)* can be determined directly from the physical structure. Therefore, from the thermal point of view a solid system can be described by means of a discrete element electrical circuit, composed by resistances and capacitances.

1.2 Analytical model and electro-thermal network topologies

The thermal behavior of an electronic component can be described correctly by a complete closed-form analytical solution [3]. However, the analytical resolution of generalized heat equation remains a complicated job due to the nonlinear problems and therefore, simplifications and approximations are needed.

Joy and Schlig performed theoretical studies on the variation of thermal resistance of a rectangular parallelepiped thermal source buried in a semi-infinite medium as a function of the source dimension [4]. This study is based on integration of the instantaneous point source over the volume of the thermally active region to yield an estimate of device thermal resistance, and provides a comprehensive study of scaling of thermal resistance. The model assume that-

- The top surface of the semiconductor is adiabatic.
- The effect of conduction through interconnect metallization is negligible and this does not affect the thermal resistance for large device.
- The power dissipation of the thermal source is independent of position inside the heat source.

Using these assumptions Joy and Schlig show that R_{TH} of the most devices can be shown as,

$$R_{TH} = \frac{1}{4\kappa\sqrt{LW}} \quad \text{Eq. 1-10}$$

where L and W are the length and width of the heat source respectively. The above equation provides an absolute estimate of the R_{TH} for a rectangular thermally active region.

In most common compact models, the device temperature rise due to self heating effect is represented by a single pole electro-thermal equivalent network as given in *Figure 1-3*. The thermal impedance in Laplace domain $Z_{TH}(p)$ is given by:

$$Z_{TH}(p) = \frac{R_{TH}}{1 + pR_{TH}C_{TH}} \quad \text{Eq. 1-11}$$

where p is the Laplace variable.

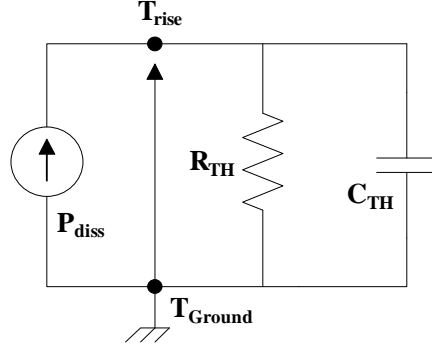


Figure 1-3: A single pole electro-thermal network

The first order self-heating model given by the dynamic relationship between instantaneous power dissipation and device temperature rise is:

$$T_{rise}(t) = \Delta T \left(1 - \exp\left(-\frac{t}{\tau_{Thermal}}\right) \right) \quad \text{Eq. 1-12}$$

Where, $\Delta T = P_{diss}(t) \cdot R_{TH}$ is the magnitude of temperature step and $\tau_{Thermal} = R_{TH} C_{TH}$ is the thermal time constant.

A generalized form of the equivalent circuit (Foster network, *Figure 1-4*) is presented in [1]. The heat diffusion process in a medium is expressed as the superposition of an infinite number of modes and each mode is characterized by its eigen-function and its time constant (τ_i) [5]. Therefore a more complete solution of the heat transform problem is:

$$T_{rise}(t) = \sum_{i=1}^n \Delta T_i \left(1 - \exp\left(-\frac{t}{\tau_i}\right) \right) \quad \text{Eq. 1-13}$$

Where $\Delta T_i = P_{diss}(t) R_{THi}$ and $\tau_i = R_{THi} C_{THi}$. Thus the thermal impedance of the generalized thermal equivalent network is given by:

$$Z_{TH}(p) = \sum_{i=1}^n \frac{R_{THi}}{1 + pR_{THi}C_{THi}} \quad \text{Eq. 1-14}$$

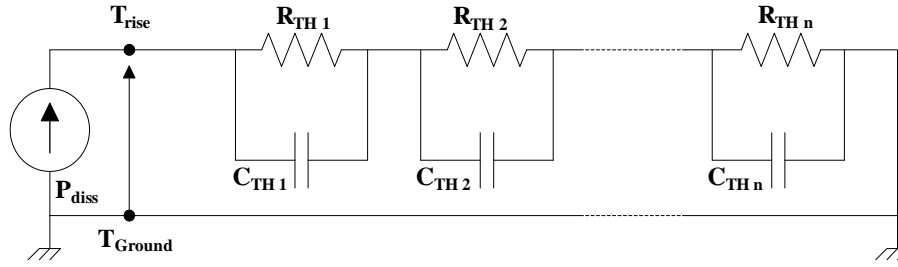


Figure 1-4: Foster network - generalized form of the equivalent circuit.

A single thermal problem resolution is proposed by Mnif, et al [5] for the modeling of self-heating in trench isolated SiGe HBTs. According to this analytical model the thermal impedance can be described as,

$$Z_{TH}(p) = \frac{R_{TH}}{(1 + \sqrt{R_{TH} C_{TH}} \sqrt{p})} \quad \text{Eq. 1-15}$$

Eq. 1-15 describes the one-over square-root dependence of the thermal impedance with respect to the Laplace variable p . Furthermore it gives the resulting thermal spreading impedance in the Laplace domain which can be used directly in frequency domain analysis. In steady-state ($t \rightarrow \infty$, $p \rightarrow 0$), $Z_{TH}(p) \rightarrow R_{TH}$, the thermal impedance can be modeled by a single resistance. In transient-state, we get: ($t \rightarrow \infty$, $p \rightarrow 0$), $Z_{TH}(p) \rightarrow \sqrt{(R_{TH}/pC_{TH})} = Z_{trans}$.

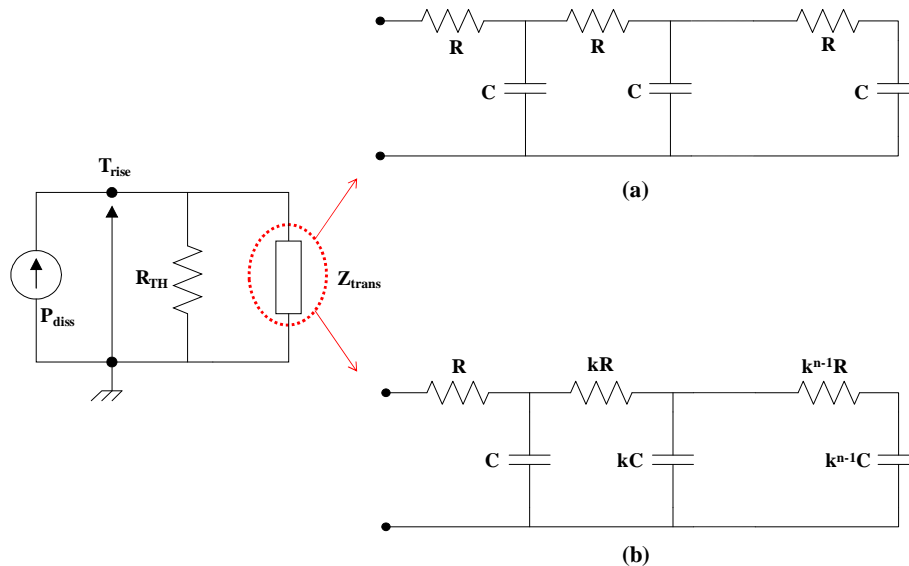


Figure 1-5: The equivalent network for the Z_{TH} - combination of steady state R_{TH} and transient state Z_{trans} , (a) Ladder network and (b) Recursive network.

Thus the resultant thermal impedance is the parallel combinations of impedances in the two states, given in *Figure 1-5*. In transient state, thermal spreading impedance is modeled by: (i) using ladder circuit consisting of n consecutive sections of a series resistance and capacitance connected to ground, given in *Figure 1-5 (a)* or (ii) using recursive network, given in *Figure 1-5 (b)*. *Figure 1-5* gives the resultant thermal impedance $Z(p)$ in the Laplace domain for an infinite number of R-C cells as a recursive form as follows:

$$Z(p) = R + \frac{1}{Cp + \frac{1}{KR + \frac{1}{KCp + \frac{1}{K^2R + \frac{1}{K^2Cp + \dots}}}}} = R + \frac{1}{Cp + \frac{1}{KZ(K^2p)}} \quad \text{Eq. 1-16}$$

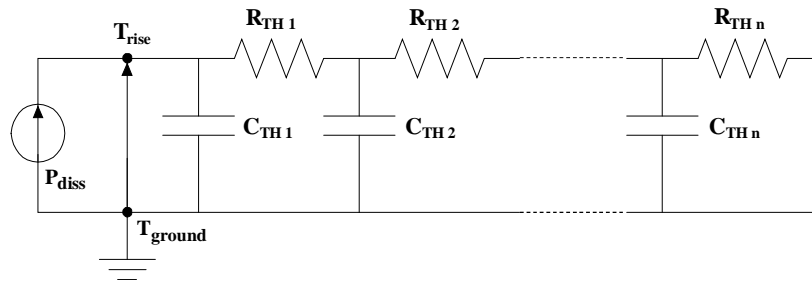


Figure 1-6: The equivalent network for the Z_{TH} – electro-thermal Cauer network

Another electro-thermal network presented in several literature [6–9] is Cauer network as shown in *Figure 1-6*. It is also pointed out by Bagnoli et al. [10] that the Cauer circuits are suitable for representing the system from the physical point of view. Suppose that a certain amount of heat energy is applied to a body made with different materials when the ambient temperature is constant. The thermal power distributes through the entire body until a thermal equilibrium is reached. There are several ways to represent this phenomena using different R-C equivalent circuit. In the electrical circuit, the current flowing across the capacitor during a dynamic regime is the same on both sides of the device due to the symmetrical variation of the positive and negative electric charges. But thermal circuits have no quantities equivalent to negative electric charge. Only the heat flow on one side of the capacitor has a real meaning and the other side should be grounded. Therefore, Ladder, Recursive and Cauer network are more suitable as a thermal analogy from the physical point of view. The time constants in the Foster

network correspond to the R-C product ($R_{THi} * C_{THi}$) of each section where, For a Ladder, Recursive or Cauer network each time constant depends on all the R's and all the C's of the circuit. Hence, the Ladder, Recursive or Cauer network calculation is not straightforward. But it can be possible by transforming these networks to Foster network. Foster network have another advantage that, the thermal time constants for each pole can be added to get the overall time constant of the network.

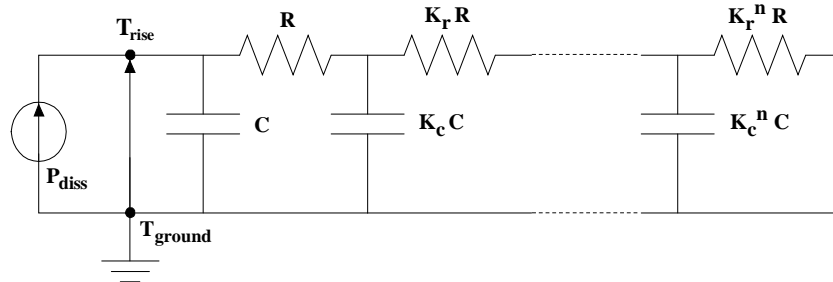


Figure 1-7: A modified recursive network for the Z_{TH} representation (Cauer type network where the aliments are in recursive order).

In Figure 1-5 (b), the transient thermal impedance Z_{trans} is represented by a recursive electro-thermal network where the steady-state thermal behavior is modeled by a single R_{TH} . This network has been modified as given in Figure 1-7. It is seen that, the network is a Cauer type network where the elements are in recursive order. Here different recursive factor (K_r and K_c) is used for R and C. The recursive network can be considered as a physical approach to characterize the steady state or transient thermal spreading behavior of the transistors. The transient variation of device temperature is mainly defined by C_{TH} where the R_{TH} is extracted at steady state condition. In steady state C_{TH} has no meaning. In this case, the sum of resistances of each recursive cell can give the total R_{TH} as follows:

$$R_{TH} = \sum_{n=0}^N K_r^n \cdot R \quad \text{Eq. 1-17}$$

where N is the number of cell in recursive network.

Another analytical model was presented by Veijola and Andersson in [11]. According to this model, the heat diffusion in a material medium can be assumed by the progress of uniformly distributed spherical thermal surface. From the active region of device the diffusion can be simplified as a spherical heat conduction path. Since the temperature of one spherical element is

constant at a certain time it can be represented by one R-C cell. The thermal resistance and capacitance for n^{th} cell of distributed network, situated at a distance z from the heat source, can be represented analytically as follows:

$$R_n = \begin{cases} \frac{1}{4\pi\kappa} \left(\frac{1}{z_n} - \frac{1}{z_{n+1}} \right), n=1 \dots N-1 \\ \frac{1}{4\pi\kappa z_N}, n=N \end{cases}, \quad C_n = \begin{cases} \frac{4\pi\kappa}{3\alpha} z_{n+0.5}^3, n=1 \\ \frac{4\pi\kappa}{3\alpha} (z_{n+0.5}^3 - z_{n-0.5}^3), n=2 \dots N \end{cases} \quad \text{Eq. 1-18}$$

Here N is the total number of cells of the distributed network, κ is the thermal conductivity and α , the heat diffusion coefficient. Following the Eq. 1-9 or Eq. 1-18, the time dependent diffusion of heat can be represented by a distributed recursive network where, the respective thermal resistance element decreases and the capacitance element increases. This behavior can be modeled by the recursive multiplication factor K_r (<1) and K_c (>1) with R and C respectively as shown in Figure 1-7.

All these different types of networks have been used in electro-thermal compact modeling. A comparative study will be presented in Chapter - 2 and 4. Finally a scalable approach for the modified recursive network (Figure 1-7) will be described in Chapter 5.

1.3 Frequency domain thermal impedance for two-port device

In this section a generalized expression for frequency domain Z_{TH} has been derived from y , h and z parameters. Although, several approaches already presented in literature. For example, generalized expressions for thermal impedance from y -parameters are proposed by Rinaldi [12] through a rigorous mathematical treatment. Also dynamic characterization of thermal effect, based on h -parameters has been proposed in [13], [14]. The dispersive phenomenon presented by the device at low frequencies is caused by dynamics self-heating effect. The assumptions, described in [13] are as follows:

- The voltages at two terminals of a two-port device can be described by two nonlinear algebraic functions of currents and the junction temperature (T_j).
- The measured parameters contain two parts: one is an equithermal part or the AC part which is measured at high frequency and the other is the thermal part where the AC self-heating effects are visible.

- The ambient temperature (T_i) is constant during the measurement

At frequencies below the thermal cutoff frequency ($1/\tau_{thermal}$), the junction temperature variation follows the instant power dissipation in the device, leading to harmonic electro-thermal feedback [15]. For the frequencies above $1/\tau_{thermal}$, the junction temperature variation cannot longer follow the instant power dissipation: the electro-thermal feedback is no more significant and the device behavior is dominated by its electrical characteristics only.

1.3.1 Z_{TH} formulation from y-parameters

The base (I_B) and collector (I_C) currents of two-port HBT can be described by two nonlinear algebraic functions of Base-Emitter voltage (V_{BE}), Collector-Emitter voltage (V_{CE}) and the junction temperature (T_J):

$$\begin{aligned} I_B &= F_1(V_{BE}, V_{CE}, T_J) \\ I_C &= F_2(V_{BE}, V_{CE}, T_J) \end{aligned} \quad \text{Eq. 1-19}$$

In terms of base-plate temperature (T_i), which is kept constant during the measurement by means of a thermal chuck, the Eq. 1-19 can be represented as:

$$\begin{aligned} I_B &= F_1^{DC}(V_{BE}, V_{CE}, T_i) \\ I_C &= F_2^{DC}(V_{BE}, V_{CE}, T_i) \end{aligned} \quad \text{Eq. 1-20}$$

Now the y-parameter matrix, given in Appendix-B, can be rewritten as,

$$\begin{aligned} I_B &= Y_{11}V_{BE} + Y_{12}V_{CE} \\ I_C &= Y_{21}V_{BE} + Y_{22}V_{CE} \end{aligned} \quad \text{Eq. 1-21}$$

From Eq. 1-21, y_{22} can be stated as,

$$Y_{22} = \left. \frac{\partial I_C}{\partial V_{CE}} \right|_{\Delta V_{BE}=0} \quad \text{Eq. 1-22}$$

Applying the function given in Eq. 1-20 on Eq. 1-22,

$$Y_{22}(\omega) = \left. \frac{\partial F_2}{\partial V_{CE}} \right|_{non-equithermal} = \left. \frac{\partial F_2}{\partial V_{CE}} \right|_{equithermal} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_{CE}} = Y_{22}^{AC} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_{CE}} \quad \text{Eq. 1-23}$$

Therefore,

$$\frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_{CE}} = Y_{22}(\omega) - Y_{22}^{AC} \quad \text{Eq. 1-24}$$

Now the junction temperature of HBT can be described in terms of thermal impedance and power dissipation as follows [13],

$$T_J = T_i + \int_{-\infty}^{+\infty} Z_{TH}(\tau) \cdot P_{diss}(t - \tau) d\tau = T_i + Z_{TH}(\omega) \cdot P_{diss}(\omega) \quad \text{Eq. 1-25}$$

where $Z_{TH}(\omega)$ is the Fourier transform of $Z_{TH}(t)$ and $P(\omega)$ is the Fourier transform of $P(t)$. Differentiating Eq. 1-25 with respect to V_{CE} at constant V_{BE} ,

$$\begin{aligned} \left. \frac{\partial T_J}{\partial V_{CE}} \right|_{\Delta V_{BE}=0} &= \frac{\partial T_i}{\partial V_{CE}} + \frac{\partial}{\partial V_{CE}} (Z_{TH}(\omega) \cdot P(\omega)) \\ &= Z_{TH}(\omega) \frac{\partial P(\omega)}{\partial V_{CE}} \\ &= Z_{TH}(\omega) \frac{\partial}{\partial V_{CE}} (V_{CE} I_C + V_{BE} I_B) \\ &= Z_{TH}(\omega) \left(I_C + V_{CE} \left. \frac{\partial I_C}{\partial V_{CE}} \right|_{\Delta V_{BE}=0} + V_{BE} \left. \frac{\partial I_B}{\partial V_{CE}} \right|_{\Delta V_{BE}=0} \right) \\ &= Z_{TH}(\omega) (I_C + V_{CE} Y_{22}(\omega) + V_{BE} Y_{12}(\omega)) \end{aligned} \quad \text{Eq. 1-26}$$

The frequency domain thermal impedance is given by,

$$Z_{TH}(\omega) = \frac{(\partial T_J / \partial V_{CE})_{\Delta V_{BE}=0}}{[I_C + V_{CE} Y_{22}(\omega) + V_{BE} Y_{12}(\omega)]} \quad \text{Eq. 1-27}$$

From Eq. 1-24 and Eq. 1-27,

$$Z_{TH}(\omega) = \frac{Y_{22}(\omega) - Y_{22}^{AC}}{(\partial F_2 / \partial T_J) [I_C + V_{CE} Y_{22}(\omega) + V_{BE} Y_{12}(\omega)]} \quad \text{Eq. 1-28}$$

Now at frequency $(\omega) \rightarrow 0$, $Z_{TH}(\omega) \rightarrow Z_{TH}(0) = R_{TH}$ (the equivalent thermal resistance) and $y(0) = y^{DC}$. Thus, from Eq. 1-28, thermal resistance can be given by,

$$R_{TH} = \frac{Y_{22}^{DC} - Y_{22}^{AC}}{(\partial F_2 / \partial T_J) [I_C + V_{CE} Y_{22}^{DC} + V_{BE} Y_{12}^{DC}]} \quad \text{Eq. 1-29}$$

The thermal impedance derived from y_{22} - parameter, can be rewritten in normalized form as follows:

$$Z_{THN}^{22}(\omega) = \frac{Z_{TH}(\omega)}{Z_{TH}(0)} = \frac{(Y_{22}(\omega) - Y_{22}^{AC})}{(Y_{22}^{DC} - Y_{22}^{AC})} \cdot \frac{(I_C + V_{CE}Y_{22}^{DC} + V_{BE}Y_{12}^{DC})}{(I_C + V_{CE}Y_{22}(\omega) + V_{BE}Y_{12}(\omega))} \quad Eq. 1-30$$

In the same way $Z_{TH}(\omega)$ can be calculated from other y -parameters (y_{11} , y_{12} , y_{21}) as given below:

$$\begin{aligned} y_{11}(\omega) &= \left. \frac{\partial F_1}{\partial V_1} \right|_{\substack{\text{non-equithermal} \\ \Delta V_2=0}} = \left. \frac{\partial F_1}{\partial V_1} \right|_{\text{equithermal}} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_1} = y_{11}^{AC} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_1} \\ y_{12}(\omega) &= \left. \frac{\partial F_1}{\partial V_2} \right|_{\substack{\text{non-equithermal} \\ \Delta V_1=0}} = \left. \frac{\partial F_1}{\partial V_2} \right|_{\text{equithermal}} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} = y_{12}^{AC} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} \\ y_{21}(\omega) &= \left. \frac{\partial F_2}{\partial V_1} \right|_{\substack{\text{non-equithermal} \\ \Delta V_2=0}} = \left. \frac{\partial F_2}{\partial V_1} \right|_{\text{equithermal}} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_1} = y_{21}^{AC} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_1} \end{aligned} \quad Eq. 1-31$$

Here,

$$\begin{aligned} \left. \frac{\partial T_J}{\partial V_1} \right|_{\Delta V_2=0} &= Z_{TH} \left(I_1 + V_1 \frac{\partial I_1}{\partial V_1} + V_2 \frac{\partial I_2}{\partial V_1} \right) = Z_{TH} (I_1 + V_1 y_{11} + V_2 y_{21}) \\ \left. \frac{\partial T_J}{\partial V_2} \right|_{\Delta V_1=0} &= Z_{TH} \left(I_2 + V_1 \frac{\partial I_1}{\partial V_2} + V_2 \frac{\partial I_2}{\partial V_2} \right) = Z_{TH} (I_2 + V_1 y_{12} + V_2 y_{22}) \end{aligned} \quad Eq. 1-32$$

From Eq. 1-31 and Eq. 1-32,

$$\begin{aligned} Z_{TH}^{11}(\omega) &= \frac{(y_{11}(\omega) - y_{11}^{AC})}{\frac{\partial F_1}{\partial T_J} (I_1 + V_1 y_{11}(\omega) + V_2 y_{21}(\omega))} \Rightarrow Z_{TH}^{11}(0) = \frac{(y_{11}^{DC} - y_{11}^{AC})}{\frac{\partial F_1}{\partial T_J} (I_1 + V_1 y_{11}^{DC} + V_2 y_{21}^{DC})} \\ Z_{TH}^{12}(\omega) &= \frac{(y_{12}(\omega) - y_{12}^{AC})}{\frac{\partial F_1}{\partial T_J} (I_2 + V_1 y_{12}(\omega) + V_2 y_{22}(\omega))} \Rightarrow Z_{TH}^{12}(0) = \frac{(y_{12}^{DC} - y_{12}^{AC})}{\frac{\partial F_1}{\partial T_J} (I_2 + V_1 y_{12}^{DC} + V_2 y_{22}^{DC})} \\ Z_{TH}^{21}(\omega) &= \frac{(y_{21}(\omega) - y_{21}^{AC})}{\frac{\partial F_2}{\partial T_J} (I_1 + V_1 y_{11}(\omega) + V_2 y_{21}(\omega))} \Rightarrow Z_{TH}^{21}(0) = \frac{(y_{21}^{DC} - y_{21}^{AC})}{\frac{\partial F_2}{\partial T_J} (I_1 + V_1 y_{11}^{DC} + V_2 y_{21}^{DC})} \end{aligned} \quad Eq. 1-33$$

Therefore in normalized form, Z_{TH} s calculated from y_{11} , y_{21} and y_{22} are given by,

$$\begin{aligned}
 Z_{THN}^{11}(\omega) &= \frac{Z_{TH}^{11}(\omega)}{Z_{TH}^{11}(0)} = \frac{(y_{11}(\omega) - y_{11}^{AC})}{(y_{11}^{DC} - y_{11}^{AC})} \cdot \frac{(I_1 + V_1 y_{11}^{DC} + V_2 y_{21}^{DC})}{(I_1 + V_1 y_{11}(\omega) + V_2 y_{21}(\omega))} \\
 Z_{THN}^{12}(\omega) &= \frac{Z_{TH}^{12}(\omega)}{Z_{TH}^{12}(0)} = \frac{(y_{12}(\omega) - y_{12}^{AC})}{(y_{12}^{DC} - y_{12}^{AC})} \cdot \frac{(I_2 + V_1 y_{12}^{DC} + V_2 y_{22}^{DC})}{(I_2 + V_1 y_{12}(\omega) + V_2 y_{22}(\omega))} \\
 Z_{THN}^{21}(\omega) &= \frac{Z_{TH}^{21}(\omega)}{Z_{TH}^{21}(0)} = \frac{(y_{21}(\omega) - y_{21}^{AC})}{(y_{21}^{DC} - y_{21}^{AC})} \cdot \frac{(I_1 + V_1 y_{11}^{DC} + V_2 y_{21}^{DC})}{(I_1 + V_1 y_{11}(\omega) + V_2 y_{21}(\omega))}
 \end{aligned} \tag{Eq. 1-34}$$

In generalized form Z_{TH} can be written as,

$$Z_{THN}^j(\omega) = \begin{cases} \frac{(y_{ij}(\omega) - y_{ij}^{AC})}{(y_{ij}^{DC} - y_{ij}^{AC})} \cdot \frac{(I_j + V_j y_{jj}^{DC} + V_{j+1} y_{j+1,j}^{DC})}{(I_j + V_j y_{jj}(\omega) + V_{j+1} y_{j+1,j}(\omega))}, & \text{for } i=1,2 \text{ and } j=1 \\ \text{or} \\ \frac{(y_{ij}(\omega) - y_{ij}^{AC})}{(y_{ij}^{DC} - y_{ij}^{AC})} \cdot \frac{(I_j + V_{j-1} y_{j-1,j}^{DC} + V_j y_{jj}^{DC})}{(I_j + V_{j-1} y_{j-1,j}(\omega) + V_j y_{jj}(\omega))}, & \text{for } i=1,2 \text{ and } j=2 \end{cases} \tag{Eq. 1-35}$$

1.3.2 The generalized form of Z_{TH}

The assumptions and methodology can be applied on h or z – parameters. This is described in *Appendix – B*. Now Z_{THN} can be expressed as a generalized form (combining Eq. 1-38, Eq. 1-36 and Eq. 1-37) as given below:

$$Z_{THN}^j(\omega) = \left(\frac{x_{ij}(\omega) - x_{ij}^{AC}}{x_{ij}^{DC} - x_{ij}^{AC}} \right) * \begin{cases} \left(\frac{a + b x_{jj}^{DC} + c x_{j+1,j}^{DC}}{a + b x_{jj}(\omega) + c x_{j+1,j}(\omega)} \right), & \text{for } j=1 \\ \left(\frac{a + b x_{j-1,j}^{DC} + c x_{jj}^{DC}}{a + b x_{j-1,j}(\omega) + c x_{jj}(\omega)} \right), & \text{for } j=2 \end{cases} \tag{Eq. 1-38}$$

Where, $j = 1$ represents the Base and 2 the collector terminal of the DUT. The parameter x and the corresponding coefficients a, b and c are given in the *TABLE 1-I*.

Using the above formula, Z_{TH} for different geometries of transistor is extracted from low frequency s-parameters measurements. The s-parameters can be converted to y, h or z –

parameters. Depending on the sensitivity of dynamic self-heating, the parameters need to be chosen for accurate Z_{TH} extraction. This will be presented in the next chapters.

TABLE 1-1
Parameters and the corresponding coefficients of Eq. 1-38

DUT port	x	a	b	c
Base :	y	I_j	V_j	V_{j+1}
$i = 1, 2$	h	V_j	I_j	V_{j+1}
$j = 1$	z	V_j	I_j	I_{j+1}
Collector :	y	I_j	V_{j-1}	V_j
$i = 1, 2$	h	I_j	V_{j-1}	I_{j-1}
$j = 2$	z	V_j	I_{j-1}	I_j

1.4 Compact model

A compact model determines the specific electrical behavior of the component, while meeting the criteria of robustness, convergence of the simulator and simulation time. It is the key element on which the circuit designer can rely and, therefore, the model should provide an accurate picture of physical phenomenon that may affect the behavior of a circuit in the useful operating area of the transistor. Nowadays the famous models for silicon-based bipolar transistors are Gummel-Poon [16], VBIC [17], MEXTRAM [18], and HICUM [19], which are physics based models. For nanometric CMOS device, the main available compact models are BSIM3v3, BSIM (SOI4) [20], EKV [21] and PSP [22].

This work mainly concentrates on HBT compact modeling. HICUM L2 has been taken for device modeling and parameter extraction. A brief description of the model is given below.

1.4.1 High-Current Model (HiCuM)

The name HiCuM was derived from **H**igh-**C**urrent **M**odel. This model is developed taking into account the high current effects which is significant for certain high speed transistor applications. The first version was introduced in 1986 by H.M. Rein and M. Schröter and arrived in the public domain since 1999. This is now a CMC standard model and it is used in a wide

range of simulators like ADS, ELDO-RF, SPECTRE-RF, Smart-SPICE, HSPICE, GoldenGate, HSPICE, SPICE3F5 etc. HiCuM is based on an extended and Generalized Integral Charge-Control Relation (GICCR). However, in contrast to the (original) Gummel-Poon model (GPM) as well as the SPICE-GPM (SGPM) and its variants, in HiCuM the (G)ICCR concept is applied consistently without inadequate simplifications and additional fitting parameters (such as the Early voltages). Since reliable design and optimization of high-speed circuits requires accurate modeling mainly of the dynamic transistor behavior, quantities like depletion capacitances and the transit time of mobile carriers as well as the associated charges, which determine the dynamic behavior, are considered as basic quantities of the model. An accurate approximation of these basic quantities as a function of bias yields, thus, not only an accurate description of the small-signal and dynamic large-signal behavior but also - via the (G)ICCR - of the DC behavior. This coupling between static and dynamic description leads, moreover, to a reduction of "artificial" model parameters like Early voltages and knee currents.

Some of the important physical effects that have been taken into account by this model are briefly summarized below:

- high-current effects (incl. quasi-saturation)
- distributed high-frequency model for the external base-collector region
- emitter periphery injection and associated charge storage
- emitter current crowding (through a bias dependent internal base resistance)
- two- and three-dimensional collector current spreading
- parasitic (bias independent) capacitances between base-emitter and base-collector terminal
- vertical non-quasi-static (NQS) effects for transfer current and minority charge
- temperature dependence and self-heating
- weak avalanche breakdown at the base-collector junction
- tunneling in the base-emitter junction
- parasitic substrate transistor
- band-gap differences (occurring in HBTs)
- lateral (geometry) scalability”

Modeling of these effects is reflected not only in the model equations but also in the topology of the equivalent circuit.

1.4.2 Large signal equivalent circuit

HiCuM large signal equivalent circuit (EC) is shown in *Figure 1-8(a)*. The internal transistor with four nodes E', B', B*, C' is pointed out. The internal circuit contains the diode current i_{jBEi} and depletion charge Q_{jEi} of the BE junction, the diode current i_{jBCi} and depletion charge Q_{jCi} of the BC junction, and the voltage controlled transfer current source i_T . Furthermore, the minority charge is represented by its forward and reverse component, Q_f and Q_r . Moreover, breakdown in the BC SCR is taken into account by the avalanche current source, i_{AVL} , and possible tunneling through the BE SCR is represented by i_{BEti} . The relation of these EC elements to distinctive regions in the transistor structure along with a physics-based description of the elements forms the core of a physics-based compact model.

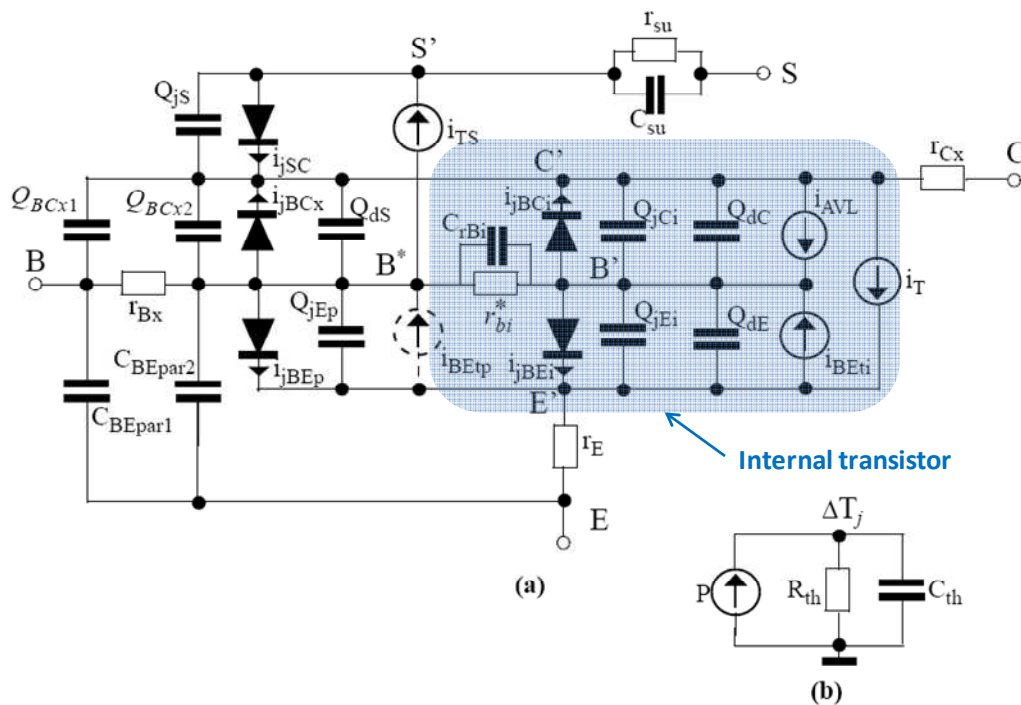


Figure 1-8: (a) Large-signal HiCuM Level2 equivalent circuit. (b) Thermal network used for self-heating calculation [23], [24].

Comparing the equivalent circuit (EC) of HiCuM level 2 with SGPM, one can see there are two additional nodes named B* and S' in HiCuM. For modern transistor, the emitter

periphery effects can play an important role. For this purpose the node B* has been added into HiCuM which separates the internal base resistance (depends on operating point) from the external component (independent of operating point). This node also takes into account the distributed nature of the external B-C region by splitting the external base-collector capacitance C_{BCx} over r_{Bx} . The emitter current crowding effect is modeled by the capacitance C_{rBi} . An emitter-base isolation capacitance C_{BEpar} as well as a base-collector oxide capacitance C_{BCpar} (included in the C_{BCx} element) is also taken into account. The addition of internal substrate node S* leads to the introduction of the substrate network with a capacitance C_{Su} and a resistance r_{Su} .

1.4.3 Temperature dependence in HiCuM

In the following discussion the temperature dependency of SiGe HBT in HiCuM compact model is described. The parameters of the compact model, corresponds to a reference temperature T_0 (e.g. 300 K) if it is not specified. During simulations, these parameters are then modified for each device according to its actual temperature T . As much as possible, the temperature dependence in HiCuM L2 is formulated in terms of the ratio T/T_0 . The corresponding equations are all based on the temperature dependence of physical quantities such as band-gap and mobility. Here only the temperature dependence of transfer current, junction current components and series resistances is specified.

1.4.3.1 Temperature dependent band-gap voltage

In order to allow simulations of devices fabricated in different materials and to make the model simulator independent, a temperature dependent band-gap voltage is included in HICUM according to

$$V_g(T) = V_g(0) + f_{2vg}T + f_{1vg}T \ln(T) \quad \text{Eq. 1-39}$$

The model parameter f_{1vg} and f_{2vg} , depend on the semiconductor material. Since the equations above is applied to all band-gap voltages available in the model, the model parameter $V_g(0)$ (zero-Kelvin band-gap voltage) needs to take into account average values for possible band-gap changes due to high-doping effects or material composition, making $V_g(0)$ an effective band-gap voltage. HICUM allows specifying an average effective band-gap voltage for each transistor region in order to provide the means for very accurate temperature modeling in integrated circuit

design. The respective model parameters are $V_{gE} = V_{gE}(0)$, $V_{gB} = V_{gB}(0)$, $V_{gC} = V_{gC}(0)$, $V_{gS} = V_{gS}(0)$.

1.4.3.2 Transfer current

The temperature dependent transfer current contains the temperature dependent model parameters c_{10} and Q_{p0} . The model equation for the prefactor c_{10} reads:

$$C_{10}(T) = C_{10} \left(\frac{T}{T_0} \right)^{\zeta_{CT}} \exp \left[\frac{V_{gB}}{V_T} \left(\frac{T}{T_0} - 1 \right) \right] \quad \text{Eq. 1-40}$$

with ζ_{CT} as model parameter.

The zero-bias hole charge Q_{p0} is only weakly temperature dependent via the influence of base width change with temperature that is mainly caused by the change in depletion width of the BE junction. Based on the temperature dependence of the zero-bias hole charge Q_{p0} can be accurately modeled by

$$Q_{p0}(T) = Q_{p0} \left[2 - \left(\frac{V_{DEi}(T)}{V_{DEi}} \right)^{z_{Ei}} \right] \quad \text{Eq. 1-41}$$

which requires no additional model parameters. The temperature modeling of $V_{DEi}(T)$ ensures that $Q_{p0}(T)$ will always remain positive without any additional smoothing effort.

1.4.3.3 Junction current components

The temperature dependent saturation current of the BE backinjection component is given by,

$$I_{BEiS}(T) = I_{BEiS} \left(\frac{T}{T_0} \right)^{\zeta_{BET}} \exp \left[\frac{V_{gE}}{V_T} \left(\frac{T}{T_0} - 1 \right) \right] \quad \text{Eq. 1-42}$$

with the model parameter ζ_{BET} and the effective emitter bandgap voltage V_{gE} . An estimate for V_{gE} can be calculated from the effective bandgap voltage in the base and the measured relative temperature coefficient (TC) α_{Bf} of the current gain:

$$V_{gE} = V_{gB} - \alpha_{Bf} \cdot T_0 \cdot V_{T0} \quad \text{Eq. 1-43}$$

The BE recombination component is given by,

$$I_{REiS}(T) = I_{REiS} \left(\frac{T}{T_0} \right)^{\zeta_{REi}} \exp \left[\frac{V_{gBE}}{2 \cdot V_T} \left(\frac{T}{T_0} - 1 \right) \right] \quad \text{Eq. 1-44}$$

with $\zeta_{REi} = m_g / 2$ and $m_g = 3 - f_{1vg} q/k_B$ as well as the average bandgap voltage V_{gBE} defined by:

$$V_{gBE} = \frac{V_{gB} + V_{gE}}{2} \quad \text{Eq. 1-45}$$

All other junction related saturation currents are also described by formulations similar to Eq. 1-42 or Eq. 1-44 but with the parameter listed in TABLE 1-II.

TABLE 1-II

*Junction saturation current components and the parameters for temperature dependence modeling.
'Equation' indicates the formulation employed.[24]*

Component	Equation	Bandgap V_{geff}	Factor ζ
I_{BEiS}	Eq. 1-42	V_{gE}	ζ_{BET}
I_{BEpS}	Eq. 1-42	V_{gE}	ζ_{BET}
I_{REiS}	Eq. 1-46	V_{gBE}	$\zeta_{REi} = m_g / 2$
I_{REpS}	Eq. 1-46	V_{gBE}	$\zeta_{REp} = m_g / 2$
I_{BCiS}	Eq. 1-42	V_{gC}	$\zeta_{BCi} = m_g + 1 - \zeta_{Ci}$
I_{BCxS}	Eq. 1-42	V_{gC}	$\zeta_{BCxT} = m_g + 1 - \zeta_{Cx}$
I_{SCS}	Eq. 1-42	V_{gS}	$\zeta_{SCT} = m_g + 1 - \zeta_{\mu pS}$

1.4.3.4 Series resistance

The temperature dependence of all series resistances is in general determined by the mobility as well as contact or interface recombination velocity of the respective regions. The zero-bias internal base resistance reads:

$$r_{Bi0}(T) = r_{Bi0} \left(\frac{T}{T_0} \right)^{\zeta_{rBi}} \quad \text{Eq. 1-46}$$

The model parameter ζ_{rBi} accounts for the (average) base doping concentration. Conductivity modulation and emitter current crowding in R_{Bi} are automatically described as a function of T by the corresponding charges and currents.

The external base resistance R_{Bx} , external collector resistance R_{Cx} , and emitter series resistance R_E follow the formulation (Eq. 1-46) with corresponding model parameters ζ_{rBx} , ζ_{rCx} , and ζ_{rE} that includes the effect of both (average) doping concentrations within the corresponding regions and contact or interface recombination velocity.

1.4.4 Self-heating in HiCuM

The increase of the transistor's "junction" temperature T_j caused by self-heating is calculated using a thermal network as shown in *Figure 1-8(b)*. The current source corresponds to the power dissipated in the device, and the node voltage corresponds to the junction temperature. The calculation requires the thermal resistance, R_{TH} , and thermal capacitance, C_{TH} , (of the particular transistor) as model parameters. The thermal network is solved together with each transistor model (provided $R_{TH} > 0$ and $FLSH$ (model parameter used as a flag for self-heating calculation) $\neq 0$) for DC and transient operation. The node voltage is passed on to the model routine in order to calculate the temperature dependent model parameters. The power dissipation is generally caused by all dissipative elements in the equivalent circuit (i.e. excluding any energy storage elements). Only the most relevant dissipative elements are included in the power calculation for $FLSH = 1$:

$$P = I_T V_{C'E'} + I_{AVL} (V_{DCi} - V_{B'C'}) \quad \text{Eq. 1-47}$$

The purpose of this measure is to reduce the computational effort without sacrificing convergence.

1.4.5 Compact modeling

Transistor models for BiCMOS9MW technology were generated by a scalable HiCuM library [25] provided by XMOD Technologies. The static and dynamic characteristics for a

device of drawn L_E 5 μm and W_E 0.27 μm with CBE configuration are presented. It is shown that, the transistor library accurately models the DC and AC behavior of the device.

1.4.5.1 Gummel plot

Static measurement is performed at $V_{BC} = 0\text{V}$ and varying V_{BE} from 0.4V to 0.98V which contains both the low and high injection regions. The modeling results are presented below which represent modeling of forward Gummel plot and current gain (β). Both these are modeled properly as shown in the *Figure 1-9* and *Figure 1-10*.

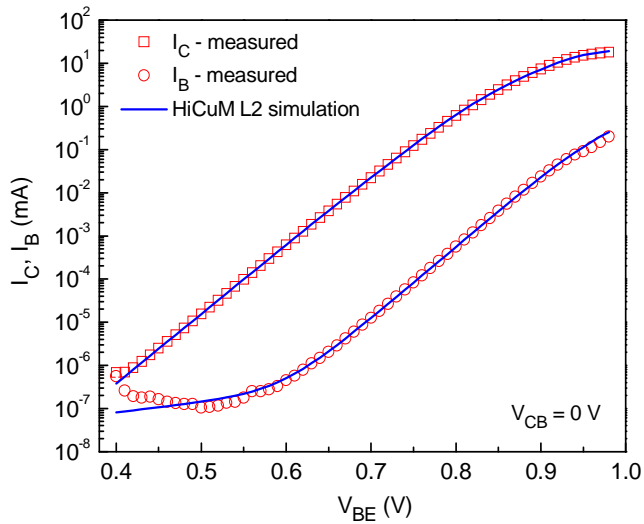


Figure 1-9: Forward Gummel plot: I_C and I_B as a function of V_{BE} (at $V_{CE} = 0\text{V}$) – comparison between measurements and HiCuM L2 simulation.

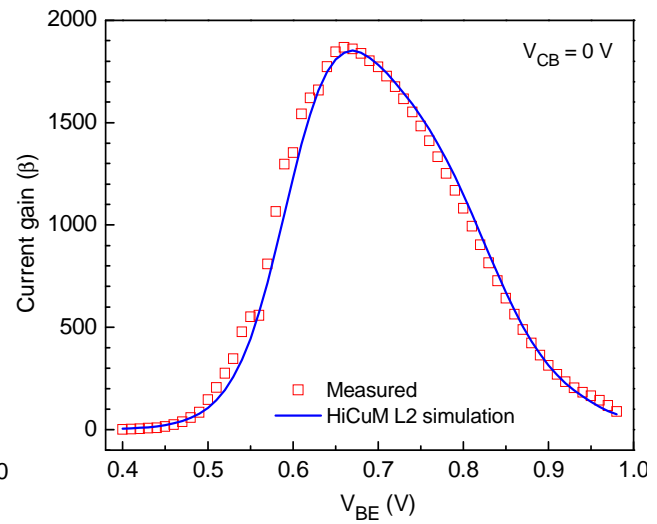


Figure 1-10: Current gain β vs V_{BE} (at $V_{CE} = 0\text{V}$) – comparison between measurements and HiCuM L2 simulation.

1.4.5.2 Output characteristic

The output characteristics are presented as follows: (i) I_C as a function of V_{CE} at constant V_{BE} in *Figure 1-11*, (ii) I_B as a function of V_{CE} at constant V_{BE} in *Figure 1-12*, (iii) I_C as a function of V_{CE} at constant I_B in *Figure 1-13* and (iv) V_{BE} as a function of V_{CE} at constant I_B in *Figure 1-14*. The maximum base emitter voltage is chosen beyond peak f_T at high current region. Base collector breakdown is not reached in the measurement. The figures show a good agreement between measurements and compact model.

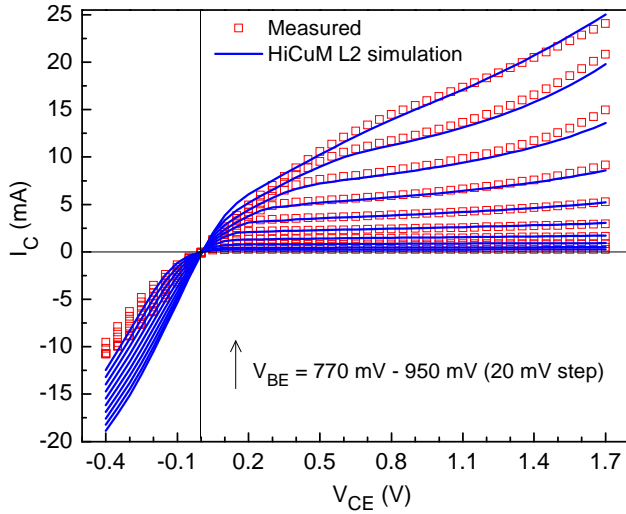


Figure 1-11: I_C as a function of V_{CE} for different V_{BE} – comparison between measurements and HiCuM L2 simulation.

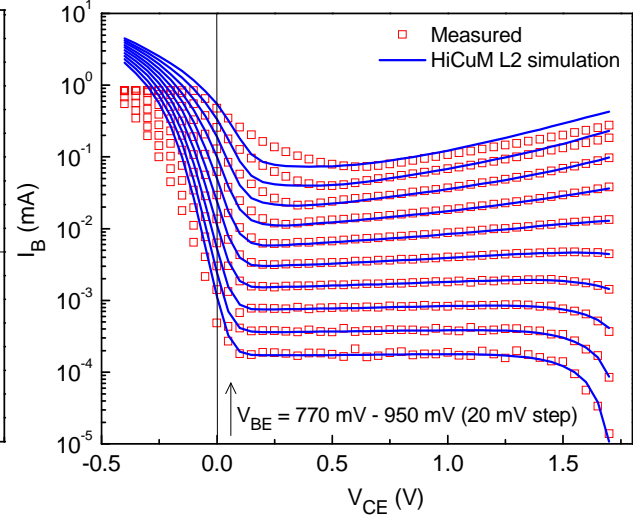


Figure 1-12: I_B as a function of V_{CE} for different V_{BE} – comparison between measurements and HiCuM L2 simulation.

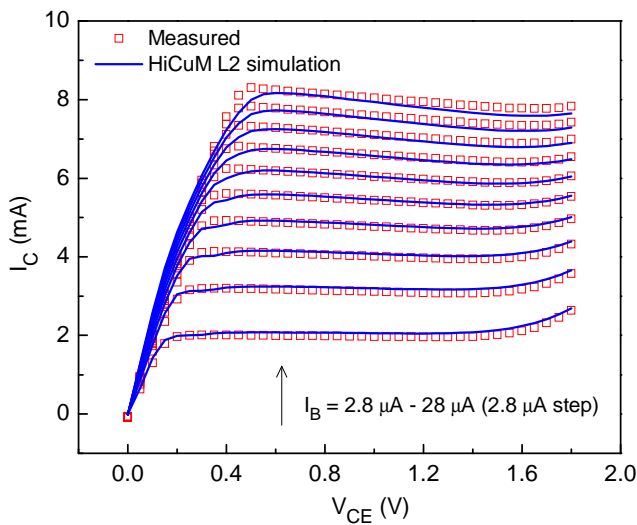


Figure 1-13: I_C as a function of V_{CE} for different I_B – comparison between measurements and HiCuM L2 simulation.

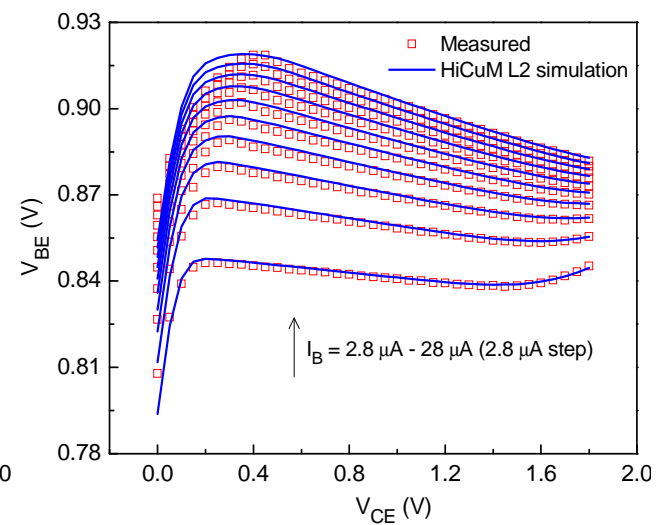


Figure 1-14: V_{BE} as a function of V_{CE} for different I_B – comparison between measurements and HiCuM L2 simulation.

1.4.5.3 Dynamic characteristics

The cut off frequency f_T as a function of V_{BE} and I_C is shown in *Figure 1-15* and *Figure 1-16* respectively. The f_T is calculated at 15 GHz where the magnitude of small signal current gain shows a perfect 20dB/dec slope. Modeling results show a fairly well accuracy as both the transit time and critical current is well modeled.

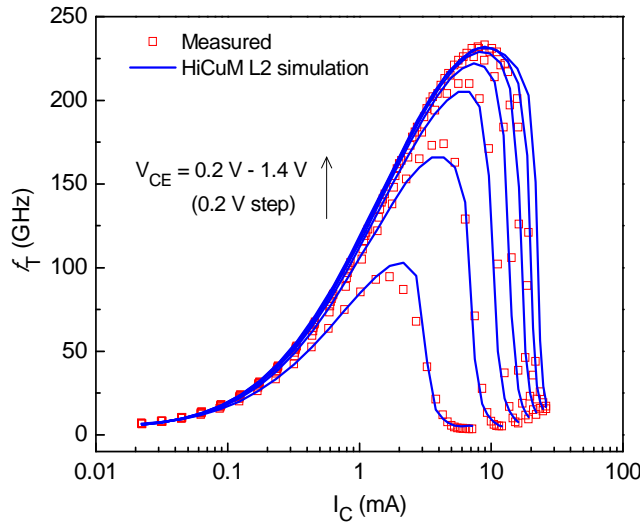


Figure 1-15: f_T as a function of I_C for different V_{CE} – comparison between measurements and HiCuM L2 simulation.

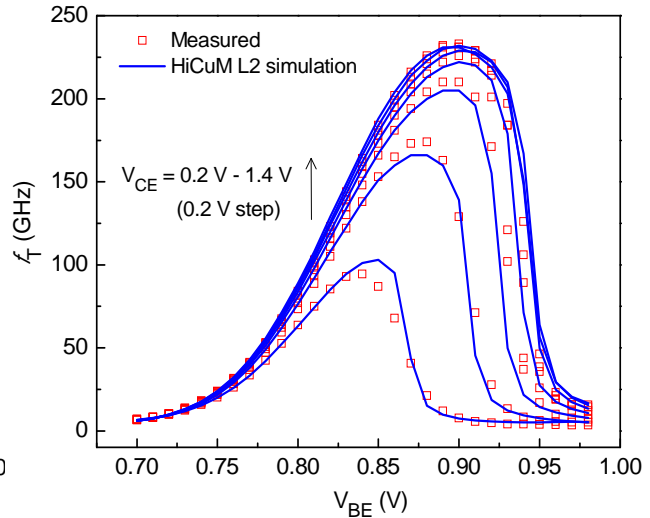


Figure 1-16: f_T as a function of V_{BE} for different V_{CE} – comparison between measurements and HiCuM L2 simulation.

1.5 Conclusions

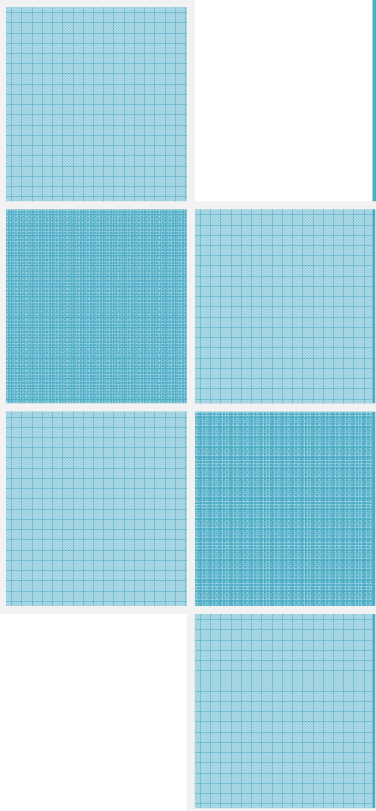
This chapter demonstrates a general overview of self-heating effect in electronic device. The Different analytical models, presented in literature, and the corresponding representation through electro-thermal networks have been described. A generalized equation for frequency domain thermal impedance of two port device has been formulated, which can be used to extract device thermal impedance in the frequency range below thermal cut-off frequency. A brief description on HBT compact model and the temperature effects in modeling have been described. HiCuM L2 compact model has been verified by forward Gummel, output and dynamic characteristics. A good agreement has been obtained. The extracted parameter library has been used in further electro-thermal investigation which will be described in next chapters.

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Characterization of SiGe:C BiCMOS HBTs

This chapter provides an extensive evaluation of self-heating in microwave SiGe:C BiCMOS HBTs through DC, pulse and low frequency s-parameter measurements. Different methodologies have been applied in order to evaluate steady state, transient and dynamic thermal behavior of the device. Thermal parameters are extracted with HiCuM L2 simulations using different electro-thermal networks at temperature node.



2.1 Introduction

The characterization and modeling of self-heating in bipolar devices remains a major research issue associated with the advancement of Heterojunction Bipolar Transistors (HBTs) technology. This characterization is mostly based on steady state condition to extract thermal resistance (R_{TH}) and transient condition to extract thermal capacitance (C_{TH}). Several researches have been performed to investigate R_{TH} and C_{TH} which are based on analytical models [1–3], numerical simulations [4–7], DC, AC and pulse measurements. In [8–15], DC measurements are carried out at different base-plate temperatures in order to extract R_{TH} considering the temperature dependence of common-emitter current gain (β) as a thermometer. Another simplified method has been proposed in [16], measuring temperature dependent standard output characteristics (I_C-V_{CE}) at constant base current (I_B). There are several pulse measurement techniques presented in [17–19] based on the assumption of isothermal operation during the short pulse. The transient temperature response can be obtained by pulses applied to the collector node and keeping the I_B constant. Measuring base-emitter voltage (V_{BE}) permits to determine the change in temperature inside the device. In order to extract accurate C_{TH} , there are major difficulties since time domain collector current (I_C) measurements are very sensitive to parasitics e.g. inductance and capacitance of coaxial cables. These lumped elements must be calibrated for an accurate characterization.

This chapter presents an extensive evaluation of self-heating in microwave HBTs. In particular, DC measurements, pulse measurements and low frequency s-parameter measurements have been carried out in order to investigate the steady, transient and dynamic thermal behavior of a submicron SiGe:C BiCMOS technology with f_T and f_{max} of 230 GHz and 290 GHz, respectively. The chapter is organized into nine different sections. The first section deals with the DC measurements at different ambient temperature. R_{TH} s of different geometry of transistors are extracted using the methodology described in [20]. In second section, pulsed output and gummel characteristic are discussed. These measurements are performed with KEITHLEY 4200 equipment. The third section focuses on a new methodology for accurate C_{TH} determination through time domain measurements. The transient variation of collector current caused by self-heating is obtained through pulse measurements which are performed with MC2 technology APMS pulse generators. Pulse measurements are described in detail including methodology,

optimization and characterization of lumped elements. Thermal modeling is performed through HiCuM L2 [21–24] simulations which have been discussed in section five. Thermal parameters have been extracted by means of compact model simulation using a scalable transistor library (chapter 1). For thermal characterization, different electro-thermal networks have been verified by connecting at the temperature node of HiCuM L2. It has been shown that, the conventional single pole thermal network is not sufficient to accurately model the transient thermal spreading behavior and therefore a distributed type network needs to be used. In section six, a new and simplified methodology for isothermal data extraction from static characteristics (measured at different ambient temperatures) is presented. Also, the extracted isothermal data has been verified by pulse measurements. Low frequency s -parameter measurements are discussed in seventh section in order to characterize the dynamic self-heating (described in section eight). The thermal impedance (Z_{TH}) has been extracted in the frequency range below thermal time constant (section nine). Different methodology has been described in order to extract Z_{TH} from y -parameters. Thermal modeling is performed using different electro-thermal networks. It has been manifested that the recursive electro-thermal network provides the best conciliation in terms of accuracy, number of model parameters and physical point of view. Compact model simulations are verified in time and frequency domain and found to be in very good agreement for various device geometries.

2.2 DC Measurements

The measurements are carried out under static conditions applying DC voltages and/or currents. The semiconductor parameter analyzer HP4155 can perform as a voltage or current generator that apply and measure voltages and currents directly on the transistor. In *Figure 2-1* SMU1 and SMU2 are two sources of voltages / current of HP4155 which is connected to base and collector terminal of the device respectively. The whole system is configured with ICCAP which can control the parameter analyzer through GPIB. A temperature regulator is used for the wafer that can hold the device at controlled temperature.

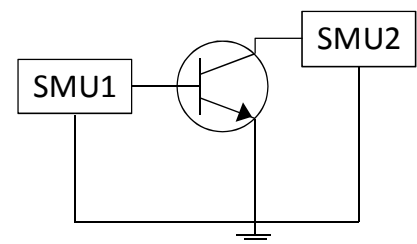


Figure 2-1: Experimental setup for DC measurements: HP4155 SMUs (source monitor unit) are the voltage / current sources.

2.2.1 Extraction methodology

The determination of R_{TH} is mostly based on the characterization at steady state conditions. In this work, the DC measurements are performed at different wafer / base-plate temperatures (T_B) between 300K and 335K. The R_{TH} s of several geometries of transistor are determined using the method described in [20]. This extraction procedure requires:

- i. Temperature dependent standard $I_C - V_{CE}$ measurements at constant I_B .
- ii. Only a few values of T_B
- iii. The effects of both T_B and power dissipation (P_{diss}) are taken into account

2.2.1.1 Gummel characteristic

The Gummel characteristic is used to measure simultaneously I_C and I_B according to the V_{BE} at constant V_{CE} . In *Figure 2-2(a)*, the Gummel plot for the transistor with drawn emitter length (L_E) 10 μm and emitter width (W_E) 0.27 μm is shown, where the collector – emitter (V_{CE}) is 1V. The corresponding common emitter current gain (β) is shown in *Figure 2-2(b)*. We consider two I_B (1.42 and 6.85 μA) in the region of V_{BE} where I_C and I_B curves are parallel indicating an almost constant current gain. These I_B s are taken into account for the output characteristics measurement at different T_B .

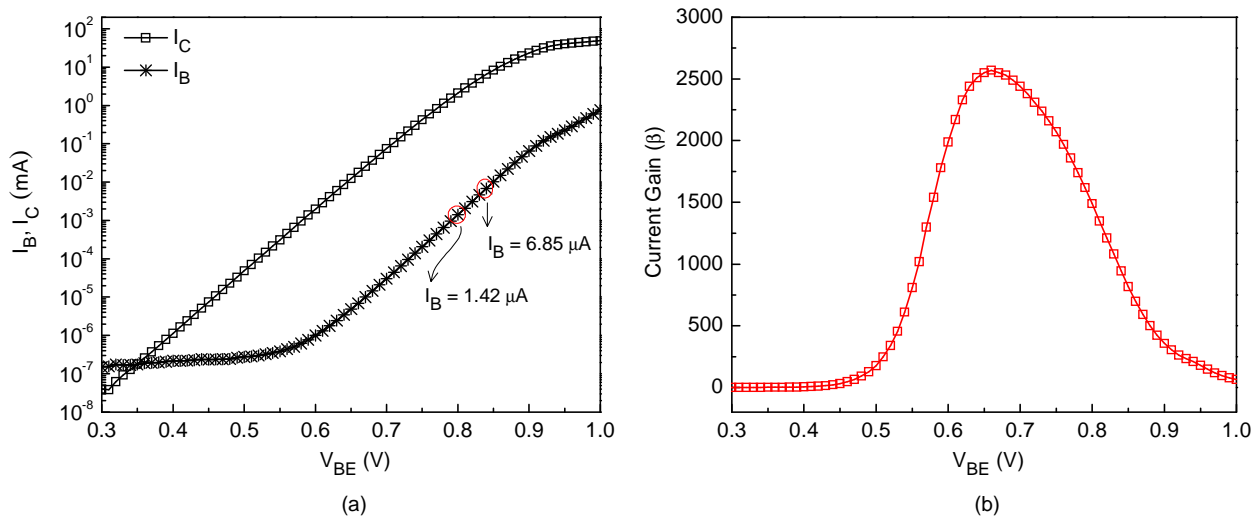


Figure 2-2: (a) Gummel plot (I_C and I_B vs. V_{BE}) at $V_{CE} = 1$ V, (b) Corresponding common emitter current gain β . $\{L_E \times W_E = 10 \times 0.27 \mu m^2\}$

2.2.1.2 Output characteristics at constant I_B

The output characteristics are measured at different temperature environment. In these measurements SMU1 is a current generator which sends the constant I_B and SMU2 is the voltage generator that provides V_{CE} of 0 to 1 V. The I_B s are selected from previous Gummel measurements. Figure 2-3 shows I_C and V_{BE} as a function of V_{CE} at I_B 1.42 μ A. These characteristics are measured at different T_B varying from 300K to 335K.

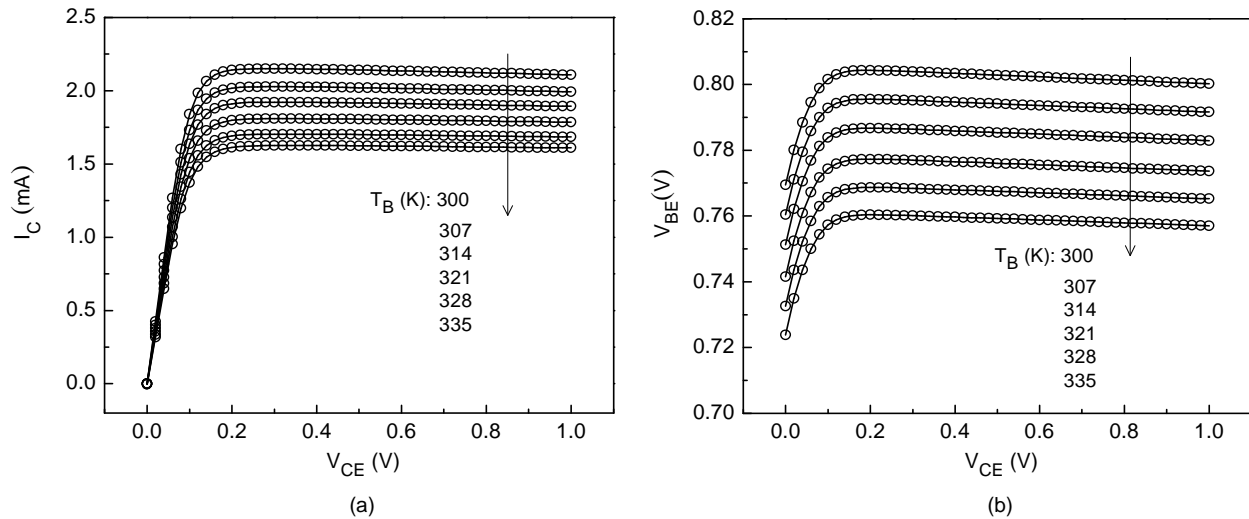


Figure 2-3: Output characteristics (a) I_C as a function of V_{CE} at $I_B = 1.42 \mu\text{A}$, (b) V_{BE} as a function of V_{CE} at $I_B = 1.42 \mu\text{A}$. $\{L_E \times W_E = 10 \times 0.27 \mu\text{m}^2\}$

2.2.1.3 V_{BE} as a function of ambient temperature

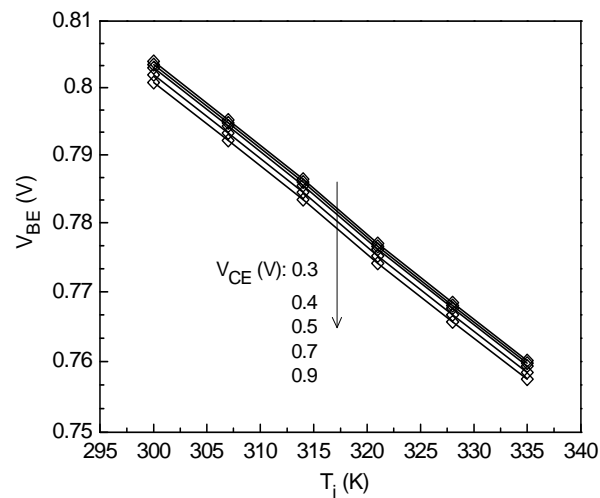


Figure 2-4: Base – emitter voltage V_{BE} as a function of ambient temperature T_i for different collector – emitter voltage V_{CE} . $\{L_E \times W_E = 10 \times 0.27 \mu\text{m}^2\}$

The ambient temperature (T_i) is same as wafer temperature (T_B). For a constant I_B , V_{BE} decreases when the V_{CE} increases. The previous output characteristics [I_C and $V_{BE} = f(V_{CE})$] allows to trace V_{BE} at different T_i . *Figure 2-4* is the calibration curve which shows a linear relationship between V_{BE} and T_i .

2.2.1.4 R_{TH} calculation

The thermal resistance of the medium can be written as,

$$R_{TH} = \frac{T_j - T_i}{P_{diss}} \quad \text{Eq. 2-1}$$

where, T_j is the temperature of base – emitter junction and P_{diss} the power dissipation. Therefore, the junction temperature T_j is given by,

$$T_j = R_{TH} P_{diss} + T_i \quad \text{Eq. 2-2}$$

From all previous curves (*Figure 2-2* to *Figure 2-4*), we can extract the terms V_{CE} , T_i and I_C for a same V_{BE} , even same I_B . Thus, the power dissipation P_{diss} for each T_i could be calculated.

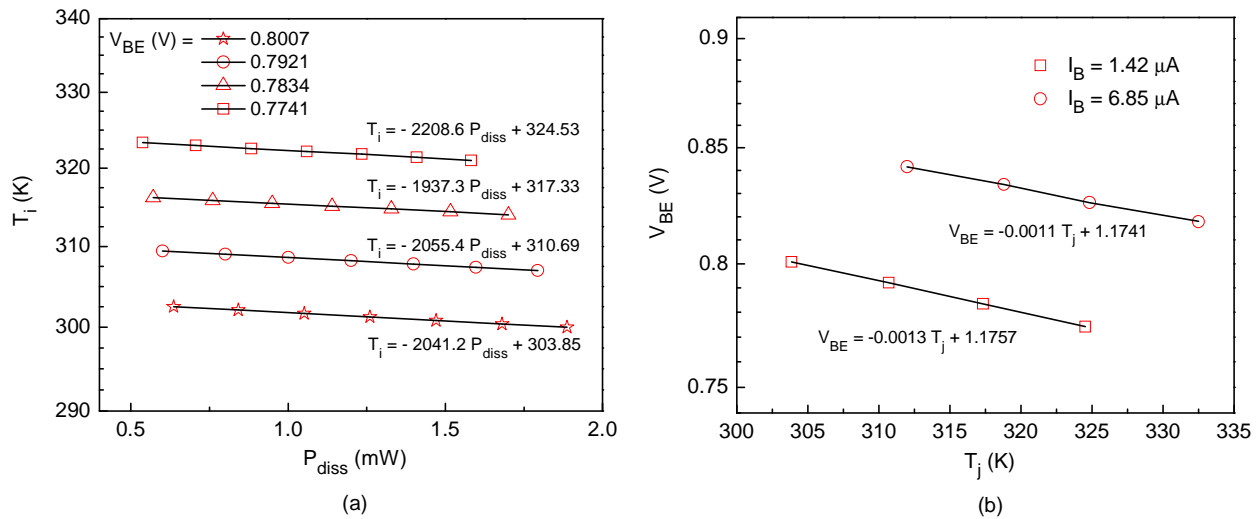


Figure 2-5: (a) T_i as a function of P_{diss} at $I_B = 1.42 \mu A$, (b) V_{BE} as a function of T_j at $I_B = 1.42 \mu A$ and 6.85. $\{L_E \times W_E = 10 \times 0.27 \mu m^2\}$

The *Eq. 2-1* and *Eq. 2-2* allow us to obtain the R_{TH} and the T_j when one stretches the “ $T_i = f(P_{diss})$ ” curve to “ $P_{diss} = 0$ ”. The important aspect of this method is to evaluate the temperature of base – emitter junction for a given bias point. *Figure 2-5* shows a linear relationship between V_{BE} and T_j .

2.2.2 R_{TH} vs. device geometry

The DC measurements are performed for different geometries of transistor. The R_{TH} s are extracted from several bias points and finally an average value has been calculated in order to obtain a better accuracy. In *Figure 2-6*, the decreasing nature of R_{TH} with the dimension of emitter area is shown. Note that for a constant emitter area, a small emitter width is preferable to reduce the R_{TH} .

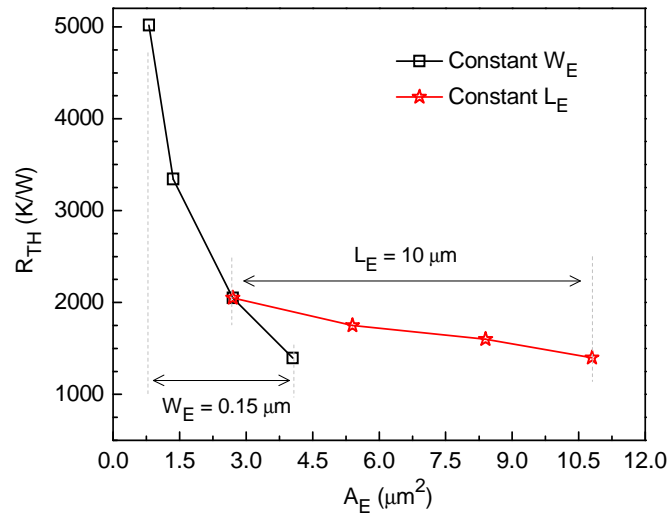


Figure 2-6: R_{TH} s for different geometries of transistor: extracted from DC measurements at different T_B .

2.3 Pulse measurements

Pulsed output and Gummel characteristics are measured with pulsed DC analyzer Keithley 4200-SCS. A brief description of the experimental setup is given below.

2.3.1 Experimental setup: KEITHLEY 4200SCS

A simplified block diagram of the experimental setup (KEITHLEY 4200SCS PIVA [25]) is given in *Figure 2-7*. Here, the 4200PIVA module (40 ns to 150 ns pulse width range) has been replaced by the 4225 module (pulse width 80 ns to DC) in order to have more flexibility in duty cycle and pulse width conditions. The Model 4225-PMU provides broad ranges of voltage sourcing, current measurement, and timing parameters [26]. The 4200-SCS consists of two pulse measurement units (PMUs) that generate the pulse and measure the pulse response. The PMU allows generating pulses larger than 100 ns with minimum rise and fall time of 20 ns. Accurate measurements are obtained in a time window between 60% and 90% of the DC pulse duration.

The pulses are applied directly to the base port of the transistor, while the collector port is biased at a certain voltage and the emitter is connected to ground. The I_C is measured at 50 Ω resistance. The change in I_C , resulting from the base pulse, appears on the digital oscilloscope.

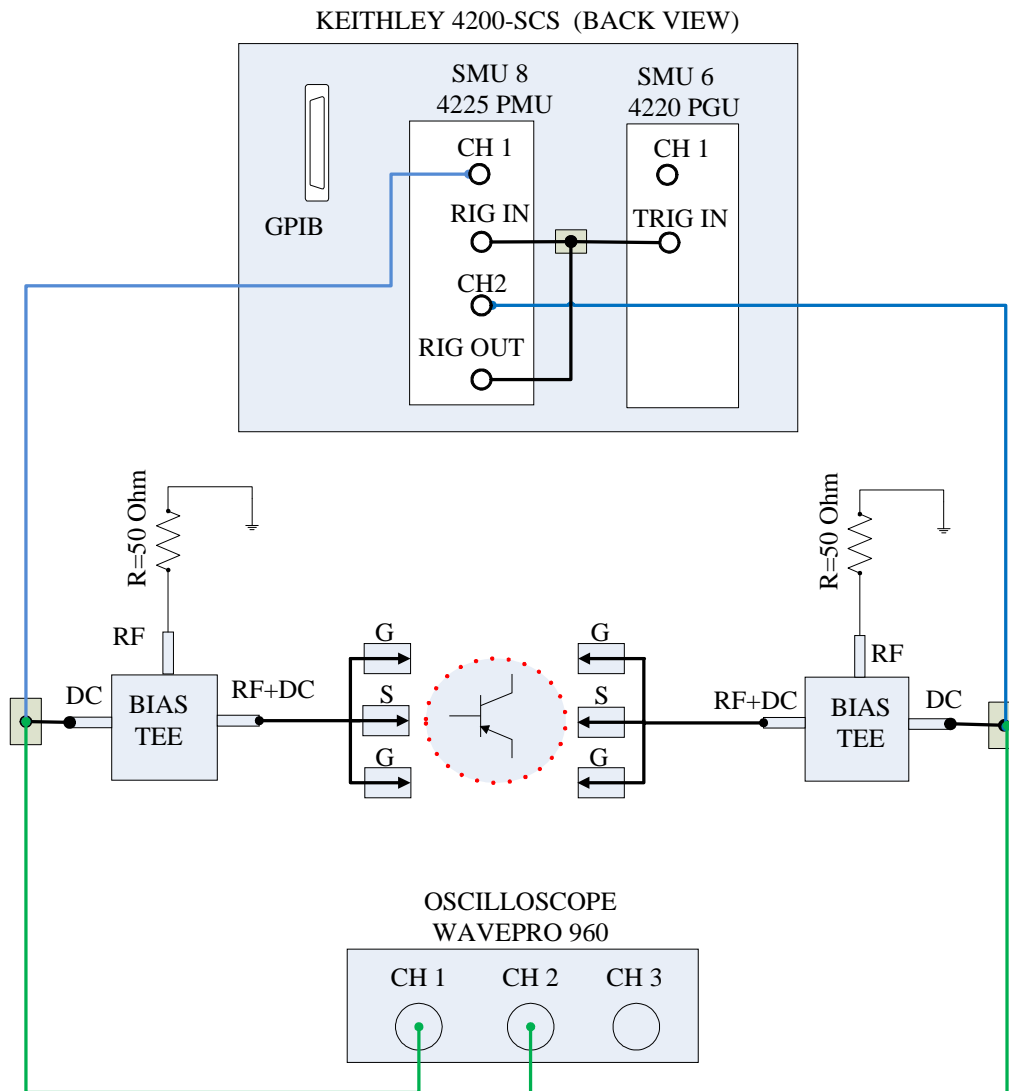


Figure 2-7: Block diagram of KEITHLEY 4200SCS pulse measurements system; the 4200PIVA module has been replaced by the 4225 module.

2.3.2 Pulsed output and Gummel characteristic

Figure 2-8 and Figure 2-9 show measured pulsed output and forward Gummel characteristics respectively for an HBT with a drawn emitter length $L_E = 5 \mu\text{m}$ and width $W_E = 0.27 \mu\text{m}$. Measurements were carried out with 4225 PMU as shown in (b) using pulse widths

from 150 ns up to 1 μ s. Increasing in I_C with pulse width and a good agreement between long pulse width and standard DC characteristics verify the accuracy of the system.

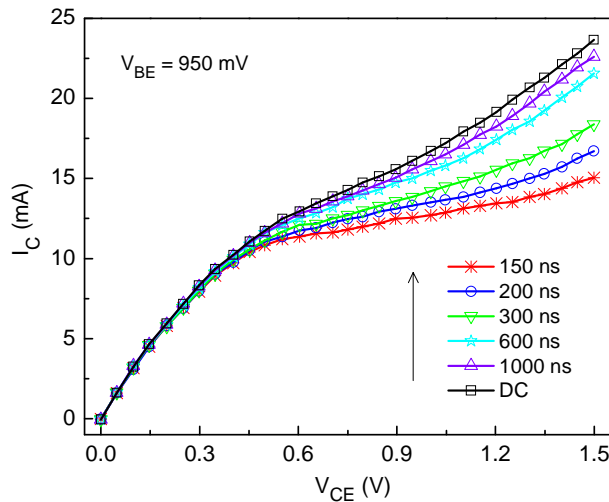


Figure 2-8: Output characteristics measured (with Keithley 4225 PMU) at various pulse width (150 to 1000 ns) and DC condition; measured with 4225 module.

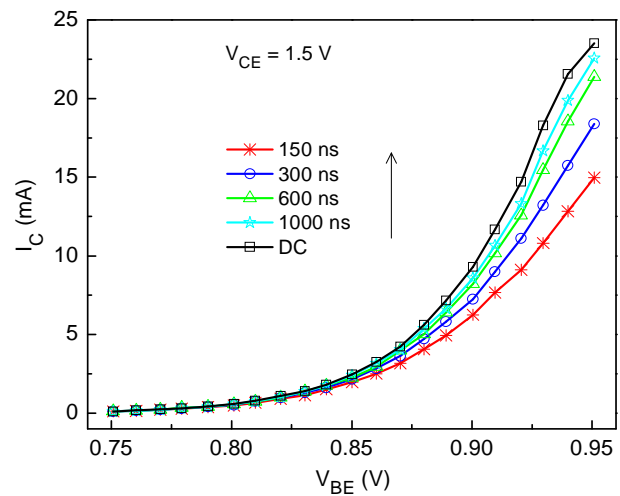


Figure 2-9: Forward Gummel characteristics measured (with Keithley 4225 PMU) at various pulse width (150 to 1000 ns) and DC condition; measured with 4225 module.

2.4 Time domain characterization

This section presents an extensive evaluation of a new technique for self-heating effect characterization through an accurate time domain I_C measurements. The measurements have been carried out over pulses applied at base and collector terminals simultaneously which show how transient self-heating affects the time response of collector current variation. A complete calibration has been performed in device compact model simulations in order to extract accurate thermal parameters for different geometry of transistors.

2.4.1 Experimental setup: MC2 Technology APMS

The pulse measurement scheme is based on the transient measurements of I_C . The device under analysis is connected to the various pulse sources and the monitoring equipment. A schematic diagram of the experimental setup is given in *Figure 2-10*. These measurements have been carried out on wafer with GSG (Ground – Signal – Ground) probe configuration at room temperature (300 K).

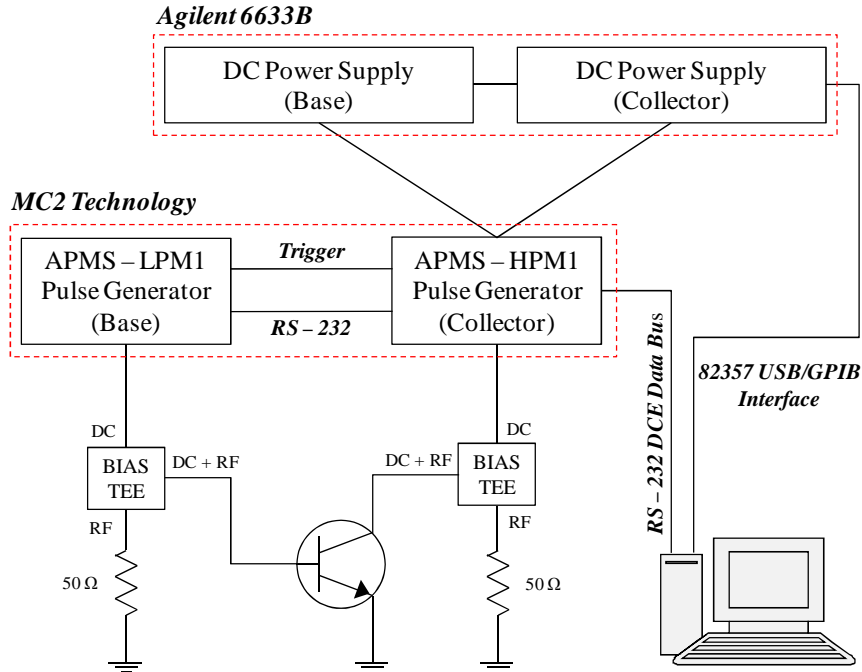


Figure 2-10: Experimental setup for pulse measurements: base and collector pulse generators (MC2 Technology APMS LPM1/HPM1) apply pulses through the bias TEE. System DC power supply (Agilent 6633B) is used to set quiescent and bias points.

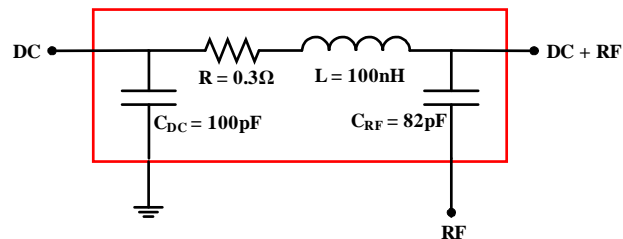


Figure 2-11: Bias TEE - Agilent Bias Network 11612A OPT OO1 - 400 MHz to 26.5 GHz and 100 V DC - 2.0 Amp Max.

Base and Collector pulse are generated by MC2 Technology APMS LPM1 and HPM1 pulse generators [27] respectively. The Agilent 6633B system DC power supply (SMU Base and Collector) are used to set the quiescent and bias points for both Base and Collector terminals. The pulses are applied to the device terminals through the bias TEE (Agilent Bias Network 11612A OPT OO1 - 400 MHz to 26.5 GHz and 100 V DC - 2.0 A Max) [28] as given in Figure 2-11. The information for the measurements is sent through the 82357 GPIB-USB interfaces and

the measured data is collected by RS-232 DCE data bus. All equipments are controlled from the PC. The experimental setup has been calibrated accurately before measurements.

2.4.2 Overview of the approach

The measurements have been carried out over pulses applied at base and collector terminals simultaneously and the time responses of collector current increase due to self-heating effect are obtained.

A simplified block diagram of the experimental set up is shown in *Figure 2-12*. P_{Base} and $P_{Collector}$ represent the pulse source for base and collector terminals respectively. Base and collector (V_{BE} and V_{CE}) pulses are applied through the DC port of the bias network. The RF port is grounded through 50 ohm resistance. Before switching on the pulse source, the device is set with the quiescent bias point. A duty-cycle of less than 5% is applied in order to maintain the device temperature. The measurement procedure consists of switching the device from a state of negligible power dissipation to the high power dissipation through fast rise / fall time (10 ns). For a very fast pulse, there is insufficient time for the temperature to change over the duration of rise time since the electrical device response is much faster. The collector current transient $I_C(t)$ variation contains information of device self-heating as the device temperature approaches its steady state value.

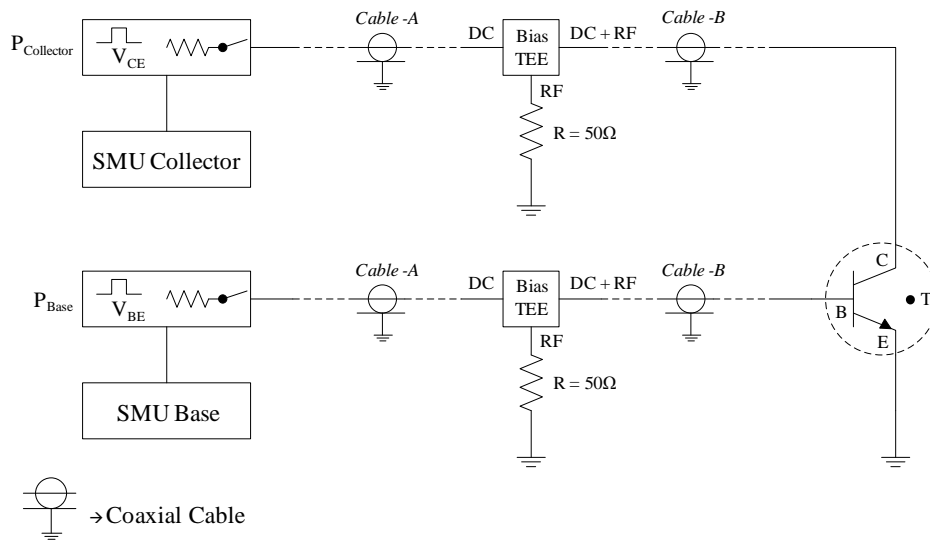


Figure 2-12: Simplified block diagram for pulse measurement setup: V_{CE} and V_{BE} pulses are applied through the DC port of the bias TEEs and RF ports are grounded through 50 Ω resistances.

2.4.3 Optimizations

Pulse measurements show often collector current overshoot when applying the pulse and this is due to the passive elements that arise from the coaxial cables, connectors and bias network. Therefore, it is necessary to optimize these elements to minimize the parasitic effect. The optimization of the parameters of the lumped elements is performed by comparing the measurements to simulation. Compact model simulations need to be performed including all the parasitics. Therefore, all the elements are connected in series to form a network as given in *Figure 2-13*. The network is symmetrical for both base and collector side.

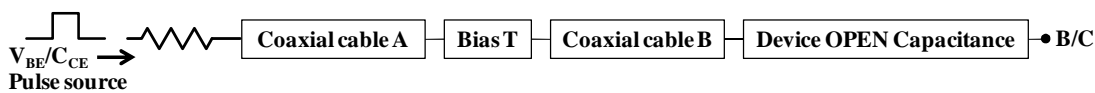


Figure 2-13: The lumped elements between pulse generator and device terminals – connected in series forming a complete parasitic network.

The internal resistance of the pulse generator is given in APMS LPM1/HPM1 pulse generator user manual. The internal network and the values of the network elements are taken from bias network manual. It has been seen through measurements that the capacitance (C_{Cable}) and inductance (L_{Cable}) of cables are most dependable for the noise arising in base and collector current pulse profiles. There, it would be necessary to know C_{Cable} and L_{Cable} for circuit simulation with compact model and, therefore, optimizations of parasitic elements.

2.4.3.1 Measurement of coaxial cable impedance

The passive elements of the coaxial cables and connectors are measured by an auto-balancing bridge type Impedance analyzer HP4194A and the 16047E test fixture. *Figure 2-14* shows the schematic diagram of experimental setup. The high terminal of the test fixture is connected to the outer conductor of the cable. The characteristic impedance is determined by measuring the impedance of the cable with its other end opened and shorted (Open-Short method). Open measurement gives capacitance and short measurement gives resistance and inductance of the cable. The characteristic impedance is given by following equation:

$$|Z|_{Cable} = \sqrt{|Z|_{OPEN} * |Z|_{SHORT}}$$

$$\theta_{Cable} = \frac{\theta_{OPEN} + \theta_{SHORT}}{2}$$
Eq. 2-3

$|Z|_{Open}$ and θ_{Open} are the Magnitude (Ω) and the phase (deg) of measured impedance when the cable end is opened. $|Z|_{Short}$ and θ_{Short} are the same when the cable end is shorted.

In *Figure 2-15* and *Figure 2-16*, the magnitude and phase of cable impedance is shown when its final end is opened and shorted. The resistance (R_{cable}), inductance (L_{cable}) and capacitance (C_{cable}) of the cable are given by the following equations:

$$|Z|_{OPEN} = \frac{1}{2\pi f C_{Cable}}$$

$$|Z|_{SHORT} = \sqrt{R_{Cable}^2 + 4\pi^2 f^2 L_{Cable}^2}$$
Eq. 2-4

where f is the characteristic frequency. As, $f \rightarrow 0$, $|Z|_{SHORT} \rightarrow R_{Cable}$.

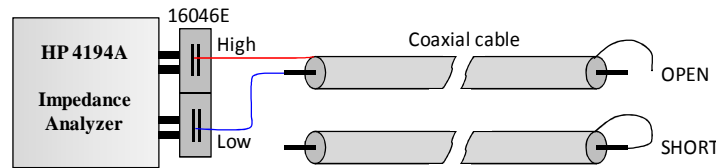


Figure 2-14: Experimental setup (HP4194A impedance analyzer with 16046E test fixture) for Coaxial cables characteristic impedance measurements.

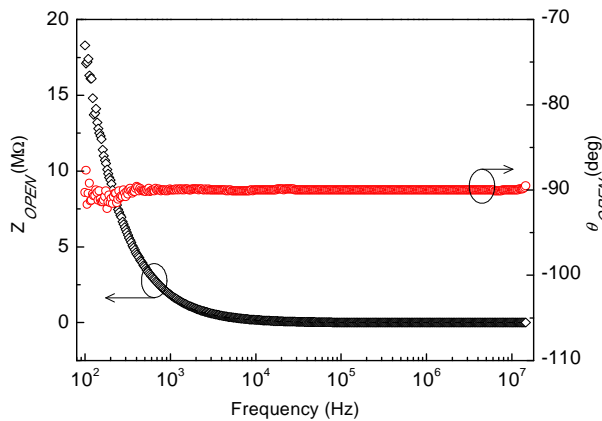


Figure 2-15: Open measurements (cable length = 100 cm) - magnitude and phase of Open impedance.

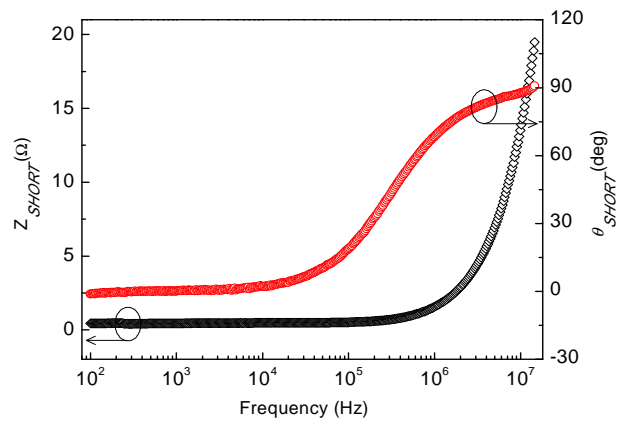


Figure 2-16: Short measurements (cable length = 100 cm) - magnitude and phase of Short impedance.

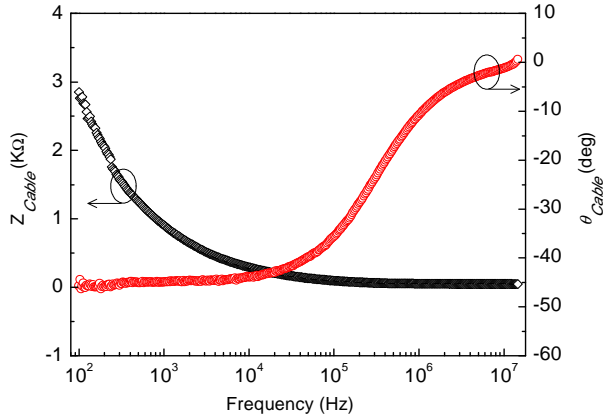


Figure 2-17: Magnitude and phase of cable impedance (length = 100 cm).

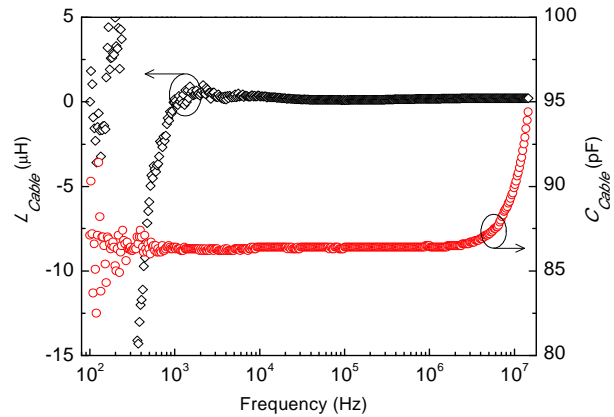


Figure 2-18: L_{cable} and C_{cable} – extracted from short and open impedance respectively.

The cable characteristic impedance $|Z|_{Cable}$ and the corresponding R_{cable} , L_{cable} and C_{cable} have been extracted by Eq. 2-3 and Eq. 2-4 as shown in Figure 2-17 and Figure 2-18 respectively. In table TABLE 2-I, R_{cable} , L_{cable} and C_{cable} are shown for three different lengths. It is noticed that, the values of capacitance and inductance increase considerably with cable length. Therefore, it would be necessary to optimize the cable length in order to minimize noise.

TABLE 2-I:

Measured R_{cable} , L_{cable} , C_{cable} and $|Z|_{Cable}$ for different lengths (~ 20, 40 and 100 cm) of coaxial cables.

Cable length (cm)	R_{cable} (Ω)	L_{cable} (nH)	C_{cable} (pF)	$ Z _{Cable} = \text{Sqrt}(L_{cable} / C_{cable})$ (Ω)
~ 20	0.3	30	15	44.72
~ 40	0.4	100	44	47.67
~ 100	0.7	250	95	51.29

2.4.3.2 “Passive circuit” design

A complete circuit is designed taking into account all the lumped elements between pulse generator and device terminals and connecting them in series (according to Figure 2-13). We could call it as a “passive circuit”. The values of each element (resistance, capacitance and inductances) are given in Figure 2-19. We have tried to use the smaller length (~20 cm) between pulse generator and bias TEE (cable – A). But, depending on the distance between measurement probe configuration and pulse generator, it is difficult to reduce the cable lengths. Therefore,

circuit simulations are performed with device compact model and “passive circuit” for different lengths of cable – B to know how the cable length is responsible for parasitic overshoot current.

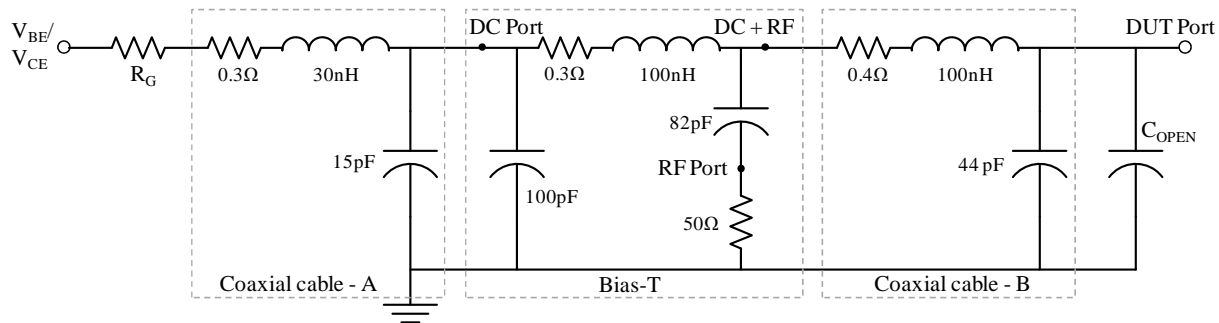


Figure 2-19: Complete passive network including coaxial cables, bias-TEE, device open capacitance ($C_{OPEN} = 21 \text{ fF}$ for both Base-Collector terminals for the device geometry $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$) and internal resistance of pulse generator (60Ω for base pulse generator and 1.5Ω for collector pulse generator). The values of the passive elements for coaxial cables are measured and optimized through simulation.

2.4.3.3 Compact model simulation with “passive circuit”

The optimizations are performed with HiCuM L2 simulations including the “passive circuit” in two ways: (i) using different cable lengths, and (ii) different pulse width configurations. A schematic diagram of the simulation setup is shown in Figure 2-20. At temperature node of the HiCuM L2, a single pole electro-thermal network is connected.

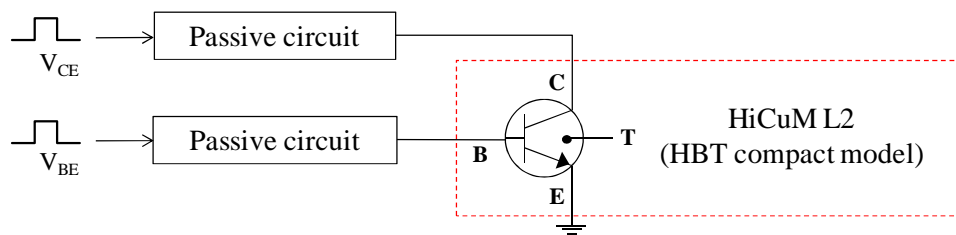


Figure 2-20: Circuit simulation setup with device compact model (HiCuM L2) and “passive circuit”.

Several simulations are performed using different cables (20, 40 and 100 cm) for cable – B” of “passive circuit”. In this simulations, “Coaxial cable – A” and other parasitics are similar. Two simulation results are presented, where we have used same quiescent and bias points ($V_{BE} = 0.7 - 0.9 \text{ V}$ and $V_{CE} = 0.3 - 1.0 \text{ V}$): (i) In Figure 2-21, V_{CE} and V_{BE} pulse widths are 300 ns. A significant parasitic noise current is observed for $L_{Cable} = 100 \text{ cm}$ ($L_{Cable} = 250 \text{ nH}$ and $C_{Cable} = 94$

pF) which is mixed with the transient I_C . Reducing L_{Cable} from 100cm to 40cm, the parasitic effect is minimized. (ii) In *Figure 2-22*, V_{CE} and V_{BE} pulse widths are 1500 and 300 ns respectively and $L_{\text{Cable}} = 20$ cm. Using smaller pulse width for V_{BE} than V_{CE} , the parasitic current is removed from the transient I_C and a smooth variation due to self-heating is observed. These optimized conditions are used for final measurements.

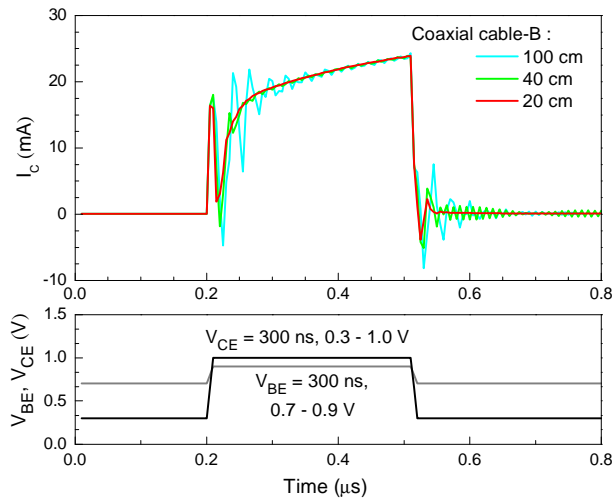


Figure 2-21: Circuit simulation with device compact model and “passive circuit” (cable lengths ~ 20, 40 and 100 cm) – pulse conditions: $V_{BE} = 300$ ns, 0.7 – 0.9 V; $V_{CE} = 300$ ns, 0.3 – 1.0 V. $\{L_E \times W_E = 10 \times 0.27 \mu\text{m}^2\}$

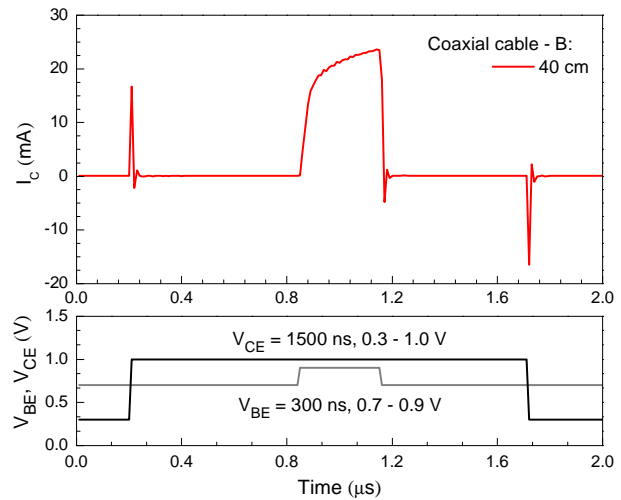


Figure 2-22: Circuit simulation with device compact model and “passive circuit” (cable lengths ~ 40 cm) – pulse conditions: $V_{BE} = 300$ ns, 0.7 – 0.9 V; $V_{CE} = 1500$ ns, 0.3 – 1.0 V. $\{L_E \times W_E = 10 \times 0.27 \mu\text{m}^2\}$

2.4.4 Measurements comparison and analysis

Two different measurements are compared in *Figure 2-23* and *Figure 2-24* for the transistor geometry with $L_E 10 \mu\text{m}$ and $W_E 0.27 \mu\text{m}$. In first measurement, a pulse width of 300 ns was applied for V_{BE} (0.7 – 0.95 V) as well as V_{CE} (0.3 – 1.5 V) and a cable length of 100 cm (for cable – B) was used (*Figure 2-23*). In second, a pulse width of 300 ns for V_{BE} (0.7 – 0.95 V) and 1500 ns for V_{CE} (0.3 – 1.5 V) was applied where the cable length was reduced to 40 cm as shown in *Figure 2-24*. The short time collector current transients $I_C(t)$ were noisy in first measurement condition. By applying a shorter V_{BE} pulse than the V_{CE} pulse, the parasitic current overshoot was separated from the $I_C(t)$. Therefore, the second condition is considered for the final measurements that have been performed on different geometries of device.

In the pulse measurement, the transistor is switched from a state of negligible power dissipation (quiescent point) to high power dissipation (bias point) with a rise/fall time of 10 ns. This rise/fall time is too short to change the temperature, only the electrical device response can be seen. Device self-heating starts after the thermal time constant and defines when I_C increases with time and reaches its steady state value.

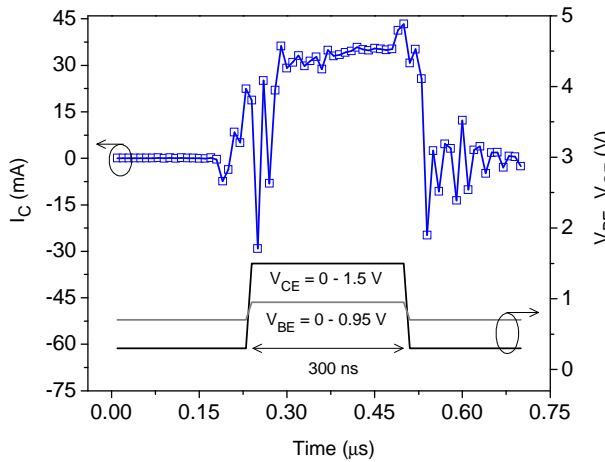


Figure 2-23: Measured $I_C(t)$ for $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$ with pulse conditions - $V_{BE} = 300 \text{ ns}, 0.7 - 0.95\text{V}$ and $V_{CE} = 300 \text{ ns}, 0.3 - 1.5\text{V}$; Coaxial cable - B ($\approx 100 \text{ cm}$ length): $L = 300\text{nH}, C = 86\text{pF}$

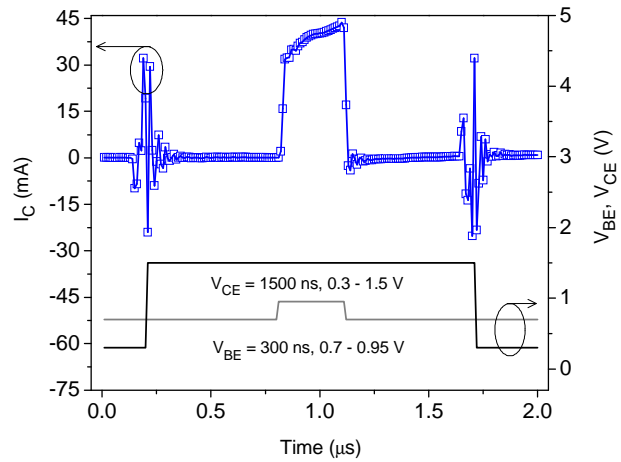


Figure 2-24: Measured $I_C(t)$ for $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$ with pulse conditions - $V_{BE} = 300 \text{ ns}, 0.7 - 0.95\text{V}$ and $V_{CE} = 1500 \text{ ns}, 0.3 - 1.5\text{V}$; Coaxial cable - B ($\approx 40 \text{ cm}$ length): $L = 100\text{nH}, C = 44\text{pF}$

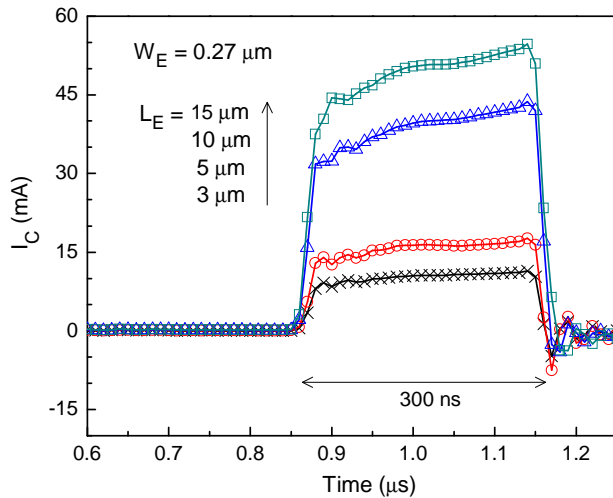


Figure 2-25: Measured $I_C(t)$ for different dimension of transistors with pulse conditions - $V_{BE} = 300 \text{ ns}, 0.7 - 0.95\text{V}$ and $V_{CE} = 1500 \text{ ns}, 0.3 - 1.5\text{V}$

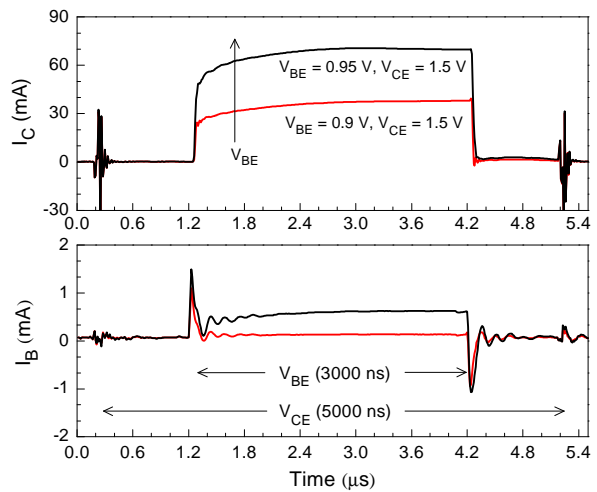


Figure 2-26: Measured $I_C(t)$ for $L_E \times W_E = 15 \times 0.27 \mu\text{m}^2$ with pulse conditions - $V_{BE} = 3000 \text{ ns}, 0.7 - 0.95\text{V}$ and $V_{CE} = 5000 \text{ ns}, 0.3 - 1.5\text{V}$

In *Figure 2-25*, $I_C(t)$ for different geometries of transistor is shown. These are measured with V_{BE} pulse 300 ns, 0.7 – 0.95 V and V_{DS} pulse 1500 ns, 0.3 – 1.5 V. The transient response of I_C increases with emitter dimension significantly due to increase in power dissipation. In order to reach the steady state of I_C we apply longer pulses like 3000 ns V_{BE} and 5000 ns V_{CE} . The measurement results are shown in *Figure 2-26*. It is noticed that nearly after 3000 ns pulse time, the I_B and I_C reaches to steady state.

2.5 Transient thermal modeling

Thermal parameters are extracted comparing measurements and transistor compact model simulations using HiCuM L2.

2.5.1 Influence of passive circuit

In order to perform an accurate extraction, the compact model is simulated in combination with the “passive circuit” (circuit simulation setup in *Figure 2-20*). The V_{BE} and V_{CE} pulse source are connected to the device terminals (B and C respectively) through the “passive circuits”. The electro-thermal network is connected at the temperature node of the compact model.

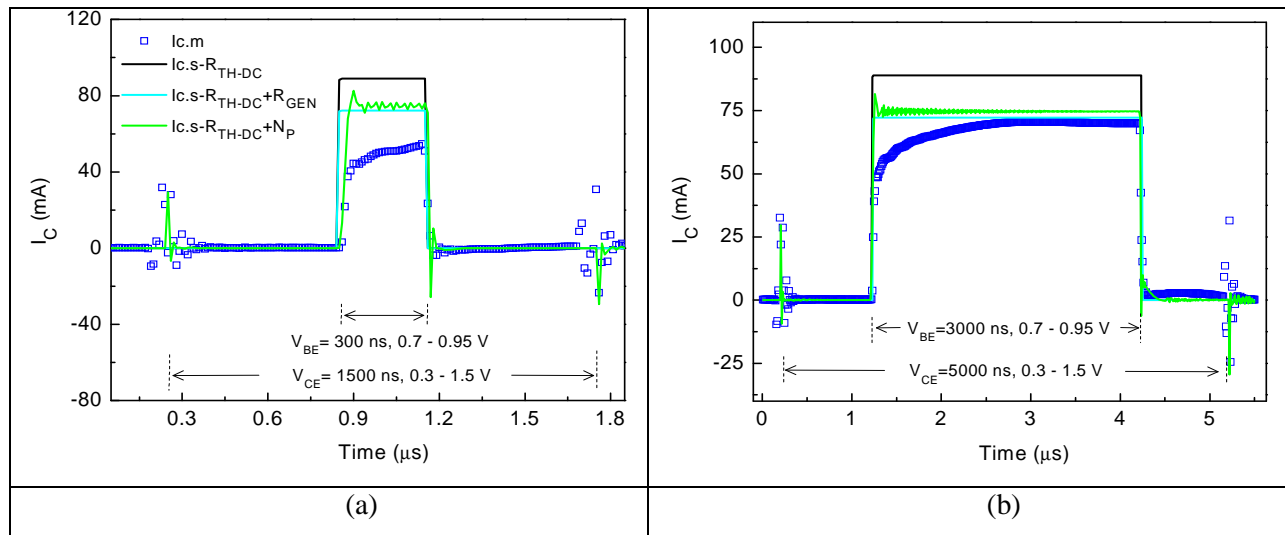


Figure 2-27: A comparison between measured transient I_C and HiCuM L2 simulation applying passive network ($L_E \times W_E = 15 \times 0.27 \mu\text{m}^2$); $I_{c.m}$ – measured I_C , $I_{c.s-R_{TH-DC}}$ – compact model simulation with a R_{TH} extracted from DC measurements at different ambient temperature, R_{GEN} – internal resistance of pulse generator, N_P – “passive circuit”: (a) $V_{BE} = 300 \text{ ns}$, 0.7 – 0.95 V; $V_{CE} = 1500 \text{ ns}$, 0.3 – 1.5 V (b)

$V_{BE} = 3000 \text{ ns}$, 0.7 – 0.95 V; $V_{CE} = 5000 \text{ ns}$, 0.3 – 1.5 V.

To underline the influence of the passive elements on compact model simulations results, different configuration are simulated, as show in *Figure 2-27*: (i) only a thermal resistance is connected: R_{TH} (IC.s- R_{TH-DC}), (ii) the internal resistance of pulse generator (IC.s- $R_{TH-DC}+R_{GEN}$) is added, and (iii) the complete “passive circuit” (IC.s- $R_{TH-DC} +N_P$) is considered. This R_{TH-DC} was extracted from DC measurements at different temperatures (section 3.1). Since a 300 ns pulse (*Figure 2-27 (a)*) is not sufficient to reach the steady state I_C , a longer pulse of 3000 ns (*Figure 2-27 (b)*) has been applied to extract R_{TH} from pulse measurement (R_{TH-P}). It can be seen that, I_C reaches steady state nearly after 2000 ns.

2.5.2 Comparison between single pole and recursive network in time domain

Compact model simulation including parasitic elements is mandatory to achieve an accurate parameter extraction. The thermal parameters for both networks are extracted from transient I_C measurements. After having an accurate value of R_{TH} , the parameters of the single pole and recursive network have been calculated using the Levenberg-Marquardt algorithm [29]. A comparison between measurement and HiCuM compact model simulation with a conventional single $R_{TH}-C_{TH}$ network is shown in *Figure 2-28*.

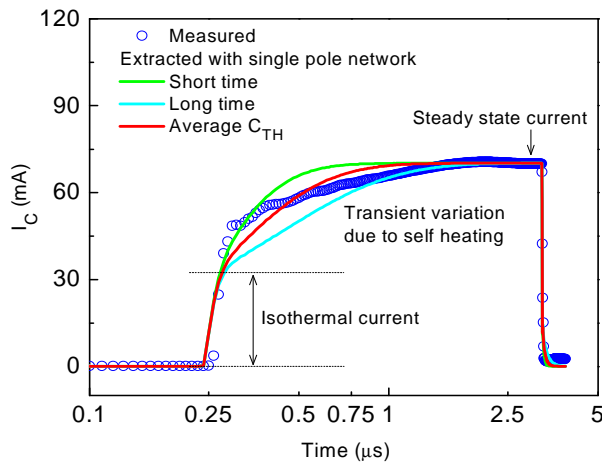


Figure 2-28: Thermal modeling with single pole network: comparison between measurements and HiCuM L2 simulation. ($A_E = 15 \times 0.27 \mu m^2$)

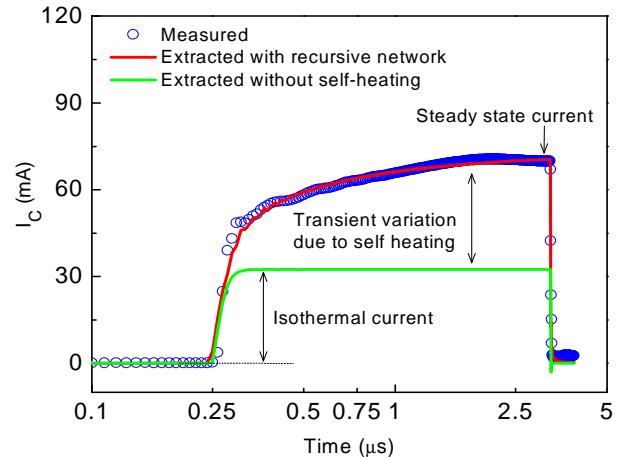


Figure 2-29: Thermal modeling with recursive network: comparison between measurements and HiCuM L2 simulation. ($A_E = 15 \times 0.27 \mu m^2$)

The steady state I_C is modeled with the R_{TH} , but it can be seen from the figure that the transient variation region cannot be properly modeled with a single C_{TH} . Therefore, different

extractions are performed in order to model the very short time and long time transient region, which could give an approximate minimum and maximum value of C_{TH} respectively. In order to model the whole transient thermal region of I_C , a recursive network has been taken into account. *Figure 2-29* shows the comparison between compact model simulations and the measurements. The isothermal current is extracted without any thermal network that shows only the device electrical response. The described methodology results a very good agreement between measured and simulated I_C . The thermal parameters for both networks are extracted and will be verified by other methods. The comparison among different results will be presented in the *chapter 5*.

2.5.3 Transient variation of junction temperature

After having an accurate value of thermal parameters, base – collector junction temperature T_j is calculated through transistor compact model simulation. In *Figure 2-30*, T_j is calculated using single pole (with average C_{TH} value) and recursive electro-thermal network for the device with $A_E = 15 \times 0.27 \mu\text{m}^2$ and at bias point $V_{CE} = 1.5 \text{ V}$ and $V_{BE} = 0.95 \text{ V}$. A significant difference is observed. Therefore, a recursive network can be used in order to determine the accurate junction temperature variations of the device.

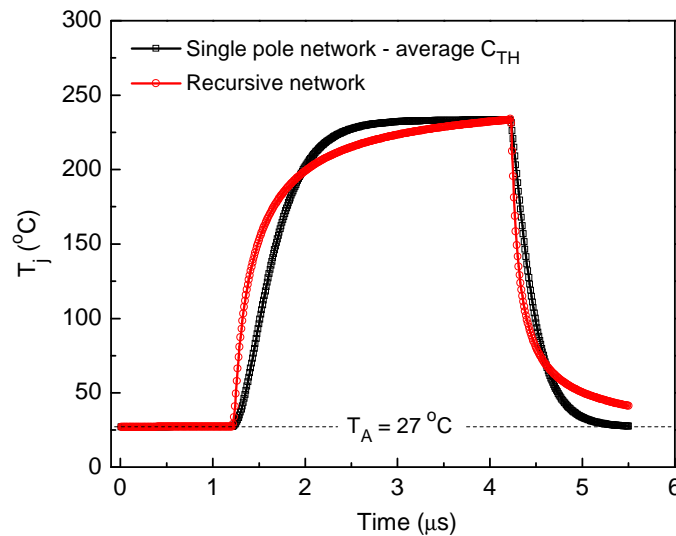


Figure 2-30: Base – collector junction temperature T_j variation with time – calculated with single pole and recursive network ($A_E = 15 \times 0.27 \mu\text{m}^2$ and bias point $V_{CE} = 1.5 \text{ V}$ and $V_{BE} = 0.95 \text{ V}$).

2.6 Isothermal data extraction

In this part we present a new and simple methodology to extract isothermal data using measurements at different wafer temperature i.e. T_A . We assume that, the variation of I_C with T_A is linear for simplicity. The extractions need,

- i. $I_C - V_{CE}$ and $I_C - V_{BE}$ characteristics at different T_A
- ii. A wide range of temperature for the accuracy in extraction
- iii. An accurate R_{TH} value

In the next section, the methodology is described to obtain isothermal characteristics. Then the method is compared to pulse measurement method applied to a $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$ HBT.

2.6.1 DC output and forward Gummel at different T_A

Steady state output and forward Gummel characteristics are measured at different T_A between 0 and 100 °C. In *Figure 2-31* and *Figure 2-32*, the DC measurements are shown between 0 and 50 °C. The variation of I_C with T_A is found to be almost linear.

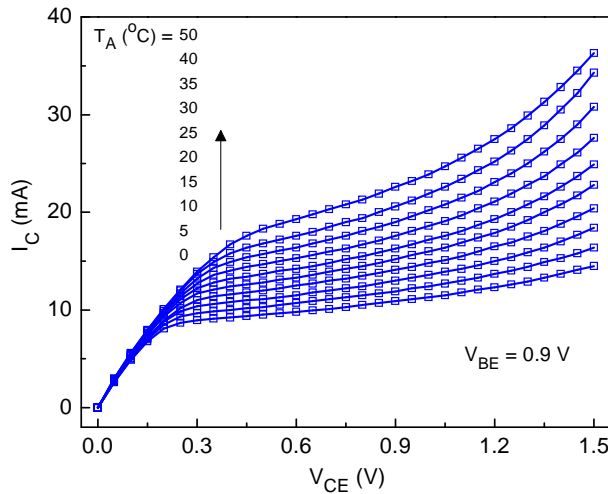


Figure 2-31: Output characteristics at different T_A (0 to 50 °C) for transistor dimension $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$.

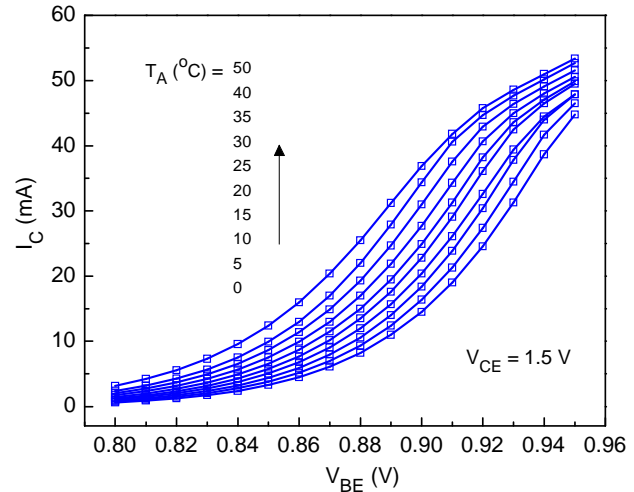


Figure 2-32: Forward Gummel characteristics at different T_A (0 to 50 °C) for transistor dimension $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$.

2.6.2 Extraction methodology

In the previous measurements, it is found that the variation of I_C is linear at wide T_A range. At low bias, the self-heating is negligible; the internal transistor temperature T_i is equal to

the wafer temperature. At higher bias, the self-heating increases the temperature due to the internal power dissipation P_{diss} . It leads to a temperature rise of ΔT in the internal transistor. The change in temperature can be described as,

$$\Delta T = T_j - T_A = R_{TH} \cdot I_C(V_{CE}, V_{BE}, T_A) \cdot V_{CE} \quad Eq. 2-5$$

Therefore, the base-collector junction temperature is given by,

$$T_j = T_A + R_{TH} \cdot P_{diss} = T_A + R_{TH} \cdot I_C(V_{CE}, V_{BE}, T_A) \cdot V_{CE} \quad Eq. 2-6$$

At different T_A value, T_j can be calculated using the previous output characteristic measurements.

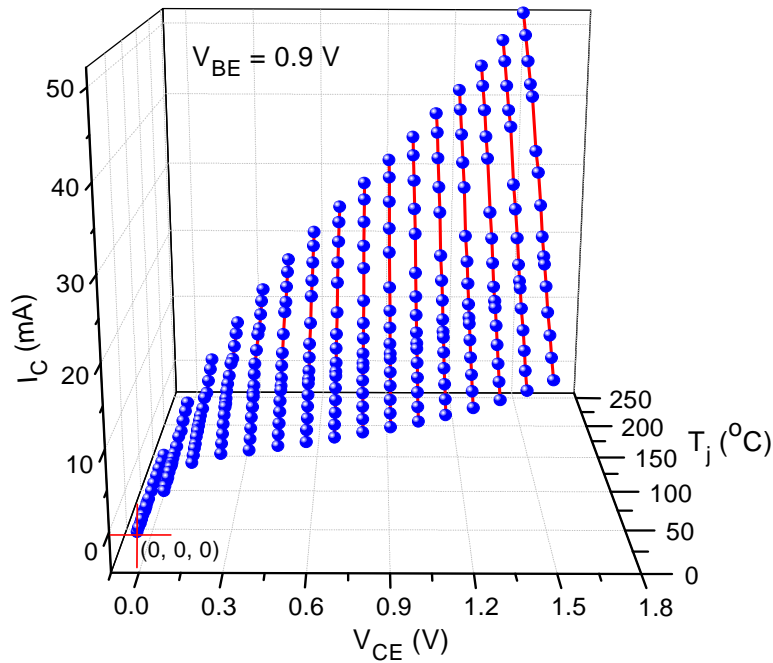


Figure 2-33: The variation of I_C with junction temperature T_j at different V_{CE} (calculated from $I_C - V_{CE}$ characteristics at different T_A); constant $V_{BE} = 0.9$ V.

In Figure 2-33, I_C vs. T_j is plotted for different V_{CE} and at $V_{BE} = 0.9$ V. This data is calculated from $I_C - V_{CE}$ characteristics at different T_A using Eq. 2-6. The I_C variation with T_j for different V_{BE} is shown in Figure 2-34 which is calculated from forward Gummel characteristics at different T_A . It can be seen from the figures that, I_C s are linear with T_j . Therefore, this can be represented by,

$$I_{C-DC}(V_{CE}, V_{BE}, T_A) = \frac{\Delta I_C(V_{CE}, V_{BE}, T_A)}{\Delta T_j} T_j + I_C^0(V_{CE}, V_{BE}, T_A = T_j) \quad \text{Eq. 2-7}$$

Here, I_{C-DC} is steady state collector current, I_C^0 is the collector current when $T_A = T_j$, i.e. $\Delta T = 0$. Hence, this is the isothermal current for a constant V_{BE} and V_{CE} .

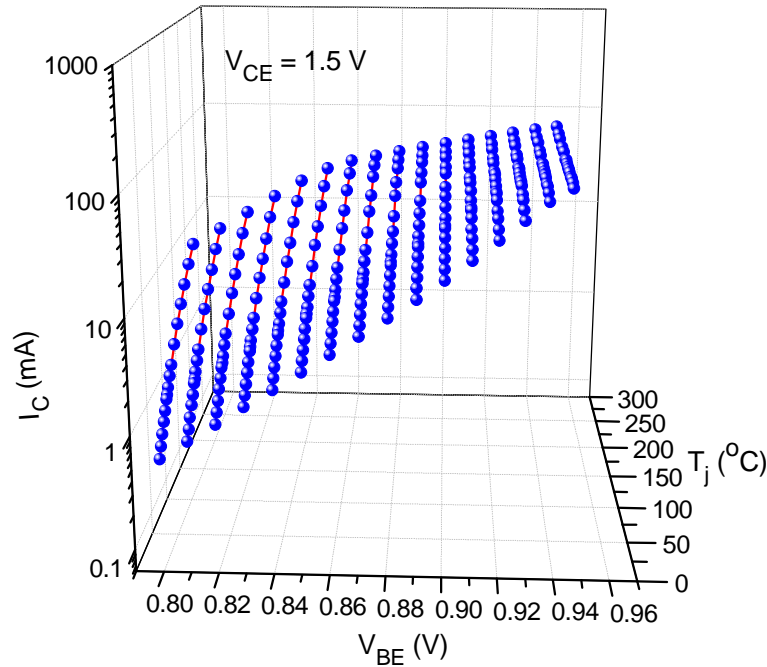


Figure 2-34: The variation of I_C with junction temperature T_j at different V_{BE} (calculated from forward Gummel characteristics at different T_A); constant $V_{CE} = 1.5$ V.

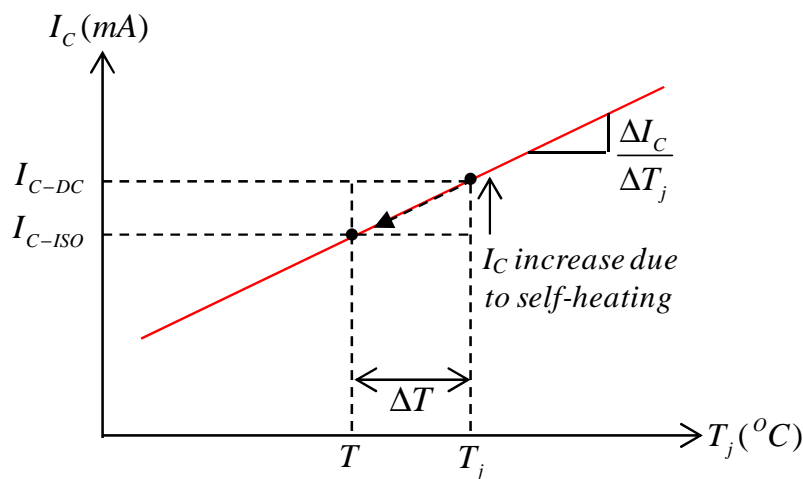


Figure 2-35: Extraction of isothermal collector current (I_{C-ISO}) from steady state collector current (I_{C-DC}) vs. junction temperature (T_j) curve.

At any value of V_{BE} and V_{CE} , the isothermal collector current (I_{C-ISO}), at any desire temperature T , can be described by,

$$I_{C-ISO}(V_{CE}, V_{BE}, \Delta T = 0) = \frac{\Delta I_C(V_{CE}, V_{BE}, T_A)}{\Delta T_j} T + I_C^0(V_{CE}, V_{BE}, T_A = T_j) \quad \text{Eq. 2-8}$$

From, Eq. 2-7 and Eq. 2-8,

$$I_{C-ISO}(V_{CE}, V_{BE}, \Delta T = 0) = I_{C-DC}(V_{CE}, V_{BE}, T_A) - \frac{\Delta I_C(V_{CE}, V_{BE}, T_A)}{\Delta T_j} (T - T_j) \quad \text{Eq. 2-9}$$

Using Eq. 2-9, the corresponding isothermal characteristic of $I_C - V_{CE}$ or $I_C - V_{BE}$ characteristics can be extracted.

2.6.3 Isothermal characteristics and validation

Following the above described methodology, the isothermal data has been extracted as follows: (i) *Figure 2-36*: output characteristic $I_C - V_{CE}$ for $V_{BE} = 0.95$ V, at temperature $T = 27$ °C and (ii) *Figure 2-37*: Gummel characteristic $I_C - V_{BE}$ for $V_{CE} = 1.5$ V, at temperature $T = 27$ °C. The extracted data is compared to pulse measurements with 150 ns pulse width at $T = 27$ °C. A good agreement is obtained.

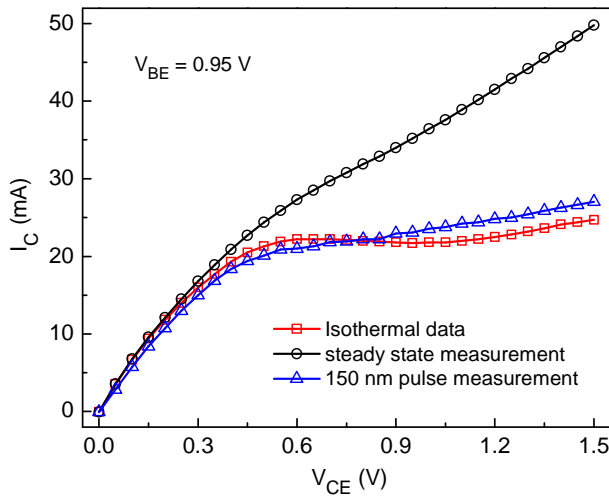


Figure 2-36: Output characteristic - Comparison between extracted isothermal data and pulse measurement; transistor dimension $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$.

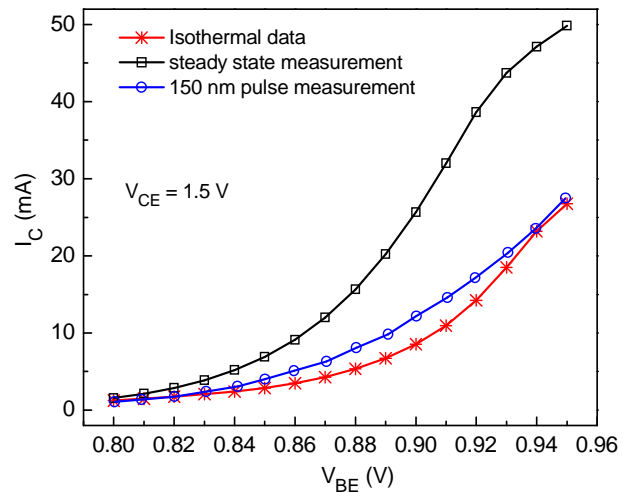


Figure 2-37: Forward Gummel characteristic - Comparison between extracted isothermal data and pulse measurement; transistor dimension $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$.

2.6.4 Limitations of the approach

The described isothermal extraction methodology is very simplified and valid only for DC characteristics. In this extraction procedure, for simplicity we assume that, the variation of I_C is linear with temperature. In case of measurements at wide temperature range, the devices with larger value of R_{TH} and the devices which present nonlinear behavior of I_C with temperature, this method may not properly work. Therefore, in order to make the methodology more generalized, instead of linear extrapolation a quadratic extrapolation may be needed. The extraction is performed with a single R_{TH} parameter. In general R_{TH} of a device depends on temperature and also P_{diss} (as the thermal conductivity of Si is strongly depend on temperature). Therefore, instead of using a single R_{TH} , a temperature/power density dependent R_{TH} model can give better isothermal data and may valid for all P_{diss} range.

2.7 Low frequency s-parameter measurements

The measurements are performed several times using different network analyzers like: (i) Agilent HP 8753C, HP 8753D network analyzer with HP 85047A test set – between 300 kHz and 3 GHz frequency range, (ii) Anritsu-MS2026B vector network analyzer – between 100 kHz and 3 GHz frequency range. HP 4145B semiconductor parameter analyzer is used to set the DC bias points. A measurements result with Agilent HP 8753C VNA is shown which is performed on wafer at room temperature (27 °C). A SOLT (Short-Open-Load-Thru) calibration technique is used. We perform, the s-parameter analysis in the low frequency band in the range of frequency where self-heating is visible. In *Figure 2-38*, magnitude and phase of s-parameters are shown, which are measured at RF power -30 dBm (at source port) and different DC bias conditions (V_{BE} , $V_{CE} = 0.90$ V, 1.0 V; 0.95 V, 1.0 V; 0.90 V, 1.5 V and 0.95 V, 1.5 V respectively). At these DC bias points device self-heating is significant which is necessary for measurement accuracy. It is evident from the measured results that, the magnitude of s_{11} and s_{21} curves (*Figure 2-38 (a) and (b)*) are almost constant with frequency (only varies with DC bias) where the slope of s_{12} and s_{21} (*Figure 2-38 (c) and (d)*) changes considerably in low frequency region after a certain frequency (nearly 200 MHz). Moreover, the slope of s_{12} and s_{21} increases with DC bias, which signifies the dynamic self-heating. The s-parameters are converted to y-parameter, as the self-heating effect explanation is more complex with s-parameters. The corresponding analysis

of dynamic self-heating with y - parameters in combination with electro-thermal modeling is presented in next section.

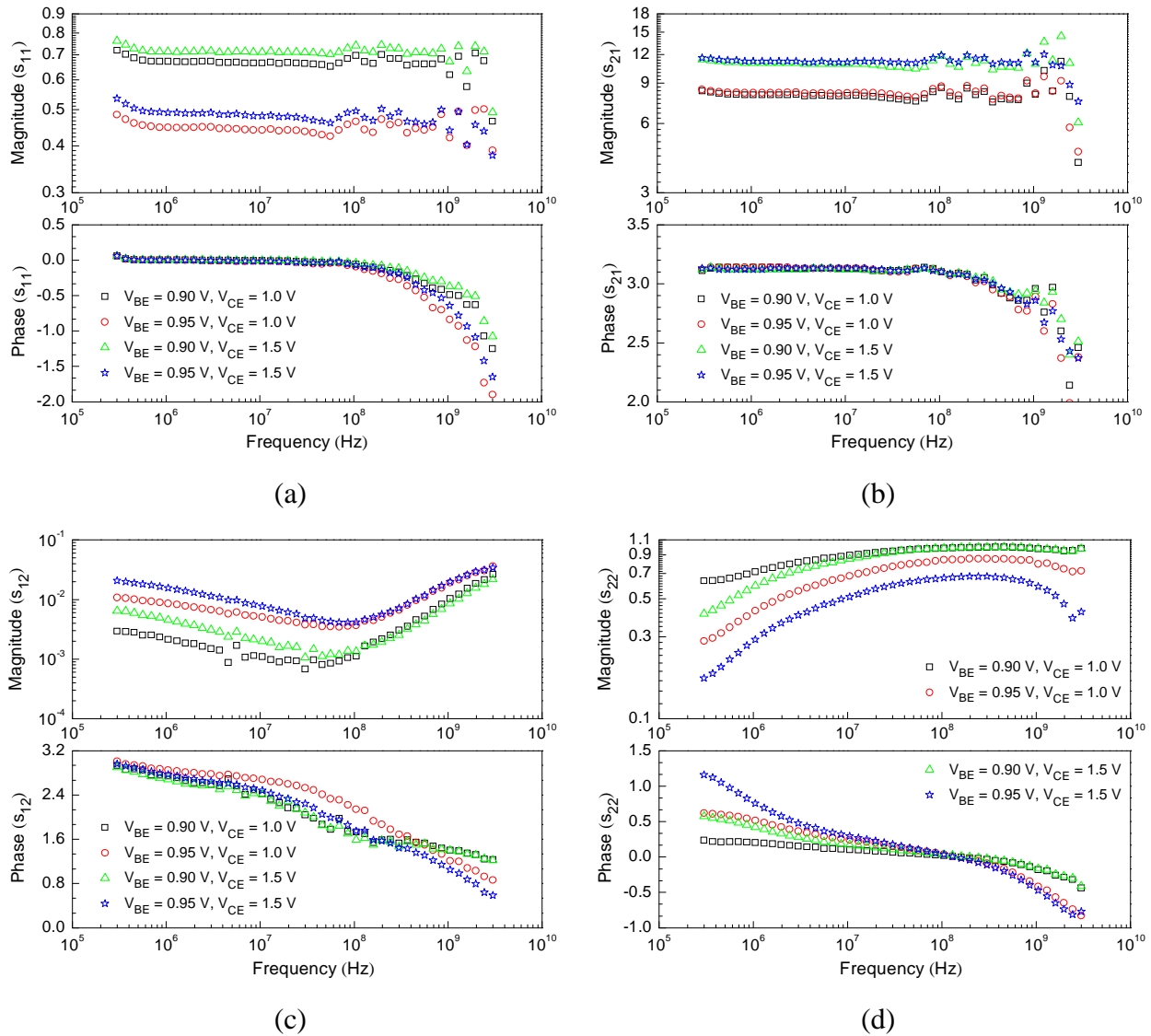


Figure 2-38: Magnitude and phase of s - parameters at different DC bias conditions $\{L_E \times W_E = 10 \times 0.27 \mu\text{m}^2\}$ - (a) s_{11} , (b) s_{21} , (c) s_{12} and (d) s_{22} .

2.8 Dynamic thermal modeling

2.8.1 Y-parameters and dynamic self-heating

Dynamic self-heating is analyzed on y -parameters which were converted from measured s - parameters. At frequency domain, y -parameters can be given by,

$$\begin{aligned}
 Y_{11} &= \left. \frac{\Delta I_B}{\Delta V_{BE}} \right|_{\Delta V_{CE}=0} & Y_{21} &= \left. \frac{\Delta I_C}{\Delta V_{BE}} \right|_{\Delta V_{CE}=0} \\
 Y_{12} &= \left. \frac{\Delta I_B}{\Delta V_{CE}} \right|_{\Delta V_{BE}=0} & Y_{22} &= \left. \frac{\Delta I_C}{\Delta V_{CE}} \right|_{\Delta V_{BE}=0}
 \end{aligned}
 \tag{Eq. 2-10}$$

According to Eq. 2-10, y_{11} and y_{21} are the slope of the $I_B=f(V_{BE})$ and $I_C=f(V_{BE})$ characteristics at constant V_{CE} which are less sensitive to self-heating. On the other hand, y_{22} and y_{12} corresponds to the slope of the $I_C=f(V_{CE})$ and $I_B=f(V_{CE})$ characteristics at constant V_{BE} . These two DC measurements are well known to be used for self-heating parameter extraction. Except at very high power level, the thermally induced deviation in y_{11} and y_{21} are minor (taking care to scale). However, y_{22} and y_{12} can change significantly even with negligible power [30] and is strongly dependent on collector current [31]. The thermally induced components of y -parameters eventually become negligible as frequency goes up. At high frequency, thermal behavior is dominated by device electrical behavior.

In Figure 2-39, measured y -parameters are compared with compact model simulations without dynamic self-heating. This is obtained by simulating without C_{TH} . As observed, the parameters y_{22} and y_{12} are much more sensitive to dynamic self-heating than y_{11} and y_{21} (taking care to the scale). Dispersive device behavior [32] has been found at frequencies below the thermal time constant (≈ 200 MHz for the transistor with $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$).

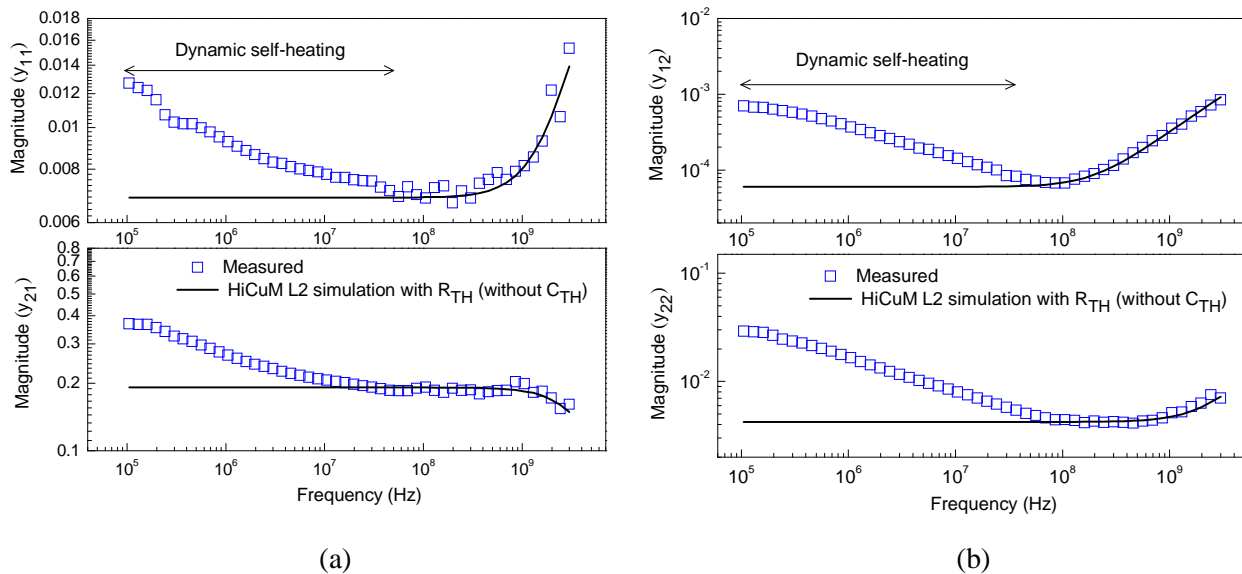


Figure 2-39: Magnitude of y -parameters ($L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$ with configuration CBE): measured and HiCuM L2 simulation without dynamic self-heating - (a) y_{11} and y_{21} , (b) y_{12} and y_{22} .

2.8.2 Comparison between single pole and recursive network in frequency domain

The y_{12} and y_{22} parameters are taken into account for electro-thermal compact modeling and parameter extraction. We have compared two different networks, single pole and recursive network, in order to model dynamic self-heating effect. A comparison between measurements and compact model simulations is presented in *Figure 2-40*. It is obvious from the measurements and compact model simulations that below 200MHz, thermal effect dominates the device electrical effect and can be modeled with C_{TH} . In this region, the parameter C_{TH} of single pole or K_C and C of the recursive network have been extracted. The recursive type thermal network provides the best conciliation to model frequency domain thermal effect. This underlines the existence of multiple thermal time-constant in dynamic self-heating effect. A good agreement between measurements and electro-thermal compact modeling has been achieved.

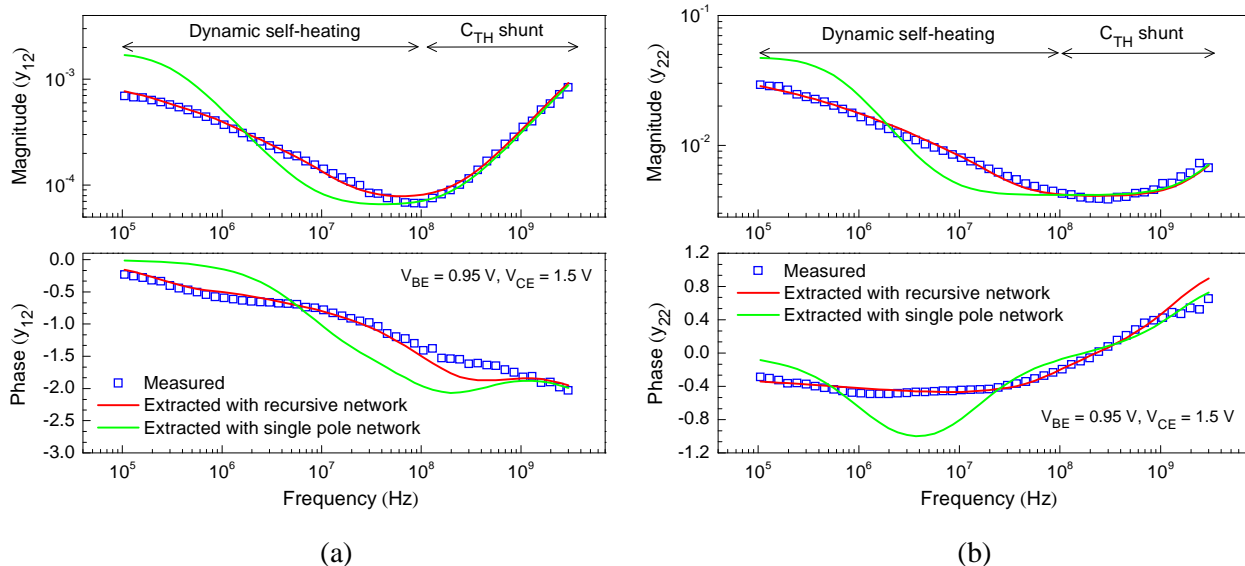


Figure 2-40: Magnitude and phase of y -parameters ($L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$ with configuration CBE): measurements and HiCuM L2 simulation without single pole and recursive network - (a) y_{12} , (b) y_{22} .

2.9 Z_{TH} extraction

It is observed in section 2.8.1 that, parameters y_{22} and y_{12} are much more sensitive to dynamic self-heating than y_{11} and y_{21} . Therefore, in order to extract Z_{TH} we consider y_{22} and y_{12} . The normalized forms of Z_{TH} , calculated from y_{12} and y_{22} , are given by the following equations (see *chapter 1*):

$$Z_{thN}^{ij}(\omega) = \frac{(y_{ij}(\omega) - y_{ij}^{AC})}{(y_{ij}^{DC} - y_{ij}^{AC})} \cdot \frac{(I_j + V_{j-1}y_{j-1,j}^{DC} + V_j y_{jj}^{DC})}{(I_j + V_{j-1}y_{j-1,j}(\omega) + V_j y_{jj}(\omega))}, \quad Eq. 2-11$$

for $i=1,2$ and $j=2$

Here, 1 and 2 denotes the base and collector terminals respectively of the two port device. Using the above equation Z_{TH} can be extracted from y_{12} and y_{22} parameters. It can be assumed that, the measured y -parameters contain two parts: one is an equithermal part or the AC part where only DC self-heating effects are visible and which has been measured at high frequency (above thermal cut-off frequency) and the other is the thermal part (below thermal cut-off frequency) where both AC and DC self-heating effects are equally visible. We have selected two regions in y -parameters: (i) the AC isothermal region (above 200 MHz) and (ii) the AC self-heating affected region or non-isothermal region (below 200 MHz). For $i=1$ and $j=2$; $y_{ij}^{DC} = y_{j-1,j}^{DC} = y_{12}^{DC}$ and $y_{jj}^{DC} = y_{22}^{DC}$. Similarly, For $i=2$ and $j=2$; $y_{ij}^{DC} = y_{jj}^{DC} = y_{22}^{DC}$ and $y_{j-1,j}^{DC} = y_{12}^{DC}$. Now y_{12} and y_{22} is given by,

$$y_{22}(\omega) = \left. \frac{\partial i_C}{\partial v_{CE}} \right|_{\Delta V_{BE}=0}, \quad y_{12}(\omega) = \left. \frac{\partial i_B}{\partial v_{CE}} \right|_{\Delta V_{BE}=0} \quad Eq. 2-12$$

At frequency $\rightarrow 0$, $y_{12}(\omega)$ and $y_{22}(\omega) \rightarrow y_{12}^{DC}$ and y_{22}^{DC} . Therefore, y^{DC} s can be calculated from the derivative of output characteristic ($I_C - V_{CE}$ and $I_B - V_{CE}$ at constant V_{BE}).

In order to extract Z_{THN} from y -parameter, the other necessary parameter is y_{ij}^{AC} . The y_{ij}^{AC} describes the AC isothermal behavior or without dynamic self-heating behavior of the device. To extrapolate y_{ij}^{AC} at low frequency region, we consider two different methodologies.

❖ **Method I (with compact model):** If the compact model is available, y_{ij}^{AC} can be obtained very easily. At frequency below thermal time constant ($\tau_{thermal}$) the y -parameters changes the slope due to dynamic self-heating, where the frequency above $f_{thermal}$, dynamic self-heating is dominated by high frequency device electrical behavior.

The self-heating only due to DC bias exists in overall frequency region that could be extracted with a R_{TH} . The AC isothermal curve is extracted through compact model simulation when $C_{TH} = 0$. In

Figure 2-41, the magnitude and phase of y_{22}^{AC} is obtained through HiCuM L2 simulation without C_{TH} .

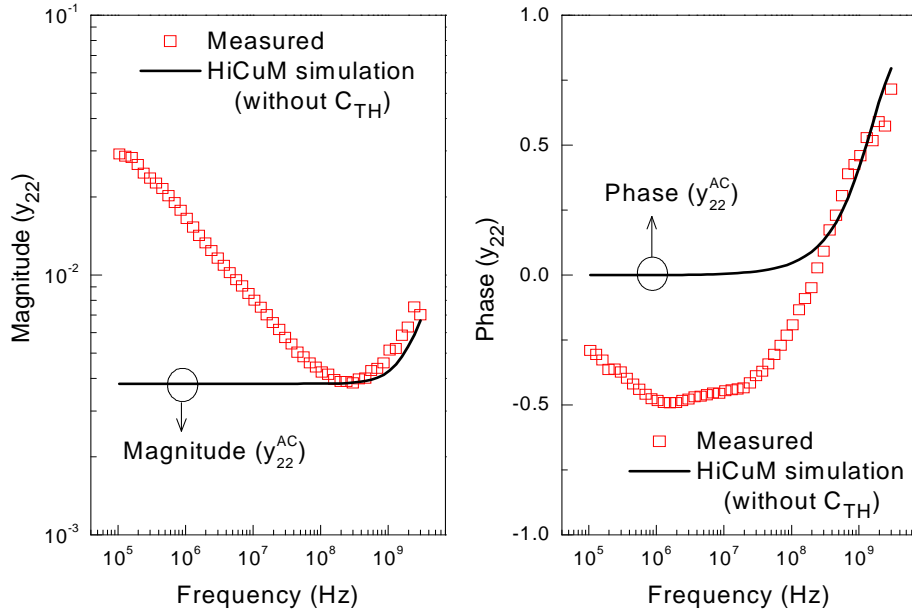


Figure 2-41: Magnitude and phase of y_{22} : Comparison between measurements and AC isothermal data (HiCuM simulation without C_{TH}).

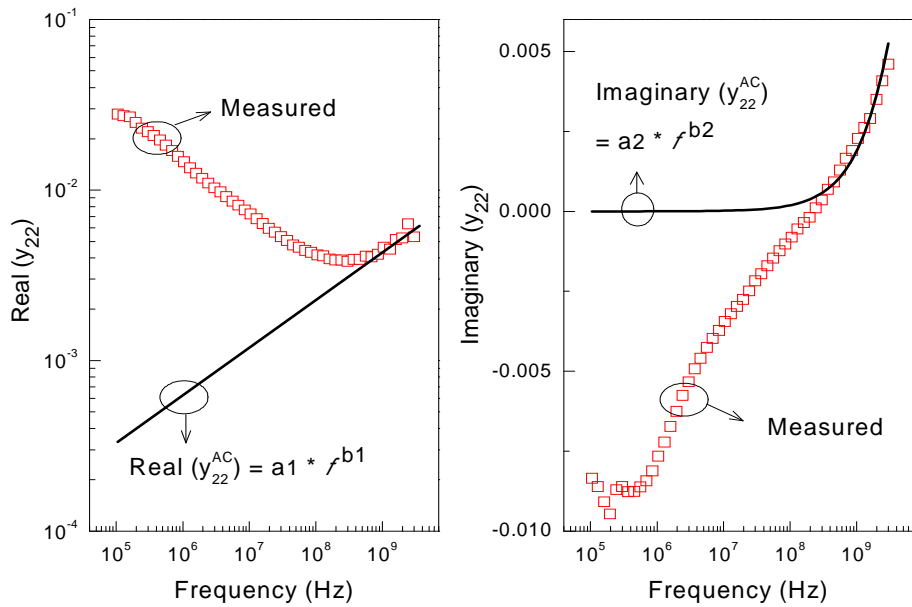


Figure 2-42: Magnitude and phase of y_{22} : extrapolation of AC isothermal data using a power function.

❖ **Method II (Without compact model):** In this case an approximate y_{ij}^{AC} can be calculated. A mathematical function can be fitted on the AC isothermal region which

corresponds to y_{ij}^{AC} . In *Figure 2-42*, a power function is taken to extrapolate the AC isothermal region of real and imaginary part of y_{22} . Therefore, y_{ij}^{AC} can be given by,

$$\begin{aligned} \text{real}(y_{22}^{AC}) &= a1 \cdot f^{b1} \\ \text{imaginary}(y_{22}^{AC}) &= a2 \cdot f^{b2} \\ y_{22}^{AC} &= a1 \cdot f^{b1} + j \cdot a2 \cdot f^{b2} \end{aligned} \quad \text{Eq. 2-13}$$

❖ Comparison between two methods:

In order to extrapolate the AC isothermal data (y_{ij}^{AC}), the above described two methods are used. A comparison in Z_{TH} extraction, using *method I* and *method II* for y_{ij}^{AC} , is shown in *Figure 2-43*. A good compromise is found between two methods.

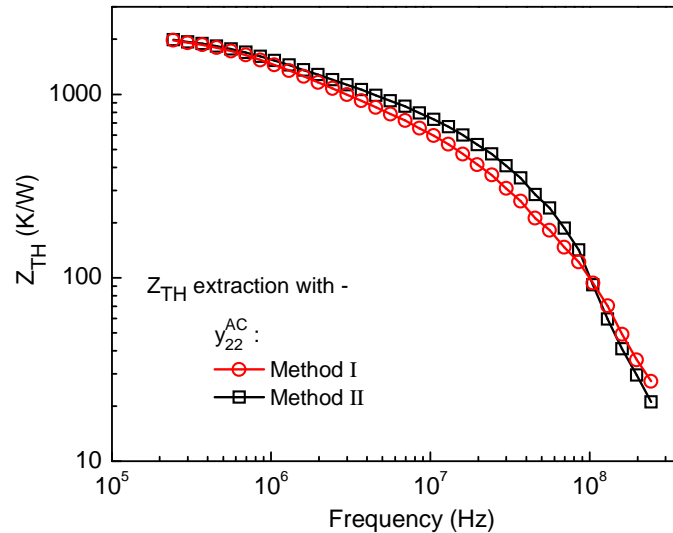


Figure 2-43: Z_{TH} extraction using Eq. 2-11: comparison between method I and II for y_{ij}^{AC} extrapolation.

2.9.1 Frequency domain slope and Maximum phase shift

Figure 2-44 shows the extracted magnitude and phase of normalized Z_{TH} for the transistor with $L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$ (configuration CBE). This extraction is performed from y_{22} parameter using the *Eq. 2-11* and with *method II* described above. We intend to point out that the slope of the curve is ~ -10 dB/dec, which confirms the one over square root dependence of the thermal impedance with respect to the Laplace variable p . This is the experimental verification of the theoretical work by Mnif et al. in [33].

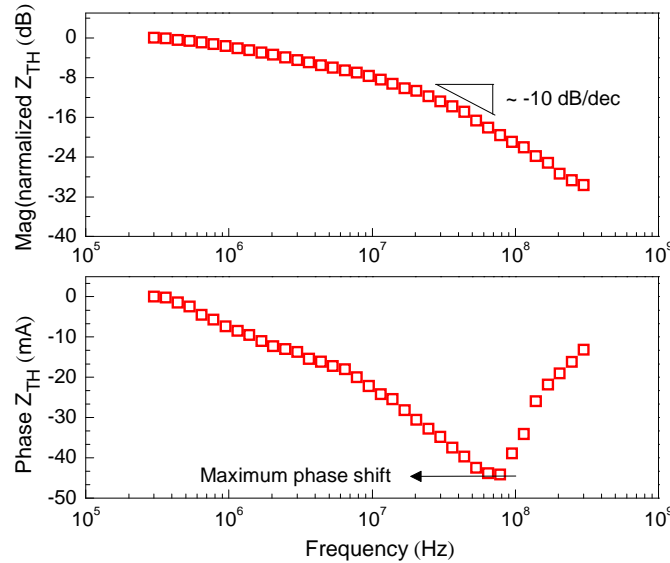


Figure 2-44: Extracted magnitude and phase of normalized Z_{TH} ; ($L_E \times W_E = 10 \times 0.27 \mu\text{m}^2$ with configuration CBE)

2.9.2 Modeling and comparison among different networks

The dynamic link between instantaneous power dissipation and the temperature variation due to self-heating is implemented into a compact model using a passive network. A variety of analytical models have been developed to analyze self-heating by connecting different electro-thermal networks, such as single pole network, Foster network, Nodal network, Cauer network, Recursive network etc. at the temperature node of the compact model. In this work, a comparison among different networks is presented in Z_{TH} modeling. Normalized Z_{TH} has been modeled in frequency domain with: (i) single pole network with a R_{TH} and C_{TH} , (ii) generalized thermal equivalent circuit or Foster network taking a 8-pole network and (iii) Nodal network with 8-cells and (iv) Recursive network taking up to the 8th exponent of k . The modeling results are shown below.

2.9.2.1 Magnitude and phase of Z_{TH}

Figure 2-45 and Figure 2-46 gives the magnitude and phase of the normalized thermal impedance. It is evident from the figure that, the measured thermal impedance is better fitted while modeling with recursive network than the other networks. From the comparison it is identified that fitting with recursive network is better than the other networks. On the other hand, it is evident that for the Foster network, it would be necessary to calculate all of the different R_{TH}

and C_{TH} elements and the number of parameters to extract is $2n$ (n is the number of cells). In contrary, in Recursive network there are only 3 parameters to be extracted and in the Nodal network there are only 2 parameters to be determined, and this for any number of cells. Thus the optimization is much more difficult in the Foster network than in the other two. That is why the Nodal or Recursive network should be used for transient thermal modeling.

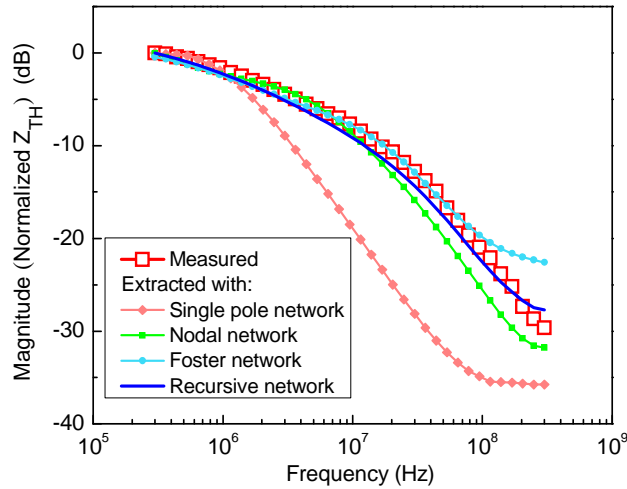


Figure 2-45: Thermal modeling of magnitude of Z_{TH} – comparison among different electro-thermal network.

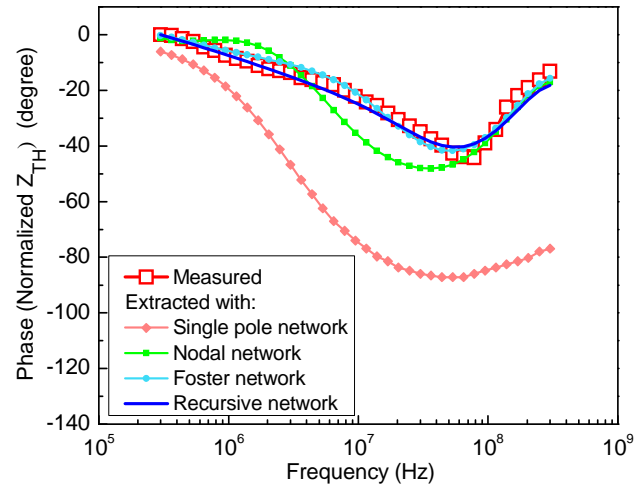


Figure 2-46: Thermal modeling of phase of Z_{TH} – comparison among different electro-thermal network.

Extracted parameter values for the electro-thermal networks:

- ❖ Simple electro-thermal network ($R_{TH} = 2230$ K/W, $C_{TH} = 109$ pWs/K)
- ❖ Generalized thermal equivalent network or Foster network with $n = 8$ (R_{THs} in K/W: $R_{TH0}, R_{TH1}, \dots, R_{TH8} = 63.5, 270.5, 971.8, 390, 65, 12, 2.5, 1.5$ and C_{THs} in Ws/K: $C_{TH0}, C_{TH1}, \dots, C_{TH8} = 9.5e-12, 13e-12, 70e-12, 70e-12, 3.5e-9, 7.25e-7, 3.0e-5, 6.8e-5$)
- ❖ Total thermal impedance including steady state thermal impedance ($R_{TH} = 2230$ K/W) and transient state thermal impedance (Z_{trans}) where Z_{trans} can be represented by Nodal network ($n = 8, R = 750$ K/W and $C = 70$ pWs/K) or Recursive network ($n = 8, R = 214$ K/W, $C = 14$ pWs/K and $k = 2.1$).

2.9.2.2 y -parameter

The magnitude of y_{22} has been modeled with different networks connecting at the temperature node of the HiCuM L2. The parameters of the electro-thermal network are same as

extracted before. A comparison between measurements and compact model simulation is shown in *Figure 2-47*. A very good agreement between measurements and compact model simulation with recursive network has been obtained.

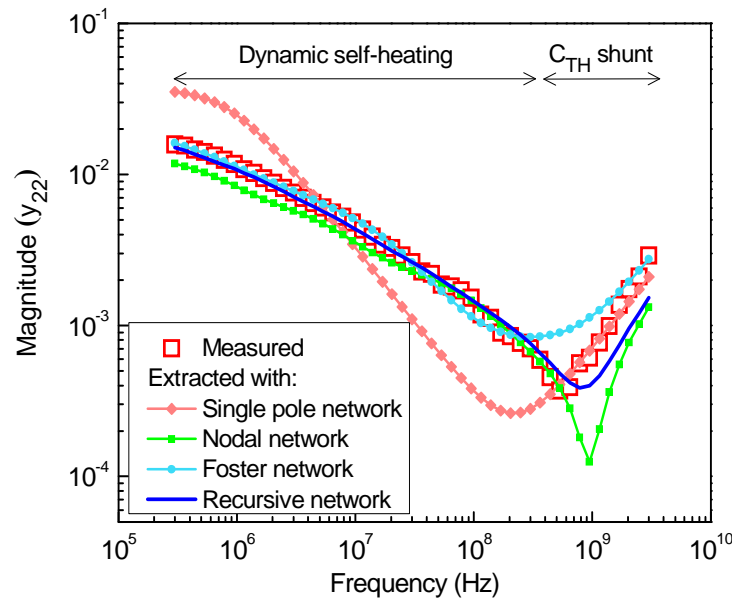


Figure 2-47: Thermal modeling of magnitude of y_{22} – comparison among different electro-thermal network.

When a transient or dynamic power is applied to the device, theoretically an infinite number of thermal time constants are necessary to represent the thermal response of the material due to the distributed nature. Thus, thermal capacitance due to dynamic self-heating could not be properly modeled with a single pole network, as it has a single time constant. Therefore, in order to model the transient or dynamic thermal behavior, a recursive network needs to be used.

2.9.3 Geometry dependent y -parameter and extracted Z_{TH} s

The magnitude of frequency domain Z_{TH} has been extracted for different transistor geometries with CBEBE configuration. These measurements are performed with Anritsu-MS2026B VNA at 27°C temperature. The Z_{TH} extractions are performed from y_{12} -parameters applying *Method - I*. In *Figure 2-48* and *Figure 2-49*, the measured y -parameters and the corresponding extracted magnitude of Z_{TH} s are presented for different geometries of transistor.

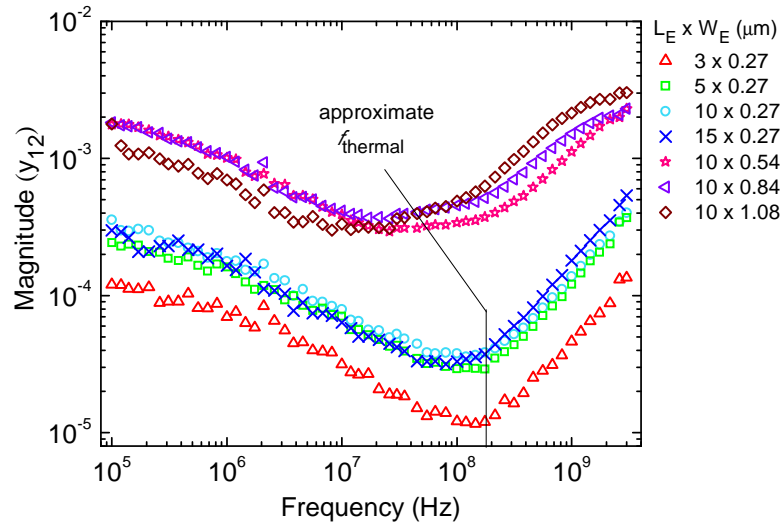


Figure 2-48: Magnitude of y_{12} for different geometries of transistors.

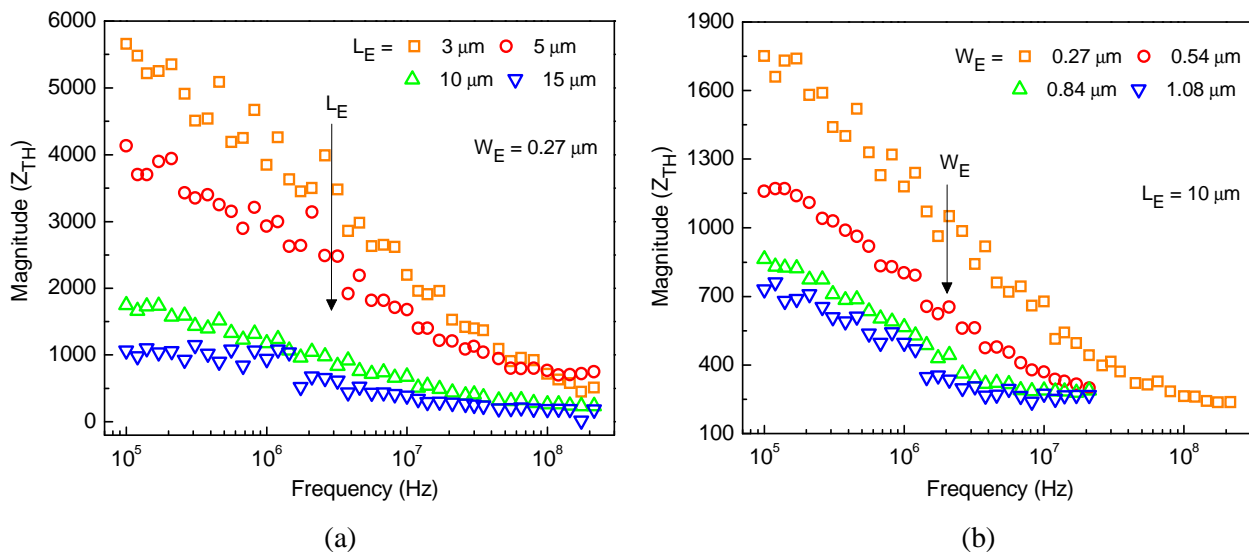


Figure 2-49: Magnitude of frequency domain Z_{TH} for different geometries of transistors – (a) different L_E at $W_E = 0.27 \mu\text{m}^2$ and (b) W_E at $L_E = 10 \mu\text{m}^2$; device configuration CBEB.

At frequencies below the thermal cutoff frequency ($1/\tau_{\text{thermal}}$), the junction temperature variation follows the instant power dissipation in the device, leading to electro-thermal feedback. The τ_{thermal} increases with the emitter area ($L_E \times W_E$). Therefore, the frequency band (below $1/\tau_{\text{thermal}}$) shifts towards lower frequencies when the dimension of the emitter window increases (Figure 2-48). For the frequencies above $1/\tau_{\text{thermal}}$, the junction temperature variation can no longer follow the instant power dissipation: the electro-thermal feedback is no longer significant

and the device behavior is dominated by its electrical characteristics only. Thus, the magnitude and phase of Z_{TH} could only be extracted up to $1/\tau_{thermal}$. For instance, in *Figure 2-49* the magnitude of Z_{TH} of larger devices (different W_E) are obtained up to 20 MHz, while Z_{TH} of smaller devices (different L_E with minimum W_E) is extracted up to 200 MHz.

2.10 Conclusion

An extensive evaluation of self-heating effect is presented through different measurements and compact model simulations. The pulse measurement technique for self heating characterization of trench isolated microwave HBTs has been extensively investigated. The transient response of collector current has been measured accurately under optimized test conditions. Model parameters are extracted and validated through circuit simulations including an accurate transistor model in combination with the lumped elements of the measurement system. The methodology has been successfully applied to a wide range of transistor geometries. The thermal behavior has been analyzed and verified through DC measurements and low frequency small signal measurements.

Frequency domain thermal spreading impedance of Si-Ge HBTs has been investigated and the thermal impedance characterized by $1/\sqrt{p}$ behavior has been modeled on a simple way by implementing the generalized and normalized thermal impedance equation in compact HiCuM model. The thermal behavior with different thermo-electric networks developed up to date has been verified with our measurement results. In comparison with the conventional single pole network, the recursive network provides the best compromise among accuracy, number of model parameters and physical basement. Moreover, compact model simulation using the recursive network found to be in excellent agreement with measurements in time and frequency domain. The accuracy in time and frequency domain thermal modeling in combination with the simple parameter extraction methodology provides a better prediction of circuit performance due to thermal issues for the design engineers.

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Characterization of nanometric CMOS

In this chapter, we present the self-heating characterization of nano-metric CMOS technology through DC measurements, pulse measurements and, DC and pulse RF measurements.



3.1 Introduction

As the demand for high-capacity and high-speed wireless communication systems has increased, the use of millimeter-wave frequency bands has become an attractive solution [1]. The recent rapid progress in Si-CMOS technology has been targeted higher frequency applications. Large-diameter Si wafers of 300 mm make it possible to reduce the chip fabrication cost. In addition, the integration of the RF front-end and base band signal processors on a single chip will possibly lead to a breakthrough in wireless communication systems.

It has been reported in many literature that, drain current decreases due to self-heating effect. Lowering of drain current heating has been found to affect analog circuit design and to degrade their performance [2] where the influence of device self-heating on the frequency dependence of the admittance parameters has been discussed. The combined effect of increased temperature on carrier mobility, threshold voltage and saturation velocity generally leads to decreased drain current at large gate bias, sometime even making the drain current decrease with increasing drain bias, leading to a negative output conductance. Roy et al has pointed out [2] using simulation that self-heating effect in CMOS technology is important while evaluating small signal AC parameters and also figure of merits of interest in analog circuit design. In particular, while the low frequency voltage gain is degraded when significant DC self-heating effect exist (double-gate silicon-on-insulator at large gate and drain voltage), inclusion of self-heating predicts an increase of voltage gain when DC self-heating effect is low (bulk MOSFET and double-gate silicon-on-insulator with low gate and drain voltages). Tenbroek et al. [3] have highlighted the self-heating impact using measurements on simple amplifier stages, current mirrors, current output D/A converters, and ring oscillators fabricated in a 0.7 μm SOI CMOS process. It is shown that circuits which rely strongly on matching, such as the current mirrors or D/A converter, are significantly affected by self-heating and thermal coupling. Anomalies due to self-heating are also clearly visible in the small-signal characteristics of the amplifier stage. Self-heating effects are less significant for fast switching circuits. In ref. [1], Joshin et al presented the importance of including self-heating effect to properly model a PA module (100-mW output power at 24 GHz) developed in a 90nm CMOS technology. The model with the self-heating effect provides a better simulation of the measured P_{in} - P_{out} characteristics than the model without this effect.

As far as reliability is concerned, most of the degradation mechanisms are exponentially accelerated by the channel temperature, i.e., the internal temperature of the active device. The literature [4], [5] show the importance of channel temperature estimation in setting the operating limits and evaluating the lifetime of RF LDMOS devices where, for example, temperature-accelerated die cracking was observed as a result of power cycling. Consequently, accurate estimates of channel temperature are extremely important when it comes to modeling the device degradation rate under accelerated stress and extrapolating lifetimes to normal operating conditions [6]. Knowledge of channel temperature is also very important in device and circuit modeling and design, particularly for medium and high power transistors and circuits [7].

This work includes DC, pulse and RF electrical characterization of CMOS045 RF MOS transistors, analysis of the device self-heating and extraction of thermal parasitics. The self-heating of the different geometries of the transistors is described through DC and Pulse measurements. The thermal resistance (R_{TH}) has been extracted from the output characteristics measured at different ambient temperature (T_A) with the methodology proposed by Menozzi et al. [6]. The extraction methodology has been described in detail. In the second part of the work, we describe a new and simple method in order to obtain isothermal data from static $I_D - V_{DS}$ and $I_D - V_{GS}$ measurements which are performed at different T_A . The extracted isothermal data has been verified by pulse measurements. The third part of the work provides the DC and RF pulse measurements. These measurements are performed at different DC and RF pulse width configurations.

3.2 DC measurements and R_{TH} extraction

Thermal resistances R_{THS} of different geometries of transistor are extracted from output characteristics with the method described in [6]. Following the methodology, the extractions need,

- Static characteristics ($I_D - V_{DS}$) at different T_A
- A wide range of temperature, to make sure that drain current (I_D) varies linearly with T_A
- Thermally effected part at the saturation region of $I_D - V_{DS}$ characteristics needs to be chosen for accurate extraction

3.2.1 Output characteristics at different ambient temperatures

DC measurements have been performed at different ambient temperatures (T_A) and bias points, gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}), for wide range of the device geometries. The measurements are performed on wafer with Ground-Signal-Ground (GSG) probe configuration. A wide range of T_A (0 °C to 100 °C) is chosen in order to obtain the temperature dependency of drain currents (I_D). An output characteristic ($I_D - V_{DS}$) measured at $T_A = 25$ °C at different V_{GS} for the device with gate length of 270 nm is shown in *Figure 3-1*.

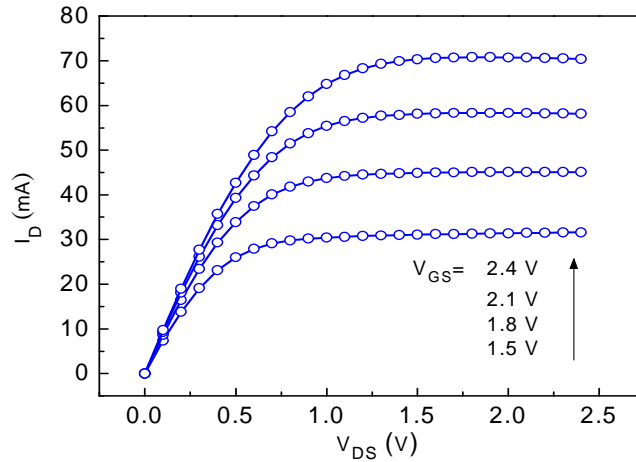


Figure 3-1: Measured output characteristic ($I_D - V_{DS}$) at different V_{GS} : $T_A = 25$ °C, Device gate length=270nm, Total gate width = 120 μ m (10 finger – 4 mos).

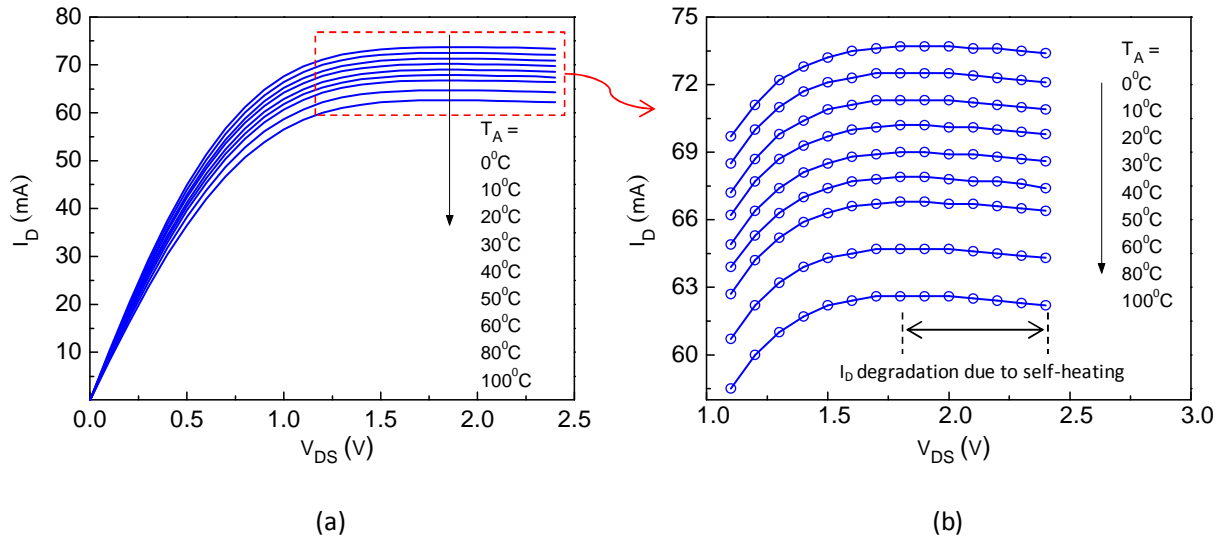


Figure 3-2: (a) Measured output characteristic ($I_D - V_{DS}$) at different T_A : $V_{GS} = 2.4$ V, Device gate length=270nm, Total gate width = 120 μ m (10 finger – 4 mos) (b) Zoom out plot of the selected region.

For the same device, the evolution of the $I_D - V_{DS}$ characteristic measured at $V_{GS} = 2.4V$ for different T_A is plotted in *Figure 3-2 (a)*. A selected region of these characteristics is zoomed out in *Figure 3-2 (b)* to point out that the I_D decreases nearly after $V_{DS} = 1.8 V$. This is due to the self-heating effect. The variation of I_D with temperature T_A has been found nearly linear between $0 ^\circ C$ and $100 ^\circ C$ for different V_{DS} and for $V_{GS} = 2.4V$ as shown in *Figure 3-3*. Also the I_D variation as a function of T_A for different transistor geometries and at $V_{GS} = 2.4 V$ and $V_{DS} = 2.4 V$ has been plotted in *Figure 3-4*. These measurement results are taken into account to extract the R_{TH} of the device as given in the next part.

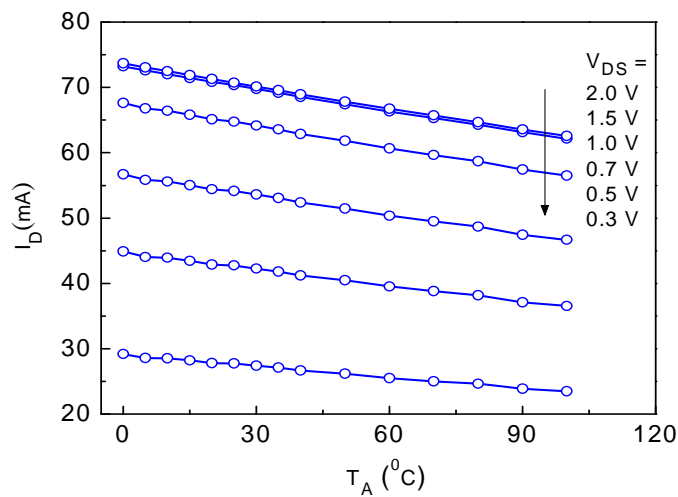


Figure 3-3: Measurement of I_D as a function of T_A for different V_{DS} : $V_{GS} = 2.4 V$, Device gate length=270nm, Total gate width = $120 \mu m$ (10 finger – 4 mos).

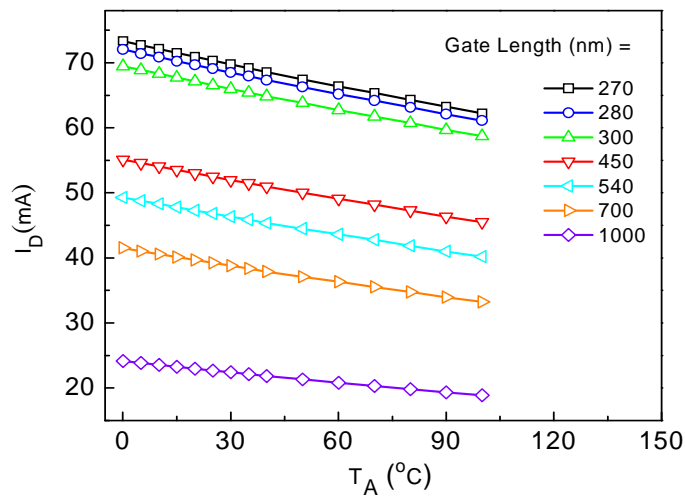


Figure 3-4: Measurement of I_D as a function of T_A for different geometries of device at $V_{GS} = 2.4 V$ and $V_{DS} = 2.4 V$, Device gate length=270nm, Total gate width = $120 \mu m$ (10 finger – 4 mos).

3.2.2 Extraction methodology

R_{TH} has been extracted from output characteristics measured at different T_A . The extraction method is based on Ref. [6], where the linear dependence of the drain current on T_A has been considered. The self-heating effect analysis consists in the determination of the device thermal resistance R_{TH} , which links the channel temperature (T_{CH}) to power dissipation (P_{diss}) through the simple equation,

$$T_{CH} = T_A + R_{TH} \cdot P_{diss} \quad \text{Eq. 3-1}$$

We consider a bias point in the saturation region of the output characteristic which is defined by an ambient temperature T_{A0} , gate-source voltage V_{GS0} , drain-source voltage V_{DS0} , drain current I_{D0} and a corresponding channel temperature T_{C0} . If the ambient temperature varies from T_{A0} to T_A , it is assumed that there is a linear dependence of the drain current on T_A as follows,

$$I_D(V_{DS0}, T_A) = I_{D0} \cdot (1 + h(T_A - T_{A0})) \quad \text{Eq. 3-2}$$

Therefore the parameter h is given by,

$$\frac{dI_D(V_{DS0}, T_A)}{dT_A} = I_{D0} \cdot h \quad \text{Eq. 3-3}$$

The parameter h can be calculated from the measured $I_D(V_{DS0}, T_A)$ vs. T_A plot.

Now, in the same T_A range, it is assumed that the drain current is a linear function of the channel temperature T_{CH} . Thus,

$$I_D(V_{DS0}, T_{CH}) = I_{D0} \cdot (1 + h'(T_{CH} - T_{C0})) \quad \text{Eq. 3-4}$$

The parameter h' can be calculated by differentiating Eq. 3-4 with respect to T_{CH} . The change in channel temperature ($T_{CH} - T_{C0}$) can be defined as,

$$T_{CH} - T_{C0} = T_A - T_{A0} + R_{TH} \cdot V_{DS0} \cdot (I_D(V_{DS0}, T_A) - I_{D0}) \quad \text{Eq. 3-5}$$

From Eq. 3-4 and Eq. 3-5,

$$I_D(V_{DS0}, T_{CH}) = I_{D0} \cdot (1 + h'(T_A - T_{A0} + R_{TH} \cdot V_{DS0} \cdot (I_D(V_{DS0}, T_A) - I_{D0}))) \quad \text{Eq. 3-6}$$

Finally, by differentiating Eq. 3-6 with respect to T_A and reformulating it, we can obtain,

$$\frac{dI_D(V_{DS0}, T_A)}{dT_A} = \frac{I_{D0} \cdot h'}{(1 - I_{D0} \cdot h' \cdot R_{TH} \cdot V_{DS0})} \quad \text{Eq. 3-7}$$

From Eq. 3-3 and Eq. 3-7,

$$\frac{1}{h} = \frac{1}{h'} - R_{TH} \cdot I_{D0} \cdot V_{DS0} \quad \text{Eq. 3-8}$$

Now, for $V_{DS} > V_{DS0}$, Eq. 3-8 can be written in more generalized form as follows,

$$\begin{aligned} \frac{1}{h} &= \frac{1}{h'} - R_{TH} \cdot I_D(V_{DS}, T_{A0}) \cdot V_{DS} \\ &= \frac{1}{h'} - R_{TH} \cdot P_{diss}(V_{DS}, T_{A0}) \end{aligned} \quad \text{Eq. 3-9}$$

Equation Eq. 3-9 gives a linear behaviour of $1/h$ as a function of P_{diss} . The slope of this linear equation gives R_{TH} .

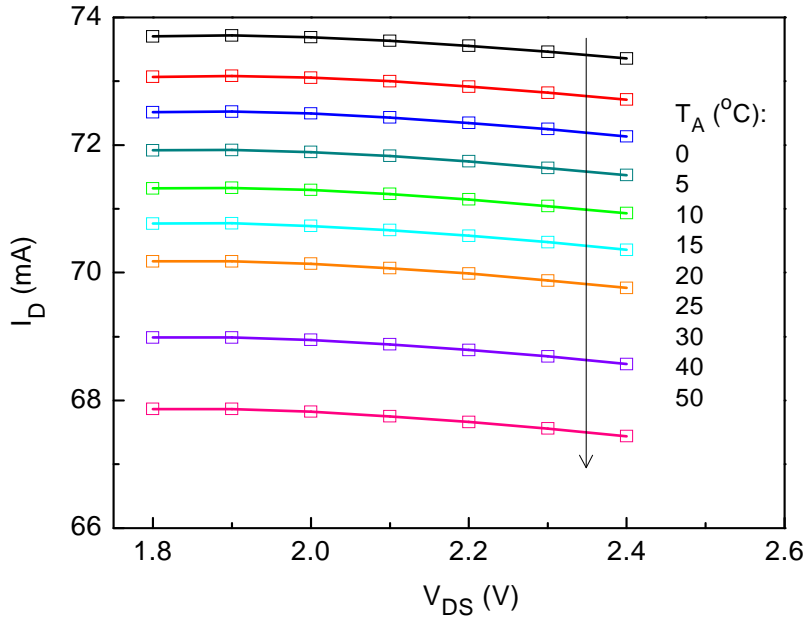


Figure 3-5: The selected region for R_{TH} extraction from measurements of I_D as a function of T_A for different V_{DS} : $V_{GS} = 2.4$ V, Device gate length=270nm, Total gate width = 120 μm (10 finger – 4 mos).

The selected bias point and temperature range used for the R_{TH} extraction is shown in Figure 3-5 for the device with a gate length of 270 nm (from Figure 3-2 (a) and (b)). Figure 3-6

shows the linear variation of I_D as a function of T_A for different V_{DS} . The slope ($dI_D(V_{DS0}, T_A)/dT_A$) of each curve is calculated with the best fit interpolation.

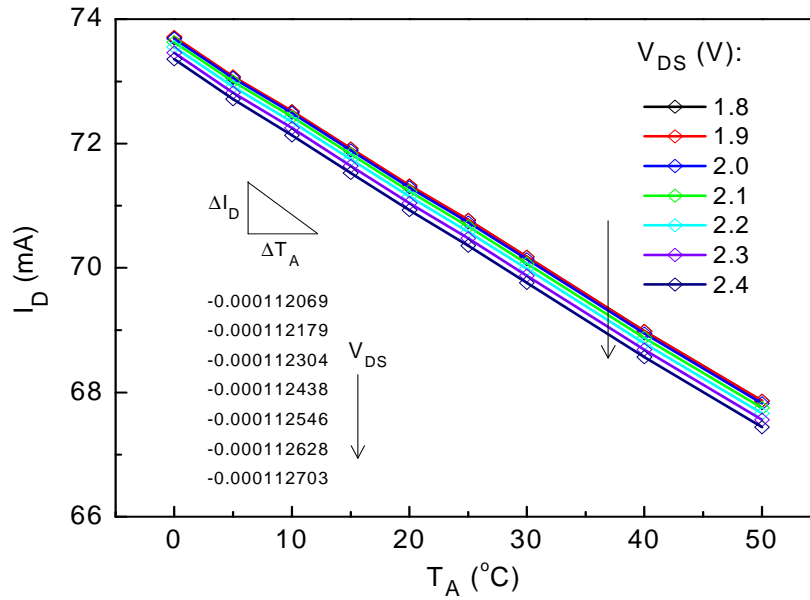


Figure 3-6: Measurements of I_D (symbols) as a function of T_A for different V_{DS} and best fit interpolation (lines): $V_{GS} = 2.4$ V, Device gate length=270nm, Total gate width = 120 μm (10 finger – 4 mos).

TABLE3-I:

Parameter h calculation

V_{DS} (V)	I_{D0} (mA) at $T_A = 0^\circ\text{C}$	$P_{\text{diss}}(V_{DS}, T_{A0})$ (W)	Best fit slope	1/h
1.8	73.705	0.132669	-0.000112069	-657.676
1.9	73.717	0.140062	-0.000112179	-657.135
2	73.69	0.14738	-0.000112304	-656.164
2.1	73.634	0.154631	-0.000112438	-654.888
2.2	73.558	0.161828	-0.000112546	-653.584
2.3	73.465	0.16897	-0.000112628	-652.279
2.4	73.355	0.176052	-0.000112703	-650.869

Therefore, the parameter h can be calculated using Eq. 3-3 as given in TABLE3-I:

- For a constant V_{GS} , the V_{DS} bias range is chosen (self-heating effected region)
- At these V_{DS} bias region, power dissipation P_{diss} is calculated taking I_D at 0°C

- $dI_D(V_{DS0}, T_A)/dT_A$ is calculated from *Figure 3-6*
- The parameter h is calculated with the following equation,

$$h = \frac{\frac{dI_D(V_{DS0}, T_A)}{dT_A}}{I_{D0}} \quad \text{Eq. 3-10}$$

According to *Eq. 3-9*, the slope of the $1/h$ vs. P_{diss} curve is the measure of R_{TH} . The parameter $(1/h)$ is calculated for different bias conditions, especially from the output characteristic of different V_{GS} .

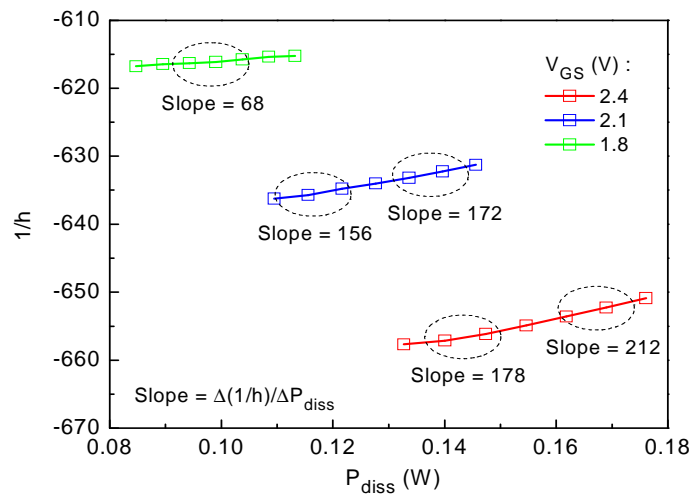


Figure 3-7: $1/h$ vs. P_{diss} for different V_{GS} - extracted from measurements; the slope is calculated from best fit interpolation, Device gate length=270nm, Total gate width = 120 μm (10 finger – 4 mos).

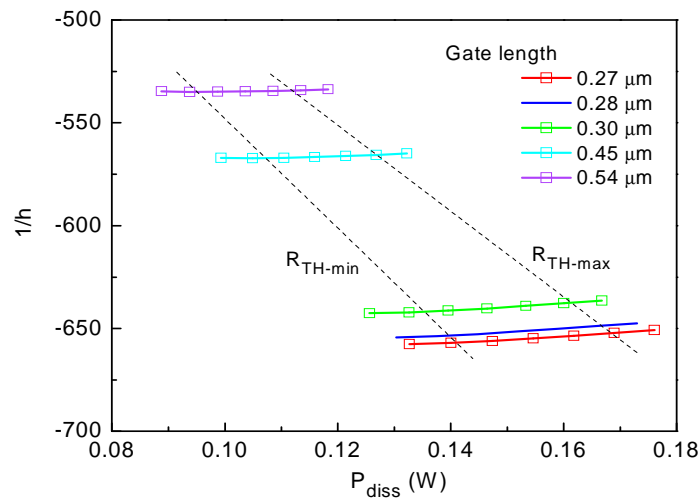


Figure 3-8: $1/h$ vs. P_{diss} for different geometries of device - extracted from measurements; the slope is calculated from best fit interpolation. Total gate width = 120 μm (10 finger – 4 mos).

In *Figure 3-7*, parameter $1/h$ vs. P_{diss} for different V_{GS} and different geometries of transistor is shown respectively. The slope is calculated from the best fit interpolation at different region. The curves are not perfectly linear, because the self-heating depends on power dissipation. At high power density region maximum and low power density region minimum slope is found. The extracted slope at low V_{GS} (1.8 V or below) is very small due to low self-heating. The lower thermal effect can give less accuracy in parameter extraction. Therefore, we consider V_{GS} value 2.1 and 2.4 V for further extraction.

3.2.3 R_{TH} with device gate length

In *Figure 3-8*, $1/h$ vs. P_{diss} at $V_{\text{GS}} = 2.4$ V for different dimension of transistors is shown. The higher power density region gives maximum R_{TH} ($R_{\text{TH-max}}$) where minimum R_{TH} ($R_{\text{TH-min}}$) is calculated from low power density region. R_{TH} s for different dimensions of device are extracted. *Figure 3-9* shows decreasing nature of R_{TH} s with increasing gate length L_{Gate} . Now using these R_{TH} values, temperature rise of the channel (ΔT_{CH}) can be calculated at different bias point [$\Delta T_{\text{CH}} = R_{\text{TH}} * (I_{\text{D}}V_{\text{DS}} + I_{\text{G}}V_{\text{GS}}$)]. For a smaller device with $L_{\text{Gate}} = 260$ nm, $\Delta T_{\text{CH}} = 35$ K and for a larger device with $L_{\text{Gate}} = 1000$ nm, $\Delta T_{\text{CH}} = 1.5$ K at maximum operating point $V_{\text{GS}} = 2.5$ V and $V_{\text{DS}} = 2.5$ V.

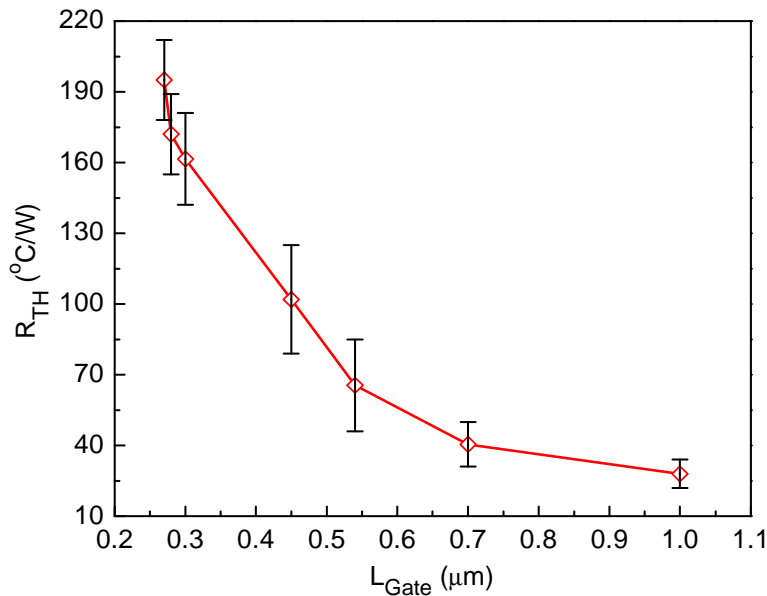


Figure 3-9: Extracted R_{TH} s for different geometries of transistors – number of gate figure = 10 and total gate width = 120 μm .

3.3 Isothermal data extraction

In this part we present a new methodology to extract isothermal data from measured steady state characteristic at different T_A . In particular, this is an improved and simpler method compared to other as proposed by Fregonese et al. in [8]. In order to develop a simplified theoretical formulation, we assume that the variation of I_D with T_{CH} is linear. Also this is verified in previous DC measurements that I_D is liner in wide T_A range. The extractions need,

- $I_D - V_{DS}$ and $I_D - V_{GS}$ characteristics at different T_A
- A wide range of temperature for the accuracy in extraction
- An accurate R_{TH} value

3.3.1 Extraction methodology

In the previous measurements, it is found that the variation of I_D is linear at wide T_A range. During the transistor operation, the device temperature varies due to the power dissipation P_{diss} . The change in temperature can be described as,

$$\Delta T = T_{CH} - T_A = R_{TH} \cdot I_D(V_{DS}, V_{GS}, T_A) \cdot V_{DS} \tag{Eq. 3-11}$$

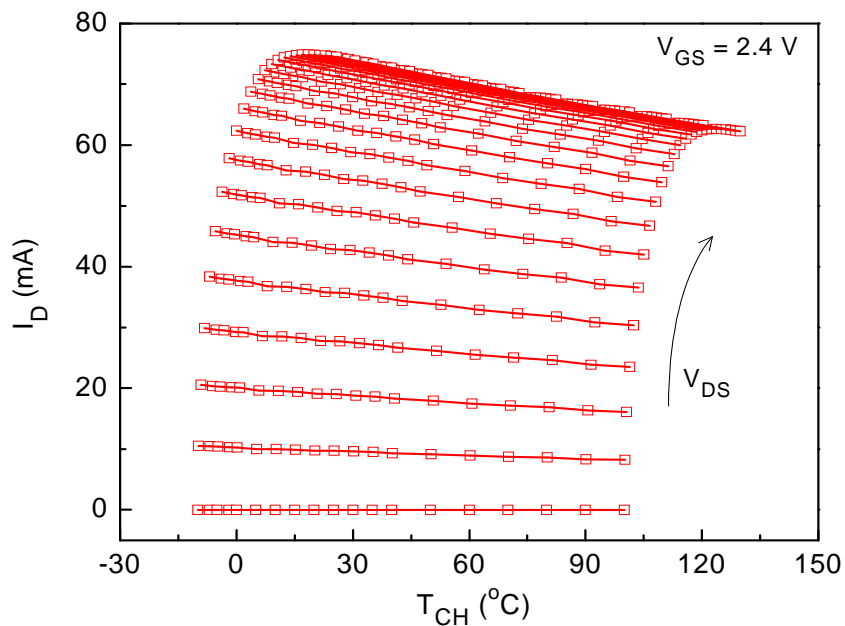


Figure 3-10: The variation of I_D with channel temperature T_{CH} at different V_{DS} (calculated from $I_D - V_{DS}$ characteristics at different T_A); constant $V_{GS} = 2.4$ V.

Therefore, the channel temperature is given by,

$$T_{CH} = T_A + R_{TH} \cdot P_{diss} = T_A + R_{TH} \cdot I_D(V_{DS}, V_{GS}, T_A) \cdot V_{DS} \quad Eq. 3-12$$

At different T_A value, T_{CH} can be calculated using the previous output characteristic measurements.

In *Figure 3-10*, I_D vs. T_{CH} is plotted for different V_{DS} and at $V_{GS} = 2.4V$. This data is calculated from $I_D - V_{DS}$ characteristics at different T_A using *Eq. 3-12*. The I_D variation with T_{CH} for different V_{GS} is shown in *Figure 3-11* which is calculated from $I_D - V_{GS}$ characteristics at different T_A .

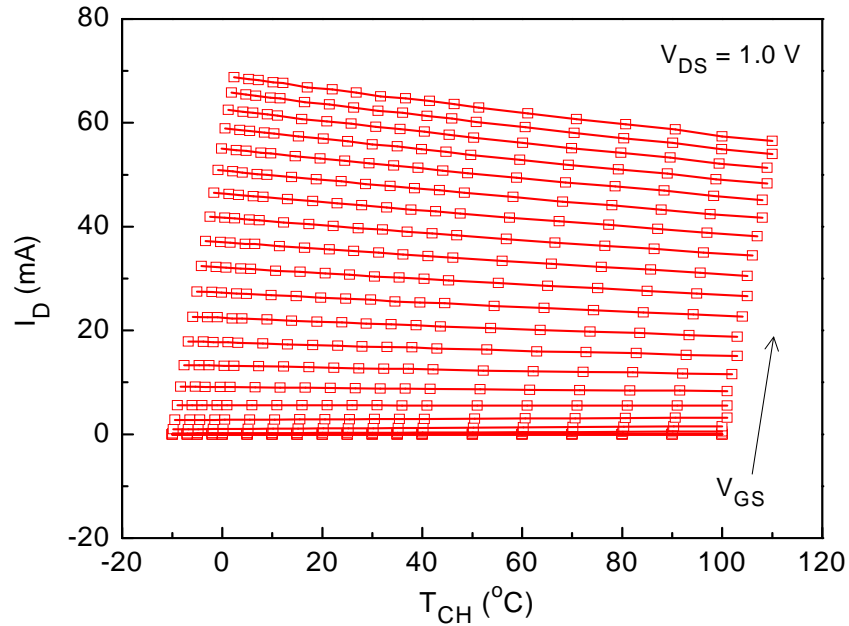


Figure 3-11: The variation of I_D with channel temperature T_{CH} at different V_{DS} (calculated from $I_D - V_{DS}$ characteristics at different T_A); constant $V_{GS} = 2.4 V$.

It can be seen from the above plot that, I_{DS} are linear with T_{CH} . Therefore, this can be represented by,

$$I_{D-DC}(V_{DS}, V_{GS}, T_A) = -\frac{\Delta I_D(V_{DS}, V_{GS}, T_A)}{\Delta T_{CH}} T_{CH} + I_D^0(V_{DS}, V_{GS}, T_A = T_{CH}) \quad Eq. 3-13$$

Here, I_{D-DC} is steady state drain current, I_D^0 is the drain current when $T_A = T_{CH}$, i.e. $\Delta T = 0$. Hence, this is the isothermal current for a constant V_{GS} and V_{DS} .

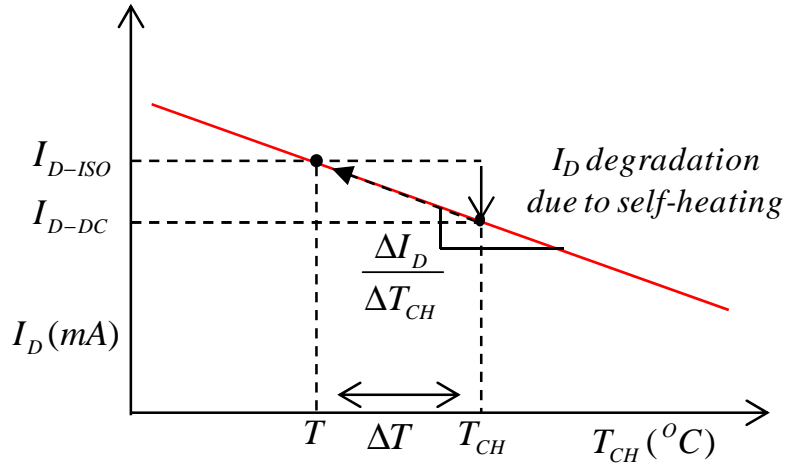


Figure 3-12: Extraction of isothermal drain current (I_{D-ISO}) from steady state drain current (I_{D-DC}) vs. channel temperature (T_{CH}) curve.

At any value of V_{GS} and V_{DS} , the isothermal drain current (I_{D-ISO}), at any desire temperature T , can be described by,

$$I_{D-ISO}(V_{DS}, V_{GS}, \Delta T = 0) = -\frac{\Delta I_D(V_{DS}, V_{GS}, T_A)}{\Delta T_{CH}} T + I_{D-DC}^0(V_{DS}, V_{GS}, T_A = T_{CH}) \quad \text{Eq. 3-14}$$

From, Eq. 3-13 and Eq. 3-14,

$$I_{D-ISO}(V_{DS}, V_{GS}, \Delta T = 0) = I_{D-DC}(V_{DS}, V_{GS}, T_A) - \frac{\Delta I_D(V_{DS}, V_{GS}, T_A)}{\Delta T_{CH}} (T - T_{CH}) \quad \text{Eq. 3-15}$$

Using Eq. 3-15, the corresponding isothermal characteristic of $I_D - V_{DS}$ or $I_D - V_{GS}$ characteristics can be extracted.

3.3.2 Isothermal characteristics

The extracted isothermal data are compared with DC measurement as follows: (i) Figure 3-13: output characteristic $I_D - V_{DS}$ for different V_{GS} , at temperature $T = 30^\circ\text{C}$. (ii) Figure 3-14: output characteristic $I_D - V_{DS}$ at temperature T , $V_{GS} = 2.4\text{ V}$ and (iii) Figure 3-15: $I_D - V_{GS}$ characteristic at different T_A .

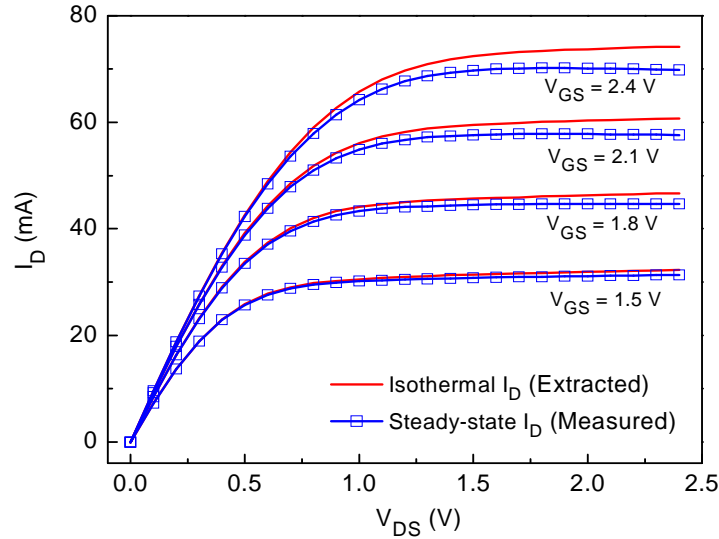


Figure 3-13: Comparison between extracted isothermal data and measured steady state characteristic at different V_{GS} – transistors gate length = 270 nm. Total gate width = 120 μm (10 finger – 4 mos).

Following the figures, at low power dissipation no difference is observed. At larger bias condition, a small difference can be observed between isothermal and DC measurement due to small R_{TH} value. This extraction method has also been applied for different ambient temperature. Finally, the extraction method demonstrates moderate effects of self-heating even at high V_{GS}/V_{DS} biases.

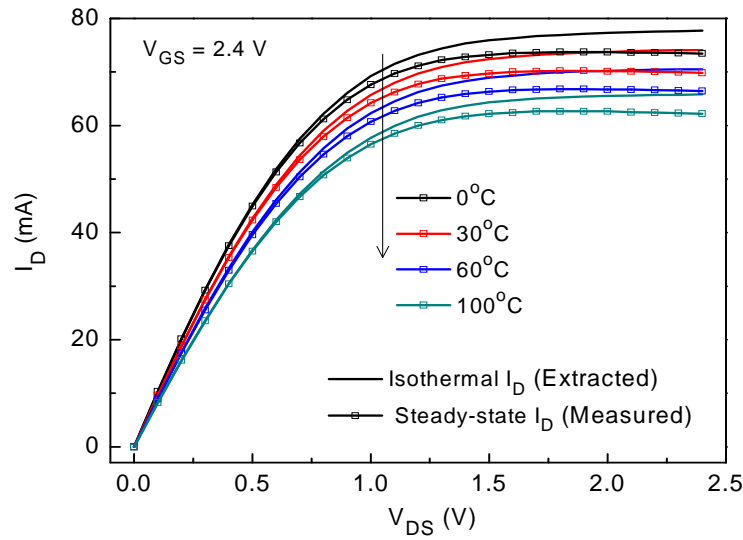


Figure 3-14: Comparison between extracted isothermal data and measured steady state characteristic at different T_A – transistors gate length = 270 nm, Total gate width = 120 μm (10 finger – 4 mos).

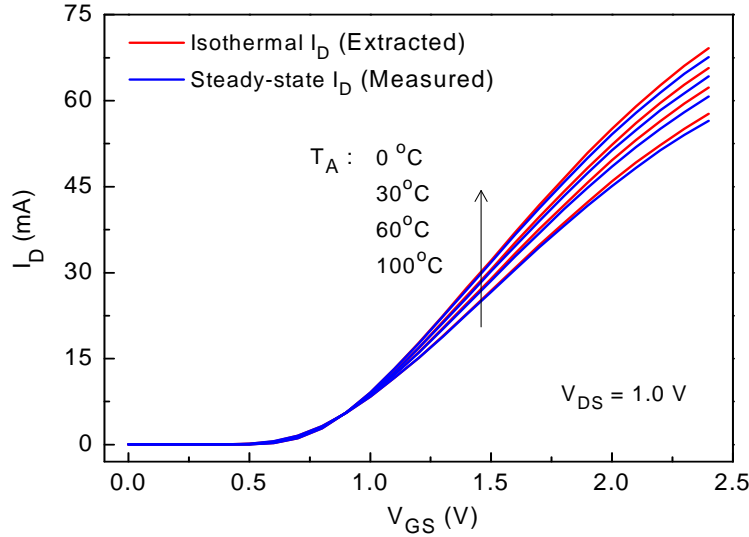


Figure 3-15: Comparison between extracted isothermal data and measured $I_D - V_{GS}$ characteristic at different T_A – transistors gate length = 270 nm, Total gate width = 120 μm (10 finger – 4 mos).

3.4 Pulse measurements

The measurements have been performed in order to evaluate the self-heating effect of CMOS045 RF MOS transistors. Pulse measurements are carried out with different experimental setup and similar results have been found. In this work, we describe measurements with two setup, (i) MC2 technology APMS pulse generator [9] and (ii) KEITHLEY 4200SCS pulse measurement setup with PIVA option and with 4225 option [10].

3.4.1 Measurements with MC2 Technology APMS

The measurements are carried out over pulses applied at gate and drain terminals simultaneously which show how transient self-heating affects the time response of drain current variation. The pulse measurement scheme is based on the transient measurements of I_D . These measurements have been carried out on wafer with GSG (Ground – Signal – Ground) probe configuration at room temperature (300 K). Gate and drain pulse are generated by MC2 Technology APMS LPM1 and HPM1 pulse generators (Figure 2-10; chapter - 2) respectively. The Agilent 6633B system DC power supply (SMU gate and drain) are used to set the quiescent and bias points for both Base and Collector terminals. The pulses are applied to the device terminals through the bias TEE (Agilent Bias Network 11612A OPT OO1 - 400 MHz to 26.5

GHz and 100 V DC - 2.0 A Max). The experimental setup has been calibrated accurately before measurements.

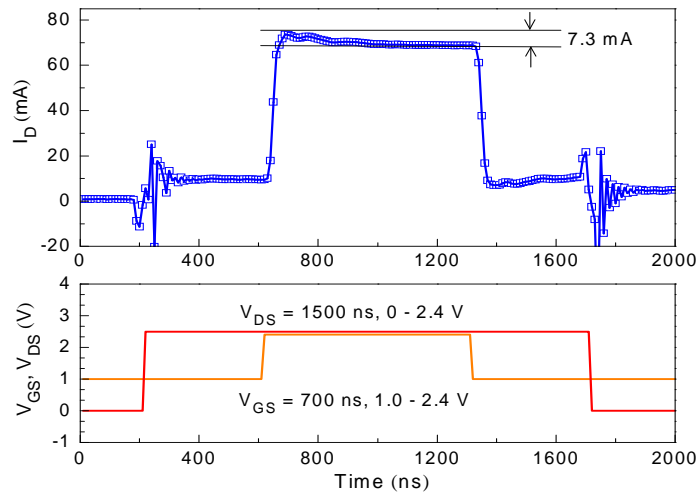


Figure 3-16: Transient I_D measurements: applied pulses – $V_{DS} = 1500$ ns with 0 – 2.6 V, $V_{GS} = 700$ ns, 1.0 – 2.4 V, transistors gate length = 260 nm, Total gate width = 120 μm (10 finger – 4 mos).

A time domain measurement result is shown in Figure 3-16. The applied pulses are $V_{DS} = 1500$ ns with 0 – 2.6 V, $V_{GS} = 700$ ns, 1.0 – 2.4 V. It is observed that, nearly 7.3 mA I_D decreases between 200 ns and 700 ns pulse time.

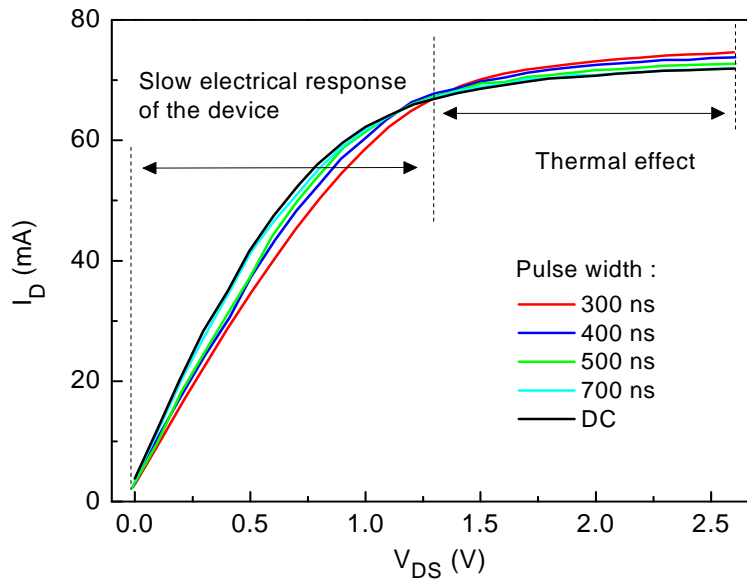


Figure 3-17: Output ($I_D - V_{DS}$) characteristics at constant V_{GS} (2.5 V) - comparison between DC and pulse (different pulse width) measurements. Gate length = 260 nm, Total gate width = 120 μm (10 finger – 4 mos).

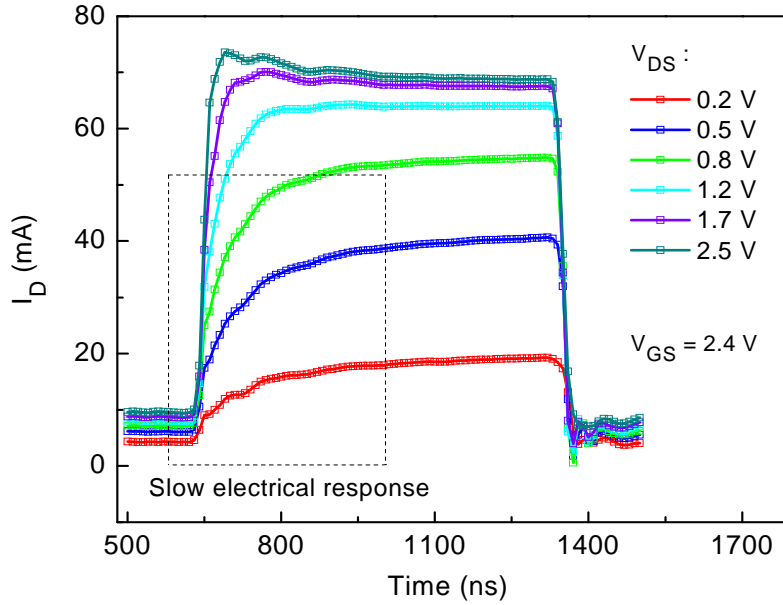


Figure 3-18: Transient I_{DS} at different V_{DS} : applied pulses – $V_{DS} = 1500$ ns, $V_{GS} = 700$ ns, 1.0 – 2.4 V, transistors gate length = 260 nm, Total gate width = 120 μ m (10 finger – 4 mos).

In *Figure 3-17*, pulse measurements for different pulse width are compared with DC measurements. At drain terminal, a 1500 ns pulse is applied where different pulse widths between 200 to 700 ns are applied at gate terminal. It can be seen from the figure that, at higher V_{DS} , I_D degradation occurs with increase in pulse width, which is due to self-heating effect. At 700 ns pulse time device reaches to steady state temperature, therefore, I_D is similar as DC measurements.

At low V_{DS} measurement results are different. Some unexpected variations with pulse width are found. At very small pulse width, I_D is significantly lower than DC value. This may be due to oxide and Si substrate interface traps or slow electrical response of the device. In order to investigate the different I_D behaviour at low bias region, different time domain measurements are performed. In *Figure 3-18*, time domain pulse profiles for different V_{DS} bias are shown. The applied pulses are, $V_{DS} = 1500$ ns, fixed $V_{GS} = 700$ ns, 1.0 – 2.4 V. It can be observed from the *Figure 3-18*, that at low V_{DS} transient behavior is dominated by electrical effects (electrical response of the device and/or traps effects) and thermal effects are negligible where at large V_{DS} transient behavior is dominated by thermal effects (faster electrical transient behavior).

3.4.2 Measurements with KEITHLEY 4200SCS

A simplified block diagram of the experimental setup (KEITHLEY 4200SCS PIVA) is given in *Figure 3-19 (a)*. The pulses are applied through the Gate terminal of the device where the Drain is kept at a constant bias. The Drain current is measured at 50Ω resistance. The 4200PIVA module generates the pulses between 40 ns and 150 ns pulse width range with 10 ns resolution. A complete circuit diagram is given in *Figure 3-19 (b)* [10].

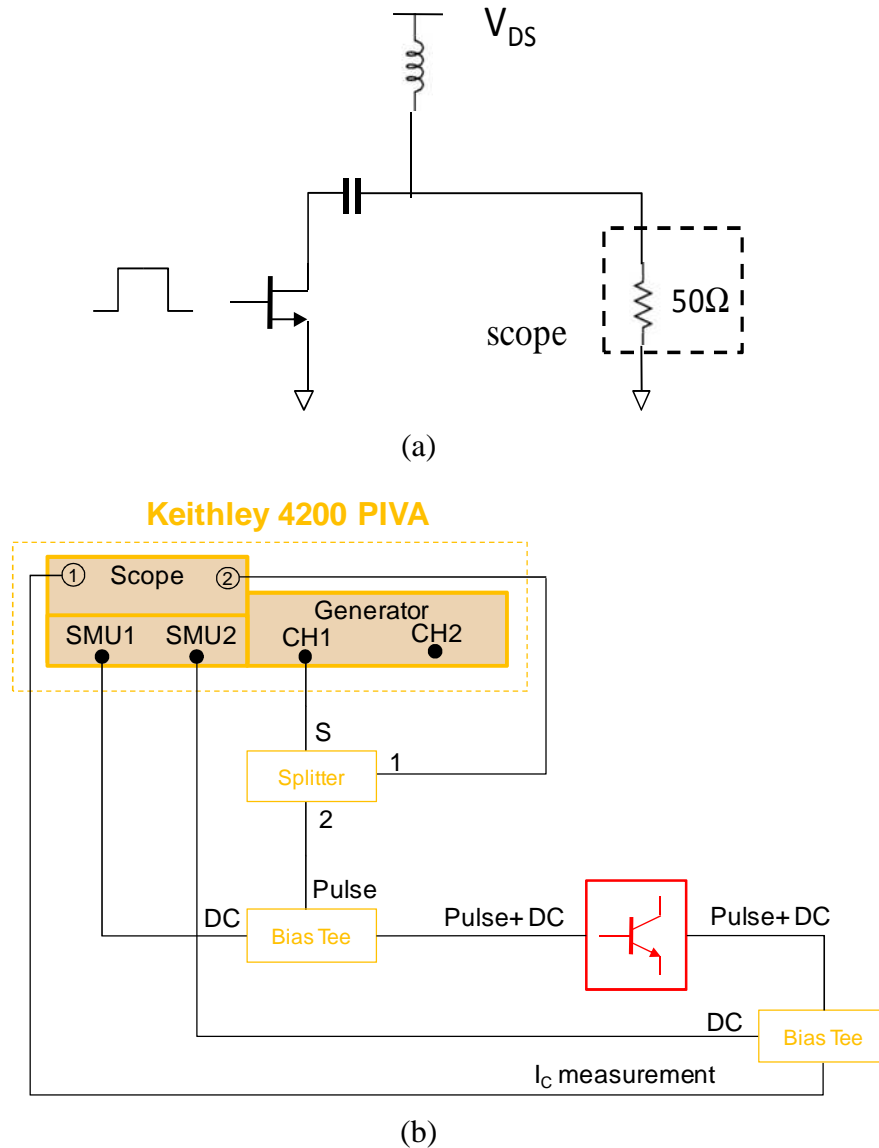


Figure 3-19: (a) Simplified block diagram and (b) complete circuit diagram of DC pulse measurements system (KEITHLEY 4200SCS).

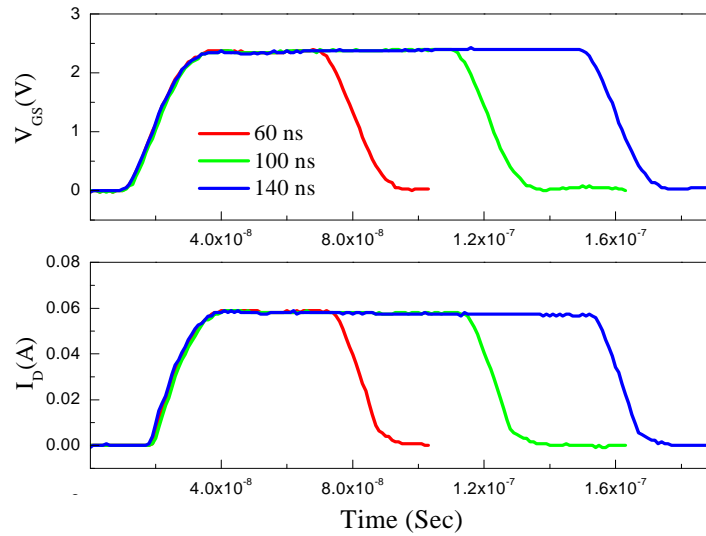


Figure 3-20: Gate voltage pulses applied to the transistor (above) and Measured Drain current pulse profile (below) for different pulse widths (60, 100, 140 ns), Device gate length=450nm, Total gate width = 120 μm (10 finger – 4 mos).

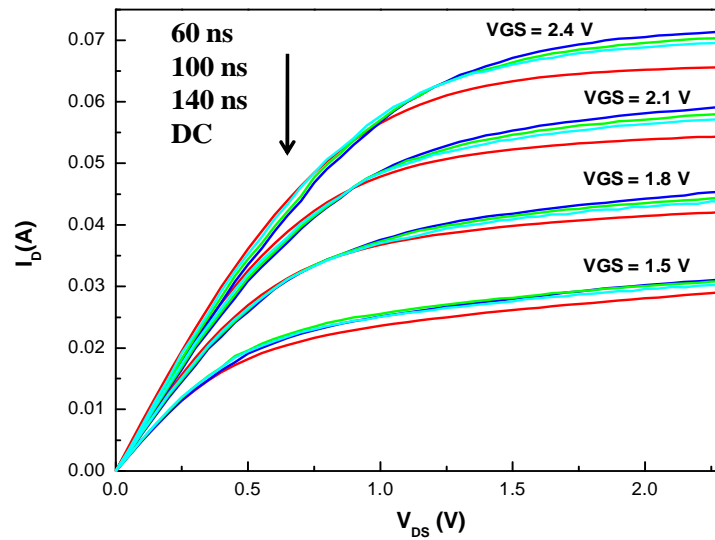


Figure 3-21: $I_D - V_{DS}$ characteristics at constant V_{GS} : Comparison between pulsed and DC conditions, transistor gate length = 300 nm, Total gate width = 120 μm (10 finger – 4 mos), $T_A = 25^\circ\text{C}$.

Figure 3-20 gives the applied Gate voltage pulse (V_{GS}) for a constant 2.5 V drain bias and for three different pulses width 60, 100 and 140ns. This figure shows that, the test bench is properly calibrated and is able to perform very short pulse down to 60ns. The resulting measured Drain current pulse profile (I_D) is also given in Figure 3-20. It is observed that the Drain currents are decreasing as the pulse width is increasing which is due to the self-heating. Complete pulsed output characteristics have been compared with DC characteristics for the device with Gate

length equal to 300 nm as given in *Figure 3-21*. As the pulse width is increasing, the I_D decreases due to self-heating and it reaches its minimum value at DC condition.

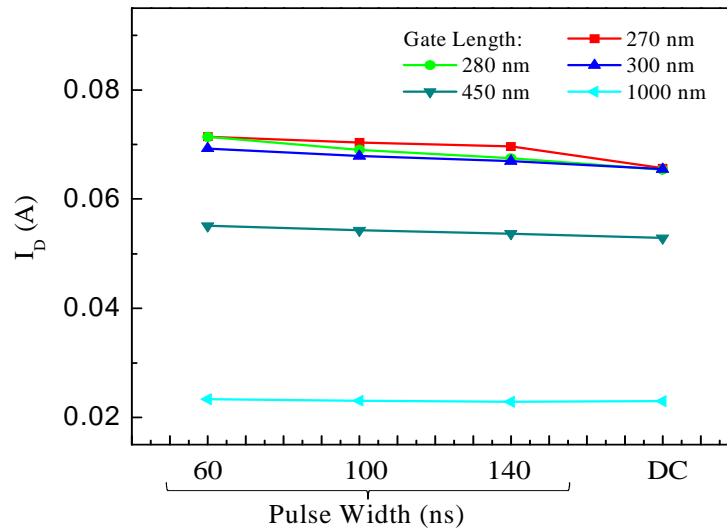


Figure 3-22: Pulse DC and DC measurements for different pulse widths of transistors with different gate lengths, Total gate width = 120 μ m (10 finger – 4 mos).

A summary of pulse measurements and DC measurements at room temperature for different geometries of MOSFETs is given in *Figure 3-22*. The measurements are performed at 60, 100 and 140 ns Gate voltage pulse width at $V_{GS} = 2.4V$ $V_{DS} = 2.3V$. It is observed from the figure that, for the smallest geometry (270nm) of the device, the Drain current decreases towards the DC value as the pulse width increases while for the longest device (1000nm) the variation of drain current is nearly null. The current variation in the short gate length devices is due to the self-heating effect. This effect is significant from 270nm to 450nm and can be neglected above. This self-heating effect in short gate length device is more pronounced for two reasons: i) The current density is higher in transistors with small gate length; ii) The decrease of the Gate length brings the source and the drain more closely, increasing the thermal resistance of the device.

3.5 Isothermal data vs. pulse measurements

In this section we compare the extracted isothermal data with pulse measurements and DC measurements as follows: (i) in *Figure 3-23*: output characteristic $I_D - V_{DS}$ for $V_{GS} = 2.4 V$, at temperature $T = 30$ °C and (ii) *Figure 3-24*: $I_D - V_{GS}$ for $V_{DS} = 1.0 V$, at temperature $T = 30$ °C. The 150 ns pulse measurement data is lower than the isothermal data. Therefore, 150 ns

pulse width is not sufficient to reach isothermal characteristics. At smaller bias pulsed I_D is lower than the DC value due to slow electrical performances of the device.

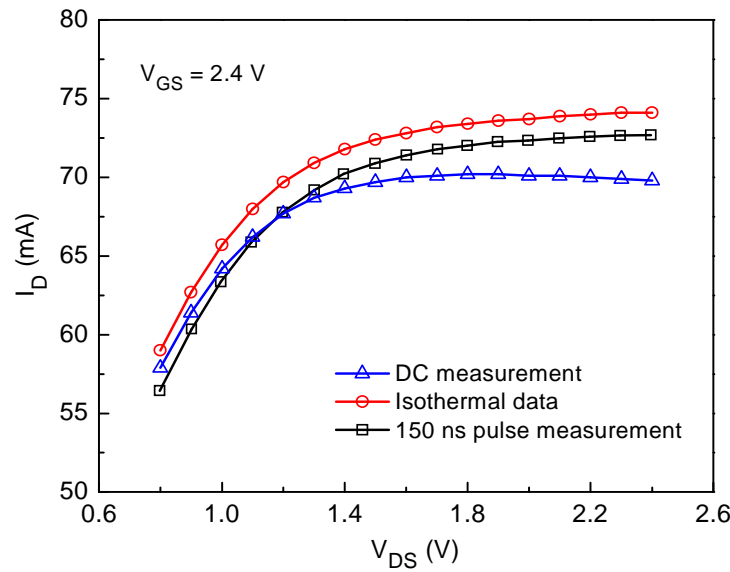


Figure 3-23: $I_D - V_{DS}$ characteristic at $V_{GS} = 2.4$ V - Comparison between extracted isothermal data and pulse measurement; transistor gate length $L_G = 270$ nm, Total gate width = $120 \mu\text{m}$ (10 finger – 4 mos).

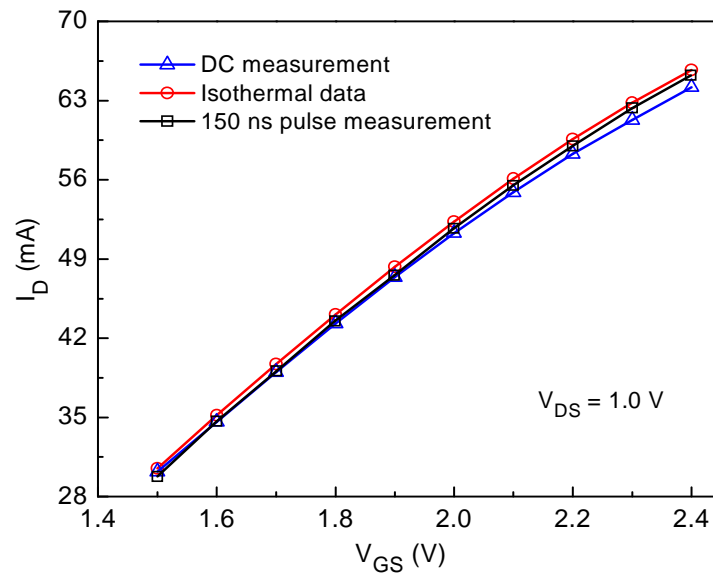


Figure 3-24: $I_D - V_{GS}$ at $V_{DS} = 1.0$ V - Comparison between extracted isothermal data and pulse measurement; transistor gate length = 270 nm, Total gate width = $120 \mu\text{m}$ (10 finger – 4 mos).

3.1 DC and RF pulse measurement

The experimental setup for DC and RF pulse measurements is shown in Figure 3-25.

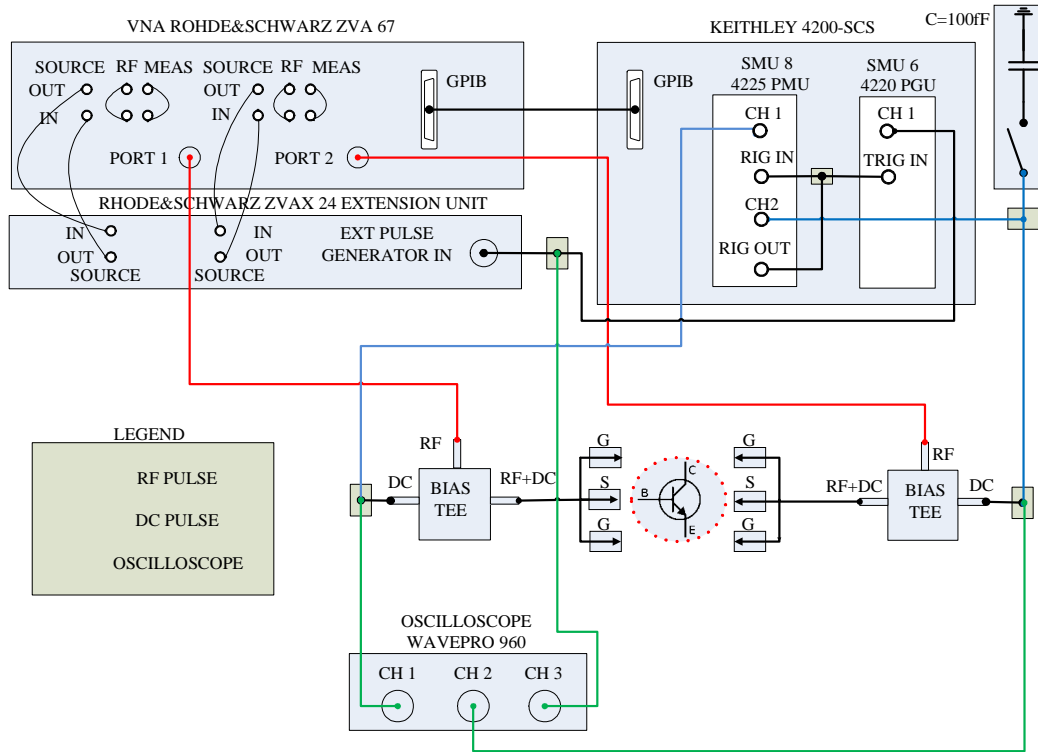


Figure 3-25: DC and RF pulse measurements setup: KEITHLEY 4200-SCS DC pulse generator with Rhode & Schwartz VNA.

In comparison to previous Keithley pulse setup; the 4200PIVA module has been replaced by the 4225 module in order to have more flexibility in duty cycle and pulse width conditions. The first step of system evaluation was to study the influence of bias tee to apply the DC pulse and RF pulse simultaneously. The bias tee has been selected to have a sufficient bandwidth of frequency to avoid deformation of DC pulse. Different tests have been performed to ensure the shape of the pulse: i) scope measurements have been performed before and after bias tee; ii) a complete pulse DC analysis of a transistor has been performed with and without bias tee.

3.1.1 DC and RF pulse synchronization

The second step for pulsed RF characterisation is the evaluation of the synchronisation between DC pulse and RF pulse. The network analyser is synchronised on the DC pulse bench using a trigger. A program has been developed to regulate the position of the RF pulse inside the DC pulse through triggering. The *Figure 3-26* shows an example of scope measurement of a synchronised DC and RF pulse measured at the output of the bias tee. The DC pulse is about

200ns while the RF pulse is about 50ns and is voluntarily delayed of 100ns. For measurement purpose, the RF power is about 0dBm.

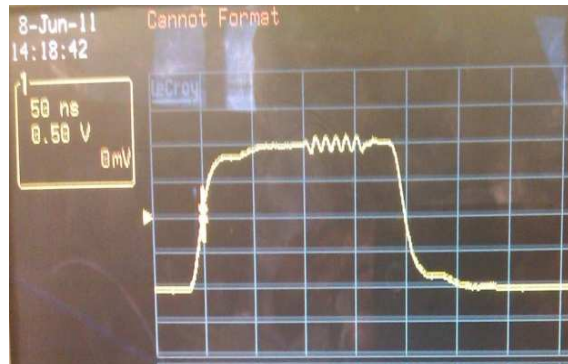


Figure 3-26: DC and RF Pulse signal synchronisation measured at the output of the bias tee.

3.1.2 Transit frequency f_T measurements

We performed DC and RF pulse measurement with DC pulse width from 150 ns to 1000 ns for V_G pulse. The corresponding RF pulse changes from 50 ns to 300 ns. (The RF pulse width is synchronized and included in DC pulse width). The f_T vs V_{GS} is shown in Figure 3-27. At Low V_{DS} : Thermal effects are negligible / Transit frequency is over-imposed. At Large V_{DS} : small thermal effects showing very small variation of transit frequency within this pulse width range.

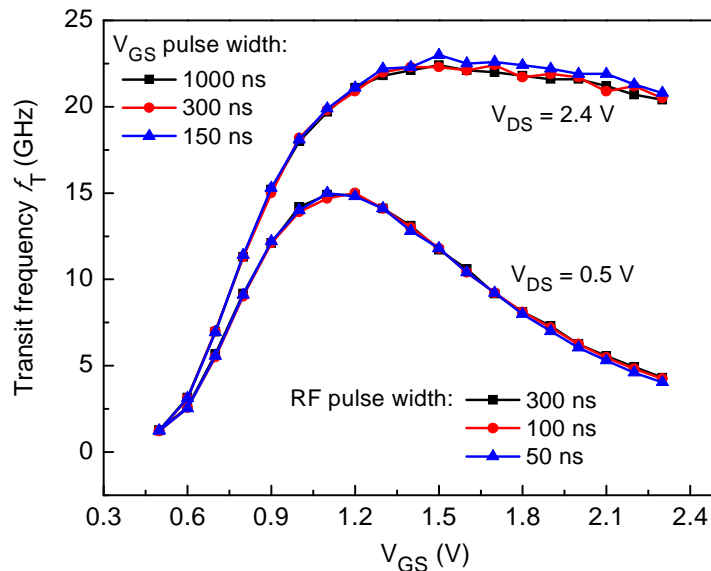


Figure 3-27: Transit frequency at different DC pulse width (150, 300 and 1000 ns) and corresponding RF pulse width (50, 100 and 300 ns), transistor gate length = 270 nm, Total gate width = 120 μm (10 finger - 4 mos), $T_A = 27^\circ\text{C}$.

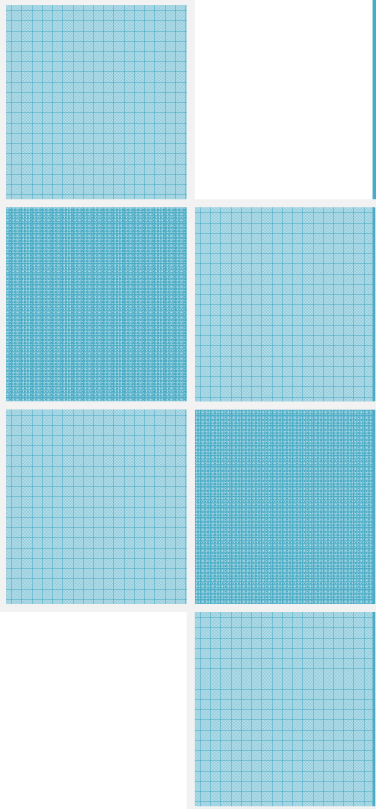
3.2 Conclusion

In this work, DC measurements are performed at different ambient temperatures. I_D Degradation due to self heating is very small in these devices. R_{THS} of different geometries of transistors are extracted. The extraction methodology has been described in detail. Due to smaller R_{TH} value, the channel temperature rise is small within maximum bias region. A new and simple methodology has been presented in order to extract isothermal data from I_D - V_{DS} and I_D - V_{GS} characteristic measured at different ambient temperature. The isothermal data has been verified by pulse measurements. It has been seen that, 150 ns pulse width is not sufficient to reach isothermal characteristics. Device electrical performances and thermal behavior (depending on bias region) have been evaluated through pulse measurements. DC and RF pulse characterization has been carried out at different DC and RF pulse width. Due to smaller R_{TH} value of this device, no difference is found in the applied pulse width range. Therefore, some complimentary measurements need to be performed. Finally, sensitivity of this device to self-heating found to be small from the different characterizations.

3.3 Reference:

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3D thermal TCAD simulations

Three dimensional thermal TCAD simulations are performed in order to investigate the transient and the dynamic behavior of the device temperature in dependence of the device architecture and material properties. The structure of the transistors is same as the measured one, submicron SiGe:C BiCMOS HBTs.



4.1 Introduction

The advancement of high speed technology is based on the implementation of trench isolated architecture like shallow trench, deep trench etc. The deep trench isolation insulates electrically the neighboring transistors and substrate in order to reduce the parasitic capacitance, substrate noise and cross-talk [1–3]. On the other hand, the introduction of shallow trench and deep trench restricts the lateral flow of heat flux and directs towards vertical. Due to poor thermal conductivity of trench wall, the heat flow from heat source is mostly confined within trench-enclosed region before spreading into substrate and thereby increasing the temperature of active device. The affect of thermal dissipation introducing the trench wall in a conventional substrate, presented by Walkey et al. in [5], [6] through 2D finite element thermal simulation, gives a considerable change in device temperature. Furthermore, the isothermal contours of heat diffusion are significantly different between trench isolated and the conventional structure. This simulation result are also verified by measurements that show a 65% increase in R_{TH} for with-trench compare to without-trench for $0.35 \times 10 \mu\text{m}^2$ device of Nortel's 35GHz f_T , 50GHz f_{Max} process technology. Also, a rigorous analysis for device temperature and thermal resistance (R_{TH}) depending on trench architecture is presented by Walkey et al. [6], [7] through an analytical model verified by 3D numerical simulations and measurements. The thermal behavior of devices fabricated in different isolation technologies like STI, DTI and SOI is compared by Haralson et al. [8] through a 2D device simulation. Also a precise analysis for device structure dependent R_{TH} is given by Marano et al. for trench isolated bipolar device [4] and also fabricated on SOI substrate [9]. The most of the literatures focus on the investigations of R_{TH} depending on the device architecture and material properties. However, in this work, transient simulations are performed in order to extract R_{TH} as well as C_{TH} . Also a new simulation methodology has been presented to extract frequency domain Z_{TH} . A detailed description of the methodology is given. Thermal simulations are performed for trench isolated device structures of a submicron SiGe:C BiCMOS technology with f_T and f_{max} of 230 GHz and 290 GHz, respectively. In first attempt, a simplified device structure without backend layers is simulated. In order to explore precisely the influence of different backend layers with metallization on device thermal behavior, a complete structure has been developed. Thermal modeling has been performed using different electro-thermal network and extracted parameters are compared among different device geometries.

4.2 Thermal simulation

From the microscopic point of view, the energy is given up by the constituent particles such as atoms, molecules or free electrons in a system possessing vibrational motion. The displacement of these particles from their equilibrium position generates heat energy in the system. Conduction is the mode of heat transfer in which energy exchange takes place in the medium from the region of high temperature to the region of low temperature due to the presence of temperature gradient in the body. The heat diffusion is a direct microscopic exchange of kinetic energy through the stationary boundary between two particles. In crystalline solids the thermal vibration arise due to the superposition of progressive displacement wave, called phonon, a quantized mode of vibration and which carries thermal energy. The microscopic heat transfer rate uses thermal energy related properties such as thermal conductivity, specific heat etc. of the material media and in turn these properties are related to the atomic-level properties. The rate at which heat flows through a certain area of a body defines the thermal conductivity and which is the main parameter to calculate the temperature distribution in any device. In an electronic device, the temperature gradient occurs at a given electrical power and the material physical properties changes since they are strongly dependent of temperature [10]. For HBTs, the temperature raises at base – collector (BC) junction due to higher localized current and it continues to rise with increase in power density. Accordingly a thermal runaway arises at a critical current, strongly dependent of thermal resistance which is the ratio between the variation of temperature at BC junction and the dissipated power.

4.2.1 Thermodynamic model

To evaluate the heat diffusion mechanism inside the device, a three dimensional numerical simulation is performed with Sentaurus device simulator (version E-2010.12) [11]. It is a multidimensional simulator for one, two and three dimensional semiconductor devices. The model is defined by the basic set of Poisson's equation and the lattice heat flow equation. The current densities for electrons and holes are given by the basic semiconductor equation. In generalized form, including temperature gradient, the current densities are,

$$\begin{aligned}\vec{J}_n &= -nq\mu_n (\nabla\Phi_n + P_n\nabla T) \\ \vec{J}_p &= -nq\mu_p (\nabla\Phi_p + P_p\nabla T)\end{aligned}\tag{Eq. 4.1}$$

where μ_n and μ_p are the electron and hole nobilities, ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials, P_n and P_p are the absolute thermoelectric powers. The second term in the current density equation is due to the non uniform distribution of temperature inside the device. It gives the flow of current due to the temperature gradient. The temperature distributions due to device self-heating are calculated by solving lattice heat flow equation as follows:

$$c_L \frac{\partial T}{\partial t} - \nabla \cdot \kappa \nabla T = -\nabla \cdot \left[(P_n T + \Phi_n) \vec{J}_n + (P_p T + \Phi_p) \vec{J}_p \right] \quad Eq. 4.2$$

where κ is the thermal conductivity and c_L is the lattice heat capacity of the material. The function T , in the above equation, represents temperature of a body.

In this simulation, we have considered only the thermal phenomena inside the device structure i.e. there is no electrical dependency. Thus the right side part of Eq. 4.2 has not been taken into account. We assume that, the body obeys the heat equation and, in addition, generates its own heat (q) at a place called “heat source”. Therefore, the temperature T satisfies an equation,

$$c_L \frac{\partial T}{\partial t} - \nabla \cdot \kappa \nabla T = q \quad Eq. 4.3$$

The thermal power q is the steady, pulse or sinusoidal power which has been generated by a “heat generator” and applied directly at the “heat source”. The applied heat dissipates into the device obeying the heat flow Eq. 4.3.

4.2.2 Simulation methodology

The temperature rises at BC junction of HBTs due to higher power density. Therefore, in this thermal simulation, BC junction of the device is treated as the “heat source”, where we generate the thermal power artificially. The “heat source” is defined by the “thermode”, which is an isothermal surface. The generated thermal power dissipates into the device through the “thermode”. In this study, we have performed two different transient simulations.

- Large signal transient simulation:

The pulse of thermal power is applied at the “thermode” and the transient variation of device temperature has been studied.

- Sinusoidal transient simulation:

The sinusoidal thermal power with a steady off-set value is applied at the “thermode” to obtain the dynamic variation of device temperature at different frequency. From this study, we can extract frequency domain magnitude and phase of thermal impedance.

In order to generate the sinusoidal thermal power from electrical power, a “power generator” is necessary. In this case, the available model is “Sentaurus Electrothermal Resistance” model as shown in *Figure 4-1*. The electrothermal resistance has two electrical contacts named “electrodes”, u_1 and u_2 , and one thermal contact “thermode”, t . The electrical behavior of the resistance is described by Ohm’s law, $u_1 - u_2 = R \cdot i$. The resistance produce Joule heat from electrical power, $q = (u_1 - u_2) \cdot i$, which is dissipated through the “thermode”.

A pure sinusoidal power cannot be generated at a resistance as, $q = (u_1 - u_2)^2/R$. Therefore, we developed an artificial “power generator” which can produce a sinusoidal thermal power that can be applied directly to the “thermode” as shown in *Figure 4-2*. This “power generator” is a compact model that has been developed in C code and which is coupled to finite element simulation.

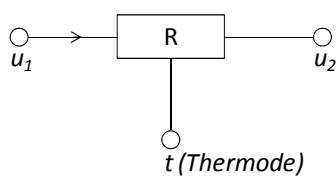


Figure 4-1: Sentaurus electro-thermal resistance model

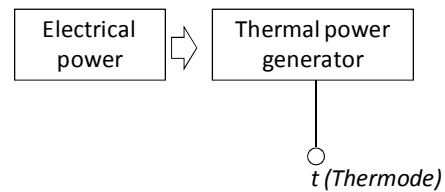


Figure 4-2: Sinusoidal thermal power generator

4.3 Device structure and material properties

The structure of device is fabricated with Sentaurus Structure Editor [12]. The device has been “placed” on a semi-infinite Si-block as shown in *Figure 4-3*. The thickness of the Si-block is L_Z ($= 300 \mu\text{m}$), same as Si-wafer. The BC junction is at $Z = 0$ plane. The “lower part” of the device, from BC junction to the wafer back-side (at $Z = 300 \mu\text{m}$), contains trench isolated structure (shallow trench and deep trench). The “upper part” of the device contains different process layers. The basic device structure consists of the rectangular heat source on a semi-infinite Si-substrate. The shallow trench and the deep trench walls are fabricated surrounding the heat source with different materials.

The applied simulations boundary conditions are:

- The boundary surfaces of the Si-block are adiabatic, i.e. there is no heat flow to the surroundings.
- The wafer back-side is isothermal and initially kept at ambient temperature (300 K). This is considered as the “thermal ground” (T_{Ground}).

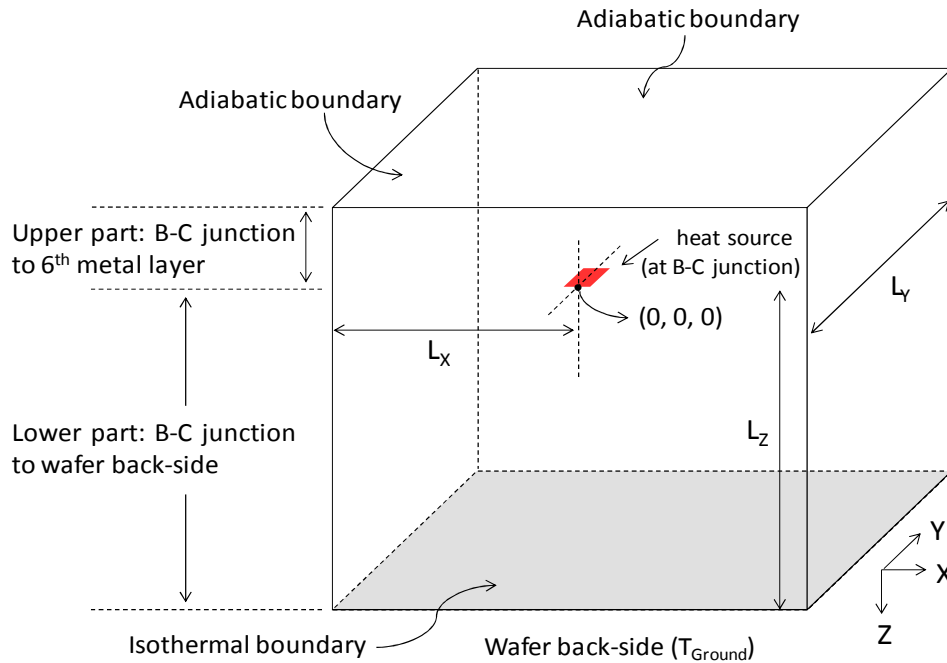


Figure 4-3: A semi-infinite Si substrate (defined by L_x , L_y and L_z), where $L_z = 300 \mu\text{m}$: the B-C junction of the transistor is at $(0, 0, 0)$.

4.3.1 The basic structure: “Lower part”

In a first attempt, the transistor structure is simplified by neglecting the “upper part” for computation time purpose. We have considered only the “lower part” starting from BC junction to T_{Ground} of the device and taking into account the deep trench, shallow trench and thick SiO_2 layer implanted in the Silicon substrate. The dimension of the heat source is same as the Emitter window ($L_E \times W_E$), where L_E and W_E are the length and width of the Emitter respectively. In this simulation the upper surface of BC junction is adiabatic which means that heat will diffuse towards the lower part of the device. We consider a simplified device with trench isolated structure as shown in *Figure 4-4* and *Figure 4-5*. The deep trench wall is constructed with SiO_2 – poli Si – SiO_2 with height D_{DT} and width W_{DT} . The shallow trench is a thick SiO_2 layer between

Emitter and Collector region with height D_{ST} and width W_{ST} . Two different structures have been studied:

- The transistor configuration is CBE (1 Collector, 1 Base and 1 Emitter) i.e., according to *Figure 4-4*, the structure is symmetric only with respect to x-axis, therefore $\frac{1}{2}$ of the device is considered.
- The transistor configuration is CBEEBC (2 Collector, 2 Base and 1 Emitter) i.e., according to *Figure 4-5*, the structure is symmetric with respect to both x and y-axis, therefore $\frac{1}{4}$ of the device is considered.

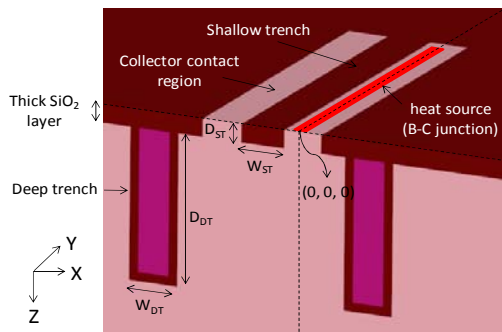


Figure 4-4: The lower part structure of the transistor with configuration CBE – $\frac{1}{2}$ of the device

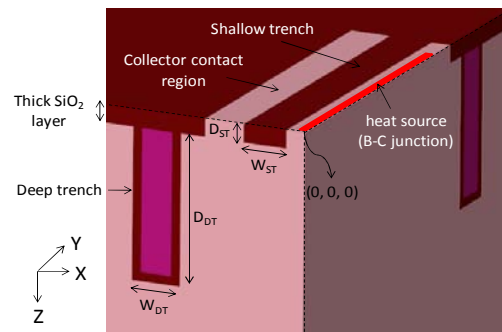


Figure 4-5: The lower part structure of the transistor with configuration CBEEBC – $\frac{1}{4}$ of the device

4.3.2 Basic structure with back-end layers: “Complete device”

In the final attempt of the simulation, we have added the backend process layers starting from SiGe base to 6th metallization layer. A brief description of this structure is given in *Figure 4-6*. The structure consists of one emitter, one base and one collector. The internal transistor with emitter, base and collector contacts is shown in the zoomed view. The process layers are SiGe – Base, poly Si – base with a single cobalt layer, Y – shape emitter, emitter poly Si, emitter – base – collector metal (copper) contacts and back–end metal layers. The back–end metal (copper) layers consist of five VIA and six metal layers. Except this structure, the surrounding region is filled with oxide (SiO_2). The heat source is placed at the interface between SiGe layer and Si substrate (base – collector junction) and its dimension is defined by the length and width of the emitter contact.

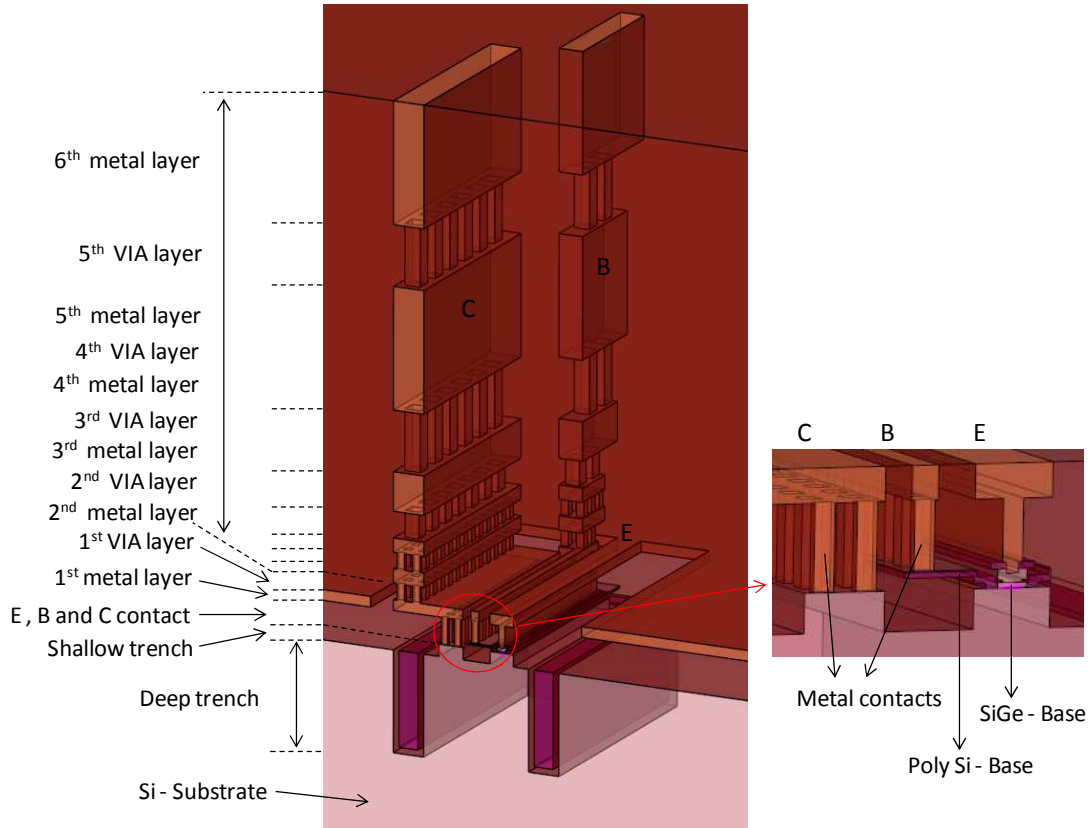


Figure 4-6: A complete structure including back-end process layers: $\frac{1}{2}$ of HBT, configuration – CBE, $L_E \times W_E = 9.88 \times 0.15$.

4.3.3 Physical parameters

The materials in the structure are silicon, SiGe, poly Si, Cobalt, SiO₂ and Copper. In this simulation, we have considered standard “Sentaurus Device” material properties. The thermal distributions inside the device due to self-heating are calculated by solving the heat flow equation. The required main physical parameters are thermal conductivity κ and lattice heat capacity c_L .

4.3.3.1 Thermal conductivity (κ)

The structure of the transistor is built on a semi-infinite Si – substrate and most of the region in “upper part” is filled with oxide. Hence, except the heat flow through the metal, most of the thermal diffusion takes place towards the wafer back-side. The introduction of deep trench restricts the lateral flow of heat flux and directs towards vertical. Due to poor thermal conductivity of trench wall, the heat flow from heat source is mostly confined within trench-enclosed region and thereby increases the temperature of the active device. Thus, the trench-

enclosed silicon substrate plays the major role in thermal phenomena. On the other hand, the thermal conductivity of silicon varies significantly with temperature than the other materials. Therefore, we have considered the temperature dependent of κ for silicon. We assume constant value of κ for poly Si, Cobalt, SiO₂ and Copper.

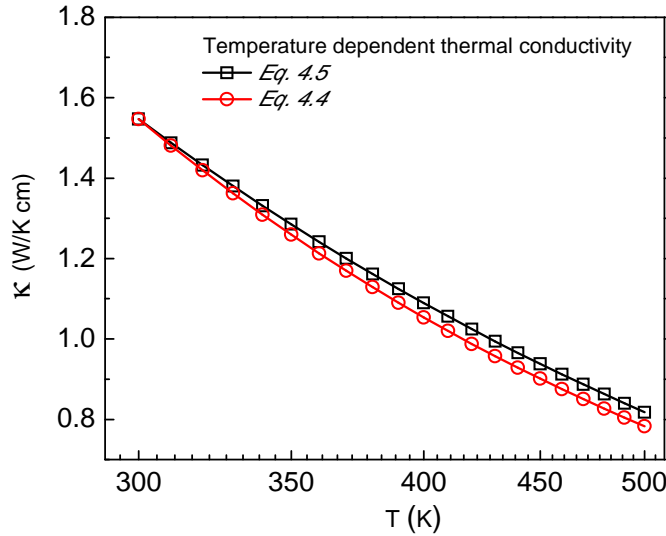


Figure 4-7: Temperature dependent thermal conductivity $\kappa(T)$: comparison between Eq. 2.4 and Eq. 2.5.

For most of the materials used in semiconductor devices, temperature dependent of κ in a relevant temperature range is approximately given by [13],

$$\kappa(T) = \kappa_{ref} \left(\frac{T}{T_{ref}} \right)^{-\alpha} \quad \text{Eq. 4.4}$$

Here κ_{ref} is the thermal conductivity at the reference temperature T_{ref} . For silicon $\alpha = 1.3$.

In “Sentaurus Device”, temperature dependent thermal conductivity is given by the following equation,

$$\kappa(T) = \frac{1}{\kappa_a + \kappa_b T + \kappa_c T^2} \quad \text{Eq. 4.5}$$

For silicon, $\kappa_a = 0.03 \text{ cmKW}^{-1}$, $\kappa_b = 1.56 \times 10^{-3} \text{ cmW}^{-1}$ and $\kappa_c = 1.65 \times 10^{-6} \text{ cmW}^{-1}\text{K}^{-1}$. The range of validity is from 200 K to well above 600 K (Sentaurus device user manual).

We present a comparison of $\kappa(T)$ for silicon between Eq. 4.4 and Eq. 4.5, where $T_{ref} = 300 \text{ K}$. We consider that, the κ_{ref} is same for both equations. Therefore, $\kappa_{ref} = \kappa(T = 300) = 1.54$

(from Eq. 4.5). Figure 4-7 shows $\kappa(T)$ vs. T calculated from Eq. 4.4 and Eq. 4.5. The constant values of κ for other materials are listed in TABLE 4-I.

4.3.3.2 Lattice heat capacity (C_L)

We assume a constant heat capacity (no temperature dependence) for all materials. The values are listed in the TABLE 4-I below.

TABLE 4-I
Constant κ and C_L at room temperature (300 K) for different materials.

Material	Thermal conductivity (κ) [W/K cm]	Lattice heat capacity (C_L) [J/K cm ³]
Silicon	1.54 @300K	1.63
SiO2	0.014	1.67
Poly Silicon	1.50	1.63
Copper	3.85	3.42
SiGe	1.54 [Si], 0.60 [Ge]	1.63 [Si], 1.67 [Ge]
Cobalt	1.00	3.74

4.4 Optimizations

Some optimization steps are needed to obtain a fast and accurate simulation. Some major steps have to be considered such as the choice of: i) the applied power density which has a significant impact on device R_{TH} through the temperature dependent κ for silicon; ii) the domain and the time of simulation: the surrounding surfaces of the Si-block are adiabatic, the heat will confine within it. Thus, sufficient heat diffusion domain is needed for simulation accuracy. The optimization has been performed in the following ways,

- **Mesh refinement:** for simulation accuracy, fine thermal contour lines and simulation time.
- **Simulation domain:** to optimize maximum heat spreading region for different dimension of heat source.
- **Power density:** due to the temperature dependent of κ .

Several simulations are performed to optimize step by step the simulation conditions as described below in detail.

4.4.1 Mesh refinement and simulation time

In order to obtain fine grid at the device regions where high lattice temperature T_{Lattice} and heat flux F_{Heat} gradients are expected, mesh refinement is especially important. One – half (for CBE) and one – fourth (for CBEBC) of the structure was simulated to reduce the CPU/memory requirements needed to achieve high level accuracy. We have applied adiabatic conditions in order to restore the missing part of the device. Mesh-building parameters have been optimized to avoid meshing issues, which are likely occurring in the following cases.

- Extremely thin layers implanted in the structure
- Interfaces between different materials
- Heat source and close to heat source regions
- Expected higher thermal gradient regions

Figure 4-8 shows an example of mesh refinement where the gradient mesh at interface between silicon and SiO_2 region, higher mesh density at heat source, close to heat source is made. The mesh density at every region has been optimized in order to obtain a sufficient accuracy at minimum simulation time.

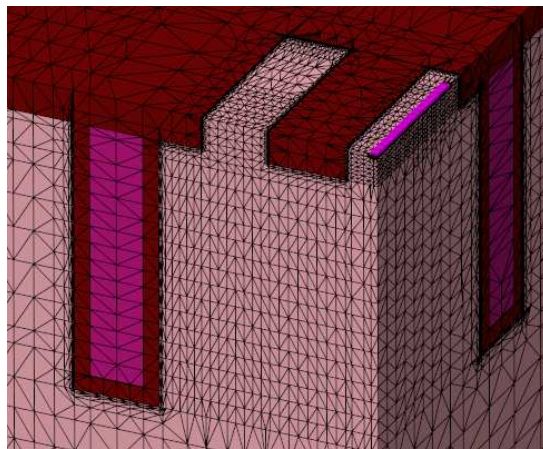


Figure 4-8: Mesh refinement of the device: $L_E \times W_E = 2.88 \times 0.15 \mu\text{m}^2$, CBEBC

All simulations are performed by using the system with 3.46 GHz 12-core processor and a 24 GB RAM. A brief analysis of simulation time for two different mesh configurations is given in *TABLE 4-II*. These simulations are performed for the dimension of heat source $9.88 \times 0.15 \mu\text{m}^2$ with CBEBC structure and the simulation domain, $L_X = L_Y = 300 \mu\text{m}$.

TABLE 4-II

Comparison of simulation times with mesh configuration and different simulations

Device structure		“Lower part”	“Complete device”
Mesh configuration		92005 (vertices)	363030 (vertices)
		619573 (edges)	2486520 (edges)
		1044847 (faces)	4228305 (faces)
		517278 (3D elements)	2104814 (3D elements)
Thermal simulation time	DC	1m 58sec	9m 57sec
	Large signal transient [Pulse: 40 ns delay, 10 ns rise and fall time, 5000 ns width, 7000 ns period]	29m 11sec	148m 45sec
	Sinusoidal transient [10^7 Hz frequency, 5 cycles]	55m 35sec	264m 35sec

4.4.2 Simulation domain

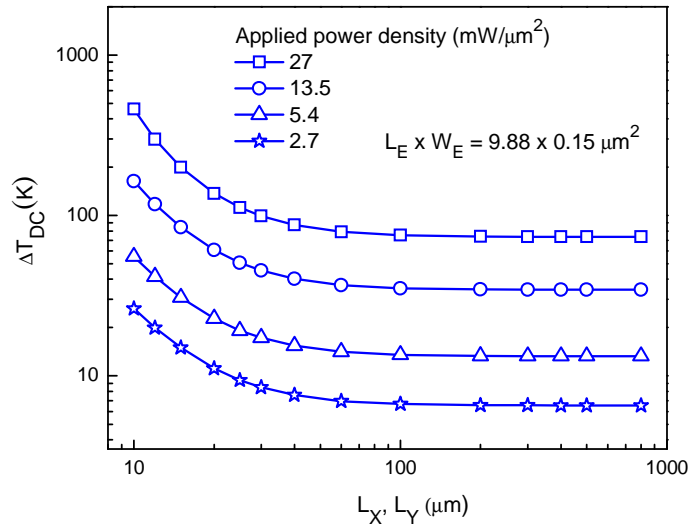


Figure 4-9: DC simulations for Si-substrate domain optimization: device temperature rise vs. L_X and L_Y at different power density (dimension of heat source = 0.15×9.88 , transistor configuration CBEBC).

The size of the 3D simulation domain (L_X and L_Y) along the heat source i.e. the dimension of the semi-infinite Si-block has been optimized through DC simulation. As the surrounding surfaces of the Si-block are adiabatic, heat flux spreads within the Si-block. In this simulation, we consider the simplified “lower part” structure i.e. heat diffusion takes place between heat source and T_{Ground} . In Figure 4-9, the device temperature rise (ΔT_{DC}) vs. length of L_X and L_Y has been

plotted when different DC powers are applied at the heat source. It is evident that, nearly above 100 μm the ΔT_{DC} s are stable at every applied DC power meaning that the horizontal heat flow is negligible. *Figure 4-10* shows that this hypothesis is verified for the complete set of geometry. Finally, for the higher accuracy we have considered $L_X = L_Y = 300 \mu\text{m}$ for all geometries of transistors in further simulations.

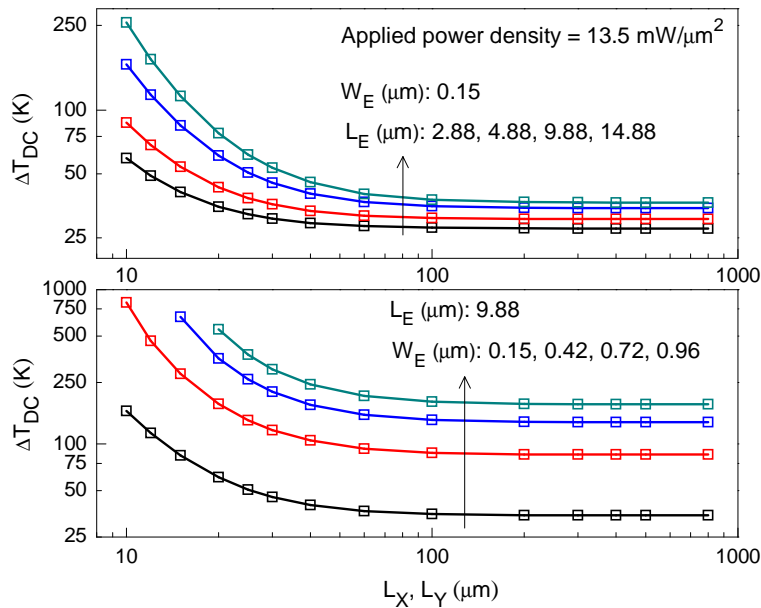


Figure 4-10: DC simulations for Si-substrate domain optimization: device temperature rise vs. L_X and L_Y for different device dimensions. Transistor configuration CBEBC

4.4.3 Applied power density

A DC thermal simulation results with temperature dependent $\kappa(T)$ and a constant κ (1.48 W/K cm) of silicon has been compared in *Figure 4-11*. The simulations have been performed applying different power densities. The constant κ prove a linear rise of ΔT , which results a constant R_{TH} (independent of temperature). In contrary, temperature dependent $\kappa(T)$ gives a non-linear change in ΔT resulting significant increase in R_{TH} .

In order to compare the device thermal effect with measurements, we have applied nearly same DC power density at the heat source to attain the practical junction temperature (same as measurements). The power density region, all the simulations performed, is noticeable in *Figure 4-11*.

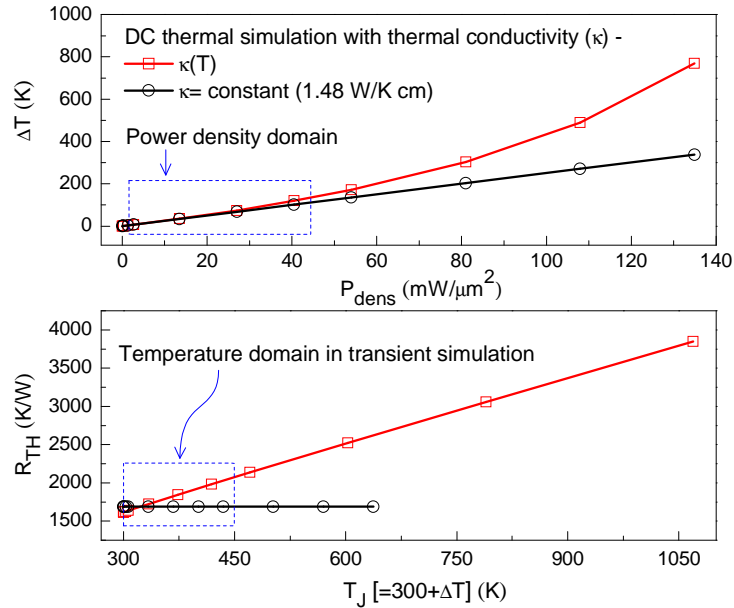


Figure 4-11: DC simulations at different power densities (transistor geometry – $L_E \times W_E = 9.88 \times 0.15 \mu m^2$, transistor configuration CBEBC): ΔT and R_{TH} comparison with temperature dependent $\kappa(T)$ and constant κ .

4.5 Transient simulations

We have performed two different transient thermal simulations as follows: (i) large signal – to obtain device temperature variations with time, and (ii) sinusoidal at different frequency – to extract magnitude and phase of thermal impedance.

4.5.1 Large signal transient simulation

Large signal transient simulations are performed by applying a square wave pulse of power at heat source. The pulse conditions are “40 ns delay, 10 ns rise and fall time, 5000 ns width, 7000 ns period”.

4.5.1.1 Transient ΔT_j

A simulation result is presented in Figure 4-12, where junction temperature changes (ΔT_j) are shown for different geometry of transistors. These simulations are performed with a constant power density $10 mW/\mu m^2$ for all devices. The total power increases with dimension of heat source, which gives rise in increase in junction temperature.

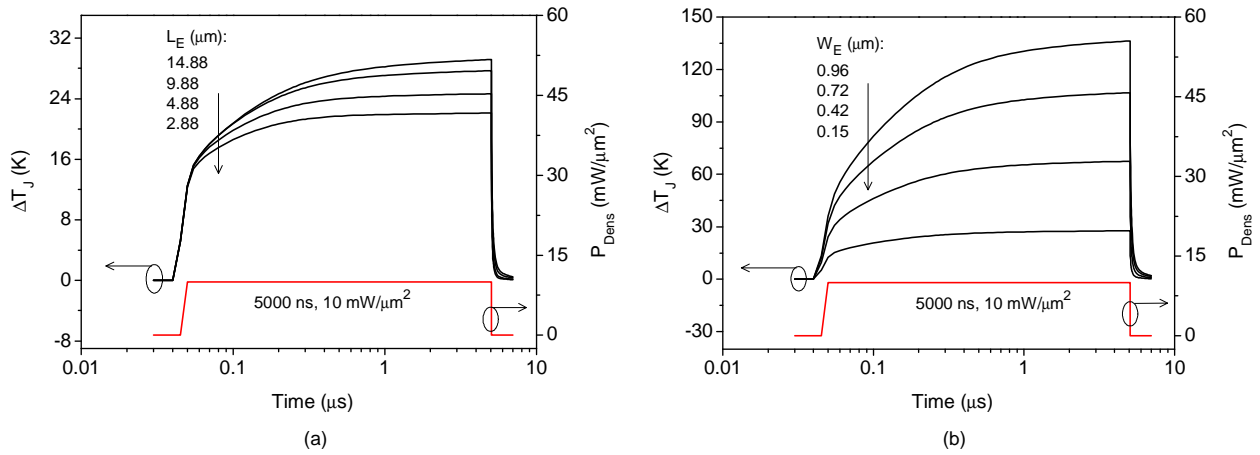


Figure 4-12: The transient ΔT_J for different geometries of device: applied pulse ($10 \text{ mW}/\mu\text{m}^2$ power density and 5000 ns width), (a) different lengths with $W_E = 0.15 \mu\text{m}$ and (b) different widths with $L_E = 9.88 \mu\text{m}$. Transistors configuration CBE

4.5.1.2 T_{Lattice} and F_{Heat} distribution

The F_{Heat} and T_{Lattice} distribution inside the complete device structure at pulse time of 5050 ns (close to steady state) are shown in Figure 4-13. Figure shows that the heat is concentrated mainly in the active region around the base-collector junction. The isolation trenches clearly influence the thermal gradient. Note that, the larger dissipation in the trench enclosed region is the result of low thermal conductivity of the SiO_2 .

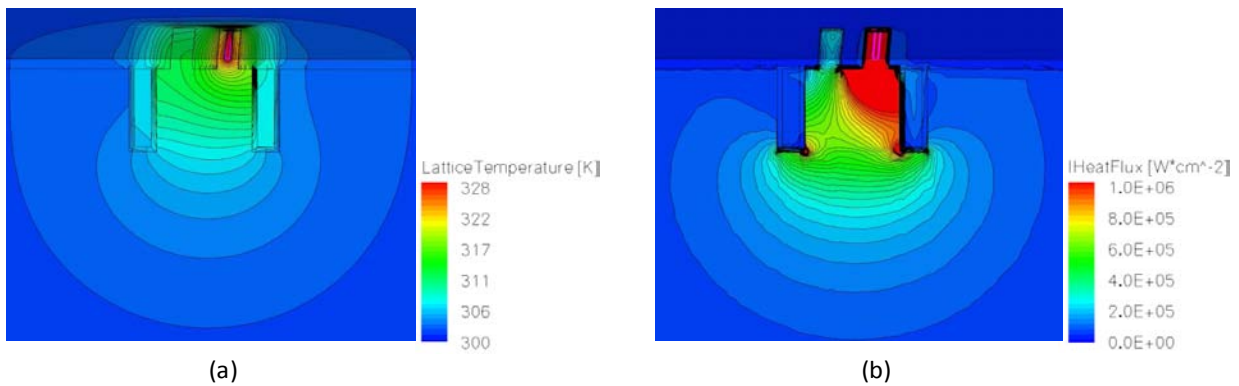


Figure 4-13: (a) T_{Lattice} and (b) F_{Heat} distribution inside the transistor at pulse time of 5050 ns with applied power density = $5.4 \text{ mW}/\mu\text{m}^2$: The dimension of the heat source ($L_E \times W_E = 9.88 \times 0.15 \mu\text{m}^2$), transistor configuration CBE.

A one-dimensional orthogonal cut through the middle of the “heat source” (0, 0, 0) of the structure has been performed at different pulse time to show the variation of temperature distribution inside the device. In Figure 4-14, we demonstrate the changes in T_{Lattice} and F_{Heat} comparison with the evolution of pulse time. At very short pulse time, higher temperature and

flux gradient are observed, which decreases successively with pulse time. The lower F_{Heat} gradient at longer pulse time (or steady state) could be the cause of significant device self-heating effect. Figure shows that the deep trench enclosed region have lower F_{Heat} slope at the pulse time higher than 220 ns, which can be due to the heat confinement by trench wall. These results clearly show that the rise in device thermal effect is almost proportional to the power dissipation. These Figures also show a high concentration of heat close to Base-Collector space.

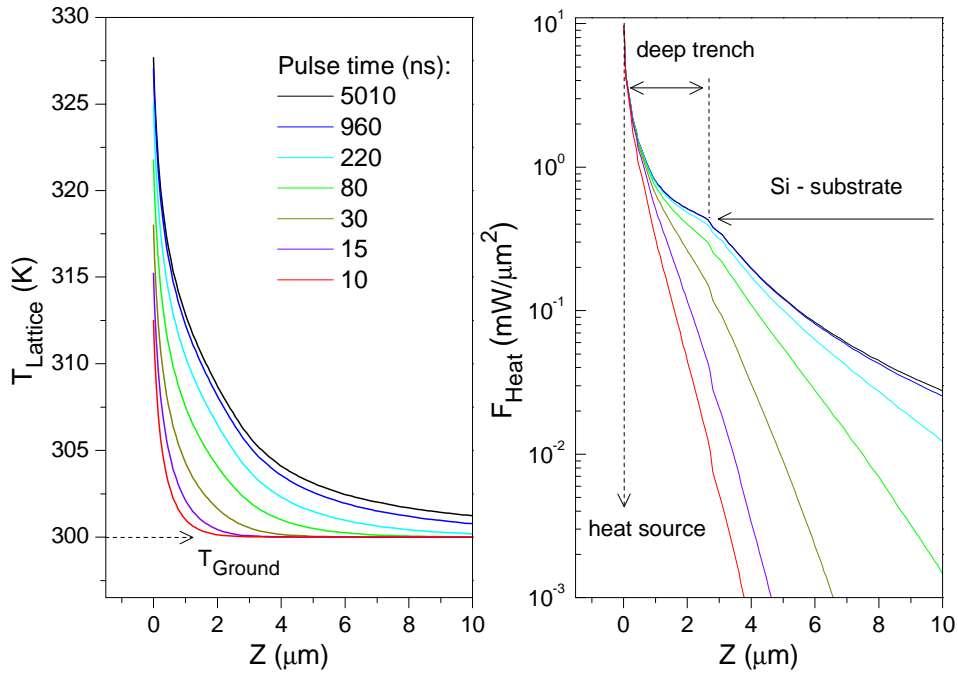


Figure 4-14: The lattice temperature (T_{Lattice}) and the heat flux (F_{Heat}) variation along z (from heat source towards wafer back-side) at different pulse time.

4.5.2 Sinusoidal transient simulation

The steady-state and sinusoidal electrical powers are applied simultaneously to a heat generator through its electrical nodes resulting in a heat dissipation inside the device through a thermal node (thermode). The thermode of the generator is placed at the BC junction of the transistor. Transient thermal simulations are performed in an isothermal condition at the bottom of the thermode so that heat dissipation can take place into the substrate region. The outside surface of the Si-block is adiabatic, i.e. ideally there is no outgoing heat flux (F_{Heat}) from the device to the environment.

4.5.2.1 Dynamic T_J

In order to obtain the dynamic variation of device temperature, the sinusoidal power with an offset value is applied. At various frequencies of the sinusoidal-signal, transient simulations have been performed until 10 complete cycles (in the figure up to 5 cycles are shown) to attain stable dynamic variation of temperature. A simulation result for the device with geometry $9.88 \times 0.15 \mu\text{m}^2$ and configuration CBEBC is shown in *Figure 4-15*. Transient simulations with three different frequency, same amplitude and DC offset power density are presented. It is noticed that the dynamic device temperature (peak-to-peak temperature) decreases when frequency of the signal increases. In *Figure 4-16*, the time delay between power density and temperature is shown.

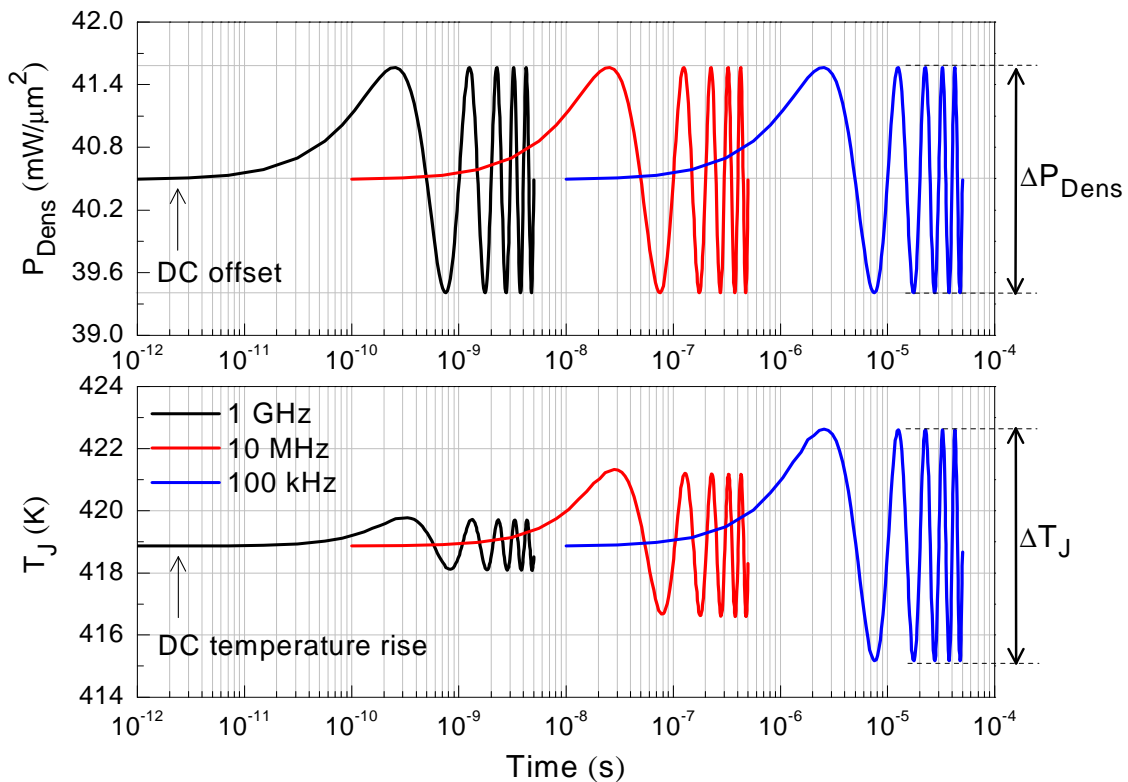


Figure 4-15: Sinusoidal transient simulation at different frequency (1kHz, 100kHz and 10 MHz): Applied P_{Dens} vs Time and dynamic T_J vs Time. DC offset = $40.5 \text{ mW}/\mu\text{m}^2$.

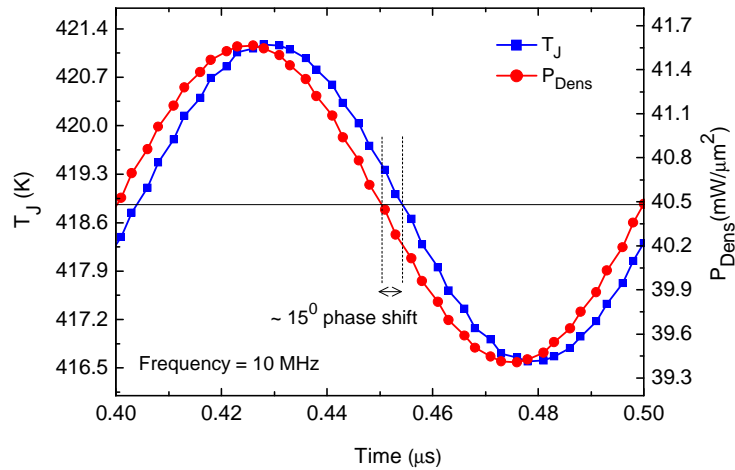


Figure 4-16: The phase shift between sinusoidal power (P_{Dens}) and dynamic temperature (T_J) at frequency = 10MHz.

4.5.2.2 Thermal impedance extraction

It has been noticed that, the dynamic change in device temperature decreases and the time delay between junction temperature (T_J) and the applied sinusoidal power density (P_{Dens}) increases with frequency. The frequency domain magnitude of Z_{TH} can be obtained from the ratio of peak-to-peak temperature differences (ΔT_J) and the corresponding peak-to-peak power density (ΔP_{Dens}) (Figure 4-15).

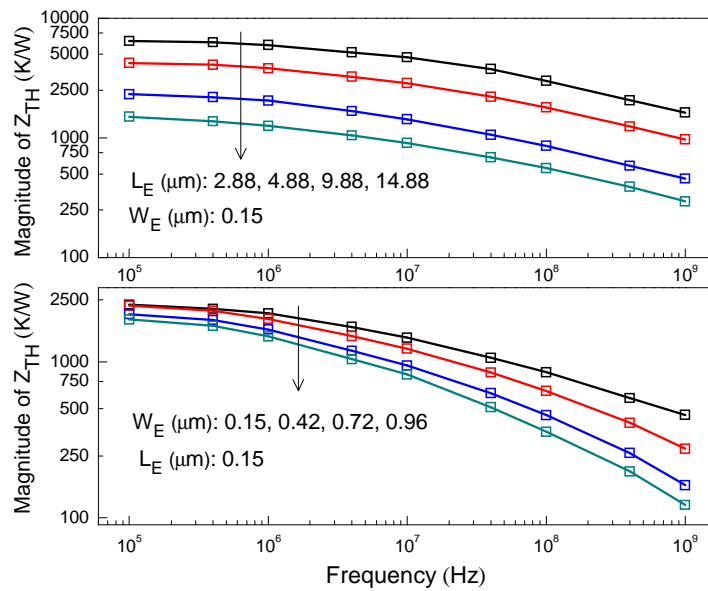


Figure 4-17: Magnitude of Z_{TH} at different frequency: for different dimension of devices (“Lower part” structure). Transistor configuration CBEC

The phase of Z_{TH} can be acquired from the time delay between T_J and P_{Sin} (Figure 4-16). In Figure 4-16, T_J and P_{Sin} for frequency 10 MHz are plotted in left and right y-axes respectively, which shows nearly 15° phase difference. The extracted magnitude (Figure 4-17) and phase (Figure 4-18) are plotted for different geometry of transistors.

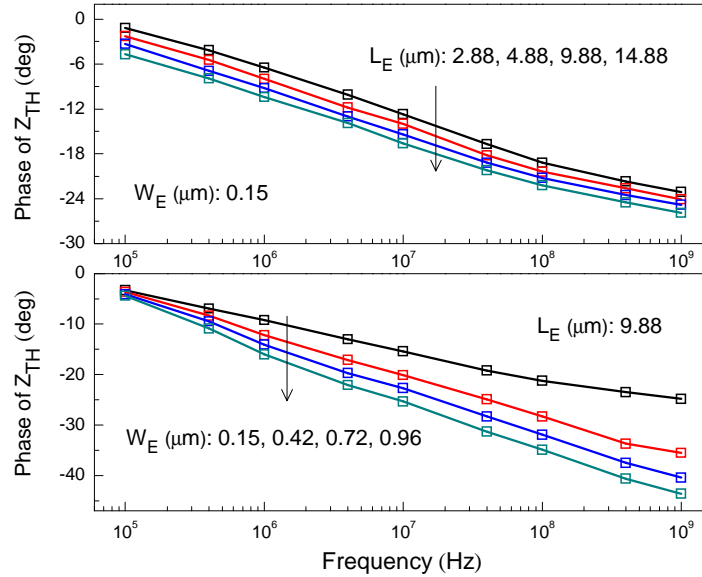


Figure 4-18: Phase of Z_{TH} at different frequency: for different dimension of devices (“Lower part” structure). Transistor configuration CBEB

4.6 Electro-thermal modeling

In this section, device thermal parameters (R_{TH} and C_{TH}) are extracted from transient ΔT_J through electro-thermal modeling. Two different electro-thermal networks, (i) a conventional single pole and (ii) a distributed recursive type network, are taken into account.

4.6.1 Single pole network

The transient variation of ΔT_J is mainly defined by C_{TH} where the steady state temperature is given by R_{TH} . In Figure 4-19, ΔT_J (TCAD data) has been modeled with the single RC network. In first step, R_{TH} is extracted by fitting the curve (without C_{TH}) at steady state region. In second step, C_{TH} is introduced to model the transient ΔT_J . It is evident that, a single pole network cannot properly model the whole transient varying region. But a possible range (maximum and minimum value) of C_{TH} can be obtained through the long time and short time extraction. Also the extraction with an average C_{TH} value is shown in figure.

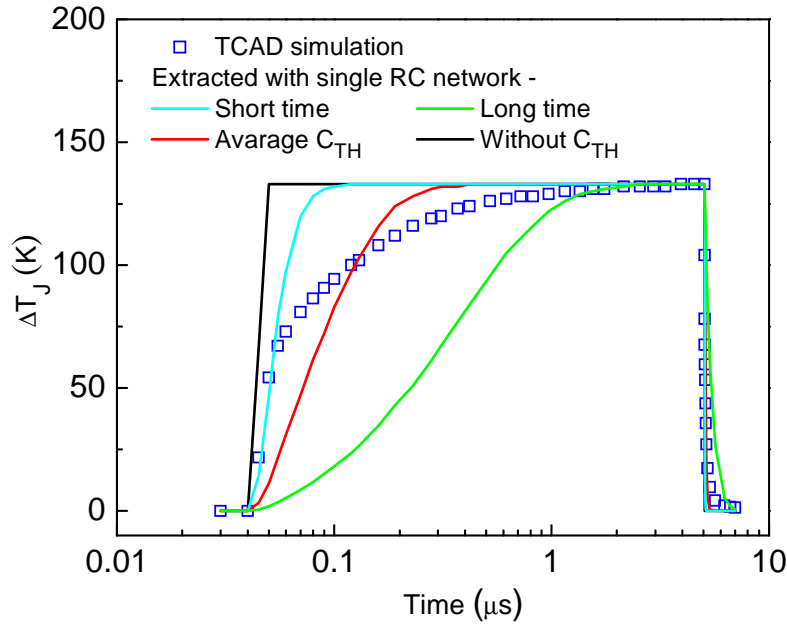


Figure 4-19: Modeling of the transient ΔT_j (simulation of lower part device structure with geometry of the heat source = $9.88 \times 0.15 \mu\text{m}^2$, Transistor configuration CBE) with single pole network.

4.6.2 Recursive network

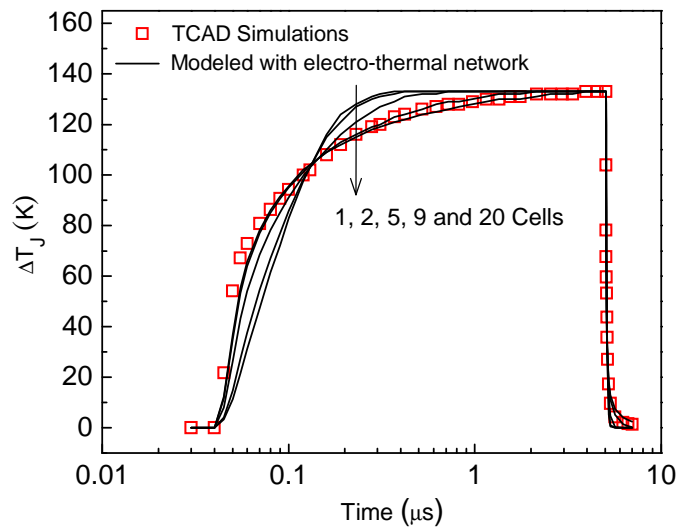


Figure 4-20: Modeling of ΔT_j (simulation of lower part device structure with geometry of the heat source = $9.88 \times 0.15 \mu\text{m}^2$, Transistor configuration CBE): Comparison of Recursive network with different number of cells in terms of accuracy in extraction.

When a transient power is applied to the device, theoretically an infinite number of thermal time constant are necessary to represent the thermal response of the material due to its distributed nature. Thus, dynamic self-heating could not be properly modeled with a single pole

network, as it has only a single time constant. Therefore, we have considered a distributed recursive type network. The network has been verified performed in terms of accuracy with increasing number of cells. In *Figure 4-20* and *Figure 4-21*, electro-thermal modeling with different number of cells has been compared. Note that, a recursive network using only one cell is equal to the single-pole network. It is clearly observed that the model with higher number of cells provides better accuracy in both time and frequency domain. Extraction with 9 cells is very close to 20 cells, therefore in further extraction and thermal modeling 9 recursive cells are taken into account.

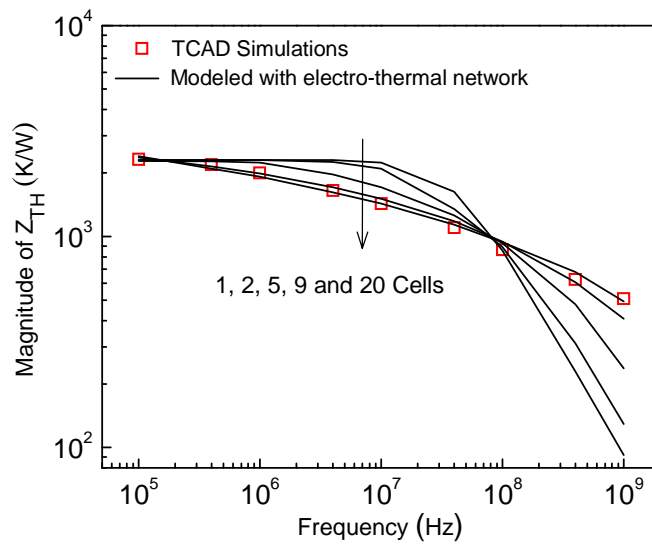


Figure 4-21: Modeling of the magnitude of Z_{TH} (lower part device structure with geometry of the heat source = $9.88 \times 0.15 \mu\text{m}^2$): Comparison of Recursive network with different number of cells in terms of accuracy in extraction.

4.6.3 Parameter extraction

Thermal parameters for both networks are extracted through electro-thermal modeling of ΔT_j . The sum of series resistance elements of the recursive cells is equal to the R_{TH} extracted from single pole network as follows,

$$R_{TH} = \sum_0^n K_r^n R \tag{Eq. 4.6}$$

In this extraction, $n = 9$. The decreasing nature of R_{TH} with the geometry of heat source i.e. device dimension is shown in the *Figure 4-22*. The average C_{TH} with a maximum and minimum

limit has been shown for different device dimension in *Figure 4-23*. The capacitance elements of each cells of the recursive network are given in *Figure 4-24*.

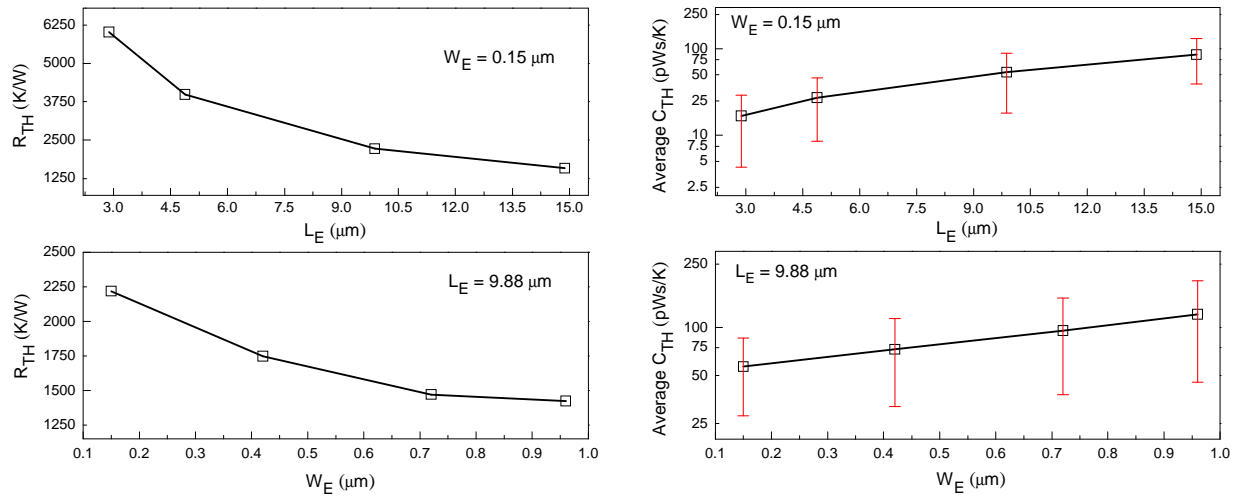


Figure 4-22: Extracted R_{TH} s (with single pole network) of different geometries of device from “lower part” simulations.

Figure 4-23: Extracted average C_{TH} s (with single pole network) of different geometries of device from “lower part” simulations.

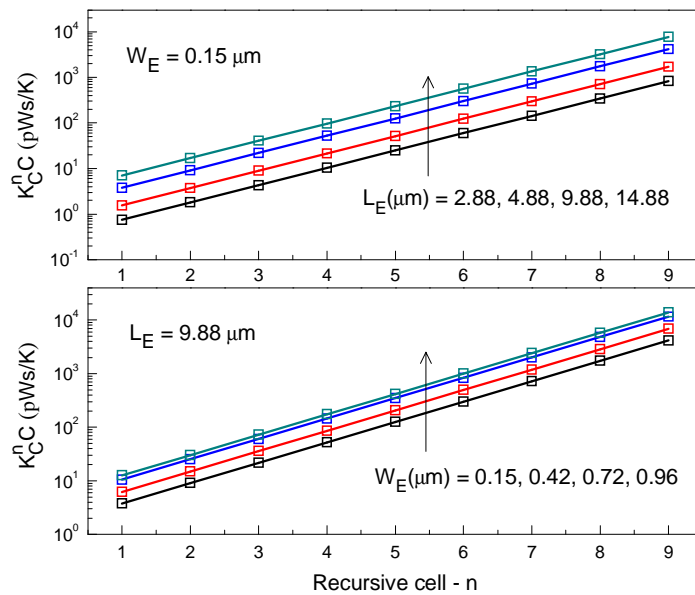


Figure 4-24: Extracted capacitance elements of recursive network for different geometries of device: “lower part” simulations.

4.7 Impact of back-end layers on thermal effect

In order to investigate the exact thermal phenomena in our transistors, a complete structure is designed. A detailed description of the structure is presented in section 2.3.2. The large signal and sinusoidal transient simulations are performed applying different back-end layers to explore the impact of these layers in device self-heating effect. For better clarity in explanation every structure is identified with the symbols which are listed below (*TABLE 4-III*).

TABLE 4-III

List of symbols for back-end structure identification.

Symbol	Device structure
L	Lower part
YE	Lower part + back-end layer upto Y-shape Emitter
E	Lower part + back-end layer up to Emitter contact
EBC	Lower part + back-end layer up to Emitter, Base and Collector contacts
M1	Lower part + back-end layer up to first metal layer
M2	Lower part + back-end layer up to second metal layer
M6	Lower part + back-end layer up to six metal layer

4.7.1 T_{Lattice} and F_{Heat} distribution

The T_{Lattice} and F_{Heat} distribution for a complete structure of the transistors are achieved from a steady state thermal simulation applying a DC power density $40 \text{ mW}/\mu\text{m}^2$. The simulation results are shown in *Figure 4-25*. The structure is with 1 emitter, 1 base and 1 collector (CBE) and the dimension of the heat source is $9.88 \times 0.15 \mu\text{m}^2$. The high conductive metal contacts and the first metal layer are very close to heat source which gives a higher thermal gradient. In *Figure 4-25*, a significant heat flow is observed through the metal layers. A one-dimensional orthogonal cut of the structure (*Figure 4-25*) through the middle of the “heat source” (0, 0, 0) is taken to show the variation of temperature distribution inside the device. In *Figure 4-26*, we demonstrate the distribution of T_{Lattice} and F_{Heat} and its change when upper back-end is added in simulations. It is noticed that, the heat flux gradient through the emitter metal contact and the 1st metal layer is higher than that of lower part region. Due to this significant heat flow, the T_{Lattice} at heat source and surrounding region decreases considerably.

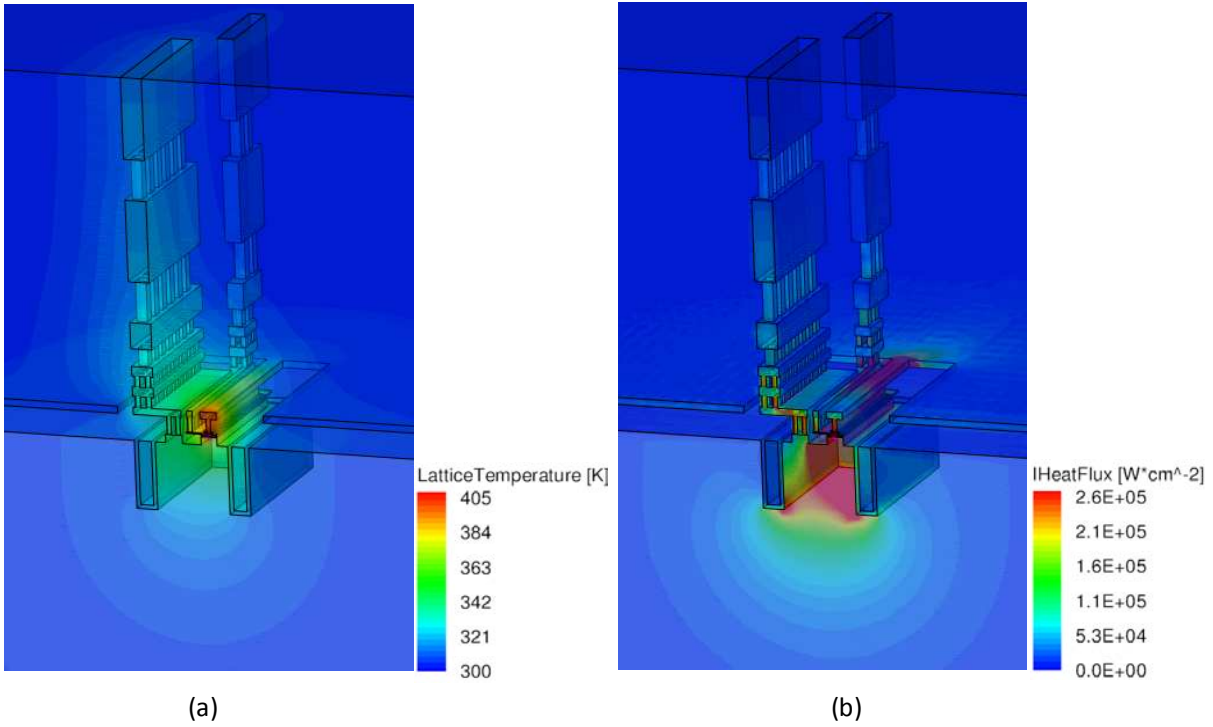


Figure 4-25: (a) F_{Heat} and (b) $T_{Lattice}$ distribution inside the transistor at steady state with applied power density = $40 \text{ mW}/\mu\text{m}^2$: Complete device structure with CBE configuration; the dimension of the heat source ($L_E \times W_E = 9.88 \times 0.15 \mu\text{m}^2$).

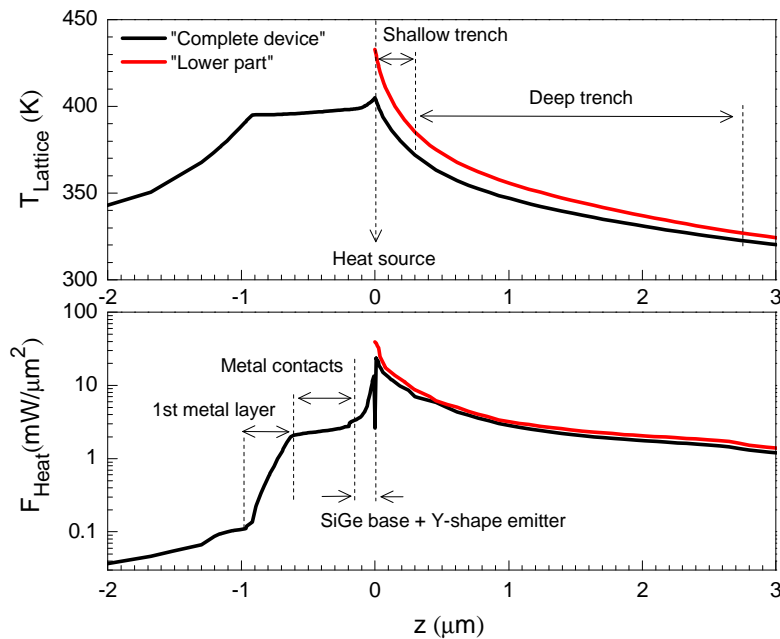


Figure 4-26: The lattice temperature ($T_{Lattice}$) and the heat flux (F_{Heat}) variation along z at pulse time 5050 ns (nearly steady state); the heat source (B-C junction) is at $z = 0$; +ve z is si-substrate region and -ve z is back-end metal layers.

4.7.2 Comparison of ΔT_J s

The transient simulations are performed for different backend structure (L, YE, E, EBC, M1, M2, M6) applying pulse condition: width = 5000 ns and power density $40 \text{ mW}/\mu\text{m}^2$. The ΔT_J for all structure are compared in *Figure 4-27*. We have subdivided the overall ΔT_J varying region into: (A) Short time domain and (B) Long time domain to steady state as marked in the *Figure 4-27*. It has been discussed in the previous section that, steady state and transient temperature can be defined by R_{TH} and C_{TH} respectively. It is observed that, the maximum device temperature (at pulse time 5050 ns) decreases significantly when the backend layers are added. The considerable ΔT_J variation in the region – B and the change of the slope in region – A from different simulations explains the influences of back-end layers on R_{TH} and C_{TH} .

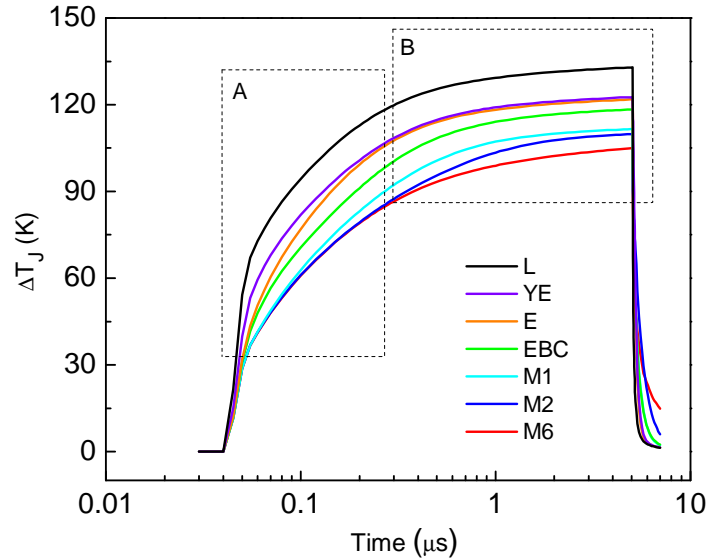


Figure 4-27: The transient junction temperatures for different device structure: (applied pulse = $5.4 \text{ mW}/\mu\text{m}^2$ power density and 5000ns width); the dimension of heat source ($L_E \times W_E$) = $9.88 \times 0.15 \mu\text{m}^2$)

4.7.3 Comparison of R_{TH} s and C_{TH} s

The R_{TH} s and average C_{TH} s are extracted from ΔT_{Ps} for all the structures (L, YE, E, EBC, M1, M2 and M6) for different back-end layers. A statistical analysis has been shown where the thermal parameter from lower part simulation is taken as a reference. When different back end layers are added, R_{TH} decreases while C_{TH} increases as shown in *Figure 4-28* and *Figure 4-29* respectively.

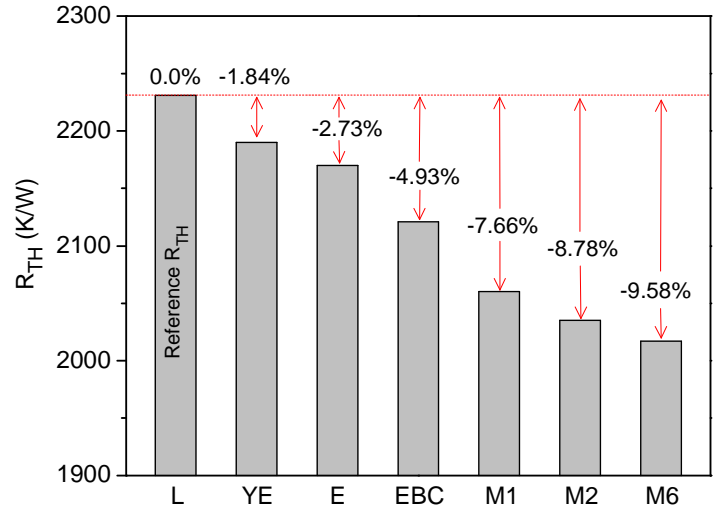


Figure 4-28: The % variation of thermal resistance when different back-end layers are added: lower part structure is considered as reference. Device configuration: CBE

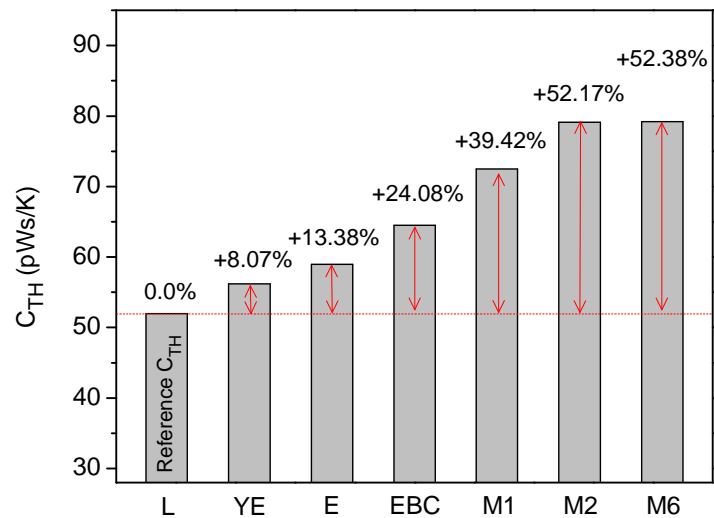


Figure 4-29: The % variation of average thermal capacitance when different back-end layers are added: lower part structure is considered as reference. Device configuration: CBE

4.7.4 Comparison of frequency domain Z_{THS}

The Z_{THS} at different frequencies are extracted from sinusoidal transient simulations for various structures. A comparison for magnitude and phase of Z_{THS} is plotted in *Figure 4-30* and *Figure 4-31* respectively. It is seen that, the frequency domain slope increases when back-end process layers are taken into account. The phase of Z_{THS} increases and nearly 40° maximum shifts is found for the structure with 6 metal layers.

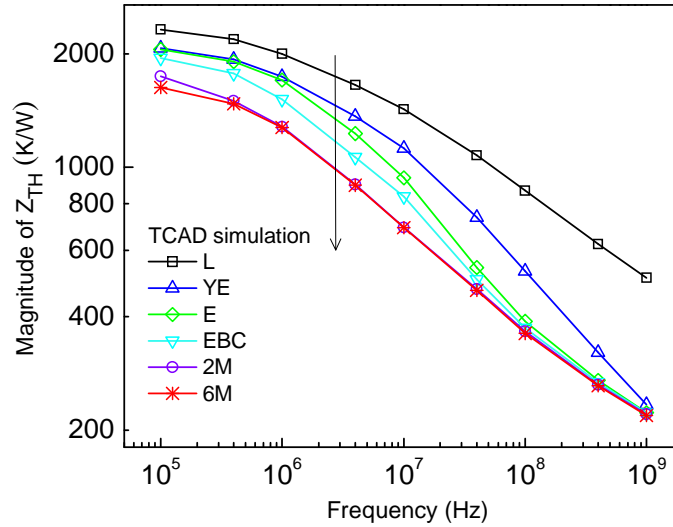


Figure 4-30: The magnitude of thermal impedance variation when different back-end layers are added: Device configuration: CBEBE

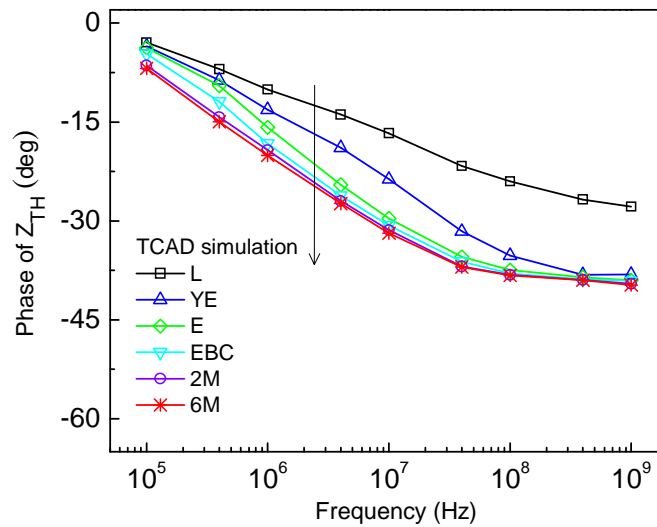


Figure 4-31: The Phase of thermal impedance variation when different back-end layers are added: Device configuration: CBEBE

4.7.5 Analysis of the effect

The thermal capacitance is a function of the temperature rise associated with a given quantity of applied energy. It is also a function of material properties, the product of material's specific heat, density and volume.

$$C_{TH} = \frac{qt}{\Delta T} = c\rho V \quad \text{Eq. 4.7}$$

Here, q is the heat transfer per second, t the time, ΔT the temperature increase, c the specific heat, ρ the density and V is the volume of the material. The specific heat of Silicon, SiO_2 and Copper is 0.703 J/gK, 1.0 J/gK and 0.385 J/gK respectively. The major regions of backend layers are fabricated with materials like silicon, poly silicon (thermal properties are same as silicon), SiO_2 and copper. The whole surroundings of the metal contact, VIA and metal layers are filled with SiO_2 . Therefore according to Eq. 4.7, these layers give reasonable contribution of thermal capacitance which could not be neglected. Furthermore, the device upper surface cannot absorb permanent heat flux since this surface is adiabatic and has less influence at steady state while the back end region can store some energy during transient state. From this analysis, we can deduce that it affects more on C_{TH} and, therefore, Z_{TH} in frequency domain.

4.8 Conclusion

In this study, three dimensional thermal TCAD simulations are performed on a submicron SiGe:C BiCMOS technology (with f_T and f_{max} of 230 GHz and 290 GHz) in order to investigate the transient and the dynamic behavior of the device temperature in dependence of the device architecture and material properties. Optimizations are performed precisely for mesh refinement, simulation domain and power densities. The structure of the transistors is same as the measured one. In the first attempt, the simplified “lower part” structures for several device geometries are simulated. Large signal transient simulations are performed to obtain time domain junction temperature variations while frequency domain thermal impedance is extracted from sinusoidal transient simulation. T_{Lattice} and F_{Heat} distribution inside the device at different pulse time are studied. R_{THS} and C_{THS} are extracted through electro-thermal modeling. Two different networks are compared in terms of accuracy in modeling and parameter extraction. In comparison with the conventional single pole network, the recursive network provides the best compromise among accuracy, number of model parameters and physical basement. Finally, a complete device structure has been built including different back-end process layers e.g. SiGe – Base, Poly Si – Base with a cobalt layer, Y – shape Emitter, Emitter poly Si, Emitter – Base – Collector metal contacts and metal layers (up to 6 metal). The impact of back-end layers on junction temperature and, therefore, on thermal parameters are investigated. The heat flow through the metal contacts causes a significant decrease in R_{TH} . Moreover, it has been found that, the backend structure has a major impact on C_{TH} and, therefore, on frequency domain Z_{TH} .

Finally, the dependence of C_{TH} with back-end demonstrates that the extracted value is layout dependant. Since the devices in measurement and in circuit configuration have a different back end structure, some modeling inaccuracy may appear for circuit simulation.

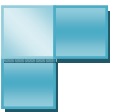
4.9 Reference

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Results validation, scalable approach and applications

This chapter presents a comparison of thermal parameters extracted from different measurements and device simulations. In the previous chapters, it has been shown that a conventional single pole network cannot properly model the transient or dynamic thermal behavior and therefore a recursive network needs to be used. Therefore, in final investigation, we propose a scalable recursive model for transient self-heating effect in trench isolated Si-Ge HBTs. This model has been verified through numerical simulations as well as low frequency s-parameter measurements and found to be in excellent agreement for various device geometries.



5.1 Results and validation: comparison between measurements and thermal TCAD simulations

In this section, the comparisons of thermal parameters are shown which are extracted from different methods like pulse measurements, DC measurements at different ambient temperatures and low frequency s-parameters measurements. Also the TCAD simulation results are compared and verified by measurements. In order to obtain the accuracy in the parameter extraction, all measurements have been performed on the same device. In these comparisons, R_{THS} extracted from DC measurements (R_{TH-DC}) and the C_{THS} (C parameter of recursive network) extracted from low frequency s-parameter measurements have been considered as the reference. The sum of resistances of each recursive cell ($\sum K_r^n R$) extracted from pulse measurements can give the total R_{TH} value (R_{TH-P}).

5.1.1 R_{THS} – different geometries of transistors

In *Figure 5-1*, extracted thermal resistances from (i) pulse measurements (R_{TH-P}), (ii) DC measurements at different ambient temperatures (R_{TH-DC}) and (iii) thermal TCAD simulations for “lower part” of device ($R_{TH-TCAD-Lower\ part}$) are compared. The decreasing nature of R_{THS} with L_E (for constant W_E) and W_E (for constant L_E) is shown.

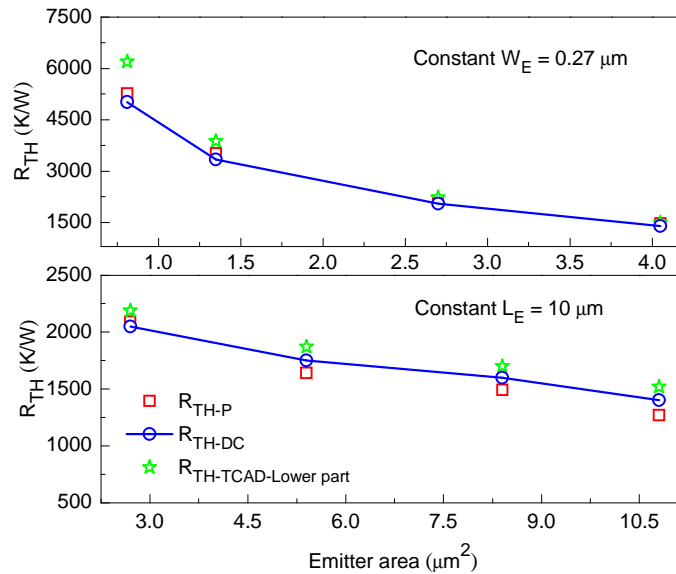


Figure 5-1: R_{THS} comparison for different geometries of transistor – extracted from Pulse measurements, DC measurements at different ambient temperature and thermal TCAD simulations

The R_{TH-P} values are very close to the reference value (R_{TH-DC}) for most of the geometries. This confirms the validity of the proposed pulsed measurement method. The $R_{TH-TCAD-Lower\ part}$ extracted from numerical simulation is higher than the measurements. It may be due of the upper part (back-end layers) of the transistor, which has not been taken into account in this simulation. There is no heat diffusion through the different back-end process layers, especially metal contacts and metal layers. As the thermal conductivity of metal (copper for this process layout) is higher than the silicon, significant heat diffusion can take place through the upper part which can reduce the R_{TH} value.

5.1.2 C_{THS} – different geometries of transistors

In *Figure 5-2*, C_{THS} for different geometries of transistors are extracted from (i) pulse measurements (C_{TH-P}) and (ii) transient TCAD simulations ($C_{TH-TCAD-Lower\ part}$) with a single pole network. The increasing behavior of C_{THS} with emitter area is shown.

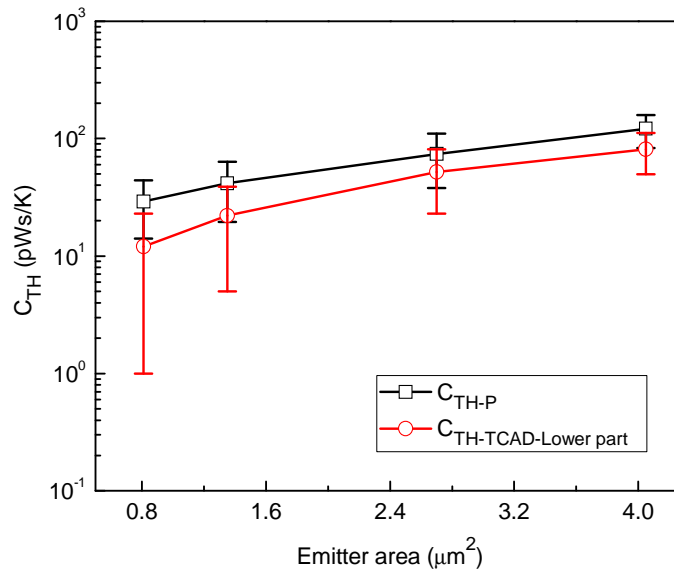


Figure 5-2: C_{THS} extracted (maximum – minimum limit) from pulse measurements (C_{TH-P}) and TCAD simulation for “lower part” structure ($C_{TH-TCAD-Lower\ part}$)

It has been exposed that (in chapter - 2) a single C_{TH} cannot properly model the time domain thermal behavior. Therefore, a maximum and minimum value has been extracted through modeling the long and very short transient time region respectively. This maximum and minimum limit of C_{TH} is indicated through the error bar. It is seen that, the C_{THS} extracted from the TCAD simulation (for lower part device structure) are lower than the measurements. In this

simulation the contribution of device “upper part” is neglected. This has been described in *chapter - 4*.

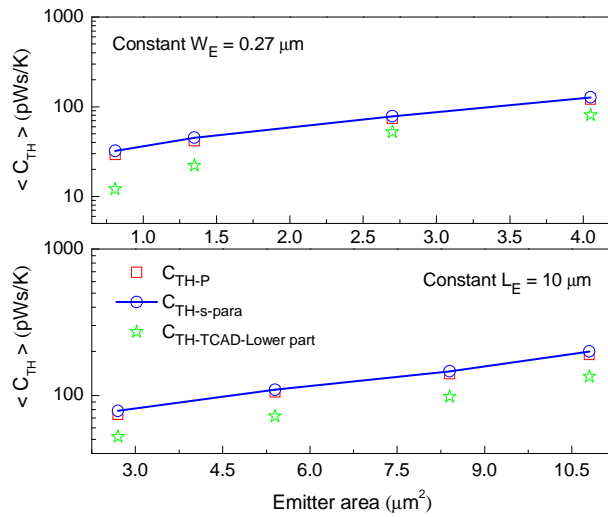


Figure 5-3: Average C_{TH} – extracted from pulse measurements (C_{TH-P}), low frequency measurements ($C_{TH-s-para}$) and thermal simulations ($C_{TH-TCAD-Lower part}$).

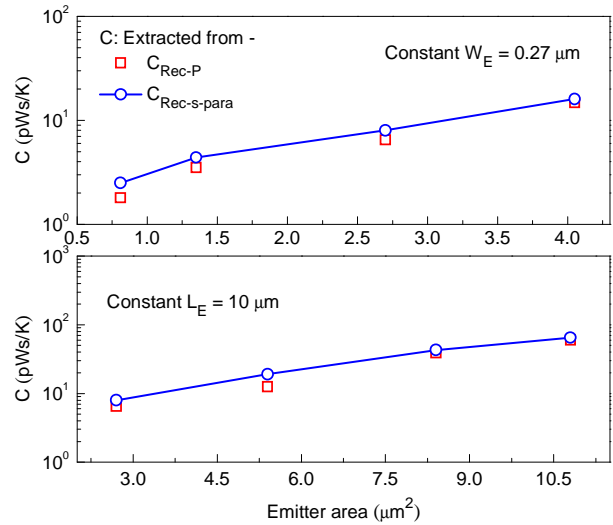


Figure 5-4: Capacitance parameter C of recursive network – extracted from pulse measurements (C_{Rec-P}) and low frequency measurements ($C_{Rec-s-para}$).

An average value of C_{TH} ($\langle C_{TH} \rangle$) can be obtained from the maximum and minimum value. The $\langle C_{TH} \rangle$ for different L_E (at constant W_E) and W_E (at constant L_E) has been compared (as shown in *Figure 5-3*) among: (i) pulse measurements (C_{TH-P}), (ii) low frequency s-parameter measurements ($C_{TH-s-para}$) and (iii) thermal TCAD simulations for “lower part” of device ($C_{TH-TCAD-Lower part}$) are compared. The capacitance parameter C of the recursive network is plotted in *Figure 5-4*. The C_{TH-P} and C_{Rec-P} values are very close to the reference value ($C_{TH-s-para}$ and $C_{Rec-s-para}$) for most of the geometries which confirms the validity of the pulsed measurement method for self-heating characterization.

5.1.3 % deviation of R_{THS} and C_{THS} from reference value

In *Figure 5-5*, all the measurements and simulations are compared with respect to the reference value. The % deviation of R_{TH-P} and $R_{TH-TCAD-Lower part}$ is shown with respect to R_{TH-DC} where with C_{TH-P} and $C_{TH-TCAD-Lower part}$ is compared with $C_{TH-s-para}$. The TCAD simulation results are significantly far from the reference measurements results. Therefore, in the next simulation step the backend structure is added which consists of SiGe Base, poly Si-Base, Y-shape emitter, metal contacts for emitter, base, and collector and after that up to six metal layers. This has been

described in the previous chapter. One device structure with an emitter window of ($L_E \times W_E$) $9.88 \times 0.15 \mu\text{m}^2$ has been considered to investigate the influence of upper metallic part on the R_{TH} and C_{TH} .

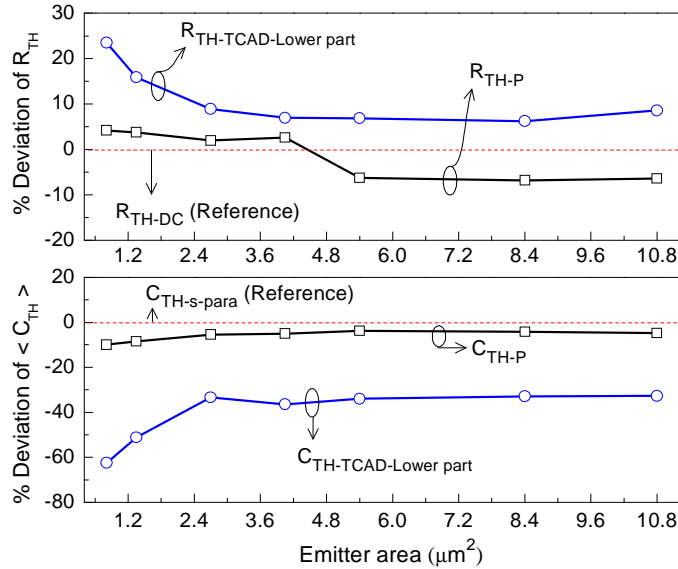


Figure 5-5: % deviation of R_{TH} s and C_{TH} s with respect to reference value: comparison among different measurements and simulations.

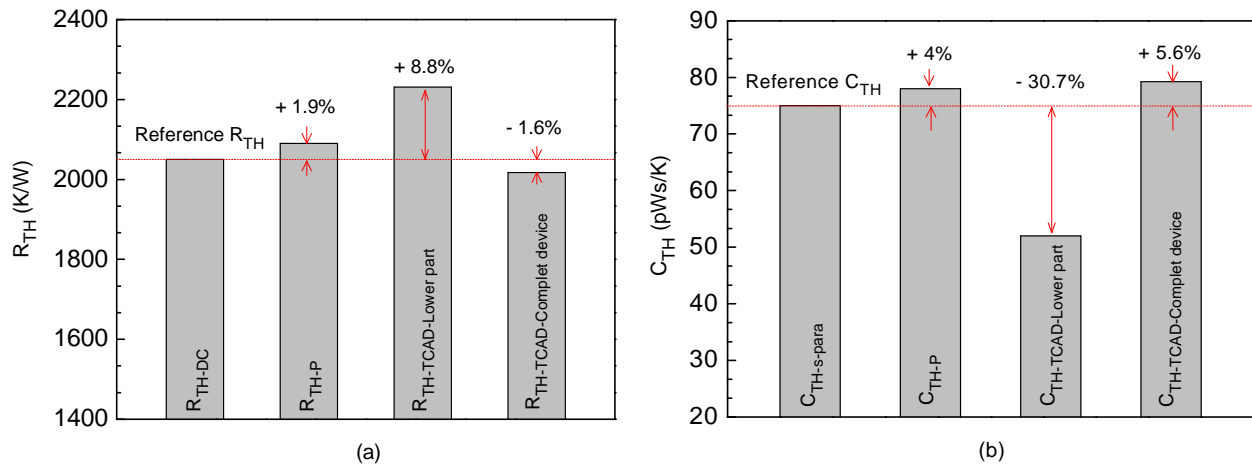


Figure 5-6: Comparison of R_{TH} s – DC measurements, pulse measurements, TCAD simulation for “lower part” and “complete device”.

Figure 5-7: Comparison of C_{TH} s – low frequency measurements, pulse measurements, TCAD simulation for “lower part” and “complete device”.

A statistical comparison among the measurements and simulations with complete structure has been given in Figure 5-6 and Figure 5-7. In the “lower part” simulation, the deviation of $R_{TH-TCAD-Lower\ part}$ and $C_{TH-TCAD-Lower\ part}$ with respect to R_{TH-DC} and $C_{TH-s-para}$ was

found to be (+) 8.8 % and (-) 30.7 % respectively. These differences are decreases by adding back-end structure where only (-) 1.6 % and (+) 5.6 % deviations are found. Therefore, the R_{TH} decreases about 10.6 % due to the heat flow through back-end part while 36.3 % of C_{TH} increases. This large variation shows a considerable impact of metal layers on thermal parasitics.

5.1.4 Z_{TH} s - measurements and thermal TCAD simulations

The magnitude and phase of frequency domain Z_{TH} s are extracted from “lower part” as well as “complete device” simulations. A comparison between simulation and measurement is presented in *Figure 5-8* (Magnitude of Z_{TH}) and *Figure 5-9* (Phase of Z_{TH}). A large variation of frequency domain slope of the magnitude (nearly -6 dB/dec for “lower part” and -9 dB/dec for “complete device”) is found. This is due to the increase in C_{TH} when the different backend layers are added. A very good agreement is obtained between “complete device” simulations and measurements.

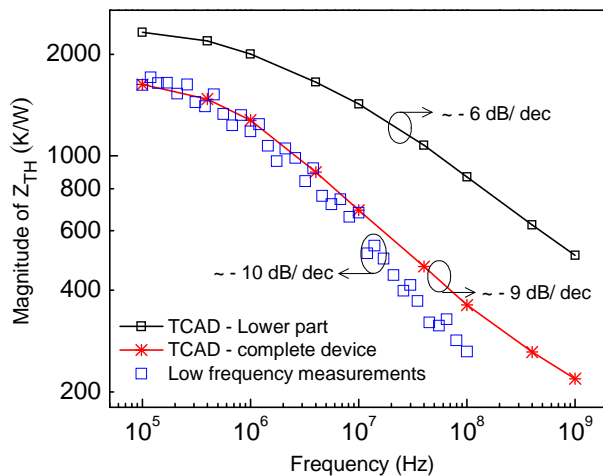


Figure 5-8: Magnitude of Z_{TH} - Comparison between measurements and TCAD simulation for “lower part” and “complete device” structure.

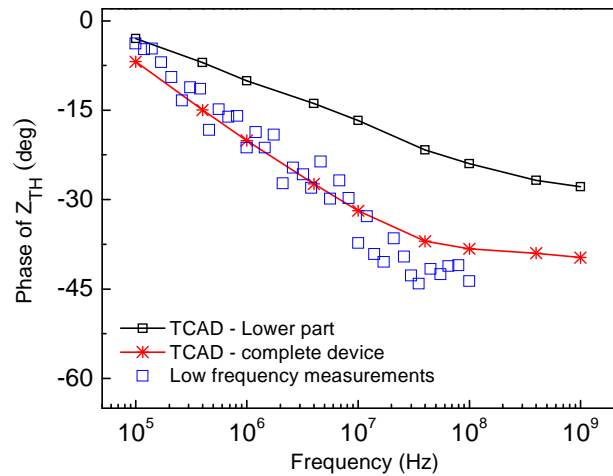


Figure 5-9: Phase of Z_{TH} - Comparison between measurements and TCAD simulation for “lower part” and “complete device” structure.

5.2 Introduction to scalable model

The dynamic relationship between instantaneous power dissipation and the temperature rise due to self-heating is incorporated inside a compact model using a passive network. A variety of analytical models have been developed to scrutinize self-heating effects by connecting different electro-thermal networks such as single RC (thermal resistor and capacitor) network,

Foster network, Nodal network, Cauer network and Recursive network at the temperature node of the compact model [1–4]. Besides that, circuit optimization requires geometry scalable models to get the best tradeoff between circuit speeds, noise, power consumption etc. A number of methods have been approached for scalable thermal model however these are limited to single RC network [5–7]. In addition to that, a comparative study based on low frequency s -parameter measurements and compact model simulation among different electro-thermal networks in the frequency domain has been investigated [8]. It is manifested from the previous chapters that recursive electro-thermal network provides the best compromise between accuracy, number of model parameters and physical point of view. Up to our knowledge, no geometrical scalable model for recursive network has been developed for trench isolated SiGe HBT. Hence, in this study, we propose a scalable electro-thermal recursive network derived from physical considerations, which can be applicable in time and frequency domain analysis. The elements of the network are obtained applying approximated spherical and pyramidal heat diffusion methods.

5.3 Theoretical analysis of thermal spreading behavior

The time dependent diffusion of heat can be modeled by a distributed electro-thermal network [9], [10]. An elementary slice at a distance ξ from the heat source towards thermal ground (T_{Ground}) with thickness $\Delta\xi$ is characterized by a resistance $\Delta R(\xi)$ and capacitance $\Delta C(\xi)$ as follows,

$$\Delta R(\xi) = \frac{1}{kA(\xi)} \Delta\xi, \quad \Delta C(\xi) = \frac{\kappa}{\alpha} A(\xi) \Delta\xi \quad \text{Eq. 5-1}$$

where $A(\xi)$ is the local cross-section area at a distance ξ . κ and α are the thermal conductivity and heat diffusion coefficient of the material. During transient heat dissipation inside the material, the distributed thermal resistance and the capacitance of the network follow the physical behavior described by Eq. 5-1.

Two different heat diffusion models have been described to demonstrate time dependent heat dissipation. The first approach describes a representation of spherical heat distribution. In the second method we consider an approximated pyramidal heat flow between the power dissipation and T_{Ground} . The elementary thermal volume elements are taken at different distance from the heat source.

5.4 Distributed Electro-thermal network

The network is considered as a combination of $N+1$ numbers of series R-C cells where each cell is placed at successive distance from the heat source. The position of each cell can be calculated physically according to the T_{Lattice} and F_{Heat} distribution inside the device.

5.4.1 Thermal distribution inside the device

The variation of T_{Lattice} and F_{Heat} from the heat source to thermal ground is obtained through thermal TCAD simulation (*Chapter-4*) as shown in *Figure 5-10*.

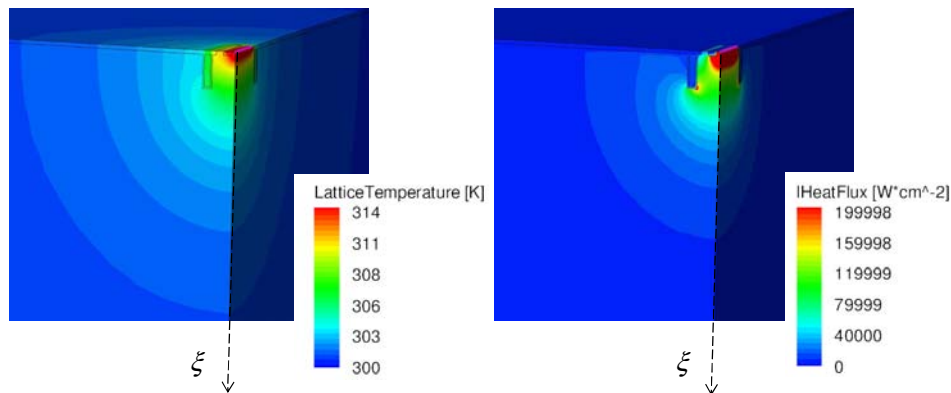


Figure 5-10: T_{Lattice} and F_{Heat} distribution inside the $1/4$ of the device with CBEC configuration: applied DC power = 2mW, dimensions of the heat source ($L_E * W_E$) = $9.88 * 0.15 \mu\text{m}^2$.

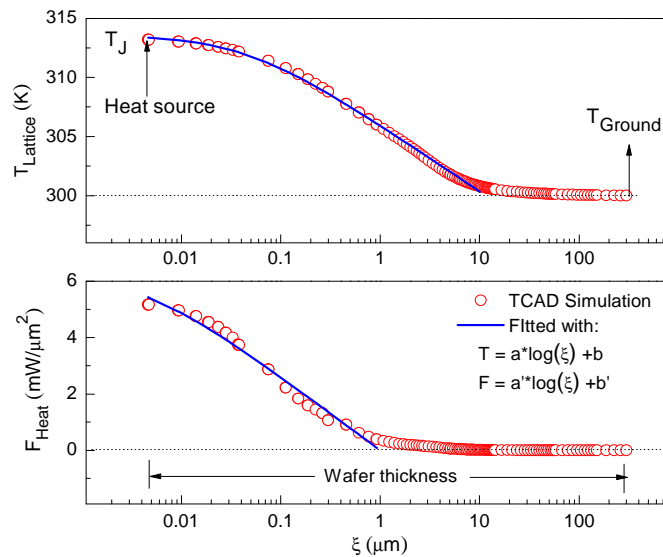


Figure 5-11: Variation of the T_{Lattice} and the F_{Heat} along ξ from the heat source to T_{Ground} from TCAD simulation (symbols) and fitted with the logarithmic function (lines).

The direction from heat source to T_{Ground} is given by ξ . A cross-section of the position of *Figure 5-10* towards the ξ has been plotted in *Figure 5-11* which shows a logarithmic variation of both T_{Lattice} and F_{Heat} with ξ . Therefore, we have considered the position of the recursive cells as an exponential order to obtain a linear variation of T_{Lattice} and F_{Heat} with distance ξ .

The heat source has been considered as a rectangular parallelepiped with height ξ_{min} and the length and width are same as L_E and W_E respectively. The placement of the network can be calculated from *Figure 5-11* where the first cell is located at ξ_{min} . The position of N^{th} recursive cell can be given by the following equation:

$$\xi_N = \xi_{\text{min}} \exp(\beta N) \quad \text{Eq. 5-2}$$

Here $(N+1)$ is the number of the R-C cells of the recursive thermal network and β (<1) is the parameter required to calculate the position of ξ_N in between the heat source and T_{Ground} .

5.4.2 Placement of the network cells

The positions of the thermal resistance and capacitance elements of the recursive network have been determined according to the *Eq. 5-2* where the first cell is located close to the heat source at ξ_{min} . For the N^{th} cell of the network, the resistance is placed between ξ_N and ξ_{N+1} where the capacitance is placed between the averages of (ξ_{N-1}, ξ_N) and (ξ_N, ξ_{N+1}) and T_{Ground} as shown in *Figure 5-12*.

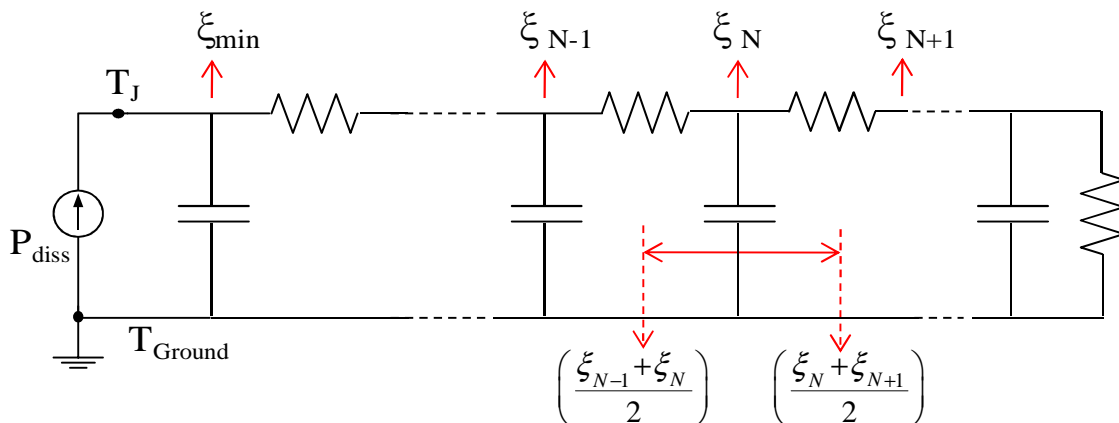


Figure 5-12: Recursive electro-thermal network: physics based electrical representation of transient or dynamic thermal impedance

5.5 Approximations in the heat diffusion mechanism

5.5.1 Spherical heat diffusion model

The heat diffusion from the active region can be simplified as spherical heat conduction path, where every element is equivalent to a heat generating sphere [10]. At every distance from the heat source the area of the sphere (equithermal surface) increases which allows heat flux to diffuse faster. According to *Eq. 5-1* the thermal resistance is inversely proportional to the elementary heat diffusing local cross-sectional area, therefore thermal resistance decreases as the distance increases from active heat source. The thermal capacitance depends on the elementary heated volume elements and thus increases with distance. In this method, the rectangular Emitter (from top view) area has been treated as a sum of m -number of identical circular area and from each circle; heat flux is dissipating in spherical heat diffusion path within a certain angle. We consider the angle (φ) as a fitting parameter where, $\varphi_{\min} < \varphi < \pi/2$. For simplicity we consider the sum of the diameter of m -circles is equal to the length of the Emitter window as given in figure below. According to *Figure 5-13* the rectangular heat source (emitter window) is the sum of m -number of circular area and heat flux is dissipating into the device from the centre of each circle. The radius and the number of the circle can be calculated by the following way:

$$\pi r^2 m = L_E \cdot W_E, \quad 2rm = L_E \quad \text{Eq. 5-3}$$

It generates m -number of parallel recursive network and therefore, m number of parallel thermal resistance and capacitance. Now at a distance ξ from the heat source, the equithermal surface element for one circular heat source contained by an angle φ is given by,

$$A_1(\xi) = 2\pi\xi^2(1 - \cos\varphi) \quad \text{Eq. 5-4}$$

Thus for m -number of circular heat source, the total surface element can be given by,

$$A_m(\xi) = 2\pi\xi^2(1 - \cos\varphi)m \quad \text{Eq. 5-5}$$

Therefore, the thermal resistance and capacitance for the N^{th} recursive cell can be calculated from *Eq. 5-1* and *Eq. 5-5* as follows:

$$R_N(\xi) = \int_{\xi_{N-1}}^{\xi_N} \frac{d\xi}{\kappa A_m(\xi)} = \frac{1}{\kappa} \int_{\xi_{N-1}}^{\xi_N} \frac{d\xi}{2\pi\xi^2(1 - \cos\varphi)m} \quad \text{Eq. 5-6}$$

$$C_N(\xi) = \frac{\int_{\frac{(\xi_{N-1} + \xi_N)}{2}}^{\frac{(\xi_N + \xi_{N+1})}{2}} \frac{\kappa}{\alpha} A_m(\xi) d\xi = \frac{\kappa}{\alpha} \int_{\frac{(\xi_{N-1} + \xi_N)}{2}}^{\frac{(\xi_N + \xi_{N+1})}{2}} 2\pi\xi^2 (1 - \cos\varphi) m d\xi \quad \text{Eq. 5-7}$$

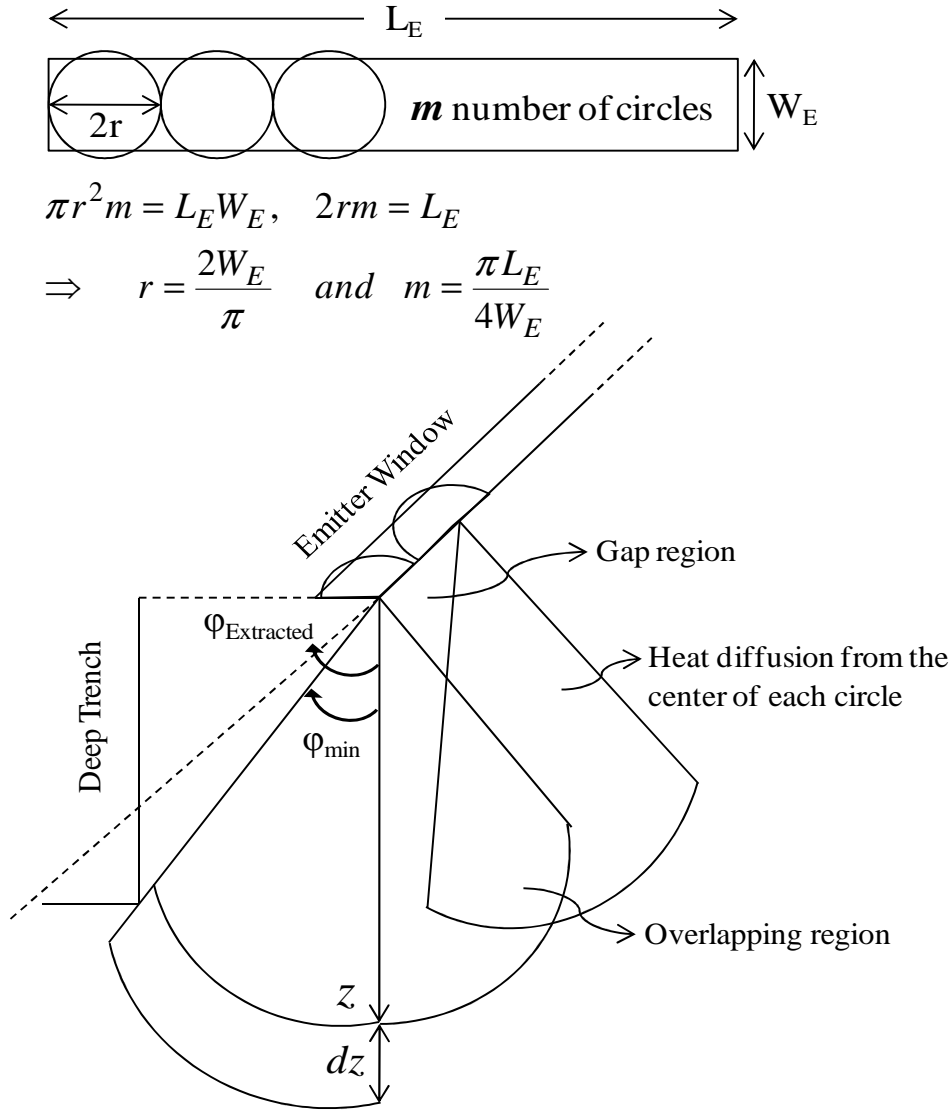


Figure 5-13: Spherical approximation of heat flux diffusion: the rectangular emitter window has been treated as the combination of m -number of identical circles where r is the radius of the circles.

Therefore, for the N^{th} R-C cell, situated at a distance ξ from the heat source, the thermal resistance and capacitance is given by,

$$R_N(\xi) = \frac{1}{2\pi\kappa(1-\cos\varphi)m} \cdot \frac{1}{\xi} \Bigg|_{\xi_{N-1}}^{\xi_N} \quad \text{Eq. 5-8}$$

$$C_N(\xi) = \frac{2\pi\kappa}{3\alpha} m(1-\cos\varphi) \xi^3 \Bigg|_{\frac{(\xi_{N-1}+\xi_N)}{2}}^{\frac{(\xi_N+\xi_{N+1})}{2}} \quad \text{Eq. 5-9}$$

Eq. 5-8 and Eq. 5-9 give the network elements as a function of m and therefore L_E and W_E . κ and α are the thermal conductivity and heat diffusion coefficient of the material. The minimum heat diffusion angle (φ_{\min}) is defined by the position of deep trench from the heat source and the height of the heat source. Therefore the heat diffusion angle can be given by,

$$\varphi = \varphi_{\min} + d\varphi = \tan^{-1} \left(\frac{W_E + \delta}{D_{dt} + D_{st}} \right) + d\varphi \quad \text{Eq. 5-10}$$

Here, W_E is the Emitter width, δ the distance between Emitter window and deep trench, D_{dt} and D_{st} are the height of the deep trench and shallow trench respectively. $d\varphi$ is taken to be a fitting parameter for heat diffusion angle.

5.5.1.1 Verification of the model: Z_{TH} modeling

The frequency domain thermal impedance for different geometry of device has been achieved with numerical TCAD simulations and has been modeled with a distributed electro-thermal network with the elements defined in Eq. 5-8 and Eq. 5-9. A comparison between simulated thermal impedance and extracted with scaling thermal network has been given in Figure 5-14. Nine recursive network cells have been used to perform the simulation. In this scalable model, κ and α are two physical parameters, L_E , W_E , D_{dt} , D_{st} , W_{dtBox} , and L_{dtBox} are the device geometrical parameters and $d\varphi$ is the angle fitting parameter. The extracted value of φ is given in TABLE 5-1. Figure 5-14 gives a good agreement between simulated and extracted thermal impedance for different length of device when width is fixed but the scaling rule does not obey for different width.

TABLE 5-1

The extracted and the minimum value of heat diffusion angle for spherical heat diffusion model.

Heat diffusing angle	φ_{\min} (deg)	Extracted φ (deg)
φ	33.4	48.7

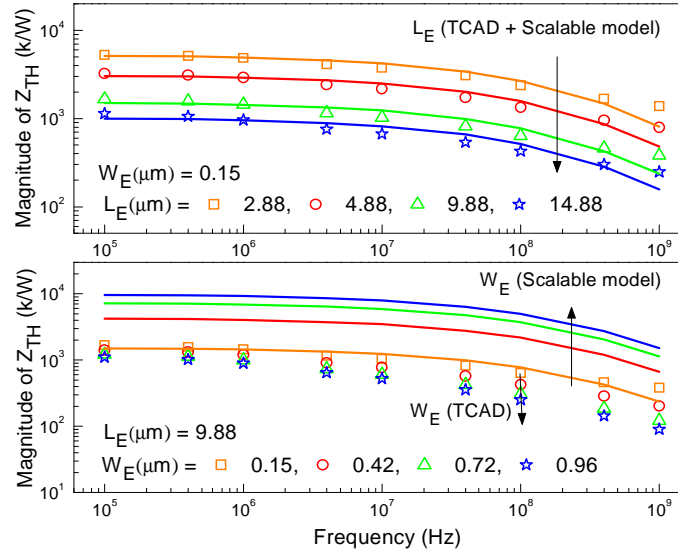


Figure 5-14: Magnitude of thermal impedance for different geometry of transistors: comparison between numerical simulation (symbols) and extracted (solid lines) with electro-thermal recursive network with spherical approximation of scaling rule.

5.5.1.2 Limitations of the model

In these device structures, the length of emitter L_E is much greater than the width W_E and therefore the m-circles have been considered over the length. The minimum heat diffusion angle ϕ_{\min} depends on the distance between the center of the circle and deep trench wall towards the Emitter width. According to Figure 5-13 the heat diffusion from two nearest circular heat source forms an overlapping region and a gap region. The heat flow through the gap region is not taken into account in the model. For the devices with identical width heat diffusing angle ϕ is the same and therefore the overlapping or the gap regions are same. But as the W_E increases i.e. the centre of the circles are moving far from each other the gap region increases and consequently, the same parameter ($d\phi$) value could not attain to the exact thermal impedance. Thus in this model the fitting parameter $d\phi$ could be dissimilar for different width of the emitter window.

5.5.2 Pyramidal heat diffusion model

In this method, the heat flow inside the device can be approximated to be confined to a pyramidal body. The key assumption is that the heat is spreading with a constant angle from heat source to T_{Ground} [9]. The spreading angle depends on the device structure and the geometrical parameters. The technology of the device under test is trench isolated and the shape of Emitter window is rectangular. The thermal dissipation from a rectangular heat source is assumed to

spread out into the substrate under two variable angles θ and ϕ where, $\theta_{\min} < \theta < \pi/2$ and $\phi_{\min} < \phi < \pi/2$. The minimum value of the angles is defined by height of deep trench as shown in *Figure 5-15*.

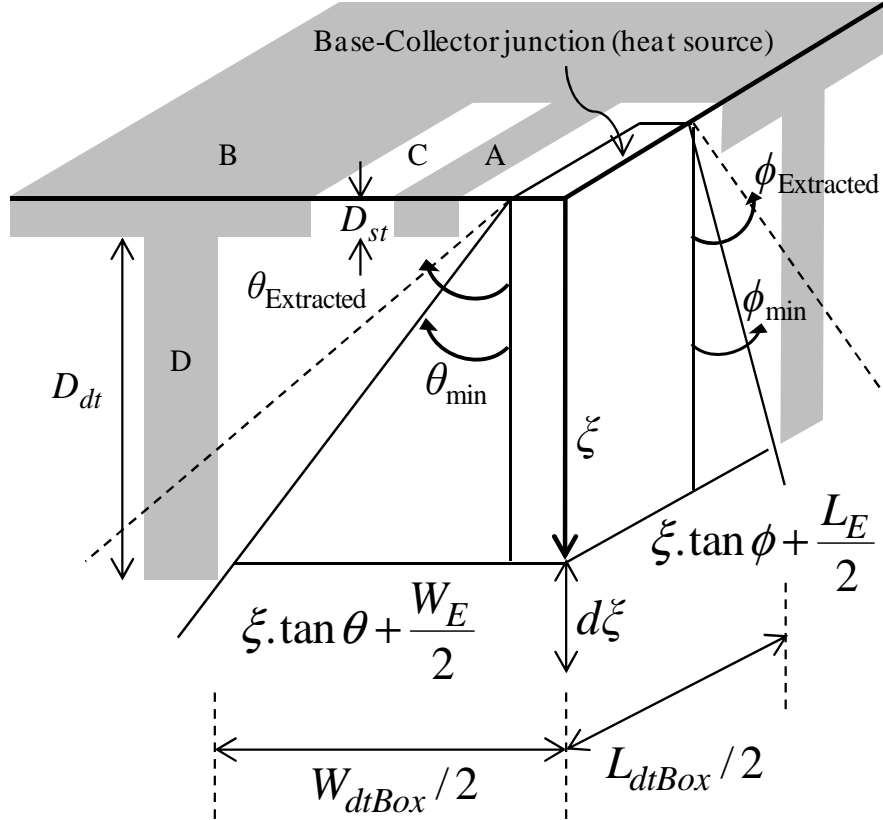


Figure 5-15: Pyramidal approximation of heat flux diffusion: The spreading angles θ and ϕ are defined by the deep trench height. A: Shallow trench, B: Thick SiO_2 layer, C: Space for Collector contact, D: Deep trench

According to *Figure 5-15*, the diffusion of the thermal flux has been approximated to be restrained to a pyramidal body region. Therefore, the area of an elementary surface at a distance ξ from heat source can be given by,

$$A(\xi) = (L_E + 2\xi \tan \theta) \cdot (W_E + 2\xi \tan \phi) = (L_E + a\xi) \cdot (W_E + b\xi) \quad \text{Eq. 5-11}$$

where,

$$a = 2 \tan \theta, b = 2 \tan \phi \quad \text{Eq. 5-12}$$

The minimum values of θ and ϕ are the angles made by deep trench towards Emitter length and width respectively as follows (*Figure 5-15*),

$$\tan \theta_{\min} = \frac{1}{2} \left(\frac{L_{dtBox} - L_E}{D_{st} + D_{dt}} \right), \quad \tan \phi_{\min} = \frac{1}{2} \left(\frac{W_{dtBox} - W_E}{D_{st} + D_{dt}} \right) \quad \text{Eq. 5-13}$$

L_{dtBox} and W_{dtBox} are the length and width of the Si-box region inside the deep trench as shown in Figure 5-15. D_{st} and D_{dt} are the height of the shallow trench and deep trench respectively. The extracted spreading angle can be given by,

$$\theta_{Extracted} = \theta_{\min} + \partial\theta, \quad \phi_{Extracted} = \phi_{\min} + \partial\phi \quad \text{Eq. 5-14}$$

where $\partial\theta$ and $\partial\phi$ are the fitting parameters for spreading angle. The thermal resistance and capacitance for the N^{th} recursive cell situated at a distance ξ from the heat source can be calculated by Eq. 5-1 as follows,

$$R_N(\xi) = \int_{\xi_N}^{\xi_{N+1}} \frac{d\xi}{\kappa A(\xi)} = \frac{1}{\kappa} \int_{\xi_N}^{\xi_{N+1}} \frac{d\xi}{(L_E + a\xi) \cdot (W_E + b\xi)} \quad \text{Eq. 5-15}$$

$$C_N(\xi) = \frac{\int_{\frac{(\xi_{N+1} + \xi_N)}{2}}^{\frac{(\xi_N + \xi_{N+1})}{2}} \frac{\kappa}{\alpha} A(\xi) d\xi}{\frac{(\xi_{N+1} + \xi_N)}{2}} = \frac{\kappa}{\alpha} \int_{\frac{(\xi_{N+1} + \xi_N)}{2}}^{\frac{(\xi_N + \xi_{N+1})}{2}} (L_E + a\xi) \cdot (W_E + b\xi) d\xi \quad \text{Eq. 5-16}$$

Therefore, for the N^{th} R-C cell, situated at a distance ξ from the heat source, the thermal resistance and capacitance is given by,

$$R_N(\xi) = \frac{1}{\kappa(aW_E - bL_E)} \cdot \ln \left(\frac{a\xi + L_E}{b\xi + W_E} \right) \Bigg|_{\xi_{N-1}}^{\xi_N} \quad \text{Eq. 5-17}$$

$$C_N(\xi) = \frac{\kappa}{6\alpha} \left[2ab\xi^3 + 3(aW_E + bL_E)\xi^2 + 6L_E W_E \xi \right] \Bigg|_{\left(\frac{\xi_{N-1} + \xi_N}{2}\right)}^{\left(\frac{\xi_N + \xi_{N+1}}{2}\right)} \quad \text{Eq. 5-18}$$

Here, κ (thermal conductivity), α (heat diffusion coefficient) are the physical parameters, a ($2 \tan\theta$) and b ($2 \tan\phi$) are function of the spreading angle θ and ϕ , and L_E and W_E are the device geometrical parameters.

5.5.2.1 Verification of the model with thermal TCAD simulations

5.5.2.1.1 Numerical Z_{TH} modeling

The numerically simulated magnitude and phase of the thermal impedance have been modeled with a recursive network where the elements of the network are calculated by Eq. 5-17

and Eq. 5-18. Nine recursive network cells have been used for the electro-thermal modeling. The position of each recursive cells are chosen according to the Eq. 5-2.

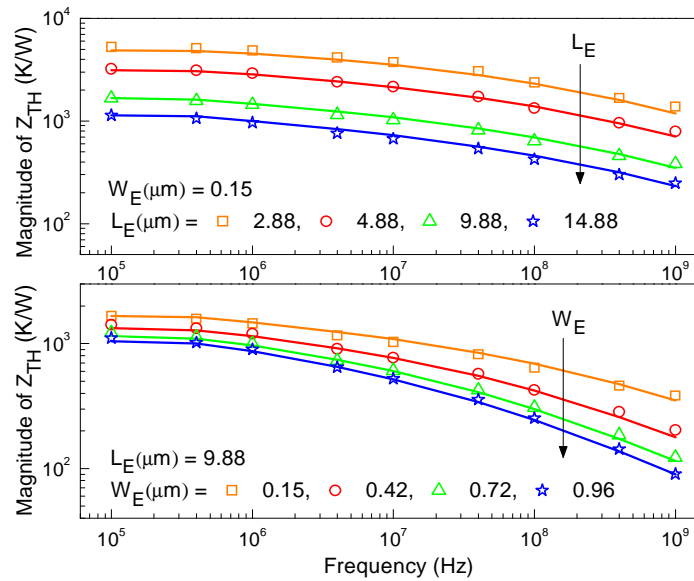


Figure 5-16: Magnitude of thermal impedance for different transistor geometries: comparison between numerical simulation (symbols) and compact simulation (solid lines) with electro-thermal recursive network with pyramidal approximation for the scaling rule.

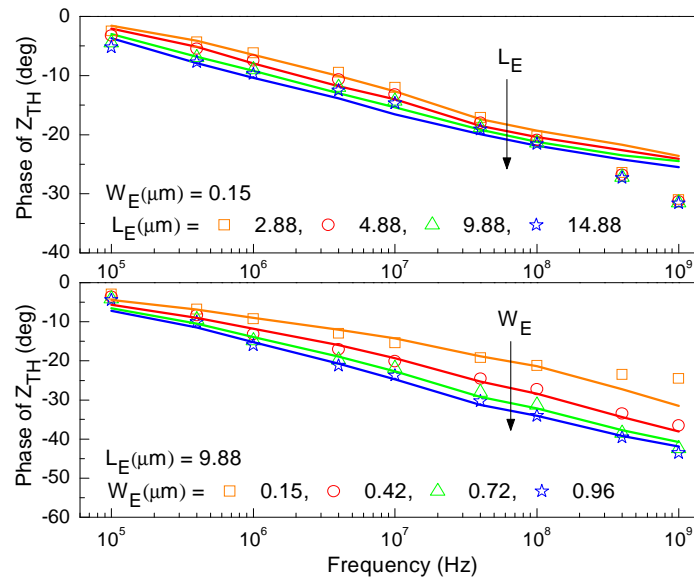


Figure 5-17: Phase of thermal impedance for different transistor geometries: comparison between numerical simulation (symbols) and compact simulation (solid lines) with electro-thermal recursive network with pyramidal approximation for the scaling rule.

The minimum values of the spreading angles (θ_{\min} and ϕ_{\min}) are calculated by Eq. 5-13 and the angle fitting parameters ($\hat{\partial}\theta$ and $\hat{\partial}\phi$) are optimized. $\hat{\partial}\theta$ and $\hat{\partial}\phi$, therefore, $\theta_{\text{Extracted}}$ and $\phi_{\text{Extracted}}$ are same for all the geometry of the devices. Figure 5-16 and Figure 5-17 give a comparison between numerical and recursive Z_{TH} for different transistor geometries. A very good agreement has been achieved over the whole geometry range (from very small transistors, e.g., $W_E = 0.15 \mu\text{m}$, $L_E = 2.88 \mu\text{m}$ to large transistors, e.g., $W_E = 0.96 \mu\text{m}$, $L_E = 9.88 \mu\text{m}$) and also on a large frequency range.

5.5.2.1.2 Numerical ΔT_J modeling

In order to verify the scalable model in time domain, large signal electro-thermal simulation has been performed applying a long pulse of electric power (pulse width = $5 \mu\text{s}$ and power = 2 mW) to reach steady state condition where the device temperature is equal to the DC temperature rise. The change in device temperature ΔT_J has been modeled with electro-thermal recursive network with pyramidal scaling rules given by Eq. 5-17 and Eq. 5-18. A good agreement has been achieved between numerical simulated data and the scalable recursive thermal network for variable length or width of the transistors as given in Figure 5-18.

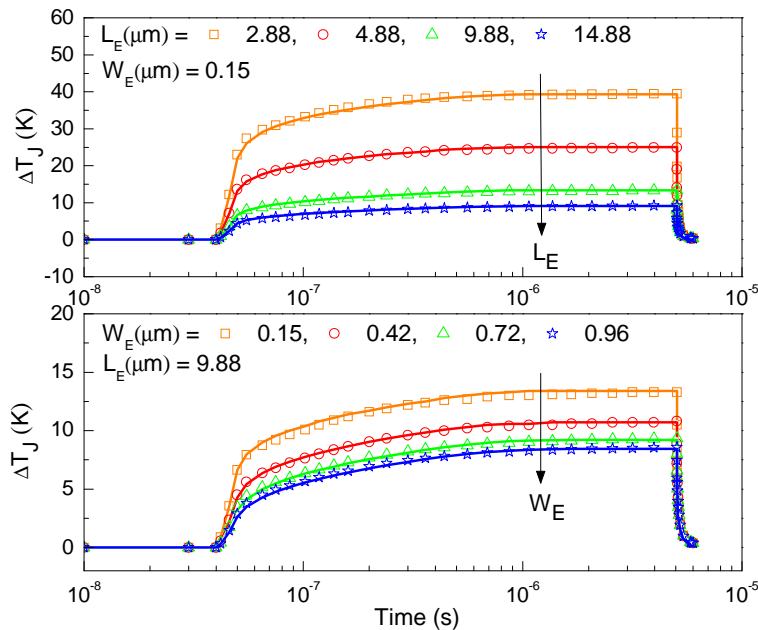


Figure 5-18: Device temperature rise (ΔT_J) for different transistor geometries : comparison between numerical simulation (symbols) and compact simulation (solid lines) with electro-thermal recursive network with pyramidal approximation for the scaling rule.

5.5.2.2 Verification of the model with low frequency s -parameter measurements

5.5.2.2.1 Z_{TH} modeling

The low frequency s -parameters have been measured at $V_{BE} = 0.95V$ and $V_{CE} = 1.5V$ bias condition for different transistor geometries. The measured s -parameters have been converted to y -parameters as given in *chapter – 2*. Following the approach from [11]; thermal impedance at low frequency has been obtained from y -parameters for different transistor geometries. This frequency domain thermal impedance has been modeled with an electro-thermal recursive network applying the pyramidal heat diffusion scaling rule and fitting the angle parameters ($\partial\theta$ and $\partial\phi$). The values of $\partial\theta$ and $\partial\phi$ are the same for all devices of the given technology. *Figure 5-19* shows a comparison between the magnitude of thermal impedances obtained from measurements and simulated with scalable thermal network. The phase of Z_{TH} vs. frequency for different geometries is shown on *Figure 5-20*. A good agreement can be observed over all transistor geometries. Despite the noisy measurement results, the global tendency of phase vs. frequency of the thermal impedance is well described.

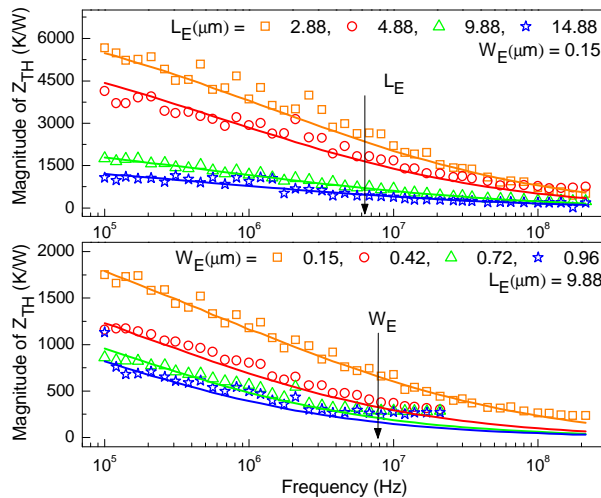


Figure 5-19: Frequency domain magnitude of Z_{TH} : comparison between measurements (symbols) and simulated (solid lines) with electro-thermal recursive network with pyramidal approximation for the scaling rule

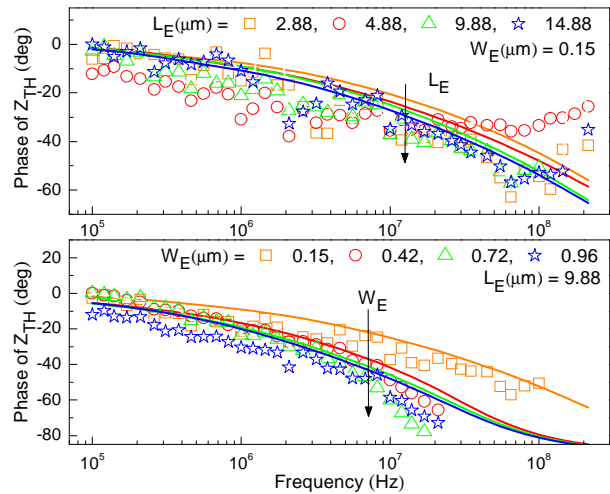


Figure 5-20: Frequency domain phase of Z_{TH} : comparison between measurements (symbols) and simulated (solid lines) with electro-thermal recursive network with pyramidal approximation for the scaling rule

Considering the device ($L_E \times W_E = 9.88 \times 0.15 \mu m^2$), it can be observed from the measured y_{12} parameter that the dynamic self-heating (decrease of y_{12}) takes place up to 200 MHz. The magnitude and phase of Z_{TH} could only be extracted up to $1/\tau_{thermal}$ (see *chapter 2* for

explanation). For instance, in *Figure 5-19* and *Figure 5-20*, the magnitude and phase of Z_{TH} of larger devices (different W_E) are obtained up to 20 MHz, while Z_{TH} of smaller devices (different L_E with minimum W_E) is extracted up to 200 MHz; but the simulation with the scalable model is shown up to 200 MHz.

5.5.2.2.2 y -parameters modeling

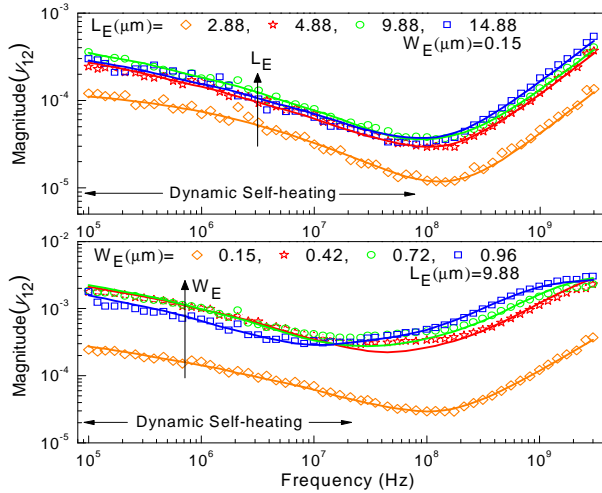


Figure 5-21: Thermal modeling of the magnitude of y_{12} parameter for different transistor geometries : comparison between measurements (symbols) and HiCuM compact model simulation with electro-thermal recursive network with pyramidal approximation for the scaling rule (solid lines).

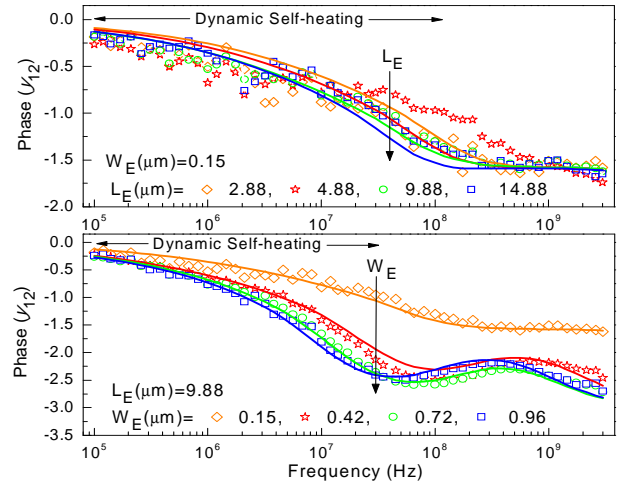


Figure 5-22: Thermal modeling of the phase of y_{12} parameter for different transistor geometries : comparison between measurements (symbols) and HiCuM compact model simulation with electro-thermal recursive network with pyramidal approximation for the scaling rule (solid lines).

In order to verify the scalability of the model, the electro-thermal network has been connected to the temperature node of HiCuM compact HBT model [12–15] for thermal modeling of y -parameters at low frequency. *Figure 5-21* and *Figure 5-22* show the magnitude and phase of the y_{12} parameter respectively. A comparison between measured and simulated y_{12} is presented for different L_E and W_E of the transistor. A very good agreement is observed using this scalable recursive pyramidal model. Moreover, the electro-thermal modeling with this scalable network needs to optimize only two angle fitting parameters (θ and ϕ). This can be achieved using commercial software like Agilent IC-CAP [16] with Levenberg-Marquardt algorithm [17].

TABLE 5-II gives a comparison between the extracted spreading angles $\theta_{\text{Extracted}}$ and $\phi_{\text{Extracted}}$ from numerical simulation and measurements. The extracted angles from simulation are lower than the extracted angles from measurements. According to *Eq. 5-17*, $R_N(\xi)$ of each cell

and, therefore, the overall thermal resistance R_{TH} decrease with spreading angle. In the TCAD simulation results (used here), the heat diffusion through the upper metal contact has not been taken into account. This can give a higher R_{TH} , i.e., lower spreading angles compared to measurements. A comparative study on the thermal resistance for different device structures (from the basic device taking only the lower part and deep trench and then adding shallow trench, SiGe base, polysilicon base contact, floating metal layer and thick SiO_2 layer surrounding the metal layer, etc.) has been carried out in the internal DOTFIVE report [18]. It has been shown that nearly 5% of the R_{TH} decrease is due to the back-end metallization for this given technology. Also, in the previous chapter (*chapter 4*) the influence of upper layers on R_{TH} and C_{TH} has been investigated. Simulating up to sixth metal layer, a significant decrease of R_{TH} and increase of C_{TH} is found compared to only “lower part” device simulation.

TABLE 5-II

Comparison of Heat spreading angle: extracted from measurements and numerical simulation.

Heat diffusing angle	Minimum value of the angles (θ_{min} and ϕ_{min}) (deg)	Extracted from numerical simulation (deg)	Extracted from measurements (deg)
θ	33.4	48.4	52.7
ϕ	10.7	15.8	19.5

5.5.2.3 Advantage of the model

The structure of the heat source is rectangular where the length is much greater than the width. In spherical heat diffusion model, the heat source is considered as the sum of m number of circles. The circles are placed successively along the L_E and the heat is dissipating from the center of each circle. Therefore, it has been seen that the scalability is valid for the different lengths but not for the width. The spreading angle (ϕ) may vary with different widths of the heat source. On the other hand in pyramidal heat diffusion model, heat dissipation occurs from the entire rectangular heat source. The spreading angles (θ and ϕ) depend on the distance between heat source and deep trench which is the same for all the devices for this technology. Therefore, the scalability of the model is valid for both different length and width of the heat source.

5.5.2.4 Convergence issues

Since several new nodes are added through the self-heating_network, the simulation time may suffer especially for transient simulations. The network has been verified with state of the

art ring oscillator circuits having 53, 106 and 212 CML cells with 106, 212 and 424 transistors, respectively. In our simulations, even for the maximum number of transistors (424) and the maximum number of recursive cells (20), no convergence issues have occurred.

5.5.2.5 Limitations of the model

The devices under analysis are the trench-isolated HBTs. The rectangular emitter window is surrounded by the shallow trench and the transistor is surrounded by the deep trench. The minimum values of the spreading angles are defined by the device geometrical parameters (D_{st} , D_{dt} , L_{dtBox} and W_{dtBox}). Also the structures of the transistors are symmetrical with 1 emitter, 2 base and 2 collector contacts. The parameters a and b in Eq. 5-17 and Eq. 5-18 depend on the spreading angles, i.e., the device geometrical parameters. Therefore, the scalability of this model is limited to symmetrical device architecture. The asymmetric structure will have a different heat spreading angle and, thus, more angle fitting parameters may be required.

5.6 Applications

In digital cellular base-station application, high linear device characteristics are mandatory. However, the distortion called thermal memory effect arises due the transient temperature variations of active devices and that are related with the time dependent envelope variation of modulated ratio signals [19]. In [19], it has been shown that a single pole electro-thermal RC network is insufficient to model accurately instantaneous temperature variations of the active devices. Therefore, a distributed network is needed. Moreover, this type of electro-thermal network can be used for accurate design of super linear microwave power amplifiers. In order to obtain an accurate estimation of the frequency domain dynamic electro-thermal device behavior and the time domain response for the short pulses in the range of the tenths of nanoseconds, a ladder-type electro-thermal network can provide more appropriate results [9].

5.7 Conclusion

The thermal parameters extracted from thermal TCAD simulations (*chapter – 4*) have been compared with different measurements (*chapter – 2*). This gives a very good compromise among different methods. Moreover, it has been found that the backend structure has a major impact on C_{TH} and therefore frequency domain Z_{TH} .

In next step, a scalable electro-thermal model for the transient self-heating effect in trench isolated Si-Ge HBTs has been presented. Two different approximated methods have been described to investigate the electro-thermal scalability of the device. The pyramidal heat diffusion model provides the best compromise among accuracy, number of model parameters and physical basement. The accuracy of the model has been verified with low frequency s-parameter measurements and thermal device simulations for various device geometries. Excellent agreement in time as well as frequency domain and simple parameter extraction methodology enable circuit optimization and a better prediction of circuit performance due to thermal issues for the circuit design engineers.

5.8 Reference:

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Summary of the work



General Conclusion

Micro and nano technologies tend towards the miniaturization of device to reach ultimate higher performances. The progress has been driven by the downscaling of the components in large-scale-integration. Moreover, power density of the transistor increases noteworthy due to the geometry shrinking. This significantly contributes to even higher device and system operational temperature. Thermal issue is one of the key factors limiting the performance and reliability of the devices and integrated circuits. Consequently, realistic thermal compact modeling is strongly mandatory in order to obtain accurate simulation results taking into account the intrinsic operating temperatures. The excessive temperature has underscored the need of thermal effect characterization in device compact models. An accurate determination of the device thermal impedance is required to specify operating temperature. Characterization of thermal phenomena is necessary for thermal stability and reliability analysis for modern bipolar circuits design.

In general, the heat conduction process in a system or device can be represented by a transmission line type network consisting of R_{TH} and C_{TH} . A variety of network topologies such as single pole network, Foster network, Nodal network, Cauer network and Recursive network are presented in the literature to scrutinize self-heating effects in electronic device. In the first chapter, we present a general overview of self-heating effect in electronic device. We demonstrate a brief description of different analytical models in combination with network topology which are described by many authors. In the next section of this chapter, a generalized equation for frequency domain thermal impedance of two port device has been formulated. This can be used to extract device thermal impedance from y , h and z – parameters in the frequency range below thermal cut-off frequency. A brief description on HBT compact model and the temperature effects in modeling have been described. HiCuM L2 HBT compact model with a scalable parameters library has been verified by static and dynamic characteristics. A good agreement has been shown. This parameter library has been used in steady state, transient and dynamic self-heating investigation.

In second chapter, an extensive evaluation of self-heating effect in trench isolated microwave HBTs is presented through different measurements and compact model simulations.

The characterizations are mostly based on steady state condition to extract R_{TH} and transient condition to extract C_{TH} . R_{TH} s of different geometries of transistors are extracted from DC characteristics, measured at different ambient temperatures. Different pulse measurement results are presented for the same transistors. The measurement setups like KEITHLEY 4200SCS PIVA and MC2 Technology APMS are described. In particular, we present a new and simple technique for accurate time domain characterization. The transient response of collector current has been measured accurately under optimized test conditions. Model parameters are extracted and validated through circuit simulations including an accurate transistor model in combination with the lumped elements of the measurement system. The methodology has been successfully applied to a wide range of transistor geometries. The thermal parameters are verified with DC measurements (for R_{TH}) and low frequency small signal measurements (for C_{TH}). We also present a simple methodology in order to extract the isothermal data from steady state characteristics. Therefore, output and Gummel characteristics are measured at the temperature between 0 and 100 °C. The extracted isothermal characteristics are verified through pulsed output and Gummel measurements. Frequency domain thermal spreading impedance of Si-Ge HBTs has been investigated and the thermal impedance characterized by $1/\sqrt{p}$ behavior has been modeled on a simple way by implementing the generalized and normalized thermal impedance equation in compact HiCuM model. The thermal behavior with different electro-thermal networks developed up to date has been verified with our measurement results. In comparison with the conventional single pole network, the recursive network provides the best compromise among accuracy, number of model parameters and physical point of view. Moreover, compact model simulation using the recursive network found to be in excellent agreement with measurements in time and frequency domain. The transient and low frequency measurements are performed at maximum 0.95V V_{BE} and 1.5V V_{CE} bias conditions. These bias conditions are very close to the peak f_T where self-heating is pronounced. In chapter 2, it has been seen that, the temperature of the intrinsic transistor reaches about 200°C (or more) at this bias condition.

In third chapter, the self-heating effect in nanometric CMOS device is presented through different measurements like static, pulse and DC & RF pulse. DC measurements are performed at different ambient temperatures and R_{TH} s of different geometries of transistors are extracted. The extraction methodology has been described in detail. Then, we present a new and simple methodology to extract isothermal data from I_D - V_{DS} and I_D - V_{GS} characteristic measured at

different ambient temperature. The isothermal data has been verified by pulse measurements. It has been seen that, 150 ns pulse width is not sufficient to reach isothermal characteristics. Device electrical performances and thermal behavior depending on bias region have been evaluated through different transient measurements. DC and RF pulse characterization has been carried out at different DC and RF pulse width. Due to smaller R_{TH} value of this device, no difference is found in the applied pulse width range. Finally, it can be conclude from the different characterizations that, sensitivity of this device to self-heating is small.

It has been seen from the different characterizations of BiCMOS SiGe HBTs and nanometric MOSFETs as described in *Chapter 2* and *3* that, the measured HBT is much more sensitive than the CMOS one. Thus, in order to perform the thermal device simulations, we have selected the SiGe HBT structure.

In the forth chapter, three dimensional thermal TCAD simulations are performed on a submicron SiGe:C BiCMOS technology in order to investigate the transient and the dynamic behavior of the device temperature in dependence of the device architecture and material properties. The structure of the transistors is same as the measured one. Different optimizations are performed precisely including mesh refinement, simulation domain and power densities. In the first attempt, the simplified “lower part” structures for several device geometries are simulated. Large signal transient simulations are performed to obtain time domain junction temperature variations while frequency domain thermal impedance is extracted from sinusoidal transient simulation. $T_{Lattice}$ and F_{Heat} distribution inside the device at different pulse time are studied. R_{THS} and C_{THS} are extracted through electro-thermal modeling. Two different networks are compared in terms of accuracy in modeling and parameter extraction. In comparison with the conventional single pole network, the recursive network provides the best compromise among accuracy, number of model parameters and physical basement. Finally, a complete device structure has been built including different back-end process layers e.g. SiGe – Base, Poly Si – Base with a cobalt layer, Y – shape Emitter, Emitter poly Si, Emitter – Base – Collector metal contacts and metal layers (up to 6 metal). The impact of back-end layers on junction temperature and, therefore, on thermal parameters are investigated. The heat flow through the metal contacts causes a significant decrease in R_{TH} . Moreover, it has been found that, the backend structure has

a major impact on C_{TH} and, therefore, on frequency domain Z_{TH} . Finally, the dependence of C_{TH} with back-end demonstrates that the extracted value is layout dependant.

The thermal parameters extracted from different measurements (*chapter – 2*) and thermal TCAD simulations (*chapter – 4*) are compared in *chapter – 5*. The different methods are verified and show consistent results. Moreover, it has been found that the backend structure has a major impact on C_{TH} and therefore frequency domain Z_{TH} . In the next step, a scalable electro-thermal model for the transient self-heating effect in trench isolated Si-Ge HBTs has been presented. Two different approximated methods have been described to investigate the electro-thermal scalability of the device. The pyramidal heat diffusion model provides the best compromise among accuracy, number of model parameters and physical basement. The accuracy of the model has been verified with low frequency s-parameter measurements and thermal device simulations for various device geometries. Excellent agreement in time as well as frequency domain and simple parameter extraction methodology provides a better prediction of circuit performance due to thermal issues for the design engineers.

Perspectives

This work explores and investigates the self-heating behavior in advanced SiGe:C BiCMOS HBT and nanometric CMOS transistors through different measurements, modeling and device simulations. We have presented various new methodologies and these are validated through different well known existing techniques. We intend to point out that, some of the works need improvement to make them more generalized. These are as follows:

❖ In *chapter – 2* and *3*, a simplified technique is demonstrated in order to extract isothermal data. This methodology is valid only for steady state characteristics and when the variation of I_C is linear with temperature. The method is not very accurate since the range of temperature is too low. In case of measurements at wide temperature range, the devices with larger value of R_{TH} and the devices which present nonlinear behavior of I_C with temperature, this method may not properly work. Therefore, in order to make the methodology more generalized, instead of linear extrapolation a quadratic extrapolation may be needed. Moreover, R_{TH} of a device depends on temperature and also P_{diss} as the thermal conductivity of Si is strongly depend on temperature. Therefore, instead of using a single R_{TH} , a temperature/power density dependent R_{TH} model can give better isothermal data and may valid for all P_{diss} range.

Hence, new extraction method needs to be developed in order to extract the R_{TH} temperature dependence. Of course, this temperature dependence have to be used for compact modeling since temperature variation within a device can reach more than 200°C at maximum biasing conditions.

❖ In *chapter – 4*, steady state, transient and dynamic thermal behavior has been investigated through 3D TCAD simulations. The simulations are performed including up to 6 metallization layers. Since the devices in measurement and in circuit configuration have a different back end structure, some strong modeling inaccuracy may appear for circuit simulation. Up to now, this point has not been considered in HBT modeling. Hence, new layout tools, such as the one used for back-end electrical parasitic element calculation, may be considered for R_{TH} evaluation.

❖ In *Chapter – 5*, a scalable electro-thermal model has been presented. This model also has been verified through measurements and simulations and a good agreement is found. But, the

scalability of this model is limited to the symmetrical device architecture like CBEBC. Therefore the model needs to be improved for a more general asymmetric structure.

Appendix – A: Theoretical formulation

In Cartesian coordinate system the heat flow equation it is described by,

$$\nabla^2 T = \frac{c\rho}{\lambda_{th}} \frac{\partial T}{\partial t} \quad \text{Eq. A-1}$$

In order to process the analytical solution of this problem, simplifications and approximations are required. Here, the solution of the above equation is described for a bidimensional axisymmetric structure, as presented by Mnif et al. in [1].

❖ Assumptions and approximations

- The transistor is represented by a parallelepiped volume element with a rectangular heat source at the top surface as shown in *Figure A-1*. The four sides and the top surface are considered adiabatic, therefore, no heat exchange with the external environment. This simplified assumption is reasonable due to insulated trench walls around the transistor structure, which is formed by SiO_2 , a very poor conductor of heat. The temperature of the adiabatic walls can be assumed same as surrounding temperature ($T = T_\infty$) [2], [3].
- The temperature dependent non-linearity of the thermal conductivity create major problem in differential equation that it cannot be solved analytically. Therefore, in the range of temperature due to self-heating of the component, conductivity is taken to be constant [4], [5].
- A three dimensional treatment of the device thermal behavior is necessary due to the isotropic nature of the thermal conductivity. But for the sake of simplification, the heat equation can be solved in cylindrical coordinate system, where the heat source is modeled by a disc with radius r_0 as shown in *Figure A-1*.

$$r_0 = \frac{WL}{\pi} \quad \text{Eq. A-2}$$

Here W and L are the width and the length of the emitter window respectively.

- Due to the symmetry of the problem (independent of θ), heat transfer have bidimensional axisymmetric geometry (depends on r and z). Therefore the heat transfer equation (*Eq. A-1*) can be transformed in cylindrical coordinates as,

$$\frac{\partial^2 T}{\partial r^2} + \frac{1}{r} \frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2} = \frac{1}{a} \frac{\partial T}{\partial t} \quad \text{Eq. A-3}$$

where, $a = \lambda_{th}/c\rho$ is called thermal diffusivity expressed in m^2/s .

❖ Boundary conditions

- The symmetry involves directly that the temperature in the r - θ plane is maximum at $r=0$, Thus,

$$\frac{\partial T}{\partial r} = 0 \quad \text{for } r = 0 \quad \text{Eq. A-4}$$

- For the special case of an ideal heat sink, Dirichlet boundary condition gives,

$$T = T_{\infty} \quad \text{for } z \rightarrow \infty \quad \text{and } r \rightarrow \infty \quad \text{Eq. A-5}$$

where T_{∞} represents the ambient temperature.

- A variable heat flow is applied within the active region at the top surface,

$$-\lambda \frac{\partial T}{\partial z} = q(r, t) \quad \text{for } z = 0 \quad \text{and } 0 < r < r_0 \quad \text{Eq. A-6}$$

$q(r, t)$ represents the heat flow density and given in W/m^2 .

- No heat flow is assumed outside the active region at top surface,

$$-\lambda \frac{\partial T}{\partial z} = 0 \quad \text{for } z = 0 \quad \text{and } r > r_0 \quad \text{Eq. A-7}$$

The last two conditions describe the Fourier law.

❖ Initial conditions

This condition is necessary for studying transient state response. At $t = 0$, $T = T_{\infty}$ throughout the system.

❖ Analytical problem resolution

Self-heating is expressed by a rise of the device temperature, $T_{rise} = T - T_{\infty}$. In this approach the transient thermal impedance is calculated which corresponds to the step response. The transient thermal impedance fully characterizes the thermal properties of the component.

The junction temperature of the device can be described in terms of thermal impedance and power dissipation as follows,

$$T_{rise}(t) = P_{diss} Z_{TH}(t) \quad \text{Eq. A-8}$$

Now the heat transfer equation (Eq.) in cylindrical coordinates for the transient temperature can be given by,

$$\frac{\partial^2 T_{rise}(r, z, t)}{\partial r^2} + \frac{1}{r} \frac{\partial T_{rise}(r, z, t)}{\partial r} + \frac{\partial^2 T_{rise}(r, z, t)}{\partial z^2} = \frac{1}{a} \frac{\partial T_{rise}(r, z, t)}{\partial t} \quad \text{Eq. A-9}$$

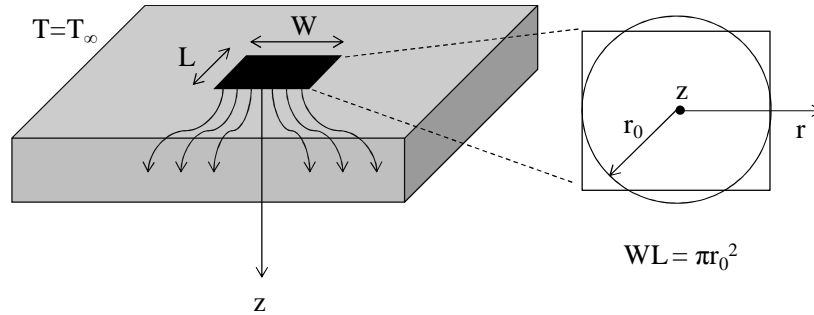


Figure A-1: The transistor – described by a parallelepiped volume element with a rectangular heat source at the top surface.

❖ Solution in frequency domain

Laplace transform of $T_{rise}(r, z, t)$:

$$L\langle T_{rise}(r, z, t) \rangle = \theta_{rise}(r, z, p) = \int_0^{\infty} T_{rise}(r, z, t) \exp(-pt) dt \quad \text{Eq. A-10}$$

where p is the Laplace variable. Thus the heat transfer equation in Laplace domain can be expressed as,

$$\frac{p}{a} \theta_{rise}(r, z, p) - T_{rise}(r, z, t=0) - \frac{\partial^2 \theta_{rise}(r, z, p)}{\partial r^2} - \frac{1}{r} \frac{\partial \theta_{rise}(r, z, p)}{\partial r} - \frac{\partial^2 \theta_{rise}(r, z, p)}{\partial z^2} = 0 \quad \text{Eq. A-11}$$

With $T_{rise}(r, z, t=0) = 0$ is the initial condition and the boundary condition is given by,

$$\frac{\partial \theta_{rise}(r, z, p)}{\partial r} = 0 \quad \text{at} \quad r = 0 \quad \text{Eq. A-12}$$

The differential equation given above can be solved using Hankel transform due to the cylindrical symmetry. This transform allows reducing the system to one space variable along the axis of symmetry. Hankel transform of zero order of a function $\theta_{rise}(r, z, p)$ symmetric around the z axis is defined by:

$$H_0(\theta_{rise}(r, z, p)) = \hat{\theta}_{rise}(r, z, p) = \int_0^{\infty} \theta_{rise}(r, z, p) J_0(\gamma r) r dr \quad Eq. A-13$$

with γ is the Hankel variable and J_0 is the zero order Bessel function.

Now applying Hankel transform of zero order in Eq. A-11,

$$\frac{p}{a} H_0(\theta_{rise}(r, z, p)) - H_0\left(\frac{\partial^2 \theta_{rise}(r, z, p)}{\partial r^2} + \frac{1}{r} \frac{\partial \theta_{rise}(r, z, p)}{\partial r}\right) - H_0\left(\frac{\partial^2 \theta_{rise}(r, z, p)}{\partial z^2}\right) = 0 \quad Eq. A-14$$

Introducing the following Hankel property,

$$H_0\left(\frac{\partial^2 \theta_{rise}(r, z, p)}{\partial r^2} + \frac{1}{r} \frac{\partial \theta_{rise}(r, z, p)}{\partial r}\right) = \gamma^2 H_0(\theta_{rise}(r, z, p)) \quad Eq. A-15$$

Eq. A-14 becomes:

$$\frac{\partial^2 \hat{\theta}_{rise}(\gamma, z, p)}{\partial z^2} - \frac{p}{a} \hat{\theta}_{rise}(\gamma, z, p) - \gamma^2 \hat{\theta}_{rise}(\gamma, z, p) = 0 \quad Eq. A-16$$

and the heat transform differential equation becomes,

$$\frac{\partial^2 \hat{\theta}_{rise}(\gamma, z, p)}{\partial z^2} - \delta^2 \hat{\theta}_{rise}(\gamma, z, p) = 0 \quad Eq. A-17$$

where,

$$\delta = \left(\frac{p}{a} + \gamma^2\right)^{\frac{1}{2}} \quad Eq. A-18$$

The solution of equation 3 has the following form:

$$\hat{\theta}_{rise}(\gamma, z, p) = A \exp(\delta z) + B \exp(-\delta z) \quad Eq. A-19$$

Boundary condition:

$$T_{rise} = 0 \quad \text{for } z \rightarrow \infty, \quad A = 0 \quad \text{Eq. A-20}$$

Therefore, the solution will be,

$$\hat{\theta}_{rise}(\gamma, z, p) = B \exp(-\delta z) \quad \text{Eq. A-21}$$

Derivative of Eq. A-21,

$$\frac{\partial \hat{\theta}_{rise}(\gamma, z, p)}{\partial z} = -\delta B \exp(-\delta z) \quad \text{Eq. A-22}$$

Applying the double transform of Laplace and Hankel on the boundary condition,

$$-\lambda \frac{\partial T}{\partial z} = q(r, t) \quad \text{for } z = 0 \text{ and } 0 < r < r_0 \quad \text{Eq. A-23}$$

we can obtain, Laplace transforms:

$$-\lambda \frac{\partial \theta_{rise}(\gamma, z = 0, p)}{\partial z} = L\langle q(r, p) \rangle = \tilde{q}(r, p) \quad \text{Eq. A-24}$$

and Hankel transforms:

$$-\lambda \frac{\partial \hat{\theta}_{rise}(\gamma, z = 0, p)}{\partial z} = \hat{q}(\gamma, p) \quad \text{Eq. A-25}$$

The Hankel transform according to r and the Laplace transform according to t such as:

$$\hat{q}(\gamma, p) = \int_{r=0}^{r_0} \tilde{q}(r, p) J_0(\gamma r) r dr \quad \text{Eq. A-26}$$

Due to the boundary condition, integration from 0 to ∞ can be limited to 0 to r_0 . Comparing Eq. A-22 and Eq. A-25,

$$B = \frac{1}{\lambda \delta} \hat{q}(\gamma, p) \quad \text{Eq. A-27}$$

Finally the solution of the Eq. A-17 is given by,

$$\hat{\theta}_{rise}(\gamma, z, p) = \frac{\hat{q}(\gamma, p)}{\lambda \delta} \exp(-\delta z) \quad \text{Eq. A-28}$$

The temperature rise in Laplace domain is obtained by the inverse Hankel transform:

$$\theta_{rise}(\gamma, z, p) = \int_0^{\infty} \frac{\hat{q}(\gamma, p)}{\lambda \delta} \exp(-\delta z) J_0(\gamma r) \gamma d\gamma \quad \text{Eq. A-29}$$

Introducing the mean value of Laplace transform over the disc shape heat source at $z = 0$ plane,

$$\begin{aligned} \bar{\theta}_{rise}(z=0, p) &= \frac{1}{\pi r_0^2} \int_0^{2\pi} \int_0^{r_0} \theta_{rise}(r, z=0, p) r dr d\theta \\ &= \frac{2}{r_0^2} \int_0^{r_0} \theta_{rise}(r, z=0, p) r dr \\ &= \frac{2}{r_0^2} \int_0^{r_0} \int_0^{\infty} \frac{\hat{q}(\gamma, p)}{\lambda \delta} J_0(\gamma r) \gamma d\gamma r dr \\ &= \frac{2}{\lambda r_0^2} \int_0^{\infty} \left[\int_0^{r_0} J_0(\gamma r) r dr \right] \hat{q}(\gamma, p) \frac{\gamma}{\delta} d\gamma \\ &= \frac{2}{\lambda r_0^2} \int_0^{\infty} \hat{q}(\gamma, p) \frac{J_1(\gamma r_0)}{\delta} d\gamma \end{aligned} \quad \text{Eq. A-30}$$

by using the integral properties of Bessel function. From Eq. A-26 and assuming $\tilde{q}(r, p)$ uniformly distributed over the heat source,

$$\begin{aligned} \hat{q}(\gamma, p) &= \tilde{q}_0(p) \int_{r=0}^{r_0} J_0(\gamma r) r dr \\ \hat{q}(\gamma, p) &= \tilde{q}_0(p) r_0 \frac{J_1(\gamma r_0)}{\gamma} \end{aligned} \quad \text{Eq. A-31}$$

Eq. A-30 becomes:

$$\bar{\theta}_{rise}(p) = \frac{2}{\lambda r_0^2} \int_0^{\infty} \hat{q}_0(p) r_0^2 \frac{J_1^2(\gamma r_0)}{\gamma \delta} d\gamma \quad \text{Eq. A-32}$$

Otherwise, the mean value of the total thermal power at $z = 0$ is given by (no heat flow outside the disc and therefore integration boundary is limited at r_0):

$$\bar{\Phi}(z=0, p) = \int_0^{2\pi} \int_0^{r_0} \tilde{q}(r, z=0, p) r dr d\theta = \pi r_0^2 \tilde{q}_0(p) \quad \text{Eq. A-33}$$

The thermal impedance can be calculated using Eq. A-32 and Eq. A-33:

$$\begin{aligned}
 Z_{TH}(p) &= \frac{\bar{\theta}_{rise}(p)}{\bar{\Phi}(p)} \\
 &= \frac{\frac{2}{\lambda r_0^2} \int_0^\infty \tilde{q}_0(p) r_0^2 \frac{J_1^2(\gamma r_0)}{\gamma \delta} d\gamma}{\pi r_0^2 \tilde{q}_0(p)} \\
 &= \frac{2}{\lambda \pi r_0^2} \int_0^\infty \frac{J_1^2(\gamma r_0)}{\gamma \delta} d\gamma
 \end{aligned} \tag{Eq. A-34}$$

Considering the variable, $\varepsilon = \gamma r_0$ and using the Eq. A-18,

$$Z_{TH}(p) = \frac{2}{\lambda \pi r_0^2} \int_0^\infty \frac{J_1^2(\varepsilon)}{\varepsilon \sqrt{\varepsilon^2 + \frac{p r_0^2}{a}}} d\varepsilon \tag{Eq. A-35}$$

According to its temporal state, Z_{TH} can be distinguished into two different expressions:

I. In steady state, $t \rightarrow \infty$, $p \rightarrow 0$, therefore,

$$\begin{aligned}
 Z_{TH}(p) &= \frac{2}{\lambda \pi r_0^2} \int_0^\infty \frac{J_1^2(\varepsilon)}{\varepsilon^2} d\varepsilon \\
 Z_{TH}(p) &\rightarrow \frac{8}{3\pi^2 \lambda r_0^2} = R_{TH}
 \end{aligned} \tag{Eq. A-36}$$

where,

$$\int_0^\infty \frac{J_1^2(\varepsilon)}{\varepsilon^2} d\varepsilon = \frac{4}{3\pi} \tag{Eq. A-37}$$

The thermal impedance can be modeled by a single thermal resistance (R_{TH}).

II. In transient state, $t \rightarrow 0$, $p \rightarrow \infty$ and therefore,

$$Z_{TH}(p) \rightarrow \frac{1}{\sqrt{\lambda \rho c} (\sqrt{p \pi r_0^2})} = Z_{trans} \tag{Eq. A-38}$$

where

$$\int_0^\infty \frac{J_1^2(\varepsilon)}{\varepsilon} d\varepsilon = \frac{1}{2} \tag{Eq. A-39}$$

The Eq. A-38 can be rewritten with Eq. A-36 as,

$$Z_{TH}(p) \rightarrow \sqrt{\frac{R_{TH}}{pC_{TH}}} \quad \text{Eq. A-40}$$

where ,

$$C_{TH} = \frac{8}{3} \rho c r_0^2 \quad \text{Eq. A-41}$$

represents the equivalent thermal capacitance.

Thus the total thermal impedance can be represented by electrical equivalent circuit diagram as shown in *Figure A-2 (chapter - 1)* and which is modeled by,

$$Z_{TH}(p) \approx \frac{1}{\frac{1}{Z_{trans}} + \frac{1}{R_{TH}}} = \frac{R_{TH}}{(1 + \sqrt{pR_{TH}C_{TH}})} \quad \text{Eq. A-42}$$

The thermal impedance in time domain is achieved by inverse Laplace transform of $Z_{TH}(p)$,

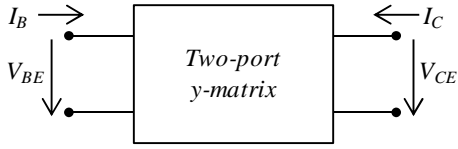
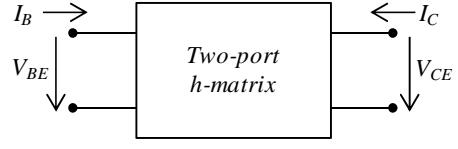
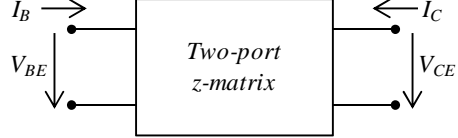
$$Z_{TH}(t) = L^{-1}\{Z_{TH}(p)\} = R_{TH} \left[1 - \exp\left(\frac{t}{R_{TH}C_{TH}}\right) \operatorname{erfc}\left(\sqrt{\frac{t}{R_{TH}C_{TH}}}\right) \right] \quad \text{Eq. A-43}$$

From *Eq. A-8*, the device junction temperature rise is given by,

$$T_{rise}(t) = R_{TH} P_{diss} \left[1 - \exp\left(\frac{t}{R_{TH}C_{TH}}\right) \operatorname{erfc}\left(\sqrt{\frac{t}{R_{TH}C_{TH}}}\right) \right] \quad \text{Eq. A-44}$$

Appendix – B: Z_{TH} calculations from h and z parameters

The two port matrix relates the voltages and currents of the two port device. For a two port device the y , h and z matrices can be given by following relations [6]:

Parameter	Matrix	Two port block diagram for HBT
y	$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} * \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}$	
h	$\begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} * \begin{pmatrix} I_1 \\ V_2 \end{pmatrix}$	
z	$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{pmatrix} * \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}$	

Therefore, the voltages and currents can be described by the following algebraic equations:

$$\begin{aligned} I_1 &= y_{11}V_1 + y_{12}V_2 & V_1 &= h_{11}I_1 + h_{12}V_2 & \text{and} & & V_1 &= z_{11}I_1 + z_{12}I_2 \\ I_2 &= y_{21}V_1 + y_{22}V_2 & I_2 &= h_{21}I_1 + h_{22}V_2 & & & V_2 &= z_{21}I_1 + z_{22}I_2 \end{aligned} \quad \text{Eq. B-1}$$

❖ Z_{TH} from h -parameter:

$$\begin{aligned} V_1 &= F_1(I_1, V_2, T_J) = F_1^{DC}(I_1, V_2, T_i) \\ I_2 &= F_2(I_1, V_2, T_J) = F_2^{DC}(I_1, V_2, T_i) \end{aligned} \quad \text{Eq. B-2}$$

$$\begin{aligned} h_{11}(\omega) &= \left. \frac{\partial F_1}{\partial I_1} \right|_{\substack{\text{non-equithermal} \\ \Delta V_2=0}} = \left. \frac{\partial F_1}{\partial I_1} \right|_{\text{equithermal}} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial I_1} = h_{11}^{AC} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial I_1} \\ h_{12}(\omega) &= \left. \frac{\partial F_1}{\partial V_2} \right|_{\substack{\text{non-equithermal} \\ \Delta I_1=0}} = \left. \frac{\partial F_1}{\partial V_2} \right|_{\text{equithermal}} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} = h_{12}^{AC} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} \\ h_{21}(\omega) &= \left. \frac{\partial F_2}{\partial I_1} \right|_{\substack{\text{non-equithermal} \\ \Delta V_2=0}} = \left. \frac{\partial F_2}{\partial I_1} \right|_{\text{equithermal}} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial I_1} = h_{21}^{AC} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial I_1} \end{aligned}$$

$$h_{22}(\omega) = \left. \frac{\partial F_2}{\partial V_2} \right|_{\substack{\text{non-equithermal} \\ \Delta I_1=0}} = \left. \frac{\partial F_2}{\partial V_2} \right|_{\text{equithermal}} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} = h_{22}^{AC} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} \quad \text{Eq. B-3}$$

$$\left. \frac{\partial T_J}{\partial I_1} \right|_{\Delta V_2=0} = Z_{th} \left(V_1 + I_1 \frac{\partial V_1}{\partial I_1} + V_2 \frac{\partial I_2}{\partial I_1} \right) = Z_{th} (V_1 + I_1 h_{11} + V_2 h_{21}) \quad \text{Eq. B-4}$$

$$\left. \frac{\partial T_J}{\partial V_2} \right|_{\Delta I_1=0} = Z_{th} \left(I_2 + I_1 \frac{\partial V_1}{\partial V_2} + V_2 \frac{\partial I_2}{\partial V_2} \right) = Z_{th} (I_2 + I_1 h_{12} + V_2 h_{22})$$

$$Z_{th}^{11}(\omega) = \frac{(h_{11}(\omega) - h_{11}^{AC})}{\frac{\partial F_1}{\partial T_J} (V_1 + I_1 h_{11}(\omega) + V_2 h_{21}(\omega))} \Rightarrow Z_{th}^{11}(0) = \frac{(h_{11}^{DC} - h_{11}^{AC})}{\frac{\partial F_1}{\partial T_J} (V_1 + I_1 h_{11}^{DC} + V_2 h_{21}^{DC})}$$

$$Z_{th}^{12}(\omega) = \frac{(h_{12}(\omega) - h_{12}^{AC})}{\frac{\partial F_1}{\partial T_J} (I_2 + I_1 h_{12}(\omega) + V_2 h_{22}(\omega))} \Rightarrow Z_{th}^{12}(0) = \frac{(h_{12}^{DC} - h_{12}^{AC})}{\frac{\partial F_1}{\partial T_J} (I_2 + I_1 h_{12}^{DC} + V_2 h_{22}^{DC})}$$

$$Z_{th}^{21}(\omega) = \frac{(h_{21}(\omega) - h_{21}^{AC})}{\frac{\partial F_2}{\partial T_J} (V_1 + I_1 h_{11}(\omega) + V_2 h_{21}(\omega))} \Rightarrow Z_{th}^{21}(0) = \frac{(h_{21}^{DC} - h_{21}^{AC})}{\frac{\partial F_2}{\partial T_J} (V_1 + I_1 h_{11}^{DC} + V_2 h_{21}^{DC})}$$

$$Z_{th}^{22}(\omega) = \frac{(h_{22}(\omega) - h_{22}^{AC})}{\frac{\partial F_2}{\partial T_J} (I_2 + I_1 h_{12}(\omega) + V_2 h_{22}(\omega))} \Rightarrow Z_{th}^{22}(0) = \frac{(h_{22}^{DC} - h_{22}^{AC})}{\frac{\partial F_2}{\partial T_J} (I_2 + I_1 h_{12}^{DC} + V_2 h_{22}^{DC})}$$

$$Z_{thN}^{11}(\omega) = \frac{Z_{th}^{11}(\omega)}{Z_{th}^{11}(0)} = \frac{(h_{11}(\omega) - h_{11}^{AC})}{(h_{11}^{DC} - h_{11}^{AC})} \cdot \frac{(V_1 + I_1 h_{11}^{DC} + V_2 h_{21}^{DC})}{(V_1 + I_1 h_{11}(\omega) + V_2 h_{21}(\omega))}$$

$$Z_{thN}^{12}(\omega) = \frac{Z_{th}^{12}(\omega)}{Z_{th}^{12}(0)} = \frac{(h_{12}(\omega) - h_{12}^{AC})}{(h_{12}^{DC} - h_{12}^{AC})} \cdot \frac{(I_2 + I_1 h_{12}^{DC} + V_2 h_{22}^{DC})}{(I_2 + I_1 h_{12}(\omega) + V_2 h_{22}(\omega))}$$

$$Z_{thN}^{21}(\omega) = \frac{Z_{th}^{21}(\omega)}{Z_{th}^{21}(0)} = \frac{(h_{21}(\omega) - h_{21}^{AC})}{(h_{21}^{DC} - h_{21}^{AC})} \cdot \frac{(V_1 + I_1 h_{11}^{DC} + V_2 h_{21}^{DC})}{(V_1 + I_1 h_{11}(\omega) + V_2 h_{21}(\omega))}$$

$$Z_{thN}^{22}(\omega) = \frac{Z_{th}^{22}(\omega)}{Z_{th}^{22}(0)} = \frac{(h_{22}(\omega) - h_{22}^{AC})}{(h_{22}^{DC} - h_{22}^{AC})} \cdot \frac{(I_2 + I_1 h_{12}^{DC} + V_2 h_{22}^{DC})}{(I_2 + I_1 h_{12}(\omega) + V_2 h_{22}(\omega))}$$

$$Z_{thN}^{ij}(\omega) = \begin{cases} \frac{(h_{ij}(\omega) - h_{ij}^{AC})}{(h_{ij}^{DC} - h_{ij}^{AC})} \cdot \frac{(V_j + I_j h_{jj}^{DC} + V_{j+1} h_{j+1,j}^{DC})}{(V_j + I_j h_{jj}(\omega) + V_{j+1} h_{j+1,j}(\omega))}, & \text{for } i=1,2 \text{ and } j=1 \\ \text{or} \\ \frac{(h_{ij}(\omega) - h_{ij}^{AC})}{(h_{ij}^{DC} - h_{ij}^{AC})} \cdot \frac{(I_j + V_{j-1} h_{j-1,j}^{DC} + I_j h_{jj}^{DC})}{(I_j + V_{j-1} h_{j-1,j}(\omega) + I_j h_{jj}(\omega))}, & \text{for } i=1,2 \text{ and } j=2 \end{cases} \quad \text{Eq. B-7}$$

❖ Z_{TH} from z -parameter:

$$\begin{aligned} V_1 &= F_1(I_1, V_2, T_J) = F_1^{DC}(I_1, V_2, T_i) \\ I_2 &= F_2(I_1, V_2, T_J) = F_2^{DC}(I_1, V_2, T_i) \end{aligned} \quad \text{Eq. B-8}$$

$$\begin{aligned} h_{11}(\omega) &= \left. \frac{\partial F_1}{\partial I_1} \right|_{\substack{\text{non-equithermal} \\ \Delta V_2=0}} = \left. \frac{\partial F_1}{\partial I_1} \right|_{\text{equithermal}} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial I_1} = h_{11}^{AC} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial I_1} \\ h_{12}(\omega) &= \left. \frac{\partial F_1}{\partial V_2} \right|_{\substack{\text{non-equithermal} \\ \Delta I_1=0}} = \left. \frac{\partial F_1}{\partial V_2} \right|_{\text{equithermal}} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} = h_{12}^{AC} + \frac{\partial F_1}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} \\ h_{21}(\omega) &= \left. \frac{\partial F_2}{\partial I_1} \right|_{\substack{\text{non-equithermal} \\ \Delta V_2=0}} = \left. \frac{\partial F_2}{\partial I_1} \right|_{\text{equithermal}} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial I_1} = h_{21}^{AC} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial I_1} \\ h_{22}(\omega) &= \left. \frac{\partial F_2}{\partial V_2} \right|_{\substack{\text{non-equithermal} \\ \Delta I_1=0}} = \left. \frac{\partial F_2}{\partial V_2} \right|_{\text{equithermal}} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} = h_{22}^{AC} + \frac{\partial F_2}{\partial T_J} \cdot \frac{\partial T_J}{\partial V_2} \end{aligned} \quad \text{Eq. B-9}$$

$$\begin{aligned} \left. \frac{\partial T_J}{\partial I_1} \right|_{\Delta V_2=0} &= Z_{th} \left(V_1 + I_1 \frac{\partial V_1}{\partial I_1} + V_2 \frac{\partial I_2}{\partial I_1} \right) = Z_{th} (V_1 + I_1 h_{11} + V_2 h_{21}) \\ \left. \frac{\partial T_J}{\partial V_2} \right|_{\Delta I_1=0} &= Z_{th} \left(I_2 + I_1 \frac{\partial V_1}{\partial V_2} + V_2 \frac{\partial I_2}{\partial V_2} \right) = Z_{th} (I_2 + I_1 h_{12} + V_2 h_{22}) \end{aligned} \quad \text{Eq. B-10}$$

$$\begin{aligned} Z_{th}^{11}(\omega) &= \frac{(h_{11}(\omega) - h_{11}^{AC})}{\frac{\partial F_1}{\partial T_J} (V_1 + I_1 h_{11}(\omega) + V_2 h_{21}(\omega))} \Rightarrow Z_{th}^{11}(0) = \frac{(h_{11}^{DC} - h_{11}^{AC})}{\frac{\partial F_1}{\partial T_J} (V_1 + I_1 h_{11}^{DC} + V_2 h_{21}^{DC})} \\ Z_{th}^{12}(\omega) &= \frac{(h_{12}(\omega) - h_{12}^{AC})}{\frac{\partial F_1}{\partial T_J} (I_2 + I_1 h_{12}(\omega) + V_2 h_{22}(\omega))} \Rightarrow Z_{th}^{12}(0) = \frac{(h_{12}^{DC} - h_{12}^{AC})}{\frac{\partial F_1}{\partial T_J} (I_2 + I_1 h_{12}^{DC} + V_2 h_{22}^{DC})} \\ Z_{th}^{21}(\omega) &= \frac{(h_{21}(\omega) - h_{21}^{AC})}{\frac{\partial F_2}{\partial T_J} (V_1 + I_1 h_{11}(\omega) + V_2 h_{21}(\omega))} \Rightarrow Z_{th}^{21}(0) = \frac{(h_{21}^{DC} - h_{21}^{AC})}{\frac{\partial F_2}{\partial T_J} (V_1 + I_1 h_{11}^{DC} + V_2 h_{21}^{DC})} \\ Z_{th}^{22}(\omega) &= \frac{(h_{22}(\omega) - h_{22}^{AC})}{\frac{\partial F_2}{\partial T_J} (I_2 + I_1 h_{12}(\omega) + V_2 h_{22}(\omega))} \Rightarrow Z_{th}^{22}(0) = \frac{(h_{22}^{DC} - h_{22}^{AC})}{\frac{\partial F_2}{\partial T_J} (I_2 + I_1 h_{12}^{DC} + V_2 h_{22}^{DC})} \\ Z_{th}^{11}(\omega) &= \frac{Z_{th}^{11}(\omega)}{Z_{th}^{11}(0)} = \frac{(h_{11}(\omega) - h_{11}^{AC})}{(h_{11}^{DC} - h_{11}^{AC})} \cdot \frac{(V_1 + I_1 h_{11}^{DC} + V_2 h_{21}^{DC})}{(V_1 + I_1 h_{11}(\omega) + V_2 h_{21}(\omega))} \end{aligned} \quad \text{Eq. B-11}$$

$$\begin{aligned}
Z_{thN}^{12}(\omega) &= \frac{Z_{th}^{12}(\omega)}{Z_{th}^{12}(0)} = \frac{(h_{12}(\omega) - h_{12}^{AC})}{(h_{12}^{DC} - h_{12}^{AC})} \cdot \frac{(I_2 + I_1 h_{12}^{DC} + V_2 h_{22}^{DC})}{(I_2 + I_1 h_{12}(\omega) + V_2 h_{22}(\omega))} \\
Z_{thN}^{21}(\omega) &= \frac{Z_{th}^{21}(\omega)}{Z_{th}^{21}(0)} = \frac{(h_{21}(\omega) - h_{21}^{AC})}{(h_{21}^{DC} - h_{21}^{AC})} \cdot \frac{(V_1 + I_1 h_{11}^{DC} + V_2 h_{21}^{DC})}{(V_1 + I_1 h_{11}(\omega) + V_2 h_{21}(\omega))} \\
Z_{thN}^{22}(\omega) &= \frac{Z_{th}^{22}(\omega)}{Z_{th}^{22}(0)} = \frac{(h_{22}(\omega) - h_{22}^{AC})}{(h_{22}^{DC} - h_{22}^{AC})} \cdot \frac{(I_2 + I_1 h_{12}^{DC} + V_2 h_{22}^{DC})}{(I_2 + I_1 h_{12}(\omega) + V_2 h_{22}(\omega))}
\end{aligned} \tag{Eq. B-12}$$

$$Z_{thN}^{ij}(\omega) = \begin{cases} \frac{(h_{ij}(\omega) - h_{ij}^{AC})}{(h_{ij}^{DC} - h_{ij}^{AC})} \cdot \frac{(V_j + I_j h_{jj}^{DC} + V_{j+1} h_{j+1,j}^{DC})}{(V_j + I_j h_{jj}(\omega) + V_{j+1} h_{j+1,j}(\omega))}, & \text{for } i=1,2 \text{ and } j=1 \\ \text{or} \\ \frac{(h_{ij}(\omega) - h_{ij}^{AC})}{(h_{ij}^{DC} - h_{ij}^{AC})} \cdot \frac{(I_j + V_{j-1} h_{j-1,j}^{DC} + I_j h_{jj}^{DC})}{(I_j + V_{j-1} h_{j-1,j}(\omega) + I_j h_{jj}(\omega))}, & \text{for } i=1,2 \text{ and } j=2 \end{cases} \tag{Eq. B-13}$$

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