Modélisation et mesure des interactions électromagnétiques dans les circuits et les systèmes en boitier

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TABLE OF CONTENTS

GLOSSARY

2.5D	**2.5 D**imensions
2D	**2 D**imensions
3D	**3 D**imensions
AF	**A**gile **F**ilter
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
BAW	**B**ulk **A**coustic **W**ave
BW	**B**onding **W**ire
COV	**COV**entor
DC	**D**rive **C**urrent
DTI	**D**eep **T**rench **I**solation
DUT	**D**evice **U**nder **T**est
EM	**E**lectro**M**agnetic
ENIAC	**E**uropean **N**ano-electronics **I**nitiative **A**dvisory **C**ouncil
ENSICAEN	**E**cole **N**ationale **S**upérieure d'**I**ngénieurs de **CAEN**
ESD	**E**lectro**S**tatic **D**ischarge
FBAR	**F**ilm **B**ulk **A**coustic **R**esonators
FEM	**F**inite **E**lement **M**ethod
FOP	**F**an-**O**ut-**P**ackage
G-S-G	**G**round-**S**ignal-**G**round
G-S-G-S-G	**G**round-**S**ignal-**G**round-**S**ignal-**G**round
HVQFN	**H**eatsink **V**ery-thin **Q**uad **F**lat-pack **N**o-leads
IC	**I**ntegrated **C**ircuit
IP	**I**ntellectual **P**roperty
ITE	**I**nstitute of **E**lectron **T**echnology
LaMIPS	**La**boratory of **M**icro-electronics and Semiconductors Physics
LTCC	**L**ow **T**emperature **C**o-fired **C**eramic
MCM	**M**ulti-**C**hip **M**odule
MCU	**M**ultipoint **C**ontrol **U**nit
MEMS	**M**icro-**E**lectro-**M**echanical **S**ystems
MiM	**M**etal **i**nsulator **M**etal

MMIC	**M**onolithic **M**icrowave **I**ntegrated **C**ircuit
MoM	**M**ethod **o**f **M**omentum
OI	**O**ff **I**solation
PARSIMO	**PAR**titioning and **MO**deling of **Si**P
PCB	**P**rinted **C**ircuit **B**oard
PI	**P**ower **I**ntegrity
RF	**R**adio **F**requency
RL	**R**eturn **L**oss
SAW	**S**urface **A**coustic **W**ave
SI	**S**ignal **I**ntegrity
SIL	**Sil**vaco
SiP	**S**ystem-**i**n-**P**ackage
SME	**S**mall and **M**edium **E**nterprise
SO	**S**mall **O**utline
SoC	**S**ystem-**o**n-**C**hip
SOLR	**S**hort-**O**pen-**L**oad-**R**eciprocal
SOLT	**S**hort-**O**pen-**L**oad-**T**hrough
SoP	**S**ystem-**o**n-**P**ackage
SW	**S**traight **W**ire
TCPMT	**T**ransactions on **C**omponents, **P**ackaging, and **M**anufacturing **T**echnology
THA	**THA**LES
TRL	**T**hrough-**R**eflect-**L**ine
UOS	**U**niversity **O**f **S**heffield
VCP	**C**harge **P**ump output **V**oltage
VNA	**V**ector **A**nalyzer **N**etwork
WRUT	**WR**ocław **U**niversity of **T**echnology

GENERAL INTRODUCTION

1. Thesis frame

The thesis subject is "Modeling and Measurement of Electromagnetic Interactions in Packaged Circuits and Systems". The thesis has been prepared in the laboratory of Micro-electronics and Semiconductors Physics (LaMIPS) which is a common laboratory of Ecole Nationale Supérieure d'Ingénieurs de CAEN (ENSICAEN), Crismat laboratory, NXP Caen, and Presto Engineering.

The thesis is in the frame of the European project PARSIMO which aim to reduce the design time for SiP. The project PARSIMO is coordinated by University of Sheffield (UOS) from UK in collaboration with eight partners from three countries.

- French partners
  - ✓ Thales (THA)
  - ✓ ESIEE Paris (ESIEE)
  - ✓ Coventor (COV)
  - ✓ LaMIPS laboratory (LaMIPS)
- Polish partners
  - ✓ Wrocław University of Technology (WRUT)
  - ✓ Institute of Electron Technology (ITE)
- English partners:
  - ✓ University of Sheffield (UOS)
  - ✓ Silvaco Europe Ltd (SIL)
  - ✓ SARAS Technology (SARAS)

The thesis begun by the measurement of MEMS switch packages. Many difficulties found during the characterization helped us to locate the critical sources of problem which lead to the next studies. Some works in this thesis are not only to resolve the challenges in the semi-conductor industry, but also to support our partners.

2. Organization of thesis manuscript

The manuscript is organized in 5 chapters.

- Chapter 1 presents the context and the state of art for the characterization of EM interactions in packaged circuits and systems. The trends of packaging technologies are introduced. In this context, the European project PARSIMO supported by ENIAC has been begun to speed up the development of SiP in different aspects: electronics, mechanics, thermal,… In the frame of this project, the thesis objectives focus on developing measurement, modeling and simulation methodologies for EM characterization. The purpose of chapter 1 is to give a global background of EM characterization, and the position of this thesis in this context. The state of art of the methods developed in this thesis will be presented in details in the next chapters.
- Chapter 2 presents the original RF measurement methods which have been developed in this thesis. They are a mixed-mode TRL de-embedding method and a four-port measurement method using a two-port Vector Analyzer Network (VNA). These methods have been verified in comparison to measurement and EM simulation for accuracy and usability. This chapter introduces also the characterization of the MEMS switch packages which will be integrated in a demonstrator of the PARSIMO project.
- Chapter 3 concentrates on modeling methodologies for interconnections. Bonding wires, crossing lines, ground plane, and comb-line filter are modeled in this chapter. The models are verified in comparison with measurement and EM simulation. Lumped-element model gives quickly RF characteristics of a structure, but is accurate enough for a real system which is more complex. In this case, EM simulation must be used.
- Chapter 4 relates to design and simulation methodology for a complete package including the effect of BW arrays, grounding, vias, and die by using different tools with suitable partitioning techniques. The circuits are realized in SiGe BiCMOS technology and packaged using advanced HVQFN solution. The simulation of a complex system needs to be segmented into partitioned sub-simulations. Different approaches are compared in terms of their accuracy and complexity backed up by correlations with measurement in this chapter.

- Chapter 5 concludes the thesis with a summary of the obtained results. The perspectives and technical challenges are presented.

Chapter I

CONTEXT AND THE STATE OF ART

I.1. Introduction

Chapter I presents the objectives and motivation of the thesis in the background of the semi-conductor industry trends. This chapter is organized as follows. Paragraph I.2 describes the trends of packaging technology which result the requirements for EM characterization of SiP (measurement, simulation, and modeling). Then, paragraph I.3 presents the European project PARSIMO to which one part of this thesis relates. Paragraph I.4 introduces the thesis objectives. Finally, paragraph I.5 concludes chapter I.

I.2. The context and motivation

The context of this thesis is relative to key drivers and enablers for mobile wireless ubiquity (Figure I-1) where the following challenges need to be addressed in order to fulfil the dilemma "*Any-Device*", "*Any-Network*", "*Any-Where*", "*Any-Time*" with seamless connectivity:

- Multi-Standard applications
- Multi-Band functionalities
- Multi-Media capabilities
- Re-configurability (e.g. use of Switches) of the RF front-end– single radio front-end that can be **software reconfigured** in a flexible way for different bands and standards

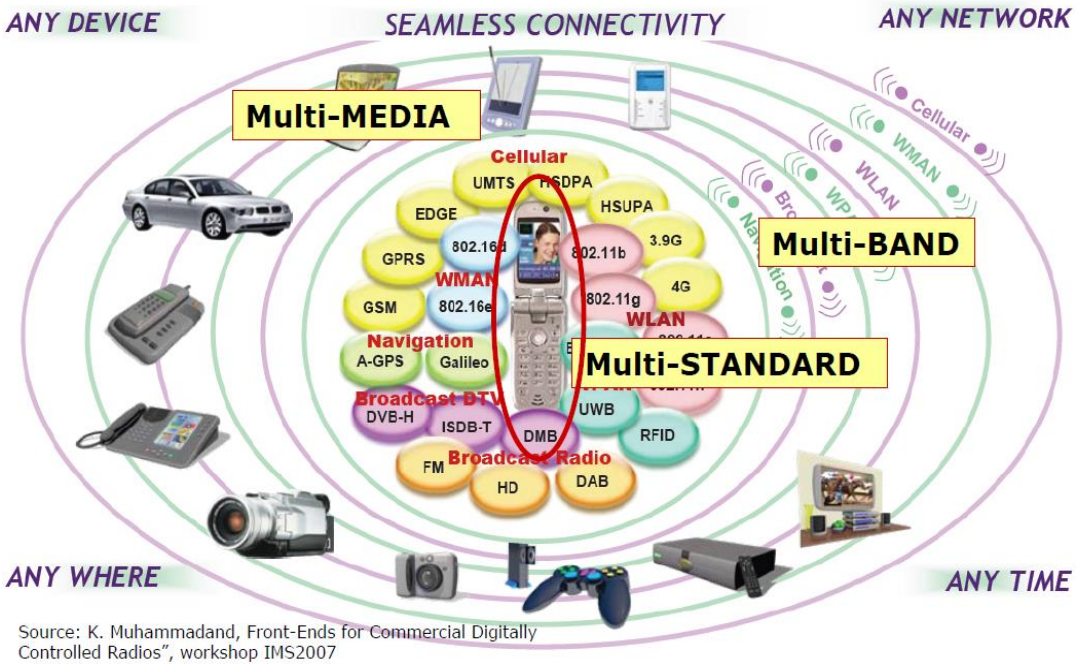


Figure I-1: Mobile Wireless Ubiquity

These challenges in order to be efficiently solved require innovation technologies and design methodologies which accurately take into account the Electro-Magnetic interactions both at component and system-level including effects of packaging and PCB.

I.2.1. Packaging trends

The International Technology Roadmap for Semiconductors (ITRS) has followed two trends shown in Figure I-2. The first trend relates to miniaturization for improving integration density, performance (higher speed, lower power) of integrated circuits. It is named More-Moore. The integration density of More-Moore devices has doubled every two years as predicted by Moore's law. The miniaturization has been along two axes: continued shrinking of physical dimensions, and development of three dimensional device structures. Beyond the 2015 horizon, silicon-based devices reach their ultimate scaling limits, as stated in the technology roadmap provided by European Nano-electronics Initiative Advisory Council (ENIAC) (Figure I-3) [2]. The new technologies "Beyond CMOS" that nm-sized features will enable, complement or replace conventional silicon technology.

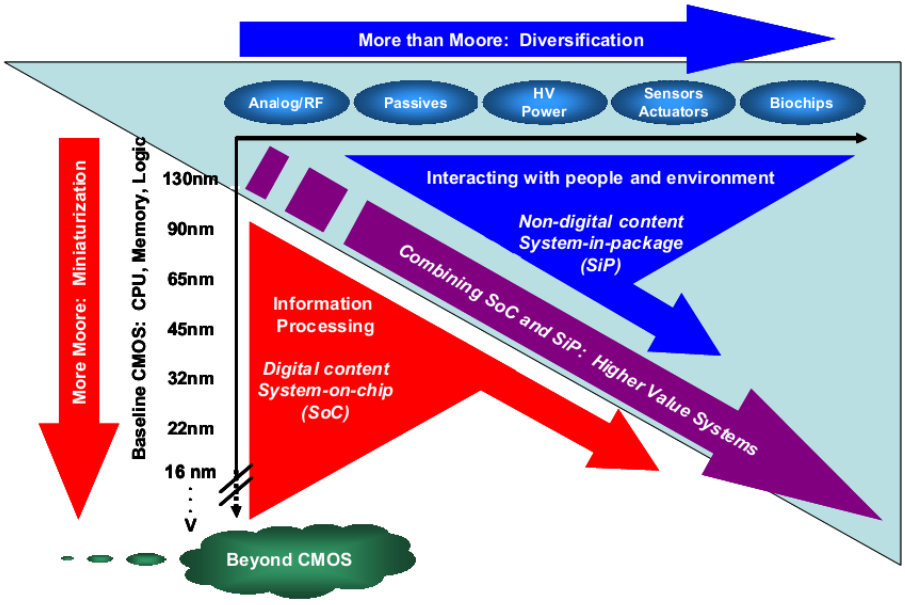


Figure I-2: International Technology Roadmap for Semiconductors

The second trend known under the name More-than-Moore relates to functional diversification of semiconductor-based devices. While More-Moore devices consist only of digital content, More-than-Moore devices combine digital and non-digital technologies (Analog, RF, MEMS, optical, biochip…) into compact systems to interact with people and environment. As a result, the More-than-Moore technology will drive a wide variety of application fields where microelectronic subsystems are key components, for example aerospace, automotive, automation, healthcare and consumer electronics, sensors, powerful processors, power drivers and RF interfaces. The combination of dissimilar components in a single package is covered by the term "heterogeneous integration" (see the blue triangle in Figure I-2). In the semiconductor industry, the heterogeneous integration is a new and potential domain (Figure I-3) which requires certainly suitable

methodologies in design, measurement, simulation, modeling, and fabrication to reduce the time-to-market.

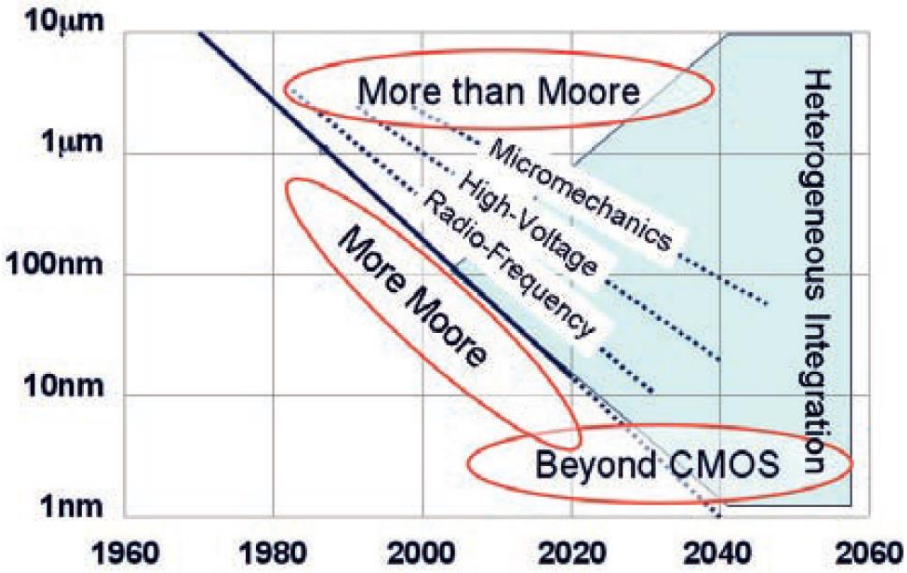


Figure I-3: ENIAC technology roadmap [3]

Package integration has the following trends [5] which are presented in Figure I-4.

- System-on-Chip (SoC)

  SoC refers to integrating onto a single die all components manufactured by a single process technology. This trend has been driven for decades through finer lithography, better materials, and larger chips and wafers, all leading to higher clock frequency. However, the key challenges to SoC progress are formidable, and include design and design verification, manufacturability, intellectual property (IP) and legal issues, time-to-market, and cost. Today electronic applications are smart and multi-functional. The multi-functionality cannot be implemented as SoC in most cases due to different manufacturing processes.

- MCM (Multi-Chip Module)

  To overcome these problems, a different approach to SoC has been pursued since the 1980s. Instead of integrating all or most of the system needs on large and complex single chips, they fabricated smaller, high-yielding chips and reconstituted them to behave like large chips as multi-chip modules (MCMs). Although MCMs were capital-intensive and technology-complex, they offered a better solution than SoCs by interconnecting dozens of chips in a small, horizontal form factor for high signal speed.

- SIP (System-in-Package)

  Instead of 2D integration as in MCM, SiP uses 3D integration which has a high potential for:

- ✓ **Dense integration** of **multi-nature systems**, whose parts cannot be manufactured (effectively) in a single technology
- ✓ Integration of bare die **hardware Intellectual Property (IP)** reduces time-to-market and development costs
- ✓ Improved **IP protection**

Through SiPs, even small or medium-sized enterprises (SME) could gain access to the development of technologically advanced, miniaturized products. However, to date, the lack of appropriate design methodologies and flows hinders the efficient development of SiPs. A comparison of the current state-of-the-art for SiP, PCB, and SoC design today reveals a significant lack of design methodology for modules with bare dies and SiP integrated system, see Table I-1. The design of SiP combines some of the advantages of PCB and SoC. Successful and efficient SiP design requires that the entire design flow is covered from simulation of the electrical behavior to design of packages.

Table I-1: Infrastructure for the design of PCB, SiP and SoC

PCB design	SiP design	SoC design
• Various tools for layout and simulation • Library with component models • Network of distributors for parts from small volume to large volume • Various PCB manufacturers	• Tools are available, but not for all aspects of SiP design. • Limited distribution for bare die parts (e.g. standard micro-controllers, DSP, memory, IO) which will not be developed by the system integrator • Missing standard, design rules etc. • Few SiP manufacturer, higher costs compared to PCB	• Sufficient design environments and tools • Foundries provide PDKs for their processes • Certain soft- IPs available, but integration could be difficult • Standards and quasi-standards for modeling and transfer languages • Foundry services available

- SoP (System-on-Package)

SoP goes a step beyond SiP by integrating thin-film components on a package substrate. Wireless components integration limits of SoC and silicon-based SiPs are also handled well in SoP because RF-components such as capacitors, filters, antennas, and high-Q inductors can be better fabricated on a package substrate than on silicon. High-speed, board-level, optical interconnects are moving to the package as chip-to-chip, high-speed interconnections replace copper, addressing both the resistance and cross-talk issues of electronic ICs. In addition, waveguides, gratings, detectors, and couplers can all be embedded in the SoP substrate. The SoP approach becomes even more significant with the emergence of bioelectronics and the need for convergent, micro-miniaturized electronic and bio-electronic systems. The integration of

microfluidics, nano-bio-sensing elements, control/feedback electronics, display, and RF/wireless components such as integrated antenna, RFID in a SoP platform makes this technology feasible for future convergent systems.

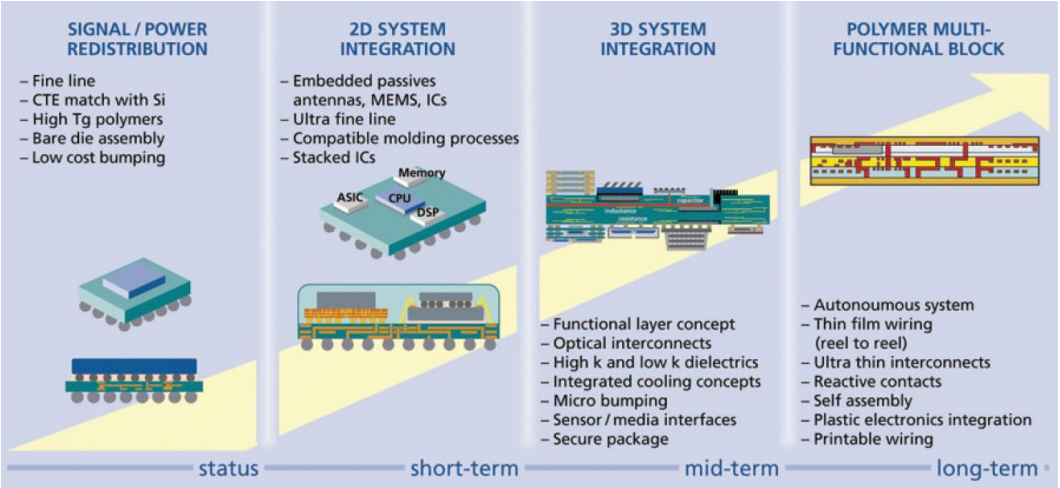


Figure I-4: Road map of module integration [2]

These trends pose many challenges for EM characterization. The main challenge that EMC engineers face for the future is how to develop test and modeling methods capable of handling billion-device ICs in an ever more complex EM environment, without incurring prohibitive costs and time penalties [6].

I.2.2. RF and microwave measurement

The ability to measure the performance of a systems at the operating frequency of interest is a key element in the design process [7]. Measurements in the frequency domain are popularly performed by Vector Analyzer Network (VNA). The results are generated in the form of *S* parameters which describe the electrical behavior of a circuit using the ratio between reflected, transmitted, and incident power waves. The trends of semiconductor industry pose challenges for RF measurement.

- Multi-port measurement is highly demanded

The first reason, which makes multi-port measurement highly demanded, concerns to the growing number of multi-port devices. If an n-port structures is measured by an <n-port VNA, a post-procedure must to be done to calculate the n-port *S* parameters. This reason results inaccuracy, long duration of characterization and more efforts.

Secondly, because of the trend of increasing operation frequency, and signal density as illustrated in Figure I-5, the mutual coupling becomes important for the performance of an IC at high frequency [11]. In order to determine correctly the mutual coupling between different lines, the electrical currents flowing through them must be comparable to each other. If the current in a line is much smaller than the others, this measurement will give wrong results [32]. To resolve this

problem with a two-port VNA, two lines could be connected together at one end to have a same currents. However, this method increases test surface, and changes circuit design. Therefore, multi-port (at least 4-port) measurement is necessarily demanded. Either a multi-port VNA or a two-port one combined with a multi-port extension test set is used [25], [27], but their cost is the barrier which makes two-port VNA still used for multi-port measurements.

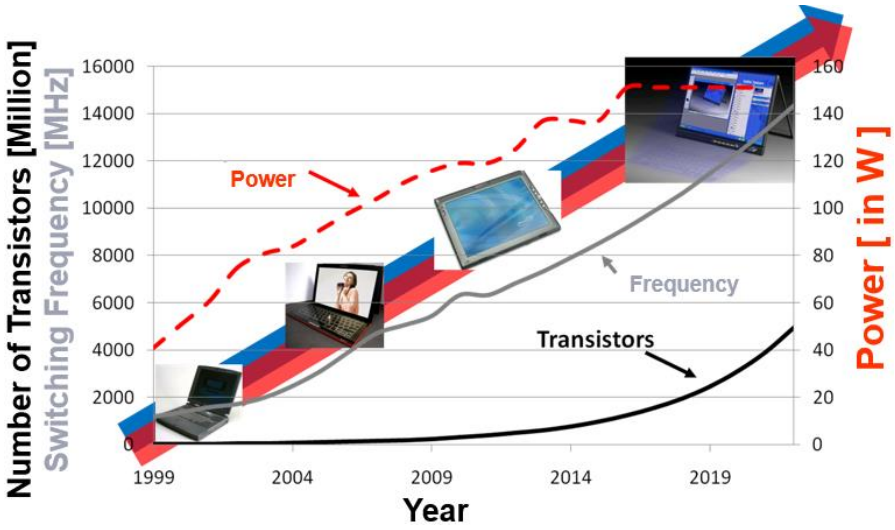


Figure I-5: Integration trend on number of transistors, on frequency, and on power

RF probe is used rather than coaxial connector between VNA and DUT

The connector between VNA and DUT is also a critical factor influencing measurement accuracy. RF connectors can be categorized into two types: coaxial connector and RF probe [7]. Their advantages and limitations are summarized in Table I-2.

Table I-2: Connectors for RF measurement

Type	Pros.	Cons.
Coaxial connector	Cheap No require manipulation experience Suitable to nonplanar, 3-D structures I/O ports can be physically spread out to place connectors	Unfavorable for on-chip measurement Limited operating frequency
RF probe	Favorable for on-wafer measurement Large frequency band	Expensive Fragile Require manipulation experience Difficulty to place mechanically all the probes required

Coaxial connector with many varieties such as SMA (Sub-Miniature version A), SMB (Sub-Miniature version B) is cheap and can be easily manipulated by a person with no experience. However, it has some limitations: limited operating frequency, big size unfavorable for on-wafer measurement. In contrast, although RF probe is expensive and requires an experiential operator, it is favorable for on-wafer measurement at high frequencies. In order to obtain good signal integrity during RF probing, a configuration of GND-Signal-GND (GSG) for RF signals is required. Because of the small size of RF die, the pad pitch is very small. As an example, the pad pitch in some products can go below 75 µm, which is the limit of the actual probe technology today. Measurement connector must be the same size as the pad pitch. Therefore, RF probe is suitable for the trend of reducing Integrated Circuit (IC) surface.

- Different methods for different technologies

The integration of sub-circuits from different providers, called Intellectual Property (IP) cores, gives an opportunity to characterize many circuits at the same time, but makes also challenges. In the recent past, mixed-signal device circuits have been increasingly integrated on the same die with digital CMOS, posing key challenges for RF measurement. Furthermore, more radically different types of semiconductor devices such as MEMS and optical components are being integrated on a single piece of silicon with CMOS logic. This trend poses a requirement of integrating different methods corresponding to these technologies into measurement process. The following technologies are highly concentrated.

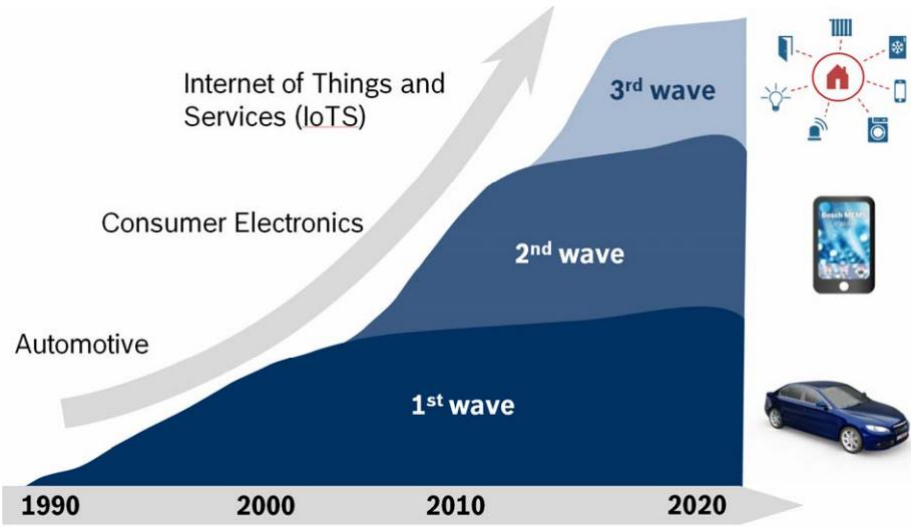


Figure I-6: The three waves of MEMS proliferation [9]

- ✓ **Differential lines** are of foremost interest for high-speed interconnects and high-speed digital circuits due to their high immunity to noise, electromagnetic interference, and crosstalk [8]. They will have improved high-frequency performance compared to single-ended (unbalanced) lines [7].

✓ **MEMS**: The MEMS market is year after year growing faster than the average semiconductor industry [9]. MEMS sensors have been started with airbag, yaw-rate and pressure sensors since the mid 90ies in automotive industry. They have been used in mobile phones in the mid of the last decade. With a potential future in Internet of Things and Service (IoTS) shown in Figure I-6, MEMS devices need to be more studied.

I.2.3. Modeling

Modeling is a procedure which replaces a real structure by a virtual one which can be a 3D design in a simulation environment, an electronics schematic, an equation or even a lookup table. Working with a real complex structure is expensive, long-time or impossible in some cases. A model helps us to understand its real structure. Therefore it must be as simple as possible, but accurate. This reason poses many challenges because IC packages are more complex as mentioned in section I.2.1. Three main classes of modeling technique can be generally distinguished:

RLCG-based Native Tools:

This class includes Static, Quasi-static, look-up tables approaches where parasitic extractions are determined based on geometry (topology) information: no concept of "**port**" only notion of "**Node**". Many tools available in the market such as: Assura Extractor of Cadence, Calibre xL of Mentor Graphics, Columbus-AMS of Sequence Design Inc....

EM S-parameters Native Field Solvers.

This class refers to 2D, 2.5D, 3D full-wave field solver engines that solve Maxwell equations in their discretized form.

Measurement/Macro-modeling based Techniques

This class is oriented towards fitting techniques to find out matching models representations that reproduce initial data from characterization measurement or available simulation results.

❖ **S-parameter model**

This model is represented as a black-box containing measurement results in the form of *S* parameters. It can be used in the simulation tools which can read S parameters.

❖ **Lumped Elements model**

Lumped element representations are derived from measurements to capture the behavior of the device/component

❖ **Laplace model**

This technique makes link between frequency domain representation and time domain response

Because RLCG-based Native Tools and EM S-parameters Native Field Solvers are programmed in a software, they are also called simulation tools. The models based on Laplace technique is used in time domain. In contrast, S-parameter model and lumped-element model are used for frequency domain. Although S-parameters model is accurate, it cannot be handled by behavior software such as HSpice. Lumped-element based model represents simply and physically a real structure. In addition, it can be used with behavior software. The advantages and limitations of these models are summarized in Table I-3. This thesis focuses on developing lumped-element-based models.

Table I-3: Measurement/Macro-modeling based Techniques

	Advantages	**Limitation**	**Complexity, CPU Time, Efficiency**
Laplace Model	Frequency dependence Accurate Delay Estimation Complex frequency Wide Frequency Range	Harmonic Assumption Z-transform approach Causality Passivity	Very Reliable Approach conformal for time domain Difficulties with HSpice (convergence issues) Long CPU Time (especially for HSpice) Sensitivity for #ports>4 (issues with multi-ports)
S-parameters Model	General Approach Accurate Delay Estimation Frequency dependent Wide Frequency Range	Low Frequency behavior Time-domain Analysis Causality Passivity	Not always reliable (Black box approach limitations) Residuals & Causality issues critical Very Long CPU Time Sensitivity for #ports>4 (issues with multi-ports)
Lumped Elements Model	Time Domain Analysis Analytical calculations Perturbation assumption	Limited frequency Range Inaccurate Delay Single RLCG Elements Artificial Ripples	Low reliability (negatives extracted values) Very stable when no negatives values No ports limitations

I.2.4. Co-design and co-simulation

System-level integration requires proper co-design and co-simulation methodologies in order to efficiently take into account the interactions between Chip, Package and PCB domains. Beyond intrinsic technology enabling attributes, bridging the gap between Chip, Package and PCB domains (see Figure I-7) will help pushing system integration to its ultimate performance limits. Both physical design and electrical-thermal analysis of single-chip (SoC: system on Chip) and multi-chip module (MCM) applications require global Co-Design methodology where constraints are pushed from Chip-level to Package-level and even up to PCB-level in an iterative forward and backward way to guarantee compliance of final product with PI (Power Integrity), SI (Signal Integrity), EMC/EMI (Electromagnetic Compatibility/Interference) specifications.

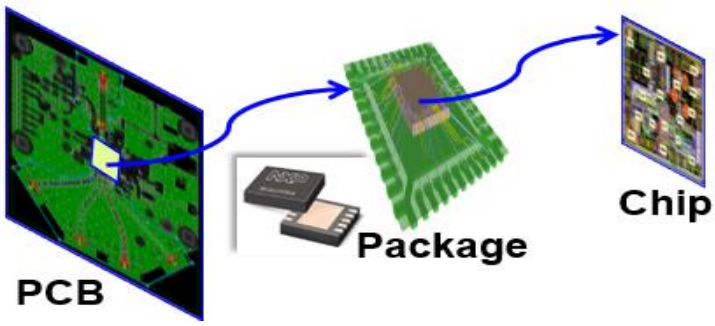


Figure I-7: Chip-Package-PCB Co-Design

Because of complexity reasons, full-wave simulation of complete Chip-Package-PCB system is extremely challenging to achieve with available modeling tools capabilities [86] - [90]. In order to make accessible simultaneous analysis of selected/identified complete paths across the different integration levels (*Chip*, *Package and Board*), functional and topological partitioning strategies are required to keep simulation burden within manageable complexity.

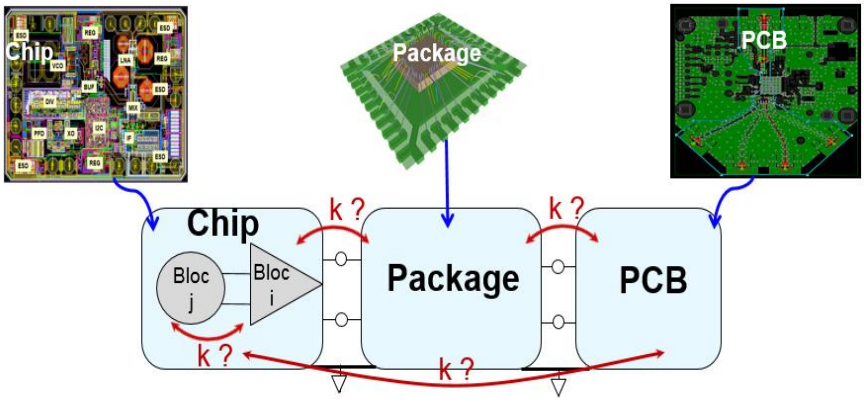


Figure I-8: Chip-Package-PCB Co-Simulation

Effective Chip-Package-PCB system Co-Simulation (see Figure I-8) results in the hybridization of different simulation techniques (*frequency-domain, time-domain, and mixed-signal*) in the framework of unified Co-design environment. *k* represents mutual coefficient. In order to loop back modeling with experimental verifications development of innovative measurement techniques represents important requirement for accurate evaluation of multi-port RF performances.

For the physical design, growing frequency of operation with increased bandwidth and integration density motivate the development of cost-effective Wafer-Level-Packaging (WLP) solutions [16]. Among emerging WLP solutions, Fan-Out-Package (FOP) eWLB (*embedded Wafer Level Ball Grid Array*) is seen as a promising option offering additional degree of freedom for routing I/O chips with reduced package parasitic and attractive grounding strategies compared to conventional lead-frame or laminate packages(e.g., HVQFN: *Heat-sink Very thin Quad Flat No lead*). Both physical design and electrical-thermal analysis of single-chip (SoC) and multi-chip module (MCM) or SiP (System-In-Package) applications require global Co-Design methodology

which lead to many advantages. The co-design methods presented in [17], [18] facilitate the overall optimization of a system.

I.3. PARSIMO project

I.3.1. Project motivation

The concept of PARSIMO is to prepare and develop a design methodology as the one outlined in Figure I-9. It will enable using bare die parts, such as sensors and RF, in special applications for wireless sensors in avionic applications (Target activity heterogeneous integration). Furthermore, it will provide the opportunity to design SiP applications to SMEs. The design methodology is developed with a direct link to target applications from ENIAC's sub-programs (SP):

- Automotive and Transport (SP1)
- Wireless Communication (SP2)
- Energy Efficiency (SP3)
- Design Methods and Tools (SP4)

To widen the range of products for SiP technologies, PARSIMO has investigated:

a. Methods that facilitate partitioning with respect to system costs, performance etc.
b. Modelling methods that can handle the high complexity of SiP (Target activity design efficiency for functional complexity)
c. Interfaces for MEMS and sensors
d. SiP design rules and language for a defined interface between designers and manufacturers
e. EDA and CAD tools filling today's gap of SiP design

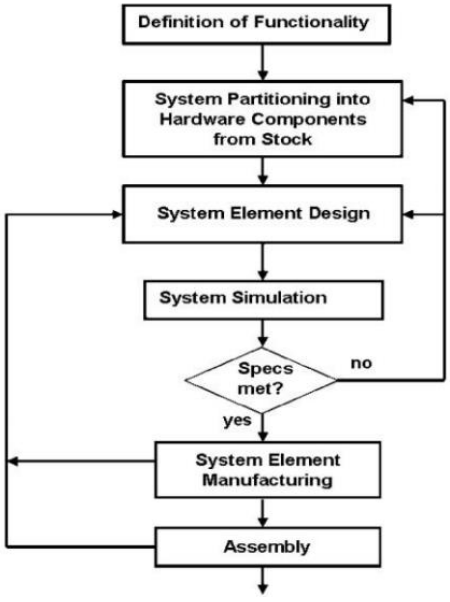


Figure I-9: Cost-effective Procedure for High Volume Production of SiPs – A European Approach

Initiating standardization activities is an important goal of PARSIMO. The standards will support a SiP ecosystem, which lays the foundations towards allowing SMEs to reuse bare dies as well as to smoothly exchange design data with manufacturers. PARSIMO will establish SiP as a third track for realizing highly complex electronic systems beside PCB and SoC. Its most striking advantages will be short times to market and low production costs.

Four industry-driven demonstrators from the aviation and wireless communication domains emphasize the relevance of SiP technology for future products and the need for the design methodology addressed in PARSIMO.

1. **Wireless Sensors for aeronautical applications**

   Being conducted by Thales in collaboration with ESIEE, COV, and LaMIPS, this demonstrator is placed in a plane with a density of up to 3000 sensors/plane to memorize time-stamped events for up to 8 hours flights (3-axis Vibrations, 3-axis Shocks, inclination, temperature in 6 directions, pressure, humidity, and time/date).

2. **System of Intelligent Sensors for Experimental Avionic Applications (SIESTA)**

   SIESTA demonstrator is conducted by ITE and WRUT. Its objective is to monitor vibrations, temperature and pressure.

3. **RF power amplifier for communications applications**

   Being conducted by SARAS, this demonstrator is a high power amplifier of up to 50W/100W targeted at various communications markets.

4. **Smart microwave Agile filter (AF) demonstrator**

   This demonstrator is conducted by THA, with contributions of ESIEE, LaMIPS, COV and SIL. Its purpose is to show how the use of the methods and technologies developed inside PARSIMO. Because this demonstrator concerns to the thesis works, it is presented in details in the next section.

I.3.2. Smart microwave Agile filter (AF) demonstrator

I.3.2.1. Package architect

The smart microwave agile filter demonstrator driven by Thales will be applied in different domains such as active antennas, radar frontend, wideband receivers, etc… It operates in a large frequency band from 1 to 18 GHz which is divided into eight sub-bands corresponding to eight sub-filters with a constant relative bandwidth of 36% (Table I-4).

Table I-4: Specifications for the Agile filter frequency bands

Filter	Bandwidth (GHz)	Relative bandwidth $\frac{\Delta f}{f_c} = \frac{f_{ch} - f_{cb}}{\sqrt{f_{ch} f_{cb}}} = \alpha$	Lower rejection frequency (GHz)	Upper rejection frequency (GHz)
1	1 – 1.44	0.37		2.44
2	1.44 – 2.06	0.36		3.06
3	2.06 – 2.95	0.36	1.06	3.95
4	2.95 – 4.24	0.36	1.95	5.24
5	4.24 – 6.08	0.36	3.24	7.08
6	6.08 – 8.74	0.36	5.08	9.74
7	8.74 – 12.54	0.36	7.74	13.54
8	12.54 – 18	0.36	11.54	19

Where: f_{cb}, f_{ch} represent the lower and upper cutoff frequency of -3 dB respectively.

In order to reduce surface, eight fixed sub-filters has been replaced by four tunable sub-filters. Tunability is strongly required in recent communications systems. The capability of a single RF front-end to cover a wide range of frequencies (2-18 GHz) would allow the commercial developments of mobile services for a lower cost and a permanent access to the applications than with a plurality of specific mobile terminals. Indeed, the tunable filters can replace the multiple filters and switches, so it can reduce cost, space and weight of a communications system [99].

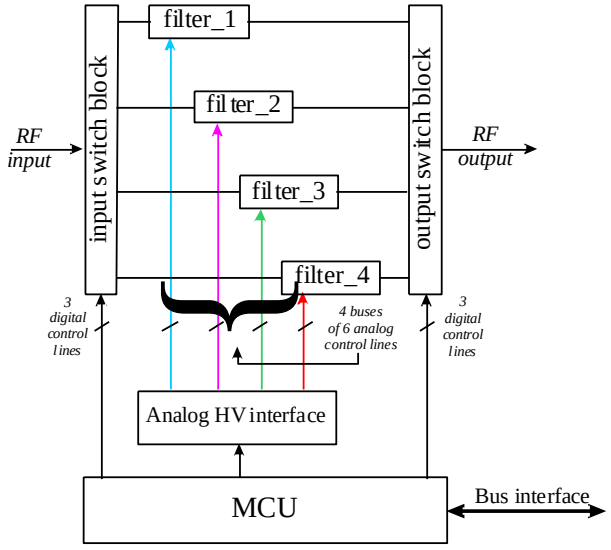


Figure I-10: Agile Filter functional diagram

The functional diagram of the demonstrator has been shown in Figure I-10. An input RF signal enters the agile filter demonstrator through a switch block which switches among four tunable sub-filters to select an expected band-width. After being filtered, the output RF signal comes out

through another switch block. The input and output switch blocks are controlled by a multipoint control unit (MCU). The MCU is also used to tune the bandwidth of the sub-filters. The MCU gets the commands from the bus and computes the control voltages to be applied to the MEMS varactors used to vary the band-widths. The demonstrator interacts with the other devices such as a computer through a bus interface. The complete AF architecture contains 24 MEMS varactors and the agile filter contains 43 blocks and approximately 200 interconnects. All components of the demonstrator will be assembled in a compact 3D package of around 4 cm^3 as shown in Figure I-11.

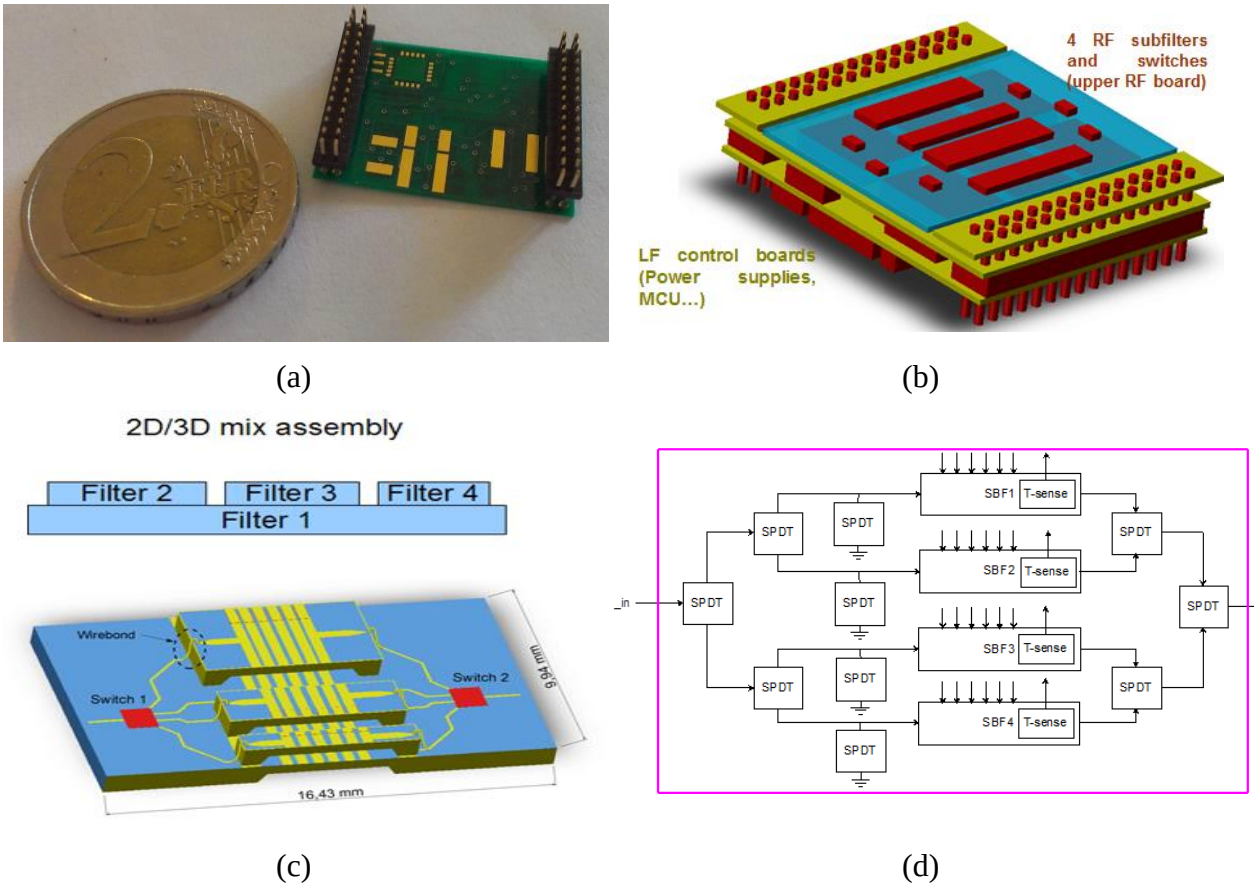


Figure I-11: Smart microwave agile filter demonstrator. (a) A prototype of the demonstrator package. (b) A 3D package design. (c) RF part (four tunable sub-filters and two switch blocks) assembly. (d) RF part schematic.

I.3.2.2. Switch block solutions

RF and microwave switches fall into the two main categories of electromechanical and solid-state switches [12]. Solid-state switches are typically more reliable, exhibit longer lifetime, and offer faster switching times than electromechanical switches. However, solid-state switches typically have higher intrinsic ON resistance and more harmonic distortion than mechanical switches.

As the first widely used solid-state switching technology, PIN diodes have been developed since 1950s. They are used in high-power, high frequency applications, but their lower frequency is limited at a few kHz to about a MHz depending on the thickness of the intrinsic region. Thus, PIN diodes cannot operate close to DC like the other switch technologies such as GaAs MMICs. In addition, they require more current to operate in comparison with the other technologies. Therefore, PIN diodes are not good for mobile applications.

Unlike PIN diode based switches controlled by current, FET based switches are voltage controlled, so they provide low power operation. Since the 1980s and 1990s, GaAs field-effect transistor (FET) based switches have been widely used at relatively low prices because of very low operating frequency, small controlling current. GaAs MMIC devices are still progressing as they shrink die sizes, develop chip scale packaging and optimize the FET design. Competing well with GaAs switches in some high volume applications such as handset switches and even some military applications, Si-on-insulator (SOI) and Si-on-sapphire (SOS) FET switches have recently been gaining market because of their cutoff frequencies and improving breakdown voltages. While GaAs technology has nearly reached its limits, SOS and SOI CMOS based devices have a lower Ron*Coff product, a good figure of merit for switches, allowing the design of switches with lower insertion loss and higher isolation. The figures of merit of some switch technologies presented in Table I-5 show that MEMS devices have the smallest value.

Table I-5: Switch Technology Figure of Merit [12]

Process	Device	Ron [Ω-mm]	Coff [fF/mm]	Ron*Roff [fs]
0.18 um thick-film SOI	5V NFET Lg = 0.6um 13.0nm gate ox	1.9	255	485
0.18 thin-film SOI	2.5V NFET Lg = 0.32um 5.2nm gate ox	0.8	310	250
0.5 um SOS	NFET 10.0nm gate ox	2.8	270	756
0.25um SOS	NFET 5.0nm gate ox	1.6	280	448
pHEMT		1.4	160	224
GaAs PIN 20	MA4GP022	1	110	110
MEMS	ARPA-proj.	0.2	0.05	0.01

Being developed and used in the early 1990s, MEMS-based switch owns high isolation up to 100 GHz, low insertion loss, near-zero power consumption, high linearity (IP3 value of about 65dBm), and small on resistance [19], [20]. Another advantage of this technology is that the devices can be manufactured by processes similar to that of VLSI and the advancement of VLSI technology has helped in the realization of many sub millimeter-sized parts to provide RF functionality [21]. The RF MEMS technology also offers the potential of large reduction in mass and volume of electronic equipment, leading to significant cost reduction [100]-[102]. It is useful for the

integration of multiband low-noise and low-power receivers [26]. Therefore, MEMS is a potential technology for replacing PIN and FET in high frequency although it still has limitations which need to be improved such as:

- Hermetic packaging, required to protect MEMS devices, may increase cost
- High voltage drive between 20 – 80 V which requires high-voltage drive circuits
- Slow switching speed

GaN has been developed mostly for high power amplifier applications but it also shows great promise as a future switch technology. In the future, GaN MMIC switches show great promise to take a foothold in higher power applications, probably replacing PIN diodes in some of these areas [12]. A detail comparison between different switch technologies has been presented in Table I-6.

Table I-6: RF switch performance comparison: MEMS, PIN diodes and FET transistor [12], [13], [19]

Switch Technology/Parameter	**Monolithic PIN diode**	**GaAS MMIC**	**CMOS SOI/SOS**	**RF MEMS**	**GaN MMIC**
Insertion Loss (dB)	0.3 – 1.5	0.3 – 2.5	0.3 – 2.5	0.1 – 5	0.1 – 1.5
Isolation (dB)	>=30	>=25	>=30	>=30	>=30
Power handling (W)	<=50	<=10	<=50	<=10	<=100
Power Consumption	High	Low	Low	Low	Low
Switching Speed	ns to μsec	ns to μsec	μsec	μsec	ns
Ron*Coff (fs)	100 – 200	224	250 (.18 μ)	0.01	400
Cost	High	Low	SOS – Low SOI – Very Low	Medium	High
ESD sensitivity	Medium	High	Low	High	Low
Linearity (IP3) (dBm)	27 – 45	27 – 45	50	66 – 80	62

RF MEMS devices consist of four different designs [22]:

- **Metal-contact** switches with excellent performance from dc to 100 GHz
- **Capacitive switches** with a capacitance ratio of 20–150:1 are suitable for On/Off application from 2 GHz to greater than 100 GHz
- **Switched capacitors** with an On/Off capacitance ratio of 4–10: 1 are ideal for tuning application from 500 MHz to greater than 100 GHz
- **Analog varactors** with a continuous tuning range of 1.5–8:1, are mostly used for tuning application from 500 MHz to greater than 100 GHz

MEMS switches using metal-contact design have been chosen as the best candidate for the agile filter demonstrator.

I.3.2.3. RF Filter solutions

The most notable RF filtering technologies include [14]:

- LC filters

  LC filters can support high frequencies and can be integrated as a SoC. However, their main drawback is that they require too much area and can offer only a limited quality factor (Q).

- Ceramic filters

  Ceramic filters offer low IL (about 1.5 - 2.5 dB), high out-of-band rejection (> 35 dB) and low cost. On the other hand the large size of ceramic filters significantly penalizes the integration.

- Surface acoustic wave (SAW) filters

  SAW technology uses surface acoustic waves in a piezoelectric material to reduce filter size. They are smaller than LC and ceramic filters, but have limitations in the frequency domain (up to 3 GHz). The main drawback is that SAW filters are not compatible with silicon integration.

- Bulk acoustic wave (BAW) filters

  BAW filters use Film Bulk Acoustic Resonators (FBAR) that are characterized by a high quality factor Q. They have a high maximal operation frequency of up to 15GHz, low IL from 1.5 – 2.5dB. They are CMOS compatible and can be integrated “above IC”.

- Low temperature co-fired ceramic (LTCC) filters.

  LTCC is a multi-layer technology that offers integration of high Q passive components along with low IL, high maximal operation frequency and acceptable out-of-band rejection. LTCC filters are smaller than LC and ceramic filters and can be integrated as SIP.

The RF filter in the AF demonstrator must operate from 1 to 18GHz, have small size, and use few components. Micro-strip RF filters are commonly used in receivers and transmitters operating in the 800 MHz to 30 GHz frequency range. Their development commenced prior to the World War II with a paper being published in 1937 by W. P. Mason and R. A. Sykes [23]. They have the main topologies presented in Figure I-12, and Figure I-13.

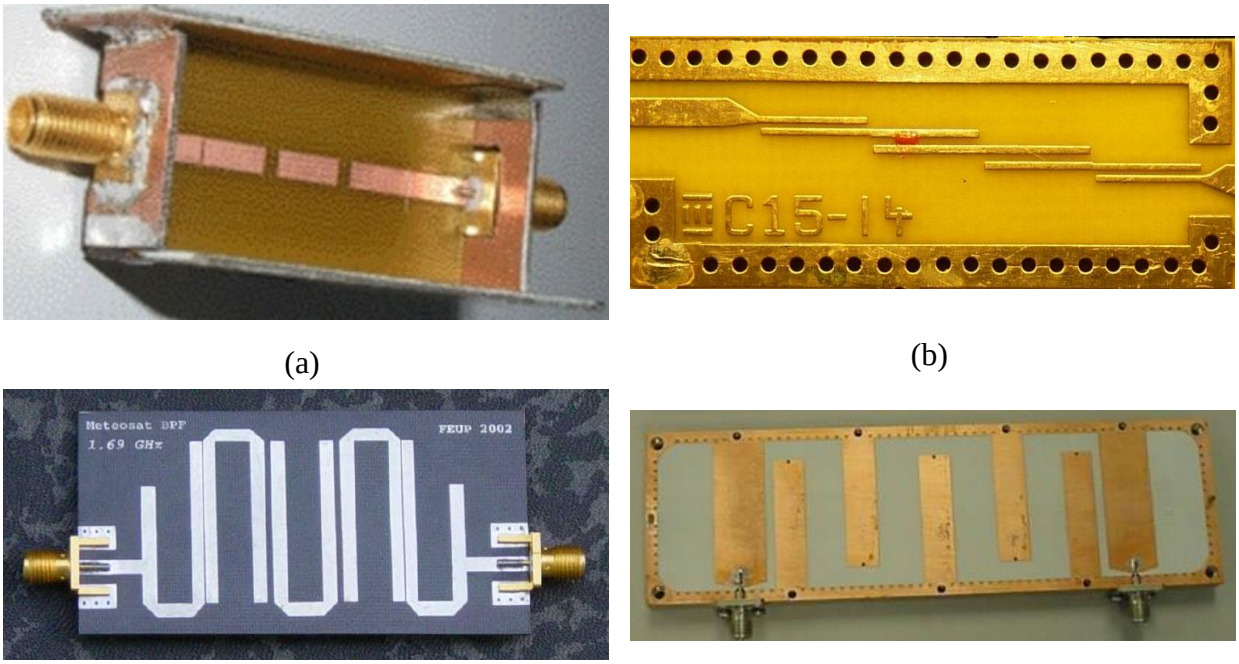
- **End-coupled filter** consists of transmission lines of λ/2 length, which are to be coupled together by the gaps between their ends (Figure I-12(a)).

- **Edge-coupled filter** is also composed of transmission lines of λ/2 length (Figure I-12(b)). The coupling between the edges of transmission lines reduces filter size and is much stronger than end coupling, so that realizable bandwidths could be much greater.
- **Hairpin filter**

  Being a variation of edge-coupled configuration, hairpin filter shown in Figure I-12(c) has transmission lines in U shape which reduce size.

- **Interdigital filter**

  The two most common types used are the parallel coupled line filter and the interdigitated filter [98]. In Figure I-12(d), interdigital configuration consists of an array of *n* TEM-mode or quasi-TEM-mode transmission line resonators, each of which has an electrical length of 90° at the mid-band frequency and is short-circuited at one end and open-circuited at the other end with alternative orientation.



(a) (b)

(c) (d)

Figure I-12: Different types of micro-strip filter. (a) End-coupled filter. (b) Edge-coupled filter. (c) Hairpin filter. (d) Interdigital filter.

- **Comb-line filter** (Figure I-13) has transmission lines of λ/4 length which have an end connected to ground, another end connected to a capacitor. Due to all capacitors on the same side which facilitate fabrication, comb-line filter is the best candidate for the AF demonstrator.

I.3.2.4. Function principle of an agile filter

The topology of a comb-line filter with six transmission lines is described in Figure I-13.

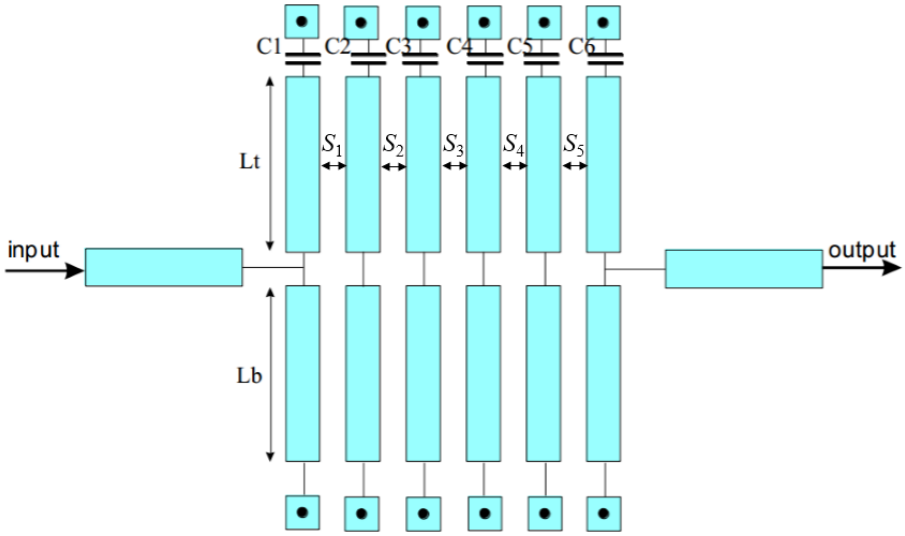


Figure I-13: Comb-line filter topology

The orders of the filters of constant relative band and of the same selectivity are identical. Because of the symmetry of comb-line filter, the capacitances C_1, C_2, C_3 equal to C_4, C_5, C_6, and the spaces S_1, S_2 equal to S_4, S_5. Therefore, there are 8 parameters for each filter:

- ✓ 3 capacitances C_1, C_2, and C_3.
- ✓ 2 lengths L_t and L_b.
- ✓ 3 spaces between lines S_1, S_2, and S_3.

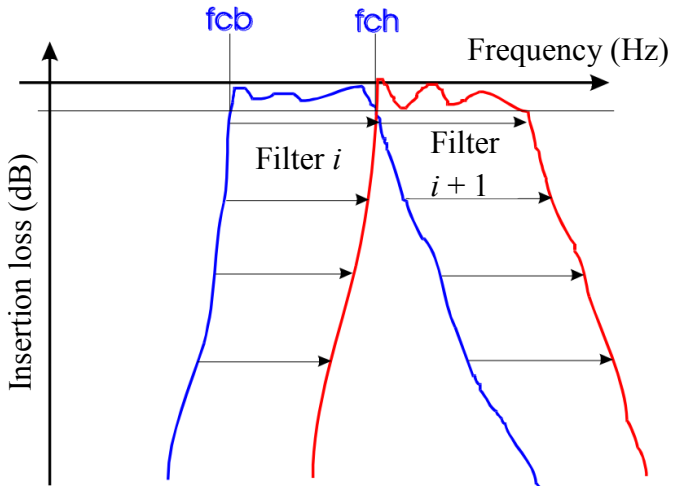


Figure I-14: Principle of the agility of filter

In order to pass from one filter to another working at lower frequencies, we must increase the value of 8 parameters. In general, the value of the spaces S_i does not need to be much varied to maintain a constant coupling. Meanwhile, the other parameters increase proportionally to wave-length. For agile filter, a tuning between the bands *i* and *i* + 1 requires varying only the capacitances. If the capacitances are continuously tuned, we can change gradually the transfer function from band *i* to band *i* + 1 (Figure I-14).

I.4. Thesis objectives

This thesis focus on characterization of EM interactions in Packaged Circuits and Systems. These methodologies presented in this thesis will be evaluated for accuracy and usability on the smart microwave agile filter demonstrator of PARSIMO project and on NXP products. It has the following objectives:

- **Establish accurate, less-efforts, less-time, and cheap methodologies of Radio Frequency (RF) measurement for Packaged Circuits and Systems**

  The measurement procedure for a package integrating many technologies (Digital, analog, optical, MEMS…) requires different equipment which can cost much. It takes also time, effort, and expertise to measure completely a package. Therefore, this objective is to develop methodologies to resolve these difficulties, and facilitate multi-port measurements for SMEs using cheaper equipment. The thesis frame concentrates on RF measurement performed by a VNA.

- **Establish EM modeling methodology for Packaged Circuits and Systems**

  Lumped-element based models will be used in conjunction with EM simulations both for Pre-Layout and Post-Layout verifications/optimizations. EM models will replace long EM simulations to characterize quickly a circuit. In addition, their physical descriptions for a package can be used for optimization. However, modeling of a complex package leads usually many difficulties (Unphysical phenomena (e.g. negative values), model too complex to extract the values of its elements, modeling too long due to a big number of elements). This thesis objective will propose models as simple as possible for different structures. It is also to speed up value extraction using automated methods. In the thesis frame, only passive structures will be modeled.

- **Establish EM simulation methodology for Packaged Circuits and Systems using different tools available in the market**

  Being an indispensable step before fabrication of electronics design, EM simulation takes much time and effort, may be impossible for complex packages. Many tools in the market cannot simulate a whole package of different technologies. This objective will speed up simulation process for Packaged Circuits and Systems using available tool with appropriate partitioning methods.

I.5. Conclusion

Chapter I introduced the trends of the semiconductor industry in which electronics devices evolve from 2D, simple, mono-functional structures to 3D complex multi-functional ones. In the motivation of making SiP, which is a potential integration technology, feasible for small and medium enterprises (SMEs), the European project PARSIMO has been begun. In the frame of this project, the thesis focuses on EM characterization including measurement, modeling, and simulation. Measurement is expensive, and takes much time. Therefore, modeling and simulation are used. Modeling is simple, and quick, but less accurate than simulation, because it cannot be applicable for a complex system.

From the global state of art mentioned in this chapter, the objectives of this thesis will be realized through the following steps:

- Measurement methodology presented in chapter II
  - A measurement method for differential devices
  - A multi-port measurement
  - Characterization of MEMS switch package
- Modeling methodology presented in chapter III
  - Models based on lumped-element approach to be simply handled by behavior software.
  - Different interconnections will be chosen to be modeled.
- Simulation methodology presented in chapter IV
  - Co-design and co-simulation methodologies combining our available simulation tools (ADS, Momentum, EMPro, and Sonnet).

The methods developed in this thesis are evaluated on the agile filter demonstrator of the PARSIMO project, and on NXP semiconductor products.

Chapter II

ORIGINAL MEASUREMENT METHODS

II.1. Introduction

More and more circuits in telecommunication technologies are differential structures. This simplifies the design of RF functions and helps to the parasitic frequencies rejection. Measurement methods developed particularly for these differential circuits will reduce characterization time and increase accuracy. A differential circuit with at least three ports (two inputs and one output) demands multi-port tests. In addition, multi-port measurement is also required to determine mutual coupling between differential interconnections which influences significantly package performance due to the trend of increasing operation frequency, and signal density [32]. Before an RF measurement, a calibration must be done. The algorithm developed in the recent publications such as [35] allows rigorous mixed modes measurement. However their main drawback is so complex with many assumptions.

The four-port VNA are now familiar and many calibration procedures developed for two-port analyzers have been extended to four-port. Before an RF measurement, a calibration must be done on an external calibration kit (Cal-kit) provided by manufacturer to eliminate the influence of VNA, cables and RF connectors. The calibration algorithms programmed in most of modern VNAs are applicable for all circuit types. After RF measurements, input and output accesses must be de-embedded from measurement results. TRL (Thru-Reflect-Line) is one of the most popular methods because it places the reference planes at the input and output of the DUT directly on the wafer. It assumes that the propagation constant is clearly defined for each line standard [35]. When the accesses are constituted by coupled lines, only the propagation constants of the quasi-TEM *c* and π modes are defined. For symmetric access lines, that means that the propagation constants are related to the odd and even modes, so called mixed modes. When the waveguides are not homogeneous (e.g. micro-strip or coplanar waveguide) these propagation constants are different each from the other. This means that the classical 4 port TRL de-embedding is not valid. The mixed mode de-embedding process presented in this chapter is more rigorous. When there is no coupling between the access lines or when the mixed modes are quasi-TEM, the propagation constants are equal. In that case, it is possible to consider the natural mode for the description of the DUT.

Four-port VNA are not always available. In that case, a two-port VNA must be used. The conventional techniques for multi-ports characterization consist of using the universal two-port VNA and perform C_2^N combinations of two-port measurements with the other unused ports terminated by perfectly matched load. When two ports of a multi-port structure are measured, the other ports are either open, or shorted, or connected to a load. All reflection coefficients at these un-measured ports must be known [29]. Nevertheless, these loads are not easy to be integrated specially for millimeter wave applications. Their uncertainty leads to the errors of multi-port S parameters reconstitution [30]. The authors in [31] proposed a model for multiport uncertainties to simplify the required test set and the measurement procedure. Furthermore, for on-wafer characterization, this procedure becomes costly due to the wafer surface that will be used. In [28], Hsin-Chia Lu and Tah-Hsiung Chu have presented a formulation for solving the *n*-port scattering

matrix from sets of the reduced (n -1)-port scattering matrix by connecting terminators to each port one at a time. Only two of the n terminators are required to be known instead of n. However, in these publications, all possible two-port combinations calculated by $C_2^n = \frac{n!}{2(n-2)!}$ must be measured to reconstruct n-port S parameters. For example, for a 5-port structure, 10 two-port measurements must be done. A simple which does not require all the 2-port combinations to be measured, has been presented in [42] with very good results in comparison with EM simulation. To do this, auxiliary terminations were used for un-measurable ports. In [39] - [42] the unused ports are either connected to auxiliary terminations or left free, it implies that each reflection coefficients must be either known or accurately measured. This leads to complicated procedures which are highly dependent on the accuracy of the measurement of these reflection coefficients. In this chapter, a very simple technique for multi-port characterization using two-port VNA is described. It consists of keeping the ports not connected of the VNA unterminated.

The chapter 2 is organized as follows. Paragraph II.2 presents the TRL mixed-mode de-embedding method. Paragraph II.3 describes four-port measurement method using a two-port VNA. Finally, in paragraph II.4, the method proposed in paragraph II.3 has been applied for characterizing MEMS switch package that are useful in the PARSIMO project.

II.2. TRL mixed-mode de-embedding method

In this paragraph, we describe a mixed mode TRL de-embedding method. The first part reminds the essential notions on natural and mixed modes, and the transformation between them. Then in the second part, the error model is proposed and the calculation of the error terms is detailed. The third part will present the experiment to verify the method with some line structures realized based on glass substrate. The final part will conclude the method.

II.2.1. Definition

II.2.1.1. Natural modes

The natural modes are defined only if the accesses are clearly separated or if the propagation structures accept TEM modes. The corresponding natural *S* and *T* parameters of a four-port structure shown in Figure II-1 are defined by Eq.(II-1) and (II-2).

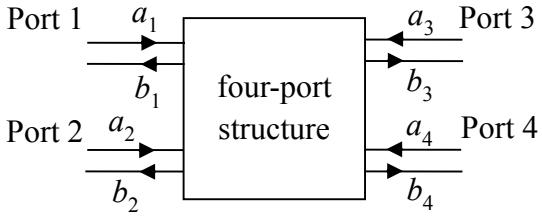


Figure II-1: Four-port structure

S parameters represent the relation between reflected and incident power waves.

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{pmatrix} = \mathbf{S_n} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{pmatrix} \quad \text{(II-1)}$$

T parameters describe the relation between input and output power waves.

$$\begin{pmatrix} b_1 \\ b_2 \\ a_1 \\ a_2 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} & T_{13} & T_{14} \\ T_{21} & T_{22} & T_{23} & T_{24} \\ T_{31} & T_{32} & T_{33} & T_{34} \\ T_{41} & T_{42} & T_{43} & T_{44} \end{pmatrix} \begin{pmatrix} a_3 \\ a_4 \\ b_3 \\ b_4 \end{pmatrix} = \mathbf{T_n} \begin{pmatrix} a_3 \\ a_4 \\ b_3 \\ b_4 \end{pmatrix} \quad \text{(II-2)}$$

Where a_i, b_i are the incident and reflected power waves for port i (i = 1, 2, 3, 4) respectively.

The natural *S* parameters can be determined from measurement or EM simulation. If we put together 4 measurement results in matrix form, we have:

$$\begin{pmatrix} b_1^{(1)} & b_1^{(2)} & b_1^{(3)} & b_1^{(4)} \\ b_2^{(1)} & b_2^{(2)} & b_2^{(3)} & b_2^{(4)} \\ b_3^{(1)} & b_3^{(2)} & b_3^{(3)} & b_3^{4)} \\ b_4^{(1)} & b_4^{(2)} & b_4^{(3)} & b_4^{(4)} \end{pmatrix} = \mathbf{S_n} \begin{pmatrix} a_1^{(1)} & a_1^{(2)} & a_1^{(3)} & a_1^{(4)} \\ a_2^{(1)} & a_2^{(2)} & a_2^{(3)} & a_2^{(4)} \\ a_3^{(1)} & a_3^{(2)} & a_3^{(3)} & a_3^{4)} \\ a_4^{(1)} & a_4^{(2)} & a_4^{(3)} & a_4^{(4)} \end{pmatrix} \quad \text{(II-3)}$$

Where the superscript $^{(i)}$ means the i^{th} measurement configuration (i = 1, 2, 3, 4) in which the source generates $a_i^{(i)}$; the others $a_j^{(i)}$($j \neq i$ and j= 1, 2, 3, 4) being very weak.

$$\begin{pmatrix} b_1^{(i)} \\ b_2^{(i)} \\ b_3^{(i)} \\ b_4^{(i)} \end{pmatrix} = \mathbf{S_n} \begin{pmatrix} a_1^{(i)} \\ a_2^{(i)} \\ a_3^{(i)} \\ a_4^{(i)} \end{pmatrix} \quad \text{(II-4)}$$

Thus:

$$\mathbf{S_n} = \begin{pmatrix} b_1^{(1)} & b_1^{(2)} & b_1^{(3)} & b_1^{(4)} \\ b_2^{(1)} & b_2^{(2)} & b_2^{(3)} & b_2^{(4)} \\ b_3^{(1)} & b_3^{(2)} & b_3^{(3)} & b_3^{4)} \\ b_4^{(1)} & b_4^{(2)} & b_4^{(3)} & b_4^{(4)} \end{pmatrix} \begin{pmatrix} a_1^{(1)} & a_1^{(2)} & a_1^{(3)} & a_1^{(4)} \\ a_2^{(1)} & a_2^{(2)} & a_2^{(3)} & a_2^{(4)} \\ a_3^{(1)} & a_3^{(2)} & a_3^{(3)} & a_3^{4)} \\ a_4^{(1)} & a_4^{(2)} & a_4^{(3)} & a_4^{(4)} \end{pmatrix}^{-1} \quad \text{(II-5)}$$

Meanwhile, the natural T parameters are obtained from S parameters using the following transformation.

$$\mathbf{T_n} = \left(\mathfrak{I}^{\mathbf{1}}_{\mathbf{Sn2Tn}} - \mathbf{S_n}.\mathfrak{I}^{\mathbf{2}}_{\mathbf{Sn2Tn}}\right)^{-1}.\left(\mathbf{S_n}.\mathfrak{I}^{\mathbf{3}}_{\mathbf{Sn2Tn}} - \mathfrak{I}^{\mathbf{4}}_{\mathbf{Sn2Tn}}\right) \quad \text{(II-6)}$$

Where $\mathfrak{I}^{\mathbf{i}}_{\mathbf{Sn2Tn}}$describes the transformation from S to T matrix in natural mode.

$$\mathfrak{I}^{\mathbf{1}}_{\mathbf{Sn2Tn}} = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix}, \ \mathfrak{I}^{\mathbf{2}}_{\mathbf{Sn2Tn}} = \begin{pmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \quad \text{(II-7)}$$

$$\mathfrak{I}^{\mathbf{3}}_{\mathbf{Sn2Tn}} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{pmatrix}, \ \mathfrak{I}^{\mathbf{4}}_{\mathbf{Sn2Tn}} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \quad \text{(II-8)}$$

II.2.1.2. Mixed modes

The differential and common modes of a four-port structure are described as in Figure II-2.

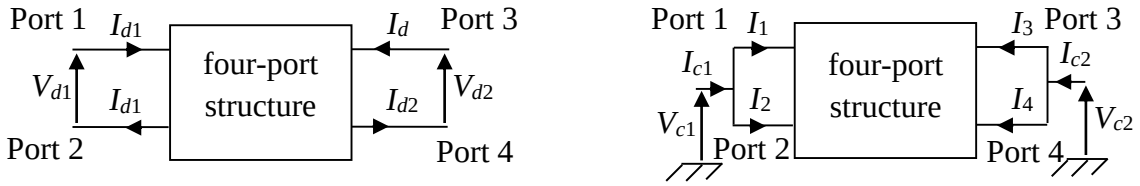


Figure II-2: Mixed modes definition. (a) Differential mode. (b) Common mode

The mixed-mode *S* parameters are defined as the relation between mixed-mode reflected and incident power waves.

$$\begin{pmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{pmatrix} = \begin{pmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{pmatrix} \begin{pmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{pmatrix} = \mathbf{S_m} \begin{pmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{pmatrix} \tag{II-9}$$

The mixed-mode *T* parameters are defined as following

$$\begin{pmatrix} b_{d1} \\ a_{d1} \\ b_{c1} \\ a_{c1} \end{pmatrix} = \begin{pmatrix} T_{dd11} & T_{dd12} & T_{dc11} & T_{dc12} \\ T_{dd21} & T_{dd22} & T_{dc21} & T_{dc22} \\ T_{cd11} & T_{cd12} & T_{cc11} & T_{cc12} \\ T_{cd21} & T_{cd22} & T_{cc21} & T_{cc22} \end{pmatrix} \begin{pmatrix} a_{d2} \\ b_{d2} \\ a_{c2} \\ b_{c2} \end{pmatrix} = \mathbf{T_m} \begin{pmatrix} a_{d2} \\ b_{d2} \\ a_{c2} \\ b_{c2} \end{pmatrix} \tag{II-10}$$

Where:

- ✓ a_{di}, b_{di} are the incident and reflected power wave for port i (i =1, 2) in differential mode respectively.
- ✓ a_{ci}, b_{ci} are the incident and reflected power wave for port i (i =1, 2) in common mode respectively.

The transformation from $\mathbf{T_m}$ to $\mathbf{S_m}$ is as Eq.

$$\mathbf{S_m} = \left(\mathfrak{I}^{1}_{\mathbf{Tm2Sm}} - \mathbf{T_m}.\mathfrak{I}^{2}_{\mathbf{Tm2Sm}}\right)^{-1}.\left(\mathbf{T_m}.\mathfrak{I}^{3}_{\mathbf{Tm2Sm}} - \mathfrak{I}^{4}_{\mathbf{Tm2Sm}}\right) \tag{II-11}$$

Where $\mathfrak{I}^{\mathbf{i}}_{\mathbf{Tm2Sm}}$ describes the transformation from T to S matrix in mixed-mode.

$$\mathfrak{I}^{1}_{\mathbf{Tm2Sm}}=\begin{pmatrix}1&0&0&0\\0&0&0&0\\0&0&1&0\\0&0&0&0\end{pmatrix},\ \mathfrak{I}^{2}_{\mathbf{Tm2Sm}}=\begin{pmatrix}0&0&0&0\\0&1&0&0\\0&0&0&0\\0&0&0&1\end{pmatrix} \quad \text{(II-12)}$$

$$\mathfrak{I}^{3}_{\mathbf{Tm2Sm}}=\begin{pmatrix}0&1&0&0\\0&0&0&0\\0&0&0&1\\0&0&0&0\end{pmatrix},\ \mathfrak{I}^{4}_{\mathbf{Tm2Sm}}=\begin{pmatrix}0&0&0&0\\1&0&0&0\\0&0&0&0\\0&0&1&0\end{pmatrix} \quad \text{(II-13)}$$

A mixed-mode matrix can be divided into 4 sub-matrices: two sub-matrices representing two modes and two others representing the coupling between two modes. For example, mixed-mode **T** matrix consists of 4 sub-matrices:

- ✓ $\mathbf{T_{dd}}=\begin{pmatrix}T_{dd11}&T_{dd12}\\T_{dd21}&T_{dd22}\end{pmatrix}$, and $\mathbf{T_{cc}}=\begin{pmatrix}T_{cc11}&T_{cc12}\\T_{cc21}&T_{cc22}\end{pmatrix}$ represent differential and common mode respectively.
- ✓ $\mathbf{T_{dc}}=\begin{pmatrix}T_{dc11}&T_{dc12}\\T_{dc21}&T_{dc22}\end{pmatrix}$, and $\mathbf{T_{cd}}=\begin{pmatrix}T_{cd11}&T_{cd12}\\T_{cd21}&T_{cd22}\end{pmatrix}$ represent the couplings between differential and common mode.

II.2.1.3. Mixed and natural mode transformation

Natural and mixed modes can be transformed one to each other. Let us consider a symmetrical tee:

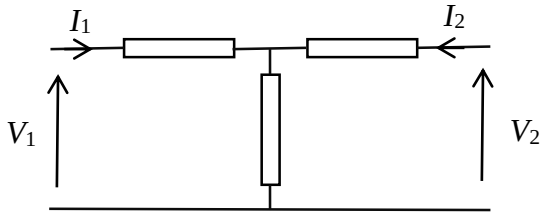


Figure II-3: Model for a symmetrical tee

The differential mode is defined as:

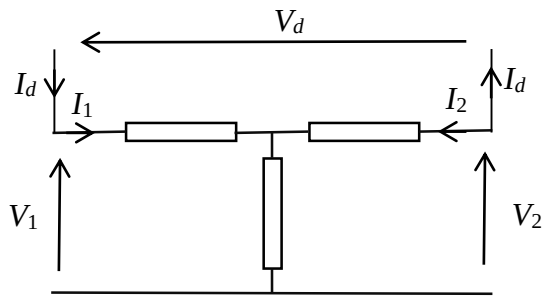


Figure II-4: Differential mode

$$V_d = V_1 - V_2, \quad I_d = I_1 = -I_2 \tag{II-14}$$

The common mode is defined as:

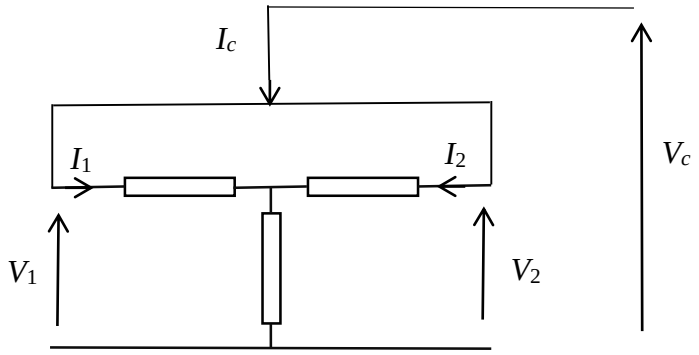


Figure II-5: Common mode

$$V_c = V_1 = V_2, \quad I_c = I_1 + I_2 \tag{II-15}$$

More generally:

$$V_d = V_1 - V_2, I_d = \frac{I_1 - I_2}{2} \tag{II-16}$$

$$V_c = \frac{V_1 + V_2}{2}, \quad I_c = I_1 + I_2 \tag{II-17}$$

Reciprocally:

$$V_1 = \frac{2V_c + V_d}{2}, I_1 = \frac{I_c + 2I_d}{2} \tag{II-18}$$

$$V_2 = \frac{2V_c - V_d}{2},\ I_2 = \frac{I_c - 2I_d}{2} \tag{II-19}$$

If we consider a symmetrical structure in TEM mode with a characteristic impedance Z_0, the forward propagation can be represented by a voltage and a current in each conductor (V_1, V_2, I_1, I_2):

$$\frac{V_1}{I_1} = \frac{V_2}{I_2} = Z_0 \tag{II-20}$$

In terms of power waves:

$$V_1 = a_1\sqrt{Z_0}\ , I_1 = \frac{a_1}{\sqrt{Z_0}} \tag{II-21}$$

$$V_2 = a_2\sqrt{Z_0}\ ,\ I_2 = \frac{a_2}{\sqrt{Z_0}} \tag{II-22}$$

If Z_0 is real, the power born by the differential mode is:

$$P_d = \frac{1}{2}\mathrm{Re}\left(V_d I_d^*\right) = \frac{1}{2}\mathrm{Re}\left(\frac{\left(V_1 - V_2\right)\left(I_1 - I_2\right)^*}{2}\right) = \frac{1}{2}\frac{\left|a_1 - a_2\right|^2}{2} = \frac{1}{2}\left|a_d\right|^2 \tag{II-23}$$

We can define the differential power wave as:

$$a_d = \frac{a_1 - a_2}{\sqrt{2}} \tag{II-24}$$

For the common mode:

$$P_c = \frac{1}{2}\mathrm{Re}\left(V_c I_c^*\right) = \frac{1}{2}\mathrm{Re}\left(\frac{\left(V_1 + V_2\right)\left(I_1 + I_2\right)^*}{2}\right) = \frac{1}{2}\frac{\left|a_1 + a_2\right|^2}{2} = \frac{1}{2}\left|a_c\right|^2 \tag{II-25}$$

The common power wave is:

$$a_c = \frac{a_1 + a_2}{\sqrt{2}} \tag{II-26}$$

Reciprocally:

$$a_1 = \frac{a_c + a_d}{\sqrt{2}},\ a_2 = \frac{a_c - a_d}{\sqrt{2}} \tag{II-27}$$

Thus we have:

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{pmatrix} = \mathfrak{I}_{\mathbf{m\_n}} . \begin{pmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{pmatrix}, \quad \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{pmatrix} = \mathfrak{I}_{\mathbf{m\_n}} . \begin{pmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{pmatrix}, \quad \begin{pmatrix} b_1 \\ b_2 \\ a_1 \\ a_2 \end{pmatrix} = \mathfrak{I}_{\mathbf{m\_n}} . \begin{pmatrix} b_{d1} \\ a_{d1} \\ b_{c1} \\ a_{c1} \end{pmatrix}, \quad \begin{pmatrix} a_3 \\ a_4 \\ b_3 \\ b_4 \end{pmatrix} = \mathfrak{I}_{\mathbf{m\_n}} . \begin{pmatrix} a_{d2} \\ b_{d2} \\ a_{c2} \\ b_{c2} \end{pmatrix} \tag{II-28}$$

Where $\mathfrak{I}_{\mathbf{m\_n}}$ is the transformation between mixed mode and natural mode.

$$\mathfrak{I}_{\mathbf{m\_n}} = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 0 & 1 & 0 \\ -1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & -1 & 0 & 1 \end{pmatrix} \tag{II-29}$$

From Eq. (II-1), (II-2), (II-9), (II-10), and (II-28), the transformations between natural and mixed modes will be

$$\mathbf{T_m} = \mathfrak{I}^{-1}_{\mathbf{m\_n}} . \mathbf{T_n} . \mathfrak{I}_{\mathbf{m\_n}} \tag{II-30}$$

$$\mathbf{S_m} = \mathfrak{I}^{-1}_{\mathbf{m\_n}} . \mathbf{S_n} . \mathfrak{I}_{\mathbf{m\_n}} \tag{II-31}$$

II.2.2. Determination of DUT mixed-mode transfer matrix

The transfer matrices of input and output accesses are determined from the ones of Thru, Reflect and Line. Then they are eliminated through a de-embedding process to get the transfer matrix of DUT.

II.2.2.1. De-embedding process

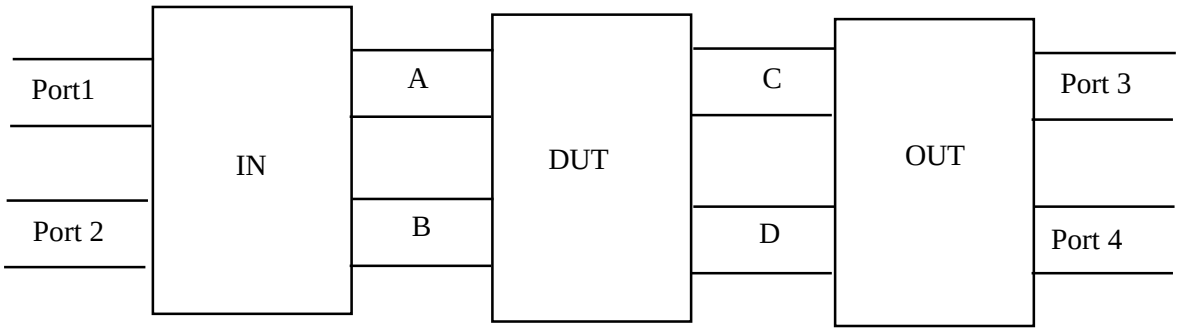


Figure II-6: Access definition

In order to determine DUT transfer matrix, input and output accesses need to be de-embedded from measurement result by using Eq. (II-32) for natural mode or Eq. (II-33) for mixed modes.

$$\mathbf{T}_{\mathbf{n}}^{\mathbf{DUT}} = \mathbf{T}_{\mathbf{n}}^{\mathbf{in}^{-1}}.\mathbf{T}_{\mathbf{n}}^{\mathbf{meas}}.\mathbf{T}_{\mathbf{n}}^{\mathbf{out}^{-1}} \tag{II-32}$$

$$\mathbf{T}_{\mathbf{m}}^{\mathbf{DUT}} = \mathbf{T}_{\mathbf{m}}^{\mathbf{in}^{-1}}.\mathbf{T}_{\mathbf{m}}^{\mathbf{meas}}.\mathbf{T}_{\mathbf{m}}^{\mathbf{out}^{-1}} \tag{II-33}$$

Where the superscripts $^{\mathbf{DUT}}$, $^{\mathbf{in}}$, $^{\mathbf{meas}}$, $^{\mathbf{out}}$ represent DUT, input, measurement, and output respectively. $\mathbf{T}_{\mathbf{n}}^{\mathbf{meas}}$ is the measured transfer matrix of DUT including input and output accesses.

In condition of no coupling between two modes, input and output transfer matrices are as Eq. (II-34).

$$\mathbf{T}_{\mathbf{m}}^{\mathbf{in}} = \begin{pmatrix} \mathbf{T}_{\mathbf{dd}}^{\mathbf{in}} & 0 \\ 0 & \mathbf{T}_{\mathbf{cc}}^{\mathbf{in}} \end{pmatrix},\ \mathbf{T}_{\mathbf{m}}^{\mathbf{out}} = \begin{pmatrix} \mathbf{T}_{\mathbf{dd}}^{\mathbf{out}} & 0 \\ 0 & \mathbf{T}_{\mathbf{cc}}^{\mathbf{out}} \end{pmatrix} \tag{II-34}$$

Where the error matrices $\mathbf{T}_{\mathbf{dd}}^{\mathbf{in}}$, $\mathbf{T}_{\mathbf{cc}}^{\mathbf{in}}$, $\mathbf{T}_{\mathbf{dd}}^{\mathbf{out}}$, $\mathbf{T}_{\mathbf{cc}}^{\mathbf{out}}$ will be determined using Thru, Reflect, and Line measurements in the next section.

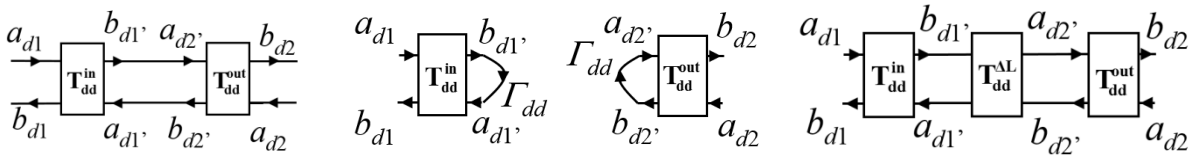
II.2.2.2. Error model calculation

We assume that the TRL patterns (Thru, Reflect and Line) are symmetrical, so that there is no coupling between two modes. Their mixed modes transfer matrices can be separated into two sub-matrices, one for differential mode, and the other for common mode.

Table II-1. Transfer matrices in two modes of Thru, Reflect and Line

	Differential mode	Common mode
Thru	$\mathbf{T}_{\mathbf{dd}}^{\mathbf{T}} = \begin{pmatrix} T_{dd11}^{T} & T_{dd12}^{T} \\ T_{dd21}^{T} & T_{dd22}^{T} \end{pmatrix}$	$\mathbf{T}_{\mathbf{cc}}^{\mathbf{T}} = \begin{pmatrix} T_{cc11}^{T} & T_{cc12}^{T} \\ T_{cc21}^{T} & T_{cc22}^{T} \end{pmatrix}$
Reflect	$\mathbf{T}_{\mathbf{dd}}^{\mathbf{R}} = \begin{pmatrix} T_{dd11}^{R} & T_{dd12}^{R} \\ T_{dd21}^{R} & T_{dd22}^{R} \end{pmatrix}$	$\mathbf{T}_{\mathbf{cc}}^{\mathbf{R}} = \begin{pmatrix} T_{cc11}^{R} & T_{cc12}^{R} \\ T_{cc21}^{R} & T_{cc22}^{R} \end{pmatrix}$
Line	$\mathbf{T}_{\mathbf{dd}}^{\mathbf{L}} = \begin{pmatrix} T_{dd11}^{L} & T_{dd12}^{L} \\ T_{dd21}^{L} & T_{dd22}^{L} \end{pmatrix}$	$\mathbf{T}_{\mathbf{cc}}^{\mathbf{L}} = \begin{pmatrix} T_{cc11}^{L} & T_{cc12}^{L} \\ T_{cc21}^{L} & T_{cc22}^{L} \end{pmatrix}$

As the error determination for each mode is identical and independent one from each other, the following calculations will be presented for differential mode.



(a) (b) (c)

Figure II-7: TRL Patterns. (a) Thru. (b) Reflect. (c) Line

The transfer matrix of Thru and Line (Figure II-7(a) and (c)) is determined by Eq. (II-35), and (II-36) respectively.

$$\mathbf{T}_{\mathbf{dd}}^{\mathbf{T}} = \mathbf{T}_{\mathbf{dd}}^{\mathbf{in}}.\mathbf{T}_{\mathbf{dd}}^{\mathbf{out}} \tag{II-35}$$

$$\mathbf{T}_{\mathbf{dd}}^{\mathbf{L}} = \mathbf{T}_{\mathbf{dd}}^{\mathbf{in}}.\mathbf{T}_{\mathbf{dd}}^{\mathbf{\Delta L}}.\mathbf{T}_{\mathbf{dd}}^{\mathbf{out}} \tag{II-36}$$

Where $\mathbf{T}_{\mathbf{dd}}^{\mathbf{\Delta L}}$ describes the differential-mode transfer matrix of the LINE. Its characteristic impedance is considered as the reference impedance. T_{dd12} and T_{dd21} are zero; and T_{dd22} is the inverse of T_{dd11}.

$$\mathbf{T}_{\mathbf{dd}}^{\mathbf{\Delta L}} = \begin{pmatrix} X_d & 0 \\ 0 & X_d^{-1} \end{pmatrix} \tag{II-37}$$

From Eq. (II-35) and (II-36), we have:

$$\mathbf{Q} = \mathbf{T}_{\mathbf{dd}}^{\mathbf{L}}.\mathbf{T}_{\mathbf{dd}}^{\mathbf{T}\,-1} = \mathbf{T}_{\mathbf{dd}}^{\mathbf{in}}.\mathbf{T}_{\mathbf{dd}}^{\mathbf{\Delta L}}.\mathbf{T}_{\mathbf{dd}}^{\mathbf{in}\,-1} \tag{II-38}$$

Because the two matrices **Q** and $\mathbf{T}_{\mathbf{dd}}^{\mathbf{\Delta L}}$ are similar, X_d and X_d^{-1} equal to the eigenvalues of **Q**.

$$X_d = \frac{Q_{11} + Q_{22} \pm \sqrt{(Q_{11} - Q_{22})^2 + 4Q_{12}Q_{21}}}{2} \tag{II-39}$$

We choose the value of X_d so that the element $\mathbf{A}_{\mathbf{dd}11}$ determined as follows is nearly equal to unity. The equations (II-35) and (II-36) are re-written as a two-equation system of two unknown variables $\mathbf{A_{dd}}$ and $\mathbf{B_{dd}}$.

$$\begin{cases} \mathbf{T}_{\mathbf{dd}}^{\mathbf{T}} = \mathbf{A}_{\mathbf{dd}} + \mathbf{B}_{\mathbf{dd}} \\ \mathbf{T}_{\mathbf{dd}}^{\mathbf{L}} = \mathbf{A}_{\mathbf{dd}} X_d + \mathbf{B}_{\mathbf{dd}} X_d^{-1} \end{cases} \tag{II-40}$$

Where:

$$\mathbf{A_{dd}} = \begin{pmatrix} T_{dd11}^{in}T_{dd11}^{out} & T_{dd11}^{in}T_{dd12}^{out} \\ T_{dd21}^{in}T_{dd11}^{out} & T_{dd21}^{in}T_{dd12}^{out} \end{pmatrix} \quad \text{(II-41)}$$

$$\mathbf{B_{dd}} = \begin{pmatrix} T_{dd12}^{in}T_{dd21}^{out} & T_{dd12}^{in}T_{dd22}^{out} \\ T_{dd22}^{in}T_{dd21}^{out} & T_{dd22}^{in}T_{dd22}^{out} \end{pmatrix} \quad \text{(II-42)}$$

$\mathbf{A_{dd}}$ and $\mathbf{B_{dd}}$ can be totally determined as the solutions of Eq. (II-40).

$$\mathbf{A_{dd}} = \frac{\mathbf{T_{dd}^{L}} - \mathbf{T_{dd}^{T}} X_d^{-1}}{X_d - X_d^{-1}} \quad \text{(II-43)}$$

$$\mathbf{B_{dd}} = \mathbf{T_{dd}^{T}} - \mathbf{A_{dd}} \quad \text{(II-44)}$$

Next, we calculate the following ratios:

$$k_{dd1}^{in} = \frac{T_{dd21}^{in}}{T_{dd11}^{in}} = \frac{A_{dd21}}{A_{dd11}},\ k_{dd2}^{in} = \frac{T_{dd12}^{in}}{T_{dd22}^{in}} = \frac{B_{dd12}}{B_{dd22}} \quad \text{(II-45)}$$

$$k_{dd1}^{out} = \frac{T_{dd12}^{out}}{T_{dd11}^{out}} = \frac{A_{dd12}}{A_{dd11}},\ k_{dd2}^{out} = \frac{T_{dd21}^{out}}{T_{dd22}^{out}} = \frac{B_{dd21}}{B_{dd22}} \quad \text{(II-46)}$$

Another ratio will be determined from Reflect measurement (Figure II-7(b)). We have

$$\begin{pmatrix} b_{1d} \\ a_{1d} \end{pmatrix} = T_{dd}^{in}\begin{pmatrix} a_{Ad} \\ b_{Ad} \end{pmatrix} \Leftrightarrow a_{1d}\begin{pmatrix} S_{dd11}^{R} \\ 1 \end{pmatrix} = T_{dd}^{in}\begin{pmatrix} \Gamma_{dd}^{in} \\ 1 \end{pmatrix} b_{Ad} \quad \text{(II-47)}$$

$$\begin{pmatrix} b_{Cd} \\ a_{Cd} \end{pmatrix} = T_{dd}^{out}\begin{pmatrix} a_{2d} \\ b_{2d} \end{pmatrix} \Leftrightarrow b_{Cd}\begin{pmatrix} 1 \\ \Gamma_{dd}^{out} \end{pmatrix} = T_{dd}^{out}\begin{pmatrix} 1 \\ S_{dd22}^{R} \end{pmatrix} a_{2d} \quad \text{(II-48)}$$

Where

- ✓ Γ_{dd}^{in}, and Γ_{dd}^{out} are un-known differential-mode reflect coefficients of input and output accesses respectively.
- ✓ S_{dd11}^{R}, and S_{dd22}^{R} are measured.

We can get reflect coefficients from Eq. (II-47), and (II-48).

$$\Gamma_{dd}^{in} = -\frac{T_{dd12}^{in} - T_{dd22}^{in} S_{dd11}^{R}}{T_{dd11}^{in} - T_{dd21}^{in} S_{dd11}^{R}} = -\frac{T_{dd22}^{in}}{T_{dd11}^{in}} \frac{k_{dd2}^{in} - S_{dd11}^{R}}{1 - k_{dd1}^{in} S_{dd11}^{R}} \tag{II-49}$$

$$\Gamma_{dd}^{out} = \frac{T_{dd22}^{out}}{T_{dd11}^{out}} \frac{k_{dd2}^{out} + S_{dd22}^{R}}{1 + k_{dd1}^{out} S_{dd22}^{R}} \tag{II-50}$$

We assume that the reflect coefficients are the same for input and output accesses. From Eq. (II-49) and (II-50), we have:

$$\frac{T_{dd22}^{in}}{T_{dd11}^{in}} \frac{T_{dd11}^{out}}{T_{dd22}^{out}} = -\frac{1 - k_{dd1}^{in} S_{dd11}^{R}}{k_{dd2}^{in} - S_{dd11}^{R}} \frac{k_{dd2}^{out} + S_{dd22}^{R}}{1 + k_{dd1}^{out} S_{dd22}^{R}} \tag{II-51}$$

In addition:

$$\frac{T_{dd11}^{in}}{T_{dd22}^{in}} \frac{T_{dd11}^{out}}{T_{dd22}^{out}} = \frac{A_{dd11}}{B_{dd22}} \tag{II-52}$$

The division of Eq. (II-51) by Eq. (II-52) gives another ratio.

$$k_{dd3}^{in} = \frac{T_{dd22}^{in}}{T_{dd11}^{in}} = \pm\sqrt{-\frac{B_{dd22}}{A_{dd11}} \frac{1 - k_{dd1}^{in} S_{dd11}^{R}}{k_{dd2}^{in} - S_{dd11}^{R}} \frac{k_{dd2}^{out} + S_{dd22}^{R}}{1 + k_{dd1}^{out} S_{dd22}^{R}}} \tag{II-53}$$

The reflection coefficient of the Reflect (Figure II-7.b.) is expressed from the input and output accesses parameters:

$$\Gamma_{dd} = -k_{dd3}^{in} \frac{k_{dd2}^{in} - S_{dd11}^{R}}{1 - k_{dd1}^{in} S_{dd11}^{R}} \tag{II-54}$$

The root of k_{dd3}^{in} in Eq. (II-53) is chosen according to the closer argument of Γ_{dd} from the value defined in the cal-kit. Finally,

$$\begin{cases} \mathbf{T}_{\mathbf{dd}}^{\mathbf{in}} = T_{dd11}^{in} \begin{pmatrix} 1 & k_{dd2}^{in} k_{dd3}^{in} \\ k_{dd1}^{in} & k_{dd3}^{in} \end{pmatrix} \\ \mathbf{T}_{\mathbf{dd}}^{\mathbf{out}} = \mathbf{T}_{\mathbf{dd}}^{\mathbf{in}^{-1}} \mathbf{T}_{\mathbf{dd}}^{\mathbf{T}} \end{cases} \tag{II-55}$$

The common mode elements are exactly calculated by the same way.

$$\begin{cases} \mathbf{T}_{\mathbf{cc}}^{\mathbf{in}} = T_{cc11}^{in} \begin{pmatrix} 1 & k_{cc2}^{in} k_{cc3}^{in} \\ k_{cc1}^{in} & k_{cc3}^{in} \end{pmatrix} \\ \mathbf{T}_{\mathbf{cc}}^{\mathbf{out}} = \mathbf{T}_{\mathbf{cc}}^{\mathbf{in}^{-1}} \mathbf{T}_{\mathbf{cc}}^{\mathbf{T}} \end{cases} \quad \text{(II-56)}$$

The values T_{dd11}^{in} and T_{cc11}^{in} will be eliminated during the de-embedding procedure. Thus their values are not important. They can have a same value, for example:

$$T_{dd11}^{in} = T_{cc11}^{in} = 0.5 \quad \text{(II-57)}$$

The mixed-mode TRL de-embedding steps are summarized in Figure II-8.

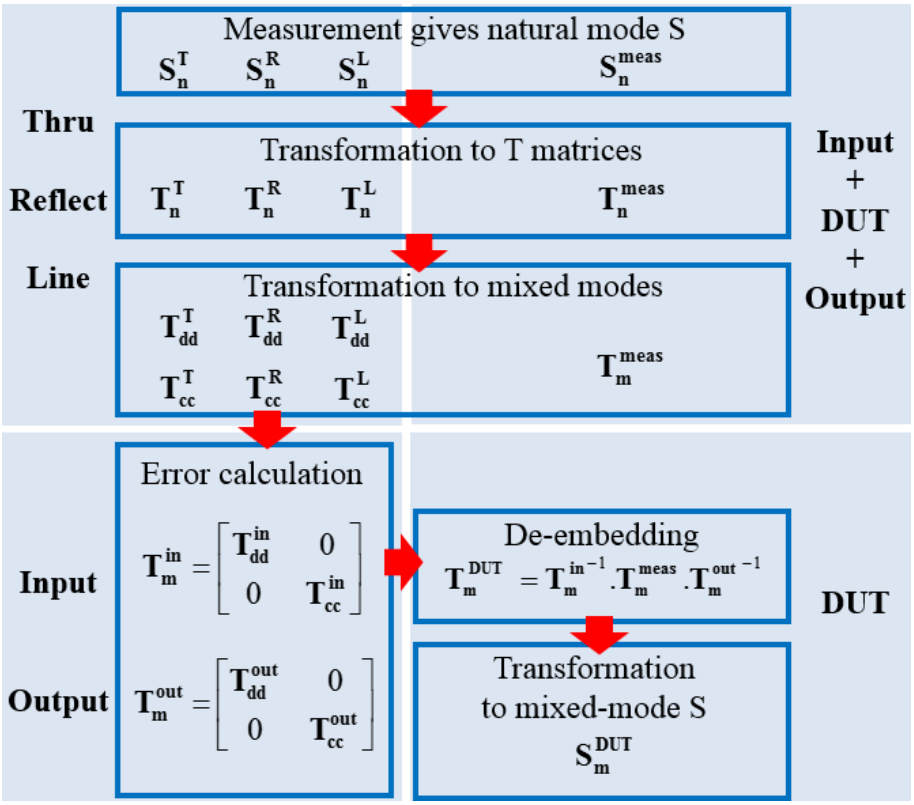
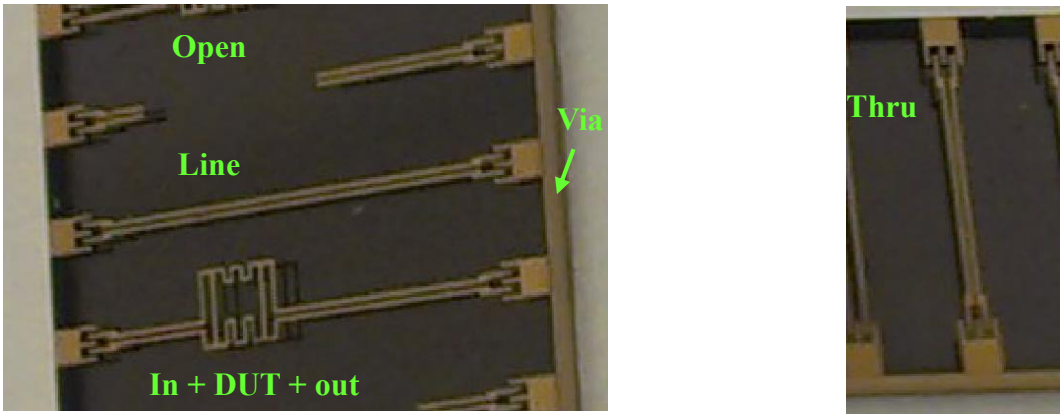


Figure II-8: TRL de-embedding procedure

II.2.3. Experiment and verification

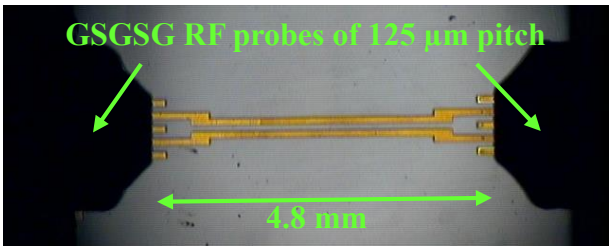
Some test structures, consisting of a Thru, an Open, a Line and a DUT + Accesses, have been realized on a glass substrate of 500 µm thickness to verify the mixed-mode TRL de-embedding method (Figure II-9). There is a ground plane under the test structures. The ground planes are connected by metalizing the edges of the substrate. The DUT is a branch line which has been asymmetrically designed to have the couplings between mixed modes.



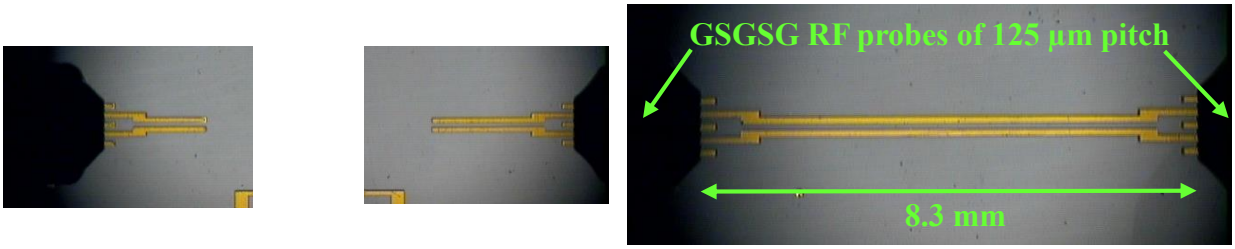
(a) (b)

Figure II-9: TRL de-embedding test structure. (a) Open, Line and DUT + in, out accesses. (b) Thru

The measurements have been performed by a four-port VNA from 10 kHz to 8.5 GHz (Figure II-10). A tier SOLT calibration has been made on an external cal-kit. The measurement results of Thru, Open, Line and DUT + Accesses have been used to calculate the S parameters of DUT using the mixed-mode de-embedding method in this section.



(a)



(b) (c)

Figure II-10: Test structures under measurement. (a) Thru. (b) Open. (c) Line

EM simulation has been used to evaluate the de-embedding method. The S parameters from EM simulation are in natural mode and referenced to 50Ω. In order to compare two methods, they must be converted to mixed modes and be referenced to the impedances of the LINE. Firstly, the simulated S parameters are converted into mixed modes using Eq. (II-31). Then, their referenced

impedance is changed using Eq. (II-58). The Line in this work has a differential impedance of 100Ω, and a common impedance of 192 Ω.

$$\mathbf{S}_{\mathbf{m}}^{\mathbf{DUT}} = \mathrm{ztos}\left(\mathbf{Z}_{\mathbf{dc}}^{\boldsymbol{\Delta l}}.\mathrm{stoz}\left(\mathbf{S}_{\mathbf{m50\Omega}}^{\mathbf{DUT}}, 50\Omega\right), \mathbf{Z}_{\mathbf{dc}}^{\boldsymbol{\Delta l}}, 1\Omega\right) \tag{II-58}$$

Where:

- ✓ $\mathbf{S}_{\mathbf{m50\Omega}}^{\mathbf{DUT}}$, $\mathbf{S}_{\mathbf{m}}^{\mathbf{DUT}}$ are mixed-mode S parameters referenced to 50Ω and to the impedances of LINE respectively
- ✓ ztos and stoz are Keysight's ADS commands transforming from Z to S and from S to Z parameters respectively
- ✓ $\mathbf{Z}_{\mathbf{dc}}^{\boldsymbol{\Delta l}} = \mathrm{diag}\left(\frac{1}{\sqrt{Z_d^{\Delta l}}}, \frac{1}{\sqrt{Z_d^{\Delta l}}}, \frac{1}{\sqrt{Z_c^{\Delta l}}}, \frac{1}{\sqrt{Z_c^{\Delta l}}}\right)$
- ✓ $Z_d^{\Delta l}$, $Z_c^{\Delta l}$ are the differential and common impedances of the Line respectively

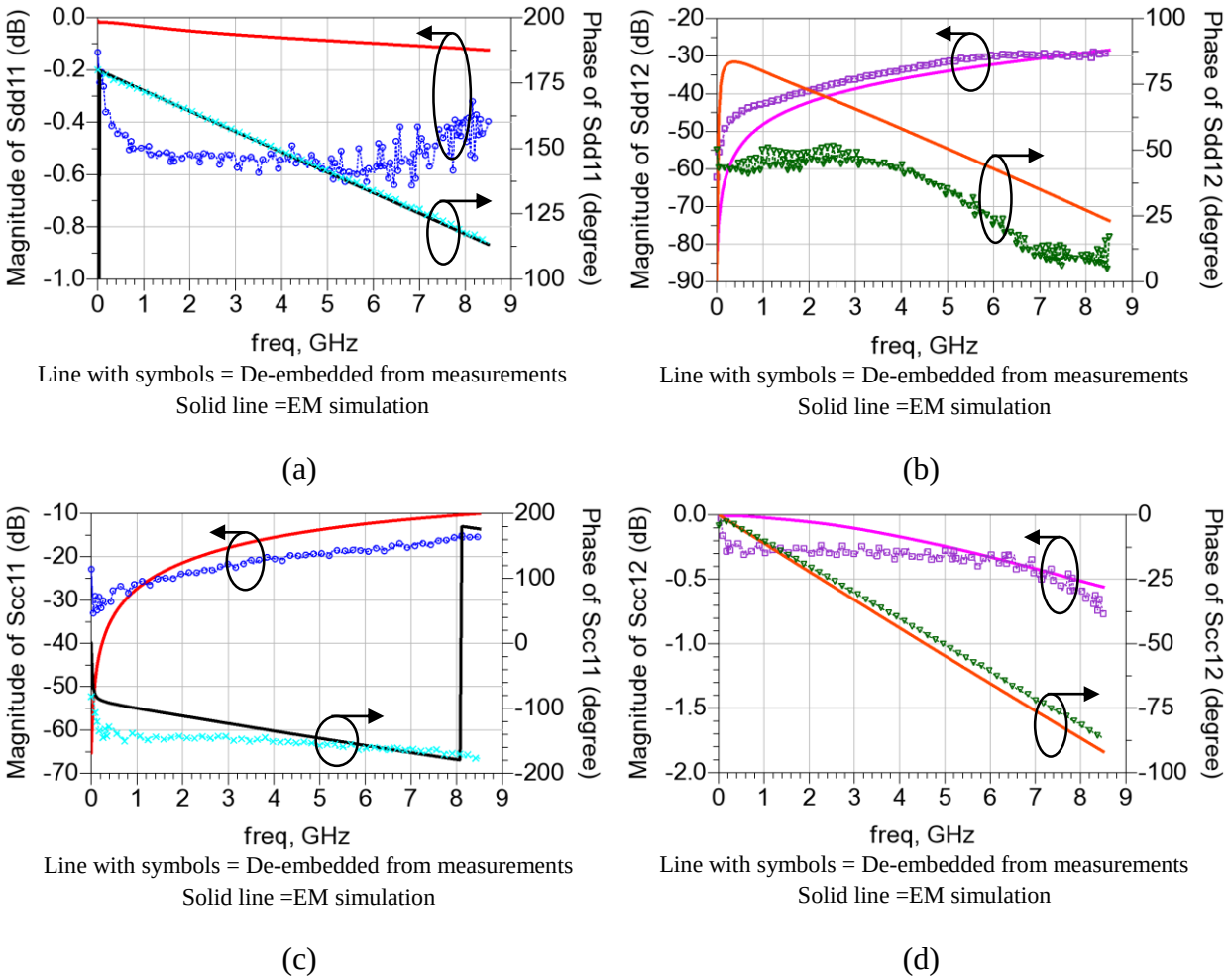


Figure II-11: TRL mixed-mode de-embedding method Vs EM simulation. (a) S_{dd11}. (b) S_{dd12}. (c) S_{cc11}. (d) S_{cc12}

The comparisons for differential and common modes have been shown in Figure II-11 with good agreement both in magnitude and phase. The lines with symbols correspond to the de-embedding method, and the solid lines represent EM simulation. The observable difference in magnitude of S_{dd11} in Figure II-11(a) is resulted by an ohmic problem. In fact, experiment has always more loss than simulation due to contact resistance, metal resistance…

Figure II-12 shows a further verification for the coupling between differential and common modes. The experimental results are close to the simulated ones.

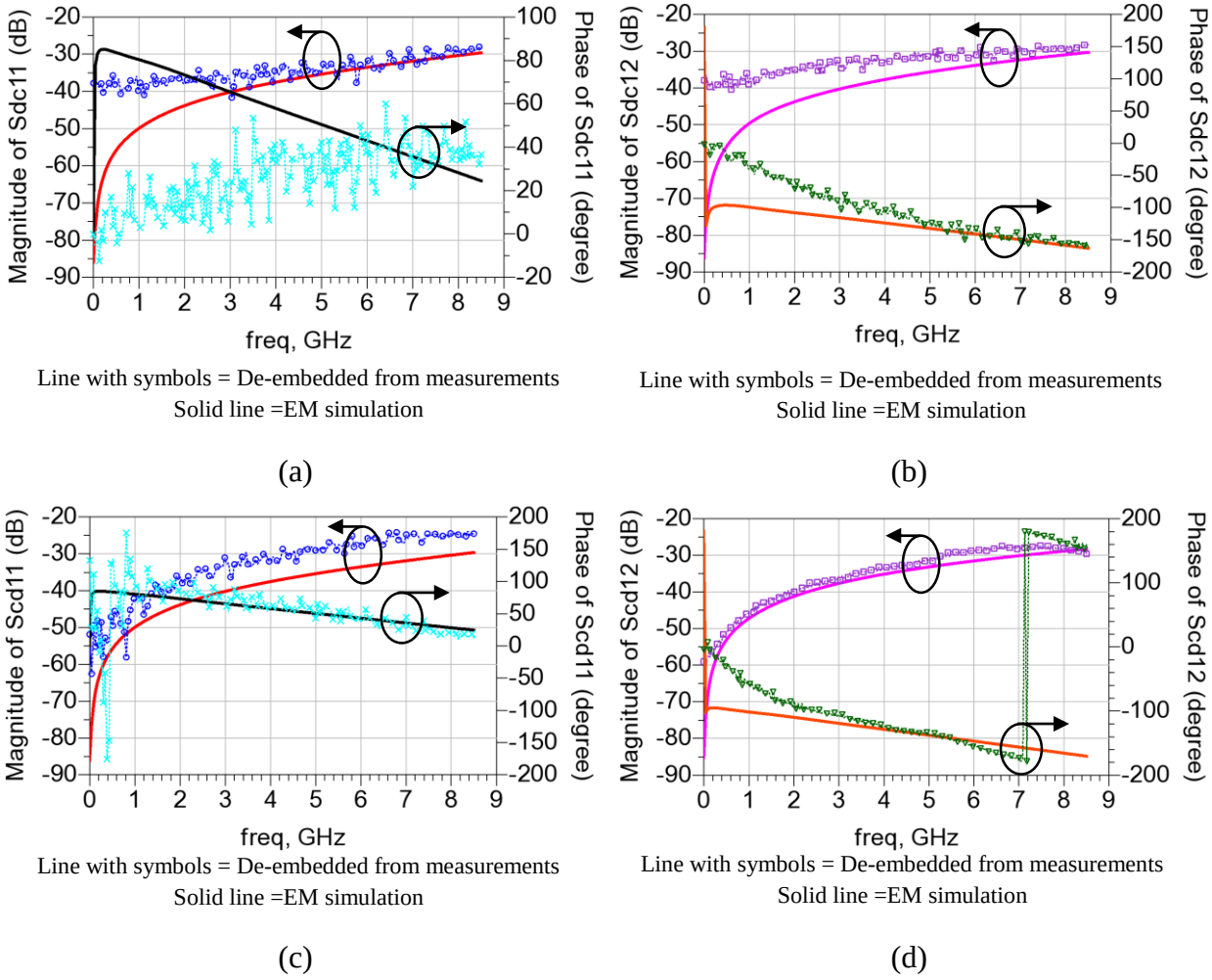
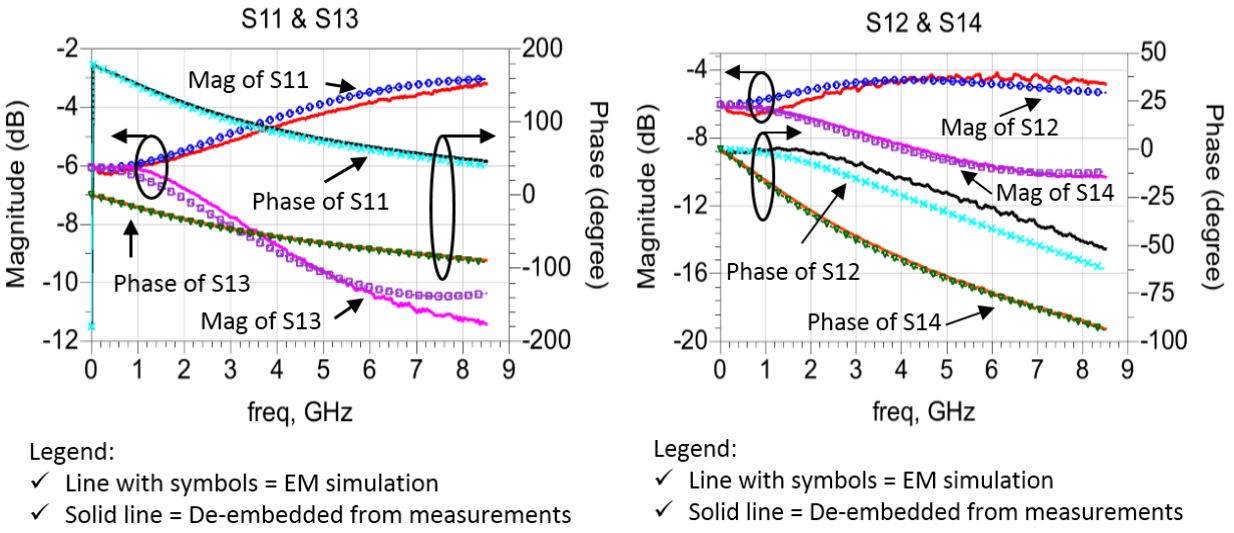


Figure II-12: Comparison of coupling between mixed modes (TRL mixed-mode de-embedding method Vs EM simulation). (a) S_{dc11}. (b) S_{dc12}. (a) S_{cd11}. (b) S_{cd12}

Another evaluation in natural modes gives also a good agreement up to 8.5 GHz in Figure II-13. The lines with symbols correspond to EM simulation, and the solid lines represent the de-embedding method. Because the S parameters in natural modes are necessary for the

characterization of mutual coupling, this TRL mixed-mode de-embedding method can be extended for measuring the coupling between interconnections.



(a) (b)

Figure II-13: Verification of TRL de-embedding method in comparison with EM simulation. (a) S_{11} and S_{13}. (b) S_{12} and S_{14}.

II.2.4. Conclusion

The TRL mixed-mode de-embedding method presented in this chapter has given a good result up to 8.5 GHz in comparison with EM simulation. The method has been evaluated in both mixed modes and natural modes. The method is applicable to measure differential devices and mutual coupling between interconnections in a package.

II.3. Four-port measurement by a two-port VNA

When only a two-port VNA is available for the measurement of an *N*-port DUT, the most used method consists of designing C_2^N identical circuits with N-2 ports terminated by a match. This takes a large area on a wafer and the termination (generally 50 Ω) could be not so accurate. Here we propose a method that uses only one circuit on the wafer. Our method is fully compatible with on-wafer characterization and provides directly the S-parameters in the device reference planes. In some cases, where a calibration is not directly possible in the DUT reference planes, the device accesses need to be characterized and modeled.

The organization of this paragraph consists of four parts. The technique that was used for these preliminary calculations is presented in section II.3.1. Section II.3.2 describes the different steps of the procedure leading to the final scattering S-parameters of the multi-port. Then, section II.3.3 presents an application of the method to a branch-line coupler. Finally, section II.3.4 concludes the method.

II.3.1. Extraction of Access Model Parameters

For lossy substrates, direct TRL calibration cannot be simple because the complex impedance reference is not easy to determine. So, we propose to perform an external LRM calibration on a separate commercial calibration substrate. Theoretically, the accesses can be modeled by two passive two-ports, this leads to a 7 error models (3 complex parameters for each two-port and the on wafer access characteristic impedance). By designing the accesses in order to have their electrical lengths equal to the electrical half-length of the "thru" standard of the LRM, we can simplify the error model (Figure II-14). The accesses between the LRM and DUT reference planes can then be modeled by the impedances Z_1, Z_2, Z_3 and Z_4. If the access lengths are correctly adjusted, Z_1 and Z_3 are small.

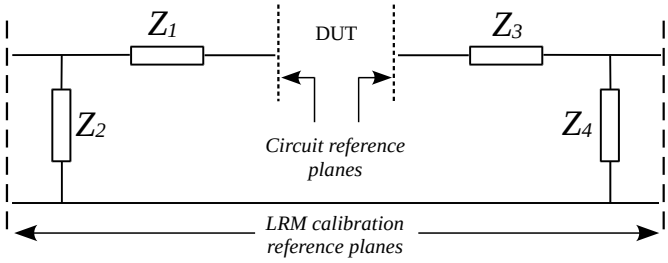


Figure II-14: Modelization of the accesses

A de-embedding procedure is necessary to extract the DUT S-parameters in its reference planes. For this purpose, a short and an open are designed on the same chip in the reference planes (Figure

II-15). The open measurement gives Z_2 and Z_4, the short measurement gives $Z_1//Z_2$ and $Z_3//Z_4$ and hence Z_1 and Z_3.

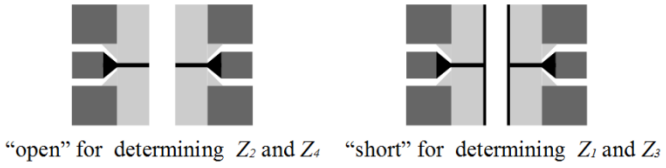


Figure II-15: "open" and "short" standards

The de-embedding can be carried out using the following procedure.$1/Z_2$ and $1/Z_4$ are subtracted from the diagonal parameters of the Y-matrix extracted from the measured S-matrix. After a Y to Z transformation, Z_1 and Z_3 are subtracted from the diagonal parameters. The resulting Z-matrix may be transformed into the DUT S-matrix defined between its reference planes. This can be expressed by the relation (II-59) where AtoB() functions, are the A to B transformation matrices.

$$\mathbf{S_{DUT}} = \mathrm{ZtoS}\left(\mathrm{YtoZ}\left(\mathrm{StoY}\left(\mathbf{S_{meas}}\right) - \begin{pmatrix} \frac{1}{Z_2} & 0 \\ 0 & \frac{1}{Z_4} \end{pmatrix}\right) - \begin{pmatrix} Z_1 & 0 \\ 0 & Z_2 \end{pmatrix}\right) \qquad \text{(II-59)}$$

II.3.2. Multi-port Measurement Procedure

In order to characterize N-port devices with traditional two-port VNA, a combination of C_2^N measurements have to be performed between all the ports of the device. While two ports of the N-port device are used in a measurement path, we propose to keep the other ports terminated with quasi-open. Each of these $N(N\text{-}1)/2$ measurements produces a 2x2 S-parameter matrix which is a function of the quasi-open terminations presented at non-connected ports. These quasi-open terminations are constituted by the access pads of the device. Such terminations represent loads seen from the DUT reference planes. Given their proximity to an ideal open-circuit, they can be considered as a simple admittance. In the following, this admittance is quoted as Y_T and need to be taken into account in the procedure. We also assume that this admittance is the same at each non-connected port.

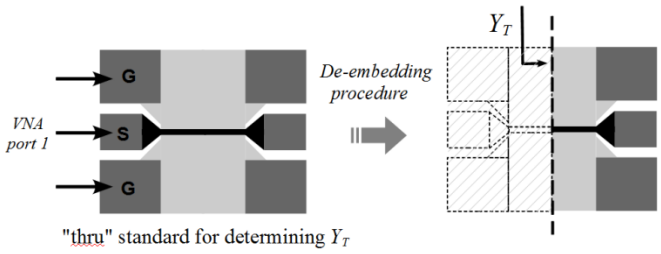


Figure II-16: Definition of the admittance Y_T

We measure Y_T with the "thru" standard with only one probe, the other access being left free. Then, Y_T is obtained after de-embedding of the left half "thru" as shown in Figure II-16.

Then, to characterize an *N*-port device the probes are laid on two pads *i* and *j* among *N* as shown in Figure II-17. The other pads are free and are seen from the *N-2* other DUT reference planes as the admittance Y_T. A de-embedding procedure is applied to the two accesses *i* and *j* in order to move the reference planes in the plane P.

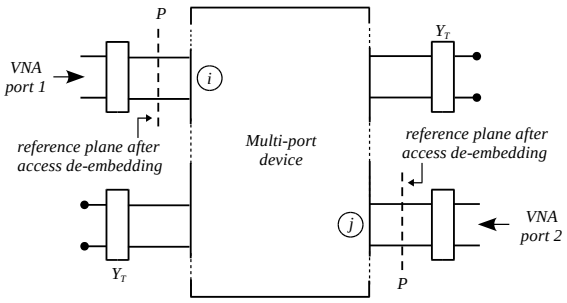


Figure II-17: Configuration of the multi-port with *N-2* open accesses

To remove the effect of Y_T, we need an NxN matrix with the same terminations for each port. Hence, we have to add Y_T to ports *i* and *j* in the 2x2 measured matrices. For that, the obtained 2x2 S-matrices are transformed into 2x2 Y-matrices and the admittance Y_T is added at the measured ports. This configuration after adding Y_T is shown in Figure II-18.

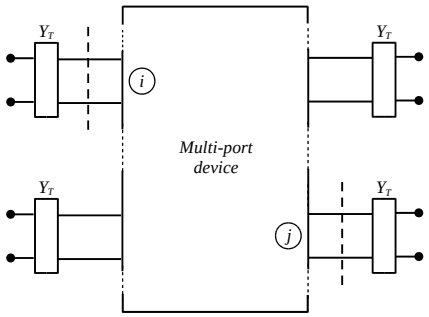


Figure II-18: Configuration after adding Y_T at the measured ports

In this configuration, where the accesses are ended by an open, the impedance formalism representation is more suitable to describe rigorously the linear behavior of the circuit. Thus, each obtained admittance sub-matrix is transformed to its equivalent 2x2 Z-matrix.

$$\mathbf{Z_E} = \begin{pmatrix} Z_{11}^{14}\text{or}Z_{11}^{12}\text{or}Z_{11}^{13} & Z_{12}^{12} & Z_{12}^{13} & Z_{12}^{14} \\ Z_{21}^{12} & Z_{11}^{24}\text{or}Z_{22}^{12}\text{or}Z_{11}^{33} & Z_{12}^{23} & Z_{12}^{24} \\ Z_{21}^{13} & Z_{21}^{23} & Z_{11}^{34}\text{or}Z_{22}^{23}\text{or}Z_{22}^{13} & Z_{12}^{34} \\ Z_{21}^{14} & Z_{21}^{24} & Z_{21}^{34} & Z_{22}^{34}\text{or}Z_{22}^{24}\text{or}Z_{22}^{14} \end{pmatrix} \quad \text{(II-60)}$$

Once completed, the whole N-port Z-matrix is reconstituted by combining all the 2x2 impedance matrices previously obtained. We note that different solutions are possible for the diagonal terms of the reconstituted NxN Z-matrix. In the particular case of a four-port device, the 4x4 Z-matrix could be reconstituted as presented in Eq. (II-60). In this relation $[Z^{ij}]$, are assumed to be the 2x2 sub-matrices measured between ports *i* and *j*.

Finally, to come down in the circuit reference plane, we have to eliminate the admittance Y_T at the different ports. This could be done by transforming the impedance matrix into its equivalent admittance matrix and then subtracting the admittance Y_T from the diagonal terms (Eq.(II-61)). Y_T should not be too close to the short circuit area otherwise the accuracy of the method would be reduced.

$$\mathbf{Y} = \mathbf{Y_E} - Y_T\mathbf{I} \tag{II-61}$$

Where **I** is the identity matrix. **Y** is finally transformed into the desired S-matrix defined in the DUT reference planes.

II.3.3. Application to Four-port Circuit

In order to check the validity of the proposed measurement method for characterizing four-port devices, a branch-line coupler with its associated standards "open", "short" and "thru" are designed and fabricated using Austria-Micro-Systems BiCMOS 0.35µm process (Figure II-19).

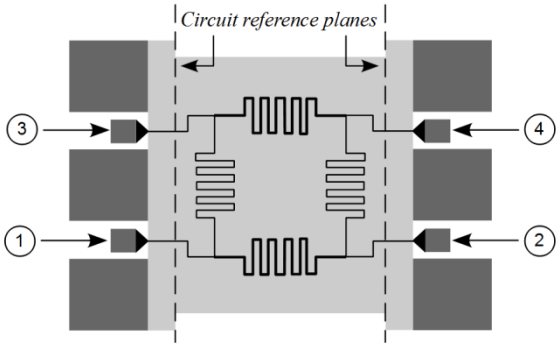


Figure II-19: The integrated branch-line coupler

The circuit was first measured by a two-port VNA corresponding to the proposed method and the obtained S-parameters are shown with solid lines in Figure II-20. The same device was measured using four-port VNA through two ground-signal-ground-signal-ground (GSGSG) microprobes. The corresponding S-parameters are shown with circular symbols. The comparison shows a good agreement showing the validity of the method. A slight difference can be observed.

This is due to the fact that the condition on the access lengths has not been met with the calibration substrate used for the four-port measurement.

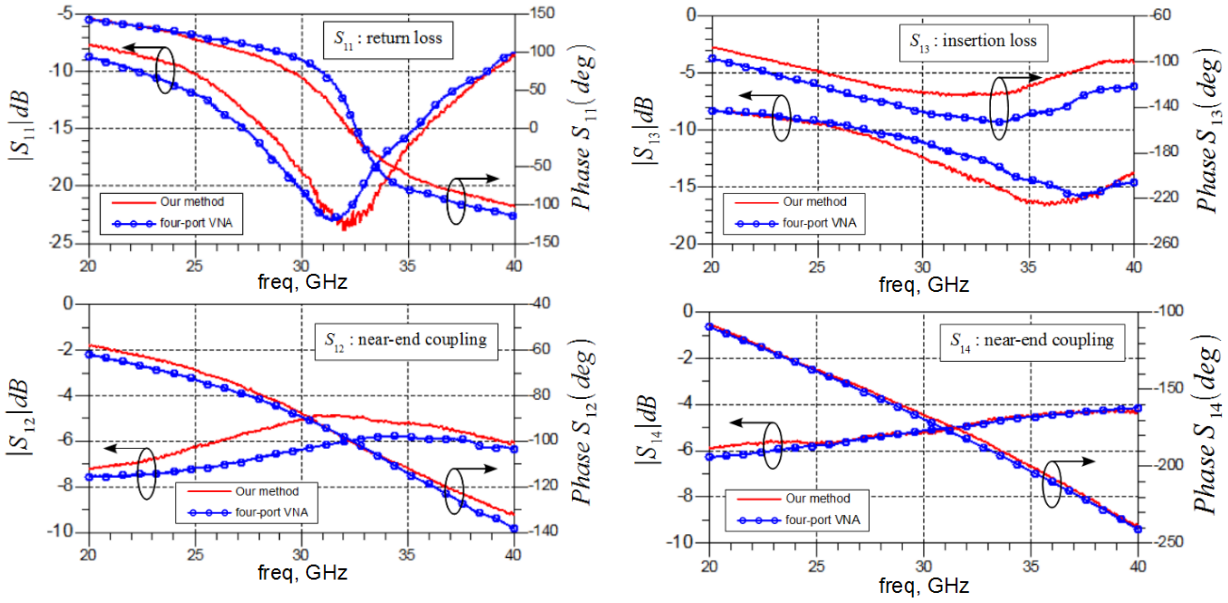


Figure II-20: Measurement of a branch-line four-port, with our method and with a four-port VNA

II.3.4. Conclusion

A simple technique has been described to measure the S-parameters of an N-port device at its reference planes using a two-port VNA. For each measurement, the unused N-2 ports are left open. The proposed method has been successfully verified with a branch-line coupler measured with a four-port VNA. On the one hand, this technique allows an accurate characterization of multi-port passive and stable devices. On the other hand, it allows a characterization cost saving in terms of test set equipment and used wafer area.

Nonetheless, due to the high reflection coefficient at non-connected ports, the device must be stable at this measurement configuration. The method applies well to passive circuits, but the stability for active circuits must be checked, even outside the measurement bandwidth. This method will be applied in the next section for the MEMS switches characterization in which a two-port VNA will be used to measure multi-port circuits.

II.4. MEMS Switches characterization

II.4.1. Introduction

The switches to be characterized are based on Micro Electro-Mechanical system (MEMS) technology. In switch package, the MEMS chip is controlled by an ASIC driver (Figure II-21). The switch contacts made of gold are protected by a silicon cap against thermal, and mechanical constraints in package.

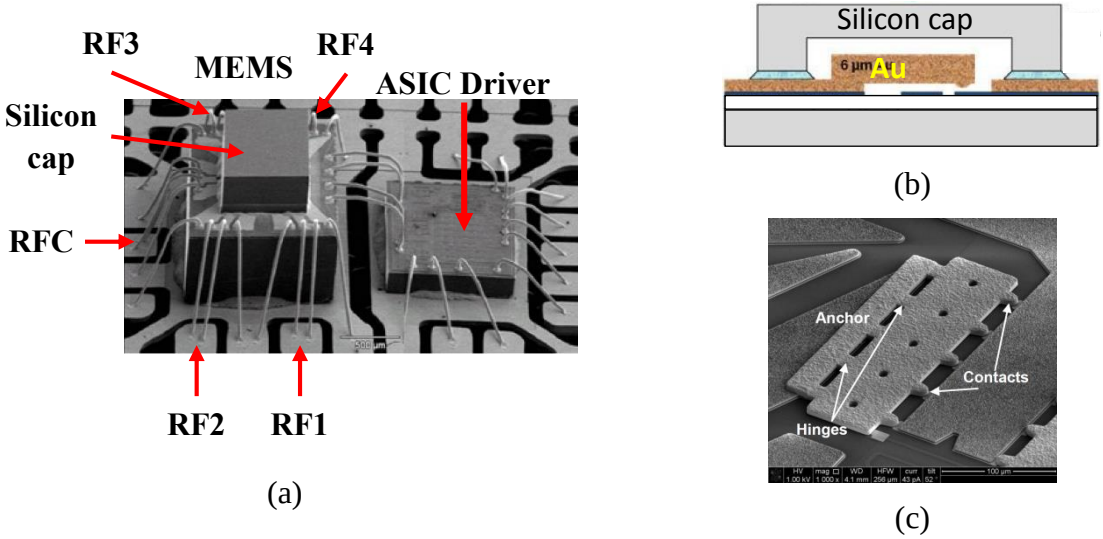


Figure II-21: SP4T MEMS Switch [43]. (a) Switch package. (b) MEMS contacts protected by a cap. (c) SEM image of MEMS contact

In this thesis, we want to characterize two switch types: Single Pole, Double Throw (SPDT) and Single Pole, Four Throw (SP4T). Pole is named RFC, and throws are named RF*i* (*i* = 1, 2 …). When a throw RF*i* is closed, an electrical channel RFC-RF*i* will be created. The signal can pass through this channel from RFC to RF*i*. Opening throw RF*i* makes the electrical channel RFC-RF*i* open. The important RF characteristic for a closed channel is its insertion loss, and for an open channel, it is its off isolation. Response times are also important. The requirements for the MEMS switch characterization are as follows:

- ✓ Off isolation less than -15 dB at 18 GHz
- ✓ Insertion loss more than -1.5 dB at 18 GHz
- ✓ Response time less than 200 µs

Two types of characterization will be done:

- ✓ RF measurements performed by a VNA from 10 MHz to 20 GHz.
- ✓ Response time measurements performed with an oscilloscope and generators.

II.4.2. RF measurement

The RF characterization follows the steps shown in Figure II-22. Firstly, the switch packages will be measured on a PCB. In the second and third steps, the plastic molding and Si cap will be removed to study their effects. Then, the MEMS chip without package and PCB will be directly measured in step 4. If the performance of the switch packages does not match the above requirements, the characterization will be continued with an improved version of the MEMS switch.

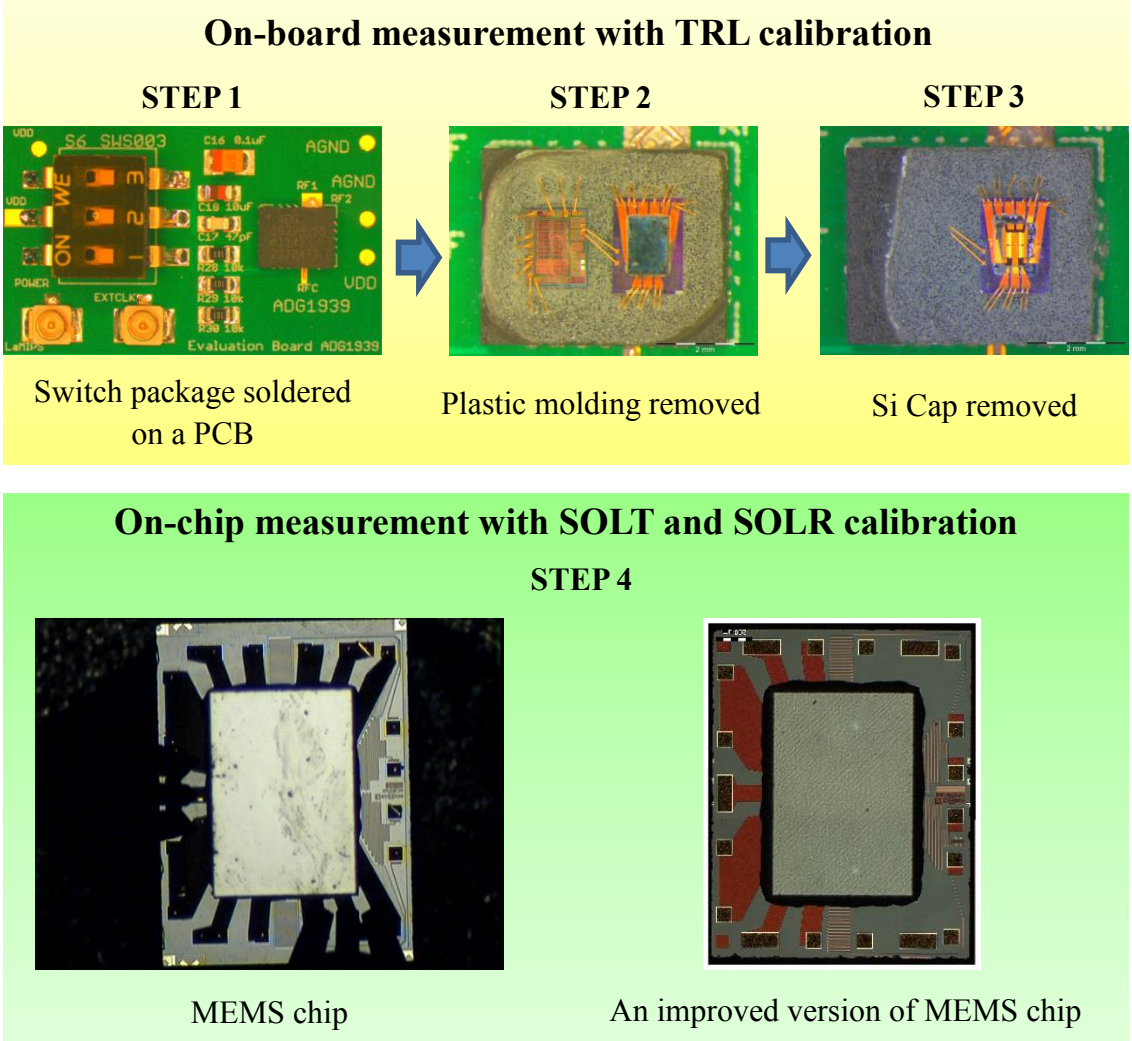


Figure II-22: RF characterization steps

Figure II-23(a) describes the test bench for RF characterization using a two-port Vector Network Analyzer (VNA) and G-S-G RF probes from 10 MHz to 20 GHz. Figure II-23(b), (c), and (d) present the calibration kits used in the RF measurements. For the on-board measurements from step 1 to 3, the Thru-Reflect-Line (TRL) calibration has been implemented directly on the board. The TRL cal-kit has been designed on the same board of switches to take the access line shape into account. For the on-chip measurements in step 4, Short-Open-Load-Thru (SOLT) and Short-Open-Load-Reciprocal Thru (SOLR) calibrations were used. SOLT calibration is used if two probes are

mounted opposite from one another. Meanwhile, SOLR calibration is used if two probes are oriented orthogonally to one another. The algorithms of the calibration methods mentioned above are already integrated in the VNA.

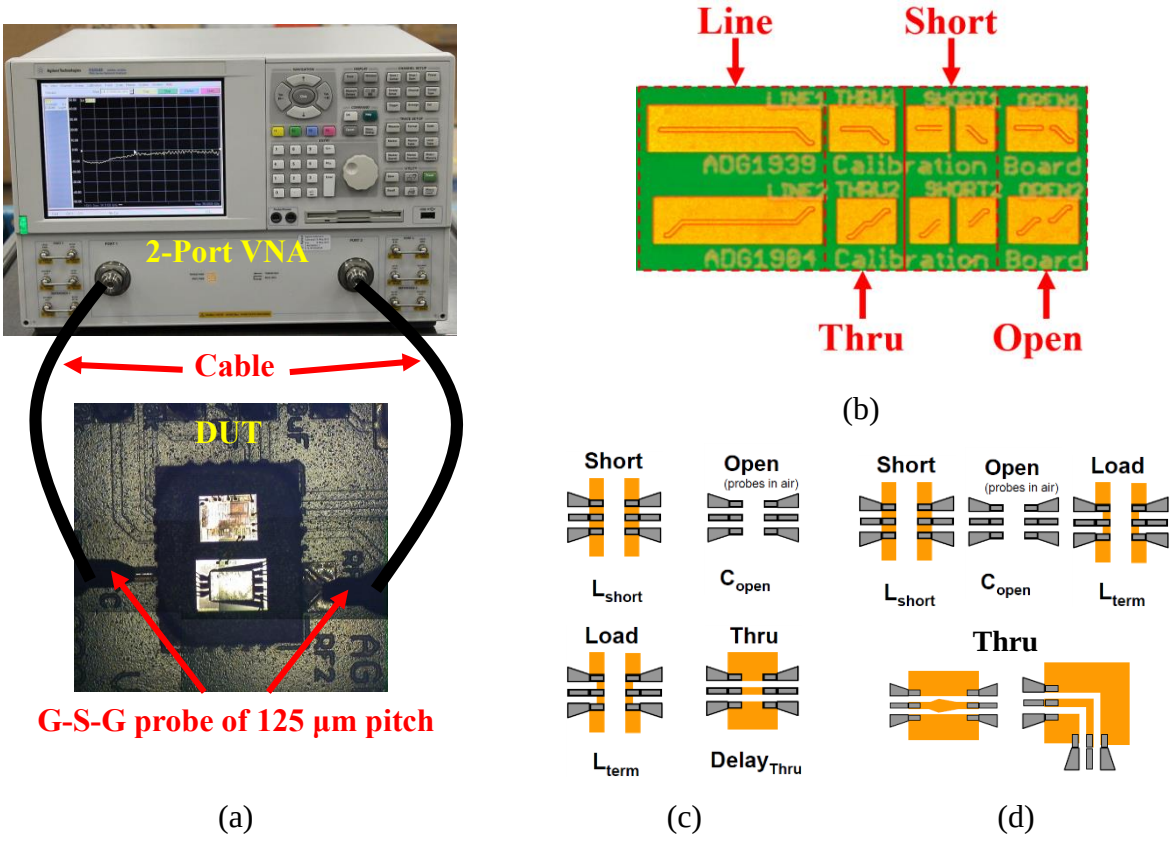


Figure II-23: RF measurement test bench. (a) Test bench. (b) TRL kit. (c) SOLT kit. (d) SOLR kit.

During a measurement between two ports, the other ports were left open. Thus, to have the S parameters of switches, the results need to be combined by using the technique presented in section II.3. Three two-port measurements must to be successfully done to reconstitute the S parameters for one state of SPDT switches. The S parameters reconstitution for one state of SP4T switch needs ten two-port measurements. The quality of evaluation boards, MEMS switch after being soldered on PCB, chip surface influence much two-port combination possibility. Only one combination cannot measured, the S parameters of switch state cannot be reconstructed. Therefore, some results presented in the next sections are obtained from two-port measurement.

II.4.2.1. Switch package soldered on an evaluation PCB

One-layer PCBs shown in Figure II-24 have been designed to evaluate the RF performance of the switch packages. These boards have been realized on an alumina substrate with a relative permittivity of 10.2, and with a thickness of 1.27 mm. The characteristic impedance of the RF accesses is 50Ω. In addition, a TRL cal-kit taking in account accesses shapes has been also designed on the same board of the switch packages (Figure II-23(b)). A thin layer of flash gold has been deposited on RF accesses to make a good contact with RF probes during measurements. The evaluation boards are powered by a 3VDC source. The ON/OFF state of the MEMS switches is changed by using a manual switch (see Figure II-24).

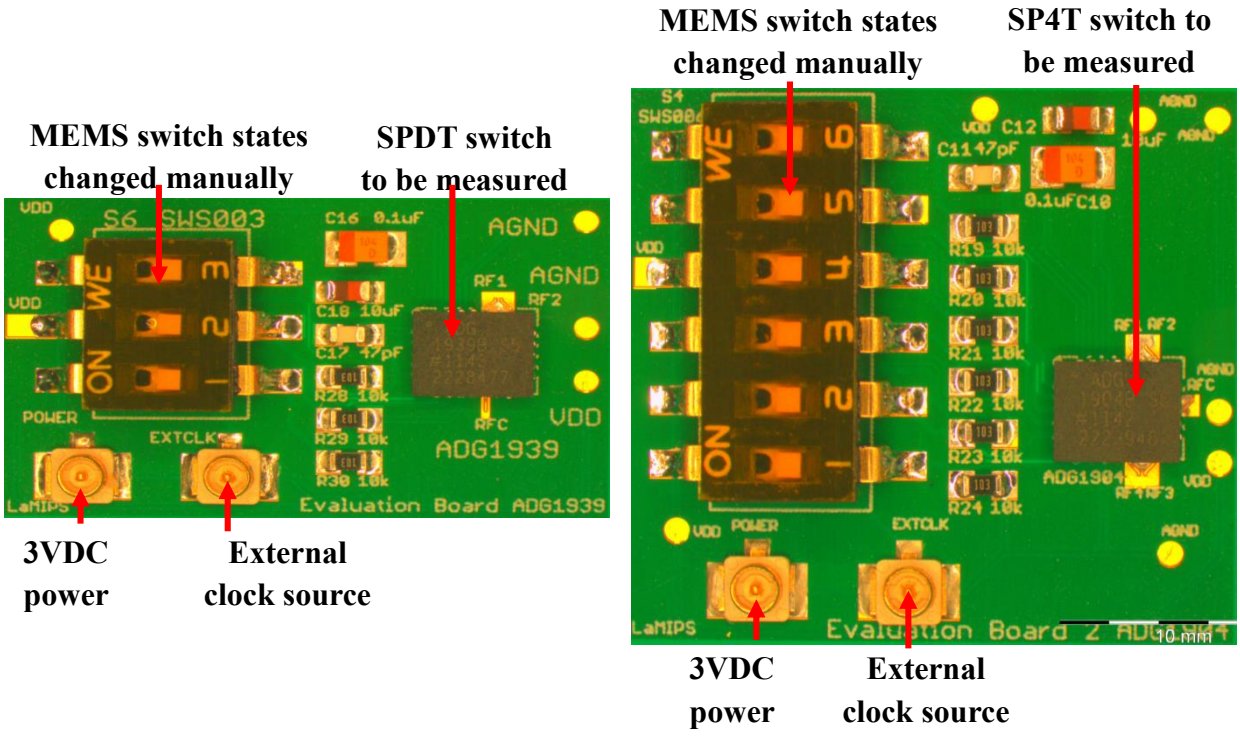


Figure II-24: MEMS switch packages soldered on an evaluation board. (a) SPDT switch. (b) SP4T switch

Figure II-25 shows the RF characteristics of the SP4T switch soldered on its evaluation board. These results are two-port measurement. There are two different bandwidths of -3 dB: 10.7 GHz for the RFC-RF4 electrical channel and 14.35 GHz for the RFC-RF3 electrical channel. When RFC-RF3 channel is closed, the Off Isolation (OI) between RFC and RF4 is always less than -20 dB from 0 to 13 GHz. Its maximal value is -11 dB at 13.87 GHz. The return loss on the RFC pole is less than -5 dB from 0 to 15 GHz.

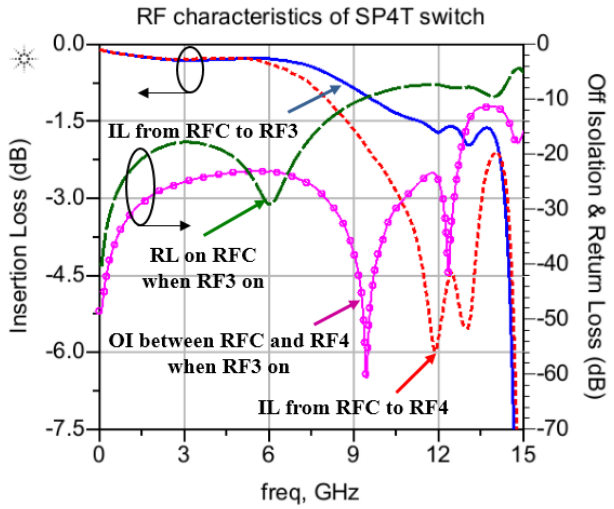


Figure II-25: RF characteristics of SP4T switch package soldered on an evaluation board

Figure II-26 presents the RF characteristics of the SPDT switch soldered on its evaluation board after a reconstitution from two-port measurements. When RFC-RF1 channel is closed, we got a bandwidth of -3dB at 8.8 GHz, an off isolation between RFC and RF2 less than -15 dB, and a return loss on RFC pole less than -5 dB from 0 to 10 GHz.

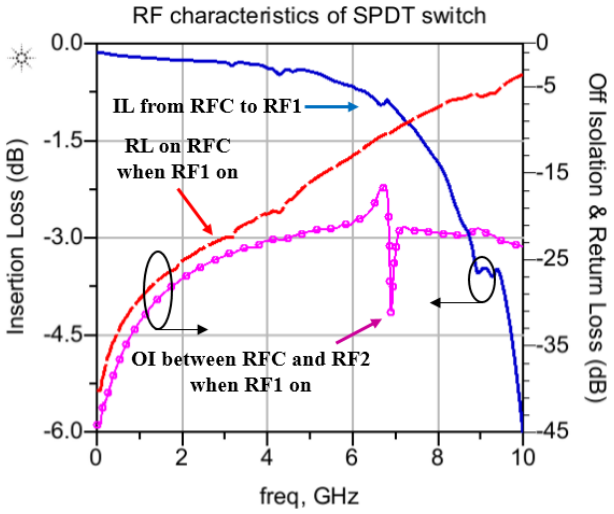


Figure II-26: RF characteristics of SPDT switch package soldered on an evaluation board

The difference in bandwidth can be explained by using the X-ray photo shown in Figure II-27 and Figure II-28. In SP4T switch, throw RF3 has a common ground plane with pole RFC, whereas throw RF4 does not (see Figure II-28(a)). Thus, in channel RFC-RF4, the current must pass through bonding wires and the ground plane under MEMS contact to make a closed loop. That reason makes the electrical length of channel RFC-RF4 longer than the one of channel RFC-RF3. As a result, the bandwidth of channel RFC-RF4 is smaller than the one of channel RFC-RF3. The

difference between the bandwidth of two switch types can be explained by the same way. Figure II-27(a) shows the throws of SPDT switch which have no common ground plane with the pole RFC. Consequently, the electrical length of SPDT channels is longer than the one of RFC-RF3 channel of SP4T switch.

II.4.2.2. Molding effects

The plastic molding of the SPDT switches has been removed to study the variation of switch RF characteristics. In order to choose a suitable removal procedure, the internal circuits of the switch packages need to be investigated by X-ray.

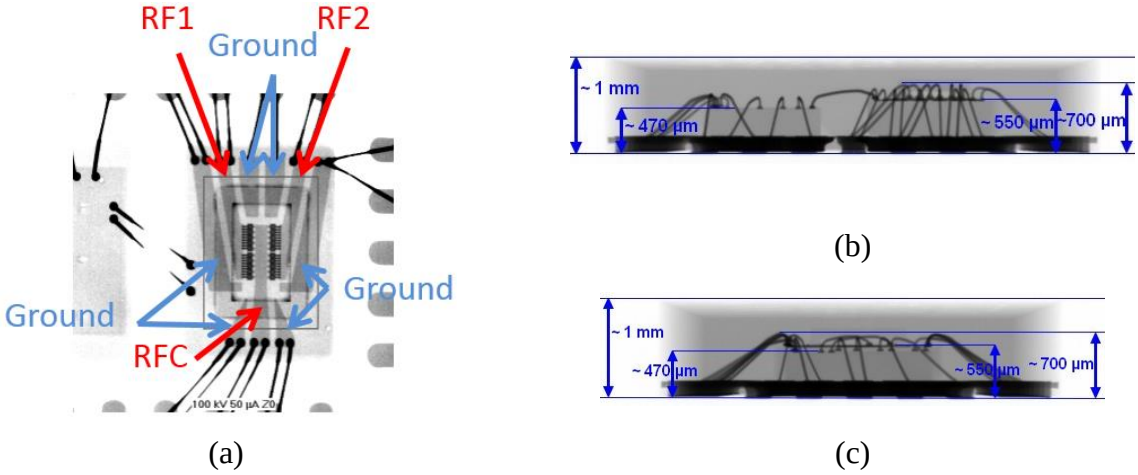


Figure II-27: SPDT X-ray photos. (a) Top view. (b) Front view. (c) Side view.

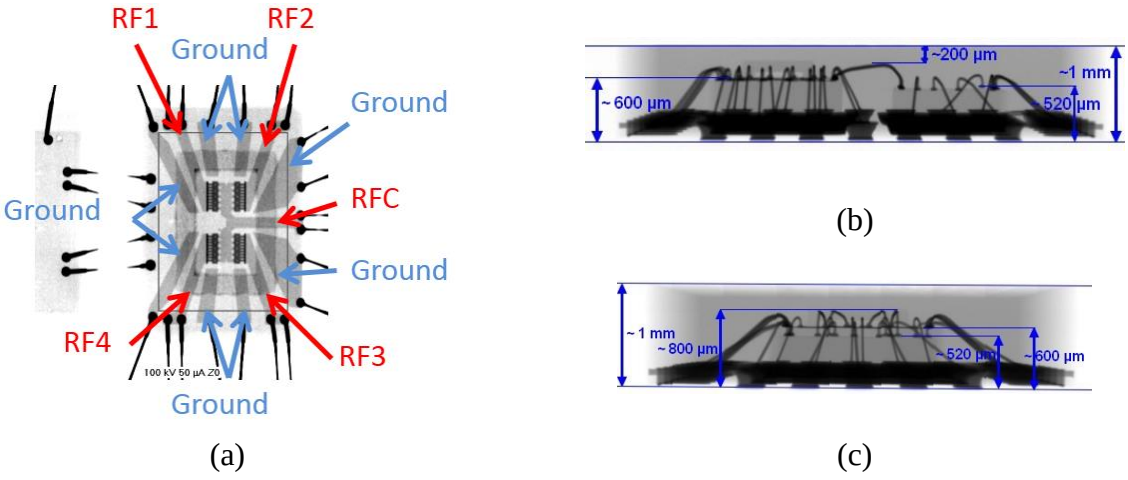


Figure II-28: SP4T X-ray photos. (a) Top view. (b) Front view. (c) Side view.

In Figure II-27 and Figure II-28, we see clearly MEMS chip, and can also estimate some dimensions of the packages. The RF ports have been designed using coplanar configuration in which a signal is between two grounds. This configuration permits signal and ground on the same

plane. There is a plastic layer of 200 µm thickness above the highest point of the metal interconnections (Figure II-28(b)). Therefore, the removal process has been begun by laser light destroying quickly the 200 µm plastic layer. Acid was used to remove the plastic rest which is close to gold interconnections. The removal results are shown in Figure II-29.

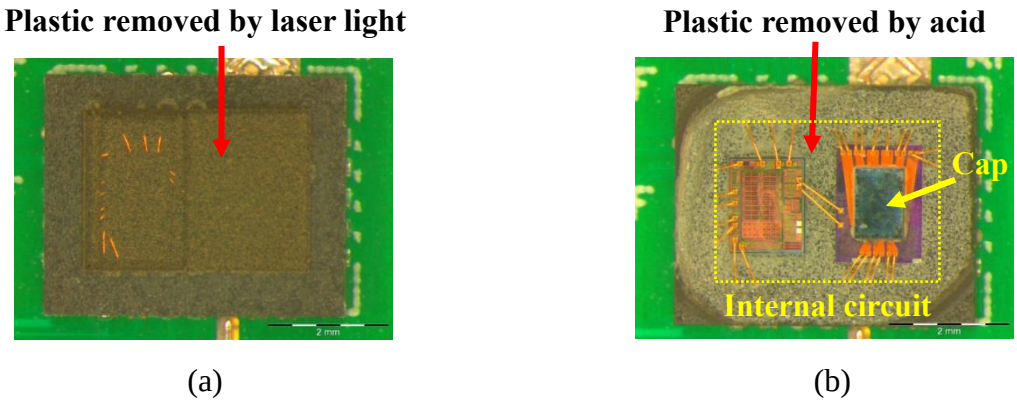
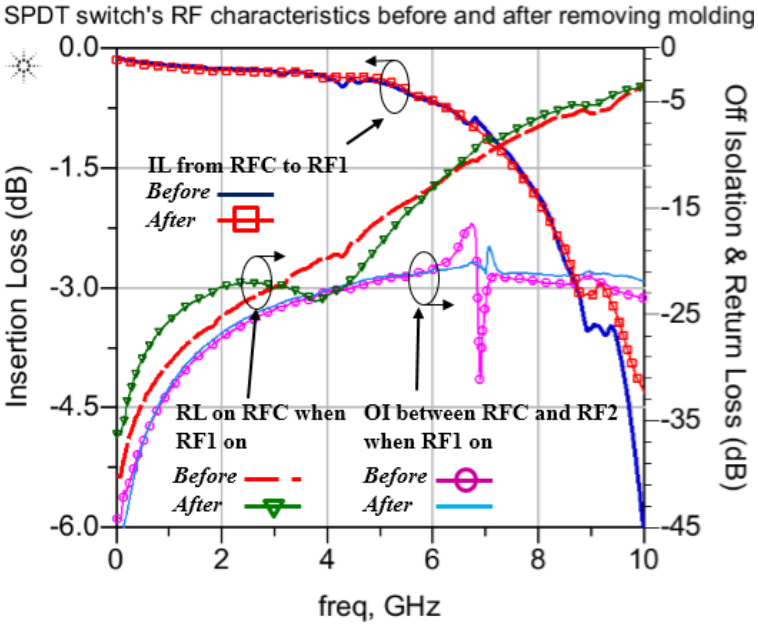
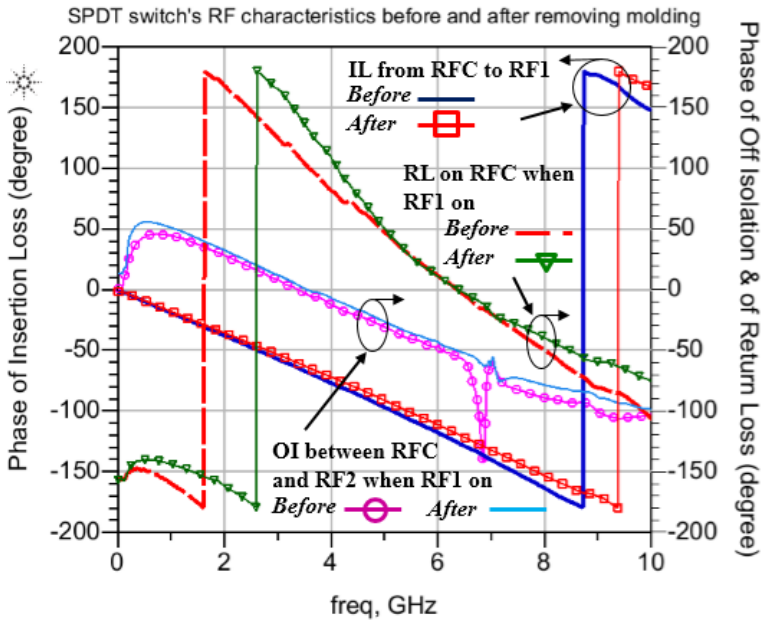


Figure II-29: Plastic molding removal process. (a) After laser step. (b) After acid step.

Being reconstituted from two-port measurements, the 3-port S parameters of the SPDT switch before and after the removal process have been compared to each other in Figure II-30. In magnitude comparison (Figure II-30(a)), removing molding increases the bandwidth 0.5 GHz, but maintains the figures for the return loss and the off isolation. Phase shift is presented in Figure II-30(b) due to the change of mutual capacitances in the packages. Therefore, molding has an effect only on the phase of the RF characteristics of the MEMS switches. As the molding removal has not significantly increased the bandwidth of SPDT switch, it has not been applied for SP4T switch.



(a)



(b)

Figure II-30: Molding effects on SPDT switch (a) in magnitude and (b) in phase

II.4.2.3. Silicon cap effects

The MEMS contacts are protected by a silicon cap. Figure II-31 shows a SPDT switch without cap under measurement.

(a) (b)

Figure II-31: SPDT switch without cap. (a) After removing silicon cap. (b) Under test

Without cap, the MEMS switches are very fragile after a few measurements. Thus, we could not do all necessary two-port measurements to reconstitute 3-port S parameters. Figure II-32 shows two-port measurement results after an on-chip TRL calibration where bandwidth is limited to 10 GHz.

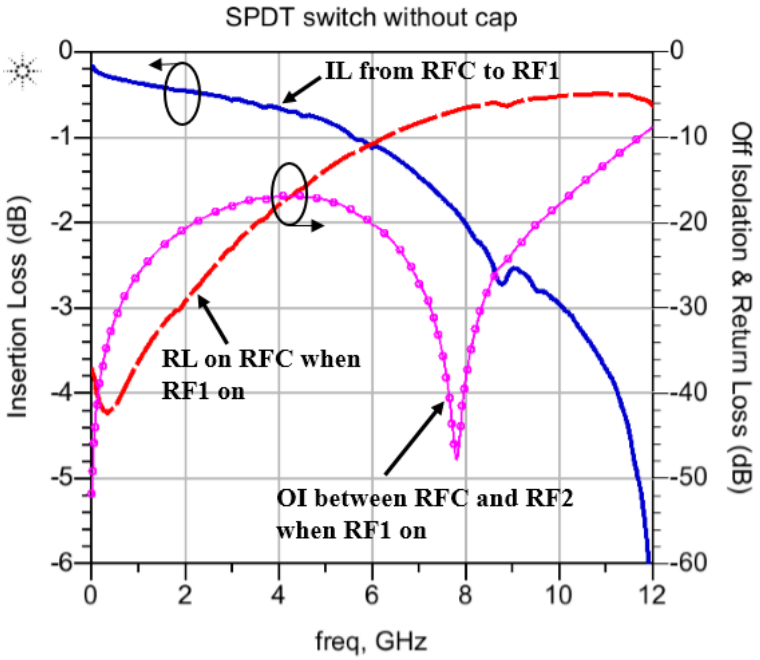
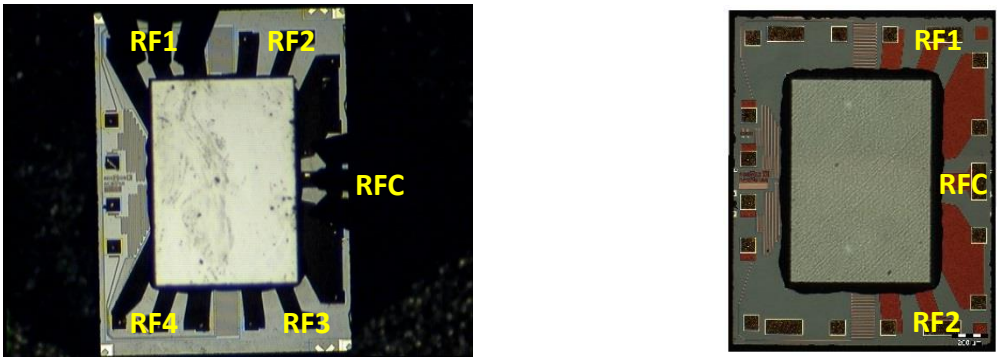


Figure II-32: Two-port measurement results of SPDT switch without cap

II.4.2.4. Package effects

In this step, the SP4T MEMS switches without package (Bonding-wires and molding) and without evaluation board (Figure II-33) are studied by an on-chip measurement. The limitation of chip surface does not permit placing two RF probes too closely to one another. For example, the on-chip measurements between RF1 and RF2, between RF3 and RF4 are impossible (see Figure II-33(a)). Therefore, the S parameters reconstitution has not been made for SP4T switch (Figure II-33(a)).



(a) (b)

Figure II-33: Direct measurements on switches. (a) SP4T switch under test. (b) An improved version of SPDT switch.

Figure II-34 compares the two-port measurements of SP4T switch in two cases: with and without package. A bandwidth of 17 GHz has been obtained from the measurements of SP4T switch without package. At low frequency, the two results are close to each other. From 13 GHz, a big difference in both insertion loss and off isolation appears. Therefore, package influences significantly the performance of circuits at high frequency.

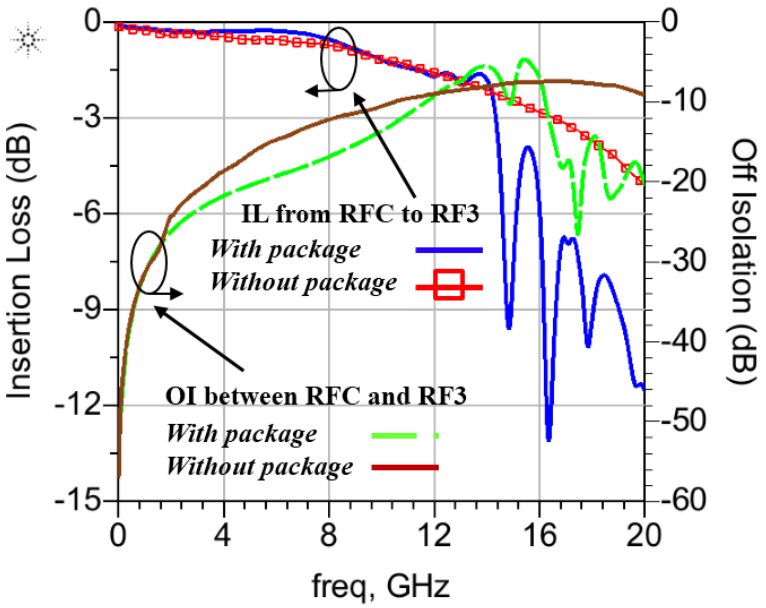


Figure II-34: A comparison between SP4T switch with and without package

An improved version of MEMS switch has been provided by manufacturer (see Figure II-33(b)). The difference between two versions is that the throws giving small bandwidth (RF1, and RF4) in the old version (Figure II-33(a)) has been removed. The chip surface of the improved SPDT switch allows measuring all two-port combinations necessary for S parameters reconstitution.

The 3-port RF characteristics are shown in Figure II-35 for different states. The un-physical phenomena at 2GHz in the Figure II-35(b)-(d) is probably due to a bad contact between MEMS and RF probe. Indeed, the aluminum micro-strips in MEMS switch are unfavorable for RF probes. When both RFC-RF1 and RFC-RF2 channel are open, a maximal off isolation is -9 dB at 14 GHz. When only one channel is closed, we got a bandwidth of -3 dB at 16 GHz, a maximal off isolation of -15dB and a maximal return loss of -5dB from 0 to 20 GHz. Finally, in case of both two channels are closed, bandwidth is much limited at 6.5GHz.

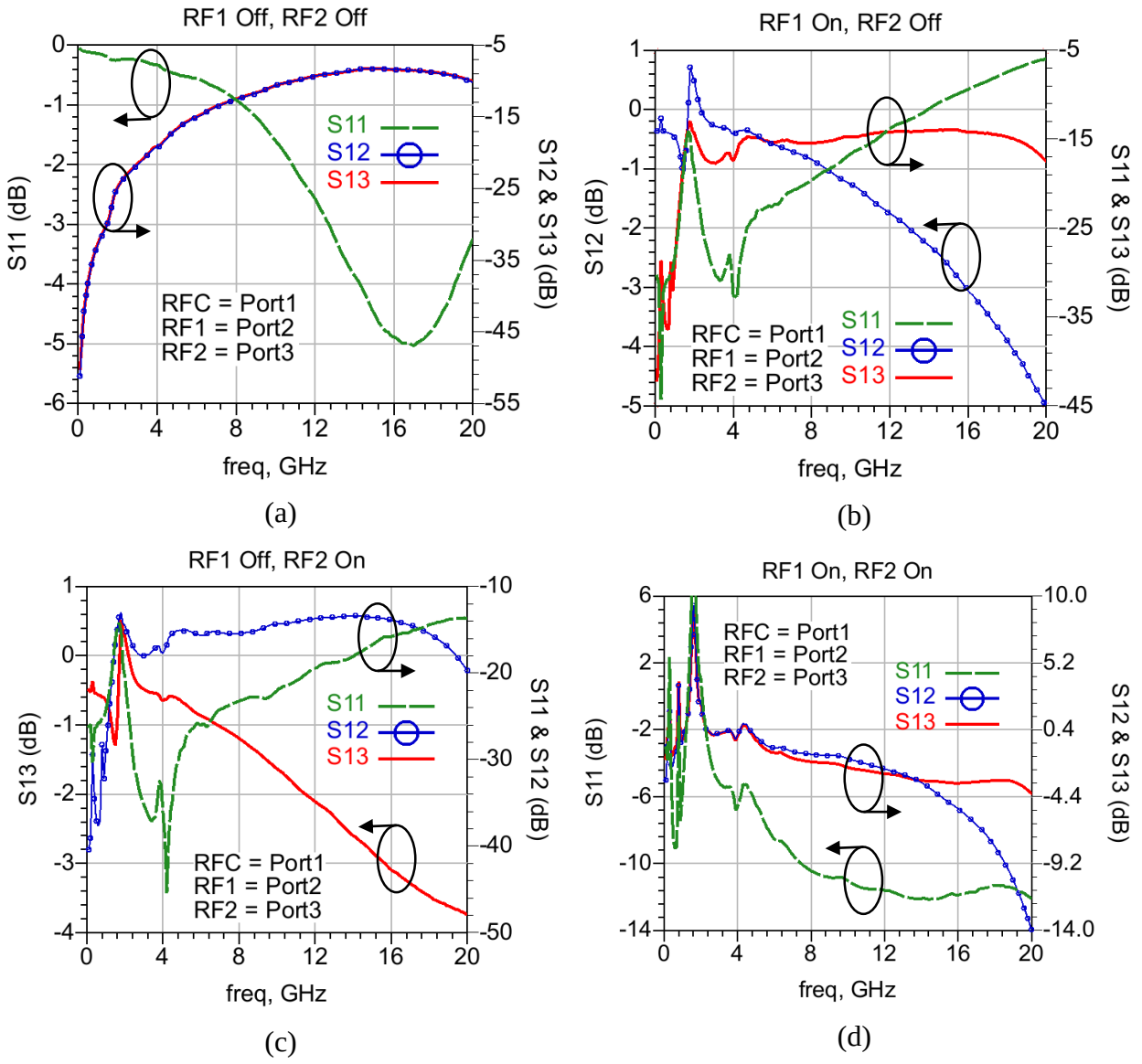
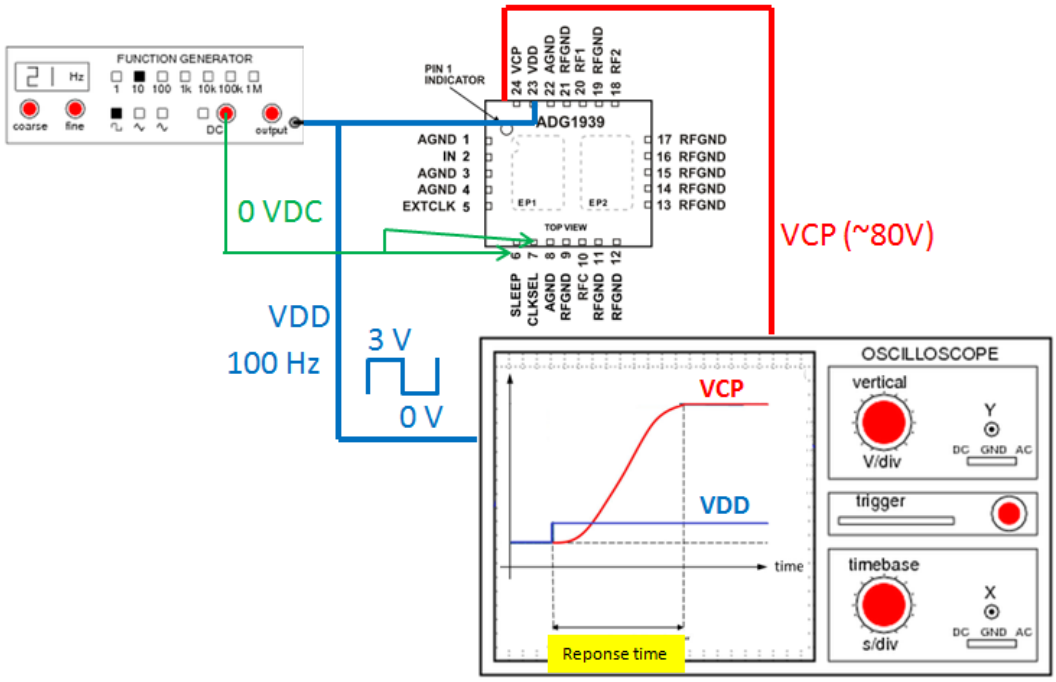
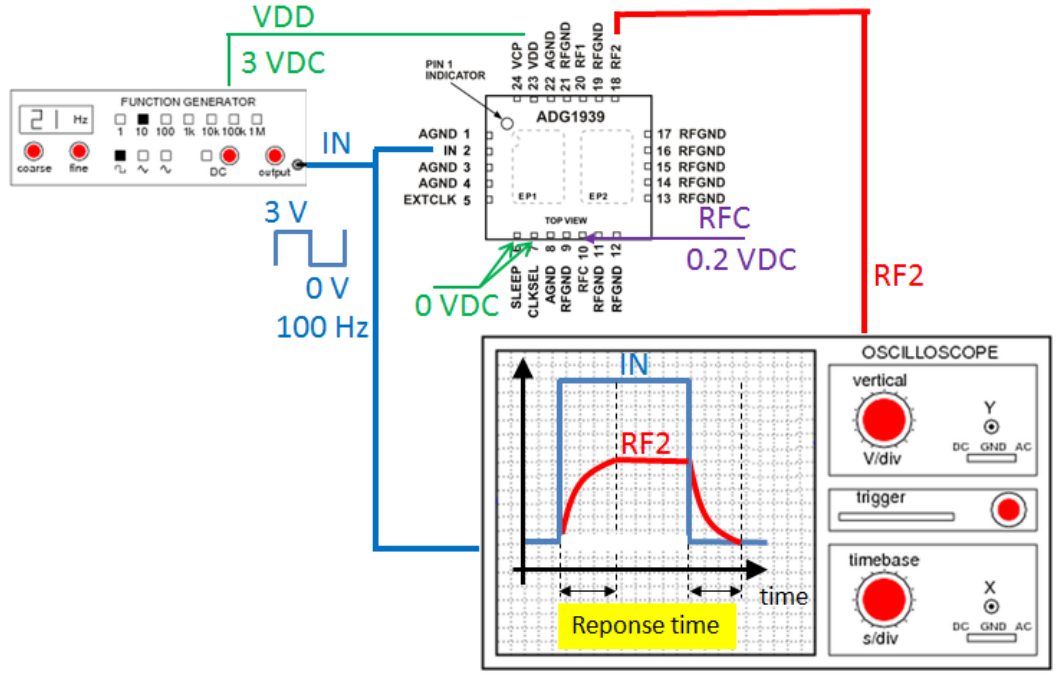


Figure II-35: RF characteristics of an improved SPDT switch. (a) RF1 and RF2 off. (b) RF1 on and RF2 off. (c) RF1 off and RF2 on. (d) RF1 and RF2 on.

II.4.3. Response time



(a)



(b)

Figure II-36: Response time test bench for (a) ASIC driver and (b) MEMS chip.

In switch application, response time is an important factor which must be as small as possible. It is defined as the time elapsed from a change of input signal to the moment where output signal

begins to stabilize. According to the state of input signal, response time is called on or off. The one corresponding to an application of input signal is named “ON” response time. In contrast, the one corresponding to stopping input signal is “OFF” response time.

The total response time of a package is contributed by its different parts. The MEMS switch packages are composed of an ASIC driver and a MEMS chip which will be separately measured. The test benches used for characterization are described in Figure II-36 where input signal is represented by blue lines, and output signal is symbolized by red lines. The green lines describe DC voltage necessary to operate switch package. Meanwhile, the violet lines in Figure II-36(b) illustrate a RF input. A function generator has been used to power the switch packages. Then, input and output signals have been observed by an oscilloscope. The input signal (blue lines) has been chosen as a square voltage with two levels (0V and 3V). As the input frequency must be small enough for output signal to begin to stabilize, it has taken a value of 100Hz.

The switch packages are powered by a 3V DC voltage through VDD pin (input of ASIC driver). When the tension at VCP pin (output of ASIC driver) begins to stabilize, the MEMS contacts are ready to be controlled. If the control signal at IN pin has high level corresponding to 3V DC voltage, MEMS contacts will be close. In opposition, if the control signal at IN pin has low level corresponding to 0V DC voltage, MEMS contacts will be opened. During the measurements for MEMS chip (Figure II-36(b)), the voltages at VDD, VCP, RFC pins are always constant. Therefore, the response time of ASIC driver is determined from a change of VDD voltage to the moment where the stabilization of VCP signal begins. The response time of MEMS chip is from a state change of the control voltage at IN pin to the moment where the stabilization of RF2 signal begins. As the ASIC driver and MEMS contacts of SPDT and SP4T switch package are identical. The measurements have been performed on a SPDT switch package.

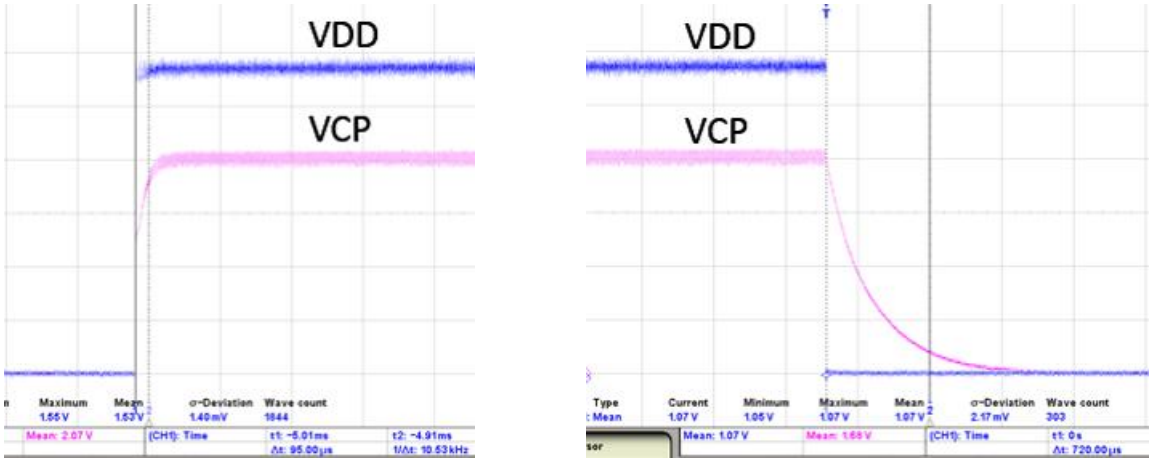


Figure II-37: Response time of ASIC driver

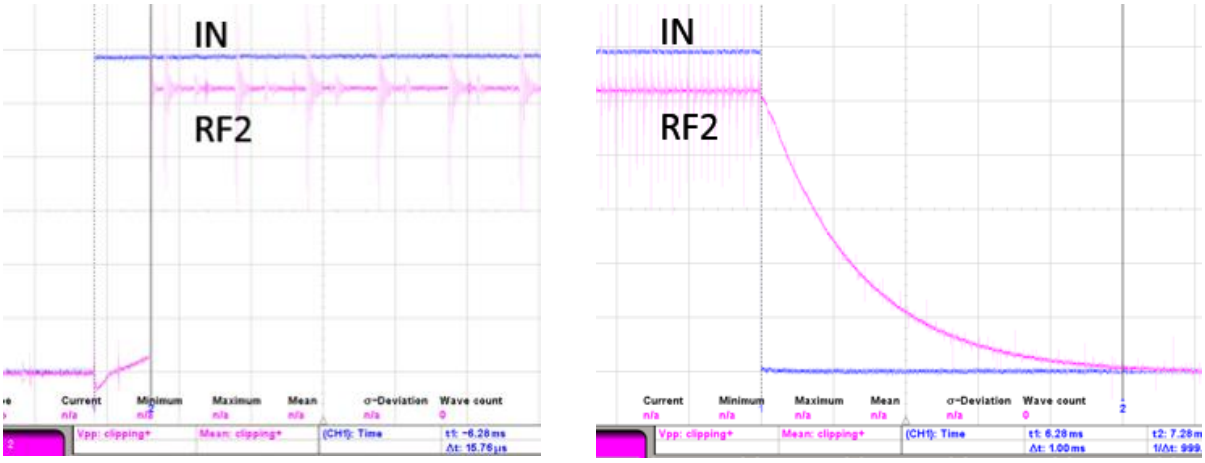


Figure II-38: Response time of MEMS chip

Figure II-37 and Figure II-38 show experimental results of the response time characterization. The ASIC driver has an on response time of 95µs, and an off response time of 720µs. The MEMS chip has an on response time of 16µs, and an off response time of 750µs. Due to electric discharge, the off response time is bigger than the on one.

II.4.4. Conclusion

The characterization results summarized in Table II-2 in the next page have not met the requirements as mentioned at the beginning of this section. Thus the MEMS switch package cannot be integrated in the agile filter demonstrator. Their designs are being improved by their provider. The MEMS contacts must be protected by a Si cap. In addition, the results show a big OFF response time of about 700 µs which is a main limitation of the MEMS technology presented in chapter I. This characterization met a common difficulty of SiP characterization which is that a poor-quality IP core will reduce the performance of a package, and make the package characterization longer. However, this analysis helps locating the important limitations of a package such as bonding wires, return-current path, and metal interconnections.

Table II-2: Characterization results of the MEMS switch package

		Characteristic	**SPDT switch package**	**SP4T switch package**
RF Performance	Step 1 DUT effected by PCB, molding, Si Cap, bond-wire	Bandwidth	8.8 GHz (RFC-RF1, RFC-RF2)	14.35 GHz (RFC-RF2, RFC-RF3) 10.7 GHz (RFC-RF1, RFC-RF4)
		Return Loss	Less than -5 dB from 0 to 10 GHz	Less than -5 dB from 0 to 15 GHz
		Off Isolation	Less than -15 dB from 0 to 10 GHz	Less than -20 dB from 0 to 13 GHz between RFC and RF4 -11 dB @ 13.87 GHz
	Step 2 Removal of Molding DUT effected by PCB, Si Cap, bond-wire	Bandwidth	9.3 GHz (RFC-RF1, RFC-RF2)	These measurements have not been done because the molding removal did not much effect the RF performance of SPDT switch package.
		Return Loss	Less than -5 dB from 0 to 10 GHz	
		Off Isolation	Less than -15 dB from 0 to 10 GHz	
	Step 3 Removal of Si Cap DUT effected by PCB, bond-wire	Bandwidth	10 GHz (RFC-RF1, RFC-RF2)	These measurements have not been done because the Si Cap removal made MEMS contacts very fragile, and did not much effect the RF performance of SPDT switch package.
		Return Loss	Less than -5 dB from 0 to 10 GHz	
		Off Isolation	Less than -15 dB from 0 to 10 GHz	
	Step 4 Removal of PCB, molding, Si Cap, bond-wire	Bandwidth	16 GHz (RFC-RF1, RFC-RF2)	17 GHz (RFC-RF2, RFC-RF3)
		Return Loss	Less than -5 dB from 0 to 20 GHz	
		Off Isolation	Less than -15 dB from 0 to 20 GHz	Less than -5 dB from 0 to 15 GHz between RFC and RF3
Response Time		On	95µs for ASIC driver 16µs for MEMS chip	
		Off	720µs for ASIC driver 750µs for MEMS chip	

II.5. Synthesis, conclusion and perspectives

In this chapter, we have studied some difficulties that happen when we need to measure an N-port. Two methods have been presented according to the available setup and the access lines properties. The first method using a four-port VNA addresses the problem of mixed mode measurement. It takes into account that the propagating modes have different propagation constants, which means that the measurement of a differential structure must not be related to the access lines but to the excited modes. The method has been used when no coupling appear between the access lines, or when the modes are purely TEM. When only a two-port VNA is available, we have presented a method which does not require the duplication of the DUT with several port terminations. This method has been verified on a branch-line coupler.

We have used the second method for characterizing three-port SPDT, and five-port SP4T switches. The switch packages are constituted by a MEMS chip that is molded into a plastic and connected to the environment by wires. The plastic molding has been removed to show that it only affects the parameters of phases. The characterization of the switches helps us pointing out difficulties in SiP characterization, and locating the main causes limiting the performance of a packaged devices.

The conducted analysis offers the basis for fair benchmarking of MEMS based switches in comparisons with SOI and BiCMOS solutions.

1. Intellectual Properties (IP) problem obstructs studying an IP core with all its information. For example, in this thesis, only measurement has been performed with several circuits provided by the manufacture. EM simulation cannot be done without substrate information. In addition, the characterization of an IP core in a research phase can be very long because it depends on the provider.
2. Connecting wires, particularly the mutual coupling (capacitive and inductive coupling) between them, play an important role in package performance at high frequency. In addition, return-path current flowing through a ground plane has also significant influence. Therefore, they will be characterized in chapter III. The mixed-mode TRL de-embedding method will be used for the measurements in chapter III.

Chapter III

INTERCONNECTION MODELING METHODOLOGY

III.1. Introduction

The interconnections between several parts of a circuit appear as limiting points in a design, mainly for high frequencies. Their effects can be reduced by optimization processes. This may need several hundreds of simulations before convergence. The interconnections can be very accurately described by electromagnetic simulations, each of them lasting several minutes. The total optimization time could reach several years. Thus, chapter III focuses on developing analytical model that can be computed within a few milliseconds. These models are based on lumped-element approach using analytical formulas. Measurement and EM simulation will be reference for evaluation.

The interconnections studied in this chapter have been chosen as the main limitations of a package mentioned in the conclusion of chapter II. Firstly, bonding wire is the most popular chip interconnection method because of its inherent low-cost, low coefficient of thermal expansion, more flexible fabrication, and very mature technology [53]. Secondly, crossing lines appears progressively in a package because the number of interconnect levels has substantially increased. In addition, ground plane as an indispensable part of all electronic circuits will be also characterized. In a package, passive components are not only interconnections, but also other types such as a comb-line filter integrated in the agile filter demonstrator of the PARSIMO project. Chapter III will present a model for it.

Chapter III is organized as follows. Paragraph III.2 presents a model for bonding wires. Then, paragraph III.3 describes a model for crossing lines. A simple approach to trace current path on a ground plane will be discussed in paragraph III.4. Paragraph III.5 introduces a model for comb-line filter. Finally, paragraph III.5 concludes chapter III.

III.2. Bonding-wire-geometric-profile-dependent model for two bonding wires

III.2.1. Introduction

Two basic models of a bonding wire are L-C-L model and C-L-C model. C-L-C model gives better insertion loss at high frequencies than L-C-L model does [56]. C-L-C models have been shown in some articles with good results [53]-[58] and are more representative of the reality. Because these models use the element values which are extracted from simulation or measurement, they lack analytical formulas as functions of geometrical dimensions of bonding wire structures. In [78], both Quasi-Static and Full-Wave solutions are used for modeling of Bond-Wire arrays accounting for their specific geometric profile. A physics-based broadband equivalent circuit extraction is proposed in [78] and [79] for an accurate modeling of bond-wire antennas.

The influence of profile on bonding wire EM characteristics (self and mutual inductances) is presented in [71]. Some articles calculated the self and mutual inductances of bonding wire by using the inductance formula of a straight wire [71]. This method is accurate if the curvature radius of bonding wire is large. Some articles have modeled the bonding wire profile by half a circle or by a Gaussian function [72], [73]. A good profile is necessary not only for EM characterization, but also for mechanical, thermal failure analysis, and fabrication. In order to reduce the time-to-market, a profile usable for different domains is required. Spline function is more flexible to capture bonding wire profile in comparison to the other profile functions [74]. They give a smoothest profile with a smallest stress energy which is a criterion to analyze mechanical failure. If it is greater than a maximal value corresponding to bond-wire material, bonding wire will be broken. Bonding wire profile based upon Spline functions have been used to analyze mechanical failures of bonding wire [61], [62], [74], but it has not been applied for electromagnetic modeling yet.

In order to calculate bonding wires' self and mutual inductances as functions of profile, the popular method is to divide bonding wire into many straight segments. This method is accurate if the number of straight segments is large enough. As a result, the inductance formulas become very complex if there are many bonding wires. A new approach to calculate the self and mutual inductances of bonding wires without dividing bonding wires into many straight segments will be presented. This method proposes to add a bonding-wire-geometric-profile-dependent term into the self-inductance formula of a straight wire. The target of this method is to be simply integrated in behavioral software avoiding a too long computation time. These inductance formulas will be used for a C-L-C model. To verify the model, a test bonding wires structure is fabricated on a glass substrate, which has many ideal properties for RF and microwave electronic packaging, including high strength, smooth surfaces for efficient signal distribution and excellent electrical characteristics [76].

This paragraph consists of four sections. The first section presents a model with extraction equations using *Y* parameters. The variation of extracted electrical values is also studied in this section. The second section develops analytical formulas using geometric dimensions to calculated

self-inductances, mutual-inductance, resistances and capacitances. The third section discusses on measurement setup, and the model evaluation. The final section concludes the model.

III.2.2. Modeling method

III.2.2.1. Extraction of the electrical model

We aim at investigating the mutual coupling between two bonding wires shown in Figure III-1. The two ends of each bonding wire are located on two different levels. A ground plane is placed under each level. The substrate is made of glass with relative permittivity ε_r of 4.6 and loss tangent tan (δ) of 4×10^{-3}. The material of these bonding wires is gold with conductivity σ of 4.1×10^{7} S.m^{-1}.

Figure III-1: Bonding wires' structure.

The model of each bonding wire consists of a resistance and an inductance in series. The mutual coupling between two bonding wires is modeled by a mutual inductance *M*.

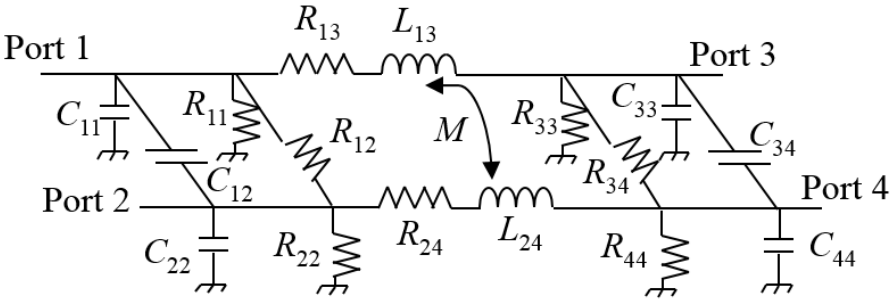


Figure III-2: Bonding wires' model.

The values of the elements in the above model (Figure III-2) are extracted from Y-parameters. The following equations have been determined by using the basic electronics theories (Kirchhoff's laws, Ohm's law…).

$$R_{13} + jL_{13}\omega = -\frac{1}{Y_{13} - \frac{Y_{23}Y_{14}}{Y_{24}}} \quad \text{(III-1)}$$

$$R_{24} + jL_{24}\omega = -\frac{1}{Y_{24} - \frac{Y_{23}Y_{14}}{Y_{13}}} \quad \text{(III-2)}$$

$$k = \text{mag}\left(\sqrt{\frac{Y_{23}Y_{14}}{Y_{13}Y_{24}}}\right) \quad \text{(III-3)}$$

$$M = k\sqrt{L_{13}L_{24}} \quad \text{(III-4)}$$

$$\frac{1}{R_{12}} + jC_{12}\omega = -Y_{12} - Y_{14} \quad \text{(III-5)}$$

$$\frac{1}{R_{34}} + jC_{34}\omega = -Y_{32} - Y_{34} \quad \text{(III-6)}$$

$$\frac{1}{R_{ii}} + jC_{ii}\omega = Y_{i1} + Y_{i2} + Y_{i3} + Y_{i4}, \quad i = 1, 2, 3, 4 \quad \text{(III-7)}$$

In this work, the losses in the glass material are negligible, so the bonding wires' model is simplified by considering the resistances R_{ii}, i = 1, 2, 3, 4 between the bonding pad and the ground plane, and the resistances R_{12}, R_{34} between two bonding pads as infinite.

III.2.2.2. Variations of self and mutual inductances

III.2.2.2.1. Effects of bonding wire dimensions

Figure III-3 shows the dependence of the extracted self and mutual inductances from the 3D EM simulation at 10 GHz on some dimensions such as distance d_{bws} and angle φ between two bonding wires, diameter d_{ia} and projected length D. These dimensions are described in detail in Figure III-3. During the variation of one dimension, the others remain their constant values shown in Figure III-3 and Table III-1.

Table III-1: Dimension variations in each case.

Case	Distance d_{bws}	Diameter d_{ia}	Projected length D	Angle φ
(a)	From 50 to 1000 µm	20 µm	840 µm	0°
(b)	500 µm	From 20 to 50 µm	840 µm	0°
(c)	500 µm	20 µm	From 400 to 840 µm	0°
(d)	Varied	20 µm	840 µm	From 0° to 180°

Increasing distance d_{bws} and angle φ does not influence extracted self-inductance, but decreases mutual inductance. Meanwhile, diameter of bonding wire affects only self-inductance. In addition, both self and mutual inductances are proportional to projected length D.

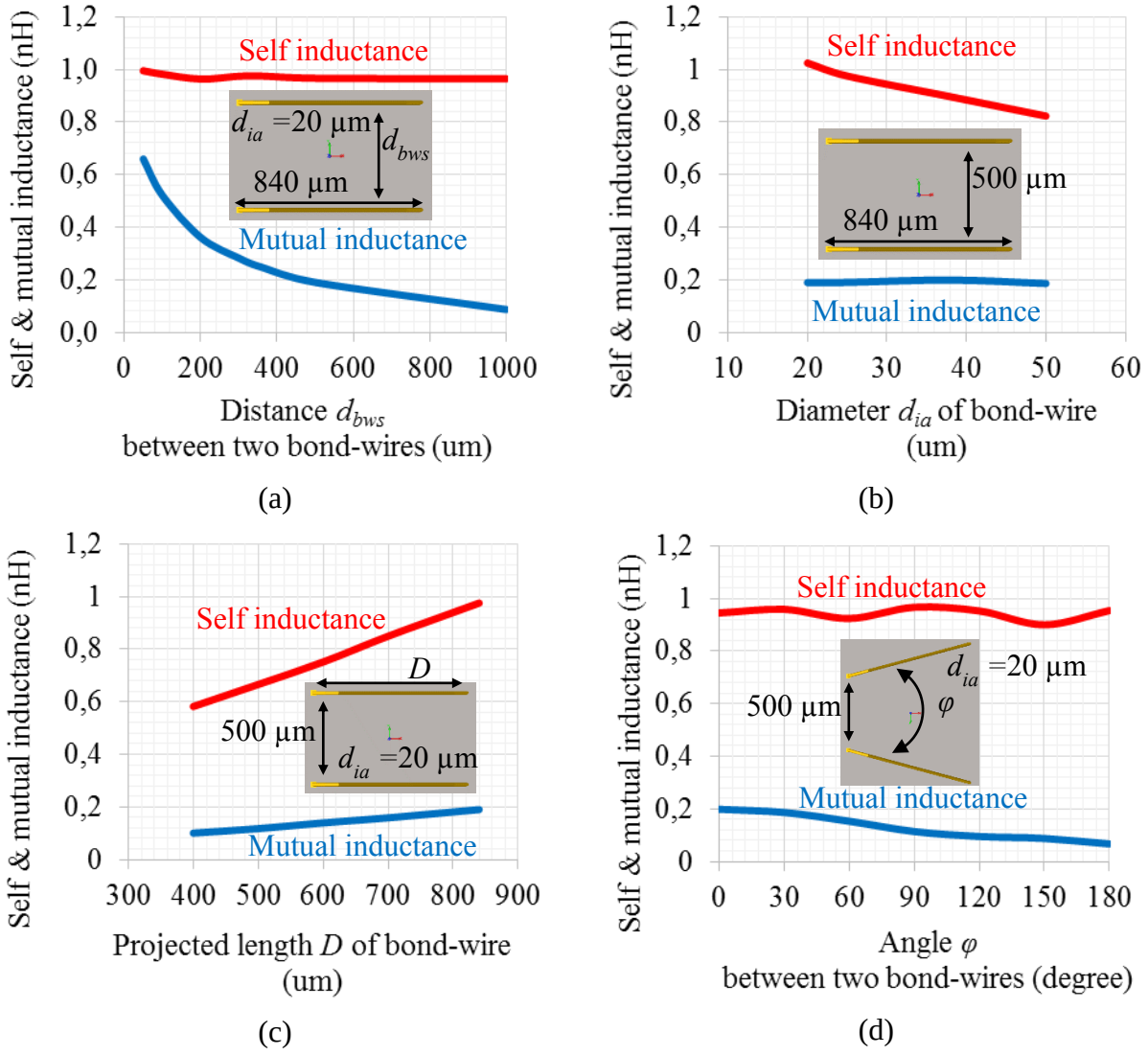


Figure III-3: Effects on extracted values of (a) distance between two bond-wires; (b) diameter of bond-wire; (c) projected length of bond-wire; (d) angle between two bond-wires.

III.2.2.2.2. Effects of Distributed Ground Plane

This section studies ground plane effects on the variations of extracted electrical values (self-inductance and resistance) from the 3D EM simulation. The combined effects of extracted self-inductance and resistance values are investigated through the calculation of the quality factor parameter defined as the ratio of ωL (pulsation times the self-inductance) by the series resistance R. Influence of ground plane on electrical characteristics (*Self-inductance, Quality-factor*) of bond-wire elements is studied in the perspective to derive analytical formulas (III-1) – (III-7) accounting for the proximity effects. From basic physical analysis, shortening the bond-wire length like making it closer to the ground plane reduces its inductance values.

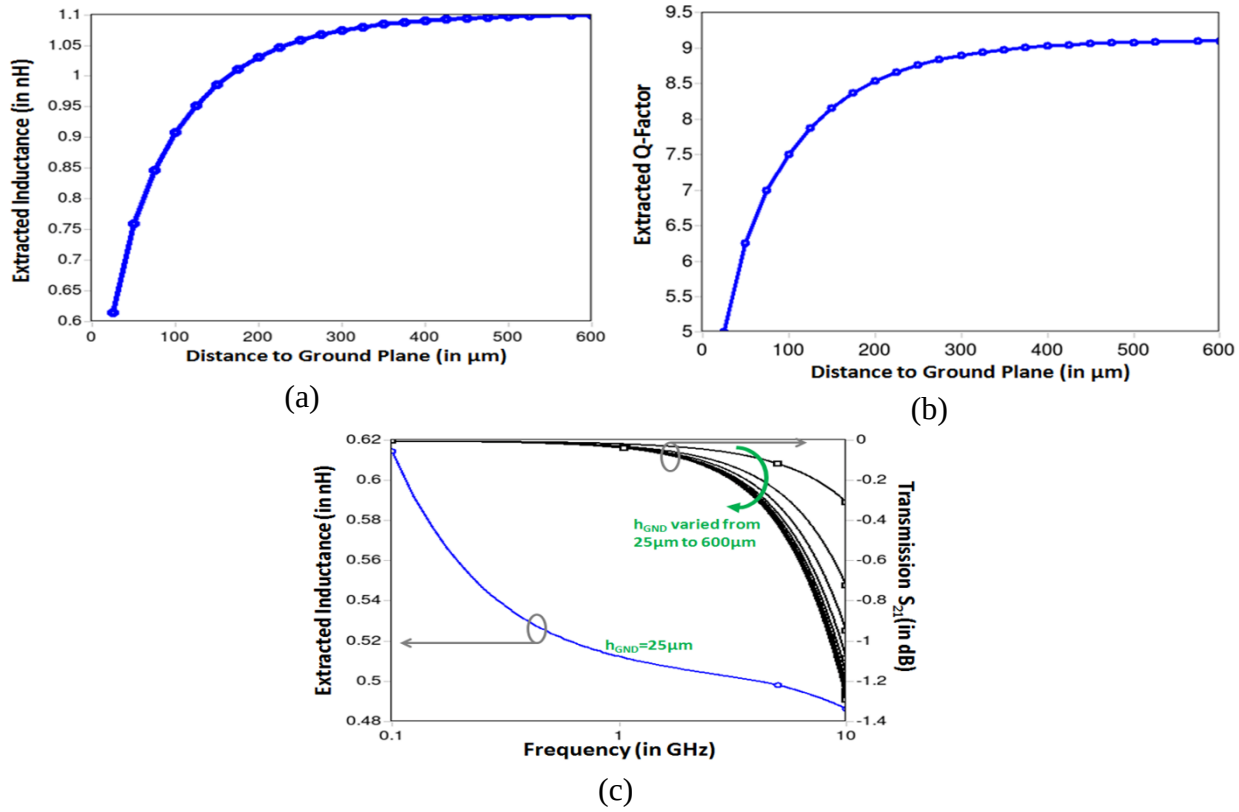


Figure III-4: Effects of distance to ground plane at 0.1GHz (a) on extracted Bond-Wire inductance; (b) on Quality-Factor; (c) Frequency dependent self-inductance and transmission parameter.

Figure III-4(a) and (b) present effects of distance to ground plane on extracted bond-wire inductance and Quality-Factor. The used 1.4mm long bond-wire element with 25µm diameter is treated as a two-port circuit assuming vertical excitations referenced to the ground plane. The distance (h_{GND}) of the bond-wire to the ground plane is parameterized as a design variable in the range from 25µm to 600µm. Varying the bond-wire distance to the ground plane from 25µm to 600µm increases the inductance value by about 40% of its nominal value.

The results in Figure III-4(a) and (b) exhibit saturation effects for distances to the ground plane greater than certain limit value which is dependent on the wire profile and electrical parameters. For the used electrical parameters this limit is found in the vicinity of 500µm. The extracted Quality factor leads to higher value for increased distance of the bond-wire to the ground reference in a proportion similar to the observed increase in the self-inductance variation. The extracted series resistance (accounting for crowding effects) of the bond-wire element, which is not reported for space constraint, decreases when the distance to the ground plane increases. So the increase in the bond-wire self-inductance combined to lower series resistance results in improved qualify-factor. Figure III-4(c) depicts the extracted self-inductance (presented for h_{GND}=25µm) and transmission parameters against frequency presented for h_{GND} increasing from 25µm to 600µm. The observed saturation effect is visible in the behavior of the transmission parameter as well.

III.2.3. Analytical formulas

III.2.3.1. Analytical description of the shape

Among different profiles standardized by organizations such as JEDEC, Spline profile is commonly used for RF connections [60]. To determine the Spline profile of a bonding wire, the following parameters need to be known (Figure III-5):

- The position of two end points and a point on the bonding wire: P_1 (x_{P1}, y_{P1}, z_{P1}), P_2 (x_{P2}, y_{P2}, z_{P2}), and P_3 (x_{P3}, y_{P3}, z_{P3}).
- The angle θ_i between the tangent line of the bonding wire at point i (i = 1, 2, 3) and the plane xy.
- The angle α between the bonding wire's plane and the plane xz.

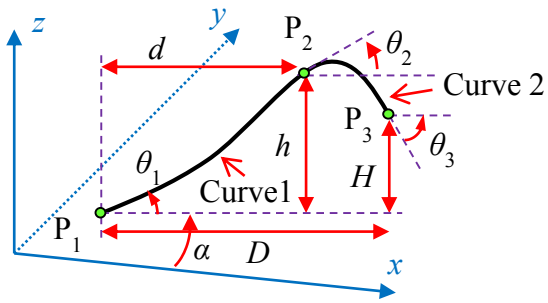


Figure III-5: Bonding wire's profile.

The positions of the two end points P_1 and P_3 are determined during the package design phase, whereas their angles (θ_1, θ_3) depend on wire bonding technology. They equal to 90° for ball bonding and 0° for wedge bonding. The point P_2 on the bonding wire should be chosen so that the strain energy of the bonding wire is minimal [61], [62]. As we only want to capture the profile of

an existing bonding wire, the point P_2 is chosen as the highest point of the bonding wire. Thus the profile functions (III-8) – (III-13) become simpler because $\theta_2 = 0$.

The bonding wire is divided into two curves (Figure III-5). The function describing each curve is determined by a third-order function passing through the two ends of the curve. Due to fabrication uncertainties, two terms e_{C1} and e_{C2} are added to the profile functions. They are manually varied around 1 to get the real bonding wire profile. For a profile in package design phase, e_{C1} and e_{C2} are equal to 1.

The profile functions of the curve 1 are

$$x_{C1}(u_c) = x_{P1} + d\left[u_c \frac{\cos\theta_1}{e_{C1}} + u_c^2\left(3 - \frac{2\cos\theta_1 + \cos\theta_2}{e_{C1}}\right) + u_c^3\left(\frac{\cos\theta_1 + \cos\theta_2}{e_{C1}} - 2\right)\right]\cos\alpha \quad \text{(III-8)}$$

$$y_{C1}(u_c) = y_{P1} + d\left[u_c \frac{\cos\theta_1}{e_{C1}} + u_c^2\left(3 - \frac{2\cos\theta_1 + \cos\theta_2}{e_{C1}}\right) + u_c^3\left(\frac{\cos\theta_1 + \cos\theta_2}{e_{C1}} - 2\right)\right]\sin\alpha \quad \text{(III-9)}$$

$$z_{C1}(u_c) = z_{P1} + d\left[u_c \frac{\sin\theta_1}{e_{C1}} + u_c^2\left(3\frac{h}{d} - \frac{2\sin\theta_1 + \sin\theta_2}{e_{C1}}\right) + u_c^3\left(\frac{\sin\theta_1 + \sin\theta_2}{e_{C1}} - 2\frac{h}{d}\right)\right] \quad \text{(III-10)}$$

The profile functions of the curve 2 are

$$x_{C2}(u_c) = x_{P2} + (D-d)\left[u_c \frac{\cos\theta_2}{e_{C2}} + u_c^2\left(3 - \frac{2\cos\theta_2 + \cos\theta_3}{e_{C2}}\right) + u_c^3\left(\frac{\cos\theta_2 + \cos\theta_3}{e_{C2}} - 2\right)\right]\cos\alpha \quad \text{(III-11)}$$

$$y_{C2}(u_c) = y_{P2} + (D-d)\left[u_c \frac{\cos\theta_2}{e_{C2}} + u_c^2\left(3 - \frac{2\cos\theta_2 + \cos\theta_3}{e_{C2}}\right) + u_c^3\left(\frac{\cos\theta_2 + \cos\theta_3}{e_{C2}} - 2\right)\right]\sin\alpha \quad \text{(III-12)}$$

$$z_{C2}(u_c) = z_{P2} + (D-d)\left[u_c \frac{\sin\theta_2}{e_{C2}} + u_c^2\left(3\frac{H-h}{D-d} - \frac{2\sin\theta_2 + \sin\theta_3}{e_{C2}}\right) + u_c^3\left(\frac{\sin\theta_2 + \sin\theta_3}{e_{C2}} - 2\frac{H-h}{D-d}\right)\right] \quad \text{(III-13)}$$

Where

- x_{Ci}, y_{Ci} and z_{Ci} are the coordinates of a point on curve i, i = 1, 2.
- u_c is a dimensionless variable, $0 \le u_c \le 1$. It corresponds to the position of the points on the curve between its ends.

The profile function of the whole bonding wire is a combination of the above functions (III-8) – (III-13).

$$x(u)=\begin{cases}x_{C1}(u) & 0\le u\le 1\\ x_{C2}(u-1) & 1<u\le 2\end{cases} \quad \text{(III-14)}$$

$$y(u)=\begin{cases}y_{C1}(u) & 0\le u\le 1\\ y_{C2}(u-1) & 1<u\le 2\end{cases} \quad \text{(III-15)}$$

$$z(u)=\begin{cases}z_{C1}(u) & 0\le u\le 1\\ z_{C2}(u-1) & 1<u\le 2\end{cases} \quad \text{(III-16)}$$

Where u is a dimensionless variable, $0 \le u \le 2$.

III.2.3.2. Self-inductance

The self-inductance of an open-loop circuit such as a bonding wire (BW) can be determined by the partial inductance theory [68]. When a bonding wire is approximated by N straight segments Δl_i, $1 \le i \le N$, the self-inductance $L|_{\text{BW}}$ of this bonding wire equals to

$$L\big|_{\text{BW}} = \sum_{i=1}^{N} L_i\big|_{\text{BW}} + 2\sum_{i=1}^{N}\sum_{j=i+1,\, j\le N}^{N} M_{ij}\big|_{\text{BW}} \quad \text{(III-17)}$$

Where:

- L_i is the self-inductance of the i^{th} segment Δl_i, $1 \le i \le N$.
- M_{ij} is the mutual inductance between the i^{th} and the j^{th} segments.

Figure III-6: Bond-wire and straightened bond-wire.

Because the partial inductance formula is undefined when the distance r_{ij} between two segments Δl_i and Δl_j is zero, the self-inductance of a bonding wire will be expressed through the one of a straight wire (SW). When the bonding wire is straightened, we have a straight wire of the same length and of the same diameter (Figure III-6). If the segments Δl_i are small enough, the self-inductance $L|_{\text{SW}}$ of this straightened bonding wire becomes

$$L\big|_{\text{SW}} = \sum_{i=1}^{N} L_i\big|_{\text{SW}} + 2\sum_{i=1}^{N}\sum_{j=i+1,\, j\le N}^{N} M_{ij}\big|_{\text{SW}} \quad \text{(III-18)}$$

Because $\Delta l_i|_{SW}=\Delta l_i|_{BW}$,

$$\sum_{i=1}^{N} L_i\big|_{SW} = \sum_{i=1}^{N} L_i\big|_{BW} \tag{III-19}$$

By subtracting Eq. (III-18) from Eq. (III-17), we have

$$L\big|_{BW} = L\big|_{SW} + \Delta L \tag{III-20}$$

Where:

$$\Delta L = 2\sum_{i=1}^{N}\sum_{j=i+1,\, j\le N}^{N}\left(M_{ij}\big|_{BW} - M_{ij}\big|_{SW}\right) \tag{III-21}$$

The geometric-profile-dependent term ΔL represents the difference between the self-inductance of a bonding wire and the one of a straight wire. The self-inductance of a straight wire is well known [59], [66]:

$$L\big|_{SW} = \frac{\mu l}{2\pi}\left[\ln\left(\frac{2l}{d_{ia}} + \sqrt{1+\left(\frac{2l}{d_{ia}}\right)^2}\right) + \frac{d_{ia}}{2l} - \sqrt{1+\left(\frac{d_{ia}}{2l}\right)^2} + \frac{Q}{4}\right] \tag{III-22}$$

Where:

$$Q = Q_{da}(1-t) \tag{III-23}$$

$$t = -\frac{0.198584}{\left[1+0.25741\left(\gamma^{1.2652}-\gamma^{-0.39709}\right)^2\right]^{2.62343}} \tag{III-24}$$

$$\gamma = 0.38691q\,,\ q = \frac{d_{ia}}{\delta\sqrt{2}}\,,\ \delta = \frac{1}{\sqrt{\pi\sigma\mu f}} \tag{III-25}$$

$$Q_{da} = Q_{\infty}\sqrt[1.5819]{1-\exp\left\{-\left(\frac{1}{Q_{\infty}}\right)^{1.5819}\right\}} \tag{III-26}$$

$$Q_{\infty} = \frac{4}{q\sqrt{2}}\left(1+\frac{0.01209}{q+1}-\frac{0.63523}{q^2+1}+\frac{0.16476}{q^3+1}\right) \tag{III-27}$$

Where:

- l is the length of bonding wire.
- d_{ia} is the diameter of bonding wire.

Next we determine the geometric-profile-dependent term ΔL. The mutual inductance M_{ij} between the i^{th} and j^{th} segments is approximated by the following function presented in [65].

$$M_{ij} \approx M_{0ij} + g(\text{cross section}) \tag{III-28}$$

Where:

- M_{0ij} is the mutual inductance between the central filaments of the i^{th} and j^{th} segments.
- g is a function of the cross section of the wire.

The function g is assumed to be identical for both the bonding wire and the straight wire because they have the same cross section.

$$M_{ij}\Big|_{\text{BW}} - M_{ij}\Big|_{\text{SW}} \approx M_{0ij}\Big|_{\text{BW}} - M_{0ij}\Big|_{\text{SW}} \tag{III-29}$$

We have:

$$M_{0ij}\Big|_{\text{BW}} = \frac{\mu}{4\pi}\frac{\overrightarrow{\Delta l_i}.\overrightarrow{\Delta l_j}}{r_{ij}},\ M_{0ij}\Big|_{\text{SW}} = \frac{\mu}{4\pi}\frac{\Delta l_i.\Delta l_j}{l_{ij}} \tag{III-30}$$

Where:

- r_{ij} is the distance from Δl_i to Δl_j.
- l_{ij} is the arc length from Δl_i to Δl_j.

From Eq. (III-21), (III-29) and (III-30), we have

$$\Delta L = \frac{\mu}{2\pi}\sum_{i=1}^{N}\sum_{j=i+1,\, j\le N}^{N}\left(\frac{\overrightarrow{\Delta l_i}.\overrightarrow{\Delta l_j}}{r_{ij}} - \frac{\Delta l_i.\Delta l_j}{l_{ij}}\right) \tag{III-31}$$

When $N \to \infty$,

$$\Delta L = \frac{\mu}{2\pi}\int_0^2\int_{u_i}^2 f^{\Delta L}(u_i,u_j)\,du_j\,du_i. \tag{III-32}$$

Where:

$$f^{\Delta L}(u_i,u_j) = \frac{\dot{x}(u_i)\dot{x}(u_j)+\dot{y}(u_i)\dot{y}(u_j)+\dot{z}(u_i)\dot{z}(u_j)}{\sqrt{\left[x(u_i)-x(u_j)\right]^2+\left[y(u_i)-y(u_j)\right]^2+\left[z(u_i)-z(u_j)\right]^2}} - \frac{\sqrt{\left[\dot{x}(u_i)^2+\dot{y}(u_i)^2+\dot{z}(u_i)^2\right]\left[\dot{x}(u_j)^2+\dot{y}(u_j)^2+\dot{z}(u_j)^2\right]}}{\int_{u_i}^{u_j}\sqrt{\dot{x}^2+\dot{y}^2+\dot{z}^2}\,du} \tag{III-33}$$

Where $x(u_i)$, $y(u_i)$ and $z(u_i)$ are the functions defined in Eq. (III-14) - (III-16). The upper point corresponds to the derivative.

Although the integration (III-32) cannot be solved in closed-form, we can find a closed-form approximation by using bi-cubic interpolation technique [63], [64]. The idea is to replace a complicated function $f(u_i,u_j)$ by a polynomial function $p(u_i,u_j)$ which is determined by the values and the partial derivatives of $f(u_i,u_j)$ at four points. In order to simplify calculations, these four

points should be chosen so that the second partial derivatives $\partial^2 f/\partial u_i \partial u_j$ can be eliminated. The final formula for ΔL is

$$\Delta L = \frac{\mu}{2\pi}\sum_{k=1}^{3}\mathbf{K_k}.\mathbf{F_k^{\Delta L}} \tag{III-34}$$

Where:

$$\mathbf{K_1} = \mathbf{K_3} = \left[\frac{7}{64}\ \frac{25}{128}\ \frac{25}{128}\ \frac{1}{96}\ \frac{-5}{192}\ \frac{5}{192}\ \frac{-1}{96}\ \frac{-5}{192}\ \frac{5}{192}\right] \tag{III-35}$$

$$\mathbf{K_2} = \left[\frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}\ \frac{1}{360}\ \frac{-1}{360}\ \frac{1}{360}\ \frac{-1}{360}\ \frac{1}{360}\ \frac{1}{360}\ \frac{-1}{360}\ \frac{-1}{360}\right] \tag{III-36}$$

$$\begin{aligned}\mathbf{F}_{\mathbf{19\times1}}^{\mathbf{\Delta L}} = \Big[& f^{\Delta L}(0,1) \quad f^{\Delta L}(0.8,1) \quad f^{\Delta L}(0,0.2) \\ & \frac{\partial f^{\Delta L}}{\partial u_i}(0,1) \quad \frac{\partial f^{\Delta L}}{\partial u_i}(0.8,1) \quad \frac{\partial f^{\Delta L}}{\partial u_i}(0,0.2) \\ & \frac{\partial f^{\Delta L}}{\partial u_j}(0,1) \quad \frac{\partial f^{\Delta L}}{\partial u_j}(0.8,1) \quad \frac{\partial f^{\Delta L}}{\partial u_j}(0,0.2)\Big]^{\mathrm{T}}\end{aligned} \tag{III-37}$$

$$\begin{aligned}\mathbf{F}_{\mathbf{212\times1}}^{\mathbf{\Delta L}} = \Big[& f^{\Delta L}(0.2,1.2) \quad f^{\Delta L}(0.8,1.2) \quad f^{\Delta L}(0.2,1.8) \quad f^{\Delta L}(0.8,1.8) \\ & \frac{\partial f^{\Delta L}}{\partial u_i}(0.2,1.2) \quad \frac{\partial f^{\Delta L}}{\partial u_i}(0.8,1.2) \quad \frac{\partial f^{\Delta L}}{\partial u_i}(0.2,1.8) \quad \frac{\partial f^{\Delta L}}{\partial u_i}(0.8,1.8) \\ & \frac{\partial f^{\Delta L}}{\partial u_j}(0.2,1.2) \quad \frac{\partial f^{\Delta L}}{\partial u_j}(0.8,1.2) \quad \frac{\partial f^{\Delta L}}{\partial u_j}(0.2,1.8) \quad \frac{\partial f^{\Delta L}}{\partial u_j}(0.8,1.8)\Big]^{\mathrm{T}}\end{aligned} \tag{III-38}$$

$$\begin{aligned}\mathbf{F}_{\mathbf{39\times1}}^{\mathbf{\Delta L}} = \Big[& f^{\Delta L}(1,2) \quad f^{\Delta L}(1.8,2) \quad f^{\Delta L}(1,1.2) \\ & \frac{\partial f^{\Delta L}}{\partial u_i}(1,2) \quad \frac{\partial f^{\Delta L}}{\partial u_i}(1.8,2) \quad \frac{\partial f^{\Delta L}}{\partial u_i}(1,1.2) \\ & \frac{\partial f^{\Delta L}}{\partial u_j}(1,2) \quad \frac{\partial f^{\Delta L}}{\partial u_j}(1.8,2) \quad \frac{\partial f^{\Delta L}}{\partial u_j}(1,1.2)\Big]^{\mathrm{T}}\end{aligned} \tag{III-39}$$

The matrices $\mathbf{K_k}$ depend only on the boundaries of the integration (III-32) and on the chosen points (u_i, u_j). Therefore they are applicable for different functions $f(u_i, u_j)$. Determining the geometric-profile-dependent term ΔL with some points (u_i, u_j) will decrease calculation time.

III.2.3.3. Mutual inductance

In this section, we calculate the mutual inductance between two bonding wires. The profile function of bonding wire 1 is $x_1(u), y_1(u), z_1(u)$ and of bonding wire 2 is $x_2(u), y_2(u), z_2(u)$. Because the distance between these two bonding wires is much larger than their diameter, the mutual inductance between them is approximated by the following formula [65]:

$$M_{12} = \frac{\mu}{4\pi}\int_{BW_1}\int_{BW_2}\frac{\overrightarrow{dl_i}.\overrightarrow{dl_j}}{r_{ij}} = \frac{\mu}{2\pi}\int_0^2\int_{u_i}^2 f^{M_{12}}(u_i,u_j)du_j du_i \qquad \text{(III-40)}$$

Where:

$$f^{M_{12}}(u_i,u_j) = \frac{\dot{x}_1(u_i)\dot{x}_2(u_j)+\dot{y}_1(u_i)\dot{y}_2(u_j)+\dot{z}_1(u_i)\dot{z}_2(u_j)}{\sqrt{\left[x_1(u_i)-x_2(u_j)\right]^2+\left[y_1(u_i)-y_2(u_j)\right]^2+\left[z_1(u_i)-z_2(u_j)\right]^2}}$$

M_{12} is an integration of a two-variable (u_i, u_j) function.

$$M_{12} = \frac{\mu}{2\pi}\sum_{k=1}^{3}\mathbf{K_k}.\mathbf{F_k^{M_{12}}} \qquad \text{(III-41)}$$

The matrices $\mathbf{K_k}$ are determined by Eq. (III-35) and (III-36). The matrices $\mathbf{F_k^{M_{12}}}$ are determined by Eq. (III-37), (III-38), and (III-39) under the condition that the function $f^{\Delta L}(u_i,u_j)$ is replaced by the function $f^{M_{12}}(u_i,u_j)$.

III.2.3.4. Resistance

Because the resistance of a bonding wire is independent of the bonding wire profile, we will use the resistance formula of a straight wire. The accuracy of the following formula is within ± 0.09% [66].

$$R_{ac} = \frac{l}{\sigma\pi\left(2r\delta'-\delta'^2\right)(1+t)} \qquad \text{(III-42)}$$

Where:

$$\delta' = \delta\left[1-\exp\left(-\frac{r}{\delta}\right)\right],\ \delta = \frac{1}{\sqrt{\pi\sigma\mu f}},\ \gamma = \frac{0.62006r}{\delta} \qquad \text{(III-43)}$$

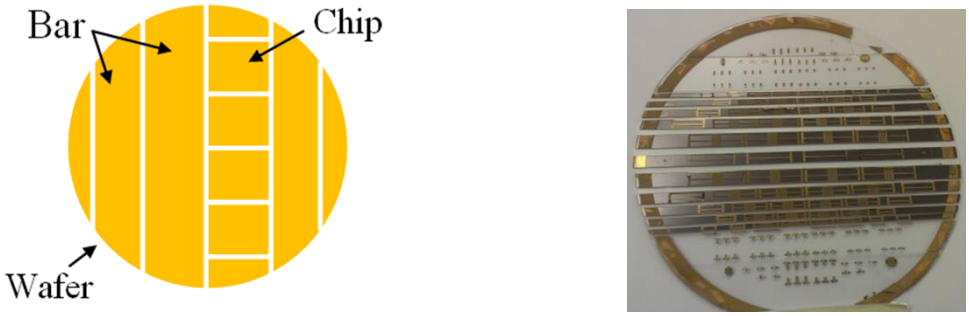
$$t = \frac{0.189774}{\left[1+0.272481\left(\gamma^{1.82938}-\gamma^{-0.99457}\right)^2\right]^{1.0941}} \qquad \text{(III-44)}$$

III.2.3.5. Capacitance

The capacitances in this work are between a bond pad and a ground plane and between two bond pads. They are calculated from the formulas in [75].

III.2.4. Experiment and discussion

III.2.4.1. Fabrication



(a) (b)

Figure III-7: Glass wafer in fabrication. (a) Wafer, bar and chip definition. (b) A glass wafer diced into bars

To evaluate the RF losses, the interconnection structure was designed on a glass wafer. The fabrication process consists of a metallization of the wafer which is followed by an etching to define the RF lines and the ground planes. Next the wafer was diced in only one way to obtain bars (Figure III-7). In order to connect the ground plane on top side and the one on back side, the lateral side was metalized by a sputtering on the back side of those bars. Then these bars were diced to obtain chips to be assembled. In the assembly phase, a pick and place equipment was used to align the contacts of the chips. The chips were soldered by using silver glue. To connect the 3D stack, gold bonding wires with a diameter of 25 µm were used. The type of bonding is a ball-wedge connection that permits to obtain a loop after the first connection.

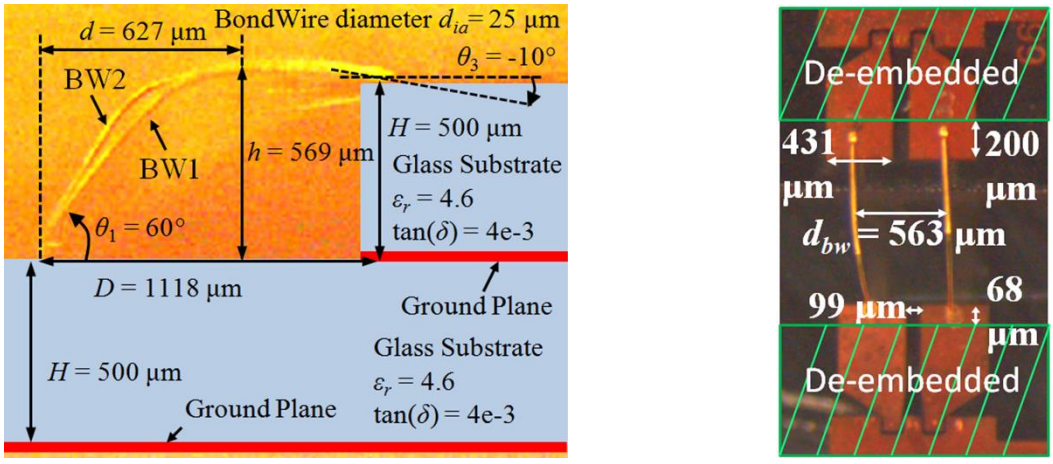


Figure III-8: Bonding wires' dimensions

Figure III-8 shows the bonding wire structure with its dimensions. The de-embedded parts have been removed by the calibration TRL technique. Because of fabrication uncertainties, the profiles of two bonding wires are different. We vary e_{C1} and e_{C2} around 1 until the profile created by the functions (III-8)-(III-16) is identical to the bonding wire's real profile. For the bonding wire 1, both e_{C1} and e_{C2} values are unity which means that the bonding wire 1 has its designed profile. In contrast, the bonding wire 2 is deformed. The chosen values are 0.6 for e_{C1} and 1 for e_{C2}.

The bonding wire profiles are well captured by the following functions (Figure III-9.b). For the bonding wire 1:

$$x_1(u)=\begin{cases}313.5u+627u^2-313.5u^3 & 0\le u\le 1\\ 627+491(u-1)+7.5(u-1)^2-9.5(u-1)^3 & 1<u\le 2\end{cases} \quad \text{(III-45)}$$

$$y_1(u)=0 \quad \text{(III-46)}$$

$$z_1(u)=\begin{cases}543u+621u^2-595u^3 & 0\le u\le 1\\ 569-112.7(u-1)^2+46.7(u-1)^3 & 1<u\le 2\end{cases} \quad \text{(III-47)}$$

Where $x_1(u)$, $y_1(u)$, and $z_1(u)$ are expressed in μm.

For the bonding wire 2:

$$x_2(u)=\begin{cases}522.5u-209u^2+313.5u^3 & 0\le u\le 1\\ 627+491(u-1)+7.5(u-1)^2-9.5(u-1)^3 & 1<u\le 2\end{cases} \quad \text{(III-48)}$$

$$y_2(u)=563 \quad \text{(III-49)}$$

$$z_2(u)=\begin{cases}905u-103u^2-233u^3 & 0\le u\le 1\\ 569-112.7(u-1)^2+46.7(u-1)^3 & 1<u\le 2\end{cases} \quad \text{(III-50)}$$

Where $x_2(u)$, $y_2(u)$, and $z_2(u)$ are expressed in μm.

III.2.4.2. Simulation and measurement setup

Electromagnetic simulations and measurements have been used to verify the accuracy and the calculation time of the model. We used two simulators, Keysight's EMPro 3D full-wave simulator based on the FEM method and Keysight's Momentum 2.5D simulator based on the method of moments. Because the simulators cannot simulate a smooth profile due to meshing problem, the bonding wires have been approximated by a JEDEC 9-point profile (Figure III-9.c and d). A structure with an infinite ground plane was built in Momentum (Figure III-9.c). However, EMPro cannot simulate an infinite ground plane. Therefore only bonding wire without ground plane has

been built in EMPro (Figure III-9(d)). The positive and negative poles of port 1 in Figure III-9(d) have been put at two ends of the bonding wire.

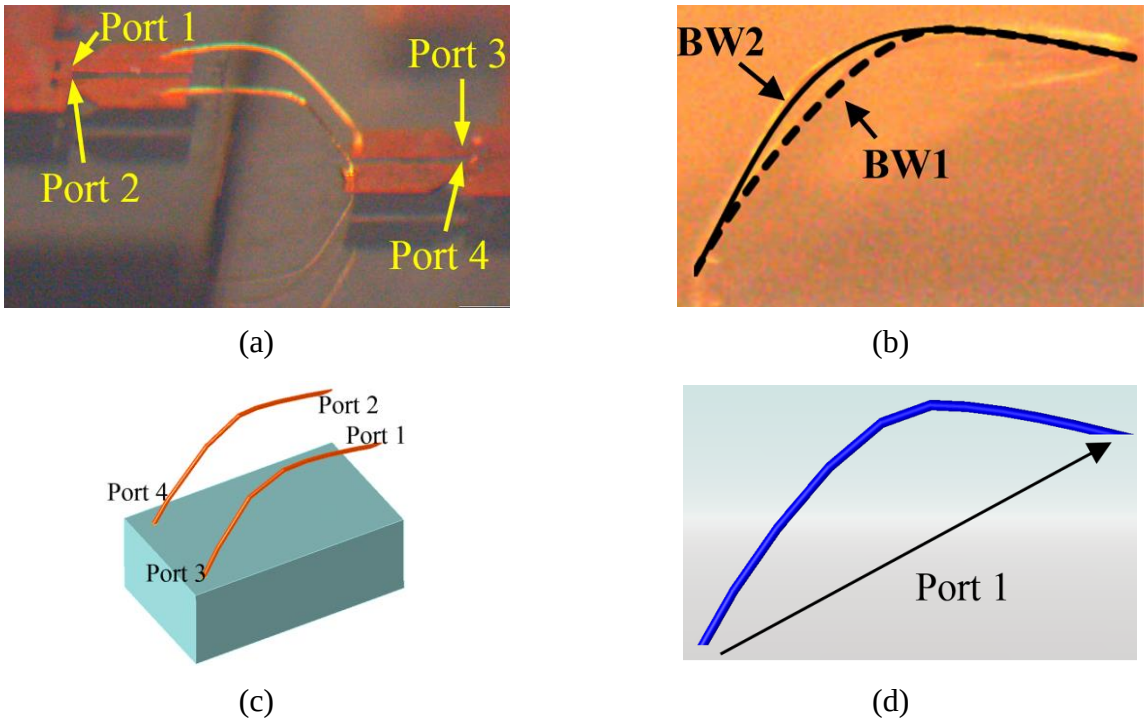


Figure III-9: Bonding wire's profile (a) fabricated, (b) created by profile functions, (c) in Momentum EM simulator, (d) in EMPro EM simulator.

The measurements have been performed by a 4-port VNA with G-S-G-S-G RF probes of 125 µm pitch. An SOLT calibration has been performed on a separate cal-kit from 1 to 8 GHz. The access transmission lines were de-embedded from the measurement results by the TRL technique presented in paragraph II.2. The measured bonding wire part after de-embedding is shown in Figure III-8.

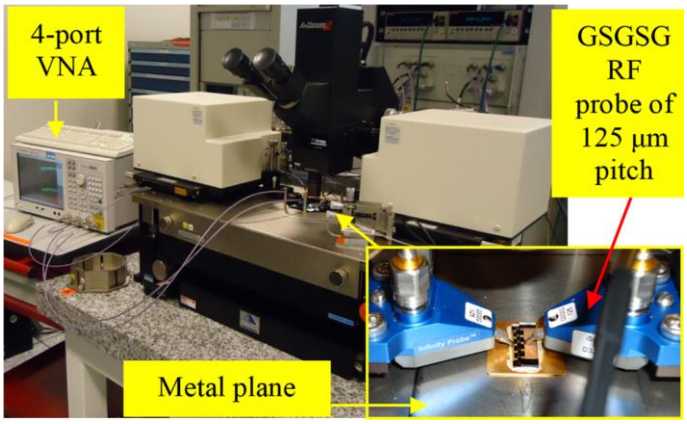


Figure III-10: Measurement setup

During the measurements, the bonding wires were put above a large metal plane which has been considered infinite (Figure III-10). Because the self-inductance of an infinite ground plane equals to zero [70], the mutual inductances between the bonding wires and the ground plane are negligible. Therefore, the self and mutual inductances in Figure III-2 are calculated by the formulas in section III.2.3.

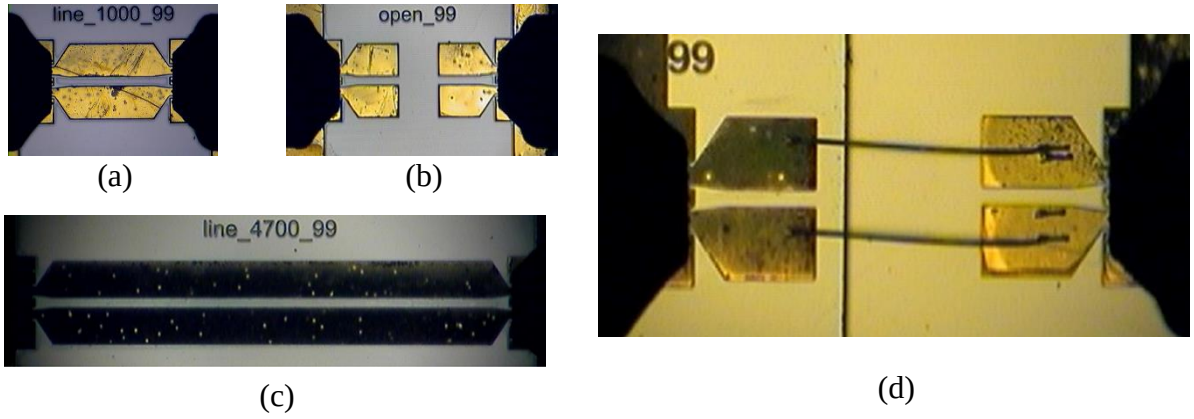


Figure III-11: Bonding wires and TRL patterns in measurement. (a) Thru. (b) Open. (c) Line. (d) Bonding wires on glass substrate

III.2.4.3. Comparisons

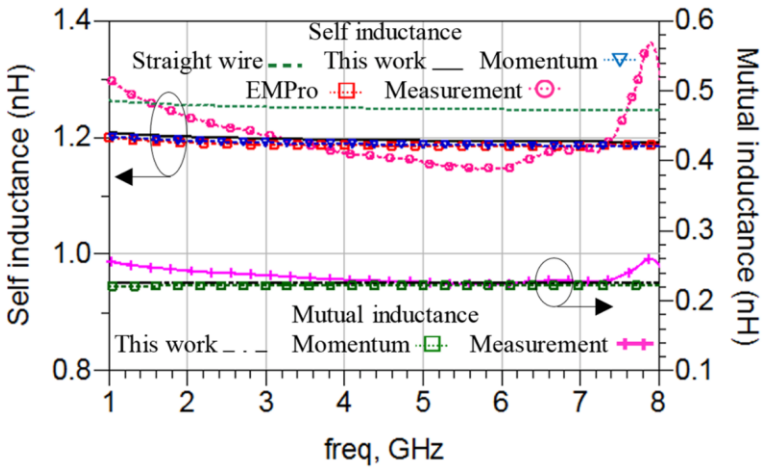


Figure III-12: Inductances of measurement, simulation and calculation

Figure III-12 shows the inductance values obtained from analytical calculation, numerical simulation and measurement. The bonding wire calculated inductances are in a good agreement with the simulations. The profile effect is visible in the difference between the self-inductance of a

straight wire and the one of a bonding wire. In other words, curvature decreases the self-inductance of a wire. When the bonding-wires are at a distance of 500 µm from the ground plane, the extracted inductances are nearly not influenced by the proximity effects. The measured inductances are close to the calculated values within a reasonable deviation. Observed differences can be attributed to skin effect for lower frequencies and/or parasitic resonance between the probes for higher frequencies. Additional correlation analysis for capacitances and resistances have been presented in Table III-2 reporting acceptable agreement between analytical calculation and extracted results from measurement.

Table III-2: The extracted and calculated values

	EXTRACTED AT 4 GHZ	CALCULATED
L_{13}	1.175 nH	1.196 nH @4 GHz
L_{24}	1.218 nH	1.211 nH @4 GHz
R_{13}	0.37 Ω	0.35 Ω @4 GHz
R_{24}	0.37 Ω	0.35 Ω @4 GHz
M	0.230 nH	0.225 nH
C_{11}	18.19 fF	16.15 fF
C_{22}	18.30 fF	16.15 fF
C_{33}	6.91 fF	5.49 fF
C_{44}	4.26 fF	5.49 fF
C_{12}	11.69 fF	10.97 fF
C_{34}	3.543 fF	3.73 fF

The model in this work has been built in Keysight's ADS software. A Matlab script is used to calculate the geometric-profile-dependent term ΔL and the mutual inductance M. The capacitances and mutual inductances refer to the calculated values shown in Table III-2 for all frequencies. The self-inductance and the resistance are calculated for each frequency by ADS. This model has a total calculation time of about 0.5 seconds. The electromagnetic simulations are much longer, 21 seconds for a simulation in Momentum and 6 minutes and 34 seconds for a simulation in EMPro. The EM simulation time is proportional to the segment number of bonding wire.

The S parameters of the model have been compared to the measurement in Figure III-13. For the most significant parameters S_{11} and S_{31}, we find the differences at high frequency due to parasitic resonance between the RF probes. The other parameters are in good agreement as far as the parasitic resonance does not appear for higher frequencies. Their differences are negligible because they are very weak signals.

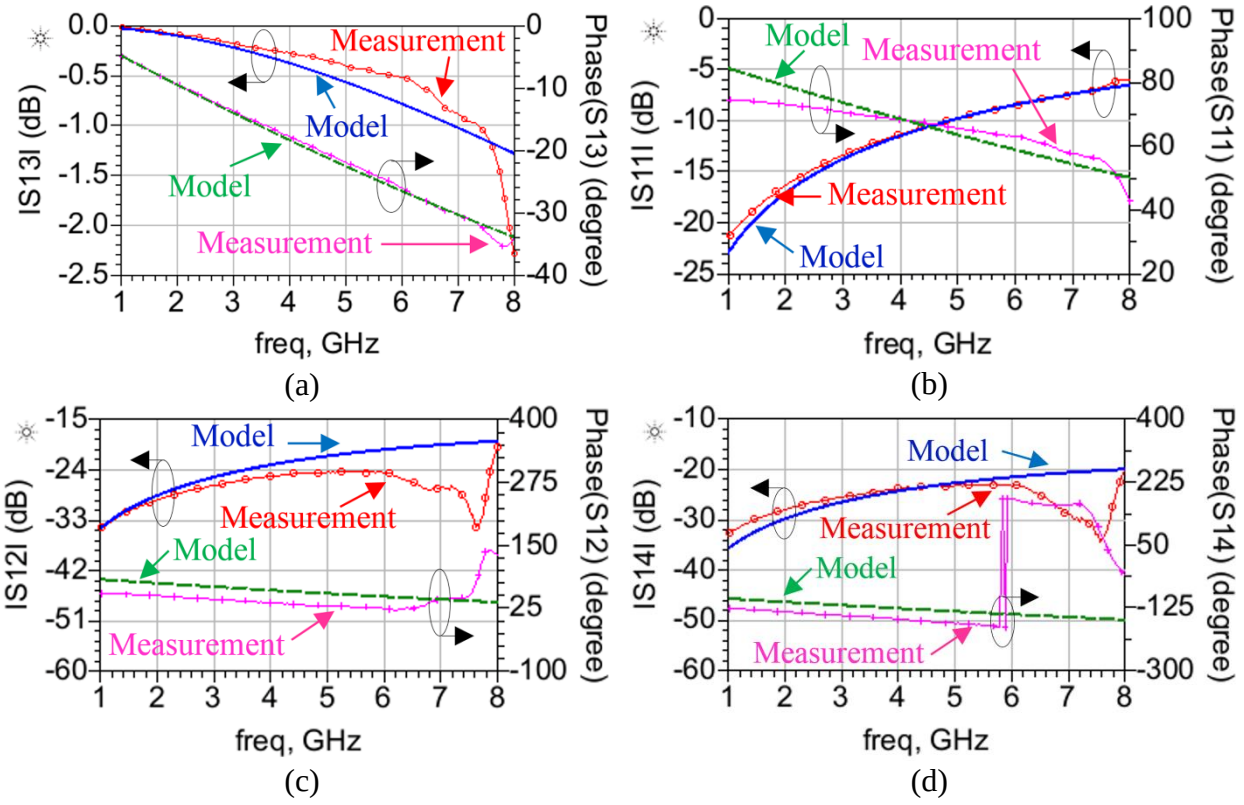


Figure III-13: Comparison between model and measurement

III.2.5. Conclusion

The model in this work has demonstrated its small calculation time and its accuracy in comparison with electromagnetic simulation and measurement. The geometric profile has significant effects on the extracted self-inductance of a bonding wire. The distance from bonding wire to a large ground plane influences also extracted inductance and resistance values if it is small enough. This modeling method can be extended to structures including several bonding wires.

III.3. Analytical modeling for Crossing line

III.3.1. Introduction

Two types of electromagnetic coupling are inductive coupling and capacitive coupling. Putting orthogonally two interconnections eliminates effectively the inductive coupling between them. None less there is no method to remove totally the capacitive coupling. However, it can be reduced by optimization. The capacitive coupling has been studied in many articles [91] - [96]. Some techniques to reduce capacitive coupling proposed in [92] are:

- The two interconnections must be far to each another
- The length of the parallel interconnections must be small
- The height of the interconnections with respect to a ground plane must be small
- The potentials difference of the two interconnections must be small
- The operating frequency must be small
- The input impedance of the victim interconnection must be low
- The insulation of between two interconnections must have a small relative permittivity ε_r

This paragraph focuses on studying the capacitive coupling between two orthogonal crossing lines. Firstly, a model for the capacitive coupling is presented. Then analytical formulas are developed to express the relation between the capacitances and the geometric dimensions. The model is evaluated in comparison with EM simulation. Finally, the paragraph is closed by some conclusions.

III.3.2. Modeling

The structure to be modeled is the crossover area of two orthogonal crossing lines shown in Figure III-14. The substrate separating the lines has been made from glass material which has relative permittivity ε_r of 4.6, and loss tangent tan(δ) of 4×10^{-3}. The frequency band is from 0 to 20 GHz.

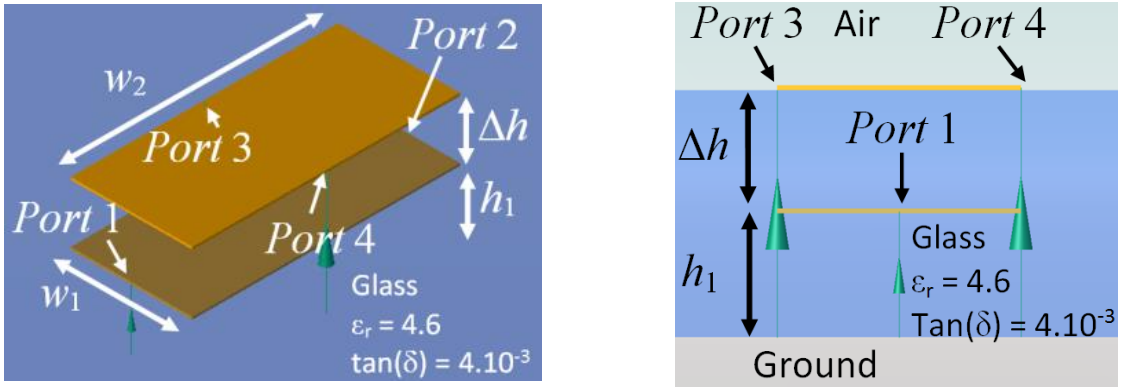
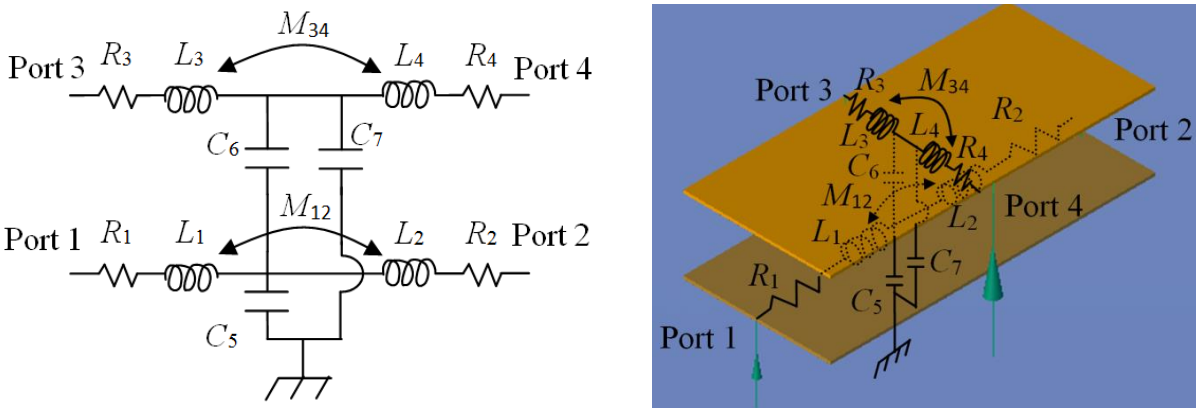


Figure III-14: Crossing lines designed in EMPro simulator.

The proposed model for this structure is in Figure III-15. The capacitance coupling is modeled by capacitors. A line is represented by resistances and self-inductances in series. Getting a large-band model requires mutual inductances between self-inductances on the same line because inductive coupling becomes significant at high frequencies. There is no inductive coupling between two lines as far as they are orthogonal.



(a) (b)

Figure III-15: Crossing lines model

The value of the model elements is extracted from *Z* parameters using Eq. (III-51) - (III-59). In this work, *Z* parameters have been obtained from EM simulation.

$$R_i = \text{real}\left(Z_{ii} - Z_{12}\right) \qquad i = 1, 2 \tag{III-51}$$

$$L_i = \frac{\text{imag}\left(Z_{ii} - Z_{12}\right)}{2\pi f} \qquad i = 1, 2 \tag{III-52}$$

$$R_i = \text{real}\left(Z_{ii} - Z_{34}\right) \qquad i = 3, 4 \tag{III-53}$$

$$L_i = \frac{\text{imag}\left(Z_{ii} - Z_{34}\right)}{2\pi f} \qquad i = 3, 4 \tag{III-54}$$

$$C_6 = \frac{\text{imag}\left[\dfrac{1}{Z_{13}\left(k_5 k_7 - 1\right)}\right]}{2\pi f} \tag{III-55}$$

$$C_5 = \frac{\text{imag}\left[\dfrac{k_5 - 1}{Z_{13}(k_5 k_7 - 1)}\right]}{2\pi f} \tag{III-56}$$

$$C_7 = \frac{\text{imag}\left[\dfrac{k_7 - 1}{Z_{13}(k_5 k_7 - 1)}\right]}{2\pi f} \tag{III-57}$$

Where

$$k_5 = Z_{34}/Z_{13} \tag{III-58}$$

$$k_7 = Z_{12}/Z_{13} \tag{III-59}$$

III.3.3. Analytical formulas

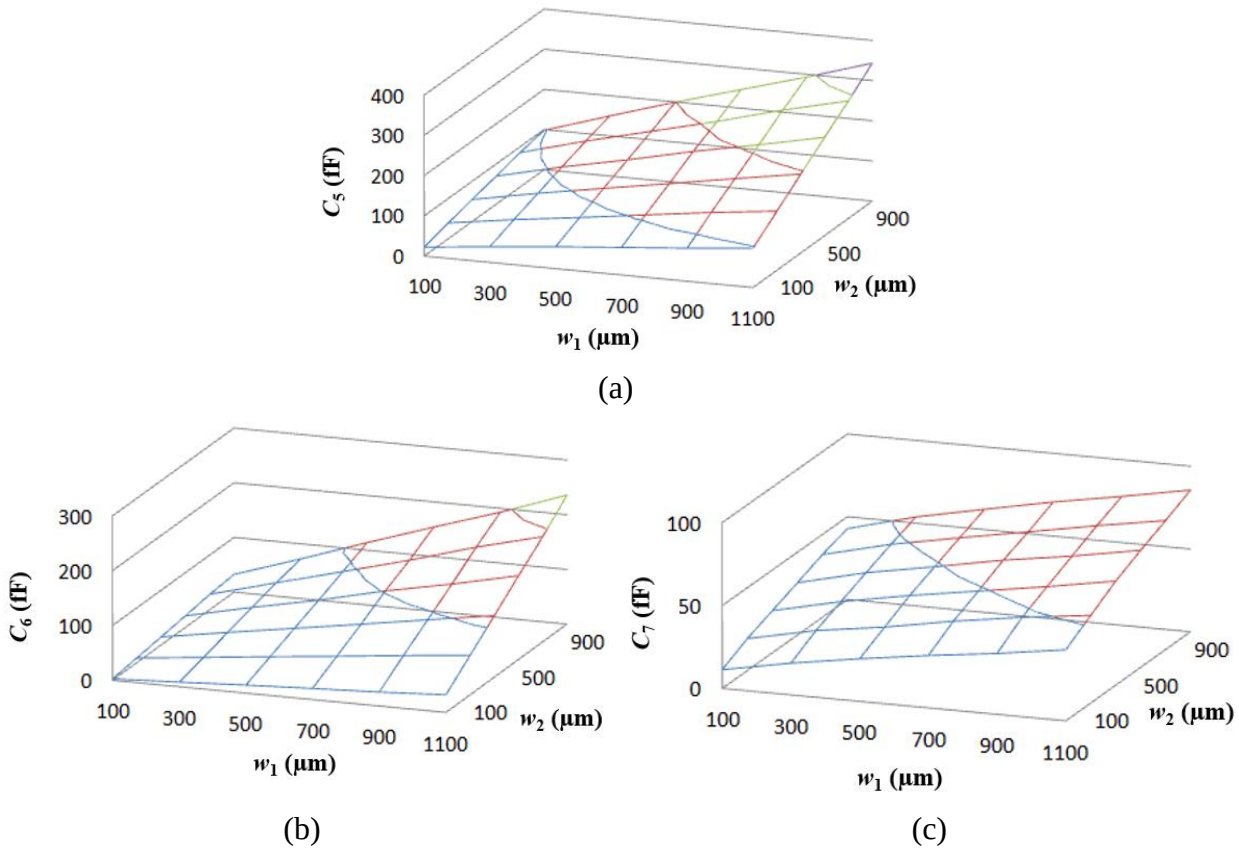


Figure III-16: Dependence on line widths w_1 and w_2 of (a) C_5, (b) C_6, and (c) C_7.

Although the results obtained from EM simulation are very accurate, they cannot give analytical functions expressing the physical relations between extracted electrical values and geometric dimensions. This section focuses on determining capacitive coupling as a function of geometric interconnection dimensions by using an electrostatic approach.

Figure III-16 shows the capacitances C_5, C_6, and C_7 as functions of line widths (w_1 and w_2) extracted from EM simulation results. The C_5, C_6, and C_7 functions (Eq. (III-60) - (III-62)) determined by the curve fitting technique consist of four terms. The first term corresponds to the fringing effects at the corners. The second and third terms relate to the peripheral fringing effects. The last term relates to parallel-plate capacitance. For the capacitance C_7 between the upper line and the ground plane, its parallel-plate term is about 10 times smaller than its other terms if w_1 and w_2 equal to 100 μm. As a result, C_7 is assumed to consist of only fringing capacitances.

$$C_5 = 1.15 + 5.99\times10^{-2}\times w_1 + 5.7\times10^{-2}\times w_2 + 1.68\times10^{-4}\times w_1\times w_2 \quad \text{(III-60)}$$

$$C_6 = -1.5 + 1.3\times10^{-2}\times w_1 + 1.17\times10^{-2}\times w_2 + 1.72\times10^{-4}\times w_1\times w_2 \quad \text{(III-61)}$$

$$C_7 = 7.27 + 3.07\times10^{-2}\times w_1 + 3.03\times10^{-2}\times w_2 + 1.08\times10^{-5}\times w_1\times w_2 \quad \text{(III-62)}$$

Where:

- The capacitances (C_5, C_6, C_7) are in fF
- The widths (w_1, and w_2) are in μm

A rectangular line of width w_2 and thickness t will be approximated by a combination of one rectangular line of width $w_2 - t/2$ and two semi-circular lines of radius $t/2$ (Figure III-17 (a) and (b)). The capacitances are separated into one part between two parallel plates and the other between two circular lines (Figure III-17(d)). We note that C_i^p, and C_i^f is the parallel-plate and fringing parts respectively of capacitance C_i.

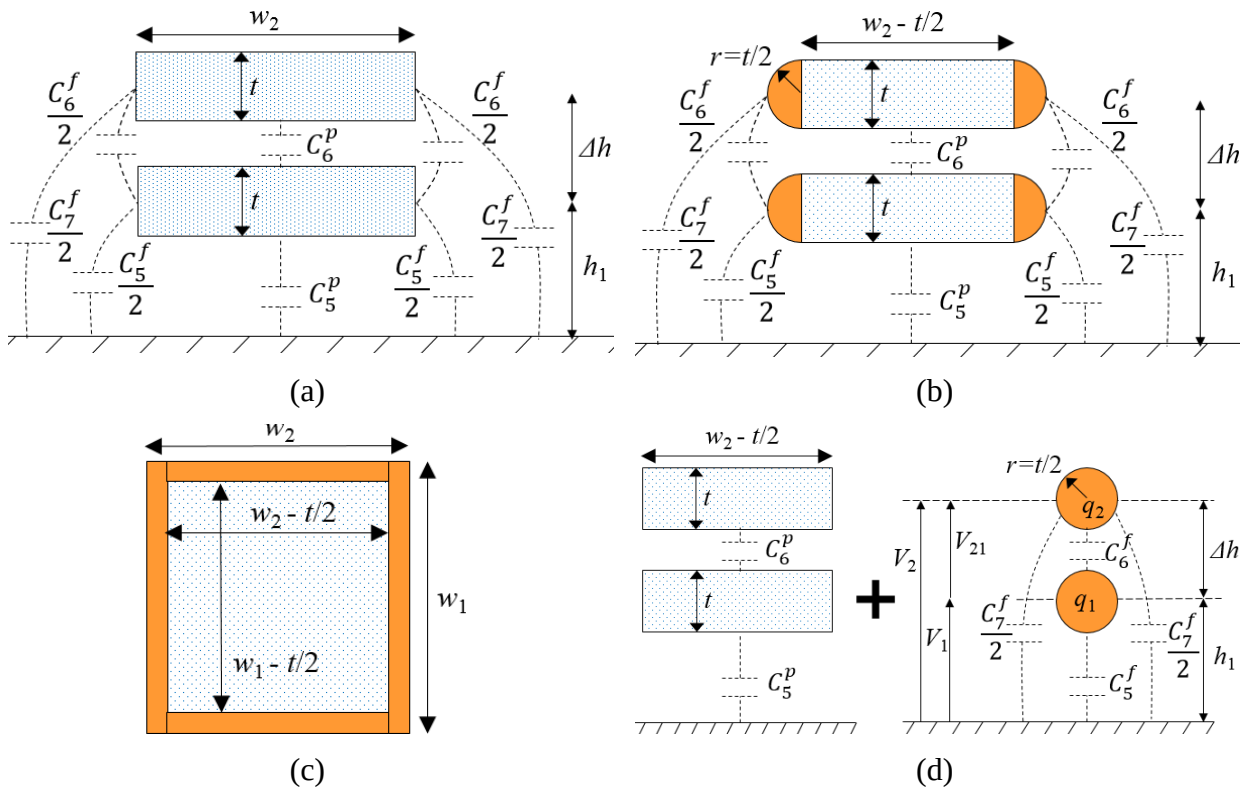


Figure III-17: Crossing line approximation. (a) Original crossing lines. (b) Rectangular cross section replaced by a rectangular and two semicircular ones. (c) Top view of the lines. (d) Capacitance calculation.

Calculation of the fringing capacitances C_i^f is based on electrostatic theory. We note that V_1, q_1, V_2, q_2 are the electric potential and charge of line 1 and line 2 respectively. The potentials V_1, V_2 created by infinite lines of charge q_1, q_2 over a ground plane (Figure III-17(d)) are described in Eq. (III-63).

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \frac{1}{2\pi\varepsilon_0\varepsilon_{eff} \times \text{length\_of\_line}} \begin{bmatrix} \ln\frac{2h_1}{r} & \ln\frac{\Delta h + 2h_1}{\Delta h} \\ \ln\frac{\Delta h + 2h_1}{\Delta h} & \ln\frac{2\Delta h + 2h_1}{r} \end{bmatrix} \begin{bmatrix} q_1 \\ q_2 \end{bmatrix} \qquad \text{(III-63)}$$

If the lines are at a potential V_1, V_2, their charges q_1, q_2 are calculated by Eq. (III-64).

$$\begin{bmatrix} q_1 \\ q_2 \end{bmatrix} = \begin{bmatrix} C_5^f + C_6^f & -C_6^f \\ -C_6^f & C_7^f + C_6^f \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad \text{(III-64)}$$

Expressing a fringing capacitances C_i^f through a shape factor k_i^{shape}(i = 5, 6, 7) will simplify the next equations. The relation between C_i^f and k_i^{shape} is described by Eq. (III-65).

$$C_i^f = \varepsilon_0 \varepsilon_{eff} \times k_i^{shape} \times \text{length\_of\_line} \tag{III-65}$$

From Eq. (III-63), (III-64), and (III-65), we have:

$$\begin{bmatrix} k_5^{shape}+k_6^{shape} & -k_6^{shape} \\ -k_6^{shape} & k_7^{shape}+k_6^{shape} \end{bmatrix} = 2\pi \times \begin{bmatrix} \ln\dfrac{2h_1}{r} & \ln\dfrac{\Delta h+2h_1}{\Delta h} \\ \ln\dfrac{\Delta h+2h_1}{\Delta h} & \ln\dfrac{2\Delta h+2h_1}{r} \end{bmatrix}^{-1} \tag{III-66}$$

Therefore:

$$k_5^{shape} = \frac{2\pi \ln\dfrac{4\Delta h(h_1+\Delta h)}{t(2h_1+\Delta h)}}{\ln\dfrac{4h_1}{t}\ln\dfrac{4(h_1+\Delta h)}{t} - \left(\ln\dfrac{2h_1+\Delta h}{\Delta h}\right)^2} \tag{III-67}$$

$$k_6^{shape} = \frac{2\pi \ln\dfrac{2h_1+\Delta h}{\Delta h}}{\ln\dfrac{4h_1}{t}\ln\dfrac{4(h_1+\Delta h)}{t} - \left(\ln\dfrac{2h_1+\Delta h}{\Delta h}\right)^2} \tag{III-68}$$

$$k_7^{shape} = \frac{2\pi \ln\dfrac{4\Delta h h_1}{t(2h_1+\Delta h)}}{\ln\dfrac{4h_1}{t}\ln\dfrac{4(h_1+\Delta h)}{t} - \left(\ln\dfrac{2h_1+\Delta h}{\Delta h}\right)^2} \tag{III-69}$$

For example, capacitance C_5 is calculated as Eq. (III-70).

$$C_5 = C_5^p + C_5^f = \varepsilon_0 \varepsilon_{eff} \frac{(w_1 - t/2)(w_2 - t/2)}{h_1} + \varepsilon_0 \varepsilon_{eff} k_5^{shape}(w_1 + w_2 - t/2) \tag{III-70}$$

Finally, we have:

$$C_5 = \varepsilon_0 \varepsilon_{eff} \frac{t}{2}\left(\frac{t}{2h_1} - k_5^{shape}\right) + \varepsilon_0 \varepsilon_{eff}\left(k_5^{shape} - \frac{t}{2h_1}\right)(w_1 + w_2) + \varepsilon_0 \varepsilon_{eff} \frac{w_1 w_2}{h_1} \tag{III-71}$$

$$C_6 = C_6^p + C_6^f = \varepsilon_0\varepsilon_{eff}\frac{t}{2}\left(\frac{t}{2\Delta h} - k_6^{shape}\right) + \varepsilon_0\varepsilon_{eff}\left(k_6^{shape} - \frac{t}{2\Delta h}\right)(w_1 + w_2) + \varepsilon_0\varepsilon_{eff}\frac{w_1 w_2}{\Delta h} \quad \text{(III-72)}$$

$$C_7 = C_7^f = -\varepsilon_0\varepsilon_{eff}k_7^{shape}\frac{t}{2} + \varepsilon_0\varepsilon_{eff}k_7^{shape}(w_1 + w_2) \quad \text{(III-73)}$$

III.3.4. Model verification

Table III-3 compares the capacitances extracted from EM simulation and calculated by Eq. (III-71) - (III-73). The analytical values are close to the ones of simulation. Relative error is 13% for C_5, 6% for C_6 and 0.8% for C_7. The differences are probably from the assumptions of effective permittivity, and electrostatic approach. The values extracted from EM simulation for resistances and inductances using Eq. (III-51) - (III-54) are presented in Table III-4. The coefficients of coupling k_{12} and k_{34} are determined by tuning method.

Table III-3: Capacitances obtained from EM simulation and analytical calculation

	C_5 (fF)	C_6 (fF)	C_7 (fF)
EM simulation	343.2	235.8	85.59
Analytical calculation	297	221.9	84.88

Table III-4: Self-inductances, coefficients of coupling and resistances obtained from EM simulation

L_1 (nH)	R_1 (Ω)	L_2 (nH)	R_2 (Ω)	L_3 (nH)	R_3 (Ω)	L_4 (nH)	R_4 (Ω)	k_{12}	k_{34}
0.249	0.064	0.256	0.066	0.426	0.196	0.426	0.202	0.17	0.16

Where

- ✓ k_{12} is the coefficient of coupling between self-inductances L_1 and L_2.
- ✓ k_{34} is the coefficient of coupling between self-inductances L_3 and L_4.

Using the analytical values in Table III-3 for capacitances, and the values in Table III-4 for the other elements, the electrical model in Figure III-15 has been built and simulated with Keysight's ADS software. The obtained *S* parameters have been compared with EM simulation in Figure III-18. A good agreement both in magnitude and in phase are observed from 0 to 20 GHz.

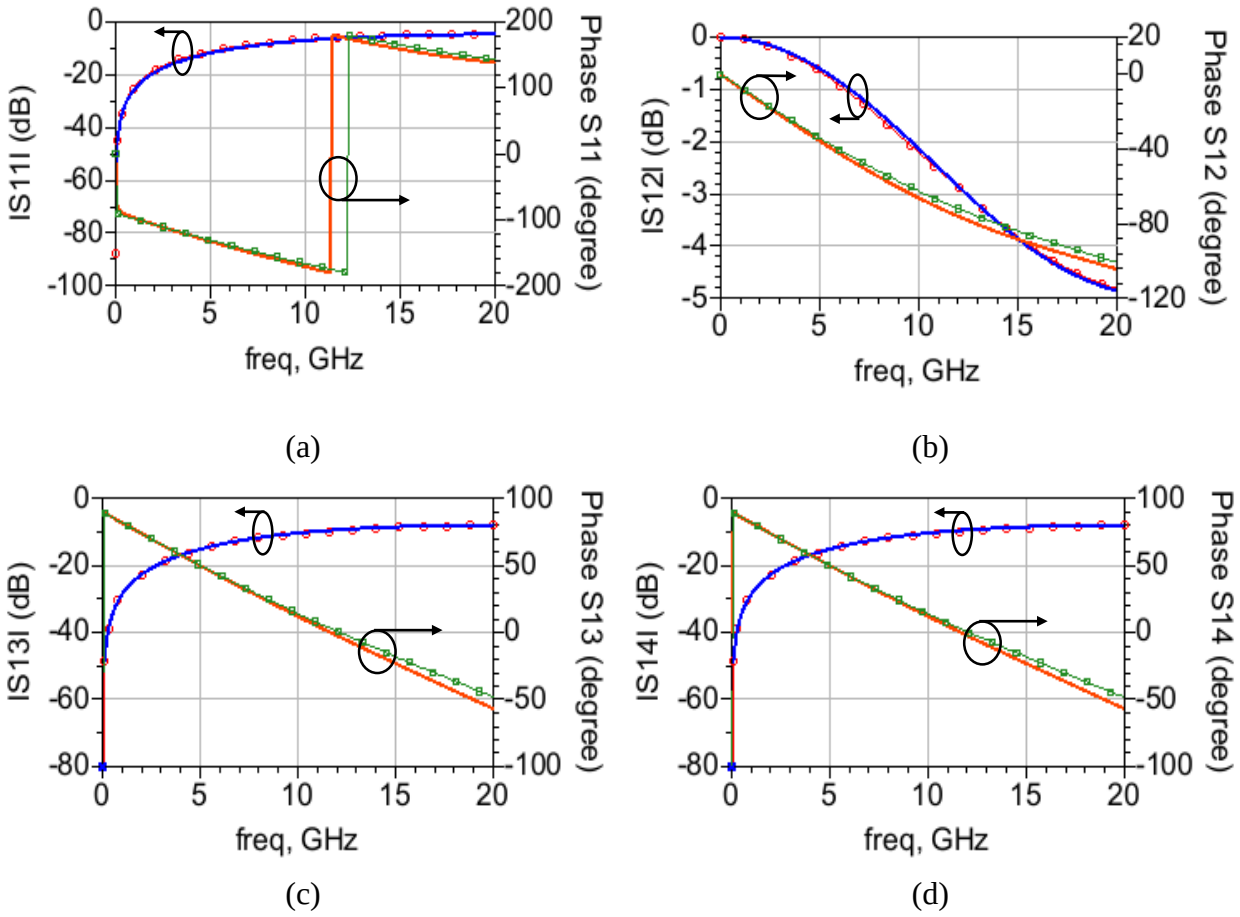


Figure III-18: Comparison between EM simulation and model. (a) S_{11}. (b) S_{12}. (c) S_{13}. (d) S_{14}

III.3.5. Conclusion

We have shown a simplified model of crossing lines that uses only analytical expressions. Its aim is not to be more accurate than the others, but to be calculated within a shorter time. They can be integrated into optimization software in which the calculation time is very short. Lots of optimization steps may be performed in a reasonable time.

III.4. Return-Path current

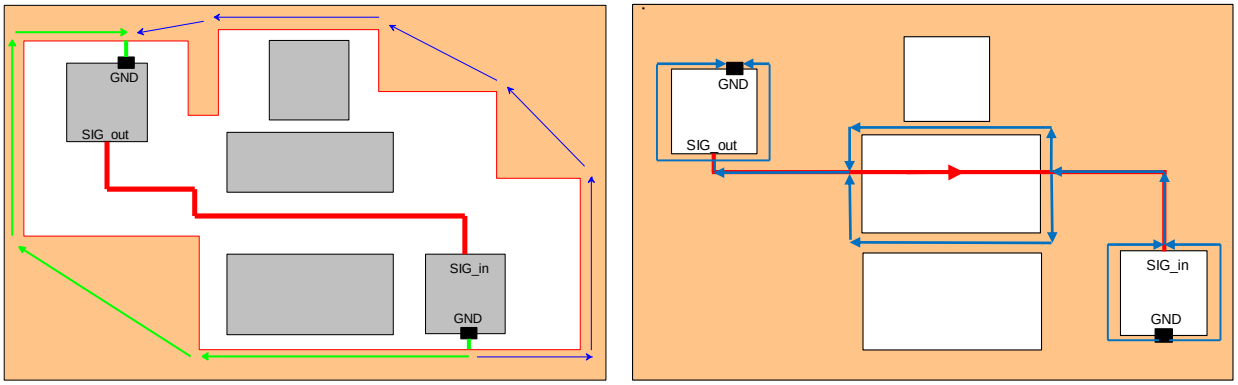
III.4.1. Introduction

When a signal SIG is generated by a pin from a component, some current flows through the associated wire. Because there is no accumulated electrical charge in the circuit having generated this current, this outgoing current has to be compensated by a GND current of the same value (at least in a quasi-static mode) going into the GND pin of the component. The problem is to trace the path for this return current in the structure.

The idea is that, once the SIG path has been fixed *in a thin wire*, the return (GND) path current always takes the geometrical configuration that minimizes the overall dissipated energy of the system, while still obeying of course to Maxwell's equations. This implies that the GND current tire to keep geometrically as near as possible to the SIG wire, or to the nearest border of the voids in the GND plane.

With the following hypotheses, an analysis of the different situations in a 3D SiP structure has to be drawn.

- Quasi-static conditions of a distribution of currents in space. These conditions are quite true if the smallest guided wavelength used is a few times bigger than the maximal dimension of the layers.
- Thin SIG wires (diameter smaller than the height of the dielectric layer onto which it is imprinted)



(a) (b)

Figure III-19: Typical situations encountered. (a) SIG and GND in the same layer. (b) SIG and GND in different layers

Figure III-19 presents two typical situations encountered: SIG and GND in the same layer and SIG and GND in different layers. The first situation corresponds to a coplanar configuration. In this case, the components, the SIG wires and the GND pseudo plane are on the same plane. The rule is that the GND return-current path will always take a path which is geometrically closest as possible to the SIG wire. In Figure III-19(a), the return-path current (GND current) will be divided

from the load circuit GND into 2 parts. The green part is supposed here to be the smallest resistance path. However, due to the potential difference between the two GND pins, there is also another current (the blue part) which flows on the other way. The resistance of this path is higher, which means that the blue current has a lower value.

If we have a micro-strip configuration in the second situation, the GND current has the tendency to crowd under the SIG wire, as is well known. The width of this GND "current strip" is to a first order proportional to the dielectric thickness. In a simple configuration such as in Figure III-20 where there is no hole in the GND plane under the SIG wire, the return-path current follows the projection of the SIG current, as far as the SIG and GND pins are close to each other from the two circuits (the one generating SIG_out and the one receiving SIG_in). If there is a hole in the GND plane under the SIG wire such as in Figure III-19(b), in the same way as in the coplanar configuration, the current divides around the hole into 2 parts that can be evaluated.

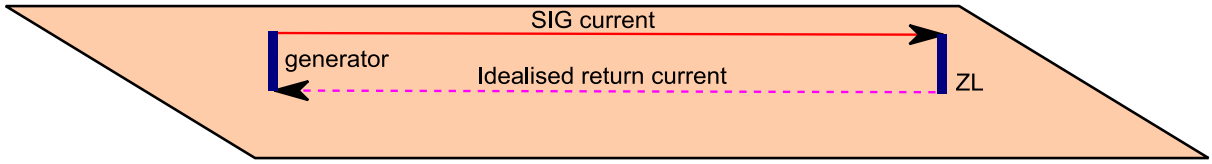


Figure III-20: Idealized return current

This paragraph is organized as follows. Section III.4.2 introduces the equations to verify the return-path current. Section III.4.3 discusses on the comparisons with EM simulations. Finally, section III.4.4 concludes the approach.

III.4.2. Return path modeling

Let's consider a simple example in Figure III-21 where current *i* flows through a SIG wire in red color, and returns through a holed ground plane in green color under the SIG wire.

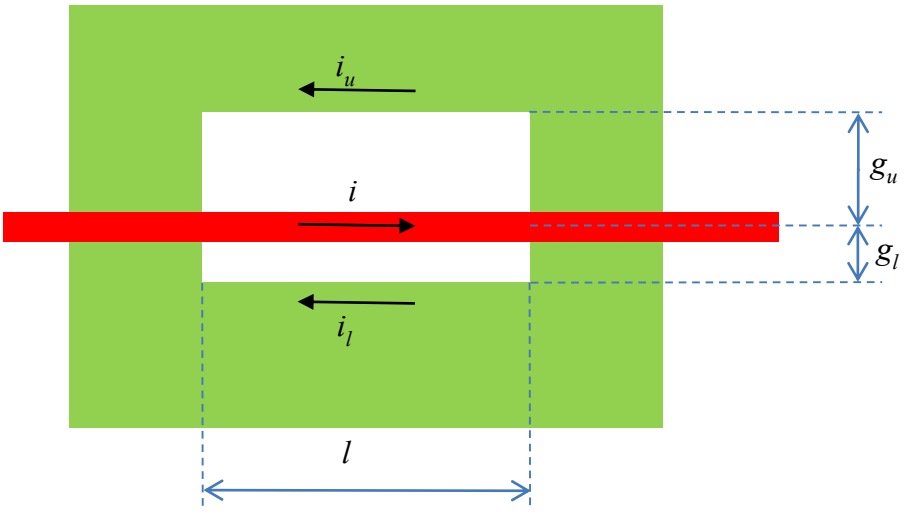


Figure III-21: Return path dimensions

The hole on ground plane has a variant length l and a variant width $g_u + g_l$. The distance to the SIG wire of the upper and lower edges of the hole will be changed by varying g_u and g_l. Meanwhile, the SIG wire has a fixed position. Due to the hole, the lowest impedance path on ground plane is along the edges of the hole. The return-path current is separated into two parts: current i_u flowing along the upper edge, and current i_l flowing along the lower edge.

The upper path length is determined by Eq. (III-74) and the lower path length is determined by Eq. (III-75).

$$d_u = l + 2g_u \tag{III-74}$$

$$d_l = l + 2g_l \tag{III-75}$$

The impedances of the upper and lower paths are respectively proportional to d_u and d_l. The global impedance of two paths should be proportional to

$$\frac{d_u d_l}{d_u + d_l} = \frac{(l + 2g_u)(l + 2g_l)}{2l + 2g_u + 2g_l} \tag{III-76}$$

The upper and lower currents are

$$i_u = \frac{V}{Kd_u}, \quad i_l = \frac{V}{Kd_l} \tag{III-77}$$

Where

- V is the voltage between the edges of the hole.
- K is a proportion coefficient which should depend on the skin effect and increase like $f^{1/2}$.

The proportions of upper and lower currents are:

$$P_u = \frac{i_u}{i_u + i_l} = \frac{\frac{1}{d_u}}{\frac{1}{d_l} + \frac{1}{d_u}} = \frac{\frac{1}{l + 2g_u}}{\frac{1}{l + 2g_l} + \frac{1}{l + 2g_u}} = \frac{l + 2g_l}{2l + 2g_u + 2g_l} \tag{III-78}$$

$$P_l = \frac{i_l}{i_u + i_l} = \frac{\frac{1}{d_l}}{\frac{1}{d_l} + \frac{1}{d_u}} = \frac{\frac{1}{l + 2g_l}}{\frac{1}{l + 2g_l} + \frac{1}{l + 2g_u}} = \frac{l + 2g_u}{2l + 2g_u + 2g_l} \tag{III-79}$$

III.4.3. Simulation and result

The return-path current structure in Figure III-21 has been simulated in EMPro, a 3D full-wave EM simulator. Figure III-22 shows the structure and its model at 0 Hz containing only resistances. The ports represented by green arrows have been put at two ends of the micro-strip line. The return path structure was simulated from 0 to 1 GHz. The proportion of the upper and lower currents can be expressed through global resistance calculated from EM simulation results.

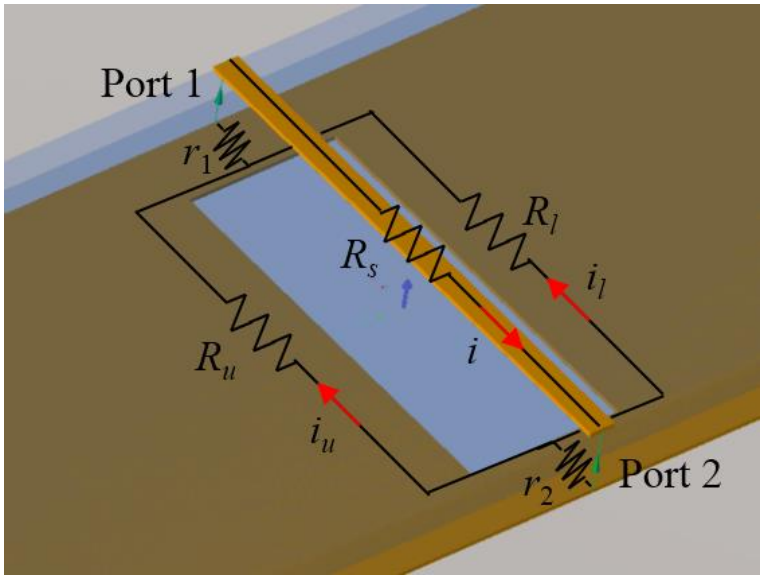


Figure III-22: Return-path current structure and its model at 0 Hz

The dimensions of the structure will be varied. There are 3 independent dimensions:

- Length l
- Upper part's width g_u
- Lower part's width g_l

Because the structure is symmetrical, we must vary only one width (either the upper part's width g_u or the lower part's width g_l). As a result, we simplify a problem of 3 independent variables to the one of 2 independent variables (Length l and one width).

III.4.3.1. Variation of the upper part width g_u

Ten EM simulations have been made with the upper part's width g_u varying from 0 to 9.5 mm. Meanwhile the length l maintained a constant value of 1.5 mm and the lower part's width g_l had also a constant value of 0.3 mm.

The global resistance of this structure has been extracted from *Y* parameter at 0 Hz by the following formula.

$$R_{global} = -\text{real}\left[\frac{1}{Y(1,2)}\right] \tag{III-80}$$

The global resistance consists of R_S, r_1, r_2, and R_u // R_l in series.

$$R_{global} = R_s + r_1 + r_2 + \frac{R_u R_l}{R_u + R_l} \tag{III-81}$$

Because during the simulations, all dimensions were not changed except the upper width g_u, the value of $R_S + r_1 + r_2$ is assumed to be constant for all the simulations. So, it can be calculated when $g_u = 0$, for example.

$$R_s + r_1 + r_2 = R_{global}\Big|_{g_u=0} - \frac{R_u R_l}{R_u + R_l}\Bigg|_{g_u=0} \tag{III-82}$$

We note that $\Delta R_{ul}\big|_{g_u}$ is the variation of global resistance in comparison to the first simulation.

$$\Delta R_{ul}\big|_{g_u} = \frac{R_u R_l}{R_u + R_l}\Bigg|_{g_u} - \frac{R_u R_l}{R_u + R_l}\Bigg|_{g_u=0} = R_{global}\big|_{g_u} - R_{global}\big|_{g_u=0} \tag{III-83}$$

Using the curve fitting technique, we can demonstrate that the variation of $\Delta R_{ul}\big|_{g_u}$ against g_u shown in Figure III-23 respects Eq. (IV-35). Its approximate function in Eq. (IV-43) contains 2 terms:

- The first one "$7.46\frac{l + 2g_u}{2l + 2g_u + 2g_l}$" as a function of g_u corresponds to $\frac{R_u R_l}{R_u + R_l}\Big|_{g_u}$.
- The second one "2.7" corresponding to $\frac{R_u R_l}{R_u + R_l}\Big|_{g_u=0}$ can be calculated from the first one by replacing g_u by zero.

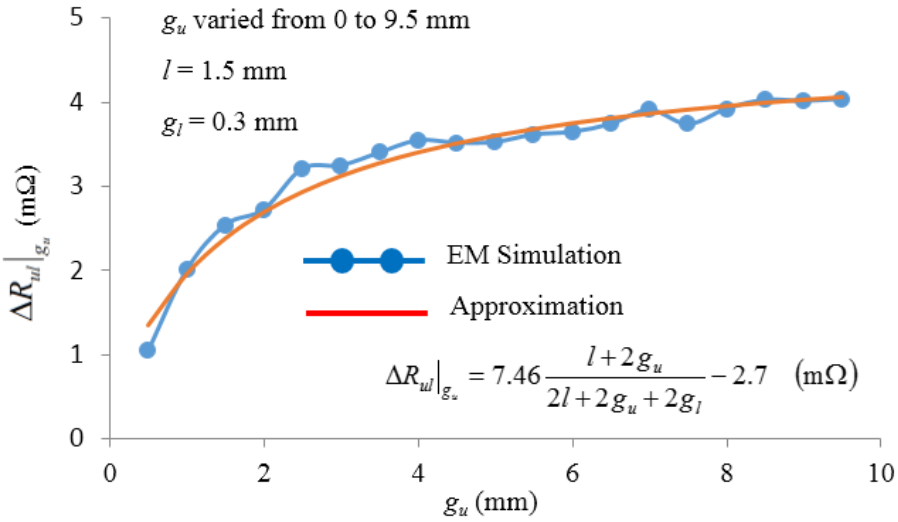


Figure III-23: Variation of $\Delta R_{ul}|_{g_u}$ against g_u

$$\Delta R_{ul}|_{g_u} = 7.46\frac{l+2g_u}{2l+2g_u+2g_l} - 2.7 = 7.46\frac{1.5+2g_u}{3.6+2g_u} - 2.7 \quad (\text{m}\Omega) \tag{III-84}$$

Figure III-24 shows the variation of the global resistance in function of frequency. This variation is proportional to $f^{1/2}$.

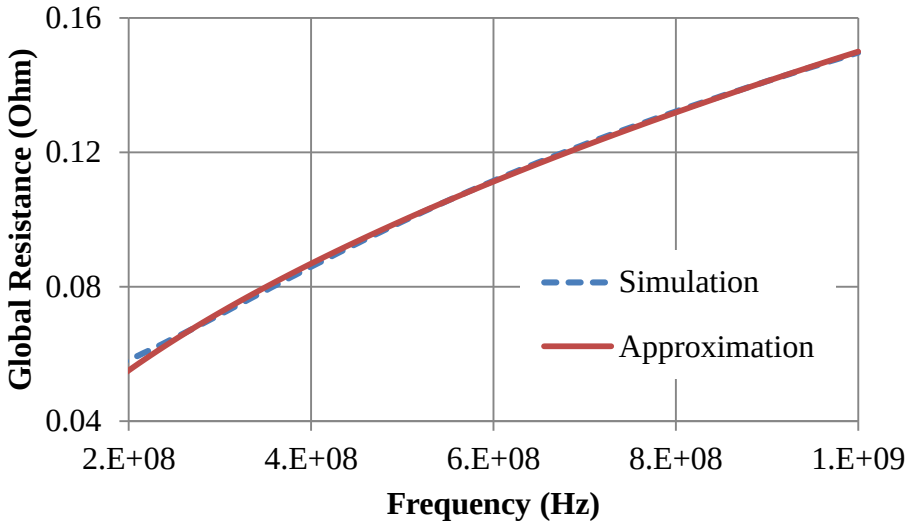


Figure III-24: Variation of the resistance in function of frequency

$$R_{global} = -2.16\times10^{-2} + 5.43\times10^{-6}\times\sqrt{f} \tag{III-85}$$

III.4.3.2. Variation of the length *l*

We varied the length *l* from 0.1 mm to 1.5 mm, and maintained constant the upper and lower widths. g_u had a value of 1 mm and g_l had a value of 0.3 mm. The negative poles of the ports were put on the edges of the hole so that the ground plane is modeled by R_u and R_l in parallel. The signal line had a length of 2 mm in all the simulations.

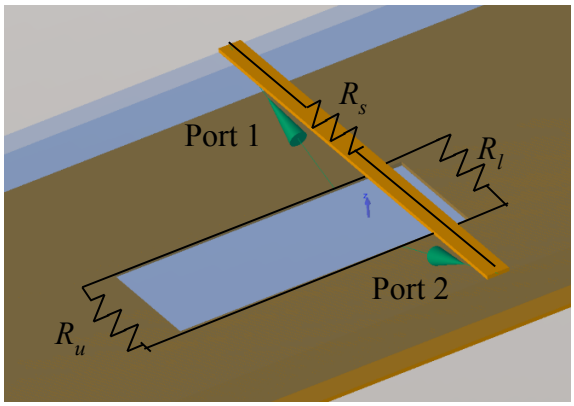


Figure III-25: Negative pole of the ports on the edges of the hole

The resistances r_1 and r_2 are eliminated when we put the negative pole of the ports on the edges of the hole (Figure III-25).

$$R_{global} = R_s + \frac{R_u R_l}{R_u + R_l} \tag{III-86}$$

So,

$$\Delta R_{ul}\big|_l = \frac{R_u R_l}{R_u + R_l}\bigg|_l - \frac{R_u R_l}{R_u + R_l}\bigg|_{l=0.1mm} = R_{global}\big|_l - R_{global}\big|_{l=0.1mm} \tag{III-87}$$

Figure III-26 shows the variation of $\Delta R_{ul}\big|_l$ as a function of *l*. We can find an approximate function as Eq. (III-88). Therefore the resistance of the upper and lower paths is a function of the length *l* which respects Eq. (III-76).

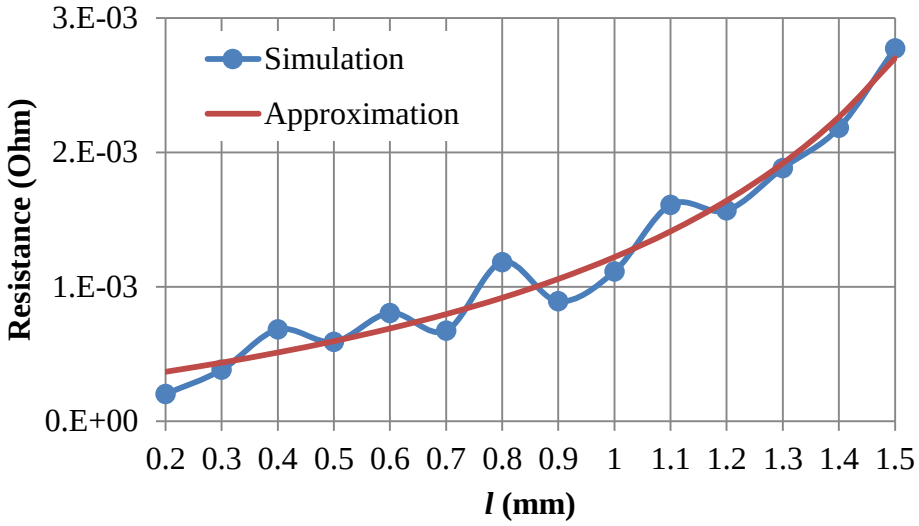


Figure III-26: Variation of $\Delta R_{ul}\big|_l$ against l

$$\Delta R_{ul}\big|_l = \frac{l^2 + 4.96\times10^6 l - 1.22\times10^6}{-3.69\times10^9 l + 8.23\times10^9} + 3.98\times10^{-4} \quad (\text{m}\Omega) \tag{III-88}$$

III.4.4. Conclusion

The simple approach to trace return-path current flowing around a void on a ground plane has been verified for utility by using EM simulation. The current on ground plane intends to keep as close as possible the SIG current. Therefore it flows along the edges of the void. In addition, skin effect has been clearly seen in the variation of extracted resistance. This approach will simplify the calculations in a simulation tool developed in the project PARSIMO. A result obtained from this tool (Figure III-27 in the next page) shows the current distribution around a void.

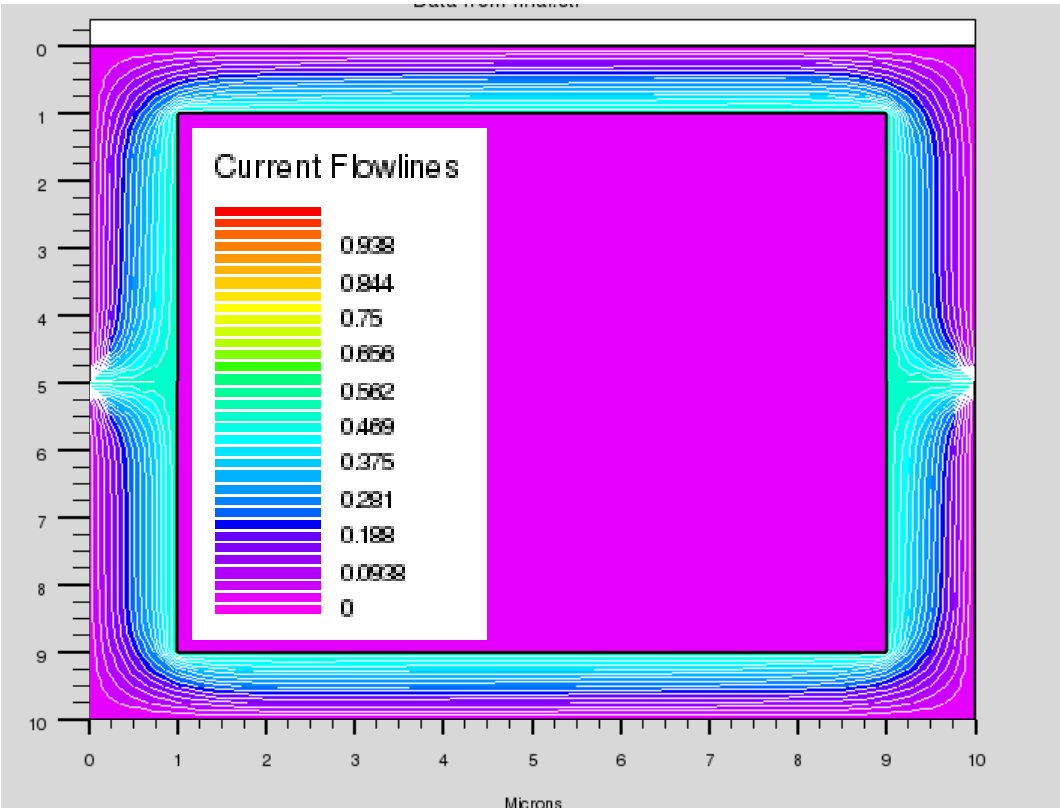


Figure III-27: An application of geometrical rules for return-path current in the project PARSIMO

III.5. Combline filter

III.5.1. Introduction

Generally, the comb-line filter models in recent publications are based on physical phenomena which leads complicated extraction equations. In fact, by investigating the distortion of the TEM EM-field pattern at the resonator open ends, a model was presented in [105]. The π-configuration model for a comb-line filter of two transmission lines presented in [104] uses two-port *Y* parameters in odd and even modes to extract model elements. Another proposed in [103] modeled a comb-line filter of three transmission lines with mutual inductance between two lines. As a result, increasing the number of the transmission lines in a filter makes modeling procedure more complex or even impossible. For some SiP applications, a simple nodal description with lumped elements is good enough (e.g. in SPICE). In this section, we propose a method to extract the lumped elements of an equivalent circuit using electromagnetic simulation results. This can be done in watching the variation of the admittance parameters against the frequency.

III.5.2. Modeling method

Each filter is described by a schematic in ADS software as shown in Figure III-28(a). An end of the transmission lines is connected to a capacitor and another end is connected to the ground. From this schematic, it is possible to simulate the filter using the parallel lines model of the software. It is also possible to generate the layout, like in Figure III-28(b) and to launch a 2.5D electromagnetic simulation. We have chosen this way. The capacitors have been replaced by simulation ports (C_1 to C_6 replaced by Port 3 to Port 8 respectively).

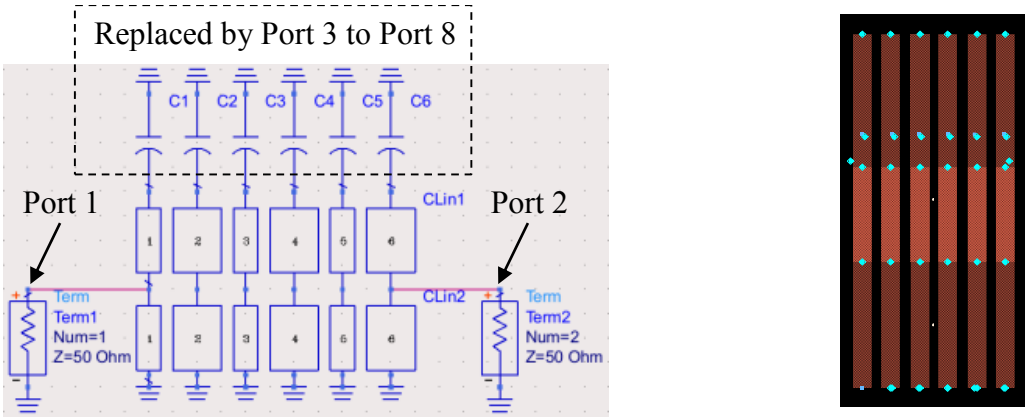


Figure III-28: Schematic of a filter. (a) Schematic. (b) Layout.

The S-parameters that are given by the simulation cannot be handled by nodal software like SPICE or Verilog-A. It is necessary to extract an equivalent circuit as shown in Figure III-29 with only discrete elements. Every two ports *i* and *j* are connected together by an impedance Z^f_{ij}. Port *i* is connected to the ground by an impedance Z^f_{ii}. The superscript ^{f} indicates "filter".

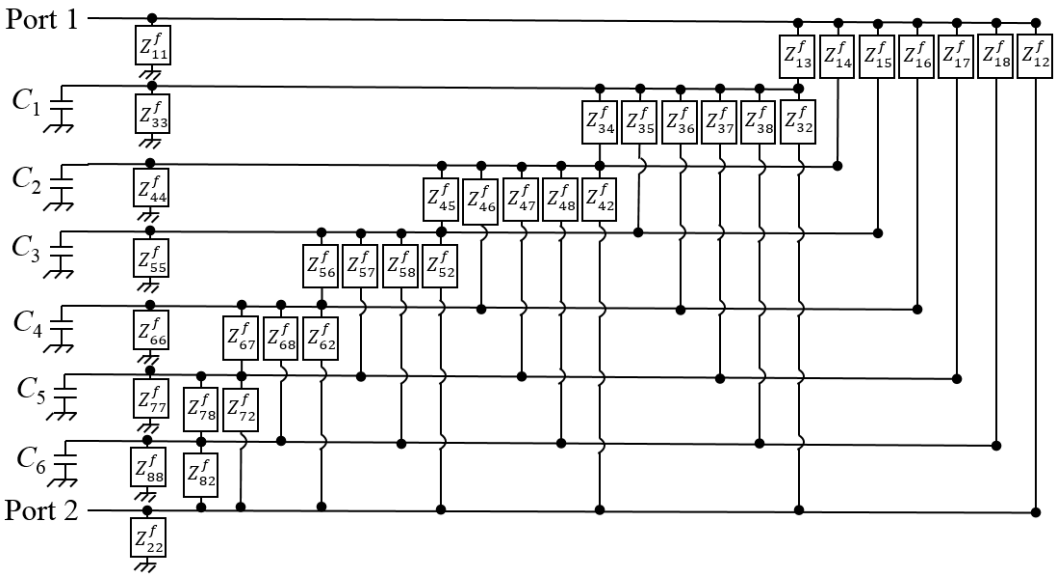


Figure III-29: Model of a comb-line filter.

The losses have not been included in the simulation. So, the equivalent circuit consists only of inductances and capacitances in series or in parallel. We transform the S-matrix into a Y-matrix. The admittance between ports *i* and *j* equals to $-Y(i, j)$ and the admittance between port *i* and the ground equals to $\Sigma_j Y(i, j)$.

$$Y^f_{ij} = -Y(i, j), \quad i, j = \{1..8\}, \quad i \neq j \tag{III-89}$$

$$Y^f_{ii} = \sum_{j=1}^{8} Y(i, j), \quad i = \{1..8\} \tag{III-90}$$

$$Z^f_{ij} = \frac{1}{Y^f_{ij}}, \quad i, j = \{1..8\} \tag{III-91}$$

As an example, Figure III-30 shows the variation of imag(Y^f_{34})ω against ω^2 for the filter #2. This variation is corresponding to an inductance and a capacitance in parallel. The inductance L_{34} can take the value of a point on the variation curve. Then its value will be corrected by a capacitance C_{34}. In order to get an identical determination of the extraction frequency for all filters, the central frequency, which is in the middle of the filter bandwidth, has been chosen. Finally, the inductance L_{34} is extracted at the central frequency; and the capacitance C_{34} is calculated from curve slope.

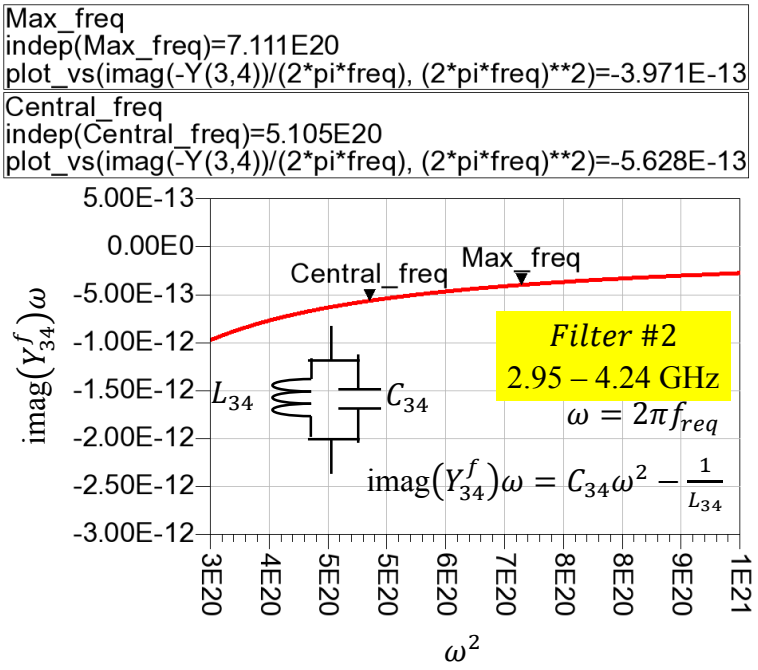


Figure III-30: Extraction of the elements of Y^f_{34}.

The extraction is very long due to a big number of elements, and many extraction equations. Thus the calculations will be expressed in matrix form. Each impedance Z^f_{ij} consists of a fundamental element and a correcting element. The inductances or the capacitances for the lower frequency can be considered as the fundamental terms. They can be corrected by a capacitance (resp. an inductance) in series or parallel according to the variation. We use a matrix **P** ("P" implies parallel) to define the topology of impedances Z^f_{ij}. If impedance Z^f_{ij} consists of an inductance and a capacitance in parallel, P_{ij} equals to 1. Meanwhile, the zero value of P_{ij} corresponds to series topology.

$$P_{ij} = \begin{cases} 1, & \text{if } L_{ij} \text{ and } C_{ij} \text{ in parallel} \\ 0, & \text{if } L_{ij} \text{ and } C_{ij} \text{ in series} \end{cases} \tag{III-92}$$

For parallel topology, fundamental element is L_{ij}; correcting element is C_{ij}; and admittance Y^f_{ij} is used for extraction (as shown in Figure III-30). In contrast, for series topology, fundamental element is C_{ij}; correcting element is L_{ij}; and impedance Z^f_{ij} is used for extraction. Either admittance Y^f_{ij} or impedance Z^f_{ij} is chosen by using a matrix **A** ("A" implies admittance) calculated from the matrix **P**.

$$A_{ij} = \begin{cases} Y_{ij}^f, & \text{if } P_{ij} = 1 \\ Z_{ij}^f, & \text{if } P_{ij} = 0 \end{cases} \tag{III-93}$$

Or:

$$\mathbf{A} = (\mathbf{O} - \mathbf{P})./\mathbf{Y^f} + \mathbf{P}.\times\mathbf{Y^f} \tag{III-94}$$

Where:

- The operators ".×", " ./ " describe element-by-element multiplication and division respectively.
- The elements of matrix $\mathbf{Y^f}$ are determined by Eq. (III-89) – (III-90).
- Matrix **O** has all elements O_{ij} equaling to one.

The fundamental elements are determined at the central frequency of the filter as Eq. (III-95).

$$\mathbf{E_{Fund}} = -\mathbf{O}./(\mathrm{imag}(\mathbf{A})\omega)\big|_{\text{central freq}} \tag{III-95}$$

The matrix **P** must be chosen so that all fundamental elements are positive in order to get a physical model. The accuracy of the model is improved with the correcting elements determined by Eq. (III-96). Because of the complexity of filters, the correcting element value can be positive or negative.

$$\mathbf{E_{Corre}} = \frac{\mathrm{imag}(\mathbf{A})\omega\big|_{\text{max freq}} - \mathrm{imag}(\mathbf{A})\omega\big|_{\text{central freq}}}{\omega^2\big|_{\text{max freq}}} \tag{III-96}$$

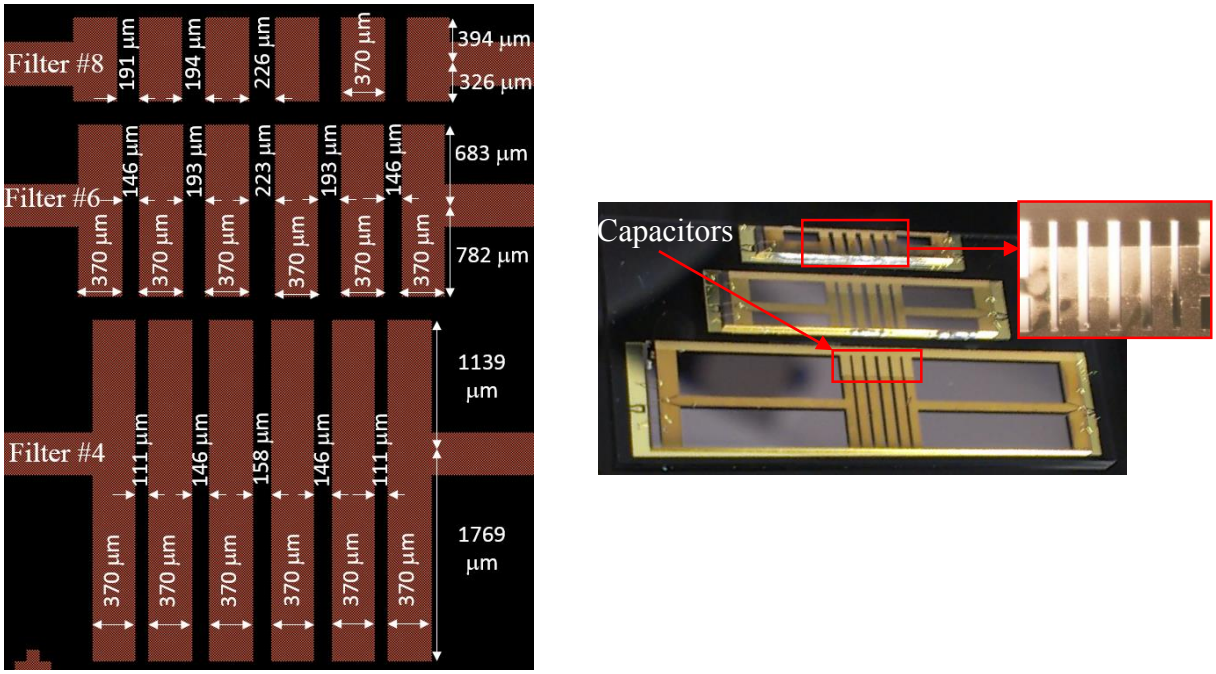
The elements L_{ij} and C_{ij} are determined as the elements of the following matrices **L** and **C**.

$$\mathbf{L} = \mathbf{P}.\times\mathbf{E_{Fund}} + (\mathbf{O} - \mathbf{P}).\times\mathbf{E_{Corre}} \tag{III-97}$$

$$\mathbf{C} = (\mathbf{O} - \mathbf{P}).\times\mathbf{E_{Fund}} + \mathbf{P}.\times\mathbf{E_{Corre}} \tag{III-98}$$

III.5.3. Simulation, measurement and discussion

EM simulation and measurement have been used to evaluate the modeling method. Figure III-31 shows the comb-line filters with their detail dimensions. The substrate has been made of glass with 250 μm thickness. The capacitors at an end of the lines have been realized with parallel plate configuration. The back and lateral sides have been metalized in copper to make ground plane and vias. The copper layers are protected by a flash gold layer. The fabricated filters are filter #4 operating from 2.95 to 4.24 GHz, filter #6 operating from 6.08 to 8.74 GHz, and filter #8 operating from 12.54 to 18 GHz. The input and output accesses have been de-embedded from the measurements performed by a two-port VNA.



(a) (b)

Figure III-31: Comb-line filters. (a) Filter dimensions. (b) Fabricated filters.

EM simulations have been also done using the schematic shown in Figure III-28(a) with the dimensions described in Figure III-31(a). The model-element values extracted from simulated *Y*-parameters have been summarized in Table III-5 where the missing elements can be found by symmetry. Only the highlighted impedances Z_{18}^{f}, and Z_{33}^{f} have series topology. The others consist of an inductance and a capacitance in parallel. Therefore, the models of filter #2, #4, #6, and #8 have the same schematic shown in Figure III-29. The modeling method can be simplified by using only fundamental elements. The simplified model in Figure III-32 has been used for verification.

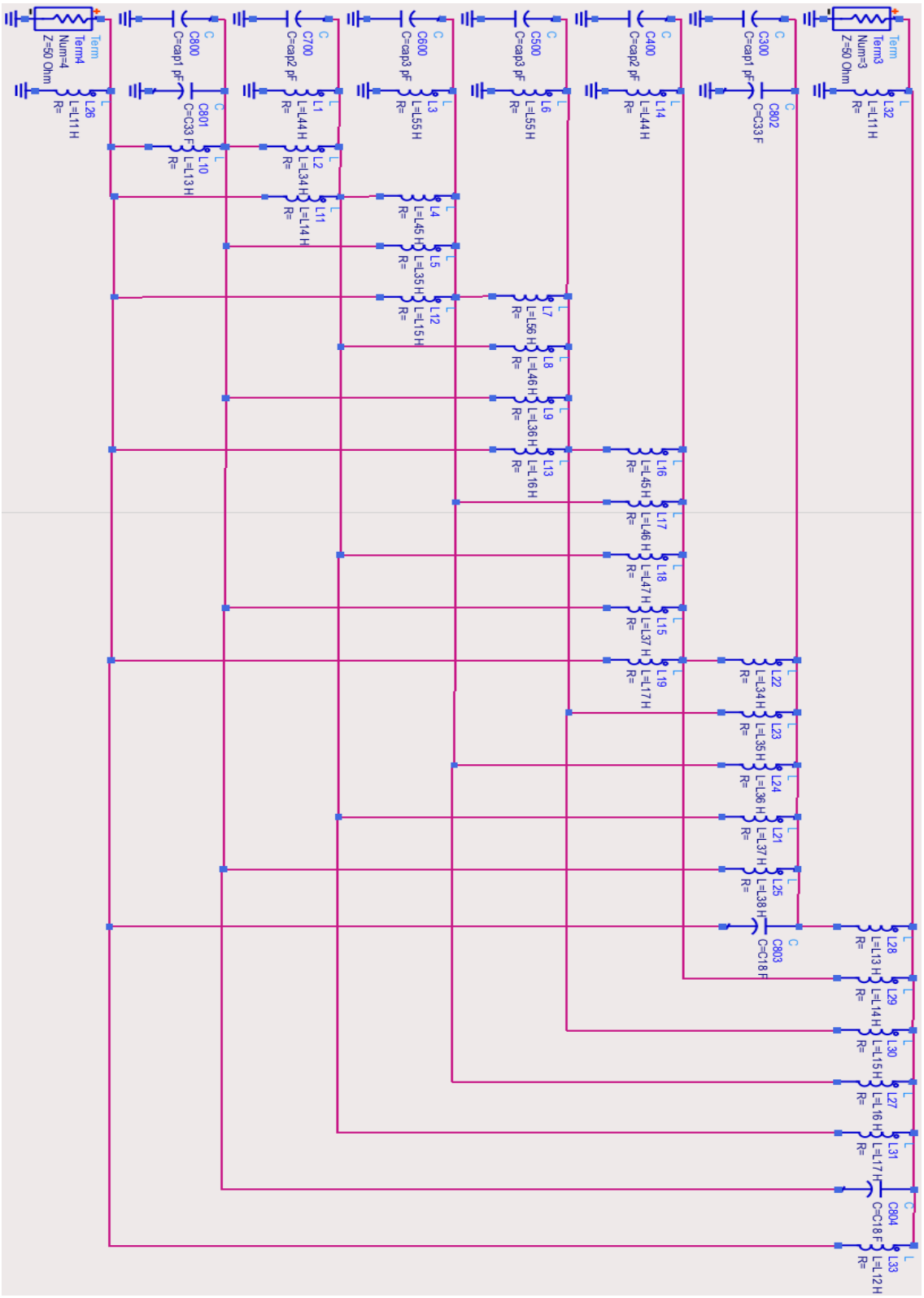


Figure III-32: Comb-line filter with only fundamental elements

Table III-5: Element values for filter #2, 4, 6, and 8

	Filter #2 1.44 – 2.06 GHz		**Filter #4 2.95 – 4.24 GHz**		**Filter #6 6.08 – 8.74 GHz**		**Filter #8 12.54 – 18 GHz**	
	Fund. @ 1.75 GHz	**Corr.**	**Fund. @ 3.6 GHz**	**Corr.**	**Fund. @ 7.4 GHz**	**Corr.**	**Fund. @ 15 GHz**	**Corr.**
Z_{11}^{f}	1.63 nH	434.3 fF	0.63 nH	136.90 fF	0.28 nH	68.47 fF	0.12 nH	33.65 fF
Z_{12}^{f}	78.42 nH	-1.91 fF	17.52 nH	-4.36 fF	12.06 nH	-0.05 fF	6.53 nH	0.05 fF
Z_{13}^{f}	1.51 nH	-77.69 fF	0.38 nH	-17.37 fF	0.23 nH	-11.5 fF	0.13 nH	-6.9 fF
Z_{14}^{f}	407.67 nH	-21.39 fF	249.5 nH	-8.05 fF	140.83 nH	-3.35 fF	74.61 nH	-1.49 fF
Z_{15}^{f}	936.79 nH	-9.45 fF	632.4 nH	-3.17 fF	330.88 nH	-1.43 fF	189.5 nH	-0.59 fF
Z_{16}^{f}	1756.45 nH	-5.09 fF	1307 nH	-1.55 fF	741.08 nH	-0.64 fF	1011 nH	-0.1 fF
Z_{17}^{f}	2928.37 nH	-3.06 fF	478.2 nH	-4.39 fF	1441.7 nH	-0.33 fF	2147 nH	-0.05 fF
Z_{18}^{f}	51.83 fF	-155 nH	66.22 fF	-29.13 nH	20.61 fF	-22.1 nH	7.59 fF	-14.08 nH
Z_{33}^{f}	735.25 fF	-7.64 nH	525.11 fF	-3.38 nH	232.6 fF	-1.7 nH	104.4 fF	-0.82 nH
Z_{34}^{f}	15.45 nH	50.35 fF	3.49 nH	22.36 fF	2.07 nH	10.09 fF	1.22 nH	3.81 fF
Z_{35}^{f}	141.62 nH	5.7 fF	40.05 nH	2.82 fF	21.10 nH	1.21 fF	10.72 nH	0.52 fF
Z_{36}^{f}	326.53 nH	2.29 fF	97.02 nH	1.19 fF	51.92 nH	0.52 fF	25.22 nH	0.13 fF
Z_{37}^{f}	558.76 nH	0.92 fF	146.1 nH	-1.78 fF	95.36 nH	0.27 fF	45.58 nH	0.1 fF
Z_{38}^{f}	219.83 nH	-0.88 fF	39.32 nH	-0.80 fF	30.92 nH	-0.13 fF	20.49 nH	-0.01 fF
Z_{44}^{f}	5.41 nH	276.9 fF	1.77 nH	80.96 fF	0.85 nH	41.53 fF	0.40 nH	19.68 fF
Z_{45}^{f}	17.37 nH	32.58 fF	4.20 nH	16.22 fF	2.56 nH	6.51 fF	1.25 nH	2.81 fF
Z_{46}^{f}	142.14 nH	1.12 fF	45.67 nH	0.89 fF	24.32 nH	0.19 fF	13.79 nH	1.52 fF
Z_{47}^{f}	337.29 nH	0.16 fF	113.9 nH	0.49 fF	59.87 nH	0.04 fF	29.02 nH	0.12 fF
Z_{55}^{f}	5.57 nH	273.3 fF	1.75 nH	78.39 fF	0.83 nH	43 fF	0.41 nH	19.92 fF
Z_{56}^{f}	14.76 nH	39.97 fF	4.43 nH	15.05 fF	2.86 nH	6.19 fF	1.40 nH	1.84 fF

Figure III-33 shows the evaluation of the proposed nodal models in comparison with EM simulation and measurement in the filter band-width. Filter #2 has not been measured. The verification has shown a good agreement in both magnitude and phase, particularly for filter #6 and #8. For filter #4, the measurement result has more losses than EM simulation and the filter model do. In fact, filter #4 is bigger than the other filters (see Figure III-31). Because the filter model does not take in account resistances, if a comb-line filter is small enough, its model is close to its measurement result. Therefore, the equivalent circuit with the fundamental terms is enough to model the comb-line filters in their bandwidth.

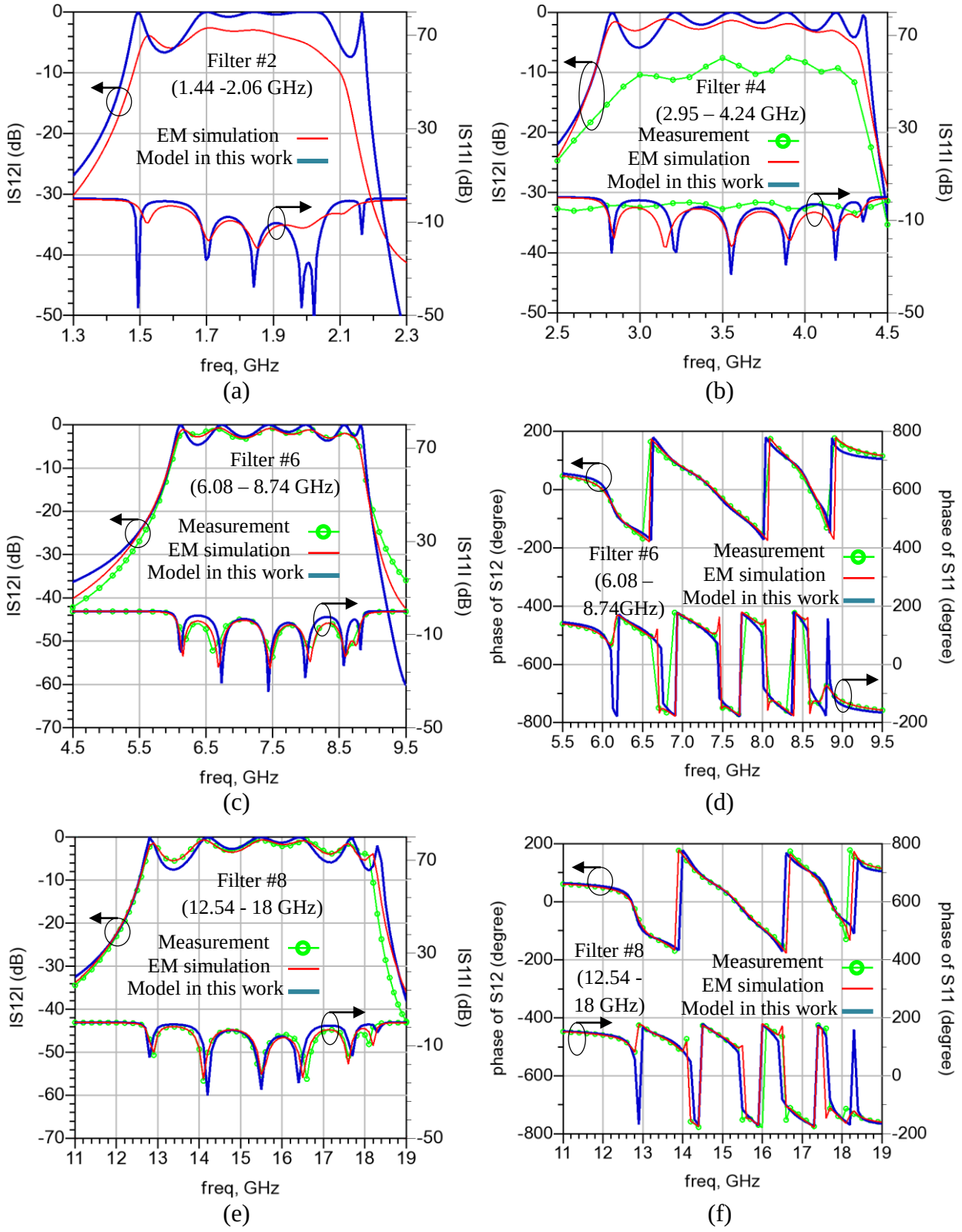


Figure III-33: Model, EM simulation, and measurement comparison. (a) Filter #2. (b) Filter #4. (c) Filter #6 in magnitude. (c) Filter #6 in phase. (e) Filter #8 in magnitude. (e) Filter #8 in phase

A validation in a large frequency band is presented in Figure III-35 where a difference between the filter model and measurement is observable at the frequencies far from the filter bandwidth. In that case, further elements must be put in parallel to describe these parasitic modes. We can also consider that the filter is disconnected by the MEMS switches when a signal at this frequency is present at the input of the total agile filter.

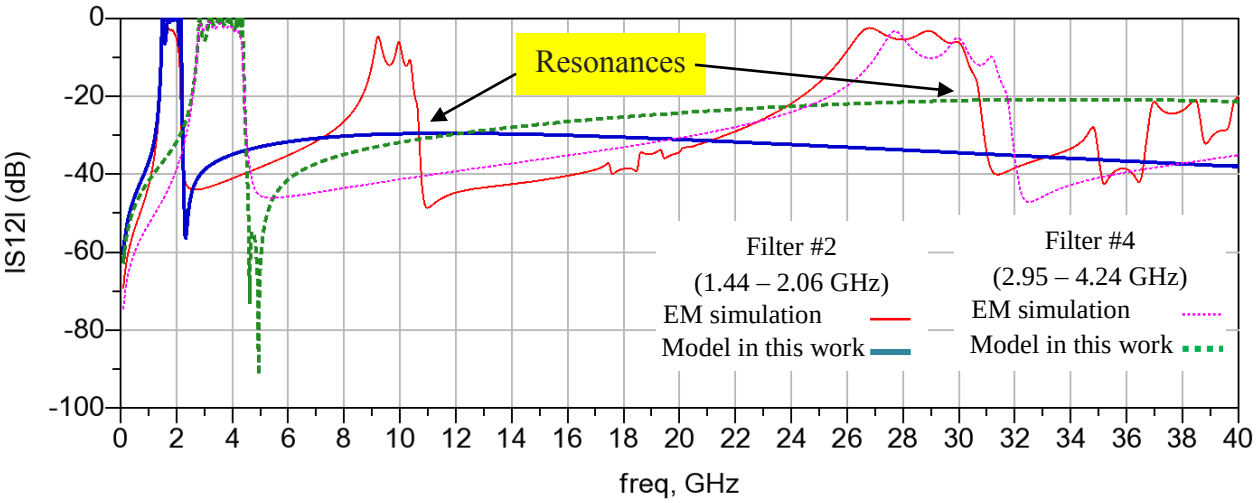


Figure III-34: Comparison from 0 to 40 GHz for filter #2 and #4

As an example, at 6.08 GHz, filter #5 is switched to filter #6. Thus the errors of their model outside their bandwidth are negligible.

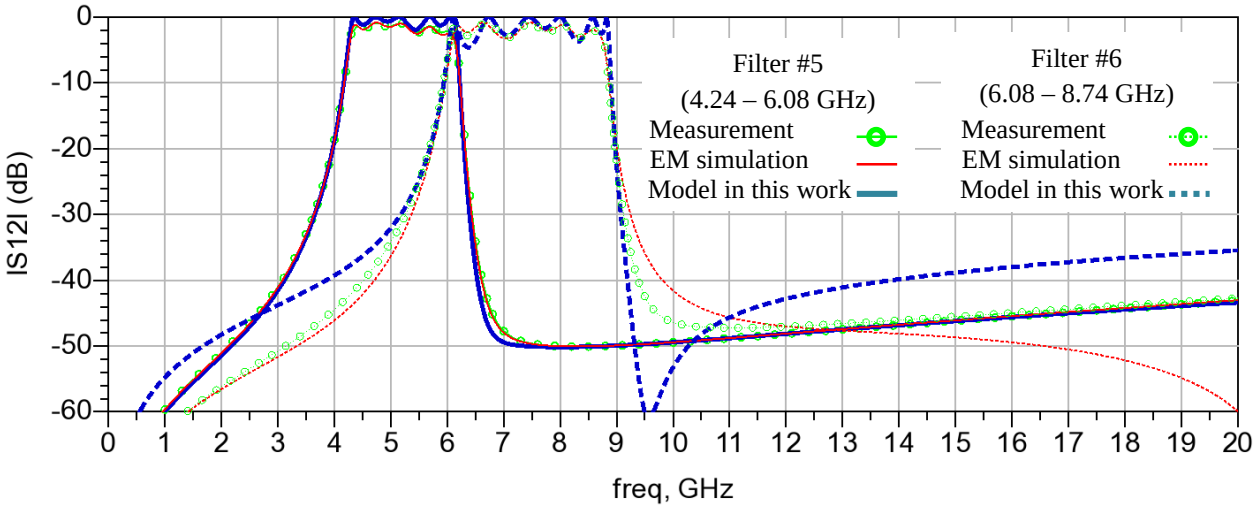


Figure III-35: Transition between filter #5 and filter #6

III.5.4. Conclusion

The modeling method for a comb-line filter presented in this section has been evaluated for its utility and accuracy in comparison with EM simulation and measurement. The nodal models with simple extraction equations will speed up the simulation procedure of a filter. In this thesis, the method has been verified with the comb-line filters which are composed of six transmission lines corresponding to six poles. It can be extended for a comb-line filter of different number of pole.

III.6. Synthesis, Conclusion and perspectives

The modeling methodologies for the critical interconnections, which are bonding wires, crossing lines, ground plane, and comb-line filter, have been presented in this chapter. The lumped-element models, which use geometric dimensions to calculate element values, have been evaluated by EM simulation and measurement with a good agreement.

- The model of two boding wires uses Spline functions to capture BW profile. An experimental structure has been realized on glass substrate to evaluate the model.
- The model of crossing lines is based on static approach to calculate capacitances. It were verified by EM simulation.
- For ground plane, 3D full wave simulation was used to trace return-current path.
- Comb-line filter model is based on a nodal approach which connects every two ports by an impedance. This approach uses very simple extraction equations from *Y* parameters. This nodal model is not physical, but can be easily integrated in behavioral software.

Only some interconnections have been modeled because of the time limitation of this thesis. A modeling method applicable for all types of interconnection has been imagined during the thesis. It will use the nodal principle of the comb-line filter model, or a neural network to imitate a system. Some mathematical operations will be performed to make these nodal models more physically.

Because of resulting quickly RF characteristics of a circuit, the lumped-element models are necessary for the pre-layout phase of package design. They have been verified by using EM simulation and measurement in an ideal condition where there is not any mutual coupling of the other circuits. However, the reality is more complex with couplings between different circuits. In that case where lumped-element models are not accuracy enough, EM simulations are used for characterization in post-layout phase of package design. The simulation methodologies will be developed in the next chapter.

Chapter IV

PARAMETRIC PACKAGE MODEL EXTRACTIONS FOR RF AND MM-WAVE APPLICATIONS

IV.1. Introduction

Packaging of integrated circuits impacts both their electrical, mechanical and thermal performances and represents a real challenge at RF and microwave frequencies. It is well established that performances of packaged RFICs significantly differ from their on-chip (on-wafer) performances. Thus, the optimization of the overall system requires Chip-Package co-design [44] approach where effects of inductance loops and ground return path over exposed Die-Paddle need to be properly taken into account including the interactions with the PCB to meet specifications at application level. Diverse research efforts have been directed towards investigating effects of HVQFN packages on RF performances of sensitive RF blocks such as of Single Pole Double Throw (SPDT) switches [45]-[47]. These studies have motivated the development of packaging solutions such as plastic Small Outline (SO) type of packages operating in the in X-band. In [48], development of a metal ceramic package for Multi-Chip Module (MCM) applications is described, emphasizing effects of the cavity structure frame wall metallization on the performance of the MMICs used in the mm-wave band. Ceramic based packages are also seen attractive for improved thermal performances. In [49], Chip-Package-PCB electrical-thermal co-analysis is proposed to address Power/Signal integrity for MCM applications.

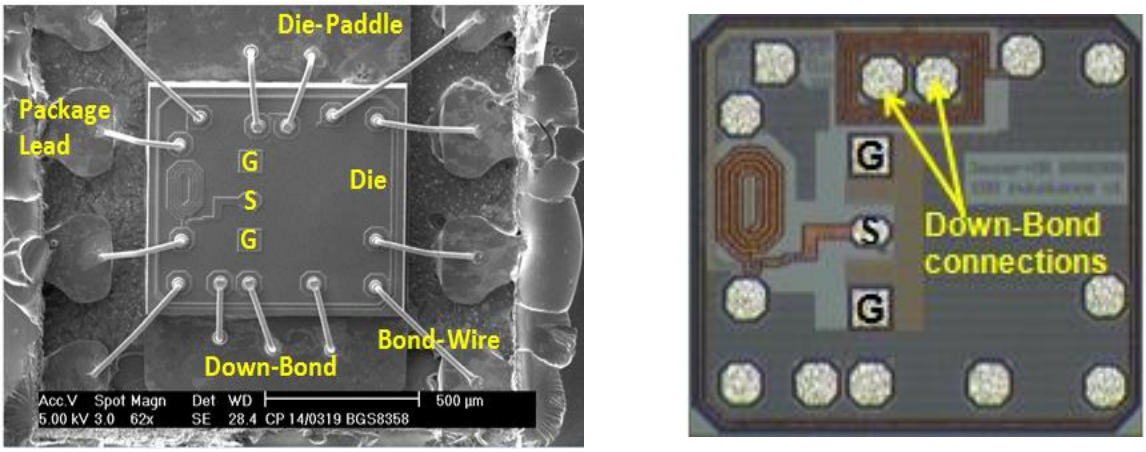
This chapter is devoted to the modeling and analysis of package parasitics resulting from lead capacitance, the self and mutual inductances of bond wires (single wire or wire arrays), and the coupling between chip and package interfaces. Full wave EM simulation and equivalent circuit extractions have been used.

The chapter is built around four main sections:

- The first section describes the chip-package application
- The second section presents in details the advantages and limitations of the EM simulation tools used in this characterization. The RLK extraction technique for a package of many bonding-wires is also described in this section.
- The third section discusses on experiment. After the characterizations of the bond-wires arrays and the vias, the circuit is designed, fabricated, and measured to evaluate different simulation approaches (cascade and global). The effects of die and package are investigated.
- The final section synthesizes the main concluding remarks and design guidelines both for pre-layout and post-layout design phases. Perspectives for further improvements are drawn as well.

IV.2. Description of Chip-Package Application

The Chip-Package application shown in Figure IV-1 consists of an integrated on-chip circuit realized in SiGe BiCMOS technology and packaged using Heatsink Very-thin Quad Flat-pack No-leads (HVQFN) solution. The on-chip circuit is a 5.8 GHz filter consisting of an integrated inductor impressed on the top metal layers and a Metal insulator Metal (MiM) capacitor. The package has 13 bond-wires. The down-bonds, which are defined as bond-wires connected to die paddle, are connections between the integrated inductor and the ground plane. As a result, they add a supplementary inductance to the on-chip circuit. The resonant frequency will decrease. Therefore, the down-bonds need to be accurately designed.



(a) (b)

Figure IV-1: (a) Practical Chip-Package system designed for experimental verification. (b) Photomicrograph of designed and fabricated GSG packaged on-chip filter.

The cross-section of a typical chip in SiGe C: BiCMOS technology is illustrated in Figure IV-2 showing a metal stack (*Multi-Layered Metal including thick metal* connections: 6 to 7 levels), in which an antenna structure can be implemented, on top of a silicon bulk substrate. The multi-layered connections can be used to realize various antenna configurations, including intermediate magnetic conductor optimization. Because bulk substrate can act as a waveguide with undesirable slab modes, via-holes, CO, POLY layers can be useful to suppress spurious modes. The buried BP-Layer: acting as low resistivity lossy conductor may be interesting for antenna grounding. It can be broken by DTI for local high impedance conditions [85].

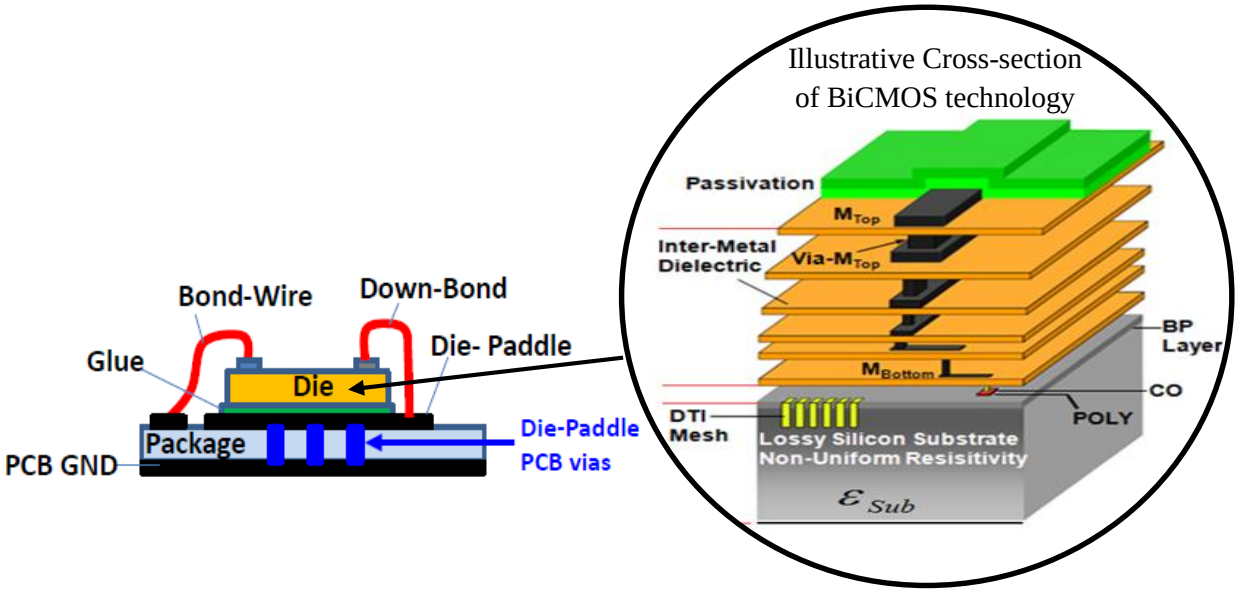


Figure IV-2: Chip-package system with global ground reference at PCB level

In order to characterize the designed on-chip circuit, the following methods have been used:

- Global measurement of the package
- EM Simulation
  - Global (On-chip circuit and package are simulated together by a same simulation tools)
  - Cascade (On-chip circuit and package are separately simulated by different simulation tools)

Table IV-1: Simulation tools

Tools for on-chip circuit simulation	Tool for combination	Tools for Package simulation
Sonnet	Keysight ADS	Keysight EMPro version 2012
Keysight Momentum		Keysight EMPro version 2013
Keysight EMPro version 2012		Keysight Momentum
Keysight EMPro version 2013		Lumped-element model

The advantages and limitations of each approach will be presented in the next sections.

IV.3. Chip-Package Co-simulate methodology

To accelerate the simulation of a complex system, a co-simulation method combines different tools according to application, frequency, fabrication technology, complexity,… We need to choose between:

- Cascade or global approach
- Functional or spatial partitioning method
- 2D, 2.5 D or 3D simulation tool
- Nature of simulation ports

IV.3.1. Cascade and global aproaches

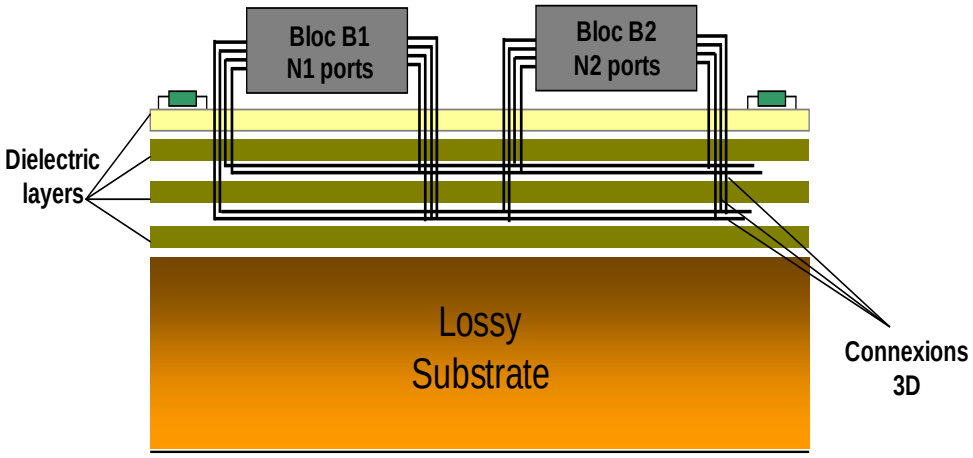
Combining Chip, Package and Board domains requires properly taking into account effects resulting from Power Integrity (PI), Signal Integrity (SI) and Electromagnetic Couplings. In order to meet global system performances, the efficient co-simulation and co-design methodologies presented in [80] - [84] are applied with iterative steps by using the tools from EDA industry leaders.

Among two simulation approaches, global approach, which simulates a system without splitting it, is more rigorous, but more complicate. For a complex package, it takes a lot of time. An alternative approach is called cascade which partitions a complex system into simple parts to simulate. It is quicker and easier to debug. However, the ground references of two simulations can be different because of port definitions. In addition, it does not take into account the mutual coupling between different parts. When the separated results are combined to simulate the complete system, mutual couplings must be add to test bench. However, it is not easy to determine this mutual coupling in particular for a complex structure. Thus the cascade approach takes the assumption that there is no coupling between these parts. These reasons lead to inaccuracy. The advantages and limitations of two approaches are summarized in Table IV-2.

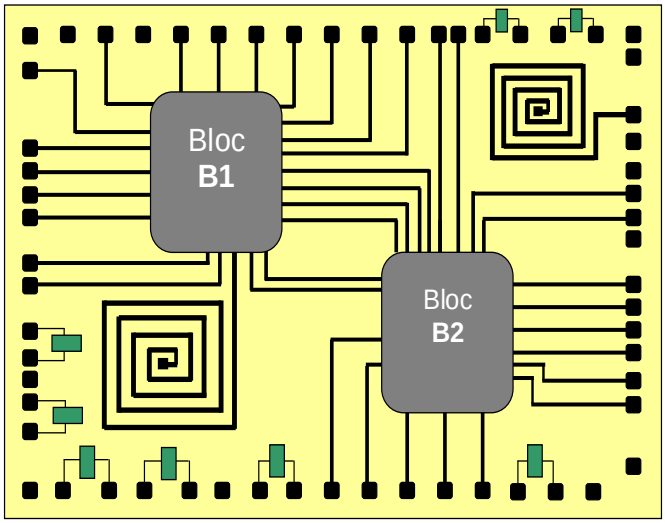
Table IV-2: Limitations of Cascade-based Approaches

Approaches [Methodology]	**Perceived Advantage**	**Perceived Limitations**
Back-End + Package treated as one single model [Global approach]	Coupling between Back-end and Package included in the analysis: more rigorous.	Complexity: requires 3D approach to account for wire shapes and finite die extensions
Back-End + Package treated as 2 separate models [Cascade approach]	Modularity + ease of debugging & tuning + Trade-off accuracy versus complexity, favorable for use of lumped models representations	Coupling between Back-end and Package NOT included in the analysis Requires same ground reference [PCB level] definition of excitation ports

For the cascade approach, a suitable partitioning method is required. The parts in a system can be separated by either their function or their spatial position. In functional partitioning technique, a task can be considered as a block (see Figure IV-3). In contrast, in spatial partitioning method, the parts, which are close to each other, are a block. Because of the simplifying assumption of the cascade approach as mentioned above, the blocs must be chosen so that the mutual coupling between them is as small as possible.



(a)



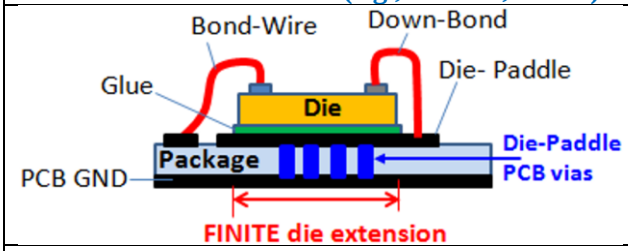
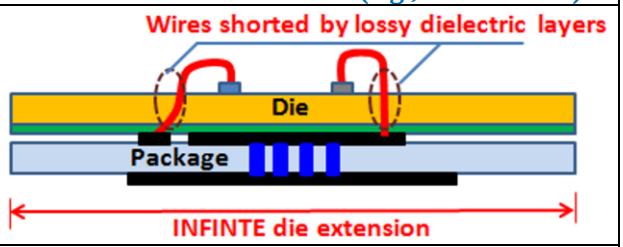
(b)

Figure IV-3: Schematic of a circuit including two function blocks (B1 and B2) integrated. (a) Front view. (b) Top view

IV.3.2. Simulation tools

The EM simulation tools available in the market solve numerically Maxwell's equations by using 2D, 2.5D, or 3D EM solver. 2.5 EM solvers are based on the Method of Momentum (MoM), provided by many vendors such as Designer of Ansoft, Momentum of Keysight, em of Sonnet Software, IE3D of Zeland Software, EMSight of Applied Wave Research, EMPOWER of Eagleware. Whereas, 2D and 3D simulators, such as EMPro of Keysight, HFSS of Ansoft are based on Finite Element Method (FEM). In this thesis, a hybrid approach is generally used which treats the Chip part using 2.5D EM approach (e.g., Momentum) and models the PACKAGE part using 3D EM approach (EMPro or HFSS), both models being combined together at schematic level in Cadence ADE or in ADS. This approach suffers from the simplifying assumption of cascading approach which supposes no coupling between CHIP and PACKAGE.

Table IV-3: Limitations of 2.5D CHIP-PACKAGE EM Global Approach

Global Model in 3D EM (e.g., EMPro, HFSS)	**Global Model in 2.5D EM (e.g., Momentum)**
	
In 3D EM analysis, the following aspects **CAN** be rigorously taken into account: • **FINITE die extension** • **Accurate Bond-wire profiles**	In 2.5D EM analysis, the following aspects **CANNOT** be rigorously taken into account: • **FINITE die extension** • **Accurate Bond-wire profiles**

For the MoM method, all dielectric layers are assumed to have infinite extension following the lateral dimensions. Thus it is not possible to have finite dielectric dimensions in Momentum because of intrinsic limitations in Green's function calculations. Since the silicon substrate has some losses (σ = 0.5S/m) the interference of the bond-wires with the silicon substrate can lead to inaccurate results. However the Momentum approach combining package and back-end in one single model can be optimal. So we need to properly account for the interactions between the CHIP, PACKAGE and PCB. Table IV-3 shows Chip and Package combined in one-single model in Momentum with simplified bond-wire models built using vias and traces. In this unified model ground loops are correctly taken into account.

The ground reference for the EM modeling is assumed to be located at PCB level with via-holes connecting the Die-Paddle to PCB ground as depicted in Fig.III-16. Via-hole connections are kept as short as possible. Extracted ground inductance strongly depends on the number of used via-holes connecting the Die-Paddle to PCB global ground: nominal simulation was done assuming variable number of via-holes (with constant diameter). Distance between Die-Paddle and PCB ground is considered as a design parameter within the limit of few hundreds microns.

Sonnet simulator is also based on 2.5D EM model, but it can define a finite extension for die, package, and PCB stacks. EMPro simulator can describe fully a 3D structure, and simulate it accurately, but with a high CPU time. To combine the simulation results of CHIP and PACKAGE, ADS with a good test bench environment is used. The Table IV-4 summarizes the used EM simulation tools with emphasis on their perceived advantages and limitations.

Table IV-4: Used EM modeling tools: perceived advantages and limitations

Tooling Solution	Perceived Advantage	Perceived Limitation
Momentum	Easy to use in conjunction with ADS and EMPro. Has good editing functionalities for design modification and updates. Has good import/export capabilities for GDS/DXF/Gerber files.	Not possible to define finite extension for die, package and PCB stacks. Cannot account for non-uniformly doped layers (e.g., DTI, Moulding surrounding package). Moulding is in top of package stack. Is based on 2.5D EM model (not fully 3D).
Sonnet	Possibility to use finite extension for die, package and PCB stacks. Macro-models available for non-uniformly doped layers (e.g., DTI, Moulding surrounding package). Has advanced de-embedding features for internal ports calibration.	Is based on 2.5D EM model (not fully 3D). Includes BOX as boundary conditions which can be challenging for parasitic resonances.
EMPro	Full 3D EM model accounting for real Chip-, Package, and PCB layers stack. Can be used for very accurate modeling of critical coupling path. Has good bridging connections to ADS;	Model is very complex to build and CPU time efforts are high: not manageable for complete Chip-package-PCB system. Only specific part of the system can be simulated in a realistic time.
Agilent Keysight ADS	Good test-bench simulation capabilities with advanced tuning options for design optimization.	Dynamic link with Cadence for co-simulation with Die including thermal analysis.

IV.3.3. RLK model extraction for single wire and wire arrays

Figure IV-4 shows the used packaging solution including 13 bond-wires. In assumption that the inductance and the resistance of leads and lead-frame pad are much smaller than the ones of bond-wires, the package can be modeled by BW resistances ***R***, BW self-inductances ***L***, and Coefficients of Coupling ***K*** between BWs. It is called RLK method which models bond-wire *i* by a resistance R_i and an inductance L_i in series, mutual coupling between BWs *i* and *j* by a mutual inductance M_{ij}.

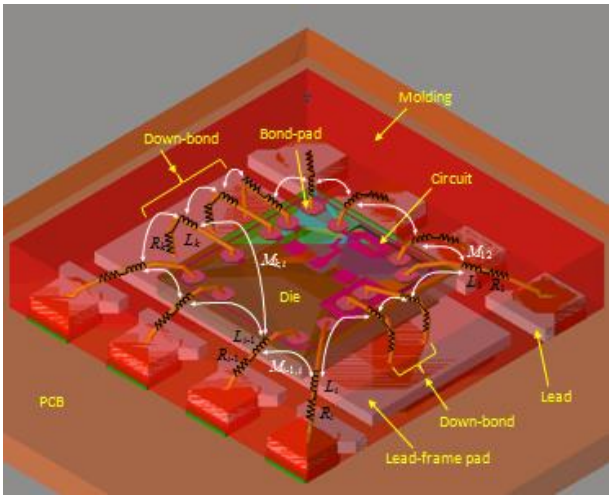


Figure IV-4: RLK model for a package of 13 bond-wires

RLK modeling using *Y* or *Z* parameters is called *Y*-based or *Z*-based respectively. The package is simulated by EM simulators to obtain *S* parameters. Ports are put at the ends of bond-wires. Figure IV-5 shows ports and bond-wires numbering in counterclockwise.

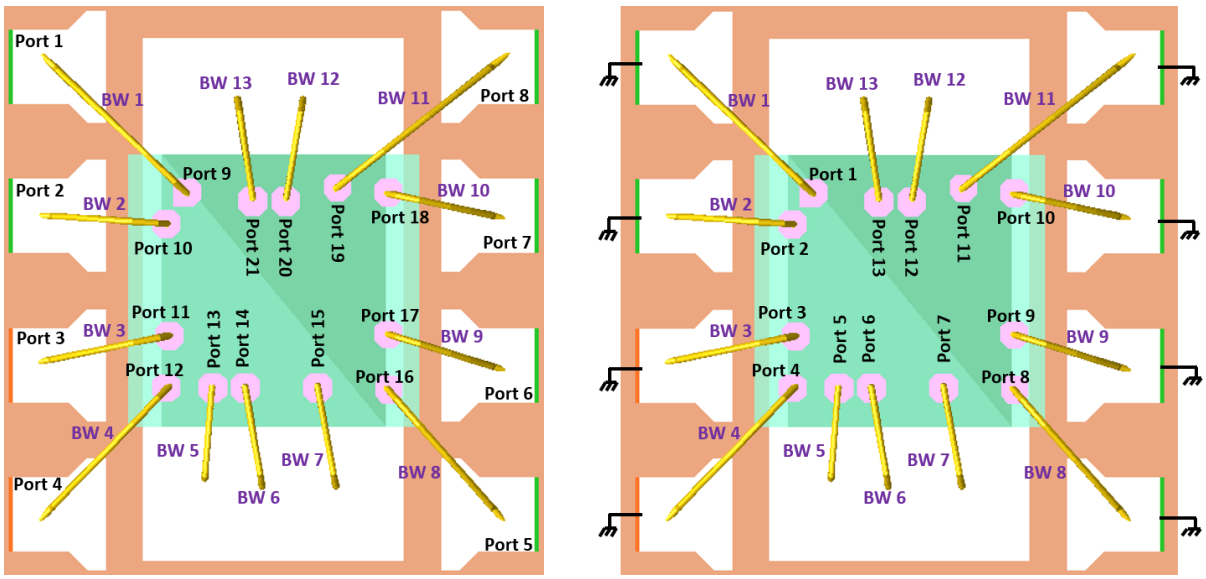


Figure IV-5: Port and bond-wire numbering. (a) Package with all ports. (b) Package with lead-side ports connected to ground.

In order to extract RLK values using *Z* parameters, all the ports on lead-side must be connected to ground. We have a new structure in which port *i* is correspondent to BW *i* (Figure IV-5(b)). Its *Z* parameters can be obtained from EM simulation or by reconstitution from *Z* parameters of the

package shown in Figure IV-5(a) using assistance tools such as Keysight's ADS to minimize simulation time. Figure IV-6 shows a test bench in ADS software for RLK modeling using only EM simulation result of the package in Figure IV-5(a).

We note that superscript [a] and [b] represent the package shown in Figure IV-5(a) and (b) respectively to distinguish *Y* or *Z* parameters of two structures. Resistances, self and mutual inductances are extracted from *Z* parameters of the structure shown in Figure IV-5(b) by using the Eq. (IV-1)-(IV-3).

$$R_i = \text{real}\left(Z^b(i,i)\right), \quad i = 1..\text{BW number} \tag{IV-1}$$

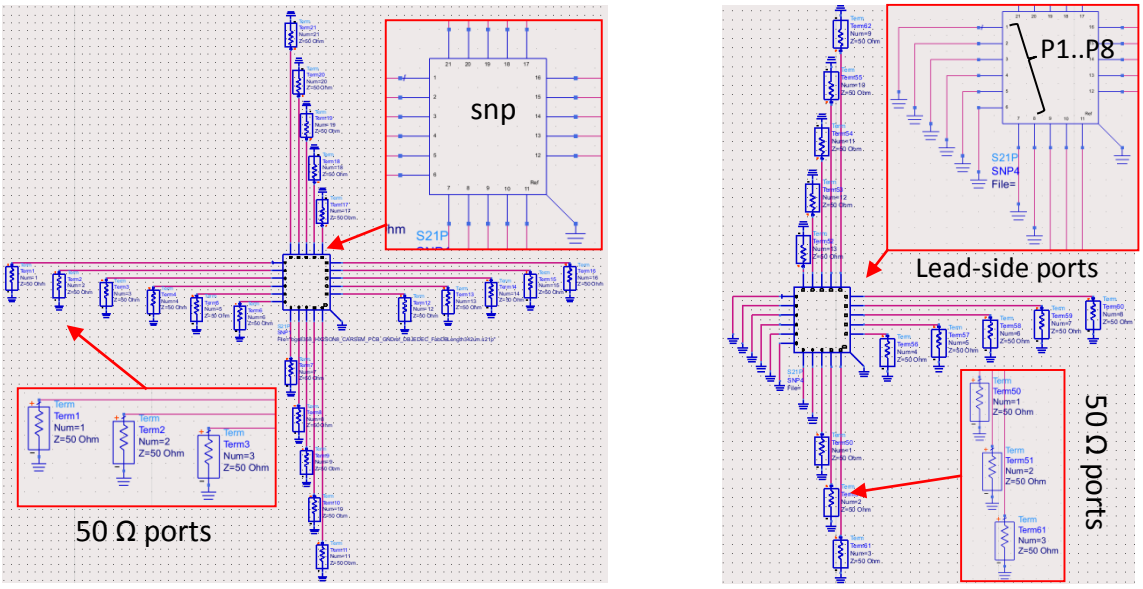
$$L_i = \frac{\text{imag}\left(Z^b(i,i)\right)}{2\pi f}, \quad i = 1..\text{BW number} \tag{IV-2}$$

$$M_{ij} = \frac{\text{imag}\left(Z^b(i,j)\right)}{2\pi f}, \quad i, j = 1..\text{BW number}, \quad i \neq j \tag{IV-3}$$

The above extraction equations are simply summarized in matrix form.

$$L = \frac{\text{imag}\left(Z^b\right)}{2\pi f} \tag{IV-4}$$

$$R = \text{real}\left(Z^b\right) \tag{IV-5}$$



(a) (b)

Figure IV-6: Test bench in ADS. The e-m simulation results are put into the s21p. (a) All ports connected to 50 Ω termination. (b) Lead-side ports connected to ground.

The element at column *i*, row *i* represents self-inductance (Eq. (IV-4)) or resistance (Eq. (IV-5)) of bond-wire *i*. The element at column *i*, row *j* represents mutual-inductance between bond-wires *i* and *j* (Eq. (IV-4)). The coefficients of coupling are determined by

$$k_{ij} = \frac{L(i,j)}{\sqrt{L(i,i)L(j,j)}} \tag{IV-6}$$

Using *Y* parameters to extract RLK values is more complicate. Resistances and self-inductances are determined from *Y* parameters of the structure shown in Figure IV-5(a).

$$R_i = \mathrm{real}\left(-1/Y^{a}(k,h)\right) \tag{IV-7}$$

$$L_i = \frac{\mathrm{imag}\left(-1/Y^{a}(k,h)\right)}{2\pi f} \tag{IV-8}$$

Where ports *k* and *h* are put at two ends of bond-wire *i*.

Meanwhile, mutual inductances are extracted from *Y* parameters of the structure shown in Figure IV-5(b).

$$M_{ij} = \frac{\mathrm{imag}\left(-1/Y^{b}(i,j)\right)}{2\pi f} \tag{IV-9}$$

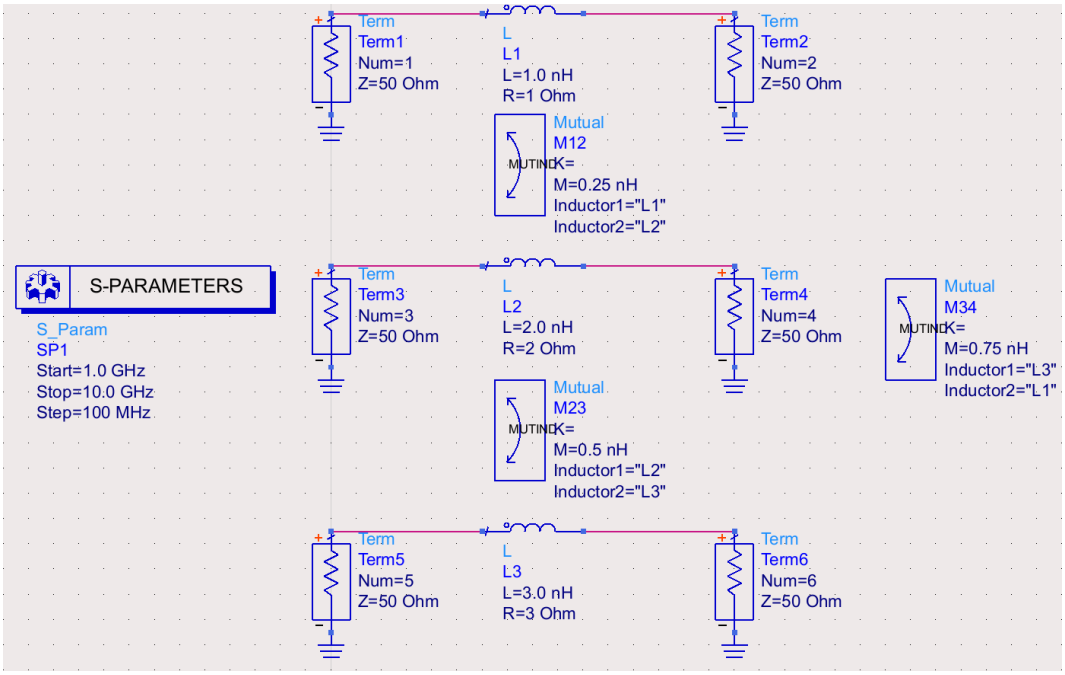


Figure IV-7: Test bench for comparison between Z-based and Y-based RLK methods

A simple structure of 3 inductances to verify two approaches of RLK extraction has been shown in Figure IV-7. The test bench has been simulated from 1 to 10 GHz to get *Y* and *Z* parameters. A comparison between the extracted values at 5.8 GHz has been presented in Table IV-5. The *Z*-based extraction gives correct values in comparison to the ones in the test bench schematic. In contrast, the *Y*-based extraction gives incorrect values with small errors for self-inductances and resistances and big errors for mutual-inductances. Therefore, the *Z*-based RLK method will be used for the next extractions in this thesis.

Table IV-5: Values in the test bench of Figure IV-7, from *Z*-based and *Y*-based extractions.

	L_1 (nH)	L_2 (nH)	L_3 (nH)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	M_{12} (nH)	M_{23} (nH)	M_{31} (nH)
In test bench	1	2	3	1	2	3	0.25	0.5	0.75
Z-based	1	2	3	1	2	3	0.25	0.5	0.75
Y-based	0.8	1.9	2.4	1.18	2.1	3.6	12.3	14.8	3.4

IV.4. Experiment and discussion

IV.4.1. Array of down-bonds

The arrays of one, two, and four bond-wires (BWs) have been realized to study the variation of self-inductance as a function of the number of BWs (Figure IV-9). The used substrate has a relative permittivity of 3.38 and a thickness of 508 μm. The BW structures have been measured from 500 MHz to 50 GHz by a two-port VNA with GSG probes. An SOLT calibration has been performed on an external cal-kit to eliminate the influence of VNA, cables, and RF probes. Then, to remove the input and output accesses from the measurement results, a Thru-Open-Short de-embedding procedure using the algorithm presented in [106] described in Figure IV-8 has been done. $T_{adapter}$, Z_S, and Y_C are calculated from Thru, short, open measurement respectively.

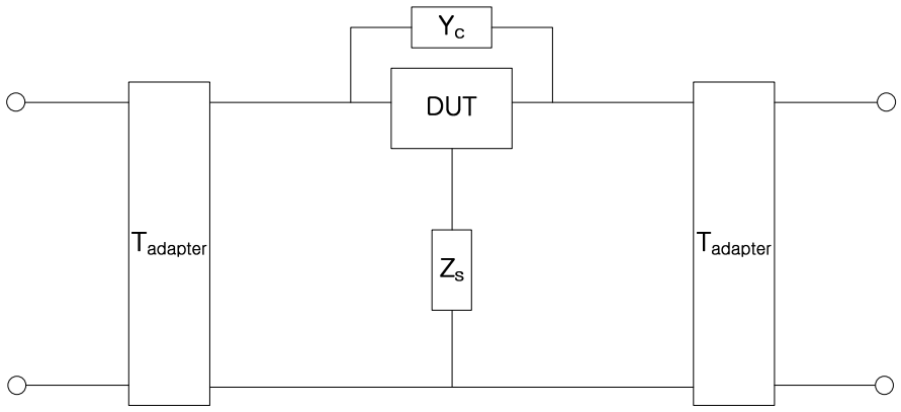
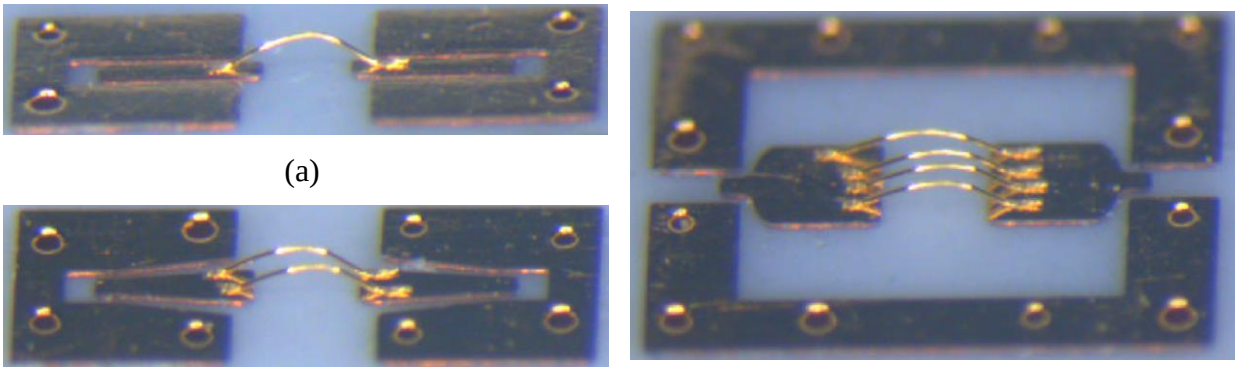


Figure IV-8: Thru-Open-Short de-embedding method [106]

The characterization of down-bond arrays has been done by measurement and EM simulation. Its objectives are:

- To verify the advantages and the limitations of the used simulation tools
- To study the effect on self-inductance and resistance of the number of down-bonds



(a) (b) (c)

Figure IV-9: Realized BW arrays. (a) One BW. (b) Two BWs. (c) Four BWs.

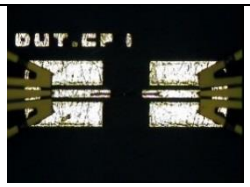
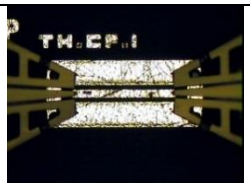
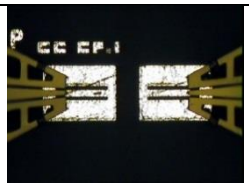
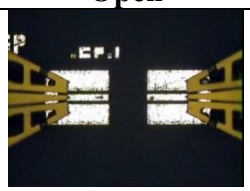
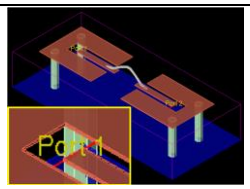
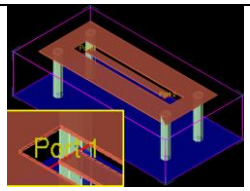
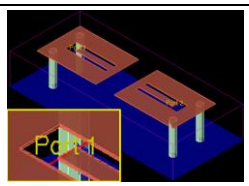
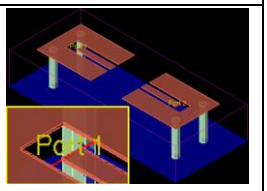
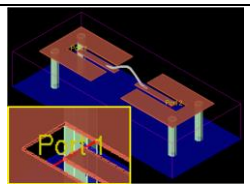
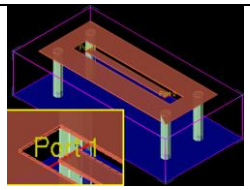
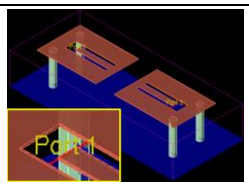
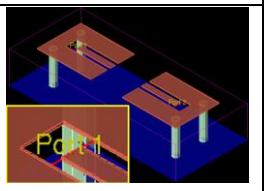
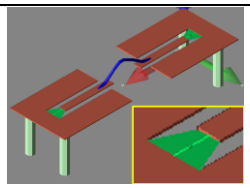
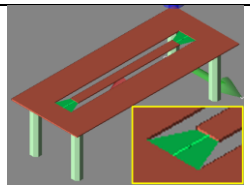
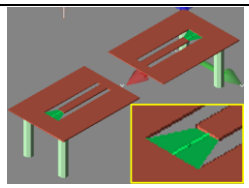
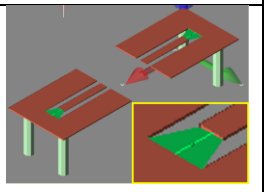
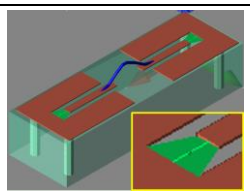
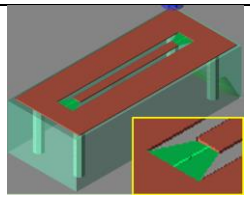
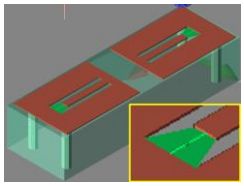
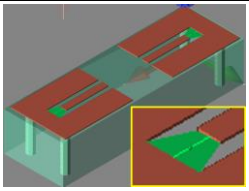
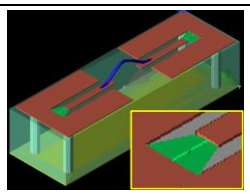
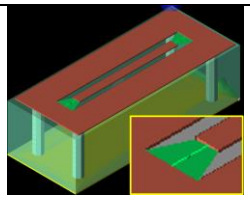
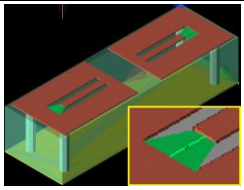
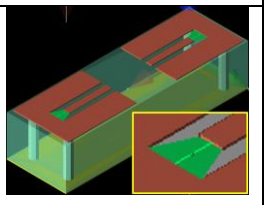
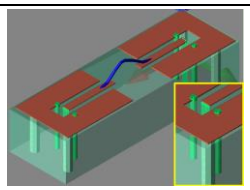
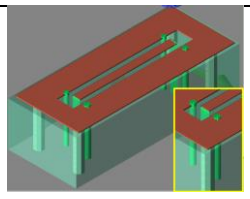
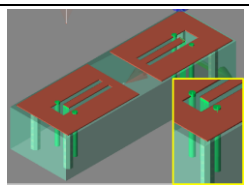
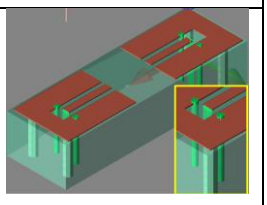
IV.4.1.1. Effect of simulation tools

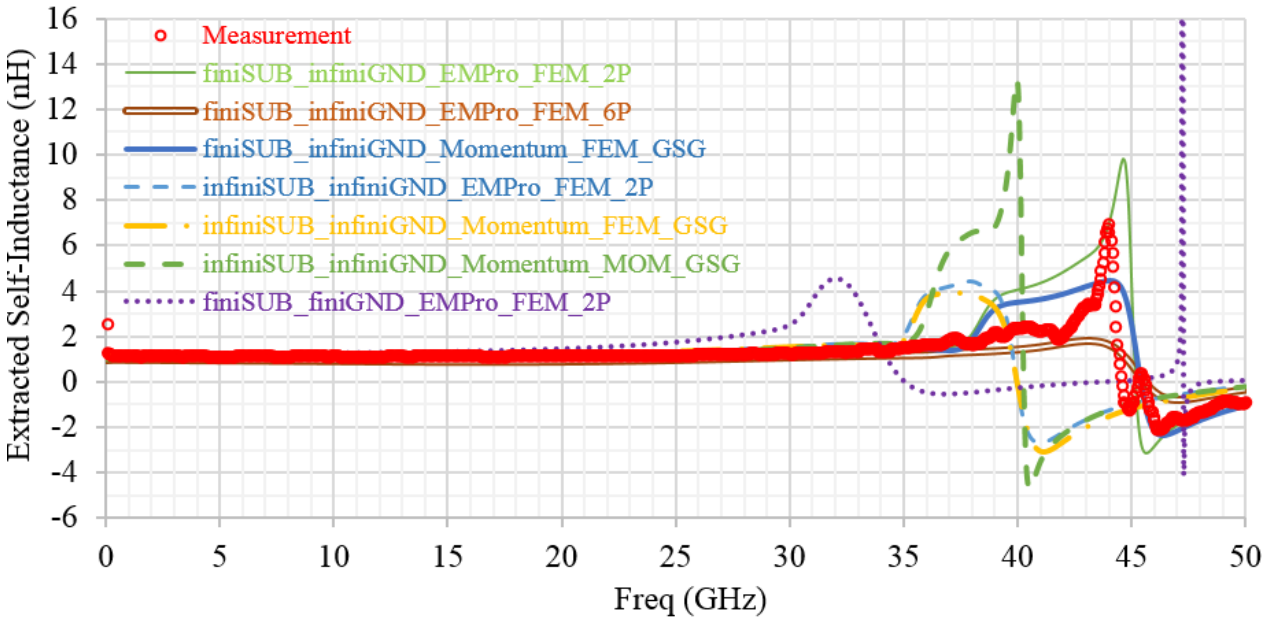
As mentioned above, the accuracy of a simulation is well influenced by EM solver, port definition, cascade or global approach,… In this section, the used simulators (Momentum and EMPro) are evaluated for their advantages and limitations. Momentum provides an easy design environment. The models of these above BW arrays have been designed in Momentum, then they are quickly exported to EMPro. In recent versions, Momentum uses both the method of moment (MoM) and FEM. EMPro uses only FEM method.

Table IV-6 shows all the evaluation options including measurement and simulation for the array of one BW. The following simulation conditions must be identical to measurement:

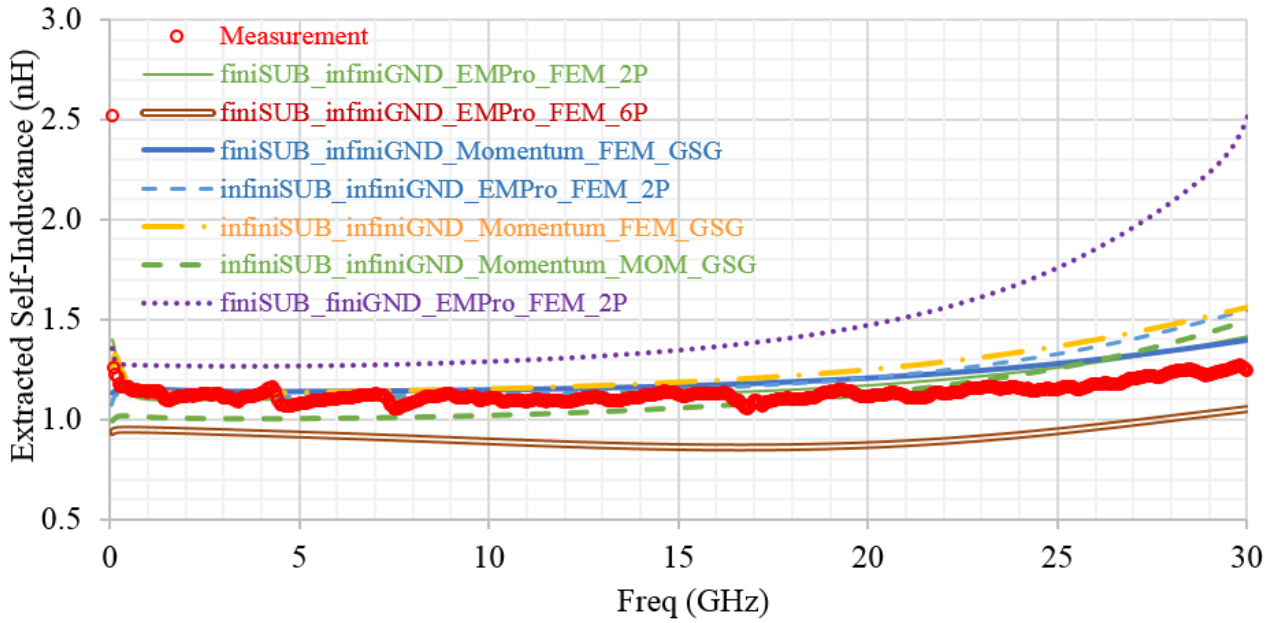
- ❖ In measurement, a Thru-Open-Short de-embedding is done. Therefore, in simulation, it must also be done.
- ❖ Simulation ports must be defined as close as GSG configuration used in measurement. Momentum supports GSG port, but EMPro does not. Therefore, in EMPro, the ports are referenced to the ground on the same plane. Another solution is that one GSG port is defined as three ports. The ports represented by red, and green arrows in Table IV-6 are enlarged.
- ❖ Substrate and ground plane are finite or infinite.

Table IV-6: Measurement and simulations options for the array of one BW

	Dut	Thru	Short	Open
Measurement				
Momentum MoM Infinite substrate Infinite GND GSG port				
Momentum FEM Finite substrate Infinite GND GSG port				
EMPro 2012 FEM 2P Infinite substrate Infinite GND				
EMPro 2012 FEM 2P Finite substrate Infinite GND				
EMPro 2012 FEM 2P Finite substrate Finite GND				
EMPro 2012 FEM 6P Finite substrate Infinite GND				



(a)



(b)

Figure IV-10: Influence of simulators on extracted self-inductance. (a) From 0 to 50 GHz. (b) From 0 to 30 GHz

In Figure IV-10, we can see that at low frequency, the extracted self-inductance has a constant value, but there is a resonance at high frequency. The results can be distinguished by three groups corresponding to three resonant frequencies. The curves which are close to measurement are obtained from the simulations with a finite substrate, an infinite ground, and FEM solver. If the

substrate is infinite, the resonant frequency decreases. In the case of a finite substrate, only one part of the electric field flows through the substrate, the other part flows through air. In the case of an infinite substrate, because the electric field flows totally through the substrate, parasitic capacitance increases. Therefore the resonant frequency decreases.

$$f_{resonance} \cong \frac{1}{2\pi\sqrt{LC}} \qquad \text{(IV-10)}$$

In comparison to an infinite ground plane, a finite one has larger self-inductance. Thus when both the substrate and the ground plane are finite, the resonant frequency decreases also. Only the dimension of the substrate and the ground plane influences the resonance. The port definition does not play an important role.

A further comparison from 0 to 30 GHz in Figure IV-10(b) shows that the simulations are in good agreement with measurement excluding two cases. When both the substrate and the ground plane are finite, the simulated self-inductance (purple dotted line) is larger than the measured value (red line), because the finite ground plane in simulation has a larger self-inductance than the infinite one in measurement. In the other case which defines a GSG port as three ports (brown line), the modified current path has reduced the extracted self-inductance. Consequently, the port definition in EM simulation is very important at low frequency.

IV.4.1.2. Effect of down-bond number

After the verification for the used simulators, the simulation option with a finite substrate, an infinite ground plane, EMPro, the two-port definition has been chosen to study the influence of BW number. Figure IV-11 shows a very good agreement between EMPro simulations and measurements. From 0 to 50 GHz, the extracted value for the one-BW array has a resonance at 45GHz. For the two-BW and four-BW arrays, there is no resonance. Because their self-inductances are smaller than the value of the one-BW array, their resonant frequency is outside of the frequency band from 0 to 50GHz. An approximate function of the self-inductance extracted at 2GHz is presented in Figure IV-11(c) by using the fitting curve technique. The self-inductances extracted at 2GHz are inversely proportional to the number of BWs. The mutual coupling between BWs is very weak in this characterization.

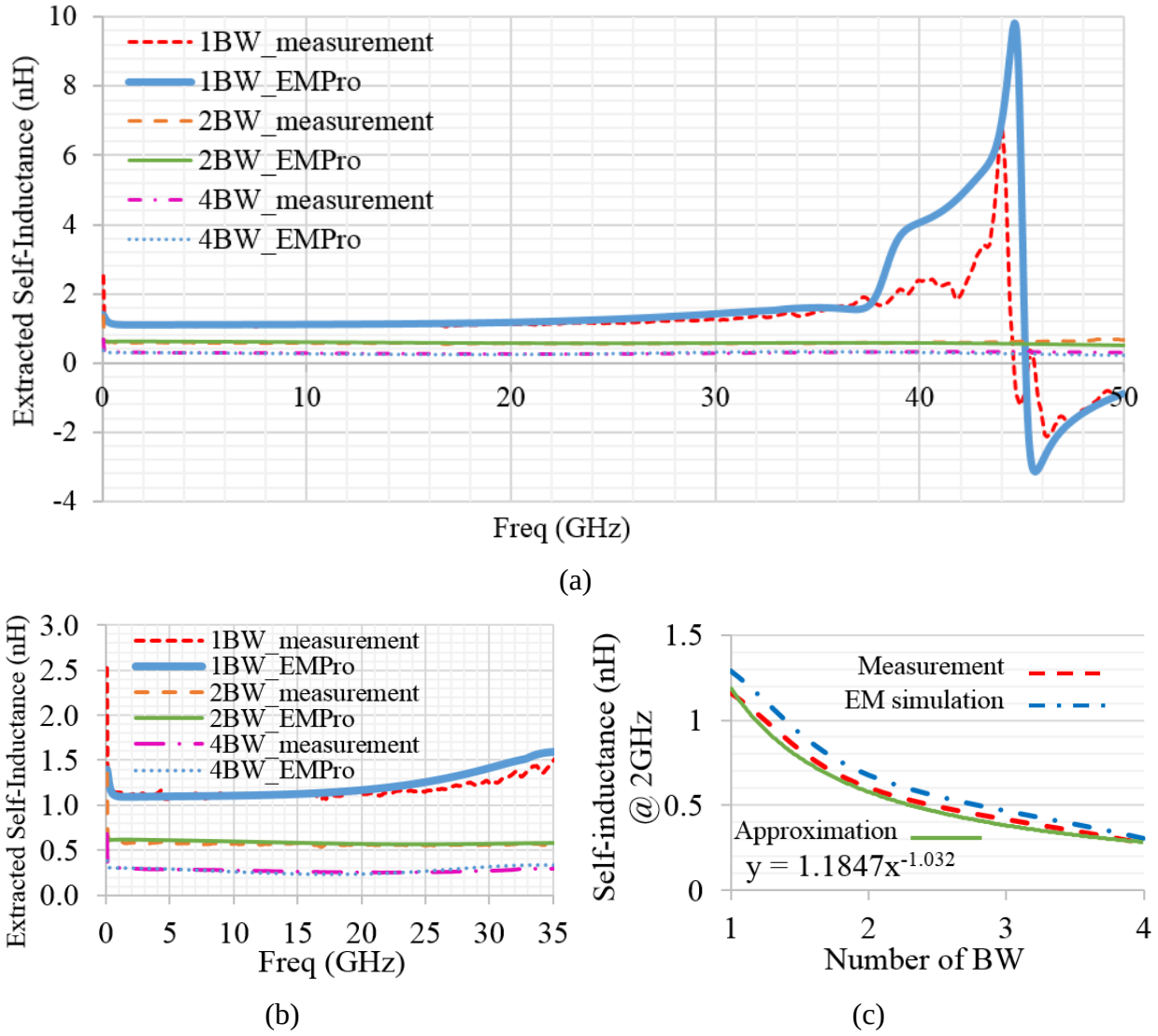


Figure IV-11: Influence of BW number. (a) From 0 to 50 GHz. (b) From 0 to 35 GHz. (c) In function of BW number

IV.4.2. Vias effects

In order to investigate effects of PCB via-hole distribution on ground inductance values, specific test-bench structure is considered to limit effects of parasitic feeding lines on model accuracy. The extraction approach uses a Tee-model architecture for robustness against variations in the feeding line.

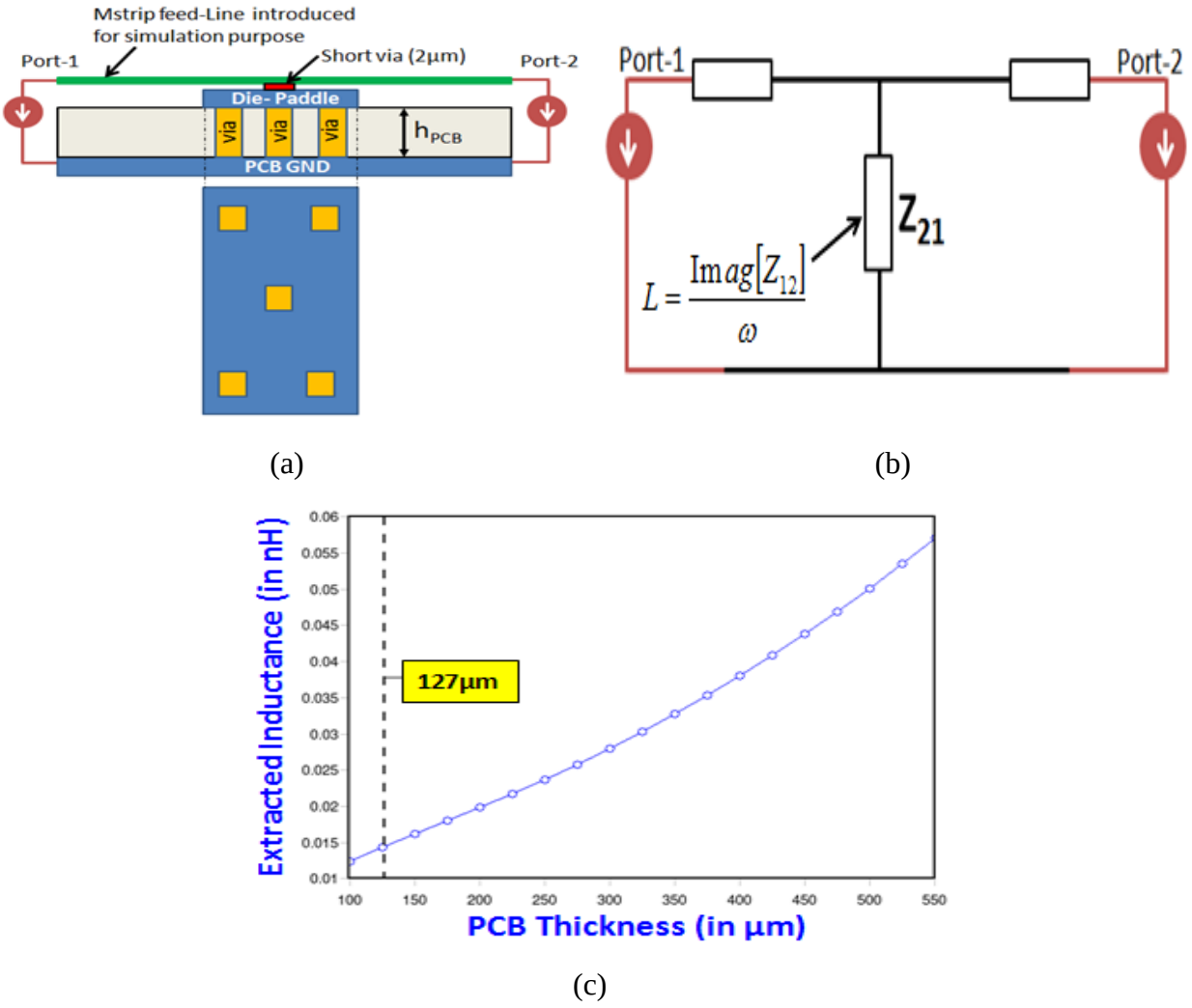
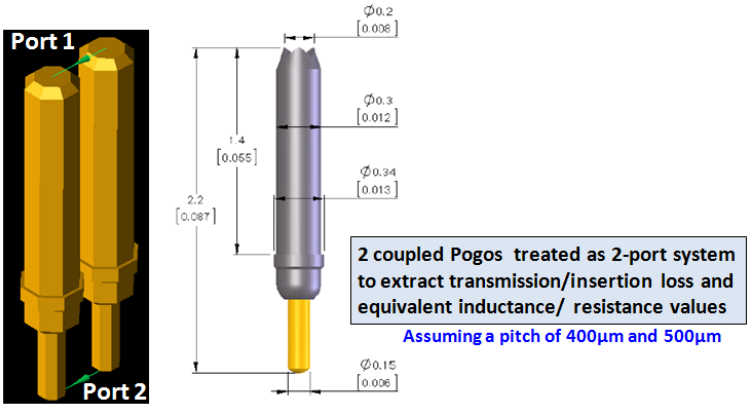


Figure IV-12: Extracted Inductance Value of Die-Paddle to PCB interface as function of PCB Thickness, Tee-model for extraction of ground inductance

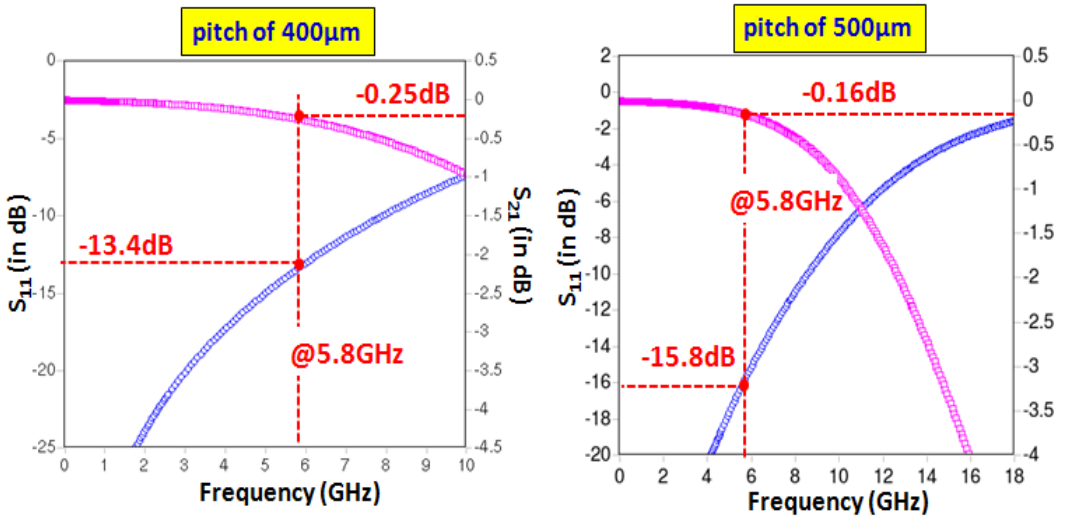
The following values are extracted for the evaluation of PCB vias inductance as a function of the number of vias:

- **L_{gnd}=6.9 pH :for 5 vias connecting Die-Paddle to PCB ground (h_{PCB}=127µm)**
- **L_{gnd}=16.2 pH : for 4 vias connecting Die-Paddle to PCB ground (h_{PCB}=127µm)**

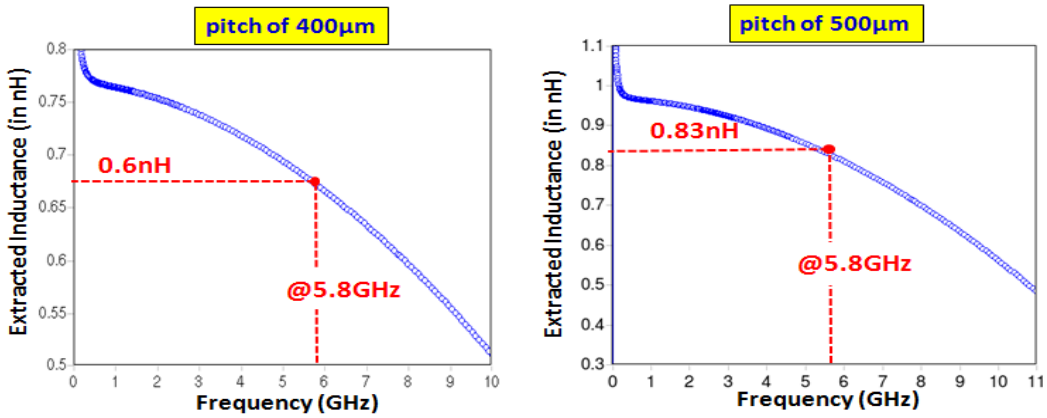
The extracted ground inductances strongly impact the tolerance on acceptable test parasitic inductance resulting from the contacting of the DUT using Pogo systems illustrated in Figure IV-13.



(a)



(b)



(c)

Figure IV-13: Extracted S_{11}, S_{21}, Loss-Factor and inductance values for two coupled Pogos

The following values are extracted from 3D EM simulations:

- **S_{11}=-13.4dB @5.8GHz, S_{21}=-0.25dB @5.8GHz for a pitch of 400µm**
- **S_{11}=-15.8dB @5.8GHz, S_{21}=-0.16dB @5.8GHz for a pitch of 500µm**

Inductance values between 0.65nH and 0.83nH at 5.8 GHz are extracted for pogo contactors with 400µm and 500µm pitch. Extracted inductance values might lead to potential oscillations in critical circuits such as LNA circuits in test-mode.

IV.4.3. Die, package contribution

To characterize the designed on-chip filter, VNA measurement was conducted for frequencies up 50 GHz using conventional ground-signal-ground (GSG) pads micro-probing system with 125µm pitch. The measurement set-up is illustrated in Figure IV-14. SOLT calibration is applied.

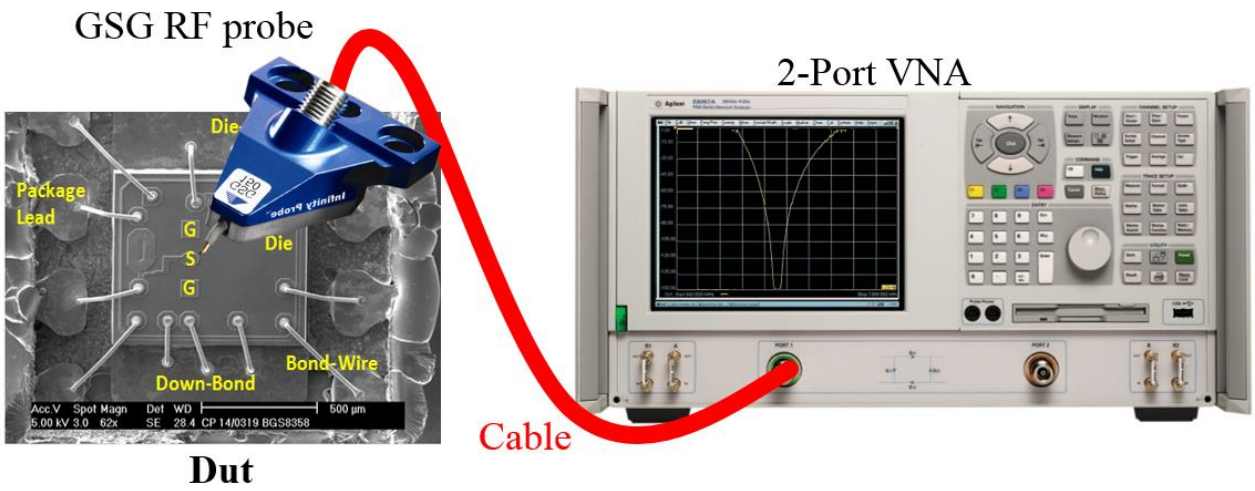
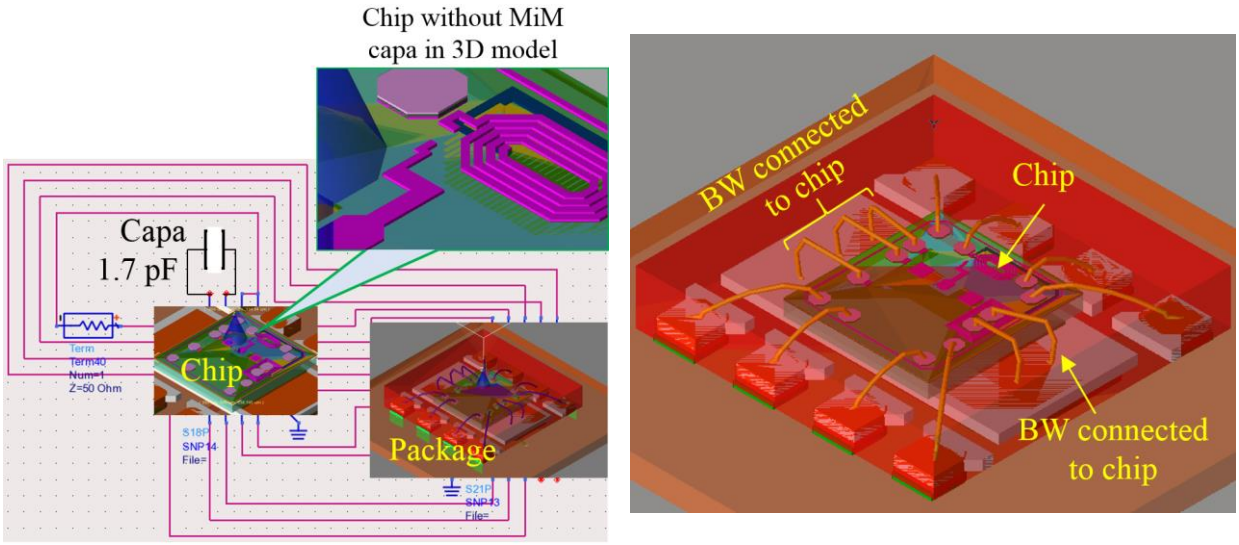


Figure IV-14: Measurement set-up

The chip-package application is also simulated using both 2.5D and 3D simulators, and in both cascade and global approaches. Sonnet simulator which is based on 2.5D solver has been used to replace Momentum because it can simulate a finite substrate. The used 3D solver is EMPro. For the cascade approach, the chip, and the package are separately simulated by different tools. The MiM capacitor is not included in the simulations because it cannot be accurately designed. To resolve this problem, two simulation ports are put at two ends of the MiM capacitor in the simulations. To reconstruct the *S* parameters of the chip-package application, a lumped capacitor of 1.7pF is used as shown in Figure IV-15(a).



(a) (b)

Figure IV-15: Simulation set-up. (a) Cascade approach. (b) Global approach.

Because the results are in the format of one-port S parameters, inductance and resistance are extracted from the imaginary and real part of $Z(1, 1)$ respectively. Table IV-7 reports the following extraction results realized at 5.8GHz which represent the fundamental application frequency:

1) *Die parasitic contribution*
2) *Package parasitic contribution*
3) *Unified Die-Package paretic contribution*

Table IV-7: Extraction of Chip-Package resistive and inductive Parasites: Correlation between Modeling and Measurement

Approach	**Cascade Approach**				**Global approach**	
	Die contribution		***Package contribution***		***Die + Package contribution***	
	R@5.8GHz	L@5.8GHz	R@5.8GHz	L@5.8GHz	R@5.8GHz	L@5.8GHz
Sonnet 2014	13.308 Ω	3.014 nH	3.05 Ω	0.769 nH	12.525 Ω	3.357 nH
EMPro 2013	7.618 Ω	3.198 nH	1.586 Ω	0.459 nH	9.966 Ω	3.698 nH
Measurement					12.376 Ω	3.188 nH

The reported extraction results are realized with shorted series MiM capacitance to properly deduce the series resistance and inductance. The die contribution is extracted from the simulation of die. The package contribution is extracted from the simulation of the package by using RLK extraction method presented in section IV.3.3. In fact, it is the contribution of the down-bonds connected to the chip to make a close current path (Figure IV-15(b)).

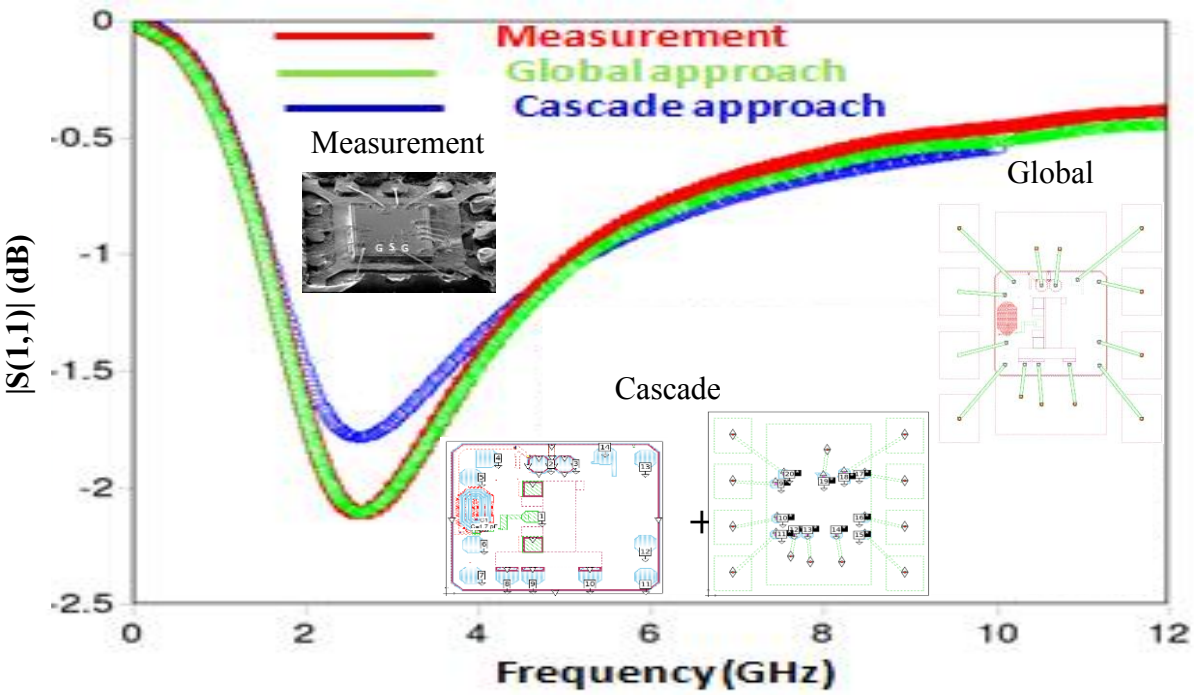


Figure IV-16: comparison between cascade and global model analysis (a), test-bench description (b), Sonnet Chip (c) and package (d) model with internal ports.

Main observations from the obtained results are:

- ✓ The cascaded approach leads to higher losses compared to the global unified solution particularly for Sonnet and EMPro 2012: this clearly shows that the global Chip-Package losses are not a simple addition of Chip and Package losses.
- ✓ The extracted resistance and inductance parasitic contributions at Die and Package levels are very sensitive to used partitioning strategies. Differences up to 30% are observed when comparing the different tools.

Another comparison, in which the package is simulated by EMPro, and Chip is simulated by 2.5D EM sonnet, is shown in Figure IV-17. The simulation results have been modified by changing EM simulator.

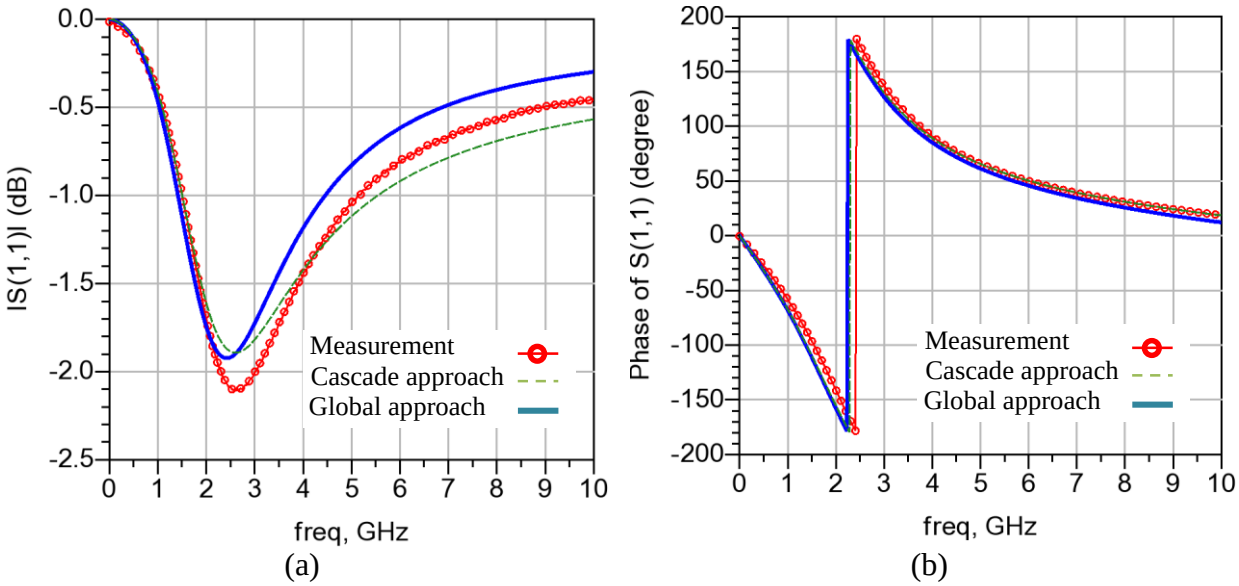


Figure IV-17: comparison between cascade option, global and measurement [package simulated using 3D EM and Chip modeled using 2.5D EM] in terms of magnitude (a) and phase (b).

IV.5. Synthesis, conclusion and perspectives

In this chapter parameterized package model extraction techniques have been proposed and applied to single wire and multi-wire interconnections to derive their RLK parasites. EM modeling simulations using Keysight/Agilent Momentum, EMPro and Sonnet have been presented and compared to measurement data.

Derivation of analytical formulas for the extraction of inductive couplings (self-inductance, mutual inductance) and resistive contributions is proposed for use during Pre-Layout design steps. Experimental verifications highlighting effects of distributed ground references are conducted. The combined effects of extracted self-inductance and resistance values are investigated. The analytical modeling has led to the derivation of geometry-dependent bond-wire models (profile, diameter, material properties). The derived models are implemented as N-Points JEDEC format Wiring-Diagram (WiDi) compatible with Keysight ADS design platform for manufacturability of bond-wire based packages. The generated N-Points JEDEC format Wiring-Diagram (WiDi) is used to extract electrical parameters (self-inductances, mutual inductances, series resistances, mutual capacitances). The electrical models are frequency dependent RLK parameters obtained out of S-parameters from 3D (EMPro) and 2.5D EM solutions (Sonnet, Momentum). The derived scalable models are compared to analytical and to de-embedded measurement data. Both Z (impedance)-based and *Y* (admittance)-based extractions are used and compared showing better accuracy for Z-based extractions.

The proposed extraction techniques are validated by application to dedicated practical structures composed of single wire, coupled wire pairs and wire-array systems. The characterization of the dedicated carrier structures has been used evaluate the accuracy of extracted EM solutions and associated equivalent circuit models. For precise description of the 3D bond-wiring profiles, SEM techniques are used to measure realized bond-wire profiles. Particular emphasis is put on proper Chip-Package partitioning strategies where the interaction between Chip, Package and PCB is assessed by comparing cascade-based approaches to global synthesis.

Ongoing work, drawn as perspectives, concerns the following:

- Generalization of derived geometry-dependent analytical RLCK models to wire-arrays which take into account capacitance extraction
- Extension of proposed applications to Flip-Chip type of packages
- Derivation of guide-lines and design rules for linking extracted RLCK models to S-parameters specification accounting for loading conditions [e.g., linking K-coupling to isolation].

Chapter V

GENERAL CONCLUSION AND PERSPECTIVES

V.1. General conclusion

This thesis focuses on measurement, modeling and simulation of electromagnetic interactions in System-in-Package (SiP), which is a potential packaging technology for semi-conductor industries. SiP integrates in 3D IP cores fabricated by different technologies (CMOS, MEMS, optical, mechanic, thermal…). In the context that the complexity and the signal density in a package increase, the characterization of a package is more complicate, and takes much time. The objectives of this thesis aim to establish measurement, modeling, simulation methodologies in order to reduce time to market for SiP. To evaluate the developed methodologies, the Agile Filter demonstrator of the PARSIMO project and a chip-package application of NXP semi-conductors have been used:

- The Agile Filter (AF) demonstrator is conducted by THALES in cooperation with CONVENTOR, ESIEE, and LaMIPS. It has a band-width from 1 to 18GHz which is divided into eight sub-bands. In order to reduce package surface, four tunable comb-line sub-filters realized on glass substrate have been used. To select the sub-filters, MEMS switches are considered to be integrated in the demonstrator because the MEMS technology owns high isolation up to 100 GHz, near-zero power consumption, and many other advantages in comparison to the competing technologies such as PIN, and FET.
- The chip-package application of NXP semi-conductors is an integrated filter consisting of an inductor and a capacitor. The chip has been realized in SiGe BiCMOS technology and packaged using HVQFN solution. This complex system needs a favorable simulation methodology.

The measurement techniques were developed to meet the requirements of the packaging trends. Firstly, a measurement method in mixed modes is highly demanded not only for differential devices which are progressively used for high-speed circuit, but also for the mutual coupling between interconnections. Because the drawback of the mixed-mode calibrations in the recent publication is very complex, a TRL de-embedding method combined with a calibration algorithm programmed in a VNA is simpler. The method has been evaluated by measurement up to 8GHz. Then, a method of 4-port measure using 2-port VNA is presented due to multi-port VNA is not always available. It has been evaluate by measurement for a branch-line coupler from 20 to 40GHz. The method has been applied for the characterization of the MEMS switches which is required firstly for the AF demonstrator, secondly to study a potential technology for RF package. More than twenty MEMS circuits have been measured through many steps:

- Measurement with PCB, and package
- Measurement with molding part removed
- Measurement with Si cap removed
- Measurement without package (molding + BWs)
- Measurement of response time

The characterization met some difficulties which are generally common in SiP characterization:

- Studying an IP cores in development phase takes much time.
- PCB quality, limited chip surface did not allow measuring all combinations of ports.
- Metal surface did not support for RF probes

The proposed analysis has helped in the diagnosis of the requirements to be met by MEMS switches for the AF demonstrator such as a bandwidth of more than 18GHz, an off-isolation of -15 dB at 18GHz. The conducted diagnosis has defined directions for improvement with inputs formulated to providers.

The next part of the thesis concentrates on modeling methodologies. Firstly, the mutual coupling between two BWs was modeled using geometric dimensions to calculate element values. The BW profile is approximated by Spline functions which give a bridge between EM and mechanic characterizations. The self-inductance of a BW is calculated by using the formula of a straight wire combining with a bonding-wire-geometric-profile-dependent term. The model has been evaluated up to 8.5GHz by using an experimental structure of two BWs realized on a glass substrate. Secondly, two orthogonal crossing lines were modeled by statistic approach, and verified by 3D EM simulation with a good agreement up to 20 GHz. Thirdly, a simple method to trace the path of a return current on a ground plane was described by using 3D EM simulations. The presented technique is useful to simplify a simulation tool developed by SIL, a partner of the project PARSIMO. Finally, a nodal model for six-pole comb-line filter was presented. Behavioral software such as PSPICE cannot read S parameters. The nodal model using simple extraction equation has been evaluated by measurement with a very good agreement. This technique can be extended for a comb-line filter of more than six poles.

The third part of the thesis discusses on the simulation methodology for a complex system. The chip-package application with the effect of parallel BWs number, vias, die and package has been used to verify the method. The accuracy of a simulation depend on many factors such as EM solver (2D, 2.5D, 3D), the nature of ports. The advantages and limitations of different tools (Momentum, ADS, EMPRO and Sonnet) were compared with measurements in the characterization of BW arrays. For precise description of the 3D bond-wiring profiles, SEM techniques are used to measure realized bond-wire profiles.

At high frequency, the simulation results are influenced by the dimension of substrate and ground plane. At low frequency, the nature of ports plays a significant role. The chip-package application has been fabricated, measured, and simulated. Physical characterization of molding compound materials has been conducted leading to broadband extraction of dielectric permittivity and dissipation factor used to assess their influence on RF performances. Particular emphasis is put on proper Chip-Package partitioning strategies where the interaction between Chip, Package and PCB is assessed by comparing cascade-based approaches to global synthesis highlighting importance of Chip-Package-PCB Co-design. The comparison between cascade, global approaches and measurement has shown that cascade approach has more loss than global method.

V.2. Perspectives

This thesis opens to many potential perspectives:

- RF measurement procedure can be quickly performed without experience by using an automatic system. RF probes must be well designed using a protection part to avoid mechanic damages caused by the contacts with DUT. They will be positioned by using coordinates programmed before each test.
- Development of dedicated de-embedding solutions for packages with a number of ports greater than 4.
- Benchmarking state of the art switches in terms of their RF performances based on the initiated de-embedding solutions. Particular attention will be drawn to SOI versus BiCMOS technology solutions using appropriate FOM indicators.
- Generalization of derived geometry-dependent analytical lumped models for wire-arrays accounting for the influence of finite ground planes
  - The geometric-profile-dependent term has been added into the formula of a straight wire to calculate the self-inductance of a curved wire. Because its calculations are still complex, more mathematical works must be done to get a simple approximate function usable by any software, or with a calculator.
  - The approach can be extended for arrays of many BWs.
- The modeling procedure for a complex system is very long, and hard. In addition, there are many device types to model. Therefore, a simple automatic generation of an electric model using the same principle of the presented comb-line model or a neural network will be necessary.
- Use of the results in an automatic 3D placement process which is the aim of the PARSIMO project.
- The link between EM simulation tools and fabrication needs to be developed. The procedure of building BWs in EM simulator, updating BW profile with X-ray photos, exporting geometric dimensions for fabrication is very long and hard because it is manually done. A connection between EM simulators and fabrication will be helpful.
- Extension of proposed applications to Flip-Chip type of packages
- The package extraction method presented in this thesis calculates only resistance *R*, inductance *L*, mutual coefficient *K*. To improve it, capacitance extraction technique will be developed.

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Applications", accepted for oral presentation at the IEEE Radio Frequency Integrated Circuits Symposium (RFIC2015), Phoenix, Arizona, **May 17-19 2015**

LIST OF FIGURES

LIST OF TABLES

LIST OF PUBLICATIONS

Journal

[1] **Dinh, T.V.**; Pagazani, J.; Lesénéchal, D.; Pasquet, D.; Descamps, P.; Lissorgues, G.; Nicole, P., "Bonding-Wire-Geometric-Profile-Dependent Model for Mutual Coupling Between Two Bonding Wires on a Glass Substrate," *Components, Packaging and Manufacturing Technology, IEEE Transactions on* , vol.5, no.1, pp.119,127, **Jan. 2015.**

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[10] **T. V. Dinh**, O. Doussin, D. Lesénéchal, B. Domengès, L. Leyssenne, D. Bajon, D. Pasquet, P. Descamps, and S. Wane, " Modeling and Characterization of Bond-Wire Arrays for Distributed Chip-Package-PCB Co-Design", accepted for poster presentation at The European Microwave Week 2015 (EuMW 2015), **September 6-11, 2015.**

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ABSTRACT

The work of this thesis deals with the modeling and the measurement of electromagnetic interactions in packaged circuits and systems. Reducing "Time to Market" for the design of RF and microwave products necessitates the development of innovative and efficient characterization and modeling methodologies.

Main results concern the following contributions:

- Development of original measurement methods for the characterization of Multiport structures by using 2 Port VNA instruments.
- Elaboration on TRL based deembedding techniques suitable for mixed modes and applicable for Multiport structures
- Application of original design partitioning methodologies accounting for electromagnetic interactions between Chip-Package-PCB integration domains through distributed Co-Design approach

The proposed measurement solutions are applied to the design and the optimization of various circuits including MEMS switches in Multiport configurations used for the realization of an "Agile Filter" demonstrator in the framework of the European project PARSIMO.

Chip-Package-PCB Co-Design methodologies are applied to the design of distributed circuits where the limitations of Cascade approaches are studied in comparison with Full-wave global approaches. The interactions analysis at Chip, Package and PCB levels are efficiently coupled through an optimized partitioning of lumped RLCK model extractions with broad-band S-parameter models issued from simulations EM. Dedicated test structures are developed for the characterization of coupled lines, bond-wire wire arrays and patterned ground planes. Electromagnetic modeling results obtained using commercial 3D and 2.5D tools are compared to broadband experimental data. Analytical and semi-analytical approaches are formulated for the extraction of 3D geometric profiles of package Wiring Diagrams (WiDi) necessary for the manufacturing process.

Key words: EM Interactions, Multi-Port Measurement, Multi-Port Deemebedding, Chip-Package-PCB Co-Simulation, Co-Design

RESUME

Les travaux de cette thèse portent sur la modélisation et la mesure des interactions électromagnétiques dans les circuits et systèmes mis en boitier. Afin de réduire les délais de commercialisation des produits radiofréquences et microondes, le développement de méthodologies innovantes pour une caractérisation et une modélisation efficaces est nécessaire.

Les principaux résultats portent sur les contributions suivantes :

- Développement de méthodes de mesures originales pour la caractérisation de structures Multiport en utilisant des instruments VNA à 2-Port.
- Elaboration de techniques de Deembedding TRL adaptées aux signaux en modes mixtes et applicables aux structures Multiport
- Application de méthodologies de modélisation originales à l'aide de stratégies de partitionnement prenant en compte les interactions électromagnétiques entre les domaines d'intégration Chip-Package-PCB par une approche de Co-Design

Les méthodes de caractérisation proposées sont appliquées à la conception et à l'optimisation de différents circuits incluant des commutateurs (switches) MEMS en configurations Multiport utilisés pour la réalisation d'un démonstrateur de « Filtres Agiles » dans le cadre du projet Européen PARSIMO.

Les méthodologies de Co-Design Chip-Package-PCB appliquées sont mises en œuvre dans la conception de circuits distribués où les limitations des approches Cascade sont étudiées en comparaison avec des approches globales. Le couplage efficace entre les analyses au niveau Chip et au niveau Package/PCB est basé sur une approche de partitionnement optimisée pour combiner les solutions d'extraction RLCK avec les résultats des modèles large-bandes de paramètres S issus des simulations EM. Des structures dédiées sont développées pour la caractérisation de lignes couplées, de fils de soudures et de plan de masses façonnés. Les résultats de modélisation électromagnétiques obtenus avec des outils commerciaux 3D et 2.5D sont comparés aux données expérimentales sur une large bande de fréquences. Des approches analytiques et semi-analytiques sont formulées pour l'extraction de profiles géométriques 3D en vue de la description des diagrammes de connexion WiDi (Wiring Diagramme) nécessaires pour la réalisation des boîtiers.

Mots clés : Interactions EM, Mesures Multi-Port, Deembedding Multi-Port, Co-Simulation Puce-Boitier-PCB, Co-Design