A Systematic Approach to Reliability Assessment of DC-DC Power Electronic Converters

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THÈSE

Pour obtenir le grade de

DOCTEUR DE LA COMMUNAUTE UNIVERSITE GRENOBLE ALPES

préparée dans le cadre d'une cotutelle *entre la Communauté Université Grenoble Alpes* et l'Université de Téhéran

Spécialité : **GENIE ELECTRIQUE**

Arrêté ministériel : 25 mai 2016

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préparée au sein des Laboratoires **Power Electronics and Energy systems** et **Grenoble Génie Electrique**

dans **les Écoles Doctorales School of Electrical and Computer Engineering** et **Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)**

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Thèse soutenue publiquement le **27 mai 2019**,
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Dedication

To my parents and my kind wife for their continuous support and encouragement.

Acknowledgements

Firstly, I would like to express my sincere gratitude to my advisors Dr. Imaneini and Dr. Avenas for the continuous support of my Ph.D study and related research, for their patience, motivation, and immense knowledge. Their guidance helped me in all the time of research and writing of this thesis.

Besides my advisors, I would like to thank the rest of my thesis committee: Prof. Fotuhi Firuzabad, Prof. Bathaee, Prof. Woirgard, Prof. Schanen, Dr. Dupont, Dr. Aminifar, Dr. Shaygani Akmal, for their insightful comments and encouragement, but also for the hard questions which incented me to widen my research from various perspectives.

My sincere thanks also goes to my brother, Majid, for enlightening me the first glance of research and also his firm supporting during this research.

I am thankful to my colleagues Mr. Alexis Derbey, Mr. Benoit Sarrazin and Mr. Florian Dumas who provided expertise that greatly assisted the experimental aspect of our research.

I thank my fellow labmates in for the stimulating discussions, for the sleepless nights we were working together before deadlines, and for all the fun we have had in the last four years.

Last but not the least, I must express my very profound gratitude to my parents and to my spouse for providing me with unfailing support and continuous encouragement throughout my years of study, through the process of researching and writing this thesis and my life in general. This accomplishment would not have been possible without them. Thank you.

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Abbreviations

AERs	Alternative Energy Resources
Al EM	Aluminum Electromigration
Al SM	Aluminum Stress Migration
Al-Caps	Aluminum Electrolytic Capacitors
APC	Accelerated Power Cycling
ATC	Accelerated Thermal Cycling
BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
CTE	Coefficient Of Thermal Expansion
Cu EM	Copper Electromigration
Cu SM	Copper Stress Migration
DBC	Direct Bonded Copper
DCM	Discontinuous Conduction Mode
DFR	Design For Reliability
DUT	Device Under Test
EOP	Electrical Operating Point
ESR	Equivalent Series Resistance
FC	Fuel Cell
FEA	Finite Element Analysis
FEM	Finite Element Method
FEoL	Front End Of Line
FFT	Fast Fourier Transform
FMMEA	Failure Modes, Mechanisms And Effect Analysis
FSR	Fourier Series Representation
GSSA	Generalized State Space Averaging
HEV	Hybrid Electric Vehicle
i-EOP	Interval Electrical Operating Point
IGBT	Insulated Gate Bipolar Transistors
inf	Infimum
i-TOP	Interval Thermal Operating Point
i-ULE	Interval Useful Lifetime Estimation
JEDEC	Joint Electron Devices Engineering Council
KBM	Krylov-Bogoliubov-Mitropolsky
KCL	Kirshohf Current Law
KTL	Kirshoff Thermal Law
KVL	Kirshohf Voltage Law
LTI	Linear Time Invariant
LTV	Linear Time Varying
MLC-Caps	Multi-Layer Ceramic Capacitors

MOSFET	Metal Oxide Field Effect Transistors
MPPF-Caps	Metallized Polypropylene Film Capacitors
NPT	Non-Punch Through
PCB	Printed Circuit Board
PoF	Physics-Of-Failure
PT	Punch Through
PV	Photovoltaic
PWM	Pulse Width Modulation
RADC	Rome Air Development Centre
RBD	Reliability Block Diagram
SAC	Sn-Ag-Cu Based Solder
SAE	Society Of Automotive Engineers
SEM	Scanning Electron Microscope
SSA	State Space Averaging
TDDB	Time-Dependent Dielectric Breakdown
TGFS	Trench Gate field Stop
TIMF	Time Invariant Multi Frequency
TMMC	Time Mode Miller Compensation
TOP	Thermal Operating Point
TSEP	Thermo Sensitive Electrical Parameter
UGFs	Universal Generating Functions
ULE	Useful Lifetime Estimation
WLTP	Worldwide Harmonized Light Vehicles Test Procedure

Notations

$\{\mathbf{A_1}, \mathbf{A}_2, \mathbf{B}_1, \mathbf{B}_2,\}$	System matrices
$\sim N(\mu,\sigma^2)$	Normal distribution with mean value of μ and variance of σ^2
$\sim W(\eta,\beta)$	Weibull distribution of η scale factor and β shape factor
$< X(t)>_T$	Average value of X on switching period
$\Delta T_{heatsink}$	Heat sink temperature swing
A	Coefficient of Coffin-Manson-Arrhenius lifetime model
A_f	Front area of HEV
A_{fin}	Total fin area
A_{plate}	Plates total area
A_{rad}	Total area of radiation heat transfering
B_S	Battery share of power transferring
BV_{CES}	Breakdown voltage
C	Capacitance
c	Time varying trigonometric vector
C_D	Aerodynamic drag coefficient
c_{hs}, s_{hs}, d_{hs}, h_{hs}, w_{hs}, t_{hs}, ℓ_{hs}	Dimensions of heat sink (Fig. 2-16)
$C_{ies}/C_{oes}/C_{res}$	Input/output/reverse capacitances
C_σ	Parasitic capacitance
D	Total damage (chapter 1 and 4, 5)
D	Duty Cycle (chapter 2)
d	Duty cycle state variable
d(t)	Duty cycle command
D_{Cap}	Damage function of capacitor
D_{Diode}	Damage function of diode
D_{IGBT}	Damage function of IGBT
$D_j(t)$	Degradation process of j^{th} ineffective component
E[T]	Mean time to failure
E_a	Activation energy
E_{onD}, E_{offD}	Diode switching energy losses
E_{onQ}, E_{offQ}	IGBT switching energy losses
F	Failure state
f_r	Rolling resistance coefficient
f_{SW}	Switching frequency
g	Gravity
G_i	Threshold value of i^{th} effective component
h	Convective heat transfer coefficient
H_c	Mapping matrix
h_i	Ideal convective heat transfer coefficient

h_{plate}	Convective heat transfer coefficient of plate
i	Inductor voltage state variables
I	Unit matrix
i- ΔT_j	Interval temperature swing
$I_0(.)$, $I_1(.)$	The first and the second terms of Modified Bessel function of the first kind
$i_C(t)$	Capacitor current
I_{Crms}	RMS current of Capacitor
$i_d(t)$	Diode current
I_{Dav}	Diode average current
I_{Drms}	Diode effective current
I_{DUT}	Current of DUT
I_i	Input average current
$i_i(t)$	Converter input current
I_L	Inductor average current
$i_L(t)$	Inductor current
I_{Lrms}	RMS current of Inductor
I_{meas}	Low bias measuring current
$i_o(t)$	Converter output current
I_P	Power current
$i_Q(t)$	IGBT current
I_{Qav}	IGBT average current
I_{Qrms}	IGBT effective current
i-T_j	Interval junction temperature
K	Coefficient of thermal resistance variation (equation (3-4))
k	Total number of effective items
$k_0(.)$, $k_1(.)$	The first and the second terms of Modified Bessel function of the second kind
$k_{air`}$	Air conductivity
K_B	Boltzmann's constant (8.62×10^{-5} ev/K)
k_{hs}	Heat sink thermal conductivity
k_i	Integral coefficient of PI controller
K_{ID}	Diode current dependency on switching energy losses
K_{IQ}	IGBT current dependency on switching energy losses
k_p	Proportional coefficient of PI controller
K_{VD}	Diode voltage dependency on switching energy losses
K_{VQ}	IGBT voltage dependency on switching energy losses
L	Inductance
ℓ	Total number of ineffective items
L and L_0	Useful lifetimes under the use condition and testing condition

L_σ	Stray inductance
M	Mass of the vehicle (Mission Profile)
M	Global system degradation states (Multistate degraded system)
M_I	Output/input converter current ratio
M_i	Degradation states of i^{th} effective component
M_v	Output/input converter voltage ratio
n	Number of distinct cycles which power semiconductors are subjected to in Palmgren–Miner's rule
n	Voltage stress exponent in capacitor lifetime model
N	Order of Fourier series
N_F	Number of cycles to failure in Coffin-Manson-Arrhenius lifetime model
N_{Fi}	Number of cycles to failure of the i^{th} particular cycle in Palmgren–Miner's rule
n_{fin}	Number of fins
N_i	Number of the i^{th} particular cycle in Palmgren–Miner's rule
Nu_b	Nusselt number
Nu_{dev}	Nusselt number for developing region
Nu_{fd}	Nusselt number for fully developed region
Nu_i	Ideal Nusselt number
$Nu_{laminar}$	Nusselt number of laminar region in the external plates
Nu_{plate}	Nusselt number of plates
$Nu_{Turbulent}$	Nusselt number of turbulent region in the external plates
P(.)	Probability function
P_{aux}	Auxiliary equipment power
P_b	Blocking power loss
P_{conv}	Power converter
$P_{CQ/CD}$	IGBT/Diode conduction power loss
P_{DUT}	Power of DUT
P_G	Gate driving power loss
P_i	Intermediate degradation state of i^{th} effective component
P_{Loss}^{Diode}	Diode total power loss
P_{Loss}^{IGBT}	IGBT total power loss
P_{Loss}^{rC}	Capacitor internal power loss
P_{Loss}^{rL}	Inductor internal power loss
P_{max}	Pointer showing the length of $\mathbf{S_{max}}$
P_{min}	Pointer showing the length of $\mathbf{S_{min}}$
P_o	Output power
Pr	Prandtl number
P_{SW}	Switching power loss

Q	Internal energy
$\mathbf{q}$	Switching function state variables
$q(t)$	Switching function
$q_{conv\text{-}fin}$	Fins convective heat transfer
$q_{conv\text{-}plate}$	Plate convective heat transfer
q_{rad}	Radiation heat transfer
Q_{rr}	Reverse recovery charge of Diode
R	Load resistance
$\mathbb{R}$	Mapping range
$R(t)$	Global system reliability function
R^{*}_{eb}	Channel Reynolds number
Ra	Rayleigh number
r_C	Capacitor resistance
r_D	Diode internal resistance
$R_{DS\text{-}on}$	Drain to Source on-state resistance
R_{eb}	Reynolds number
R_g	Gas constant (8.314 $jmol^{-1}.K^{-1}$)
R_g	Gate driving resistance
$R_{Global\text{-}series}(t)$	Global reliability function of a series system
$R_i(t)$	i^{th} subset of Global system reliability function
r_L	Inductor equivalent series resistance
r_Q	IGBT internal resistance
$R_{th(c\text{-}h)}$	Thermal resistance from case to heat sink
$R_{th(h\text{-}a)}$	Thermal resistance from heat sink to ambient
$R_{th(j\text{-}c)}^{Diode}$	Thermal resistance from Diode junction to case
$R_{th(j\text{-}c)}^{IGBT}$	Thermal resistance from IGBT junction to case
$R_{th\text{-}base}$	Thermal resistance of heat sink base
$R_{th\text{-}fin}$	Thermal resistance of fins
$R_{th\text{-}i}$	i^{th} thermal resistance in Foster thermal model
$R_{th\text{-}plate}$	Equivalent thermal resistance of plates
$R_{th\text{-}rad\text{-}plate}$	Thermal radiation resistance
$R_{th\text{-}spread}$	Spreading thermal resistance
$R_x(t)$	Reliability function of x^{th} item in a series system
S_j	Threshold value of j^{th} ineffective component
$\mathbf{S_{max}}$	Flexible buffer for maxima
$\mathbf{S_{min}}$	Flexible buffer for minima
$\mathbf{T}$	Input temperature vector
$\mathbf{t}$	Input time vector corresponding to $\mathbf{T}$
T and T_0	Temperature in Kelvin at use condition and test condition
T_a	Ambient temperature
T_{base}	Base temperature

t_c	Creep time
TC_{Err}	Reverse recovery energy temperature coefficient
TC_{Ets}	Switching energy temperature coefficient
TC_{rD}	Diode resistance temperature coefficient
TC_{rQ}	IGBT resistance temperature coefficient
TC_{VD}	Diode voltage temperature coefficient
TC_{VQ}	IGBT voltage temperature coefficient
T^e_{mean}	Equivalent mean temperature
t_{FC}	Full cycle time
t_h	High time in switching function
T_h	Heat sink temperature
T_j^{Diode}	Diode junction temperature
T_j^{IGBT}	IGBT junction temperature
T_{jmax}	Maximum junction temperature
T_{jmin}	Minimum junction temperature
t_ℓ	Low time in switching function
T_m	Mean junction temperature
T_S	Switching period
$\mathbf{u}(t)$	Input vector
$\mathbf{v}$	Capacitor voltage state variables
V	HEV speed
V and V_0	Voltage at use condition and test condition
$v_c(t)$	Capacitor voltage
V_{CE}	Collector Emitter voltage
$V_{ce,on}$	On-state collector-emitter voltage
$V_{ce,on-}$	Nagetive component of on-state collector-emitter voltage
$V_{ce,on+}$	Positive component of on-state collector-emitter voltage
V_{CE0}	Collector-emitter saturation voltage
$V_{contact}$	Electrical contact resistance voltage drop in MOSFET-BJT model of IGBT
V_D	Diode voltage
V_{D0}	Diode forward saturation voltage
V_{DUT}	Voltage of DUT
V_g	Gate-Emitter voltage
$V_{G\text{-}TH}$	Gate threshold voltage
V_i	Input average voltage
$v_i(t)$	Input voltage
$v_L(t)$	Inductor voltage
V_{MOS}	MOSFET region voltage drop in MOSFET-BJT model of IGBT
V_{NB}	Drift region voltage drop in MOSFET-BJT model of IGBT
V_o	Output average voltage

$v_o(t)$	Output voltage
V_{on}	On-state voltage of the power semiconductors
V_{pn}	p^+-n^- junction voltage in MOSFET-BJT model of IGBT
V_{ref}	Reference voltage
W_{Mi}	Threshold value of state M in i^{th} component
$\mathbf{x}$	State variables (in FSR representation)
$\mathbf{x}(t)$	State vector
$\bar{\mathbf{x}}(\mathbf{t})$	Average state vector
$\underline{X}$	Minimum value of parameter X
$\overline{X}$	Maximum value of parameter X
$x(t)$	FSR of x(t)
$x_0(t)$	Time dependent zero component of FSR of x(t)
$X_{fully\text{-}degraded}$	Fully degraded component
X_{new}	New component
$x_{\alpha n}(t)$	n^{th} even component of FSR of x(t)
$x_{\beta n}(t)$	n^{th} odd component of FSR of x(t)
$Y_i(t)$	Degradation processes of i^{th} effective component
Z_{Diode}	Diode thermal impedance
$Z_{Diode\text{-}IGBT}$	Cross coupling thermal impedance of IGBT on diode
Z_{IGBT}	IGBT thermal impedance
$Z_{IGBT\text{-}Diode}$	Cross coupling thermal impedance of diode on IGBT
Z_{th}	Thermal impedance
α	Exponent of Coffin-Manson-Arrhenius lifetime model
β_{air}	Air density
Γ	Characteristics length
γ	Ratio of total heat sources surface and the heat sink base area
δ	Mass factor
Δi_L	Inductor current ripple
Δt	Creep dwelling time
ΔT_j	Junction temperature swing
Δv_C	Capacitor voltage ripple
ε_{rad}	Emissivity of Heat sink
η	Converter efficiency
η_{fin}	Fin efficiency
η_t	Total efficiency of transmission system and electric motor
λ	Failure rate
$\lambda(t)$	Time varying failure rate
ν_{air}	Air viscosity
ρ_a	Air density

σ	Mechanical stress (Chapter 1) Boltzmann constant ($5.669\times10^{-8}W/m^2k^4$) (Chapter 2)
τ_i	i^{th} thermal time constant in Foster thermal model
Φ	Cumulative normal distribution function
$\boldsymbol{\Omega}$	Derivative matrix of $\mathbf{c}$ ($d\mathbf{c}/dt=-\mathbf{c}\,\boldsymbol{\Omega}$)
$\boldsymbol{\Omega}$	Modified Global system state space (Chapter 5)
$\boldsymbol{\Omega_i}$	i^{th} effective component state space
ω_S	Angular switching frequency
$\boldsymbol{\Omega_U}$	Global system state space

Introduction

On a global scale, burning of fossil fuels for supplying power are causing irreparable damage to our environment and disturbing the ecological balance. It is not possible to continue in this way without there being dire consequences. Therefore, developing alternative energy resources and full and hybrid electric vehicles (HEV) seems to be essential. Renewable energies can make a real difference as a golden opportunity. Due to the uncertain inherent of renewable energy resources, power conditioners are required for supplying the demanded power. Researchers are pushing back the frontiers of knowledge of power converters every day. Harnessing of technology in all sort of creative ways for designing reliable power converters grasps the importance. New cutting-edge design of power converters is transforming our visions from narrow-minded design to the reliable design of power converters. Importance of reliability of power converters is a widespread belief for long-term investment and stimulating the investors.

Reliability of power electronic converters plays a central role in persuading the investors and general users since renewable energy resources and other related issues have the lion's share in supplying power demands. We also take the view that reliability assessment of a power converter is contributing factor in its design. Keen interests have been paid to the reliability of the power electronic converters either in component-level or in system-level.

Among all the power electronic converters, DC-DC power converters make a meaningful contribution in transferring and smoothing electrical power. Abundance use of DC-DC power electronic converters is a compelling reason for its importance as a reliability point of view. Several frameworks have been established for reliability assessment of DC-DC power converters and also a heated debate has been sparked off for DC-DC power converters reliability evaluation. The new reliability discipline focusing on mathematical or physical reliability assessments have been widely applied to the power converters. However, each of them has their own pros and cons. Those who support the claim of mathematical reliability evaluation advocate that this method is capable of assessing system-level reliability. On the other sides, some researchers who have taken the position of physical reliability

assessment have laid emphasize on its capability of considering the failure mechanisms and mission profiles.

In mathematical approach (called also as structural approach), collected reliability data in the specified field has been utilized. Despite its wrong basic assumption, namely an exponential distribution of failures, reliability hand books have become the almost exclusive prediction method for the reliability of electronic systems. Mathematical approach is capable of assessing reliability either in a component- or in a system-level employing some stochastic processes. This means that if a power electronic converter can roughly-appropriate works under a local failure occurrence, the method is still able to assess the reliability. The weakness point of this kind of reliability assessment is the absence of mission profile consideration such as temperature cycles and operational cycles. In addition, degradation and wearing out of one component on itself and on the other critical components is not taken into account leading to much more optimistic reliability assessment.

Physical approach or physics-of-failure (PoF) based approach is based on the knowledge of failure mechanisms by which the considered components and systems are failing. This method requires the knowledge of deterministic sciences and probabilistic variation theories. Consideration of the mission profile including both environmental and operational factors is one of the notable points of physical reliability assessment leading to much more realistic reliability estimation of a component. In addition, the wearing out of a component is also taken into account. However, in addition to its high cost and being time consuming, the detriment of this method as well as mathematical approach is the lack of consideration of mutual and self-degradation effects on itself and each other. The weakest point of this method is that it is restricted to the only component-level or multi component-level reliability assessment. Although, this method can deal with the simple reliability constructions such as series, parallel and k-out-of-n systems (multi component-level), it is not suitable for reliability evaluation of redundant system such as interleaved power converters. Because in the redundant systems, by changing the configuration of the system, operating conditions of the power converter would be varied leading to different damage models.

Thesis objectives and contribution

Lack of consideration of the dependencies (self- and mutual degradation effects) of the power converter's components in both approaches, lack of consideration of the mission profile in mathematical approach and inability of tackling system-level reliability evaluation in physical approach as well shape our thinking to provide a rationale to meet the above mentioned challenges. The thrust of our argument is to merge all the advantages of both approaches by developing a physical reliability assessment approach.

By time passing, it is clear that the degradation process of a component or a system might be accelerated owing to the aging. Accordingly, static reliability assessment has not been able to estimate the reliability of a system and some dynamic reliability assessments seem to be required. For mitigating the problems of system-level reliability assessment, consideration of self and mutual degradation effects (dependencies), degradation levels (states) and consideration of mission profile, a new method has to be put forward.

The objectives of this thesis are to integrate the pros of both mathematical and physical methods and also tackling their detriments. In the proposed method, mission profile of undertaken system has been considered and applied to a multistate degraded system. This approach tries to consider the dependencies between the power components by defining a finite number of states for the global system. In the other word, this method converts a dependent system to a multi-state independent system by discretizing the global system states to the specific state space. In each state of the global system, detached operating conditions are assumed. Accordingly, in addition to the aforementioned challenges, this method is capable of analyzing time-varying failure rate.

Thesis framework and limitations

Two different reliability assessment frameworks will be proposed in this thesis for tackling abovementioned detriments. The first one is interval reliability analysis. By using interval reliability analysis instead of an inaccurate value for reliability, one can find an interval for the reliability of power electronic converters. Degraded and new states of the global system (power electronic converters) both are considered in this approach. The second approach is multi state degraded reliability assessment and defining a finite number of states in the global system to consider dependencies.

As a case study, a conventional DC-DC boost converter is taken into account as an interface between a battery bank and a motor driver in HEV. A customized 3000W 200V/400V setup was implemented for validating the effects of degradations (dependencies) in the power electronic systems. Based on the literature review, the two most critical components in the power electronic converters are power semiconductors and power capacitors. It has to be mentioned that the customized DC-DC boost converter consists of an IGBT and a power diode as power semiconductors.

Employing the customized conventional DC-DC boost converter, we were able to observe the effects of self- and mutual degradations of the components on each other. Accordingly, the first challenge, namely dependencies, has grasped the importance. For providing aged devices (power semiconductors), an accelerated thermal cycling (ATC) aging test was performed.

For validating the new frameworks, i.e. interval reliability assessment and multi state degraded system, some aging information was extracted from an accelerated power cycling (APC) aging test. Regarding to the time limitation, the main focus of aging have been zoomed on the power semiconductor aging tests and power capacitors' data has been extracted from literature reviews.

Thesis organization

Chapter one deals with the literature review and fundamental theories of conventional approaches. In this chapter the failure mechanisms of the critical power components and their correlations in their lifetime models have been discussed. Chapter two expresses electrical, thermal and power loss modeling of DC-DC boost power converter. In this chapter, time invariant multi frequency (TIMF) modeling capable of evaluating states' ripples has been investigated. Iterative power loss calculation is also expressed. The chapter is ending with the forced convection heat sink design and expressing a complete dynamic thermal modeling. While, chapter three deals with the experimental procedure and their results including thermo sensitive electrical parameter (TSEP) tests, customized DC-DC boost power converter, accelerated power cycling aging test, accelerated thermal cycling aging test, scanning electron microscope (SEM) and 3D X-ray tomography microscope, a newly proposed cycle counting algorithm capable of considering time-temperature mean value and creep-fatigue failure mechanism is launched in chapter four. Chapter five is expressing the reliability assessment of 3000W 200V/400V DC-DC boost power converter as an interface power conditioner in an HEV exposing to worldwide harmonized light vehicles test procedure (WLTP) driving cycle. The reliability assessment falls into three categories, namely conventional physical approach, interval reliability analysis and multi state degraded reliability assessment, in this chapter. Finally, a conclusion and summary is drawn in the last chapter.

1

Literature review

1-1 Introduction

There is undoubtedly no dispute in the importance and necessity of the reliability of an item. Small wonder, then, that general users lay emphasize on how reliable products they utilize. In addition, some organizations such as military systems and airline companies are fully aware of the costs of their unreliable products and try their bests to make their services as reliable as it is possible. Manufacturers have also dealt with their products' reliability and done their bests to make their business profitable. They often push up a huge cost of failure under warranty period time. Although the costumers have accepted failure occurrence in their products, they are becoming highly sensitive to the failure in warranty time. Thus, manufacturers inevitably have to estimate the reliability of their products for the warranty period.

The ability of well working (without occurring any failure) of a product/system/ equipment in the certain period of time is the raised question addressing with the aid of the science of probabilities and statistics. Therefore, a clear definition of reliability engineering is [1]:

"*The probability that an item will perform a required function without failure under stated conditions for a stated period of time*."

Reliability as a simple definition is the number of failures in a specific period of time. Generally, the objectives of reliability engineering are falling into the following categories [1], [2]:

1- To apply engineering and technical knowledge in order to avoid or to decline the probability or frequency of failures.
2- To identify and to mitigate the prime causes of failures that do occur whether or not some efforts have been made to remove them.
3- To determine some ways of relieving the failures that do occur providing that their causes have not been eradicated.
4- To estimate the reliability of newly-design items.

Hence, reliability assessment is said to be an inseparable part in engineering fields. However, considerable challenges have been also remained and have to be wrestled [3], [4].

An engineering product could fail owing to different reasons. The main reasons are as follows: inherently capability of product design, exposing to the overstressed working environment, product wearing out, uncertainty of product strength or uncertainty of applied load (strength-stress variation), time dependency of failure mechanism, errors owing to incorrect specifications and design. Failures have various causes and effects and there are also different concepts, perceptions and definitions for categorizing the events in the failure or not [1], [4].

Reliability history belonged to the much earlier time. However, the new reliability discipline focusing on one of the Rome Air Development Centre (RADC) objectives, namely "*developing prediction methods for electronic components and systems*", launched in early 1960s [2]. Two launched approaches fell into two following categories:

1- Statistical approach (also called mathematical approach): in this method, collected reliability data in the specified field has been utilized. MIL-HDBK-217A is the first reliability prediction handbook published in December 1965 by the US Navy. It shed the light being well accepted by all designers of electronic systems, owing to its flexibility and ease of use. Despite its wrong basic assumption, namely an exponential distribution of failures [5], MIL-HDBK-217A became the almost exclusive prediction method for the reliability of electronic systems, and subsequently other sources of prediction methods gradually disappeared [6].
2- Physic of failure approach (PoF and also called physical reliability): it is based on the knowledge of failure mechanisms by which the considered components and systems are failing. This approach was firstly taken into account in Physics of Failure in Electronics symposium sponsored by the RADC and the IIT Research Institute (IITRI), in 1962. However, this symposium worked in the different name of International Reliability Physics Symposium (IRPS) which was the most influential scientific event in failure physics.

The two approaches seemed to be distinctive; system engineers were focused on the 'statistical approach' while component engineers working on PoF. However, both groups realized that two methods were complementary and attempted to unify the two approaches.

In 1974, the RADC as a promoter of PoF approach became responsible for providing the second version of MIL-HDBK-217, and of also its subsequent successive versions (C to F). In the latest versions, they tried to update the handbook by considering new advances in fabrication technology. However, more complex models were extracted which made the new models too complex, too costly and unrealistic [6]. In the 1980s,

a lot of manufacturers of electronic systems had tried to develop specific prediction methods for reliability such as proposed models for automotive electronics by the Society of Automotive Engineers (SAE) Reliability Standards Committee and for the telecommunication industry (Bellcore reliability-prediction standards).

1-1-1 Statistical method

In this approach, mathematical models based on the experimental and/or test data has been used for reliability assessment of an item, especially, electronic components such as different types of transistors, capacitors, etc. These models and data as well could be found in different reliability handbooks. Reliability assessment based on the reliability handbooks has two features as follows [7], [8]:

1- Failure rates are sorted and listed in the "Failure Rate Table" based on the components type.
2- Correction factors are being prepared for modifying the failure rates in the different conditions.

Accordingly, statistical method has tried to estimate the reliability of a specified item (here it can be considered as an electronic component) utilizing constant failure rates during their performances. Heretofore, a huge number of reliability handbooks have been provided by various organizations (but mostly military organizations) in order to evaluate and estimate reliability of electronic components [7]–[11]. Some of them are explained here as a snapshot.

1-1-1-1 MIL-HDBK217 reliability handbook

MIL-HDBK217 is one of the most important reliability hand books and has been extensively applied in electronic equipment and components reliability assessment. It has been published in 1965 by US navy [2]. It comprised a significant number of electrical components and devices and thus, its importance and ease of use being grasped by various military and commercial organizations [12]–[15]. Nevertheless, its proceeding versions have been published in the different periods of time regarding ever-increasing new electronic components production. The latest version was published in1995 and never has been updated yet. However, it has to be mentioned that there are still substantial number of studies employing such reliability models based on MIL-HDBK217 [15]–[17].

Two estimation models, namely part count and part stress, have been provided in MIL-HDBK217. Part count model is applied in the initial design phases in which the number of components and their quality levels are specified [7]. In this model, there is no detailed information about the components and stress level they are exposed to. Part stress model is based on the effects of mechanical, electrical and environmental stresses such as temperature and humidity on the failure rates. This model is used whenever the design has been roughly completed and the details of

applied stresses has been determined. Since much more information is in access, more precise estimation is achieved in comparison with part count model.

In this model, environmental coefficients indicates the environmental stresses on the components or equipment. Almost all of the environmental stresses have been considered in the latest version [7]. Part stress model, in the component level (but not in the system level), calculates the component failure rate of a component regarding to the applied environmental stresses. For instance, a component failure rate can be estimated as follows:

$$\lambda_P = \lambda_b \pi_Q \pi_E \pi_A \pi_T \pi_V \quad (1\text{-}1)$$

where λ_b is the base failure rate extracted from experimental tests in an specified condition. Correction factors are including π_T (temperature coefficient), π_A (application coefficient), π_V (voltage stress coefficient), π_Q (quality coefficient) and π_E (environment coefficient). Equipment failure rate (at the system level) can be predicted using part count models as follows:

$$\lambda_{EQUIP} = \sum_{i=1}^{n} N_{part-i} \left(\lambda_g \pi_Q\right)_i \quad (1\text{-}2)$$

where λ_{EQUIP} is the equipment failure rate. λ_g and π_Q are the general failure rate and quality coefficient for the i^{th} component, respectively. N_{part-i} is the number of i^{th} component in the system and n is the total number of different components in the system.

MIL-HDBK-217 has provided a considerable database for many different types of parts including capacitors, switches, relays, magnetic devices, printed circuit board (PCB), etc. This reliability handbook prepares a uniform reliability assessment database without emphasizing on significant reliability experiences as a particular component [13], [14]. However, this reliability handbook does have limitations [7]. Assuming a constant failure rate for different components during their useful lifetimes is one of the main limitation this reliability handbook confronts to [3]. Field experiences show that the reliability estimation of either components or systems have been significantly optimistic. Furthermore, it does not reflect the temperature swing effects (or any other mission profile which are completely important to power electronics converter) leading to an inaccurate life estimation. Failure rate models and database of some components such as insulated gate bipolar transistors (IGBT) have not been included and thus the other switches have been considered instead.

1-1-1-2 IEC-TR-6238 reliability handbook

This reliability handbook was published in 2004 and aimed to assess the reliability of power electronic components and equipment [8]. Environmental and performance stresses have been also considered in power electronic components'

reliability assessment as it has been done in the MIL-HDBK-217. With regard to the application, level of effectiveness of these kinds of environmental stresses (mechanical, chemical, etc.) has been launched [18].

In addition to the above-mentioned parameters and coefficients, another parameter called "mission profile" parameter has been also seriously contemplated through reliability assessment in order to increase the accuracy of reliability estimation of power electronic components. In fact, mission profile reflects loading level of power electronic components (regarding to their application and the converter topology). For example, irradiation level is being identified during the year regarding the global irradiation map [19]. Hence, in the photovoltaic (PV) applications, the power which can be harvested from the sun irradiation and transferred to the grid utility via a PV inverter might be specified. Accordingly, one can calculate the electrical stresses (finally resulting to thermo-mechanical stresses in PV inverter components) during a year or any other specified period of time. This weakness (lack of considering mission profile) is evident in MIL-HDBK-217 reliability hand book. It generally means that the correction factors have only effects on the base failure rate of the component under specified conditions (stresses). For instance, π_T is considered as a constant temperature coefficient assuming that the component is exposed to the specified stresses in MIL-HDBK-217 reliability handbook. Thus, it is not the case in the real applications in which the component confronts various stresses (mission profile). Furthermore, a much more reliability estimation is achieved regarding the consideration of failure sites e.g. package or chip (die) in this reliability handbook. For example, a mathematical model of power diode gives:

$$\lambda = \left[\begin{array}{l} \left\{\lambda_0 \pi_U\right\} \times \left\{ \dfrac{\sum_{i=1}^{y} \tau_i \left(\pi_t\right)_i}{\tau_{on} + \tau_{off}} \right\} + \left\{ \left(2.75 \times 10^{-3} \sum_{i=1}^{z} \left(\Delta T_i\right)^{0.68} \left(\pi_n\right)_i \right) \times \lambda_B \right\} \\ + \left\{\pi_I \times \lambda_{EOS}\right\} \end{array} \right] \times 10^{-9} / \mathrm{h} \qquad (1\text{-}3)$$

where π_U is the utilization coefficient, λ_0 the base failure rate of chip, $(\pi_t)_i$ the i^{th} temperature coefficient corresponded to the i^{th} diode junction temperature in mission profile, τ_i the i^{th} working time of diode for the i^{th} diode junction temperature in mission profile, $\tau_{on}(=\Sigma^{y}_{i=1}\ \tau_i)$and τ_{off} the on and off working time of the diode, $(\pi_n)_i$ the i^{th} temperature cycling impact factor seen by the component package with temperature cycle of ΔT_i in the mission profile. λ_B , π_I and λ_{EOS} are base failure rate of packaging, utilization impact factor of diode and failure rate related to over stresses regarding the application, respectively.

Although, a considerable number of studies have made effort to assess the reliability of their systems by this reliability handbook [18]–[20], lack of consideration of

manufacturing technology and various types of power electronic devices result in inefficiency.

1-1-1-3 Other reliability handbooks

TELCORDIA-SR-332, BT-HRD-5, NTT, CNET, RDF93, RDF2000, SAE, SIMENS-SN-29500, 217-PLUS and FIDES are the other reliability references, especially employed in electronic and power electronic components' reliability assessment, which have been developed their data based on the US army, transportation and telecommunication industries [21]–[24].

TELCORDIA-SR-332 is related to the telecommunication components and equipment and provides Bayesian analysis for reliability assessment. The principle of mathematical models of TELCORDIA-SR-332 is based on black box approach [24]. This part count approach defines steady state failure rate of equipment and based on the experimental data gives mathematical models for reliability assessment. Discussing other reliability references is beyond this study and hence interested readers are referred to [24], [25].

1-1-1-4 Comparison of reliability assessment based on the aforementioned reliability references

Table 1-1 indicates a quantitative and qualitative comparison among five well-known reliability handbooks, namely MIL-HDBK-217, TELCORDIA-SR-332, IEC-TR-62380, 217-PLUS and FIDES2004. Regarding this Table, one can find that 217-PLUS has paramount features in comparison with the other reliability references [26].

Numerous studies have been estimated reliability of power electronic converters by employing mathematical approach [20], [27]–[30]. These studies have been applied the above-mentioned reliability handbooks for calculating failure rates of different components and finally predicted system level reliability using stochastic processes (or other probabilistic methods). These probabilistic methods have been extensively used in reliability assessment and risk taking analysis in power electronic systems [3].

1-1-2 Physics of failure method

Despite that this approach has been extensively used in microelectronic reliability for the plenty of years, power electronic researchers have opened up a new issue in reliability assessment employing this method [31]–[39]. In power electronic systems, this method has been gained considerable interests among the researchers owing to the limitation of a systematic design for reliability (DFR) and optimistic reliability assessment by the other approaches [40].

Table 1-1. A quantitative and qualitative comparison among five well-known reliability handbooks

Reliability references	MIL-HDBK-217	IEC-TR-62380	TELCORDIA-SR-332	217-PLUS	FIDES
Version	F	Edition 1	Issue 1	Edition 1	Issue A
Date of publication	1995	2004	2001	2006	2004
Failure rate Unit	Failure in 10^6 hours	Failure in 10^6 hours	Failure in 10^9 hours	Failure in 10^6 hours	Failure in 10^9 hours
Software	Yes	Yes	Yes	Yes	No
Default environmental options	14	12	5	37	7
Component model	Multiplication	Multiplication	Multiplication	Sum	sum
Mission Profile	No	Yes	No	Yes	Yes
Temperature cycling	No	Yes	No	Yes	Yes
Temperature rise in the component	Yes	Yes	Yes	No	Yes
Failure in soldering	No	Yes	No	Yes	Yes
Failure in off	No	No	Yes	Yes	Yes
Bayesian analysis	No	No	No	Yes	No

On the contrary to the statistical method, PoF does not concentrate on a constant failure rate model of component and takes into account the mission profile in which the components are exposed to. Physics of failure is based on deterministic sciences (such as material and chemical sciences) and is able to assess the component reliability applying probabilistic and statistic sciences. Not only does this method assist in performance recognition and risk reduction in the design phase, but also models the failure root causes including fatigue, creep, fracture, corrosion, etc [41].

PoF based reliability assessment aims to find failure mechanisms and investigate the effects of mission profile on the critical failure mechanisms. This leads to transfer reliability analysis from component level to the failure mechanism and enhances it from reliability prediction to DFR [38].

In other words, physics of failure of electronic devices have been initially determined and then the failure root causes have been recognized. Based on the determined failure root causes (such as power cycling or temperature swing) and the mission profile (of the considered component) and employing reliability models, one can estimate component's aging and useful lifetime regarding its mission profile.

In addition, by identifying the failure mechanisms and their corresponding root causes, one can use this data for condition monitoring of considered power electronic components. As an example, bonding wire lift off in a power semiconductor can decrease useful lifetime of the device. Thus, on-state voltage of power semiconductor (V_{on}) can be utilized as a failure indicator providing that there is sufficient data about the relevance of this voltage to the aging of device [36].

1-1-2-1 Physics of failure terminology

In this section, some expressions which are commonly used in physic of failure method will be discussed.

- Mission profile (Load cycle): It is related to all operational or environmental (non-operational) conditions affecting the device. There exist numerous load cycles that can be individually or simultaneously applied. One can find some examples in Table 1-2.
- Failure mode: It is the effect by which a failure is observed including short circuit, open circuit, loss of gate control, parameter drift ($R_{DS\text{-}on}$, ESR, C and …), etc. The permissive value of parameter drift is denoted through Failure criteria. In addition, one can use these parameter drifting as indicators. For example, 20% increase in $R_{DS\text{-}on}$ in power metal oxide field effect transistors (MOSFETs) is considered as the failure criterion.
- Failure mechanism: The physical, chemical, thermodynamic or any other processes which results in the failure. The failure mechanisms fall into two main categories, overstress and wear-out. Some examples are listed in Table 1-2 [42].
- Root cause (failure cause): A specific process, design and environmental factors that initiated the failure whose removal will eliminate failure. Some examples are listed in Table 1-3 [43].
- Failure site: A location in component which a specific failure occurs in it. Some examples are listed in Table 1-3.
- Failure criteria: Criteria or standards, with regard to applications, define or denote the failure boundaries. It is totally different from one component to the others and also from one failure mechanism to the other failure mechanisms. For example, a failure criterion is 100% increase of ESR in capacitor.
- Failure model: It relates to either deterministic or stochastic models (even both simultaneously) governing the failure mechanisms. Maybe, in the system level reliability assessment, newly established models are required.
- Damage indicator: It is in charge of indicating the degradation level of component required for maintenance or reliability evaluation. These damage indicators can be employed for condition monitoring. It is often used to stop the aging tests before failure using the Failure criteria.

Table 1-2. Mission profiles [42]

Load	Load conditions
Thermal	steady state temperature, temperature swing (cycling), temperature gradient , temperature swing rate, thermal loss
Mechanical	Pressure magnitude, pressure gradient, vibration, stress, strain
Chemical	Humidity level, pollution, particles
Physical	Radiation, magnetic interface, altitude
Electrical	Current, voltage, power, frequency

Table 1-3. Example of Power Semiconductor failure mechanisms [43]

Failure Mechanism	Failure Site	Root Cause	Failure Models
Fatigue	Die attach, wire bond/TAB, solder leads, bond pads, traces, vias/PTHs, interfaces	ΔT, Tmean, dT /dt, dwell time, J ΔV and ΔH	Nonlinear power law (Coffin–Manson)
Corrosion	Metallization	M, ΔV , T	Eyring (Howard)
Electro-migration	Metallization	T , J	Eyring (Black)
Conductive filament formation	Between metallization	M, ∇V	Power law (Rudra)
Stress driven diffusion voiding	Metal traces	S, T	Eyring (Okabayashi)
Time-dependent dielectric breakdown	Dielectric layers	V, T	Arrhenius (Fowler–Nordheim)

M: Moisture V: Voltage H: Humidity J: Current Density S: Stress T: Temperature

Failure modes, mechanisms and effect analysis (FMMEA) has been extensively used in PoF reliability assessment approaches as shown in Fig. 1-1 [32], [44], [45]. Firstly, the system and the components and the functions having to be analyzed are defined. Then, the potential failure mode is identified. Based on the mission profile (either operational or environmental) the potential failure causes are also identified. Next, the failure mechanisms and their associated failure models such as Coffin-Manson law are identified. Failure models are curve fitted by some accelerated aging tests. Finally, one can prioritize the most critical failure mechanism and begin PoF reliability assessment approach. Thus, identifying the critical failure mechanisms and their root causes as well is paramount of importance in reliability assessment based on the PoF algorithm.

1-1-3 Pros and cons of the two reliability assessment methods

As seen above, two distinct methods, namely mathematical approach and physics of failure based approach have been launched for years and years. However, none of them is capable of mitigating the challenges raising in this field.

On one side, as a mathematical reliability assessment point of view, this method is capable of assessing reliability either in a component- or in a system-level employing some stochastic processes. This means that if a system (power electronic

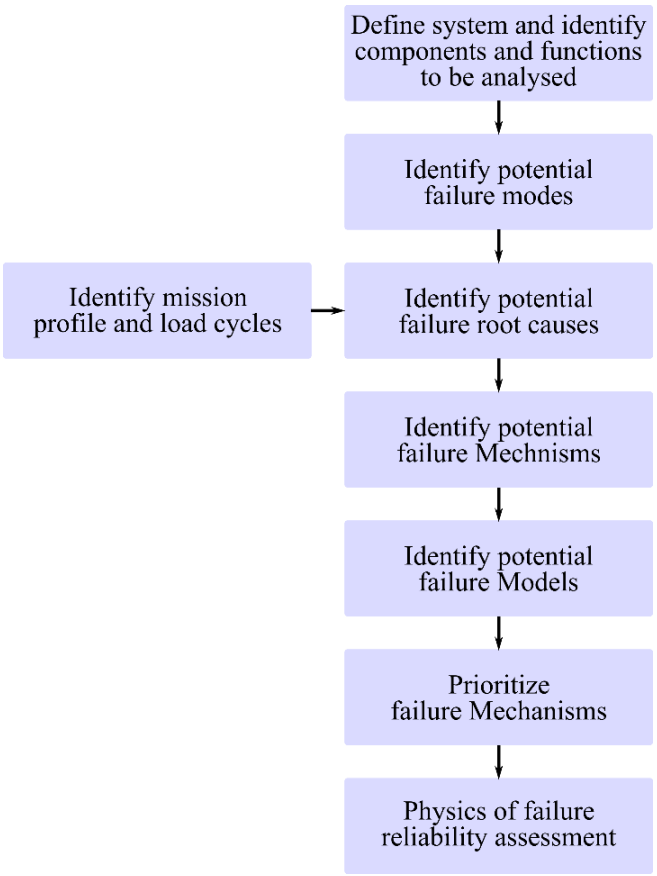


Fig. 1-1. Failure mode, mechanisms and effect analysis physics of failure reliability assessment method

converter as an example) can roughly-appropriate works under a local failure occurrence (one of the components fails during the normal working but the system is well working so far owing to the fault tolerance of system design), the method is still able to assess the reliability. Another weakness point of this kind of reliability assessment is absence of mission profile consideration such as temperature cycles and operational cycles. In other words, the failure rate (λ) is supposed to be constant during the systems' performances.

DFR is one of the other important aspects in the reliability assessment which is playing a major role in the design of a reliable system. Since in the mathematical approach there is no consideration on root causes' identification, thus there is no ability to enhance the reliability of the system in the design phase and the reliability assessment output is only and only a number. In addition, degradation and wearing out of one component on the other critical components is not taken into account leading to much more optimistic reliability assessment. Last but not least is the consideration of the components' manufacturing technologies which is still lacking in the mathematical reliability assessment.

On the other side, consideration of the mission profile including both environmental and operational factors is one of the notable point of PoF based reliability

assessment leading to much more realistic reliability estimation of a component. In addition, the wearing out of a component is also taken into account. DFR is also achieved owing to the identification of critical failure mechanisms and their corresponding root causes. This means that one can easily design a reliable system in the design phase by minimizing the root causes effects on the critical components.

However, this method is significantly costly and time consuming and regarding to the distinct manufacturing technologies from one component to the others it becomes much more complicated. Another detriment of this method as well as mathematical approach is the lack of consideration of mutual degradation effects on each other. It means that degradation and wearing out of one components on the other critical components is not taken into account.

The weakest point of this method is that it is restricted to the only component level reliability assessment. Thus, in a tolerant system in which the system can also work after a failure occurrence in a sole component, this method is not able to estimate system level reliability assessment.

Regarding the above-mentioned discussion one can find that the advantages of PoF based reliability assessment far outweigh its disadvantages and it is encouraging enough to be modified for proposed method here.

1-2 Literature review

By ever-increasing demand of energy and environment protection as well, developing alternative energy resources (AERs) and hybrid electric vehicles (HEVs) are paramount of importance. Renewable energy resources such as solar and wind energies can make a real difference. However, efficient and sustainable exploitation of these sorts of energies become an enormous challenge having to be wrestled among all the researchers. Additionally, effective employing of HEVs has assessed a meaningful significance. Thus, it is undoubtedly one of the most pressing concerns facing all the electrical engineers. With regard to their non-fixed and uncertain nature, some power converters and conditioners have to be resorted [46]–[50]. According to the application and its power range, many types of converters including DC-DC, AC-DC, DC-AC and AC-AC have been applied in energy harvesting [46], [51], [52].

Since power converters are wise and popular choices in power conversion and power management, the quality of their demand responses play a key role in the reliable power systems and equipment. Reliable systems either in utility grid (electrical grid in which all the consumers meet their electrical demands) or in individual applications must be achieved owing to some reasons. Perfectly reliable products have the main priority among all individual consumers due to economic issues. Furthermore, utility grid is in charge of supplying uninterrupted electrical

energy to the general users. Therefore, a highly reliable utility grid has been expected. Since renewable energies account for a considerable share in the energy supplying in the utility grid through some power converters and conditioners [53]–[55], namely power electronic converters, reliability of power electronic converters has been gaining importance [40]. Interested in renewable energy conversion, automobile systems and the other related applications, persuading investors along with the technical issues such as power system stability has always sparked off a heated debate among the researchers and businessmen. Furthermore, concerns of manufacturers about guaranty time period coupled with the maintenance cost and its time period are also undoubtedly two of the most pressing concerns facing all electrical engineers. Accordingly, researchers have recently opened up a new issue about power electronic converter reliability [56], [57].

In the last few years, significant attention has been gained in the reliability of power electronic converters. Numerous and different metrics of estimating system reliability are defined and discussed [58], [59]. Power electronic converters as a meaningful system requires mathematical reliability assessment. Component-level based failure models are widely discussed [56], [60]–[66]. Several quantitative and qualitative methodologies have been also given to establish system-level based reliability. These two supplementary models, namely component and system level models, merge together to provide precise reliability estimation [58], [67]–[70]. For the different cases in which classic design of power electronic converters have been used reliability requirements have not been met and thus, numerous approaches such as active online/offline monitoring, faults managing, and extending fault-tolerant operation have been applied for reliability improvement [71]–[82]. One of the most efficient solutions for the power electronic converters' redundancy (leading to much higher reliability of power electronic systems) is fault tolerant designing [83]–[88]. This kind of designing declines the number of failure by managing post fault strategy either in controlling strategy or in converter topology and leading to more reliable power electronic systems. Reliability assessment plays a considerable part in designing and operating of the systems. Quantitative reliability assessment seems necessary in determining whether or not a particular design meets requirements. It is also a great metric for comparing various topologies, controlling scheme and devices.

Reliability of power electronic systems' performances has launched considerable challenges in various applications, especially renewable energy exploitations and electric motor drive systems, in which power electronic converters are exposed to various severe environmental or mission profile stresses [89], [90]. Power electronic equipment might be exposed to various stresses such as electrical, mechanical, thermal, physical and chemical ones [91]. These sorts of stresses might affect power converter's performance and even might lead to useful lifetime

reduction of power electronic equipment [92], [93]. Consequently, useful lifetime estimation of power electronic equipment could expect the approximate periodical repair and maintenance times. According to this lifetime pattern, one can organize repair and maintenance time in order to minimize downtime and repair and maintenance costs.

As an example in the wind farm, distribution of failure rates and their associated downtime in various part of wind turbine is illustrated in Fig. 1-2 [40]. Based on Fig. 1-2, one can find that electrical parts of a turbine have been more likely exposed to failure. Hence, reliability assessment in power electronic converters is paramount of importance [38], [43], [94]–[96]. In PV systems, PV inverters have been employed for converting DC voltage to AC voltage in order to connect the solar panels to the grid [97]. In addition to ever-increasing development of PV systems, PV inverters are still the most critical sub-system as the failure rate, useful lifetime and maintenance cost points of view [97], [98]. Although all the early pioneers in this field guarantee at least 20-year-old useful lifetime for their PV modules, useful lifetime of PV inverters has been reported about 5 years on average in 2012 [97]. Recent report in [98] indicates that 37% of unscheduled repair and maintenance and 59% of its corresponding costs were allocated to PV inverters.

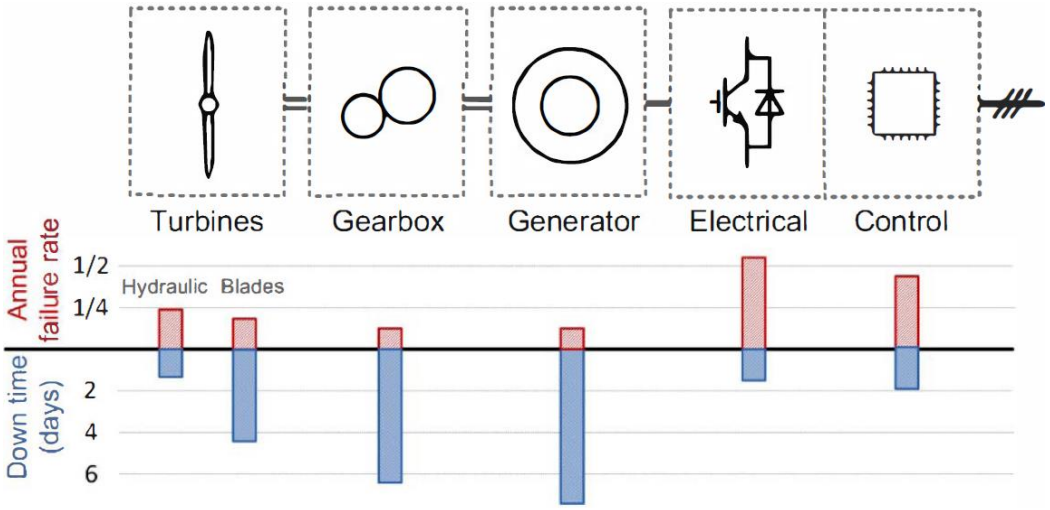


Fig. 1-2. Distribution of failure rates and their associated downtime in various part of wind turbine [40].

Among all of aforementioned power converters and power conditioners, DC-DC power converters have a great contribution as a widespread belief in renewable energy exploitation and HEVs power conditioning. Meaningful interests have been attracted in the reliability assessment of DC-DC power converters in the various applications during recent years [99]–[105]. In [99], a modular DC-DC converter has been proposed for reliability enhancement of power conditioning of fuel cell (FC) stacks. This proposed converter improves the reliability by designing a fault tolerant system. This paper does not deal with reliability assessment but with design for

reliability. A high area efficient DC-DC power converter has been proposed by [100] in which reliability improvement has been achieved via time mode miller compensation (TMMC). In [103], passive snubber circuits have been employed in DC-DC power electronic converters for enhancing reliability of power converters by decreasing switching power loss of IGBT. In this paper, Choe et. al have tried to assess reliability of a specific power converter through classical method in both cases, namely in absence and presence of passive snubber circuits. Ref. [104] has wrestled out with optimum designing of multiple-active-bridge DC–DC converter for smart transformer as the reliability point of view. Reliability-oriented optimizing of the LC filter of Buck DC-DC power converter has been launched in [105]. In this study, a closed loop circuit design and reliability assessment procedure has been applied for optimizing LC filter volume versus reliability and power converter useful lifetime.

As it was also mentioned in the first section, there are generally two different reliability approaches, namely physical and mathematical approaches also extending to the DC-DC power electronic reliability assessment. Numerous studies have been carried out for reliability evaluation of DC-DC power converters based on the above-mentioned approaches [20], [21], [27], [29], [30], [106]–[112]. Reliability assessment of a multistate interleaved DC-DC converters and cost minimizing have been considered in [108] employing MIL-HDBK-217F [7]. It reveals that 3-phase interleaved DC-DC power converters with 43.4 kHz switching frequency demonstrates a much higher reliability in comparison with two other proposed scenarios, namely 81 kHz one-phase and 100 kHz two-phase interleaved DC-DC power converters as shown in Fig. 1-3. Although, reliability estimation has been performed fast, mission profile at which the components are exposed to has not been considered leading to some errors in reliability assessment of DC-DC power converters.

This detriment has been tried to be solved by considering mission profile effects on the reliability assessment of power electronic converters [20], [21]. In [20], a conventional push pull DC-DC converter as an interface in PV application has been understudies and demonstrated that temperature cycling as a mission profile has a significant effect on the reliability assessment of power electronic DC-DC converter applying MIL-HDBK-217F and IEC-TR-62380 reliability handbooks [7], [8]. Temperature cycles contribute with a significant share to the overall failure rate; therefore, it is necessary to correctly identify the mission profile that the converter is subjected to. There are meaningful differences between the failure rates extracted with both methodologies. The discrepancies can be explained by the fact that, in each methodology, the sensitivity of the failure rate to a given influence factor is different. Thus mission profile consideration plays a major role in reliability assessment of power electronic converters. Although, using IEC-TR-62380

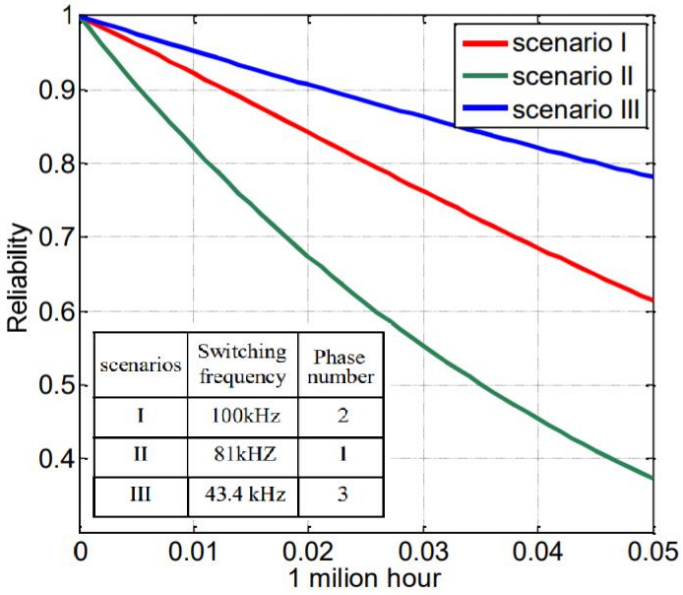


Fig. 1-3. Reliability curves as a function of time for different scenarios [108].

reliability handbook can somewhat solve mission profile consideration (no mathematical approaches can completely solve this problem), failure rates are assumed to be constant during their useful lifetimes which is not the case in the real applications. Failure rate has to be assumed as a bathtub curve in which at the beginning and the ending the failure rate is much higher owing to infant mortality and wear out, respectively as shown in Fig. 1-4 [3].

Reliability evaluation of boost DC-DC converter has been performed in [29]. This paper tried to consider degradation of devices in the boost converter by taking into account some different values for critical components such as capacitors and MOSFETs. The procedure is shown in Fig. 1-5. This led to time dependent failure rate which was not solvable mathematically owing to a complex reliability integral. The mathematics had been numerically solved for only a few specified points. This reveals a very small increase in system failure rate due to parameter drifting or aging.

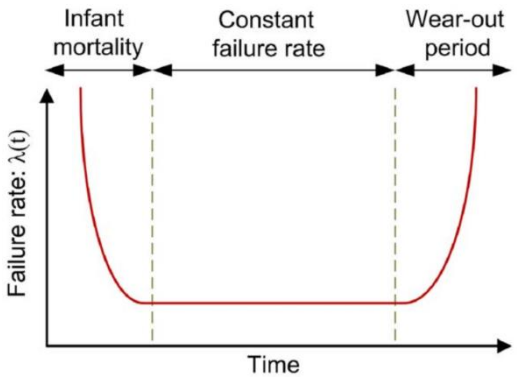


Fig. 1-4. Bathtub curve of failure rate [29].

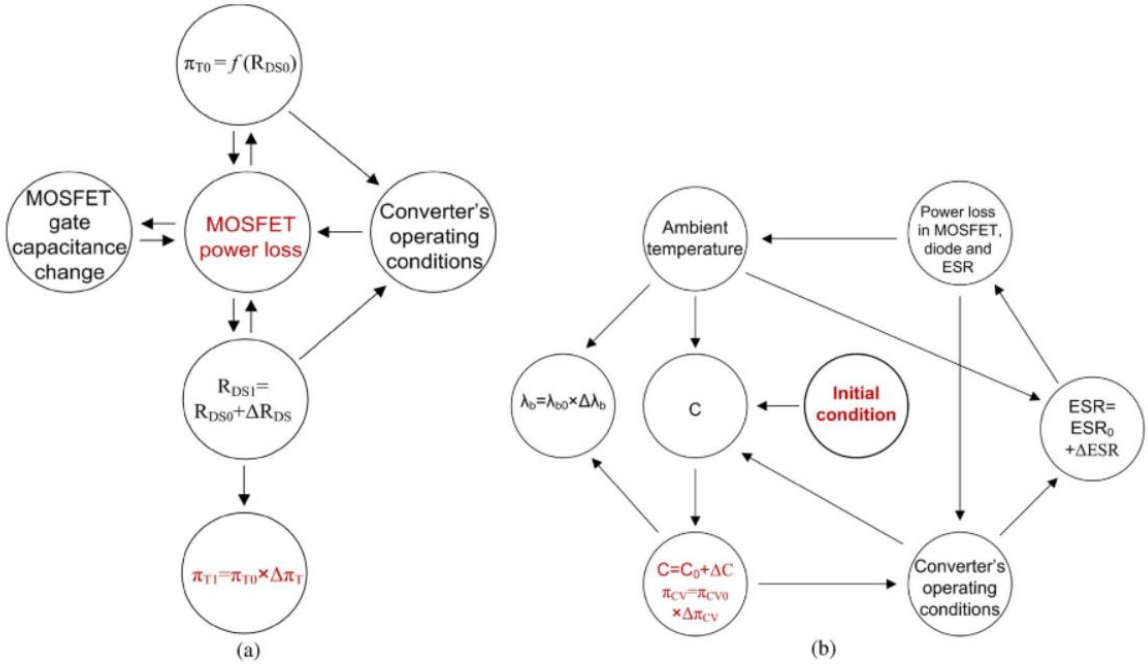


Fig. 1-5. (a) Effect of $R_{DS\text{-}on}$ variation of the MOSFET on the reliability of the converter. (b) Effect of capacitance C and ESR variations on the reliability of the converter [29].

Studies in [27], [30], [110] concentrated on the reliability assessment of multiphase interleaved DC-DC power converters (as shown in Fig. 1-6a) using mathematical approach. Effect of power switches' parameters on the failure rate has been investigated. It was also the case for the output capacitors. Based on these effects, reliability models of the capacitor and the power devices extracted from MIL-HDBK-217F have been defined and then a system level reliability assessment based on the Markov process (stochastic process) as shown in Fig. 1-6b has been performed [111], [112]. As it is shown in Fig. 1-6b, there are ten different health states in Markov process. State 00 represents the new stage of power converter working while state 33 represents a failure stage in power converter in which the converter is no longer working. Design for reliability, failure root cause identification, mission profile consideration and mutual and self-degradation effects consideration as well are all being missed in these studies leading to the optimistic results.

There are various studies concentrating on DC-DC converters reliability assessment based on mathematical method [28], [106], [107], [113]–[117]. All of these studies have the same procedure as explained for previous investigations. All the mathematical based reliability assessment include the advantages and disadvantages presented in 1-1-3.

On the other side, some most recent studies have focused on PoF reliability assessment of DC-DC power converters [118]–[122]. Existing converter-level reliability analysis approaches deal with two major limitations: 1) being based on constant failure rate models; and 2) lack of consideration of long-term operation

conditions (mission profile) [118]. One can complete the limitations by categorizing lack of consideration of manufacturing technology, lack of consideration of mutual and self-degradation effects on the performance of converters, and lack of focusing on the critical failure root causes in order to facilitate design for reliability.

The main procedure of reliability assessment of DC-DC power converter as an interface between the utility and FC plant is shown in Fig. 1-7. Regarding this figure, the mission profile has been translated to electrical and thermal parameters and then applied to power loss modeling and then to the thermal modeling and finally applied to lifetime model and damage model. A notable point is the consideration of parameters deviation due to the manufacturing process uncertainties and uncertainties of the accelerated aging test owing to the low number of samples regarding time and expense limitation. Thereby, normal distribution for the constant parameters of power semiconductor lifetime model has been considered lading to the Weibull damage distribution employing 10000-sample Monte Carlo simulation.

This procedure also applied for reliability evaluation of capacitors leading to another damage distribution. Employing reliability block diagram (RBD) together with fundamental system-level reliability led to eventual DC-DC power electronic converters.

On the contrary to the mathematical methods, this applied method tackled some of mathematical methods' detriments. Mission profile, DFR related issues, manufacturing technology, and wear-out have been all considered. Additionally, it has overcome system level reliability but not as a systematic approach. However, mutual and self-degradation effects on the entire system reliability has been opened up yet. Also, a systematic system-level reliability assessment approach considering mission profile, mutual and self-degradation effects and wear-out is still lacking.

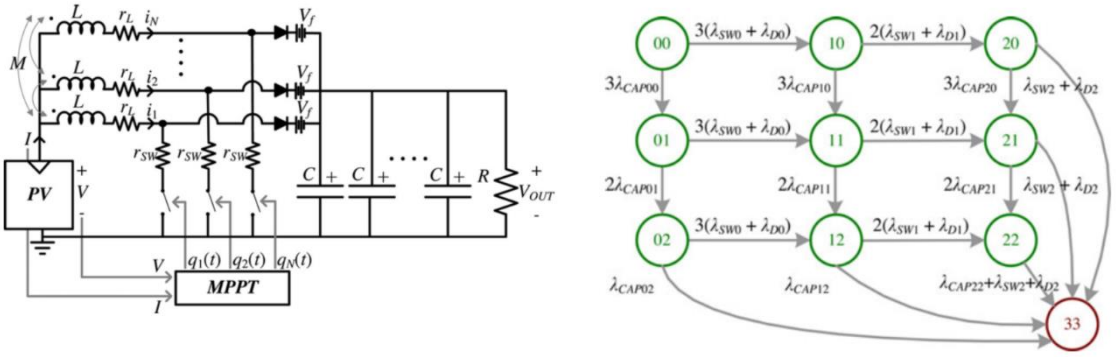


Fig. 1-6. (a) N-phase, interleaved boost converter model. (b) State-transition diagram of three-phase converter [27].

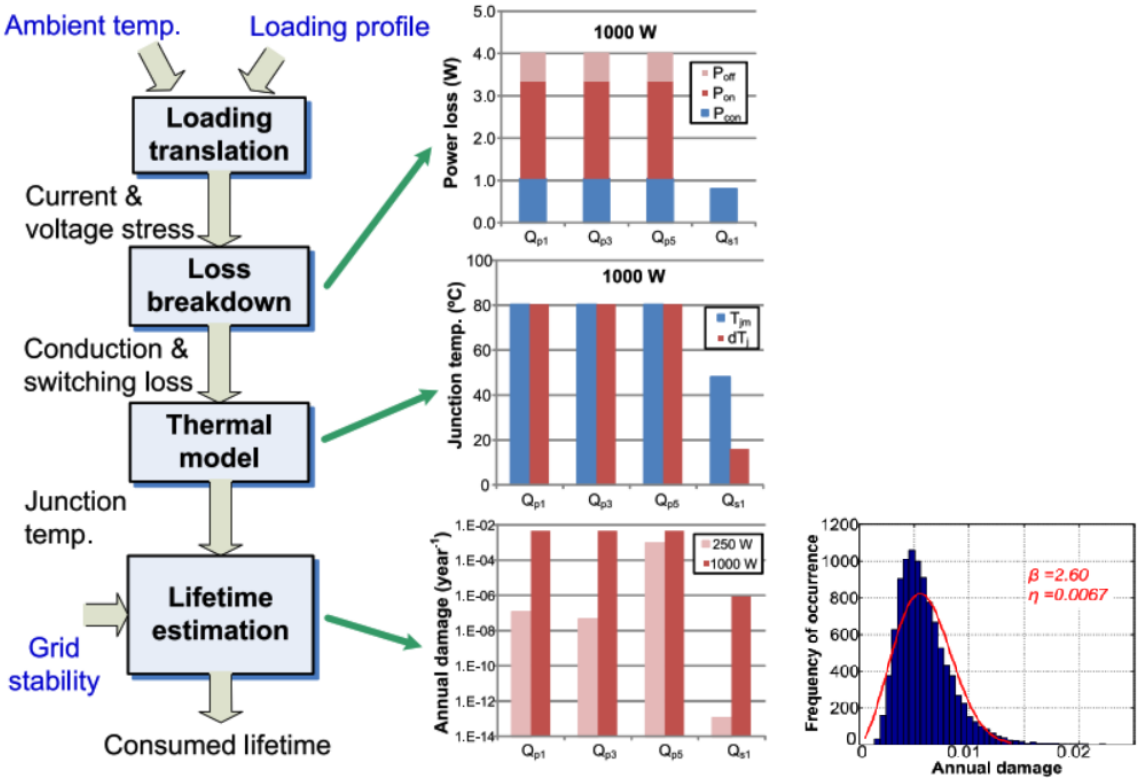


Fig. 1-7. Flowchart to predict lifetime of power semiconductor in the operation mode [118].

1-2-1 Reliability Models

1-2-1-1 Component-level based reliability models

As the component-level based reliability models in power electronic systems, the main concentrations have been directed to the failure rate based models in the most critical parts including power semiconductors and capacitors [58], [67], [68], [70], [123]. Field experiences and previous studies have indicated that capacitors and power devices, namely IGBTs and MOSFETs, are the most vulnerable components in the power electronic converters. Despite that magnetic elements have also be widely used in power electronic converters, previous experiences and studies demonstrated that they are much more reliable [124], [125]. Thus, a large number of available reliability models have been directed and adopted for these components. Empirical-based models, which are typically based on the observed failure data to quantify and metricize model variables, are most extensively used to analyze the reliability of components. The premise is that the valid failure-rate data are readily available either from field applications or from laboratory tests [94]. There are many empirical-based reliability models as described in previous sections.

On the other side, PoF based reliability estimation of the critical components such as capacitors (especially electrolytic capacitors), power IGBTs and power MOSFETs has been also extensively undertaken in component-level [62]–[65]. The PoF based

reliability method can model critical failure mechanisms, estimate wear-out conditions, and integrate reliability into design process, but in component-level reliability. However, as previously mentioned it is costly and time consuming and requires a substantial knowledge of materials and failure mechanisms [66].

1-2-1-2 System-level based reliability models

For designing a reliable power electronic system, providing a systematic framework for reliability assessment is paramount of importance. Vast number of studies and methodologies for assessing reliability of power electronic converters have been launched in recent years. They fall into three different categories, namely part-count methods, combinatorial models, and state-space models [94], [95].

Part count model simplicity is one the most brilliant advantages of reliability assessment in part count model. Additionally, capability of comparing several architectures of power electronic systems is another outline feature of this method. However, over conservative reliability estimation of repairable systems or fault tolerant system is its detriment.

Combinatorial models are generalization of part-count models and comprise fault trees, success trees, and other reliability blocks diagrams. These approaches are able to be used for analyzing reliability of redundant systems. These methods lack specifying the details of fault-tolerant systems, such as repair process, imperfect coverage, state-dependent failure rates, order of component failures, and system reconfiguration [95].

One of the most well-known systematic reliability assessment is state space modelling such as Markov model. It is based on graphical representation of system states corresponding to the different system states as a failure point of view. For example, state 1 allocated to the well working states of all components contributing in a system and state 2 is allocated to another state with a failure occurrence in one of the components. As functionally point of view, Markov models states fall into two categories, namely absorbing states and nonabsorbing. First states are allocated to failed system configurations, while second states are allocated to the configurations in which the system can work properly or with partial functionalities.

1-2-2 An overview on vulnerable and critical power electronic components

1-2-2-1 Failure distribution and stress sources in power electronic systems

A comprehensive and extensive study performed by Yang et. al [91] which has been also validated by much more recent studies [43], [94], [95] demonstrated the main failure sources and distributions based on the experimental fields. From failure structure point of view, there are two types of failure, namely intrinsic and non-

intrinsic. Intrinsic failure is originated by internal degradation of devices or power electronic converters. This degradation may be affected by external factors and stresses. However, non-intrinsic failure by itself is divided into two cases. First, failures originated by over stresses. Second, mal-design of power electronic converters. In power electronic systems, over stresses may be wrestled out by employing various types of protection systems including hardware and software parts.

For the reliability based designing, indicating failure mode and failure mechanism in the critical components (as reliability point of view) is essential. Fig. 1-8a indicates failure distribution among power electronic components [126], [127]. Regarding this figure, failure probability of capacitors and power semiconductors are far higher than the other parts. This fact that capacitors and power semiconductors both have allocated the greatest share in power electronic failure occurrence has been verified during several recent years [93], [96] and no one disputes on.

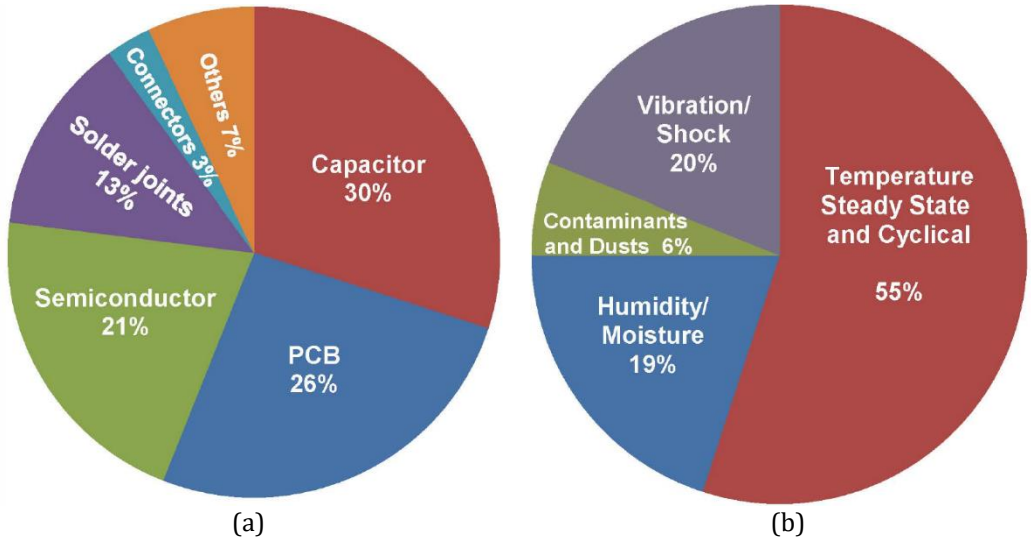


Fig. 1-8. Failure and stress distribution in power electronic components [40].

Fig. 1-8b demonstrates the most affecting stress sources in reliability of power electronic systems [128]. Regarding this figure one can find that temperature cycling and steady state temperature as well are the most dominant stressors in the power electronic components' and systems' reliability. Accordingly, electro thermal analysis and simulation has a significance importance on reliability in power electronic systems. It can also clearly be seen that not only are the thermal related issues important, but also mechanical related issues such as vibration and shock have also paramount of importance. That is why a large number of power electronic reliability studies have been directed to mechanical and electro-thermal reliability assessment [129]–[131].

1-2-2-2 Widely used power electronic components

It has been reported that power semiconductors as well as power capacitors are both the most affecting components in power electronic systems [38], [40]. Fig. 1-9 depicts abundance of power electronic semiconductors utilization in industrial applications including automotive applications, PV system, etc [91]. Power IGBTs allocate a considerable share (42%) among the power semiconductors usages in power electronic systems. It has been also predictable regarding the considered applications dealing with high voltage, high power and low switching frequency. This fact has been also validated by recent researches presented in [43], [118], [119]. Power MOSFETs and Thyristors are following it by smaller shares, i.e. 27% and 14% respectively. The other power devices such as GTO and IGCT do not have meaningful contributions in industry applications.

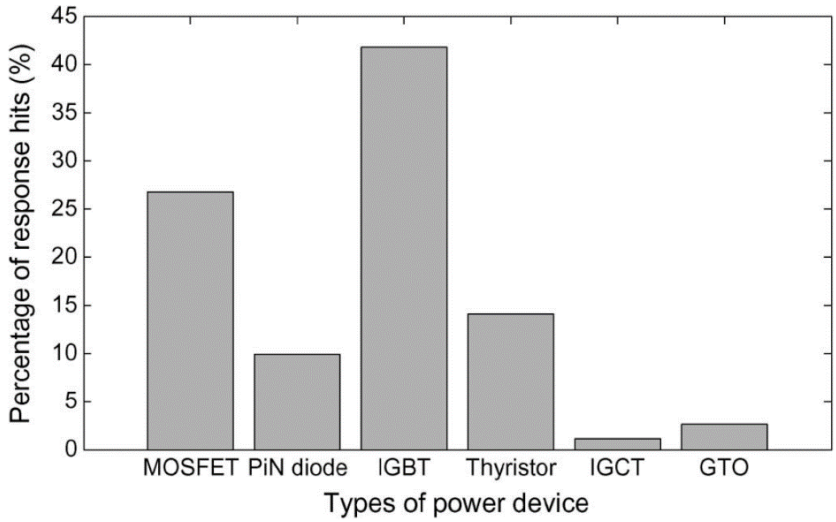


Fig. 1-9. Abundance of power electronic semiconductors utilization [91].

Three various types of capacitors have been commonly employed in power electronic systems with the distinct features, namely Aluminum Electrolytic Capacitors (Al-Caps), Metallized Polypropylene Film Capacitors (MPPF-Caps) and high capacitance Multi-Layer Ceramic Capacitors (MLC-Caps) [93]. As a capacitor point view, despite there is no quantitative comparisons among all types of capacitors, Al-Caps are the most applied capacitors in power electronic systems [109], [118].

1-2-2-3 Impact, Management and importance of power electronic reliability

The distribution of failure costs relative to the system costs are shown in Fig. 1-10. Regarding this figure, it reveals that 25% of failure occurrence (the greatest share) have led to more than 80% of failure cost to the system cost. It shows that a considerable cost has been burdened to the power electronic systems whenever a failure has occurred in the systems. Thus, many researchers and engineers have tried to minimize this cost ratio by some redundant parts leading to higher initial

cost investment. Fig. 1-11 demonstrates the methods for mitigating this problem. Roughly 42% of reliability improvement methods appertain to the cooling issues separated to 24% increased coolant (stronger cooling system) and 18% larger heat sink.

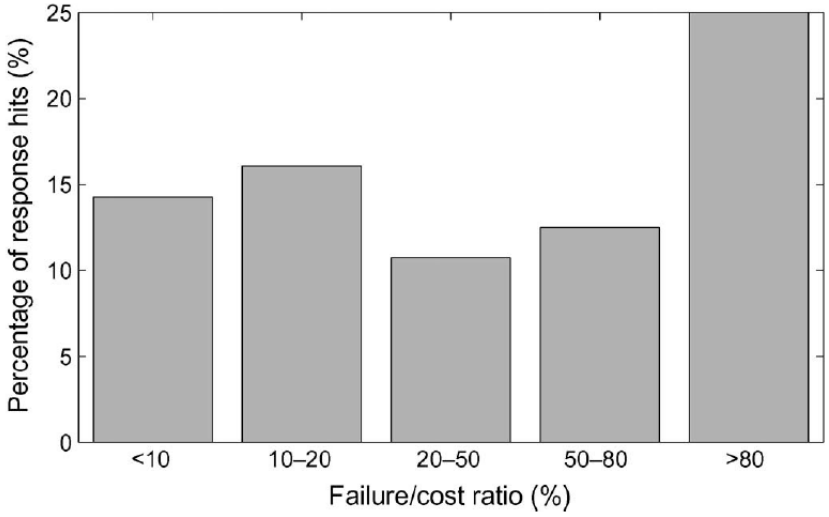


Fig. 1-10. Failure cost distribution [91].

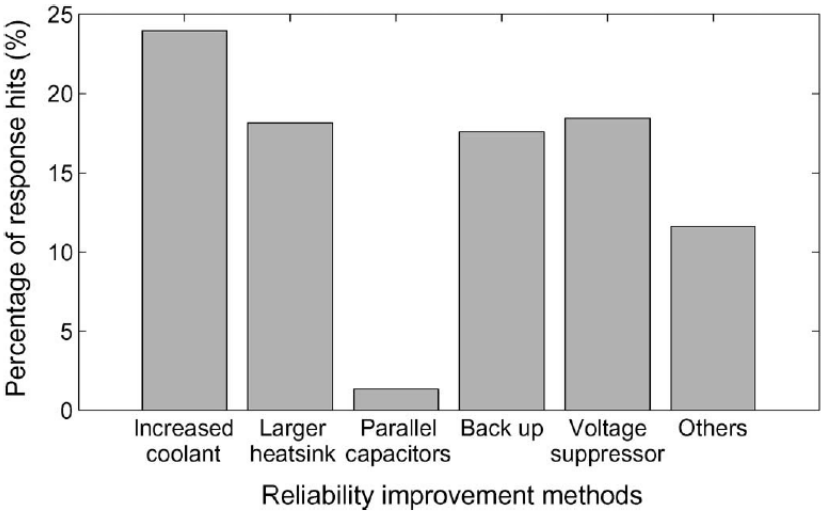


Fig. 1-11. Methods to improve reliability [91].

Fig. 1-12 shows the most fragile power electronic components categorized in distinct applications. In utility power industry and motor drives, power devices (such as IGBTs, MOSFETs, etc.) and capacitors as well are the most fragile components, while resistors and inductors do not play a significant role in the failure occurrence. It is not true in the case of automotive applications in which insignificant capacitor failures have been reported. Accordingly, the most critical power electronic components are totally dependent on the applications and are different form one application to another. However, one can find that power devices and capacitors both play a major part in power electronic reliability in almost all applications [91].

Failure cost to original system cost ratio versus various applications and industries is shown in Fig. 1-13. It reveals that failure occurrence in a power electronic system has a meaningful effect on the maintenance and repair cost. For example, failure cost to original system cost ratio of 80% and above is allocated 7%, 6% and 5% shares in component manufacturers, motor drives and aerospace industries, respectively. Disregarding the industries and applications, failure cost to original system cost ratio of larger than 80% is approximately 25% of all failure occurrences.

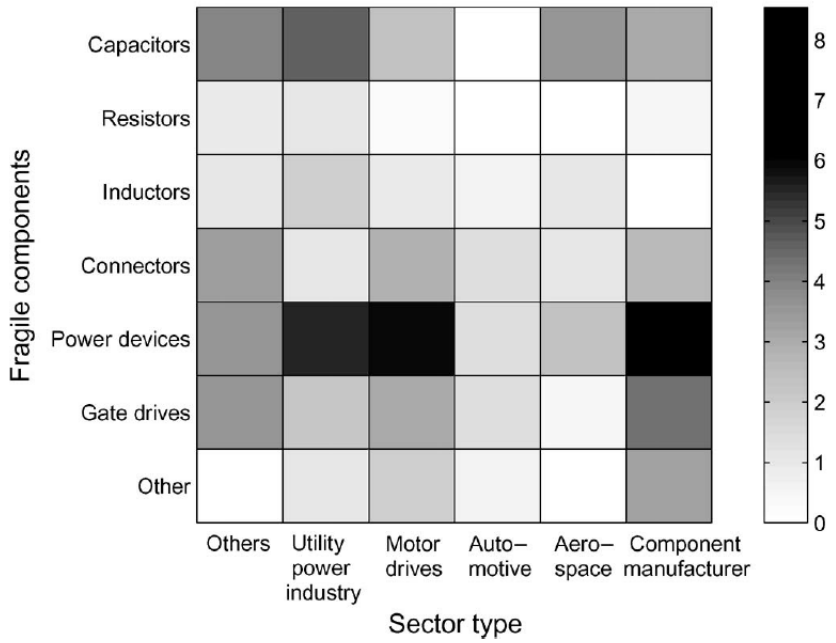


Fig. 1-12. Correlation between various sectors and fragile components [91].

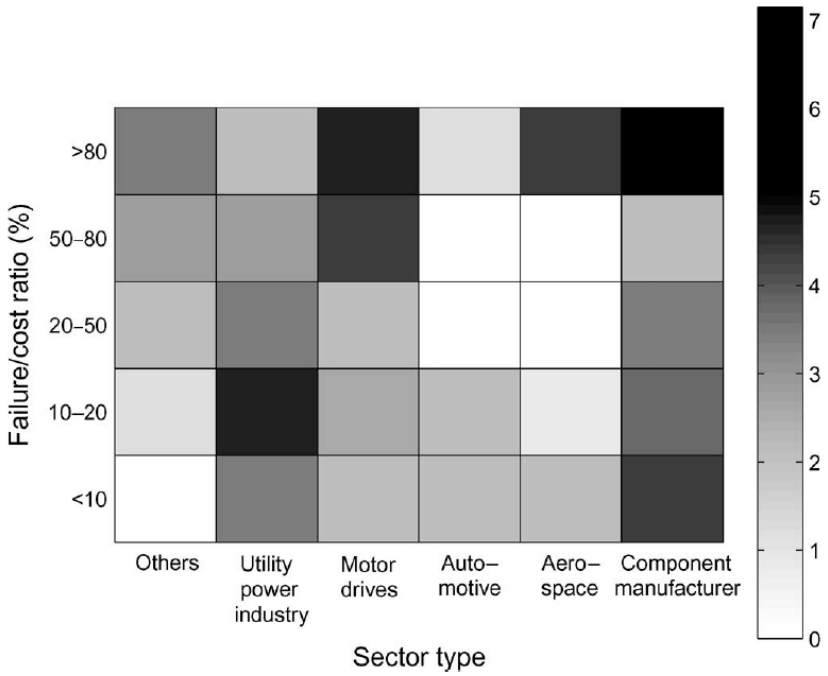


Fig. 1-13. Correlation between various sectors and failure/cost ratio. [91].

It is found that failure costs caused by power devices are highly application dependent. As a comparison, failure costs in utility power industries and consumer electronics are not high owing to redundant designing of power electronic systems. However, failure costs in transport applications, military, aerospace, and motor drives are very high owing to catastrophic results and have unrecoverable effects.

Fig. 1-14 depicts failure cost to original system cost ratio versus different power electronic converters. Regarding Fig. 1-14 and Fig. 1-8, one can find that not only do capacitors and power electronic devices have a lion share in failure occurrence in power electronic systems, but also they allocate the most failure/cost ratio. In different failure/cost ratios, power electronic devices have significant effects.

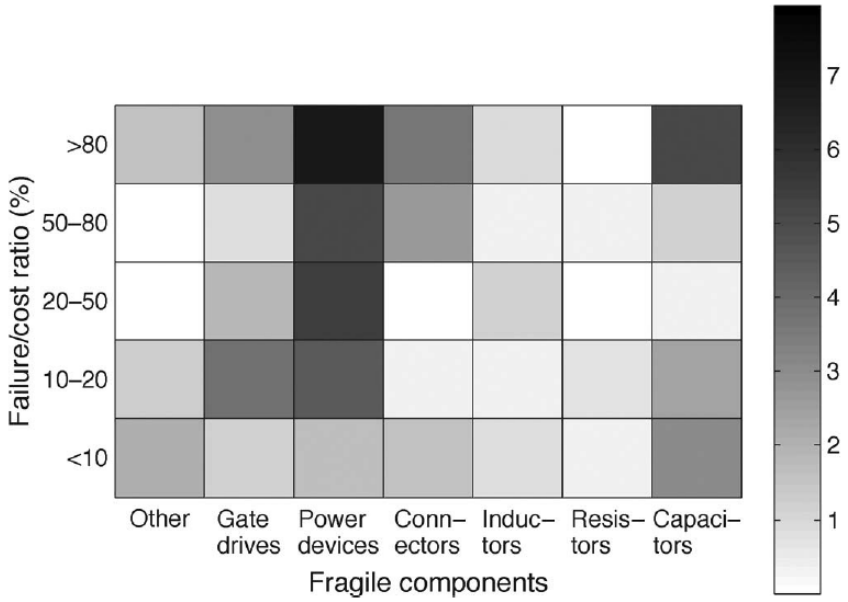


Fig. 1-14. Correlation between fragile components and failure/cost ratio [91].

1-2-3 Power electronic semiconductors main failure mechanisms

Modular and discrete power semiconductors including IGBTs and power MOSFETs are extensively used in high power and low/medium power applications, respectively. As it was previously mentioned, a power converter is one of the most fragile parts of energy conversion systems and among its internal components, power semiconductors are the most vulnerable parts. Power semiconductor devices' failure mechanisms can generally be separated into two categories: chip-related failures and packaging-related failures. In fact, chip-related failures can generally be attributed to catastrophic failures. These kind of failure mechanisms are originated from various factors comprising transient over-voltage, over-current, electrical-over-stress etc. However, due to their short transient process, these failures are included in the protection category and excluded from the focus of reliability research. In this section, the main failure mechanisms in power semiconductors are discussed.

1-2-3-1 IGBT chip fabrication technologies

There are various fabrication technologies for discrete power IGBT fabricating processes. It is clear that the fabrication technology plays a major role in failure occurrence and mechanisms as well. The more types of fabrications, the more failure mechanisms and failure indicators have been created. Since the main failures are directed by package related issues, importance of failure indicators for evaluating useful lifetime seems to be more necessary. Hence, a quick glance on the different type of fabrication technologies has been investigated here. This section has focused on the commonly held belief in failure indicator in discrete IGBTs, namely $V_{ce,on}$ (on-state collector-emitter voltage) variations [132] during its aging for developing devices' lifetime estimation. There are different fabrication technologies including punch through (PT), nonpunch through (NPT), and trench gate field stop (TGFS) discrete IGBTs [132]–[134].

Fig. 1-15 demonstrates these three different internal structures as well as IGBT equivalent circuit. An IGBT can be considered as a MOSFET-controlled bipolar junction transistor (BJT) switch. By MOSFET-BJT modeling (Fig. 1-15a), one can model $V_{ce,on}$ as follows:

$$V_{ce,on} = V_{pn} + V_{NB} + V_{MOS} + V_{contact} \quad (1\text{-}4)$$

where V_{pn} is p^+-n^- junction voltage, V_{NB} (V_{drift}) is the drift region voltage drop (n^- layer), V_{MOS} is the MOSFET region (p-base) voltage drop and $V_{contact}$ is the electrical contact resistance voltage drop. A much more detailed estimation of on-state collector-emitter voltage can be found in [135].

The internal structures (Front End of Line (FEoL)) of three widely used discrete IGBT technologies, namely PT, transparent emitter symmetric structure or NPT, and TGFS are demonstrated in Fig. 1-15b– d. There is an extra n^+buffer layer on top of p^+ -substrate and also higher doping concentration in p^+ substrate in PT technology in comparison with NPT. This additional buffer layer is in charge of declining high-level minority carrier injection from p^+ -substrate into the drift region. Thus, minority carrier lifetime has been reduced and consequently the switching time and the $V_{ce,on}$ have been also declined [135]. Furthermore, temperature coefficient of $V_{ce,on}$ is expressed as a function of collector current for both PT and NPT fabrication technologies . $V_{ce,on}$ of PT IGBT is said to exhibit negative temperature coefficient for relatively wider range of collector current in comparison with NPT IGBT. In NPT IGBT the temperature coefficient has been changed to positive value at far less collector current values (also known as intersection point on the IGBT IV curve). Hence, this makes NPT IGBT much more suitable candidate for thermally coupled parallel solution [134], [136]. While PT technology indicates faster turn-off switching transient and also lower $V_{ce,on}$ voltage drop, NPT technology has better thermal paralleling capabilities. On the other side, trench embedded gate in TGFS

design enhances IGBT channel utilization and conductivity by removing the JFET effect allowing higher cell packing ratio for the same die size [134]. Generally, TGFS technology is known to have faster turn off capability, lower on-state losses (conduction losses), short-circuit robustness, and convenience of paralleling multiple IGBTs [136].

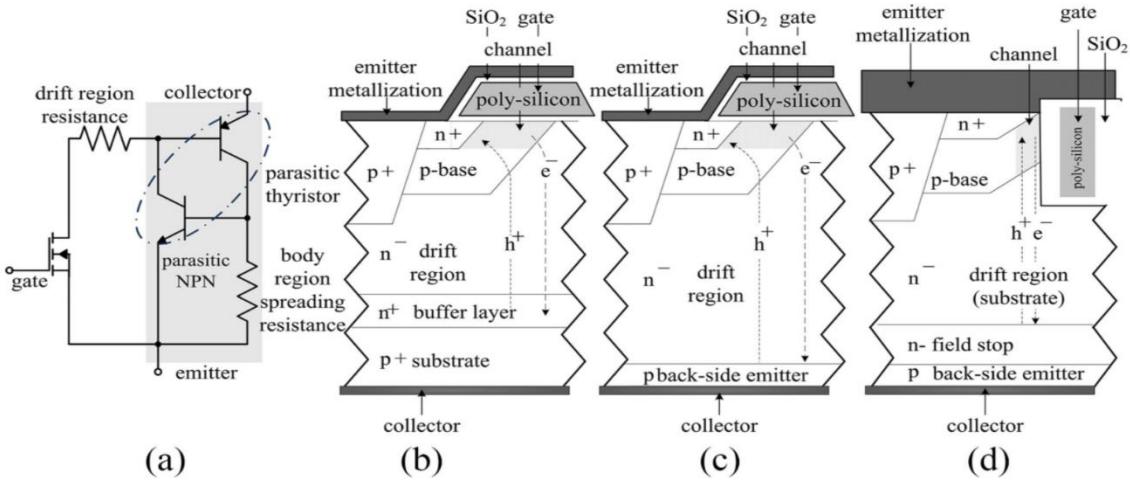


Fig. 1-15. Simplified IGBT device structure: a) equivalent circuit, b) PT, c) NPT, and d) TGFS [133].

1-2-3-2 Packaging structure of power semiconductor

Power semiconductors, especially discrete type, have been widely used in DC-DC power electronic converters. In almost all DC-DC power electronic converters, low or medium power conditioning has been considered and consequently discrete packaging of power semiconductors are of a great interest. Fig. 1-16 depicts the structure of a sample discrete power semiconductor. Regarding this figure, several different components have been used in the power device fabrications and packaging.

The main parts of its packaging are including chip (die), solder, baseplate and bonding wires. Generally, silicon based chip has been used in discrete power devices fabrication due to its technologic maturity. Sn-Ag-Cu based solder (SAC) has been also used in fabrication owing to electrical, mechanical and thermal connections between chip and baseplate. Baseplate is generally made from copper due to its high specific heat rate. Since there is commonly no need for isolating the baseplate from the chip and also it is too costly, direct bonded copper (DBC) has not been employed in contrary to power modules in which it looks essential. There is no DBC layer (isolation substrate), even in “co-PAK” packages in which an antiparallel diode is also included. Accordingly, the chip is directly soldered onto the copper base plate leading to the large difference in coefficients of thermal expansion (CTEs) in comparing to power module containing DBC. In addition, longitudinal dimensions of Si-die and Cu base plate layers produce the maximum shear stress in the die attach interface. It stands to reason that in the absence of DBC layer, thermal

transient (thermal capacity and thermal time constants) are much faster leading to the accelerated degradation of die attach.

Another important part is bonding wires being in charge of electrical connection between emitter and gate to their corresponded leads (in the case of discrete IGBT). These wires are made of aluminum owing to their flexibility and their electrical and mechanical properties. The number of power bonding wires totally depends on the power ranges and lies between 1 to 3 wires. There is a thin aluminum metallization between the bonding wires and chip surface for simplicity of soldering processes. There is also an epoxy protection layer for avoiding external damages.

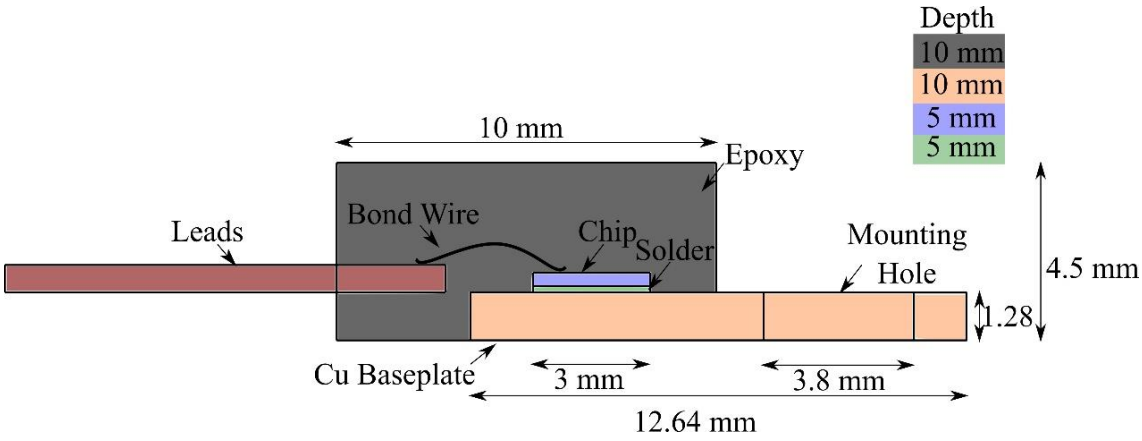


Fig. 1-16. Structure of sample discrete power devices

1-2-3-3 Chip related failure mechanisms

It was mentioned that chip-related failures are generally leading to catastrophic failures and have to be eliminated by either hardware or software protection systems or algorithms. Thus, these kind of failure mechanisms are included in protection category and excluded from reliability issues in power electronic converters. There are several chip-related failure mechanisms including time-dependent dielectric breakdown (TDDB) [137], latch-up [138] and secondary break down [139], aluminum electromigration (Al EM), copper electromigration (Cu EM), Aluminum and Copper Corrosion , Aluminum Stress Migration (Al SM), Copper Stress Migration (Cu SM), hot electrons, delamination of die, Conductive Filament Formation and Stress Driven Diffusion Voiding. These failures typically occurr in die, dielectric layer (oxide layer) and metallization and lead to gate control loss, burnout and short circuit. Investigating on this sort of failures are completely beyond this study and interested readers are referred to [43], [140].

1-2-3-4 Package related failure mechanisms

We will discuss about package related failure mechanisms which are the main object of this study. Although there are different failure mechanisms likely occurring in power semiconductors, especially discrete power IGBTs, regarding the critical stressors, namely steady state temperature and temperature swings [40] (see Fig.

1-8b), only the two main probable failure mechanisms are discussed here. It was mentioned that the main parts in the packaging of a discrete power semiconductors are including bonding wire, die attach (chip solder) and aluminum metallization. All of these three parts are in charge of electrical/mechanical/ thermal connections in IGBT packaging and package failure mechanisms are implied to these parts.

1-2-3-4-1 Electro-thermo-mechanical fatigue failure mechanism

This section concerns the phenomenon of fatigue damage happening when power semiconductors are subjected to cyclic loadings. One can describe fatigue phenomenon by splitting the domain of the numbers of cycles to rupture into three various parts corresponding to different strain behaviors and also different fields of applications: first, elasticity corresponds to relatively small stress amplitudes which induce large numbers of cycles to failure (see elastic behavior in Fig. 1-17). Generally, it has been called "high cycle fatigue"; second, elasto-plasticity corresponds to stresses above the yield stress which induce lower numbers of cycles to failure. Generally, it has been called "low cycle fatigue"; third, elasto-visco-plasticity also implies to small number of cycles to failure.

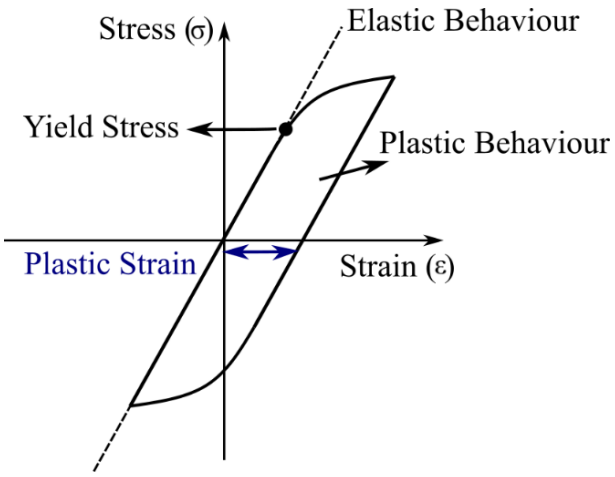


Fig. 1-17. Typical stress-strain (σ-ε) curve for a material.

From a physical point of view, the repeated variations of stress may induce in metals alternate plastic strains producing internal micro stresses responsible of microdecohesions by slip band arrests. The initiated micro cracks grow either inside the crystals or along the grains boundaries, depending on the materials and the loadings, up to coalescence corresponding to initiation of a mesocrack. Plastic strain and stress both participate in this phenomenon.

As previously mentioned, power semiconductors are employed in various electrical operating points and conditions e.g. mission profile. Thus, they are exposed to different thermal cycling owing to their power losses made in the chip junction. Regarding physical structure of power semiconductors comprising various layers as shown in Fig. 1-16 with different

CTE from 2.6×10^{-6}/K for silicon to 17×10^{-6}/K for copper and 22.3×10^{-6}/K for aluminum, a meaningful set of shear and normal stresses are induced in these layers [96], [132]. Thereby, electro-thermo-mechanical stresses have been occurred during the power semiconductor operations. Thus, power loss in any kind of power semiconductors is found to be one of the main drivers for thermal cycling range.

A repetitive set of shear and normal stresses either in elastic and plastic regions of materials are induced in materials (power semiconductors) by electro-thermo-mechanical behaviors of devices. These stresses are led to elastic and plastic strains occurrence in the materials and eventually lead to produce fatigue phenomenon along with the materials of power semiconductors. After a large number of cyclic stresses, material may be fatigued due to the void coalescence and crack growth.

Temperature variations can be translated to compression and tensile stresses along with materials owing to the multilayer structures as described in the previous sections. One can explain the effect of thermal cycling using a typical stress-strain curve as shown in Fig. 1-17 [40]. σ and ε are defined as the cyclic stress and irreversible/reversible strain (plastic/elastic deformations). Source of cyclic stresses are belonged to the temperature cycling in the material. There would be a little damage at a low cyclic stresses (below σ_{yield}) leading to the reversible strain deformation here before called **high cycle fatigue**. However, a much higher damage occurred whenever cyclic stresses are above yield stress (this yield stress is different from one material to the others) leading to much more strain with the irreversible strain and deformation. Eventually, these kinds of deformations gradually either produce some micro cracks and micro voids or grow pre-induced micro cracks and micro voids. This kind of stresses are called **low cycle fatigue**.

High/low cycle fatigue both can influence the health of power devices such as IGBT. Micro cracks production and growth as well as voids creation and coalescence can affect the performance of any parts of packaging in a discrete power chip comprising bonding wires, aluminum metallization, die attach to the baseplate, etc.

1-2-3-4-2 Solder joint creep-fatigue failure mechanism

In general, the time-dependent strength of most materials deteriorates with the increase in the operating temperature. The creep and creep-fatigue failures are the events that activated with the rise in temperature above the one-third of melting point of metals. The mentioned events are intensified upon passing of the time, when high temperature induces viscous effects to the materials. From a physical viewpoint, the evolution of creep damage includes the formation and growth of micro-voids, micro-crack formation at inter-granular sites and their coalescence in the crystals triple points. It is also suggested that the formation of inter-granular micro-cracks under fatigue cycles can develop among the grain boundaries and interact with the defects caused by the creep event. This interaction is nonlinear and

the effects of accumulated damage are associated with the materials properties, environmental conditions, system design and etc.

Regarding low melting temperature point of die attach (solder joint between chip and baseplate), the most fragile part in the discrete power semiconductor is undoubtedly the solder joint (die attach), as a creep-fatigue failure mechanism point of view. Due to their low cost and high mechanical properties, Pb-Sn based solder materials have been a long time applied to interconnect different components in power electronic packages. Nevertheless, the toxic nature of lead affects the human health and the environment. Hence, a wide interest has been taken by researchers to develop Pb-free solders with different chemical compositions [141]. In recent years, SAC based solder materials with low melting point and superior mechanical properties have been proposed in the electronic industry. However, their reliability properties, including fatigue resistance and creep behavior (due to its lower melting temperature), play a major role in the usefulness of power electronic packages. The difference in CTE of components along with the thermo-mechanical stresses during the operation lead to a creep-fatigue event into the system. In the meantime, it was found that the solder joints are the most vulnerable parts for the damage initiation and the failure [142], [143]. In order to evaluate the reliability of solder joints under thermo-mechanical loading, it is required to analyze the creep behavior of the solder and then the produced strain takes into account of fatigue evolution.

Recently, several studies have been published on the constitutive equation for creep strain analysis of SAC solders [144], [145]. Among them, Garofalo-Arrhenius creep model is one of the most applicative constitutive models for evaluation of SnAgCu solder joints [146]. This model proposes a hyperbolic sine creep equation to model the creep event of the solder joints. The following equation demonstrates the steady state creep strain rate [147]:

$$\dot{\varepsilon}_{cr} = A_1\left[\sin\left(\alpha\sigma\right)\right]^n \exp\left(\frac{-Q}{kT}\right) \tag{1-5}$$

The mentioned equation should be re-written into the following format to adapt with the input for implicit Garofalo-Arrhenius creep model [147]:

$$\dot{\varepsilon}_{cr} = C_1\left[\sin\left(C_2\sigma\right)\right]^{C_3} \exp\left(\frac{-C_4}{T}\right) \tag{1-6}$$

$\dot{\varepsilon}_{cr}$ is the creep strain rate and C_1, C_2, C_3 and C_4 are constant values for SnAgCu solder [146]. The creep event is the primary damage mechanism for Sn-based solder joints under thermal cycling [148]. Hence, it is theoretically necessary to consider the creep deformation in the life prediction model.

Many studies have been done to evaluate the effects of thermo-mechanical cycling on the reliability of solder joints in electronic packages. Here we mention some of

these works to elucidate the effects of thermo-mechanical events on the performance of power electronic packages. Zarmai et al [149] investigated the thermo-mechanical response of solder joints in a crystalline silicon solar cell assembly using Garofalo-Arrhenius creep model. Their results indicate that the joint dimension plays a vital role in the thermo-mechanical reliability of solder joints. Talebanpour et al [150] investigated the influence of thermal-mechanical history on the creep behavior of Sn-based solders. It was found that during power cycles ranging from 0.44 to 0.8 T_m, the thermal cycling reliability of power electronic packages was steeply declined. Le et al [151] indicated that process-induced voids acts as a key role in the creep-fatigue lifetime of solder joints of a power module. The voids are the potential sites for the concentration of stress and crack initiation in the solder joints. There are also some other works modeling and demonstrating the role of primary voids trapped in the solder material [152]–[154]. Zhang et al [155] used finite element simulation and showed that the maximum stress concentrated location established a relationship with heights of solder joints. Chen et al [156] proposed a model to evaluate the coupling damage effects of low cycle fatigue and creep events under thermal cycling of an electronic device. Their case study on a lead free solder joint validated the damage model. Coffin-Manson method was used to evaluate the solder joints in a package-on-package structure [157]. It was reported that the maximum inelastic hysteresis energy accumulated on the solder joints in the bottom fine-pitch ball grid array structure. The thermal-fatigue crack also initiated in the two symmetrical corners of solder balls in fine-pitch ball grid array structure. Zhang et al [158] applied simulation along with Taguchi method to study the thermo-mechanical reliability of solder joints in FGBGA device subjected to a thermal cyclic loading. They revealed that the solder material is the most significant factor among the control factors in the device. Baber and Guven [159] proposed peridynamic approach to predict fatigue lifetime of solder joints. This approach expresses that the material degradation through energy dissipative mechanisms plays a key role in crack initiation and propagation and the cracks follow paths similar to cracks produced under quasi-static cycling. Metais et al [160] proposed a viscoplastic-fatigue-creep damage model based on a non-linear mechanical behavior of solder at the beginning of deformation as well as during continuous cyclic aging. Material modeling concentrated on the interpretation of the complicated interaction between fatigue and creep and viscoplastic processes. Their results had a good agreement with the experimental works.

1-2-3-5 Failure events

In the previous section, critical and potential failure mechanisms based on the empirical and physical studies have been investigated and revealed that electro-thermo-mechanical fatigue and creep-fatigue failure mechanisms both are trigged whenever power devices are subjected to temperature cycling which is the case in

all power electronic converters. In the proceeding section, we concentrate on the events, effects and sites of these failure mechanisms occurrences in the power discrete semiconductors. Three most common failure mechanism events have been reported in significant studies categorized as aluminum reconstruction [161], bond wire cracks and lift-off [162], solder joint degradation [163] occur simultaneously. The compression and tensile stresses in both chip and packaging parts cause deformation and degradation [136], [164].

1-2-3-5-1 Bond wire

Degradation and failure events commonly reported is bonding wire cracks and lift-off [165]. Fig. 1-18 illustrates bonding wire cracks of an aged discrete IGBT. Bonding wires are typically made from aluminum and are in charge of electrical connection from top layer of power semiconductor, namely Emitter. These wires and their pads are much close to the active die subjected to higher thermal swing. Since there is a yawning difference between their coefficients of thermal expansion and silicon's, bonding wires experience much higher electro thermo mechanical shear and normal stresses. This event signifies considerably at higher switching frequencies in which the skin effect (or ac resistance) reduces the effective cross-sectional area of the conducting path leading to a non-uniform heat distribution. Consequently, a micro crack may grow at the bond wire heel and propagate till a lift off occurs [166].

1-2-3-5-2 Aluminum reconstruction

As it was mention, there is an aluminum metallization on the top surface of the chip for simplifying electrical connection to the bonding wire and also packaging. Aluminum reconstruction is the degradation mechanism occurring at high temperature owing to the significant difference in the CTE of aluminum 22.3×10^{-6}/K and silicon 2.6×10^{-6}/K (see Fig. 1-19) [38], [132]. Owing to this considerable disparity, thermal cycling at significantly higher temperature develops tensile stresses on the metallization surface. These tensile stresses can lead to Al grains extrusion at the grain boundaries provided that the stresses go through plastic region. This develops discontinuity in the conduction path for the electrons through the material and eventually increases the Al sheet electrical resistance leading to an increase of $V_{ce,on}$ [166].

1-2-3-5-3 Solder degradation

One of the most critical failure events is undoubtedly die-attach or solder joint degradation [132]. Regarding to the low absolute melting temperature and significant CTE disparity between Si chip and copper base plate, both creep-fatigue and electro thermo mechanical fatigue failure mechanisms play major roles in solder degradation [39], [135], [167]. Die attach degradation increases both the electrical resistance and thermal impedance [168]–[170]. Fig. 1-20 depicts solder joint in the case of new and degraded devices. At lower switching frequencies,

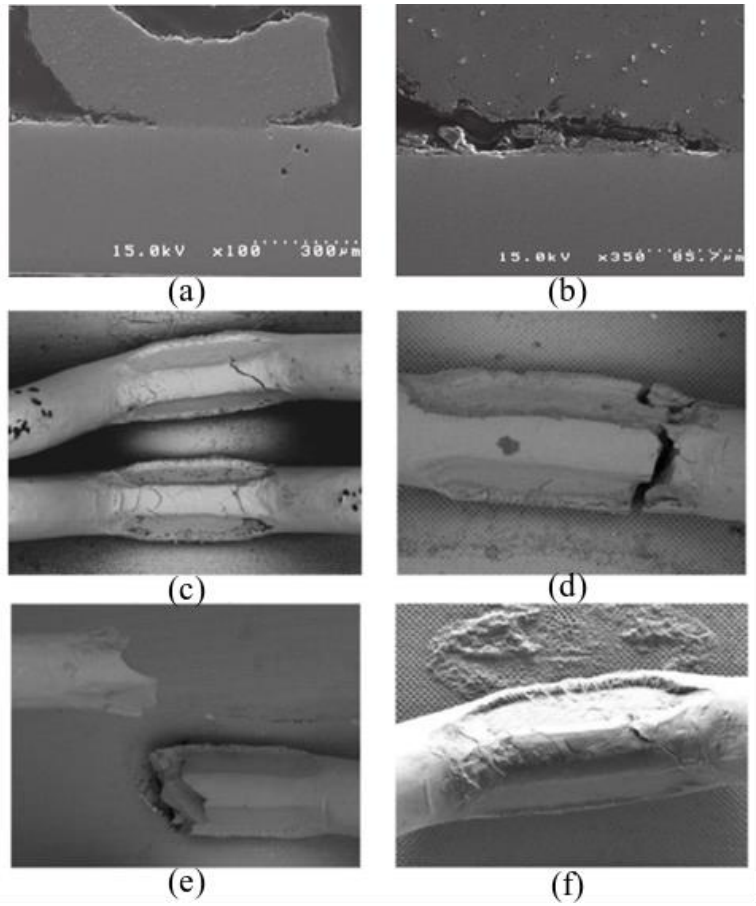


Fig. 1-18. Damaged bonding wire. a) Cracked bonding wire full scale cross section [133], b) zoomed-in scale of (a) [133], c) foot crack [165], d) heel crack [165], e) fracture [165], f) lift off [165].

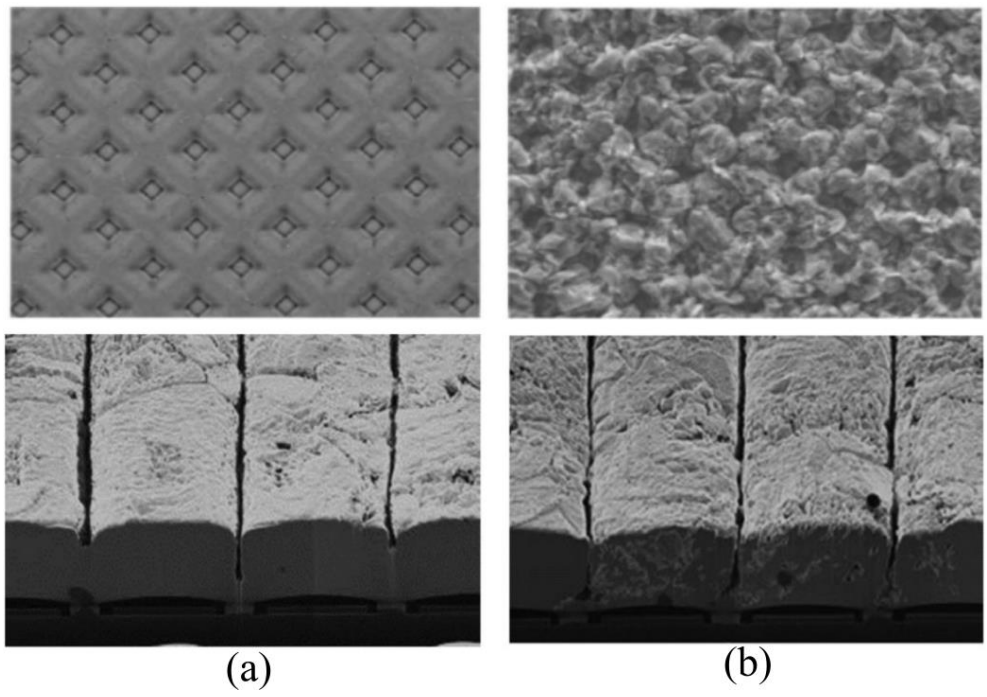


Fig. 1-19. Damaged aluminum metallization. a) New device, b) Aged device [165, 39].

deterioration of die attach is much faster than that of in bonding wires owing to much larger contact surface between the die and the baseplate leading to inducing convex/concave stresses. On the contrary to the power module having isolation substrate, namely DBC, magnitudes of shear and normal stresses increase owing to larger mismatch between the CTE of copper and silicon in discrete power semiconductors. While in the power module the range of isolation substrate CTE lies within $4 \sim 7.1\times10^{-6}$/K (which is closer to to 2.6×10^{-6}/K) leading to much lower shear and normal stresses. In addition, the thermal dynamics of discrete devices is much faster than power module devices due to the absence of DBC layer (mass reduction of discrete devices in comparison to power module devices). Hence, faster die attach degradation is expected in comparison to bonding wire degradation at lower switching frequencies.

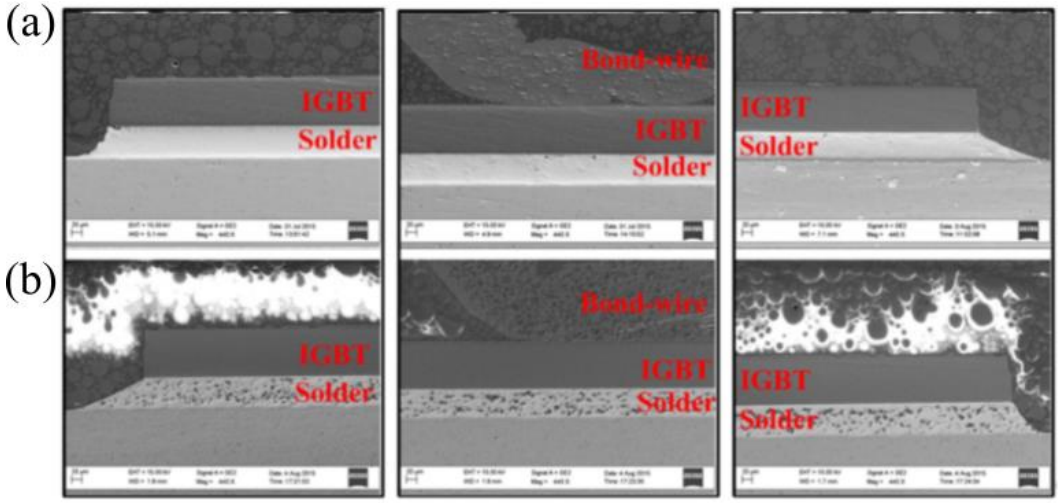


Fig. 1-20. Solder joint. a) New device, b) Aged device [170].

1-2-3-6 Power semiconductor failure modes (parameter drifting)

As it was mentioned, three different failure modes, namely open circuit, short circuit and parameter drifting, are common in power semiconductors both in power modules or discrete chips. Open and short circuits are categorized in catastrophic failures being expected that protection system controls them either by software algorithm or hardware equipment. Last but not least is the parameters drifting playing a major role in failure definition. In the literature, several parameters drifting, namely gate threshold voltage ($V_{G\text{-}TH}$), input/output/reverse capacitances (C_{ies}, C_{oes} and C_{res}), on-state collector-emitter voltage drop ($V_{ce,on}$), breakdown voltage (BV_{CES}) and thermal resistance have been reported [133]. Although, gate threshold voltage ($V_{G\text{-}TH}$), input/output/reverse capacitances (C_{ies}, C_{oes} and C_{res}) and breakdown voltage all vary during aging, on-state collector-emitter voltage drop ($V_{ce,on}$) and thermal resistance are common parameter drifting in discrete power devices (IGBTs and diodes) and can significantly affect devices performances during its aging [133]. Thus, hereafter, the main focus of this study is allocated to them.

1-2-3-6-1 On-state collector-emitter voltage drop

Since $V_{ce,on}$ is a well-known failure indicator in discrete IGBT, its trend during the discrete IGBT aging is paramount of importance. As it was illustrated in Fig. 1-8b, steady state temperature and temperature cycling are the main stressors in power semiconductors leading to thermo mechanical creep-fatigue failure mechanism (it will be thoroughly discussed in the next sub-sections). Accordingly, $V_{ce,on}$ variation as a main failure indicator in the discrete power IGBT during its thermal aging has to be expressed for all different fabrication technologies, namely PT, NPT and TGFS.

Empirical aging tests performed in [132]–[134] revealed a considerable data about on-state voltage trend in discrete power IGBTs. Dusmez et. al [134] demonstrated that there is a tangible decreasing trend in the on-state collector-emitter voltage in PT technology while with a little lower decreasing trend in NPT and TGFS technologies at **high temperature** (around 200°C). However, this trend converts to an increasing trend before the complete device failure [132]. Fig. 1-21 illustrates the aging test results of various discrete IGBTs in the specified testing conditions shown in the figure.

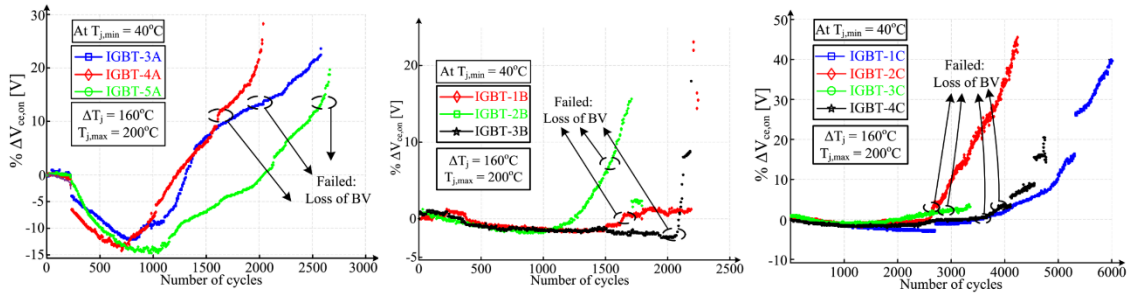


Fig. 1-21. On-state voltage drop measurement during aging test. a) PT, b) NPT, c) TGFS [134].

In other studies, various trends have been reported. As an example, strictly increasing on-state voltage trend has been reported for different junction temperature swing in [165] while a decrease in the on-state voltage value at the end of power device lifetime compared to its initial value has also been reported in [138], [163].

In discrete IGBTs, it has been said that there is a "dip before rise" in the on-state collector-emitter voltage during its aging [133]. There are two competing physical phenomena (mechanisms) in which at the beginning there is sag and then increasing region reveals in the $V_{ce,on}$. Normally, it is expected to observe an increased electrical resistance with respect to aging. It is well-known that crack growth and void coalescence in the contact area under thermo mechanical stresses lead to an increase in electrical contact resistance. However, it is not the case in all IGBT fabrication technologies as shown in Fig. 1-21. Thus, on-state voltage variation is prompted by two competing degradations, namely thermal or electrical impedances. Die attach deterioration causes thermal impedance degradation

leading to a junction temperature rise and intrinsic carrier concentration [171], which subsequently lowers on-state collector-emitter voltage reaching the minimum value of $V_{ce,on}$. Beyond that minimum value, the increased electrical resistance starts to dominate more and increases the overall $V_{ce,on}$. It is a notable point that increased minority carrier lifetime or reduced gate threshold voltage (owing to the temperature rise) may also decline $V_{ce,on}$. On the other hand, junction temperature rise may decrease the carrier mobility leading to $V_{ce,on}$ increase. Thus, one can divide on-state collector-emitter voltage to two separate components as follows [134]:

$$V_{ce,on} = V_{ce,on+} + V_{ce,on-} \tag{1-7}$$

Two competing failure mechanisms are illustrate in Fig. 1-22. In this figure, two degradations including electrical and thermal impedances are in stiff competition to dictate on-state voltage variation. These physical phenomena are thoroughly dependent on the fabrication technology. That is why there are various trends in $V_{ce,on}$ from one fabrication technology to the others.

Hence, it is supposed that negative on-state voltage temperature coefficient together with degraded thermal impedance is responsible for considerably larger $V_{ce,on}$ sag in PT fabrication technology. On the other side, the positive on-state voltage temperature coefficient compensates $V_{ce,on}$ sag in on-state collector-emitter voltage for NPT and TGFS fabrication technologies as shown in Fig. 1-21.

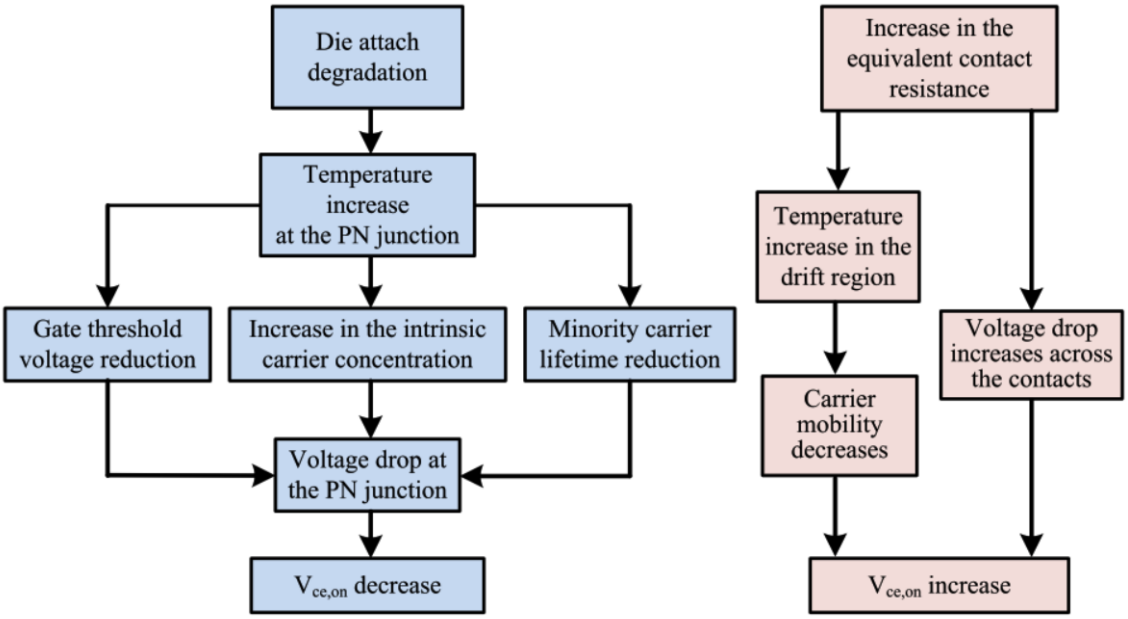


Fig. 1-22. Competing physical phenomena responsible for the Vce, on variation in IGBT [134].

At lower temperature working (around T_{jmax}=150°C), typically electrical degradation dominates thermal degradation. It means that there will be no considerable voltage dip in on-state collector-emitter voltage even in PT fabrication

technology. It is the case also in high switching frequency applications in which bonding wire degradation is predominant and leads to electrical degradation [163], [165], [172].

Fig. 1-23 depicts generic behavior of discrete IGBT on-state voltage during aging for various fabrication technologies at two different working temperatures. Regarding this figure, one can find that in all fabrication technologies and at the lower junction temperature, the trends of on-state collector-emitter voltage are strictly increasing. While, in the much higher junction temperature, $V_{ce,on}$ trend is significantly "dip before rise" for PT series. It is also the case in the NPT and TGFS series but with a very smooth decreasing before rising.

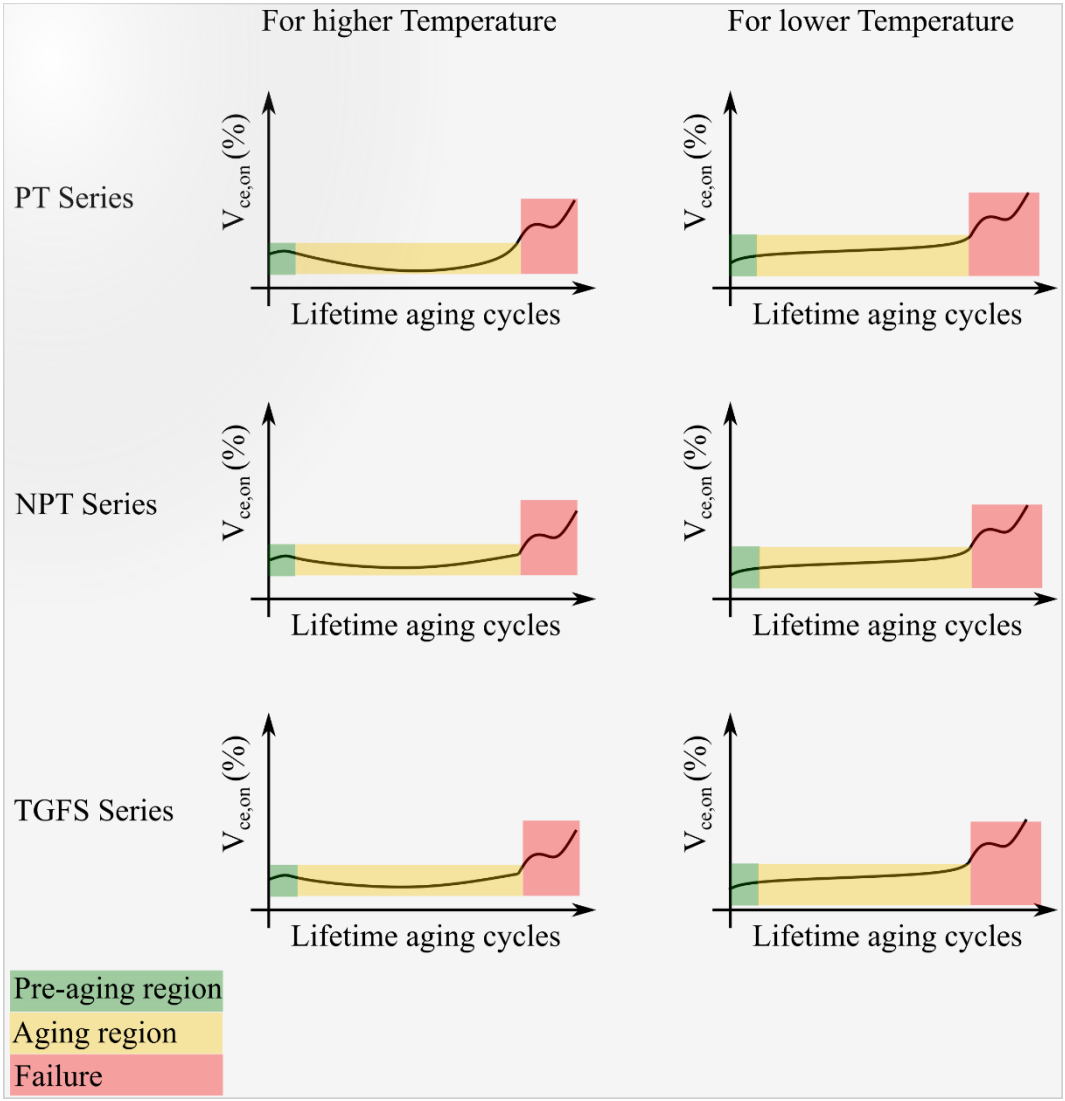


Fig. 1-23. Generic variations in on-state voltage during IGBT aging.

1-2-3-6-2 Junction-case thermal resistance

Another important failure indicator is junction-case thermal resistance. Since one of the failure events during aging is die attach degradation, junction-case thermal

resistance can be significantly affected. Of course, cooling and thermal interface material degradations can also affect junction-case thermal resistance. As previously mentioned, die attach degradation is illustrated by crack growth and void coalescence in the solder joint. Elasto-visco-plastic strain in the solder joint owing to creep-fatigue failure mechanisms is the main factor in the die attach deterioration [172].

Not only is the high junction temperature important, but also the temperature swing plays a major role. Manufacturing process induces stress in the solder joint which is stored as residual stress leading to initial micro cracks and micro voids [172]. The stress close to the crack tips and voids becomes greater than the overall average owing to stress concentration. Therefore, plastic deformation zone is formed around the tip or voids, causing progressive further degradation. That is why there is also plastic deformation (strain) in the solder joint even in the lower temperature cycling. In addition to plastic deformation due to fatigue failure mechanism, creep accumulated strain is also accelerating die attach degradation.

Regarding presence of initial micro voids and cracks, trend of the junction-case thermal resistance has been expected as nonlinear exponential function as reported in [172].

1-2-3-7 Life time model

1-2-3-7-1 Electro thermo mechanical fatigue lifetime model

There are numerous proposed lifetime estimation models for thermal fatigue failure mechanisms [172]. They generally falls into two categories 1) analytical behavior models such as the Coffin-Manson [173], Norris-Landzberg [174] and Bayerer models [175], and 2) physics-of-failure models [175], [176]. The most common and well-known lifetime model is undoubtedly Coffin-Manson lifetime model reported and validated in numerous studies [174], [175]. The model is defined as follows:

$$N_f(\Delta T_j) = A \times \Delta T_j^{\alpha} \tag{1-8}$$

where A and α are both constant and device-dependent. ΔT_j expresses the junction temperature swing of devices in ^oC. N_f is the number of cycle to failure based on the failure criteria definition (for example 20% increase in junction-case thermal resistance). However, regarding the dependency of strain-stress behavior of materials, mean temperature of material during shear stress inducing is paramount of importance. As a sample, Fig. 1-24a demonstrates stress-strain curve of a material. The trace falls into two elastic and plastic regions. Stress-strain behaviors of solder for different temperatures are also depicted in Fig. 1-24b [177]. As it can be seen from Fig. 1-24b, the material temperature has a significant effect on the strain occurring inside the material. Material strain is a key factor in the fatigue aging mechanism. Accordingly, in the same stresses, the created strain in the

material varies significantly with the temperature variations. In such materials that the temperature varies during its loading, the importance of considering time-temperature-dependent mean temperature has become outstanding leading to employ Coffin-Manson-Arrhenius lifetime model [174], [175] as follow:

$$N_f(T_m, \Delta T_j) = A \times \Delta T_j^{\alpha} \times \exp(Q/R_g T_m) \quad (1\text{-}9)$$

where R_g and Q are the gas constant (8.314 $JMol^{-1}.K^{-1}$), internal energy and T_m is the mean junction temperature of devices in Kelvin. Thereby, Coffin-Manson-Arrhenius model has been widely used in the materials whose strain-stress curve are largely depends on mean temperature as the case of solder [177].

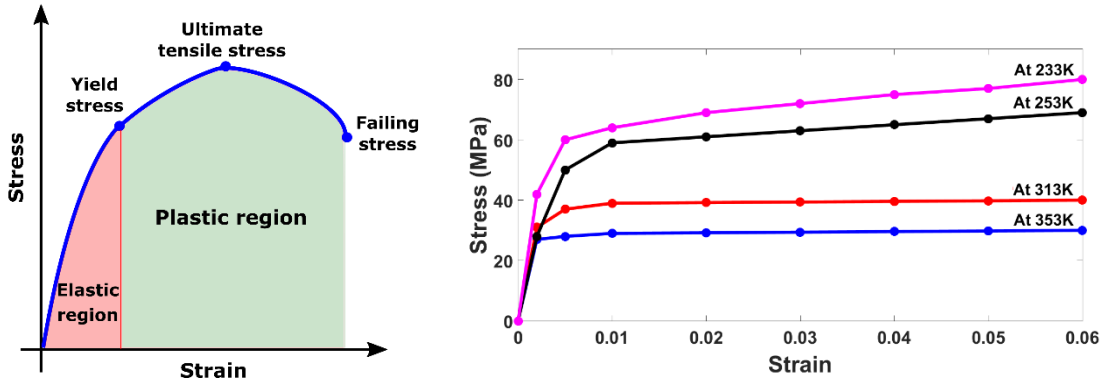


Fig. 1-24. Strain-stress graph. (a) Typical, (b) Temperature-dependent curve of solder based on [177].

1-2-3-7-2 Creep lifetime model

Creep mechanism is one of the most critical aging mechanisms in the material in which the working temperature is sufficiently high and is above the one third of its absolute melting temperature [178]. In the most materials, a temperature increase leads to a decrease in strength of material. In the creep mechanism both the time and the temperature are paramount of importance due to its physical mechanism. Physically, creep degradation in the materials is owing to the propagation and nucleation of micro-cracks and their coalescence to meso-cracks [178], [179].
On the contrary to the low-cycle fatigue damage process, namely load cycles, creep degradation is time-dependent and highly impressed by the dwelling time period [156]. For expressing lifetime model of the materials on the creep failure mechanism, Monkman-Grant (MG) model has been extensively used [180]:

$$\dot{\varepsilon}_{cr}\, t_c^{\beta} = C_{MG} \quad (1\text{-}10)$$

where $\dot{\varepsilon}_{cr}$ is the stable creep strain rate, C_{MG} and β are constant and material-dependent.

Creep strain rate is a function of environmental temperature, applied stress, dwelling time [180]. There are many correlations that can express the creep strain

rate such as Anand, sine-hyperbolic and Dorn [147]. Recently, several studies have been published on the constitutive equation for creep strain analysis of SnAgCu solders [144], [145]. Among them, Garofalo-Arrhenius creep model is one of the most applicative constitutive models for evaluation of SnAgCu solder joints [145]. This model proposes a hyperbolic sine creep equation to model the creep event of the solder joints. The following equation demonstrates the steady state creep strain rate [147]:

$$\dot{\varepsilon}_{cr} = C_1\left[\sin\left(C_2\sigma\right)\right]^{C_3}\exp\left(\frac{-C_4}{T}\right) \tag{1-11}$$

C_1, C_2, C_3 and C_4 are constant values for SnAgCu solder [146]. The creep event is the primary damage mechanism for Sn-based solder joints under thermal cycling [148]. Hence, it is theoretically necessary to consider the creep deformation in the life prediction model. It was previously mentioned and also revealed from equation (1-10) that the creep failure mechanism is time dependent which means that the longer time the material is exposed to the roughly constant temperature, the more degradation occurs. Based on Monkman-Grant model, the dwelling time (Δt) is a key factor in calculating the creep useful lifetime.

1-2-3-7-3 Creep-fatigue lifetime model interaction

Previous works have only been limited to the high/low cycle fatigue by considering only the stress swings and the mean stresses and failed to purpose the dwelling times in which the materials have been rested in the roughly constant temperature. Fig. 1-25 demonstrates a thermal stress as a function of time. As it is shown in the thermal stresses, there can be a lot of dwelling time in which the material is exposed to. Thus, it is thoroughly important to also consider the creep failure mechanism in lifetime estimation. Creep-fatigue coupled analysis is becoming important owing to solder working temperature range.

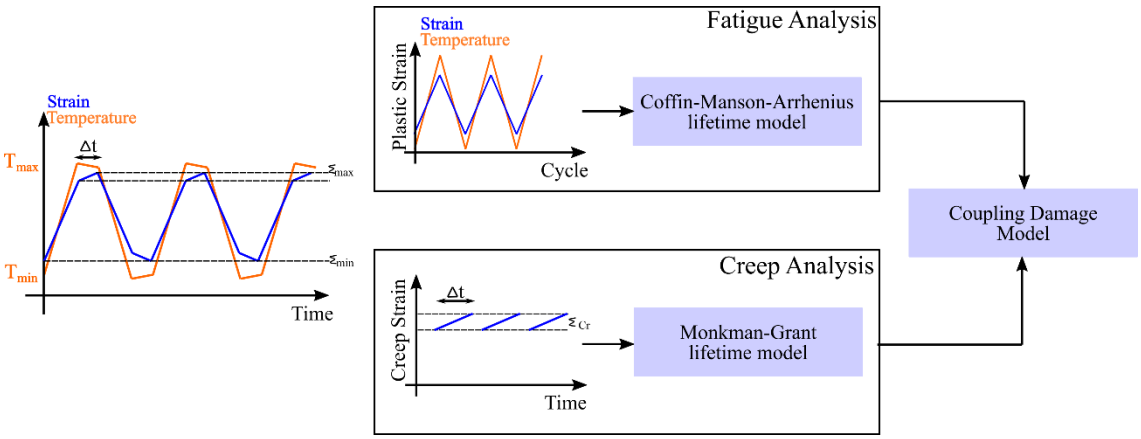


Fig. 1-25. Coupled creep-fatigue lifetime estimation model.

1-2-3-8 Damage models

1-2-3-8-1 Fatigue damage model

Several deterministic damage accumulation models have been proposed mainly fallen into two categories [181], [182]: linear and nonlinear damage cumulative models. Among these fatigue damage accumulation models, the linear damage accumulation theory, also known as Palmgren–Miner's rule [183], is commonly used in analyzing cumulative fatigue damage due to its relative simplicity, close approximation to reality, and widespread knowledge and utilization.
The Miner's rule can be expressed as [134]:

$$D_F = \sum_{i=1}^{n} N_i(T_m, \Delta T_j) \big/ N_{fi}(T_m, \Delta T_j) \quad (1\text{-}12)$$

where D_F is the total linear accumulated damage, N_i is the number of the i^{th} particular cycle, N_{Fi} is the number of cycles to failure of the i^{th} particular cycle and n is the number of distinct cycles which power semiconductors are subjected to.
However, linear cumulative damage have some detriments such as absence of considering load history, load sequence effects and effects of load interaction. Under complex loading, either small cycles or large cycles are dependent on loading interaction, sequence, or memory effects.

Researchers have tried to overcome these detriments by proposing several methods such as Damage theories based on the physical property degradation of materials, Damage curve approaches, Continuum damage mechanics approaches, Damage theories based on energy, Damage theories accounting for load interaction effects, Damage theories based on thermodynamic entropy [184]. Although these methods have been proposed through recent years, they could not satisfy the users due to their complexity and also some disadvantages are reported in [185]. That is why linear damage cumulative method also has taken much interests.

1-2-3-8-2 Creep damage model

There are many damage models available for solder creep damage model. They can be categorized into three groups: creep strain based, creep energy based, and damage accumulation based [147].
The accumulated creep strain and creep strain energy density per cycle are exerted on the fatigue equations to anticipate the lifetime of solder joints. The relation of lifetime to the accumulated creep strain follows as [147]:

$$N_f = (C^*.\varepsilon_{acc})^{-1} \quad (1\text{-}13)$$

where N_f defines the number of cycles to failure and C* introduces inverse of creep ductility. ε_{acc} is the accumulated creep strain per cycle. The following equation gives the dependency of accumulated creep strain energy density on fatigue lifetime [147]:

$$N_f = (W^*.w_{acc})^{-1} \quad (1\text{-}14)$$

w_{acc} is the accumulated creep energy density per cycle and W* defines the creep energy density for failure.

As described, there are several failure models proposing the creep evolution of solder joints under thermal cycling. However, it should be noted that the above-mentioned models rely on the application of accumulated strain or energy during a thermal event into a fatigue model predicting the number of cycles before failure. It is of course very important to choose the best model based on the electronic configuration, thermal cycle range and the environmental conditions to achieve a close prediction for the solder joints.

Damage accumulation model is based on the Monkman-Grant model (1-10). Thus, one can find time per unit creep damage as follows:

$$d_c = \frac{1}{t_c} = \left(\frac{\dot{\varepsilon}}{C_{MG}} \right)^{1/\beta} \quad (1\text{-}15)$$

Accumulated creep damage during the dwelling period under the same condition gives:

$$D_C = \frac{\Delta t}{t_C} = \Delta t \left(\frac{\dot{\varepsilon}}{C_{MG}} \right)^{1/\beta} \quad (1\text{-}16)$$

where Δt is the dwelling time. Creep damage accumulation model has been widely used in several studies and can predict the useful lifetime with an acceptable precision [186].

1-2-3-8-3 Coupled creep-fatigue damage model

Although there are many fatigue-creep damage coupling models such as strain range partitioning, strain energy partitioning, frequency-modified strain-life equation, unified damage and mechanism-based model [187]–[189], the global linear damage model [189] will be assumed and expresses as follows

$$D = D_F + D_C \quad (1\text{-}17)$$

where D_F and D_C are defined by (1-12) and (1-16) respectively.

1-2-4 Power capacitor main failure mechanisms and lifetime models

As previously mentioned, power capacitors are also critical components in power electronic converters as energy savers. There are three various types of power capacitors widely used in power conditioners, namely Aluminum Electrolytic Capacitors (Al-Caps), Metallized Polypropylene Film Capacitors (MPPF-Caps) and high capacitance Multi-Layer Ceramic Capacitors (MLC-Caps) [93], [109], [118]. A

comprehensive description of various types of capacitors has been carried out in [93].

Fig. 1-26 illustrates performance of these various power capacitors. Although, MPPF-Caps have superior performance in the most different aspects such as voltage rating, frequency, reliability, etc, Al-Caps have been widely used due to their energy density, cost and capacitance performances. Regardless of what kind of power capacitors have been employed in DC-DC power electronic converters, their reliability issues have been gaining importance due to the practical and empirical records as published by [91].

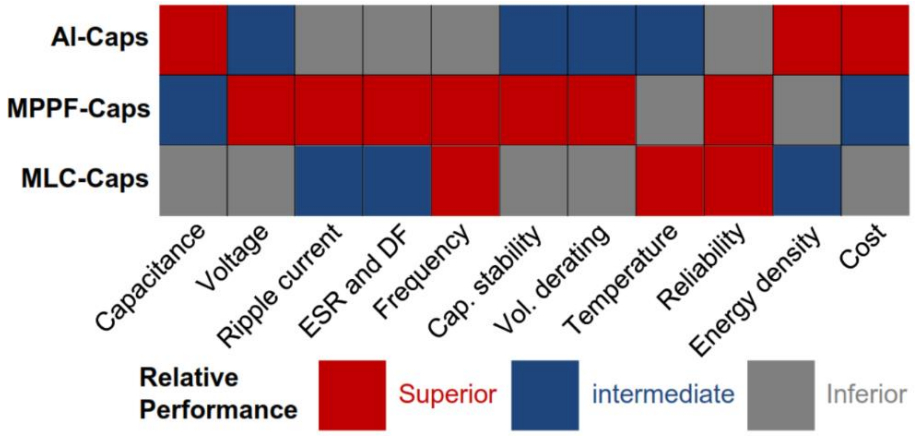


Fig. 1-26. Qualitative comparison of various types of capacitors [93]

Failure modes and critical failure mechanisms in all three capacitors are listed in Table 1-4. Based on these table, parameters drifting including capacitance (C), equivalent series resistor (ESR) are predominant damage indicators in all types of power capacitors. Thereby, C and ESR changes due to aging have to be considered as main failure indicators in power capacitors. Current and voltage ripples and ambient temperature are the most critical stressors in C and ESR drifting in all types of power capacitors.

Equation (1-18) expresses capacitor lifetime model based on the empirical tests describing the influence of temperature and voltage stresses [93].

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \exp\left[\left(\frac{E_a}{K_B}\right)\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \qquad (1\text{-}18)$$

where L and L_0 are the useful lifetimes under the use condition and testing condition, respectively. V and V_0 are the voltages at use condition and test condition, respectively. T and T_0 are the temperatures in Kelvin at use condition and test condition, respectively. E_a is the activation energy, K_B is Boltzmann's constant (8.62×10^{-5} eV/K), and n is the voltage stress exponent. Hence, the values of E_a and n are the key parameters to be determined in the above model and obtained as 1.19

and 2.46 in [190] and 1.3~1.5 and 1.5~7 in [191], [192], respectively . A simplified model from (1-18) is given as follows [193]:

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times 2^{\frac{T_0 - T}{10}} \tag{1-19}$$

For MPPF-Caps, the exponent n is around 7~9.4 used by leading capacitor manufacturers [194]. For Al-Caps, the value of n typically varies from 3 to 5 [195].

Table 1-4. Overview of failure modes, critical failure mechanisms and critical stressors [93]

Cap. type	Failure modes	Critical failure mechanisms	Critical stressors
Al-Caps	Open circuit	Self-healing dielectric breakdown	V_C, T_a, i_C
		Disconnection of terminals	Vibration
	Short circuit	Dielectric breakdown of oxide layer	V_C, T_a, i_C
	Wear out: electrical parameter drift (C, ESR, tanδ, I_{LC}, R_p)	Electrolyte vaporization	T_a, i_C
		Electrochemical reaction (e.g. degradation of oxide layer, anode foil capacitance drop)	V_C
MPPF-Caps	Open circuit (typical)	Self-healing dielectric breakdown	V_C, T_a, dV_C/dt
		Connection instability by heat contraction of a dielectric film	T_a, i_C
		Reduction in electrode area caused by oxidation of evaporated metal due to moisture absorption	Humidity
	Short circuit (with resistance)	Dielectric film breakdown	V_C, dV_C/dt
		Self-healing due to overcurrent	T_a, i_C
		Moisture absorption by film	Humidity
	Wear out: electrical parameter drift (C, ESR, tanδ, I_{LC}, R_p)	Dielectric loss	V_C, T_a, i_C, humidity
MLC-Caps	Short circuit (typical)	Dielectric breakdown	V_C, T_a, i_C
		Cracking; damage to capacitor body	Vibration
	Wear out: electrical parameter drift (C, ESR, tanδ, I_{LC}, R_p)	Oxide vacancy migration; dielectric puncture; insulation degradation; micro-crack within ceramic	V_C, T_a, i_C, vibration

V_C-capacitor voltage stress, i_C-capacitor ripple current stress, i_{LC}-leakage current, T_a- ambient temperature.

1-3 Conclusion and proposed approach

According to the state of art, two different approaches have been applied in reliability assessment of power converters, namely, mathematical and physics-of-failure approaches. They both have their specific advantages and disadvantages. Since, the advantages of physics-of-failure far outweigh its disadvantages, a PoF based reliability assessment would be established through this thesis. In the PoF based approach, identifying failure mechanisms and their corresponding root causes has paramount of importance.

The most fragile parts in the power converter system is power semiconductors and power capacitors. Discrete power semiconductors, especially IGBT and power diode, are exposing to the steady state temperature and temperature swings during their useful lifetime due to their internal power losses or environmental temperature cycling. Based on the failure root causes, two most probable failure mechanisms i.e. electro thermo mechanical fatigue and creep may occur in the different sites of packaging such as bonding wires, aluminum metallization and

solder die attach all at the package level. These deteriorations finally lead to the parameter drifting in the power semiconductors deviating thermal and electrical operating points and subsequently accelerating their aging. It is also the case in the power capacitors, in which ESR and capacitance deviations may lead to operating point changing and consequently power capacitor accelerated aging.

In the previous reliability assessments of power electronic systems which have been deeply focused on the capacitors and the power semiconductors useful lifetime estimations based on the physics of failure, researchers have been wrestling with some significant detriments. Lack of consideration of the dependencies of the components in both approaches, lack of consideration of the mission profile in mathematical approach and inability of tackling system-level reliability evaluation as well are all facing challenges. The thrust of our argument is to merge all the advantages of both approaches by developing physical reliability assessment approach.

By time passing, it is clear that the degradation process of a component or a system might be accelerated owing to the aging. Accordingly, static reliability assessment has not been able to estimate the reliability of a system and some dynamic reliability assessments seem to be required. For mitigating the problem of system-level reliability assessment, consideration of self and mutual degradation effects (dependencies), degradation level (states) and consideration of mission profile have to be put forward.

The objectives of this thesis are to integrate the pros of both mathematical and physical methods and also tackling their detriments. In the proposed method, mission profile of undertaken system has been considered and applied to a multistate degraded system. This approach tries to consider the dependencies between the power components by defining a finite number of states for the global system. In the other word, this method converts a dependent system to the multi-state independent system by discretizing the global system state to the specific state space. In each state of the global system, detached operating conditions are assumed. Accordingly, in addition to the aforementioned challenges, this method is capable of analyzing time-varying failure rate. System-level reliability assessment is also achievable using proposed method.

In the proceeding chapter, electrical, thermal and power loss modeling of DC-DC boost power converter as a case study will be discussed. In this chapter, TIMF modeling capable of evaluating states' ripples has been investigated. Iterative power loss calculation is also expressed. Chapter three deals with the experimental procedure and their results including TSEP test, customized DC-DC boost power converter, accelerated power cycling aging test, accelerated thermal cycling aging test. A newly proposed cycle counting algorithm capable of considering time-

temperature mean value and creep-fatigue failure mechanism is launched in chapter four. Chapter five is expressing the reliability assessment of 3000W 200V/400V DC-DC boost power converter as an interface power conditioner in an HEV exposing to WLTP driving cycle. In this chapter, the reliability assessment falls into three categories, namely conventional physical approach, interval reliability analysis and multi state degraded reliability assessment. Finally, a conclusion and summary is drawn in the last chapter.

2

Modeling Approach

Thermal induced failure mechanisms play major roles in aging of power devices. It was mentioned that two critical components, i.e. capacitors and power semiconductors, have been undertaken. In this study, a conventional DC-DC boost converter has been considered as a case study for reliability evaluating. Electrical operating point (EOP) and thermal operating point (TOP) are important in the aging evaluation of power components. As a perfect example, power semiconductor lifetime model is based on the Coffin-Manson-Arrhenius lifetime model (described in chapter 1) correlated to the mean junction temperature and junction temperature swing. Since junction temperature has been induced from power loss and power loss is TOP- and EOP-dependent, electrical, power loss and thermal modeling of power electronic converter are grasping importance. In this chapter, electrical, power loss and thermal modeling of a conventional DC-DC boost converter will be thoroughly discussed. Electrical modeling deals with newly proposed electrical analyses capable of well ripple estimation. Voltage and current ripples estimations play a meaningful part in the power loss modeling of power semiconductors. Complete thermal modeling of global thermal system, considering coupling effect, and its validation through finite element simulation will be discussed in the last section.

2-1 Electrical modeling

2-1-1 Introduction

Electrical modeling along with its controlling system analyzing plays a significant part in the power conditioning and reliability assessment. EOPs and their dynamics have to be taken into consideration in-detail for making the reliability assessment much more accurate and realistic [196], [197]. Therefore, electrical modeling has a significant contribution in the reliability evaluation. A power electronic system is inherently containing time dependent behavior owing to its internal components as well as external load or supply variations. In a switching period, almost all the active switches such as IGBT, Diode and power MOSFET change their state from conducting to blocking or vice versa resulting in time varying power electronic system. Accordingly, one can consider that a power electronic system is a linear time

varying (LTV) system [198], [199]. Therefore, we encounter an inherent LTV system and should employ some approaches to accurately solve this system.
Generally, power electronic systems solving approaches fall into two main categories: linear time varying (LTV) and linear time invariant (LTI). Due to its inherent feature, a power electronic system is an LTV system. However, there are lots of methods making this LTV system change to a LTI system [200]. This section touches the issues related to the electrical modeling of a power electronic system. Owing to the their simplicity and convenience, author takes up the position that LTI approaches can be more efficient and accordingly only concisely draws an analogy between LTV and LTI approaches.

Firstly, circuit design consideration has been done based on the state space averaging model (see Fig. 2-1). It is worth mentioning that active components of these DC-DC converters are taken into account as IGBTs and their anti-parallel internal diodes (see Fig. 2-2). Secondly, regarding the equivalent circuit of DC-DC boost converter in both IGBT conduction and blocking states in a switching period, its time varying state space equations would be obtained. In this case, parasitic components which have paramount of importance in reliability assessment are taken into account (see Fig. 2-2).

Next, based on the above-extracted state space equations, some LTV approaches and LTI approaches have been thoroughly investigated and the parallels and distinctions between these two approaches have been briefly drawn. Regarding to the significant numbers of components which can be individually affect the whole reliability assessment, we lay emphasize on that the chosen approach should have sufficient simplicity and accuracy.

Then, one of the LTI approaches, namely time invariant multi-frequency (TIMF) approach, has been employed for solving the time varying state space equations. In this section, TIMF will be fully illustrated and applied to our considered converter. For having an acceptable accuracy, third-order TIMF will be applied. In addition, the results of this method have been compared to the detailed switching simulations in MATLAB environment.

Due to the aging, the electrical parameters deviations such as capacitance decrease, equivalent series resistance of capacitor increase and on-state voltage drop of IGBT and power diode can affect the reliability assessment. Therefore, one should investigate via electrical modeling whether or not these deviation can influence reliability evaluation. As it was mentioned, thermo mechanical failures have been considered as main failure mechanisms in the discrete IGBT and diode. Accordingly, we should deeply concentrated on this issue that how electrical parameters deviations can affect the thermal behavior (mainly power loss) of DC-DC boost converter.

Considering parasitic components (non-idealities) is important in electrical modeling. Although, there are numerous parasitic components, only inductor series resistor, saturated collector-emitter voltage, IGBT internal resistor, diode forward-bias voltage along with its internal resistor and equivalent series resistor of capacitor are considered here because of their knock on impacts on the converter's operating point. All of the analyses are based on the following assumptions and constraints:

1- Power IGBT is modeled as an open circuit in off-state and a constant collector-emitter voltage source V_{CE0} as well as a constant resistor r_Q in on-state.
2- Power Diode is modeled as an open circuit in off-state and a constant forward voltage source V_{D0} as well as a constant resistor r_D in on-state.
3- All of the passive components are supposed to be linear and time-invariant. In a specified switching frequency, inductors and capacitors are modeled with an ideal inductor in series with a resistor r_L and with an ideal capacitor in series with an equivalent series resistor r_C.
4- Power consumption of control circuit is not considered.
5- Power losses of components have been considered.

2-1-2 Ideal DC-DC boost converter analysis

In this section, steady state behavior of an ideal DC-DC boost converter has been analyzed. This study will be focused only on the continuous conduction mode (CCM). However, one can also easily extract the expressions in discontinuous conduction mode (DCM). A schematic of a DC-DC boost converter and its key waveforms are shown in Fig. 2-1. With the assumptions of CCM working and a switching frequency much higher than the converter natural frequencies, state space averaging (SSA) method can be applied to determine the converter model regarding the small-ripple approximation [201]. The equations describing the behavior of converter in two different states has been thoroughly discussed in Appendix A.

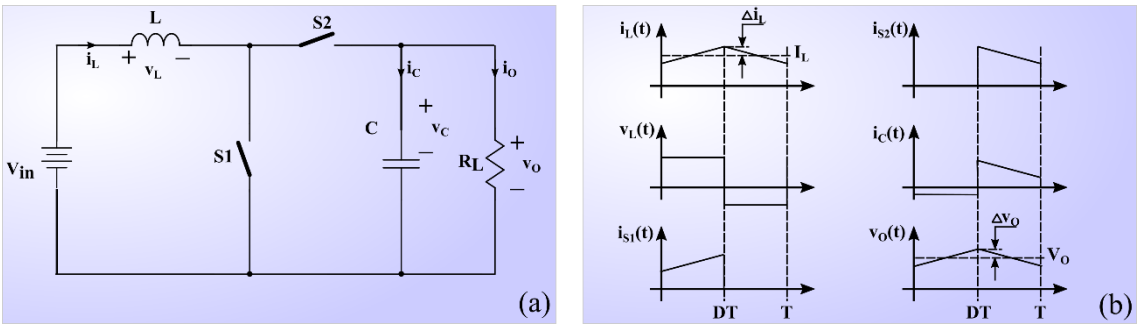


Fig. 2-1. DC-DC Boost converter, (a) circuit schematic, (b) key waveforms.

2-1-3 Circuit design consideration

In this section, a DC-DC boost converter is designed as battery regulation converter in HEV so that its input voltage range is about 200 V (battery side). The maximum output power is 3000W. Regarding output voltage value, 400V, corresponding load resistance is 53.33 Ohm. Regarding eq. (A-3), it can be easily observed that duty ratio is close to 0.5. The switching frequency is assumed to be 20 kHz and the inductor current ripple is restricted to $\Delta i_L = 1A$ while output capacitor voltage ripple is limited to Δv_C=0.5%=2V. Expressions required for calculating values of capacitor and inductor can easily obtained from equations (A-4) as 46.87μF and 2.5mH, respectively. Accordingly, all of the circuit parameters are known. Regarding above-mentioned circuit specifications, a 600V-15A power IGBT from Infineon Company, namely IKP15N60T, can be employed.

2-1-4 Detail analysis of Boost Converter

In this section, we focus on the detailed analysis of the DC-DC boost converter. The schematic of this converter with the all of considered parasitic components is shown in Fig. 2-2. Fig. 2-2a depicts the converter containing actual components while Fig. 2-2b demonstrates its equivalent circuit. As it is shown, both IGBT and diode have been modeled by a series circuit including an ideal switch, an internal resistor and

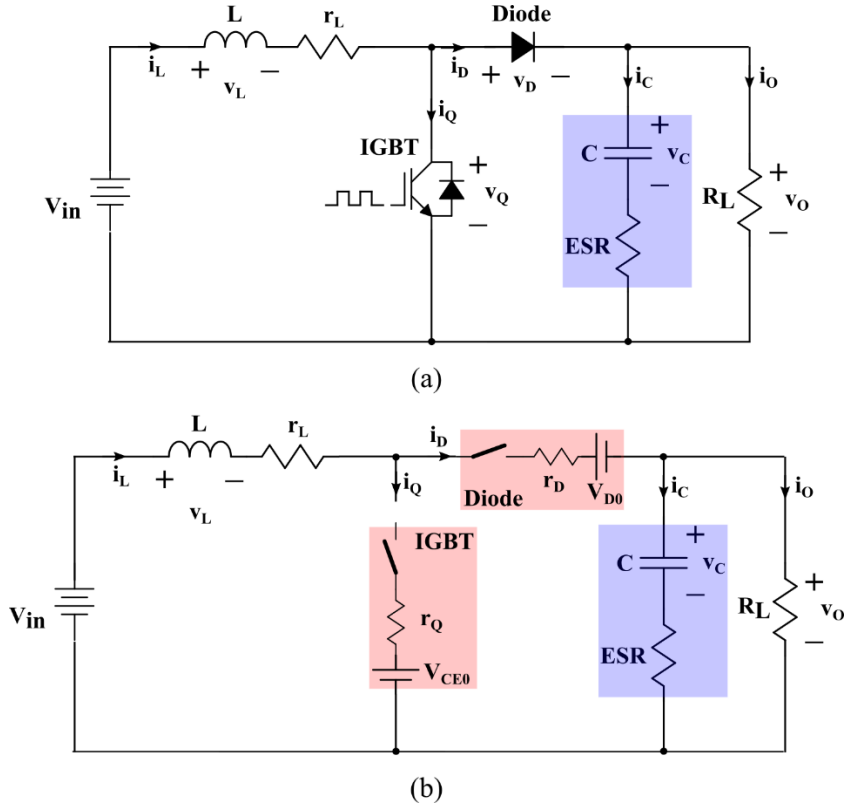


Fig. 2-2. DC-DC boost converter with parasitic components, (a) converter schematic, (b) equivalent circuit.

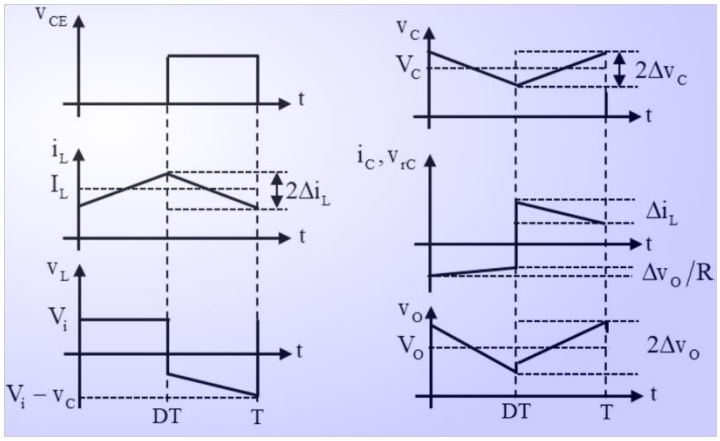


Fig. 2-3. DC-DC boost converter key waveforms considering parasitic components.

an internal forward voltage. With the assumption of $5L/r_L >> T$, the variation of the inductor current is linear. The key waveforms of this converter working in the CCM is shown in Fig. 2-3. Accordingly, two dependent states have been presented, one is related to the period time in which IGBT is on while diode is in blocking state (hereafter we shall call this period "on-state") and the other one is related to the remained period in which IGBT is off while diode is in conducting state (hereafter we shall call this period "off-state"). The equivalent circuit in both states has been demonstrated in Fig. 2-4. Fig. 2-4a shows the converter in on-state in which IGBT is on and Diode is off. Fig. 2-4b depicts the converter in off-state in which IGBT is off and diode is on. For analyzing and modeling DC-DC boost converter, one should obtain state space equations in both operating states. As there are only two independent energy storing components, there will be only two independent state space equations [196].

Time varying state space equations for describing a DC-DC converter in general form is written as follows:

$$\frac{d\mathbf{x}(t)}{dt} = [q(t)\mathbf{A}_1 + (1-q(t))\mathbf{A}_2]\mathbf{x}(t) + [q(t)\mathbf{B}_1 + (1-q(t))\mathbf{B}_2]\mathbf{u}(t) \qquad (2\text{-}1)$$

where $\mathbf{x}(t)$ is the state vector, $q(t)$ is the switching function and getting only 1 or 0 value (PWM), $\mathbf{u}(t)$ is the input vector and $\{\mathbf{A}_1, \mathbf{A}_2, \mathbf{B}_1, \mathbf{B}_2\}$ are the system matrices related to the on-state and off-state operation modes. All the letters written in **bold** are either vectors or matrices. One can easily observe that the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$ are time varying parameters resulting in time varying global state space system. There are also lots of approaches that can translate this time varying state space system to the much more simplified time invariant state space system at the expense of accuracy loss [202]–[204].

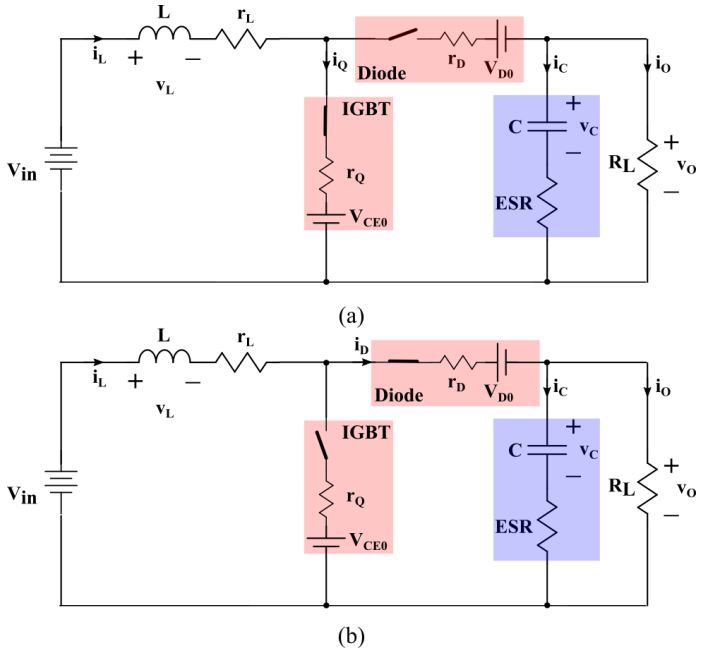


Fig. 2-4. DC-DC boost converter with parasitic components, (a) on-state, (b) off-state equivalent circuits.

One can consider $\mathbf{x}$ as the following vector:

$$\mathbf{x}(t)=\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix}$$

Input voltage, saturation collector-emitter voltage of IGBT and Diode forward voltage are all considered as an input vector. Accordingly

$$\mathbf{u}(t)=\begin{bmatrix} v_i(t) \\ v_{CE0}(t) \\ v_{D0}(t) \end{bmatrix}$$

Differential equations of the considered converter have been carried out in both states in Appendix A. According to equations (A-6), (A-7), (A-10) and (A-12) and regarding the general time varying state space modeling expressed in (2-1), the time varying state space equations for the DC-DC boost converter can obtain as follows:

$$\begin{aligned} L\frac{di_L(t)}{dt} &= q(t)\left\{-(r_Q-r_D-\frac{Rr_C}{R+r_C})i_L(t)+\frac{R}{R+r_C}v_C(t)+v_{D0}(t)-v_{CE0}(t)\right\} \\ &\quad -(r_L+r_D+\frac{Rr_C}{R+r_C})i_L(t)-\frac{R}{R+r_C}v_C(t)+v_i(t)-v_{D0}(t) \\ C\frac{dv_C(t)}{dt} &= q(t)\left\{-\frac{R}{R+r_C}i_L(t)\right\}+\frac{R}{R+r_C}i_L(t)-\frac{1}{R+r_C}v_C(t) \end{aligned} \qquad (2\text{-}2)$$

Rearranging above-mentioned equation in matrix form as described in (2-1), one can attain that

$$\mathbf{A}_1=\begin{bmatrix} -\frac{1}{L}(r_L+r_Q) & 0 \\ 0 & -\frac{1}{C}\frac{1}{R+r_C} \end{bmatrix}_{2\times 2} \qquad \mathbf{A}_2=\begin{bmatrix} -\frac{1}{L}(r_L+r_D+\frac{Rr_C}{R+r_C}) & -\frac{1}{L}\frac{R}{R+r_C} \\ \frac{1}{C}\frac{R}{R+r_C} & -\frac{1}{C}\frac{1}{R+r_C} \end{bmatrix}_{2\times 2}$$

$$\mathbf{B}_1=\begin{bmatrix} \frac{1}{L} & -\frac{1}{L} & 0 \\ 0 & 0 & 0 \end{bmatrix}_{2\times 3} \qquad \mathbf{B}_2=\begin{bmatrix} \frac{1}{L} & 0 & -\frac{1}{L} \\ 0 & 0 & 0 \end{bmatrix}_{2\times 3}$$

Accordingly, the time varying state space model extraction now has been completed. As it was mentioned there are lots of approaches to solve this set of linear equations. These methods totally fall into two categories, namely time varying approaches and time invariant approaches. However, some methods attempt to firstly make the LTV system to a LTI system and then solve the new extracted LTI system with some time invariant approaches [200]. Regarding equation (2-1), it is observed that our system is LTV due to its coefficients matrices describing the system behavior.

2-1-5 Applicable approaches to DC-DC converters

In this section some approaches recently reported in the literature are investigated [205]–[207]. All of the discussed methods are based on averaging technique. Generalized state space averaging (GSSA) is based on the most common approach i.e. state space averaging (SSA) method [201]. In this method, it is assumed that the rate of duty cycle command d(t) change in respect to PWM signal frequency is slow enough and subsequently the switching function q(t) during a switching time period is almost constant. Regarding this assumption one can define the switching function q(t) as following (see Fig. 2-5):

$$q(t)=\begin{cases} 1 & 0\le t<dT_S \\ 0 & dT_S\le t<T_S \end{cases} \qquad (2\text{-}3)$$

where T_S is the switching period. Accordingly, by averaging the state space equation in two separated states discussed previously, namely on-state ($q(t)=1$) and off-state ($q(t)=0$), one can obtain SSA model employing (2-1) and (2-3) as follows

$$\frac{d\bar{\mathbf{x}}(t)}{dt}=d\left(\mathbf{A}_1\bar{\mathbf{x}}(t)+\mathbf{B}_1\mathbf{u}(t)\right)+\left(1-d\right)\left(\mathbf{A}_2\bar{\mathbf{x}}(t)+\mathbf{B}_2\mathbf{u}(t)\right) \qquad (2\text{-}4)$$

where $\bar{\mathbf{x}}(t)$ is the average state vector and indicates the averaged dynamic behavior of the interested system. By the assumption that duty cycle command d(t) change in one switching period is not significant, equation (2-1) has been transferred (LTV model) to equation (2-4) which is time invariant state space equation (LTI model). Of course, irrefutable proof has shown that this approach is only valid and sufficiently

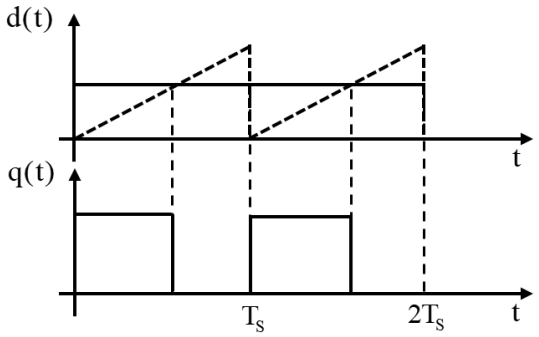


Fig. 2-5. Duty cycle command and resulted switching function.

accurate when the switching frequency (f_S) is much higher than DC-DC converter natural frequencies [208].

SSA has some disadvantages including lack of estimating states' ripple (e.g. inductor current or capacitor voltage), lack of calculating ripple cross coupling effects [207] and it cannot consider the duty cycle command changes during one switching period. However, it is easily constructed and can be applied to complicated circuit and in addition one can consider closed loop behavior in the global system. One of the main reasons that make us not to apply this method in our reliability assessment is the lack of estimating states' ripple (e.g. inductor current or capacitor voltage) in the SSA. It is clear that for the reliability assessment, either voltage or current ripples play a major role in semiconductor power losses calculation. Since SSA is not capable of ripple estimating, it cannot be a sufficiently accurate approach for reliability assessment.

Another approach for analyzing state space equations of DC-DC converters is TIMF modeling [200]. This approach is based on the Fourier series and let the coefficients of Fourier series be the state variables of the interested system. It is clear that if higher order Fourier series (N) was under study, a much more accurate modeling can be achieved. This approach has lots of advantages including ripple estimation (with arbitrary accuracy thanks to the higher order Fourier series), capable of considering feedback and easy construction. Thus, it can be a suitable choice for electrical analyzing in reliability assessment. A comprehensive comparison among recent approaches (GSSA [209], Krylov-Bogoliubov-Mitropolsky Method [210] and Floquet theory [204]) are listed in Table. 2-1.

Table. 2-1. Comparison of different approaches

	SSA	GSSA	KBM	Floquet	TIMF
Ripple estimation	No	Yes	Yes	Yes	Yes
Model construction	Easy	Difficult	Difficult	Difficult	Easy
Closed loop modeling capability	Yes	Yes	Yes	No	Yes
Complexity of development of higher-order models	-	Difficult	Difficult	Difficult	Easy

2-1-6 Time invariant multi frequency modeling of DC-DC boost converter

In this section, TIMF modeling of a DC-DC boost converter with the assumptions that were mentioned at the beginning of this chapter will be explained. This modeling will be expressed based on the state space equations of DC-DC boost converter and then developed by the rules listed in Table. A-1. Detailed TIMF description has been presented in Appendix A. The state space equations was obtained in (2-2).
Using the rules listed in Table. A-1,

$$\begin{cases} x \to \mathbf{x} & i_L \to \mathbf{i}_L, v_C \to \mathbf{v}_C \\ \dfrac{dx}{dt} \to -\boldsymbol{\Omega}\mathbf{x} + \dfrac{d\mathbf{x}}{dt} & L\dfrac{di_L}{dt} \to L\left(-\boldsymbol{\Omega}\mathbf{i}_L + \dfrac{d\mathbf{i}_L}{dt}\right),\ C\dfrac{dv_C}{dt} \to C\left(-\boldsymbol{\Omega}\mathbf{v}_C + \dfrac{d\mathbf{v}_C}{dt}\right) \\ q \to \mathbf{Q} & (1-q) \to (\mathbf{I}_{2N+1} - \mathbf{Q}) \\ z \to \mathbf{z} & v_i \to \mathbf{v}_i = \begin{bmatrix} v_i \\ 0 \\ \vdots \\ 0 \end{bmatrix}, v_{CE0} \to \mathbf{v}_{CE0} = \begin{bmatrix} v_{CE0} \\ 0 \\ \vdots \\ 0 \end{bmatrix}, v_{D0} \to \mathbf{v}_{D0} = \begin{bmatrix} v_{d0} \\ 0 \\ \vdots \\ 0 \end{bmatrix} \end{cases} \tag{2-5}$$

With a tradeoff between accuracy and manipulation time consuming, third order Fourier series will be employed (N=3). Accordingly, size of matrices $\boldsymbol{\Omega}$ and $\mathbf{Q}$ is (2N+1)×(2N+1)=7×7. As there are only two energy storing components, size of matrices $\mathbf{x}$ and $\mathbf{A}$ are respectively (2×(2N+1))×1=14×1 and (2×(2N+1))× (2×(2N+1))=14×14. Since three input vectors ($\mathbf{u}_{21\times1}$) have been considered, the size of matrix $\mathbf{B}$ is 2×(2N+1)×21=14×21. By using equation (2-2), we have:

$$\begin{aligned} L\left(-\boldsymbol{\Omega}\mathbf{i}_L + \frac{d\mathbf{i}_L}{dt}\right) &= \mathbf{Q}\left\{-(r_Q - r_D - \frac{Rr_C}{R+r_C})\mathbf{i}_L + \frac{R}{R+r_C}\mathbf{v}_C + \mathbf{v}_{D0} - \mathbf{v}_{CE0}\right\} \\ &\quad -(r_L + r_D + \frac{Rr_C}{R+r_C})\mathbf{i}_L - \frac{R}{R+r_C}\mathbf{v}_C + \mathbf{v}_i - \mathbf{v}_{D0} \\ C\left(-\boldsymbol{\Omega}\mathbf{v}_C + \frac{d\mathbf{v}_C}{dt}\right) &= (\mathbf{I}_7 - \mathbf{Q})\frac{R}{R+r_C}\mathbf{i}_L - \frac{1}{R+r_C}\mathbf{v}_C \end{aligned} \tag{2-6}$$

where $\mathbf{i}_L$ and $\mathbf{v}_C$ can be considered as (A-13). Since N=3,

$$\begin{aligned} \mathbf{i}_L &= \begin{bmatrix} i_{L0} & i_{L\alpha1} & i_{L\beta1} & i_{L\alpha2} & i_{L\beta2} & i_{L\alpha3} & i_{L\beta3} \end{bmatrix}^T \\ \mathbf{v}_C &= \begin{bmatrix} v_{C0} & v_{C\alpha1} & v_{C\beta1} & v_{C\alpha2} & v_{C\beta2} & v_{C\alpha3} & v_{C\beta3} \end{bmatrix}^T \\ \mathbf{x} &= \begin{bmatrix} \mathbf{i}_L & \mathbf{v}_C \end{bmatrix}^T \end{aligned} \tag{2-7}$$

where FSR coefficients can be estimated by (A-14).

Rearranging equation (2-6), state space equations are calculated as follows:

$$\frac{d\mathbf{i}_L}{dt}=\left\{\left(\frac{-\mathbf{Q}}{L}\right)\left(r_Q-r_D-\frac{Rr_C}{R+r_C}\right)-\frac{\mathbf{I}_7}{L}(r_L+r_D+\frac{Rr_C}{R+r_C})+\mathbf{\Omega}\right\}\mathbf{i}_L$$
$$+\left\{\frac{\mathbf{Q}}{L}\frac{R}{R+r_C}-\frac{\mathbf{I}_7}{L}\frac{R}{R+r_C}\right\}\mathbf{v}_C+\frac{\mathbf{I}_7}{L}\mathbf{v}_i-\frac{\mathbf{Q}}{L}\mathbf{v}_{CE0}+\left\{\frac{\mathbf{Q}}{L}-\frac{\mathbf{I}_7}{L}\right\}\mathbf{v}_{D0} \quad (2\text{-}8)$$

$$\frac{d\mathbf{v}_C}{dt}=\left\{\frac{(\mathbf{I}_7-\mathbf{Q})}{C}\frac{R}{R+r_C}\right\}\mathbf{i}_L+\left\{-\frac{\mathbf{I}_7}{C}\frac{1}{R+r_C}+\mathbf{\Omega}\right\}\mathbf{v}_C$$

Where $\mathbf{I}_7$ is 7×7 unit matrix. Regarding equation (A-19), one can find that:

$$\mathbf{\Omega}=\begin{bmatrix}0&0&0&0&0&0&0\\0&0&-\omega_s&0&0&0&0\\0&\omega_s&0&0&0&0&0\\0&0&0&0&-2\omega_s&0&0\\0&0&0&2\omega_s&0&0&0\\0&0&0&0&0&0&-3\omega_s\\0&0&0&0&0&3\omega_s&0\end{bmatrix}_{7\times7} \quad (2\text{-}9)$$

Now, Fourier series representation of the switching function for N=3 is written as:

$$q(t)=q_0+q_{\alpha1}\cos\omega_s t+q_{\beta1}\sin\omega_s t+q_{\alpha2}\cos2\omega_s t+q_{\beta2}\sin2\omega_s t+q_{\alpha3}\cos3\omega_s t$$
$$+q_{\beta3}\sin3\omega_s t \quad (2\text{-}10)$$

where

$$q_0=\frac{1}{2\pi}\int_{\omega_s t_\ell}^{\omega_s t_h}d(\omega_s t)=\frac{t_h-t_\ell}{T_s}$$
$$q_{\alpha n}=\frac{1}{\pi}\int_{\omega_s t_\ell}^{\omega_s t_h}\cos(n\omega_s t)d(\omega_s t)=\frac{2}{n\pi}\left[\cos\left(n\pi\frac{t_h+t_\ell}{T_S}\right)\sin\left(n\pi\frac{t_h-t_\ell}{T_S}\right)\right] \quad (2\text{-}11)$$
$$q_{\beta n}=\frac{1}{\pi}\int_{\omega_s t_\ell}^{\omega_s t_h}\sin(n\omega_s t)d(\omega_s t)=\frac{2}{n\pi}\left[\sin\left(n\pi\frac{t_h+t_\ell}{T_S}\right)\sin\left(n\pi\frac{t_h-t_\ell}{T_S}\right)\right]$$

Regarding Fig. 2-5, one can find that t_ℓ=0 and t_h can be calculated by intersecting carrier signal (sawtooth signal) with duty cycle command. Duty cycle command is considered as follows:

$$d(t)=d_0+d_{\alpha1}\cos\omega_s t+d_{\beta1}\sin\omega_s t+d_{\alpha2}\cos2\omega_s t+d_{\beta2}\sin2\omega_s t+d_{\alpha3}\cos3\omega_s t$$
$$+d_{\beta3}\sin3\omega_s t \quad (2\text{-}12)$$

Thus, applying Newton-Raphson iterative algorithm with initial value of $t_{h0}=d_0T_S$, it yields:

$$f(t)=\frac{t}{T_S}-\left(\begin{matrix}d_0+d_{\alpha1}\cos\omega_s t+d_{\beta1}\sin\omega_s t+d_{\alpha2}\cos2\omega_s t\\+d_{\beta2}\sin2\omega_s t+d_{\alpha3}\cos3\omega_s t+d_{\beta3}\sin3\omega_s t\end{matrix}\right)=0 \tag{2-13}$$

$$f(t_h)=\frac{t_h}{T_S}-\left(\begin{matrix}d_0+d_{\alpha1}\cos\omega_s t_h+d_{\beta1}\sin\omega_s t_h+d_{\alpha2}\cos2\omega_s t_h\\+d_{\beta2}\sin2\omega_s t_h+d_{\alpha3}\cos3\omega_s t_h+d_{\beta3}\sin3\omega_s t_h\end{matrix}\right)=0$$

$$f'(t_h)=\frac{1}{T_S}-\frac{2\pi}{T_S}\left(\begin{matrix}-d_{\alpha1}\sin\omega_s t_h+d_{\beta1}\cos\omega_s t_h-2d_{\alpha2}\sin2\omega_s t_h\\+2d_{\beta2}\cos2\omega_s t_h-3d_{\alpha3}\sin3\omega_s t_h+3d_{\beta3}\cos3\omega_s t_h\end{matrix}\right) \tag{2-14}$$

$$t_{hn+1}=t_{hn}-\frac{f(t_{hn})}{f'(t_{hn})}$$

Only one iteration is sufficiently acceptable. Thus

$$t_h=t_{h0}-\frac{f(t_{h0})}{f'(t_{h0})}=d_0T_S-\frac{d_0-\left(\begin{matrix}d_0+d_{\alpha1}\cos2\pi d_0+d_{\beta1}\sin2\pi d_0+d_{\alpha2}\cos4\pi d_0\\+d_{\beta2}\sin4\pi d_0+d_{\alpha3}\cos6\pi d_0+d_{\beta3}\sin6\pi d_0\end{matrix}\right)}{\frac{1}{T_S}-\frac{2\pi}{T_S}\left(\begin{matrix}-d_{\alpha1}\sin2\pi d_0+d_{\beta1}\cos2\pi d_0-2d_{\alpha2}\sin4\pi d_0\\+2d_{\beta2}\cos4\pi d_0-3d_{\alpha3}\sin6\pi d_0+3d_{\beta3}\cos6\pi d_0\end{matrix}\right)} \tag{2-15}$$

Accordingly,

$$t_h=T_S\left(d_0+\frac{\left(\begin{matrix}d_{\alpha1}\cos2\pi d_0+d_{\beta1}\sin2\pi d_0+d_{\alpha2}\cos4\pi d_0\\+d_{\beta2}\sin4\pi d_0+d_{\alpha3}\cos6\pi d_0+d_{\beta3}\sin6\pi d_0\end{matrix}\right)}{1+2\pi\left(\begin{matrix}d_{\alpha1}\sin2\pi d_0-d_{\beta1}\cos2\pi d_0+2d_{\alpha2}\sin4\pi d_0\\-2d_{\beta2}\cos4\pi d_0+3d_{\alpha3}\sin6\pi d_0-3d_{\beta3}\cos6\pi d_0\end{matrix}\right)}\right) \tag{2-16}$$

If we assume open loop operation, i.e. duty cycle command is approximately constant (regarding the operating point calculated in equation (A-3), $d(t)=d_0=0.5$), it can be easily seen that:

$$t_h=d_0T_S \tag{2-17}$$

Therefore,

$$\begin{aligned}&q_0=\frac{t_h-t_\ell}{T_S}=\frac{d_0T_S-0}{T_S}=d_0=0.5\\&q_{\alpha1}=\frac{2}{\pi}\left[\cos(\pi d_0)\sin(\pi d_0)\right]=0 \qquad q_{\beta1}=\frac{2}{\pi}\left[\sin(\pi d_0)\sin(\pi d_0)\right]=\frac{2}{\pi}\\&q_{\alpha2}=\frac{1}{\pi}\left[\cos(2\pi d_0)\sin(2\pi d_0)\right]=0 \quad q_{\beta2}=\frac{1}{\pi}\left[\sin(2\pi d_0)\sin(2\pi d_0)\right]=0\\&q_{\alpha3}=\frac{2}{3\pi}\left[\cos(3\pi d_0)\sin(3\pi d_0)\right]=0 \quad q_{\beta3}=\frac{2}{3\pi}\left[\sin(3\pi d_0)\sin(3\pi d_0)\right]=\frac{2}{3\pi}\end{aligned} \tag{2-18}$$

It should be mentioned that here $d_0=0.5$ is only an example for validating the approach. In the later sections for mitigating power losses in the DC-DC boost

converter duty cycle command is constant but it will be considered $d_0 = 0.52$. This value results in nominal voltage ratio, namely M_V=2, and converter efficiency of 96%.

For N=3, one can easily find the **Q** matrix as follows,

$$\begin{bmatrix} q_0 & 0 & \frac{q_{\beta 1}}{2} & 0 & 0 & 0 & \frac{q_{\beta 3}}{2} \\ 0 & q_0 & 0 & 0 & \frac{q_{\beta 1}}{2}+\frac{q_{\beta 3}}{2} & 0 & 0 \\ q_{\beta 1} & 0 & q_0 & \frac{q_{\beta 3}}{2}-\frac{q_{\beta 1}}{2} & 0 & 0 & 0 \\ 0 & 0 & \frac{q_{\beta 3}}{2}-\frac{q_{\beta 1}}{2} & q_0 & 0 & -\frac{q_{\beta 3}}{2} & \frac{q_{\beta 3}}{2} \\ 0 & \frac{q_{\beta 3}}{2}+\frac{q_{\beta 1}}{2} & 0 & 0 & q_0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{q_{\beta 1}}{2} & q_0 & 0 \\ q_{\beta 3} & 0 & 0 & \frac{q_{\beta 1}}{2} & 0 & 0 & q_0 \end{bmatrix} \quad (2\text{-}19)$$

Accordingly,

$$\begin{bmatrix} 0.5 & 0 & 1/\pi & 0 & 0 & 0 & 1/3\pi \\ 0 & 0.5 & 0 & 0 & 4/3\pi & 0 & 0 \\ 2/\pi & 0 & 0.5 & -2/3\pi & 0 & 0 & 0 \\ 0 & 0 & -2/3\pi & 0.5 & 0 & -1/3\pi & 1/3\pi \\ 0 & 4/3\pi & 0 & 0 & 0.5 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1/\pi & 0.5 & 0 \\ 2/3\pi & 0 & 0 & 1/\pi & 0 & 0 & 0.5 \end{bmatrix} \quad (2\text{-}20)$$

Here for validating the TIMF approach, TIMF modeling is comparing with detailed switching modeling performed in MATLAB environment. In this comparison, two state variables waveforms, inductor current and capacitor voltage, will be compared with each other. The specifications of the considered DC-DC boost converter are listed in Table 2-2.

Fig. 2-6 and 2-7 depict the capacitor voltage and inductor current in three different modeling i.e. TIMF, SSA and detailed switching model. Regarding these figures, one can find that TIMF has sufficiently acceptable accuracy, both in transient and steady state operation modes, being able to be employed in the reliability assessment. It is clear that the voltage ripple and current ripple playing a significant role in power loss calculation have been completely estimated. Therefore, TIMF modeling will be used in reliability evaluation.

Table 2-2. Working Conditions and Parameters Values

Parameter	Value	Parameter	VALUE
V_i	200V	V_{out}	400V
P_o	3000W	R	53.34 Ohm
L	2.50mH	r_L	0.3 Ohm
C	47 µF	r_C	0.05 Ohm
r_D	0.04 Ohm @T_j=175°C	V_{D0}	1V @T_j=175°C
r_Q	0.0726 Ohm @T_j=175°C	V_{CE0}	0.81V @T_j=175°C

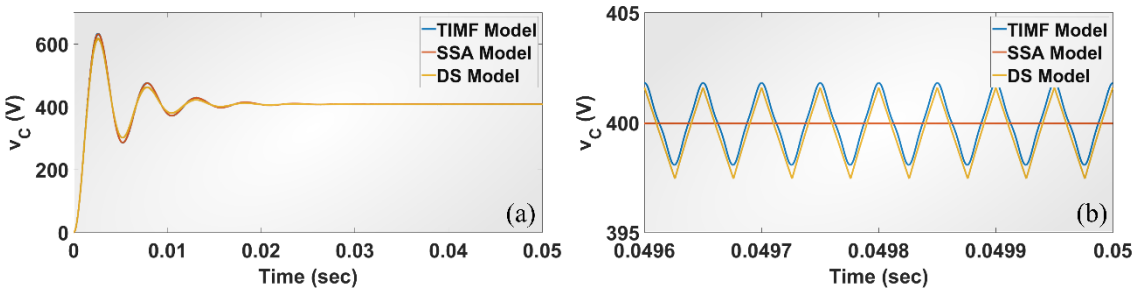


Fig. 2-6. (a) Transient of capacitor voltage, (b) Steady state of capacitor voltage

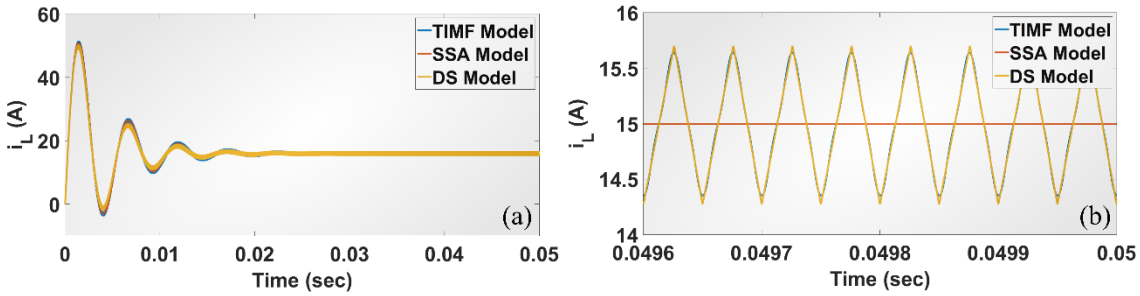


Fig. 2-7. (a) Transient of Inductor current, (b) Steady state of Inductor current

2-2 Power loss modeling

2-2-1 Introduction

Power loss calculation has paramount of importance in estimating useful life time of power semiconductor devices exposed to electro-thermo-mechanical creep-fatigue failure [211], [212]. For processing electrical power in all power levels, all the power electronic devices have their own losses. These power losses are thermally dissipated to the environment. The main procedure of specified device power loss calculation has been generally provided by its manufacturer. Thus, in this section, our focus will be on the relationships expressed by the manufacturer, i.e. Infineon Company [213], [214] .

2-2-2 Power loss calculation (semiconductors)

In this section, we will concentrate on the power loss calculation of power IGBT and diode only based on the component's datasheet and its application note. To evaluate

the efficiency of the DC-DC boost converter and thermal related issues, all the components' power losses will be separately calculated. At first, calculation of IGBT and diode power losses will be considered. IGBT and diode power losses can be divided in four different groups as conduction losses (P_{cond}), switching losses (P_{sw}), blocking losses (P_b), gate driving loss (P_G). Generally, blocking and gate driving losses are neglected.

2-2-2-1 Conduction loss

IGBT conduction losses can be estimated using an IGBT approximation with a series connection of DC voltage source (v_{CE0}) representing IGBT on-state zero-current collector-emitter voltage and a collector emitter on-state resistance (r_Q):

$$v_{CE}(i_Q) = v_{CE0} + r_Q i_Q \tag{2-21}$$

The same approximation can be used for the diode, giving:

$$v_D(i_D) = v_{D0} + r_D i_D \tag{2-22}$$

These important parameters can be extracted directly from the datasheet at the specified temperature [213]. Fig. 2-8 demonstrates collector emitter and diode forward voltages. One can find that both equivalent voltages and series resistors in IGBT and diode are changing with junction temperature. Therefore, in our calculation we should consider this changing. That is why following coefficients are being expressed (with regard to Fig. 2-8).

$$\begin{aligned} v_{CE0}(T_j) &= v_{CE0}(25^\circ C) + TC_{VQ}(T_j - 25^\circ C) \\ r_Q(T_j) &= r_Q(25^\circ C) + TC_{rQ}(T_j - 25^\circ C) \end{aligned} \tag{2-23}$$

where

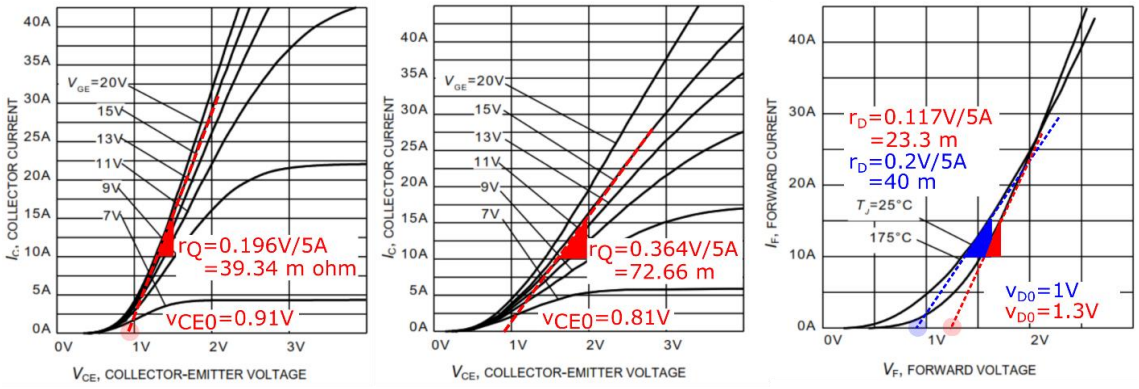
$$\begin{aligned} TC_{VQ} &= \frac{v_{CE0}(175^\circ C) - v_{CE0}(25^\circ C)}{175^\circ C - 25^\circ C} = -6.667\times10^{-4}\,\frac{V}{^\circ C} \\ TC_{rQ} &= \frac{r_Q(175^\circ C) - r_Q(25^\circ C)}{175^\circ C - 25^\circ C} = 0.222\,\frac{m\Omega}{^\circ C} \end{aligned} \tag{2-24}$$

and

$$\begin{aligned} v_{D0}(T_j) &= v_{D0}(25^\circ C) + TC_{VD}(T_j - 25^\circ C) \\ r_D(T_j) &= r_D(25^\circ C) + TC_{rD}(T_j - 25^\circ C) \end{aligned} \tag{2-25}$$

where

$$\begin{aligned} TC_{VD} &= \frac{v_{D0}(175^\circ C) - v_{D0}(25^\circ C)}{175^\circ C - 25^\circ C} = -2\times10^{-3}\,\frac{V}{^\circ C} \\ TC_{rD} &= \frac{r_D(175^\circ C) - r_D(25^\circ C)}{175^\circ C - 25^\circ C} = 0.111\,\frac{m\Omega}{^\circ C} \end{aligned} \tag{2-26}$$



(a) (b) (c)

Fig.2-8. I-V characteristics of IGBT and power diode (a) Collector-emitter voltage at 20℃, (b) Collector-emitter voltage at 175℃, (c) Diode forward voltage [213].

The instantaneous value of the IGBT conduction losses is:

$$\begin{aligned} p_{CQ}(t,T_j) = v_{CE}(t,T_j)\times i_Q(t) &= \left\{v_{CE0}(25^\circ C) + TC_{VQ}(T_j - 25^\circ C)\right\}\times i_Q(t) \\ &+ \left\{r_Q(25^\circ C) + TC_{rQ}(T_j - 25^\circ C)\right\}\times i_Q^2(t) \end{aligned} \quad (2\text{-}27)$$

If the average IGBT current value is I_{Qav}, and the rms value of IGBT current is I_{Qrms}, then the average losses can be expressed as (T_S is the switching period):

$$\begin{aligned} P_{CQ}(T_j) &= \frac{1}{T_S}\int_0^{T_S} p_{CQ}(t,T_j)\,dt = \frac{1}{T_S}\int_0^{T_S} v_{CE}(t,T_j)\times i_Q(t)\,dt \\ &= \left\{v_{CE0}(25^\circ C) + TC_{VQ}(T_j - 25^\circ C)\right\} I_{Qav} \\ &+ \left\{r_Q(25^\circ C) + TC_{rQ}(T_j - 25^\circ C)\right\} I_{Qrms}^2 \end{aligned} \quad (2\text{-}28)$$

The same calculation procedure can be also performed for power diode.

2-2-2-2 Switching Loss

The circuit for the examination of the IGBT switching losses is presented in Fig. 2-9. It is a single-quadrant chopper supplying an inductive type load. The IGBT is driven from the driver circuit, providing a voltage U_{Dr} at its output. The IGBT internal diode is used as a free-wheeling diode. If an external freewheeling diode is used, the calculations are still valid, considering the diode parameters that are taken from the diode's datasheet.

The turn-on and turn-off energy losses in IGBT and diode depend on numerous external parameters including gate driving resistor (R_g), gate-emitter voltage (V_g), stray inductance (L_σ), parasitic capacitance (C_σ), collector-emitter voltage (V_{CE}), collector current (I_Q) and junction temperature (T_j). In this study, we assume that R_g , V_g , C_σ and L_σ are constant and equal to 15Ω, 15V, 39 pF and 154 nH, respectively. The others including collector-emitter voltage (V_{CE}), collector current (I_Q) and junction temperature (T_j) will be considered in the power loss calculation. It is

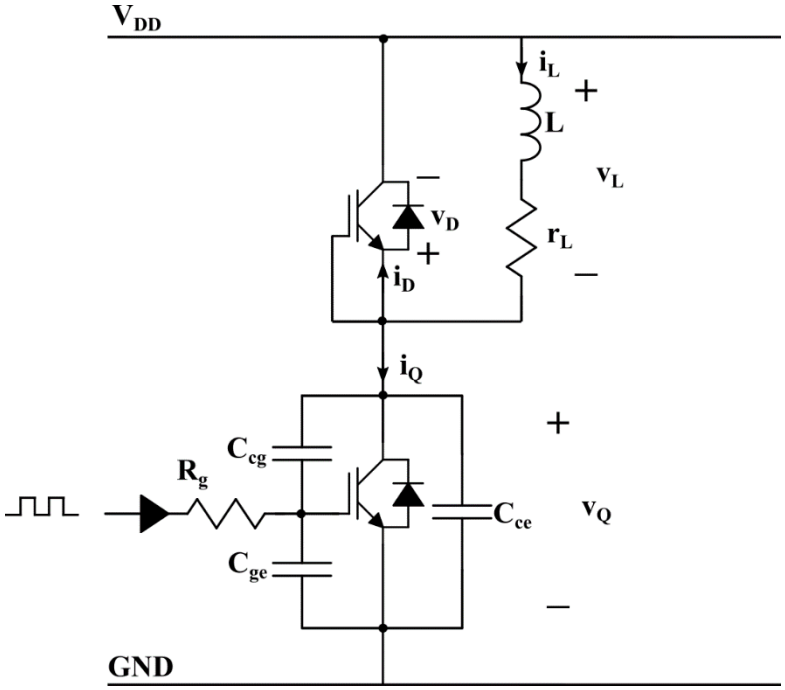


Fig. 2-9. IGBT chopper driving an inductive load [214]

noted that in the total switching energy losses, the reverse recovery energy of the free-wheeling diode is also considered.

The switching losses in the IGBT and the diode are the product of the switching energies with the switching frequency (f_S):

$$\begin{aligned} P_{SQ} &= (E_{onQ} + E_{offQ}).f_S = E_{tsQ}.f_S \\ P_{SD} &= (E_{onD} + E_{offD}).f_S \approx E_{onD}.f_S = E_{rrD}.f_S \end{aligned} \quad (2\text{-}29)$$

where E_{onQ}, E_{offQ}, E_{onD} and E_{offD} are IGBT and diode switching energy losses at the time they are turning on or turning off. E_{rrD} is the reverse recovery energy of diode. These energy losses are estimated from manufacturer datasheet at typical voltage, current and junction temperature [214]. Since, operating points are different from these typical values and regarding to the circuit configuration, equation (2-29) can be modified as follows:

$$\begin{aligned} P_{SQ}(T_j) &= E_{ts}.f_S \left(\frac{I_{in}}{I_{typ}}\right)^{K_{IQ}} \left(\frac{V_o}{V_{typ}}\right)^{K_{VQ}} \left\{1 + TC_{Ets}\left(T_j - T_{ref}\right)\right\} \\ P_{SD}(T_j) &= E_{rr}.f_S \left(\frac{I_{in}}{I_{typ}}\right)^{K_{ID}} \left(\frac{V_o}{V_{typ}}\right)^{K_D} \left\{1 + TC_{Err}\left(T_j - T_{ref}\right)\right\} \\ &= \left(\frac{1}{4} Q_{rr} V_o\right).f_S \left(\frac{I_{in}}{I_{typ}}\right)^{K_{ID}} \left(\frac{V_o}{V_{typ}}\right)^{K_D} \left\{1 + TC_{Err}\left(T_j - T_{ref}\right)\right\} \end{aligned} \quad (2\text{-}30)$$

where typical values (X_{typ}) are the values in which the manufacturer has tested the devices and measured the interested values including switching loss energy which are 15A and 400V for I_{typ} and V_{typ}, respectively.

Power K_{IQ} , K_{VQ} , K_{ID} and K_{VD} are power coefficients expressing the voltage and the current dependencies of switching energy losses in IGBT and Diode, respectively. These power coefficients are extracted from the curves demonstrated in datasheet [213]. Referring to datasheet, it is found that:

$$K_{IQ} \approx 1 \qquad K_{VQ} \approx 1.35$$
$$K_{ID} \approx 0.6 \qquad K_{VD} \approx 0.6$$

Last but not least is the switching energy loss temperature coefficients in IGBT and diode expressing as following (considering T_{ref}=175°C).

$$TC_{Ets} = \frac{E_{ts}(175^{\circ}C) - E_{ts}(25^{\circ}C)}{(175^{\circ}C - 25^{\circ}C)E_{ts}(T_{ref})} = \frac{0.81mJ - 0.57mJ}{150^{\circ}C \times 0.81mJ} = 0.00197\frac{1}{^{\circ}C}$$
$$TC_{Err} = \frac{Q_{rr}(175^{\circ}C) - Q_{rr}(25^{\circ}C)}{(175^{\circ}C - 25^{\circ}C)Q_{rr}(T_{ref})} = \frac{1\mu C - 0.24\mu C}{150^{\circ}C \times 1\mu C} = 0.00506\frac{1}{^{\circ}C} \qquad (2\text{-}31)$$

Power losses in the IGBT and the free-wheeling diode can be expressed as the sum of the conduction and switching losses giving:

$$P_{Loss}^{IGBT} = P_{CQ}(T_j) + P_{SQ}(T_j)$$
$$P_{Loss}^{Diode} = P_{CD}(T_j) + P_{SD}(T_j) \qquad (2\text{-}32)$$

2-2-3 Analysis of boost converter

In this section, we focus on the detailed analysis of the DC-DC boost converter. The schematic of this converter with the all of parasitic components is shown in Fig. 2-2. With the assumption of $5L/R_L >> T_S$, the variation of the inductor current will be linear. The key waveforms of this converter are shown in Fig. 2-3.

In the previous section, the state space equations of the DC-DC boost converter has been obtained. Modeling and analyzing this converter has been performed via TIMF approach which is based on the Fourier series. One can readily calculate rms and average values of input current (inductor current) as follows:

$$I_{Lav} = i_{L0} = 15.955\,A$$
$$I_{Lrms} = \sqrt{i_{L0}^2 + \frac{i_{L\alpha 1}^2}{2} + \frac{i_{L\beta 1}^2}{2} + \frac{i_{L\alpha 2}^2}{2} + \frac{i_{L\beta 2}^2}{2} + \frac{i_{L\alpha 3}^2}{2} + \frac{i_{L\beta 3}^2}{2}} = 15.96A \qquad (2\text{-}33)$$

Therefore,

$$
\begin{aligned}
&I_{Qav} = i_{L0}\, D = 15.955 \times 0.52 = 8.2966A \\
&I_{Qrms} = I_{Lrms}\sqrt{D} = 15.96 \times \sqrt{0.52} = 11.5097A \\
&I_{Dav} = i_{L0}\,(1-D) = 15.955 \times (1-0.52) = 7.6584A \\
&I_{Drms} = I_{Lrms}\sqrt{(1-D)} = 15.96 \times \sqrt{(1-0.52)} = 11.0546A
\end{aligned}
\qquad (2\text{-}34)
$$

For overcoming the power losses effect on the voltage ratio, we consider D=0.52. Since IGBT and diode power losses are both temperature dependent, the power losses should be calculated by iterative algorithm [215]. This algorithm is demonstrated in Fig. 2-10. In this algorithm, for ten iterations, power losses of IGBT and diode have been calculated.

For completing the power losses calculation, one needs to employ thermal resistance for temperature calculation. One simple thermal equivalent circuit model is depicted in Fig. 2-11. Based on this figure, one can easily calculate the junction temperature and subsequently power losses. It should be mentioned that thermal resistances are as follows (see the next section):

$$
\begin{aligned}
&R_{th(h-a)} = 1.16\,^{\circ}C/W \qquad R^{IGBT}_{th(j-c)} = 1.15\,^{\circ}C/W \\
&R^{IGBT}_{th(c-h)} = 0.5\,^{\circ}C/W \qquad R^{Diode}_{th(j-c)} = 1.9\,^{\circ}C/W
\end{aligned}
$$

After 10 iterations using MATLAB environment, finally power losses along with junction temperatures of IGBT and Diode have been calculated and written as

$$
\begin{aligned}
&P^{IGBT}_{Loss} = P_{CQ} + P_{SQ} = 15.5742 + 15.1723 = 30.7466W \qquad T^{IGBT}_{j} = 142.8^{\circ}C \\
&P^{Diode}_{Loss} = P_{CD} + P_{SD} = 12.6339 + 1.5041 = 14.1380W \qquad T^{Diode}_{j} = 126^{\circ}C
\end{aligned}
$$

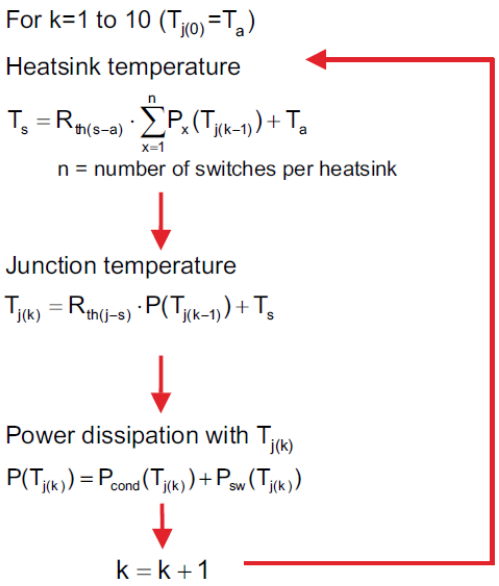


Fig. 2-10. Iterative algorithm for power loss calculation [215].

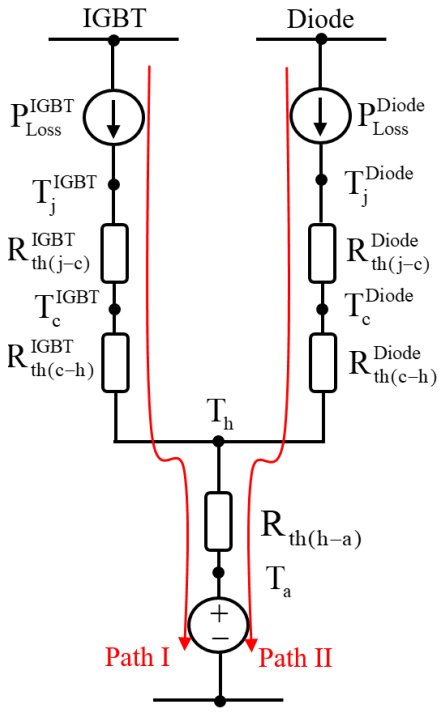


Fig. 2-11. Thermal equivalent circuit model

Power losses of this converter have been calculated as following:

$$P_{Loss} = P_{Loss}^{IGBT} + P_{Loss}^{Diode} + P_{Loss}^{r_L} + P_{Loss}^{r_C} \tag{2-35}$$

where

$$\begin{aligned} P_{Loss}^{r_L} &= I_{Lrms}^2 \times r_L = 15.96^2 \times 0.3 = 76.42\,W \\ P_{Loss}^{r_C} &= I_{Crms}^2 \times r_C = 7.98^2 \times 0.05 = 3.18\,W \end{aligned} \tag{2-36}$$

Converter efficiency can be calculated as following:

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} = \frac{P_{out}}{P_{in}} = \frac{V_O I_O}{V_i I_i} = M_V M_I \quad ; \; M_I = 1 - D \tag{2-37}$$

Accordingly,

$$\eta = \frac{1}{1 + \frac{P_{Loss}}{V_O I_O}} = \frac{1}{1 + \frac{P_{Loss}^{IGBT} + P_{Loss}^{Diode} + P_{Loss}^{r_L} + P_{Loss}^{r_C}}{P_{out}}} = 0.96 \tag{2-38}$$

Voltage transfer ratio:

$$M_V = \frac{\eta}{1-D} = \frac{1}{1-D}\frac{1}{1 + \frac{P_{Loss}}{V_O I_O}} = \frac{1}{1-D}\frac{1}{1 + \frac{P_{Loss}^{IGBT} + P_{Loss}^{Diode} + P_{Loss}^{r_L} + P_{Loss}^{r_C}}{P_{out}}} = 2 \tag{2-39}$$

2-3 Thermal modeling

Although all the power electronic components encounter several failures with the different mechanisms, power semiconductors such as IGBT and diode have the lion's share in power electronic devices' failures. Accordingly, almost all the researchers dealing with power electronic reliability have paid a considerable attention to thermal related issues of power semiconductors. Accordingly, obtaining a comprehensive thermal model with a precise and accurate modeling of the junction temperature plays a major role in reliability assessment.

In the next section, a brief heat sink design will be studied. In this stage, although there are lots of key factors and parameters being able to affect the design procedure (such as all the multi-physics problems) [216]–[218], by avoiding going into great detail (viscous flow and thermodynamics issues) and employing previous works a compact and tentative procedure has been used. Secondly, static and dynamic individual thermal modeling of a chip (either IGBT or diode) will be studied. This section makes a practical case for validating the new proposed mathematical model via steady state and transient simulation results in ABAQUS environment.

2-3-1 Heat sink design and validation

In this section, conventional heat sink, namely trapezoidal plate-fin heat sink, in forced convection heat transfer condition will be designed. It is worth mentioning that there are lots of heat sink types commercially available [216]. However, owing to the wide applications of plate-fin heat sinks [217], [218], only this kind of well-known heat sink will be considered in this study. Regarding previous section, in the nominal condition power loss in IGBT chip is about 30.74 W while for diode chip is about 14.13. Based on these values and based on the conventional static thermal equivalent circuit model including only thermal resistances, required thermal resistance of heat sink can be easily calculated. Therefore, by estimating this thermal resistance, one can continue either mathematical thermal modeling or simulations. In this part of study, despite roughly inaccurate responses in thermal modeling in comparison with 3D representation, only 1D representation of heat transfer (with only thermal resistances) have been employed. It is worth mentioning that this kind of modeling has been only used for heat sink designing and would have been validated by simulations. However, after heat sink designing, an accurate thermal model will be proposed in which all the thermal dynamics and thermal cross couplings have been considered.

2-3-1-1 Heat sink thermal resistance

The IGBT and diode chips mounted on a single heat sink have been depicted in Fig. 2-12. $R_{th(j-c)}$, $R_{th(c-h)}$ and $R_{th(h-a)}$ are thermal resistances of junction to case, case to heat

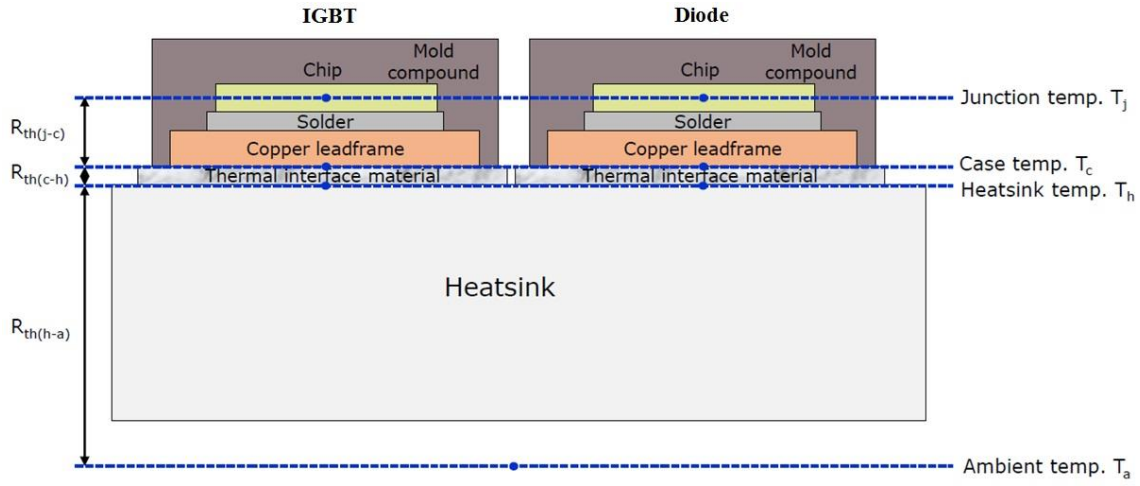


Fig. 2-12. Physical configuration of IGBT and Diode.

sink and heat sink to ambient, respectively. All the temperature nodes are defined in the figure. The main goal is to estimate $R_{th(h-a)}$. Regarding Fig. 2-12, one can find that this configuration induces a thermal coupling between both chips. Therefore, simultaneously discussing of thermal modeling using thermal impedance matrix seems necessary [219], [220]. This study will be carried out in the last section of the current chapter.

Regarding obtained results and the depicted structure in Fig. 2-12, static thermal equivalent circuit model can be drawn in Fig. 2-11 [220]. As it is shown in Fig. 2-11, there are two thermal paths. Therefore, by writing KTL (Kirshoff Thermal Law) on this two closed loops, one can find the following equations:

$$\begin{aligned} T_j^{IGBT} &= P_{Loss}^{IGBT}(R_{th(j-c)}^{IGBT} + R_{th(c-h)}^{IGBT}) + (P_{Loss}^{IGBT} + P_{Loss}^{Diode})R_{th(h-a)} + T_a \\ T_j^{Diode} &= P_{Loss}^{Diode}(R_{th(j-c)}^{Diode} + R_{th(c-h)}^{Diode}) + (P_{Loss}^{IGBT} + P_{Loss}^{Diode})R_{th(h-a)} + T_a \end{aligned} \quad (2\text{-}40)$$

where P_{Loss}^{IGBT} and P_{Loss}^{Diode} are the power loss in IGBT and diode, respectively, T_j^{IGBT} and T_j^{Diode} are the junction temperatures of IGBT and diode, respectively. Therefore, one can easily calculate heat sink to ambient thermal resistance as follows:

$$\begin{aligned} R_{th(h-a)} &= \frac{T_j^{IGBT} - T_a - P_{Loss}^{IGBT}(R_{th(j-c)}^{IGBT} + R_{th(c-h)}^{IGBT})}{(P_{Loss}^{IGBT} + P_{Loss}^{Diode})} \\ R_{th(h-a)} &= \frac{T_j^{Diode} - T_a - P_{Loss}^{Diode}(R_{th(j-c)}^{Diode} + R_{th(c-h)}^{Diode})}{(P_{Loss}^{IGBT} + P_{Loss}^{Diode})} \end{aligned} \quad (2\text{-}41)$$

All of the right side parameters of equation (2-41) are known (either calculated or extracted from datasheet). Between two equations of (2-41), the lower heat sink to ambient thermal resistance has to be considered. $R_{th(j-c)}^{IGBT}$ and $R_{th(j-c)}^{Diode}$ are 1.15°C/W

and 1.9℃/W, respectively [213]. For both IGBT and diode, the same thermal interface material with 0.5℃/W thermal resistance (at 400 psi) has been used.

Therefore, from equations (2-41), $R_{th(h-a)}$ can be calculated as 1.16℃/W and 1.53℃/W (for the worst case, junction temperatures in both IGBT and diode are assumed to be 170℃ and ambient temperature is assumed to be 40℃. We also assumed that both IGBT and diode have been aged and their junction-to-case thermal resistances have increased by 20% leading to 1.38℃/W and 2.3℃/W, respectively. In this degraded case, the internal on-state resistances of IGBT and diode have become 165% (39.34×165%) and 200% (23.34×200%) nominal values, respectively, i.e. 20% increase in either IGBT collector-emitter voltage or diode forward voltage. Therefore, the power losses of IGBT and diode can be calculated 35.9W and 17.4W, respectively).

Since, the chips are not identical, the required thermal resistance is the smaller of the two above-mentioned values. Accordingly, $R_{th(h-a)}$=1.16℃/W will be taken into account. At the end of this section, we support the claim that this thermal resistance would be sufficient for our converter thorough simulation.

2-3-1-2 Heat sink design

In this section, the procedure of the heat sink design will be briefly explained. Fig. 2-13 has depicted the IGBT and diode devices mounted on the back of plate-fin heat sink. The distance between these two devices should be estimated as a trade off between cooling quality and parasitic inductance in power circuit [216]. There are lots of physical issues having to be known such as computional fluid dynamic and heat transfer as a background for heat sink design. However, stating them here seems to be beyond this study and interested readers are refered to [216]–[218]. It is also mentioned that the goal of this section is not to optimize the heat sink.

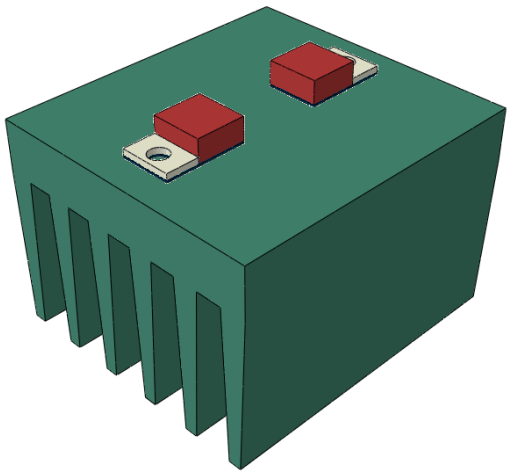


Fig. 2-13. Assembly of chips on the heat sink

Heat transfer types fall into three categories, conduction (Fourier's law), convection (Newton cooling law) and radiation (Stefan-Boltzmann) [216]. Regarding Fig. 2-12, the heat transfers from heat sources (namely IGBT and diode chips) as a conductive heat transfer mode to the lead frame of the chips thorough solder areas and then conduct to the heat sink. After that this amount of heat dissipates into the ambient thorough heat sink fins and flat plates (external sections of heat sink including the plates where the chips are located on and the side plates) in convective and radiating heat transfer modes. In comparison with the convective heat transfer coefficient of fins, radiating heat transfer coefficient can be neglected. While, in the heat sink outer plates, the effect of radiating heat transfer should be taken into account. With regard to the length of fins, one can assume that temperature distribution (temperature gradient) and fins' area are both non-uniform. It means that heat transfer will not be uniform along with the fins of heat sink. Accordingly, a coefficient called fin efficiency is defined to take into consideration this non-uniformity in the temperature gradient and fins' area [216]–[218]. This coefficient makes a significant contribution in this kind of analysis. Therefore, here a complete discussion would be carried out.

2-3-1-2-1 Convective heat transfer

Fig. 2-14 shows the plate-fin heat sink with its in-detail dimensions. Designing heat sink is beyond this study and interested readers are referred to [217]. However, some key correlations are described here. In the air forced convection, the fluid flowing pattern completely depends on length and roughness of channels surfaces in which air is blowing. Fig. 2-15 shows the fluid pattern along the length of channel. Empirical correlations have been proposed to consider two merged Nusselt numbers (i.e. developing and developed).

$$Nu_i = \left[\left(\frac{1}{Nu_{fd}} \right)^3 + \left(\frac{1}{Nu_{dev}} \right)^3 \right]^{-1/3} = \frac{h_i \Gamma}{k_{air}} \tag{2-42}$$

where Nu_i is ideal Nusselt numbers and Nu_{fd} and Nu_{dev} are fully developed and developing parts of Nusselt numbers, respectively. h_i is ideal convective heat transfer coefficient. k_{air} is the air thermal conductivity and Γ is a characteristics length and defined by:

$$\Gamma = \frac{2c_{hs}s_{hs}}{2c_{hs} + s_{hs}} \tag{2-43}$$

where s_{hs} is average fin spacing. Fully developed and developing parts of Nusselt numbers are defined as follows for $0.26<R^*_{eb}<175$ [221]:

$$Nu_{fd} = 0.5 \times R^{*}_{eb} \times Pr$$

$$Nu_{dev} = 0.664\sqrt{R^{*}_{eb}}\, Pr^{1/3} \sqrt{\left(1 + \frac{3.65}{\sqrt{R^{*}_{eb}}}\right)} \qquad (2\text{-}44)$$

R^{*}_{eb} is the channel Reynolds number and equals to $R_{eb} \times (s_{hs}/\ell_{hs})$ in which R_{eb} is Reynolds number. Pr is Prandtl number. Reynolds number and Prandtl number are related to kinematic viscosity, thermal diffusivity, average air velocity in channels and heat sink geometry [221].

One can also calculate ideal convective heat transfer h_i from eq. (2-42). Nu_b can be estimated by applying fin efficiency to the Nu_i. Fin efficiency for trapezoidal channels can be calculated by the following expression:

$$\eta_{fin} = \frac{\mu_b}{2K^2 C_{hs}} \left\{ \frac{k_1(\mu_a) I_1(\mu_b) - I_1(\mu_a) k_1(\mu_b)}{k_1(\mu_a) I_0(\mu_b) - I_1(\mu_a) k_0(\mu_b)} \right\} \qquad (2\text{-}45)$$

where $k_0(.)$, $k_1(.)$, $I_0(.)$ and $I_1(.)$ are the first and the second term of Modified Bessel function of second kind and the first and the second term of Modified Bessel function of first kind and

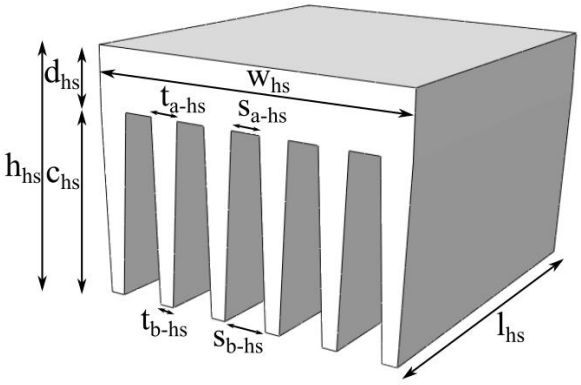


Fig. 2-14. Interested plate-fin heat sink

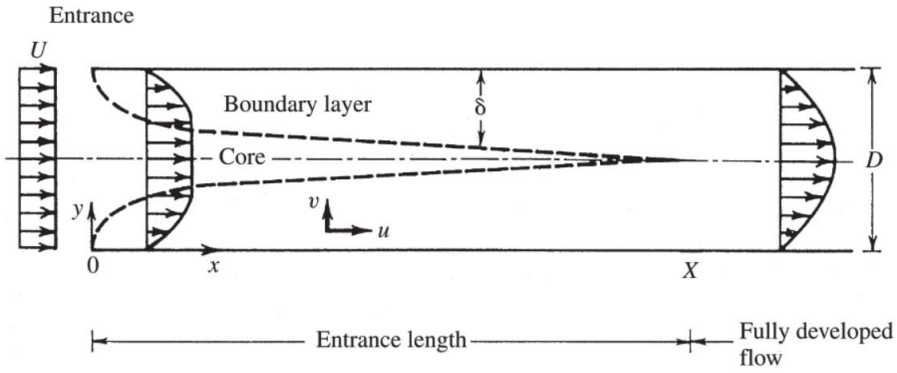


Fig. 2-15. Type of fluid flow [216]

$$\chi = \tan^{-1}\left(\frac{t_{a-hs} - t_{b-hs}}{2c_{hs}}\right) \qquad \mu_a = 2K\sqrt{\frac{t_{b-hs}(1-\tan\chi)}{2\tan\chi}}$$
$$K = \sqrt{\frac{h_i}{k_{hs}\sin\chi}} \qquad \mu_b = 2K\sqrt{\frac{c_{hs} + t_{b-hs}(1-\tan\chi)}{2\tan\chi}} \tag{2-46}$$

Accordingly,

$$Nu_b = \eta_{fin} Nu_i \tag{2-47}$$

where Nu_b is the actual Nusselt number and η_{fin} is expressed by equation (2-45). And

$$h = \frac{k_{air} Nu_b}{\Gamma} \tag{2-48}$$

Now, thermal resistance of fins can be easily obtained by

$$R_{th-fin} = \frac{1}{hA_{fin}}$$
$$A_{fin} = (n_{fin} - 1)(s_{hs} + 2c_{hs})\ell_{hs} \tag{2-49}$$

where n_{fin} is the number of fins in the considered heat sink.

Other parts of the heat sink are also exposed to the ambient and accordingly should be taken into consideration in our calculation. The plates of heat sink (side plates) are also exposed to the ambient. For estimating convective heat transfer coefficient on the heat sink plates, the following equations based on the mathematical model in [216] will be employed,

$$Nu_{plate} = ((Nu_{laminar})^m + (Nu_{turbulant})^m)^{1/m}; \qquad 10^{-1} < Ra < 10^{12}$$
$$Nu_{laminar} = \frac{2}{\ln(1 + 2/(C_{laminar} Ra_{plate}^{1/4}))}$$
$$Nu_{turbulant} = \frac{C_{turbulant} Ra_{plate}^{1/3}}{1 + 1.4\times10^9 \times Pr/Ra_{plate}} \tag{2-50}$$

where Ra is the Rayleigh number and is defined as follows:

$$Ra_{plate} = \frac{g\beta_{air}(T_{base} - T_\infty)Pr\,\ell_{hs}^{\,3}}{\nu_{air}^2} \tag{2-51}$$
$$C_{laminar} = 0.103 \qquad C_{turbulant} = 0.515 \qquad m = 6$$

It should be mentioned that all of these side plates are in vertical orientation and consequently, above-mentioned correlation can be simultaneously apply to all of them. Accordingly, thermal resistance of these plates can be obtained by

$$R_{th-plate} = \frac{1}{h_{plate} A_{plate}} = \frac{\ell_{hs}}{k_{air} Nu_{plate} A_{plate}} = \frac{1}{k_{air} Nu_{plate} (w_{hs} + h_{hs})} \quad (2\text{-}52)$$

Therefore, all the convection thermal resistances have been estimated.

2-3-1-2-2 Radiating heat transfer

In the case of natural convection, thermal radiation heat transfer is also significant and should be considered. Only the heat sink plates, namely, side plates, will be under discussion (fin thermal radiation heat transfer has been neglected). It is assumed that the heat sink is surrounded by an atmosphere at the given ambient temperature (here40°C). In these conditions, as it was mentioned earlier, thermal radiation heat transfer is expressed by the general Stefan-Boltzmann equation as follows [217]:

$$q_{rad} = \varepsilon_{rad} \sigma A_{rad} (T_{base}^4 - T_a^4) \quad (2\text{-}53)$$

where ε_{rad} is the emissivity of the solid (heat sink), σ is the Boltzmann constant ($5.669\times10^{-8} W/m^2K^4$) and A_{rad} is the surface area of thermal radiation and is defined as follow:

$$A_{rad} = 2(\ell_{hs}(c_{hs} + d_{hs}) + w_{hs} d_{hs}) + \ell_{hs} w_{hs} \quad (2\text{-}54)$$

All the above parameters and dimensions have been defined in Fig. 2-16. Regarding the considered wall temperature, the emissivity for aluminum heat sink is assumed to be 0.09 [216], [217].

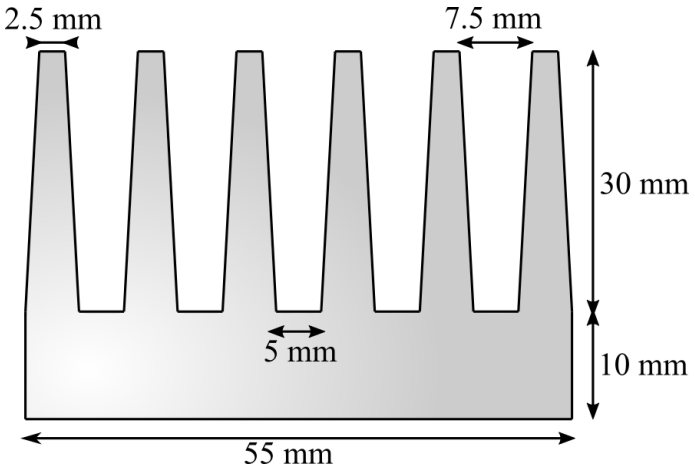


Fig. 2-16. Plate-fin heat sink dimensions

2-3-1-2-3 Total heat sink thermal resistance

Fig. 2.17 demonstrates the equivalent thermal circuit of heat sink. There are four various thermal resistances according to heat transfer mechanisms previously discussed. $R_{th\text{-}rad\text{-}plate}$ is the equivalent thermal resistance of heat sink owing to radiating heat transfer and can be calculated from eq. (2-53). $R_{th\text{-}base}$ is thermal resistance of base area in the heat sink and defined as follows

$$\begin{aligned} R_{th-base} &= R'_{th-base} + R_{th-spread} \\ R'_{th-base} &= \frac{d_{hs}}{k_{base} A_{base}} = \frac{d_{hs}}{k_{base} \ell_{hs} w_{hs}} \\ R_{th-spread} &= \frac{1 - 1.41\gamma + 0.344\gamma^3 + 0.013\gamma^5 + 0.034\gamma^7}{4 k_{hs} a} \end{aligned} \tag{2-55}$$

Where $R'_{th\text{-}base}$ is the thermal resistance of base part of heat sink in the case in which heat flux density is assumed to be uniform and heat flux is only transferred in one direction, $R_{th\text{-}spread}$ is the spreading thermal resistance [222] and considers non-uniformity of the heat flux through heat sink base thickness, γ is the ratio of total heat sources surface and the heat sink base area, *a* is the square root of total heat sources surface and k_{hs} is the thermal conductivity of heat sink. Regarding Fig. 2-17, total thermal resistance can be estimated by

$$R_{th(h-a)} = \frac{(R_{th-fin} + R_{th-base}) R_{th-plate} R_{th-rad-plate}}{(R_{th-fin} + R_{th-base}) R_{th-plate} + (R_{th-fin} + R_{th-base}) R_{th-rad-plate} + R_{th-rad-plate} R_{th-plate}} \tag{2-56}$$

Employing above-mentioned equations describing the thermal resistance of heat sink, one can readily calculate the heat sink length (ℓ_{hs}) and the fan speed. A fan with the model of AFB0612DH has been employed and the air velocity has been considered as 8 m/s. As it was mentioned previously, the goal is not to design and optimize the heat sink. We will use a commercially available plate-fin heat sink. Accordingly, a heat sink with the material properties of Aluminum-6 series (6061) and physical dimensions indicated in Fig. 2-16 has been selected.

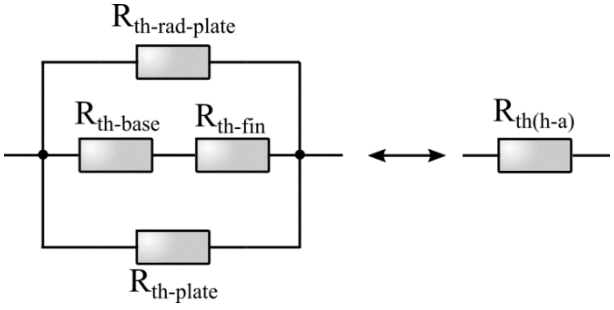


Fig. 2.17. Equivalent thermal circuit of heat sink according to the various heat transfer mechanisms

From equation (2-41), $R_{th(h-a)}$=1.16°C/W. ℓ_{hs} should be calculated so that $R_{th(h-a)}$ becomes 1.16°C/W. Therefore, based on the above-mentioned equations, some codes have been written in MATLAB environment. Finally, the proper length of heat sink for dissipating 53.4 Watt heat power to the environment is calculated as ℓ_{hs}=6cm.

Regarding to the temperature-dependent inherent of physical parameters such as air density, thermal conductivity of air and aluminum, Prandtl number, Reynolds number, kinematic viscosity, etc in heat sink designing, all heat sink designing-related equations have been considered in different base temperatures from 50°C to 160°C. These temperature dependancies lead to different forced, natural and radiating heat transfer coefficients as shown in Fig. 2-18. Based on this figure, forced convective heat transfer coefficient does not change significantly by base temperature variation due to its forced air flowing. On the other side, natural convective heat transfer coefficient i.e. external plates considerably varies by base temperature variation. It is not the case in which equivalent radiating heat transfer coefficient experiences a roughly constant trend versus base temperature variation. Totally, thermal resistance does not have a significant changes owing to its massive resistance share of forced convection. Thermal values are listed in Table 2-3. Steady state thermal behavior of the global system has been carried out in Appendix A.

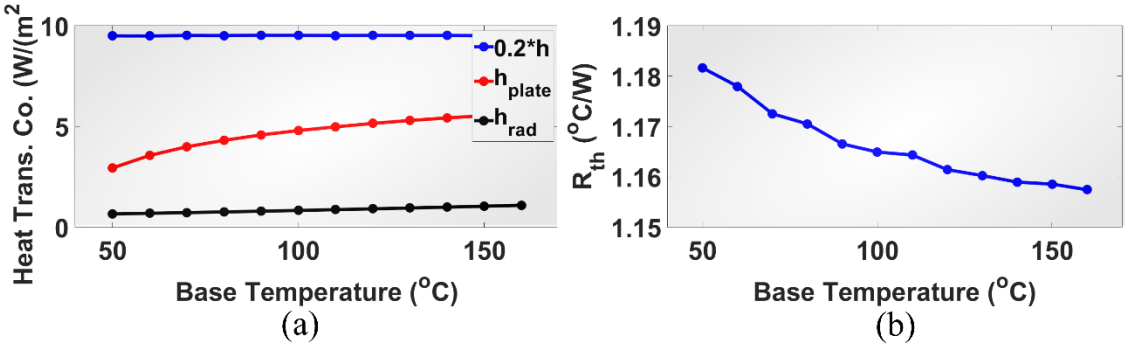


Fig. 2.18. Temperature dependencies of a) heat transfer coefficients and b) heat sink thermal resistance.

Table 2-3 Heat sink Dimensions and Thermal Parameters Values

Parameter	Value
Emissivity	0.09
Natural convection heat transfer of the external plates	2.8 W.m^{-2}.K^{-1} (50°C) 5.5 W.m^{-2}.K^{-1} (160°C)
Forced convection of fin	47.5 W.m^{-2}.K^{-1}(50°C) 47.52 W.m^{-2}.K^{-1}(160°C)
IGBT junction-case thermal resistance	1.15 °C/W
Diode junction-case thermal resistance	1.9 °C/W
Thermal film resistance	0.5 °C/W

2-3-2 Thermal modeling

There are lots of thermal modeling approaches [219]. The simplest and readily-available approach is the use of 2D thermal lumped RC equivalent circuits. In 2D thermal modeling, there are various models including Time-Domain Estimation, Fast Fourier Transform FFT, FFT with Overlap-Add method and Breaking down the mission profile into single pulses. However, analytical solution based on the defined impedance network i.e. Foster and Cauer has been applied here owing to its high accuracy and its less time consuming in comparison with the others [215].

Assume that ambient temperature and both power losses in IGBT and diode are constant and equal to 40℃, 36W and 17.4W, respectively. Other thermal parameters, $R_{th(j-c)}^{IGBT}$ and $R_{th(j-c)}^{Diode}$ are 1.4℃/W and 2.3℃/W, respectively. The simple thermal equivalent circuit is redrawn in Fig. 2-11. Based on this figure, junction tempratures of IGBT and diode can be calculated as follows

$$\begin{aligned} T_j^{IGBT} &= P_{Loss}^{IGBT}(R_{th(j-c)}^{IGBT} + R_{th(c-h)}^{IGBT}) + R_{th(h-a)}(P_{Loss}^{IGBT} + P_{Loss}^{Diode}) + T_a \\ T_j^{Diode} &= P_{Loss}^{Diode}(R_{th(j-c)}^{Diode} + R_{th(c-h)}^{Diode}) + R_{th(h-a)}(P_{Loss}^{IGBT} + P_{Loss}^{Diode}) + T_a \end{aligned} \quad (2\text{-}57)$$

Regarding above mentioned equations, any changes in either P_{Loss}^{IGBT} or P_{Loss}^{Diode} can affect both chips junction temperatures. In addition, any changes in $R_{th(j-c)}^{IGBT}$ or $R_{th(j-c)}^{Diode}$ influence the chip junction temperature in which the thermal parameter deviation has been occurred (for instance, 20% increase in $R_{th(j-c)}^{Diode}$ can change the junction temperature of diode by 6.2℃) and also have a knock-on effects on the other ones as described in the following sentences. When $R_{th(j-c)}^{IGBT}$ ($R_{th(j-c)}^{Diode}$) increases, consequently T_j^{IGBT} (T_j^{diode}) also increases resulting in power loss P_{Loss}^{IGBT} (P_{Loss}^{Diode}) increase. Finally, this power loss increase indirectly makes the diode junction temperature T_j^{diode} (IGBT junction temperature T_j^{IGBT}) become a little higher. The complete thermal model considering the thermal coupling effects will be employed and applied to the thermal system. Accordingly, following matrix equation should be solved after estimating all of its elements by performing finite element analysis (FEA) via ABAQUS. In this case, in addition to static thermal model, transient thermal model (including thermal impedances) are available making our calculation much more accurate.

$$\begin{bmatrix} T_j^{IGBT} \\ T_j^{Diode} \end{bmatrix} = \begin{bmatrix} Z_{IGBT} & Z_{IGBT-Diode} \\ Z_{Diode-IGBT} & Z_{Diode} \end{bmatrix} \begin{bmatrix} P_{Loss}^{IGBT} \\ P_{Loss}^{Diode} \end{bmatrix} + T_a \quad (2\text{-}58)$$

Each of the thermal impedance matrix elements is a thermal impedance showing the thermal dynamic behaviour of the considered thermal model. It is worth mentioning that the different thermal impedances of the different layers are thoroughly

boundary conditions dependant. For instance, the amount of power loss as well as the cooling system (free or forced convection or even fixed temprature) can affect the material thermal properties specially thermal conductivity resulting in different thermal impedances [219]. Accordingly, regarding different power losses in IGBT and diode (almost always IGBT power loss is greater than diode's), it seems to have unequal cross coupling thermal impedances ($Z_{IGBT\text{-}Diode} \neq Z_{Diode\text{-}IGBT}$) [219], [220]. It should be also mentioned that the cross coupling thermal impedances are drastically position-dependant. It means that the position where IGBT or diode have been mounted on the heat sink will affect cross coupling thermal impedances [220]. For simplicity, the position is fixed and optimizing the position is not considered.

There are two conventional thermal impedance models, namely, Foster (mathematical model) and Cauer (physical model). These two models are depicted in Fig. 2-19. Almost all of the semiconductor manufacturers are providing the Foster model for their components' datasheets due to its simplicity. Although this model is really simple, it cannot physically describe the exact thermal behaviour among different layers. Both self thermal impedance and cross coupling thermal impedance are assumed to have Foster model due to availibility of this model in the most of datasheet and its simplicity. In the Foster model, mathematical equation expressing the temprature behaviour is as follows

$$Z_{th} = \sum_{i=1}^{n} R_{thi}(1 - e^{-t/\tau_i}) \tag{2-59}$$

Where n is the total number of the Foster layer, R_{thi} and τ_i are the i^{th} thermal resistance and thermal time constant, respectively.

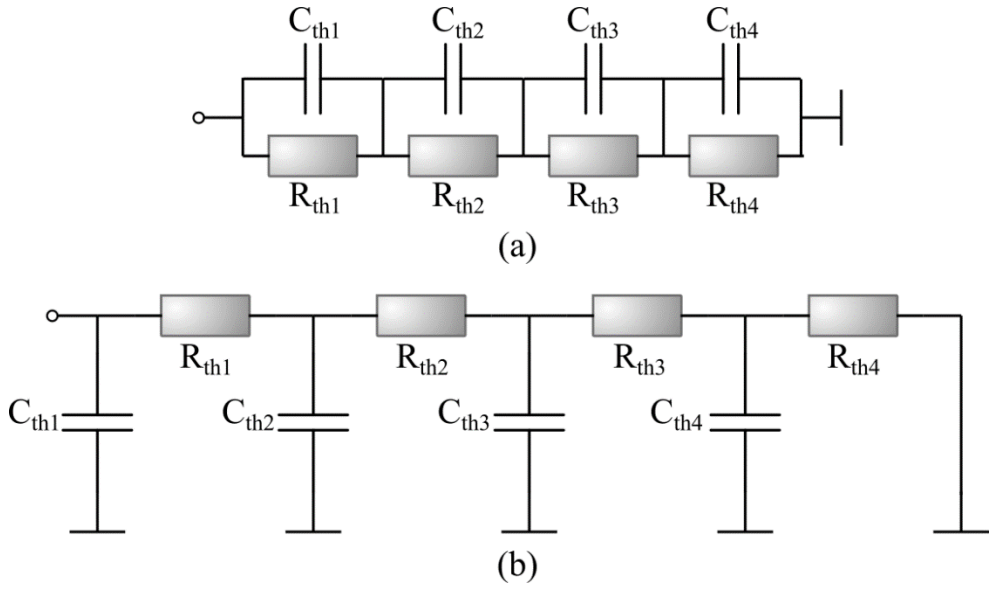


Fig. 2. 19. Thermal model. (a) Foster model, (b) Cauer model.

For obtaining the thermal impedance matrix elements in equation (2-58), one can easily use superposition theory resulting in following equations [219], [220]:

$$\begin{cases} Z_{IGBT} = \dfrac{T_j^{IGBT} - T_a}{P_{Loss}^{IGBT}} & P_{Loss}^{Diode} = 0 \\ Z_{IGBT-Diode} = \dfrac{T_j^{IGBT} - T_a}{P_{Loss}^{Diode}} & P_{Loss}^{IGBT} = 0 \\ Z_{Diode-IGBT} = \dfrac{T_j^{Diode} - T_a}{P_{Loss}^{IGBT}} & P_{Loss}^{Diode} = 0 \\ Z_{Diode} = \dfrac{T_j^{Diode} - T_a}{P_{Loss}^{Diode}} & P_{Loss}^{IGBT} = 0 \end{cases} \quad (2\text{-}60)$$

Accordingly, one can easily calculate both self and cross coupling thermal impedances. For this reason, two separate simulations (in transient mode) have been done. In these simulations a step power loss has been applied to the chips (diode or IGBT), and mean-temperature responses of their chips' surfaces have been monitored. The process of thermal impedance extraction is shown in Fig. 2-20. These simulations have been been performed in ABAQUS in transient heat transfer mode with the variable step time (short step ($1\mu s$) at the beginning and long step ($10ms$) at the end of simulation time). Boundary conditions are the same as static heat transfer analysis mentioned in Appendix A. Sink temperature is considered $40℃$ and film coefficient of the fins and the plates of the heat sink are those calculated in the previous section.

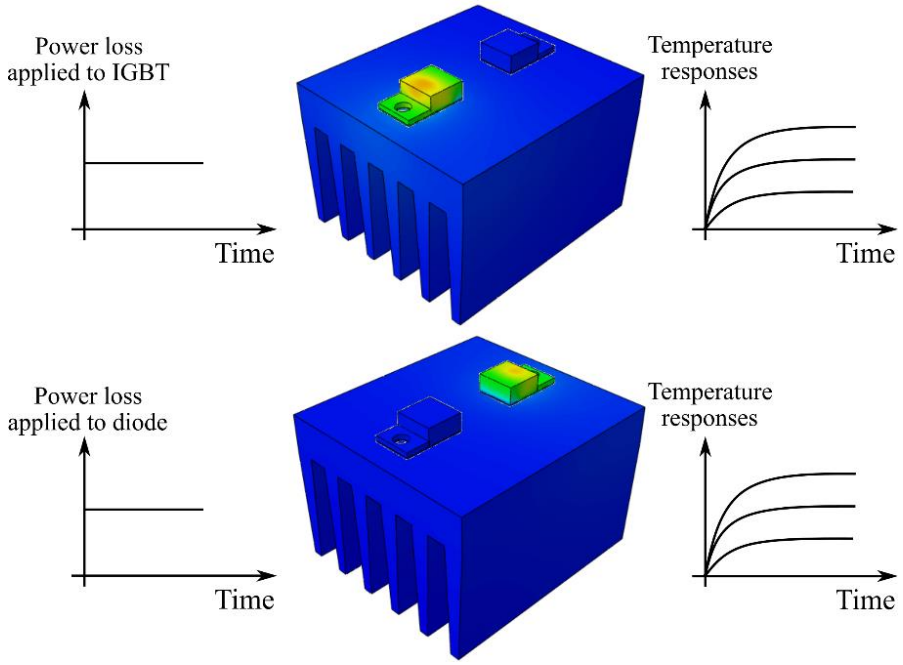


Fig. 2-20. Process of thermal impedance extraction

From these simulations, both self and cross coupling thermal impedances have been derived. The thermal impedance traces are shown in Fig.2-21. Regarding these figures, all of the thermal impedances have been in steady state in maximum 1000 sec. As it was expected, the coupling impedances, namely $Z_{IGBT\text{-}Diode}$ and $Z_{Diode\text{-}IGBT}$, do not have the same values (see Fig. 2-21). This inequality is due to the different amount of power losses in the chips.

As it is explained, a 4-layer Foster thermal model (Fig. 2-22) can accurately express the transient thermal behaviour of either self or coupling impedances. The parameters of thermal Foster model have been fitted by curve fit tool of MATLAB software. The final curve fitted parameters of Foster model for all of thermal impedances are listed in Table. 2-4. All the fitted curves have been depicted in Fig. 2-23.

Table 2-4. Parameters of Foster model of Thermal impedances according to equations (2-59) and (2-60)

Foster Model	Layer 1		Layer 2		Layer 3		Layer 4	
Thermal impedance	$R_{th\text{-}1}$	$1/\tau_1$	$R_{th\text{-}2}$	$1/\tau_2$	$R_{th\text{-}3}$	$1/\tau_3$	$R_{th\text{-}4}$	$1/\tau_4$
Z_{IGBT}	0.5201	0.2994	0.3225	100	1.152	0.0048	1.001	2.339
Z_{Diode}	0.7399	0.336	1.218	2.628	0.5163	130	1.482	0.0048
$Z_{IGBT\text{-}Diode}$	0.001379	0.01475	0.0004025	0.01819	1.186	0.004598	0.01089	0.0166
$Z_{Diode\text{-}IGBT}$	0.002431	0.0137	0.007033	0.01305	0.004667	0.01602	1.104	0.004614

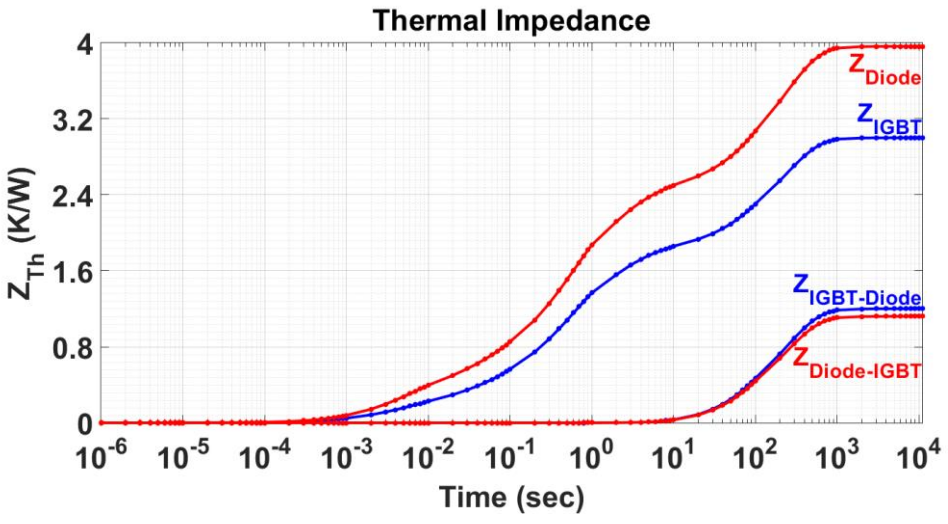


Fig. 2. 21. Thermal impedences of complete thermal model

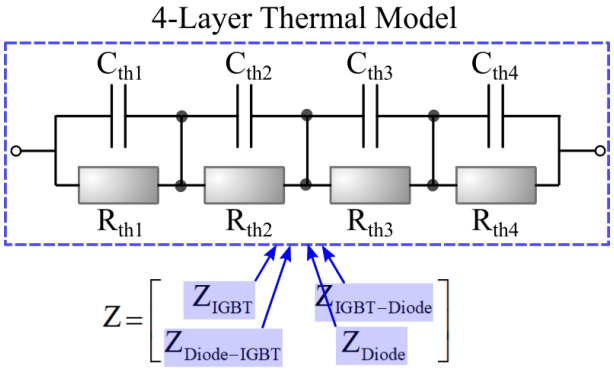
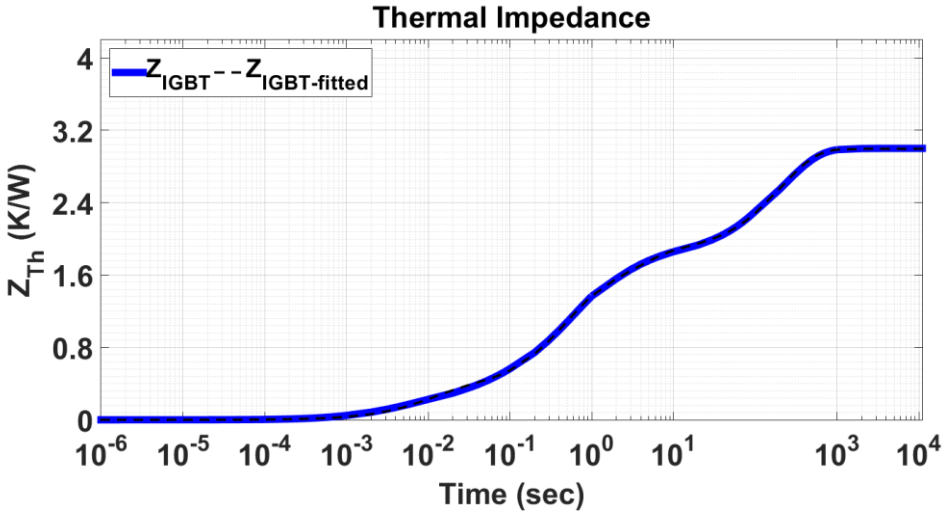


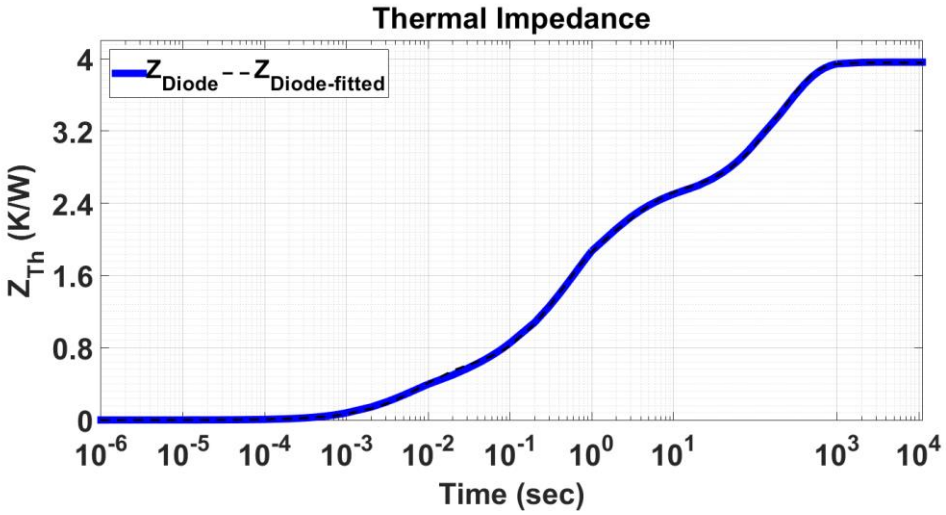
Fig. 2. 22. 4-layer Foster thermal model expressing thermal impedances

2-4 Conclusion

In this chapter, electrical, thermal and power loss models have been presented. Time invariant multi frequency modeling has been employed and applied to the conventional DC-DC boost converter for electrical modeling. The results showed that this model has a highly precision in estimating electrial quantities. Voltage and current ripples were both well estimated by using three-order coefficients of Fourier series. Power loss modeling has been presented based on the manufacturer's correlations with 10 iteration for considering temperature dependencies. Finally, the forced convection heat sink design was launched and a complete thermal model was extracted using ABAQUS environment. Since, proposed reliability evaluation is based on mission profile and consequently depends on thermal and electrical operating points of power converter, experssing accurate electrical and thermal models play important roles in useful lifetime estimation of power components. Accordingly, the results of this chapter will apply to the proposed approach which will be throughly discussed in Chapter 5.



(a)



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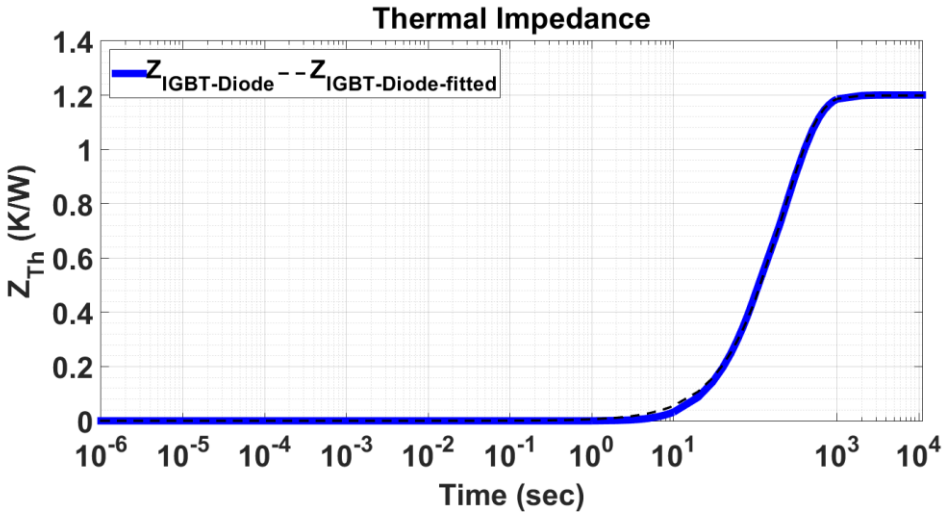
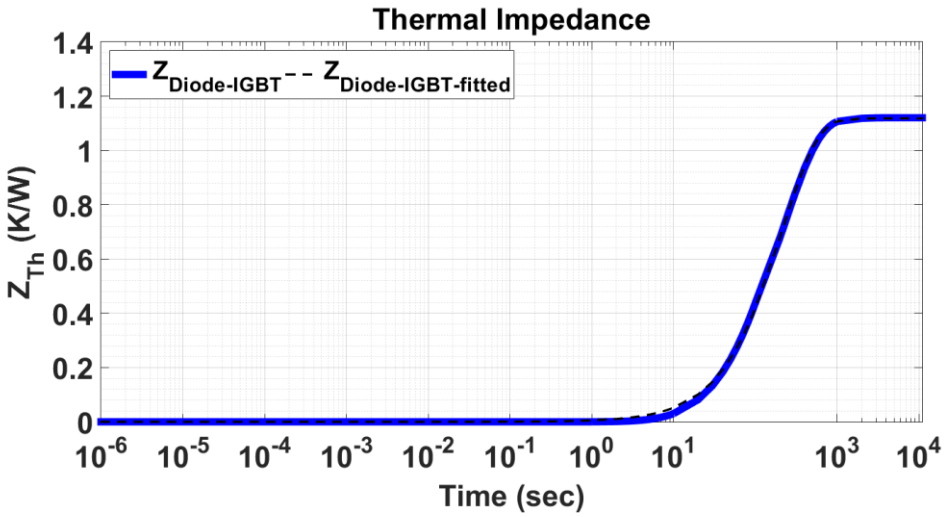


(c)



(d)

Fig. 2. 23. Curve fitted of thermal impedances, a) Z_{IGBT}, b) Z_{Diode}, c) $Z_{IGBT\text{-}Diode}$, d) $Z_{Diode\text{-}IGBT}$.

3

Experimental Procedure

Several experiments and tests were designed and performed through this study for making data for validating the different aspects of the newly proposed methods. This chapter deals with the experimental procedures in which the design procedures and algorithms are thoroughly discussed. All the test benches, circuits, standards, conditions and equipment and their objectives are investigated. Thermo sensitive electrical parameter (TSEP) test bench, accelerated power cycling aging test, accelerated thermal cycling aging test, creep test, scanning electron microscope (SEM), 3D X-ray tomography and modified DC-DC boost power converter test bench are all described.

3-1 Thermo-sensitive electrical parameters (TSEP)

3-1-1 Experimental procedure

As previously mentioned, two important failure indicators, namely junction to case thermal resistance ($R_{th(j-c)}$) and on-state voltage (V_{on}) have been considered and taken into account here [36], [223]. In this study, main concentration was on the 600V 15A discrete DuoPack power IGBT including an extra internal anti parallel diode, namely IKP15N60T which was launched by Infineon Technology. Its technology is based on the trench gate field stop (TGFS) technology. The features of this technology has been discussed in details in section 1-2-3-1. It was shown that two aforementioned parameters, but much faster in junction to case thermal resistance, can be deviated through aging in discrete power IGBT and power diodes. Hence, their deviations' monitoring are important for health prognosis and reliability evaluation. Based on the fabrication technology and working conditions (especially junction temperature), it is predicted that junction to case thermal resistance of the power discrete chip reaches failure criteria in logarithmic envelope faster than on-state voltage owing to its two opposite failure mechanisms (Fig. 1-22).

Aging monitoring or health prognosis are both paramount of importance. Directly measuring on-state collector emitter voltage is achievable employing a high accurate data logger or any kind of precise voltmeters, here 6-channel data

acquisition (HBM-Gen3i). For estimating thermal resistance, one can use the following equation in direct current condition:

$$R_{th-G} = \frac{T_j - T_{ref}}{P_{DUT}} = \frac{T_j - T_{ref}}{V_{DUT} \times I_{DUT}} \quad (3\text{-}1)$$

where $R_{th\text{-}G}$ is the global thermal resistance of heat flux path (including junction to case, thermal interface material (TIM) and cold plate thermal resistances), T_j is the junction temperature of devices in steady state, T_{ref} is the reference temperature (fluid temperature here) and P_{DUT} is the power loss in the considered device under test (DUT). However, discrete chips have been electrically and mechanically protected by the rough protection cover made by epoxy resin and thereby it is impossible to directly measure the junction temperature by any kind of thermal imaging infrared camera. Hence, junction temperature has to be estimated indirectly using TSEP. Voltage drop across pn junction in power semiconductors under low bias current (I_{meas}) has been a robust representative of junction temperature [224], [225]. For silicon based power semiconductors temperature dependency is about -2mV per Kelvin [224]. Hence, one can indirectly estimate junction temperature of devices by injecting a low bias current through the device and measuring its produced voltage. In this way, junction to case thermal resistance (global thermal resistance $R_{th\text{-}G}$) can be calculated and monitored. This procedure can be applied only for a low bias current (few mA) for limiting self-heating effect of pn junction [226]. However, it cannot be very low owing to accuracy loss of voltage measurement. Thereby, there was a trade off in selecting the amount of low bias measuring current. In this study, on-state voltage of power semiconductors was considered as TSEP. Therefore, by injecting a low bias current (22.5mA) into the chip, one could measure on-state voltage and then estimate the junction temperature using a simple look-up table [227].

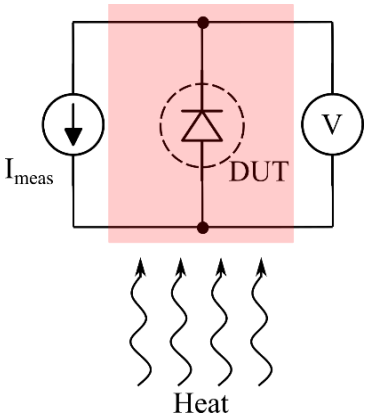


Fig. 3-1. Thermo-sensitive electrical parameter test.

The schematic of TSEP experiments is depicted in Fig. 3-1. Regarding this Figure, the power devices had been kept in the controlled oven and after reaching to the steady

state condition, low bias current was injected to the devices and the produced voltages were recorded by a highly accurate voltmeter. Several aforementioned IGBTs and diodes were under the test.

For having a large data and to be confident about the results, 20 IGBTs and 20 diodes as well were under the test. The tests were performed for different temperatures from 30°C to 170°C (maximum allowable junction temperature) with the interval of 20°C. For every distinctive temperature, 1 hour was spent to assure temperature stability in the pn junction inside the power device.

3-1-2 Results and discussion

As it was mentioned, 20 samples for each of IGBT and diode were provided. The results are shown in Fig. 3-2. It can be seen that by junction temperature increasing, IGBT and diode voltages decrease from 572.6mV to 268mV and 573mV to 288mV, respectively. Regarding equation (3-1), junction temperature estimation is required for assessing thermal resistance calculation. Therefore, IGBT and diode TSEP voltages have to be curve fitted for having access to the intermediate junction temperatures. Three polynomial correlation are considered for curve fitting. Thus (temperature is in °C and voltages are in mV):

$$T_j^{IGBT} = -7.8\times10^{-5}V_{CE}^2 - 2.15V_{CE} + 640$$
$$T_j^{Diode} = -3.2\times10^{-4}V_D^2 - 2V_D + 634.7 \qquad (3\text{-}2)$$

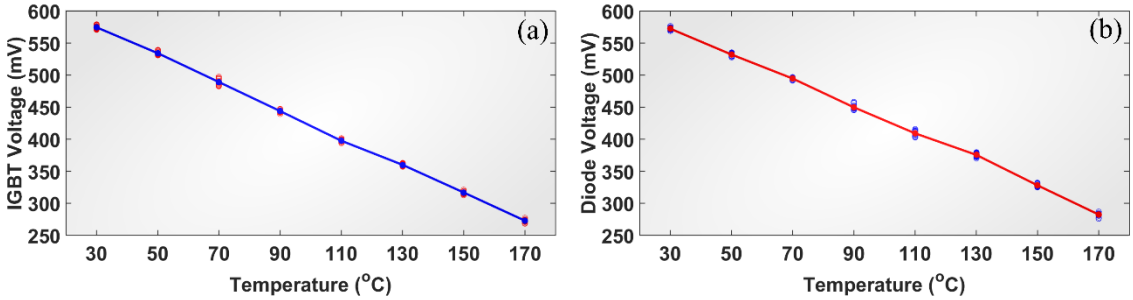


Fig. 3-2 TSEP voltages of a) IGBT and b) diode under 22.5mA low bias current

3-2 Accelerated power cycling test (APC)

3-2-1 Experimental Procedure

Electro-thermo-mechanical fatigue has been known as the most critical failure mechanism owing to the multi-layer structure of power devices and their different CTEs leading to the considerable shear and normal stresses [228]. On the contrary to the accelerated thermal cycling (ATC) aging test in which much lower heating and cooling rates (in order of some minutes to an hour) are applied to all the materials of the device, in active power cycling test much faster thermal cycles are applied to the materials close to the chip (some seconds to few minutes) for activating electro

thermo mechanical fatigue failure mechanism. The higher cooling and heating rates (faster thermal cycles), the more shear stresses induce in the different layer of power semiconductors leading to much more accelerated aging by fatigue mechanism.

A power current is periodically injected into the DUT and thereby a junction temperature swing (ΔT_j) is induced in the chip. Every heating up and cooling down in the junction of DUT has been defined as a distinct one power cycle. With regard to the internal heating of power semiconductor (making power losses in the chip), the spent time for aging is much lower in comparison with ATC. APC is continued till the failure indicators reach the defined failure criteria. The number of cycles before fulfilment of failure criteria has been considered as a number of cycles to failure (N_F) for different temperature swings and mean temperatures. In comparison to ATC, heat distribution is much less uniform in the chip leading to different failure sites in the chip while the temperature is roughly homogenously distributed in ATC tests.

With regard to real applications in which temperature swings have been internally trigged by switching and conduction power losses, inherent type of APC tests are often preferred in comparison to ATC tests. However, ATC has been also employed in order to activate different failure mechanisms such as creep.

Joint Electron Devices Engineering Council (JEDEC) standards JESD22-A105C, JESD22-A122A, JESD22-A104E, JESD659B and JESD91A are the most well-known APC testing algorithms. But, they never go into much detail of circuit design regarding different applications and various failure mechanisms. That is why various studies have been under taken by proposing their customized APC tests [168], [175], [228], [229].

There are four different strategies for accelerated power cycling tests reported in previous studies and a detailed description has been reported in [229], [230]. These are as follows:

1) Constant t_{on} and t_{off}:
Power current (I_p) is injected to the devices (DUTs) in a fixed time interval (t_{on}=cte) and also switched off in a fixed time interval (t_{off}=cte). At the beginning of the test, ΔT_j is defined at the considered value, but during the APC temperature swing and mean temperature increase due to the aging effects with no compensation by a control strategy. This strategy is the closest to real application and the most severe one. It has to be mentioned that 70% of APC tests have been done based on this method [230].

2) Constant heat sink temperature swing ($\Delta T_{heatsink}$=cte)
By online controlling the heat sink temperature, this method is achievable. This control strategy varies on-time and off-time for keeping temperature swing

constant in the heat sink. A change in the cooling and heating times would compensate the degradation effects in the devices. In comparison with strategy 1, an increase of about 50% in the number of cycles to failure has been reported in [230] employing this method.

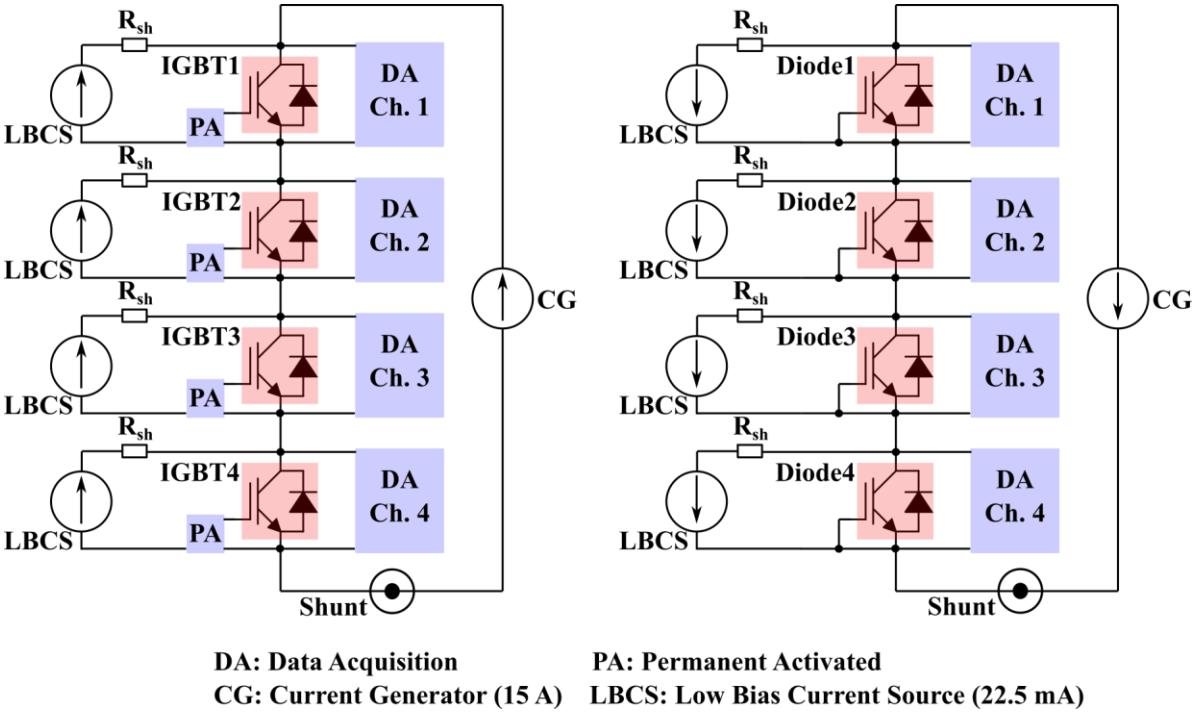
3) Constant power loss (P_{Loss}=cte)
This control strategy is based on constant t_{on} and t_{off} but with a compensation in either injecting power current or gate voltage for keeping the total power loss constant during APC. By performing this strategy, direct degradation effect of on-state voltage drop increase and indirect degradation effect of thermal resistance increase can be compensated in total power loss leading to much less severe strategy. In comparison with strategy 1, an increase of about 120% in the number of cycles to failure has been reported in [230] employing this method.

4) Constant junction temperature swing (ΔT_j=cte)
This latest strategy inspects T_{jmin} and T_{jmax} and varies t_{on} or the power current I_P to keep these parameters constant. This compensates all degradation effects and leads to the highest lifetime. In comparison with strategy 1, an increase of about 220% in the number of cycles to failure has been reported in [230] employing this method.
Different types of APC tests have been employed in recent studies generally falling into two main categories, namely DC current and Pulse Width Modulation (PWM) APC tests [165]. Although, PWM APC test is much closer to real applications owing to its switching power losses which can even activate other failure mechanisms, DC APC is much simpler and it is possible to readily perform “online” measurements of electrical and thermal indicators without stopping power cycling.

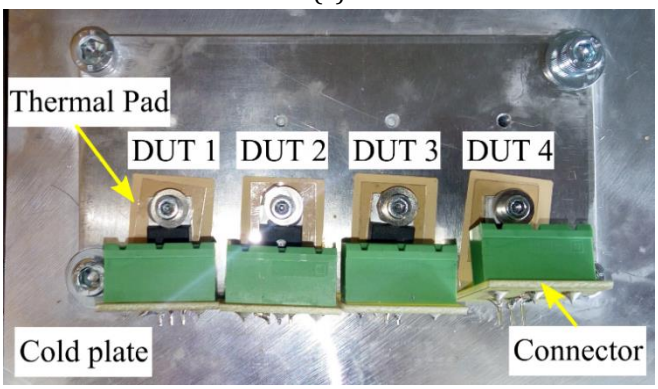
For obtaining the lifetime model of IGBT and diode, a conventional accelerated aging test (DC APC) had been performed. In this case, IGBTs and diodes were exposed to cyclic thermal variations. Accelerated power cycling aging test was employed by injecting a constant current into the IGBTs and diodes. With regard to the low working frequency of devices, solder layer degradation and aluminum delamination were the most probable failure sites [169], [181]. In the low frequency working (few kHz), the skin effect in bonding wires was not too significant and accordingly the produced heat at the connection site was not considerable in comparison with solder layer. In addition, protective epoxy resin of the discrete chips can also improve the connection site of bonding wires.

In this test, there were 8 different conditions (different mean temperatures and temperature swings) for IGBTs and power diodes. For each of them, there were 4 diodes and IGBTs for making the results much more accurate and reliable. Therefore, 32 IGBTs and 32 diodes were under the test. It has to be mentioned that all devices were screwed with a dynamometer screw driver for assuring the same conditions for all tests. In all tests, the pressure of the baseplate on the cold plate

was kept fixed at 400 psi to have the same contact thermal resistance (thermal interface material). 6-channel data acquisition (HBM-Gen^{3i}) was used. In each test, 4 channels were allocated to the four in series samples (see Fig. 3-3a), one to the trigger command and the last one was allocated to the measurement of the current passing through the devices using a very high accurate shunt resistor with a large bandwidth (LEMSYS ISM100 1 mΩ–200 MHz, -3dB).



(a)



(b)

Fig. 3-3. Devices under test. a) Schematic circuit of IGBTs and diodes under test, b) mounted DUTs on cold plate

For avoiding catastrophic failure and changes in the failure mechanisms, a maximum current of 15 A was injected in the devices (15A is the current rating of the device). This current injection led to a conduction power loss in the device which was finally leading to a temperature rise in the devices' dies until T_{jmax}. It should be noted that the devices were mounted on a cold plate with the fixed temperature (see

Fig. 3-3b). Therefore, after stopping current injection, the temperature of devices decreased to the temperature of cold plate (so called T_{jmin}). The relaxing time for the devices was much more than injecting time to make sure that the devices' junction temperatures have reached to T_{jmin}. This accelerated power cycling test had continued until devices reach their failures (on-state voltage or thermal resistance). Since the reference temperature was the cold plate (flowing fluid inside the cold plate), this procedure led to estimating global thermal resistance including junction to case, thermal interface material and plate thermal resistances as shown in Fig. 3-4. Therefore, increases in the global thermal resistance might be due to degradations of device, TIM and cold plate or a combination thereof. On the contrary to the cold plate made from aluminum, thermal interface material was aging through the APC tests. It has to be mentioned that TIM's degradations and their shares were taken into account in the junction to case thermal resistance estimation.

Fig. 3-5 demonstrates the test bench for this accelerated power cycling test. The test bench included high current generator, a PC for controlling high current pulses, device under test (DUTs) mounted on the cold plate and data acquisition systems.

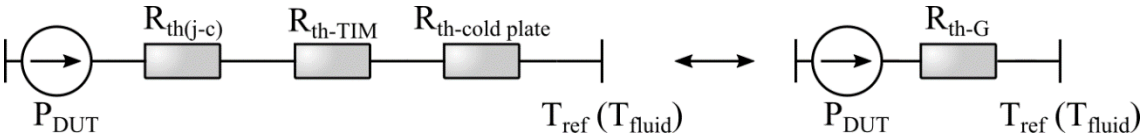


Fig. 3-4. Global thermal resistance.

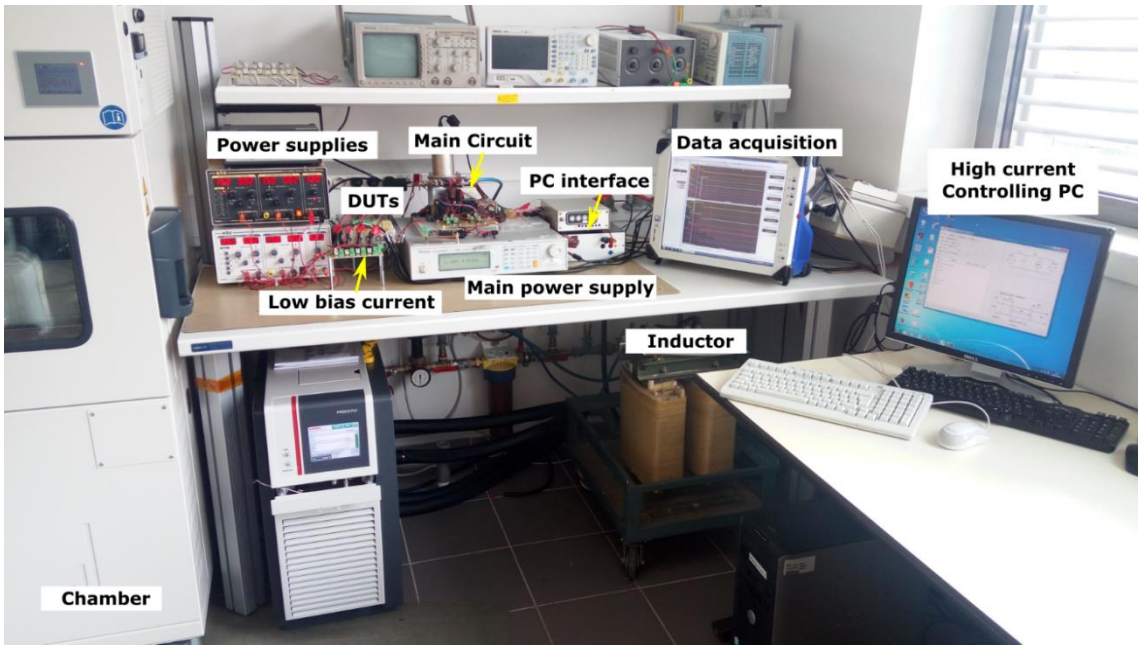


Fig. 3-5. Implemented test bench for power cycling and thermal cycling accelerated aging tests.

In order to make the current generator, a power circuit as shown in Fig. 3-6a was employed. Its switching pattern has been also shown in Fig. 3-6b. In this circuit, some amount of energy was saved in the inductor (L) by turning the MOS1 on (see

first part in the time period). In this period of time input power supply (I_P) prepared energy in L. In the second part of the time period (switching transition between MOS1 and MOS2), I_P is injected to DUTs as shown in Fig. 3-6. There was a time overlap (t_{OL}) in switching transition to assure continuity of inductor current. An accurate 1-mΩ shunt resistor (LEMSYS ISM100) is used to measure the current passing through DUTs (15A). Since measuring current (22.5mA) was continuously injected into the DUTs, D_1 was put in the power circuit to avoid bypass current through MOS2 and MOS1.

As mentioned in the previous sections, regarding to the frequency and power semiconductor packaging, solder layer degradation and aluminum delamination are the most critical failure sites in the power semiconductors. Solder layer degradation as well as aluminum delamination can influence on-state voltage and junction-case thermal resistance values. Accordingly, these two parameters had been measured during this accelerated power cycling aging test every cycle. These two variables were considered as the failure indicators. Therefore, power cycling test had continued till one of these failure indicators exceeded their failure criteria.

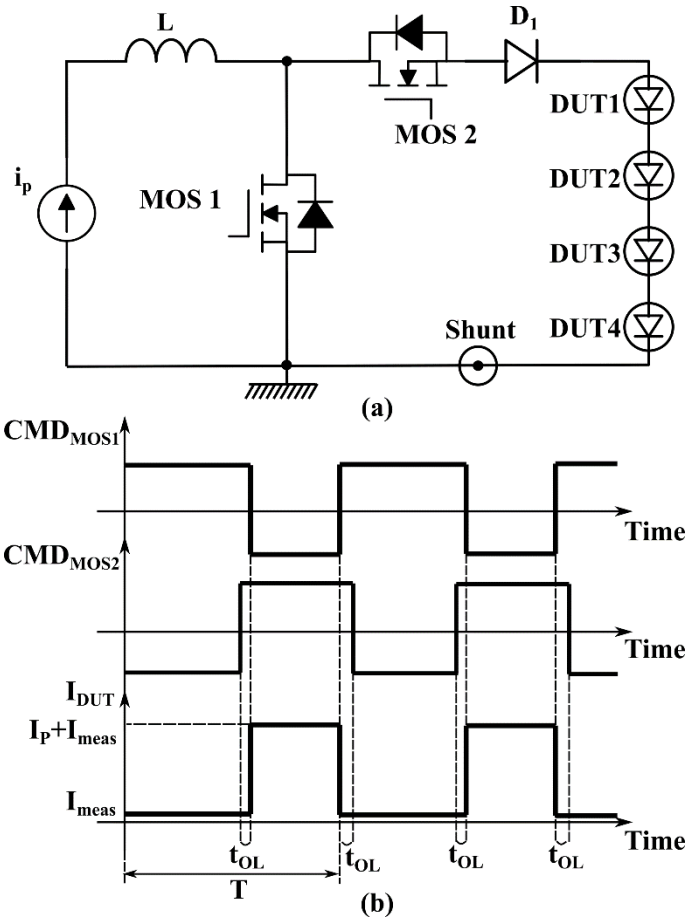


Fig. 3-6. High current generator. a) schematic, b) switching pattern.

For calculating case-junction thermal resistance (excluding TIM and plate thermal resistances), one can use equation (3-1) where P_{DUT} is the power loss in the considered DUT and equals to $V_{DUT}\times(I_P+I_{meas})$. The junction temperature was estimated using the TSEP presented earlier. The process of the failure indicators' extraction is shown in Fig. 3-7. For measuring on-state voltage of power IGBT/diode, the ① area was picked up. On-state voltage increases by an increase in junction temperature. By device aging (increases of R_{th} and V_{DUT}), the power loss in device increases leading to an increase in junction temperature. Therefore, this measurement had to be performed as close as possible to the switching transition to avoid self-heating aging effect on the voltage. Maximum junction temperatures of devices were also estimated through TSEP by on-state voltage measuring at low bias current as shown in ② area. The reference temperature (case temperature) was estimated through TSEP by on-state voltage measuring at low bias current as shown in ③ area. Some conditions had to be met to augment the accuracy of measurement and interested readers are referred to [224].

Fig. 3-8 shows the sample waveform of $V_{ce,on}$ in the measurement period (area ②). Regarding the impedance change and noises during data acquisition at the beginning of the measuring time and for having an accurate result, an interpolation of $V_{ce,on}$ was defined as a function of polynomial root square of time [224]. Then an extrapolation has been used to extract the voltage value at t_{meas}. In this case by using the TSEP, one could find that junction temperature of IGBT was 170°C. Accordingly, thermal resistance of the circuit would be obtained.

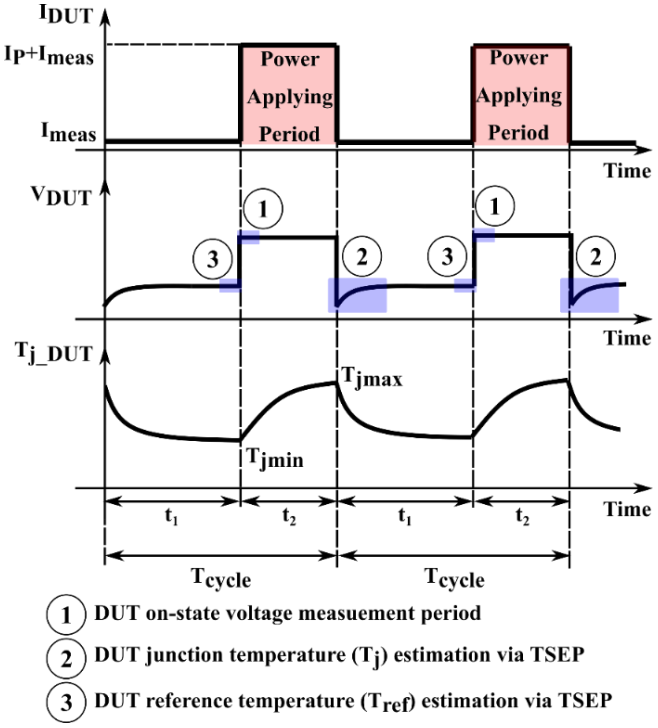


Fig. 3-7. Aging monitoring process.

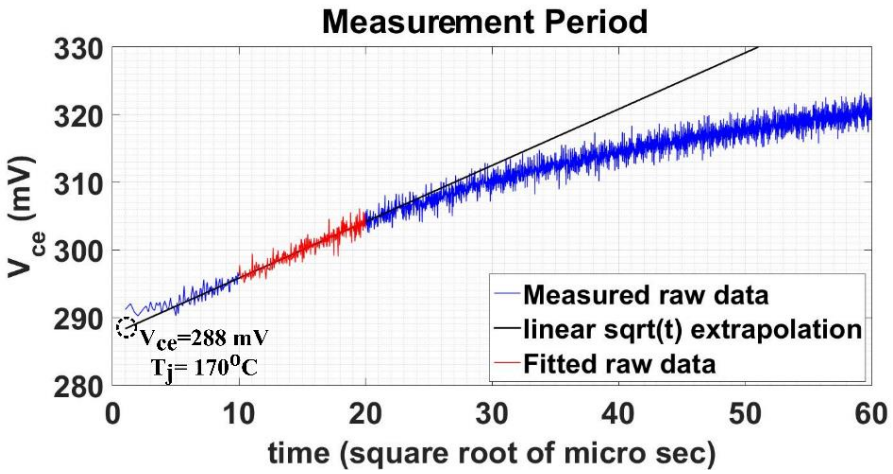


Fig. 3-8. Collector-emitter Voltage during measuring period measured by 6-channel data acquisition (HBM-Gen^{3i})

APC tests were performed for various mean temperatures and temperature swings for both IGBTs and power diodes. 130, 110, 90 and 70^{o}C temperature swings for mean temperature of 105^{o}C, and 110, 90, 70 and 50^{o}C for mean temperature of 95^{o}C were the different conditions of APC tests for preparing number of cycle to failure lifetime model.

3-2-2 Results and discussion

Based on the above-mentioned procedure, 64 power cycling tests performed; 32 tests for IGBT and 32 tests for diodes. Table 3-1 and Table 3-2 list the results of power cycling accelerated tests. The results are also shown in Fig. 3-9. Time of the current injecting (t_2) was adjusted based on some practical trials and errors for each test (see Fig. 3-7). It was also true for the cooling down time (t_1) that is much longer to be sure about the thermal stabilization. For example, it was about 22 sec and 8 sec for t_1 and t_2 respectively (for A1). Of course, these times had been manually adjusted periodically for compensating the degradation effects and kept test conditions almost constant. In these power cycling tests, both junction to case thermal resistance (global thermal resistance excluding TIM and plate thermal resistances) and on-state voltage (both as failure indicators) had been evaluated through the TSEP and direct measurements at the rated current, respectively. It has to be mentioned that during these tests, junction to case thermal resistance exceeded the failure criterion (20% increase). However, on-state voltage did not exceed its failure criterion (20% increase) and averagely reached 103% of nominal voltage. It stands to reason that by solder degradation (coalesced voids and cracks), the effective volume of solder decreased significantly leading to an increase in the junction to case thermal resistance and electrical resistance of solder interface. Since, the electrical resistance of bonding wire connection is higher than the solder electrical resistance, this increase could not significantly affect the on-state voltage.

Table 3-1. IGBT cycles to failure for power cycling accelerated tests

Test code	Temperature swing (°C)	T_{mean} (°C)	ΔT (°C)	Mean number of Cycles to Failure
A1	**40-170**	**105**	**130**	**6853**
A2	**50-160**		**110**	**8303**
A3	**60-150**		**90**	**10212**
A4	**70-140**		**70**	**13820**
B1	**40-150**	**95**	**110**	**9825**
B2	**50-140**		**90**	**12233**
B3	**60-130**		**70**	**16102**
B4	**70-120**		**50**	**NA**

Table 3-2. Diode cycles to failure for power cycling accelerated tests

Test code	Temperature swing (°C)	T_{mean} (°C)	ΔT (°C)	Mean number of Cycles to Failure
C1	**40-170**	**105**	**130**	**6266**
C2	**50-160**		**110**	**7603**
C3	**60-150**		**90**	**9625**
C4	**70-140**		**70**	**12006**
D1	**40-150**	**95**	**110**	**9051**
D2	**50-140**		**90**	**11208**
D3	**60-130**		**70**	**14864**
D4	**70-120**		**50**	**NA**

Regarding Table 3-1, Table 3-2 and Fig. 3-9, the higher mean temperature and temperature swing, the lower number of cycles to failure. For instance, A1 can tolerate 6853 cycles with the mean temperature of 105°C and the temperature swing of 130°C, while B3 can tolerate about 16102 cycles with the mean temperature of 95°C and the temperature swing of 70°C. It is worthy to mention that for each condition, four different IGBTs/diodes had been under the test. B4 and D4 were not accessible (NA) and achieved owing to the low temperature swing during the test.

In this study, the well accepted law, namely Arrhenius-Coffin-Manson, has been employed as explained in equation (1-9). This law demonstrates the number of cycles to the failure occurrence in specified mean temperature and temperature swing. Arrhenius-Coffin-Manson's lifetime model expresses the number of cycles before the failure in terms of the mean temperature and the amplitude of junction temperature as:

$$N_f(T_m, \Delta T_j) = A \times \Delta T_j^{\alpha} \times \exp(Q/RT_m) \tag{3-3}$$

where A and α are both constant and device-dependent, R and Q are the gas constant (8.314 $JMol^{-1}.K^{-1}$), internal energy and T_m is the mean junction temperature of devices in Kelvin. ΔT_j expresses the junction temperature swing of devices in °C.

Based on the experiments' results listed in Table 3-1 and Table 3-2 and using the least square curve fitting to that of (3-3), one can find that $\alpha=-1.117$, $A=4.352\times10^{3}$ and $Q=1.8523\times10^{4}$ for IGBT and $\alpha=-1.128$, $A=4.093\times10^{3}$ and $Q=1.8604\times10^{4}$ for diodes.

As previously mentioned, die attach degradation is illustrated by crack growth and void coalescence in the solder joint. Elasto-visco-plastic strain in the solder joint owing to the fatigue failure mechanism is the main factor in the die attach deterioration. Since Coffin-Manson-Arrhenius lifetime model has been widely employed for lifetime estimation, thermal resistance degradation process may be expressed as follow:

$$\Delta R_{th} = K\left\{\exp\left(\frac{N}{A\times\Delta T_j^{\alpha}\times\exp\left(Q/RT_m\right)}\right)-1\right\} \tag{3-4}$$

The parameters have been introduced in equation (3-3). N is the number of cycles applied to the power semiconductors and K is the material dependent coefficient and extracted using curve-fitting. It is 0.155 for IGBT and 0.232 for diode. The deterioration trend of thermal resistance, in the two mostly applied power

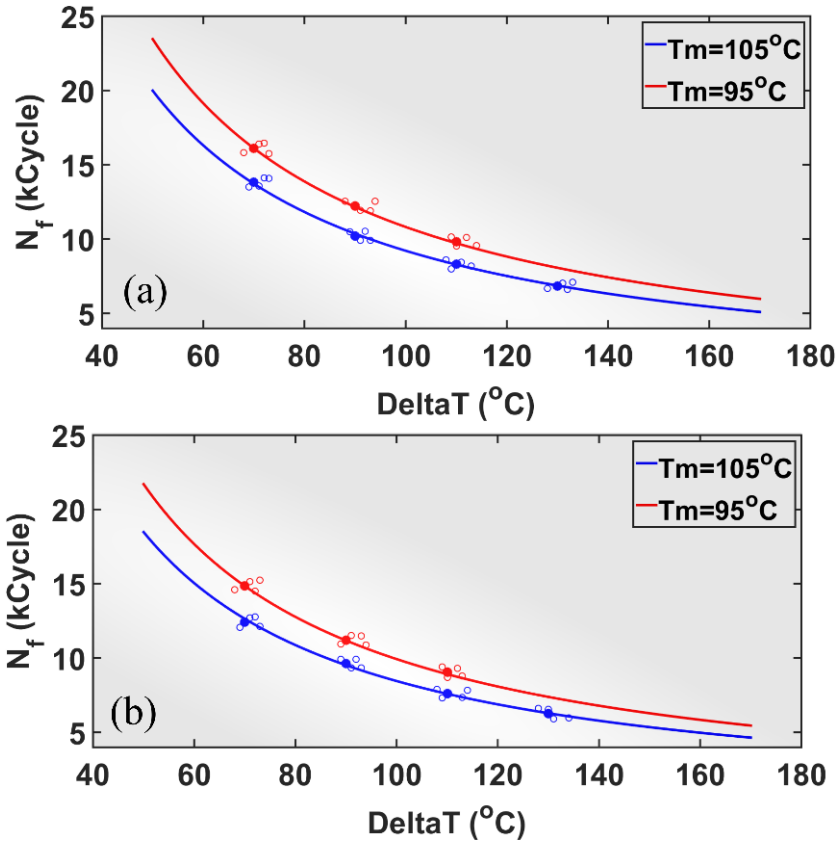


Fig. 3-9. Number of cycles to failure of a) IGBT and b) diode exposed to APC.

semiconductors i.e. IGBT and diode, is shown in Fig. 3-10. This figure demonstrates the deterioration trends of thermal resistance of power diode and IGBT in terms of thermal cycles. These results show a logarithmic trend expressing accelerated aging of IGBT and diode.

3-3 Accelerated thermal cycling tests (ATC)

3-3-1 Experimental Procedure

In this test, an automatic chamber was employed for performing accelerated thermal cycling tests. This test setup was designed for preparing aged IGBT and diode samples for different cases in order to investigate the self and mutual effects (Section 3-5) and activating creep failure mechanism and investigating its effects on the devices' aging.

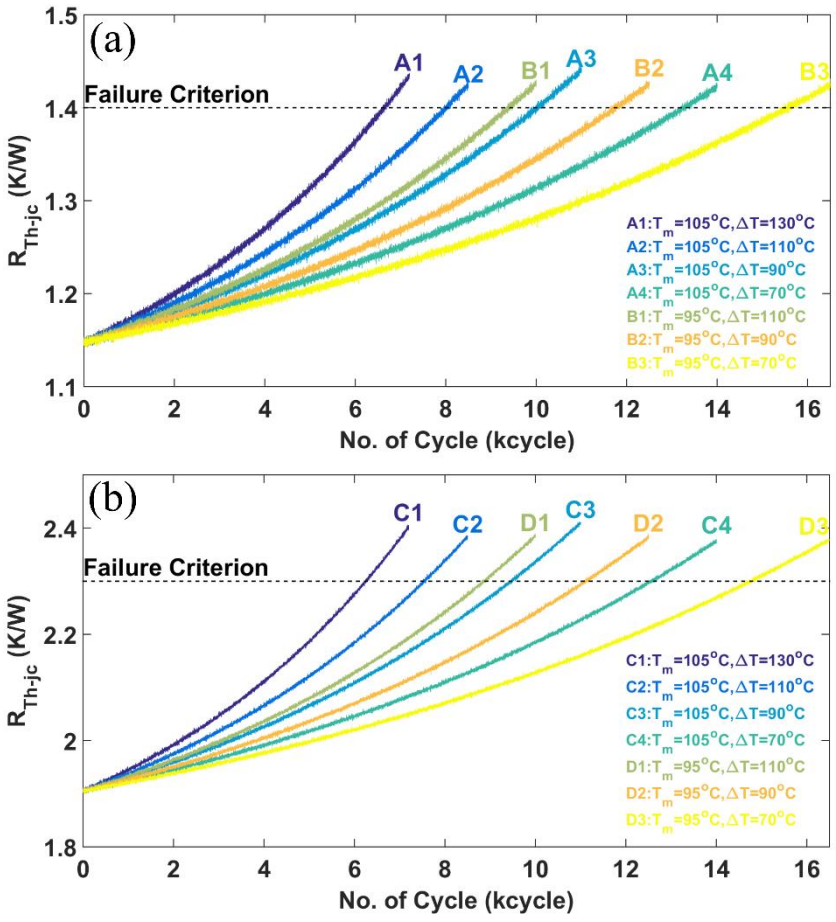


Fig. 3-10. Deterioration trends of power semiconductors against various thermal cycles. a) IGBT, b) diode.

Thermal cycling test was based on JESD22-A105C standard [231] and performed for several months and 2500 cycles (-40°C to 170°C) in a programmable chamber, namely, WTL 34/70 chamber. The aging test was stopped after reaching the failure criteria for both IGBTs and diodes, namely junction to case thermal resistance and

on-state collector-emitter voltage. While the voltages of new IGBT and new diodes at the nominal current were 1.51V and 1.43V respectively, IGBT collector-emitter and diode forward voltages reached 1.81V and 1.72V respectively when they had been aged. Junction-case thermal resistances reached 1.4 and 2.3 ^{o}C/W for IGBT and diode respectively (they were 1.15 and 1.9^{o}C/W with new devices, respectively).

The details of parameters for thermal cycle loadings are illustrated in Fig. 3-11. Roughly every ten cycles, IGBTs and diodes were put out of programmable chamber and were under the test individually by measuring two parameters, namely junction to case thermal resistance and on-state voltage. The test equipment is shown in Fig. 3-5. This test bench was prepared for estimating thermal resistance of IGBT and diode. 15A power current was injected to the diode or IGBT for 100 ms

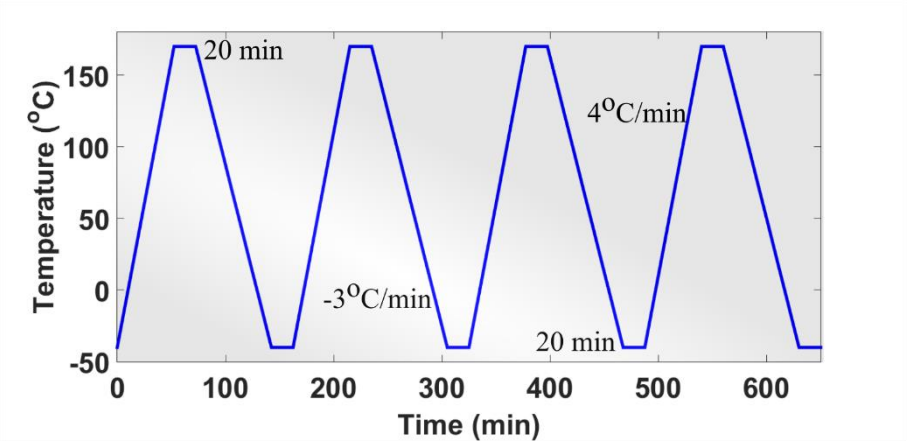


Fig. 3-11. Thermal cycling profile

(to assure approaching to maximum junction temperature) and then rested for several seconds to be stabilized. The procedure of thermal resistance estimation has been expressed in section 3-2-1.

3-3-2 Results and discussion

Parameters drifting (due to the degradation) playing a major role in the failure definition. On-state voltage drop (V_{on}) and thermal resistance (R_{th}) are common parameters drifting in the power semiconductors and can affect device performance significantly during its aging.

As previously mentioned, die attach degradation is illustrated by cracks growth and voids coalescence in the solder joint. Elasto-visco-plasticitic and creep strain in the solder joint owing to the creep failure mechanism is one the main factors in the die attach deterioration. The average deterioration trends of thermal resistance and on-state voltage drop in the power semiconductors is shown in Fig. 3-12. This figure demonstrates the deterioration trends of thermal resistance and on state voltage drop of the discrete power semiconductors in terms of thermal cycles. These results

show a logarithmic trend expressing accelerated aging of power semiconductors. FEM simulation, had been also performed for demonstrating the creep failure mechanism effects on the solder joint in the power semiconductors. One can find more information and results in Appendix B.

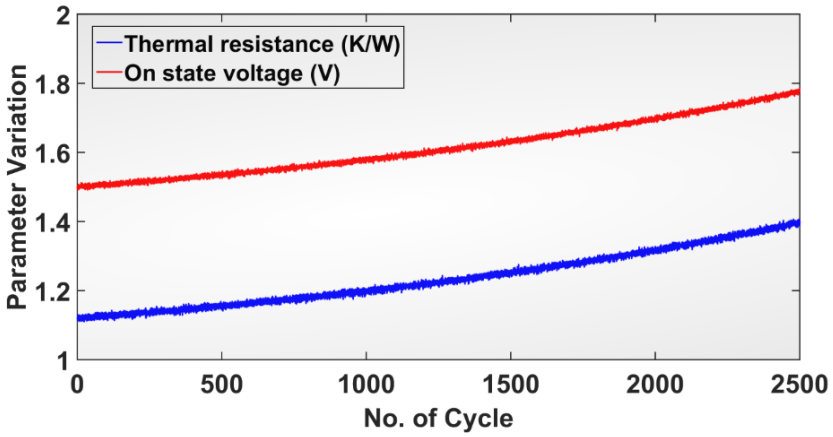


Fig. 3-12. Parameters drifting during aging.

3-4 Creep test

In this work, creep test was performed to attain the solder constants for Garofalo equation (equation (1-5)). Solder specimen (Sn-3.5Ag-0.5Cu) is illustrated in Fig. 3-13. Solder tensile specimen was designed based on the standard guidelines described in [232]. Regarding this figure, a uniform uniaxial stress in the declined radius gauge section was obtained. The dimensions are also illustrated in Fig. 3-13. Tensile tests at the constant strain rate test conditions can be used to characterize the creep steady strain rate data at high stress levels. Constant strain rate tensile tests were reported by [232]. Four temperatures including 0°C, 25°C, 75°C and 125°C under four different stresses were carried out. In 0°C, the loaded stresses were 15, 45, 60 and 75MPa and by temperature increasing, each of them decreased by 2.5MPa. In the following equation, the hyperbolic sine law for the steady-state creep rate includes both low and high stresses creep. The coefficients in the equation were achieved through fitting of experimental data. The mentioned equation adapts with the steady-state creep stage including an activation energy (Q).

$$\dot{\varepsilon}_{cr} = A_1\left[\sin(\alpha\sigma)\right]^n \exp\left(\frac{-Q}{kT}\right) = C_1\left[\sin(C_2\sigma)\right]^{C_3} \exp\left(\frac{-C_4}{T}\right) \qquad (3\text{-}5)$$

The collected data from the different temperatures could be plotted as log ε_{min} and log sinh $\alpha\sigma$ and consequently, the four steady-state creep coefficients (Cx) were measured for Sn-3.5Ag-0.5Cu. At each step, a set of best fits (α, A, n, Q) was taken using Matlab™ Statistics Toolbox™. Regarding the results one can easily find the creep constant coefficients as 2.73×10^5 (1/s), 0.023 $(MPa)^{-1}$, 6.3 and 6480.3 for C_1, C_2, C_3 and C_4, respectively.

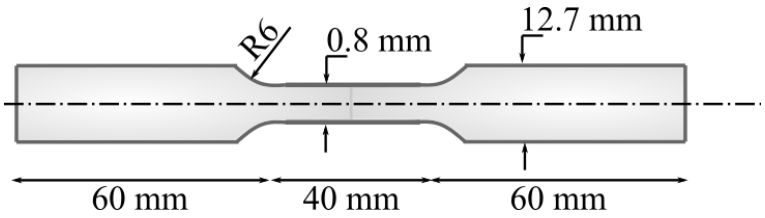


Fig. 3-13. Geometry of creep specimen.

3-5 Modified DC-DC boost converter

Since thermal and electrical operating points (TOPs and EOPs) of the converters are strongly correlated to the status of power components (see Fig. 3-14), considering the effects of self and mutual degradations in reliability assessment of the converters seems to be necessary. In this figure, the devices of a conventional boost converter are considered. Their related waveforms and temperatures can be estimated by using electrical, loss and thermal models. These models are fed by electrical and thermal parameters and by working conditions of the converter. The waveforms and temperatures can then be used to estimate the ageing status of every device. However, the aging of one device will induce a deviation of its electrical and/or thermal parameters. Thus, due to the electrical and thermal coupling in the converter, the deviation of one electrical or one thermal parameter of one device will be able to affect the waveforms and temperatures of the others which, in turn, will impact their own aging status.

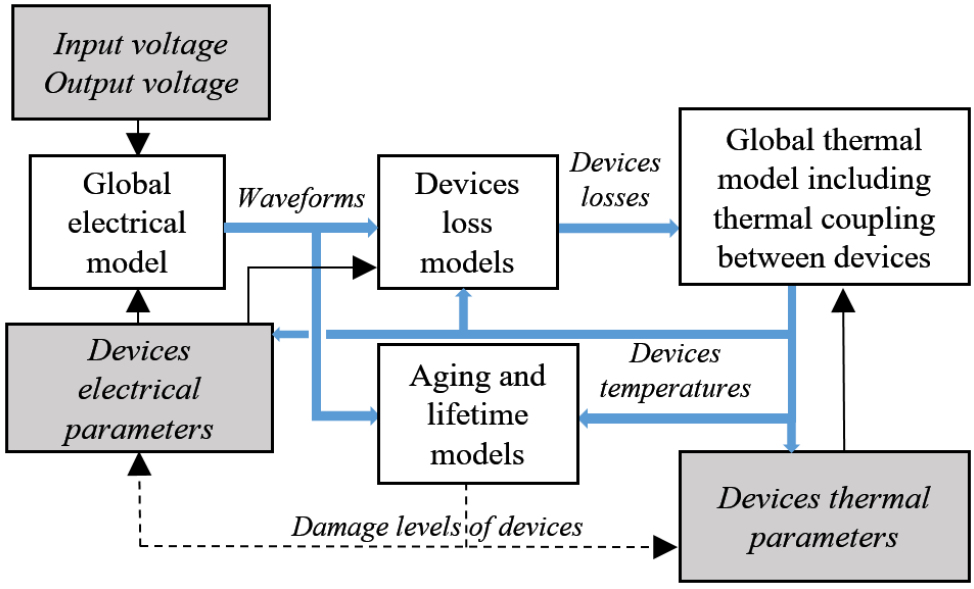


Fig. 3-14. Thermal and Electrical reliability correlations in a converter.

It was expressed that in a converter the degradations of power components lead to the TOP and EOP changes. Accordingly, degradation of one device can have effect on the thermal and/or electrical performance of other devices. It means that not only does the degradation of one device accelerate its aging, but also it accelerates other

devices' aging. In this study, for demonstrating the effects of degradations of the devices on EOP and TOP, a conventional 200/400V and 3000W DC-DC boost converter was considered as a case study (see also Table 2-2 for detailed specifications).

Fig. 3-15 demonstrates a DC-DC boost converter with additional devices. This conventional DC-DC boost converter was designed in such a way to monitor junction temperature of power semiconductors in the real time for proving and evaluating TOP changes during aging. Fig. 3-15a shows the schematic of this converter. As it can be seen from this figure, two auxiliary power switches and two low power switches were included. There were also two low current sources (22.5 mA) for thermo-sensitive electrical parameter (TSEP) measurement. Fig. 3-15b depicts switching pattern of this customized DC-DC boost converter. The converter was working under normal condition for a period of time (20~30 min) to be thermally stabilized. Then, for 1 msec S_2 and S_1 turn off and S_3 turns on. For avoiding voltage spike, this switching transition occurs with 5 μs overlap. At this time, two low bias currents (I_{meas}) are injected to IGBT and power diode through S_4 and S_5, respectively. Then, collector-emitter and diode forward voltages have been measured by a data logger. During normal working, data logger sees a very large voltage (off state voltages of IGBT and power diode). That is why an active voltage clamp circuit has been used. Then with a look up table (collector emitter and diode forward voltage as functions of their junction temperatures at 22.5 mA), junction temperatures of IGBT and power diode have been estimated.

For expressing the mutual effects of the degradations of devices on each other, five different cases have been designed as follows. These cases are based on this knowledge that the critical components are capacitors and power semiconductors (IGBT and diode) [93], [136], [233], [234].

Case I, in this case all the devices including IGBT and diode are new and have their own nominal parameters.

Case II, in this case (aged case) all the devices including IGBT and diode have been degraded and reached their failure criterion. The failure criterion have been defined by 20% increase in both junction-case thermal resistance and collector-emitter/forward voltage in IGBT/diode [235], [236]. Based on this definition of the failure criterion, after complete aging of IGBT and diode, the junction temperatures of IGBT and diode have been reached their maximum allowable temperatures, namely 170^{o}C.

Case III, in this case IGBT has been electrically and thermally degraded while all other components have remained unchanged. It is assumed that junction to case thermal resistance of IGBT increases by 20% and its collector-emitter voltage increases by 20%.

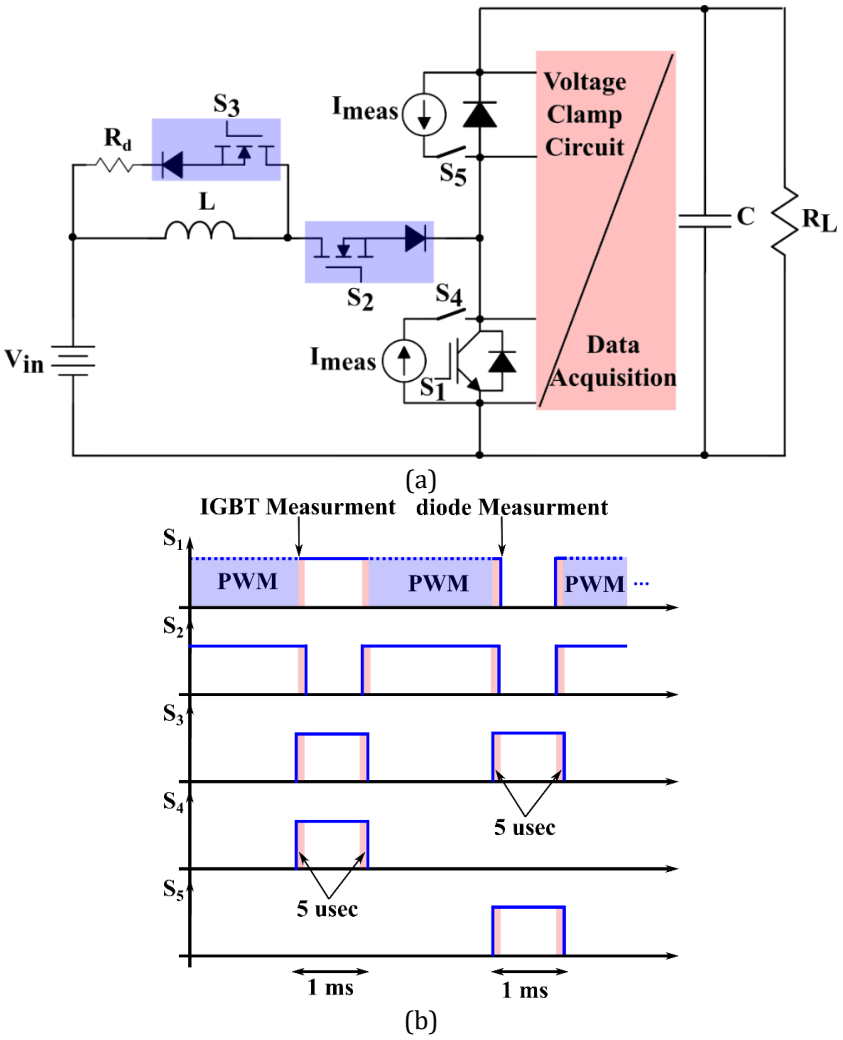


Fig. 3-15. Conventional DC-DC boost converter equipped with auxiliary circuits. a) Schematic, b) switching pattern

Case IV, in this case the diode has been electrically and thermally degraded while all other components have remained unchanged. It assumes that junction to case thermal resistance of diode increases by 20% and its forward voltage increases by 20%.

Case V, in this case output capacitor has been degraded while all the other components have been unchanged [93], [118].

In the abovementioned cases, parameters' deviations are based on the failure criteria. These deviations are completely different from one application to another and have been extracted from literature [235]–[237].

Fig. 3-16 illustrates the test bench of the customized DC-DC boost converter. The main power supply was used for preparing 3000 W power transfer to the pure resistance load. A data logger with the brand of HBM-Gen^{3i} was employed for recording on-state voltage of IGBT and diode. During measuring time (1ms), a low

bias constant current (22.5 mA) was injected to IGBT or diode alternatively for evaluating on-state voltage and then calculating junction temperature using TSEP as described in the previous section. Fig. 3-17 shows the main switching cell of the considered DC-DC boost converter. Main IGBT and power diode both are mounted on a common heat sink as shown in Fig. 2-17. S2 switch including a MOSFET and power diode as well were both mounted on the other heat sink. Five 10uF capacitors were employed in parallel located in series with four high power resistor playing the role of ESR.

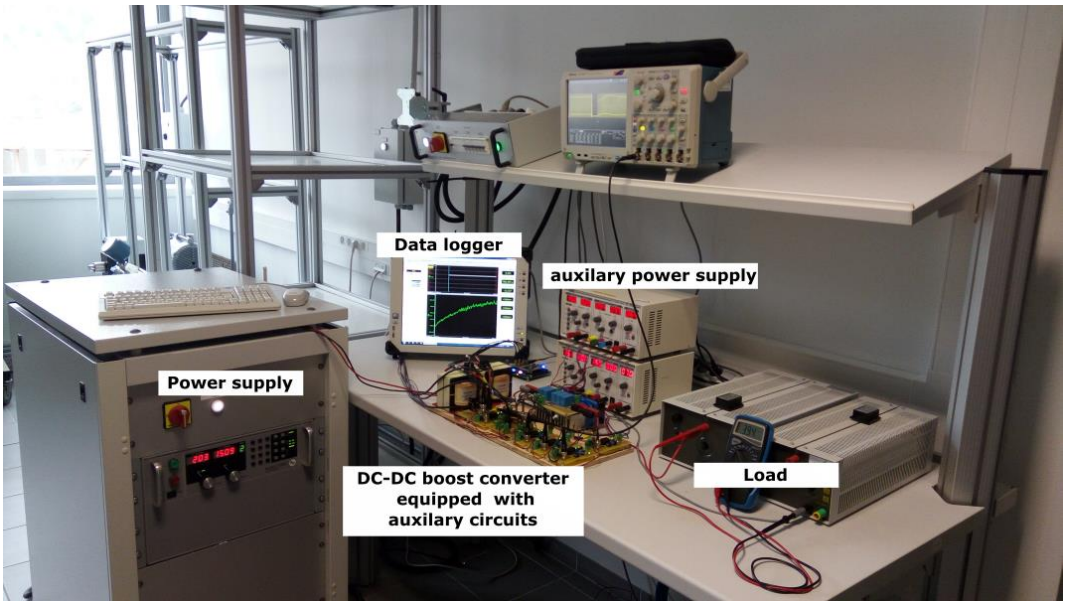


Fig. 3-16 Test bench of customized DC-DC boost converter

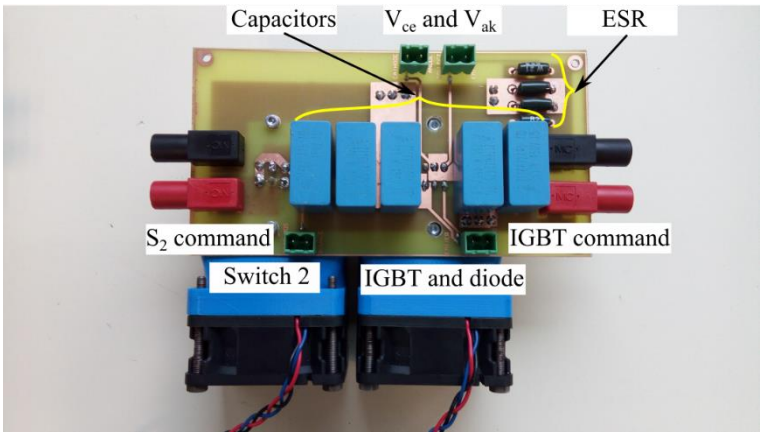


Fig. 3-17. Main switching cell of the considered DC-DC boost converter

Command signals for the switches were performed by Altera Cyclone IV-e FPGA DE0-Nano and transferred to the switches by using individual gate drivers as shown in Fig. 3-18. As it was mentioned, there was a need for clamping high voltages IGBT and diode during their normal working to avoid making data logger saturated. Also, a low bias current source had been designed for measuring period. A schematic of

active clamping circuit and low bias current circuit is shown in Fig. 3-19a and b. These circuits were based on the circuits proposed in [165]. Active clamping circuit was working with the fast dynamic response and low power consumptions. Low bias current circuit was working very fast and after activation, the low bias current worked without any impressive transients leading to accurate voltage measurements. For higher accuracy, one hundred tests for each of IGBT and power diode junction temperatures measurement have been performed during this study. Five sets of 20 tests were considered for IGBT and power diode. After every thermal stabilization, 20 measurements were done for both IGBT and diode. This procedure was repeated for 5 times. Finally, the junction temperatures of IGBT and diode were estimated by averaging this 100 measurements.

Power semiconductors' junction temperatures play a major role in converters' useful lifetime. Therefore, for having a quantitative comparison, junction temperatures of IGBT and diode have been listed in Table 3-3 for the different cases (case I to case V presented earlier). In each case, the devices had been changed based on their corresponding status. For example, in Case II, both IGBT and diode were replaced by the aged ones (the aged IGBT and diode were taken from ATC test). One can find detailed information about this experiment in [227]. Regarding Table. 3-3, one can verify that degradations of IGBT and/or diode can significantly affect their junction temperatures. For example, in case II in which all the critical components have been degraded, IGBT's and diode's junction temperatures increased by 30.2^{o}C and 25.6^{o}C, respectively. In case III (aged IGBT), diode's junction temperature increased by 7.2^{o}C. It means that IGBT aging can directly affect the junction temperature of the power diode leading to more accelerated power diode degradation.

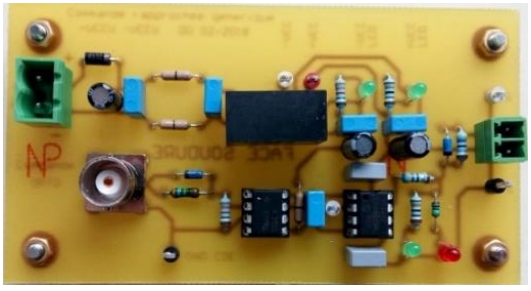


Fig. 3-18. Gate driver circuit.

On the other hand, in case IV, IGBT's junction temperature increased by 4.8^{o}C. It means that power diode aging can directly affect the junction temperature of the IGBT leading to more accelerated IGBT degradation. However, capacitor aging cannot significantly affect junction temperatures of IGBT and diode. These facts confirm that degradation of either IGBT or diode have significant mutual- and self-aging effects on them. Therefore, these effects have to be considered in t reliability assessment of power converters as proposed in this manuscript.

Table 3-3. Junction temperature of IGBT and diode

State	T_j^{IGBT} (°C)	T_j^{Diode} (°C)
Case I	**140.3**	**122.6**
Case II	**170.5**	**148.2**
Case III	**165.6**	**129.8**
Case IV	**145.1**	**141.9**
Case V	**140.8**	**123.3**

3-6 SEM and 3D X-ray Tomography

For evaluating the material properties of IGBTs and diodes after ATC and APC, Scanning electron microscope (SEM) and X-ray Tomography were employed. SEM microscope with the brand of Thermo Fisher was used. For 3D analysis, X-ray Tomography (Tomograph EASYTOMXL (CMTC) with Camera Princeton and X-ray tube Hamamatsu L10711) was employed in "*SIMAP groupe*".

Since Sn-Ag-Cu solder has a very high absorption, very small samples had to be prepared for 3D X-ray Tomography. The samples had been softly polished till they reached the 20µm thickness. The conditions were: Voltage : 100kV, Current : 15µA, Voxel size =0.75 µm leading to spatial true resolution = 1.5µm, Number of projection = 600 and exposure time = 4s.

Due to the stresses supervened during temperature swinging of power chips, some failure mechanisms such as fatigue and creep can occur and result to crack and void initiation and propagation. Solder layer of a new and an aged power semiconductor is depicted in Fig. 3-20. Fig. 3-20a shows the solder layer of a new power device. There are some initial process induced voids and cracks (generated during the manufacturing). Fig. 3-20b and 3-20c shows the aged power devices which were being under APC and ATC aging tests. One can find that how thermal loading can propagate the voids and cracks.

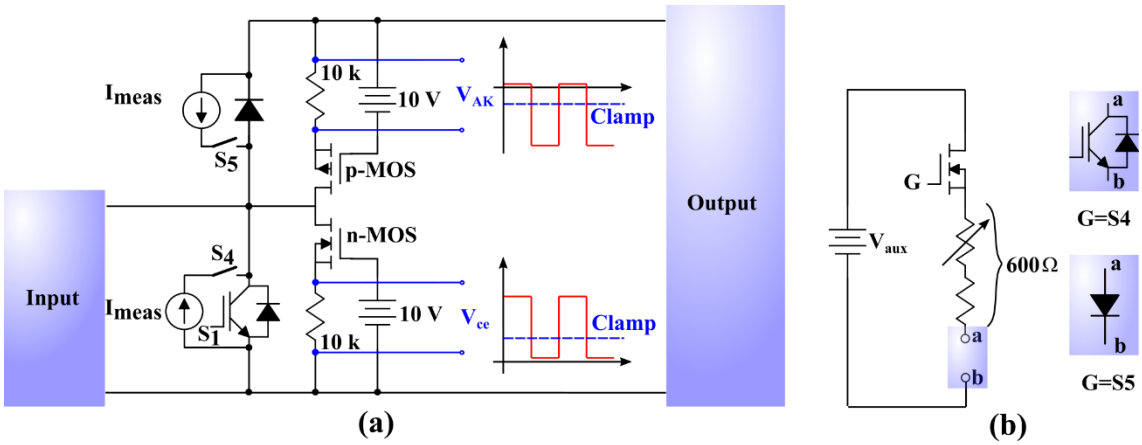


Fig. 3-19. Schematic circuit of a) voltage clamping circuit and b) low bias current source circuit.

Fig. 3-21 demonstrates a part of solder joint in a power device. Increase in voids volume of the solder joints can be obviously seen. The solder material tends to voids growth and coalescence during the aging evolution. This phenomenon is related to simultaneous effects of hydrostatic tension stresses and inelastic strains so that the micro-voids nucleate around the secondary phases and grow during the fatigue evolution. The void growth intensifies the strain domain among the neighbor voids and facilitate the coalescence and the micro-crack formation in the structure. Moreover, primary voids shapes and sizes and void-to-void interactions can complicate the damage mechanism and the reliability assessment in the solder joint. It stands to reason that by solder degradation (making voids and cracks), the volume of voids and cracks significantly increased leading to an increase in the junction to case thermal resistance.

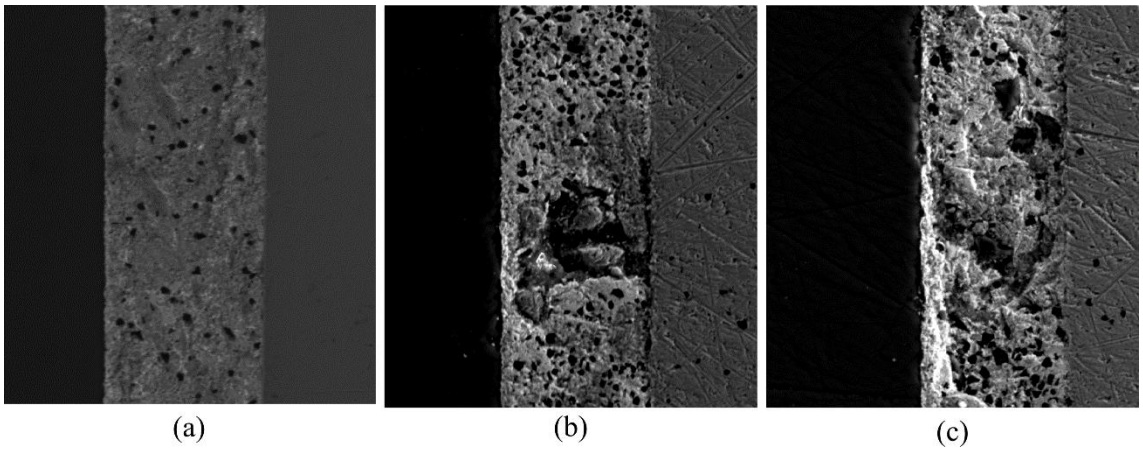


Fig. 3-20. SEM microscopic image of solder joint, a) new device, b) aged device under APC test, c) aged device under ATC test.

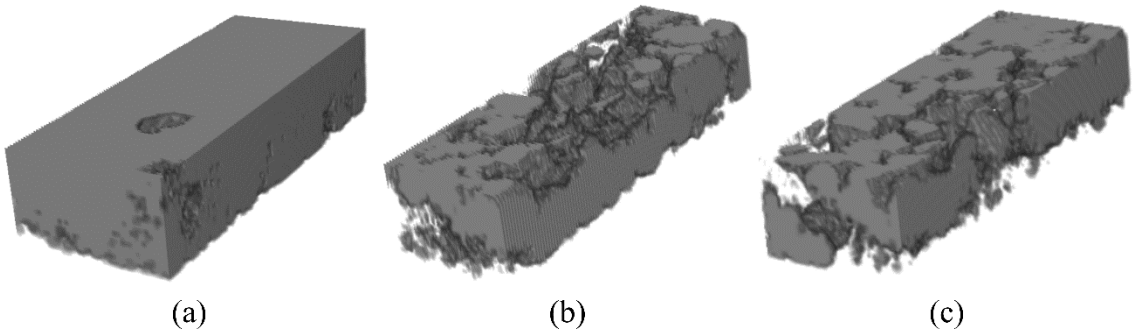


Fig. 3-21. 3D X-ray tomography of solder joint, a) new device, b) aged device under APC test, c) aged device under ATC test.

3-7 Conclusion

The main objectives of this chapter falls into three categories; first of all, we demonstrated the importance of mutual and self-degradations of power semiconductors on the electrical and thermal performances of the power converter implementing a customized conventional DC-DC boost converter capable of on-line

junction temperature estimation. For this reason, five different cases were defined for evaluating these effects. The results showed that either IGBT or diode degradations affected thermal operating points of the considered power converter. IGBT and diode degradations finally led to roughly 22% and 21% variations in IGBT and diode junction temperatures, respectively. Therefore, it revealed that semiconductors' degradations have to be considered in reliability evaluation of the power converter. However, power capacitor degradation did not have significant effects on electrical and thermal performances of the considered power converter. Secondly, the effects of the potential failure mechanisms, namely electro-thermo-mechanical fatigue and creep, had been observed trough APC and ATC tests, respectively. SEM and 3D X-ray Tomography images of solder layer as the vulnerable part in the power semiconductors showed that the potential failure mechanisms could thoroughly affect the performance of power semiconductors. Thirdly, for obtaining constant coefficients of Arrhenius-Coffin-Manson and Monkman-Grant lifetime and damage models, APC and creep tests were performed. These results will play an important role in our proposed useful lifetime estimation.

4

Rainflow algorithm

4-1 Introduction

Counting of complicated loading cycles applied to any physical systems is increasingly becoming a vital factor in the life time estimation, particularly in the thermo-mechanical fatigue study. Cycle counting algorithms are attracting considerable interest due to their capability of compacting a long time history data to the somewhat sorted data expediting the analysis of the fatigue useful lifetime [238], [239].

For many years, numerous cycle counting algorithms including peak counting, crossing counting, level counting, simple rate counting, Hayes method, racetrack method, simple range counting, Moshrefifar and Azamfar method and Rainflow counting method have been applied in the various applications [240], [241]. In real applications, loading cycles are not in a simple pattern to be counted. Moreover, they do comprise a long-term data which is highly involved to be either analyzed or compared. Fig. 4-1 depicts two sets of data (temperature), applied to a system. Regarding this figure, it is roughly impossible to analyze how these two stresses can affect the lifetime of the system. As a reliability point of view, it is also impossible to compare these two stress patterns. However, thanks to the cycle-counting algorithm, analyzing and comparing long and complicated stresses has become possible.

The primary algorithm was established by T. Endo and M. Matsuishi in 1968 [242] based on a rain drop over a Pagoda roof as shown in Fig. 4-2. Each of the closed hysteresis loop is considered as one load cycle with the specified strain (stress) range and its corresponding mean value. For instance, after applying a specific stress to the material, it starts tensioning (from point ①) leading to the material deformation. This tension continues to point ② in which a new stress makes the material compress to point ③. Then it starts being tensioned and therefore passes point ② leading to form a stress-strain hysteresis loop (③-②) with the strain (stress) range of $|S_{③}-S_{②}|$ and mean value of $(S_{③}+S_{②})/2$. This deformation continues to point ④ and after that a compression stress makes the material strain

decrease to point ⑤. Then a positive stress applies and a positive strain occurs (⑥). After that by compressing the material, a material deformation occurs and by passing through point ⑤ another stress-strain hysteresis loop is formed (with the range of $|S_{⑥}-S_{⑤}|$ and mean value of $(S_{⑥}+S_{⑤})/2$). The process will be continued till all the data has been analyzed.

As it was mentioned, there are numerous cycle-counting algorithms [240]. Among all of them, Rainflow algorithm has gained lots of attractions owing to its simplicity of implementation and insignificant errors [243], [244]. As the procedure of algorithm performing point of view, Rainflow algorithm generally falls into two categories, namely, three-point and four-point [245]. Although C.H. McInnes and P.A. Meehan [246] have mathematically proved that the three-point and the four-point methods are both equal, the three-point algorithm gains much popularity among engineers [247]. Based on the ASTM E1049-85 standard [245], the three-point Rainflow algorithm coding was implemented by A. Nieslony [248] using MATLAB tools. Rainflow is based on the local maxima and minima of the time domain data history. It means that for applying Rainflow cycle counting algorithm (either in three-point or four-point cases) to the time domain data history, it primarily needs to be transferred to the local extrema.

Generally, major flaws of Rainflow algorithm are including as follows:

1- In the conventional Rainflow only the extrema (peaks and valleys) have been employed leading to lose the time data of signal.

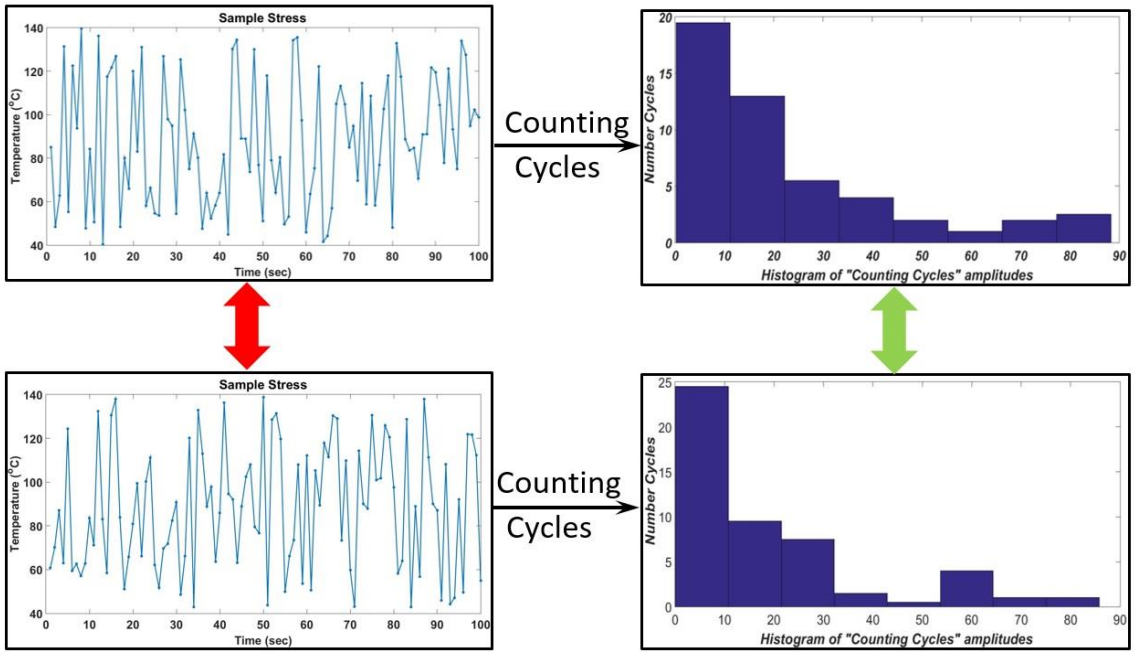


Fig. 4-1. Time domain data versus cycle-counting domain

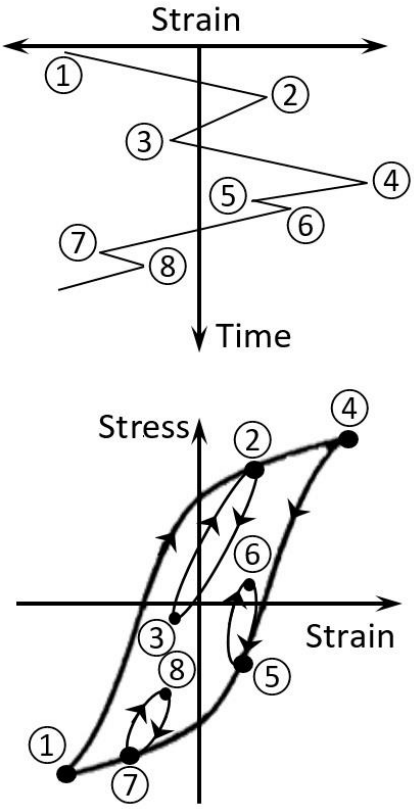


Fig.4-2. Time domain data and its corresponding stress-strain hysteresis loop

2- Based on the most widely-used thermo-mechanical fatigue failure model, namely Arrhenius-Coffin-Manson, mean temperature has paramount of importance in the acceptable confidence level fatigue lifetime evaluation [249]. In the previous Rainflow versions, the dependency of time on the mean temperature has been missed out.

3- A neglected area in the field of the Rainflow is the creep degradation. Creep mechanism plays a major role in the device/system degradation, particularly when the thermal stress ranges are sufficiently near to device melting temperature [146], [147]. Therefore, the current solutions to the Rainflow algorithms are inefficient in the precise lifetime estimation.

Based on the reviewed literature, these aforementioned drawbacks of Rainflow cycles counting have not been simultaneously mitigated yet. Although time-temperature-dependency of the mean temperature were addressed by L. R. GopiReddy [244], the other defects especially creep-included algorithm have remained.

This chapter formulates a new approach to the Rainflow cycle counting algorithm and seeks to address how to tackle above-mentioned defects. The aim of this chapter is to broaden the current four-point Rainflow algorithm capable of considering creep mechanism, time-temperature-dependency of mean temperature.

4-2 Importance of Creep Mechanism and Time-Temperature-Dependent Mean Temperature

In this section, the importance of time-temperature-dependent mean temperature and creep mechanism will be discussed. As a sample, Fig. 1-24a demonstrates stress-strain curve of a material. The trace falls into two elastic and plastic regions. Stress-strain behaviors of solder for different temperatures are also depicted in Fig. 1-24b [146]. As it can be seen from Fig. 1-24b, the material temperature has a significant effect on the strain occurring inside the material. Material strain is a key factor in the fatigue aging mechanism. Accordingly, in the same stresses, the created strain in the material varies significantly by the temperature variations. In such materials that the temperature varies during its loading, the importance of considering time-temperature-dependent mean temperature has become outstanding leading to the different useful lifetime estimations.

Creep mechanism is one of the most critical aging mechanisms in the materials in which their working temperatures are sufficiently high and are above the one third of their absolute melting temperatures[146]. In the most materials, a temperature increase leads to a decrease in strength of material. In the creep mechanism both the time and the temperature are paramount of importance due to its physical mechanism. Physically, creep degradation in the materials is owing to the propagation and nucleation of micro-cracks and their coalescence to meso-cracks [146], [147].

On the contrary to the low-cycle fatigue damage process, namely load cycles, creep degradation is time-dependent and highly impressed by the dwelling time period [148]. For expressing lifetime model of the materials on the creep failure mechanism, Monkman-Grant (MG) model has been extensively used. Creep lifetime and creep damage models have been extensively described in sections 1-2-3-7-2 and 1-2-3-8-2, respectively.

It was previously mentioned and also revealed from the equation (1-10) that the creep failure mechanism is time dependent which means that the longer time the material exposed to the roughly constant temperature, the more degradation occurs. Based on Monkman-Grant model, the dwelling time (Δt) is a key factor in calculating the creep useful lifetime. Previous works have only been limited to the high/low cycle fatigue by considering only the stress swings and the mean stresses and failed to purpose the dwelling times in which the material have been rested in the roughly constant temperature. Fig. 1-25 demonstrates a thermal stress as a function of time. As it is shown in the thermal stresses, there can be a lot of dwelling times in which the material is exposed to. Thus, it is thoroughly important to also consider the creep failure mechanism in cycle counting algorithm.

4-3 Time-Temperature-Dependent Creep-Fatigue Rainflow Counting Algorithm

As it was mentioned in the conventional Rainflow, only the extrema (peaks and valleys) have been employed. This leads to lose the time data of the signal. In addition, the dependency of the time on the mean temperature and creep degradation have been neglected. In this section, a novel efficient time-temperature-dependent creep-fatigue Rainflow counting algorithm will be proposed.

4-3-1 Time-temperature-dependent mean temperature evaluation

Fig. 4-3 demonstrates four thermal points in a specific thermal cycle which is constituting a full thermal cycle. T_1 to T_4 are the temperatures and t_1 to t_4 are their corresponded times (See also points ① to ④ in Fig. 4-2b). t_{FC} is the time at which the thermal cycle is completely formed. Based on the Rainflow algorithm, T_2 and T_3 formed a thermal full cycle. As previously mentioned, strain-stress curve of almost all materials are temperature dependent (see Fig. 1-24b). Therefore, one can find that the time between the thermal points at which full thermal cycles (local hysteresis loop) occur is undoubtedly important for the mean temperature evaluation.

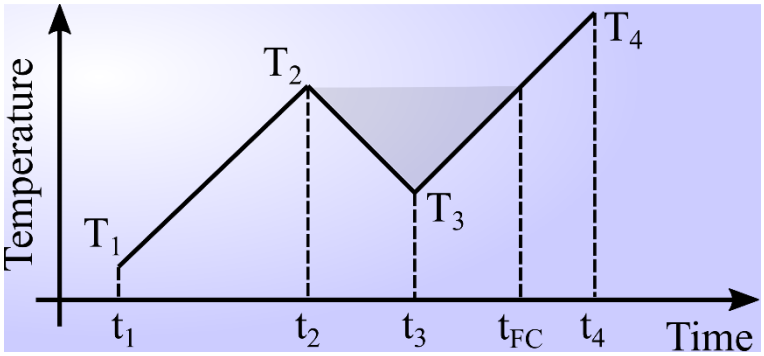


Fig. 4-3. Four-point thermal full cycle.

Without considering the time between the thermal points, mean temperature can be readily calculated by $(T_3+T_2)/2$. However, it is not acceptable for the materials in which their strain-stress curves are temperature dependent. In the other words, the time of the complete formation of the local hysteresis loop is thoroughly important in the mean temperature calculation (see Fig. 4-2b). Based on Fig. 4-3, the thermal cycle has been completed in t_{FC}. Therefore, a whole time of the full cycle is t_{FC}-t_2. The mean temperature between the points t_2-t_3 and t_3-t_4 are $(T_2+T_3)/2$ and $(T_3+T_4)/2$, respectively. The time-weighted mean temperature of this full cycle is the average

of these two mean temperatures in terms of their associated times. Accordingly, an equivalent mean temperature can be calculated as follows [244]:

$$T_{mean}^{e} = \frac{t_3 - t_2}{t_{FC} - t_2}\frac{(T_3 + T_2)}{2} + \frac{t_{FC} - t_3}{t_{FC} - t_2}\frac{(T_4 + T_3)}{2} \quad (4\text{-}1)$$

where T^{e}_{mean} is the new equivalent mean temperature and

$$t_{FC} = \frac{T_2 - T_3}{T_4 - T_3}(t_4 - t_3) + t_3 \quad (4\text{-}2)$$

It is clear that by increasing t_3-t_2, the equivalent mean temperature will be also increased which has to be taken into account in reliability assessment of the materials. Thus, in the proposed Rainflow algorithm this equivalent mean temperature will be employed to increase accuracy of reliability evaluation.

4-3-2 Developing of newly proposed time-temperature-dependent creep-fatigue Rainflow counting algorithm

To mitigate the previous mentioned problems, a newly introduced online counting cycle will be discussed in this section. In addition to considering the creep degradation and the time-temperature-dependent mean temperature, the proposed method is capable of counting half cycles at the exact times they occur. Input data including stresses (e.g. temperature) and their corresponding times should have been inserted to the proposed algorithm as a real time vectors. There are two flexible buffers being in charge of temporarily memorizing of maxima and minima, respectively. In addition, there are also three pointers for specifying the maxima and minima precession/inferiority, size of two flexible buffers.

Fig. 4-4 depicts schematic block diagram of proposed algorithm. The key algorithm is based on the four-point Rainflow method but applying some new features to address the above-mentioned challenges. **T** is the input temperature vector which is updated online by inserting new data to the algorithm. **t** is the corresponding time vector which is also simultaneously updated. These two vectors are considered as the input data at the top of the algorithm in Fig. 4-4. $\mathbf{S_{min}}$ and $\mathbf{S_{max}}$ are defined as flexible buffers allocated for minima and maxima, respectively. P_{min} and P_{max} are the pointers indicating the length of $\mathbf{S_{min}}$ and $\mathbf{S_{max}}$, respectively. These two pointers make the algorithm be simply implemented. j is also an indicator which shows whether or not local maximum or minimum is coming. If j=1, local minimum will be coming and if j=0, maximum will be coming as a next input data. H is creep hysteresis band.

Once, input data inserted the algorithm will be started. The first step is to check that enough inputs have been coming or not. In this case, because the algorithm is based on the four-point method, at least four inputs are needed. However, for the local

extremum checking, there is another need to have the fifth inputs to judge whether or not the fourth point is the extremum. Accordingly, the size of **T** as an input data has to be 5 at any time to make it possible to run the algorithm. The auxiliary variable k is in charge of validating the number of enough inputs for the creep and extremum checks.

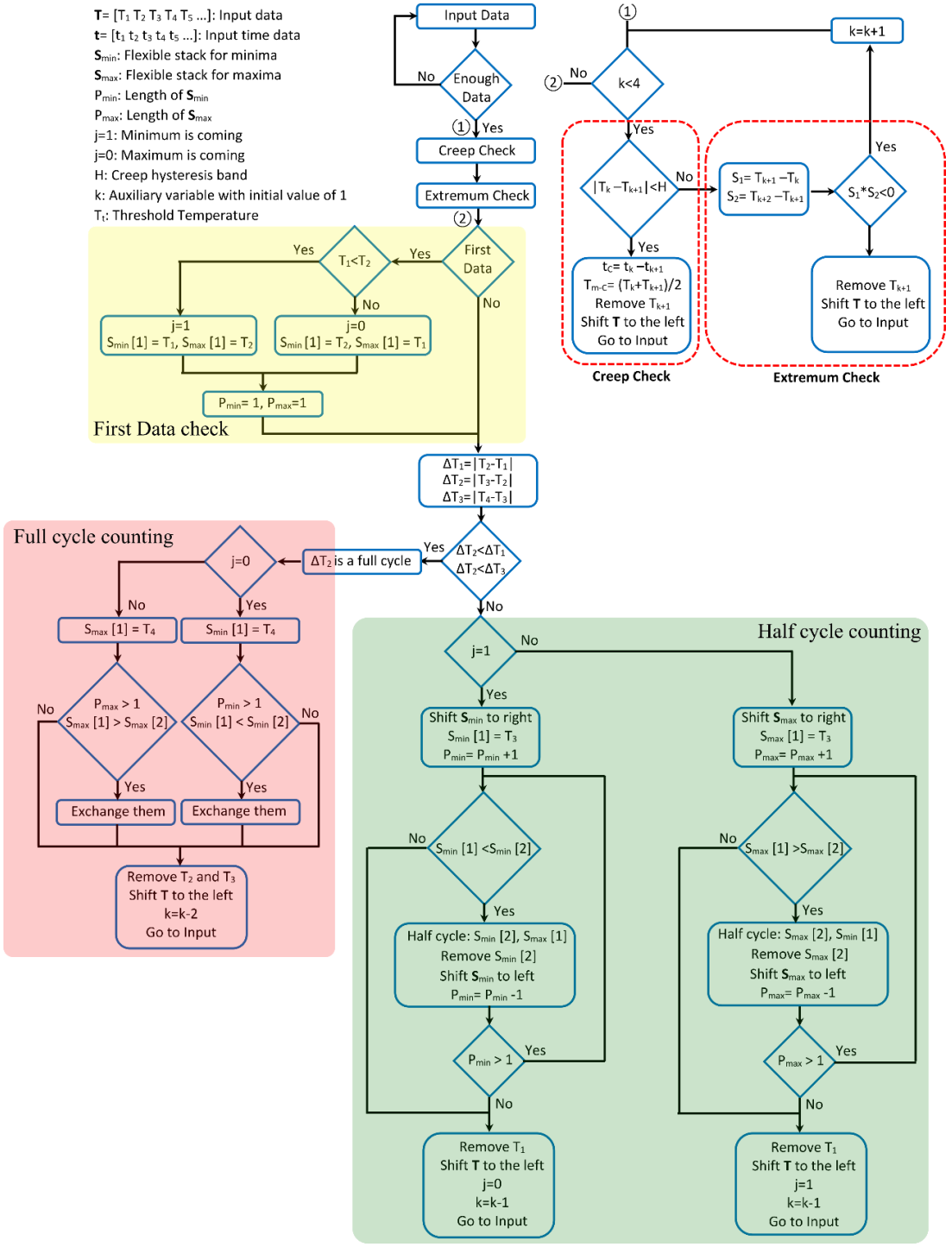


Fig. 4-4. Flowchart of newly proposed online time-temperature-dependent creep-fatigue Rainflow counting algorithm

After that creep check will be done. In this step, the algorithm checks whether or not two consecutive inputs are roughly equal to each other. For this purpose, a creep hysteresis band (H) is defined. It means that if the difference of two consecutive inputs lay between the creep hysteresis band, absolute lower of them will be removed from the input data, then it is also left-shifted and the algorithm waits for the new input. At the same time, the mean temperature of these two points (T_m= (T_*-T_{**})/2) is considered as a creep temperature which is needed in the creep degradation mode (see Fig. 1-25). Moreover, the time period between these two points is also reported which is needed in the creep degradation mode (t_c= t_*-t_{**}). The procedure of creep check has been indicated in Fig. 4-4 as a red dashed-line border on the right corner of the figure.

Then the local extrema extraction is obtained. The extrema extractions are based on discrete derivative. Thus, the direction of two consecutive slopes is taken into account as a local extremum determination. For checking the fourth point, it is necessary to know the fifth point (checking the slope direction). That is why, the enough number of inputs is considered to be five. If two consecutive points do not form a local extremum, absolute lower temperature is removed from the input vector, then it is also left-shifted and the algorithm goes at the beginning and waits until new input data is coming. Otherwise, after checking all points, algorithm exits from creep and extremum checks and continue at ② (top right corner of Fig. 4-4).

After creep and extremum checks and for the first data which is coming out from ②, it is necessary to define two flexible buffers, namely $\mathbf{S_{min}}$ and $\mathbf{S_{max}}$, and determine the kind of the first extremum for activating pointer j. If the first local extremum is minimum, j will be 1. Otherwise it becomes 0. In this step the first two extrema are inserted to their corresponding flexible buffers and the pointers, namely P_{min} and P_{max}, become both 1 (“First data” conditional block diagram in Fig. 4-4**,** yellow highlighted area).

Next, four-point Rainflow algorithm has been applied to the first four input data. If the absolute inner stress swing ($\Delta T_2=|T_2-T_3|$) is simultaneously lower than the two outer stress swings ($\Delta T_1=|T_1-T_2|$ and ($\Delta T_3=|T_3-T_4|$)), full cycle occurs. Thus, one can consider T_2 and T_3 as a full cycle with the stress cycle of $\Delta T_2=|T_2-T_3|$ and the mean temperature of T^e_{mean} which is calculated by (4-1). In this case, depending on the kind of extremum T_2 is replaced by the first element in flexible buffers. If the number of elements in flexible buffers is greater than one, then $\mathbf{S_{min}}$ or $\mathbf{S_{max}}$ have to be sorted up. Then, T_2 and T_3 will be removed from the input data vector and **T** is also left-shifted. The procedure of full cycle counting is indicated by the red highlighted area on the left of Fig. 4-4. And algorithm will wait for two new inputs. Of course, these two inputs must pass through the creep and extremum checks.

However if full cycle is not formed, algorithm tries to find the half cycles (the two rightmost flowcharts in Fig. 4-4, green highlighted area). On one hand, when the first extremum is a local minimum, the procedure will be as follows. **S_{min}** is right-shifted and T_3 will be laid on **S_{min}** [1] (new input). The elements number of **S_{min}** increases by one and accordingly, $P_{min}= P_{min} +1$. After that the first two elements of minimum buffer compare with each other and if the value of new input is lower than the older one, algorithm reports **S_{min}** [2] (old minimum) and **S_{max}** [1] as a half cycle. Then, it crosses out the old minimum (**S_{min}** [2]) from minimum buffer and left-shifts it. Now, because of this removing we have $P_{min}= P_{min}-1$. This half cycle determination procedure is continuing while only one member exists in **S_{min}**. Then T_1 will be removed from **T** and it is left-shifted. Then, j has to be interchanged because the next extremum is certainly maximum (thanks to extremum check). Algorithm now is waiting new input data.

On the other hand, when the first extremum is a local maximum, the procedure will be as follows. **S_{max}** is right-shifted and T_3 will be laid on **S_{max}** [1] (new input). The elements number of **S_{max}** increases by one and accordingly, $P_{max}= P_{max} +1$. After that the first two elements of maximum buffer are compared with each other and if the value of new input is greater than the older one, algorithm reports **S_{max}** [2] (old maximum) and **S_{min}** [1] as a half cycle. Then, it crosses out the old maximum (**S_{max}** [2]) from maximum buffer and left-shifts it. Now, because of this removing we have $P_{max}= P_{max}-1$. This half cycle determination procedure is continuing while only one member exists in **S_{max}**. Then T_1 will be removed from **T** and it is left-shifted. Then, j has to be interchanged because the next extremum is certainly minimum (thanks to extremum check). Algorithm now is waiting new input data. In both cases, it is clear that buffers have been dynamically changed based on the input data.

4-3-3 Case study

In this section, as an application example, the new approach has been applied to a sample load history. Fig. 4-5a shows a thermal cycle with 17 points. For the simplicity, the time between two adjacent points is assumed to be the same and equal to 1 sec. As it was mentioned, the enough input data is five consecutive points. The first sections of algorithm have been allocated to the creep and extremum checks. Creep hysteresis band is assumed to be 3°C. In the first five points, only there is one non-extremum point shown by red highlighted circle (120°C). This point is removed from the thermal cycles as it also can be seen from Fig. 4-5b. Fig. 4-5b shows the thermal cycles after the creep and the extremum cancellation. 75°C and 130°C are saved in the minimum and the maximum buffers, respectively. Inner thermal swing ($\Delta T_2=|T_2-T_3|= 64$°C) is not lower than the two outer thermal swings ($\Delta T_1=|T_1-T_2|=55$°C and $\Delta T_3=|T_3-T_4|= 46$°C), accordingly, full cycle does not occur. Since the first point is the minimum (j=1), **S_{min}** is right-shifted and T_3 lays as the first element in **S_{min}**. New temperature (66°C) in the minimum buffer is lower than the

old one and consequently old minimum temperature (75°C) and the maximum temperature in maximum flexible buffer (130°C) constitutes a half cycle by temperature swing of 55°C and mean temperature of 102.5°C. Therefore the old minimum temperature has been removed from $\mathbf{S_{min}}$ and it has been left-shifted. Finally, T_1 has also been removed from **T** and **T** has been also left-shifted and j→0. Now, algorithm is waiting for the new temperature point. By inserting new point, **T**= [130 66 112 43 45] °C. So, the creep and the extremum checks should have been performed. Regarding the creep hysteresis band, namely 3°C, a creep status occurs in T_4 and T_5. Based on the proposed algorithm, the lower one will be crossed out and algorithm has been going to wait for the new input data. Here T_4 has been removed from **T**. This creep status is indicated by green highlighted area in Fig. 4-5a. j has been also unchanged. Algorithm, again, has been waiting for the new input data. By inserting new data, **T**= [130 66 112 43 135] °C. Inner thermal swing ($\Delta T_2=|T_2-T_3|=$ 46°C) is lower than the two outer thermal swings ($\Delta T_1=|T_1-T_2|=64$°C and $\Delta T_3=|T_3-T_4|=$ 69°C), full cycle does occur. The algorithm reports T_2 and T_3 as a full cycle with the temperature swing of 46°C and mean temperature of

$$t_{FC}=\frac{T_2-T_3}{T_4-T_3}(t_4-t_3)+t_3=\frac{66-112}{43-112}(5-4)+4=4.67\,\text{sec}$$
$$T^{e}_{mean}=\frac{t_3-t_2}{t_{FC}-t_2}\frac{(T_3+T_2)}{2}+\frac{t_{FC}-t_3}{t_{FC}-t_2}\frac{(T_4+T_3)}{2}=84.4^{\circ}\text{C} \quad (4\text{-}3)$$

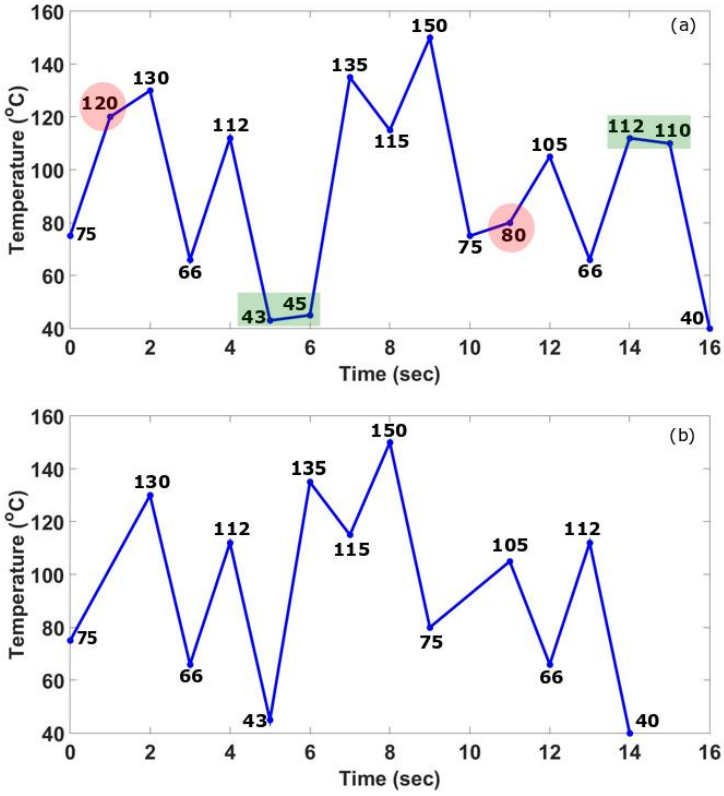


Fig. 4-5. Sample load cycles. (a) Thermal cycles, (b) thermal cycles after creep and extremum checks

Table 4.1. True table of algorithm

T (°C)	CC [t_c T_m] ([sec, °C])	EC(°C)	j	[ΔT_1 ΔT_2 ΔT_3] (°C)	S_{min} (°C)	S_{max} (°C)	FC/HC [ΔT T^e_{mean} T_{mean}] (°C)
[75 120 130 66 112]	—	120	—	—	—	—	—
[75 130 66 112 43]	—	—	—	—	[75]	[130]	—
[75 130 66 112 43]	—	—	1→0	[55 64 46]	[66 75]	[130]	HC [|75-130| 102.5 102.5]
[130 66 112 43 45]	[1 44]	—	0	—	[65]	[130]	—
[130 66 112 43 135]	—	—	0	[64 46 69]	[43]	[130]	FC [|66-112| 84.4 89]
[130 43 135 115 150]	—	—	0→1	[87 92 20]	[43]	[135 130]	HC [|130-43| 86.5 86.5]
[43 135 115 150 75]	—	—	1	[92 20 35]	[43]	[135]	FC [|135-115| 127.72 125]
[43 150 75 80 105]	—	80	1	—	[43]	[135]	—
[43 150 75 105 66]	—	—	1→0	[107 75 30]	[75 43]	[135]	—
[150 75 105 66 112]	—	—	0	[75 30 39]	[75 43]	[135]	FC, [|75-105| 88.75 90]
[150 66 112 110 40]	[1 111]	—	0	—	[75 43]	[135]	—
[150 66 112 40 ...]	Algorithm is waiting for the new data!!!						
CC: Creep Check,	EC: Extremum Check,		FC: Full cycle,		HC: Half cycle		

In the full cycle calculation, the equivalent mean temperature (84.4°C) is different from convention mean temperature (89°C). While as it is seen from Fig. 1-24b, strain-stress curve is thoroughly mean temperature dependent. That is why in this proposed method time-temperature-dependent mean temperature (equivalent mean temperature) has been considered. One can follow the algorithm from Fig. 4-4 and obtain the associated results as listed in Table 4-1. Regarding the input data history (Fig. 4-5a), there are two creep occurrences and two non-extremum points shown as green highlighted and red highlighted regions, respectively.

4-4 Conclusion

In this chapter a novel cycle counting method was proposed. This method represents innovative alternative to the conventional Rainflow algorithm. Our method is a clear improvement on the current Rainflow cycle counting by considering time-temperature-dependent mean temperature and creep failure. Since strain-stress behavior of materials, especially in metals, is thoroughly temperature dependent, the equivalent mean temperature is considered making useful lifetime estimation to be much more accurate. In addition, creep failure mechanism, a very common failure mechanism in high temperatures, has been also considered. Outputs of this chapter will be used in the proposed reliability assessment for sorting a complex mission profile. The sorted data will be applied to Arrhenius-Coffin-Manson and Monkman-Grant lifetime models for fatigue and creep failures, respectively for reliability assessment of power semiconductors. In the next chapter, two reliability frameworks will be explained and the application of this cycle counting algorithm will be thoroughly discussed.

5

Reliability Assessment of DC-DC Converters

5-1 Introduction

The main focus of this chapter is allocated to the reliability assessment of a DC-DC boost power electronics converter. We present two new reliability assessment as well as conventional frameworks. These three frameworks will be studied and their pros and cons will be discussed. Due to the prominent features of PoF based reliability assessment, the principle of the newly proposed reliability models have been based on the PoF model. Therefore, only PoF based reliability assessment of converters will be extensively carried out in this chapter. It has to be mentioned that in the DC-DC boost converter, there assumed to be three critical components as a reliability point of view. IGBT, diode and DC link capacitor as well are considered as potential items. For estimating IGBT and power diode lifetime models (based on the Coffin-Manson-Arrhenius modeling), accelerated power cycling tests and accelerated thermal tests were performed (see Chapter 3). Capacitor lifetime model is extracted from literature [93].

5-2 Conventional PoF based reliability assessment of DC-DC converters

5-2-1 Basic concepts

Conventional PoF based reliability assessment of DC-DC converters has been extensively used in the power semiconductor useful lifetime estimation [93]. PoF based reliability assessment aims to find failure mechanisms and investigate the effects of mission profile on the critical failure mechanisms. This leads to transfer reliability analysis from component level to the failure mechanism and enhances it from reliability prediction to design for reliability [95].

Based on determined failure root causes (such as power cycling or temperature swing) and the mission profile and employing reliability models, one can estimate the aging of a component and its useful lifetime regarding its mission profile.

Fig. 5-1 illustrates the conventional reliability framework of critical components of converters (power semiconductors). Regarding this figure, one can find out that how mission profile can affect the reliability assessment of power components. Mission profile (vehicle speed, wind velocity, etc.) along with electrical and thermal parameters and ambient temperature are the main inputs of this framework. Mission profile has to be translated to electrical profiles such as power or current profiles by translating mechanical power (or other kind of powers and energies) to electrical power.

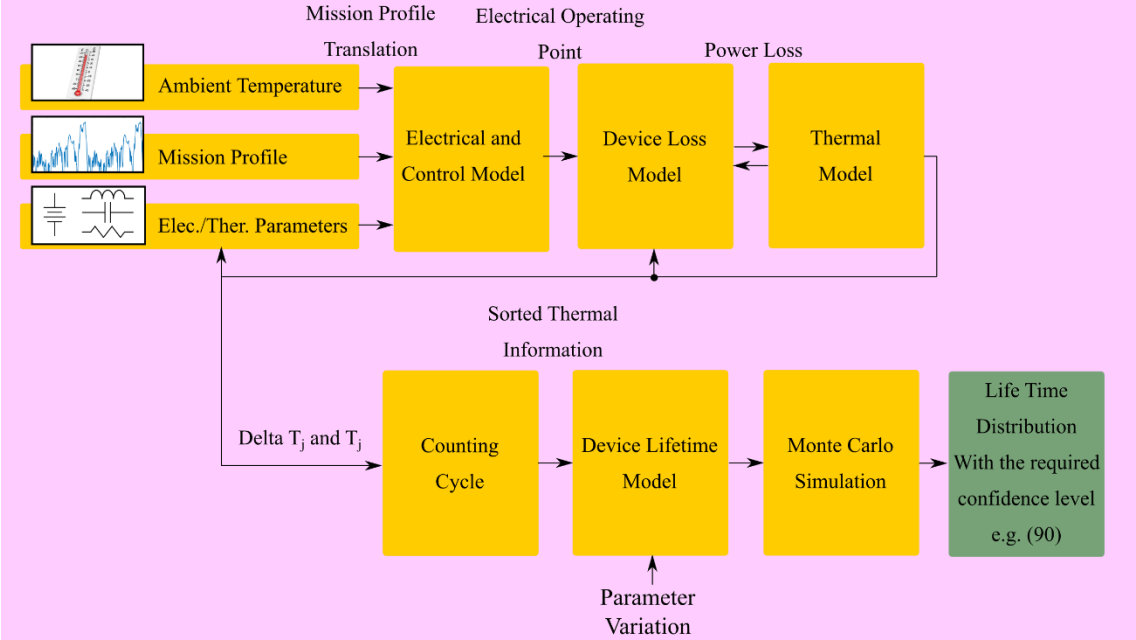


Fig. 5-1. Conventional reliability assessment of critical components of power electronic systems.

Translated electrical power profile has been inserted to the electrical model. Using this translated mission profile, electrical/thermal parameters, ambient temperature and some conditions (such as output voltage range) as well, one can find the electrical operating point. Output of electrical model block diagram is the processed electrical mission profile such as components' currents and voltages. Control model can also be considered in the closed loop converters. Since ambient temperature and thermal parameters of power semiconductors have both significant effects on the performance of converter and have to be considered in electrical and control model of converter, a feedback is defined from output of thermal modeling to the electrical and thermal parameters.

After obtaining electrical operating point profile, device loss model has to be performed owing to the potential failure mechanisms. In addition to electrical operating point profile, junction temperatures of power semiconductors make a meaningful contribution in calculating power losses of power semiconductors and thereby, a feedback has been defined for power loss model as shown in Fig. 5-1. It

was also mentioned that because power loss calculation is temperature dependent, an iterative algorithm has to be applied.

Since the failure root causes of the power semiconductors are related to thermal issues (creep-fatigue failure mechanism), the power losses of power semiconductors have been estimated. The power losses profile is inserted to the thermal modeling of the power electronic system as main heat sources. Based on these heat sources and the global thermal model of power electronic system, one can obtain the junction temperatures of the power semiconductors including their swings and mean temperature. The output of this stage is junction temperatures profiles.

The main root causes of the failures in power semiconductors are the junction temperature swing and the mean junction temperature. Although, output of thermal modelling is the trend of junction temperature, it is a complex information and difficult to be detached and analyzed. Therefore, a cycle counting algorithm has to be applied to detaching junction temperature into its swings and mean values. A rainflow algorithm is commonly employed for detaching and sorting the temperature data.

The sorted junction temperature data is then applied to the lifetime models of power semiconductors. It is notable that the modified Coffin-Manson lifetime model has been widely used in lifetime estimation of power semiconductors [174], [175]. The constant coefficients of the lifetime model are material dependent and extracted from accelerated aging tests. Since there exist some uncertainties due to the few population of accelerated aging test, a variation is considered in each of lifetime model constant coefficients. Generally, lifetime model constant coefficients are assumed to be normally distributed with 5% deviation around their mean values.

For considering these parameters variations, Monte Carlo simulation is applied to this method. By Monte Carlo application, one can find a damage distribution instead of an exact damage level in the reliability assessment of converters.

5-2-2 DC-DC Boost converter reliability assessment based on the conventional framework

A conventional DC-DC boost converter is considered here as shown in Fig. 5-2. Its specifications are listed in Table 5-1. The considered converter is assumed to be employed in a hybrid electric vehicle (HEV) as an interface converter between battery bank and the electrical motor drive system.

Table 5-1Working Conditions and Parameters Values

Parameter	Value	Parameter	VALUE
V_i	200V	V_{out}	400V
P_o	3000W	R	53.34 Ohm
L	2.50mH	r_L	0.3 Ohm
C	47 µF	r_C	0.05 Ohm
r_D	0.04 Ohm @T_j=175°C	V_{D0}	1V @T_j=175°C
r_Q	0.0726 Ohm @T_j=175°C	V_{CE0}	0.81V @T_j=175°C

The considered mission profile is a well-known driving cycle, namely, worldwide harmonized light vehicles test procedure (WLTP-class3) as shown in Fig. 5-3. The failure root causes in the power semiconductors are including junction temperature swing and mean junction temperature modelling with Coffin-Manson-Arrhenius and Monkman-Grant [174], [175]. Therefore, the mission profile has to be translated to these temperatures through the electrical, power loss and thermal modeling as shown in Fig. 5-1. Accordingly, HEV speed based on WLTP-class3 has translated to the required power as expressed in the following equation:

$$P_{conv} = \frac{B_S V}{\eta_t}\left\{Mg\left(f_r + i\right) + \frac{1}{2}\rho_a C_D A_f V^2 + M\delta\frac{dV}{dt}\right\} + P_{aux} \qquad (5\text{-}1)$$

where V is the vehicle speed, B_S the battery share of power transferring, η_t the total efficiency of transmission system and electric motor. M is the mass of the vehicle, g the gravity, f_r the rolling resistance coefficient, ρ_a the air density, C_D the aerodynamic drag coefficient, A_f the front area of the vehicle and δ the mass factor. P_{aux} is 100W for auxiliary equipment. All the parameters are in SI units. This power has been inserted to power loss and thermal modeling leading to find the IGBT's and diode's junction temperatures. It has to be mentioned that in this modeling ambient temperature was assumed to be 40°C.

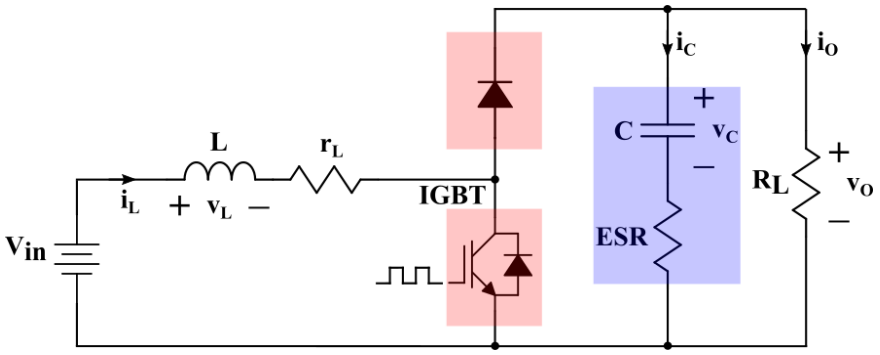


Fig. 5-2. A conventional DC-DC boost power converter

Electrical, power loss and thermal modeling have been performed based on what was expressed in Chapter 2. Using the equations and correlations of Chapter 2, one

can find diode and IGBT junction temperature profiles as shown in Fig. 5-4. The maximum junction temperature never reaches its allowable maximum junction temperature either in IGBT and diode due to the dynamic response of thermal impedances. As described in Chapter two, analytic model has been used for thermal modeling. In other words, the dynamic of mission profile is much faster than the dynamic of thermal impedances. Regarding higher IGBT power loss, higher junction temperature occurs in comparison with diode junction temperature.

Now, the junction temperature profiles of IGBT and diode have to be sorted using cycle counting algorithm as it was completely described in Chapter 4. The rainflow algorithm have detached the junction temperature data based on their swings and mean values for fatigue liftime model. It has also extracted dwelling times and their corresponding temperatures for creep lifetime model. Fig. 5-5a depicts the sorted junction temperature of IGBT and diode data. This figure shows the junction temperature swings and mean junction temperatures extracted from one mission profile, namely 30 minutes driving cycle. Fig. 5-5b shows the dwelling times versus junction temperatures of IGBT and diode. The data extracted from Fig. 5-5a will be applied to Coffin-Manson-Arrhenius fatigue lifetime model and those extracted from Fig. 5-5b will be applied to Monkman-Grant creep lifetime model as the two most probable failure mechanisms in the IGBT and diode. Their interactions will be considered using a linear accumulated damage model.

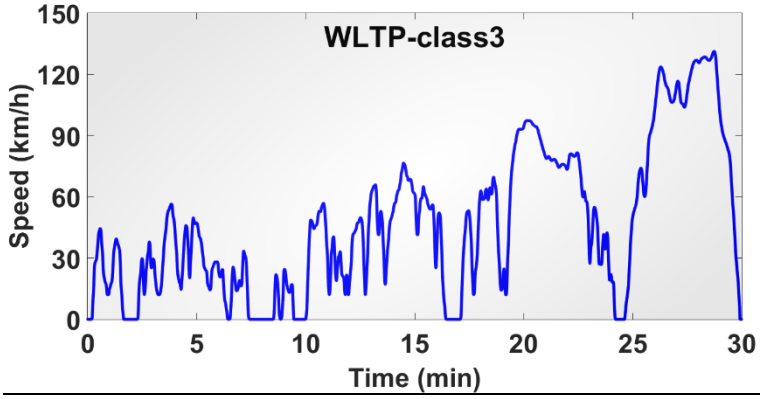


Fig. 5-3. Mission profile, HEV speed based on WLTP-class3.

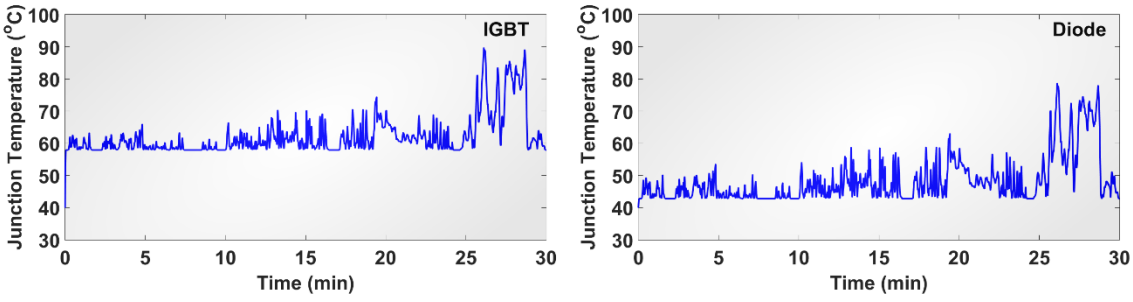
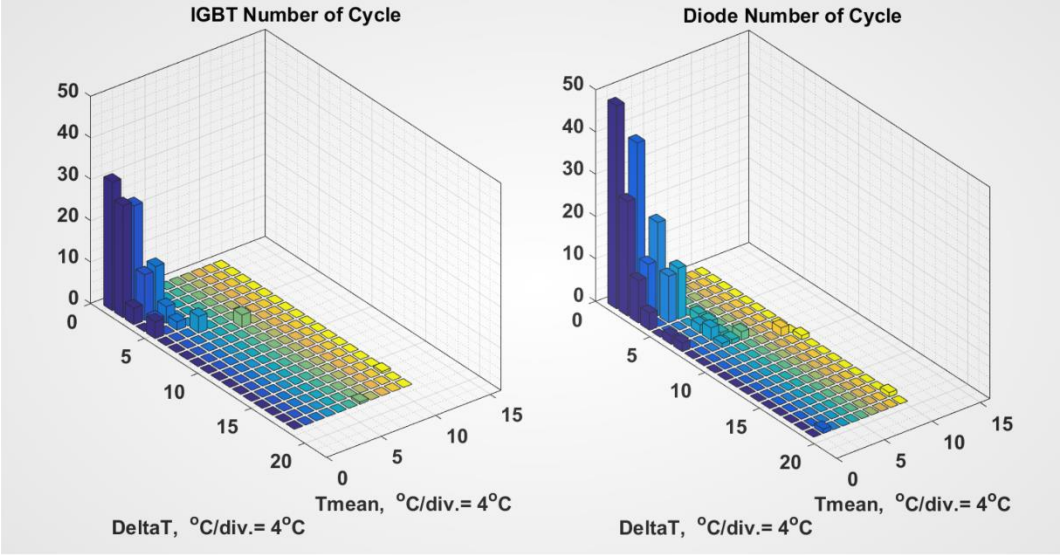
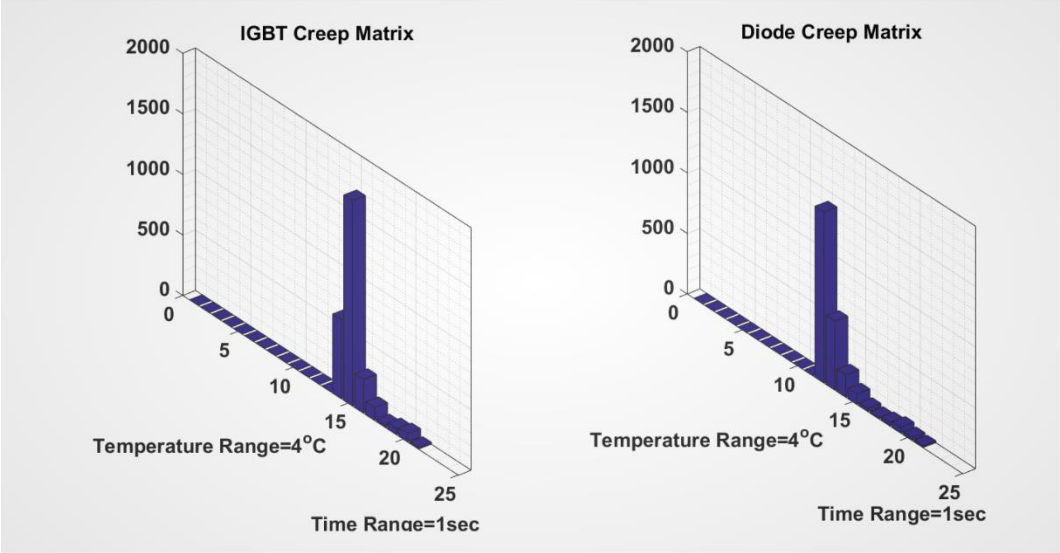


Fig. 5-4. Junction temperature profiles.



(a)



(b)

Fig. 5-5. Sorted junction temperature of IGBT and power diode for (a) fatigue and (b) creep lifetime models.

Based on the lifetime model of IGBT and power diode (Section 1-2-3-7-1, Section 1-2-3-7-2) and their extracted parameters from APC and creep tests (Section 3-2-2, Section 3-4), one can estimate the useful lifetime of IGBT and diode as described here. The lifetime model of power semiconductors is rewritten as follows:

$$N_f(T_m, \Delta T_j) = A \times \Delta T_j^{\alpha} \times \exp(Q/RT_m)$$
$$t_C = \left(\frac{C_{MG}}{\dot{\varepsilon}_{cr}} \right)^{1/\beta} \quad (5\text{-}2)$$

where R and Q are the gas constant (8.314 JMol-1.K-1), internal energy and T_m is the mean junction temperature of devices in Kelvin and A, α and Q are device dependent

and estimated by curve fitting from APC aging tests (section 3-2-2). $\dot{\varepsilon}_{cr}$ is the stable creep strain rate (equation (1-11)), C_{MG} and β are constant and material-dependent and extracted from creep test (section 3-4). The constant coefficients are extracted as follows for IGBT and diode:

$$\begin{cases} A \sim N(4.352\times10^{3}, 0.725\times10^{2}) \\ \alpha \sim N(-1.117, 0.0186) \\ Q \sim N(1.852\times10^{4}, 0.31\times10^{3}) \end{cases} \quad \text{For IGBT}$$

$$\begin{cases} A \sim N(4.093\times10^{3}, 0.682\times10^{2}) \\ \alpha \sim N(-1.128, 0.0188) \\ Q \sim N(1.861\times10^{4}, 0.31\times10^{3}) \end{cases} \quad \text{For Diode} \qquad (5\text{-}3)$$

$$\begin{cases} \beta \sim N(1.02\times10^{4}, 0.17) \\ C_{MG} \sim N(2.2\times10^{-3}, 0.36\times10^{-4}) \end{cases} \quad \text{For IGBT and Diode}$$

As it is observed, the constant coefficients of power semiconductors lifetime models are assumed to be normally distributed. For estimating the reliability of IGBT or power diode, one can employ well-known Monte Carlo simulation. Monte Carlo simulation has been performed for 50000 samples via MATLAB environment. Fig. 5-6 demonstrates the frequency of IGBT and diode damages using creep-fatigue linear damage model (equation (1-17) and Fig. 1-25). Regarding this figure, it seems that normal distribution curve fitting is suitable for evaluating the damage distribution. Fig. 5-7 depicts the reliability function of IGBT and power diode. One driving cycle damage of IGBT and power diode have normal distribution of:

$$\begin{aligned} D_{IGBT} &\sim N\left(1.11\times10^{-4}, \left(5.36\times10^{-6}\right)^{2}\right) \\ D_{Diode} &\sim N\left(2.33\times10^{-4}, \left(1.14\times10^{-5}\right)^{2}\right) \end{aligned} \qquad (5\text{-}4)$$

Power capacitor is considered to have a time to failure distribution following Weibull damage model ($D_{cap}(t)\sim W(\eta, \beta)$ where η and β are the scale factor and shape factor, respectively) [6]. In this case study, power capacitor is considered with the following time to failure distribution [118] (see Fig. 5-8.):

$$D_{Cap}(t;\eta,\beta) \sim W(1471680, 1.93) \qquad (5\text{-}5)$$

Since we assumed that three critical components have been considered, a multicomponents reliability assessment of converter has to be utilized. After the reliability (or surviving function) of individual power electronics components under the given mission profiles, overall reliability of the global converter system can be estimated depending on the logic connection of the components. In this case study, all the three components are logically connected in series, i.e. if one of them is failing, the global system will be failed. Therefore

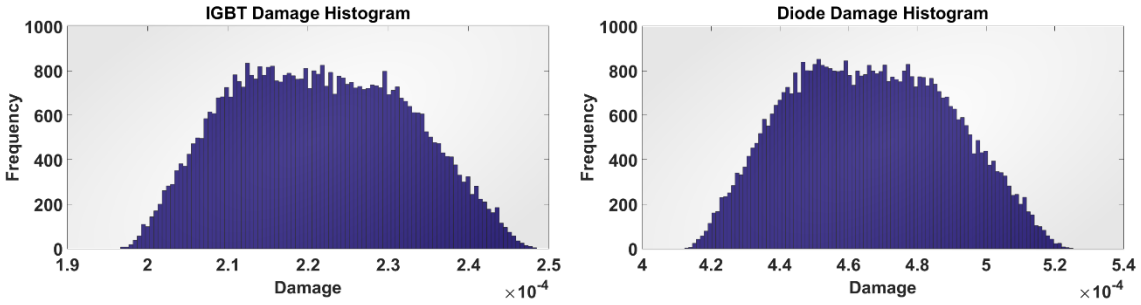


Fig. 5-6. Frequency of damages in IGBT and diode.

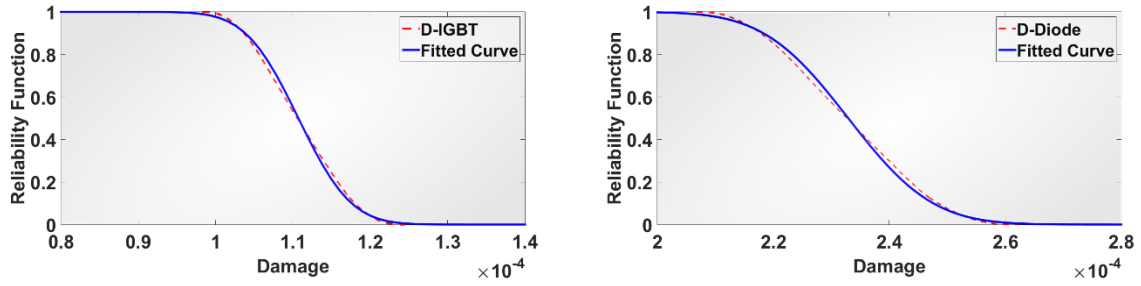


Fig. 5-7. Reliability function of IGBT and diode damages during one driving cycle

$$R_{Global-Series}(t) = \prod_{x=1}^{3} R_x(t) \tag{5-6}$$

where $R_{Global\text{-}Series}$ is the system overall reliability and R_x is the x^{th} component's reliability function. Therefore, the global reliability of the considered multicomponent DC-DC boost power converter is the product of reliability functions of IGBT, power diode and power capacitor as shown in Fig. 5-9. Useful lifetime of power capacitor is much higher than the other components, namely IGBT and diode. B_{10} reliability is the estimated time when the probability of failure will reach 10%. In this case study, B_{10} reliability of the global system is 66680 hours. It means that 10% of the power electronic system is expected to fail by 7.61 years of operation.

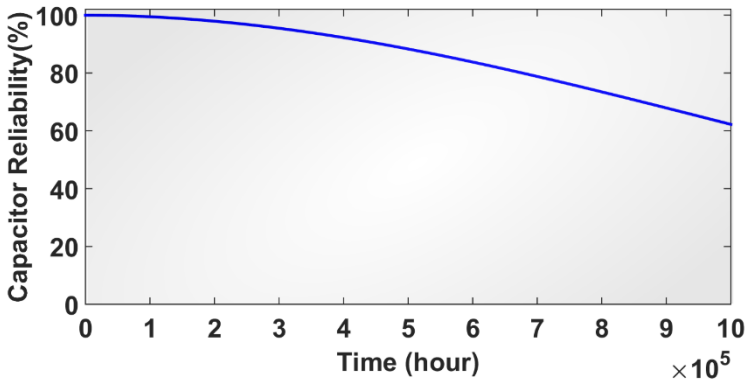


Fig. 5.8. Reliability function of power capacitor in terms of hour

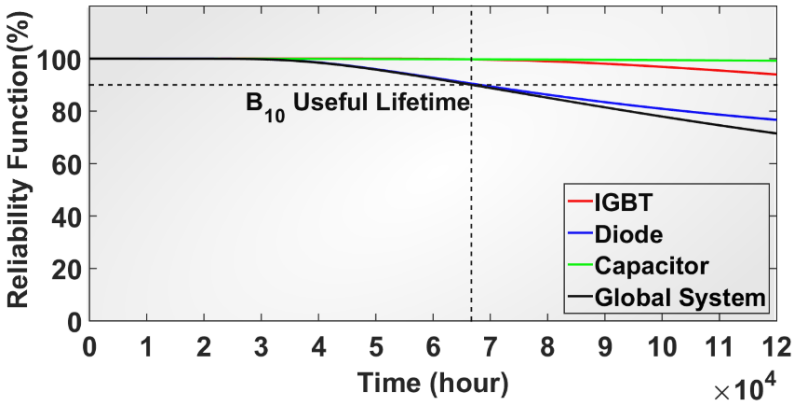


Fig. 5.9. Reliability function of global multi component system, power capacitor, IGBT and power diode

5-2-3 Discussion

Reliability assessment of the conventional DC-DC boost converter has been considered in the previous section. The result demonstrates the B_{10} reliability of 66680 hours for the global systems containing three critical components, namely IGBT, diode and power capacitor. Although, this framework has utilized Monte Carlo simulation for the consideration of the parameter variations (due to the uncertainties in the APC aging tests), it is not able to take into account the dependency of various components. It means that degradation of any components cannot be considered in the useful lifetime estimation of converter while it was shown that these dependencies are paramount of importance in this case study (refer to chapter 3). In addition, this reliability framework is not capable of assessing the reliability in the redundant systems. Although, this method can deal with the simple reliability constructions such as series, parallel and k-out-of-n systems, it is not suitable for reliability evaluation of redundant systems such as interleaved power converters. Because in the redundant systems, by changing the configuration of the system, the EOP and TOP of the power converter would be varied leading to different damage models.

5-3 Interval reliability assessment

These various components have knock-on effects on each other's performances (both thermally and electrically) during their working in the power converters. As a perfect example, a common DC-DC converter is demonstrated in Fig. 5-10. Regarding Fig. 5-10, capacitance and its ESR changes can influence power semiconductors' performances. For example, the greater capacitor voltage ripple (the lower capacitance or the higher ESR), the more induced switching power losses in the power semiconductors.

Consequently, junction temperatures of IGBT and diode will be increased. These changes in the junction temperatures of IGBT and diode can directly affect their

internal parameters (such as voltage drop and internal resistance). Along with the internal parameters variations, since diode and IGBT are thermally coupled (almost always mounted on the same heat sink), either increase of diode junction temperature or IGBT's can indirectly have effects on the TOP of each other in which finally affect EOP of power converter. Electrical and thermal correlations are shown by red and blue double-arrowed line in Fig. 5-10. Double-arrowed lines show that there are coupling effects among the components.

Therefore, internal parameters of the components such as junction to case thermal resistance and internal voltage in power semiconductors, and capacitance and dissipation factor in power capacitors can be changed [93], [133].

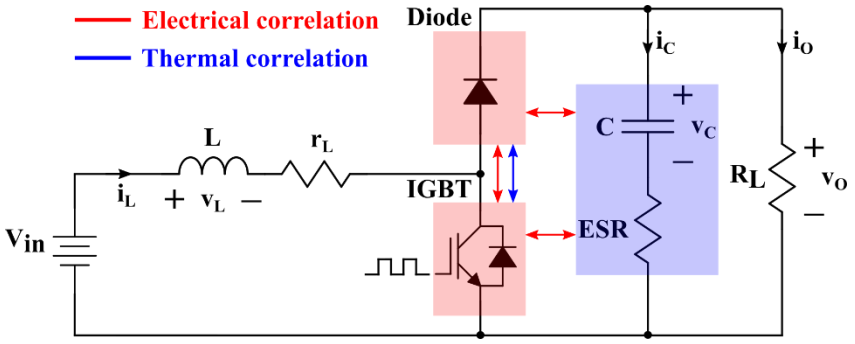


Fig. 5-10. A conventional DC-DC boost power converter.

Parameters' drifting of capacitors, IGBT and diode have electrical and thermal effects in the performance of a power converter. These parameters' drifting can be due to the components' degradation. Accordingly, coupling effects of components' aging on the performance of converter and its elements (EOP and TOP) have to be considered. These effects had been validated by implementing a customized DC-DC boost converter as described in Section 3-5. Table 3-3 demonstrates the importance of these effects. For having a more reasonable ULE of power converters, these coupling effects have to be undertaken in the reliability assessment. In this section, we want to state the opinion of employing interval reliability assessment to cover the effects of these parameters' drifting owing to the aging. Instead of presenting an inaccurate ULE for power converters, the proposed method tries to put forward a range for the ULE (i-ULE) leading to much more reasonable analysis for engineering.

5-3-1 Interval reliability assessment of DC-DC boost converters

Variability of the power components either owing to the degradation or their manufactured processes can be highly effective in TOP and EOP of power converters. Since reliability assessment of power converters is thoroughly TOP- and EOP-dependent (regarding their failure mechanisms and the mission profile they have been exposed to), these variations have to be taken into account. Fig. 5-11

demonstrates a new ULE algorithm. Based on this new algorithm, one can find an interval reliability estimation.

In this algorithm, ambient temperature profile as well as mission profile have been considered as the interval values regarding their uncertainties. Electrical and thermal parameters' deviations (due to their degradations) have been also considered as the interval values with the specified range from their new to fully-degraded values ($[X_{new}\ X_{fully\text{-}degraded}]$). Although there are different definitions for the failure [250], here catastrophic failure and degradation failure have been distinguished from each other. Catastrophic failure has been defined as a state in which the power converter no longer cannot work such as permanent short circuit or open circuit of power components in the power converter. Definition of degradation failure has been allocated to the gradually degradation of the power components and henceforth it has been called as a failure.

Regarding the proposed algorithm (Fig. 5-11), the ambient temperature and the mission profile (interval values with the preset ranges e.g. ±5% deviation from their actual values) and electrical and thermal constant parameters (interval values with the ranges from the new to the fully degraded values) have been inserted to the interval analysis. This analysis has mapped the conventional mathematical domain to the interval domain in which every quantities have had a range. Based on these inputs, the actual and available mission profile (e.g. wind speed, sun irradiation and vehicle speed) has been translated to the electrical parameters e.g. current, voltage or electrical power. Again it has to be noted that this translated mission profile is also an interval value. Regarding to the converter's specifications, its controlling system and its desired reference points, state variables and state matrix of power system can be extracted from a mathematical model. Every matrix, vector or other quantities in the electrical modeling have been changed to the interval matrices, vectors and quantities, respectively. Accordingly, the output of this stage become a range for electrical operating point for each point of translated mission profile.

In the next step, interval EOP (i-EOP) has been inserted to the device loss model. Since device loss model completely depends on the junction temperature of device (T_j), a feedback is required from semiconductor's thermal modeling. Regarding i-EOP and interval junction temperature (i-T_j), one can find a range for the power losses of the devices. This power losses' range has been inserted to the thermal modeling of a power converter. The outputs of thermal modeling are i-T_j and i-ΔT_j (interval junction temperature swing). As previously mentioned, the main and critical failure mechanism in the power semiconductors is electro-thermo-mechanical creep-fatigue. This failure occurs owing to the junction temperature swings and junction mean temperature based on the Coffin-Manson-Arrhenius and Monkman-Grant models [174], [175].

In the next step, i-T_j and i-ΔT_j (i-TOP) i.e. failure root causes of the interested failure mechanism have to be sorted based on the one of the cycle counting algorithms. This cycle counting step can be based on different algorithms. Despite of the philosophy of cycle counting algorithm, one can note that the outputs of this step are also interval values. Now, the sorted i-TOP have been inserted to the device lifetime model. As mentioned previously, based on the critical failure mechanism, Coffin-Manson-Arrhenius and Monkman-Grant models as well as some constant parameters extracted from datasheet or accelerated power/thermal cycle tests have been used for i-ULE. Based on the proposed ULE algorithm (i-ULE), the reliability assessment of power electronic systems has become a range instead of an exact value. This feature demonstrates the feasibility of employing i-ULE instead of conventional ULE. In this case, the degradations of the power components have been also taken into account leading to much more reasonable useful lifetime estimation of power converters.

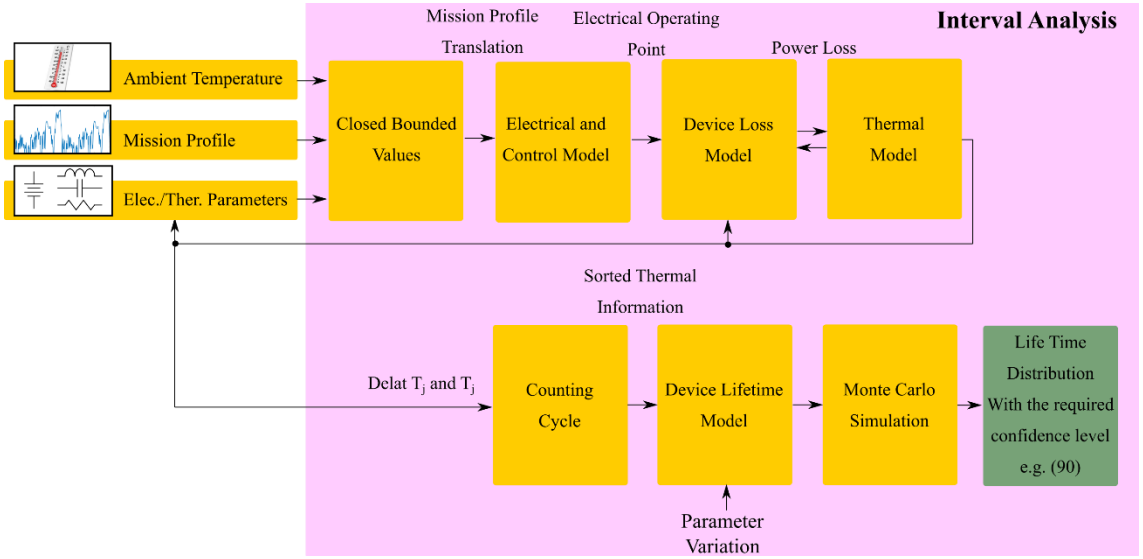


Fig. 5-11. New algorithm of interval reliability assessment for converters.

5-3-2 Interval analysis fundamental

Interval arithmetic has been extensively employed in digital numerical computation [251]. At the beginning, lack of necessity of analyzing the pointwise floating point computations led to gaining keen attractions [252]. However, it has become an attractive quantitative-sensitivity analysis and solver of nonlinear problems among researchers and engineers [227]. Interval analysis has numerous advantages including correctness, totality, closedness, optimality and efficiency. Explaining all the above mentioned features is beyond this study and interested readers are referred to [251]. The key factor that encourages us to use interval arithmetic in the reliability assessment of converters is its correctness. In this case, interval arithmetic has been applied to all the calculations and modeling of the power converters. Since all the input quantities have bounded ranges (owing to their

degradation processes or even their uncertainties), the output will be interval ULE (i-ULE) with the higher accuracy in comparison with the conventional ULE. In the following of this section, fundamental of interval analysis and its application to the basic operators will be discussed.

This method is based on the bounded arithmetic which means that every parameter can have not an exact value but a bounded interval. This interval can be due to the manufacturing tolerance, aging, and temperature dependency. Here although, the main purpose of using interval analysis is to consider the parameter value variations resulted from aging and degradation, the manufacturing tolerance and temperature dependency can also be taken into account. Although there are different types of interval including closed, open, upper half open and lower half open, here only closed interval numbers have been considered. Basic terms and concepts will have been indicated. It should be mentioned that only main and related issues will be discussed and accordingly the interested readers refer to [252].

A closed real interval x is a set of real numbers defined as follows

$$X = \left[\underline{X}, \overline{X} \right] = \left\{ x \in R : \underline{X} \le x \le \overline{X} \right\} \tag{5-7}$$

where $\underline{X}$ is the minimum and $\overline{X}$ is the maximum values of parameter X which can be taken. As an example, $\underline{X}$ can be considered as a value of a parameter of a new device, while $\overline{X}$ can be considered as a degraded value. Other types of intervals including open and half-open intervals appear in mathematics. However, our focus here will be on the closed intervals.

Two intervals X and Y are said to be equal provided that

$$X = Y \quad \text{if} \quad \underline{X} = \underline{Y}, \quad \overline{X} = \overline{Y} \tag{5-8}$$

A real number with the exact value can be expressed as an interval real number with the same bounded range i.e. [X, X]. The next step is to define the basic arithmetic operations between closed intervals. Instead of applying operations to the only real numbers, now we should apply them to the set of real numbers (closed interval). For instance, sum of two intervals results in a new interval containing the sums of all pairs of numbers. Accordingly, sum of two intervals X and Y is the set given by

$$X + Y = \left[\underline{X} + \underline{Y}, \overline{X} + \overline{Y} \right] = \{ x + y : x \in X, \ y \in Y \} \tag{5-9}$$

The difference of two intervals X and Y is the set given by

$$X - Y = \left[\underline{X} - \overline{Y}, \overline{X} - \underline{Y} \right] = \{ x - y : x \in X, \ y \in Y \} \tag{5-10}$$

The product of X and Y is given by

$$X.Y = \begin{bmatrix} \min\left(\underline{X}\underline{Y}, \underline{X}\overline{Y}, \overline{X}\underline{Y}, \overline{X}\overline{Y}\right), \\ \max\left(\underline{X}\underline{Y}, \underline{X}\overline{Y}, \overline{X}\underline{Y}, \overline{X}\overline{Y}\right) \end{bmatrix} = \{x.y \ : \ x \in X, \ y \in Y \} \quad (5\text{-}11)$$

Dividing interval X to Y is given by

$$X / Y = \frac{\left[\underline{X}, \overline{X}\right]}{\left[\underline{Y}, \overline{Y}\right]} = \left[\underline{X}, \overline{X}\right] * \frac{1}{\left[\underline{Y}, \overline{Y}\right]} = \left[\underline{X}, \overline{X}\right] * \left[\frac{1}{\overline{Y}}, \frac{1}{\underline{Y}}\right] = \{x / y \ : \ x \in X, \ y \in Y \} \quad (5\text{-}12)$$

In addition, we can express the intervals with two parameters expressing the mean value (mid(x)) of interval as well as its radius (rad(X)) defining as follow

$$\begin{aligned} \mathrm{mid}(X) &= 1/2\left(\overline{X} + \underline{X}\right) \\ \mathrm{rad}(X) &= 1/2\left(\overline{X} - \underline{X}\right) \end{aligned} \quad (5\text{-}13)$$

Based on what has been expressed here, one can easily generalize all conventional mathematical arithmetic. In numerous engineering environments, especially electrical engineering, mathematic models of physical phenomena are including either matrix or vector forms. As it was mentioned, one has to use the state space equations (in matrix form) for electrical modeling. In addition, in the sort of thermal modeling in which mutual effect of heating systems (mutual effect of heat power sources on each other) has been considered, a thermal impedance matrix has been introduced. Therefore, discussing the interval matrices has paramount of importance. Interval matrix is a matrix whose elements are interval numbers given as follows:

$$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} = \begin{bmatrix} \left[\underline{A}_{11}, \overline{A}_{11}\right] & \left[\underline{A}_{12}, \overline{A}_{12}\right] \\ \left[\underline{A}_{21}, \overline{A}_{21}\right] & \left[\underline{A}_{22}, \overline{A}_{22}\right] \end{bmatrix} \quad (5\text{-}14)$$

All the basic operators can be easily applied in vector or matrix forms based on what has been said previously. Expressing all the issues related to the interval analysis is beyond of this study. In this study modified INTLAB software tool has been used. This package is one of the MATLAB tools and can be easily implemented in MATLAB. INTLAB uses MATLAB's arithmetic based on the IEEE 754 binary standard arithmetic.

5-3-3 A paradigm shift from ULE to i-ULE

The degradations of power components lead to the TOP and EOP changes in a power converter. It means that not only does the degradation of one device accelerate its aging, but also it accelerates other devices' aging. In the previous studies, there cannot be found any structural solution for considering these effects. In this section, a conventional DC-DC boost converter as shown in Fig. 5-2 has been considered. As it was mentioned in the previous section, this conventional DC-DC boost converter is assumed to be an interface in HEV.

It has to be mentioned that in this modeling, ambient temperature was assumed to be 40°C with ±5%. Therefore, ambient temperature became as a bounded value i.e. Ta=[38 42] °C. It is also the case for the vehicle speed. Every point in the vehicle speed was allocated as an interval value i.e. v=[95%vrated 105%vrated].

Electrical, power loss and thermal modeling have been performed based on what expressed in Chapter 2 for both new and fully degraded cases. Using the equations and correlations on chapter 2, one can find diode and IGBT junction temperature profiles as shown in Fig. 5.12 in the fully degraded case. It has to be mentioned that the new case has been depicted in Fig. 5-4. The maximum junction temperature never reaches its allowable maximum junction temperature either in IGBT and diode due to the dynamic response of thermal impedance. However, IGBT and diode experience at least an increase of 12°C in their junction temperatures as predicted.

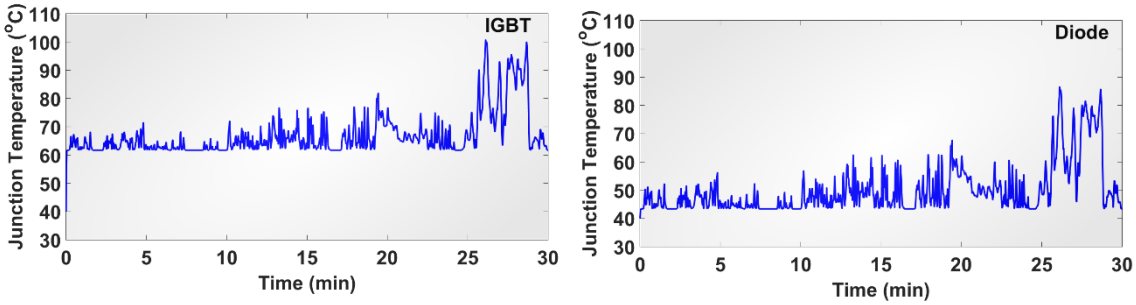
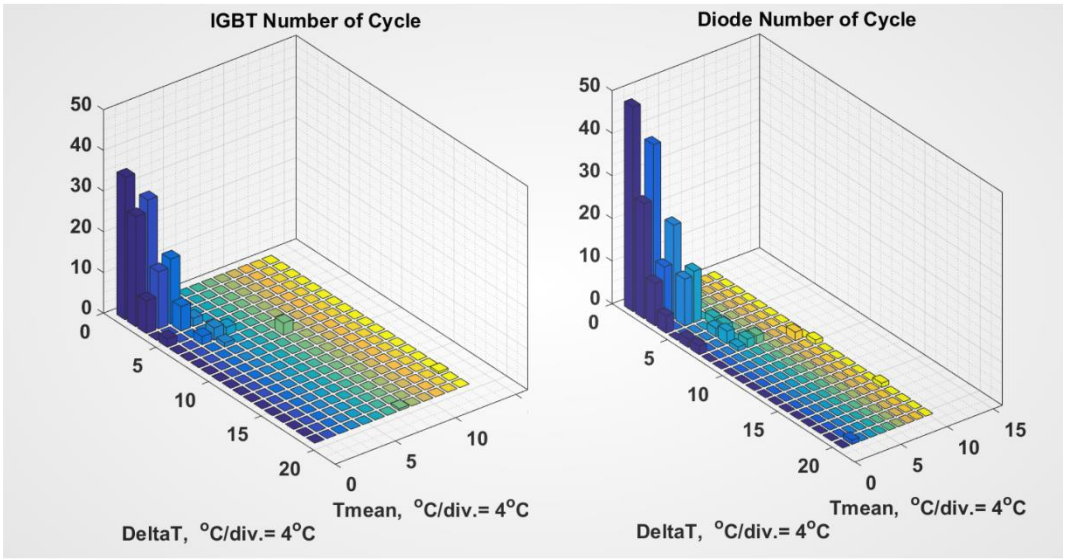
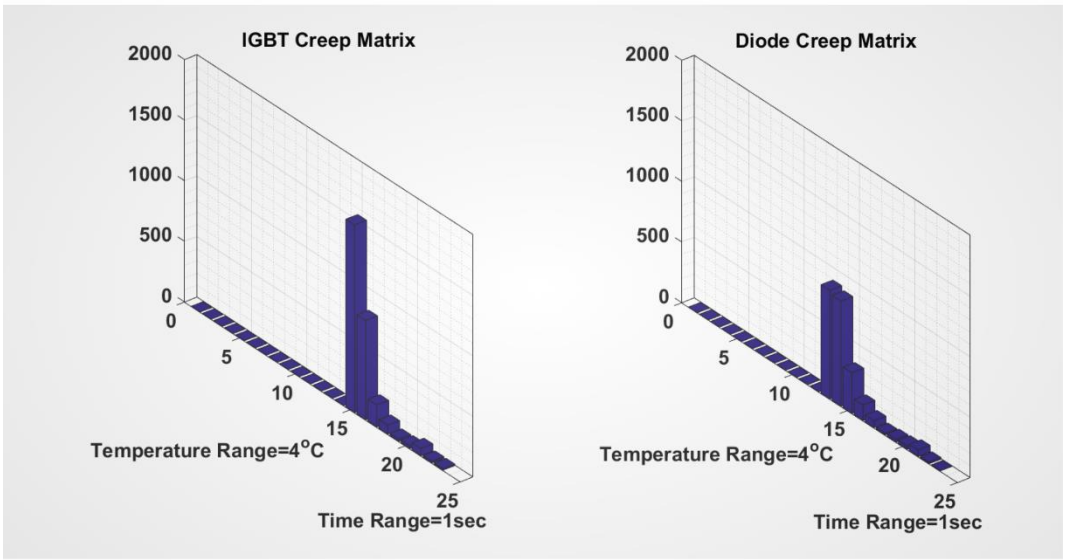


Fig. 5-12. Junction temperature profiles of a) IGBT and b) diode in the fully degraded case.

Now, the junction temperature profiles of IGBT and diode have to be sorted using cycle counting algorithm as it was completely described in Chapter 4 in both new and fully degraded. The rainflow algorithm have detached the junction temperature data based on their swings and mean values for fatigue liftime model. It has also extracted dwelling times and their corresponding temperatures for creep lifetime model. Fig. 5-5 depicts the sorted junction temperature of IGBT and diode data in the new case while Fig. 5-13 demonstrates the sorted junction temperature of IGBT and diode data in the degraded case. Fig. 5-13a depicts the sorted junction temperature of IGBT and diode data. This figure shows the junction temperature swings and mean junction temperatures extracted from one mission profile, namely 30 minutes driving cycle. Fig. 5-13b shows the dwelling times versus junction temperatures of IGBT and diode. The data extracted from Fig. 5-13a will be applied to Coffin-Manson-Arrhenius fatigue lifetime model and those extracted from Fig. 5-13b will be applied to Monkman-Grant creep lifetime model as the two most probable failure mechanisms in the IGBT and diode. Their interactions will be considered using a linear accumulated damage model.



(a)



(b)

Fig. 5.13. Sorted junction temperature of IGBT and diode in the fully degraded case.

Based on the lifetime model of IGBT and power diode (Section 1-2-3-7-1, Section 1-2-3-7-2) and their extracted parameters from APC and creep tests (Section 3-2-2, Section 3-4), one can estimate the useful lifetime of IGBT and diode in fully degraded case as described in eq. (5-2) , (5-3).

For the fully degraded case, Monte Carlo simulation is also applied with 50000 samples. Fig. 5-14 demonstrates the frequency of IGBT and diode damage for this case. Regarding this figure, it seems that normal distribution curve fitting is suitable for evaluating the damage distribution. Fig. 5.15 depicts the reliability function of IGBT and power diode in the fully degraded case. One driving cycle damage of IGBT and power diode have normal distribution of

$$D_{IGBT} \sim N\left(1.8\times10^{-4}, 8.73\left(5.36\times10^{-6}\right)^2\right)$$
$$D_{Diode} \sim N\left(3.01\times10^{-4}, \left(1.47\times10^{-5}\right)^2\right) \quad (5\text{-}15)$$

Power capacitor has the degradation trend of equation (5-5). Since we assumed that three critical components have been considered, a multicomponents reliability assessment of converter has to be utilized. Therefore, regarding equation (5-6), the global reliability of the considered multicomponent DC-DC boost power converter is the product of reliability functions of IGBT, diode and power capacitor as shown in Fig. 5-16. Useful lifetime of power capacitor is much higher than the other components, namely IGBT and diode. In fully degraded case, B_{10} reliability of the global system is 50029 hours. It means that the 10% of the power electronic systems are expected to fail by 5.71 years.

5-3-4 Discussion

Reliability assessment of the conventional DC-DC boost converter has been considered in the previous section. The result demonstrates the B_{10} reliability for the global system containing three critical components, namely IGBT, diode and power capacitor laid between [50029 66680] hours. Based on this method, instead of obtaining an inaccurate reliability value, one can attain an interval for reliability of global system whose useful lifetime undoubtedly lays between the boundaries. In addition to employing Monte Carlo simulation for the consideration of the parameter variations (due to the uncertainties in the APC aging tests), the dependencies of various components have been taken into account because EOPs and TOPs have been considered as i-EOPs and i-TOPs. It means that operating points of power converter in fully degraded case have been also extracted. However, this reliability framework is no capable of assessing the reliability in redundant systems. Although, this method can deal with the simple reliability constructions such as series, parallel and k-out-of-n systems, it is not suitable for reliability evaluation of redundant system such as interleaved power converters. Because in the redundant system, by changing the configuration of the system, the EOP and TOP of the power converter would be varied leading to the different damage model.

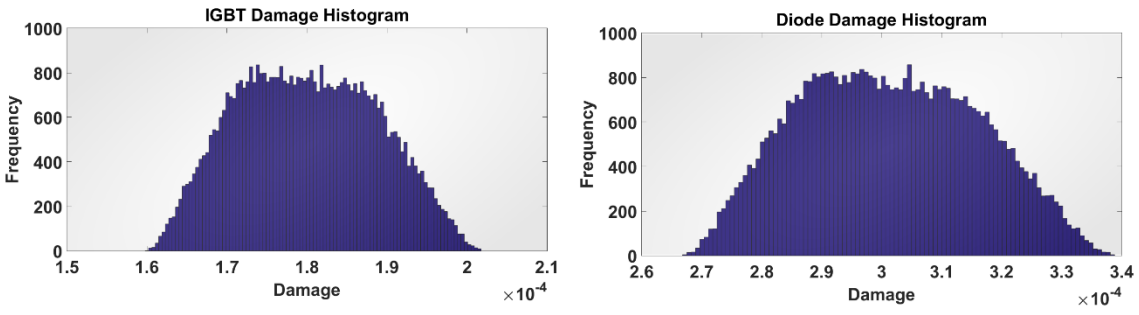


Fig. 5.14. Frequency of damages in IGBT and diode in fully degraded case.

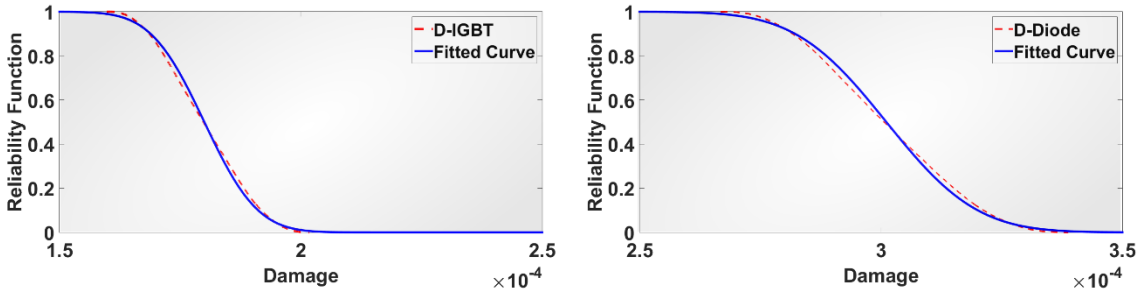


Fig. 5.15. Reliability functions of IGBT and diode damages during one driving cycle in fully degraded case.

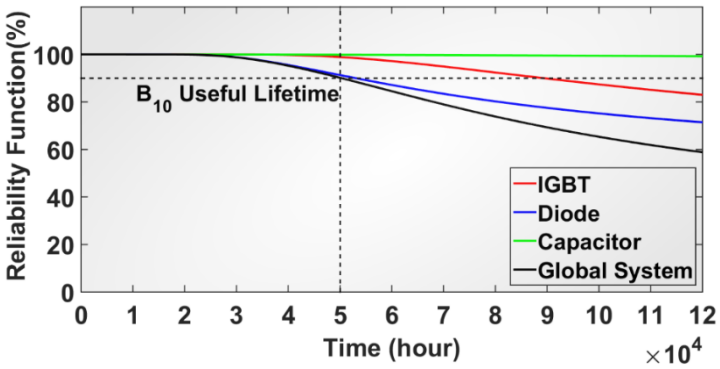


Fig. 5.16. Reliability function of global multi component system, power capacitor.

5-4 Multistate degraded reliability assessment of DC-DC converter

On one side, as the mathematical reliability assessment point of view, this is capable of assessing reliability either in a component- or in a system-level employing some stochastic processes. This means that if a system (power electronic converter as an example) can roughly-appropriate works under a local failure occurrence (one of the components fails during the normal working but the system is well working so far owing to the fault tolerance of system design), the method is still able to assess the reliability. The weakness point of this kind of reliability assessment is absence of mission profile consideration such as temperature cycles and operational cycles. In addition, degradation and wearing out of one component on itself and the other critical components is not taken into account leading to much more optimistic reliability assessment.

On the other side, consideration of the mission profile including both environmental and operational factors is one of the notable point of PoF based reliability assessment leading to much more realistic reliability estimation of a component. In addition, the wearing out of a component is also taken into account. However, in addition to its high cost and being time consuming, the detriment of this method as well as mathematical approach is the lack of consideration of mutual and self-degradation effects on itself and each other. The weakest point of this method is that

it is restricted to the only component level reliability assessment. Thus, in the tolerant system in which a system can also work after a failure occurrence in a sole component, this method is not able to estimate system level reliability assessment. It is clear that by time passing the degradation process of a component or a system might be accelerated owing to aging. Accordingly, static reliability assessment has not been able to estimate the reliability of a system and some dynamic reliability assessments seem to be required [253], [254]. For mitigating the problem of system-level reliability assessment, consideration of self and mutual degradation effects and consideration of degradation level (state), many studies have been undertaken [255]–[259]. However, they have not considered the mission profile in their reliability evaluation.

A Markov model for a continuously operating component with degradation, and Poisson failures was proposed by Sim & Endrenyi [255]. In this study, the distribution of the inter-arrival between consecutive deterioration states was considered to be exponentially distributed. Some researchers investigated the development of reliability models in such a way to take account self-deterioration [256]–[259]. For example, a combined model was discussed based on the two different subsystems in which one is allocated to the catastrophic failure and the other is allocated to degradation process [256]. Generalized Stochastic Petri Nets based model was also proposed in [257]. Xue & Yang [258] developed the reliability model of the multi-state degradation systems based on the continuous-time Markov process, and semi-Markov Process. However, some earlier mentioned problems such as lack of mission profile consideration is evident leading to much optimistic reliability evaluation.

Many dynamic reliability assessments have been developed for evaluating the reliability and performance of a variety of multistate systems in a computationally efficient behavior such as the stochastic processes [260], the extended decision diagram-based methods [261], the universal generating functions (UGFs) [262], the simulation-based methods [263] and the recursive algorithms [264]. The other information such as deteriorating processes [265] and internal and external covariates such as stress and environmental factors [266] have been also used to dynamically update the reliability models of a specific multi state system. Furthermore, owing to ability of estimating reliability based on residual useful lifetime, many studies focusing on remaining useful life estimation have been also viewed as the paradigm of dynamic reliability [267], [268].

In this section, for integrating the pros of both mathematical and physical methods and also tackling their detriments such as system-level reliability assessment, consideration of self and mutual degradation effects and consideration of degradation level (state), a new reliability assessment approach is proposed. In the proposed method, mission profile of undertaken system has been considered as

shown in Fig. 5-17. Translated Mission profile has been applied to the rain flow algorithm to sort the complex data to the understandable data. The sorted data also applied to the lifetime model of an item. The output of lifetime model is one or more failure indicators. The trends of failure indicators have been curve-fitted as a function of mission profile period of time and finally applied to the main multistate degraded system reliability assessment. Based on the failure criterion of each item and their corresponded degradation level, a state for the system will be defined. Accordingly, multistate system is defined based on the items' degradation states.

This section comes up with a new opened-up reliability assessment framework and demonstrates the feasibility of using multistate degraded system analysis for attaining much more accuracy in the reliability evaluation. The proposed method is capable of estimating system-level reliability, while mission profile and physics of failure of the system's items are taken into account. In addition, the self and mutual degradation effects of items on the operation of the global system have been considered. The multi-state degraded system reliability model exposed to multiple failure processes has been generalized. The operating condition of the global system is defined by a finite number of states. Not only does the proposed framework can be employed in determining the reliability of the degraded systems in terms of multi-state functions, but also obtains the states of the systems by estimating the system state probabilities.

5-4-1 Multistate degraded systems

5-4-1-1 System description

A system can be constituted by several subsystems or items in which they are exposed to various failure processes. In a reliability point of view, some important issues have to be considered and are described as follows: 1) the degradation of every item does not follow a constant trend (constant failure rate) due to the wearing out manner which is also accelerated by aging, 2) the degradations of different items can affect the degradation process of the other items by changing the operational point of the considered system and 3) mission profile does play a central role on the wearing out behavior of the items. Accordingly, the degradation trends (process) of the items have to be considered based on the mission profile which the system/items are exposed to. In addition, by dividing different system degraded states (new operational points), the effect of mutual and self-degradations of the items in the system will be considered.

The degradation process of some items are considered as a function of time and denoted by $Y_i(t)$, i=1, 2, …, k. These degradation processes are directly affecting the system reliability by changing its operating point. Hereafter, they have been called effective items. However in some cases, the degradation of some items do not affect the system operating point (system state).

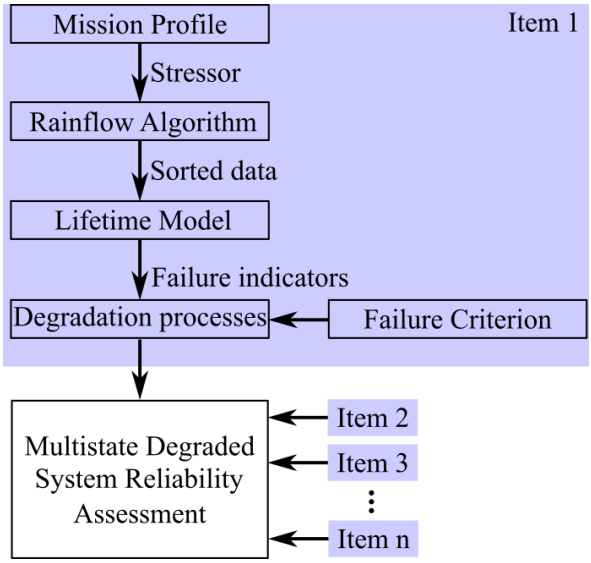


Fig. 5-17. Global flowchart of reliability assessment of n-component system

Hereafter, they have been called ineffective items. Therefore, there is no need of considering degradation processes and only their complete failures (D_{ℓ} (t), j=1, 2, …, ℓ) can affect system's failure. k and ℓ are the number of effective and ineffective items, respectively (also k+ℓ=n, where n is the total number of items in the global system).

Since every item is initially in its perfect state (M_i), the global system is also being in its perfect state. By time passing (aging), the items may reach either another degraded state, namely $(M-1)_i$, or system failed state (F). After degradation, the item can go to the other state, namely $(M-2)_i$ or failure state (F). A transition may be occurred from any system states to the failure state whenever an ineffective item fails owing to the random shock which is subjected to.

The degradation process may continue and pass all the aging stages till the last degradation state, i.e. 0_k is reached. If the system reaches the last degradation state, there is an imperfection in the functionality of the system, and the system must be considered as a failure (state 0). Fig. 5-18 demonstrates the system block diagram of the multiple competing degradation processes including effective and ineffective items. In Fig. 5-18, the above part presents the degradation process of effective items (components) and the bottom part presents the degradation process of ineffective items. While ineffective items may directly lead to catastrophic failure owing to the mission profile they are exposed to, the degradation processes of the effective items may lead an item to transmit from healthier state to either the more degraded states or the catastrophic failure state. Although the system can continue working during the degraded states, the system does not work in the perfect state. Thereby, some imperfect states have to be defined for the system as shown in Fig. 5-18. Various combinations of imperfect states of the items may make a common or different imperfect states for the global system.

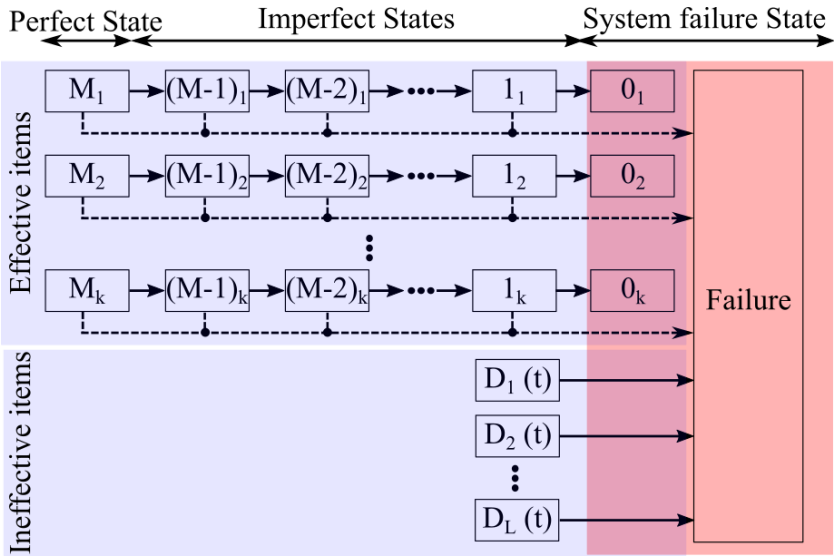


Fig. 5-18. Block diagram of the n-component system subjected to multiple failure processes.

5-4-1-2 Method assumptions

Some assumptions in formulating this newly proposed method have been defined as follows:

1. The system consists of M+2 states in which state 0 and state F are both complete failure states. State 0 represents that the degradation threshold has been exceeded and state F demonstrates a complete (catastrophic) failure occurred by ineffective items or sudden defects in the effective items as shown in Fig. 5-18. State P_i is an intermediate degradation state in the i^{th} effective item and lays on $1<P_i<M_i$.
2. It is assumed that there is no repair and maintenance performing on the system (system is non-repairable).

3. It is assumed that degradation processes of effective items, i.e. $Y_i(t)$, are nonnegative and strictly non-decreasing functions at time t owing to the irreversible accumulation of damages.
4. It is assumed that $Y_i(t)$, i=1, 2, …, k and $D_j(t)$, j=1, 2, …, ℓ are statistically independent. It means that the degradation process of one item in its specific state does not have an effect on the others.
5. The system is in the perfect state at time t=0.
6. The system may fail either owing to the each effective degradation process, i.e. $Y_i(t)>G_i$, i=1, 2, …, k or owing to each ineffective degradation process, e.g. $D_j(t;\eta,\beta)\sim W_j(\eta,\beta)>B_{sj}$, j=1, 2, …, ℓ. where G_i and S_j are the critical values for effective degradation processes and threshold values in which the probability of failure process will reach a specified point (S_j) for ineffective items, respectively.
7. The critical value G_i depends upon the function of intermediate degradation states of the system.

5-4-1-3 Methodology

Degradation paths (processes) are assumed to be modeled by some continuous probabilistic functions. System state space of $\boldsymbol{\Omega_U}$ is defined due to the finite number of operating conditions. Firstly, a generic discrete continuous process has to be defined for giving a set to each effective degradation process. In step 1, a procedure will be discussed for forcing to discrete the effective degradation processes to obtain $\boldsymbol{\Omega_i}$, i=0, 1, …, k. After obtaining the degradation process state space $\boldsymbol{\Omega_i}$, in Step 2, a methodology will be formulated to establish a relation among the system state space $\boldsymbol{\Omega_U}$ and effective and ineffective state spaces as $\{\boldsymbol{\Omega_i}, F\}$ in which F corresponded to the catastrophic failure occurrence.

5-4-1-3-1 Formulating effective degradation processes in terms of discrete state space sets

k effective degradation processes have been considered here. For each of them, a finite number of different discrete states has been also taken into account. The state space is denoted by $\boldsymbol{\Omega_i}=\{M_i, (M-1)_i, \ldots, 1_i, 0_i\}$, i=1, 2, …, k corresponding to the degradation process i with M_i+1 states. M_i, i=1, 2, …, k may or may not be the same and $M_i<\infty$.

Degradation processes are defined by the finite number of states. As an example, $Y_i(t)$ falls into predefined intervals corresponded to the specified intermediate degradation states. Let define the intervals as follows: $[0, W_{Mi}]$, $(W_{Mi}, W_{(M-1)i}]$, …, $(W_{2i}, W_{1i}]$ where $W_{Mi}>W_{(M-1)i}>W_{(M-2)i}>\ldots> W_{1i}$ as shown in Fig. 5-19. Fig. 5-19 demonstrates a sample degradation trend. As it is clearly observed, the degradation trend follows an accelerated strict-increasing pattern. Intervals are respectively corresponding to the intermediate degradation states as M_i, $(M-1)_i$, …, 1_i, 0_i.

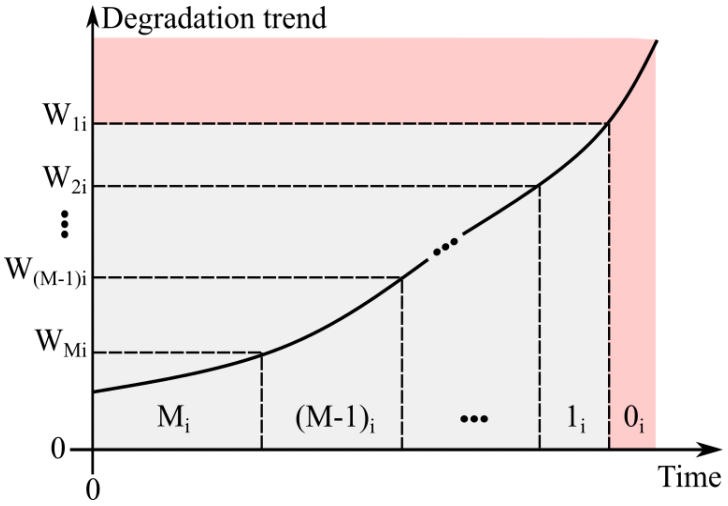


Fig. 5-19. Degradation process of an effective item.

Mathematically, one can find the relationship between degradation process states and their corresponding intervals as expressed in equation (5-16) as follows:

$$\begin{array}{lcl} \text{Effective degradation process} & & \text{State} \\ 0 < Y_i(t) \le W_{Mi} & \Rightarrow & M_i \\ W_{Mi} < Y_i(t) \le W_{(M-1)i} & \Rightarrow & (M-1)_i \\ \vdots & & \\ W_{2i} < Y_i(t) \le W_{1i} & \Rightarrow & 1_i \\ G_i = W_{1i} < Y_i(t) & \Rightarrow & 0_i \end{array} \qquad (5\text{-}16)$$

5-4-1-3-2 System State Space

System state space is defined as $\boldsymbol{\Omega_U}$={M, …, 1, 0, F} consisting in M+2 distinct states. In this section, a relationship between the effective degradation processes {$\boldsymbol{\Omega_i}$, F}, i=0, 1, …, k and the global system state space $\boldsymbol{\Omega_U}$ will be established. Assume that at the time t, the system is not in its catastrophic failure state (F). Accordingly, one can cross out the state F from global system state space. Thus, a correlation between $\boldsymbol{\Omega}$ and $\boldsymbol{\Omega_i}$ is required instead of a correlation between $\boldsymbol{\Omega_U}$ and {$\boldsymbol{\Omega_i}$, F}, i=0, 1, …, k.

A mapping function has to be defined for relating these two different sets as f: $\mathbb{R}=\boldsymbol{\Omega_1\times\Omega_2\times\ldots\times\Omega_k}\rightarrow\ \boldsymbol{\Omega}$={M, M-1, …, 1, 0} where $\mathbb{R}=\boldsymbol{\Omega_1\times\Omega_2\times\ldots\times\Omega_k}=\{(i_1,i_2,\ldots,i_k)|\ i_1\in\boldsymbol{\Omega_1},i_2\in\boldsymbol{\Omega_2},\ldots,\ i_k\in\boldsymbol{\Omega_k}\}$ is a Cartesian product as the input space domain, and shown in Fig. 5-20. The domain and the range of the mapping function has been indicated in Fig. 50-20a. H_c is the mapping matrix with the dimensions of $(M_1+1)\times(M_2+1)\times\ldots\times(M_k+1)$ in which M_i is the number of probable states for the i^{th} effective item and i=0,1, …, k. For example for k=3, a 3 dimensional mapping matrix is required. Thereby, the first item constitutes the rows of the mapping matrix, the second one constitutes the columns and the third one constitutes the pages of the matrix as shown in Fig. 5-20b. Mapping matrix of H_c has mapped the different input states to the specific output global states containing M+1 distinct states.

While different rows of mapping matrix H_c are allocated to different intermediate degradation states of the first item, different columns and pages are allocated to the second and the third items, respectively. The elements of H_c represent $f(i_1,i_2,\ldots,i_k)=P$ in which $i_1\in\boldsymbol{\Omega_1}$, $i_2\in\boldsymbol{\Omega_2}$,…, $i_k\in\boldsymbol{\Omega_k}$ and $P\in${ M-1, M-2, …, 1}. Regarding Fig. 5-20b, the first elements of mapping matrix H_c in whole the matrix pages and the first column and the first row of the first mapping matrix page as well have been demonstrated by ×. These elements are not achievable, because if one of the items reaches its failure state (0_i), the system stops working and necessarily the others cannot reach their failure states as well. All the other elements in the first page in which the third item is in its failure state (0_3) are equal to zero. In addition, for all the matrix pages, the first rows and the first columns (except the first element) are also zero due to the zero states of the first and the second items degradation states. The last element of

mapping matrix H_c is the perfect state of the global system (M) in which the system is initially in it because all the effective items are in their healthy (perfect) states. The other elements in H_c are imperfect states belonging to the global state space **Ω** except M, namely global system perfect state. Some other elements also may be considered zero when the items are in their low states. It means that in the states in which some of the effective items are roughly degraded, one can define those states as the global degraded states.

Time-to-failure of the global system is defined as follows:

$$T = \inf\{t : Y_i(t) > G_i, i = 1,2,\ldots,k \ \text{ or } \ F_j > B_{S_j}, j = 1,2,\ldots,\ell\} \qquad (5\text{-}17)$$

All the degradation processes including effective and ineffective items are competing in the reliability of the global system. However, the global system will be failed provided that the only one of the degradation processes exceeds its critical value. Accordingly for all combinations of $Y_i(t)$, i=1,2,..., k and also for all combinations of $D_j(t)$, j=1,2,..., ℓ, following events never occurred:

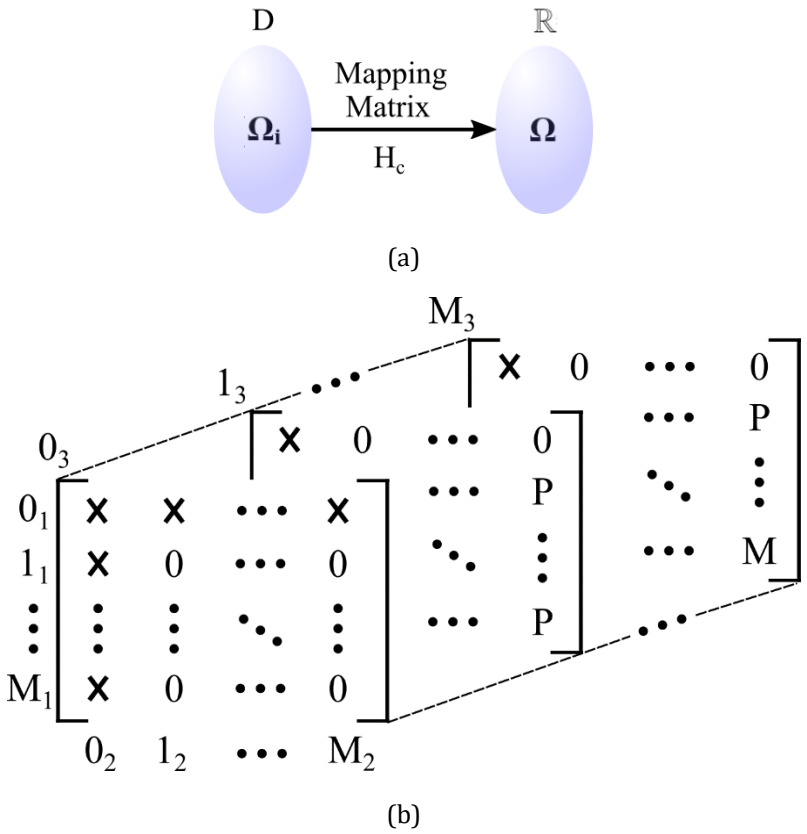


Fig. 5-20. Mapping matrix. a) Each state of effective items is allocated to a specific global system state, b) Three-item mapping matrix H_c where P∈**Ω**={M-1, M-2, ..., 1}.

$$P\left\{\begin{array}{l} Y_i(t) > G_i, \forall \bigcup_{ii=1}^{k,ii\neq i} Y_{ii}(t) \,|\, i = 1,2,...,k, \\ D_j(t) < B(S_j) \,|\, j = 1,2,...,l \end{array}\right\} = 0$$

$$P\left\{\begin{array}{l} Y_i(t) < G_i \,|\, i = 1,2,...,k, \\ D_j(t) > B(S_j), \forall \bigcup_{jj=1}^{k,jj\neq j} D_{jj}(t) \,|\, j = 1,2,...,l \end{array}\right\} = 0 \qquad (5\text{-}18)$$

$$P\left\{\begin{array}{l} Y_i(t) > G_i, \forall \bigcup_{ii=1}^{k,ii\neq i} Y_{ii}(t) \,|\, i = 1,2,...,k, \\ D_j(t) > B(S_j), \forall \bigcup_{jj=1}^{k,jj\neq j} D_{jj}(t) \,|\, j = 1,2,...,l \end{array}\right\} = 0$$

The function f: $\mathbb{R}= \boldsymbol{\Omega_1 \times \Omega_2 \times \ldots \times \Omega_k} \rightarrow \boldsymbol{\Omega}=\{M, M\text{-}1, \ldots, 1, 0\}$ has to meet the following requirements.

1. $f(M_1, M_2, \ldots, M_k)=M$ and $f(0_1, a_2, \ldots, a_k) = f(a_1, 0_2, \ldots, a_k)= f(a_1, a_2, \ldots, 0_k)= 0$ where $a_i \in \boldsymbol{\Omega_i}$, i=1, 2, ..., k.
2. f is a monotonic strictly non-decreasing function for each argument. For example,

$$\begin{array}{l} f(a_1, a_2, \ldots, a_k) \geq f(b_1, a_2, \ldots, a_k) \quad \text{if } a_1 \geq b_1 \\ f(a_1, a_2, \ldots, a_k) \geq f(a_1, b_2, \ldots, a_k) \quad \text{if } a_2 \geq b_2 \\ \qquad\qquad \vdots \\ f(a_1, a_2, \ldots, a_k) \geq f(a_1, a_2, \ldots, b_k) \quad \text{if } a_k \geq b_k \end{array} \qquad (5\text{-}19)$$

In real applications, different degradation state combinations can generate the same outputs. Thereby, in the mapping matrix H_c, there may be the same outputs in the different elements. The following definition has to be considered for explaining this similarity in the mapping matrix.

Definition. The i^{th} equivalent category R_i is defined as

$$R_m = \left\{\begin{array}{l} (a_1, a_2, \ldots, a_k) \text{ where } a_1 \in \boldsymbol{\Omega}_1, a_2 \in \boldsymbol{\Omega}_2 \\ \ldots, a_k \in \boldsymbol{\Omega}_k \,|\, f(a_1, a_2, \ldots, a_k) = m \end{array}\right\}, m = 0,1,\ldots,M \qquad (5\text{-}20)$$

where R_m demonstrates all the possible degradation state combinations which generate the global system state m and R_0 to R_M are the distinct subsets dividing R to the M+1 equivalent categories, so that

$$R = \bigcup_{m=0}^{M} R_i \qquad (5\text{-}21)$$

5-4-1-4 Reliability Assessment

In this section, the probability density function and mean time to failure will be obtained on the state probabilities mentioned in previous section. Initially, the

global system is considered to be in its perfect state, i.e. M=f(R_M). The probability of being in state M yields by

$$P_t(M) = P_t(f(R_M)) \tag{5-22}$$

As defined, R_m illustrates all possible degradation state combinations leading to the global system state of m. The probability of being in state m yields by

$$P_t(m) = P(f(R_m)) \tag{5-23}$$

The probability of catastrophic failure state (F) is evaluated by

$$P_t(F) = P\left\{ Y_i(t) \le G_i \mid i = 1, 2, \ldots, k,\ \ D_j(t) \ge B(S_j) \mid j = 1, 2, \ldots, l \right\} \tag{5-24}$$

System reliability R(t) can be assessed by:

$$\begin{aligned} R(t) &= P\{\text{global system state} \ge 1\} \\ &= \bigcup_{m=1}^{M} P\{f(R_m)\} \\ &= \sum_{m=1}^{M} P_t(m) \end{aligned} \tag{5-25}$$

where $P_t(m)$ is the probability of being in the global system state of m.

Assume T as a continuous random variable of mean time to failure. One can calculate the mean time to failure as follows:

$$\begin{aligned} E[T] &= \int_0^{\infty} P\{T > t\}\, dt \\ &= \int_0^{\infty} \prod_{i=1}^{k} P\{Y_i(t) \le G_i\} \times \prod_{j=1}^{\ell} \left(F_j(\eta, \beta) < B(S_j) \right) dt \end{aligned} \tag{5-26}$$

The results in (5-26) would significantly depend on the $\prod_{i=1}^{k} P\{Y_i(t) \le G_i\}$.

5-4-2 DC-DC Boost converter reliability assessment based on the multistate degraded reliability assessment

In this section, we consider a DC-DC boost converter containing various components individually confronted to the different failure mechanisms. Every component has effects on the system operating conditions during its working (see Chapter 3). It has been proved that the components' degradations can extensively be effective in the power electronic systems' operating points (see section 3-4). A DC-DC boost converter contains IGBT, diode and capacitor which each of them is sensitive to the various failure mechanisms leading to aging (parameter drifting).

In addition, it is notable that power semiconductors' degradations, namely either thermally or electrically, can strongly effect the power electronic systems' electrical and thermal operating points. It was illustrated in section 3-5 that the junction

temperature of insulated-gate bipolar transistor (IGBT) was increased from 140.3°C to 170.5°C during the aging which affected significantly the operating points of converter. However, it was not the case in the power capacitor's degradation. By capacitor aging, its parameters were considerably varied. But, these parameters drifting did not lead to a change in converter's operating points. Although, reliability of power capacitors, thereby, will be considered here, power capacitors' failure mechanisms are beyond this study and the interested readers referred to [30].

Power semiconductors are exposed to the different thermal cycling owing to their power losses made in the chip junction. A repetitive set of shear and normal stresses either in elastic and plastic regions of materials are induced in power semiconductors by electro-thermo-mechanical behaviors of devices. These stresses are led to elastic and plastic strains occurrence in the materials and eventually lead to produce fatigue phenomenon along with the materials of power semiconductors. Eventually, these kinds of deformations gradually either produce some micro cracks and micro voids or grow pre-induced micro cracks and micro voids. After a large number of cyclic stresses, material may be fatigued due to the voids coalescence and cracks growth. Fatigue can influence the health of power semiconductors such as IGBT. Micro cracks production and growth as well as voids creation and coalescence can affect the performance of any parts of packaging in a discrete power chip comprising bonding wires, aluminum metallization, die attach to the baseplate, etc.

It was shown that the thermal resistance ($R_{th(j\text{-}c)}$) increased in the power semiconductors and can affect device performance significantly during its aging (Section 3-2). It was shown in equation (3-4) that thermal resistance degradation may follow Coffin-Manson-Arrhenius lifetime model as follows:

$$\Delta R_{th} = K\left\{\exp\left(\frac{N}{A\times\Delta T_j^{\alpha}\times\exp\left(Q/RT_m\right)}\right)-1\right\} \qquad (5\text{-}27)$$

The deterioration trends of thermal resistances, in IGBT and diode, have been shown in Fig. 3-10. This figure demonstrates the deterioration trends of thermal resistance of diode and IGBT in terms of thermal cycles. For multi states reliability assessment, time-dependent degradation process has been required. Accordingly, based on the cumulative damage model, one can obtain deterioration of IGBT and diode as functions of time describing in the next section.

A DC-DC boost converter containing two critical effective components, namely IGBT and diode, and one critical ineffective component, namely power capacitor, has been assumed. This converter is assumed to be employed as an interface between the battery bank and the electric motor of a hybrid electric vehicle. There are three distinct items as the system reliability point of view in which the system would be failed provided that one of these items is being failed.

Mission profile play a major role on the wearing out behavior of these items. Accordingly, the degradation trends of the items have to be considered based on the mission profile which the system/items are exposed to.

The degradation processes of IGBT and power diode are considered as functions of time and denoted by $Y_1(t)$ and $Y_2(t)$, respectively. Power capacitor is considered as an ineffective item with D(t) time to failure distribution following Weibull damage model ($D(t)\sim W(\eta, \beta)$ where η and β are the scale factor and shape factor, respectively). Degradation processes are assumed to be modeled by some continuous probabilistic functions. In addition, the previously mentioned assumptions are hold in this case.

The converter has two effective degradation processes. For each of them, 5 different discrete states have been also taken into account. Their state spaces are denoted by $\boldsymbol{\Omega_1}=\{4_1, 3_1, 2_1, 1_1, 0_1\}$ and $\boldsymbol{\Omega_2}=\{4_2, 3_2, 2_2, 1_2, 0_2\}$. The perfect states of them are 4_1 and 4_2 and the failure states are 0_1 and 0_2. Accordingly, once either IGBT or power diode reach their zero states, the system is failed.

$Y_1(t)$ and $Y_2(t)$ fall into predefined intervals corresponded to their five intermediate degradation states. Let consider the intervals as follows: [1.15, 1.2075], (1.2075, 1.265], (1.265, 1.3225] and (1.3225, 1.4] K/W and [1.9, 1.995], (1.995, 2.09], (2.09, 2.185] and (2.185, 2.3] K/W for IGBT and power diode, respectively. IGBT (power diode) would be failed whenever it exceeds its failure threshold, i.e. $R_{th\text{-}IGBT}$>1.4 K/W ($R_{th\text{-}diode}$>2.3 K/W). Therefore,

$$
\begin{aligned}
&0 < Y_1(t) \le 1.2075 && \Rightarrow && 4_1\\
&1.2075 < Y_1(t) \le 1.265 && \Rightarrow && 3_1\\
&1.265 < Y_1(t) \le 1.3225 && \Rightarrow && 2_1\\
&1.3225 < Y_1(t) \le 1.4 && \Rightarrow && 1_1\\
&G_1 = 1.4 < Y_1(t) && \Rightarrow && 0_1
\end{aligned}
$$

And (5-28)

$$
\begin{aligned}
&0 < Y_2(t) \le 1.995 && \Rightarrow && 4_2\\
&1.995 < Y_2(t) \le 2.09 && \Rightarrow && 3_2\\
&2.09 < Y_2(t) \le 2.185 && \Rightarrow && 2_2\\
&2.185 < Y_2(t) \le 2.3 && \Rightarrow && 1_2\\
&G_2 = 2.3 < Y_2(t) && \Rightarrow && 0_2
\end{aligned}
$$

The degradation trends of IGBT and power diode in four different conditions have been shown in Fig. 3-10. As it was previously mentioned, these trends have been in terms of thermal cycles while they have to be in terms of time for reliability assessment. Accordingly, WLTP-class3 driving cycle mission profile has been translated from the vehicle speed to the thermal cycling data via power electronic electrical model, power loss model and thermal model. Then this set of complex data

has been inserted to the Rainflow algorithm to be sorted. Finally, this set of sorted data has been applied to the Coffin-Manson-Arrhenius and Monkman-Grant lifetime models (equation (5-2)) for evaluating the degradation processes as functions of time. Based on the aforementioned procedure, one can obtain time-dependent degradation processes of IGBT and power diode as follows using linear interpolation:

$$Y_1(t)=\begin{cases}1.1500+2.246\times10^{-6}t & 0<t<25602\,\text{hours}\\ 1.2075+2.438\times10^{-6}t & 25602<t<49194\,\text{hours}\\ 1.2650+2.562\times10^{-6}t & 49194<t<71634\,\text{hours}\\ 1.3225+2.812\times10^{-6}t & 71634<t<92082\,\text{hours}\end{cases}$$

And (5-29)

$$Y_2(t)=\begin{cases}1.900+7.124\times10^{-6}t & 0<t<13336\,\text{hours}\\ 1.995+7.189\times10^{-6}t & 13336<t<26552\text{hours}\\ 2.090+7.670\times10^{-6}t & 26552<t<38912\,\text{hours}\\ 2.185+7.740\times10^{-6}t & 38912<t<51192\text{hours}\end{cases}$$

Regarding above mentioned equation, one can find the accelerating degradation of power semiconductors, i.e. IGBT and power diode. Each of the constant in equation (5-29) is assumed to be *normally distributed* with 5% variation for considering uncertainty. Fig. 5-21 demonstrates the degradation trends of IGBT and power diode and their corresponding degradation states.

In this case study, power capacitor is considered as an ineffective item with following time to failure distribution [6]:

$$D(t;\eta,\beta)\sim W(1471680,1.93) \qquad (5\text{-}30)$$

System state space is assumed as $\boldsymbol{\Omega}_U$={4, 3, 2, 1, 0, F} consisting 6 distinct states. Assume that at the time t, the system is not in its catastrophic failure state (F). Accordingly, one can assume $\boldsymbol{\Omega}$={4, 3, 2, 1, 0} instead of $\boldsymbol{\Omega}_U$.

$$H_c=\begin{array}{c}\\ 0_1\\ 1_1\\ 2_1\\ 3_1\\ 4_1\end{array}\begin{array}{c}\begin{array}{ccccc}0_2 & 1_2 & 2_2 & 3_2 & 4_2\end{array}\\ \begin{bmatrix}\times & 0 & 0 & 0 & 0\\ 0 & 0 & 1 & 1 & 1\\ 0 & 1 & 2 & 2 & 2\\ 0 & 1 & 2 & 3 & 3\\ 0 & 1 & 2 & 3 & 4\end{bmatrix}\end{array} \qquad (5\text{-}31)$$

Accordingly, one can numerate R as

$$\begin{Bmatrix} (0_1,1_2),(0_1,2_2),(0_1,3_2),(0_1,4_2),(1_1,0_2),(1_1,1_2), \\ (1_1,2_2),(1_1,3_2),(1_1,4_2),(2_1,0_2),(2_1,1_2),(2_1,2_2), \\ (2_1,3_2),(2_1,4_2),(3_1,0_2),(3_1,1_2),(3_1,2_2),(3_1,3_2), \\ (3_1,4_2),(4_1,0_2),(4_1,1_2),(4_1,2_2),(4_1,3_2)(4_1,4_2) \end{Bmatrix} \quad (5\text{-}32)$$

Regarding H_c and the global system state space, there are five different categories as follows

$$\begin{aligned} R_0 &= \begin{Bmatrix} (0_1,1_2),(0_1,2_2),(0_1,3_2),(0_1,4_2),(1_1,0_2), \\ (2_1,0_2),(3_1,0_2),(4_1,0_2),(1_1,1_2) \end{Bmatrix} \\ R_1 &= \{(1_1,2_2),(1_1,3_2),(1_1,4_2),(2_1,1_2),(3_1,1_2),(4_1,1_2)\} \\ R_2 &= \{(2_1,2_2),(2_1,3_2),(2_1,4_2),(3_1,2_2),(3_1,4_2)\} \\ R_3 &= \{(3_1,3_2),(3_1,4_2),(4_1,3_2)\} \\ R_4 &= \{(4_1,4_2)\} \\ R &= \bigcup_{m=0}^{4} R_i \end{aligned} \quad (5\text{-}33)$$

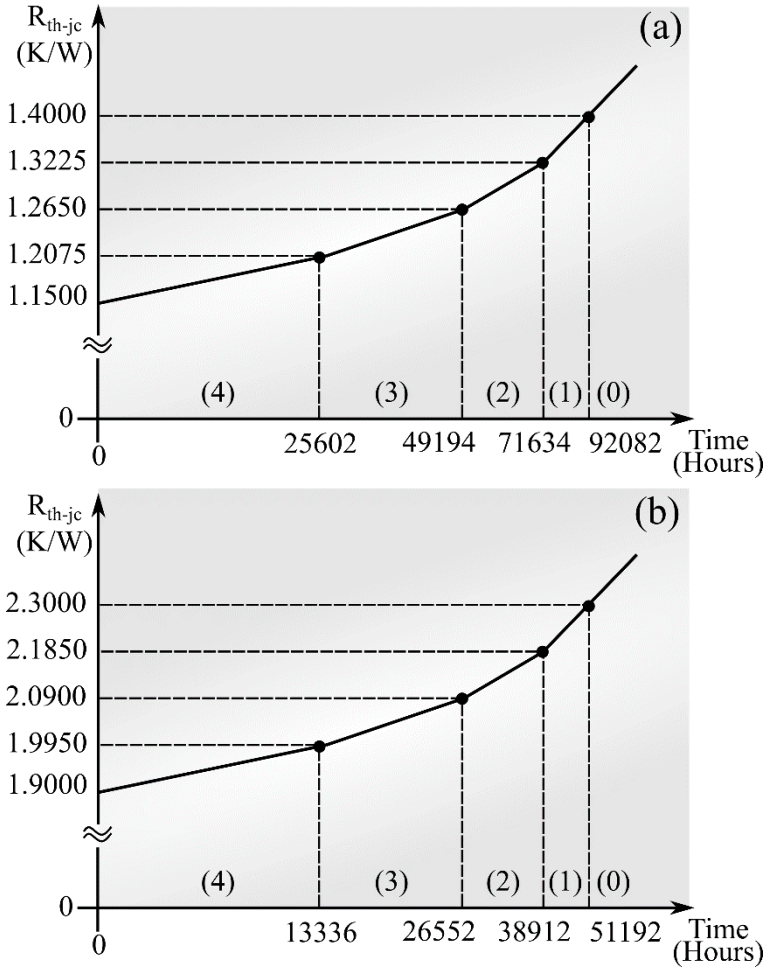


Fig. 5-21. Degradation processes of a) IGBT and b) power diode.

The probability density function and mean time to failure will be obtained on the state probabilities mentioned. The probability of being in state M=4 would be calculated as follows:

$$P_t(4) = P(f(R_4)) = P(0 < Y_1(t) < W_{4_1} \cap 0 < Y_2(t) < W_{4_2}) \times P(D(t) < B_{10}) \quad (5\text{-}34)$$

Since the degradation processes are assumed to be independent, one can find that

$$\begin{aligned} P_t(4) &= P(0 < Y_1(t) < W_{4_1}) \times P(0 < Y_2(t) < W_{4_2}) \\ &= \left\{P(Y_1(t) < W_{4_1}) - P(Y_1(t) < 0)\right\} \times \left\{P(Y_2(t) < W_{4_2}) - P(Y_2(t) < 0)\right\} \times \\ &\quad \left(1 - F(t;\eta,\beta)\right) \end{aligned} \quad (5\text{-}35)$$

Since $Y_i(t)=a_i+b_it$ where $a_i \sim N(\mu_{ai},\sigma_{ai}^2)$ and $b_i \sim N(\mu_{bi},\sigma_{bi}^2)$, $Y_i(t)$ will follow normal distribution as follows:

$$\begin{aligned} &Y_i(t) \sim N(\mu_{ai} + \mu_{bi}t, \sigma_{ai}^2 + t^2\sigma_{bi}^2); \qquad i = 1,2 \\ &\mu_i = \mu_{ai} + \mu_{bi}t \\ &\sigma_i = \sigma_{ai}^2 + t^2\sigma_{bi}^2 \end{aligned} \quad (5\text{-}36)$$

Therefore, one can calculate equation (5-35) as follows:

$$P_t(4) = \Phi\left(\frac{W_{4_1} - \mu_1}{\sigma_1}\right) \times \Phi\left(\frac{W_{4_2} - \mu_2}{\sigma_2}\right) \times \left(1 - F(t;\eta,\beta)\right) \quad (5\text{-}37)$$

The other system states probablities can also be estimated in the same procedure described in (5-34)-(5-37). Fig. 5-22, 23 illustrates the reliability of the different system states. Since the coefficients have been assumed to be normally distributed, the system probability is also normally distributed. The yellow curve is shown the reliability of the global system. 10% unreliability or 90% reliability (B_{10}) is achieved at 58040 hours. Accordingly, the power electronic system may work over 6.5 years with 90% reliability. State 4 is perfect state and has a large share in the reliability of the converter. In each state, capacitor reliability has been also considered and consequently, there is no need to multiply capacitor reliability to the global system reliability.

5-4-3 Discussion

In this section, a new reliability assessment framework has been proposed. Based on this method, operating condition of a system has been characterized by a finite number of degraded states. This leads to the consideration of the dependancy of components' aging on the operating condition which finally leads to much more realistic reliability assessment.

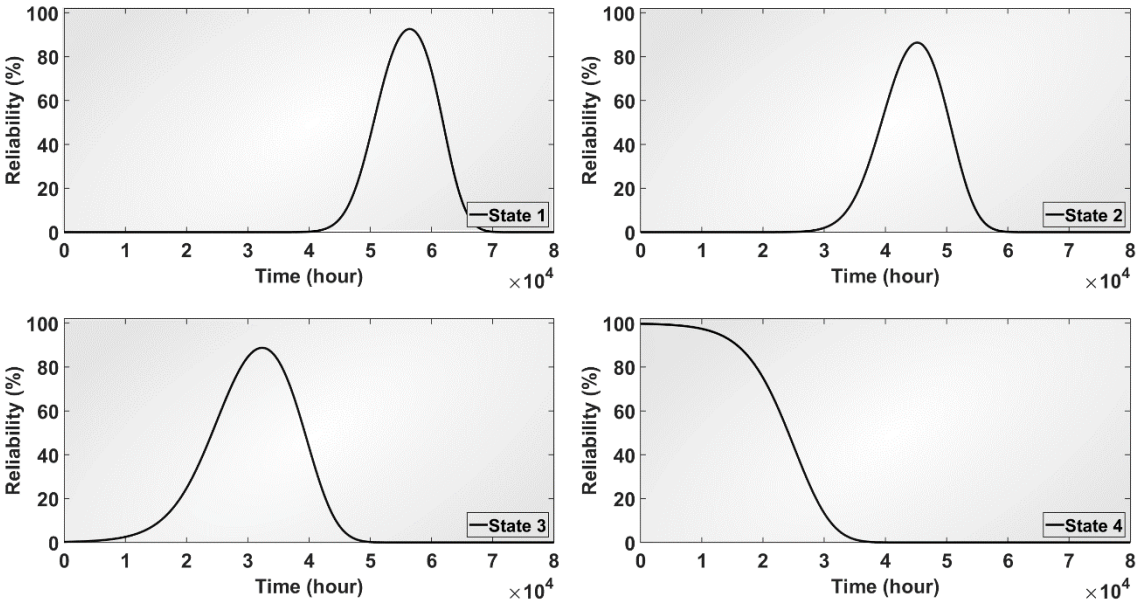


Fig. 5-22. Reliability functions of different states.

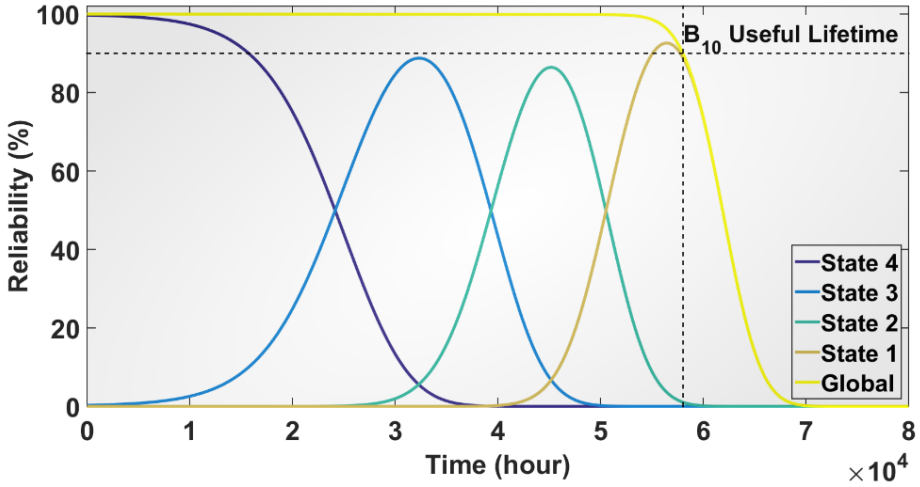


Fig. 5-23. Reliability functions.

The items of a system have been categorized into two different items, effective and ineffective items. Effective items are thoes which directly affect on the operating condition of the system. While, ineffective items do not make meaningful contribution on the operating condition of the system and their failures lead to the catastrophic failure of the system. Degradation processes of the effective items have been extracted from the mission profile based aging tests and have been divided to the several intermediate degraded states. The various combinations of the effective items' states have mapped to the global system states using a mapping matrix.

The proposed framework has been applied to DC-DC boost converter containing two effective components, namely IGBT and diode, and one ineffective item, namely power capacitor. Mission profile based aging tests have been performed to find the

the degradation processes of IGBT and power diode. The results showed that the power electronic system which was exposed to the WLTP-class3 driving cycle might work over 58040 hours by 90% reliability. This framework can be easily applied to a redundant system by suitable defining mapping matrix H_c. Assume that two items are in parallel as a reliability point of view. In a redundant system, one can consider that (0_1,x) and (x,0_2) are not mapped to the 0 state of H_c. In addition to the ability of evaluating the system-level reliability (not multi component level reliability), components' degradations and their effects on the performance of power converter (EOP and TOP) have been applied by considering these degradations on EOP and TOP in every degradation state of the system.

6

Summary and Conclusion

This study was primarily undertaken to evaluate the reliability of DC-DC power converters via a newly proposed algorithm, namely multistate degraded reliability assessment. This approach was launched to overcome some significant difficulties in reliability assessment of power electronic converters. The difficulties were included in lack of consideration of mission profile in the classic (mathematical) reliability, inability to evaluate reliability in the system-level and lack of consideration of mutual- and self-degradation effects (dependencies) of components in the system (do not consider the effects of components degradations on the global system operating point).

Chapter one dealt with an overview of previous studies and introduced potential failure mechanisms in the critical power electronic components i.e. power semiconductors and power capacitors. It revealed that among all components, capacitors and power semiconductors played major roles in the healthy working of power electronic converters. Power semiconductors (discrete chips) and power capacitors encountered creep-fatigue and electrochemical reaction failure mechanisms during their performances, respectively. Physics of failures were discussed and their lifetime and damage models based on the literature and physical and empirical aspects were launched.

Electrical, power loss and thermal models were investigated in Chapter two. Electrical modeling was based on time invariant multi frequency model in which electrical behaviors of a DC-DC boost power converter were precisely extracted according to the high-order modeling of TIMF. While power loss modeling was carried out based on the conventional modeling, a complete thermal modeling of the considered power converter was also discussed based on the analytic and the simulating approaches.

The experimental procedure was discussed in Chapter three. In this chapter, the procedure of performing accelerated thermal and power cycling tests were introduced. The results were used in the proposed reliability assessment frameworks of power converter. A customized DC-DC boost power converter capable of real time measuring of junction temperature was also implemented to

investigate the mutual- and self-degradations effects. The results revealed the importance and effects of dependencies in the considered power converter.

A modified Rainflow algorithm capable of simultaneously creep-fatigue cycle counting and considering time-temperature-dependent mean temperature was proposed in Chapter Four. This algorithm was employed to cycle counting of considered mission profile in the reliability assessment.

Multistate degraded reliability assessment was put forward to tackle above-mentioned issues by dividing a time-reliability-dependent system to some independent subsystems in Chapter five. The approach was trying to solve the dependency issues by defining some intermediate degradation intervals. Instead of assuming a system being only in a perfect state or in a failure state, a system by some intermediate degradation states (imperfect states) was defined. The imperfect states of the system were led by imperfect components states. The approach divided the components into two different categories, namely effective and ineffective components. Ineffective components were those their degradations could not affect the system operating points, while effective ones were said to be effective in the global system operating points. Since the reliability of a converter is operating point dependent, the effective items might directly affect the reliability of power converters.

The combination of various imperfect components states might lead to the unique imperfect global system states. The relationships among the components degradation states and the system states were mapped using a mapping matrix called H_c. The dimensions of this matrix depended on the number of effective components which were included in the global system. The number of rows, columns and pages were directly determined by the number of components individual degradation states. The more imperfect states considered for the components, the more accurate evaluation of reliability assessed and the more time would be consumed.

Degradation processes of individual components were assumed as probabilistic distributions for taking into account the uncertainties in the estimation. Degradation processes of individual components might be any functions of time and extracted from experimental aging tests. Some threshold values were defined for distinguishing the imperfect states of individual components. By time passing (aging), the degradation processes were passing from a healthier state to the less healthy states which made the global system be in the new imperfect state. Since, the damages were assumed to be cumulative and irreversible, the degradation states were alternated only from healthier states to the less healthy states and not vice versa.

The degradation processes of ineffective components might have any kind of probabilistic distributions with the random variable of time to failure. Ineffective components made the global system transmit directly from the perfect state to the failure state without passing through the degradation states.

As a case study, a conventional DC-DC boost power converter was under studied. This converter included active switches, capacitor and inductor. Since the most critical components in the reliability assessment of power converters are capacitor and active switches, RBD of the system was assumed to have only three components, namely an IGBT, diode and capacitor. An experiment had been designed and implemented for investigating on the dependencies of degradations of individual components on the TOP and EOP of the global system in a customized DC-DC boost power converter. The results revealed that IGBT and diode had direct effects on the thermal and electrical operating points of the global system. In addition, there were also self- and mutual- degradation effects on the performance of IGBT and diode leading to much more accelerated aging. Accordingly, two effective components, namely IGBT and diode, and one ineffective component i.e. capacitor were assumed in the reliability evaluation of the global system (conventional DC-DC boost power converter).

Capacitor failure (20% decrease in its capacitance or 100% increase in its ESR) directly led to the system failure, while power semiconductors degradation processes resulted to the different imperfect global system states. Five distinct degradation states were defined for the IGBT and diode in which their thermal resistances were increased by 5% till reached the failure criteria (20% increase in junction to case thermal resistance). State 4 to 0 degradation trends were occurred whenever the thermal resistance of IGBT or diode between (1, 1.05], [1.05, 1.1), [1.1, 1.15), [1.15, 2] and greater than 1.2, respectively. The degradation processes of IGBT and diode were extracted from the APC and ATC aging tests. APC and ATC results revealed the degradation trends of IGBT and diode in terms of number of cycles. For converting the number of cycles to the time, a driving cycle, namely WLTP-class3, with various cycles with period of 30 min was applied to the APC and ATC aging test results. This conversion led to find the degradation processes of IGBT and diode in terms of time. The data was piecewise linear functions for both IGBT and diode in which the slope of these piecewise linear functions were strictly increasing due to the irreversibility of damage.

The B_{10} reliability result was estimated 58040 hours for the global power electronic system. It means that the DC-DC boost power converter might work with 90% probability of well-working for 58040 hours. While, as conventional reliability assessment frame work, the B_{10} reliability was 66680 hours. It reveals that the conventional approach (which is not capable of system-level reliability assessment) is too optimistic owing to lack of consideration self- and mutual degradation effects.

Not only the newly proposed reliability assessment framework is a systematic approach and capable of applying to the various power electronic converters, but also it tackles the detriments of conventional frameworks by considering mission profile and mutual and self-degradation effects on the performance of power converter leading to much more accurate and realistic assessment. There is still one remaining open problem associated with the proposed algorithm. In the systems with a large number of critical components, mapping matrix size will be increased. Furthermore, mapping matrix size can also be increased by increasing the number of global's and components' states in order to reach a higher accuracy. The larger the size of mapping matrix, the higher accuracy obtained and the more consuming time for the reliability evaluation. Therefore, an optimization algorithm as a preprocess algorithm for the newly proposed reliability assessment framework between the reliability evaluation accuracy and required consuming time seems to be proposed.

Bibliography

[1] P. O'Connor and A. Kleyner, *Practical reliability engineering*. John Wiley & Sons, 2012.

[2] M. Bâzu and T. Băjenescu, *Failure Analysis: A Practical Guide for Manufacturers of Electronic Components and Systems*. 2011.

[3] M. Rausand and A. Høyland, *System reliability theory: models, statistical methods, and applications*, vol. 396. John Wiley & Sons, 2004.

[4] P. Viswanadham and P. Singh, *Failure Modes and Mechanisms in Electronic Packages*, vol. 53. 1998.

[5] F. R. Nash, *Estimating Device Reliability: Assessment of Credibility (The Springer International Series in Engineering and Computer Science)*. Kluwer Academic New York, NY, USA, 1993.

[6] W. Denson, "The History of Reliability Prediction," *IEEE Trans. Reliab.*, vol. 47, no. 3, p. sp-321-sp-328, 1998.

[7] M. S. Handbook, "MIL-HDBK-217F," *Reliab. Predict. Electron. Equipment, US Dep. Def.*, 1995.

[8] J. Vigen and O. No, "IEC TR 62380 - Reliability data handbook - Universal model for reliability prediction of electronic components," vol. 2004, 2005.

[9] M. Pecht, D. Das, and A. Ramakrishnan, "The IEEE standards on reliability program and reliability prediction methods for electronic equipment," *Microelectron. Reliab.*, vol. 42, no. 9–11, pp. 1259–1266, 2002.

[10] J. G. McLeish, "Enhancing MIL-HDBK-217 reliability predictions with physics of failure methods," in *Reliability and Maintainability Symposium (RAMS), 2010 Proceedings-Annual*, 2010, pp. 1–6.

[11] E. Moreau, "FIDES Guide 2004 issue A Reliability Methodology for Electronic Systems," *Technology*, pp. 1–347, 2004.

[12] S. Harb and R. S. Balog, "Reliability of candidate photovoltaic module-integrated-inverter (PV-MII) topologies—A usage model approach," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 3019–3027, 2013.

[13] K. Choudhary and P. Sidharthan, "Reliability prediction of Electronic Power Conditioner (EPC) using MIL-HDBK-217 based parts count method," *IEEE Int. Conf. Comput. Commun. Control. IC4 2015*, no. 1, pp. 2–5, 2016.

[14] B. B. Fong and C. K. Li, "Methods for Assessing Product Reliability," no. January 2012, pp. 43–48, 2011.

[15] Y. S. Thakur and D. K. Sakravdia, "Reliability Prediction Methods for Electronic Devices and Systems- A Review," vol. 13, no. 17, pp. 13063–13069, 2018.

[16] M. Catelani *et al.*, "Reliability analysis and electrical characterization of a Class-E resonant inverter," *I2MTC 2018 - 2018 IEEE Int. Instrum. Meas. Technol. Conf. Discov. New Horizons Instrum. Meas. Proc.*, pp. 1–6, 2018.

[17] M. Talmor and S. Reliability, "System Reliability Estimation with Failure Modes Analysis Applying Bayesian Approach - Case Study," *2018 Annu. Reliab. Maintainab. Symp.*, pp. 1–6.

[18] N. Li, G. Tong, J. Yang, G. Sun, and D. Han, "Reliability Prediction Approaches For Domestic Intelligent Electric Energy Meter Based on IEC62380 Reliability Prediction Approaches For Domestic Intelligent Electric Energy Meter Based on IEC62380," 2018.

[19] N. Shahidirad, M. Niroomand, and R. A. Hooshmand, "Investigation of PV Power Plant Structures Based on Monte Carlo Reliability and Economic Analysis," *IEEE J. Photovoltaics*, vol. 8, no. 3, pp. 825–833, 2018.

[20] S. E. De Léon-Aldaco, H. Calleja, F. Chan, and H. R. Jiḿenez-Grajales, "Effect of the mission profile on the reliability of a power converter aimed at photovoltaic applications-A case study," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2998–3007, 2013.

[21] S. E. De Leon-Aldaco, H. Calleja, and J. Aguayo Alquicira, "Reliability and mission profiles of photovoltaic systems: A FIDES approach," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2578–2586, 2015.

[22] H. Y. Go, S.-I. Sung, and Y. S. Kim, "Prediction of system reliability using failure types of components based on Weibull lifetime distribution," *J. Mech. Sci. Technol.*, vol. 32, no. 6, pp. 2463–2471, 2018.

[23] S. De León Aldaco, H. Calleja, and J. Mina, "Converter reliability optimization based on mission profile," *2015 IEEE 6th Int. Symp. Power Electron. Distrib. Gener. Syst. PEDG 2015*, no. 2, 2015.

[24] M. White and J. B. Bernstein, "Microelectronics reliability: physics-of-failure based modeling and lifetime evaluation," *JPL Publ.*, pp. 1–216, 2008.

[25] P. Charpenel *et al.*, "The right way to assess electronic system reliability: FIDES," *Microelectron. Reliab.*, vol. 43, no. 9–11, pp. 1401–1404, 2003.

[26] S. Salemi, *Physics-of-failure based handbook of microelectronic systems*. RiAC, 2008.

[27] S. V Dhople, A. Davoudi, A. D. Dom, and P. L. Chapman, "A Unified Approach to Reliability Assessment of Energy Conversion Systems," *Ieee Trans. Power Electron.*, vol. 27, no. 2, pp. 739–751, 2012.

[28] H. Behjati and A. Davoudi, "Reliability analysis framework for structural redundancy in power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4376–4386, 2013.

[29] M. K. Alam and F. H. Khan, "Reliability analysis and performance degradation of a boost converter," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3986–3994, 2014.

[30] H. Behjati and A. Davoudi, "Comparative reliability study of hybrid energy storage systems in hybrid electric vehicles," *2012 IEEE Transp. Electrif. Conf. Expo, ITEC 2012*, 2012.

[31] S. Mathew, D. Das, R. Rossenberger, and M. Pecht, "Failure mechanisms based prognostics," in *Proceedings of the 1st International Conference on Prognostics and Health Management, Denver, CO*, 2008.

[32] N. Valentine, D. Das, and P. M. Pecht, "Failure Mechanisms of Insulated Gate Bipolar Transistors (IGBTs)," pp. 1–30, 2015.

[33] N. M. Vichare and M. G. Pecht, "Prognostics and health management of electronics," *IEEE Trans. components Packag. Technol.*, vol. 29, no. 1, pp. 222–229, 2006.

[34] N. Vichare, P. Rodgers, V. Eveloy, and M. Pecht, "Environment and Usage Monitoringof Electronic Products for Health Assessment and Product Design," *Qual. Technol. Quant. Manag.*, vol. 4, no. 2, pp. 235–250, 2007.

[35] D. Chamund and D. Newcombe, "AN 5945 IGBT Module Reliability," *October*, no. October, pp. 1–8, 2010.

[36] Y. Avenas, L. Dupont, N. Baker, H. Zara, and F. Barruel, "Condition Monitoring: A Decade of Proposed Techniques," *IEEE Ind. Electron. Mag.*, vol. 9, no. 4, pp. 22–36, 2015.

[37] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power Converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 590–602, 2015.

[38] W. Huai *et al.*, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 1, pp. 97–114, 2014.

[39] A. Testa, S. De Caro, and S. Russo, "A reliability model for power MOSFETs working in avalanche mode based on an experimental temperature distribution analysis," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3093–3100, 2012.

[40] H. Wang, K. Ma, and F. Blaabjerg, "Design for reliability of power electronic systems," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 33–44.

[41] G. H. Ebel, "Reliability physics in electronics: a historical view," *IEEE Trans. Reliab.*, vol. 47, no. 3, pp. SP379-SP389, 1998.

[42] B. Tuchband, N. Vichare, and M. Pecht, "A method for implementing prognostics to legacy systems," *Proc. IMAPS Mil. Aerospace, Sp. Homel. Secur. Packag. Issues Appl.*, 2006.

[43] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2413–2426, 2015.

[44] M. Pecht, *Product reliability, maintainability, and supportability handbook*. CRC Press, 2009.

[45] M. Pecht, "Chapter 150 Prognostics and Health Management," *Prism*, pp. 1–13, 1991.
[46] Y. Yang, H. Wang, F. Blaabjerg, and T. Kerekes, "A hybrid power control concept for PV inverters with reduced thermal loading," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6271–6275, 2014.
[47] A. Anurag, Y. Yang, and F. Blaabjerg, "Reliability analysis of single-phase PV inverters with reactive power injection at night considering mission profiles," *2015 IEEE Energy Convers. Congr. Expo. ECCE 2015*, vol. 3, no. 4, pp. 2132–2139, 2015.
[48] B. Van Tassell *et al.*, "Metacapacitors: Printed thin film, flexible capacitors for power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2695–2708, 2016.
[49] M. Musallam, C. Yin, C. Bailey, and M. Johnson, "Mission profile-based reliability design and real-time life consumption estimation in power electronics," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2601–2613, 2015.
[50] U. Choi, F. Blaabjerg, and K. Lee, "Study and Handling Methods of Power IGBT Module Failures in Power Electronic Converter Systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, 2015.
[51] V. Samavatian and A. Radan, "A high efficiency input/output magnetically coupled interleaved buck-boost converter with low internal oscillation for fuel-cell applications: CCM steady-state analysis," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5560–5568, 2015.
[52] F. Meinguet *et al.*, "Fault-Tolerant Operation of an Open-End Winding Five-Phase PMSM Drive with Inverter Faults To cite this version : Science Arts & Métiers (SAM)," pp. 5189–5194, 2013.
[53] Y. Li, H. Lin, H. Huang, C. Chen, and H. Yang, "Analysis and Performance Evaluation of an Efficient Power-Fed Permanent Magnet Adjustable Speed Drive," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 784–794, 2019.
[54] C. Wang, J. Li, Y. Yang, and F. Ye, "Combining Solar Energy Harvesting with Wireless Charging for Hybrid Wireless Sensor Networks," *IEEE Trans. Mob. Comput.*, vol. 17, no. 3, pp. 560–576, 2018.
[55] J. W. Kimball, B. T. Kuhn, and R. S. Balog, "A system design approach for unattended solar energy harvesting supply," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 952–962, 2009.
[56] A. Ristow, M. Begović, A. Pregelj, and A. Rohatgi, "Development of a methodology for improving photovoltaic inverter reliability," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2581–2592, 2008.
[57] J. Jones and J. Hayes, "Estimation of system reliability using a 'non-constant failure rate' model," *IEEE Trans. Reliab.*, vol. 50, no. 3, pp. 286–288, 2001.
[58] P. Wikström, L. A. Terens, and H. Kobi, "Reliability, availability, and maintainability of high-power variable-speed drive systems," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 231–241, 2000.
[59] E. Strangas, S. Aviyente, J. Neely, and S. S. H. Zaidi, "Improving the reliability of electrical drives through failure prognosis," *SDEMPED 2011 - 8th IEEE Symp. Diagnostics Electr. Mach. Power Electron. Drives*, pp. 172–178, 2011.
[60] S. Ceballos, J. Pou, E. Robles, J. Zaragoza, and J. L. Martin, "Performance evaluation of fault-tolerant neutral-point-clamped converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2709–2718, 2010.
[61] M. Pecht and W. C. Kang, "A Critique of Mil-Hdbk-217E Reliability Prediction Methods," *IEEE Trans. Reliab.*, vol. 37, no. 5, pp. 453–457, 1988.
[62] A. T. Bryant, P. A. Mawby, P. R. Palmer, E. Santi, and J. L. Hudgins, "Exploration of power device reliability using compact device models and fast electrothermal simulation," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 894–903, 2008.
[63] H. de Lambilly and H. O. Keser, "Failure Analysis of Power Modules: A Look at the Packaging and Reliability of Large IGBT's," *IEEE Trans. Components, Hybrids, Manuf. Technol.*, vol. 16, no. 4, pp. 412–417, 1993.
[64] M. Ciappa, F. Carbognani, P. Cova, and W. Fichtner, "Lifetime prediction and design of reliability tests for high-power devices in automotive applications," *IEEE Int. Reliab. Phys. Symp. Proc.*, vol. 2003–Janua, no. 4, pp. 523–528, 2003.
[65] C. Bailey, T. Tilford, and H. Lu, "Reliability analysis for power electronics modules," *ISSE 2007 - 30th Int. Spring Semin. Electron. Technol. 2007; Conf. Proc. Emerg. Technol. Electron. Packag.*, pp. 12–17, 2007.
[66] M. J. Cushing, D. E. Mortin, T. J. Stadterman, and A. Malhotra, "Comparison of Electronics-

Reliability Assessment Approaches," *IEEE Trans. Reliab.*, vol. 42, no. 4, pp. 542–546, 1993.
[67] D. Hirschmann, D. Tissen, S. Schröder, and R. W. De Doncker, "Reliability prediction for inverters in hybrid electrical vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2511–2517, 2007.
[68] A. D. Domínguez-García and P. T. Krein, "Integrating reliability into the design of fault-tolerant power electronics systems," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, pp. 2665–2671, 2008.
[69] Y. Wu, J. Kang, Y. Zhang, S. Jing, and D. Hu, "Study of reliability and accelerated life test of electric drive system," *2009 IEEE 6th Int. Power Electron. Motion Control Conf. IPEMC '09*, vol. 3, pp. 1060–1064, 2009.
[70] S. S. Smater and A. D. Domínguez-García, "A unified framework for reliability assessment of wind energy conversion systems," in *IEEE PES General Meeting*, 2010, pp. 1–4.
[71] D. A. Murdock, J. E. Ramos Torres, J. J. Connors, and R. D. Lorenz, "Active thermal control of power electronic modules," *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 552–558, 2006.
[72] Y. Xiong, X. Cheng, Z. J. Shen, C. Mi, H. Wu, and V. K. Garg, "Prognostic and warning system for power-electronic modules in electric, hybrid electric, and fuel-cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2268–2276, 2008.
[73] S. Khomfoi and L. M. Tolbert, "Fault diagnosis and reconfiguration for multilevel inverter drive using AI-based techniques," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2954–2968, 2007.
[74] L. Sun, Q. T. An, L. Z. Sun, and K. Zhao, "Switching function model-based fast-diagnostic method of open-switch faults in inverters without sensors," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 119–126, 2011.
[75] A. Ginart, I. Barlas, J. Dorrity, P. Kalgren, and M. Roemer, "Self-Healing from a PHM Perspective," *2006 IEEE Autotestcon*, pp. 697–703, 2006.
[76] A. Lahyani, P. Venet, G. Grellet, and P. J. Viverge, "Failure prediction of electrolytic capacitors during operation of a switchmode power supply," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1199–1207, 1998.
[77] P. Lezana, J. Rodrguez, R. Aguilera, and C. Silva, "Fault Detection on Multicell Converter Based on Output Voltage Frequency Analysis," in *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, 2006, pp. 1691–1696.
[78] F. Richardeau, P. Baudesson, and T. A. Meynard, "Failures-tolerance and remedial strategies of a PWM multicell inverter," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 905–912, 2002.
[79] C. Turpin, P. Baudesson, F. Richardeau, F. Forest, and T. A. Meynard, "Fault management of multicell converters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 988–997, 2002.
[80] K. S. Smith, L. Ran, and J. Penman, "Real-time detection of intermittent misfiring in a voltage-fed pwm inverter induction-motor drive," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 468–476, 1997.
[81] R. Peuget, S. Courtine, and J.-. Rognon, "Fault detection and isolation on a PWM inverter by knowledge-based model," *IEEE Trans. Ind. Appl.*, vol. 34, no. 6, pp. 1318–1326, 1998.
[82] D. Diallo, M. E. H. Benbouzid, D. Hamad, and X. Pierre, "Fault detection and diagnosis in an induction machine drive: A pattern recognition approach based on Concordia stator mean current vector," *IEMDC 2003 - IEEE Int. Electr. Mach. Drives Conf.*, vol. 3, no. 3, pp. 1448–1453, 2003.
[83] O. Wallmark, L. Harnefors, and O. Carlson, "Control algorithms for a fault-tolerant PMSM drive," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1973–1980, 2007.
[84] S. Li and L. Xu, "Strategies of fault tolerant operation for three-level PWM inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 933–940, 2006.
[85] T. Liu, J. Fu, S. Member, and T. A. Lipo, "A Strategy for Improving Reliability of Field-Oriented Controlled Induction Motor Drives," vol. 29, no. 5, pp. 910–918, 1993.
[86] W. Song and A. Q. Huang, "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2700–2708, 2010.
[87] M. A. Parker, C. Ng, and L. Ran, "Fault-Tolerant Control for a Modular Generator–Converter Scheme for Direct-Drive Wind Turbines," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 305–315, 2011.
[88] X. Kou, K. A. Corzine, Y. L. Familiant, and S. Member, "A Unique Fault-Tolerant Design for

Flying Capacitor Multilevel Inverter," vol. 19, no. 4, pp. 979–987, 2004.
[89] H. Wang, D. Zhou, and F. Blaabjerg, "A reliability-oriented design method for power electronic converters," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 2921–2928.
[90] D. Zhou, G. Zhang, and F. Blaabjerg, "Optimal Selection of Power Converter in DFIG Wind Turbine with Enhanced System-Level Reliability," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3637–3644, 2018.
[91] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, 2011.
[92] B. Wang, "Review of Power Semiconductor Device Reliability for Power Converters," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 101–117, 2017.
[93] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters - An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, 2014.
[94] Y. Song and B. Wang, "Survey on reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 591–604, 2013.
[95] K. Ma, H. Wang, and F. Blaabjerg, "New Approaches to Reliability Assessment," *IEEE Power Electron. Mag.*, vol. 3, no. December, p. 13, 2016.
[96] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 17–26, 2013.
[97] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, 2005.
[98] L. M. Moore and H. N. Post, "Five years of operating experience at a large, utility-scale photovoltaic generating plant," *Prog. Photovoltaics Res. Appl.*, vol. 16, no. 3, pp. 249–259, 2008.
[99] L. Palma and P. N. Enjeti, "A modular fuel cell, modular DC-DC converter concept for high performance and enhanced reliability," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1437–1443, 2009.
[100] S. W. Hong *et al.*, "High area-efficient DC-DC converter with high reliability using time-mode miller compensation (TMMC)," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2457–2468, 2013.
[101] Z. Zhong, Y. Chen, and Y. Kang, "Function-integrated network for flying-capacitor three-level DC–DC conversion system," *Electron. Lett.*, vol. 52, no. 9, pp. 754–755, 2016.
[102] A. Khaligh, A. M. Rahimi, and A. Emadi, "Modified pulse-adjustment technique to control DC/DC converters driving variable constant-power loads," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1133–1146, 2008.
[103] H. J. Choe, Y. C. Chung, C. H. Sung, J. J. Yun, and B. Kang, "Passive snubber for reducing switching-power losses of an IGBT in a DC-DC boost converter," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6332–6341, 2014.
[104] L. F. Costa, G. Buticchi, and M. Liserre, "Optimum Design of a Multiple-Active-Bridge DC-DC Converter for Smart Transformer," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10112–10121, 2018.
[105] Y. Liu, M. Huang, H. Wang, X. Zha, J. Gong, and J. Sun, "Reliability-Oriented Optimization of the LC Filter in a Buck DC-DC Converter," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6323–6337, 2017.
[106] A. Sadeghfam, S. Tohidi, and M. Abapour, "Reliability comparison of different power electronic converters for grid-connected PMSG wind turbines," *Int. Trans. Electr. Energy Syst.*, vol. 27, no. 9, pp. 1–11, 2017.
[107] T. Rahimi, S. H. Hosseini, M. Sabahi, G. B. Gharehpetian, and M. Abapour, "Reliability evaluation of a fault-tolerant three-phase interleaved DC-DC boost converter," *Trans. Inst. Meas. Control*, pp. 1–12, 2018.
[108] H. Khazraj, M. Ashouri, F. F. Silva, and C. L. Bak, "Investigation of DC-DC Boost Converter for Reliability of Operational Planning," *2018 IEEE Int. Conf. Environ. Electr. Eng. 2018 IEEE Ind. Commer. Power Syst. Eur. (EEEIC / I&CPS Eur.*, pp. 1–5, 2018.
[109] J. Hannonen, J. Honkanen, J. P. Ström, T. Kärkkäinen, S. Räisänen, and P. Silventoinen, "Capacitor Aging Detection in a DC-DC Converter Output Stage," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3224–3233, 2016.

[110] S. V. Dhople and A. D. Domínguez-García, "Estimation of photovoltaic system reliability and performance metrics," *IEEE Trans. Power Syst.*, vol. 27, no. 1, pp. 554–563, 2012.
[111] A. M. Bazzi, A. Dominguez-Garcia, and P. T. Krein, "Markov reliability modeling for induction motor drives under field-oriented control," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 534–546, 2012.
[112] J. Sakly, A. Bennani-Ben Abdelghani, I. Slama-Belkhodja, and H. Sammoud, "Reconfigurable DC/DC Converter for Efficiency and Reliability Optimization," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 3, pp. 1216–1224, 2017.
[113] A. Khosroshahi, M. Abapour, and M. Sabahi, "Reliability evaluation of conventional and interleaved DC-DC boost converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5821–5828, 2015.
[114] H. Marien, M. Steyaert, E. van Veenendaal, and P. Heremans, "Organic dual DC-DC upconverter on foil for improved circuit reliability," *Electron. Lett.*, vol. 47, no. 4, p. 278, 2011.
[115] F. H. Aghdam and M. Abapour, "Reliability and Cost Analysis of Multistage Boost Converters Connected to PV Panels," *IEEE J. Photovoltaics*, vol. 6, no. 4, pp. 981–989, 2016.
[116] H. Tarzamni, E. Babaei, A. Zarrin Gharehkoushan, and M. Sabahi, "Interleaved full ZVZCS DC–DC boost converter: analysis, design, reliability evaluations and experimental results," *IET Power Electron.*, vol. 10, no. 7, pp. 835–845, 2017.
[117] I. Villanueva, M. A. Juarez, P. R. Martínez, J. M. Sosa, and G. Vazquez, "Comparative analysis of the reliability of drivers for power LED," *2015 IEEE Int. Autumn Meet. Power, Electron. Comput. ROPEC 2015*, no. 3, 2016.
[118] D. Zhou, H. Wang, and F. Blaabjerg, "Mission Profile Based System-Level Reliability Analysis of DC/DC Converters for a Backup Power Application," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8030–8039, 2018.
[119] B. Yao, H. Chen, X. He, and Q. Xiao, "16-02-20095308V1_N1_Artigo 10.Pdf," pp. 1133–1135, 2013.
[120] E. Jamshidpour, P. Poure, and S. Saadate, "Photovoltaic Systems Reliability Improvement by Real-Time FPGA-Based Switch Failure Diagnosis and Fault-Tolerant DC-DC Converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7247–7255, 2015.
[121] S. Dusmez, M. Bhardwaj, L. Sun, and B. Akin, "A software frequency response analysis method to monitor degradation of power MOSFETs in basic single-switch converters," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2016–May, pp. 505–510, 2016.
[122] N. Degrenne and S. Mollov, "Real-life vs. standard driving cycles and implications on EV power electronic reliability," *IECON Proc. (Industrial Electron. Conf.*, pp. 2177–2182, 2016.
[123] G. Petrone, G. Spagnuolo, R. Teodorescu, M. Veerachary, and M. Vitelli, "Reliability issues in photovoltaic power processing systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2569–2580, 2008.
[124] F. Chan and H. Calleja, "Design strategy to optimize the reliability of grid-connected PV systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4465–4472, 2009.
[125] L. Maharjan, S. Member, T. Yamagishi, H. Akagi, and J. Asakura, "Specyfication Cortical Area.Pdf," vol. 25, no. 9, pp. 2386–2396, 2010.
[126] R. Burgos, G. Chen, F. Wang, D. Boroyevich, W. G. Odendaal, and J. D. Van Wyk, "Reliability-oriented design of three-phase power converters for aircraft applications," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 48, no. 2, pp. 1249–1263, 2012.
[127] Y. Luo *et al.*, "Failure Analysis of Power Devices."
[128] ZVEI, "Handbook for Robustness Validation of Automotive Electrical / Electronic Modules," pp. 1–44, 2008.
[129] J. H. L. Pang, F. L. Wong, K. T. Heng, Y. S. Chua, and C. E. Long, "Combined vibration and thermal cycling fatigue analysis for SAC305 lead free solder assemblies," in *2013 IEEE 63rd Electronic Components and Technology Conference*, 2013, pp. 1300–1307.
[130] Y. Wang, Y. Yao, and L. M. Keer, "A statistical mechanics model to predict electromigration induced damage and void growth in solder interconnects," *Phys. A Stat. Mech. its Appl.*, vol. 468, no. Supplement C, pp. 195–204, 2017.
[131] P. Darbandi, T. R. Bieler, F. Pourboghrat, and T. Lee, "The Effect of Cooling Rate on Grain Orientation and Misorientation Microstructure of SAC105 Solder Joints Before and After Impact Drop Tests," *J. Electron. Mater.*, vol. 43, no. 7, pp. 2521–2529, Jul. 2014.
[132] S. H. Ali, S. Dusmez, and B. Akin, "Investigation of collector emitter voltage characteristics in

thermally stressed discrete IGBT devices," *ECCE 2016 - IEEE Energy Convers. Congr. Expo. Proc.*, 2016.

[133] S. H. Ali, S. Dusmez, and B. Akin, "A comprehensive study on variations of discrete IGBT characteristics due to package degradation triggered by thermal stress," *ECCE 2016 - IEEE Energy Convers. Congr. Expo. Proc.*, pp. 1–6, 2016.

[134] S. H. Ali, M. Heydarzadeh, S. Dusmez, X. Li, A. S. Kamath, and B. Akin, "Lifetime Estimation of Discrete IGBT Devices Based on Gaussian Process," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 395–403, 2018.

[135] B. J. Baliga, *Fundamentals of power semiconductor devices*. Springer Science & Business Media, 2010.

[136] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor power devices: physics, characteristics, reliability*. Springer Science & Business Media, 2011.

[137] M. A. Rodríguez, A. Claudio, D. Theilliol, and L. G. Vela, "A new fault detection technique for IGBT based on gate voltage monitoring," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, pp. 1001–1005, 2007.

[138] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, "Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics," *IEEE Trans. Reliab.*, vol. 58, no. 2, pp. 271–276, 2009.

[139] D. W. Brown, M. Abbas, A. Ginart, I. N. Ali, P. W. Kalgren, and G. J. Vachtsevanos, "Turn-off time as an early indicator of insulated gate bipolar transistor latch-up," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 479–489, 2012.

[140] J. S. S. T. Association, "Failure mechanisms and models for semiconductor devices," *JEDEC Publ. JEP122-B*, 2003.

[141] K. Zeng and K. N. Tu, "Six cases of reliability study of Pb-free solder joints in electronic packaging technology," *Mater. Sci. Eng. R Reports*, vol. 38, no. 2, pp. 55–105, 2002.

[142] M. Brincker, S. Söhl, R. Eisele, and V. N. Popok, "Strength and reliability of low temperature transient liquid phase bonded CuSnCu interconnects," *Microelectron. Reliab.*, vol. 76–77, pp. 378–382, 2017.

[143] J. Wang, X. Long, and Y. Yao, "Effects of aging temperature on tensile and fatigue behavior of Sn-3.0Ag-0.5Cu solder joints," *J. Mater. Sci. Mater. Electron.*, vol. 28, no. 19, pp. 14884–14892, 2017.

[144] X. Zhao, P. Watte, H. de Vries, and G. van Hees, "Challenges in Predicting the Solder Interconnect Lifetime of High Power Electronics," in *2018 19th International Conference on Electronic Packaging Technology (ICEPT)*, 2018, pp. 1511–1517.

[145] V. Ramachandran and K. Chiang, "Feasibility Evaluation of Creep Model for Failure Assessment of Solder Joint Reliability of Wafer-Level Packaging," *IEEE Trans. Device Mater. Reliab.*, vol. 17, no. 4, pp. 672–677, 2017.

[146] E. H. Amalu and N. N. Ekere, "Modelling evaluation of Garofalo-Arrhenius creep relation for lead-free solder joints in surface mount electronic component assemblies," *J. Manuf. Syst.*, vol. 39, no. Supplement C, pp. 9–23, 2016.

[147] M. T. Zarmai, N. N. Ekere, C. F. Oduoza, and E. H. Amalu, "Evaluation of thermo-mechanical damage and fatigue life of solar cell solder interconnections," *Robot. Comput. Integr. Manuf.*, vol. 47, pp. 37–43, Oct. 2017.

[148] A. Syed, "Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints," in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, 2004, vol. 1, p. 737–746 Vol.1.

[149] E. H. Amalu, N. N. Ekere, M. T. Zarmai, and G. Takyi, "Optimisation of thermo-fatigue reliability of solder joints in surface mount resistor assembly using Taguchi method," *Finite Elem. Anal. Des.*, vol. 107, pp. 13–27, Dec. 2015.

[150] B. Talebanpour, U. Sahaym, and I. Dutta, "Effect of Composition and Thermal-Mechanical History on the Creep Behavior of Sn-Ag-Cu Solders-Part II: Model," *IEEE Trans. Device Mater. Reliab.*, vol. 16, no. 3, pp. 326–335, 2016.

[151] V. N. Le, L. Benabou, V. Etgens, and Q. B. Tao, "Finite element analysis of the effect of process-induced voids on the fatigue lifetime of a lead-free solder joint under thermal cycling," *Microelectron. Reliab.*, vol. 65, pp. 243–254, Oct. 2016.

[152] P. Xu, M. Rauer, M. Kaloudis, and J. Franke, "Simulation-aided analysis of the influence of voids on the reliability of solder-joints for LED-applications," in *2016 6th Electronic System-*

Integration Technology Conference (ESTC), 2016, pp. 1–5.
[153] K. C. Otiaba, M. I. Okereke, and R. S. Bhatti, "Numerical assessment of the effect of void morphology on thermo-mechanical performance of solder thermal interface material," *Appl. Therm. Eng.*, vol. 64, no. 1, pp. 51–63, 2014.
[154] R. Schwerz, S. Meyer, M. Roellig, K. Meier, and K. J. Wolter, "Finite element modeling on thermal fatigue of BGA solder joints with multiple voids," *Proc. Int. Spring Semin. Electron. Technol.*, pp. 380–385, 2011.
[155] L. Zhang, L. Sun, Y. Guo, and C. He, "Reliability of lead-free solder joints in CSP device under thermal cycling," *J. Mater. Sci. Mater. Electron.*, vol. 25, no. 3, pp. 1209–1213, 2014.
[156] Y. Chen, Y. Jin, and R. Kang, "Coupling damage and reliability modeling for creep and fatigue of solder joint," *Microelectron. Reliab.*, vol. 75, pp. 233–238, 2017.
[157] Z.-H. Zhang, X.-S. Wang, H.-H. Ren, S. Jia, and H.-H. Yang, "Simulation study on thermo-fatigue failure behavior of solder joints in package-on-package structure," *Microelectron. Reliab.*, vol. 75, pp. 127–134, Aug. 2017.
[158] L. Zhang and L. Sun, "Reliability of Pb-free solder joints in FCBGA using finite element simulation and Taguchi method," pp. 197–200, 2015.
[159] F. Baber and I. Guven, "Solder joint fatigue life prediction using peridynamic approach," *Microelectron. Reliab.*, vol. 79, pp. 20–31, 2017.
[160] B. Metais *et al.*, "A viscoplastic-fatigue-creep damage model for tin-based solder alloy," *2015 16th Int. Conf. Therm. Mech. Multi-Physics Simul. Exp. Microelectron. Microsystems, EuroSimE 2015*, pp. 1–5, 2015.
[161] R. Schmidt, F. Zeyss, and U. Scheuermann, "Impact of absolute junction temperature on power cycling lifetime," *2013 15th Eur. Conf. Power Electron. Appl. EPE 2013*, 2013.
[162] R. Amro, J. Lutz, and O. U. Magdeburg-germany, "Double-Sided Low-Temperature Joining Technique for Power Cycling Capa- kB Tm ATj [K]."
[163] D. Xiang, L. Ran, P. Tavner, A. Bryant, S. Yang, and P. Mawby, "Monitoring solder fatigue in a power module using case-above-ambient temperature rise," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2578–2591, 2011.
[164] W. W. Sheng and R. P. Colino, *Power electronic modules: design and manufacture*. CRC press, 2004.
[165] V. Smet, F. Forest, J. J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of Vcemonitoring as a real-time method to estimate aging of bond wire-IGBT modules stressed by power cycling," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2760–2770, 2013.
[166] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectron. Reliab.*, vol. 42, no. 4, pp. 653–667, 2002.
[167] J.-. Thebaud, E. Woirgard, C. Zardini, S. Azzopardi, O. Briat, and J.-. Vinassa, "Strategy for designing accelerated aging tests to evaluate IGBT power modules lifetime in real operation mode," *IEEE Trans. Components Packag. Technol.*, vol. 26, no. 2, pp. 429–438, 2003.
[168] H. Berg and E. Wolfgang, "Advanced IGBT modules for railway traction applications: Reliability testing," *Microelectron. Reliab.*, vol. 38, no. 6–8, pp. 1319–1323, 1998.
[169] S. Dusmez, H. Duran, and B. Akin, "Remaining Useful Lifetime Estimation for Thermally Stressed Power MOSFETs Based on on-State Resistance Variation," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2554–2563, 2016.
[170] U. M. Choi *et al.*, "Power cycling test and failure analysis of molded Intelligent Power IGBT Module under different temperature swing durations," *Microelectron. Reliab.*, vol. 64, pp. 403–408, 2016.
[171] H. Kuhn and A. Mertens, "On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters," in *Power Electronics and Applications, 2009. EPE'09. 13th European Conference on*, 2009, pp. 1–10.
[172] W. Lai, M. Chen, L. Ran, O. Alatise, S. Xu, and P. Mawby, "Low ΔtjStress Cycle Effect in IGBT Power Module Die-Attach Lifetime Modeling," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6575–6585, 2016.
[173] C. Busca *et al.*, "An overview of the reliability prediction related aspects of high power IGBTs in wind power applications," *Microelectron. Reliab.*, vol. 51, no. 9–11, pp. 1903–1907, 2011.
[174] I. F. Kovacevic, U. Drofenik, and J. W. Kolar, "New physical model for lifetime estimation of power modules," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 2106–2114.

[175] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules - various factors influencing lifetime," *5th Int. Conf. Integr. Power Syst.*, pp. 1–6, 2008.
[176] L. Yang, P. A. Agyakwa, and C. M. Johnson, "Physics-of-{Failure} {Lifetime} {Prediction} {Models} for {Wire} {Bond} {Interconnects} in {Power} {Electronic} {Modules}," *IEEE Trans. Device Mater. Reliab.*, vol. 13, no. 1, pp. 9–17, 2013.
[177] J. Lemaitre and R. Desmorat, *Engineering damage mechanics: ductile, creep, fatigue and brittle failures*. Springer Science & Business Media, 2005.
[178] C. Lin, W. S. Chow, C. N. Madu, C. H. Kuei, and P. Pei Yu, "A structural equation model of supply chain quality management and organizational performance," *Int. J. Prod. Econ.*, vol. 96, no. 3, pp. 355–365, 2005.
[179] P. Hegde, D. C. Whalley, and V. V. Silberschmidt, "Creep damage study at powercycling of lead-free surface mount device," *Comput. Mater. Sci.*, vol. 45, no. 3, pp. 638–645, 2009.
[180] E. H. Amalu and N. N. Ekere, "High temperature reliability of lead-free solder joints in a flip chip assembly," *J. Mater. Process. Technol.*, vol. 212, no. 2, pp. 471–483, 2012.
[181] S. Dusmez, S. H. Ali, M. Heydarzadeh, A. S. Kamath, H. Duran, and B. Akin, "Aging precursor identification and lifetime estimation for thermally aged discrete package silicon power switches," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 251–260, 2017.
[182] X. H. Yang, W. X. Yao, and C. M. Duan, "The development of deterministic fatigue cumulative damage theory," *Eng. Sci.*, vol. 15, no. 14, pp. 81–87, 2003.
[183] E. W. C. Wilkins, "Cumulative damage in fatigue," in *Colloquium on Fatigue/Colloque de Fatigue/Kolloquium über Ermüdungsfestigkeit*, 1956, pp. 321–332.
[184] S. P. Zhu, H. Z. Huang, L. P. He, Y. Liu, and Z. Wang, "A generalized energy-based fatigue-creep damage parameter for life prediction of turbine disk alloys," *Eng. Fract. Mech.*, vol. 90, pp. 89–100, 2012.
[185] Z. Lv, H.-Z. Huang, S.-P. Zhu, H. Gao, and F. Zuo, "A modified nonlinear fatigue damage accumulation model," *Int. J. Damage Mech.*, vol. 24, no. 2, pp. 168–181, Mar. 2015.
[186] V. Samavatian, H. Iman-eini, and Y. Avenas, "An e ffi cient online time-temperature-dependent creep-fatigue rain fl ow counting algorithm," vol. 116, no. April, pp. 284–292, 2018.
[187] G. R. Halford, M. H. Hirschberg, and S. S. Manson, "Creep fatigue analysis by strain-range partitioning," 1971.
[188] S. Majumdar and P. S. Maiya, "Damage equation for creep-fatigue interaction.[Total plastic strain, strain rate]," Argonne National Lab., IL (USA), 1976.
[189] E. G. Ellison and A. Al-Zamily, "FRACTURE AND LIFE PREDICTION UNDER THERMAL-MECHANICAL STRAIN CYCLING," *Fatigue Fract. Eng. Mater. Struct.*, vol. 17, no. 1, pp. 53–67, 1994.
[190] W. J. Minford, "Accelerated Life Testing and Reliability of High K Multilayer Ceramic Capacitors," *IEEE Trans. Components, Hybrids, Manuf. Technol.*, vol. 5, no. 3, pp. 297–300, 1982.
[191] South Africa's NEMO, "White Paper:," pp. 4–19, 2014.
[192] N. Kubodera, T. Oguni, M. Matsuda, H. Wada, N. Inoue, and T. Nakamura, "Study of the long term reliability for MLCCs," *Proc. Cart. Int.*, pp. 1–9, 2012.
[193] S. G. Parler Jr and P. E. C. Dubilier, "Deriving life multipliers for electrolytic capacitors," *IEEE Power Electron. Soc. Newsl.*, vol. 16, no. 1, pp. 11–12, 2004.
[194] E. N. Power, "Capacitors age and capacitors have an end of life," *White Pap.*, 2008.
[195] A. Albertsen, "Electrolytic capacitor lifetime estimation," *Jianghai Eur. GmbH*, 2010.
[196] S. V Dhople, A. Davoudi, A. D. Domínguez-García, and P. L. Chapman, "A Unified Approach to Reliability Assessment of Multiphase DC–DC Converters in Photovoltaic Energy Conversion Systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 739–751, 2012.
[197] H. Behjati and A. Davoudi, "Reliability Analysis Framework for Structural Redundancy in Power Semiconductors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4376–4386, 2013.
[198] G. Fontana, A. Luchetta, S. Manetti, and M. C. Piccirilli, "A Testability Measure for DC-Excited Periodically Switched Networks With Applications to DC-DC Converters," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 10, pp. 2321–2341, 2016.
[199] M. di Bernardo and F. Vasca, "Discrete-time maps for the analysis of bifurcations and chaos in DC/DC converters," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 47, no. 2, pp. 130–143, 2000.

[200] Y. Chen, A. Davoudi, and P. L. Chapman, "Multifrequency modeling of a multiple-input Dc-Dc converter," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 4604–4610.
[201] V. P. N and M. K. Kazimierczuk, "Small-Signal Modeling of Open-Loop PWM Z-Source Converter by Circuit-Averaging Technique," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1286–1296, 2013.
[202] C. Bernal, E. Oyarbide, P. M. Gaudo, and A. Mediano, "Dynamic Model of Class-E Inverter With Multifrequency Averaged Analysis," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3737–3744, 2012.
[203] F. Wang, H. Zhang, and X. Ma, "Analysis of Slow-Scale Instability in Boost PFC Converter Using the Method of Harmonic Balance and Floquet Theory," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 57, no. 2, pp. 405–414, 2010.
[204] J. A. Á. Martín, J. R. Melgoza, and J. J. R. Pasaye, "Exact steady state analysis in power converters using Floquet decomposition," in *2011 North American Power Symposium*, 2011, pp. 1–7.
[205] R. Trinchero, I. S. Stievano, and F. G. Canavero, "Steady-State Analysis of Switching Power Converters Via Augmented Time-Invariant Equivalents," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5657–5661, 2014.
[206] S. Caporale, F. Pareschi, V. Cambareri, R. Rovatti, and G. Setti, "A Soft-Defined Pulse Width Modulation Approach—Part I: Principles," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 62, no. 9, pp. 2280–2289, 2015.
[207] R. Trinchero, P. Manfredi, I. S. Stievano, and F. G. Canavero, "Steady-State Analysis of Switching Converters via Frequency-Domain Circuit Equivalents," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 63, no. 8, pp. 748–752, 2016.
[208] B. Zhou and T. Zhao, "On Asymptotic Stability of Discrete-Time Linear Time-Varying Systems," *IEEE Trans. Automat. Contr.*, vol. 62, no. 8, pp. 4274–4281, 2017.
[209] H. Qin and J. W. Kimball, "Generalized Average Modeling of Dual Active Bridge DC–DC Converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2078–2084, 2012.
[210] J. W. Kimball and P. T. Krein, "Singular Perturbation Theory for DC-DC Converters and Application to PFC Converters," in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 882–887.
[211] B. Gao, F. Yang, M. Chen, M. Dong, P. Duan, and U. Irfan, "A temperature spectrum density distribution based condition evaluation method and application in IGBT," *Appl. Therm. Eng.*, vol. 106, pp. 1440–1457, 2016.
[212] K. Ma, U. Choi, and F. Blaabjerg, "Impacts of ripple current to the loading and lifetime of power semiconductor device," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2305–2311.
[213] Infineon, "IKP15N60T," 2015.
[214] Infineon, "Explanation of Discrete IGBTs' datasheets," 2015.
[215] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application manual power semiconductors*. 2015.
[216] J. P. Holman, "Heat transfer. 10th." New York: McGraw-Hill, 2010.
[217] D. Christen, M. Stojadinovic, and J. Biela, "Energy efficient heat sink design: Natural vs. forced convection cooling," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016, pp. 1–8.
[218] D. Van de Pol and J. Tierney, "Free Convection Heat Transfer from Vertical Fin-Arrays," *IEEE Trans. Parts, Hybrids, Packag.*, vol. 10, no. 4, pp. 267–271, 1974.
[219] A. S. Bahman, K. Ma, and F. Blaabjerg, "A Lumped Thermal Model Including Thermal Coupling and Thermal Boundary Conditions for High-Power IGBT Modules," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2518–2530, 2018.
[220] A. S. Bahman, K. Ma, and F. Blaabjerg, "Thermal impedance model of high power IGBT modules considering heat coupling effects," in *2014 International Power Electronics and Application Conference and Exposition*, 2014, pp. 1382–1387.
[221] P. Teertstra, M. M. Yovanovich, J. R. Culham, and T. Lemczyk, "Analytical forced convection modeling of plate fin heat sinks," in *Fifteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.99CH36306)*, 1999, pp. 34–41.
[222] Y. S. Muzychka, J. R. Culham, and M. M. Yovanovich, "Thermal Spreading Resistance of Eccentric Heat Sources on Rectangular Flux Channels," *J. Electron. Packag.*, vol. 125, no. 2, pp. 178–185, Jun. 2003.

[223] M. Bouarroudj, Z. Khatir, J. P. Ousten, F. Badel, L. Dupont, and S. Lefebvre, "Degradation behavior of 600 V-200 A IGBT modules under power cycling and high temperature environment conditions," *Microelectron. Reliab.*, vol. 47, no. 9–11 SPEC. ISS., pp. 1719–1724, 2007.

[224] B. Thollin, L. Dupont, Y. Avenas, J. C. Crebier, Z. Khatir, and P. O. Jeannin, "Numerical and Experimental Evaluation of the Microsecond Pulsed Heating Curve Technique Dedicated to Die Interconnection Characterization," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 6, no. 6, pp. 835–845, 2016.

[225] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters - A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, 2012.

[226] D. L. Blackburn, "Temperature measurements of semiconductor devices - a review," *Twent. Annu. IEEE Semicond. Therm. Meas. Manag. Symp. (IEEE Cat. No.04CH37545)*, pp. 70–80, 2004.

[227] V. Samavatian, Y. Avenas, and H. Iman-Eini, "Mutual and self-aging effects of power semiconductors on the thermal behaviour of DC-DC boost power converter," *Microelectron. Reliab.*, vol. 88–90, no. May, pp. 493–499, 2018.

[228] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, 2010.

[229] U. Scheuermann and S. Schuler, "Power cycling results for different control strategies," *Microelectron. Reliab.*, vol. 50, no. 9–11, pp. 1203–1209, 2010.

[230] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power Cycling Reliability of Power Module: A Survey," *IEEE Trans. Device Mater. Reliab.*, vol. 16, no. 1, pp. 80–97, 2016.

[231] "POWER AND TEMPERATURE CYCLING," *JEDEC*, vol. JESD22, no. A105C, 2011.

[232] J. H. L. Pang, B. S. Xiong, C. C. Neo, X. R. Mang, and T. H. Low, "Bulk solder and solder joint properties for lead free 95.5Sn-3.8Ag-0.7Cu solder alloy," in *53rd Electronic Components and Technology Conference, 2003. Proceedings.*, 2003, pp. 673–679.

[233] P. Ghimire, S. Bęczkowski, S. Munk-Nielsen, B. Rannestad, and P. B. Thøgersen, "A review on real time physical measurement techniques and their attempt to predict wear-out status of IGBT," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10.

[234] W. Lai, M. Chen, L. Ran, O. Alatise, S. Xu, and P. Mawby, "Low <inline-formula><tex-math notation="LaTeX">ΔT_{j}</tex-math></inline-formula> Stress Cycle Effect in IGBT Power Module Die-Attach Lifetime Modeling," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6575–6585, 2016.

[235] M. Lai, S.-S. Feng, G.-Y. Huang, and J.-N. Bian, "Damage of different reinforced structures subjected to underwater contact explosion," *Baozha Yu Chongji/Explosion Shock Waves*, vol. 32, no. 6, 2012.

[236] H. Huang and P. A. Mawby, "A lifetime estimation technique for voltage source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4113–4119, 2013.

[237] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: A literature survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, 2015.

[238] G. Marsh *et al.*, "Review and application of Rainflow residue processing techniques for accurate fatigue damage estimation," *Int. J. Fatigue*, vol. 82, pp. 757–765, 2016.

[239] M. Ciappa and A. Blascovich, "Reliability odometer for real-time and in situ lifetime measurement of power devices," *Microelectron. Reliab.*, vol. 55, no. 9, pp. 1351–1356, 2015.

[240] J. A. Bannantine, J. J. Comer, and J. L. Handrock, *Fundamentals of metal fatigue analysis*, vol. 90. Prentice hall Englewood Cliffs, NJ, 1990.

[241] M. Azamfar and M. Moshrefifar, "Moshrefifar and Azamfar method, a new cycle counting method for evaluating fatigue life," *Int. J. Fatigue*, vol. 69, pp. 2–15, 2014.

[242] M. Matsuishi and T. Endo, "Fatigue of metals subjected to varying stress," *Japan Soc. Mech. Eng. Fukuoka, Japan*, vol. 68, no. 2, pp. 37–40, 1968.

[243] K. Mainka, M. Thoben, and O. Schilling, "Lifetime calculation for power modules, application and theory of models and counting methods," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1–8.

[244] L. R. GopiReddy, L. M. Tolbert, B. Ozpineci, and J. O. P. Pinto, "Rainflow Algorithm-Based Lifetime Estimation of Power Semiconductors in Utility Applications," *IEEE Trans. Ind. Appl.*,

vol. 51, no. 4, pp. 3368–3375, 2015.
[245] A. Standard, "Standard practices for cycle counting in fatigue analysis," *ASTM E1049-85, Am. Soc. Test. Mater. West Conshohocken, PA*, 1997.
[246] C. H. McInnes and P. A. Meehan, "Equivalence of four-point and three-point rainflow cycle counting algorithms," *Int. J. Fatigue*, vol. 30, no. 3, pp. 547–559, 2008.
[247] L. L. Schluter, "Programmer's guide for LIFE2's rainflow counting algorithm," Sandia National Labs., Albuquerque, NM (USA), 1991.
[248] A. Nieslony, "Rainflow counting algorithm," *File Exch. Cent. http//www. mathworks. com/matlabcentral/fileexchange/3026-rainflow-counting-algorithm*, 2003.
[249] V. Granados-Alejo, C. Rubio-González, C. A. Vázquez-Jiménez, J. A. Banderas, and G. Gómez-Rosas, "Influence of specimen thickness on the fatigue behavior of notched steel plates subjected to laser shock peening," *Opt. Laser Technol.*, vol. 101, pp. 531–544, 2018.
[250] B. Gao, F. Yang, M. Chen, Y. Chen, W. Lai, and C. Liu, "Thermal lifetime estimation method of IGBT module considering solder fatigue damage feedback loop," *Microelectron. Reliab.*, vol. 82, pp. 51–61, Mar. 2018.
[251] R. E. Moore, *Methods and applications of interval analysis*, vol. 2. Siam, 1979.
[252] S. M. Rump, "INTLAB—interval laboratory," in *Developments in reliable computing*, Springer, 1999, pp. 77–104.
[253] Y. Liu and C. Chen, "Dynamic Reliability Assessment for Nonrepairable Multistate Systems by Aggregating Multilevel Imperfect Inspection Data," *IEEE Trans. Reliab.*, vol. 66, no. 2, pp. 281–297, 2017.
[254] Y. Sun, T. Sun, M. G. Pecht, and C. Yu, "Computing Lifetime Distributions and Reliability for Systems With Outsourced Components: A Case Study," *IEEE Access*, vol. 6, pp. 31359–31366, 2018.
[255] S. H. Sim and J. Endrenyi, "A failure-repair model with minimal and major maintenance," *IEEE Trans. Reliab.*, vol. 42, no. 1, pp. 134–140, 1993.
[256] M. J. Zuo, R. Jiang, and R. C. M. Yam, "Approaches for reliability modeling of continuous-state devices," *IEEE Trans. Reliab.*, vol. 48, no. 1, pp. 9–18, 1999.
[257] M. M. Hosseini, R. M. Kerr, and R. B. Randall, "An inspection model with minimal and major maintenance for a system with deterioration and Poisson failures," *IEEE Trans. Reliab.*, vol. 49, no. 1, pp. 88–98, 2000.
[258] J. Xue and K. Yang, "Dynamic reliability analysis of coherent multistate systems," *IEEE Trans. Reliab.*, vol. 44, no. 4, pp. 683–688, 1995.
[259] H. Pham, A. Suprasad, and R. B. Misra, "Availability and mean life time prediction of multistage degraded system with partial repairs," *Reliab. Eng. Syst. Saf.*, vol. 56, no. 2, pp. 169–173, 1997.
[260] A. Lisnianski, "Extended block diagram method for a multi-state system reliability assessment," *Reliab. Eng. Syst. Saf.*, vol. 92, no. 12, pp. 1601–1607, 2007.
[261] A. Shrestha and L. Xing, "A Logarithmic Binary Decision Diagram-Based Method for Multistate System Analysis," *IEEE Trans. Reliab.*, vol. 57, no. 4, pp. 595–606, 2008.
[262] A. Lisnianski and G. Levitin, *Multi-state system reliability: assessment, optimization and applications*, vol. 6. World Scientific Publishing Company, 2003.
[263] E. Zio, L. Podofillini, and G. Levitin, "Estimation of the importance measures of multi-state elements by Monte Carlo simulation," *Reliab. Eng. Syst. Saf.*, vol. 86, no. 3, pp. 191–204, 2004.
[264] W. Li and M. J. Zuo, "Reliability evaluation of multi-state weighted k-out-of-n systems," *Reliab. Eng. Syst. Saf.*, vol. 93, no. 1, pp. 160–167, 2008.
[265] S. Mathew, P. Rodgers, V. Eveloy, N. Vichare, and M. Pecht, "A methodology for assessing the remaining life of electronic products," *Int. J. Performability Eng.*, vol. 2, no. 4, pp. 383–395, 2006.
[266] H. Liao, W. Zhao, and H. Guo, "Predicting remaining useful life of an individual unit using proportional hazards model and logistic regression model," in *Reliability and Maintainability Symposium, 2006. RAMS'06. Annual*, 2006, pp. 127–132.
[267] N. Z. Gebraeel, M. A. Lawley, R. Li, and J. K. Ryan, "Residual-life distributions from component degradation signals: A Bayesian approach," *IiE Trans.*, vol. 37, no. 6, pp. 543–557, 2005.
[268] W. Wang and A. H. Christer, "Towards a general condition based maintenance model for a stochastic dynamic system," *J. Oper. Res. Soc.*, vol. 51, no. 2, pp. 145–155, 2000.

Appendices

A. power converter modeling

A.1. Electrical modeling

A.1.1. Ideal DC-DC boost converter equations

Regarding Fig. 2-1, in the first period of switching in which S1 is conducting while S2 is off (0<t<DT_S), following equations are held:

$$\begin{cases} v_L(t) = v_i(t) = V_i \\ i_C(t) = -\dfrac{v_o(t)}{R_L} = -\dfrac{V_o}{R_L} \end{cases} \quad \text{(A-1)}$$

where T_S and D are switching period and duty cycle, respectively. In the second period of switching which in S2 is conducting while S1 is off (DT_S <t<T_S) following equations are held:

$$\begin{cases} v_L(t) = v_i(t) - v_o(t) = V_i - V_o \\ i_C(t) = i_L(t) - \dfrac{v_o(t)}{R} = I_L - \dfrac{V_o}{R} \end{cases} \quad \text{(A-2)}$$

Regarding the principles of inductor volt-second balance and capacitor charge balance [199], we can use all time intervals and exerting averaging technique on evaluated equations over one switching period, it yields:

$$\begin{cases} \langle v_L(t) \rangle_T = 0 \Rightarrow V_o = \dfrac{V_i}{1-D} \\ \langle i_C(t) \rangle_T = 0 \Rightarrow I_i = I_L = \dfrac{I_o}{1-D} \end{cases} \quad \text{(A-3)}$$

From equation either (A-1) or (A-2), one can easily find following expressions for the appropriate values of capacitance and inductance meeting specified input current and output voltage ripples.

$$\begin{cases} L = \dfrac{V_i}{2\Delta i_L} DT \\ C = \dfrac{V_o}{2\Delta v_o R} DT \end{cases} \quad \text{(A-4)}$$

A.1.2. Differential equations for the DC-DC boost converter

Regarding Fig. 2-4a, one can write differential equations of the circuit including inductor current and capacitor voltage as following. For obtaining a differential equation describing inductor current, one should use Kirchhoff's voltage law (KVL) in the leftmost loop of the equivalent circuit. Therefore:

$$-v_i(t) + v_L(t) + r_L i_L(t) + v_{CE0}(t) + r_Q i_L(t) = 0 \quad \text{(A-5)}$$

Rearranging the above equation and writing $L\,di_L(t)/dt$ instead of $v_L(t)$, it yields:

$$L\frac{di_L(t)}{dt} = -(r_L + r_Q)i_L(t) + v_i(t) - v_{CE0}(t) \quad \text{(A-6)}$$

For obtaining a differential equation describng capacitor voltage, one should use Kirchhoff's current law (KCL) in the rightmost node of equivalent circuit. Therefore

$$i_C(t) = -\frac{v_O(t)}{R} = -\frac{v_C(t) + r_C i_C(t)}{R} \quad \text{(A-7)}$$

Rearranging above equation and writing $C\,dv_C(t)/dt$ instead of $i_C(t)$, it yields:

$$C\frac{dv_C(t)}{dt} = -\frac{v_C(t)}{R + r_C} \quad \text{(A-8)}$$

Now, with regard to Fig. 2-4b, one can obtain the differential equations including the state variables ($[i_L(t) \quad v_C(t)]^T$) associated to off-state operation mode as follows. Applying KVL to the left loop, it yields:

$$-v_i(t) + v_L(t) + r_L i_L(t) + v_{D0}(t) + r_D i_L(t) + r_C(i_L(t) - i_o(t)) + v_C(t) = 0 \quad \text{(A-9)}$$

Rearranging above equation and writing $L\dfrac{di_L(t)}{dt}$ instead of $v_L(t)$ and $\dfrac{v_C(t) + r_C i_L(t)}{R + r_C}$ instead of $i_O(t)$, it yields:

$$L\frac{di_L(t)}{dt} = -(r_L + r_D + \frac{Rr_C}{R + r_C})i_L(t) - \frac{R}{R + r_C}v_C(t) + v_i(t) - v_{D0}(t) \quad \text{(A-10)}$$

Applying KCL to the rightmost node, it yields

$$i_C(t) = i_L(t) - i_O(t) \quad \text{(A-11)}$$

Rearranging the above equation and writing $C\frac{dv_C(t)}{dt}$ instead of $i_C(t)$ and $\frac{v_C(t)+r_C i_L(t)}{R+r_C}$ instead of $i_O(t)$, it yields:

$$C\frac{dv_C(t)}{dt}=\frac{R}{R+r_C}i_L(t)-\frac{1}{R+r_C}v_C(t) \qquad \text{(A-12)}$$

A.1.3. Time invariant multi frequency modeling

The TIMF modeling is based on the Fourier series representation (FSR) of the switching function, duty cycle command and state variables (inductor current and capacitor voltage) of the DC-DC PWM converters. The FSR of a specified variable (in TIMF it can be the switching function, duty cycle command and state variables), namely $x(t)$, can written as follows

$$x(t)=x_0(t)+\sum_{n=1}^{N}x_{\alpha n}(t)\cos(n\omega_s t)+x_{\beta n}(t)\sin(n\omega_s t) \qquad \text{(A-13)}$$

Where x_0 (t), $x_{\alpha n}$(t), $x_{\beta n}$(t) and ω_s are time-dependent coefficient of FSR and angular switching frequency. More accuracy will be achieved providing that higher-order harmonics (N) have been considered. FSR coefficient is given as

$$\begin{aligned} x_0(t)&=\frac{1}{2\pi}\int_{\omega_s t}^{\omega_s t+2\pi}x(t)\,d(\omega_s t)\\ x_{\alpha n}(t)&=\frac{1}{\pi}\int_{\omega_s t}^{\omega_s t+2\pi}x(t)\cos(n\omega_s t)\,d(\omega_s t)\\ x_{\beta n}(t)&=\frac{1}{\pi}\int_{\omega_s t}^{\omega_s t+2\pi}x(t)\sin(n\omega_s t)\,d(\omega_s t) \end{aligned} \qquad \text{(A-14)}$$

In the vector form, state variables yield (hereafter the time dependency is not indicated for simplicity i.e. instead of writing x(t), we only write x):

$$x=\mathbf{cx} \qquad \text{(A-15)}$$

where $\mathbf{c}$ is the time varying trigonometric vector and $\mathbf{x}$ is the state variables (FSR coefficients).

$$\begin{aligned} \mathbf{c}&=\begin{bmatrix}1 & \cos(\omega_s t) & \sin(\omega_s t) & \dots & \cos(N\omega_s t) & \sin(N\omega_s t)\end{bmatrix}\\ \mathbf{x}&=\begin{bmatrix}x_0 & x_{\alpha 1} & x_{\beta 1} & \dots & x_{\alpha N} & x_{\beta N}\end{bmatrix}^T \end{aligned} \qquad \text{(A-16)}$$

These state variables can allocate to the capacitor voltage (v=**cv**), current inductor (i=**ci**) and switching function (q=**cq**), duty cycle command (d=**cd**).

Determination of derivative of state variables, switching function, product of state variables by switching function has paramount of importance. Regarding equation (A-15), derivative of state variables can be obtained as follows:

$$\mathbf{c} = \begin{bmatrix} 1 & \cos(\omega_s t) & \sin(\omega_s t) & \dots & \cos(N\omega_s t) & \sin(N\omega_s t) \end{bmatrix}$$
$$\mathbf{x} = \begin{bmatrix} x_0 & x_{\alpha 1} & x_{\beta 1} & \dots & x_{\alpha N} & x_{\beta N} \end{bmatrix}^T \quad \text{(A-17)}$$

$d\mathbf{c}/dt$ can be found as follows.

$$\begin{aligned} \frac{d\mathbf{c}}{dt} &= \frac{d}{dt}\begin{bmatrix} 1 & \cos(\omega_s t) & \sin(\omega_s t) & \dots & \cos(N\omega_s t) & \sin(N\omega_s t) \end{bmatrix} \\ &= -\begin{bmatrix} 0 & \omega_s \sin(\omega_s t) & -\omega_s \cos(\omega_s t) & \dots \\ & N\omega_s \sin(N\omega_s t) & -N\omega_s \cos(N\omega_s t) \end{bmatrix} = -\mathbf{c\Omega} \end{aligned} \quad \text{(A-18)}$$

where $\mathbf{\Omega}$ is defined as

$$\mathbf{\Omega} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & -\omega_s & \cdots & 0 & 0 \\ 0 & \omega_s & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 & 0 \\ 0 & 0 & 0 & \cdots & 0 & -N\omega_s \\ 0 & 0 & 0 & \cdots & N\omega_s & 0 \end{bmatrix}_{(2N+1)\times(2N+1)} \quad \text{(A-19)}$$

Thus, the derivative of state variables can be rearrange as:

$$\frac{dx}{dt} = \mathbf{c}\left(-\mathbf{\Omega x} + \frac{d\mathbf{x}}{dt}\right) \quad \text{(A-20)}$$

Fourier series representation of switching function q(t) is defined as

$$q(t) = q_0(t) + \sum_{n=1}^{N} q_{\alpha n}(t)\cos(n\omega_s t) + q_{\beta n}(t)\sin(n\omega_s t) = \mathbf{cq} \quad \text{(A-21)}$$

Switching function has been resulted from a comparison between duty cycle command and sawtooth carrier signal. When duty cycle command is greater than sawtooth signal, switching function equals to one and whenever the duty cycle command is lower that sawtooth signal, it becomes zero. Fig. A-1 depicts its development. Fourier series coefficient of switching function can be defined as

$$\begin{aligned} q_0 &= \frac{1}{2\pi}\int_{\omega_s t_\ell}^{\omega_s t_h} d(\omega_s t) = \frac{t_h - t_\ell}{T_s} \\ q_{\alpha n} &= \frac{1}{\pi}\int_{\omega_s t_\ell}^{\omega_s t_h} \cos(n\omega_s t)d(\omega_s t) = \frac{2}{n\pi}\left[\cos\left(n\pi\frac{t_h + t_\ell}{T_S}\right)\sin\left(n\pi\frac{t_h - t_\ell}{T_S}\right)\right] \\ q_{\beta n} &= \frac{1}{\pi}\int_{\omega_s t_\ell}^{\omega_s t_h} \sin(n\omega_s t)d(\omega_s t) = \frac{2}{n\pi}\left[\sin\left(n\pi\frac{t_h + t_\ell}{T_S}\right)\sin\left(n\pi\frac{t_h - t_\ell}{T_S}\right)\right] \end{aligned} \quad \text{(A-22)}$$

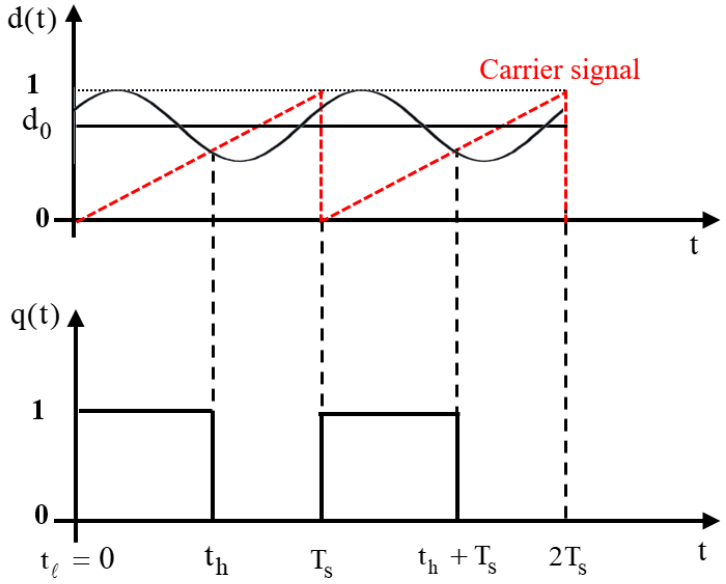


Fig. A-1. Time-dependent duty cycle command and resulted switching function.

Regarding Fig. A-1, t_ℓ equals zero in the sawtooth carrier signal. One can easily find t_h by intersecting the sawtooth carrier signal and duty cycle command signal and employing Newton-Raphson algorithm.

Regarding equation (2-1), another important correlation is the product of state variables by the switching function q(t). This product can be written in FSR matrix form as

$$g = qx = \mathbf{cg} \tag{A-23}$$

where $\mathbf{g}$ is the vector of FSR coefficients and written as

$$\mathbf{g} = \begin{bmatrix} g_0 & g_{\alpha 1} & g_{\beta 1} & \cdots & g_{\alpha N} & g_{\beta N} \end{bmatrix}^T \tag{A-24}$$

The FSR coefficients of $\mathbf{g}$ are calculated by multiplying (A-13) to (A-21) by ignoring higher-order harmonics. Rearranging the resultant, one can find that:

$$\mathbf{g} = \mathbf{Qx} \tag{A-25}$$

Accordingly,

$$qx = \mathbf{cg} = \mathbf{c(Qx)} \tag{A-26}$$

As an example for a second order TIMF (N=2), matrix $\mathbf{Q}$ can be calculated as follows.

$$\mathbf{Q} = \begin{bmatrix} q_0 & \frac{q_{\alpha 1}}{2} & \frac{q_{\beta 1}}{2} & \frac{q_{\alpha 2}}{2} & \frac{q_{\beta 2}}{2} \\ q_{\alpha 1} & q_0 + \frac{q_{\alpha 2}}{2} & \frac{q_{\beta 2}}{2} & \frac{q_{\alpha 1}}{2} & \frac{q_{\beta 1}}{2} \\ q_{\beta 1} & \frac{q_{\beta 2}}{2} & q_0 - \frac{q_{\alpha 2}}{2} & -\frac{q_{\beta 1}}{2} & \frac{q_{\alpha 1}}{2} \\ q_{\alpha 2} & \frac{q_{\alpha 1}}{2} & -\frac{q_{\beta 1}}{2} & q_0 & 0 \\ q_{\beta 2} & \frac{q_{\beta 1}}{2} & \frac{q_{\alpha 1}}{2} & 0 & q_0 \end{bmatrix}_{5\times 5} \tag{A-27}$$

TIMF model can be applied to the state-space model of PWM dc-dc converters expressed in equation (2-1) by substituting equations (A-15), (A-20), (A-21), and (A-26) in the general state space equation (2-1). Because of the presence of the time varying coefficient vector **c** in all terms, one can omit it from both sides of the resulting equations to determine the TIMF model. As a simple rule for transferring state space model to TIMF model, one can easily use Table. A-1.

Another important issue related to closed loop DC-DC converters is feedback modeling. Mostly in DC-DC converters as assumed here proportional-integral (PI) controller has been employed. In the voltage control mode, the error between output voltage and reference voltage has been used for controlling circuit. Thus duty cycle command can be calculated as follows:

$$d(t) = k_P(v_{ref} - v_{out}(t)) + k_i\int(v_{ref} - v_{out}(t))dt \qquad \text{(A-28)}$$

where v_{ref}, $v_{out}(t)$, k_p, k_i and $d(t)$ are reference voltage, output voltage, proportional coefficient, integral coefficient and duty cycle command respectively. One can find TIMF modeling by substituting Fourier series representation of all time dependent functions of equation (2-36), namely, output voltage and duty cycle command. Thus

$$\begin{aligned} d_0 + \sum_{n=1}^{N} d_{\alpha n}\cos(n\omega_s t) + d_{\beta n}\sin(n\omega_s t) &= k_p(v_{ref} - v_{out-0}) + k_i\int(v_{ref} - v_{out-0})dt \\ &+ k_p\left(\sum_{n=1}^{N} -v_{out-\alpha n}\cos(n\omega_s t) - v_{out-\beta n}\sin(n\omega_s t)\right) \\ &+ k_i\left(\sum_{n=1}^{N} -\frac{v_{out-\alpha n}}{n\omega_s}\sin(n\omega_s t) + \frac{v_{out-\beta n}}{n\omega_s}\cos(n\omega_s t)\right) \end{aligned} \qquad \text{(A-29)}$$

One can determine the FSR coefficients of duty cycle command by equaling all the same frequencies in the left side to right side of above-mentioned equation.

Table A-1. Rules of converting state-space model to TIMF

Rule	Example
$x \to \mathbf{x}$	$i_L \to \mathbf{i}_L$
$\frac{dx}{dt} \to -\mathbf{\Omega x} + \frac{d\mathbf{x}}{dt}$	$\frac{di_L}{dt} \to -\mathbf{\Omega i}_L + \frac{d\mathbf{i}_L}{dt}$
$q \to \mathbf{Q}$	$(1-q) \to (\mathbf{I}_{2N+1} - \mathbf{Q})$
$z \to \mathbf{z}$	$v_d \to \mathbf{v}_d = \begin{bmatrix} v_d & 0 & \cdots & 0 \end{bmatrix}^T$

A.2. Thermal FEM simulation

For validating the analytic model mentioned in section 2-3-1, some simulations have been performed in ABAQUS environment based on finite element method (FEM). Four different materials have been used in this simulation for IGBT and diode. Aluminum for heat sink, copper for lead frame, tin and silver (Sn-Ag-Cu) for solder (die attach) and silicon for chip (die) [213]. Three main parts are only integrated in the chip, namely, leadframe, soldering and die. These layers have been shown in Fig. A-2 as a macro image. Although, bonding wires are included, for simpilicity in the thermal analysis they have not been taken into account without losing accuracy [219]. The area of the chip is estimated to be 3×5mm. The height of die, solder and leadframe are approximately 300µm, 60µm and 1280µm, respectively.

General and thermal characteristics of these materials are listed in Table. A-2. Regarding this table, one can easily find that copper, aluminum and silicon all have temperature-dependant thermal conductivities. Thanks to the ABAQUS environment, this dependency can be easily applied in the simulation. With regard to Fig. 2-16 and material properties listed in Table. A-2, simulations have been performed in ABAQUS environment. A surface heat flux source ($36W/(3\times5)mm^2 = 2.4\times10^6\ W/m^2$) equals to 36W is applied to the top face of the IGBT die and another ($17.4W/(3\times5)mm^2 = 1.16\times10^6\ W/m^2$) equals to 17.4W is applied to the top face of the diode chip.

Table A-2. Material general and thermal properties [211], [216], [219]

Material	Density (kg/m³)	Specific heat (J/kg°C)	Thermal conductivity (W/m°C)	
			Temperature (°C)	Conductivity
Silicon	2330	705	0	168
			100	112
			200	82
Copper	8954	384	0	401
			100	391
			200	389
Aluminium 6061	2700	896	0	167
			100	189
			200	195
SnAgCu	7370	220	all	57
Thermal pad	2300	1000	all	5

Both chips are assumed to be adiabatic from top. Ambient temperature surrounding the heat sink is assumed to be 40°C and the wall temperature has been considered to be 140°C, respectively. All the convective heat transfer coefficient and radiation coefficient are those which were obtained from Table 2-3. Meshes' size are automatically chosen based on the optimizing tool in ABAQUS. Optimization module in ABAQUS environment is an especial tool for optimizing the meshes' size and type

in order to make convergence and increase accuracy level. Complete explanation of these tools is beyond this study and interested reviewers refer to ABAQUS online user manual. The static results are shown in Fig. A-3. Temperature distribution shows that above-mention heat sink design and analysis has been completey validated. The maximum temperature 169.1℃ is occurred in IGBT chip as predicted and it is about the maximum allowable temperature (170℃).

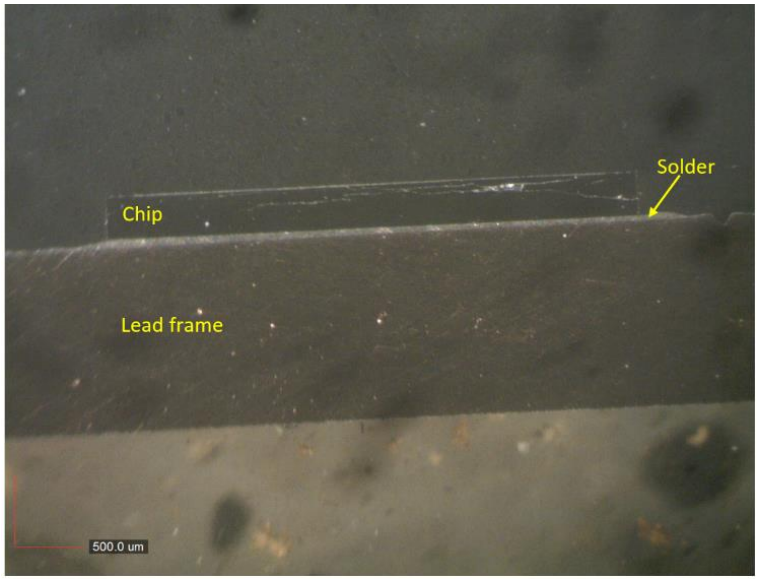


Fig. A-2. IGBT/diode layers.

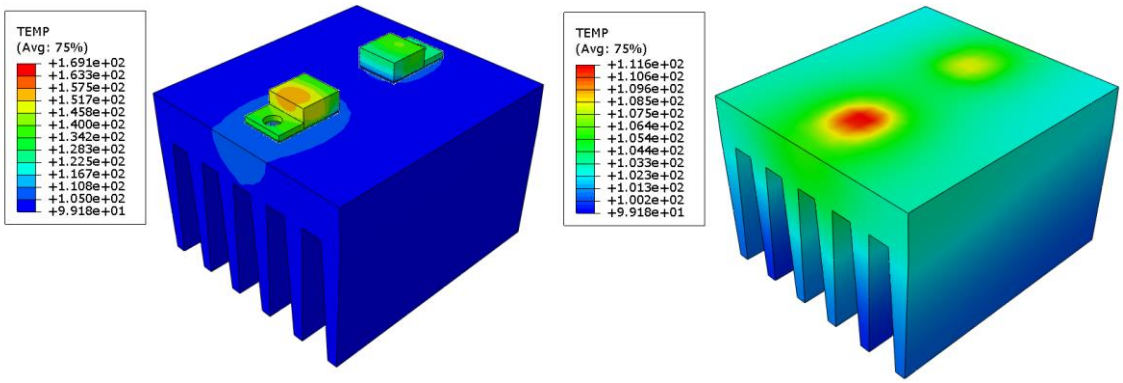


Fig. A-3. Simulation results in ABAQUS environment based on analytic manipulations

B. Creep Behavior

B.1. FEM simulation

ABAQUS finite element environment was used to investigate the induced strain in the power semiconductor chip. The meshed geometric model of the assembly is presented in Fig. B-1. The mesh of assembly includes 53424 elements and 70128 nodes. Several parts with the different physical and geometrical properties existed in the power semiconductor assembly. Therefore different material and physical properties have to be considered. These properties are listed in Table B-1 [147]. Joint zone consists of The SAC solder layer, Cu baseplate and Si wafer. Considering the thermal expansion coefficients of the mentioned parts, contraction and expansion of these materials during thermal cycle are undoubtedly expected.

The solder layer in power semiconductor tolerates thermal cycling loading during accelerated thermal experiments similar to the conditions provided in the real application. Garofalo-Arrhenius constitutive model presents the deformation behavior of the solder layer (elastic and inelastic properties). Creep behavior of solder layer was modeled by the hyperbolic sine creep equation (equation (1-6)). The constant values were extracted from creep test (section 3-4) and are 2.73×10^5 (1/s), 0.023 $(MPa)^{-1}$, 6.3 and 6480.3 for C_1, C_2, C_3 and C_4, respectively.

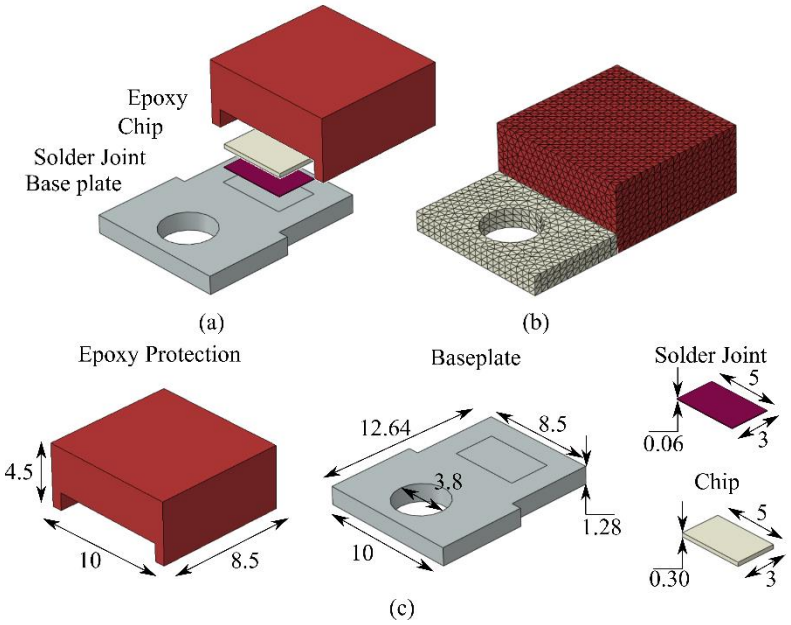


Fig. B-1. Discrete Power semiconductor, a) structure, b) meshed model and c) dimensions in mm.

One of the most important failure mechanisms for SAC solders during thermal cycling is creep. Thus, creep induced deformation can affect the lifetime of solder layer and propagate the cracks and the voids. Accumulated creep strain can be extracted using FEM simulation. The values of accumulated creep strain in a solder joint used to estimate the number of cycles to failure.

Table B-1. Properties of the parts in discrete chip

parts	E (GPa)	CTE (10^{-6}/°C)	Poisson's Ratio	Density ($\times 10^{-6}$kg/mm^3)
SAC	43	23.2	0.3	7.370
Si Chip	130	3.5	0.22	2.33
Cu baseplate	129	17	0.34	8.69
epoxy	3	75	0.42	0.3

Several accelerated thermal cycles based on what explained on section 3-3 were used in the FEM simulations. The temperature loading started from -40°C, increased up at a rate of 4°C/min up to 170°C and then a hot dwell time of 20 min at the peak of cycle was applied. The temperature was then decreased to -40°C at the rate of -3°C/min. There is a cold dwell time of 20 min in the cold peaks.

B.2. Results and discussion

Creep deformation in Sn-base solder such as Sn3.5Ag0.5Cu plays a major role in lifetime estimation of power semiconductors. The creep accumulated strain, strain energy and stress distributions are illustrated in Fig. B-2. It is found that the minimal strain occurs in the middle of solder joint and it rises towards the corner of joint. The case is also true for the strain energy and stress distributions. This corner accumulated strain/energy/stress is also reported in [147]. It is also experimentally reported that the crack initiated at the corner of solder joint and propagated into the center of the solder [147]. Fig. B-3 gives the evolution of accumulated creep strain as a function of thermal cycle numbers. The plot indicates that the increase in number of cycles leads to a growing trend in creep strain of solder joint. The sharp incline at the beginning of plot is sign of primary creep stage in the solder material, while the steady-state stage with a constant strain rate comes into play with the increase in the number of thermal cycles.

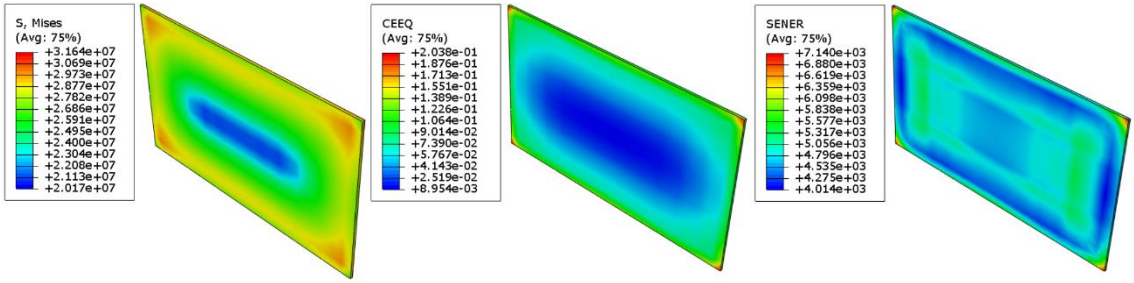


Fig. B-2. Accumulated strain, strain energy and stress distributions in the solder joint.

Von-Mises stress as a function of time (number of thermal cycle) is depicted in Fig. B-4 (a few last cycles). There are 5 different phases in this plot which they individually demonstrate a physical behavior occurring in the material. The phases 1 and 2 happens in the heating up phase from -40 °C to 170°C. At these phases, stress relaxation is dominant but much slower at the phase 2. The reason is due to the considerable difference in the coefficients of thermal expansion (CTE) of the solder layer, chip and the baseplate making a residual stress in the materials. The effects of

staying in the hot dwelling time shows itself as a relaxed stress due to the high temperature exposure and the generation of creep strain (phase 3). In the cooling down phase (phase 4) the solder layer tolerates an enormous stress shock intensifying the failure. The solder experiences another relaxing stress in the cold dwelling time (phase 5).

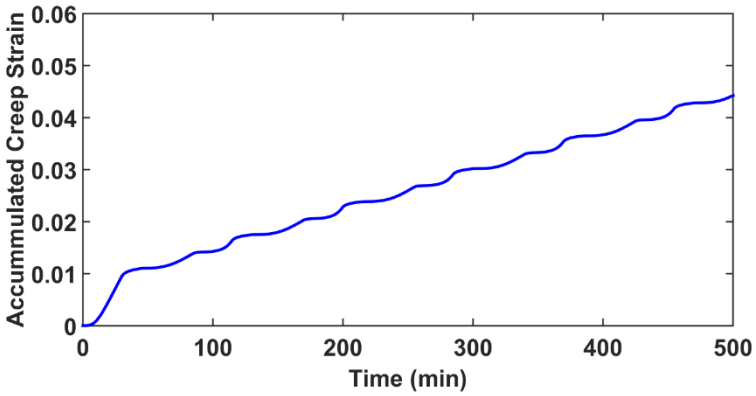


Fig. B-3. Accumulated creep strain in solder joint.

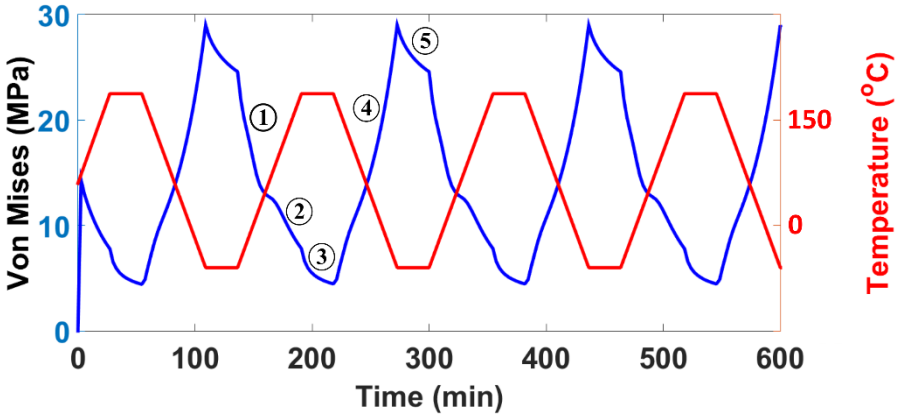


Fig. B-4. Von-Mises stress in solder joint.

Résumé long en Français

À l'échelle mondiale, l'utilisation de combustibles fossiles génère des dommages irréparables à notre environnement et perturbe l'équilibre écologique. Il n'est pas possible de continuer ainsi sans envisager des conséquences désastreuses. Il semble donc essentiel de développer des sources d'énergie alternatives et des véhicules entièrement électriques voire hybrides. Les énergies renouvelables et l'utilisation des véhicules électriques sont une réelle opportunité mais, en raison de l'incertitude inhérente aux ressources énergétiques renouvelables et aux diverses conditions de fonctionnement des véhicules électriques, des conditionneurs d'énergie performants sont nécessaires pour fournir l'énergie demandée. Dans ce contexte, les chercheurs repoussent chaque jour les frontières de la connaissance des convertisseurs d'électronique de puissance. Exploiter la technologie de manière créative pour concevoir des convertisseurs statiques fiables est aujourd'hui d'une réelle importance. La fiabilité des convertisseurs de puissance est maintenant connue pour être une thématique majeure dans le domaine de l'électronique de puissance.

Suite à un premier chapitre qui fait un état des lieux des différentes méthodes utilisées en fiabilité pour l'électronique et l'électronique de puissance, cette thèse présente de nouvelles méthodes d'évaluation de la fiabilité et tente de démontrer l'intérêt d'utiliser une analyse basée sur des systèmes dégradés à plusieurs états ou une analyse par intervalles afin d'atteindre beaucoup plus de précision dans l'évaluation de la durée de vie des convertisseurs statiques. La prise en compte des effets de dégradation des éléments sur l'estimation de leur propre durée de vie ainsi que sur la durée de vie des autres composants du système est une problématique peu voire pas abordée dans la littérature scientifique. L'objectif de cette thèse est d'envisager une prise en compte de tous ces phénomènes et permet d'aller vers une analyse de fiabilité qui se veut plus système.
L'analyse de fiabilité par intervalles est capable d'estimer un intervalle de durée de vie pour les convertisseurs DC-DC dans lesquels les effets d'auto-dégradation et de dégradation couplée ont été pris en compte. Fondamentalement, il s'appuie sur la physique des défaillances classique. Sur la base de cette méthode, au lieu d'obtenir une valeur de durée de vie imprécise, il est possible d'obtenir un intervalle de fiabilité d'un système global dont la durée de vie utile se situe entre les limites calculées. Cette méthode est capable de prendre en compte les dépendances à la dégradation et d'évaluer la fiabilité au niveau système multi-composants mais ne fonctionne pas avec les systèmes redondants.
Une autre tentative a été proposée pour améliorer l'analyse de fiabilité conventionnelle afin de parvenir à une approche systématique capable d'estimer la durée de vie en tenant compte des effets de dégradation propres et mutuels, et d'être

capable d'évaluer la fiabilité au niveau du système. L'analyse de la fiabilité d'un système dégradé à plusieurs états est ainsi capable d'estimer la fiabilité au niveau du système, tout en tenant compte du profil de mission et de la physique de la défaillance des éléments du système. En outre, les effets de dégradation individuels et mutuels des éléments sur le fonctionnement du système complet ont été pris en compte. Le modèle de fiabilité de système dégradé multi-états exposé à de multiples processus de défaillance a été généralisé. La condition de fonctionnement du système global est définie par un nombre fini d'états. Le cadre proposé peut non seulement être utilisé pour déterminer la fiabilité des systèmes dégradés en termes de fonctions multi-états, mais peut également permettre d'obtenir les états des systèmes en estimant les probabilités d'état du système.

Les composants les plus fragiles du système de conversion de puissance sont les composants semi-conducteurs de puissance et les condensateurs de puissance. Les composants semi-conducteurs de puissance discrets, en particulier les IGBT et les diodes de puissance, sont exposés à des variations de température en raison de leurs pertes ou de la variation de la température environnementale. Deux mécanismes de défaillance les plus fréquents, à savoir la fatigue électro-thermomécanique et le fluage, peuvent se produire en différents points du boîtier. Il peut s'agir des fils de liaison (wire bonding), de la métallisation en aluminium et de la brasure en face arrière. Ces détériorations entraînent finalement une dérive des paramètres thermiques et électriques des semi-conducteurs de puissance et accélère par la suite leur vieillissement. Dans le cas des condensateurs de puissance, les variations de la résistance série (ESR) et de la capacité peuvent entraîner un changement de point de fonctionnement et par conséquent un vieillissement accéléré du condensateur.
Au fil du temps, il est clair que le processus de dégradation d'un composant ou d'un système peut être accéléré en raison du vieillissement. En conséquence, l'évaluation de la fiabilité statique n'est pas en mesure d'estimer la fiabilité d'un système et une évaluation dynamique de la fiabilité semble être nécessaire. Pour atténuer le problème de l'évaluation de la fiabilité au niveau du système, il convient de prendre en compte les effets de dégradation individuels (dépendances), le niveau de dégradation (états) et le profil de la mission.

Dans le chapitre 2, un convertisseur DC/DC de type boost contenant trois éléments critiques est étudié. Dans cette étude de cas, deux semi-conducteurs de puissance, à savoir un IGBT et une diode, et un condensateur de puissance sont considérés comme trois processus de dégradation et leurs effets de vieillissement sur l'estimation de la durée de vie utile du système électronique de puissance sont discutés. Pour avoir une idée du cadre d'étude proposé, un convertisseur DC/DC classique de 3000W (200V/400V) pour les applications de véhicules électriques exposés à un cycle de conduite WLTP est considéré. Sa modélisation électrique est

basée sur un modèle multifréquence invariant dans le temps dans lequel les comportements électriques d'un convertisseur de puissance continu-continu ont été extraits avec précision. La modélisation des pertes est réalisée sur la base d'une modélisation conventionnelle. Une modélisation thermique complète du convertisseur de puissance considéré est également discutée sur la base d'approches analytiques et de simulation.

Pour la collecte de données, des tests de cyclage thermique (ATC) et de cyclage actif (APC) de semi-conducteurs de puissance ont été effectués et sont présentés dans le chapitre 3. Les résultats sont utilisés dans les chapitre suivants pour estimer la durée de vie du convertisseur étudié. Un prototype de convertisseur de puissance continu DC-DC boost capable de mesurer en temps réel la température de jonction a également été mis en œuvre pour étudier les effets de la dégradation mutuelle et de l'auto-dégradation des composants dus aux contraintes thermiques. Les résultats ont révélé l'importance des effets de couplage thermique dans le convertisseur de puissance considéré sur le vieillissement des composants.

Dans le chapitre 4, un algorithme de Rainflow modifié capable de compter simultanément les cycles de fatigue-fluage et de tenir compte de la température moyenne en fonction du temps et de la température a été proposé. Cet algorithme a été utilisé pour prendre en compte le profil de mission considéré dans l'évaluation de la fiabilité.

La partie principale du mémoire est le chapitre 5. Ce dernier présente une méthode d'évaluation de la fiabilité basée sur les systèmes dégradés multi-états. Son objectif est de résoudre les problèmes susmentionnés en divisant un système dépendant du temps (effet du vieillissement sur les composants) en plusieurs sous-systèmes indépendants. L'approche vise à résoudre les problèmes de dépendance en définissant des intervalles de dégradation intermédiaires. Au lieu de supposer qu'un système est dans un état parfait ou dans un état de défaillance, un système représenté par plusieurs états de dégradation intermédiaires (états imparfaits) a été défini. Les états imparfaits du système sont dépendants des états propres des composants. L'approche sépare deux catégories de composants à savoir les composants effectifs et composants non-effectifs. Ces derniers sont le siège de dégradations qui n'affectent pas le point de fonctionnement du système global contrairement aux autres. Etant donné que la durée de vie d'un convertisseur dépend du point de fonctionnement, les éléments effectifs ont un rôle sur la fiabilité globale du convertisseur de puissance.
La combinaison de divers états de composants imparfaits peut conduire à des états de système globaux imparfaits uniques. Les relations entre les états de dégradation des composants et les états du système ont été cartographiées à l'aide d'une matrice

de mappage appelée Hc. Les dimensions de cette matrice dépendent du nombre de composants effectifs inclus dans le système global. Le nombre de lignes, de colonnes et de pages est directement déterminé par le nombre d'états de dégradation individuels des composants. Plus il y a d'états considérés comme imparfaits pour les composants, plus l'évaluation de la fiabilité sera précise et plus le temps de traitement sera long.

Les processus de dégradation des composants individuels sont supposés être des distributions probabilistes permettant de prendre en compte les incertitudes de l'estimation. Les processus de dégradation de composants individuels peuvent être n'importe quelle fonction du temps et être extraits d'essais de vieillissement expérimentaux. Certaines valeurs seuil ont été définies pour distinguer les états imparfaits de composants individuels. Au fil du temps (vieillissement), les processus de dégradation passent d'un état sain à un état moins sain. Étant donné que les dommages sont supposés être cumulatifs et irréversibles, les états de dégradation ne peuvent aller que d'états plus sains et vers des états moins sains, et non l'inverse. Les processus de dégradation des composants ineffectifs peuvent avoir n'importe quel type de distributions probabilistes jusque à la dégradation. Ils n'interviennent pas sur les états de dégradation intermédiaires.

Le même convertisseur de puissance continu DC-DC boost a été étudié dans ce chapitre. Ce convertisseur comprend des composants actifs, un condensateur et une inductance. Étant donné que les composants les plus critiques dans l'évaluation de la fiabilité des convertisseurs de puissance sont les condensateurs et les composants actifs, il a été supposé que le système ne comportait que trois composants, à savoir un IGBT, une diode et un condensateur. Une expérience est présentée dans le chapitre 3 et est mise en œuvre pour étudier les dépendances des dégradations de composants individuels sur les points de fonctionnement thermique et électrique du système mondial dans un convertisseur de puissance boost continu DC-DC. Les résultats ont révélé que l'IGBT et la diode avaient des effets directs sur les points de fonctionnement thermique et électrique du système global. En outre, il a été observé également qu'il existe des effets d'auto-dégradation mutuelle entre ces composant, ce qui a tendance à accélérer le vieillissement des composants. En conséquence, deux composants effectifs, à savoir un IGBT et une diode, et un composant ineffectif, à savoir un condensateur, ont été pris en compte dans l'évaluation de la fiabilité du système global (convertisseur de puissance boost continu DC-DC).

Une défaillance du condensateur (diminution de sa capacité de 20% ou augmentation de son ESR de 100%) a directement entraîné la défaillance du système, tandis que les processus de dégradation des semi-conducteurs de puissance ont entraîné plusieurs états de système imparfaits différents. Cinq états de dégradation distincts ont été définis pour l'IGBT et la diode dans lesquels leurs résistances thermiques ont été augmentées de 5% jusqu'à atteindre le critère de défaillance (augmentation de 20% de la résistance thermique entre jonctions et

boîtiers). Des tendances de dégradation de l'état 4 à 0 ont été observées chaque fois que la résistance thermique de l'IGBT ou de la diode était comprise entre (1, 1,05), [1,05, 1,1), [1,1, 1,15), [1,15, 2] et supérieure à 1,2, respectivement. Les processus de dégradation de l'IGBT et de la diode ont été extraits des tests de vieillissement APC et ATC (cf chapitre 3). Les résultats ont révélé les tendances de la dégradation de l'IGBT et de la diode en termes de nombre de cycles. Pour convertir le nombre de cycles en temps, un cycle de conduite, à savoir le WLTP-class3, avec différents cycles d'une durée de 30 minutes a été appliqué aux résultats des tests de vieillissement APC et ATC. Cette conversion a permis de trouver les processus de dégradation de l'IGBT et de la diode en termes de temps. Les données étaient des fonctions linéaires par morceaux, à la fois pour l'IGBT et la diode, dans lesquelles la pente de ces fonctions linéaires par morceaux augmentait de manière stricte en raison de la réversibilité des dommages.
Le résultat de la durée de vie B_{10} a été estimé à 58040 heures pour le système électronique de puissance global. Cela signifie que le convertisseur de puissance continu-continu peut fonctionner avec une probabilité de 90% de fonctionnement correct pendant 58040 heures. Alors que, dans le cadre d'une évaluation de fiabilité classique, la fiabilité du B10 était de 66680 heures. Il en ressort que l'approche classique (qui ne permet pas d'évaluer la fiabilité au niveau du système) est trop optimiste en raison du manque de prise en compte des effets de dégradation mutuels et propres.

Les méthodes d'évaluation de la fiabilité proposées dans ce manuscrit constituent non seulement une approche systématique capable de s'appliquer aux différents convertisseurs d'électronique de puissance, mais permet également d'apporter des parades aux inconvénients des méthodes classiques en permettant de prendre en compte le profil de mission et les effets de dégradation mutuelle et propres sur les performances des convertisseurs de puissance.

Abstract

Reliable and unceasing exploitation of power electronic converters plays a major part in every application. This PhD thesis comes up with new opened-up reliability assessment frameworks and demonstrates the feasibility of using multistate degraded system analysis and interval analysis as well for attaining much more accuracy in reliability evaluation. Considering self- and coupling degradation effects of the items and assessing reliability in the system level are important issues which are still lacking in the previous studies and the present thesis has made an effort to overcome these problems. The thesis tries to launch two distinct reliability assessment frameworks, namely interval reliability and Multistate degraded system reliability.

Interval reliability is capable of introducing an interval useful lifetime for DC-DC power electronic converters in which the self and coupling degradations effects of items have been taken into account. Fundamentally, it is based on the conventional physics of failure reliability assessment. Based on this method, instead of obtaining an inaccurate reliability value, one can attain an interval for the reliability of a global system whose useful lifetime undoubtedly lays between the boundaries. This method is able to consider degradation dependencies and assess multi-component system level reliability but not redundant system. An attempt was made to enhance the conventional reliability framework to reach a systematic approach capable of estimating a reliability assessment considering self and mutual degradation effects and being able to evaluate system-level reliability including redundant system. Multistate degraded system reliability analysis is capable of estimating system-level reliability, while mission profile and physics of failure of the system's items are taken into account. In addition, the self and mutual degradation effects of items on the operation of the global system have been considered. The multi-state degraded system reliability model exposed to multiple failure processes has been generalized. The operating condition of the global system is defined by a finite number of states. Not only can the proposed framework be employed in determining the reliability of the degraded systems in terms of multi-state functions, but also it can obtain the states of the systems by estimating the system state probabilities.

As an application, a DC-DC power electronic system containing three critical items has been studied. In this case study, two power semiconductors, namely IGBT and diode, and a power capacitor have been considered as three degradation processes and their aging effects on the useful lifetime estimation of the power electronic system have been discussed. For having a sense about newly proposed reliability frameworks, a 3000W and 200/400 V conventional DC-DC converter for electric vehicle application exposed to WLTP driving cycle is considered.

Résumé

La fiabilité et la sureté de fonctionnement de l'électronique de puissance jouent un rôle majeur aujourd'hui dans l'industrie. Cette thèse propose un nouveau cadre d'étude de la fiabilité à partir de deux méthodes afin d'améliorer la précision des études de fiabilité : une analyse utilisant la méthode des système dégradés multi état, et une analyse par intervalles. La considération des effets de dégradation propres et couplés de chaque composant est également une problématique qu'il reste aujourd'hui à étudier et qui est traitée dans ce travail.

L'étude de la fiabilité par intervalles permet d'estimer des intervalles de durée de vie des convertisseurs DC/DC en prenant en compte les dégradations propres et mutuelles des composants. Fondamentalement, cette méthode est basée sur la compréhension des phénomènes physiques. A partir de cette méthode, on peut obtenir un intervalle pour la durée de vie d'un système complet. Cette méthode n'est toutefois pas adaptée aux systèmes redondants.

De son côté, la fiabilité des systèmes dégradés multi-états est capable de proposer une étude au niveau système en prenant en compte le profil de mission et la physique des dégradations. Cette méthode a été généralisée dans cette thèse au procédés subissant de multiples dégradations.

L'exemple d'un convertisseur DC/DC conprenant trois composants critiques a été étudié comme cas d'application. Deux composants semiconducteurs, diode et IGBT, et un condensateur sont considérés comme trois process de dégradation et l'effet de leur vieillissement sur la durée de vie du convertisseur est discutée. Le convertisseur étudié a pour puissance 3 kW (200/400V) et est dédié aux applications de type véhicule électrique. Il subit un profil de mission typique automobile (cycle WLTP).