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Communauté UNIVERSITÉ Grenoble Alpes

THÈSE

Pour obtenir le grade de

DOCTEUR DE LA COMMUNAUTE UNIVERSITE GRENOBLE ALPES

Spécialité : **Génie Electrique**

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Présentée par

Mylène Delhommais

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préparée au sein du **Laboratoire G2ELab**
dans **l'École Doctorale EEATS**

Méthode de Pré-design par Optimisation en Electronique de Puissance

Preliminary Design Method in Power Electronics

Thèse soutenue publiquement le **« 28 Mars 2019 »**,
devant le jury composé de :

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Abstract

When a designer of power electronics systems is involved in a pre-design process, i.e. the definition of the system specifications, he/she has to overcome several difficulties. The first is to find, based on its experience and literature, all the architectures, conversion topologies and component technologies that can meet the needs of the system.

From this list of possibilities, the designer must eliminate a certain number of them via qualitative or quantitative arguments until only a small number remains. It is essential for the designer that he/she knows the design limits of each remaining choices to define with certainty the product development plan and the future design issues to be solved. In other words, it must define the correct problem formulation.

Having a method to achieve this objective with confidence and on schedule is highly desirable. This is the purpose of this thesis.

We therefore propose a new approach based on preliminary design by optimization in the continuous (imaginary) world of power electronics systems. The proposed method uses an optimization algorithm based on the calculation of the gradient of the system model. This algorithm allows to manage a very large number of design parameters, in other words to explore a wide range of solutions in the imaginary world. It therefore requires continuous and differentiable models of power electronics systems with continuous (imaginary) optimization variables despite the discrete nature of the components used in electronics.

The present thesis work has thus consisted in proposing continuous and derivable optimization models of an interleaved Buck converter used in an aircraft called "Stratobus" and validating these optimization models by an experimental approach on a complete prototype. These models have then been used for the pre-dimensioning of this converter as part of the Stratobus project. Firstly a study on the conduction mode and magnetic materials minimizing the mass of the converter has been performed. And then the impact of variation of the specifications on the mass of the converter has been analyzed. Finally, since the converters are built from electronic components chosen off the shelf, a discretization procedure has been set up to return to the real world.

Key word: Optimization – Power Electronics – Pre-design – Aeronautical

Résumé

Lorsqu'un concepteur de systèmes d'électronique de puissance est engagé dans un processus de pré-design, c'est-à-dire la définition du cahier des charges du système, il doit surmonter plusieurs difficultés. La première étant de trouver grâce à son expérience et à la littérature, toutes les architectures, topologies de conversion et technologies de composants susceptibles de répondre aux besoins du système.

A partir de cette éventail, le concepteur doit en éliminer un certain nombre via des arguments qualitatifs ou quantitatifs jusqu'à ce qu'il n'en reste plus qu'un nombre très restreint. Il est primordial pour le concepteur que parmi les choix restant, celui-ci en connaisse les limites de design pour définir avec certitude le plan de développement du produit et les problématiques futures à résoudre. En d'autres termes, il lui faut définir la juste formulation du problème qui lui est posée.

Posséder une méthode lui permettant d'atteindre cet objectif en toute confiance et dans les délais impartis est fortement désirable. Ceci est l'objet de cette thèse.

Nous proposons donc une nouvelle approche basée sur le pré-dimensionnement par optimisation dans le monde continu (imaginaire) de systèmes d'électronique de puissance. La méthode proposée utilise en effet un algorithme d'optimisation basé sur le calcul du gradient du modèle du système. Cet algorithme permet de gérer un très grand nombre de paramètres de design, autrement dit permet d'explorer un large éventail de solutions dans le monde imaginaire. Il nécessite donc des modèles de systèmes d'électronique de puissance continus et dérivables avec des variables d'optimisation continues (imaginaires) malgré le caractère discret des composants utilisés en électronique.

Les présents travaux de thèse ont donc consistés à proposer des modèles d'optimisation continus et dérivables d'un convertisseur Buck entrelacé utilisé dans un aéronef appelé « Stratobus » et à valider ces modèles d'optimisation par une démarche expérimentale sur un prototype complet. Ces modèles ont ensuite été utilisés pour le pré-dimensionnement de ce convertisseur dans le cadre du projet Stratobus permettant dans un premier temps une étude sur le mode de conduction et les matériaux magnétique minimisant la masse du convertisseur, puis une analyse de l'impact de variation de cahier des charges sur la masse du convertisseur. Enfin, les convertisseurs étant construits à partir de composants électroniques choisis sur étagère, une procédure de discrétisation a été mise en place pour revenir au monde réel.

Mots clés : Optimisation – Electronique de puissance – Pré-design – Aéronautique

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I would like to underline the deep investment of my thesis directors Jean-Luc and Fred and Tronico's supervisors Cécile and Sylvain. I particularly enjoyed all the discussions we had for making a meaningful and coherent thesis according to academic and industrial needs. It was a real pleasure to work with all of you. I even more enjoyed the time we spent outside of work!

Thanks to Tronico's management for trusting its engineers and letting them be innovative.

This work could not have been possible without my colleagues. Especially the Gronicois that supported me these last 3 years, the technicians that helped me (Jennifer and Loïc for the prototype layout, Edyta for the BOM, Cyrille for the inductor samples), Maryline for the daily help and to the engineers such as Jonathan and Valentin that were open-mind to new design methods.

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Cảm ơn bạn Anh Dao et merci aux ladies 2000 (#Lucie#Pauline#Ambre) pour être des soutiens indéfectibles.

Merci aussi à mon Doudou d'amour pour tes encouragements sur cette fin de thèse et d'être à mes côtés chaque jour, chose qui me remplit de bonheur !

Glossary of abbreviations

Abbreviation	Signification
μ	Fluid dynamic viscosity
CADES	Component Architecture for Design of Engineering Systems (optimization framework)
Cal_Idiode	SiC 1200 V Schottky diode current rating
Cal_Imos	SiC 1200 V MOSFET current rating
CCM	Continuous Conduction Mode : conduction mode of a converter
CD	Conduction mode
C_D	Diode junction capacitance
C_{GD}, C_{GS} & C_{DS}	MOSFET junction capacitances
Chigh	Input single capacitor value
C_L or CL	Phase inductor capacitance
Clow	Output single capacitor value
COTS	Commercial Off-The-Shelf: components taken in manufacturer catalogs
d	Command delay between the MOSFETs of each phase
DC	Optimization variable that indicates the conduction mode of the converter (=1 if DCM, =0 if CCM)
DCD	Diode conduction duration
DCM	Depends on the context: either Discontinuous Conduction Mode of the converter, either Duty-Cycle of the MOSFET
Dh	Hydraulic diameter
DIL	Current ripple in the phase inductor
Din	Inductor core internal diameter
$Dlitz_{ext}$ or Dlitz_ext	External diameter of the Litz wire
DlitzLphase	Litz strand diameter of the phase inductor
Dout	Inductor core external diameter
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interferences
Fs	Switching frequency
H	Inductor core height
HVPCU	High Voltage Power Conditioning Unit (set of the DC-DC converters of Stratobus between solar panels and DC power bus)
IBC	Interleaved Buck Converter
ID or I_D	Diode current
IDmoy	Average current in the diode
IDrms	Diode RMS current
Ihigh	Input current of the IBC
IL or I_L	Phase inductor current

Abbreviation	Signification
Ilow	Output current of the IBC
IQ or I_Q or I_{DS} or Ids	MOSFET drain current
IQrms	MOSFET RMS current
Lcrit	Critical value of the phase inductor to be on the limit of the continuous or discontinuous conduction mode
Ld or L_D	MOSFET drain inductance of the switching cell
Lhigh_max	Input single filtering inductor value @ 0A
Llow_max	Output single filtering inductor value @ 0A
Ls or L_S	MOSFET source inductance of the switching cell
material	Inductor core material
N_Chigh	Number of input capacitors in parallel
N_Clow	Number of output capacitors in parallel
NA	Not Applicable
NBphase or Nb_phase or Nphase	Number of phase of the IBC
Nbunching	Number of bunching operations for the Litz wire
Ncabling	Number of cabling operations for the Litz wire
Np_Lhigh	Number of input inductors in parallel
Np_Llow	Number of output inductors in parallel
Ns_Lhigh	Number of input inductors in series
Ns_Llow	Number of output inductors in series
nstrandLphase	Litz number of strands
NturnsLphase	Phase inductor number of turns
Nu_{exp}	Experimental Nusselt numer
$Nu_{predict}$	Predicted Nusselt numer
OP	Operating point
PCB	Printed circuit board
$Pcond^{diode}$	Diode on-state losses
$Pcond^{MOSFET}$	MOSFET on-state losses
PDR	Preliminary Design Review (design phase milestone)
Phigh	Input power of the IBC converter
Pr	Prandt number
PWM	Pulse Width Modulation
Q	Fluid flow rate
RacLitz	AC resistance of the Litz wire
RdcLitz	DC resistance of the Litz wire
Rds_{on}	On-state resistance of the MOSFET
Re	Reynolds number
R_G	Gate resistance of a MOSFET
RMS	Root Mean Square

Abbreviation	Signification
Rs	Linear resistance of a strand
Rt	Diode on-state resistance
Rth	Thermal resistance of a device/material
S	Thermal exchange surface of a device/material
SiC	Silicon Carbide
SML	System Modeling Language (CADES specific)
SQP	Sequential Quadratic Programming (gradient based optimization algorithm)
SRR	System Readiness Review (design phase milestone)
TBD	To Be Defined
THD	Total Harmonics Distortion
Tj	Junction temperature of a semiconductor
T_{Oscill}	Period of the oscillations that appear on diode, MOSFET and phase inductor voltages in DCM
Ts	Switching period
VD or V_D	Diode voltage
Vhigh	Input voltage of the IBC
VL or V_L	Phase inductor voltage
Vlow	Output voltage of the IBC
VQ or V_Q or V_{DS} or Vds	MOSFET drain-source voltage
Vt	Diode threshold voltage
α	Fluid coefficient (0.33 for water) for $Nu_{predict}$
ΔT_{exp}	measured temperature difference between the heated wall and the bulk fluid
$\eta_{computed}$	Computed converter efficiency (optimization output variable)
η_{des}	Desired converter efficiency (optimization input variable)
λ or k	Material thermal conductivity
ρ	Fluid volume density
σ_H	Coefficient about the proportions of the inductor core geometries (on height)
σ_{in}	Coefficient about the proportions of the inductor core geometries (on internal diameter)
σ_{turns}	Coefficient about the proportions between the inductor actual number of turns and maximum number of turns
φ_{exp}	Heat flux

Résumé en Français

Partie A : Enjeux et solution proposée pour relever le défi de la phase de conception préliminaire des systèmes électroniques de puissance

Chapitre 1: Processus de conception actuel en électronique de puissance

L'électricité est le vecteur énergétique préconisée par les scientifiques pour faire face à l'un des plus grands défis de l'humanité qu'est le réchauffement climatique et donc la réduction d'émission de CO_2 dans l'atmosphère. Cela signifie que les besoins de système d'électronique de puissance pour contrôler et convertir l'énergie électrique continueront de grandir dans les prochaines décennies.

Mais un convertisseur statique n'assurant pas une fonction finale mais seulement une fonction partiel d'un système, les contraintes de design sont souvent très fortes. Par exemple, son rendement doit s'approcher de 100% pour être transparent dans les calculs d'efficacité énergétique des systèmes, et ce dans un volume et un poids minimaux.

Pour définir un cahier des charges réalisable d'après les exigences des intégrateurs systèmes, les concepteurs d'électronique de puissance suivent un processus de pré-design comme présenté par la Figure *1*.

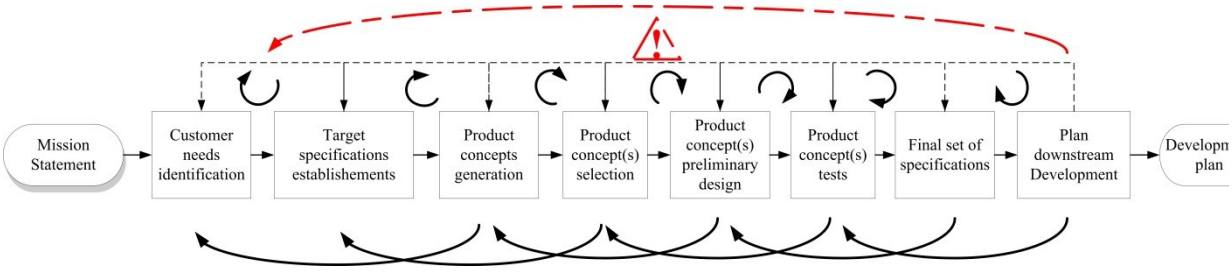


Figure *1*: Processus de pré-design selon Ulrich and Eppinger

Cette phase de pré-design est très importante puisqu'elle influence 90% du coût du développement du convertisseur dans la phase de conception détaillée Figure *2*. **Cette phase de préconception ne doit pas être négligée.**

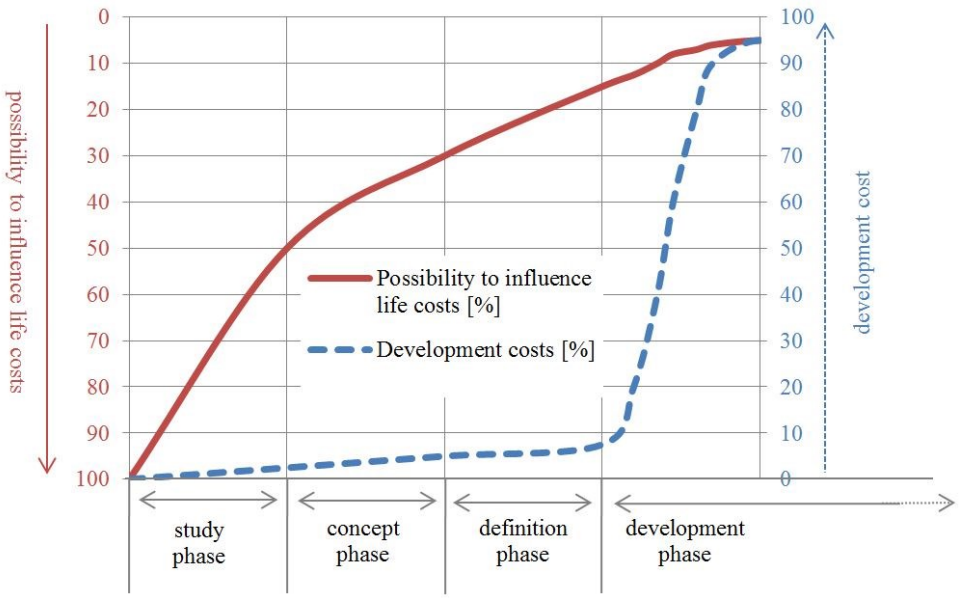


Figure *2*: Effet de levier sur le coût du développement du produit selon Zablit et Zimmer

Selon Kline et Schindel, les conceptions qui aboutissent à un produit coûteux sont parfois dues à des raccourcis pris par concepteurs : ils ne recueillent pas assez d'information ou la bonne information avant de commencer à concevoir, ils ne se concentrent que sur une ou quelques idées ou ils suivent un chemin linéaire simple ou d'autres processus infructueux lors de la conception.

Ce constat fait échos avec le paradoxe du processus de design qui est que le nombre de degrés de liberté du concepteur diminue avec l'accroissement des connaissances du systeme lors de l'avancement dans le design.

Le domaine de l'électronique de puissance a, qui plus est, la particularité d'être intrinsèquement très discrétisé puisque les convertisseurs statiques sont principalement constitués de composants électroniques choisis sur catalogue. Mais il existe peu de méthodes et d'outils pour cette phase de pré-design dans ce domaine (contrairement aux méthodes de design sur un cahier des charges fixé largement étudiées dans la littérature).

Chapitre 2: Une nouvelle approche pour la conception préliminaire de l'électronique de puissance

En électronique de puissance le concepteur doit sélectionner l'architecture puis la topologie puis les technologies à utiliser dans son système. Parce que le choix est grand, le nombre de branches de l'arbre des propositions techniques possibles peut très vite exploser (Figure *3*). Le nombre de choix possible peut diminuer à l'aide d'arguments qualitatifs mais parmi les choix restants, les données quantitatives sont indispensables.

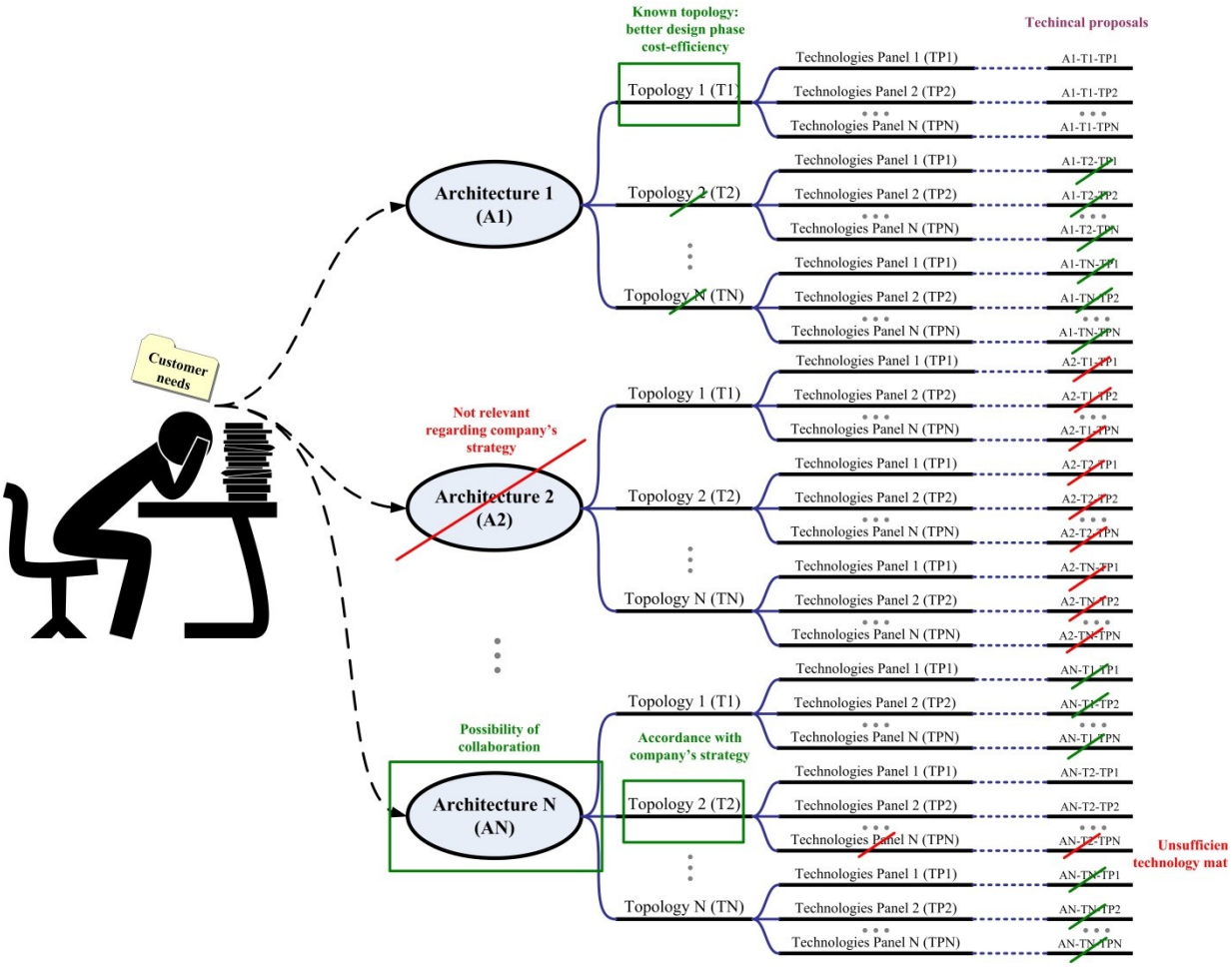


Figure *3*: Arbre de propositions techniques possibles pour un cahier des charges donné

Afin de fournir ces données, une nouvelle méthode de pré-design qui a la capacité d'explorer rapidement un large éventail de solutions pour chaque proposition et de les comparer objectivement (c'est-à-dire optimisées selon les mêmes critères) permettrait d'aider les designers dans cette phase.

C'est pourquoi, afin de répondre à la problématique de conception préliminaire de systèmes d'électronique de puissance, nous proposons une nouvelle approche basée sur l'algorithme d'optimisation par gradient SQP qui est capable de gérer jusqu'à quelques centaines de paramètres de conception et correspond donc plus ou moins à la

taille du problème de pré-dimensionnement d'une alimentation à découpage. Elle a l'inconvénient de ne pas pouvoir traiter des paramètres discrets : toutes les variables de conception doivent être continues et les modèles dérivables. Malheureusement pour les concepteurs d'électronique de puissance qui travaillent avec des composants discrets, tout algorithme (heuristique ou énumération) ou technique (branche & bound) capable d'utiliser des variables discrètes est nécessairement moins efficace pour des problèmes d'optimisation importants et fortement contraints. Cette approche consiste donc à optimiser chaque proposition technique avec des variables continues et non discrètes dans le monde imaginaire décrit par la Figure 4.

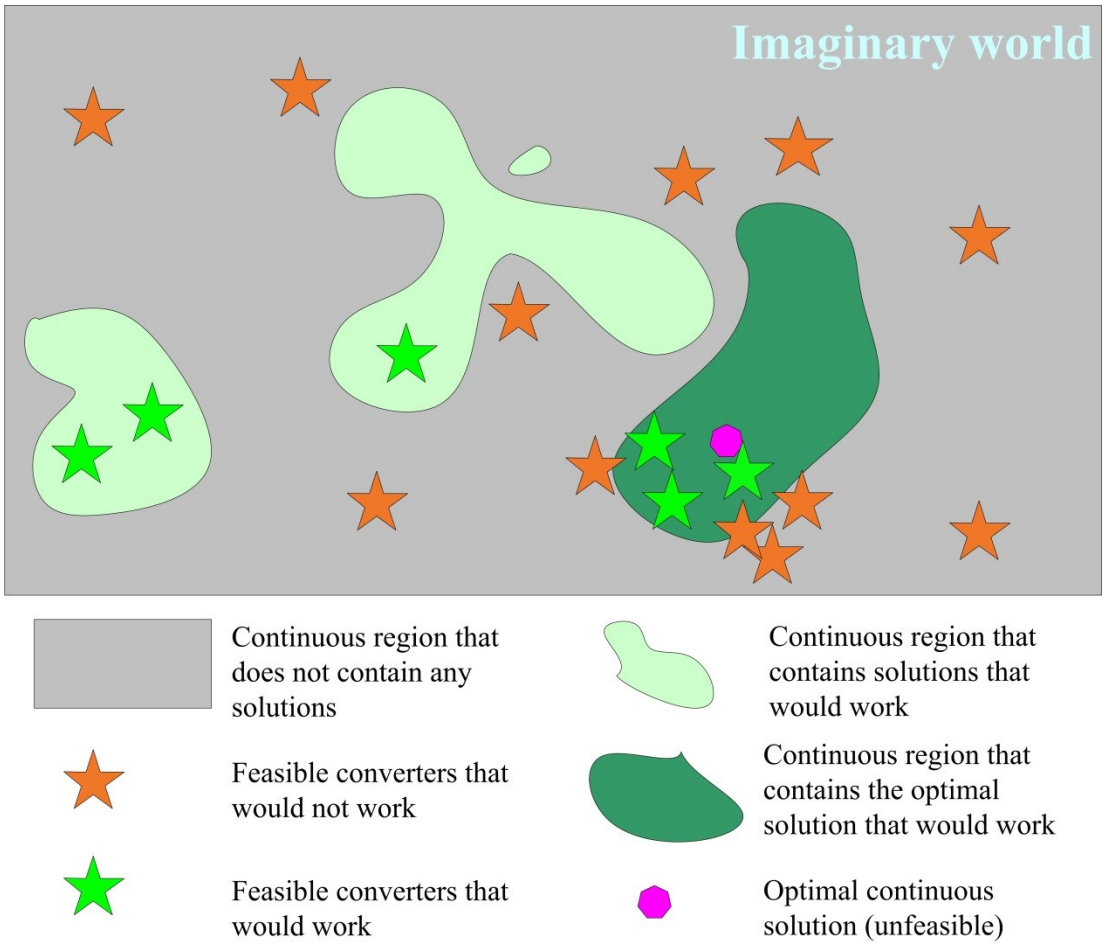


Figure 4: Illustration du monde imaginaire des convertisseurs statiques

Elle est résumée par la *Figure 5* : le processus commence par la formulation du problème d'optimisation et la modélisation du système. L'analyse des résultats de l'optimisation dans le monde imaginaire permet de modifier et corriger la formulation du problème. Lorsque celle-ci est figée, des optimisations paramétrées en fonction des paramètres du cahier des charges et des fronts de Pareto permettent aux designers de dialoguer et négocier le cahier des charges rapidement, i.e. lorsque le degré de liberté dans la conception est encore important. Lorsque le systémier et l'intégrateur système se sont mis d'accord sur un cahier des charges, les concepteurs peuvent utiliser

un processus de discrétisation de la solution imaginaire du cahier des charges. Cette discrétisation permet notamment de définir rapidement les propriétés du convertisseur réel (fabricable) et de définir les axes de travail lors de la phase de design.

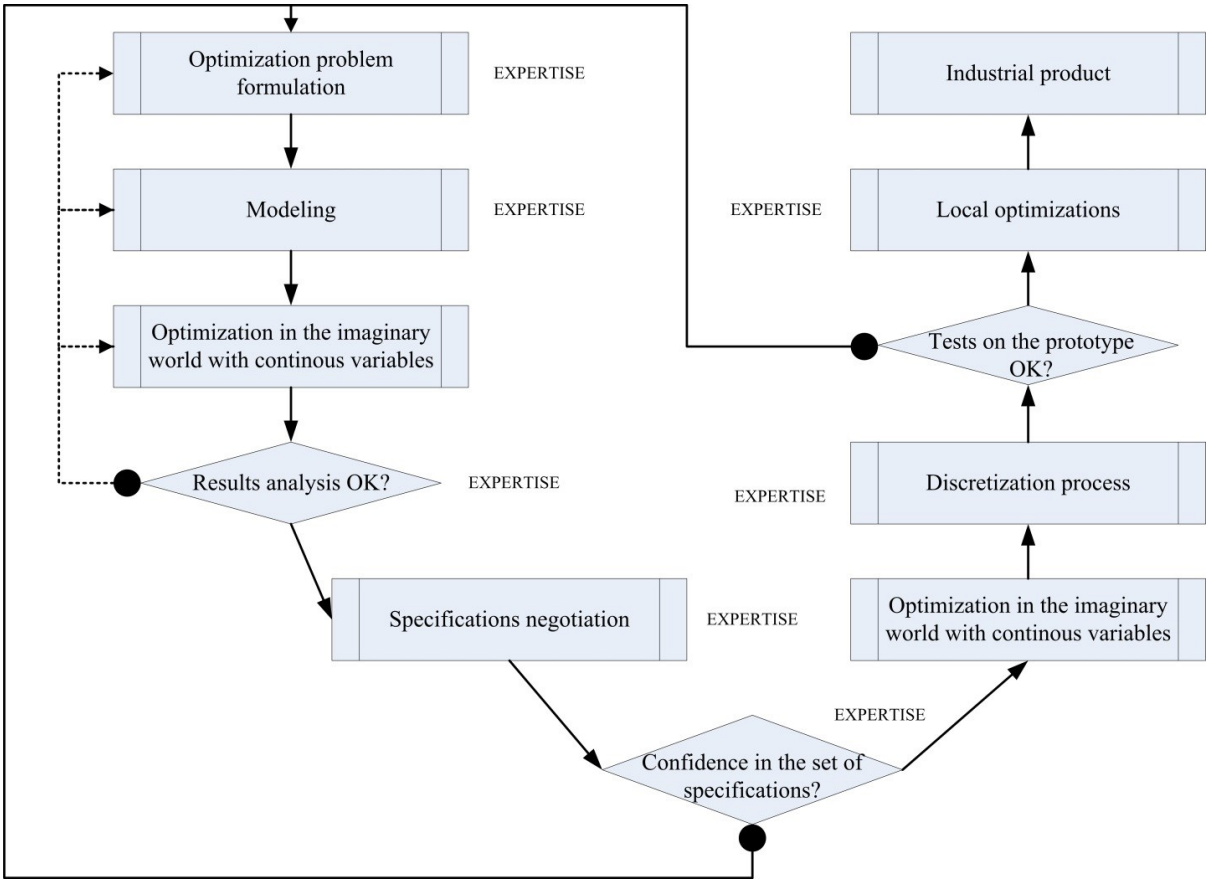


Figure 5: Organigramme de l'approche de pré-dimensionnement dans le monde imaginaire

Chapitre 3: Un défi de conception pour l'exemple

Le pré-design du convertisseur DC-DC situé entre les panneaux photovoltaïques et le bus de distribution d'énergie de l'aéronef Stratobus (Figure *6*) est un parfait exemple pour illustrer cette thèse.

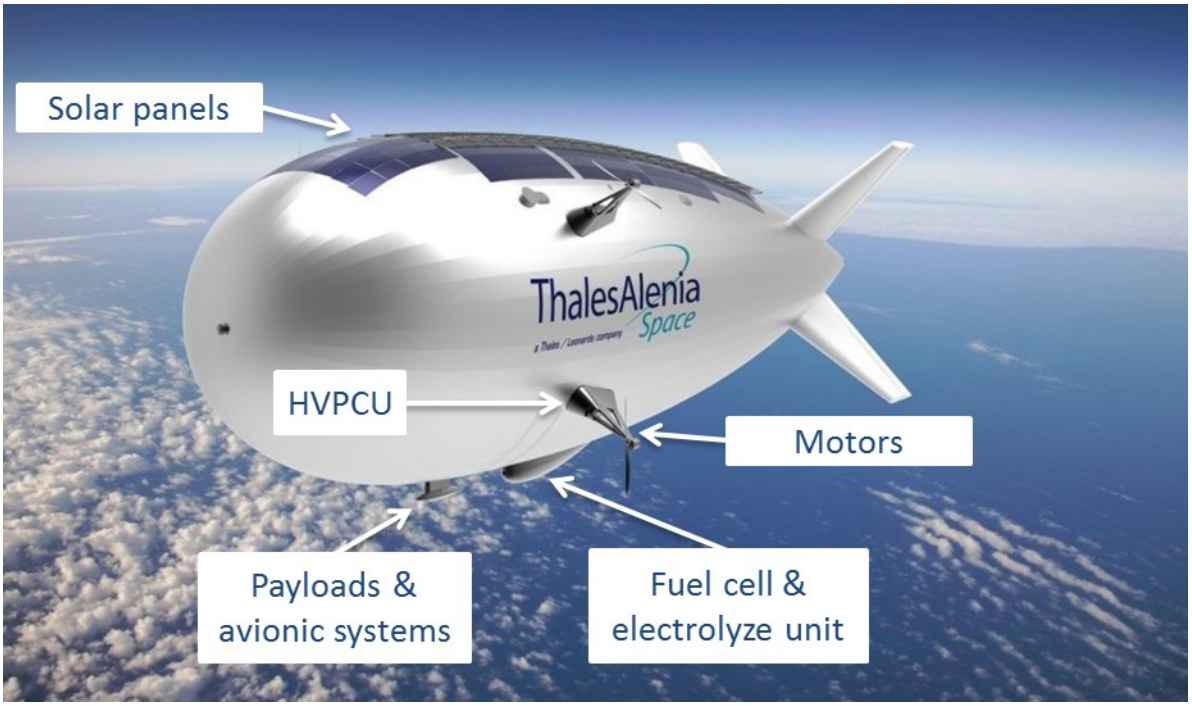


Figure *6*: Illustration 3D du Stratobus (projet mené par Thalès Alenia Space)

Dans ce projet où le nombre d'innovations technologiques est très important, la phase plateau sert à la définition du cahier des charges de chaque sous-système permettant le meilleur compromis d'un point de vue système. C'est lors de cette phase plateau que l'approche proposée dans cette thèse a une vraie valeur ajouté pour la formulation de la problématique de design du convertisseur DC-DC. En effet, les caractéristiques du convertisseur ne sont pas figées mais l'intégrateur système a besoin de données quantitatives pour déterminer la faisabilité du système complet.

Néanmoins, les ordres de grandeurs de la plage de fonctionnement du convertisseur sont connus : large plage de tension d'entrée ([450 - 800] V) et de sortie ([200 - 430] V) avec une puissance variant de 0 à 5 kW[1]. Il est aussi certain que le critère le plus important du convertisseur est sa masse à minimiser.

Les arguments qualitatifs ont permis de définir une architecture et une topologie de ce convertisseur : le Buck entrelacé à inductances non couplées (Figure *7*). Cependant, de nombreux paramètres restent à déterminer : le mode de conduction, le nombre de bras et les composants.

[1] Toutes ces données sont purement fictives (mais du même ordre de grandeur) pour des raisons de confidentialité

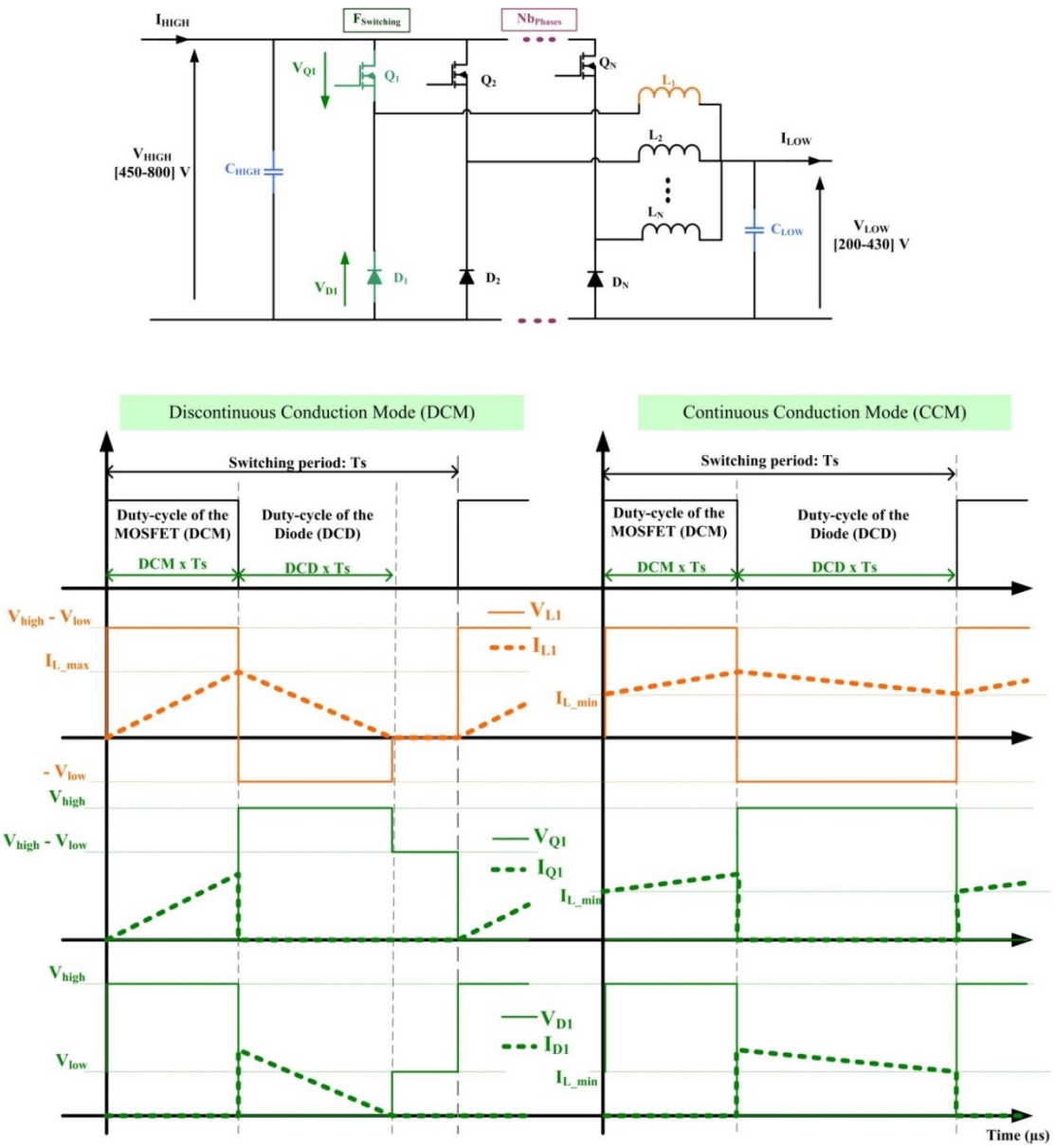


Figure 7: Schéma du Buck entrelacé et ses formes d'ondes idéales associées

Les technologies de chaque composant du hacheur série entrelacé ont aussi été présélectionnées. La cellule de commutation sera en Carbure de Silicium. L'inductance de bras sera constituée d'un noyau magnétique à poudre de fer et de fil de Litz entourés d'une résine.

Partie B : Formulation du problème d'optimisation pour le pré-dimensionnement dans le monde imaginaire

Chapitre 4 : Formulation du problème d'optimisation des systèmes électroniques de puissance pour l'utilisation de l'algorithme d'optimisation par gradient

Alors qu'un dimensionnement manuel requière un modèle « indirecte », il est préférable d'appliquer les algorithmes d'optimisation sur des modèles dits « directes ». La différence entre ces deux types de modèles pour un même système est illustrée avec la Figure 8 sur le dimensionnement d'un condensateur de filtrage. Il est à noter que le degré de liberté sera plus important avec un modèle directe.

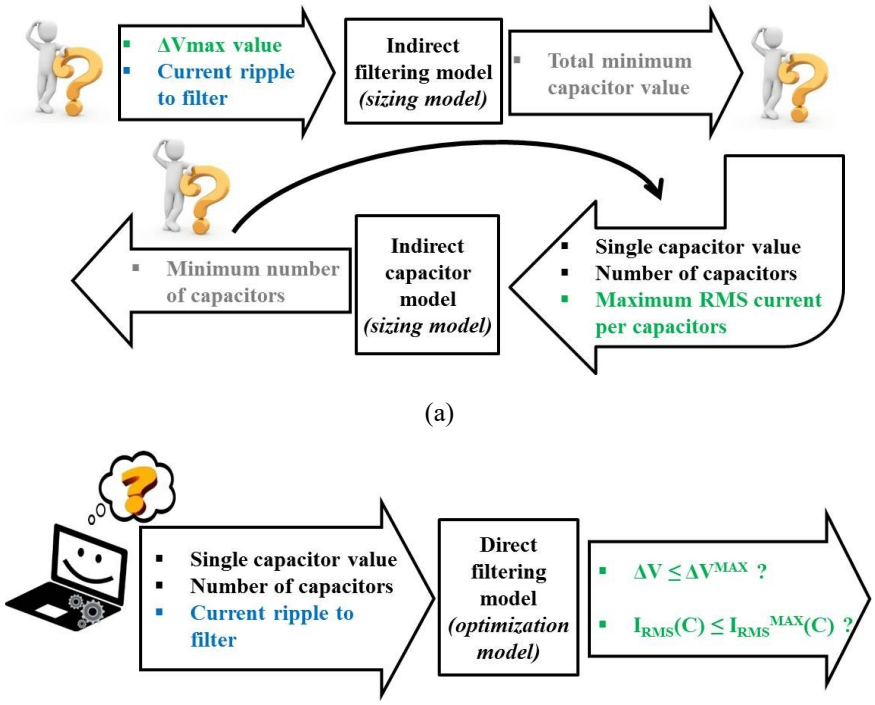


Figure 8: Illustration des modèles (a) de dimensionnement « indirects » et (b) d'optimisation « directs »

Un modèle doit être construit suivant le contexte dans lequel il est utilisé. Dans le cadre de cette thèse, les modèles d'optimisations se doivent d'être directs, continus, dérivables et avoir un coût de calcul faible. Les modèles analytiques sont alors préférentiels.

Afin de réaliser un modèle direc de convertisseur statique, il est conseillé de construire ce modèle suivant la Figure 9. C'est-à-dire partir de la description physique du convertisseur : les performances du convertisseur dépendent de ses formes d'ondes qui dépendent elles-mêmes des propriétés des composants sélectionnés.

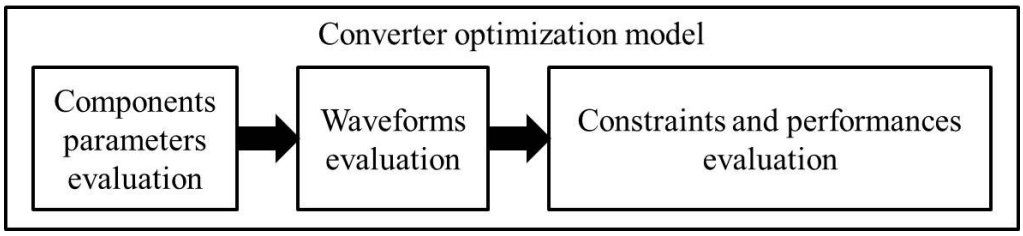


Figure 9: Modèle d'optimisation directe d'un convertisseur statique

En électronique de puissance, les performances du système influent sur les propriétés de ses composants qui influent sur les performances du dit système... C'est par exemple le cas avec la température de jonction du transistor qui dépend des pertes qui sont liées à sa température. Afin de gérer cette boucle, appelée implicite car non résoluble directement, des contraintes d'optimisation sont ajoutées et résolues par l'algorithme d'optimisation comme indiqué par la Figure 10.

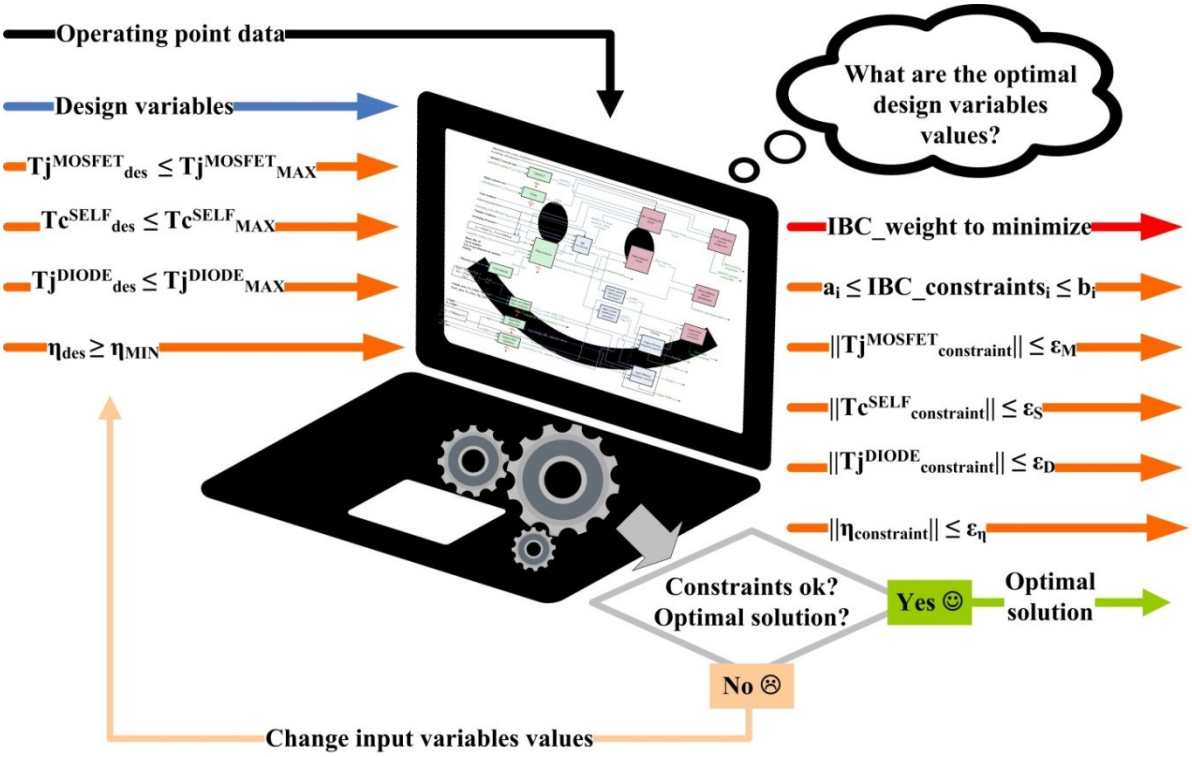


Figure 10: Illustration de la résolution des boucles implicites par l'algorithme d'optimisation

Les chapitres suivants présentent la modélisation du convertisseur Buck entrelacé pour l'application Stratobus.

Chapitre 5 : Modèles d'évaluations des paramètres des composants et des formes d'ondes du convertisseur Buck entrelacé

Comme dit précédemment, les modèles d'optimisation se doivent d'être continus et dérivables.

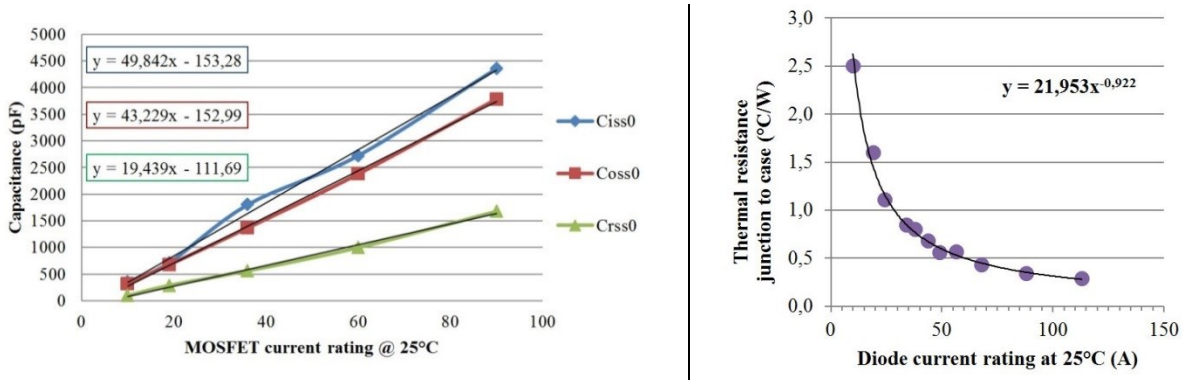
Parmi les composants électroniques dont nous désirons déterminer les paramètres, nous identifions trois types de discontinuités :

- Une simple discrétisation du paramètre continu, pour des raisons industrielles et économiques. Par exemple, les valeurs des condensateurs dépendent de la surface diélectrique et sont intrinsèquement continues, mais sont discrétisées en séries industrielles.

- Variables numériques intrinsèquement discrètes comme le nombre de tours d'une inductance ou le nombre de bras d'un convertisseur Buck entrelacé. Le monde imaginaire avec des valeurs non entières de phases nécessitera des développements spécifiques pour proposer des modèles continus et dérivables.

- Choix intrinsèquement discret d'une technologie, comme par exemple SiC vs Si, ou de matériaux magnétiques spécifiques.

Parmi les composants du convertisseur, les semi-conducteurs font partie des variables de dimensionnement discrétisées pour des raisons industrielles. En effet, pour une technologie et un processus de fabrication donnée, leurs propriétés sont liées à la hauteur et surface de la puce semi-conductrice. Dans le cas étudié le choix du calibre en tension ne se pose pas. Les paramètres du MOSFET et de la diode comme leur résistance à l'état passant ou leurs capacités de jonction ont donc été interpolés en fonction de leur calibre en courant d'après les données du fabricant (Figure 11).



(a) *(b)*

Figure 11: Exemple de paramètres du MOSFET et de la diode en fonction de leur calibre en courant à 25°C, (a) capacités du MOSFET, (b) résistance thermique de la diode

La même méthodologie de modélisation fut appliquée pour les composants de filtrage.

Quant à l'inductance de bras qui est constituée d'un noyau magnétique en poudre de fer, de fil de Litz et de

résine, une description géométrique et matérielle avec des équations analytiques permet de déterminer sa valeur. La densité de courant dans le fil de Litz étant limitée à une valeur faible pour des raisons techniques, le modèle de résistance parasite du fil de Litz n'a pas besoin d'être d'une grande précision et résulte d'une simple équation analytique fournie par le fabricant.

L'évaluation dans le domaine temporel des oscillations et du taux de distorsion harmonique en courant en entrée et sortie du convertisseur n'est pas aisée pour les convertisseurs entrelacés avec des modèles analytiques continus et dérivables (Figure 12). Cependant, transposer ce problème dans le domaine fréquentiel est tâche facile (Figure 13).

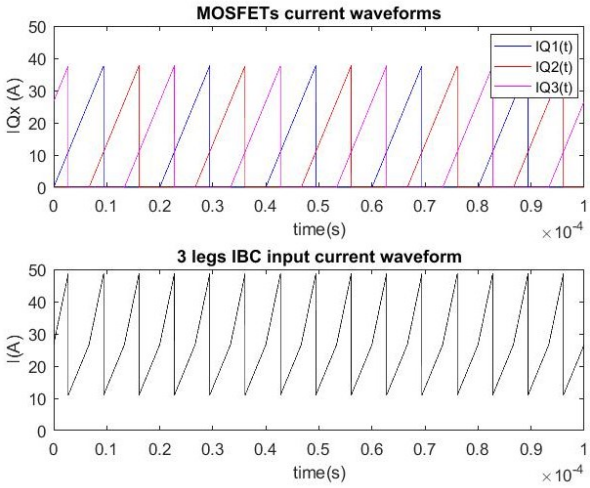


Figure 12: Formes d'ondes temporelles du courant dans les MOSFET et en entrée d'un Buck entrelacé 3-bras en conduction discontinue

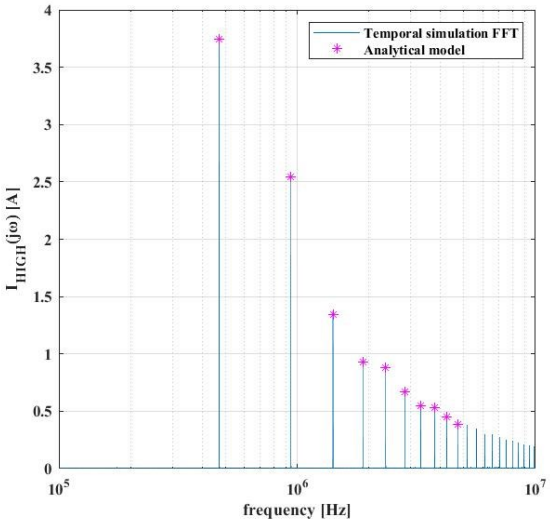


Figure 13: Spectre fréquentiel du courant en entrée du convertisseur Buck entrelacé 3-bras

Pour les formes d'ondes des composants dans un bras du hacheur entrelacé, les équations sont très connues si l'on reste dans le cas idéal. Cependant, lorsque les éléments parasites entre en jeu, notamment pour la conduction discontinue (Figure 14), il faut choisir le juste équilibre dans la précision du modèle.

Par ailleurs, le passage entre conduction continue et discontinue durant l'optimisation et la contrainte associée doit se faire de manière intelligente. Évaluer la différence entre la valeur de l'inductance de bras et la valeur critique pour être en limite de conduction continue et discontinue permet une formulation continue de la contrainte.

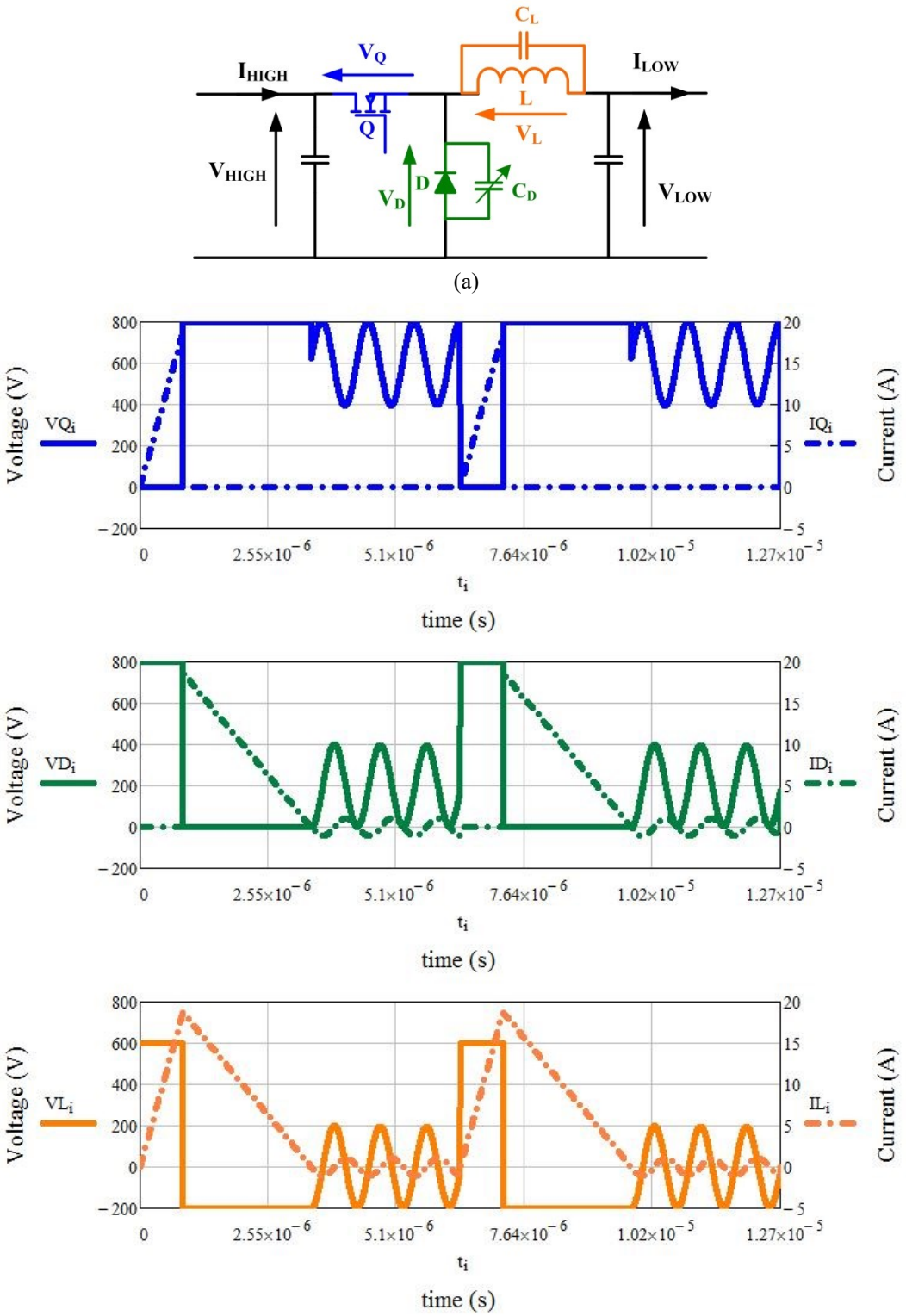


Figure 14: Formes d'ondes du convertisseur Buck en conduction discontinue avec la résonance due aux éléments parasites, (a) schéma de Buck avec les éléments parasites, (b) formes d'onde des composants de puissance

Chapitre 6 : Modèles de pertes et thermiques des composants de puissance du convertisseur Buck entrelacé

Modèles de pertes et thermiques de la cellule de commutation

Les pertes en conduction des semi-conducteurs sont évaluées à l'aide des classiques équations Eq. 1et Eq. 2.

$$Pcond^{MOSFET} = Rds_{on} * IQrms^2 \qquad \text{Eq. 1}$$

Avec Rds_{on} la résistance à l'état passant du MOSFET et IQrms le courant efficace de ce dernier (obtenu à l'aide des modèles de formes d'ondes).

$$Pcond^{diode} = Vt * IDmoy + Rt * IDrms^2 \qquad \text{Eq. 2}$$

Avec Vt la tension de seuil, IDmoy le courant moyen dans la diode, Rt sa résistance à l'état passant et IDrms son courant efficace

Le modèle de pertes en commutation de la cellule en Carbure de Silicium est basé sur le découpage en plusieurs phases de la commutation (Figure 15). Pour chaque phase, les équations du circuit sont résolues de manière analytique.

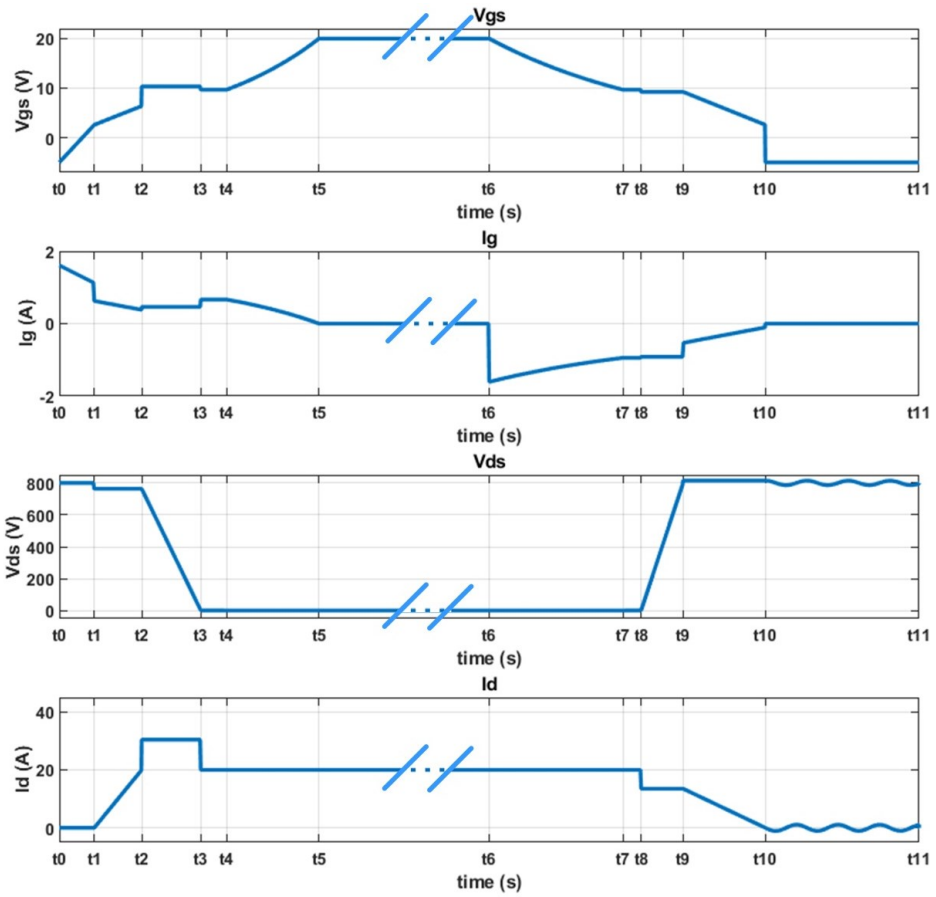


Figure 15: Formes d'ondes de la commutation utilisées pour évaluer les pertes

Pour obtenir des modèles continus et dérivables, il fut nécessaire de faire quelques hypothèses comme négliger l'influence de l'inductance de grille du MOSFET pour le calcul des pertes en commutation. Comme

expliqué dans le chapitre 2, la formulation du problème d'optimisation et la modélisation associée est un processus itératif. Or, les expérimentations conduites sur un prototype ont révélé un phénomène physique inattendu sur la diode SiC Schottky. En effet, celle-ci chauffait plus qu'elle ne l'aurait due démontrant l'existence de pertes non quantifiées mais reliées à la différence de tension entre la phase oscillatoire et la phase de conduction du MOSFET (Figure *16*).

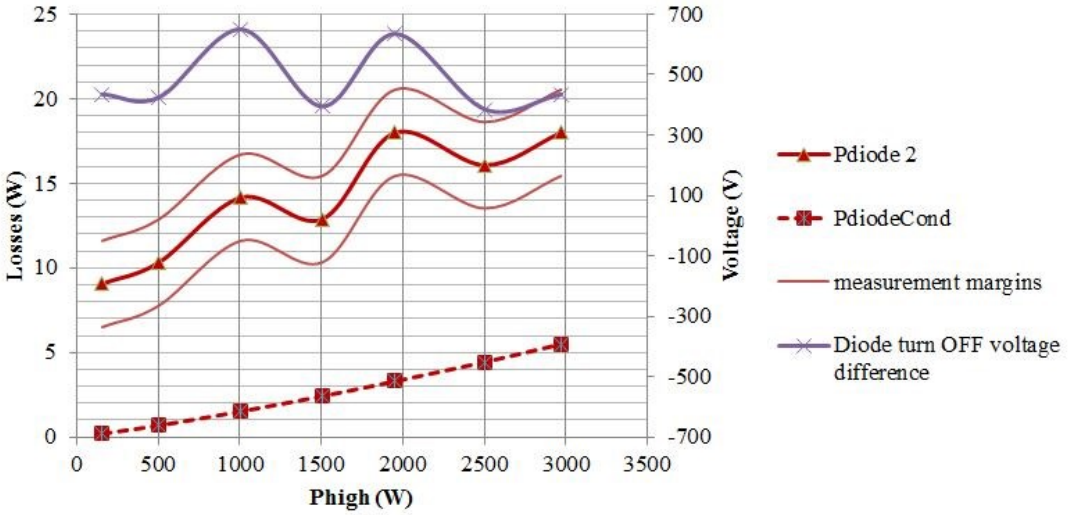


Figure *16*: Diode Schottky SiC dans un IBC à 3 bras (a) formes d'onde théoriques à Pin = 2,5 kW, Vin = 700 V et Vout = 200 V, (b) mesure des pertes (Pdiode2) avec ses marges d'erreur, ses pertes théoriques par conduction et la différence de tension de la diode entre la phase oscillatoire et la phase de conduction du MOSFET

Ces pertes supplémentaires proviennent très probablement du comportement hystérétique de la charge de la capacité de jonction de la diode (phénomène découvert en 2018 par l'équipe de recherche de Juan Rivas-Davila à l'université de Standford). Après avoir observé et partiellement compris ce phénomène, une équation analytique a été proposée puis simplifiée (pour le modèle d'optimisation) pour évaluer quantitativement ces pertes.

Le modèle thermique des composants semi-conducteurs est un modèle 1D classique.

<u>Modèles de pertes et thermique l'inductance de bras</u>

Les pertes dans le noyau magnétique de l'inductance de bras du Buck sont évaluées à l'aide du modèle IGSE (Improved Generalized Steinmetz Equation). Les pertes dans le bobinage sont la résultante de l'évaluation de la résistance continue et alternative du fil de Litz avec le courant moyen et efficace de l'inductance.

La littérature propose de nombreux modèles analytiques de pertes, mais est encore relativement peu fournie quant aux modèles thermiques analytiques d'inductances. Cela est d'autant plus regrettable pour le Buck entrelacé dont le composant le plus lourd est d'inductance de bras et que l'on cherche à définir le meilleur cahier

des charges minimisant la masse du système Stratobus.

Les conductivités thermiques des matériaux constituants l'inductance étaient notamment inconnues, particulièrement en ce qui concerne le fil de Litz. Celui-ci étant constitué d'isolant électrique, de cuivre et de résine entre chacun de ses brins (Figure 17), il est aussi anisotrope.

(a) *(b)* *(c)*

Figure 17: Inductance de puissance du Buck entrelacé (a) sans la résine, (b) moulée dans la résine, et (c) coupe transversale montrant la répartition de la résine

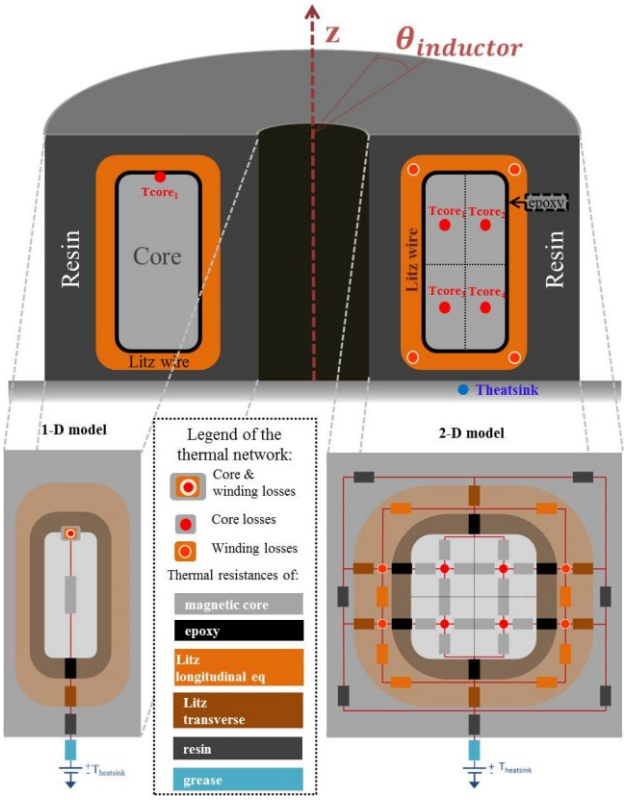


Figure 18: Modèles thermiques 1D ou 2D de l'inductance de bras du hacheur série entrelacé

Des mesures expérimentales (Figure 19) nous ont permis d'identifier les conductivités thermiques du noyau magnétique ainsi que celles du fil de Litz. Cette étude expérimentale a aussi démontré l'importance de modéliser le comportement thermique de l'inductance en 2 dimensions malgré une plus grande complexité du modèle d'optimisation que pour le modèle 1-D (Figure 18).

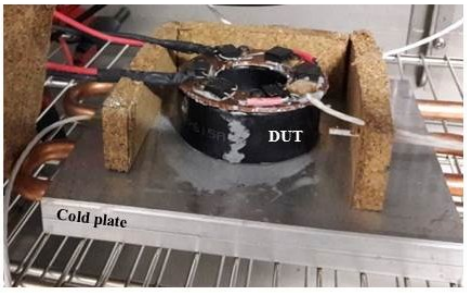


Figure 19: photos du banc de test

Chapitre 7 : Comparaisons des modèles de pertes des composants de puissance du convertisseur Buck entrelacé avec des données expérimentales

Démarche

L'objectif principal des expérimentations est de définir le domaine de validité des modèles d'optimisation du convertisseur Buck entrelacé dans le but global de définir les limites propres de l'optimisation et de vérifier qu'aucun phénomène physique n'a été oublié.

La validité des modèles sera remise en question en deux étapes :

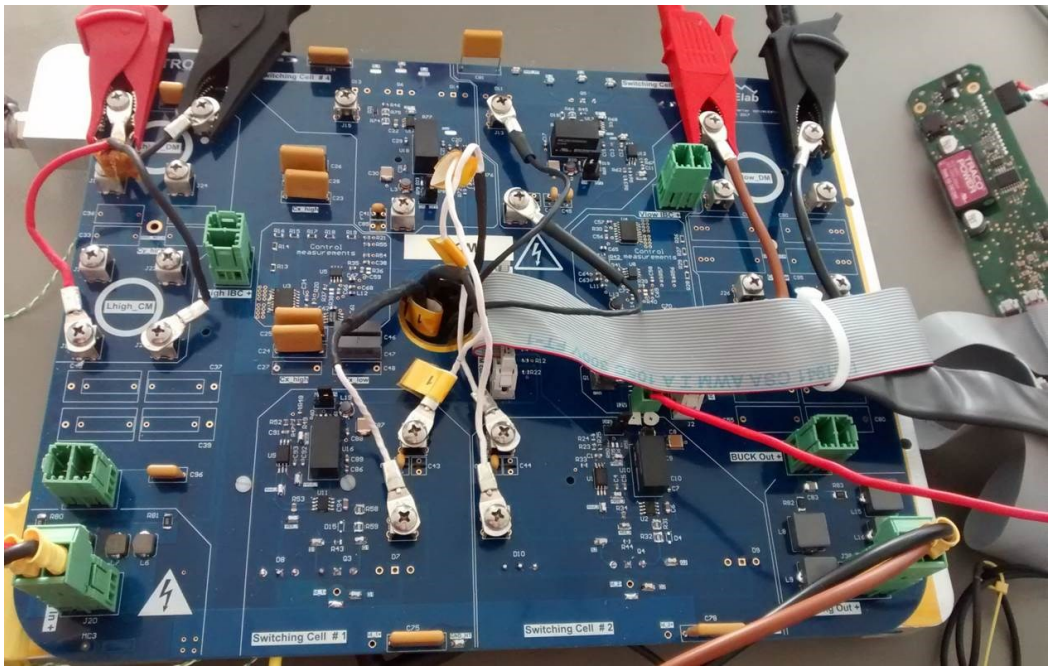
- d'abord en utilisant toutes les données disponibles (circuit de cellule de commutation, données de caractérisation de l'inductance et mesure de la tension du MOSFET à sa fermeture) afin de confirmer la compréhension de la physique du système (c'est-à-dire sans les simplifications et hypothèses nécessaires faites sur certains paramètres pour les modèles d'optimisation),

- deuxièmement, en comparant les mesures expérimentales au modèle d'optimisation avec les paramètres estimés du système.

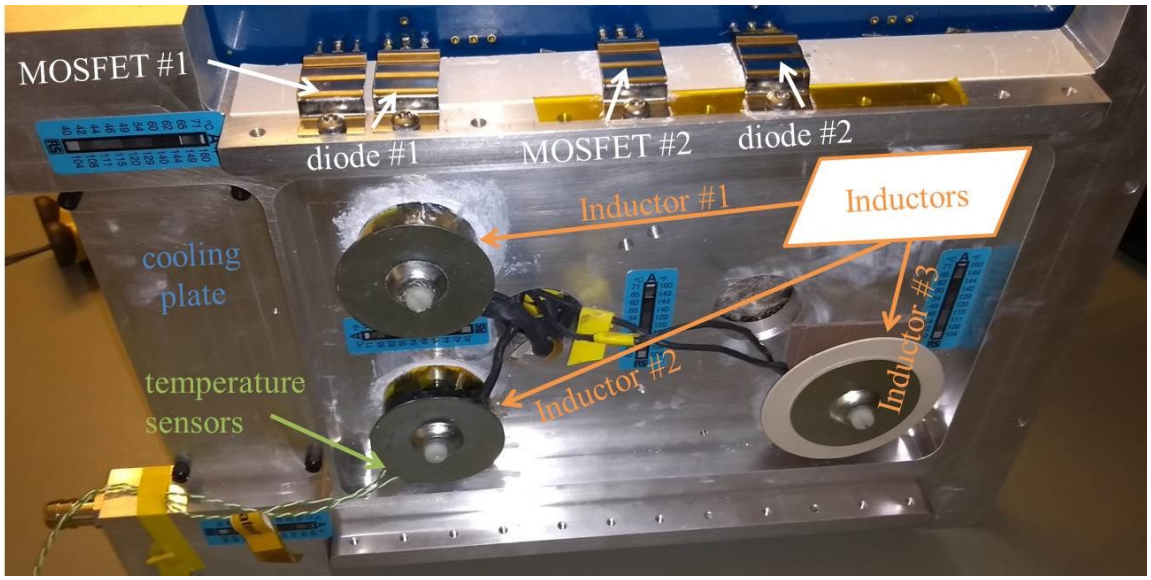
Un convertisseur Buck entrelacé à 3 bras (Table 1) fonctionnant en conduction discontinue a été réalisé (Figure *20*) à des fins de mesures expérimentales. Celui-ci est donc instrumenté et tout l'espace nécessaire fut occupé (il n'y a pas eu de recherche d'optimisation de l'intégration volumique).

Table 1: Caractéristiques principales du prototype

Puissance d'entrée	[0 – 3] kW	Fréquence de découpage	157 kHz
Tension d'entrée	[480 – 800] V	référence MOSFET	C2M0040120D
Tension de sortie	[200 – 400] V	référence Diode	C4D10120D
Refroidissement à eau	[35 – 65] °C	Résistance de grille	13.8 Ω
Mode de conduction	DCM	Inductance de phase	matériau: KoolMu 26 ; valeur: 28.5 µH
Nombre de bras	3	fil de Litz	143 brins de 100 µm



(a)

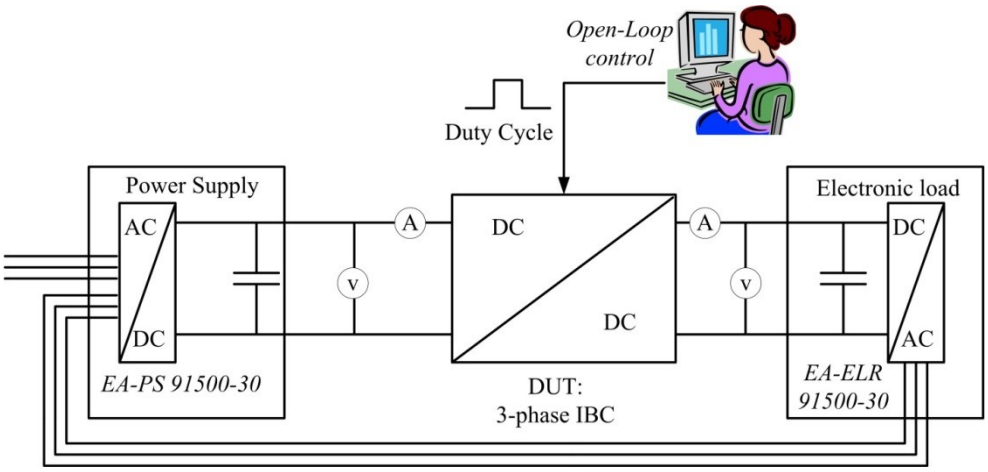


(b)

Figure *20*: Photos du prototype, (a) vue du dessus, (b) vue du dessous

Avant de réaliser les tests fonctionnels, les composants du convertisseur ont été caractérisés. Ainsi les paramètres électriques des 3 inductances de phases ont été mesurés à l'analyseur d'impédance ainsi que les inductances parasites du circuit imprimé. Il a été confirmé les que la fréquence des oscillations apparaissant en conduction discontinue ne sont pas prévisibles. De plus, les valeurs des éléments parasites du circuit imprimé sont du même ordre de grandeur que ceux estimés dans le chapitre 5.

Pour caractériser le convertisseur en fonctionnement, le banc de test expérimental illustré par la Figure *21* a été mis en œuvre.

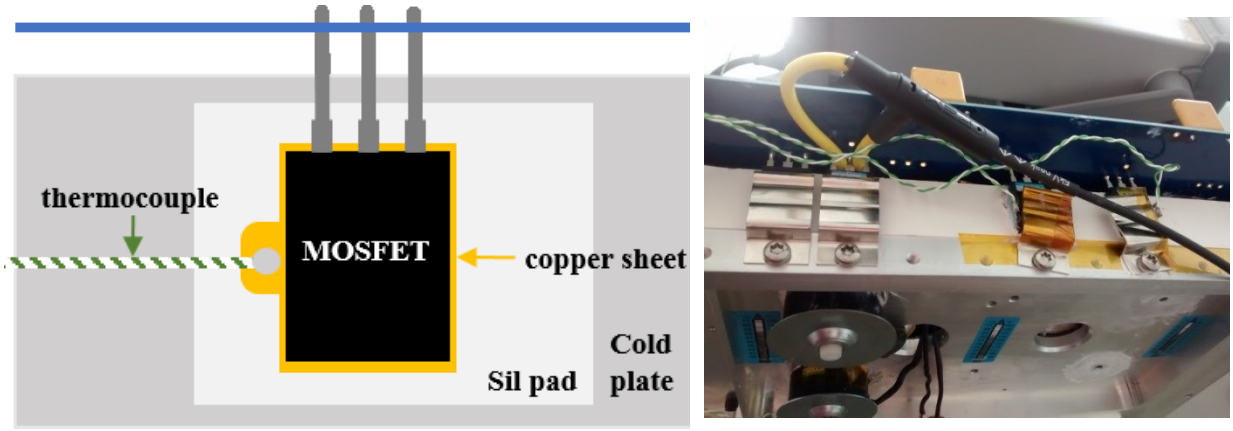


(a)

(b)

Figure *21*: Banc de test électrique: (a) schéma, (b) photo

Puisque l'objectif des expérimentations est de valider les modèles de pertes des composants de puissance sans en modifier le comportement, les pertes globales des semi-conducteurs ont été mesurées thermiquement (Figure *22*) et les pertes de l'inductance de bras électriquement.

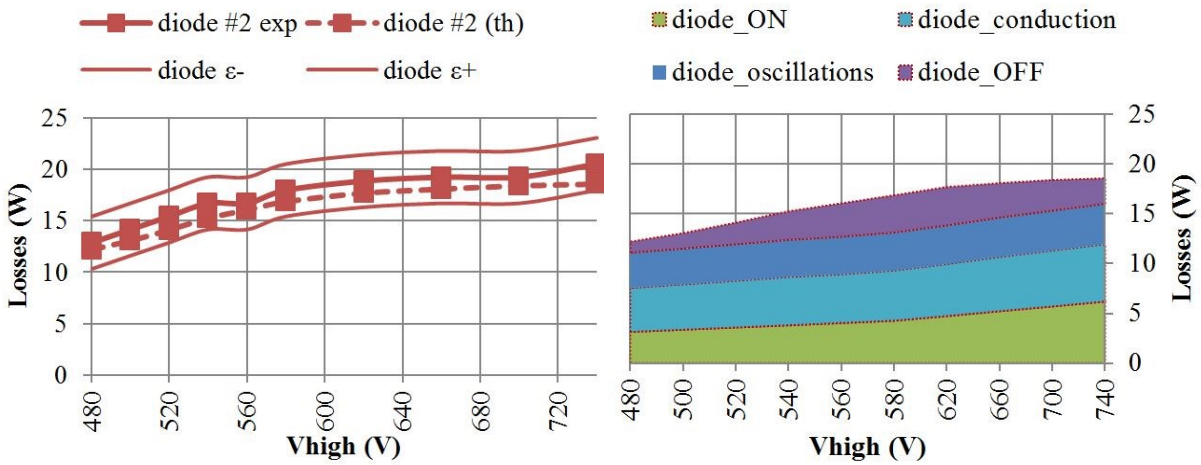


(a) (b)

Figure *22*: (a) Schéma, (b) photo de la mesure de la température du boîtier du MOSFET côté semelle

Validation des modèles analytiques

Figure 23 est un exemple de comparaison entre le modèle analytique et les mesures expérimentales où la tension d'entrée du convertisseur fut variée de 480 à 740 V pour une tension de sortie de 200 V et une puissance de 3kW.

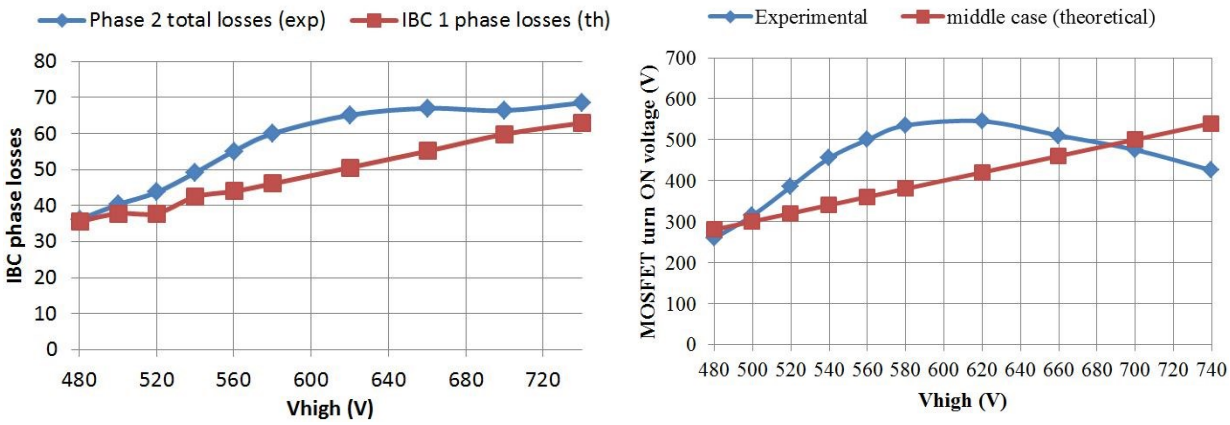


(a) (b)

Figure 23: pertes dans la diode du bras #2 : (a) comparaison entre les mesures expérimentales (les erreurs de mesure étant représentés par les petites lignes) et le modèle analytique, (b) pertes de la diode #2 dans chaque de phase de la commutation

Validation des modèles d'optimisations créés à partir d'hypothèses faites sur les modèles analytiques

Enfin, les modèles d'optimisation de pertes du convertisseur sont validés en comparant les résultats théoriques et expérimentaux sur les pertes du bras #2 (Figure *24*) et sur le rendement global du convertisseur (Figure *25*).



(a) (b)

Figure *24*: comparaison entre données théoriques (avec modèles d'optimisation) et données expérimentales : (a) pertes de phase (b) tension du MOSFET #2 lors de sa fermeture

L'erreur sur le calcul des pertes globales des convertisseurs est inférieure à celle des modèles d'optimisation dont les pertes sont mesurées sur la phase #2. Ceci est normal puisque les modèles d'optimisation sont basés sur le pari qu'en faisant la moyenne des N phases du convertisseur, l'erreur sur le rendement global sera faible et que le convertisseur ne sera donc pas surdimensionné.

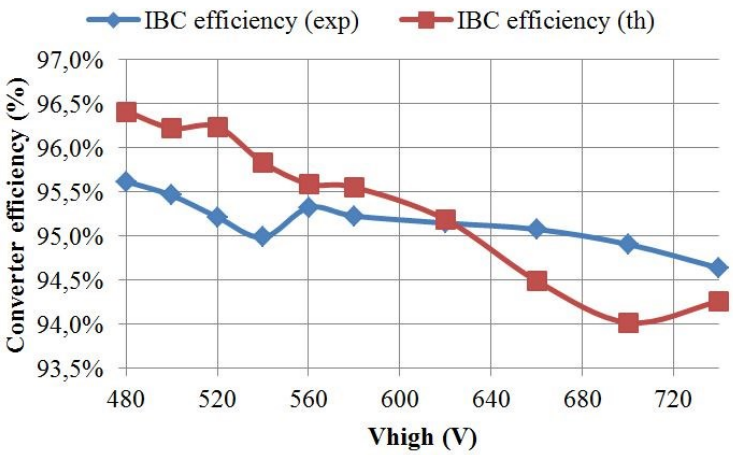


Figure *25*: Comparaison du rendement global théorique avec le rendement global mesuré en fonction de la tension d'entrée du convertisseur

Ainsi la formulation du problème d'optimisation et les modèles associés sont jugés suffisamment bons pour être utilisés dans des routines d'optimisation pour la négociation du cahier des charges.

Partie C :
Illustration de la force du pré-dimensionnement dans le monde imaginaire de systèmes d'électronique de puissance

Chapitre 8 : Pré-dimensionnement par optimisation du hacheur série entrelacé sur un cahier des charges initial

Le convertisseur de l'étude de cas (Stratobus) ayant de larges plages de fonctionnement, il est nécessaire de définir les points de fonctionnement dimensionnant. Pour cela, d'une part l'expertise du designer est nécessaire. Ensuite, il est démontré comment un algorithme basé sur le calcul du gradient peut aisément supporter des points de fonctionnements supplémentaires (i.e. voir la taille du problème d'optimisation augmenter) en cas de doutes du designer. L'analyse des résultats d'optimisation aide les concepteurs à finaliser le choix des points de fonctionnements à optimiser simultanément, autrement dit à formuler le problème correctement.

Table 2: Cahier des charge initial[2]

Criteria	**Minimum Value**	**Maximum Value**	**Conditions/Remarks**
Power density (objective)	7 kW/kg is mandatory	10 kW/ kg nice to have	Depends on the following specifications complexity
Input power	0 W	5 kW	For the entire of input/output voltage ranges (at this point of project starting)
Input voltage	450 V	800 V	For a power range [0 ; 5] kW
Output voltage	200 V	400 V	For a power range [0 ; 5] kW
Efficiency	96 %	NA	at 5 kW
Efficiency at a third of full load	90 %		at 1.7 kW
Input/Output current THD	NA	5 %	For a power range [1.7 ; 5] kW
Cooling temperature	-40 °C	65 °C	For a power range [0 ; 5] kW
Conduction mode	NA	NA	Must be the same for a power range [1.7 ; 5] kW

Ainsi, sur le cahier des charges initial (Table 2) [2] du convertisseur, les points de fonctionnement dimensionnant en conduction discontinue sont les #1, #3 et #4 lorsque le critère de l'optimisation est la masse des composants électronique du convertisseur.

[2] Fictif pour des raisons de confidentialités

Table 3: Points de fonctionnement dimensionnant

Operating point number	Input voltage (Vhigh) [V]	Output voltage (Vlow) [V]	Input power (Phigh) [W]	Cooling plate temperature (Tcooling) [°C]	Concerned conduction mode	Possible limiting constraints
# 1	800	200	5000	65	Both	IBC efficiency, power components temperature, current density in the phase inductor and output filtering components
# 2	800	200	5000	-40	Both	IBC efficiency due to diode on state resistance?
# 3	800	200	1700	65	Both	input and output current THD, efficiency
# 4	450	400	5000	65	DCM	conduction mode, maximum input DC current in filtering inductors
#5	450	200	1700	65	CCM	conduction mode, maximum input DC current in filtering inductors
# 6	800	400	5000	65	CCM	phase inductor temperature

Par la suite, il est démontré que la rapidité des optimisations dans le monde imaginaire (à peine quelques secondes pour un convertisseur optimisé sur 3 ou 4 points de fonctionnement simultanément) permet d'explorer différentes solutions technologiques de manière séquentielle. Cette exploration s'est fait dans le cas présent sur le matériau magnétique de l'inductance de bras du hacheur série entrelacé ainsi que sur le mode de conduction du convertisseur.

Par exemple, la Figure 26 démontre que sur ce cahier des charges, la perméabilité 60µ du matériau KoolMu 60 donne un résultat optimal en conduction continue.

Finalement, sur ce cahier des charges fictif, la meilleure densité de puissance massique fut obtenue avec un mode de conduction discontinue et du MPP 60µ comme matériau magnétique d'inductance de bras.

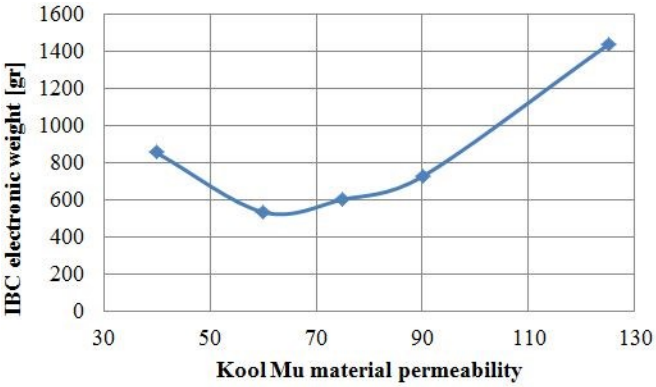


Figure 26: Poids du convertisseur en conduction continue pour différentes perméabilités du noyau Kool Mu (résultats d'optimisation)

Chapitre 9 : Négociation des exigences

La négociation du cahier des charges peut désormais se faire à partir de la solution optimale déterminée à partir du cahier des charges initial. Dans un premier temps, des optimisations paramétrées imaginaires permettent de négocier les plages de fonctionnement du convertisseur. Il est en effet évident qu'un convertisseur 5 kW sera plus lourd qu'un convertisseur de 3 kW. Mais quand est-il de la densité de puissance ? La Figure 27 obtenue en moins de 5 minutes permet au concepteur de répondre à cette question.

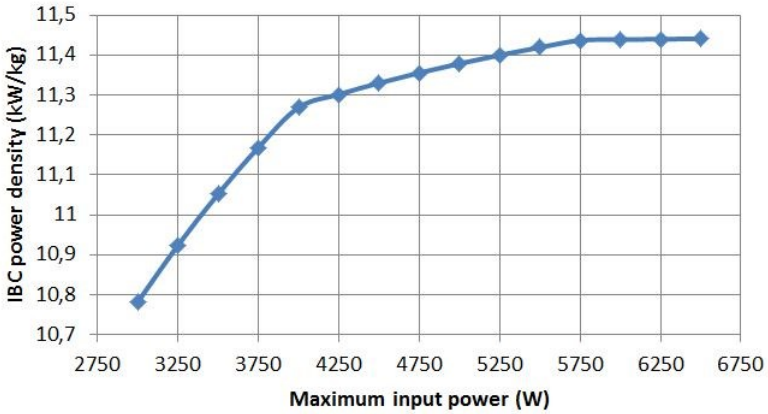


Figure 27: Evolution de la densité de puissance du convertisseur en fonction de sa puissance nominale

Cela est l'objectif premier des optimisations paramétrées : renseigner quantitativement les concepteurs sur un l'impact d'un changement de cahier des charges. De plus, l'utilisation d'un algorithme d'optimisation basé sur le calcul du gradient et utilisé dans le monde imaginaire permet d'analyser très facilement les résultats : ainsi le concepteur connaît quelle est la contrainte limitante déterminant la forme de la courbe paramétrée. Sur la Figure 27, les 3 morceaux de courbes différentes sont liées aux contraintes sur le filtrage du convertisseur qui impactent la fréquence de découpage et la masse de l'inductance de bras (Figure 28).

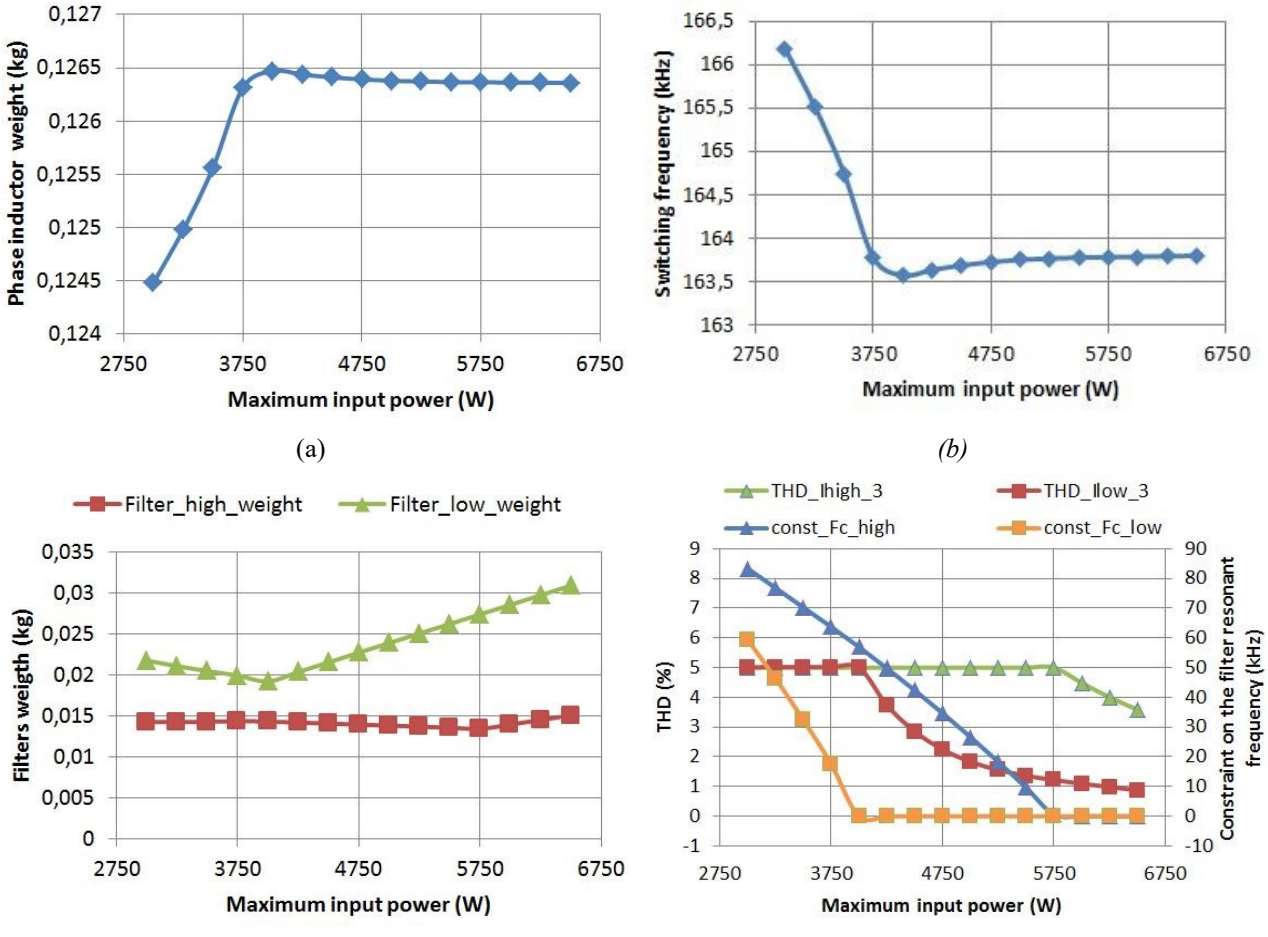


Figure 28: (a) Masse de l'inductance de bras, (b) fréquence de découpage, (c) masse des filtres et (d) contraintes sur les filtres via le THD du point de fonctionnement #3 (doit être < 5 %) et la fréquence de coupure du filtre (doit être > 0 kHz), en fonction de la puissance nominale du convertisseur

Enfin, pour les même raisons que précédemment, les Fronts de Pareto imaginaires (comme sur la Figure 29) permettent de comprendre le système et de trouver le meilleur compromis entre équipementiers de l'aéronef.

Une fois déterminé ce meilleur compromis et formalisé dans un nouveau cahier de charges, une dernière optimisation du convertisseur est réalisé dans le monde imaginaire.

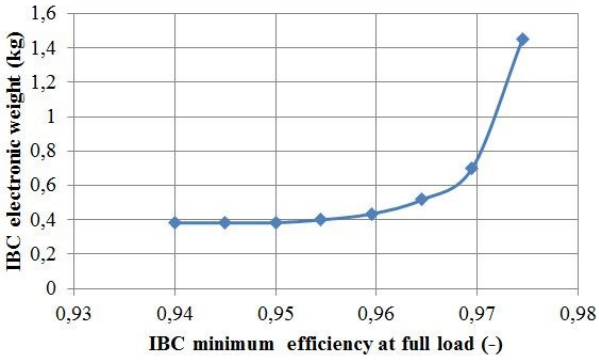


Figure 29: Front de Pareto entre le rendement et la masse du convertisseur

Chapitre 10 : Procédure de discrétisation pour revenir dans le monde réel

A partir de la solution imaginaire optimale sur le cahier des charges négocié, il est essentiel de revenir dans le monde réel en discrétisant la solution imaginaire pour deux raisons majeures :

- Déterminer de combien la solution sera dégradée lors du processus de discrétisation
- Rapidement prototyper cette dernière, valider qu'aucun phénomène n'a été oublié et définir les prochains axes de travail lors de la phase de design

La procédure de discrétisation proposée dans la thèse permet de profiter des efforts mis dans la formulation du problème d'optimisation. En effet, celle-ci se base sur de l'analyse de sensibilité locale rendue possible grâce aux modèles d'optimisation continus et dérivables, ainsi que sur l'expertise des concepteurs, d'où une procédure dite heuristique.

Cette procédure est décrite par la Figure 30.

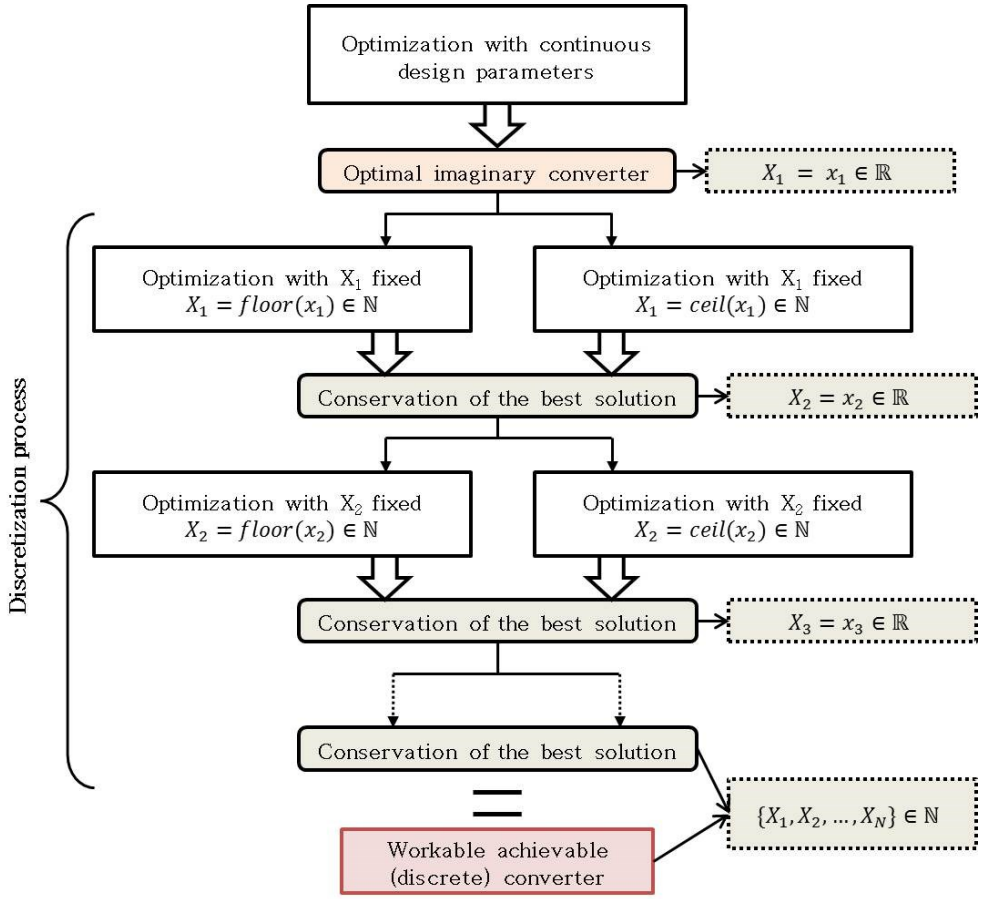


Figure 30: Processus de discrétisation heuristique avec X_n la $n^{ème}$ variable discrète, et la function objectif plus sensible à la variable X_1 que X_2, etc.

Cette procédure est une recherche de solution discrète locale et est par conséquent proche de la solution imaginaire. Cette particularité est visible sur les Figure 31 et Figure 32 puisque les ratios de masse et pertes

sont conservatifs durant le processus de discrétisation.

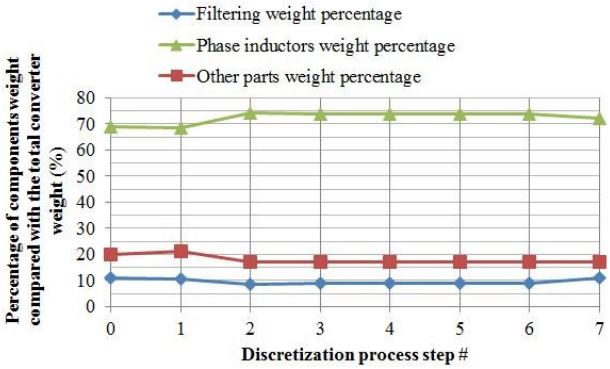


Figure 31: Evolution du ratio de la masse des composants durant le processus de discrétisation

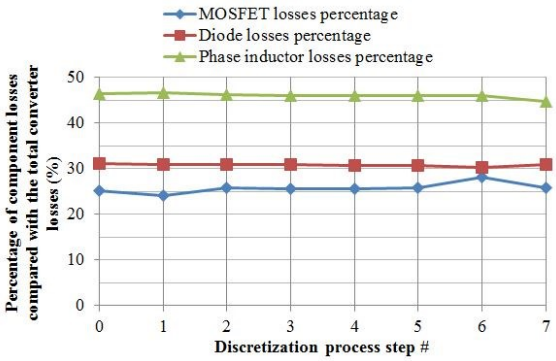


Figure 32: Evolution du ratio des pertes des composants durant le processus de discrétisation

Conclusion et perspectives

Le nombre de systèmes électroniques de puissance va continuer à augmenter dans les décennies à venir car l'électricité est l'énergie la plus appropriée pour relever le défi de la réduction des émissions de CO2. Au cours des dernières décennies, plusieurs méthodes et outils de conception ont été développés pour aider les concepteurs d'électronique de puissance pendant la phase de conception d'un produit. Cependant, il n'existait jusqu'à présent aucun outil ou méthode pour une phase de conception préliminaire d'un système électronique de puissance. Pour rappel, une phase de conception préliminaire doit déboucher sur des exigences fixes (et réalisables) du système à concevoir et sur un plan de développement consolidé du produit. Les exigences doivent donc être négociées entre les différents partenaires avec des données quantitatives. Il est également préférable de disposer d'un large champ de recherche pour proposer des solutions innovantes.

Cette thèse s'appuie sur cette observation et propose une nouvelle approche de conception préliminaire pour les systèmes électroniques de puissance capable d'explorer rapidement un large éventail de solutions tout en offrant une facilitation d'analyse. Ces particularités de l'approche proposée sont garanties par l'utilisation d'un algorithme d'optimisation de 1er ordre (basé sur le calcul du gradient) appliqué au monde imaginaire (continu) des systèmes électroniques de puissance.

Cette nouvelle approche suit la philosophie de la célèbre phrase d'Albert Einstein : "Si je n'avais qu'une heure pour résoudre un problème, je prendrais 55 minutes à définir le problème et seulement 5 minutes à trouver la solution". Sur l'organigramme de l'approche (illustré par la *Figure 5*), les premières étapes consistent à formuler le problème d'optimisation et à créer le modèle associé. Ces étapes sont détaillées dans les chapitres 5 à 7 de cette thèse et ont pris une douzaine de mois de travail. A l'inverse, les optimisations appliquées sur un ensemble d'exigences fixées afin d'identifier les propriétés critiques et le matériau de noyau magnétique le plus approprié d'un hacheur série entrelacées n'ont nécessité qu'une journée de travail (chapitre 8). Le même temps a été nécessaire pour tracer les optimisations paramétrées imaginaires et les fronts de Pareto du chapitre 9. Une autre journée de travail a été nécessaire pour revenir dans le monde réel avec une solution discrétisée basée sur la solution optimale imaginaire (chapitre 10).

Perspectives de la thèse

Les perspectives de cette thèse sont nombreuses, tant dans le domaine de l'électronique de puissance que dans le domaine du pré-dimensionnement par optimisation de systèmes d'électronique de puissance.

Tout d'abord, les optimisations appliquées à un convertisseur entrelacé utilisant des semi-conducteurs grand-gap (SiC) démontrent que le prochain axe de travail pour l'amélioration de la densité de puissance des systèmes d'électronique de puissance est la recherche de matériaux magnétiques performants à des fréquences de découpage élevées. Cependant, le travail sur les semi-conducteurs, bien que très avancé n'est pas encore terminé : il serait intéressant de comprendre en détails le phénomène hystérétique de la capacité de jonction de la diode Schottky puisque gênante pour les topologies à résonnance sensées minimiser les pertes en commutations des semi-conducteurs.

Concernant le pré-dimensionnement par optimisation pour des systèmes d'électronique de puissance, il serait intéressant de posséder un outil de capitalisation ergonomique utilisé par une large communauté de designers pour diminuer le temps passé à créer des modèles d'optimisation continus et dérivables. Cet outil devra cependant intégrer le contexte de chaque modèle créé afin que les concepteurs puissent le reprendre et modifier en toute confiance.

Une étude sur l'impact du niveau de précision des modèles sur les résultats d'optimisation, optimisation paramétrée et Front de Pareto pourrait aussi définir si l'une des pistes pour la diminution du temps de formulation du problème réside dans cette voie. L'étude de la prise en compte ou non des tolérances des composants électronique pourrait y être adjointe.

Enfin, il est nécessaire de définir à l'avenir la meilleure articulation entre les différentes méthodologies de pré-design et de design lors de la conception d'un produit suivant les acteurs (systémiers ou équipementiers) concernés.

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Introduction

The number of power electronics systems will proportionally increase with the number of embedded electrical systems such as electrical vehicles. To face the challenge of reducing CO_2 emissions, energy losses must be tracked and minimized (electrical conversion, mechanical friction). Devices will therefore be more and more constrained in the future, especially in power electronics with a 100% desired efficiency in a low volume and weight. If technology improvements such as wide band gap semiconductors contributes to that purpose, finding the optimal assembly and operating configuration between the different devices in a design is still necessary. Indeed, the wide band gap semiconductors allow the use of high switching frequencies. However, the size reduction of the power supply will be limited by passive components due to the lack of efficient materials for this range of frequencies. The ability to account for these parameters in design methods and tools will therefore significantly increase in the next few years.

In addition to that, power electronics systems are never end-user products but interface with various electrical systems; their design must take the specific constraints of each of them into account. In a design process, the objective of the preliminary design phase is to define the product requirements and the development plan while building confidence in the project feasibility.

This thesis offers a new preliminary design approach that addresses the challenge of helping power electronics designers to explore the continuously growing area of solutions (topologies, technologies, etc.) and negotiating specifications with quantitative data.

Gradient-based optimization algorithms are able to manage hundreds of design parameters and constraints and are therefore proposed. Nevertheless, this kind of algorithm requires a continuous and differentiable optimization problem formulation: all design variables must be continuous. For example, the design variable such as the number of turns for an inductor is no longer expressed as an integer but a continuous number. It means that the optimization problem with discrete parameters needs to be re-formulated in a continuous world we qualified as an "imaginary world". The major benefit of this approach is its ability to explore a large number of solutions.

The first part of this thesis "*Issues and a proposed solution to address the challenge of the preliminary design phase of power electronics systems*" further details the design process for power electronics (*Chapter 1*), the proposed approach (*Chapter 2*) and introduces a case study used to illustrate the approach (*Chapter 3*).

The second part focuses on the "*Optimization problem formulation for predesign in the imaginary world"*

with a generic method (detailed in *Chapter 4*) applied to the case study in *Chapter 5* and *Chapter 6*. The validity of the problem formulation is verified in *Chapter 7* through experiments.

Finally, the last part of the thesis "*Illustration of the strength of predesigning power electronics in the imaginary world*" shows how the proposed approach successfully helped a designer face the challenge of the preliminary design phase (*Chapter 8* and *Chapter 9)*. To finish, *Chapter 10* demonstrates that formulating the optimization problem in the "imaginary world" does not prevent the definition of a discrete solution.

Part A

Issues and a Proposed Solution to Address the Challenge of the Preliminary Design Phase of Power Electronics Systems

Chapter 1: Present Design Processes in Power Electronics

Chapter 2: A New Approach for Power Electronics Preliminary Design

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Chapter 1: Present Design Processes in Power Electronics

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I. WHY DESIGN STATIC CONVERTERS?

Among the challenges scientists face nowadays, climate change is probably one of the most important and tricky to deal with. The leading human influence on climate is from fossil fuel combustion that accounts for 80% of anthropogenic emissions. To cope with this challenge, research has been carried out on renewable energies, which provide electricity without giving rise to CO_2 emissions. Electrical energy is therefore the preferable choice for CO_2 reduction in addition to meeting the energy needs induced by the widespread and growing use of electronic devices.

To interconnect electrical sources to these electronic devices converters are needed. For that purpose, converters mostly use semiconductor technology since the invention of the first diode in 1902 by Peter Cooper Hewitt [1]. Thanks to this technology, converters are static and have an acceptable efficiency compared with the rotating machine converters, which explains their quick emergence in less than a century. Static converters are henceforth widespread in space and terrestrial use: all around the world, most individuals have a converter to charge their mobile phones, computers, television, etc., most factories use more or less powerful electrical machines that need to be supplied and controlled, and vehicles are becoming more electrical (Electrical Vehicles, More Electrical Aircrafts, drones, etc.)

But as stated in [2]: "Power electronics converters assume in many applications only a supporting partial function, which enables a main function to be realized, but does not itself represent the main function.", which leads to the conclusion that the static converter should be transparent in the system. In other words, the converter should have a 100% efficiency, no volume, no weight and no risk of failure, cost nothing and should not disturb the system by heat, Electromagnetic Interferences, etc. This is hardly achievable in practice, but engineers and researchers work to find the converter that simultaneously minimizes volume, weight, risk of failure, power losses, cost, thermal and EMI disturbance [2] or at least find the best compromise among these criteria (Figure *1*) depending on the main objectives and constraints associated with the application. The question is how can the designers reach this goal? One way is to follow a design process that allows efficient system optimization.

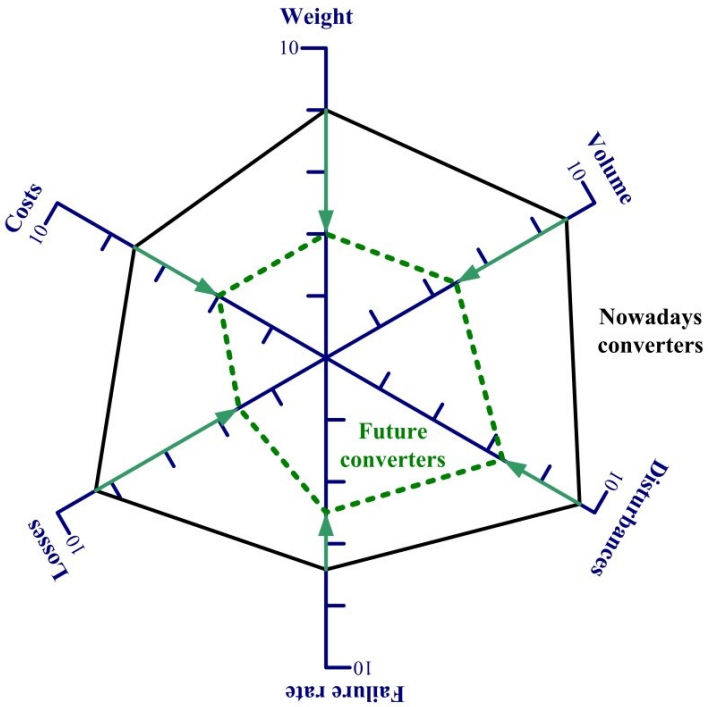

Figure *1*: Schematic of power electronics designer objective from [2]

II. General Design Process Description

The process of designing a new service or product typically includes the following phases (Figure *2*) before the design phase itself: identification of the customer's needs, establishment of the target specifications, product concept(s) generation, selection and preliminary design, test of the concept, establishment of final specifications, and finally development scheduling [3].

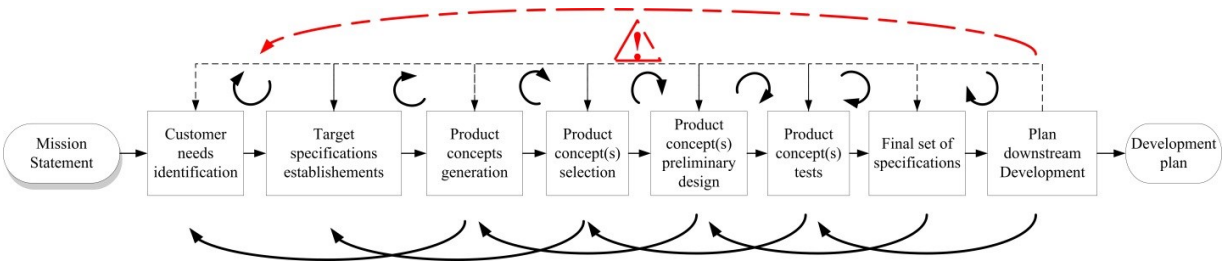

Figure *2*: Pre-design process according Ulrich and Eppinger [3]

The identification of customer needs does not only come from marketing but is the result of a collaborative effort between at least the designers and the customers. Let us take for example the design of a purse: the designers might know of new textiles that could be *in* next year. When the designers actively participate in the identification of the needs, the establishment of the first set of specifications is usually fast and the preliminary concepts of the products can even emerge during the “Customer needs identification” and “Target specification establishment” phases. The “Product concepts selection” phase depends on the project time, budget and resources (methods, tools, humans).

Alternatively, designers may select only one or two concepts that they believe in based on their experience or instinct, in other words, they limit the field of investigation. Although this approach saves time and money, there is still a risk of failure: a too premature decision can be fatal for the project (the purse becoming smaller when it is raining preventing the customer from retrieving their possessions). On the other hand, designers may have enough resources and time to explore the different concepts to limit the risk. This risk is usually drastically reduced thanks to the results analysis of the product concepts test. Thanks to this analysis, the final specifications can also be set as well as the corresponding development schedule.

These phases are never perfectly ordered; several iterations and backward steps are necessary to develop a useable product. The cost of product development is reduced if the number of iterations or the time spent in each phase is limited.

In a given design process, the substance of the different phases depends on the company core business. However the design process paradox, which consists in a depletion of the degrees of freedom in the design while the knowledge about the system grows, is always the same (Figure *3*) [4].

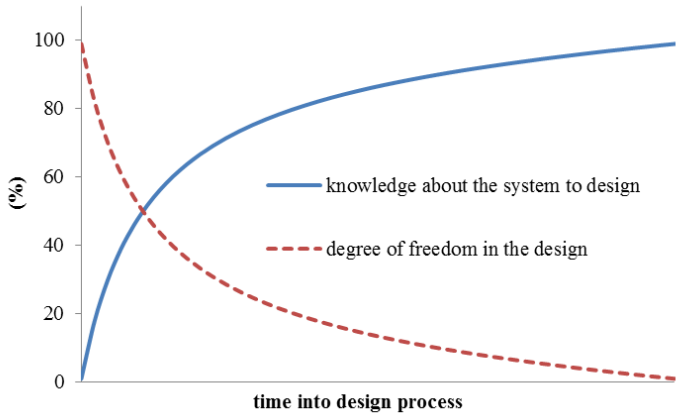

Figure *3*: Design process paradox

Aware of the possible consequences of such paradox, designers and managers have proposed many general methods, process and tools to overcome this problem over the last century [5] but what about power electronics design methods? The specifics of this field in the process of design are described in the following paragraphs.

III. Typical Power Electronics Design Process

A. Detail of the various design phases involved in power electronics development

One of the particularities of the power electronics field is that the converter is never a final product but is a part of a system. The converter designer has to work more or less in collaboration with the system integrator to adapt the converter design to the application.

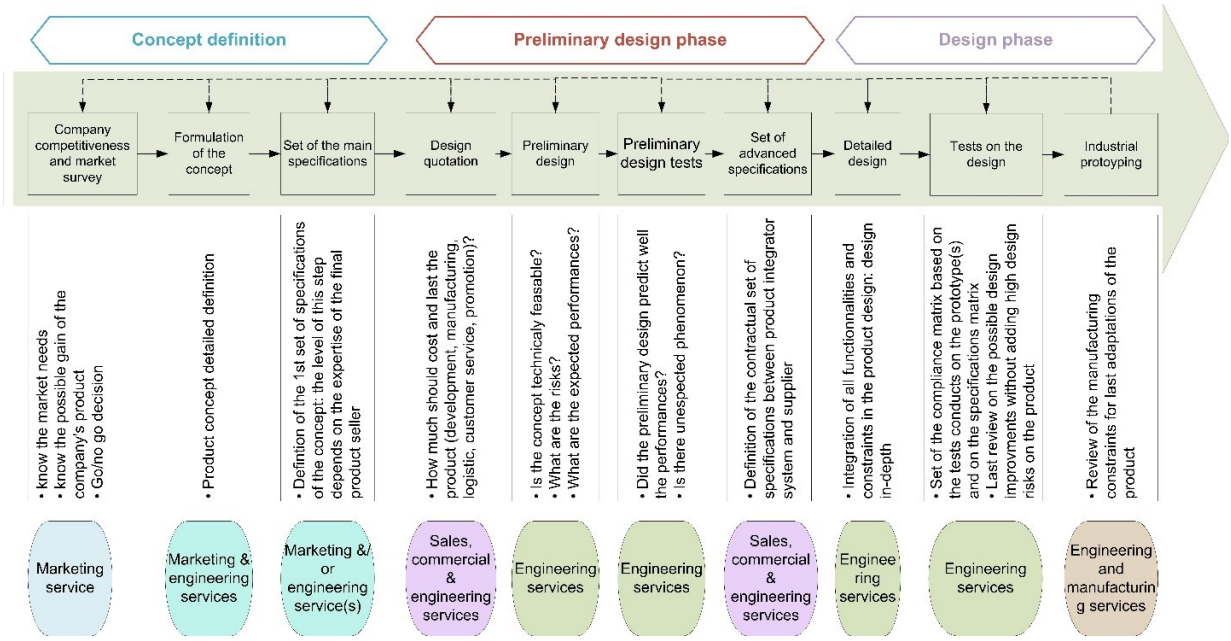

Figure *4*: Design process in power electronics

Figure 4 gives the detailed concept definition, pre-design and design phases of power static converters based on the general design process from [3]. The objectives and risks associated with each project actor are indicated below each step. These steps are the same whether the final product is a specific development for a customer or a proprietary development. As it is obvious on *Figure 4* the concept definition and preliminary design phases are those with a higher number of actors/services which explains why these phases are more likely to require several iterations.

Figure 5 indicates in more detail the design timeline with the evolution of the engineers' work depending on the evolution of system knowledge during preliminary design and design phases.

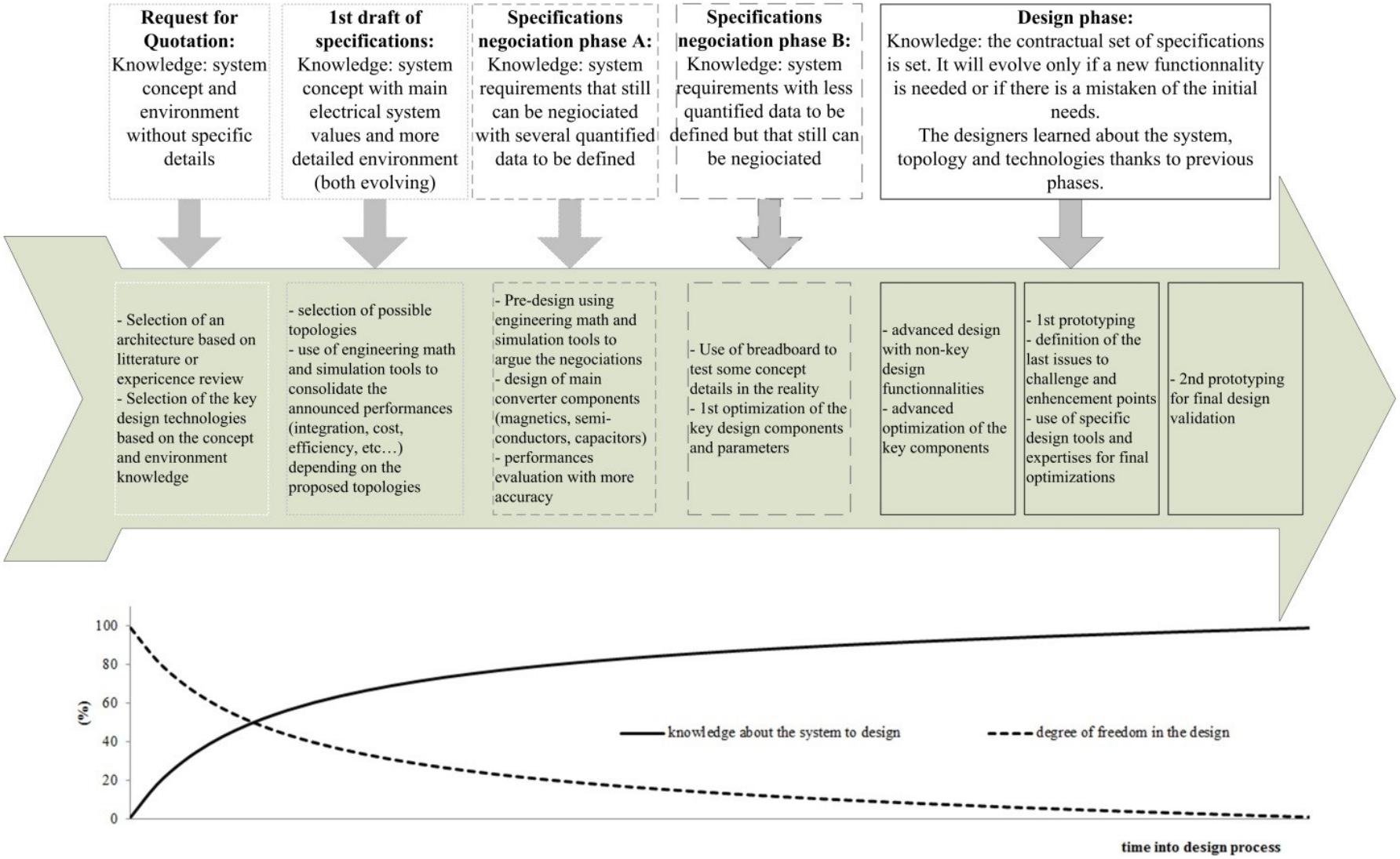

Figure 5: Pre-design and design phases conduct in power electronics

It is important to note that during the design phase the contractual set of specifications is defined: this step is one that carries a major financial risk along with the market survey phase.

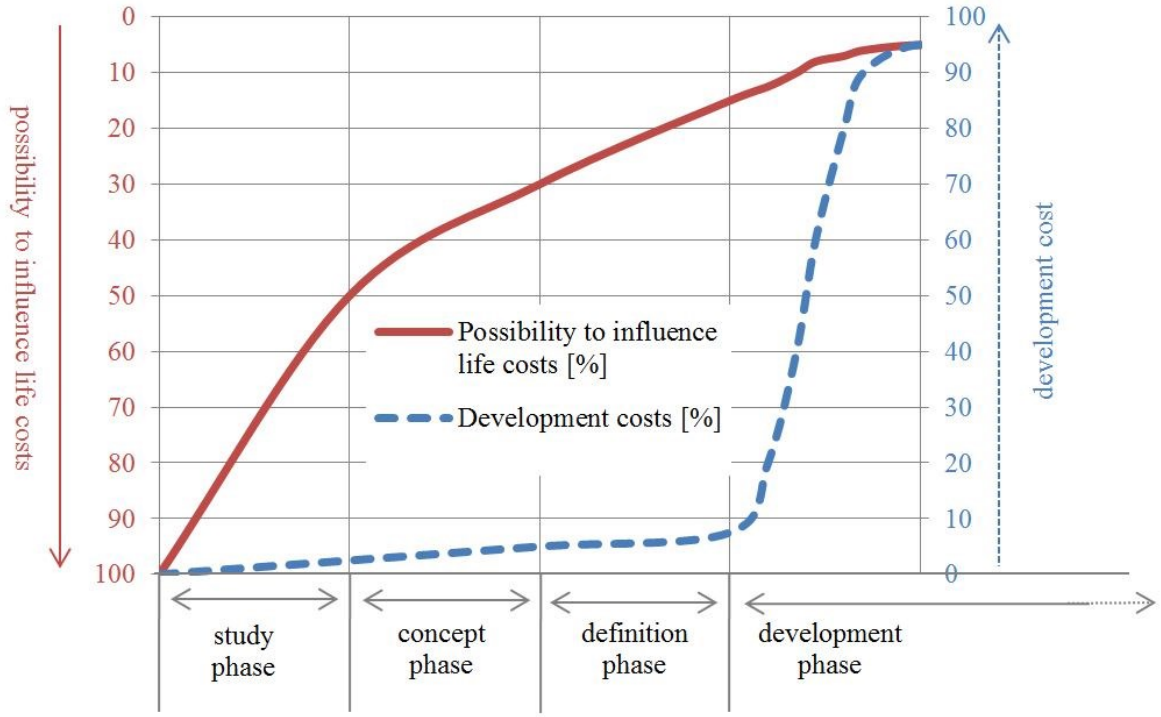

Figure *6*: Leverage of development expenditures from [6]

Figure *6* presents the evolution of the possibility to influence life cost and the development cost during the different phases for the conception of an aircraft [6]**.** This figure can actually be extended to all design processes and it is a parallel to Figure 5. **The preliminary design phase including the tests should therefore not be neglected.**

According to [5], designs that lead to a costly product are sometimes due to short-comings made by designers:

a. they do not collect enough or the right information before they start designing,

b. they focus on just one or a few ideas,

c. they fail to consider a range of options,

d. they follow a simple linear path or other unsuccessful processes when conducting the design.

In other words, to limit the failure rate, the process should offer the possibility to explore a range of concepts and generate enough material for discussions with customers and partners. But as [7] correctly predicted for decades, the current methods and computer assisted tools in power electronics are mainly circuit drawing and simulation, engineering math tools and finite element analysis. These kinds of methods and tools are actually perfect for the detailed design but not well adapted for the preliminary design phases.

There are no specific methods and tools that have yet been proposed in power electronics for the preliminary design phase with the aim of helping the designer to rapidly try several sets of specifications and different concepts or configurations. As already noted, the preliminary design phases often take place during the Requests for Quotation (RFQ) step, i.e. when the designer is not granted much time by the customer, so it should be shorter than the design phase itself. But hopefully, when this step is properly carried out, the design phase will be shortened.

B. An example of specific difficulties in power electronics preliminary design

Each engineering field has its specific design difficulty. In power electronics, the designers try to limit the number of topologies or possible architectures for the design as early as possible because for one converter topology, the number of design parameters is important. For example, let us consider the basic Buck converter (Figure 7).

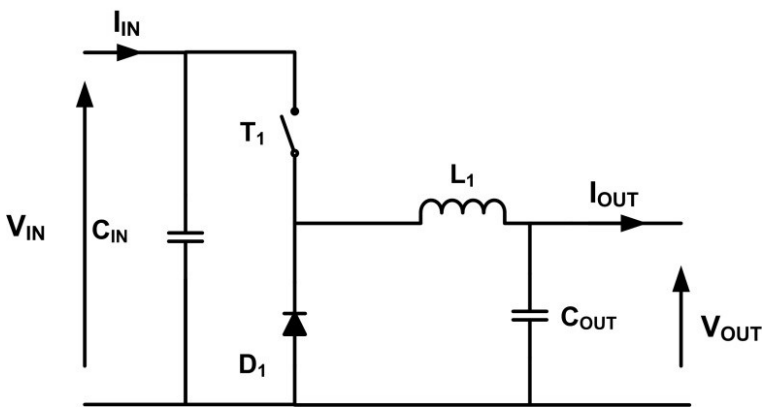

Figure *7*: Buck topology

With this topology, used here for DC-DC conversion, the design parameters are the following: input and output capacitors, output inductor, diode, transistor and conduction mode. Besides their electrical value chosen for the electrical behavior of the converter, they have to be chosen among several thousands of references in distributors' catalogs according to their ratings, mechanical design, losses, thermal constraints and failure rates. Finally, there are billions of possibilities for one topology and as every power electronics designer knows, for one conversion function, there are sometimes dozens of possible topologies. Knowing which combination of all of these design parameters will fulfill the specifications and cost constraints is challenging.

C. Methods and tools used in power electronics design

In cases where the static converter environment is perfectly known and controlled (i.e. the operating conditions and the standards are fixed) the designer has several ways to complete its design and often uses a

combination of methods. He can use his personal experience [8], the design rules proposed in the literature or capitalized in his company [9], try different designs by sweeping the main design variables [10]–[14] or use a combination of these methodologies [15]–[20].

The converter also has to be designed according to its preliminary requirements: its performance (in terms of weight, cost efficiency, etc.) will be linked with all of these requirements. With a global design process, it will be possible to determine a fair and quantified prediction on all of the requirements.

That is why the use of optimization algorithms has emerged for the design of converters [21]–[31], but due to the discrete nature of the power electronics (made of discrete components), the design problematic is generally formulated with discrete design variables. This leads to the common employment of database and stochastic algorithms like for example the Genetic Algorithm (GA) [23]: the number of design variables and constraints have to be limited to ensure convergence [32], [33]. This sort of optimization method should be applied in the more advanced design phase, i.e. when the number of unknown design parameters is small, for example optimizing only the magnetic component in the converter [26].

Finally, the multi-level optimization methods are for now the most suitable to define the optimal requirements of the different suppliers of a system [34], [35]. It nevertheless does not help the suppliers in their system problem formulation.

As already stated, all of these methods are useful when the specifications are fixed. However, with Requests for Quotation (RFQ) or for discussions with the partners at the beginning of a project a method that accounts for dozens of design parameters and hundreds of constraints is highly desirable.

IV. CONCLUSION

The demand for power converters will keep growing over the next few years. This raises the following question: are current design methods able to handle the resulting activity expansion without a proportional increase in the number of power electronics designers?

Around 90% of major decisions are taken during the pre-design phase (design paradox), so this activity will be the focus of the remainder of this thesis. A new approach to the pre-design of a static converter will be proposed and illustrated with a concrete example of a converter pre-design for an aeronautical project. The main objectives of this novel approach will be to decrease the risk of project failure and to provide a tool for effective negotiation by offering to the designer a wide range of possibilities that can be explored during this short design phase.

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Chapter 2: A New Approach for Power Electronics Preliminary Design

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I. REASONS FOR USING OPTIMIZATION DURING A PRELIMINARY DESIGN

The previous chapter introduced the design process paradox and stated that the number of degrees of freedom is higher in the early stages of design (and thus the impact of design choices is greater whereas the amount of available information is lower). It may be noticed that having a high number of degrees of freedom leads the designer to consider many potential architectures, to define the proper topologies and then technologies for each before evaluating their performance in the aim of eliminating those which are not suitable. This process is shown in Figure *1* below.

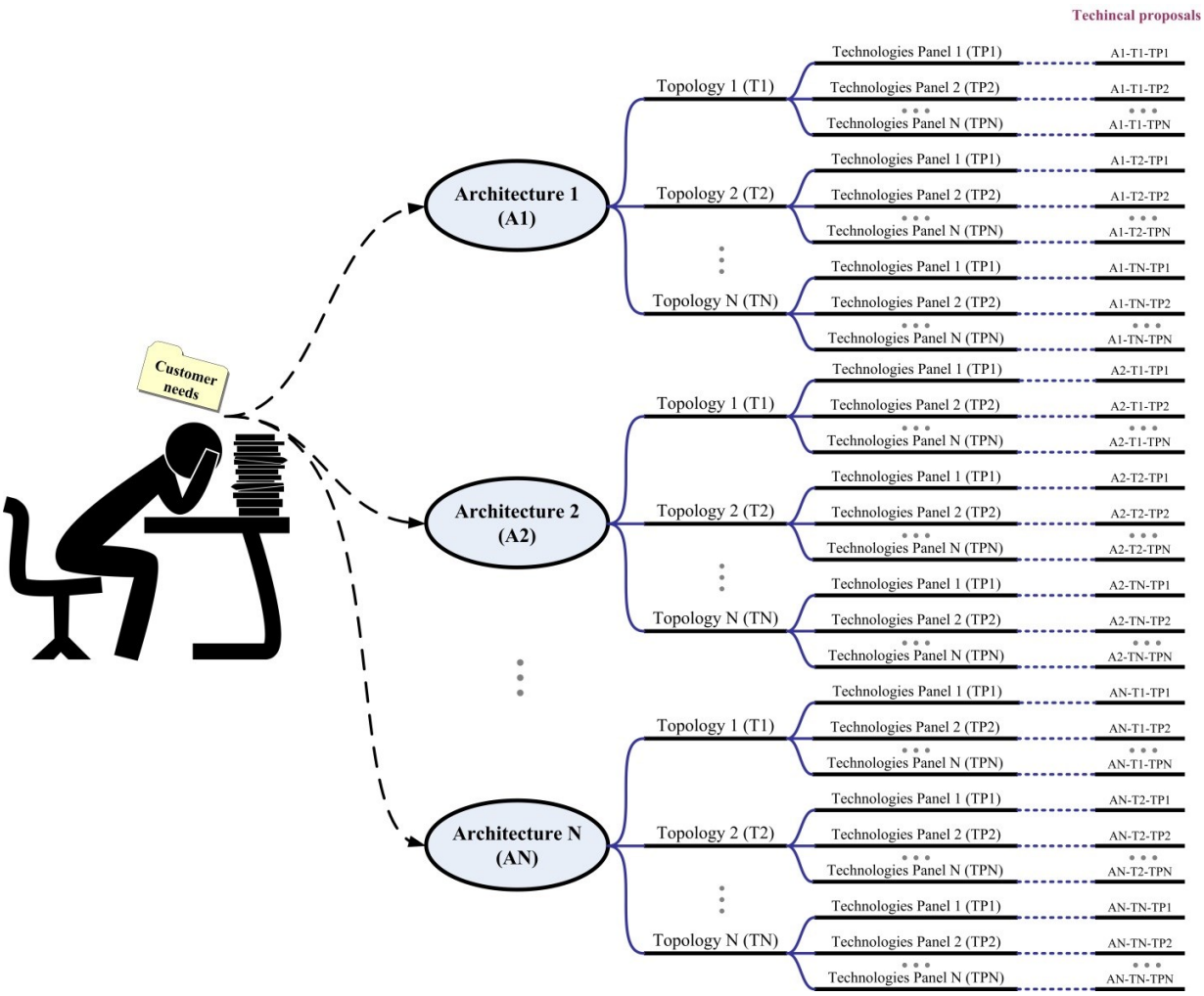


Figure *1*: Architecture proposals tree

The designer generally does not have years to prepare the architecture proposal for the customer. He or she usually tries to eliminate as many branches as possible in the architecture proposals tree by considering quantified or qualitative criteria.

A qualitative criterion to cap the panel of possible topologies for a conversion function might be to reuse an existing design in the company since key design parameters would then be known and design tools would already be in place thanks to accumulated expertise. In this case, the design phase can be more cost-efficient than

starting from literature only. Other external criteria such as desired collaboration with local research laboratories or suppliers, company strategies, etc. can also be considered as qualitative. These criteria facilitate quick removal of some of the branches from the proposal tree (Figure *2*).

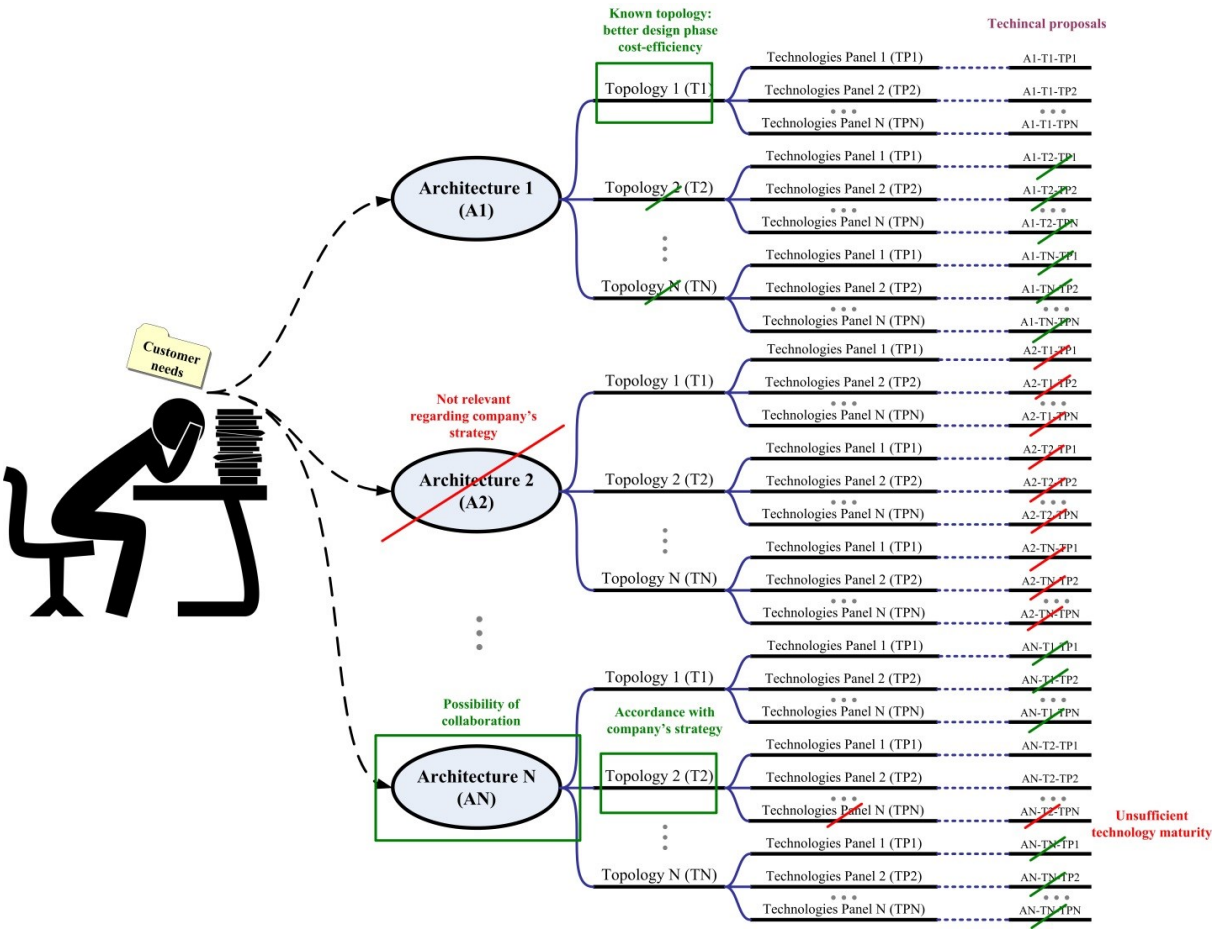


Figure *2*: Removing branches from the architecture proposal tree with qualitative criteria

In cases where qualitative criteria are not sufficient to remove all concepts except one, engineers have to validate their choice with objective quantitative criteria (typically in a short time frame). For example in Figure *2*, proposals A1-T1-TP1, A1-T1-TP2 … A1-T1-TPN, AN-T2-TP1 and AN-T2-TP2 have to be compared based on quantified data. If the designer has methods and tools available that rapidly compute quantitative and objective performance information that subsequently allows the elimination of some of the proposals, he/she can have more confidence in his/her statements when talking with the customer or with partners. In addition, the risks of project overspending and missed deadlines can be considerably decreased. Furthermore, he/she will be under less stress and able to pay more attention to the final customer's needs.

Table 1 shows a set of requirements for a pre-design approach that addresses the needs described above. In the remainder of this thesis, we present a new methodology that meets these specifications.

Table 1: Pre-design approach requirements

Mandatory requirements	**Nice to have**
• Ability to quickly explore a wide range of solutions for each proposal • Each proposal should be optimized in the aim of comparing them objectively	• Ability to simultaneously or sequentially explore each branch in a short time • A comprehensive library of models and case studies • Insight into the robustness and potential of the proposed concept with respect to requirements – margins, limitations, etc.

II. INTRODUCTION TO OPTIMIZATION CONCEPTS AND VOCABULARY

The electronic part of a static converter is primarily constructed from appropriate off-the-shelf discrete electronic components, and has suitably design parameters (e.g. switching frequency). According to Table 1, the designer should be able to perform rapid optimization on each of the proposed architectures taking into account many degrees of freedom, i.e. with a large number of design parameters. A brief review of the optimization problem definition and of the different existing optimization methods is therefore necessary so that the best algorithm may be chosen for the new pre-design approach.

A. Optimization problem definition

An optimization problem can be either constrained or unconstrained. There are several examples of mathematical unconstrained optimization problems; however, the design of a product is always subjected to at least a few design constraints. The constrained optimization problem can be described as follows (Eq. *1*) with *Y* as the objective function(s), *X* as a vector of input variables and *g* as the constrained output variables.

$$\begin{cases} minimize\ Y(X) \\ with\ g_j(X) \leq 0,\ \ j = 1..n \\ with\ g_j(X) = 0,\quad j = n+1..m \\ with\ X_i^{min} \leq X_i \leq X_i^{max},\quad i = 1..l \end{cases} \qquad Eq.\ 1$$

B. An overview of the different optimization algorithms

The following process underlies all optimization algorithms (Figure *3*):

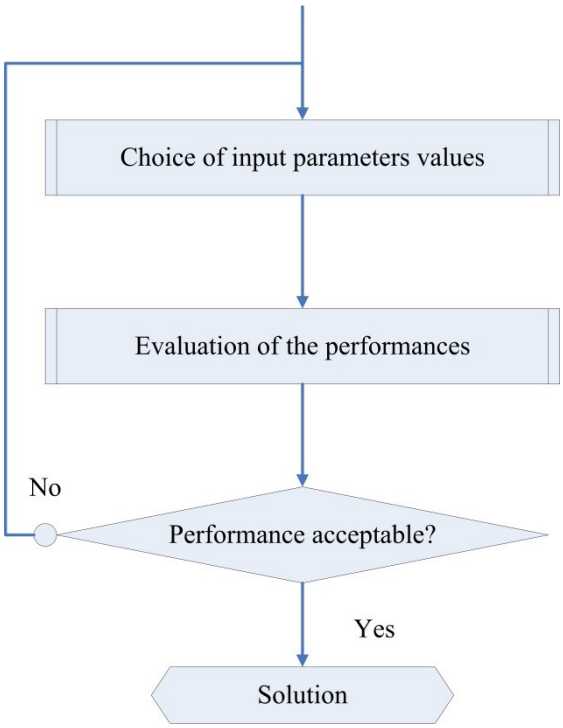


Figure *3*: General optimization algorithm process

Optimization algorithms can be classified under two big families: deterministic algorithms and stochastic algorithms. The heuristic family can be split into further categories. Figure *4* shows a non-exhaustive classification tree along with some optimization algorithm examples.

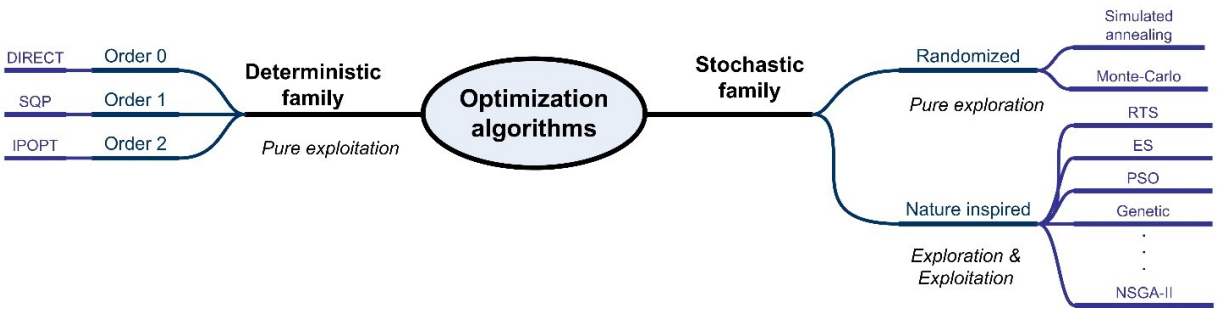


Figure *4*: Optimization algorithm non-exhaustive classification tree

In the stochastic family, some algorithms use a pure random search strategy. Others, such as the nature-based algorithms, also evaluate the model during optimization and use this information to update the input parameters values accordingly in an iterative manner. In the deterministic family, the order 0 algorithms are those that only need the optimization model evaluation data to progress whereas 1st order algorithms also need the gradient information (first derivatives) and 2nd order algorithms the second derivatives of the model. Table 2 gives the main properties, advantages and drawbacks of each sub-family. The maximum problem size partly depends on the optimization problem formulation: the value in the table is an order of magnitude of size corresponding to a basic formulation of the optimization problem. References for some of these algorithms are: DIRECT [1], SQP [2], IPopt [3], RTS [4], ES [5], PSO [6], Genetic [7] and NSGA-II [8].

Table 2: Algorithm main properties

Algorithm family	Algorithm sub-family	Number of objectives	Fast	Complex problems (many constraints)	Accuracy of the solution	Handling discrete parameters	Maximum problem size	Can be stuck in local optimum?
Deterministic	Order 0	1	✔	✖	✔	✖	30	Yes
	Order 1	1	✔	✔	✔	✖	1000	Yes
	Order 2	1	✔	✔	✔	✖	10000	Yes
Stochastic	Randomized	1	✖	✖	~	✔	30	No
	Nature inspired	[1 ; 5]	✖	~	~	✔	30	No

C. *Using a gradient-based optimization algorithm to design in the imaginary world*

1) *Proposed optimization algorithm for power electronics pre-design*

The new proposed approach in this work will be based on the gradient-based optimization algorithm SQP [2] which is capable of managing up to a hundred design parameters and thus corresponds more or less to the pre-design power converter problem size. It has the drawback of not being able to handle discrete parameters: all design variables have to be continuous. Unfortunately for power electronics designers who work with discrete components, any algorithm (heuristic or enumeration) or technique (branch & bound) that is able to use discrete variables is necessarily less efficient for large and highly constrained optimization problems [9], [10]. It has been proven in the past that "the problem of minimizing a linear form over polynomial constraints in at most 10 integer variables is not computable by a recursive function" [11], [12].

2) *Philosophy of the new approach: designing in the imaginary world*

The novel approach consists in designing a converter in an *"imaginary world", i.e.* with continuous variables. In the field of power electronics many items are discrete; this means that the design will be created from fictitious components and parameters. This approach for testing a concept can be decomposed into several steps illustrated in Figure *5* and detailed further on.

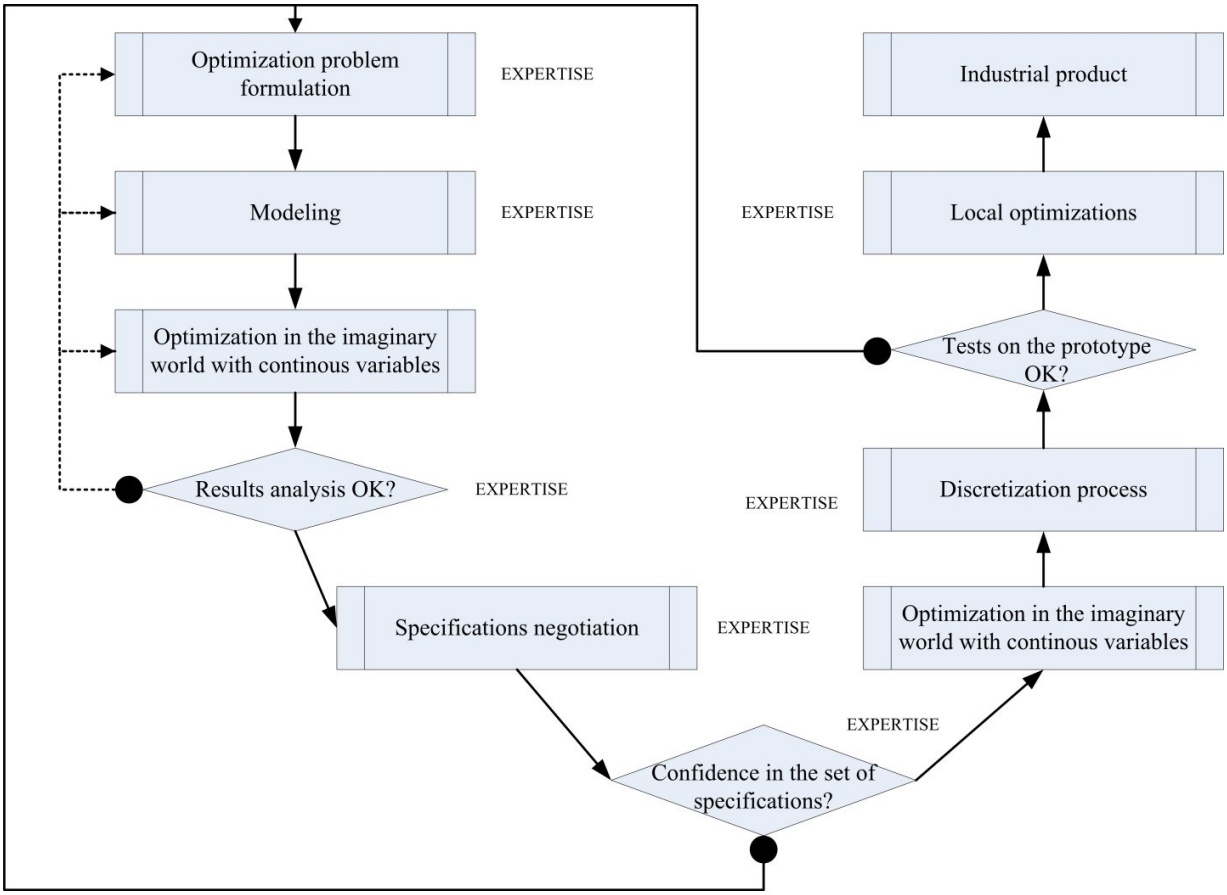


Figure 5: Pre-design in the imaginary world approach flowchart

a) Optimization problem formulation

Starting from the proposal(s) selected with qualitative criteria, designers have to formulate the optimization problem including the known specifications or hypotheses. Once the formulation is clear, the designer's task is to create the appropriate model according to this formulation. They often realize during this step that it is impossible to create models that fit the formulation and they need to update the formulation accordingly.

After the concept and the formulation of the problem are properly expressed in the analytical models, optimization can be performed using the gradient-based algorithm. Usually, whether the optimization converges to a solution or not, the engineer will have to refine the optimization problem formulation. This is due to several factors; three of them are explained here:

(1) The designer did not think to formulate "obvious" or "natural" (for them) choices in the design. In this case the algorithm will take advantage of the formulation vulnerability and offer an unrealistic solution. For example, if the necessary thermal model for an inductor has been forgotten and the only remaining constraints are saturation and efficiency, the algorithm will suggest an incredibly

small inductor!

(2) The problem is over constrained and the algorithm does not have enough degrees of freedom.

(3) The problem is under constrained and the algorithm converges to an invalid domain in the model space (which results in infinity values, etc.).

Our experience shows that formulating the optimization problem is one of the biggest challenges facing users of the proposed approach. Several chapters of this thesis will be devoted to this task.

Once the optimization produces satisfactory results, the designer will be able to submit specifications and negotiate the specification limits if necessary.

b) Specification negotiation based on optimization results in the imaginary world

The specifications of a system can be evaluated and refined by the following methods: simple optimization in the imaginary world, Pareto curves and parameterized optimization curves.

Indeed, it should be noticed that if there is no solution in the imaginary world with the continuous variables, then there will be no solutions with discrete variables either and as such they do not need to be explored (Figure *6*).

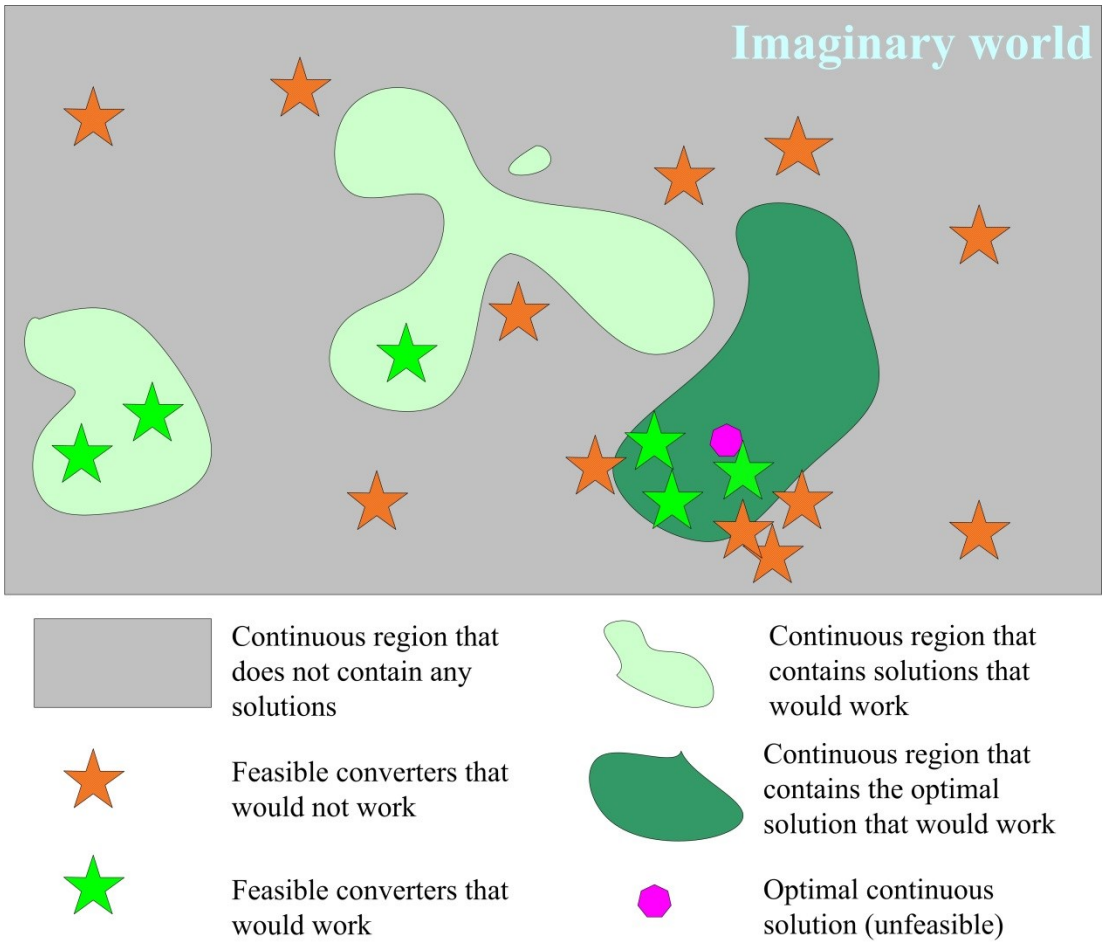
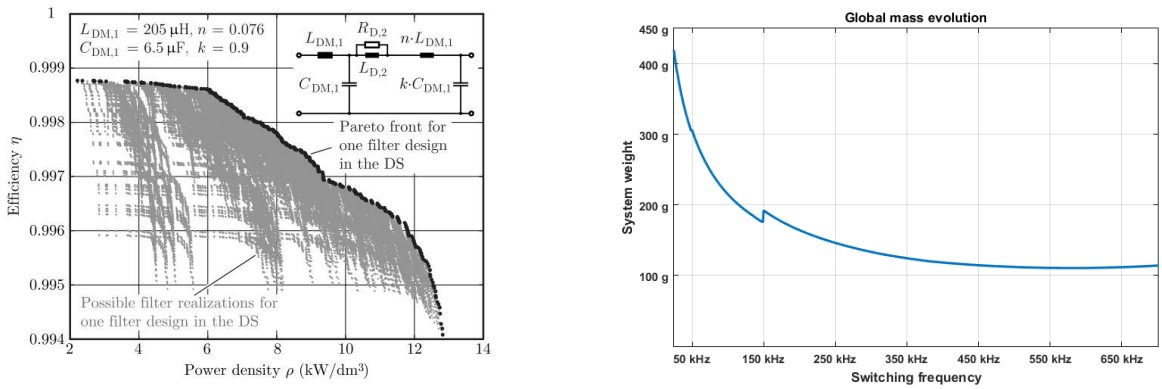


Figure *6*: Imaginary world in power electronics illustration

In addition, when the requirements around the static converter are not yet fixed, it is possible to trace Pareto curves (to find the optimal point between two divergent objective functions) or parameterized optimization curves (objective function or requirement plotted as a function of another requirement or design variable). For example Figure *7* (a) shows a Pareto front as a function of efficiency and power density for the output filter of a 10-kW, four-quadrant, three-phase, switch-mode controllable AC power source (CPS) from [13]. Figure *7* (b) shows a parameterized curve for the variation of the global weight of a simple Buck converter as a function of its switching frequency [14].



(a) (b)

Figure 7: Pareto front (a) and parameterized (b) curves examples from respectively [13], [14]

c) Optimization of the system with the negotiated requirements to design the prototype

Designing a system in the imaginary world (Figure *6*) it is equivalent to removing the barriers that come from the discrete variables in the system. It means that the designer can imagine solutions that are not achievable in reality thus moving away from conventional designs. This can be a source for new ideas. When the requirements negotiation phase is successfully completed and the designer is confident that the design is feasible, final optimization is performed in the continuous domain in the imaginary world with the negotiated set of specifications and, why not, some new converter architecture proposals!

Then the designer needs to translate the optimal imaginary solution into a real world implementation. It is possible to run a discretization process to define a practical converter that can be prototyped. If experimental results confirm the designer's expectations, he/she can refine the converter design based on first prototype results. For example, with a better idea of the mechanical assembly, the switching cell layout parasitic elements can be optimized, and a more accurate model of the magnetics (e.g. a finite element model) can help in reducing the parasitic capacitances.

3) Summary of the proposed approach

This approach provides a way to obtain an optimized industrial product with efficient risk management during the specification negotiation phase.

To conclude, as for all design processes, it is sometimes necessary with this approach to go back to a previous step in the process (there will still be some iterations), but hopefully the optimizations will accelerate the optimization problem formulation, specification negotiation and prototype design phases without too much time spent on modeling.

4) Introduction of the proposed approach vocabulary

A static power converter is constructed from electronic components that are selected in accordance with the converter topology and the converter's requirements (performance criteria, etc.) to work under a certain control strategy. From this, we can define four classes of design variables: continuous variables (C), discretized variables (D), numerically discrete variables (N) and variables related to the technology or topology choices (T).

- The **continuous variables (C)** are the physical continuous parameters of a power system (switching frequency, power, voltage and current levels, etc.)
- The **discretized variables (D)** are those that are physically continuous but industrially discretized (such as electronic components (transistors, capacitors, wires, etc.)).
- The **natural number discrete variables (N)** are the variables in the systems that are constrained to natural numbers for practical purposes (number of turns of a transformer, number of levels of a multi-level converter, etc.)
- The **technology or topology choice variables (T)** are those variables that only have distinct values (as topology choice, switching choice (zero-voltage, zero-current, synchronous, etc.) or technology choice).

III. DETAILED DESCRIPTION AND IMPLEMENTATION OF THE GRADIENT BASED OPTIMIZATION ALGORITHM SQP

A. Gradient-based optimization algorithm SQP

A gradient-based optimization algorithm uses, as its name suggests, the gradient from the optimization model to find the optimal point and to solve the constraint problem.

1) SQP algorithm optimum search method

These algorithms are able to search in the right direction by using the partial differentiation of the optimization model outputs with the inputs, i.e. the model Jacobian matrix (Figure *8*, Eq. *2*).

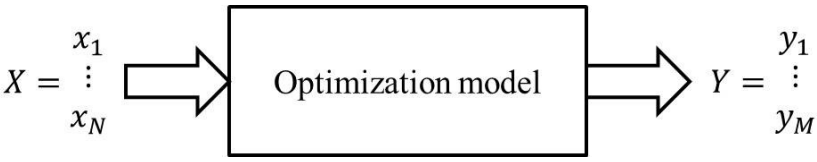


Figure *8*: Optimization model framework

$$\frac{\partial Y}{\partial X} = \begin{pmatrix} \frac{\partial y_1}{\partial x_1} & \cdots & \frac{\partial y_1}{\partial x_N} \\ \vdots & \ddots & \vdots \\ \frac{\partial y_M}{\partial x_1} & \cdots & \frac{\partial y_M}{\partial x_N} \end{pmatrix} \qquad Eq.\ 2$$

A Gradient-based optimization algorithm needs an initial point from which to start searching. Figure *9* illustrates this point. It shows a 2-dimensional constraint optimization problem with Y as the objective function to be minimized and X as the optimization input variable. The best initial point is the red and white target symbol: it only takes 3 iterations and 4 Jacobian matrix computations for the algorithm to find the global optimal point. However, if the starting point is located as shown by the blue and white target symbol, the algorithm can get trapped in a local minimum. The worst case is the red and purple target: the algorithm is stuck against a constraint barrier.

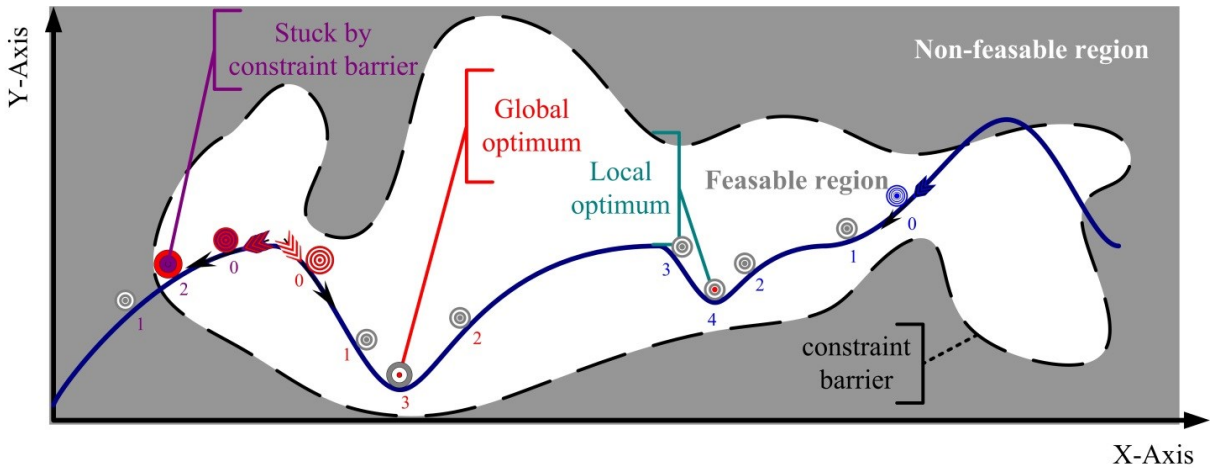


Figure *9*: Illustration of optimal point search using a gradient-based optimization algorithm

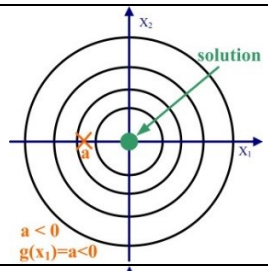
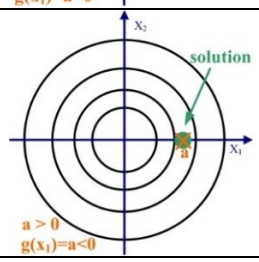
2) SQP algorithm constraints management

Constraint management is essential for an optimization algorithm to be used for highly constrained product design. The heuristic algorithms use the penalization technique, i.e. if a constraint is violated the objective function to be minimized is given a penalty. On the other hand, the SQP algorithm makes use of the Kuhn-Tucker conditions and directly solves the constraints thanks to gradient information as soon as constraints are "*active*" (i.e. when the previously computed point is on the wrong side of a constraint limit). Eq. *3* gives the Lagrange function of the optimization problem with λ as the Lagrange multiplier.

$$\begin{cases} \nabla Y(X) + \sum_{1}^{m} \lambda_j \nabla g_j(X) = 0 \\ g_j(X) = 0 \\ \lambda_j \geq 0 \end{cases} \qquad Eq.\ 3$$

Therefore, if one or more constraints are "activated", the Kuhn-Tucker will transform the inequality equations $g_j(X) \leq 0$ into several linear equations to be solved (an easy task for a computer). An example [15] with a basic mathematical problem is illustrated below in Table 3. It shows the efficiency of the SQP algorithm for quadratic problems as well as the necessity to accurately compute the gradient.

Table 3: Kuhn-Tucker conditions simple example from [15]

Problem definition:	$minimize\ Y(x_1, x_2) = {x_1}^2 + {x_2}^2\ \ with\ the\ constraint\ g_1(x_1, x_2) = a - x_1\ \leq 0$			
Constraint state	**Equations to solve**	**Linearized equations**	**Solution**	**Figure**
Inactive: $g_1(x_1, x_2) = a - x_1 \leq 0$	$\nabla Y(X) = 0$	$\begin{cases} 2x_1 = 0 \\ 2x_2 = 0 \end{cases}$	$\begin{cases} x_1 = 0 \\ x_2 = 0 \end{cases}$ 1 iteration	
Active: $g_1(x_1, x_2) = a - x_1\ > 0$	Lagrange function is : $\begin{cases} \nabla Y(X) + \lambda_1 \nabla g_j(X) \\ g_1(X) = 0 \\ \lambda_1 \geq 0 \end{cases}$	Lagrange function is : $\begin{cases} 2x_1 - \lambda_1 = 0 \\ 2x_2 = 0 \\ a - x_1 = 0 \\ \lambda_1 \geq 0 \end{cases}$	$\begin{cases} x_1 = a \\ x_2 = 0 \\ \lambda = 2a \end{cases}$ 1 iteration	

B. SQP algorithm implementation

1) Issues

Gradient-based optimization algorithms are so powerful in that they are able to handle hundreds of design parameters while finding an optimal point with high accuracy. The drawbacks of using such an algorithm in practice are:

a) The algorithm needs a well-chosen initial point and carries a risk of becoming stuck in a sub-optimal location

b) The SQP algorithm cannot test and analyze different proposals simultaneously since there are no continuous and differentiable transitions between each of them.

c) The need for model gradients, i.e. continuous optimization models

d) The exact gradient has to be found otherwise the algorithm will not succeed in finding the optimal point

2) Possible solutions

Issue (a) can be readily solved using the hybridization optimization technique combining the gradient-based and the heuristic algorithms: this consists of setting several initial points at random for the gradient-based algorithm to solve. This technique increases the domain coverage.

Issue (b) cannot be solved but can be mitigated by using scripting such that each concept is optimized sequentially and their optimization results are then sorted; this facilitates analysis by the designer.

Issue (c) will be discussed in detail in this thesis since it represents a major challenge in the power electronics field.

Finally, issue (d) is a matter of selecting the proper method and tool for the optimization model and algorithm implementation.

3) Optimization tool choice for using SQP algorithm

This thesis has benefited from the use of a specific optimization tool named CADES dedicated to electro-technical optimization. CADES (Component Architecture for Design of Engineering Systems) was first developed in the G2Elab laboratory. Development was continued by the company Vesta-System and the latest versions are available for professional use. This tool is a software environment integrating several services that allow the designer to focus on problem formulation and results analysis [16]–[18].

```
10
11  Y1 = 2*x1+x2;
12
13  Y2 = pow(Y1,2) + pow(Y3,2);
14
15  Y3 = 3*x1-x2;
16
```

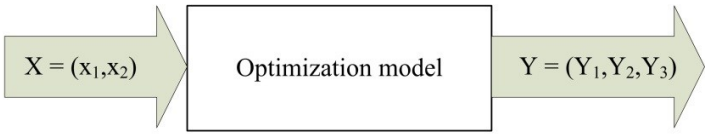


Figure 10: SML language features example

Figure 11 shows an overview of the CADES framework which has been designed to be ergonomic for designers. For example, the dedicated modeling language SML (System Modeling Language) Figure 10 is designed such that the order of the equations in the model file does not matter; in the example above, we can see that the statement defining Y2 uses Y3 even though the definition of Y3 comes after Y2.

In addition, the selected optimization algorithm is automatically linked to the model: an HMI (Human Machine Interface) helps to define the type (free, fixed, variable, bounded or objective) and the bounds of the behavior. The data is saved as a set of specifications for the optimization problem. When a gradient-based

optimization algorithm is used, the optimization service is able to determine the exact Jacobian matrix of the model thanks to the Automatic differentiation Adol-C integrated within CADES [19]. This is much more efficient than computing finite differences and means that the designer does not have to write equations for the derivatives.

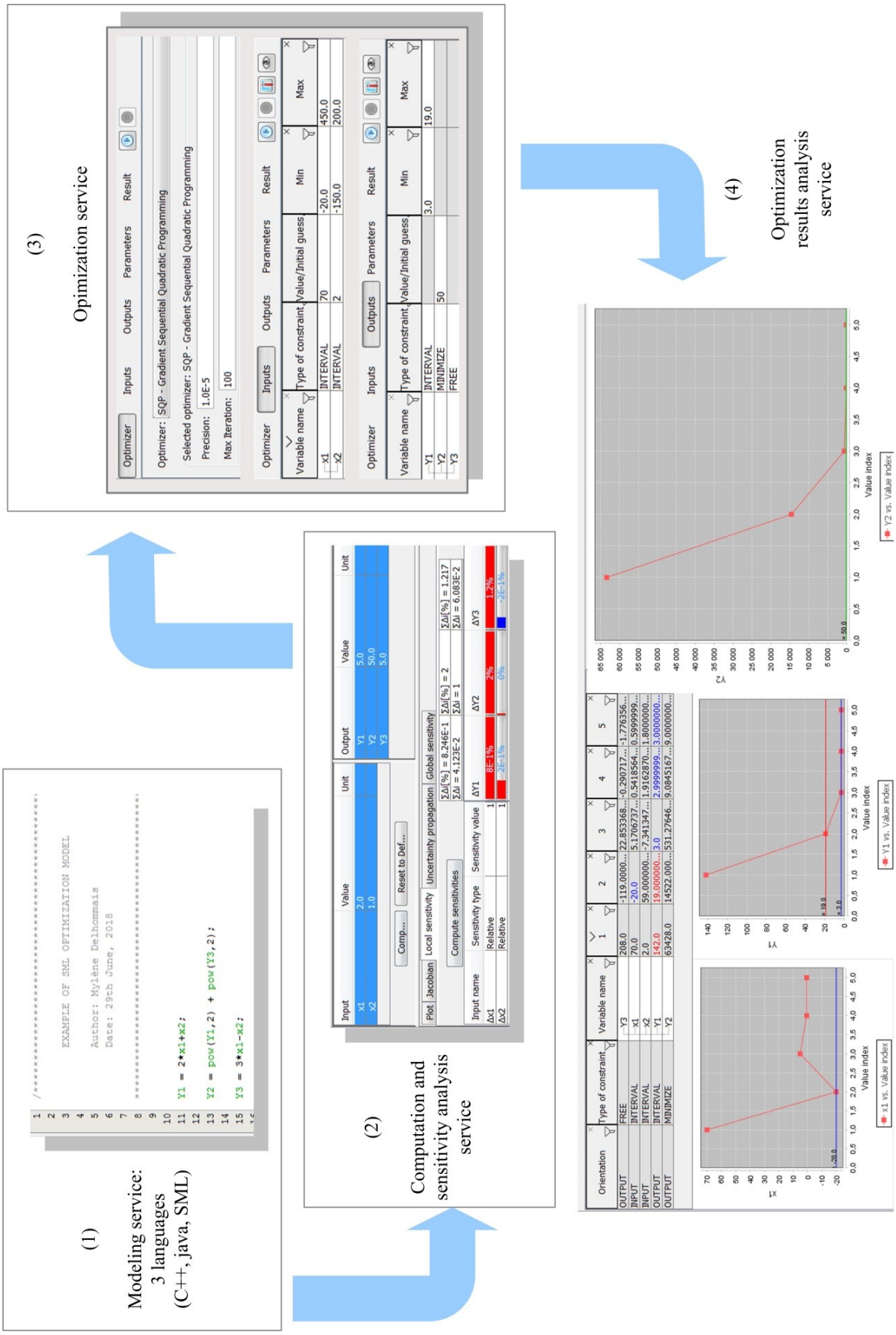


Figure 11: CADES framework

IV. CONCLUSIONS

In the early steps of a design, the number of degrees of freedom is high, which means that the architecture proposals tree can contain up to a dozen of possibilities (called branches). Unfortunately qualitative criteria will rarely suffice for the removal of all concepts leaving only one: quantified data is therefore necessary. Over the last few decades, many design methods have been proposed, but pre-design methods have been largely left aside.

In this thesis, a new pre-design approach is proposed, which:

- helps the designer in negotiating the requirements,
- has the ability to explore a wide range of solutions for each architecture proposal in a short time,
- optimizes each proposal, this helps the designer compare them objectively.

The approach involves designing in an imaginary world (where discrete design parameters are expressed as continuous variables) before returning from the optimal imaginary solution to one that is discrete. Table 4 indicates the risks inherent with the use of this new approach in academia and industry regarding human resources and tools.

Table 4: Risks of a novel pre-design approach

Category	**Risk**
Human resources	• Difficulty in adapting to a new design philosophy • Cost of training
Numerical tools	• Poor capitalization of case studies and models (lower cost efficiency) • Cost of the software licenses, maintenance, services

Several kinds of optimization algorithm exist but the 1st order optimization algorithm SQP seems to better fit with the new approach requirements, i.e. it is particularly efficient for testing the formulation of the problem in the imaginary design space.

The challenges of using such an approach and algorithm are:

- making continuous and differentiable optimization models of power converters,
- computing exact derivatives of the model parameters.

The second point is already solved using a tool dedicated to optimization for electro-technical designers.

The first point will be developed in several chapters of this thesis since it is the most challenging task for optimizing power converters in the imaginary world.

The proposed approach has been applied to a real project throughout this thesis in order to provide a concrete illustration of the methodology and validate the proposed approach in the real rather than imaginary world…

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Chapter 3: A Design Challenge for Illustration

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I. STRATOBUS PROJECT DESCRIPTION

Stratobus is a stratospheric airship (Figure *1*) midway between a drone and a satellite regarding its mission.

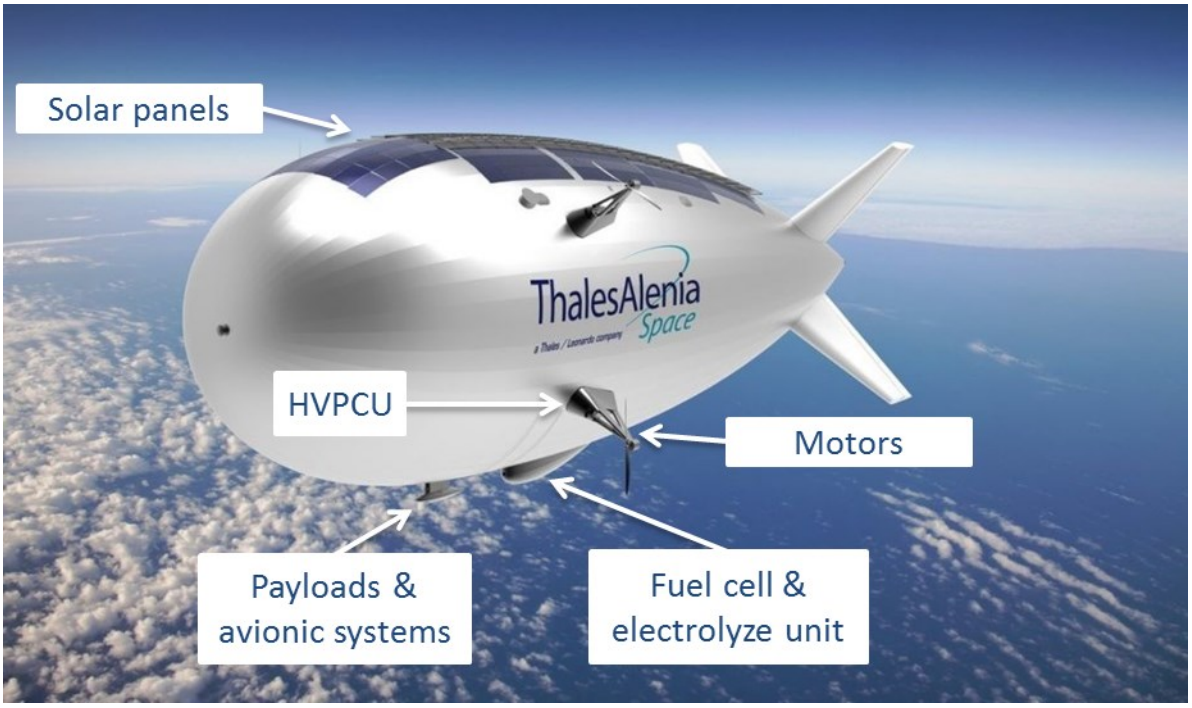

Figure *1*: Stratobus airship illustration

Stratobus's missions can either consist of surveillance and/or communications (both military and civilian). The objectives of the system integrator Thales Alenia Space are the following:

- The ability for the airship to be stationary at 20 km in the Stratosphere
- A full autonomy of 1 year
- The ability to embed 250 kg / 5 kW payloads (surveillance & communication systems) for customers

A. A very complex and ever evolving system

There are thousands of constraints that the system integrator should take into account but their main challenge is reducing the weight of the Stratobus functional systems in the aim to embed more payloads: the lighter the functional systems, the better it is for the integrator. This is the reason why Thales has the huge and difficult task of finding the best trade-offs between all the sub-systems so as to minimize the global weight of Stratobus.

For example the technology of the solar panel will influence their number, weight, location and power which, in turn, will influence the storage device choice, weight, etc., the motors' design and so the ability to handle the Stratospheric wind, which itself depends on the form and material of the envelope, etc. These examples of interactions between subsystems are not exhaustive. What is important to keep in mind during the preliminary design phase is that everything is linked and a change in one element of a subsystem can impact the feasibility

and design of all the other subsystems.

Another challenge for the system integrator is that the stratospheric environment is different from that of space and the atmosphere, which means that environmental challenges such as radiation, ozone, low pressure, extreme temperatures, etc. have to be studied and defined. This process results in constraints and design parameters being added or removed from subsystems' requirements.

The combination of the unknown environment and need for trade-offs make the global system hard to optimize. The integrator has no choice but to perform iterations to converge to the optimal solution. Every new iteration, the set of specifications evolve and all subsystems designers have to reevaluate the expected performance of their system.

This project is thus a concrete example (but not exhaustive) of the need for a new approach for pre-design activities, especially for the airship's static converters whose main function is to connect the different electrical systems together. This kind of system is indeed particularly subjected to requirement evolution. Being able to predict key performance parameters of the converter (weight, efficiency, ripple etc.) as a function of a change to the operating point or some of the requirements thanks to Pareto or optimized parameterized curves can help the designers significantly.

B. A tight timeline

Optimization is a necessary part of the design activity for this highly innovative airship. However project resources and available time are not unlimited. For this project, Thales has proposed the following schedule [1] (Figure *2*). From the 26th April, 2016 to the SRR milestone, Thales and their partners collaboratively developed several concept baselines. During this half year period systems designers reevaluated feasibility and weight for each baseline. Then, during the preliminary design phase that lasted 6 months more, the main architecture was defined but the specific requirements continued to evolve, or were still to be defined for the PDR milestone. The critical design phase consists of designing and testing the critical systems of Stratobus (the main functions, etc.) as well as trying to define limits for the less critical requirements as the main requirements mature.

Finally, the project timeline adds a challenge for the designers: exploring a large space of possibilities in a short time. Hopefully the approach proposed in this thesis will help the designers to meet this challenge.

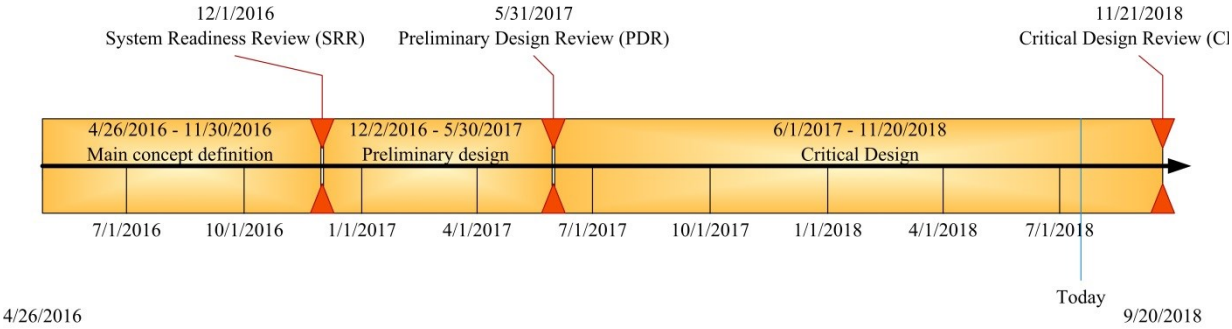

Figure *2*: Stratobus main time line from [1]

II. Global architecture choices of Stratobus High Voltage Power Conditioning Unit (HVPCU)

The concept of Stratobus regarding its energy supply is summarized in this section. For both complexity and confidentiality reasons, only an overview is given. This section concerns only the main concept definition phase and preliminary design phase.

A. Stratobus energy supply: HVPCU environment

During the day the airship's solar panels provide the required electrical energy for the electrical motors, avionics systems, payloads and an electrolyzer unit. During the night a fuel cell uses the hydrogen produced during the day by the electrolyzer unit to deliver the energy to the electrical systems listed previously. Figure *3* is the chosen global architecture by Thales to implement the energy cycle described above (note that for obvious confidentiality reasons, many details and values will be omitted or a little modified).

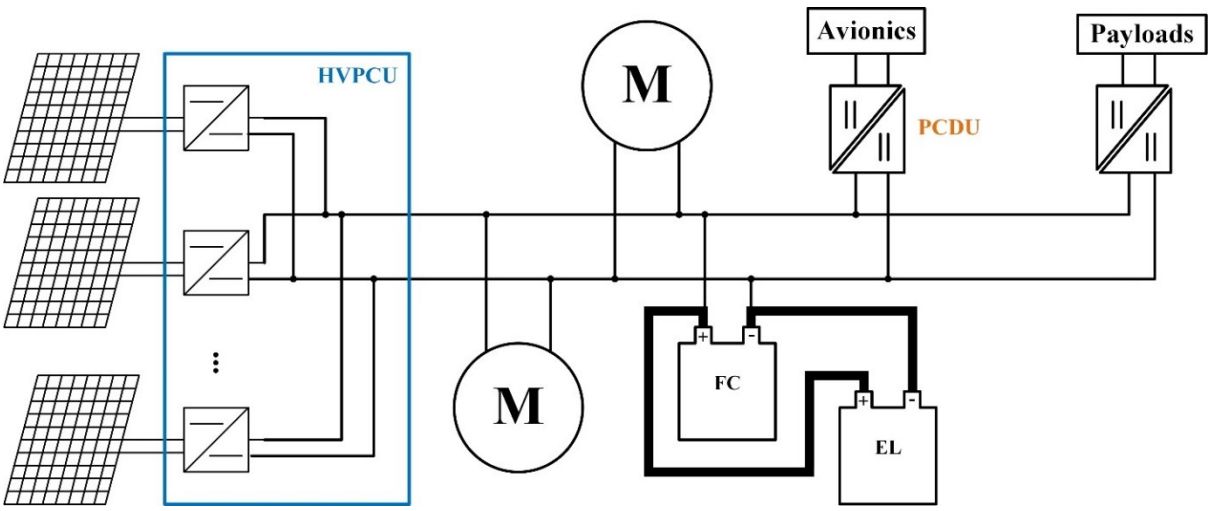

Figure *3*: Global electrical architecture of Stratobus

In order to exploit as much of the solar panels' capacity as possible and so limit their number and weight, a static converter should perform Maximum Power Point Tracking (MPPT) and connect this energy source to the DC bus that supplies the Stratobus with electrical energy. There are in fact as many DC-DC converters as solar

panels (several dozen) and these converters are grouped together in the High Voltage Power Conditioning Unit (HVPCU) which the French company Tronico has the responsibility of designing.

B. HVPCU DC-DC topology selection through the architecture proposals tree

1) Converter main constraints

The DC-DC converters of the HVPCU should be optimized regarding their weight (it is the **main** objective). The efficiency is treated more as a constraint for several reasons. Firstly, a low efficiency would mean that the number of MPPT converters and solar panels would have to increase to compensate the energy loss. The second reason is the size of the wiring (and so the weight) between the solar panels and the converter that would also increase. Finally the third reason is the size and weight of the cooling system, these factors would increase if the thermal energy due to losses to be dissipated is too high.

The cooling system was not defined before the PDR milestone. Because of this, it will not be described in this thesis.

Each DC-DC converter needs to convert a wide input voltage (about [450 - 800] V) and output voltage (about [200 - 430] V) with a power range of [0 – 5] kW. For reasons explained earlier these values have evolved several times during preliminary design activities (although they have remained within the same order of magnitude).

2) Converter topology selection

The architecture proposals tree of these DC-DC converters has to be built, as previous chapters described, drawing on the experience of Tronico's power electronics engineers.

The application and the voltage levels involved are such that the converters do not need to be isolated.

Considering the more classical non-isolated DC-DC topologies; a quick comparison has been provided between Buck, Interleaved Buck, Buck-Boost and Single-Ended Primary Inductor Converter (SEPIC) in Table 1. Simplified schematic diagrams for these topologies are shown in Figure *4*.

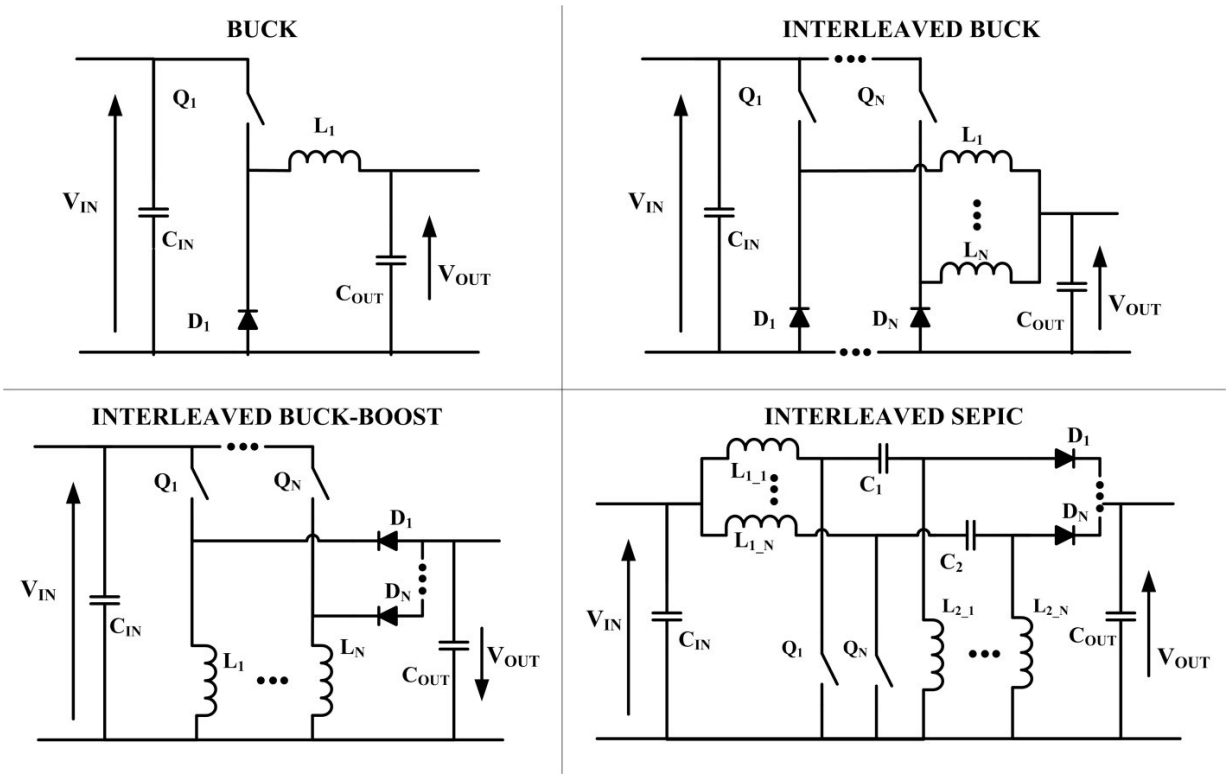

Figure *4*: Compared DC-DC converter topologies schemes

Selecting the right topology is a matter of finding a good compromise and limiting the risk of non-feasibility at the end of the project. For example, regarding this criteria SEPIC topology presents more risks than the others: the coupling capacitor needs to be large and would have to be able to work in a near-vacuum space environment. Also, its semiconductors, as well as satisfying radiation constraints, would have to handle a very high voltage. These are two reasons to discount this topology from the architecture proposals tree. The Buck-Boost topology also has the disadvantage of highly constraining the transistor, it is less efficient than a Buck topology and the output voltage polarity is inverted. For a simple Buck topology, input and output current ripple is relatively high. It is not ideal because the solar panels and the eletrolyzer unit are sensitive to these phenomena (premature aging) and reducing the ripple increases the weight of filtering components unacceptably. The Interleaved Buck Converter (IBC) is therefore the best solution regarding global weight power density. Finally, Tronico's engineers have a very good understanding of the advantages, design difficulties and risks associated with this topology: they have the needed experience to react quickly to requirement changes, to provide data on the resulting impacts and to make the discussions with other partners effective.

The IBC topology can use single inductors per phase or coupled inductors. The first option is less complex than the second one and is more suited to the design time scales. Nonetheless, a design based on coupled inductors is kept in mind in case the weight of the single phase inductor IBC is an issue.

Table 1: Non isolated DC-DC converter topologies comparative table

Criteria/Topology	Buck	Interleaved Buck	Interleaved Buck-Boost	Interleaved SEPIC
Power (Able to convert up to 5 kW?)	😐	☺	☺	☺
MPPT (MPPT algorithm simplicity implementation)	😐	😐	☺	☺
450 V to 430 V conversion	😐	😐	☺	☺
Constraint on active semi-conductors (Maximum voltage on the transistor?)	😐 Vt_max =Vin_max = 800 V	😐 Vt_max = Vin_max = 800 V	☹ Vt_max = Vin_max + Vout_max =1230 V	☹ Vt_max = Vin_max + Vout_max = 1230 V
Efficiency	😐	😐	☹	☹
Is the converter normally off?	☺	☺	☺	☹
Output voltage polarity?	☺ Non-inverted	☺ Non inverted	☹ Inverted	☺ Non inverted
Redundancy	☹	☺	☺	☺
Manufacturing feasibility	☺	☺	😐	☹
Input/output current ripple	☹	😐	😐	😐
Design simplicity	☺	☺	☹	😐
Cost	☺	😐	☹	☹
Weight	😐	☺	😐	😐

3) Converter conduction mode selection

After selecting the converter topology, the conduction mode is chosen among:

- continuous (CCM) for a range of power [Pmax/3 ... Pmax],
- discontinuous (DCM) for the entire operating range,
- optimized CCM-DCM, i.e. going between both modes depending on the operating point.

Figure *5* shows the power components' ideal current and voltage waveforms for continuous and discontinuous modes.

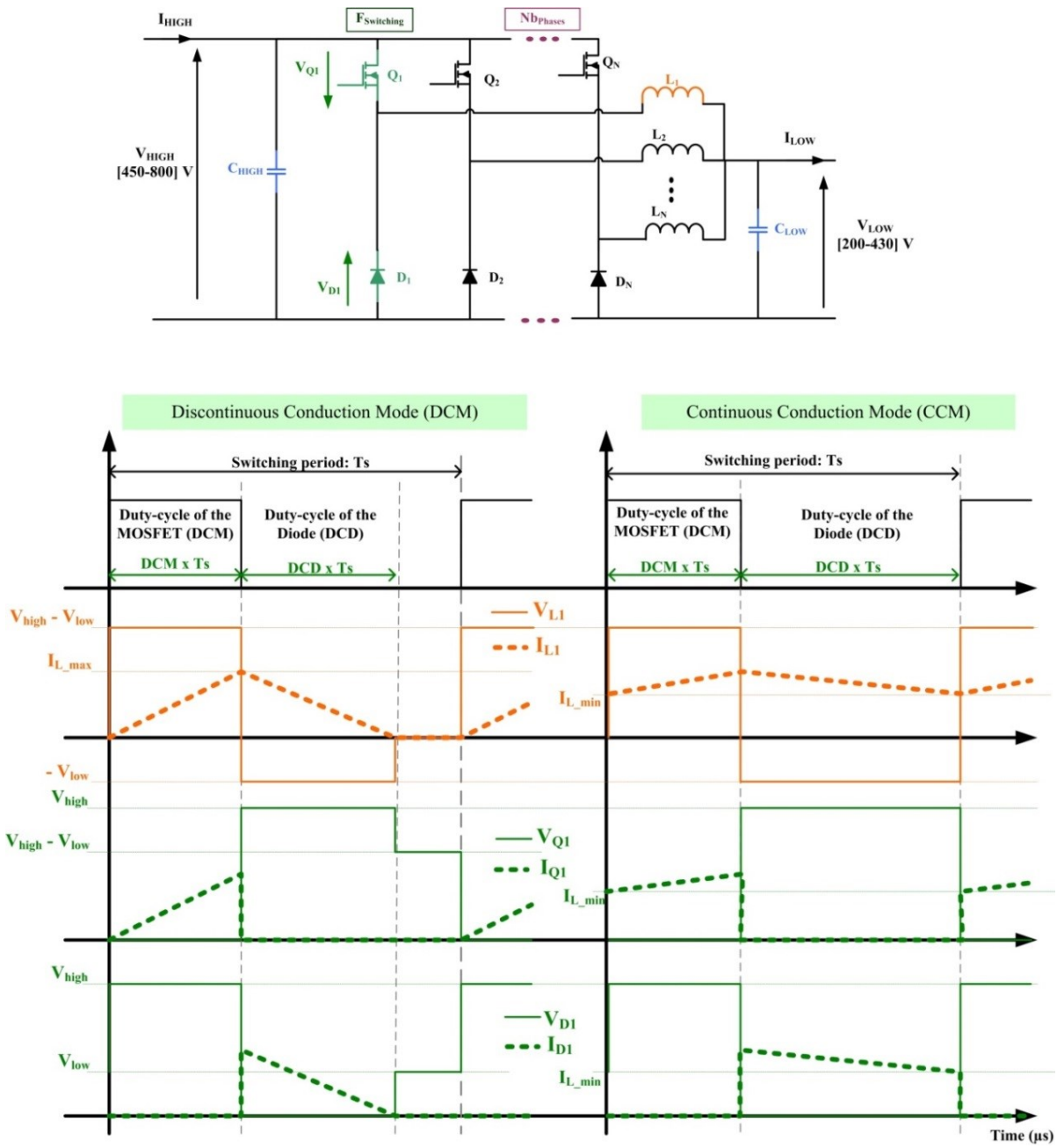

Figure 5: Interleaved Buck Converter schematic and components ideal current and voltage waveforms

Table 2 gives the advantages and disadvantages of various options combined with the conduction mode with respect to the main objective that is minimizing the weight while ensuring continuous service of the converter. For example the use of the optimized CCM-DCM conduction mode would require an additional current sensor which complicates the design of the converter's regulation: it is therefore removed from the possibilities tree due to this qualitative criterion. But quantitative data is needed to decide between continuous and discontinuous conduction modes.

Table 2: Comparison of conduction modes for the IBC

Criteria	DCM	CCM	Optimized CCM-DCM
Control/Command complexity	☺	😐	☹
Inductors size (per phase)	☺	☹	☺
Number of required phases	☹	☺	😐
Inductor losses	☹	☺	☺
Switching losses [2]	☺	☹	☹
Input/Output current ripples and EMI (impact filter weight)	☹	☺	? depends on the EMI requirements at low power: not defined before the PDR
Statement	?		**Eliminated**

4) Converter switching mode selection

For both modes the classical switching technique has been retained since synchronous switching is slightly more complex. The input and output filtering topologies will be chosen in the same way: 1st order topology is selected for its simplicity. If it proves to be insufficient, it will be modified.

5) HVPCU DC-DC converters global architecture proposals tree

Figure *6* shows the final set of the HVPCU DC-DC converters global architecture proposals tree.

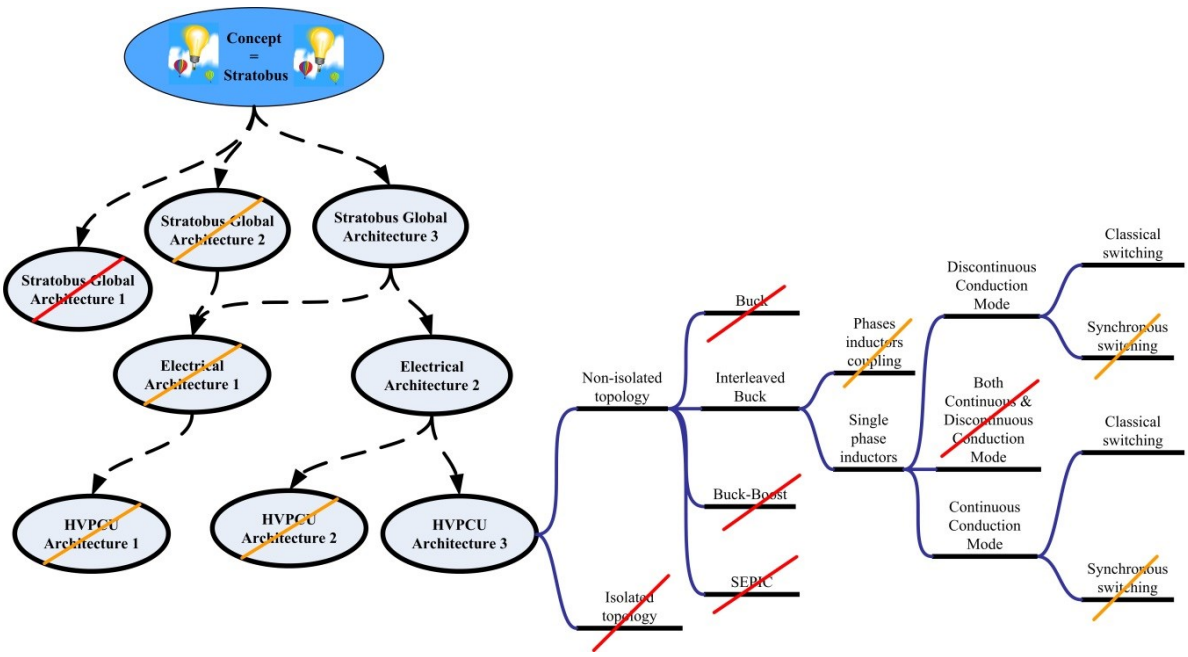

Figure *6*: HVPCU DC-DC converters architecture proposals tree

However, the task of topology and technology pre-selection is not finished: the choice of the number of phases for the IBC and power components' technology is discussed in the next section.

III. DETAILED DESIGN CHOICES OF HVPCU

These detailed concepts now have to be evaluated with mainly quantitative data. The key specifications of the DC-DC converters (although subject to some modification during the preliminary design phase) therefore need to be taken into consideration.

A. Converter main specifications at the beginning of the project

The converter's main specifications are listed in Table 3. The abbreviations "THD", "NA" and "TBD" mean "Total Harmonics Distortion", "Not Applicable" and "To Be Defined" respectively.

Table 3: HVPCU DC-DC converter specifications

Criteria	Minimum Value	Maximum Value	Conditions/Remarks
Power density	7 kW/kg is a must	10 kW/ kg nice to have	Depends on the following specifications complexity
Input power	0 W	4,5 kW // 5 kW for peak value	For the entire of input/output voltage ranges (at this initial stage in the project)
Input voltage	450 V	800 V	For a power range TBD
Output voltage	200 V	430 V	For a power range TBD
Efficiency	96 %	NA	For a power range TBD
Input/Output current THD	NA	5 %	For a power range TBD
Cooling temperature	-40 °C	65 °C	For a power range TBD
Ambient temperature	TBD	85 °C	
Ambient pressure	0.07 bar	1 bar	
Wiring input impedance/line	0.75 µH	TBD	Minimum value is "worst case" while maximum value is "better case"

Besides the numerous items that are TBD, the values in Table 3 are subject to several changes during the preliminary design process. Any designer that sees so many unknown parameters will say it is nearly impossible to design this converter and quantify its expected performance. These unknown parameters come from the fact that the number of solar panels and their technology is not fixed at the beginning of the project, as well as the number of motors and the number of hydrogen unit cells. It is the motivation of the approach proposed in this thesis: during the preliminary design phases, several decisions have to be taken without complete knowledge. The approach should be able to rapidly produce quantified information to the system integrator.

Since the values given in Table 3 should remain within the same order of magnitude during the design phase it is appropriate to select technologies and topologies for the converter.

B. IBC technological choices through the architecture proposals tree

Figure 7 shows the DC-DC converter schematic after the architecture proposals removal phase. As previously noted it is an IBC. The colored items indicate design parameters. In the IBC each phase is identical to the others, this is why the design parameters associated with only one of the phases is shown.

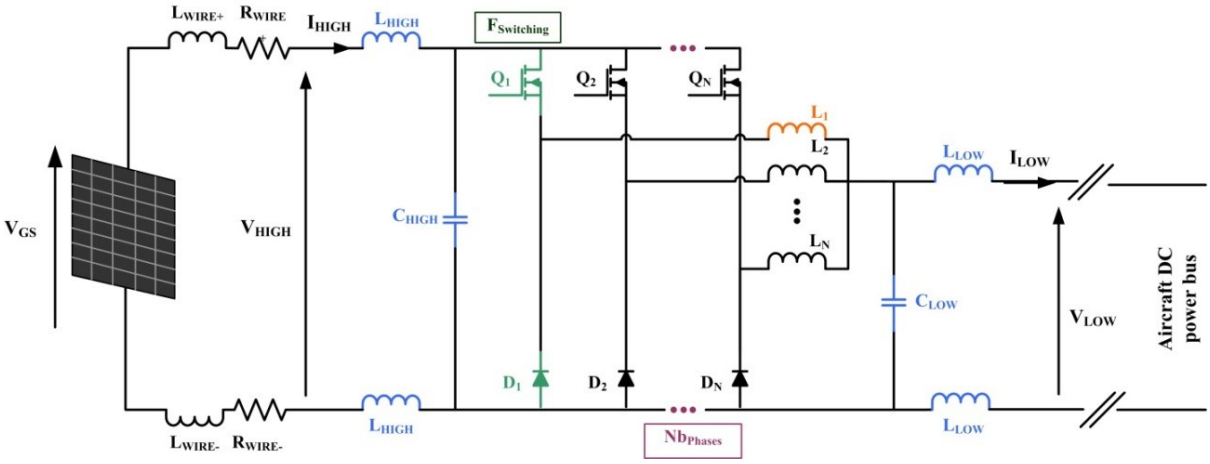

Figure 7: IBC to optimize schematic

The components L_{HIGH}, L_{LOW}, C_{HIGH}, C_{LOW}, MOSFET, diode and L_{PHASE} have to be chosen among all components that are available on the market. Thankfully the search space can be reduced by selecting specific technologies that seem to better match with the application.

1) Semiconductors technology selection

In this case study, the semiconductors will have to switch at 800 V and to be normally OFF: 1200 V SiC N-MOSFET are well suited. Additionally they can switch faster than silicon devices allowing a pretty high switching frequency (up to 300 kHz) and so minimizing the weight of the passive components in the design.

2) Filtering components technology selection

Again, because the order of magnitude of the voltages, the environment and the functional objectives is known, two series of capacitors and a set of filtering inductors have been easily selected among Commercial Off-The-Shelf (COTS) components: the choice was limited. These components can be put in parallel or in series depending on the voltage and current constraints.

It should be noted that using COTS devices for the filtering inductors is the approach taken in here for reasons of manufacturing simplicity and low cost. If design testing indicates that the filtering requirement or the weight is an issue, then a custom design should be implemented.

3) Phase inductors technology selection

Based on their experience, Tronico's power electronics engineers know that the power inductors in an IBC are a large part of the electronic components weight and volume: customization is required, in other words commercial off the shelf (COTS) inductors are prohibited here. But due to the really high cost of fully customized inductor core and wire, the phase inductor L_{PHASE} should be designed thanks to an assembly of commercial parts. Figure 8 represents the architecture proposals tree of the inductor L_{PHASE}.

An inductor core without airgaps is preferred for manufacturing and mechanical reasons: the powder core material family is for now selected. The most suitable powder core material is unknown at this stage: no qualitative arguments have been conclusive. For the winding, there are two main materials (copper and aluminum) and several kinds. Copper Litz wire is for now voted in the aim of limiting skin effects. Strand diameter and number remain to be determined with a quantified analysis.

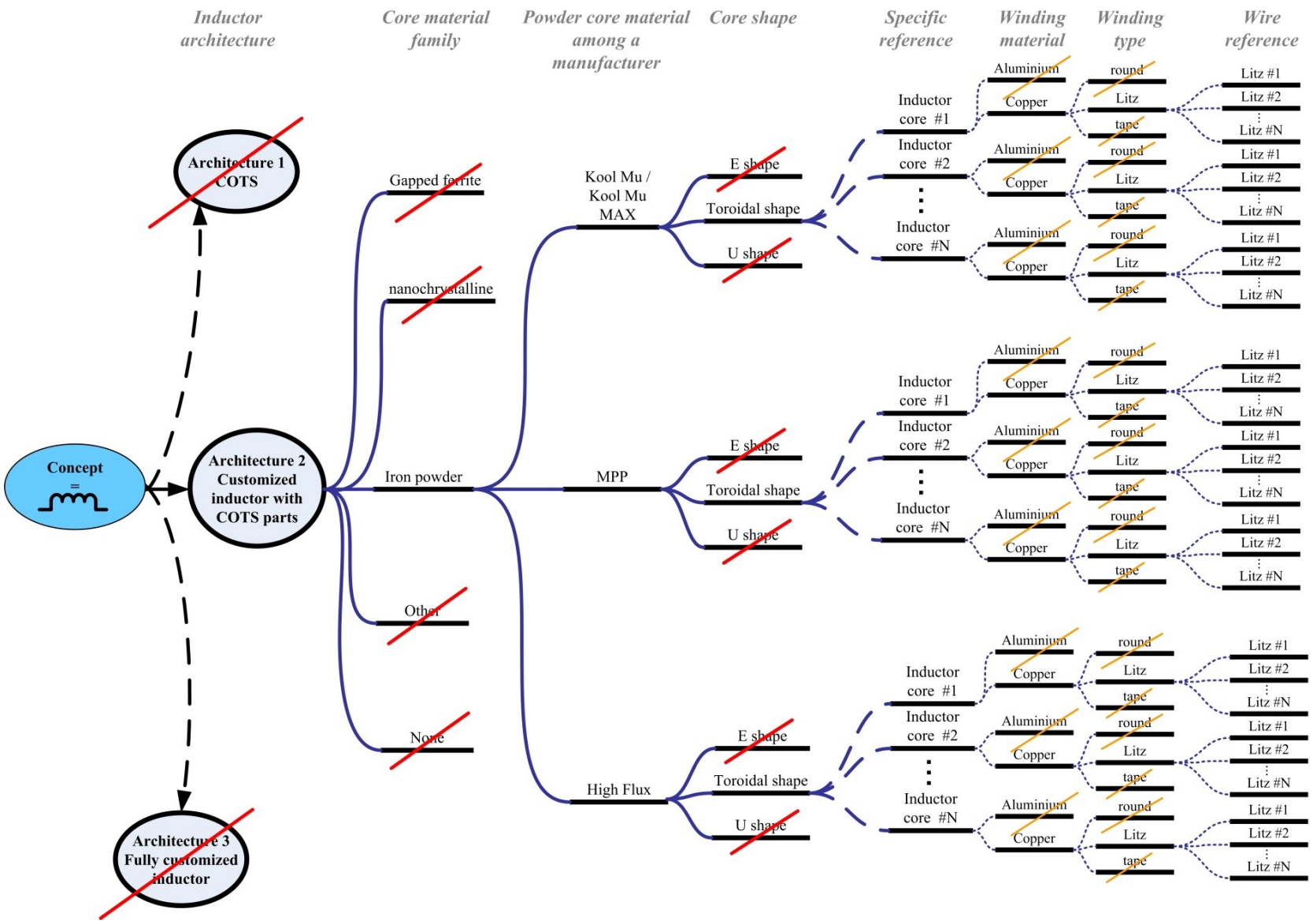

Figure 8: Architecture proposals tree for the IBC phase inductor

Table 4 gives the discrete design variables of the IBC design problem. Despite the efforts that have been made to restrain the search space, it is still impossible to test all the concepts because of the complexity of this combinatory problem (around $4.30 \cdot 10^{19}$ possible combinations). Actually, the only one continuous design variable is the switching frequency Fs. This number of possible combinations is particularly high since the problem formulation has been oriented for continuous optimization and not combinatory or manual design methods.

Table 4: IBC discrete variables of the architecture proposals tree

Design discrete parameter	**Abbreviation**	**Choices number**	**Design discrete parameter**	**Abbreviation**	**Choices number**
Number of IBC Phase	NBphase	6	Input single capacitor value	Chigh	17
Conduction mode	CD	2	Output single capacitor value	Clow	46
Inductor core material	material	3	Number of input capacitors in parallel	N_Chigh	15
Inductor core main permeabilities (14, 26, 40, 60, 125)		5	Number of output capacitors in parallel	N_Clow	15
Toroidal inductor core size (choice number /material/μ)	Dout, Din, H	[4 - 36]	Input single filtering inductor value @ 0A	Lhigh_max	17
Litz strand diameter (AWG 33, 36, 38, 40, 42)	DlitzLphase	5	Output single filtering inductor value @ 0A	Llow_max	17
Litz number of strands	nstrandLphase	15	Number of input inductors in series	Ns_Lhigh	5
Phase inductor number of turns	NturnsLphase	~100	Number of output inductors in series	Ns_Llow	5
SiC 1200 V MOSFET current rating	Cal_Imos	5	Number of input inductors in parallel	Np_Lhigh	5
SiC 1200 V Schottky diode current rating	Cal_Idiode	10	Number of output inductors in parallel	Np_Llow	5

This demonstrates the reasons why the method of pre-design in the imaginary world presented in chapter 2 will be applied on this preliminary design problem. The next chapters will detail the different steps of this method on the Stratobus DC-DC converters.

Furthermore, Appendix I presents other design methods of Interleaved Buck or Boost converters. But these methods have been used under a fixed set of specifications and could not be used to negotiate it.

IV. CONCLUSION

Stratobus is a wonderful innovative project. Unfortunately the timeline is incredibly short (less than 3 years) considering the activities that need to be completed:

- defining the overall system concept feasibility,
- defining the specifications of each sub-system,
- defining the technical proposals for each sub-system,

- performing pre-design on all of the sub-systems.

However, as stated in previous chapters it is during the concept analysis and definition phases that 85% of the development's critical decisions are made [3]. It is thus essential to improve the working methods dedicated to these phases. Indeed, the designers need methods and tools that show the various interactions between requirements, constraints and objectives of the project so that specifications negotiation and proposal is less of a challenge.

These are the reasons why a new efficient pre-design by optimization approach is so needed to help the designers in setting achievable specifications during the negotiation phases.

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Part B

Optimization problem formulation for predesign in the imaginary world

Chapter 4: Formulation of the Optimization Problem of Power Electronics Systems for Using Gradient-based Optimization Algorithm

Chapter 5: Evaluation Models of the Components Parameters and Converter Waveforms of the Interleaved Buck

Chapter 6: IBC power components losses and thermal models

Chapter 7: IBC Power Components Losses Models Compared to Experimental Data

Chapter 4: Formulation of the Optimization Problem of Power Electronics Systems for Using Gradient-based Optimization Algorithm

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I. INTRODUCTION

Thanks to the qualitative criteria, it has been possible to fix a majority of the technology or topology choice variables (T variables). It is now necessary to get quantitative data in the aim to finish the preliminary design of the Interleaved Buck Converter. Before getting these data, the optimization problem must be properly formulated. That is the subject of this chapter.

II. DEFINITION OF A MODEL

A. Main but not exhaustive characteristics of a model

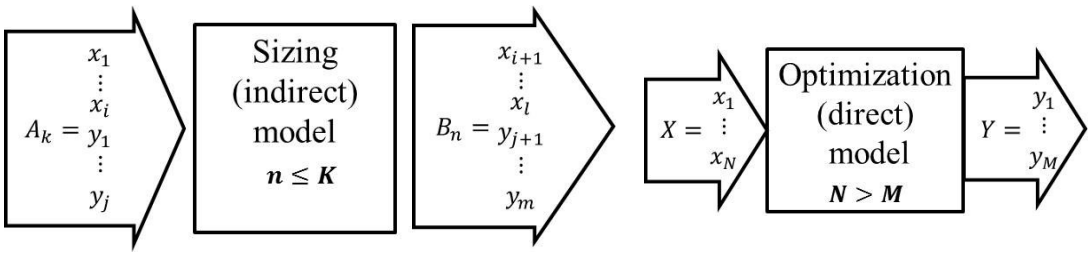
When speaking about a model, many questions arise to clearly define it:

(1) Should the model be made independently of the application?

(2) Should the model be made independently of its context, i.e. whatever case it will be used?

(3) Is the model indirect (sizing model) or direct (optimization model) or a mixed of?

In the "classical" sizing models, the input (A) and output (B) vectors can contain both performance criteria variables (y) and design variables (x). On the contrary, the optimization models should have only the design variables as inputs (X) and only the performances (Y) as outputs. As it is shown on Figure *1*, the input vector is bigger than the output vector for the optimization model whereas in the sizing model, the input vector must be smaller than the output vector [1]. Indeed, in the aim to efficiently compute the outputs, the sizing model generally needs to fix some inputs thanks to the designer hypothesis: the degree of freedom must be limited. A concrete example illustrating the difference between sizing and optimization model is given in the next section.



(a) (b)

Figure *1*: Illustration of indirect (a) and direct (b) models

(4) What are the required levels of accuracy and fineness?

(5) What is the nature of the model? Should the model be empiric or theoretic? Should the model be represented by circuit in the time or in the frequency domain simulations, finite elements, numerical

and algorithmic formulations or analytical equations?

B. Concrete example of the differences between a sizing and an optimization model

Figure *2* is a better practical illustration of the difference between sizing and optimization models of filtering capacitors.

a. Aim:

The capacitor should filter the current ripple ΔIout from the power supply of 2A within period ΔTs of 50 µs in the aim to limit the voltage ripple ΔVmax at a maximum value of 2V. The RMS current in each capacitor should not be up than their limit.

b. Hypothesis:

- The capacitors absorb all the RMS current, i.e. 580 mA (Eq. 1).

$$ICrms_{TOT} = \frac{\Delta Iout}{2 * \sqrt{3}} = 577\ mA \qquad \text{Eq. } 1$$

- There are only 3 available capacitors with the properties listed in Table 1.

Table 1: Available capacitors

Capacitor reference	Value (µF)	Maximum RMS current (mA)
C47	4.7	200
C33	3.3	300
C22	2.2	350

c. Sizing model

For a maximum voltage ripple of 2V, the necessary capacitance C_{TOT} is 7.2 µF (Eq. *2*).

$$C_{TOT}^{min} = \frac{ICrms_{TOT} * \frac{\Delta Ts}{2}}{\Delta Vmax} = 7.2\ \mu F \qquad \text{Eq. } 2$$

- Choice #1: Three C22 capacitors are set in parallel (first choice to fulfil the RMS current constraint). This choice does not fulfill the requirement of total capacitance value.

$$C_{TOT}^{choice1} = 3 * 2.2\ \mu F = 6.6\ \mu F \qquad IC1 = \frac{ICrms_{TOT}}{3} = 192\ mA$$

- Choice #2: Two C47 capacitors are set in parallel: the total capacitance is 9.4µF: it does fulfill the voltage ripple requirement. But the RMS current in a single capacitor does not fulfill the maximum RMS current requirement.

$$C_{TOT}^{choice2} = 2 * 4.7\ \mu F = 9.4\ \mu F \qquad IC2 = \frac{ICrms_{TOT}}{2} = 288\ mA$$

- Choice #3: Three capacitors of 3.3 µF. The total capacitance requirement is fulfilled and the RMS current in a capacitor being 193 mA, it also respect the RMS constraint.

$$C_{TOT}^{choice3} = 3 * 3.3\ \mu F = 9.9\ \mu F \qquad IC1 = \frac{ICrms_{TOT}}{3} = 192\ mA$$

d. Optimization model

Based on the selected values for the number of capacitors in parallel and their capacitance, the constraints are computed simultaneously thanks to (Eq. 3, Eq. 4, Eq. 5).

$$C_{TOT} = N_{capacitors} * C_{value} \qquad \text{Eq. } 3$$

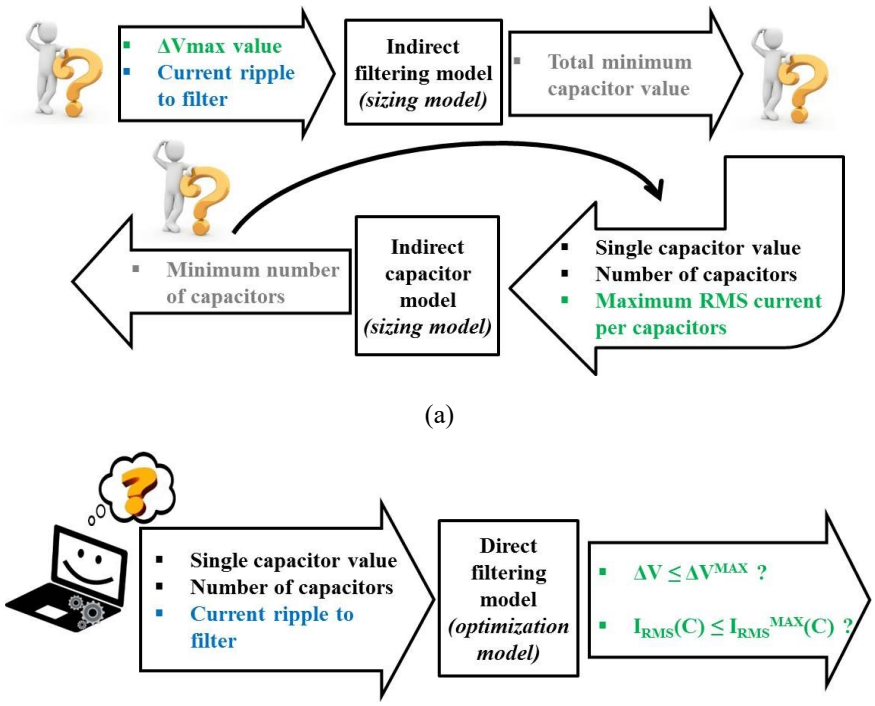
$$\Delta V = \frac{ICrms_{TOT} * \frac{\Delta Ts}{2}}{C_{TOT}} \qquad \text{Eq. } 4$$

$$IC = \frac{ICrms_{TOT}}{N_{capacitors}} \qquad \text{Eq. } 5$$

Then the algorithm can explore several solutions as in Table 2 and finally select the one that would also minimize or maximize the objective function as price, weight or volume.

Table 2: Possible associations of input design variables

Number of capacitors / reference	C22	C33	C47
1	ΔV NOK ICrms NOK	ΔV NOK ICrms NOK	ΔV NOK ICrms NOK
2	ΔV NOK ICrms OK	ΔV NOK ICrms OK	ΔV OK ICrms NOK
3	ΔV NOK ICrms OK	ΔV OK ICrms OK	ΔV OK ICrms NOK
4	ΔV OK ICrms OK	ΔV OK ICrms OK	ΔV OK ICrms OK



(a)

(b)

Figure *2*: Illustration of sizing (a) and optimization (b) models

The degree of freedom is higher in the case of direct (optimization) model.

C. Guidelines and recommendations toward models for gradient-based optimization algorithms

In the aim to use gradient-based optimization approach for the pre-sizing of a power electronic system, the definition of the model used for 1st order optimization method is as follow:

(1) The model should be made regarding the application despite the loss of the possibility to create a library of "generic" optimization models. Indeed, a "generic" model requires being adapted for all possible situations (for example MOSFET model). But, it is hard to predict all these cases. Second, it would conduct to an increase of the model size while in optimization the designers try to minimize the computation time.

(2) A model should be made accordingly to the context: an optimization model has to be different from a characterization model whose purpose is to check later the health of the system or its behavior when integrating with other devices. Again, an optimization model requires low computation time and for the pre-sizing of optimization, a large degree of freedom.

(3) This latter point conducts to say that the optimization model should be direct.

(4) First, fineness and accuracy should not be mistaken (Figure *3*). It is not because the model is fine that it is also accurate. Indeed, when the model fineness is so high that it requires the use of unknown parameters, the accuracy of the model drops. A trade-off must be found. Based on the required model accuracy according to the application and the system sensitivity to some design parameters [2], the required fineness becomes obvious. But designers should always try to minimize computation time…

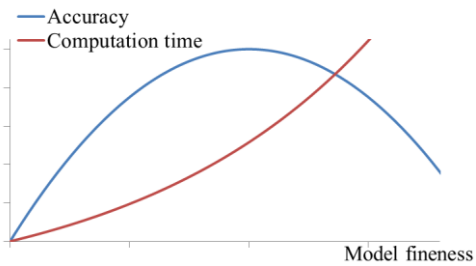


Figure *3*: Accuracy and fineness

(5) The nature of the model depends on the model's subject and its time and cost development. For optimization, analytical models are generally preferred.

III. Modeling Strategies for 1st Order Optimization on Power Electronics Systems

A. Model requirements regarding SQP algorithm

As stated in Chapter 2, the gradient-based optimization algorithm needs to be continuous and differentiable with an exact evaluation of the gradient. CADES software [3] is able to compute the exact Jacobian matrix of analytical and algorithmic models if the following rules are respected:

- The model describes a physical phenomenon that is naturally differentiable
- The model does not contain non-differentiable functions or discontinuous algorithmic conditions as floor, ceil, switch case, etc.

B. Modeling power electronics parts in the continuous world

As defined in the Chapter 2, there are two big families of discrete design variables in power electronics: the chopped ones (physically continuous but industrially discretized) and the distinct ones (naturally discrete like topology or technology choices).

It is quite simple to make a continuous model for the first category: because they are physically continuous, a direct empiric (experiments or datasheet interpolations) or direct theoretical analytical models are quickly set.

On the contrary, it is a difficult task to create a continuous model of a distinct variable, but it is not impossible. Trouble is there are no particular methods: the designers have to find some tips [4], [5] to limit as much as possible the number of distinct variables. Latter in this thesis, it will be shown that to make the IBC number of phases a continuous design variable, a part of the converter has been designed in the frequency domain instead of the usual time domain.

IV. IDENTIFICATION BY OPTIMIZATION OF SOME MODEL PARAMETERS

If gradient based optimization algorithm compels the designers to create continuous differentiable models, it in contrary helps them in the setting of empirical models. Indeed these models, in which the parameters values are defined thanks to experimental tests, require mathematical tools to be set. Optimization algorithm can be used to determine the good mathematical model parameters that fit to experimental data by minimizing the error between the model and the experimental data. The condition is again that the model is continuous and differentiable.

For example, in the fluid mechanics field (so helpful in power electronics systems), one of the problematic is to define the heat exchange coefficients between a heat source (semiconductor junction) and a cold source (cooling fluid). As the Nusselt number which represents the heat transfer between a fluidic and a boundary. This dimensionless number depends on: the thermos-physical properties of the fluid, the canal geometry and the flow regime. This Nusselt number is defined by (Eq. *6*).

$$Nu_{exp} = \frac{convective\ heat\ transfer}{conductive\ heat\ transfer} = \frac{\varphi_{exp} \cdot Dh}{\lambda \cdot S \cdot \Delta T_{exp}} \qquad \text{Eq. } 6$$

With φ_{exp} the heat flux, Dh the hydraulic diameter of the canal, λ the fluid thermal conductivity, S the heat exchange surface and ΔT_{exp} the measured temperature difference between the heated wall and the bulk fluid.

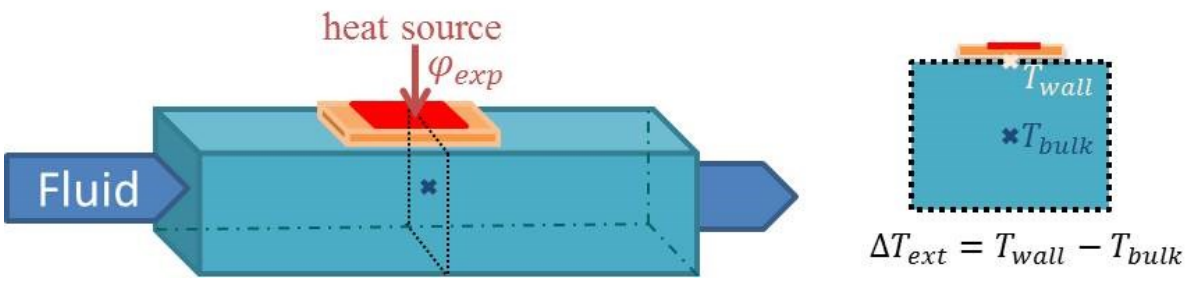


Figure *4*: Experiment setup to determine the Nusselt number of the canal associated to a specific fluid and flow rate

With this experiment, it is also possible to calculate the Reynolds number which is also a dimensionless quantity used to help predict flow patterns in different fluid flow situation (Eq. *7*).

$$Re = \frac{\rho \cdot Dh \cdot Q}{\mu} \qquad \text{Eq. } 7$$

With ρ the fluid volume density, Q the fluid flow rate and μ the fluid dynamic viscosity.

Thanks to these experiments, it is possible to define a mathematical formula that could predict the Nusselt number for the dedicated canal geometry used in other conditions (other fluid, other flow rate). For forced convection, the Nusselt number is generally a function of the Reynolds and Prandt numbers as define in (Eq. *8*).

$$Nu_{predict} = C \cdot Re^{m} \cdot Pr^{\alpha} \qquad \text{Eq. } 8$$

With C a constant to determine, Re the Reynolds number (dimensionless quantity used to help predict flow patterns in different fluid flow situation), m a coefficient to determine, Pr the Prandt number and α the fluid coefficient (0.33 for water).

The optimization algorithm can help into defining the model unknown coefficient *m* and constant *C* that minimize the quadratic error between the experimental results and the predictive results (Figure *5*).

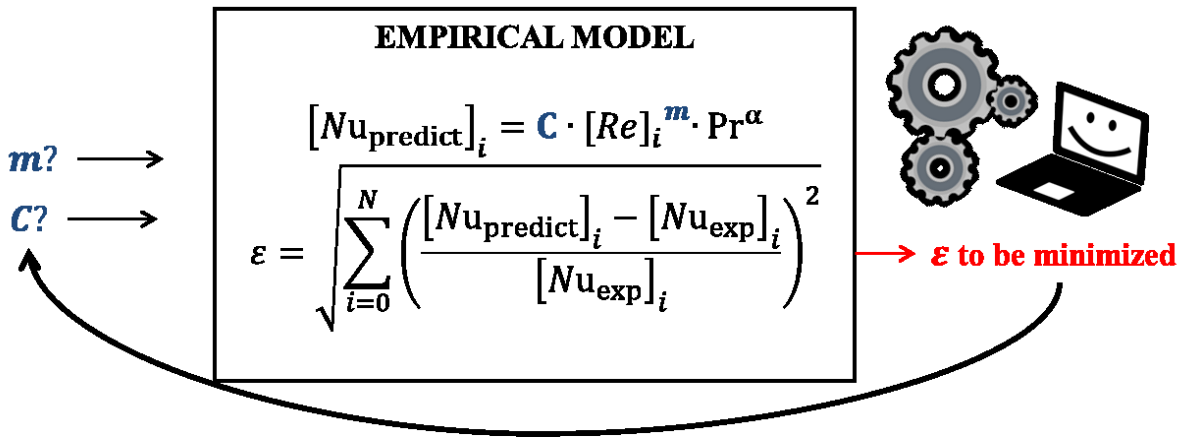


Figure *5*: Identification by optimization of model parameters

Once the fluid mechanical engineer has a model to predict the heat transfer in the duct, he can optimize the thermal-hydraulic behavior of a static power converter. Or even better, the engineer team can make a global optimization of the converter coupling the power electronics and mechanical fluidic physics: that is the great power of using differentiable analytical models for the optimization.

In the preliminary design phases of power electronics systems, this method is also particularly grateful to quickly determine the unknown parameters. For example, determining the parasitic elements of the switching losses test circuit based on semiconductors manufacturer data or determining a material thermal conductivity based on thermal experiments.

V. SETTING OF THE INTERLEAVED BUCK CONVERTER MODEL

A. Proposed problem formulation for the optimization of a converter

Unlike a "classical" indirect sizing model, the optimization model of a converter will not start from the desired performances and a directly computation of the associated functional voltage and current waveforms, but from the components parameters (electrical values, thermal data, etc.) evaluation (Figure *6*).

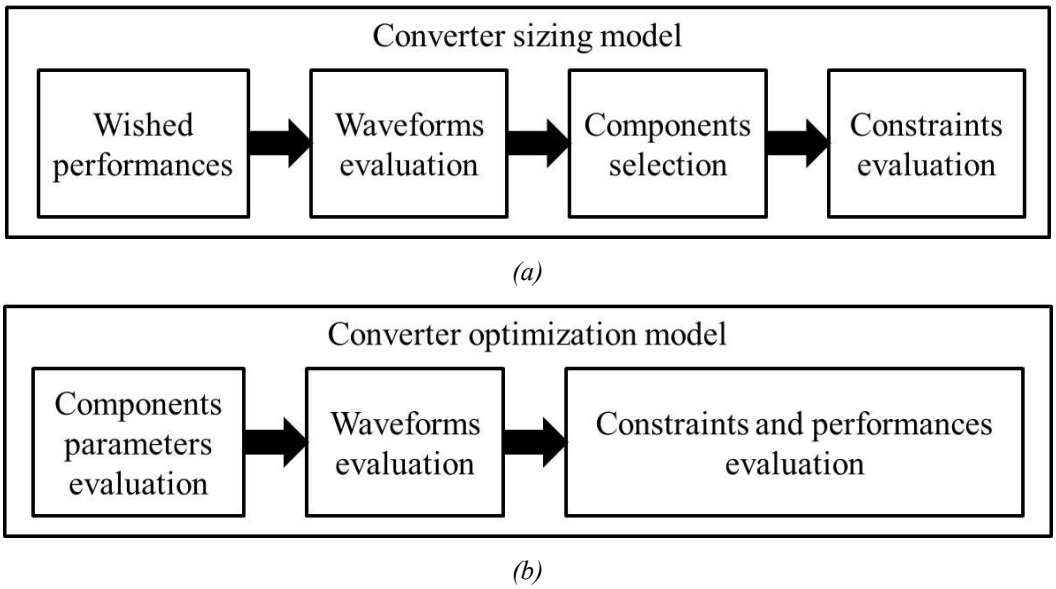


Figure *6*: Converter sizing (a) and optimization (b) models

The direct optimization model is again closer from the physic of the system. Indeed, when the user runs the converter, the components are already selected and assembled together: the converter will give some current and voltage waveforms depending on the source and the load properties. While the converter is running, the components submitted to these waveforms will create some losses thus generating heat (when they do not break). In other words, the converter components are constrained by electrical, thermal, etc. phenomena and the converter in its whole provides some performances (good or bad) as: ripples, EMI, efficiency, etc.

When using a 1st order optimization algorithm for pre-sizing a converter, it is recommended to make the converter model as in Figure *6*, (b), i.e. as it actually physically happens.

By using this natural direction for the converter optimization model, the designers will offer a large degree of freedom for the optimization algorithm and will limit the number of hypothesis that need to be taken.

B. Proposed problem formulation for the IBC of Stratobus project for one operating point

1) Proposed model of the IBC for one operating point

Figure 7 illustrates the global model of the IBC for one operating point. It follows the theoretical converter optimization model from Figure *6* (b). But it is of course dedicated to the Stratobus HVPCU DC-DC converter which the objective function is minimizing the electronics component weight.

The proposed formulation in Figure 7 was not the first one created for this application but is the result of several iterations between models creation, optimization results analysis and experimental tests. For example, the algorithm could not select itself the proper MOSFET and diode current rates when the number of phases was an optimization parameter. It appended that the converter weight get high by increasing the number of IBC phases to limit the current in the semiconductors in the final aim to fulfill the junction temperature constraint.

For the IBC topology, the main design variables are the number of phases, the switching frequency, the phase inductors value and the semiconductors choice. In the same spirit of [6]–[8] and in the contrary to the sequential design method [9], the filtering components are also taken as design variable. These global input design parameters appear in bold types and blue arrows on Figure 7.

The global input design parameters allow to select the components (whose models appear in green) and define their electrical, magnetic and thermal properties (blue arrows and police on Figure 7).

Then, based on the operating point data (black arrows on Figure 7), i.e. the input and output IBC voltages, input power and cooling plate temperature, the current and voltage waveforms inside these components are evaluated thanks to the blue boxes models. These waveforms are both analytically described in temporal or frequency domains (green arrows on Figure 7).

With these computed waveforms, it is then possible to evaluate both the IBC and components losses (purple arrows) and constraints (current THD and intrinsic temperatures in orange arrows) thanks to the models that appear in red on Figure 7.

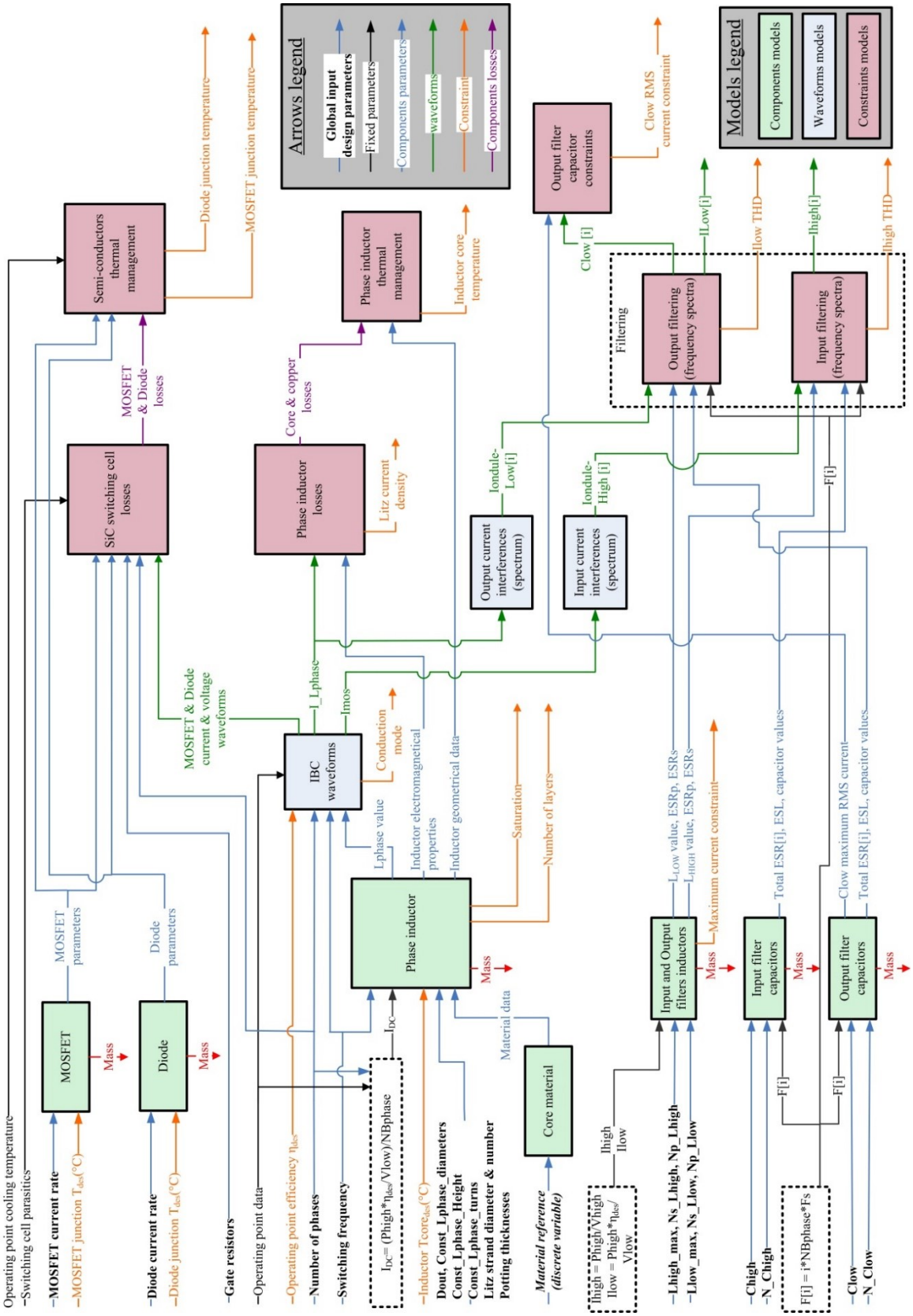


Figure 7: IBC optimization model for an only one operating point

2) Management of the implicit equations of the model

Of course the temperature dependency of the components behavior has been taken into account in this optimization model: it is so mandatory to give a temperature data to the components models as well as a "desired" IBC efficiency to the IBC waveforms model. These data are however computed with the constraints models. If these computed data are different from the given ones, it means that the operating point model with the chosen inputs could not exist in the reality. In the optimization's vocabulary, it is called "an implicit equation to solve". For example about the IBC operating point efficiency implicit equation to solve is Eq. *9*, with η_{des} the "desired" IBC efficiency and $\eta_{computed}$ the computed one.

$$\eta_{des} - \eta_{computed} = 0 \qquad Eq.\ 9$$

As demonstrated in [10] there are two ways to solve Eq. *9*. Or the designer uses a numerical method (like Newton-Raphson) or he uses the optimization algorithm thanks to the formulation of a new constraint: Eq. *10*, with η_{des} the constraint to fulfill and ε the chosen solution accuracy.

$$\eta_{constraint} = \left\|\eta_{des} - \eta_{computed}\right\| \leq \varepsilon \qquad Eq.\ 10$$

When using 1st or 2nd order optimization algorithm, it is advised to use the second way. Indeed these algorithms are able to handle up to 100 constraints, so adding a few ones is not really adding big difficulties to the optimization problem. Moreover, using numerical methods inside the optimization loop adds the risk of non-convergence or bad evaluation of the model's gradient. In addition, it can be problematic to express an implicit equation as Eq. *9* for the numerical method, given that this equation concerns a global variable in which several models are simultaneously involved.

Finally, for one operating point, the optimization algorithm has to find the proper design variables while fulfilling the constraints and solving the implicit equations Figure *8*.

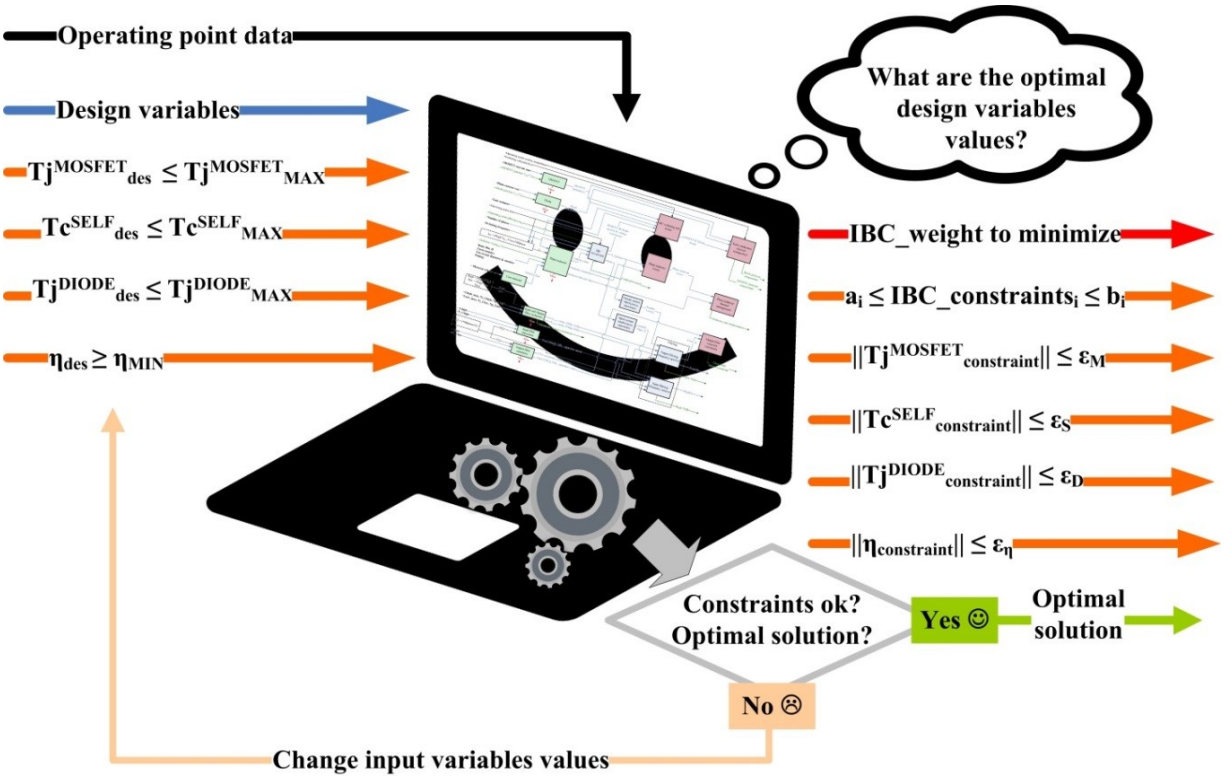


Figure *8*: Picture of the IBC optimization problem solving

VI. Conclusion

The coupling between a gradient-based optimization algorithm handling only continuous variables and a power electronics system made with an assembly of discrete electronics parts is non-natural. Despite this fact, there are some technics to properly formulate the power electronics optimization problem in the aim to use a 1st order optimization algorithm.

The next chapters of this thesis will focus on each models of Figure 7, in particular how in practice all discrete design variables of the IBC except the inductor material have been issued continuous.

Then it will be demonstrated that this approach and problem formulation allows a pre-sizing of the converter in its whole for several operating points simultaneously for the specification negotiation and prototyping phases.

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Chapter 5: Evaluation Models of the Components Parameters and Converter Waveforms of the Interleaved Buck Converter

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I. INTRODUCTION

As it has been described in chapter 4, the input design variables are not defined in the electrical world: for semiconductors, it is the current ratings, for inductors, they are constituted by core size, material, turn number, etc. Since the converter behavior is obviously based on its electrical parameters, there is a need of obtaining these ones. As we need continuous and differentiable models, the parameters have also to be continuous. We identify three kinds of discontinuities:

- A simple discretization of continuous parameter, due to industrial and economic reasons. For instance capacitor values depend on the dielectric surface and are intrinsically continuous, but are discretized into industrial series. In this case, coming back to the continuous variation of the parameters, or imaginary world, is not very difficult since the physic is continuous.
- Intrinsically discrete numerical variables as turn number, or number of IBC legs. The imaginary world with non-integer values of converter phases or levels will necessitate specific developments to propose continuous and differentiable models.
- Intrinsically discrete choice of a technology, as for instance SiC vs Si, or specific magnetic materials. In this case, there is no simple way to evolve continuously in the imaginary world from one choice to the other. We thus chose to perform several optimizations with fixed values of the relevant discrete variables.

This chapter will describe how to manage all these discontinuities (summarized in Table 1), for all components of the IBC (Figure *1*): semiconductors, inductors, capacitors and IBC electrical waveforms.

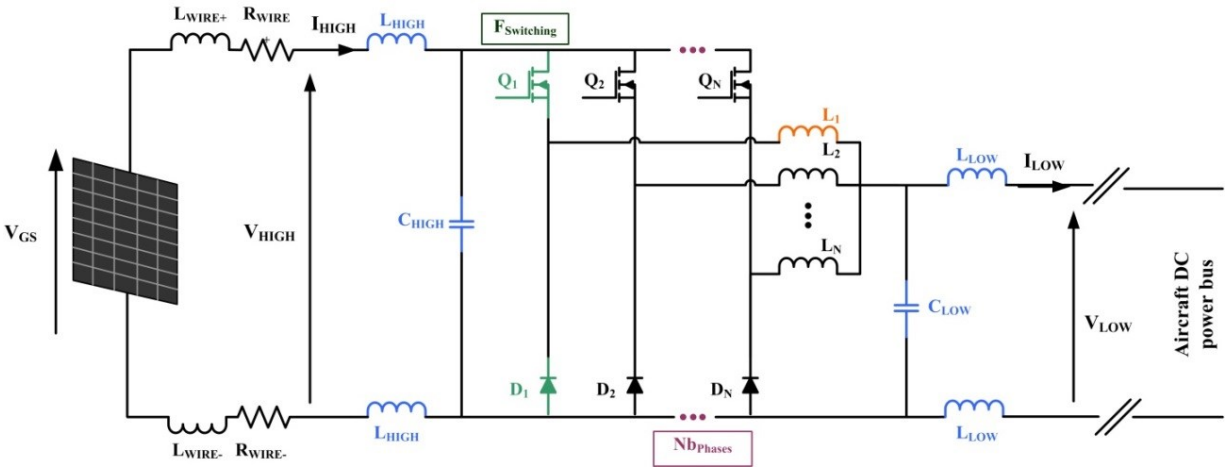


Figure *1*: IBC to optimize schematic

Table 1: IBC discrete variables of the technical proposals tree

Design discrete parameter	Abbreviation	Choices number	Design discrete parameter	Abbreviation	Choices number
Number of IBC Phase	$NBphase^{N}$	6	Input single capacitor value	$Chigh^{D}$	17
Conduction mode	CD^{T}	2	Output single capacitor value	$Clow^{D}$	46
Inductor core material	$Material^{T}$	3	Number of input capacitors in parallel	N_Chigh^{N}	15
Inductor core main permeabilities (14, 26, 40, 60, 125)	$Material^{D}$	5	Number of output capacitors in parallel	N_Clow^{N}	15
Toroidal inductor core size (choice number /material/µ)	$Dout^{D}$, Din^{D}, H^{D}	[4 - 36]	Input single filtering inductor value @ 0A	$Lhigh_max^{D}$	17
Litz strand diameter (AWG 33, 36, 38, 40, 42)	$DlitzLphase^{D}$	5	Output single filtering inductor value @ 0A	$Llow_max^{D}$	17
Litz number of strands	$nstrandLphase^{N}$	15	Number of input inductors in series	Ns_Lhigh^{N}	5
Phase inductor number of turns	$NturnsLphase^{N}$	~100	Number of output inductors in series	Ns_Llow^{N}	5
SiC 1200 V MOSFET current rating	Cal_Imos^{D}	5	Number of input inductors in parallel	Np_Lhigh^{N}	5
SiC 1200 V Schottky diode current rating	Cal_Idiode^{D}	10	Number of output inductors in parallel	Np_Llow^{N}	5

The variable abbreviation superscript letter "D" indicates if it is a discretized variable, "N" if it is a natural number discrete variable and "T" a technology or topology choice variables according to the method introduced vocabulary presented in Chapter 2.

After this step, the next chapter will present the models used to evaluate the converter performances and constraints on the components. These models will take advantage of the continuous parameters introduced here.

II. EVALUATING THE ELECTRICAL PARAMETERS OF THE COMPONENTS

A. Evaluating the Semiconductors parameters

In the study case of the IBC, as specified in chapter 3, 1200 V SiC N-MOSFET and Schottky diode have been pre-selected, therefore avoiding the issue of material discontinuity. The choice of the manufacturer (CREE) and casing (TO-247) have been made based on datasheet pre-analysis.

The semiconductors switching losses are sensitive to the following elements:

- the gate resistance R_G (influences the switching speed),
- the MOSFET (C_{GD}, C_{GS} and C_{DS}), diode (C_D) and phase inductor (C_L) parasitic capacitances (influence the switching speed and directly the losses),
- the MOSFET transfer characteristic (influences the switching speed and directly the losses),
- the devices switched currents and voltages (influence directly the losses),

- and the switching cell layout global inductances (L_D and L_S) (create the turn OFF MOSFET drain-source voltage overshoot and influence the switching speed).

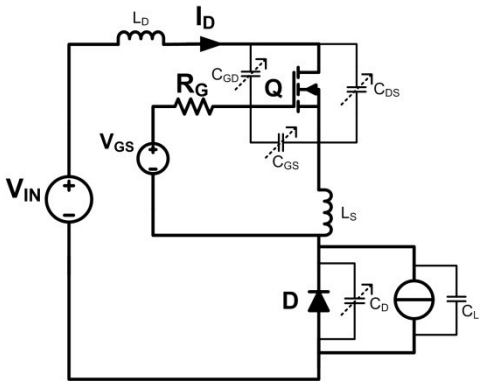
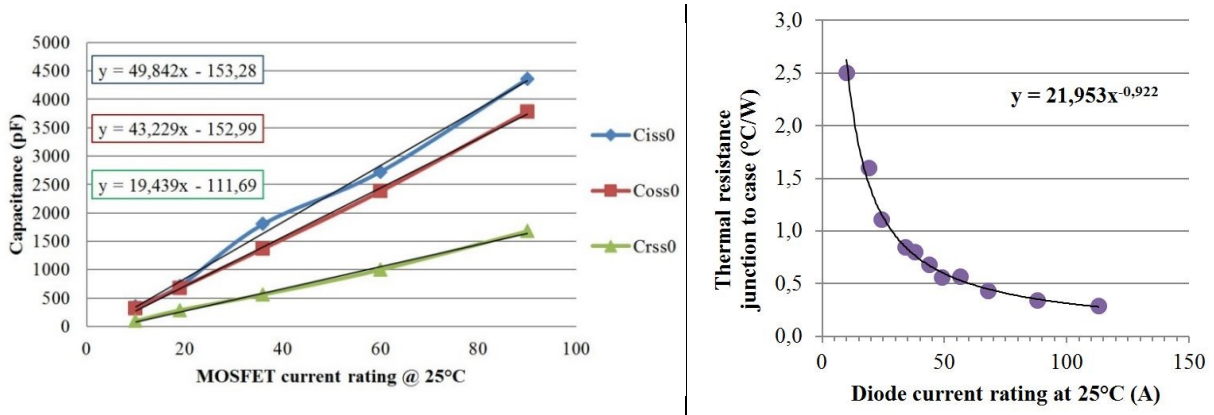


Figure 2: Switching cell under computation schematic

1) Semiconductors intrinsic parameters evaluation models

The number of phases of the IBC and the phase inductor evolve during the optimization, and so the average, RMS and peak current values in each IBC phase. To avoid a premature limitation of the optimization because of the semiconductors junction temperature or the IBC global efficiency, it is important to optimize the switching devices. But it is impossible to select discrete design variables (i.e. component reference) in database with gradient-based optimization algorithm. The previous listed parameters of the semiconductors and their thermal resistance junction to case are fortunately linked to the device chip area [1], and for some to the device junction temperature. The device current rating being the image of the chip area, it has been possible to interpolate the needed data of the semiconductors as functions of the devices current rating (Figure *3*), and junction temperature (Figure *4*).



(a) *(b)*

Figure *3*: Example of MOSFET and diode parameters depending on their current rating at 25°C

(a): MOSFET input (Ciss), output (Coss) and reverse transfer (Crss) capacitances under a low value of drain-source MOSFET voltage, (b): Diode thermal resistance

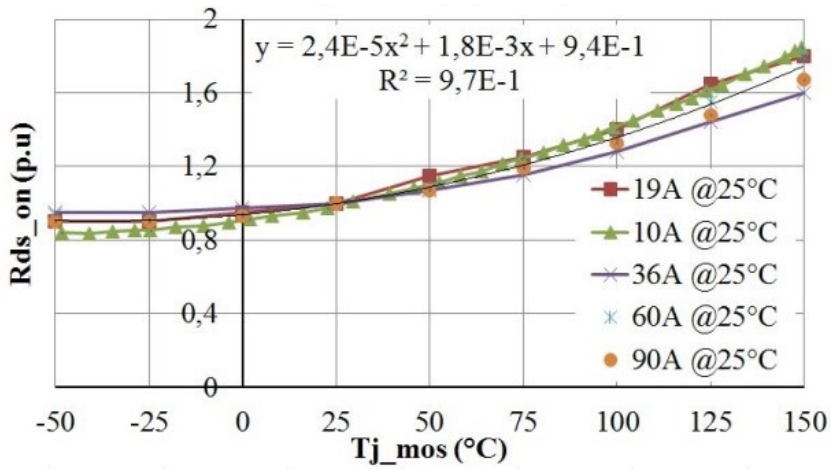


Figure *4*: MOSFET on state-resistance depending on both the current rating and the junction temperature

For these models, the current rating is so the continuous input design variables. The needed parameters for the losses and thermal models are the continuous output variables (the equations are detailed in the appendix of this chapter). As parameters are temperature dependent, there is a need of junction temperature variable as input. The dependence of MOSFET losses with temperature leads to an implicit equation, as detailed in chapter 4.

2) Switching cell circuit parameters evaluation model

a) Switching cell parasitic elements of the circuit evaluation

Modern devices as SiC exhibit so large commutation speed that the parasitic elements of the switching cell (Ls, Ld and C_L in Figure 2) cannot be simply neglected ([2], [3]). Unfortunately during the pre-design phase, the layout is not yet set and so Ls and Ld are unknown. Besides, the power inductor electrical parameters model does not provide C_L.

Here are some classical propositions to define the values of Ls and Ld:

(1) The company owns a library of pre-designed and optimized layouts of basic functions as SiC TO-247 command.

(2) The designer measures or estimates the layout parasitic inductances of a breadboard.

(3) The designer takes some typical values.

Regarding the power inductor capacitance C_L, the difficulty is quite different: based on the geometrical description of the inductor, an analytical model for simple round wire as [4] can be used to estimate the capacitance. But for power inductor made of Litz wire, the model can be a labyrinthine system, and so not adapted to optimization. A solution to determine this capacitance could be making an empiric model based on different same technology inductors characterization, which is time consuming.

Finally in this pre-design, another method has been used to define together the parasitic values of C_L, Ls and Ld for the pre-design purpose. It is supposed that the switching cell layout and inductor design will be at least as good as the test circuit of manufacturer switching devices. An identification by optimization (method explained in chapter 4) of the test circuit parasitic elements thanks to the manufacturer datasheet has been used [5].

This identification has been made on the C2M0080120D [6] test circuit (Figure 6), i.e. on the CREE SiC transistor current rating middle scale.

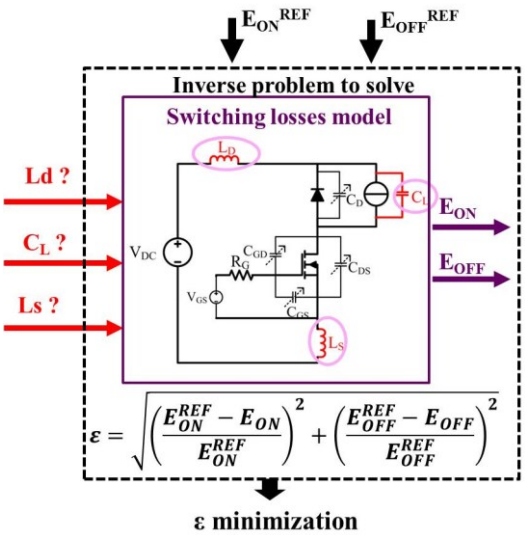


Figure 5: Identification of stray elements by optimization method

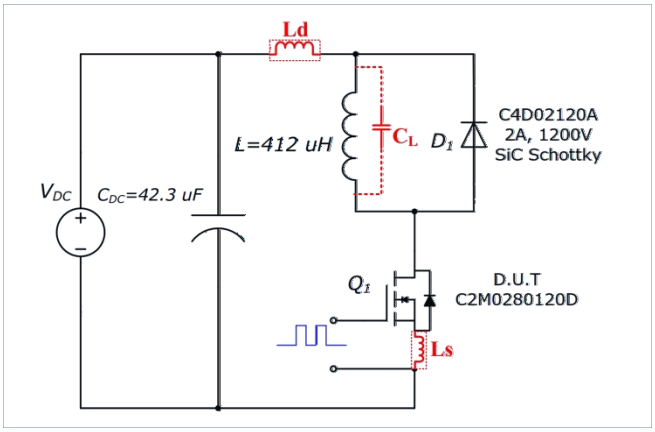


Figure 6: Clamped inductive switching waveform test circuit from [6]

Thanks to this identification by optimization method used on the switching losses model proposed in [3], the following parasitic elements have been identified for C2M0080120D test circuit: CL = 46.8 pF, Ls = 11 nH and Ld = 5 nH.

The curves of switching energies as function of switched current or gate external resistance obtained with the identified parasitic elements values and an analytical model are closed from the manufacturer measures (Figure 7).

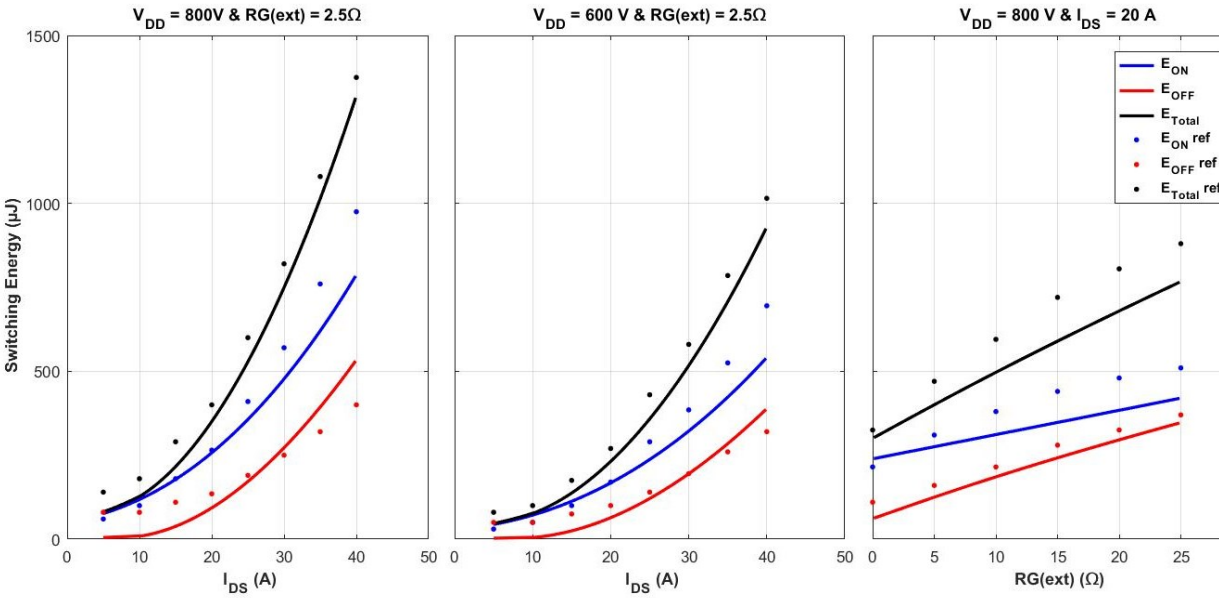


Figure 7: C2M0080120D switching energies evolvements: comparison between the estimation based on the analytical model with the identified parasitic elements (curves) and the manufacturer datasheet (points)

Because the switching cell devices placement on the printed circuit board should be different for the IBC from C2M0080120D test circuit (Figure 6), some extrapolations have been made. First the MOSFET source inductance Ls for the IBC should be equal to identified Ld from the manufacture test circuit since the MOSFET source should be close from the diode cathode. Then the total drain capacitance of the IBC circuit may be larger than the source inductance of manufacturer test circuit since the mechanical integration may be complicated in this stratospheric application: Ld = 20 nH.

Finally, the following values are taken: Ld = 20 nH,. CL = 46.8 pF and, Ls = 5 nH (Figure *8*).

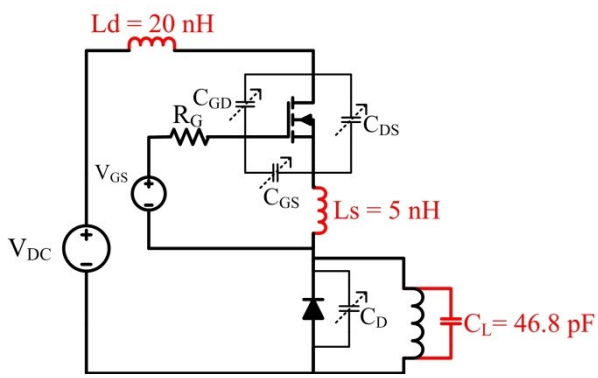


Figure *8*: Considered switching cell circuit of the IBC for the optimization model

b) Switching cell weight parameter evaluation

Because the number of phases impacts the number of semiconductors, drivers and the PCB needed surface, it is important to integrate the weight of the driver and the semiconductors in the components parameters models. All weights of semiconductors and drivers are independent of the current ratings. They have been measured and are constant.

3) Conclusion on the switching cell parameters evaluation model

Finally, Figure 9 presents the semiconductors parameters evaluation model requirements for the optimization problem formulation.

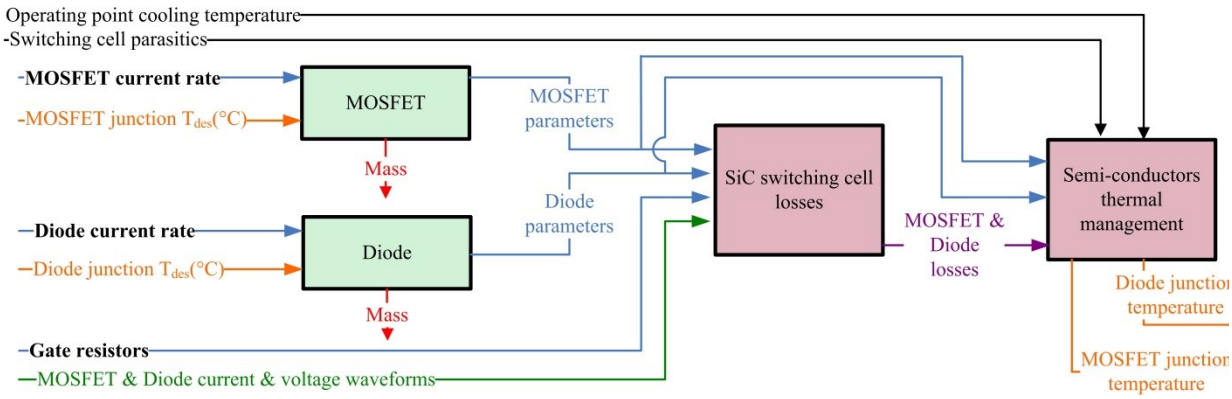


Figure *9*: Semiconductors models organization

B. Evaluating the filtering components parameters

As explained in chapter 3, the high frequency filtering capacitors and inductors have been chosen among commercial off the shelf (COTS) for simplicity reasons. The selection criteria were voltage and current ratings but also temperature operating range. It should be noticed that the inductor could also have been a custom design (in the aim to optimize the filter weight) but for industrial reasons COTS is preferred in this study case: a custom design will be made only if the COTS does not fulfill the requirements (as it will be the case for phase inductor in the next part).

The model of these filtering components should provide the total electrical data (inductances, resistances and capacitances global values). The weight and surface are also required for the global model. These parameters are so interpolated as function of the capacitor/inductor value (see Figure *10* as an example for capacitor).

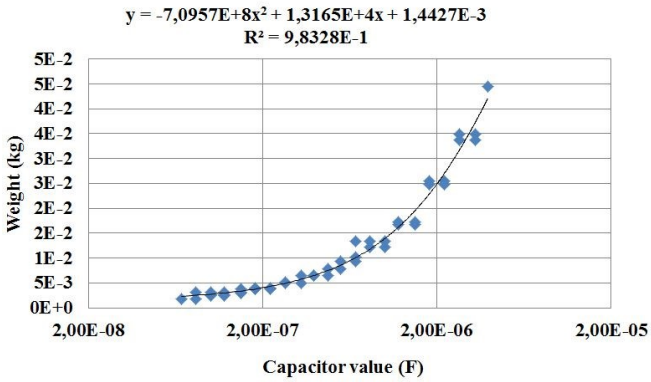


Figure *10*: Example of weight interpolation of capacitor

When there are several capacitor or inductor values for a same case (so same weight, volume and parasitic elements) in a series of them, it is advised to take only the one corresponding to the optimization problem objective function. In this case the capacitor presenting the better weight power density will be taken (Figure *11*).

VDC	VAC	Capacitance Value (µF)	Dimensions in mm			Lead Spacing (p)
			B	H	L	
1,000	250	0.47	11.0	22.0	41.5	37.5
1,000	250	0.56	13.0	24.0	41.5	37.5
1,000	250	0.68	13.0	24.0	41.5	37.5
1,000	250	0.82	16.0	28.5	41.5	37.5
1,000	250	1.0	16.0	28.5	41.5	37.5

Figure *11*: Example of capacitor selection in a manufacturer catalog

Also, when some electrical parameters as the parasitic inductance of the capacitor present some discontinuities as in Figure *12*, the designer can use the worst case technic. Here, the single capacitor esl value is fixed to 19 nH.

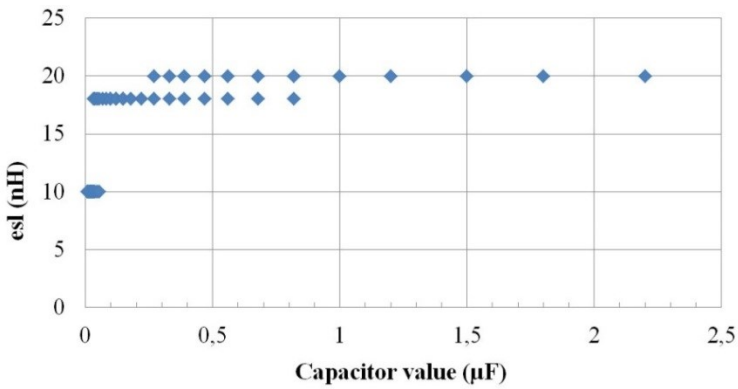


Figure *12*: Parasitic inductance value of the capacitors taken in the datasheet
(depends on the lead spacing, industrially discretized)

Of course, the number of components put in parallel and/or in series are also design variables.

There are some "fixed" input data to these models which depend on the operating point under study such as the input and output lines DC current values.

Figure *13* presents the schematic of the filtering components parameters evaluation models. Note that depending on the technology choice, the constraints can be different from a model to another. For example, the maximum admissible RMS current in the ceramic capacitors is nearly never given contrary to for film capacitors. Then, the film capacitors selection model should give the maximum RMS current of the selected one.

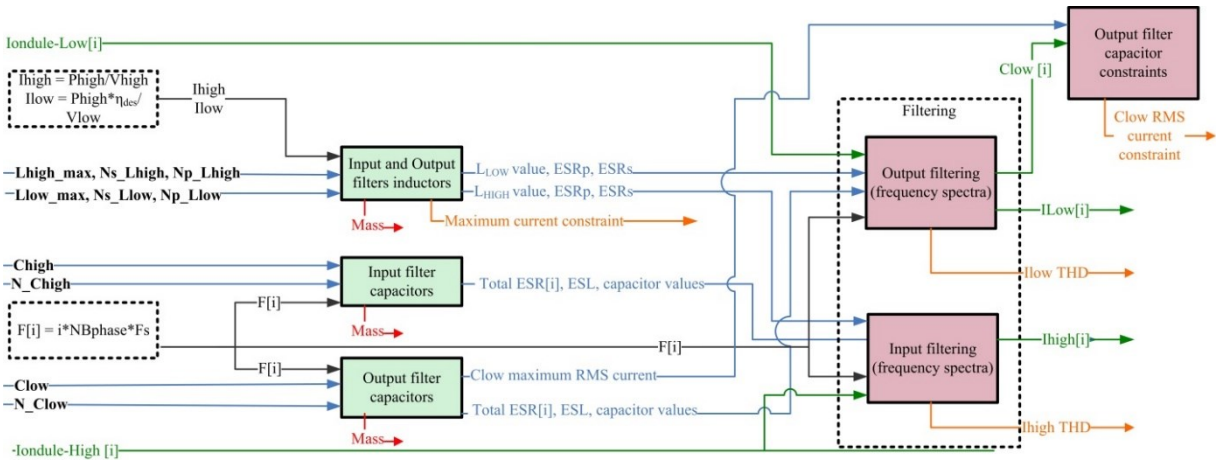


Figure *13*: Filtering components models organization

C. *Modeling the phase inductor parameters*

Because the inductors are a main part of the IBC weight, it has been decided to make a custom design made with several commercial off the shelf parts: externally uncoated Litz wire and inductor iron powder core both molded with a resin for thermal and dielectrical reasons (Figure *14*).

(a) (b) (c)

Figure *14*: IBC power inductor technology (a) Inductor without resin, (b) molded inductor, and (c) cross-section showing the inside of the molded inductor

For this customized electronic component, its electrical parameters (inductor value, parasitic capacitance and resistances) can be evaluated thanks to the technology description, i.e. with the equations describing the physics. This leads to the following input design parameters: the core material data, the geometrical data of the core and the winding characteristics.

1) Inductor core material

Except for the inductor core material which chemical elements choice is a technologically discrete variable, all of the inductor parts are discretized variables, included the inductor core permeability (the permeability

depends on the chemical elements mass concentration). These discretized variables can be transformed into continuous variables thanks to interpolation. But since the accuracy of iron powder core material permeability is already poor (for example, the manufacturer gives a ±8% of certainty for the nominal core inductance), the inductor core permeability for a given material will stay a discrete variable. For such influent variable on the IBC weight, adding again uncertainties is indeed dangerous.

2) Inductor geometries

The inductor turn number and the Litz number of strands are numerically discrete variables. Hopefully, there is not so much difference between 135 strands Litz wire and 136 strands Litz wire properties, and a continuous variation between two integers (e.g. 135.5) is still physically sound. On the contrary, the toroidal core dimensions are discretized variables since the discretization of the magnetic core is due to economic and manufacturing considerations. The situation is similar for the Litz strand diameter. These design variables will therefore be considered as continuous.

Based on the magnetic core manufacturer datasheet [7], the dimensions are quite homothetic (Figure *15*). The coefficients σ_{in} and σ_H defined with (Eq. 1) and (Eq. 2) are bordered between two value, respectively [0.4 0.7] and [0.75 1.0], for manufacturing reasons.

$$\sigma_{in} = \frac{Din}{Dout} \qquad 0.4 < \sigma_{in} < 0.7 \qquad \textit{Eq. 1}$$

$$\sigma_H = \frac{Dout - Din}{H} \qquad 0.75 < \sigma_H < 1.0 \qquad \textit{Eq. 2}$$

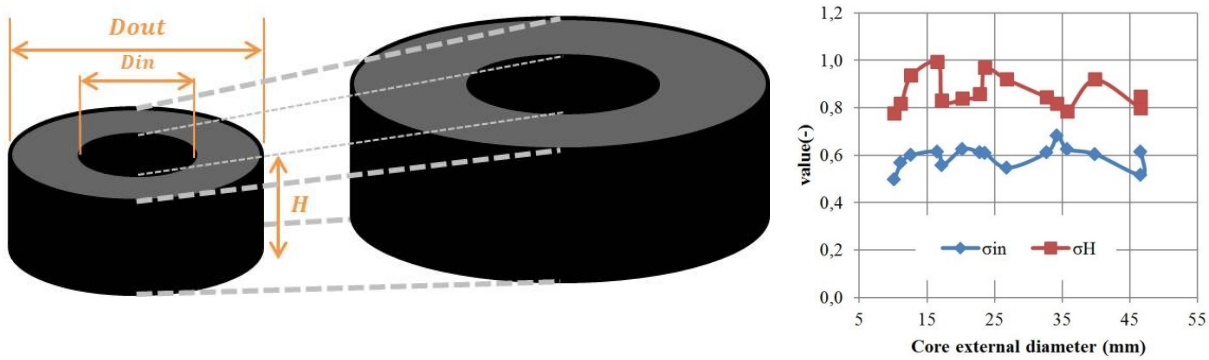


Figure *15*: Core dimension coefficients value from the manufacturer catalog

Based on this observation, there are two ways to stay in the limits of the manufacturer. Either the internal diameter, the external diameter and the height are input design variables and coefficients σ_{in} and σ_H are output constraint variables. Or the external diameter and these coefficients are defined as input design variables bordered between two values: the internal diameter and the height are so free output design variables. The

second solution is preferred in optimization because it allows limiting the number of constraints without limiting the degrees of freedom.

It should be noticed that it has been decided to impose such constraints to obtain cores compatible with manufacturing constraints. Obviously, removing those constraints is easy, if we want to increase the space of solutions.

Another technological constraint has been considered: since the switching frequency is supposed to reach high values, it is not possible to use too capacitive inductors. Therefore, it is wise to limit the winding layers to one and again an input variable σ_{turns} has been defined (Eq. 3).

$$\sigma_{turns} = \frac{Inductor\ number\ of\ turns}{Inductor\ maximal\ number\ of\ turns} \qquad 0.9 < \sigma_{turns} < 1.0 \qquad Eq.\ 3$$

3) Inductor electrical parameters evaluation

Finally, a simple reluctant model of the inductor is used to determine its inductance (in appendix of this chapter). This model takes into account the permeability drop of the magnetic material as function of the frequency, DC bias and temperature. Since these material properties cannot be guaranteed by manufacturers, the permeability drop has been limited to 20% for the robustness of the design.

The current density in the conductors, as well as the operating flux density in the core should in theory not be limited except by the estimated temperature of the inductor (see thermal model on the inductor, chapter 7). But due to a technical choice on the inductor connection terminals that has been made in the early steps of the design, the current density in the inductor wiring is limited to a very low value by the spatial wiring standards [8] combined with integrator derating rules. Consequently, with a core density of 5 A/mm², copper losses are very low in this design. Further work may relax this constraint to evaluate how much the optimal design would be affected by this early choice.

Since copper losses will be low, it is not necessary to put too many efforts in the modelling. Therefore, "hard computation" models (like [9] in this case) are not very useful. The AC resistance of the Litz wire is determined with simple formula from a Litz wire manufacturer [10],(Eq. *4* ; Eq. *5* ; Eq. *6*).

$$RdcLitz = \frac{Litz_{lenght} * Rs * 1.015^{Nbunching} * 1.025^{Ncabling}}{Nb_{strand}} \qquad \text{Eq. } 4$$

With RdcLitz the DC resistance of the Litz wire, $Litz_{lenght}$ the total length of the Litz wire, Nbunching the number of bunching operations (2 is taken for the optimization), Ncabling the number of cabling operations (2 is taken for the optimization) and Nb_{strand} the number of strands of the Litz wire.

$$Gac = \left(Dlitz * \frac{\sqrt{Fs}}{10.44}\right)^4 \qquad \text{Eq. } 5$$

With Gac, the Eddy-current basis factor, Dlitz the strand diameter (in inch unit) and Fs the operating frequency in Hz.

$$RacLitz = RdcLitz * \left(Sac + Kac * Gac\left(Nb_{strand} * \frac{Dlitz}{Dlitz_{ext}}\right)^2\right) \qquad \text{Eq. } 6$$

With RacLitz the AC resistance of the Litz wire, Sac the resistance ration of individual strands when isolated (1 is taken for the optimization), Kac a constant depending on the number of strands (2 is taken for the optimization), and $Dlitz_{ext}$ the external diameter of the Litz wire.

The number of layers is limited to one, thus the inductor capacitance is supposed to be negligible and is not evaluated.

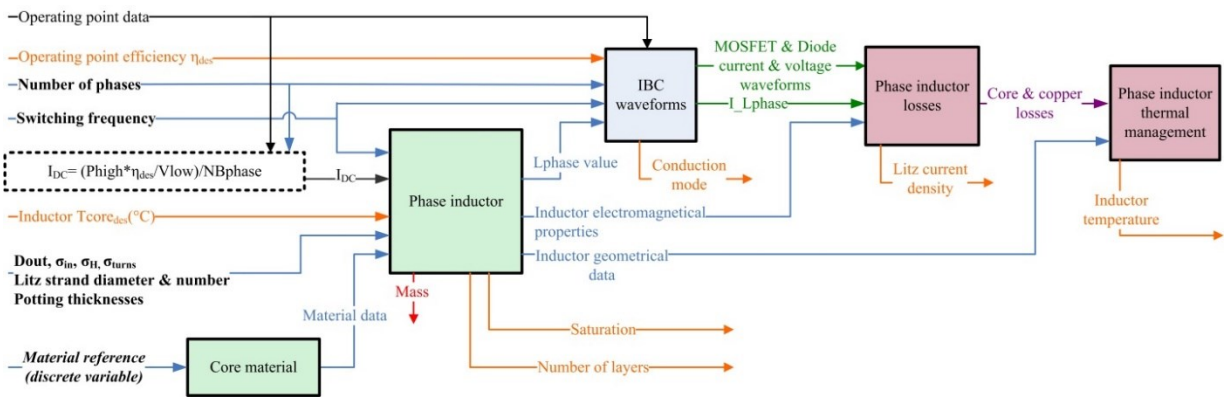


Figure *16*: IBC phase inductor models organization

III. CONVERTER CURRENT AND VOLTAGE WAVEFORMS MODELS

Once the electrical values are known, it is possible with the operating point information to determine the functional waveforms of the Interleaved Buck Converter and then to compute the input and output current disturbances (i.e. their frequency spectra) which have to be filtered.

A. IBC power functional waveforms model

Determining the current and voltage waveforms (are shown in Figure *17*) in the IBC components is necessary to figure out the external and internal converter constraints (components temperature, efficiency, THD, etc.).

1) Conduction mode determination

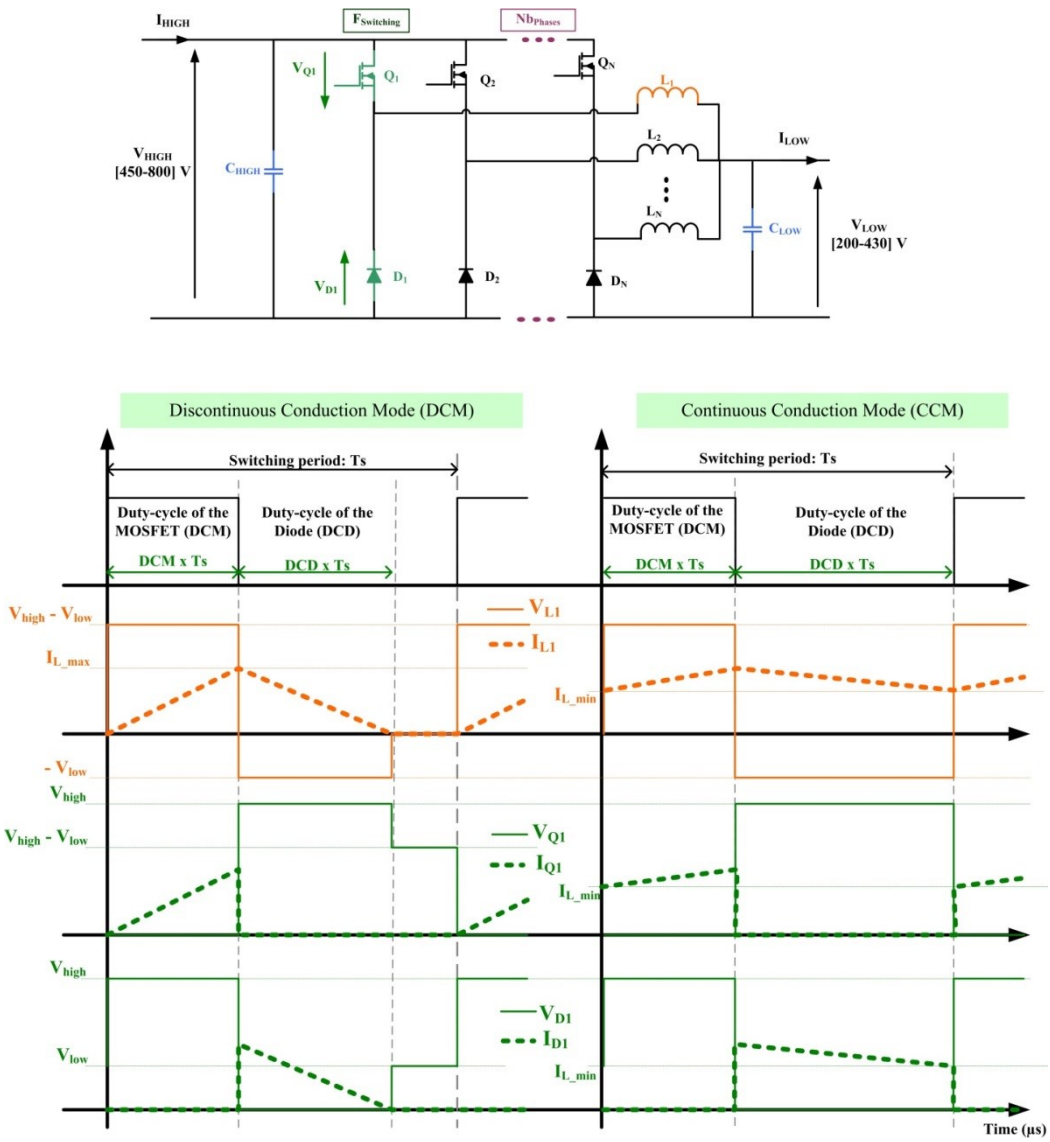


Figure *17*: Single phase Buck converter waveforms

For the optimization model, the first variable to be evaluated is the critical phase inductor value (Lcrit) that would conduct the converter to be on the limit of continuous and discontinuous conduction (Eq. *7*).

$$Lcrit = \frac{(Vhigh - Vlow) * \frac{Vlow}{Vigh} * Ts}{2 * \frac{Ilow}{Nphase}} \qquad Eq.\ 7$$

With Vhigh and Ihigh the converter input voltage and current, Vlow and Ilow the output converter voltage and current, Ts the switching period and Nphase the IBC number of phases.

This Lcrit variable can be compared with the designed inductor value (Lphase). **If** Lphase is higher than Lcrit, then the converter is running in continuous conduction mode (DC = 0), and **if** it is the opposite, the converter is running is discontinuous conduction mode (DC = 1). Thanks to this knowledge, the semiconductors duty-cycles can be computed (the equations are detailed in appendix).

It should be noticed that this model needs the use of the algorithmic condition “if”. This algorithmic condition is not differentiable. Because all output variables stay continuous and differentiable by parts (Figure *18*) it is however permitted to use this condition “if”. Only the output variable named “CD” representing the conduction mode state of the converter is not continuous derivable. Therefore, it is prohibited to constraint the conduction mode with this “CD” variable.

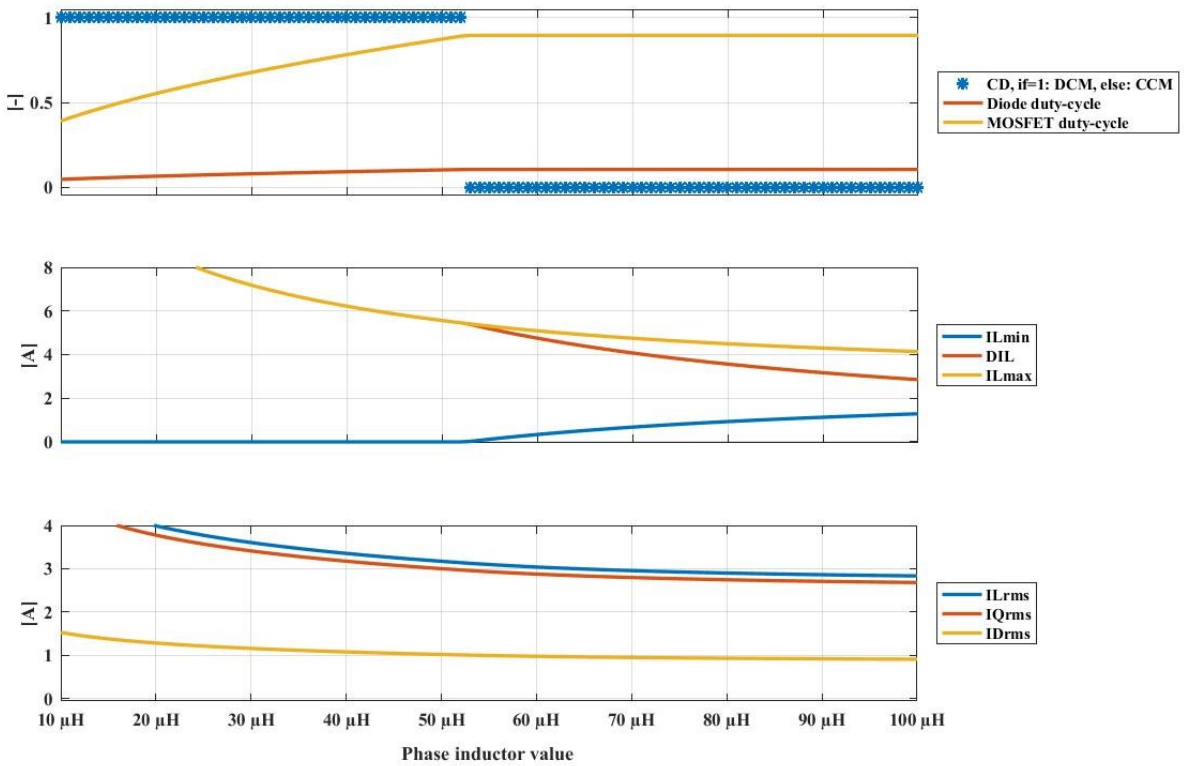


Figure *18*: Impact of condition “if” and conduction mode on IBC waveforms model outputs as a function of the phase inductor value

A new variable named “cont_conduction” is created for this purpose (Eq. 8) which is perfectly continuous and differentiable (Figure *19*). It is simply the difference between the inductor value and Lcrit. If "cont_conduction" is positive, the conduction mode will be continuous, if it is negative, the conduction mode will be discontinuous.

$$cont\ conduction = Lphase - Lcrit \qquad Eq.\ 8$$

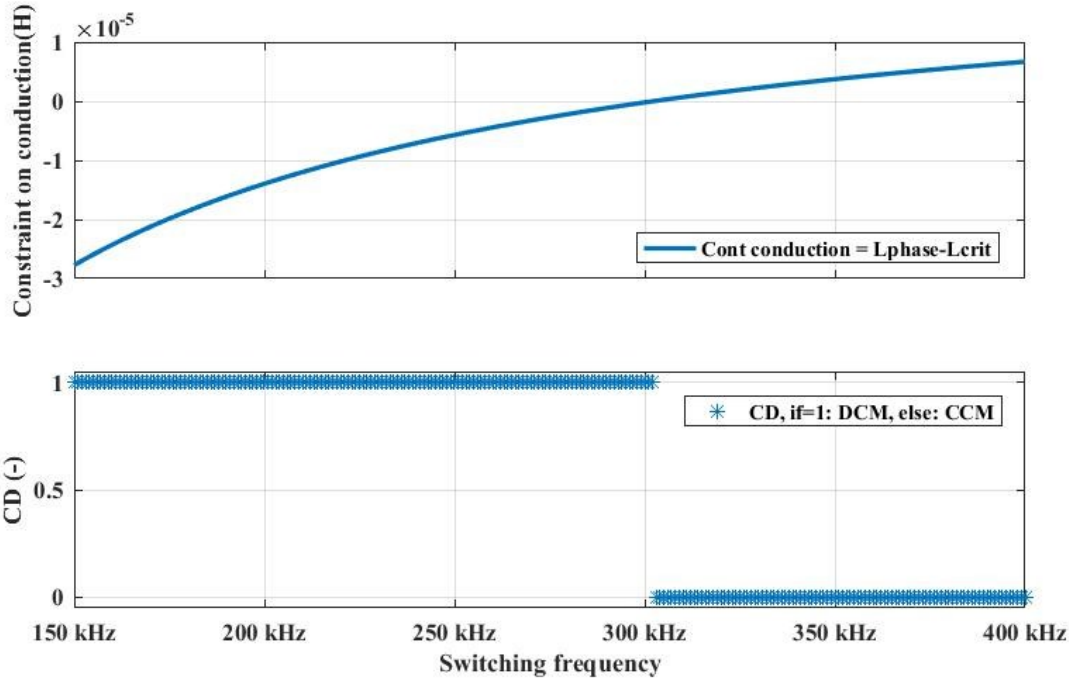


Figure *19*: Conduction mode constraint as a function of the switching frequency

2) Current and voltage values in the power components

Once the conduction mode is determined, it is possible to define the current and voltage values across the power components during each phase of the switching period (Ts). There are two phases in continuous conduction mode, i.e. when the MOSFET is in ON state ($t \in [0; DCM \cdot Ts]$ with DCM the MOSFET duty-cycle) and when it is in OFF state ($t \in [DCM \cdot Ts\,; Ts]$). There are three phases for the discontinuous conduction mode, i.e. when the MOSFET is in ON state ($t \in [0; DCM \cdot Ts]$), when the diode is in ON state ($t \in [DCM \cdot Ts\,; (DCM + DCD) \cdot Ts]$ with DCD the diode conduction duration) and when the MOSFET and the diode are in OFF state ($t \in [(DCM + DCD) \cdot Ts\,; Ts]$). Here the transients that appear during the semiconductors switches are not considered.

a) Considered voltage and current values in CCM

Table 2 gives the voltages and current values of the power devices during the two phases of the continuous conduction mode.

Table 2: Voltage and current values across power components in CCM

Component	$t \in [0; DCM \cdot Ts]$	$t \in [DCM \cdot Ts\,; Ts]$
MOSFET	$V_Q = 0\,V$	$V_Q = Vhigh$
	$I_Q(t) = ILmin + \frac{Vhigh - Vlow}{L_{phase}} \cdot t$	$I_Q = 0\,A$
diode	$V_D = Vhigh$	$V_D = 0\,V$
	$I_D = 0\,A$	$I_D(t) = ILmax + \frac{-Vlow}{L_{phase}} \cdot (t - DCM \cdot Ts)$
Phase inductor	$V_{DS} = Vhigh$	$V_L = -Vlow$
	$I_L(t) = ILmin + \frac{Vhigh - Vlow}{L_{phase}} \cdot t$	$I_L(t) = ILmax + \frac{-Vlow}{L_{phase}} \cdot (t - DCM \cdot Ts)$

With Vhigh, the converter input voltage, Vlow the converter output voltage, ILmin and ILmax respectively the minimal and maximal values of the current in the phase inductor, Lphase the phase inductor value

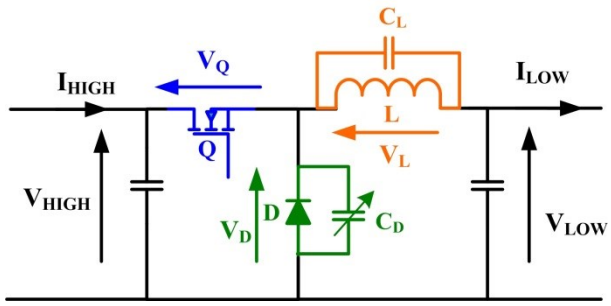
b) Considered current and voltage values in DCM

Table 3 gives the ideal voltages and current values of the power devices during the last phase of the discontinuous conduction mode. Indeed, the first phases ($t \in [0\,; DCM \cdot Ts]$ and $t \in [DCM \cdot Ts\,; (DCM + DCD) \cdot Ts]$) are similar to CCM.

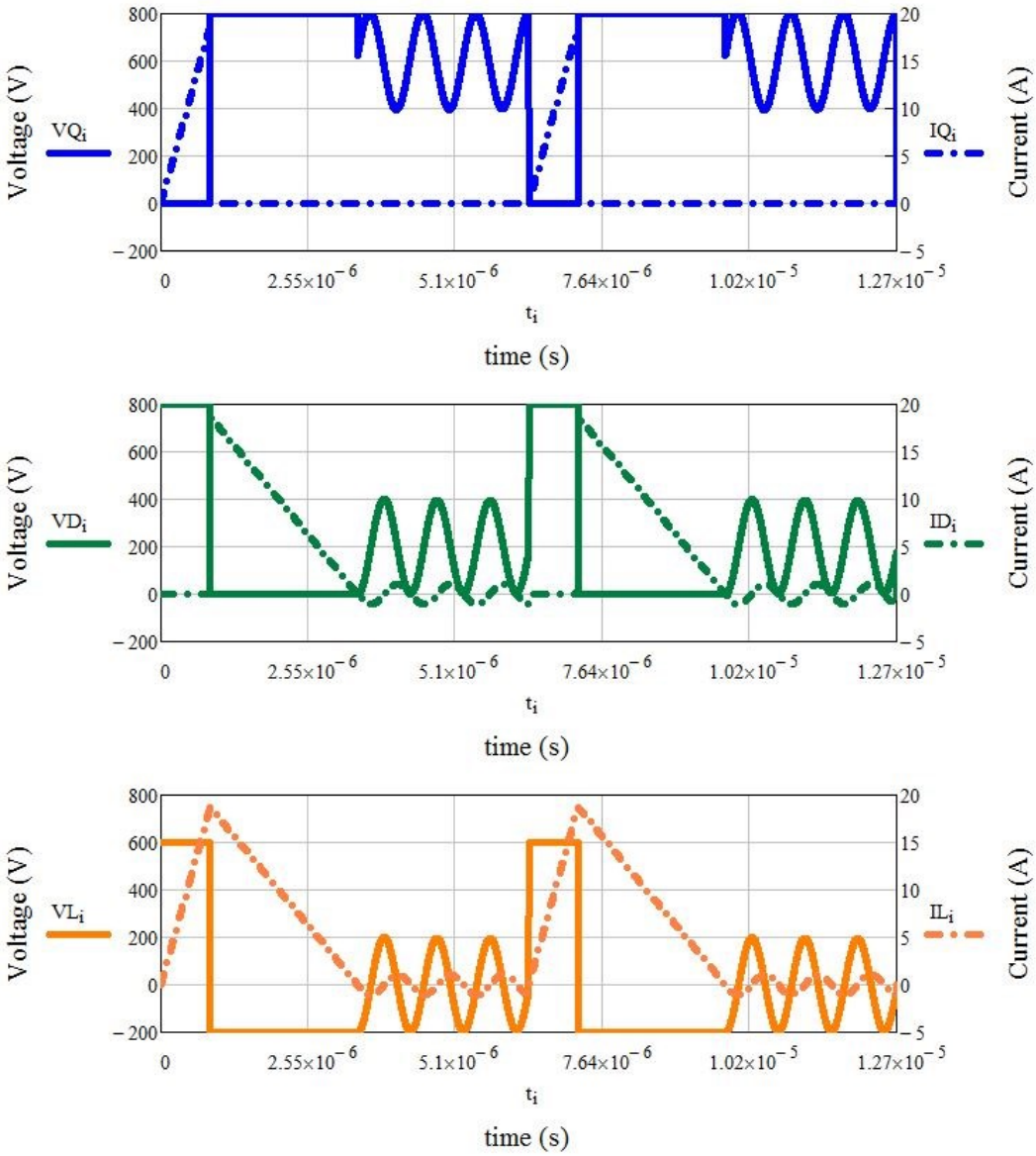
Table 3: Voltage and current values across power components in the last two phases of DCM

Component	$t \in [(DCM + DCD) \cdot Ts\,; Ts]$
MOSFET	$V_Q = Vhigh - Vlow$
	$I_Q = 0\,A$
diode	$V_D = Vlow$
	$I_D = 0\,A$
Phase inductor	$V_L = 0\,V$
	$I_L = 0\,A$

Unfortunately, the preliminary design is made in the imaginary world, i.e. with continuous variables, not in the ideal one. Indeed, an oscillation appears at $t \in [(DCM + DCD) \cdot Ts\,; Ts]$ (Figure *20*) in discontinuous conduction mode due to the parasitic elements of the switching cell that are: the diode non-linear capacitance, the inductor capacitance and to the phase inductor itself.



(a)



(b)

Figure *20*: Buck converter waveforms in DCM including the ringing due to the parasitic elements, (a) Buck schematic with the parasitic elements, (b) power devices waveforms

All equations of this phase are described and detailed in appendix. The period of this high frequency oscillations is linked to the parasitic capacitances and phase inductor value (Eq. 9).

$$T_{Oscill} = 2\pi\sqrt{(C_L + C_D) \cdot L_{phase}} \qquad Eq.\ 9$$

With C_L the phase inductor parasitic capacitance, C_D the diode parasitic capacitance (which depends on the reverse voltage of the diode: taking the value for 0 V well approximate the oscillations frequency) and L_{phase} the phase inductor value.

This period is very sensitive to these parasitic elements, themselves being not predictable with accuracy (for a same design the uncertainties due to the manufacturing are important: about 25% for phase inductor capacitance, 8% for the inductor value according to the magnetic core manufacturer). It would therefore be presumptuous to predict the voltage and current values across the power devices when the MOSFET is turned ON. Figure *21* shows the measured three MOSFETs drain-source voltage values during their turn ON of a 3-Phases IBC in DCM mode according to the input converter power (Phigh), compared with the ideal MOSFET turn ON switched voltage. Of course, the three phases were similar in their design (same diode and phase inductor).

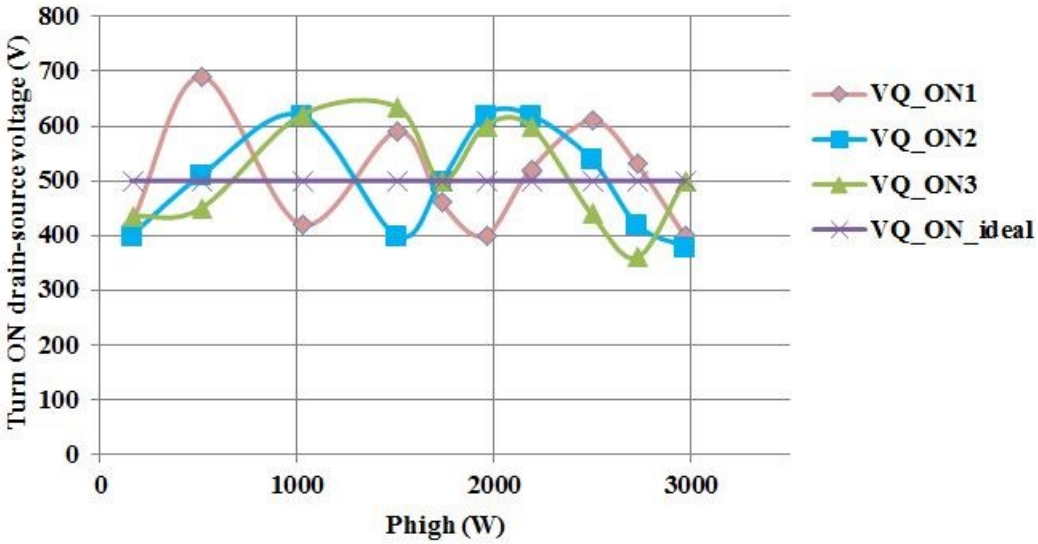


Figure *21*: Measured MOSFETs drain-source voltage values during their turn ON of a 3-Phases IBC in DCM mode

This large uncertainty is really unfortunate since this ringing effect modifies the converter efficiency when the operating point is changed (see the efficiency oscillations on Figure *22*).

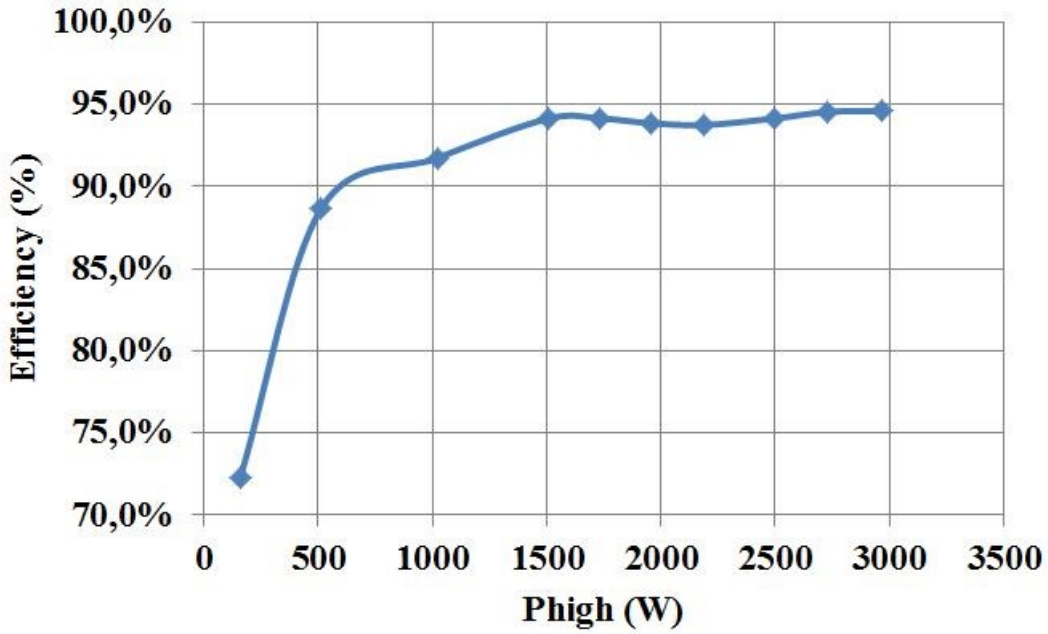


Figure *22*: Measured efficiency of a 3-Phases IBC in DCM mode

In other word, these oscillations in DCM are not negligible regarding the converter performances and so should be taken into account.

There are two possible strategies:

i. Make the pre-design in the worst case for all power components

ii. Make the pre-design in the middle case for all power components

The first proposal should guarantee the constraint for any case but would also conduct into a non-negligible oversizing of the converter. In contrary the second proposal should predict the mean value of the performances: hopefully this assumption about the converter global efficiency should be close to reality with a high number of phases of the IBC. There is a risk that the under-estimate losses in the semiconductors of an IBC phase conducts into a large error on junction temperature estimation. Since in this aero-spatial application, the margin on the semiconductors maximum temperature is quite large; the second proposal has so been selected for this application.

c) Conclusion

Finally Table 4 gives the switched voltages and current values of the semiconductors for both continuous and discontinuous conduction modes. These values will be used by the semiconductors losses models that are presented in the next chapter.

Table 4: switched voltages and current values of the semiconductors in both CCM and DCM

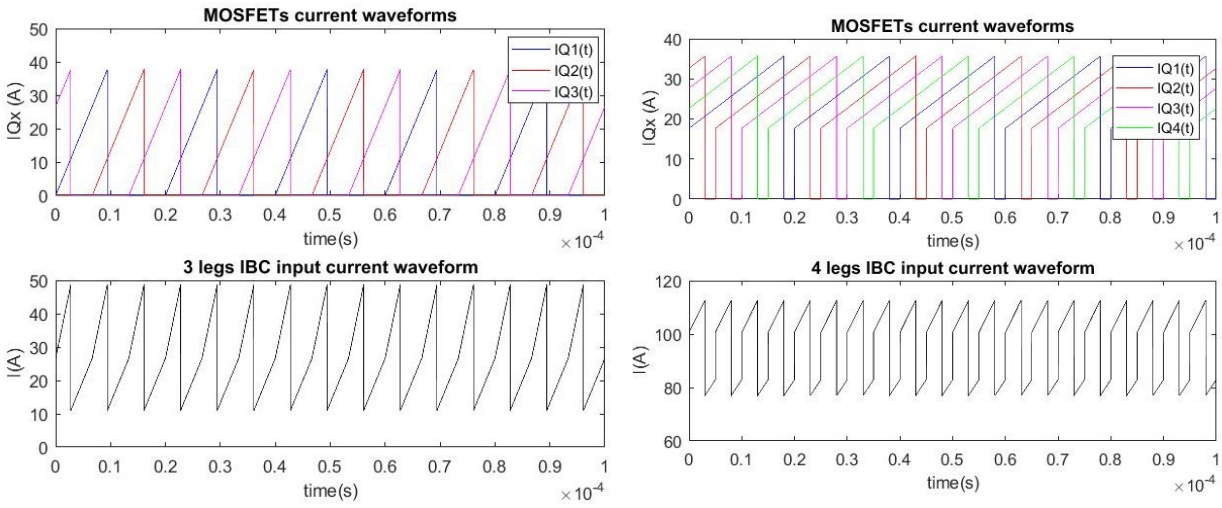
MOSFET	Turn ON	From $V_Q^{ON} = Vhigh - Vlow \cdot CD$ to $0\ V$	From $0\ A$ to $I_Q^{ON} = ILmin$
	Turn OFF	From $0\ V$ to $V_Q^{OFF} = Vhigh$	$From\ I_Q^{OFF} = ILmax$ to $0\ A$
diode	Turn ON	From $V_D^{ON} = Vhigh$ to $0\ V$	From $0\ A$ to $I_D^{ON} = ILmax$
	Turn OFF	From $0\ V$ to $V_D^{OFF} = Vhigh \cdot CD + (1 - CD) \cdot Vlow$	$From\ I_D^{OFF} = ILmin$ to $0\ A$

With CD the conduction mode variable (0 if CCM and 1 if DCM)

B. IBC input and output current disturbances model

1) IBC input current ripple before filtering

Getting an estimation of the input and output converter current ripples is challenging because it depends on the number of phases of the IBC [11]. Figure *23* is an illustration of the current ripple at the input of an Interleaved Buck Converter in two different cases. The number of phases of the converter has a non-negligible impact on its weight that is why it should stay a design parameter for the optimization and so a continuous design variable.



(a) (b)

Figure *23*: Interleaved Buck Converter MOSFETs and input current waveforms: (a) 3-phases IBC in DCM, (b) 4-phases IBC in CCM

(1) Analytical expression of current ripple

The proposed analytical model in the time domain in [11] that gives the IBC input and output current ripple value (ΔIhigh and ΔIlow) is nearly perfect for the optimization. But it unfortunately uses the mathematical

functions “floor” and “ceil” which are definitively not differentiable and so the gradient based optimization algorithm cannot be employed. We show in the following that it is possible to get the input and output current spectra with a continuous differentiable model of the IBC in the frequency domain.

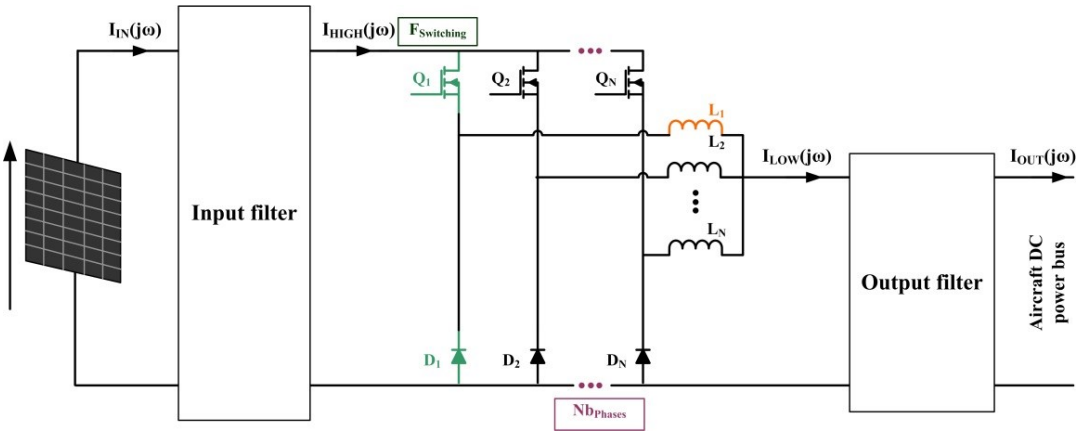


Figure *24*: IBC schematic to represent the computed spectra

On Figure *24*, the input current interferences is called $I_{HIGH}(j\omega)$ and the output current interferences is called $I_{LOW}(j\omega)$.

Figure *25* presents the current waveforms inside the MOSFETs of the IBC.

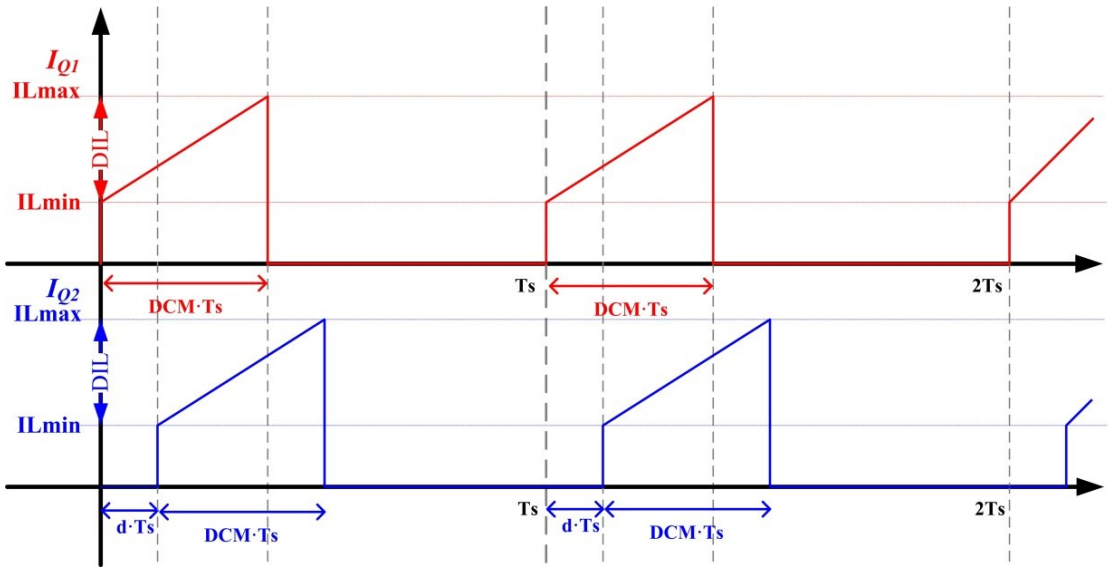


Figure *25*: IBC current waveforms in the MOSFETs

The command delay between each IBC phase is defined as *d* with *Nphase* the number of IBC phases (Eq. 10).

$$d = \frac{1}{Nphase} \qquad \textit{Eq. 10}$$

The Fourier series of the MOSFET drain current *IQ1(jω)* in the phase 1 of the IBC is defined by (Eq. 11).

$$IQ1(j\omega) = \frac{2}{T_s}\left\{(1 - e^{-j\omega DCM \cdot T_s})\left(\frac{ILmin}{j\omega} + \frac{DIL}{DCM \cdot T_s(j\omega)^2}\right) - \frac{DIL}{j\omega}e^{-j\omega DCM \cdot T_s}\right\} \qquad Eq.\ 11$$

With Ts the switching period, DCM the MOSFET duty cycle, DCD the diode conduction duration, ILmin the minimum value of phase inductor current and DIL the phase inductor ripple value.

So the Fourier series of the input current inside the second IBC phase MOSFET *IQ2(jω)* can be simply expressed with (Eq. 12) and finally, IBC input current Fourier serie $I_{HIGH}(j\omega)$ can be expressed as (Eq. 13).

$$IQ2(j\omega) = IQ1(j\omega) * e^{-j\omega * d * T_s} \qquad Eq.\ 12$$

$$I_{HIGH}(j\omega) = IQ1(j\omega) \sum_{n=0}^{Nphase-1} e^{-j\omega * n * d * T_s} \qquad Eq.\ 13$$

Since the harmonics exist in theory only on the multiples of the switching frequency *Fs* and *Nphase*, the harmonics will be looked at the pulsation ω_O (Eq. 14), which leads to (Eq. 15) that can be simplified by (Eq. 16).

$$\omega_O = 2\pi * \frac{Nphase}{Ts} \qquad Eq.\ 14$$

$$I_{HIGH}(j\omega_O) = IQ1(j\omega_O) \sum_{n=0}^{Nphase-1} e^{-n * j * 2\pi * \frac{Nphase}{Nphase} * \frac{T_s}{T_s}} \qquad Eq.\ 15$$

$$I_{HIGH}(j\omega_O) = IQ1(j\omega) * Nphase \qquad Eq.\ 16$$

The same approach has been used for the output current ripple, which leads to equations {Eq. 17 - Eq. 20}.

$$\alpha_1 = -\omega * DCM * Ts \qquad Eq.\ 17$$

$$\alpha_2 = -\omega * (DCM + DCD) * Ts \qquad Eq.\ 18$$

$$IL1(j\omega) = \frac{2}{T_s}\left\{\frac{j}{\omega}ILmin(1 - e^{-j\alpha_2}) - \frac{DIL(1 - e^{-j\alpha_1})}{DCM \cdot T_s(j\omega)^2} + \frac{DIL(e^{-j\alpha_1} - e^{-j\alpha_2})}{DCD \cdot T_s(j\omega)^2}\right\} \qquad Eq.\ 19$$

$$I_{LOW}(j\omega) = IL1(j\omega) * Nphase \qquad Eq.\ 20$$

(2) Validation thanks to the simulations

These analytical equations have been compared with the Fast Fourier Transform (FFT) of a time simulation under the same assumptions, i.e. each IBC phases are exactly similar and there are no parasitic elements in the switching cells (Figure *26*).

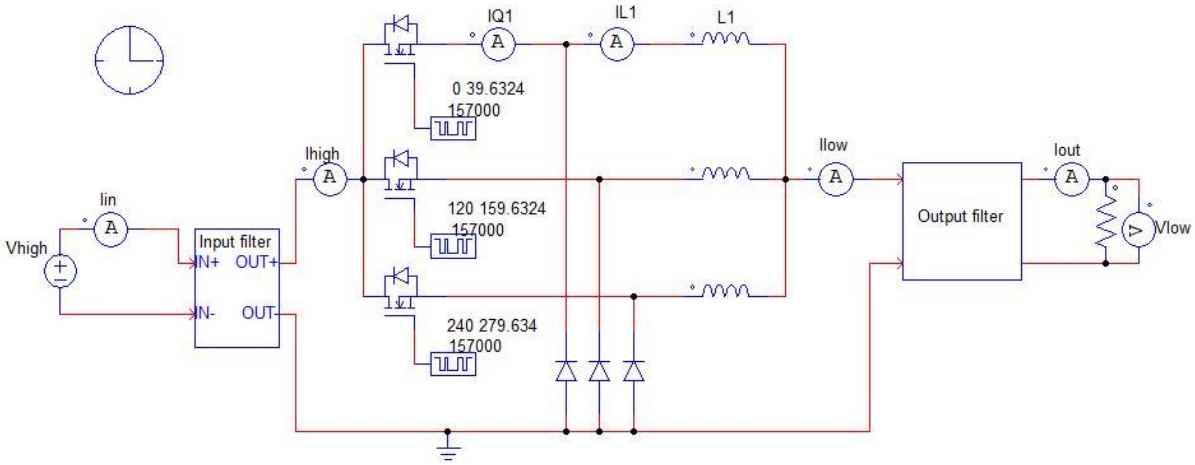
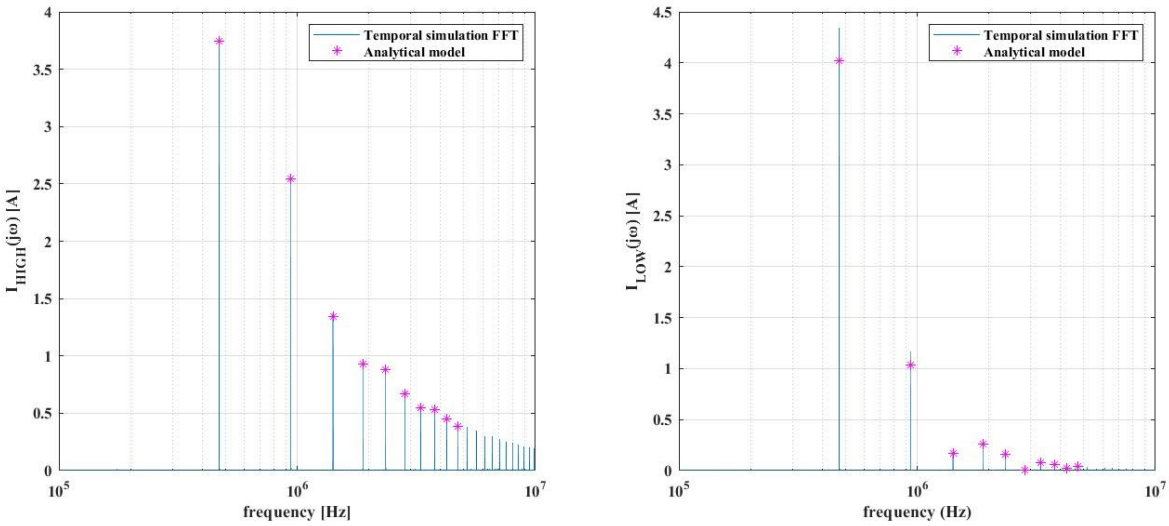


Figure *26*: Time simulation schematic of a 157 kHz 3-phases IBC working at 1484 W, 700V to 200 V

Figure *27* presents the differences between the analytical model and the time simulation FFT. There are some little differences between the simulation results and the analytical model on the output current. This comes from the fact that the losses in the components are not considered in the time simulation whereas it is the case for the analytical model (diode conduction duration is different).



(a) *(b)*

Figure *27*: Comparison of the current spectra of time simulation FFT and of the analytical model for the input (a) and the output (b)

2) IBC filtered currents

Once the harmonics of the input and output currents of the IBC have been obtained, input and output filtered currents I_{IN} and I_{OUT} are straightforward, using the frequency model of the filter circuit (i.e. its current transfer function).

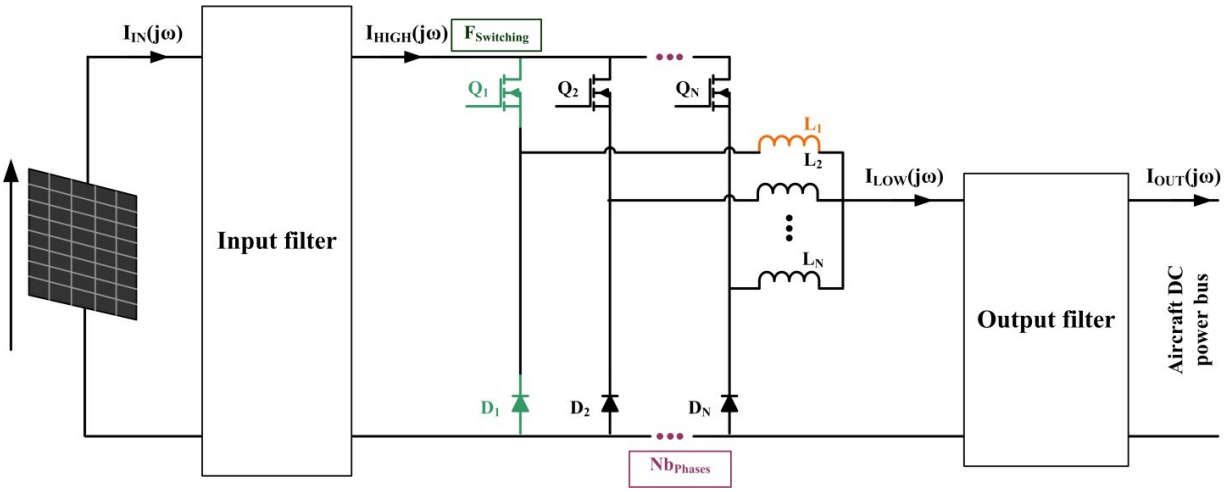


Figure *28*: Interleaved Buck Converter schematic

Figure *29* shows the schematic of the input filter of the IBC. For reminder, the solar panels (V_{GS}) should work at least 5 years (to limit the aging the current THD creating by the converter should be low). Because the main objective is to minimize the weight of the Stratobus sub-systems, the parasitic inductance of the wiring between the converter and the solar generator contributes to the THD reduction and is therefore considered in the input filter model (L_{WIRE} and R_{WIRE} on Figure 29). The filtering components equivalent models (see section II. B.) are then integrated to the filter circuit (L_{HIGH} and C_{HIGH} on Figure 29). The solar panel impedance being unknown at the beginning of the project, it is supposed to be a short circuit (worst case), represented by a low resistance (R_{GS} = 1 mΩ).

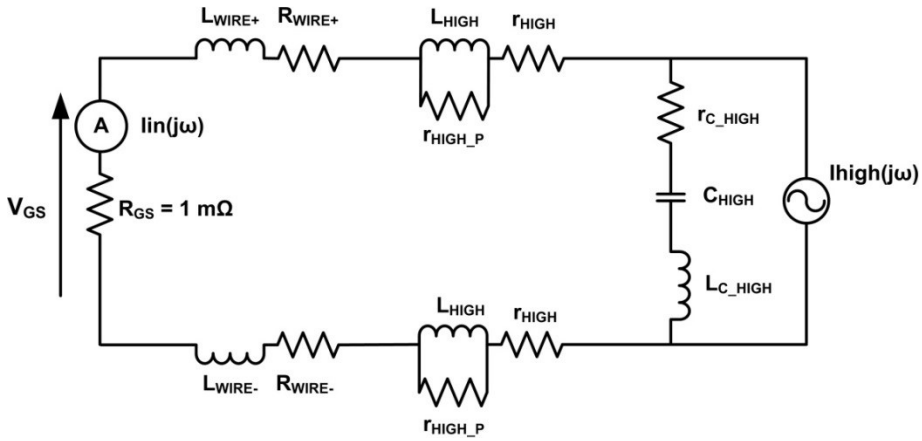


Figure *29*: Input filter and wires of the IBC frequency circuit model

Finally the model of the filter has for inputs the components electrical values and the interleaved Buck input current spectrum I_{HIGH} and for output the converter input current spectrum I_{IN}.

The same method is used for the IBC output filter except that there is no help from the wiring in this case

which conducts into the output filter schematic of Figure *30*. Because the chosen technology of the output filter capacitor is film technology in which the RMS current must be limited, its current spectrum is also computed (Ic_low on Figure *30*).

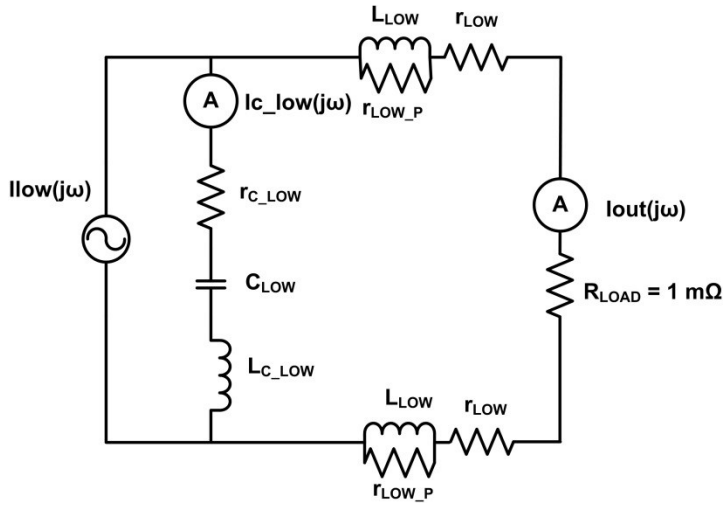
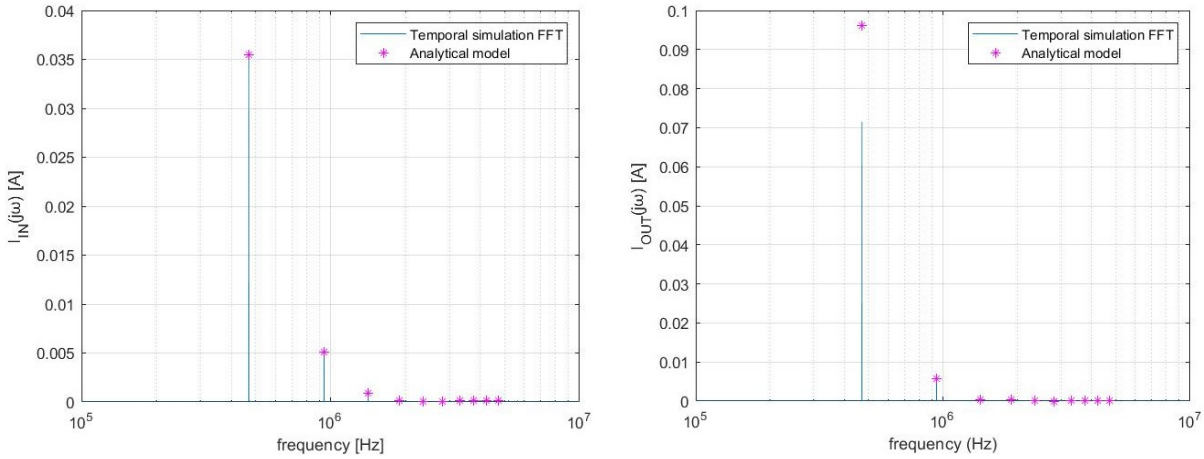


Figure *30*: Output filter of the IBC frequency circuit model

A tools has been developed in the G2ELab laboratory with the aim to automatically generate the frequency model of electronic circuits and its Jacobian matrix [12]. This automatically generated frequency model is compatible with the optimization software CADES and the computation time has been minimized for the optimization of power electronics systems purpose [13] (it takes a few dozen of ms to obtain the computation results and the associated Jacobian matrix of both filters model for 10 studied frequency on a personal computer).

Finally, the analytical model of the filters is compared with the fast Fourier transform of a temporal simulation (Figure *26*, Figure *31* and Figure *32*) under the same conditions except that the simulation does not consider the converter losses and the dependence of the capacitors resistances as a function of the studied frequency.

This explains the slight differences for the spectra of output current and output capacitor.



(a) *(b)*

Figure *31*: Comparison between temporal simulation FFT and analytical input (a) and output (b) current disturbances models

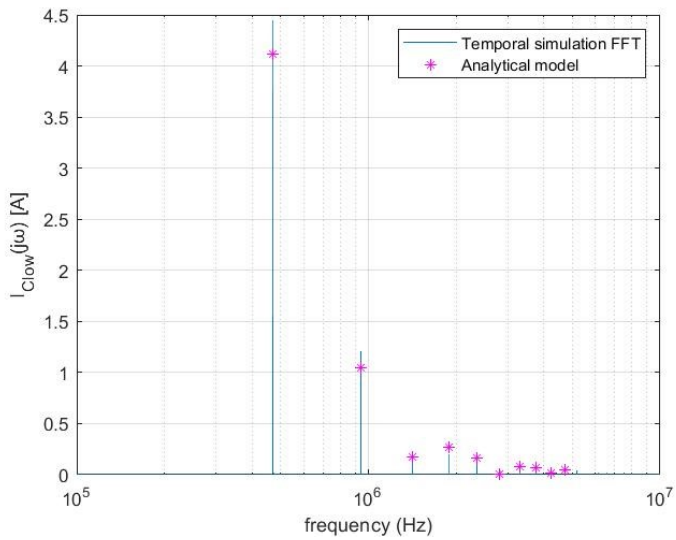


Figure *32*: Comparison between temporal simulation FFT and analytical models of the current spectrum in the output filtering capacitor

C. Conclusion on the IBC waveforms models

Finally, the Interleaved Buck Converter current and voltage waveforms models are organized as presented in Figure *33*. These waveforms are necessary to compute both the power components losses and the converter interferences. The converter waveforms are usually considered as an obvious step by the designers, but when used in an optimization algorithm, the effort to generate them in a suitable form for optimization should not be neglected.

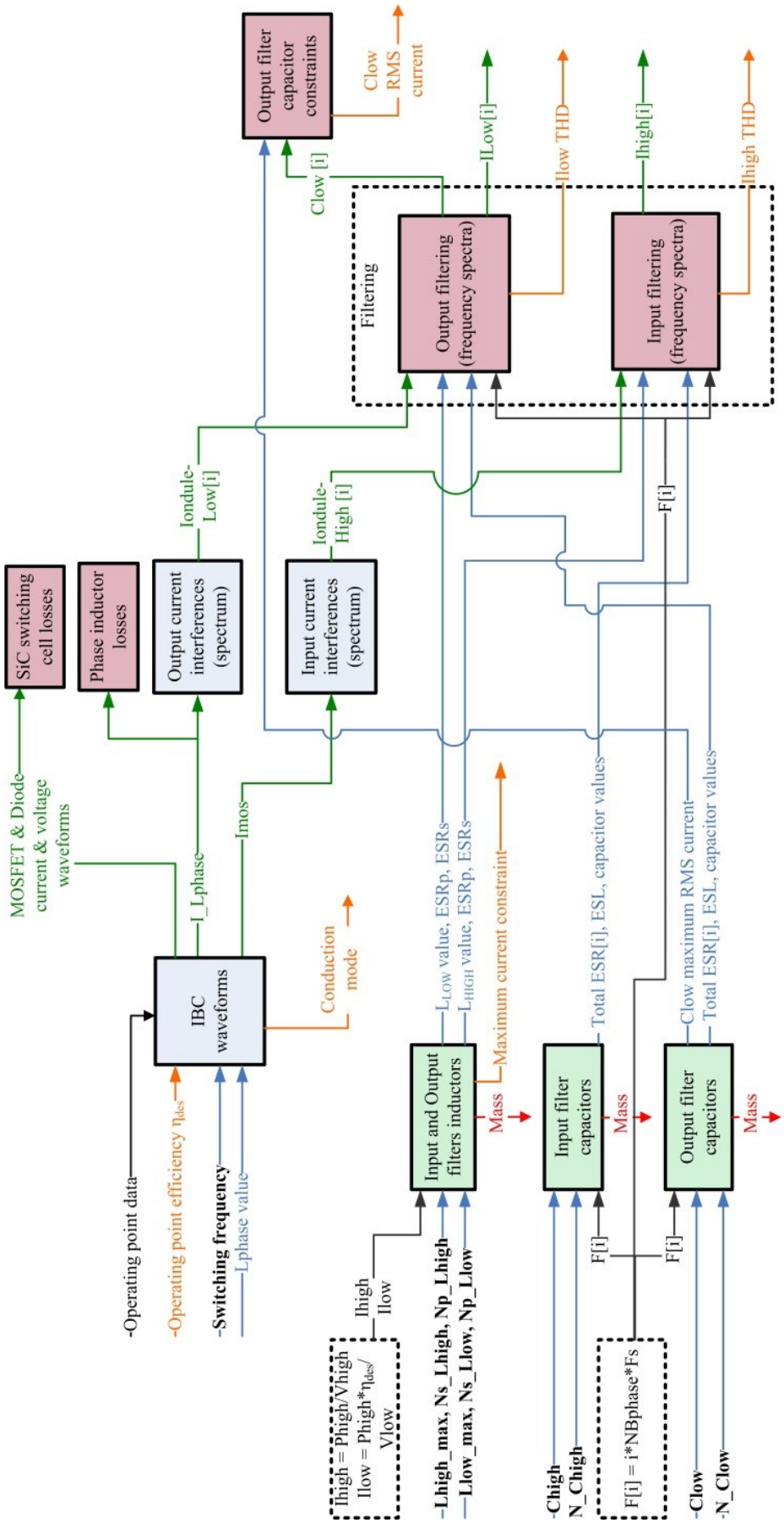


Figure 33: IBC waveforms models organization

It has been demonstrated that despite the apparent difficulty of having the IBC number of phases as a continuous design parameter, it is actually possible by using the frequency domain mathematical properties. This is a major improvement for using gradient-based optimization algorithm in the aim to pre-design in the imaginary world.

However, it is important to notice that the proposed models are valid only when the studied frequency are multiples of the IBC number of phases times the converter switching frequency. In other words, the disturbances created at the switching frequency by the parasitic elements of the converter cannot be taken into account. . Here, for the pre-design, it is not an issue but in the frequency range of EMI, the proposed method should be refined.

IV. CONCLUSION

In this chapter, it has been demonstrated that it is possible to get the components and topology (here the number of phases and the conduction mode) of the converter as directly or indirectly continuous design variables.

For the semiconductors, their current rating is used as optimization input variable. With this variable, all necessary device parameters for the losses and thermal models can be computed.

Getting all the electrical values of the filtering components (that are COTS in this case) is simply done thanks to the judicious interpolations of manufacturer datasheets.

Because the phase inductor is a custom design, a technological description is sufficient to obtain its main electrical parameters. About the converter waveforms, they are linked to three aspects:

- the operating point (fixed in this case),
- the electrical values of the converter components,
- and its topology parameters (here the number of phases and conduction mode).

Specific development and reformulations have been used to get free from the numerically discrete variables inherent to power electronics systems.

For example, condition “if” has been smartly used and the converter has been projected from the time domain to the frequency domain.

These ways depend on the application, but experience and creativity of the designer are also solicited to propose the most adapted model for the dedicated optimization.

Next chapter will focus on the IBC losses models and the associated experimental tests to define the models validity domain.

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Chapter 6: IBC power components losses and thermal models

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I. INTRODUCTION

In the previous chapter it was explained how to get the converter components electrical properties and the current and voltage waveforms with continuous design variables. These data can now be used to evaluate the main constraints of the converter: its losses and their impact on IBC efficiency and components temperature. For the computation of the Interleaved Buck Converter (IBC) efficiency of Stratobus HVPCU, the hypothesis is that only the semiconductors and phase inductor are creating significant losses. Indeed, the filtering components losses are supposed to be negligible and the control command is supplied thanks to an auxiliary source.

Differentiable analytical models of components performances abound in the literature, especially on losses. The designer has to find the closest model from the optimization problem requirements according to the application and make the adaptations if needed.

In the following parts, the requirements for the losses and thermal models will be given in order to properly select them in the literature before a possible adaptation to our DC-DC converter.

Figure 1 reminds the ideal waveforms of the Buck converter in DCM, in the aim to compare the differences with the real waveforms.

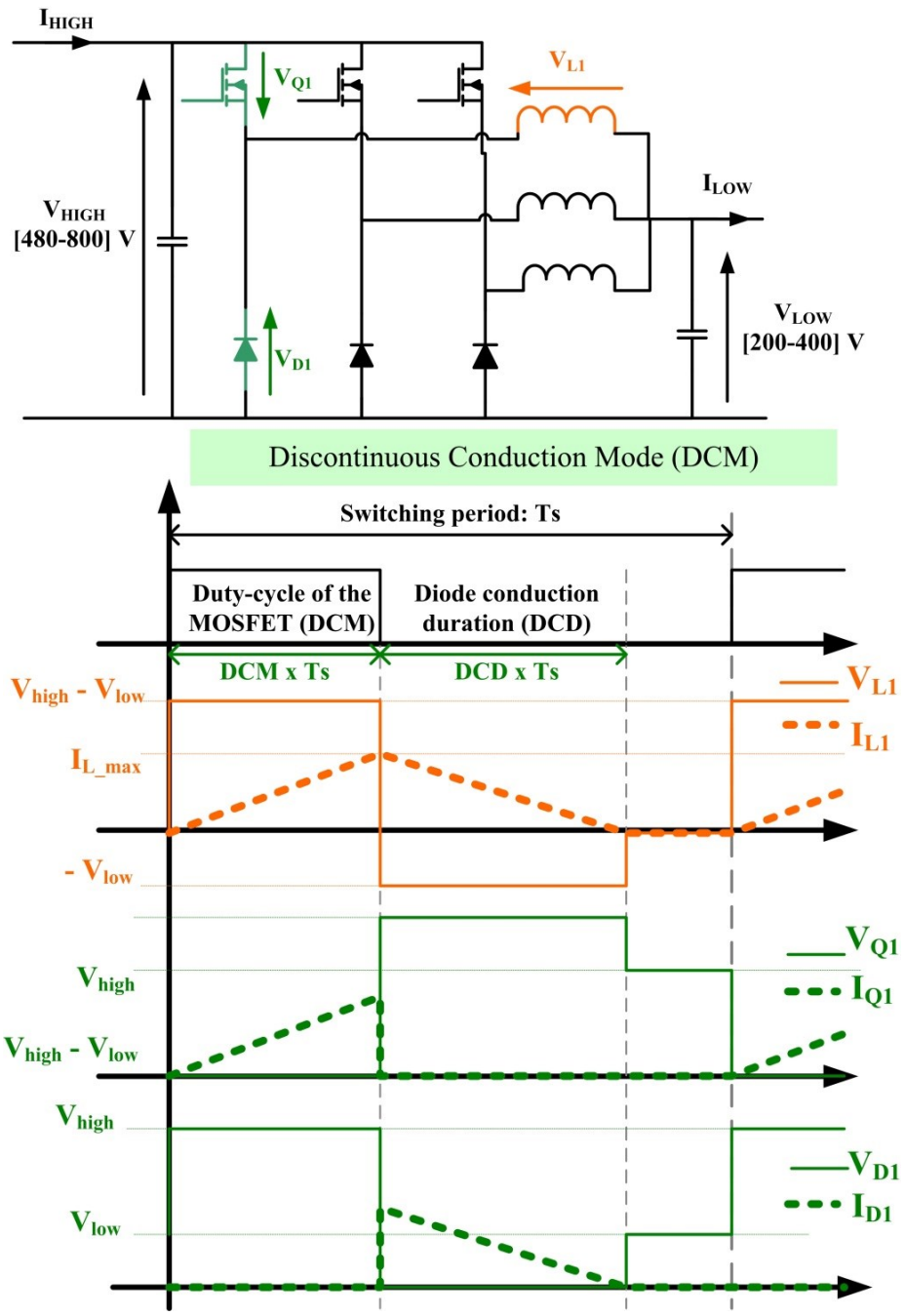


Figure 1: Buck converter ideal waveforms

II. SWITCHING CELL LOSSES AND THERMAL MODELS

In power electronics, the semiconductors junction temperatures need to be well evaluated during the design phase since there is a large risk of failure if it reaches the limit. So the global converter optimization model needs a thermal model of the semiconductors which itself needs the components losses. Those dependencies are highlighted in the optimization problem formulation as shown in Figure 2. As a reminder, all the components

and circuit parameters are provided by the evaluation models detailed in previous chapter. Since they are temperature dependent, the actual junction temperature of the device modifies the components parameters values (see Chapter 5 section II.A.3.).

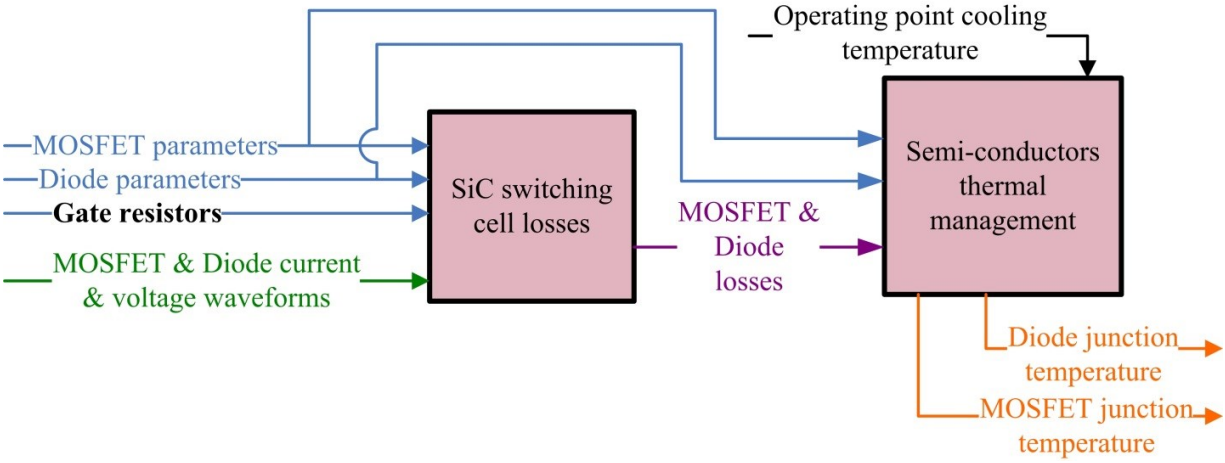


Figure 2: IBC switching cell losses and thermal models schematic

In the following, the choice of the switching losses model selected in the literature is explained as well as the necessary adaptations for the dedicated application. The thermal model of the semiconductors is eventually described.

A. MOSFET and diode losses model

1) Semiconductors conduction losses model

About the MOSFET and diode conduction losses, there are simply computed thanks to the classical equations {Eq. 1;Eq. 2}.

$$Pcond^{MOSFET} = Rds_{on} * IQrms^2 \qquad \text{Eq. 1}$$

With Rds_{on} the on state resistance of the MOSFET at the operating junction temperature and IQrms the RMS current of the MOSFET (obtained from waveforms model).

$$Pcond^{diode} = Vt * IDmoy + Rt * IDrms^2 \qquad \text{Eq. 2}$$

With Vt the threshold voltage, IDmoy the diode average current, Rt the on state resistance and IDrms the diode RMS current (obtained from waveforms model).

2) Semiconductors switching losses model

a) Chosen model and adaptation to the application needs

For reminder, SiC technology has been chosen for the switching cell composed of a N-MOSFET and a

Schottky diode. In the literature, paper [1] was particularly close to IBC application since it gives the analytical model of the switching losses of a SiC MOSFET and SiC Schottky diode pair (Figure 4).

Besides, this analytical model is differentiable and does not contain any inner algorithmic loops: this point is important to bring stability to the optimization. These inner loops have been avoided thanks notably to some hypothesis. One of them is the components capacitances having a step-wise characteristic with two different values as a function of the drain-source voltage (Figure 3). Another one is the neglected gate inductance: it reduces the order of the circuit differential equations to solve.

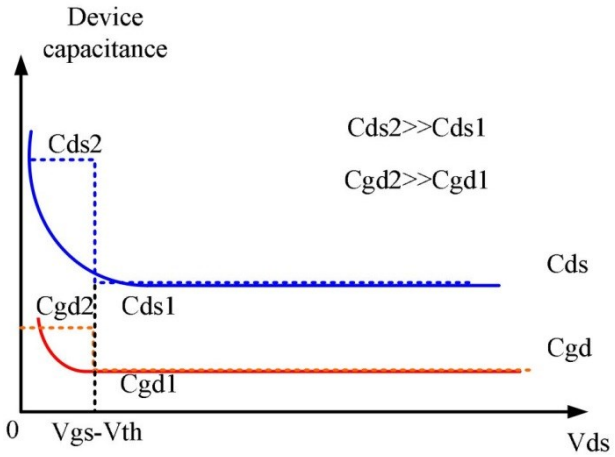


Figure 3: Hypothesis illustration of the nonlinear capacitances Cds and Cgd as a function of Vds from [1]

Slight simplifying modifications have been made on the circuit to better fit our IBC application (Figure 5) as regrouping the parasitic inductances into Ld and Ls or as taking into account that the output current source is not perfect.

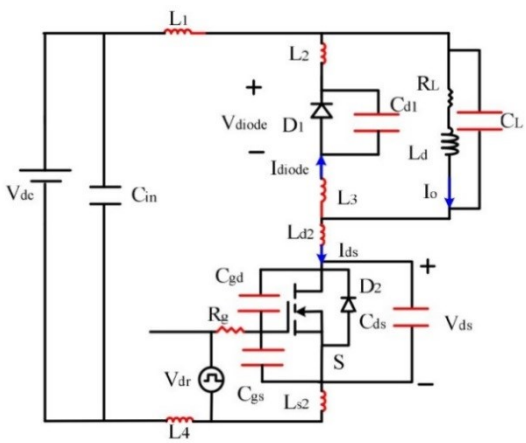


Figure 4: Switching cell under study in [1] paper

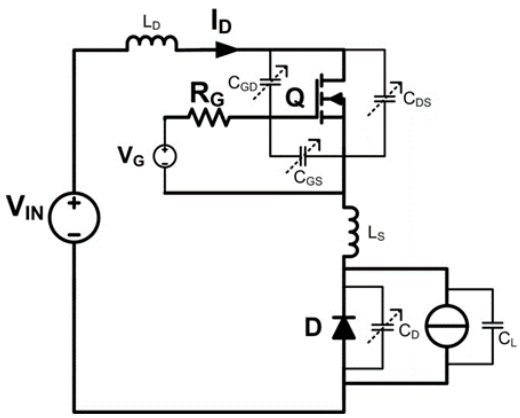


Figure 5: Switching cell under study for the Stratobus IBC

This model is based on the switching waveforms that are divided into several time intervals in which the equations of the cell behavior are directly solved (Figure 6). The detailed hypothesis and equations for each phase are gathered in appendix.

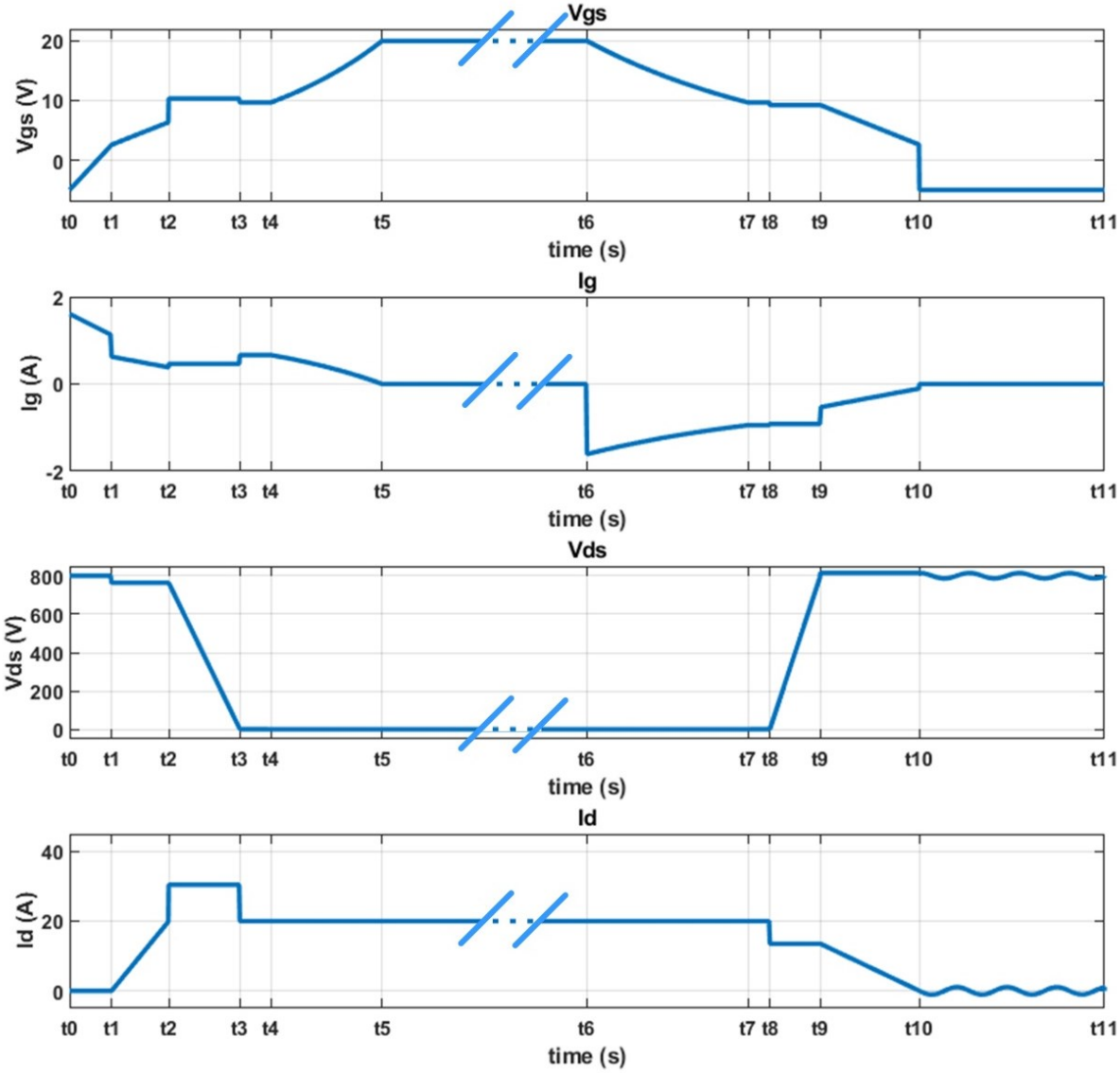
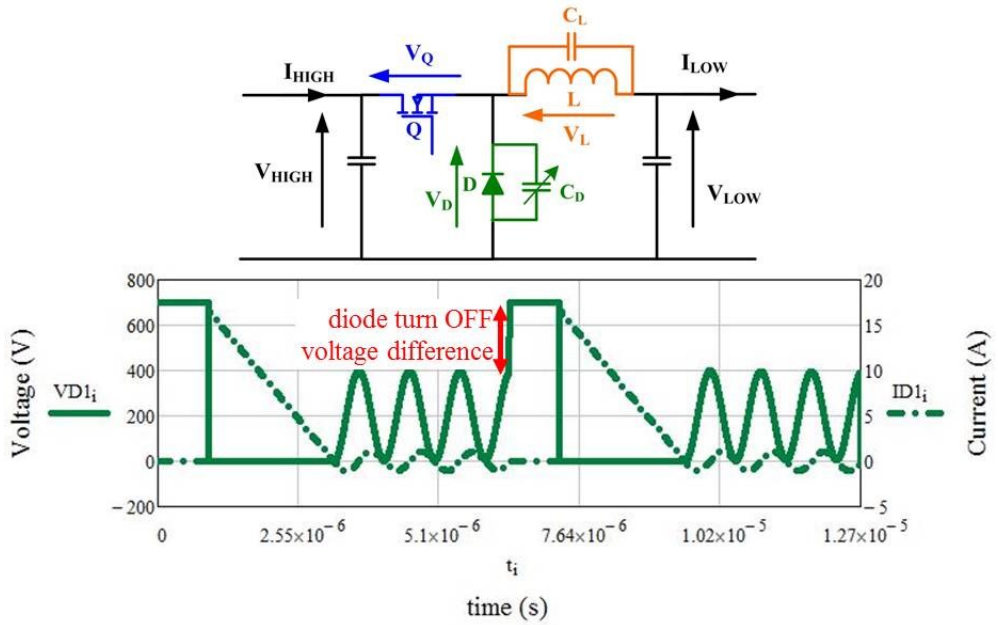


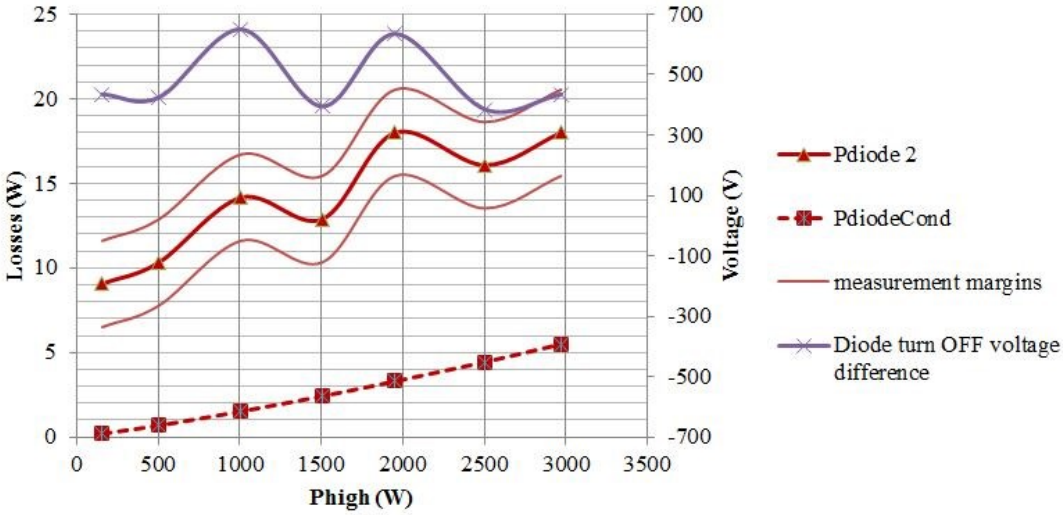
Figure 6: Switching waveforms used for the switching cell losses model inspired from [1] work

b) SiC Schottky diode particularity

The common hypothesis for a SiC Schottky diode is that the reverse recovery is negligible [2], and usually no switching losses are considered: so the only losses are conduction losses. But when the semiconductors losses model - first written under this hypothesis - has been compared to the experimental measurements, the measured losses were surprisingly higher than expected. Figure 7 shows the diode losses measurements with the associated error margins and the computed conduction losses. These losses have been measured thanks to a thermal method that is presented in the next chapter.



(a)



(b)

Figure 7: SiC Schottky diode in a 3-phase IBC (a) theorical waveforms at Phigh = 2.5 kW, Vhigh = 700 V and Vlow = 200 V, (b) losses measurement (Pdiode2) with its error margins, theoretical conduction losses (evaluated with Eq. 2) and the measured diode turn OFF voltage difference (as shown in picture (a) for the operating point Vhigh = 700 V to Vlow = 200 V, input power Phigh being swept

Based on Figure 7 and after checking the method, two statements can be made:

- the difference between estimated conduction losses and the measured losses is too high to be attributed to measurement errors,
- there is a correlation between the diode losses and the value of the turn OFF diode voltage difference as defined in Figure 7 (a).

Besides, this difference between the expected losses of the diode and the actual losses has also been observed

in [3]. The authors made the assumption that the additional losses come from the charge and the discharge of the junction capacitance (so linked to the change of the voltage direction).

This assumption is quite surprising since the charging and discharging of a (parasitic or not) capacitor should not create losses. In Figure *8* the trajectory of the Schottky diode charge vs its voltage is illustrated: from Vhigh at t_0=0, it decreases to zero (phase ①). Then several oscillations between almost zero and Vlow occur (phase ②), until the end of Discontinuous conduction mode, when the diode voltage reaches again Vhigh (phase ③). Of course, depending on the exact time of MOSFET turn on, the initial value of phase ③ may not be exactly Vlow, this is very sensitive to the oscillations parameters. But, as quite recently discovered [4]–[6], the junction capacitance of SiC Schottky diode and Super-Junction MOSFET present an hysteresis that can be shown thanks to Sawyer-Tower test circuit (as shown in Figure *9* from [6]).

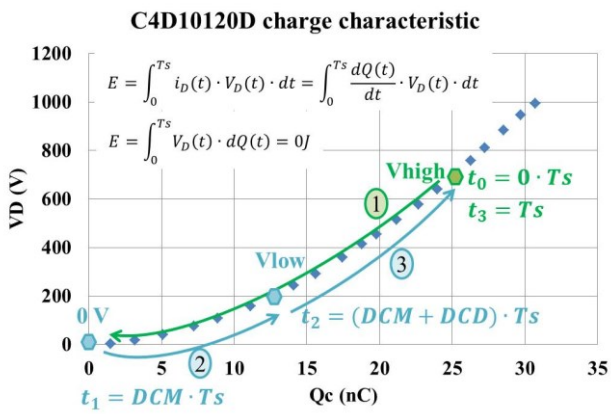


Figure *8*: Illustration of the charging and discharging of the diode junction capacitance in a Buck converter working in DCM

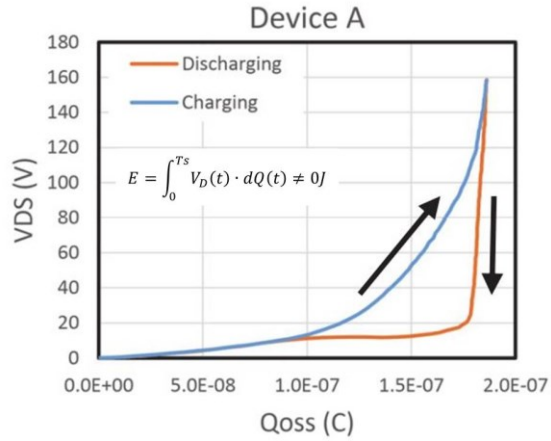


Figure *9*: VDS versus QOSS of Super-Junction MOSFET curve measured with the Sawyer-Tower circuit at F = 10 kHz and Vpk-pk = 160 V from [6]

The authors of [6] suggested based on these observations to use an equation (Eq. 3) similar to Steinmetz equation, to describe the hysteresis losses over the diode capacitor.

$$P_{hysteresis} = k * V^{\beta} * Fs^{\alpha} \qquad \text{Eq. 3}$$

With k, α and β some constants, Fs the frequency of the hysteresis cycle and V the voltage variation across the device.

We can use this equation for our application, based on the experimental results of Figure *7*. We decided to fix the value of α to 1, to keep consistency with the phenomena of switching losses occurring at each diode commutation.

According to the three phases explained previously, and computing the number of oscillations during the discontinuous conduction phase ②, the best combination for fitting the results of Figure *7* was obtained for k =

567 pF and β = 2.37 (see Figure *10*, which will be investigated more in details in chapter 7).

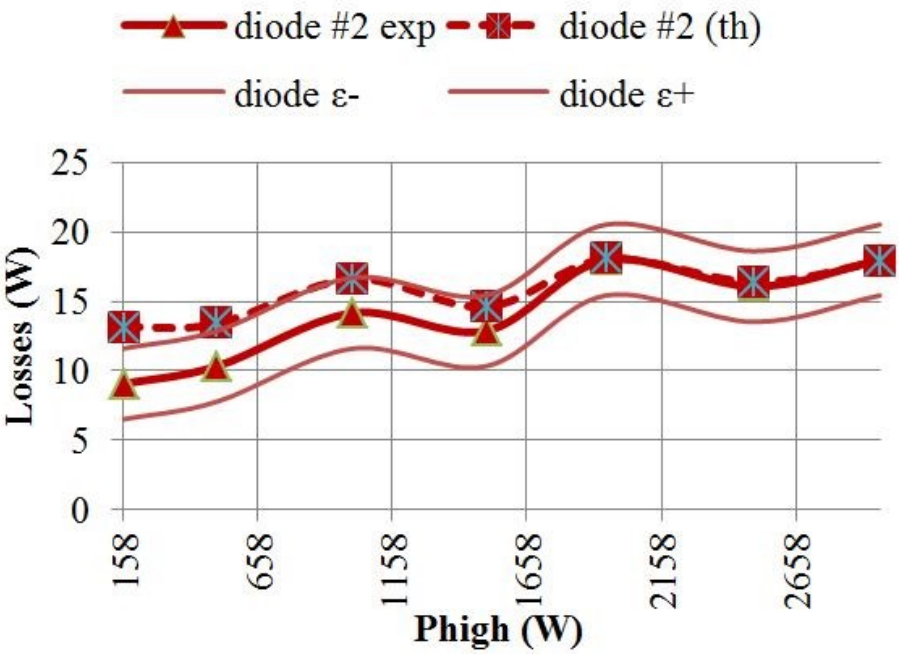


Figure *10*: Results of diode losses versus input power of the converter variation Phigh, with consideration of hysteresis losses of the Schottky junction

Unfortunately, this result depends on the diode characteristics, and cannot be extrapolated to its current ratings, as the other parameters. To be compatible with our modelling strategy, we decided to link the value of k to the diode capacitance, and to fix the value of β to 2, in order to refer to the conventional"CV²" expression, even if the scientific basement for this is not funded for hysteresis behavior. The best value of k fitting our measurements was the value of the diode capacitance at high voltage, k = Cd2, i.e. the diode junction capacitance value under a high reverse voltage.

Finally, the SiC Schottky diode charging and discharging losses can be evaluated during the optimization thanks to {Eq. 4 ; Eq. 5 ; Eq. 6}. To be noted that these expressions can be used for Continuous Conduction Mode operation, thanks to the variable CD which is zero for this mode, therefore cancelling the contribution of oscillations (phase ②).

$$Pdiode^{ON} = Cd_2 * Vhigh^2 * Fs \qquad \text{Eq. 4}$$

$$Pdiode^{OFF} = Cd_2 * (Vhigh - Vlow)^2 * Fs \qquad \text{Eq. 5}$$

$$Pdiode^{oscillation} = CD * \left(Cd_2 * Vlow^2 * \frac{(1 - DCM - DCD) * Ts}{T_{HF}} * Fs \right) \qquad \text{Eq. 6}$$

With Cd2 the diode capacitance value for high diode voltage, Fs the switching frequency, Vhigh the IBC input voltage, Vlow the IBC output voltage, CD the converter conduction mode variable (= 1 if discontinuous, = 0 is continuous), DCM the MOSFET duty-cycle, DCD the diode conduction duration, Ts the switching period of the converter and THF the oscillations period that appear in discontinuous conduction mode.

Figure *11*shows the new results with this other expression. They are not as good as the previous ones, but they are compatible with our design strategy. Again this figure will be commented more in details in chapter 7.

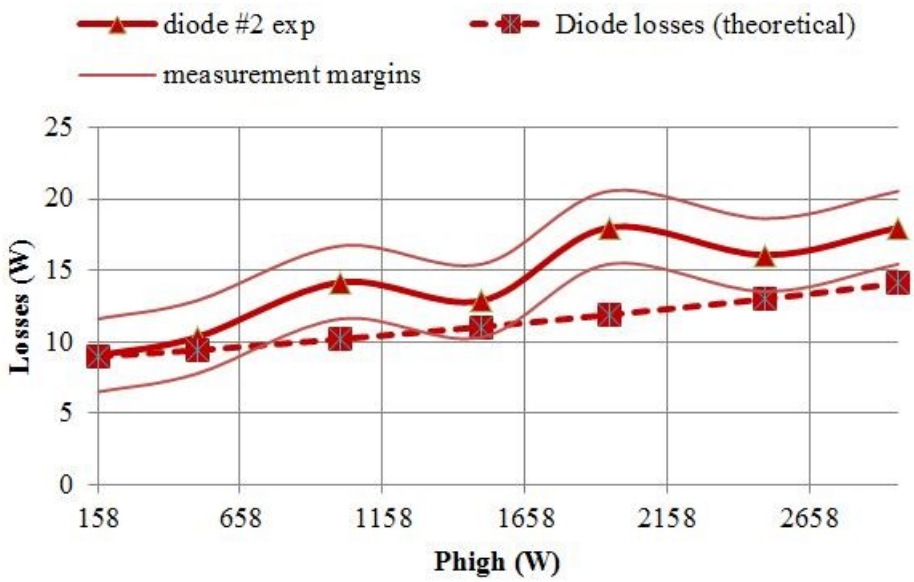


Figure *11*: Results of diode losses versus input power of the converter variation Phigh, with simplified consideration of hysteresis losses of the Schottky junction

Finally, it should be noticed that in the experiment, a high current rating diode has been used (lower current rating was unfortunately not available at the time of validation). Therefore, the stray capacitance and the hysteresis effect are especially highlighted: indeed switching losses are higher and conduction losses lower. Nevertheless, this phenomenon of hysteretic behavior of Schottky diode is very interesting, has been related very recently, and further work on this topic is clearly needed.

B. Semiconductors thermal models

For the pre-design, only the static thermal behavior is considered. The mounting of the discrete devices on the heatsink uses sil-pad (thermal resistance Rth_c,s), which also ensures the dielectric strength. The cold plate is supposed to be ideal, i.e. its temperature does not rise.

A very well known unidimensional electrical equivalent thermal model is sufficient to compute the junction temperature of the device which will be constraint. This model is schematized in Figure 12. The thermal resistance between the device junction and the device case (Rth_j,c) is given by the evaluation model of semiconductor thermal and electrical parameters and the device losses by the switching cell losses model.

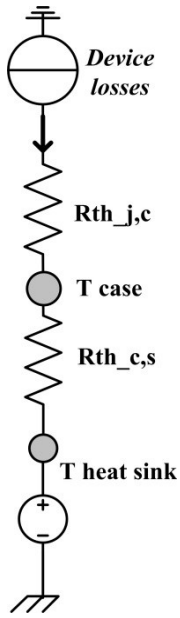


Figure 12: Semiconductors 1-D static thermal model

III. PHASE INDUCTOR LOSSES AND THERMAL MODELS

It is reminded that the power inductors of the Interleaved Buck Converter are made of a toroidal iron powder core and uncoated copper Litz wire molded into a resin. Figure 13 is a picture of the chosen technology.

(a) *(b)* *(c)*

Figure 13: IBC power inductor technology (a) Inductor without resin, (b) molded inductor, and (c) cross-section showing the inside of the molded inductor

The phase inductor represents a large part of components weight in the interleaved buck topology. The algorithm will tend to minimize this component: the risk is to design an inductor too small to properly evacuate its losses. There are two ways to avoid this failure:

- limit the inductor volumetric losses to a certain value,
- estimate the inductor hot point temperature thanks to a thermal model and limit this temperature.

The first solution is too rough if constant volumetric losses are chosen. Indeed, the temperature increase

depends on the capability of the inductor to evacuate the losses, thus on its geometry. Determining the volumetric losses for all possible geometries would be feasible, but asks time consuming characterizations, involving all possible various geometries as illustrated in Figure 14. Therefore, it has been chosen to develop a thermal model of the inductor.

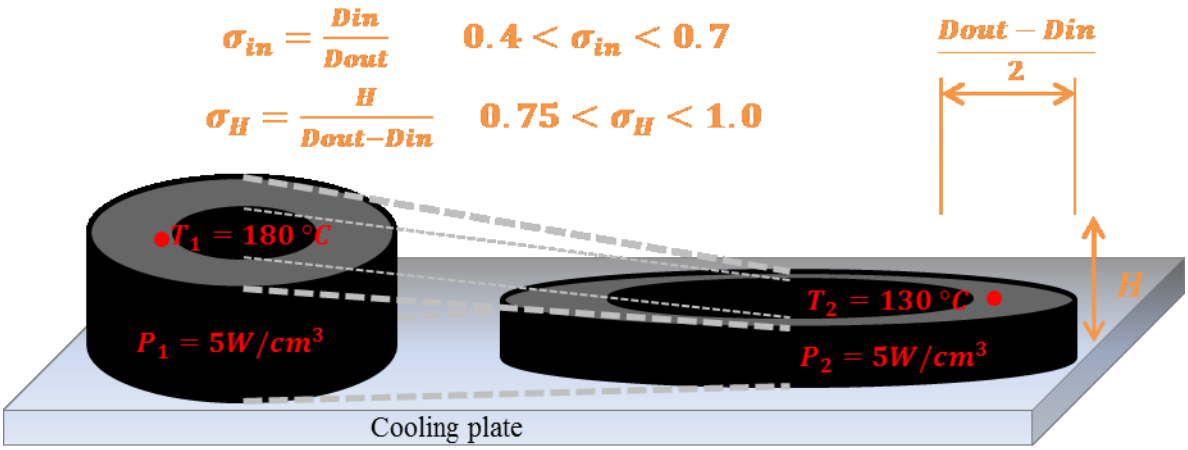


Figure 14: Power inductor quasi-homothetic coefficients definition

Finally Figure 15 presents the organization of the inductor losses and thermal model. In this figure, the orange arrows represent the constraints, the blue arrows the components parameters and the purple arrow the components losses. These models will be briefly described in the following parts.

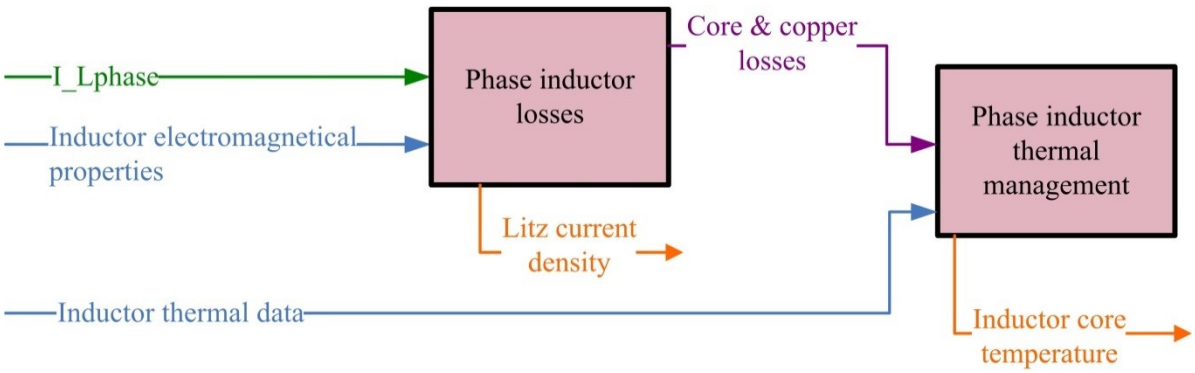


Figure 15: Power inductor losses and thermal models organization

A. Phase inductor losses model

The inductor losses are decomposed into core losses and winding losses. The inductor current and voltage waveforms have been reminded in Figure 1.

1) Core losses

This is a long story in power electronics, and analytical models about core losses abound in the literature.

The impact of saturation is still difficult to be included in analytical models, and the work published up to now [7], [8] necessitate additional measurements on samples, which is not desired in this work where we want to limit the parameters to those available in the datasheet, as Steinmetz coefficients [9]. Fortunately, losses in iron powder material are less sensitive to the DC bias [7] than other materials.

The Steinmetz equation is very appropriate for the gradient based optimization algorithm because it is very simple. However, it is only valid with sinusoidal waveforms: the use of IGSE [10] is therefore required. This formulation is interesting since it does not necessitate other parameters than the Steinmetz parameters and the waveforms (which are already defined in our model) and it is not too complicated to set up inside optimization loop. The full model is described in appendix.

2) Winding losses

The winding losses come from:

- the Joule effect (DC losses),
- the skin effects (AC losses),
- and the proximity effects (AC losses).

The AC and DC resistances are provided by the phase inductor parameters evaluation model (see previous chapter).

Then the winding losses are computed straight forward (Eq. 7 ; Eq. 8 ; Eq. 9).

$$ILphase_{DC} = \frac{Ilow}{Nphase} \quad \text{Eq. 7}$$

$$ILphase_{AC} = \sqrt{ILphase_{RMS}^2 - ILphase_{DC}^2} \quad \text{Eq. 8}$$

$$PLphase_{winding} = R_{DC}^{LITZ} * ILphase_{DC}^2 + R_{AC}^{LITZ} * ILphase_{AC}^2 \quad \text{Eq. 9}$$

With respectively $ILphase_{DC}$, $ILphase_{AC}$ and $ILphase_{RMS}$ the DC, AC and RMS current in the phase inductor, Ilow the IBC output current, Nphase the IBC number of phases, R_{DC}^{LITZ} and R_{AC}^{LITZ} respectively the DC and AC resistances of the Litz wire.

B. Phase inductor thermal model

The inductor thermal model should give the hot point temperature based on:

- the inductor core losses,
- the copper losses,
- the cold-plate temperature (considered ideal so constant in this pre-design),

- and the inductor design (materials, geometries).

This model should be preferentially analytical or semi-analytical for the optimization purpose [11]. That is the reason why one-dimensional (1D) model is preferred over two-dimensional (2-D) model or even three-dimensional (3D) models. Thanks to the azimuthal symmetry of the inductor, 3-D model is unnecessary (Figure 16). It will be shown with the results of this section that a 2D model is required.

The geometry data are provided thanks to the phase inductor parameters evaluation model described in the previous chapter. Aside from the thermal model dimension, knowing the thermal properties of the different materials of the inductor is necessary (Table 1).

Table 1: Required material thermal conductivity value

Material	**Value**	**Material**	**Value**
Thermal paste	$10\ W \cdot m^{-1} \cdot K^{-1}$	Inductor core	Unknown
Resin	$2.16\ W \cdot m^{-1} \cdot K^{-1}$	Inductor core epoxy	Unknown
Copper	$385\ W \cdot m^{-1} \cdot K^{-1}$	Litz wire (transverse)	Unknown
Strand insulator	$0.028\ W \cdot m^{-1} \cdot K^{-1}$	Litz wire (longitudinal)	Can be obtained with Eq. 10

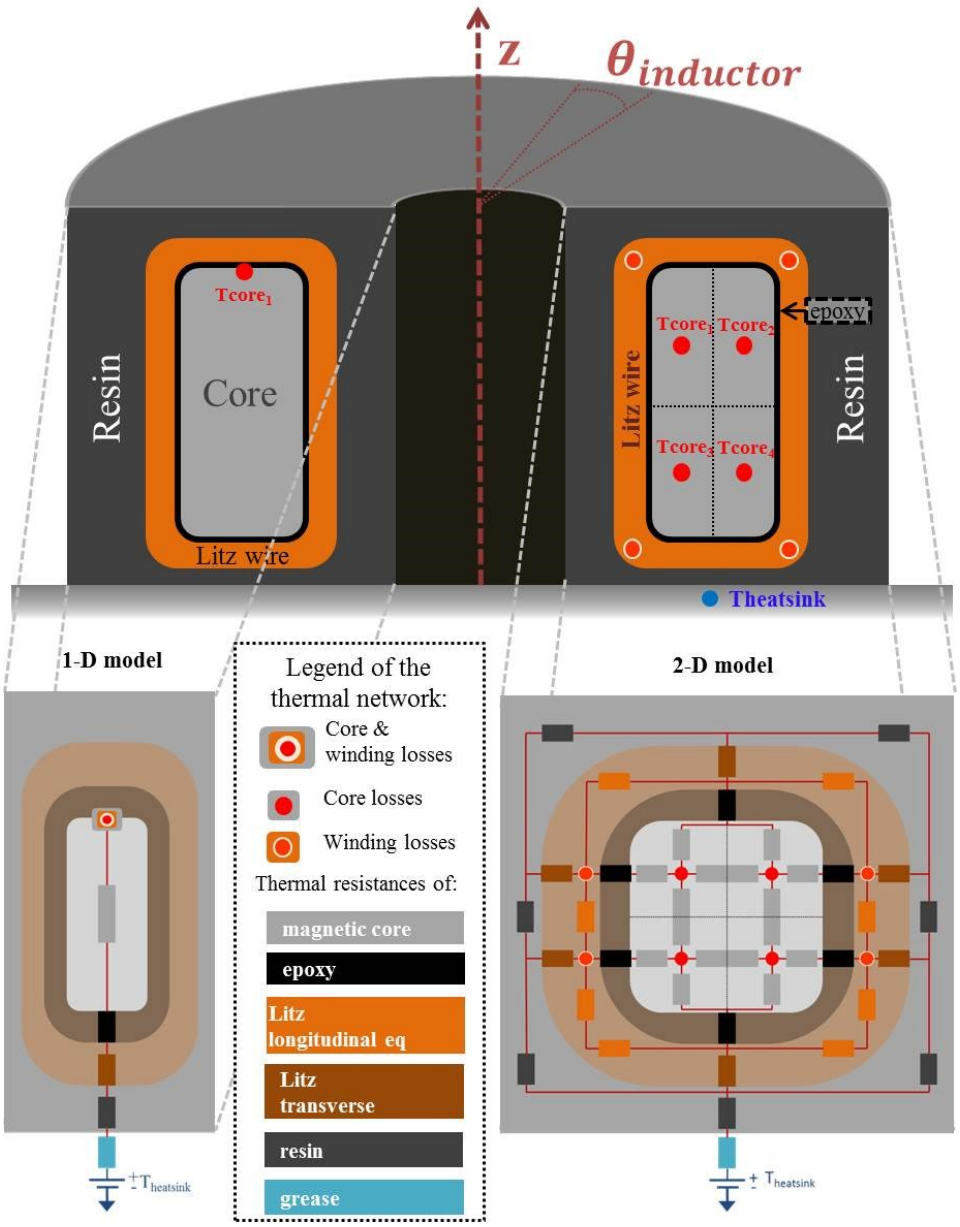


Figure 16: Phase inductor 1-D or 2-D thermal models

Unfortunately the thermal properties of the magnetic core and of the Litz wire are not provided by the manufacturers. Besides, the Litz wire made of copper and insulator and taken in the resin is thermally anisotropic (the thermal conductivity of the Litz wire is different in transverse or longitudinal directions). The longitudinal conductivity of the Litz wire is easy to compute since it is simply a parallel association of several thermal conductors (copper, insulator and resin) (Eq. 10), but unfortunately, the heat flux has to go through sometime in the transverse direction in a practical inductor: it is necessary to determine the Litz wire transverse conductivity.

$$\lambda_{Longiudinal}^{Litz} = \frac{\lambda_{copper} * S_{copper} + \lambda_{insulator} * S_{insulator} + \lambda_{resin} * Sresin}{S_{copper} + S_{insulator} + S_{resin}} \qquad \text{Eq. 10}$$

With λ_X the thermal conductivity of the material X and S_X the section in which the heat flux go trough of the material X

In the literature, reference [12] proposed a 2D thermal model for a toroidal transformer made of several layers of round wires. This is not applicable to the study case because Litz wire strands are randomly distributed. Reference [13],[14] offered an analytical thermal model for magnetics with Litz wire based on physical and geometrical description. But they demonstrated that there is around 50% of error for the case of Litz wires. Reference [15] proposes analytical formula for the thermal conductivity of impregnated Litz wire with different strand shapes (round, square or rectangular) but this model still needs tuning and calibration using experimental data to predict correctly the thermal transfer.

Finally in 2018 another analytical model to determine the Litz wire transversal conductivity with an accuracy of 20% has been proposed [16] (it is the same model than from [13], [14] but with an added resistance taking into account the gap between the strands). But our work was performed in 2017. Therefore we finally chose an experimental method to get the unknown information of Table 1. They have been carried out on toroidal inductor samples with different Litz wires [17].

1) Determination of the inductor core thermal conductivities

A toroidal inductor from the same technology than the one under study in the IBC is used in the experiment. The thermal resistance of the toroidal inductor was measured using the thermal test bench shown in Figure *17*.

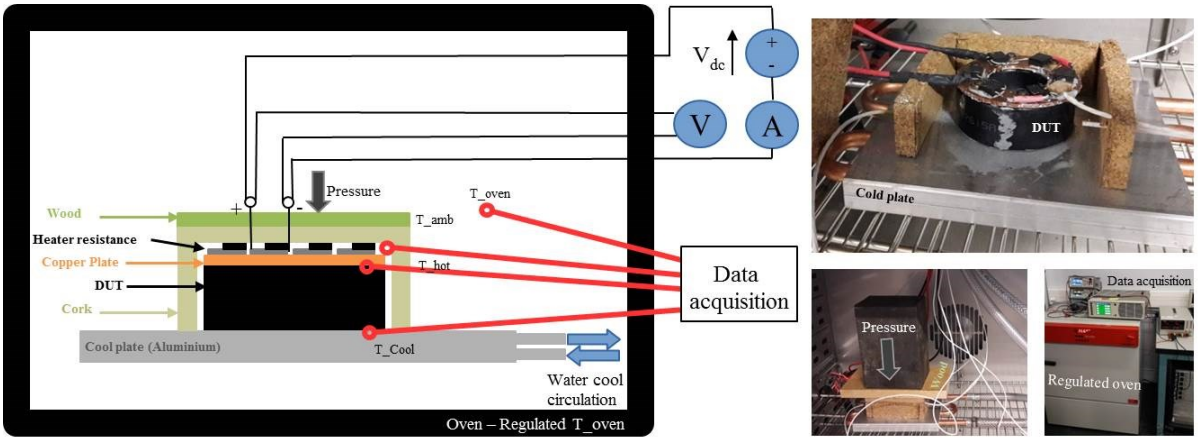


Figure 17: Test bench schematic: top, set-up pictures: bottom

The inductor, or device under test (DUT), was placed on a cooling base plate with a set temperature. Heater resistors placed on a copper plate on top of the DUT generate a fixed amount of heat, hence a temperature gradient across the DUT. The measured temperature gradient ΔT and the generated heat Q can be used to calculate the thermal resistance across the DUT (Eq. 11).

$$R_{DUT} = \frac{\Delta T}{Q} \qquad \text{Eq. 11}$$

Accurate determination of the thermal conductivity of a DUT requires negligible convection and radiation from the DUT, and good thermal contact from the DUT to the heater resistors and the cooling plate. Thus, the DUT was placed inside a closed cork box with k_{cork}≈0.04W/(m.K), and the box itself was put in an oven with regulated temperature. The oven temperature is regulated at the mean value of cold plate and hot plate temperatures to limit convection. Thermal paste k_{paste}≈10W/(m.K) [18] with a supposed thickness of 500 µm is applied to the DUT and a pressure of 78 N is applied through a wooden plate to ensure a good thermal contact between the DUT and the heating and the cooling plates.

A brass sample with a known thermal conductivity was used to validate the thermal test bench. This sample has the same internal and external diameters as the sample toroidal inductor, but is 3.44 times thicker to obtain a measurable gradient of temperatures along this sample with relatively high conductivity. The error between the measured and the estimated thermal resistance of this brass sample is 10.7 %, attributable to measurement uncertainty, ignored convection and impurities in the sample. The measurement on the sample is also reproducible, with only 0.5 % difference in results between different measurements.

First, only the magnetic core thermal resistance has been measured ($R_{CORE+EPOXY}$ = 3.92 K/W). This core had to be also polished and measured again in the aim to deduce also the thermal resistance of the epoxy that surrounds the core. With the present experimental set up, the material conductivity can be directly deduced thanks to (Eq. 12).

$$\lambda_{MATERIAL} = \frac{L}{S \cdot R_{DUT}} \qquad \text{Eq. 12}$$

with S the section of the material that the heat crosses along the length L.

Finally, the magnetic core and epoxy thermal conductivities are summarized in (Table *2*).

Table *2*: thermal conductivities of magnetic core materials

Material	**Thermal conductivities**
Magnetic powder core	λ_{CORE} = 3.95 W.m^{-1}.K^{-1}
Epoxy	λ_{EPOXY} = 0.34 W.m^{-1}.K^{-1}

2) Determination of the Litz wire transversal thermal conductivity

Once the magnetic material conductivities are known, the Litz wire is studied. In order to ensure that the measured data will be valid for the optimization search area, thermal measurements are performed on various samples of Litz wire and inductor. Four different samples of Litz wire, described in Table 3, were used. Two of the Litz samples (#1 and #2) have similar copper section as well as the other two Litz samples (#3 and #4). Two

samples (#1 and #3) have the same strand diameter to address the same switching frequency, and so do the other two samples (#2 and #4).

Table 3: Litz wire samples

Litz sample	**#1**	**#2**	**#3**	**#4**
Number of strands	81	320	210	855
Strand diameter [mm]	0.2	0.1	0.2	0.1
Strand insulator thickness [µm]	12.5	8	12.5	8
Measured external diameter [mm]	2.56	2.74	4.92	5

The molding of the inductor and the number of turns in the winding were also varied. In order to test the impact of the Litz wire on the side, four inductor samples (1, 2, 4 and 6) were molded only at the bottom of the inductor (Figure 18 (a)) whereas three samples (3, 5 and 7) were molded up to the top of the inductor (Figure 18 (b)). All the samples have a single-layer winding but some samples (6 and 7) have fewer turns such that the winding covers only 66\% of the core in order to check the impact of filling rate. Figure 18 (c) shows an inductor with partial winding filling which is molded only at the bottom. The impact of the number of strands within a Litz wire is also analyzed on the samples.

(a) (a) (b) (b) (c) (c)

Figure 18: Sample pictures. Left: before the Litz wire cutting, right: after the litz wire cutting (used for measurements). (a) molded only at the bottom and 100\% layer fill rate, (b) molded to the top and 100 % layer fill rate, (c) molded only at the bottom and 66% layer fill rate

These different samples are summarized in Table *4*.

Table 4: Measurement results of the different sample

	sample 1	***sample 2***	***sample 3***	***sample 4***	***sample 5***	***sample 6***	***sample 7***	***sample 8***
Litz #	1	2	3	4	3	4	4	4
Molding height	Bottom	Bottom	Bottom	Bottom	Top	Top	Bottom	Top
Layer fill rate	100 %	100 %	100 %	100 %	100 %	100 %	66 %	66 %

A thermocouple has been installed between the magnetic core and Litz wire at the bottom of the DUT (Figure 19) for direct measurement of thermal resistance between the hot plate and the bottom of the core R_1 and that between the bottom of the core and the cooling plate R_2.

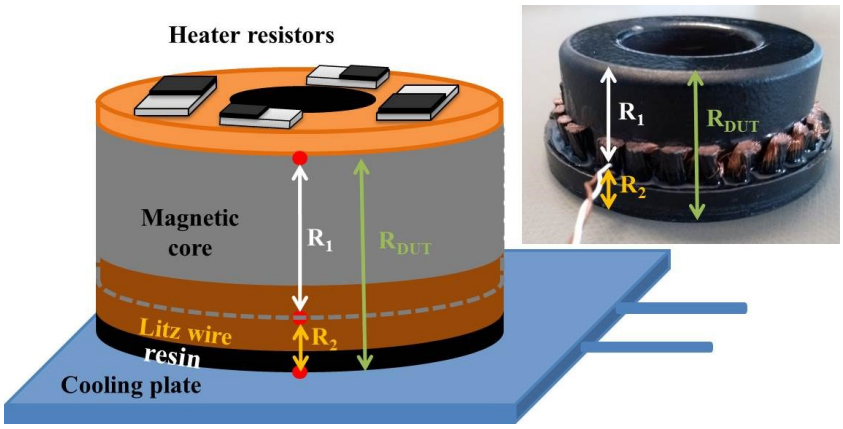


Figure 19: Measured thermal resistances on the DUT

3) Measurement results and analysis

a) Measures

The thermal resistances R_1 (from the hot plate to the bottom of the core), R_2 (from the bottom of the core to the cooling plate) and R_{DUT} (R_1+ R_2) as shown in Figure 19 were calculated from the known generated heat and the measured temperature gradient, and the results are summarized in Table 5.

Table 5: Measurement results of the different sample

	sample 1	***sample 2***	***sample 3***	***sample 4***	***sample 5***	***sample 6***	***sample 7***	***sample 8***
Litz #	1	2	3	4	3	4	4	4
$R_{TH}1$ [°C/W]	3.17	3.04	-	-	2.15	1.71	3.10	1.72
Molding height	Bottom				Top		Bottom	Top
Layer fill rate	100 %						66 %	
$R_{TH}2$ [°C/W]	0.82	0.76	*0.86*	-	0.92	0.57	0.74	0.76
$R_{TH}TOT$ [°C/W]	4.00	3.80	-	3.50	3.07	2.28	3.85	2.49

Note: For Sample 4, R_1 and R_2 are excluded because of a failed thermocouple.

The results can be used to obtain the effective thermal resistances of Litz wire since the thermal properties of all other materials (epoxy, resin, core) as well as the contact thermal resistances (thermal paste) are known.

Comparison of R_{DUT} of samples 4 and 6 shows the influence of the molding height on the cooling of the sample. It proves that 2D-model is necessary for this application (1-D model would conduct into an oversizing of the inductor).

b) Analysis

It is possible to identify the Litz-wire conductivity based on the measurements of Table 5 using optimization method as presented in Chapter 4. In order to limit the meshing level of litz-wire material in a sample thermal network model (as Figure 16), an equivalent longitudinal conductivity k_{leq} is defined (Figure 20). This k_{leq} is a

representation of the faculty for heat to spread longitudinally in the Litz wire when the heat comes from its transverse direction. If only transverse and pure longitudinal conductivities (k_t and k_l) are used, a thinner meshing will be required.

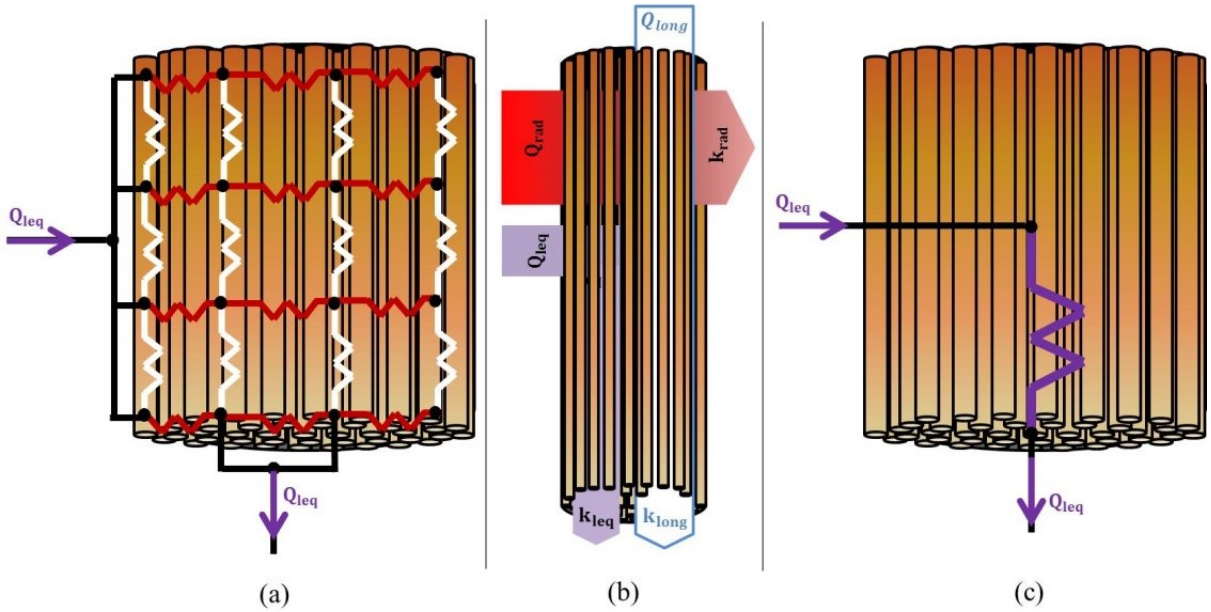
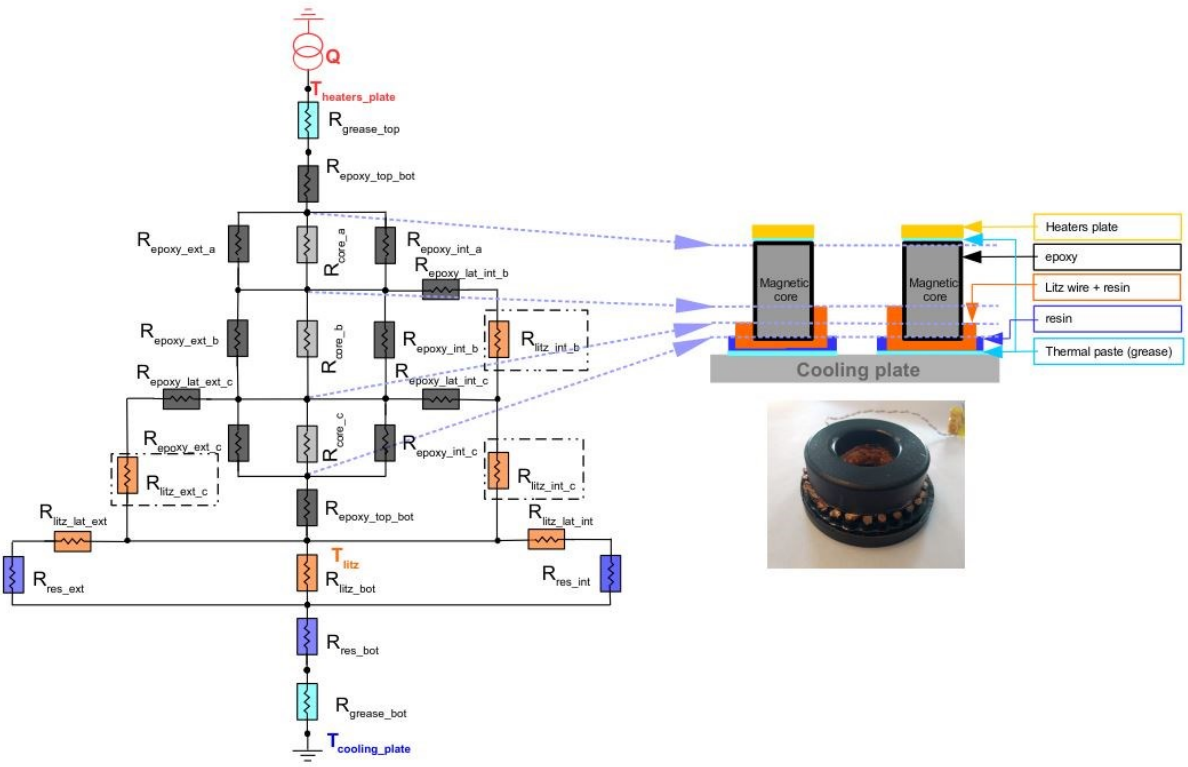
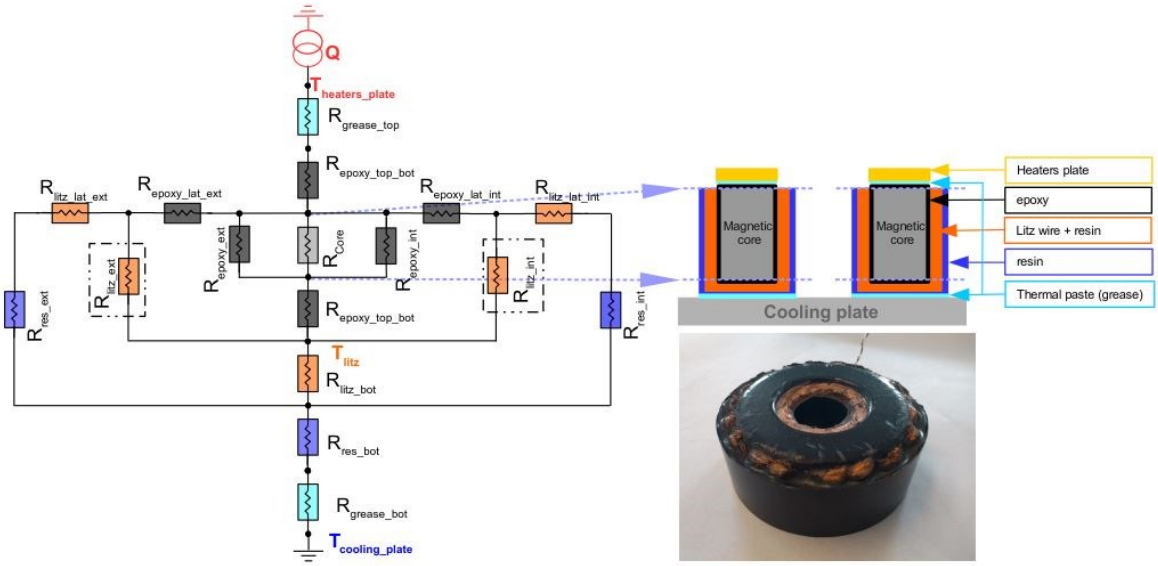


Figure 20: Definition of Litz wire thermal conductivities. (a) Path of different heat sources, (b) the transverse and longitudinal resistances set as a thermal network inside the Litz wire, (c) definition of the longitudinal equivalent thermal resistance with a conductivity of k_{leq} substituing the thermal network in (b).

There are altogether four different thermal network models, one for each combination of molding height (top and bottom) and layer fill rate (100 % and 66 %). Figure 21 shows the thermal network models for samples having 100% layer fill rate. Thermal network models for samples 7 and 8 having 66% of filler rate are respectively similar to those in Figure 21 (a) and (b), but with an additional thermal resistance representing resin in parallel with R_{litz_bot} to account for the fact that the layer is not full.



(a)



(b)

Figure 21: Thermal network models for samples 1 to 4 (a), and 5-6 (b), showing thermal resistances corresponding to the core material (light grey), epoxy (dark grey), grease (light blue), resin (dark blue) and Litz wire (orange). Litz wire thermal resistances calculated using the equivalent longitudinal conductivity are surrounded by dashed rectangle; the other Litz wire thermal resistances are calculated using the transverse conductivity.

For each Litz wire sample (#1 to #4), an optimization routine is used to solve the inverse problem of finding the thermal conductivity of the Litz wire which minimizes the squared error between the model estimations and

the measurements. Figure 22 shows the inverse problem to solve for estimating the Litz wire thermal conductivity. For Litz #3, the inverse problem is solved simultaneously for inductor samples 3 and 5 and for Litz #4 it is solved simultaneously with samples {4,6,7,8}.

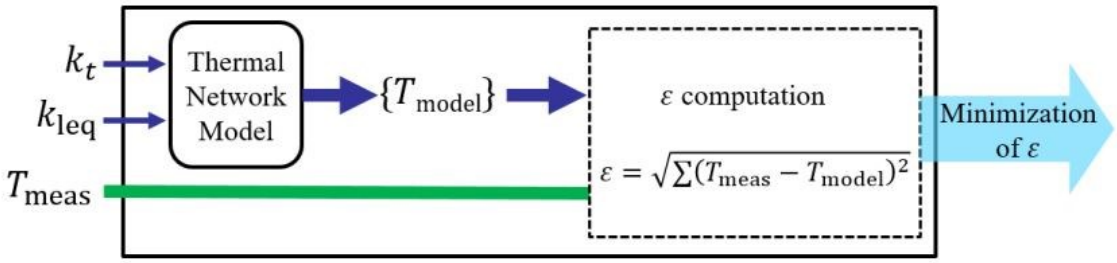


Figure 22: Inverse problem for calculating the thermal properties of Litz wire

Table 6 summarizes for each Litz wire the values of the thermal conductivities k_t and k_{leq} obtained with the identification method and k_l the pure longitudinal conductivity obtained with Eq. 10. This table shows that the thermal transverse conductivity of the considered Litz wires is not very good and that it impacts the longitudinal equivalent conductivity value despite the very good pure longitudinal conductivity.

Table 6: Transversal and longitudinal equivalent thermal conductivities of the Litz wire sample

Litz	**#1**	**#2**	**#3**	**#4**
k_t [W.m^{-1}.K^{-1}]	0.79	0.85	1.11	1.23
k_{leq}[W.m^{-1}.K^{-1}]	26.3	22.5	19.3	35.2
k_l [W.m^{-1}.K^{-1}]	191.15	165.03	134.82	132.84

4) Thermal model of the phase inductor used for the optimization of the IBC

Table 6 gives the measured thermal conductivities for different wires. But in the pre-design process, it is necessary to optimize the Litz wire configuration (number and diameter of strands) since the switching frequency is an optimization parameter (but global copper section is constraint by the current density constraint).

It would so be useful to get a simple relation-ship between the structure of the Litz wire and its thermal conductivity. We tried to investigate if the copper ratio of the Litz wire was correlated to its thermal conductivity. Figure *23* shows the Litz wire conductivities as a function of its copper ratio.

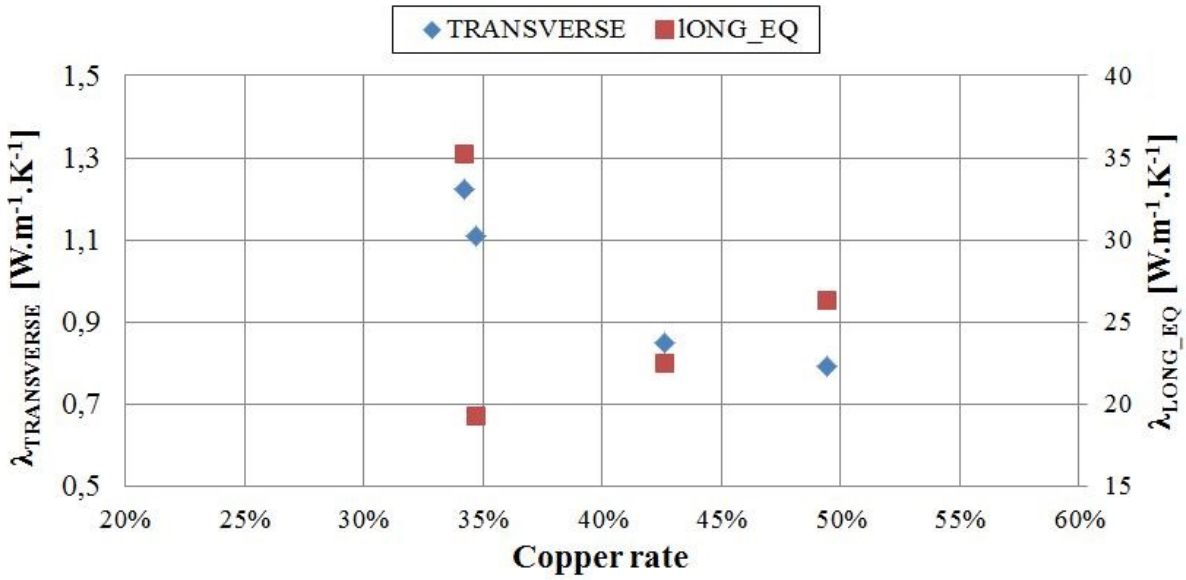


Figure *23*: Litz thermal conductivities repartition depending on its copper rate

When the copper (λ_{copper} = 360 W/(m.K)) ratio decreases and the resin-air (λ_{resin} = 2.16 W/(m.K) ; λ_{air} = 0.025 W/(m.K))) ratio increases, the radial conductivity of Litz wire rises! This is due to the complexity of the Litz wire, which explains the difficulty to find in the literature analytical models of the transverse conductivity.

Thankfully, it has been demonstrated in [17] by sensitivity analysis that the toroidal inductor thermal behavior is much more impacted by its geometrical dimensions than by a slight sweep of the Litz wire thermal conductivity. Besides, the Litz wire configuration used in the previous experiments should not be far from the optimizable Litz wire for the IBC. It has so been decided to take the mean value of the longitudinal equivalent and transverse thermal conductivities of the Litz wire. It is not accurate but provides a good order of magnitude for a predesign step. Table 7 summarizes the values of the thermal conductivities that will be considered for the optimization thermal model of the IBC toroidal phase inductor.

Table 7: Material thermal conductivity values

Material	Value	Material	Value
Thermal paste	$10\ W \cdot m^{-1} \cdot K^{-1}$	Inductor core	$3.95\ W \cdot m^{-1} \cdot K^{-1}$
Resin	$2.16\ W \cdot m^{-1} \cdot K^{-1}$	Inductor core epoxy	$0.34\ W \cdot m^{-1} \cdot K^{-1}$
Copper	$385\ W \cdot m^{-1} \cdot K^{-1}$	Litz wire (transverse)	$1\ W \cdot m^{-1} \cdot K^{-1}$
Strand insulator	$0.028\ W \cdot m^{-1} \cdot K^{-1}$	Litz wire (long_eq)	$25.8\ W \cdot m^{-1} \cdot K^{-1}$

Finally a 2D-thermal model of the toroidal inductor has been built as in Figure 16. The equivalent electrical circuit of the toroidal phase inductor thermal network has been automatically generated thanks to the specific generator tool developed in G2ELab to be compatible with CADES framework [11], as for the input and output filters in chapter 5.

IV. CONCLUSION

The losses and thermal models of the power components are critical for the design of a power converter since they lead to important constraints. Analytical losses models abound in the literature. The choice of one model among the others must be done based on mainly the technology choice of the component and secondly on the optimization algorithm constraints (differentiability, no inner loops, etc.). Generally, the model from literature must be adapted to the application like components implementation, control of the converter or technical constraints.

Finally the models must be tested on practical breadboard. That is the subject of the next chapter.

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Chapter 7: IBC Power Components Losses Models Compared to Experimental Data

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I. INTRODUCTION: OBJECTIVES OF THE EXPERIMENTS

The main objective of the following experiments is to define the validity domain of the IBC optimization models in the global aim to define the proper limits of the optimization and to check that no physical phenomenon has been forgotten. In this Stratobus application, the optimization will first have for purpose to negotiate the main specifications, in other words the converter working voltages and power ranges. Therefore the input voltage, output voltage and converter power will be swept to verify that the optimization models follow the same tendencies than the experimental data.

The experimental data to be checked are:

- the converter functional waveforms and associated electrical constraints,
- the converter power components losses,
- the converter global efficiency.

These experiments will be performed on a prototype working only in discontinuous conduction mode (DCM) for two reasons. First the preliminary optimizations demonstrated that the optimal CCM IBC is much heavier than the optimal DCM IBC (see next chapter). Besides the models uncertainties are higher in DCM, in particular about the switching cell losses due to the oscillations during the diode and MOSFET dead time. Therefore, measurements are especially useful in this mode to confirm the various assumptions.

The validity of the models will be questioned in two steps:

- first by using all available data (switching cell circuit, inductor characterization data and MOSFET turned ON voltage measurement) in order to confirm the understanding of the physic in the system (i.e. without the necessary simplifications and assumptions made on some parameters for the optimization models),
- secondly, by comparing experimental measurements to the optimization model with the estimated parameters of the system.

II. EXPERIMENTAL SET-UP

A. Prototype characteristics

1) Description of the prototype

The prototype has been designed to ensure the conversion [480 – 800] V to [200-400] V with a maximum power of 3200 W. It is composed of 3 phases, working in Discontinuous Conduction Mode. KoolMu 26 material was used for the phase inductor. The MOSFET and diode references have been chosen according to the available ones on the world market on that time (July 2017). The switching frequency is 157 kHz. It is worth noting that the prototype is not the result of the optimization which will be presented in next section. Even if some parts of the design have been carried out with our models and optimization strategy (number of phases, phase inductors design, switching frequency…), it has been built based on available components on the market place and for model validation purpose.

Due to the prototype instrumentation (test connection, solder points, semiconductors location, etc..), the switching cell circuit parasitic inductances will be larger than in an actual implementation. This will be discussed in the following sections. To avoid the destruction of the material and to facilitate the validation of the semiconductor switching losses model, the gate resistor (for both turn ON and turn OFF) is chosen to have a large value (13.8 Ω).

The main characteristics of the prototype are summarized in Table 1.

Table 1: Prototype main characteristics

Input power	[0 – 3] kW	Switching frequency	157 kHz
Input voltage	[480 – 800] V	MOSFET reference	C2M0040120D
Output voltage	[200 – 400] V	Diode reference	C4D10120D
Cooling plate temperature	[35 – 65] °C	Gate resistor value	13.8 Ω
Conduction mode	DCM	Phase inductor	material: KoolMu 26 ; value: 28.5 µH
Number of phase	3	Litz wire	143 strands of 100 µm

In addition, the prototype is versatile: it is possible to change the number of phases (from 1 to 4), to change or add filtering capacitors and inductors and to add an EMI filter at both input and output of the converter. Figure 1 is a 3D view of the top of the PCB from CAO software showing the different parts of the prototype.

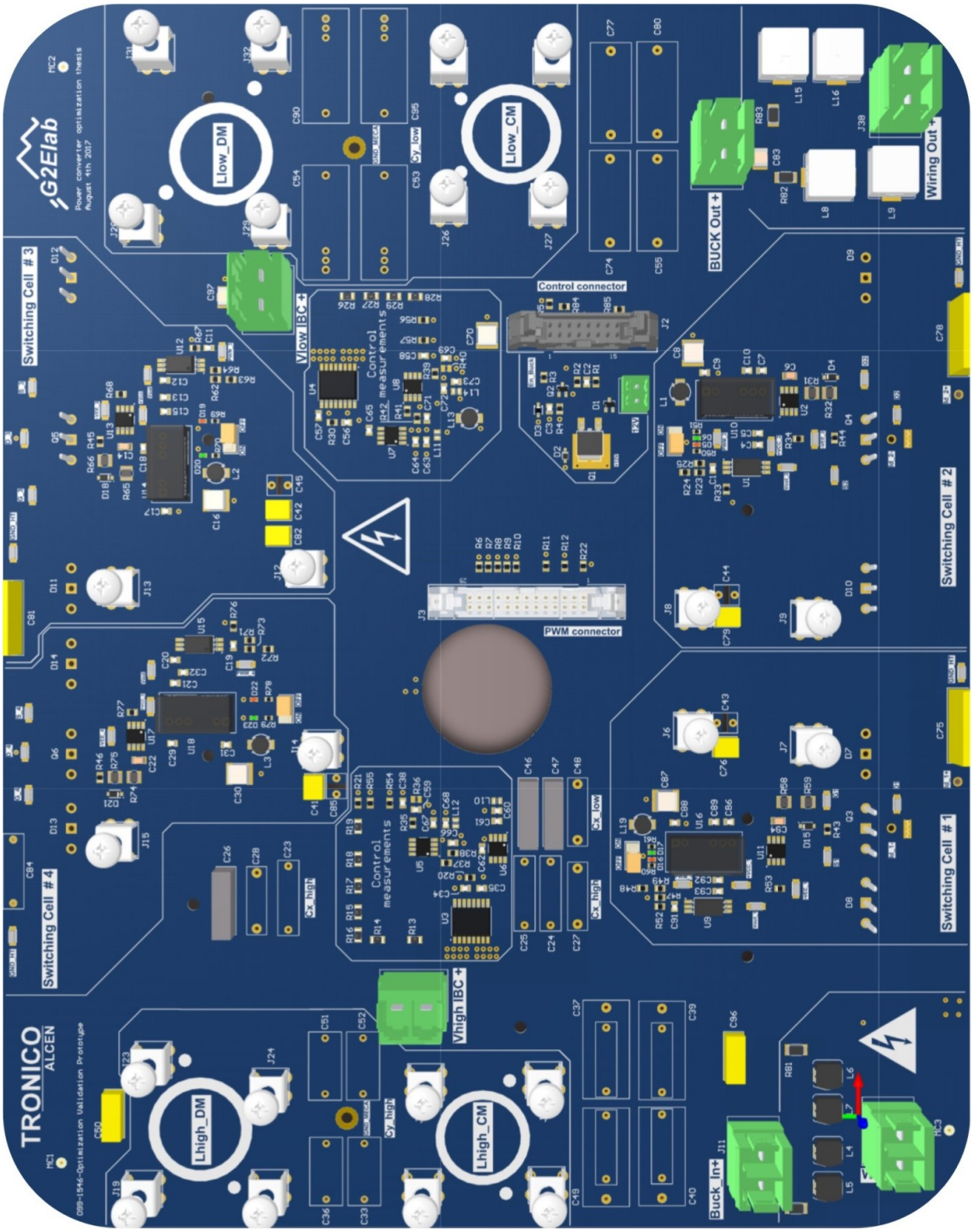
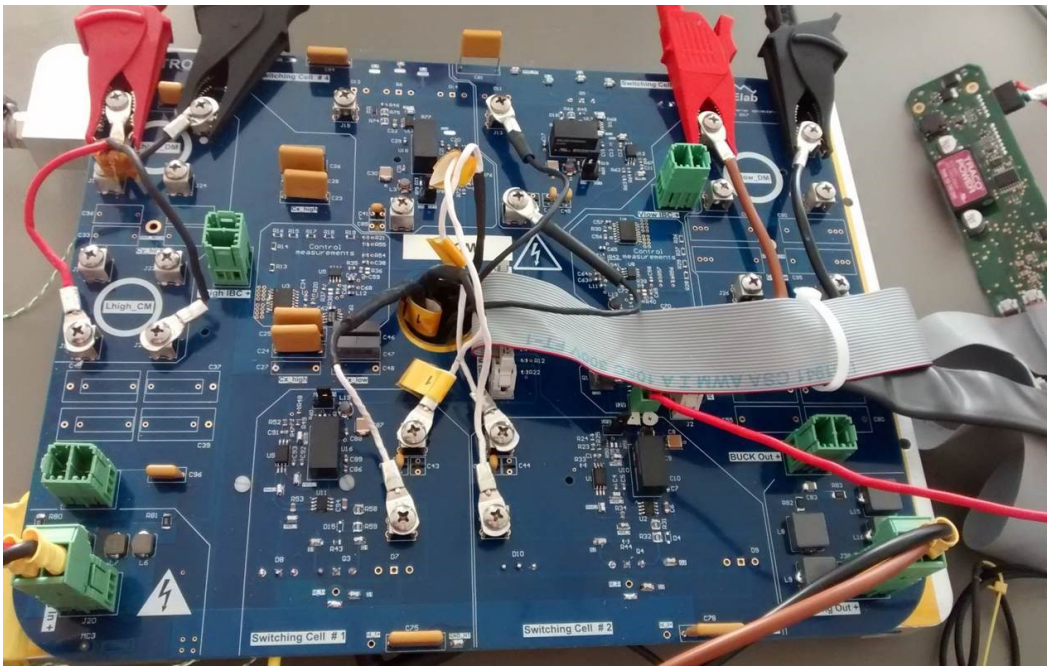


Figure 1: Prototype printed circuit board 3D view from CAO software

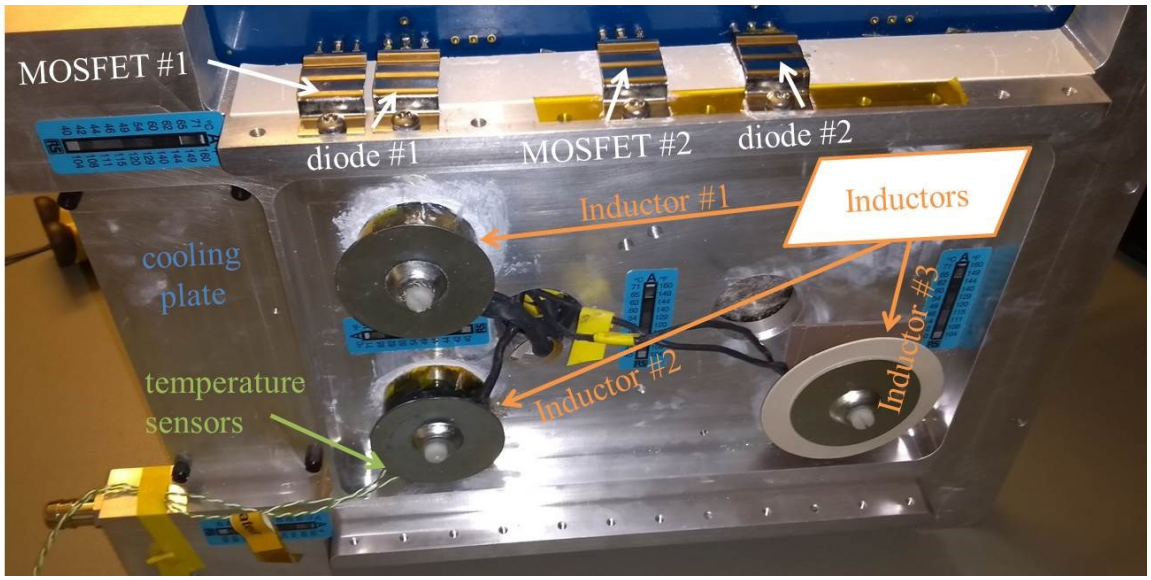
The wiring between the converter and the source and load can be simulated through small inductors at the input and output of the converter. There are dedicated locations for future EMI filters

The cooling is ensured thanks to a water heat sink and an external heat exchanger. The water temperature regulation accuracy is 1°C. The semiconductors are located on the side of the cooling plate whereas the phase inductors are situated on the bottom (Figure *2*).

The drivers have been oversized to be able to work from 16 to 300 kHz with an IBC power MOSFET maximum current rate of 90 A. Their individual power supply can be activated or deactivated thanks to a switch. The control (i.e. PWM signal) is ensured by a micro-controller placed on an external control board (green board on Figure *2*(a). The PCB has been designed for a 1000 V maximum voltage and it is made with 4 layers. The bottom layer is a plane set to be the voltage reference of the IBC, the top layer is dedicated to the signal traces while the inner layers are dedicated to the power traces of the IBC.



(a)



(b)

Figure *2*: Prototype pictures, (a) top view, (b) bottom view of the built prototype

2) Characterization of the prototype parasitic elements: C_L, Ls and Ld

The first step prior testing the prototype is to characterize the elements for which the uncertainties are high. The parasitic elements C_L (stray capacitance of the phase inductor), Ls and Ld (stray inductances of the PCB) used in the switching cell losses model, have thus been measured with an impedance analyzer (Keysight E4990A 20 Hz-120 MHz with Keystone 16047E terminal (F ≤ 100 MHz)).

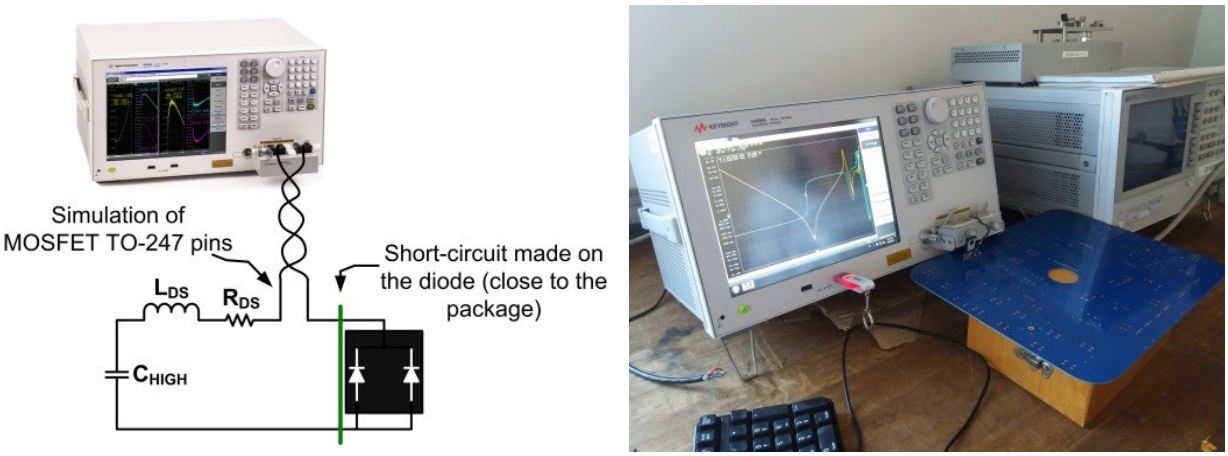
First the phase inductors characterization results are presented in Table 2. Lphase is the inductance, C_L the

parallel capacitance, Rs the serie resistance and Fr the resonant frequency of the inductor. It should be noticed that the phase inductor #3 used in this bench is unmolded, contrary to the phase inductors #1 and #2, resulting into a lower parasitic capacitance. This characterization shows that first C_L is strongly dependent of the manufacturing. This will be discussed in the following section. The resin multiplies the capacitance C_L by around 2. In other word, there is an impact of the technology choice to cool the phase inductor on the semiconductors losses and on the EMI behavior of the converter. As often in power electronics, everything is linked showing the importance of optimizing the converter in its whole. On the other hand, the consequence of technological choice is tricky to take into account in our work. Another remark is that the capacitance is different from a phase inductor to another one for a same design: it will result in different oscillations frequencies during DCM, thus leading to hard quantification of this phenomenon, highly sensitive to this stray element. Eventually, the phase inductor values are also not exactly equal between each component. There is also incertitude about this value during the design phase.

Table 2: Phase inductor impedance measurements

Inductor reference	Lphase (µH)	C_L (pF)	Rs (mΩ)	Fr (MHz)
inductor #01	28.3	37 (16 before molding)	39.8	4.91
inductor #02	28.7	72 (41 before molding)	34	3.50
inductor #03 (unmolded)	28.8	21 (not molded)	24.7	6.48

The PCB has also been characterized with the impedance analyzer according to the test schematic of Figure *3*.



(a) (b)

Figure *3*: PCB inductance measurement (a) schematic, (b) picture

The definition of a switching cell is not easy in multicellular converters, since the DC bus is shared between each of them. In the PCB design, one decoupling capacitor has been placed close to each switching cell. In order to get an order of magnitude of the switching cell inductance, several measurements have been carried out. First, only the decoupling capacitor of switching cell #1 has been soldered on the PCB. The MOSFET of this switching cell has been removed, and the diode short-circuited as close as possible to the package, to keep the impact of the diode's pins in the measurement (Figure *3* (a)). The measurement of the resonant frequency combined with the value of the decoupling capacitance (obtained from low frequency) leads to the value of the inductance. The same method has been applied to switching cell #3 (decoupling capacitor #3 and diode #3 short circuited).

However, during normal operation, all decoupling capacitors of all switching cells may contribute to any commutation. To quantify this phenomenon, two decoupling capacitors (#1 and #3) have been soldered, and the new values of the loop inductance #1 and #3 have been measured again (Figure *4*). All results are summarized in Table 3.

Despite a small decrease of the inductance, due to paralleled circuits, the order of magnitude is not changed so much.

Table 3: Printed circuit board inductances measurements

switching cell inductance #1 (Ld+Ls) with only Capacitance #1	31 nH	*switching cell inductance #3 (Ld+Ls) with only Capacitance #3*	43 nH
switching cell inductance #1 (Ld+Ls) with Capacitance #1 and Capacitance #3	28 nH	*switching cell inductance #3 (Ld+Ls) with Capacitance #1 and Capacitance #3*	32 nH

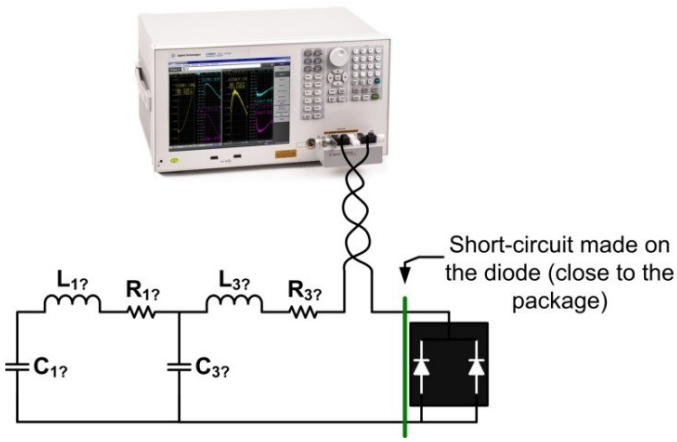


Figure *4*: Measure of the apparent inductance L1-3

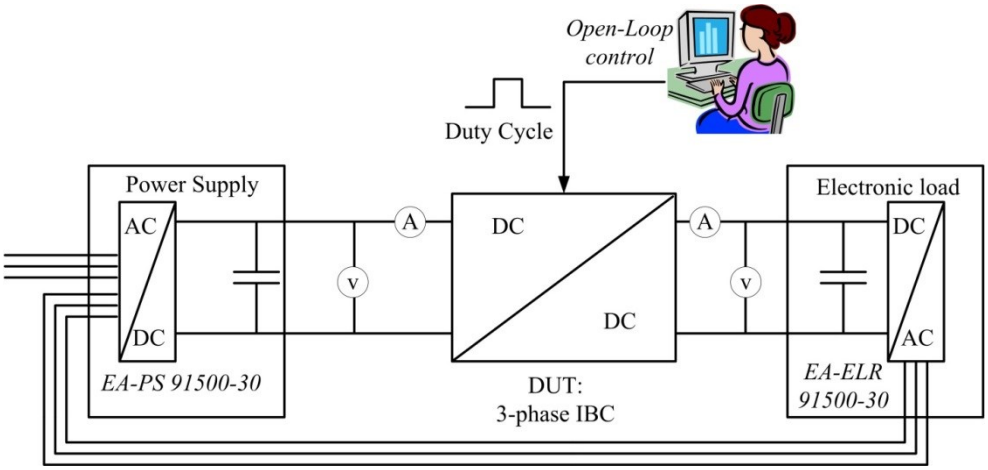
Finally, an order of magnitude of 30nH (or even less with the influence of decoupling capacitor #2) can be

considered for the loop inductance of the PCB. This not far from what could be identified based on the manufacturer datasheet (see chapter 5), based on the MOSFET C2M0080120D manufacturer switching losses test circuit.

B. Test bench and measurements set-up description

1) Converter global measurements test bench

Figure 5 shows the electrical power test bench used for the experiments. The prototype has been power supplied thanks to a DC-source set in voltage control and provided power to a voltage controlled electronic load. The power transfer is controlled thanks to the MOSFET duty-cycle (open-loop control).



(a)

(b)

Figure 5: Electrical power test bench: (a) schematic, (b) picture

The input and output currents have been measured thanks to shunt resistors and 34401A Agilent multi-meters

for a good accuracy of the global converter efficiency measurement (± 1%).

2) Semiconductors measurements set-up

The diode and MOSFET voltage waveforms have been observed thanks to THDPO200 differential voltage probe and the MOSFET drain current thanks to a Rogowski current waveform transducer.

The semiconductors losses have been thermally measured. A first calibration step has been performed with DC current in the devices for which both the electrical conductions losses and the case temperature are measured. As shown in Figure *6*, a thin copper sheet is placed between the MOSFET case and the Sil pad with grease to ensure a good contact. A thermocouple has been glued with a thermal adhesive on the copper sheet close to the MOSFET (same procedure for the diode).

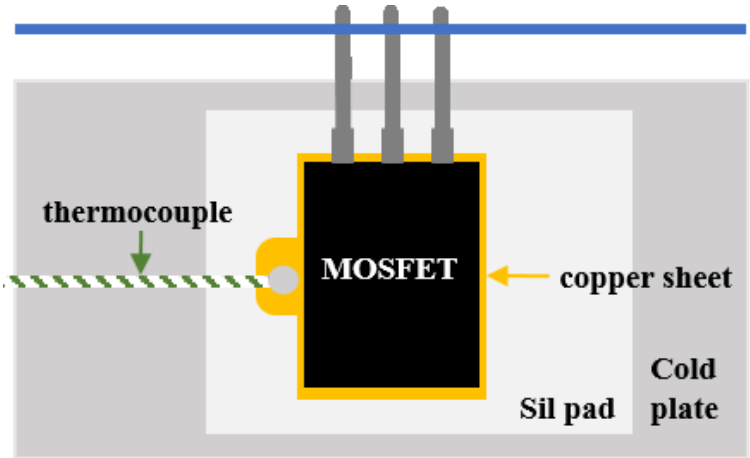
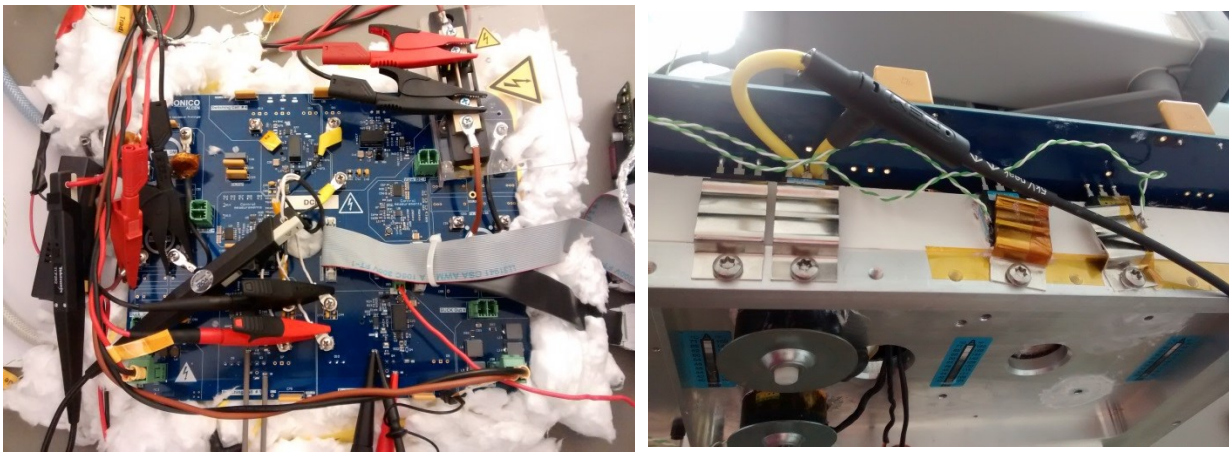


Figure *6*: Semiconductor case temperature measurement schematic

The thermal environment must be controlled: the room temperature is regulated around the cooling temperature (22°C for 25 °C) so that the thermal exchanger regulation is better (water temperature ripple limited to 0.5 °C). The thermal convection has been limited thanks to the glass protection all around the prototype (Figure *5*, (b)) and to the thermal resistance fiber put nearby the converter (Figure *7* (a)). The assembly is kept constant between calibration and actual measurements. The chosen switching cell for the losses measurements is the #2 for which the routing has been done in order to have a certain distance between the MOSFET and the diode (as shown on Figure *7* (b)). This distance was necessary to uncouple the thermal behavior of each device (this has been verified during the calibration).



(a) (b)

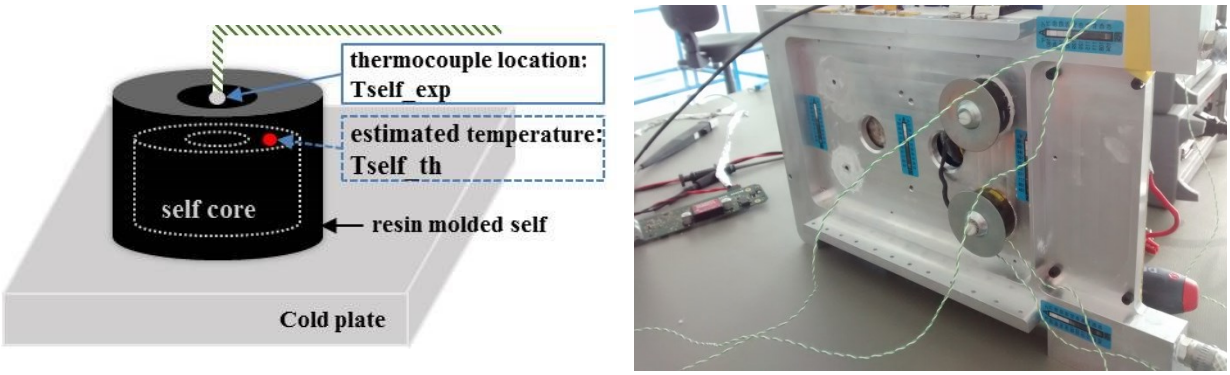
Figure 7: Prototype pictures: (a) top view with probes and thermal fiber, (b) aside view of semiconductors of switching cell #1 (at the left of the picture) and #2 (at the right of the picture)

3) Phase inductor measurements set-up

Contrary to the semiconductors, the phase inductor losses measurement could not simply be obtained with thermal measurements. Indeed, the thermal calibration of the losses would have required a specific sinusoidal power generator to create the required core and copper losses linked to the inductor temperature. But even so, the results would not have been very precise, since the inductor external temperature of the core depends of the losses repartition inside the device, due to the 2D-thermal behavior presented in previous chapter. The losses in normal operation are different from the ones generated by a sinewave, so the thermal measurement would not be so helpful.

Therefore the inductor losses have been electrically measured thanks to THDPO200 differential voltage probe and TCP0030 current probe despite the large measurement errors. The temperature of the inductor has however been measured, just to obtain a qualitative evaluation of the losses (a temperature increase corresponds to higher losses).

For material safety reasons, the thermocouple has been glued on the internal top side of the molded inductor of the phase #2 (Figure *8*). Then thermal fiber has also been put all around the inductors to avoid convection. This means that the measured temperature location will be different from the estimated temperature location which conducts to a difference on the temperature values. Finally, the measurements set-up of the inductors allow keeping the converter prototype close to the application with the drawback of lower accuracy: only the trends and order of magnitude could be verified.



(a) (b)

Figure *8*: Inductor external temperature measurement, (a) schematic, (b) picture

III. EXPERIMENTAL RESULTS COMPARED TO THEORETICAL DATA

A. Introduction

The following experiments have two objectives. First, it is about checking that all sensitive phenomena have been well understood and that the associated analytical models are able to properly quantify these phenomena.

Second, the various assumptions made, especially for semiconductor losses will be verified:

- Due to oscillations during discontinuous conduction, the MOSFET voltage at turn on is not known, and the average value (Vhigh-Vlow) has been considered.
- The equations Eq. 4 to Eq. 6 from Chapter 6 will be used to estimate the SiC Schottky diode switching losses due to hysteresis
- the parasitic elements of the switching cell are supposed to be Ld = 20 nH, Ls = 5 nH and C_L = 46.8 pF, based on the MOSFET C2M0080120D manufacturer switching losses test circuit identification from chapter 4. The impact of this inaccuracy will be checked.

B. Comparison of experiments to the analytical models before their simplifications

The values of the parasitic elements for the analytical model are the following ones: Ld_2 = 25 nH, Ls_2 = 5 nH and C_{L2} = 72 pF. The MOSFET #2 drain-source switched voltage at turn ON is systematically measured during the experiments (for instance measured Vds_turn_ON = 620 V on Figure *9*). These parameters are used in the analytical losses model.

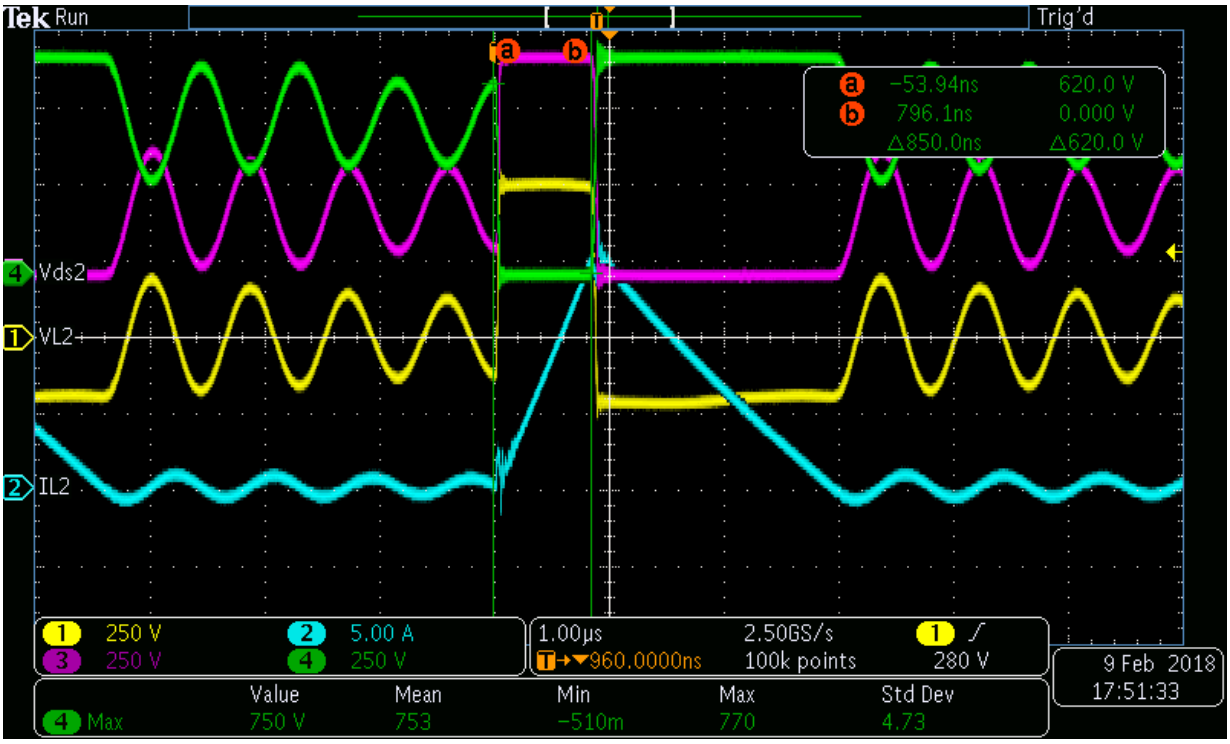
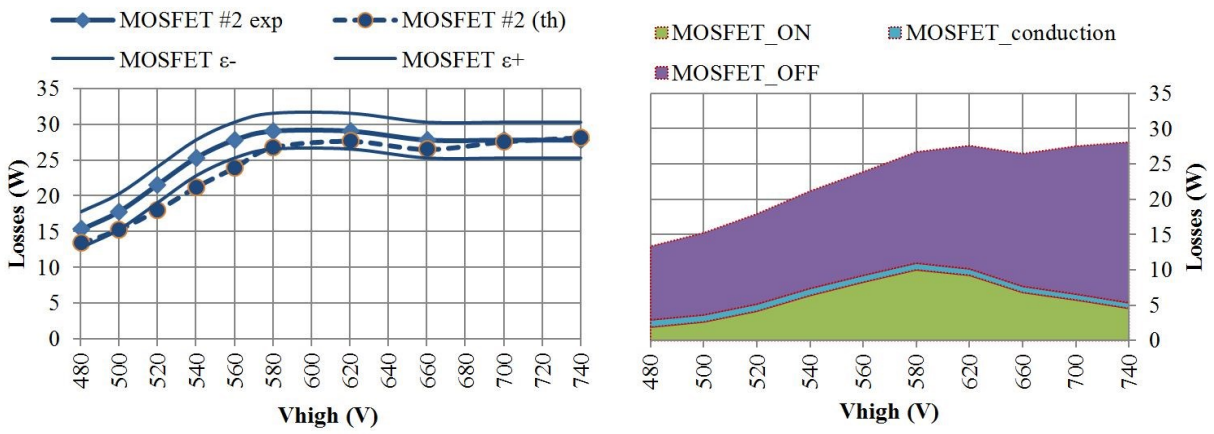


Figure *9*: Oscilloscope screen-shot. Prototype working at 700-200V 2187 W. Yellow trace is the phase inductor #2 voltage, the blue trace its current, the purple trace the diode reverse voltage and the green trace the MOSFET drain-source voltage

a) Input voltage sweeping

First, the input voltage (Vhigh) is swept from 480 V to 740 V thanks to the voltage power supply while the electrical load regulates the converter output voltage at 200 V. The input power converter is fixed and controlled at 3kW with the MOSFETs duty-cycles (the switching frequency is kept constant at 157 kHz).

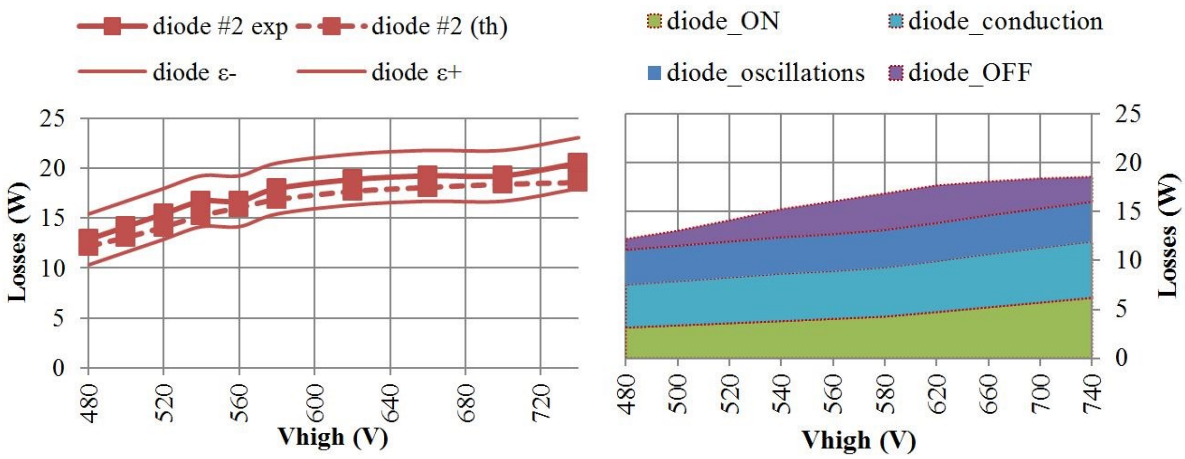
Figure *10* shows the experimental measurements of MOSFET losses compared to the analytical model: the analytical model is close to the experimental data. The global shape of the losses evolution versus input voltage sweep is well reproduced, including the "oscillation" attributed to the change in the voltage switched at turn on, due to the oscillations in discontinuous conduction. These curves show that all phenomena have been well understood and transcript in the analytical model.



(a) (b)

Figure *10*: MOSFET losses: (a) comparison between experimental measurements (measurement errors being the small lines) and analytical model, (b) MOSFET losses in each phase ratio

Figure *11* shows the experimental measurements of diode losses compared to the analytical model: the analytical model is close to the experimental data. Figure *11* (b) shows the repartition of losses in the diode, between conduction, turn ON, turn OFF and oscillations.



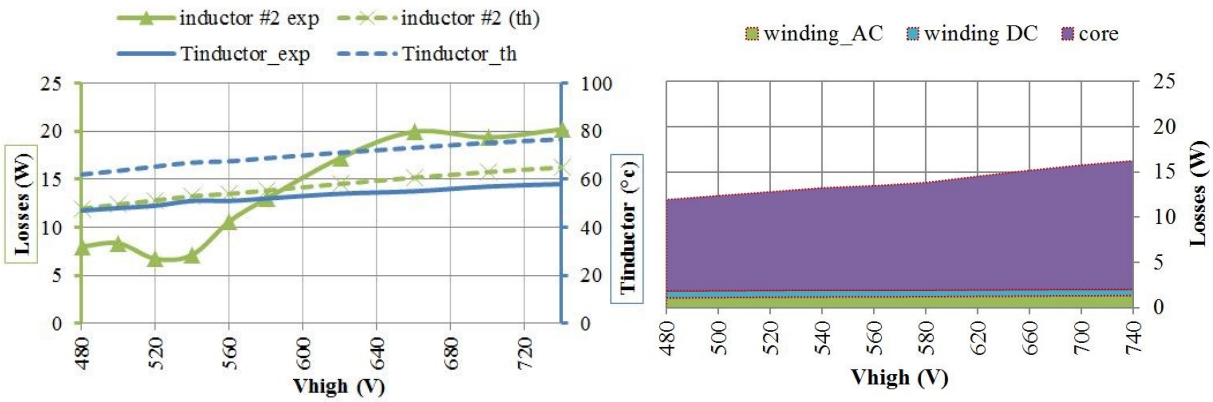
(a) (b)

Figure *11*: Diode losses: (a) comparison between experimental measurements (measurement errors being the small lines) and analytical model, (b) diode losses in each phase ratio

Figure *12* shows the experimental measurements of the phase inductor losses compared to the analytical model as well as the temperature measurements and estimation (for reminder, the location of these two temperatures is different). Unfortunately the low accuracy of the electrical measurements of the inductor losses prevents drawing any conclusion about the analytical model validity domain. The following observations can nevertheless be made:

- the order of magnitude of the measured losses is the same than the theoretical one,

- the measured temperature of the inductor on the resin is lower than the estimated temperature (between the Litz wire and the resin in the inductor): it means that at least there is not an important error on the estimation of the losses and of the thermal model,
- the global trend of the temperatures is the same. This means that the influence of the input voltage on the losses and thermal behavior of the inductor has been well understood



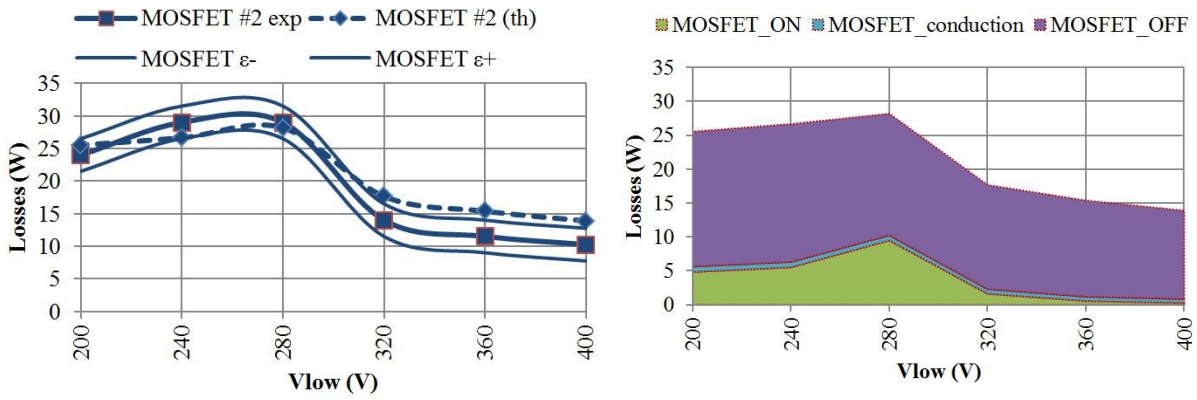
(a) (b)

Figure *12*: Phase inductor losses and temperatures: (a) comparison between experimental measurements (losses in green and temperature in blue lines) and analytical model (same colors than for the experiments but dashed lines), (b) inductor winding and core losses theoretical ratio

b) Output voltage sweeping

The output voltage (Vlow) is swept from 200 V to 400 V thanks to the voltage electrical load while the power supply regulates the converter input voltage at 700 V. As previously, the input power converter is fixed and controlled at 3kW with the MOSFETs duty-cycles.

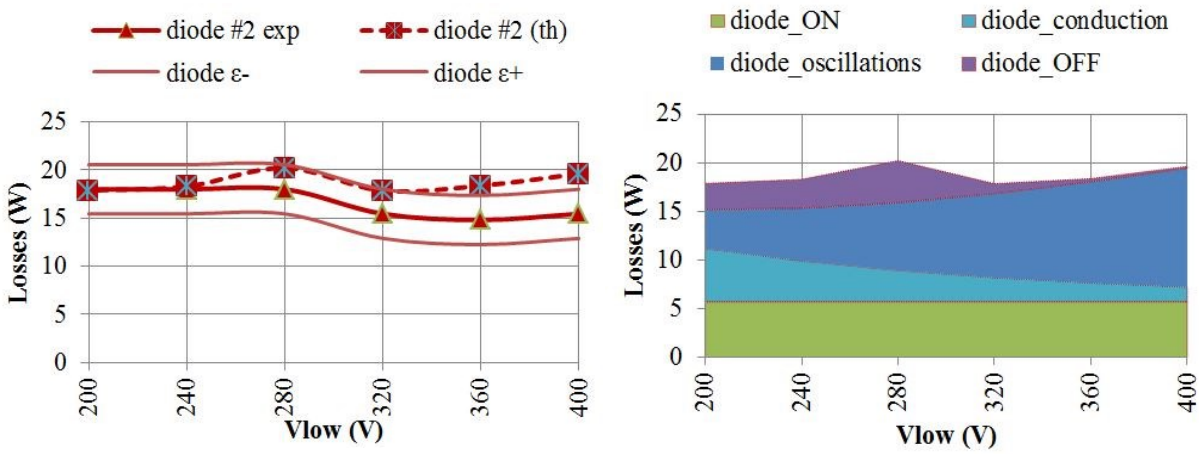
Figure *13* shows the experimental measurements of MOSFET losses compared to the analytical model which are again very similar.



(a) (b)

Figure *13*: MOSFET losses: (a) comparison between experimental measurements (measurement errors being the small lines) and analytical model, (b) MOSFET losses in each phase ratio

Figure *14* shows the experimental measurements of diode losses compared to the analytical model. If the model is similar to the measurements for low output voltage, this is not the case for higher output voltage values. This error between the measurements and the analytical model may come from the computation of the diode losses during the oscillations (the empiric formulation of the diode junction capacitance charging and discharging losses is may be not very accurate). However, the high value of the diode losses is confirmed through the damping of the oscillations on Figure *15*.



(a) (b)

Figure *14*: Diode losses: (a) comparison between experimental measurements (measurement errors being the small lines) and analytical model, (b) diode losses in each phase ratio

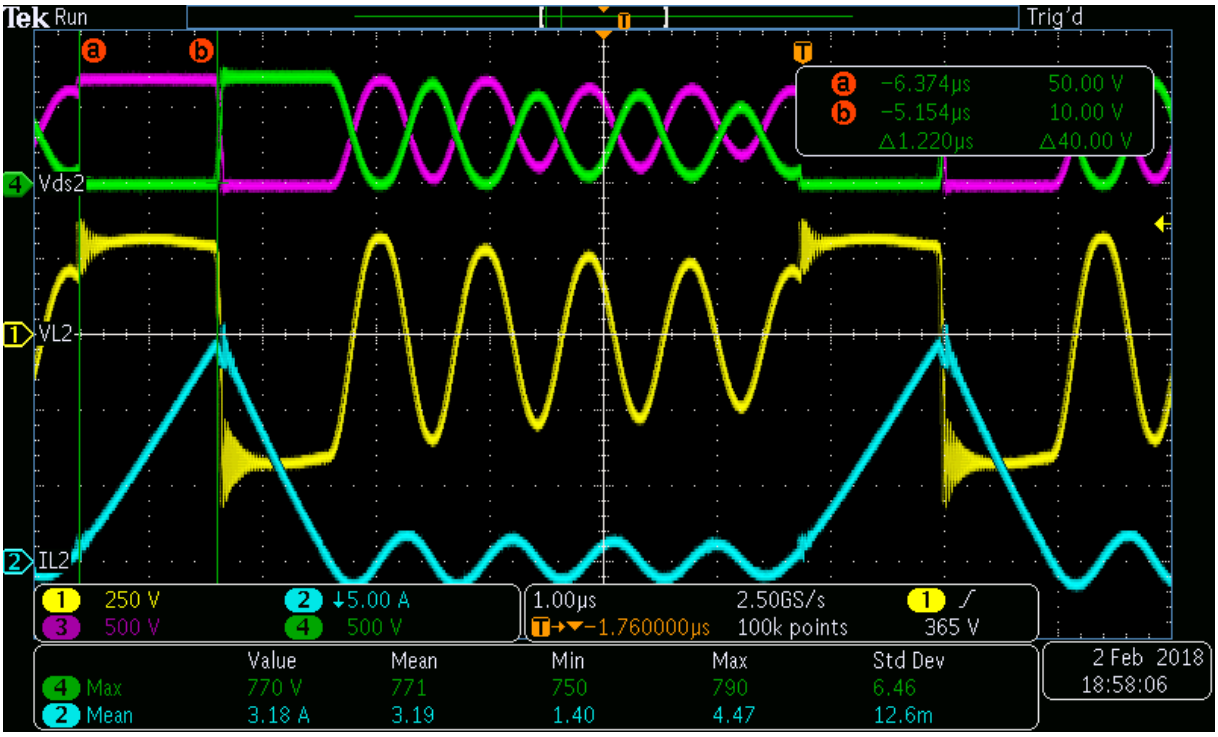
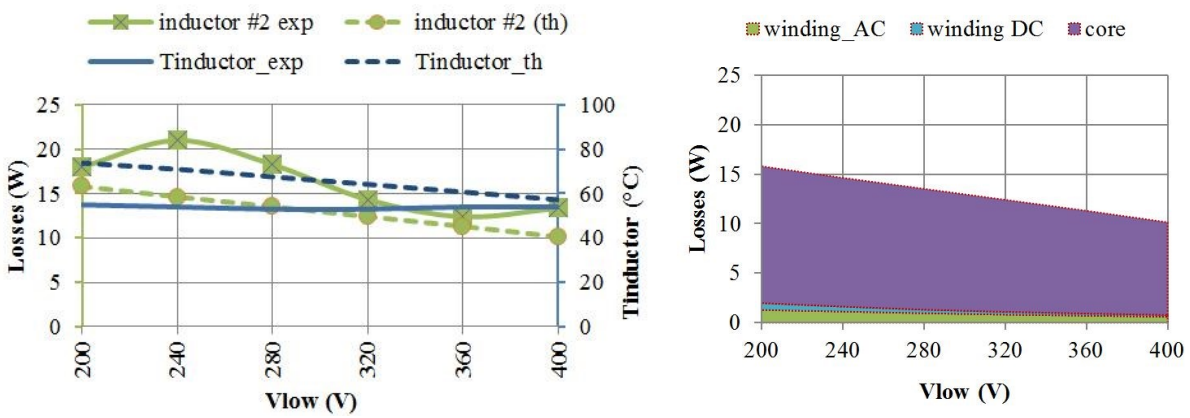


Figure *15*: 3-phase IBC oscilloscope capture at 3 kW 700 V to 400 V. Yellow trace is the phase inductor #2 voltage, the blue trace its current, the purple trace the diode #2 reverse voltage and the green trace the MOSFET #2 drain-source voltage

Figure *16* shows the experimental measurements of the phase inductor losses compared to the analytical model as well as the temperature measurements. Again, only the global trend can be confirmed, due to measurement inaccuracy.



(a) (b)

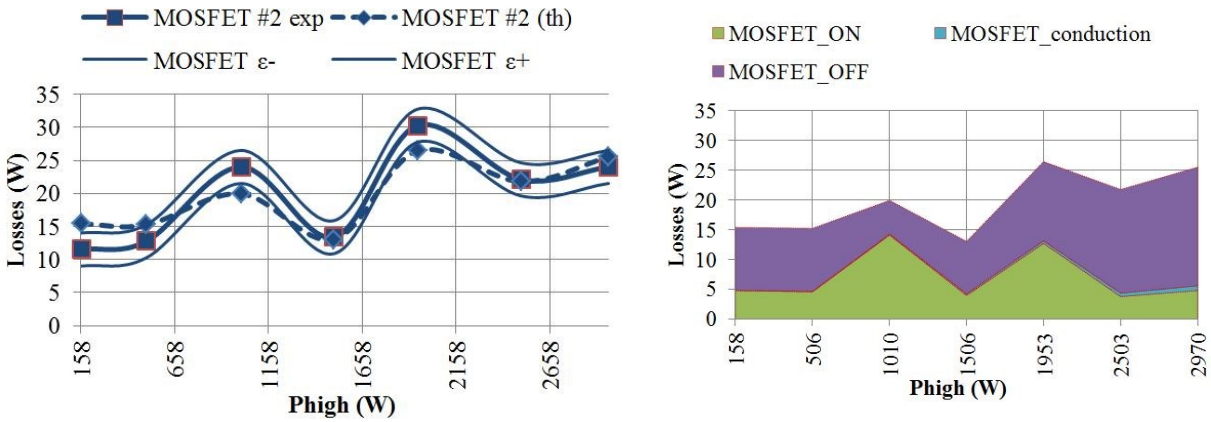
Figure *16*: Phase inductor losses and temperatures: (a) comparison between experimental measurements (measurement errors being the small lines) and analytical model, (b) inductor winding and core losses theoretical ratio

c) Input power sweeping

The input power (Phigh) is swept from 160 W to 2970 kW by changing the MOSFET duty-cycle, while the

input and output voltages are regulated thanks to the power supply and the electronic load at respectively 700 V and 200 V.

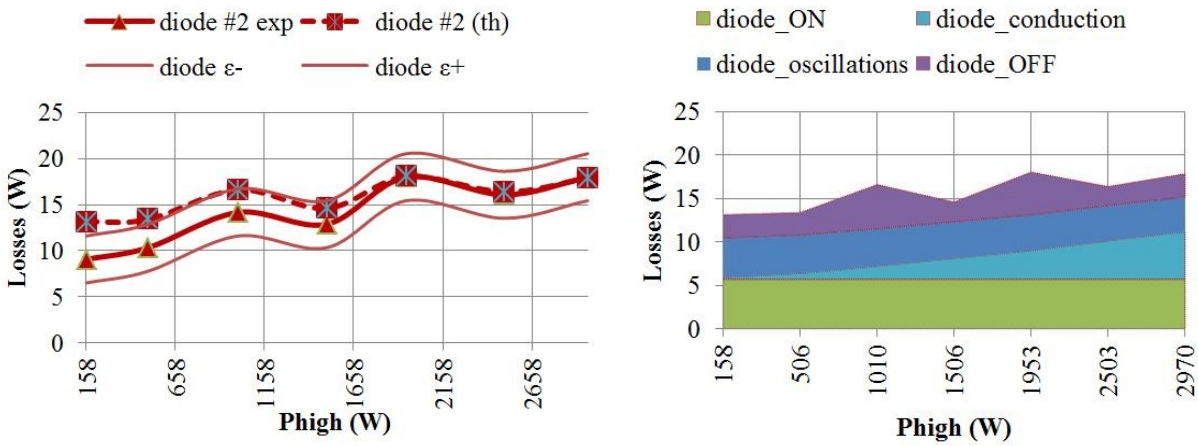
Figure *17* shows the experimental measurements of MOSFET losses compared to the analytical model (still using the measured voltage at turn on for losses evaluation): the analytical model is close to the experimental data.



(a) (b)

Figure *17*: MOSFET losses: (a) comparison between experimental measurements (measurement errors being the small lines) and analytical model, (b) MOSFET losses in each phase ratio

Figure *18* shows the experimental measurements of diode losses compared to the analytical model: the analytical model is well reproducing the losses, especially for high power.

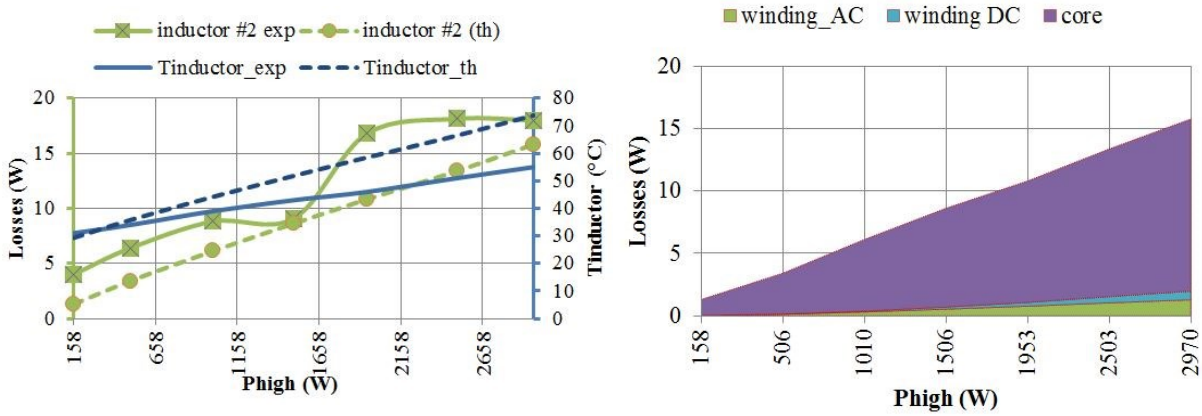


(a) (b)

Figure *18*: Diode losses: (a) comparison between experimental measurements (measurement errors being the small lines) and analytical model, (b) diode losses in each phase ratio

Figure *19* shows the experimental measurements of the phase inductor losses compared to the analytical model as well as the temperature measurements and estimation. The results are again the same order of

magnitude but no more conclusions can be made due to the low accuracy of those inductor losses electrical measurements.



(a) (b)

Figure *19*: Phase inductor losses and temperatures: (a) comparison between experimental measurements (measurement errors being the small lines) and analytical model, (b) inductor winding and core losses theoretical ratio

d) Conclusion

Based on these results, it can be concluded that the switching cell analytical losses model is relatively good. At least, almost all physical phenomena have been considered and understood. However, the MOSFET voltage at turn ON in discontinuous conduction is needed, as well as the actual values of the switching cell parasitic elements C_L, Ls and Ld.

Unfortunately, the inductor losses analytical model could not be verified. If we are confident about the trends and the order of magnitude of this model, no conclusions can be made on its accuracy. Other work in the G2ELab laboratory have been carried out on the experimental validation of inductor losses, using calorimetric measurements [1], and this can be used in the future.

C. Comparison of the experiments with the optimization models (i.e. with further assumptions)

The analytical models have been validated. It is now important to validate that the assumptions made to handle the parasitic elements do not worsen the optimization models.

That is why the following curves are given with:

- MOSFET turned ON voltage: Vswitch_ON = Vhigh – Vlow (middle case),
- Ld = 25 nH, Ls = 5 nH and C_L = 46.8 pF (based on the MOSFET C2M0080120D manufacturer

switching losses test circuit identification),

- and the diode hysteretic losses are computed with the equations Eq. 4 to Eq. 6 given in the previous chapter in which k factor is the diode capacitance Cd_2, i.e. the diode capacitance for a reverse voltage about 400 V.

Figure *20* allows comparing the optimization analytical models with the losses measurements on phase #2 of the interleaved Buck Converter. This figure shows that the optimization models are able to give the right trends of the power components losses.

It nevertheless confirms that substantial margins should be taken for the design. Indeed, as it appears on Figure *20* (a) at Vhigh = 620 V, the estimated single phase losses is about 50 W when the phase #2 measured losses due to the high value of MOSFET turn ON voltage are about 65 W. This 15 W difference is not negligible regarding the cooling of the power components.

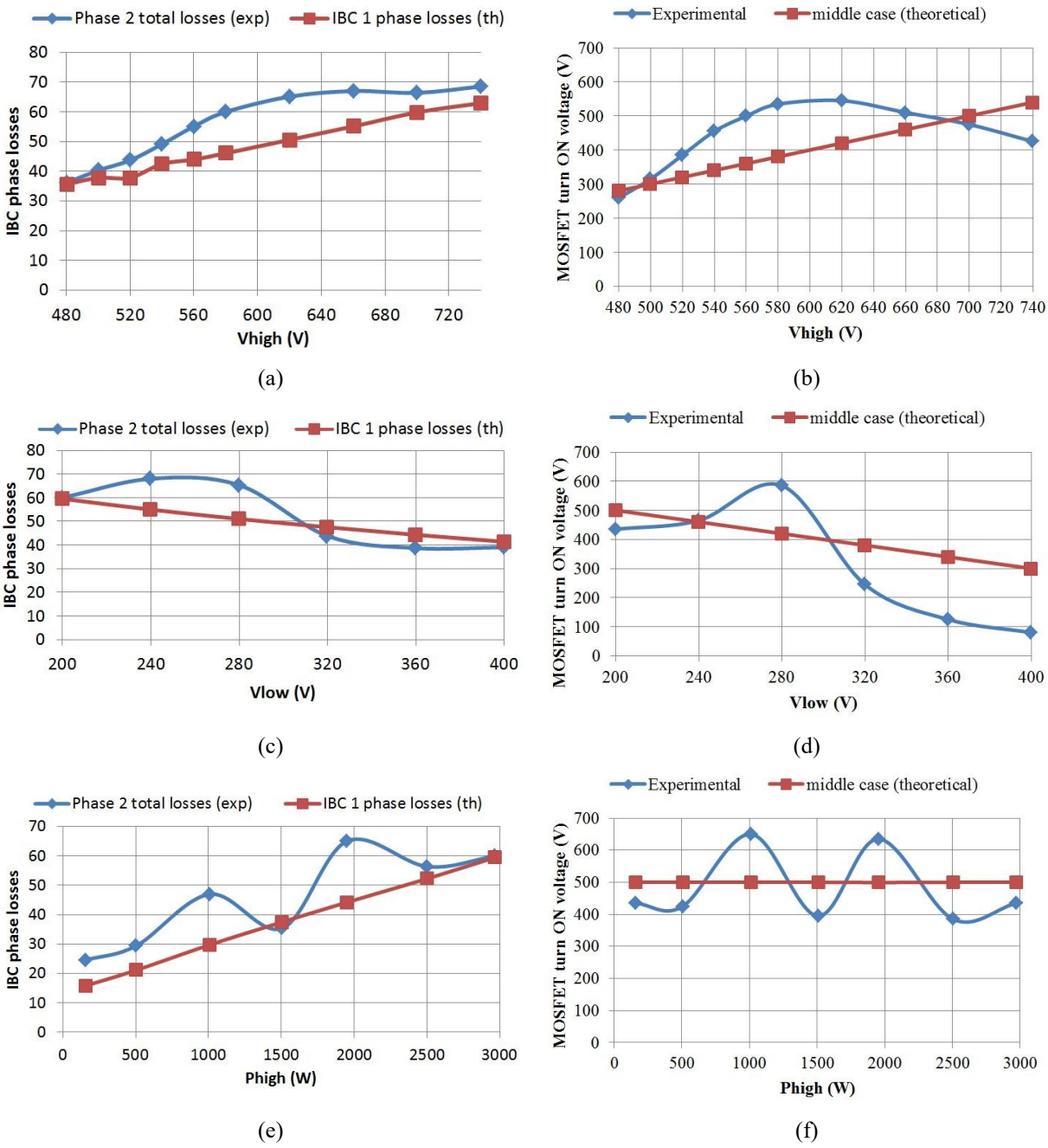


Figure *20*: Comparison between theoretical (with optimization models) and experimental data: phase losses {(a),(c),(e)} and MOSFET #2 turn ON switched voltage {(b),(d),(f)}.

Figure *21* shows the interleaved Buck converter global efficiency according to the experiments and to the optimization analytical models. The error between experimental data and the optimization models data on the efficiency is about 1%, and the trend is good when changing either Vhigh, Vlow or power transfer. The error on the calculation of the overall converter losses is lower compared to the optimization models with the losses measured on phase #2. This is normal since the optimization models are based on the bet that by averaging the N phases of the converter, the error on the overall efficiency will be small and that the converter will then not be

oversized.

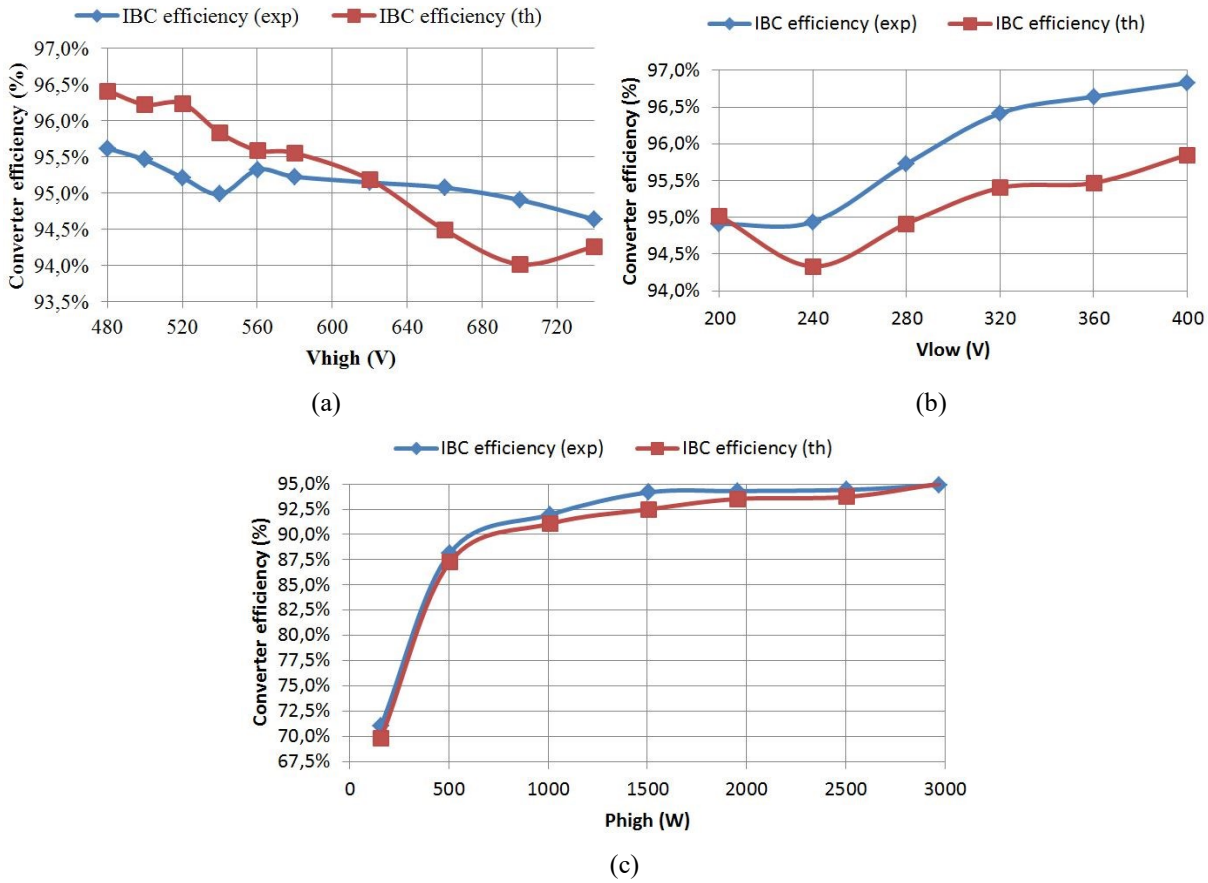


Figure *21*: Comparison of 3-phase IBC prototype measured and theoretical global efficiency, (a) input voltage sweeping, (b) output voltage sweeping and (c) input power sweeping

D. Conclusion

Considering the different necessary assumptions that had to be made for the optimization models (i.e. models for a pre-design phase where several data are unknown), the optimization analytical models are able to predict the right trends for the negotiation of the specifications. However, in discontinuous conduction mode the oscillations that appear during MOSFET and diode OFF time are hardly predictable with accuracy. Therefore, stray elements are of great importance, and must be estimated, thus reducing the accuracy of the model, but allowing a closer-to-reality optimization for the predesign step.

IV. CONCLUSION

By definition, the design is made with assumptions and models. Testing the validity domain of these models

thanks to simulation and/or experiments is necessary for the designer before negotiating the specifications (at least the trends must be equivalent).

In discontinuous conduction mode the converter suffers from a hardly predictable phenomenon that is the oscillations during MOSFET and diode turn OFF time. Two options can be considered:

1. Take the worst case for each component and oversized the all system.
2. Take the middle case for which some constraints (efficiency and devices temperatures) will not be ensure for the all range of operating.

Because the asked margins on devices temperature in aeronautical standards are high (25%), the second solution has been preferred.

Finally, the comparison between the optimization analytical models and the experimental data endorses these statements. It is worth noting that all models also apply for continuous conduction mode, and even if they have not been validated, they will provide also good results, and even better since the uncertainties due to oscillations will not apply.

V. REFERENCES

[1] A. Voldoire, J. Schanen, J.-P. Ferrieux, C. Rizet, C. Gautier, and C. Saber, "Validation of Inductor Analytical Loss Models under Saturation Conditions for PWM Inverter," in *21th European Power Electronics and Applications, in acceptance process*, 2019, vol. 2, no. 1, pp. 2–7.

Part C

Illustration of the strength of predesigning power electronics in the imaginary world

Chapter 8: Preliminary Design by Optimization of the IBC on an Initial Set of Specifications

Chapter 9: Negotiation of the Requirements

Chapter 10: Discretization Procedure to Come Back in the Real World

Chapter 8: Preliminary Design by Optimization of the IBC on an Initial Set of Specifications

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I. INTRODUCTION

In the three previous chapters, the Interleaved Buck Converter optimization models have been presented and their validity domain experimentally checked. These models are gathered as presented in Figure 7 of chapter 4 constituting the whole model of the IBC for one operating point. This global model has the property to be continuous and differentiable.

It is now time for considering optimizing the converter. The difficulty of designing a wide operating range converter will be first exposed and a solution will be proposed. Then, the optimizations will be performed with a fictive set of specifications on the IBC and the results will be analyzed. In particular, the influence of the choice of the magnetic material and of the conduction mode on the converter weight will be studied.

II. PROPOSED MODEL TO OPTIMIZE SIMULTANEOUSLY SEVERAL OPERATING POINTS

A. Problematic linked to wide operating range of the system

The optimal design of a system for a single operating point can be easily made thanks to a smart procedure. But when optimizing the same system for a wide operating range, the designer should create its design procedure including all the sizing operating points. This can be complicated since the components constraints are not the same according to the studied operating point. As it has been shown with the experiments of the prototype, the power components temperatures should be critical for the highest level of voltage conversion at maximum power. While the constraint about the conduction mode if discontinuous is for the lowest voltage conversion at maximum power.

In other words, the designer has to take advantage of his (her) expertise to define the proper sizing operating points. Despite the experience of the designer on the system, additional system-independent uncertainties can interfere with design definitions, for example if a new technology is introduced.

Thanks to the property of the optimization algorithm SQP which handles the constraint only if they are "active" (c.f. chapter 2 section III.A.), and thanks to the quickness of the optimizations it is not a real problem for the gradient-based optimization algorithm to study further operating points if the problem size is kept in the limit of the algorithm. It can manage up to 1000 input variables and output constraints. For example the computation of the outputs and of the partial derivatives of the outputs according to the inputs, in the CADES 4 software with a classical personal computer, takes indeed around one second for one operating point. And because the gradient evaluation makes the necessary number of optimization iterations pretty low (less than 50 in

this case for 10^{-3} accuracy), the optimization for one operating point lasts less than few minutes.

B. Definition of the sizing operating points based on designer expertise

1) Set of specifications for the study case

A fictive set of specifications[1] will be used for the study case of this thesis. It is summarized in Table 1.

Table 1: Interleaved Buck Converter specifications

Criteria	Minimum Value	Maximum Value	Conditions/Remarks
Power density (objective)	7 kW/kg is mandatory	10 kW/ kg nice to have	Depends on the following specifications complexity
Input power	0 W	5 kW	For the entire of input/output voltage ranges (at this point of project starting)
Input voltage	450 V	800 V	For a power range [0 ; 5] kW
Output voltage	200 V	400 V	For a power range [0 ; 5] kW
Efficiency	96 %	NA	at 5 kW
Efficiency at a third of full load	90 %		at 1.7 kW
Input/Output current THD	NA	5 %	For a power range [1.7 ; 5] kW
Cooling temperature	-40 °C	65 °C	For a power range [0 ; 5] kW
Conduction mode	NA	NA	Must be the same for a power range [1.7 ; 5] kW

The requirements for this converter are especially difficult to comply with: wide input and output voltages, wide input power range with high efficiency requirements, very high power density. This is because in the preliminary phase, PV technology is still uncertain and the system integrator has to specify some margin to take into account PV technology evolutions.

As mentioned in chapter 3, the conduction mode of the IBC could not be defined with qualitative criteria. The only condition for a good control of the converter is that the conduction mode stays the same for a wide operating range. In this chapter, the acronyms CCM and DCM will indicates respectively continuous and discontinuous conduction modes.

[1] The actual requirements are not provided in this thesis for confidentiality reasons. However, they exhibit similar complexity as in reality.

2) Sizing operating points of the IBC with these fictive specifications

The possible sizing operating points of the IBC for this set of specifications is presented in Table *2* with the supposed limiting (active) constraints.

Table *2*: Sizing operating points of the IBC

Operating point number	Input voltage (Vhigh) [V]	Output voltage (Vlow) [V]	Input power (Phigh) [W]	Cooling plate temperature (Tcooling) [°C]	Concerned conduction mode	Possible limiting constraints
# 1	800	200	5000	65	Both	IBC efficiency, power components temperature, current density in the phase inductor and output filtering components
# 2	800	200	5000	-40	Both	IBC efficiency due to diode on state resistance?
# 3	800	200	1700	65	Both	input and output current THD, efficiency
# 4	450	400	5000	65	DCM	conduction mode, maximum input DC current in filtering inductors
#5	450	200	1700	65	CCM	conduction mode, maximum input DC current in filtering inductors
# 6	800	400	5000	65	CCM	phase inductor temperature

Finally we suppose that there are six sizing operating points to study for the optimizations. These hypothesis will be confirmed or not in the next section.

C. Optimization model of the IBC for Stratobus HVPCU handling several operating points

In this study case, the operating point model is generic (i.e. is fully independent). The optimization model to design the system for several operating points is set as shown in Figure *1*. The global input design parameters are:

- the selected components: semiconductors current ratings, filtering capacitor and inductor values and numbers, phase inductor geometries, etc.,
- the number of phase and the switching frequency.

There are however design variables dedicated to the studied operating point which are the implicit constraints:

- the MOSFET and diode estimated junction temperatures,
- the inductor core estimated temperature
- and the IBC estimated efficiency.

These estimated data are indeed needed to determine the thermal sensitive electrical properties of the

components and the converter output current. The algorithm must check that the estimated data is closed to the computed one during the iteration: that is an operating point implicit constraint (see chapter 4 section V.B.2).

In the aim to limit the computation time, the global output variables (that are the components weight or nominal properties) are called with an only one operating point model (OP #1). This allows to limit the size of the output matrix and so the simple and the differentiation computations times. It should be noticed that a model dedicated to the computation of these variables could have been set up instead of makink the computation in each operating point model: then the operating point model would not have been independent anymore).

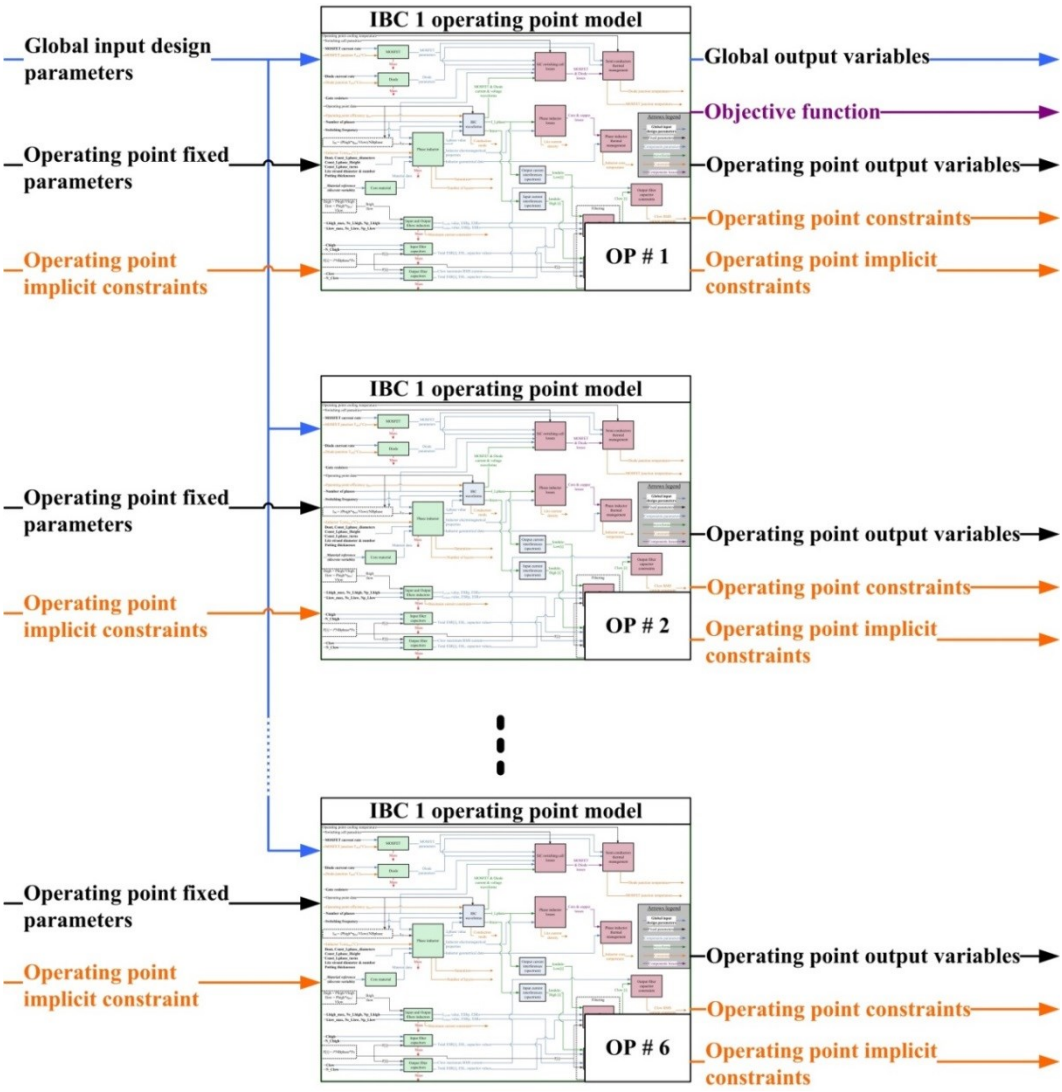

Figure *1*: IBC 6 operating points optimization model

III. OPTIMIZATIONS OF THE IBC TO DEFINE THE BEST TOPOLOGIES AND TECHNOLOGIES

A. Detailed set of specifications of the optimization model

Table 3 shows the input variables bounds for the optimizations under the set of specifications. The initial value of the input design variables is necessary for a gradient based optimization algorithm as SQP. This initial point can be defined in two ways: either the result of a manual pre-design is taken as initial point of the optimization; or several starting points are chosen randomly (by using a mixed of genetic algorithm with SQP algorithm). The first solution is preferred to better handle the optimization problem. Here, the prototype data are taken as the initial point despite the maximum power is different (but the initial number of IBC phases is taken as 4 instead of 3).

Table 3: Specifications of the input variables of the optimization model

Variable name	legend	unit	type	initial value	minimum value	maximum value
Input filter variables						
Lfilter_val_max_high	Nominal value (for no current) of the filtering single inductor	H	interval	2.7E-6	5.6E-7	4.7E-5
Nis_high	Number of inductors in series configuration	-	interval	2.0	1.0	5.0
Nip_high	Number of inductors in parallel configuration	-	interval	2	1.0	5.0
Cer_high	Capacitor value between 5.6nF and 0.39µF	nF	interval	170.0	5.6	390.0
N_Cer_high	number of capacitors put in parallel	-	interval	3	1.0	10.0
Output filter variables						
Lfilter_val_max_low	Nominal value (for no current) of the filtering single inductor	H	interval	1.0E-6	5.6E-7	4.7E-5
Nis_low	Number of inductors in series configuration	-	interval	2.0	1.0	5.0
Nip_low	Number of inductors in parallel configuration	-	interval	2.0	1.0	5.0
CFilm_low	Capacitor value between 6.8nF and 3.9µF	nF	interval	240	68	3900
N_Film_low	Number of capacitors put in parallel	-	interval	3	1.0	10.0
Converter global parameters						
Nphase	Buck Interleaved phases number	-	interval	4	1.0	8.0
Fs	Buck Interleaved phases switching frequency	Hz	interval	157000.0	20000.0	250000.0
Converter phase inductor						
Material¤	*Phase inductor material index*	-	*fixed*¤	*326*		
const_Lphase_Diameters	Proportional coefficients for Buck cores geometry. Extrapolation from Datasheet : should be [0.4 0.7]	-	interval	0.7	0.4	0.7
Lphase_Dout	External Buck inductance diameter	m	interval	0.05	0.01	0.05
const_Lphase_Height	Proportional coefficients for Buck cores geometry. Extrapolation from Datasheet : should be [0.75 1.0]	-	interval	1.0	0.75	1.0
const_Lphase_turns	Turns number coefficient: should be [0.9 1] to keep thermal model valid	-	interval	1.0	0.9	1.0

nstrandLphase	Number of strands of the Litz wire of the IBC phase inductor : [20 , 900]	-	interval	437.0	20.0	900.0
resine_density	*Weight density of the resin*	*kg/m³*	*fixed*	*2000.0*		
EresineTopLphase	Thickness of the resin at the top of the inductor	m	interval	0.001	0.001	0.01
EresineExtLphase	Thickness of the resin at the external side of the inductor	m	interval	0.001	0.001	0.01
EresineIntLphase	Thickness of the resin at the internal side of the inductor	m	interval	0.001	0.001	0.01
Vdielec_min	*Minimum value of the dielectric voltage to hold*	*kV*	*fixed*	*10.0*		
DlitzLphase	Litz strand diameter	m	interval	8.7E-5	7.5E-5	2.0E-4
TotalConnectionLenght	*Total Litz connection length: for the both terminations*	*m*	*fixed*	*0.2*		
Switching cell variables						
cal_Imos	MOSFET current rating at 25degC (from 10 to 90 A)	A	interval	65.0	10.0	90.0
cal_Idiode	Diode current rating at 25degC (from 5 to 113 A)	A	interval	30.0	5.0	60.0
Rg_ext	External Gate resistor	Ohm	interval	2.5	2.5	15.0
Vdr_L	*Vdriver low*	*V*	*fixed*	*-5.0*		
Vdr_H	*Vdriver high*	*V*	*fixed*	*20.0*		
Ls	*Source global inductance*	*H*	*fixed*	*5.0E-9*		
Ld	*Drain global inductance*	*H*	*fixed*	*2.5E-8*		
CL	*IBC phase inductor parasitic capacitance*	*F*	*fixed*	*4.2E-11*		
Converter operating point #X variables						
desired_efficiency_X	Desired efficiency at the input of the model : should be the same or almost the same than the future computed one	-	interval	0.96	0.96	0.999
desired_Tj_diode_X	Diode junction temperature	degC	interval	80.0	65.0*	110.0
desired_Tj_mos_X	MOSFET junction temperature	degC	interval	85.0	65.0*	110.0
desired_TLphase_X	Estimated temperature of the phase inductor core	degC	interval	95.0	65.0*	150.0

**The minimum authorized value for the components temperature of the operating point #X must be the temperature of the cooling plate of the studied operating point. In other word, 65 °C for operating points #1, #3, #4, #5 and #6 and -40°C for operating point #2.*

¤ *The phase inductor core material is the only one discrete design variable of the converter: must be fixed during the optimization*

As it appears in Table 3, the design variable range value is quite wide: for example, the switching frequency can be swept from 20 kHz to 250 kHz. The algorithm is able to handle wide range of parameter values, but the designer must pay attention to the validity domain of the optimization models by setting realistic minimum and maximum values. In the opposite, the model can consider a too wide range of parameters for the dedicated application (for example with diode current rating limited to 60 A in the optimization).

There are finally 24 optimization input variables in this study case and 6 (i.e. number of studied operating points) times 4 implicit equations to handle (i.e. the input variables as “desired” efficiency and components temperature).

Table 4 shows the specifications of the output variables.

Table 4: Specifications of the output variables of the optimization model

Variable name	legend	unit	minimum value	maximum value
filter_high				
const_Fr_high	Constraint on the input filter resonance frequency const_Fr_high = 0.9*Fs-Fr_high has to be >0	Hz	0.0	250000.0
Const_N_Cer_high	Constraint on the number of filtering capacitors at high side: has to be >0	-	0.0	20.0
filter_low				
const_Fr_low	Constraint on the output filter resonance frequency: const_Fc_low = 0.9*Fs-Fr_low has to be >0	Hz	0.0	250000.0
Const_N_Film_low	Constraint on the number of filtering capacitors at low side: has to be >0	-	0.0	15.0
globalParam				
IBC_weight	IBC estimated weight without measurement and control components	kg	minimize	
OP_X_Buck (Output variables from operating point #X)				
cont_eff_X	Constraint on efficiency : should be close to zero	-	-0.001	0.001
Cont_Tj_diode_X	Constraint on the implicit equation of the diode junction temperature : should be close to zero	degC	-1.0	1.0
Cont_Tj_mos_X	Constraint on the implicit equation of the MOSFET junction temperature : should be close to zero	degC	-1.0	1.0
Cont_TLphase_X	Constraint on the implicit equation of the IBC phase inductor core temperature: should be close to zero	degC	-1.0	1.0
Cont_conduction_X	Constraint on the conduction mode : if > 0 = CCM ; if < 0 = DCM	H	-0.001[#]	-5.0e-7[#]
THD_Ihigh_X	Total harmonics distortion of input IBC current	%	0.0	5.0
THD_Ilow_X	Total harmonics distortion of output IBC current	%	0.0	5.0
OP_X_filtering_high				
const_Idc_Lfilter_high_X	Constraint on the filter inductors maximum current : has to be >0	A	0.0	50.0
OP_X_filtering_low				
const_Idc_Lfilter_low_X	Constraint on the filter inductors maximum current : has to be >0	A	0.0	50.0
Cont_I_Clow_film_rms_X	Constraint on film capacitors RMS current: has to be <0	A	-50.0	0.0
OP_X_mosfet_diode				
Vmiller2_OFF_X	Miller voltage at MOSFET turn OFF	V	0.0	16.0
OP_X_phaseInductor				
Lphase_saturation_constraints_X	Saturation criterion	%	80.0	105.0
JlitzLphase_X	Litz wire density current in the Buck phase inductor	A/mm²	0.0	5.0

[#]For discontinuous conduction mode only. The values in continuous conduction mode are : minimum value = 5.0e-7 and maximum value = 1.0e-3

Some of these constraints are intrinsic ones (constraint on the conduction mode for instance), and some are set to force the optimization algorithm to stay in the limits of the optimization models validity domain. It is the case for the variables named “Vmiller2_OFF_X” which corresponds to the miller voltage of the MOSFET at turn OFF. It is constraint to be lower than 16V: if it is higher, it would means that the switched current is very high compared to the MOSFET selected current rating (Eq. 1) and that the design is out of the limits of the validity domain of the switching cell losses model.

$$Vmiller2_{OFF} \propto \frac{Iswitch_{OFF}}{gfs} \qquad Eq.\ 1$$

With $Vmiller2_{OFF}$ the miller voltage at turn OFF, gfs the selected MOSFET transconductance and $Iswitch_{OFF}$ the switched current at MOSFET turn OFF.

The filters resonance frequency is forced to be lower than 90% of the IBC phases switching frequency. Indeed, the frequency models described in Chapter 5 do not take into account the parasitic elements of the switching cell. The oscillations occurring in discontinuous conduction mode at different frequencies for each phase create disturbances at the switching frequency. It is preferable to limit the noise level at this frequency. It also means that the optimal solution should be checked thanks to a time simulation considering the parasitic elements before prototyping. The number of filtering capacitors is constraint to be equal or higher than the IBC number of phases in the aim to reduce the switching cell parasitic inductance by putting a capacitor as close as possible.

As it appears in this Table 4, the implicit equations of the optimization problem are constraint to be near zero. There are no needs to constraint also the direct value of the variable such as the efficiency or components temperature since they are set as input optimization variables that the optimization algorithm cannot exceed the limits. In other words, the components temperatures and the converter efficiency are indirectly constrained.

There are finally one objective function (components weight to minimize), 4 global constraints and 13 constraints per studied operating points: 82 constraints in total that the optimization algorithm must check.

B. Optimization procedure

Before negotiating the set of specifications with the system integrator, it is essential to identify the critical properties of the converter. Some optimizations are performed on the first set of specifications to understand what would be the limits, which technologies could be improved, etc.

1) Procedure to determine the sizing operating points

In the following, first the sizing operating points will be verified. The technic consists into optimizing the converter with the constraints first set on only one operating point and to observe the objective function value. Then, the second operating point is added to the optimization and again the objective function value is observed. If the result is the same than for the first optimization, it means that the second operating point is not a sizing one. On the contrary, if the objective function has been degraded then the operating point is sizing. The designer performs this procedure (that we will call “sizing operating points study”) until all estimated sizing operating points have been optimized.

2) Procedure to define the best technologies for a dedicated set of specifications

Once the real sizing operating points have been found for a dedicated technology and/or topology, the designer can look for the better combination of its technology and/or topology for the initial set of specification. In this study case, we will look for the best conduction mode and phase inductor core material. It will also be good to study the influence of these discrete parameters on the converter weight. For this purpose, 11 core materials are examined (listed in Table 5).

Table 5: phase inductor core materials to study

Material	**Composition**	**Properties according to the manufacturer [1]**	**Studied permeabilities**
Kool Mu	FeSiAl	moderate cost and has significantly lower losses and substantially better thermal properties when compared to powdered iron cores	26 ; 40 ; 60 ; 75 ; 90 ; 125
Kool Mu Max (new)	FeSiAl	combination of high DC bias and low core loss density: solution for high efficiency, high power inductors	26 ; 60
MPP	FeNiMo	lowest inductor losses (but most expensive)	26 ; 60 ; 125

C. Analysis of the optimizations performed in the imaginary world

All the following optimizations will be performed with the gradient based optimization algorithm SQP with 5.0e-4 accuracy in CADES 4.0.14.beta software. It means that all of the following optimizations are performed in the imaginary world with continuous design variables.

1) Sizing operating points study

a) Study in discontinuous conduction mode

Table 6 gives the optimization results of the sizing operating point study of the IBC in DCM. The inductor material for this study is the Kool Mu with a permeability of 26 (i.e. same as the prototype). The operating point number description is given in Table *2* and the limiting constraint legend in Table 3 and Table 4.

Table 6: Optimization results of the sizing operating point study of the IBC in DCM

Optimized operating points	**Number of iterations**	**Optimization time (s)**	**IBC electronic weight (gr)**	**Fs (kHz)**	**number of phases**	**Inductor value (µH)**	**limiting constraints**
#1	8	50	476,5	241	2,45	31,1	efficiency_1, Tj_diode_1, Jlitz_1, THD_1, conduction_1
#1 & #2	8	70	476,5	240	2,45	31,1	efficiency_1, Tj_diode_1, Jlitz_1, THD_1, THD_2, conduction_2
#1;#2 & **#3**	8	115	477	240	2,46	31,1	efficiency_1, Tj_diode_1, Jlitz_1, THD_3, conduction_2
#1;#2;#3 & **#4**	7	30	515	164	2,54	26,5	efficiency_1, Tj_diode_1, Jlitz_1, THD_3, conduction_4
#1;#2;#3; #4 & #5	7	31	515	164	2,54	26,5	efficiency_1, Tj_diode_1, Jlitz_1, THD_3, conduction_4
#1;#2;#3; #4;#5 & #6	13	101	515	164	2,54	26,5	efficiency_1, Tj_diode_1, Jlitz_1, THD_3, conduction_4

As it appears in this table, there is no difference on the objective function (the weight to minimize) when adding the operating point #2 constraints in the optimization: apparently, the diode on state resistance sensitivity to the junction temperature does not impact so much the converter global efficiency when the cooling plate temperature is about -40°C. In contrary to the constraint on the total harmonic distortion of input and output currents for the operating point #3, i.e. for the higher voltage conversion at a third of maximum power. The operating point #4 is also very important to consider since the phase inductor value must be sufficiently lower than the critical value to stay in discontinuous conduction mode. As anticipated, the operating points #4 and #5 are not sizing ones in discontinuous conduction mode.

Finally the sizing operating points are the #1, #3 and #4.

b) Study in continuous conduction mode

Table 7 gives the optimization results of the sizing operating point study of the IBC in CCM. The phase inductor material for this study is the Kool Mu with a permeability of 60 (higher than for the optimizations in DCM since continuous conduction mode needs higher permeability for higher inductance).

Table 7: Optimization results of the sizing operating point study of the IBC in CCM

Optimized operating points	**Number of iterations**	**Optimization time (s)**	**IBC electronic weight (gr)**	**Fs (kHz)**	**number of phases**	**Inductor value (µH)**	**limiting constraints**
#1	18	225	399	202	2,37	44,7	saturation_1, Jlitz_1, efficiency_1, Tj_mos_1, THD_1
#1 & #2	18	361	399	202	2,37	44,7	saturation_1, Jlitz_1, efficiency_1, Tj_mos_1, THD_1
#1;#2 & **#3**	14	174	531	250	2,6	87,5	saturation_1, Jlitz_1, efficiency_1, Tj_diode_1, Tself_1, THD_3, condcution_3
#1;#2;#3 & **#4**	7	123	534	250	2,6	87,4	saturation_1, Jlitz_1, efficiency_1, Tj_diode_1, Tj_mos_1, THD_3, conduction_3, I_DC_Litz_4
#1;#2;#3; #4 & #5	7	45	534	250	2,6	87,3	saturation_1, Jlitz_1, efficiency_1, Tj_diode_1, Tj_mos_1, THD_3, conduction_3
#1;#2;#3; #4;#5 & **#6**	16	205	534	250	2,6	87,5	saturation_1, Jlitz_1, efficiency_1, Tj_diode_1, Tj_mos_1, THD_3, conduction_3. *Note: phase inductor temperature high for operating point #6 (123 °C) than for #1 (102 °C).*

Based on these results, the sizing operating points in continuous conduction mode are the #1, #3 and #4. The operating point #6 will also be considered in the future optimizations with other inductor core material because of the risk for these materials to push the boundary of the inductor core maximal temperature.

2) Phase inductor core materials influence study

From now, the optimizations will be performed on the deduced sizing operating points, in other words on the #1, #3 and #4 for the IBC in DCM and on the #1, #3, #4 and #6 for the IBC in CCM. All the previously studied operating points could have been kept for the following optimizations. But the optimization time and the computer temporary memory fill rate would have been higher than necessary.

a) Study in discontinuous conduction mode

Table 8 gives the optimization results for the converter in DCM with different inductor core materials.

Table 8: Optimization results of the sizing operating point study of the IBC in DCM

Material	Permeability	Solution?	Number of iterations	IBC electronic weight (gr)	Fs (kHz)	number of phases	Inductor value (µH)	limiting constraints
Kool Mu	26	✓	7	515	164	2.5	26.5	efficiency_1, Tj_diode_1, Jlitz_1, THD_3, conduction_4
	40	✓	10	511	127	2.7	35	efficiency_1, Tself_1, Jlitz_1, THD_3, conduction_4
	60	✓	20	483	122	3.1	40.4	efficiency_1, Tself_1, Jlitz_1, THD_3, conduction_4
	75	✓	9	528	104	3.6	52.6	efficiency_1, saturation_1, Tself_1, Jlitz_1, THD_3, conduction_4
	90	✓	19	673	68	4	68	efficiency_1, saturation_1, Tself_1, Jlitz_1, THD_3, conduction_4
	125	✗						
MPP	26	✓	43	566	168	2.5	26.5	efficiency_1, Tj_diode_1, Jlitz_1, THD_3, conduction_4
	60	✓	**10**	**439**	**164**	**3.2**	**33.6**	efficiency_1, Tself _1, Jlitz_1, THD_3, conduction_4
	125	✗						
Kool Mu Max	26	✓	5	467	203	2.5	21.7	efficiency_1, Tj_diode_1, Jlitz_1, THD_3, conduction_4
	60	✓	**11**	**441**	**152**	**3.2**	36	efficiency_1, Tself_1, Jlitz_1, THD_3, conduction_4

All the results will not be analyzed in details. But it is interesting to understand the operation of the SQP algorithm with the optimization of the IBC with MPP 26µ material. For this material, there were 5 limiting constraints and of course one objective function. The evolution of these parameters during the optimization as well as the input global parameters (the switching frequency Fs, the IBC number of phases Nphases and the Litz wire strand diameter DlitzLphase) are presented in Figure *2* (legend of the variables in Table 3 and Table 4).

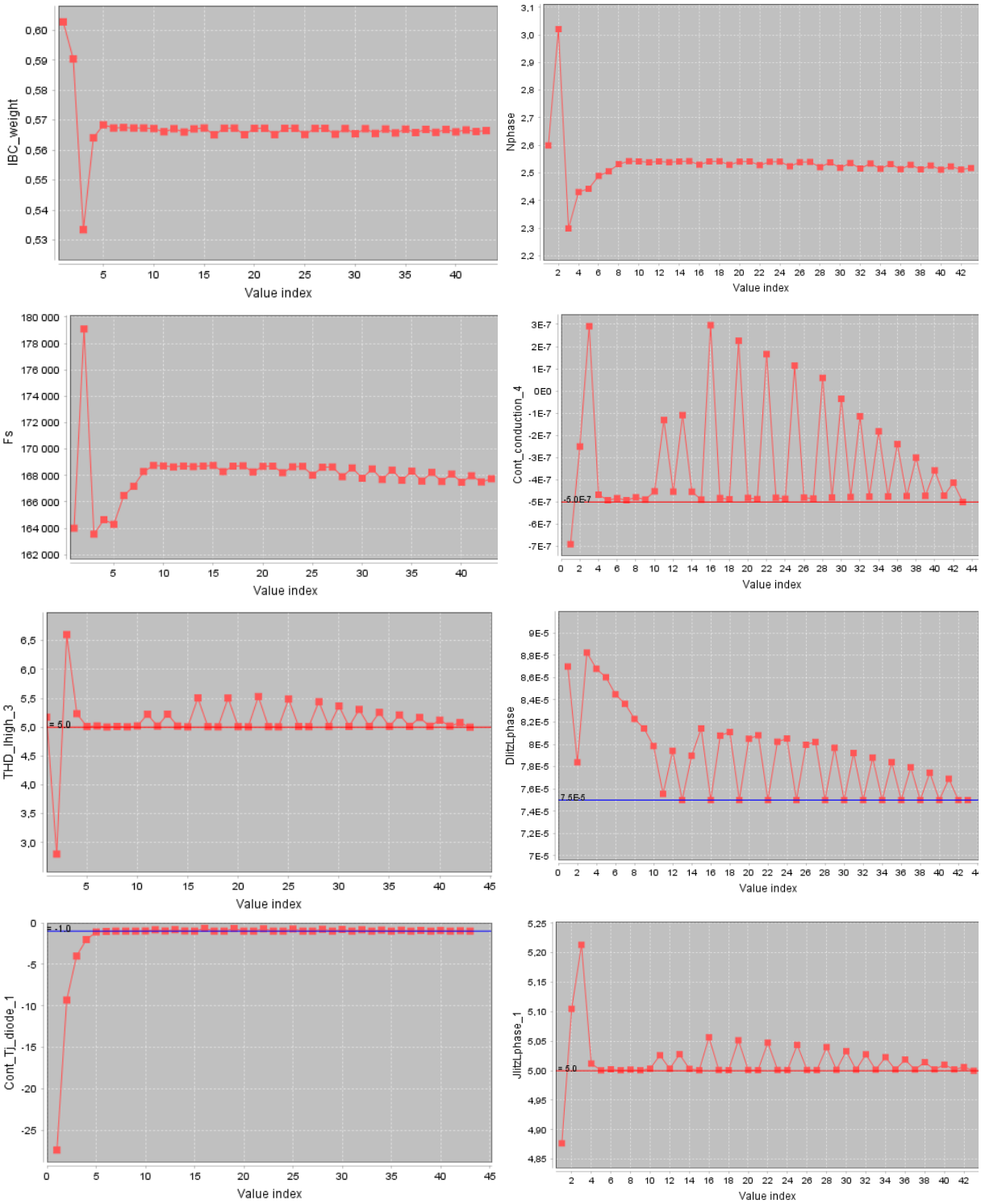

Figure 2: Optimization of the IBC in DCM with MPP 26µ material on the initial set of specifications

Only a few of the design variables have been traced, but this figure shows the important correlation between each variable of the converter. For example, the constraint on the conduction mode for the operating point #4 in related to the constraint of current density in the inductor winding at operating point #1. The oscillations on the input variable that is the switching frequency of the converter impact the diode maximum junction temperature,

etc.

Besides the strength on the gradient based optimization algorithm is easily visible since the constraints are rapidly fulfilled (with a quadratic behavior). It should be noticed that if the algorithm accuracy would have been set at 1.0e-3 instead of 5.0e-4, the optimization would have probably stopped at the iteration number 15 despite the unfulfilled constraint on the conduction mode (see Figure *3*).

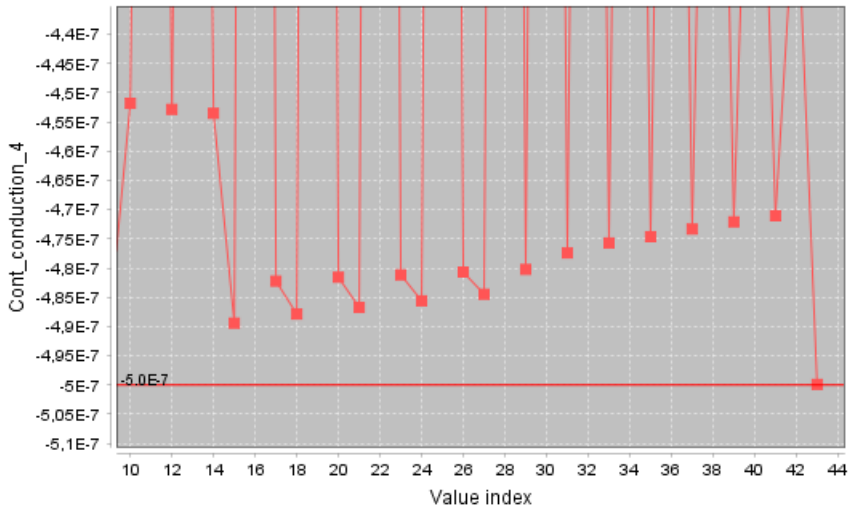

Figure *3*: Zoom in the trace of the conduction constraint of operating point #4: must be below -5.0E-7

Finally, the better material for this initial set of specifications is the MPP with a 60µ permeability with a power density in the imaginary world of 11.4 kW/kg considering only the electronic weight (i.e. without cooling and input and output connectors).

b) Study in continuous conduction mode

Table 9 gives the optimization results for the converter in CCM with different inductor core materials. Finally, the phase inductor core temperature of operating point #6 has never limited the optimizations.

Table 9: Optimization results of the sizing operating point study of the IBC in CCM

Material	Permeability	Solution?	Number of iterations	IBC electronic weight (gr)	Fs (kHz)	number of phases	Inductor value (µH)	limiting constraints
Kool Mu	26	✗						
	40	✓	59	853	250	2.6	95.2	Jlitz1, Tj_mos_1, THD_3, condcution_3, I_DC_Filter_4
	60	✓	**11**	**534**	**250**	**2.6**	**87.4**	**saturation_1, Jlitz_1, efficiency_1, Tj_diode_1, Tj_mos_1, THD_3, conduction_3, I_DC_Lfilter_4**
	75	✓	15	602	250	2.6	87.5	saturation_1, Jlitz_1, efficiency_1, Tj_diode_1, THD_3, conduction_3, I_DC_Lgilter_4
	90	✓	35	726	250	2.65	89.7	saturation_1, Jlitz_1, efficiency_1, Tj_diode_1, THD_3, conduction_3, I_DC_Lfilter_4
	125	✓	21	1437	250	4	194	saturation_1, efficiency_1, efficiency_6, Tj_diode_1, I_DC_Lfilter_4
MPP	26	✗						
	60	✓	11	534	250	2.6	87.5	saturation_1, Jlitz_1, efficiency_1, Tj_diode_1, Tj_mos_1, THD_3, conduction_3
	125	✓	12	552	250	3.18	121	saturation_1, Jlitz_1, efficiency_1, Tself_6, I_DC_filter_high_4
Kool Mu Max	26	✗						
	60	✓	50	551	246	2.55	95.8	efficiency_1, saturation_1, Tj_diode_1, Tj_mosfet_1, THD_3, conduction_3 IDC_filter_4

For the IBC in CCM mode, it is not surprising that the algorithm could not found any solutions with low core permeabilities. It means that the constraints and input design variables must be released (for example authorized a higher switching frequency) if the use of cheap 26µ materials is desired.

It is also interesting to notice that there is an optimum to be found in the choice of the permeability for a same material technology. Figure *4* shows the evolution of the optimal converter weight as a function of the Kool Mu inductor core permeability value. Finding a continuous relationship between the material permeability and its magnetic properties such as the saturation under DC bias, temperature influence, etc. would be exciting. This knowledge could be indeed precious for the manufacturers of strong value-added products that can order customized magnetic cores since they could define the optimal permeability. It is also funny to notice that the 60 permeability is the most widespread among the magnetic core manufacturers. Then the question is: does the 60µ permeability naturally offer the best properties explaining their large use or is that because it is widespread that

the manufacturers took care to its properties?...

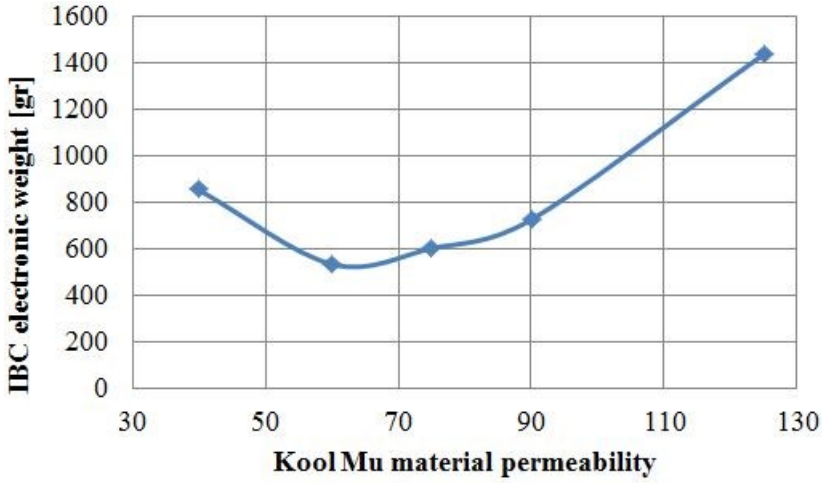

Figure *4*: Weight of the IBC in CCM for different permeabilities of the Kool Mu inductor core (that are optimization results)

Finally, there are two materials giving the best solution: the MPP 60 and Kool Mu 60. The second being around 10 times cheapest and easier to provide, the obvious choice for an industrial is the Kool Mu 60. The power density in the imaginary world for this optimal converter is 9.4 kW/kg.

3) Conclusion on material and conduction mode choices

With this initial set of specifications, the optimal imaginary converter in DCM has a power density of 11.4 kW/kg while the optimal converter in CCM has a power density of 9.4 kW/kg. Since the control of the converter will be easier if the conduction mode is discontinuous and since the converter in continuous conduction mode is heavier, the next part will focus on the discontinuous conduction mode Interleaved Buck Converter.

IV. CONCLUSION

It has been demonstrated that formulating an optimization problem for several operating points is really easy with the proposed method of pre-sizing in the imaginary (continuous) world. The difficulty being to define the sizing operating points based on designer knowledge. It is worth noting that the method allows quickly taking off the doubts of the designer about this critical issue.

The gradient based optimization algorithm does not require hard configuration in the CADES environment: only the maximum number of iterations and the accuracy of the solution. This may be one of the reasons why all of the results of this chapter have been obtained in one day work: including set of the optimization requirements, data saving and analysis).

Nevertheless, optimization is a science that must be learned by experience of the designer into the algorithm behavior, implementation environment and of course into the system to design.

Eventually, the pre-design in the imaginary world is a very suitable tool for understanding the design problematic, rapidly test different technologies or other discrete choices such as the conduction mode of the converter. For the illustrating study case of the thesis, the discontinuous conduction mode will be retained. The next steps in the design process will be first to negotiate the specifications with the system integrator to release or in contrary to more constraint the design requirements. Secondly, the power density of 11.4 kW/kg given by the optimization with the 60µ MPP material seems impressive… but the optimal Interleaved Buck converter is made of 3.2 phases! The designer will thus have to pre-size the converter with the negotiated set of specifications and to come back in the real world (i.e. with discrete components) before prototyping purpose.

V. REFERENCE

[1] Magnetics, "Magnetics® Powder Cores," 2018. [Online]. Available: https://www.mag-inc.com/Products/Powder-Cores. [Accessed: 01-Jul-2018].

Chapter 9: Negotiation of the Requirements

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I. INTRODUCTION

Figure *1* remembers the flowchart of the proposed pre-design in the imaginary world approach.

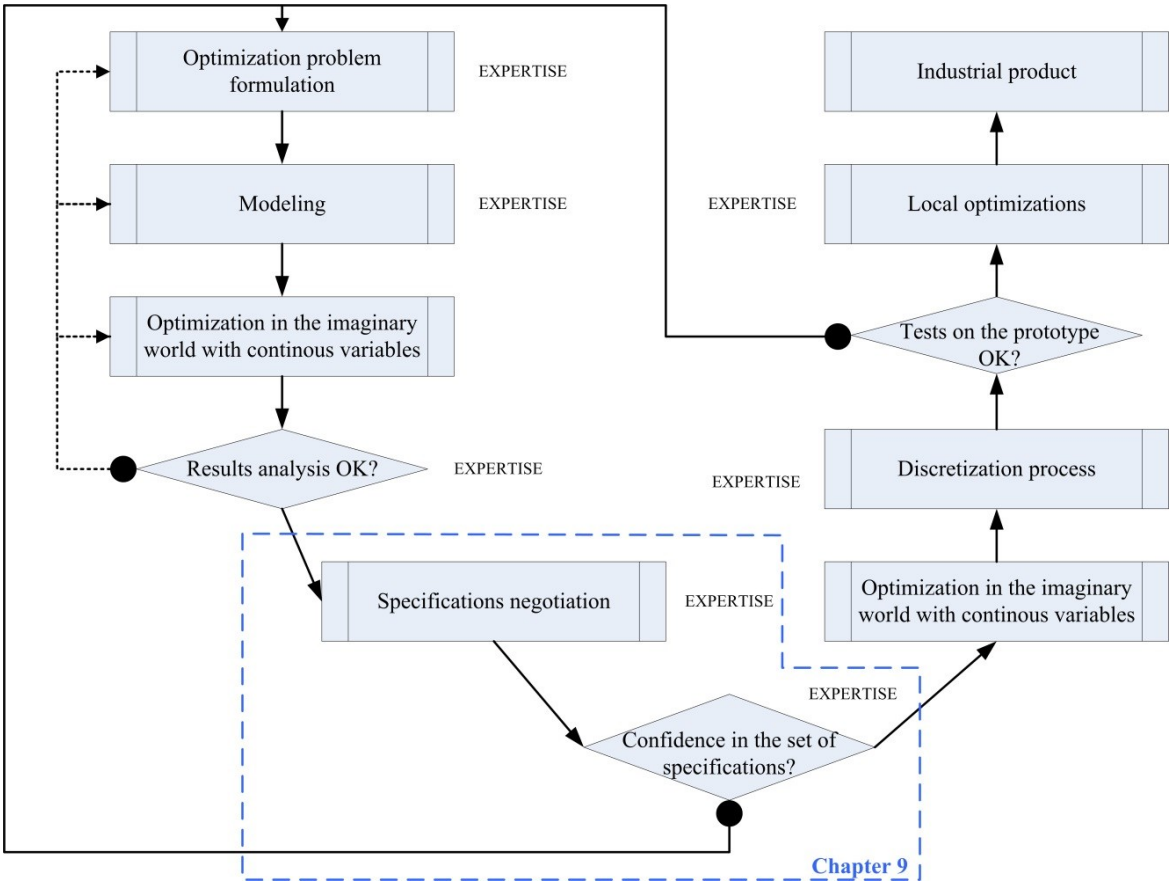


Figure *1*: Flowchart of the preliminary design in the imaginary world approach

In this chapter, the main objective is to negotiate the power electronic system requirements with the system integrator. The specifications negotiation requires quantitative data in which the designer is confident. One way is using imaginary parameterized optimizations and Pareto fronts. An imaginary parameterized optimization is the result of several optimizations in the continuous imaginary world of a system under a fixed set of specifications with one or several swept variables. An imaginary Pareto front is the boundary front of the optimal solutions between two divergent objective functions. Their usefulness of these curves has been exposed in [1],[2],[3] and Chapter 2 of this thesis.

First the strategies to obtain in practice these curves will be exposed and used on the study case. Then, imaginary parameterized and Pareto optimizations will be performed in the continuous imaginary world. It will show the advantage of questioning the requirements in the imaginary world thanks to a facilitated understanding of the problem in a very short time to address "problem setting". A "problem setting" (also called "problem formulation") means finding the good formulation of the design problem as a set of objectives and constraints,

before searching a real and discrete solution inside the design space defined by the optimization problem formulation, what will the objective of a later "problem solving" step.

II. STRATEGIES TO OBTAIN IMAGINARY PARAMETERIZED OPTIMIZATION CURVES AND PARETO FRONTS

This section will give the method to obtain these curves in practice with 1st order optimization algorithm.

In the present optimization problem formulation, there are three kinds of variables: the inputs, the fixed parameters and the outputs. The input variables are either design variables such as the phase inductor external diameter, or implicit constraint parameter like the "desired" efficiency of the converter. The fixed parameters are either materials physical property such as the weight density of the phase inductor resin or operating point parameter such as the converter maximum input power. The output variables are the intermediate computed data and the optimization constraints. Besides, some of these variables are shared between different operating points: for example the maximum total harmonic distortion (THD) on input and output currents of the converter that is 5% for all operating points.

The technic will so be different if the optimized and/or swept variable is an input, a fixed parameter or an output variable in the optimization problem formulation and if it is shared between several operating points.

A. Imaginary parameterized curves or Pareto fronts with input variable as swept parameter

The technic to obtain these curves with a model input swept variable is simple. The designer creates or uses a script that launches N times the optimization under constraints with the *N* different values of the swept parameter. In the aim to limit the optimization time and number of iterations, it is interesting with gradient based optimization algorithm, to use the solution of the previous optimization as starting point of the new optimization. It is assumed that changing the swept parameter a little will not change dramatically the optimum area in the space of solutions.

B. Imaginary parameterized curves or Pareto fronts with shared output optimization variable as swept parameter

The previous strategy is valid for the global input design variables. But in the study case, several operating

points are studied simultaneously. In order to get a Pareto Front with a shared output constraint variable, a new input global parameter and a new constraint for each studied operating points should be created as in Figure *2*.

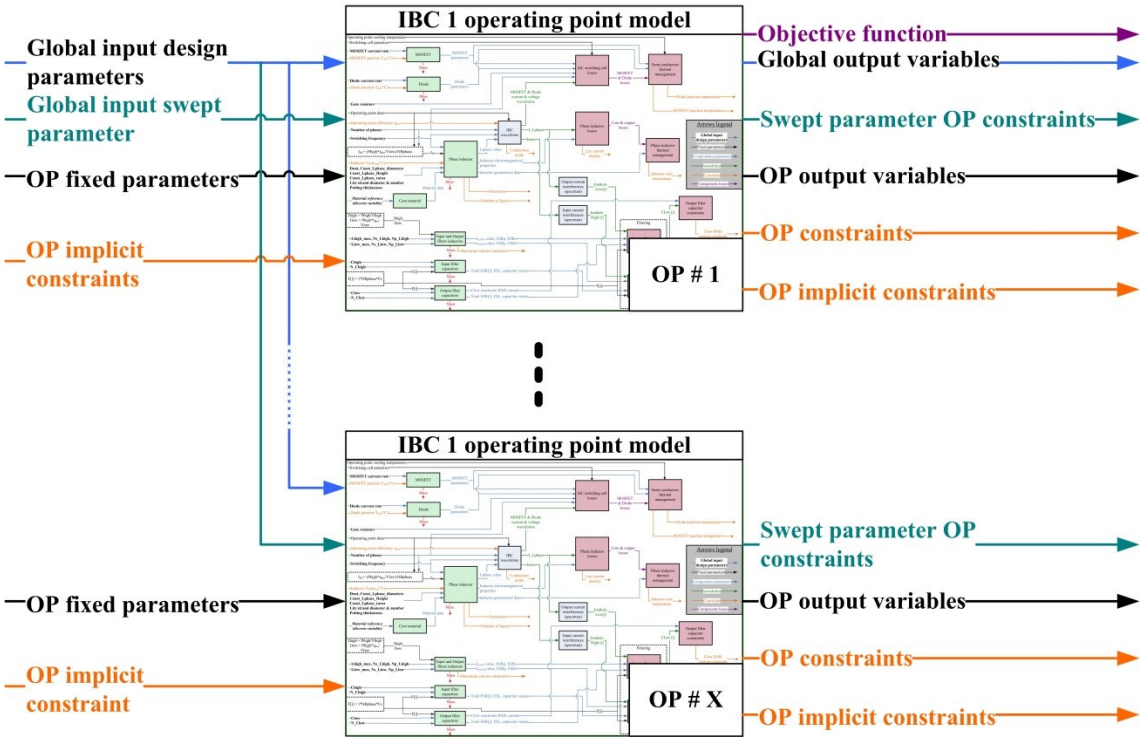


Figure *2*: Handling the swept variables that are shared between several operating points

For example to study the influence of the THD requirement level on the all operating points, a new input global variable named "*THD_max*" and a new output constraint per studied operating point #X named "*const_THD_X*" should be created (as in Eq. *1*, "S*wept parameter OP constraint"* on Figure *2*)). Then the swept parameter will be "*THD_max*" ("*Global input swept parameter"* on Figure *2*) as for the parameterized curves obtained by sweeping the input parameters.

$$const\ THD\ X = THD\ max - THD\ X\ \ : must\ be > 0 \qquad \text{Eq. } 1$$

III. IMAGINARY PARAMETERIZED OPTIMIZATIONS AND PARETO FRONTS TO NEGOTIATE THE REQUIREMENTS

Table 1 reminds the initial set of specifications that the designer should negotiate.

Table 1: Interleaved Buck Converter specifications

Criteria	Minimum Value	Maximum Value	Conditions/Remarks
Input power	0 W	5 kW	For the entire of input/output voltage ranges (at this point of project starting)
Input voltage	450 V	800 V	For a power range [0 ; 5] kW
Output voltage	200 V	400 V	For a power range [0 ; 5] kW
Efficiency	96 %	NA	at 5 kW
Efficiency at a third of full load	90 %		at 1.7 kW = (5 kW)/3
Input/Output current THD	NA	5 %	For a power range [Pmax/3 ; Pmax] kW
Cooling temperature	-40 °C	65 °C	For a power range [0 ; 5] kW

In the study case, despite the efforts there remain two discrete variables that are the constraint on the conduction mode for all the operating range and the phase inductor core material. To negotiate the set of specifications with the system integrator, either the designer plots one parameterized optimization for each discrete variable and keeps only the best solutions, or he/she plots the parameterized curves with only one fixed discrete variable. The second choice allowing a simpler analysis, it will be used for the study case.

The following parameterized optimization traces and Pareto fronts have been obtained with the Interleaved Buck Converter working in Discontinuous Conduction Mode (DCM) and with the 60µ MPP material for the phase inductor core. *Table 2* reminds the sizing operating points for this converter. All of the following plots have been obtained with these three operating points optimized simultaneously.

Table 2: Sizing operating points of the IBC

Operating point number	Input voltage [V]	Output voltage [V]	Input power [W]	Cooling temperature [°C]	Possible limiting constraints
# 1	800	200	5000	65	IBC efficiency, power components temperature, current density in the phase inductor and output filtering components
# 3	800	200	1700	65	input and output current THD, efficiency
# 4	450	400	5000	65	conduction mode, maximum input DC current in filtering inductors

A. *Imaginary parameterized optimization curves as function of the input parameters*

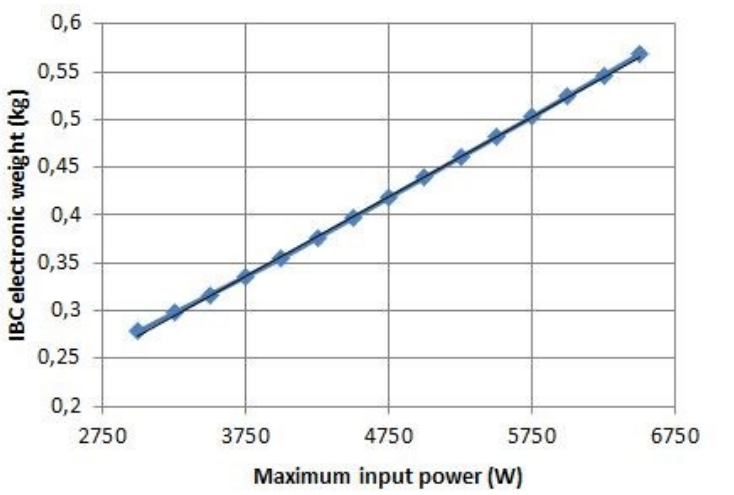
Apart from the efficiency or harmonics constraints, the major sensitive parameters on the design of the converter are the operating voltages, the power and the thermal environment. That is why the first parameterized optimization curves are about the maximum input voltage (so the range of input voltage is increased), the maximum and minimum output voltages (range of output voltage is changed), the cooling plate temperature and the maximum power of the converter (range of converter power is increased).

1) Maximum input power sweeping

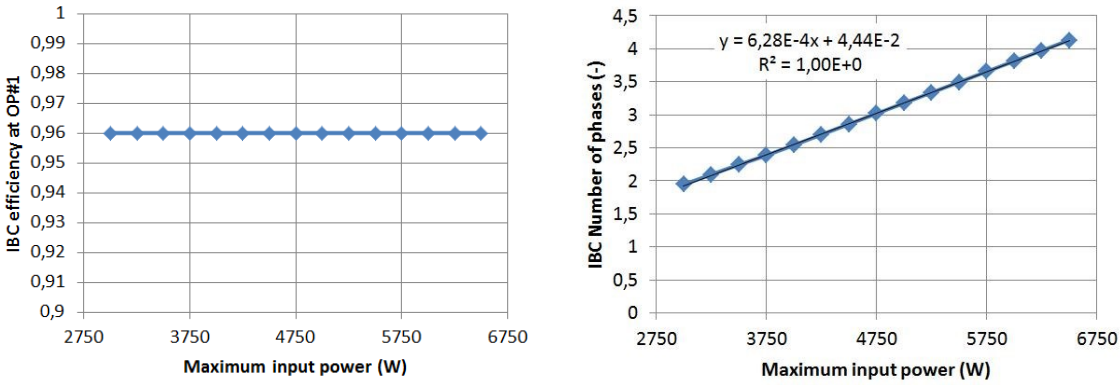
Table 3 gives the evolution of the converter weight as a function of its maximum input power. In other word, the converter electronic weight is the objective function to minimize and the converter maximum (nominal) input power is swept (i.e. the range of converter power is swept). Table 3 also indicates the value of the other operating range parameters and constraints.

Table 3: Sweeping of the converter maximum input power value

Criteria	**Minimum Value**	**Maximum Value**
Input power	**Pmax / 3**	**Swept**
Input voltage	450 V	800 V
Output voltage	200 V	400 V
Efficiency at Pmax	96 %	NA
Efficiency at Pmax/3	90 %	
Input/Output current THD	NA	5 %
Cooling temperature	65 °C	



The converter weight linearly increases with the converter required maximum input power. It is expected that an optimal design of the converter regarding its weight will not oversize the efficiency. The converter efficiency stays indeed constant during the parameterized optimization (Figure *3*, (a)). It means that the losses to evacuate through the cooling plate increase linearly with the converter input power. In order to respect the constraints on components maximum temperature, the optimization algorithm increases the IBC number of phases (Figure *3*, (b)), i.e. the thermal exchange surface for constant components size. That is the case of the semiconductors in TO-247 package.



(a) (b)

Figure *3*: IBC (a) efficiency, (b) optimal number of phases evolution, during the parameterized optimization of the converter maximum power

Figure *4* (a) shows the evolution of the phase inductor weight during the parameterized optimization. The difference between an IBC of 3 kW and an IBC of 6.5 kW is negligible (only 2 grams). The shape of the plot of the phase inductor weight is explained by the evolution of the switching frequency during the parameterized optimization (Figure *4*, (b)). It is itself explained by the filters weight evolution (Figure *4*, (c)) due to the input and output current THD constraints and the resonant frequency of the filters that must be lower than 90% of the switching frequency(Figure *4*, (d)).

Finally, the evolution of the power density of the converter (Figure *5*) summarized these statements since the shape is a mixed between the linearity evolution of the number of phases and the plot shapes of the power components weight.

All these plots have been obtained in 110 s with a personal computer. It shows the interest of using the proposed approach for the negotiations. Indeed, with that information, the system integrator could define the optimal configuration of the solar panels to minimize the global weight of the power supply of the airship.

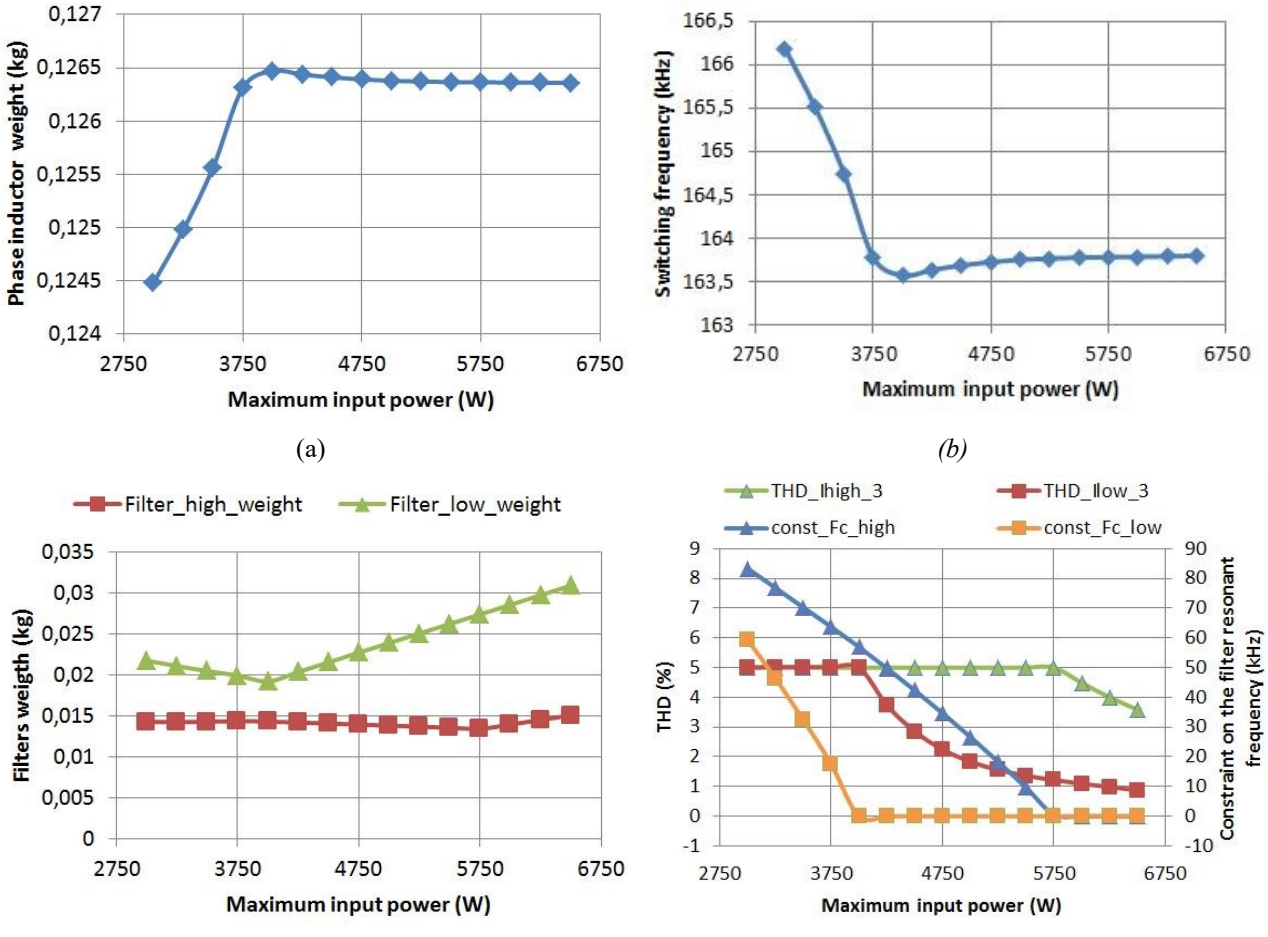


Figure *4*: Interleaved Buck converter (a) phase inductor weight, (b) switching frequency, (c) filtering weight and (d) input and output currents THD at OP#3 (must be < 5 %) and constraints on filters resonant frequency (must be > 0 kHz), as function of its maximum input power

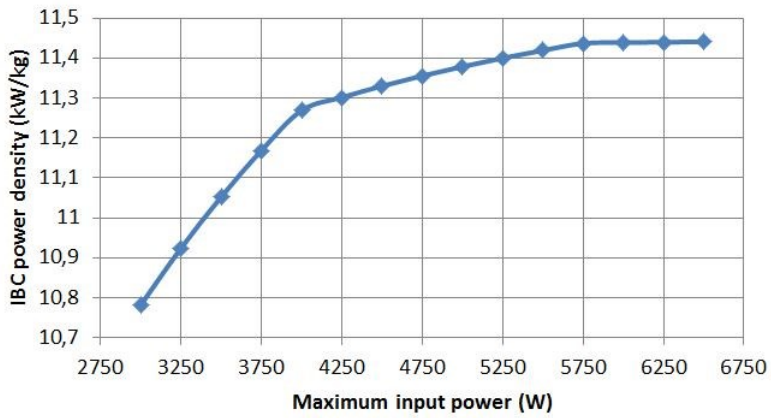


Figure *5*: Evolution of the converter power density as a function of its maximum input power

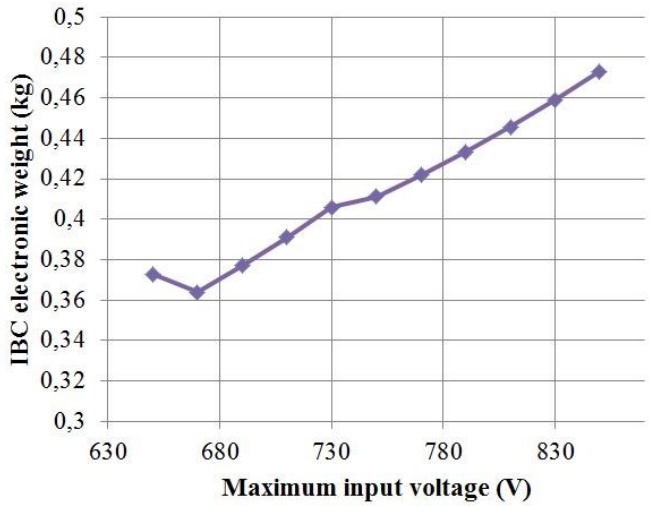
2) Maximum input voltage sweeping

Table 4 gives the evolution of the converter weight as a function of its maximum input voltage. It also

indicates the value of the other operating range parameters and constraints.

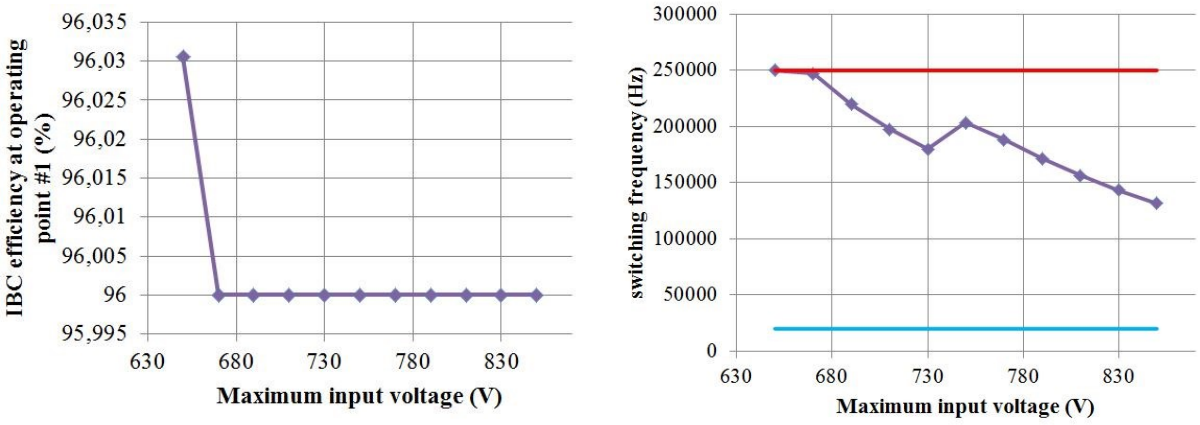
Table 4: Parameterized optimization of the IBC as a function of its maximum input voltage

Criteria	Minimum Value	Maximum Value
Input power	5000/3	5000
Input voltage	450 V	**Swept (650-850 V)**
Output voltage	200 V	400 V
Efficiency	96 %	NA
Efficiency at Pmax/3	90 %	
Input/Output current THD	NA	5 %
Cooling temperature	65 °C	



The global trend Table 4 shows that when the range of input voltage increases, the converter weight rises. But it is surprising that the converter weight is higher for a maximum input voltage of 650 V (so an input voltage range of 200 V between 450 V and 650 V) than for a maximum input voltage of 670 V (so a range of 220 V between 450 V and 670 V). Because the converter is re-optimized in its whole for each value of the swept parameter, it is necessary to watch the different constraints and input design variables to understand the results if they are not the expected ones.

Figure *6* (a) shows that for a maximum input voltage of 650 V, the converter efficiency is a little bit higher than the limit given by the specifications. It is due to the fact that the switching frequency is limited to 250 kHz when apparently the optimization algorithm would like to increase it!



(a) (b)

Figure *6*: Evolution of the (a) converter efficiency of operating point #1, (b) switching frequency value, as a function of the maximum input voltage of the converter

With more investigations on Table 4 and Figure *6*, a change in the tendency of the converter weight and the switching frequency between 730 V and 750 V can be seen. An analysis of what happens during the optimization helps to understand it: Figure *7* shows the evolution of the IBC number of phases as a function of the converter maximum input voltage. The IBC has 0.8 phases more for a maximum input voltage of 730 V than for 750 V.

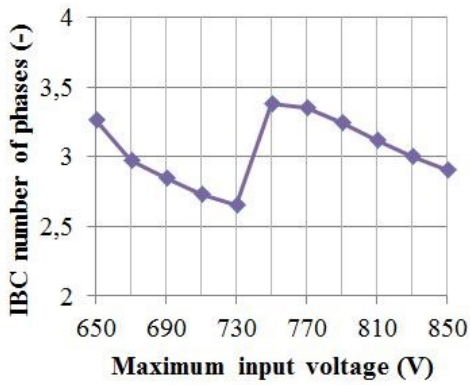


Figure *7*: Evolution of the optimum number of phases as a function of the maximum input voltage swept parameter

Figure *8* shows the evolution of the IBC number of phase during the optimization for a maximum input voltage of 750 V as well as of the phase inductor temperature at the operating point #1.

It seems that one of the major limiting constraints is the phase inductor temperature (confirming the importance of having a thermal model of this component): once again, the higher is the number of phases, the higher is the total thermal exchange surface to evacuate the losses.

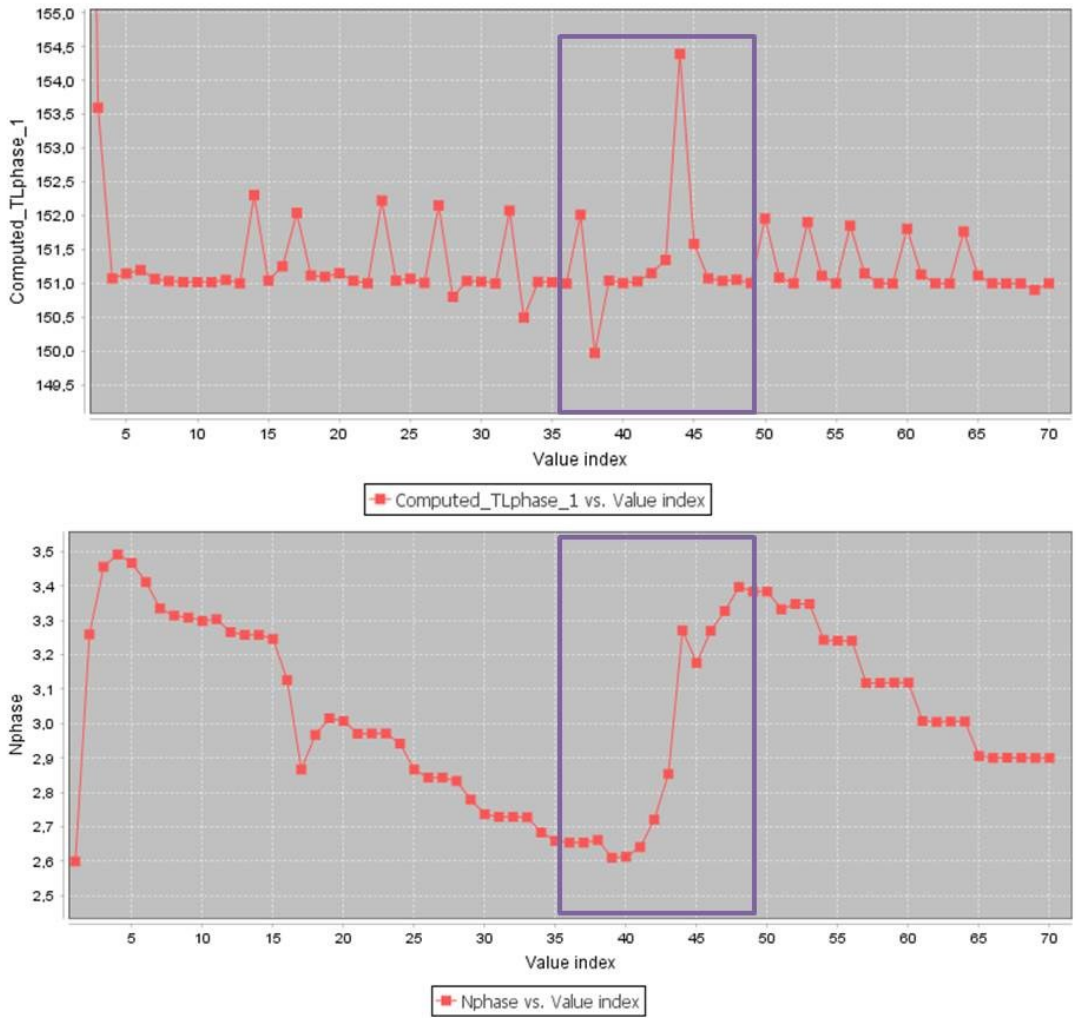


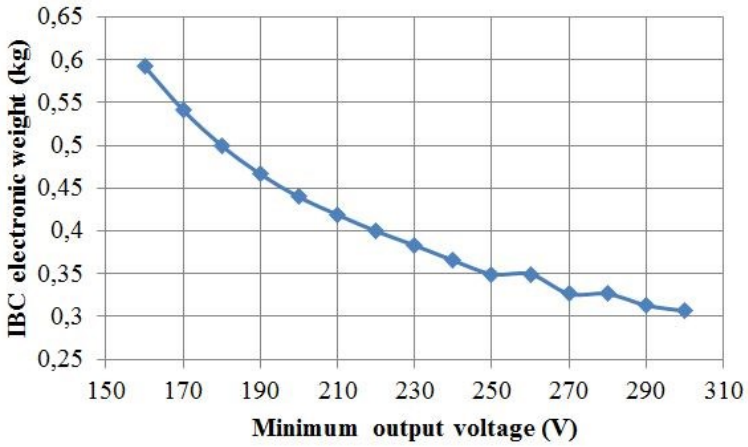
Figure *8*: Evolution of the phase inductor temperature (top) and of the number of phase (bottom) as a function of the iteration index of the parameterized optimization (solution at 730 V being iteration #36 and solution at 750 V being iteration #49)

3) Minimum output voltage sweeping

Table 5 gives the evolution of the converter weight as a function of its minimum output voltage and it indicates the value of the other operating range parameters and constraints.

Table 5: Parameterized optimization of the IBC as a function of its minimum output voltage

Criteria	Minimum Value	Maximum Value
Input power	5000/3	5000
Input voltage	450 V	800 V
Output voltage	**Swept (150 – 300 V)**	400 V
Efficiency	96 %	NA
Efficiency at Pmax/3	90 %	
Input/Output current THD	NA	5 %
Cooling temperature	65 °C	



Once again, when the converter operating range decreases (100 V of output voltage range for a minimal value of 300 V against 250 V of output voltage range for a minimal value of 150 V), the electronic weight decreases too.

4) Maximum output voltage sweeping

One of the operating point that the designer must hardly negotiate with the system integrator is when the minimum input voltage and maximum output voltage are close. Indeed, if the difference between the input and the output voltages of the converter is too small, the power inductor of the converter should be as low as possible. This leads to a high switched current for the MOSFET at its turn OFF and the number of phases will so have to increase. In other words, the topology and conduction mode choices will have to be reviewed. The designer should so demonstrate that a too small difference between input and output voltages will induce a large weight penalty for the converter with the considered topology. Of course, the topology may also be revisited at this point, but this is out of the scope of this thesis.

Table 6 shows how the converter electronic weight rises exponentially with the increase of maximum output voltage value (thus closer to the input voltage).

Table 6: Parameterized optimization of the IBC as a function of its maximum output voltage

Criteria	Minimum Value	Maximum Value
Input power	5000/3	5000
Input voltage	450 V	800 V
Output voltage	200 V	**Swept (330 – 430 V)**
Efficiency	96 %	NA
Efficiency at Pmax/3	90 %	
Input/Output current THD	NA	5 %
Cooling temperature	65 °C	

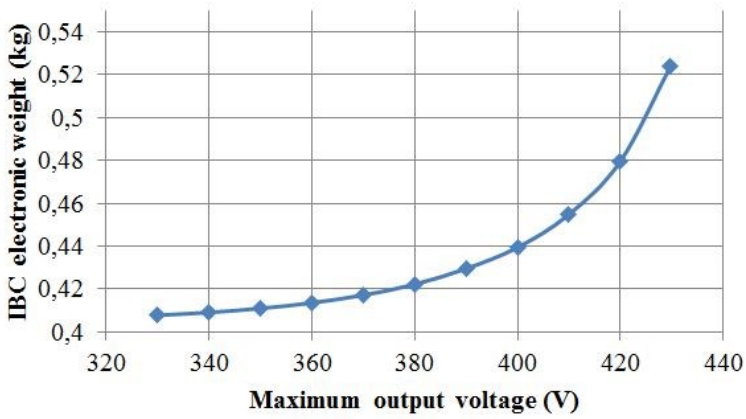


Figure *9* is the illustration of how the electronic designer can justify a minimum distance of 50 V between the input and the output voltage of the converter with quantitative arguments.

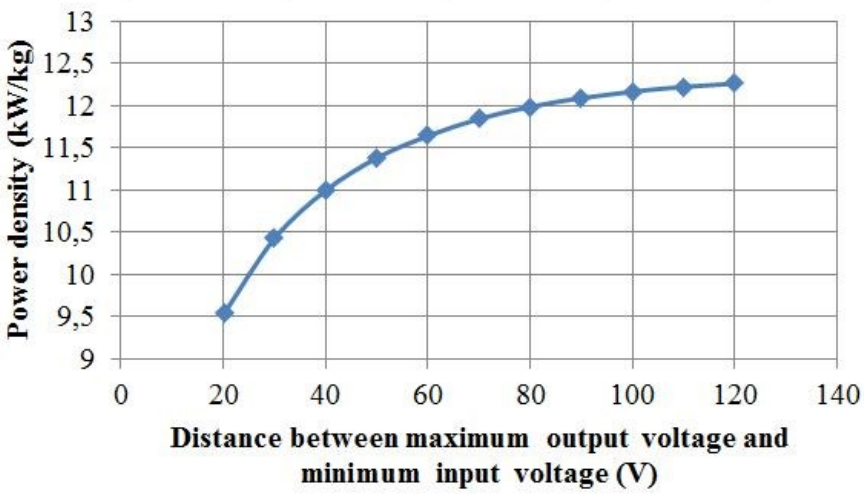


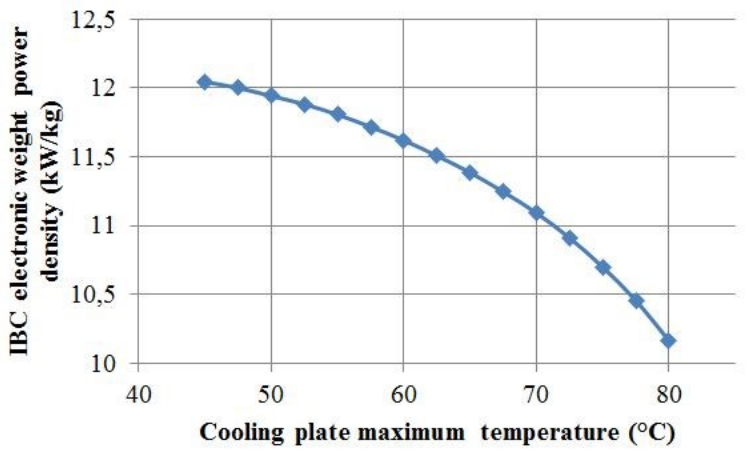
Figure *9*: Evolution of the converter electronic weight power density as a function of the distance between input and output voltage

5) Maximum cooling plate temperature sweeping

Finally, one of the most important data for the designer and for the system integrator is the power density of the converter as a function of the cooling plate temperature. Indeed, the gains on the converter weight can be compared to the additional weight of the thermal system to obtain the desired temperature. A system level trade off can thus be found. That is the purpose of Table 7.

Table 7: Parameterized optimization of the IBC as a function of the cooling plate maximum temperature

Criteria	Minimum Value	Maximum Value
Input power	5000/3	5000
Input voltage	450 V	800 V
Output voltage	200 V	400 V
Efficiency	96 %	NA
Efficiency at Pmax/3	90 %	
Input/Output current THD	NA	5 %
Cooling temperature	**Swept (45 – 80) °C**	



B. *Imaginary Pareto fronts*

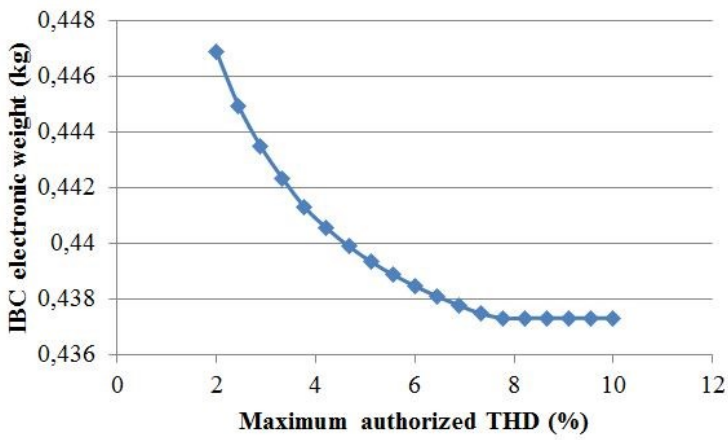
The Pareto in its definition is the boundary between two antagonistic objective functions. In the study case, the efficiency can be defined as the second objective function after the converter weight. Besides, the constraints coming from the aeronautical standards, like the total harmonics distortion (THD), could also be seen as objective function: i.e. as safety criteria to minimize.

1) Imaginary Pareto front between the Total Harmonic Distortion and the converter weight

Table 8 presents the imaginary Pareto front between the maximum allowed THD and the converter weight.

Table 8: Pareto front between the maximum authorized THD value and the converter weight

Criteria	Minimum Value	Maximum Value
Input power	5000/3	5000
Input voltage	450 V	800 V
Output voltage	200 V	400 V
Efficiency	96 %	NA
Efficiency at Pmax/3	90 %	
Input/Output current THD	NA	**Swept (2-10) %**
Cooling temperature	65 °C	



From 8% as maximum authorized THD, the converter weight stopped to decrease. It is due to the fact that the

THD is not anymore constraining the optimization of the converter from this value: Figure *10* shows the THD actual value at the sizing operating point #3.

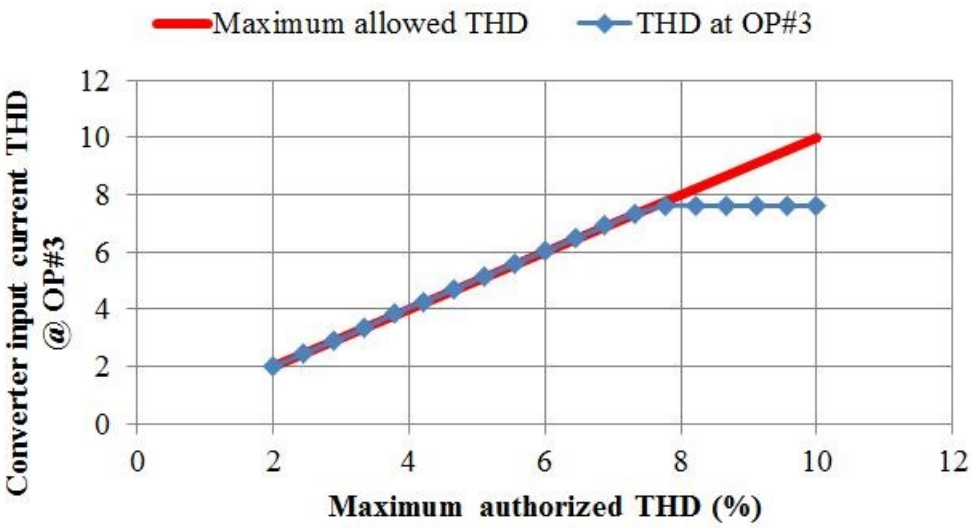


Figure *10*: Converter input current THD for the operating point #3

2) Imaginary Pareto front between the current density of inductor wiring and the converter weight

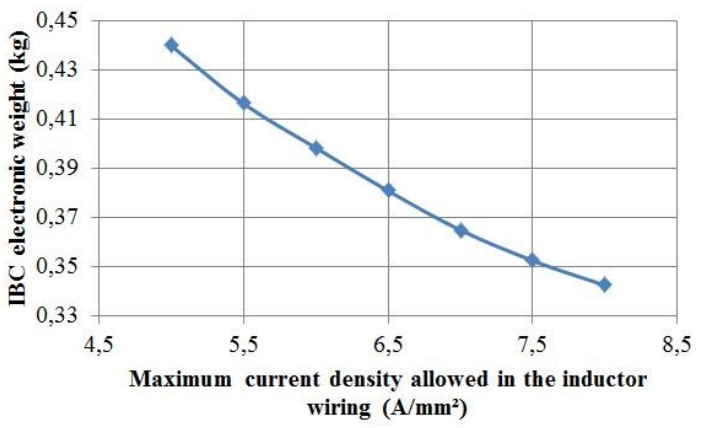
Table 9 presents the Pareto front between the maximum authorized current density in the inductor wiring connectors and so wiring itself (see chapter 5, section II.C.3.) and the converter weight. This limit (i.e. constraint) has been imposed by the system integrator. But he would perhaps release this requirement regarding the weight saving.

Unfortunately, the losses model of the phase inductor wiring does not authorize to optimize the converter with current density higher than 8 A/mm² since it does not accurately evaluate the winding AC losses. It is necessary to pay attention to the validity domain of the models and should not trace Pareto front aside from them.

Nevertheless, it is shown that a release of 3A/mm² allows winning almost 10 grams per DC-DC converter: it is particularly interesting since there are dozen of them in the aircraft.

Table 9: Pareto front between the maximum authorized maximum current density and the converter weight

Criteria	Minimum Value	Maximum Value
Input power	5000/3	5000
Input voltage	450 V	800 V
Output voltage	200 V	400 V
Efficiency	96 %	NA
Efficiency at Pmax/3	90 %	
Input/Output current THD	NA	5 %
Cooling temperature	65 °C	

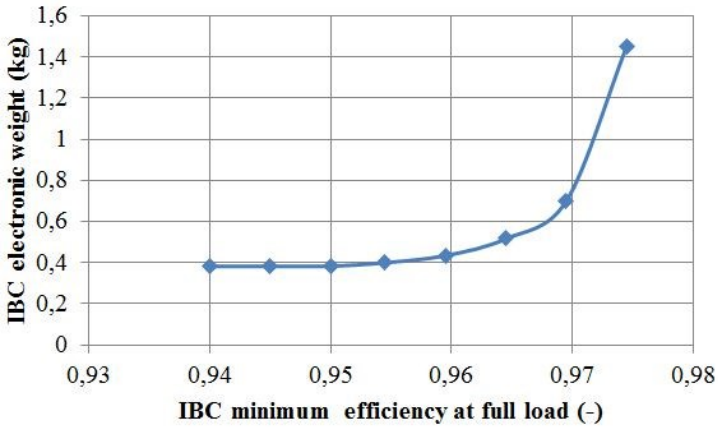


3) Pareto front between the converter efficiency and the converter weight

Eventually the most expected Pareto front (between the converter efficiency to maximize and the converter weight to minimize) is shown in Table 10.

Table 10: Pareto front between the minimum authorized efficiency value at full load and the converter weight

Criteria	Minimum Value	Maximum Value
Input power	5000/3	5000
Input voltage	450 V	800 V
Output voltage	200 V	400 V
Efficiency	**swept (94 -97.5 %)**	NA
Efficiency at Pmax/3	90 %	
Input/Output current THD	NA	5 %
Cooling temperature	65 °C	



Not surprisingly, increasing the efficiency also increase the converter weight. Again, this is a system level trade off since low efficiency will require more solar panels to provide the necessary energy to the aircraft and a more efficient (so heavy) cooling system.

IV. SET-UP OF THE NEW REQUIREMENTS AND OPTIMIZATION IN THE IMAGINARY WORLD

A. Final negotiated requirements

Finally, it is possible to imagine that after a first negotiation phase between the power electronic designers and the system integrator, there is a new set of specifications as presented in Table 11 (still fictive[1]). For example, a required efficiency of 96.5% instead of 96% may reduce the total solar panels weight of 12 kg and the cooling system weight of 3 kg when the added weight on the High Voltage Power Conditioning Unit would be about 5 kg. The difference between minimum input voltage and maximum output voltage is set at 40 V instead of 50 V initially because it would be the best trade-off between the solar panels, the DC-DC converters and the energy storage system regarding the global weight.

Table 11: Negotiated set of specifications

Criteria	**Minimum Value**	**Maximum Value**
Input power	5000/3	5000
Input voltage	475 V	850 V
Output voltage	235 V	435 V
Efficiency	96.5 %	NA
Efficiency at Pmax/3	93 %	
Input/Output current THD	NA	5 %
Cooling temperature	70 °C	

As stated in the first chapters, these negotiations are current in aeronautical projects and several iterations are necessary to converge. Hopefully, the Imaginary Pareto front and parameterized optimization curves presented in this chapter took one day of work on a personal computer (including setting the specifications and performing the first analysis). Again, once the optimization is properly formulated, the proposed approach is very fast in its optimization execution.

B. Optimization with negotiated requirements

Once the negotiations are finalized and requirements are finally fixed, the final optimizations in the imaginary world can be performed. As previously stated, only the 60µ MPP material has been considered for the example.

[1] For confidentiality reasons

Table 12 gives the optimal but imaginary solutions of the converter with the initial and negotiated set of specifications.

Table 12: Optimal imaginary converter for the initial and negotiated set of specifications

legend	unit	Solution with initial set of specifications	Solution with negotiated set of specifications
Input design variables			
Converter global parameters			
Buck Interleaved phases number	-	3.178	2.848
Buck Interleaved phases switching frequency	kHz	163.79	104.33
Phase inductor variables			
External Buck inductance diameter	cm	4.02	4.42
Turns number coefficient: should be [0.85 1] to keep thermal model valid	-	1	1
Number of strands of the Litz wire of the IBC phase inductor : [16 , 1050]	-	466	436
Litz strand diameter	µm	75.4	79.7
Switching cell variables			
MOSFET current rate at 25degC (from 10 to 90 A)	A	55.5	62.5
Diode current rate at 25degC (from 5 to 113 A)	A	22.8	26.8
External Gate resistor	Ohm	2.5	2.5
Input filter variables			
Nominal value (for no current) of the filtering single inductor	µH	1.54	4.35
Number of inductors in series configuration	-	1.93	2.62
Number of inductors in parallel configuration	-	1.05	1.76
Capacitor value between 5.6nF and 0.39µF	nF	108	194
number of capacitors put in parallel	-	3.17	2.85
Output filter variables			
Nominal value (for no current) of the filtering single inductor	µH	0.96	1.62
Number of inductors in series configuration	-	1.79	2
Number of inductors in parallel configuration	-	2.3	2.62
Capacitor value between 8.2 nF and 2.2µF	nF	188	293
Number of capacitors put in parallel	-	3.17	2.85

Table 12: Optimal imaginary converter for the initial and negotiated set of specifications (continuation)

legend	unit	Solution with initial set of specifications	Solution with negotiated set of specifications
Output design variables			
Global variables			
Converter electronic weight power density	kW/kg	11.37	10.50
Converter weight	g	439	476
Phase inductor weight (core + resin + wiring)	g	92.9 (46.3+10.1+27.5)	115 (61.4+11.9+32.7)
Filtering weight	g	38	53
Phase inductor internal diameter	cm	28.1	30.9
Phase inductor height	cm	9.05	9.95
Phase inductor turns number	-	31	33.3
Phase inductor value	µH	33.6	42.7
Constraint on the input filter resonance frequency const_Fr_high = 0.9*Fs-Fr_high has to be >0	kHz	25	30
Constraint on the output filter resonance frequency: const_Fc_low = 0.9*Fs-Fr_low has to be >0	kHz	0	0
Output variables and limiting constraint from operating point #1			
Converter efficiency	%	96	96.5
MOSFET losses	W	16.7	15.45
MOSFET computed junction temperature	°C	84	87
Diode losses	W	20.85	19.19
Diode computed junction temperature	°C	105	104
Phase inductor losses	W	26.9	28.5
Phase inductor core computed temperature	°C	150	150
Phase inductor current density in Litz wires	A/mm²	5	5
Output filtering inductor DC current constrain (must be > 0)	A	0	0
Output variables and limiting constraint from operating point #3			
Total harmonics distortion of input IBC current (THD_Ihigh)	%	5	5
Total harmonics distortion of output IBC current (THD_Ilow)	%	1.85	4.75
Output variables and limiting constraint from operating point #4			
Constraint on conduction mode (must be < -0.5 µH)	µH	-0.5	-0.5
Input filtering inductor DC current constrain (must be > 0)	A	0	0

The negotiated set of specifications being in its whole more constraining, it is normal for the converter weight to rise. For example, the new requirement about the converter efficiency (96.5% instead of 96%) makes the optimal switched frequency lower. A lower switching frequency conducts into higher passive components weights.

V. CONCLUSION

The negotiations of the requirements during preliminary design phases impact around 90% of the development cost of a project. The designer from one side and the system integrator from the other side are so under pressure to success this phase. Quantitative data obtained with a rigorous method help in the quality of the discussions during the negotiations. That is the object of this thesis and in particular of this chapter.

It has also been demonstrated that making the parameterized optimizations and Pareto fronts in the imaginary world allow understanding and setting the optimization problem. This is notably possible thanks to the analysis of the evolution of the design variables and constraints. In particular during each optimization since understanding the behavior of the gradient based optimization algorithm is an easy task as exposed in previous chapter.

The preliminary design phase should also result into a development plan in which the designer is confident: prototyping the solution is essential. A heuristic discretization process is proposed in the next chapter to rapidly pre-size a power electronic system in the real world.

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Chapter 10: Discretization Procedure to Come Back in the Real World

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I. INTRODUCTION

The advantage of using the proposed Imaginary design approach in the preliminary design phase of a power system is the possibility to explore a wide range of solutions, within the limit of the models validity domain. This wide research area browsed in a short time is made with the compromise that the optimum solutions are given in the imaginary world. Coming back in the real world is therefore necessary, since some non-integer values are obviously not possible (as the number of phase), and fully customized power electronics components are for now very expensive and hard to industrialize.

There are at least two major methods to come back in the real world from the optimal imaginary converter.

- By using a combinatory exploration or a genetic algorithm handling the discrete design variables on a reduced optimization problem size as presented in the 1st Appendix of this thesis.
- By applying a discretization procedure on the already formulated optimization problem.

The first method would increase the chances to ensure the optimality of the discrete solution. On the downside, it requires a new formulation of the optimization problem, in contrary to the second method, which takes advantage of the designer knowledge and the data provided by the optimizations in the imaginary world.

In this work, we have chosen the second method, which will be detailed in the next sections.

II. HEURISTIC DISCRETIZATION PROCESS DESCRIPTION

A. Discretization process principle

Based on the optimal imaginary solution, we sequentially re-optimize in the imaginary world with the two discrete variables closest from the imaginary optimal one until no more discrete variables remain. The order of the variable to be discretized is chosen as a function of their influence on the objective function, the first variable being the one that affects the most the objective. The proposed heuristic discretization process is shown in Figure *1*.

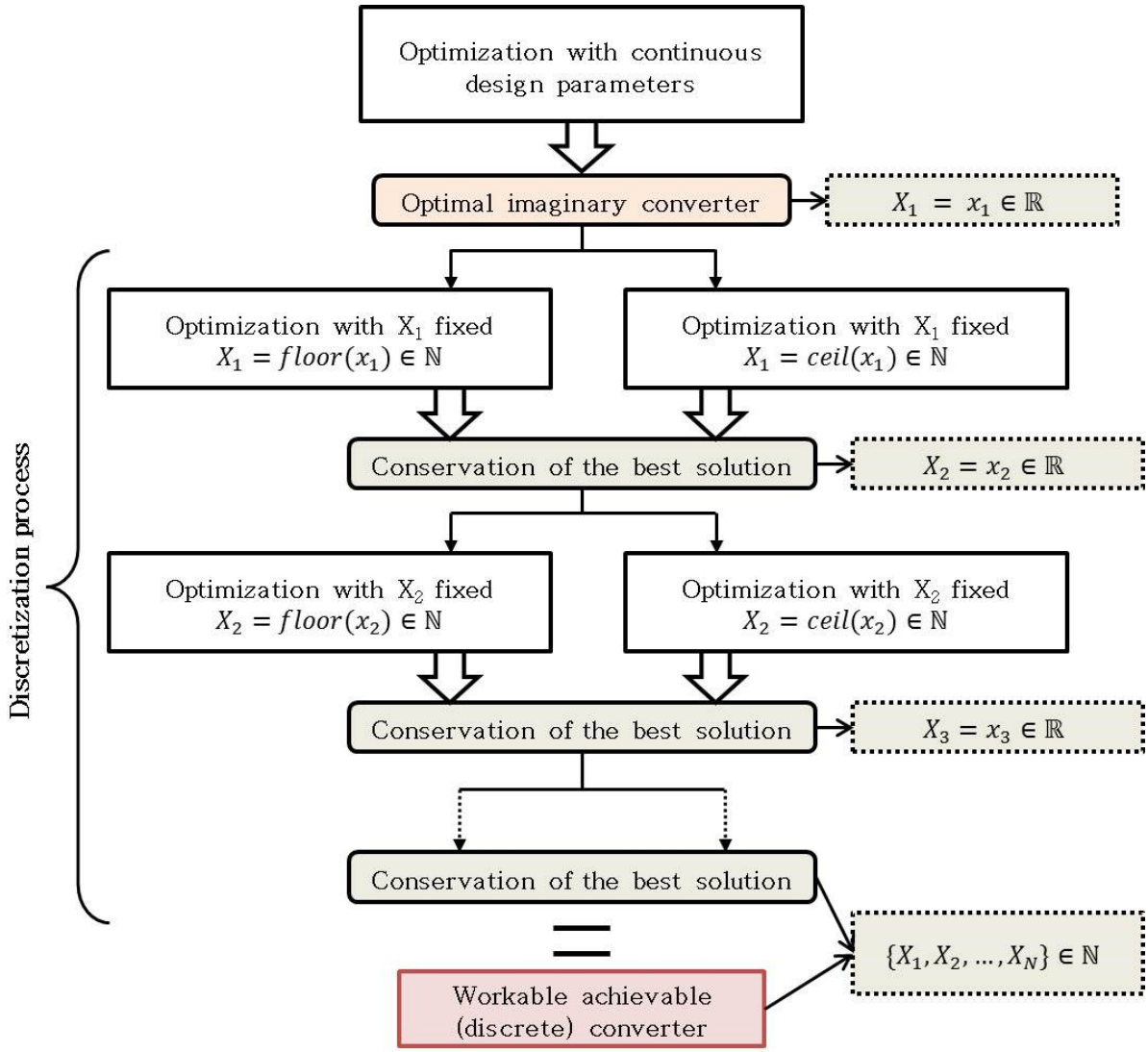


Figure *1*: Heuristic discretization process with X_n the nth discrete variable, with the objective function more sensitive to X_1 than X_2, etc.

In this approach, determining which variable is more influent than the other one can be made based on both model sensitivity analysis and the knowledge and experience of the designer (hence the heuristic term) .

It should be noticed that this approach is looking for an optimum close to the imaginary solution: it is a local research. In other words, it may not provide the optimal discrete solution of the optimization problem as it is illustrated in Figure *2*.

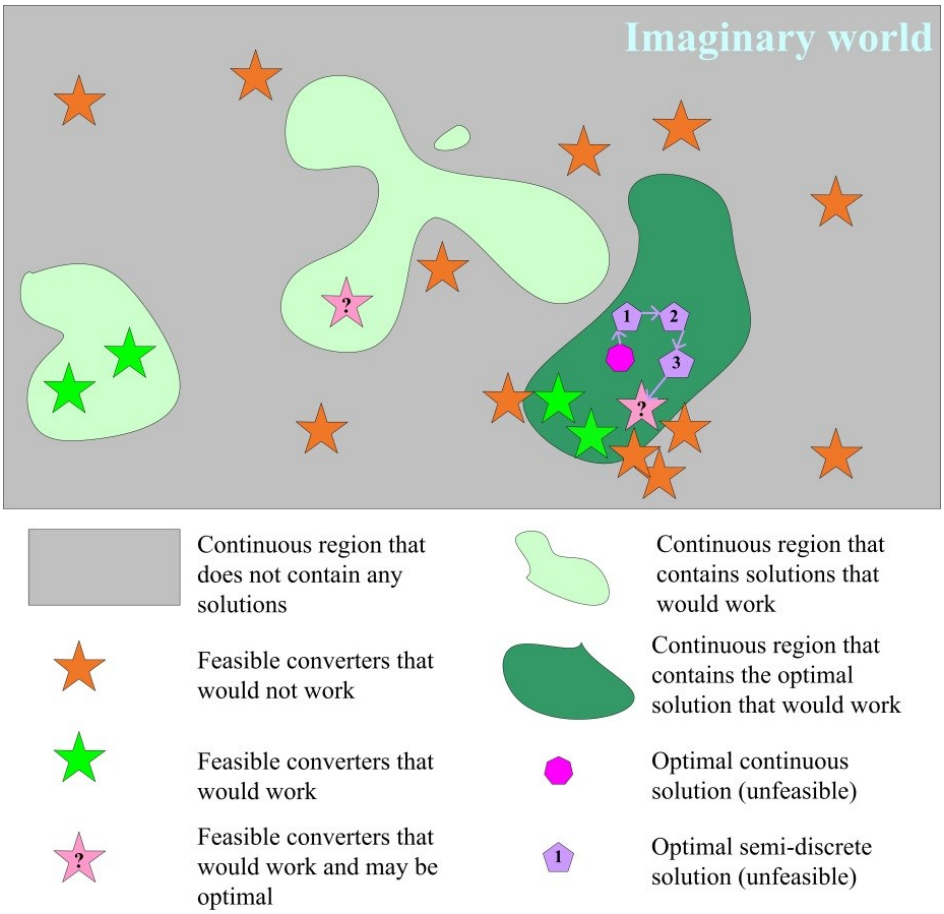


Figure *2*: Illustration of the proposed heuristic discretization process

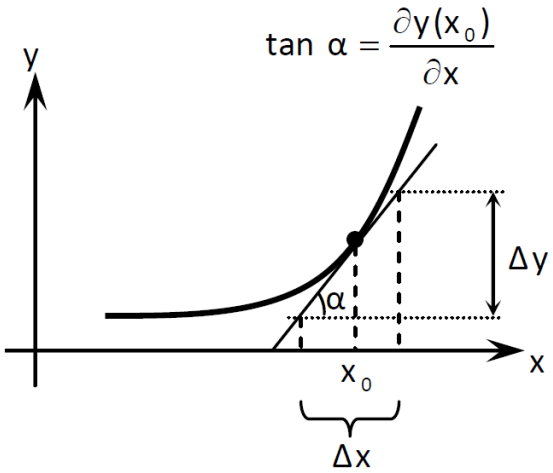
B. Discretization process for the study case

According to the discretization procedure, it is essential to determine the appropriate sequence of influent variables. In this study case the objective function is minimizing the converter electronic weight.

1) Local sensitivity analysis on the optimal imaginary solution

As previously stated, the suggested heuristic discretization procedure to determine a real solution to the set of specifications is based on a local research. It is so possible to use a local sensitivity analysis to determine the best discretization sequence.

The sensitivities are computed by the linearization of the outputs around the optimal imaginary solution as shown on Figure *3*. This linearization is possible thanks again to the computation of the partial derivatives of the continuous and differentiable optimization model.



The formula of the sensitivity computation is:
- In absolute: $\Delta y = tan(\alpha) \cdot \Delta x$

Figure *3*: Local sensitivity analysis illustration on an optimization model with x an input variable and y an output variable

In the studied case, the design variables to be discretized are: the IBC number of phases, the phase inductor core and winding, the filtering components, the semiconductors current ratings. The sensitivity analysis is so performed with these design variables on the objective function but also on the limiting constraints (which indirectly impact the objective function) and is shown on Figure *4*. This analysis has been performed with absolute values that are representative of the possible jump of the variables could make during the discretization.

		ΔComputed_Tj_diode_1	ΔComputed_Tj_mos_1	ΔComputed_TLphase_1	ΔComputedEfficiency_1	ΔJlitzLphase_1
Δ input capacitance	1 µF	0	0	0	0	0
Δ input inductance	1 µH	0	0	0	0	0
Δ output capacitance	1 µF	0	0	0	3.092E-14	0
Δ output inductance	1 µH	0	0	0	8.452E-7	0
Δ number of phases-	1	-1.131E1	-5.859	-2.671E1	-8.508E-4	-1.345
Δ inductor core ext. diam	5 mm	-3.568	-5.016	-1.476E1	4.061E-3	-1.511E-1
Δ diode current rating	5 A	-4.116	5.61E-1	0	-8.928E-5	0
Δ MOSFET current rating	10 A	0	-7.982E-1	0	-1.405E-5	0

(a)

		ΔIBC_weight	ΔTHD_Ihigh_3	ΔTHD_Ilow_3	ΔCont_conduction_4	Δconst_Idc_Lfilter_high_4
Δ input capacitance	1 µF	5.362E-11	-2.718E-8	0	0	0
Δ input inductance	1 µH	0	-1.039	0	0	-7.503E-1
Δ output capacitance	1 µF	4.236E-11	0	-1.797E-8	0	0
Δ output inductance	1 µH	0	0	-3.053	0	0
Δ number of phases-	1	1.484E-1	-3.86	-5.486	-1.517E-5	0
Δ inductor core ext. diam	5 mm	8.267E-2	-1.847E-1	-1.84	1.561E-5	0
Δ diode current rating	5 A	0	0	0	0	0
Δ MOSFET current rating	10 A	0	0	0	0	0

(b)

Figure *4*: Local sensitivity analysis of the optimal imaginary solution (a) on the operating point #1 limiting constraints, (b) on the objective function and operating points #3 and #4 limiting constraints

The sensitivity values are displayed: in red if it increases, in blue if it decreases, in grey if there is no variation on the output [1].

This sensitivity analysis confirms once again that for the chosen design variable absolute value variations, the most sensitive parameter of the optimization is the number of phase (one more phase increasing the converter

weight of 148 g at this point) and then the phase inductor core dimension (an increase of 5 mm of the inductor external diameter increases the converter weight of 82,6 g at this point). Then, it is the filtering inductors and then the filtering capacitors. Finally the semi-conductors do not directly influence the converter weight (0 g on Figure *4*) but impacts the choice of the switching frequency through the efficiency and the junction temperature constraints (see Figure *4*) and so the passives weight indirectly.

2) Designer knowledge added to the local sensitivity analysis

Other factors than sensitivity must be taken into account to set a proper sequence of the discretization: for example, the number of choices among manufacturer series. In order to limit the number of steps of the discretization procedure, the natural number discrete variables such as the phase inductor number of turns or the number of filtering inductors to be set in parallel will be taken as the round of the continuous value (ceil or floor according to the associated constraint). That is the reason why they have not been considered in the sensitivity analysis. Finally, Table 1 proposes a discretization process for the optimal imaginary converter of the study case.

Table 1: Details about the different steps of the discretization process for the application

Discretization process step #	Concerned discrete variable(s)	Reasons
1	**Number of phases** of the Interleaved Buck Converter	The most sensitive parameter
2	**Inductor core** i. Number of turns = floor(imaginary number of turns) ii. Strand diameter : closest available AWG iii. number of strands = ceil(Nstrands minimal for Jlitz = Jlitz_max)	The second most sensitive parameter. Number of turns and strands fixed right after since not really sizing parameters once the core is fixed
3	**MOSFET current rating**	There are fewer references than for the diode: it is so less adaptable.
4	**Diode current rating**	There are fewer references than for the filtering components: it is so less adaptable.
5	**Input and output filtering capacitors references** i. Number of capacitors in parallel = ceil (imaginary number of capacitors)	Can be optimized simultaneously since coupled by the only continuous parameter of the converter (Fs). Heavier than the filtering inductors.
6	**Input and output filtering inductors references** i. Number of inductors in parallel = ceil (imaginary number of parallel inductors) ii. Number of inductors in serie = ceil (imaginary number of parallel inductors)	Can be optimized simultaneously since coupled by the only continuous parameter of the converter (Fs).

So finally, there are 12 optimizations to perform with this heuristic procedure.

III. DISCRETIZATION OF THE OPTIMAL IMAGINARY IBC CONVERTER OF THE STUDY CASE

A. Results of the discretization

The results of the different steps of the discretization process are summarized in Table 2 (in the following page). The grey columns are the non-conserved solutions.

Step #0 corresponds to the optimal imaginary solution of the new set of requirements. Because the optimal number of phases is 2.82, the 2 optimizations of the step #1 have been done with a number of phases of 2 and then a number of phases of 3. The best solution is with 3 phases: this variable is fixed to this value for the following optimizations.

For the step #2, the imaginary optimal phase inductor core has an external diameter of 42.6 mm. In the manufacturer catalog [2], there are one core with an external diameter of 39.9 mm (ref. 55083) and two cores with an external diameter of 46.7 mm. The choice among these last two cores is made thanks to the optimal cross section of the inductor (64.6 mm²): ref. 55090 has a cross section of 134 mm² and ref. 55439 of 199 mm². Reference 55090 is therefore selected for the optimization. The better optimization result was for reference 55083.

The discretization process has been followed in that way until the definition of a real converter (i.e. that can be built). The process took 494 s in total for the 12 performed optimizations. With the analysis of the data, the optimizations set up and the manual selection of the components in the manufacturer's datasheets, the discretization of the imaginary converter took one working day.

Table 2: Results of the discretization procedure step by step

label			unit	Discretization process													Real (discrete) solution
Discretization proces step				0	1		2		3		4		5		6		7
Optimization process		Solution?		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	NA
		Number of iterations		9	18	8	10	9	7	7	7	10	7	7	7	7	NA
		Optimization time	s	22	48	34	44	53	19	23	48	62	19	23	49	50	NA
Optimization input design variables	Converter global parameters	**IBC number of phases**	-	2.848	**2**	3	3	3	3	3	3	3	3	3	3	3	3
		IBC switching frequency	kHz	104.33	81	108.4	106.7	110	103.5	103.5	103.5		103.6	103.5	103.5	103.5	103.5
	Phase inductor variables	**Phase inductor core external diameter**	cm	4.42	5	4.26	**3.99**	4.67	3.99	3.99	3.99	3.99	3.99	3.99	3.99	3.99	3.99
		Turns number coefficient: should be [0.85 1] to keep thermal model valid	-	1	1	1	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9
		Number of strands of the Litz wire of the IBC phase inductor : [16 , 1050]	-	436	703	424	465	439	412	412	412	412	412	412	412	412	412
		Litz strand diameter	µm	79.7	75	78	75.3	88.8	79.9	79.9	79.9	79.9	79.9	79.9	79.9	79.9	79.9
	Switching cell variables	**MOSFET current rating at 25degC**	A	62.5	85	59	65	67	**60**	90	60	60	60	60	60	60	60
		Diode current rating at 25degC	A	26.8	47	24.6	33	30	35.5	30.7	**34**	**38**	34	34	34	34	34
	Input filter variables	**Nominal value (for no current) of the filtering single inductor**	µH	4.35	4.23	3.68	2.39	2.8	4	4	4		4.35	**3.3**	3.3	3.3	3.3
		Number of inductors in series configuration	-	2.62	5	2.33	2.82	2.66	2.4	2.4	2.3		2.4	2	2	2	3
		Number of inductors in parallel configuration	-	1.76	1.7	1.6	1.27	1.38	1.7	1.7	1.7		1.76	1.5	1.5	1.5	2
		Capacitor value between 5.6nF and 0.39µF	nF	194	390	180	187	173	190	190	189		**180**	**220**	220	220	220
		number of capacitors put in parallel	-	2.85	2.8	3	3	3	3	3	3		3	3	3	3	3
	Output filter variables	**Nominal value (for no current) of the filtering single inductor**	µH	1.62	1.8	1.8	1	1.25	2	2	2		2.3	2	**1.5**	2.2	2.2
		Number of inductors in series configuration	-	2	5	2.6	3.2	3	2.66	2.65	2.65		3	2.6	2.9	2.5	3
		Number of inductors in parallel configuration	-	2.62	2.1	2.1	1.5	1.74	2.3	2.2	2.2		2.4	2.2	1.9	2.3	3
		Capacitor value between 8.2 nF and 2.2µF	µF	0.293	1.14	0.256	0.280	0.251	0.261	0.264	0.261		**0.22**	**0.27**	0.27	0.27	0.27
		Number of capacitors put in parallel	-	2.85	2	3	3	3	3	3	3		3	3	3	3	3

Table 2: Results of the discretization procedure step by step (continuation)

		label	unit	Discretization process													Real (discrete) solution
		Discretization proces step		**0**	**1**		**2**		**3**		**4**		**5**		**6**		**7**
Optimization output design variables	**Global variables**	**Converter electronic weight power density**	**kW/kg**	**10.50**	**8,73**	**10,460251**	**8,47457627**	**6,89**	**8,43**	**8,43**	**8,43**		**8,42**	**8,43**	**8,43**	**8,43**	**8.255**
		Converter weight	gr	476	572.9	478	590	726	593.1	593.1	593.1		593.8	593.3	593	593.4	605.77
		Phase inductor weight (core + resin + wiring)	gr	115 (61+12+32)	203 (99+48+47)	109 (57+11+30)	146 (91+18+28)	192 (127+16+39)	146	146	146	146	146	146	146	146	146
		Filtering weight	gr	53	99	50,5	50,6	49.2	52.8	52.8	52.8		53.5	53,1	52.8	53,2	65,5
		Phase inductor internal diameter	mm	30.9	34	29.8	24.1	28.7	24.1	24.1	24.1	24.1	24.1	24.1	24.1	24.1	24.1
		Phase inductor height	mm	9.95	11.9	10.1	14.5	15.2	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5
		Phase inductor turns number	-	33.3	27.8	33.2	23.6	23	24	24	24	24	24	24	24	24	24
		Phase inductor value	µH	42.7	38.4	43.3	44.4	43.1	45.7	45.7	45.7	45.7	45.7	45.7	45.7	45.7	45.7
		Constraint on the input filter resonance frequency const_Fr_high = 0.9*Fs-Fr_high has to be >0	kHz	30	40	27	26.5	27.5	26	26	26		26.3	25	25	25	27.8
		Constraint on the output filter resonance frequency: const_Fc_low = 0.9*Fs-Fr_low has to be >0	kHz	0	32	0	0	0	0	0	0		0	0	0	0	0.4
	Output variables and limiting constraint from operating point #1	Converter efficiency	%	96.5	96.5	96.5	96.5	96.5	96.5	96.5	0.965	NOK	96.5	96.5	96.6	96.5	96.5
		MOSFET losses	W	15.45	24.7	14	15	15	14.9	15.25	14.9		14.9	15	16	15	15
		MOSFET computed junction temperature	°C	87	96	86	88	86	86	100.4	100		86	86.9	86.10	87	87
		Diode losses	W	19.19	25.8	18	18	18.2	18	17.8	17.9		17.9	17.9	17.10	18	18
		Diode computed junction temperature	°C	104	106	104	98	101	98	85	87		99	99	100	100	100
		Phase inductor losses	W	28.5	39.5	27.2	27	26.6	26.9	26.9	26.9		26.9	26.9	26.10	26.9	26.10
		Phase inductor core computed temperature	°C	150	150	150	150	141	150	150	150		150	150	151	150	150
		Phase inductor current density in Litz wires	A/mm²	5	5	5	5	3.78	5	5	5		5	5	5	5	5
		Output filtering inductor DC current constraint (must be > 0)	A	0	0	0	0	0	0	0	0		0	0	0	0	1.84
	Limiting constraint from operating point #3	Total harmonics distortion of input IBC current (THD_Ihigh)	%	5	5	5	5	5	5	5	5		5	5	6	5	4.75
		Total harmonics distortion of output IBC current (THD_Ilow)	%	4.75	5	3.8	3.8	3.83	3.81	3.81	3.81		3.83	3.8	3.9	3.91	3.65
	Limiting constraint from operating point #4	Constraint on conduction mode (must be < -0.5 µH)	µH	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5		-0.5	-0.5	-0.5	-0.5	-0.5
		Input filtering inductor DC current constrain (must be > 0)	A	0	0	0	0	0	0	0	0		0	0	0	0	1.7

B. Analysis of the discretization process

Figure *5* gives the evolution of the converter weight power density during the discretization process.

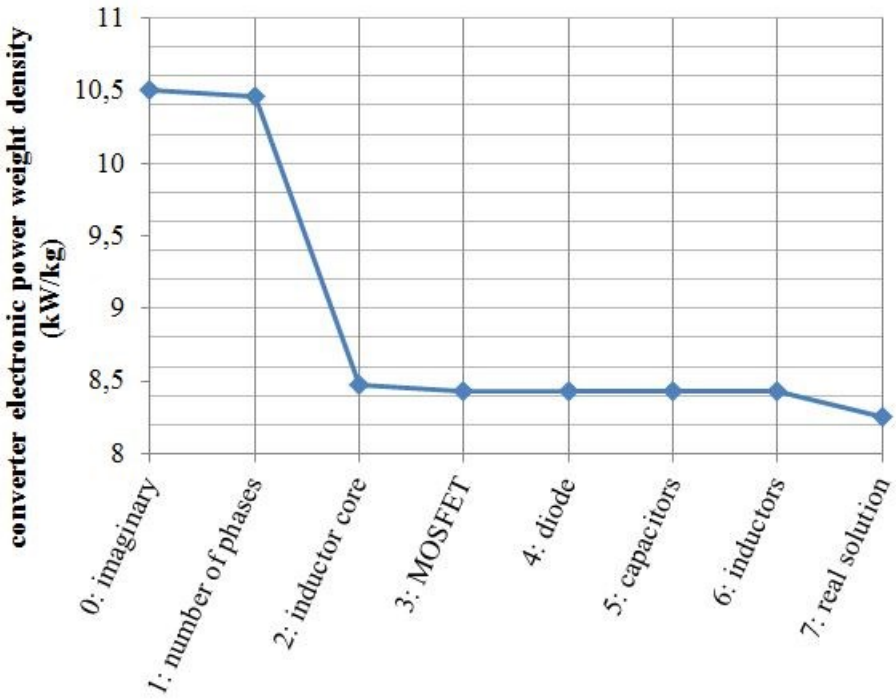


Figure *5*: Evolution of the converter power density during the discretization process

Based on this figure, several observations can be made. First, because the discrete value of the IBC number of phases (3) is close to the optimal imaginary one (2.848), the power density does not decrease too much. On the opposite, the few number of available different sizes of magnetic cores impacts badly the power density of the converter. The discretization of the other components does not affect a lot the converter weight.

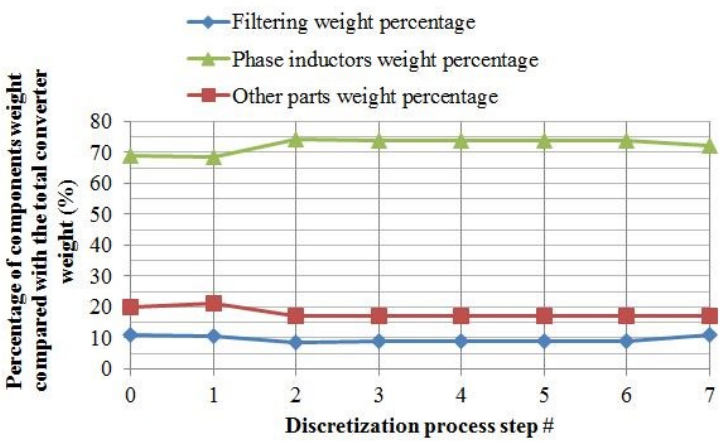


Figure *6*: Evolution of the components weight percentage during the discretization process

This statement is confirmed by Figure *6*.

The constraints on converter efficiency and power components temperatures also contribute to the converter

weight. Figure 7 demonstrates that the losses ratio of each power components is stable during the discretization confirming one again that the procedure is local. It also means that despite the negotiation of the set of specifications in the imaginary world, a real discrete degraded solution exists with a conservation of the main properties.

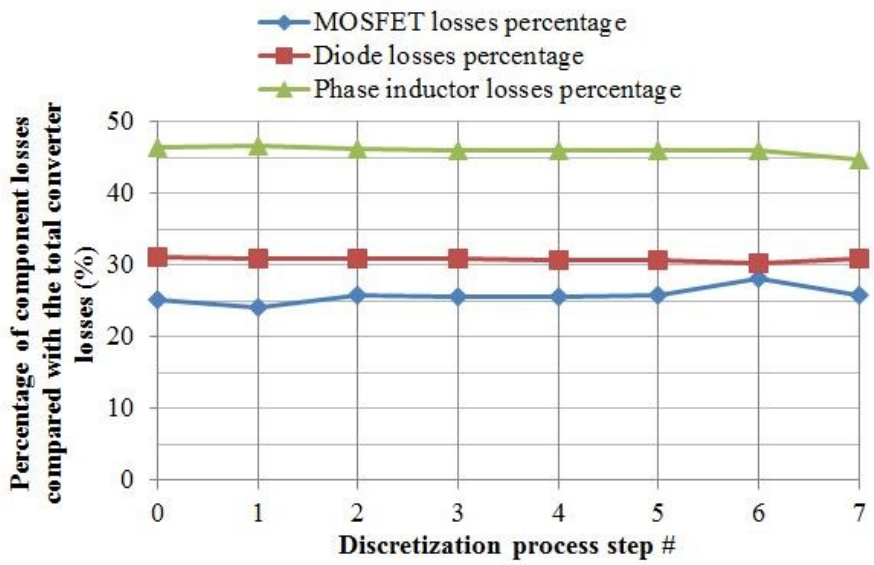


Figure 7: Evolution of the losses ratio of the power components

C. *Exploitation of the real discrete converter*

Depending on the chosen heuristic procedure and set of specifications, it may happen that the discrete solution is oversized. It is so interesting to re-optimize the discrete converter with a new objective function. For example in this case, maximize the power density or the efficiency by keeping only the converter maximum input power and the switching frequency as optimization variables.

But in the present case, the optimization gives a maximum input power of 5000.82 W instead of 5000 W and the maximum efficiency is still 96.5%. In other words, the discrete converter may be not optimal but it is not oversized regarding its power density.

IV. CONCLUSION

The preliminary design phase should result into a development plan based on fixed requirements in which the designer is confident: prototyping the solution is essential. A heuristic discretization process has been proposed to rapidly pre-size a power electronic system in the real world based on the optimization material previously set.

The drawback of such procedure is that the research of the discrete solution is local. It means that another

more optimal real converter may have been missed. Nevertheless, it has the advantage of being simple to set up and the result to be easy to analyze thanks to the conservation of the main properties of the system between the imaginary and the real solution.

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Conclusion

Number of power electronics systems will continue to grow in the future decades since electricity is the most suitable energy from now to face up the challenge of reducing the CO_2 emissions. In the last decades, several design methods and tools have been developed to help the power electronics designers during the design phase of a product. The non-exhaustive list being schematic and PCB layout design computer programs, engineer mathematical tools, schematic simulators, electromagnetic finite elements analysis methods and dedicated optimization methods and tools.

However, there were until now no tools or methods for a preliminary design phase of a power electronics system. For the reminder, a preliminary design phase must result into fixed (and feasible) requirements of the system to design and into a consolidated development plan of the product. The requirements must therefore be negotiated between the different partners with quantitative data. Having a large research area of possibilities to propose innovative solutions is also desirable.

This thesis stands on this observation and offers a new preliminary design approach for power electronics systems (Figure *1*). The specificities of this new approach are its ability to quickly explore a wide range of solutions for each technical architecture proposal and to compare them fairly. It also takes insight into the robustness and potential of the proposed concept with respect to requirements – margins, limitations, etc. These particularities of the proposed approach are granted by the use of a 1st order (gradient-based) optimization algorithm applied to the imaginary (continuous) world of power electronics systems.

This new approach follows the philosophy of the famous sentence of Albert Einstein: *"If I had only one hour to save the world, I would spend 55 minutes defining the problem and only 5 minutes finding the solution"*. On the approach flowchart (shown on Figure *1*), the first steps consist into formulating the optimization problem and into creating the associated model. These steps are detailed in chapters 5 to 7 of this thesis and they took a dozen of working months. On the opposite, the optimizations applied on a fixed set of requirements in order to identify the critical properties and the most suitable magnetic core material of an Interleaved Buck Converter took only one working day (chapter 8). The same time was needed to plot the imaginary parameterized optimizations and Pareto fronts of chapter 9. Another one working day was necessary to come back in the real world with a discretized solution based on the imaginary optimal solution (chapter 10).

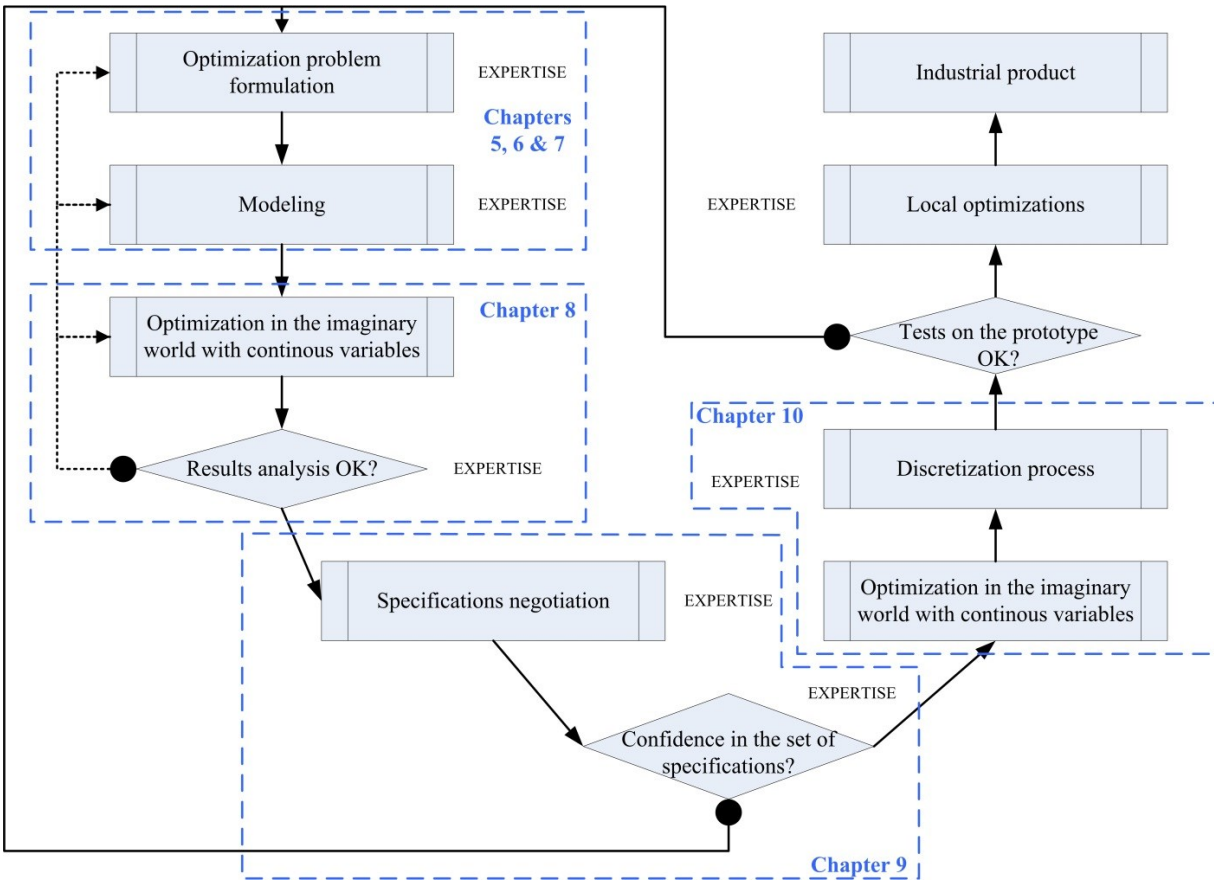

Figure *1*: Proposed approach flowchart

Perspectives of the thesis

The perspectives of this thesis are numerous, both in the field of power electronics and in the field of pre-sizing by optimization of power electronics systems.

First of all, the optimizations applied to an interleaved converter using wide-band-gap semiconductors (SiC) demonstrate that the next researches for improving the power density of power electronics systems is on high-performance magnetic materials at high switching frequencies. However, the work on semiconductors, although very advanced, is not yet finished. It would be interesting to understand in detail the hysteretic phenomenon of the junction capacity of the Schottky diode since it is problematic for resonant topologies that are supposed to minimize the switching losses of semiconductors.

Regarding pre-sizing by optimization for power electronics systems, it would be interesting to have an ergonomic capitalization tool used by a large community of designers to reduce the time spent in creating continuous and differentiable optimization models. However, this tool will have to integrate the context of each model created so that designers can use it and modify it with confidence.

A study on the impact of the accuracy level of the models on the optimization results, parameterized

optimizations and Pareto fronts could also define if it is one of the ways of reducing the time spent into problem formulation. The study of whether or not the tolerances of electronic components are taken into account could be added.

Finally, it is necessary to define in the future the best articulation between the different pre-design and design methodologies when designing a product according to the concerned participants (system integrators or equipment suppliers).

Appendices

Appendix 1: Review of Interleaved Buck/Boost Converters Design Methods

Appendix 2: Components parameters evaluation and IBC waveforms models capitalization

Appendix 3: Power components losses and thermal models capitalization

Appendix 1: Review of Interleaved Buck/Boost Converters Design Methods

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I. INTRODUCTION

The interleaved Buck or Boost converters are commonly used, especially for automotive application. There are several design methods proposed in the power electronics community that try to get an optimal configuration regarding a specific application. The aim of this chapter is to highlight the critical design parameters or the difficulties of this topology through three (non-exhaustive) design examples in which the design method will be briefly explained. Table 1 gives the main specification of the designs.

Table 1: Some design examples of interleaved Buck or Boost converters

Design example	Application	Objective function(s)	Direction	Power range	Input voltage range	Output voltage range	CCM or DCM?
[1]	Unknown	Volume to minimize	Boost	6 kW at nominal power	[290-480] V	650 V	CCM on [4-6] kW power
[2]	Automotive	Volume & losses to minimize	Buck	[250-1750] W	60 V	14 V	CCM
[3]	Automotive or renewable energy	Power density and efficiency to maximize	Buck & Boost	40 kW	220 V	600 V	CCM
[4]				100 kW	[300 – 380] V	750 V	

II. A DESIGN USING SEQUENTIAL METHOD

In the paper [1] a 6kW interleaved Boost converter is studied.

A. Design method description

The authors used a sequential design method making step by step some design choices. First, they wished to limit as much as possible the current ripples at the input and output of the Boost interleaved phases, i.e. before the filters with the intention to limit their size. So, continuous conduction mode (CCM) has been preferred over discontinuous.

Secondly, based on the research results from [5], the authors chose 4 as the number of IBC phases (Figure *1*). They could select 5 phases but the gain on current ripple does not value the price of the added phase volume.

The switching frequency has again been chosen regarding the filtering: the author's objective was to get an apparent frequency of 0.5 MHz: with 4 phases it means a switching frequency of 125 kHz.

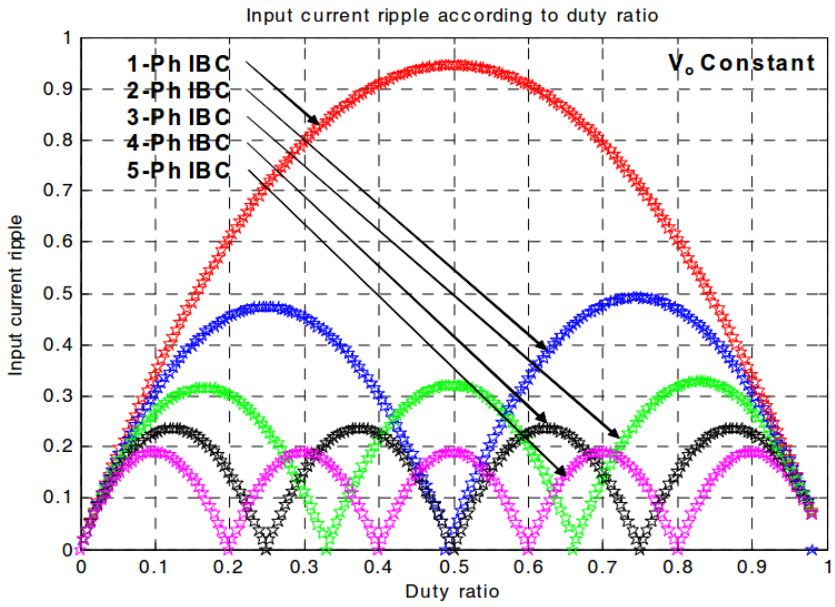


Figure *1*: IBC input current variation according to duty ration from [5]

For the inductor design, they first run an electrical analysis to determine the needed electrical value to stay in CCM for a [4-6] kW power range at 125 kHz (again to limit filtering size). They plotted the IBC phase inductor average current (Iin/4) and the half of peak-to-peak phase inductor current (di/2) for three different inductor and power values (Figure *2*). They selected 220 µH for the IBC phase inductance despite the fact that they were in DCM mode under 340 V input voltage at 4kW.

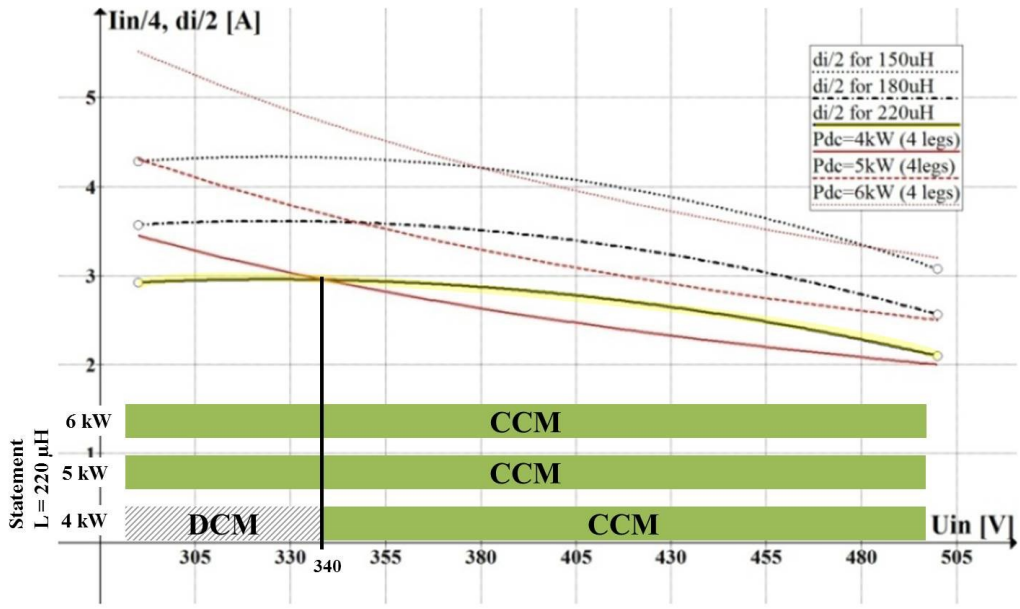


Figure *2*: Minimum inductance selection from [1]

For semi-conductors, 1200 V SiC N-MOSFET and Schottky diode have been used considering the 650V switching voltage and taking advantage of the low losses of this technology to limit cooling bulk. Current rating

of the semi-conductors is not justified.

For the heatsink design, the authors plotted 4 surfaces representing the constraint (semi-conductors junction temperature) and objective criterion P (the converter losses to minimize) and Rth the heatsink thermal resistance (cooling volume) according to major design parameters that are the switching frequency fsw and di representing the maximum current ripple in the phase inductor (so inductor value) which influence the switching losses (Figure *3*).

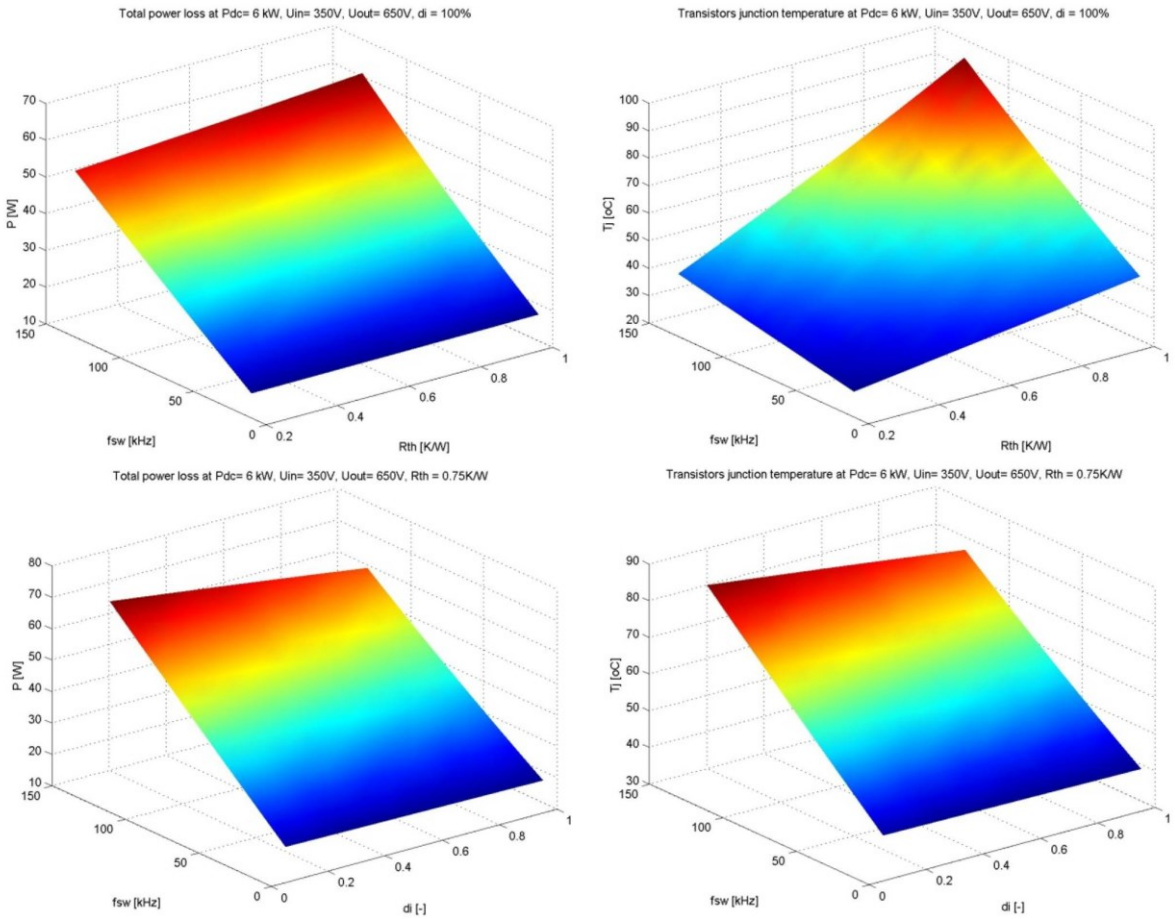


Figure *3*: Constraints and objective criteria trade-off surfaces from [1]

The authors chose finally fsw = 130 kHz according to these surfaces instead of 125 kHz. There is no information provided to confirm or infirm that they changed the phase inductor value. Figure *4* gives the final set of design parameters and the prototype picture.

Parameter	Value
Rated power	6 kW
Input/output voltage range	290 - 480 V/650 V
Switching frequency	up to 130 kHz / leg
Input capacitor	220 nF / 1000 V
Output capacitor	6 µF / 700 V, 4x47nF / 1000V
Transistors	1.2 kV / 80 mΩ (C2M080120D)
SiC Schottky diode	1.2 kV / 10A (IDH10S120)

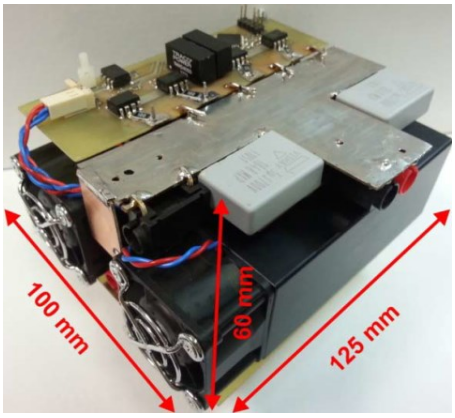


Figure *4*: 6 kW Interleaved Boost Converter parameter and prototype picture from [1]

B. Design method analysis

The design method employed in [1] by the authors can be summarized with Figure *5*.

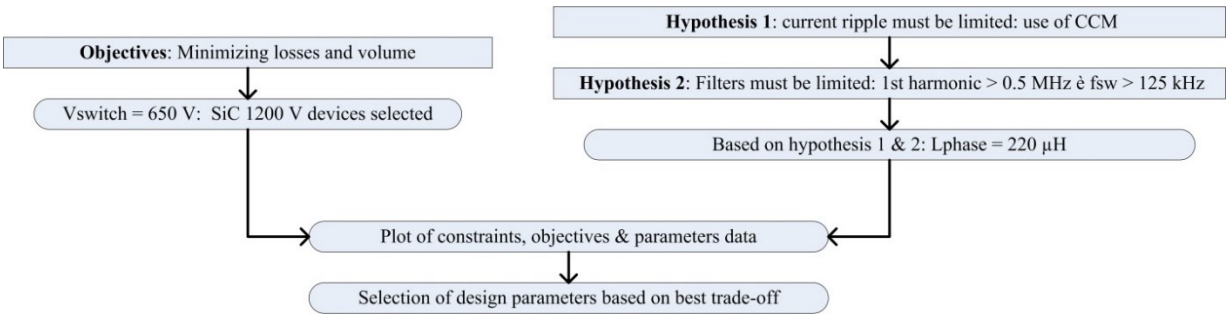


Figure *5*: Design of IBC using sequential method summary

This methodology based on literature review, experience and data analysis is quite simple to use. Finally, their converter reached a very good power density of 8 kW/L but this converter is not necessarily optimal.

This methodology has nevertheless the virtue of highlighting the critical design parameters of the IBC that are interdependent witch are: the cooling, the switching frequency, the current ripple in the phase inductor and switching devices.

III. A DESIGN USING GENETIC MULTI-OBJECTIVE OPTIMIZATION

The authors of [2] rightly pointed out that the architecture of the IBC, especially its number of phases, is a key design parameter to optimize both the power density and the efficiency of the converter. The design method is directed by that purpose.

A. Design method description

The converter conduction mode is limited to be continuous because DCM "yields to important constraints

especially on active components, in addition to more important core losses in the inductors".

For the others design parameters, the authors will use a heuristic nature inspired genetic algorithm named NSGA-II [6] to determine the optimal configuration (Figure *6*). With the number of phases and switching frequency, the different possible technologies of the IBC passives components greatly affect the volume of the converter. This is the reason why the authors put different technologies in the database of a same component.

This optimization is carried out on a purely analytical model of the converter (the authors excluded time simulation because of the effect on optimization time) for a single operating point (i.e. for an only one power value). The authors obtained the optimization results (Figure *7*) in 30 minutes (computation conditions unspecified).

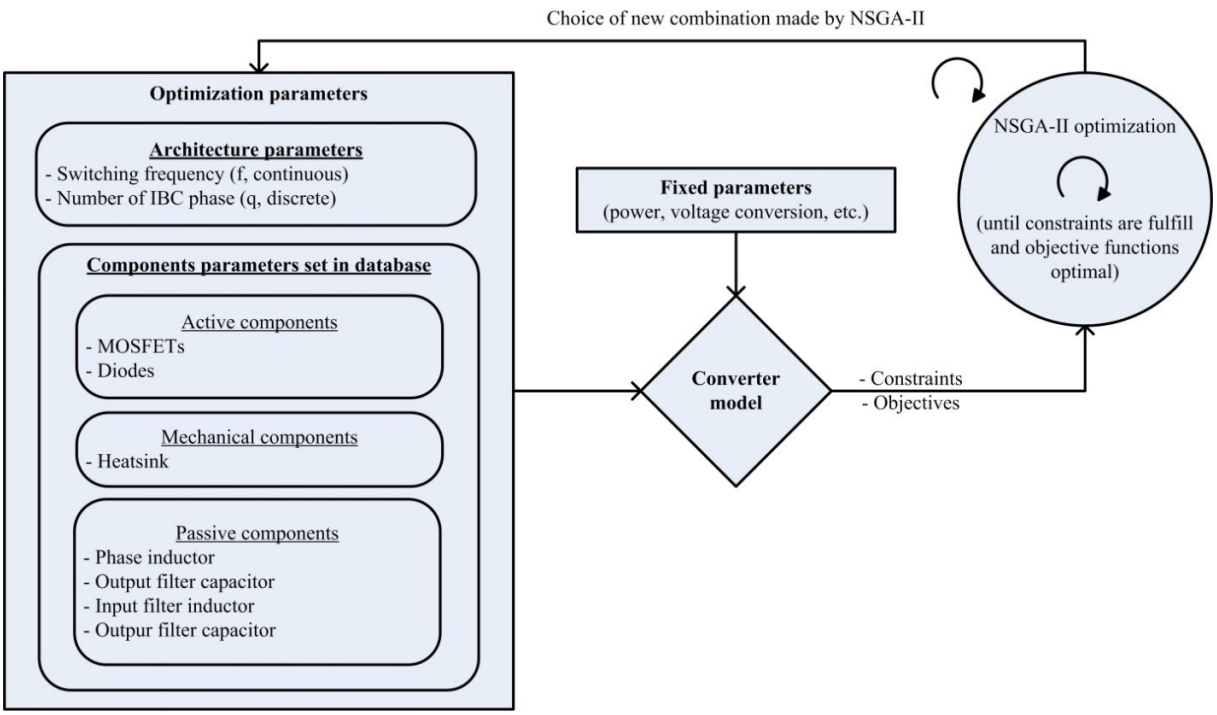


Figure *6*: Optimization approach from [2]

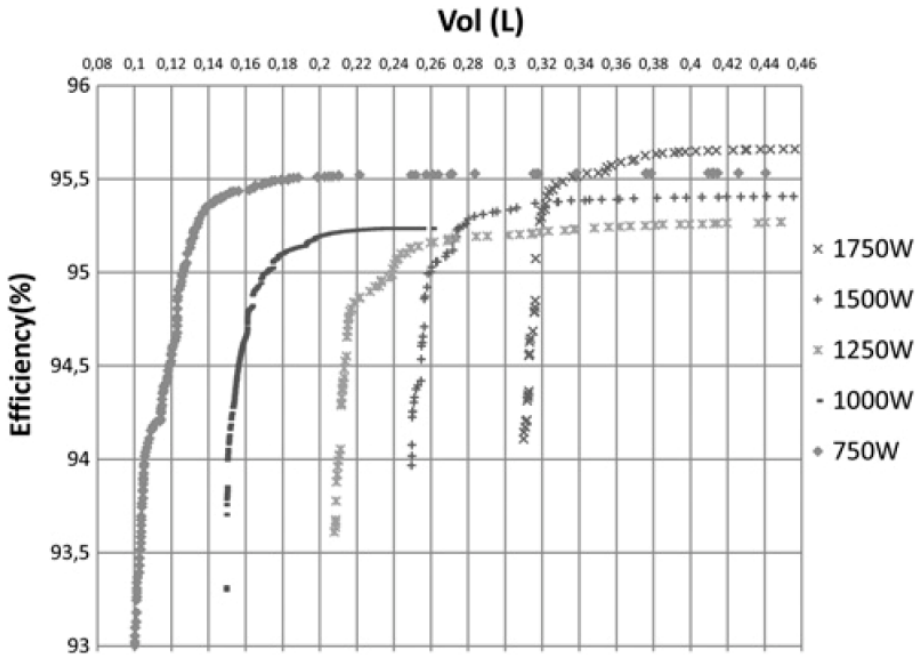


Figure *7*: Pareto evolution of the IBC from [2] according to converter power

B. Design method analysis

This method has the obvious advantage to give in a single run the converter optimal design: its prototype could be built directly based on the optimization results (no needs to run intermediate process since all components come from a database).

But the designers did not take into account simultaneously a range of operating points. Nevertheless the Pareto optimizations for different output power show the sensitivity of the design to this specification parameter. Besides, the Pareto curves traced with discrete design parameters, including discrete technologies for same component, present a pretty continuous shape.

IV. A DESIGN USING COMBINATORY EXPLORATION TECHNIC

The last illustrative design method [3], [4] has for objective to maximize the efficiency and the power density of the converter. The authors wonder if coupled inductors could help to gain some power density and if the added design complexity worth it. They also wonder about the optimal number of phases for each case. For the 100 kW converter of [4], three different configurations are considered [3]: 3 phases with single inductors (3P-DI), 4 phases with single inductors (4P-DI) and 4 phases with coupled inductors (4P-IPT).

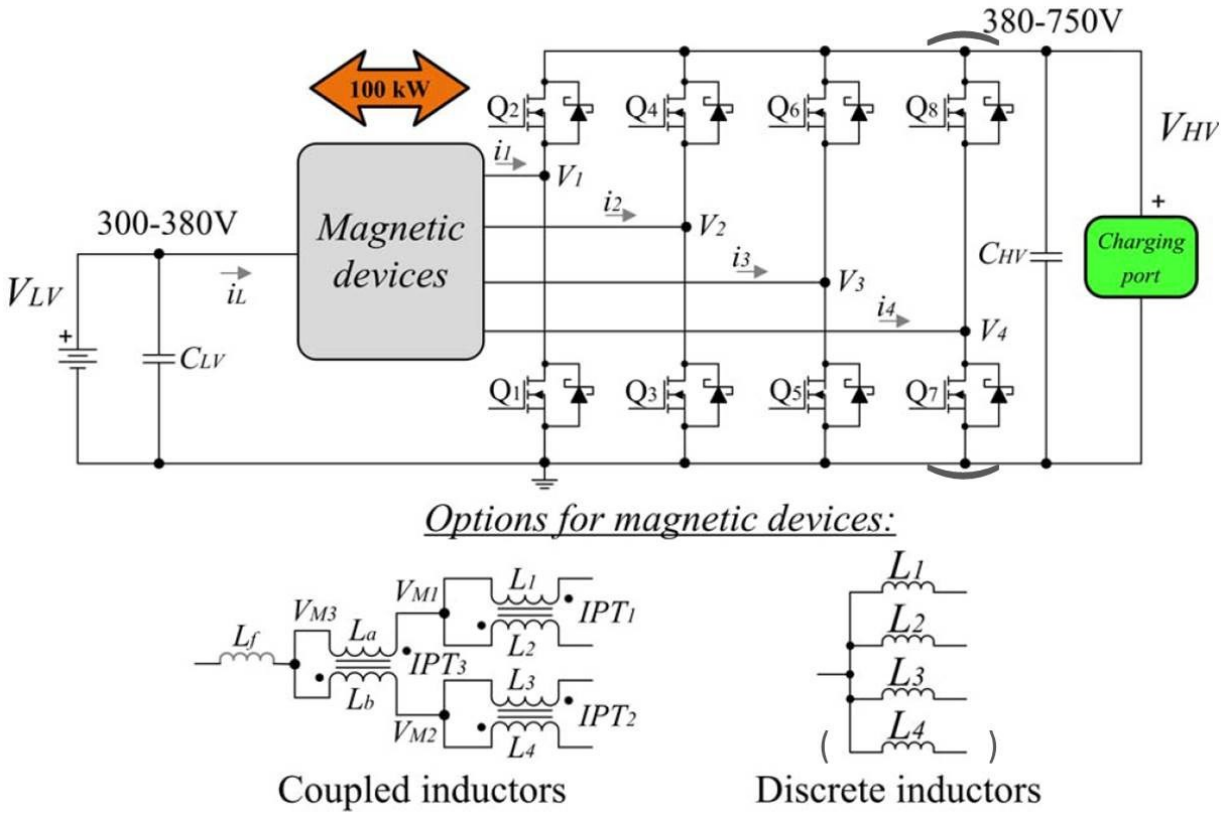


Figure *8*: Schematic from [4] of the DC-DC converter with different magnetics topologies

A. Design method description

To evaluate the gain of the use of coupled inductors, the authors compared the power density of each optimized configuration. These optimizations have been made with Chen's rearrangement for explicit enumeration for integer programming problems [7]. In other (comprehensive) words, the authors used an algorithm allowing testing almost all possible combinations of their concepts tree with discrete parameters. Table *2* presents the design problem formulation of the 100 kW IBC.

The switching frequency (that is naturally continuous) had to be discretized in to 14 discrete values (every 10 kHz, which is reasonable). The semi-conductors are not optimized for this converter, but was an optimization parameter for [3]. Finally, the design space of the 100 kW IBC is 13.65 million, i.e. there are 13.65 million possible designs. For computation time and problem understanding reasons, the authors preferred to run 3 optimizations: one for each topology. The optimization results of each topologies will be so compared manually. Thanks to this decision and Chen's rearrangement algorithm, the number of feasible designs drops to 52656. Finally, for the 3P-DI the computation time was 13 minutes when implemented in MATLAB on a 64-bit PC with a 3.4 GHz Intel Core i7 processor and 16 GB RAM.

Table *2*: Optimization problem formulation of the 100 kW IBC from [4]

Variable	Range of values
Coupled inductor topology	
IPT_1, IPT_2 core type	Finemet F3CC series: F3CC06.3 - 0125
IPT_3 core type	Finemet F3CC series: F3CC06.3 - 0125
IPT_1, IPT_2 turns	{4, 8, ..., 24}
IPT_3 turns	{4, 8, ..., 24}
IPT_1, IPT_2 foil thickness	{0.2, 0.25, 0.3} mm
IPT_3 foil thickness	{0.4, 0.5, 0.6} mm
Discrete inductor topology	
$L_1 - L_4$ core type	Finemet F3CC series: F3CC06.3 - 0125
$L_1 - L_4$ turns	{2, 4, ..., 24}
$L_1 - L_4$ gap length	{2, 3, ..., 6} mm
$L_1 - L_4$ foil thickness	{0.1, 0.15, 0.2, 0.25, 0.3} mm
Both topologies	
Switching frequency	{20, 30, ..., 150} kHz
Low-side capacitor type	EPCOS Ceralink
No. low-side capacitors	{1, 2, ..., 5}
High-side capacitor type	TDK B3277 series
No. high-side capacitors	{1, 2, ..., 5}

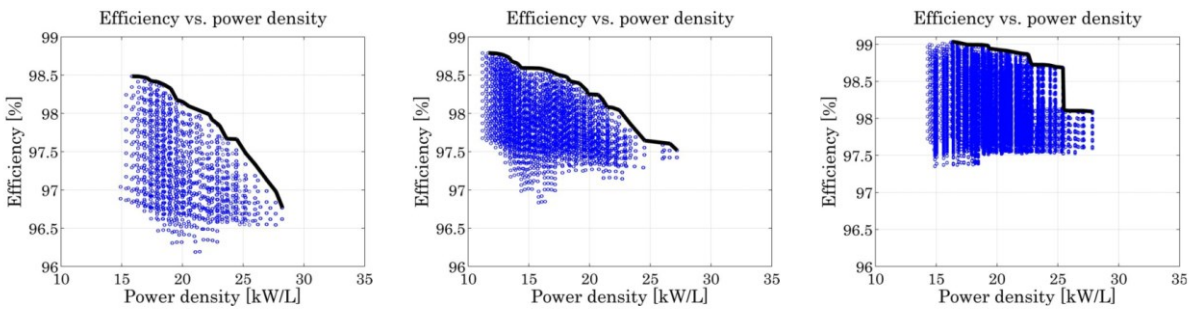
Nominal converter specifications

Low-side voltage range, V_{LV}	300 - 380 V
High-side voltage, V_{HV}	750 V
Output power, P	100 kW

Constrained quantities and their nominal limits

Quantity	Nominal limit
Window fill factor	≤ 0.7
Current density	≤ 10 A/mm^2
Peak flux density	≤ 1.1 T
Core temp.	≤ 155°C or 180°C
Junction temp.	≤ 150°C
Low-side voltage ripple	$\leq 2\%$ of V_{LV}
High-side voltage ripple	$\leq 2\%$ of V_{HV}

The optimization results are presented in Figure *9*. The optimizations are again done with analytical models of the IBC: analytical models are always preferred for optimization procedures.



(a) Three-phase discrete inductor topology. (b) Four-phase discrete inductor topology. (c) Four-phase coupled inductor topology.

Figure *9*: Feasible and Pareto-optimal designs for the three topologies under investigation in terms of efficiency and power density with Tcore ≤ 155 °C from [4]

B. Design method analysis

The design method provided in [3], [4] is very efficient thanks to a smart enumeration algorithm but mainly thanks to a clever problem formulation. The authors preferred to optimize with discrete variables with the arguments that it better fits with power electronics field. But by the author's confession, the algorithm main task is finding solutions that fulfill the constraint instead of looking for the optimal. It is maybe why the authors run the optimization on a single operating point. It can be observed that the Pareto curves of the single inductor IBC topologies are almost continuous. On the other hand the Pareto curve for the coupled inductors topology 4P-IPT is absolutely not.

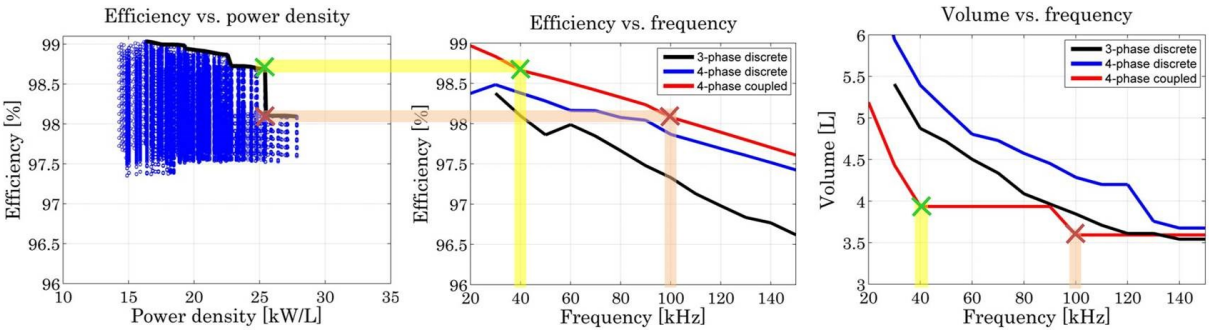


Figure *10*: Pareto sudden drop explanation from [4]

The efficiency sudden drop can be explained with Figure *10* by the fact that between 40 kHz and 90 kHz, the converter volume stays constant. The authors explained this by "*the fact that whilst the volume of the converter is largely dominated by the modules* (the switching modules) *and the cold plate, meaning that the overall dimensions of the converter are relatively insensitive to changes in the magnetic dimensions, the mass density of the magnetic components is much higher than the modules and cold plate, meaning the total weight of the converter is comparatively sensitive to changes in the magnetic weight*.". Actually, the module and the heatsink should have been included in the optimization if a continuous Pareto front was desired.

V. Conclusion

In this chapter, a quick review of three different IBC design methods has been presented. These non-exhaustive examples notably allow highlighting the design parameters of the interleaved Buck or Boost topologies that are interdependent and influence the converter power density and efficiency. They are listed below:

- The IBC number of phases
- The switching frequency
- The phase inductor values
- The semi-conductor choice
- The cooling system efficiency (i.e. thermal resistance)

This list is absolutely not surprising from a power electronics designer point of view. Nonetheless we should also realize that sequential method cannot be applied to optimize a converter in its whole if design time resource is limited. It shows the interest of simultaneous optimization of power, filtering and mechanical parts.

Also, the cited paper show the advantage of using an algorithm handling discrete variables: the optimal converter with real components can be directly assembled. The drawback of such algorithm is that to avoid the

combinatorial explosion the optimization problem size must be limited and so design parameters number and/or range.

That are concrete examples that show the interest of using gradient-based optimization methods for preliminary design phases in the aim to keep the advantage of having a large degree of freedom.

VI. References

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Appendix 2: Components parameters evaluation and IBC waveforms models capitalization

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SiC power MOSFET parameters evaluation model

Subject:
This appendix gives the equations to obtain the parameters of a power SiC MOSFET from CREE C2MXXXX120D serie:
- C2M0280120D, C2M0160120D, C2M0080120D, C2M0040120D, C2M0025120D

Note:
Mathcad having some difficulties to handle the °C, all temperature data are expressed in K BUT are actually in °C

1. Input design variables

0. Thermal data

MOSFET supposed junction temperature $Tj_mos := 25 \cdot K$ *So actually : Tj_mos = 25 °C*

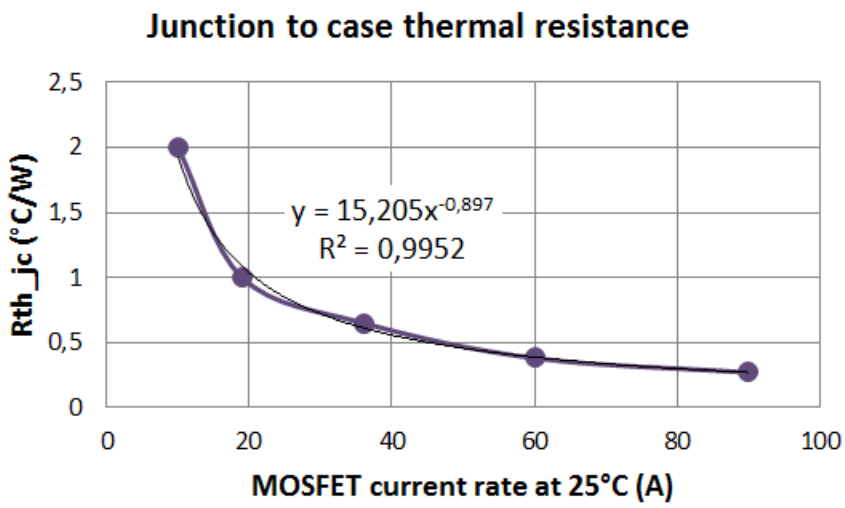
1. MOSFET selection variable

MOSFET current rate @ 25 °C: $cal_Imos := 60 \cdot A$

1. Output variables computation

0. MOSFET thermal parameters:

MOSFET junction to case thermal resistance: $Rth_jc_mos := 15.205 \cdot \frac{K}{W} \cdot \left(\frac{cal_Imos}{A}\right)^{-0.897} = 0.386 \cdot \frac{K}{W}$

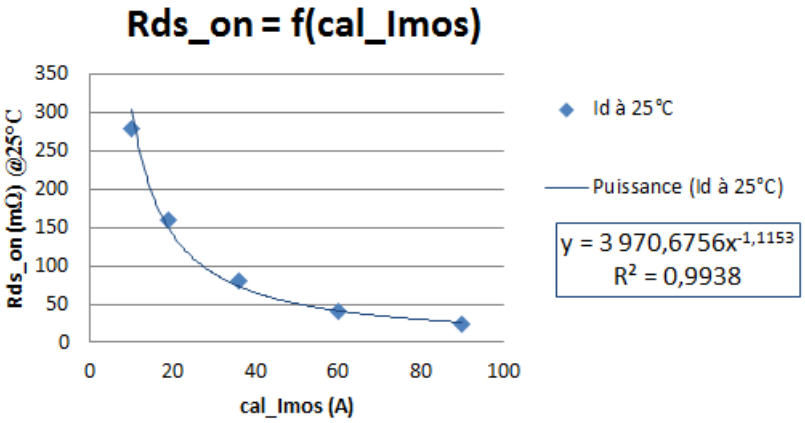


Thermal exchange surface (TO-247 case):

$$Smos := 16.25 \cdot 12.38 \cdot mm^2 - \pi \cdot \frac{(7.18mm)^2}{4} = 1.607 \cdot cm^2$$

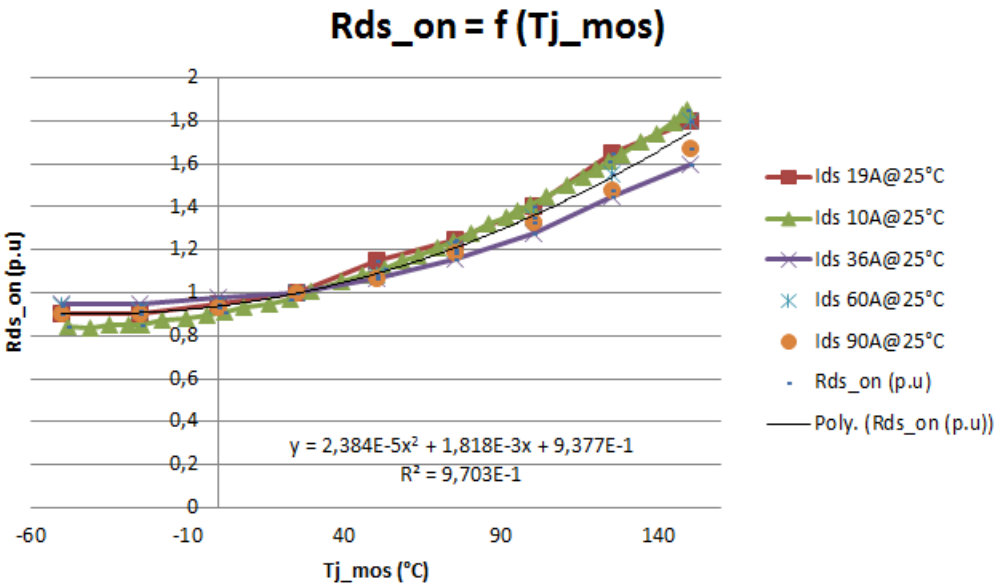
1. MOSFET electrical static parameters:

MOSFET ON state resistance @ 25°C: $Rds_on_25 := 3.9706756 \cdot \Omega \cdot \left(\frac{cal_Imos}{A}\right)^{-1.1153} = 0.041 \cdot \Omega$



MOSFET ON state resistance @Tj_mos:

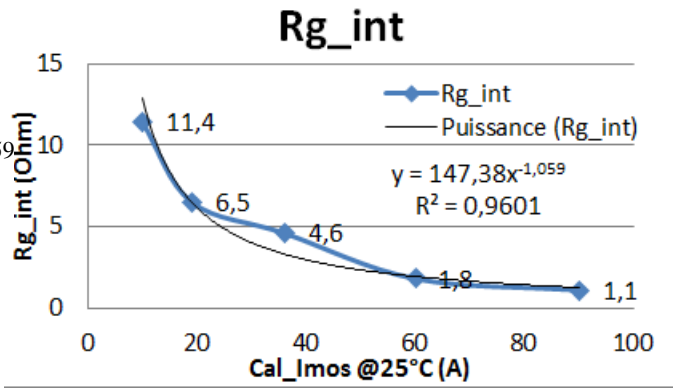
$$Rds_on := Rds_on_25 \cdot \left(\frac{2.384 \cdot 10^{-5}}{K^2} \cdot Tj_mos^2 + \frac{1.818 \cdot 10^{-3}}{K} \cdot Tj_mos + 0.9377\right) = 0.041\,\Omega$$



Internal gate resistance:

$$Rg_int := 147.38 \cdot \Omega \cdot \left(\frac{cal_Imos}{A}\right)^{-1.059}$$

$Rg_int = 1.929\,\Omega$



MOSFET weight: $Masse_mos := 6 \cdot gm$

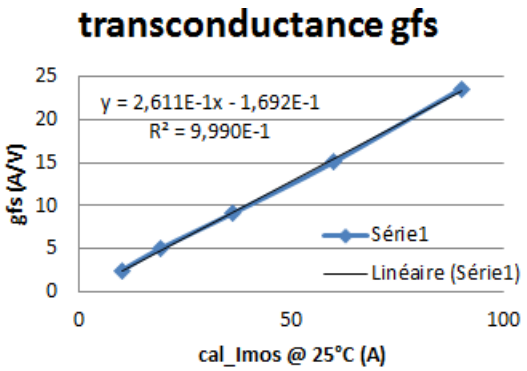
2. MOSFET electrical dynamic parameters:

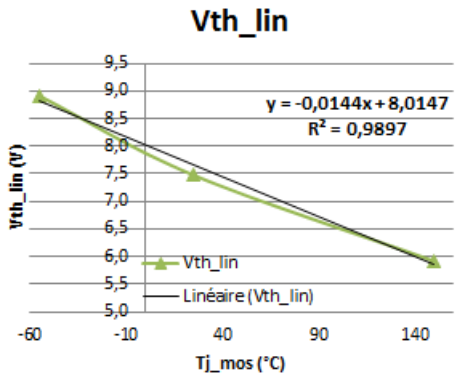
For the switching cell losses model, the transfer characterisitic of the MOSFET can be either linear or quadratic depending on the drain current value durong the commutation (for low ones: quadratic)

For the linear transfer function:

transconductance: $gfs := 0.2611 \cdot V^{-1} \cdot cal_Imos - 0.1692 \cdot S = 15.497 \cdot S$

Linear threshold voltage: $Vth_lin := 0.0144 \cdot \frac{V}{K} \cdot Tj_mos + 8.0147 \cdot V = 8.375\,V$

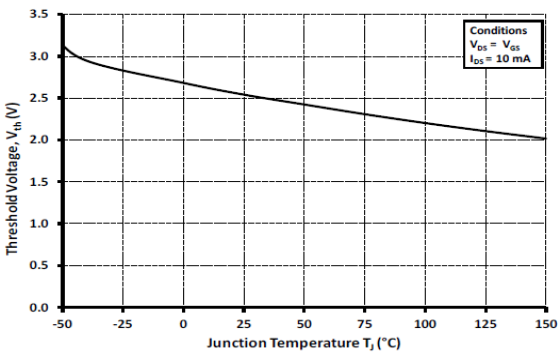


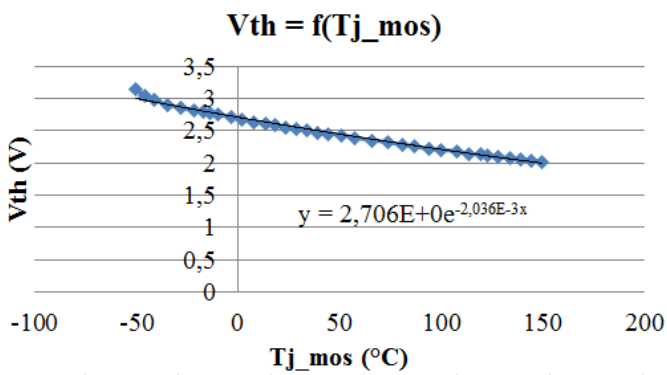


For the quaratic transfer function:

Threshold voltage: $Vth := 2.718 \cdot V \cdot \exp\left(\frac{-2.04 \cdot 10^{-3}}{K} \cdot Tj_mos\right) = 2.583\,V$

This threshold voltage is defined with the datasheet curve :





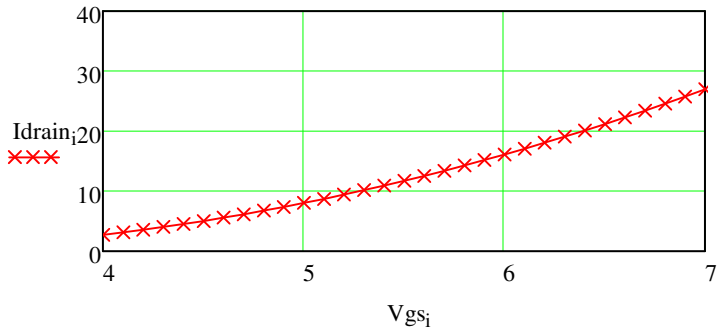
Quadratic characteristic coefficient Kfs:

$$aKfs := \frac{-2.113\cdot 10^{-7}}{A\cdot K\cdot V^2}\cdot cal_Imos^2 - \frac{1.5775\cdot 10^{-5}}{K\cdot V^2}\cdot cal_Imos - 3.28\cdot 10^{-4}\cdot\frac{A}{K\cdot V^2} = -2.035\times 10^{-3}\cdot\frac{A}{K\cdot V}$$

$$bKfs := \frac{2.157\cdot 10^{-4}}{A\cdot V^2}\cdot cal_Imos^2 + \frac{6.307\cdot 10^{-3}}{V^2}\cdot cal_Imos + 2.805\cdot 10^{-1}\cdot\frac{A}{V^2} = 1.435\cdot\frac{A}{V^2}$$

$$Kfs := aKfs\cdot Tj_mos + bKfs = 1.385\cdot\frac{A}{V^2} \qquad i := 0, 1 .. 70 \qquad Vgs_i := \frac{i}{10}\cdot V$$

$$Idrain_i := Kfs\cdot\left(Vgs_i - Vth\right)^2$$



It is quite different from the curve given in the datasheet, since the scale given in the datasheet is not convenient: the threshold voltage is given for few mA when the gradutation is in A. It conducts into a bad interpolation. Besides, the curve given in the datasheet is for Vds=Vgs<20V while we use these parameters for Vds > 200 V... So it is not really meticulous but it seems that the model gives quite good results so it may not have a lot of influence...

<u>Intrinsic MOSFET capacitances:</u>

when the MOSFET drain-source voltage is lower than threshold voltage, we consider:

Input capacitance value is: $Ciss0 := 49.842\cdot\frac{pF}{A}\cdot cal_Imos - 153.28\cdot pF = 2.837\cdot nF$

Output capacitance value is: $Coss0 := 43.229\cdot\frac{pF}{A}\cdot cal_Imos - 152.99\cdot pF = 2.441\cdot nF$

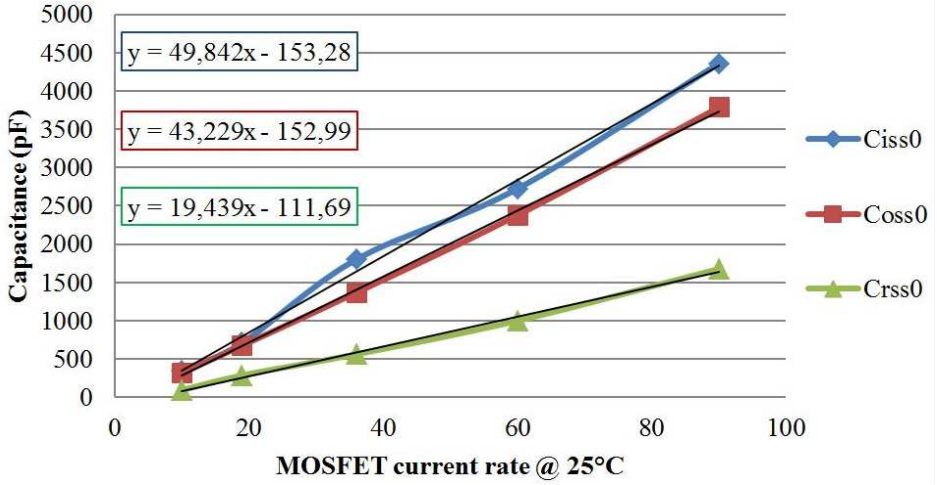
Transfer capacitance value is: $Crss0 := 19.439\cdot\frac{pF}{A}\cdot cal_Imos - 111.69\cdot pF = 1.055\cdot nF$

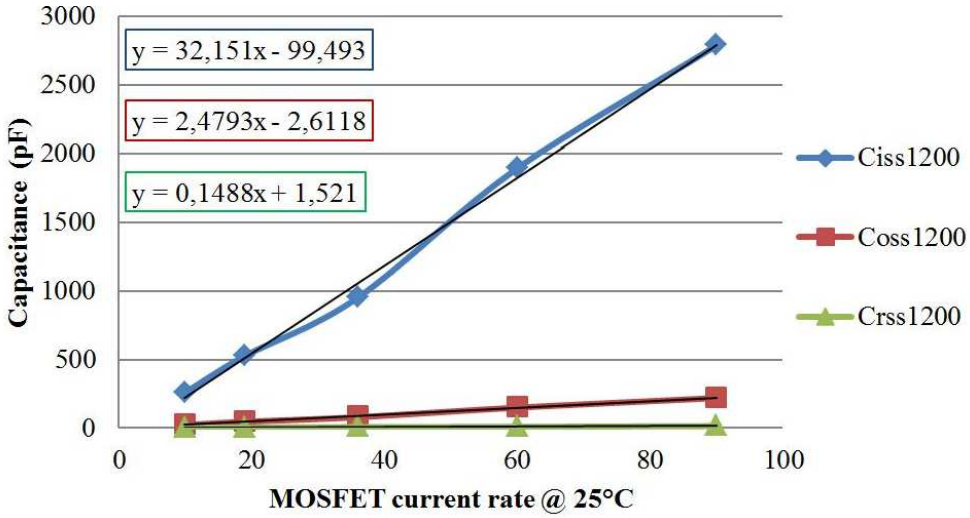
when the MOSFET drain-source voltage is higher than threshold voltage, we consider:

Input capacitance value is: $Ciss1200 := 32.151\cdot\frac{pF}{A}\cdot cal_Imos - 99.493\cdot pF = 1.83\cdot nF$

Output capacitance value is: $Coss1200 := 2.4793\cdot\frac{pF}{A}\cdot cal_Imos - 2.6118\cdot pF = 146.146\cdot pF$

Transfer capacitance value is: $Crss1200 := 0.1488\cdot\frac{pF}{A}\cdot cal_Imos + 1.521\cdot pF = 10.449\cdot pF$


y = 49,842x - 153,28
y = 43,229x - 152,99
y = 19,439x - 111,69
Capacitance (pF)
MOSFET current rate @ 25°C
Ciss0
Coss0
Crss0


y = 32,151x - 99,493
y = 2,4793x - 2,6118
y = 0,1488x + 1,521
Capacitance (pF)
MOSFET current rate @ 25°C
Ciss1200
Coss1200
Crss1200

Diode parameters evaluation model

Subject:
This appendix gives the equations to obtain the parameters of a power SiC Schottky diode serie from CREE C4DXX120D serie :
- C4D10120D, C4D20120D, C4D30120D, C4D40120D, **considering that only one or both of the 2 diodes in the package are connected.**

Note:
Mathcad having some difficulties to handle the °C, all temperature data are expressed in K BUT are actually in °C

1. Input design variables

0. Thermal data

Diode supposed junction temperature $Tj_diode := 25 \cdot K$ *So actually : Tj_diode = 25 °C*

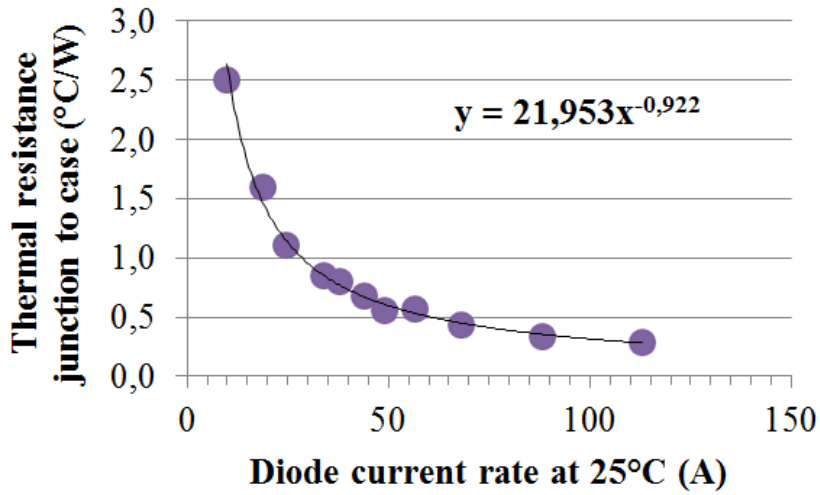
1. Diode selection variable

Diode current rate @ 25 °C: $cal_Idiode := 38 \cdot A$ (C4D10120D with both chips)

1. Output variables computation

0. Diode thermal parameters:

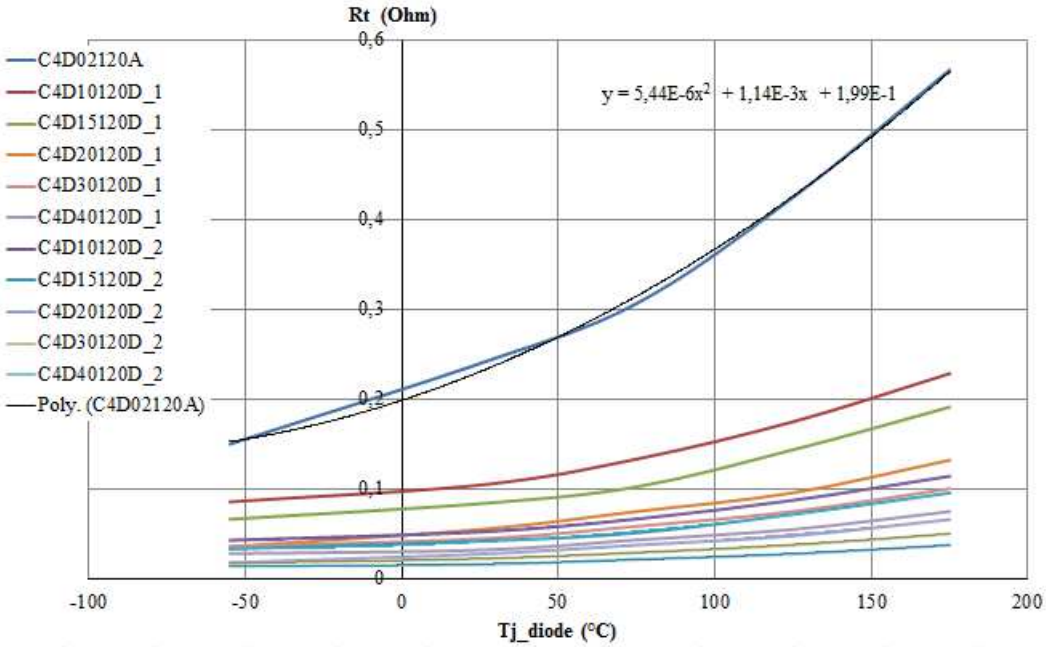
Diode junction to case thermal resistance: $Rth_jc_diode := 21.953 \cdot \frac{K}{W} \cdot \left(\frac{cal_Idiode}{A}\right)^{-0.922} = 0.767 \cdot \frac{K}{W}$



Thermal exchange surface (TO-247 case): $Sdiode := 16.25 \cdot 12.38 \cdot mm^2 - \pi \cdot \frac{(7.18mm)^2}{4} = 1.607 \cdot cm^2$

1. Diode electrical static parameters:

Diode ON state resistance



$$aRt := 2.54 \cdot 10^{-5} \cdot \frac{\Omega}{K^2} \cdot \left(\frac{cal_Idiode}{A}\right)^{-0.828} = 1.25 \times 10^{-6} \cdot \frac{\Omega}{K^2}$$

$$bRt := 6.09 \cdot 10^{-3} \cdot \frac{\Omega}{K} \cdot \left(\frac{cal_Idiode}{A}\right)^{-0.99} = 1.662 \times 10^{-4} \cdot \frac{\Omega}{K}$$

$$cRt := 9.78 \cdot 10^{-1} \cdot \Omega \cdot \left(\frac{cal_Idiode}{A}\right)^{-0.857} = 0.043\,K \cdot \frac{\Omega}{K}$$

$$Rt := aRt \cdot Tj_diode^2 + bRt \cdot Tj_diode + cRt = 0.048\,\Omega$$

Voltage drop during the diode ON state Vt.
It depends only on the diode voltage rating (fixed to 1200 V here) and on the junction temperature:

$$Vt := -1.63 \cdot 10^{-3} \cdot \frac{V}{K} \cdot Tj_diode + 0.9665 \cdot V = 0.926\,V$$

Diode weight: $Diode_weight := 5.42 \cdot gm$

2. Diode electrical dynamic parameters:

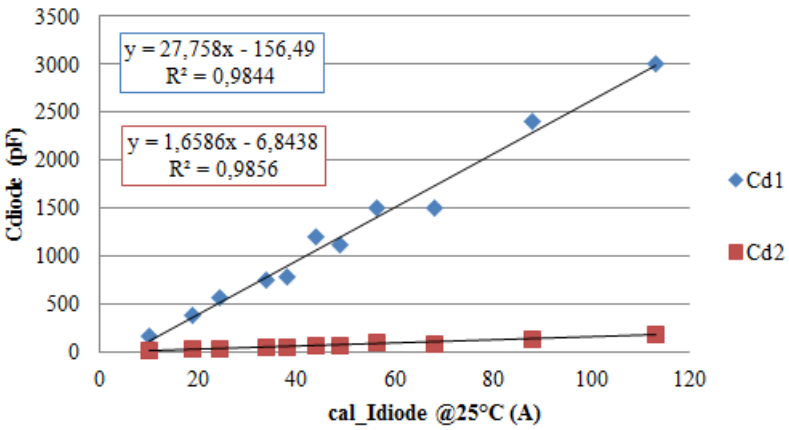
Intrinsic Diode capacitance:

when the diode reverse voltage is low (around 0):

Diode capacitance is: $Cd1 := 27.114 \cdot \frac{pF}{A} \cdot cal_Idiode - 112.32 \cdot pF = 918.012 \cdot pF$

when the diode reverse voltage is high (around 400 V)

Diode capacitance is: $Cd2 := 1.6209 \cdot \frac{pF}{A} \cdot cal_Idiode - 4.2418 \cdot pF = 57.352 \cdot pF$



Filtering ceramic capacitors parameters evaluation Model

Subject:
This appendix gives the equations to obtain the parameters of the selected filtering capacitors of the IBC from AVX High voltage MLC radials SV style X7R serie 1500 V

1. Input design variables

0. Number of capacitors and capacitor choices

Number of capacitors set in parallel: $N_Cer := 5$

Nominale value of the (single) capacitor $Cer := 0.27 \cdot \mu F$

1. IBC data

Number of phases: $Nphase := 3$ Switching frequency: $Fs := 157 \cdot kHz$ $i := 1 .. 10$

Looked frequencies: $f_i := Nphase \cdot Fs \cdot i = ...$

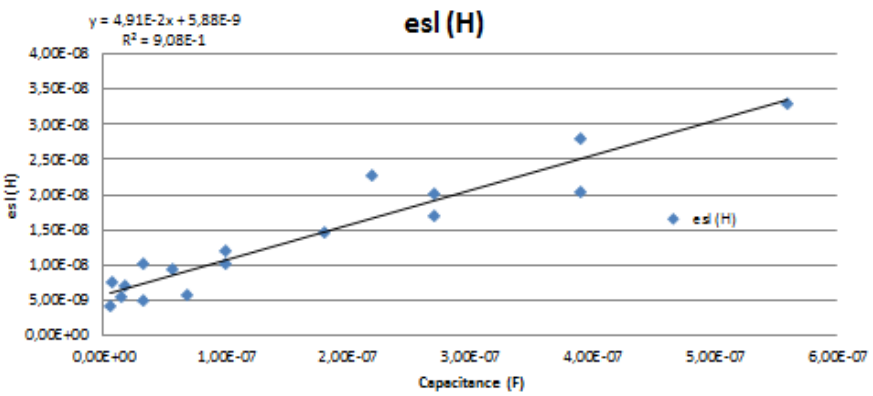
2. Output variables computation

0. Electrical paramaters of the total capacitance:

Total capacitance:

$$CersTot := Cer \cdot N_Cer = 1.35 \cdot \mu F$$

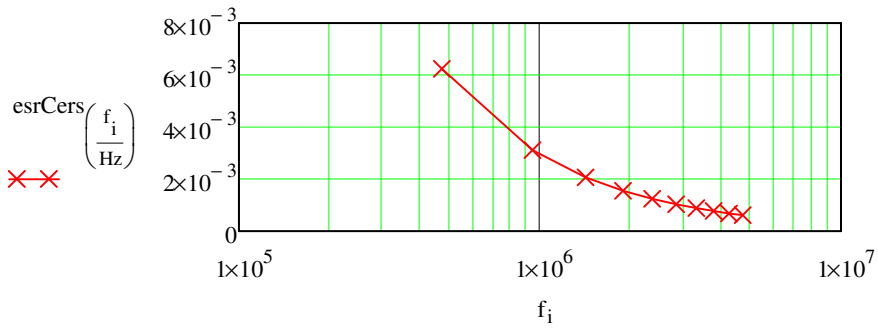
Capacitor parasitic serie inductance:



$$eslCers := \frac{4.91 \cdot 10^{-2} \cdot H \cdot \frac{Cer}{F} + 5.88 \cdot 10^{-9} \cdot H}{N_Cer} = 3.827 \times 10^{-9} \cdot H$$

Dissipaction factor: $\text{tanDCer} := \frac{2.5}{100}$

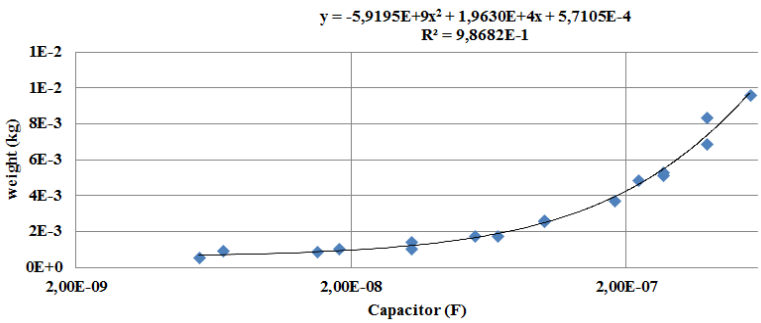
Capacitor parasitic serie resistance: $\text{esrCers}\left(\frac{f_i}{Hz}\right) := \frac{\text{tanDCer}}{2\cdot\pi\cdot f_i\cdot \text{Cer}\cdot \text{N_Cer}}$



1. Weight and surface parameters:

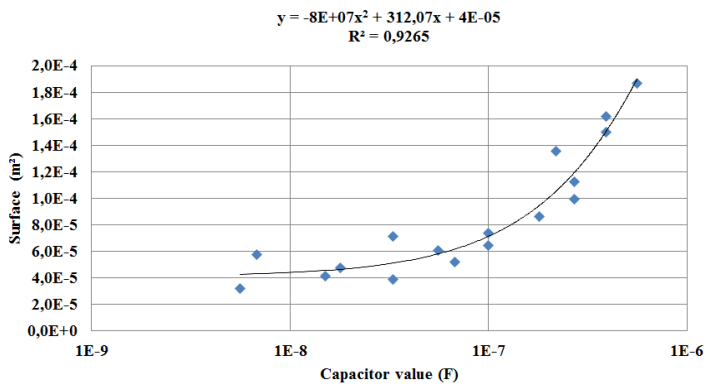
Total weight of filtering capacitors:

$$\text{WeightCers} := \text{N_Cer}\cdot\left[-5.9195\cdot 10^{9}\cdot kg\cdot\left(\frac{\text{Cer}}{F}\right)^{2} + 1.963\cdot 10^{4}\cdot kg\cdot\frac{\text{Cer}}{F} + 0.57105\cdot gm\right] = 27.198\cdot gm$$



Total surface of the filtering capacitors (needed to compute PCB weigth):

$$\text{surfaceCers} := \text{N_Cer}\cdot\left[-8.2876\cdot 10^{7}\cdot m^{2}\cdot\left(\frac{\text{Cer}}{F}\right)^{2} + 3.1207\cdot 10^{2}\cdot m^{2}\cdot\frac{\text{Cer}}{F} + 40.988\cdot mm^{2}\right] = 5.96\cdot cm^{2}$$



Filtering film capacitors parameters evaluation Model

Subject:
This appendix gives the equations to obtain the parameters of the selected filtering output capacitor of the IBC from Kemet R75 Series Single Mettalized Polypropylene Film Radial 630 V

1. Input design variables

0. Number of capacitors and capacitor choices

Number of capacitors set in parallel: $N_Film := 3$

Nominale value of the (single) capacitor $CFilm := 0.01 \cdot \mu F$

1. IBC data

Number of phases: $Nphase := 3$ Switching frequency: $Fs := 157 \cdot kHz$ $i := 1 .. 10$

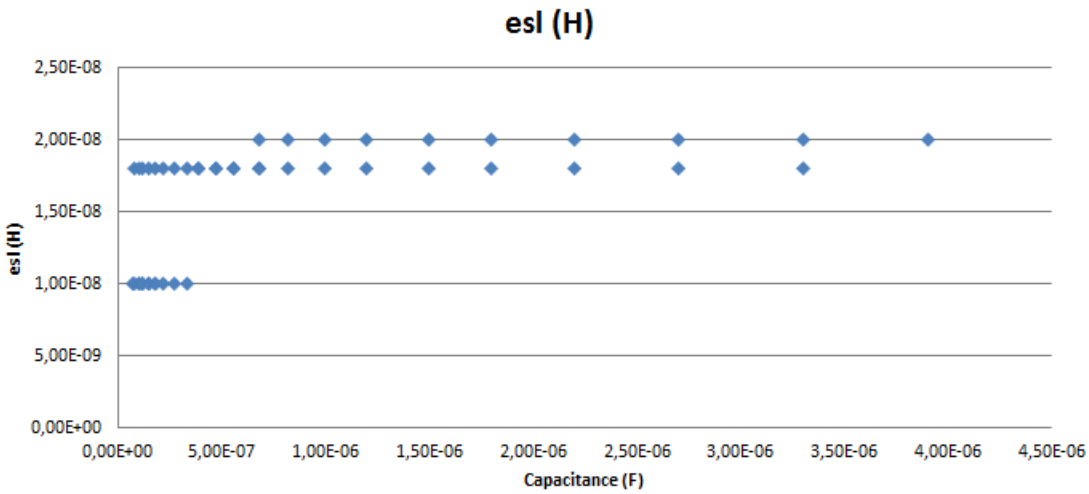
Looked frequencies: $f_i := Nphase \cdot Fs \cdot i = ...$

2. Output variables computation

0. Electrical paramaters of the total capacitance:

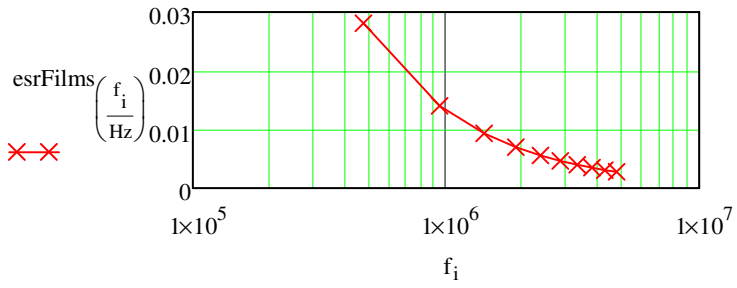
Total capacitance: $FilmsTot := CFilm \cdot N_Film = 0.03 \cdot \mu F$

Capacitor parasitic serie inductance: (worst case) $eslFilms := \frac{19 \cdot 10^{-9} \cdot H}{N_Film} = 6.333 \times 10^{-9} \cdot H$



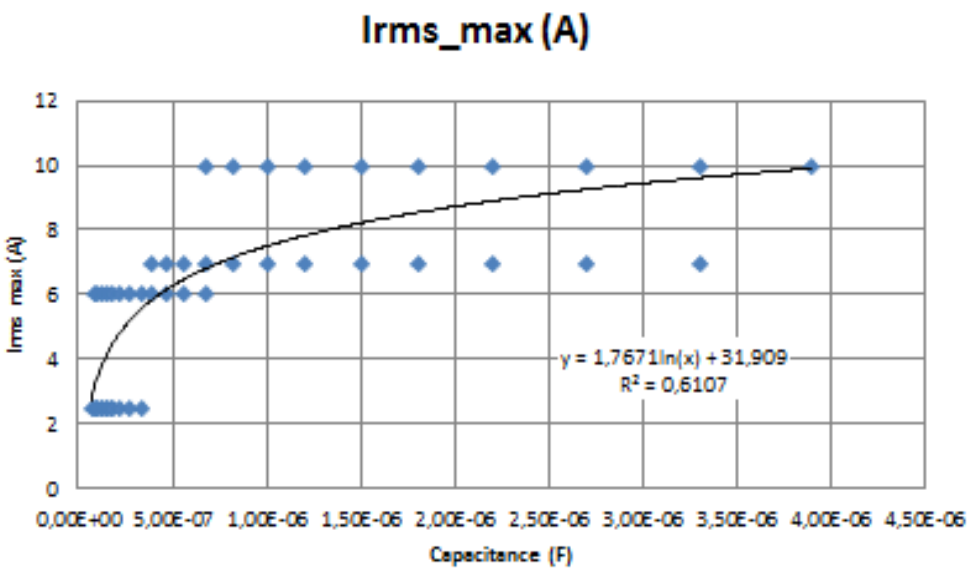
Dissipaction factor: $\text{tanDFilm} := \frac{0.25}{100}$

Capacitor parasitic serie resistance: $\text{esrFilms}\left(\frac{f_i}{\text{Hz}}\right) := \frac{\text{tanDFilm}}{2\cdot\pi\cdot f_i\cdot\text{CFilm}\cdot\text{N_Film}}$



Maximum RMS current in all capacitors togethers:

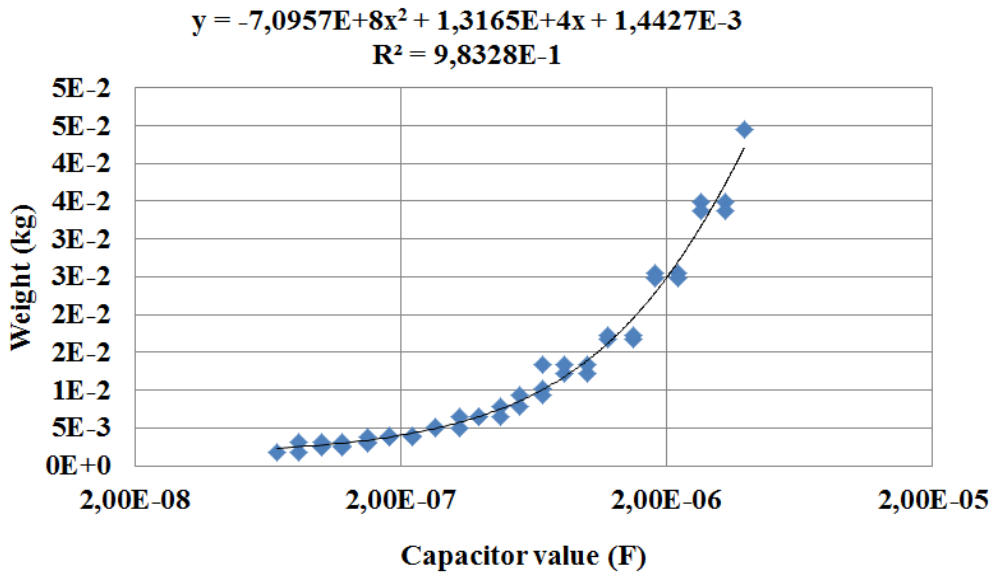
$$\text{Irms_max_Films} := \text{N_Film}\cdot\left(1.7671\cdot\text{A}\cdot\ln\left(\frac{\text{CFilm}}{\text{F}}\right) + 31.909\cdot\text{A}\right) = -1.927\,\text{A}$$



1. Weight and surface parameters:

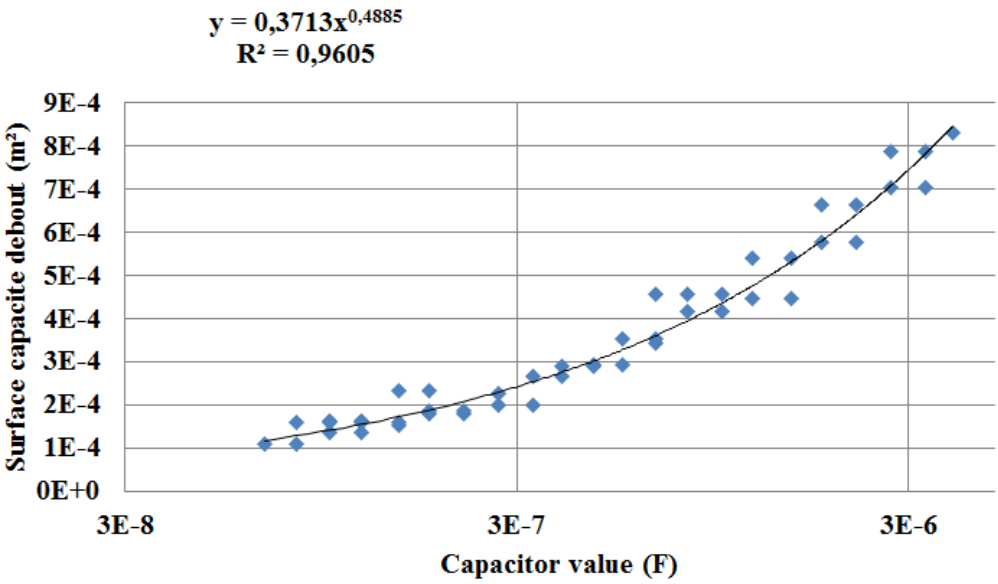
Total weight of filtering capacitors:

$$WeightCers := N_Film \cdot \left[-7.0957 \cdot 10^{8} \cdot kg \cdot \left(\frac{CFilm}{F} \right)^{2} + 1.3165 \cdot 10^{4} \cdot kg \cdot \frac{CFilm}{F} + 1.4427 \cdot gm \right] = 4.723 \cdot gm$$



Total surface of the filtering capacitors:

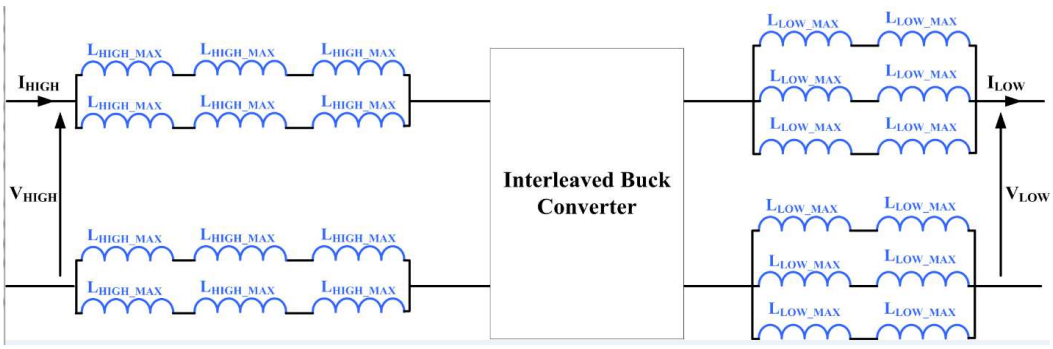
$$surfaceCers := N_Film \cdot \left[0.3713 \cdot m^{2} \cdot \left(\frac{CFilm}{F} \right)^{0.4885} \right] = 1.377 \cdot cm^{2}$$



Filtering inductor(s) parameters evaluation Model

Subject:
This appendix gives the equations to obtain the parameters of the selected filtering inductors of the IBC from Bourns SRP6540 serie

1. Input design variables



0. Number of inductors per line

Number of inductors set in serie: $Nis := 3$

Number of inductors set in parallele: $Nip := 2$

For the high side case on the previous figure

1. IBC data

DC current value in the line $Idc := 15 \cdot A$ For example Ihigh value here

2. Inductor choice in the Bourns serie

Nominal value of the (single) inductor:

$Lfilter_val_max := 2.2 \cdot \mu H$

This nominal value is actually the inductor inductance for a DC current of 0 A. It is also the maximal inductance of the inductor.
For example with SRP6540 - 1R0M inductor : his inductance decreases with the DC current. Below the equation to estimate the inductance under the DC current of the converter.

2. Output variables computation for a single inductor

0. Electrical paramaters of a single inductor:

Maximum current admissible by the inductor for 40°C rise.
Hypothesis : I_RMS = I_DC...

$$Idc_max_one := 7.0615 \cdot mA \cdot \left(\frac{Lfilter_val_max}{H}\right)^{-0.54612} = 8.682 \cdot$$

Inductor value at this maximum current:

$$Lfilter_val_min := 0.8562 \cdot H \cdot \left(\frac{Lfilter_val_max}{H}\right)^{1.0072} = 1.715 \cdot \mu H$$

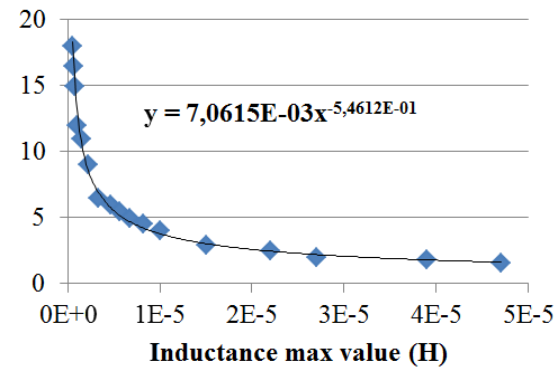
Inductor parasitic serie resistance:

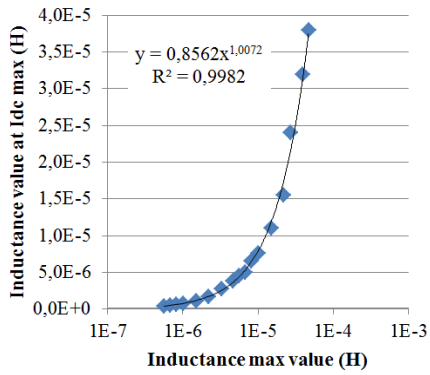
$$Lfilter_esr_one := 10578.0 \cdot \Omega \cdot \left(\frac{Lfilter_val_max}{H}\right)^{1.0299} = 0.016 \cdot \Omega$$

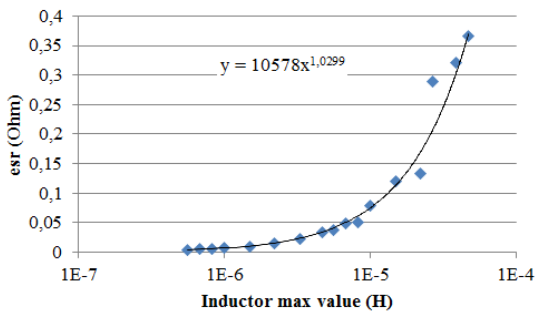
Inductor parasitic parallel resistance:

$$Lfilter_esrP_one := 3 \cdot K\Omega = 3 \times 10^{3} \cdot \Omega$$

(empiric)







DC current in a single inductor:

$$Idc_one := \frac{Idc}{Nip} = 7.5\,A$$

Constraint on the maximal current per inductor (for a 40°C rise):

$$const_Idc_filter := Idc_max_one - Idc_one = 1.182\,A$$

Value of a single inductor under the DC current:

$$Lfilter_val_one := \frac{Lfilter_val_min - Lfilter_val_max}{Idc_max_one} \cdot Idc_one + Lfilter_val_max = 1.781 \cdot \mu H$$

1. Weight and surface parameters:

Single inductor weight:

$$Lfilter_weight_one := 1.85 \cdot gm$$

Single inductor PCB surface:

$$Lfilter_surface_one := 7.2 \cdot mm \cdot 6.5 \cdot mm = 0.468 \cdot cm^{2}$$

3. Output variables computation for the all inductors

0. Electrical data:

Total value of the filtering inductors: $Lfilter_val := \frac{Nis}{Nip} \cdot Lfilter_val_one = 2.672 \cdot \mu H$

Total value of the serie resistance: $Lfilter_esr := \frac{Nis}{Nip} \cdot Lfilter_esr_one = 0.024\,\Omega$

Total value of the parallel resistance: $Lfilter_esrP := \frac{Nis}{Nip} \cdot Lfilter_esrP_one = 4.5 \cdot K\Omega$

1. Mass data:

Total weight of filtering inductors: $Lfilter_weight := Nis \cdot Nip \cdot Lfilter_weight_one = 11.1 \cdot gm$

Total surface of the filtering inductors: $Lfilter_surface := Nis \cdot Nip \cdot Lfilter_surface_one = 2.808 \cdot cm^2$

Power Inductor Model

Subject:
This appendix gives the quations to obtain the paarameters of the phase inductor. This component is made with :
- Iron powder toroidal core (frome Magnetics for the present data)
- Copper Litz wire

The inductor of this model is supposed to be potted in a resin that has two main functions:
- assuring the dielectric strenght of the inductor with the heat-sink
- allowing a sufficient disspipation of the heat to the heat-sink

Material references for the present example:
- inductor core : 77587 from Magntics (KoolMu26)
- Litz wire: from Le Guippage Moderne
- Resine: Reference not provided for confidentiality reasons

Note: Mathcad having some trouble to handle the unit "°C", all given temperatures will have for unit "K" but are actually "°C"

1. Input design variables

0. IBC data

Switching frequency : $Fs := 157 \cdot kHz$

IBC output current: $Ilow := 15 \cdot A$

IBC number of phases: $Nb_phases := 3$

1. Inductor core material properties data

For the KoolMu 26 material:

Nominal permeability: $muR_Lphase_nom := 26$

To compute the permeability drop as a function of the DC bias:

$a_mag := 1.0$ $\quad b_mag := -1.248 \cdot 10^{-3} \cdot \frac{cm}{A}$ $\quad c_mag := -2.02 \cdot 10^{-5} \cdot \left(\frac{cm}{A}\right)^2$

$d_mag := 8.354 \cdot 10^{-8} \left(\frac{cm}{A}\right)^3$ $\quad e_mag := -9.503 \cdot 10^{-11} \cdot \left(\frac{cm}{A}\right)^4$

To compute the permeability drop as a function of the flux frequency:

$a_freq := 0.0$ $\quad b_freq := -5.50 \cdot 10^{-3} \cdot \frac{1}{MHz}$ $\quad c_freq := 1.4 \cdot 10^{-3} \cdot \left(\frac{1}{MHz}\right)^2$

$d_freq := -6.2 \cdot 10^{-4} \left(\frac{1}{MHz}\right)^3$ $\quad e_freq := 3.7 \cdot 10^{-5} \cdot \left(\frac{1}{MHz}\right)^4$

To compute the permeability drop as a function of the core temperature:

$a_temp := -4.289 \cdot 10^{-3}$ $b_temp := 2.521 \cdot 10^{-4} \cdot \frac{1}{K}$ $c_temp := -3.557 \cdot 10^{-6} \cdot \left(\frac{1}{K}\right)^2$

$d_temp := 1.384 \cdot 10^{-8} \left(\frac{1}{K}\right)^3$ $e_temp := -2.066 \cdot 10^{-11} \cdot \left(\frac{1}{K}\right)^4$

$core_density := 0.86 \cdot \frac{25.0 \cdot 10^{-3} \cdot kg}{4150 \cdot 10^{-9} \cdot m^3} = 5.181 \times 10^3 \frac{kg}{m^3}$ core 77587 for computation

Core "desired" temperature: $TcoreLphase := (160) \cdot K$ *In reality: 160 °C*

Void permeability: $\mu 0 := \pi \cdot 4 \cdot 10^{-7} \cdot \frac{m}{A} \cdot T$

2. Inductor core geometric properties data

External diameter: $Lphase_Dout := 34.30 \cdot mm$

Internal diameter coefficient: $Const_Lphase_Diameters := 0.6822157$ must be [0.4 ; 0.7]

Height coefficient: $Const_Lphase_Height := 0.815596$ must be [0.75 ; 1.0]

3. Inductor winding properties data

Number of turns coefficient: $const_Lphase_turns := 1.0$ must be [0.9 ; 1.0] for the thermal model validity

Litz strand diameter: $Dlitz := 0.1 \cdot mm$

Litz strands number: $nstrandLphase := 125$

Litz connection lenght: $TotalConnectionLenght := 15 \cdot cm$

4. Resin properties data

Top thickness: $EresineTopLphase := 6.96 \cdot mm$

External thickness: $EresineExtLphase := 1.03 \cdot mm$

Internal thickness: $EresineIntLphase := 2.87 \cdot mm$

To determine bottom thickness:

Dielectric strenght to hold: $Vdielec_min := 9000 \cdot V$

Resin dieclectric nominal strenght: $Vdielec_resine := 19 \cdot \frac{kV}{mm}$

Resin density $resine_density := 2250 \cdot \frac{kg}{m^3}$

1. Output variables computation

0. IBC data

DC current: $I_Lphase_DC := \frac{Ilow}{Nb_phases} = 5\ A$

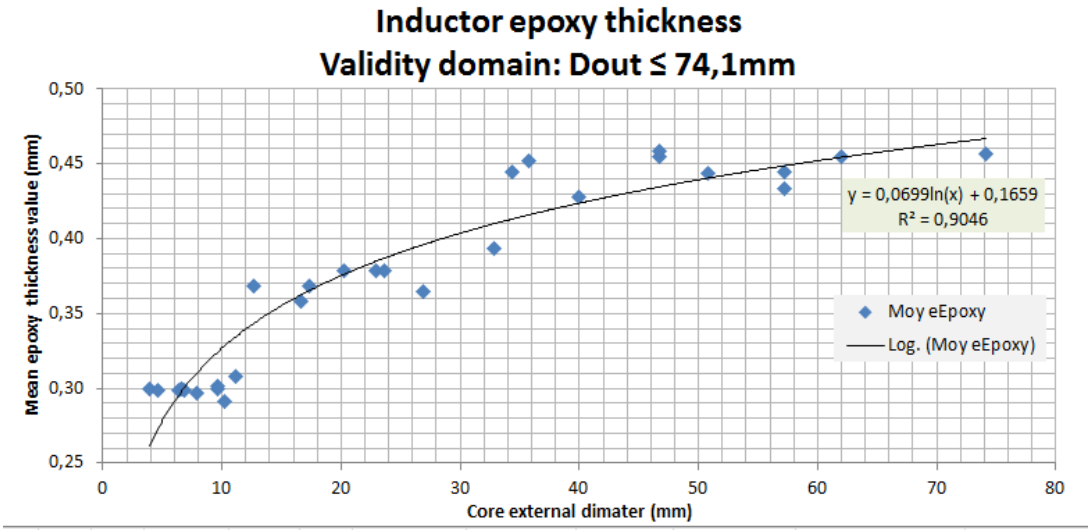
1. Inductor core geometric properties data

Internal diameter: $Lphase_Din := Const_Lphase_Diameters \cdot Lphase_Dout = 23.4 \cdot mm$

Height: $Lphase_H := Const_Lphase_Height \cdot (Lphase_Dout - Lphase_Din) = 8.89 \cdot mm$

Mean lenght: $Lphase_Le := \frac{\pi}{2} \cdot (Lphase_Dout + Lphase_Din) = 90.635 \cdot mm$

Cross section: $Lphase_Ae := Lphase_H \cdot \frac{(Lphase_Dout - Lphase_Din)}{2} = 48.45 \cdot mm^2$



Epoxy thickness: $eEpoxy := 0.0699 \cdot \ln\left(\frac{Lphase_Dout}{mm}\right) \cdot mm + 0.1659 \cdot mm = 0.413 \cdot mm$

2. Winding properties data

Litz wire strand section: $Slitz := \pi \cdot \frac{Dlitz^2}{4} = 7.854 \times 10^{-3} \cdot mm^2$

External dimater of Litz wire: $DextLitz := \frac{7.6647 \cdot 10^2}{m} \cdot Slitz \cdot nstrandLphase + 7.1728 \cdot 10^{-4} \cdot m = 1.47 \cdot mm$

Lenght of one wire turn:

Be:

$Dout := Lphase_Dout + eEpoxy$ $Din := Lphase_Din - eEpoxy$ $He := Lphase_H + eEpoxy$

$Lphase_Lturn := 2 \cdot He + (Dout - Din + 4 \cdot DextLitz) = 36.211 \cdot mm$ *Mean Lenght Turn*

Maximum number of turns: $Lphase_Nmax := 0.9 \cdot \frac{\pi \cdot (Din - DextLitz)}{DextLitz} = 41.394$

$Lphase_N := const_Lphase_turns \cdot Lphase_Nmax = 41.394$

Copper resistance computation:

Copper resistivity: $rhoCu := 17.5 \cdot 10^{-9} \cdot \Omega \cdot m$

Linear DC resistance: $Rs := \frac{rhoCu}{Slitz} = 2.228 \cdot \frac{\Omega}{m}$

Litz number of bunching (an average is taken): $nbunching := 2$

Litz number of cabling (an average is taken): $ncabling := 2$

Litz total lenght: $Litz_total_lenght := Lphase_N \cdot Lphase_Lturn + TotalConnectionLenght = 1.649\,m$

DC resistance: $RdcLitz := \frac{Litz_total_lenght \cdot Rs \cdot 1.015^{nbunching} \cdot 1.025^{ncabling}}{nstrandLphase} = 0.032\,\Omega$

AC resistance computation: empiric relation from New England Wire

For Fs<350 kHz: $Sac := 1.0$ For nstrand > 27 : $Kac := 2.0$

Eddy curent basis factor: Dlitz has to be expressed in inch unit

$$Gac := \left(\frac{\frac{Dlitz}{m} \cdot 39.370079 \cdot \sqrt{\frac{Fs}{Hz}}}{10.44} \right)^4 = 4.985 \times 10^{-4}$$

$$RacLitz := RdcLitz \cdot \left[Sac + Kac \cdot \left(\frac{nstrandLphase \cdot Dlitz}{DextLitz} \right)^2 \cdot Gac \right] = 0.034\,\Omega$$

3. Inductor core material properties data

Permeability drop computation:

Drop due to DC:

Magnetic DC field: $Lphase_Hfield := Lphase_N \cdot \frac{I_Lphase_DC}{Lphase_Le} = 2.284 \times 10^3 \frac{A}{m}$

Be: $x := Lphase_Hfield$

$muR_drop_mag := a_mag + b_mag \cdot x + c_mag \cdot x^2 + d_mag \cdot x^3 + e_mag \cdot x^4 = 0.962$

Drop due to switching frequency:

$muR_drop_freq := 1 + a_freq + b_freq \cdot Fs + c_freq \cdot Fs^2 + d_freq \cdot Fs^3 + e_freq \cdot Fs^4 = 0.999$

Drop due to core temperature:

Be: $T := TcoreLphase = 160 \cdot K$ *Actually it is in °C*

$muR_drop_temp := 1 + a_temp + b_temp \cdot T + c_temp \cdot T^2 + d_temp \cdot T^3 + e_temp \cdot T^4 = 0.988$

Finally:

$muR_Lphase := muR_Lphase_nom \cdot muR_drop_mag \cdot muR_drop_freq \cdot muR_drop_freq = 24.969$

Constraint on the saturation

$Lphase_saturation_constraints := \frac{muR_Lphase}{muR_Lphase_nom} = 96.034 \cdot \%$ Should be > 80%

Inductance factor value: $Lphase_Al := 0.92 \cdot \mu 0 \cdot muR_Lphase \cdot \frac{Lphase_Ae}{Lphase_Le} = 1.543 \times 10^{-8} \cdot \frac{H}{turn^2}$

4. General inductor properties data

Inductor value: $Lphase := Lphase_Al \cdot Lphase_N^2 = 2.644 \times 10^{-5}\,H$

Weight evaluation:

Copper weight density: $Cu_density := 8920 \cdot \frac{kg}{m^3}$

Wire weight: $Lphase_weight_wire := Cu_density \cdot Litz_total_lenght \cdot nstrandLphase \cdot Slitz = 14.44 \cdot gm$

Core weight:

$$Lphase_weight_core := \frac{\pi}{4} \cdot \left(Lphase_Dout^2 - Lphase_Din^2\right) \cdot Lphase_H \cdot core_density = 22.75 \cdot gm$$

terminal connection weight: $Lphase_terminal_weight := 9 \cdot gm$

Inductor volume:

$$LphaseVol := (Lphase_H + 2 \cdot DextLitz) \cdot \pi \cdot \frac{\left[(Lphase_Dout + 2 \cdot DextLitz)^2 - (Lphase_Din - 2 \cdot DextLitz)\right.}{4}$$

$$LphaseVol = 8.995 \cdot cm^3$$

Inductor core volume:

$$Lphase_volume_core := \frac{\pi}{4} \cdot \left(Lphase_Dout^2 - Lphase_Din^2\right) \cdot Lphase_H = 4.391 \cdot cm^3$$

Resin volume:

Bottom resin thickness: $EresineLphase := \frac{Vdielec_min}{(0.9 \cdot Vdielec_resine)} = 0.526 \cdot mm$

$$Hr := Lphase_H + EresineTopLphase + EresineLphase + 2 \cdot DextLitz = 19.316 \cdot mm$$

$$Doutr := Lphase_Dout + 2 \cdot DextLitz + 2 \cdot EresineExtLphase = 39.3 \cdot mm$$

$$Dinr := Lphase_Din - 2 \cdot DextLitz - 2 \cdot EresineIntLphase = 14.72 \cdot mm$$

$$Vmoule := Hr \cdot \pi \cdot \frac{Doutr^2 - Dinr^2}{4} - LphaseVol = 11.148 \cdot cm^3$$

Resin weight : $Lphase_weight_resine := Vmoule \cdot resine_density = 25.083 \cdot gm$

Inuctor weight:

$$Lphase_weight := Lphase_weight_wire + Lphase_weight_core + Lphase_terminal_weight + Lphase_we$$

$$Lphase_weight = 71.273 \cdot gm$$

IBC functional waveforms model

Subject:
This appendix gives the current and voltage waveforms of the IBC at a specific operating point.

1. Input design variables

0. IBC data

Switching frequency : $Fs := 157 \cdot kHz$

IBC number of phases: $Nphase := 3$

IBC input current: $Ihigh := 4.876 \cdot A$

IBC output current: $Ilow := 16.4675 \cdot A$ *Note : Ilow = desired_efficiency*Phigh/Vlow*

IBC input voltage value: $Vhigh := 700 \cdot V$

IBC output voltage value: $Vlow := 200 \cdot V$

1. Inductor properties data

IBC phase inductor value: $Lphase := 27.31 \cdot \mu H$

2. Output variables computation

0. IBC data

Switching period: $Ts := \frac{1}{Fs} = 6.369 \times 10^{-6} \cdot s$

1. IBC conduction mode

Critical inductor value to be in CCM/DCM limit: $Lcrit := \frac{1}{2} \frac{(Vhigh - Vlow) \cdot \frac{Vlow}{Vhigh} \cdot Ts}{\frac{Ilow}{Nphase}} = 82.883 \cdot \mu H$

Constraint on conduction mode: $Cont_conduction := Lphase - Lcrit = -55.573 \cdot \mu H$

Conduction mode (CD = 0 if continuous, CD = 1 if dicontinuous): $CD := si(Cont_conduction \geq 0, 0, 1) = 1$

Note: CD is a discontinous output variable when Cont_conduction is a continuous one. So the conduction contraint will be applied on Cont_conduction variable for the 1st order optimization algorithm

MOSFET duty-cylce : $DCM := \frac{Vlow}{Vhigh} \cdot (1 - CD) + \sqrt{\frac{2 \cdot Lphase \cdot Fs \cdot Ihigh}{Nphase \cdot (Vhigh - Vlow)}} \cdot CD = 16.696 \cdot$

Inductor current ripple: $DIL := \frac{Vhigh - Vlow}{Lphase} \cdot DCM \cdot Ts = 19.47\,A$

Diode duty-cycle: $DCD := (1 - DCM) \cdot (1 - CD) + \frac{Lphase \cdot DIL}{Vlow \cdot Ts} \cdot CD = 41.74 \cdot \%$

Inductor current minimum value: $ILmin := \left(\frac{Ilow}{Nphase} - \frac{DIL}{2}\right)\cdot(1 - CD) + 0\cdot A\cdot CD = 0\,A$

Inductor current maximum value: $ILmax := ILmin + DIL = 19.47\,A$

Diode RMS current value: $IDrms := \sqrt{DCD\cdot\left(ILmin^2 + DIL\cdot ILmin + \frac{DIL^2}{3}\right)} = 7.262\,A$

MOSFET RMS current value: $IQrms := \sqrt{DCM\cdot\left(ILmin^2 + DIL\cdot ILmin + \frac{DIL^2}{3}\right)} = 4.593\,A$

Inductor RMS current value: $ILrms := \sqrt{IDrms^2 + IQrms^2} = 8.593\,A$

Diode average current value: $IDmoy := DCD\cdot\left(ILmin + \frac{DIL}{2}\right) = 4.063\,A$

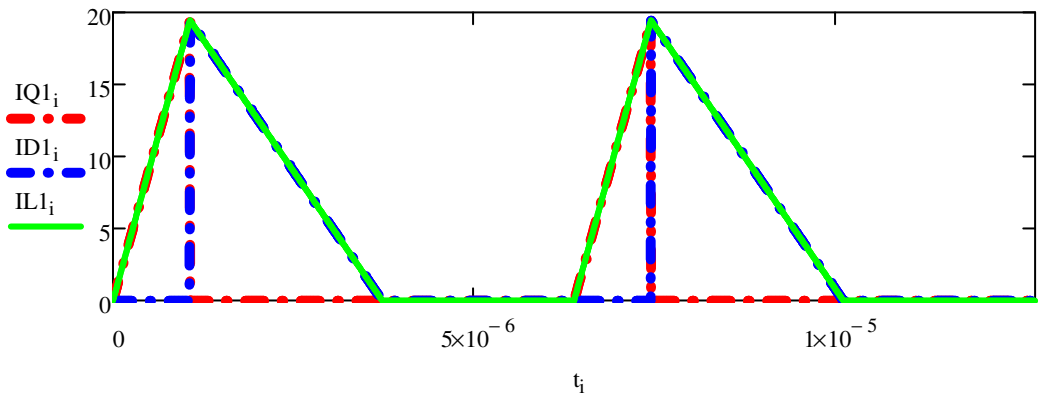
2. Plot of the IBC waveforms

Time definition: $i := 0, 1 .. 2000$ $\quad t_i := i \cdot \frac{2Ts}{2000}$

$$IQ1_{(i)} := \begin{cases} \left(\frac{Vhigh - Vlow}{Lphase}\right) \cdot t_i + ILmin & \text{if } t_i < DCM \cdot Ts \\ 0 & \text{if } DCM \cdot Ts \le t_i \le Ts \\ \left[\left(\frac{Vhigh - Vlow}{Lphase}\right) \cdot (t_i - Ts) + ILmin\right] & \text{if } Ts < t_i < Ts + DCM \cdot Ts \\ 0 & \text{if } DCM \cdot Ts + Ts \le t_i \le 2 \cdot Ts \end{cases}$$

$$ID1_{(i)} := \begin{cases} ILmin & \text{if } t_i < DCM \cdot Ts \\ DIL + \frac{-Vlow}{Lphase} \cdot (t_i - DCM \cdot Ts) & \text{if } DCM \cdot Ts \le t_i < (DCM + DCD) \cdot Ts \\ ILmin & \text{if } (DCM + DCD) \cdot Ts \le t_i \le Ts \\ 0 & \text{if } Ts < t_i < DCM \cdot Ts + Ts \\ DIL + \frac{-Vlow}{Lphase} \cdot (t_i - Ts - DCM \cdot Ts) & \text{if } DCM \cdot Ts + Ts \le t_i < (DCM + DCD) \cdot Ts + Ts \\ 0 & \text{if } (DCM + DCD) \cdot Ts + Ts \le t_i \le 2Ts \end{cases}$$

$$IL1_i := \begin{cases} \frac{Vhigh - Vlow}{Lphase} \cdot t_i + ILmin & \text{if } t_i < DCM \cdot Ts \\ DIL + \frac{-Vlow}{Lphase} \cdot (t_i - DCM \cdot Ts) & \text{if } DCM \cdot Ts < t_i < (DCM + DCD) \cdot Ts \\ ILmin & \text{if } (DCM + DCD) \cdot Ts \le t_i \le Ts \\ \left[\left(\frac{Vhigh - Vlow}{Lphase}\right) \cdot (t_i - Ts) + ILmin\right] & \text{if } Ts < t_i < Ts + DCM \cdot Ts \\ DIL + \frac{-Vlow}{Lphase} \cdot (t_i - Ts - DCM \cdot Ts) & \text{if } DCM \cdot Ts + Ts \le t_i < (DCM + DCD) \cdot Ts + Ts \\ ILmin & \text{if } (DCM + DCD) \cdot Ts + Ts \le t_i \le 2Ts \end{cases}$$



$$IQ2_{(i)} := \begin{cases} \frac{Vhigh - Vlow}{Lphase} \cdot \left(t_i - \frac{Ts}{3}\right) + ILmin & \text{if } \frac{Ts}{3} < t_i < DCM \cdot Ts + \frac{Ts}{3} \\ 0 & \text{if } DCM \cdot Ts + \frac{Ts}{3} \le t_i \le Ts + \frac{Ts}{3} \\ \frac{Vhigh - Vlow}{Lphase} \cdot \left(t_i - \frac{Ts}{3} - Ts\right) + ILmin & \text{if } \frac{Ts}{3} + Ts < t_i < DCM \cdot Ts + \frac{Ts}{3} + Ts \\ 0 & \text{otherwise} \end{cases}$$

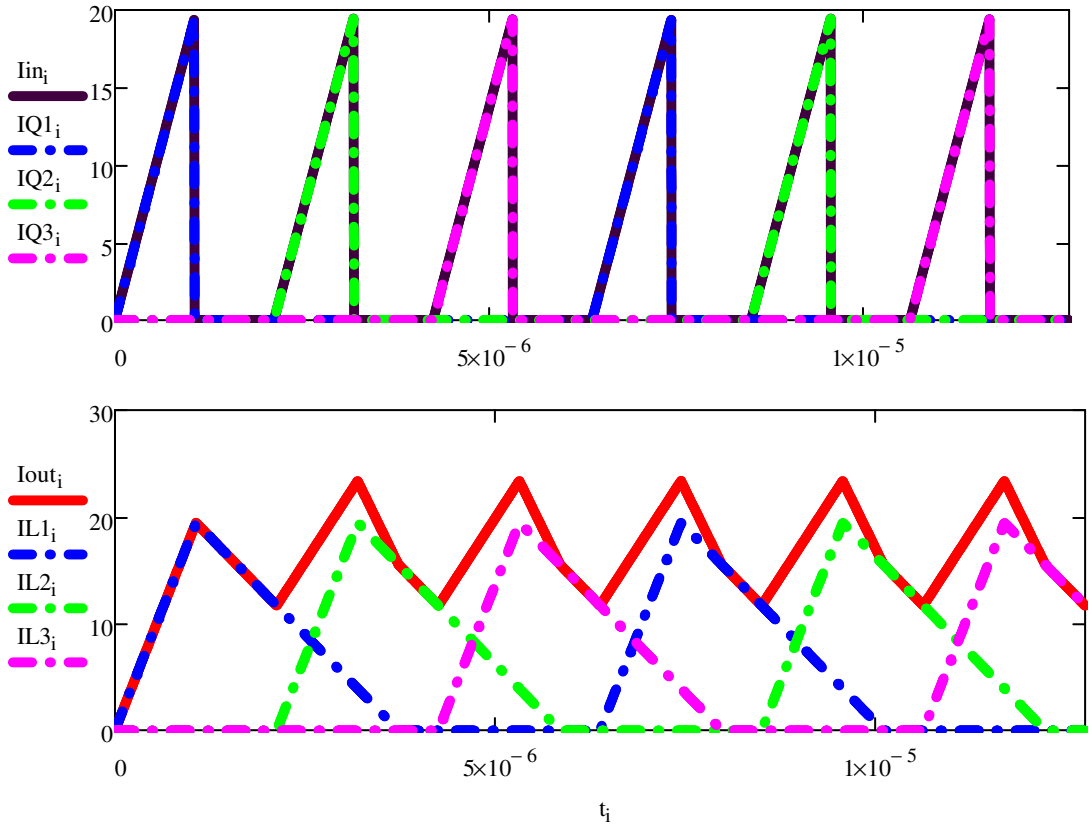
$$IQ3_{(i)} := \begin{cases} \frac{Vhigh - Vlow}{Lphase} \cdot \left(t_i - \frac{2Ts}{3}\right) + ILmin & \text{if } \frac{2Ts}{3} < t_i < DCM \cdot Ts + \frac{2Ts}{3} \\ 0 & \text{if } DCM \cdot Ts + \frac{2Ts}{3} \le t_i \le Ts + \frac{2Ts}{3} \\ \frac{Vhigh - Vlow}{Lphase} \cdot \left(t_i - \frac{2Ts}{3} - Ts\right) + ILmin & \text{if } \frac{2Ts}{3} + Ts < t_i < DCM \cdot Ts + \frac{2Ts}{3} + Ts \\ 0 & \text{otherwise} \end{cases}$$

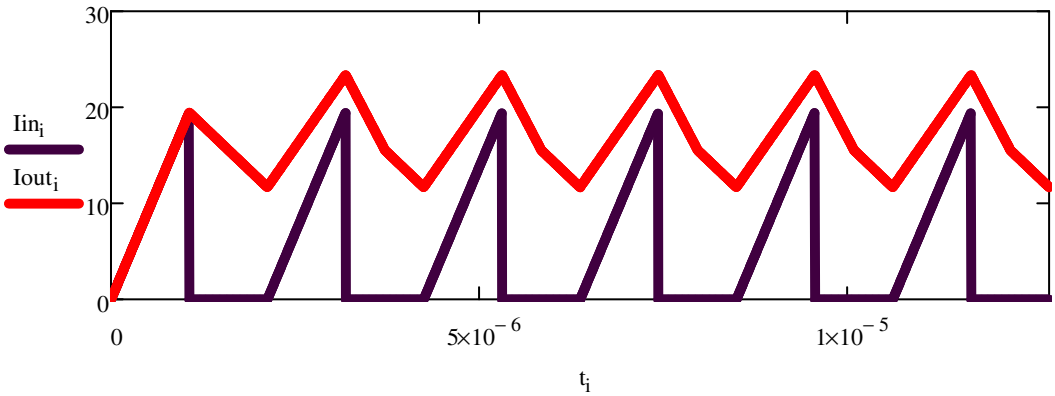
$$Iin_{(i)} := IQ1_i + IQ2_i + IQ3_i$$

$$IL2_i := \begin{cases} \frac{Vhigh - Vlow}{Lphase} \cdot \left(t_i - \frac{Ts}{3}\right) + ILmin & \text{if } \frac{Ts}{3} < t_i < DCM \cdot Ts + \frac{Ts}{3} \\ DIL + \frac{-Vlow}{Lphase} \cdot \left(t_i - DCM \cdot Ts - \frac{Ts}{3}\right) & \text{if } DCM \cdot Ts + \frac{Ts}{3} < t_i < (DCM + DCD) \cdot Ts + \frac{Ts}{3} \\ \frac{Vhigh - Vlow}{Lphase} \cdot \left(t_i - \frac{Ts}{3} - Ts\right) + ILmin & \text{if } \frac{Ts}{3} + Ts < t_i < DCM \cdot Ts + \frac{Ts}{3} + Ts \\ DIL + \frac{-Vlow}{Lphase} \cdot \left(t_i - DCM \cdot Ts - \frac{Ts}{3} - Ts\right) & \text{if } DCM \cdot Ts + \frac{Ts}{3} + Ts < t_i < (DCM + DCD) \cdot Ts + \frac{Ts}{3} + \\ 0 & \text{otherwise} \end{cases}$$

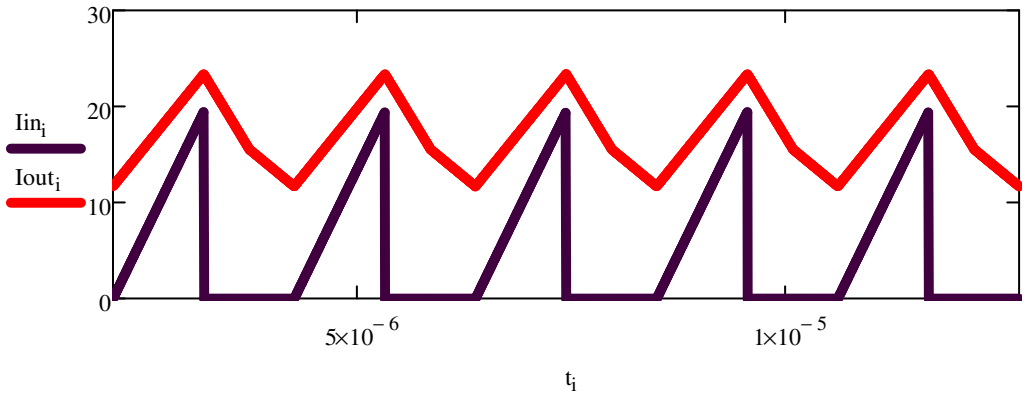
$$IL3_i := \begin{cases} \frac{Vhigh - Vlow}{Lphase} \cdot \left(t_i - \frac{2Ts}{3}\right) + ILmin & \text{if } \frac{2Ts}{3} < t_i < DCM \cdot Ts + \frac{2Ts}{3} \\ DIL + \frac{-Vlow}{Lphase} \cdot \left(t_i - DCM \cdot Ts - \frac{2Ts}{3}\right) & \text{if } DCM \cdot Ts + \frac{2Ts}{3} < t_i < (DCM + DCD) \cdot Ts + \frac{2Ts}{3} \\ \frac{Vhigh - Vlow}{Lphase} \cdot \left(t_i - \frac{2Ts}{3} - Ts\right) + ILmin & \text{if } \frac{2Ts}{3} + Ts < t_i < DCM \cdot Ts + \frac{2Ts}{3} + Ts \\ DIL + \frac{-Vlow}{Lphase} \cdot \left(t_i - DCM \cdot Ts - \frac{2Ts}{3} - Ts\right) & \text{if } DCM \cdot Ts + \frac{2Ts}{3} + Ts < t_i < (DCM + DCD) \cdot Ts + \frac{2Ts}{3} \\ 0 & \text{otherwise} \end{cases}$$

$$Iout_i := IL1_i + IL2_i + IL3_i$$


Iin_i
IQ1_i
IQ2_i
IQ3_i
Iout_i
IL1_i
IL2_i
IL3_i
t_i


Iin_i
Iout_i
t_i

In static
:


Iin_i
Iout_i
t_i

Filters transfer functions computation and determination of converter input & output currents spectra

Subject:
This appendix gives the transfer function of the LC filters which are used un the optimization model and from which the sprectra of the converter input and output currents can be determined.
It should be noticed that the optimization models in CADES software actually take into acount the parastic elements of the filtering components. But for more simplicity the parasitic elements will not be considered in this Mathcad sheet.

1. Input design variables

0. IBC data

Switching frequency :	$Fs := 157 \cdot kHz$
IBC number of phases:	$Nphase := 3$
MOSFET duty-cylce :	$DCM := 16.69\%$
Diode duty-cycle:	$DCD := 41.74\%$
Inductor current ripple:	$DIL := 19.47 \cdot A$
Inductor current minimum value:	$ILmin := 0 \cdot A$
IBC DC line input current:	$I_high := 4.876 \cdot A$
IBC DC line output current:	$I_low := 16.4675 \cdot A$

1. IBC Filters data

Total value of the input capacitor:	$C_Chigh := 1.35 \cdot \mu F$
Total value of the input inductor on **one** DC line:	$Lhigh := 2.762 \cdot \mu H$
DC line wiring inductance value on **one** DC line:	$Lline_high := 0.75 \cdot \mu H$
Total value of the output capacitor:	$C_Clow := 0.27 \cdot \mu F$
Total value of the output inductor on **one** DC line:	$L_low := 1.5 \cdot \mu H$

2. Output variables computation

0. IBC data

Switching period: $Ts := \frac{1}{Fs} = 6.369 \times 10^{-6} \cdot s$

Command delay: $d := \frac{1}{Nphase} = 0.333$

1. Ihigh and Ilow before filtering current spectra

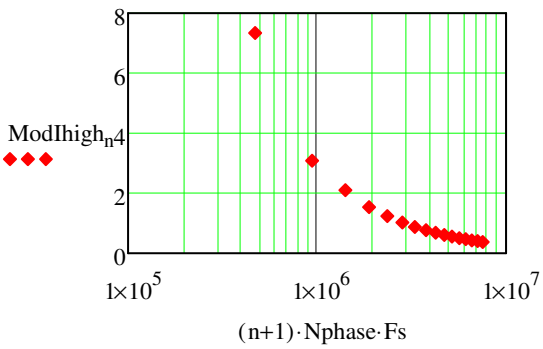
$n := 0, 1 .. 15 \qquad \omega_n := 2\cdot\pi\cdot Nphase\cdot Fs\cdot(n+1)$

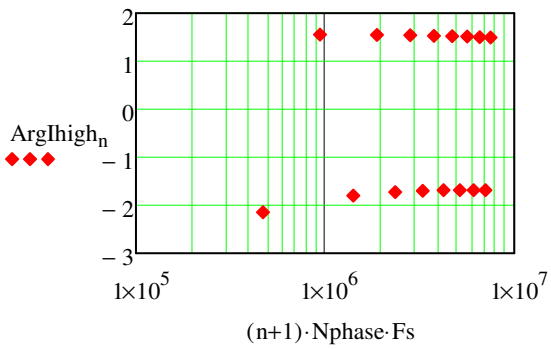
Input current:

$$IQ1N_n := \frac{2}{Ts}\cdot\left[\left(1-\exp\left(-i\cdot\omega_n\cdot DCM\cdot Ts\right)\right)\cdot\left[\frac{ILmin}{i\cdot\omega_n}+\frac{DIL}{DCM\cdot Ts\cdot\left(i\cdot\omega_n\right)^2}\right]-\frac{DIL}{i\cdot\omega_n}\cdot\exp\left(-i\cdot\omega_n\cdot DCM\cdot Ts\right)\right]$$

$Ihigh_n := IQ1N_n\cdot Nphase$ Because by theoritic, the harmonics appear only at Nphase*Fs: sum simplification

$$ModIhigh_n := \sqrt{Re\left(Ihigh_n\right)^2+Im\left(Ihigh_n\right)^2} \qquad ArgIhigh_n := \arg\left(Ihigh_n\right)$$





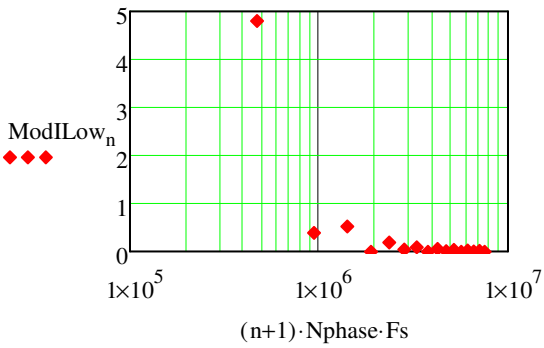
Output current:

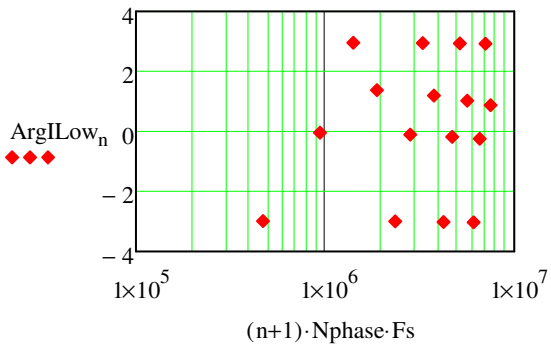
$arg1N_n := -\omega_n\cdot DCM\cdot Ts \qquad arg2N_n := -\omega_n\cdot(DCM+DCD)\cdot Ts$

$$ILN_n := \frac{2}{Ts}\cdot\left[\frac{i\cdot ILmin\cdot\left(1-\exp\left(i\cdot arg2N_n\right)\right)}{\omega_n}-\frac{DIL\cdot\left(1-\exp\left(i\cdot arg1N_n\right)\right)}{\left(\omega_n\right)^2\cdot DCM\cdot Ts}+\frac{DIL\cdot\left(\exp\left(i\cdot arg1N_n\right)-\exp\left(i\cdot arg2N_n\right)\right)}{\left(\omega_n\right)^2\cdot DCD\cdot Ts}\right.$$

$Ilow_n := ILN_n\cdot Nphase$ Because by theoritic, the harmonics appear only at Nphase*Fs: sum simplification

$$ModILow_n := \sqrt{Re\left(Ilow_n\right)^2+Im\left(Ilow_n\right)^2} \qquad ArgILow_n := \arg\left(Ilow_n\right)$$





2. Filters impedance computation

Frequency vectors: $q := 0, 1 .. 80 \quad f_q := 1 \cdot Hz \cdot 10^{\frac{q}{10}} \quad \omega f_q := 2 \cdot \pi \cdot f_q$

Filtering components impedance: $ZChighf_q := \frac{1}{i \cdot C_Chigh \cdot \omega f_q} \quad ZLhighf_q := i \cdot 2 \cdot (Lhigh + Lline_high) \cdot \omega f$

$ZClowf_q := \frac{1}{i \cdot C_Clow \cdot \omega f_q} \quad ZLlowf_q := i \cdot 2 \cdot L_low \cdot \omega f_q$

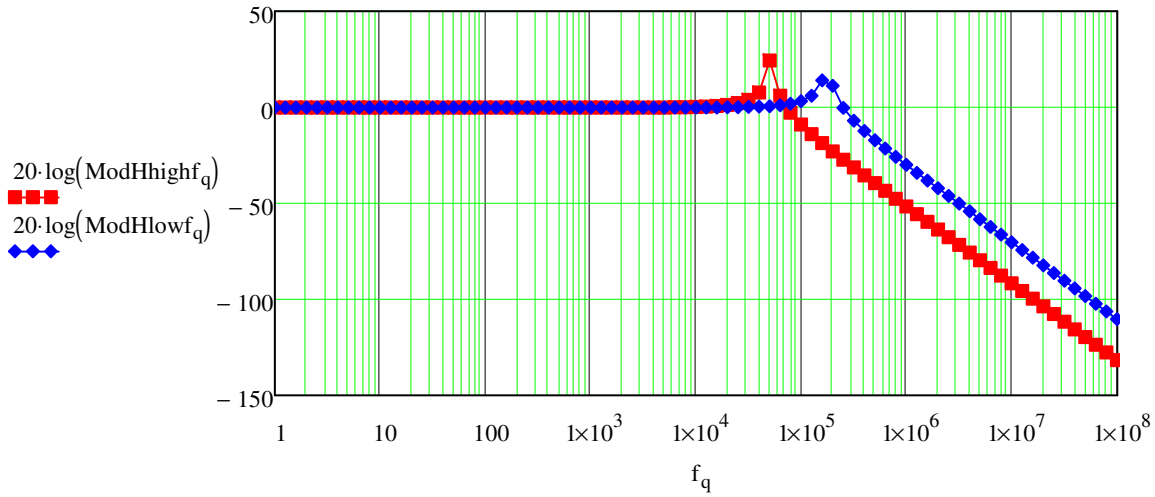
Transfer function of the input filter: $Hhighf_q := \frac{ZChighf_q}{ZChighf_q + ZLhighf_q}$

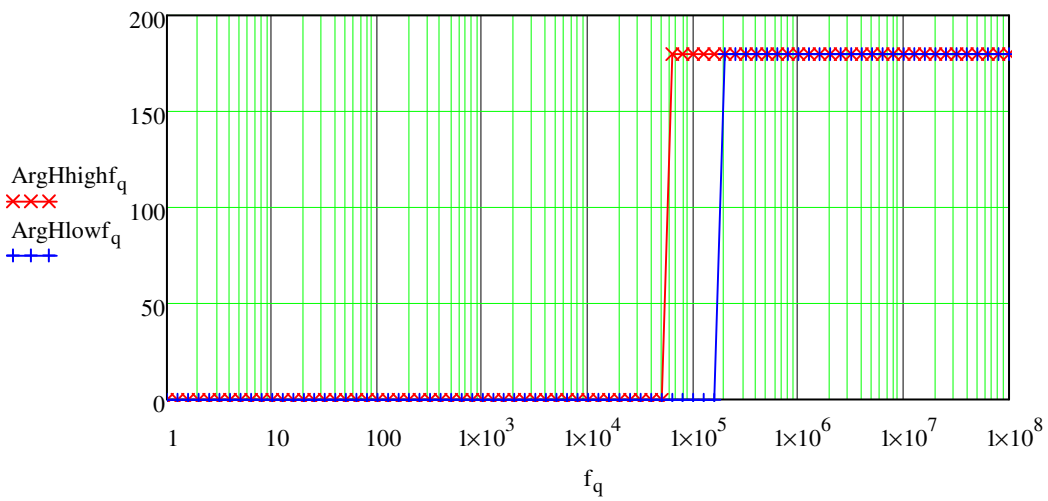
$ModHhighf_q := \sqrt{Re(Hhighf_q)^2 + Im(Hhighf_q)^2} \quad ArgHhighf_q := arg(Hhighf_q) \cdot \frac{180}{\pi}$

Transfer function of the output filter: $Hlowf_q := \frac{ZClowf_q}{ZClowf_q + ZLlowf_q}$

$ModHlowf_q := \sqrt{Re(Hlowf_q)^2 + Im(Hlowf_q)^2} \quad ArgHlowf_q := arg(Hlowf_q) \cdot \frac{180}{\pi}$

Bode
d





2. Ihigh and Ilow after filtering current spectra

Input current spectra and THD computation:

Input filter resonant frequency:

$$fchigh := \frac{1}{2\cdot\pi\cdot\sqrt{2\cdot Lhigh\cdot C_Chigh}} = 58.281\cdot kHz$$

Filtering components impedance:

$$ZChigh_n := \frac{1}{i\cdot C_Chigh\cdot\omega} \qquad ZLhigh_n := i\cdot 2\cdot(Lhigh + Lline_high)\cdot$$

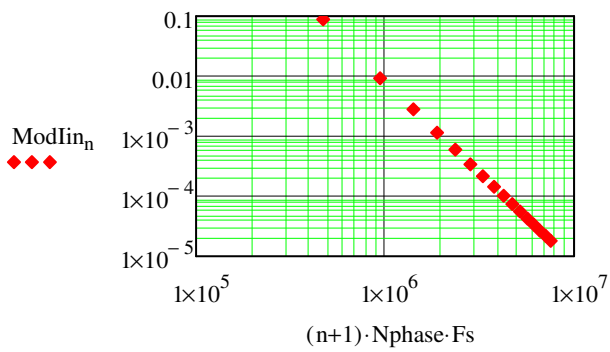
Transfer function of the input filter:

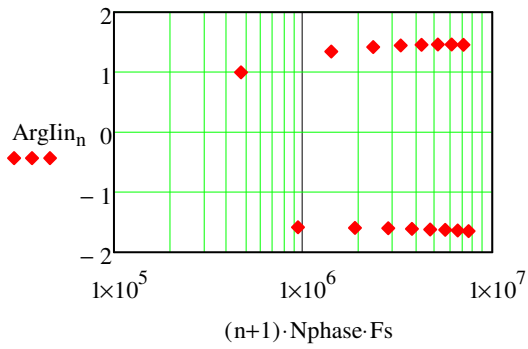
$$Hhigh_n := \frac{ZChigh_n}{ZChigh_n + ZLhigh_n}$$

Input current spectrum after filtering:

$$Iin_n := Ihigh_n\cdot Hhigh_n$$

$$ModIin_n := \sqrt{Re(Iin_n)^2 + Im(Iin_n)^2} \qquad ArgIin_n := arg(Iin_n)$$





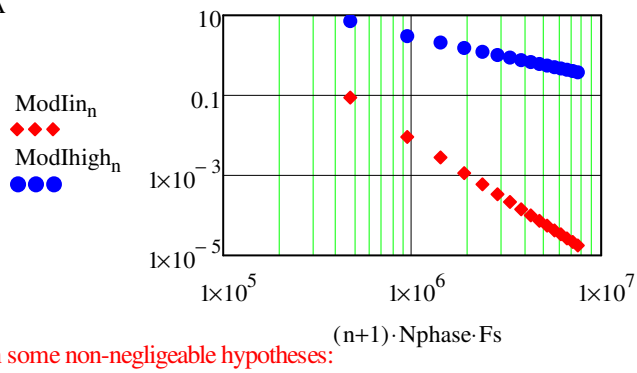
Input RMS current computation:

$$Ihigh_rms := \sqrt{I_high^2 + \frac{\sum_n (ModIin_n)^2}{2}} = 4.876\,A$$

Input current THD computation

$$THD_Ihigh := \frac{\sqrt{\frac{\sum_n (ModIin_n)^2}{2}}}{Ihigh_rms} = 1.307\cdot\%$$

Comparaison of current spectra befor and after filtering:



Be careful: this THD computation has been made based on some non-negligeable hypotheses:

- The current disturbances appear only at the following frequencies: Nphase*Fs ==> this is valid only when the IBC switching cell parasitic elements are not taken into account (so in the pure imaginary world), that the delay between each phase is perfect and that no common mode current is flying through the converter ground....
- This THD has been computed with a perfect filter: in the reality, it has some parasitics which decrease its efficiency for high frequencies. So the high frequency noise that appears in the reality is not taken into account in this calculation : the designer has to take some safety margins.

Nevertheless, this computation gives an idea of the phenomena that appear in the IBC.

Output current spectra and THD computation:

Output filter resonant frequency:

$$fclow := \frac{1}{2\cdot\pi\cdot\sqrt{2\cdot L_low\cdot C_Clow}} = 176.839\cdot kHz$$

Filtering components impedance:

$$ZClow_n := \frac{1}{i\cdot C_Clow\cdot\omega_n} \qquad ZLlow_n := i\cdot 2\cdot L_low\cdot\omega_n$$

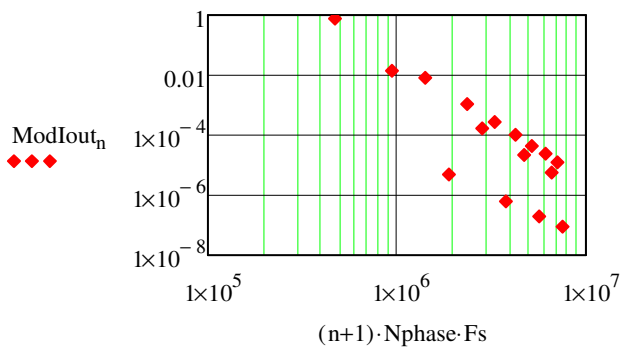
Transfer function of the output filter:

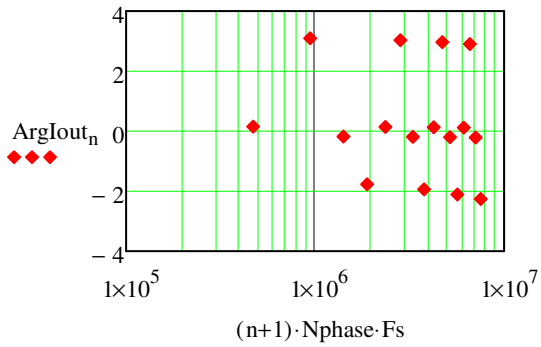
$$Hlow_n := \frac{ZClow_n}{ZClow_n + ZLlow_n}$$

Output current spectrum after filtering:

$$Iout_n := Ilow_n\cdot Hlow_n$$

$$ModIout_n := \sqrt{Re(Iout_n)^2 + Im(Iout_n)^2} \qquad ArgIout_n := arg(Iout_n)$$

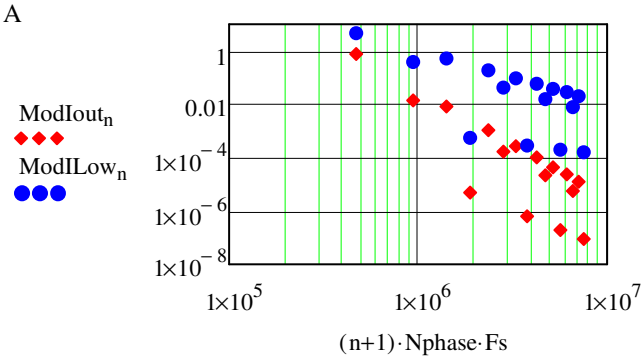




Output RMS current computation:

$$Ilow_rms := \sqrt{I_low^2 + \frac{\sum_n (ModIout_n)^2}{2}} = 16.477\,A$$

Comparaison of current spectra befor and after filtering:



Input current THD computation

$$THD_Ilow := \frac{\sqrt{\frac{\sum_n (ModIout_n)^2}{2}}}{Ilow_rms} = 3.385\cdot\%$$

Be careful: this THD computation has been made based on some non-negligeable hypotheses:

- The current disturbances appear only at the following frequencies: Nphase*Fs ==> this is valid only when the IBC switching cell parasitic elements are not taken into account (so in the pure imaginary world), that the delay between each phase is perfect and that no common mode current is flying through the converter ground....
- This THD has been computed with a perfect filter: in the reality, it has some parasitics which decrease its efficiency for high frequencies. So the high frequency noise that appears in the reality is not taken into account in this calculation : the designer has to take some safety margins.

Nevertheless, this computation gives an idea of the phenomena that appear in the IBC.

Appendix 3: Power components losses and thermal models capitalization

1. **SiC SWITCHING CELL LOSSES MODEL……257**

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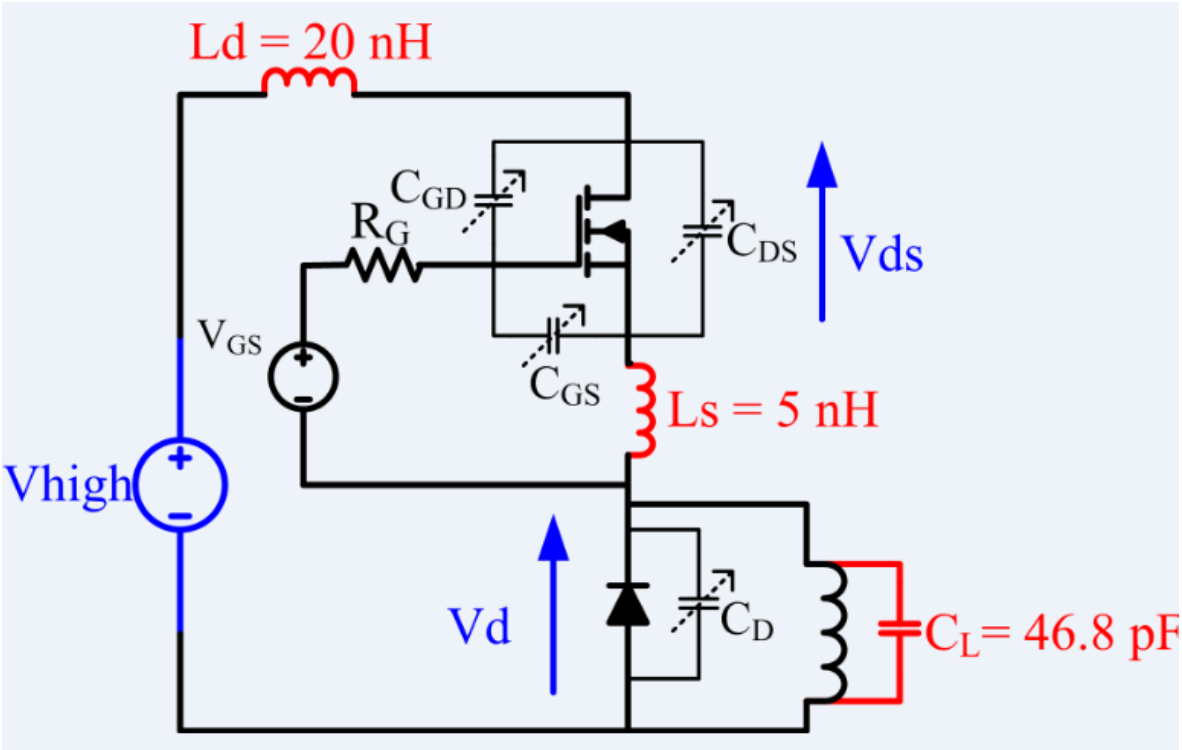
3. **SEMI-CONDUCTORS THERMAL MODEL……301**

4. **PHASE INDUCTOR THERMAL MODEL** *(not provided yet for confidentiality reasons)*

SiC switching cell Losses Model

Subject:
This appendix gives the equations to compute the losses of a SiC switching cell losses made of :
- a N-MOSFET
- a Schottky diode

This model has been mainly inspired by the following paper:
[1] K. Peng, S. Eskandari, and E. Santi, "Analytical loss model for power converters with SiC MOSFET and SiC schottky diode pair," 2015 IEEE Energy Convers. Congr. Expo. ECCE 2015, pp. 6153–6160, 2015.



1. Input design variables

0. IBC data

Switching frequency :	$Fs := 157 \cdot kHz$
IBC output current:	$Ilow := 16.4675 \cdot A$
IC number of phases:	$Nb_phases := 3$
MOSFET duty-cylce :	$DCM := 0.1684$
Diode duty-cycle:	$DCD := 0.421$
IBC input voltage value:	$Vhigh := 700 \cdot V$
IBC output voltage value:	$Vlow := 200 \cdot V$
Condcution mode:	$CD := 1$ if = 1: Discontinuous

1. Inductor data

Phase inductor minimum current value: $ILmin := 0 \cdot A$

Phase inductor current ripple: $DIL := 19.789 \cdot A$

Phase inductor RMS current: $ILrms := 8.772 \cdot A$

Phase inductor supposed parasitic capacitor value: $CL := 42 \cdot pF$

Phase inductor value: $Lphase := 27.31 \cdot \mu H$

2. MOSFET data

On-state resistance: $Rds_on := 0.041 \Omega$

Internal gate resistance: $Rg_int := 1.929 \cdot \Omega$

Linear transconductance: $gfs := 15.497 \cdot S$

Linear threshold voltage: $Vth_lin := 8.375 \cdot V$

Real threshold voltage: $Vth := 2.583 \cdot V$

Transfer characteristic quadratic coefficient: $Kfs := 1.385 \cdot \frac{A}{V^2}$

Input capacitance value for low and high Vds: $Ciss0 := 2.837 \cdot nF$, $Ciss1200 := 1.83 \cdot nF$

Output capacitance value for low and high Vds: $Coss0 := 2.441 \cdot nF$, $Coss1200 := 146.146 \cdot pF$

Transfer capacitance value for low and high Vds: $Crss0 := 1.055 \cdot nF$, $Crss1200 := 10.449 \cdot pF$

RMS current: $IQrms := 4.593 \cdot A$

3. Diode data

On-state resistance: $Rt := 0.048 \cdot \Omega$

On-state voltage drop: $Vt := 0.926 \cdot V$

Capacitance for low and high (400 V) reverse voltage: $Cd1 := 918.012 \cdot pF$, $Cd2 := 57.352 \cdot pF$

RMS current: $IDrms := 7.262 \cdot A$

average current: $IDmoy := 4.063 \cdot A$

4. Switching cell and driver data

Drain global indutance: $Ld := 20 \cdot 10^{-9} \cdot H$

Source global inductance: $Ls := 5 \cdot 10^{-9} \cdot H$

Mutual indcutance value: $Mds := 0.0 \cdot H$

External gate resistance: $Rg_ext := 13.6 \cdot \Omega$ $\quad Rg := Rg_int + Rg_ext = 15.529\,\Omega$

Turn on driver voltage: $Vdr_H := 20 \cdot V$

Turn off driver voltage: $Vdr_L := -5 \cdot V$

1. Output variables computation

0. Switching currents and voltages data

Switching cell input voltage at Turn ON: $VswitchON := Vhigh - Vlow \cdot CD = 500\ V$

Switching cell input voltageat Turn OFF $VswitchOFF := Vhigh = 700\ V$

Switched current at Turn ON: $IswitchON := ILmin + 0.001A \cdot CD = 1 \times 10^{-3}\ A$

If the converter is running in Discontinuous Conduction Mode, CD = 1. But for numerical reasons, it is better to avoid the pure zero for this variable IswitchON.

Switched current at Turn OFF: $IswitchOFF := ILmin + DIL = 19.789\ A$

0. MOSFET capacitances:

MOSFET GD Capacitor High Vds $Cgd1 := Crss1200 = 10.449 \cdot pF$

MOSFET GD Capacitor Low Vds $Cgd2 := Crss0 = 1.055 \cdot nF$

MOSFET DS Capacitor High Vds $Cds1 := Coss1200 - Crss1200 = 135.697 \cdot pF$

MOSFET DS Capacitor Low Vds $Cds2 := Coss0 - Crss0 = 1.386 \cdot nF$

MOSFET GS Capacitor High Vds $Cgs1 := Ciss1200 - Crss1200 = 1.82 \cdot nF$

2. Switching losses during the turn-ON

1. Stage #1: period t0-t1

During that stage, the gate voltage goes from Vdr_L to Vgs_th and starts to charge input MOSFET capacitor Ciss. Ciss value is "Ciss_high" because Vds is High. Often, this stage is called "delay time of the MOSFET turn ON because Vds and Id do not evolve yet.

$t0 := 0 \cdot s$

$$t0t1 := Rg \cdot Ciss1200 \cdot \frac{Vth - Vdr_L}{Vdr_H - \frac{Vth + Vdr_L}{2}} = 10.161 \cdot ns \quad t1 := t0 + t0t1 = 10.161 \cdot ns$$

2. Stage #2: period t1-t2

During that stage, Vgs rises from Vth to Vmiller1 and the MOSFET drain currrent Id rises from 0 to IswitchON. The source parasitic inductance impacts the gate voltage due to the high dI/dt during that stage.
To make the calculations easier, we fix the diode ON state voltage to Vd_on (the variation is negligeable).
Because Id value starts from 0 to I0, we use the quadratic transfer charcteristic of the MOSFET but we suppose that Id rises in a linear way (use of SiC material). That is why, we express Vmiller1 as :

$Id = Kfs \cdot (Vgs - Vth)^2$ So at time t2 : $Id_t2 = Kfs \cdot (Vmiller1_ON - Vth)^2 = IswitchON$

$$Vmiller1_ON := Vth + \sqrt{\frac{IswitchON}{Kfs}} = 2.61\ V$$

The gate current is equal to :

$$Ig(t) = \frac{1}{Rg} \cdot \left[Vdr_H - Vgs(t) - (Ls + Mds)\frac{dId}{dt} \right] \quad \text{With:} \quad Vgs(t) = Vth + \frac{Vmiller1_ON - Vth}{t2 - t1} \cdot t$$

If we say that : $Id(t) = k \cdot t$ with : $k = \frac{I0}{(t2 - t1)}$ then : $\frac{dId}{dt} = k$

The average gate current can therefore be expressed as :

$$Ig_average = \frac{1}{Rg}\cdot\left[Vdr_H - \frac{1}{t2-t1}\int_0^{t2-t1} Vgs(t)\,dt - (Ls+Mds)\cdot\frac{1}{t2-t1}\int_0^{t2-t1}\frac{dId}{dt}\,dt\right]$$

$$Ig_average = \frac{1}{Rg}\cdot\left[Vdr_H - \frac{Vth+Vmiller1_ON}{2} - (Ls+Mds)\cdot\frac{I0}{t2-t1}\right] \qquad (1)$$

We also have the following gate average current expression:

$$Ig_average = Ciss1200\cdot\frac{dVgs(t)}{dt} = Ciss1200\cdot\frac{Vmiller1_ON - Vth}{t2-t1} \qquad (2)$$

Combining (1) with (2), it is possible to get the stage 2 time t1t2 :

$$\boxed{t1t2 := \frac{Ciss1200\cdot Rg\cdot(Vmiller1_ON - Vth) + (Ls+Mds)\cdot IswitchON}{Vdr_H - \frac{Vth+Vmiller1_ON}{2}} = 0.044\cdot ns}$$

$$t2 := t1 + t1t2 = 10.205\cdot ns$$

For stage 2 energy losses computation : we suppose that Vds is linear with the following equation :

$$Vds(t) = VswitchON - (Ls+Ld+2\cdot Mds)\cdot\frac{dId(t)}{dt}$$

$$\boxed{E12 := \left[\frac{t1t2}{2}\cdot(VswitchON)IswitchON - (Ls+Ld+2\cdot Mds)\cdot\frac{IswitchON^2}{2}\right] = 1.103\times 10^{-11}\,J}$$

In the same time, the diode begins to turn OFF

Vds voltage is a constant named Vdsr that is equal to:

$$Vdsr := VswitchON - (Ls+Ld+2\cdot Mds)\frac{IswitchON}{t1t2} = 499.434\,V$$

The average gate current is equal to :

$$Ig2 := \frac{1}{Rg}\cdot\left[Vdr_H - \frac{Vmiller1_ON - Vth}{2} - (Ls+Mds)\frac{IswitchON}{t1t2}\right] = 1.28\,A$$

3. Stage #3: period t2-t3

During that stage, the diode is in the OFF state : its voltage value as well as the MOSFET voltage value are eveloving duringthat stage. Indeed, Vgs ~ Vmiller and Vds drops from Vdsr to Vmiller2-Vth_lin.
Indeed, the drain current value is quite high during that stage, then we consider a linear transfer characteristic of the mosfet (even in discontinuous conduction mode) and the threshold voltage as well as Vmiller are different from last stage (Vth_lin and Vmiller2).
The diode and inductance parasitic capacitances Cd and CL are charging thanks to the dVd/dt introduced by the MOSFET. This changes a little bit Vgs and give a little current from the MOSFET (Id). This over-current is small enough to consider that it does not create a voltage through (Ls+Mds). Finally, it is possible to write these equations :

1- Because the drain current value is high, we consider that the transfer characteristic of the MOSFET is linear for that stage.

$$Id = gfs\cdot(Vgs(t) - Vth) \qquad \text{So :} \quad Vgs(t) = Vth + \frac{Id}{gfs} \qquad \text{where :}$$

$$Id = IswitchON - (Cd2 + CL)\frac{dVd(t)}{dt} = IswitchON - (Cd2 + CL)\frac{dVds(t)}{dt}$$

Because : $Vd(t) = Vds(t) - Vhigh$

So : $$Vgs(t) = (Vmiller2_ON) - \frac{(Cd2 + CL)}{gfs}\frac{dVds(t)}{dt}$$

Where : $$Vmiller2_ON := Vth_lin + \frac{IswitchON}{gfs} = 8.375\,V$$

Finally, the gate current is equal to :

$$Ig(t)_3 = \frac{1}{Rg}\cdot(Vdr_H - Vgs(t)) \qquad Ig(t)_3 = \frac{1}{Rg}\cdot\left[Vdr_H - Vmiller2_ON + \frac{(Cd2 + CL)}{gfs}\frac{dVds(t)}{dt}\right]$$

2- We suppose that the drain-source MOSFET voltage Vds decreases linearly from Vdsr to Vmiller2-Vth_lin :

$$Vds(t) = Vdsr + k\cdot t \quad \text{with :} \qquad k = -\frac{Vdsr - (Vmiller2_ON - Vth_lin)}{t3 - t2}$$

In conclusion, the gate current can be expressed as :

$$Ig_3 = \frac{1}{Rg}\cdot\left[Vdr_H - Vmiller2_ON + \frac{(Cd2 + CL)}{gfs}\cdot -\frac{Vdsr - (Vmiller2_ON - Vth_lin)}{t3 - t2}\right]$$

$$Ig_3 = \frac{1}{Rg}\cdot\left[(Vdr_H - Vmiller2_ON) - \frac{(Cd2 + CL)}{gfs}\cdot\frac{Vdsr - (Vmiller2_ON - Vth_lin)}{t3 - t2}\right] = c\,(3)$$

We also have the following average gate current :

$$Ig_average_3 = -Cgd1\cdot\frac{dVds(t)}{dt} = Cgd1\cdot\frac{Vr - (Vmiller2_ON - Vth_lin)}{t3 - t2} \qquad (4)$$

Combining (3) with (4), it is possible to get the stage 3 time :

$$\boxed{t2t3 := \frac{Cgd1\cdot Rg\cdot(Vdsr - Vmiller2_ON + Vth_lin) + \frac{(Cd1 + CL)(Vdsr - Vmiller2_ON + Vth_lin)}{gfs}}{Vdr_H - Vmiller2_ON}}$$

$t2t3 = 9.633\cdot ns$

For stage 3 time computation, we decided to take Cd1 instead of Cd2 because at the begining of this phase, the high value of Cd slows the switching.

$t3 := t2 + t2t3 = 19.838\cdot ns$

For stage 3 energy losses computation : we suppose that Id is a constant with the following equation :

$$Id(t) = IswitchON - (Cd2 + CL)\frac{dVds(t)}{dt} = IswitchON + (Cd2 + CL)\cdot\frac{Vr - (Vmiller2 - Vth_lin)}{t3 - t2} = cste$$

Id current between t2 and t3, named Id3:

$$Id3 := IswitchON + (Cd2 + CL)\cdot\frac{Vdsr - (Vmiller2_ON - Vth_lin)}{t3 - t2} = 5.152\,A$$

$$\boxed{E23 := Id3\cdot\left[Vdsr - \frac{1}{2}\cdot[Vdsr - (Vmiller2_ON - Vth_lin)]\right]\cdot t2t3 = 1.239\times 10^{-5}\,J}$$

The gate current is equal to :

$$Ig3 := Cgd1\cdot\frac{Vdsr - (Vmiller2_ON - Vth_lin)}{t3 - t2} = 0.542\,A$$

During this stage, the diode voltage is evolving due to MOSFET voltage evolution.
Diode voltage is going from 0 to Vhigh in continuous conduction mode and from Vlow (ideal case without oscillations) to Vhigh in discontinuous conduction mode.

Diode recovery charge during its turn OFF: $QdiodeOFF := Cd2\cdot VswitchON = 2.868\times 10^{-8}\,C$

$$\boxed{PdiodeOFF := QdiodeOFF\cdot(VswitchON)\cdot Fs = 2.251\,W}$$

4. Stage #4: period t3-t4

During that phase, the capacitance Cgd is high (since Vds is low) and dVds/dt is slower. And so there are no more current coming from diode and load capacitances charge. Finally, Vgs = Vmiller2, Vds drops linearly from Vmiller1-Vth to Von. The drain current is equal to IswitchON. It is then possible to write these equations :

$$Vds(t) = Vmiller2_ON - Vth_lin + \frac{Von - (Vmiller2_ON - Vth_lin)}{t4 - t3}\cdot t = linear$$

With: $Von := Rds_on\cdot IswitchON = 4.1\times 10^{-5}\,V$

$$Ig(t)_4 = \frac{1}{Rg}\cdot(Vdr_H - Vgs(t)) = \frac{1}{Rg}(Vdr_H - Vmiller2_ON) = cste \quad (5)$$

We also have the fllowing gate average current :

$$Ig_average_4 = -Cgd\,2\cdot\frac{dVds(t)}{dt} = Cgd2\cdot\frac{Vr - (Vmiller2_ON - Vth_lin)}{t3 - t2} \qquad (6)$$

Combining (5) with (6), it is possible to get the stage 4 time t3t4 :

$$\boxed{t3t4 := \frac{Cgd2\cdot Rg\cdot(Vmiller2_ON - Vth_lin - Von)}{Vdr_H - Vmiller2_ON} = 3.316\times 10^{-5}\cdot ns}$$

$$t4 := t3 + t3t4 = 19.838\cdot ns$$

$$\boxed{E34 := IswitchON\cdot\left(\frac{Von + Vmiller2_ON - Vth_lin}{2}\right)\cdot t3t4 = 0\,J}$$

The gate current is equal to : $Ig4 := \frac{1}{Rg}(Vdr_H - Vmiller2_ON) = 0.749\,A$

5. Stage #5: period t4-t5

During that phase, the gate power supply continues to charge Cgd but the MOSFET is in ON state : the "only" losses are the conduction losses. And so, Vgs(t) rises from Vmiller1 to Vdr_H in exponential way.

$$Vgs(t) = Vmiller2_ON \cdot \exp\left(\frac{\ln\left(\frac{Vdr_H}{Vmiller2_ON}\right)}{t5 - t4} \cdot t\right)$$

$$Ig(t)_5 = \frac{1}{Rg} \cdot (Vdr_H - Vgs(t)) = \frac{1}{Rg}\left(Vdr_H - Vmiller2_ON \cdot \exp\left(\frac{\ln\left(\frac{Vdr_H}{Vmiller2_ON}\right)}{t5 - t4} \cdot t\right)\right)$$

It is possible to estimate the stage 5 time t4t5 with classical RC circuit integration :

$$\boxed{t4t5 := -Cgd2 \cdot Rg \cdot \ln\left(\frac{0.9Vdr_H - Vdr_H}{Vmiller2_ON - Vdr_H}\right) = 28.834 \cdot ns}$$

$$t5 := t4 + t4t5 = 48.672 \cdot ns$$

$$\boxed{E45 := IswitchON \cdot Von \cdot t4t5 = 1.182 \times 10^{-15} J}$$

6. Turn ON conclusion about MOSFET losses

$$\boxed{Eon := E12 + E23 + E34 + E45 = 1.239 \times 10^{-5} J}$$

For information :

Duration of turn on when the switching losses appends:

$$tswitch_on := t1t2 + t2t3 + t3t4 = 9.677 \cdot ns$$

Turn ON duration with delay time and complete gate charge time :

$$ton := t0t1 + tswitch_on + t4t5 = 48.672 \cdot ns$$

$E12 = 1.103 \times 10^{-11} J$ $E23 = 1.239 \times 10^{-5} J$ $E34 = 0 J$ $E45 = 1.182 \times 10^{-15} J$

$$\boxed{Pmosfet_ON := Eon \cdot Fs = 1.946 W}$$

Only stage 2 and 3 are influencing the global active losses...

3. MOSFET conduction losses

During that phase, the MOSFET is in ON state : the "only" losses are the conduction losses:

$t5t6 := DCM \cdot \frac{1}{Fs} - t5 = 1.024 \times 10^{-6} s$ $t6 := t5 + t5t6 = 1.073 \times 10^{-6} s$

$$\boxed{E56 := \frac{Rds_on \cdot IQrms^2}{Fs} = 5.509 \times 10^{-6} J}$$

$$Econd_mosfet := E56 = 5.509 \times 10^{-6} J$$

$$\boxed{Pmosfet_cond := E56 \cdot Fs = 0.865 W}$$

4. Switching losses during MOSFET turn OFF

1. Stage #7: period t6-t7

The gate driver voltage Vdr is set to its low value (Vdr_L) at t6, but there is a delay time before MOSFET begins to turn off. During this t6-t7 phase, the MOSFET is so still in ON state : the "only" losses are the conduction losses. Vgs value is decreasing from Vdr_H to Vmiller1 in a exponential way.

$$Vgs(t) = Vdr_H \cdot \exp\left(\frac{\ln\left(\frac{Vmiller2_OFF}{Vdr_H}\right)}{t7 - t6} \cdot t\right)$$

$$Ig(t)_5 = \frac{1}{Rg} \cdot (Vdr_L - Vgs(t)) = \frac{1}{Rg}\left(Vdr_L - Vdr_H \cdot \exp\left(\frac{\ln\left(\frac{Vmiller2_OFF}{Vdr_H}\right)}{t7 - t6} \cdot t\right)\right)$$

$$Vmiller2_OFF := Vth_lin + \frac{IswitchOFF}{gfs} = 9.652\,V$$

It is possible to estimate the stage 7 time t6t7 with classical RC circuit integration :

$$\boxed{t6t7 := -Ciss0 \cdot Rg \cdot \ln\left(\frac{Vdr_H - Vmiller2_OFF}{Vdr_H - Vdr_L}\right) = 38.861 \cdot ns}$$

$$t7 := t6 + t6t7 = 1.111 \times 10^{-6}\,s$$

$$\boxed{E67 := IswitchOFF^2 \cdot Rds_on \cdot t6t7 = 6.239 \times 10^{-7}\,J}$$ should be negligeable

2. Stage #8: period t7-t8

During that stage Vds grows from Von to Vmiller2-Vth_lin linearly and Vgs = Vmiller2. The drain current stays I0.

$$Vds(t) = Von + \frac{Vmiller2_OFF - Vth_lin - Von}{t8 - t7} \cdot t = linear$$

$$Ig(t)_8 = \frac{1}{Rg} \cdot (Vdr_L \cdot -Vgs(t)) = \frac{1}{Rg}(Vdr_L - Vmiller2_OFF) = cste \qquad (7)$$

We also have the fllowing gate average current :

$$Ig_average_8 = -Cgd\,2 \cdot \frac{dVds(t)}{dt} = Cgd2 \cdot \frac{Von - (Vmiller2_OFF - Vth_lin)}{t8 - t7} \qquad (8)$$

Combining (7) with (8), it is possible to get the stage 8 time t7t8 :

$$\boxed{t7t8 := \frac{Cgd2 \cdot Rg \cdot (Vmiller2_OFF - Vth_lin - Von)}{Vmiller2_OFF - Vdr_L} = 1.428 \cdot ns}$$

$$t8 := t7 + t7t8 = 1.113 \times 10^{-6}\,s$$

$$\boxed{E78 := IswitchOFF \cdot \left(Von + \frac{Vmiller2_OFF - Vth_lin - Von}{2}\right) \cdot t7t8 = 1.804 \times 10^{-8}\,J}$$ Should be negligeable...

The gate current is equal to : $Ig8 := \frac{1}{Rg}(Vdr_L - Vmiller2_OFF) = -0.944\,A$

3. Stage #9: period t8-t9

This stage is the opposite of stage 3: during that stage, the diode is in the ON state : its voltage value as well as the MOSFET voltage value are eveloving during that stage. Indeed, Vgs ~ Vmiller2 and Vds rises from Vmiller2-Vth_lin to Vdc+Vd_on.
The diode and inductance parasitic capacitances Cd and CL are discharging their energy thank to the dVd/dt introduced by the MOSFET (so diode capacitance strat from Cd2 value to Cd1 value). Cd1 is considered to compute stage duration and Cd2 to compute the current drop.

$Cd1 = 918.012 \cdot pF$ for Vr = 0V $\quad Cd2 = 57.352 \cdot pF$ for Vr=400V

This changes a little bit Vgs and take a little current from the MOSFET (Id). This up-current is small enough to consider that it does not creat a voltage through (Ls+Mds). Finally, it is possible to write these equations :

1- Because the drain current value is high, we consider that the transfer characteristic of the MOSFET is linear for that stage.

$Id = gfs \cdot (Vgs(t) - Vth)$ So : $Vgs(t) = Vth_lin + \frac{Id}{gfs}$ where :

Because : $Vd(t) = Vds(t) - VswitchOFF$

$$Id = IswitchOFF - (Cd1 + CL)\frac{dVd(t)}{dt} = IswitchOFF - (Cd2 + CL)\frac{dVds(t)}{dt}$$

So : $Vgs(t) = \left(Vth + \frac{IswitchOFF}{gfs}\right) - \frac{(Cd2 + CL)}{gfs}\frac{dVds(t)}{dt}$

And we can note that : $Vth_lin + \frac{IswitchOFF}{gfs} = Vmiller2_OFF$

Finally, the gate current is equal to :

$Ig(t)_9 = \frac{1}{Rg} \cdot (Vdr_L - Vgs(t))$ so : $Ig(t)_9 = \frac{1}{Rg} \cdot \left[Vdr_L - Vmiller2_OFF + \frac{(Cd1 + CL)}{gfs}\frac{dVds(t)}{dt}\right]$

2- We suppose that the drain-source MOSFET voltage Vds decreases linearly :

$Vds(t) = Vmiller2_OFF - Vth_lin + k \cdot t$ with : $k = \frac{VswitchOFF + Vd_on - (Vmiller2_OFF - Vth_lin)}{t9 - t8}$

In conclusion, the gate current can be expressed as :

$$Ig_9 = \frac{1}{Rg} \cdot \left[(Vdr_L - Vmiller2_OFF) + \frac{(Cd1 + CL)}{gfs} \cdot \frac{VswitchOFF + Vd_on - (Vmiller2_OFF - Vth_lin)}{t9 - t8}\right] = cs \quad (9)$$

We also have the fllowing gate average current :

$$Ig_average_9 = -Cgd1 \cdot \frac{dVds(t)}{dt} = -Cgd1 \cdot \frac{VswitchOFF + Vd_on - (Vmiller2_OFF - Vth_lin)}{t9 - t8} \quad (10)$$

Combining (9) with (10), it is possible to get the stage 9 time t9t10 :

$$\boxed{t8t9 := \frac{\left[Cgd1 \cdot Rg + \frac{(Cd1 + CL)}{gfs}\right] \cdot (VswitchOFF - Vmiller2_OFF + Vth_lin)}{Vmiller2_OFF - Vdr_L} = 10.692 \cdot ns}$$

$t9 := t8 + t8t9 = 1.124 \times 10^{-6}\,s$

For stage 9 energy losses computation : we suppose that Id is a constant with the following equation :

$$Id(t) = IswitchOFF - (Cd2 + CL)\frac{dVds(t)}{dt}$$

$$Id(t) = \left[IswitchOFF - (Cd2 + CL)\cdot\frac{VswitchOFF + Vd_on - (Vmiller2_OFF - Vth_lin)}{t9 - t8} = cste\right]$$

Id current between t8 and t9, named Ids9:

$$Ids9 := IswitchOFF - (Cd2 + CL)\cdot\frac{VswitchOFF - (Vmiller2_OFF - Vth_lin)}{t9 - t8} = 13.296\,A$$

We suppose that the MOSFET drain-source voltage Vds decreases linearly:

It may happens that Id9 becomes negative due to capacitances. But we wll consider that it does not go under 0A for the model $offstate := \begin{cases} 1.0 & \text{if } Ids9 > 0A \\ 0.0 & \text{if } Ids9 \le 0A \end{cases} = 1$

$$E89 = \int_{t8}^{t9} Id(t)\cdot Vds(t)\,dt$$

$$E89_a := IswitchOFF\cdot(Vmiller2_OFF - Vth_lin)\cdot t8t9 = 2.702\times 10^{-7}\,J$$

$$b1 := IswitchOFF\cdot(VswitchOFF - Vmiller2_OFF + Vth_lin)$$

$$b2 := (IswitchOFF - Ids9\cdot offstate)\cdot(Vmiller2_OFF - Vth_lin)$$

$$E89_b := (b1 - b2)\cdot\frac{t8t9}{2} = 7.388\times 10^{-5}\,J$$

$$E89_c := \frac{-t8t9\cdot[(IswitchOFF - Ids9\cdot offstate)\cdot(VswitchOFF - Vmiller2_OFF + Vth_lin)]}{3}$$

$$E89_c = -1.617\times 10^{-5}\,J$$

$$\boxed{E89 := E89_a + E89_b + E89_c = 5.798\times 10^{-5}\,J}$$

The gate current is equal to :

$$Ig9 := \frac{(Vdr_L - Vmiller2_OFF)}{Rg} + \frac{(Cd2 + CL)}{Rg\cdot gfs}\cdot\frac{VswitchOFF - (Vmiller2_OFF - Vth_lin)}{t9 - t8} = -0.917\,A$$

The gate voltage is equal to :

$$Vgs9 := Vmiller2_OFF - \frac{Cd2 + CL}{gfs}\cdot\frac{VswitchOFF - (Vmiller2_OFF - Vth_lin)}{t8t9} = 9.233\,V$$

<u>Diode recovery charge during its turn ON:</u> $QdiodeON := Cd2\cdot(Vhigh - 0) = 4.015\times 10^{-8}\,C$

$$\boxed{Pdiode_ON := QdiodeON\cdot(Vhigh - 0)\cdot Fs = 4.412\,W}$$

4. Stage #10: period t9-t10

This stage is the opposite of stage 2: Vgs rises from Vmiller1+CdVd/dt to Vth. Its evolution is linear when Id drops from Id9 to 0 with in a quadratic way. So here, we will use Vmiller1 and Vth. Besides, the Id drop through the parasitic inductances of the MOSFET source and impacts the gate voltage due to the high dI/dt during that stage.

$$Id = Kfs\cdot(Vgs - Vth)^2$$

The gate current is equal to :

$$Ig(t) = \frac{1}{Rg}\cdot\left[Vdr_L - Vgs(t) - (Ls + Mds)\frac{dIds}{dt}\right] \quad \text{With:} \quad Vgs(t) = Vgs9 + \frac{Vth - Vgs9}{t10 - t9}\cdot t$$

If we say that : $Ids(t) = Ids9 + k\cdot t$ with : $k = \frac{-Ids9}{(t10 - t9)}$ then : $\frac{dIds}{dt} = k$

and finally, the average gate current can be expressed as :

$$Ig_average_{10} = \frac{1}{Rg}\cdot\left[Vdr_L - \frac{1}{t10 - t9}\int_0^{t10-t9} Vgs(t)\,dt - (Ls + Mds)\cdot\frac{1}{t10 - t9}\int_0^{t10-t9}\frac{dIds}{dt}\,dt\right]$$

$$Ig_average_{10} = \frac{1}{Rg}\cdot\left[Vdr_L - \frac{Vgs9 + Vth}{2} - (Ls + Mds)\cdot\frac{-Ids9}{t10 - t9}\right] \qquad (11)$$

We also have the fllowing gate average current :

$$Ig_average = -Ciss1200\cdot\frac{dVgs(t)}{dt} = -Ciss1200\cdot\frac{Vgs9 - Vth}{t10 - t9} \qquad (12)$$

Combining (11) with (12), it is possible to get the stage 10 time t9t10 :

$$t9t10 := \frac{-[Ciss1200\cdot Rg\cdot(Vgs9 - Vth) + (Ls + Mds)\cdot Ids9]}{Vdr_L - \frac{Vgs9 + Vth}{2}} = 23.42\cdot ns$$

$$t10 := t9 + t9t10 = 1.147\times 10^{-6}\,s$$

For stage 10 energy losses computation : we suppose that Vds is linear with the following equation :

$$Vds(t) = VswitchOFF + Vd_on - (Ls + Ld + 2\cdot Mds)\cdot\frac{dId(t)}{dt} = Vdc + Vd_on - (Ls + Ld + 2\cdot Mds)\cdot\frac{-Id9}{(t10 - t9)}$$

The drain-source MOSFET voltage reaches a peak value:

$$Vds_peak := VswitchOFF - (Ls + Ld + 2\cdot Mds)\cdot\frac{-Ids9}{(t10 - t9)} = 714.194\,V$$

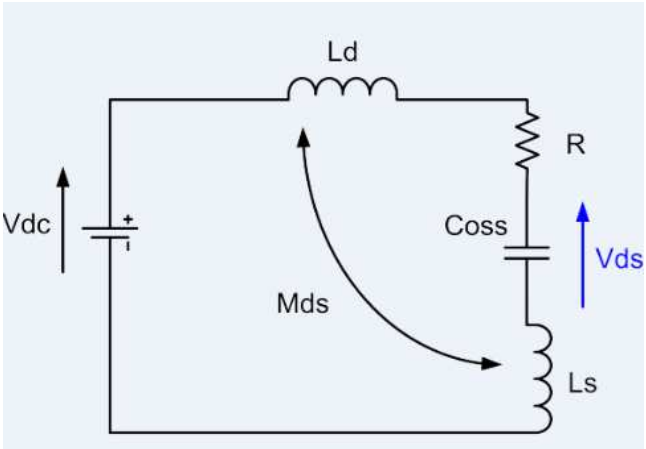
$$E910 := \frac{Vds_peak\cdot Ids9}{2}\cdot t9t10\cdot offstate = 1.112\times 10^{-4}\,J$$

The average gate current is equal to :

$$Ig10 := -Ciss1200\cdot\frac{Vgs9 - Vth}{t10 - t9} = -0.52\,A$$

5. Stage #11: period t10-t11

During that stage, the voltage is ringing due to the resonnance between the MOSFET output capacitance and stray inductances. It is a RLC serie circuit as drawn below :



At the begining of the ringing period, Vds(t) = Vds_peak

At the end of the ringing period, Vds(t) = Vds_off = Vdc+Vd_on

The energy losses can be computed with the Coss energy storage:

Mosfet output capacitance stored energy at Vds_peak (i.e. at time t10):

We considered here that Coss varitation for these high Vds values is too small to be considered.

$$QVds_peak := Coss1200 \cdot Vds_peak = 104.377 \cdot nC$$

$$QVds_off := Coss1200 \cdot (VswitchOFF) = 102.302 \cdot nC$$

$$\boxed{Ering := offstate \cdot \left[\frac{QVds_peak \cdot Vds_peak}{2} - QVds_off \cdot \frac{VswitchOFF}{2} - (QVds_peak - QVds_off) VswitchOFF \right]}$$

$$Ering = 1.472 \times 10^{-8} J$$

For future EMI considerations, below the electrical parameters time equations:

For easier writtings :

$$R := Rt = 0.048\,\Omega \qquad L := Ls + Ld + 2Mds = 2.5 \times 10^{-8} H$$

$$C := Coss1200 = 146.146 \cdot pF$$

Global cicuit equation:

$$L \cdot C \cdot \frac{d^2}{dt^2} Vds(t) + R \cdot C \cdot \frac{d}{dt} Vds(t) + Vds(t) = VswitchOFF$$

Equation without the 2nd member :

$$L \cdot C \cdot \frac{d^2}{dt^2} Vds(t) + R \cdot C \cdot \frac{d}{dt} Vds(t) + Vds(t) = 0$$

i.e. : $r^2 + \frac{R}{L} r + \frac{1}{LC} = 0$

whether :

$$\omega o := \frac{1}{\sqrt{L \cdot C}} = 5.232 \times 10^{8} \cdot \frac{rad}{s}$$ the pulsation

$$\lambda := \frac{R}{2 \cdot L} = 960 \cdot kHz$$ the damping factor

$$\alpha := \frac{\lambda}{\omega o} = 1.835 \times 10^{-3}$$ the damping coefficient

$$Q := \frac{1}{R \cdot C \cdot \omega o} = 272.48$$ the quality factor

So the discriminant : $\Delta := 4 \cdot \lambda^{2} - 4\omega o^{2} = -1.095 \times 10^{18} \frac{1}{s^{2}}$

The reduced discriminant : $\Delta p := \frac{\Delta}{4} = -2.737 \times 10^{17} \frac{1}{s^{2}}$

Because Δ is negative, we are in pseudo-periodic regime:

$Vds(t) = (A1 \cdot \cos(\omega \cdot t) + A2 \cdot \sin(\omega \cdot t))\exp(-\lambda \cdot t)$ with : $\omega := \sqrt{-\Delta p} = 5.232 \times 10^{8} \cdot \frac{rad}{s}$

Whereas : $Vds(0) = A1 = Vds_peak - (Vdc + Vd_on)$ $Ids(0) = C \cdot \left(\frac{d}{dt} Vds(t)\right) = A2 \cdot \omega - A1 \cdot \lambda = 0$

So : $A1 := Vds_peak - (VswitchOFF) = 14.194\,V$ $A2 := \frac{\lambda \cdot A1}{\omega} = 0.026\,V$

Because we have a second member :

$$Vds(t) = VswitchOFF + Vd_on + (A1 \cdot \cos(\omega \cdot t) + A2 \cdot \sin(\omega \cdot t))\exp(-\lambda \cdot t)$$

$$Id(t) = -C \cdot A1 \cdot \frac{\omega^{2} + \lambda^{2}}{\omega} \cdot \exp(-\lambda \cdot t) \cdot \sin(\omega t)$$

Finally the pseudo-periodic phase ends at :

$$t11 := \begin{cases} \left(t10 + \frac{3}{\lambda}\right) & \text{if } t10 + \frac{3}{\lambda} < \frac{(DCM + DCD)}{Fs} \\ \frac{(DCM + DCD)}{Fs} & \text{otherwise} \end{cases} = 3.754 \times 10^{-6}\,s$$

$$\boxed{t10t11 := t11 - t10 = 2.607 \times 10^{-6}\,s}$$

6. Turn OFF summary

MOSFET turn off losses:

$Eoff := E67 + E78 + E89 + E910 + Ering = 1.698 \times 10^{-4}\,J$

$Pmosfet_OFF := (E67 + E78 + E89 + E910 + Ering) \cdot Fs = 26.664\,W$

4. MOSFET losses summary

$Eswitch := Eon + Eoff = 1.822 \times 10^{-4}\,J$

$Pmosfet := Pmosfet_ON + Pmosfet_cond + Pmosfet_OFF = 29.475\,W$

5. Diode conduction losses

Diode conduction period: $\frac{DCD}{Fs} = t11 - t6$ $\qquad$ $Vdiode_on = Vt + Rt \cdot Id(t)$

Diode conduction losses: $EcondD := \frac{\left(Vt \cdot IDmoy + Rt \cdot IDrms^2\right)}{Fs} = 4.009 \times 10^{-5}\,J$

$$\boxed{Pdiode_cond := Vt \cdot IDmoy + Rt \cdot IDrms^2 = 6.294\,W}$$

6. Switching losses during diode and MOSFET turn OFF in discontinuous conduction mode (due to resonnance oscillations)

1. Stage #12: period t11-t12

$t12 := \frac{1}{Fs} = 6.369 \times 10^{-6}\,s$

$toscill := \frac{(DCM + DCD)}{Fs} = 3.754 \times 10^{-6}\,s$

Diode recovery charge during oscillation (mean value):

$Qdiode_Oscill := Cd2 \cdot Vlow = 1.147 \times 10^{-8}\,C$

$\omega 0 := \frac{1}{\sqrt{Lphase \cdot (CL + Cd1)}} = 6.176 \times 10^{6}\,\frac{1}{s}$

$THF := 2 \cdot \frac{\pi}{\omega 0} = 1.017 \times 10^{-6}\,s$ $\qquad$ $FHF := \frac{1}{THF} = 982.926 \cdot kHz$

$$\boxed{Pdiode_oscill := Qdiode_Oscill \cdot Vlow \cdot Fs \cdot \frac{(1 - DCM - DCD)}{Fs \cdot THF} = 0.926\,W}$$

7. Conclusion about diode losses

$Pdiode_ON = 4.412\,W$

$Pdiode_cond = 6.294\,W$

$PdiodeOFF = 2.251\,W$

$Pdiode_oscill = 0.926\,W$

$$\boxed{Pdiode := Pdiode_ON + Pdiode_cond + PdiodeOFF + Pdiode_oscill = 13.883\,W}$$

$DiodeConductionRatio := \frac{Pdiode_cond}{Pdiode} = 45.335 \cdot \%$

3. Switching cell electrical parameters waveforms

If you want ideal waveforms for DCM durong diode and MOSFET turn off: Ideal = 1, 0 else $\quad Ideal := 0$

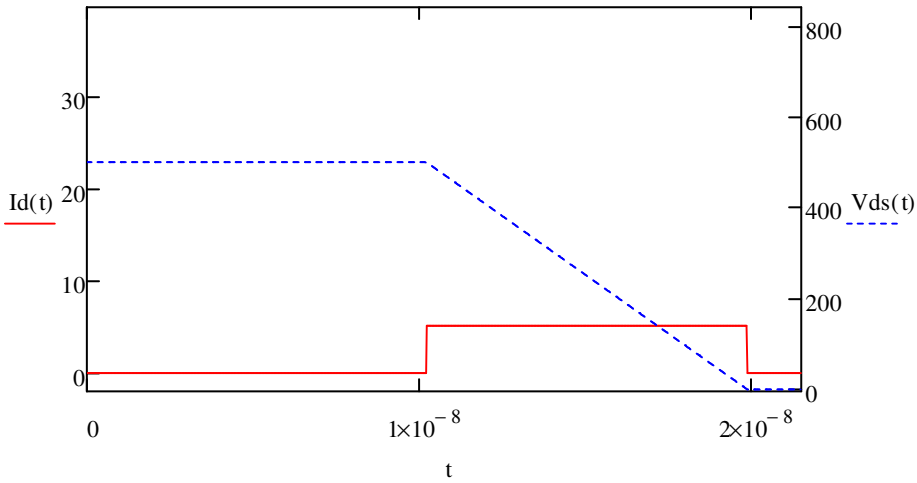
$$\omega oscill := \frac{1}{\sqrt{Lphase \cdot (CL + Cd2)}} = 1.92 \times 10^{7} \frac{1}{s} \qquad VswitchON = 500\ V \qquad Vdsr = 499.434\ V$$

- **Mosfet :**

$$Vds(t) := \begin{cases} VswitchON & \text{if } t < t1 \\ Vdsr & \text{if } t1 < t \le t2 \\ \left[Vdsr - \frac{Vdsr - (Vmiller2_ON - Vth_lin)}{t2t3} \cdot (t - t2)\right] & \text{if } t2 < t \le t3 \\ Vmiller2_ON - Vth_lin + \frac{Von - (Vmiller2_ON - Vth_lin)}{t4 - t3} \cdot (t - t3) & \text{if } t3 < t \le t4 \\ Von & \text{if } t4 < t \le t5 \\ Von & \text{if } t5 < t \le t6 \\ Von & \text{if } t6 < t \le t7 \\ Von + \frac{Vmiller2_OFF - Vth_lin - Von}{t8 - t7} \cdot (t - t7) & \text{if } t7 < t \le t8 \\ Vmiller2_OFF - Vth_lin + \frac{VswitchOFF - (Vmiller2_OFF - Vth_lin)}{t9 - t8} \cdot (t - t8) & \text{if } t8 < t \le t9 \\ Vds_peak & \text{if } t9 < t \le t10 \\ VswitchOFF + [A1 \cdot \cos[\omega \cdot (t - t10)] + A2 \cdot \sin[\omega \cdot (t - t10)]]\exp[-\lambda \cdot (t - t10)] & \text{if } t10 < t \le t11 \\ VswitchON & \text{if } (t11 < t \le t12 \wedge Ideal = 1) \\ \left[Vhigh - Vlow \cdot [1 - \cos[\omega oscill \cdot (t - t11)]] \cdot \exp\left[\frac{0.01\Omega}{Lphase} \cdot (t - t11)\right]\right] & \text{if } (t11 < t \le t12 \wedge Ideal = 0) \end{cases}$$

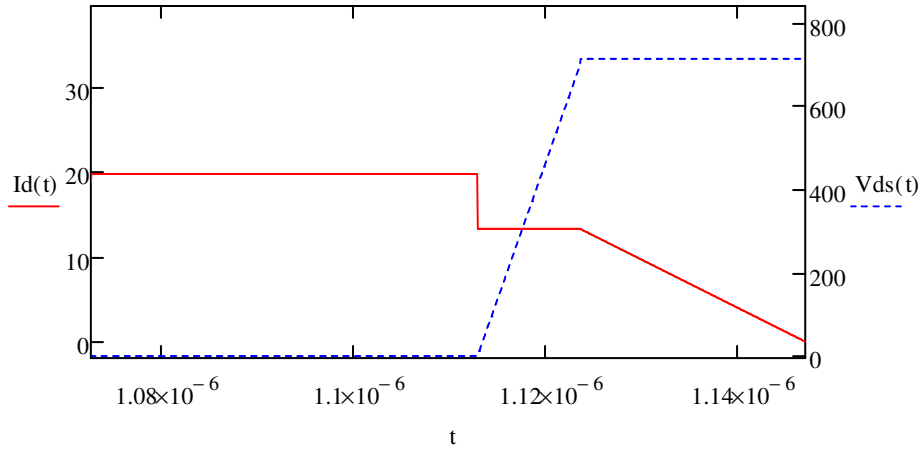
$$
Id(t) := \begin{cases}
0 \quad \text{if } t < t1 \\
IswitchON \cdot \left(\dfrac{t - t1}{t2 - t1} \right) \quad \text{if } t1 < t \le t2 \\
Id3 \quad \text{if } t2 < t \le t3 \\
IswitchON \quad \text{if } t3 < t \le t4 \\
IswitchON \quad \text{if } t4 < t \le t5 \\
IswitchON + \dfrac{Vhigh - Vlow}{Lphase} \cdot (t - t5) \quad \text{if } t5 < t \le t6 \\
IswitchOFF \quad \text{if } t6 < t \le t7 \\
IswitchOFF \quad \text{if } t7 < t \le t8 \\
Ids9 \quad \text{if } t8 < t \le t9 \\
Ids9 + \dfrac{-Ids9}{(t10 - t9)} \cdot (t - t9) \quad \text{if } t9 < t \le t10 \\
-C \cdot A1 \cdot \dfrac{\omega^2 + \lambda^2}{\omega} \cdot \exp[-\lambda \cdot (t - t10)] \cdot \sin[\omega \cdot (t - t10)] \quad \text{if } t10 < t \le t11 \\
0A \quad \text{if } t11 < t \le t12
\end{cases}
$$

Turn on:

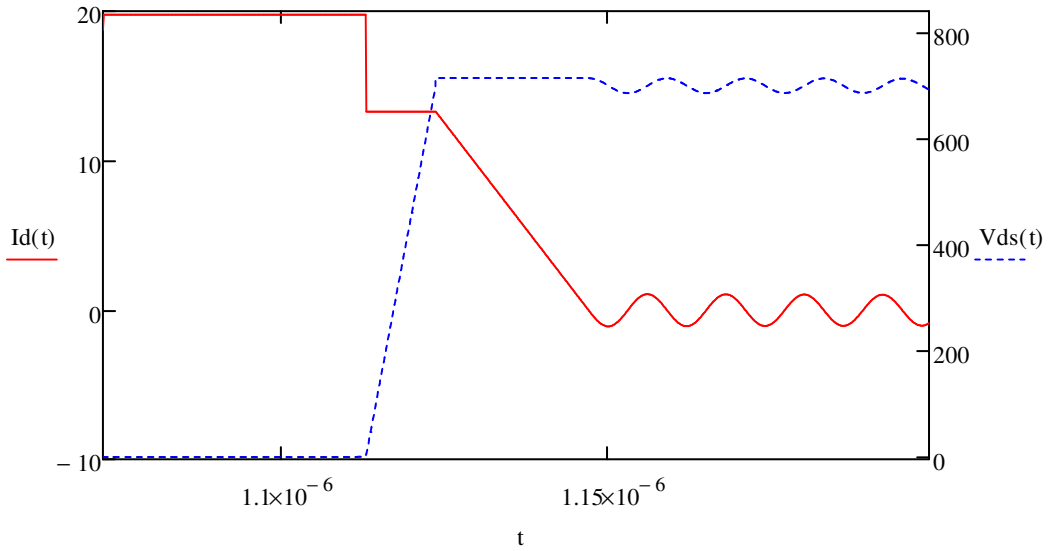


Turn off:

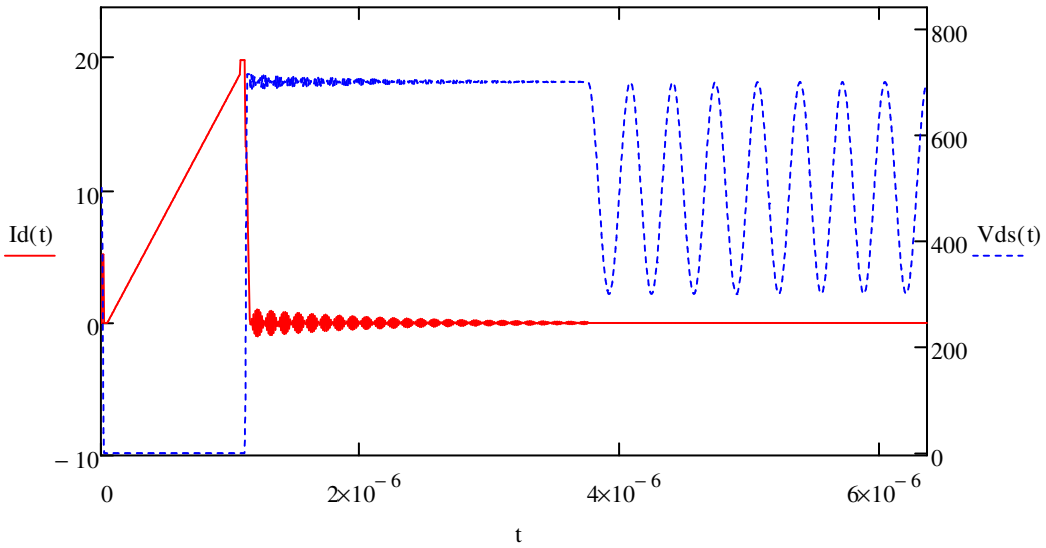
Start of turn OFF



End of turn OFF



Total period



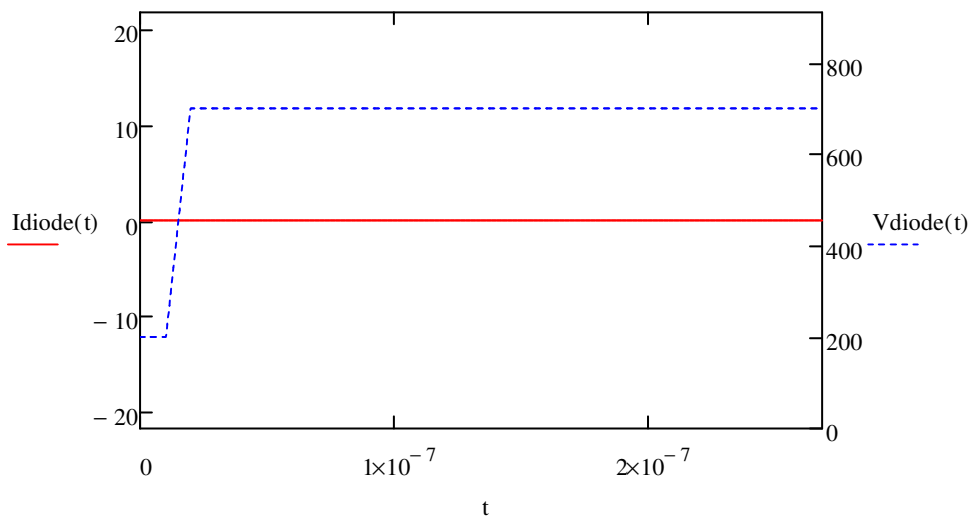
- **Inductor :**

$$IL(t) := \begin{cases} 0 \ \text{ if } \ t < t1 \\ IswitchON \cdot \left(\dfrac{t - t1}{t2 - t1}\right) \ \text{ if } \ t1 < t \le t2 \\ Id3 \ \text{ if } \ t2 < t \le t3 \\ IswitchON \ \text{ if } \ t3 < t \le t4 \\ IswitchON \ \text{ if } \ t4 < t \le t5 \\ IswitchON + \dfrac{Vhigh - Vlow}{Lphase} \cdot (t - t5) \ \text{ if } \ t5 < t \le t6 \\ IswitchOFF + \dfrac{-Vlow}{Lphase} \cdot (t - t6) \ \text{ if } \ t6 < t \le \dfrac{DCD + DCM}{Fs} \\ 0 \cdot A \ \text{ if } \left[\left(\dfrac{DCD + DCM}{Fs} \le t \le \dfrac{1}{Fs}\right) \wedge Ideal = 1\right] \\ \left[\dfrac{Vlow}{\omega oscill \cdot Lphase} \cdot \sin[\omega oscill \cdot (t - t11)]\right] \ \text{ if } \left[\left(\dfrac{DCD + DCM}{Fs} \le t \le \dfrac{1}{Fs}\right) \wedge Ideal = 0\right] \end{cases}$$

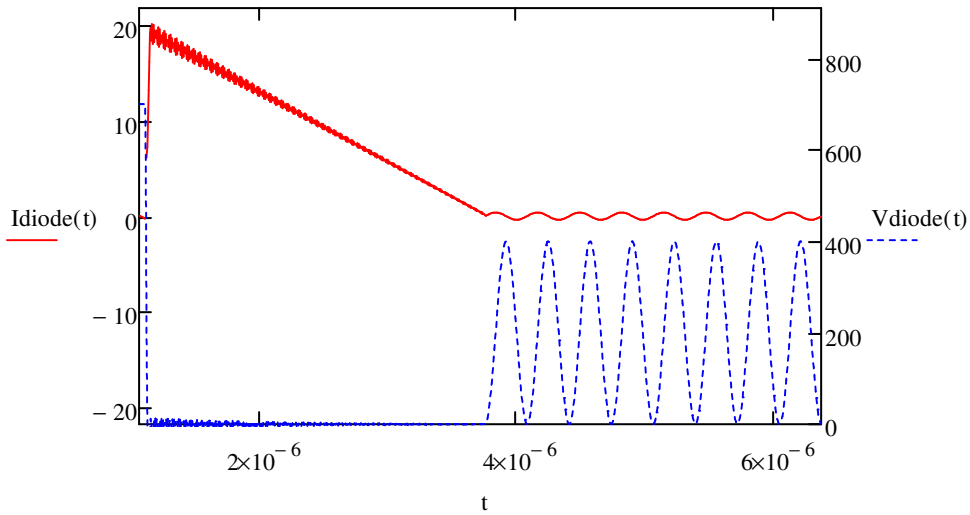
- **Diode :**

$Vdiode(t) := Vhigh - Vds(t)$ $\qquad$ $Idiode(t) := IL(t) - Id(t)$

<u>Turn on:</u>



<u>Turn off :</u>

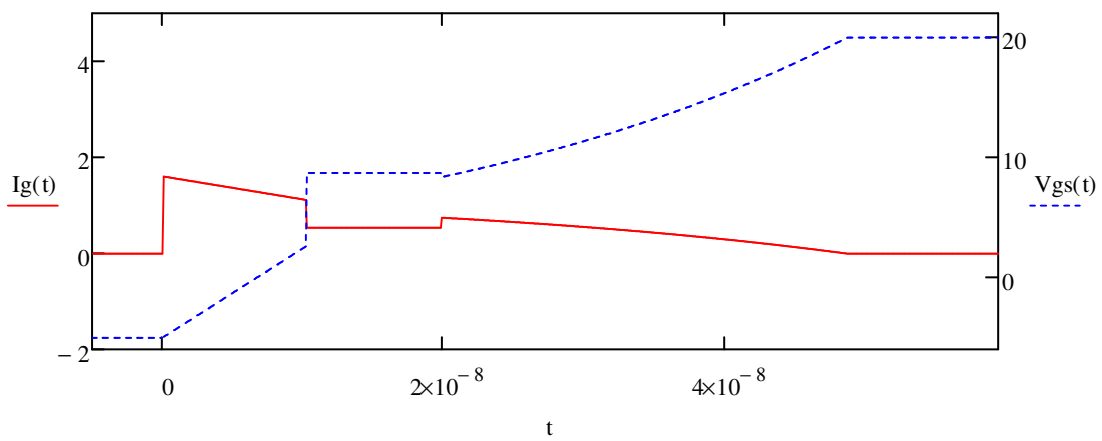


- **Gate circuit :**

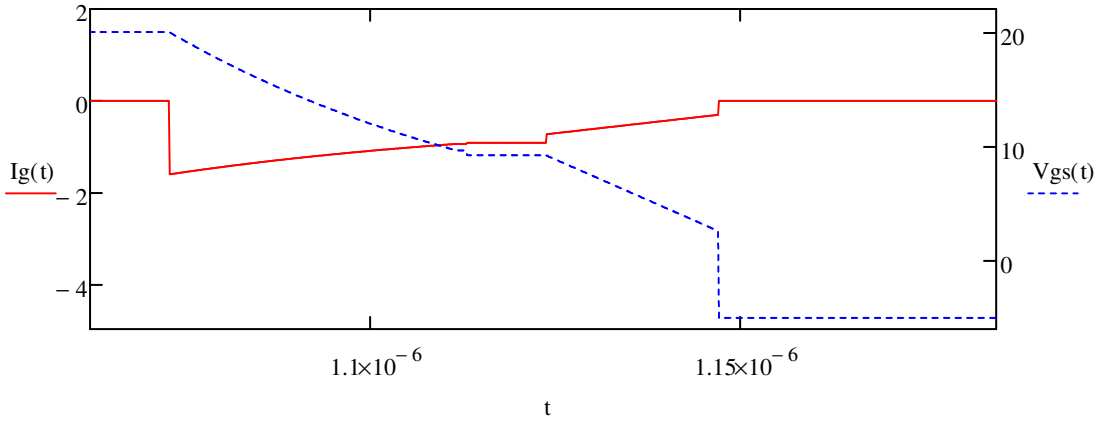
$$
Vgs(t) := \begin{cases}
Vdr_L \quad \text{if } t < t0 \\
Vdr_L + \dfrac{Vth - Vdr_L}{t0t1} \cdot t \quad \text{if } t0 < t \le t1 \\
Vth + \dfrac{Vmiller1_ON - Vth}{t2 - t1} \cdot (t - t1) \quad \text{if } t1 < t \le t2 \\
Vmiller2_ON + \dfrac{(Cd2 + CL)}{gfs} \cdot \dfrac{Vdsr - (Vmiller2_ON - Vth_lin)}{t3 - t2} \quad \text{if } t2 < t \le t3 \\
Vmiller2_ON \quad \text{if } t3 < t \le t4 \\
Vmiller2_ON \cdot \exp\left[\dfrac{\ln\left(\dfrac{Vdr_H}{Vmiller2_ON}\right)}{t5 - t4} \cdot (t - t4)\right] \quad \text{if } t4 < t \le t5 \\
Vdr_H \quad \text{if } t5 < t \le t6 \\
Vdr_H \cdot \exp\left[\dfrac{\ln\left(\dfrac{Vmiller2_OFF}{Vdr_H}\right)}{t7 - t6} \cdot (t - t6)\right] \quad \text{if } t6 < t \le t7 \\
Vmiller2_OFF \quad \text{if } t7 < t \le t8 \\
Vgs9 \quad \text{if } t8 < t \le t9 \\
Vgs9 + \dfrac{Vth - Vgs9}{t10 - t9} \cdot (t - t9) \quad \text{if } t9 < t \le t10 \\
Vdr_L \quad \text{if } t10 < t \le t11 \\
Vdr_L \quad \text{if } t11 < t \le t12
\end{cases}
$$

$$
Ig(t) := \begin{cases}
0.0A \ \text{ if } \ -5ns < t \le t0 \\
\frac{1}{Rg}\cdot(Vdr_H - Vgs(t)) \ \text{ if } \ t0 < t \le t1 \\
\frac{1}{Rg}\cdot\left[Vdr_H - Vgs(t) - (Ls + Mds)\frac{IswitchON}{t1t2}\right] \ \text{ if } \ t1 < t \le t2 \\
Ig3 \ \text{ if } \ t2 < t \le t3 \\
Ig4 \ \text{ if } \ t3 < t \le t4 \\
\frac{Vdr_H - Vgs(t)}{Rg} \ \text{ if } \ t4 < t \le t5 \\
(0A) \ \text{ if } \ t5 < t \le t6 \\
\frac{1}{Rg}\cdot(Vdr_L - Vgs(t)) \ \text{ if } \ t6 < t \le t7 \\
Ig8 \ \text{ if } \ t7 < t \le t8 \\
\frac{1}{Rg}\cdot\left[Vdr_L - Vmiller2_OFF + \frac{(Cd2 + CL)}{gfs}\,\frac{VswitchOFF - (Vmiller2_OFF - Vth)}{t9 - t8}\right] \ \text{ if } \ t8 < t \le t9 \\
\frac{1}{Rg}\cdot\left[Vdr_L - Vgs(t) - (Ls + Mds)\frac{-Ids9}{(t10 - t9)}\right] \ \text{ if } \ t9 < t \le t10 \\
0A \ \text{ if } \ t10 < t \le t11 \\
0A \ \text{ if } \ t11 < t \le t12
\end{cases}
$$

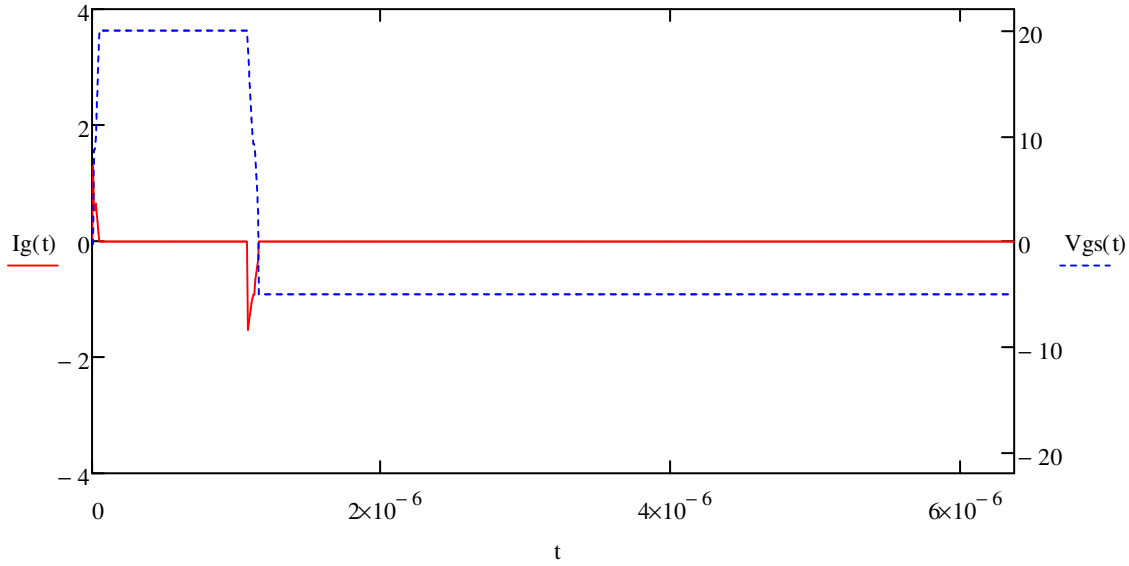
Turn on:



Turn off:


2
0
Ig(t)
− 2
− 4
20
10
Vgs(t)
0
1.1×10^−6
1.15×10^−6
t

1 period:


4
2
Ig(t)
0
− 2
− 4
20
10
0
Vgs(t)
− 10
− 20
0
2×10^−6
4×10^−6
6×10^−6
t

Power Inductor Losses Model

Subject:
This appendix gives the equations to compute the phase inductor losses. This inductor is made of :
- Iron powder toroidal core (frome Magnetics for the present data)
- Copper Litz wire

The inductor of this model is supposed to be potted in a resin that has two main functions:
- assuring the dielectric strenght of the inductor with the heat-sink
- allowing a quite "good" disspipation of the heat to the heat-sink

Material references for the present example:
- inductor core : 77587 from Magntics (KoolMu26)
- Litz wire: from Le Guippage Moderne
- Resine: confidential

1. Input design variables

0. IBC data

Switching frequency : $Fs := 157 \cdot kHz$

IBC output current: $Ilow := 16.4675 \cdot A$

IC number of phases: $Nb_phases := 3$

MOSFET duty-cylce : $DCM := 0.1684$

Diode duty-cycle: $DCD := 0.421$

IBC input voltage value: $Vhigh := 700 \cdot V$

IBC output voltage value: $Vlow := 200 \cdot V$

1. Inductor properties data

Inductance: $Lphase := 27.2 \cdot 10^{-6} \cdot H$

Phase inductor minimum current value: $ILmin := 0 \cdot A$

Phase inductor current ripple: $DIL := 19.789 \cdot A$

Phase inductor RMS current: $ILrms := 8.772 \cdot A$

Inductor core properties:

Inductor core volume: $Lphase_volume_core := 4.391 \cdot cm^3$

Phase inductor cross-section: $Lphase_Ae := 48.45 \cdot mm^2$

Density losses for Steinmetz: $k := 120 \cdot \frac{mW}{cm^3}$

Power Steinmetz coefficient on the freqency: $alpha := 1.46$

Power Steinmetz coefficient on the induction: $beta := 2.09$

Inductor Litz wire properties:

Litz wire DC resistance: $RdcLitz := 0.029\Omega$

Litz wire AC resistance: $RacLitz := 0.032\Omega$

Litz strand section: $Slitz := 7.854 \cdot 10^{-3} \cdot mm^2$

Litz strands number: $nstrandLphase := 138$

Inductor turn number: $Lphase_N := 42$

1. Output variables computation

0. IBC data

DC current: $I_Lphase_DC := \frac{Ilow}{Nb_phases} = 5.489\,A$

1. Inductor core losses : IGSE

The core losses are based on the following paper

[1] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsimisoidal waveforms using only steinmetz parameters," in Proceedings of the IEEE Workshop on Computers in Power Electronics, COMPEL, 2002, vol. 2002–Janua, no. June, pp. 36–41.

A particularly common type of flux waveform in power electronics is piecewise linear (PWL). For PWL waveforms, the integral in (9) may be split into one piece for each linear segment

$$\overline{P_v} = \frac{k_i(\Delta B)^{\beta-\alpha}}{T}\int_0^T \left|\frac{dB}{dt}\right|^{\alpha} dt$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}2^{\beta-\alpha}d\theta}$$

$$\int_0^{2\pi}|\cos\theta|^{\alpha}d\theta = 4\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)$$

parameter for ki computation: $q := 0.2761 + \frac{1.7061}{alpha + 1.354} = 0.882$

Be carefull with the 4 value factor that has not be put here for easy writing reasons

ki computation: $ki := \frac{k}{\pi^{alpha-1}\cdot 2^{beta+1}\cdot q} = 9.433\cdot\frac{mW}{cm^3}$

The core losses formula being large, it is computed in two steps:

$$P := \frac{\left(\frac{Lphase\cdot DIL}{A\cdot H}\right)^{beta-alpha}\cdot Lphase_volume_core\cdot ki\cdot\left[DCM\cdot\left(\frac{Vhigh - Vlow}{V}\right)^{alpha} + DCD\cdot\left(\frac{Vlow}{V}\right)^{alpha}\right]}{\left(Lphase_N\cdot\frac{Lphase_Ae}{m^2}\right)^{beta}}$$

$PLphase_Iron := \left(10^3\right)^{-alpha}\cdot P$ $\quad PLphase_Iron = 15.445\,W$

Volumic losses: $PLphase_iron_vol := \frac{PLphase_Iron}{Lphase_volume_core} = 3.518\cdot\frac{W}{cm^3}$

2. Inductor winding losses :

DC losses: $PLphase_Cu_dc := RdcLitz \cdot I_Lphase_DC^2 = 0.874\,W$

AC losses: $I_Lphase_AC := \sqrt{ILrms^2 - I_Lphase_DC^2} = 6.842\,A$

$PLphase_Cu_ac := RacLitz \cdot I_Lphase_AC^2 = 1.498\,W$

Current density: $Jlitz := \frac{ILrms}{Slitz \cdot nstrandLphase} = 8.093 \cdot \frac{A}{mm^2}$

3. Inductor losses :

Total inductor losses: $PLphase_tot := PLphase_Iron + PLphase_Cu_dc + PLphase_Cu_ac = 17.817\,W$

Inductor efficiency: $\eta_inductor := \frac{\left(\frac{Vlow \cdot Ilow}{Nb_phases}\right) - PLphase_tot}{\left(\frac{Vlow \cdot Ilow}{Nb_phases}\right)} = 0.984$

Semi-conductors thermal model

Subject:
This appendix gives the equations to evaluate the junction temperature of the semi-conductors based on their losses, thermal properties and Sil Pad material properties.

Note: The °C unit will be expressed as K since Mathcad presents some difficulties to handle the °C

1. Input design variables

0. Semi-conductor data

Junction to case thermal resistance and thermal exchange surface: $Rth_jc := 0.767 \cdot \frac{K}{W}$ $Surface := 1.607 \cdot cm^2$

Device lossese: $P := 13.88 \cdot W$

1. Converter requirement

IBC required dielectric voltage rating : $Vdielec_min := 10 \cdot kV$

Cooling plate temperature: $Tcooling := 65 \cdot K$

2. Sil-pad properties

Thermal capacity : $Cth := 4 \cdot \frac{W}{m \cdot K}$

Dielectric strenght : $Vdielec_sil_pad := 20 \cdot \frac{kV}{mm}$

Sil Pad weight : $Sil_pad_density := 2765 \cdot \frac{kg}{m^3}$

2. Output variables computation

0. Sil pad required thickness

Sil pad thickness: $ep := \frac{Vdielec_min}{Vdielec_sil_pad} = 0.5 \cdot mm$

1. Sil pad properties

Sil pad weigth: $Sil_pad_weight := Sil_pad_density \cdot Surface \cdot ep = 0.222 \cdot gm$

Sil pad thermal resistance: $\boxed{Sil_pad_Rth := \frac{ep}{Cth \cdot Surface} = 0.778 \cdot \frac{K}{W}}$

2. temperatures computation

Device case temperature : $Tc := P \cdot Sil_pad_Rth + Tcooling = 75.797\,K$ *So actually 75°C*

Device junction temperature : $Tj := P \cdot (Sil_pad_Rth + Rth_jc) + Tcooling = 86.442\,K$ *So actually 86°C*