

Built-In Self-Test solutions for high-performance and reliable analog, mixed-signal, and RF integrated circuits

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Built-In Self-Test solutions for high-performance and reliable analog, mixed-signal, and RF integrated circuits

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Résumé en français

La capacité d'intégration des technologies CMOS nanométriques actuelles permet la fabrication de systèmes complets et très complexes sur une seule puce (les *Systems-on-Chip*, SoCs) ou dans un seul boîtier (*Systems in Package*, SiPs). Cependant, les procédés de fabrication sont sujets à des imperfections qui peuvent dégrader, parfois de façon catastrophique, la fonctionnalité prévue des circuits fabriqués. Des tests de production approfondis sont alors nécessaires afin de séparer ces pièces défectueuses ou peu fiables des dispositifs fonctionnellement corrects. Malheureusement, la co-intégration de blocs de nature très différente (analogique, mixte, numérique, RF,...) ainsi que l'accès limité aux nœuds internes dans un système intégré rendent le test de ces dispositifs très difficile et coûteux.

Un schéma conceptuel général de l'architecture d'un système de communication sans fil est illustré à la Figure 1. La partie principale d'un tel système est constituée de circuits numériques, qui contiennent généralement des processeurs multicœurs, plusieurs Mo de mémoire et plusieurs processeurs de signaux numériques dédiés. La partie non numérique du système occupe généralement moins de 20 % de la surface totale de silicium et comprend des composants analogiques, mixtes et RF tels que des capteurs, des circuits de conditionnement de signaux, des convertisseurs analogique-numérique, ainsi que des fonctions de réception et de transmission RF. Malgré sa petite taille comparative, le principal goulet d'étranglement dans le test de production de ces systèmes complexes réside dans la partie non numérique. En effet, il est estimé que le coût de test en production d'un système complexe à signaux mixtes peut atteindre 50 % du coût total de production (incluant le silicium et le coût de mise en boîtier) en raison du coût de test des composants non numériques intégrés [1, 2].

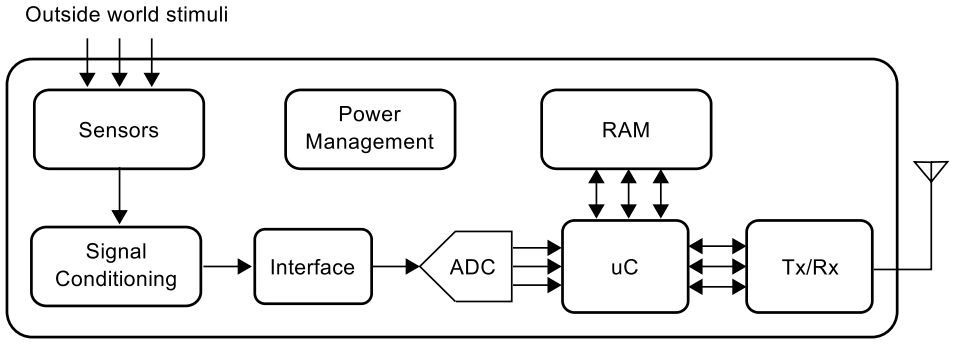


FIGURE 1 – Schéma fonctionnel général d'un SoC/SiP.

Les méthodes de test traditionnelles pour les circuits analogiques, mixtes et RF (AMS-RF) reposent sur des mesures fonctionnelles, c'est-à-dire que l'ensemble des spécifications du circuit est mesuré et comparé aux performances ciblées en conception. D'un point de vue industriel, les tests fonctionnels sont ainsi considérés comme la pierre angulaire du tests AMS-RF. La principale raison est que les fabricants de circuits intégrés commercialisent leur produit sur la base de leur fiche technique, il est donc primordial que les performances indiquées soient exactes. Cependant, les tendances actuelles du marché dans des secteurs en forte croissance (automobile, espace, santé, etc.) exigent le développement de systèmes à signaux mixtes très complexes, étroitement intégrés et avec des exigences strictes en matière de qualité. Caractériser les performances de ces systèmes de pointe dans une chaîne de production est ainsi une tâche difficile. De plus, la validation exhaustive a un coût prohibitif pour la plupart des circuits AMS-RF complexes, car elle nécessite un équipement de test automatisé (ATE) haut de gamme et de longs temps de mesures. À cela s'ajoute le fait que chaque famille de circuits AMS-RF exige un ensemble de configurations de test différentes et un accès dédié aux broches d'entrée-sortie. Afin de répondre aux demandes toujours plus exigeantes en termes de qualité de tels systèmes, les coûts engendrés par leurs test tendent à augmenter. Afin d'inverser cette tendance, il semble essentiel de proposer des paradigmes de test alternatifs.

Des techniques de *Built-In Self-Test* (BIST) ont été proposées afin de répondre à cette problématique. Ces techniques visent à inclure une partie de la fonctionnalité de l'ATE dans le Dispositif Sous Test (*Device Under Test*, DUT), de telle sorte que chaque système fabriqué puisse s'auto-tester, réduisant ainsi la complexité (et donc le coût) de l'ATE externe requis. Idéalement, les instruments de test intégrés devraient être inclus avec le DUT de telle sorte que seul un testeur numérique à faible performance soit nécessaire pour lancer la procédure d'autotest et récupérer les résultats. Ainsi, les techniques BIST peuvent réduire le coût global de production d'un système complexe en prenant en considération le test de ses blocs constitutifs dès le stade de la conception. De plus, les solutions BIST ouvrent la porte à une fiabilité accrue, au test en ligne et à des fonctions de diagnostic utilisables durant le cycle de vie du circuit. La fiabilité et l'amélioration de la qualité deviennent aujourd'hui l'un des principaux moteurs du développement du BIST analogique et mixte. Dans des applications critiques pour la sécurité, comme l'automobile, le BIST devient même une exigence de conception pour de nombreux circuits.

L'application de techniques de BIST à la partie numérique d'un circuit intégré complexe à signaux mixtes est une pratique courante et normalisée. De nombreuses alternatives de test, basées sur des modèles de défauts et largement éprouvées dans la pratique, sont ainsi disponibles. En revanche, les techniques de BIST AMS-RF ne sont pas aussi abouties. D'un point de vue purement théorique, ils devraient être une simple extension de leurs homologues numériques. En ce sens, un schéma général exposant le test d'un système complexe à signaux mixtes serait celui proposé à la Figure 2. Afin de fournir les fonctions de BIST AMS-RF, il suffirait de déplacer les générateurs et les convertisseurs au sein du système à tester. Toutefois, cela est quasiment impossible dans la pratique en raison des exigences strictes imposées par les circuits analogiques. En effet, les circuits AMS-RF sont généralement testés en mesurant leurs spécifications fonctionnelles, ce qui signifie que chaque mesure doit respecter des contraintes de précision strictes pour indiquer correctement les performances des circuits testés. De plus, en raison de l'hétérogénéité des blocs analogiques, mixtes et RF, il serait nécessaire de combiner des générateurs de signaux allant de la bande de base à la RF, avec une linéarité similaire ou supérieure à celle des circuits testés.

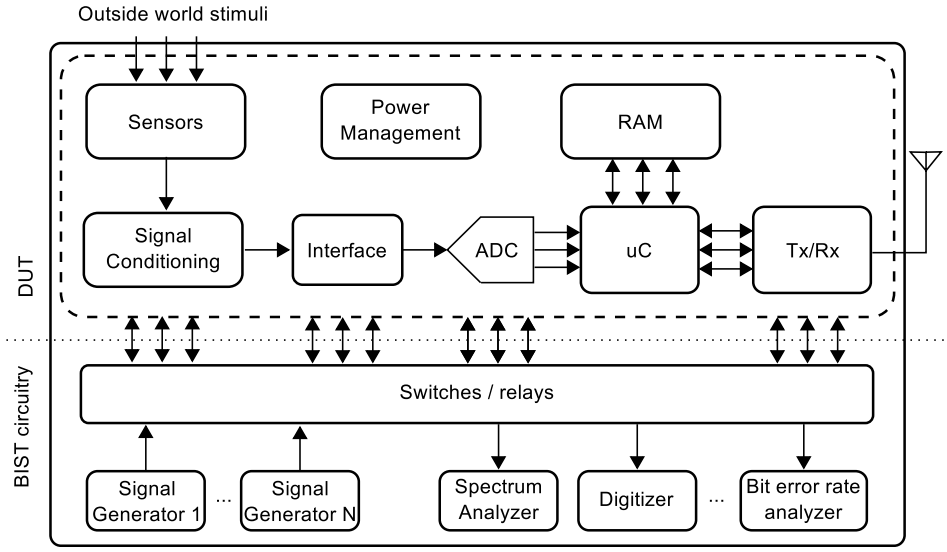


FIGURE 2 – Schéma fonctionnel général d'un SoC/SiP avec BIST.

Une solution prometteuse à ces problèmes est la combinaison de stratégies de BIST et de tests indirects basés sur l'apprentissage automatique (*machine learning*). De telles stratégies permettent de remplacer les coûteuses mesures analogiques, mixtes et RF par un ensemble de mesures plus simples, qui peuvent être effectuées sur puce et par des circuits de test intégrés peu onéreux. L'idée de base est de construire un modèle de régression à partir d'un ensemble de mesures simples, généralement appelées signatures, jusqu'à l'ensemble des spécifications fonctionnelles.

L'approche habituelle du test indirect est basée sur des algorithmes d'apprentissage automatique supervisés. Le processus est développé en deux étapes, comme le montre la Figure 3 : une étape d'apprentissage et une étape de test. Pendant la phase d'apprentissage, les performances et les signatures sont mesurés sur en ensemble de puces (ensemble d'apprentissage). Un algorithme d'apprentissage automatique est ensuite utilisé pour construire un modèle de régression entre performances et signatures. Durant la phase de test, les signatures sont mesurées pour chaque DUT, et les performances sont déduites à l'aide du modèle de régression obtenu à l'étape précédente. L'interprétation des résultats des tests est alors la même que pour les tests fonctionnels conventionnels. C'est ainsi une façon élégante de traiter la question des fenêtres d'acceptation requises pour les différentes performances. Cette approche donne également de précieux renseignements sur la fiabilité puisque les distances entre les performances du DUT et ses spécification nominales sont connues. De plus, les algorithmes d'apprentissage automatique sont conçus pour gérer des relations multidimensionnelles et non linéaires complexes comme celles qui existent entre les défauts de fabrication et les spécifications, et par extension, entre les signatures et les spécifications.

Les principaux avantages de cette méthode de test indirect par apprentissage machine sont les suivants. Tout d'abord, le résultat du test peut être interprété de manière conventionnelle : les spécifications estimées sont directement comparées à leurs fenêtres d'acceptation classiques. Deuxièmement, les mesures simples sont conçues pour être moins coûteuses que leurs homologues fonctionnelles.

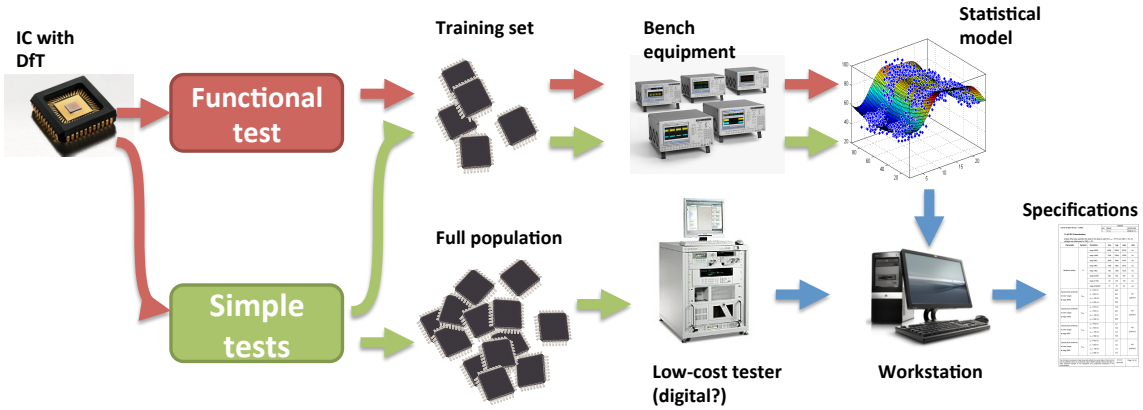


FIGURE 3 – Test indirect basé sur des modèles d'apprentissage automatique supervisés.

Enfin, ces mesures simples peuvent également être adaptées afin d'obtenir une couverture des défauts plus élevée que les spécifications traditionnelles.

Cependant, la stratégie de test basée sur l'apprentissage automatique n'est pas non plus sans faiblesses. Une point clé est de trouver un ensemble approprié de signatures pour construire des modèles de prédiction performants. La proposition d'un ensemble de signatures est généralement *ad hoc*, basée sur une connaissance précise du DUT, et sous-optimale : il peut contenir des informations redondantes, des données non pertinentes, du bruit de mesure, etc. Une autre question qui a attiré l'attention de la communauté ces dernières années est la validation *a priori* du test indirect. C'est-à-dire, l'évaluation de sa qualité, généralement en termes de certains paramètres du test standard, avant le déploiement de la technique dans la chaîne de production. Une autre question fondamentale qui doit être abordée découle de sa philosophie basée sur le modèle : tout phénomène ou erreur non modélisé entraînera de mauvais résultats.

Mes recherches se sont concentrées sur le dépassement des limites des BISTs actuels et des tests basés sur l'apprentissage automatique pour les circuits AMS-RF complexes, dans le but final de fournir des solutions de test innovantes et de pointe pour de tels systèmes. Mes activités de recherche peuvent être structurées selon deux grands axes interdépendants, à savoir :

a. Développement de nouvelles techniques pour incorporer des techniques de BIST dans des circuits AMS-RF haute performance.

b. Développement de méthodologies systématiques pour la conception de programmes de test précis et fiables basés sur l'apprentissage automatique pour les circuits AMS-RF.

Le reste du document est structuré en deux grandes sections qui reflètent les axes de recherche présentés ci-dessus. La première section, centrée sur les applications BIST à signaux mixtes, comprend les chapitres 2 à 5, où je détaille mes recherches sur le développement de nouvelles solutions pour la caractérisation statique et dynamique des convertisseurs analogique-numérique. La deuxième section, centrée sur les applications d'apprentissage automatique, comprend les chapitres 6 et 7, où je

détaille mes recherches sur les algorithmes de sélection des caractéristiques et l'automatisation de la conception des signatures pour les applications de test indirect.

Le chapitre 2 présente un générateur de stimulus de rampe sur puce destiné aux applications de test de linéarité statique pour les convertisseurs analogique-numérique (*Analog-to-Digital Converter*, ADC). Le générateur de rampe proposé est basé sur un simple intégrateur à capacité commutée avec une entrée DC constante. L'intégrateur a été modifié pour produire un gain d'intégration très faible et proportionnel à la différence de capacité des deux condensateurs. Ainsi, le signal de rampe à la sortie présente un pas de taille inférieure au bit de poids le plus faible (*Least Significant Bit*, LSB) de l'ADC sous test. Afin de vérifier la faisabilité de la technique de génération de rampe proposée, un prototype a été conçu et fabriqué en utilisant la technologie CMOS 65 nm de STMicroelectronics. Les résultats expérimentaux obtenus sur 15 échantillons fabriqués montrent une linéarité moyenne de 14,5 bits effectifs dans une plage de sortie différentielle de ± 2 V. De plus, la stratégie de mesure de linéarité statique proposée est vérifiée sur un ADC 11 bits. Les résultats expérimentaux montrent une précision de $\pm 0,3$ LSB dans la mesure de la non-linéarité intégrale (INL) de l'ADC sous test.

Le chapitre 3 présente la conception d'un générateur de signaux sinusoïdaux sur puce, basé sur une stratégie d'annulation d'harmonique calibrée. Le générateur proposé utilise un registre numérique à décalage pour fournir un ensemble de signaux numériques déphasés. Ces signaux rectangulaires sont pondérés et combinés en utilisant un convertisseur numérique-analogique simplifié. L'architecture proposée permet l'annulation de toutes les harmoniques jusqu'à l'onzième. La simplicité du système proposé rend cette approche appropriée pour les applications de BIST à signaux mixtes. Un prototype du générateur de signaux sinusoïdaux a été intégré en utilisant la technologie FDSOI 28 nm de STMicroelectronics. Les résultats expérimentaux obtenus montrent un SFDR de 52 dB pour un signal sinusoïdal généré à 166,67 MHz. Le générateur a été testé dans une gamme de fréquences de fonctionnement allant de 1 MHz à 333 MHz.

Le chapitre 4 présente une architecture de BIST entièrement numérique pour le test dynamique d'ADCs $\Sigma\Delta$. Le BIST proposé repose sur la génération d'une sequence numérique ternaire qui code un signal sinusoïdal analogique de haute linéarité et l'injecte directement à l'entrée du modulateur $\Sigma\Delta$. Par rapport à une sequence binaire, l'utilisation de trois niveaux logiques réduit le bruit de quantification et, par conséquent, permet d'obtenir un test avec une plage dynamique plus élevée, couvrant toute celle de l'ADC. La réponse en sortie est analysée sur puce en utilisant une version simplifiée de l'algorithme d'ajustement sinusoïdal pour calculer le SNDR. Un bus SPI standard fournit un accès externe numérique aux instruments de test embarqués. Le BIST proposé a été intégrée dans un ADC $\Sigma\Delta$ 18 bits réalisé dans une technologie CMOS 40 nm fournie par STMicroelectronics. Les résultats expérimentaux sur des puces fabriquées démontrent une excellente corrélation entre le BIST et le test fonctionnel standard.

Le chapitre 5 présente une méthodologie générique permettant d'évaluer une technique de test alternative par rapport à la technique standard. La méthodologie cible spécifiquement les circuits dont les temps de simulation au niveau transistors sont longs et qui ne peuvent donc pas être traités par les méthodologies existantes. Elle se base sur des simulations Monte Carlo et est accélérée par l'utilisation de la technique de *statistical blockade*. On obtient alors un ensemble d'instances de circuits extrêmes qui réussissent ou échouent marginalement aux spécifications. Cet ensemble permet d'étudier facilement l'équivalence des techniques de test alternatives et standard, lorsque les circuits sont loin de leur

point de conception nominal et où des erreurs de classification peuvent survenir. La méthodologie est illustrée pour l'évaluation d'une stratégie de BIST appliqué à un ADC $\Sigma\Delta$ à 18-bit.

Le chapitre 6 présente une méthode de calcul efficace pour la sélection des signatures pour le test indirect basée sur une approche de recherche par corrélation. Elle s'appuie sur la mesure de corrélation de distance brownienne multivariée, métrique de corrélation de la distances par paire de données de l'espace d'entrée (l'espace des caractéristiques) et de l'espace de sortie (l'espace des performance). A chaque itération de l'algorithme de recherche, on sélectionne la caractéristique qui correspond le mieux aux résidus de l'itération précédente. La recherche par corrélation de distance brownienne surpasse les méthodes de sélection de caractéristiques précédentes à une fraction de leur coût de calcul. C'est une approche fiable pour une sélection de caractéristiques efficace, qui peut donc être utilisée pour identifier rapidement les ensembles de signatures appropriés pour effectuer un test indirect à un coût de calcul réduit.

Le chapitre 7 présente des méthodes génériques et automatisées pour trouver un ensemble approprié de mesures indirectes et guider la conception du programme de test indirect. La méthodologie proposée repose sur une analyse des causes fondamentales de la variation des performances. Les méthodologies proposées sont validées sur deux cas d'études différents, à savoir un amplificateur à faible bruit à 2,5 GHz conçu dans une technologie CMOS 90 nm et un amplificateur de puissance à 60 GHz conçu dans une technologie BiCMOS 55 nm.

Enfin, dans le chapitre 8, nous présentons les perspectives envisageables pour de futurs travaux.

Curriculum Vitae

Personal data

Born in Seville, Spain, 19th August 1980.

Education

— **European Ph.D. in Microelectronics** *July 2009*
Universidad de Sevilla, Spain
Thesis Title: On-Chip Generation and Evaluation of Analog Test Signals for Analog and Mixed-Signal BIST Applications
Thesis Supervisor: Dr. Diego Vázquez

— **Licenciado en Física (5-year degree in Physics), graduated with honors, ranked first in class** *June 2003*
Universidad de Sevilla, Spain.

Current Professional Position

Chargé de Recherche CNRS at Laboratoire TIMA, Grenoble, France *1st October 2014*

Research Interests

Analog/Mixed-Signal/RF design and test, Built-In Self-Test, machine learning.

Previous Positions

— Collaborateur Expert at Grenoble INP - Laboratoire TIMA, Grenoble, France, 1st May 2013 - 30th September 2014.

— Post-Doctoral Researcher, CSIC, Instituto de Microelectrónica de Sevilla - Spanish National Microelectronics Center (IMSE-CNM-CSIC), Seville, Spain, 1st May 2010 - 30th April 2013.

— Researcher under contracts associated to National and European Research Projects, CSIC, Instituto de Microelectrónica de Sevilla - Spanish National Microelectronics Center (IMSE-CNM-CSIC), Seville, Spain, 1st October 2007 - 30th April 2010.

— Internship at NXP Research (Previously Philips Research), Mixed-Signal Circuits and Systems Group, Eindhoven, The Netherlands, 3rd April 2006 - 31st July 2006.

— Pre-Doc Grant from the Spanish National Program "FPU: Formación de Profesorado Universitario", University of Seville, Seville, Spain, 23rd January 2004 - 30th November 2007.

Publications

Bibliometrics:

— Google Scholar personal profile: *https://scholar.google.fr/citations?user=Ukr0QhcAAAAJ&hl=es&oi=ao*

— *h*-index: 11 (Source: Google Scholar)

— *i*10-index: 13 (Source: Google Scholar)

— Total number of citations: 347 (Source: Google Scholar)

— International journal papers: 16

— Editorials in international journals: 2

— Peer-reviewed international conference papers: 44

— Book chapters: 3

— Invited talks: 4

— Patents: 2

— Others: 2

Journal papers:

1 R. S. Feitoza, M. J. Barragan, D. Dzahini and S. Mir, "Reduced-code static linearity test of split-capacitor SAR ADCs using an embedded incremental $\Sigma\Delta$ converter," in IEEE Transactions on Device and Materials Reliability, 2019, *early access*. DOI: 10.1109/TDMR.2019.2891298.

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10 A. Zjajo, M. J. Barragan, J. Pineda de Gyvez, "Low-Power Die-Level Process Variation and Temperature Monitors for Yield Analysis and Optimization in Deep-Submicron CMOS", IEEE Transactions on Instrumentation and Measurement, vol 16, no. 8, pp. 2212 - 2221, 2012.

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1 K. Huang, M. J. Barragan, "Guest Editorial: Analog, Mixed-Signal and RF Testing", Journal of Electronic Testing, 2018, vol. 34, no 3, pp 213-214.

2 M. J. Barragan, W. R. Eisenstadt, "Guest Editorial: Analog, Mixed-Signal and RF Testing", Journal of Electronic Testing, 2017, vol. 33, no 3, pp 281-282.

Book chapters:

1 A. Gines, R. Fiorelli, A. Villegas, R. Doldan, M. Barragan, D. Vazquez, A. Rueda, E. Peralias, "Chapter 7: Design of an energy-efficient ZigBee Transceiver", Mixed-Signal Circuits, Edited by Thomas Noulis and Mani Soma, CRC Press, October 23, 2015

2 M. Dubois, H. G. Stratigopoulos, S. Mir, M. J. Barragan, "Statistical Evaluation of Digital Techniques for Sigma-Delta ADC BIST", VLSI-SoC: Internet of Things Foundations, Edited by Luc Claesen, Maria-Teresa Sanz-Pascual, Ricardo Reis, Arturo Sarmiento-Reyes, Springer International Publishing, 2015, ISBN 978-3-319-25279-7.

3 M. J. Barragan, R. Fiorelli, G. Leger, A. Rueda, J. L. Huertas, "20th Anniversary Compendium of Papers from Asian Test Symposium" Chapter 2011-1: Improving the accuracy of RF alternate test using multi-VDD conditions, IEEE Computer Society, 2011.

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1 H. Malloug, M. J. Barragan, S. Mir, "A 52 dB-SFDR 166 MHz sinusoidal signal generator for mixed-signal BIST applications in 28 nm FDSOI technology", accepted for publication in Proc. of IEEE European Test Symposium (ETS), 2019.

2 F. Cilici, M. J. Barragan, S. Mir, E. Lauga-Larroze, S. Bourdel, and G. Leger, "Yield recovery of mm-wave power amplifiers using variable decoupling cells and one-shot statistical calibration", accepted for publication in Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), 2019.

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4 F. Cilici, M. J. Barragan, S. Mir, E. Lauga-Larroze, S. Bourdel, "Assisted test design for non-intrusive machine learning indirect test of millimeter-wave circuits", in Proc. of European Test Symposium (ETS), 2018. **Best Paper Award**

5 M. Margalef-Rovira, M. J. Barragan, P. Ferrari and E. Pistono, "An Oscillation-Based Test technique for on-chip testing of mm-wave phase shifters", in Proc. of VLSI Test Symposium (VTS), 2018. **Selected Best Paper Candidate**

6 G. Leger, M. J. Barragan, "Mixed-signal test automation: are we there yet?", in Proc. of International Symposium on Circuits and Systems (ISCAS), 2018.

7 M. J. Barragan, G. Leger, A. Gines, E. Peralias, A. Rueda, “On the limits of machine learning-based test: a calibrated mixed-signal system case study”, in Proc. of Design Automation and Test in Europe, 2017. **Selected Best Paper Candidate**

8 H. Stratigopoulos, M. J. Barragan, S. Mir, H. Le-Gall, N. Bhargava, A. Bal, “Evaluation of Low-Cost Mixed-Signal Test Techniques for Circuits with Long Simulation Times” in Proc. of the IEEE International Test Conference, 2015. **Selected Top Papers from ITC 2015**

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10 M. J. Barragan, D. Vazquez, A. Rueda, “Practical Implementation of a Network Analyzer for Analog BIST Applications”, in Proc. of Design, Automation, and Test in Europe, 2008.

11 A. Zjajo, M. J. Barragan, J. Pineda de Gyvez, “BIST method for die-level process parameter variation monitoring in analog/mixed-signal integrated circuits”, in Proc. of Design, Automation, and Test in Europe, 2007.

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13 H. Malloug, M. J. Barragan, S. Mir, L. Bastères, H. Le Gall, “Design of a sinusoidal signal generator with calibrated harmonic cancellation for mixed-signal BIST in a 28 nm FDSOI technology”, in Proc. of the 22nd European Test Symposium (ETS), 2017.

14 G. Renaud, M. Margalef-Rovira, M. J. Barragan, S. Mir, “Analysis of an efficient on-chip servo-loop technique for reduced-code static linearity test of pipeline ADCs,” in Proc. of the 35th IEEE VLSI Test Symposium (VTS), 2017.

15 G. Leger and M. J. Barragan, “Questioning the reliability of monte carlo simulation for machine learning test validation”, in Proc. of 21st IEEE European Test Symposium (ETS), 2016.

16 A. J. Gines, E. Peralias, G. Leger, A. Rueda, G. Renaud, M. J. Barragan, and S. Mir, “Linearity Test of High-speed High-performance ADCs using a Self-Testable On-chip Generator,” in Proc. of 21st IEEE European Test Symposium (ETS), 2016.

17 M. J. Barragan, G. Leger, F. Azais, R. D. Blanton, A. Singh, and S. Sunter, “Special Session: Hot Topics: Statistical Test Methods,” in IEEE 33rd VLSI Test Symposium (VTS), 2015. **VTS 2015 Best Special Session Award**

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19 M. J. Barragan, G. Leger, “Efficient selection of signatures for analog/RF alternate test”, in Proc. of the IEEE European Test Symposium, 2013.

20 M. J. Barragan, G. Leger, J. L. Huertas, “OBT for settling error test of sampled data systems using signal-dependent clocking”, in Proc. of the IEEE European Test Symposium, 2012.

21 M. J. Barragan, R. Fiorelli, G. Leger, A. Rueda, J. L. Huertas, “Improving the accuracy of RF alternate test using multi-VDD conditions: application to envelope-based test of LNAs”, in Proc. of the IEEE Asian Test Symposium, 2011.

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1 R. Silveira-Feitoza, M. J. Barragan, S. Mir, D. Dzahini, "Reduced-code static linearity test of SAR ADCs using a built-in incremental $\Sigma\Delta$ converter", Proc. of IEEE International Symposium on On-Line Testing and Robust System Design, 2018.

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5 A. J. Gines, E. Peralias, G. Leger, A. Rueda, G. Renaud, M. J. Barragan, and S. Mir, "Design Trade-offs for On-chip Driving of High-speed High-performance ADCs in Static BIST Applications," in Proc. of IEEE International Mixed-Signal Testing Workshop, 2016.

6 H. Mallough, M. Barragan, S. Mir, H. Le-Gall, "Mostly-digital design of sinusoidal signal generators for mixed-signal BIST applications using harmonic cancellation" in Proc. of IEEE International Mixed-Signal Testing Workshop, 2016.

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18 M. J. Barragan, D. Vazquez, G. Huertas, A. Rueda, J. L. Huertas, "Efficient and Accurate Analog Sinewave Generator for BIST Applications", in Informal Digest of Papers from IEEE European Test Symposium, 2006.

19 M. J. Barragan, D. Vazquez, A. Rueda, J. L. Huertas, "On-chip analog sine wave generator with reduced circuitry resources", in Proc. of the IEEE Midwest Symposium on Circuits and Sytems, 2006.

20 M. J. Barragan, D. Vazquez, A. Rueda, "Guidelines for the Design of a Sine-Wave Analyzer for BIST Applications", in Proc. of the Conference on Design of Circuits and Integrated Systems, 2004.

Invited talks:

1 G. Leger, M. J. Barragan, "Mixed-signal test automation: are we there yet?", in Proc. of International Symposium on Circuits and Systems (ISCAS), 2018.

2 G. Leger, M. J. Barragan, "Why is systematic AMS-RF test not there yet?", in IEEE CEDA-NANOVAR Workshop, November 2017.

3 M. Barragan, G. Leger, "Efficient strategies for feature selection and discovery in machine learning test applications" XXX Conference on Design of Circuits and Integrated Systems, Estoril, Portugal, November 25-27, 2015.

4 M. Dubois, H. Stratigopoulos, M. Barragan, R. Alhakim, S. Mir, "Analog/RF test problem solving with statistically sampled data", Invited Elevator Talk at the 32nd IEEE VLSI Test Symposium, Napa, USA, May 14-16, 2014.

Other publications:

1 M. Margalef-Rovira, M. J. Barragan, E. Pistono, S. Bourdel, P. Ferrari, "Conception de déphaseurs RTPS faible consommation en bande millimétrique", accepted for publication in XXIèmes Journées Nationales Microondes, 2019.

2 H. Malloug, M. J. Barragan, S. Mir, "Conception d'un Générateur de Signal Sinusoïdal Basé sur les Techniques d'Annulation d'Harmonique en 28nm FDSOI". 13ème Colloque National du GDR SoC-SiP, 2018.

3 F. Cilici, M. J. Barragan, E. Lauga-Larroze, S. Bourdel, S. Mir, "Conception en vue du test d'un amplificateur de puissance a 60 GHz", Journees Nationales du Reseau Doctoral en Micro-Nanoelectronique, 2017, **Best Poster Award: Design and Test Micro-Nano**.

Patents:

1 PCT Patent WO2008/135917A1 and US Patent US8310265B2: A. Zjajo, M. J. Barragan, J. Pineda de Gyvez, "IC Testing Method and Apparatus", holding institution: NXP B. V., 30/4/2008 and 13/11/2012, respectively.

2 PCT Patent WO2013/001131A1: J. L. Huertas, M. J. Barragan, "Method and system for testing integrated radio-frequency circuits at the wafer level and the use thereof", holding institution: Consejo Superior de Investigaciones Científicas, 3/1/2013.

Participation in Research Projects Funded in Competitive Calls

— **IndieTEST: Indirect Test Solutions for analog, Mixed-Signal and RF Systems**
Funding institutions: CNRS PICS, project PICS07703
Role: Project leader
Budget managed: 12000 € (4000 € per year)
2017-2019

— **CAFE&Test: Causal feature selection for machine learning test of analog, mixed-signal and RF systems**
Funding institutions: LabEx PERSYVAL-Lab (ANR-11-LABX-0025-01) funded by the French program Investissement d'avenir
Role: Project leader
Budget managed: 6000 €
1 April 2016-30 September 2017

— **Structures embarquées pour le test dynamique de circuits mixtes**
Funding Institution: Programme de recherche & développement coopératif Nano 2017, Lot 9.5.2.
Role: researcher

2014-2017

— **TARANTO: TowARds Advanced bicmos NanoTechnology platforms for rf to the applicatiOns**
Funding Institution: ECSEL Joint Undertaking
Role: researcher
2017-2020

— **HADES: Hierarchy-Aware and secure embedded test infrastructure for Dependability and performance Enhancement of integrated Systems**
Funding institutions: PENTA European Program
Role: Task leader for Task "Embedded Test Instruments for performance measurement and improvement"
2017-2020

— **ELESIS: European library-based flow of embedded silicon test instruments**
Funding institutions: ENIAC European Program
Role: researcher
2012-2015

— **SR2: Short Range Radio**
Funding institutions: Catrene European Program, projets 2A105-CATRENE / TSI-020400-2008-71 and 2A105-CATRENE / TSI-020400-2010-55
Role: researcher
2008 - 2011

— **TOETS: Toward One European Test Solution**
Funding Institution: Catrene European Program, project CT-302
Role: researcher
2009 - 2011

— **Development of Test Solutions for Complex Analog and RF Microelectronic Circuits**
Funding Institution: Spanish Research Council (CSIC), project 200450E667
Role: researcher
2009 - 2011

— **DANTE: Adapting Mixed-Signal and RF IC Design to Process and Environmental Variations**
Funding institution: Spanish Ministry of Science and Innovation, project: EC2011-28302
Role: researcher
2012 - 2014

— **ACATEX: Self-Calibration and Self-Test in Analog Mixed-Signal and RF Circuits**
Funding institution: Andalusian Regional Government, project P09-TIC-5386
Role: researcher
2010 -2013

— **TEST: Techniques for improving test quality and design performance in submicron CMOS technologies**
Funding institution: Spanish Ministry of Science and Innovation, project TEC-2007-68072/MIC
Role: researcher
2007 - 2009

— **TEMITE: Design and Test Techniques for Mixed-Signal ICs in Emerging Technologies**
Funding institution: Andalusian Regional Government, project: EXC/2005/TIC-927
Role: researcher
2006 - 2008

— **TAMBIST: Design-for-Test for high-performance analog and mixed-Signal Circuits with special focus in Built-In Self-Test**
Funding institution: Spanish Ministry of Science and Innovation, project TEC2004-02949
Role: researcher
2004 - 2006

Organization of scientific events and editorial work

— Guest Editor for the Journal of Electronic Testing: Theory and Applications (JETTA) Special Issue on analog, mixed-signal and RF test, vol. 33, no 3, 2017.

— Guest Editor for the Journal of Electronic Testing: Theory and Applications (JETTA) Special Issue on analog, mixed-signal and RF test, vol. 34, no 3, 2018.

— Review Editor at Wiley International Journal of Circuit Theory and Applications since 2014.

— Program Chair of the 22st IEEE International Mixed-Signal Testing Workshop, Thesaloniki, Greece, July, 2017.

— Program Chair of the 21st IEEE International Mixed-Signal Testing Workshop, Sant Feliu de Guixols, Spain, July 4-6, 2016.

— Program Chair of the 5th IEEE International Workshop on Test and Validation of High Speed Analog Circuits, Phoenix, Arizona, USA, November 1-2, 2018.

— Program Chair of the 4th IEEE International Workshop on Test and Validation of High Speed Analog Circuits, Disneyland Hotel, Anaheim, California, USA, October 8-9, 2015.

— General Chair of the 1^{st} Statistical Test Methods Workshop, fringe event to the 19^{th} IEEE European Test Symposium, Paderborn, Germany, 29-30 May, 2014.

— Topic co-chair for the 21^{st} IEEE International Conference on Electronics Circuits and Systems, Topic 12: Test, Reliability, and Fault Tolerance, Marseille, France, 7-10 December, 2014.

— Topic co-chair for the IFIP/IEEE International Conference on Very Large Scale Integration, Topic: Machine learning for SoC design and Electronic Design Automation, 2018.

— Topic chair for the IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Topic: Analog Design and Test, 2018.

— Review Committee member for IEEE International Symposium on Circuits and Systems (ISCAS), 2018.

— Program Committee member for the IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2018.

— Program Committee member for topic Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS, at Design Automation and Test in Europe for DATE 2016, 2017 and 2018 editions.

— Program Committee member for IEEE European Test Symposium, 2017 and 2018 editions.

— Program Committee member for IEEE VLSI Test Symposium, 2017 and 2018 editions.

— Program Committee member for IEEE Computer Society Annual Symposium on VLSI, 2016, 2017, and 2018 editions.

— Program Committee member for the 20th IEEE International Mixed-Signal Testing Workshop, 2015, 2016, 2017, and 2018 editions.

Research awards

— ETS 2018 Best Paper Award, IEEE European Test Symposium 2018.

— VTS 2018 Best Paper Candidate, IEEE VLSI Test Symposium 2018.

— JNRDM 2017 Best Poster Award: Design and Test Micro-Nano, Journees Nationales du Reseau Doctoral en Micro-Nanoelectronique, 2017.

— DATE 2017 Best Paper Candidate, Design Automation and Test in Europe 2017.

— VTS 2015 Best Special Session Award, IEEE VLSI Test Symposium 2015.

— Selected Best Contributions Presented in Asian Test Symposium from 2002 to 2011, awarded by IEEE Computer Society Test Technology Technical Council, 2011.

— Silver Leaf Award from the IEEE Ph.D. Research on Microelectronics and Electronics (IEEE PRIME Conference).

Teaching

— **Design for Test**
Degree: Master Electronique, Énergie Électrique, Automatique; Second year, Specialization in

Wireless Integrated Circuits and Systems (WICS)
University: Université Grenoble-Alpes
School year: 2016-2017, 2017-2018, and 2018-2019
Hours: 10 per school year

— **Electrónica Básica (Basic Electronics)**
Degree: Licenciado en Física (5-year degree in Physics); Second year
University: Universidad de Sevilla
School year: 2006-2007
Hours: 30

— **Técnicas experimentales en electrónica (Experimental Techniques in Electronics)**
Degree: Licenciado en Física (5-year degree in Physics); Fourth year
University: Universidad de Sevilla
School year: 2005-2006
Hours: 20

Supervision of PhD students

— **Co-supervisor of PhD student Guillaume Renaud, 2013-2016**
Supervisors: Salvador Mir (30%); Manuel J. Barragan (70%)
PhD project: Auto Test de Convertisseurs de Signal de Type Pipeline
PhD thesis defended on November 2016
Current position: Ingénieur de recherche, CEA - Commissariat à l'énergie atomique et aux énergies alternatives, Grenoble, France

— **Co-supervisor of PhD student Hani Malloug, 2014-2018**
Supervisors: Salvador Mir (20%); Manuel J. Barragan (80%)
PhD project: Built-in test strategies for dynamic test of high-performance Analog-to-Digital Converters
NANO2017 joint collaboration project with STMicroelectronics
PhD thesis defended on September 2018
Current position: Post-doc position at Pyxcad (Common Laboratory TIMA-Xdigit)

— **Co-supervisor of PhD student Florent Cilici, 2016-**
Supervisors: Salvador Mir (25%); Sylvain Bourdel (25%); Manuel J. Barragan (25%); Estelle Lauga-Larroze (25%)
PhD project: Development of Built-In Self-Test solutions for RF/mmW integrated circuits
Sujet fléché Ecole doctorale EEATS, Grenoble
Joint collaboration with IMEP-LaCH (UMR 5130)

— **Co-supervisor of PhD student Marc Margalef-Rovira, 2017-**
Supervisors: Philippe Ferrari (30%); Emmanuel Pistono (30%); Manuel J. Barragan (30%), Christophe Gaquière (10%)
PhD project: On-chip test structures for self-test and self-calibration applications of phase-shifters in millimeter-wave phased arrays.
TARANTO project: joint collaboration TIMA, IMEP-LaHC, STMicroelectronics

— **Supervisor of PhD student Renato Silveira-Feitoza, 2017-**
Supervisors: Manuel J. Barragan (70%); Salvador Mir (30%)
PhD project: Reduced-code linearity test techniques for high-performance SAR ADCs
HADES project: joint collaboration with STMicroelectronics

Supervision of Master students

— Marc Margalef-Rovira: Master WICS (PHITEM, Univeristé Grenoble Alpes): "Exploration and design of test structures for self-test applications of phase shifters in millimeter-wave phased arrays", Co-supervised by M.J. Barragan, E. Pistono, P. Ferrari. Defended on 30/06/17.

— Marc Margalef-Rovira: E2I 4A (Polytech Grenoble): "Digital design of a Code Selector for ADC BIST applications using a Reduced Code Linearity Test Technique", Supervised by M. J. Barragan. Defended on 20/06/16.

Other responsibilities

— FMNT, Federation des Micro Nano Technologies, FR 2542, (CNRS, Grenoble INP, UGA)
Role: Coordinator of strategic axe "Composants et systèmes pour les télécommunications"

Chapter 1

Introduction

1.1 Background

The integration capabilities offered by current nanoscale CMOS technologies enable the fabrication of complete and very complex mixed-signal systems on a single die (the so-called Systems on Chip, SoCs) or in a single package (Systems in Package, SiPs). However, manufacturing processes are prone to imperfections that may degrade –sometimes catastrophically– the intended functionality of the fabricated circuits. Extensive production tests are then needed in order to separate these defective or unreliable parts from functionally correct devices. Unfortunately, the co-integration of blocks of very distinct nature (analog, mixed-signal, digital, RF, ...) as well as the limited access to internal nodes in an integrated system make the test of these devices a very challenging and costly task.

A general conceptual scheme for the architecture of these systems is shown in Figure 1.1, where any generic wireless-based application is virtually covered. By far, the largest portion of these systems is digital circuitry, that usually contains multi-core processors, multiple Mbytes of memory, and several dedicated digital signal processors. The non-digital part of the system typically occupies less than 20% of the total silicon area, and it includes analog, mixed-signal, and RF components such as input

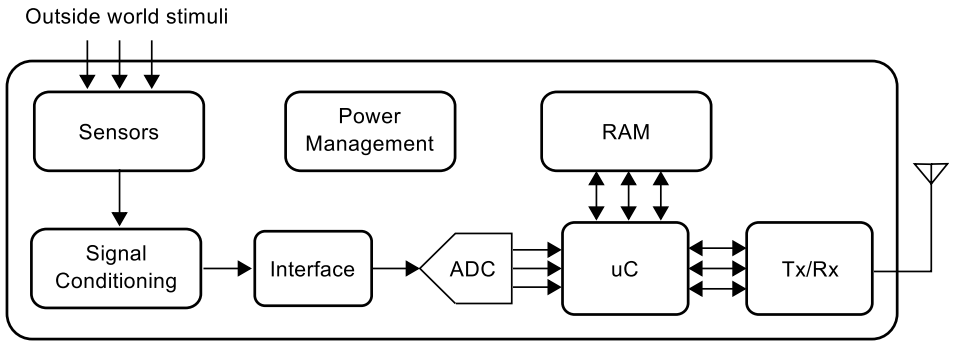


Figure 1.1 – General SoC/SiP block diagram.

sensors, signal conditioning circuitry, Analog-to-Digital converters, as well as RF receive and transmit functions. Despite its small comparative size, the main bottleneck in the production test of these complex systems lies in the non-digital portion. Indeed, it has been estimated that the cost of testing a complex mixed-signal system at the production line can escalate up to 50% of the overall production cost (including silicon and packaging cost) due to the cost of testing embedded non-digital components [1, 2].

Traditional test methods for analog, mixed-signal and RF (AMS-RF) circuits rely on functional measurements, that is, the complete set of the circuit specifications is measured and compared to the target design performance. From an industrial point of view, functional tests are indeed considered as the cornerstone of AMS-RF testing. There is a simple reason for that: IC manufacturers market circuits based on their data-sheet, and hence it is of paramount importance that the performance figures listed in the data-sheet are accurate. We could even wonder if the functional test paradigm should be questioned. However, current market trends in rapidly growing sectors (e.g., automotive, space, healthcare, etc.) demand the development of very complex, tightly integrated mixed-signal systems with stringent test quality requirements. Characterizing the performance of these state-of-the art systems in a production line is a challenging task. Moreover, exhaustive validation is prohibitively costly for most AMS-RF circuits of reasonable complexity, since it requires high-end Automated Test Equipment (ATE) and long test times. Not to mention that each AMS-RF circuit family demands a set of different test setups and dedicated test access to its input-output pins for very diverse measurements. The main reason for challenging the functional test golden standard is the ever increasing cost of guaranteeing quality. The production of current and future mixed-signal systems demands an alternative test paradigm in order to achieve the required test quality at a lower test cost.

Built-In Self-Test (BIST) techniques have been proposed as a way to overcome these issues. These techniques aim at including some of the ATE functionality into the Device Under Test (DUT), in such a way that each fabricated system becomes self-testable, thus reducing the complexity –and hence the cost– of the required external ATE. Ideally, embedded test instruments would be included together with the DUT and only a low-performance digital tester would be needed to launch the self-test procedure and retrieve the test results. Thus, BIST may reduce the overall production cost of a complex system by taking into consideration the test of its constituent blocks at the design stage. Moreover, BIST solutions also open the door to enhanced reliability, on-line test, and diagnosis features along the complete life cycle of an integrated circuit. Indeed, reliability and quality enhancement is becoming one of the main drivers for the development of analog and mixed-signal BIST. For instance, in safety critical applications such as automotive, BIST is even becoming a design requirement for many applications.

Applying BIST to the digital part of a complex mixed-signal integrated circuit is a common and standardized practice. Many test alternatives broadly proven in practice are available, all of them based on defect test and fault models. On the other hand, AMS-RF BIST techniques are still lagging behind. From a purely theoretical perspective they should be a simple extension of their digital counterparts. In that sense, a general on-chip scheme for testing a complex mixed-signal system would be as the one shown in Figure 1.2. Providing AMS-RF BIST functions would just require to move generators and digitizers into the system under test. However, this is in practice almost unfeasible due to the strict requirements imposed by the analog circuitry. Since AMS-RF circuits are usually tested by measuring

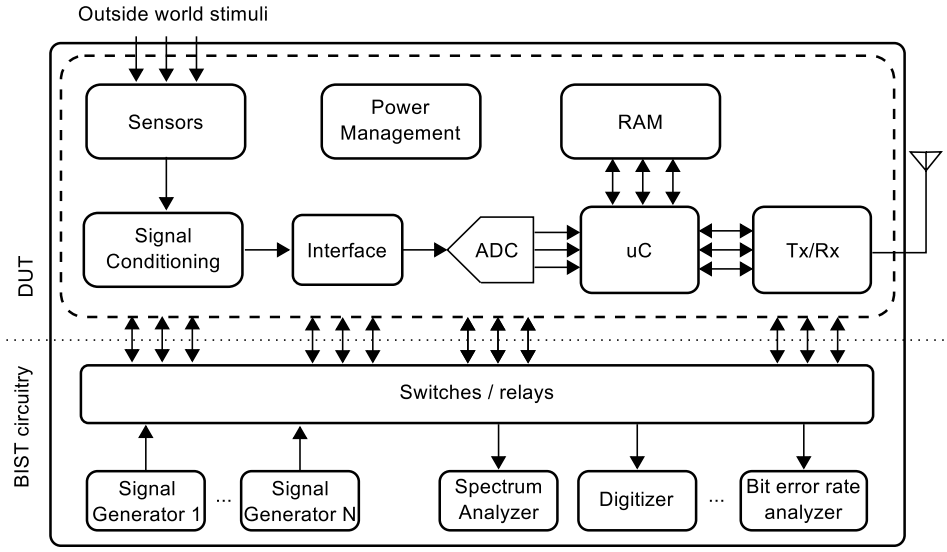


Figure 1.2 – General SoC/SiP block diagram with added BIST functionality.

their functional specifications, this means that each measurement has to comply with strict accuracy constraints to match the performance of the circuits under test. Moreover, due to the heterogeneity of the analog, mixed-signal and RF blocks, it would be necessary to combine signal generators ranging from the baseband frequency up to the radio frequency, with a linearity similar or higher than the tested circuits.

A promising solution to these pressing issues is the combination of BIST strategies and machine learning based tests. Machine learning test strategies replace costly analog, mixed-signal and RF performance measurements by a set of simpler measurements that can be performed on-chip by low-cost built-in test circuitry. The core idea is to build a mapping model from a set of simple measurements, usually called signatures, to the set of functional specifications.

The usual approach to machine learning indirect test is based on supervised machine learning algorithms. The process is developed in two stages, as conceptually depicted in Fig. 1.3: a learning stage, and a testing stage. During the learning stage both performance parameters and signatures are measured from a set of training devices. A machine learning algorithm is then trained over the two sets of measurements to build a mapping model. In the testing stage, signatures are measured for each DUT, and performances are inferred by using the mapping model obtained in the previous stage. Test result interpretation is the same as in conventional functional test. This is an elegant way to deal with the issue of valid ranges of acceptance, and also gives a valuable insight into reliability since we can estimate how far the circuit is from its nominal specification. In addition, machine learning algorithms are designed to handle complex multi-dimensional and non-linear relations like those between defects and specifications, and by extension, between signatures and specifications.

The benefits of this machine learning indirect test methodology are threefold. First, the outcome of the test can be interpreted in a conventional manner: the estimated specifications are directly compared to their test acceptance windows. Second, the simple measurements are devised to be cheaper than

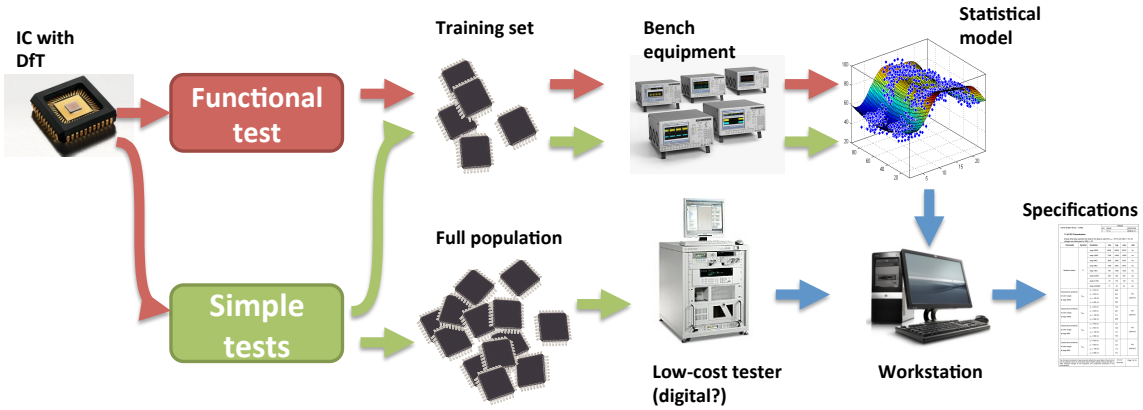


Figure 1.3 – Indirect test based on supervised machine learning models.

their functional counterparts. And third, these simple measurements can also be tailored to yield a higher defect coverage than traditional specifications.

However, the machine learning based test strategy is not free of shortcomings either. A key issue is finding an appropriate set of signatures to extract meaningful prediction models. The proposal of a set of signatures is usually *ad hoc*, based on a precise knowledge of the DUT, and sub-optimum: they may contain redundant information, non-relevant data, noisy signatures, etc. Another issue that has gathered attention in the past few years is the *a priori* validation of machine learning test. That is, the assessment of its quality, usually in terms of some standard test metrics, before deploying the technique in the production line. Another fundamental issue that has to be addressed derives from its model-oriented philosophy: any non-model errors can lead to unexpected bad results.

1.2 Research activities and document outline

My research has been focused on overcoming the limitations of current BIST and machine learning based test for complex AMS-RF circuits, with the final goal of providing innovative state-of-the-art test solutions for these complex systems. My research activities can be structured into two main interrelated research lines, namely,

a. Development of new techniques for incorporating Built-In Self-Test (BIST) into high-performance AMS-RF circuits.

b. Development of systematic methodologies for the design of accurate and reliable machine learning-based test programs for AMS-RF circuits.

Both research lines are currently being developed within the Reliable Mixed-Signal Systems Group at TIMA Laboratory (UMR5159), Grenoble, France, continuing previous work carried out at the Instituto de Microelectrónica de Sevilla, Sevilla, Spain (IMSE, CSIC-Universidad de Sevilla mixed

research unit). Thus, research line (a) has been supported by the JAE-DOC Spanish program (competitive post-doctoral contract program) and the ACATEX and DANTE Spanish research projects during my stay at IMSE, and by joint collaboration projects with STMicroelectronics, namely the ENIAC ELESIS European project, the PENTA HADES project and the NANO2017 program during my stay at TIMA. Research line (b) is being developed as a TIMA-IMSE international collaboration and supported by a LabEx PERSYVAL-Lab Exploratory Project and a CNRS PICS project. Further details are provided in the next chapters.

This document summarizes the main scientific developments and results obtained in my career as a researcher since the defense of my PhD. The rest of this document is structured in two main sections that mirrors the main research lines presented above. The first section, focused on mixed-signal BIST applications, comprises chapters 2 to 5, where I detail my research on the development of novel solutions for the static and dynamic characterization of ADC converters. The second section, focused on machine learning applications, comprises chapters 6 and 7, where I detail my research on feature selection and feature design automation for machine learning indirect test applications. Finally, my future research perspectives are summarized in chapter 8.

Chapter 2

Step-wise ramp generation for ADC static linearity BIST

2.1 Introduction

Static linearity test of Analog-to-Digital Converters (ADCs) is one of the most challenging and time consuming tasks in the production test of a mixed-signal system. Standard approaches to characterize static linearity consist in applying a high-linearity stimulus to the ADC under test, retrieving and storing a high volume of ADC output samples, and processing these samples to estimate the Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) metrics [3]. Given that analog-to-digital conversion is one of the basic functions in a mixed-signal system, moving static ADC testing on chip in a full BIST framework can enable a huge reduction in the production cost of these complex systems. In this line, one of the key challenges for adapting standard ADC static tests to a full-BIST scheme is to provide an appropriate test stimulus to excite the converter. As it is usually accepted by the industry, standard test techniques for static linearity characterization require a test stimulus whose linearity is 2 to 3 bits above the linearity of the ADC under test. Given that ADC resolutions are steadily increasing, this has become a major issue for the development of on-chip static linearity test solutions.

Providing an appropriate test stimulus generator for on-chip static test applications has been an open research problem for over a decade. Mainly, two basic architectures of on-chip ramp signal generators have been explored in the literature: ramp generators based on analog integrators and ramp generators based on Digital-to-Analog Converters (DACs). In essence, integrator-based ramp generators rely on a controlled current source that charges a capacitor in order to generate a ramp voltage signal [4–10]. On the other hand, static stimulus generators based on a modified DAC design have been proposed in [11–13]. These works take advantage of a Deterministic Dynamic Element Matching (DDEM) technique for relaxing the linearity requirements of the DAC for static test applications of ADCs. Digital $\Sigma\Delta$ encoding has been also proposed for generating triangular waves [14, 15]. These works employ a digital $\Sigma\Delta$ bitstream encoding a high resolution triangular wave followed by a 1-bit DAC and a lowpass filter to remove the shaped quantization noise.

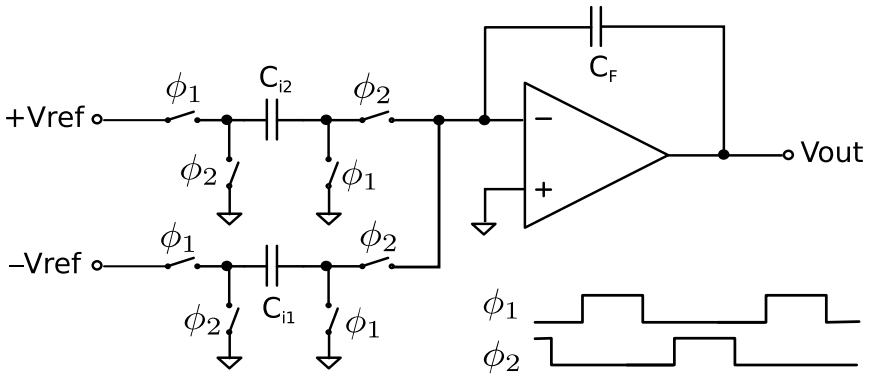


Figure 2.1 – a) Conceptual schematic of the proposed ramp signal generator; b) Diagram of the generator non-overlapping clock phases.

Recent works on static linearity test of ADCs focus on relaxing the stringent requirements of standard static test. Thus, the work in [16–18] present a Design-for-Test (DfT) strategy aimed at relaxing the linearity of the test stimulus, while the work in [19–25] is targeted at reducing the number of necessary measurements for a complete static characterization, hence reducing static test time. Extending these DfT methodologies to a full-BIST scheme still requires the integration of a static test stimulus generator on-chip.

Our main goals in this research are the design and experimental validation of a novel on-chip ramp stimulus generator suitable for on-chip static linearity test applications of ADCs. The proposed generator is based on a simple Switched-Capacitor (SC) integrator whose input stage has been conveniently modified to produce a very small integration gain proportional to the difference of two capacitances. Thus, as response to a DC input reference, the integrator outputs a controlled step-wise ramp signal with a small step size.

The work described in this chapter has been performed in the framework of the PhD thesis of Dr. Guillaume Renaud, that I co-supervised together with Dr. Salvador Mir at TIMA within the ELESIS project (ENIAC joint undertaking European program) in partnership with STMicroelectronics. This PhD thesis was successfully defended on November 29th 2016 and the obtained results have been published in international journal and conference papers [26–30]. Moreover, this work was extended with an international collaboration with the Instituto de Microelectrónica de Sevilla for adding self-testability to the proposed on-chip ramp stimulus generator. In this collaboration we developed a double-histogram test strategy that can separate the contributions of generator and ADC under test to the observed non-linearity at the output of the ADC under test. The resulting self-testable on-chip generator has also the added feature of being insensitive to kickback noise from the ADC, that is a key limiting problem for the static test of high-frequency converters [31, 32].

2.2 Theoretical basis

2.2.1 Proposed signal generation technique

Conceptually, the proposed ramp stimulus generation technique is based on the operation of a two-input SC integrator. Figure 2.1 shows a simplified schematic of the proposed ramp generator to illustrate the generation strategy (a single-ended schematic is shown for simplicity). As it is shown in Fig. 2.1, the core of the proposed generator is a SC integrator that operates with two non-overlapping clock phases ϕ_1 and ϕ_2. Assuming that the integrator is excited by DC voltages V_{ref} and $-V_{ref}$, the output voltage of the integrator, neglecting second-order effects, is given by

$$V_{out}(n) = V_{out}(n-1) + \frac{C_{i2} - C_{i1}}{C_F} V_{ref}, \tag{2.1}$$

at the end of the integration phase, that is, at time $t = nT_{clk}$, where T_{clk} is the integrator clock period, C_F is the feedback capacitor, and C_{i1} and C_{i2} are the input capacitors. As it can be derived from (2.1), the integrator output voltage evolves, ideally, as a step-wise ramp signal with a constant step that depends on the capacitance difference between the two input capacitors. Assuming that $C_F \gg C_{i2} - C_{i1}$, this step can be made small, in such a way that in a given ADC static test scenario it could be made significantly smaller than the Least Significant Bit (LSB) of the ADC under test. In other words, the proposed technique offers a feasible and simple strategy for providing a high-resolution discrete-time ramp stimulus that can be suitable for ADC static test. However, it has to be taken into account that practical limitations of the proposed step-wise generation strategy may impact the accuracy of the test. Indeed, non-idealities in the practical implementation of the ramp generator may impact the resolution and linearity of the generated ramp, degrading the accuracy of the measurements.

2.2.2 Performance limits of the proposed signal generation technique

The proposed step-wise ramp generation strategy is based on introducing a small difference between two capacitors in order to achieve a small step size. However, this technique, despite being simple, is prone to variations of the step size due to random mismatch in the capacitors and, moreover, non-idealities such as integrator leakage, amplifier offset, settling errors, noise, etc., may have also an impact in the quality of the generated ramp stimulus in terms of resolution and linearity.

Throughout this chapter, we will refer to the *resolution* of the generated step-wise ramp signal to denote the number of step levels defined by the ramp signal in a given Full-Scale voltage range. Thus, in this document we define the resolution, N, of the generated step-wise ramp, measured in bits, as

$$N = \log_2 n_{steps} \tag{2.2}$$

where n_{steps} is the number of step levels in the step-wise ramp in the complete Full Scale (FS) range. Under ideal operation conditions, n_{steps} can be expressed as

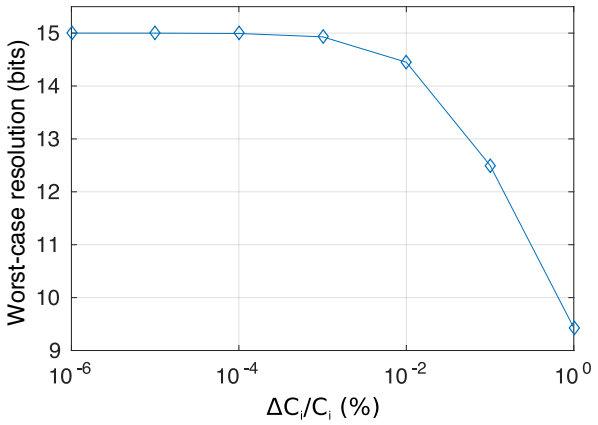


Figure 2.2 – Worst-case resolution of the generated step-wise ramp stimulus as a function of the input capacitor mismatch, for a ramp signal generator with an ideal resolution of 15 bit.

$$n_{steps} = \frac{FS}{\frac{C_{i2}-C_{i1}}{C_F} V_{ref}}. \tag{2.3}$$

On the other hand, the *linearity* of the generated step-wise ramp will be evaluated in terms of its Integral Non-Linearity, INL_{ramp}, defined as the maximum absolute deviation from the best linear fit of the generated ramp (in a least squares sense) and expressed as an equivalent number of bits, $ENOB_{static}$, as defined in [6],

$$ENOB_{static} = \log_2 \frac{FS}{INL_{ramp}}. \tag{2.4}$$

Capacitor mismatch

Capacitor mismatch is undoubtedly one of the key limiting factors for the resolution of the proposed ramp generator. As it is easily derived from equation (2.1), random variations of the capacitance value of capacitors C_{i1}, C_{i2} and C_F have a direct impact on the size of the step in the step-wise ramp. The output voltage of the integrator in Fig. 2.1 at time $t = nT_{clk}$ including the effect of mismatch can be modeled as

$$V_{out}(n) \cong V_{out}(n-1) + \left(\frac{C_{i2} - C_{i1}}{C_F} + \frac{\sqrt{2}\Delta C_i}{C_F} \right) V_{ref} \tag{2.5}$$

where ΔC_i is the random variation of capacitance due to mismatch of the input capacitors. It is assumed that $\Delta C_{i1} \cong \Delta C_{i2}$, $C_{i1} \cong C_{i2}$, and $C_F \gg C_{i2} - C_{i1}$. As it is clear from equation (2.5), the linearity of the ramp is not affected by capacitor mismatch: the size of the step deviates from the nominal, but it remains constant throughout the complete *FS* of the ramp.

It is important to notice that $|\Delta C_i / C_F|$ should be minimized in order to ensure that the nominal step size of the ramp is larger than the contribution of the mismatch in (2.5). That is, for a practical ramp generator it has to be verified that

$$\frac{C_{i2}-C_{i1}}{C_F} \gg \sqrt{2}\left|\frac{\Delta C_i}{C_F}\right|. \tag{2.6}$$

Fulfilling the condition in (2.6) represents a feasibility limit for the practical implementation of the proposed ramp generator in a given technology. Under this feasibility condition, Fig. 2.2 shows the evolution of the worst-case resolution for the generated ramp stimulus as a function of the maximum relative mismatch, $\Delta C_i/C_i$, affecting the input capacitors, for a ramp generator with a 15-bit ideal resolution. These results were obtained by simulating a Matlab behavioral model of the generator in Fig. 2.1 under capacitor mismatch conditions, based on the analytical behavior in equation (2.5). As it is clearly shown in Fig. 2.2, an increase in the relative mismatch level results in a significant degradation of the resolution of the generated ramp.

Integrator leakage

Integrator leakage is a direct consequence of the finite gain of the operational amplifier in the SC integrator. As a result, instead of the ideal behavior in (2.1), only a fraction α of the previous integrator output sample is added in each integration cycle. The output voltage of the integrator in Fig. 2.1 including the effect of leakage at time $t = nT_{clk}$ is given by

$$V_{out}(n) = \alpha V_{out}(n-1) + gV_{ref} \tag{2.7}$$

where α and g are given by

$$g \cong \frac{C_{i2}-C_{i1}}{C_F}\left(1-\frac{1+\frac{C_{i2}-C_{i1}}{C_F}}{A_0}\right), \tag{2.8}$$

$$\alpha \cong 1-\frac{C_{i2}-C_{i1}}{C_F A_0}, \tag{2.9}$$

where A_0 is the finite open-loop gain of the amplifier in the integrator. It is clear that the cumulative effect of the integrator leakage has a direct impact in the linearity of the generated ramp stimulus. Thus, Figure 2.3 shows the evolution of the static ENOB of the generated ramp stimulus as a function of the amplifier gain, for a ramp generator with a 15-bit ideal resolution. These results were obtained by simulating in Matlab a behavioral model of the generator in Fig. 2.1 under finite gain conditions, based on the analytical behavior in equations (2.7)-(2.9). As it can be seen, reducing the gain of the amplifier in the integrator yields a significant degradation of the linearity of the generated ramp.

Amplifier input offset

In the proposed generator architecture depicted in Fig. 2.1, an uncompensated offset V_{off} at the input of the amplifier would be integrated together with the reference voltage, in such a way that the output of the integrator at time $t = nT_{clk}$ would be given by

$$V_{out}(n) = V_{out}(n-1) + \frac{C_{i2}-C_{i1}}{C_F}V_{ref} + \left(1+\frac{C_{i2}+C_{i1}}{C_F}\right)V_{off} \tag{2.10}$$

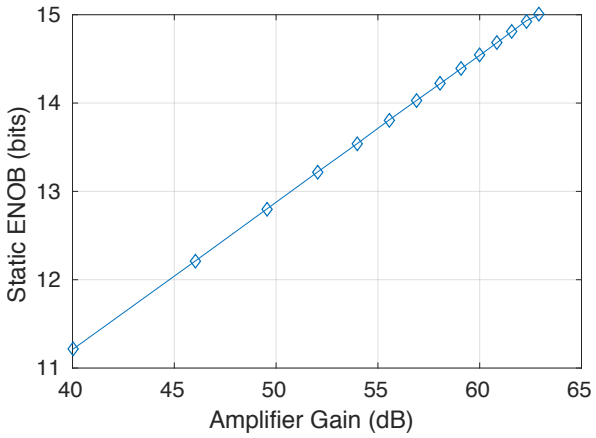


Figure 2.3 – Static Effective Number of Bits of the generated step-wise ramp stimulus as a function of the amplifier gain in the integrator, for a ramp signal generator with an ideal resolution of 15 bit.

The integration of the offset can significantly affect the step size of the generated ramp signal. Similarly to the effect of capacitor mismatch, the offset of the amplifier affects the resolution of the generated ramp, but not its linearity. Nevertheless, taking into account that C_{i1} and C_{i2} would be approximately equal to assure a small step size under nominal conditions, an uncompensated input offset may even become the dominant contribution to the evolution of the output. In order to avoid this issue, for a practical implementation of the proposed generator it has to be verified that,

$$\frac{C_{i2} - C_{i1}}{C_F} V_{ref} \gg \left(1 + \frac{C_{i2} + C_{i1}}{C_F}\right) |V_{off}| \,. \tag{2.11}$$

Figure 2.4 shows the results of a Matlab behavioral simulation of the proposed generator taking into account the effect of a positive input offset, for a generator with a 15-bit ideal resolution and assuming $\frac{C_{i1}}{C_F} \cong \frac{C_{i2}}{C_F} = 0.1$. As it can be seen, a positive input offset can degrade significantly the resolution of the generated ramp stimulus.

An uncompensated negative offset can be even more harmful if the feasibility condition in (2.11) does not hold. In that case, the contribution of a negative offset in (2.10) could cancel the ideal integration step produced by the capacitance difference between the input capacitors, hence destroying the functionality of the generator.

Settling error

Ideally, the discrete-time integrator in Fig. 2.1 performs the cumulative sum in equation (2.1) that defines the desired ramp stimulus. However, a non-ideal dynamic behavior of the integrator may introduce a settling error in the evolution of the output, hence deviating from this ideal behavior. Neglecting second-order dynamic effects due to the parasitic resistances and capacitors associated to the switched-capacitor network, the dynamic behavior of an integrator with non-ideal settling can

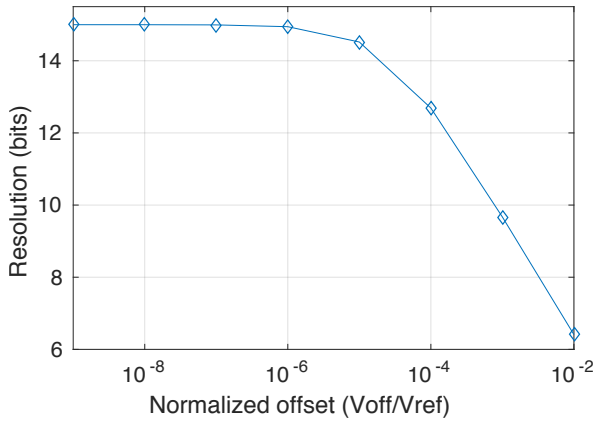


Figure 2.4 – Resolution of the generated step-wise ramp stimulus as a function of the amplifier input offset, for a ramp signal generator with an ideal resolution of 15 bit.

be easily modeled using a one-pole approximation for the dynamics of the amplifier, together with a maximum current limitation. In such a model, the settling of the integrator output is defined by two parameters: the Gain-Bandwidth product, *GBW*, and the Slew-Rate, *SR*, of the amplifier. For the sake of readability, in the following analysis we will consider a time and frequency normalization to a sampling frequency of one, that is,

$$\begin{aligned} T_{clk} &= 1, \\ SR &= SR^* \times f_{clk} \\ GBW &= GBW^* \times f_{clk} \end{aligned} \tag{2.12}$$

where *SR* and *GBW* are the conventional slew-rate and gain-bandwidth product, and $f_{clk} = 1/T_{clk}$ is the sampling frequency. Parameters SR^* and GBW^* are time-normalized versions of the slew-rate and gain-bandwidth product, respectively. Different regions of operation can be considered, depending on parameter t_0 defined as,

$$t_0 = \frac{bV_{ref}}{SR^*} - \frac{1}{2\pi GBW^*}, \tag{2.13}$$

where $b = \frac{C_{i2}-C_{i1}}{C_F}$ is the integrator gain. Phenomenologically, t_0 indicates the time at which the amplifier stops slewing. If $t_0 \geqslant 0$, the amplifier output slews during its dynamic evolution, introducing this way a non-linear contribution to the generated ramp signal. On the other hand, if $t_0 < 0$, the amplifier does not slew, the settling is then determined only by the GBW and is exponentially shaped. At the end of the integration phase, the output voltage can be expressed as,

$$V_{out}(n) = V_{out}(n-1) + bV_{ref}(1 - e^{-\pi GBW^*}). \tag{2.14}$$

It is easily seen that in this operation region the ideal integration gain, b, is decreased by a constant factor that depends on the *GBW* and the sampling frequency.

In order to guarantee the linearity of the proposed ramp stimulus generator, the operation of the integrator has to be kept in the $t_0 < 0$ region to avoid non-linear settling errors. Additionally, the

contribution of the linear settling error in (2.14) has to be minimized. In a practical implementation and for a given clock frequency for the integrator, these design conditions can be assured by making $t_0 \ll 0$, that is,

$$\frac{bV_{ref}}{SR^*} \ll \frac{1}{2\pi GBW^*}. \tag{2.15}$$

Noise

Assuming a clean input voltage reference, the main noise contributions in the integrator in Fig. 2.1 are the thermal noise due to the switches and the noise due to the amplifier. These noise sources are sampled by the input capacitors C_{i1} and C_{i2} during phases ϕ_1 and ϕ_2 together with the reference voltage V_{ref}. The output voltage of the integrator in Fig. 2.1 at time $t = nT_{clk}$ including noise contributions is given by

$$\begin{aligned} V_{out}(n) &= V_{out}(n-1) + \frac{C_{i2}}{C_F}\left[V_{ref} + N_{2\phi_1}(n-1) - N_{2\phi_2}(n)\right] \\ &\quad + \frac{C_{i1}}{C_F}\left[-V_{ref} + N_{1\phi_1}(n-1) - N_{1\phi_2}(n)\right], \end{aligned} \tag{2.16}$$

where $N_{2\phi_1}$, $N_{2\phi_2}$, $N_{1\phi_1}$ and $N_{1\phi_2}$ represent the noise voltages sampled by capacitors C_{i2} and C_{i1} during clock phases ϕ_1 and ϕ_2, respectively. Notice that noise voltages associated to phase ϕ_1 are due to thermal noise from switches in *on* state, while noise voltages associated to phase ϕ_2 have contributions from the thermal noise of *on* switches and from the amplifier noise. The interested reader is referred to [33, 34] for a detailed analysis of noise contributions in a multi-input switched-capacitor integrator. Regarding the proposed ramp generation strategy, equation (2.16) imposes a lower limit on the magnitude of the reference voltage V_{ref}. In order to avoid a degradation of the generated ramp due to noise, the reference voltage has to be significantly larger than the sampled noise in the input capacitors. In a practical ADC BIST implementation, this condition can be easily ensured by co-designing the reference voltage of the ADC under test to drive both the ADC and the ramp stimulus generator.

2.3 Practical implementation

In order to demonstrate the feasibility of the proposed ramp stimulus generator, a proof-of-concept prototype was implemented in STMicroelectronics 2.5V 65nm CMOS technology. Figure 2.5 shows a block diagram of the proposed fully-differential implementation. The generator in Fig. 2.5 is a fully differential version of the basic generator in Fig. 2.1. The choice of a fully-differential architecture minimizes the effect of parasitics in the SC network, as they naturally tend to compensate between the positive and negative signal paths, and greatly reduces other second-order effects in SC circuits, such as charge injection and clock feedthrough in the switches.

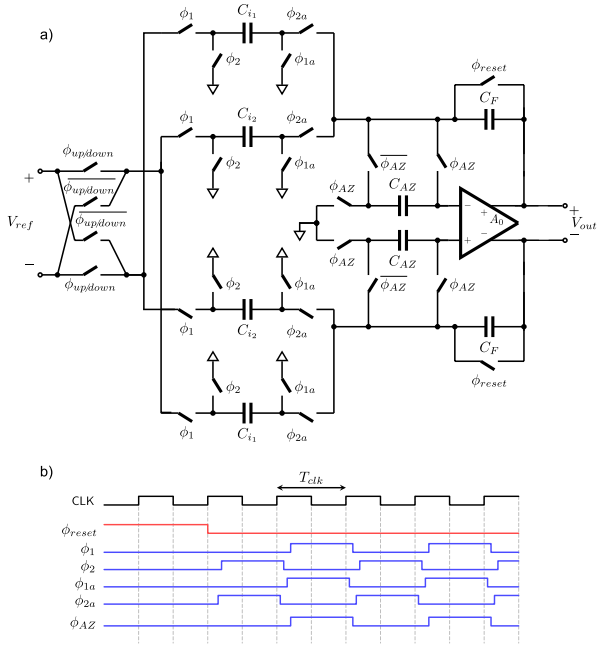


Figure 2.5 – a) Block diagram of the proposed differential step-wise ramp signal generator; b) Timing diagram for the clock phases.

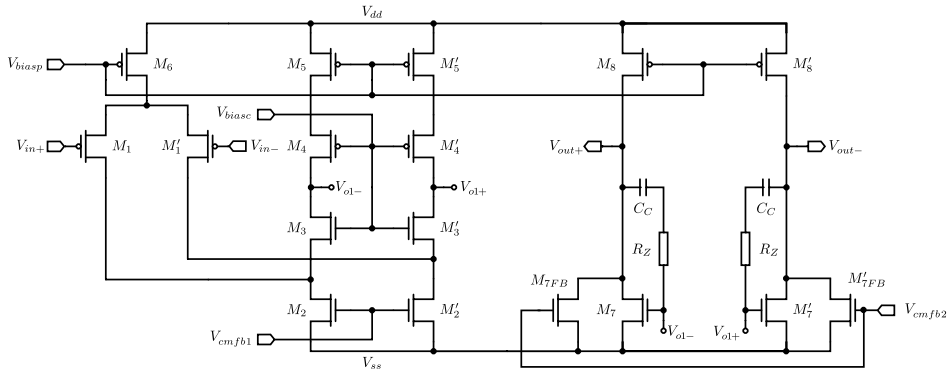


Figure 2.6 – Transistor-level schematic of the operational amplifier.

Differential output range	± 2 V
Nominal clock frequency, $1/T_{clk}$	up to 200 kHz
Reference voltage, V_{ref}	1 V
Ramp step size	~ 100 μV
Resolution, N	~ 15 bit
Linearity, ENOB$_{static}$	$\gtrsim 14$ bit

Table 2.1 – Summary of design goals for the step-wise ramp generation prototype

The proposed architecture includes a classical auto-zero to reduce the influence of the amplifier offset on the generated ramp step size [35]. A switching scheme controlled by digital signal $\phi_{up/down}$ has been added at the input in order to control the slope (positive or negative) of the generated ramp, and the feedback capacitor can be reset by activating control signal ϕ_{reset} in order to initialize the output ramp. Additionally, as it can be seen in the timing diagram, clock phases ϕ_{1a} and ϕ_{2a} are advanced versions of clock phases ϕ_1 and ϕ_2 that have been added to reduce charge injection during the operation of the sampling switches. The design goal for this ramp generator is to generate a quasi-static step-wise ramp with a step size around 100 μV in a differential Full-Scale range of ± 2 V, which, under ideal conditions, represents a nominal resolution around $N = 15.3$ bits. We target a linearity around ENOB$_{static} = 14$ bits, which in a practical test scenario would be enough for the static test of 11 bit ADCs. Table 2.1 summarizes the design goals of the ramp stimulus generator prototype.

To achieve the design goals in Table 2.1, we take advantage of the analytical results in the previous section to evaluate the required performance for each of the blocks composing the step-wise ramp generator in Fig. 2.5. The analysis in section 2.2 imposes practical limits for the implementation of the proposed step-wise ramp generator concerning technological and design parameters, i.e., the relative mismatch level affecting the input capacitors, the input offset in the integrator, the open-loop gain of the amplifier in the integrator, and the dynamic performance of the amplifier. Table 2.2 summarizes the main design parameters for the building blocks of the step-wise ramp generator to achieve the desired performance, according to the analytical results in (2.5)-(2.15). Since the problem has multiple degrees of freedom within the constrains of the feasibility conditions in (2.6), (2.11), and (2.15), conservative goals have been set to make the contributions of amplifier non-idealities negligible, while the requirements on mismatch have been relaxed to reduce the area of the capacitors. As it will be shown in the following sections, this choice makes capacitor mismatch the main limiting factor for the resolution of the described implementation of the step-wise ramp generator.

The following subsections detail the implementation of the different blocks composing the ramp stimulus generator, that is, the operational amplifier, the capacitors, and the switches.

2.3.1 Operational amplifier

Figure 2.6 shows a transistor level schematic of the designed amplifier. The selected design is a standard fully-differential two-stage folded-cascode topology with a Miller compensation using a nulling resistor (the bias voltage circuitry and common-mode feedback networks are not shown for simplicity). The selected topology offers a good trade-off between the amplifier performance (in

Amplifier	Open loop gain, A_0	> 80 dB
	Gain-bandwidth product, GBW	$\gtrsim 90$ MHz
	Slew-Rate, SR	~ 100 V/μs
	Output range	$\geqslant \pm 2$ V
	Equivalent input noise	minimize
Auto-Zero	Residual input offset	< 1 μV
Input capacitors	Mismatch, ΔC_i	$\lesssim 0.1$ fF
Switches	Charge injection	minimize

Table 2.2 – Summary of required design parameters for the building blocks of the step-wise ramp generation prototype

MOSFETs	**W/L** (μm/μm)	**Capacitors**	**Value**
M1-M1′	100/0.3	C_C	2.94 pF
M2-M2′	32/0.8	C_{ch}	495 fF
M3-M3′	30/0.48	C_h	495 fF
M4-M4′	310/1		
M5-M5′	310/1	**Resistors**	**Value**
M6	5/2	R_Z	601 Ω
M7-M7′	12/0.3		
M8-M8′	475/0.3		
M7FB-M7FB′	0.5/0.3		

Table 2.3 – Sizing of amplifier components

terms of static gain and dynamic behavior) and simplicity of design.

Two dynamic common-mode feedback networks were designed following the guidelines in [36] to independently compensate output common mode deviations of both the first and second stages of the amplifier. Common-mode compensation signal V_{cmfb1} controls the biasing of transistors M_2 and M_2', while the compensation of the second stage is applied in current mode, through auxiliary transistors M_{7FB} and M_{7FB}'.

Transistors were sized using the g_m/I_D methodology [37] with the design goals in Table 2.2 in the selected 2.5V 65nm CMOS technology. Transistors M_2, M_2', M_7 and M_7' were biased in strong inversion to minimize the amplifier noise, while the rest of transistors were biased in moderate inversion as it offers the best area-to-performance trade-off solution for the desired design goals. Table 2.3 lists the dimensions of the transistors, capacitors, and nulling resistors, while Table IV shows the main performance figures of the designed amplifier obtained by electrical post-layout simulation. All the obtained performance parameters comply with the design goals for the step-wise ramp generator listed in Table 2.2.

Open loop gain, A_0	93 dB
Phase Margin, PM	75°
Gain-bandwidth product, GBW	95 MHz
Slew-Rate, SR	150 V/μs
Output range	$\pm$2.3 V
Equivalent input noise	89 μV_{rms}

Table 2.4 – Performance parameters of the amplifier obtained by electrical simulation

2.3.2 Amplifier offset autozeroing

Electrical Monte Carlo simulations of the amplifier described in the previous subsection were performed using the Monte Carlo process and mismatch models provided in the Process Design Kit of the selected 65 nm CMOS technology. These simulations show an equivalent input offset that varies with a standard deviation $\sigma_{Voff} \simeq 1$ mV. According to the analysis in section 2.2, this input offset would not comply with the feasibility condition in equation (2.11). That is, in this scenario, the size of the step in the generated step-wise ramp would be dominated by the contribution of this random offset, and not by the difference of the input capacitors as intended by design.

In order to compensate this offset, we have implemented a classical closed-loop autozeroing technique adapted from [35], as it is shown in Fig. 2.5. Capacitor C_{AZ} is used to store the amplifier offset during the sampling phase of the integrator and to subtract this offset in the integration phase. The equivalent input-referred residual offset $V_{res,off}$ can be roughly approximated by

$$V_{res,off} \sim \frac{V_{off}}{A_0} + \frac{\Delta q_{inj}}{C_{AZ}} \tag{2.17}$$

where V_{off} is the uncompensated input-referred offset of the amplifier, and Δq_{inj} is the difference of charge injection between the positive and negative paths in capacitors C_{AZ} due to mismatch. Capacitors C_{AZ} were designed as $\sim$ 1 pF MOM capacitors in the selected CMOS technology. Using this simple configuration, the residual offset is below 100 nV. Both our theoretical analysis in section 2.2 and extensive electrical simulations show that this residual offset does not have a significant effect on the resolution of the step-wise ramp generator prototype.

2.3.3 Capacitors

The sizing of the sampling and feedback capacitors, C_{i1}, C_{i2}, and C_F, respectively, is a key point in the design of the generator given that it defines the nominal size of the step in the generated step-wise ramp signal. According to the design goals in Table 2.1, achieving the target resolution in the desired output swing requires to set the step of the ramp to $\sim$ 100 μV. In order to realize this design goal for the step-wise ramp generator prototype, we propose to make

$$\frac{C_{i2} - C_{i1}}{C_F} V_{ref} = 100\,\mu\text{V}. \tag{2.18}$$

This capacitance ratio is feasible in the selected 65 nm CMOS technology by making $C_F = 10$ pF and $C_{i2} - C_{i1} = 1$ fF. Then, according to the choice of design parameters in Table 2.2, we can size the input capacitors C_{i1} and C_{i2} to comply with the mismatch requirement $\Delta C_i \lesssim 0.1$ fF. According to the mismatch model provided in the Process Design Kit of the selected technology, if we implement the input capacitors as ~ 1 pF MOM capacitors (i.e., $C_{i1} \sim 1$ pF and $C_{i2} = C_{i1} + 1$ fF), with a geometry of about 100 by 100 metal 2 to metal 5 fingers, the capacitance value of the input capacitors will vary with a standard deviation $\sigma_C = 0.04$ fF, which, considering a $\pm 3\sigma$ variation, would limit the resolution of the step-wise ramp generator in the range from $N = 14.8$ bits to $N = 15.7$ bits. This is an acceptable trade-off between the area of the capacitors and the expected variation of the generator resolution for our design goals. Additionally, this implementation allows for an easy realization of the desired capacitance difference between C_{i1} and C_{i2} simply by adjusting properly the number of fingers. Electrical simulations also show that other second-order effects in the selected MOM capacitors, such as capacitance non-linearity, do not have a significant contribution to the linearity and resolution of the generated step-wise ramp in the proposed implementation. Additionally, the effect of parasitic capacitances due to interconnections and switches in the SC network are minimized by a careful symmetrical layout of the proposed fully-differential architecture.

2.3.4 Switches

Switches in the integrator were designed as CMOS switches to reduce its equivalent *on* resistance along the complete signal range considered. Charge injection due to the switches turning *off* may degrade the performance of the proposed step-wise ramp generator strategy. Indeed, in a single-ended implementation such as the simplified generator in Fig. 2.1, the effect of charge injection in the sampling capacitors would appear as an uncompensated signal-dependent offset that would be integrated together with the desired ramp steps limiting the resolution and linearity of the ramp generator. In a fully differential implementation, such as the proposed step-wise ramp generator prototype, the effect of charge injection is greatly reduced since charge injection in the positive and negative paths tend to compensate. To further reduce the effect of charge injection in the input sampling switches, they are designed with two added dummy PMOS transistors. These dummy transistors are intended to acquire the charge stored in the channel of the PMOS transistor in the switch when it turns off when sampling the reference voltage. Additionally, two advanced phases ϕ_{1a} and ϕ_{2a} (see Fig. 2.5b) have been introduced to enable bottom plate sampling. The switch at the bottom plate of the capacitor opens before the top plate switch does. When the top plate switch opens, the bottom plate is floating and no charge is injected on the capacitor, further reducing charge injection issues.

An additional concern in the design of the switches is the eventual discharge of the capacitors through its equivalent *off* resistance. Given that the ramp signal generator is aimed at static test applications, this effect has to be carefully considered to ensure a correct charge transfer in the SC integrator at the desired clock frequency. Transistors in the CMOS switch were sized to ensure a correct operation for clock frequencies above 10 kHz.

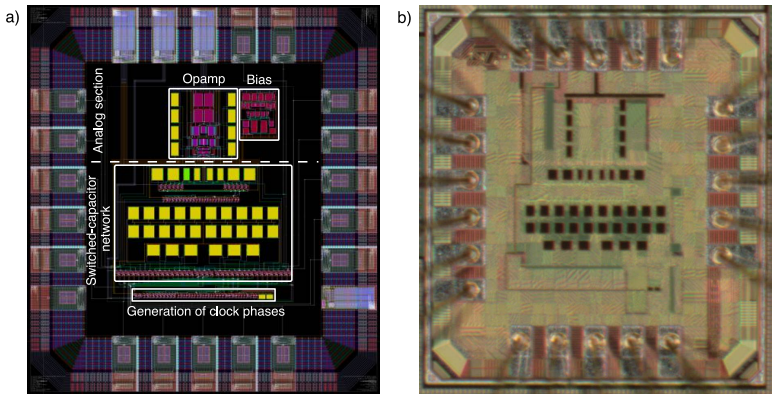


Figure 2.7 – a) Layout and floorplan of the step-wise ramp signal generator prototype; b) Microphotograph of one of the fabricated samples.

2.4 Experimental results

The described step-wise ramp generator prototype was fabricated in the selected STMicroelectronics 2.5 V 65 nm CMOS technology. Figure 2.7a shows the layout and floorplan of the ramp signal generator prototype. Positive and negative signal paths have been carefully drawn to respect the symmetry of the fully-differential architecture, while the analog section is separated from the switched-capacitor network and digital clock generation circuitry to minimize noise injection due to the switching activity. Figure 2.7b shows a microphotograph of one of the fabricated chip samples. It occupies an active area of 0.06 mm^2, including dedicated bias and clock phase generation circuitry. A total of 15 samples were fabricated, packaged and fully characterized in the laboratory in order to validate the feasibility and performance of the developed ramp signal generator prototype.

Our test setup is depicted in Fig. 2.8. It makes use of two National Instrument USB-6361 Data Acquisition Cards (DAQs) controlled by a conventional computer. Two sets of experiments are carried out to validate the functionality and performance of the fabricated ramp generator. The first set of experiments is aimed at characterizing the linearity performance of the fabricated ramp generator as a stand-alone circuit. The second set of experiments is aimed at validating the functionality of the fabricated ramp generator in a proof-of-concept static test scenario. In this proof-of-concept we characterize the linearity of an 11-bit ADC by using the proposed step-wise ramp generator.

2.4.1 Performance of the on-chip step-wise ramp generator

Our first set of experiments is focused on validating the performance of the proposed ramp signal generator as a stand-alone device, for the 15 fabricated samples. The instrumentation cards provide the master clock signal for the generator and capture the generated differential analog ramp at the output of the generator with a 16-bit quantizer. The captured signals are then processed in Matlab to

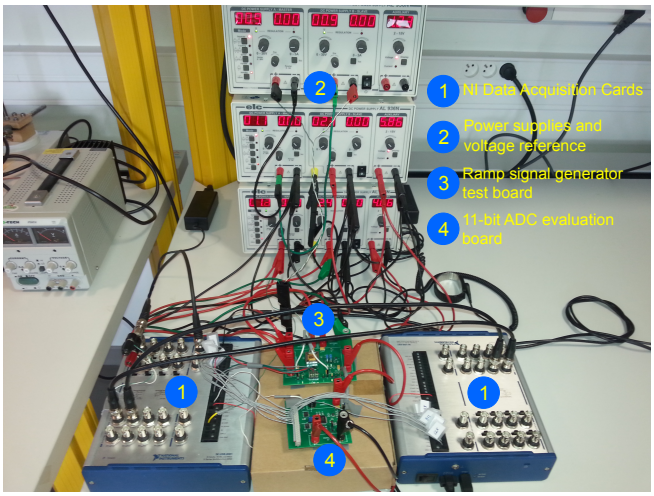


Figure 2.8 – Photograph of the test setup for the step-wise ramp signal generator prototype.

evaluate the resolution and linearity of the generated step-wise ramp signals.

Figures 2.9 and 2.10 show the histograms of the measured resolution and static ENOB, respectively, for the 15 fabricated ramp signal generator samples. These performance metrics were evaluated considering a ± 2 V differential output range for the generated ramp signal, while the generator operates at a clock frequency $f_{clk} = 200$ kHz and with a reference input voltage $V_{ref} = 1$ V. As it can be observed in Fig. 2.9, the histogram of the measured resolution of the generated ramp signal across the 15 fabricated samples is contained in the range of $N = 14.5$ bits to $N = 15.5$ bits, which matches very well with the predicted resolution range –that is, $N = 14.8$ bits to $N = 15.7$ bits– due to capacitor mismatch limitations discussed in the previous section. The measured linearity of the generated ramp signal is contained in the range of $\text{ENOB}_{static} = 13.3$ bits to $\text{ENOB}_{static} = 15.1$ bits, as it can be observed in Fig. 2.10, with an average static ENOB of 14.5 bits, in agreement with our target design specifications. The measured non-linearity of the fabricated ramp generators can be explained by uncompensated second-order effects such as the non-linearity of the amplifier gain and the non-linear behavior of capacitors for large signal values.

Table 2.5 compares the measured performance of the proposed step-wise ramp signal generator with other state-of-the-art on-chip ramp generators published in the literature. As it can be observed, the proposed step-wise ramp generator compares very well to the state-of-the-art. The proposed ramp signal generator yields one of the highest linearity and output swing figures among the considered references.

2.4.2 ADC static linearity measurements using step-wise ramp stimuli

Our second set of experiments is focused on validating the functionality of the generator in a static test scenario. For that purpose, we employ the fabricated step-wise ramp generator to provide the test stimulus for characterizing the static linearity of an off-the-shelf 11-bit ADC. The selected ADC under

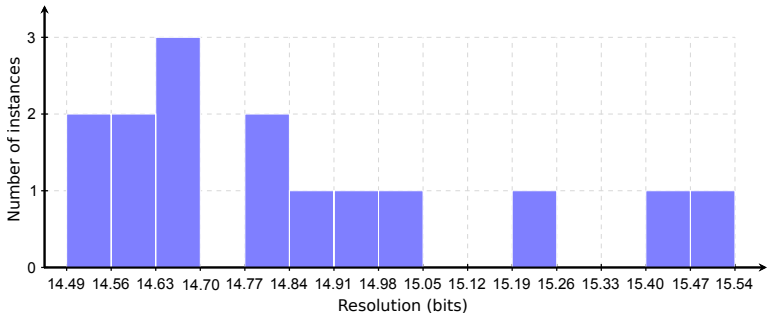


Figure 2.9 – Histogram of the measured resolution of the generated step-wise ramp signal for the 15 fabricated generator samples.

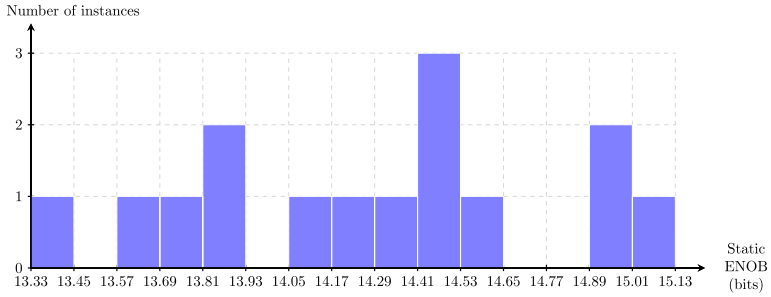


Figure 2.10 – Histogram of the measured static ENOB of the generated step-wise ramp signal for the 15 fabricated generator samples.

Reference	Generation technique	Linearity (bits)	Output swing (V)	Area (mm^2)	Technology
This work	Step-wise ramp generation	14.5	–2/2	0.06	65nm CMOS
[4]	Automatic slope adjustment ramp generation	8	–2/2	N/A	N/A
[5]	Current source integration	14*	0.1/0.9	0.11	2.0μm CMOS
[5]	Relaxation oscillator	12*	0.2/1.4	0.51	1.2μm CMOS
[6]	Adaptive triangle-wave generation	14*	–1/1	0.05	0.6μm CMOS
[9]	Error-cancellation Least-Mean-Square integrator	10	N/A	N/A	N/A
[9]	SC fully-differential Least-Mean-Square integrator	11	0.7/1.3	0.18	180nm CMOS
[15]	$\Sigma\Delta$ modulation-based generation	12*	0.4/1.4	0.02	250nm CMOS
[8]	Integration of voltage controlled current source	15*	0/1	0.9	0.5μm CMOS
[10]	Bootstrap integrator-based generator	> 8*	N/A	N/A	180nm CMOS
[38]	Segmented resistor-string DAC	9	0/1.8	0.91	180nm CMOS

* Electrical simulation results.

Table 2.5 – Comparison of the measured signal generator performance with previous work on on-chip ramp stimulus generation

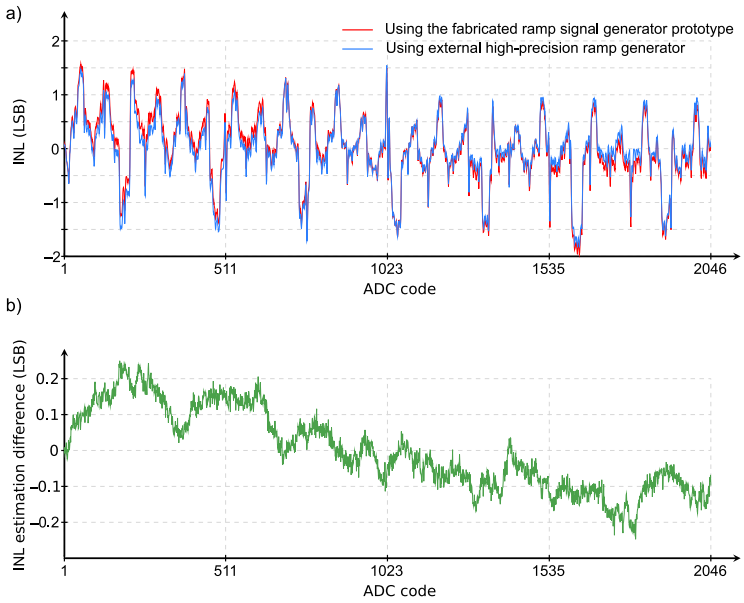


Figure 2.11 – a) INL measurements across the complete signal range of the ADC under test using the NI Data Acquisition Card to provide a high-resolution ramp stimulus, and using the fabricated ramp signal generator; b) INL estimation difference.

test is a 10 MSamples/s 11-bit ADC with a differential input range of ± 1 V. In this set of experiments, the generated ramp stimulus is fed to an evaluation board containing the ADC under test, while the output codes generated by the ADC are captured by a Data Acquisition Card. The ramp stimulus generator works in the same operating conditions as in the previous set of experiments. The captured output codes are then processed in Matlab using the classical histogram test algorithm to extract the INL of the ADC under test [3]. For validating the obtained results, the ADC is also characterized by using the arbitrary waveform generator in one Data Acquisition Card to excite the ADC with a slow 16-bit analog ramp as test stimulus. The INL is then extracted for each ADC output code using the histogram test algorithm and the obtained values are stored as a reference for comparison. It is important to remark that this is a proof-of-concept experiment devised to show the equivalence between the proposed on-chip ramp stimulus generator and dedicated external test equipment. In an actual on-chip test application, both the ramp stimulus generator and the ADC under test would be integrated in the same die.

Figure 2.11 shows the obtained INL per code across the complete output range of the ADC, obtained by exciting the ADC under test with one of the samples of the fabricated ramp signal generator. In this experiment, we selected one representative sample of the generator with $N = 14.5$ bits and $\text{ENOB}_{static} = 14.1$ bits. Results are compared to the measurements obtained by using the high-precision ramp generated by the instrumentation card. As it can be seen, differences in the estimation of INL are well contained in the ± 0.25 LSB band. It is interesting to notice that the magnitude of the observed INL estimation error agrees very well with the step-wise nature of the generated ramp

Reference	Brief description of key features	Nature of validation	ADC under test	Accuracy (INL measurement)
This work	On-chip step-wise ramp signal generator	Experimental	11 bit	± 0.3 LSB
[5]	On-chip signal generator based on current source integration	Simulation	10 bit	± 0.03 LSB (DNL)
[5]	On-chip signal generator based on relaxation oscillator	Simulation	10 bit	± 0.15 LSB (DNL)
[11]	On-chip signal generator based on low-resolution DAC with DDEM	Experimental	11 bit	± 0.5 LSB
[11]	On-chip signal generator based on low-resolution DAC with DDEM	Experimental	12 bit	± 1 LSB
[13]	ADC/DAC loopback test	Experimental	10 bit	± 0.4 LSB
[39]	DAC-ADC co-testing	Simulation	12 bit	± 0.5 LSB
[18]	Low resolution DAC with polynomial fitting algorithm	Experimental	12 bit	± 0.6 LSB
[16]	Stimulus error identification and removal	Experimental	16 bit	± 2 LSB
[25]	Error identification and segmented model identification	Simulation	16 bit	± 0.8 LSB
[17]	Double histogram strategy	Simulation	16 bit	± 1 LSB
[19]	Reduced code linearity testing of pipeline ADCs	Experimental	11 bit	± 0.2 LSB
[23]	Transition-code linearity test of pipeline ADCs	Experimental	12 bit	± 1.1 LSB
[22]	Code-density testing with non-linearity identification and removal	Experimental	16 bit	± 1 LSB

Table 2.6 – Comparison of the obtained measurement accuracy with previous work on static linearity testing

stimulus, which, for the selected ramp generator sample, has a step size of ~ 0.2 LSB.

In order to further show the equivalence between our ramp signal generator and the external high-precision test equipment, we measured the maximum INL, INL_{max}, of the ADC under test using the 15 fabricated ramp generator samples. Fig. 2.12 shows the histogram of the INL_{max} estimation error in the characterization of the ADC static linearity, for the 15 fabricated ramp generator samples. This INL_{max} estimation error is defined as the difference between the INL_{max} estimation obtained by using the fabricated ramp signal generator, and the INL_{max} measurement obtained by using the high-precision 16-bit ramp provided by the external equipment. As it can be observed, for the 15 fabricated samples, the measured INL_{max} estimation error is contained between 0.2 LSB and 0.6 LSB, with an average INL estimation error of 0.33 LSB, again in agreement with the expected error due to the discrete nature of the step-wise ramp stimulus.

To put the obtained results into perspective, Table 2.6 shows a comparison between different static linearity measurement techniques recently presented in the literature. For a fair comparison, it has to be noted that each of the measurement techniques in Table 2.6 is aimed at a different target application. Thus, the works in [5, 11, 13] are aimed at static linearity BIST applications of ADCs using embedded signal generators, while the measurement strategies in [16–19, 22, 23] rely on external equipment and dedicated post-processing to either relax the linearity requirement of the signal generator [16–18, 39], reduce the number of necessary measurements [19, 23], or both [22, 25]. The work presented in this document is aimed at BIST applications, and, as it is shown in Table 2.6, the obtained experimental results compare very well to the state-of-the-art.

2.5 Conclusions

This chapter presented some of our most relevant achievements in our research towards the design of an on-chip step-wise ramp generator architecture for static test of ADCs. The proposed ramp generator is based on a discrete-time SC integrator whose input stage has been modified to produce a very small integration gain. The main non-idealities affecting the performance of the ramp generator and the accuracy of the proposed static linearity measurements have been comprehensively explored and analytical design equations for a practical implementation have been developed.

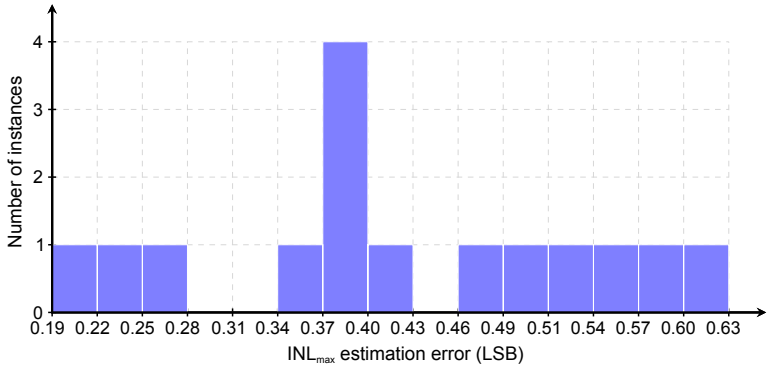


Figure 2.12 – Histogram of the INL estimation error for the 15 fabricated generator samples.

The proposed discrete-time ramp generator has been designed in a 65 nm CMOS technology and its performance has been experimentally validated in the laboratory. Obtained measurements on 15 fabricated samples show an average static ENOB of 14.5 bit, in a ± 2 V differential output range. The feasibility and performance of the proposed static linearity measurement strategy has been verified in an ADC static test scenario with experimental measurements. The fabricated ramp stimulus generator has been employed for characterizing the INL of an off-the-shelf 11-bit ADC. Experimental results show an error in the estimation of the INL of $\sim \pm 0.3$ LSB, compared to reference measurements performed with external high-precision equipment.

Chapter 3

Sinusoidal signal generation for analog and mixed-signal BIST

3.1 Introduction

One of the main key points to enable mixed-signal BIST solutions is the development of accurate on-chip analog signal generators that can provide appropriate test stimuli and replace costly external signal generators in standard analog and mixed-signal functional test protocols. In this line, the on-chip generation of sinusoidal stimuli is an unavoidable first step for moving many functional test approaches to a full-BIST solution. Just to provide an example, the majority of the standard test setups for ADC characterization described in [3] require the application of precise analog sinusoidal test stimuli. However, the increasing performance of current analog and mixed-signal circuitry makes the design of these embedded generators quite challenging. For a proper functional characterization, the embedded sinusoidal signal generator has to work at the DUT operation frequency and provide a spectrally pure stimulus at least two effective bits above the nominal linearity of the DUT. At the same time, the embedded sinusoidal signal generator has to be simple, robust and compact, in such a way that the additional design effort and area overhead are limited.

Sinusoidal signal generation for BIST applications continues to be a recurrent topic in the test research community. A number of different proposals for on-chip sinusoidal signal generation have been published in the last years [14,40–48]. In general, proposed generation solutions can be classified into two main families: closed-loop oscillators and open-loop generators.

Closed-loop oscillators are a classical solution for sinusoidal signal generation. They consist in a filtering stage with a non-linear feedback. An example of implementation of an oscillator-based generator is proposed in [43]. The proposed oscillator is based on a high-Q switched-capacitor band-pass filter with a limiter in the feedback loop. The work in [40] proposes an improved design based on a band-pass filter with a multilevel hard limiter in the feedback loop. The multilevel limiter is used to attenuate the third- and fifth-order harmonic components in the spectrum of the output signal.The work in [44] presents a high-linearity analog oscillator based on a digital $\Sigma\Delta$ resonator. An external

6-th order filter is required to reject the shaped quantization noise. In general, the linearity of an oscillator-based generator depends strongly on the linearity and the selectivity of the employed filter and the smoothness of the non-linear feedback which make the implementation of these circuits quite challenging.

On the other hand, open-loop generators are based on a digital pattern generator that provides a digitized high-resolution sinusoidal signal, a D/A converter to translate the signal to the analog domain and a smoothing filter to attenuate undesired harmonic components. In this line, the work in [14, 46] propose practical implementations of an on-chip signal generator based on storing and reproducing a digital $\Sigma\Delta$ bitstream encoding a high-resolution sinusoidal signal. This 1-bit bitstream is converted to the analog domain using a 1-bit D/A converter and then filtered. The quality of the output signal is usually limited by the filtering stage and the order of the $\Sigma\Delta$ modulation. The output filter has to be of a higher order than the modulation, which may increase the complexity of the filter.

Other open-loop generation strategies propose to remove unwanted distortion harmonic components at the output of the D/A converter by measuring the magnitude and phase of the harmonic components and pre-distorting the input bitstream to cancel them, as presented in [49]. However, this digital correction technique requires the use of additional resources (namely additional A/D and D/A converters) for measuring the target harmonic components of the generated sinusoidal signal and injecting the correction into the initial digital signal.

The proposal of sinusoidal signal generators based on harmonic cancellation principles may be an efficient solution for the aforementioned limitations. Harmonic cancellation is a signal manipulation technique aimed at generating an analog signal with a high spectral quality by combining a set of scaled and time-shifted versions of an arbitrary periodic signal. This technique allows removing a set of unwanted harmonic distortion components from the spectrum of a generic periodical signal, without additional resources for measuring and pre-distortion. Hence, harmonic cancellation can be used in a practical sinusoidal signal generation scenario to cancel harmonic components close to the fundamental frequency of the desired signal, while a lenient low-pass filter attenuates higher-order harmonics. The first practical implementation of a sinusoidal signal generator based on harmonic cancellation principles was presented for the first time back in the 60's [50], although this proposal has not been fully developed until recent years because of technological limitations. Thus, in the last few years, several sinusoidal signal generators have been presented that take advantage of harmonic cancellation to reduce the complexity of the required circuitry [41, 45, 48, 51–54].

In this line, harmonic cancellation techniques have been applied in [51–54] to design efficient analog signal generators based on mostly-digital circuitry. The work in [51] proposes a mostly digital architecture based on a ring oscillator to produce time-delayed versions of a digital square-wave, a weighted resistor summing network to combine the time-delayed square-wave signals in order to cancel the 3^{rd}-, 5^{th}-, 7^{th}- and 9^{th}-order harmonic components in the generated signal, and a low order analog low-pass filter to attenuate high-order harmonic components. The feasibility of this strategy was demonstrated experimentally. However, the employed circuitry is very sensitive to delay errors in the ring oscillator and an external calibration loop is required. Based on this work, a second generator combining two stages of harmonic cancellation to attenuate a larger number of harmonics was designed in [52]. The number of cancelled harmonic components was extended until the 21^{st}-order component. The weighting stages were designed as a network of current mirrors to scale the

phase-shifted square-waves.

Similarly, the sinusoidal signal generator proposed in [53] also proposes a mostly-digital architecture based on harmonic cancellation principles. The proposed generator is composed of a digital counter followed by some digital logic for generating digital square-wave signals with controlled duty-cycles. The generated square-waves are combined and converted to the digital domain using a current-steering DAC. The generator is limited by the variations of the current-steering sources of the DAC due to mismatch, which may degrade the performance of the proposed system. In order to overcome the mismatch issues in the DAC, authors in [54] propose to use a Dynamic Element Matching (DEM) strategy to improve the linearity of the generator.

My research in this line started with my PhD thesis under the direction of Dr. Diego Vázquez at the University of Seville, Spain. During my PhD, I proposed a novel family of analog sinusoidal signal generators based on a modified analog filter [42]. This modification consisted in integrating a time-dependent input stage that allowed the generation of an arbitrary analog waveform when the filter was excited by a constant DC signal. This research continued during my post-doc under the direction of Dr. Gildas Léger at the Instituto de Microelectrónica de Sevilla (IMSE-CNM), Spain, where I explored the implementation of harmonic cancellation techniques within the architecture of my previous analog signal generator [41]. More recently, this work has been continued within the PhD thesis of Dr. Hani Malloug, who I co-supervised together with Salvador Mir at TIMA laboratory in the framework of a Nano2017 collaborative project with STMicroelectronics. This PhD project was focused in the development of mostly-digital sinusoidal signal generators for mixed-signal BIST applications in advanced nanometric nodes, namely in STMicroelectronics 28 nm FDSOI technology. Dr. Malloug successfully defended his PhD thesis on September 28th 2018 and the obtained results have been published in international journals and conferences [55–59]. This chapter summarizes the main developments and results obtained during this PhD project.

3.2 Theoretical basis: harmonic cancellation

Harmonic cancellation is a signal processing strategy aimed at cancelling a selected set of harmonic components in a periodical signal by adding scaled and delayed versions of the original signal.

Let us consider a generic periodic signal $x(t)$ expressed as a Fourier series expansion as:

$$x(t) = \sum_{k=1}^{\infty} A_k \cos(k\omega_0 t + \varphi_k) \tag{3.1}$$

where A_k and φ_k are the amplitude and phase of harmonic component k in signal $x(t)$, respectively, and ω_0 is the fundamental frequency of $x(t)$.

Without loss of generality, let us define signal $y(t)$ as the linear combination of signal $x(t)$ scaled by a factor α_0 and p pairs of scaled and shifted signals with opposite time-shifts Δt_i and $-\Delta t_i$ with

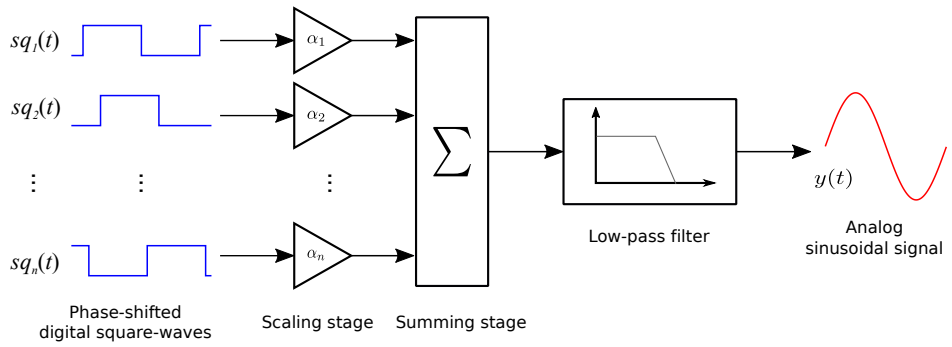


Figure 3.1 – Analog sinusoidal signal generator based on applying harmonic cancellation principles to a set of phase-shifted and scaled digital square-waves.

respect to signal $x(t)$ and scaled by a factor α_i,

$$y(t) = \alpha_0 x(t) + \sum_{i=1}^{p} \alpha_i \left[x(t + \Delta t_i) + x(t - \Delta t_i) \right] \tag{3.2}$$

From equations (3.1) and (3.2) it can be derived,

$$y(t) = \sum_{k=1}^{\infty} A_k \left[\alpha_0 + 2 \sum_{i=1}^{p} \alpha_i \cos(k\phi_i) \right] \cos(k\omega_0 t + \varphi_k) \tag{3.3}$$

where $\phi_i = \omega_0 \Delta t_i$.

Thus, the combination of a periodical signal and its scaled and phase-shifted versions has a spectral content which is that of the original periodic signal but scaled by coefficients $[\alpha_0 + 2\sum_{i=1}^{p} \alpha_i \cos(k\phi_i)]$. In other words, by selecting an appropriate set of phase shifts ϕ_i and scale weights α_0, α_i such as these coefficients are small for given values of k, unwanted harmonic components in $y(t)$ can be attenuated or completely cancelled.

3.3 Practical implementation

We propose to apply the described harmonic cancellation technique to a set of digital square-waves to produce a high-quality analog sinusoidal signal, as it is conceptually shown in Fig. 3.1. Square-wave signals can be easily and efficiently generated in the digital domain, which simplifies the design of the generator. The Fourier series expansion of a square-wave signal $sq(t)$ with a 50% duty-cycle, unit amplitude, and period T, can be expressed as

$$sq(t) = \frac{4}{\pi} \sum_{k=1,3,5,\ldots}^{\infty} \frac{1}{k} \sin(k\omega_0 t) \tag{3.4}$$

where $\omega_0 = 2\pi/T$. The spectral content of the square-wave signal includes only odd-order harmonics whose magnitude decreases as their frequency increases. Harmonic cancellation can be used for cancelling low-order odd harmonic components. According to the previous analysis, multiple practical implementations are possible corresponding to different solutions to the harmonic cancellation conditions.

3.3.1 Harmonic cancellation using irrational weight ratios

Let us assume that we have available p pairs of scaled and delayed versions of $sq(t)$, as defined in (3.3). According to (3.3), in order to cancel the k-th harmonic component of $sq(t)$, we have to find the phase-shifts ϕ_i and weights α_0, α_i that verify,

$$\alpha_0 + 2\sum_{i=1}^{p} \alpha_i \cos(k\phi_i) = 0. \tag{3.5}$$

A possible solution for cancelling all odd-order harmonic components lower than the $2(2p+1)$-th order is to make $\alpha_0 = 1$, and set phase shifts ϕ_i and weights α_i as

$$\begin{cases} \phi_i = i\frac{2\pi}{4(p+1)} & 1 \leq i \leq p \\ \alpha_i = cos(i\frac{2\pi}{4(p+1)}) & 1 \leq i \leq p \end{cases} \tag{3.6}$$

These design equations allow cancelling a given set of low-order odd harmonic components in the original square-wave signal $sq(t)$, while a lenient low-pass filter can be used to attenuate high-frequency harmonic components. Figure 3.2 shows a conceptual block diagram of the proposed generator. The core of the generator is a circular shift-register with N flip-flops. The shift-register is loaded at the beginning of the operation by $N/2$ consecutive logic ones followed by $N/2$ consecutive logic zeros. When the circular shift-register is driven by a clock signal at frequency f_{ck}, the output of each flip-flop is a square-wave signal with a 50% duty-cycle and frequency f_{ck}/N. By construction, the phase-shift between two consecutive outputs in the circular shift-register is $2\pi/N$, which allows an easy implementation of the required phase-shifts in (3.6) just by properly adjusting the number of flip-flops N in the register and selecting the appropriate flip-flop output in the shift-register.

Subsequently, the set of selected phase-shifted square-waves from the shift-register are conveniently scaled according to (3.6) and summed to generate a sinusoidal output. Different practical implementations of the scaling and summing node have been proposed in the literature, including weighted resistor networks [45, 51, 56], weighted current sources [57], and complete current-steering DACs [60]. Finally, a lenient first-order lowpass filter attenuates higher-order harmonics not affected by the harmonic cancellation strategy.

In a practical implementation, there is a clear trade-off between the number of harmonics that can be cancelled and the complexity of the generator, since the necessary number of delayed versions of the original square-wave increases if harmonic cancellation is extended to high-order harmonics. A good trade-off solution explored in previous work [51,56–58,60,61] and conceptually depicted in Fig. 3.3 is to consider five time-delayed square-waves with opposite phase-shifts $\phi_1 = \frac{\pi}{6}$, and $\phi_2 = \frac{\pi}{3}$ and

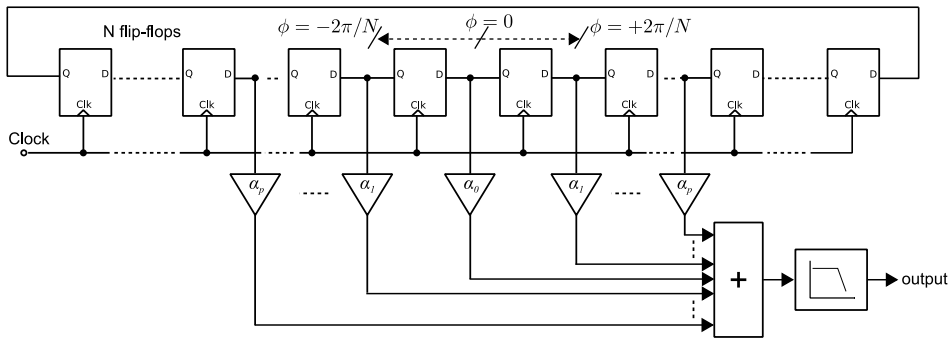


Figure 3.2 – Generic architecture of the proposed sinusoidal signal generator.

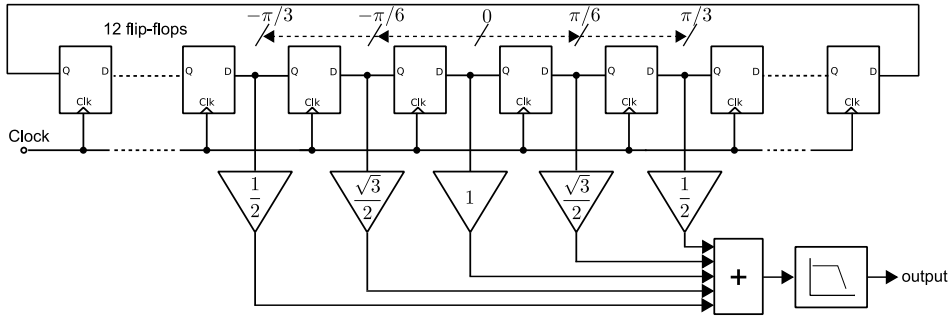


Figure 3.3 – Architecture of the proposed sinusoidal signal generator using five signal phases to cancel the third-, fifth-, seventh-, and ninth-order harmonic components.

scale weights $\alpha_0 = 1$, $\alpha_1 = \frac{\sqrt{3}}{2}$, and $\alpha_2 = \frac{1}{2}$, using the notation in (3.3). According to the analytical results in (3.3)-(3.6), this configuration cancels the third-, fifth-, seventh-, and ninth-order harmonic components in the original square-wave, while keeping a reduced design complexity. However, the practical implementation of the irrational weight $\alpha_1 = \frac{\sqrt{3}}{2}$ can be challenging, either as a resistor ratio or as a weighted current source, which makes the effectiveness of the harmonic cancellation very sensitive to mismatch and requires careful layout of the elements and, usually, dedicated calibration [51, 56, 57] or mismatch compensation techniques like Dynamic Element Matching [60].

3.3.2 Harmonic cancellation using integer scale weight ratios

Let us consider signal $y_1(t)$ defined as signal $y(t)$ in (3.2) with weights $\alpha_0 = 2$, $\alpha_1 = 1$, and $p = 1$ as

$$\begin{aligned} y_1(t) &= 2\,x(t) + x(t + \Delta t_1) + x(t - \Delta t_1) \\ &= \sum_{k=1}^{\infty} 2A_k \left[1 + \cos(k\phi_1)\right] \cos(k\omega_0 t + \varphi_k) \end{aligned} \tag{3.7}$$

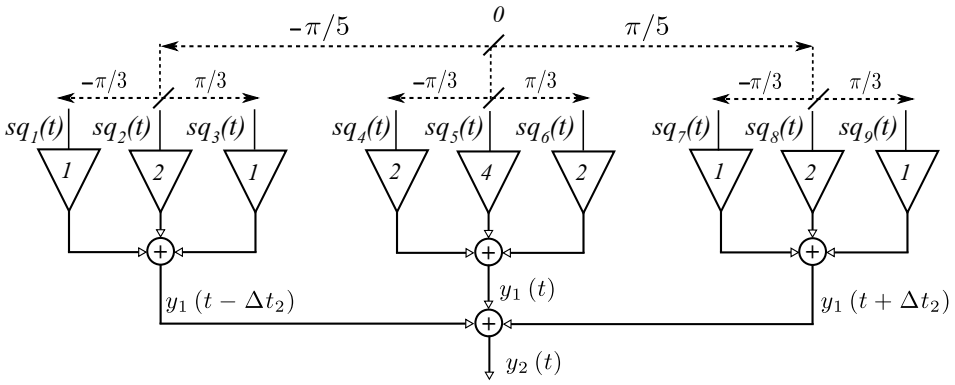


Figure 3.4 – Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios to cancel the 3^{rd} and 5^{th} order harmonic components

with the same notation defined in the previous section. In this configuration, it is easy to demonstrate that the third-harmonic component of the original signal $x(t)$ can be cancelled by setting $\phi_1 = \pi/3$. Let us iterate the same process and define now signal $y_2(t)$ as the linear combination of signal $y_1(t)$ and two phase-shifted versions of $y_1(t)$ with opposite delays $\pm\Delta t_2$ as

$$\begin{aligned} y_2(t) &= 2\,y_1(t) + y_1(t+\Delta t_2) + y_1(t-\Delta t_2) \\ &= \sum_{k=1}^{\infty} 2^2 A_k \left[1+\cos(k\phi_1)\right]\left[1+\cos(k\phi_2)\right]\cos(k\omega_0 t + \varphi_k) \end{aligned} \tag{3.8}$$

again with the same notation defined in the previous section. As it can be observed, by adding a new pair of delayed signals now we can cancel two harmonic components of the original signal $x(t)$.

For instance, by setting $\phi_1 = \pi/3$ and $\phi_2 = \pi/5$ we can cancel the third- and fifth- order harmonic components. This solution employs a combination of 9 square-waves $sq_1(t)$ to $sq_9(t)$, as it is schematically shown in Fig. 3.4. These 9 square-waves are distributed into three sets of square-waves, each set contains three square-waves with a relative phase-shift of $\pm\pi/3$, and the sets are phase shifted by $\pm\pi/5$.

Figure 3.5 shows a block diagram of a sinusoidal signal generator based on this harmonic cancellation strategy for canceling the third- and fifth-order harmonic components. The required phase-shifts can be easily achieved using a shift-register with 30 flip-flops, initially loaded to 15 consecutive logic ones and 15 consecutive logic zeros to generate a 50% duty-cycle square-wave. In this case, scale factors ratios are integer –and powers of 2– which simplifies matching of the different signal branches in a practical implementation and relaxes its design effort.

This harmonic cancellation strategy can be easily generalized for cancelling any number of harmonics. Thus, if we iterate the process p times, the resulting signal $y_p(t)$ can be written as

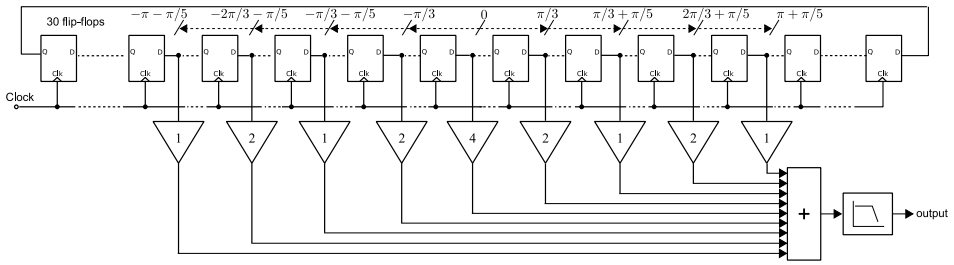


Figure 3.5 – Architecture of the proposed sinusoidal signal generator using nine signal phases and integer scale weights to cancel the third-, and fifth-order harmonic components.

$$\begin{aligned} y_p(t) &= 2\,y_{p-1}(t) + y_{p-1}(t+\Delta t_p) + y_{p-1}(t-\Delta t_p) \\ &= \sum_{k=1}^{\infty} 2^p A_k \prod_{i=1}^{p} [1+\cos(k\phi_i)]\cos(k\omega_0 t+\varphi_k) \end{aligned} \tag{3.9}$$

And the resulting cancellation condition for a given harmonic k can be expressed as

$$\prod_{i=1}^{p} [1+\cos(k\phi_i)] = 0 \tag{3.10}$$

However, cancelling multiple harmonic components requires longer shift-registers to be able to generate the required relative phase-shifts and increases the number of required square-wave signals that have to be combined, hence increasing the complexity of the design.

3.3.3 Harmonic cancellation using unitary scale weight ratios and an odd number of signals

A similar strategy can be devised to achieve harmonic cancellation conditions using unitary weight ratios for all the signal phases. Let us consider signal $y_1(t)$ defined as signal $y(t)$ in (3.2) with weights $\alpha_0 = 1$, $\alpha_1 = 1$, and $p = 1$ as

$$\begin{aligned} y_1(t) &= x(t) + x(t+\Delta t_1) + x(t-\Delta t_1) \\ &= \sum_{k=1}^{\infty} A_k\,[1+2\cos(k\phi_1)]\cos(k\omega_0 t+\varphi_k) \end{aligned} \tag{3.11}$$

with the same notation defined in the previous section. In this configuration, a given harmonic component can be cancelled by choosing an appropriate value of ϕ_1. For instance, the third-order harmonic component can be cancelled by setting $\phi_1 = 2\pi/9$. Similarly to the previous case, the process can be

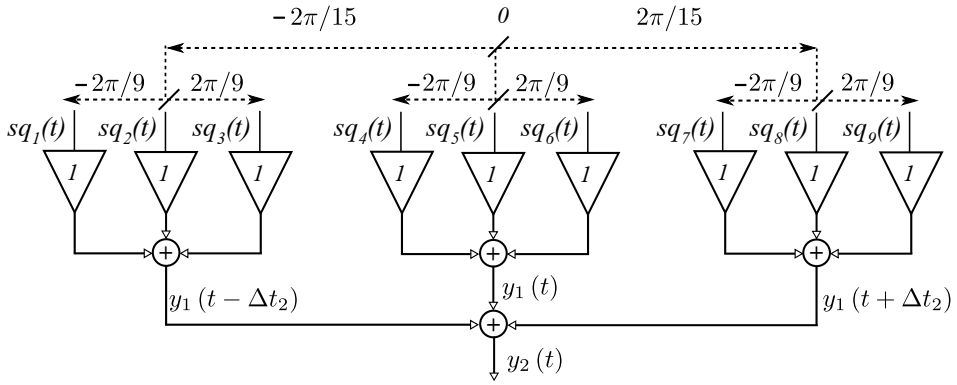


Figure 3.6 – Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3^{rd} and 5^{th} order harmonic components

iterated. Let us define signal $y_2(t)$ as

$$\begin{aligned} y_2(t) &= y_1(t) + y_1(t + \Delta t_2) + y_1(t - \Delta t_2) \\ &= \sum_{k=1}^{\infty} A_k \left[1 + 2\cos(k\phi_1)\right] \left[1 + 2\cos(k\phi_2)\right] \cos(k\omega_0 t + \varphi_k) \end{aligned} \tag{3.12}$$

Again, as it can be observed, two harmonic components can be cancelled by carefully selecting variables ϕ_1 and ϕ_2. For instance, the third- and fifth-order harmonic components can be cancelled by setting $\phi_1 = 2\pi/9$ and $\phi_2 = 2\pi/15$.

Similarly to the harmonic cancellation strategy with integer scale ratios presented in the previous subsection, the harmonic cancellation strategy with unitary scale ratios can be easily implemented using 9 square-waves $sq_1(t)$ to $sq_9(t)$, as it is schematically shown in Fig. 3.6. These 9 square-waves are distributed into three sets of square-waves, each set contains three square-waves with a relative phase-shift or $\pm 2\pi/9$, and the sets are phase shifted by $\pm 2\pi/15$.

Figure 3.7 shows a conceptual block diagram of a signal generator based on this harmonic cancellation strategy with built-in cancellation of the third and fifth harmonic components. As in the previous strategy, the required phase-shifts can be achieved using a shift-register with 90 flip-flops, initially loaded to 45 consecutive logic ones and 45 consecutive logic zeros. In this case, the scale factors in all signal paths can be made equal (i.e., unitary ratios), which further relaxes the design effort for improving the matching of the different signal paths.

Again, this harmonic cancellation strategy can be also generalized to cancel any number of harmonics. If we iterate the process p times, the resulting signal $y_p(t)$ can be written as

$$\begin{aligned} y_p(t) &= y_{p-1} + y_{p-1}(t + \Delta t_p) + y_{p-1}(t - \Delta t_p) \\ &= \sum_{k=1}^{\infty} A_k \prod_{i=1}^{p} [1 + 2\cos(k\phi_i)] \cos(k\omega_0 t + \varphi_k) \end{aligned} \tag{3.13}$$

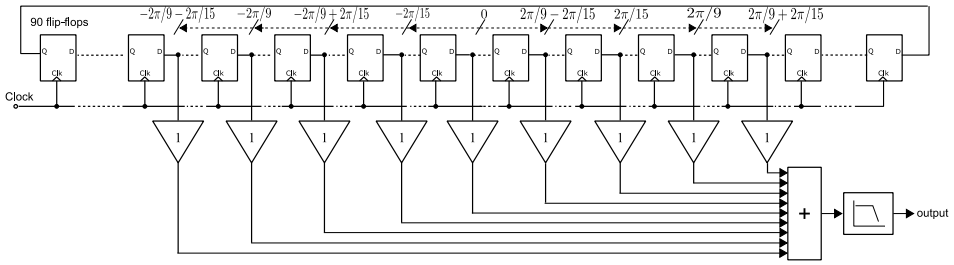


Figure 3.7 – Architecture of the proposed sinusoidal signal generator using 9 signal phases and unitary scale weights to cancel the third-, and fifth-order harmonic components.

And the resulting cancellation condition for a given harmonic k lower than $2p+1$ can be expressed as

$$\prod_{i=1}^{p}[1+2\cos(k\phi_i)]=0. \tag{3.14}$$

This harmonic cancellation strategy simplify the implementation of scale weight by making them equal using the same number of square-waves, however it requires a longer shift-register to provide the appropriate phase-shifts.

3.3.4 Harmonic cancellation using unitary scale weight ratios and an even number of signals

In order to further reduce the complexity of the previous generation strategy, we propose a similar harmonic cancellation strategy using unitary weight ratios with a reduced number of square-waves. Let us consider signal $y_1(t)$ defined as signal $y(t)$ in (3.2) with weights $\alpha_0=0$, $\alpha_1=1$, and $p=1$ as

$$\begin{aligned} y_1(t) &= x(t+\Delta t_1)+x(t-\Delta t_1) \\ &= \sum_{k=1}^{\infty} 2A_k\cos(k\phi_1)\cos(k\omega_0 t+\varphi_k) \end{aligned} \tag{3.15}$$

with the same notation defined in the previous section. In this configuration, a given harmonic component can be cancelled by choosing an appropriate value of ϕ_1. For instance, the third harmonic component can be cancelled by setting $\phi_1=\pi/6$. Similarly to the previous case, the process can be iterated. Let us define signal $y_2(t)$ as

$$\begin{aligned} y_2(t) &= y_1(t+\Delta t_2)+y_1(t-\Delta t_2) \\ &= \sum_{k=1}^{\infty} 2^2A_k\cos(k\phi_1)\cos(k\phi_2)\cos(k\omega_0 t+\varphi_k) \end{aligned} \tag{3.16}$$

In the resultant signal $y_2(t)$, two harmonic components can be cancelled by carefully selecting variables ϕ_1 and ϕ_2. For instance, the third- and fifth-order harmonic components can be suppressed

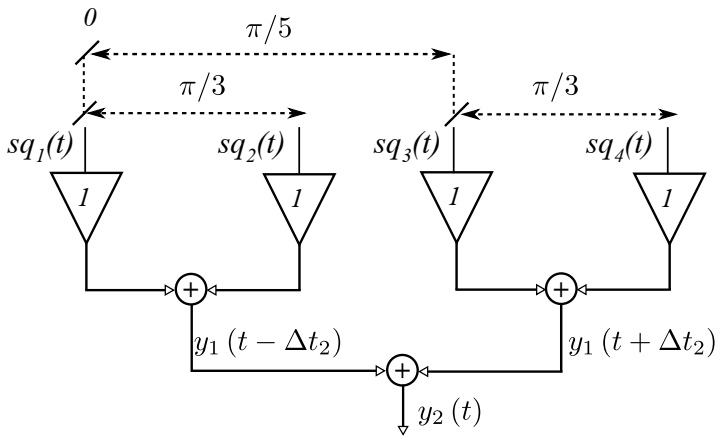


Figure 3.8 – Conceptual block diagram of the harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3^{rd} and 5^{th} order harmonic components

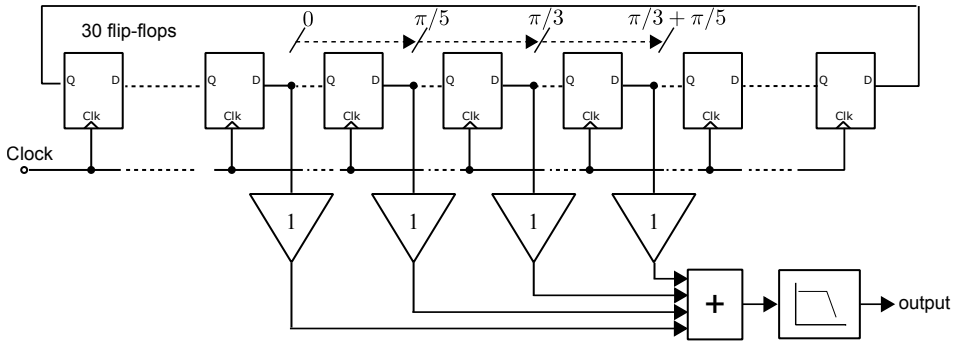


Figure 3.9 – Architecture of the proposed sinusoidal signal generator using four signal phases and unitary scale weights to cancel the third-, and fifth-order harmonic components.

by setting $\phi_1 = \pi/6$ and $\phi_2 = \pi/10$. This harmonic cancellation strategy can be implemented by combining four square-waves $sq_1(t)$ to $sq_4(t)$, as schematically shown in Fig. 3.8. These 4 square-waves are distributed into two sets of two square-waves with relative phase-shifts of $\pi/3$, while the phase-shift between the two sets is of $\pi/5$.

Figure 3.9 shows a conceptual block diagram of a signal generator based on this harmonic cancellation strategy with built-in cancellation of the third- and fifth-order harmonic components. As in the previous strategy, the required phase-shifts can be easily achieved using a shift-register with 30 flip-flops, initially loaded to 15 consecutive logic ones and 15 consecutive logic zeros. In this case, the scale factors in all signal paths can be made equal (i.e., unitary ratios), which further relaxes the design effort for improving the matching of the different signal paths.

Again, this harmonic cancellation strategy can be also generalized to cancel any number of har-

monics. If we iterate the process p times, the resulting signal $y_p(t)$ can be written as

$$\begin{aligned} y_p(t) &= y_{p-1}(t+\Delta t_p) + y_{p-1}(t-\Delta t_p) \\ &= \sum_{k=1}^{\infty} 2^p A_k \prod_{i=1}^{p} \cos(k\phi_i)\cos(k\omega_0 t + \varphi_k) \end{aligned} \tag{3.17}$$

And the resulting cancellation condition for a given harmonic k can be expressed as

$$\prod_{i=1}^{p} \cos(k\phi_i) = 0. \tag{3.18}$$

Similarly to the previous harmonic cancellation strategies, multiple harmonic components can be cancelled using this design equation, at the cost of increasing the design complexity. However, it has to be noted that for this solution there is a risk of attenuating strongly the fundamental component if a high number of square-waves are combined: the magnitude of the fundamental component is scaled by factor $2^p \prod_{i=1}^{p} \cos(\phi_i)$ (see (3.17)), and this factor tends to zero as p increases.

3.3.5 Discussion

In the view of the obtained analytical results, it can be stated that there is a trade-off between the complexity of the scaling and summing network, the number of distortion harmonic components that can be cancelled, the number of necessary phase-shifted square-waves, and the frequency of the generated sinusoidal signal. Table 3.1 summarizes the main characteristics of the four considered cancellation techniques in this line. Thus, harmonic cancellation using irrational scale weight ratios in Fig. 3.3 is interesting in terms of the frequency of the generated signal, the reduced number of square-waves and the number of harmonic components that can be canceled. However the implementation of this strategy may be complex and prone to scale weight mismatch because of the irrational scale weight ratios. The harmonic cancellation technique with unitary scale ratios and four signal paths in Fig. 3.9 reduces the necessary hardware resources, but the frequency of the provided signal is decreased with respect to the previous technique. The unitary harmonic cancellation with 9 signal paths in Fig. 3.7 requires a longer shift-register which decreases the frequency of the generated signal. On the other hand, the harmonic cancellation technique using integer scale ratios with 9 square waves in Fig. 3.5 uses the same number of square-wave signals with a shorter shift-register, which increase the frequency of the final output, but it requires different scale ratios between each signal path. Figure 3.10 further clarifies this trade-off. This figure represents the order of the first non-canceled harmonic as a function the number of necessary phase-shifted square-waves for each of the presented sinusoidal signal generation techniques. Additionally, we indicate, for each data point, the set of different weights required for implementing each generator (for the generators with non-unitary weights).

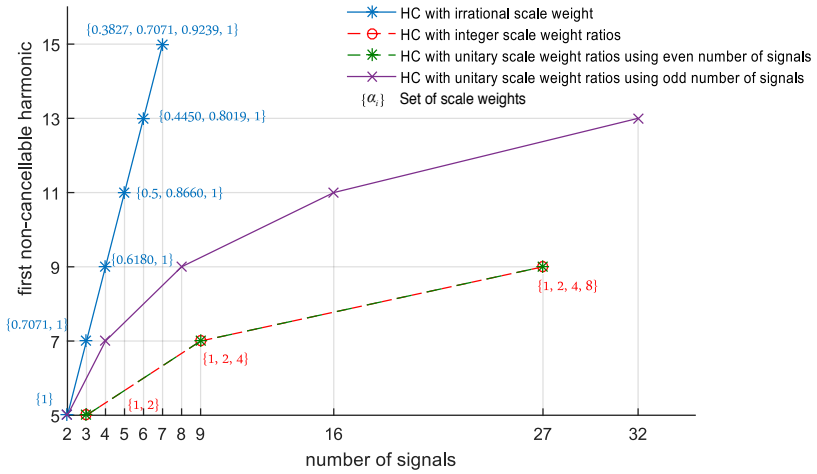


Figure 3.10 – Comparison of the proposed harmonic cancellation strategies.

Type of Scale ratios	Irrational	Integer	Unitary	
Number of square-waves	5	9	9	4
length of flip-flops	12	30	90	30
Frequency of the generated sine-wave	$f_{clk}/12$	$f_{clk}/30$	$f_{clk}/90$	$f_{clk}/30$
Relative phase-shift	$\pi/6$	$\pi/15$	$\pi/45$	$\pi/15$
Harmonic components to be cancelled	$3^{rd}, 5^{th}, 7^{th}, 9^{th}$	$3^{rd}, 5^{th}$	$3^{rd}, 5^{th}$	$3^{rd}, 5^{th}$
Design complexity of the weighting stage	High	low	low	low

Table 3.1 – Comparison of harmonic cancellation strategies

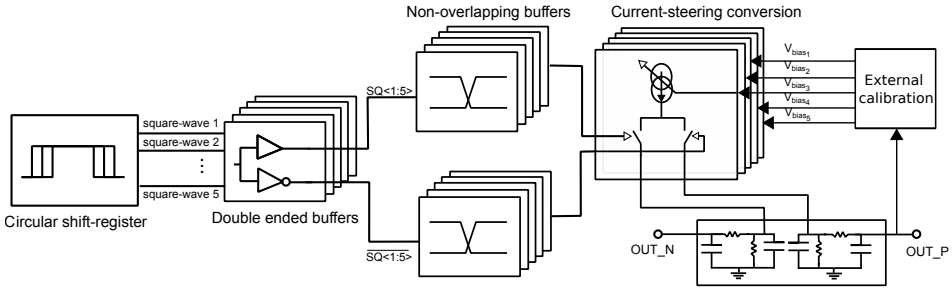


Figure 3.11 – Conceptual block diagram of the proposed sinusoidal signal generator.

3.4 Design of a proof-of-concept prototype

In order to validate the proposed generation strategy in a practical silicon demonstrator, this section presents the design and experimental validation of a proof-of-concept prototype. The proposed generator prototype considers five time-delayed square-waves with opposite phase-shifts $\phi_1 = \frac{\pi}{6}$ and $\phi_2 = \frac{\pi}{3}$ and scale weights $\alpha_0 = 1$, $\alpha_1 = \frac{\sqrt{3}}{2}$ and $\alpha_2 = \frac{1}{2}$, according to the notation in (3.3). These coefficients allow cancelling the third-, fifth-, seventh- and ninth-order harmonic components in the original square-wave signal. The main design goal of this proof-of-concept implementation is to show the feasibility of the harmonic cancellation based on the proposed circuit architecture for the generation of high-speed sinusoidal signals, targeting a generated frequency in the range of hundreds of MHz.

Figure 3.11 shows a conceptual block diagram of the proposed sinusoidal signal generator architecture, directly derived from the general block diagram in Fig. 3.3. The proposed circuitry is composed of six main blocks: circular shift-register, double-ended buffers, non-overlapping buffers, an external calibration block, current-steering branches, and an output low-pass filter.

3.4.1 Circular shift-register

A circular shift-register with twelve flip-flops provides the five square-waves with a 50% duty-cycle and phase-shifts $\phi_1 = \frac{\pi}{6}$ and $\phi_2 = \frac{\pi}{3}$ that are used for harmonic cancellation. The nominal clock frequency for the shift-register was set to $f_{clk} = 2\,\text{GHz}$, which would generate output square-waves at $f = \frac{f_{clk}}{12} = 166.7\,\text{MHz}$. The employed flip-flops are standard scan D-flip-flops with a two-input multiplexer (test enable, T_e, and test input, T_i) on the D input. The scan flip-flop behaves as a normal D-flip-flop when T_e is at a logic '0', i.e., the output Q follows the input D at the clock rising edge. On the other hand when T_e is set to a logic '1', the output Q is set to T_i, asynchronously and independent of D. These asynchronous inputs are used for loading in parallel the initial digital square-wave into the circular register.

Two key points for the functionality of the proposed system are the duty-cycle of the five square-wave outputs of the circular shift-register, that has to be kept at 50% (otherwise even harmonics will appear at the output), and the relative phase-shifts between the outputs, that have to comply to

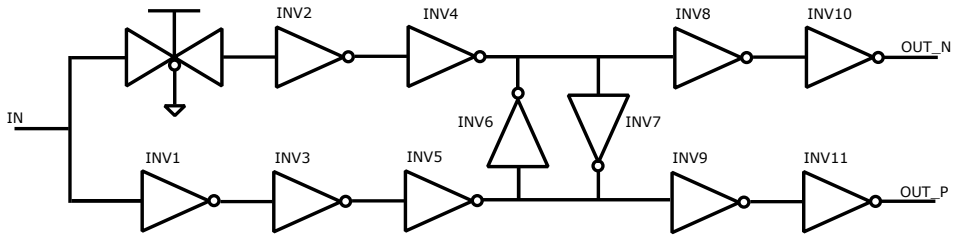


Figure 3.12 – Schematic of the low-skew double-ended buffer.

the design values $\phi_1 = \frac{\pi}{6}$ and $\phi_2 = \frac{\pi}{3}$ (otherwise the effectiveness of the harmonic cancellation is compromised). Ideally, the synchronous operation of the circular shift-register guarantees these two conditions. However, non-idealities such as mismatch between the delays of the individual flip-flops or clock skew in the distribution of the clock signal to the flip-flops could jeopardize these conditions, specially for high clock frequencies.

3.4.2 Double-ended buffer

The square-waves provided by the circular shift-register are converted to differential signals using a single-ended to double-ended buffer. This double-ended buffer is designed in order to ensure a low skew between the complementary outputs. As illustrated in Fig. 3.12, the input stage of the buffer has two branches, the input of the positive branch includes a transmission gate followed by two inverters (INV2 and INV4) to generate a buffered version of the input, while the input of the negative branch has a chain of three inverters (INV1, INV2 and INV3) to generate the complement of the input signal. The transmission gate in the positive branch is used to compensate the propagation delay of INV1 in the negative branch, and it is designed to be continuously enabled. A cross-coupled latch (INV6 and INV7) is used to reduce the rise and fall times of the buffer and to reduce the skew between the differential signals. A buffering output stage (INV8 to INV11) is used to provide appropriate fan out to drive the following stage.

3.4.3 Non-overlapping buffer

Ideally, the outputs of the double-ended buffer may drive the PMOS switches in the differential current-steering branches (see the conceptual block diagram in Fig. 3.2). However, to ensure a good switching of current-sources, it is important to avoid opening the differential switches at the same time. For this reason, we designed a non-overlapping buffer, similar to the classical non-overlapping phase generators for switched-capacitor circuits [62]. The non-overlapping buffer is designed to provide complementary signals which intersect close to the low state to avoid opening the differential switches simultaneously, while keeping the 50% duty cycle of the square-waves to avoid even-order harmonics in the generated sinusoid.

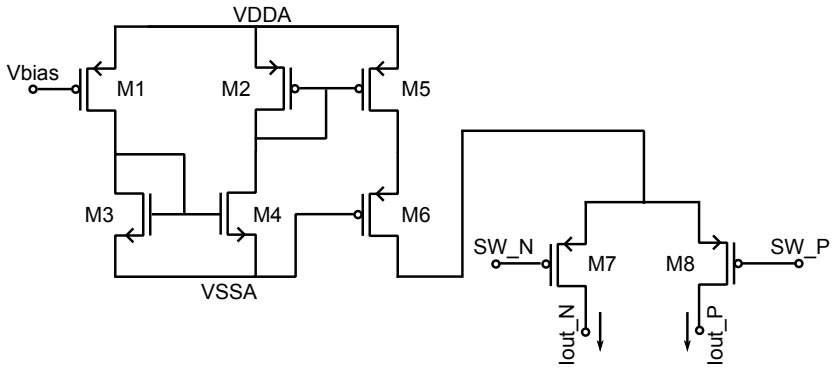


Figure 3.13 – Basic current-steering digital-to-analog conversion branch.

3.4.4 Current-steering digital-to-analog conversion

The set of time-delayed square-waves provided by the non-overlapping buffers drive a simplified current-steering DAC with five branches. Each branch is designed to generate a weighted current with weight ratios equal to $\alpha_1 = \sqrt{3}/2$ and $\alpha_2 = 1/2$ as it was described in section III. Fig. 3.13 shows the transistor-level schematic of the basic current-source employed in the design. Transistor M1 is biased at a controlled voltage V_{bias} to generate a current that is then replicated by two current mirrors (M2 to M5). Transistor M6 is a cascode transistor to increase the output impedance of the current source. The output current is switched in a differential mode by switches M7 and M8 which are controlled by the time-delayed square-wave signals provided from the digital part of the circuit. The switches are designed with minimum sizes to reduce the parasitic capacitors at the transistor gates.

3.4.5 Output filter

The output filter is a simple second-order passive low-pass filter, built as the cascade of two RC filters. This filter acts as summing node for the currents generated by the current-steering branches, and provides the attenuation of higher-order harmonics.

3.4.6 External calibration

According to the guidelines in [57], the digital circuitry has been sized to guarantee a timing accuracy better than 2 ps in terms of phase-shift and duty cycle deviations, across the operation corners. This timing accuracy assures a correct harmonic cancellation at the target generated frequency $f_{sine} = \frac{f_{clk}}{12} = 166.67$ MHz. On the other hand, the analysis in [57] also shows that the mismatch between the weighted current-steering branches should be below 1% for a correct harmonic cancelation. Matching the PMOS current-steering branches to this level of accuracy would require a significant area and/or power overhead. Instead, for this proof-of-concept prototype, we resort to an external calibration strategy for adjusting the current ratios to the required harmonic cancellation weights. Moreover, this calibration strategy is simple enough to be implemented on-chip in a future demonstrator.

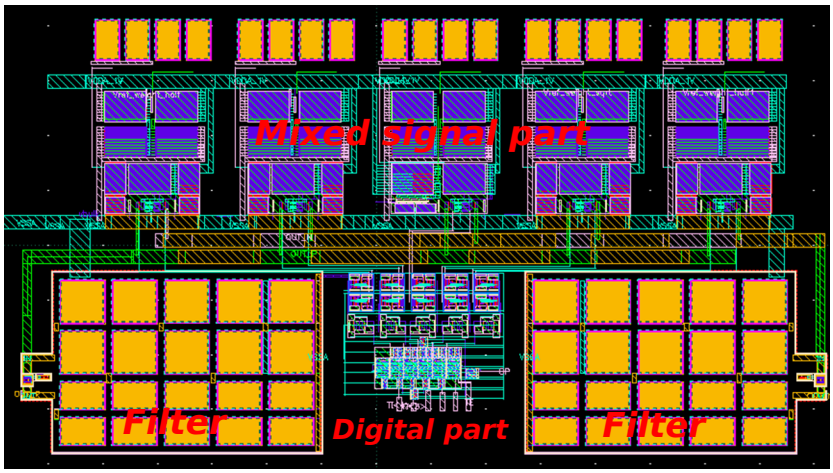


Figure 3.14 – Layout of the sinusoidal signal generator in the selected 28 nm FDSOI technology. The circuit occupies $140\,\mu$m by $80\,\mu$m.

The current provided by the i-th current-steering branch is controlled via its bias voltage $V_{bias,i}$ ($i = 1, \ldots, 5$). In this proof-of-concept generator, each $V_{bias,i}$ is generated by external DC sources based on an iterative calibration process that relies on external DC measurements. The calibration technique starts by setting the initial bias voltages $V_{bias,i}$ to their nominal values obtained by electrical simulation. Then we program the flip-flops in the digital shift-register to activate the current-steering branches sequentially and one at a time. By monitoring the resulting DC output voltages and adjusting $V_{bias,i}$ appropriately, it is possible to recover the target current ratios required by the harmonic calibration algorithm.

3.5 Experimental results

Figure 3.14 shows the layout of the proof-of-concept prototype. The layout was developed according to the design rules of the 28 nm FDSOI technology and following mixed-signal conventional layout practices. Thus, the analog and digital sections are clearly separated. We minimized the number of crossings between analog and digital paths, and added appropriate shielding when necessary. The current sources have an identical layout to improve matching, while the output filter is laid out to keep a differential path to the output pads. Decoupling capacitors have been added to sensitive DC nodes. The digital section is laid out in a symmetrical fashion with respect to the central vertical axis of the circuit, while the routing of the phase-shifted square-waves to the analog section has been carefully designed to provide the same length for the different signals in order to avoid imbalanced delays. The area of the circuit is $140\,\mu$m by $80\,\mu$m.

The proof-of-concept prototype was designed for wafer-level tests using micro-probes. The clock signal, DC bias voltages and digital configuration signals are generated using external equipment, while the differential output of the generator is fed to a spectrum analyzer for evaluating the linearity

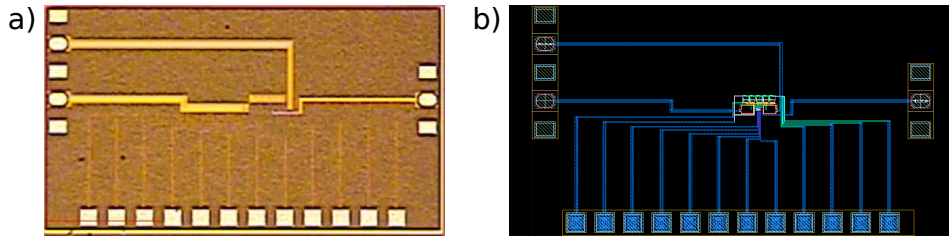


Figure 3.15 – a) Microphotograph of the fabricated sinusoidal signal generator; b) Layout including micro-probe pads.

of the generated signal. The experimental setup is completed by an external high-precision voltmeter used for calibration purposes, as described in the previous section. Fig. 3.15a shows a microphotograph of the fabricated circuit, including the micro-probe pads. An image of the layout including the micro-probe pads has been included in Fig. 3.15b for reference.

In order to show the feasibility of the proposed calibrated harmonic cancellation strategy, Fig. 3.16 and Fig. 3.17 show the spectrum of the generated sinusoidal signal as captured by the spectrum analyzer, before and after calibration, respectively. The clock signal was set to 2 GHz for both experiments, which provides a generated output sinusoid at 166.67 MHz. In terms of linearity, the performance of the uncalibrated generator is limited by the $3^{rd}-$ and the 5^{th}-order harmonic components with a power equal to -41 dBc and -45 dBc, respectively, while even order harmonics are below the noise floor of the spectrum analyzer. The THD and SFDR of the uncalibrated generated signal at 166.67 MHz are -38.9 dB and 41.5 dB, respectively. On the other hand, after the calibration procedure, the obtained spectrum (see Fig. 3.17) shows an improvement of the linearity of the generated signal where all odd harmonic components are significantly attenuated. Indeed, in terms of power, the magnitude of the odd harmonic components after calibration is very close to the noise floor of the spectrum analyzer (around -93 dBm). The harmonic components above the 11^{th}-order harmonic component are also attenuated by the low-pass filter and are below the noise floor. The calibrated signal at 166.67 MHz has a THD of -46 dB and a SFDR of 52 dB, which represents an improvement of ~ 10 dB with respect to the uncalibrated generator. The linearity of the calibrated generator is limited by the even-order harmonic components, mainly the 4^{th}- and the 6^{th}-order harmonics that cannot be calibrated with the proposed strategy.

The limitations in the linearity of the obtained experimental results can be explained by taking into account: a) the finite resolution of the calibration sources (about ± 1 mV) and b) the unavoidable unbalances in our test setup that break the symmetry of the differential output signal paths. Point a) causes incomplete harmonic cancellation of the odd-order harmonics, while point b) generates even-order harmonics.

For the purpose of exploring the frequency behavior of the fabricated prototype, the previous experiment was repeated by sweeping the clock frequency from 20 MHz to 4 GHz, which generates sinusoidal signals from 1.67 MHz to 333 MHz. Figure 3.18 shows the SFDR and THD of the generated signals after calibration, as a function of the generated output frequency. It has to be noted that the proposed proof-of-concept implementation has a fixed low-pass output filter with a cut-off frequency



Figure 3.16 – Spectrum of the generated sinusoidal signal before calibration, captured from the spectrum analyzer screen.

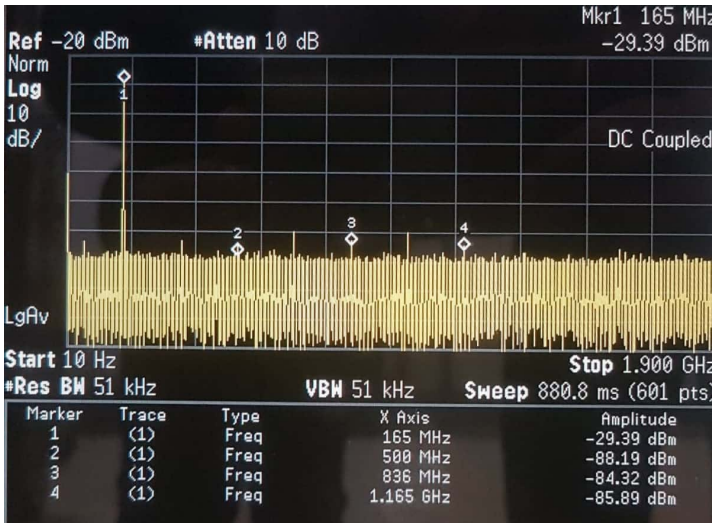


Figure 3.17 – Spectrum of the generated sinusoidal signal after calibration, captured from the spectrum analyzer screen.

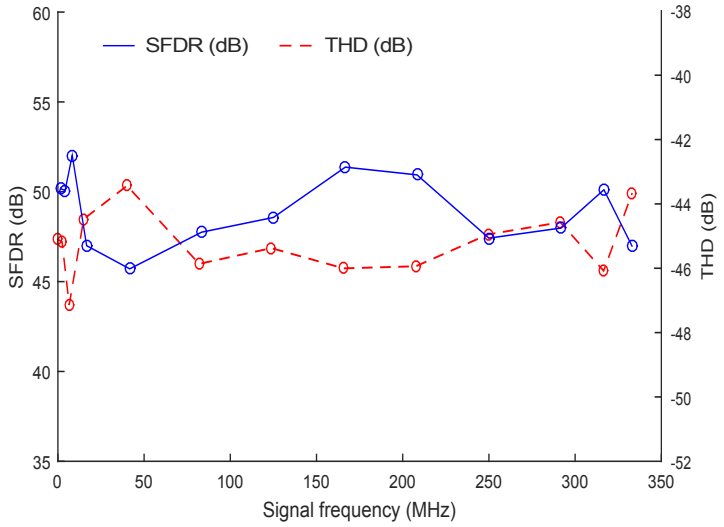


Figure 3.18 – Generator linearity variation as a function of the generated frequency. The clock frequency was varied from 20 MHz to 4 GHz.

of 166.67 MHz. It is then expected that the attenuation of the high-order harmonic components will be reduced for generated output frequencies lower than 166 MHz, while the fundamental component will be attenuated for output frequencies above 166 MHz. Results in Fig. 3.18, even contemplating this expected degradation, show a fairly constant behavior across the considered frequency range, with an average SFDR of 49 dB and an average THD of -45 dB. It is also clear that the maximum linearity performance is achieved in the frequency range from 150 MHz to 200 MHz, which is coherent with the initial design target of a 166 MHz operation frequency.

In order to get further insight into the linearity of the fabricated prototype, Fig. 3.19 shows a boxplot diagram of the measured power on the $50\,\Omega$ input of the spectrum analyzer for the first ten harmonic distortion components of the generated sinusoidal signal, across the considered frequency range. It is clear that harmonic distortion components are centered around -50 dBc with respect to the fundamental, barely above the noise floor of the spectrum analyzer. It is also clear that dispersion of the seventh-order harmonic component is larger than the dispersion of other components. This is a consequence of the limited resolution of the DC sources used for calibration, that does not allow us to cancel the seventh harmonic component completely.

Additional insight into the distortion mechanisms limiting the performance of the generator can be gained by analyzing the partial THD and SFDR computed alternatively with the even and odd harmonic components. Thus, in Fig. 3.20.a we show the measured SFDR across the considered frequency range, together with the partial SFDR due to even components, SFDR_{even}, and the partial SFDR due to odd harmonic components, SFDR_{odd}. Equivalently, Fig. 3.20.b shows the THD across the considered frequency range, together with the partial figures THD_{even} and THD_{odd}. It is clear to see that for low frequencies, below 150 MHz, the observed linearity is mainly limited by the odd harmonic components due to incomplete harmonic cancellation because of the limited resolution of the DC sources. For higher output frequencies, timing errors due to circuit imbalances and non-idealities

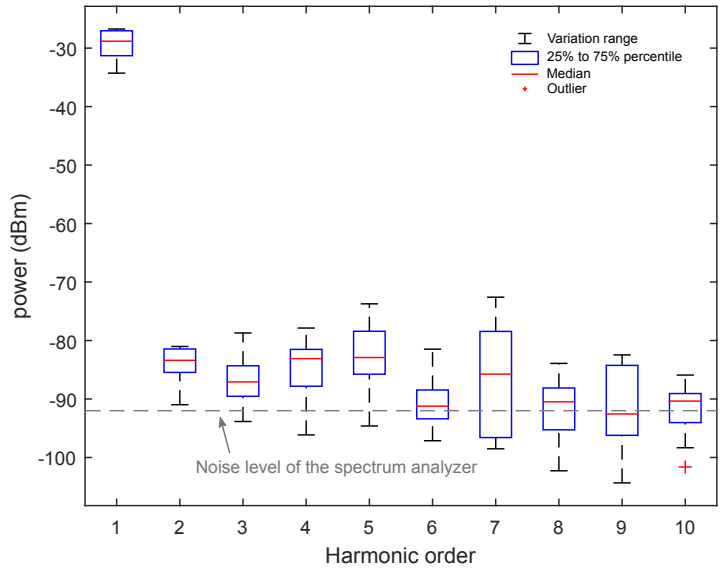


Figure 3.19 – Boxplot of the measured power of the generated output first ten harmonic components, across the considered frequency range.

of the external clock lead to degradation of the 50% duty-cycle of the digital square-waves and may affect also the balance between the differential outputs, both effects leading to even-order harmonic distortion.

3.6 Conclusions

This chapter summarized some of our main contributions to the definition of an efficient on-chip sinusoidal signal generator aimed at analog and mixed-signal BIST. In this line, we have explored different harmonic cancellation strategies that led to a simple mostly-digital architecture for the design of efficient sinusoidal signal generators.

In order to validate the feasibility of the proposed generator, this chapter presented the design, integration and experimental characterization of a proof-of-concept prototype, that has been integrated using STMicroelectronics 28 nm FDSOI technology. This prototype has been characterized in the laboratory and results show that the sinusoidal signal generated by the calibrated generator presents a THD of -46 dB and a SFDR of 52 dB at 166.67 MHz, with an improvement of 10 dB compared to the uncalibrated generator. Experimental results show that the calibrated generator presents fairly constant performances in an operating frequency range from 1 MHz to 333 MHz, with a clock frequency between 20 MHz and 4 GHz. The obtained average of THD is around -45 dB and the average of the SFDR is around 50 dB. Obtained results validate the proposed circuit architecture, while the critical discussion of the observed performance limitations can be used for guiding the design and improving the performance of this family of generators.

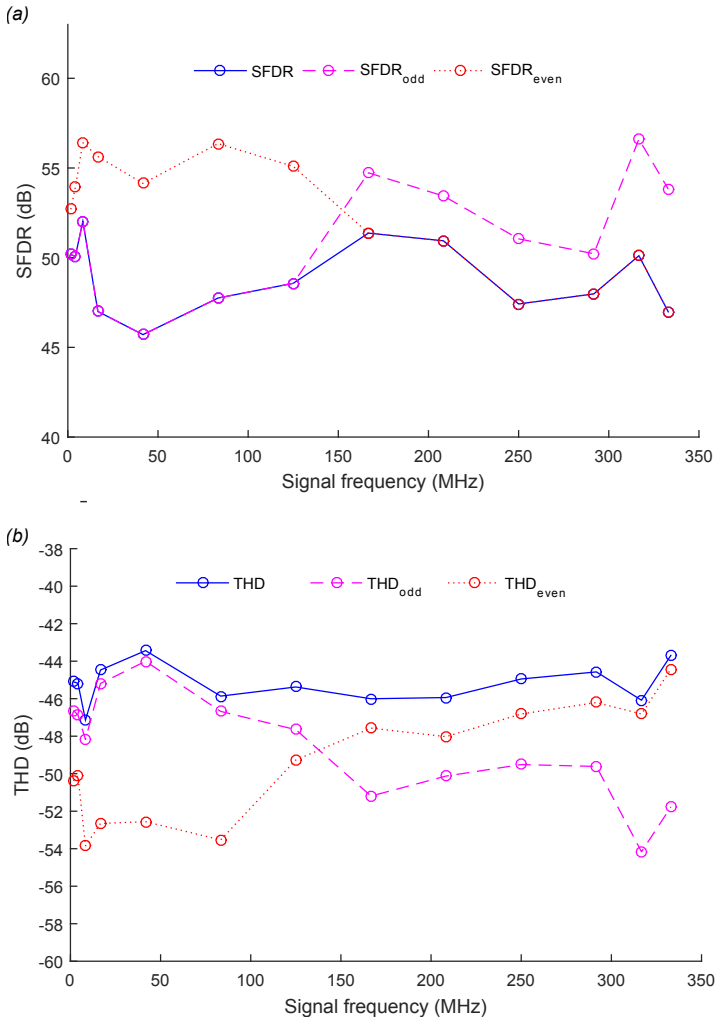


Figure 3.20 – Impact of odd- and even-order harmonics on the: (a) SFDR, and (b) THD of the generated signal.

Chapter 4

Fully-digital BIST wrapper for the dynamic test of $\Sigma\Delta$ ADCs

4.1 Introduction

Current market trends in the IC industry towards the design of highly integrated mixed-signal SoCs and heterogeneous SiPs are supported by the reuse of parametrized Intellectual Property cores (IPs) –either in-house developed or provided by different IP vendors– that implement different analog, mixed-signal, and digital functions within the system. In an ideal scenario, each IP core in the system should include dedicated DfT and/or BIST functionality for enabling and facilitating the test of each individual core. As it was discussed in previous chapters, this is relatively straightforward for digital IP cores. Indeed, a wide variety of broadly proven DfT and BIST strategies for accessing these cores and evaluating their correct functionality are routinely (and often automatically) embedded in every digital IP. On the other hand, complete BIST solutions for analog and mixed-signal IPs are still lacking behind. Certainly, a wide variety of embedded test instruments for mixed-signal BIST applications have been presented over the last years, but complete demonstrations of a fully testable mixed-signal IP with BIST functionalities are seldom found.

In this chapter, I present the design and experimental validation of a complete embedded test solution for a commercial IP. In particular, we proposed a fully-digital test wrapper for the dynamic test of a 40 nm CMOS 18-bit stereo $\Sigma\Delta$ ADC IP core for high-quality audio applications provided by STMicroelectronics. This research was carried out as a TIMA-STMicroelectronics collaboration within the framework of the ELESIS European project (ENIAC joint undertaking). I was the design leader of the complete BIST IP, coordinating the design teams in ST Noida (India), ST Grenoble and TIMA, and in charge of the mixed-signal design tasks. The main results derived from this research were published in a high-impact international journal [63].

Testing the dynamic performance of an ADC in terms of Signal-to-Noise-and-Distortion ratio (SNDR) requires exciting the ADC Under Test (ADCUT) with a high-resolution sinusoidal stimulus –at least two effective bits higher than the resolution of the ADCUT. Moreover, the demand for

high-quality audio devices is driving the improvement in the performance of ΣΔ ADCs toward higher resolutions and dynamic ranges. Therefore, generating the required test stimulus efficiently on-chip for a fully integrated BIST implementation is a very challenging task. The proposed BIST wrapper achieves this objective by relying on the generation of a digital ternary test stimulus that encodes a high-resolution sine-wave. The ternary test stimulus is directly injected into the input of the modulator of the ΣΔ ADC requiring minimal design modifications. The BIST wrapper also includes a test response analyzer for computing the SNDR on-chip and providing a 1-bit go/no-go test response, as well as a control unit for managing the test execution.

In recent years there has been an intense research effort towards developing BIST strategies for ΣΔ ADCs. In [64], an Oscillation-Based BIST (OBIST) strategy for ΣΔ modulators is proposed that consists of reconfiguring the modulator under test into an oscillator. Both the frequency and amplitude of the oscillation are monitored and processed to distinguish faulty from fault-free circuits. This test strategy provides a structural verification of the modulator under test targeting defects. However, the sensitivity to process variations and the need of extensive circuit reconfiguration can deteriorate the quality of this approach.

In [65,66], it is proposed to estimate the magnitude of the leakage in the integrators of the modulator which is directly related to the in-band quantization noise power at the modulator output, thus allowing to estimate the dynamic performance of the modulator. However, as demonstrated in [67], additional tests targeting different modulator parameters (i.e. settling time, amplifier non-linearity, etc.) are required for a complete validation of the modulator performance.

Another idea that has been thoroughly explored in the literature is the use of digital ΣΔ bitstreams. The starting point is to use an ideal ΣΔ modulator in software to convert a high-resolution analog sine-wave to a digital bitstream. The bitstream is truncated to get an optimized sequence that is periodically reproduced using a circular shift-register [14]. Bitstreams can also be generated using on-chip digital oscillators, but their design is not straightforward [68]. The bitstream can be converted to a high-resolution analog sine-wave by passing it through a 1-bit digital-to-analog converter (DAC) followed by a low-pass filter to remove quantization noise. Although this solution is applicable for a built-off test where the 1-bit DAC and the low-pass filter are placed on the load board, it is not applicable for BIST since for high-resolution applications the low-pass filter may be far more complex than the modulator under test [69, 70].

Interestingly, in the case of Switched-Capacitor (SC) ΣΔ ADCs, the bitstream can be fed directly into the modulator by adding simple circuitry at its input [71–73]. A 1-bit DAC –typically a replica of the feedback DAC in the modulator input stage– is used to convert the bitstream to the analog reference voltages of the modulator. However, the direct injection of the bitstream to the input of the ADC will overload the modulator, unless the reference voltages of the 1-bit DAC are adequately attenuated [72]. This attenuation also scales down the amplitude of the encoded sine-wave, which, in effect, will be far below the Full Scale (FS) of the ADCUT. This is a key limitation of this test technique, since for an accurate dynamic test the amplitude of the test stimulus has to be as close as possible to the FS such that the harmonic distortion introduced by the ADCUT is amply manifested [74].

A solution to this problem has been proposed in [75, 76], where the input switched-capacitor network of the ΣΔ modulator is reconfigured in test mode such that it accepts multiple bitstreams delayed

from each other. This technique has been proved to attenuate the noise power of the test stimulus, allowing this way to test the modulator at amplitudes closer to the FS. However, this comes at the cost of significantly increasing the design complexity of the input stage of the modulator.

A simpler solution was proposed by our group at TIMA in [77]. A sinusoidal test stimulus is encoded in a ternary stream that is composed of three logic levels $\{-1,\ 0,\ +1\}$ and injected directly at the input of the modulator of the $\Sigma\Delta$ ADC under test. Intuitively, encoding the test stimulus in a digital ternary stream reduces the quantization noise with respect to the classic binary $\Sigma\Delta$ sequence proposed in previous work and hence should allow us to test closer to the FS. In this project we demonstrated the feasibility of this technique by integrating it together with a $\Sigma\Delta$ IP provided by STMicroelectronics.

4.2 Theoretical basis: ternary test stimulus

Let us consider a ternary stimulus generated in the digital domain by adding a $\Sigma\Delta$ encoded binary bitstream with a delayed version of itself. From a spectral point of view, the Discrete Fourier Transform (DFT) of a length-N bitstream $\{b_0, \cdots, b_{N-1}\}$ is given by

$$B(k) = \sum_{n=0}^{N-1} b_n \cdot e^{-j\frac{2\pi \cdot n}{N}k}, \quad k = 0, \cdots, N-1. \tag{4.1}$$

The N periodic extension leads to a spectrum made by N lines located at $f_k = kf_s/N$, where f_s is the sampling frequency. The DFT of the circular-shifted bitstream delayed by one sample $\{b_1, \cdots, b_{N-1}, b_0\}$ is obtained by applying the time shift theorem to (4.1)

$$B_\delta(k) = B(k) \cdot e^{-j\frac{2\pi}{N}k}, \quad k = 0, \cdots, N-1. \tag{4.2}$$

The DFT of the ternary stream is then obtained by averaging the DFT of the original bitstream and the DFT of the circular-shifted version of it and by using the linearity property of the DFT

$$T(k) = \frac{B(k)}{2}\left(1 + e^{-j\frac{2\pi}{N}k}\right), \quad k = 0, \cdots, N-1. \tag{4.3}$$

The Power Spectral Density (PSD) of the bitstream and the ternary stream are given by

$$\begin{aligned} S_B(k) &= \|B(k)\|^2 \\ S_T(k) &= S_B(k) \cdot cos^2\left(\frac{\pi k}{N}\right) \\ & \quad k = 0, \cdots, N-1, \end{aligned} \tag{4.4}$$

respectively. Therefore the spectrum of the ternary stream presents a lowpass filter behavior that attenuates the shaped quantization noise at high frequencies. In other words, the ternary stream overloads less the modulator compared to the bitstream and, thereby, offers the possibility of testing the $\Sigma\Delta$ ADC closer to full scale.

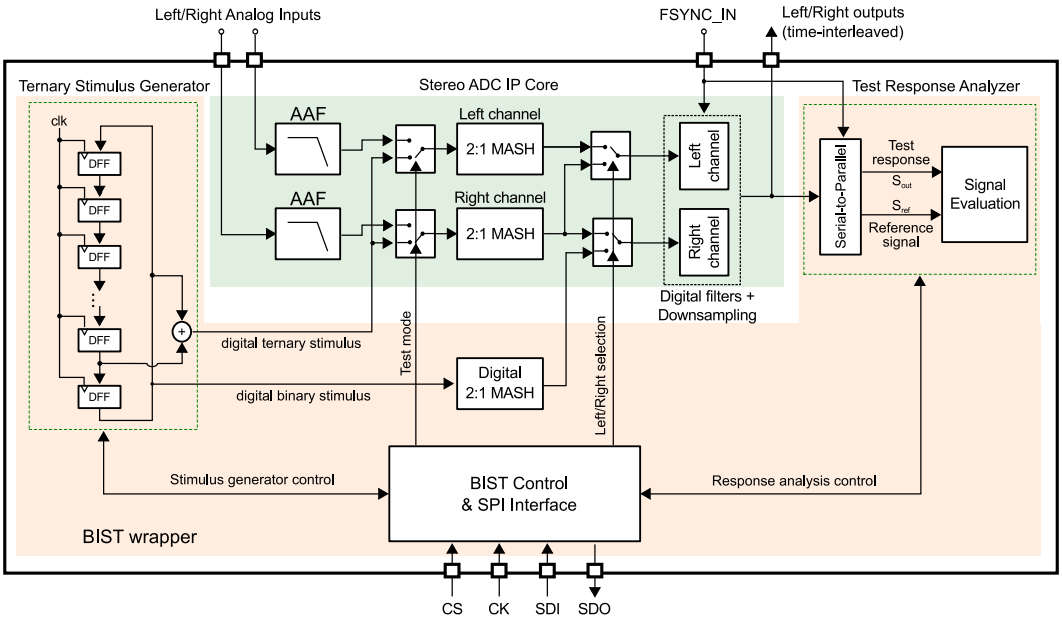


Figure 4.1 – Architecture of the self-testable ΣΔ ADC.

Injecting a ternary stimulus at the input of a ΣΔ modulator does not require a significant reconfiguration of the input stage. Indeed, the ternary stream can be converted to a three-level analog signal and injected directly at the input stage of the modulator. In fact, the implementation is, in essence, equivalent to the case of applying a binary bitstream. The proposed approach presents a minimal overhead and allows measuring SNDR for amplitudes close to FS.

4.3 Design of a self-testable ΣΔ ADC architecture

4.3.1 System level overview

Fig. 4.1 shows a conceptual block diagram of the complete ΣΔ ADC IP core incorporating the BIST wrapper for measuring the SNDR on-chip. In normal operation mode, the analog input signals for Left and Right channels are first filtered by an active-RC second-order low-pass anti-aliasing filter that also provides a single-ended-to-fully-differential signal conversion. A 2:1 MASH SC modulator converts these differential signals to a digital bitstream and a fourth-order digital decimation filter eliminates the shaped high-frequency noise to provide the 18-bit digital output. The IP features a single output port with 18 bits in parallel, where the Left and Right channel outputs are time-interleaved according to the rising and falling edges of a control signal (labelled FSYNC_IN in Fig. 4.1). Relevant performance and design parameters of the ADC IP are summarized in Table 4.1.

In BIST mode, an optimized digital bitstream stored in a circular shift-register is periodically repeated and combined with a delayed version of itself to generate a digital ternary test stimulus en-

Input range	1.4 V
Input bandwidth	24 kHz
Sampling frequency (MASH input)	6.144 MHz
Sampling frequency (ADC output)	48 kHz
Nominal resolution	18 bits
SNDR (typical)	94 dB
Analog power supply	3.3 V
Digital power supply	1.1 V
Power consumption	41.8 mW

Table 4.1 – Summary of performance and design parameters of the ADCUT

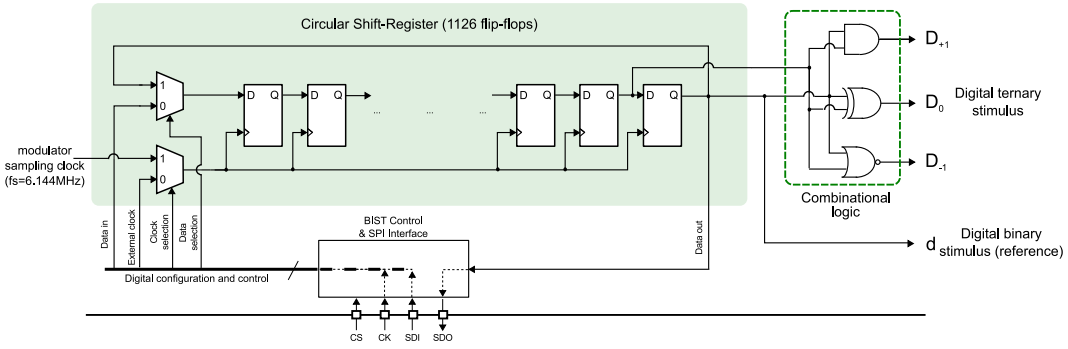


Figure 4.2 – Micro-architecture of the ternary test stimulus generator block.

coding a high-resolution sinusoidal test stimulus within the bandwidth and input dynamic range of the ADCUT. The ternary test stimulus is injected directly at the input of the 2:1 MASH modulator of one of the ADC channels, which has been previously selected and disconnected from the input signal path. The resulting output bitstream is routed to the Left channel of the decimation filter to produce an 18-bit test response signal, labelled S_{out} in Fig. 4.1. At the same time, the original optimized digital bitstream is fed to a fully-digital implementation of the 2:1 MASH modulator. The resulting output bitstream is fed to the Right channel of the decimation filter to produce a high-precision 21-bit digital sine-wave, labelled S_{ref} in Fig. 4.1, that serves as the reference signal. The digital 2:1 MASH assures the synchronization between Right and Left channel output signals, since both the modulator in the channel under test and the digital 2:1 MASH introduce a z^{-3} signal delay. Then, the test output response from the Left channel and the reference signal from the Right channel are extracted from the time-interleaved output of the ADCUT using the synchronization signal FSYNC_IN and fed to the test response analyzer block. This block computes the SNDR of the channel under test from the response and reference signals using a simplified version of the sine-wave fitting algorithm. The obtained SNDR is finally compared to a pre-loaded specification limit and a go/no-go digital signal is generated. The complete test is managed by a BIST control block which also includes a standard Serial-Peripheral Interface (SPI) digital bus for external programming and communication.

The following subsections detail the design and functionality of the main building blocks of the proposed BIST wrapper.

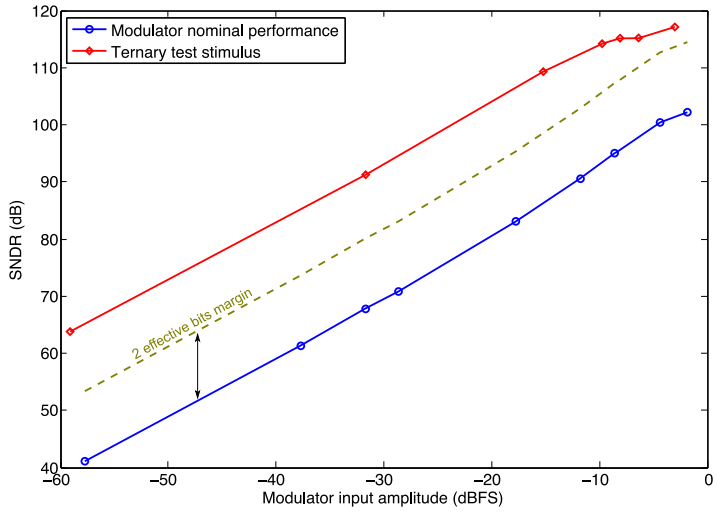


Figure 4.3 – SNDR of the modulator and the optimized ternary test stimulus as a function of the input amplitude.

4.3.2 Ternary stimulus generator

Fig. 4.2 shows a schematic view of the on-chip digital ternary test stimulus generator and its interface signals with the ADCUT, the BIST control, and the digital 2:1 MASH modulator. The core of the ternary test stimulus generator circuitry is a circular shift-register composed of $n = 1126$ flip-flops. During test mode, this circular shift-register stores and reproduces a bitstream that encodes one period of a high-precision sinusoidal test stimulus. The circular shift-register is clocked at the modulator sampling frequency of $f_s = 6.144$ MHz and produces a bitstream with a fundamental tone at $f_{test} = f_s/n = 5.46$ kHz. This frequency is fixed by design and it has been chosen such that the main tone of the test stimulus and the first three harmonic components (i.e. up to the fourth harmonic component) lie within the audio bandwidth of the ADCUT. The bitstream is obtained by simulating in software an ideal ΣΔ modulator excited by a pure sine-wave.

The ternary test stimulus is obtained by adding the bitstream stored in the circular shift-register with a version of the same bitstream delayed by one clock cycle. As previously discussed, this operation has a lowpass filtering effect on the shaped quantization noise at high frequencies and achieves a significant reduction of the total quantization noise power with respect to the original bitstream. The combination of the two bitstreams only requires the addition of three logic gates to generate the three digital signals D_{-1}, D_0, and D_{+1} encoding the three levels of the ternary test stimulus.

Fig. 4.3 plots together the nominal SNDR of the 2:1 MASH modulator in the ADCUT as a function of its input amplitude and the SNDR of the ternary test stimulus as a function of the amplitude of the encoded sine-wave, both measured at $f_{test} = 5.46$ kHz. The amplitude is varied across the complete FS of the modulator. As it can be seen, the encoded ternary stimuli have a SNDR at least 2.5 equivalent bits higher than the SNDR of the modulator, thus respecting the requirement that the test stimulus must have a resolution at least two effective bits higher than the resolution of the ADCUT.

4.3.3 Ternary test stimulus injection

The ternary test stimulus is directly injected into the input of the modulator using a three-level DAC controlled by signals D_{-1}, D_0, and D_{+1}. Fig. 4.4 shows the original schematic of the input switching stage of the 2:1 MASH modulator and the diagram of its clock phases. The 2:1 MASH modulators in the ADC IP core work with two non-overlapped clock phases, denoted by ϕ_1 and ϕ_2 in Fig. 4.4. The input sampling operation is divided into two sub-phases within clock phase ϕ_1. During clock sub-phase ϕ_{1a}, the input capacitors are reset by shorting their nodes to the common-mode voltage. During clock sub-phase ϕ_{1b}, the input capacitors are charged to the input voltages. The digital output bitstreams at the output of the modulator, denoted by *outXYZ*, are fed back to the input of the modulator in clock phase ϕ_2, which is also divided into two steps. In a first step, the feedback signals *out1YZ* are activated, connecting the input node to reference voltages *AGND* or *VHX*. Note that index *Y* makes reference to the signal path –positive or negative– to which the switch is connected, while index *Z* makes reference to the type of transistor. Reference voltages *AGND* and *VHX* offer a fast signal settling at the cost of a low precision. They are used to pre-load the input capacitor to a value close to the ΣΔ ADC references. In a second step, feedback signals *out2YZ* are activated, connecting the input node to the ADC reference voltages *VL* or *VH*. These reference voltages offer a high precision reference value, but signal settling is slower. The division of the modulator feedback operation in these two steps allows relaxing the design of the integrated bandgap reference generator.

Fig. 4.5 shows the modification of the input switching stage for the purpose of injecting the ternary test stimulus. During test mode, control signal T is set to "1" by the BIST control block, turning off the input sampling switches, denoted by *S6* and *S6'* in Fig. 4.5, and, thereby, isolating the modulator under test from the input signal path. At the same time, extra switches *STX* are connected to the input node of the sampling capacitors. This set of switches implements a simple and robust three-level differential DAC that reconstructs the analog sine-wave encoded in the ternary test stimulus $\{D_{-1},\, D_0,\, D_{+1}\}$ and injects it directly into the input sampling capacitors of the modulator under test. As opposed to [72], it is not required to scale down the reference voltages *VH* and *VL*, thus no modifications of the bandgap reference generator and no extra external analog references are needed. States "$+1$" and "-1" in the ternary test stimulus are directly converted to the differential analog levels $VH - VL$ and $VL - VH$, respectively, while the "0" state is implemented by generating a null differential voltage at the input nodes of the sampling capacitors. This is achieved by connecting the input capacitors to the common-mode voltage V_{cm} through switches *ST1* and *ST1'* to discharge them. Alternatively, this null differential voltage could have been produced by activating switches *S1* and *S1'* during clock phase ϕ_{1b}, but this would have required an extensive modification of the internal clock phase generator to avoid overlapping between clock phases ϕ_{1a} and ϕ_{1b} during normal operation. We opted for adding independent switches *ST1* and *ST1'* since it is a simpler option.

The overall overhead for injecting the ternary test stimulus is only the six switches *ST1*, *ST1'*, *ST2*, *ST2'*, *ST3*, and *ST3'* which is equivalent to only four CMOS switches. From a design point of view, switches *ST1* and *ST1'* are an exact replica of switches *S1* and *S1'*, whereas switches *ST2*, *ST3*, *ST2'*, and *ST3'* are an exact replica of switches *S4*, *S5*, *S4'*, and *S5'*, respectively.

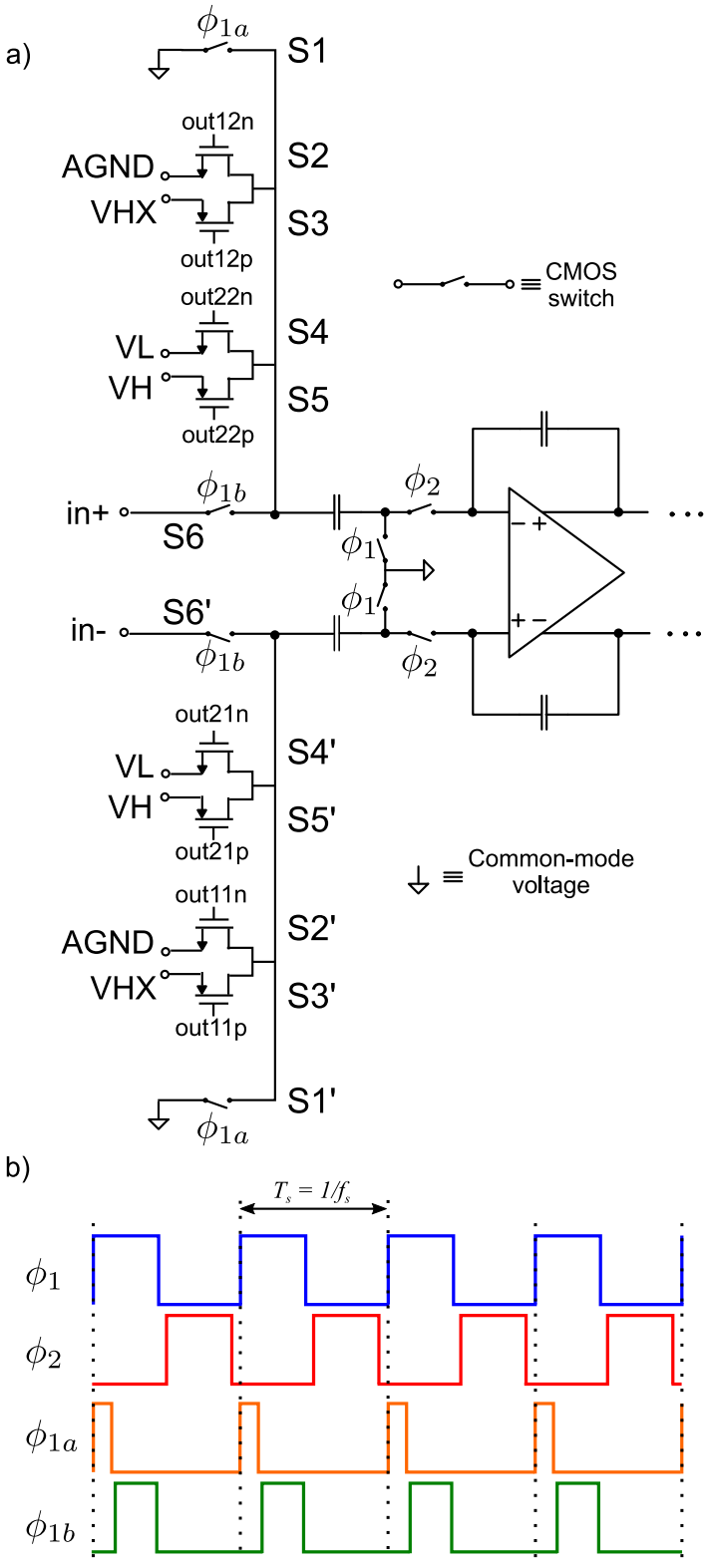


Figure 4.4 – a) Fully-differential input stage of the 2:1 MASH modulators in the ΣΔ ADC IP core; b) Diagram of modulator's clock phases.

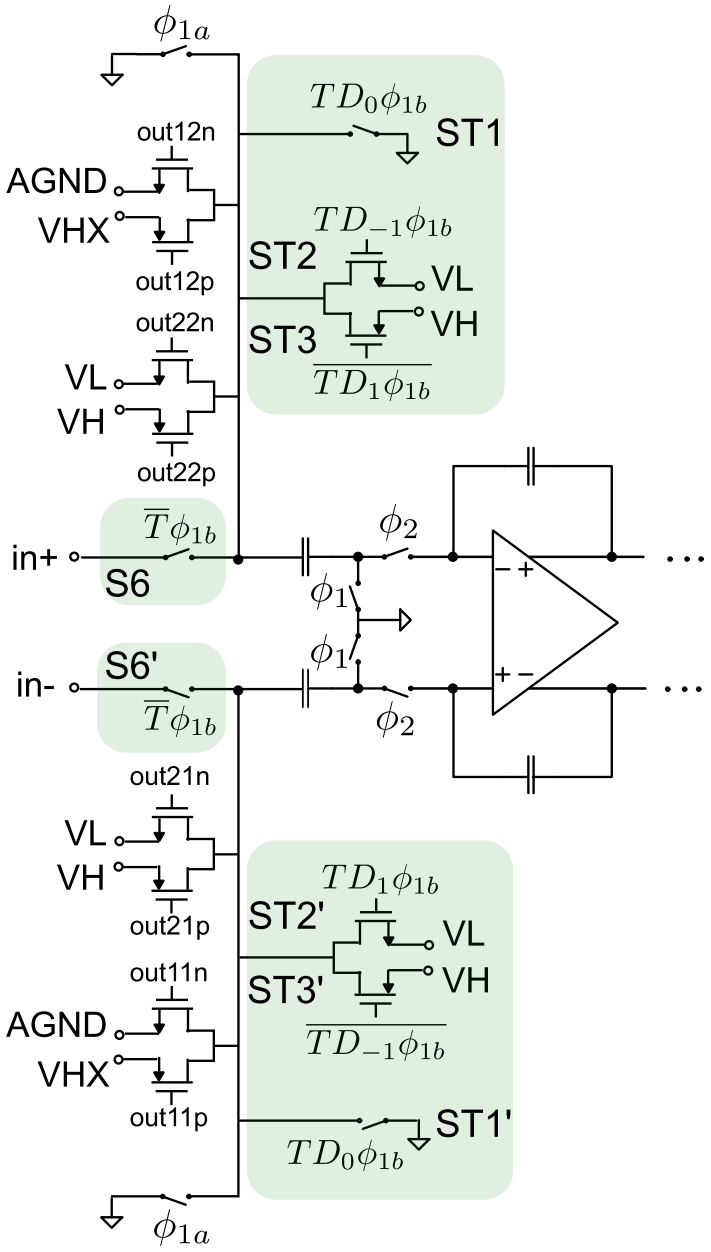


Figure 4.5 – Modification of the fully-differential input stage of the 2:1 MASH for the purpose of injecting the ternary test stimulus. The modifications have been highlighted.

4.3.4 Test response analyzer

The test response evaluation is performed by a version of the sine-wave fitting algorithm [3, 78]. Many efficient implementations of the sine-wave fitting algorithm have been proposed in the literature [72,79,80]. In this work, we implement a simplified version of the sine-wave fitting algorithm that was first introduced in [72]. The classical sine-wave fitting algorithm aims at fitting in a least-square sense a pure sinusoidal reference signal to the output response of the ADCUT. The goal is to determine the DC level, amplitude, frequency, and phase of the fundamental tone in the test response signal. Noise and distortion components can then be easily computed as the residues of the fitted curve. The interested reader is referred to [3, 78] for a detailed analysis of the sine-wave fitting technique. The proposed simplification of the sine-wave fitting algorithm is based on the fact that the test response and reference signals have the same frequency and they are completely synchronized, which saves us from having to compute the phase and frequency of the test response signal. Next, we describe the algorithm for computing the SNDR and making a direct go/no-go test decision on-chip.

Firstly, the algorithm first computes the DC component of the test response signal as

$$DC = \frac{1}{N}\sum_{i=1}^{N} S_{out}(i), \tag{4.5}$$

where $S_{out}(i)$ are the samples of the test response signal at the output channel under test and N is the total number of samples considered in the evaluation. In our implementation, the number of samples is fixed to $N = 563$ which corresponds to 64 signal periods coherently sampled.

In the next step, the algorithm computes the point-to-point correlation of test response and reference signals as

$$Correl = \sum_{i=1}^{N} S_{out}(i)S_{ref}(i), \tag{4.6}$$

where $S_{ref}(i)$ are the samples of the reference signal. The amplitude of the test response signal is related to the computed correlation as

$$A = \frac{2}{NA_{ref}}Correl, \tag{4.7}$$

where A_{ref} is the amplitude of the reference signal encoded in the ternary test stimulus, which is known *a priori*.

Once the amplitude has been computed, the algorithm adjusts the reference signal to the amplitude A and DC values as

$$S_{ref,adj}(i) = \frac{A}{A_{ref}}S_{ref}(i) + DC. \tag{4.8}$$

Finally, the algorithm computes the noise and distortion power in the test response signal, denoted by P_{error}, as

$$P_{error} = \frac{1}{N}\sum_{i=1}^{N}\left(S_{out}(i) - S_{ref,adj}(i)\right)^2. \tag{4.9}$$

The SNDR of the test response signal can be computed as

$$SNDR = 10 \log \frac{A^2/2}{P_{error}}. \tag{4.10}$$

However, to avoid an excessive overhead, the test response analyzer does not compute directly the SNDR value. Instead, it performs a comparison with a preloaded threshold to provide a go/no-go test decision. From (4.10)

$$\text{go/no-go} = \begin{cases} 1, & \text{if } \frac{A^2}{2} \geqslant P_{error} 10^{SNDR_{spec}/10} \\ 0, & \text{if } \frac{A^2}{2} < P_{error} 10^{SNDR_{\text{spec}}/10} \end{cases} \tag{4.11}$$

where $SNDR_{\text{spec}}$ is the SNDR specification of the ADCUT. The threshold value $Threshold = 10^{SNDR_{\text{spec}}/10}$ is a known constant that is loaded into the test response analyzer prior to the evaluation.

The proposed test response analyzer has been implemented with an embedded Arithmetic Logic Unit (ALU) and a Finite-State Machine (FSM) controller, schematically depicted in Fig. 4.6. The ALU has three main blocks –addition, multiplication, and division– together with two blocks for complement operations and one block for comparison operations. The blocks for the complement operations are required to enable subtractions, while the block for comparison is required to compare P_{error} with the preloaded threshold value. The proposed implementation uses Booth's multiplication algorithm to build the multiplier, while the division is actually performed by multiplying by the inverse of the denominator. The FSM controller is programmed to evaluate equations (4.5)-(4.11) sequentially, using only one adder, one multiplier, and one divider. In order to further reduce the area overhead of the test response analyzer, S_{out} and S_{ref} samples are not stored into a memory, but sequentially read from the outputs of the ADCUT and fed to the evaluation algorithm. As a consequence, the evaluation algorithm is executed in two sequential steps: in the first step the algorithm evaluate equations (4.5)-(4.7) over N ADCUT output samples, while in the second step N additional samples are read to evaluate equations (4.8)-(4.11).

The functionality of the test response analyzer is also controlled by the BIST control block through the SPI bus. The reference values A_{ref} and *Threshold* are externally loaded through the SDI port, synchronized to the external clock fed by the CK port. The BIST control block manages the execution of the evaluation algorithm and outputs the go/no-go test decision through the SDO port at the end of the evaluation.

4.3.5 BIST control and SPI interface

The BIST control block manages the test program by supervising the execution of the test and, as it has been described previously, it also interfaces the BIST wrapper with the external ATE through a standard SPI bus. The BIST control block consists of four main units, as shown in Fig. 4.7, namely a SPI Slave port Unit, a Fetch and Execute Unit, a Configuration Unit, and a Reset Unit.

The SPI Slave port Unit has been designed to provide a robust and simple serial interface between the BIST wrapper and the ATE. This standard serial connection allows the ATE to configure the test parameters (i.e. load input stimulus, write configuration registers, etc.) and read out the test results

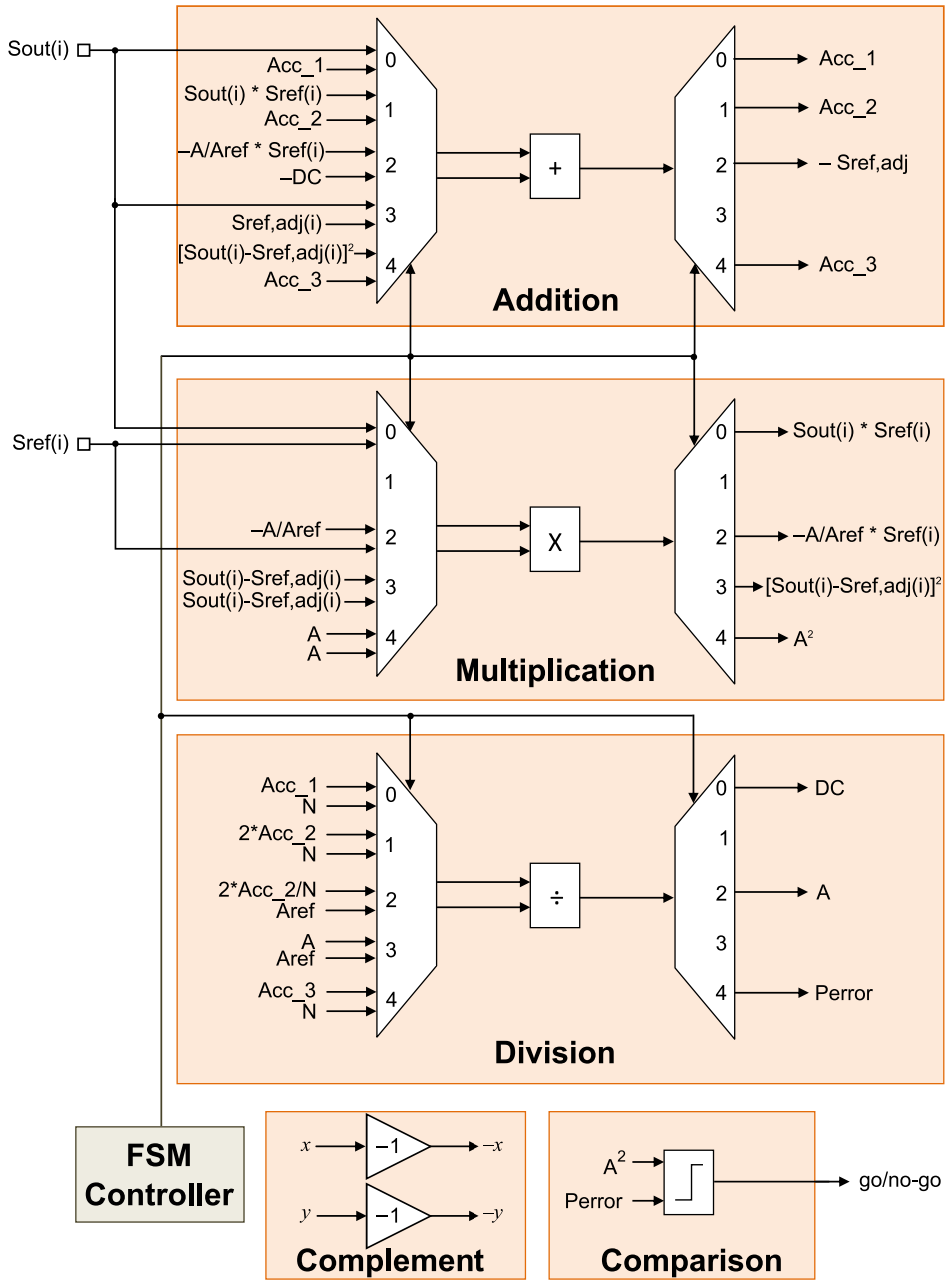


Figure 4.6 – Micro-architecture of the test response analyzer.

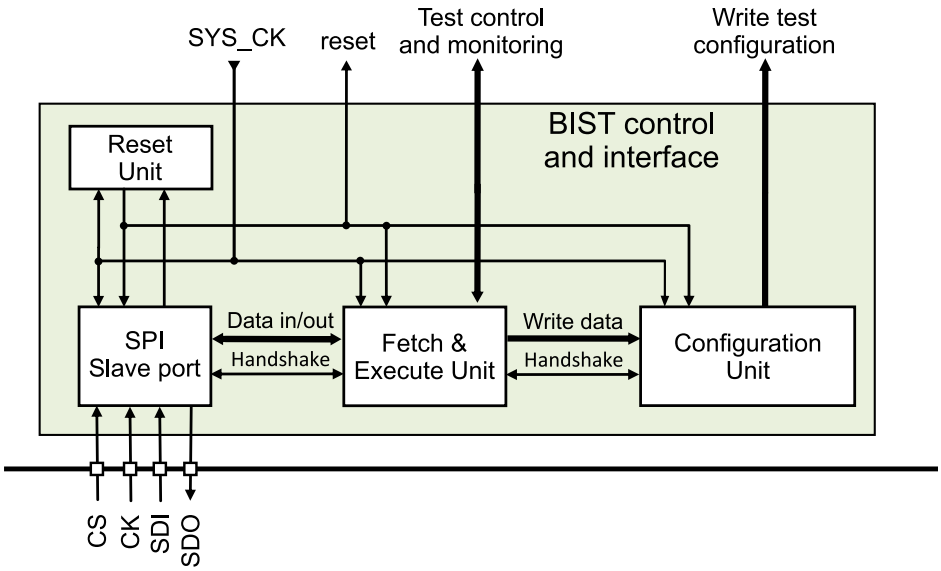


Figure 4.7 – Micro-architecture of the BIST control and SPI interface block.

through the SPI standard ports CS, CK, SDO, and SDI. The SPI Slave port Unit is connected to the Fetch and Execute Unit using a parallel interface which is clocked at the master system clock of the IP, which is denoted by SYS_CK in Fig. 4.7. The SPI Slave port Unit works on two asynchronous clock domains, namely the external clock CK and the master system clock SYS_CK. It has been designed to guarantee a correct data transfer over these two asynchronous clock domains without any data loss or undesired meta-stability behavior.

The Reset Unit initializes all registers in the BIST wrapper. This global reset instruction can be activated directly via the SPI Slave port Unit sending the appropriate command sequence.

The Fetch and Execute Unit has been designed to receive 8-bit command messages from the SPI Slave port Unit, decode them, and execute the corresponding action. It transmits all external configuration data coming from the SPI Slave port Unit to the Configuration Unit. Then, the Configuration Unit loads these data to the appropriate register in the BIST wrapper. The Fetch and Execute Unit also receives the test result data and sends them to the SPI Slave port Unit to be read out through the SPI interface. In addition, it acts as the global test processor of the BIST wrapper and controls the execution of the self-test procedure.

A complete test sequence starts by loading a test configuration through the SPI bus (i.e., the bit-stream in the circular shift-register and the reference values A_{ref} and *Threshold*) and defining the channel under test (i.e., Left or Right). Then, upon receiving the "execute test" command, the BIST control block interrupts the normal operation of the ADCUT by enabling the test mode and the ternary test stimulus is injected into the input of the selected channel. The first 20 periods of the test response are discarded to avoid capturing transient effects, then the following 128 periods are processed by the test response analyzer which compares the SNDR of the test response signal to the preloaded specification value, as detailed previously. Once the self-test has been completed, the BIST control restores

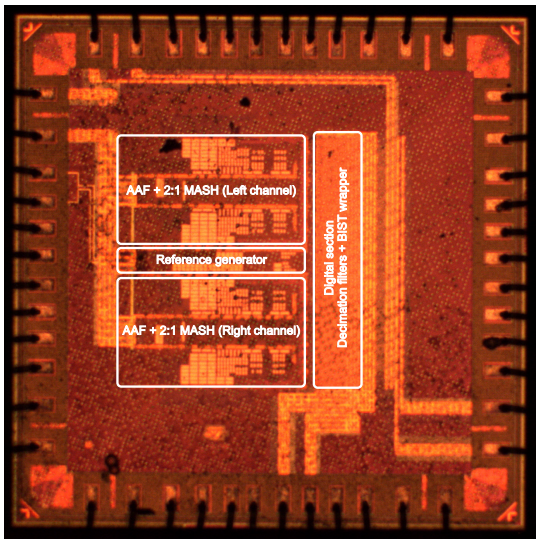


Figure 4.8 – Microphotograph and floorplanning of the fabricated ΣΔ ADC IP with BIST.

normal operation and stores the test results, which can be thereafter read out via the SPI bus upon receiving the appropriate commands. The whole self-test procedure takes 28 ms per ADC channel.

4.4 Experimental results

We redesigned the 40nm CMOS 18-bit stereo audio ΣΔ ADC IP provided by STMicroelectronics to include the complete BIST wrapper. In total, 56 prototype chips were fabricated. Fig. 4.8 shows a microphotograph of one of the fabricated chips. The BIST wrapper incurs an area overhead that is only 7.1% of the area of the ΣΔ ADC. This area overhead is dominated by the test stimulus generator, test response analyzer, and BIST control blocks, which are fully digital blocks. The area of the modulators has not been modified since the extra switches for injecting the ternary test stimulus have been inserted within the existing layout of the modulators. Furthermore, no power consumption overhead is observed during test mode since power consumption is dominated by the analog section of the ΣΔ ADC which is not modified.

In order to provide an experimental validation of the proposed BIST strategy and the functionality of the test instruments within the BIST wrapper, we compare the BIST to the standard functional specification test approach. The BIST is based on a digital ternary test stimulus that encodes a high-resolution analog sine-wave, whereas the standard functional specification test approach is based on applying directly a high-resolution analog sine-wave at the input of the ADCUT.

Our test setup aims at showing the equivalence between the proposed digital ternary test stimulus and the standard functional specification test. Firstly, we employ a conventional workstation as SPI master device for configuring and executing the on-chip BIST program. Then, for comparison, we perform the functional specification test using an Audio Precision Audio Analyzer both for generating

the high-resolution analog sine-wave test stimulus and for computing the SNDR. The procedure is repeated considering seven different input amplitudes, namely, -59.1 dBFS, -31.7 dBFS, -14.6 dBFS, -10.6 dBFS, -8.6 dBFS, -6.4 dBFS, and -3.0 dBFS, and for the 2 channels of all 56 fabricated chips (i.e., 112 ADCs under test in total).

The SNDR values obtained using the BIST circuitry and the standard functional specification test, as well as their comparison, are shown in Fig. 4.9. In the x-axis, we show the amplitude of the signal at the input of the modulator, while in the y-axis we show the measured SNDR values. Fig. 4.9(a) shows the SNDR measured using the functional specification test, Fig. 4.9(b) shows the SNDR measured using the BIST circuitry, and Fig. 4.9(c) shows a superposition of both sets of curves in Fig. 4.9(a) and Fig. 4.9(b) for a direct visual comparison.

By comparing Fig. 4.9(a) and Fig. 4.9(b), for the standard functional specification test set up, we observe that the amplitude of the signal at the input of the modulator is consistently attenuated. This attenuation is clearly visible by looking at the position of the data points on the x-axis. As it can be observed, the circle markers in Fig. 4.9(a) are consistently 2.3 dBFS below the diamond markers in Fig. 4.9(b) when the markers are projected to the x-axis (i.e. modulator input amplitude) for all seven test stimuli considered in our experiment. This constant attenuation of the input amplitude is due to the anti-aliasing filter that is placed before the modulator. It is not apparent when using the digital ternary test stimulus generator because the anti-aliasing filter is disconnected from the signal path and the ternary test stimulus is fed directly into the modulator. In Fig. 4.9(b), the higher spread of the SNDR measurements that appears for input amplitudes close to the FS can be easily explained by the fact that these input amplitudes are in the vicinity of the stability limit of the modulator. In contrast, in Fig. 4.9(a), the SNDR measurements obtained by the functional specification test do not show a similar spread because the input amplitude is attenuated by the anti-aliasing filter and the signal amplitude at the input of the modulator is less than the stability limit. The knee that is apparent in the SNDR measurements in Fig. 4.9(a) is due to the additional distortion introduced by the anti-aliasing filter that essentially limits the SNDR of the ADC in normal operation. From Fig. 4.9(c) it can be seen that the SNDR measurements obtained using the digital ternary test stimulus track very well, along the complete input amplitude range, the SNDR measurements obtained with the standard functional specification test.

Fig. 4.10 shows the histogram of the SNDR estimation error, defined as the difference between the SNDR obtained by the standard functional specification test and by using the on-chip test instruments. The histogram is produced by considering all fabricated chips and by measuring the SNDR in both ways at different input amplitudes, that is, -59.1 dBFS, -31.7 dBFS, -14.6 dBFS, -10.6 dBFS, and -8.6 dBFS. Higher amplitudes close to the FS are excluded since, as explained above, they give rise to other phenomena (e.g., instability of modulators, distortion introduced by the anti-aliasing filter) which are not related to the BIST precision. A good indicator of the average precision of the SNDR measurement using the BIST circuitry is the standard deviation σ of the SNDR error distribution. From Fig. 4.10, we calculate $3\sigma = 1.4$ dB, which is essentially equivalent to the precision of the standard functional specification test performed on dedicated ATE. Therefore, the results demonstrate the equivalence between the proposed BIST circuitry and the functional specification test that employs a high-precision analog sine-wave test stimulus.

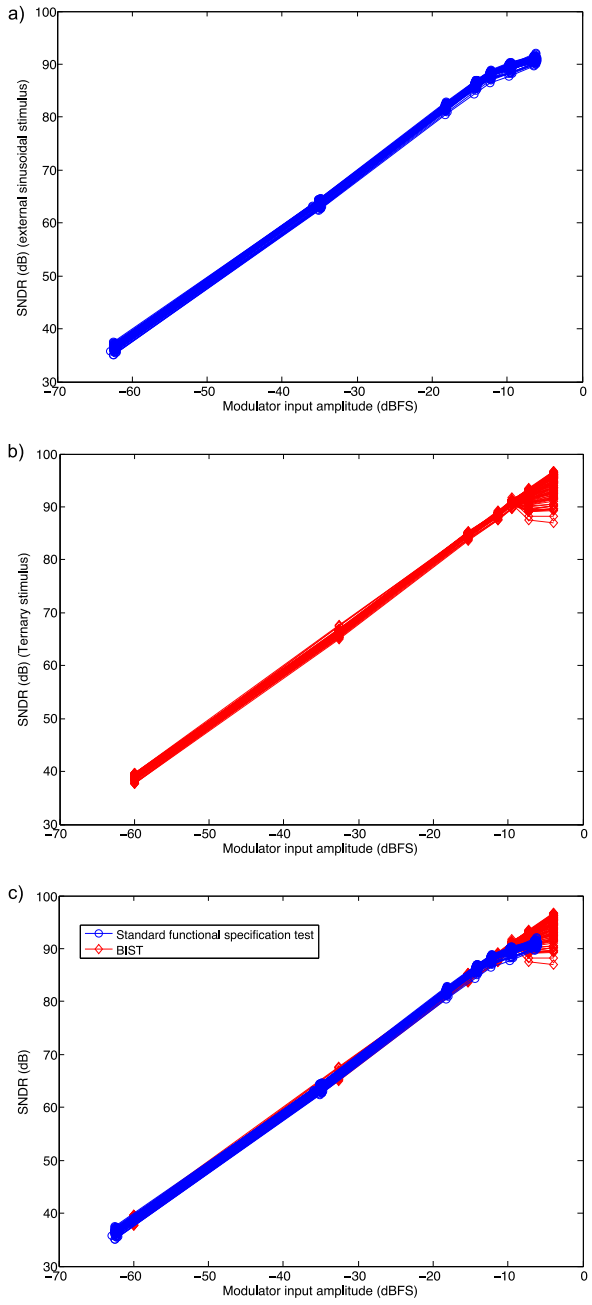


Figure 4.9 – Measured SNDR versus signal amplitude at the input of the modulator for: (a) standard functional specification test and (b) on-chip test instruments. Each curve corresponds to the SNDR of one channel of a fabricated chip (i.e., in total $2 \times 56 = 112$ curves). The curves in (a) and (b) are superimposed in (c) for the purpose of comparison.

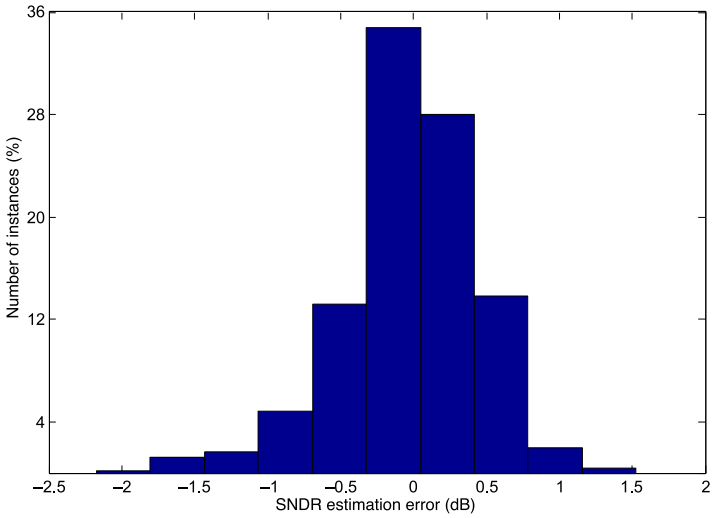


Figure 4.10 – Histogram of SNDR estimation error.

4.5 Conclusions

This chapter presented a 40nm CMOS 18-bit stereo audio $\Sigma\Delta$ ADC that features a fully-digital BIST wrapper for measuring the SNDR on-chip. The proposed BIST is based on injecting a digital ternary test stimulus that encodes a high-precision analog sine-wave directly into the input of the modulator. The test response analysis is also carried out on-chip based on a simplified sine-wave fitting algorithm. The BIST includes a dedicated control block based on a standard SPI bus for switching to test mode, monitoring the test execution, and reading out the test results. The estimated total area overhead of the BIST is 7.1% and the total test time per channel is 28 ms. Experimental results on 56 fabricated chips (112 ADCs under test) prove the feasibility and effectiveness of the proposed BIST approach. Results show an excellent match across the complete dynamic range between SNDR measurements obtained using BIST and standard functional specification test using precision equipment.

Chapter 5

Test quality evaluation for low-cost mixed-signal test techniques

5.1 Introduction

A variety of alternative test paradigms have been proposed to reduce the high cost of direct functional testing of AMS-RF circuits embedded in complex SoCs and SiPs. These techniques include structural defect-oriented test [81], built-in test [82,83], built-off test [84], alternate test [85], statistical learning [86], etc. The aim of any such alternative test technique is to alleviate the ATE requirements, for example, by inferring the test results from simple measurements that are cheaper to perform than functional tests, or by including part of the tester functionality into the DUT itself, or by reducing the test time with adaptive test protocols, etc.

Although it is typically an easy exercise to project test cost savings resulting by employing alternative test techniques, it is not as straightforward to prove that an alternative test technique maintains a test accuracy that is comparable, if not equivalent, to the test accuracy of the standard test technique. Ideally, the test accuracy, typically expressed by the test coverage and yield coverage metrics or, equivalently, by the test escape and yield loss metrics, should be evaluated during the design and test development phases through simulation. This is important so as to be able to adjust, refine, or abandon the alternative test technique at this early stage before moving to high-volume production. Otherwise, it would be needed to apply both the standard and alternative test techniques repeatedly on a high-volume of fabricated circuits, in order to examine how well they correlate. If at this late stage it is concluded that the alternative test technique results in insufficient test accuracy, then significant resources would have been wasted and we could face a significant setback in the test development.

The challenge for evaluating alternative test techniques through simulation is to be able to perform the analysis in a time-efficient manner. Regarding catastrophic defects, the design of the simulation campaign to evaluate the test coverage is straightforward, however, in the case where the number of defects is too high, sophisticated defect sampling techniques must be used [87]. On the other hand, evaluating alternative test techniques against process variations is far more challenging. The reason is

that the specifications are set to 3σ or higher and, thereby, a straightforward Monte Carlo simulation that generates failing instances to evaluate test coverage and marginally functional instances to evaluate yield loss is not a viable option since an intractable number of iterations are required. We use the term *parametric test metrics* to refer to the test coverage and yield loss in the case where only process variations are considered and catastrophic defects are excluded from the analysis. The problem is even more severe for complex (but ubiquitous) mixed-signal devices such $\Sigma\Delta$ ADCs, Phased-Locked Loops (PLLs), RF transceivers, etc, where a single Monte Carlo iteration may be measured in days.

This chapter presents a reliable methodology for speeding up the estimation of parametric test metrics associated to alternative test techniques for these long-to-simulate mixed-signal devices. This research is a continuation of the work presented in the previous chapter. In fact, the proposed test evaluation technique was developed with the goal of assuring to STMicroelectronics that the developed BIST technique is suitable for high-volume production. Similar to the work in the previous chapter, this research was a joint collaboration between TIMA and STMicroelectronics under the framework of the ELESIS European ENIAC project. The main results produced in this research were published in international journals, conferences and a book chapter [88–91].

In recent years, several fast alternatives to Monte Carlo simulation have been published in the literature [92]. In the context of parametric test metrics evaluation, several approaches have been studied, including density estimation [93, 94], Copulas theory [95], extreme value theory [96, 97], importance sampling [98], and generation of parametric fault models [99, 100]. However, all these approaches make the tacit assumption that the circuit can be simulated at transistor-level at least a few hundreds or thousand times. Therefore, they are not applicable for complex mixed-signal circuits with long simulation times.

Approaches applicable to circuits with long simulation times are proposed in [88, 101]. The underlying idea to speed up the analysis is to replace transistor-level simulations with behavioral-level simulations. The behavioral parameters are extracted by following a divide and conquer approach to decompose the circuit into individual blocks that can be simulated independently at transistor-level. In [101], the Monte Carlo analysis is performed at behavioral-level by sampling an estimate of the joint probability density function (PDF) of behavioral parameters to quickly generate millions of "synthetic" circuit instances so as to be able to estimate test metrics with parts-per-million (PPM) using relative frequencies. In [88], a hyper-rectangular in the space of behavioral parameters is defined based on the minimum and maximum values of the behavioral parameters. Thereafter, uniform sampling is performed within this hyper-rectangular to generate "synthetic" faulty and marginally functional circuit instances so as to be able to study the correlation between alternative and standard test techniques beyond the nominal design point. The disadvantage of the approach in [101] is that the PDF is estimated based on centered circuit instances, thus, the tails of the PDF where the faulty and marginally functional circuit instances occur are inaccurately estimated, resulting, in turn, in inaccurate parametric test metrics. The disadvantage of the approach in [88] is that the extracted faulty and marginally functional circuit instances are not necessarily realistic and feasible circuit instances, thus, there is little confidence in the resultant correlation between alternative and standard test techniques.

This chapter describes an efficient methodology that also uses behavioral modeling as a mean to speed up the analysis, yet it builds upon the ideas proposed in [100] to speed up further the analysis so as to be able to generate a realistic and feasible set of faulty and marginally functional circuit instances

based on which the correlation between alternative and standard test techniques can be studied with confidence.

5.2 Theoretical basis

The goal of the proposed approach to parametric test metrics evaluation is to generate, in a time-efficient manner, two sets of circuit instances, namely a set of faulty circuits, which contains a set of circuit instances that fail the specification limit of at least one performance, and a set of marginally functional circuit instances that have at least one performance that lies close to its specification limit. These two sets that comprise extreme circuit instances are used to examine the correlation between the alternative and standard test techniques at the tails of the design distribution where test escape and yield loss events occur.

Our aim is to stick to the Monte Carlo approach, so the results are coherent with the actual process variations in the PDK models provided by the technology. However, this entails several challenges that we have to overcome. To speed up simulation, we first replace the transistor-level design with a behavioral model that captures effectively the circuit functionality, as well as the non-idealities (i.e. noise sources, non-linearity, etc.). For circuits with long simulation times, such a behavioral model is usually available during the design phase and is used repeatedly to guide the design and achieve the best possible performance trade-offs. Thus, the development of the behavioral model does not introduce an extra effort towards our objective.

The next step is to be able to run Monte Carlo simulations at behavioral-level. Our approach is to estimate the joint PDF of behavioral parameters and use it as a behavioral model design kit (BMDK), similar to how the process design kit (PDK) is employed in Monte Carlo transistor-level simulations. To address the scenario where the PDF does not follow a known parametric form (i.e. Gaussian, etc.), we use non-parametric kernel density estimation (KDE) which makes no assumption about the underlying form of the distribution [102].

To estimate the joint PDF of behavioral parameters, we require an initial Monte Carlo sample of behavioral parameters which draws upon the correlations that exist amongst the low-level process parameters, as these are defined in the actual PDK of the technology. Our approach is to run a Monte Carlo simulation at transistor-level and use appropriate test benches to extract the behavioral parameters. For this purpose, taking into consideration that a single transistor-level simulation of the complete circuit may take more than one day to complete, we decompose the circuit into individual simpler blocks that can be simulated independently of each other at transistor-level, much faster than the complete circuit itself. Test benches using one block at a time are designed to extract all the relevant behavioral parameters. The key is to use the same Monte Carlo seed for every test bench such that the same global process parameter vectors are visited in each Monte Carlo run. This ensures that the correlations between the behavioral parameters are captured efficiently.

To perform a Monte Carlo simulation at behavioral level, we use the BMDK to sample a behavioral parameter vector in each run. Although behavioral simulation is considerably faster than transistor-level simulation, it is in the order of minutes and, thereby, it is still not time-efficient enough for the

purpose of evaluating parametric test metrics. To address this challenge, we employ the statistical blockade technique [103, 104]. The underlying idea is to decide whether a circuit instance is extreme before actually running the behavioral simulation since any non-extreme circuit instance is worthless for evaluating parametric test metrics. If a circuit instance is unlikely to be extreme, then the behavioral simulation is blocked and we proceed by sampling a new behavioral parameter vector. The decision block that is introduced into the Monte Carlo loop is fine-tuned in the course of the algorithm so as to increase the confidence on whether to run a behavioral simulation and, thereby, save a maximum of simulation effort.

The proposed algorithm for parametric test metric evaluation can be detailed as follows:

step 1 Build a behavioral model of the circuit.

step 2 Decompose the circuit into individual blocks.

step 3 Build test benches for each individual block for extracting all relevant behavioral parameters.

step 4 Run n Monte Carlo simulations at transistor-level independently for each test bench using the same seed and extract the behavioral parameters.

step 5 Use the sample of n behavioral parameters from step 4 to build the joint PDF of behavioral parameters using non-parametric KDE. This joint PDF serves as the BMDK.

The behavioral model from step 1 and the BMDK from step 5 are the inputs to the main loop of the algorithm that is based on statistical blockade. The algorithm is run separately for each performance of interest. Let us denote a performance of interest by P and let us assume without loss of generality that it has a lower specification limit, denoted by s. Suppose that we target generating a set of faulty circuits of size at least N. As a by-product, the algorithm returns a set of marginally functional circuit instances of size $M > N$.

step 6 Sample the BMDK to generate n' independent behavioral parameter vectors. Set $i = 1$.

step 7.i Run n' behavioral-level simulations using the n' behavioral parameter vectors and compute the performance P in each run.

step 8.i The circuit instances that satisfy $P < s$ are put into the set of faulty circuits while the circuit instances that satisfy $s < P < s + |\epsilon|$ are put into the set of marginally functional circuit instances. If the size of the set of faulty circuits exceeds N, then the algorithm terminates.

step 9.i Consider the ordered sequence of performances from step 7.i, denoted by $P^{(1)} \leq \cdots \leq P^{(j)} \leq \cdots \leq P^{(n')}$, and calculate the q%-quantile as $u_i = P^{(j)}$, where $j = \lceil n'q/100 \rceil$. In other words, $\Pr\{P \leq u_i\} \approx q/100$. We create two sets, namely the set S_{-i} that includes the $\lceil n'q/100 \rceil$ circuit instances that satisfy $P \leq u_i$ and the set S_{+i} that includes the rest $n' - \lceil n'q/100 \rceil$ circuit instances that satisfy $P > u_i$. The set S_{-i} contains the most extreme circuit instances with performance that lies closer to the specification limit.

step 10.i Train a non-linear binary classifier to allocate a boundary b_i that separates the sets S_{-i} and S_{+i} in the space of behavioral parameters.

step 11.i Apply the statistical blockade technique to generate a sample of n' behavioral parameter vectors that is more extreme than the sample used in step 7.i. Specifically, we sample the BMDK sequentially and we examine the footprint of each generated behavioral parameter vector with respect to boundary b_i. Sampling stops when we identify n' behavioral parameter vectors that lie in the area that corresponds to S_{-i}. The underlying idea is that a behavioral parameter that lies in the area that corresponds to S_{+i} more likely will result in a performance that satisfies $P > u_i$ if we were to run a behavioral-level simulation. For this reason, these behavioral parameters are skipped since our objective is to generate circuit instances that satisfy $P < s$ and given that, at least in the first iterations of the algorithm, $s < u_i$. In short, the aim of the statistical blockade is to concentrate the simulation effort in areas of the behavioral parameter space that are more likely to result in extreme circuit instances violating the specification limit and circumvent running a behavioral-level simulation if, with very high probability, the resultant performance will be much higher than the specification limit.

step 12.i Set $i = i + 1$. Go to step 7.i where the behavioral-level simulations use the n' behavioral parameter vectors generated in step 11.i-1.

In successive iterations of the loop, the threshold u_i reduces and the boundary allocated by the classifier in step 10.i moves towards the true boundary that separates the functional from the faulty circuit instances in the space of behavioral parameters. In this way, the sample that is generated in step 11.i is more and more extreme and its geometric mean is approaching gradually the specification limit. After few iterations, the size of the set of faulty circuits reaches N and the algorithm terminates. A set of marginally functional circuit instances of size M is also made available.

The parameters n', q, and ϵ are user-defined. n' should be selected as high as possible given the simulation time budget. For selecting q, there is trade-off between simulation time and how well the area of failing circuit instances is approximated. By setting $q = 50$, we maintain balanced training sets S_{+i} and S_{-i} at each iteration and we populate heavily the area around the boundary that separates them. Therefore, the allocation of the boundary b_i is more accurate and the area of failing circuit instances is well approximated in the end. However, the boundary moves slowly towards the true boundary that separates the functional from the faulty circuit instances in the space of behavioral parameters and, thereby, the algorithm takes more time to terminate. By setting q at a small value, say $q = 10$, the boundary moves faster towards the true boundary and, thereby, the algorithm terminates faster, however, the set S_{+i} may overshadow the set S_{-i}, risking not to approximate equally well the area of failing circuit instances in the end. Finally, ϵ defines the area of marginal functionality. For a large enough and practical value of ϵ, for example, setting ϵ equal to one standard deviation, a circuit instance that fails the specification limit is sampled with lower probability than a marginally functional circuit instance and, thereby, at any time during the course of algorithm, a set of marginally functional circuit instances of size $M > N$ is maintained.

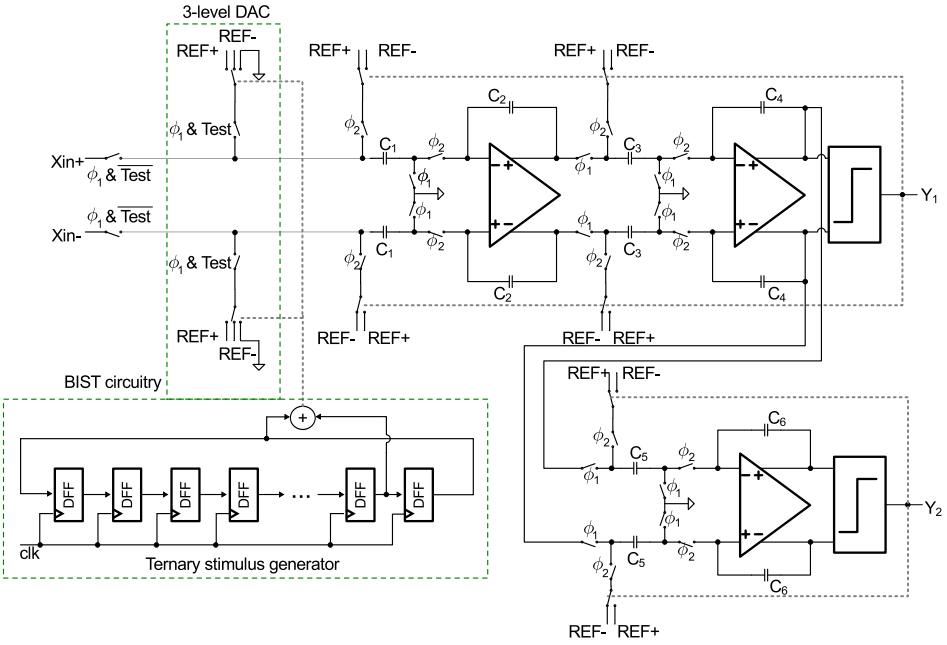


Figure 5.1 – Simplified schematic of the 2:1 MASH modulator including built-in test circuitry.

5.3 Case study

Our case study is the fully-digital, low-cost BIST strategy for measuring the SNDR of $\Sigma\Delta$ ADCs described in the previous chapter. The first step in the proposed algorithm consists in developing a behavioral model of the DUT. As described in the previous chapter, the ADC under test in our case study is a 18-bit $\Sigma\Delta$ ADC designed in a 40nm CMOS technology and provided by STMicroelectronics. Fig. 5.1 shows a simplified schematic of the modulator of the $\Sigma\Delta$ ADC which is a fully-differential 2:1 MASH. Fig. 5.1 includes the circular shift register of the Stimulus Generator and shows how the input stage of the modulator is modified for injecting the ternary test stimulus. The required 3-level DAC has been merged together with the input stage of the modulator simply by adding dedicated input switches [63]. This DAC interfaces the three digital symbols '$+1$', '0', and '-1' in the ternary test stimulus to the three analog differential levels $+V_{ref} = \text{REF}^+ - \text{REF}^-$, 0, and $-V_{ref} = \text{REF}^- - \text{REF}^+$, respectively, in order to retrieve the analog sine-wave encoded in the ternary test stimulus and inject it at the input of the modulator. The decimation filter of the $\Sigma\Delta$ ADC and the Response Analyzer are completely digital blocks and they are not considered in our analysis.

Direct transistor-level simulation of the complete system in Fig. 5.1 takes up very long times. Specifically, a single simulation to obtain the SNDR of the 2:1 MASH modulator for a given input amplitude with an accuracy of 1dB takes more than one day to complete on dedicated simulation servers. To this end, according to steps 1-3 of the proposed evaluation algorithm, we developed a realistic behavioral model following the guidelines provided in [105, 106] and we decomposed the modulator into simpler building blocks that can be efficiently and separately simulated at transistor-level. The

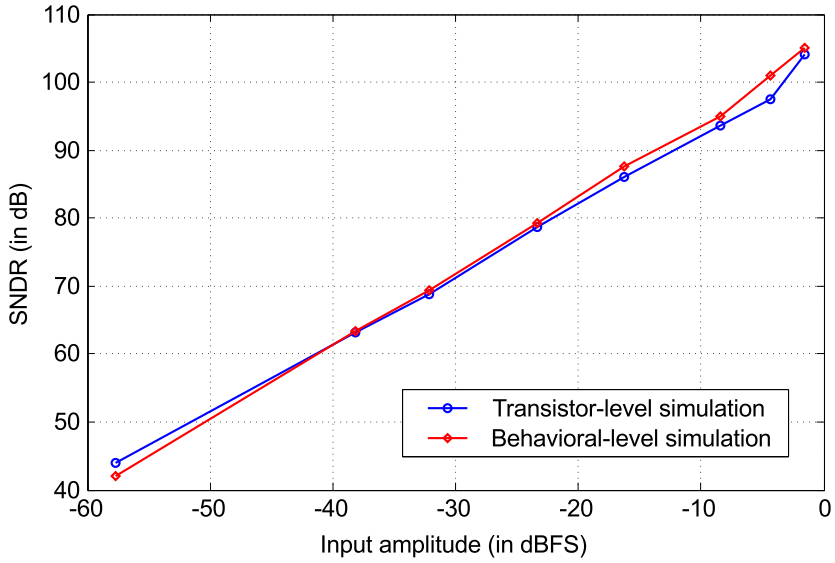


Figure 5.2 – SNDR vs. input amplitude curves obtained by transistor-level and behavioral-level simulation.

main sources of dynamic non-linearity and noise in the modulator that result in SNDR variations are modeled explicitly as behavioral parameters in the behavioral model. In particular, we consider the finite gain-bandwidth product (GBW), limited slew-rate (SR), finite open-loop gain, reference voltage of the modulator, and noise of the amplifier in the first integrator and we set up transistor-level test benches including only the first integrator to extract these behavioral parameters. In addition, we consider jitter noise and kT/C noise. Notice that in behavioral-level Monte Carlo simulations all noise sources are treated as random variables and only the GBW, SR, open-loop gain, and reference voltage of the modulator vary according to their distribution in the BMDK reflecting process variations in the PDK of the technology. The dynamic performance of the modulator is mainly limited by the first integrator, thus, for simplicity, the second and third integrators, as well as the comparators, are modeled as ideal blocks [105,106]. In addition, the behavioral model excludes other non-idealities, such as charge injection, clock feedthrough, capacitor non-linearity, non-linearity of the 3-level DAC, kickback noise from comparators to integrators, etc., since, based on our evaluations, their impact on the dynamic performance is far less significant compared to the aforementioned modeled non-idealities.

Fig. 5.2 shows the SNDR of the complete 2:1 MASH modulator as a function of the input amplitude at the nominal design point using both transistor-level and behavioral-level simulations. As it can be observed, there is a very good agreement between the transistor-level and behavioral-level simulations across the whole amplitude range, demonstrating the accuracy of the behavioral model. Regarding simulation time, it took about one week to run the set of transistor-level simulations, while the set of behavioral-level simulations was completed in about 1.5 minutes.

Referring again to the proposed algorithm for parametric test metric evaluation, in the next step (step 4), we perform $n = 10^3$ transistor-level Monte Carlo simulations for the different test benches, in order to generate $n = 10^3$ behavioral-level circuit instances. These data are used in step 5 to fit a

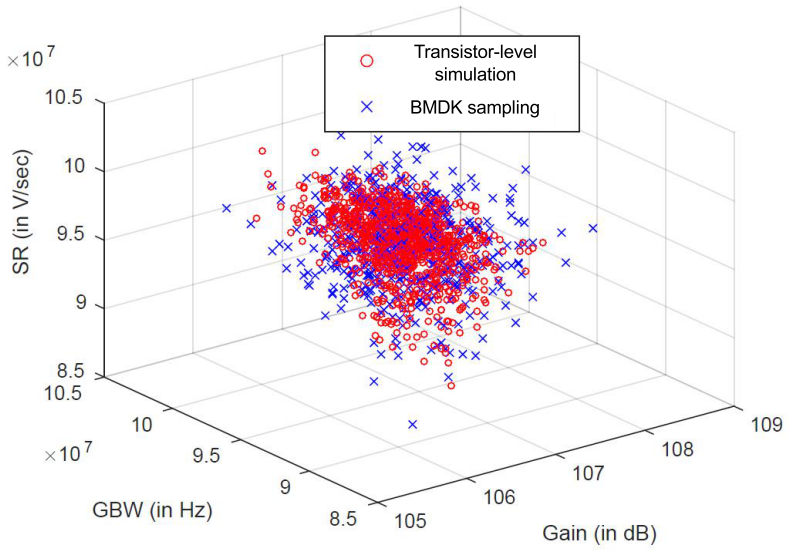


Figure 5.3 – Circuit instances generated through transistor-level simulation and non-parametric density sampling projected onto the space of three behavioral parameters.

non-parametric joint PDF of the behavioral parameters that serves as the BMDK. The BMDK can be sampled very fast to generate new behavioral-level circuit instances. Fig. 5.3 projects circuit instances generated by transistor-level simulation and BMDK sampling onto the space of three behavioral parameters. We excluded from this scatter plot and from the scatter plots that will follow the reference voltage of the modulator since it exhibits the smallest variations and turns out not to be responsible for SNDR failures. As it can be observed from Fig. 5.3, the two populations are practically indistinguishable and, for the purpose of test metrics evaluation, BMDK sampling can replace transistor-level simulation.

For further validation of the proposed behavioral-level Monte Carlo simulation, in Fig. 5.4 we consider the maximum input amplitude and we compare the SNDR histogram obtained by transistor-level Monte Carlo simulation using the technology PDK with the SNDR histogram obtained by behavioral-level Monte Carlo simulation using the developed BMDK. In the case of transistor-level Monte Carlo simulation, it took one month to perform only 21 runs, while in the case of behavioral-level simulation it took only 50 minutes to perform 250 runs. The average SNDR in the case of transistor-level simulations is 104.8 dB with a standard deviation 1.07 dB, while in the case of behavioral-level simulations the average SNDR is 105.7 dB with a standard deviation 1.09 dB. Although the statistical significance of the SNDR histogram obtained by transistor-level Monte Carlo simulation is limited by the low number of runs, which are still very time-consuming and prohibitive to perform in practice, the two SNDR histograms show a good agreement.

Next, we run the statistical blockade loop in steps 6-11, in order to generate the set of extreme circuit instances. The SNDR has a lower specification that is set at 101.2 dB for an input amplitude of -2.3 dBFS, which corresponds to 4σ variation. In this case study, the $\Sigma\Delta$ modulator is clocked at

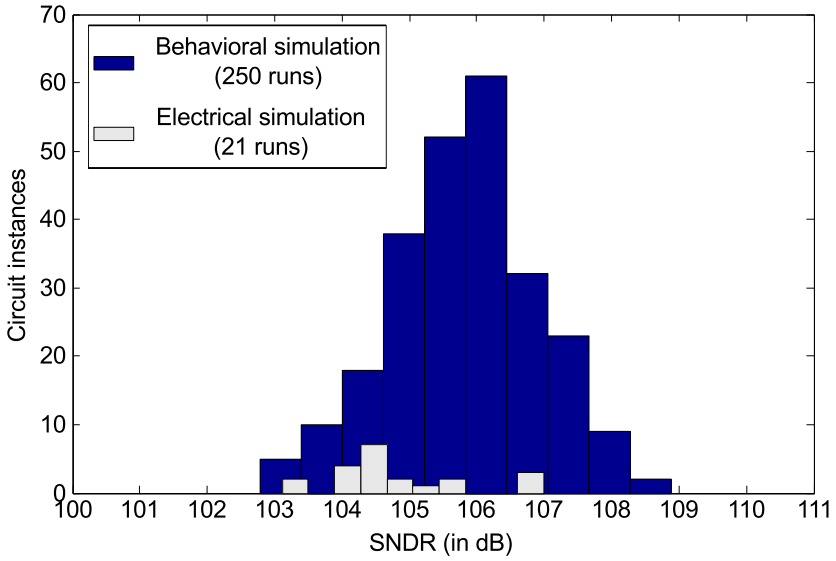


Figure 5.4 – SNDR histograms obtained by transistor-level and behavioral-level Monte Carlo simulations using, respectively, the PDK and the BMDK.

a higher frequency (around $1/4$ times the GBW of the amplifiers in the modulator) than the nominal operation described in the previous chapter. We chose this operating point because it appears to be the most challenging for the BIST strategy. Indeed, it can be proved that due to the different dynamic of ternary and sinusoidal stimuli, in this scenario the SNDR measured with the BIST strategy becomes a signature that is correlated to the actual SNDR [90]. We aim at generating $N = 100$ circuit instances that fail the specification. The margin ϵ is set at 0.8 dB. Finally, we use $q = 10$ and in each iteration of the loop we simulate $n' = 500$ circuit instances.

The loop terminates after four iterations when we have finally generated a set of faulty circuits of size $N = 100$. Fig. 5.5 shows the SNDR values of the samples of circuit instances simulated across the four iterations. Each circle point corresponds to one circuit instance. As it can be observed, in subsequent iterations the SNDR median drops linearly and the number of circuit instances in the set of faulty circuits increases. Fig. 5.6 provides another visual illustration. It shows that in subsequent iterations the SNDR histograms move to the left, closer to the specification limit, and a larger part of the tail of the histograms lies beyond the specification. Fig. 5.6 also shows that the number M of marginally functional circuits that are simulated across the four iterations is, as expected, much larger than N.

Fig. 5.7 projects the circuits instances in the first iteration and the set of faulty circuits onto the space of the same three behavioral parameters plotted in Fig. 5.3. As it can be observed, circuit instances in the set of faulty circuits have a combination of low GBW and low SR. Since the set of faulty circuits is generated in a Monte Carlo sense, we conclude that failures most likely will be due to a combination of low GBW and low SR.

Once the sets of faulty and marginally functional circuits have been obtained by the proposed

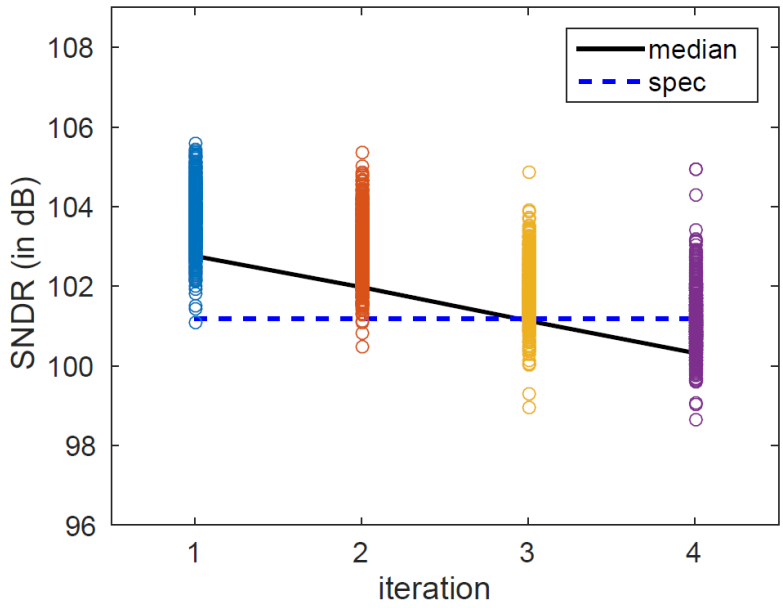


Figure 5.5 – SNDR values of circuit instances simulated in each iteration.

algorithm, the quality of any alternative test can be evaluated by applying the test to the obtained sets of circuits and verifying the agreement with the standard test. In this line, Fig. 5.8 plots the SNDR measurements obtained by the BIST strategy and the standard test technique on the faulty and the marginally functional circuit instances, as well as on the circuit instances in the initial Monte Carlo run, which, by default, are expected to be centered around the nominal design point.

As it can be observed, the two SNDR measurements correlate very well not only around the nominal design point, but, most importantly at the tails of the distribution where test escape and yield loss events may occur. The correlation is slightly non-linear with a knee that lies well into the region of functional circuits. We observe also that some marginally faulty circuit instances are now shown to satisfy the SNDR specification of 101.2dB and, vice versa, some marginally functional circuit instances are now shown to violate the SNDR specification of 101.2dB. These circuit instances correspond to the overlapping area of the faulty and marginally functional populations in Fig. 5.8. Finally, we observe that there is a spread in the points around the correlation curve. The overlapping and the spread are both due to noise in the modulator and the limited number of samples that are used to compute the Fast Fourier Transform (FFT) from which the SNDR is derived. Fig. 5.8 is a strong proof that the BIST strategy achieves high fault coverage and low yield loss and, thereby, we can proceed with implementing it in high-volume production test.

Regarding computation time, it took 50 minutes to run the $n = 10^3$ transistor-level simulations of the individual blocks of the decomposed circuit in step 4, 1 minute to estimate the joint PDF in step 5 and derive the BMDK, a few seconds to sample one behavioral parameter vector from the BMDK in step 6, and less than one 1 minute to run a behavioral-level simulation in step 7i. The majority of

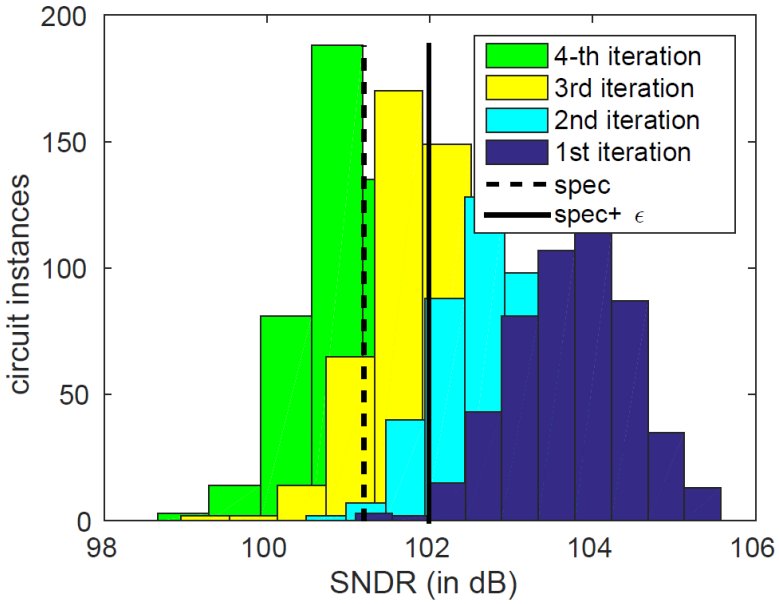


Figure 5.6 – Histograms of circuit instances simulated in each iteration.

the time is consumed for running the behavioral-level simulations in the statistical blockade loop in steps 7i-12i. Overall, it took about 6 hours to produce the data for the plots in Fig. 5.3-5.8, in order to complete the evaluation.

5.4 Conclusions

This chapter presented a generic methodology for evaluating alternative test techniques against the standard test technique. The methodology specifically targets circuits with long transistor-level simulation times that cannot be handled by existing methodologies. It is based on running Monte Carlo simulations at behavioral-level while respecting the joint PDF of process parameters defined in the PDK. The simulation campaign is further accelerated by employing the statistical blockade technique. The output of the methodology is a set of extreme circuit instances that marginally pass or fail the specifications. This set allows to readily study the equivalence of the alternative and standard test techniques far from the nominal design point where test escapes and yield loss events may occur. The methodology was illustrated step by step for the evaluation of a BIST strategy for a 40nm 18-bit $\Sigma\Delta$ ADC.

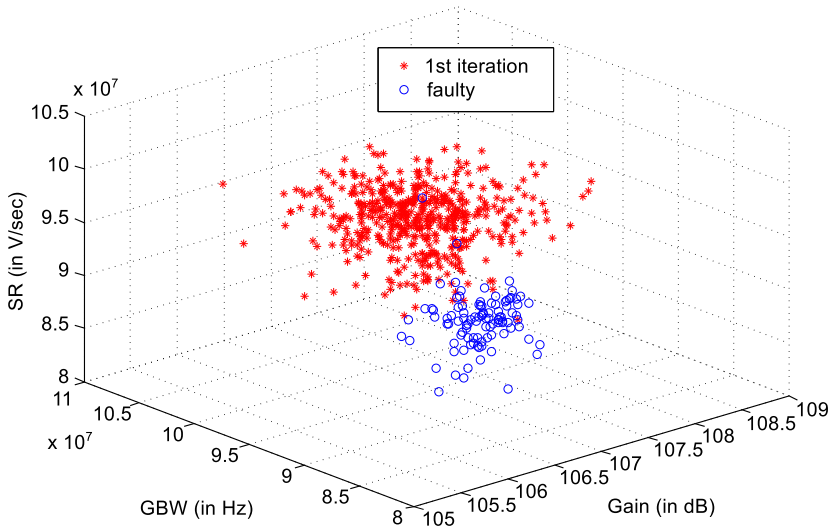


Figure 5.7 – Circuit instances in the first iteration and faulty circuit instances projected onto the space of three behavioral parameters.

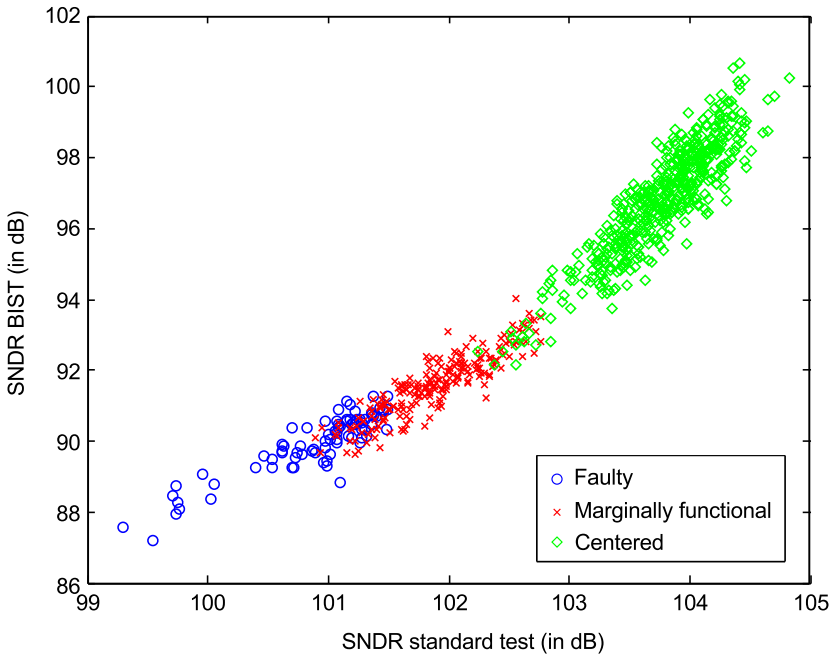


Figure 5.8 – True SNDR value vs. BIST measurement for faulty, marginally functional, and centered circuit instances.

Chapter 6

Feature selection techniques for machine learning indirect test

6.1 Introduction

In the last few years the preeminent position of functional specification test for AMS-RF testing has been challenged. Current market trends in rapidly growing sectors (e.g., automotive, space, healthcare, etc.) put a lot of pressure on quality and reliability. A defect that induces no performance loss at production time may be unacceptable as a potential threat for field operation. The goal is to achieve sub-ppm defect levels and, as a matter of fact, functional tests are not enough for guaranteeing this target defect coverage. Moreover, the *a priori* evaluation of defect coverage for functional test is seldom carried out due to computational power constraints.

In the last decade, a promising alternative to functional test has been proposed based on leveraging the power of advanced machine learning algorithms [107]. The core idea is to build a mapping model from simple measurements, usually called signatures, to the set of functional specifications. The premise of machine learning indirect test is that the simple measurements and the specifications are correlated since their variations are controlled by the same statistical process (i.e., the parametric stochastic variations of the fabrication process). Conceptually this is not different from the linear approach proposed in [108]. However, using modern regression tools greatly extends the validity range of the models.

The benefits of this machine learning indirect test methodology are threefold. First, the outcome of the test can be interpreted in a conventional manner: the estimated specifications are directly compared to their test acceptance windows. Second, the simple measurements are devised to be cheaper than their functional counterparts. And third, these simple measurements can also be tailored to yield a higher defect coverage.

The usual approach to machine learning indirect test is based on supervised machine learning algorithms. The process is developed in two stages: a learning stage, and a testing stage. During the

learning stage both performance parameters and signatures are measured from a set of training devices. A machine learning algorithm is then trained over the two sets of measurements to build a mapping model. In the testing stage, signatures are measured for each DUT, and performances are inferred by using the mapping model obtained in the previous stage. Test result interpretation is the same as in conventional functional test. This is an elegant way to deal with the issue of valid ranges of acceptance, and also gives a valuable insight into reliability since we can estimate how far the circuit is from its nominal specification. In addition, machine learning algorithms are designed to handle complex multi-dimensional and non-linear relations like those between defects and specifications, and by extension, between signatures and specifications.

Machine learning indirect test is a promising test framework. However, it is not free of shortcomings that should be addressed. One of the key issues for the adoption of machine learning indirect test is the definition of an appropriate set of signatures. It is obvious that such a set must capture the major part of the circuit parametric variability but with limited redundancy. In practice, signature sets are proposed based on expert knowledge but are usually suboptimal: they may contain redundant information, noisy signatures, signatures that are actually uncorrelated to the target performances, and even some functional test measurements. The statistic field of feature selection comes at hand to clean up such an *ad hoc* signature set. A variety of feature selection proposals can be found in the literature based on different strategies [109–116].

In this research line, I have analyzed and proposed a variety of feature selection techniques in the context of machine learning indirect test. This research started during my post-doc at the Instituto de Microelectrónica de Sevilla (IMSE-CNM), Sevilla, Spain, under the supervision of Dr. Gildas Léger. After that, I secured the funding for continuing and extending our collaboration with projects CAFE&Test: Causal feature selection for machine learning test of analog, mixed-signal and RF systems (LabEx PERSYVAL-Lab, ANR-11-LABX-0025-01) and IndieTEST: Indirect Test Solutions for Analog, Mixed-Signal and RF Systems (CNRS PICS, project PICS07703). I had the role of project leader for both projects. Scientific results in this research line have been published in international conferences and journals [109, 112, 117–122].

6.2 Theoretical basis: Feature selection

Feature selection can be defined as the process of selecting a subset of relevant features for use in model construction. It is a recurrent problem in machine learning, and has been addressed by numerous researchers in the specialized literature. Interested readers can refer to [123] for an excellent introduction to the topic. In summary, the way to find a solution to the problem of selecting relevant features depends on several parameters:

— The number of features N_{feat}, which determines the size of the search space ($2^{N_{feat}}$)

— The particular regression model: It appears obvious that a linear model may not select the same features as a neural network.

— The number of training samples which limits the number of selected features due to the Curse of Dimensionality: As sample density decreases with dimensionality, it is well known that

regression models fail to properly discriminate between real relevant features and noise.

— The information relevance of the features: The information carried out by a given feature can be relevant or not depending on the presence or absence of other features in the input space.

One important thing to notice is that Statistics literature almost always addresses feature selection from the viewpoint of overfitting and model performance. That is to say: dimensionality reduction is usually the main concern. Indeed, training a model with too many features is detrimental since it ultimately tends to identify noise as relevant patterns. However, in the particular application case of IC testing there is a specific additional concern: each extra feature corresponds to an additional measurement that must be performed in production which increases test time. In the field of test, feature selection has actually been used before the apparition of advanced machine learning algorithms in the field of test compaction [124, 125]. It was early acknowledged that the different specifications of a circuit are likely to be correlated and that it may not be worth measuring all of them. In a generic way, it is thus beneficial to reduce the number of features.

6.2.1 The wrapper approach

The wrapper approach consists in using the machine learning prediction model as a black box within an optimization loop. The model is used to evaluate the prediction error (also called generalization error) for a given feature subset, and the optimization loop tries to minimize this error. An example of wrapper approach applied to test can be found in [126] in the context of classification.

In principle, if the feature space could be exhaustively explored, wrapper approaches should give the most accurate results since the criterion to select or drop a feature is the model error: the same model that will be used to perform the regression in the Alternate Test procedure itself. There are significant pitfalls, though, to the use of wrapper approaches. One of them is that the optimization process itself is a machine learning process. In this sense, it somehow competes with the embedded and implicit optimization loop of model training. The generalization error is evaluated on a test set that is different from the training set. However, if this generalization error is used as the cost function for the feature selection optimizer, the optimizer may end up selecting the features that are most suited for that particular test set. At some point, due to the finite sample size of the set, it would be even possible to fit the data with random noise variables. We thus need an out-of-the-loop criterion to ensure/verify that the model is not overfitting.

Another issue is that many modern machine learning algorithms contemplate some form of embedded dimensionality reduction techniques. These techniques are not equivalent to feature selection: transformations of the input space through kernels, linear combinations of features, regularization penalties etc. They may not drop any feature but combine them to form more predictive ones. Though they are different, these techniques clearly compete with the feature selection optimizer and hence the impact of adding a useless feature may not appear as negatively as it should on the generalization error.

But the most important issue is computational: training a state-of-the-art machine learning model takes time. This time is a complex function of the model type, the number of features (the dimension-

# of features	5	10	20
# of samples	300		
Perceptron	7s	48s	3mn
Nearest Neighbors	8s	18s	28s
MARS	1mn 40s	4mn	9mn 40s
Radial Basis Function	12s	13s	17s
# of samples	1000		
Perceptron	15s	1mn 6s	3mn 15s
Nearest Neighbors	34s	1mn 40s	3mn 7s
MARS	7mn 30s	19mn 40s	47mn 13s
Radial Basis Function	1mn 27s	1mn 50s	2mn
# of samples	10000		
Perceptron	4mn 25s	8mn 20s	16mn 50s
Nearest Neighbors	19mn 15s	1h 32mn	2h 28mn
MARS	1h	2h 10mn	7h 20mn
Radial Basis Function	4h 40mn	12h 55mn	15h 40mn

Table 6.1 – Training time for different model ensembles

ality of the input space) and the number of training samples. To illustrate this fact, Table 6.1 shows the training time for four different models taken from the ENTOOL toolbox [127] (we assume that all models are encoded with the same efficiency): Perceptron Neural Network, Nearest Neighbors, Multivariate Adaptive Regression Splines and Radial Basis Function networks. These models were trained over 300, 1000 and 10000 samples for 5, 10 and 20 input features. It can be seen that the computational burden of training the models scales differently with respect to the dimensionality and the number of samples. In practice, it is clear that exploring a large feature space using wrappers is a computationally expensive task, independently of the regression model used. In what follows, we will consider the use of a perceptron neural network which is a model with a low computational burden, in average, while it maintains a good accuracy.

A particularly simple algorithm for implementing a wrapper consists in a stepwise search, as conceptually depicted in Fig. 6.1. This approach is based on a combination of stepwise forward addition and backward elimination. Starting from an initial subset of features, it explores all the possible children obtained by removing one existing feature or adding one new feature. At each iteration of the search, a number of new models are trained that depends on the already visited states of the search tree, but is approximately equal to the number of features in the search space, N_{feat}.

The choice of the starting point will give different outcomes. If we consider the complete set of available features as the initial set of features, the search will be geared toward backward elimination. This is the case in [128] where the focus is put on test compaction, starting from a known good set of tests that the authors want to reduce. However, in a more generic case where a large space is to be explored, such a backward elimination may lead to an outcome with more features than necessary, due

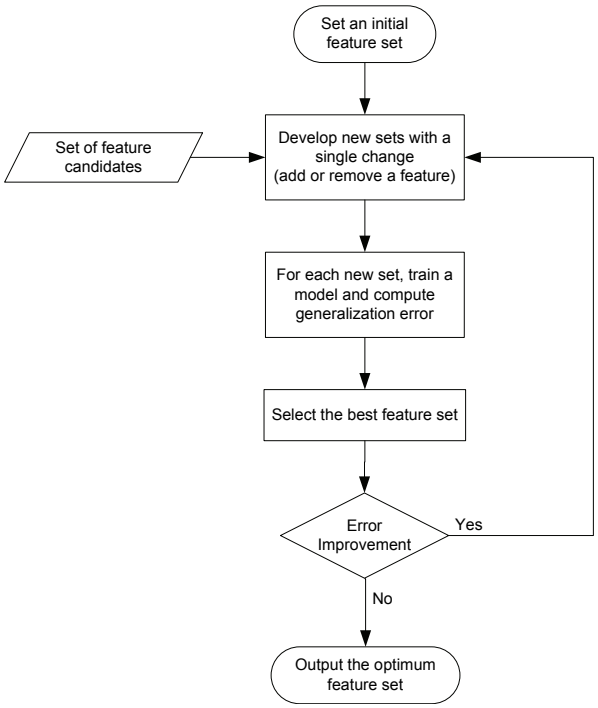


Figure 6.1 – Flow diagram for stepwise search wrapper approach to feature selection

to the embedded regularization mechanisms of the machine learning model itself, as discussed above. Taking a void set as the initial search point gears the search toward forward addition, which should lead to more compact sets. The drawback is that it may be more difficult to select groups of features that are significant together but not individually. Another possibility would consist in performing this search from different random seeds with an arbitrary (but reasonable) number of features. Obviously, the higher the number of seeds, the higher the computational cost. To speed-up the convergence, Kohavi proposed in [129] to consider, at each iteration, the compound operators formed by the best children. In this case, it may be possible to add (or remove) several features in a single step if this provides a better model.

6.2.2 The filtering approach

On the other end of the feature selection spectrum, filtering approaches select adequate features without training any regression model. This is particularly relevant in situations where the number of feature candidates is extremely high. In such cases, they can be viewed as a pre-processing step to wrapper search discarding the less promising features to reduce the cardinality of the search space to a manageable size.

A wide variety of filtering approaches can be found in specialized statistics literature dedicated to dimensionality reduction [130] or feature selection [131]. It is impossible to cover all the methodologies that have been proposed. Instead, in this chapter we will compare different filtering strategies

based on correlation. In addition, we will also comment the use of Principal Component Analysis (PCA) which is not strictly speaking a feature selection method but rather a dimensionality reduction technique. Despite of this, it is a widely-used pre-processing step in machine learning and has actually been applied to machine learning indirect test [115].

Correlation with performance

A straightforward approach to supervised filtering would be to select the features that best correlate to the target specification. However, redundancy is an issue: if two features are almost identical, they could both be selected while only one bring original information.

In [112], it was proposed to use Brownian distance correlation (dCor) instead of Pearson's correlation. The distance correlation statistics is defined in [132]. It is generated as follows: For a random sample $(\mathbf{X}, \mathbf{Y}) = \{(X_k, Y_k) : k = 1, ..., n\}$ of n i.i.d. random vectors (X, Y) from the joint distribution of random vectors X in $\mathbb{R}^p$ and Y in $\mathbb{R}^q$, compute the Euclidian distance matrices $(a_{kl}) = (|X_k - X_l|_p)$ and $(b_{kl}) = (|Y_k - Y_l|_q)$. Define

$$A_{kl} = a_{kl} - \bar{a}_{k\cdot} - \bar{a}_{\cdot l} + \bar{a}_{\cdot\cdot} \qquad k, l = 1, ..., n \tag{6.1}$$

where

$$\bar{a}_{k\cdot} = \frac{1}{n}\sum_{l=1}^{n} a_{kl}, \;\; \bar{a}_{\cdot l} = \frac{1}{n}\sum_{k=1}^{n} a_{kl}, \;\; \bar{a}_{\cdot\cdot} = \frac{1}{n^2}\sum_{k,l=1}^{n} a_{kl} \tag{6.2}$$

Similarly, define $B_{kl} = b_{kl} - \bar{b}_{k\cdot} - \bar{b}_{\cdot l} + \bar{b}_{\cdot\cdot}$ for $k, l = 1, ..., n$. The Brownian distance covariance $\mathcal{V}_n(\mathbf{X}, \mathbf{Y})$ and Brownian distance correlation $\mathcal{R}_n(\mathbf{X}, \mathbf{Y})$ are then given by

$$\mathcal{V}_n^2(\mathbf{X}, \mathbf{Y}) = \frac{1}{n^2}\sum_{k,l=1}^{n} A_{kl}B_{kl} \tag{6.3}$$

and

$$\mathcal{R}_n^2(\mathbf{X}, \mathbf{Y}) = \begin{cases} \frac{\mathcal{V}_n^2(\mathbf{X},\mathbf{Y})}{\sqrt{\mathcal{V}_n^2(\mathbf{X})\mathcal{V}_n^2(\mathbf{Y})}} & \mathcal{V}_n^2(\mathbf{X})\mathcal{V}_n^2(\mathbf{Y}) > 0; \\ 0 & \mathcal{V}_n^2(\mathbf{X})\mathcal{V}_n^2(\mathbf{Y}) = 0 \end{cases} \tag{6.4}$$

respectively, where the variance is given by

$$\mathcal{V}_n^2(\mathbf{X}) = \mathcal{V}_n^2(\mathbf{X}, \mathbf{X}) = \frac{1}{n^2}\sum_{k,l=1}^{n} A_{kl}^2 \tag{6.5}$$

Distance correlation satisfies $0 \leq \mathcal{R} \leq 1$, and $\mathcal{R} = 0$ only if X and Y are independent. In the bivariate normal case, $\mathcal{R}$ is a deterministic function of ρ, and $\mathcal{R}(X, Y) \leq |\rho(X, Y)|$ with equality when $\rho = \pm 1$.

Notice that the computation of Brownian distance correlation is quadratic in the number of samples. This may lead to large computation time on rich training sets. However, if we are looking for global trends –which is implicitly the case since Brownian distance correlation is not local but acts on the complete variation range– it is possible to restrict the computation to a manageable subset of data points.

Compared to classical Pearson's correlation, the main advantage of Brownian distance correlation is its sensitivity to non-linear dependencies. Consider for instance two parameters that are deterministically related: X is a uniform random variable in $[-1;1]$ and Y is expressed as $Y = e^{-10X^2}$. For 1000 random samples, Pearson's correlation is 0.02 and Brownian distance correlation is 0.5. The former leads to think that the variables are uncorrelated while the latter clearly points at a dependency. Another advantage of Brownian distance correlation is that it is multidimensional. The Brownian distance correlation computes the correlation between pair-wise distances of samples in the two matrices under study. In this sense the dimensionality of the two matrices does not need to be the same. We can thus correlate the pair-wise distances between samples in the space of the selected features with the pair-wise distances in the vector of a given performance parameter.

Similarly to Brownian distance correlation, Kendall's Tau or rank correlation is usually used to assess non-linear variable independence and has also been used in the context of Alternate Test [113, 133]. Basically, it tests the hypothesis that for correlated variables, pairwise sample variations should always evolve in the same direction. Hence,

$$\tau = \frac{\sum_{i=1}^{n}\sum_{j=1}^{i}\left[(x_i < x_j \Rightarrow y_i < y_j)\ OR\ (x_i > x_j \Rightarrow y_i > y_j)\right]}{n\left(n-1\right)/2} \tag{6.6}$$

where x and y are the variables and n is the number of samples. The logical expression in the numerator takes the value 1 if true and -1 if false. It can be seen that the philosophy is similar to Brownian distance correlation. However, the strength of the pairwise variations is not taken into account in Kendall's Tau which suggest a lower sensitivity. In addition, comparison between multidimensional spaces is not contemplated.

For Pearson's correlation and Kendall's Tau, features are independently ranked, one by one, as a function of their correlation to the performance. However, the multi-dimensional nature of Brownian distance correlation allow us to consider an iterative search increasing the dimensionality of the input space. We can first select the feature that has the best univariate Brownian distance correlation with the performance. This feature is thus included in the input space. At the second iteration we compute the multivariate Brownian distance correlation between the performance and the two-dimensional input spaces formed by the first feature and the remaining candidate features, and the process can be iterated until the input space is populated.

Principal Component Analysis

The filtering techniques described above are supervised ones, in the sense that they make use of the target parameter (the performance) to select the features. On the other hand, Principal Component

Analysis (PCA) is an unsupervised technique, that is, it acts only on the feature space. When considering the full candidate feature space, in most cases all the features are not independent. If we could plot the samples on this multidimensional space, it may result that the cloud of point lays on a manifold of lower dimension. The goal of PCA is to determine this reduced manifold, supposing that it is linear in the feature space. In other words, it identifies the directions in the full candidate feature space that best explain the variation observed in the data. To do so, it performs an eigenvalue decomposition of the features covariance matrix. The Principal Components (PCs) are the eigenvectors that correspond to the largest eigenvalues.

While PCA may effectively reduce the dimensionality of the problem and solve the computational issue of model training, it does not necessarily reduce the number of features to be acquired. The eigenvectors that form the principal components are linear combinations of the original features. It may happen (and it usually does) that the first few principal components require the complete set of features for their computations. Besides this practical test cost aspect, one of the of the main conceptual drawbacks of PCA is the fact that it is a linear method, while the relation between features may be non-linear.

6.2.3 Proposed approach: Brownian distance correlation-Directed Search

Filtering approaches are extremely fast but with low accuracy while wrapper approaches are slow but accurate. In order to get the best of both worlds, we propose the following directed search:

Algorithm 1 Feature selection using a Brownian distance correlation-Directed Search

```
Compute the correlation of all the features with the performance and add the best feature to the input space
while continue do
    Train a model mapping the input space onto the performance
    Compute the residues of the model
    Compute the mean square of the residues (the mean square error)
    if The mean square error is equal or higher than for previous step then
        continue ← 0
    else
        continue ← 1
        Compute the correlation of the remaining features with the residue
        Add the best feature to the input space
    end if
end while
return The input space (the feature list) and the mean square error
```

The idea behind this algorithm is the same as projection pursuit: a given feature may explain the coarse behavior of the specification but fine details look like noise with respect to the main contribution. However, instead of subtracting the projection of the selected feature from the performance measurement, which would work fine only for a linear problem, we rather train a model and compute

the residues (i.e., subtracting the model prediction from the actual values). The residues thus contain the non-modeled information. The next step of the algorithm (step 10 in algorithm 1) computes the distance correlation of the remaining feature candidates with the residues and selects the most correlated as the next feature to be included in the search space.

This procedure acknowledges the essentially non-linear and multivariate relation between the feature space and the performance measurement. In that way, the next selected feature should always bring additional information. Redundant features should never be selected because their effects are already modeled and cannot be present in the residues.

A key point of the algorithm above is the concept of correlation. We propose to use multivariate Brownian distance correlation instead of conventional correlation metrics such as Pearson's correlation. If we were to use Pearson's correlation, we would be implicitly considering a linear problem. Assuming linear conditions is a huge restriction that may lead to incorrect feature selection decisions. The introduction of Brownian distance correlation, on the other hand, allows us to handle multivariate non-linear dependencies in order to direct the search of relevant features. The correlation is actually computed between the augmented input space –i.e., the matrix of previously selected features plus the feature candidate– and the vector of residues.

6.3 Experimental validation

In order to validate the performance and feasibility of the proposed feature selection technique, in this section we analyze its application to a 2.4 GHz Low Noise Amplifier (LNA) case study. LNAs are simple circuits with very few components but that are quite sensitive to process variability. Figure 6.2 shows the schematic of the LNA, which has been designed in a 90nm CMOS technology. The envelope detector at the output of the LNA has been included as a built-in test instrument [42]. This detector was intended to analytically retrieve specification information but can also be used in a machine learning indirect test framework, as demonstrated in [42].

Our initial set of candidates in this case study contains the following features features: the DC voltages in all the nodes of the LNA, the biasing current, and the output of the envelope detector. Additionally, all the previous features were measured under nominal power supply and also with supply stress (below nominal supply) since it was shown that this change in the operating conditions could bring additional information on the circuit. In total, our initial set of features contains 42 signatures. A population of 2000 instances of the RF LNA was generated using Monte Carlo simulation of the technology process parameters as stated in the design kit and 500 of them were set aside to form the validation set. The 42 identified features as well as the small signal gain of the LNA were extracted for each instance.

In this validation, we use a perceptron neural-network in MATLAB as the machine learning model to predict the small signal gain of the LNA under test. The available data is split between a training set and a validation set. As their names indicate, the training set is used to train the machine learning model while the validation set is set appart from the training and is used to check the predicting power of the model on unknown samples.

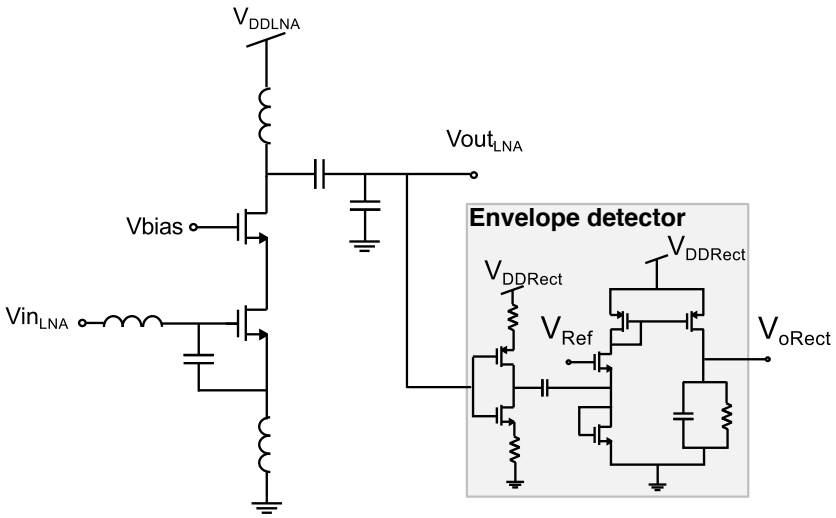


Figure 6.2 – Schematic view of the LNA with envelope detector

The available data in the training set is split in 15 random fractions and 15 different models realizations are obtained by leaving one of the 15 fractions out of the actual training data. This left-out fraction is used as a test set to estimate the generalization error, in a classical cross-validation fashion. At the end of this process, an ensemble model is created: the 9 best performing models are selected and their outcome is averaged to get the ensemble model output. One advantage of this scheme is that the training set data is randomly shuffled at each training iteration, which reduces the risk of overfitting during feature selection.

Notice that the validation set that is kept apart is not involved by any means in model training or feature selection algorithms. It is exclusively used to monitor the evolution of the generalization error in an independent manner. Indeed, it is a common procedural error to apply the feature selection criterion on the validation set. This is not a problem for filtering approaches since the list of candidates is sorted *a-priori* . But for wrapper approaches, the chosen optimizer always ends up optimizing the generalization error for that particular validation set, leading to overfitting. Unless otherwise stated, all the results in what follows are referred to this validation set and any improvement in the generalization error can be guaranteed to be due to feature information.

6.3.1 Comparison of filtering methods

In order to validate our approach, we first explore different filtering approaches. For a direct comparison, the initial set of 42 features has been ranked according to:

— Pearson's Correlation to the LNA gain

— Kendall's Tau

— Univariate Brownian distance correlation to the LNA gain

— Multivariate Brownian distance correlation to the LNA gain

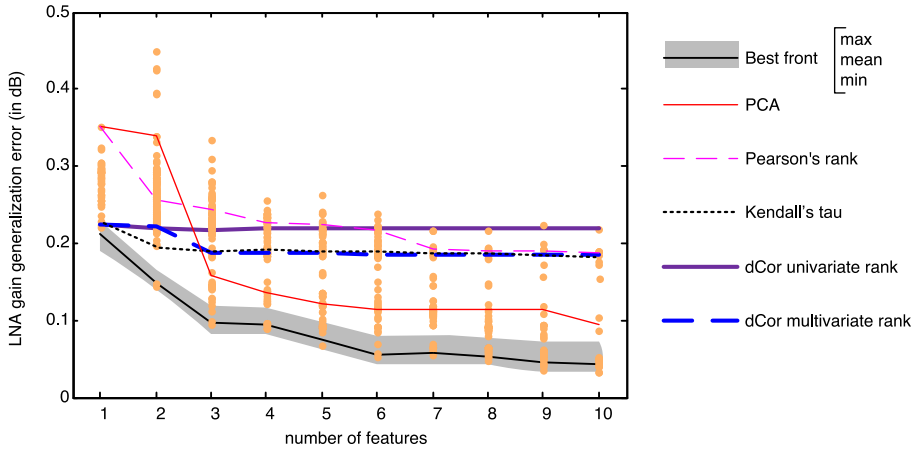


Figure 6.3 – Generalization error for the prediction of LNA gain: Fronts obtained from different feature filtering methods and scatterplot of the explored space through wrapper search.

# of PCs (n)	1	2	3	4	5	6	7
Variability (in %)	75.6	96.9	99.0	99.82	99.93	99.98	99.99

Table 6.2 – Amount of variability concentrated in the first Principal Components

— Principal Component Analysis. Notice that in this case, all the features are actually used to compute the principal components.

Figure 6.3 displays the obtained results –the different fronts up to a dimension of 10– together with the scatterplot obtained by wrapper search, to give an idea of the search space. Error values are computed on the verification set. For comparison purposes, in the following we will consider the stepwise wrapper search as the reference in terms of accuracy and the produced fronts will be considered as the optimum fronts. After identifying the best front from the wrapper search, we have repeated model training 30 times considering random data splits between training and validation sets. We thus obtain, for each point of the front, 30 different generalization errors from which we can extract an estimate of the confidence interval. The interval between the minimum and maximum error of the optimum front is depicted as a gray zone on the figure.

For correlation-based feature ranking, it appears that Kendall's Tau and Brownian distance correlation (both univariate and multivariate) accurately select the best first feature but fail to correctly identify the best additional features. Unsurprisingly, Pearson's correlation even fails to identify the best first feature, possibly due to non-linearity.

The case of PCA is worth some dedicated comments. As it was discussed in Section 2.2.3, PCA is not a feature selection method but rather a dimensionality reduction technique. In this case, the X-axis legend in Fig. 6.3 must be understood as the dimensionality of the input space. That is, in the case of PCA it is the number of principal components (all of which are actually linear combinations of all the existing features).

The principal components are designed to concentrate most of the variability information. Table 6.2 shows the percentage of the total input space variability explained by the first n principal components. This is computed as the sum of the first n eigenvalues of the input space covariance matrix over the total sum of eigenvalues. It can be seen that, in theory, the first principal component (i.e., the first eigenvector) concentrates more than 75% of the variability and the first two more than 96%. Hence, it should be reasonable to expect that a model trained with the first few principal components should outperform any model trained with a few genuine features because these few principal components contain the major part of the variability information. However, it can be seen in Fig. 6.3 that models trained with a few (up to 10) PCs are actually worse than the models trained with the best subset of genuine features. Models trained with the first or the first two PCs are even worse than the those produced by the considered filtering methods. For a dimensionality above 3, PCA-based models never reach the optimum front. This is probably due to the fact that PCA implicitly considers that the correlations between features can be explained by linear relationships, which is clearly not the case for the considered application.

6.3.2 Directed search with different correlation metrics

As described above, the underlying principle of the proposed directed search approach consists in subtracting the contribution of the already selected features from the performance and select the features that best correlate with the generated residues. In this subsection we compare the proposed algorithm based on the multivariate Brownian distance correlation to three variants that use Pearson's correlation, Kendall's tau and univariate Brownian distance correlation, respectively.

Figure 6.4 shows the obtained fronts for our RF LNA case study. As expected, the version that uses Pearson's correlation performs much worse than the proposed technique. More surprisingly, the version of the directed search based on Kendall's Tau also performs poorly. It manages to identify the first best feature but fails to find the best correlation with residues in further iterations. This is probably because Kendall's tau is more an independence test than a tool to measure the strength of the interactions between two variables. The version with univariate Brownian distance correlation works well initially but appears to saturate for models that use more than 3 features.

Noticeably, the proposed approach based on the multivariate Brownian distance correlation performs extremely well compared with the optimum wrapper approach. Indeed, the obtained front is very close to the repeatability range of the optimum wrapper front. In terms of computation time, the proposed Brownian distance directed search offers a significant advantage with respect to the wrapper search. Each iteration of the directed search adds a significant feature and requires to train a single regression model. The wrapper search, on the other hand, explores the complete feature space blindly, just guided by an optimization loop, and a regression model is trained for each of the feature sets visited during the search.

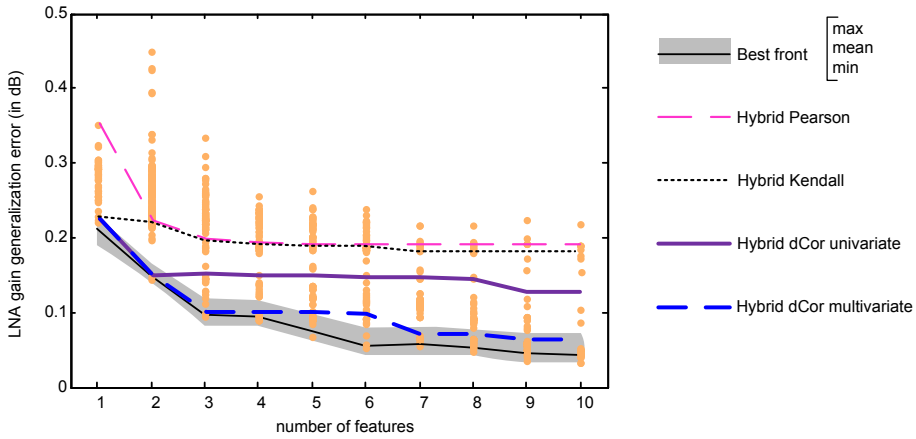


Figure 6.4 – Generalization error for the prediction of LNA gain: Fronts obtained for correlation-directed search with different correlations and scatterplot of the explored space through wrapper approach

6.4 Conclusions

This chapter describes a computationally efficient method for feature selection based on a correlation-directed search approach. Relying on multivariate Brownian distance correlation, which compute the correlation between pairwise distances in the input space (the feature space) and the output space (the performance space), each iteration of the search algorithm selects the feature that best correlates to the residues of the previous fit.

The proposed algorithm has been validated for an RF LNA case study. Obtained results show that the proposed Brownian distance correlation-directed search outperforms the best reviewed filtering methods and provides models that are close to the optimum fronts obtained by wrapper search at a fraction of the computational cost. It is thus a reliable candidate for efficient feature selection that can be used to quickly identify appropriate features sets to perform machine learning indirect test at a reduced computational cost.

Chapter 7

Feature design and machine learning indirect test automation

7.1 Introduction

As it was extensively discussed in the previous chapter, one of the key issues that currently limits the adoption of machine learning indirect test is the lack of a reliable methodology for defining the input space of signatures for an accurate test. The current approach for designing signatures is mostly *ad hoc* and heavily relies on the expertise of the designer. Some generic approaches exist for providing an initial set of signatures, such as DC node probing, I_{DDQ} test, V-transform coefficients [134], process monitoring [135], etc. Work has been also presented on optimizing a particular stimulus to define optimized signatures that minimize the prediction error [136–138], but the choice and the parametrization of the input stimulus are still *ad hoc*.

This chapter describes methodologies to move beyond a feature selection framework, i.e., selecting the best features among a set of pre-defined candidates, towards a feature design strategy, aimed at designing new features that cover relevant information, and even automating the design of the initial set of features itself. As it was the case for the previous chapter, this research started during my post-doc at the Instituto de Microelectrónica de Sevilla (IMSE-CNM), Sevilla, Spain, under the supervision of Dr. Gildas Léger, and continued with my two international collaboration projects CAFE&Test (LabEx PERSYVAL-Lab, ANR-11-LABX-0025-01) and IndieTEST (CNRS PICS, project PICS07703). Moreover, this research was the object of a *Bourse Fléchée* of the *École Doctorale EEATS* (Communauté Université Grenoble Alpes) and has been continued by PhD candidate Florent Cilici, who is currently in the third year of his PhD project under my co-supervision. In the context of this PhD, this work has been the recipient of two awards: the Best Poster Award form the *Journées National du Réseau Doctoral en Micro-nanoélectronique 2017*, and the Best Paper Award from the *IEEE European Test Symposium 2018*. The main results derived from this research line have been published in international conferences and journals [109, 118, 139, 140].

7.2 Theoretical basis

7.2.1 Stepwise addition of relevant features

In the view of the existing feature selection strategies for indirect test applications discussed in the previous chapter, the first logical step for designing new signatures would be to identify relevant information missing from a given set of signatures. The fundamental principle of machine learning indirect test is that circuit signatures and specifications are tightly correlated through a non-linear mapping function. The justification for this affirmation is that there is a unique underlying stochastic process –the fabrication process– that affects the signatures and causes performance fluctuation (and incidentally performance degradation). Then, if process variations are the root cause of both signature and performance variations, they are the perfect candidates for diagnosing a lack of relevant information. However, in a real fabrication process, we hardly have access to all the physical parameters. On the other hand, the real fabrication process is already modeled in most design kits and we do have access to the process parameters during the design phase at simulation level: this is the base of Monte Carlo process simulation. The Monte Carlo variables can be then traced back to actual physical components in the DUT thanks to the models of transistors and passive elements.

We propose to explore the set of Monte Carlo variables as if they were additional signatures that we could add to our initial set of signatures for training regression models. Since the process parameters are independent random variables, we can simply perform stepwise addition. Starting from the best available signature subset determined by feature selection, we train a regression model and evaluate the model performance adding one process parameter at a time, include the best candidate in the test list, and iterate. In that case, we would be able to identify which Monte Carlo variables bring significant additional information with respect to the already available signatures.

This methodology can be easily extended to complex SoCs. We can perform a system-level diagnosis search including higher-level parameters for each building block in the system. For instance, if the circuit contains an amplifier, we could perform Monte Carlo simulations to retrieve its gain, bandwidth, slew-rate, etc. at a small computational cost. These high-level parameters can be also included in the search list to guide the design of new features.

The final step of the procedure consists in designing simple tests that target the selected parameters in the DUT, in order to add the identified missing information to the regression. Obviously, the last point of this procedure still depends on the expertise of the designer but the diagnosis of the most important variation causes does bring significant information: identified signatures are those that bring relevant *additional* information. The value of the proposed procedure for guided feature design is to help the designer to go beyond an available set of initial features by proposing new ones.

7.2.2 Assisted test design for non-intrusive machine learning indirect test

The previous subsection proposes a methodology for guiding the design of *additional* features that target relevant information that was missing in the *initial* set of features. This rises an obvious question: how do we get the initial features?

In this research, we aim at fully automating the proposal of the initial set of signatures for the particular case of non-intrusive machine learning indirect test. Non-intrusive indirect test was first proposed in [135] for mixed-signal test applications, and later extended to the RF and mm-wave domain in [141, 142]. As it will be shown in this chapter, non-intrusive indirect tests are particularly suitable for automating the design of the test process. Non-intrusive techniques propose to use process variation sensors that mimic sensitive portions of the DUT. Then, DC measurements on these sensors, that are not electrically connected to the DUT, are used as test signatures for training machine learning regression models. The technique has obvious advantages for RF and mm-wave test, since the topology of the circuit is not modified and no additional loads are added to the DUT nodes. However, this technique is highly dependent on design knowledge: sensors are proposed based on an expert analysis on the circuit topology and no systematic approach for defining the set of initial signatures is proposed.

Let us consider a generic non-intrusive machine learning indirect test scenario in which we intend to regress a set of performances of a given DUT from a set of signatures measured from a set of non-intrusive process variation sensors. The problem we address in this chapter can be defined as follows, given the netlist of a particular DUT in a given technology and a set of target performances, how can we systematize the proposal of the set of signatures and the design of the associated sensors?

The methodology that we propose is divided into two interrelated steps. The first step is aimed at unveiling the root causes of parametric performance variation in the simulation environment. The second step is devised to find process variation sensors that are sensitive to the identified set of root causes. Let us describe these steps separately.

Step 1: Unveiling the root causes of parametric performance variation

The key idea for finding the root causes of performance variation at the design stage is to take advantage of the available information in the Monte Carlo (MC) models included in the Process Design Kit (PDK). Indeed, in a MC simulation environment, we have direct access to the complete set of root causes behind the DUT performance variation, that is, the set of statistical model parameters generated for each MC iteration. There are two sets of statistical parameters, describing global parametric process variations and local random mismatch. The non-intrusive machine learning indirect test approach works under the assumption that the effect of mismatch can be neglected with respect to process variations. Thus, our methodology explores the space of MC global process variation parameters to find the minimum subset that explains the observed parametric performance variation within a given accuracy threshold.

Exploring the space of process variation parameters can be seen as a feature selection problem in which we consider the MC parameters as candidate features to regress a given target performance using a machine learning regression model. Thus, we propose to adapt the Brownian distance correlation-directed search, previously presented in [110], according to the algorithm described in Algorithm 2.

Given a target performance, the proposed algorithm first ranks the MC process parameters with respect to their distance correlation to the target performance and trains an initial regression model

Algorithm 2 Exploring the space of MC process parameters using a Brownian distance correlation-Directed Search

```
Compute the distance correlation of all the MC process parameters with the performance and add the associated most correlated process parameter to the input space
while continue do
    Train a model mapping the input space onto the performance
    Compute the residues of the model
    Compute the mean square of the residues (the mean square error of the model fit)
    if The mean square error is less than or equal to a given threshold then
        continue ← 0
    else
        continue ← 1
        Compute the distance correlation of the remaining MC process parameters with the residue
        Add the most correlated MC process parameter to the input space
    end if
end while
return The input space (the most significant MC process parameters) and the mean square error of the fit
```

with the most correlated parameter. Then, we compute the residues of the fit (i.e. the individual errors for all the training samples). After that, the algorithm ranks the remaining MC process parameters with respect to their distance correlation to the residues of the fit and selects the best candidate to be added to the set of the most significant MC parameters. By iterating this procedure, the search is guided so that each iteration of the algorithm should identify a MC parameter that adds relevant information that was previously missing.

A key point of the algorithm above is the concept of correlation, that relies on the evaluation of the Brownian distance correlation [112, 132] as explained in the previous chapter.

Step 2: Assisted design of non-intrusive process variation sensors

The following step is to devise simple process variation sensors that provide a signature sensitive to the set of the most significant MC process parameters selected by the previous algorithm. Again, we take advantage of the information contained in the PDK of the technology to identify the underlying physical meaning of the selected process parameters. This way we can guide the design of appropriate non-intrusive sensors to target the desired information. Ideally, a dedicated sensor may be designed for each one of the selected process parameters. However, signatures, in practice, may contain contributions from several process parameters. The devised sensors, and their associated signatures, are then stored in a library for further reuse. Indeed, as the methodology is applied to different DUTs in the same technology, sensors may be reused if the same MC process parameters are deemed significant for new DUTs. In fact, once this library covers the complete set of MC parameters, the design of the test protocol becomes a simple test selection problem within the tests in the library. The methodology only calls for human intervention if there is no sensor in the library associated to a given process parameter.

This simple strategy leads the proposed methodology to capture the expert knowledge of the designer for the generation of new tests and sensors. It is worth noticing that, since the methodology guides the design of the sensors towards a target MC process parameter, sensors are actually independent of the topology of the DUT. In fact, no expert design knowledge on the DUT is required for any of the stages of the proposed methodology.

As a sanity check, we implement an automated validation for each developed sensor consisting in applying a Brownian distance correlation directed-search in the complete space of MC process parameters to train a regression model toward the sensor output signature. The goal of this validation is to ensure that the proposed signature is actually sensitive to the desired MC parameters.

The final output of the proposed test design algorithm for indirect test is the set of non-intrusive sensors and the actual set of measurements (i.e., the signatures associated to the sensors) for the regression of the DUT performances in a machine learning indirect test scenario.

7.3 Case studies

In order to demonstrate the feasibility of the proposed feature design strategies, this section details their application to two case studies and discusses the obtained results. The first case study reuses the RF LNA described in the previous chapter. It will be shown how stepwise addition may guide the design of additional features that can improve an initial indirect test scenario. The second case study is aimed at automating the design of a complete indirect test program for a millimeter-wave (mm-wave) Power Amplifier (PA).

7.3.1 Completing the initial set of features for the indirect test of an RF LNA

Going back to the LNA case study in the previous chapter, after feature selection we were able to obtain good predictions for its gain, while reducing the number of necessary measurements. For reference, Fig. 7.1 shows the generalization error for the gain prediction as a function of the number of selected features, obtained using a wrapper search for four different sets of initial features: only DC features (labelled as Dc set), DC features and power stress (Dc + vdd set), DC and envelope detector output features (Dc + env. set), and the complete set of 42 features (Dc + env. + vdd set).

After performing feature selection, the question of completeness still remains: could we add new signatures in order to improve the predictions even more? Is there non-modeled information? In order to explore these questions, this section revisits our LNA case study from the point of view of the proposed strategy for stepwise addition of features.

Firstly, in order to get an intuitive insight into the information contained into the Monte Carlo variables, we perform a feature selection wrapper search over the 33 process variables that are defined in the design kit of the selected 90nm CMOS technology. After 9 iterations, we end up with a reduced model of 12 process variables and a generalization error of 0.024dB, as can be seen in Figure 7.2.

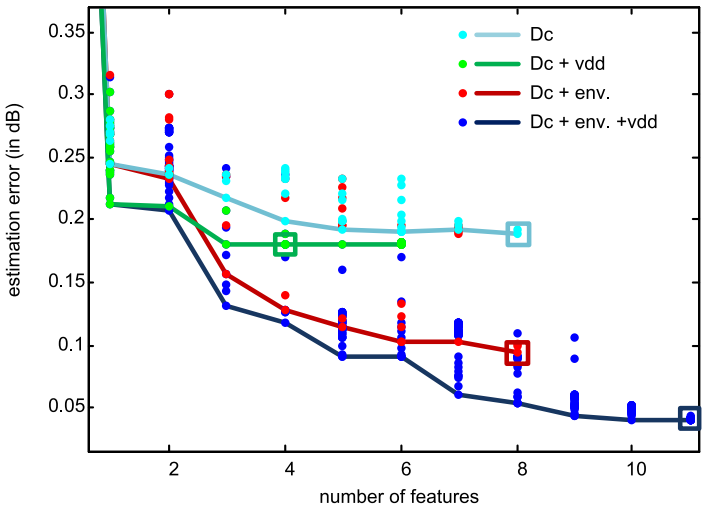


Figure 7.1 – Generalization error versus number of features, for all of the visited cases of the four different training scenarios

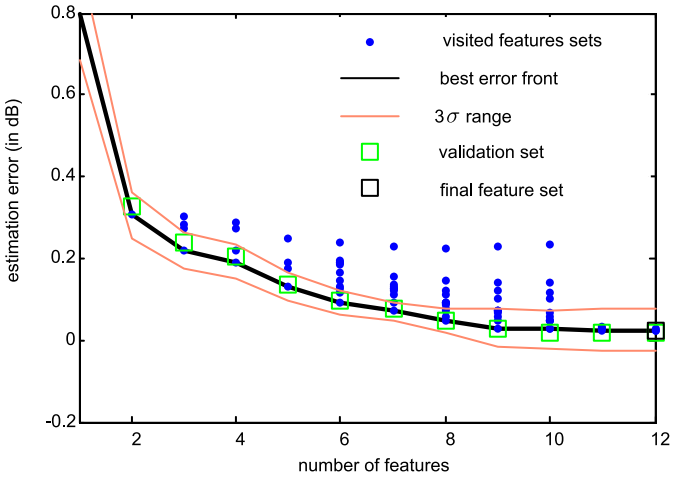


Figure 7.2 – Generalization error versus number of process variables, for all of the visited cases during the optimization search

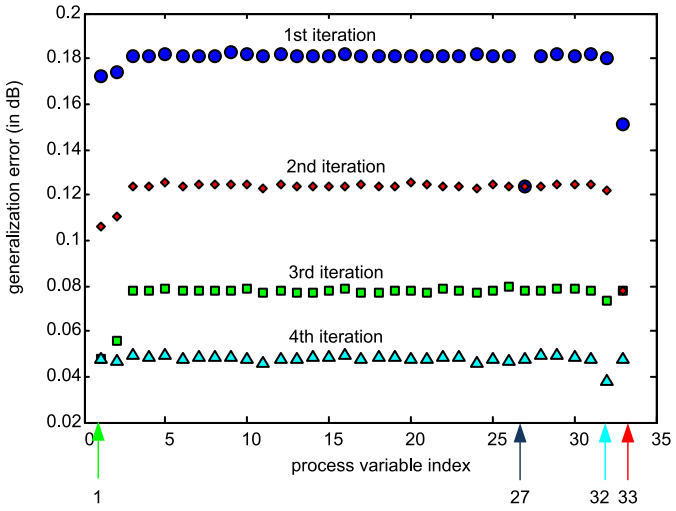


Figure 7.3 – Generalization error for stepwise addition of process parameters, starting from the DC signatures with supply stress.

This error value is significantly lower than that obtained with DC signatures, and lower than the obtained including the envelope detector with power supply stress. These feature sets can thus be improved if we are able to design specific tests that target the missing information. In order to diagnose which parameters should be targeted, we perform a stepwise addition search using the 33 technology process parameters. For this example, we consider as initial set of signatures the best feature set from the DC signatures with supply stress (corresponding to the Dc + vdd set in Fig. 7.1).

Figure 7.3 shows the generalization errors obtained by adding one process parameter, for four iterations. At the fourth iteration, we see that the improvement is marginal. As a result of this procedure, we can identify three Monte Carlo process variables –labelled 1, 27, and 33 in Fig. 7.3– that bring significant additional information. By tracing back these process variables to the physical models of the devices in the design kit, we found out that our algorithm pointed at metal-insulator-metal capacitors, polysilicon resistors, and RF inductors as non-modeled information. This result is coherent with an electrical analysis of the DUT: our initial set of signatures was composed by DC levels, so parametric variations of capacitors and inductors would not have been detected, leading to non-modeled information in our regression.

The next step to improve our regression is then to design new tests to target these components. In this example we rely on Process Monitors for this purpose. These structures mimic selected parts of the DUT and are located in the close proximity of the replicated sections, in such a way that process variations affect both structures in a similar way [135]. Thus, we replicate capacitors C_1 and C_2 (capacitor C_3 is equal to C_2), and resistor R in the arrangement shown in Fig. 7.4a. An external low-frequency AC source is used at the input of each monitor circuit for measuring its impedance. This methodology, however, is not appropriate for characterizing the effect of process variations across the inductors in the LNA, given that replicating inductors L_g, L_s, and L_d would result in an excessive area overhead. Instead of that, we propose to use the arrangement depicted in Fig. 7.4b. In this test set

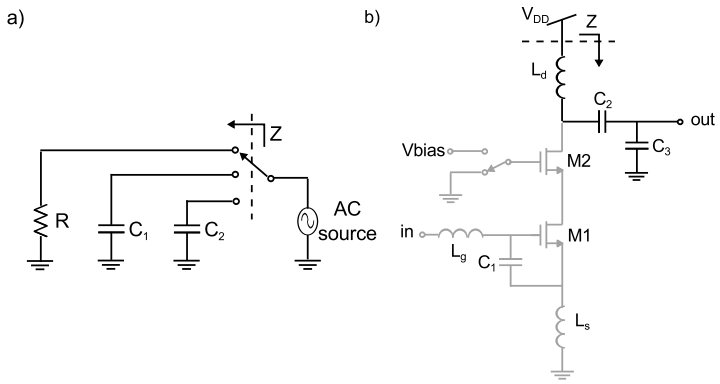


Figure 7.4 – a) R and C monitors; b) Test set-up for detecting inductance variations

Feature space	Prediction error (in dB)	σ_{Err} (in dB)	Validation set error (in dB)	$n_{feature}$	Reduction factor
DC	0.189	0.018	0.191	8	-
DC + vdd	0.180	0.014	0.187	4	-
DC + env.	0.092	0.009	0.090	9	-
DC + env. + vdd	0.040	0.011	0.039	11	-
Process Variables	0.024	0.017	0.019	12	-
DC + passive	0.065	0.011	0.066	12	2.9
DC + vdd + passive	0.042	0.014	0.036	9	4.3
DC + env. + passive	0.030	0.014	0.027	11	3.1
DC + env. + vdd + passive	0.025	0.014	0.022	13	1.6

Table 7.1 – summary of the best feature sets results

up the signal path in the LNA is broken by switching off the cascode transistor $M2$. An external AC source can then be used to characterize the impedance seen from the V_{DD} node, which is a function of the inductance value of L_d.

With these simple low-cost tests, we get four additional signatures. Including these new signatures, we then re-run the optimization process from scratch for the same four scenarios as in figure 7.1. Table 7.1 shows a summary of the past and new results. In all scenarios, the introduction of passive signatures greatly improves the obtained prediction error. In particular, it is worth noticing that with the complete set of signatures a precision of 0.025dB is achieved, which is similar to the limit obtained by regressing directly from the process variables. The best improvement is observed for the case of DC signatures with supply stress, which lowers the prediction error from 0.18dB to 0.042dB. This precision is comparable to what was obtained with the envelope detector and the supply stress, but without the need of any BIST circuitry.

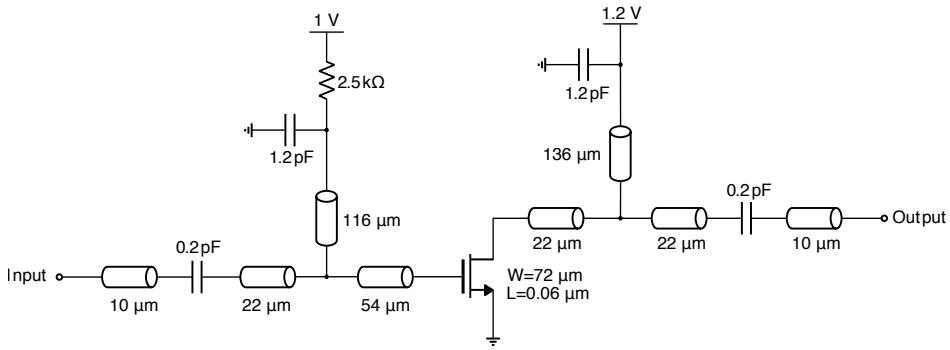


Figure 7.5 – Transistor level schematic of the Power Amplifier under test

Operating frequency range	59 to 61 GHz
DC current, I_{DC}	28.2 mA
Power supply, V_{DD}	1.2 V
Gain (S_{21})	5.6 dB @ 60 GHz
Power Added Efficiency, *PAE*	11%
S_{11}	< -20 dB
S_{22}	< -20 dB
S_{12}	< -13 dB
Input referred 1dB-Compression Point, CP_{1dB}	0.7 dBm
Saturation output power, P_{sat}	10.5 dBm
Input referred third-order intercept point, *IIP3*	11 dBm

Table 7.2 – Performance and design parameters of the PA under test

7.3.2 Assisted design of a non-intrusive indirect test program for a mm-wave PA

The selected DUT for this case study is a one-stage mm-wave Power Amplifier designed in STMicroelectronics 55 nm BiCMOS technology. Despite the apparent simplicity of the circuit, it is difficult to identify *a priori* the dominant source of performance degradation of the PA, since it is affected by variations of both the active and passive components. This makes it an interesting case study for the proposed test generation methodology. Figure 7.5 shows the transistor-level schematic of the circuit. The PA input and output nodes are matched to a $50\ \Omega$ impedance at 60 GHz using microstrip line stubs. The main performance specifications of the designed PA, obtained after post-layout simulation, under typical corner operation conditions are listed in Table 7.2.

The presented methodology for test design has been applied to the selected DUT as a practical case study to illustrate the technique. The goal of this case study is to generate a set of appropriate non-intrusive sensors that provide meaningful signatures for testing the DUT using a machine learning indirect test strategy.

A set of 2000 instances of the selected PA has been generated using the MC models provided in the PDK of the technology. A total of 300 instances of the PA are set apart to be used as an

independent verification set and the remaining instances are used for training. The first step of the proposed methodology, as described above, is to find the root-causes of parametric variation within the set of MC parameters defined in the technology. The MC simulation of the PA in the selected 55 nm BiCMOS technology includes 154 independent process parameters $\{MC_1, \ldots, MC_{154}\}$ that define the search space. The exploration of the MC parameter space uses the proposed Brownian distance correlation-directed search for regressing the PA specifications. A perceptron Neural Network is used as machine learning regression algorithm. In this chapter we illustrate the complete procedure for one of the specifications, namely, the small signal gain of the PA at 60 GHz. The process can be iterated for the rest of the specifications.

Figure 7.6 presents the Root-Mean-Square (RMS) error in the regression as a function of the number of MC parameters selected by the search algorithm, for the complete set of training instances (marked with blue diamonds), and the samples in the independent verification set (marked with red circles). For illustration purposes, instead of setting a target prediction error as stopping condition for the algorithm, the search has been set to find and rank the 20 most relevant MC parameters, as shown in Fig. 7.6. It is interesting to notice that the proposed algorithm guides the selection of MC parameters in such a way that it yields a monotonic improvement of the prediction error. Moreover, it is clear to see that this improvement of the prediction error tends to slow down around the fifteenth iteration of the search. In this line, the 15 most significant parameters have been selected and are labelled to the corresponding data points in the figure. Figure 7.7 shows the scatterplot of the predicted versus actual gain of the PA when we train a Neural Network regression model using these 15 selected MC parameters as input features. Blue dots represent the training data set, while red circles mark the samples in the independent verification set. It is clear that the selected MC parameters have a very strong correlation to the target performance.

Once the most relevant MC parameters for the prediction of the targeted performance have been identified, the second step in the presented test design methodology is to propose appropriate non-intrusive sensors that yield signatures strongly correlated to these parameters. The design of these sensors and their associated measurements is guided by the physical meaning of the selected MC parameters. Parameters MC_{46}, MC_{48}, MC_{49}, MC_{60}, MC_{69}, MC_{150} and MC_{154} are linked to the electrical properties of transmission lines, parameters MC_{12}, and MC_{23} point to MOM capacitor variations, and the rest of identified MC parameters (MC_{77}, MC_{78}, MC_{80}, MC_{85}, MC_{86}, and MC_{111}) are related to variations of the NMOS transistor.

Taking into account the physical meaning of the parameters, Table 7.3 details the schematics of the developed sensors and the associated measurements (i.e., signatures). In order to verify that the 15 selected MC parameters are covered by the proposed signatures, we perform our Brownian distance correlation-directed search in the space of process parameters for regressing each one of the proposed signatures. In this line, Table 7.3 also includes the list of most significant MC parameters that explain the variation of each proposed signature for validation. As it can be seen, all 15 relevant MC parameters are covered by the devised signatures.

In total, for covering the identified 15 most significant MC parameters we have developed 5 non-intrusive sensors and 9 signatures labelled as $\{S_1, \ldots, S_9\}$. Notice that signatures are sensitive to multiple MC parameters, which reduces the number of necessary measurements. The proposed set of signatures contains DC measurements and low frequency AC measurements extracted at 100 MHz.

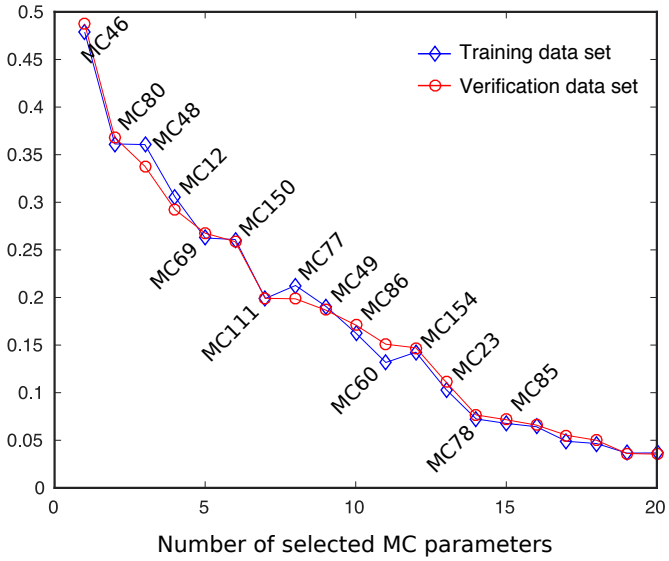


Figure 7.6 – Exploration of the MC process parameter space for finding the root causes of gain parametric variation for the DUT. Data point labels indicate the MC process parameter MC_i selected in each iteration of the search algorithm.

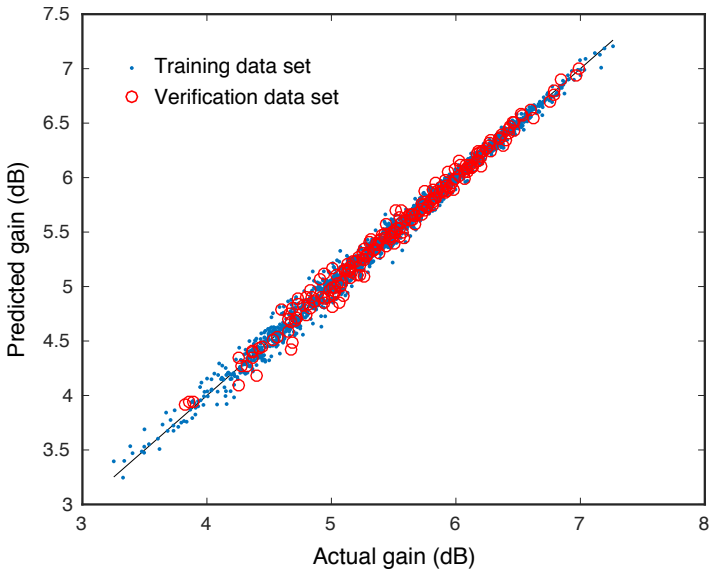


Figure 7.7 – Scatterplot of predicted versus actual gain of the PA using the 15 most relevant MC parameters as signatures.

These low frequency measurements are simpler and cheaper to extract than at-speed 60 GHz measurements on the PA under test. From an electrical point of view, the proposed signatures contain information about phase-shifts in the elements of the PA (S_1, S_2, S_4), capacitive behavior (S_6, and S_7), electrical losses (S_3, S_5, and S_8) and the operation point of the NMOS transistor (S_9).

The developed non-intrusive sensors and their corresponding signatures are then stored in a library for reuse in future indirect test programs. As it was mentioned above, the developed sensors are independent of the DUT topology, since they are devised to target specific root causes of parametric variation in a given technology. The reuse of the library of non-intrusive sensors for other DUTs offers an additional layer of automation to the proposed test design strategy.

As a final validation of the performance of the proposed assisted test design strategy, we applied the resulting non-intrusive machine learning indirect test to the PA. A perceptron Neural Network is trained to regress the gain of the PA under test from the identified 9 input signatures $\{S_1, \ldots, S_9\}$ extracted from the generated non-intrusive sensors. Figure 7.8 shows the scatterplot of the predicted versus actual gain over the 2000 generated instances of the PA under test. Blue dots mark the training data set, while red circles represent the samples in the independent verification set. As it can be seen, the proposed test program offers a good estimation of the gain performance across the complete variation range. The RMS error of the prediction for samples in the independent verification set is of only 0.08 dB, which is comparable to the regression in Fig. 7.7 that employed the 15 most significant MC process parameters as input signatures and yields an RMS prediction error of 0.07 dB. This result is a good indicator of the relevance of the proposed set of signatures to capture the variation of the target performance.

Finally, the complete test design process can be repeated for the rest of the specifications of the PA under test. Interestingly, if we consider the complete set of PA performances in Table 7.2, the described assisted test design algorithm leads to an additional measurement on one of the already proposed non-intrusive sensors. This new signature, S_{10} using the previous notation, is the imaginary part of scattering parameter S_{11} measured at 100 MHz for the MOS transistor sensor described in Table 7.3. In order to validate the resulting non-intrusive indirect tests, perceptron Neural Network models have been trained for regressing the complete set of PA specifications using the identified set of signatures $\{S_1, \ldots, S_{10}\}$. Table 7.4 lists the RMS prediction error for samples in the independent verification set for each specification. In order to evaluate the quality of the regression models, Table 7.4 compares the obtained RMS errors with the standard variation of the specification in MC simulations. It is clear to see that the obtained models trained with the automatically identified set of signatures offer significant predictions for all the considered specifications.

7.4 Conclusions

This chapter described methodologies for automating the design of relevant test signatures for machine learning indirect test applications. The proposed methodologies have been validated on two different case studies, namely a RF LNA and a mm-wave PA. Obtained results demonstrate the capabilities of the developed algorithms for guiding the design of new signatures and show a promising potential for automating the design of the complete indirect test protocol.

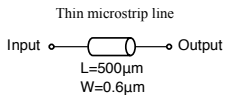
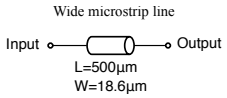
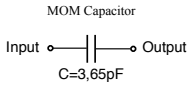
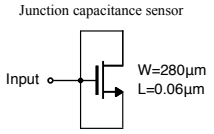
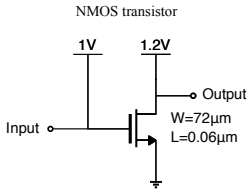
Process variation sensor schematic	Signature description	MC parameters covered
	— S_1: Imaginary part of S_{11} @ 100 MHz	— MC_{46}, MC_{48}, MC_{49}, MC_{69}, MC_{150}
	— S_2: Imaginary part of S_{21} @ 100 MHz	— MC_{46}, MC_{48}, MC_{69}, MC_{150}, MC_{154}
	— S_3: Resistance	— MC_{48}
	— S_4: Imaginary part of S_{11} @ 100 MHz	— MC_{69}, MC_{150}, MC_{154}, MC_{60}, MC_{46}
	— S_5: Real part of Y_{11} @ 100 MHz	— MC_{12}, MC_{31}
	— S_6: Imaginary part of S_{21} @ 100 MHz	— MC_{23}, MC_{31}
	— S_7: Imaginary part of S_{11} @ 100 MHz	— MC_{86}, MC_{85}, MC_{111}, MC_{91}
	— S_8: Gate resistance	— MC_{80}, MC_{111}, MC_4, MC_{77}, MC_{78}
	— S_9: Bias current	— MC_{11}, MC_{91}, MC_{35}

Table 7.3 – Developed non-intrusive sensors and associated signatures for gain prediction

Specification	Unit	σ_{spec}	RMS prediction error
Gain (S_{21})	dB	0.69	0.08
PAE	%	1.98	0.17
S_{11}	dB	4.46	0.5
S_{22}	dB	4.92	0.7
S_{12}	dB	0.75	0.13
CP_{1dB}	dBm	0.58	0.075
P_{sat}	dBm	0.17	0.025
*IIP*3	dBm	0.67	0.11

Table 7.4 – Prediction of PA performances using the generated indirect test program

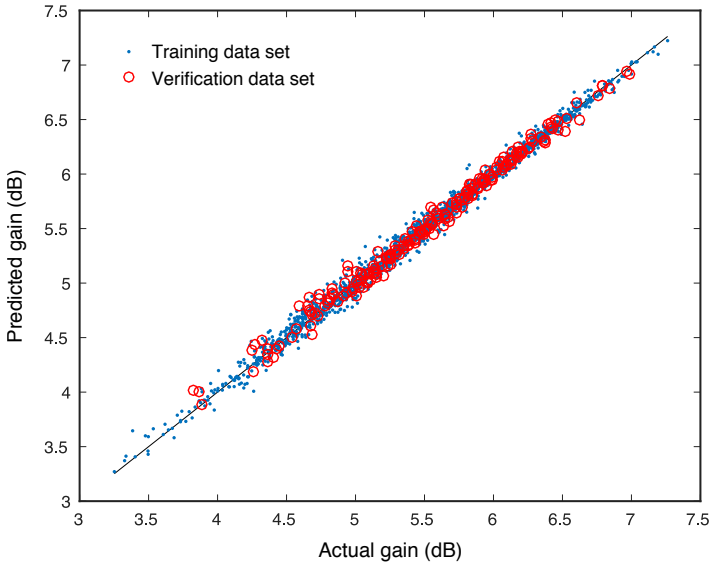


Figure 7.8 – Scatterplot of predicted versus actual gain of the PA using the generated indirect test program with 9 non-intrusive signatures.

Chapter 8

Perspectives

My research objectives for the following years can be organized into four principal research axes related to AMS-RF integrated circuits, namely:

a. BIST and design-for-test solutions

b. Calibration, self-repair, fault tolerance and self-healing of integrated circuits

c. Computer-aided design-for-test

d. Emerging design paradigms

Research lines (a) to (c) represent near- and mid-term research goals currently supported by research projects HADES (PENTA European program, in collaboration with STMicroelectronics), TARANTO (ECSEL Joint Undertaking, in collaboration with RFICLab and STMicroelectronics) and IndieTEST (CNRS PICS, in collaboration with IMSE-CNM). To further support these research lines in the near future, we partnered with STMicroelectronics within the Nano2022 project, currently under evaluation by the French authorities, and we plan on building on the base of our current PICS project to further extend our collaboration with IMSE-CNM, with the mid-term goal of creating an international joint laboratory.

Research line (d) represents mid- to long-term goals that will be built on recent research activities that I led in our group. In this line, we recently started a collaboration with STMicroelectronics and the University of Sherbrooke, Quebec, on cryo-CMOS circuits for quantum computing applications, and we have submitted regional project ADMIL, currently under evaluation, in collaboration with RFICLab and ASYGN on mm-wave integrated circuit design, test and calibration using advanced machine learning algorithms.

8.1 BIST and design-for-test solutions

Nowadays, testing the AMS-RF functions in a complex integrated system represents the largest fraction of the test cost. Moreover, AMS-RF tests are usually time consuming and require multiple test configurations using dedicated test equipment for the characterization of the complete set of circuit

specifications. Indeed, AMS-RF tests are one of the main bottlenecks for the production of mixed-signal integrated systems. Therefore, simplifying the test of AMS-RF circuits is an area of innovation that may have a significant impact for the IC industry. In this line, Design-for-Test solutions are aimed at reducing test cost and complexity by taking into consideration the testability of the circuit at the design stage. This research line is focused on a) extending our portfolio of embedded test instruments for BIST applications of high-performance AMS-RF circuits, b) proposing dedicated DfT solutions for relaxing the stringent AMS-RF test requirements, and c) leveraging the power of advanced machine learning algorithm to simplify and minimize the number of required analog measurements. We will prioritize test solutions that are mostly digital and preferably non-intrusive, in such a way that the performance of the DUT is not degraded, the developed test instruments can be easily ported between different technological nodes, and the complete test can be controlled from a cheap low-performance digital tester.

8.2 Calibration, self-repair, fault tolerance and self-healing of integrated circuits

Standard BIST techniques and machine learning-enhanced BIST techniques, if made feasible, not only would reduce AMS-RF test complexity and cost, but they would enable interesting features such as in-the-field test, on-line test, diagnosis capabilities, adaptive operation, self-calibration, and self-healing that can have a huge socio-economic impact in many different applications. In the following years, we intend to transcend the production test paradigm and explore these advance features in novel application scenarios. For instance, self calibration and self healing are key attributes for high reliability applications (e.g., harsh environments, systems with limited or impossible access) or that are safety critical (e.g., automotive, avionics, space operations, healthcare systems). Adaptive operation may enable significant battery savings in low-power consumer devices such as Internet-of-Things applications, and in-the-field test and on-line test may give us insight into the aging mechanisms and reliability hazards in complex AMS-RF systems.

8.3 Computer-aided design-for-test

Machine learning-based test offers a systematic approach to AMS-RF testing that may open the door to automated test generation flows. However, it has to be noted that enabling mixed-signal test automation faces a key roadblock. This challenge consists in finding a way to capitalize expert design knowledge to provide appropriate indirect measurements –signatures– to build robust prediction models. These indirect signatures should accurately capture the main degradation mechanisms of a given DUT while relaxing the required measurement protocols compared to a complete functional test. In this line, novel feature selection paradigms such as causality inference may give us an enhanced insight into the performance degradation mechanisms which may lead to the definition of novel test strategies and tools for test and design automation. Traditional feature selection methods rely on implicit correlations. However, this is not satisfying from a robustness perspective since the information

on the underlying mechanisms that link the features to the metric of interest is lost. These mechanisms are the causal relations that reflect the rules of physics governing the circuit behavior. Causality inference may improve current machine learning indirect test by guiding the design of test features towards causally relevant features. Moreover, the resulting causal features can potentially improve defect detection and diagnosis. We intend to advance this research line towards the design of robust defect filters based on causal features. Such defect filters should be more robust to unknown defects than current defect filters based on observational features. In addition, from a designer point of view, the use of causal discovery algorithms may also be interesting. The extraction of the causal structure around a set of specifications of a given circuit is a valuable diagnosis tool that can be used for guiding automated design flows.

8.4 Emerging design paradigms

In the long term, our goal is to take advantage of our Design-for-Test techniques in novel design paradigms, namely the mm-wave integrated circuits for high-data-rate communications and the cryo-CMOS electronics for quantum computing applications. Mm-wave integrated circuits are one of the key enabling technologies for the development of future telecommunication standards such as 5G. Enabling on-chip testing, calibration and adaptive operation of these devices is an open research problem that can improve the reliability and power efficiency of these systems. On the other hand, cryo-CMOS electronics has been recently proposed for future monolithic qubits that include the required control electronics on-chip. Sensing and controlling the state of integrated qubits requires the application of appropriate stimuli and the acquisition of the response. Moving these operations on-chip without degrading the performance of the integrated qubits mirrors traditional mixed-signal BIST strategies with embedded test instruments and is currently a major challenge for enabling future quantum computers.

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Title: Built-In Self-Test solutions for high-performance and reliable analog, mixed-signal, and RF integrated circuits

Abstract: The integration capabilities offered by current nanoscale CMOS technologies enable the fabrication of complete and very complex mixed-signal systems. However, manufacturing processes are prone to imperfections that may degrade –sometimes catastrophically– the intended functionality of the fabricated circuits. Extensive production tests are then needed in order to separate these defective or unreliable parts from functionally correct devices. Unfortunately, the co-integration of blocks of very distinct nature (analog, mixed-signal, digital, RF, ...) as well as the limited access to internal nodes in an integrated system make the test of these devices a very challenging and costly task.

BIST techniques have been proposed as a way to overcome these issues. These techniques aim at including some of the ATE functionality into the Device Under Test, in such a way that each fabricated system becomes self-testable. Applying BIST to the digital part of a complex integrated system is a common and standardized practice. Many test alternatives broadly proven in practice are available, all of them based on defect test and fault models. On the other hand, AMS-RF BIST techniques are still lagging behind due to the strict requirements imposed by the analog circuitry. Since AMS-RF circuits are usually tested by measuring their functional specifications, this means that each measurement has to comply with strict accuracy constraints to match the performance of the circuits under test.

A promising solution to these issues is the combination of BIST strategies and machine learning-based tests. Machine learning test strategies replace costly analog, mixed-signal and RF performance measurements by a set of simpler measurements that can be performed on-chip by low-cost built-in test circuitry. The core idea is to build a mapping model from a set of simple measurements to the set of functional specifications. However, this test strategy is not free of shortcomings either.

My research has been focused on overcoming the limitations of current BIST and machine learning-based test for complex AMS-RF circuits, with the final goal of providing innovative state-of-the-art test solutions for these complex systems

Keywords: Design-for-Test ; Built-In Self-Test ; Machine Learning ; Feature selection

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