Metal gate work function modulation mechanisms for 20-14 nm CMOS low thermal budget integration

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Compréhension de la modulation du travail de sortie de métaux de grille pour l'intégration à bas budget thermique du CMOS 20-14 nm

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Glossary

ϕ, ϕ_m, ϕ_s	Vacuum Work function, of the metal, of the substrate
ALD	Atomic Layer Deposition
BEOL	Back End Of Line
Cs	Spherical aberration coefficient
C-V	Capacitance - Voltage
CET	Capacitance Equivalent Thickness
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
δ	Voltage shift due to dipole
EDX	Energy Dispersive X-ray
EELS	Electron Energy Loss Spectroscopy
EOT	Equivalent Oxide Thickness
EWF	Effective Work Function
FDSOI	Fully Depleted Silicon On Insulator
FEG	Field Emission Gun
FEOL	Frond End Of Line
FG	Forming Gas
Fin FET	Fin Field Effect transistor
GF	Gate First
GL	Gate Last
HAADF	High Angle Annular Dark Field
HK	High permittivity
HRTEM	High Resolution Transmission Electron Microscopy
IBD	Ion Beam Deposition
IL	Interlayer
ITRS	International Technology Roadmap for Semiconductors
MG	Metal Gate
MIGS	Metal Induced Gap States
MOS	Metal Oxide Semiconductor

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PIPS	Precision Ion Polishing System
Poly-Si	Polysilicon
PVD	Physical Vapor Deposition
Q	Interface charge density
ρ	bulk charge density
RMG	Replacement Metal Gate
RTP	Rapid Thermal Processing
S/D	Source/Drain
SDD	Silicon Drift Detector
SEM	Scanning Electron Microscopy
SOI	Silicon On Insulator
STEM	Scanning Transmission Electron Microscopy
TEM	Transmission Electron Microscopy
ToF SIMS	Time of Flight - Secondary Ion Mass Spectrometry
UTSOI	Ultra Thin Silicon On Insulator
V_{fb}	Flat Band Voltage
V_{th}	Threshold voltage
WF	Work Function
XPS	X-ray photoelectron spectroscopy
XRD	X-Ray Diffraction
XRR	X-Ray Reflectivity

Introduction

Three engineers working for Bell labs achieved the realization of the first bipolar transistor on Ge in 1947: Bardeen, Brattain and Shockley. Their work was awarded the Nobel price of physics in 1956. Two years later, the first silicon-based integrated circuit has been realized by Jack Kilby, engineer at Texas Instruments (Nobel Price in 2000). This enabled the reduction of computers cost and size by integrating on the same circuit several transistors. In 1960, Khang and Attala realized the first Metal Oxide Semiconductor Field Effect transistor (MOSFET) on Si. These different breakthroughs made possible the realization of the first transistor-based computer by IBM (IBM 7000). Then, since the size of the elementary transistor device steadily decreased, higher transistor integration on a constant ship surface was possible, which had two benefits. First, the manufacturing cost per transistor can be reduced and second, the chips performances were improved. At this time (1965), Intel's co-founder Gordon Moore predicted that the transistors number would double approximately every two years.

Until the late 90's, this miniaturization relied on size reduction of fully silicon-based transistors made of a silicon substrate, a native silicon oxide (SiO_2) and a polysilicon gate. The decrease of the transistor dimensions accompanied the thinning of the gate oxide in order to maintain enough control on the conduction channel by increasing the capacitive coupling. However, in the same time, exponential increase of the leakage currents occurred due to the drastic reduction of the silicon oxide thickness. The only way to continue the miniaturization path was to replace the historical SiO_2 insulator by a high-k dielectric. This enabled to return to a reasonable dielectric thickness, which reduced the leakage currents while keeping a high capacitive control on the conduction channel.

In the 2000's, ZrO_2 and HfO_2 oxides were intensively studied as potential replacement gate oxides. Finally, HfO_2 oxide was chosen thanks to its high dielectric constant, its adapted band gap offset with respect to silicon valence and conduction bands and its high thermodynamic stability on Si. Then, to limit the degradation of the equivalent oxide thickness and the difficulty to modulate the effective work function (EWF) when the commonly polysilicon gate is used on HfO_2, metal gate electrodes were introduced. However, from the materials point of view, some problems remained. In particular, with today's gate first process, the

whole gate stack has to withstand the source/drain dopant activation anneals at high temperature (1050°C, gate first integration), which may alter the metal gate work function because of severe elemental diffusion and reaction. A proposed alternative is to process the HfO_2/metal gate structure at a lower thermal budget (T<500°C). The corresponding process is known as gate-last or replacement gate integration.

At the beginning of this PhD work, only Intel Corporation integrated High-k/Metal gate using the gate-last approach for its 45 and 32nm CMOS technology mass production. STMicroelectronics that is involved in the International Semiconductor Development Alliance (ISDA) followed the gate first approach for its 32 nm CMOS node. My thesis work aims to give to STMicroelectronics the key parameters that enable the control of the gate electrode effective work function and the scaling of the equivalent oxide thickness, two major gate stack parameters that drive the transistor threshold voltage (V_{th}) and Capacitance Equivalent Thickness (CET). This is done with in mind future low thermal budget integrations for ST's sub-20nm CMOS nodes.

The thesis work was performed on three locations: CEA Leti, STMicroelectronics and CEMES-CNRS. Mass production industrial tools have been used for metals deposition at STMicroelectronics and CEA-Leti. Advanced material characterization methods such as backside XPS and ToF-SIMS analysis at CEA-Leti together with state of the art TEM tools (Tecnai OSIRIS at ST Crolles, Cs-Corrected Tecnai at CEMES) have been used for a high quality characterization of the studied structures.

The different fabricated electrodes on HfO_2 and the complementary advanced material characterization techniques were chosen to investigate systematically chemical stability and effective work function modulation in these stacks.

In the first chapter, we will describe the main limits of the famous SiO_2/Polysilicon gate in CMOS scaling as encountered at the end of the 1990's. Then, we will introduce the state of the art situation dealing with the integration of HfO_2/metal gate stacks. We will define and discuss two important parameters for CMOS application, i.e. the effective work function and the equivalent oxide thickness. Finally, we will detail the challenges to be overcome for their optimization with a particular attention to the gate last processes.

In chapter II, we will present the different characterization techniques investigated in this thesis work with a particular focus on the advantages and drawbacks of each technique regarding the studied gate stack structures.

In the following chapters, III to VI, we aim at designing metal gates for HfO_2 dedicated for low thermal budget processes. For this, we will consider mainly gate stacks made of bilayers, with a p-type work function metal first or an n-type work function metal first. We will study their chemical state, i.e. the species distribution in the whole stack and the bonding of the elements, in parallel with the electrical properties of the corresponding MOS capacitors, i.e. their effective work function and equivalent oxide thickness. In particular, we will propose discussions about the impact of the chemical state on the electrical performances.

In chapter III, we will consider the case of TiN-based metal electrodes. TiN is well known for its compatible p-character when deposited on HfO_2. In order to propose a candidate for n-MOS co-integration with TiN, we will first investigate layers of reactive elemental metals deposited on TiN like Ti and Al. Then in chapter IV we will consider the case of binary metallic TiAl deposition on TiN and the ternary TiAlN metal alloy directly deposited on HfO_2 with varying N content. The thermal stability of these stacks will be studied in chapter V.

In chapter VI, more innovative metal gates will be considered. In particular, we will study the deposition of TaN, Ta and Ni on HfO_2. We will investigate the alloying of TaN with Ta in HfO_2/TaN/Ta as an alternative gate stack to previously studied HfO_2/TiN/(TiAl, Al, Ti). We will finally propose innovative options based on alloying p-type metals on n-type first metal. Ni will be alloyed with Ta and Ti in HfO_2/Ta/Ni and HfO_2/Ni/Ti respectively. Here again, we will evaluate the thermal stability of these alternative gates.

Chapter I

High-k/Metal Gate effective work function modulation and equivalent oxide thickness scaling for gate last integration

I-1. CMOS scaling: from SiO_2/Poly-Si to High-k (HK)/metal gate (MG)

The metal-oxide-semiconductor field effect transistor (MOSFET) consists of four terminals, namely the source, gate, drain, and substrate. It is, in its very simplest form, a mere extension of the MOS capacitor, in which the gate electrode and the semiconductor channel constitute the parallel capacitor plates and the insulating oxide layer is equivalent to the dielectric material. A schematic representation of an nMOSFET is shown in Figure I-1. The gate electrode controls the carrier density in the channel by transmitting an electric field through the gate oxide. In particular, for an nMOSFET (pMOSFET), a hole (electron) depleted region is created in the channel and a flow of electrons (holes) goes from the source to the drain (ON state, inverted channel). Complementary-MOS (CMOS) circuits use a combination of pMOSFET and nMOSFET to implement logic gates and other digital circuits.

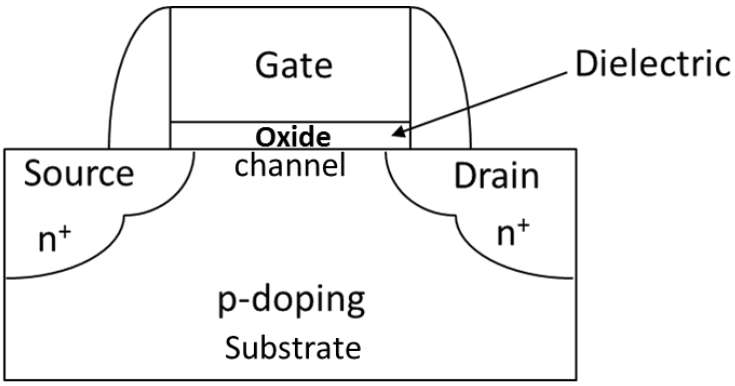


***Fig. I-1** – A typical nMOSFET*

Power dissipation in MOSFETs, which limits today the device performance, is minimized if the voltage over the gate required to achieve the inverted channel (ON state), namely the threshold voltage, is low and symmetric for nMOS and pMOS. This requires that the effective work function (EWF) of the gate stack can be tuned close to the bottom of the conduction band energy and to the top of the valence band energy. This means the need to find band edge metals with EWF of 4-4.2 eV for nMOS and 5-5.2 eV for pMOS in MOSFET bulk technology [Cheng01, De00]. It is less severe for the case of "Thin Body" MOSFET technology (Silicon On Insulator SOI or Fully Depleted SOI, Multiple gate FinFET), EWF being ±0.2eV with respect to the midgap, namely about 4.4eV for nMOS and 4.8eV for

pMOS [Cheng01, Chang00]. Figure I-2 illustrates the required EWF for n and pMOS transistors using bulk or "Thin Body" CMOS technologies.

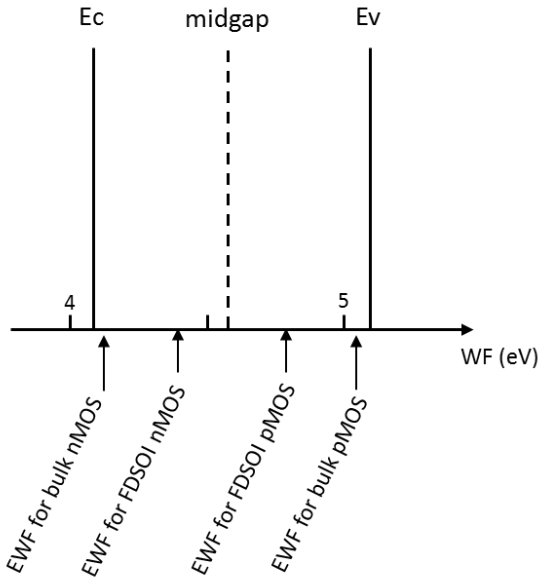


***Fig. I-2** – Required gate EWF for n and pMOS transistors in bulk or "thin body" (FDSOI) CMOS technologies*

With the Si-based CMOS technology, the MOSFET gate electrode materials were unchanged until the late 90's with SiO_2 as the gate oxide and polysilicon (poly-Si) as the gate electrode. Typical construction of the contact electrode for the n-type and p-type MOS is differentiated by doping the poly-Si electrode with n- and p-type dopants. This modulates the poly-Si EWF at ~4.0 eV and ~5.1 eV, respectively.

For the sub-65 nm node, this standard structure reached a fundamental limit. Gate oxide leakage due to direct tunneling current became much higher than desired because of the very low physical thickness of the silicon oxide (~about 1.2nm of SiO_2 for the Intel's 65nm [Bohr07]). In addition, poly-Si gate suffered from the depletion effect where a depleted portion of the gate electrode occurs when the channel is inverted. This induced an increase of the dielectric thickness of the insulator adding a capacitance in series with the one of the gate dielectric [Joss99].

To face these problems, intensive investigations have been conducted to find the best candidates for the replacement of the SiO_2/poly-Si couple and extend the Si CMOS technology beyond the 65nm gate length node.

Hf-based oxides with higher permittivity (k) than SiO_2 (commonly called high-k, noted in this manuscript HK) prepared by Atomic Layer Deposition (ALD) emerged as the best choice to replace SiO_2 thanks to their high dielectric constant, suitable band gap and sufficient barrier height needed to suppress leakage current, and good chemical and thermal stability [Wilk01, Robertson06, Robertson08, Ray06, Wong06, Houssa06, Mistry07, Bohr07]. The HK oxide did not completely replace SiO_2. Indeed, a very thin SiO_2 layer remained necessary as an interlayer (IL) between the HK oxide and the silicon substrate preserving a rather good electrical interface quality [Kim04]. The HK introduction conducted to a new definition of the insulator electrical thickness called Equivalent Oxide Thickness (EOT), which takes into account the contribution of SiO_2 and HK dielectric constants. The EOT will be well described later in this chapter.

At the beginning, the poly-Si gate has been maintained on the HK oxide. However, very soon different drawbacks appeared. The poly-Si depletion phenomenon, the dopant diffusion to the gate/oxide interface (in particular boron for p-doped poly-Si) and the difficulty to control the poly-Si EWF because of the Fermi level pinning effect [Hobbs03, Hobbs04_I, Hobbs04_II, Robsertson07] required to find new solutions. High doping concentrations of the poly-Si gate have been achieved revealing that higher doping level doesn't reduce the gate depletion phenomenon. Moreover, parasitic charge centers created at the poly-silicon/gate dielectric interface further degraded the carrier mobility by remote coulomb scattering [Fischetti01, Datta03, Gusev01, Gámiz03]. The necessity to use metallic materials (MG) to replace the historical poly-Si gates became essential to overcome these difficulties [Gusev 06, Bohr 07]. It took ten years before the industry converged on the material and integration first strategy for HK/MG [Bohr 07].

I-2.HK/MG integration challenges

By changing from SiO_2/poly-Si to HK/MG, it was clear for the microelectronic industry that from this moment the CMOS technology scaling will not only be driven by the classical lithography evolution but also it will depend on its ability to find new and innovative materials, to integrate them on a reliable industrial process and to have an advanced understanding of the physical and chemical behavior of these materials.

I-2-a. Metal gate required properties

The metal material must satisfy several criteria in order to be viable for use in a Si-based CMOS fabrication process. Beyond a low resistivity to fit the ITRS specifications in terms of gate sheet resistance, the research was oriented towards metals or metallic materials with: i) the proper nMOS and pMOS vacuum work functions, ii) the thermal and chemical stability toward the underlying dielectrics, iii) the ease of co-integration in a device fabrication process.

The last point means that the metals must be deposited with conventional techniques used by the semiconductor manufacturing (CVD, PVD or ALD) and is compatible with an industrial etch techniques (Dry and Wet).

I-2-b. Integration scheme and MG work function engineering

Two options were finally followed.

In the first one, IBM-led Fishkill alliance (including SAMSUNG, STMICROELECTRONICS, and GLOBALFOUNDRIES) developed the capping layer integration for their 32/28nm HK/MG nodes. This integration uses a high thermal budget process called “gate first” integration process, where TiN is used as a common material deposited on Si/SiON/HfSiON for both nMOS and pMOS sides. Subsequently, very thin capping layers (few Ångström) of aluminum (pMOS) [Jung05] and lanthanum (nMOS) [Narayanan06, Guha07] are deposited and capped by TiN. Finally, the gate fabrication is finished by poly-Si deposition as in figure I-3.l. In this integration scheme, the electrode EWF modulation is based on the diffusion of Al and La to the SiON/HfSiON interface and subsequent dipoles formation during the Source/Drain (S/D) activation annealing [Bosman10]. However, even if the capping layer integration is implemented at the industrial scale for the 28nm (Bulk/FDSOI) node, it appears that it is difficult to control after the S/D activation annealing the interdiffusion of the chemical species present in the HK/MG structure, in particular nitrogen and oxygen (oxygen vacancies in HK) which finally have also a significant contribution in the EWF modulation and EOT regrowth.

In parallel, Intel followed another integration scheme since their 45nm node CMOS technology. This approach is the so-called “gate last” or “RMG” (Replacement Metal Gate) or “damascene” integration process. The key process step for this integration is the replacement of the SiO_2/poly-Si gate after the S/D activation anneal by HK/MG structure with

the adapted gate materials for pMOS and nMOS transistors. After metal gate deposition, the thermal budget is limited to back end of line (BEOL) annealing temperatures which are at maximum 400°C. This opened the door to new choices for the gate materials; in particular new opportunities to integrate highly reactive low work function metals were offered (see § I-3, § I-4). Besides, gate last flow has the benefit to enhance channel strain during the removal of the sacrificial poly-Si gate process step, one of the few strain enhancement techniques that simultaneously improves both nMOS and pMOS electrodes [Auth08, Mayuzumi07]. However, the RMG approach increases process complexity compared to gate first due to additional planarization steps in the front end of line (FEOL) gate process flow (addition of 2 planarization steps: poly open chemical mechanical polishing (CMP) + contact CMP to decontact n and pMOS metal gates). A schematic representation of the capping layer and gate last integration main steps is shown in Figure I-3.II.

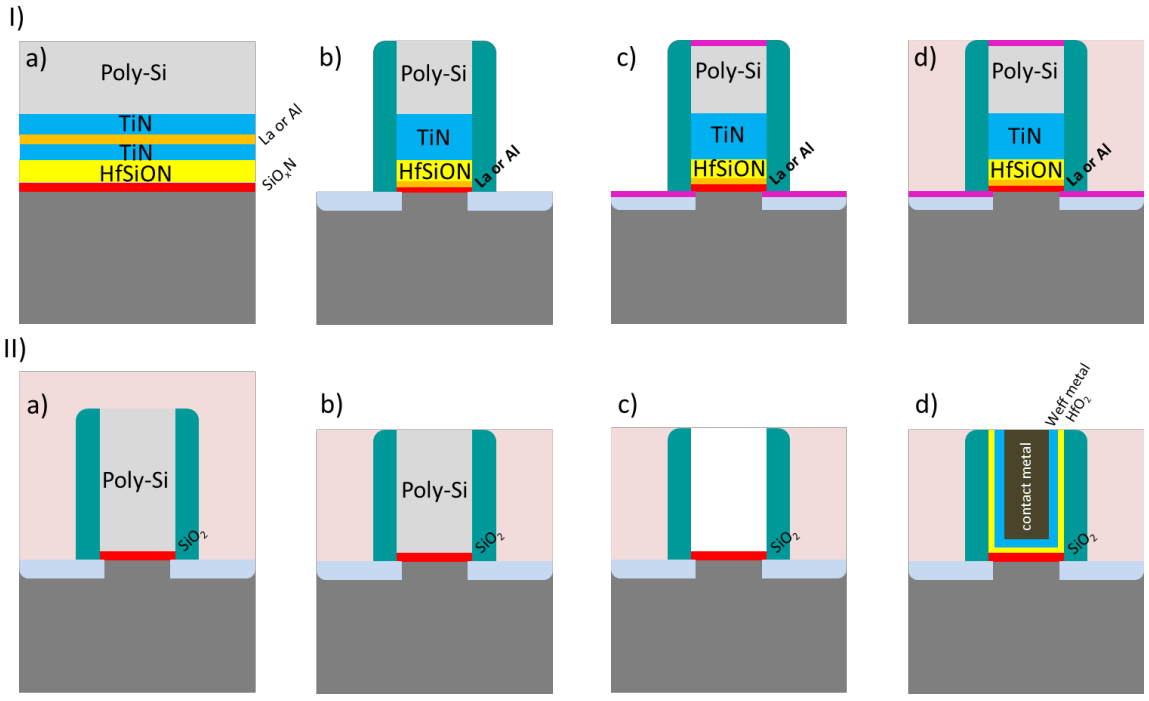


Fig. I-3 *– Scheme of the gate first (capping layer) (I) and gate last (II) main integration steps.*
In the gate first approach: (I-a) deposition of the gate stack, (I-b) patterning of the gate stack, deposition of spacers, ion implantation and S/D activation anneal, high temperature annealing. (I-c) silicide formation for high conductive S/D and top Poly-Si areas, (I-d) several passivation steps, deposition of stress liners prior to Middle-End and Back-End metallization.
In the gate-last process, (II-a) pattern of the poly-Si dummy gate, substrate implantation and activation anneal, dielectric fill (also called flowable oxide), (II-b) Chemical Mechanical Planarization (CMP), (II-c) wet etch (high Si/SiO_2 selective chemistry) of the poly-Si dummy gate, (II-d) conformal deposition of the high-κ (HfO_2), of the work function metal gate and the contact metal; second CMP to planarize and to decontact n and p gates.

In this work, we will investigate MG choices for EWF/EOT modulation in a gate last integration scheme. We explored choices with the perspective of the co-integration of p and nMOS transistors (see Fig. I-4).

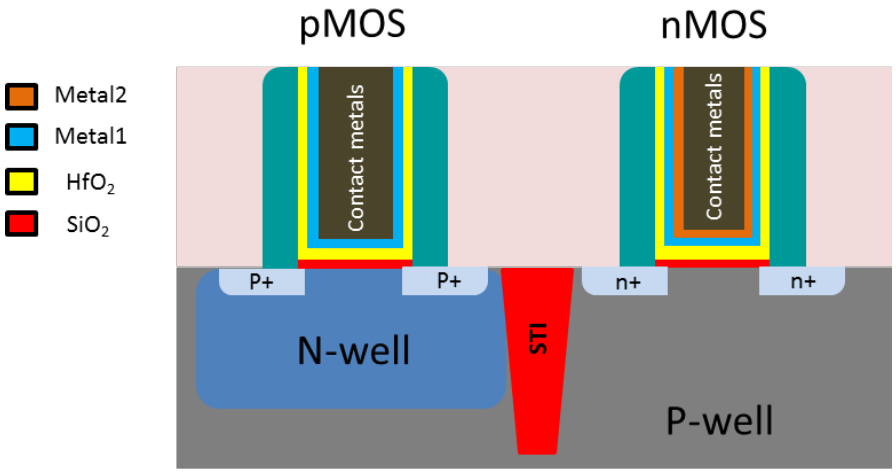


***Fig. I-4** – Co-integration of n and pMOS transistors in the gate last integration scheme*

We will see that the EWF and EOT are closely related but to simplify the understanding of the important parameters (materials and process) that play a part in determining their modulation, we will discuss them separately in the following.

I-3.HK/MG effective work function (EWF) modulation

I-3-a. Definition

The threshold voltage is related to the gate electrode work function by the **flat band** voltage, which is typically the parameter measured from capacitance-voltage (C-V) characteristics.

If there is no charge present in the oxide or at the oxide-semiconductor interface, the flatband voltage (V_{fb}) simply equals the vacuum work function difference between the metal gate (ϕ_m) and the semiconductor substrate (ϕ_s) according to the relation $V_{fb} = \phi_m - \phi_s$ where the vacuum work function is the voltage required to extract an electron from the Fermi energy to the vacuum level (see Fig. I-5).

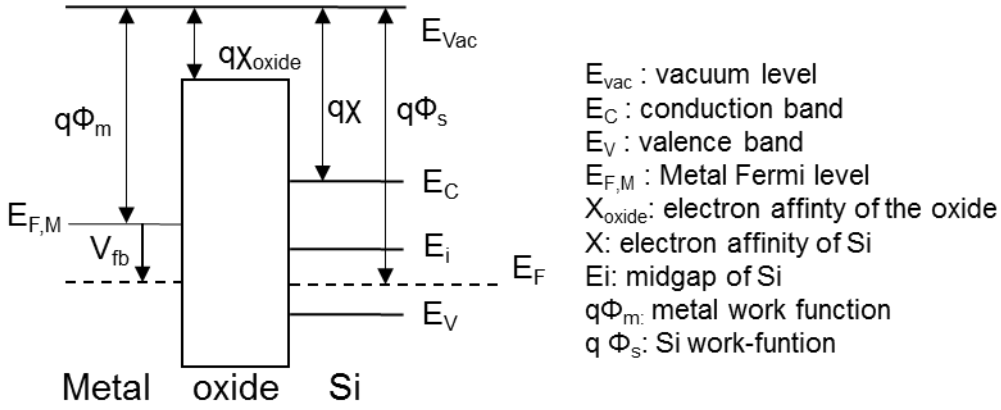


Fig. I-5 *- Flatband energy diagram of a MOS structure at V_g=0, ideal case with no interface/bulk charges.*

In a real MOS as schematically illustrated in figure I-6, V_{fb} depends not only on the intrinsic metal work function and Fermi level position in Si but also on a drop voltage (V_{ext}) due to extrinsic contributions like the fixed charges (ρ_{SiO2}, ρ_{HfO2}), intrinsic charges densities ($Q_{HfO2/SiO2}$, $Q_{SiO2/Si}$), and the dipole ($\delta_{HfO2/SiO2}$, $\delta_{MG/\ HfO2}$) present at their interfaces [Jha04, Han13, Leroux13]. These extrinsic contributions can be dipole formation at interfaces due to charge transfer between the MG and the HK, interface mixing during processing, oxygen or other elements redistribution across the HK/MG interface, compositional variations in electrode material. Therefore, the EWF can be written as:

$$V_{fb} = (\phi_m - V_{ext}) - \phi_s = EWF - \phi_s \quad \text{(Eq. I-1)}$$

The effective work function of the metal gate electrode is the term between the brackets. As ϕ_s is a known parameter related to the substrate doping level, the EWF can then be extracted from the measured V_{fb} value through a time dependent C-V experiment.

The EWF expression can be given by the following general equation:

$$EWF = \phi_m - \int_0^{EOT} \frac{\rho(x)x}{\varepsilon_{SiO_2}} dx + \sum_i \delta_i \quad \text{(Eq. I-2)}$$

where $\int_0^{EOT} \frac{\rho(x)x}{\varepsilon_{SiO_2}} dx$ are the contribution of the fixed charges distributed in the bulk and at interfaces of the oxide with x their distance from the metal gate, δ_i are the interface dipoles contributions.

Using the charge and dipole convention as illustrated in figure I-6, the EWF can be expressed as [Jha04, Han13]:

$$EWF = \phi_m - \frac{1}{\epsilon_{SiO_2}}\left(Q_{SiO_2/Si}EOT + \frac{\rho_{SiO_2}EOT^2}{2} + Q_{HfO_2/SiO_2}EOT_{HfO_2} + \frac{\rho_{HfO_2}EOT_{HfO_2}^2}{2} - \frac{\rho_{SiO_2}EOT_{HfO_2}^2}{2}\right) + \delta_{HfO_2/SiO_2} + \delta_{MG/HfO_2} \quad \text{(Eq. I-3)}$$

where EOT is the equivalent oxide thickness of the stack, EOT_{HfO2} is the equivalent oxide thickness of the HK oxide, $Q_{HfO2/SiO2}$ and $Q_{SiO2/Si}$ are the real charge densities at the HfO_2/SiO_2 and SiO_2/Si interfaces respectively, ρ_{HfO2} and ρ_{SiO2} are the bulk charge densities in HfO_2 and SiO_2 oxides respectively, ε_{SiO2} is the SiO_2 relative permittivity, ε_{HfO2} is the HK relative permittivity, $\delta_{HfO2/SiO2}$ and $\delta_{MG/\ HfO2}$ represent the possible moments of V_{fb} shift caused by the electric dipole at the HfO_2/SiO_2 and MG/ HfO_2 interfaces.

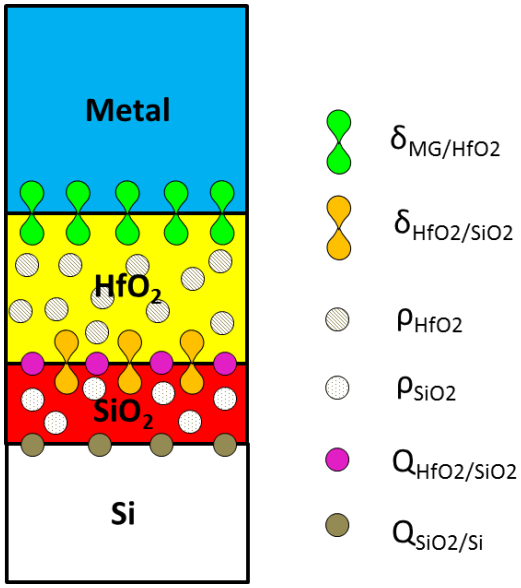


***Fig. I-6** – Schematic representation of a real MOS(Si/SiO_2/HfO_2/MG) with a model of charges location*

First of all, as reported in several literature data, let us consider that the bulk charges in the SiO_2 pedestal (ρ_{SiO2}) and HK oxide (ρ_{HfO2}) are negligible. Indeed, this assumption is based on different observations. First, the linear dependence observed between V_{fb} (or EWF) and EOT implies that the quadratic dependence with EOT does not exist and therefore that ρ_{SiO2} can be neglected (see Eq. I-3) [Jha04, Charbonnier10, Han13]. Second, it is also stated that ρ_{SiO2} and ρ_{HfO2} are negligible compared to the SiO_2/Si and HfO_2/SiO_2 interface charges respectively [Jha04, Wen06, Wilk02, Kerber03]. The minimized contribution of the ρ_{HfO2} is particularly considered true if nanometer thick HK films are considered [Wen06].

This implies that the EWF can finally be simplified as follow:

$$EWF = \phi_m - \frac{1}{\epsilon_{SiO_2}}(Q_{SiO_2/Si}EOT + Q_{HfO_2/SiO_2}EOT_{HfO_2}) + \delta_{HfO_2/SiO_2} + \delta_{MG/HfO_2} \quad \text{(Eq. I-4)}$$

I-3-b. The particular cases of gate first and gate last processes

For the gate first approach, there is a consensus about the main reason of the EWF tuning towards the nMOS and pMOS required values. It results from the La and Al diffusion to the SiO_2/HK interface during the Source/Drain (S/D) activation annealing [Guha07, Bosman10]. *Ab initio* calculations showed also that the elements segregate preferably to the HfO_2/SiO_2 interface and the calculated change in the flatband voltage resulting from this configuration is consistent with experimental observations. It is then proposed that the presence of La or Al at the HK/IL interface is the main origin of V_{fb} shift where La and Al-related dipoles set the EWF of nMOS and pMOS electrodes (Fig. I-7) [Kirsch08, Kita09, Robertson11, Leroux13]. As a consequence, the term δ_{HfO_2/SiO_2} in Eq. I-4 can be considered for the capping layer approach as the main contributor to the EWF tuning **for a given metal electrode (fixed ϕ_m)**. Note that this contribution results from the high enough thermal budget (above 800°C) necessary to allow the diffusion of the La and Al element to the SiO_2/HK interface [Copel09].

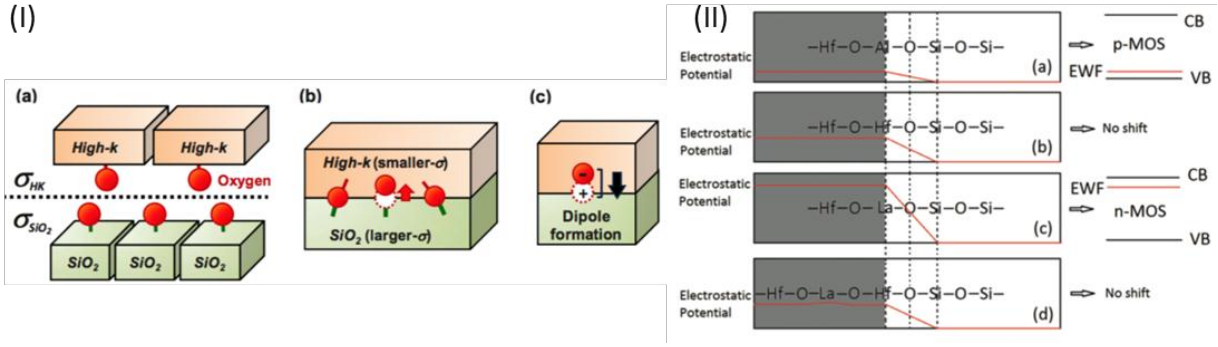


***Fig. I-7** – (I) Schematic representation of dipole formation at the SiO_2/HK interface: (a) oxygen location in SiO_2 and HK with different areal density ($\square_{HK} < \square_{SiO2}$), (b) modification of oxygen atoms position to relax the structure after interface formation between SiO_2 and HK, (c) negatively-charged oxygen ions in the HK and positively charged oxygen vacancy in SiO_2 after oxygen transfer. From [Kita09].*

(II) Electronegativity discontinuity at the SiO_2/HK interface due to the presence of dopant elements (La and Al) generates dipoles, which shift the Valence Band Offsets and thus the EWF. From [Robertson11].

In the gate last approach where temperatures do not exceed 500°C, the diffusion of elements is much more limited in such a way that, generally, the SiO_2/Si and HfO_2/SiO_2

interfaces remain unchanged after the process. In this case, we can consider that the $Q_{SiO_2/Si}$, Q_{HfO_2/SiO_2} and δ_{HfO_2/SiO_2} terms in Eq. I-4 have constant values. This means that in addition to metal intrinsic work function ϕ_m, the main contributor to the EWF tuning is the dipole that can form at the MG/HfO_2 interface. The band-edge work function depends on the vacuum metal work function value ϕ_m(Eq. I-4), which leads to the choice of a relevant metal adapted for an nMOS or a pMOS-type work. This value is modulated by the drop voltage at the MG/HfO_2 interface, which depends on the particular state of this interface [yeo04, Wen11]. These considerations will be the starting point of the discussions presented in chapter III to VI of this thesis work. Metals will be first chosen as a function of their vacuum work function and then the chemical state of the corresponding metal/HfO_2 interface will be carefully studied.

I-3-c. Classification of metals work function

Michaelson from IBM [Michaelson77] reported in a review paper the vacuum work function of pure metals as a function of their atomic number (see Table I-1). This allows classifying the n or p character of pure metals. Metals in columns IIIB, IVB and VB such as Hf, Ti, and Ta exhibit low work functions adapted for nMOS gate electrode on Si whereas VIII columns metals with high work functions such as Ni, Pt, and Pd may be useable as pMOS metal gate.

IA	IIA	IIIB	IVB	VB	VIB	VIIB		VIII		IB	IIB	IIIA	IVA	VA	VIA	VIIA
3	4											5	6			
Li	Be											B	C			
2.9	4.98											4.45	5.0			
11	12											13	14	15	16	
Na	Mg											Al	Si	P	S	
2.75	3.66											4.28	4.85	...	...	
19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br
2.30	2.87	3.5	4.33	4.3	4.5	4.1	4.5	5.0	5.15	4.65	4.33	4.2	5.0	3.75	5.9	
37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I
2.16	2.59	3.1	4.05	4.3	4.6	...	4.71	4.98	5.12	4.26	4.22	4.12	4.42	4.55	4.95	
55	56	57	72	73	74	75	76	77	78	79	80	81	82	83	84	
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At
2.14	2.7	3.5	3.9	4.25	4.55	4.96	4.83	5.27	5.65	5.1	4.49	3.84	4.25	4.22	...	
87	88	89	90	91	92											
Fr	Ra	Ac	Th	Pa	U											
...	...	...	3.4	...	3.63											
			58	59	60	61	62	63	64	65	66	67	68	69	70	71
			Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
			2.9	...	3.2	...	2.7	2.5	3.1	3.0	...	...	...	...	...	3.3
			90	91	92	93										
			Th	Pa	U	Np	...	...	...	...	...	...	...	...	...	...
			3.4		3.63											

***Table I-1** – Vacuum work function and periodicity of elements. From [Michaelson77].*

Some authors explored later the work function of metals when deposited on HK dielectrics [Afanasev02, Yeo02, Yeo04]. The measured values differ significantly from their

values on SiO_2 or in vacuum (see Table I-2). The results were interpreted by applying the interface dipole theory to the MG/HK interface. A dipole can be created at this interface because of the formation of charged metal induced gap states in the dielectric band gap (MIGS) [Heine65, Louie76], which are an intrinsic property of the stack. Later, this model was assumed to predict the EWF for low temperature processed HK/MG but not after high temperature annealing [Gusev06].

Metal/dielectric	Work function (eV)	Barrier height (eV)	Measurement method	Reference
Mg	3.66		Photoelectric effect	16
Mg/Al_2O_3	3.6	2.6	Internal photoemission	7
Mg/SiO_2	3.45	2.5	Internal photoemission	7
Mg/ZrO_2	4.15	2.6	Internal photoemission	7
Ta (polycrystalline)	4.25		Thermionic emission	17
Ta/SiO_2	4.2		MOS capacitor V_{FB}	18
Al	4.28			19
Al/Al_2O_3	3.9	2.9	Internal photoemission	7
Al/SiO_2	4.14		MOS capacitor V_{FB}	6
Al/Si_3N_4	4.06		MOS capacitor V_{FB}	6
Al/ZrO_2	4.25	2.7	Internal photoemission	7
W	4.63		Field emission	20
W/SiO_2	4.6–4.7	3.65–3.75	Fowler-Nordheim tunneling	21
Mo(110)	4.95		Photoelectric effect	22
Mo/SiO_2	5.05		MOS capacitor V_{FB}	23
Mo/Si_3N_4	4.76		MOS capacitor V_{FB}	3
Mo/HfO_2	4.95		MOS capacitor V_{FB}	24
Pt	5.65		Photoelectric effect	25
Pt/SiO_2	5.59		MOS capacitor V_{FB}	6
Pt/HfO_2	5.23		MOS capacitor V_{FB}	26
Pt/ZrO_2	5.05		MOS capacitor V_{FB}	27
Ni(110)	5.04		Photoelectric effect	16
Ni/Al_2O_3	4.5	3.5	Internal photoemission	7
Ni/ZrO_2	4.75	3.25	Internal photoemission	7
Au	5.31–5.47		Photoelectric effect	16
Au/Al_2O_3	5.1	4.1	Internal photoemission	7
Au/ZrO_2	5.05	3.5	Internal photoemission	7
Hf(polycrystalline)	3.95		Photoelectric effect	16
Hf/SiO_2	4.0		MOS capacitor V_{FB}	28

***Table I-2** – Work function (in eV) of different metals in vacuum and when deposited on different gate oxides. From [Yeo02]*

I-3-d. Some integration criteria

Concerning the thermal stability of metals on oxides, several pure metals and some binary/ternary conducting compounds deposited on SiO_2 and Al_2O_3 were evaluated using in situ XRD, resistance, and optical scattering analysis techniques [Cabral04, Gusev06]. The corresponding results are summarized in the periodic table of figure I-8.

Low work function pure metals are intrinsically very reactive with the dielectrics even for low thermal budgets. Conventional CMOS processing that requires temperatures greater than

950°C may not be an integration option for most elemental n-FET electrodes, only low thermal budget processes can be considered.

High work function metals, in particular noble metals, and alloys exhibit higher chemical stability toward gate oxides. But, since they belong to semi-noble or noble metals family, they remain in general incompatible with industrial commonly used etching process (high resistance to wet and dry etching agents), which is an important issue to their integration in a CMOS manufacturing flow. Finally, due to the low abundance in earth's crust (Au, Pt, Rh…), mines extraction induces high cost, which appears also as a limitation to manufacture volume production.

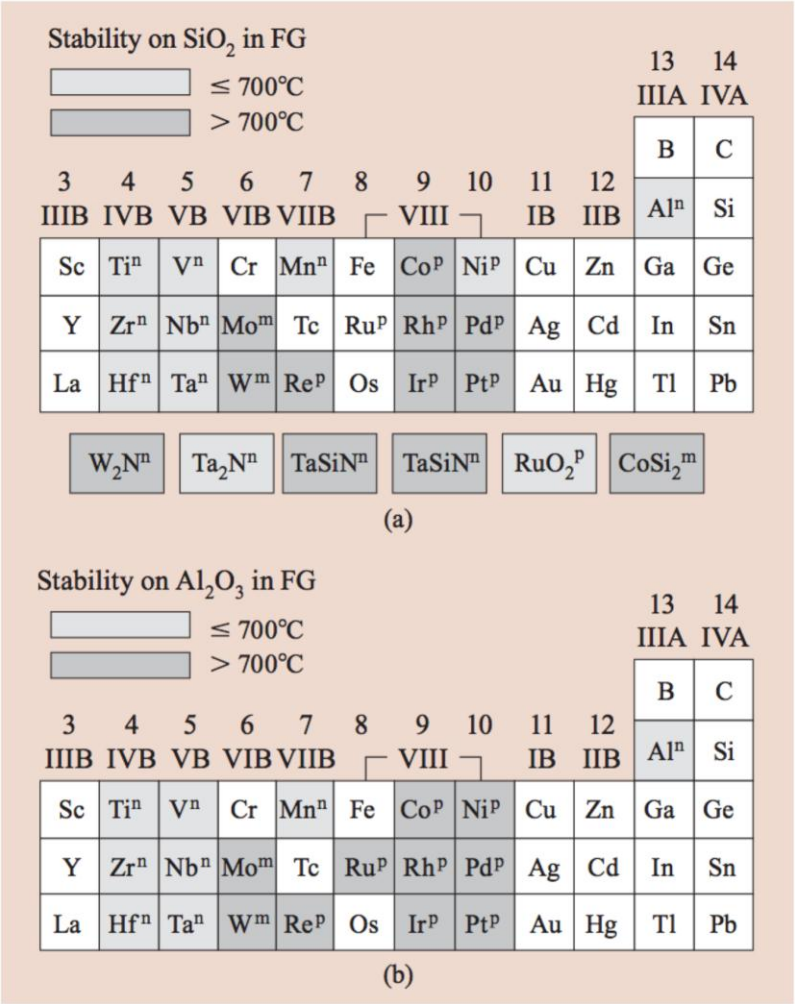


***Fig. I-8** – Periodic table indicating the thermal stability (less than 700°C in light gray or greater than 700°C in darker gray) of electrode materials deposited on (a) SiO_2 and (b) Al_2O_3. Superscripts indicate the type of metal work function (n=nMOS, m=midgap, p=pMOS). From [Cabral04, Gusev06].*

I-4. Choice of MG for gate last integration

I-4-a. Nitride-based

The first proposed metals to replace poly-Si as gate materials were those already used in CMOS Back End Of Line (BEOL) process flow. Hence, refractory Ta and Ti binary nitrides (TaN and TiN), so far used as diffusion barriers to copper in BEOL, have been early studied as gate electrode materials. Chemically stable on gate oxides and compatible with conventional CMOS fabrication process steps, TiN and TaN are very promising MG.

TiN is without any doubt one of the most studied metal nitride, which consequently led to a considerable development in equipment's technologies and deposition techniques such as PVD, CVD or ALD. Depending on the deposition technique, EWF of HfO_2/TiN stack varies from 4.8 to 5.0 eV at moderate temperature [Tai06]. In particular, the deposition of PVD TiN on HfO_2 results on a pMOS-like EWF of about ~4.8eV [Tai06, Veloso11]. This ~0.2eV shift toward p+ regarding silicon midgap has been explained by the presence of a dipole at HfO_2/SiO_2 interface [Charbonnier10]. Thus, deposited on HfO_2 at low temperature, TiN is suitable for FDSOI pMOS architecture where band gap edges constraints in term of metal gate EWF are not severe (+/- 0.2eV around Si-midgap) [Chang00, Majhi05].

With a well-controlled oxidation anneal, Hinkle *et al*. show that the EWF of HfO_2/ PVD TiN could be increased from 4.8eV to 5.1eV to reach the Si valence edge as required for bulk Si pMOS architecture. In this work, it was suggested that O_2 anneal acts on the HfO_2/TiN interface inducing the formation of Hf-N bonds and subsequent electrical dipoles, which results on the gate electrode EWF increase [Hinkle10]. On his side, Westlinder *et al*. show a direct dependence of the EWF on the stoichiometry of TiN_x when deposited on SiO_2 [Westlinder04]. Varying the nitrogen amount in TiN modifies the EWF between 5.0eV and 4.1eV, which makes TiN_x adapted for SiO_2-based p ($x \geq 1$) or nMOS ($x << 1$) transistors. Similar approaches using nitrogen amount variation in ternary $TiAlN_x$ on SiO_2 [Cha02] or $TaAlN_x$ nitrides on SiO_2 and HfO_2 [Alshareef06] result also in nMOS ($x << 1$) and pMOS ($x \geq 1$) adapted EWF. These studies pointed-out the importance of nitrogen amount control in binary or ternary nitrides on the EWF modulation.

At the same time as this thesis work, few studies proposed to add a low work function metal on top of the HK/pMOS TiN MG electrode in order to achieve an nMOS adapted EWF. Al [Hinkle12] and TiAl [Veloso11, Veloso13] metals were used. The diffusion of the low work

function Al towards the HfO_2/TiN interface in conjunction with low O concentration in the TiN is proposed as enabling the low EWF. Al addition into the TiN MG has also been considered and the resulting low EWF explained by Al-based dipole and O vacancy models [Nakamura11]. To our knowledge, no further investigations were conducted on these systems. It is the purpose of chapter III to V to investigate systematically and thoroughly the distribution of elements (Ti, Al, N and O) and the bonds they form in HfO_2/TiN/Ti, HfO_2/TiN/Al, HfO_2/TiN/TiAl and HfO_2/$TiAlN_x$ stacks, successively. These investigations will be conducted in parallel with electrical measurements with the aim to control the EWF and minimize the EOT by improving our understanding of the mechanisms involved in the establishment of these parameters. This is mandatory for metal gate integration in CMOS devices.

I-4-b. Pure metals alloying

Besides of the classical materials (TaN, TiN) already used in CMOS technology, pure metals have been studied when deposited on SiO_2 with low thermal budget for both n and pMOS transistors integration.

Tsui *et al*. studied the alloying of Ta with high work function Pt and low work function Ti. The binary metal systems Ta_xTi_y and Ta_xPt_y were deposited on SiO_2. Their composition was varied in order to observe the EWF modulation of the corresponding SiO_2/Ta_xTi_y and SiO_2/Ta_xPt_y gate stacks [Tsui03]. Using $Ta_{63}Ti_{37}$ results in a bulk nMOSFET adapted EWF of 4.2eV after annealing at 400°C. Complementarily, using $Ta_{58}Pt_{42}$ results in a bulk pMOSFET adapted EWF of 5.05 eV. Moreover, annealing at higher temperatures of both SiO_2/$Ta_{58}Pt_{42}$ and SiO_2/$Ta_{74}Pt_{28}$, at T=600°C, results in complementary 4.8 and 4.4eV EWFs adapted for thin body CMOS technologies integration.

On the other hand, Nickel based SiO_2/Ta/Ni and SiO_2/Ti/Ni gate stacks have been studied with a focus on interdiffusion mechanisms impact on the EWF modulation. First study shows that Ni deposition on SiO_2/Ta have a low impact gate electrode EWF variation with only 0.1 eV EWF increase compared to SiO_2/Ta reference, despite the diffusion of Ni to SiO_2/Ta interface. This has been assigned to an undesired reaction between Ta and SiO_2, which pins the electrode EWF close to Ta work function values [Matsukawa05]. In the case of Ni deposition on SiO_2/Ti electrode, no reaction between Ti and SiO_2 is evidenced and Ni segregation at SiO_2/Ti interface results on a 1eV EWF shift going from 4.1eV for SiO_2/Ti to

5.1eV for SiO_2/Ti/Ni electrode [Polishchuck01]. These studies show that alloying high work function Pt or Ni with low work function metals such as Ti or Ta is a promising approach for p and nMOS co-integration.

In chapter IV of this work, we will investigate for the first time the effect of alloying high work function Ni with low work function Ta and Ti on the EWF modulation and the EOT scaling of HfO_2-based stacks.

I-5. HK/MG equivalent oxide thickness (EOT) scaling

Another important criterion for the metal gate material selection is its thermodynamic stability toward oxygen present in the SiO_2 interlayer (IL) and the high-k HfO_2-based insulator. Indeed, the equivalent oxide thickness (EOT), which has to be minimized, is directly dependent on this stability.

The equivalent oxide thickness (EOT) is a length, usually given in nanometers (nm), which indicates how thick a silicon oxide film would need to be to produce the same capacitance as the HK material being used. It is a material parameter independent of quantum confinement and polySi depletion. These contributions are taken into account in the Capacitance Equivalent Thickness (CET) of a MOSFET transistor measured in inversion and defined as follows: CET ≈ EOT + 0.3nm.

A gate oxide composed of a pedestal SiO_2 IL and a HK dielectric is characterized by the following EOT:

$$EOT = t_{SiO2} + t_{HK} \frac{\varepsilon_{SiO2}}{\varepsilon_{HK}} = EOT_{SiO2} + EOT_{HK} \quad \text{(Eq. I-5)}$$

where ε_{SiO2}, ε_{HK} and t_{Si}, t_{HK} are the permittivity and physical thicknesses of the SiO_2 IL and the HK respectively.

Continuous MOS scaling induces the reduction of EOT value in order to increase devices performance. The EOT of the first generation HK/MG (45 nm node) was around 1 nm. Now, above the 32 nm node for planar MOS and even above the 22 nm node for ultra-thin SOI (UTSOI), the requirement is sub-nm EOT. From Eq. I-5, we can deduce that the reduction of the EOT can be achieved through three approaches: i) increase the dielectric constant of the HK oxide, ii) increase the dielectric constant of the IL, iii) and/or reduce the IL thickness.

I-5-a. Dielectric constant of the IL and the HK

In the case of HfO_2, EOT scaling has been achieved by increasing the dielectric constant of HfO_2 oxide using a nitridation process with the formation of a ternary HfON compound. The use of nitrogen diffusion from HfN nitride to HfO_2 in $Si/SiO_2/HfO_2/HfN$ stack is an example of such an approach [Choi10]. Another way concerns the stabilization of the higher-k phases (tetragonal and cubic) by doping HfO_2 with elements such as zirconium, yttrium and silicon [Hedge05, Kita06, Tomida06, Fischer08, Ando12]. A moderate k value ranging between 20 and 30 is required because of the tradeoff between the k value and the band gap, which has an inverse dependence on k. Eq. I-5 indicates that the contribution to the EOT of a 2nm-thick HK film with a permittivity of 25 is 0.31nm. This defines the reasonable lowest contribution of the HK to the EOT without noticeable degradation of the transistor performances.

The permittivity of the IL can be enhanced by La diffusion towards the SiO_2 IL after high temperature anneals through La silicate formation [Copel09]. It was recently shown that a thin epitaxial strontium oxide (SrO) interfacial layer prior to HfO_2 deposition results in EOT of 0.50 nm and 0.60 nm for gate-last and gate-first integrations, respectively [Marchiori11, Frank11].

I-5-b. Remote scavenging

To have an efficient EOT scaling of the gate electrode, it is necessary to think first about a way to limit unwanted regrowth of IL oxide or even better to reduce its thickness during thermal process.

One method for IL thickness reduction consists in the incorporation of an oxygen scavenging material in the gate electrode. Regarding the location of the incorporated scavenger element in the gate stack, we can distinguish two different scavenging techniques: direct and remote scavenging.

Direct scavenging of SiO_2 IL consists in the incorporation of the scavenger directly in the HK layer. An advantage of this technique is the low driving force required to induce IL scavenging which enables the use of weak scavenger materials such as Ta. However, the use of this scavenging technique may impact negatively different gate electrode characteristics such as undesirable variation of the gate EWF due to the formation of fixed charges in the HK and interface dipoles [Ando12].

On the other hand, remote scavenging consists in the deposition of a scavenging layer not directly on the HfO_2 gate oxide but on a metal, which is thermally stable on HfO_2 (ex: classical binary nitrides such as TiN, TaN or innovative materials such as Ni, Ta) [Ando12]. The result is the IL scaling without the diffusion of the scavenger in the HK layer. This scavenging technique enables aggressive EOT scaling without the degradation of the gate EWF, carrier mobility or leakage currents. In this work, we used remote scavenging technique for IL thickness reduction by the deposition of scavenger element on HfO_2/TiN (chapter III), TaN or Ni (chapter VI).

The reduction of SiO_2 IL thickness by a scavenging metal (M) obeys to the following thermodynamic reaction:

$$2\frac{x}{y}M + SiO_2 \rightarrow Si + \frac{2}{y}M_xO_y \qquad \text{(Eq. I-6)}$$

The choice of the scavenger depends mainly on the Gibbs free energy for the M_yO_x oxide formation. This defines the driving force for the O scavenging reaction. Figure I-9 shows the Ellingham diagram, i.e. Gibbs free energy of formation vs. temperature, for Ta_2O_5, TiO and Al_2O_3 oxides compared to the one of SiO_2. The energies were normalized to the reaction of a single oxygen atom. We observe that ΔG_{Al2O3} and ΔG_{TiO} are lower than ΔG_{SiO2}, which suggests that Ti and Al are able to reduce oxygen from SiO_2 IL, whereas ΔG_{Ta2O5} is higher than ΔG_{SiO2}, which indicates that Ta does not scavenge oxygen from SiO_2 IL. Note that HfO_2 is the most stable of these oxides. Scavenging has been reported through thin HfO_2 layers [Kim04]. Oxygen diffusion through the layers is fast being mediated by oxygen vacancies with a quite rapid kinetics [Goncharova06, Zafar 11].

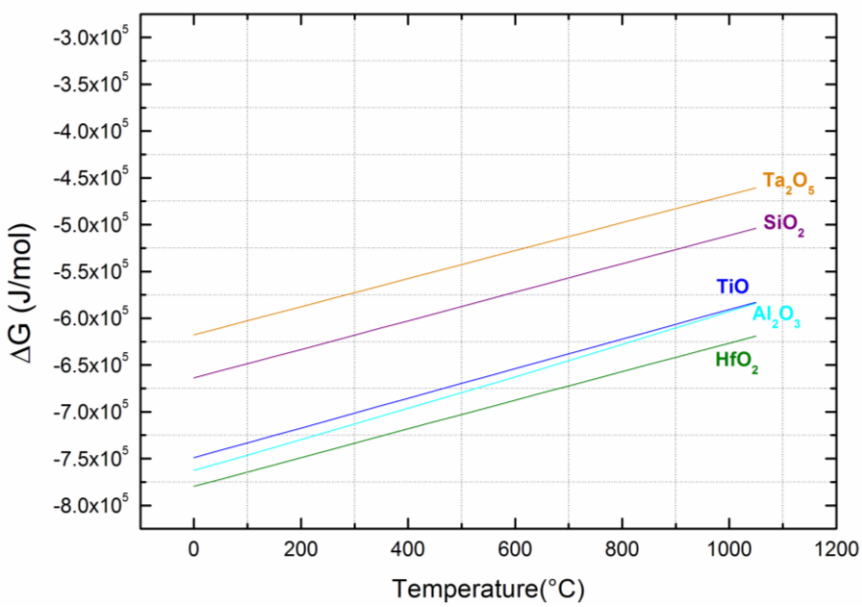


***Fig. I-9** – Ellingham diagram of the Gibbs free energy of formation vs. temperature for Hf, Ti, Al, Si and Ta oxides.*

Kim *et al*. shows the reduction of SiO_2 IL by remote scavenging using deposition of Titanium or Aluminum on $Si/SiO_2/HfO_2$ and $Si/SiO_2/ZrO_2$ stacks, for low thermal budget [Kim04]. This work pointed out the different behaviors of Ti and Al regarding the SiO_2 IL, Ti being a stronger O getter compared to Al. Indeed, titanium has favorable Gibbs free energy change and high oxygen solubility. However, no clear chemical mechanism was given to understand the different behaviors of Ti and Al regarding oxygen. In addition, the very low thermal budget used for this study (T=300°C) is not representative of both gate first and gate last integrations schemes. Recently, aluminum has been proposed as an oxygen scavenger in $Si/SiO_2/HfO_2/TiN/NiSi/Al$ stack in gate first approach [Nichau13]. Aggressive scaling of EOT, 0.46nm, has been obtained thanks the thermal budget and TiN layer thickness optimization which enables low diffusion of aluminum to the HfO_2 oxide while keeping significant oxygen scavenging from the SiO_2 IL.

In chapter III to VI of this work, in addition to the Gibbs free energy of MO_x formation compared to the SiO_2 one, we will consider other thermodynamic parameters to understand the mechanisms responsible for the EOT scaling. This will enable efficient EOT scaling for a final CMOS device integration.

I-6.Thesis chapters organization

This thesis work is mainly focused on developments of gate materials with sub-nm EOT control and EWF tuning in the frame of the gate last approach for planar CMOS devices. For this, we first performed material investigations at the nanometer level of different chosen HfO_2/MG stacks (MG: nitride-based or alloys) and electrical characterization of the corresponding capacitors. Then, we correlated these experimental results on the basis of thermodynamic considerations in order to understand the mechanisms responsible for the modulation of the EOT and EWF.

In chapter II, we present the material and electrical characterization techniques used in this work. We will discuss the suitability and the contribution of each preparation and characterization technique regarding the materials and studied gate structures. In addition, the work method based on the systematic characterization of the studied structures and combination of characterization techniques will be presented.

We notice that in the gate last integration scheme, the maximum thermal budget is limited to T<500°C which induces low interdiffusion of the chemical species in the gate electrode. As a consequence, the EWF engineering in mainly driven by the chemical species diffusion at the HK/MG interface and the EOT scaling is achieved only by remote scavenging technique.
The chapter III will address the EWF modulation of HfO_2/TiN stack by low work function Ti and Al metal deposition. The chemical mechanism of EWF modulation and the metal electrode stability toward gate oxide will be investigated. The first part of chapter IV deals with HfO_2/TiN EWF modulation by TiAl metal alloy deposition. Using the conclusions of chapter III, we will try to understand the effect of Ti and Al alloying in a TiAl monolayer on electrode EWF modulation and EOT scaling. In the second part of this chapter, variation of nitrogen flow during $TiAlN_x$ direct deposition on HfO_2 will be achieved to modulate the HfO_2/$TiAlN_x$ electrode EWF. Same systematic characterization path than HfO_2/TiN/(Ti, Al) will be followed to understand the impact of nitrogen modulation on the metal electrode chemical stability and EWF variation. In Chapter V, the thermal stability (T≤700°C) of these potential electrodes materials will be investigated.

Chapter VI will address combination of pure metals like Tantalum, Nickel and Titanium as innovative gate electrode materials for HfO_2. Here again materials inter-diffusion, particularly

the case of high and low work function metals alloying, is investigated with a particular attention to their impact on the EWF modulation. This will be coupled to the evaluation of the material stability toward oxygen for EOT scaling. The thermal stability of these materials on HfO_2 will be also evaluated.

Chapter II

Nanoanalytical tools for the study of interdiffusion in high-k/metal gate stacks

II-1. Introduction

As presented in the previous chapter, advanced CMOS integration nodes require the use of high-k/metal (HK/MG) gate stack to avoid parasitic phenomena such as gate poly depletion and gate oxide leakage current [Green01, Chang99, Wilk01]. In addition, the reduction of gate electrode dimensions (length, width and height) imposes a drastic reduction of deposited materials thicknesses to guarantee an optimal filling of the gate cavity. Hence, the characterization tools of such systems with very small volumes of different materials must be adapted to enable the observation of weak chemical interdiffusion phenomena occurring during the fabrication process. In addition, samples preparation for the different characterization techniques must be developed and optimized for these damascene full metal gate structures.

In this chapter, we present the different characterization techniques used for HK/MG gate stacks investigations. We will evidence the relevant information they bring for the understanding of the chemical state of the fabricated stacks, the results being a support to discuss the electrical performances. We will also present innovative samples preparation techniques developed in order to have an easy access to the characterization of the HK/MG interface, which is of prime interest in the case of gate last processed stacks.

II-2. X-ray reflectivity

X-ray reflectivity (XRR) is dedicated for the characterization of thin films and multilayers with thicknesses in the range 1 to 300 nm. XRR technique enables the measurement of three parameters: the thickness, the density and the roughness of the films. The operating principle of XRR is based on the reflection of a beam of x-rays from a flat surface and the measurement of the intensity of x-rays reflected in the specular direction.

XRR analysis presents several advantages:

- it is a non destructive technique which enables to reuse the samples for other type of analysis or additional process steps. This enables its introduction as a control analysis technique in a CMOS production flow;
- metallic films (opaque materials) with thicknesses up to 300nm can be analyzed;
- it is a relatively quick analysis technique compared to cross sectional TEM or SEM imaging.

For films with multiple layers, the reflected X-rays from the layers interfaces result in the formation of oscillations, which depend on the thickness, the density and roughness of the deposited layers (Fig. II-1). To determine the thickness of each layer in the stack, the Jordan Valley JVXRR© software is used to fit the XRR spectra. À priori knowledge of the nominal thicknesses is necessary to be able to build the best description of the stack. In addition, the identification of a rough film within the stack is not possible by XRR analysis alone. It requires the use of complementary characterization technique. The typical case of rough layer identification in a stack will be shown in chapter III.

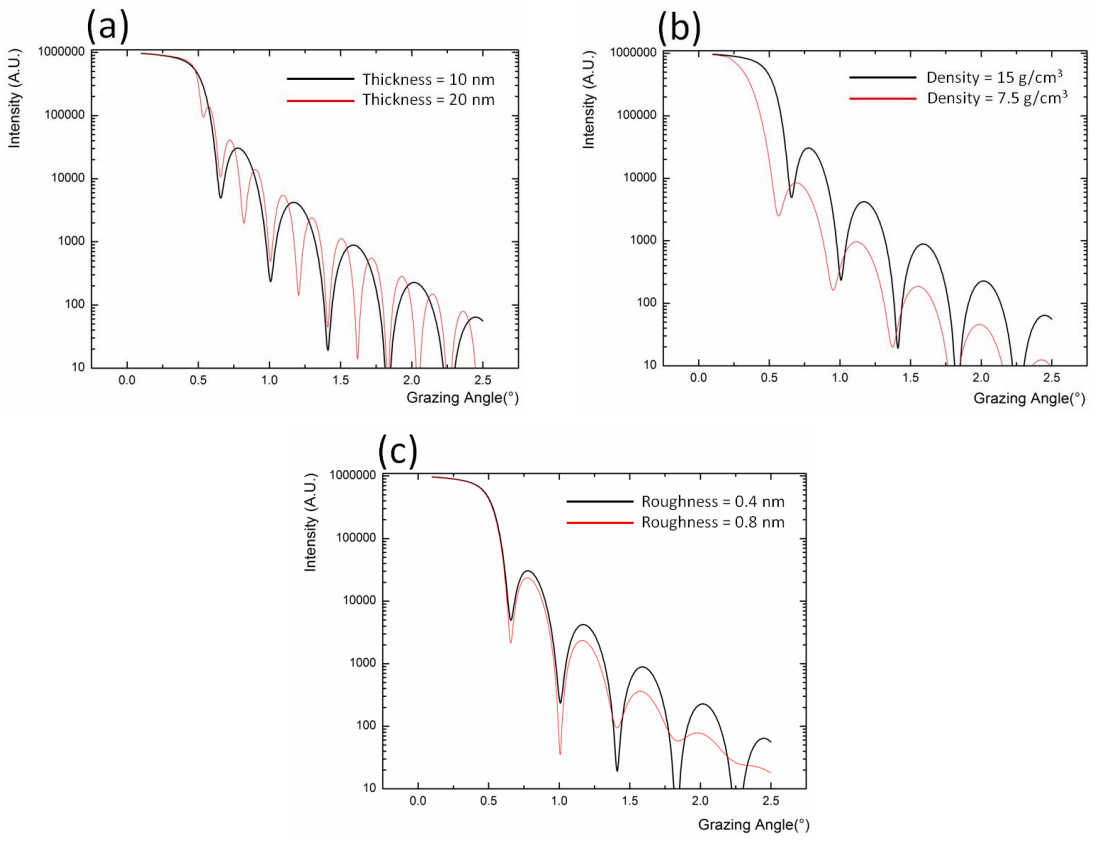


***Fig. II-1**- XRR of Ta films on a Si substrate for different (a) thicknesses, (b) densities and (c) roughnesses*

In this work, XRR analysis has been performed by measuring 49 points on 200 or 300mm full sheet wafers with an XRR spot irradiating areas of about 100 µm by 3-6mm [Agnihotri03] in order to validate the thicknesses of the deposited thin films and check their roughness.

II-3. Transmission Electron Microscopy (TEM)

TEM is a technique dedicated for examining materials at very small scales from micrometer to the atomic scale using an electron probe and exploiting electron-mater interactions. TEM will be used to image directly the whole stack to be studied with the aim to identify each layer of the stack in terms of thickness and chemical state.

The high-resolution mode (HRTEM) with an aberration-corrected (Cs-corrected) objective lens will allow examining atomic structure in the layers and at their interface.

The energy dispersive X-ray (EDX) analysis will be mainly used to identify the elemental distribution in the different layers. In particular cases, it will be replaced by electron energy-loss spectroscopy (EELS). In both cases, a nanometer-sized probe is focused on the sample and scanned over the sample area of interest (STEM: scanning TEM). At each focused point, an EDX/EELS spectrum is collected.

These techniques are nowadays well documented in dedicated reference books [Reimer 2008, Egerton 2011, Goldstein03]. In the following, only particular details associated to specific instrumentations and methods recently developed are underlined in relation with the objectives of this thesis work.

II-3-a. Cs-corrected HRTEM imaging

Spherical aberration (Cs) is responsible for the blurring of images constructed by optical devices such as lenses, mirrors. Figure II-2 illustrates the spherical aberration introduced by a convex optical lens. With a perfect lens, all the rays emerging from the object point A have to focus at the image focal point A'. With a real lens, high angle rays prematurely focus at point A''. The different rays do not meet after the lens in one focal point so that the object point A appears blurred in the image plane because of the presence of spherical aberration.

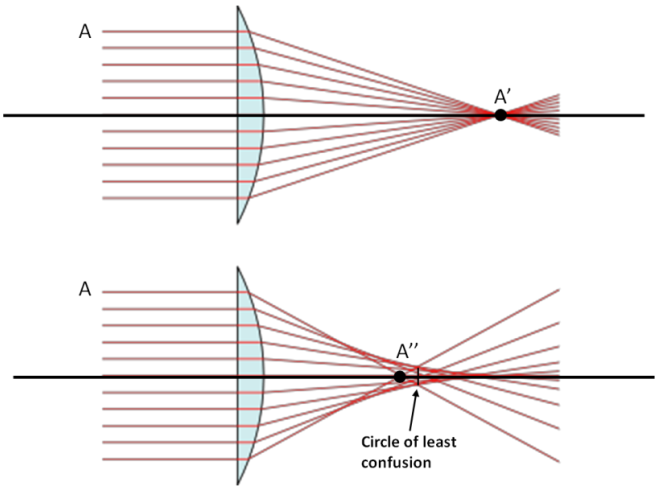


***Fig. II-2**- Rays paths for a perfect lens (top) and a real lens with spherical aberration (bottom)*

The same physical phenomenon is observed with the magnetic lens (objective lens) used in a transmission electron microscope (TEM). The correction of this phenomenon is based on the introduction of a negative spherical aberration, which compensates the positive aberration of the microscope objective lens [Haider98].

In this work, where stacks with different thin layers are studied, the use of a spherical aberration corrected microscope (Cs-corrected TEM) reduces substantially contrast delocalization at interfaces as illustrated in Figure II-3 for a Si/Si-based low-k/La-based high-k stack [Inamoto10]. Aberration makes difficult the identification of the different interfaces between the layers in the stack. This is rather well reduced with the use of a Cs-corrected microscope.

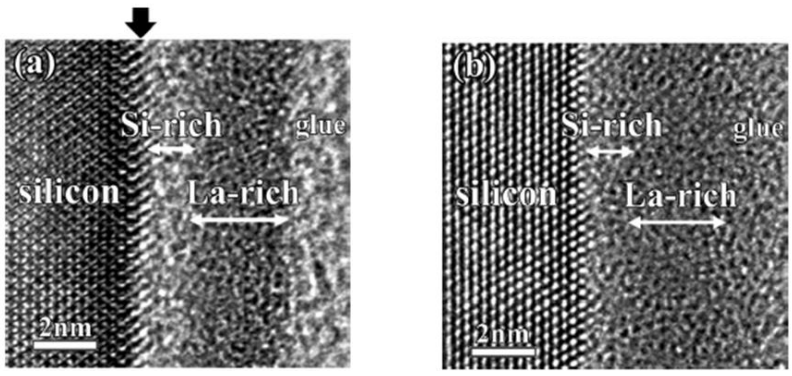


***Fig. II-3**- High-resolution images of a Si/Si-rich oxide/La-rich oxide stack using (a) a conventional TEM and (b) a Cs-corrected TEM*

For the present work, the use of a Cs-corrected TEM - the FEI Tecnai F20 installed at CEMES - is mandatory to identify clearly each layer of the gate stack. It will also be useful to measure the local thickness of each layer (t_{SiO2} and t_{HfO2}) and compare them with the more macroscopic XRR measurements. This will give an additional insight for the estimation and comparison of the corresponding calculated EOT (EOT = t_{SiO2}+ t_{HfO2} x 3.9 /k_{HfO2}) and the electrically determined EOT from C-V experiments (cf § II-8). The observed samples are prepared as cross sections. When a sample is observed in TEM, it is oriented in such way that the electron beam is parallel to the Si/electrode interface and to a particular zone axis of the substrate.

II-3-b. Chemical analysis by STEM-EDX (Energy Dispersive X-rays)

EDX analysis is based on atoms ionization by a focused electron beam. The ionization of the atoms results in two physical phenomena, which compete to bring ionized atoms energy to a stable level. The first effect is the emission of Auger electrons and the second effect is the emission of X-photons coming from K, L, M energy levels of atoms. As the energy of the emitted photons associated to the energy difference between the initial (excited) and final (stable) state is characteristic of the analyzed element, Auger/EDX allows the elemental composition of a sample to be measured. Classically, Auger is more dedicated for light elements (Z below 20) and EDX for heavier elements. In the experiment, a detector measures the number and energy of the X-rays emitted from the analyzed sample. A small electron probe is scanned over the sample along a line of interest (for examples-, across the gate stack from the substrate to the top surface) or over a selected area. Then, the data are treated in order to extract a profile or a map of the elemental distributions. The STEM-EDX profiles are determined from a Cliff-Lorimer quantification method based on the ratio of the X-ray peak intensity [Cliff75]. In the case of a sample composed of A and B elements, the relationship between the X-ray intensities I_A and I_B and the concentration C_A, C_B of element A and B respectively is given by equation II-1:

$$\frac{I_A}{I_B} = \kappa_{AB} * \frac{C_A}{C_B} \qquad \text{(Eq. II-1)}$$

where κ_{AB} is a sensitivity factor used by Esprit © analysis software. Practically, the software fits the peaks corresponding to the elements of interest using Gaussians with theoretically calculated height and width to provide elements quantification.

Tecnai OSIRIS©, Super-X technology for STEM EDX analysis

The Tecnai OSIRIS© (Fig. II-4) installed at STMicroelectronics is used for the STEM-EDX investigation. It is a transmission electron microscope optimized for EDX chemical analysis because of a high brightness, small size and highly stable X-FEG source and 4 new generation SDD (silicon drift detector).

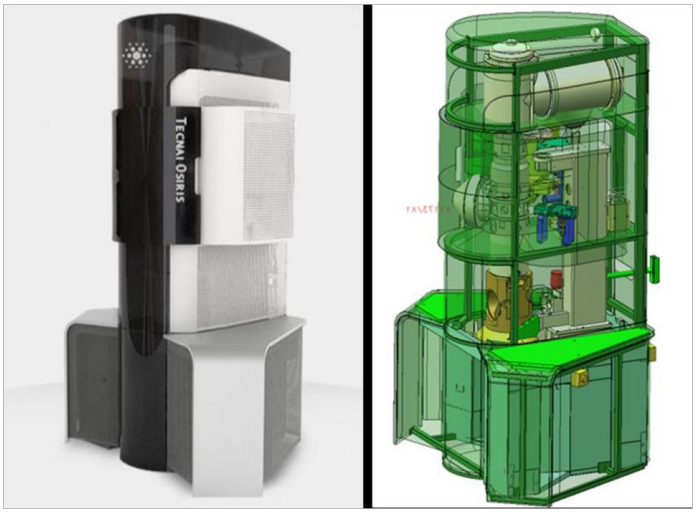


***Fig. II-4**- Image and intern structure of a Tecnai OSIRIS© microscope.*

The X-FEG source has brightness 3.6 orders of magnitude higher than a classical Schottky-FEG source like the one of the Tecnai F20 microscope used for HRTEM. The use of such a TEM source enables the formation of very small probe (about 0.4 nm in diameter) with sufficient current to generate a high amount of electrons with a reasonable exposition time. After the interaction of the STEM electron beam with the TEM lamella, we estimate the resolution of STEM-EDX analysis to be about 1nm.

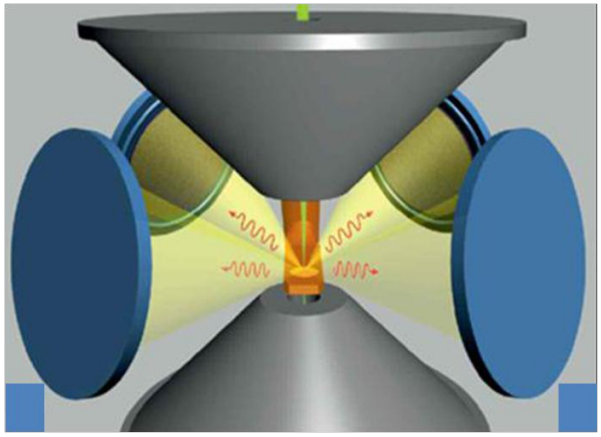


***Fig. II-5**- scheme of the Osiris 4 SDD detectors [Schlossmacher10].*

In addition, the use of 4 new generation SDD detectors (Fig. II-5) instead of one presents several advantages:

- SDD detectors have counting rates 5 magnitudes higher than Si (Li) detectors (600k c/s), which limits dead time (photon emitted but not counted by the detector);
- use of thin silicon layer in SDD (8 magnitude lower than for a classic Si (Li) detector) minimizes the escape peak parasitic effect, then enables the detection of light elements such as carbon or boron (up to 50% concentration);
- multi SDD detector improves the solid angle of collection from 0.15 to 0.9 Sr, which increases the collected photons amount from the analyzed sample [Schlossmacher10].

To highlight the importance of high source brightness, small probe and multi-SDD detectors combination for the studied samples here, we performed a comparison between a STEM-EDX analysis with the Tecnai Osiris (at ST) and a conventional Tecnai F20 (at LETI) equipped with FEG Schottky electron source and a more classical single Si (Li) diode X-ray. Same sample consisting in a gate stack with the following structure: $Si/SiO_2/HfO_2/TiN/Al/TiN/W$ have been analyzed with the two microscopes. The STEM-EDX analyses in each TEM have been performed with the parameters presented in Table II-1.

Parameters	Tecnai OSIRIS	Tecnai F20
Probe size	≤1nm	>1nm
Point number	2D mapping 151x251 pts	1D Line profile 100 pts
Acquisition time	1.52 min	10 min

Table. II-1*- STEM EDX profiles acquisition parameters for Tecnai Osiris and Tecnai F20*

Figure. II-6 shows the STEM-EDX maps and corresponding profiles across the stack obtained with the Tecnai Osiris and the conventional Tecnai F20. The collection time being largely reduced with the Tecnai OSIRIS, it is possible to obtain maps from large field of view with a duration that is even smaller than the one necessary to collect a single line with a standard machine. With the Tecnai OSIRIS, the profiles are obtained over about 35 nm length going from Si substrate to W metal plug by integrating the intensity along a direction parallel to the Si/gate stack interface over tens of nm (14 nm for the rectangle on Fig. II-6(a)). In the case of the Tecnai F20, STEM EDX acquisition is achieved using 1D line profile of about 38 nm length going from Si substrate to the W metal plug (see Fig. II-6 (c)).

For each element of interest, the K, L, M rays going from 0 and 40KeV are taken into account with a minimum resolution of 10eV for each core level ray provided by Brucker Spirit© software. In the case of the Tecnai F20, the STEM EDX spectrum is acquired and analyzed with TEM Imaging & Analysis© software.

Profiles are smoother in the case of the analysis on the Osiris microscope and, in addition, we can reasonably place the position of the interfaces between each layer, which is not always the case for the analysis on the F20 microscope. Indeed the higher performances of the equipment on the Osiris microscope allow an improved sampling of the data (x2.5) and a shorter time of acquisition (5x less). Another important point, which is mandatory for the study of stacks which contains heavy but also light elements, is the better sensitivity for light elements (oxygen and nitrogen) of the Osiris microscope because of the combination of high brightness source and 4 SDD multi detectors. Moreover, the use of the Brucker© EDX data processing software enables the separation between titanium and nitrogen low energy peaks by specific operation. The N and Ti separation has been validated on test samples by comparison to a STEM-EELS analysis where N and Ti are perfectly separated. However, the software performs no separation between Si and Hf profiles. This is the reason why Si profile is removed from the STEM-EDX analysis presented in this work.

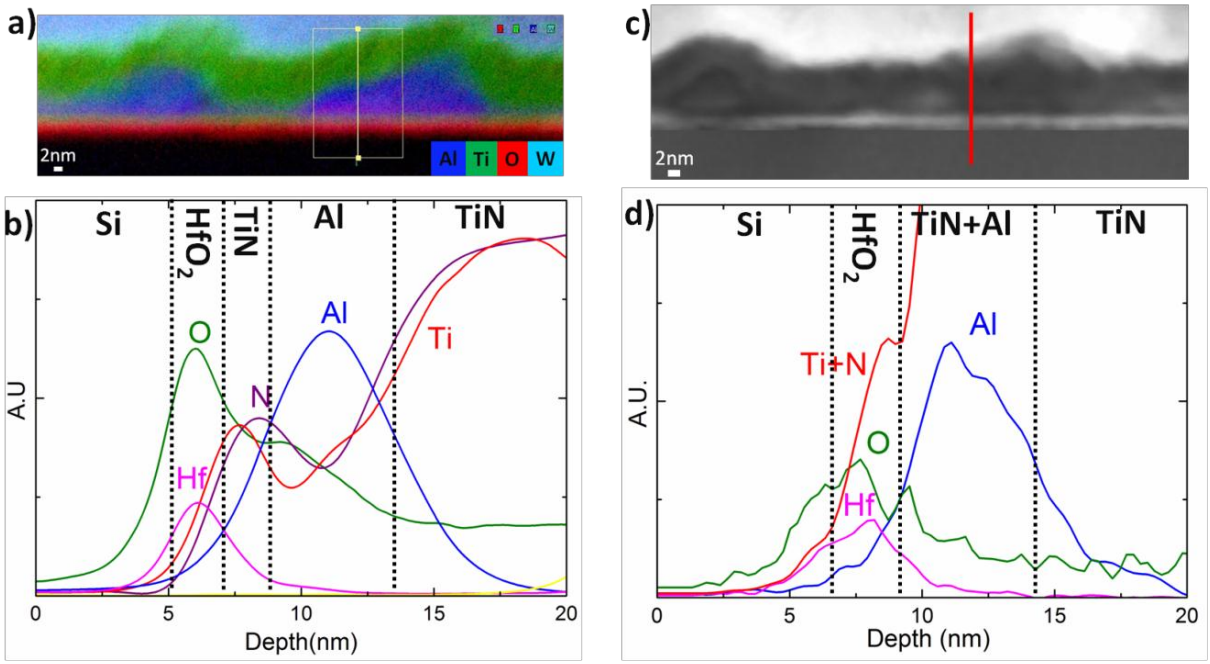


Fig. II-6- *STEM-EDX profiles of Si/SiO_2/HfO_2/TiN/Al/TiN/W performed (b) with a Tecnai Osiris and (d) with a conventional Tecnai F20. Profiles are obtained in (b) by integration of intensity over 14 nm along the Si/gate stack interface as indicated by the rectangular area of the corresponding STEM-EDX map (a) and in (d) are obtained from intensities collected along the red line on the HAADF image (c). Vertical lines are proposals for the location of interfaces between each layer.*

In addition to this, we developed a specific methodology, which took advantage of the high sensitivity for oxygen of the TEM Osiris and of the directly interpretable HRTEM images obtained on the Cs-corrected microscope. This method was useful for the qualification of the state of the low-k SiO_2 interfacial layer (IL) between the Si substrate and the HfO_2 layer. As shown on figure II-7, we observed that the misalignment of Hf and O EDX profiles is directly connected to the thickness of the SiO_2-IL as imaged by HRTEM with a white band between the crystalline Si substrate and the dark amorphous HfO_2. As soon as the thickness of the IL is below 0.7 nm, Hf and O profiles are aligned (Fig. II-7 left case). Then, increasing IL's thickness increases the shift between the position of the maxima of the Hf and O peaks (Fig. II-7 middle and right cases). Therefore, simply looking at the Hf and O profiles allows a quick and relevant estimation of the thickness of the IL, which is directly related to electrical EOT and to the oxygen scavenging by metal electrode.

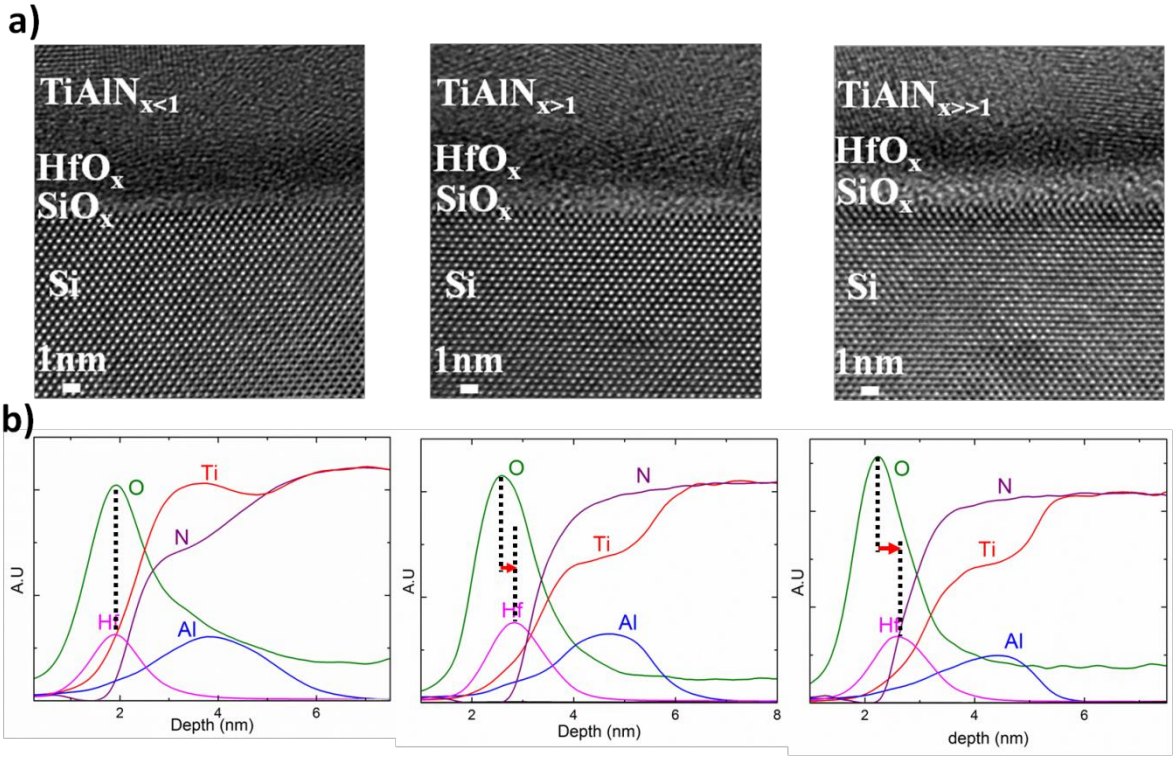


***Fig. II-7**- Qualitative method for estimating the SiO_2-IL thickness. Comparison between the HRTEM images (a) and the corresponding STEM-EDX elemental profiles (b) shows that the thicker the SiO_2-IL, the more separated the positions of the Hf and O profiles*

The analyzed samples in this work have been prepared by mechanical polishing followed by smooth ion etching with a PIPS system (Precision Ion Polishing System). The final thickness of the samples is below 80nm. This TEM sample preparation technique avoids local heating and sample amorphisation.

II-4. Time of Flight - Secondary Ion Mass Spectrometry (ToF-SIMS)

SIMS analysis technique is dedicated for the analyses of the chemical elements distribution in thin solid films. SIMS operating technique is based on the sputtering of the sample surface using focused ion beam (here Cs+ accelerated at 500eV) which results in secondary ions ejection. The secondary ions are then accelerated through a mass spectrometer detector, which enables the chemical composition analysis of the sample (Fig. II-8) [Benninghoven87]. The focused ion beam is pulsed and the time of flight of the ejected secondary ions is measured. This time of flight is associated to the ejected atoms mass and charge [Benninghoven87, Vickerman01]. Using standards, the sample chemical composition can be determined and this for all the chemical elements present in the periodic table.

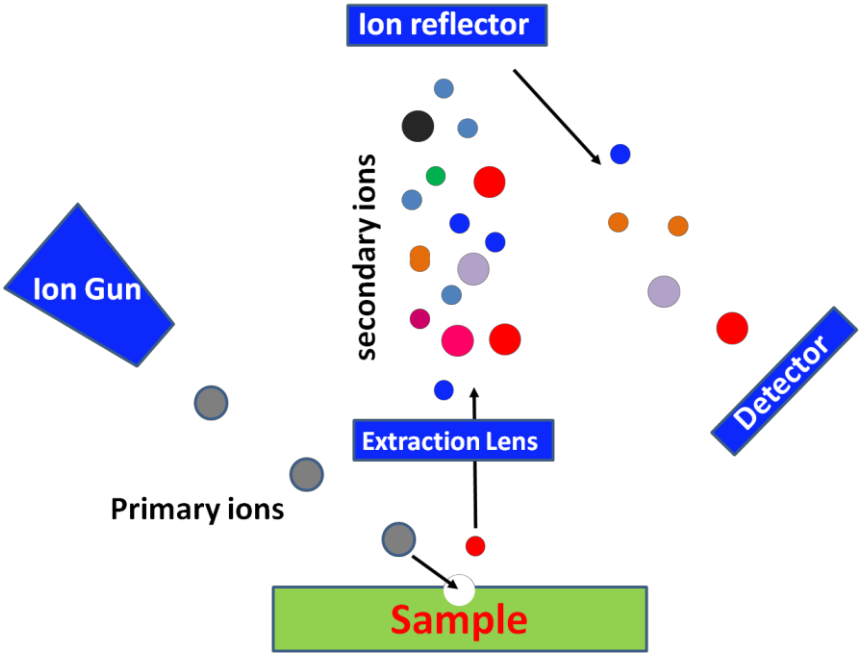


Fig. II-8 - **Schematics of Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS)**

In this work, ToF-SIMS was used because of its high sensitivity (detection limit between 10^{15} and 10^{18} atm/cm^3) and very good depth resolution (about 0.5 nm). In addition, thanks to its micrometric sized probe (about 1µm diameter here, it gives in contrast with STEM EDX an averaged behavior of the chemical species distribution in the gate electrode.

II-5. X-ray photoelectron spectroscopy analysis

X-ray photoelectron spectroscopy analysis (XPS) is a surface-sensitive analysis technique based on the interaction between X-rays and the core level electrons of atoms. It is a quantitative, non-destructive technique for solid conductive materials, which allows the detection of all the chemical species except H and He [Moulder95, Briggs90]. It is most commonly used for the determination of the bonding state of the analyzed elements (chemical environment). The spectrum obtained from XPS is a plot of the number of electrons detected versus their binding energy.

Indeed, the measurement of the kinetic energy provides the binding energy of each element present in the analyzed sample. Equation II-2 gives the relationship between the kinetic energy of the emitted photoelectron (E_c) and the binding energy of a chemical element (BE):

$$E_c = \hbar\nu - BE - \varphi_m \qquad \text{(Eq. II-2)}$$

$\hbar\nu$ is the incident x-ray energy and φ_m the work function of the spectrometer.

Different contributions are present in the XPS spectrum:

- the photoelectron peaks which is exploited in our work (the energies of the peaks are characteristic of the element analyzed ; they are tabulated in handbooks [Moulder95]);
- the background (it results from all those electrons for which scattering events cause energy losses prior to emission from the sample). This induces a background of counts which is generally subtracted by using dedicated software;
- charging effect (in a case of an insulator material, a substantial charge can accumulate on the surface and give rise to a surface potential between 0.1 to several hundred electron volts. This effect has been observed in the studied samples in this work and we used the deposition of a thin metallic silver layer between the analyzed sample and the carrier to avoid it.

In addition to these contributions, secondary peaks may occur in a XPS spectrum due to Auger transitions, plasmon structures, shake-up and shake-off energy loss peaks.

In this work, the “XPS peak” freeware is used for XPS spectra analysis. After using non-linear Shirley algorithm for the background subtraction [Shirley72], the chemical environments identification is carried out by peaks decomposition using the function presented in equation II-3 [Kwok00].

$$GL(x,p,w,h,m) = h\left\{\frac{e^{-(1-m)\cdot\ln(2)\cdot Q}}{1+m\cdot Q}\right\} \quad \text{(Eq. II-3)}$$

where $Q = \left[\frac{x-p}{w}\right]^2$, h is the peak height, x is the independent variable, p is the peak position, w is the FWHM of the peak and m is 0 for a 100% Gaussian function and 1 for a 100% Lorentzian function.

Here, a 100% Gaussian function with m=0 is used for peaks decomposition and chemical environment identification. The relative areas of the different contributions to the peak analyzed have been calculated for comparison between the different chemical environments present in the gate electrode. Besides, Si2*p* Si^0 peak energy at E=99.6eV is chosen in this work as a reference to adjust the other peaks energies and highlight a possible charging effect.

II-6. Architecture of the studied stacks

Investigations in this thesis work have been conducted on full metal gate electrodes integrated with the gate last approach. The studied stacks have a common general architecture presented in Figure II-9(a). It consists in a succession of layers above the Si substrate described below along with their nominal thicknesses:

- two successive oxide layers which define the gate oxide
  - first, wafers received an initial HF bath cleaning to remove the native oxide followed by 0.7nm SiO_2 chemical oxide formation by a wet oxidation,
  - then a 2nm HfO_2 layer deposited by atomic layer deposition (ALD) using $HfCl_4$ and H_2O precursors at 350°C;
- layers which constitutes the metal gate of the stack
  - one or several layers of metals are deposited using Physical Vapor Deposition (PVD) or Ion Beam Deposition (IBD) at room temperature for gate electrode work function control;
- finally, the contact metal plug, which is
  - either a PVD Metal plug (150 nm of W deposited at room temperature),
  - or a CVD metal plug (about 5nm CVD deposited TiN with $TiCl_4$ precursor and NH_3 plasma densification at T=395°C followed by about 150nm CVD deposited W with WF_6 precursor at T=405°C).

200mm MOS Capacitors (Fig. II-9(b)) received specific preparation to introduce a beveled SiO_2-IL, which means that the films were deposited on a SiO_2 layer with varying thickness as illustrated in figure II-9(d). This allows the extraction of the metal EWF as explained in §II-8. The stacks deposited on the 300mm devices have a constant SiO_2 thickness (Fig. II-9(c)).

The detailed gate stack structures with the different work function materials investigated in this work are presented in figure II-9(b) and (c).

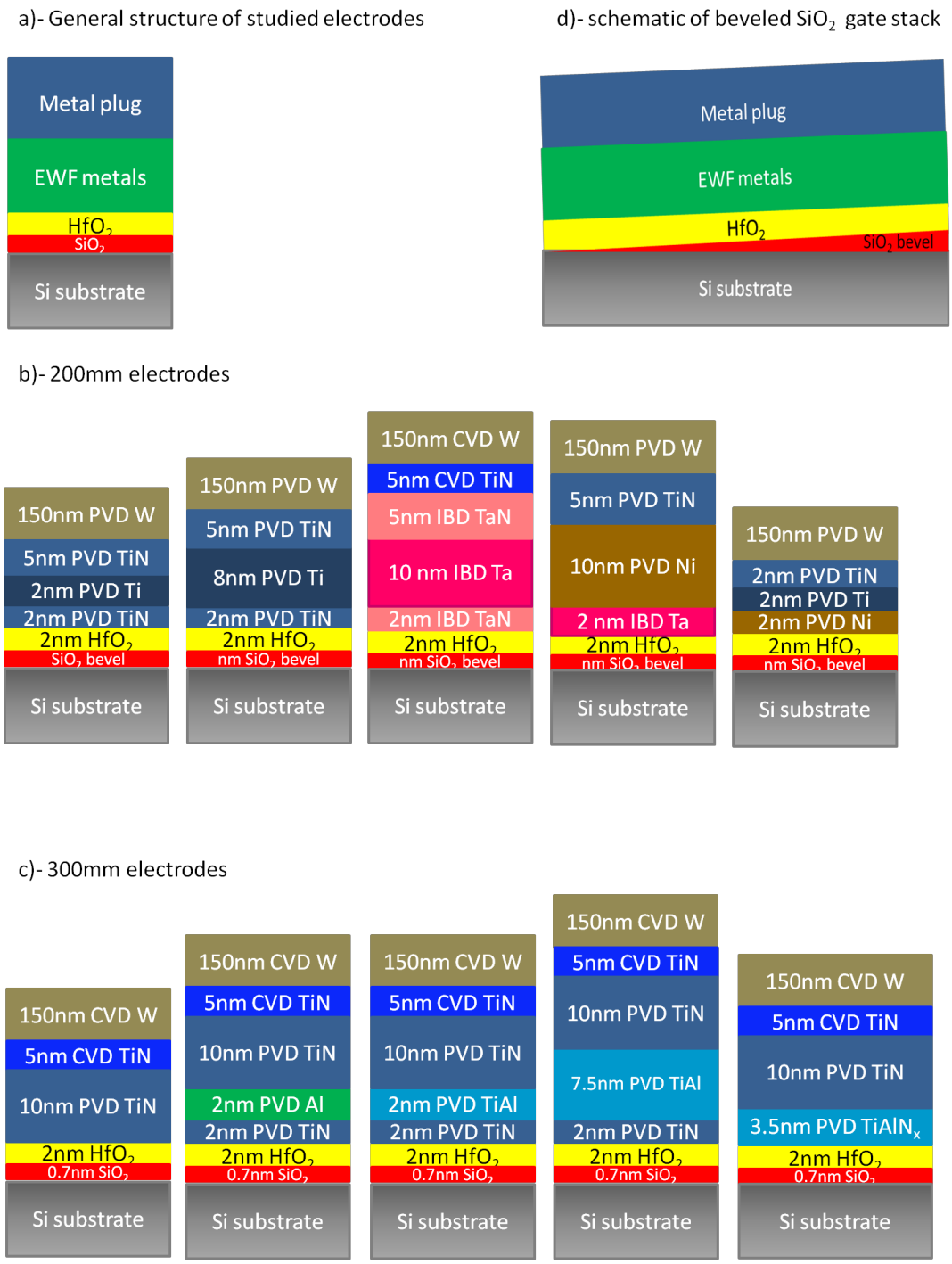


***Fig. II-9**- Architecture of the studied gate electrodes*

II-7. Back-side samples preparation for chemical analysis:

Owing to the architecture of the stacks and due to the limited depth that can be analyzed by XPS (about 5nm from the surface), we decided to develop specific sample preparation techniques to have an easy access to the interface of interest, i.e. HfO_2/metal gate, which is embedded below a thick metal gate/plug.

Two approaches can be used: front-side metal plug de-processing or back side substrate removal. In the case of a wet chemical front side metal plug de-processing, the lack of chemical etch stop layer between the metal plug and the work function metals in the studied stacks here makes difficult the conservation of the area of interest. Thus, the chemical analysis conducted in this work has been achieved on backside prepared sample [Py11].
This specific sample preparation method is performed within three steps:

a) the first step consists in 5mm per 5mm piece of wafer extraction from the 200 or 300mm wafer. The front side of the sample is glued on a silicon support;
b) the second step consists in mechanical polishing of the silicon substrate with a stop at few microns far from the sample/silicon support interface;
c) the final step consists in a TMAH (Tetramethylammonium hydroxid) etching of the remaining silicon substrate with a stop at the SiO_2-IL.

Figure II-10 presents a scheme summarizing these different steps and figure II-11 shows an optical image of the sample after a full backside preparation. With this sample preparation method, the thermal budget and the structure of the studied stacks remain identical to the ones of the electrical devices, which enables direct comparison between the electrical and material results.

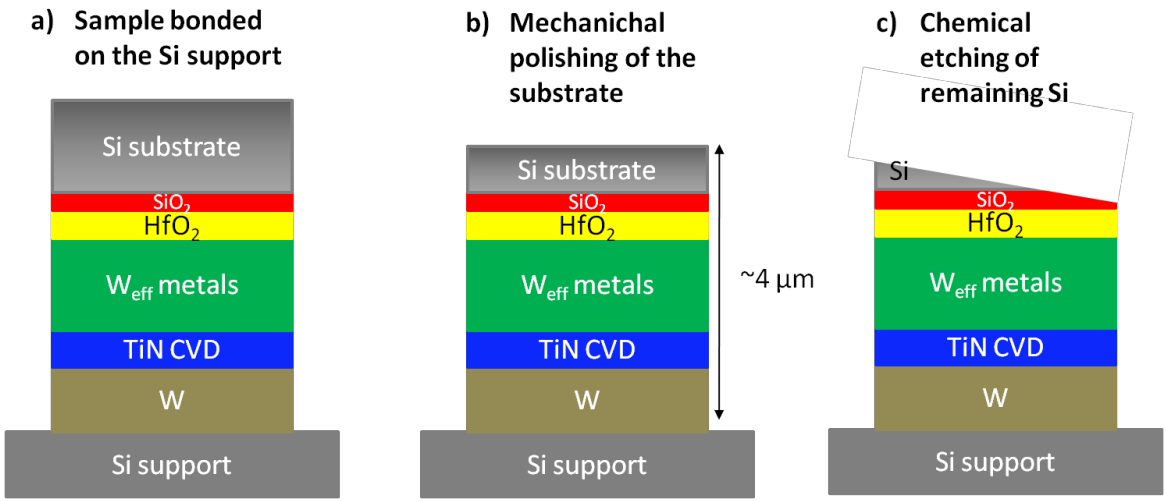


***Fig. II-10**- backside sample preparation steps*

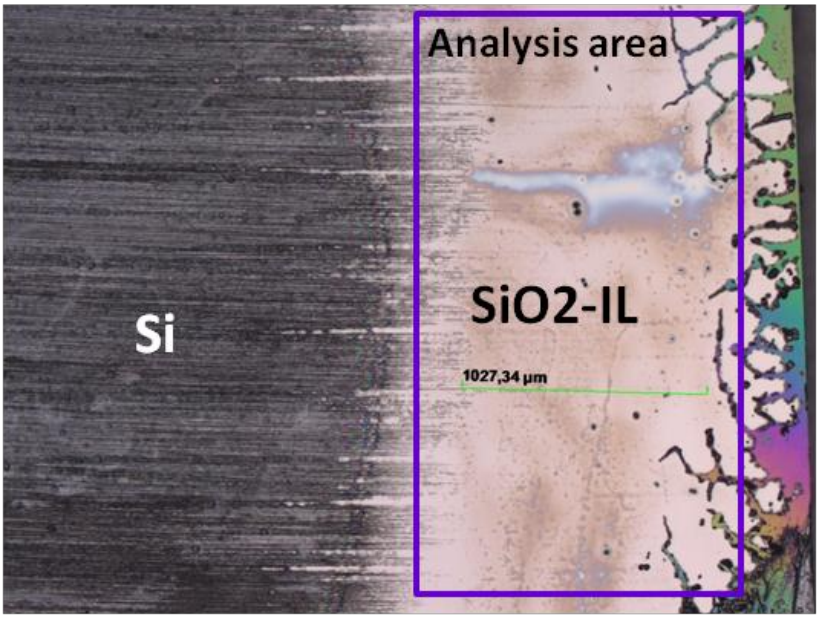


***Fig. II-11**- Optical microscope image of the sample after backside preparation*

II-8. Electrical characterization

In order to obtain the electrical characteristics of the studied gate electrodes, Capacitance-Voltage measurements (C-V_g) have been performed on large HK/MG MOS capacitors (without Source/Drain, see Fig. II-12).

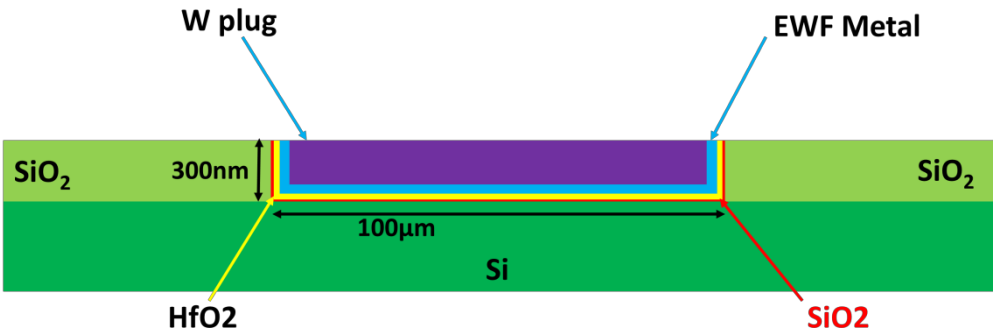


***Fig. II-12**- Schematic representation of a MOS capacitor used for C(V) measurements*

The applied voltage (V_g DC voltage and v_g AC voltage) is performed using a tip contact on the metal plug (Fig. II-13a) and results in a C-V_g characteristic from depletion to accumulation using 1, 10, 100kHz frequencies (Fig. II-13b). The Equivalent oxide thickness (EOT) is deduced from the measured Capacitance Equivalent Thickness (CET) by subtraction of a thickness of about 3Å related to the quantum effect at the substrate inversion layer. The corresponding relation is CET=EOT+3Å.

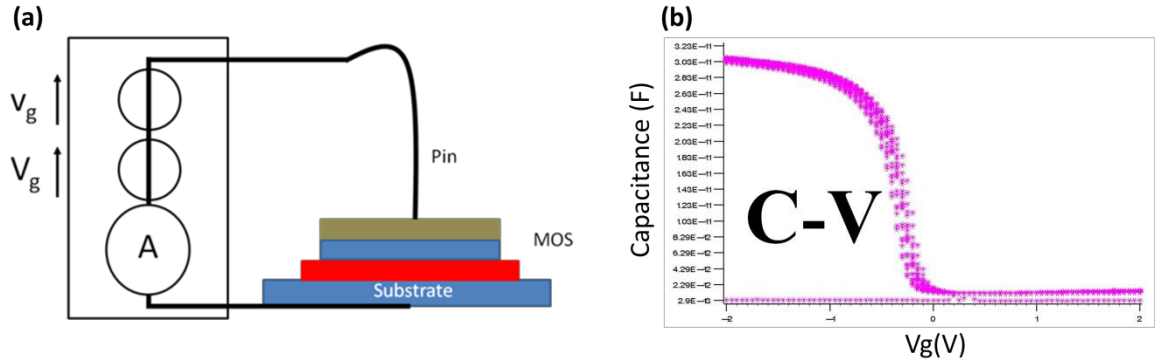


***Fig. II-13**- (a) Measurement circuit of MOS capacitor.*
(b) Typical C-V_g characteristic obtained from a TiN/SiO_2/Si MOS capacitor.

The effective work function (EWF) depends on the flat band voltage (V_{fb}) (Eq. I-1).
In this work, two kinds of wafer have been prepared for C-V measurements.

First, 200mm wafers have been prepared with a beveled SiO_2 oxide and a fixed HfO_2 thickness. Considering a constant fixed interface charge between the Si substrate and the dielectric, this specific wafer preparation method enables a linear extraction from the V_{fb}-EOT curve. According to equations I-1 and I-4 recalled below

$$V_{fb} = (\phi_m - V_{ext}) - \phi_s = EWF - \phi_s \quad \text{(Eq. I-1)}$$

$$EWF = \phi_m - \frac{1}{\epsilon_{SiO_2}}(Q_{SiO_2/Si}EOT + Q_{HfO_2/SiO_2}EOT_{HfO_2}) + \delta_{HfO_2/SiO_2} + \delta_{MG/HfO_2} \quad \text{(Eq. I-4)}$$

the slope of the V_{fb}-EOT straight line matches the charge density at Si/SiO_2 interface. EWF is measured from the Y-axis intercept; it only depends on the metal work function, fixed charges at HfO_2/SiO_2 interface and dipoles at HfO_2/SiO_2 and metal/HfO_2 interfaces. As noticed in chapter I, the fixed charges in the HK can be minimized due to its small thickness.

Besides, 300mm wafers have been processed with constant SiO_2 and HfO_2 oxides thicknesses. Then, EWF is described by equation I-4 above.

II-9. Contributions to this work

In this work, we performed all the in-line characterization analyses which enable a first evaluation of the deposited layers characteristics such as thickness (XRR, TEM), resistivity and the crystallinity (XRD, TEM).

Besides, in-depth characterizations such as XPS, STEM EDX and SIMS have been achieved by CEA-Leti and STMicroelectronics physical and chemical characterization experts. However, we have a partial contribution to this state of the art characterization work with: XPS peaks fits and chemical bonds identification, STEM EDX analysis development on polished TEM prepared samples and back side sample preparation development for full metal gate structure.

Chapter III

Single Ti and Al deposition on TiN: EOT scaling and EWF elementary mechanisms

III-1. Introduction

Since the introduction of HK/MG materials in CMOS technology, TiN was chosen as the reference metal for the pMOS side transistor in both gate first [Cosnier07, Wu10, Kadoshima09] and gate last [Tai06, Veloso11] integrations thanks to its adapted EWF and to its high chemical stability on HfO_2.

In this chapter, starting with the reference stack HfO_2/TiN for pMOS transistor, we will investigate how adding single Ti and Al metals on top of TiN allows obtaining an nMOS adapted EWF. This will be done in the context of the gate last approach, where the thermal budget is limited to 400°C, 30 min.

The choice of the Ti and Al metals was made following two main criteria. These metals have:

- a low work function in vacuum in order to favor the nMOS EWF (see tables I-1 and I-2, Fig. I-8) [Michaelson77],
- a free energy of metal-oxide formation lower than the one of SiO_2 which enables the oxygen scavenging from the SiO_2-IL ($\Delta G_{Al2O3} < \Delta G_{TiO} < \Delta G_{SiO2}$, see Fig. I-9).

The interdiffusion of chemical species in the gate stack after depositing Ti or Al on HfO_2/TiN is studied here with a particular focus on their effect on the modulation of the electrodes EWF and stack EOT.

These studies will be performed by systematic analytical investigations from the submillimetric to the nanometric scale with XPS, TOF-SIMS and STEM-EDX techniques. The aim is to correlate the elemental distribution across the stack, particularly at the HfO_2/MG interface, and the chemical bonds these elements form to the electrical parameters EWF and EOT as determined from C-V experiments. Interpretation of the results will be based on thermodynamic considerations.

III-2. TiN reference

This section presents the electrical and physico-chemical investigations achieved on the Si/SiO_2/HfO_2/TiN/W reference stack.

The different layers in the stack going from the [110] projected structure of the Si substrate to the dark polycrystalline W contact metal plug are imaged on the Cs-corrected high-resolution (HRTEM) micrograph of figure III-1. Just above the Si substrate, the

amorphous SiO_2 and HfO_2 thin layers appear successively clear and dark respectively. On top of these nanometric layers, the polycrystalline 10nm PVD-TiN followed by the 5nm CVD-TiN appear clearer with respect to the dark HfO_2 and W layers.

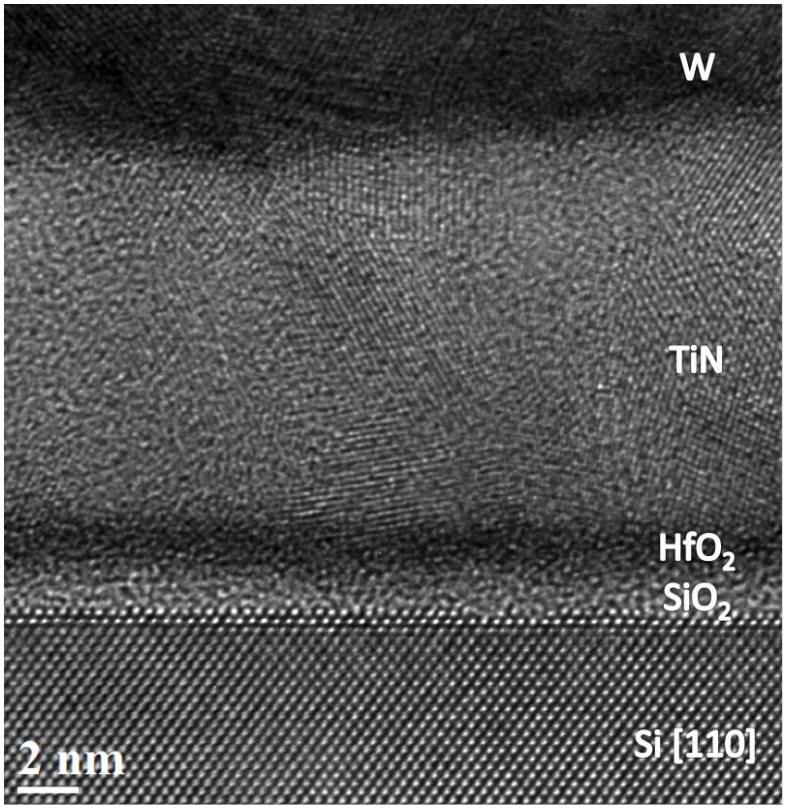


***Fig. III-1**- Cs-corrected HRTEM micrograph of a Si/SiO_2/HfO_2 2 nm/TiN 15nm/W stack*

The distribution of the elements across the stack is illustrated on the STEM-EDX map of figure III-2a. It is homogeneous over large areas. As shown on figure III-2b, the projected intensity profiles along the Si/SiO_2 interface direction determined from this map allow determining Hf, O, N and Ti elemental profiles across the stack and proposing a location of the interfaces at places near inflexion points on the profiles. The increase of the O profile intensity at the top of the TiN layer is a feature that will be present on all the profiles shown in this thesis work. It is due to the process air break before deposition of the TiN/W metal plug. As discussed in chapter II, the maximum of O profile is separated from the maximum of the Hf profile and shifted toward the silicon substrate, which confirms a thicker SiO_2-IL than the 0.7nm initial one (§ II-6) imaged by HRTEM. Above the oxides layers, N and Ti profiles are very close in bulk TiN and also at the HfO_2/TiN interface, which reveals the stoichiometric composition of TiN layer with Ti/N~1.

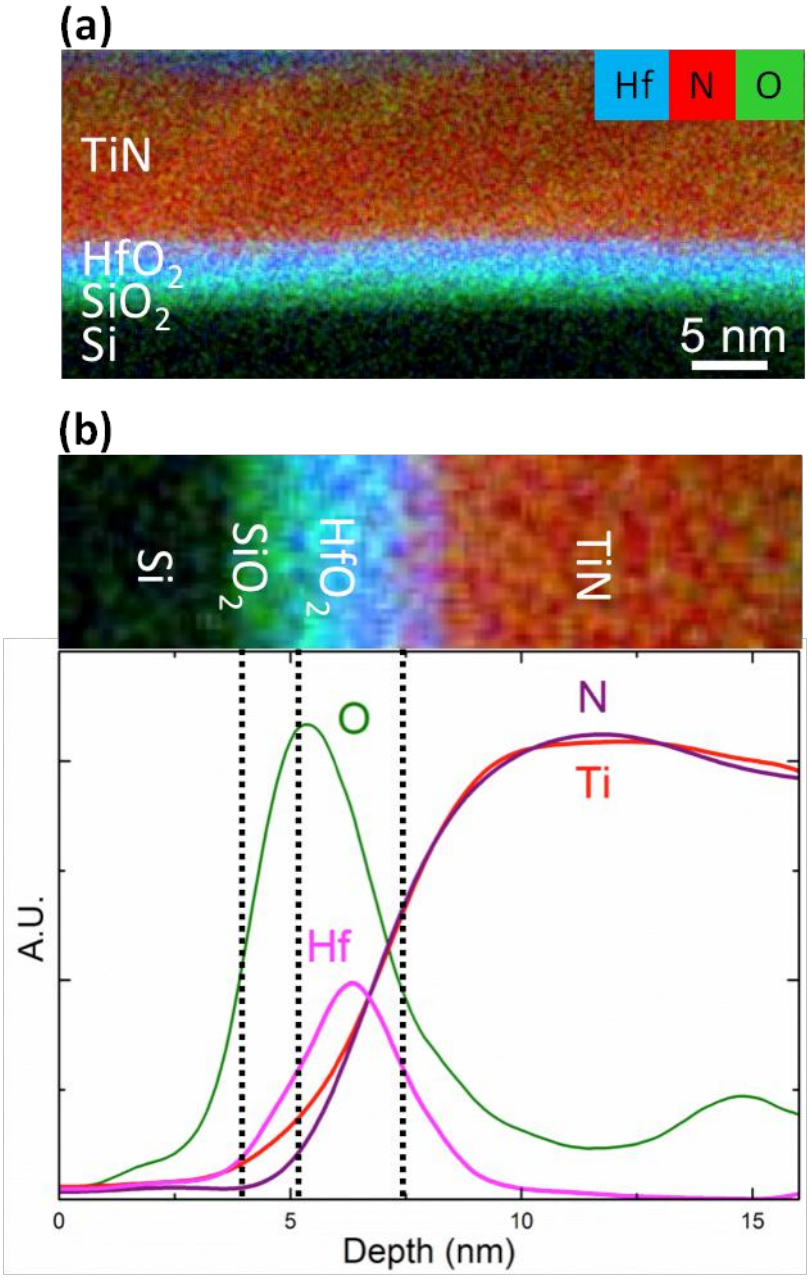


Fig. III-2*- (a) STEM-EDX map of a Si/SiO_2/HfO_2 2 nm/TiN 15nm/W stack and (b) corresponding Hf, O, N and Ti profiles across the stack with localization of the different sublayers (dashed lines)*

The XPS Hf4*f*, N1*s* and Ti2*p* core level spectra obtained from a backside prepared (§ II-7) HfO_2/TiN/W stack are shown on figure III-3 and the corresponding peaks decomposition summarized in table III-1. The stoichiometric nature of TiN is confirmed by the component at 455.3 eV [Saha92, Bertoti95, Jaeger12]. In addition, Ti-O_2 and Ti-O-N significant contributions highlight the high oxidation level of TiN.

Diffusion of nitrogen from TiN toward the bottom of the stack is stated from the presence of some components in the Hf4*f* and N1*s* core level spectra:

- Hf-N (Hf4*f*, N1*s*) components support diffusion of N in HfO_2 and,
- Si-N and Si-O-N (N 1*s*) components support diffusion of N in SiO_2.

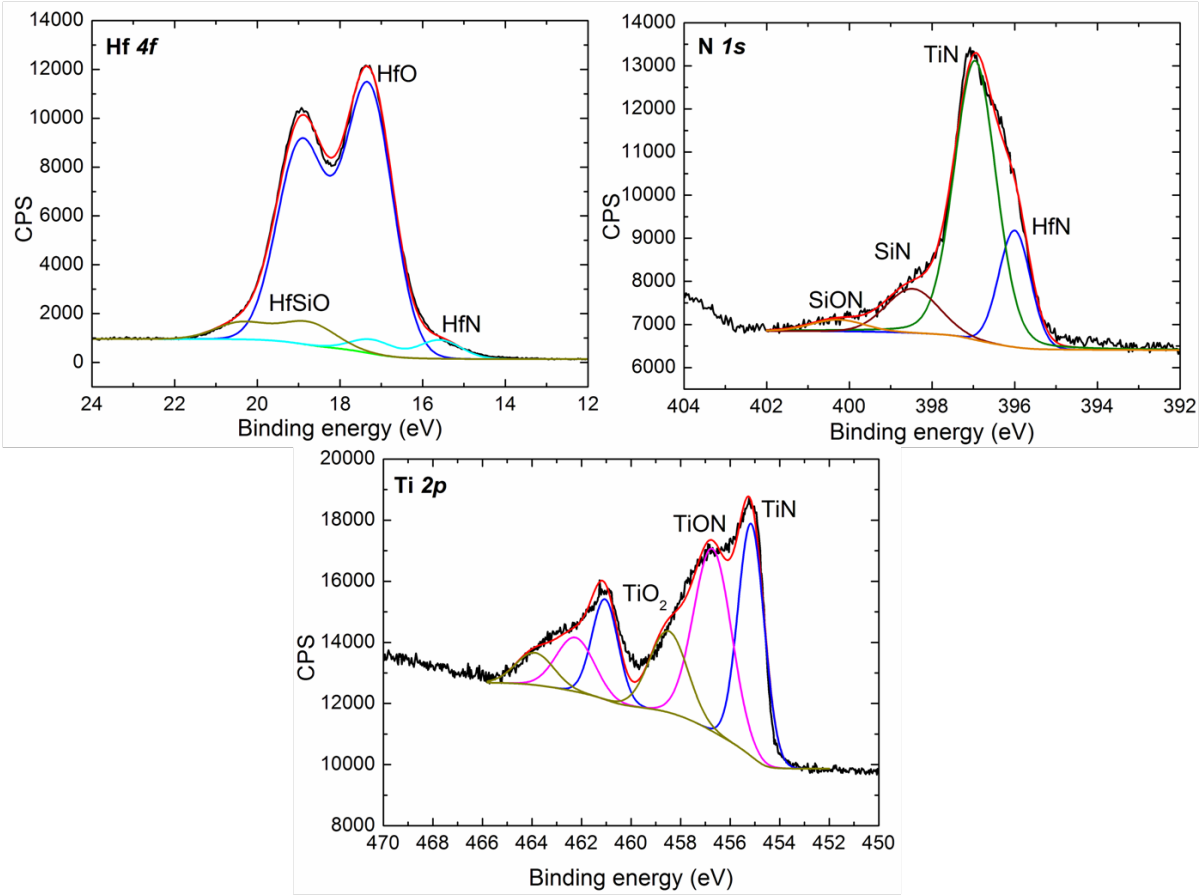


***Fig. III-3**- XPS Hf4f, N1s and Ti2p core level spectra obtained from a backside prepared $SiO_2/HfO_2/TiN/W$ sample*

Ti2*p*	BE (eV)	RA (%)	N1*s*	BE (eV)	RA (%)	Hf4*f*	BE (eV)	RA (%)
Ti-N	455.3	40	Hf-N	396.1	20	Hf-N	15.7	5
Ti-O-N	456.7	40	Ti-N	397	60	Hf-O	17.3	87
$Ti-O_2$	458.5	20	Si-N	398	15	Hf-Si-O	18.75	8
			Si-O-N	400	5			

***Table III-1**- Binding energies and relative areas (RA) for the different chemical environments extracted from the Ti2p, N1s and Hf4f core level spectra of a $SiO_2/HfO_2/TiN/W$ backside sample*

Electrical C-V measurements reveal the pMOS behavior of this HfO_2/TiN-based stack with a EWF value of 4.85eV (Fig. III-4). This result is directly connected to the stoichiometric character of TiN at the HfO_2/TiN interface. As stated in chapter I (§I-4-a), the EWF of HfO_2/TiN results from the addition of the EWF of TiN/SiO_2 .i.e $EWF_{SiO2/TiN}$=4.6eV

to the HfO_2/SiO_2 dipole value estimated between 0.1eV~0.2eV [Charbonnier10]. Hinkle *et al.* showed that Hf-N formation at the HfO_2/TiN interface may induce an increase of the electrode EWF. Since we observe the formation of Hf-N here, we believe that Hf-N dipole formation at HfO_2/TiN interface have a contribution on the measured EWF=4.85eV.

Besides, the recorded EWF here is in agreement with commonly measured EWF of PVD deposited TiN on HfO_2 (Fig. III-4) [Veloso11]. This pMOS adapted EWF is associated to a sub-1nm EOT of 0.95nm.

III-3. TiN/Ti bi-layer: a too strong scavenger

In this section, Ti deposition on HfO_2 2nm/TiN 2nm reference is achieved in order to favor an nMOS adapted work function. Two stacks with a 2nm and an 8nm thick Ti layer were prepared following the sequence HfO_2 2nm/TiN 2nm/Ti/TiN 5nm/W.

Remarkably, the electrical investigation showed a great instability of these stacks. A total short circuit occurred for the 8nm thick Ti electrode. Therefore, measurements were performed on the 2 nm thick Ti electrode and there an early short circuit is also observed for a 1.8nm EOT value. The EWF shifted by -0.75eV with respect to the reference with an nMOS adapted EWF measured at 4.1eV (Fig. III-4).

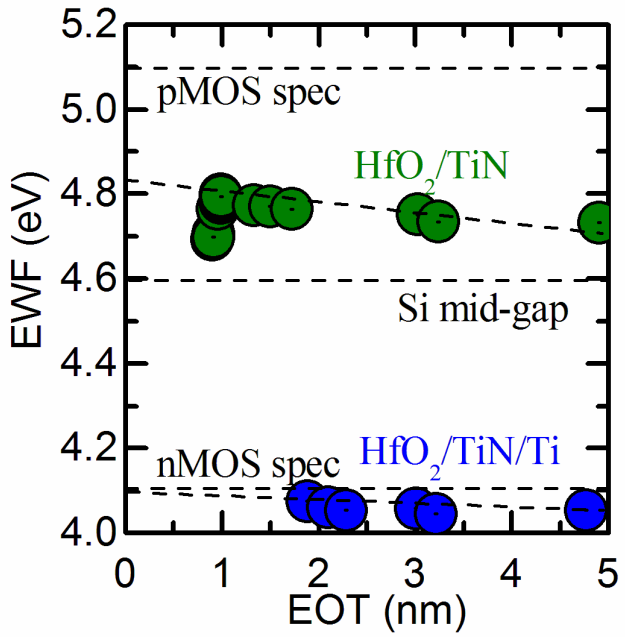


Fig. III-4*- EWF versus EOT recorded from the HfO_2/TiN reference stack and the HfO_2/TiN 2nm /Ti 2nm stack. Measurements have been performed on beveled SiO_2-IL*

The homogeneous elemental distribution across the stack with the 8 nm Ti layer is shown on the STEM-EDX map of figure III-5a. On the corresponding elemental profiles (Fig. III-5b), a striking phenomenon is observed, the O profile is exclusively located in the titanium layer. No oxygen is detected in the dielectrics, which indicates a total reduction of oxygen from the SiO_2 and HfO_2 oxides. The result is the formation of metallic Hf directly in contact with the silicon substrate as imaged with the red color on the STEM-EDX map (Fig. III-5a). This analysis explains why short circuits occurred during the electrical measurements and their dependence on the Ti electrode thickness. It confirms that a single Ti layer on top of TiN is not a stable electrode against oxygen scavenging.

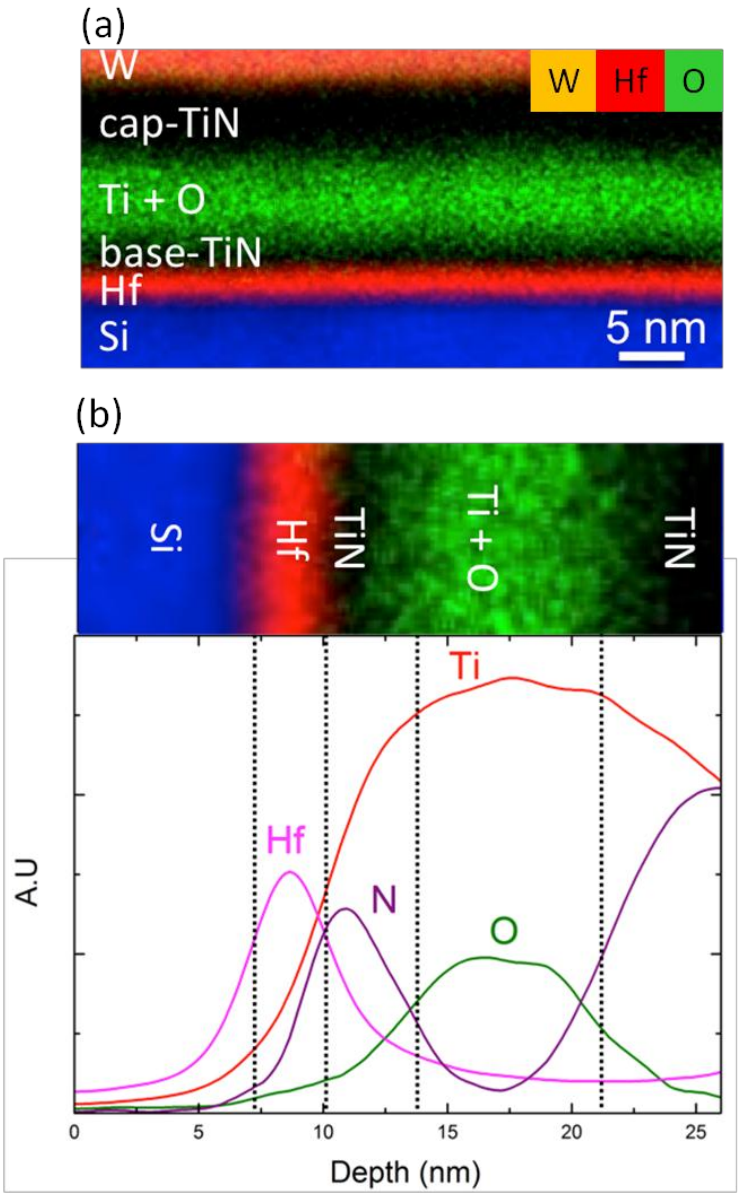


***Fig. III-5**- (a) STEM-EDX map of a Si/SiO2/HfO_2/TiN/Ti 8nm/TiN/W stack and (b) corresponding*
Hf, O, N and Ti profiles across the stack with localization of the different sublayers

As discussed in the paper of Kim et al. [Kim04], the thermodynamic driving force for decomposition of the SiO_2-IL of $Si/SiO_2/HfO_2/Ti$ stacks is related to the Gibbs free energy change of the following reaction, $C/2\ SiO_2 + Ti \rightarrow C/2\ Si + TiO_C$. This energy as calculated by Kim is reproduced in figure III-6. It is largely negative at 300°C and it is more negative at higher temperature, i.e. at 400°C, the maximum temperature the Ti-based electrode was exposed in this work. When O reaches the Ti layer, its incorporation by dissolution in the Ti electrode material is then promoted due the high solubility of oxygen in titanium (up to 33% at 400°C, see Fig. III-7, see the α-Ti domain) [Murray87, Cancarevic07]. Oxygen is then localized in interstitial position without formation of Ti-O bonds [Ruban10, Tsuji97].

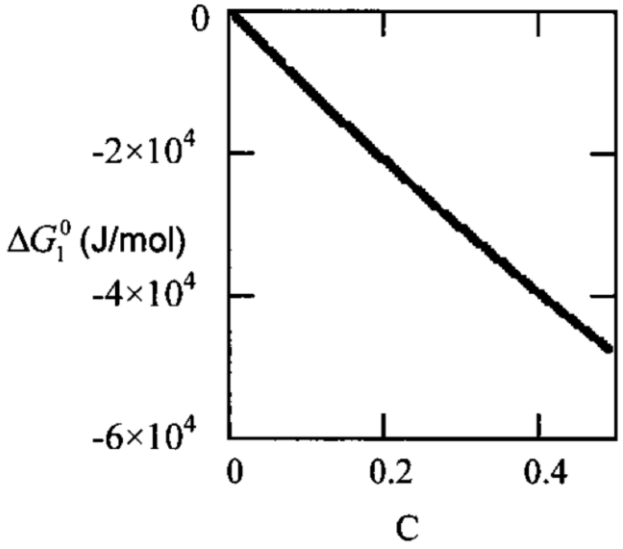


***Fig. III-6**- Gibbs free energy change of the reaction* $C/2\ SiO_2 + Ti \rightarrow C/2\ Si + TiO_C$ as a function of C at 300°C

Moreover, the decomposition of the SiO_2-IL and the dissolution of oxygen in Ti suppose that oxygen can diffuse through the HfO_2 dielectric. Kim et al. supported that oxygen diffuses with quite rapid kinetics in the case of their stack annealed at 300°C. This should be enhanced in the case of our films that were subjected to a higher temperature anneal, i.e. 400°C.

The oxygen has also to diffuse through the base TiN layer, i.e. the TiN layer sandwiched between the HfO_2 and Ti layers. This is apparently thermodynamically and kinetically favored because not only the oxygen of the SiO_2-IL has been consumed but also the one of the HfO_2 layer. The reason for the simultaneous reduction of HfO_2 to the metallic Hf is not clear. Indeed, the Gibbs free energy change associated to this transformation is not favorable, the Gibbs free energy of formation of HfO_2 being more negative than the one of TiO (see Ellingham diagram, Fig. I-9). However, some works proved the O scavenging capability of a

Ti layer deposited on amorphous HfO_2, even it occurs with a more limited extent to what is observed in this study. Note also that this phenomenon has been recently considered to explain resistive switching mechanism in HfO_2-based metal-insulator-metal (MIM) cells [Goncharova07, Kim13, Calka14].

The STEM-EDX N profile enables determining the location of the base-TiN. In the bulk of this layer, the Ti profile intensity is higher than the N one and to a lesser level at the HfO_2/TiN interface. This suggests a redistribution of Ti and N, which results in a substoichiometric base-TiN (TiN_x, $x<1$). At a first glance, we can try to explain this situation looking at the phase diagrams proposed for the Ti-N system (see Fig. III-8). If we suppose an equilibrium between the same quantity of α-Ti (pure Ti, 0% of N) and the stoichiometric δ-TiN at 400°C (here only the 500°C values are known), then a redistribution of N should occur. At equilibrium, it would result to a Ti-rich mixture of ε-Ti_2N and α-Ti(N). α-Ti(N) is Ti which has incorporated nitrogen in interstitial position [Ruban10] i.e. without the formation of Ti-N bonds. Hence, knowing the low work function of Ti in vacuum (4.33 eV) [Michaelson77], the low EWF=4.1eV obtained with a HfO_2/TiN2nm/Ti2nm electrode is induced by the Ti-rich character of the substoichiometric $TiN_{x<1}$ at the HfO_2/TiN interface. A similar value was obtained for intentionally prepared substoichiometric TiN_x electrode on a SiO_2 gate oxide [Westlinder04].

The TiN/Ti electrode allows reaching the n-like character (substoichiometric $TiN_{x<1}$) but is a too strong oxygen scavenger.

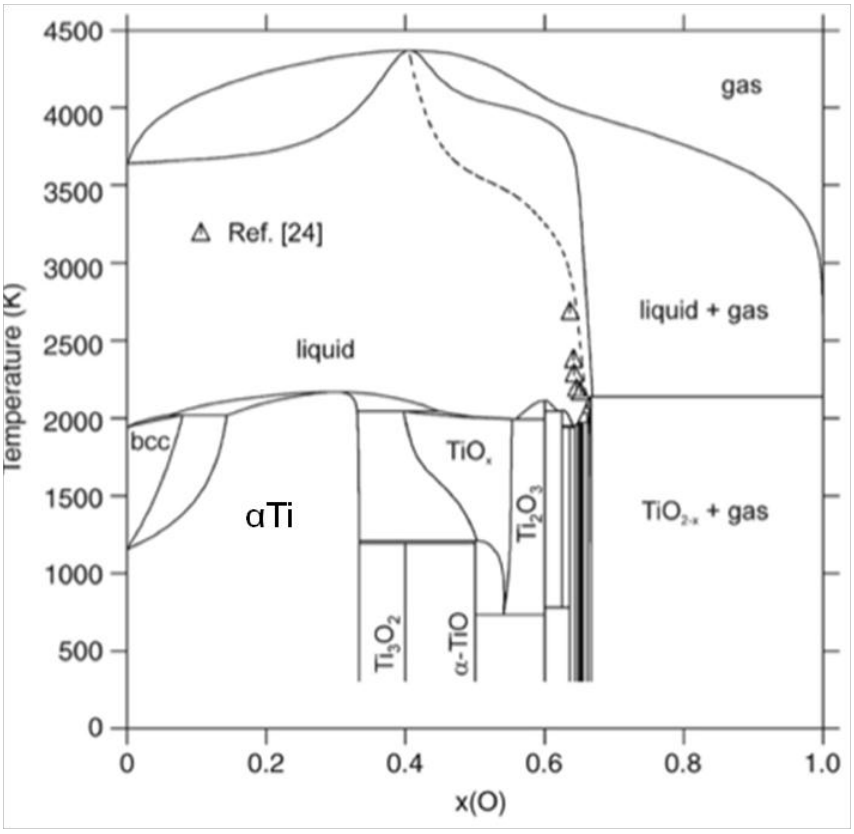


***Fig. III-7**- Ti-O binary phase diagram from [Cancarevic07].*

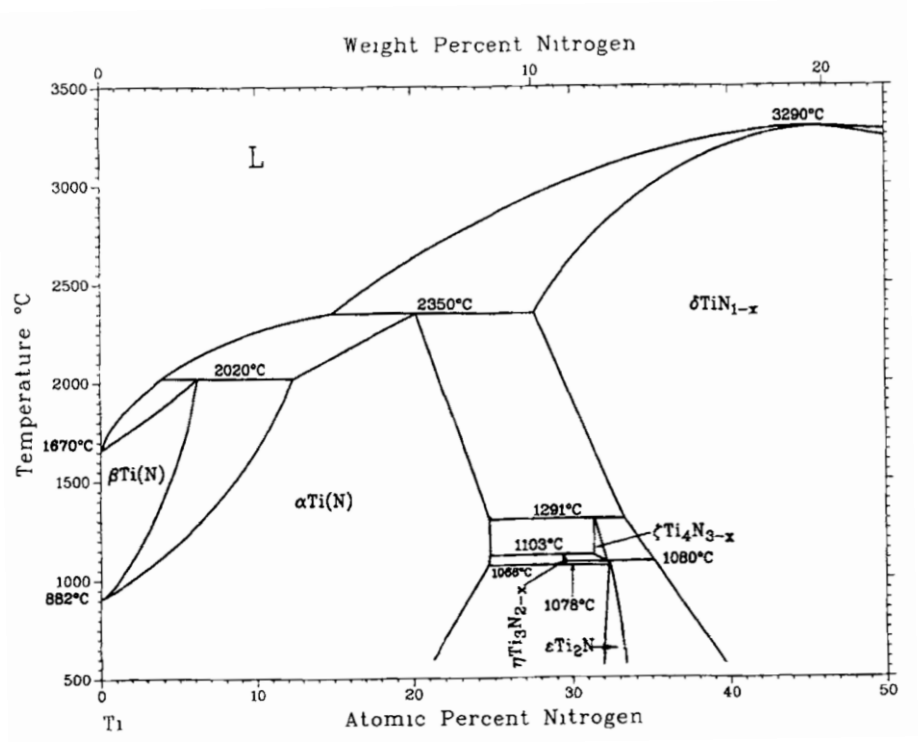


***Fig. III-8**- Ti-N binary phase diagram from [Okamoto93]*

III-4. TiN/Al bi-layer: a controlled but inhomogeneous scavenger

Aluminum is similar to titanium concerning its low vacuum work function and its driving force for O scavenging, the Gibbs free energy of formation of Al_2O_3 being similar to the one of TiO (see Ellingham diagram, Fig. I-9). We study here the behavior of the corresponding TiN/Al metal electrode. For this, an HfO_2 2nm/TiN 2nm/Al 2nm /TiN 15nm/W gate stack was prepared.

Surprisingly and contrarily to all the other stacks studied in this thesis work, the XRR analysis reveals a high roughness in this stack as illustrated by the high attenuation of the arches amplitude in figure III-9.

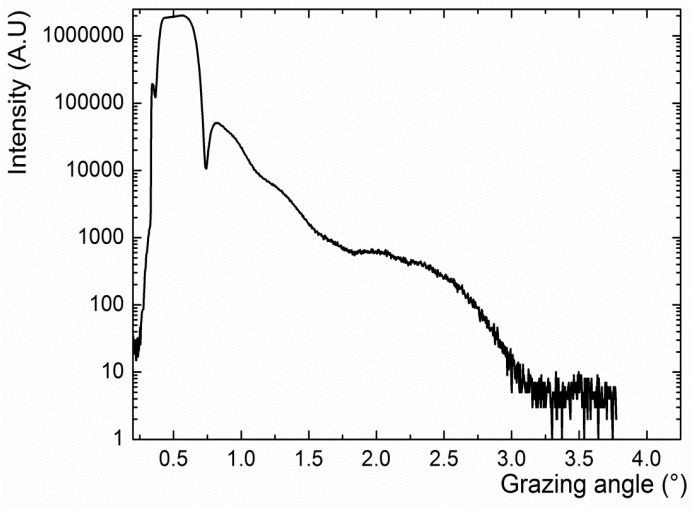


***Fig. III-9**- XRR spectrum of the $Si/SiO_2/HfO_2/TiN/Al/TiN$ stack*

Indeed, the TEM micrograph of the stack shows the presence of a rough interface between the TiN-cap and the final W layer (Fig. III-10). More precisely, the chemical STEM-EDX map enables to identify aluminum as the origin of the roughness in the stack (Fig. III-11). Indeed, we observe a succession of thin and thick Al islands deposited on the base-TiN layer. Moreover, in the region of the base-TiN layer, the distribution of the elements (see colors on Fig. III-11) seems dependent on the location below either a thin or a thick Al island. Therefore, we extracted the elemental profiles of these two kinds of area.

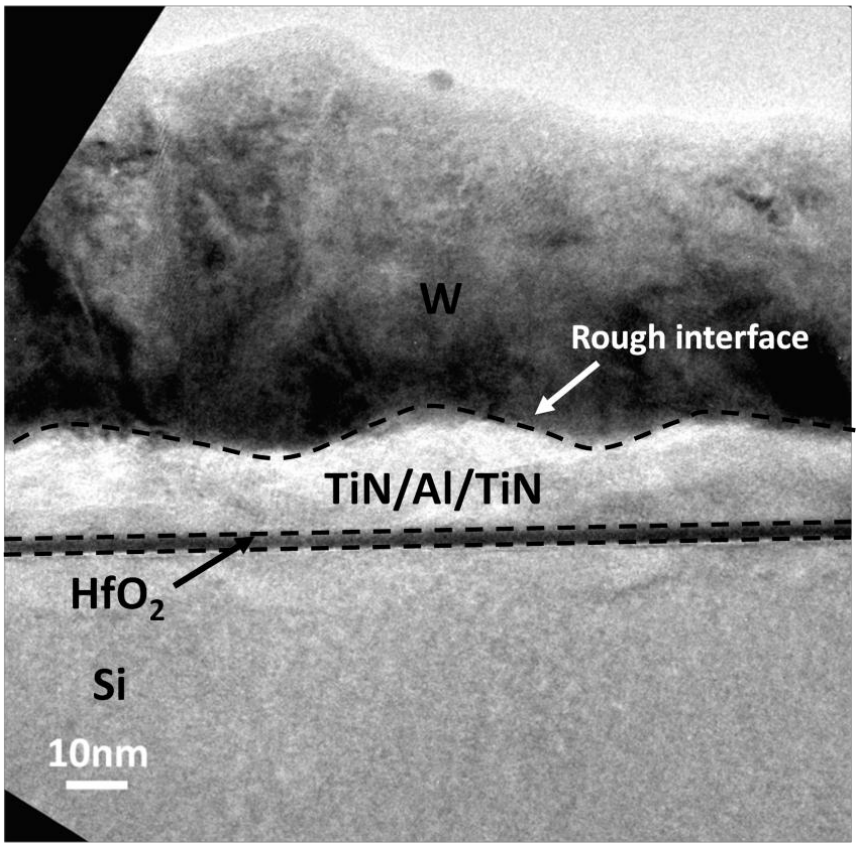


***Fig.III-10**- TEM micrograph of the Si/SiO_2/HfO_2 2 nm/TiN 2nm/Al 2nm/TiN 15nm/W stack*

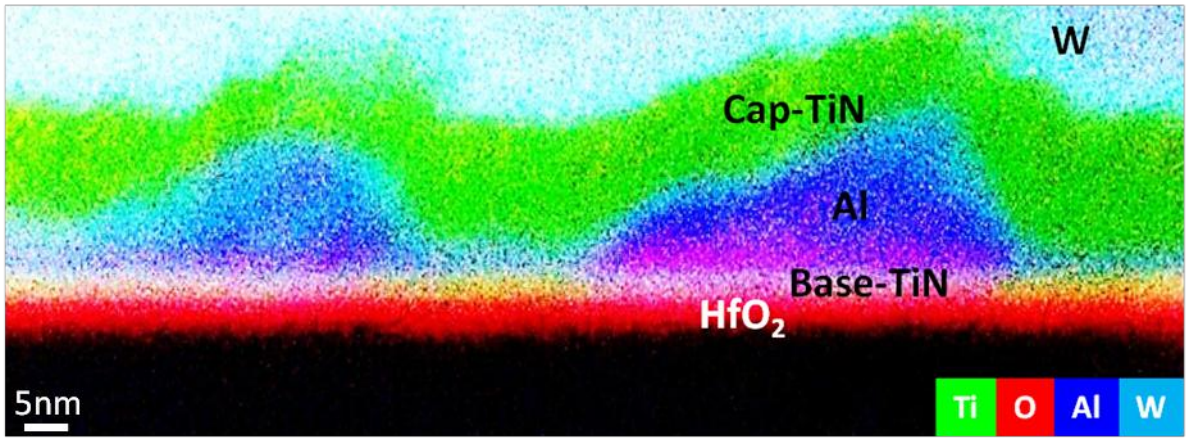


***Fig. III-11**- STEM-EDX map of O, Al and Ti in the Si/SiO_2/HfO_2/TiN/Al /TiN/W gate stack*

Below a thin Al island (Fig. III-12a), the maximum of the O profile is not aligned with the one of Hf but slightly shifted toward the silicon substrate. This indicates that the SiO_2-IL thickness is slightly larger than the original one (> 0.7nm). An estimation of the Al layer

thickness can be obtained from the full width at half maximum of the symmetric Al profile, about 3-4 nm. Around the HfO_2/base-TiN interface, the Al level is low and the Ti/N ratio is close to 1, the Ti profile mostly fitting the N profile. The base-TiN in contact with HfO_2 is nearly stoichiometric for a thin Al electrode layer.

Below a thick Al island (Fig. III-12b), the maximum of the O profile is aligned with the maximum of the Hf one suggesting a thinner SiO_2-IL compared to the case of the thin Al island area, i.e. around or below the original thickness of 0.7nm. This observation supports the fact that a thick Al island on top of HfO_2/base-TiN scavenges the SiO_2-IL which is coherent with the increase of the O profile at the base-TiN/Al interface. The thickness of the Al island here is estimated around 8-9 nm. Close to the HfO_2/base-TiN interface, the Ti/N ratio is higher than 1. Compared to the thin Al island case, this suggests that an increase of the deposited Al thickness induces N and Ti redistribution in the base-TiN, which results in a substoichiometric base-$TiN_{x<1}$ particularly at the HfO_2/base-TiN interface. In addition, Al profile goes deeper through the base-TiN layer and its content is significant at the HfO_2/base-TiN interface.

These observations show that the Al layer thickness is an important parameter, which changes the chemical species distribution within the gate electrode, i.e. the amount of O scavenged from the SiO_2-IL, the N and Ti redistribution in the base-TiN and the diffused Al amount at the HK/MG interface.

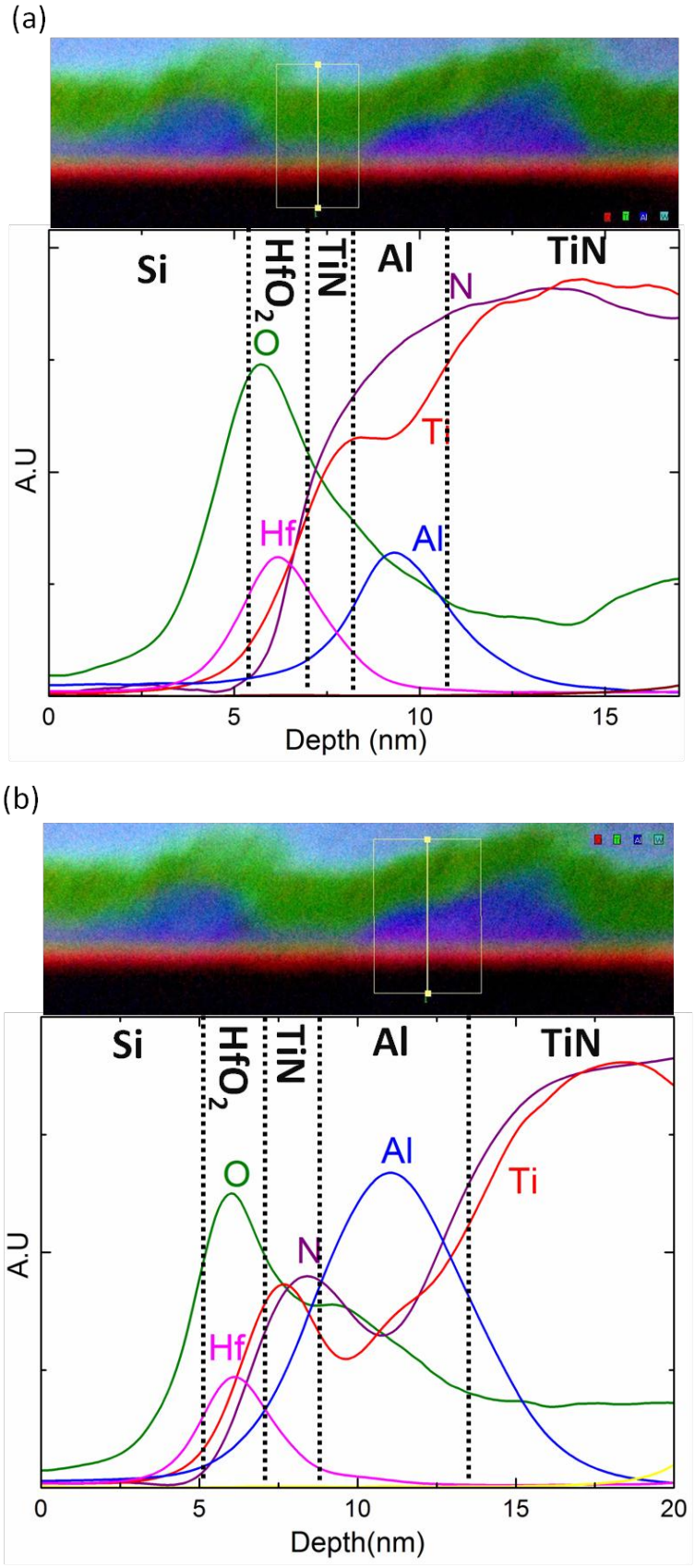


Fig. III-12*- STEM-EDX map of a Si/SiO_2/HfO_2/TiN/Al/TiN/W stack and, for an integration window localized around (a) a thin and (b) a thick Al island, the corresponding Hf, O, N, Al and Ti profiles across the stack with localization of the different sublayers*

The gate stack EWF and EOT measured on this heterogeneous stack are shown on figure III-13. The EWF shifted by -0.6eV with respect to the HfO_2/TiN reference with an nMOS adapted EWF of 4.25eV. In addition to the EWF shift, Al deposition results in a slightly lower scaling of EOT compared to the TiN reference case with a value of 0.93nm.

These parameters are measured on large HK/MG MOS capacitors (100µm). Therefore, in order to achieve a more reliable discussion on the EWF shift and EOT variation mechanisms, the heterogeneous character of the Al layer imposes to go to an analytical investigation at a larger scale than the nanometric one used for the TEM analyses. Analyses on submillimetric and millimetric areas have thus been performed by SIMS and XPS respectively.

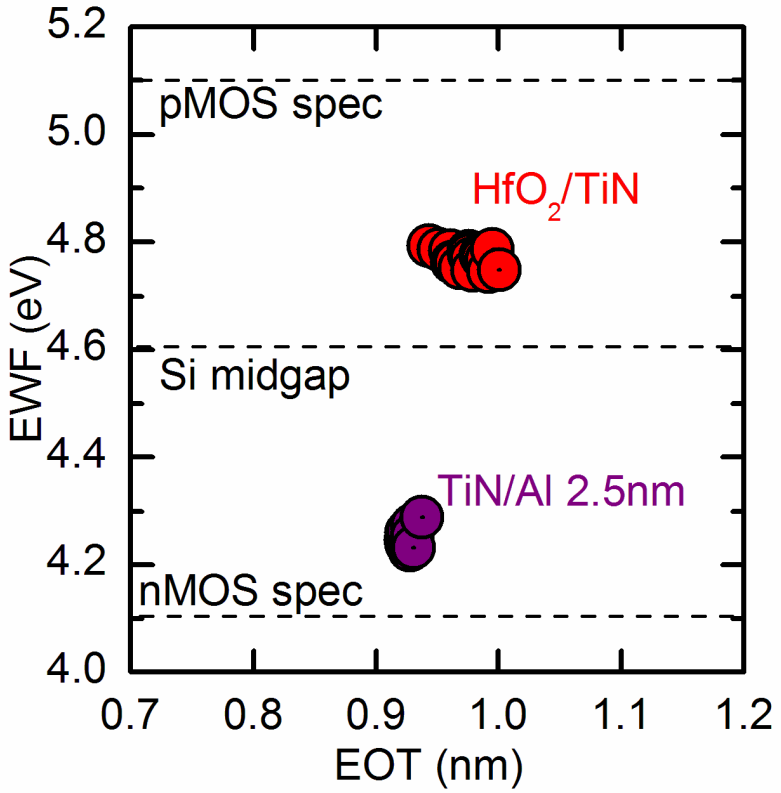


***Fig. III-13**- EWF versus EOT recorded from the HfO_2/TiN reference stack and the HfO_2/TiN 2nm /Al 2nm stack*

On the ToF-SIMS spectra (Fig. III-14), it is possible to estimate a location of the interfaces between the sublayers of the stack, like for the STEM-EDX profiles. The measured mean thickness of the Al layer is rather large if we compare with the 2 nm thick HfO_2 and base-TiN layers. Al has diffused through the base-TiN layer and reaches the HfO_2/base-TiN interface. The presence of this low vacuum work function metal at the HK/MG interface can be considered as responsible for the obtained low EWF (Fig. III-13). We cannot exclude the

additional contribution to the low EWF of the Ti-rich character of the HfO_2/base-TiN interface observed below the large Al islands.

As observed on the STEM-EDX profiles for the thick Al islands, oxygen scavenging is also evidenced on the O ToF-SIMS profile at the bottom of the Al layer close to the base-TiN/Al interface. The O profile then decreases and becomes null in the Al layer before increasing only above the Al/cap-TiN interface. This proves that oxygen scavenging is only localized and limited to the base-TiN/Al interface. It also shows that the aluminum layer is an efficient barrier to the diffusion of air-break oxygen from Cap-TiN layer.

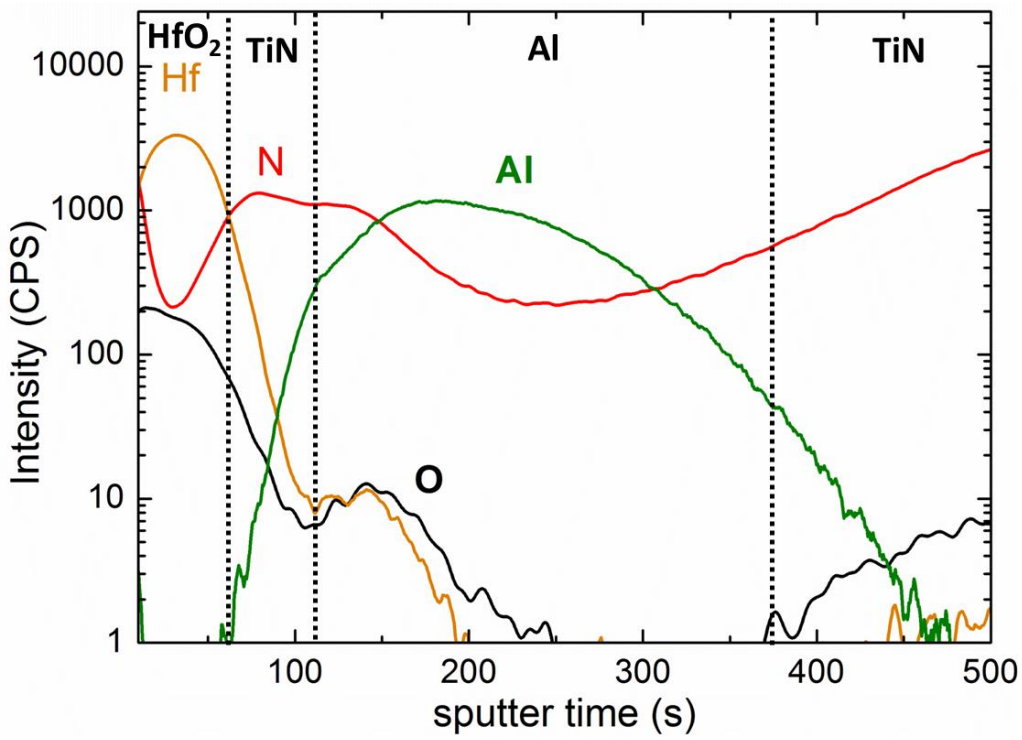


Fig. III-14- *ToF-SIMS spectra of Hf, O, N and Al clusters recorded from a backside prepared SiO_2/HfO_2/TiN/Al/TiN/W sample*

The XPS Al2*p*, Hf4*f*, N1*s* and Ti2*p* core level spectra obtained from a backside prepared HfO_2/TiN/Al/TiN/W stack are shown on figure III-15 and the corresponding peaks decomposition summarized in table III-2. Keeping in mind that the depth probed by XPS is around 5 nm, only the sublayers above the Si substrate up to first nm of the Al layer are probed here.

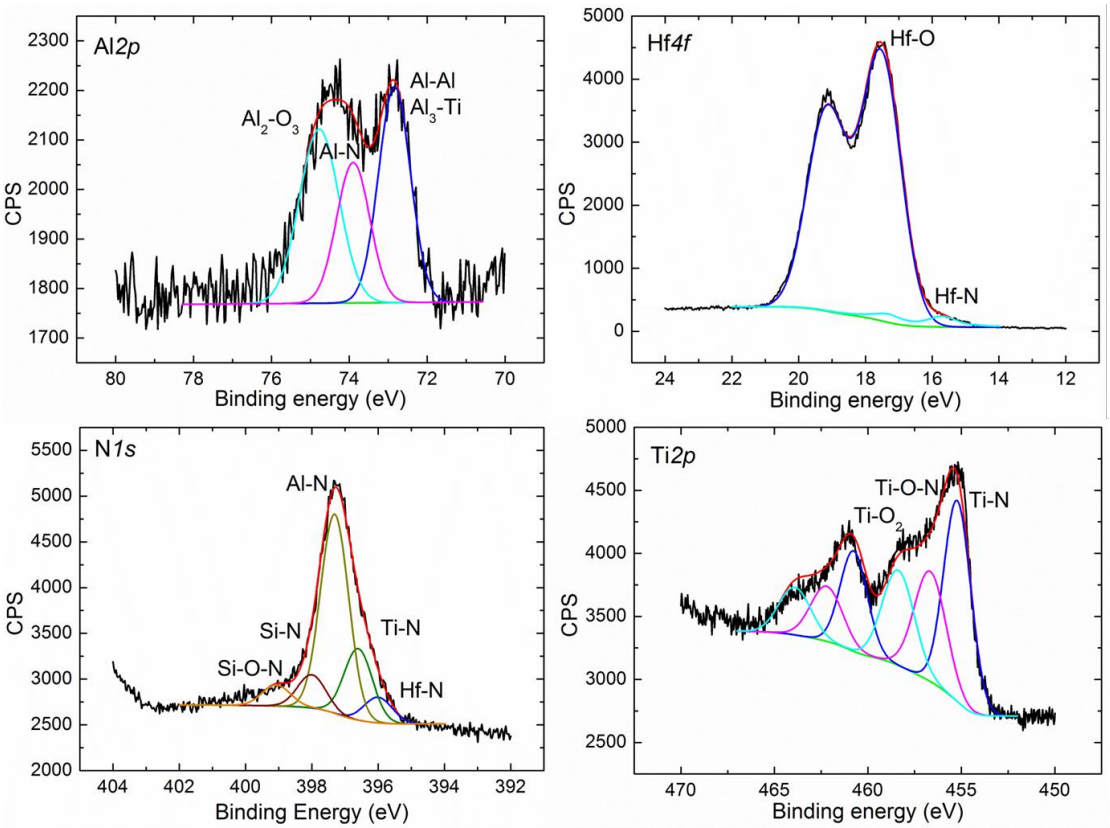


***Fig. III-15**- XPS Hf4f, Ti 2p, N 1s and Al 2p core level spectra obtained from a backside prepared HfO_2/TiN/Al/TiN/W sample*

Ti2*p*	**BE (eV)**	**RA (%)**	**N*1s***	**BE (eV)**	**RA (%)**	**Hf*4f***	**BE (eV)**	**RA (%)**	**Al2*p***	**BE (eV)**	**RA (%)**
Ti-N	455.2	45	Hf-N	396	7	Hf-N	15.7	5	Al-Al	72.8	35
Ti-O-N	456.7	30	Ti-N	396.6	27	Hf-O	17.3	87	Al-N	73.9	31
$Ti-O_2$	458.5	25	Al-N	397.3	44				Al-O	74.7	34
			SiN	398	15						
			Si-O-N	399	7						

***Table III-2**- Binding energies and relative areas (RA) for the different chemical environments extracted from the Ti2p, N1s, Hf4f and Al2p core level spectra of a SiO_2/HfO_2/TiN/Al/TiN/W backside prepared sample*

Hf 4*f* and N1*s* core level spectra reveal low diffusion of nitrogen in the dielectrics with low relative areas of Hf-N, and Si-N in comparison with HfO_2/TiN reference.

The decomposition of the Al2*p* core level spectrum shows an Al equally distributed between Al-Al, Al-O and Al-N. In line with the ToF-SIMS result, the observed oxidation of Al (Al-O) may be related to oxygen scavenging from the SiO_2-IL. This is coherent with the lower oxidation of the base-TiN as observed when comparing Ti *2p* between TiN/Al and TiN electrodes. However, electrical investigation shows only an EOT gain of 0.02nm compared to

the HfO_2/TiN reference, which means that the oxygen scavenging from the SiO_2-IL is weak. From this point of view, a TiN/Al electrode appears more stable against O compared to a TiN/Ti one even the Gibbs free energy for the $2\frac{x}{y}M + SiO_2 \rightarrow Si + \frac{2}{y}M_xO_y$ reaction is close for Ti and Al metals. This higher stability is certainly due the very limited solubility of oxygen in aluminum (close to zero at T=400°C, see Fig. III-16) [Wriedt85, Zhang10] compared to the high one in Ti (around 33%). This suggests that despite to the high affinity of Al for O, it can reduce very low oxygen amount from the SiO_2-IL.

This conclusion gives a further insight about the different behaviors of Al and Ti regarding to O given the study of Kim *et al*. These authors observed a similar behavior to ours comparing SiO_2/HfO_2/Al and SiO_2/HfO_2/Ti stacks (no TiN intermediary layer). The total reduction of the SiO_2-IL was observed for the Ti electrode but not for the Al electrode [Kim04]. If the Ti case was discussed in their study, no explanation was proposed about the higher stability of Al against the SiO_2-IL dielectric compared to Ti.

The formation of Al-N bonds revealed by the components in the Al 2*p* and N 1*s* XPS core level spectra is due to a reaction between the base-TiN and the Al metal layer. The phenomena could be associated to the redistribution of Al and N with a diffusion of Al in the base-TiN and a diffusion of N from the base-TiN into Al as seen on the corresponding Al and N TOF-SIMS spectra. The visibility of the second phenomenon is certainly limited because of the limited depth analysed to the first nanometer of the Al layer. In addition, the amount of nitrogen that could be scavenged by Al from base-TiN is limited due to the low solubility of nitrogen in Aluminum (close to zero at low temperature see figure III-17) [Han04, Hillert92]. We believe that the formation of AlN reduces substantially the amount of Al reaching the HK/MG interface. This is particularly observed in the case of thin Al islands where a low amount of Al is detected at the HfO_2/base-TiN interface. This suggests a barrier effect of base-TiN against Al diffusion. This TiN barrier effect against Al diffusion was also observed in the case of high thermal budget gate first integration where AlN clusters formation was proposed by the authors to explain the TiN barrier behaviour against Al diffusion [Panciera12]. Indeed, when more Al is available, the TiN barrier is weakened and Al can reach the interface as seen for the thick Al island. Therefore, if the Al quantity is large enough, Al diffusion within the base-TiN layer forming Al-N bonds transforms the stoichiometric TiN (50/50) in a slightly substoichiometric nitride, i.e. $TiN_{x<1}$, particularly at the HfO_2/base-TiN interface. Therefore, in addition to the low vacuum work function Al

metal at the HK/MG interface, the associated Ti-rich character could add a contribution to the measured low EWF for Al electrode metal.

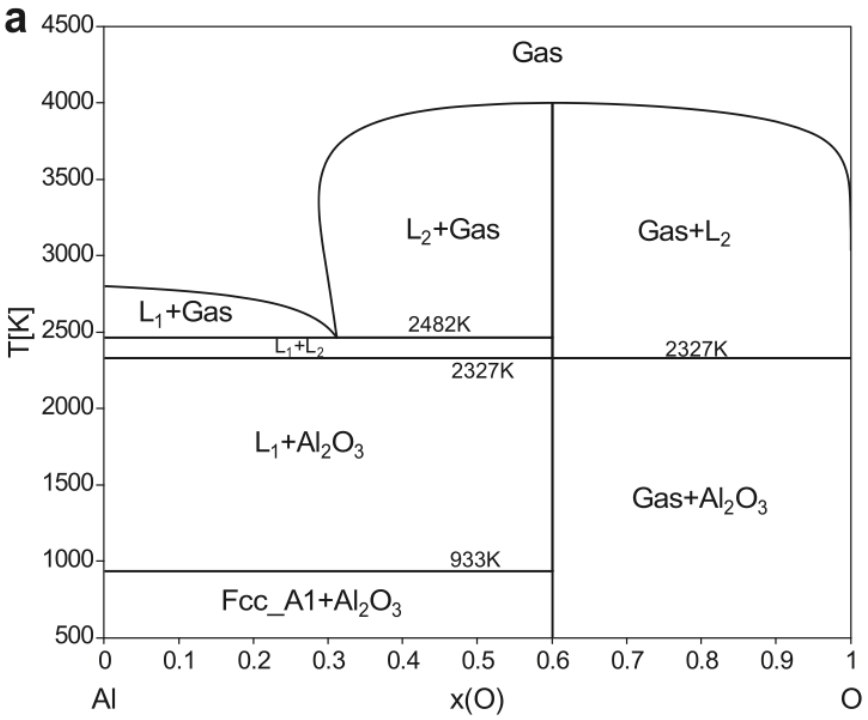


***Fig.III-16**- Al-O binary phase diagram from [Zhang10]*

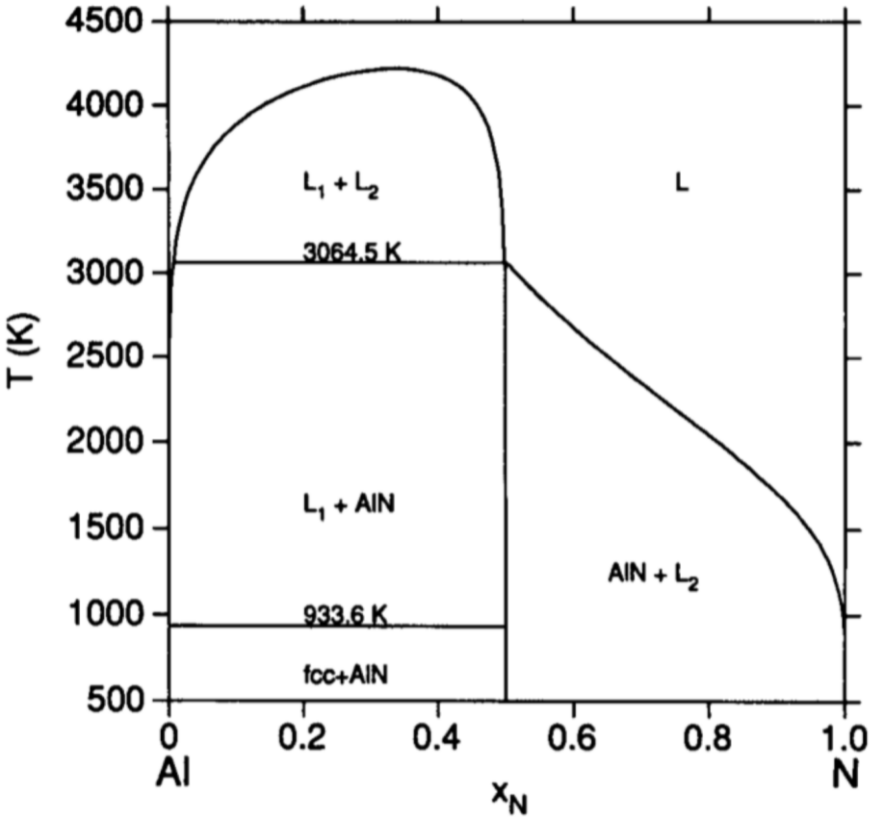


***Fig. III-17**- Al-N binary phase diagram from [Hillert92].*

III-5. Conclusion

In conclusion, with titanium deposition on reference HfO_2/TiN, we obtain an nMOS adapted EWF with 4.1 eV measured on HfO_2/TiN 2nm/Ti 2nm. The mechanism of EWF shift regarding the HfO_2/TiN reference is assigned to the formation of a substoichiometric base-TiN due to Ti addition. However, due to the high reactivity of Ti regarding O (ΔG_{TiO} more negative than ΔG_{SiO2} together with a high amount of oxygen absorbed in Ti bulk (high O solubility), Ti deposition on base-TiN induces a too drastic reduction of oxygen from the SiO_2-IL and HfO_2 oxides which makes it not adapted for final integration as an nMOS metal electrode.

On the other hand, the deposition of a heterogeneous Al layer on the reference HfO_2/TiN leads to an nMOS adapted EWF of 4.25 eV. The main mechanism of the EWF shift regarding the HfO_2/TiN reference is assigned to the diffusion and the segregation of low work function Al to the HfO_2/TiN interface. This electrode exhibits a high stability toward oxygen reduction from the dielectrics at 400°C which avoids aggressive O scavenging and MOSCAP short circuit. This is assigned to the lower solubility of O in Al compared to Ti which enables, through the modulation of the Al layer thickness, to control the amount of oxygen scavenged from the dielectric. We also notice the same behaviour of Al toward N than toward O where the modulation of Al thickness induces more or less nitrogen redistribution from base-TiN and thus enables the control Al amount diffusing through HfO_2/TiN interface.

In the next chapter, we will investigate the alloying of Ti and Al with TiAl deposition on HfO_2/TiN reference and the conjugation of their intrinsic behaviours with respect to O and N with the aim to favour a controlled stability and avoid the thickness heterogeneity of the layer for a better scaling of the EOT and modulation of the EWF. In addition, for a further investigation, $TiAlN_x$ monolayer deposition on HfO_2 will be investigated with a focus on nitrogen amount impact on gate EOT and EWF modulation.

Chapter IV

TiAl(N) metal alloys:
Role of O and N on EWF modulation and EOT scaling

IV-1. Introduction

We will use here the knowledge gained through the previously studied elementary TiN/Ti and TiN/Al electrodes. We will try to take profit from their individual characteristics by alloying them, depositing TiAl layer on the HfO_2/TiN reference. Knowing the important role of N in these stacks, we will also consider the more complex system, which consists in direct deposition of the ternary $TiAlN_x$ alloy on HfO_2. This will be done with a particular focus on the impact of nitrogen amount in $TiAlN_x$ on the electrode EWF and EOT variation.

Here again, systematic analytical investigations are conducted using XPS, TOF-SIMS (submillimetric scale) and STEM-EDX (nanometric scale) techniques with the aim to correlate the chemical species distribution across the stack and particularly at the HK/MG interface to the variation of the electrode EWF and stack EOT. Interpretation of the results will be also based on thermodynamic considerations

IV-2. TiN/TiAl bilayer: a better and homogenous scavenger

We observed previously that the aluminum thickness deposited on HfO_2/TiN has an effect on the chemical species distribution in the gate electrode. Therefore two stacks HfO_2 2nm/TiN 2nm/TiAl/TiN 15nm/W were prepared, one with a thin TiAl layer (2.5nm) and another with a thick TiAl layer (7.5 nm). Ti and Al atomic compositions in the alloy were 0.8 and 0.2 respectively. For simplicity, the alloy will be noted TiAl in the following.

The Cs-corrected HRTEM micrographs of the stacks are shown on figure IV-1. As for the HfO_2/TiN reference stack, one can see the two amorphous thin SiO_2 (0.5-0.7 nm) and HfO_2 (~1.8nm) layers and the polycrystalline base-TiN, TiAl, cap-TiN and W layers. The layers with heavier elements appear darker. White dashed lines inside the base-TiN/TiAl/cap-TiN have been added to help the reader to distinguish the frontier between the three sublayers. The frontiers between the sublayers are best seen on the chemical STEM-EDX maps of figure IV-2. This time, the TiAl layer is homogeneous in thickness suggesting that alloying Ti with Al avoids the high roughness observed with only pure Al layer.

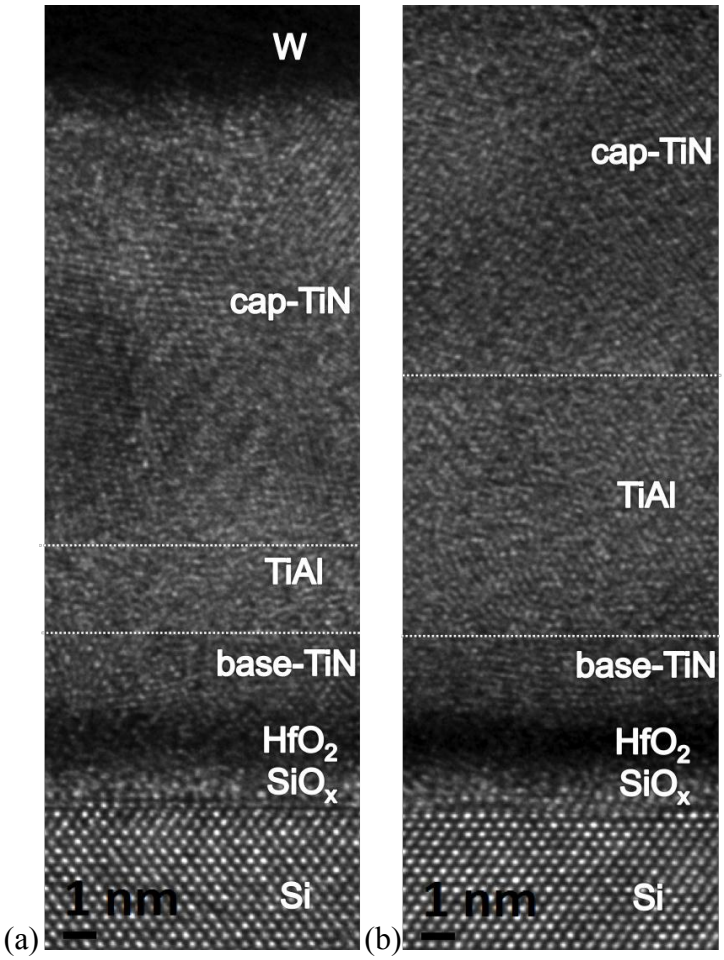


Fig. IV-1*- Cs-corrected HRTEM micrograph of Si/SiO_2/HfO_2/TiN/TiAl/TiN/W stacks with (a) a thin (2.5 nm) TiAl layer and (b) a thick (7.5 nm) TiAl layer*

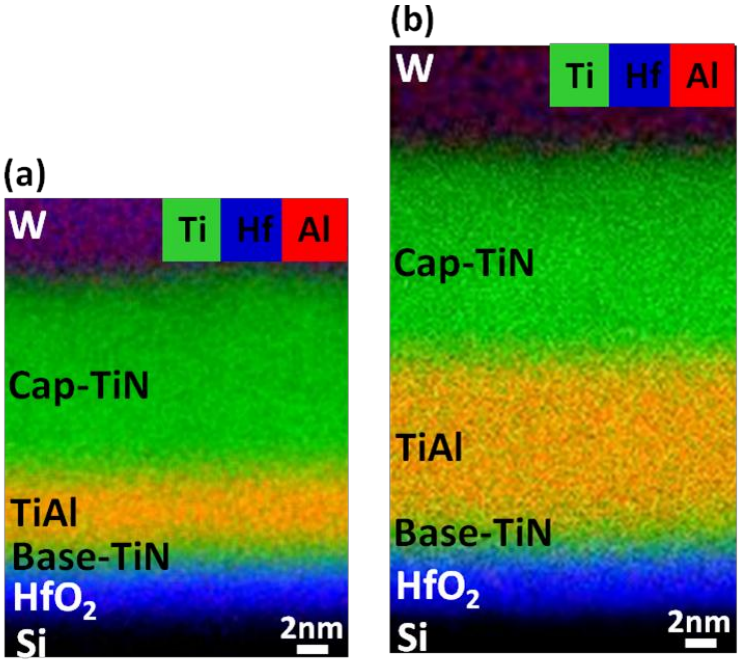


Fig. IV-2*- STEM-EDX maps of HfO_2/TiN/TiAl/TiN electrodes with (a) a thin (2.5 nm) TiAl layer and (b) a thick (7.5 nm) TiAl layer*

On the STEM-EDX profiles obtained for both thin and thick TiAl electrode (Fig. IV-3), the distribution of the elements has common and different features than the one obtained for the Al-based and Ti-based electrodes. Let us comment these different features.

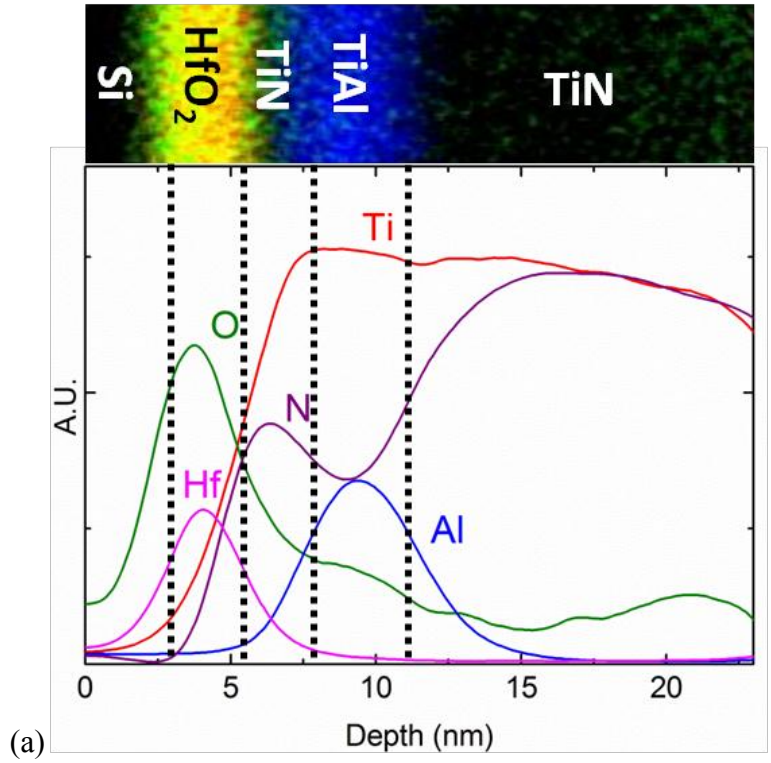
First of all, O and Hf profiles are nearly aligned (or aligned) for the thin (or thick) TiAl electrode, thus supporting the low thickness of the SiO_2 IL measured by HRTEM. This is coupled to a visible partial oxidation of the entire TiAl layer. Remember that only the bottom part of the Al layer was oxidized with the Al-based electrode and oxygen was largely incorporated in the whole α-Ti layer in the case of the Ti-based electrode. Alloying Ti with Al thus reinforce the scavenging character of the metal electrode but not in a drastic way as for the Ti-based electrode. We notice also that even increasing by 3 times the TiAl thickness from 2.5 to 7.5nm, no aggressive scavenging of oxygen from the dielectrics was induced despite the Ti-rich nature of TiAl (Ti=0.8 at%, Al=0.2at%), which highlights the high stability of TiAl toward oxygen. This suggests that alloying Al with Ti results in a more stable gate electrode while keeping a significant O scavenging for an efficient EOT scaling. This point will be discussed in details further.

Second, Ti and N profiles evidence some substoichiometry for N in the base-TiN layer including the HfO_2/base-TiN interface. The phenomenon is the more pronounced, the thicker the TiAl layer (2.5nm versus 7.5 nm). This is assigned to the scavenging of nitrogen from base-TiN by the TiAl layer. Significant nitrogen scavenging from TiN is observed right from the lowest thickness of TiAl, which indicates a similar chemical behavior than the Ti-based and Al-based electrodes.

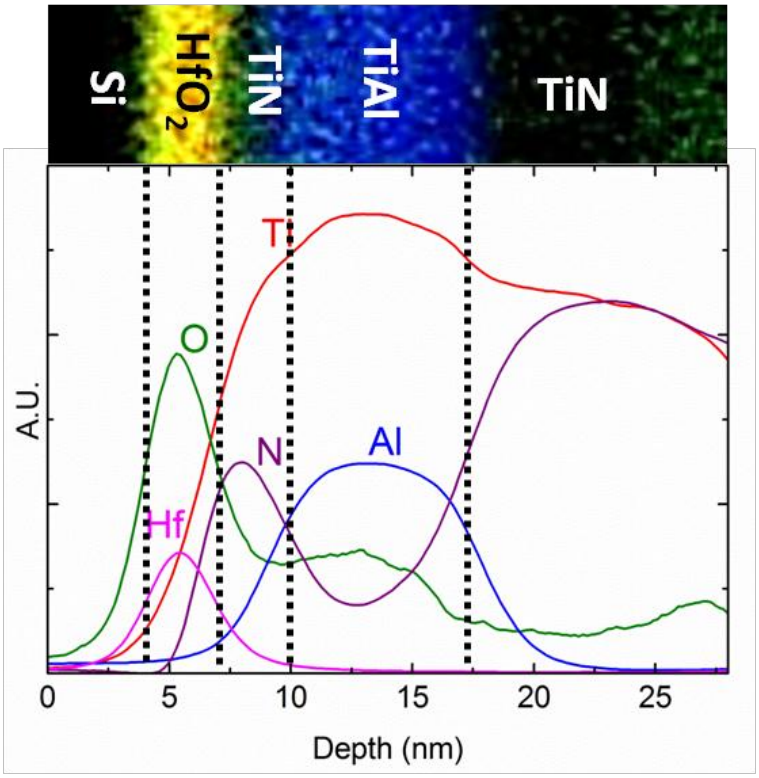
Finally, what is noticeable for this TiAl-based metal electrode is that the Al profile shows a low diffusion of aluminum in TiN metal layer with a significant reduction of aluminum amount when going deeper in base-TiN. Therefore, no aluminum is detected at HfO_2/base-TiN interface contrary to what happens with the Al-based electrode.

In order to be viable for sub 20nm CMOS integration, the layer thicknesses must be reduced to the minimum in order to deposit enough contact metal plug matter in the cavity which warrant the lowest possible gate resistance required for the good operation of CMOS circuits. Regarding this condition, a thin TiAl layer seems to be more adapted for integration. We will develop further material investigations using the 2.5nm TiAl-based gate. As for the pure aluminum stack, less localized techniques such as ToF-SIMS and XPS analyses have

been achieved to get complementary data for a deeper understanding of the chemical species behavior in the MOS electrode.



(a)



(b)

Fig. IV-3*- STEM-EDX map of Si/SiO_2/HfO_2/TiN/TiAl/TiN/W stacks and corresponding Hf, O, N, Ti and Al profiles across the stack with localization of the different sublayers for a (a) thin TiAl layer (2.5 nm) and a (b) thick TiAl layer (7.5 nm)*

The ToF-SIMS analysis performed on a micrometric-sized area presented in figure IV-4 confirms the three main observations reported from the local STEM-EDX analysis:

- the high contribution of the TiAl layer to oxygen scavenging from the SiO_2 IL as shown by the O profile increase and in phase with the Al profile in the TiAl layer,
- the N redistribution in the TiAl layer, nitrogen being scavenged from base-TiN by the TiAl layer,
- the limited diffusion of aluminum to the base-TiN with no aluminum detected at HfO_2/base-TiN interface.

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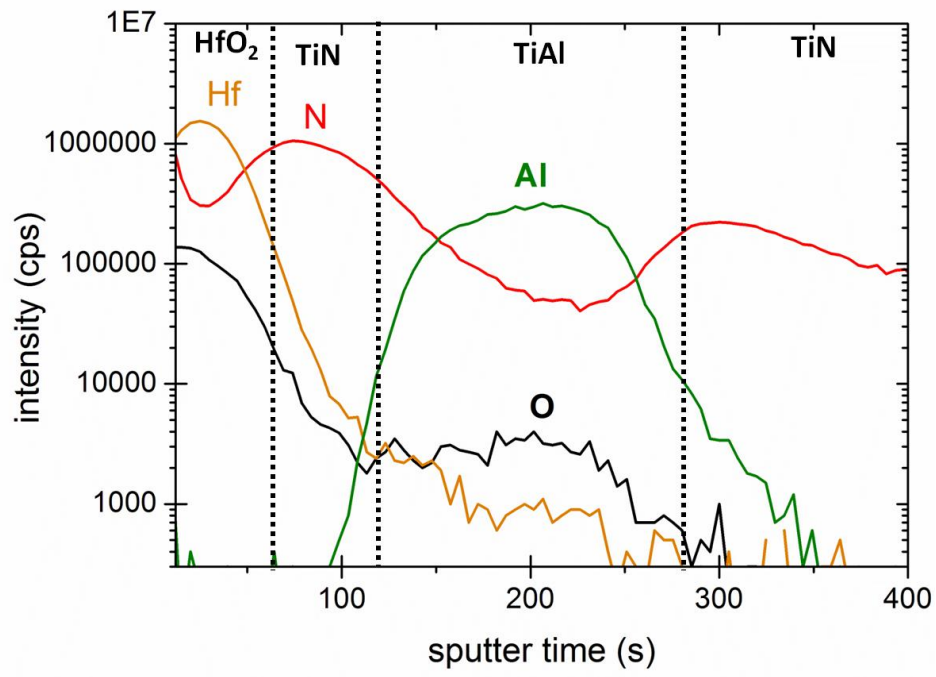

***Fig. IV-4**- ToF SIMS profiles of HfO_2, O, CN, Al and TiO clusters in the SiO_2/HfO_2/TiN/TiAl 2.5nm/TiN/W gate electrode.*

The XPS Al2*p*, Hf4*f*, N1*s* and Ti2*p* core level spectra obtained from a backside prepared HfO_2/TiN/TiAl 2.5 nm/TiN/W stack are shown on figure IV-5 and the corresponding peaks decomposition summarized in table IV-1.

Hf 4*f* and N1*s* core level spectra reveal low diffusion of nitrogen in the dielectrics with low relative areas of Hf-N and Si-N in comparison with the HfO_2/TiN reference.
Besides, N *1s* spectrum shows a clear predominance of AlN environment compared to TiN with 60% and 20% calculated relative areas, respectively. As pointed out for HfO_2/TiN/Al

electrode analysis and since the depth probed by XPS in back side sample is limited to about 5nm, the contribution of AlN can be related to both the scavenging of N by the Ti-rich TiAl electrode and the concomitant diffusion of aluminum in the base-TiN layer where aluminum bounds to nitrogen. The resulting substoichiometric composition of base-$TiN_{x<1}$ which was observed by STEM-EDX analysis is confirmed here because the Ti-N binding energy in the Ti*2p* core level spectrum is between the ones of pure metallic Ti (Ti-Ti : 454eV) and stoichiometric Ti-N. In addition, Ti*2p* spectrum reveals the low oxidation of base-TiN which is due to oxygen scavening by TiAl reactive layer.

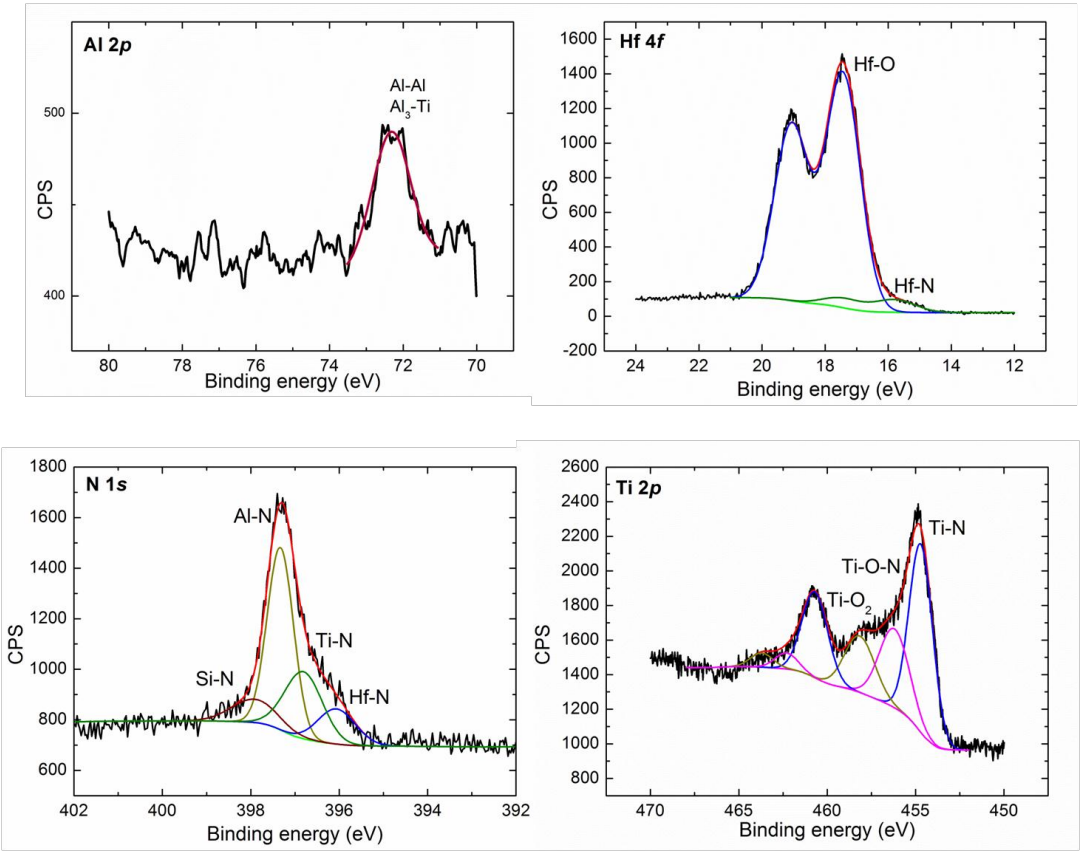

Fig. IV-5*- XPS Hf4f, Ti 2p, N 1s and Al 2p core levels spectra obtained from a backside prepared HfO_2/TiN/TiAl 2.5nm/TiN/W sample.*

Note that the Al 2*p* core level spectrum is very noisy with low statistics obtained from the backside prepared sample. Only metallic Al-Al or Al_3-Ti environment can be identified. Therefore, frontside XPS analysis (Fig. IV-6) has been conducted on HfO_2/base-TiN 2nm/TiAl 2.5nm/cap-TiN 2nm with a thin TiN-cap and without metal plug. Frontside Al *2p* core level spectrum reveals the predominance of Al-N environment compared to metallic Al-

Al or Al_3-Ti and Al_2-O_3 which confirms that Al is bonded predominantly with nitrogen in the gate electrode.

Ti*2p*	BE (eV)	RA (%)	N*1s*	BE (eV)	RA (%)	Hf*4f*	BE (eV)	RA (%)	Al*2p**	BE (eV)*	RA (%)*
Ti-N	454.6	52	Hf-N	396	10	Hf-N	15.8	4	Al-Al	72.4	27
Ti-O-N	456.2	28	Ti-N	396.6	20	Hf-O	17.4	96	Al-N	73.9	51
Ti-O_2	458.2	20	Al-N	397.3	62				Al-O	74.8	22
			SiN	398	8						

***Table IV-1**- Binding energies and relative areas (RA) for the different chemical environments extracted from the Ti2p, N1s, Hf4f and Al2p core level spectra of a SiO_2/HfO_2/TiN/TiAl 2.5nm/TiN/W backside prepared sample. * These data have been obtained on the frontside prepared sample*

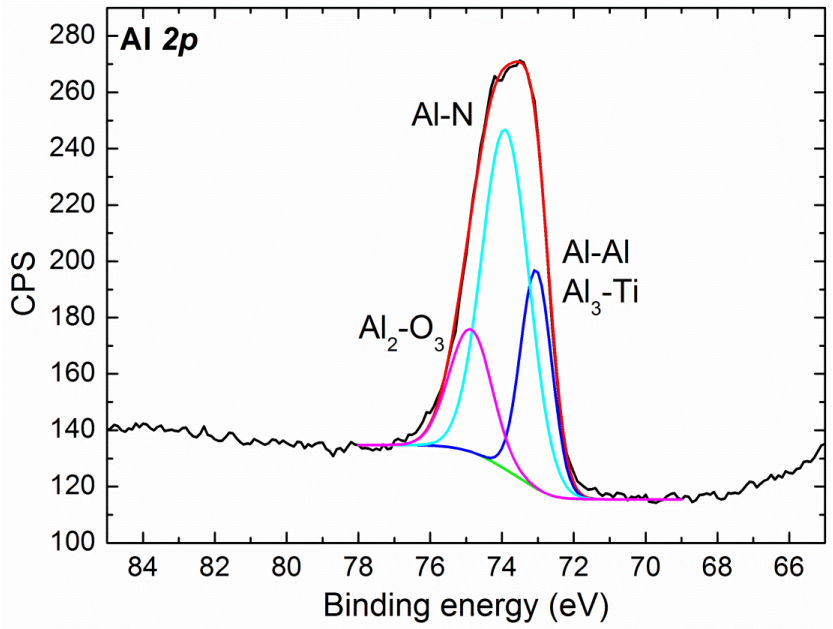

***Fig. IV-6**- XPS Al 2p core level spectrum obtained from a backside prepared HfO_2/TiN/TiAl 2.5nm/TiN/W sample*

To conclude about the effects of the deposition of a Ti-rich TiAl layer on the reference HfO_2/TiN, we will consider the EWF and EOT parameters of all the metal electrodes studied till now. The corresponding data are gathered on figure IV-7 and in table IV-2.

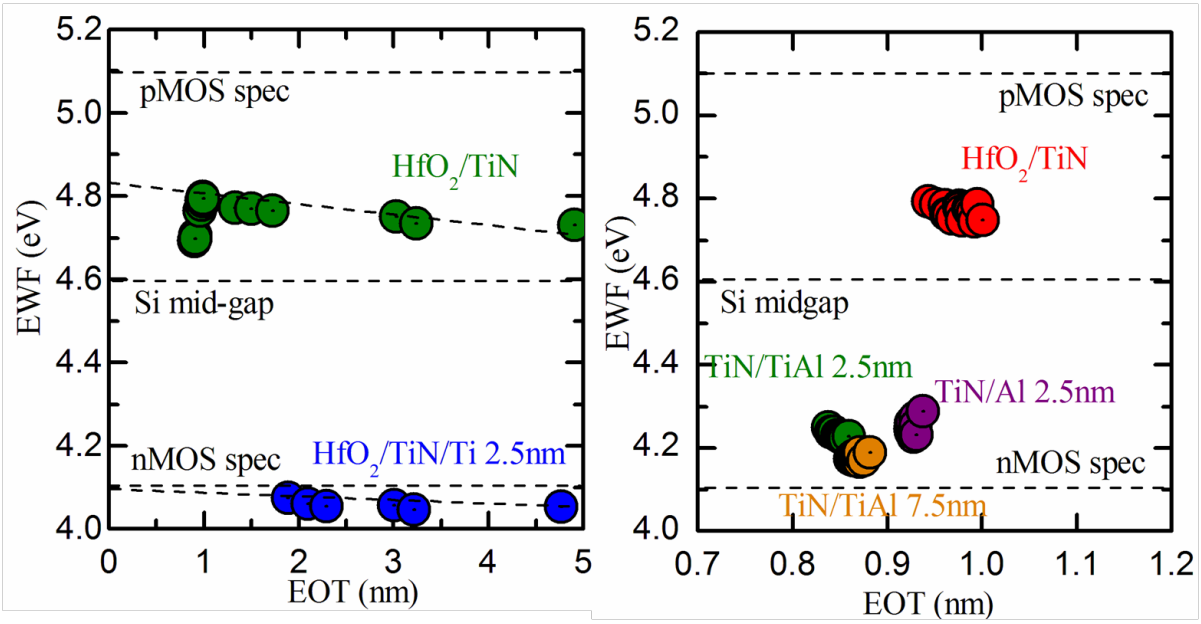

***Fig. IV-7**-EWF versus EOT measured (left) on HfO_2/TiN, HfO_2/TiN/Ti 2.5nm capacitors (beveled SiO_2 IL) and (right) on HfO_2/TiN, HfO_2/TiN/Al 2.5nm, HfO_2/TiN/TiAl 2.5nm and 7.5nm capacitors*

MG (HfO_2/TiN 2nm/MG/TiN/W)	EWF (eV)	EOT (nm)
Reference (no MG)	4.85	0.95
Ti 2.5nm	4.1	1.8 (on bevel)
Ti 8nm	Short circuit	Short circuit
Al 2.5nm	4.25	0.93
TiAl 2.5nm	4.24	0.83
TiAl 7.5nm	4.18	0.86

***Table IV-2** – Summarized EWF and EOT values obtained with different metals deposited on the HfO_2/TiN reference*

Compared to the p-MOS character obtained with the HfO_2/TiN reference MG, the deposition of thin Ti or Al or TiAl layers on HfO_2/TiN results in a significant shift of the electrode EWF toward the n-MOS side. Indeed, the shifts are -0.6eV for the 2.5nm thick Al or TiAl layers and, -0.68eV and -0.75eV for the 7.5nm TiAl and 2nm Ti layers, respectively.

In parallel, a significant EOT scaling is realized mainly for the TiAl-based electrode with a decrease of 0.12 and 0.09 nm for the 2.5 and 7.5nm TiAl layers compared to 0.95nm recorded

for TiN reference, respectively. The Ti and Al layers were respectively too strong or similar scavengers compared to the reference TiN-based MG.

Alloying aluminum with titanium avoids the aggressive scavenging of oxygen from the dielectric stack and this even for the thicker TiAl layer. Let us comment why the TiN/TiAl metal electrode is more stable toward oxygen than the TiN/Ti one. On the Ti-Al-O ternary phase diagram shown on figure IV-8 (this diagram is for 800°C, we did not find a diagram at lower temperatures), the point which corresponds to the initial TiAl alloy composition (Ti=0.8 at%, Al=0.2 at%) is located at the αTi+Ti_3Al border domain and even a little nearer to the Ti edge, if we recall that a part of the Al atoms is consumed by the Al-N bonds formed near the base-TiN/TiAl interface (see ToF-SIMS of Fig. IV-4 and N*1s*, Al*2p* XPS of Fig. IV-5 and IV-6). Adding O to the TiAl alloy implies to enter the Ti+Ti_3Al domain where Ti atoms are distributed between α-Ti and Ti_3Al and O is dissolved in α-Ti. Therefore, compared to the pure Ti MG case, there is less α-Ti available for dissolving O in the case of the TiAl alloy compared to the pure Ti case. The scavenging occurs but in a limited way compared to pure α-Ti. In other words, alloying Al with Ti reduces the capability of Ti to dissolve oxygen.

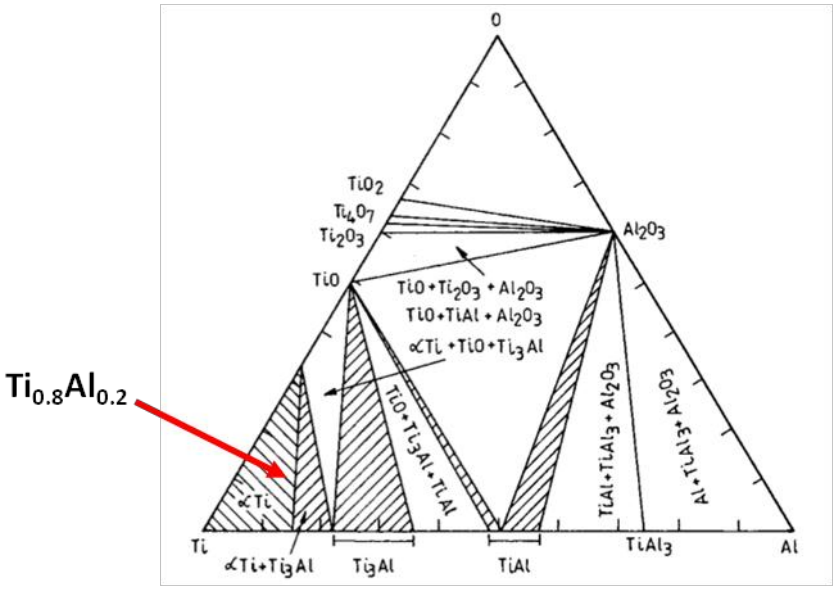

Fig. IV-8*-Ti-Al-O ternary phase diagram at 800°C, from [Das02]*

The low EWFs, 4.24eV and 4.18eV, respectively obtained with the thin and thick TiAl-based electrodes are similar to the one measured by Veloso *et al.* on a TiN/TiAl stack with a thickness ratio equal to 1 i.e. same TiN and TiAl thicknesses. Note that the increase of the

TiN/TiAl thickness ratio from 1 to 2 in their work is accompanied by a degradation of the EWF [Veloso11, Veloso13] unlike our case (see Fig.IV-7, thick TiAl with thickness ratio of 3). The low EWF was assigned to Al diffusion into the underneath TiN layer based on a ToF-SIMS analysis. However, the work lack of extended materials investigation and discussion in order to support the conclusion. In our study, based on STEM-EDX and ToF-SIMS profiles for Al, Hf, Ti and N elements but also on the basis of the Ti2*p* and Al2*p* XPS core level spectra, we are able to conclude that Al diffusion in the base-TiN is limited with no aluminum detected at the HfO_2/base-TiN interface but that a substoichiometric base-$TiN_{x<1}$ is formed at this interface. Therefore, we conclude, differently from the study of Veloso, that in the case of HfO_2/TiN/TiAl with a low Al content (20 at%), aluminum has no effect on the EWF modulation. In our case, the formation of Ti-rich base-$TiN_{x<1}$ induced by TiAl, nitrogen scavenging is the main chemical mechanism resulting in the observed low EWF. Here again, the limited diffusion of aluminum is due to the base-TiN barrier effect against Al diffusion with AlN formation, a phenomenon already observed for HfO_2/TiN/Al electrode and to the intrinsic low Al content (20 at%) of the TiAl MG.

For the previous discussions, for sake of simplicity, we considered separately the TiAl behavior against N and O. Indeed, Ti has similar affinity toward O and N and similarly Al has similar affinity but different efficiency toward O and N. More precisely, when these elements are alloyed in TiAl, the Ti character is favorable to an N scavenging from the base-TiN in addition to the formation of Al-N bonds due to Al diffusion in the base-TiN. The resulting formation of the substoichiometric $TiN_{x<1}$ at the HfO_2/base-TiN interface is responsible for the n-EWF. The Al character in TiAl preserves the dielectrics from strong oxygen scavenging by reducing α-Ti solubility against oxygen. These simple effects are even more complex and intricate in $TiAl_xN_y$ which is formed on top of HfO_2 by N and Al diffusions. Next step is to study the direct deposition of $TiAlN_x$ monolayers on HfO_2 and investigate the impact of nitrogen flow modulation on the EWF and EOT variations of HfO_2/TiAlN electrodes.

IV-3. $TiAlN_x$ single layers: an adjustable EWF MG with sub-nm EOT

In the previous section, we investigated the EWF modulation induced by a bi-layer in-situ deposited on HfO_2 oxide i.e. TiN/TiAl. As we used the low thermal budget gate last approach, the EWF modulation was achieved through HfO_2/base-TiN chemical interface control. In the case of TiAl deposition on HfO_2/base-TiN, we highlighted the role of nitrogen amount in base-TiN on the EWF modulation. Besides, the evaluation of TiAl scavenging properties enabled an advanced understanding of EOT scaling mechanisms. In this section, we will evaluate the impact of process parameters variation on the electrode EWF and stack EOT modulations of ternary $Ti_xAl_yN_z$ metal layers directly deposited on HfO_2. We will focus in particular on the nitrogen/titanium ratio content effect. For this, three nitrogen flows were used during the deposition of the $Ti_xAl_yN_z$ layers on HfO_2. The corresponding compositions are indicated in Table IV-3 together with a simplified notation. Al content is nearly constant in the three layers, the N/Ti (x) ratio varies. Like for the other metallic layers (except the Al one), the XRR measured thickness of the 3 TiAlN layers correspond to the targeted one, i.e. 3.5 ±0.3nm.

Flow	Low-N flow	Medium-N flow	High-N flow
Compositions	$Ti_{45}Al_{18}N_{37}$	$Ti_{37}Al_{17}N_{46}$	$Ti_{33}Al_{16}N_{51}$
x=N/Ti	0.82	1.24	1.55
Notation	$TiAlN_{x<1}$	$TiAlN_{x>1}$	$TiAlN_{x>>1}$

***Table IV-3**- Compositions of the ternary TiAlN deposited on HfO_2 for three different nitrogen flows and their simplified notation (x=N/Ti)*

Like for the TiAl-based stacks, the succession of the different layers in the 3 $Si/SiO_2/HfO_2/TiAlN_x/TiN/W$ stacks can be seen in the HRTEM images of figure IV-9 but the frontier between the polycrystalline TiAlN and cap-TiN layers is difficult to define. Therefore, to guide the reader, thin dashed lines have been added on the image based on the STEM-EDX maps in figure IV-10, which enables the identification of the different layers and indicates their homogeneous thicknesses and compositions.

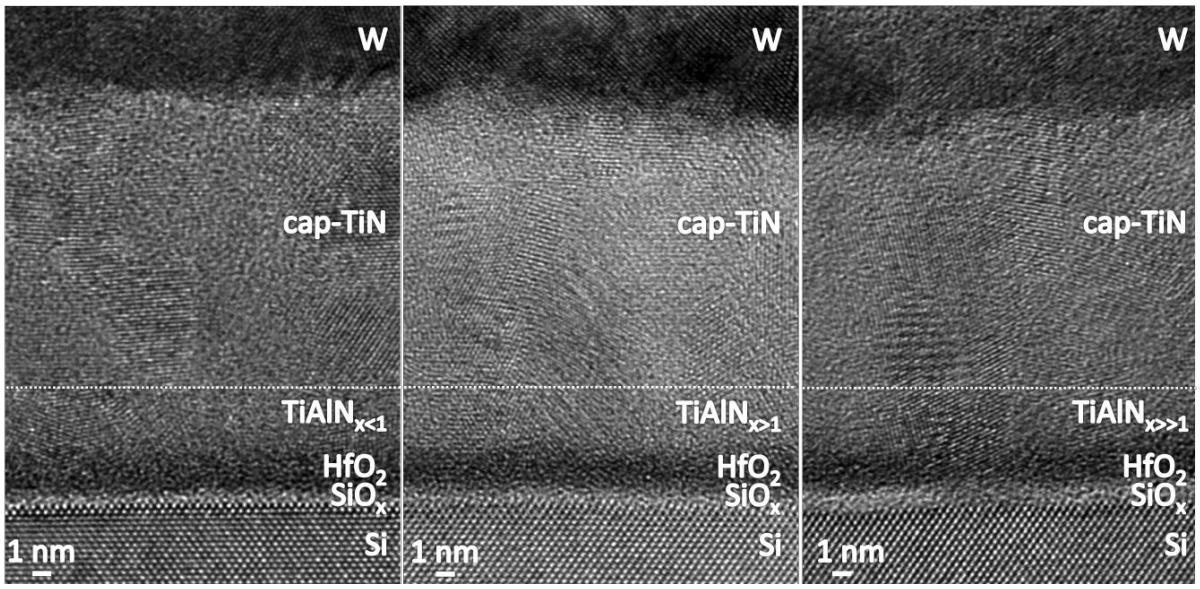

***Fig. IV-9**- Cs-corrected HRTEM micrographs*
for the (a) low-N, (b) medium-N and (c) high-N flow in the $TiAlN_x$ metal layer

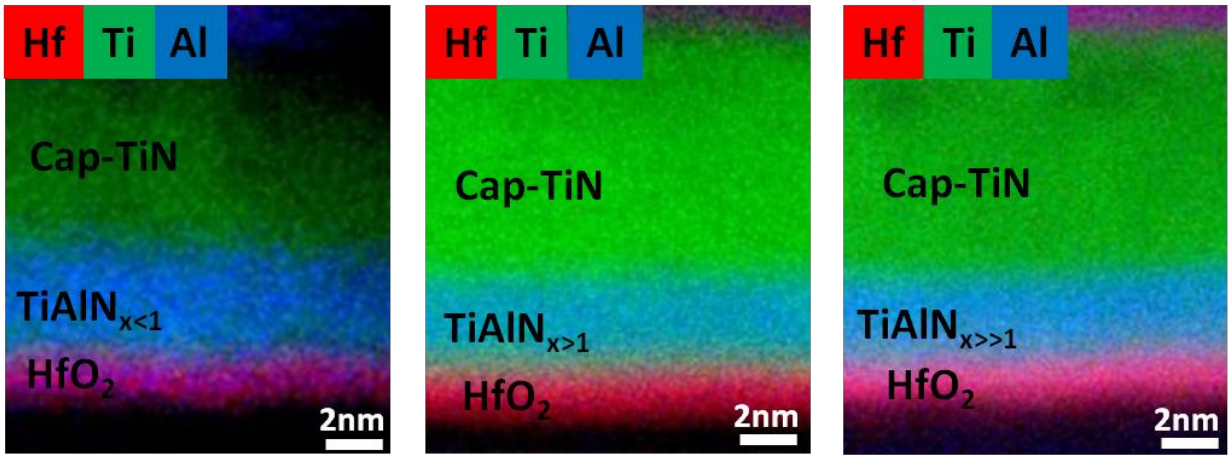

***Fig. IV-10**- STEM-EDX maps of the (a) low, (b) medium and (c) high N flow in the $TiAlN_x$ metal layer*

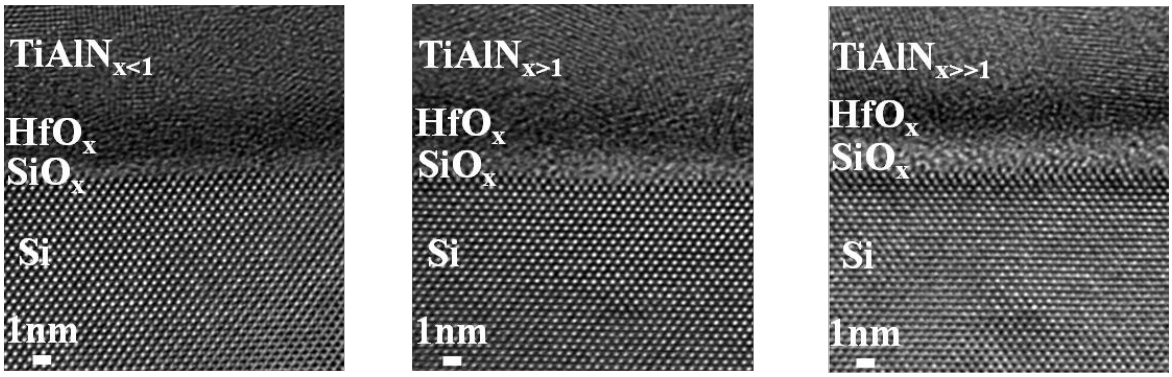

***Fig. IV-11**- Cs-corrected HRTEM micrographs*
for the (a) low, (b) medium and (c) high N flow in the $TiAlN_x$ metal layer

What is noticeable and better seen on the higher magnified images of figure IV-11 is the variation of the SiO_2 IL thickness regarding the nitrogen flow. Decreasing the N flow decreases the SiO_2 IL thickness. This is confirmed by the Hf and O STEM-EDX profiles of figure IV-12. The shift between the O and Hf maxima is the less, the less the flow of N is. This suggests that the oxygen scavenging from the SiO_2 IL is related to the nitrogen flow used during $TiAlN_x$ deposition.

The comparison of N and Ti profiles for the different N flow TiAlN electrodes reveals a significant modification of nitrogen and titanium distribution in the gate. For the low N TiAlN, the intensity of the Ti profile is above the one of the N profile which means a N/Ti ratio lower than 1 suggesting a substoichiometric $TiAlN_{x<1}$ layer. In contrast, the intensity of the Ti profile is below the one of the N profile for both medium and high N flow. The situation is more pronounced for the high-N flow. This indicates overstoichiometric $TiAlN_{x>1}$ layers with N/Ti>1 for the medium N and N/Ti>>1 for the high N flow, respectively. These compositions are true inside the TiAlN layer but also at the HfO_2/TiAlN interface. What is noticeable also is the N profile for the high N flow which goes deeper into HfO_2 compared with the medium and low N $TiAlN_x$ revealing significant nitrogen diffusion through HfO_2.
N-flow variation induces a slight modification of Al amount present in $TiAlN_x$. However, no impact is reported on the Al amount present at the HfO_2/$TiAlN_x$ interface. Al has no differentiating effect with regard to the N flow.

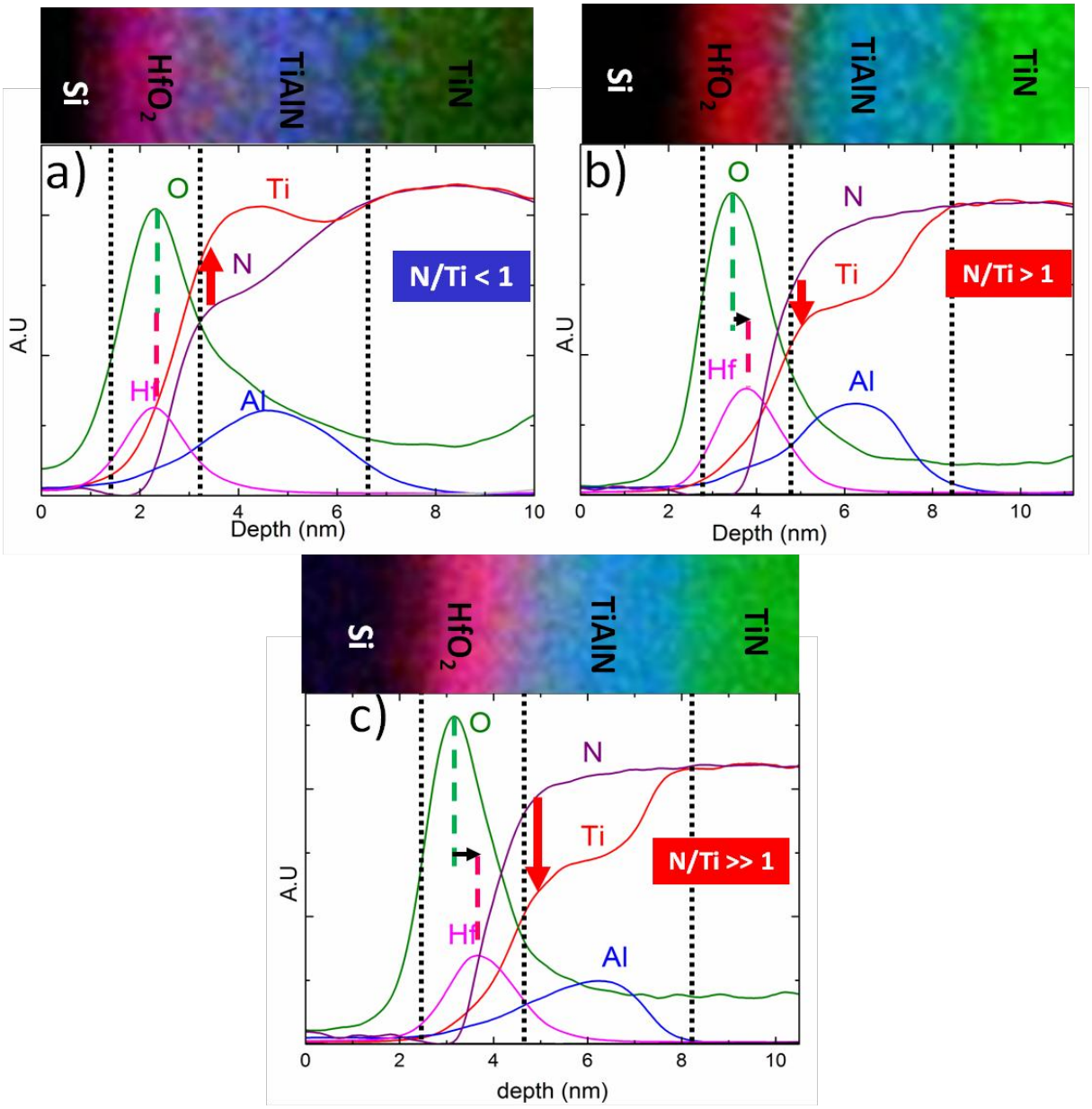

***Fig. IV-12**- STEM-EDX map of Si/SiO_2/HfO_2/TiAlNx/TiN/W stacks and corresponding Hf, O, N, Ti and Al profiles across the stack for a (a) low-N flow, (b) medium-N flow and (c) high-N flow*

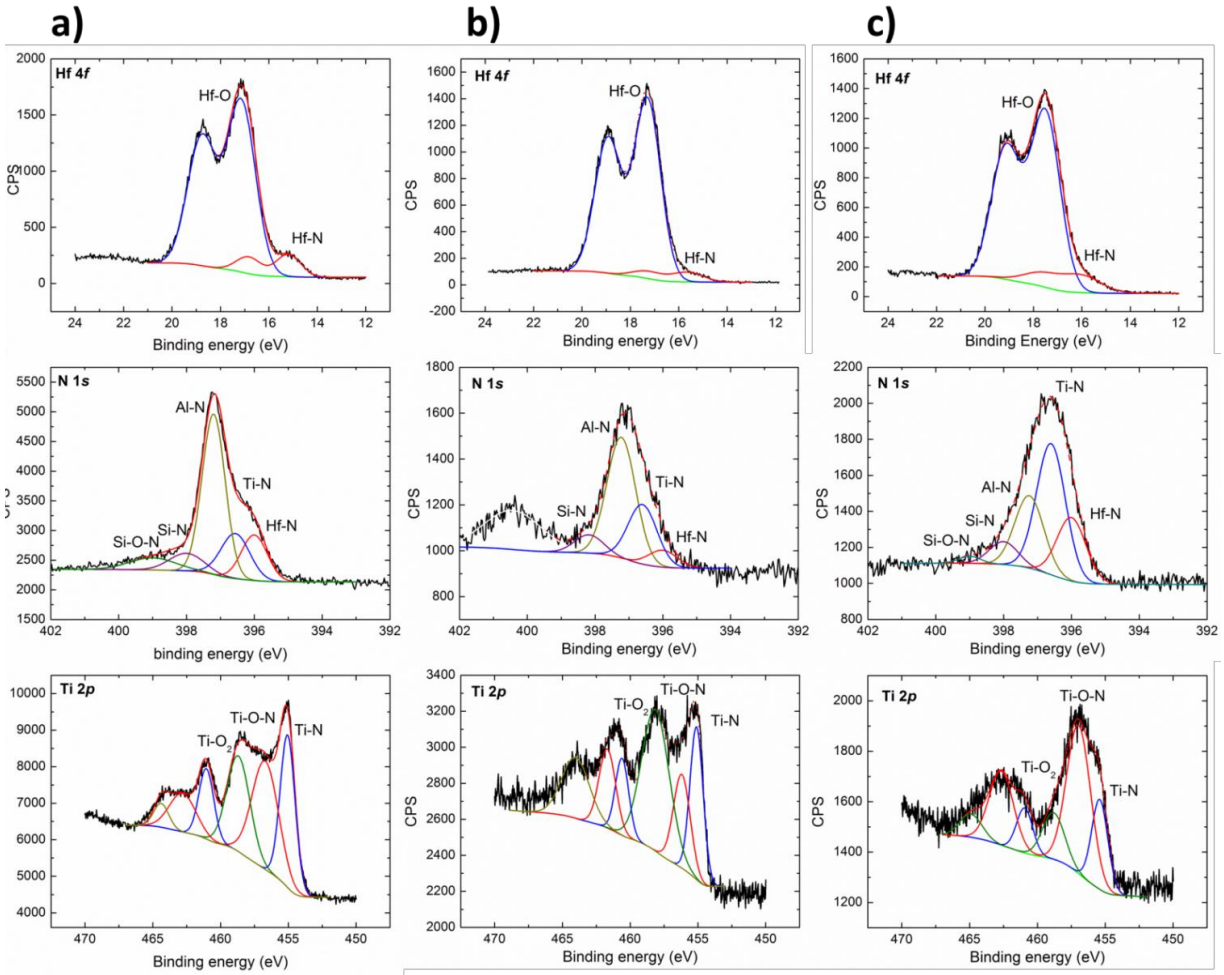

***Fig. IV-13**- XPS Hf4f, N 1s and Ti 2p core level spectra obtained from backside prepared HfO_2/TiAlN/TiN/W electrodes deposited with a) low, b) medium and c) high nitrogen flows*

Ti*2p*	BE (eV)			N*1s*	BE (eV)			Hf*4f*	BE (eV)		
	low N	med. N	high N		low N	med. N	high N		low N	med. N	high N
Ti-N	455	455	455.4	Hf-N	396	396	396	Hf-N	15.2	15.6	16
Ti-O-N	456.5	456.1	456.9	Ti-N	396.6	396.6	396.6	Hf-O	17.1	17.3	17.5
$Ti-O_2$	458.6	458.2	458.8	Al-N	397.3	397.3	397.3				
				Si-N	398	398	398				
				Si-O-N	399	399	399				

***Table IV-4**- Binding energies for the different chemical environments extracted from the Ti2p, N1s and Hf4f core level spectra of a SiO_2/HfO_2/TiAlN/TiN/W backside prepared sample*

Table IV-4 summarizes the binding energies of the chemical environments identified for Hf4*f*, N1*s* and Ti2*p* core level spectra registered on backside prepared samples and shown on figure IV-13. For these TiAlN-based electrodes, the probed depth allows to integrate nearly all the stack from the SiO_2-IL to nearly the top of the TiAlN layer.

The main difference/similarity between the three gate stacks is the respective contribution of N-Al and N-Ti to the N1*s* core level spectra (Fig. IV-13, second row). Al-N peaks are the major contributions for both low and medium N $TiAlN_x$. Therefore, despite the different amounts of nitrogen recorded by STEM-EDX for the low and medium N $TiAlN_x$, i.e. corresponding to N/Ti<1 and N/Ti>1 respectively, a similar behavior is observed for the main contribution to the N chemical environment. In contrast, for the two overstoichiometric films, i.e. both with N/Ti>1, different chemical environment is observed with a predominant Ti-N contribution for the high N $TiAlN_x$ film.

Another noticeable point is the significant Hf-N contribution observed for the high N $TiAlN_x$ which is a little higher than the one in the low N $TiAlN_x$ sample but much higher than the one in the medium N $TiAlN_x$. Before going to some explanation, let us precise that the deposition sequence for the first monolayers of the TiAlN films was not exactly the same for the three samples. Indeed, nitrogen flow gradient is used during first monolayer deposition for medium and high N $TiAlN_x$ whereas constant nitrogen flow is used for low-N TiAlN as soon as the first monolayers are deposited. This results in a higher nitrogen amount at the beginning of the low-N TiAlN process deposition compared to the medium and high-N TiAlN. This could explain the higher Hf-N relative areas compared to the medium N TiAlN. If now we go back to the two comparable samples, the medium and high N $TiAlN_x$ stacks, the higher Hf-N amount observed also for the high-N flow sample but also the merging Si-O-N contribution confirms the high diffusion of nitrogen in the dielectrics evidenced by STEM-EDX for this sample (Fig. IV-13(c)).

Finally, oxygen and nitrogen environments in the Ti2*p* core level spectrum evidence a larger contribution from the Ti-O(-N) compared to the Ti-N one for the high N $TiAlN_x$ layer than for the low and medium N cases. This will be commented later. We can also notice that the energy of the Ti-N contribution is not the same for the low/medium and high N $TiAlN_x$ stacks. It is similar to the stoichiometric TiN (455.3 eV) for the high N $TiAlN_x$ sample but

lower for the low and medium N cases. This is most probably the signature of an added metallic Ti-Ti contribution, which means some α-Ti contribution.

Conjugating all the above information, we will bring some insight about the electrical parameters measured for these TiAlN-based electrodes, which are gathered on figure IV-14. Significant modifications of the EWF and the EOT are observed depending on the N flow used to fabricate the electrodes.

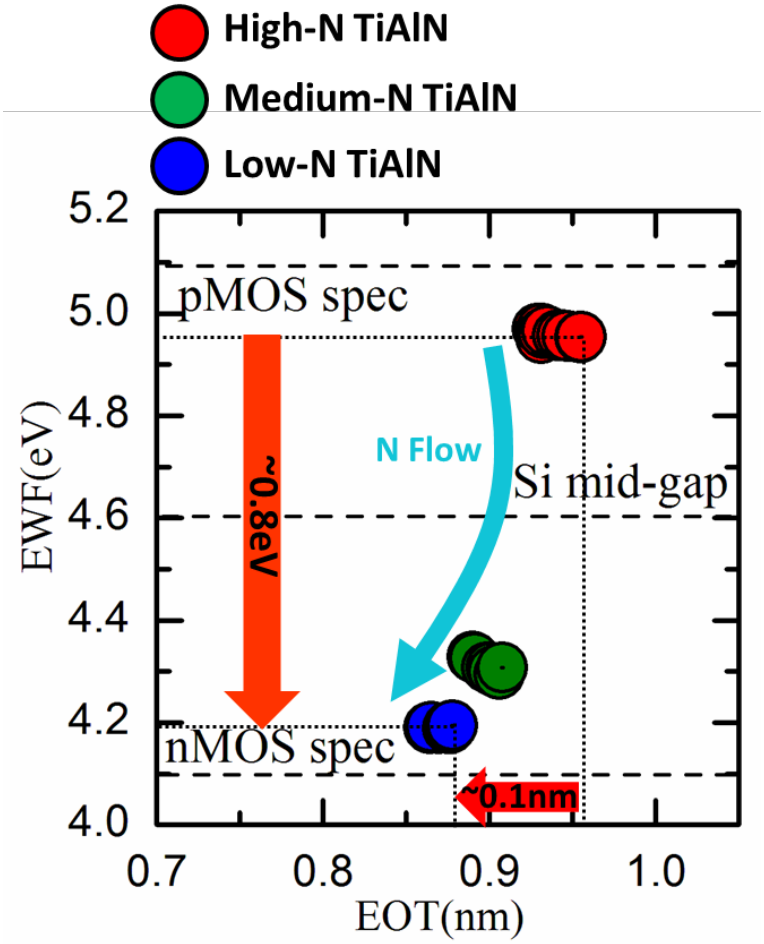

***Fig. IV-14**- EWF versus EOT on MOS capacitors for low, medium and high-N TiAlN electrodes.*

Decreasing the N flow, the EOT is scaled by 0.07 nm from 0.93nm to 0.86nm. Indeed, lowering the nitrogen flow results in the increase of titanium content most probably to a level where some α-Ti is formed as suggested by the binding energy of the Ti-N contribution in the Ti2*p* XPS core level spectrum at least for the low and medium N $TiAlN_x$ layers. α-Ti being a high oxygen scavenger, the increase of its content in $TiAlN_x$ by the use of a lower N-flow results in a higher amount of oxygen scavenged from the SiO_2-IL and thus in the observed EOT scaling. Indeed, the increase of α-Ti phase in $TiAlN_x$ reduces its visible XPS oxidation

thanks to the O unbounded with Ti in α-Ti phase. Therefore, the higher the amount of the α-Ti phase is (.i.e by lowering the N-flow), the lesser the oxidation in Ti *2p* core level spectrum is visible and the higher the scavenging of O from the SiO_2-IL occurs. Besides, notice that despite the Ti-rich composition of the low-N $TiAlN_x$, no aggressive scavenging of oxygen from the dielectrics is observed. This suggests that as stated in section IV-2, the alloying of titanium with aluminum in a single $TiAlN_{x<1}$ layer reduces the solubility of oxygen in the alloy, which results in a more stable electrode toward the dielectrics. Moreover, the EOT values of the TiAlN electrodes is a little higher than the one of the TiN/TiAl one, which can be attributed to the fact that N directly incorporated in the TiAlN electrode contributes to an additional limitation to the solubility of O in the Ti-rich metal.

Lowering the N flow, the EWF decreases by 0.8eV between the high N $TiAlN_{x>>1}$ (EWF=5.0eV) and the low-N $TiAlN_{x<1}$ (EWF=4.2eV). As stated previously for HfO_2/TiN/Ti and HfO_2/TiN/TiAl electrodes, the obtained low EWF for low-N $TiAlN_{x<1}$ is assigned to the substoichiometric composition (Ti/N>1) of $TiAlN_x$ which means some α-Ti contribution at the HfO_2/TiAlN interface.

In the case of medium-N $TiAlN_{x>1}$, the increase of nitrogen flow has low impact on the EWF variation compared to the low-N $TiAlN_{x<1}$. Only +0.1eV EWF increase (EWF=4.3eV) is observed despite the reverse situation about the N/Ti ratio, which is higher than one in this case. Indeed, like for the low-N $TiAlN_{x<1}$, from Ti2*p* XPS, some metallic α-Ti contribution has been deduced which explains the low EWF measured. Moreover, we also observed an Al-N predominant chemical environment instead of a Ti-N one for N. This can be explained by the fact that part of the N is probably dissolved in the α-Ti phase (Fig. III-8). This means that titanium is observed weakly bounded with nitrogen despite the high N/Ti STEM-EDX ratio. This result shows that Ti-rich behavior with a low level of Ti bounded with N may be kept in a large range of nitrogen concentration which enable the observed nMOS-adapted low EWF for medium-N $TiAlN_{x>1}$ despite its overstoichiometric nature.

Finally, high N $TiAlN_{x>>1}$ results in a pMOS adapted work function with EWF=5.0eV. This value may result from the addition of two contributions. First, compared to the medium N flow, the much higher content of N in the high N TiAlNx is well visible on the STEM-EDX profiles. From XPS, N is mainly bounded to Ti in this case with a marked stoichiometric TiN character. The corresponding EWF, 4.85 eV, is however not enough high to explain the measured 5eV value. A second contribution has to be taken into account. Hinkle *et al.* showed

that performing controlled oxidation of HfO_2/TiN electrodes leads to an increase of the gate EWF. They assigned this behavior to the diffusion of nitrogen at the HK/MG interface resulting in the formation of interfacial Hf-N dipole and a significant increase of the gate EWF of about 550meV [Hinkle10]. We suppose that in the case of the high N $TiAlN_{x>>1}$, the significant nitrogen diffusion to the HfO_2/$TiAlN_{x>>1}$ interface which stems from STEM-EDX and XPS discussions induces interfacial Hf-N dipole formation. As calculated in the work of Hinkle, if N atoms replace all O atoms at the TiN/HfO_2 interface, the EWF increases by 450 meV and if only 1/3 of O atoms are replaced, the EWF increases by 180 meV. Therefore, it is reasonable to think that the +150meV work function increase necessary to justify the measured EWF of 5.0eV can be correlated to the formation of Hf-N dipoles at the HfO_2/high N TiAlN interface.

IV-4. Conclusion

In conclusion, with TiAl deposition on reference HfO_2/TiN, we obtain an nMOS adapted EWF of 4.24 eV measured on HfO_2/TiN 2nm/TiAl 2.5nm. The mechanism of EWF shift regarding HfO_2/TiN reference is assigned to the formation of a substoichiometric base-TiN (Ti rich). This electrode exhibits a very low EOT value, 0.83nm, which reflects significant oxygen scavenging from the SiO_2-IL. However, no aggressive scavenging is observed here despite the Ti-rich composition of the TiAl alloy. This is assigned to Al alloying with Ti which reduces oxygen solubility in titanium i.e. reduction of the α-Ti phase domain avoiding the total reduction of oxygen from the dielectrics.

In addition, we demonstrated that the modulation of the nitrogen flow during $TiAlN_x$ single layer deposition on HfO_2 results in both n and pMOS adapted EWF, which enables the use of $TiAlN_x$ in dual metal gate CMOS integration. We obtained highly stable electrodes with a controlled sub-1nm EOT scaling required for sub-20nm CMOS RMG integration.
In the next section, we will try to evaluate the thermal stability of the previously studied electrode at temperatures up to 700°C. This is achieved in order to give insight into the possibility to integrate these metals using a higher thermal budget gate first approach or 3D integration where high level transistors have to sustain different thermal budgets at temperatures higher than 400°C.

Chapter V

Thermal stability and spiking

V-1. Introduction

In this chapter, we evaluate the thermal stability of all previously studied gate electrodes in order to give an insight on their possible integration using gate first approach or in 3D integration where second and third level transistors have to sustain higher thermal budget than the initial 400°C, 30min [Batude11]. This initial state will be named in the following, as-deposited.

Therefore, HfO_2/TiN/Al/TiN, HfO_2/TiN/TiAl/TiN and HfO_2/$TiAlN_x$/TiN stacks were subjected to 500°C and 700°C anneals during 1min under vacuum (~10^{-5} Pa) using a Rapid Thermal Processing (RTP) equipment. Same gate stacks on patterned and blanket wafers were processed simultaneously which ensures comparable electrical and analytical results. The Ti-based electrode has not been considered because it is too reactive and unstable since 400°C.

V-2. TiN/Al bi-layer

HRTEM images of HfO_2/TiN/Al-based stack annealed at 500°C show the occurrence of dark areas in the silicon substrate just below the Si/oxide interface (Fig. V-1). In depth observation of medium HRTEM micrographs as the one shown on figure V-2 reveals no interfacial layer between the HK and the Si substrate. The SiO_2 IL is completely reduced by the metal gate after the annealing.

The dark areas within the Si substrate contain silicon, aluminum and titanium as seen from the STEM-EDX analysis (Fig. V-3). Lee *et al.* have already observed the same dark areas in the Si substrate of Si/TiN/Al stacks without a HfO_2 dielectric, annealed at 550°C [Lee99]. Their study reveals that these dark areas match Al_3Ti spikes dissolving some Si (20%), which is in agreement with our qualitative analysis. Lee *et al*. concluded that Al piles up at the bottom of TiN because Al has no solubility in Si (see Fig. V-4). Then an interfacial reaction occurs between Al and TiN, which produces Al_3Ti as a spike and an AlN layer between the spike and TiN. Because Al_3Ti can dissolve a large amount of Si (about 20% [Nishimura92]) and Si can diffuse in the substrate as defects or through TiN and dissolve into Al, it grows in the substrate.

In our case, an added HfO_2 layer is present between the Si substrate and the TiN layer. Despite this physical and chemical barrier, Al_3Ti (Si) forms in the substrate. Therefore, we

should conclude that Al, Ti and N diffuse through the HfO_2 layer and finally form the Al_3Ti spike at the contact with the Si substrate.

In conclusion, due to spike formations, the substrate integrity of $Si/SiO_2/HfO_2/TiN/Al$ stacks annealed at 500°C is not preserved. A possible solution to improve the stack chemical stability is to moderate the Al diffusion due to annealing by either increasing in a reasonable way the TiN thickness or by depositing an Al diffusion barrier to mediate the Al diffusion through the base-TiN [Nichau13].

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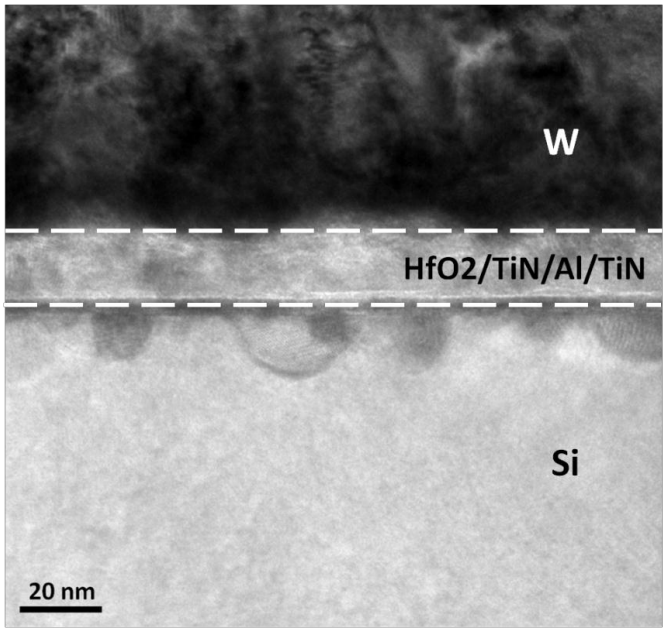


Fig. V-1*- Low magnification TEM micrograph of a HfO_2/TiN/Al/TiN/Wstack after annealing at 500°C*

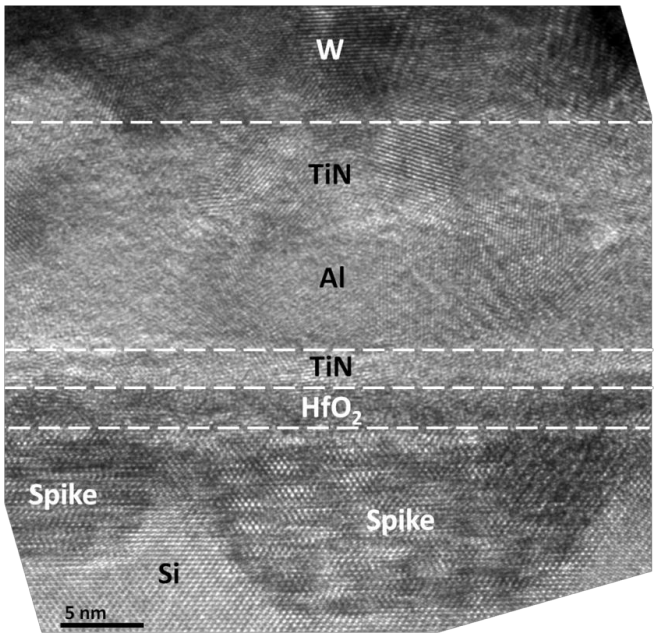


***Fig. V-2**- Medium magnification TEM micrograph of a HfO_2/TiN/Al/TiN/Wstack after annealing at 500°C*

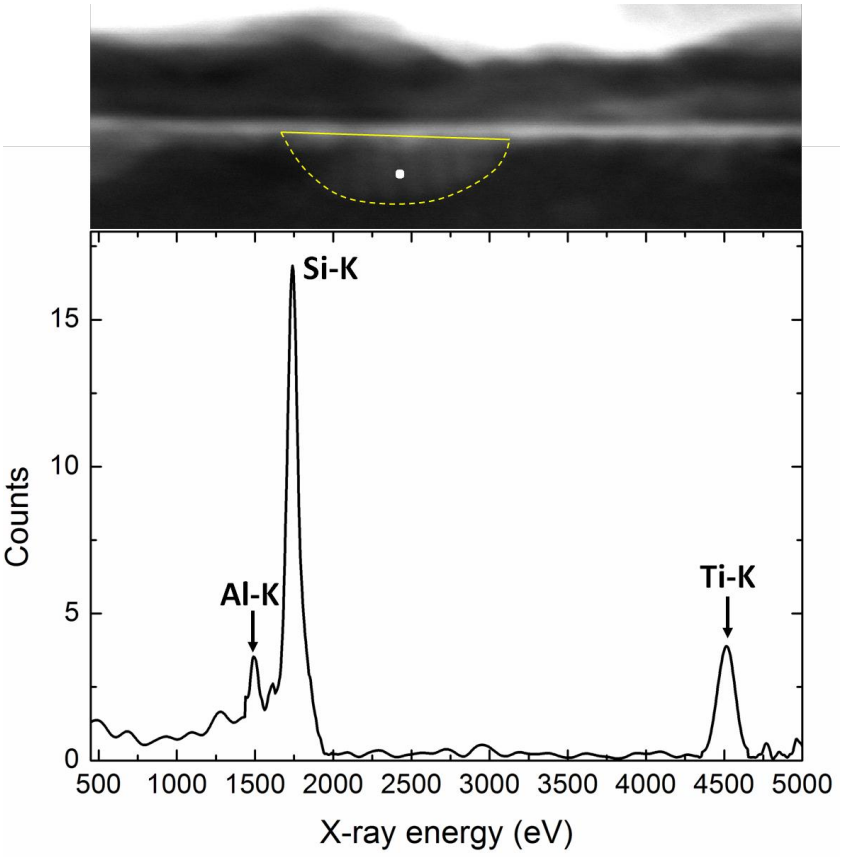


***Fig. V-3**- STEM-EDX spectrum of a spike and, above, STEM-HAADF image with the localization of the analyzed area.*

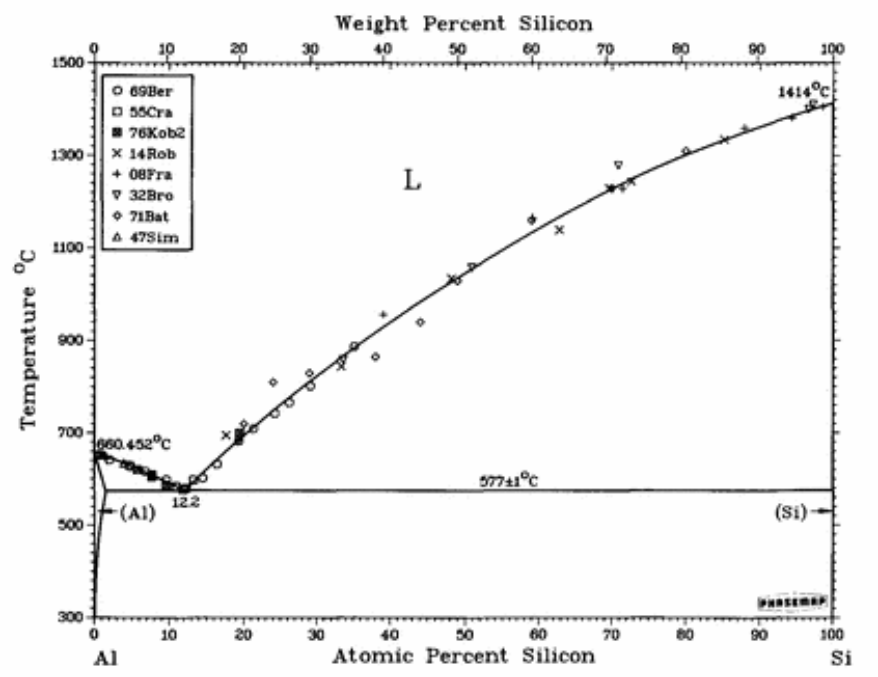


Fig. V-4*- Al-Si binary phase diagram. From* [Murray84].

V-3. TiN/TiAl bi-layer

Contrary to the Al-based electrode case, the annealing of $Si/SiO_2/HfO_2/TiN/TiAl$ at 500°C reveals that the Si substrate is not affected by spike formation. However, we notice the complete consumption of the SiO_2 IL after annealing similarly to the Al case (see Fig. V-5 and Fig. V-6). This suggests that alloying Ti with Al avoids the formation of spikes in the silicon substrate at temperatures up to 500°C but suppress the chemical stability of TiAl regarding O with an aggressive scavenging of oxygen from SiO_2 IL. Thus the stabilization toward O gained by alloying Ti with Al as discussed in chapter IV is limited thermally to a temperature between $400°C \leq T < 500°C$. This is probably due to a thermal activation of the O diffusion and the subsequent dissolution in the Ti-rich TiAl layer.

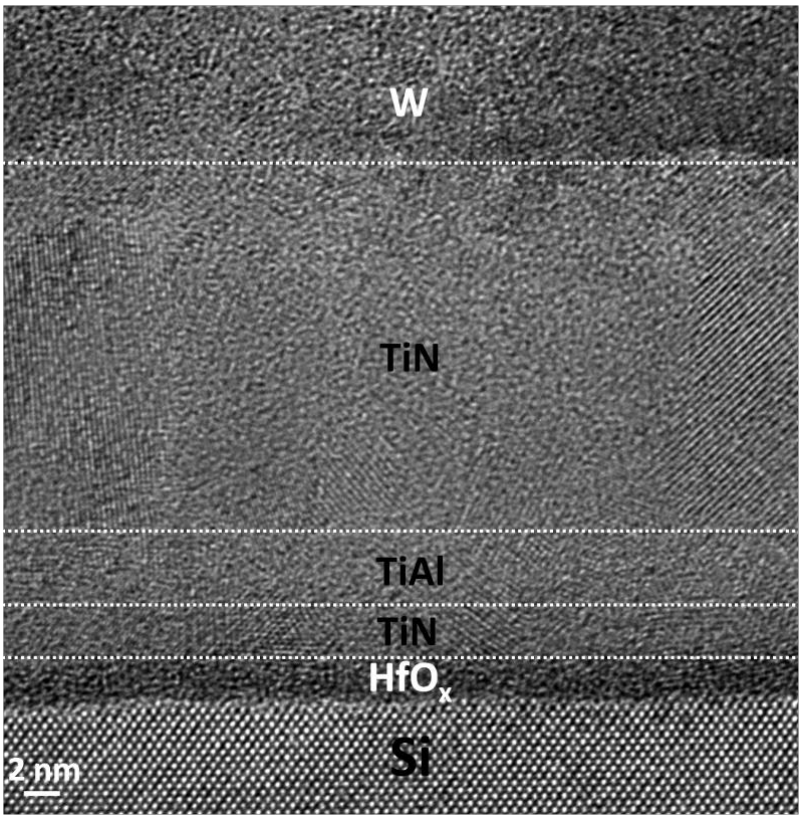


***Fig. V-5**- HRTEM micrograph of a HfO_2/TiN/TiAl stack after annealing at 500°C*

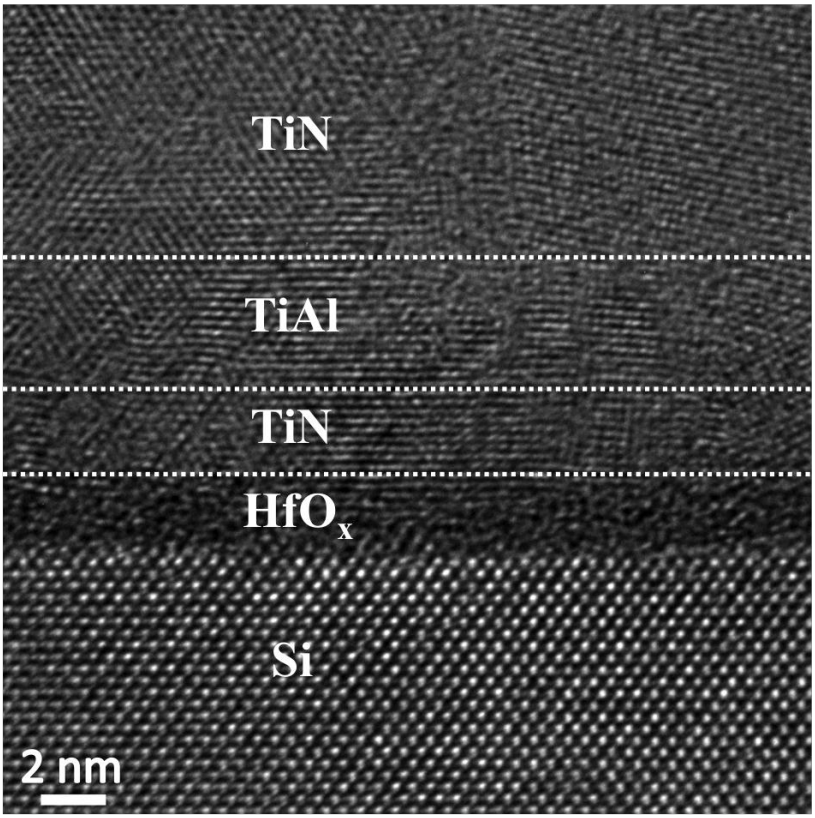


***Fig. V-6**- Higher magnified HRTEM micrograph of a HfO_2/TiN/TiAl stack after annealing at 500°C*

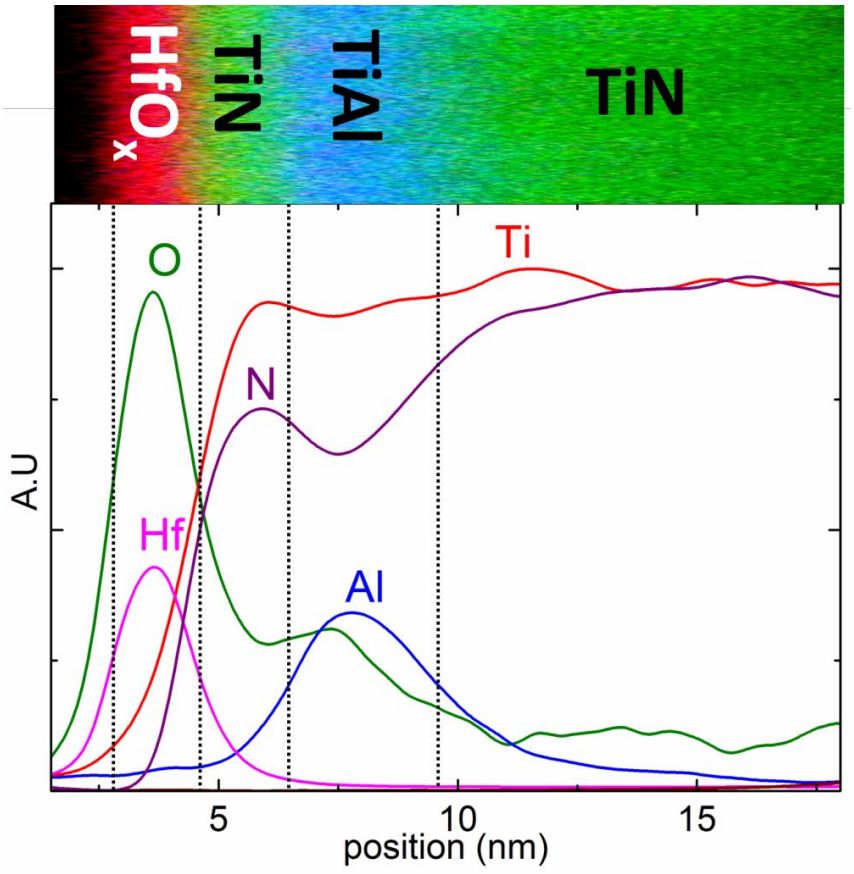


Fig. V-7*- STEM-EDX map of a Si/SiO_2/HfO_2/TiAl/TiN/W stack and Hf, O, N, Ti and Al profiles across the stack with localization of the different sublayers after annealing at 500°C*

he characteristics of the STEM-EDX O profile shown on figure V-7 confirm the TiAl aggressive scavenging from the SiO_2 IL. It is aligned with the Hf profile and its intensity increases significantly in the TiAl layer revealing high amount of oxygen absorbed from the SiO_2 IL dielectric.

Annealing up to 500°C preserves a similar substoichiometry of the base-TiN compared to the one observed for the as-deposited stack, in particular at the HfO_2/TiN interface. Al profile remains also unchanged with no aluminum diffusion through the base-TiN, in particular with no aluminum detected at the HfO_2/TiN interface. TiN barrier against Al diffusion as observed in chapters III and IV remains efficient even after 500°C annealing.

The previous observations reveal that the diffusion of Al through HfO_2/TiN and its segregation at Si/HfO_2 interface is a key parameter for the spiking in the silicon substrate. In the case of HfO_2/TiN/TiAl, the poor Al nature of TiAl ([Al]~20%) together with the barrier effect of base-TiN against the diffusion of aluminum results in no variation of the aluminum

amount diffusion through base-TiN after annealing which avoids the formation of Al spikes in the silicon substrate.

We increased the Al amount in TiAl to about 50% in order to improve the thermal stability concerning the O scavenging. However, the barrier efficiency is lost; spikes appear (see Fig. V-8(a) and (b)). Al can diffuse through the HfO_2/base-TiN, react with Ti and reach Si substrate where Al_3Ti spikes in Si substrate are present.

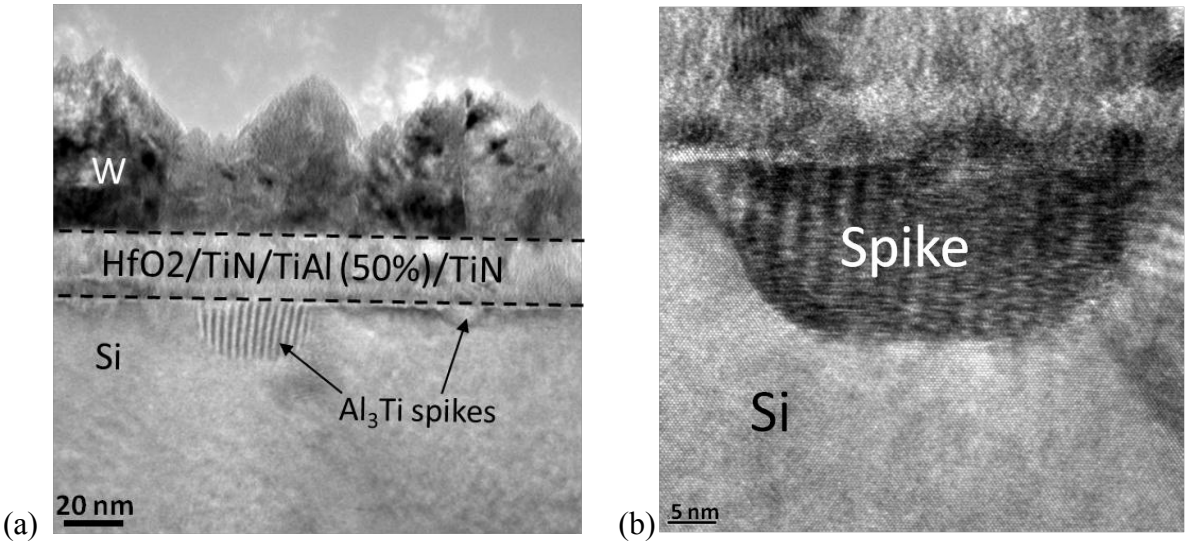


***Fig. V-8**- (a) low magnification and (b) medium magnification TEM micrographs of a HfO_2/TiN/TiAl (Al~50%) stack after annealing at 500°C*

To assess the upper limit of the thermal stability for HfO_2/TiN/TiAl ([Al]~20%) stack, 700°C anneal has also been achieved. As shown on figure V-9, the Si substrate is affected by the formation of spikes, which suggests the failure of base-TiN barrier against Al diffusion.

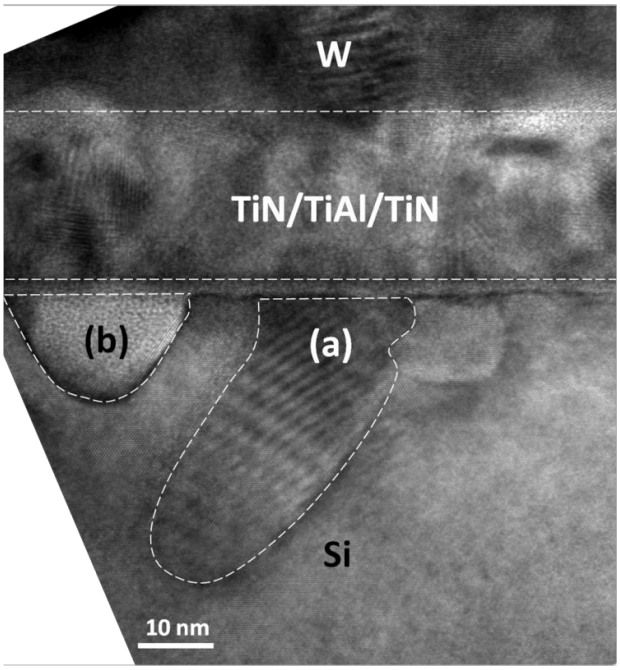


Fig. V-9- *Low magnification TEM micrograph of a Si/SiO_2/HfO_2/TiN/TiAl/TiN/W stack annealed at 700°C with spikes at (a) an early stage and (b) an advanced stage*

As stated in the chapters III and IV, the TiN barrier against Al diffusion mechanism operates through the formation of AlN during Al diffusion and simultaneous N scavenging by the TiAl layer. Hence, the lower the nitrogen amount in base-TiN is, the higher is the diffusion of aluminum. We suppose that annealing at 700°C activates thermally nitrogen diffusion thus nitrogen scavenging by TiAl resulting in a more substoichiometric $TiN_{x<<1}$ which favors the failure of the base-TiN barrier against Al diffusion. We suppose that the HfO_2 layer remains stable and do not react with Al, Ti and Al_3Ti diffusing through it.

To conclude, we assume that a higher Al amount in TiAl alloy may induce a reduced O solubility in Ti. Aggressive oxygen scavenging will then be avoided extending the thermal stability of HfO_2/TiN/TiAl electrode for above 500°C. However, the counterpart could be the diffusion of Al through HfO_2 down to the Si substrate and the formation of highly defective silicon substrate. Hence, we observe an unsteady situation where one should find the right amounts of Al in Ti, which will result in the good compromise between avoiding Si/Al intermix and a controlled SiO_2 IL scavenging. From the present investigations, this value if it works should be between 20 and 50%.

V-4. $TiAlN_x$ single layers

We concentrate here on the case of the high-N TiAlN representative of a pMOS electrode, complementary to the TiAl (or the low and medium N TiAlN electrodes). Electrical investigations showed no short circuit for the 500 and 700°C annealed stacks, which supposes that no spikes or drastic O scavenging occur in these cases.

The electrical parameters modifications after 500 and 700°C anneals are shown in figure V-10 and summarized in Table V-1(EWF, EOT). Compared to the as-deposited electrode, annealed ones correspond to a dramatic increase of EOT together with a decrease of the EWF.

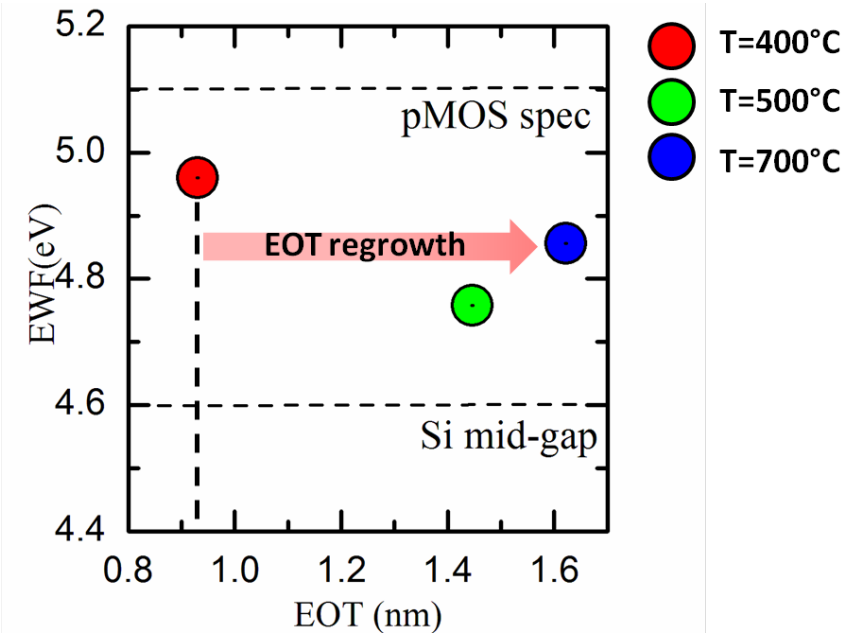
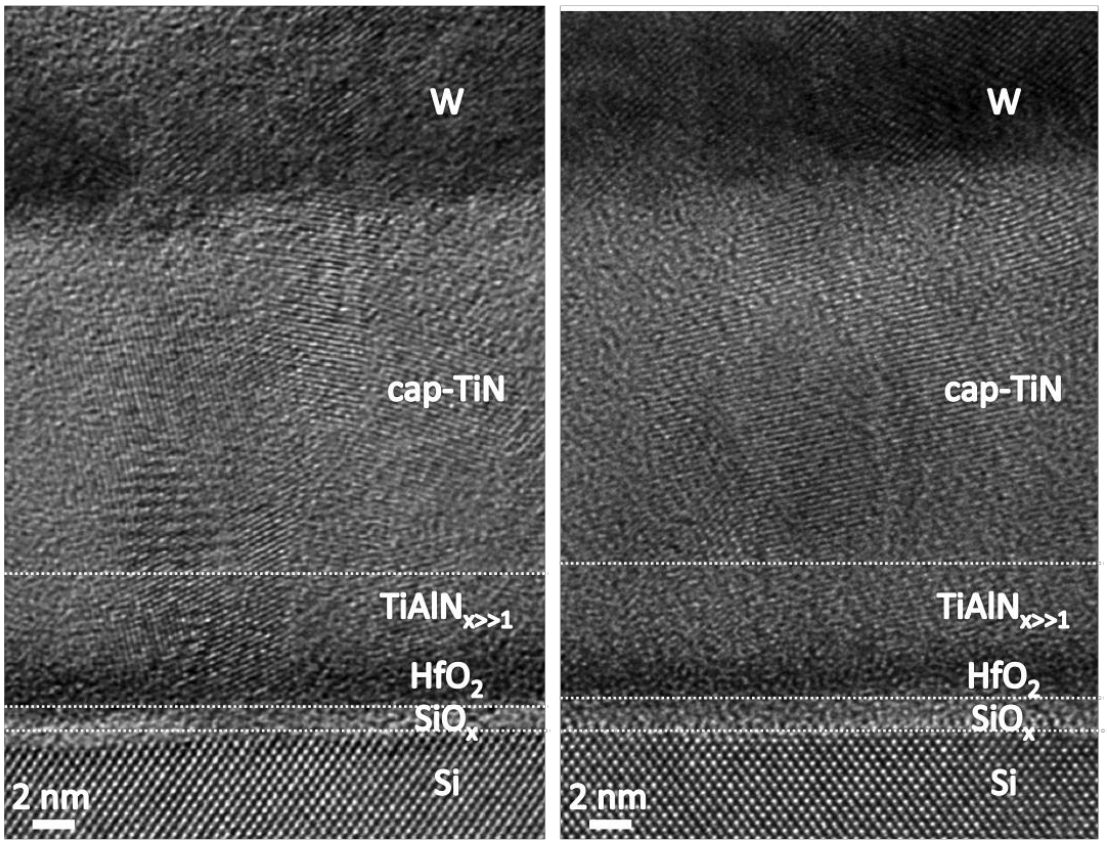


***Fig. V-10**- EWF versus EOT recorded on a HfO_2/High N TiAlN as-deposited and after annealing at 500°C and 700°C*

Annealing temperature	EWF (eV)	EOT (nm)
$HfO_2/TiAlN_{x>>1}$ T=400°C (as dep)	5.0eV	0.95
$HfO_2/TiAlN_{x>>1}$ T=500°C	4.76eV	1.44
$HfO_2/TiAlN_{x>>1}$ T=700°C	4.86eV	1.62

***Table V-1**- EWF and EOT values obtained with HfO_2/high N $TiAlN_{x>>1}$ as-deposited and after annealing at 500°C and 700°C.*

The loss of EOT scaling is confirmed by the HRTEM images (Fig.V-11) where the main difference between the as-deposited and the annealed stacks is the thicker SiO_2 IL. These images confirm that the annealing did not impact the quality of the substrate, which suggests a higher thermal stability against spike formation.



(a) (b)

***Fig. V-11**- HRTEM micrographs achieved on a Si/SiO_2/HfO_2/$TiAlN_x$/TiN/W stack with a high-N content (a) as-deposited and (b) after annealing at 500°C*

The STEM-EDX O and Hf profiles of figure V-12 also support the loss of EOT scaling. A slight evolution of Al profile for the 500°C annealed sample compared to the as-deposited one suggests a limited impact of the annealing on Al diffusion, thus the maintained thermal stability with regard to the spike formation. Similarly, the N profile evidences a lesser diffusion in the HfO_2 layer probably leading to a minor influence of the eventual HfN bonds formed on the EWF. Finally, N and Ti intensity profiles are closer after 500°C annealing which suggests a slight decrease of the N/Ti ratio in the $TiAlN_x$ layer. We suppose that the nitrogen amount lowering in $TiAlN_x$ results from its diffusion in soichiometric cap-TiN until reach the thermodynamic equilibrium resulting on both overtoichiometric $TiAlN_{x>1}$ and cap-$TiN_{x>1}$.

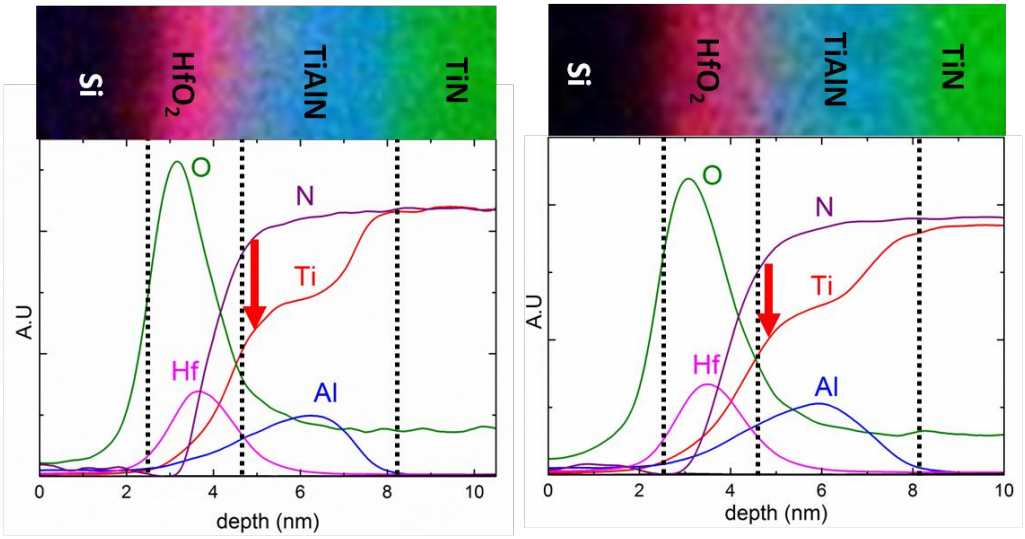


Fig. V-12*- STEM-EDX map of a Si/SiO_2/HfO_2/TiAlN high N/TiN/W stack and Hf, O, N, Ti and Al profiles across the stack with localization of the different sublayers (left) as-deposited and (right) annealed at 500°C*

The XPS Al*2p* core level spectrum (see Fig.V-13) shows that aluminum is completely bounded with nitrogen with no free metallic aluminum in the $TiAlN_{x>>1}$. This has different implications. First, this corroborates that the diffusion of Al is not possible even after 500 or 700°C annealing which avoids the formation of spikes in the Si substrate as confirmed by the HRTEM images. Second, because there is no metallic aluminum to play the role of oxygen diffusion barrier, annealing induces the diffusion of air break oxygen present in the bulk Cap-TiN through $TiAlN_{x>>1}$. Therefore, O reaches the silicon substrate and reacts with it inducing the increase of SiO_2 thickness degrading the EOT.

Finally, looking at the Ti-Al-N phase diagram (Fig. V-14) with in mind the N-rich character of the $TiAlN_{x>>1}$ layer and the presence of Al-N bonds in this layer, we corroborate that the position representative of the $TiAlN_{x>>1}$ layer is on the AlN-TiN equilibrium line nearer to the TiN boundary. The TiN bonds contribute there to the establishment of a TiN-like pMOS EWF as measured electrically.

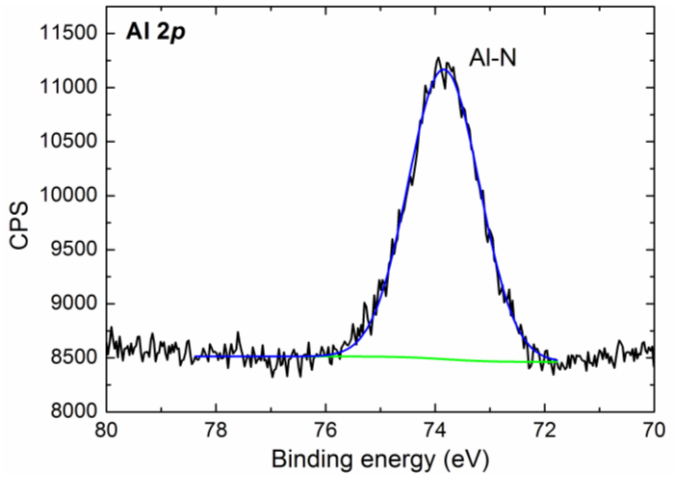


Fig. V-13*- Backside XPS of Al2p core level spectrum obtained from a HfO_2/High N $TiAlN_x$ stack annealed at 500°C*

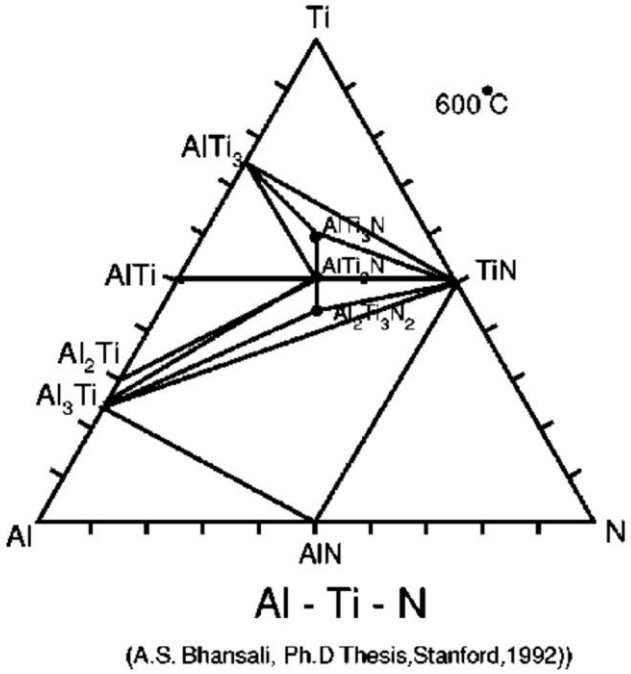


Fig. V-14*- Al-Ti-N phase diagram. From* [Lee99]

We propose some strategies to try to stabilize further in temperature the TiAlNx electrode.

We assume that the replacement of the cap-TiN by an efficient barrier to oxygen diffusion may induces lower air break oxygen amount which will extend the thermal stability of $TiAlN_{x>>1}$ electrode. In addition, we think that reducing TiN-cap thickness will result in less nitrogen interaction with TiAlN layer, which may avoid the EWF decrease after annealing.

V-5. Conclusion

In conclusion, the annealing of TiN/Al, TiN/TiAl reveals a loss of thermal stability at T>400°C with:

- the substrate degradation induced by the formation of spikes (Al_3Ti) (low-N $TiAlN_{x<1}$, TiN/Al and TiN/TiAl (Al~50%) at 500°C and TiN/TiAl ([Al]~20% at 700°C);
- the complete oxygen scavenging from the SiO_2 IL (TiN/TiAl ([Al]~20%));
- the significant degradation of the EOT (high-N $TiAlN_{x>>1}$ at 500°C and 700°C)

Strategies have been proposed to try to shift to higher temperatures the thermal stability of each stack and make them adapted for higher thermal budget integration:

- for Al/TiN : deposition of thicker base-TiN or diffusion barrier to Al diffusion;
- for TiAl: optimization of the Al amount in TiAl (20%<Al<50%) to increase stability against O scavenging while keeping low Al diffusion to preserve Si from Al_3Ti spiking;
- for $TiAlN_x$: find an efficient cap-barrier against oxygen diffusion to preserve the low EOT after annealing.

In the next chapter, we will present the investigations conducted on more thermally stable Tantalum and Nickel based innovative electrodes.

Chapter VI

Innovative gate electrodes

VI-1. Introduction

In the previous chapters, we showed that as-deposited (400°C) HfO_2/TiN/TiAl (Al~20%) and HfO_2/$TiAlN_{x>>1}$ were well adapted for nMOS and pMOS EWF respectively. However, these performances are compromised after a 500°C annealing treatment, i.e. degradation of the EOT for TiAl and of the EWT for TiAlN.

This chapter focused on the search for more thermally stable electrode materials for moderate thermal budget corresponding to one minute annealing at 500°C and/or 600°C. The aim is to find adapted materials for gate first approach or 3D innovative integration [Batude11].

For the nMOS side, as presented in chapter I, the Ellingham diagram for MO_x formation reveals the high stability of Ta toward oxygen compared to Ti and Al with a $\Delta G_{Ta2O5} > \Delta G_{SiO2}$ for $0 \leq T \leq 1050$°C. This reveals that Ta does not scavenge oxygen from the SiO_2 IL, which is not common for a low WF nMOS-adapted material (Ta WF in vacuum=4.25eV [Michaelson77]).

For the pMOS side, we also pointed out in chapter I the high chemical stability of noble and semi-noble metals. We study here the particular case of nickel. Ni presents several advantages compared to noble metals such as Ru, Pd or Pt [Cabral04]:

- first, it is well known by semi-conductor industry as already used for S/D and poly-Si silicide formation;
- it is adapted for wet and etch conventional process;
- its cost is clearly lower than noble metals and it presents the same high chemical stability toward oxygen.

In the first part of this chapter, we propose to study the case of the low WF Ta when deposited on HfO_2/TaN to have a similar but alternative nMOS gate electrode to HfO_2/TiN/Al or TiAl. The thermal stability of the gate electrode is evaluated for temperatures up to 600°C. In particular, the chemical stability of the TaN/Ta electrode regarding oxygen for $400°C \leq T \leq 600°C$ will be compared with previously studied TiN/TiAl and TiN/Al electrodes. Moreover, attention will be paid on the study of the behavior of Ta regarding N and the corresponding effect on the EWF.

In a second part, we will consider the opposite situation to what was proposed until now, where an nMOS metal is deposited first. We will consider the alloying of the high WF nickel with the low WF Ta and Ti metals in Ta/Ni and Ni/Ti electrodes, respectively. The impact of Ta/Ni and Ni/Ti alloying on the electrodes EWF and EOT will be investigated at 500°C.

VI-2. Ta deposition on HfO_2/TaN: highly stable nitrogen scavenger

The $Si/SiO_2/HfO_2$/TaN 2nm/Ta 10nm/TaN 5nm/TiN 5nm/W stack is considered here. HRTEM micrographs of this stack in the as deposited state (400°C, 30 min) and after adding annealing at 500°C and 600°C for 1 min are shown on figure VI-1.

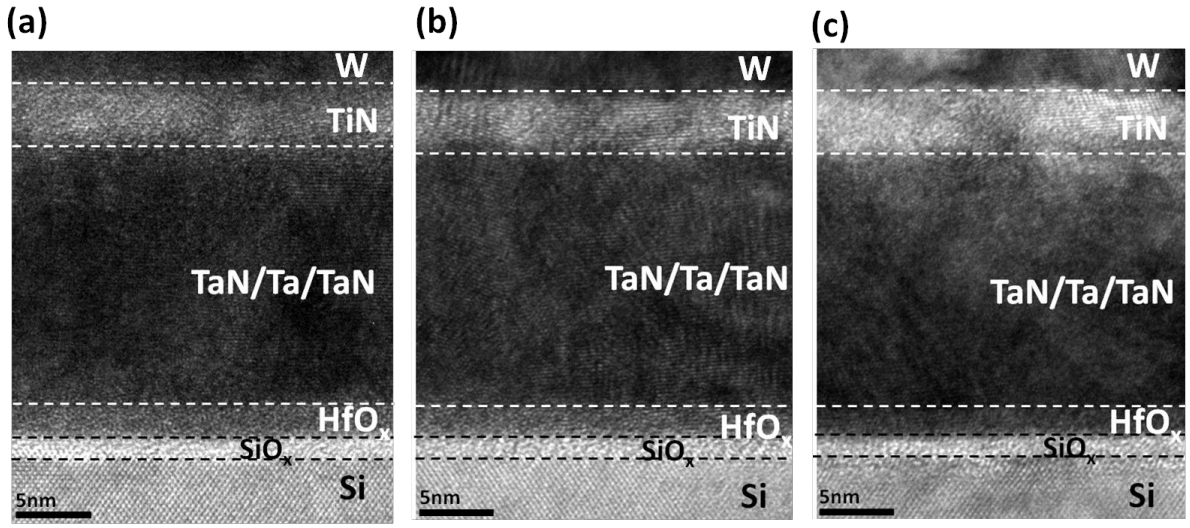


***Fig.VI-1**- HRTEM images of a HfO_2/TaN 2nm/Ta10nm/TaN5nm/TiN5nm/W electrode (a) before and after (b) 500°C and (c) 600°C annealing*

The high thermal and chemical stability of this gate electrode after additional 500°C or 600°C annealing is proved by only slight variations of the SiO_2 IL thickness. Contrary to the case of the light elements based electrodes, i.e. TiAlN, the heavier elements based layers, i.e. TaN/Ta/TaN, appear dark. Above HfO_2, all the layers are polycrystalline and their thicknesses fit the target values.

Electrical C(V) measurements were performed on a reference TaN layer deposited on HfO_2 in addition to the HfO_2/TaN/Ta electrode before and after 500°C and 600°C annealing (Fig. VI-2). The stoichiometric nitride leads to a Si-mid gap EWF of 4.6eV. Compared to the HfO_2/TaN reference, the HfO_2/TaN/Ta electrode exhibits a lowered EWF by 0.30eV, i.e. 4.3eV before and after 500°C annealing but the 600°C annealed stack returns to near the midgap position with an EWF of 4.48 eV. Besides, electrical analysis attests the high stability of tantalum regarding oxygen with a low EOT of 0.9nm measured before and after 500°C

annealing samples whereas a slight increase of the EOT is recorded for the 600°C annealed electrode with an EOT of 0.96nm.

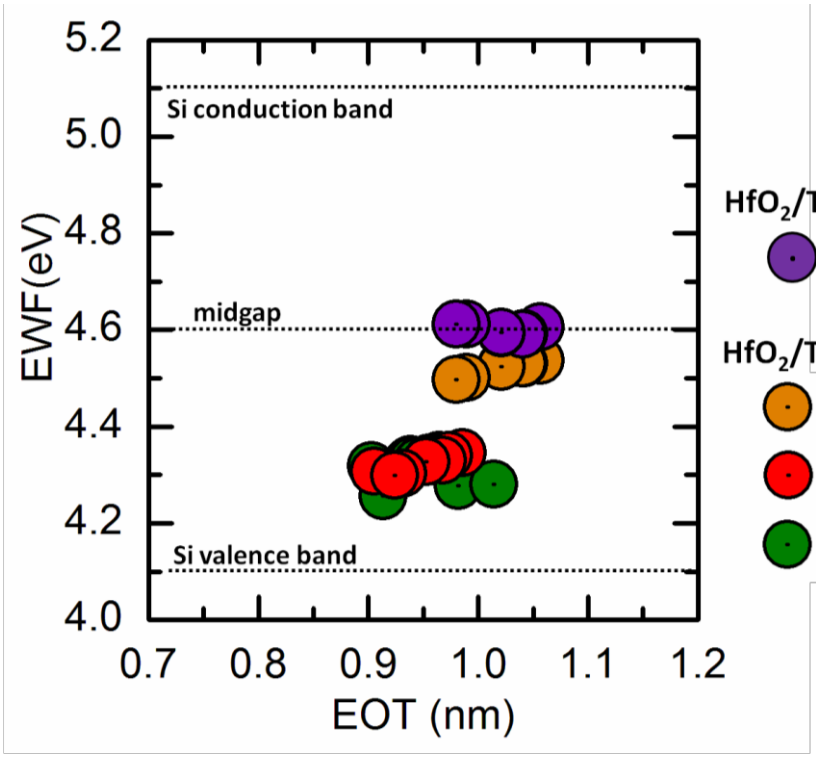


***Fig.VI-2**- EWF versus EOT for an as depositedHfO_2/TaN capacitor and a HfO_2/TaN/Ta capacitor before and after 500°C and 600°C annealing.*

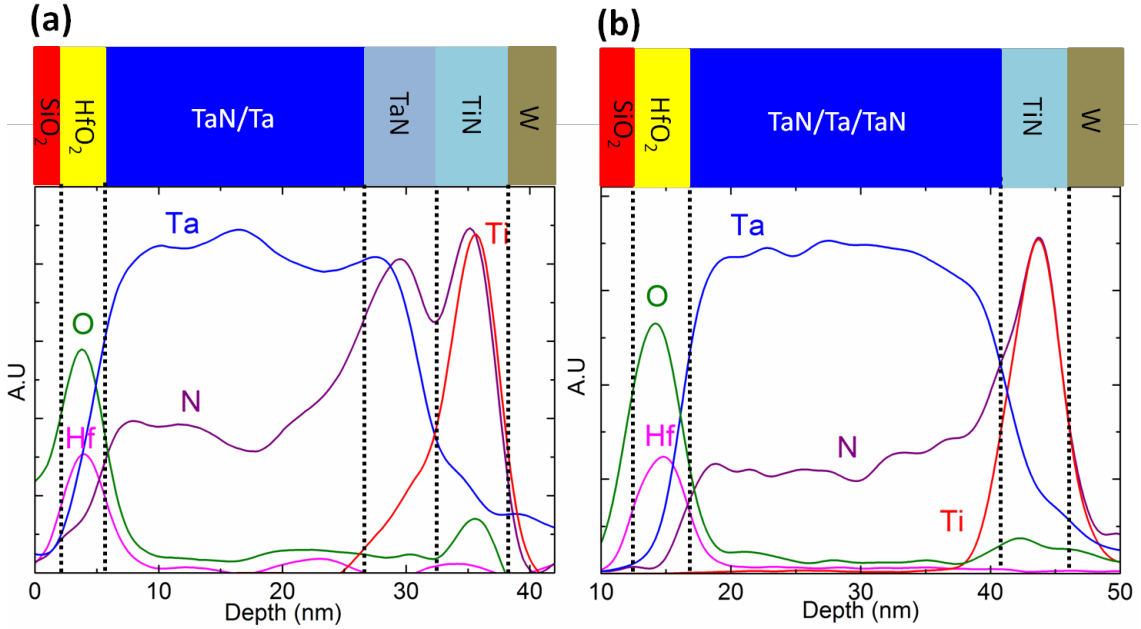


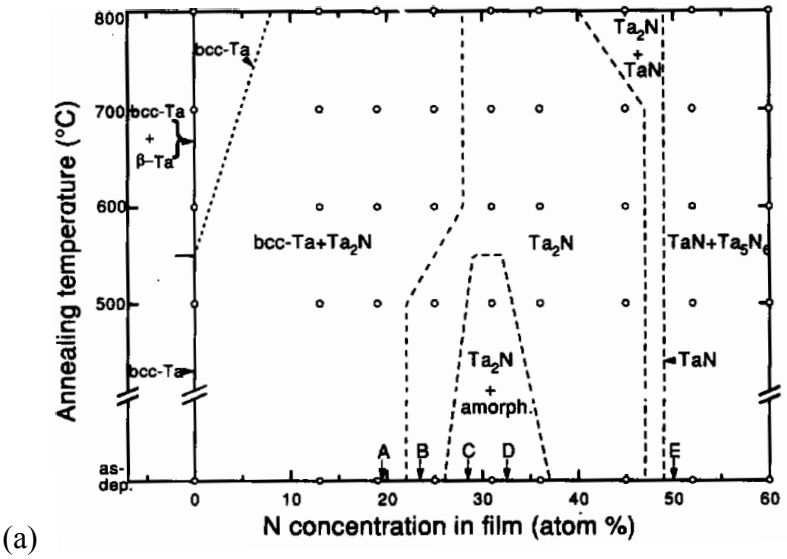
***Fig. VI-3**- STEM-EELS profiles of Hf, O, N, Ta and Ti for HfO_2/TaN 2nm/Ta 10nm gate electrode (a) before and (b) after 500°C annealing. Vertical dashed lines propose the localization of the interfaces between the different layers, which are schematically represented on top.*

Simultaneous STEM-EELS and STEM-EDX line profiles have been acquired for these stacks. Profiles of the light N and O elements are extracted from the STEM-EELS spectra whereas the ones of the heavy Ta, Hf and Ti elements are extracted from the STEM-EDX spectra. The aligned and very slightly misaligned maxima of the O and Hf profiles before and after 500°C annealing respectively indicate a thin SiO_2 IL in agreement with the low measured EOT for both capacitors (Fig. VI-3). We notice that despite the thick 10 nm Ta deposited on the HfO_2/base-TaN, no aggressive scavenging from SiO_2 IL is reported here in opposition to what was observed for the HfO_2/TiN 2nm/Ti 8nm stack (short circuit). This result confirms that Ta is highly stable regarding oxygen. This stability is mainly due to the positive Gibbs free energy change for the $\frac{4}{5}$ Ta + SiO_2 → Si + $\frac{2}{5}$ Ta_2O_5 reaction as can be deduced from the Ellingham diagram of chapter I (Fig.I-9). There is no driving force to decompose the SiO_2 IL.

Besides, the O profile increase in the cap-TiN layer of the stack before 500°C annealing reflects a high oxidation level due to the process air break before the metal plug deposition. However, despite this air break operated between the cap-TaN / cap-TiN and the cap-TiN/W, a low oxygen amount is measured in the cap-TaN, which indicates its high ability to withstand oxidation. Even after the 500°C annealing step, the very tiny increase of the SiO_2 IL testimony the high efficiency of TaN to act as a barrier against atmospheric oxygen diffusion during the first process air break (cap-TaN /cap-TiN). It indicates that this TaN barrier also withstands the diffusion of the oxygen species dissolved as a solid solution in TiN during the second air break (TiN cap/W) [Ha07]. However, for the 600°C annealed sample, we observe a 0.06nm increase of the EOT, which may indicate the beginning of TaN barrier failure against air break oxygen diffusion.

N and Ta profiles of the stack before 500°C annealing reveal a noticeable modification of the stoichiometric base-TaN toward substoichiometry with N/Ta well below 1 at the HfO_2/TaN interface and within the TaN/Ta layers. Note the N and Ta profile intensities in the cap-TaN layer, which mainly reflect the N/Ta (x) initial 1/1 stoichiometry. Consequently, Ta deposition on base-TaN induces nitrogen scavenging from the base-TaN resulting in substoichiometric $TaN_{x<1}$. The situation is similar after 500°C annealing with a lower N/Ta ratio in the TaN/Ta layers even it is less modified at the HfO_2/base-TaN interface.

If we look at the tantalum-nitrogen binary phase diagram shown on Figure VI-4, we see that, in contrast with titanium, the solubility of nitrogen in tantalum is zero or very close to zero at 500°C and even 600°C [Sun93]. Moreover, based on the low level of N measured on the STEM-EELS profiles (N/Ti near 0.5), we can predict from this diagram that before and even after annealing, N is incorporated in the TaN/Ta layers forming either the Ta_2N phase or the Ta_2N phase in equilibrium with Ta. We measured the HfO_2/Ta EWF (see § VI-3, Fig.VI-9) at 4.4 eV and we know from a recent work that HfO_2/TaN_x has a lower EWF (4.3 eV in [Gassilloud14]. Therefore, the 4.3eV EWF measured for both stacks is consistent with such electrodes with nMOS character. Note that the mechanism responsible for the EWF shift is similar to the one observed for the HfO_2/TiN/Ti and HfO_2/TiN/TiAl stacks studied in chapter III and IV respectively.



(a) (b)

***Fig.VI-4**- Ta-N binary phase diagram from (a) [Sun93]*

We conclude from this study that nitrogen redistribution between TaN and Ta is the first order mechanism that contributes to the lowering of the EWF for HfO_2/TaN/Ta/TaN stack similarly to what happens in the HfO_2/TiN/Ti (TiAl)/TiN electrodes. High thermal stability of Ta toward the SiO_2 IL is also demonstrated in addition to the high efficiency of TaN to act as a barrier against oxygen coming from process air break. But the co-integration of n and p metals in CMOS devices using HfO_2/TaN/Ta solutions could be difficult. Indeed, despite the fact that TaN/Ta shows the right work function for n side, HfO_2/TaN is rather Si-midgap and subsequently far away from pMOS specification.

In the next section, we will present why an alternative metal couple based on Ta and Ni on HfO_2 can be adapted to possible CMOS co-integration.

VI-3. Ta and Ni alloying: two stable metals for pMOS integration

Now, we investigate on the alloying of Ta and Ni, two chemically stable metals regarding oxygen which exhibit different vacuum WF with WF_{Ta}=4.25eV and WF_{Ni}=5.05eV [Michaelson77]. The strategy here is to start with an nMOS reference electrode with Ta deposition on HfO_2 and to add on the Ta a subsequent Ni layer with the aim to obtain a pMOS adapted gate electrode. Hence, Si/SiO_2/HfO_2 2nm/Ta 2nm/(Ni 10nm)/TiN 5nm/W stacks are considered here.

On the HRTEM images (Fig. VI-6), two main differences appear before and after the 500°C annealing samples. First, we observe the presence of a thick SiO_2 IL oxide layer of about 2nm before annealing and even thicker after 500°C annealing. This is simply due to the fact that the native oxide has not been removed. The chemical oxide formation step has been skipped on these blanket samples, which is not the case for the capacitors used for the electrical measurements.

Second, on top of the amorphous HfO_2 oxide a thin dark layer of about 1nm is evidenced before the 500°C annealing which should correspond to the tantalum layer. On top of this Ta layer, another layer, about 1.5nm thick, appears brighter than the Ta one but darker than the following Ni layer. This intermediary contrast suggests some mixing between the Ta and Ni layers. For the 500°C annealed sample, the dark contrast layer disappears in favor of a thicker intermediate contrast layer (about 3nm here) which indicates that the annealing induces a higher mixing between Ta and Ni.

The STEM-EDX map in figure VI-7 reveals the homogeneous thicknesses of the Ta and Ni layers over large areas of the prepared sample. It also confirms the significant interdiffusion between Ta and Ni with a light blue-green instead of green Ta color in contact with HfO_2.

On the STEM-EDX profiles of figure VI-8, the relative positions of the Hf and O profiles for the sample before annealing confirms the significant thickness of the SiO_2 native oxide with an important shift of O toward the Si substrate. The shift between the two profiles is increased by the 500°C annealing proving the SiO_2 regrowth. O is also present in the Ni and cap-TiN layers.

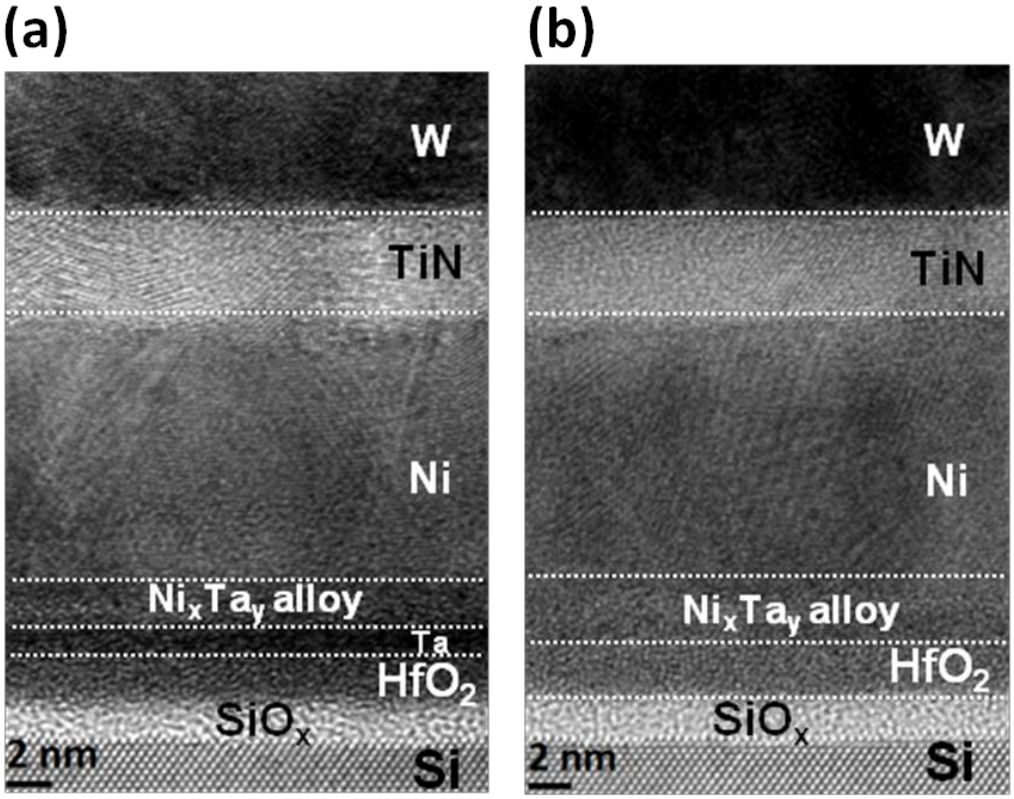


***Fig. VI-6**- HRTEM images of a (a) before and (b) after 500°C annealed HfO_2/Ta 2nm/Ni 10nm/TiN5nm/W stack*

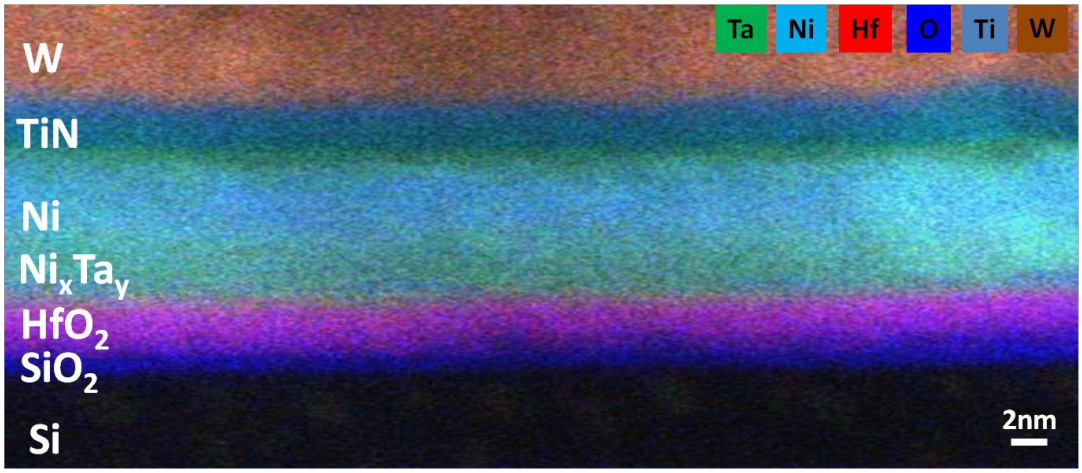


***Fig. VI-7**- STEM-EDX map of the 500°C annealed HfO_2/Ta 2nm/Ni 10nm/TiN5nm/W electrode*

This oxygen does not come from the IL because NiO is more stable than SiO_2 (Fig. VI-17). It is most probably the result of residual oxygen in the process chamber during Ni deposition. Note also that the air breaks performed between the Ta and Ni deposition and before the W

plug deposition are also sources of oxygen. As a consequence, Ni is partly oxidized. The phenomenon is amplified for the annealed sample.

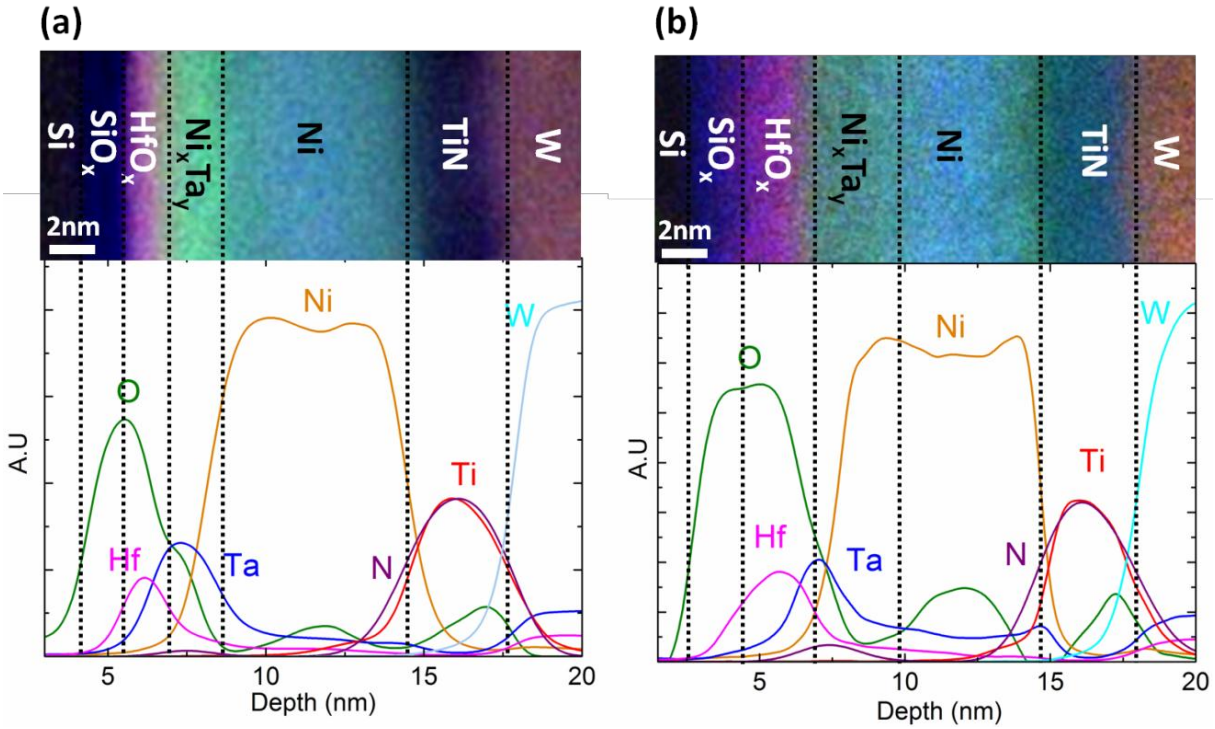


***Fig.VI-8**- STEM-EDX map of a HfO_2/Ta 2nm/Ni 10nm/TiN5nm/W stack and Hf, O, Ni, Ta, Ti, N and W profiles along the stack with localization of the different sublayers (vertical dashed lines)*
(a) before and (b) after the 500°C annealing step

The Ta profile evidences a diffusion of Ta toward the top of the stack, which is more pronounced after annealing. This results in an intermixing, particularly between Ta and Ni. This chemical information supports what was suspected from the HRTEM images about the existence of a mixed TaNi layer above HfO_2. Note the stoichiometric nature of the cap-TiN layer.

The effect of the mixing between the low WF Ta and the high WF Ni is observed on the electrical results (Fig. VI-9, Table VI-1). The reference HfO_2/Ta 10nm/-TiN/W is measured with a low EWF at 4.35 and 4.4eV before and after 500°C annealing respectively whereas the HfO_2/Ta2nm/Ni 10nm/TiN/W is measured with a 0.4 eV higher EWF before annealing, i.e. 4.75eV, and a slightly same value after the 500°C additional annealing, i.e. 4.74eV.

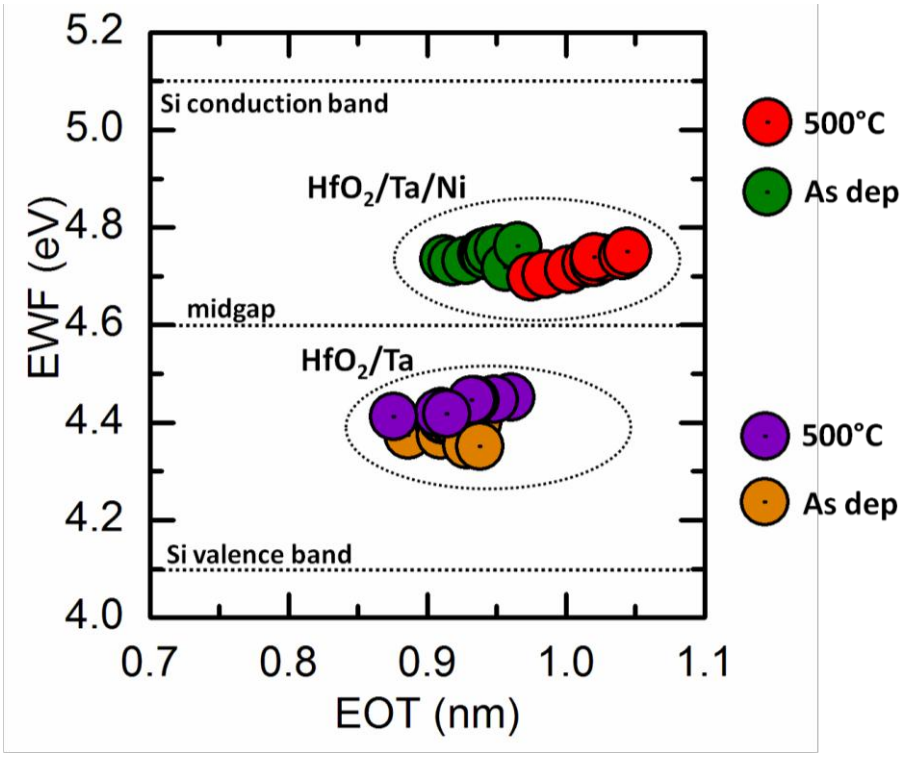


Fig.VI-9- *EWF versus EOT for HfO_2/Ta and HfO_2/Ta/Ni capacitors before and after 500°C annealing.*

Stack composition	EWF (eV)	EOT (nm)
HfO_2/Ta	4.35	0.87
HfO_2/Ta 500°C	4.4	0.89
HfO_2/Ta/Ni	4.75	0.92
HfO_2/Ta/Ni 500°C	4.74	0.96

Table VI-1- *EWF and EOT values obtained with HfO_2/Ta and HfO_2/Ta/Ni before and after 500°C annealing step.*

As we are studying pure metals alloying, we suppose that Ni and Ta intermixing may result on the formation of a new crystalline phase, which has its own vacuum WF. Therefore, In order to investigate on the Ta-Ni alloying effect on the crystalline structure of the metal gate, X-ray diffraction (XRD) analysis has been achieved on thick SiO_2/10nm Ta/ 30nm Ni stack in order to obtain signals with good quality. In addition, the possible evolution of the crystalline structure regarding temperature is investigated with 400°C and 500°C annealing for 15min duration (see Fig. VI-10).

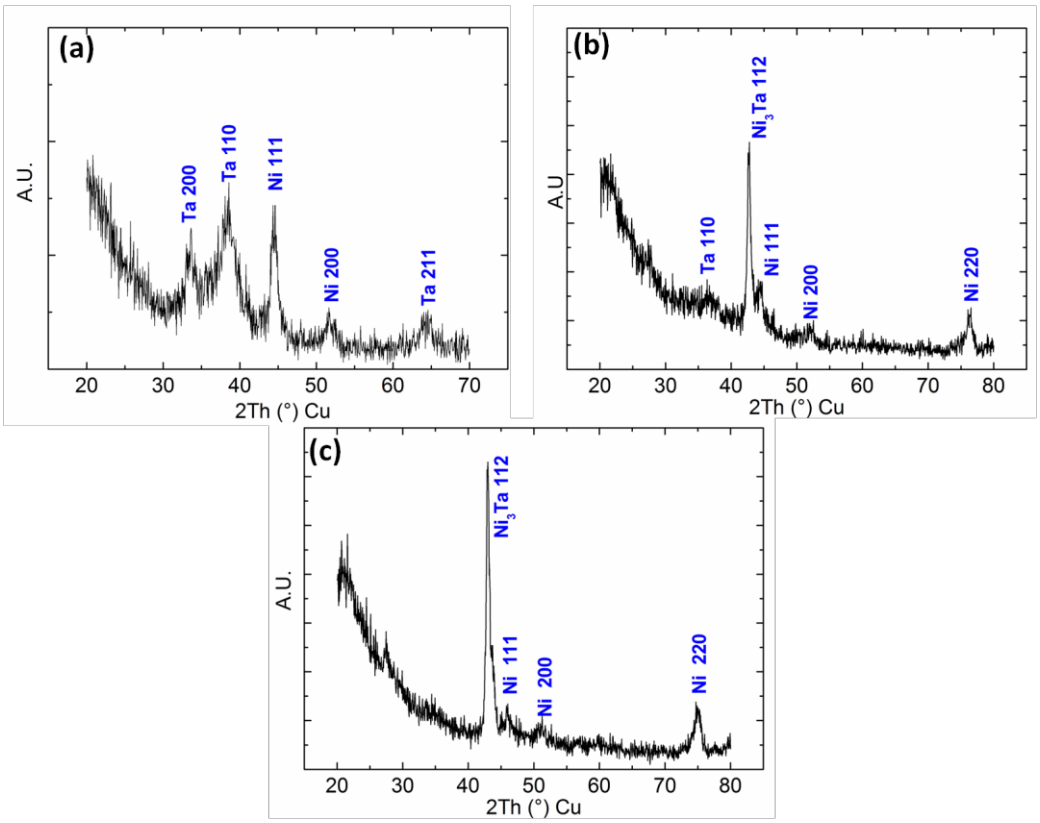


***Fig.VI-10**- XRD spectra of a SiO_2/Ta 10nm/Ni 30nm stack at room temperature (a) and annealed at 400°C (b) and 500°C (c)*

First, the room temperature $Si/SiO_2/Ta/Ni$ diffraction spectrum (Fig.VI-10(a)) reveals the presence of the well-known cubic based Ta crystalline structure (Ta 200, 110 and 211 peaks) associated to the Ni one (Ni 111 and 200 peaks). After 400°C annealing (Fig. VI-10(b)), we notice the vanishing of Ta 200 and 211 peaks, associated to significant decrease of Ta peak in the 110 reflection. In addition, we report the occurrence of Ni_3Ta alloy (112 peak), which attests that a significant intermix between Ni and Ta layers occurs at 400°C annealing and results on a new Ni_3Ta phase formation. Furthermore, the increase of annealing temperature to 500°C (Fig.VI-10(c)) reveals a higher level of intermixing between Ni and Ta with no more visible Ta contribution together with the increase of the Ni_3Ta peak intensity. We suppose that after 500°C annealing, the thermodynamic equilibrium is reached with total consumption of the Ta layer associated to the Ni_3Ta phase formation. This XRD study proves the formation of a new phase when a Ni layer is deposited on top of a Ta layer as predicted by the Ti-Na binary phase diagram of figure VI-11 [Okamoto00]. In our devices, the Ni/Ta ratio is higher than the one studied by XRD, rather near 5 (see the STEM-EDX profiles of Fig. VI-8). In this composition domain, the Ni-Ta phase diagram predicts the formation of a mix of two phases, Ni_3Ta and Ni_8Ta. Knowing the high work function of Ni in vacuum (5.3 eV), the formation of

Ni-rich Ni_xTa phases explains the increase of the work function observed after Ni deposition on HfO_2/Ta. Notice that lower thicknesses (Ta 2nm/Ni 10nm) are involved during the Ta-Ni intermix for the devices samples which suggests that 500°C, short time (1min) annealing is sufficient to reach thermodynamic equilibrium instead of 500°C, 15min for the thick XRD samples.

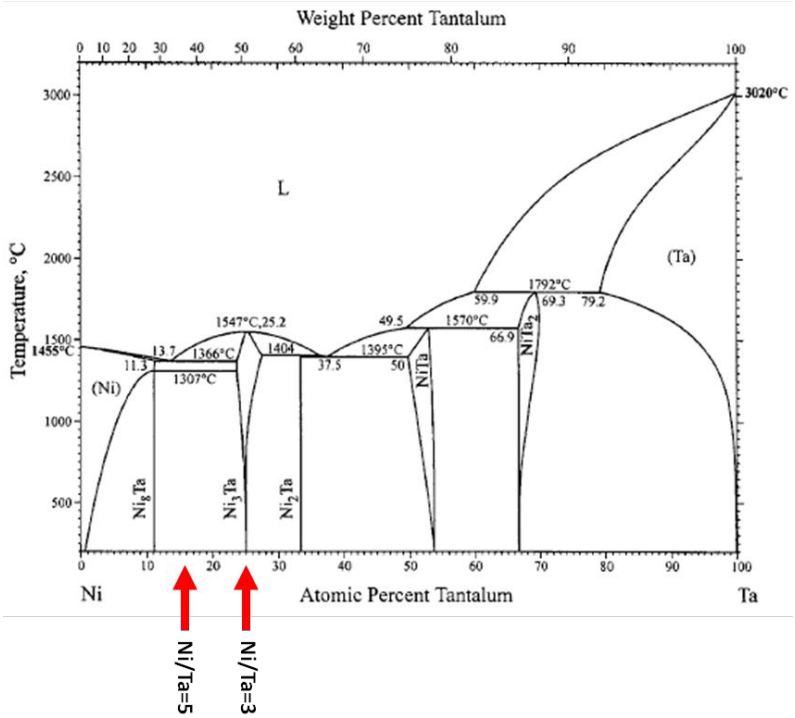


***Fig. VI-11**- Ta-Ni binary phase diagram from [Okamoto00]*

Ta/Ni thin films alloying was already studied by Matsukawa *et al*. on SiO_2 insulator [Matsukawa05]. Here, we clearly record a higher work function for Ta/Ni deposited on HfO_2 (4.75eV) than Ta/Ni deposited on SiO_2 (4.5eV). Matsukawa *et al*. suggest that the gate EWF is pinned at the SiO_2/Ta value due to the interaction between Ta and SiO_2. In contrast, due to the higher stability of Ta on HfO_2 oxide reported here, and since it exists a strong intermixing between Ta and Ni since the lowest temperatures, the work function of our gate electrode seems clearly induced by new crystalline phase formation Ni-rich. Thus, it could explain the high work function obtained with HfO_2/Ta/Ni electrode.

Besides, theses electrodes exhibit sub-1nm EOT values before and after 500°C annealing with the recorded values reported in table VI-1. These very low EOT values suggest the high stability of the Ta-Ni stack on HfO_2. Moreover, despite the process air-break done between Ta and Ni, we observe no significant degradation of EOT indicating that Ta is a strong barrier against the diffusion of air break oxygen which enables sub-1nm EOT values.

In conclusion, we show in this section that deposition of Ni on HfO_2/Ta results in a p-type electrode with an EWF of 4.75eV and a low 0.92nm EOT. In addition, we demonstrate the reasonable thermal stability of both electrode work function and EOT for temperature up to 500°C. The obtained 0.4eV difference between HfO_2/Ta and HfO_2/Ta/Ni makes these alternative electrodes at first order useable for a low thermal budget CMOS FDSOI co-integration.

VI-4. Ni-Ti alloying: a stable/reactive system for co-integration on HfO_2

By replacing tantalum with titanium as the low work function material while keeping nickel as the high work function metal, Polishshuk *et al*. showed a possible co-integration using Ti/Ni on SiO_2 for low thermal budget gate last approach [Polishshuck01]. In their study, titanium is deposited first on SiO_2 as the n-MOS side metal while the diffusion of Ni to SiO_2/Ti interface is used for p-MOS side work function modulation. However, knowing the high reactivity of titanium toward oxygen demonstrated in chapter III, we suspect that its direct deposition on HfO_2 will result on a thermally and chemically unstable gate electrode. Therefore, we study here a possible co-integration of Ni and Ti on HfO_2 with Ni deposited first. The deposition of titanium on HfO_2/Ni is achieved in order to obtain a low nMOS adapted work function. In particular, we investigate the effect of Ti alloying with Ni on the reactivity of Ti toward oxygen. Here again, the thermal stability of HfO_2/Ni/Ti is assessed to T≤500°C. The successive layers in the studied stack here are Si/SiO_2/HfO_2 2nm/Ni 2nm/(Ti 2nm)/TiN 5nm/W.

The different layers composing the stack are directly visible on the chemical STEM-EDX map of figure VI-12 of the stack before additional annealing. In particular, Ni and Ti layers appear mixed. The STEM-EDX profiles of the stack before and after an additional 500°C annealing are very similar (Fig. VI-13) except for the N and Ti profiles in cap-TiN. After annealing, the nitrogen profile shifts toward the W contact metal. We assume that it is due to N pushback in cap-TiN by Ni, since no stable NiN phase exists. Such effect is also known as “snow plow” effect of N by Ni.

Otherwise, examining O and Hf profiles evidences thicknesses significantly larger than 1 nm. Like for the Ta/Ni electrode, this is assigned to the presence of a thick native SiO_2 oxide as the thin chemical oxide formation step has also been skipped for the blanket samples of this

series. Moreover, the Ti profile goes deep inside the Ni one which indicates the significant diffusion of titanium in nickel. Finally, even if the N profile goes inside the Ni-Ti mixed layer, it is zero at the HfO_2/Ni-Ti interface.

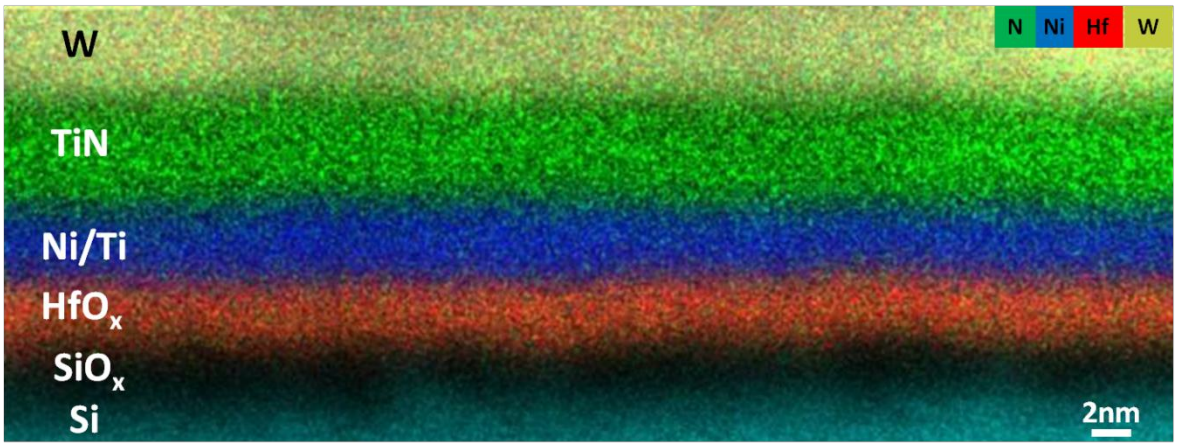


***Fig. VI-12**- STEM-EDX map of HfO_2/Ni 2nm/Ti 2nm/TiN2nm/W electrode before 500°C annealing.*

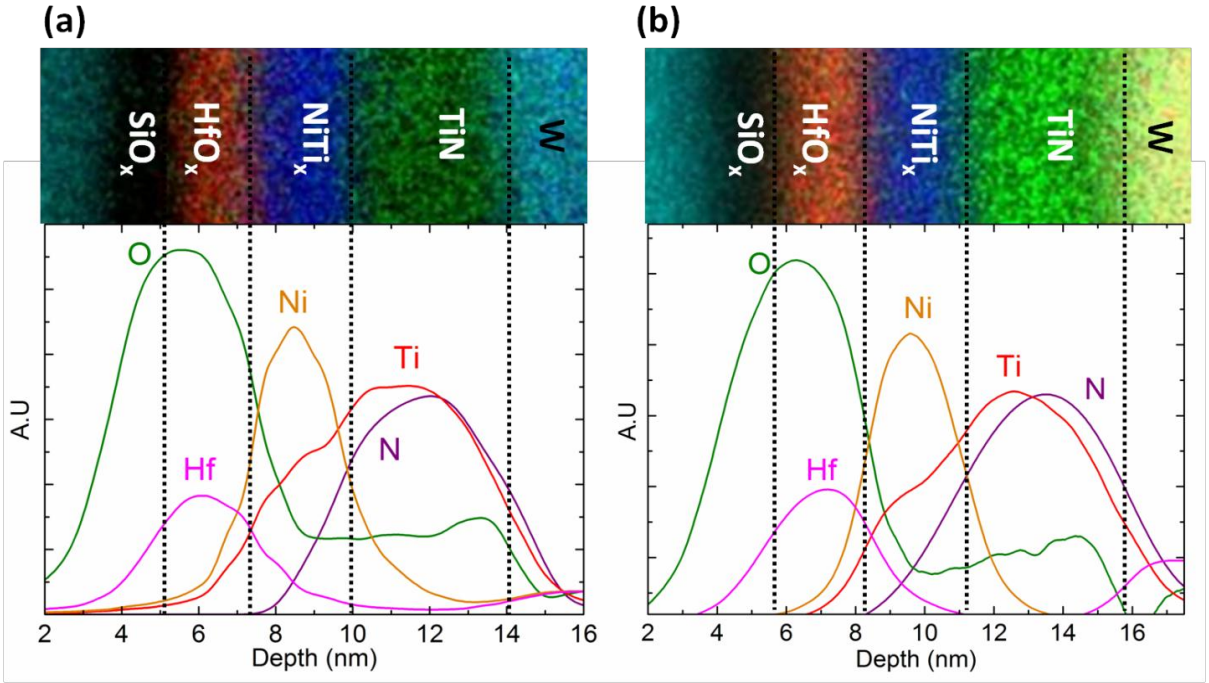


***Fig.VI-13**- STEM-EDX map of a HfO_2/Ni 2nm/Ti 2nm/TiN5nm/W stack and Hf, O, Ni, Ta, Ti, N and W profiles across the stack with localization of the different sublayers (vertical dashed lines) (a) before and (b) after the 500°C annealing step*

The XPS core level spectra of Hf *4f*, N *1s*, Ti *2p* and Ni *2p* are recorded from a backside SiO_2/HfO_2/Ni/Ti/TiN/W prepared sample are presented in figure VI-14.

Only one component at 404 eV is extracted from the N *1s* spectrum. It is assigned to N-O bonds with no visible Ti-N bonds. This is reasonable. Indeed, due to the significant thickness

of native SiO_2 (about 2nm) and the low depth probed from the backside of the sample (~5nm), the analysis is limited to a volume going from the SiO_2 native oxide to the first nanometer of the Ni-Ti mixed layer. Ti *2p* spectrum confirms this observation with only Ti-Ti bonds of the metal (spin-orbit coupling components respectively located at 454 and 460 eV). Then, three components are identified on the Ni *2p* spectrum and assigned to Ni-Ni (also possibly to Ni-Ti) bonds at 852.9 eV, Ni-O bonds at 854.1 eV and a satellite at 859.9eV. No diffusion of nitrogen to the HfO_2 is revealed by Hf *4f* spectrum where only Hf-O component is identified with no traces of Hf-N bonds.

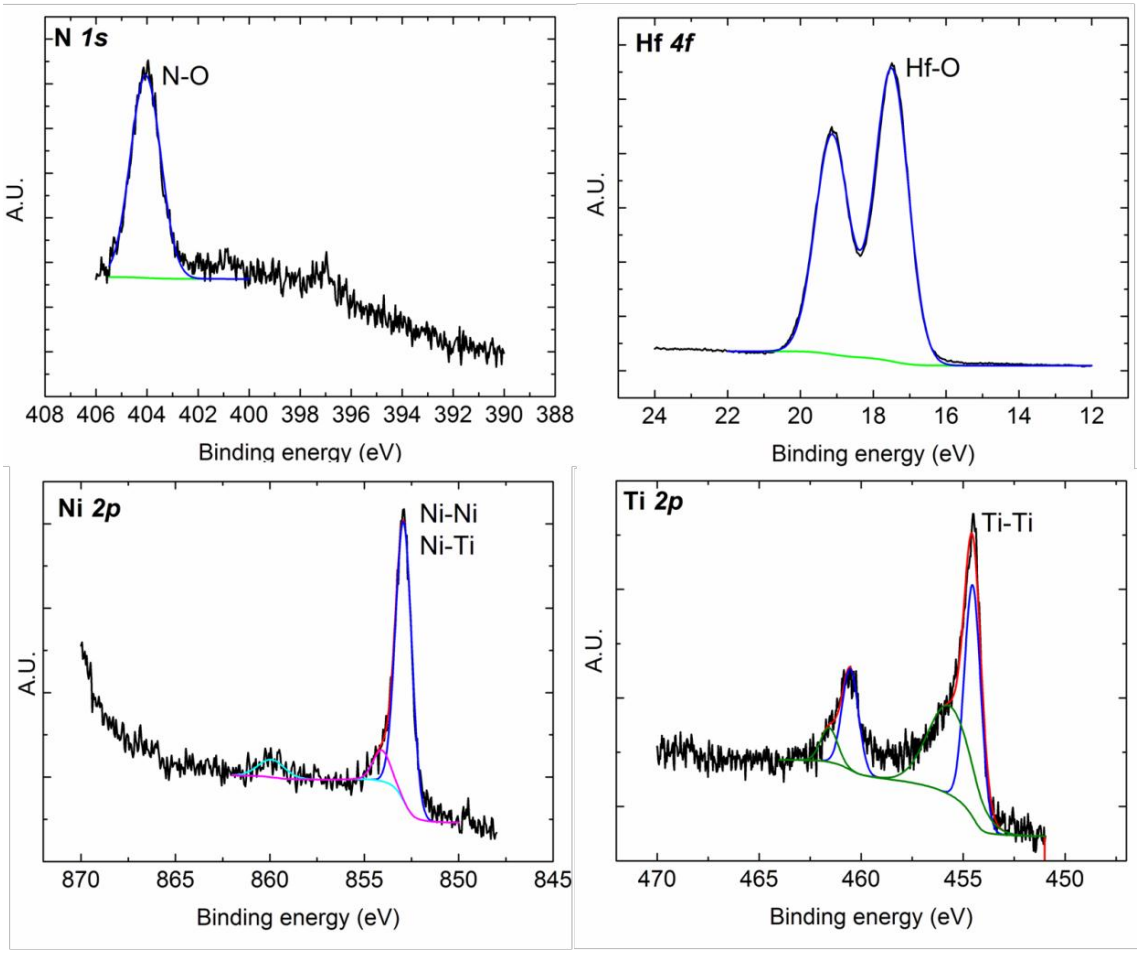


***Fig.VI-14**- N1s, Hf4f, Ni2p, and Ti2p XPS core level spectra obtained from a backside prepared HfO_2/Ni/Ti/TiN/W sample*

Fig.VI-15 summarizes the C(V) measurements achieved on HfO_2/Ni reference and HfO_2/Ni/Ti electrode before and after the 500°C additional annealing.

First, it shows that HfO_2/Ni 2nm electrode results in a clearly higher EWF than the HfO_2/TiN reference studied in chapter III, with EWF=5.0eV measured at 0.99 nm EOT. The deposition of Ti on Ni in HfO_2/Ni/Ti electrode results in a significant lowering of the EWF measured at

4.2eV for both as deposited and 500°C annealed samples. The STEM-EDX analysis indicates that the low the work function recorded for HfO_2/Ni/Ti appears to be induced by the alloying of Ni and Ti i.e. Ni-Ti significant interdiffusion, resulting in the formation of a new low work function Ni_xTi alloy in contact with HfO_2. Since no crystallographic analysis has been achieved, we are not able to identify the exact Ni_xTi phase formed after the interdiffusion of Ni and Ti. Meanwhile, the measured EWF tends to support the formation of a Ti-rich Ni_xTi phase, since a low Ti-like work function is recorded.

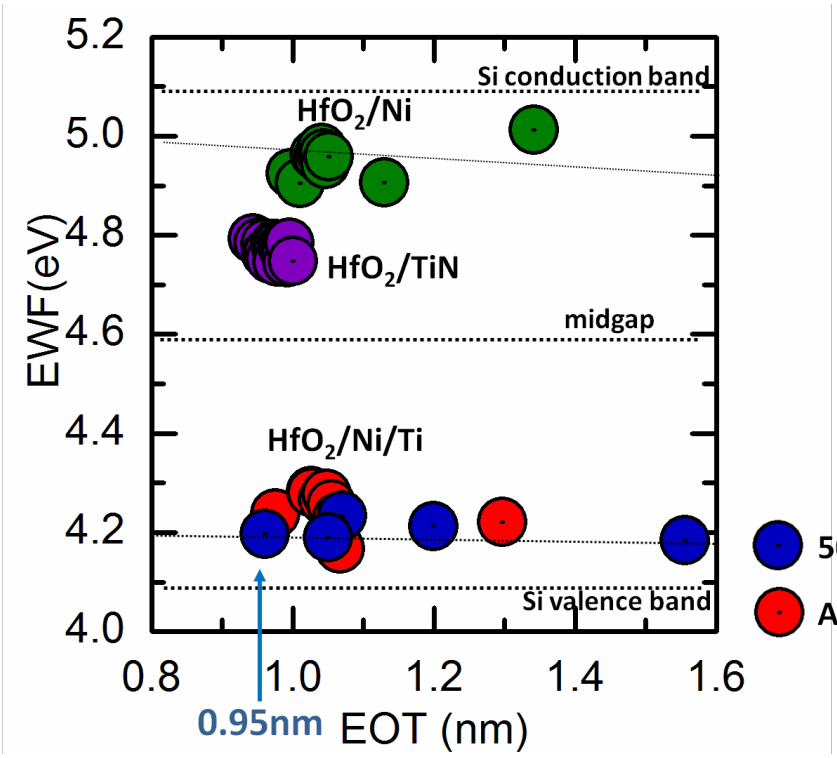


Fig.VI-15- *EWF versus EOT of HfO_2/TiN and HfO_2/Ni references compared to HfO_2/Ni/Ti electrodes before and after 500°C annealing*

Besides, together with this EWF shift, we notice a slight decrease of the EOT compared to HfO_2/Ni reference with EOT=0.97 nm and 0.95 nm recorded with as deposited and 500°C annealed samples. In addition, we observe that in contrast with HfO_2/TiN 2nm/Ti 2nm studied in chapter III, no aggressive scavenging of oxygen from SiO_2 or HfO_2 is reported here. This higher stability toward oxygen may be assigned to the lowering of oxygen solubility in titanium by nickel alloying as the solubility of O in Ni is very low (about 0.05%) in Ni-O system (see figure. VI-16 [Neumann84]).

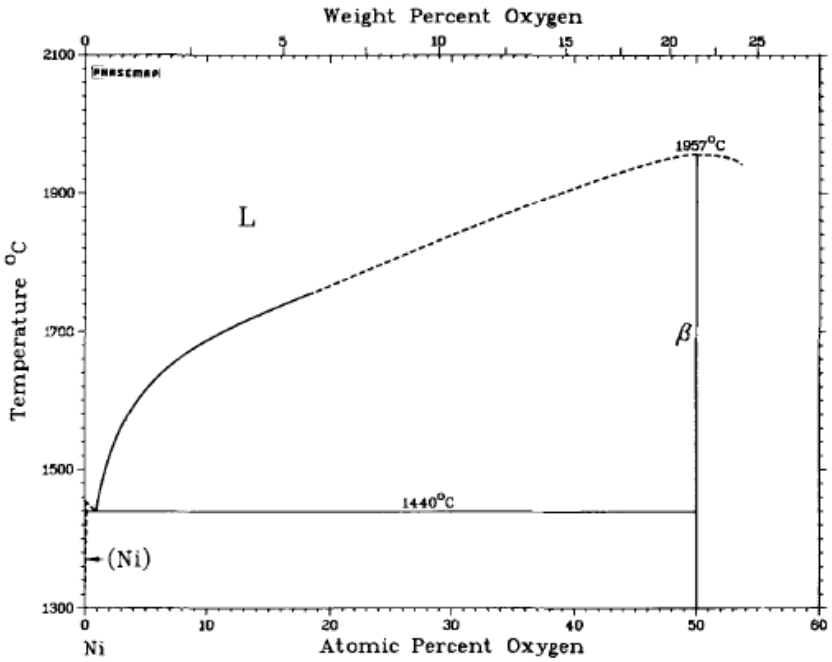


Fig.VI-16- *Ni-O binary phase diagram of Ni-O from [Neumann84]*

The solid solubility of oxygen in $NiTi_x$ was previously estimated at about ~0.045 at % [Otsuka99]. Therefore, the amount of oxygen that can be absorbed by Ti is significantly reduced by alloying it with Ni which avoids an aggressive scavenging of oxygen from the dielectrics.

We notice a common behavior of Ti stabilization toward O between Ti/Ni and Ti/Al alloys investigated in chapter III. In both cases, the use of Ni or Al elements with low O solubility reduces the ability of Ti to scavenge O from the dielectrics. However, Ti/Ni system appears to be more stable than Ti/Al at 500°C, since the Gibbs free energy of Ni-O is clearly above Al_2O_3 as observed in figure VI-17 (i.e. driving force of Ni toward O is clearly lower than Al).

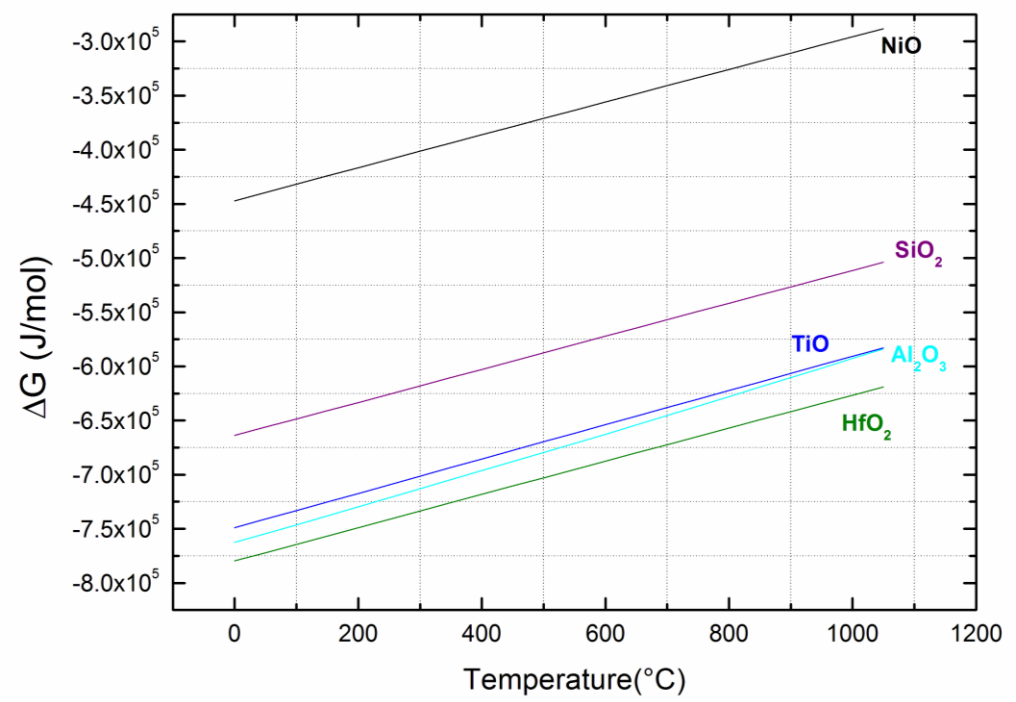


Fig.VI-17- *Ellingham diagram of the Gibbs free energy of formation vs. temperature of NiO compared to TiO, Al_20_3, SiO_2 and HfO_2 oxides*

Therefore, Ni has a very low contribution to the oxygen scavenging from the SiO_2/HfO_2 bi-layer whereas, Al through the formation of Al_2O_3, as shown in chapter III, enables more or less oxygen reduction from SiO_2 oxide depending on the Al layer thickness and thermal budget.

From this study, we can conclude that uses of Ni/Ti alloying is very promising for a CMOS co-integration at low thermal budget (T≤500°C) in gate last approach.

VI-5. Conclusion

In conclusion, we demonstrate in this chapter that Ta and Ni are very promising gate and stable gate electrode materials.

First, tantalum deposition on the reference HfO_2/TaN results in an nMOS adapted EWF with 4.3 eV measured on HfO_2/TaN 2nm/Ti 10nm. The mechanism of EWF shift regarding a HfO_2/TaN refrence is assigned to the formation of a substoichiometric TaN_x which consists in a combination of Ta_2N and Ta phases. In addition, it exhibits a good chemical and thermal stability up to 500°C with stable EWF and EOT. This is assigned to the higher Gibbs free energy of formation of Ta oxide with respect to Si oxide ($\Delta G_{Ta2O5} > \Delta G_{SiO2}$)

reflecting no reduction of the SiO_2 IL together with an efficient cap-TaN barrier against O diffusion keeping a constant EOT after 500°C annealing.

Besides, low WF Ta with high WF Ni alloying in HfO_2/Ta/Ni electrode results in p-MOS adapted EWF=4.75eV. Good thermal stability with constant EWF and EOT is also reported in this case due to the alloying of highly stable Ta and Ni materials. This approach is very promising for FDSOI devices since 0.4eV separation is obtained between the nMOS (Ta) and pMOS (Ta/Ni) electrodes.

Alloying stable Ni with highly reactive Ti in a HfO_2/Ni/Ti electrode, we demonstrated a -0.8eV EWF drop to 4.2eV measured with sub-1nm EOT=0.97nm compared to the reference HfO_2/Ni electrode. Ni/Ti alloying exhibits a high chemical stability after annealing with constant EWF together with a slight improvement of the EOT=0.95nm. This high stability toward dielectrics is assigned here to the lowering of oxygen solubility of Ti by alloying it with Ni which reduces the amount of oxygen that Ti can absorb. This results in a moderate oxygen scavenging of the SiO_2 IL dielectric even after annealing at 500°C.

Conclusion

Beyond the CMOS 65nm node, the replacement of the historical SiO_2/Polysilicon gate stack by High-k/Metal structures was one of the most important challenges of the semiconductor industry. This important modification of the gate materials arose intensive studies on metals stability on high-k oxides together with investigation on suitable work function (WF) for both n and pMOS transistors. In parallel, different integration schemes have been developed to reach chemically stable electrode with relevant effective work function (EWF). The gate last integration scheme was chosen as an alternative to the historical gate first approach thanks to its overall low thermal budget, which allows higher control of the chemical species interdiffusion and reaction. It enables better modulation of the electrode EWF while keeping good metal stability toward the dielectrics thus allowing the scaling of the equivalent oxide thickness (EOT). For advanced sub-20nm planar CMOS technology, due to the aggressive narrowing of the gate length, very thin metal layers must be deposited in order to have an optimal gate electrode contact metal filling while keeping a suitable EWF for both n and pMOS sides and efficient EOT scaling (<0.9nm, ITRS requirement for planar 20nm nodes).

Within an industrial context, i.e. the 20-14nm CMOS integration with a low thermal budget process, the objective of this thesis work was to highlight the key parameters that enable the control of the EWF and the scaling of the EOT. To reach this goal, a systematic structural and analytical study was conducted on nanometric-sized stacks deposited on blanket wafers, i.e. metal multilayers deposited on HfO_2. In parallel, electrical measurements were performed on the corresponding capacitors in order to determine the two parameters discussed in this work, i.e. the EWF and the EOT. Then correlations between the analytical and electrical measured parameters have been discussed on the basis of thermodynamic considerations. Before investigating the stacks, it was demonstrated that, in the context of low thermal budget process

- the EWF is mainly dependent on the chemical state of the metal gate just at and above the High-k/Metal gate interface;
- the EOT is scaled through a remote scavenging process where the driving force is dependent on the Gibbs free energy of the metal oxide formation compared to the SiO_2 one.

Owing to the very small size of the stack, local investigations based on transmission electron microscopy (TEM) were favored in this work. Systematic structural and chemical studies by high resolution TEM (HRTEM) and scanning TEM-energy dispersive X-ray (or to a less extent electron energy loss spectroscopy, STEM-EDX/EELS) were conducted on state of the art microscopes in order to provide images from which fine and thorough description of the structural and chemical organization in the stack can be proposed. STEM-EDX elemental profiles were useful to provide semi-quantitative information on the spatial distribution of the elements across the stack from the substrate to the top metal plug. The local analytical studies were completed by the systematic consideration of the way atoms are bonded in the stack. X-ray Photoelectron Spectroscopy (XPS) used for this gave a more macroscopic view of the stack. It was performed on specifically backside prepared samples. This specific sample preparation was also beneficial for Time of Flight-Secondary Ion Mass Spectrometry (ToF-SIMS) a sensitive method that was necessary for providing average information particularly for the case of heterogeneous stacks.

Following this methodology enables to give reliable comparison between the different studied materials and allows confident interpretation of the electrical results obtained from MOS capacitors C (V) measurements. For the interpretation, we often based our discussion on thermodynamic concepts i.e. Gibbs free energy of formation, solid solubility and phase diagrams. It was a way to approach the understanding of the complex chemical interactions between the different species in the gate stack layers.

In this work, we studied different metallic materials deposition on HfO_2 oxide in order to evaluate the EWF controllability and EOT scaling level for the corresponding gate stack structures.

First, we followed a known strategy where a reactive n-type metal is deposited on the p-type metal TiN (HfO_2/TiN, EWF=4.85eV) in order to obtain an nMOS adapted EWF electrode. After learning how the low WF metals Ti and Al behave separately on TiN, we investigated the effect of alloying Ti with Al.

In particular, we have shown that the nMOS adapted EWF of both TiN/Ti and TiN/Al when deposited on HfO_2 corresponds to two different mechanisms: formation of substoichiometric TiN_x for TiN/Ti stack and low WF aluminum segregation at the HfO_2/TiN interface for TiN/Al. The different behaviors of Ti and Al metals against oxygen scavenging from the SiO_2 IL is mainly related to their difference for O solid solubility (in Al, close to 0% at 400°C and

in Ti, 40% at 400°C) despite the very close free energy changes associated to the formation of SiO_2 from the metal oxides (TiO or Al_2O_3). Indeed, total scavenging of O from the dielectrics is observed for the TiN/Ti electrode where Ti can incorporate large amount of O whereas slight scavenging is reported for the TiN/Al electrode with no capacity to absorb O.

For TiN/TiAl bi-layer, low EWF is obtained and assigned to substoichiometric TiN_x formation induced by N scavenging by TiAl. The higher chemical stability of TiN/TiAl compared to TiN/Ti with no drastic reduction of O from the dielectrics but with a higher oxygen scavenging than with the TiN/Al electrode is the result of moderate reduction of the solid solubility of O in TiAl due to alloying Al with Ti. An nMOS adapted EWF=4.25eV together with state of the art EOT=0.83nm were obtained for the TiN/TiAl electrode.

These investigations showed that metal gate interactions regarding nitrogen and oxygen are key parameters for the control of the gate EWF modulation and EOT scaling in HfO_2/TiN/Metal stacks.

Based on the gained knowledge, we deposited $TiAlN_x$ layers directly on HfO_2 with different and controlled N flow during the fabrication process in order to have a better control on the EWF and the EOT. We demonstrated, for the first time on HfO_2, a ~0.8eV gap between the low-N flow $TiAlN_{x<1}$ EWF=4.2eV and the high-N flow $TiAlN_{x>1}$ EWF=5.0eV with sub-1nm EOTs.

The thermal stability of the above electrodes was evaluated in order to give some insight on their adaptability for a higher thermal budget gate first or innovative 3D integration. Since 500°C annealing, all these gate electrodes loose their chemical stability with Al_3Ti formation in the Si substrate (spiking). It was observed for TiN/Al, TiN/TiAl (Al~50%), low and medium N-$TiAlN_x$. The TiN/TiAl (Al~20%) is stable against spike but looses its stability regarding oxygen with aggressive scavenging of the SiO_2 IL. Significant degradation of EOT together with EWF lowering is observed for the high-N $TiAlN_{>>1}$.

In order to find other solutions with less limited thermal stability than the TiAl(N)-based electrodes, we had the will to think about alternative thermally stable gate materials. We first considered a metal more stable than Ti with respect to O, i.e. Ta. Similarly to the TiN/Ti electrode, the TaN/Ta based electrode was studied for thermal budget going from 400°C to 600°C. The electrode is stable for both temperatures with an nMOS adapted EWF of 4.3 eV and a sub-1nm EOT=0.9nm for both 400 and 500°C thermal budgets. Same EWF mechanism

was reported for TaN/Ta than for TiN/Ti or TiN/TiAl with subsoitchiometric TaN_x formation in contact with HfO_2. Constant EOT after the 500°C annealing was recorded thanks to the very low driving force of Ta toward O in SiO_2 ($\Delta G_{Ta2O5} > \Delta G_{SiO2}$). The comparison of the different thermodynamic properties of Ta, Ti and Al toward oxygen enables us to suggest a model to describe the different metals behavior regarding oxygen. We assume that the oxygen scavenging is related to the first order to the Gibbs free energy change associated to MO_x formation starting from SiO_2 (ΔG) which determines if the metal is able to reduce oxygen from the dielectric or not. Then a second order parameter is the concept of oxygen solubility, which impacts only the metals which form oxides with lower Gibbs free energy of formation than the one of SiO_2 :

- if solubility of O in M is high, it results in an oxygen scavenging level independent on the M layer thickness (typically Ti case)
- if solubility of O in M is low, it results in an oxygen scavenging level dependent on the M layer thickness (typically Al case)

We continued to investigate new options for better thermal stability. Thanks to the high chemical stability of Ta toward oxygen and its low WF in vacuum (4.25eV), an nMOS first integration process on HfO_2 strategy was followed. It consists in depositing the high WF Ni on the HfO_2/Ta in order to obtain a pMOS adapted EWF electrode. We demonstrated that alloying Ni with Ta results in the formation of new Ni-rich Ni_xTa metal alloy. This results in a pMOS adapted EWF of 4.75eV with ΔEWF=+0.4eV regarding HfO_2/Ta reference together with sub-1nm EOT for both 400°C and annealed 500°C samples. The EWF separation between n and pMOS electrodes makes this approach adapted for FDSOI and thin body CMOS integration.

Another strategy was to alloy the stable high WF Ni with the reactive low WF Ti with Ni-first deposition on HfO_2. We showed that alloying Ni with Ti in HfO_2/Ni/Ti electrode results in significant drop of the EWF with ΔEWF= -0.8eV compared to HfO_2/Ni reference recorded at EWF=5.0eV. We also demonstrated the high stability of the Ni/Ti gate electrode toward oxygen for 400 and 500°C thermal budget. It is induced by alloying Ti with Ni, which reduces the oxygen solid solubility in Ti and thus results an a slight oxygen scavenging from the SiO_2 IL.

All the studied materials in this work have to be integrated in final transistor devices before obtaining a reliable answer about their thermal and chemical stability on HfO_2. Regarding the

first results gathered in this thesis work, we can suggest to use a high amount of Al in TiAl metal alloy (30<Al<50%) with careful optimization of base-TiN thickness to obtain the needed chemical and thermal stability of the HfO_2/TiN/TiAl electrode. As an alternative, we think that Ta/Ni is a reliable solution to replace present TiN based electrodes. However, Ta and Ni deposition must be performed in situ to avoid eventual air beaks, which may result in lower EOT. Ta and Ni ratio have to be optimized to obtain the desirable EWF.

For a better understanding of the mechanisms underlying the modifications in the state of the gate stack after processing, we tried to use thermodynamics at a simple level. Most probably, this aspect of the work could gain in-depth if a common work with specialized people in this area can be developed.

French Summary

Compréhension de la modulation du travail de sortie de métaux de grilles pour l'intégration à bas budget thermique du CMOS 20-14 nm

Introduction

L'ère de la microélectronique a commencé par la vision théorique de Lilienfeld d'un composant servant à contrôler le courant, brevetée en 1925. Le premier transistor bipolaire à base de Ge fut proposé par trois ingénieurs des laboratoires Bell: Bardeen, Brattain et Shockley en 1947. Ils reçurent pour cela le prix Nobel de physique en 1956. Deux ans plus tard, Jack Kilby, ingénieur chez Texas Instruments (Prix Nobel en 2000), réalisa le premier circuit intégré à base de silicium qui permit la réduction de la taille et du coût des ordinateurs en intégrant sur le même circuit plusieurs transistors. Enfin en 1960, Khang et Attala ont fabriqué le premier MOSFET (Metal Oxide Semiconductor Field Effect Transistor) sur Silicium. Ces différentes avancées ont permis à IBM de fabriquer le premier ordinateur à base de transistors MOS sur silicium, l'IBM 7000. Depuis, la réduction de la taille des transistors élémentaires a permis d'augmenter considérablement le nombre de transistors par puce et en même temps de réduire le coût de fabrication par transistor tout en améliorant les performances des puces électroniques. A la même époque (1965), le co-fondateur d'Intel Gordon Moore prédit que le nombre de transistors doublerait environ tous les deux ans avec une augmentation des performances et une réduction des coûts de fabrication à chaque nouveau nœud technologique.

Jusqu'à la fin des années 90, cette miniaturisation a pu être réalisée grâce à la réduction de la taille des transistors à base de silicium constitués d'un substrat de silicium, d'un oxyde de grille en silice native (SiO_2) et d'une grille en polysilicium (poly-Si). Cependant, l'amincissement de la silice nécessaire pour maintenir un contrôle suffisant sur le canal de conduction en augmentant le couplage capacitif s'accompagnait en même temps d'une augmentation exponentielle des courants de fuite. La miniaturisation ne pouvait donc plus continuer seulement avec la silice. La seule issue consistait à la remplacer par un isolant à constante diélectrique plus élevée (appelé high-k). Dans les années 2000, les oxydes métalliques à permittivité élevée à base de Zr ou de Hf (ZrO_2, HfO_2) ont été largement étudiés comme de potentiels remplaçant de SiO_2 comme oxyde de grille. Finalement, c'est l'oxyde d'hafnium (HfO_2) qui a été choisi à cause : (i) de sa constante diélectrique élevée, (ii) de ses décalages de bande de conduction et de valence adaptés par rapport aux bandes du silicium et (iii) de sa bonne stabilité thermodynamique. En plus de l'introduction de HfO_2, une électrode de grille en métal a dû être intégrée afin de limiter la dégradation de l'épaisseur d'oxyde

équivalent (EOT) due à la déplétion du polysilicium (poly-Si) utilisé comme grille en plus de la difficulté rencontrée pour moduler son travail de sortie effectif (EWF).

Cependant, ce changement abrupt des matériaux de grille (SiO_2/poly-Si à HfO_2/Métal) a apporté son lot de difficultés. En effet, l'intégration classique dite « gate first » avec une étape de recuit d'activation des dopants source/drain à haute température (1050 °C) altère la travail de sortie effectif de la grille en raison de diffusions et réactions incontrôlées des espèces chimiques contenues dans l'empilement de grille. C'est pourquoi, une alternative a été proposée qui consiste à intégrer l'empilement HfO_2/Métal avec un budget thermique inférieur à 500°C. Cette approche à bas budget thermique est connue sous le nom d'intégration « gate Last » ou damascene.

Au début de ce travail, seul Intel utilisait l'intégration bas budget thermique « gate last » pour la production de sa technologie CMOS 45 et 32 nm alors que STMicroelectronics avec les autres membres de l'Alliance ISDA (International Semiconductor Development Alliance) suivaient l'intégration « gate first » pour son nœud CMOS 32 nm. Ma thèse (cifre STMicroelectronics) avait pour objectif de déterminer pour STMicroelectronics les paramètres clés qui contrôlent la tension de seuil du transistor (V_{th}) et l'épaisseur de capacité équivalente (CET) de l'électrode de grille, i.e. le travail de sortie effectif (EWF) et l'épaisseur diélectrique (EOT) de l'empilement de grille. Cela a été fait dans la perspective d'une intégration à faible budget thermique pour les nœuds CMOS sub-20nm de STMicroelectronics.

Ce travail de thèse a été réalisé sur 3 sites différents: le CEA Leti à Grenoble, STMicroelectronics à Crolles et le CEMES-CNRS à Toulouse. Des outils de production de masse dans l'industrie des semi-conducteurs ont été utilisés pour le dépôt des métaux de grille, à STMicroelectronics et au CEA-Leti. Des méthodes de caractérisation avancées de matériaux de grille tels que les analyses XPS et TOF-SIMS par la face arrière (CEA-Leti) et des expériences de microscopie électronique à transmission (MET) avec des appareils qui définissent l'état de l'art en terme d'analyse chimique et d'imagerie (Tecnai OSIRIS à Crolles, Cs corrigé Tecnai au CEMES) ont été utilisées pour une caractérisation fine des structures étudiées. Elles ont été mises en œuvre de façon systématique et efficace pour étudier la modulation du travail de sortie effectif des empilements de grilles et la réduction de l'épaisseur d'oxyde équivalent.

Les six parties suivantes résument le contenu de chacun des chapitres correspondants du mémoire. Les équations, figures et tableaux dans ce texte sont appelées avec le même numéro que celui du mémoire et indication de la page du mémoire où les trouver. Enfin, les références bibliographiques se trouvent en fin de mémoire.

En plus de la problématique de l'empilement de grille diélectrique/métal, la première partie introduit les notions de EWF, d'EOT et les moyens pour les moduler. Le choix des couples métalliques TiN/métal (métal : Ti, Al, TiAl, TiAlN) ou des alliages TaNi et NiTi étudiés dans ce travail de thèse est en particulier justifié.

Les différentes techniques de caractérisation utilisées dans ce travail de thèse sont présentées dans une deuxième partie en soulignant surtout l'intérêt que chacune apporte par rapport à l'objet étudié, i.e. un empilement de couches de dimensions nanométriques.

Dans les quatre parties suivantes (III à VI), à la recherche de gilles métalliques pour HfO_2 adaptées à une intégration à faible budget thermique « gate last », nous étudions de façon systématique la distribution des espèces chimiques et les liaisons chimiques qu'elles établissent entres elles dans chacun des empilements de grille à base de nitrure ou à base d'alliages métalliques. En parallèle, nous effectuons des mesures électriques (C-V) sur de larges capacités MOS afin d'extraire les EWFs et les EOTs que les distributions élémentaires mesurées précédemment induisent. Sur la base de ces observations, nous tentons d'expliquer la relation entre le comportement électrique et l'état chimique des empilements.

Dans la troisième et la quatrième partie, nous considérons en particulier le cas d'électrodes métalliques sous forme de couples TiN/métal. Le TiN est bien connu pour son travail de sortie effectif adapté au côté p-MOS lorsqu'il est déposé sur HfO_2. Nous proposons donc des candidats pour le côté n-MOS, co-intégrables avec le TiN. Tout d'abord (partie III), il s'agit de métaux élémentaires réactifs comme le titane et l'aluminium. Puis (partie IV), nous allions Ti et Al en examinant le cas du binaire TiAl (TiN/)TiAl. Finalement (partie IV), sur la base des résultats acquis, nous exploitons l'intérêt de déposer directement le ternaire TiAlN sur HfO_2.

La stabilité thermique limitée de ces empilements est étudiée dans la cinquième partie.
La sixième et dernière partie est centrée sur la recherche d'empilements alternatifs aux métaux à base de nitrures de Ti précédemment étudiés. Ils mettent en jeu des métaux moins sensibles thermiquement comme TaN, Ta, Ni et Ti.

I- Modulation du travail de sortie effectif (EWF) et réduction de l'épaisseur d'oxyde équivalent (EOT) pour l'intégration à bas budget thermique

- **Contrôle de travail de sortie effectif d'un empilement de grille**

Depuis le remplacement de la structure de grille historique SiO_2 / poly-Si par la structure « high-k » / métal (notée dans la suite HK/MG), il était clair pour l'industrie de la microélectronique que la miniaturisation des dispositifs allait dépendre de plus en plus de sa capacité à trouver des matériaux de remplacement et de les intégrer dans une route de fabrication industrielle fiable, ce qui suppose d'avoir une compréhension approfondie du comportement physique et chimique de ces matériaux.

Le remplacement direct de la structure SiO_2/poly-Si par la structure high-k/metal (HK/MG) a très vite montré ses limites : la modulation du travail de sortie effectif des empilements de grille s'est montrée difficile à réaliser à cause du décalage systématique vers le milieu de la bande interdite du Si qui s'opérait après le recuit d'activation Source/Drain (S/D). Pour résoudre ce problème, l'introduction de la structure HK/MG a été accompagnée d'un changement des schémas d'intégrations afin de garantir l'obtention des bons travaux de sortie pour les transistors n et p, indispensables pour le bon fonctionnement d'un inverseur CMOS. L'approche suivie par l'alliance ISDA appelé « capping layer » consiste à déposer une fine couche d'aluminium (lanthane) pour le côté pMOS (nMOS) afin de le faire diffuser jusqu'à l'interface SiO_xN_y-IL/HK et induire un dipôle d'interface qui module le travail de sortie de l'empilement de grille. Cependant, même si l'intégration « capping layer » est utilisée à l'échelle industrielle pour le nœud technologique CMOS 28nm (BULK / FDSOI), il semble que le contrôle des travaux de sortie effectifs des empilements de grille soit difficile après le recuit d'activation S/D. Il se produit une interdiffusion incontrôlée des espèces chimiques présentes dans la structure HK/MG, en particulier de l'azote et de l'oxygène (lacunes d'oxygène dans le HK) qui ont finalement une contribution significative à la modulation du EWF et aussi de l'EOT. L'approche de fabrication mise en œuvre dans nos travaux présentés ici est celle suivie par Intel pour ses nœuds technologiques 45 et 32nm appelés « gate last » et qui consiste à utiliser le poly-Si comme grille sacrificielle qui subit le recuit haute température S/D. Par la suite, cette grille sacrificielle est retirée afin de déposer les métaux de grilles qui ne subiront que les bas budgets thermiques du back-end ($T<400°C$).

Le travail de sortie dans le vide d'un métal est l'énergie minimum nécessaire pour arracher un électron depuis le niveau de Fermi du métal jusque dans le vide en dehors du métal. Lorsque le métal est déposé sur un autre matériau, ce travail de sortie peut-être modifié, il devient le travail de sortie effectif. D'une façon générale, l'expression du travail de sortie effectif d'un empilement de grille HK/MG comprend plusieurs contributions en plus du travail de sortie du MG dans le vide (Equation I-4). Ces contributions correspondent à la présence de dipôles aux interfaces HK/MG et IL/HK, de charges fixes aux interfaces Si/IL, IL/HK, de charges fixes dans le volume des oxydes HK et IL. Il a été démontré que les termes de volume peuvent être négligés devant les termes de surface. Par ailleurs, dans le contexte de l'approche « gate last », les interfaces enterrées (Si/IL, IL/HK) ne sont pas ou peu affectées par le traitement thermique basse température car la diffusion des espèces réactives activée thermiquement reste limitée. Finalement, les deux facteurs qui fixent EWF sont le travail de sortie dans le vide du métal et le décalage de tension associé à l'éventuelle formation de dipôles à l'interface HK/MG. Le choix du travail de sortie du métal dans le vide a donc une importance centrale.

Dans la classification périodique des éléments, les métaux peuvent être classés dans deux groupes en fonction de leur travail de sortie dans le vide ; les métaux à faible travail de sortie pour le côté nMOS (Ti, Al, Ta, Sc, Mg…) et les métaux à fort travail de sortie pour le côté pMOS (Co, Ni, Rh, Pd …) (TableauI-1). Les premiers sont réactifs pour la plupart et ne peuvent être utilisés qu'avec une approche faible budget thermique. Les seconds sont très stables mais incompatibles avec les procédés de gravure utilisés dans l'industrie des semi-conducteurs. Par ailleurs, ils présentent un coup d'exploitation trop élevé car ils sont peu abondants naturellement. Le comportement en température, réactif ou stable, de ces métaux a aussi été vérifié lorsqu'ils sont déposés sur SiO2 ou un oxyde (tableau I-2 et figure I-8). Dans ce cas, le travail de sortie du métal sur l'oxyde est effectivement modifié par rapport au travail dans le vide à cause de contributions extrinsèques (charges, dipoles).

Finalement, le choix des industriels ne s'est pas porté directement sur des métaux simples mais ce sont le nitrure de titane et le nitrure de tantale qui ont été les premiers métaux utilisés pour le coté pMOS à cause de leur stabilité thermique, de leur coût moins élevé que ceux des métaux nobles et de leur compatibilité avec les procédés de gravure industriels. A faible budget thermique le nitrure de titane présente un travail de sortie d'environ 4.85eV sur HfO2 modulable à 5.1eV en utilisant un procédé d'oxydation contrôlé. Récemment, parallèlement à ce travail de thèse, la modulation du travail de sortie d'une électrode HfO2/TiN afin d'obtenir

un EWF compatible avec le côté nMOS a été proposée par le dépôt d'un métal à faible travail de sortie (aluminium [Hinkle12], TiAl [Veloso11, Veloso13]) sur la couche TiN. La diffusion de l'aluminium à l'interface HfO_2/TiN a été considérée comme le mécanisme principal de l'abaissement du travail de sortie de l'empilement de grille associé. Dans le cas de l'oxyde de grille SiO_2, la modulation du travail de sortie d'un nitrure (4.1 à 5.0 eV) a aussi été réalisée en contrôlant la quantité d'azote dans une couche de TiNx [Westlinder04] ou de TiAlNx [Cha02]. Dans le début des années 2000, l'utilisation de métaux innovants a aussi été exploré avec des alliages Ta/Ni, Ti/Ni, Ta/Pt ou Ta/Ti déposés sur SiO_2. Dans ce travail de thèse (parties III à VI), nous explorons de façon systématique certaines de ces voies de façon à comprendre les mécanismes physico-chimiques sous-jacents dans le cas de HfO_2 et nous proposons d'autres alternatives.

- **Réduction de l'épaisseur d'oxyde équivalent par « remote scavenging »**

L'épaisseur d'oxyde équivalent est une longueur qui indique quelle serait l'épaisseur de silice qui aurait les mêmes propriétés que le HK utilisé pour le remplacer. La modulation de l'épaisseur d'oxyde équivalent (EOT) d'un empilement de grille HK/MG dépend essentiellement de la capacité à contrôler l'épaisseur physique de l'oxyde de plus faible permittivité, i.e. d'oxyde de silicium interfacial (SiO_2-IL), présent entre le substrat et l'oxyde de permittivité élevée. Une réduction efficace de l'EOT passe par une réduction de l'épaisseur de cet oxyde interfacial. La méthode que l'on utilise dans ce travail consiste à réduire à distance (« remote scavenging ») le SiO_2-IL par le dépôt d'un métal réactif sur l'empilement TiN/HfO_2. Cette méthode permet une réduction efficace de l'EOT avec un impact réduit sur l'EWF, la mobilité des porteurs et les courants de fuite de l'empilement de grille. La réaction chimique qui accompagne cette réduction s'appuie sur l'équation de réduction de la silice par le métal (Equation I-5). La réaction de formation de l'oxyde du métal sera favorable si l'énergie libre de formation de l'oxyde métallique est inférieure à celle de SiO_2.

Cependant, l'observation expérimentale montre des différences de comportement même pour des métaux dont les énergies libres de formation des oxydes correspondants sont proches (Ellingham, figure I-9). Par exemple, l'efficacité de la réduction à distance n'est pas équivalente pour le titane et l'aluminium.

Dans les parties III à VI de ce travail, en plus de l'énergie libre de formation d'oxyde métallique MO_x par rapport à celle du SiO_2, nous étudions d'autres paramètres

thermodynamiques qui nous aident à comprendre les mécanismes chimiques responsables de la réduction de l'EOT.

II- Outils de caractérisation nano analytiques pour l'étude de l'interdiffusion dans les empilements high-k/grille métallique

Afin de comprendre les interactions entre les différentes couches de l'empilement de grille et leur impact sur l'EWF de la grille ainsi que sur l'EOT, la caractérisation physico-chimique systématique entreprise dans ce travail a été couplée à une caractérisation électrique élémentaire capacité-tension (C(V)) effectuée sur de larges capacité MOS.

La caractérisation physico-chimique a été réalisée de manière systématique sur tous les empilements de grille étudiés en mettant en œuvre différentes techniques : (i) réflectométrie des rayons X (XRR) et MET corrigée en image afin de vérifier la qualité (épaisseur, rugosité) des couches déposées, (ii) STEM-EDX (STEM : mode balayage) et ToF-SIMS afin d'analyser la distribution des espèces chimiques au sein des couches, (iii) XPS afin d'obtenir des informations sur les environnements chimiques des différents éléments présents dans les couches.

En particulier, l'utilisation d'un MET dédié à l'analyse chimique (Tecnai Osiris) a permis de cartographier la distribution des espèces chimiques dans les empilements de grille avec une bonne résolution spatiale (environ 1 nm) tout en gardant une très bonne qualité de signal. Ceci est possible grâce à une source d'électrons de très haute brillance XFEG et à l'utilisation de 4 détecteurs SDD (Silicon Drift Detector, figure II-5). Avec un tel outil, l'analyse fine de l'interdiffusion des espèces chimiques entre les différentes couches de très faible épaisseur (de l'ordre de 2nm) constituant les empilements de grille a été rendue possible. Un autre avantage qui prend de l'importance lorsqu'on étudie des empilements contenant à la fois des éléments lourds et des éléments légers est la meilleure sensibilité de ce microscope aux éléments N et O. Un exemple d'analyse est montré à la figure II-6.

Notons que nous avons introduit au cours de ce travail de thèse une méthode simple pour évaluer l'épaisseur d'oxyde de silicium qui est présent à l'interface Si/HfO_2 (SiO_2-IL). Elle est basée sur le repérage de la position relative des profils de concentration en O et en Hf que l'on peut déduire des cartographies élémentaires EDX. Ce décalage est mis en relation avec la variation de l'épaisseur de SiO_2 observée en MET à haute résolution (HRTEM) comme illustré à la figure II-7.

Des analyses complémentaires de la distribution des espèces chimiques à l'échelle micrométrique par ToF-SIMS ont été entreprises afin d'être comparées aux résultats obtenus très localement en EDX. De plus, l'environnement chimique, i.e. liaison chimique de chaque élément constituant les empilements de grille, a été étudié par spectrométrie de photoélectrons X (XPS).

Les échantillons analysés par ToF-SIMS et XPS ont reçu une préparation spécifique qui consiste à retirer le substrat de silicium afin d'être sondé par la face arrière. Cette préparation permet de conserver un budget thermique et une oxydation des métaux de grille identique aux dispositifs analysés électriquement. De ce fait, une comparaison directe des analyses matériaux/analyse électrique C(V) a pu être effectuée dans ce travail.

L'interdiffusion des espèces chimiques dans les empilements de grille est étudiée avec une attention particulière portée sur leur impact quand à la modulation de l'EWF et la réduction de l'EOT. Cela implique de déterminer l'état chimique au niveau de l'interface HfO_2/MG pour l'EWF et d'évaluer l'épaisseur physique de la couche SiO_2-IL pour l'EOT. Ces études seront réalisées suivant une méthode d'analyse systématique allant de l'échelle submillimétrique à l'échelle nanométrique par XPS, TOF-SIMS et STEM-EDX. Le but est d'établir une corrélation entre la répartition des éléments dans l'empilement de grille, en particulier à l'interface HfO_2/métal, et les liaisons chimiques que les éléments forment entre eux avec les paramètres électriques EWF et EOT, mesurés à partir des analyses C(V). L'interprétation des résultats et les mécanismes suggérés sont basés sur des considérations thermodynamiques. La figure II-9résume l'ensemble des architectures des différents empilements de grille étudiés dans cette thèse.

III- Dépôt de métaux simples Al et Ti sur HfO_2/TiN: mécanismes de réduction de l'EOT et de modulation du EWF

A cause de son travail de sortie adapté et de sa stabilité chimique vis-à-vis de HfO_2, le TiN a été choisi comme le métal de référence pour le transistor côté pMOS à la fois pour l'intégration « gate first » et l'intégration « gate last ».

Dans cette partie, après avoir étudié le comportement chimique et électrique d'un empilement de référence HfO_2/TiN (transistor de type p), nous examinons l'effet du dépôt sur HfO_2/TiN d'un métal simple Ti puis Al. Cette étude est faite dans le cadre de l'approche « gate last » où le budget thermique est limité à 400 ° C, 30 min.

Ti et Al ont été choisis à cause de leur faible travail de sortie dans le vide adapté au côté nMOS d'un inverseur CMOS et parce que l'énergie libre de formation des oxydes de titane et d'aluminium est inférieure à celle de SiO_2 ce qui est favorable à la réduction de l'oxygène de la couche de SiO_2-IL ($\Delta G_{Al2O3} < \Delta G_{TiO} < \Delta G_{SiO2}$).

Dans un premier temps, l'analyse STEM-EDX réalisée sur l'empilement de référence HfO_2/TiN montre la nature stœchiométrique de la couche de TiN avec un ratio Ti/N=1, en particulier à l'interface HfO_2/TiN (Figure III-2). La mesure électrique C(V) est en accord avec les données bibliographiques avec un EWF=4.85eV et un EOT sub-nanométrique (0.95 nm).

Le dépôt de titane sur l'empilement de référence HfO_2/TiN induit un décalage du EWF vers la bande de conduction du silicium avec EWF=4,1 eV. Le mécanisme responsable de ce faible travail de sortie est attribué à la formation d'un TiN sous-stœchiométrique en N induit par le dépôt de Ti. Toutefois, en raison de la forte réactivité de Ti envers l'O ($\Delta G_{TiO} < \Delta G_{SiO2}$) couplé à la grande quantité d'oxygène que le Ti peut incorporer (solubilité limite élevée de l'O dans Ti, au moins 33%, figure III-7), son dépôt sur l'empilement de référence HfO_2/TiN induit une réduction totale de l'oxygène des couches SiO_2-IL et HfO_2 (STEM-EDX, figure III-5). Cette réactivité excessive écarte l'utilisation du titane comme une électrode métallique finale pour le transistor nMOS d'un inverseur CMOS.

En revanche, le dépôt d'une couche d'aluminium hétérogène en épaisseur (STEM-EDX, figure III-11) sur la référence HfO_2/TiN conduit à une électrode à faible travail de sortie effectif avec EWF=4,25 eV tout en gardant une EOT sub-nanométrique (0.93nm). Le

mécanisme principal de la chute du EWF comparé à la référence HfO_2/TiN est lié à la diffusion et la ségrégation de l'aluminium à l'interface HfO_2/TiN. De plus, cette électrode présente une grande stabilité envers l'oxygène des diélectriques SiO_2 et HfO_2 à 400 °C, ce qui permet d'éviter une réduction agressive de l'oxygène des oxydes de grille (STEM-EDX et TOF-SIMS, figure III-12 et III-14). Ceci est attribué à la faible solubilité de l'oxygène dans l'aluminium comparé au titane (binaire Al-O, figure III-17). Dans ce cas, et contrairement à ce qui a été observé pour le titane, la quantité d'oxygène consommée par le métal est dépendante de l'épaisseur de la couche d'aluminium. Nous remarquons le même comportement de l'aluminium envers l'azote qu'envers l'oxygène avec un impact de modulation de l'épaisseur sur la redistribution de l'azote entre la couche de TiN et l'aluminium ce qui permet le contrôle de la quantité d'aluminium qui diffuse vers l'interface HfO_2/TiN liée à la formation d'AlN dans le volume de la couche de TiN.

IV- Alliages de métaux à base de TiAl(N): impact de la redistribution de l'azote et de l'oxygène sur l'EWF et l'EOT

Dans cette partie, nous utilisons les connaissances acquises lors de l'étude précédente sur les électrodes élémentaires TiN/Ti et TiN/Al en explorant l'effet d'alliage de Ti avec Al. L'alliage TiAl est donc déposé sur l'empilement de référence HfO_2/TiN. Ensuite, afin de tirer parti du rôle que peut jouer l'azote dans ce type d'empilement, nous examinons le cas du dépôt direct sur HfO_2 d'un alliage ternaire $TiAlN_x$.

Le dépôt d'une couche de TiAl sur la référence HfO_2/TiN montre, à l'inverse du dépôt d'une couche de titane pur, une stabilité élevée envers la réduction de l'oxygène des diélectriques. De plus, changer l'épaisseur de la couche TiAl de 2,5 nm à 7,5 nm n'a qu'un effet mineur sur l'EOT qui est sub-nanométrique avec 0,83nm et 0,86nm mesurés respectivement. Nous montrons que cette stabilité est liée à la diminution de la solubilité de l'oxygène dans le titane à cause de l'alliage avec l'aluminium ce qui réduit la quantité d'oxygène que la couche de TiAl peut incorporer. Cette conclusion s'appuie sur l'analyse du diagramme de phase ternaire Ti-Al-O qui met en évidence la réduction du domaine d'existence de la phase de α-Ti (phase ou solubilité de l'oxygène est très élevée) pour le domaine de composition en Al étudié ici (ternaire Ti-Al-O, figure IV-8). Ceci implique une plus faible quantité de O dissoute dans la phase α-Ti et favorise une réduction contrôlée de l'oxygène du SiO_2-IL comparé à l'effet agressif d'une couche de titane pur.

Nous démontrons aussi que l'aluminium présent dans la couche TiAl n'a pas d'effet sur le EWF obtenu. EWF = 4,2 eV est adapté au côté nMOS d'un inverseur CMOS. L'Al est en fait « consommé » dans des liaisons AlN lors de sa diffusion à travers la couche TiN avant d'arriver à l'interface HfO_2/TiN. Nous expliquons que le mécanisme associé au décalage du EWF par rapport à la référence TiN est lié à la redistribution d'azote entre les couches de TiAl et TiN ce qui induit la formation d'un $TiN_{x<1}$ sous-stœchiométrique en N en contact avec le HfO_2.

Nous avons voulu exploiter davantage et de façon plus contrôlée le rôle que l'azote joue sur le EWF, voire sur l'EOT. Nous avons déposé directement une couche d'un nitrure ternaire $TiAlN_x$ sur HfO_2 en faisant varier le flux d'azote lors du dépôt. Trois flux ont été étudiés : bas ($TiAlN_{x<1}$), moyen ($TiAlN_{x>1}$), et haut flux d'azote ($TiAlN_{x>>1}$).

Nous observons que diminuer le flux d'azote réduit l'épaisseur du SiO_2-IL et de fait, réduit aussi l'EOT mesuré électriquement (HRTEM et STEM-EDX, figures IV-11 et IV-12) avec une diminution de 0.07nm entre les grilles $HfO_2/TiAlN_{x>>1}$ et $HfO_2/TiAlN_{x<1}$. En effet, la diminution du flux d'azote lors du dépôt de la couche de $TiAlN_x$ sur HfO_2 est accompagnée de l'augmentation de la concentration en titane dans le TiAlN ce qui conduit à la formation de la phase α-Ti. Sachant que α-Ti dissout l'oxygène, l'augmentation de sa quantité dans la couche de $TiAlN_x$ augmente la quantité d'oxygène de la couche de SiO_2-IL qui peut être réduite ce qui diminue l'EOT.

Nous observons aussi que la diminution du flux d'azote impacte le EWF des grilles $HfO_2/TiAlN_x$ avec une différence de 0.8eV entre la grille de $HfO_2/TiAlN_{x>>1}$ (EWF = 5.0eV) et $HfO_2/TiAlN_{x<1}$ (EWF = 4.2eV) (EWF-EOT, figure III-14). Comme dans le cas des structures de grille HfO_2/TiN/Ti ou HfO_2/TiN/TiAl, le faible EWF obtenu avec le $TiAlN_{x<1}$ est relié à la composition sous-stœchiométrique en N du TiAlN (rapport N/Ti<1) à l'interface HfO_2/TiAlN.

Dans le cas $TiAlN_{x>1}$, l'augmentation du débit d'azote par rapport à la grille $HfO_2/TiAlN_{x<1}$ modifie peu l'EWF qui augmente seulement d'environ 0.1eV (EWF = 4.3eV). Ceci est observé en dépit de la nature sur-stœchiométrique du $TiAlN_{x>1}$ avec un rapport N/Ti>1. Nous attribuons ce comportement similaire en termes de EWF à la forte solubilité de l'azote dans le titane qui garde à ce ternaire $TiAlN_{x>1}$ un caractère riche en Ti. En effet, dans le spectre XPS N1*s*, l'environnement chimique Al-N est prédominant par rapport à l'environnement Ti-N, ce qui révèle que le titane est faiblement lié à l'azote en dépit du rapport N/Ti>1 (figure IV-13). Ce comportement se comprend si une partie de l'azote est dissoute dans la phase riche en Ti, α-Ti (Fig. III-8). Par conséquent, le comportement Ti-riche du $TiAlN_x$ peux être conservé dans une large gamme de concentration d'azote ce qui permet d'obtenir un faible travail de sortie pour la grille $HfO_2/TiAlN_{x>1}$ malgré sa nature surstœchiométrique en azote.

Enfin, dans le cas de la grille $HfO_2/TiAlN_{x>>1}$ correspondant à un fort flux d'azote, on obtient un travail de sortie effectif élevé d'environ 5.0eV adapté au transistor de type p d'un inverseur CMOS. Nous montrons que deux phénomènes contribuent à cette valeur. Tout d'abord, comparé au $TiAlN_{x>1}$ déposé avec un flux d'azote moyen, le contenu beaucoup plus élevé en azote est bien visible sur les profils STEM-EDX (figure IV-12). Il s'accompagne d'un environnement prédominant Ti-N observé par XPS (figure IV-13) qui justifierait un EWF de 4,85 eV. A cette valeur s'ajoute celle associée à la formation de dipôles Hf-N qui résulteraient

de la diffusion de l'azote jusqu'à l'interface HfO_2/TiN (STEM-EDX et XPS, figures IV-12 et IV-13) [Hinkle10].

En conclusion de cette partie IV, avec un dépôt d'une couche de TiAl sur la référence HfO_2/TiN, nous obtenons un faible EWF=4.2eV adapté au transistor de type n d'un inverseur CMOS. Le mécanisme de la chute du EWF comparé à la référence HfO_2/TiN est attribué à la formation d'un $TiN_{x<1}$ sous-stœchiométrique en contact avec HfO_2. Cette électrode présente une valeur d'EOT sub-0.9nm qui reflètent l'importante réduction de l'oxygène de la couche de SiO_2-IL. Toutefois, la stabilité chimique de la grille envers l'oxygène est observée ici malgré la composition intrinsèque titane-riche de l'alliage TiAl. Cette stabilité est attribuée à l'alliage du titane avec l'aluminium qui réduit la solubilité de l'oxygène dans la couche de TiAl avec la réduction de la phase α-Ti ce qui empêche la réduction totale de l'oxygène des diélectriques SiO_2 et HfO_2. De plus, nous avons démontré que la modulation du flux d'azote pendant le dépôt d'une couche de $TiAlN_x$ directement sur HfO_2 conduit à la fois à l'obtention de travaux de sortie effectifs adaptés aux transistors de type n et de type p ce qui rend l'utilisation du $TiAlN_x$ viable pour une co-intégration n/p dans un inverseur CMOS. De plus, des EOT sub-1nm sont obtenues avec une stabilité chimique élevée pour tous les flux utilisés pour le dépôt des différents TiAlN ce qui rend ce matériau très prometteur pour une intégration CMOS au nœud technologique 20nm en utilisant l'approche bas budget thermique.

V- Stabilité thermique des empilements de grille à base de Ti et Al sur HfO_2

Dans ce chapitre, nous évaluons la stabilité thermique de l'ensemble des empilements de grilles étudiés jusqu'à présent afin d'estimer la possibilité de les intégrer en utilisant l'approche classique « gate first » ou en utilisant une intégration de type 3D pour laquelle les transistors des niveaux supérieurs doivent subir différents budgets thermiques plus élevés que le budget thermique initial de fabrication limité à 400°C, 30min. Les empilements HfO_2/TiN/Al, HfO_2/TiN/TiAl et HfO_2/ TiAlNx ont donc été soumis à des recuits de 500°C et 700°C pendant 1 min sous vide (~ 10^{-5} Pa) en utilisant un équipement de recuit rapide (RTP).

Le recuit à 500°C de l'empilement HfO_2/TiN/Al provoque la formation de zones sombres contenant du silicium, de l'aluminium et du titane dans le substrat de silicium juste en dessous de l'interface Si/SiO_2 (STEM-EDX, figure V-3). Elles ont déjà été observées dans un empilement Si/TiN/Al, recuit à 550°C [Lee99] et attribuées à la phase Al_3Ti contenant de Si dissous en solution solide (environ 20%). Dans notre cas, la couche supplémentaire de HfO_2 présente entre le substrat de silicium et la couche de TiN ne semble pas modifier la formation des domaines Al_3Ti (Si) dans le substrat ce qui suggère que la couche HfO_2 ne constitue pas une barrière à la diffusion de Al, Ti et N voire de Al_3Ti. La formation de domaines Al_3Ti dans le substrat altère donc son intégrité après recuit. Une solution possible pour améliorer la stabilité chimique de l'empilement est de modérer la diffusion d'aluminium après le recuit, soit en augmentant d'une manière raisonnable l'épaisseur du TiN ou par un dépôt d'une couche barrière afin de modérer la diffusion de l'aluminium à travers le TiN l'empêchant ainsi d'atteindre le substrat de silicium.

Contrairement à l'électrode utilisant de l'aluminium pur, le recuit de l'empilement $Si/SiO_2/HfO_2$/TiN/TiAl à 500°C révèle que le substrat de silicium n'est pas affecté par la formation d'Al_3Ti. Cependant, nous remarquons la consommation complète du SiO_2-IL comme dans le cas du Ti (HRTEM, figures III-5 et III-6). Ceci suggère que l'alliage TiAl empêche la formation d'Al_3Ti dans le substrat de silicium à des températures allant jusqu'à 500°C avec cependant une perte de la stabilité chimique de la couche de TiAl envers l'oxygène avec une réduction totale de l'oxygène du SiO_2-IL. La stabilisation envers l'oxygène acquise par alliage du titane avec l'aluminium limitée thermiquement est probablement due à une contribution plus élevée de la phase α-Ti dans la couche TiAl après

recuit permettant ainsi une plus forte dissolution de l'O par le Ti et ainsi une réduction plus importante de la couche de SiO_2-IL. L'absence de domaines Al_3Ti dans le substrat quand à elle est interprétée sur la base du maintien de l'effet barrière de la couche TiN contre la diffusion d'aluminium observé dans les empilements non recuits (STEM-EDX, figure V-7).

Par conséquent, l'accumulation d'aluminium à l'interface Si/HfO_2 nécessaire pour la formation de Al_3Ti dans le substrat de silicium n'a pas lieu. En revanche, nous montrons que si la quantité d'aluminium dans l'alliage TiAl est augmentée jusqu'à environ 50% (au lieu de ~20%) l'efficacité de la barrière de TiN contre la diffusion de l'aluminium est perdue après recuit, les domaines Al_3Ti étant formés dans le substrat de silicium (TEM, figure V-8). De la même façon, nous montrons que l'efficacité de l'effet barrière de la couche de TiN contre la diffusion d'aluminium est perdue après recuit à 700°C, 1 min de HfO_2/TiN/TiAl (Al ~20%) (TEM, figure V-9). Comme indiqué dans les chapitres III et IV, l'effet barrière de la couche TiN contre la diffusion d'aluminium fonctionne à travers la formation d'AIN pendant la diffusion d'aluminium couplé à la réduction d'azote du TiN par la couche de TiAl. Par conséquent, plus faible est la quantité d'azote dans la couche de TiN, plus la diffusion de l'aluminium est élevée. Nous supposons que le recuit à 700 °C active une réduction d'azote plus élevée par la couche de TiAl résultant en une couche TiN très pauvre en azote ce qui favorise la défaillance de la barrière TiN contre la diffusion d'aluminium. Pour conclure, contrôler la réduction agressive de l'oxygène des couches de diélectrique et étendre la stabilité thermique de l'empilement HfO_2/TiN/TiAl au-dessus de 500 °C suppose de trouver les bonnes proportions d'aluminium et de titane afin de contrôler la réduction d'oxygène des couches de diélectriques tout en évitant une diffusion importante de l'aluminium à travers l'empilement HfO_2/TiN. D'après les résultats précédents, on peut estimer que ce compromis correspond à une quantité d'aluminium comprise entre 30 et 50%.

Dans le cas des empilements de grille $HfO_2/TiAlN_x$, les couches de $TiAlN_x$ deposées à faible et moyen flux d'azote sont instables chimiquement après le recuit à 500°C et non mesurables électriquement. Seul l'empilement $TiAlN_{x>>1}$ déposé avec un fort flux d'azote est mesurable et il ne se forme pas d'Al_3Ti. On observe une chute de l'EWF de la grille allant de 5.0eV a 4.76eV après recuit à 500°C et l'EOT croit fortement. La chute du travail de sortie peut être liée à une plus faible diffusion de l'azote à l'interface $HfO_2/TiAlN_x$ (STEM-EDX, figure V-12) qui conduit probablement à une contribution minorée des liaisons Hf-N après recuit. En même temps, le ratio N/Ti qui décroit sensiblement à l'interface HfO_2/TiAlNx peut être une autre cause de la diminution du EWF de la grille. Enfin, l'augmentation de l'EOT est

probablement liée à la diffusion de l'oxygène stocké dans la couche supérieure de TiN due à des étapes de mise à l'air dans le procédé de fabrication.

Pour conclure, les empilements de grilles étudiés jusqu'à présent sont instables thermiquement pour différentes raisons résumées ici:

- la dégradation du substrat induite par la formation d'Al_3Ti (bas-N $TiAlN_{x<1}$, TiN/Al et TiN/TiAl (Al~50%) à 500°C et TiN/TiAl (Al~20%)) à 700° C) ;
- la réduction complète de l'oxygène du SiO_2-IL (TiN/TiAl (Al~20%)) ;
- la dégradation significative de l'EOT.

Nous proposons quelques solutions pour tenter d'obtenir une stabilité thermique plus élevée pour chaque empilement :

- HfO_2/TiN/Al: dépôt d'un TiN plus épais ou d'une barrière de diffusion à l'aluminium ;
- HfO_2/TiN/TiAl: optimisation de la quantité d'aluminium dans la couche de TiAl (30% <Al <50%) pour augmenter la stabilité contre la réduction de l'oxygène tout en gardant une faible diffusion de l'aluminium à travers l'empilement HfO_2/TiN et préserver le substrat de silicium;
- $HfO_2/TiAlN_x$: trouver une barrière efficace contre la diffusion de l'oxygène lors de la mise à l'air afin préserver une EOT faible.

VI- Métaux de grille innovants

Dans les chapitres précédents, nous avons montré qu'à faible budget thermique (T=400°C), les empilements HfO_2/TiN/TiAl (Al ~20%) et HfO_2 /TiAlNx sont intégrables en tant qu'électrodes de grilles en utilisant l'approche « gate last ». Toutefois, leur stabilité chimique et thermique est compromise après un recuit à T=500 ° C. Dans ce paragraphe, nous recherchons des métaux innovants stables pour un budget thermique modéré correspondant à un recuit de 1 minute à 500°C ou 600°C.

Pour le côté nMOS, nous considérons le Ta à cause de son faible travail de sortie (dans le vide = 4.25eV) et en même temps sa stabilité vis-à-vis de l'oxygène du SiO_2-IL (Ellingham, figure I-9). Pour le côté pMOS, nous considérons le Ni qui est bien connu de l'industrie des semi-conducteurs puisque déjà utilisé pour la formation de siliciure dans les S/D et le poly-Si. Son coût est nettement inférieur à celui des métaux précieux et il présente la même stabilité chimique élevée envers l'oxygène. Nous proposons donc d'étudier l'empilement HfO_2/TaN/Ta afin d'obtenir un faible EWF de type n similaire aux électrodes de HfO_2 /TiN/Al, Ti ou TiAl. Puis, nous étudierons l'alliage de nickel à fort travail de sortie avec des métaux à faible travail de sortie Ta et Ti.

L'empilement HfO_2/TaN/Ta conduit à un faible travail de sortie d'environ 4.3eV avec un EOT d'environ 0.9nm. Le mécanisme du décalage de travail de sortie par rapport à la référence HfO_2/TaN mesurée à EWF=4.6eV est lié à la formation d'un TaN_x sous-stœchiométrique à cause de la redistribution de l'azote entre TaN et Ta. Ce mécanisme est similaire à celui observé précédemment avec les empilements HfO_2/TiN/Ti (TiAl)/TiN. La grande stabilité thermique de Ta envers la silice interfaciale est également démontrée en plus de la grande efficacité du TaN à agir comme une barrière contre la diffusion de l'oxygène provenant de la mise à l'air entre les couches de TaN-cap et TiN-cap. Cependant, une co-intégration HfO_2/TaN et HfO_2/TaN/Ta n'est pas possible à cause du travail de sortie effectif de l'empilement HfO_2/TaN mesuré à 4.6eV (milieu de la bande interdite du silicium).

Dans le cas de l'empilement HfO_2/Ta/Ni, nous démontrons que la formation d'un alliage Ni riche Ni_3Ta a permis d'augmenter le travail de sortie effectif d'environ 0.4eV à 4.75eV en comparaison avec la référence HfO_2/Ta mesuré à 4.35eV. Notons qu'on a inversé ici l'ordre du dépôt des métaux en commençant par le métal n (Ta) qui sert de grille de référence puis en déposant un métal de type p (Ni). Ces valeurs de EWF sont compatibles pour une intégration

« dual gate » dans une technologie de type FDSOI. De plus, la stabilité chimique du Ta envers l'oxygène a permis la conservation d'une EOT et d'un EWF stable après le recuit à 500°C, 1min. Dans le cas de l'alliage de Ni avec Ti, on revient à une intégration p-first, HfO_2/Ni représentant l'empilement de grille de référence avec un EWF mesuré de 5.0eV environ. L'alliage de Ni avec Ti dans l'empilement HfO_2/Ni/Ti induit une chute importante du travail de sortie effectif de l'empilement avec EWF=4.2eV, soit une séparation nMOS-pMOS d'environ 0.8eV. Cette séparation est maintenue après recuit à 500°C témoignant de la stabilité thermique et chimique de cette grille.

Conclusion

Au-delà du nœud technologique CMOS 65nm, le remplacement de l'empilement de grille historique SiO_2/poly-Si par la structure HK/MG a été l'un des défis les plus importants de l'industrie des semi-conducteurs. Ce changement important de la composition chimique des matériaux de grille a poussé la communauté scientifique à entreprendre des études approfondies concernant la stabilité des métaux sur les oxydes à permittivité élevée (HK) avec la recherche de métaux adaptés en terme de travail de sortie dans le vide (WF) aux deux types de transistors n et p constituant un inverseur CMOS. En parallèle, différentes intégrations ont été développées afin d'obtenir des électrodes stable chimiquement tout en ayant un travail de sortie effectif (EWF) adapté. Le schéma d'intégration « gate last » a été choisi comme une alternative à la classique intégration « gate first » grâce à son faible budget thermique global qui permet de mieux contrôler l'interdiffusion des espèces chimiques et les différentes réactions entre les couches des empilements de grilles. Cette approche permet une meilleure modulation du travail de sortie effectif des électrodes de grille tout en gardant une bonne stabilité du métal envers les diélectriques, permettant ainsi une réduction contrôlée de l'épaisseur d'oxyde équivalent (EOT). Pour les technologies CMOS sub-20nm planaire, en raison de la réduction agressive de la taille des grilles, des couches métalliques très minces doivent être déposées afin d'avoir une électrode de grille présentant un remplissage optimal du contact métallique tout en gardant un EWF approprié pour les deux côtés n et pMOS ainsi qu'une réduction efficace de l'EOT (<0.9nm selon la feuille de route de l'ITRS pour les nœuds sub-20nm planaires).

Dans un contexte industriel, à savoir l'intégration CMOS 20-14nm avec intégration à faible budget thermique, l'objectif de ce travail de thèse a été de mettre en évidence les paramètres clés qui permettent le contrôle du travail de sortie effectif d'une électrode de grille ainsi que la réduction efficace mais contrôlée de l'EOT. Pour atteindre cet objectif, des études structurales et analytiques ont été menées de manière systématique sur des empilements de grille d'épaisseurs nanométrique déposés sur des plaquettes 200 ou 300mm sans motifs. En parallèle, des mesures électriques ont été effectuées sur des plaquettes 200 ou 300mm contenant des capacités MOS large afin de déterminer les deux paramètres clef étudiés dans ce travail, à savoir le EWF et l'EOT. Par la suite, la corrélation entre les analyses matériaux et les mesures électriques a été discutée sur la base de considérations thermodynamiques. Avant d'étudier les différents empilements de grille, il a été démontré que, dans le cadre de

l'intégration « gate last », i.e. à bas budget thermique : (i) le travail de sortie effectif est principalement dépendant de l'état chimique de la grille métallique à l'interface HK/MG, (ii) la diminution de l'EOT se fait par un mécanisme de réduction à distance de l'oxygène de la couche de silice et le niveau de réduction de l'oxygène par le métal de grille dépend de l'énergie libre de la formation de l'oxyde du métal par rapport à celle du SiO_2. En raison de la très petite taille des empilements de grille (quelques nanomètres), des caractérisations matériaux très localisées basées sur la microscopie électronique à transmission (MET) ont été mises en œuvre dans ce travail. Les analyses structurales et chimiques ont été faites de manière systématique en utilisant la microscopie haute résolution TEM (HRTEM) et l'analyse dispersive en énergie des rayons X (ou à moindre mesure, de la spectroscopie de perte d'énergie d'électrons, EELS). Pour cela, des microscopes de dernière génération ont été utilisés afin de fournir des images et des cartographies chimiques à partir desquelles une description fine et approfondie de l'organisation structurale et chimique dans les empilements de grille a pu être proposé. Les profils élémentaires STEM-EDX sont utiles pour fournir des informations semi-quantitative de la répartition spatiale des éléments dans les empilements de grille allant du substrat de silicium jusqu'au contact métallique supérieur. Les études analytiques locales ont été complétées systématiquement par une étude des liaisons établie pour chaque espèce chimique dans l'empilement de grille en utilisant de la spectroscopie de photoelectron X (XPS). Cette analyse XPS a été réalisée par la face arrière sur des échantillons ayant reçu une préparation spécifique. Cette préparation d'échantillon spécifique a également été bénéfique pour les analyses TOF-SIMS nécessaire pour fournir des informations moyennées particulièrement dans le cas des empilements contenant des couches hétérogènes. Cette méthodologie de travail nous a permis (i) de fournir une comparaison fiable entre les différents matériaux étudiés et (ii) d'interpréter avec confiance les résultats obtenus à partir de mesures électriques C(V) sur capacité MOS. Pour interpréter les résultats et suggérer des mécanismes réactionnels, nous avons souvent basé nos discussions sur des concepts thermodynamiques incluant les énergies libres de formation, la solubilité solide et les diagrammes de phase.

Dans ce travail, nous avons étudié différents matériaux métalliques déposés sur HfO_2 afin d'évaluer la contrôlabilité du travail de sortie effectif et le niveau de réduction de l'EOT pour les empilements de gille correspondants. Tout d'abord, nous avons suivi une stratégie classique où un métal type n (métal réactif) est déposé sur un métal de type p (HfO_2/TiN, EWF = 4.85eV) afin d'obtenir une grille nMOS avec un faible travail de sortie effectif. Après

avoir étudié séparément le comportement des métaux à bas WF Ti et Al déposés sur TiN, nous avons étudié l'effet de l'alliage de Ti avec Al. En particulier, nous avons montré que le travail de sortie effectif obtenu avec les deux empilements TiN/Ti et TiN/Al déposés sur HfO_2 était lié à deux mécanismes différents: la formation d'un TiN_x sous-stœchiométrique pour l'empilement TiN/Ti et la diffusion et ségrégation de l'aluminium à l'interface HfO_2/TiN pour l'empilement TiN/Al. Les différents comportements de Ti et Al envers la réduction de l'oxygène de la couche de SiO_2-IL sont principalement liés à la différence de la solubilité limite de l'oxygène dans ces deux matériaux (Al, proche de 0% à 400°C et Ti, 40% à 400 °C) malgré des énergies libres de formation d'oxyde métallique très proches (Al_2O_3 ou TiO). En effet, la réduction agressive et totale de l'oxygène des diélectriques SiO_2 et HfO_2 est observée pour l'électrode TiN/Ti où Ti peut absorber une grande quantité d'oxygène alors qu'une légère réduction de celui-ci est observé pour l'électrode TiN/Al liée à la faible quantité d'oxygène que l'aluminium peux absorber dans son volume. Pour l'empilement TiN/TiAl, un faible travail de sortie effectif est obtenu. Il est lié à la formation d'un TiN sous-stœchiométrique induit par une réduction d'azote par la couche de TiAl. La stabilité chimique plus élevée de l'empilement TiN/TiAl par rapport à TiN/Ti est le résultat de la réduction de la solubilité solide de O dans la couche TiAl due à l'alliage de Al avec Ti. Finalement, un faible travail de sortie effectif adapté au côté nMOS avec EWF = 4.25eV et une faible EOT = 0.83nm ont été obtenus pour l'électrode TiN/TiAl. Ces investigations ont montré que les interactions des différentes couches d'un empilement de grille, en particulier celles liée à l'azote et à l'oxygène, sont des paramètres clefs pour la modulation du travail de sortie effectif et le contrôle de l'EOT pour les empilements HfO_2/TiN/métal. Basé sur ces connaissances, nous avons déposé des couches TiAlNx directement sur HfO_2 en modulant le débit d'azote afin d'avoir un meilleur contrôle du travail de sortie effectif et de l'EOT. Nous avons démontré, pour la première fois sur HfO_2, un écart de EWF de 0.8eV avec des EOT sub-nanométriques pour un métal ternaire $TiAlN_x$ en faisant varier la concentration en N de $TiAlN_{x<1}$ (EWF = 4.2eV) à $TiAlN_{x>1}$ (EWF = 5.0eV). La stabilité thermique des électrodes ci-dessus a été évaluée afin de donner un aperçu de leur intégrabilité utilisant un budget thermique plus élevé (intégration « gate first » ou 3D). On a observé que, dès le premier recuit à T=500 ° C, ces électrodes de grille perdent leur stabilité chimique avec formation d'Al_3Ti dans le substrat de Si. Ce phénomène a été observé pour les empilements TiN /Al, Ti N/TiAl (50%), et les $TiAlN_x$ déposés à faible et moyen flux d'azote. L'empilement TiN/TiAl (Al ~20%) est stable envers le substrat de silicium (pas de formation de Al_3Ti) mais perd sa stabilité envers l'oxygène avec une réduction agressive du SiO_2-IL. Une dégradation

significative de l'EOT et une chute du travail de sortie effectif est observée pour l'empilement $HfO_2/TiAlN_{x>>1}$. Afin de trouver des alternatives aux électrodes à base de TiAl (N) instable thermiquement, nous avons cherché d'autres matériaux de grille innovants plus stables à plus haut budget thermique. Nous avons d'abord étudié le tantale, un matériau plus stable que le titane envers l'oxygène. De même que pour l'empilement TiN/Ti, l'électrode à base de TaN/Ta a été étudiée pour un budget thermique allant de 400°C à 600°C. L'électrode est stable thermiquement avec une très faible évolution du travail de sortie effectif et de l'EOT après recuit. Le même mécanisme du décalage du travail de sortie effectif a été mis en évidence pour l'empilement TaN/Ta que pour les empilements TiN/Ti ou TiN/TiAl avec la formation TaN_x sous-stœchiométrique à faible travail de sortie. La comparaison des différentes propriétés thermodynamiques de Ta, Ti et Al nous a permis de définir plusieurs comportements vis-à-vis de la réduction d'oxygène du SiO_2-IL. Au premier ordre, la variation d'énergie libre (ΔG) associée à la formation de l'oxyde du métal MO_X par rapport à l'énergie de formation du SiO_2 détermine si le métal est capable de réduire l'oxygène du diélectrique ou non. Au second ordre vient le concept de solubilité solide de l'oxygène dans le métal. On peut résumer ces différents comportements selon :

• $\Delta G < 0$ et forte solubilité de l'oxygène dans le métal M : le niveau de réduction de l'oxygène est indépendant de l'épaisseur de la couche de métal M (typiquement de cas Ti) ;

• $\Delta G < 0$ et faible solubilité de l'oxygène dans le métal M : le niveau de réduction de l'oxygène est dépendant de l'épaisseur de la couche de métal M (Al typiquement cas).

D'autres options ont été étudiées dans ce travail afin d'obtenir des électrodes de grille ayant une meilleure stabilité thermique et chimique. Grâce à la grande stabilité chimique du tantale envers l'oxygène et à son faible travail de sortie dans le vide (4.25eV), une intégration métal n-first sur HfO_2 a été étudiée. Cette intégration consiste à déposer sur le métal de type n un autre métal à fort travail de sortie dans le vide (ex Ni) afin d'obtenir une grille de type pMOS. Nous avons démontré que l'alliage de Ni avec Ta induisait la formation d'un alliage métallique Ni-riche Ni_3Ta. Il en résulte un travail de sortie effectif de 4.75eV avec $\Delta EWF = +0.4eV$ comparé à la référence HfO_2/Ta associée à une EOT sub-1 nm. Cette différence de travail de sortie effectif des empilements n et p est adaptée pour une intégration CMOS « dual gate » utilisant la technologie FDSOI. Une autre approche proposée dans ce travail consiste à allier le nickel (métal stable) avec du titane (métal réactif) avec une intégration p-first utilisant le dépôt de nickel en premier sur HfO_2 suivi d'un dépôt de titane. Nous avons montré que l'alliage de Ni avec Ti baisse significativement le travail sortie effectif de l'empilement de grille HfO_2/Ni/Ti avec $\Delta EWF = -0.8eV$ par rapport à la référence HfO_2/Ni mesuré à EWF =

5.0eV. Nous avons également démontré la grande stabilité de l'empilement HfO_2/Ni/Ti envers l'oxygène pour le budget thermique initial à 400°C mais aussi après le recuit additionnel à 500°C. Cette stabilité est induite par l'alliage de Ti avec Ni, ce qui réduit la solubilité de l'oxygène dans le titane et donc entraîne une réduction contrôlée de l'oxygène de la couche de SiO_2-IL.

Afin d'avoir une réponse fiable sur la stabilité thermique et chimique de ces matériaux, une intégration dans des dispositifs transistors finaux doit être envisagée. En ce qui concerne les premiers résultats recueillis dans ce travail de thèse, nous pouvons suggérer l'augmentation de la concentration d'aluminium dans la couche de TiAl (30% < [Al] <50%) associée à une optimisation de l'épaisseur du TiN pour une stabilité chimique et thermique plus élevée. Comme alternative, nous pensons que Ta/Ni est une solution fiable pour remplacer des électrodes à base de TiN. Cependant, un dépôt in-situ de Ta et de Ni doit être effectué pour éviter la diffusion de l'oxygène lors des mises à l'air entre le dépôt de différents métaux de grille, ce qui peut contribuer à garder une EOT stable. Les épaisseurs de Ta et Ni doivent être optimisées afin d'obtenir le travail de sortie effectif visé.

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To continue CMOS scaling, the HfO_2/metal gate stack replaced the historical SiO_2/PolySi gate stack. But the uncontrolled interdiffusion and reactivities of the new gate materials integrated with the classical high thermal budget approach appear to be a roadblock to reach the effective work function (EWF) and equivalent oxide thickness (EOT) ITRS targets. One solution consisted in implementing an approach with a lower thermal budget. Using this new approach, the aim of this thesis work was to understand the physical mechanisms, which enable to reach an EOT<1nm and an EWF relevant for nMOS and pMOS co-integration as required for the next 20-14nm CMOS nodes. Using spatially resolved TEM/EDX analyses and macroscopic TOF-SIMS and XPS techniques, elemental distributions and chemical bonds across nanometric-sized stacks were discussed and, based on thermodynamic considerations, correlated with the measured EWF and EOT. We showed for the first time that the modulation of nitrogen during TiAlN deposition on HfO_2 results in a ~0.8eV EWF shift between the N-poor and N-rich HfO_2/$TiAlN_x$ electrodes. The TiAlN complex system was understood after the identification of the EWF and EOT modulation mechanisms in the simple gate stacks TiN/Ti, Al or TiAl. Although $TiAlN_x$ electrodes define the best compromise for a variable EWF with a sub-nm EOT, it exhibits a low thermal stability. Therefore, we investigated two simpler metallic and stable systems using $TaNi_x$ and $NiTi_x$ alloys resulting from thermally assisted Ni-Ta and Ni-Ti interdiffusion in HfO_2/Ta/Ni and HfO_2/Ni/Ti stacks, respectively. These Ni-based electrodes are shown to be promising for a low thermal budget CMOS co-integration.

Keywords: Gate stack, gate last, TiAlN, TiAl, Al, Ti, TaN, Ta, Ni, HfO2, STEM/EDX, XPS, interfaces, thermodynamics, interdiffusion, alloys, EOT, EWF, Remote Scavenging

Afin de poursuivre la miniaturisation des dispositifs CMOS, l'empilement HfO_2/Métal a remplacé l'empilement SiO_2/polySi. Cependant, la diffusion incontrôlée des espèces chimiques dans ces nouveaux empilements fabriqués avec un fort budget thermique compromet l'obtention des travaux de sortie (EWF) et des épaisseurs d'oxyde équivalent (EOT) définis par l'ITRS. Une solution consiste à utiliser une intégration à plus bas budget thermique. Avec cette nouvelle approche, l'objectif de ce travail de thèse était de comprendre les paramètres physiques permettant d'obtenir une EOT<1nm et des EWF permettant une co-intégration nMOS et pMOS pour des nœuds futurs CMOS 20-14 nm. En nous appuyant sur différents méthodes d'analyse physico-chimique (STEM EDX, TOF-SIMS et XPS), la distribution spatiale des éléments et leurs liaisons chimiques au sein d'empilements de taille nanométrique ont été discutées et, sur la base de considérations thermodynamiques, corrélées aux valeurs mesurées de l'EOT et EWF. Nous avons démontré pour la première fois un écart de ~0.8eV entre une électrode $TiAlN_x$ déficitaire et riche en azote, déposée sur HfO_2. Ces résultats ont été obtenus après avoir identifié les mécanismes qui contrôlent l'EWF et l'EOT dans des empilements plus simples TiN/Ti, Al et TiAl. Les grilles HfO_2/$TiAlN_x$ ne sont cependant pas stables thermiquement. Nous avons alors proposé deux systèmes métalliques plus simples et plus stables utilisant des alliages $TaNi_x$ et $NiTi_x$ obtenus par interdiffusion dans les empilements HfO_2/Ta/Ni et de HfO_2/Ni/Ti. Ces structures de grilles à base de Ni apparaissent prometteuses pour une co-intégration CMOS à bas budget thermique.

Mots clef: Empilements de grilles, gate last, TiAlN, TiAl, Al, Ti, TaN, Ta, Ni, HfO_2, STEM/EDX, XPS, interfaces, thermodynamique, interdiffusion, alliages, EOT, EWF, Remote Scavenging