Defects Engineering in Heteroepitaxial Growth of Ge-on-Si: Porous Germanium-based Virtual Substrates for High-Efficiency Photovoltaic Devices

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UNIVERSITÉ DE SHERBROOKE
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Ingénierie de défauts liés à l'hétéroépitaxie de Ge sur Si: Substrats virtuels à base de germanium poreux pour le photovoltaïque

Thèse de doctorat
Spécialité : Génie électrique

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Rien au monde ne peut remplacer la persévérance,
ni l'instruction, ni le talent, ni le génie.

Ray Kroc

RÉSUMÉ

L'électricité d'origine photovoltaïque constituera une composante majeure des apports énergétiques domestiques dans les prochaines décennies. Aujourd'hui et malgré des rendements records, le coût des cellules solaires à base de matériau III-V sur germanium (Ge) est toujours trop dispendieux pour démocratiser cette technologie au niveau grand public. Le prix du substrat de Ge s'élève à plus de 50 % du prix de la cellule au complet alors que moins de 1% du substrat de Ge constitue la zone active du composant où le courant est généré. Une alternative serait donc d'intégrer une couche épitaxiale de Ge sur un support mécanique ou un substrat semi-conducteur à faible coût comme le silicium. Cependant, l'épitaxie de Ge sur substrat de Si présente des barrières physiques et technologiques. Le fort désaccord en paramètre de maille (4,2%) engendre des dislocations et contribuent majoritairement à dégrader le rendement des cellules. Dans le cadre de cette thèse, nous avons développé de nouvelles architectures de substrat virtuels de germanium-sur-silicium à base de porosification électrochimique. Les dislocations sont éliminées de la couche épitaxiale par un procédé de nano structuration thermo-électrochimique, permettant de créer une barrière de nano-cavités qui piège les dislocations. Le procédé de fabrication de ces substrats virtuels répond aux critères industriels : Monocristallins en surface, exempts de défauts, epi-ready et réalisés sur des substrats de grande taille par un procédé faible coût. La densité de dislocations moyenne est réduite de plus de trois ordres de grandeur, de ~ 10^7 cm^{-2} à ~ 10^4 cm^{-2} pour des couches de Ge de 1,5 μm d'épaisseur, ce qui est considéré comme très faible pour une couche épitaxiale aussi mince.

L'utilisation de ces procédés simples, par anodisation électrochimique et recuit thermique adéquat, s'est révélée très efficace et innovante permettant de réduire significativement le coût des cellules photovoltaïques à base de matériau III-V sur substrat silicium, ainsi que leurs intégrations probables dans le marché grand public.

Mots-clés: Germanium méso-poreux, Électrochimie des semi-conducteurs, Dislocations / cavités, Substrats virtuels, Hétéroépitaxie, Cellules photovoltaïques.

ABSTRACT

Today's photovoltaics market is dominated by silicon-based technology, as it is inexpensive and mature. Solar cells (SCs) based on III-V compound semiconductors have attained the highest reported efficiency of any photovoltaic devices to date. However, the high cost for producing these cells is limiting their use to concentrated photovoltaic (CPV) space applications. The market demand will be higher if the cost of III-V solar cells was reduced and adapted for low-concentration applications. The major contribution in the cost for III-V SCs scaled up to high volume manufacturing is associated with the cost of the substrate. This could substantially be reduced, if a Ge/Si substrate were used, especially that Ge offers advantages in strength and cost over GaAs substrates while providing a similar lattice constant. However, the integration of these lattice-mismatched materials (Ge/Si) remains difficult and presents physical and technological challenges. Threading dislocations introduced inside the germanium layers have a detrimental effect on device performances. In this research, we seek to accommodate the effects of the lattice mismatch by introducing a voided germanium interface layer (porous Ge layer) on the silicon substrate to intercept dislocations and prevent them from reaching the active layers of the device. The nanovoids are formed by a scalable process, through dislocation-selective electrochemical deep etching and thermal annealing, which leads to the formation of a continuous Ge layer, in which, a large portion of the original threading dislocations are pinned and annihilated close to a free surface. The fabrication process of these virtual substrates meets the industrial criteria: Monocrystalline on the surface, defect-fee, epi-ready and obtained at the wafer scale by a low cost process. The averaged threading dislocation density is reduced by over three orders of magnitude, from ~10^7 cm^{-2} to ~10^4 cm^{-2} for 1.5 µm thick Ge layers, which is considered very low for such a thin epitaxial layer. Our technique may be applied to realize virtual substrates for multi-junctions solar cells on a Si support. As a result, significant cost savings become possible if the bulk Ge substrates can be replaced with our virtual analogs consisting of micron-thick Ge buffers grown on Si wafers.

Keywords: Porous germanium, Electrochemistry of Semiconductors, Dislocations / voids, Virtual Substrates, Heteroepitaxy, Multi-junction solar cells.

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Acronyme	Définition
AFM	Microscopie à force atomique ou *atomic force microscopy*
BEE	Bipolar Electrochemical Etching
CBE	Épitaxie par faisceaux chimiques ou *chemical beam epitaxy*
CL	Cathodoluminescence
CMP	Chemical-mechanical planarization
CPV	Photovoltaïque concentré ou *concentrated photovoltaic*
EPD	Etch Pit Density
FF	Facteur de forme
FTIR	Infrarouge à transformée de Fourier ou *Fourier transform infrared*
FWHM	Largeur à mi-hauteur ou *full width half maximum*
LEPECVD	Low-energy plasma-enhanced chemical vapour deposition
LM	Lattice mismatch
LPCVD	Low pressure *Chemical Vapor Deposition*
MACE	Metal-Assisted Chemical Etching
MBE	Épitaxie par faisceaux moléculaires ou *molecular beam epitaxy*
MJ	Multi-jonction
MJSC	*Multi-junction solar cell*
MM	Metamorphic
MOCVD	Déposition chimique métalorganique de vapeur ou *metalorganic chemical vapor deposition*
PV	Photovoltaïque
RMS	Root mean square
RTA	Recuit thermique rapide ou *Rapid Thermal Annealing*
RTCVD	*Rapid Thermal Chemical Vapor Deposition*
SEM	Scanning electron microscope
STEM	Scanning transmission electron microscopy
TDD	Threading Dislocation Density
TEM	transmission electron microscopy
UHVCVD	*Ultra-High Vacuum Chemical Vapor Deposition*
XRD	*X-ray diffraction*

CHAPITRE I INTRODUCTION

L'humanité ne cesse d'accroître sa consommation d'énergie pour répondre à la complexification des sociétés particulièrement depuis l'avènement de l’ère industrielle. La conquête de toutes les ressources disponibles est donc une nécessité absolue pour y répondre et maintenir une qualité de vie pour chacun. Le solaire est une source intarissable d’énergie qui nous parvient à chaque instant sous forme de lumière. Pourtant, de toutes les formes d’énergie disponibles, la part occupée par cette source d’énergie est demeurée à ce jour insignifiante.

Les principales technologies solaires se basent sur deux propriétés des ondes électromagnétiques : la chaleur et la lumière. Différentes technologies sont associées à cette source d’énergie : le solaire thermique, le solaire thermodynamique et le solaire photovoltaïque. Ce dernier, qui consiste à exploiter la lumière du soleil pour la convertir en électricité, est probablement la forme d’énergie solaire la plus connue. Toutefois, le rayonnement solaire est une source d'énergie largement réparties à la fois en termes de distance géographique, nécessitant de gros collecteurs, coûteux, et en termes de gamme de longueurs d'onde. En plus, les cellules photovoltaïques utilisant cette technologie présentent de faibles rendements et un coût inadéquat en comparaison avec celles offertes par toutes les autres technologies déployées actuellement. Malgré cela, cette solution, en symbiose avec l’environnement, reste pertinente pour atteindre notamment une autonomie énergétique lorsque le réseau de distribution est hors de portée.

Depuis trois décennies, des efforts continus ont été fournis pour trouver des moyens de réduire le ratio coût-efficacité des cellules photovoltaïques [1]. En ce qui concerne l'efficacité seulement, les cellules solaires multi jonctions (MJSCs) sont conçues avec une technologie bien connue basée sur la superposition des différentes jonctions P/N. Ces cellules sont formées par des semi-conducteurs de bande interdite croissante, à partir de la bande interdite la plus faible de la cellule inférieure à la cellule supérieure ayant la plus courte longueur d'onde d'absorption. La lumière incidente est automatiquement filtrée lors de son passage à travers cet empilement [2]. Les jonctions tunnel p+/n+ sont utilisés pour fournir une faible résistance électrique et des connexions optiques à faible perte entre deux sous cellules. Cela permet une meilleure collecte des photo-porteurs du spectre solaire. La limites théoriques d'efficacité étant 34/37% (Shockley-Queisser) [3-4], 42/55%, 49/63%, 53/68%, et de 68/86% respectivement pour 1, 2, 3, 4 et un nombre infini de jonctions P/N à concentration 46 000x soleils.

Une feuille de route basée sur le nombre de jonctions se heurte rapidement avec l'augmentation des coûts de fabrication et de la complexité de ces empilements épitaxiaux. Afin de couvrir la partie infrarouge du spectre solaire avec une cellule inférieure (bottom cell) et de réduire la densité de défauts, le désaccord de maille (LM), des empilements épitaxiales métamorphiques (MM) ont été fabriqués historiquement sur GaAs, Ge et InP et même sur des substrats de GaSb. La contrepartie d'une telle stratégie est l'augmentation du coût du substrat III-V. En 2016, les records d'efficacité étaient 28,8% (1J, Alta Devices), 31,1%/34,1% $^{(467x)}$ (2J, NRE), 37,9%/44,4% $^{(302x)}$ (3J, Sharp), 43,5% $^{(418x)}$ /44% $^{(947x)}$ (3J, Solar Junction), 43,6% $^{(319x)}$ (4J, Wafer Bounding, Soitec), et 38,8% (5J, Boeing Spectrolab). En 2018, le record d'efficacité mondial est de 46,1 % $^{(312x)}$ (Fraunhofer ISE) [5-8].

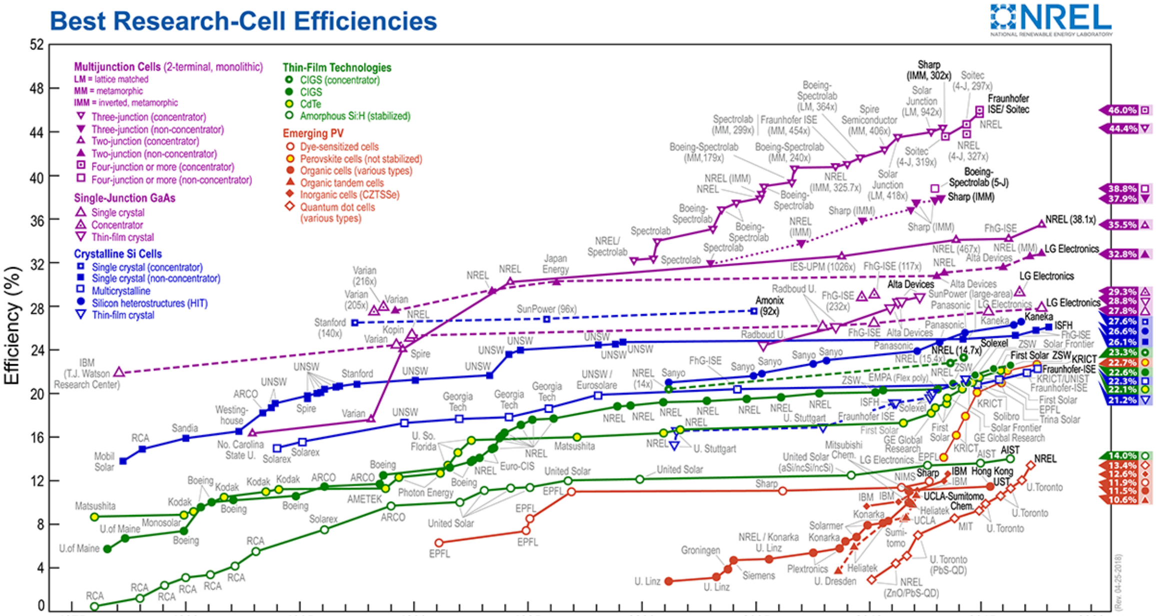


Figure I 1: Rendements records des cellules solaires depuis 1975 compilées par NREL [9].

Par conséquent le Ge semble être le substrat de choix, en particulier pour les cellules LM-InGaP/InGaAs/Ge MJSCs conçues avec une jonction supplémentaire de GaInAsNSb entre InGaAs et Ge pour une meilleure efficacité. La principale difficulté dans la réalisation de ce type de structure est la croissance de couches tampons entre le Ge et le GaInAs pour réduire les effets de dislocations. Les contraintes apparaissent au début de la croissance. En plus, moins de 5 µm d'épaisseur de substrat de Ge sont suffisants pour générer autant de courant excédentaire de la cellule du bas de Ge. Le reste du substrat de Ge engendre une résistance en série ainsi que des pertes dues aux recombinaisons volumiques [10]. De plus, le prix du substrat de Ge s'élève à 50% du prix de la cellule complète [11]. L'idée est donc d'intégrer une couche mince de Ge sur un support moins couteux. Le silicium apparait comme une plateforme idéale à cause de son prix compétitif et sa compatibilité avec les procédés micro-optoélectroniques.

Néanmoins, en raison d'un désaccord de paramètre de maille entre Si et Ge de 4,2%, l'apparition d'une contrainte mécanique est inévitable dans les couches de Ge épitaxiées sur Si. Cette contrainte sera soit stockée comme énergie de déformation dans la couche ou logée par un réseau de dislocations *(misfit)* à l'interface [9-10]. Cette génération de contrainte est accompagnée par une forte densité de dislocations > 10^9 cm^{-2} [14], qui se propagent à la surface de Ge et abaisse les performances des dispositifs optoélectroniques et microélectroniques [12-13].

Dans ce contexte, de nombreuses approches ont été explorées pour résoudre le problème de fabrication des couches relaxées de Ge/Si, ayant une haute qualité morphologique, structurelle en termes de taux de relaxation et une densité de défauts inférieure ou égale à 10^6 cm^{-2} (Fig.2).

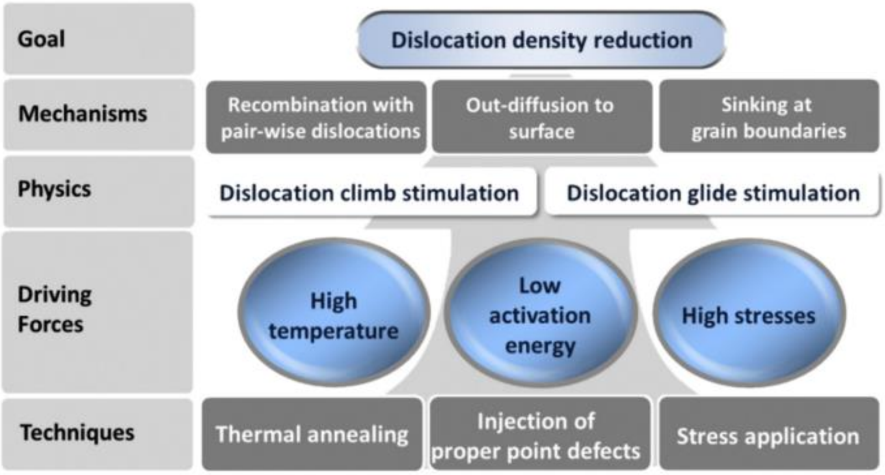


Figure I 2: Organigramme technologique pour la réduction de la densité de dislocations [17].

L'objectif de ce travail de thèse de doctorat est, dans un premier temps, de démontrer qu'il est techniquement faisable et économiquement rentable, de développer une nouvelle filière de substrat virtuel de Ge/Si en symbiose avec les autres technologies, afin de remplacer le Ge bulk en gardant ces mêmes propriétés qualitatives.

L'objectif dans un deuxième temps, est d'optimiser un procédé technologique de pré-conditionnement d'une couche tampon en désaccord de maille de manière à réduire le taux de dislocations émergeantes responsables des fuites de courant dans les dispositifs électroniques. Il sera alors possible d'améliorer le rendement, les tensions de claquage des dispositifs électroniques et photoniques désirés et par conséquent, leur fiabilité nécessaire à toute viabilité économique. Ce nouveau procédé est réalisable sur des wafers de Ge sur substrat de Silicium (001) de grandes échelles et peut être aisément industrialisé.

Pour surmonter ce verrou technologique, nous proposons une nouvelle stratégie inspirée de plusieurs phénomènes observés dans la littérature pour réduire la densité des dislocations émergentes dans une couche de Ge/Si.

L'approche est basée sur l'élaboration d'un substrat virtuel post-épitaxie dit « substrat à nano-cavités » basé sur deux aspects : (i) la nano-structuration des couches de Ge/Si par anodisation électrochimique et (ii) l'auto-assemblage des cavités nanométriques à l'interface de Ge/Si afin de relaxer la contrainte et diminuer massivement la densité de dislocations. L'adoption et la démonstration de cette approche contribue non seulement dans l'intégration facile de cellules solaires III-V multi-jonctions sur silicium, mais aussi dans l'amélioration des performances des dispositifs électroniques et photoniques basés sur la technologie Ge/Si tel que les photodétecteurs, les transistors, les microprocesseurs et les modulateurs. De plus, la démonstration de cette approche sur un système élémentaire comme le Ge/Si pourra ouvrir la voie pour produire des couches à base de d'autres matériaux de bonne qualité malgré le fort désaccord de maille.

Ce document est constitué de sept chapitres. L'introduction s'attache à souligner l'intérêt de développer une nouvelle filière de substrat virtuel pour l'industrie du photovoltaïque, les retombés sur le rapport qualité/prix des MJSCs et la difficulté de l'intégration de Ge/Si à cause du fort désaccord de maille.

Le CHAPITRE II offre une revue de l'état de l'art relatif aux différentes stratégies employées pour réduire la densité de dislocations dans le Ge/Si, de la croissance directe à la croissance à travers des buffers, finissant par discuter les limites des différentes techniques. Afin de justifier cette approche, les travaux rapportés jusqu'à présent sur l'ingénierie des défauts sont résumés. Les méthodes d'intégration les plus prometteuse sont également identifiées dans ce chapitre.

Le CHAPITRE III présente un article publié dans *Electrochemica Acta* résumant les travaux sur la porosification électrochimique de Ge et sa mise-en-échelle. Un nouveau régime nommé *Fast Bipolar Electrochemical Etching* est proposé afin d'atteindre des vitesses de gravure très élevées avec une qualité surfacique et latérale supérieure obtenue sur grandes échelles. Les paramètres de porosifiation électrochimique sont alors optimisés en étudiant l'effet de la densité de courant sur la vitesse de gravure et la porosité. Suite à ces résultats, un modèle de gravure électrochimique raffiné est proposé et confirmé par des caractérisations chimiques et électrochimiques. Enfin, un capteur interférométrique à base de Ge mésoporeux est démontré avec une sensibilité importante aux liquides incorporés dans la structure poreuse.

Le CHAPITRE IV présente un article publié dans *Nanotechnology* résumant les travaux sur la transformation morphologique de Ge poreux sous traitement thermique et l'évolution des propriétés électriques et structurelles des couches poreuses. Une conductivité électrique hautement contrôlable dans des couches de Ge mésoporeux en conduisant une étude systématique de la taille des cristallites a été rapportée.

Le CHAPITRE V présente une lettre soumise dans *APL Materials* résumant les travaux sur la nouvelle architecture de substrat virtuel de Ge/Si basé sur la reprise de croissance de Ge sur un substrat de Ge/Si poreux formant des nono-cavités dans la couche de germanium.

Le CHAPITRE VI présente un article sous révision soumis dans *Nature Communications* résumant les travaux sur une stratégie innovante pour atteindre la densité de dislocation émergentes très faible en utilisant un processus peu coûteux dans le domaine de l'ingénierie des défauts dans la croissance hétéroépitaxiale. Nous montrons expérimentalement, à travers une porosification électrochimique sélective suivant les dislocations et par auto-assemblage de nano-cavités autour de l'interface Ge/Si, qu'une grande partie des dislocations sont figées et bloquées près d'une surface libre. La densité de dislocation de filetage moyenne est réduite de plus de trois ordres de grandeur, de ~ 10^7 cm^{-2} à ~ 10^4 cm^{-2} pour des couches de Ge de 1,5 µm d'épaisseur, ce qui est considéré comme très faible pour une couche épitaxiale aussi mince. Des modèles expliquant ces résultats expérimentaux sont incluses. En utilisant cette approche, nous avons créé un substrat virtuel Ge/Si *epi-ready* produit à plus grande échelle, qui répond à toutes les exigences pour l'épitaxie des alliages et des dispositifs III-V. Les propriétés optiques, étudiées par cathodoluminescence à température ambiante, indiquent une forte amélioration du rendement d’émission de films de GaAs crûs sur ce substrat virtuel Ge/Si.

Le dernier chapitre présente une synthèse des résultats et une liste des travaux futurs.

L’ANNEXE 1 présente un article publié dans *Nanoscale Research Letters* résumant les travaux nano structuration de p-GaAs par anodisation électrochimique. Les paramètres de porosifiation électrochimique sont alors optimisés en étudiant l’effet de la densité de courant sur la vitesse de gravure et la porosité. La nature chimique de la couche obtenue a été révélée par différentes techniques de caractérisation montrant que contrairement aux rapports de littérature sur la porosification de p-GaAs, la couche est principalement transformée en oxyde d’arsénique poreux. Un modèle électrochimique est donc proposé montrant que la nanostructuration des semi-conducteurs binaires par anodisation électrochimique s'avère plus complexe.

CHAPITRE II ÉTAT DE L'ART

Les propriétés optoélectroniques supérieures de Ge par rapport à Si, font de ce semi-conducteurs un candidat très prometteur pour les technologies photoniques. Cependant, le facteur clé de toutes ces applications est la qualité du matériau. Les techniques d'épitaxie actuelles ne permettent pas de combiner le Ge avec le Silicium facilement en raison d'un désaccord de maille (4,2%). Or, ce dernier génère des contraintes mécaniques qui en se relaxant provoquent la formation de défauts structuraux étendus (dislocations) qui détériorent les propriétés optoélectroniques du dispositif. En effet, au-delà d'une certaine épaisseur critique, il se produit une relaxation des contraintes avec la formation, à l'interface, d'un réseau de dislocations de rattrapage de maille appelées « dislocations misfits » [17-18], [12]. Ces dislocations qui se propagent dans la couche de Ge, donnent naissance à des dislocations émergentes de type 60° ou « threading dislocations » qui glissent dans le plan (111) [18]. Il est évident donc que ces défauts peuvent dégrader les propriétés du germanium, et notamment servir comme centre de recombinaison/génération de porteurs ce qui va jouer sur les performances des dispositifs microélectroniques [20]. La forte densité de dislocations est préjudiciable pour le bon fonctionnement de ces dispositifs [21]. Dans ce cas, il est nécessaire de fabriquer des couches de Ge/Si ayant une haute qualité structurelle en termes de relaxation, morphologie et densité de défauts. A cet effet, plusieurs approches ont été proposées et développées au cours des dernières années pour réaliser des couches de Ge/Si relaxées à faible densité de dislocations.

II.1 Croissance épitaxiale et bilan énergétique

L'obtention de couches minces monocristallines nécessite l'utilisation des techniques de croissance hors équilibre tels que l'épitaxie en phase liquide ou vapeur, l'épitaxie par jet moléculaire ou par faisceau chimique. Le mécanisme de la croissance épitaxiale est basé sur l'incorporation des adatomes sur la surface du substrat. Les adatomes sont faiblement liés et donc, très mobiles. La surface réelle d'un cristal présente des sites d'incorporation de natures différentes, tels que les marches atomiques et les agrégats de nucléation (Fig. 1). Les adatomes donc migrent sur la surface ou diffusent dans des sites énergétiquement plus stables [22]. Dans le cas de l'épitaxie Ge/Si, la couche et le substrat ne sont pas de même nature. On parle alors d'hétéroépitaxie. Pour que l'épitaxie puisse avoir lieu, il va falloir tenir compte des différences entre la couche et le substrat telles que :

- Les énergies de surface et d'interfaces
- La structure cristalline de la couche et du substrat
- Les paramètres de maille.

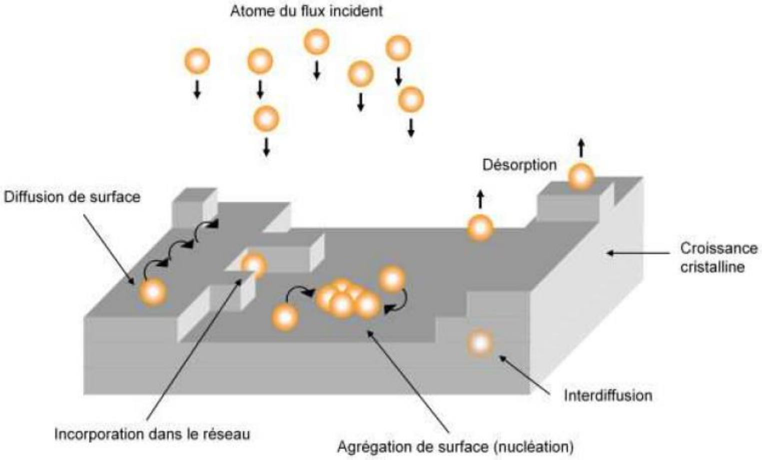


Figure II 1: Différents phénomènes intervenant dans le processus d'épitaxie [22].

II.1.1 Énergies de surface et d'interfaces

La morphologie des couches obtenue durant le processus de l'épitaxie dépond fortement des différences des énergies de surface entre le matériau déposé et le substrat. En effet, l'énergie totale du système $\Delta\gamma$ va être augmentée ou diminuée en fonction de l'énergie de surface de substrat γ_s, l'énergie de surface de la couche γ_c et l'énergie d'interface γ_i selon :

$$\Delta\gamma = \gamma_c + \gamma_i - \gamma_s$$

Selon le signe de cette énergie, on peut distinguer deux modes de croissance : Le mode de Frank-Van der Merwe qui correspond à une croissance bidimensionnelle si $\Delta\gamma$ est négative ou le mode Volmer-Weber qui correspond à une croissance tridimensionnelle si $\Delta\gamma$ est positive. Dans cette dernière, des ilots de matériau se forment car les atomes sont plus attirés entre eux que par le substrat [23].

II.1.2 Énergie de la contrainte

Le fait que le Ge a un paramètre de maille plus grand que le Si, la couche de Ge va être contrainte en compression ce qui va engendrer un autre mode de croissance : le mode Stranski-Krastanov. Dans ce cas, l'arrangement des atomes sera contrôlé par les énergies de surface $\Delta\gamma$ mais aussi par l'énergie élastique emmagasinée dans la couche ΔE_e causée par le désaccord de maille. Le bilan de l'énergie de système dans ce cas est donné par :

$$\Delta E = \Delta\gamma + \Delta E_e$$

L'énergie élastique emmagasinée E_e dépendra proportionnellement de l'épaisseur de la couche déposée, le désaccord de maille ainsi qu'au coefficient de Poisson V et le module de Young G selon [24]:

$$E_e = \frac{2G(1+V)}{(1-V).(\Delta a/a)^2.e}$$

e : l'épaisseur de la couche.

Dans ce mode, la croissance de la couche se fait dans un premier temps en 2D (monocouche par monocouche), mais au-delà de certaine épaisseur critique e_c, l'énergie élastique accumulée par l'augmentation de l'épaisseur va être supérieure à l'énergie de surface. A partir de cette épaisseur, la couche va adopter le mode de croissance 3D et forme des ilots qui vont permettre une relaxation élastique partielle de la contrainte sur le niveau supérieur des ilots (Fig. 2).

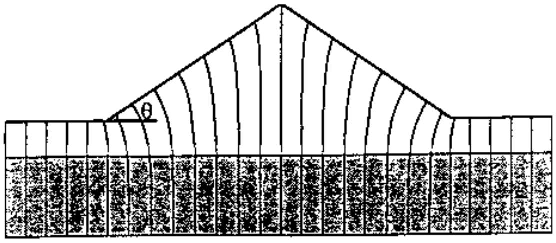


Figure II 2: Croissance de Ge sur Si selon le mode Stranski-Krastanov [25].

La formation d'un îlot entraîne une diminution de l'énergie élastique emmagasinée, E_e, et une augmentation de l'énergie de surface. La variation de l'énergie totale est donnée en fonction de l'énergie de relaxation par la formation des ilots ΔE_{3D} et égale à :

$$\Delta E = \Delta\gamma + \Delta E_e - \Delta E_{3D}$$

Il faut noter que la formation de la morphologie 3D peut être influencée par des paramètres cinétiques. Donc, si la thermodynamique indique que de grands ilots sont plus stables qu'une couche contrainte, leur formation nécessite des conditions cinétiques plus exigeantes (longueur de diffusion très grande). Cependant, la formation des ilots peut être défavorisée dans l'épitaxie de Ge/Si à basse température. En fait, la diffusion des adatomes qui forment les ilots diminue par l'absence d'une activation thermique ce qui conserve la croissance plane.

II.1.3 Minimisation de l'énergie par relaxation élastique

L'énergie élastique emmagasinée dans la couche augmente avec l'augmentation de l'épaisseur de la couche. Cette dernière va conserver une croissance bidimensionnelle mais avec l'apparition des ondulations sous l'effet des contraintes en compression [26]. Ces ondulations vont relaxer partiellement la contrainte au sommet. Le bilan énergétique dans ce cas reste favorable à l'apparition des ondulations mais pas pour longtemps. Le bilan énergétique dans ce cas est donné par :

$$\Delta E = \Delta\gamma + \Delta E_e - \Delta E_{\sim}$$

D'où ΔE~ est l'énergie de relaxation par la formation des ondulations.

II.1.4 Minimisation de l'énergie par relaxation plastique

L'énergie élastique emmagasinée dans la couche ne cesse pas d'augmenter avec l'augmentation de l'épaisseur jusqu'à dépasser l'énergie nécessaire pour générer les dislocations. En effet, les dislocations vont permettre à la couche d'adapter son paramètre de maille à celui de l'état massif. La nucléation des dislocations permettra le relâchement des contraintes.

II.1.5 Le model de Matthews et Blackeslee

Ce modèle explique la naissance des dislocations émergentes au-delà de l'épaisseur critique. En fait, lors de la croissance, la contrainte générée par le désaccord de maille crée une force qui s'exerce sur les dislocations préexistantes dans la couche. Ces dislocations vont glisser et créer des segments d'adaptation. L'épaisseur critique e_c est donnée en fonction du désaccord de maille ε, le vecteur de burgers b, le coefficient de poisson V, l'angle entre le vecteur de burgers et la ligne de la dislocation ϑ, l'angle entre le vecteur de burgers et la norme de la ligne de la dislocation λ et α : le facteur de l'énergie de cœur de la dislocation selon :

$$e_c = \frac{b}{8\pi\varepsilon}\,\frac{1-\nu cos^2\theta}{(1-\nu)cos\lambda}\,\ln(\frac{\alpha e_c}{b})$$

La figure 3 montre le calcul théorique de l'épaisseur critique à partir de ce model et quelques valeurs expérimentales obtenue sous différentes températures. Les valeurs de l'épaisseur peuvent être dépassées selon la température de croissance. En effet, la nucléation des dislocations est un phénomène activé thermiquement, on peut donc obtenir des couches contraintes au-delà de l'épaisseur critique à basse température.

Dans le cas de Ge/Si, l'épaisseur critique théorique est de l'ordre de quelques angströms soit quelques monocouches, Mais plus la température de croissance est basse plus l'épaisseur critiques est grande.

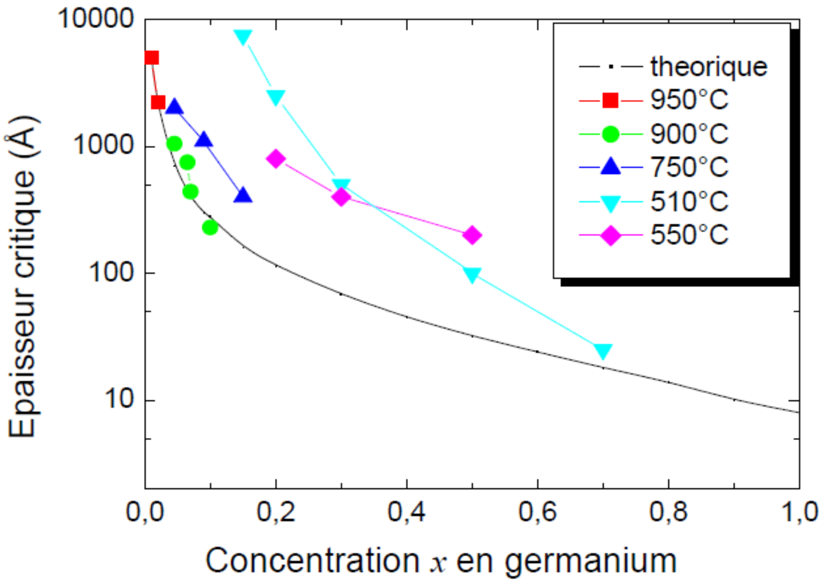


Figure II 3: Épaisseurs critiques théoriques - modèle Matthews et Blackeslee et expérimentales d'une couche de SiGe/Si. La courbe théorique montre l'épaisseur critique de Ge/Si de quelques Angströms. Les valeurs utilisée sont : b = 3.9Å, ν = 0.28, cos θ = 0.5, cos λ =0.5, et α = 2 [27], [28].

II.1.6 Le taux de relaxation

La relaxation de la couche contrainte ne se fait pas directement d'un état complètement contraint à un état complètement relaxé. En effet le taux de relaxation dépend de nombre de dislocations générées au-delà de l'épaisseur critique plastique. R est donné par :

$$R = \frac{(a_c^{//} - a_s)}{(a_c - a_s)}$$

II.1.7 Le bilan énergétique

Le bilan énergétique dans ce cas dépend du taux de relaxation qui va permettre de quantifier l'état de contrainte de la couche. En effet, si toute l'énergie du désaccord de maille emmagasinée E_e est dégagée sous forme de dislocation, et que le nombre de dislocation est suffisant, le paramètre de maille de la couche $a_c{}^{//}$ sera égale au paramètre de maille à l'état naturel a_c, le taux de relaxation égale donc à 1. On parle ici d'une couche complètement relaxée mais contient des défauts. Dans ce cas, l'énergie plastique ΔE_P va équilibrer l'énergie du système et le bilan énergétique donc, tend vers zéro :

$$\Delta E = \Delta\gamma + \Delta E_e - \Delta E_{3D\ ou\sim} - \Delta E_p$$
$$\Delta E = 0$$

Si la relaxation est partielle, l'énergie résiduelle $\Delta E_{P\%}$ reste emmagasinée dans la couche. Le bilan énergétique dans ce cas est positif.

$$\Delta E = \Delta\gamma + \Delta E_e - \Delta E_{3D\ ou\sim} - \Delta E_{p\%}$$
$$\Delta E > 0$$

II.2 Les différentes architectures de substrat virtuel Ge/Si

II.2.1 Croissance directe sur Si (001)

Il existe deux approches principales pour déposer le Ge à faible densité de dislocations traversantes (TDD) sur Si (001) : Croissance directe ou à travers une couche tampon. La croissance direct en mode Stranski-Krastanov qui est une combinaison de croissance 2D (planaire) et de croissance 3D par îlots produit une densité de dislocations très élevée et une grande rugosité de surface [29]. La TDD est de l'ordre de 10^{10} à 10^{9} cm^{-2} dépendamment de l'épaisseur de la couche [30]. Il est possible d'éviter la formation d'îlots et de garder une croissance planaire en utilisant des conditions de croissance appropriées, notamment une température de croissance modérée [14]. Pour cela, la croissance à basse température peut être réalisée pour défavoriser le mode de croissance 3D afin d'avoir une couche mince fermée avec une surface relativement lisse. Ensuite, la température élevée sera utilisée pour produire des taux de croissance plus élevés et améliorés.

II.2.2 Stratégie des recuits

L'une des manières les plus répandues pour abaisser la TDD est le traitement thermique lors ou après la croissance de matériaux. Le recuit à haute température engendre une forte mobilité des dislocations rend la recombinaison de ces dernières plus efficace. Par exemple, Takagi et al. ont appliqué un recuit sur des couches de GaAs/Si dans un RTA pendant quelque seconds à hautes températures entre 900°C et 1000°C, ce qui a permis une réduction significative de la TDD [31]. Yamamoto et al. ont réussi à diminuer la densité de dislocation des couches de Ge/Si élaborées par RPCVD de 10^8 cm^{-2} à 7.10^5 cm^{-2} pour une épaisseur de 4,7µm. La croissance a été faite à 300°C puis à 550°C. La rugosité de la surface obtenue est de l'ordre de 0,44 nm [32] (Fig. 4). Ces valeurs dépendent de l'épaisseur de la couche; (une couche de Ge > 1 µm sera nécessaire pour atteindre TDD $<10^7$ cm^{-2})[33].

Lee et al. ont changé la séquence de la croissance de Ge/Si par MOCVD. Le cycle se compose de plusieurs étapes à basse température (LT) à 400°C, rampe de température intermédiaire (LT-HT) de 10°C / min et à haute température (HT) à 600°C. Elle est suivie par un recuit post-croissance dans l'hydrogène à température allant de 650 à 825°C. Le film de Ge épitaxié d'épaisseur ~1 µm montre une densité de dislocations de $\sim10^7$ cm^{-2} et une rugosité de ~ 0,75 nm [34]. Choi et al. ont employé une étape additionnelle de recuit à haute température sous flux d'hydrogène. Cette étape a amélioré la qualité de la surface de la couche Ge/Si [35].

Également, l'effet de recuit sur le contrôle de la TDD dans GaAs/Si dépend du nombre de cycles. Il a été démontré par Okamoto, que la densité de dislocations peut être réduite jusqu'à $\sim2\times10^6$ cm^{-2} pour 13 cycles de recuit [36].

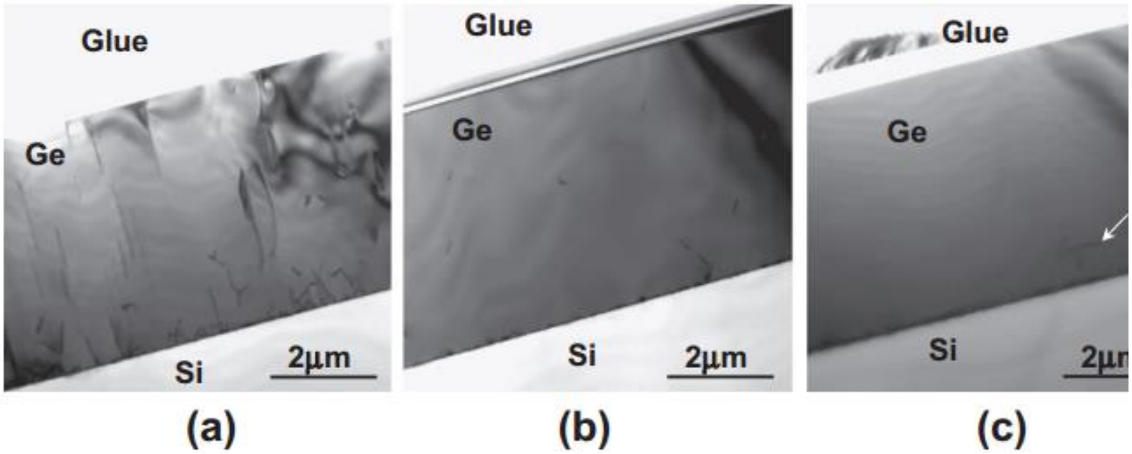


Figure II 4: TEM de 4.7µm de Ge/Si (a) sans recuit (b) avec recuit direct à 800°C (c) avec un recuit cyclique [32].

II.2.3 Recombinaison des défauts dans des couches épaisses

La recombinaison des dislocations se fait soit par coalescence lors de la croissance, soit par annihilation (déflection de dislocation par une tension locale). Afin d'obtenir une couche de Ge avec une faible densité de dislocations < 10^6 cm^{-2}, une grande épaisseur déposée sera nécessaire [37]. Dans le cas d'une croissance de GaAs sur Si, pour atteindre une densité de dislocation de 4.10^5 cm^{-2}, il faut 180µm de GaAs epitaxiés sur Si. Ceci rend cette stratégie très couteuse [38].

II.2.4 Désorientation de substrat

Cette approche consiste à désorienter le vecteur de burger des dislocations en faisant la croissance sur une surface désorientée (4°). Otsuka et al. supposent que la présence des marches atomiques favorise la nucléation des dislocations avec un vecteur de burger horizontal qui permettent d'accommoder plus efficacement le désaccord de maille. Ce type de dislocation est relativement plus favorable et engendre une diminution significative de la TDD dans le cas de GaAs/Si [39].

II.2.5 Croissance sur buffer

(1) Par l’intermédiaire d’une couche tampon (SiGe buffer)

C’est le procédé le plus étudié pour atteindre de faible TDD de Ge/Si. Cette approche consiste à utiliser un alliage de SiGe de composition graduelle en tant que buffer entre la couche de Ge et le substrat de Si [32-34]. La relaxation de la contrainte entre le Ge et le Si résulte après une augmentation progressive de la concentration en Ge de 0% à 100%. Cette approche nécessite l’association d’une étape de CMP afin de réduire la rugosité de la couche. Cependant, le compromis pour avoir une bonne qualité cristalline de Ge est l’augmentation de l'épaisseur du buffer (typiquement de l'ordre de quelques µm), ce qui rend l’implication de la CMP primordiale après 50% de composition (Fig. 5).

La densité de dislocations obtenue est de l’ordre de 10^6 cm^{-2} [41].

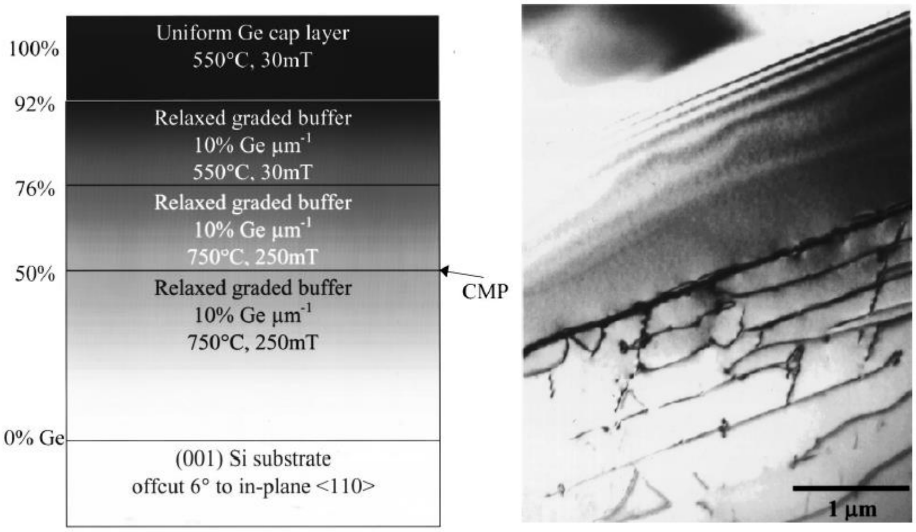


Figure II 5: Schéma des conditions de croissance et la structure nécessaires pour l'intégration de Ge sur Si (001) par une couche composition graduelle de Ge [41].

Plusieurs méthodes pour réduire l'épaisseur de SiGe ont été proposées récemment. Huang et al. [42]. ont développé deux couches tampons en SiGe de différente composition. Les couches ont été déposées par UVCVD à basse pression, la première couche tampon est composée de 55 % de Ge avec une épaisseur de 0,4 µm et la deuxième en 65% avec une épaisseur de 0,6µm. Immédiatement après la croissance de chaque couche tampon, la plaquette a été recuite in-situ pendant 15 minutes à 750°C pour réduire davantage la densité de dislocations [43]. Ensuite, la température a été réglée à 400°C pour croître une couche de Ge de 2,5 µm. Ang et al. [44] ont réalisé un photo-détecteur à base de Ge avec une couche tampon de SiGe très mince ~30 nm d'une concentration graduelle de 10% à 50% suivie d'une couche de Ge crûe à basse température ~370°C et enfin, un film de 2µm de Ge. Cette succession de croissance conduit à des couches relaxées à faibles TDD en surface de Ge.

(2) Par l'intermédiaire d'une couche d'oxyde (Oxyde buffer)

Les propriétés physicochimiques des oxydes sont riches et permettent d'adapter les paramètres importants de la croissance de Ge sur une large gamme (paramètre de maille, coefficient de dilatation thermique, l'énergie de surface…etc.) [45]. Un autre avantage est donné par le fait que l'oxyde agit également comme une barrière contre la diffusion du Si. Par conséquent, des films ultra-minces de Ge pur peuvent être obtenus sur Si. Cependant, cette approche est plutôt nouvelle et les densités de défauts sont encore plus élevées par rapport à la couche tampon de SiGe classique.

Giussani et al. ont essayé d'utiliser des oxydes cristallins complexes tel que l'oxyde de Praseodymium (Pr_2O_3) comme couche tampon pour l'intégration de Ge (111)/Si (111) [38¬39]. La couche de Ge a été déposée à deux températures différentes à 600°C puis à 300°C (Fig. 6). La densité de dislocations obtenues est de l'ordre de 10^7 cm^{-2} [48].

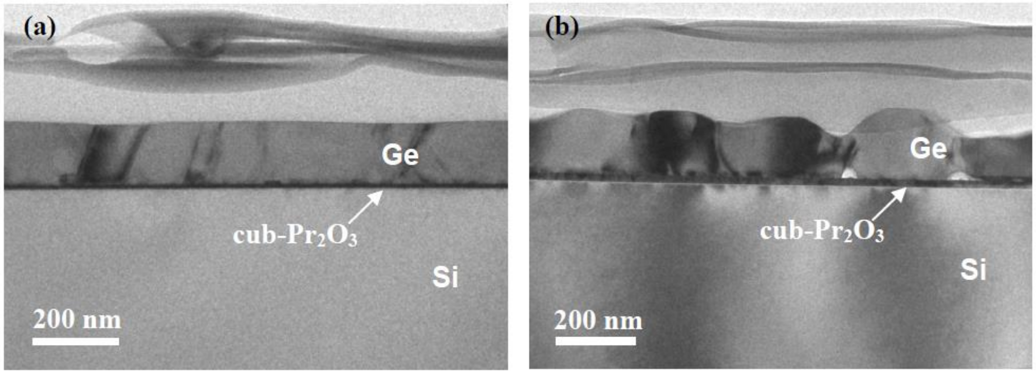


Figure II 6: Images TEM d'une couche de Ge (a) déposée en deux étapes à 600°C, puis à 300°C sur une couche tampon de Pr2O3. (b) un film Ge entièrement cru à 600°C [47].

(3) Croissance sélective sur Deep-Substrate-Patterning

En 1989, Fitzgerald a montré que la densité des dislocations émergentes peut être réduite dans des hétérostructures en désaccord de maille par croissance sur des petites surfaces. L'énorme avantage de la croissance sur de petites surfaces est dérivé de la courte longueur de la dislocation *(misfit)* générée par chacune des sources de dislocation. L'extension de cette technique aux systèmes à désadaptation élevée peut conduire à une meilleure qualité cristalline [49]. A. Marzegalli et al. ont fait croitre le Ge dans des tranchées de Si gravées profondément. Les prismes micrométriques de Ge déposés sont rapprochés afin de former un film quasi-continu de bonne qualité tel que démontré dans la figure 7. La densité des dislocations peut être réduite par un facteur d'environ 30 par recuit à 415°C [50].

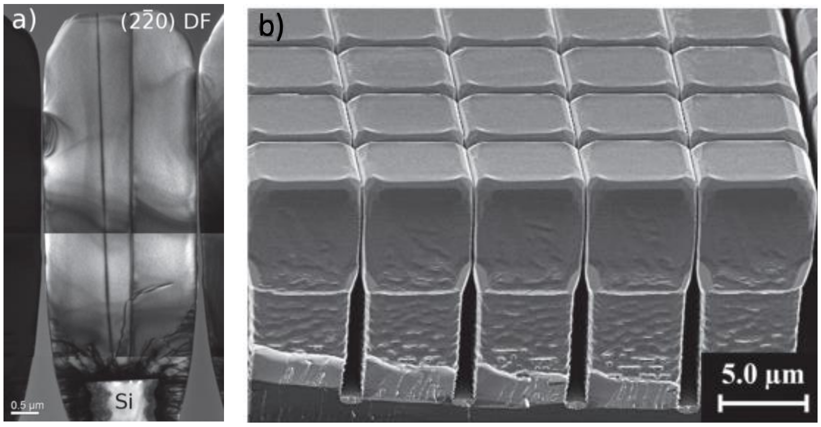


Figure II 7: (a) Analyse par TEM de 8 µm d'épaisseur du prisme de Ge sur 2µm × 2µm de motif de Si (b) Image SEM du film de Ge quasi-continu montrant les sommets plats des prismes de Ge après une gravure sélective [50].

(4) Piégeage de dislocations par aspect ratio trapping (ART)

Après que Li et al. aient démontré qu'on puisse réaliser une croissance sélective de Ge/Si via des ouvertures dans une couche de SiO_2 [51], une nouvelle approche prometteuse permis l'intégration de Ge/Si par l'utilisation d'une architecture dite «aspect ratio trapping (ART)». Avec cette approche, le matériau en désaccord de maille est déposé dans des tranchées en SiO_2 ou nitrure de Si avec des ratios suffisants pour confiner les dislocations dans la partie inférieure de la tranchée. L'idée a été proposée pour la première fois par Liu et al. [52] qui ont déposés une couche de Ge polycristallin suivie d'un recuit rapide proche de la température de fusion de Ge (930°C) pour produire une épitaxie en phase liquide. La majorité des défauts cristallins restent emprisonnés dans les fenêtres de SiO_2 [53]. Park et al. ont défini le rapport de forme (AR>1) nécessaire pour emprisonner les dislocations [54] (Fig. 8-a). Ensuite, Bai et al. ont étudié le mécanisme d'élimination de dislocations dans la configuration ART. La figure 8-b montre que durant la croissance, les dislocation sont répliqués le long de la facette normale puis sont déviées à partir du centre des régions sélectives [55].

Le développement de cette approche permettra de produire des couches de Ge/Si avec une densité de dislocations suffisamment faible pour les dispositifs microélectroniques [51]. La qualité de la couche de Ge relaxée a été évaluée par HRXRD et montre une très bonne qualité cristalline [53].

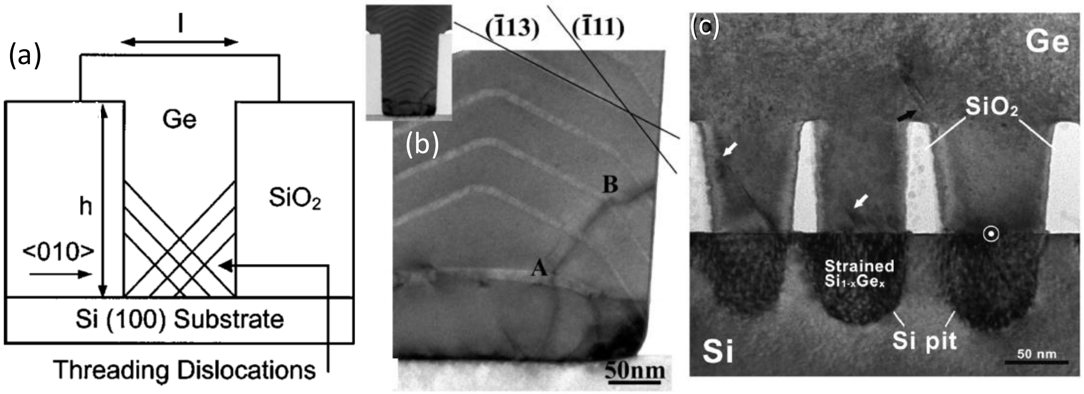


Figure II 8: (a) Représentation schématique du principe de piégeage de dislocation par des ouvertures dans le SiO_2. (b) Images TEM montrant le mécanisme de déviation de dislocations (c) Images TEM montrant de faible densité de dislocations à la surface du Ge via des fenêtres [54]–[56].

Huangfu et al. ont introduit des nano-fenêtres dans la couche de SiO_2 par l'utilisation d'une membrane ultra-mince d'alumine poreuse (PAM) au lieu d'une lithographie conventionnelle qui limite le procédé par le cout et les dimensions (Fig 8-c). Avec une telle approche la densité de dislocations a diminué de 10^8 cm^{-2} à 10^6 cm^{-2} [56].

(5) Blocage par SiO_2

Leonhardt et al. ont proposé une technique qui réduit de manière significative la densité de dislocations de Ge sur Si hétéroépitaxié. Dans cette approche, on fait croitre tout d'abord une couche de Ge sur Si. Ensuite, le Ge sera gravé aux niveaux des terminaisons des dislocations à la surface. Une fine couche de SiO_2 sera ensuite déposée par PECVD puis protégée par une résine de manière à localiser le SiO_2 juste au niveau des terminaisons des dislocations. La croissance de la couche de Ge sera reprise ensuite. Le SiO_2 stoppe donc la propagation des dislocations dans la couche épitaxiale supérieure de Ge (2µm) (Fig. 9). Ce procédé se termine par un recuit de la couche de Ge et permet de réduire la densité de défauts de 10^8 cm^{-2} à 10^6 cm^{-2} [57].

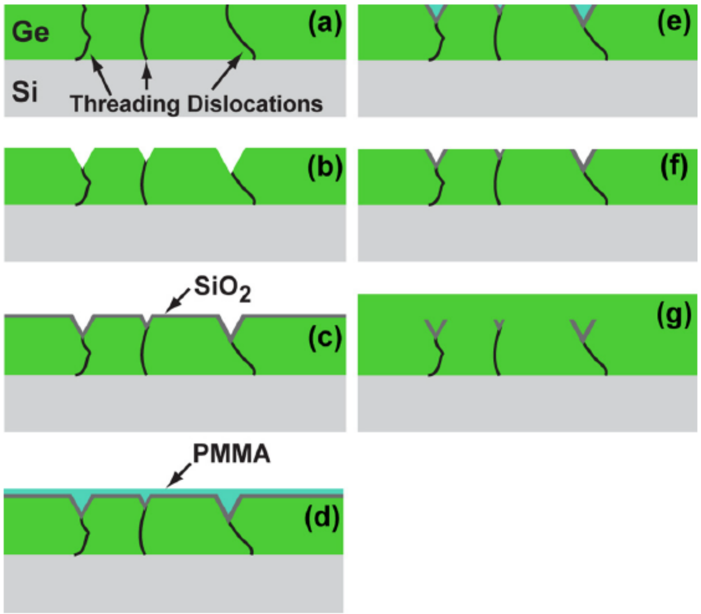


Figure II 9: Représentation schématique du processus « Blocage par SiO$_2$ ». Image (a) montre les dislocations se terminant à la surface de la couche de Ge/Si. (b) montre la révélation des dislocations. (c) montre le dépôt d'une fine couche de SiO$_2$. (d) dépôt d'une couche de résine PMMA. (e) élimination de la résine et l'oxyde par gravure ionique. (f) développement de la résine qui reste (g) Reprise de l'épitaxie de Ge et blocage de la propagation des dislocations dans la couche de Ge supérieure [57].

(6) Formation de Ge par condensation de SiGe

Tezuka et al. ont proposé une nouvelle technique d'intégration de Ge/Isolant/Si par condensation d'une couche de SiGe à faible concentration en Ge. Au départ, une couche de SiGe est épitaxiée avec une faible composition de Ge. Du fait du très léger désaccord de maille, cette couche reste contrainte sur SOI. Puis, en effectuant une oxydation sélective du Si de la couche SiGe à 900°C-1050°C, l'épaisseur de SiGe diminue du fait de la consommation du Si pour former l'oxyde de Si, alors que le Ge diffuse dans la couche de SiGe jusqu'à la silice du substrat de SOI. En retirant la couche de SiO$_2$ formée par oxydation de Si de la couche de SiGe, on obtient une structure de type GeOI [58]. Ce procédé est très lent (7h pour 16 nm) et la concentration de Ge dans la couche formée est impure (57%). De plus, la contrainte appliquée lors de l'oxydation génère plus de dislocations (Fig. 10).

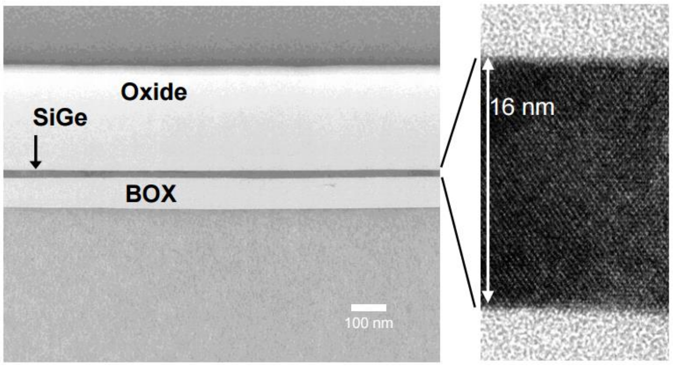


Figure II 10: Image TEM d’une couche de $Si_{0.4}Ge_{0.6}OI$ (16 nm d'épaisseur) obtenue par oxydation de 140 nm de la couche de $Si_{0.9}Ge_{0.1}$ pendant 7 h [58].

(7) Ge épitaxié sur Si poreux

Ce concept a été proposé par Lo et al. en 1991, il s’agit d’un substrat qui se déforme élastiquement ou plastiquement lors de la croissance de la couche de Ge, afin que cette dernière retrouve son paramètre de maille non contraint tout en étant exempte de dislocations. Plusieurs stratégies ont été proposées soit par la réalisation de l’épitaxie sur une membrane libre d’épaisseur très faible [59]; cette dernière va s’adapter à la couche épitaxiale en cours de croissance, ce genre de substrat est nommé [substrat compliant] [60]. Les travaux de Calabrese et al. ont démontré que l'intégration de germanium directement sur silicium poreux pour surmonter l'écart entre les paramètres de maille est faisable (Fig. 11). La croissance du Ge se fait par Low-energy plasma-enhanced chemical vapour deposition (LEPECVD) à environ 500°C [61] puis à 750°C [62]. Les meilleurs résultats ont été obtenus pour une porosité de 22%. La densité de dislocations est de l’ordre est 10^6 cm^{-2} pour 5µm de Ge/Si poreux.

Boucherif et Lysenko ont proposé d'utiliser l'oxydation contrôlée du silicium poreux comme un moyen d'étendre et d'ajuster le paramètre de maille du Si. L’idée est basée sur l’oxydation du substrat de Si rendu poreux de façon à augmenter son volume et donc à contraindre en tension la fine couche monocristalline dessus. Le paramètre de maille de surface de cette dernière en devenant plus grand se rapprochera de celui du germanium. En jouant sur la porosité et/ou le taux d'oxydation, ce paramètre de maille pourra être ajusté aux applications envisagées. La densité de dislocations obtenue par cette stratégie sur des fines couches (50 nm) de $Si_{0.72}Ge_{0.28}$ est de l’ordre de 6.10^6 cm^{-2} [60], [55-56].

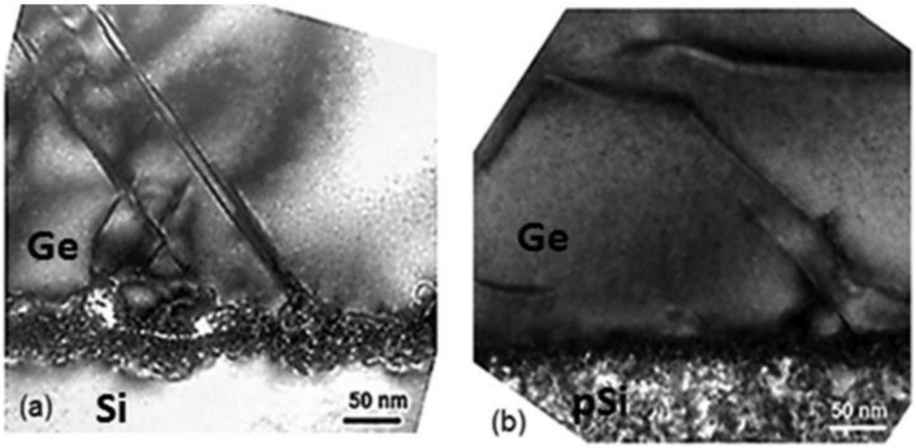


Figure II 11: Image TEM de (a) Ge/Si bulk et (b) Ge/Si poreux (22%) cru à 750°C [62].

II.2.6 Collage direct

Cette approche consiste à mettre en contact deux matériaux parfaitement polis, plats et propre pour les relier mécaniquement à la température ambiante grâce aux forces de van der Waals [65] [66]. La technologie Smart Cut consiste à implanter l'hydrogène ou l'hélium dans le substrat de Ge, lier et coller les deux substrats de Ge et de Si après le nettoyage, puis séparer une fine couche de Ge au niveau de la zone implantée donnant lieu à la structure Ge/Isolant/Si, le reste de substrat de Ge peut être recyclé (Fig. 12) [59-60].

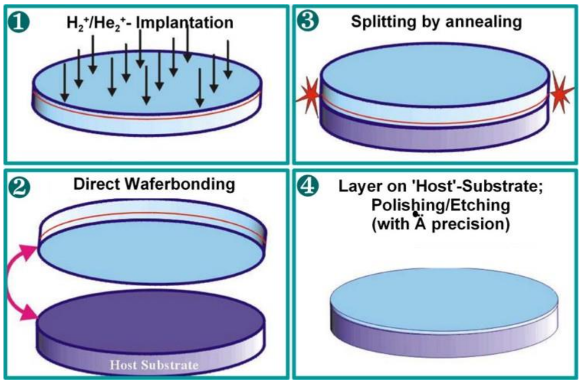


Figure II 12: Représentation schématique du processus Smart Cut. (1) Implantation d'hydrogène dans le substrat de Ge. (2) Wafer bonding. (3) Séparation au niveau de la zone implantée (4) Lissage de la surface de Ge collé [68].

Cette approche est économique d'un point de vu matériaux mais limitée par son cout élevé, sa complexité, et par le fait qu'elle ne permet pas de traitement (pleine plaque) de substrats de Si de grande taille, étant limité par la taille généralement plus petite du substrat de Ge.

II.3 Approches alternatives pour l'intégration des matériaux à fort désaccord de maille

II.3.1 Modification de substrat par implantation ionique

Cette nouvelle approche a été énoncée par B. Hollander et al. pour réaliser une couche de $Si_{0.67}Ge_{0.33}$ relaxée avec une densité de dislocations inférieure à 10^4 cm^{-2}. Les auteurs ont employé l'implantation d'He pour contrôler la relaxation de la couche de SiGe déposée sur Si/SiO_2 [69]. Les résultats ont montré que quelles que soient le nature des ions implantés He^+ ou Si^+ (au cours ou après la croissance) et l'hétérostructure SiGe/Si, $SiGe/Si/SiO_2$ ou Si/SiGe/Si(100) [70], la densité de dislocations obtenue n'est pas moindre de 10^6 cm^{-2}. La figure 13-a présente une image TEM d'une couche de SiGe/Si déposée sur un substrat SOI (silicium-oxyde-isolant). Des défauts causés par l'implantation qui affectent la rugosité de surface et la qualité cristalline ont été observés.

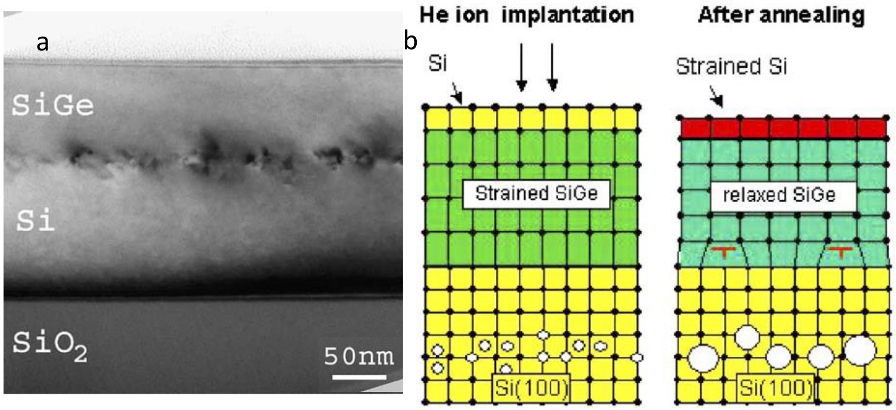


Figure II 13: (a) Images en MET vue transverse de 88 nm de $Si_{0.67}Ge_{0.33}$ cru sur substrat SOI après implantation de Si^+ et recuit à 850°C (b) Mécanisme de relaxation de SiGe par implantation d'He^+ [70], [71].

Buca et al. ont montré que le degré de relaxation de la couche de SiGe augmente avec la dose d'ions de Si implantés jusqu'à 77%. Après un recuit à 800°C, les atomes d'He localisés dans les sites interstitiels ou dans les lacunes diffusent pour former des bulles qui vont relaxer la couche SiGe [71]. La figure 13-b illustre le mécanisme de la relaxation de la couche SiGe après l'implantation de l'He. Cependant, cette stratégie nécessite la croissance d'une fine couche de Si (strained Si) sur la couche de SiGe qui contribue efficacement à améliorer la qualité de la surface. La densité des dislocations de la couche SiGe est de l'ordre de 10^5 cm^2.

G. Regura et al. ont optimisé les paramètres d’implantations (He et Ne) et de recuit afin d’obtenir une densité des dislocation égale à 10^4 cm^{-2}. Cette fois, la préparation du pseudo substrat se fait avant l’épitaxie de la couche SiGe. La formation de bulles d’He est obtenue entre 700° et 1050° et la croissance de $Si_{0.8}Ge_{0.2}$ se fait dans un PECVD à 600°C [72]. M. Raissi et al. ont poursuit la même thématique avec une augmentation considérable de la densité de cavités nanométriques formées (nanobubble) [73]. La figure 14 présente une image TEM en section transverse de la couche épitaxiée SiGe sur silicium implanté, l’épaisseur de cette couche est 215 nm. Cette observation ne révèle aucune présence du réseau de dislocations misfit systématiquement observé dans le cas de couche SiGe élaborée sur substrat de silicium non implanté. L’explication pourrait être l’annulation des dislocations à la surface interne des bulles formées par implantation. Après la révélation chimique de l’émergence en surface de ces dislocations 60° fournit une EPD inférieure à 10^3 cm^{-2}. Cette valeur a été confirmée également par des mesures de photoluminescence [74].

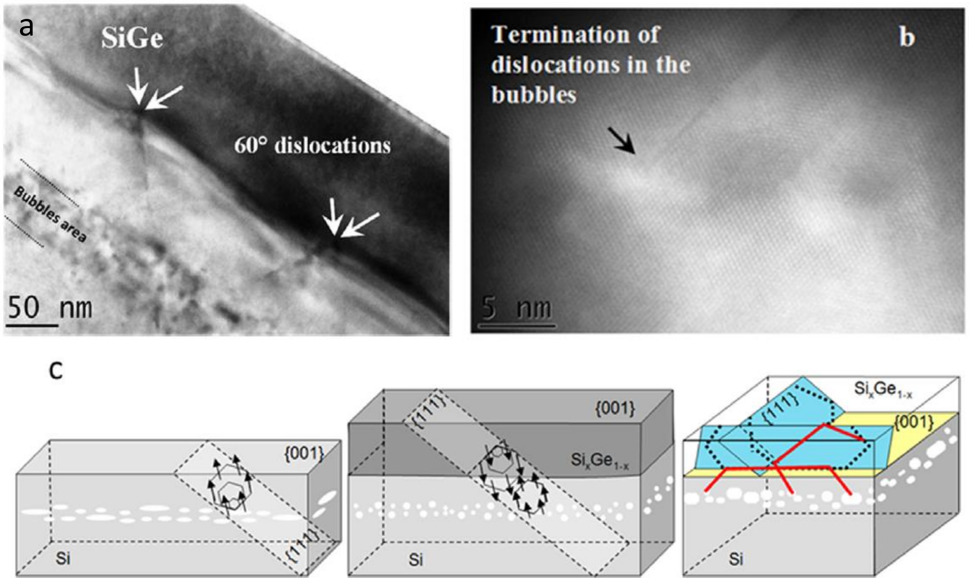


Figure II 14: (a) Images en TEM vue transverse d’une zone indiquée par les flèches sur l’image qui présente le blocage des dislocations 60° à l’interface. (b) Blocage de dislocations au niveau des bulles. (c) Schéma descriptif explique le mécanisme de relaxation de la couche sur les plans des bulles [74].

Cette technique est récente et démontre un fort potentiel de leur concept, mais le mécanisme d’élimination des dislocations émergentes reste à développer dans les prochaines années.

(1) Mécanisme de formation des bulles par implantation ionique :

La configuration la plus stable de l'hélium, dans le silicium, est la position interstitielle avec une énergie de migration théorique de 0,96 eV [75].

Le coefficient de diffusion D de l'He à la température T est donnée par :

$$D = D_0 e^{E_A/KT} \quad avec \quad D_0 = \nu . l^2$$

v est la fréquence de vibration de l'hélium en site interstitiel, l est la séparation entre deux sites interstitiels, K la constante de Boltzmann et E_A l'énergie d'activation de migration.

Durant le recuit, les atomes d'hélium interstitiels vont diffuser (T > 250°C) soit vers la surface, soit vers la région des complexes lacunaires où ils vont se faire piéger. C'est seulement pour des températures supérieures à 500°C que l'hélium va pouvoir commencer à piéger des complexes. L'une des conséquences de l'implantation d'ions hélium après recuit consiste en la formation de cavités (bulles) de différentes épaisseurs et l'apparition de lacunes [76].

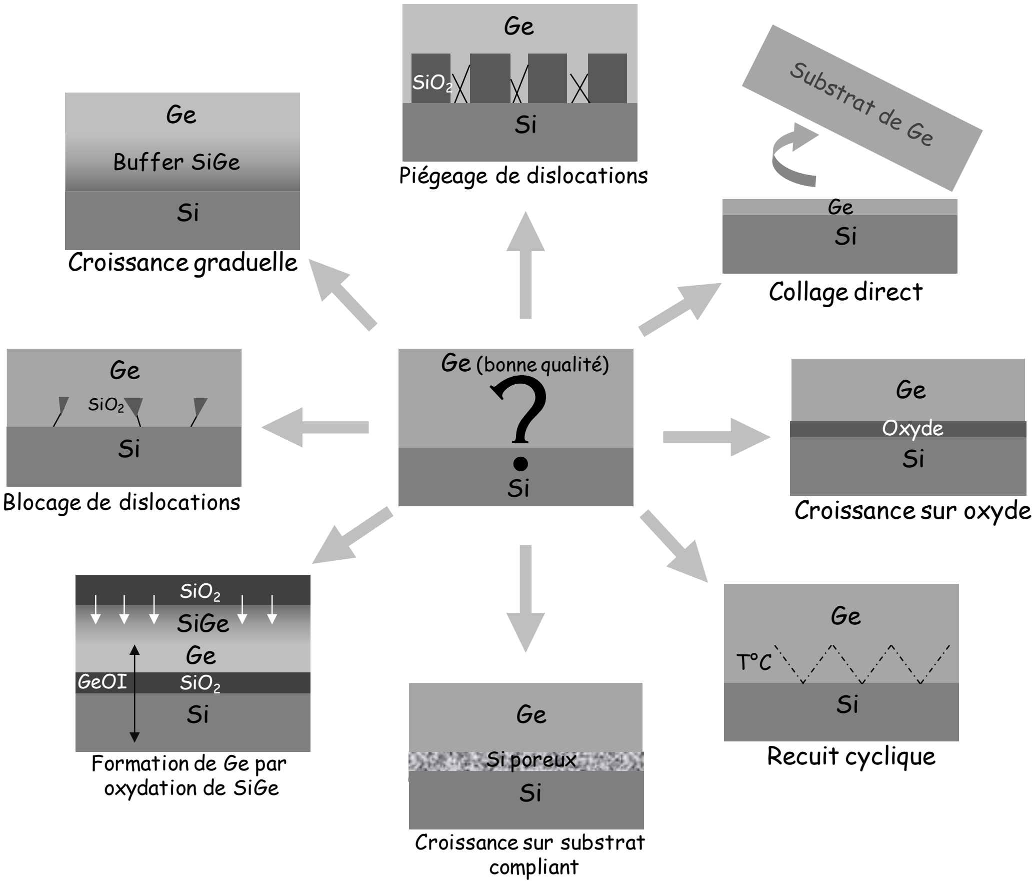
II.4 Réflexion sur les différentes stratégies

En résumé, nous avons passé en revue les progrès réalisés dans la croissance épitaxiale de Ge/Si de ces dernières décennies. Le désaccord de maille de 4,2% entre ces deux matériaux apporte de grands défis pour atteindre des couches de Ge de haute qualité. L'émergence de différentes techniques telles l'insertion d'une couche tampon de composition graduelle ou LT/HT en deux étapes et recuit thermique cyclique ou la croissance épitaxiale sélective… etc peuvent être des solutions valables pour une diminution de la TDD.

La majorité des approches citées a démontré la faisabilité de leurs concepts. Cependant, une comparaison quantitative de la densité de dislocations reste difficile, dépendamment de l'épaisseur de la couche. En effet, l'augmentation rapide de la densité de dislocations au-delà de l'épaisseur critique pourra être expliquée par la relaxation de la couche qui génère par cet effet des dislocations. En plus, La diminution de la densité de dislocations en fonction de l'augmentation de l'épaisseur pourra être expliquée selon Speck et al. par l'augmentation la probabilité d'auto recombinaison des dislocations [69-70]. On ne peut pas donc attribuer la faible densité des dislocations mesurée juste par le fait qu'il y a une progression dans les approches proposées alors que l'épaisseur de la couche de Ge est un facteur non négligeable dans la comparaison quantitative.

Malgré que la modification du substrat par implantation d'ions ait été étudiée sur un système différent SiGe, elle montre un phénomène intéressant qu'on pourra l'introduire dans notre approche. En effet, l'introduction des bulles nanométriques joue un rôle important dans la recombinaison ou l'annulation des dislocations. Aussi, les bulles peuvent à priori permettre la relaxation totale du paramètre de maille des couches fines de SiGe en servant d'adaptateur des contraintes, tout en limitant la densité de dislocations émergentes à la surface et sa rugosité.

Les autres difficultés rencontrées relèvent soit d'un facteur d'échelle, de coût ou de complexité. En effet vouloir relaxer des couches de Ge sur des substrats de Si de grandes dimensions avec une faible densité des dislocations relève un défi majeur d'où la nécessité de mettre en place une nouvelle approche qui ne dépend pas de toutes ces contraintes.



Mode	Strategie	TDD cm^{-2}	Epaisseur (µm)	Ref.	Remarques
Croissance directe sur Si	Sans traitement	5.10^{9}	0,1	Claeys et al. [22]	Varie en fonction de l'epaisseur
	Strategie de recuit	7.10^{5}	4,7	Yamamoto et al. [24]	Ge >1µm : TDD < 10^{7} cm^{-2}
	Recombinaison dans des couches epaisses	10^{6}	>50	Romanov et al. [29]	180µm GaAs/Si : 10^{5} cm^{-2}
	Desorientation de Substrat	/	/	Otsuka et al. [31]	Diminution de dislocation : GaAs/Si
Croissance indirecte sur Si	SiGe buffer	10^{6}	~ 7	Currie et al. [33]	Ang et al. Faible TDD : Ge (2µm)/SiGe (30nm)
	Oxyde buffer	10^{7}	0,2	Giussani et al. [38]	Buffer : Oxyde de Praseodymium (Pr_2O_3)
	Piégeage de dislocations	10^{6}	1	Huangfu et al. [48]	Depend du facteur de forme des fenetres
	Blocage par SiO_2	10^{6}	2	Leonhardt et al. [49]	/
	Oxidation de SiGe	/	16 nm	Tezuka et al. [50]	$Si_{0,4}Ge_{0,6}$ OI
	Epitaxie sur Si poreux	10^{6}	5	Calabrese et al. [54]	Si poreux 22%
Collage direct	Collage direct	/	/	Smart Cut	Ge/Si (Liaisons de Van Der Waals)

Tableau II 1: Représentation schématique et tableau récapitulatif de l'état de l'art des différentes stratégies pour l'intégration de Ge/Si.

II.5 Germanium poreux

Dans le cadre de cette thèse, le Ge mésoporeux est développé en vue de la réalisation de substrat virtuel de Ge/Si pour des applications photovoltaïques, mais l'élaboration et la maîtrise de ce matériau contribuerait largement à la science des matériaux et pourrait servir pour les nombreuses applications mentionnées ci-dessus.

Le germanium comme le silicium constituent des matériaux d'importance technologique majeure puisqu'ils interviennent dans plusieurs domaines d'intérêt comme la microélectronique et l'optoélectronique. D'un point de vue scientifique, ces matériaux servent souvent de modèle car ils sont produits sous forme de monocristaux de pureté très bien contrôlée et avec une densité de dislocations résiduelles extrêmement faible [79]. Dernièrement, le Ge a attiré une grande attention grâce à une large gamme de propriétés qui pourrait susciter de nouvelles applications. Le Ge a relativement une faible bande interdite (0,67 eV), il possède une constante diélectrique très élevées ($\varepsilon Ge = 16.2$) comparée aux ($\varepsilon Si = 11.7$), ($\varepsilon GaAs = 12.9$), ($\varepsilon InP = 12.5$) ce qui lui rend un matériau intéressant pour des applications dans les cristaux photoniques [80]. Le Ge a une large gamme d'applications dans le domaine d'optique grâce à son indice de réfraction très élevé ($nGe = 4$ dans l'infra-rouge) [81]. La surface de Ge pourra être hydrophobe avec une terminaison H ou hydrophile avec une terminaison OH juste par un switch de courant anodique ou cathodique appliqué [82],[83]. La fonctionnalisation chimique de Ge est assez facile grâce à l'absence d'un oxyde stable au niveau de la surface [84]. Ainsi, la réduction dimensionnelle de Ge à une échelle nanométrique induit l'apparition de nouvelles fonctionnalités, telle que le confinement quantique [85]. Nous allons détailler dans les paragraphes suivants les principales propriétés de Ge bulk et de Ge poreux qui est le matériau de base de notre procédé de fabrication du substrat virtuel à Nano-cavités.

II.5.1 Anodisation de Ge poreux

L'anodisation de Ge pour la fabrication des couches de Ge poreux s'effectue dans la cellule électrochimique présentée dans la figure 15, suivant le principe détaillé dans le chapitre III. Le substrat de germanium (001), dopé (p+), est placé sur l'anode de cuivre en bas de la cellule. La cathode est une électrode en spirale en platine (inerte chimiquement) et est placée dans l'électrolyte en haut de la cellule. La cellule est remplie d'acide fluorhydrique à 49% et d'éthanol 30% (HF : éthanol 5 :1). La densité du courant qui circule entre les deux électrodes est contrôlée de manière à contrôler la porosité du Ge poreux. L'anodisation a été optimisée afin d'obtenir des couches nanostructurée très épaisses dépassant les 10 µm de qualité bien maitrisée et homogènes

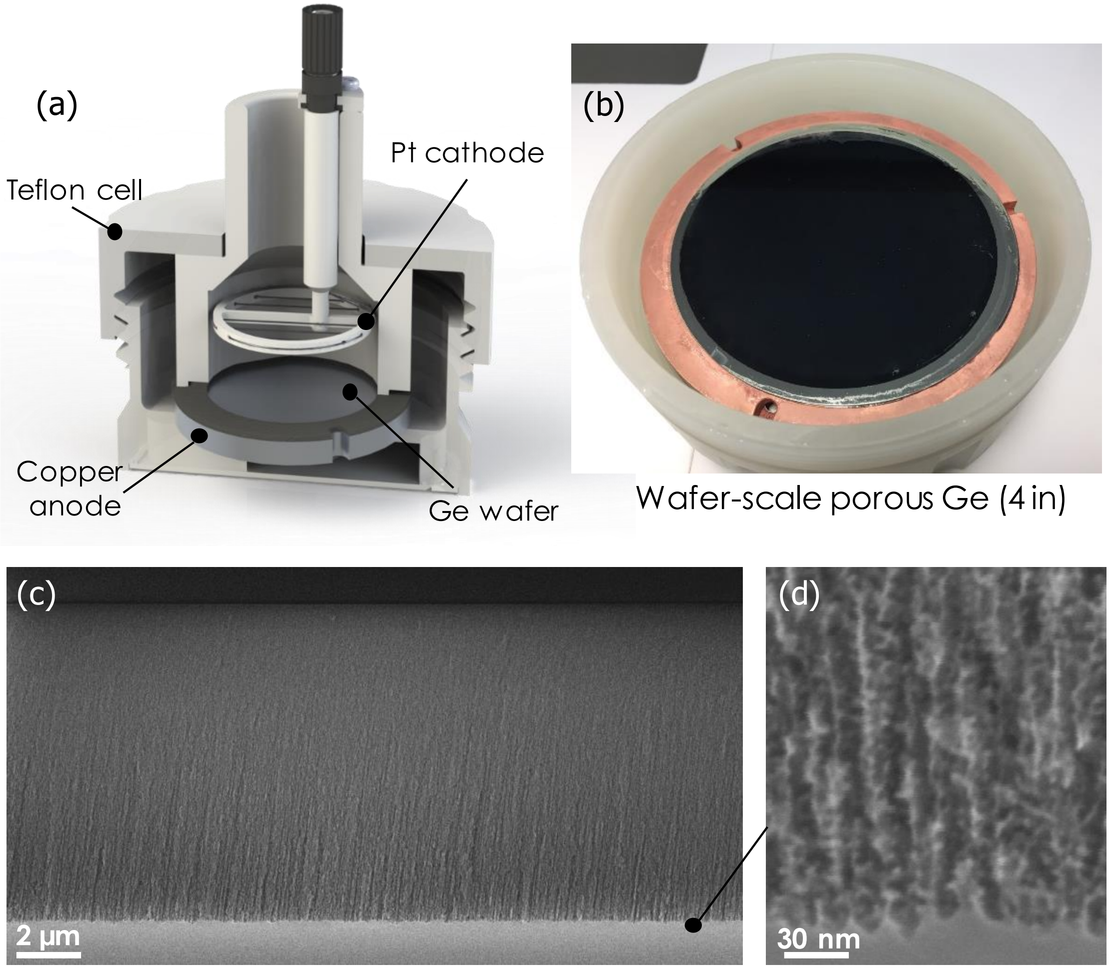


Figure II 15: (a) Vue schématique de la cellule d'anodisation améliorée par Kymosis. (b) Photo d'un substrat de Ge poreux fabriqué à partir d'un wafer de 4 pouces.(c,d) Photo en microscopie électronique à balayage du germanium mésoporeux avec une épaisseur de 10 µm obtenue par Fast Bipolar Electrochemical Etching (FBEE) (Travaux de thèse).

II.5.2 Les propriétés de Ge poreux

(1) Les propriétés électroniques

Les matériaux poreux présentent des avantages par rapport aux matériaux originels dont ils sont issus. Ces avantages se situent aussi bien au niveau des applications que dans le domaine de la recherche fondamentale. Les propriétés électroniques de Ge peuvent être affectées après le processus de porosification et notamment, la structure de bande électronique. En effet, la réduction de la taille des cristallites lors de la porosification est le phénomène essentiel qui pourra générer des propriétés électroniques différentes à celles du bulk.

Guzman *et al.* [86] ont présenté une étude comparative sur les structures des bandes électroniques de Ge bulk et poreux calculées par le model *tight-binding* (TB) et par *Local Density Approximation* DFT-LDA. Le système modélisé s'agit d'une structure cristalline de Ge dans lequel les pores périodiques sont produits en supprimant des colonnes d'atomes le long de la direction [001] et la surface des pores est passivée par des atomes d'hydrogène. Les résultats de la structure des bandes électroniques montrent un élargissement évident de la bande interdite de Ge poreux (Fig. 16-a). Cet écart augmente en fonction de la porosité et diminue en augmentant la taille des cristallites (Fig. 16b).

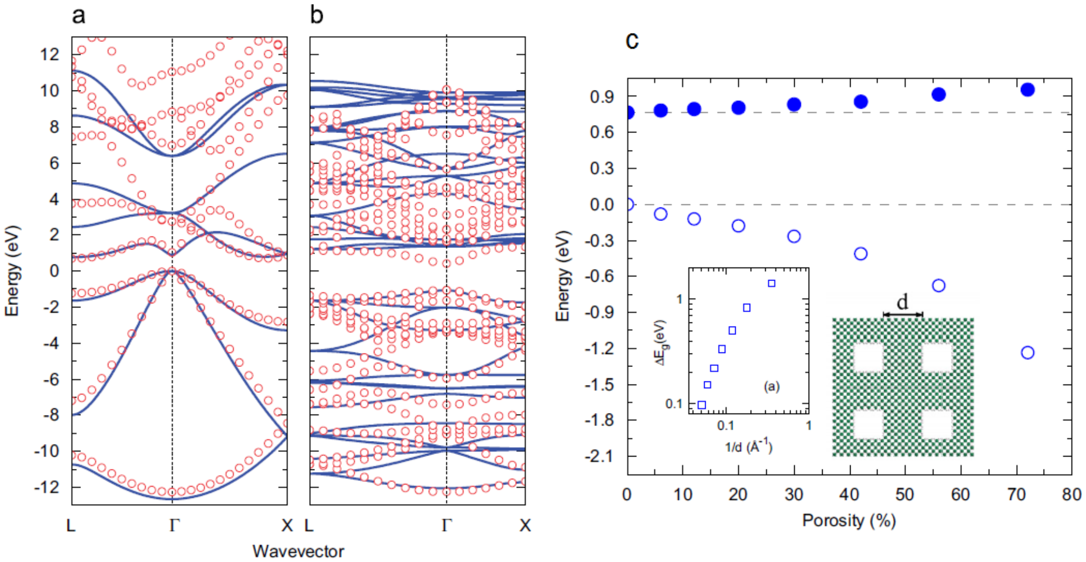


Figure II 16: Structures de bandes de Ge (a) et Ge poreux (b) calculées par TB (bleu) et DFT-LDA (rouge). L'écart entre la bande de valence et la bande de conduction en fonction de la porosité (c) et en fonction de la taille des cristallites (Inset) [86].

(2) Les propriétés optiques

(a) Confinement quantique et piégeage de lumière :

Lorsqu’un matériau semiconducteur absorbe un photon, un électron est excité dans la bande de conduction, ce qui laisse un trou dans la bande de valence. L’interaction de Coulomb entre l’électron et le trou génère un état lié appelé exciton, qui contrôle en grande partie les propriétés optiques des semi-conducteurs. Il s’avère de plus que lorsque le milieu est structuré sur une échelle nanométrique, la réponse optique des semi-conducteurs est radicalement modifiée par le confinement quantique. En fait, la diminution de la taille du cristal conduit à la situation spécifique où le rayon de Bohr de l’exciton est plus grand que la particule (Ge_{Bohr} = 24 nm). On parle alors de confinement quantique, c'est-à-dire que le déplacement des électrons-trous est limité par les dimensions du matériau [87].

Après la découverte en 1990 d’une photoluminescence intense de Si poreux nanostructurés à la température ambiante [88], [89] les semi-conducteurs poreux ont suscité un grand intérêt grâce à leur potentiel d’applications en nanoélectronique, nanophotonique, photocatalyse, ainsi que dans les domaines de la conversion d’énergie et de la détection biologique. Les nano-cristaux de Ge poreux fabriqués par gravure électrochimique bipolaire ayant une taille moyenne de 5-7 nm ont montré une émission dans le proche infrarouge (1095-1360nm) (Fig. 17). Cette photoluminescence au-dessus du bandgap de Ge bulk obtenue à basse température (25K) est une preuve solide de confinement quantique dans les cristallites [90].

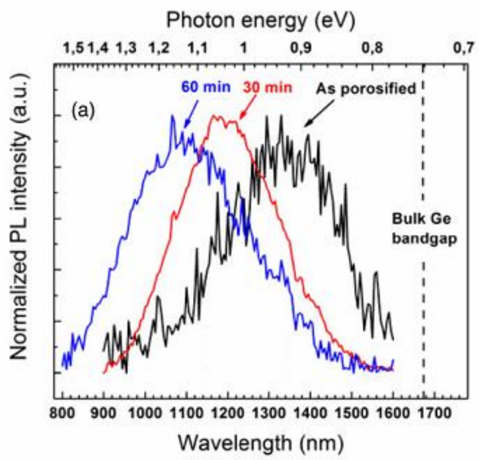


Figure II 17: Spectres de photoluminescence des échantillons de Ge poreux immédiatement après porosification (noire) et après ajustement de la taille des cristallites pas oxydation et gravure chimique (rouge et bleu) [90].

Le phénomène de confinement quantique et les effets de piégeage de la lumière ont été aussi observés dans des couches de Ge nano-poreux obtenues par implantation ionique [91]. En effet, un décalage de la PL vers le bleu a été clairement observé dans le Ge poreux sur SiO_2 ayant une taille de cristallite de l'ordre de 14 nm. Cet effet n'a pas été observé dans l'échantillon de Ge poreux fabriqué directement sur Ge bulk. Les auteurs ont expliqué ce phénomène par le déplacement des porteurs photo-générés à partir de la couche nano-poreuse au substrat de Ge connectée directement avec la couche poreuse, perdant ainsi le confinement. En revanche, dans les couches de Ge poreux sur SiO_2, les porteurs photo-générés restent confinées à l'intérieur des nanostructures qu'ils vont rencontrer un obstacle potentiel à l'interface avec SiO_2 pour atteindre le substrat (Fig. 18).

Une forte augmentation de l'intensité de la PL a été observée dans les couches de Ge poreux. Cette amélioration du signal doit être liée au piégeage de la lumière dans les pores. Cet effet engendre une amélioration de l'absorption de la lumière dans les structures 3D.

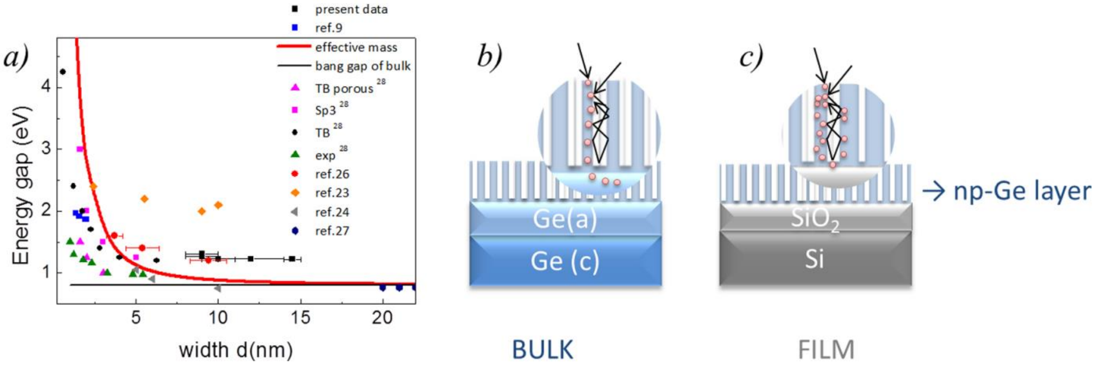


Figure II 18: (a) Les valeurs de la bande interdite mesurées en fonction de la taille moyenne des cristallites dans la littérature. Piégeage de la lumière et génération des porteurs dans le Ge poreux sur (b) Ge bulk et (c) SiO_2 [91].

Il est important donc de souligner, que les nanostructures à base de Ge poreux contribuent non seulement à améliorer l'absorption de la lumière piégée dans les structures nano-poreuses, mais aussi dans la photo-génération des porteurs libres par confinement quantique. Ces porteurs peuvent être collectés pour générer un photo-courant, ce qui est un point clé pour atteindre des dispositifs photovoltaïques très efficaces.

(b) L’indice de réfraction

Il a été démontré que la porosification est un outil efficace pour ajuster l'indice de réfraction de Si [81]. La modulation de l'échelle nanométrique des propriétés du matériau telles que la porosité et de la morphologie ouvre des perspectives intéressantes pour la réalisation d'une grande variété de dispositifs optiques tels que Fabry Pérot, miroirs de Bragg, guides d'ondes, ou des structures à cristaux photoniques. L’indice de réfractions élevé de Ge (4 dans l'infrarouge) offre des avantages pour le développement de dispositifs de détection à puce.

Le phénomène de Fabry-Perot était souvent utilisé afin d'étudier les performances de détection de la couche de germanium poreux. La lumière réfléchie par l'interface supérieure (air-MPGe) et l'interface de fond (substrat MPGe-Ge) interfèrent les uns avec les autres et affiche des franges typiques Fabry-Perot dans le spectre de réflectance. L’indice de réfraction de Ge poreux est donné selon :

$$n_{pGe} = {}^{k}/_{(2.\,\delta \mathrm{v}.\mathrm{t})}$$

t : l’épaisseur de la couche.

δν : la région du nombre d'onde utilisée.

k : le nombre de franges dans la région du nombre d'onde.

L’infiltration des liquides dans le matériau poreux ou la fonctionnalisation chimique de la surface poreuse en changeant l’indice du milieu effectif offrent des voies pour le développement des dispositifs de détection tel que les détecteurs d’humidité [92] ou les biocapteurs [81].

(3) Les propriétés thermiques

Les nanostructures du groupe IV tels que le silicium, le germanium et le carbure de silicium sont particulièrement intéressants dans le domaine de l’isolation thermique des dispositifs microélectroniques [93]. La conductivité thermique d’un système poreux doit prendre en compte certains paramètres tels que la conductivité thermique de chaque phase (solide et gaz), leur fraction volumique (porosité) et la structure de la matière solide. Par exemple, le silicium poreux fabriqué par gravure électrochimique a une conductivité thermique inferieure de 2 à 3 ordres de grandeur à celle du silicium bulk [94]. Cependant, la porosification du germanium était réputée difficile, en particulier pour obtenir des couches épaisses et uniformes. Le problème de l'uniformité a été relativement réglé mais la vitesse de gravure reste trop lente, de l'ordre de 1 µm/h.

Isaev et al. ont étudié la conductivité thermique des structures spongieuses de Ge poreux obtenues par gravure électrochimique bipolaire. La valeur de conductivité thermique mesurée par technique photo-acoustique à température ambiante égale à 0,6 W/mK. La figure 19 montre que les résultats expérimentaux sont en excellent accord avec les simulations de Monte Carlo. Ces expériences montrent une importante réduction de la conductivité thermique des couches de Ge poreux (0,6W/mK) par rapport au Ge bulk (58W/mK). Il est évident donc que le Ge poreux est un candidat intéressant pour les applications thermoélectriques et photovoltaïques dans lequel le transport thermique est une question vraiment cruciale [94].

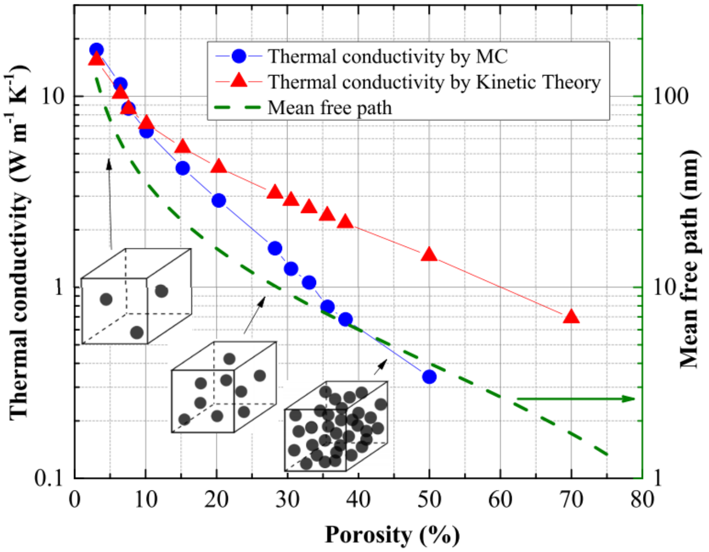


Figure II 19: Variation de la conductivité thermique de Ge nano-poreux (6 nm) en fonction de la porosité par des simulations de Monte Carlo (bleu) et par un modèle théorique (rouge). Réduction de libre parcours moyen des phonons en fonction de la porosité (vert) [94].

(4) Les propriétés mécaniques

La nano-structuration des matériaux monocristallins tels que la porosification, pourrait leurs donner des propriétés mécaniques convenables pour en faire des substrats compliants [61], [62].

Il existe peu de données quantitatives sur la résistance à la rupture (ténacité) de Si poreux, mais le travail théorique prédit que ces nanostructures pourraient être très mécaniquement durables. Canham a rassemblé les données disponibles sur le module de Young en fonction de la porosité et la morphologie des couches [95]. La figure 20 démontre que la présence d'une porosité nanométrique dans le silicium réduit considérablement sa rigidité indépendamment de la technique de mesure utilisée. Plus la porosité augmente, le module de Young diminue (pour des distributions de pores et des morphologies similaires). La valeur du module de Young peut être réduite à des valeurs d'environ 1 GPa, ces valeurs sont inférieures à celle des polymères tels que le nylon et le polystyrène. Pour le silicium macroporeux, la réduction de la rigidité par rapport à la porosité est moins spectaculaire.

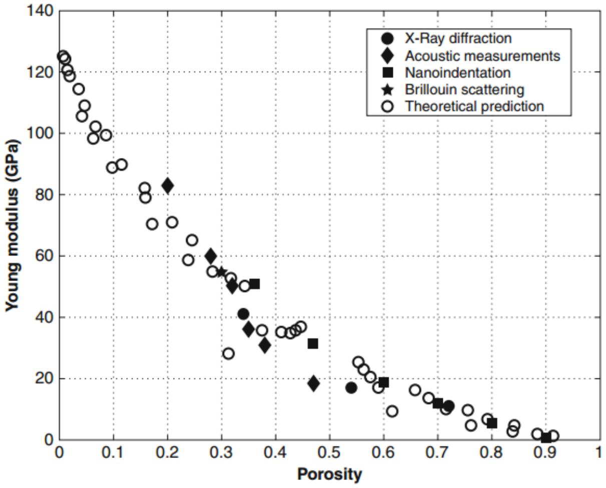


Figure II 20: Module de Young de Si poreux en fonction de la porosité [95].

(5) Impacts des propriétés mécaniques sur l'épitaxie

Les propriétés mécaniques remarquables de Si poreux ont attirées l'attention des chercheurs dans le domaine de la genèse et la croissance des couches minces. Beaucoup de travaux ont été réalisé pour croitre des matériaux semi-conducteurs IV, III-V, II-VI et autres sur un substrat compliant de Si poreux [96]. En effet, la configuration du substrat poreux devrait permettre de réaliser l'épitaxie des couches en désaccord de maille de grande épaisseur sans générer les défauts structuraux liés à la relaxation des contraintes de désaccord.

Lors de l’épitaxie, la contrainte élastique serait dans un premier temps répartie entre le substrat compliant et la couche épitaxiale, puis supportée par le substrat seul. En effet, au fur et à mesure de sa croissance, la couche épitaxiale imposerait de plus en plus son paramètre de maille. Le substrat poreux serait alors déformé (compliance élastique) ou disloqué (compliance plastique). Lors de la compliance plastique, les dislocations se dirigent vers le substrat poreux car il possède la surface libre la plus proche et c’est énergétiquement plus favorable [22].

II.6 Transformation morphologique sous traitement thermique

L’évolution de la couche poreuse lors de recuit a fait l’objet de plusieurs études. Les premiers travaux ont été faits sur le Si poreux pour la fabrication de miroir de Bragg [97] et pour le report des couches. La structuration du matériau poreux lors du recuit est basée sur la minimisation de l’énergie de surface du fait de sa grande surface spécifique. Plusieurs modèles ont été proposés pour décrire ce phénomène :

II.6.1 Le modèle de Muller et Brendel – minimisation de la surface

Muller et Brendel ont clairement mis en évidence un modèle qui explique les phénomènes d’auto-organisation de Si poreux lors de recuit. Des simulations Monté Carlo ont été effectuées et confirment les mêmes morphologies des pores obtenues par MEB sur des couches qui ont de différentes porosités [98], [99].

Ce modèle est basé sur le déplacement des atomes activés thermiquement vers les positions vacantes les plus proches. Ce déplacement se traduit par une réorganisation de la morphologie.

Les atomes de Si sont représentés dans un réseau de carrés 2D, chaque atome représente un carré et chaque facette représente une liaison chimique. Par définition, les atomes de la surface de Si poreux vont avoir une, deux ou trois liaisons, tandis que les atomes en vrac ont quatre liaisons avec des atomes de silicium voisins.

Seuls les atomes de surface sont impliqués dans le processus de recuit, parce qu'ils ont des sites vacants au voisinage. La reconstruction de surface s’effectue par le déplacement d’un atome de surface le plus labile (moins de liaison) vers un site de destination énergétiquement plus stable.

La figure 21 montre une représentation schématique en coupe bidimensionnelle d'un échantillon de Si poreux. Trois exemples différents pour des sauts atomiques sont indiqués :

- Déplacement N°1 : C'est la diffusion d'un atome de la surface vers la surface d'un pore intérieur.
- Déplacement N°2 : La diffusion d'un atome pour combler une lacune.
- Déplacement N°3 : l'évaporation d'un atome de Si.

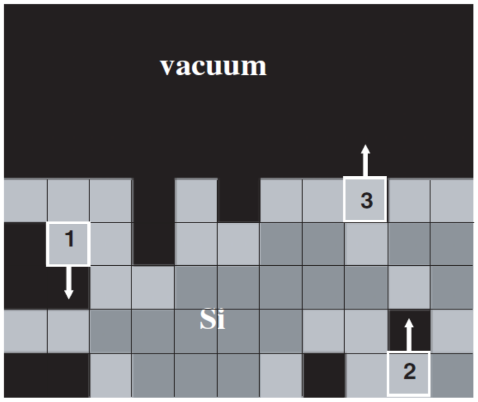


Figure II 21: Représentation 2D de la section transversale d'une surface de Si. Les atomes de surface sont représentés en gris clair, les atomes en vrac sont en gris foncé, et le noir est le vide [99].

Chaque déplacement a une énergie d'activation. L'énergie nécessaire pour casser une liaison de Si-Si est E_b = 2.34 eV. Si cette liaison se reforme dans le site de destination, l'énergie d'activation égale a E_r = 1.34 eV.

L'énergie d'activation totale pour le déplacement des atomes dans ce modèle est donnée par :

$$E = N_b E_b + N_r E_r$$

D'où N_b est le nombre de liaison cassées et N_r est le nombre des liaisons reformées.

Le déplacement des atomes aura lieu si la distribution aléatoire des atomes (r) satisfera la condition :

$$r < e^{\left(-E/_{kT_s}\right)}$$

D'où Ts est la température de recuit et k est la constante de Boltzmann.

Ce modèle comporte certaines limites car il ne tient pas en compte de l'orientation cristalline. En effet, l'énergie d'activation E et la direction de déplacement dépondent de l'orientation cristalline de la surface des pores [98].

Malgré la limite de ce modèle, les morphologies obtenues par les simulations Monté Carlo correspondent exactement aux images MEB. En effet, la formation des macros ou de microcavités dépond de la porosité initiale de la couche poreuse. Le contrôle de la porosité offre des configurations de Miroir de Bragg, des couches séparées ou des surfaces fermées. La figure 22 montre l'évolution de la porosité et la configuration des pores avant et après le recuit des couches poreuse de 20 % fabriquées et simulées.

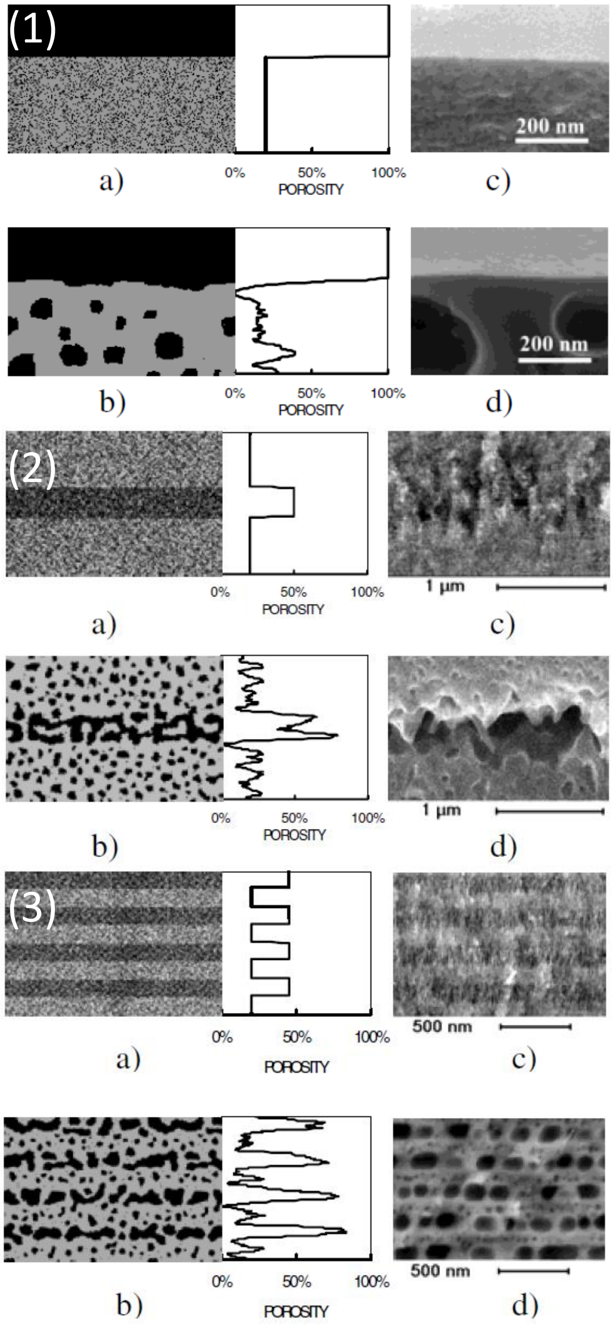


Figure II 22: Différentes configurations obtenues lors du recuit d'une couche poreuse (1) de 20% de porosité avec une surface fermée (2) une alternance de 20 % et 50 % (3) une série de porosité alternée de 20% et 45% [98].

II.6.2 Évolution des pores en fonction de temps et de la température

Les changements structuraux en volume sont guidés par un phénomène de coalescence des pores qui dépend du temps et température de recuit [97], [99]. Les pores se referment sur eux-mêmes pour former des cavités. Comme illustré sur la figure 23, les dimensions des pores augmentent clairement avec l’augmentation de la température de recuit de 1000°C à 1300°C. Ces pores augmentent également avec le temps de recuit par effet de coalescence [100], la même tendance a été observée dans le cas de Ge poreux [101].

Pour une bicouche poreuse, la présence de la couche enterrée influence la restructuration de la couche supérieure faiblement poreuse. En fait, les atomes ont tendance à s’orienter vers la porosité la plus faible d’où les sites de destination sont énergétiquement plus favorables, l’atome dans ce cas satisfait sa valence dans la couche a faible porosité et participe à former une couche fermée. La couche a forte porosité continue à augmenter ce qui reflète la formation des macrospores. Ceci explique le phénomène de la coalescence, la recristallisation des couches a faible porosité et la formation des grandes cavités dans les couches à forte porosité.

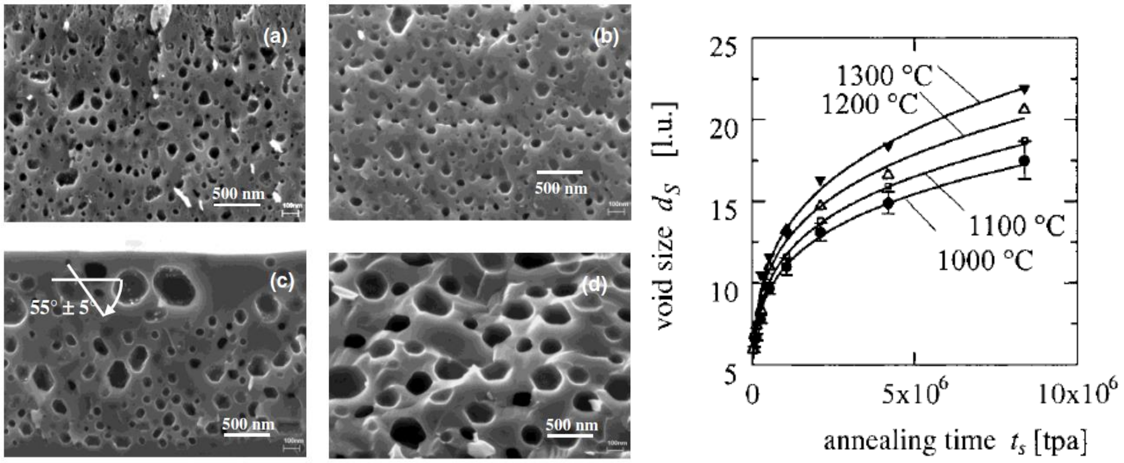


Figure II 23: Évolution des pores en fonction de la température de recuit obtenue par MEB: a) 1000°C, b) 1100°C, c) 1200°C, d) 1300°C avec une porosité initiale de 20 %. Évolution de la taille des pores en fonction de la température et le temps de recuit (à droite) [98].

II.6.3 Le rayon critique

Un autre modèle géométrique est basé sur la détermination de la forme des pores et leur distribution finale à partir du traitement à haute température. Au cours du traitement thermique, les pores agissent sous l'effet de deux mécanismes (1) les forces mécaniques appliquées sur les pores, et (2) Le mécanisme de diffusion. En effet, ce modèle prend en compte la compétition entre la contrainte mécanique interne due à la présence des pores et celle engendrée par la dilatation thermique.

La figure 24 montre la simulation de l'augmentation du rayon de pore après un recuit à 1000°C avec une contrainte résiduelle égale à 1.3 GPa et la réduction du rayon de pores après un recuit avec une contrainte résiduelle égale à 1.2 GPa [102].

Il a été constaté que l'évolution de la forme des pores lors du recuit à haute température dépend essentiellement de la contrainte initiale créée par les pores. Cette contrainte initiale est définie par le rayon critique, dans ce cas Rc = 2 nm.

Cependant, les conclusions sont semblables : les cavités ayant un rayon initial supérieur au rayon critique voient leur taille augmentée alors que les autres sont vouées à disparaître. Le rayon critique augmente avec la température [97].

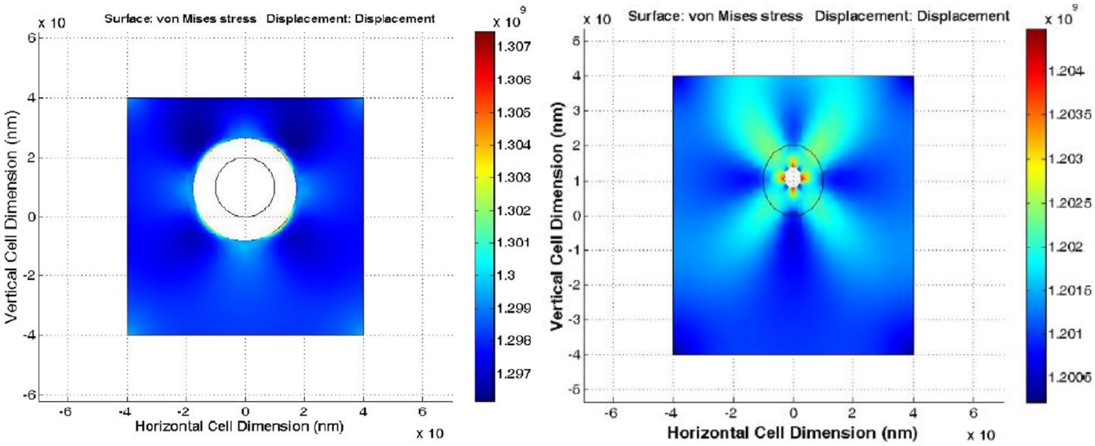


Figure II 24: Évolution du rayon critique de pore en fonction de la contrainte résiduelle [102].

II.6.4 Le facteur de forme

Le facteur de forme est un autre paramètre qui influence la configuration des cavités. En effet, il a été démontré que lorsqu'un pore cylindrique subit un recuit thermique, ce dernier se transforme à des sphères alignée sous certaines conditions.

Ce transfert est assuré par la diffusion des atomes de la surface en maintenant le volume de la cavité inchangée. Les pores colonnaires sont transformés à des cavités circulaires fermées alignées verticalement comme ulster dans la figure 25.

Cette transformation fait une démonstration du modèle de Rayleigh pour lesquels les atomes diffusent selon un gradient de potentiel chimique de la zone de surface la plus courbée vers la zone de surface la moins courbée, ce qui transforme un cylindre en une série de sphères. Une façon pour uniformiser le rayon de courbure et minimiser l'énergie de système.

Pour un rapport de forme L/Rc >> 14.4, la distance verticale entre les cavités formées λc ~ 8,9 Rc. Le rayon des sphères formées Rs ~ 1.88 Rc.

Ces valeurs ont été obtenues selon [103] :

$$R_s = 0.91\ (R_c^2 L)^{1/3}\ \ , \lambda_c = 2^{2/3}\pi R_c$$

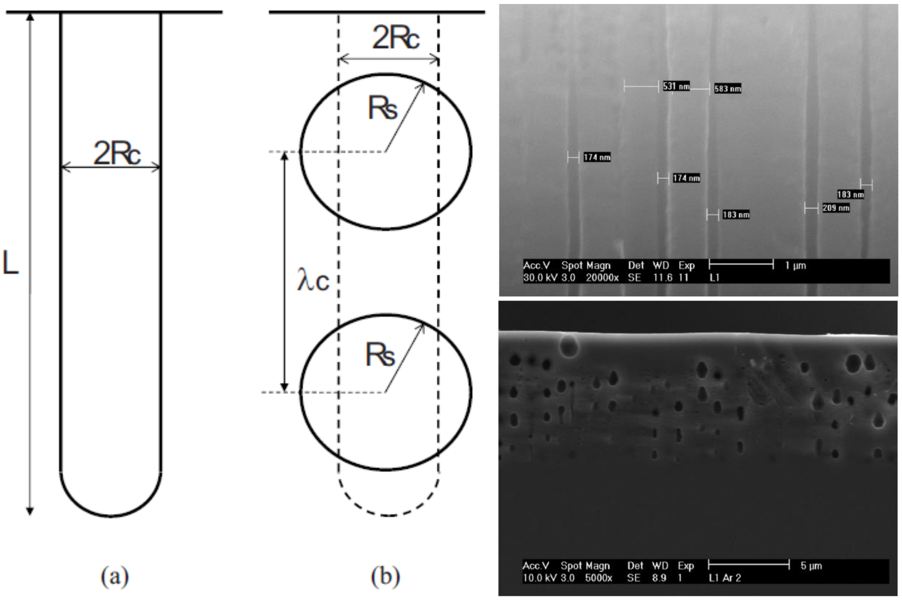


Figure II 25: Transformation des pores cylindrique obtenus par gravure électrochimique en sphères après recuit de 2h à 1150 °C [103].

II.7 Le polissage mécano-chimique du Ge

II.7.1 La CMP en général

L'étape de CMP proposée dans ce projet semble indispensable pour atteindre les faibles niveaux de rugosité nécessaires pour une reprise de croissance des matériaux III-V, surtout que le substrat virtuel de Ge/Si a subi une forte perturbation lors sa fabrication (porosification + recuit thermique). Cependant, tout traitement mécano-chimique de la surface d'un substrat destiné à l'épitaxie peut entrainer des problèmes majeurs pour l'épitaxie (défauts, contaminations etc.). Dans cette partie, nous allons détailler un procédé utilisé dans l'industrie du Germanium de manière à les rendre epi-ready.

Le polissage mécano-chimique (CMP) est devenu un procédé incontournable de l'industrie microélectronique. Son rôle principal est de fournir une planéité de surface suffisance des niveaux d'interconnections. Le procédé de polissage mécano-chimique est employé aussi dans l'étape finale de la fabrication des plaques de semi-conducteur et notamment la diminution de la rugosité. La CMP fait intervenir deux grands types d'interaction : Chimique; qui vient transformer la surface pour en changer la structure chimique. Mécanique; qui vient arracher la couche transformée chimiquement par l'intermédiaire des particules abrasives présentes dans les liquides de polissage.

Le retrait de la matière par la conjugaison d'une action chimique et mécanique est assuré par une solution abrasive qui s'écoule entre la plaque et le tissu de polissage et par une pression appliquée sur la tête de polissage, qui presse de son côté la face avant de la plaque contre le tissu de polissage. Les rotations s'effectuent dans le même sens pour une raison d'uniformité de polissage. Enfin, pour but de retirer les résidus de polissage, l'étape finale de nettoyage est constituée d'un bain chimique, de brosses et d'un dispositif de séchage [104].

Singh et al. proposent une liste des paramètres physiques, chimiques et mécaniques qui jouent le rôle dans le processus d'enlèvement de la matière [105]. Les paramètres d'entrée sont tous les propriétés imposées par l'opérateur tels que :

- Caractéristiques liées aux particules en suspension (taille moyenne, distribution des tailles, forme, propriétés mécaniques, chimie, dispersion, concentration, etc.).
- Caractéristiques liées à la chimie des slurries (oxydants, stabilisateurs de pH, agents complexant, dispersants, concentrations, pH, inhibiteurs de corrosion, etc.).
- Caractéristiques du pad (propriétés mécaniques, rugosité, ravivage, vieillissement, etc.).
- Caractéristiques du wafer (dimensions et densités des motifs, etc.).
- Pression appliquée sur le wafer.
- Vitesse linéaire.
- Débits des slurries.
- Température.

Les paramètres de sortie sont les conséquences des paramètres d’entrée, mesurés au cours ou après le polissage tels que :

- Vitesse d'attaque (vitesse d'enlèvement de matière).
- Aplanissement.
- État de surface.
- Sélectivité.

La figure 26 représente une carte générale des paramètres qu’on peut appliquer ou mesurer dans le procédé de la CMP afin de polir ou planariser la surface du matériau [106].

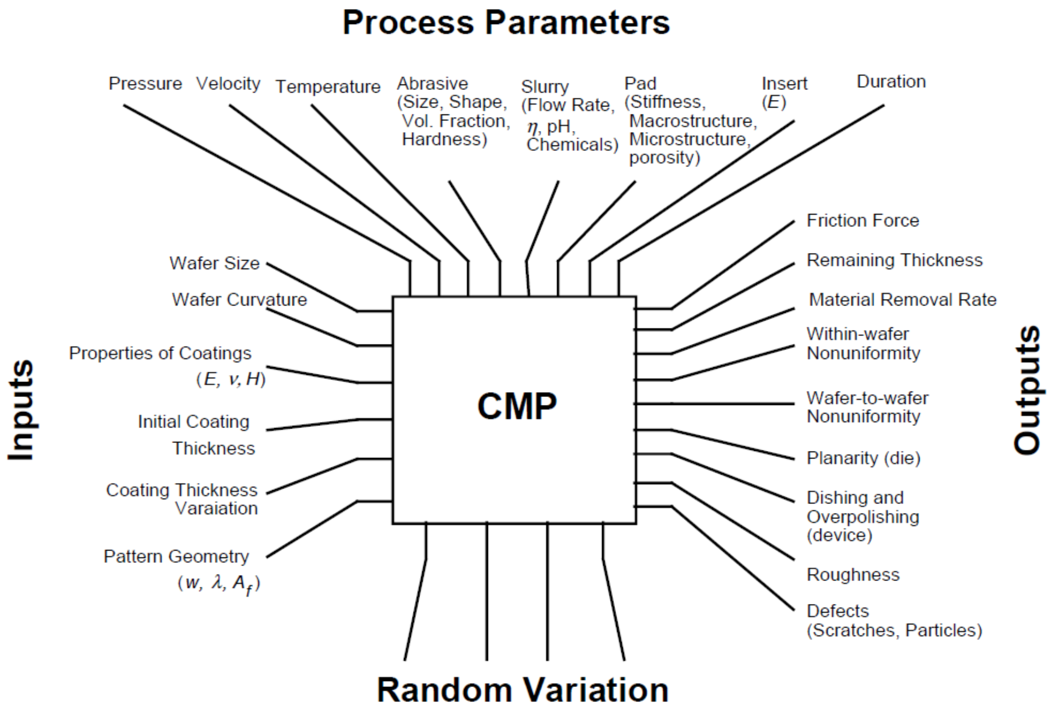


Figure II 26: Complexité du procédé de CMP [106]

L’influence des paramètres d’entrée varie selon les dimensions caractéristiques. On peut distinguer donc des aspects macroscopiques reliés aux Pad (pression sur le pad, particules sur le pad), concentrations chimiques des slurries ou le mode de contact (élastique ou hydrodynamique). Les aspects nanométriques tel que la rugosité; se produisent à l’échelle de l’atome et sont contrôlés principalement par les slurries (attaque chimique et abrasion mécanique) [107]. Donc, on s’intéresse dans cette partie à étudier les différents types des slurries utilisés dans l’industrie de Ge afin de réduire la rugosité de la surface et rendre le wafer prêt pour l’épitaxie.

Rajiv et al. ont classé les solutions chimiques utilisées dans la CMP selon leurs réactivités avec la surface [108] : les oxydants par exemples sont responsable de la transformation du matériau a son oxyde. Cette transformation est nécessaire car elle facilite le décapage du matériau par abrasion. Les surfactants sont des agents tensioactifs qui varient la tension superficielle du liquide et protègent la surface de l’agression des grosses molécules. Le bon contrôle des sels qui sont à l’origine des résidus de la synthèse du surfactant peut influencer aussi le polissage. La température peut activer certaines réactions chimiques et enfin, la taille, la concentration et la composition des particules abrasives peuvent réduire les dommages à la surface et augmenter la vitesse d’enlèvement.

II.7.2 État de l’art sur la CMP du Ge

Le germanium est un matériau relativement difficile à polir qu'il soit sous forme massive (Ge Bulk) ou obtenu par hétéroépitaxie sur un substrat en silicium, en particulier lorsque on cherche à obtenir un état de surface compatible avec l’épitaxie. L'intégration de CMP dans le procédé de fabrication de Ge est considéré comme étape essentielle dans plusieurs technologies de pointes comme : La technologie Smart Cut^{TM} pour produire des wafers de Germanium-On-Insulator (GeOI) [109],[110], la croissance épitaxiale de Ge sur des substrats de silicium [111]. Cette dernière est plus complexe à cause de la formation des dislocations à l’interface entre le substrat et la couche de Ge qui se traduit par l’apparition de défauts à la surface de Ge ou bien par l’apparition du réseau cross-hatch [112] ou sinon par la perturbation de la surface par porosification électrochimique dans le cas de notre procédé. Ces défauts augmentent la rugosité de la surface de la couche de Ge épitaxiée. En plus, l'absence d’une bibliographie complète sur le polissage mécanochimique de Ge est un autre obstacle pour la fabrication réussie de dispositifs basés sur Ge. Notant que les recettes de finition par CMP d'une couche de silicium d'une structure SOI obtenue par la technologie Smart Cut™ ne sont pas compatible avec le Ge [113]. En effet, le taux d'enlèvement de la matière obtenue avec ces procédés sur le silicium diminue d'au moins d'un facteur 5 lorsqu'il s'agit de germanium.

Le procédé de CMP le plus couramment utilisée dans le cas de Ge est une solution de polissage contenant à la fois un agent (NH_4OH) apte à attaquer chimiquement la surface de la couche et des particules de silice aptes à attaquer mécaniquement la surface. Il existe, par conséquent, un besoin d'améliorer la vitesse d'enlèvement ainsi que le niveau de rugosité de surface lors du polissage des couches de Ge.

Les chercheurs dans le passé ont utilisé des sleurries à base de (KOH et silice colloïdale) pour le polissage Ge et ont constaté que les taux d'enlèvement étaient faibles [114].

Les sleurris à base de composé Alcalins et de particule de Silice abrasif ont été élaborés dans un premier temps pour la CMP de Ge [115]. Ce processus a montré ses limites immédiatement, il a été rapporté qu'après environ une semaine de la préparation, les particules de silice se précipitent dans la solution probablement en raison de l'agglomération de la silice. Les dommages sur les échantillons étaient graves et les rayures dans la surface polie étaient clairement observées.

L'intégration des dérivées de cellulose pour empêcher l'agglomération de la silice dans cette solution a été proposé par Tredinnick et al. Cependant, cet additifs augmente la visquosité de la solution et ralenti la vitesse de polissage [116].

Les sleurris à base de HCl et NH_4OH contant des particules abrasives d'Al ont été utilisé pour éliminer une couche sacrificielle de Ge dans un système MEMS [117]. L'épaisseur de Ge a été réduite de 2µm à 100 nm mais les mécanismes d'enlèvement n'ont pas été discutés en détails.

Le polissage sélectif de Ge dans des tranchés de SiO_2 dans la configuration (Aspect Technique Ratio) a été étudié par Hydrick et al. [118]. Le polissage a été fait en utilisant des particules de silice colloïdale (Nalco 2350) et des additifs comprenant des oxydants (NaOCl et H_2O_2) et de NH_4OH pour améliorer le taux d'élimination de Ge. Ces sleurries ont fournit des taux d'enlèvement de Ge acceptables mais le phénomène de Dishing était majeur. Le mélange constitué de Nalco 2360, H_2O_2 et l'eau di-ionisée montre un faible Dishing, une faible contamination par des métaux (enlevé par H_2O_2), et un aplatissement des structures très efficace [118].

Deux autres solutions ont été testées par Peddeti et al. de IMEC [119] composée de i) 12% de particules de silice + 0,5% de H_2O_2 à pH 2 et ii) 3% de particules de silice colloïdale +

1% H_2O_2 + 0,2 M KNO_3 + 0,1 mM de cétyl triméthyl bromure d'ammonium à un pH de 8. Les valeurs de rugosité obtenues par la première solution sont de l'ordre de ~0.3 nm alors que la deuxième solution présente un Dishing sur les tranches de Ge entre SiO_2. Cette étude montre une rugosité acceptable mais les paramètres d'entrée ne sont pas bien détaillés.

II.7.3 Le mécanisme décapage de Ge par CMP

Bien qu'il existe une étude approfondie sur la vitesse de gravure de Ge dans diverses solutions chimiques faite par IMEC [120], les sleurries à base de H_2O_2 sont les plus utilisées dans la CMP de Ge [121], [122]. Contrairement au Si la vitesse de gravure de Ge est significativement plus grande. Cela est dû au fait que le Si forme un oxyde mince (SiO_2) qui passive la surface lors de la CMP dans les solutions d'oxydation (H_2O_2, eau ozonée). Ce SiO_2 limite alors la vitesse de gravure du silicium dans ces solutions. GeO_2 est solubles dans l'eau, de telle sorte qu'en présence d'H_2O_2, le Ge est oxydé et immédiatement attaquée par l'eau. Les particules abrasives décapent d'une façon homogène l'oxyde de Ge formé selon la figure 27 pour produire de faible niveau de rugosité:

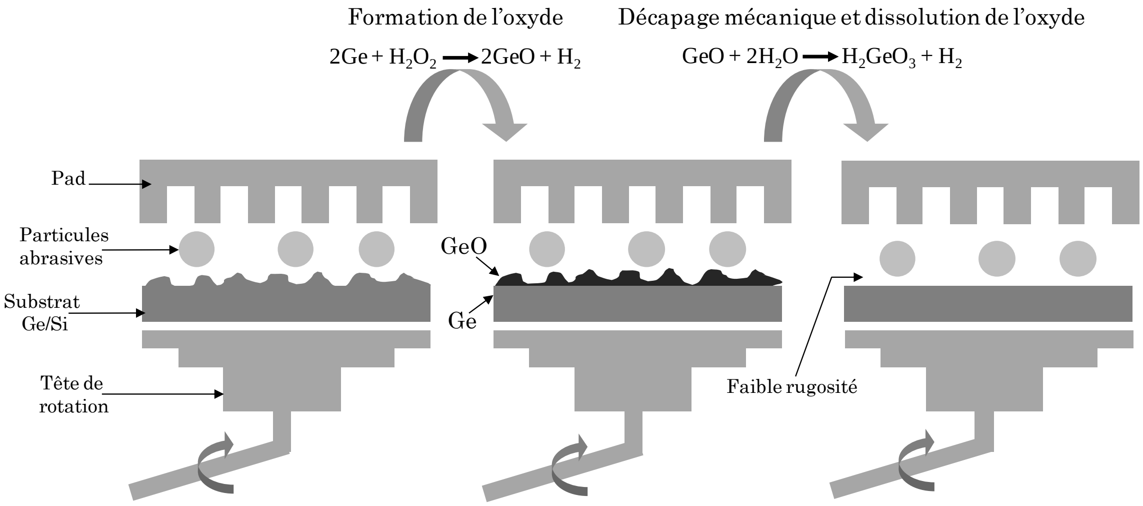


Figure II 27: Mécanisme mécano-chimique d'enlèvement de Ge par CMP

II.7.4 Le procédé de CMP de SOITEC

SOITEC propose une solution pour le polissage des couches de germanium ayant une vitesse d'enlèvement croissante tout en permettant de réduire encore le niveau de rugosité présent à la surface de couches de germanium [123], [124].

(1) Étapes du procédé

La première étape du polissage est réalisée sur une couche de germanium sacrificielle avec une solution de polissage présentant un pH acide.

- Le but de cette étape, dans un premier temps, est d'enlever suffisamment de germanium pour éliminer les défauts de surface issus de la croissance épitaxiale de la couche de germanium et réduire en partie la rugosité de surface.
- Cette étape est réalisée avec un tissu de polissage dur ayant un premier taux de compressibilité compris entre 2% et 4%.
- Lorsque la première étape de polissage est effectuée avec un tissu très dur, le cross-hatch disparaitra mais non pas la microrugosité.
- La première solution de polissage comprend des particules de silice ayant un diamètre compris entre 40 nm et 60 nm avec une concentration de particules de silice de 30%.
- La première étape de polissage: $V_{\text{tête}}$ comprise entre 75 et 95 tours/mn, préférentiellement 87 tours/mn. V_{plateau} comprise entre 85 et 100 tours/mn.
- La vitesse d'enlèvement lors de la première étape de polissage est d'environ 1,5 nm/sec et la durée de la première étape est d'environ 2 minutes.

Une deuxième étape de polissage mécano-chimique de la couche de germanium est réalisée avec une deuxième solution de polissage présentant un pH basique.

La deuxième étape de polissage permet de réduire significativement la microrugosité et la microrugosité de surface de la couche de germanium.

- La deuxième étape de polissage mécano-chimique est réalisée avec un tissu de polissage ayant un second taux de compressibilité compris entre 5% et 9%.
- La seconde étape de polissage permet de réduire la microrugosité globale à un niveau plus faible que dans le cas d'un procédé visant à minimiser la microrugosité directement en une seule étape, ce qui ne permet pas d'éliminer le cross-hatch complètement.
- Lors de la deuxième étape de polissage, la solution de polissage comprend des particules de silice ayant un diamètre compris entre 30 nm et 40 nm avec une concentration de particules de silice de 28%.

- La deuxième étape de polissage; V$_{\text{tête}}$ comprise entre 30 et 45 tours/mn, préférentiellement 36 tours/mn. V$_{\text{plateau}}$ comprise entre 25 et 40 tours/mn.
- La vitesse d'enlèvement lors de la seconde étape de polissage est de 0.5 nm/sec et la durée de la deuxième étape est d'environ 2 minutes.

Paramètres	**1 étape**	**2 étape**
Tissus (Pad)	dur	/
Pression	2% à 4%	6%
Diamètres des particules	40 nm à 60 nm	30 nm à 40 nm
pH	acide	basique
Concentration de sleurry	30%	28 %
Vitesse de la tête	75 à 95 tours/min	30 à 45 tours/min
Vitesse du plateau	85 à 100 tours/min	25 à 40 tours/min
Durée de l'étape	2 min	2 min
Vitesse d'enlèvement	1.5 nm/sec	0.5 nm/min

Tableau II 2: Tableau récapitulatif du procédé de CMP Soitec.

(2) Analyse de la rugosité

La figure 28 montre les valeurs de la rugosité obtenues par AFM sur des surfaces de dimensions variables ce qui présentent différentes fréquences spatiales. La courbe montre que le polissage réalisé en une seule étape correspondant à la première étape du procédé SOITEC corrige très bien la rugosité pour les grandes surfaces (rugosité RMS proche de 2 Â) tandis que la rugosité sur les petites surfaces reste importante (rugosité RMS de l'ordre de 4 à 5 Â pour des mesures au microscope à force atomique (AFM) sur des surfaces de balayage de 2x2 μm^2 et de 10x10 μm^2).

La courbe B montre que l'on obtient l'effet inverse lorsque le polissage est réalisé toujours en une seule étape mais avec une solution de polissage correspondant à celle utilisée lors de la deuxième étape de polissage du procédé SOITEC. En effet, ce polissage corrige très bien la rugosité pour les petites surfaces (rugosité RMS proche de 2 Â) tandis que la rugosité relevée pour les mesures des grandes surfaces reste importante (rugosité RMS de l'ordre de 4 à 5 Â pour des mesures au microscope à force atomique (AFM) sur des surfaces de balayage de 500*500 μm^2).

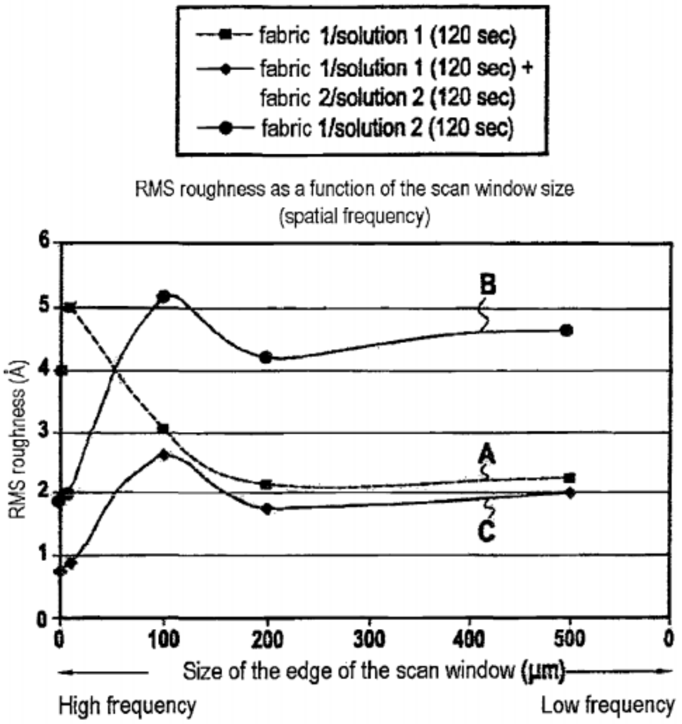


Figure II 28: Évolution de la rugosité pour la première étape du procédé de CMP Soitec (A), la deuxième étape (B) et les deux étapes ensemble (C) [123].

Enfin, la courbe C montre que le polissage en deux étapes permet d'obtenir un bon niveau de rugosité à la fois pour les mesures les petites ou les grandes surfaces. Plus précisément, on obtient, après le polissage en deux étapes, une microrugosité et une macrorugosité de surface qui sont de l'ordre de 0.1 à 0.2 nm RMS, et ce quelle que soit la longueur d'onde spatiale.

(3) Conséquences du procédé SOITEC

- En utilisant une solution de polissage ayant un pH acide lors d'une première étape de polissage mécano-chimique, on obtient une vitesse d'enlèvement du germanium bien plus élevée qu'avec une solution de polissage habituellement utilisée pour ce type de matériau, à savoir une solution ayant un pH basique.
- Lorsque la première étape de polissage est effectuée avec un tissu très dur, il s'avère que le cross-hatch disparaît réellement. L'ensemble des deux étapes du procédé permet d'éliminer de façon plus efficace à la fois le réseau de contraintes appelé "cross-hatch" ainsi que la microrugosité et la macrorugosité de surface.
- La structure à polir selon ce procédé peut comprendre une couche de Ge Bulk ou une couche de Ge hétéroépitaxiale sur un substrat de Si. Dans le cas d'une couche de Ge obtenue par hétéroépitaxie, la couche présente, après la deuxième étape de polissage mécano-chimique, une microrugosité de surface inférieure à **0,1 nm RMS** pour une mesure de rugosité réalisée au microscope à force atomique sur des surfaces de balayage de 2x2 μm^2.

Le procédé de polissage proposé par SOITEC permet en outre d'obtenir des wafers de Ge/Si de très bonne qualité et de réduire, par conséquent, le nombre des wafers déclassées.

Grâce au procédé, on atteint une qualité de surface de germanium remarquable, notamment en ce qui concerne les phénomènes de cross-hatch et de micro et macrorugosité, qui permet de reprendre directement l’épitaxie sur Ge.

CHAPITRE III ARTICLE : GERMANIUM MÉSO-POREUX : DÉVELIPPEMENT ET MISE-À-L’ÉCHELLE

III.1 Avant-propos

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Titre français : Synthèse de croissance rapide de films de germanium mésoporeux par gravure électrochimique bipolaire à haute fréquence

Contribution au document : Cet article contribue à la thèse en démontrant la synthèse de Ge mésoporeux. Il introduit une nouvelle technique de fabrication et explique son intérêt. Cet article présente donc le développement du matériau de base pour la thèse.

Résumé français :

Il a été mentionné que le germanium mésoporeux (MP-Ge) jouerait un rôle important dans un large éventail d'applications potentielles. Ces réseaux de Ge poreux sont distingués par des propriétés physiques et chimiques particulières par rapport à son homologue en vrac. Pendant plus de deux décennies, les méthodes utilisées pour synthétiser ces matériaux étaient extrêmement lentes et produisent des couches non uniformes qui limitent leurs applications. Ici, nous démontrons la synthèse de films épais MP-Ge avec un taux de gravure élevé (jusqu'à 300 nm/min) en utilisant une densité de courant élevée avec une gravure électrochimique bipolaire à haute fréquence. Une procédure de nucléation optimisée est également rapportée qui permet une meilleure homogénéité latérale des films MP-Ge. Suite à ces résultats, un modèle de gravure électrochimique est proposé et confirmé par des mesures de spectroscopie infrarouge à transformée de Fourier et de voltampérométrie cyclique. Des mesures de réflectivité ont également été utilisées pour démontrer que l'indice de réfraction effectif de MP-Ge peut être ajusté en fonction de la porosité de la couche. Il a été réduit à 1,76 en raison de la présence des mésopores. Enfin, un capteur interférométrique à base de Ge poreux a été démontré, une sensibilité de détection de 711 nm/RIU a été mesurée lors de l'exposition à des solutions de glycérol-eau.

Fast growth synthesis of mesoporous germanium films by high frequency bipolar electrochemical etching

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KEYWORDS: Porous germanium, Bipolar electrochemical etching, Nucleation, Passivation, Refractive index, Sensing.

III.2 Abstract

Mesoporous germanium (MP-Ge) has been predicted to play an important role in a wide range of potential applications. These porous Ge networks are characterized by physical and chemical properties that contrast with their bulk counterpart. For more than two decades, the methods that were used to synthesize these materials were extremely slow and yield non-uniform layers, which limit their applications. Here we demonstrate the synthesis of thick MP-Ge films with high growth rate (up to 300 nm/min) by using high-current density and high-frequency bipolar electrochemical etching. An optimized nucleation procedure is also reported. It enables a much better lateral homogeneity of the MP-Ge films. Following these results a refined electrochemical Ge etching model is proposed. The model is confirmed by Fourier Transform Infrared Spectroscopy and Cyclic Voltammetry measurements. Reflectivity measurements were also used to demonstrate that the effective refractive index of MP-Ge can be adjusted as a function of layer porosity. It has been reduced down to 1.76 due to the presence of the mesopores. Finally, a basic interferometric porous Ge sensor is demonstrated, a detection sensitivity of 711 nm/RIU was measured upon exposure to glycerol-water solutions.

III.3 Introduction

Recently, germanium (Ge) nanostructures have attracted a lot of attention because of their unique physicochemical properties, which differ significantly from those of bulk crystals. Due to their unique and versatile properties, nanocrystals, nanowires and porous forms of Ge have the potential to be used in a broad range of applications such as electrochemical energy storage [125], [126], sensing [127], photovoltaics [128], microelectronics [129], and photonics [130]. Porous Ge is a very promising material and has been already leveraged for various uses, such as a template for epitaxial growth of III-V materials with high crystalline quality [131], a viable anode material of Lithium Ion Batteries [132] and has been predicted as an ideal candidate for thermoelectric applications [133]. Additionally, it was recently reported by Gerasimos et al. that mesoporous Ge (MP-Ge) with hexagonal pore ordering and very high surface area, exhibits strongly size-dependent optical properties as well as photoluminescence [134], [135]. Besides, near-infrared emission from MP-Ge formed by electrochemical etching is evidence that luminescence originates from quantum confinement effect [136]. Moreover, germanium has one of the largest refractive indices ($n \sim 4.0$) amongst classical semiconductors, making it a promising material for optical applications. The synthesis approaches to fabricate Ge nanoparticles [137], [138] and nanowires [139], [140] are well-established, but the routes to the large-scale manufacturing of porous materials are much less developed. Very few techniques are available to fabricate MP-Ge films by a variety of chemical and physical techniques, among them, spark processing [141], inductively coupled plasma chemical vapor deposition (ICPCVD) [142], Wet-chemical synthesis in a template mold [143], Se^+ and Te^+ ions implantation [144] or Ge^+ self-implantation [91], reduction alloying/dealloying approach [145] and electrochemical etching [146]–[149]. But mesoporous nanostructures fabricated from electrochemical etching have some distinctive advantages: (i) high density of nanocrystals, (ii) pure material (iii) low fabrication cost. Despite all these advantages, the use of the electrochemical etching process to produce self-assembled Ge nanostructures remains limited. This is mainly due to the poor lateral homogeneity of the process and the relatively low growth rate.

In the recent years, bipolar electrochemical etching (BEE) has been introduced for the fabrication of porous Ge layers [83], [150]. For this technique, the anodic polarization is used for etching, while a cathodic polarization is used for the passivation of the already formed mesoporous layer to avoid its dissolution [146]. Buriak et al. produced porous n-doped Ge layers with thicknesses in a range of 1 µm to 15 µm using highly concentrated HCl-based electrolytes diluted in ethanol [83], [84]. But, no structural details regarding the germanium layer were reported. A few years later, Föll et al. studied the nucleation and growth of n- and p-type porous Ge with various types of electrolytes, crystal orientations and doping concentrations [150]. However, the formation of MP-Ge layers with different morphologies by BEE have been reported for the first time by our group [147]. An optimized anodic/cathodic sequence was used and showed very diverse nanoscale morphologies which allowed the observation of size dependent photoluminescence [136], [147]. Once more, the importance of anodic/cathodic ratio to engineer different morphologies has been reported [151]. But despite the effectiveness of BEE to form stable MP-Ge layers, etch rates obtained by this method on p-doped Ge are rather low, ranging between 15nm/min [152] and 50 nm/min [147]. So far, the etch rates obtained from the electrochemical etching of p-doped Ge are quite different from that of the n-doped type. For n-Ge, the material pore density, pore dimension and layer structure depend on the doping density and the crystallographic orientation of the wafer. However, for p-Ge, the holes are the majority carriers and are certainly omnipresent, which will lead to a uniform dissolution even without backside illumination [153]. As a consequence, etch rates during porous p-Ge formation is very slow, which is a major drawback, making the synthesis of MP-Ge time consuming and thereby preventing its large-scale deployment in many industrial processes.

In this paper, we introduce a new technique called fast bipolar electrochemical etching (FBEE) to fabricate thick MP-Ge films with high growth rate (above 300nm/min). Additionally, we demonstrate an optimized procedure for nucleation that allows an enhanced uniformity in the pores formation and a much better lateral homogeneity of the MP-Ge films. Then, we propose a refined electrochemical model based on FTIR (Fourier Transform Infrared Spectroscopy) and CV (Cyclic Voltammetry) results. Finally, we report optical properties of MP-Ge layer by IR reflectivity measurements, as well as a first proof of concept of an optical interferometer device.

III.4 Experimental section

Galvanostatic etching of germanium has been performed in a two-electrode electrochemical cell with a Pt wire counter electrode. The p^+ type Ge wafers are (100) oriented with a 6° miscut and have a nominal resistivity of 0.025 Ω.cm. The electrical contact was ensured by pressing the backside of the sample on a gold-coated copper electrode. The electrolyte is a 5:1 mixture of hydrofluoric acid (49%) and anhydrous ethanol. Two types of experiments are reported in this study, namely fast bipolar electrochemical etching (FBEE) and the conventional bipolar electrochemical etching (CBEE), which is used as a reference as shown in Figure 1. Both experiments are conducted for a total duration of 40 min. For the FBEE, the current densities of anodic and cathodic pulses and their duration are respectively 20 mA/cm^2 for 0.04s and $-60 mA/cm^2$ for 0.04s. For the CBEE, the current densities of anodic and cathodic pulses and their duration are respectively 20 mA/cm^2 for 1s and -20 mA/cm^2 for 1s. The morphology and thicknesses of the porous layers are extracted from the Scanning Electron Microscopy (SEM) pictures and the bulk porosity is determined by gravimetric measurements and IR reflectivity. All spectra were recorded with a VERTEX 80/80v FTIR spectrometer using a Globar source, a KBr beam splitter and a MCT D15 detector. The spectral resolution in transmission mode was 2.0 cm^{-1} with a total scanning time of 5 min. For FTIR microscopic reflectance analysis, a standard 15x objective is used with gold surface as reference. Cyclic Voltammetry (CV) was performed using an O-ring electrochemical cell. This cell consisted of a Teflon bath with a classical three-electrode arrangement: p-Ge substrate as a working electrode (WE), counter electrode (CE) being Pt wires and a saturated calomel reference electrode (SCE) HF resistant. The best results were obtained with an electrolyte consisting of 49% HF at 2°C.

III.5 Results and discussion

III.5.1 MP-Ge morphologies by CBEE and FBEE

The lateral homogeneity of porous Ge layers is of paramount importance for future applications of this material. Homogeneous porous Ge layers can be in many cases challenging to obtain as can be seen in Figure 2a. Possible reasons for this inhomogeneity are a random initiation due to current lines, which pass preferentially through defects on the surface where the local electric field is amplified as shown in Figure 2c. To circumvent this type of nucleation, we propose to use a controlled nucleation step, which consists to apply a higher direct current for 10 seconds before alternating current; this procedure forces the nucleation of uniformly distributed mesopores as shown in Figure 2d. The result of this procedure is shown in Figure 2b; we can clearly see a high difference of porous Ge spot quality after the initiation step. Similarly, all the experiments that will be reported hereafter are obtained after using this optimized nucleation procedure.

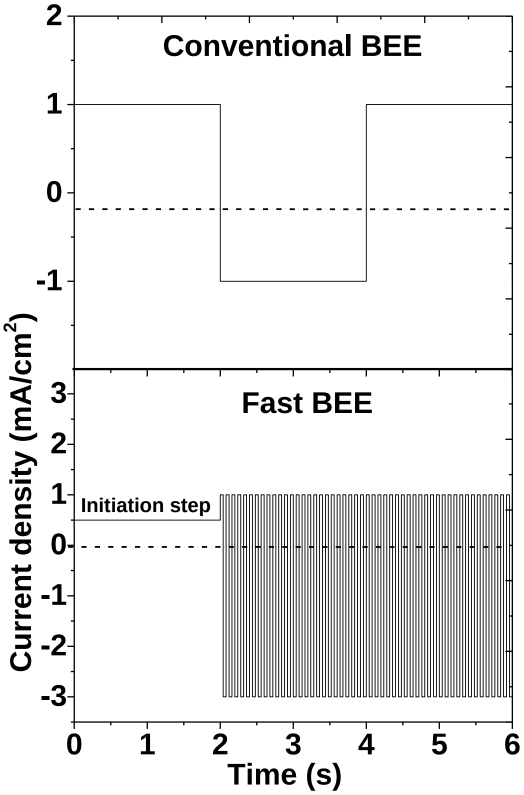

Figure III 1: Electrical etching regime of Conventional BEE and Fast BEE (note that in FBEE, the switching time is much faster than CBEE).

To compare FBEE with CBEE regime, two samples have been fabricated during 40 min under the conditions described above. Results in Figure 3b show that for FBEE, the thickness of the layer is approximately 6 µm with a porosity of 53%, whereas in CBEE, we observe a total dissolution of porous Ge in HF electrolyte with thick, high-porosity spongy layer. In the case of FBEE regime, the achievement of high thickness with moderate porosity by using a high cathodic current can be explained by an enhanced surface passivation in comparison to the classical regime. Such a passivated surface presents an energy barrier for the charge transfer across the germanium-electrolyte interface and thus inhibits the uniform dissolution of Ge [152].

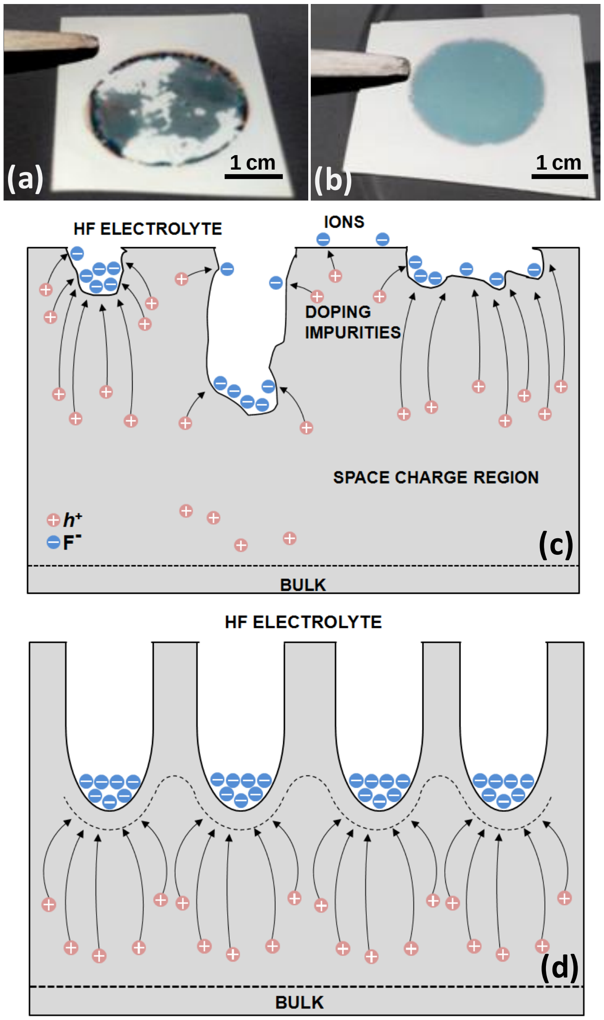

Figure III 2: Electrochemically etched (100) p-Ge sample (a) without DC nucleation, (b) with DC nucleation. Schematic models of (c) random initiation and (d) controlled initiation.

To further investigate this effect, we report a detailed study of FBEE and CBEE regimes as a function of current density. Figure 4a shows cross-sectional SEM images of three porous wafers fabricated with different current densities: (α) 3.8 mA/cm^2, (β) 7.5 mA/cm^2 and (γ) 20 mA/cm^2 by FBEE with $t_\alpha = 0.2$s, $t_\beta = 0.1$s and $t_\gamma = 0.04$s, so that the total charge exchange rate remains the same (~1mA.s).

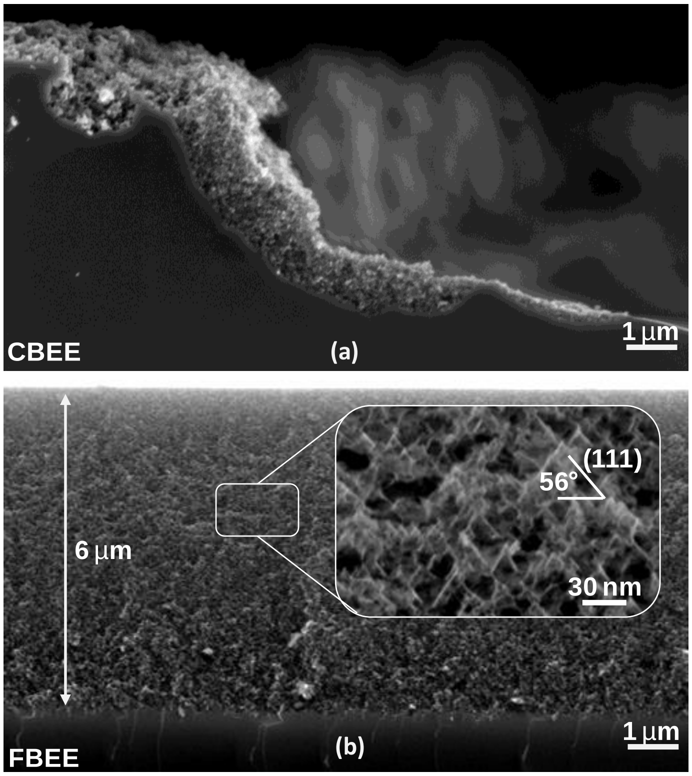

Figure III 3: Cross-section SEM images of MP-Ge layers formed at 20mA/cm2 by (a) Conventional BEE, (b) Fast BEE technique.

For all samples, we observe uniformly distributed mesopores. We also notice diamond-like shaped pores following the <111> directions with sizes of several nanometers, which seems to increase with current density as shown in Figure 4c. The pore morphologies, as depicted in Figure 4d, display few general trends: (i) As porous Si [154], the pore diameter increases with increasing current density. The same anisotropic etching was also observed in Ge by using H_2O_2 containing solutions [155] and in Si by using laser beams etching [156]. It was found that the anisotropic character of the etching process is manifested by the fact that (111) surfaces are etched at a much slower rate than all other crystallographic planes. Another experiment shows that the (100) planes are etched 50 times faster than the (111) planes [157]. (ii) The pore density (D) was therefore approximated from the observed pore diameter (d) and the porosity (p) using: $D=p/\pi d^2$.

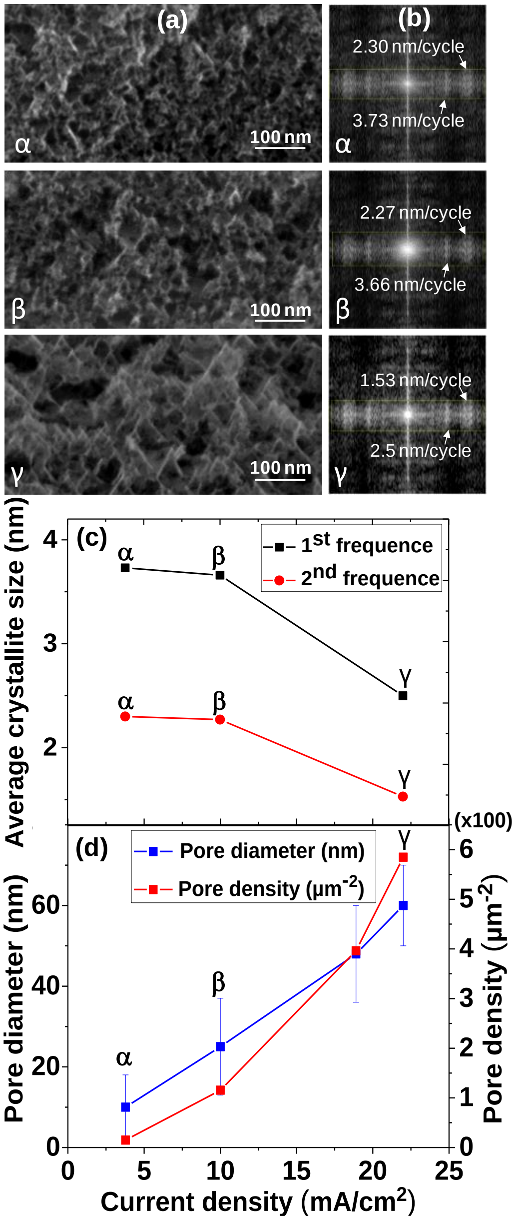

Figure III 4: Cross-section SEM images of MP-Ge layers formed by fast BEE technique with the same charge quantity=1mA.s in pure HF49%, EthOH (5-1) electrolyteat (α) 3.8 mA/cm^2, (β) 7.5 mA/cm^2 and (γ) 20 mA/cm^2 with pulse durations fixed to 0.2 s, 0.1s and 0.04 s respectively. (b) The FFT power spectrum calculated by ImageJ software of SEM images. (c) Average crystallite size by FFT of different samples. (d) Pore density and pore diameter versus etching current density.

A plot of the pore diameter and pore density versus etching current density is reported in Figure 4d. A quasi-linear dependence of mesopore density on current density is observed.

Note that (D) is approximated assuming a diamond shape and unbranched pores of diameter (d). Other pore shapes, side pores branching out of the main pore, or the presence of micropores contribute to the porosity, which leads to an underestimation given by the diamond shape. (iii) The determination of the average pore wall thickness suffers from similar approximations [158]. Average crystallite sizes of the same samples are obtained by FFT treatment of the porous Ge cross sectional images. Figure 4b shows that for (α) and (β) samples, crystallite size is below 2.3 nm and 3.7 nm. However, for sample (γ) where the applied current density is much higher (~ 20 mA/cm^2), the nanocrystallite size is ranging between 1.5nm and 2.5nm with a low aspect ratio. This highly controllable nanostructure size is below the Bohr radius of Ge and can emit above the bulk Ge bandgap, in the near-infrared range due to quantum confinement within the crystallites [136].

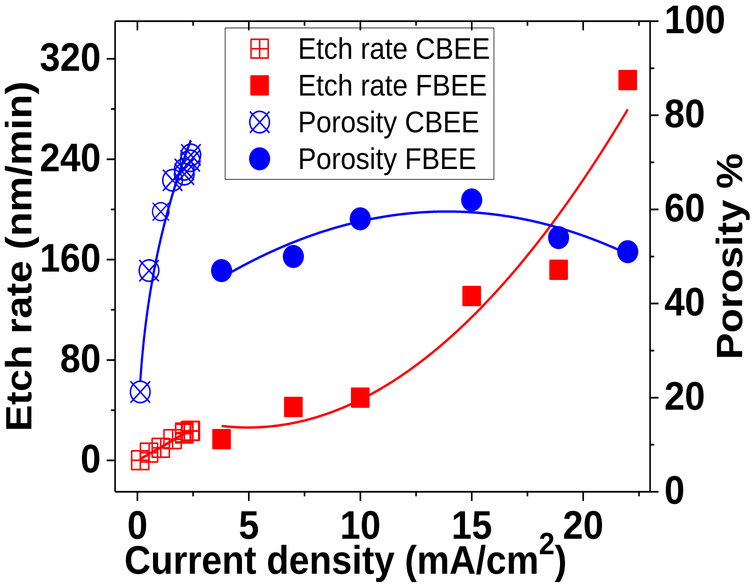

Figure III 5: Etch rate and porosity versus current density of MP-Ge layers formed by CBEE and FBEE regime. For FBEE, the switching time between Cath-Ano is adjusted to keep a constant charge density.

Figure 5 compares FBEE and CBEE in terms of etch rates and porosity for different etching current densities. By CBEE, porous Ge etch rate lies in the range 3 nm/min to 25 nm/min for etching current densities of 0.2 mA/cm^2 to 2,5 mA/cm^2. Specifically, the etch rate increases linearly with etching current density. We observe that, similarly to the anodization of p-type Si with the same substrate resistivity, the etch rate also increases with etching current density [159]. Exceeding 2.5mA/cm^2, Ge dissolves completely in HF which limits the formation of thick porous layer. In the case of FBEE, the layer morphology is well preserved at much higher current densities as illustrated in Figure 5. It shows also that porous Ge etch rate lies in the range 17 nm/min to 300 nm/min for etching current densities between 4 mA/cm^2 and 25 mA/cm^2. In particular, the etch rate increases exponentially with etching current density. On the other side, we observe that for CBEE, the porosity lies in the range 20 % to 92% for etching current densities of 0.2 mA/cm^2 to 2,5 mA/cm^2. The latter increases with etching current density until it exceeds 90% where electropolishing regime takes place. Interestingly, the dependence of the porosity in FBEE on the etching current density is not significant compared to CBEE where the porosity increases with etching current density [160] which explains the large stability domain of porous layer formation. This special case could explain why the ratio crystallite volume/pores volume is constant despite changing current density. The stable porosity is essential to increase the etch rate; these effects will be discussed in details in “Pore wall passivation mechanisms” section.

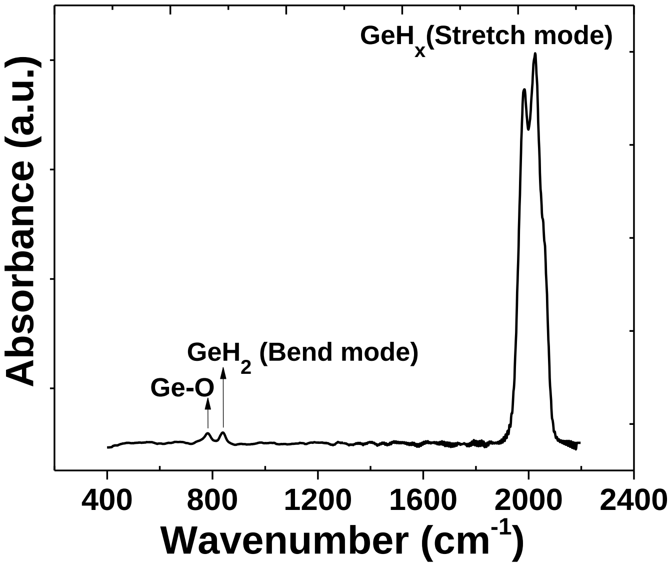

Figure III 6: Typical transmission-FTIR spectrum of MP-Ge layer fabricated by BEE technique in HF49%, EthOH (5:1) electrolyte at 20 mA/cm2 during 40 min using HF treated Ge bulk surface as reference.

III.5.2 Electrochemical-Chemical characterizations

In order to confirm and clarify the electrochemical mechanism of Ge during BEE, we present a chemical and electrochemical analysis by Fourier Transform Infrared Spectroscopy (FTIR) and Cyclic Voltammetry (CV) measurements. Figure 6 shows the absorbance obtained by Fourier Transform Infrared Spectroscopy of MP-Ge sample fabricated by FBEE with a current density of 20 mA/cm^2 in HF 49% electrolyte during 40 min. The dominant feature of this spectrum is at 2050 cm^{-1}, which corresponds to the stretching mode of the GeH_x bonds [161], [162]. GeH_x bending modes are also present and centered at 840 cm^{-1} [162]. The peak at 780 cm^{-1} is attributed to the vibration of Ge-O which forms after exposure to an ambient atmosphere [163]. The analysis of the GeH_x band shown in figure 7. was fitted using three Gaussian line shapes. This band appears to involve three components: a band at 1982 cm^{-1}, attributable to the mono-hydride stretch mode, a dominant band in the 2024 cm^{-1} originates from GeH_2 groups and a weaker band around 2060 cm^{-1}, attributable to the tri-hydride stretch mode [164], [165]. Because of the rough surface of MP-Ge (Fig. 7), such a varied H termination is expected, like in porous silicon [166]. Vibrational measurements show clear evidence that following the BEE process; the porous Ge surface is hydrogen-terminated and contains GeH_x bonds.

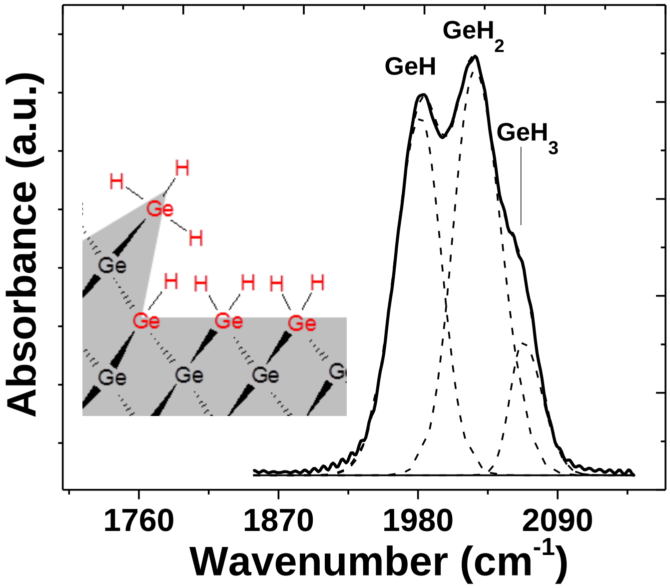

Figure III 7: Analysis of the νGeHx band in the transmission-FTIR spectrum of MP-Ge layer. The position of mono-, di-, and trihydride stretch modes are indicated. (Inset) Schematic view of the specific surface area of MP-Ge.

Cyclic Voltammetry (CV) is used to investigate electrochemical reaction mechanisms that give rise to the electroanalytical current signals. In addition, CV gives information on the chemical reactivity of species and a rapid qualitative elucidation of electrode reaction mechanisms. Figure 7 shows the voltammogram of p-Ge electrode (0.025 Ω.cm) at a scan rate of 50 mV s^{-1} in the potential range +0.5 V to -2.5 V/SCE. The I-V curves for p-type

Ge can be divided in three main regions: the electropolishing region [+0.5 V, 0 V], the pore formation region [0 V, -0.3 V] and the hydrogenation region [-0.3 V, -2.5 V]. Similar to Si, the electropolishing region has two sub-regions: non-oscillating and oscillating. The non-oscillating sub-region is mainly between 0 V/SCE and the oxidation peak, whereas oscillations are found after the oxidation peak [167]. These oscillations appear because: i) the measured voltage oscillates in time (in the galvanostatic regime) or ii) the measured current oscillates in time (in the potentiostatic regime) [167]. Overall, the positive end of the anodic loop overlaps with the onset of germanium oxidation and dissolution [168].

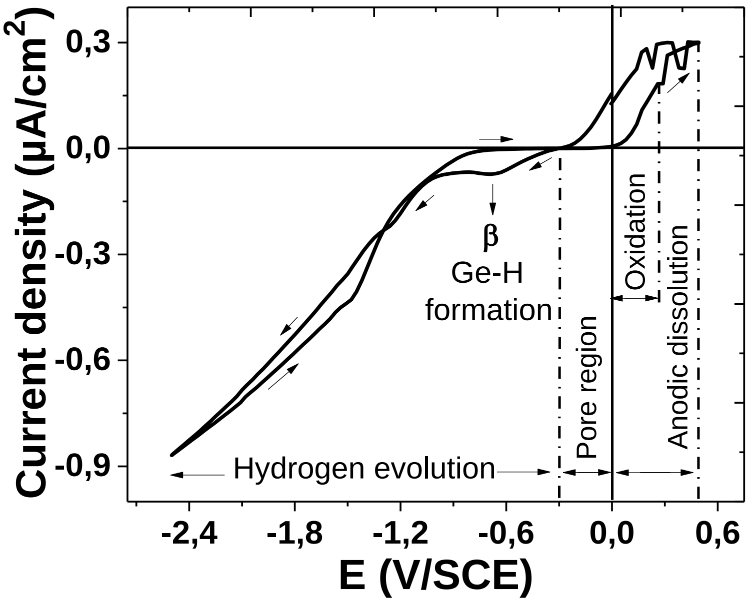

Figure III 8: Cyclic voltammogram of a p-type Ge-electrode (2.5E-2 Ω cm) at 0.5 V s^{-1}, in 49%HF at 2 °C and with a Pt wire electrode. (Electrode potential measured against satd. calomel electrode).

For the hydrogenation region, scanning in the cathodic direction reveals two negative peaks at -0.65V/SCE and -1.2V/SCE. Memming et al. have shown that there are two current peaks (α and β) responsible of the formation of a Ge-H surface depending on the crystal planes exposed to the electrolyte [168], [169]. In our case, a (100) plane (miscut 6°), only one peak (β) appears clearly at -0.65V/SCE. Therefore, it can be inferred that the β peak is typical for the formation of hydride groups on the (100) surface. The peak at -1.2 V/SCE is not related with the formation of a germanium hydride surface. It may be correlated with the formation of hydrogen adsorbed on the Ge-H surface [170]. Finally, the cyclic voltammogram of p-type monocrystalline Ge electrode in HF electrolyte exhibits two loops corresponding to a back-and-forth change of the surface chemistry between a hydroxylated state and a hydrogenated state, which confirms that during the sweep of cathodic current in BEE, the hydroxide surface is converted into a hydride surface.

III.5.3 Electrochemical mechanism

Two reactions pathways for the electrochemical dissolution of germanium in HF are discussed in the literature, based essentially on the calculated valence number of the reactions [171]. We notice divalent anodic dissolution [170] and tetravalent anodic dissolution [147] depending on the applied potential [172]. The divalent reaction:

$$Ge + 4HF_2^- + \ h^+ \ \rightarrow GeF_6^{-2} + 2HF + \ H_2 + \ e^- \quad (1)$$

takes place below 0.15 V [51] and foresees hydrogen formation. The tetravalent reaction:

$$Ge + 6HF + 4h^+ \ \rightarrow \ H_2GeF_6 + 4H^+ \quad (2)$$

takes place above 0.15 V. These mechanisms are in agreement with Batenkov results [173], who observed two slopes on the same Tafel curve correspond to two different electrochemical reactions taking place at different potentials values [152]. In our case, all the values of dissolution valence number calculated using Faradays law for CBEE [152] and FBEE are greater than 4. Based on this result, the tetravalent dissolution mechanism seems to dominate in these regimes. In highly concentrated HF medium, the strong polarity of the Ge-F bond (465kJ.mol^{-1}) promotes the substitution at Ge centers upon nucleophilic attack and hence is kinetically very labile [84].

As shown in Figure 9, during anodic etching, the first chemical change that occurs is the replacement of chemisorbed H atoms with chemisorbed F atoms. A hole from the Ge bulk approaches the surface where F$^-$ ions are present, which enables the nucleophilic substitution of a H atom by a F atom. Whereas, the high electronegativity difference between Ge and F moves the electronic cloud, pulling out the Ge atom, which helps other

F- ions, attacks to release an atom from the surface. Consequently, Ge atoms are separated from the surface as GeF_4 following:

$$Ge + 4F^- + 4h^+ \rightarrow GeF_4 \quad (3)$$

GeF_4 quickly transforms in HF electrolyte to the H_2GeF_6 compound (GeF_6^{-2}: $2H^+$) following:

$$GeF_4 + 2HF \rightarrow H_2GeF_6 \quad (4)$$

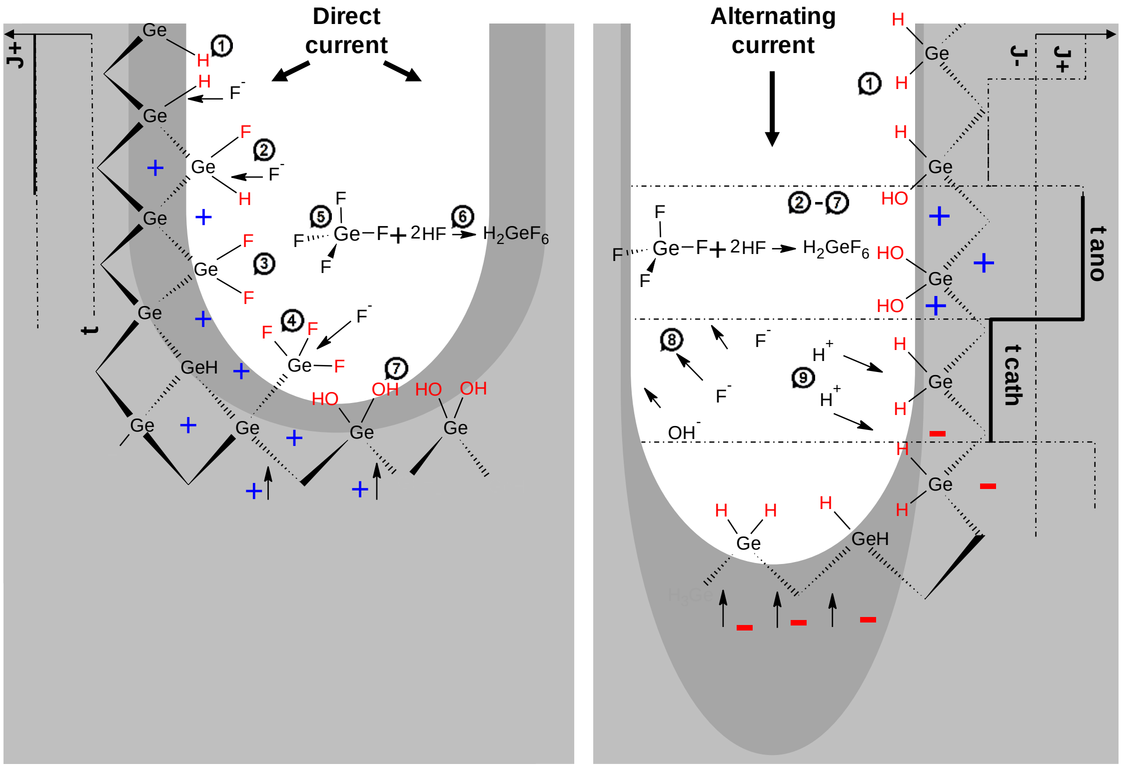

Figure III 9 : Step by step electrochemical porosification mechanism of Ge in HF medium by: (left) direct current: (1) H-passivated Ge in HF without anodic current, (2) F^- ions attack the Ge-H bonds, (3) F-passivated Ge in the presence of holes, (4) Pulled out Ge from the bulk, (5) Ge-Ge bonds breaking and GeF_4 molecule release, (6) GeF_4 transformation in HF electrolyte, (7) OH-passivated Ge in the presence of holes. (right) Alternating current (BEE technique): (1) H-passivated Ge, (2-7 steps) anodic etching, (8) repulsed negative charges, (9) cathodic passivation in the presence of electrons and Ge-H bonds formation.

In terms of morphology, the application of a direct current produces porous Ge layers with low thickness and very high porosity, followed by the total dissolution called the electropolishing regime [148] as shown schematically in Figure 9. However, with alternating current, in the anodic section, the reaction stated in equation 3 will take place.

But in the cathodic section, injecting a high negative current (3 times higher than the anodic current) repulses all negative charges at the electrolyte/Ge interface (F^-, OH^-) and promotes the hydrogenation of the surface [82], [168] according to:

$$= Ge(OH)_2 + 4e^- + 4H^+ \rightarrow = GeH_2 + 2H_2O \quad (5)$$

This description is in accordance with the voltammetric loop observed on a Ge electrode surface, which undergoes reversible changes between a hydroxylated and a hydrogenated state by switching from positive to negative current [165].

III.5.4 Pore wall passivation mechanisms in CBEE and FBEE regimes

Similarly to porous Si formation, the formation of a porous Ge requires a mechanism that locally stops the dissolution reaction at the pores walls, whereas the etching process continues at the pores tips [174]. Several physical and chemical phenomena can contribute in the passivation mechanism of porous semiconducting materials, among them: (i) the quantum confinement (QC) effect in which the band gap increases by reducing the crystallites size and causes a partial depletion of holes in the porous region [175]. The condition for the total depletion of the walls is, that their thickest parts are smaller than two times the space-charge region width [176]. So, the porous structure remains undissolved [177]. (ii) In contrast to QC which is only present in the confined pores walls, the formation of a space charge region (SCR) at the pore tips requires a mechanism of passivity breakdown that explains the remarkable stability of the pore walls against dissolution [178]. (iii) In porous Si, anodic oxidation can therefore be excluded as a possible cause for pore wall passivation [179]. Note that QC and SCR passivation apply not only to Si but are widespread for all semiconducting electrodes.

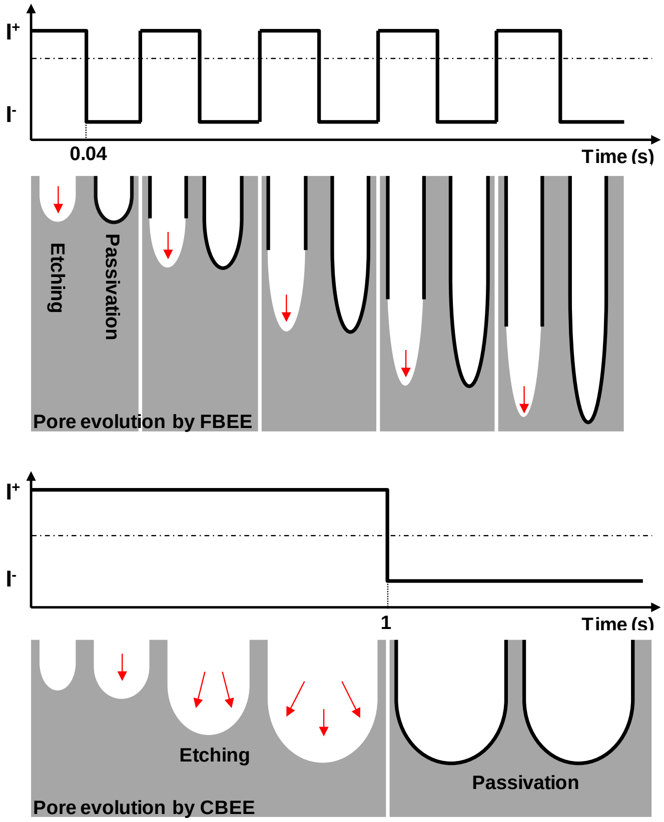

Figure III 10: Pore shape evolution model pending in: (top) FBEE and (bottom) CBEE.

However, another type of passivation is usually specific to a certain electrode material as Ge. The chemical passivation consists to create the necessary conditions such as: cathodic current [180] and cathodic pulses duration [147] to form a hydrogen monolayer at the surface during cathodic bias. This layer presents an energy barrier for the charge transfer across the Ge electrolyte interface [84], [150]. The work of Buriak *et al.* on the passivation of porous germanium layers during the electrochemical etching confirmed the hydrogen termination of Ge which is strongly resistant to oxidation [83]'[181]. In this context, Figure 9 illustrates the difference in the pore morphology by changing switching time in CBEE and FBEE regimes. In the case of CBEE, a switching time of about 1s is used for cathodic and anodic pulses respectively, which for high current density implies a significant amount of Ge etching which erases the pore walls passivation and thereby promotes the dissolution of the already formed porous Ge layer. However, in the case of FBEE, the anodic step duration is too short as compared to the characteristic lifetime of hydrogen passivation of the pore walls what will prevent the layer dissolution and promote the pore growth at the pore tip. By taking advantage of this regime, a tunable high pores growth rate is obtained, while maintaining a good passivation of the Ge layers with moderate porosity.

III.5.5 Optical properties

It has been shown that the porosification is an efficient tool to tune the refractive index of Si [31-33]. The nanoscale modulation of material properties such as porosity and morphology opens interesting perspectives for the realization of a large variety of optical devices such as Fabry-Perot cavities [182], [183], Bragg mirrors[184], waveguides [185], or photonic crystal structures [186]. The extremely large internal surface area of the germanium sponge-like structure, its high refractive index (4 in the infrared), low cost, and compatibility with standard microfabrication technology provide significant advantages for the development of smart sensing devices. To investigate the sensing performance of the single porous germanium layer fabricated by BEE, critical parameters such as the physical thickness and the refractive index (or porosity) should be considered. Light reflected from the top interface (air/MP-Ge) and the bottom interface (MP-Ge/Ge substrate) interfere with each other and display the typical Fabry-Perot fringes in the reflectance spectrum shown in Figure 10.

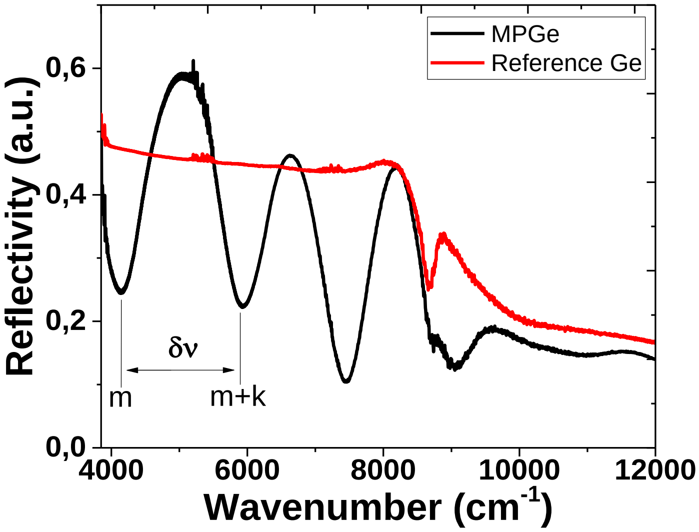

Figure III 11: Reflectivity spectra of a reference Ge substrate and a MP-Ge layer fabricated by FBEE technique with a thickness of 1.8µm and a porosity of 70%.

The interference pattern is used to determine the refractive index of the film with the following expression:

$$\mathrm{n}_{MPGe} = {}^{k}\!/_{(2.\,\delta\nu.\,\mathrm{t})} \quad \text{Eq1,}$$

With t the film thickness estimated with the SEM image, k the number of fringes in the wavenumber region, and δν the wavenumber region used. A value of 1.76 for the refractive index of the MP-Ge film is extracted from the data. In the approximation of an isotropic medium, the Landau-Lifshitz-Looyenga (LLL) [187] model is well suited for the calculation of the porosity. In the case of a freshly prepared porous germanium, the refractive index is a weighted average of the refractive index of germanium and the refractive index of air and can be expressed as:

$$n_{porous}^{2/3} = n_{substrat}^{2/3}(1 - \mathrm{P}) + \mathrm{P} \qquad \text{Eq2,}$$

With P representing the porosity of the material (i.e. air filling fraction). A 70% porosity value is obtained, close to the value given by the gravimetric analysis.

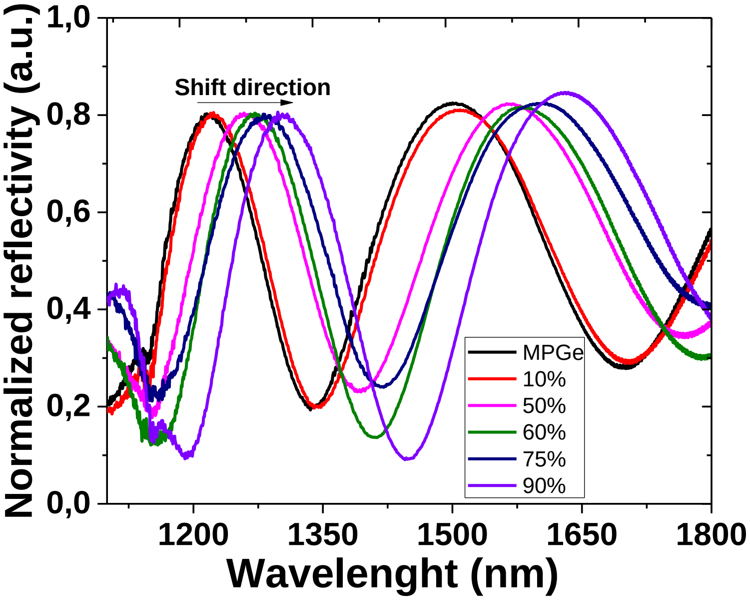

Figure III 12: Reflectivity spectra evolution of the MP-Ge layer fabricated by FBEE technique and immersed in glycerol-water solution with different volumic concentrations.

In order to evaluate the sensitivity of the MP-Ge layer to the environment, the spectrum was recorded in a glycerol/water based medium (see Figure 11). The oscillation fringes showed a significant red shift after infiltration of the pores. The solution-filled pores increase the structure overall effective refractive index and consequently increases its optical thickness. This effect promotes a wavelength shift in the reflectance spectrum with the glycerol concentration and is in perfect agreement with the theory when the refractive index of air is replaced by the one of the solution in the LLL model. The refractive indices of the solution can be estimated according to the glycerol volume concentration [188]'[189] following:

$$n_a = \left[k.n_{glycerol}^2 + (1-k)n_{water}^2\right]^{1/2} \quad Eq3,$$

The performance of the interferometric refractive index (RI) sensor can be evaluated by using the sensitivity S, which is defined as the magnitude of the of the wavelength shift divided by the change in refractive index of the analyte.

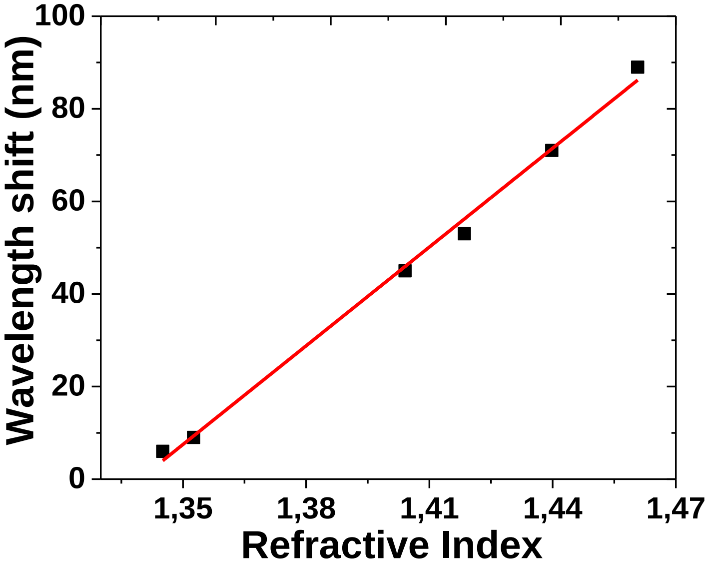

Figure III 13: Wavelength shift of the reflectivity spectra as a function of the refractive index of the solution for different glycerol volume concentrations. The red line is the numerically fitted curve of the experimental data.

Figure 12 shows the wavelength shift as a function of the refractive index of the glycerol-water based solution with different volume concentrations. Considering a linear relation (red curve) between the shift (Δλ) and the variation of the refraction index (Δn), we have extracted a sensitivity S = Δλ/Δn = 711±23nm/RIU. This value is higher than that observed for porous silicon Fabry-Perot cavitiesThis value is more important than porous silicon based optical sensors [190]’[81] making porous Ge a good candidate for optical interferometric biosensing applications.

III.6 Conclusion

High growth rate synthesis of MP-Ge has been demonstrated by a new Fast bipolar electrochemical etching technique. A DC nucleation step allows a uniform lateral homogeneity and a cathodic current step can be used to control the surface morphology. FTIR (Fourier Transform Infrared Spectroscopy) measurements and Cyclic Voltammetry confirm the presence of Ge-H_x termination in the as formed MP-Ge. High switching time between etching and passivation in the FBEE regime contributes effectively to protect crystallite walls and stimulates etching at the pore tips. Finally, we show that this technique is very effective to tune the refractive index of porous Ge and demonstrated a basic optical sensor device, which could open-up opportunities for application in bio-sensing and photonic devices.

III.7 Acknowledgment

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III.8 Abreviatons

MP-Ge Mesoporous Germanium, FBEE Fast Bipolar Electrochemical Etching, CBEE Conventional Bipolar Electrochemical Etching, DC Direct current, CV Cyclic Voltammetry, LLL Landau-Lifshitz-Looyenga, SCE Saturated Calomel Electrode, QC Quantum Confinement, SCR Space Charge Region.

CHAPITRE IV ARTICLE: TRANSFORMATION MORPHOLOGIQUE ET PROPRIÉTÉS ÉLECTRIQUES ET STRUCTURALES DU GERMANIUM MÉSO-POREUX

IV.1 Avant-propos

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Revue : Nanotechnology

Référence : [67]

Titre français : Conductivité électrique ajustable dans le germanium méso-poreux

Contribution au document : Cet article contribue à la thèse en étudiant les propriétés électriques, et structurelles de Ge poreux, ainsi qu'en démontrant la transformation morphologique de ce matériau sous traitement thermique, qui est un processus important dans la fabrication des substrats virtuels proposés.

Résumé français :

Les nanostructures à base de germanium ont attiré une attention importante en raison des propriétés électriques et optiques favorables, qui sont ajustables à l'échelle nanométrique. Des densités élevées de nanocristaux de germanium sont synthétisées par gravure électrochimique, rendant le germanium poreux un matériau attrayant pour une variété d'applications. Dans ce travail, nous avons démontré une conductivité électrique fortement ajustable dans des couches de germanium mésoporeuses en réalisant une étude systématique de la taille des cristallites en utilisant un recuit thermique, avec des conductivités expérimentales allant de 0,6 à 33 ($x10^{-3}$) $\Omega^{-1}cm^{-1}$. La conductivité du germanium mésoporeux tel que préparé avec une porosité de 70% et une taille de cristallite comprise entre 4 et 10 nm est de ~ 0,9 x 10^{-3} $\Omega^{-1}cm^{-1}$, 5 ordres de grandeur inférieure à celle du germanium de type p en vrac. Le recuit thermique pendant 10 minutes à 400 °C réduit davantage la conductivité; cependant, le recuit à 450 °C a provoqué une transformation morphologique des cristallites colonnaires en cristallites granulaires interconnectés et une augmentation de la conductivité de deux ordres de grandeur par rapport au germanium mésoporeux préparé due à l'influence des états de surface.

Note: Ma contribution essentielle dans cet article couvre les analyses morphologique, structurales et électriques des couches poreuses. Le modèle du transport électrique a été développé par l’auteur principal.

Tunable conductivity in mesoporous germanium

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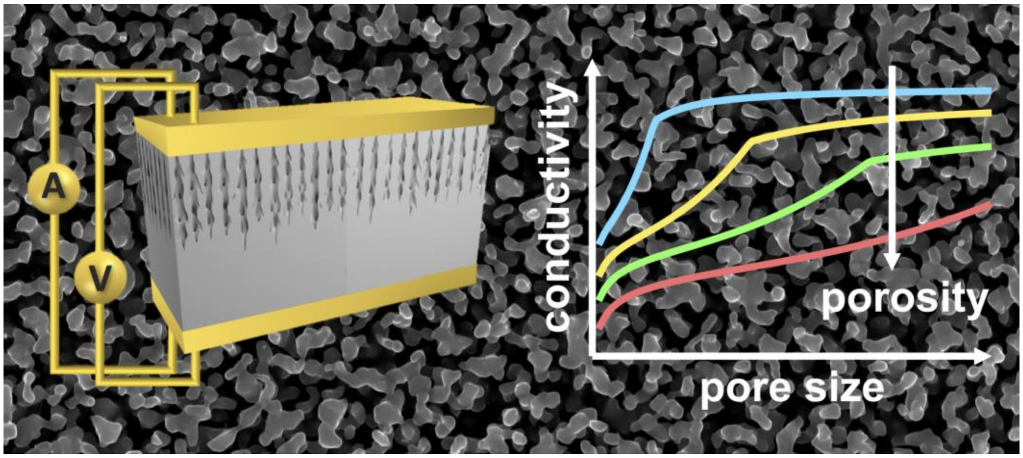
[3] These authors contributed equally.

Keywords: porous germanium, bipolar electrochemical etching, electrical conductivity, nanostructured germanium, electrical transport, surface states, thermal annealing.



Graphical abstract

IV.2 Abstract

Germanium-based nanostructures have attracted increasing attention due to favorable electrical and optical properties, which are tunable on the nanoscale. High densities of germanium nanocrystals are synthesized *via* electrochemical etching, making porous

germanium an appealing nanostructured material for a variety of applications. In this work, we have demonstrated highly tunable electrical conductivity in mesoporous germanium layers by conducting a systematic study varying crystallite size using thermal annealing, with experimental conductivities ranging from 0.6 to 33 ($\times 10^{-3}$) Ω^{-1}cm^{-1}. The conductivity of as-prepared mesoporous germanium with 70% porosity and crystallite size between 4 and 10 nm is shown to be ~ 0.9×10^{-3} Ω^{-1}cm^{-1}, 5 orders of magnitude smaller than that of bulk p-type germanium. Thermal annealing for 10 minutes at 400 °C further reduced the conductivity; however, annealing at 450 °C caused a morphological transformation from columnar crystallites to interconnecting granular crystallites and an increase in conductivity by two orders of magnitude relative to as-prepared mesoporous germanium caused by reduced influence of surface states. We developed an electrostatic model relating the carrier concentration and mobility of p-type mesoporous germanium to the nanoscale morphology. Correlation within an order of magnitude was found between modelled and experimental conductivities, limited by variation in sample uniformity and uncertainty in void size and fraction after annealing. Furthermore, theoretical results suggest that mesoporous germanium conductivity could be tuned over four orders of magnitude, leading to optimized hybrid devices.

IV.3 Introduction

Germanium (Ge) nanostructures have received significant attention in recent years due to their remarkable optical and electrical properties. Strong quantum confinement has been observed in these materials allowing the optical and electrical properties of Ge to be precisely tuned by varying the nanostructure size and shape [135], [191]–[195]. Furthermore, the lack of a stable oxide in Ge allows straightforward functionalization of nanostructures and can be used for surface passivation, for improving compatibility with solvents, and for triggering responses in the material to external stimuli [83], [181], [196]. Ge nanostructures are also being investigated as anodes for next generation lithium-ion rechargeable batteries because of the outstanding volumetric lithium storage capacity of Ge as well as much improved cycling stability relative to bulk Ge due to the high surface to volume ratio and the space separation between nanostructures [126], [132], [197]–[203].

In the fabrication of nanostructures, it is often desirable to achieve a high-density film rather than small quantities of singular nanocrystals. Additionally, for lithium-ion batteries, it is essential to have sufficient space between nanostructures to allow for volumetric expansion over lithiation/delithiation cycles [201]. Both of these preceding criteria can be achieved by bipolar electrochemical etching of bulk Ge to make porous Ge films up to several microns in thickness [83], [146]–[148], [152], [204]. Though other techniques including redox-transmetalation reactions [197], surfactant templating [205]–[207], and nanoparticle assisted growth [142] have been used to synthesize porous Ge, bipolar electrochemical etching has become a leading fabrication choice because it is simple and offers a high degree of flexibility and control. This technique generates high densities of columnar Ge nanocrystals separated by pores with diameters on the order of 10 nm (mesoporous Ge). Structural properties such as porosity and crystallite size are varied by changing the etching conditions such as etching current and pulse duration [147], [152]. Recent studies characterizing the optical properties of porous Ge demonstrate tunable photoluminescence and bandgap [135], [136], [208], [209]. Previous work by Jing *et al.* reported lateral conductivities on the order of 0.1 to 1 Ω^{-1} cm^{-1} for mesoporous Ge fabricated by annealing of GeO_2 ceramic films [210]; however, little information is available regarding the electrical properties of mesoporous germanium fabricated by electrochemical etching. Knowledge of these electrical properties is crucial for optimal implementation in applications such as lithium-ion batteries, thin-film multi-junction solar cells [211], near-infrared light emitting diodes [136], and optical sensors [204].

Electrical properties in the most extensively studied porous semiconductor, porous silicon, made by electrochemical etching [212], [213] have been shown to vary significantly with crystallite size, porosity, and fabrication conditions. Conductivities ranging from 10^{-11} to 10^{-3} Ω^{-1} cm^{-1} have been reported for meso- and nanoporous silicon [214]–[219] with crystallite sizes typically in the range of 5 to 10 nm. Changes in electrical behavior have been observed with thermal treatment [217], gas adsorption [220], [221], and exposure to polar liquids [222]. Similar studies have not been performed in mesoporous Ge due to historical challenges associated with reproducibility and control in the fabrication process [147], [150], [223]; however, recent advances in the electrochemical etching procedures have vastly improved the viability of this technique [147], [152], [204] and systematic studies are now possible.

In this work, we show that mesoporous Ge films have conductivity several orders of magnitude smaller than the Ge substrate on which they are fabricated. We investigate the effect of thermal annealing on the morphology of mesoporous Ge and correlate changes in the electrical behavior with morphological and structural changes produced by thermal treatment. The results show that this annealing procedure allows controllable tuning of the nanostructure size over more than two orders of magnitude. Furthermore, the conductivity increases by at least two orders of magnitude with annealing temperature as the crystallites become larger, indicating that there is potential to achieve reasonable conductivities for applications such as energy conversion and storage while still maintaining the benefits of the nanostructures introduced by porosification. Finally, we propose an electrostatic model that predicts the evolution of average free carrier concentration and mobility with changing morphology in mesoporous Ge. This model considers the void shape and size, the porosity, the Ge doping concentration, and the expected density of surface states on the pore walls, which act as traps for the free carriers. The calculations assume that a depletion region exists at the interface between Ge and the void and that the void-dependent mobility is inversely proportional to the density of surface states. This model makes a direct link between morphology and electrical conductivity in porous Ge, and could equally be applied to any porous semiconductor.

IV.4 Methods

IV.4.1 Preparation of mesoporous Ge films

Mesoporous Ge layers were fabricated on p+ type Ge wafers by bipolar electrochemical etching (BEE) [147], [204] in a two-electrode electrochemical cell with a platinum wire counter electrode manufactured by Kymosis using an electrolyte consisting of 5:1 hydrofluoric acid (49%) and anhydrous ethanol. The p+ type Ge wafers were (100) oriented with a 6° miscut and had a nominal resistivity of 0.025 Ω cm. Electrical contact was established by pressing the backside of the wafer onto a gold-coated copper electrode. To ensure the formation of a uniform mesoporous layer, a DC initiation step was used during which a anodic etching current of +1.5 mA/cm^2 was applied for 10 s prior to beginning the BEE step [204]. After initiation, anodic and cathodic currents with densities of ±1.5 mA/cm^2 were applied alternately with pulse durations of 1s. The etching rate was approximately 15 nm/min and etching times were varied to fabricate mesoporous Ge layers with thicknesses ranging from 0.1-3 µm.

IV.4.2 Thermal annealing

Annealing of mesoporous Ge samples was performed in a forming gas (N_2:H_2 90:10) ambient using a J.I.P. ELEC JetFirst rapid thermal annealing (RTA) system with a ramp rate of 25 °C/s. Annealing temperatures ranged from 250°C to 650°C. The duration was fixed at 10 minutes for all temperatures.

IV.4.3 Material characterization

The structural morphologies and thicknesses of as-prepared and annealed mesoporous Ge films were characterized by scanning electron microscopy (SEM) using a Zeiss 1540XB CrossBeam Workstation. Quantitative nanostructural analysis of the crystallite size distribution was performed by Fourier analysis of the SEM images using the ImageJ software. The crystal structure of as-prepared mesoporous Ge was further examined by high-resolution scanning transmission electron microscopy (HRSTEM) using a FEI Titan Cubed electron microscope equipped with a CEOS image and probe corrector operated at 300 kV. X-ray diffractograms of as-prepared and annealed mesoporous Ge samples were measured using a Philips X’Pert powder diffractometer immediately after preparation. Transport of porous Ge samples was performed under propanol. Fourier-transform infrared (FTIR) spectroscopy was performed on as-prepared and annealed mesoporous Ge samples using a VERTEX 80/70v FTIR spectrometer using a Globar source, a KBr beam splitter, and a MCT D15 detector. Hydrogen absorbance was determined by transmission FTIR spectroscopy with a spectral resolution of 2.0 cm^{-1} and a scanning time of 5 minutes for as-prepared mesoporous Ge and after annealing at various temperatures. Microscopic FTIR reflectance analysis was used to determine the porosity of as-prepared mesoporous Ge using a standard 15x objective with a gold surface as reference.

IV.4.4 Current-voltage measurement

Ohmic contacts were realized by direct deposition of nickel (30 nm) and gold (450 nm) on the top side and nickel (30 nm) and gold (150 nm) on the back side. Preliminary samples were fabricated with equal thickness of gold (150 nm) on both faces, however the thickness of the top gold layer was increased to ensure a singly connected contact after non-ohmic behaviour was observed in some samples. The specific contact resistivity ρ_c ranges from about 5×10^{-3} - 5×10^{-2} Ω cm^2 depending on the annealing condition (ρ_c decreases with increasing annealing temperature). Metallization of annealed samples was performed after the thermal treatment. Samples were cleaved after metallization. Current-voltage (I-V) characteristics were measured by four-wire sensing. Samples were fixed to a gold-plated stage using a vacuum connection. Electrical contact was made to the top of the samples using tungsten tipped probes and to the bottom *via* connection to the stage. The I-V characteristic was measured for each sample by ramping the applied voltage from -200 mV to 200 mV in steps of 1 mV, using a limit of ±150 mA for the current. A Keithley 2420 source meter was used as the power source and to perform measurements of current and voltage.

IV.5 Results and discussion

IV.5.1 Morphology of mesoporous germanium films

Mesoporous Ge layers were fabricated on p+ type Ge wafers by bipolar electrochemical etching (BEE), as described in the Methods section. Top view and cross-sectional scanning electron microscope (SEM) images of as-prepared mesoporous Ge are shown in figure 1a-c. A uniform distribution of nano-sized columnar pores extends down from the surface with some branchial pore channels. The pores terminate abruptly at the interface between the mesoporous layer and the parent substrate. The size of the Ge nanocrystallites is estimated to be in the range of 4-10 nm (see figure 1c). The high-resolution scanning transmission electron microscopy (HRSTEM) micrograph shown in figure 1d reveals that the Ge nanostructures retain the same crystallographic orientation as the Ge substrate with diamond lattice structure and an inter-planar spacing of ~0.3 nm, which is consistent with previous findings [136].

Porosities were measured by analyzing Fabry-Perot fringes observed in the infrared reflectance spectrum [204] (see Supporting Information, section 1). We observed an average porosity of 72% in as-prepared mesoporous Ge samples.

Top view and cross-sectional SEM images of mesoporous Ge after annealing for 10 minutes at temperatures ranging from 350 °C to 600 °C are shown in figure 1e-p. As the annealing temperature was increased, the Ge nanocrystallites grew larger in size.

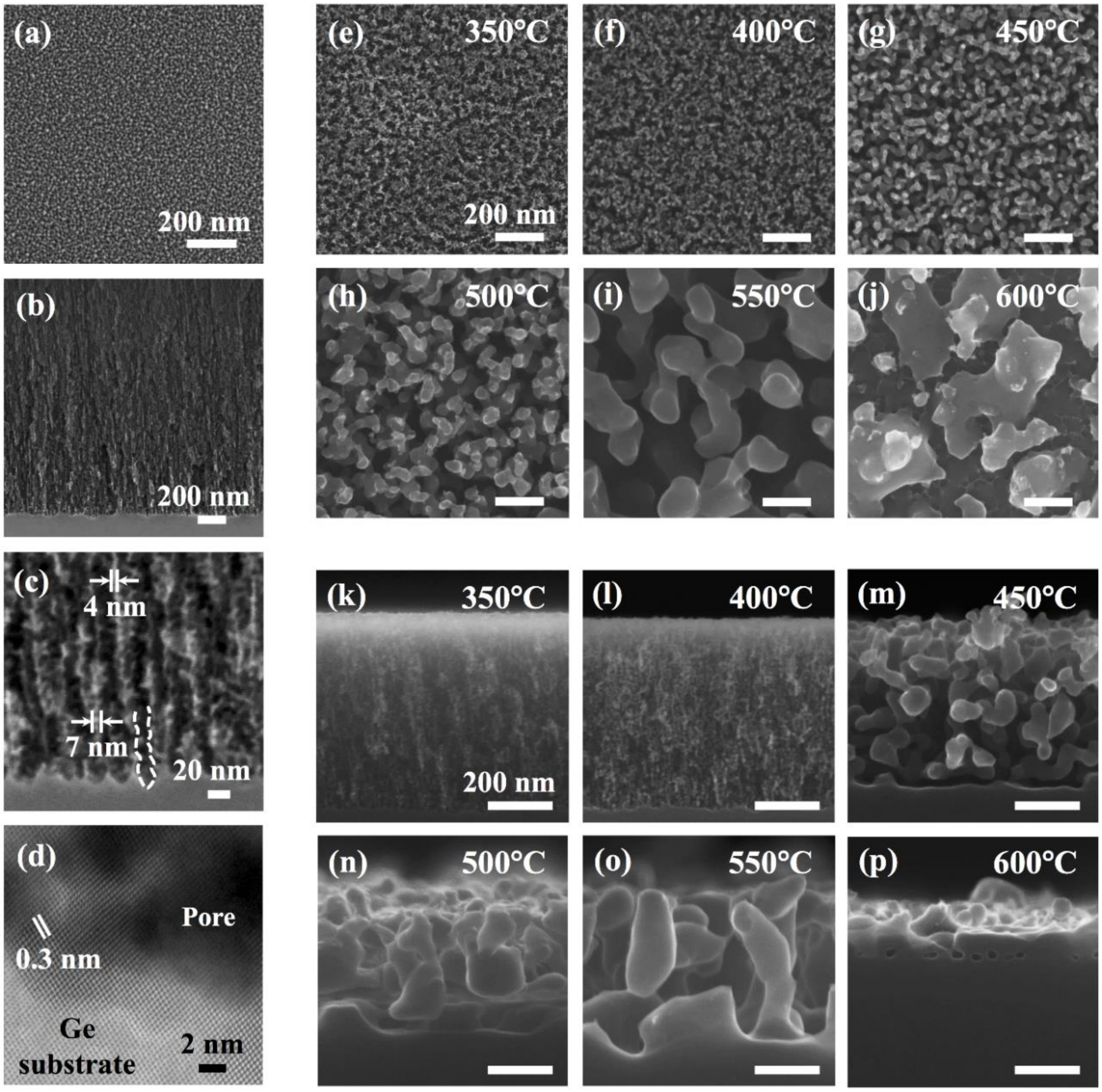


Figure IV 1: (a) Top view and (b) cross-sectional SEM image of as-prepared mesoporous Ge layer formed by BEE.(c) High-resolution SEM image of the Ge crystallites. Crystallite sizes and pore morphology at the substrate interface are indicated. (d) HRSTEM micrograph showing the interface between the Ge substrate and the mesoporous Ge interface. (e-j) Top view and (k-p) cross-sectional SEM images of mesoporous Ge layers annealed at 350 – 600 °C under hydrogen flow. Scale bars are 200 nm in length unless otherwise indicated. The evolution of the morphology and crystallite size with annealing temperature is evident.

At an annealing temperature of 450 °C, a significant morphological transformation occurred in which the porous structure self-organized into a network of elongated granular crystallites. After annealing at 600 °C, the upper crystallites became interconnected forming nano-voids [224], [225] with average sizes in the range of 20-50 nm. For some samples, the creation of a layer of nano-voids was observed after annealing at 550 °C rather than 600 °C. This was likely due to minute changes in substrate resistivity and etching current between samples.

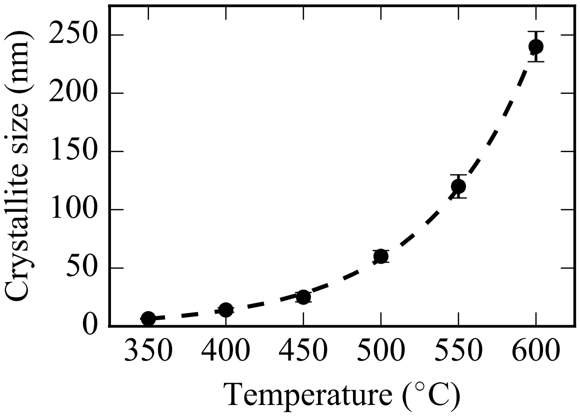


Figure IV 2: Variation of the surface crystallite size with annealing temperature.

The sizes of the Ge nanocrystallites at the surface of the annealed samples were extracted from top view SEM observations using the Fourier transform of the images (see figure 1e-j). The average crystallite size was determined by fitting the size distribution with a log-normal function. The reorganization of the structure to form larger crystallites is induced by Ostwald ripening [225], in which the Ge atoms on the surface jump to more favorable energy positions during thermal annealing below the Ge melting point (938 °C). The average surface crystallite size ($d_{\text{crystallite}}$) increased exponentially with annealing temperature (T), as shown in figure 2, indicating strong Boltzmann-like temperature dependence, which is consistent with sintering theory developed for porous materials [99]. This relationship indicates that the average crystallite size can be precisely tuned through annealing temperature and duration. Further details are given in the Supporting Information, section 2.

IV.5.2 Electrical resistivity of mesoporous germanium

Surface effects caused by the high density of mesoscopic pores have a significant impact on electrical transport. Due to the nature of the samples (highly resistive film bonded to a comparatively low resistance substrate), conventional methods for measuring conductivity such as Hall effect measurements were not appropriate. For this reason, a simple thickness-dependent experimental technique was devised.

Blanket contacts of nickel and gold were applied to the top and bottom surfaces of as-prepared and annealed mesoporous Ge samples on the parent substrate in preparation for current-voltage measurements. After metallization, the sample edges were cleaved, creating a sandwich-type structure (see figure 3).

Linear current-voltage characteristics observed using the four-wire sensing technique for both as-prepared and annealed samples indicated the formation of ohmic contacts (see figures 3 and 4a). Total resistance R_T was determined from current-voltage measurements and the average value for each sample was plotted as a function of porous layer thickness (see figure 4b). The resistivity of the porous layer ρ_{PGe} was determined by assuming the following relationship between total resistance and porous layer thickness:

$$R_T = \frac{\rho_{PGe}}{A}t + \frac{\rho_{Ge}(h - t)}{A} + R_{contact} \approx \frac{\rho_{PGe}}{A}t + R_0 \qquad (1)$$

where A, t, and h are indicated in figure 3. $R_{contact}$ is the contact resistance, which is grouped along with the initial substrate resistance into the thickness-independent term R_0. Contact resistance was assumed to be similar for all samples at each annealing condition because surface porosity variation between samples annealed at the same temperature is small. In the final expression, we have used the fact that the Ge substrate resistivity ($\rho_{Ge} \sim 0.025\ \Omega$ cm) is negligible compared to the resistivity of the porous layer. Conductivity is simply the inverse of resistivity.

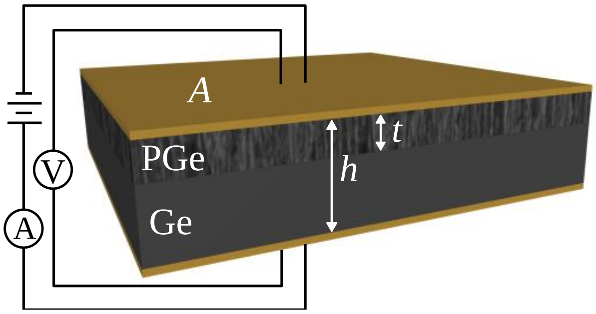


Figure IV 3: Schematic of layer stack and four-wire sensing configuration for current-voltage measurements across the porous Ge (PGe) and Ge substrate layers indicating the area perpendicular to current flow A, the porous layer thickness t, and the total thickness of the PGe-Ge layer stack h.

Figure 4b shows the total resistance (averaged over multiple measurements) as a function of porous layer thickness for as-prepared mesoporous Ge. A linear fit was performed by weighted least squares and the resistivity of the mesoporous Ge was found to be 1100 ± 300 Ω cm, five orders of magnitude larger than that of the original Ge substrate. The uncertainty corresponds to the standard deviation of the fitting parameters.

The large increase in resistivity after porosification can be explained by the high surface to volume ratio of mesoporous Ge films, on the order of 10^7 cm^{-1}, and the high density of surface states generated on the pore walls. Although the surface state density has yet to be measured in mesoporous Ge, total surface state densities of at least 10^{13} cm^{-2} and possibly exceeding 10^{14} cm^{-2} are expected for Ge with native oxide [226]–[229]. For clean Ge surfaces, surface state densities may be on the order of 4×10^{14} cm^{-2} eV^{-1}, assuming (as in section 3.4) that the states are evenly distributed throughout the band gap [226], [229]. The impact of surface states on carrier transport has previously been observed in Ge nanowires [227], [228] as well as in porous silicon layers [215], [230]. Surface states trap carriers, creating a space charge region and depleting the free carrier concentration in the material [215], [227], [228], [230], [231] while simultaneously reducing carrier mobility [232]. This results in the high resistivity (low conductivity) that we have observed in the porous material.

These assumptions are further supported by relating changes in electrical behavior to morphological changes induced by annealing. After annealing at 450 °C, the transition from a porous structure to a granular-type structure caused the resistivity to decrease by two orders of magnitude relative to that of the as-prepared mesoporous Ge. The dependence of resistivity and conductivity on annealing temperature is shown in figure 5.

When the Ge nanocrystallites are small, surface state interactions dominate the electrical transport properties. With increasing nanocrystallite size, the specific surface area of the material goes down and surface states become less important. The most significant change in resistivity occurred at the transition to granular morphology after annealing at 450 °C; however, the resistivity continued to decrease at higher annealing temperatures as the crystallites continued to grow. At temperatures exceeding 550 °C, variations between samples became dominant relative to the trend of increasing resistance with porous layer thickness and so it was not possible to extract reliable estimates of resistivity.

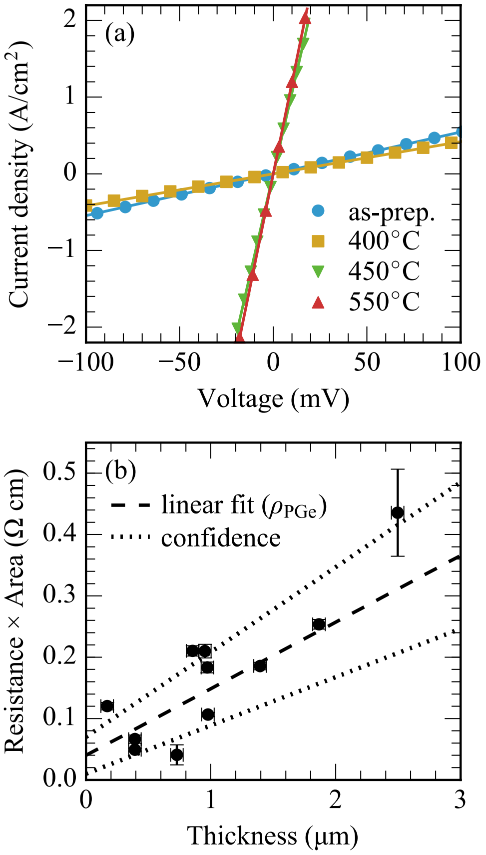


Figure IV 4: (a) Current-voltage characteristics for as-prepared Ge (as-prep.) and after thermal annealing at 400, 450 and 550 °C for 10 minutes. The thickness of the porous layer is between 1.4 and 1.45 µm for all samples shown in (a). (b) Product of average total resistance and area, R_TA, as a function of porous layer thickness, t, for as-prepared mesoporous Ge. Dashed line is the linear fit, which gives resistivity, and dotted lines are confidence interval bounds calculated using standard deviation on the fitting parameters. Error in A is 3%, in t is ± 50 nm, and in R_T is determined from the standard deviation of multiple measurements for each sample. The resistivity of as-prepared porous Ge is found to be 1100 ± 300 Ω cm.

IV.5.3 Structural analysis

To investigate the processes behind the morphological and electrical transformations that occurred with thermal annealing, further analysis of crystallographic properties and surface chemistry was performed.

X-ray diffraction measurements were performed to investigate the crystal structure before and after annealing. The diffraction signal between 20° and 100° for as-prepared mesoporous Ge with a layer thickness of 2 μm on the parent substrate wafer is shown in figure 6 together with those of porous layers annealed at temperatures from 350 to 650 °C. The samples were measured immediately after preparation and transported in propanol to prevent the formation of an oxide. All the diffraction peaks are identified and correspond to the diamond lattice structure of Ge with a lattice constant of 5.65 Å. No peaks from oxides such as GeO_2 (hexagonal or tetragonal) were observed within the detection limit of our equipment. For as-prepared mesoporous Ge, only one significant diffraction peak was observed, originating from the (400) plane family. X-ray diffraction measurements were performed on single crystal samples using a powder diffractometer, and therefore the intensity of the (400) peak varied between samples depending on the orientation. The relative intensity of the peaks between samples is not important.

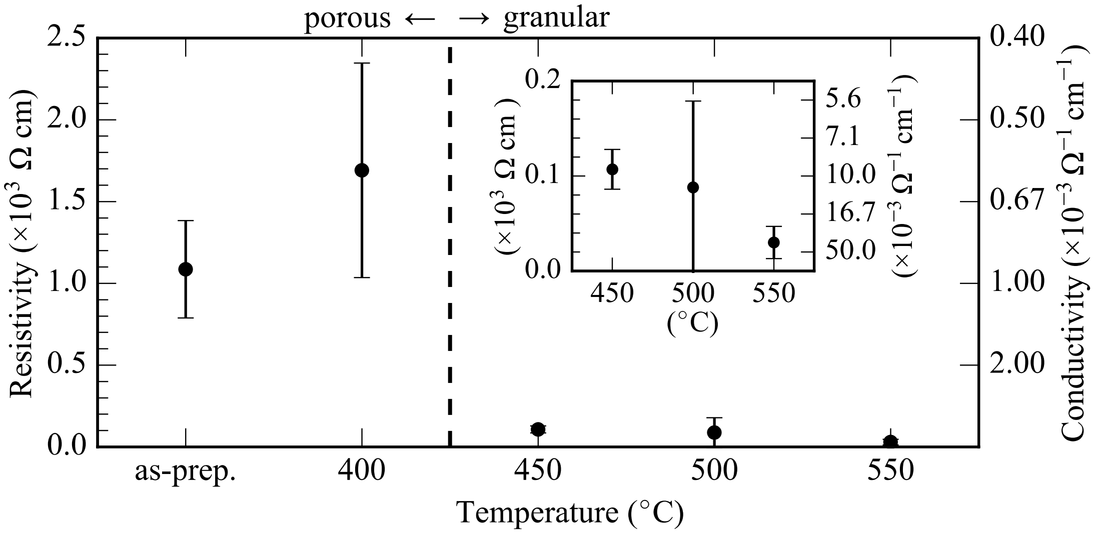


Figure IV 5: Porous Ge resistivity as a function of annealing temperature. The inset shows the resistivities between 450 °C and 550 °C on a smaller scale for clarity. The transition between porous and granular morphologies is indicated. The large uncertainty associated with the data point at 400 °C is due to significant variability between samples that is presumed to be caused primarily by inconsistent contact resistance. Conductivity is given on the secondary y-axes.

After annealing at temperatures exceeding 450°C, diffraction peaks were observed from several additional crystallographic directions suggesting that randomly oriented crystallites were formed. The peaks from mesoporous Ge samples annealed at 550°C and 650°C coincide with the diffraction signature that can be observed in poly-Ge [233], confirming the polycrystalline nature of the nanostructures for this range of annealing temperatures. Atom migration and Ostwald ripening led to the formation of misoriented nanocrystallites that had lost crystallographic coherence with the substrate during annealing at high temperatures. The appearance of polycrystalline Ge signified the presence of trap states at grain boundaries that have a similar effect to the surface states on void walls, reducing majority carrier concentration and mobility and limiting the conductivity of the material [234]. The observed increase in conductivity after annealing would likely be even more significant if crystallographic order was maintained throughout the process.

The wide diffraction peak observed near 66° at all temperatures in figure 6 is amorphous-like in shape. A similar effect has been observed by X-ray diffraction in porous Si [235] and by Raman spectroscopy in porous Ge [236]. No disordered region was observed in the TEM image corresponding to the amorphous phase for as-prepared mesoporous Ge near the interface with the bulk substrate (see figure 1d).

As-prepared mesoporous Ge is coated with covalently bonded hydrogen [83], [84], providing electronic passivation [162] of the surface. We investigate the stability of this coating by studying hydrogen desorption with thermal annealing to clarify the surface diffusion mechanism that results in a reorganization of the structure in mesoporous germanium and to see its influence on electrical properties.

Fourier transform infrared (FTIR) spectra were recorded for mesoporous Ge layers at a series of annealing temperatures to monitor the hydrogen desorption. The transmission FTIR spectrum of as-prepared mesoporous Ge (figure 7) reveals an absorbance band in the range of 1900-2100 cm-1 attributed to germanium hydride (GeHx) stretch mode vibrations. This asymmetric stretching band is dominated by two components at 1982 and 2024 cm-1, corresponding to germanium mono- and di-hydride species, with a smaller component at 2063 cm-1 associated with the tri-hydride [162], [237]. Due to the high surface area of mesoporous Ge compared to a 2D bulk Ge surface [83], the mono-, di-, and tri-hydride stretch modes can be clearly distinguished and their positions are indicated in the spectrum. Such varied H-termination is typical of an atomically rough or porous material, such as porous Si [166].

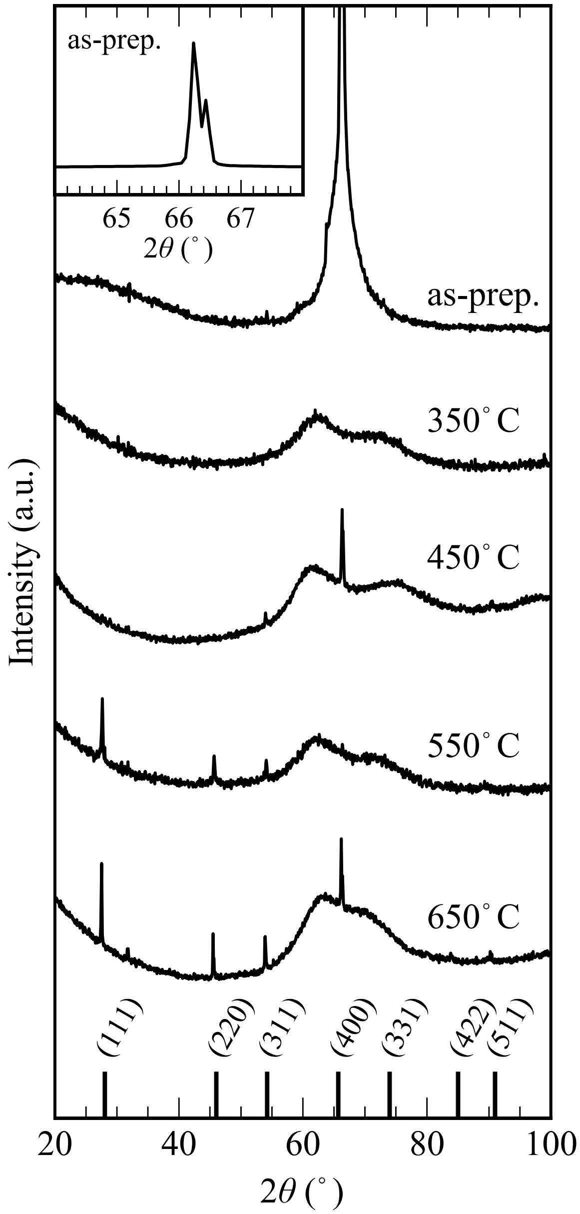


Figure IV 6: X-ray diffraction signal of as-prepared mesoporous Ge (as-prep.) and after annealing at 350 – 650 °C. Note: single crystal samples were measured on a powder diffractometer and so relative peak intensity between samples is due to the orientation of the sample and is of no significance. For as-prepared mesoporous Ge, only the (400) diffraction peak is observed. At annealing temperatures exceeding 450 °C, polycrystallinity is observed as the appearance of new peaks including (111), (220), (311), (331), and (511). Inset shows the full peak for the as-prepared mesoporous Ge sample.

Figure 7 shows the evolution of the GeH_x absorbance band after annealing at temperatures ranging from 250 °C to 550 °C for 10 minutes. The annealing process is identical to that carried out to induce morphological changes (see section 2.2). The band was modeled as the sum of three Gaussians corresponding to the three stretch modes [204]. The amount of GeH_x absorbance decreased with annealing temperature. This is attributed to the surface diffusion of germanium atoms along the pore walls, which tends to minimize the high surface energy [237].

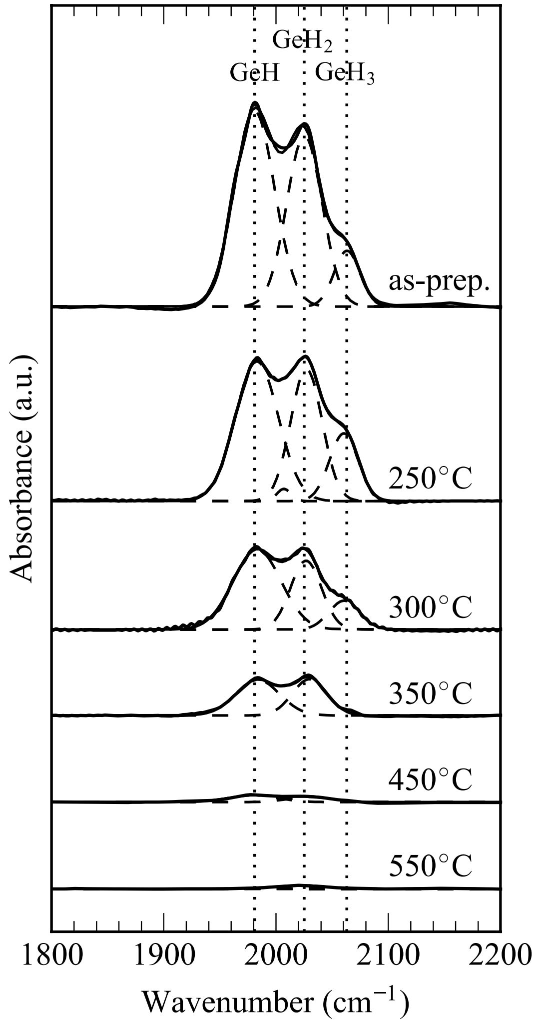


Figure IV 7: GeHx band in the transmission-FTIR spectrum of as-prepared mesoporous Ge and after thermal annealing at 250 – 550 °C. The positions of mono-, di-, and tri-hydride stretch modes are indicated by vertical lines. Decreasing absorbance with annealing temperature indicates hydrogen desorption.

Figure 8 illustrates the strong non-linear dependence of the integrated absorbance on annealing temperature. In the range of 250 °C to 350 °C, the infrared absorbance decreased abruptly due to hydrogen desorption [215], causing the formation of dangling bonds, which facilitated the surface diffusion of germanium atoms and the changes in morphology observed with thermal annealing.

The most significant desorption (between 250 °C and 350 °C), preceded the abrupt morphological transformation that occurred at 450 °C (see figure 1). This suggests that hydrogen desorption and Ostwald ripening may not be simultaneous processes. In this case, there may have been an increase in the surface state density prior to the onset of significant Ostwald ripening, which would explain the observed increase in resistivity of the samples annealed at 400 °C. The hydrogen is almost fully desorbed after annealing at 550 °C.

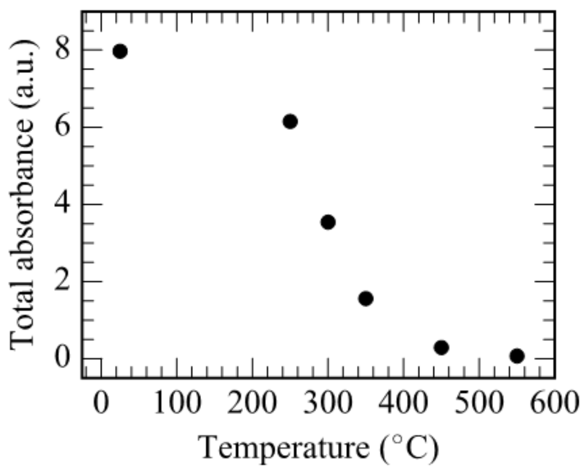


Figure IV 8: Integrated absorbance of the three GeHx species as a function of annealing temperature.

IV.5.4 Electrical transport modelling

Banerjee *et al.* proposed simple electrostatic models for the free carrier concentration and mobility in annealed porous Si [231], [232]. Starting from this framework, we have developed new models specifically for as-prepared and annealed porous Ge. Key differences in these models relative to those introduced by Banerjee *et al.* include the calculation of the electric potential in three dimensions rather than one, the expansion of the mobility model into multiple terms combined according to Matthiessen's rule, and the choice of cylindrical pore as well as spherical void unit cell geometries to represent mesoporous and voided materials, respectively. This model is intended to be indicative, and more detailed experimental characterization of key material parameters (such as surface state density and internal surface area) will improve its accuracy.

The columnar pores of as-prepared mesoporous Ge were modelled as cylindrical pores within cubic unit cells, shown in figure 9a, assuming periodic repetition of the unit cells through all space. This periodic array of identical pores is meant to represent the average pore shape, size, and distribution over a large area.

We do not attempt to model the complex granular morphology produced by annealing at lower temperatures, and rather turn our attention to the voided Ge material that begins to form in some samples after annealing for 10 minutes at temperatures exceeding 550 °C (see figure 1p). We have chosen to represent this system as a network of Ge nanocrystallites divided by spherical voids, shown in figure 9b. As with the columnar pores, this model applies a periodic array of identical voids to represent an average geometry over a large area, rather than attempting to incorporate the non-uniformity in void shape, size, and distribution that is characteristic of voided Ge materials [211], [238]. This spherical void model would best be applied to Ge layers with a high density of spherical cavities, which can be synthesized by annealing of mesoporous Ge under certain conditions, as shown in previous studies [211], [238].

Schematics of the band diagrams are shown in figure 9c-d where the effect of the surface states on the bands is illustrated near the void-Ge interface. Surface state energies are assumed to be distributed uniformly throughout the band gap [226], [239]. The neutral level Φ_0 represents the level at which the surface would be charge neutral if all surface states below were occupied and all surface states above were vacant. In p-type Ge, the Fermi level is below the neutral level and so the surface states act as donors, trapping p-type carriers and creating a buildup of positive charge on the surface. This separation of charge creates a space-charge region surrounding the void, inducing band bending at the interface. Assuming a density of surface states N_s, a doping concentration N_a, and taking the unit cell to be charge neutral, the width of the space charge region W was calculated using Gauss' law to solve for the electric potential Φ under the depletion approximation where it was assumed that the space charge region was depleted of carriers and that the electric field was confined to this region (see Supporting Information, section 3).

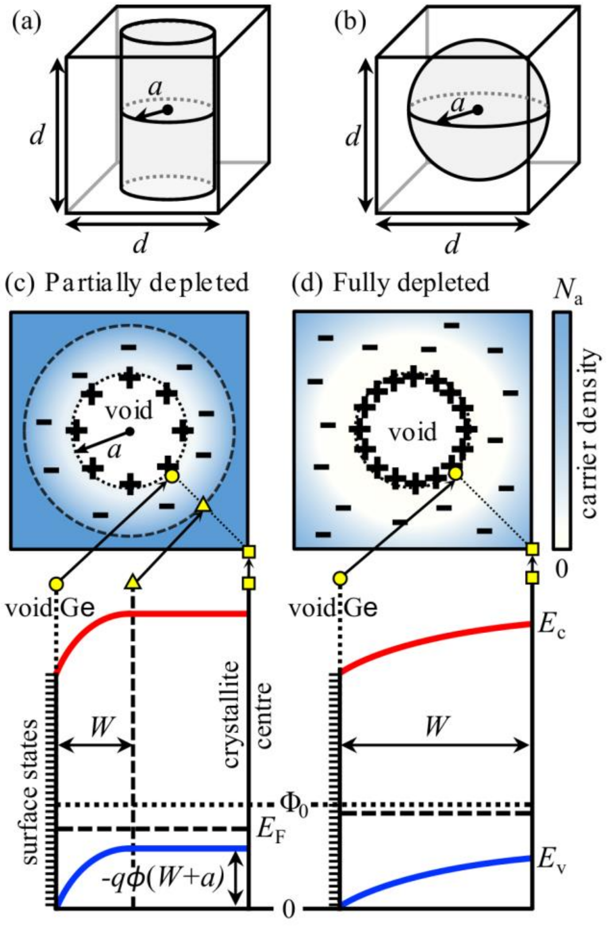


Figure IV 9: Unit cells for (a) as-prepared and (b) annealed porous Ge electrical transport models. The dimension of the unit cell is given by 'd' and the radius of the pore/void is given by 'a'. (c-d) Schematic of carrier densities and band diagrams for unit cells that are (c) partially and (d) fully depleted of carriers under the depletion approximation. Ionized acceptor atoms are indicated by (-) and holes trapped by surface states are indicated by (+). The conduction E_c and valence E_v bands, the Fermi level E_F, the neutral level Φ_0, and the width of the space charge region W are shown. The energies of the bands are determined relative to the bottom of the valence band at the void-Ge interface. The band bending is determined by the electrostatic potential at the boundary of the space charge region, Φ (W+a). Spatial markers relate the band diagrams to the corresponding carrier density schematics.

Once the space charge region was defined, the depletion approximation was relaxed. The spatial density of carriers is given by

$$p(r) = \begin{cases} 0 & 0 \leq r < a \\ N_a \exp\left[- \dfrac{q\Phi_\infty(r)}{kT} \right] & a \leq r < W + a \\ N_a & r \geq W + a \end{cases} \qquad (2)$$

where Φ_∞ is the electric potential defined relative to infinity. The approximate spatial carrier density is shown in figure 9c-d for the cases where the unit cell is partially and fully depleted of carriers under the depletion approximation. The average carrier concentration p_{ave} in porous Ge was found by integrating the spatial density over the volume of Ge in the unit cell.

The mobility Φ_∞ was calculated using Matthiessen's rule with a correction factor (1–P), where P is porosity, to account for the fact that no carriers can travel in the void.

$$\mu = \left(\frac{1}{\mu_{\mathrm{Ge}}} + \frac{1}{\mu_{\mathrm{void}}}\right)^{-1} (1\text{-}P) \tag{3}$$

Where μ_{Ge} is the mobility of bulk Ge calculated according to Klassen's unified mobility model [240] based on parameters from Palankovski [241] (see Supporting Information, section 4). The mobility contribution due to the voids is given by

$$\mu_{\mathrm{void}} = C\frac{1}{N_{\mathrm{sv}}} \tag{4}$$

where $N_{\mathrm{sv}} = N_{\mathrm{s}}\, E_{\mathrm{g}}\, (A_{\mathrm{void}}/d^3)$ is the number of surface states per unit volume (A_{void} is the surface area of the void) and C is a fitting parameter.

Having calculated the average carrier concentration and mobility, it is straightforward to calculate the resistivity:

$$\rho = \frac{1}{q p_{\mathrm{ave}} \mu} = \frac{1}{\sigma} \tag{5}$$

where σ is conductivity.

The fitting parameter C was found by comparing to the experimental resistivity for as-prepared porous Ge. We assumed a pore diameter $2a = 7$ nm, a porosity $P = 70\%$, and a doping concentration $N_{\mathrm{a}} = 3\times10^{17}\mathrm{cm}^{-3}$ assuming uniform spacing and 100% activation. A surface state density $N_{\mathrm{s}} = 5\times10^{14}\ \mathrm{cm}^{-2}\ \mathrm{eV}^{-1}$ is chosen to slightly exceed that which is expected for clean Ge surfaces [226], [229]. In this way, we account for the irregularity of the void walls, which we are modelling as smooth cylinders or spheres. The neutral level Φ_0 was taken to be one third of the bandgap [239] (0.22 eV). Based on these assumptions and setting $\rho = 1100\ \Omega$ cm, a value of $C \sim 320{,}000\ \mathrm{cm}^{-1}\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ was obtained.

The modelled free carrier concentration, carrier mobility, and resistivity for as-prepared mesoporous Ge are shown as a function of pore size in figure 10a-c. For a void diameter of 7 nm and a porosity of 70%, the average free carrier concentration is reduced by three orders of magnitude relative to the substrate doping density and the mobility is reduced by two orders of magnitude. These reductions are caused by the strong influence of surface states near the void-Ge interface. As anticipated, both carrier concentration and mobility increase as the pores become larger and further apart, resulting in increased conductivity. Similar trends are observed for the spherical void model. The cusp-like features observed in the carrier concentration and resistivity curves correspond to the transition from the fully depleted case to the partially depleted case (see Supporting Information, section 3). As the porosity increases, the fully depleted case applies over a wider range of void sizes. In the partially depleted case for large void size, both carrier concentration and mobility scale with $(1 - P)$. This is also the limiting case when the surface state density goes to zero. Reducing the surface state density could increase the conductivity by up to five orders of magnitude for highly porous materials with small pore size.

Figure 10c and f show a comparison between the modelled and experimental conductivities for as-prepared porous Ge and after annealing at 550°C. We did not directly compare the experimental data at other annealing temperatures to the model because of the substantial difference between the modelled geometry (spherical voids) and the true morphology of the material (interconnected granular crystallites). Although the morphology of the sample shown in figure 1 after annealing at 550°C also has granular form, at this temperature we started to see the formation of spherical voids in some samples. The margins of average void size indicated in figure 10f are determined by assuming the void size is equivalent to the average spacing between crystallites for samples with granular morphology.

The continuously decreasing resistivity shown in figure 10 as a function of void size does not strictly agree with what was observed in experiment, where we first saw an increase after annealing at 400°C before the expected decrease was observed. The reason for this discrepancy is that the model assumes the density of surface states is unchanged for all void sizes. This does not account for the variation in hydrogen coverage observed in experiment, where we expect that significant hydrogen desorption first results in an increased surface state density prior to the onset of significant Ostwald ripening.

Given that the porosity of mesoporous Ge is expected to decrease with annealing due to thinning of the porous layer that was observed experimentally (see figure 1k-p), the estimation of porosity in the range of 30-50% after annealing at 550°C for 10 minutes, obtained by comparing the experimental and theoretical results in figure 10f, is reasonable. This implies that surface state densities are similar for as-prepared mesoporous Ge and for annealed mesoporous Ge after the onset of Ostwald ripening, indicating that any initial increase in surface states density is countered by the rearrangement of the Ge atoms at sufficiently high temperature. Decreasing the surface state density by optimizing the surface passivation would allow for significant enhancement of the mesoporous Ge conductivity.

For smaller crystallite sizes, quantum confinement effects are expected to change the band-gap [135], [136]. This effect was not included in this model because it has yet to be well characterized for mesoporous Ge materials. Inclusion of this effect will improve the accuracy of this model, particularly for high porosities and small pore / void sizes [231].

Values used for the neutral level and the density of surface states are estimated and assumed to be unchanged by thermal annealing. Experimental measurements of these values for the material systems being studied would improve the accuracy of the model. Additionally, experimental determination of the internal surface area of mesoporous Ge would be highly beneficial, given that the pores are not smooth cylinders as was assumed in the model, and this may increase the effective interface state density that should be used. Further discussion of the impact of interface state density on the simulated transport properties is included in the Supporting Information, section 5.

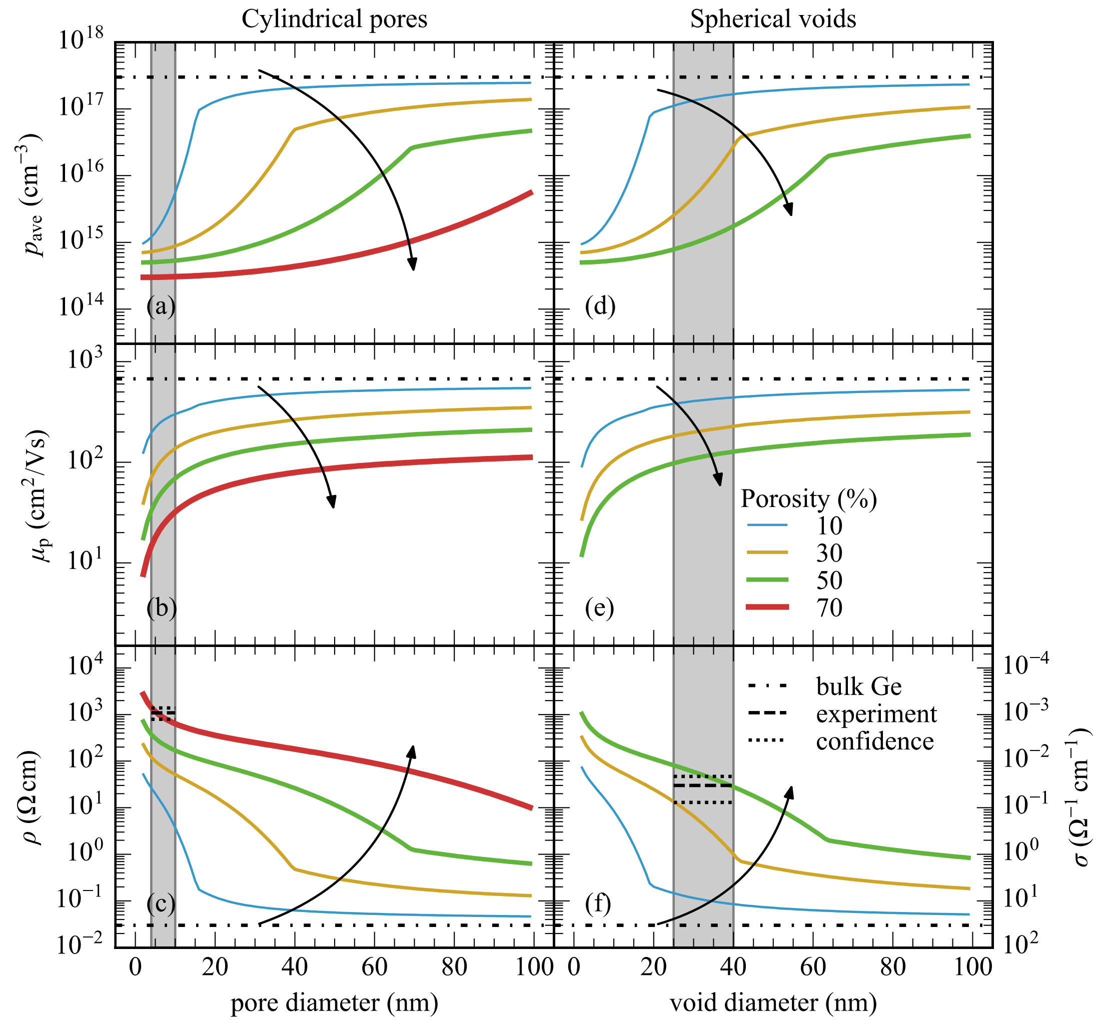


Figure IV 10: (a, d) Average free carrier concentration, (b, e) carrier mobility, and (c, f) resistivity of (left) as-prepared and (right) annealed mesoporous Ge. Conductivity is shown on the secondary y-axis of (c) and (f). Electrical properties are shown for a variety of porosities as a function of pore/void size. A doping concentration of 3×10^{17} cm^{-3} and an interface state density of 5×10^{14} cm^{-2} eV^{-1} are assumed. Highlighted regions show the range of diameters over which the model can be compared with experimental results, for as-prepared mesoporous Ge (left) and after annealing at 550 °C (right). Arrows indicate direction of increasing porosity. Values for bulk Ge (substrate) are shown. Simulated results are not shown for annealed mesoporous Ge with 70% porosity because porosities exceeding 52% are not permitted for the selected unit cell geometry.

IV.6 Conclusion

The resistivity of as-prepared mesoporous Ge with an average porosity of 72% and crystallite sizes ranging from 4-10 nm was found to be ~ 1100 Ω cm, five orders of magnitude higher than that of the p-type Ge substrate (0.025 Ω cm). This high resistivity is due to the high density of surface states on the pore walls, which trap free carriers, significantly reducing average carrier concentration and mobility, and could be useful for electrical isolation in Ge circuits. This is supported by modelling results, which suggest that there is a depletion of carriers by several orders of magnitude for mesoporous samples with high porosity.

Thermal annealing initiated hydrogen desorption from the pore walls and surface diffusion of Ge atoms *via* Ostwald ripening, allowing the size of the Ge nano-crystallites to be predictably controlled by varying the annealing temperature and duration. At low annealing temperatures (< 450 °C), considerable hydrogen desorption was observed without significant changes in the morphology of the material. We predict that this imbalance results in an increased surface state density, which would explain the increased resistivity observed after annealing for 10 minutes at 400 °C relative to the resistivity of as-prepared mesoporous Ge. A morphological transformation was observed after annealing for 10 minutes at 450 °C from porous-type material to a granular crystallite structure. Long range crystalline order, which was observed after the etching process, was slowly lost during annealing as the Ge atoms reorganized. The average size of the crystallites increased exponentially with annealing temperature until they connected to each other, creating a layer of nano-voids beneath the surface after annealing at 550 - 600 °C. Increasing crystallite size reduced the influence of surface states on the electrical properties of the material, and our electrostatic model predicted rapidly decreasing resistivity with increasing void size. This was clearly observed in experiment after annealing at 450 °C where an abrupt drop in resistivity by two orders of magnitude relative to the as-prepared mesoporous Ge occurred.

The high resistivity of mesoporous Ge after initial preparation and the variability with annealing demonstrates the potential for mesoporous Ge materials to be used as tunable resistors or insulating layers in a variety of applications. Furthermore, we believe that the resistivity can be sufficiently reduced to allow for annealed mesoporous Ge to be used in energy conversion and storage applications.

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IV.7 Acknowledgments

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IV.8 Supporting Information

IV.8.1 Measuring porosity by infrared reflectance

Infrared light incident on the surface of as-prepared mesoporous Ge samples is reflected from both the top interface (air to porous Ge) and the bottom interface (porous Ge to Ge substrate). Interference between reflections from the two interfaces generates Fabry-Perot fringes in the reflectance spectrum shown in figure 9. The interference pattern is used to determine the refractive index of the film using the following expression:

$$n_{PGe} = \frac{m}{2\,\delta v\, t} \qquad (S1)$$

Where *m* is the number of fringes within wavenumber region δ*v* and *t* is the film thickness, estimated from SEM images.

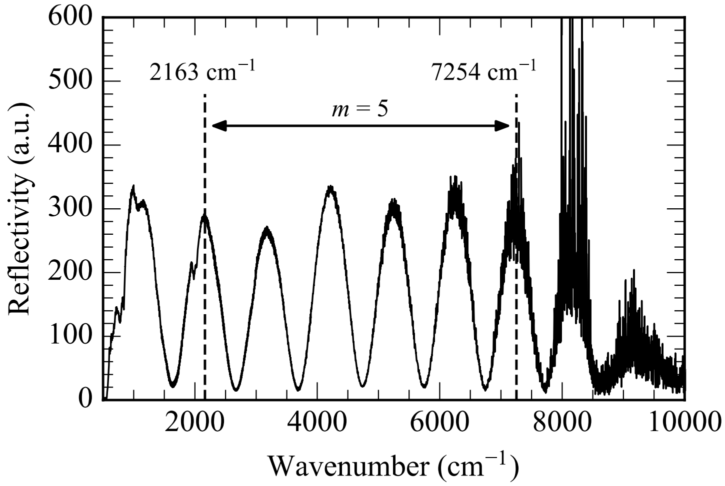

Figure IV 11: Infrared reflectivity spectra of as-prepared mesoporous Ge layer with a thickness of 2.88 µm and a porosity of 72%. There are m = 5 clearly defined Fabry-Perot fringes between 2163 and 7254 cm^{-1} (δv = 5061 cm^{-1}).

In the approximation of an isotropic medium, the Landau-Lifshitz-Looyenga model [187] is well suited for determining the porosity of the mesoporous Ge layer. In the case of freshly prepared porous Ge, the refractive index is a weighted average of the refractive indices of Ge and air:

$$P = \frac{n_{PGe}^{2/3} - n_{Ge}^{2/3}}{1 - n_{Ge}^{2/3}} \qquad (S2)$$

where we have taken the refractive index of air to be unity. The refractive index of Ge is reasonably stable around $n_{Ge} \approx 4$ in the range of interest.

The porous layer thickness for the sample corresponding to the data in figure S1 is 2.88 μm, and so the calculated porosity is 72%.

IV.8.2 Relationship between annealing temperature and surface crystallite size

Figure 10 shows the average crystallite size of mesoporous Ge for various annealing temperatures, depicted as an Arrhenius plot. The activation energy (E_a) for this mass-diffusion process is found to be 0.69 eV, larger than the activation energies found for sintering of porous Si (0.16 – 0.23 eV).[99], [242] The crystallite size varies strongly with temperature and obeys the Arrhenius-like relation:

$$d_{\mathrm{crystallite}} \propto \exp\left(-\frac{E_a}{kT}\right) \quad \text{(S3)}$$

where k is the Boltzmann constant.

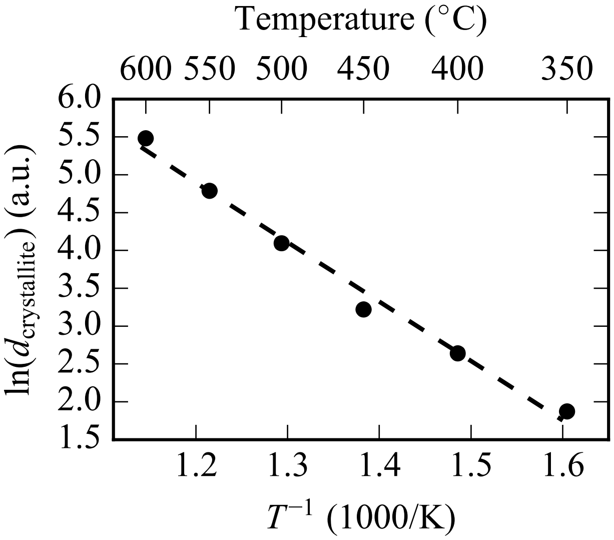

Figure IV 12: Arrhenius-like plot of the temperature-dependent crystallite size (dcrystallite) of annealed mesoporous Ge.

IV.8.3 Defining the space charge region and the Fermi level

By Gauss' law under the depletion approximation, the electric potential in the cylindrical pore unit cell, calculated relative to the center of the void, is

$$\phi_{\mathrm{cyl}}(r) = \begin{cases} 0, & 0 \leq r < a \\ \dfrac{qN_{\mathrm{a}}}{2\varepsilon_{\mathrm{r}}\varepsilon_0}\left[\dfrac{r^2 - a^2}{2} - (W+a)^2 \ln\left(\dfrac{r}{a}\right)\right] & a \leq r < W+a \\ \dfrac{qN_{\mathrm{a}}}{2\varepsilon_{\mathrm{r}}\varepsilon_0}\left[\dfrac{(W+a)^2 - a^2}{2} - (W+a)^2 \ln\left(\dfrac{W+a}{a}\right)\right] & r \leq W+a \end{cases} \tag{S4}$$

Similarly, for the spherical void unit cell, the potential is given by

$$\phi_{\mathrm{sph}}(r) = \begin{cases} 0, & 0 \leq r < a \\ \dfrac{qN_{\mathrm{a}}}{3\varepsilon_{\mathrm{r}}\varepsilon_0}\left[\dfrac{r^2 - a^2}{2} - (W+a)^3 \left(\dfrac{1}{r} - \dfrac{1}{a}\right)\right] & a \leq r < W+a \\ \dfrac{qN_{\mathrm{a}}}{3\varepsilon_{\mathrm{r}}\varepsilon_0}\left[\dfrac{3(W+a)^2 - a^2}{2} - \dfrac{(W+a)^3}{a}\right] & r \leq W+a \end{cases} \tag{S5}$$

All parameters are defined in table S1.

Parameter	*Description*	*Value/Units*
q	Elementary charge on an electron.	C (f.c.)
ε_{r}	Relative permittivity (Ge).	16.2
ε_0	Vacuum permittivity.	F/m (f.c.)
N_{a}	Doping concentration.	cm^{-3}
N_{s}	Surface state density.	$\mathrm{cm}^{-2}\ \mathrm{eV}^{-1}$
N_{v}	Effective density of states in the valence band (Ge).	$5 \times 10^{18}\ \mathrm{cm}^{-3}$
E_{v}	Valence band edge.	eV
A_{void}	Surface area of a void.	cm^2
$V_{\mathrm{S.C.}}$	Volume of the space charge region.	cm^3

Table IV 1: List of parameters used in determining the space charge region and the Fermi level. Fixed values are given, fundamental constants are indicated by (f.c.).

The space charge width W is calculated using the charge neutrality condition where it is assumed that the charges contributed by the positively charged surface states (Q_{S}) and by the ionized acceptor atoms (Q_{V}) sum to zero.

$$Q_{\mathrm{S}} + Q_{\mathrm{V}} = 0 \tag{S6}$$

$$Q_{\mathrm{S}} = qN_{\mathrm{s}}\, A_{\mathrm{void}}\, (\Phi_0 - E_{\mathrm{F}}) \tag{S7}$$

$$Q_{\mathrm{V}} = -\, qN_{\mathrm{a}}\, V_{\mathrm{S.C.}}(W) \tag{S8}$$

We first assume that the space charge region has the same symmetry as the void (either cylindrical or spherical). Assuming all acceptor atoms are fully ionized, the Fermi level E_F is found using the standard expression for the carrier concentration in a bulk semiconductor

$$p_0 = N_\mathrm{v}\, \mathrm{e}^{-\frac{E_\mathrm{F} - E_\mathrm{v}}{kT}} \cong N_\mathrm{a} \tag{S9}$$

The valence band edge E_v, indicated in Figure 9c, is given by

$$E_\mathrm{v} = - q\phi(W_0 + a) \tag{S10}$$

using ϕ_cyl or ϕ_sph, as appropriate. The baseline width of the space charge region (W_0) is found by numerically solving the transcendental equation (S6). There are three scenarios that arise, depicted in figure S3.

a) The space charge region is fully contained within the unit cell. In this case, the Fermi level is appropriate and we can proceed with $W \equiv W_0$.

b) The baseline space charge width W_0 extends beyond the boundaries of the unit cell in some directions but not in others. In this case, we define a space charge region that is no longer symmetrical about the void and is instead bounded by the unit cell wherever W_0 extends beyond its boundaries. W_0 is incremented in steps of 0.01 nm until either the charge neutrality condition is satisfied or the space charge region reaches the boundaries of the unit cell in all directions (see case iii).

c) The baseline space charge width W_0 extends beyond the boundaries of the unit cell in all directions. In this case, we assume the entire unit cell is depleted of carriers and adjust the Fermi level to satisfy the charge neutrality condition (S6). The final space charge width is maximized such that $W = d\frac{\sqrt{3}}{2} - a$.

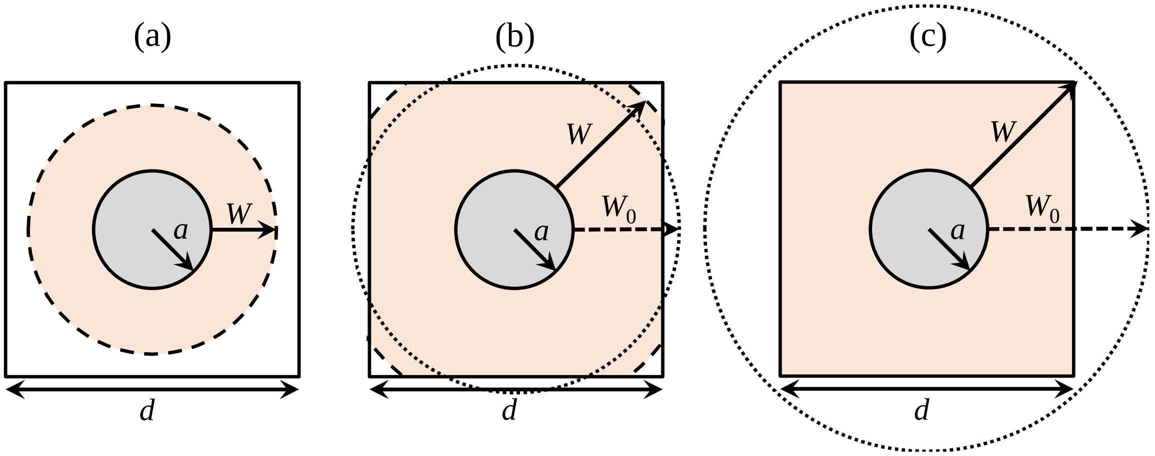

Figure IV 13: (a) Space charge region is contained within the unit cell. (b) When the baseline space charge width W_0 extends beyond the boundaries of the unit cell in some directions, the width is redefined so that it is fully contained. (c) When the baseline space charge width extends beyond the boundaries of the unit cell in all directions, the width is redefined to terminate at the boundaries of the unit cell and the Fermi level is adjusted accordingly.

IV.8.4 Mobility contributions from lattice and charged impurity scattering

The Ge p-type mobility comprises components due to lattice scattering and due to scattering of charged impurities. This is calculated according to Klaasen's unified mobility model [240]

$$\mu_{\mathrm{Ge}} = \left(\frac{1}{\mu_{\mathrm{lattice}}} + \frac{1}{\mu_{\mathrm{impurities}}}\right)^{-1} \tag{S11}$$

$$\mu_{\mathrm{lattice}} = \mu_{\mathrm{max}} \tag{S12}$$

$$\mu_{\mathrm{impurities}} = \frac{\mu_{\mathrm{max}}^2}{\mu_{\mathrm{max}} - \mu_{\mathrm{min}}}\left(\frac{N_{\mathrm{ref}}}{N_{\mathrm{a}}}\right) + \frac{\mu_{\mathrm{max}}\mu_{\mathrm{min}}}{\mu_{\mathrm{max}} - \mu_{\mathrm{min}}}\left(\frac{p_{\mathrm{ave}}}{N_{\mathrm{a}}}\right) \tag{S13}$$

with parameters from Palankovski [241] given in table S2.

For bulk Ge, the average carrier concentration is roughly equal to the doping density ($p_{\mathrm{ave}} \approx N_{\mathrm{a}}$) and Klaasen's model gives identical results to Palankovski. In mesoporous germanium, $p_{\mathrm{ave}} < N_{\mathrm{a}}$ and so the resulting mobility calculated using Klaasen's model is lower than results computed according to Palankovski.

Note that this model is only valid at room temperature and does not include minority impurity scattering or electron-hole scattering as these effects are assumed to be negligible for this system.

Parameter	*Value*
μ_{max}	1800 cm^2/Vs
μ_{min}	300 cm^2/Vs
N_{ref}	10^{17} cm^{-3}

Table IV 2: Parameters from Palankovski used for calculating the p-type carrier mobility of bulk germanium at room temperature.

IV.8.5 Effect of interface state density on transport model

The interface state density for mesoporous Ge has not yet been measured, and so estimated values from the literature are used in the electrostatic model that has been described. Here, the impact of the surface state density on simulated transport properties is explored for densities ranging from 5×10^{12} to 5×10^{15} cm^{-2} eV^{-1}.

As the interface state concentration increases, we first see a large drop in average carrier concentration (figure S4a); however, for interface state densities exceeding 5×10^{13} cm^{-2} eV^{-1}, the number of surface states is so large that enlarging the interface state density further has minimal impact. Conversely, the impact of the interface states on mobility becomes dominant as the interface state density increases (figure S4b). Overall, the resistivity increases considerably with increasing surface state density, as shown in figure S4c. It should be noted that the calculations shown in figure S4 were done using the fitting parameter C ~ 320,000 cm^{-1} V^{-1} s^{-1}, which was obtained by comparison to experiment assuming an interface state density of 4×10^{14} cm^{-2} eV^{-1}. If the true interface state density of the material differs from this value, the fitting parameter C must differ as well, and so the mobilities and resistivities shown in figures S4b and c would change accordingly; however, the general trends shown in figure S4 would be the same.

Ultimately, obtaining an accurate measurement of the interface state density for mesoporous Ge and establishing the effect of annealing on this value will greatly improve the accuracy of this model for the material systems under investigation. Furthermore, the preliminary simulation results shown in figure S4 suggest that surface treatment in order to reduce the interface state density (see for example [243], [244]) in addition to varying the morphology may prove to be highly effective in tuning the conductivity of mesoporous Ge films.

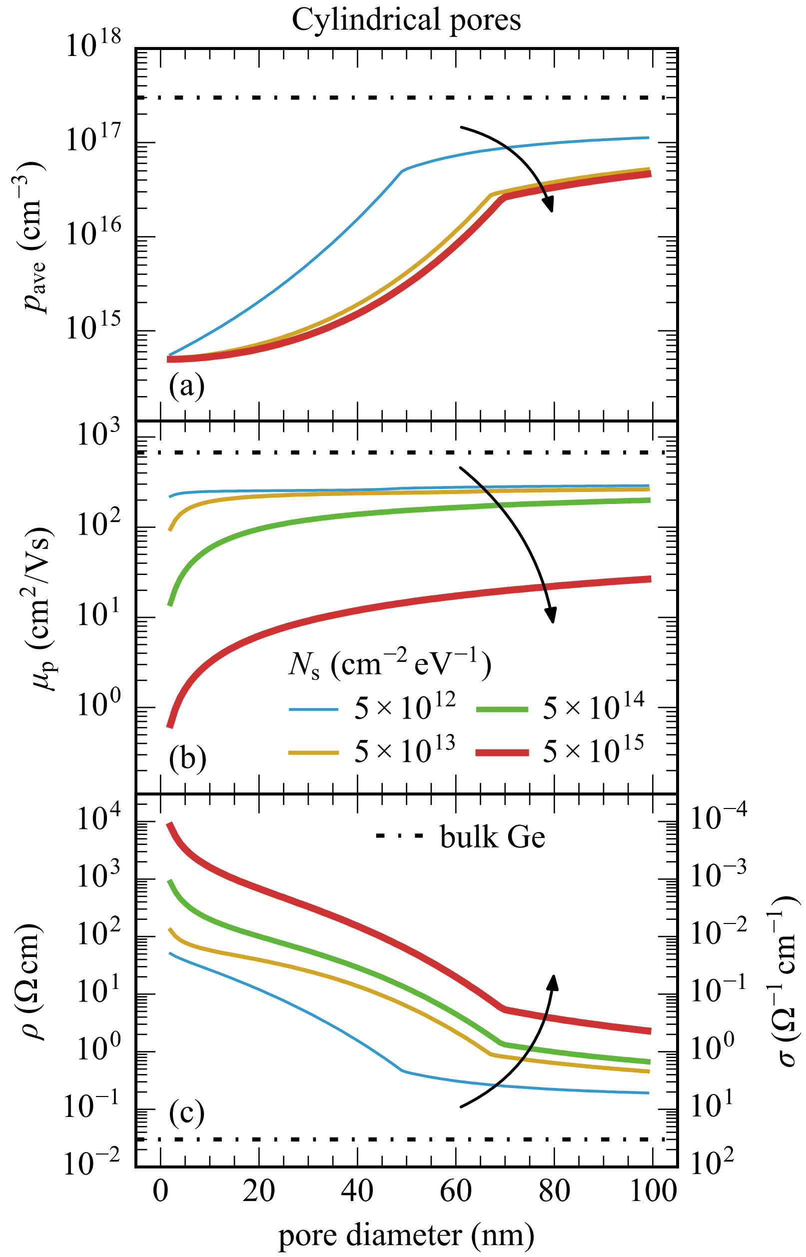

Figure IV 14: (a) Modelled average free carrier concentration, (b) carrier mobility, and (c) resistivity of mesoporous Ge as a function of pore/void size for interface state densities ranging from 5×10^{12} to 5×10^{15} cm^{-2} eV^{-1}. Conductivity is shown on the secondary y-axis of (c). A doping concentration of 3×10^{17} cm^{-3} and a porosity of 50% are assumed. Arrows indicate direction of increasing interface state density. Values for bulk Ge are shown.

CHAPITRE V ARTICLE: INGÉNIERIE DE DÉFAUTS PAR REPRISE DE CROISSANCE ÉPITAXIALE SUR GERMANIUM POREUX-SUR-SILICIUM

V.1 Avant-propos

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Référence: [51]

Titre français: Élaboration de couches de germanium de haute qualité par reprise de croissance sur un substrat modifié de Ge/Si poreux

Contribution au document: Cet article contribue à la thèse par une approche alternative pour la réduction de la densité des dislocations, ainsi qu’en démontrant des phénomènes d’interaction entre les dislocations et les cavité nanométrique.

Résumé français:

Des couches épitaxiées de germanium de haute qualité sur Si avec une faible densité de dislocation (TDD) ont été obtenues par croissance épitaxiale sur un substrat de Ge/Si poreux. Cette approche consiste en la formation des nanostructures poreuses de Ge par gravure électrochimique sélective aux dislocations suivie d'une surcroissance de germanium à haute température pour transformer la structure nanoporeuse en une couche de Ge intermédiaire riche en nano-cavités. Ces nano-cavités offrent des surfaces libres pour la terminaison et le piégeage des dislocations, permettant à cette approche de réduire les dislocations de plus de trois ordres de grandeur, de ~ 10^7 cm^{-2} à ~ 10^4 cm^{-2} pour les couches de Ge de 2 μm. En utilisant cette approche, un substrat virtuel de Ge/Si épi-prêt est produit à plus grande échelle jusqu'à 4 pouces, ce qui permet d'intégrer des dispositifs à haute performance sur Ge/Si et ouvrirait la voie aux dispositifs III-V à l'intégration sur la plate-forme Si.

High quality germanium epitaxial overgrowth on porous Ge-on-Si engineered substrate

V.2 Abstract

High-quality germanium epilayers on Si with low threading-dislocation densities (TDDs) were achieved by epitaxial overgrowth on porous Ge/Si approach. This consists on the formation of porous Ge nanostructures by dislocation-selective electrochemical deep etching of Ge/Si films followed by an overgrowth of germanium a high temperature to transform the nanoporous structure into an intermediate voided Ge layer. These nanovoids offer free surfaces for dislocation termination and trapping, enabling the EOP approach to reduce dislocations by over three orders of magnitude, from ~10^7 cm^{-2} to ~10^4 cm^{-2} for 2 μm thick Ge layers. By using this approach, an epi-ready Ge/Si engineered substrate is produced on a larger scale dimension up to 4 inches, which enables to integrate high performance Ge devices on Si and would open the way for III-V devices on integration on the Si platform.

V.3 Introduction

The integration of various optoelectronic devices on Si is one of the most important challenges in current electronic materials research. This technological issue is mainly due to the incompatibility of these materials with Si. Developing high quality, crystalline Ge-on-Si substrates, with low-cost, scalable techniques, has the potential to exploit the optical and electronic functionality of Ge based devices such as photodetectors, [245] microprocessors, [246] and modulators [247]. In addition it would allow to integrate GaAs and other III-V compound on Si due to close lattice constant with Ge, and this would allow various devices including: multi-junction solar cells on Si, [248]–[250] and CMOS [251]. However, due to the 4.2% lattice mismatch and 116% thermal expansion coefficient mismatch between silicon and germanium, the deposition of a Ge layer on Si remains challenging. The large lattice mismatch induces a strain at the interface which will leads by the generation of a network of threading dislocations extending to the surface, above a certain critical thickness [252]. Furthermore, the thermal expansion coefficient mismatch can lead to micro-cracks in Ge films or their eventual delamination, as the film thickness exceeds several micrometers [253]. In general, these defects act as nonradiative recombination and scattering centers that impact the diffusion length[254] and minority carrier lifetime [255], reduce thermal conductivity, [256] and form easy pathways for impurity diffusion. Thus, they strongly deteriorate the performance, and reliability of optoelectronic devices [257], [258]. Early attempts of dislocation control were in-situ epitaxial methods involving compositional grading, [259]–[261] and low/high temperature two-step growth [262], in addition to cyclic thermal annealing [263]. Alternative approaches based on engineering dislocations have been shown to be effective in reducing the threading-dislocation densities in Ge grown on Si, such as, selective area growth [264], epitaxial necking, [265] epitaxial lateral overgrowth, [266], [267] mesa structuring, [268] 3D heteroepitaxy, [269] aspect ratio trapping [270], [271] and ion implanted substrates [272]. Although technical reports on engineering dislocations have been published, the improvement of device performance after these processes is still very limited in regions with high dislocation densities (~10^6 cm^{-2}) [258], [273]. Furthermore, many of these techniques are limited to small-scale processes and require the use of expensive and complex processing technologies [14]. Hence, the compliant substrate based on porous structure appear to be promising candidate for the epitaxy of heterogeneous systems, and offers some distinctive advantages, such as, flexible material, scalable process and compatibility with microelectronic technology. It is therefore expected to accommodate the mismatch of heterogeneous layers and to serve as a mechanically stretchable pseudo substrate [274]–[276]. More recently, we have shown that the morphological transformation of mesoporous materials, which generate nanovoids, could trap dislocations. In this letter, we exploit this effect to create a high quality germanium virtual substrate. Our Ge layers grow strain free and exhibit dislocation densities below 10^4 cm^{-2}, indicate that the resulting substrate may represent an ideal platform for the integration of III-V alloys, could improve the device performance and may lower their producing costs.

V.4 Results and discussions

The epitaxial overgrowth on porous Ge/Si EOP approach is a three-step process, including a post-epitaxy step, as shown in Fig. 1. First, it starts with a commercial bulk Ge film, 1 μm thick, grown by the metal organic chemical vapor deposition on a 4” Si (001) wafer with a dislocation density of ~10^7/cm^2. The next step consists on dislocation-selective electrochemical deep etching to form porous Ge nanostructures from the bulk-grown Ge film, as shown in Figure 1(b). The final step consists of homoepitaxial Ge overgrowth, voids formation, dislocation trapping, and annihilation by nanovoids, as seen in Fig. 1(c).

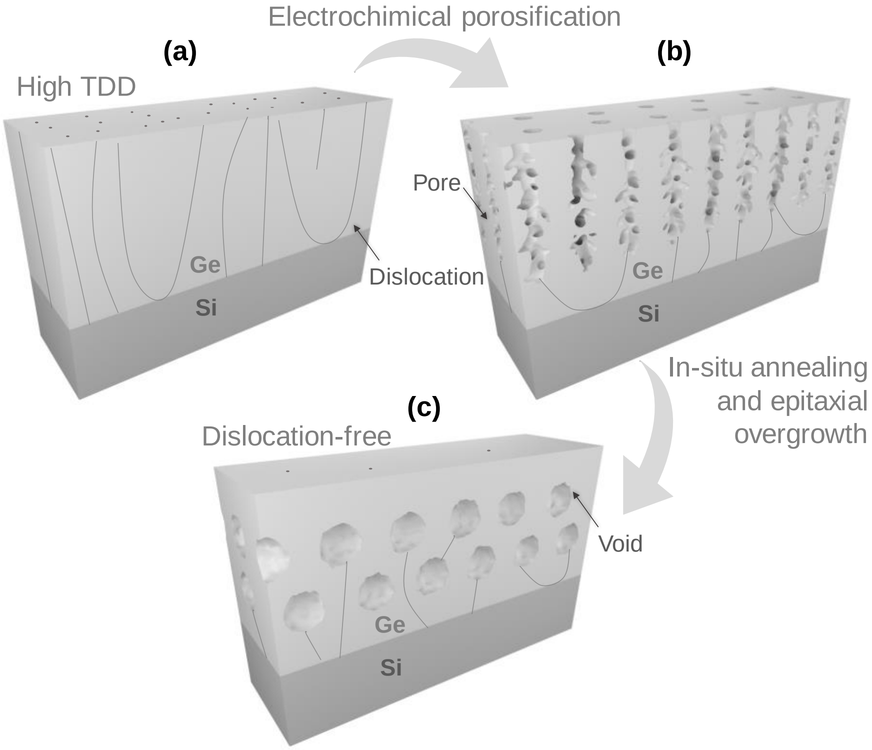

Figure V 1: 3D schematics of epitaxial the overgrowth on porous Ge/Si (EOP) approach. (a) Bulk Ge film growth on (001) Si substrate, (b) nanoporous Ge layer formation by dislocation-selective electrochemical deep etching and (c) in-situ annealing, Ge overgrowth and voids creation.

Nanoporous Ge layers are fabricated on dislocated Ge/Si (001) films by bipolar electrochemical etching (BEE) [204], [277], [278] in a two-electrode electrochemical cell with a platinum wire counter electrode manufactured using an electrolyte consisting of 5:1 hydrofluoric acid (49%) and anhydrous ethanol. Electrical contact is established by pressing the backside of the wafer onto a gold-coated copper electrode. A DC initiation step is used during etching which an anodic etching current of +1.5 mA/cm^2 is applied for

10 s. After that, anodic and cathodic currents with a density of ±3 mA/cm^2 is applied alternately with pulse durations of 1 s, during 30 min. The initiation step is necessary to ensure the formation of a uniform Ge nanoporous layer[204]. After etching, the samples are rinsed in de-ionised water, blown dry with nitrogen; then introduced promptly into the loading chamber of the Reduced Pressure Chemical Vapour Deposition (RP-CVD) reactor, to avoid the Ge oxidation. Before the growth, the porous Ge/Si layer has undergone an in-situ annealing at 550°C during 10 min, in a forming gas (N_2:H_2 90:10) ambient with a ramp rate of 25 °C/s, in order to transform the nanoporous structure into quasi-monocrystalline voided Ge layer. An additional 1µm of Ge is deposited using GeH_4 precursor including 100 nm thick low temperature Ge at 400°C followed by a high temperature layer, which is grown at 600 °C.

Fig. 2(a) shows top scanning electron microscopy (SEM) image of the porous Ge/Si layer. A uniform distribution of nano-sized pores with etch-pits in the range of 50 nm is shown (the inset). These large pores are formed at the dislocation sites; extend down from the surface, which essentially reveal the emergent point of dislocations at the surface. Contrary to bulk Ge porosification, in which, the layer structure shows uniformly distributed nanopores with controllable nanostructure and size, dislocated Ge/Si substrates show a thick porous Ge layer with weakly branched pores selectively crossing threading dislocation cores, as shown in Fig. 2(b). This preferential anodic etching through dislocations could manifest itself as a local effect. In fact, the impurity gettering by the dislocation core increases doping concentration locally, which is reflected by the displacement of the Fermi level [279]. As a result, a lower energy barrier increases Ge dissolution during anodization, thus accelerating pore formation around dislocations, which are considered as selective nucleation sites.

At an annealing temperature of 550°C, a significant morphological transformation occurred, in which the porous structure self-organized into a network of nanovoids following the dislocation lines. The driving force for the spherodization of pores results from the system’s tendency to minimize its total surface energy, in which the Ge atoms on the surface move to more favorable energy positions during thermal annealing below the Ge melting point (938°C), and obeys Oswald ripening process [103], [211], [225].

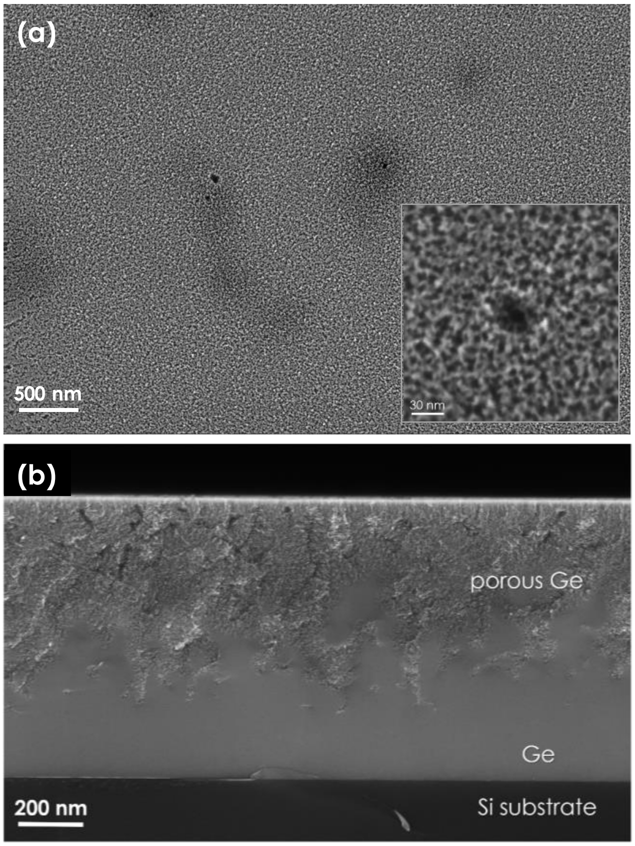

Figure V 2: Planar-view SEM image of porous Ge/Si layer formed at 1.5 mA/cm^2 (a) with a dislocation etch-pit (the inset). (b) Cross-section SEM view showing weakly branched pores crossing threading dislocation cores.

Figure 3(a) shows a SEM image of the Ge film grown over the nanovoided region, indicating that the voids are preserved in the underlying Ge layer. High magnification TEM view reveals the interaction dislocation-voids, and shows clear evidence that threading dislocation can be blocked by nanovoids (see Fig. 3(b)-3(c)). Figure 3(d) shows a bright-field STEM image of the EOP substrate. It shown that the threading dislocations present in the initial Ge/Si growth are confined at the voided Ge region and do not propagate into the overgrown Ge layer. Almost, a dislocation-free region was achieved at the upper part of the voided region. The dislocation pinning at voids depends on several effects including; gliding, [280] climbing processes, [281] interfacial effects [282], and the void size effect [283].

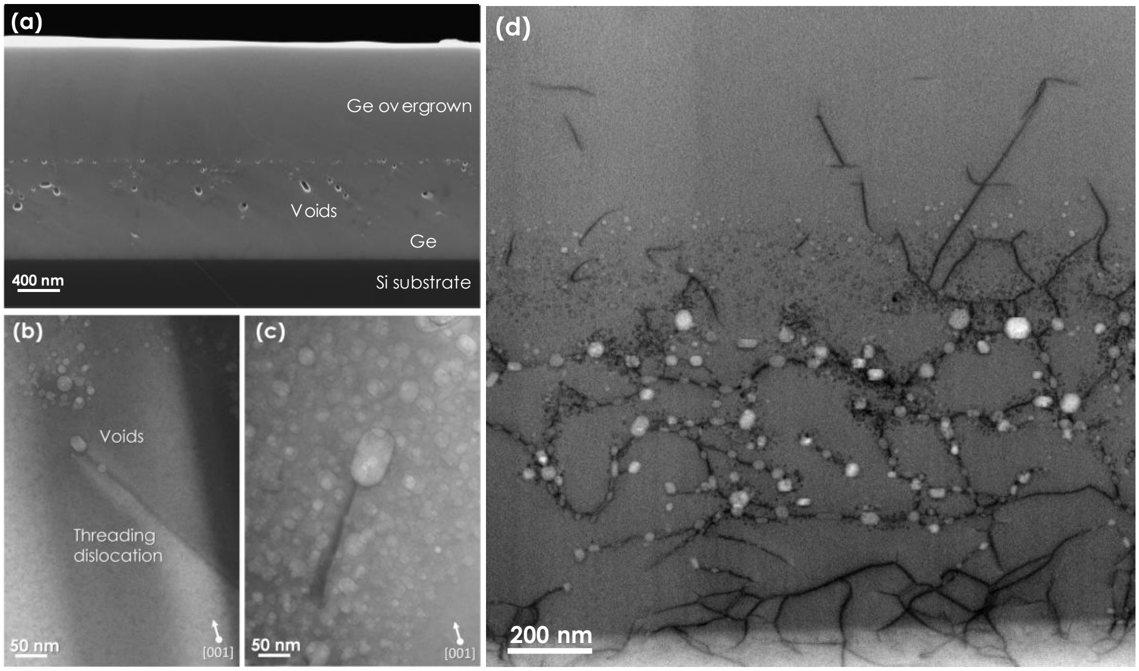

Figure V 3Cross-section SEM view of Ge layer grown on the electrochemically etched nanoporous Ge-on-Si substrate, forming a nanovoided region in the underlying Ge layer (a). High magnification TEM image of the nanovoided Ge layer showing the termination of a dislocation segment in the nanovoid area (a,c). Bright-field STEM image shows a dislocation network confined at the nanovoided region with no propagation beyond (d).

Fig. 4(a) indicates clearly that the dislocations cut through the small voids without being trapped. For the larger voids, the obstacle strength dominates, causing the dislocation to be pinned by the voids and to bow under the internal shear stress. For large voids that are sufficiently spaced-out, dislocation can bypass the obstacle via the Orowan mechanism [284]. The critical stress τ_c required for an edge dislocation to pass the array of voids was determined according to [284]–[286]:

$$\tau_c = \frac{\mu b}{2\pi L}\left[ln\frac{\overline{D}}{b} + \Delta\right] \qquad eq. 1$$

Where $\Delta = 0.77$ for impenetrable obstacles and $\Delta = 1.52$ for voids [287]. D the void diameter, L the void spacing, $\overline{D} = (D^{-1} + L^{-1})^{-1}$, μ is the shear modulus and b the magnitude of the Burgers vector.

To identify the minimum resolved shear stress required a dislocation to be pinned by the voids in this virtual substrate; the experimental void dimensions obtained from Fig. 4(a) are plotted in Fig. 4(b). For two simultaneous voids having not the same diameter, an average diameter D_a is used. The approximates critical stress τ_c for every two void peers are summarized in table 1. τ_c varies from 0.81 GPa to 5.21 GPa depending on void spacing and void diameters. Indeed, voids with the adequate dimensions create a stable energetic well for the dislocations, strongly pinning them in place.

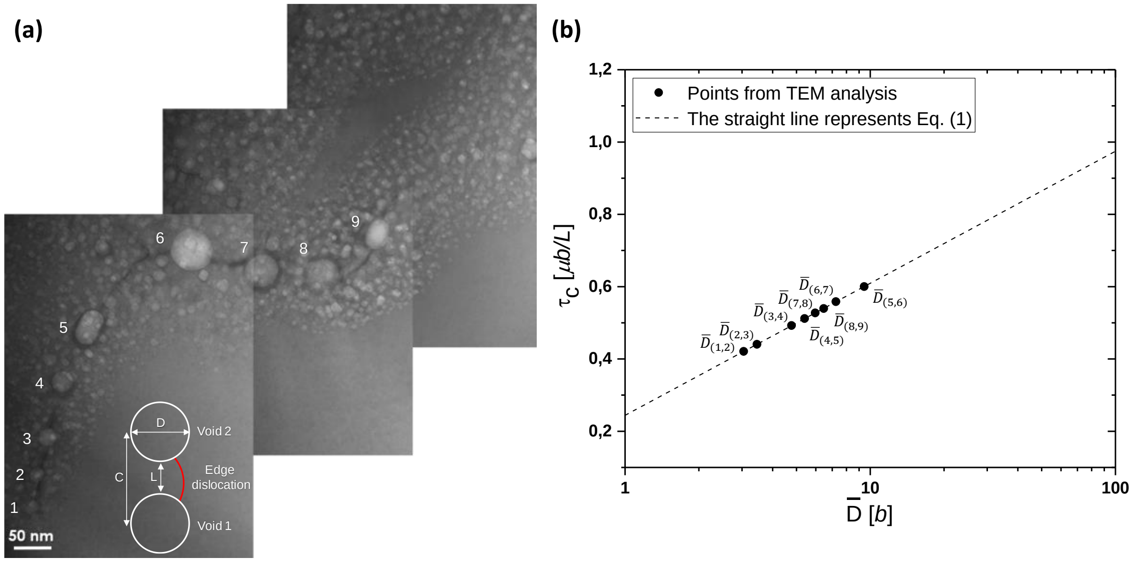

Figure V 4: TEM image shows the pinning of a dislocation segment in the array of nanovoids (a) and schematic illustration of voids parameters (Inset). Normalized τ_c as a function of void size and spacing illustrating the Orowan's model (b). The straight line represents Eq. (1) with experimental void dimensions obtained from (a).

$D_{a_{(n,n+1)}}$		$C_{(n,n+1)}$		$L_{(n,n+1)}$=(C-D_a)		$\overline{D}_{(n,n+1)}$=D_aL/(D_a+L)		$\tau_{c_{(n,n+1)}}$(GPa)	
$D_{a_{(1,2)}}$	16,7	$C_{(1,2)}$	44,9	$L_{(1,2)}$	28,1	$\overline{D}_{(1,2)}$	10,5	$\tau_{c_{(1,2)}}$	0,81
$D_{a_{(2,3)}}$	20,8	$C_{(2,3)}$	48,6	$L_{(2,3)}$	27,8	$\overline{D}_{(2,3)}$	11,8	$\tau_{c_{(2,3)}}$	0,84
$D_{a_{(3,4)}}$	24,0	$C_{(3,4)}$	76,3	$L_{(3,4)}$	52,2	$\overline{D}_{(3,4)}$	16,4	$\tau_{c_{(3,4)}}$	1,77
$D_{a_{(4,5)}}$	29,1	$C_{(4,5)}$	80,7	$L_{(4,5)}$	51,5	$\overline{D}_{(4,5)}$	18,6	$\tau_{c_{(4,5)}}$	1,81
$D_{a_{(5,6)}}$	43,9	$C_{(5,6)}$	170	$L_{(5,6)}$	126	$\overline{D}_{(5,6)}$	32,5	$\tau_{c_{(5,6)}}$	5,21
$D_{a_{(6,7)}}$	50,9	$C_{(6,7)}$	100	$L_{(6,7)}$	49,1	$\overline{D}_{(6,7)}$	24,9	$\tau_{c_{(6,7)}}$	1,89
$D_{a_{(7,8)}}$	42,6	$C_{(7,8)}$	82,4	$L_{(7,8)}$	39,8	$\overline{D}_{(7,8)}$	20,5	$\tau_{c_{(7,8)}}$	1,44
$D_{a_{(8,9)}}$	37	$C_{(8,9)}$	93	$L_{(8,9)}$	56	$\overline{D}_{(8,9)}$	22,2	$\tau_{c_{(8,9)}}$	2,08

Table V 1: Average void diameters (Da) and center-to-center spacing (C) used throughout this work. Harmonic mean defined as ($\overline{D}$) = DL/D+L where L = C-D.

In order to investigate the threading dislocation density using the EOP approach, etch pits are created in the Ge using a solution of 2 volumetric parts 49 wt. % HF and 1 part 0.1 M $K_2Cr_2O_7$ [267]. SEM images from the Ge/Si reference and the EOP substrate, having the same thickness, are presented for comparison in Figure 4(a) and 4(b), respectively. The dislocation density was determined by the revealed pits count in the scanned area. The etch pit density is clearly lower in the EOP substrate compared by the Ge/Si reference without treatment, which confirms that the threading dislocations are effectively blocked from propagating in the voided region. The averaged TD density is reduced significantly from ~10^7 cm^{-2} to ~10^4 cm^{-2} for 2 μm thick Ge layers, which is considered very low for such a thin epitaxial layer [14],[288].

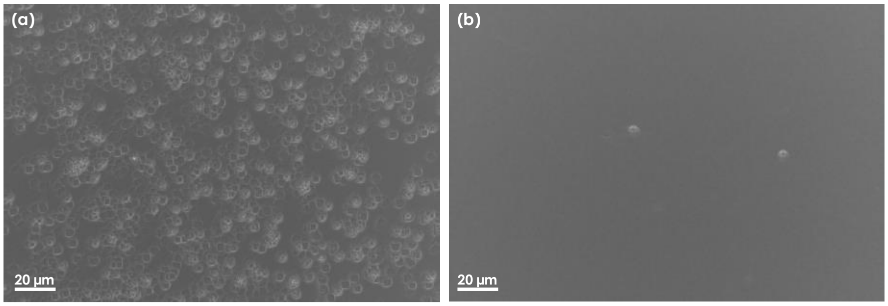

Figure V 5: Etch-pit-density results indicating threading-dislocation density in the sample Ge/Si reference and the EOP substrate. The average TDD is reduced from ~10^7 cm^{-2} to ~10^4 cm^{-2} for 2 μm thick Ge layer using the EOP approach.

We offer three possible explanations of the dislocations reduction by nanovoids. The first concept consists of the elimination of singular screw dislocation by one void. In this case, the atomic step characterizes the initial screw dislocation should be taken up by the lower surface of the void. Consequently, the threading dislocations did not climb through the upper part of the void forming a perfect crystal. Around the void, the crystal should be elastically deformed which requests an atomic arrangement throughout the void surface. This mechanism appears energetically less favorable despite its obvious illustrative appeal (see Fig. (3b) and (3c)). The second concept consists of the elimination of two threading dislocations by the void to produce a single one generating a Y-shaped defect. This so-called “Fusion” is an energetically favorable reaction [289],[290]. The third consists on the annihilation of threading segments with antiparallel Burgers vectors. As an example, threading segments from different dislocation sources on the same slip plane or on the parallel slip can annihilate by gliding, climbing and crossing slip motion [77]. In addition, threading segments on intersecting slip systems can annihilate by glide or by climb or a combination of both glide and climb [291]. As the relative motion between TDs is characterized by a critical interaction radius, the presence of an attractive force created by the nanovoids bring them within a lower reaction distance, in which the TDs begin to glide together and annihilate or fuse [292]. These mechanisms give a reasonable explanation for the dislocations reduction by introducing nanovoids in heteroepitaxial diamond films, in which, the TDs have a critical interaction radius higher than the interaction radius in the conventional structure without voids, which in turn increases their recombination probability.

V.5 Conclusion

In conclusion, we demonstrated the growth of high quality Ge-on-Si exhibiting low threading-dislocation density. Our method, EOP, consisted of trapping and annihilating dislocations propagation by forming nanovoids barrier inside the Ge layer. The process, described in this letter, consisted of the combination of dislocation-selective electrochemical etching with the overgrowth of germanium on porous nanostructures, enabled an average threading-dislocation density as low as $\sim 10^4$ cm^{-2}. TEM and EPD analysis confirm that the dislocations were effectively blocked from propagating in the EOP substrate, and studied different mechanism process for TDD reducing. The developed concept could be applied to many other systems and could serve to facilitate heterogeneous epitaxy on silicon.

V.6 Acknowledgments

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CHAPITRE VI ARTICLE : SUBSTRAT VIRTUEL GERMANIUM-SUR-SILICIUM À BASE DE NANO-CAVITÉS

VI.1 Avant-propos

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Titre français : Déracinement de défauts pour permettre l'émission des matériaux III-V sur Si

Contribution au document : Cet article contribue à la thèse en développant une stratégie pour réduire la densité des défauts par introduction des nono-cavités dans la couche de Ge et dans le substrat de Si. Il introduit des explications profondes sur l'origine des interactions dislocations/cavités. L'approche proposé dans cet article a permis une amélioration de l'efficacité d'émission des matériaux III-V sur Si.

Résumé français :

L'intégration monolithique de dispositifs semi-conducteurs III-V avec du silicium offre une occasion unique pour combiner les fonctionnalités optiques et électroniques de la technologie III-V avec des techniques de production en volume et à faible coût associées au silicium. Cependant, l'intégration de ces matériaux à fort désaccord de maille reste difficile et présente des défis physiques et technologiques menant à la formation de défauts. Dans ce document, une nouvelle stratégie d'élimination des défauts dans l'hétéro-épitaxie à fort désaccord de maille a été démontrée. Elle permet d'obtenir un substrat virtuel d'une densité de dislocation ultra faible, epi-ready et réalisé sur des substrats de grande taille, en utilisant un processus hautement évolutif. Les dislocations sont éliminées de la couche épitaxiale par une attaque électrochimique sélective à travers les dislocations suivie d'un recuit thermique. Ceci permet de créer une barrière de nano-cavités qui piège les dislocations. En conséquence, une couche de Ge continue est obtenue, dans laquelle une grande partie des dislocations émergentes d'origine sont épinglées et annihilées loin de la couche épaisse. La densité de dislocations moyenne est réduite de plus de trois ordres de grandeur, de ~ 10^7 cm^{-2} à ~ 10^4 cm^{-2} pour des couches de Ge de 1,5 μm d'épaisseur. Basant sur des analyses en microscopie électronique à balayage et à transmission, un modèle est proposé pour expliquer les processus physiques à l'origine de l'annulation des dislocations, ainsi que leur interaction avec les nano-cavités. Enfin, grâce à l'ingénierie de défauts par les nanocavités, les propriétés optiques, étudiées par cathodoluminescence à température ambiante, indiquent une forte amélioration du rendement d'émission de films de GaAs crûs sur ce substrat virtuel Ge/Si. En général, ces travaux démontrent des perspectives prometteuses pour le transfert de cette technologie de substrat virtuel à la production de dispositifs photoniques et optoélectroniques intégrés sur silicium avec des économies significatives.

Uprooting defects to enable light-emitting III-V on Si

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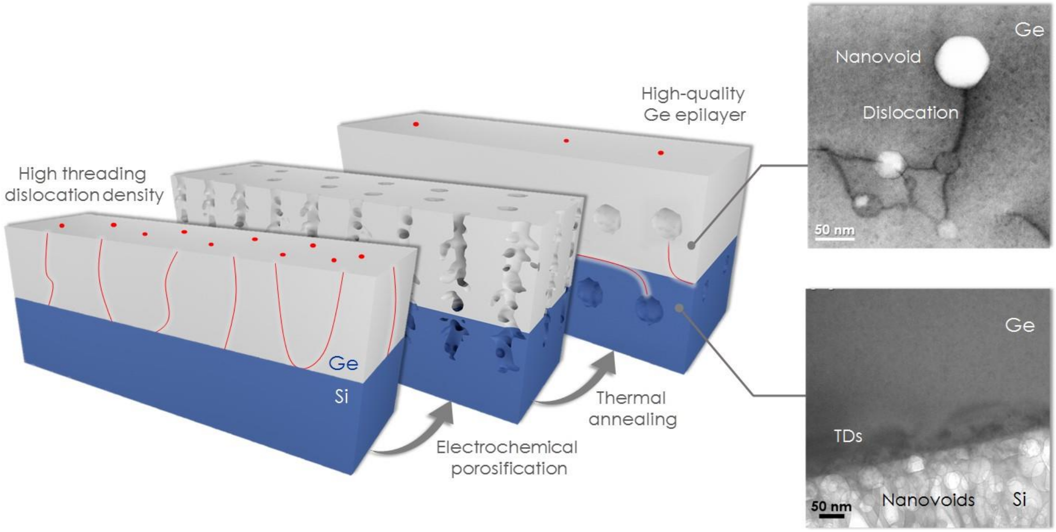
Keywords: defect-engineering, heteroepitaxy, dislocation, nanovoid, Ge on Si virtual substrate



Graphical abstract

VI.2 Abstract

The monolithic integration of III–V semiconductor devices with silicon provides a unique opportunity to combine the optical and electronic functionalities of III–V technology with low-cost volume production techniques associated with silicon. However, the integration of these lattice-mismatched materials remains difficult and presents physical and technological challenges, leading to the formation of defects. Herein, a new defect elimination strategy in highly mismatched hetero-epitaxy is demonstrated to achieve ultra-low dislocation density, epi-ready Ge/Si virtual substrate on a wafer scale, using a highly scalable process. Dislocations are eliminated from the epilayer through dislocation-selective electrochemical deep etching followed by thermal annealing which creates a nanovoid barrier that traps dislocations near the Ge/Si interface. As a result, a continuous Ge layer is obtained, in which, a large portion of the original threading dislocations (TD) are pinned and annihilated far from the epilayer. The averaged TD density is reduced by over three orders of magnitude, from ~10^7 cm^{-2} to ~10^4 cm^{-2} for 1.5 µm thick Ge layers. A model is proposed, based on scanning and transmission electron microscopy to explain the physical processes behind the annihilation of TD as well as their interaction with nanovoids. Finally, the optical properties, investigated using room temperature cathodoluminescence, indicate a strong enhancement of emission efficiency in GaAs grown on this Ge/Si virtual substrate, thanks to defect engineering by nanovoids. Collectively, this work demonstrates the promise for transferring our virtual substrate technology to the industrial scale production of integrated photonic and optoelectronic devices on Si platforms with significant cost-effective saves.

VI.3 Introduction

Developing inexpensive, high-performance epitaxial devices with the hope of achieving widespread market adoption, depends critically on production costs and ultimate material quality. Any process that meets these challenges successfully provides solutions for a wide range of leading-edge applications, in different areas, including energy, photonics, electronics, communications and health care. The last decade has witnessed important progress in many advanced technologies based on mismatched hetero-epitaxial semiconductors [293], [294]. As an example: A GaInP/GaAs//GaInAsP/GaInAs four-junction solar cell achieves a record efficiency of 46% exceeding those of other technologies [295].This structure must however combine two tandem cells grown on different lattice constant substrates and subsequently bonded together. This application demonstrates how powerful heterogeneous material integration can be, however the monolithic integration of high-quality mismatched semiconductors remains difficult due to the large difference in the lattice constant and thermal expansion coefficients between the epitaxial materials and hetero-substrates [296]. During growth, the strain introduced in the epitaxial layer will be either stored as strain energy in the film or accommodated by a network of misfit dislocations at the interface above a certain critical thickness, depending on the lattice mismatch [252]. Misfit dislocation segments are always accompanied by a high density of threading dislocations extending to the surface [297]. Threading dislocations (TD) are most undesirable, because they may penetrate active device regions and generate a variety of detrimental effects, such as, non-radiative recombination centers for carriers, reducing their mobility and lifetime [298], [299] optical birefringence [300] or parasitic current leakage paths [301]. Devices like photodetectors [245], [302], multi-junction solar cells [250], microprocessors [246], modulators [247], based on Ge-on-Si (001) technology are facing these issues. To this end, several approaches have been proposed for reducing the TD density, such as compositional grading [303], cyclic annealing [263], [304], epitaxial lateral overgrowth [266], selective area depositions [264], 3D heteroepitaxy [269], virtual graded layers [305], mesa structuring [268], compliant substrates [306], and ion implanted substrates [272]. Despite their feasibility and originality, many of these techniques are limited to small scale processes and require the use of expensive and complex processing technologies [14]. Despite the implementation of mitigation measures, in a number of these devices, the TD density remains high (~10^6 cm^{-2}) [304]. Alternatively, a new approach called “aspect ratio trapping (ART)” has been proposed as one of the strategies that has the potential to completely annihilate dislocations [270], [271]. Through the use of substrate patterning, the ART method favors the termination of TD at free surfaces on the side facets of the patterns, leading to a confinement of dislocations in lateral sectors or their termination [307]. However, nanoscale patterning lithography and the discontinuous characteristics of the resulting Ge/Si films, can limit their application.

By tuning dislocation motion in relaxed Ge epilayers grown on Si substrates through self-assembling nanovoids, this work aims at providing a reliable and inexpensive approach for achieving very low dislocation densities produced on a wafer scale.

One area in which the approach proposed herein can provide a significant opportunity is the fabrication of virtual substrates for III-V multi-junction solar cells (MJSC) on a Si. As a result, significant cost savings become possible if the bulk Ge substrates would be replaced with our virtual analogs consisting of micron-thick, or even less, Ge buffers grown on Si wafers. The cost reduction per solar cell can be as high as 75% when the much lower prices and larger areas of Si wafers are considered [308]. Additionally, this approach would offer a viable path toward the monolithic integration of mismatched Ge/Si in CMOS circuits and overcome their imminent performance limitation [309], [310].

This work shows that dislocation-engineering using nanovoids in the heteroepitaxy of Ge/Si can be a plausible path for monolithic integration of high quality GaAs on Si platform. The innovation here is to use this strategy in mismatched Ge/Si structure, which reveals new beneficial phenomena for reducing the threading dislocation density (TDD). Possible mechanisms responsible for TD reduction that lead to either annihilation or fusion through nanovoids have been discussed. In addition, strengthening effects due to the interaction between edge dislocations and voids, particularly, threading-arm pinning have been demonstrated. The results show clear evidence that introducing nanovoids increased recombination probabilities of threading dislocations by increasing their interaction radius, drastically reducing their presence within the Ge layer. Therefore, cathodoluminescence (CL) measurements shows an increased CL signal from the GaAs layer on the engineered Ge/Si substrate, in stark contrast to the CL signal from the GaAs layer on a conventional Ge/Si substrate. Such an enhancement is attributed to the role of nanovoids in reducing the dislocation density.

VI.4 Results

VI.4.1 Ge/Si Virtual Substrate: Design and Fabrication

In this work, a Ge/Si substrate is treated with a post epitaxial process to create a region with a high density of nanovoids within the Ge/Si structure, which acts as a free surface that blocks dislocation propagation. Schematically shown in Figure 1, nanovoids are formed in the Ge layer as well as in the Si substrate by electrochemical porosification, followed by thermal annealing giving a new configuration referred to as "Nanovoid-based Ge/Si Virtual Substrate (NVS)".

Firstly, Ge/Si (001) samples with high TDD are anodically porosified by the bipolar electrochemical etching technique previously described [204], [278]. Contrary to bulk Ge porosification, in which, the layer structure shows uniformly distributed mesopores with controllable nanostructure and size [277], [311], dislocated Ge/Si substrates show selectively distributed mesopores. Typical SEM views at low and high magnifications of the mesoporous Ge/Si layer prepared under 1.5 mA/cm^2, are presented in Figure 2a and b, respectively. Large pores in the range of 50 nm are formed at the dislocation sites, which essentially reveal the emergent point of the dislocations in the surface. This is reflected in the cross-sectional view by a thick porous Ge (PGe) layer with weakly branched pores that tend to follow threading dislocation cores, as shown in Figure 2c.

Calibration of porous layer parameters, such as etching rate, has been done by varying the current density in the electrochemical process of bulk and dislocated Ge in Figure 2d. The etch rate ratio between dislocated and bulk regions shows very high values up to 6. Beyond 3.7 mA/cm^2, porous Si layer was obtained by HF crossing dislocations. Figure 2e shows a dark-field TEM image of porous Ge/Si formed using 4 mA/cm^2 for the electrochemical etching for a period of 30 min. The porosification front has reached the Ge/Si heterointerface, by following primarily threading segments, and by uprooting the misfit dislocations. A porous Si layer of 200 nm is formed after 35 min, even before the complete porosification of the Ge layer (see Figure 2f and g).

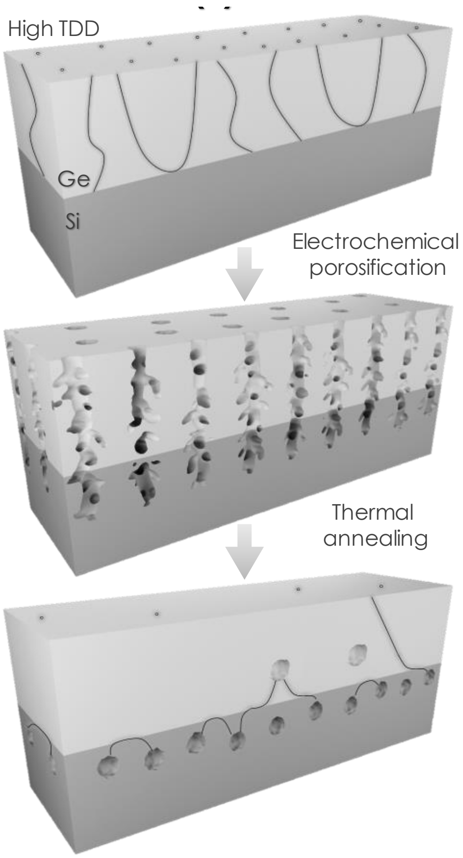


Figure VI 1: Schematic illustration of the nanovoid based Ge/Si virtual substrate (NVS) architecture.

Figure 2h shows schematically the energy band diagrams of p-doped Ge with HF electrolyte, in the case of bulk and dislocated substrates, showing the surface energy band bending in each case. At thermodynamic equilibrium, the Fermi energy (E_f) in Ge is aligned with the equilibrium energy (µ) of the electrolyte, causing the formation of an electrical double layer form the electrolyte side and the surface charge region (SCR) within the electrode. As a result, the energy bands bends close to the Ge surface and a Schottky barrier ($e\Delta\Phi_{SCL}$) that inhibits holes injection across the interface is formed. When a positive bias is applied to the Ge electrode, the SCR is reduced and valence band holes begin to accumulate at the interface. The holes participate in the electrochemical etching reactions according to:

$$\mathrm{Ge} + 6\mathrm{HF} + 4\mathrm{h}^{+} \rightarrow \mathrm{H_2GeF_6} + 4\mathrm{H}^{+}$$

The preferential anodic etching through dislocations could manifest itself as a local effect. In fact, the impurity gettering by the dislocation core increases doping concentration locally, which is reflected by the displacement of the Fermi level [279]. As a result, a lower energy barrier $e\Delta\Phi_{SCL}$ increases Ge dissolution during anodization, thus accelerating pore formation around dislocations, which are considered as selective nucleation sites. Another effect, which could stimulate this localised dissolution, can be seen from a structural viewpoint, the lattice is locally distorted for a distance of a few atoms around dislocations. As a result of the stress field generated by the deformation, the lattice elements dissolve more easily at the dislocation sites than in stress-free, undeformed areas. Such preferential porosification significantly enhances the atomic mobility allowing preferential diffusion paths for voids and dislocations during annealing.

The next step consists of thermally induced structural reorganisation of the porous nanostructure. The morphological change of porous Ge/Si during annealing is based on thermally activated diffusion of surface atoms to stable positions following a surface diffusion mechanism, for which atoms seek a maximum of covalent bonds until their outer energy level is full [99]. The driving force for the spherodization of pores results from the system's tendency to minimize its total surface energy. Such a change has been previously observed following to Rayleigh instabilities [312], [313]. Depending on the annealing temperature, different void shapes in the Ge layer are obtained (see Figure VI 7. Supporting information), which are in a good agreement with the theory describing Oswald ripening phenomenon [314], in which smaller voids tends to merge together in order to create larger voids in a process that is driven by reducing the total surface energy. The restoration of the bulk order of the annealed porous Ge matrix is confirmed by micro-Raman spectroscopy (Figure VI 7. Supporting information).

The void formation in the Ge layer occurs in an isotropic manner, thanks to the dislocation-selective electrochemical etching, and in an anisotropic manner in the Si substrate (Figure 4a). Our observations show that this architecture is effective in reducing the TDD and confining them to the voids' surrounding.

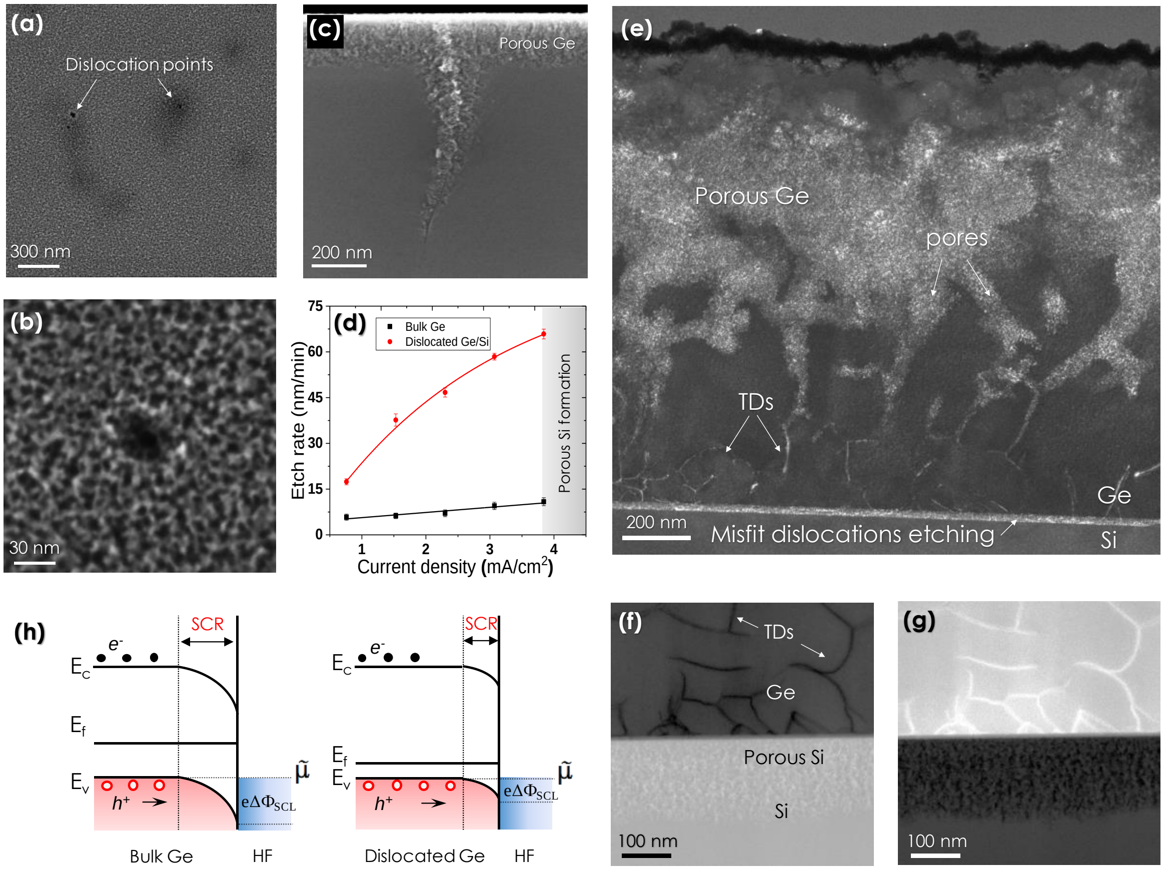


Figure VI 2: Planar-view SEM image of porous Ge/Si layer formed at 1.5 mA/cm^2 (a,b) and cross-section SEM view (c) showing preferential etching through dislocations. (d) Etching rate evolution versus the current density of bulk Ge and dislocated Ge/Si layer. Dark-field TEM image of porous Ge/Si formed using a current density of 4 mA/cm^2 during 30 min shows a thick porous Ge layer with weakly branched pores crossing threading dislocation cores up to full uprooting of misfit dislocations (e). BF- (f) and DF-STEM (g) micrographs showing the formation of porous Si obtained by HF crossing dislocations at 4 mA/cm^2 during 35 min. The energy band diagrams of p-doped Ge with HF electrolyte under a positive bias, in the case of bulk and dislocated substrates, showing the surface energy band bending in each case (h). The displacement of the Fermi level in the dislocated Ge is due to a rise of the doping concentration locally around dislocations cores. The illustration is not based on any calculations.

VI.4.2 Dislocation Annihilation Mechanisms and Crystal Quality

In order to investigate the presence of misfit and threading dislocations (MDs and TDs) throughout the NVS and study their interactions with nanovoids, detailed structural characterization was performed by STEM and TEM. High magnification STEM view in DF and BF shows clearly the overlap dislocation-voids as can be seen in Figure 3b and c. The dislocation segment glides to connect void areas until its complete annihilation. Different phenomena may come into play in the dislocation pinning mechanism, which are all promoted by high temperature achieved during annealing including; gliding [280], climbing processes [287], [315], the void size effect [283] and inertial effects [282]. For Ge/Si (001), dislocation arms are located on the (111) and the (11-1) slip systems. An initially perfect 60° edge dislocation dissociates into two separated Shockley partials, (e.g., 60° dislocations dissociate into 30° and 90° partial dislocations), in which, the energy state of the sum of the partials is less than the energy state of the original dislocation [316], [317]. The attraction and detachment process between dislocations and voids depends on the void diameter and the distance between the partials [282]. For the smaller voids, the partials strength dominates the obstacle strength. Consequently, the dislocations cut through the small voids without being trapped. For the larger voids, the obstacle strength dominates, causing the dislocation to be pinned by the voids and to bow under the internal shear stress. For large voids that are sufficiently spaced out, dislocation can bypass the obstacle via the Orowan mechanism [280]. Indeed, voids with the adequate dimensions create a stable energetic well for the dislocations, strongly pinning them in place.

For TDs annihilation, the arrow in Figure 3b indicates the location where a dislocation segment terminates on the nanovoid with no propagation beyond. A reasonable explanation for the TD termination is that two dislocations or more with opposite Burgers vectors having the same magnitude have reached the void. From Frank's rule of conservation of Burgers vectors, the net Burgers b_{net} vector resulting from this overlap must be zero [318]. Possible reactions between threading dislocations in heteroepitaxial cubic semiconductors have been presented including fusions, complete and half annihilation reactions.

As shown in Figure 3d and e, threading segments from either different dislocation sources on the same slip plane (111) (e.g., a/2[1-10] and a/2[-110]), or on the parallel slip system (e.g., a/2[01-1] and a/2[0-11]) can annihilate. In addition, by thermally activating both glide and climb of the threading segments, annihilation may be achieved from different dislocation sources on intersecting slip systems as shown in Figure 3f (e.g., a/2[101] and a/2[-10-1]) [291]. The fusion of threading segments is also an energetically favorable reaction in which two dislocations merge to form a single one generating a Y-shaped defect as highlighted by the arrow in Figure 3c and schematized in Figure 3g. For example, fusion is favorable between two TDs with Burgers vectors (e.g., a/2[10-1] and a/2[011]) leading to a single TD with Burgers vectors a/2[110] [77].

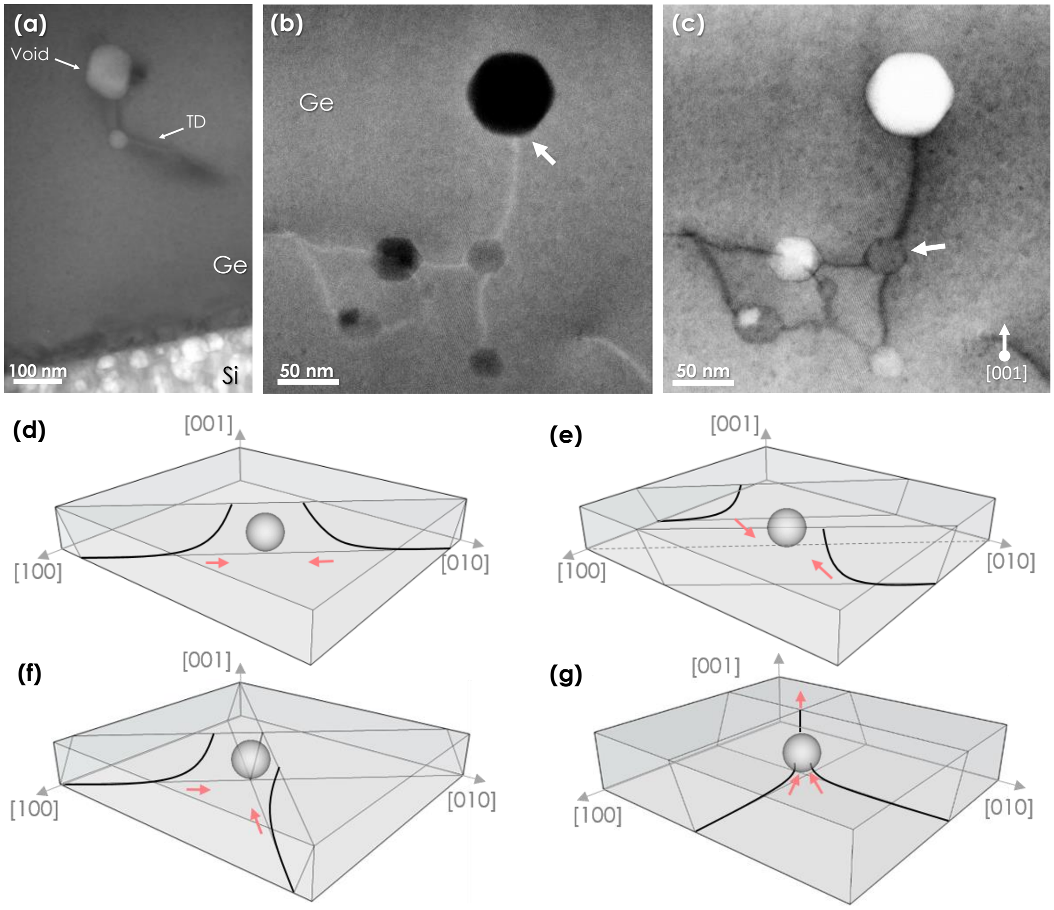


Figure VI 3: Low magnification TEM image close to the Ge/Si interface of the nanovoid based Ge/Si virtual substrate (NVS) showing the presence of the voids in the Ge layer as well as in the Si substrate (a). STEM images show different interactions between dislocations and voids in DF (b) and BF (c). The gliding dislocations in the Ge layer shows slight curvature to join the void area until its complete annihilation. Possible processes for annihilation of threading dislocations at the void surface by interaction of several threading segments from: the same slip system (d), the parallel slip system (e), by a combination of glide and slip motion (f) and by fusion (g).

These different interactions between neighbouring dislocations are characterized by the interaction radius, which corresponds to the distance at which the interaction force between dislocations becomes larger than the friction resistance of the lattice [289]. Due to the attractive force created by the population of smaller voids, the approach distance between two TDs with different Burgers reaches a low value in which the TDs begin to glide together and annihilate or fuse. These mechanisms give a reasonable explanation for the dislocations reduction by introducing nanovoids in heteroepitaxial diamond films, in which, the TDs have an interaction radius higher than the interaction radius in the conventional structure without voids, which in turn increases their recombination probability.

In order to study the effect of nanovoids formed in the Si substrate on TD reducing, low-magnification TEM micrographs from the Ge/Si reference and the NVS are presented for comparison in Figure 4a and b, respectively. A high defect density region, extending from the heterointerface towards the surface may be observed for the Ge/Si reference. A dense dislocation network confined in a region of 50 nm close to the Ge/Si interface of the NVS, and almost nonexistent defects within the Ge layer are shown. Fourier analysis from the Ge/Si interface is given in (Fig. VI 8 Supporting Information), indicates the epitaxial reconstruction of the Ge layer over the voided Si substrate with the same crystallographic orientation as the parent Si wafer. Figure 4c and d show enlarged images near to the Ge/Si interface for both substrates. For the Ge/Si reference, it is seen that the only defects in the Ge/Si heterostructure are the misfit dislocations located at the Ge/Si interface. Several misfit dislocation cores marked by white arrows at the Ge/Si interface can be identified clearly. The type of these misfit dislocations was determined to be 60° dislocation and 90° full-edge dislocation from the HRTEM images by drawing a Burgers circuit around the dislocations. For the NVS, voids are observed as clear areas. The amorphous zone appear in the void zone, probably due to the amorphisation of the void wall during the TEM sample milling. A rough interface at the atomic scale is observed. This indicates that the Ge/Si interface has undergone a strong perturbation during the electrochemical etching and annealing. To analyze the local strain distribution at the interface, we have used the geometric phase analysis (GPA) on the HRTEM images. Figure 3e and f show the ε_{xx} component of the strain field (x-axis along the [100]) derived from Figure 4c and the square from Figure 4d, respectively. At the upper region (Ge), the strains are positive and tensile, and the lattice is compressive at the lower region (Si). On these images, the dislocation cores are easily located, as they corresponding to the blue areas at the interface. To quantify the strain relaxation state, we calculate the average ε_{xx} at the upper region (Ge) for both cases. The average value of ε_{xx} in Ge/Si reference (3.9% ±0.5) is larger than the NVS (3.2% ±0.5) indicative of a better strain relaxation of the Ge layer in the NVS. These values are confirmed by calculating the distances from the 000 spot to the paired separate spots in the selected area diffraction pattern (SADP), for both paired spots of 020 and 002 as shown in Figure 4g.

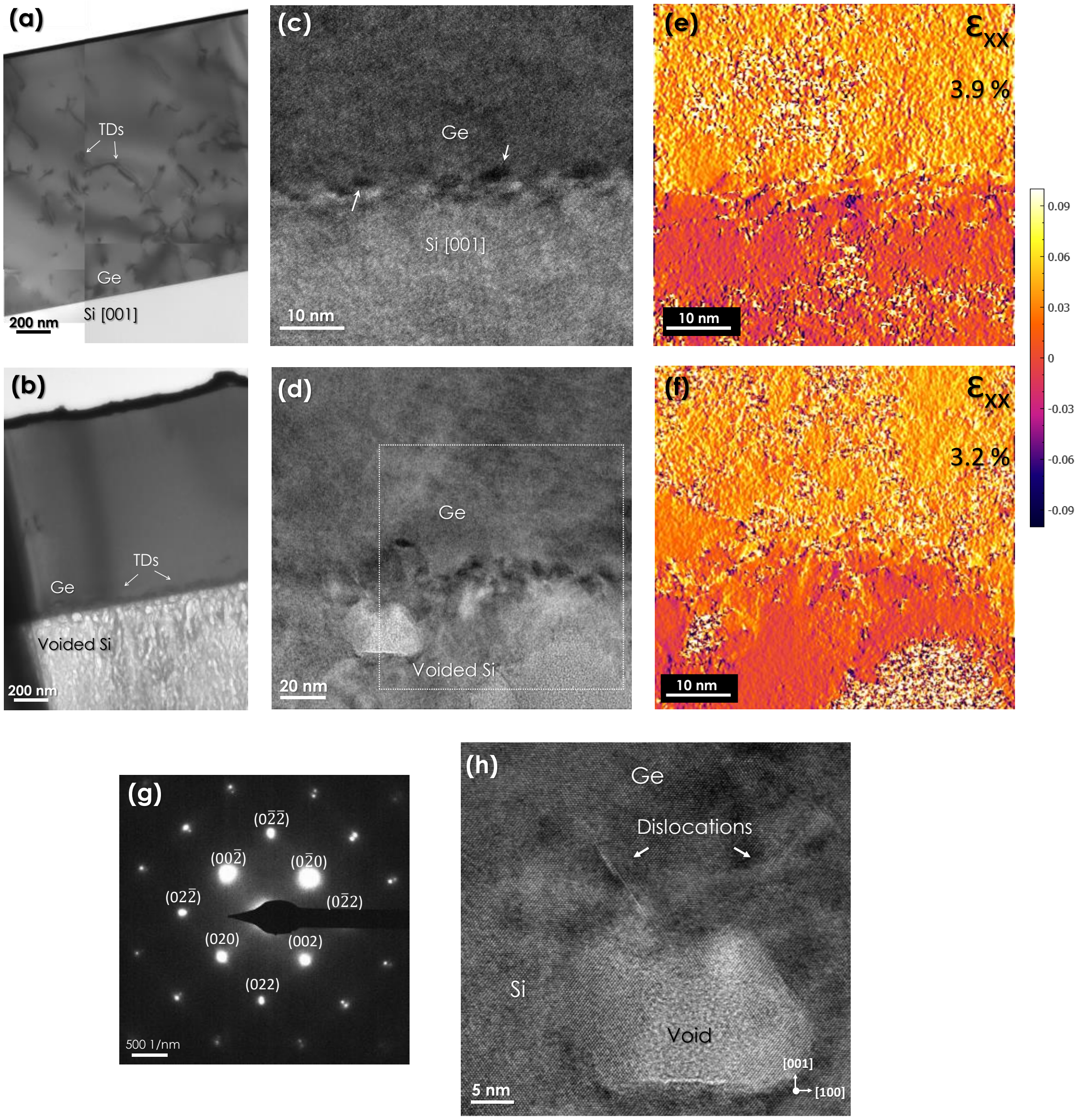


Figure VI 4: Low magnification BF-TEM images of the Ge/Si reference substrate (a) and the nanovoid based Ge/Si virtual substrate (NVS) with almost nonexistent defects within the Ge layer (b). High-resolution TEM images from the Ge/Si reference (c) and the NVS (d) show a dense dislocation network close to the Ge/Si interface. Experimental strain components ε_{xx} at the Ge/Si heterostructure interface for both substrates show a better strain relaxation of the Ge layer in the case of the NVS (e,f). SAED patterns from the NVS show a monocrystalline quality of the Ge layer (g). Atomic-resolution TEM image shows the annihilation of dislocation segments coming from the Ge/Si interface at the void located in the Si substrate: dislocations bend towards the voided area, instead of emerging at the Ge surface (h).

The lattice mismatch strain of the Ge film in Ge/Si reference remains a little high, despite the plastic relaxation, which generates misfit dislocations. However, the Ge film in the NVS is almost fully relaxed, the strain relaxation is engineered elastically thanks to the voided Si substrate. Due to its porosity, the elastic modulus of Si is reduced and the substrate can be stretched, compressed, and deformed. It is therefore expected to accommodate the mismatch of heterogeneous layers and to serve as a mechanically stretchable compliant substrate. In addition to this propriety, the nanovoids formed in the silicon substrate act as a free surface for inhibiting dislocation propagation. In fact, an enlarged image of the region near the Ge/Si interface by HRTEM, shown in Figure 4h, clearly demonstrates two dislocation loops occur from the heterointerface and annihilate at the last row of voids located in the Si substrate, instead of emerging at the Ge surface. In Si, TDs bend into the glide plane towards the voids in Si onto the glide plane in order to minimize their length, causing their elimination at the nearest free surface.

In the NVS configuration, the voids located at the Si substrate offer elastic properties to accommodate the lattice mismatch and act as a buffer layer that traps and confines TDs close to the heterointerface. While, the voids located at the Ge film favor the recombination of TDs and annihilated them far from the surface. This process was successfully used to produce wafer scale NVS on 4 in, as shown in Figure 5a.

To quantify the TDD reduction, etch-pit density (EPD) analyses were carried-out. The NVS was immersed in a solution of 2 volumetric parts 49 wt. % HF and 1 part 0.1 M $K_2Cr_2O_7$, to selectively etch the mixed and screw dislocations in the Ge layer. The Figure VI 9 (Supporting Information) shows the top view microscope images revealing a number of dark pits at the center. Figure 5b-d show SEM images of the EPD taken from the edge of the NVS with non-treated area, and from different regions of the sample. The etch pit density is clearly lower in this area compared by the non-treated area, which confirms that the dislocations were effectively blocked from propagating in the NVS. By combining different interaction between dislocations and voids, located either in the Ge layer or in the Si substrate, the averaged TD density from the pit counting is reduced significantly from ~10^7 cm^{-2} to ~10^4 cm^{-2} for 1.5 µm thick Ge layers, which is considered very low for such a thin epitaxial layer [14], [319].

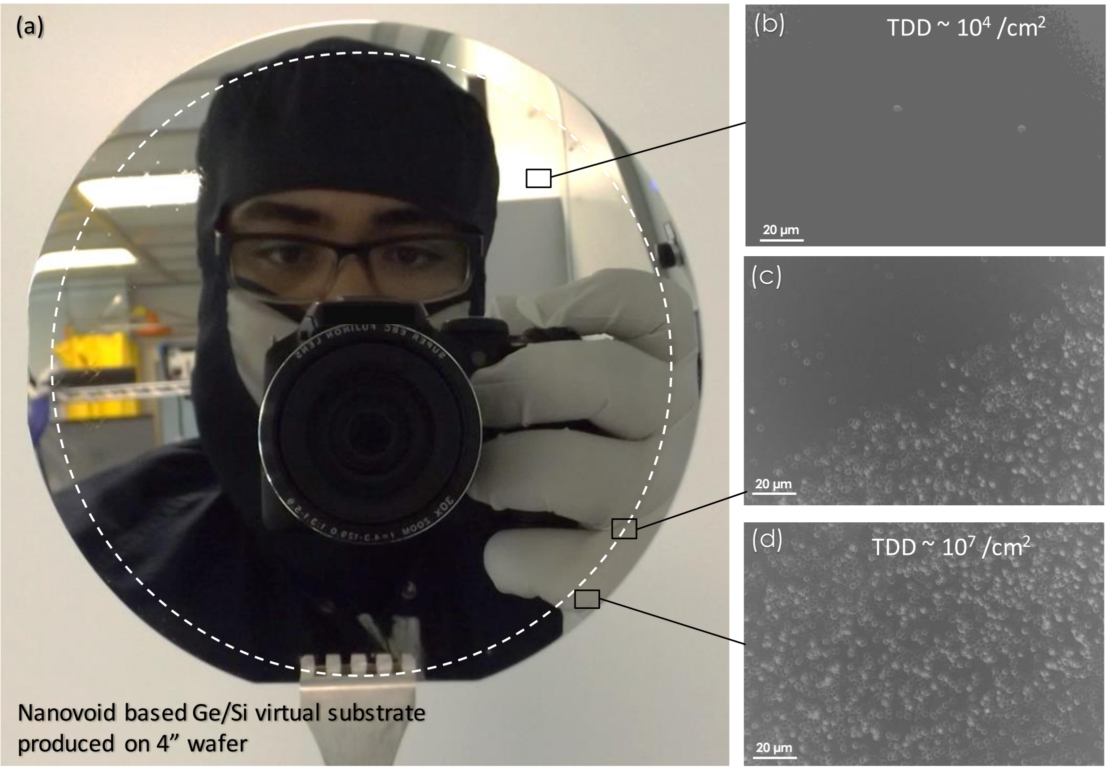


Figure VI 5: Picture of the NVS produced on a 4 in. wafer (a) and etch pit densities taken from different regions of the NVS show the TDD reducing from ~10^7 cm^{-2} to ~10^4 cm^{-2} for 1.5μm thick Ge layer by introducing nanovoids inside the Ge/Si substrate (b-d).

VI.4.3 Room Temperature Optical Emission

As the TDD is significantly reduced, one would expect that the NVS could be as an ideal starting point for the growth of high-quality III-V alloys and devices. To prove this, an epitaxial growth of 300 nm thick GaAs layers were carried-out on three substrates for comparison: bulk Ge, commercial Ge/Si with TDD ~10^7 cm^{-2} and the NVS with TDD ~10^4 cm^{-2}. Light emission efficiency and optical emission spectra from these substrates were measured by cathodoluminescence (CL).

First, the use of surface preparation before the growth always led to a noticeable reduction of the surface roughness. Calibrations of the RMS of varied Chemical-mechanical planarization (CMP) durations were carried-out on a rough Ge/Si substrate using a mixture of commercial CMP slurries, DI water dilution, and 1 wt% H_2O_2 (Fig. VI 10 Supporting Information). Using this process, the initial RMS of the NVS (2 nm for a large window size of 20x20 µm^2) was reduced to 0.5 nm, to fulfill the requirements for the epitaxy of III-V alloys. The polished thickness of the NVS is around 40 nm.

Optical emission properties of GaAs films were investigated under electron irradiation using cathodoluminescence (CL) measurements. The energy-loss and CL generation profiles simulated for a 300 nm thick epilayer of GaAs (density 5.32 g/cm^2) on Ge (density 5.32 g/cm^2), for monoenergetic beams of 5 keV, 10 keV and 20 keV are given in (Fig. VI 11 Supporting Information). These parameters were calculated using the Monte Carlo simulation CASINO [320] in order to optimize the CL emission depth profile of GaAs films and compare the recombination behaviour at the surface and in the bulk for each substrate. CASINO simulation of the electron interaction volume of a 300 nm thick GaAs film grown on Ge substrate is presented in Figure 6a and e. The color scale indicates the irradiated electron energy concentration. The thickness of GaAs used in this work has been overlaid in the diagram to facilitate comparison. Simulations show that interactions occurred at the surface could be revealed using 5 keV e-beam and across the entire layer of GaAs using 20 keV e-beam.

CL spectra from all samples show luminescence in the near infrared region with a maximum intensity at 860 nm as shown in Figure 6i-k. The peak is correlated to the interband recombination process of exited charge carriers across the direct bandgap of GaAs (1.43 eV) at room temperature [321]. At the surface (5 keV e-beam), the recombination process is less radiative for all samples due to a high density of surface states (Figure 6b-d). The CL intensity of GaAs on Ge/Si substrate is very low to compare with GaAs on Ge bulk. The correlation between CL spectra and CL micrographs shows that this attenuation is due to the electrical activity of defects, which reveals dark regions where the recombination is non-radiative. These defects are mainly the threading dislocations present in the GaAs layer, which propagate from the mismatched Ge layer on Si. For the NVS, the GaAs CL intensity was considerably improved to compare with GaAs/Ge/Si. The CL micrographs shows the disappearance of dark regions, which corresponds to a low threading dislocation density inside the GaAs layer, as shown in Figure 6h. These results confirm that the dislocations were effectively blocked from propagating, which reflect by enhancing the emission efficiency of GaAs grown upon the NVS.

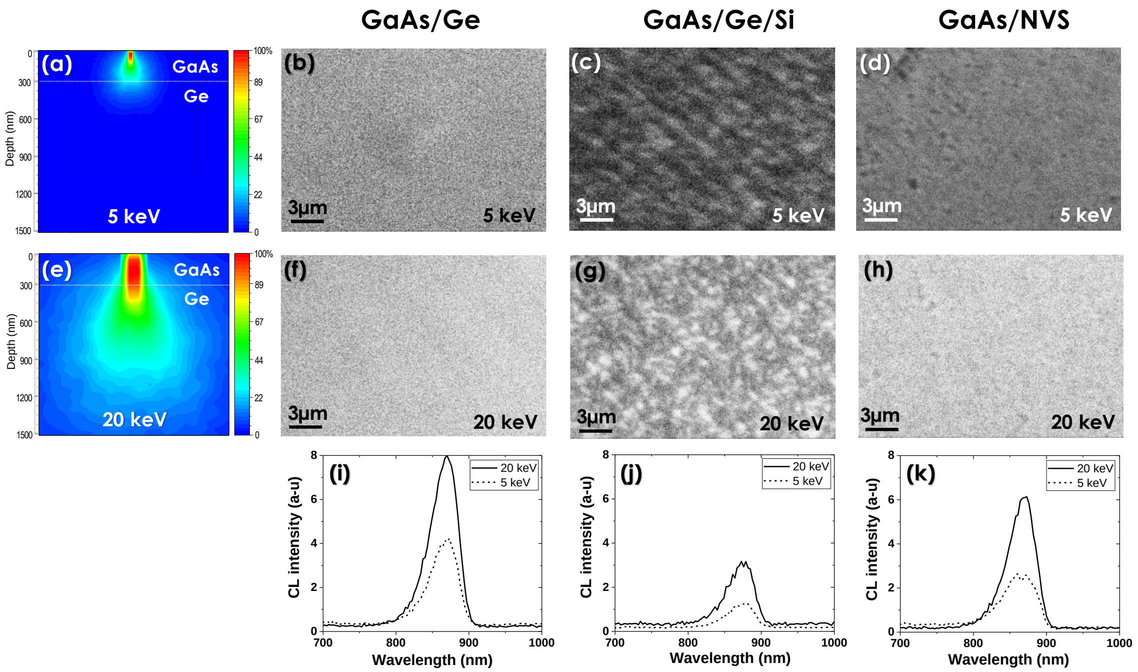


Figure VI 6: Monte-Carlo simulations CASINO of the electron interaction volume, and planar cathodoluminescence (CL) micrographs of a 300 nm thick GaAs layer grown on bulk Ge substrate, Ge/Si substrate and the NVS at 5keV (a,b,c,d) and 20keV (e,f,g,h), respectively. The CL micrographs show the emission and the recombination behaviour at the surface (5 keV) and in the bulk (20 keV) of GaAs on each substrate. Room temperature cathodoluminescence spectra recorded from (i) GaAs/Ge, (j) GaAs/Ge/Si with TDD ~10^7 cm^{-2} and (k) GaAs/NVS with TDD ~10^4 cm^{-2}, at 5 keV and 20 keV. CL measurements confirm that the dislocations were effectively blocked from propagating using nanovoids, which reflect by enhancing the emission efficiency of GaAs grown upon the NVS.

VI.5 Discussion

In summary, low TDD in mismatched Ge-on-Si substrate is produced by an innovative approach, which consists of trapping and annihilating dislocations propagation by self-assembling nanovoids barrier close to the Ge/Si interface. The nanovoids are formed in the Ge layer as well as in the Si substrate by electrochemical porosification followed by thermal annealing. The results show that porous Ge is selectively formed through threading dislocation cores with high etch rate, up to full uprooting of misfit dislocations. We have demonstrated by TEM analysis different effects of either of the free wedge surfaces on dislocation, particularly, threading-arm pinning by nanovoids. Possible mechanisms responsible for TD reduction that lead to either annihilation or fusion have been discussed. The results show clear evidence that introducing nanovoids favors recombination of dislocations by increasing their interaction radius (Figure VI 12 Supporting information). In addition, the voids formed in the silicon substrate act as a free surface for inhibiting dislocation propagation. The TDs bend backwards, towards the voids in Si in order to minimize their length, causing their elimination at the nearest free surface, leading to the creation of an almost defect free Ge layer on Si.

Cathodoluminescence measurements indicate a strong enhancement of emission efficiency in GaAs grown on this Ge/Si virtual substrate (with TDD ~10^4 cm^{-2}) to compare with a commercial Ge/Si (with TDD ~10^7 cm^{-2}) confirming that TDs were effectively blocked from propagating, thanks to the nanovoids. Using a simple, inexpensive process through electrochemical etching and thermal annealing will be crucial in cutting manufacturing costs and enabling market penetration of III–V on Si based devices.

VI.6 Methods

VI.6.1 Ge/Si porosification

A p+ type Ge layer of 1,5 µm was grown on nominal B-doped Si (001) wafers (4 inches diameter) using ultrahigh vacuum chemical vapor deposition (UHV-CVD), with initial TDD of ~10^7 cm^{-2}. Mesoporous Ge structures were fabricated by bipolar electrochemical etching (BEE) in a two-electrode electrochemical cell with a platinum wire counter electrode using an electrolyte consisting of 5:1 hydrofluoric acid (49%) and anhydrous ethanol. Anodic and cathodic currents with densities of ±4 mA/cm^2 were applied alternately with pulse durations of 1s during 35 min to fabricate porous Ge/Si sample.

VI.6.2 Thermal Annealing

Annealing of mesoporous Ge/Si structures was performed in a forming gas (N_2:H_2 90:10) ambient using a J.I.P. ELEC JetFirst rapid thermal annealing (RTA) system with a ramp rate of 25 °C/s. The duration was fixed at 10 minutes and the annealing was performed between 300-600°C to obtain the voids in the Ge layer as well as the Si substrate.

VI.6.3 Epitaxial growth

GaAs growth was carried-out in a VG Semicon VG90H CBE reactor. A 300 nm of GaAs was deposited using triethylgallium (TEGa) and cracked arsine (AsH_3) as the Group III and V sources, respectively. Prior to growth, the Ge substrates were heated at a temperature of 650 °C in the growth chamber (under vacuum) for 10 minutes in order to allow for complete oxide desorption. The growth run was carried-out at 550 °C.

VI.6.4 Structural characterization via transmission electron microscopy

The samples were observed in a scanning/ transmission electron microscope (S/TEM) in the high-angle annular dark field (HAADF) mode using a Titan Themis operated at 200 kV and equipped with a CEOS probe corrector and a Ceta 16M camera from FEI. The sample was prepared for S/TEM using focused ion beam (FIB) thinning and ion milling. 100 nm-thick carbon was deposited before FIB in order to protect the surface. Elemental distribution analysis was carried out using the Gatan Digital Micrograph (DM) and Energy Dispersive X-ray spectroscopy (EDX) combined with STEM. For EPD, the etchant was a mixture of 2 volumetric parts 49 wt. % HF and 1 part 0.1 M $K_2Cr_2O_7$. Etch pits were counted on the top surface by examining SEM images of several samples. Additional nanoscale structural information has been obtained by means of micro-Raman spectroscopy at room temperature using an excitation wavelength of 532 nm and an excitation power of 1 mW/cm^2.

VI.6.5 Cathodoluminescence

The cathodoluminescence (CL) spectra and images are acquired at room temperature, in the same SEM setup as the one used for imaging the layers. Our CL system, in association with a spectrometer, allows monochromatic CL (GATAN MonoCL2) imaging as well as acquisition of CL spectra on localized spots of a sample with a spectral resolution of 0.5 nm. The accelerating voltages used in the CL characterization are 5 and 20 KeV.

VI.7 Acknowledgements

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VI.8 Author Contributions

Y.A.B. performed the experiments, analyzed the data and wrote the manuscript. M.M. developed Ge growth, A.S. prepares TEM samples, Y.A.B and N.B. carried out GPA analyses, Characterization of HR-TEM was performed by Y.A.B and G.P., CL was measured by Y.A.B. The manuscript was revised by all authors. The project was planned, directed, and supervised by D.D. A.B and R.A. All authors discussed the results and commented on the manuscript.

VI.9 Supporting Information

VI.9.1 Nano-voids formation

Figure S1 shows different void of different shapes stabilized following heat treatment of the porous Ge layer. The atoms diffuse from the larger curvature surface toward the lower curvature surface down a gradient potential following to Rayleigh instabilities.[103], [312] Depending on annealing temperature, random pores obtained after electrochemical etching become spherical voids beginning from 350°C (Fig. 6a). The neighboring voids are then coalesced to form larger ones at 450°C, as shown in Figure 6b. Keeping activation energy, surface atoms of spherical voids form faced voids that are minimizing the surface energy by favoring the growth of low-energy facets (see Figure 6c,d). Faced voids start to dominate, from 600°C. The measured angle between the two prominent orientations is in perfect agreement with the angle value of ~54° between the lowest surface energy (100) and (111) oriented facets in crystalline Ge [322]. High magnification HAADF-STEM micrograph from the facet void is presented in Figure S1e and shows a monocrystalline quality of the Ge after annealing at 600°C.

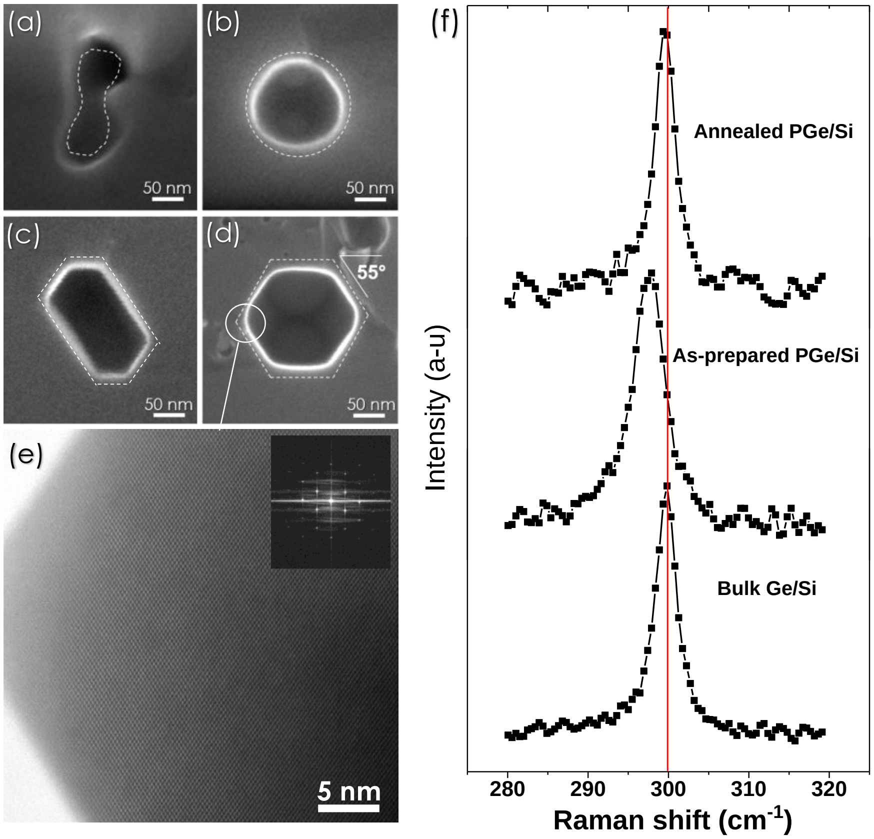

Figure VI 7: Voids of different shapes observed during the annealing of Ge/Si layer formed following to the mass transport mechanism: (a) at 350°C, the beginning of the coalescence of two nearest pores given elongated voids (b) at 450°C, spherical voids start to dominate and (c,d) from 600°C, faced voids can be observed. The heat treatment was performed in hydrogen ambient during 10 min. The measured angle is in perfect agreement with the angle value of ~54° between the (100) and (111) oriented facets. (e) High magnification HAADF-STEM micrograph from (d) showing a monocrystalline quality of the Ge after annealing at 600°C. (f) Evolution of Raman spectra at the porosification and annealing steps. The Raman spectra of bulk Ge/Si is also presented for comparison.

Structural analysis by µ-Raman of as-prepared porous- and annealed Ge/Si is presented in (Figure 6f). The spectral position, the width and the shape of the Raman peak of as-prepared PGe/Si are quite different from the well-known Ge bulk position at 300 cm^{-1}. These changes are attributed to the quantum confinement of phonons at low crystal size confirming the nanostructuration of the Ge layer [323]. However, the peak from the annealed PGe/Si shows the disappearance of the asymmetric form, a decrease of the width and a coincidence with the spectrum of bulk Ge, indicting the restoring of the bulk order in the voided Ge/Si substrate.

VI.9.2 FFT analyses of the NVS interface

Figure 7a-c shows EDX mapping of the NVS revealing an unclear, unsharp, Ge/Si interface. This is probably due to a mixed reorganization of the porous Si and Ge atoms at the interface during thermal annealing.

Figure 7d shows an enlarged image of the region near the Ge/Si interface by HRTEM. Voids are observed as clear areas. A fast Fourier transform (FFT) image of Fig. 7d is given from different zones, which reveals clearly the monocrystalline quality of the Ge layer with the same crystallographic orientation as the parent Si wafer. The amorphous zone appear in the void zone, probably due to the amorphisation of the void wall during the TEM sample milling. A rough interface at the atomic scale is observed. This indicates that the Ge/Si interface has undergone a strong perturbation during the electrochemical etching and annealing. The diffraction spots from the interface are divided into paired separate spots that are indicated by two white lines, which correspond with those of Si and Ge crystals. From the distances between spots and the 000 spot, the difference in lattice constant is estimated to be about 4%, indicating that the lattice mismatch strain of the Ge films was almost relaxed.

Figure 7e shows an inverse FFT image (IFFT) obtained through the 11-1 spots in Fig. 7d. Lines in the numerical Moiré images correspond with lattice planes. From the interface, the edge component *b* of the 60° dislocation in the Si is inclined at ~54° to the interface, and only one extra half-plane exists, marked by an arrow. The period lines in Fig. 7f are 0.33 nm and 0.32 nm, correspond to the Ge and Si {111} interplanar spacing, respectively.

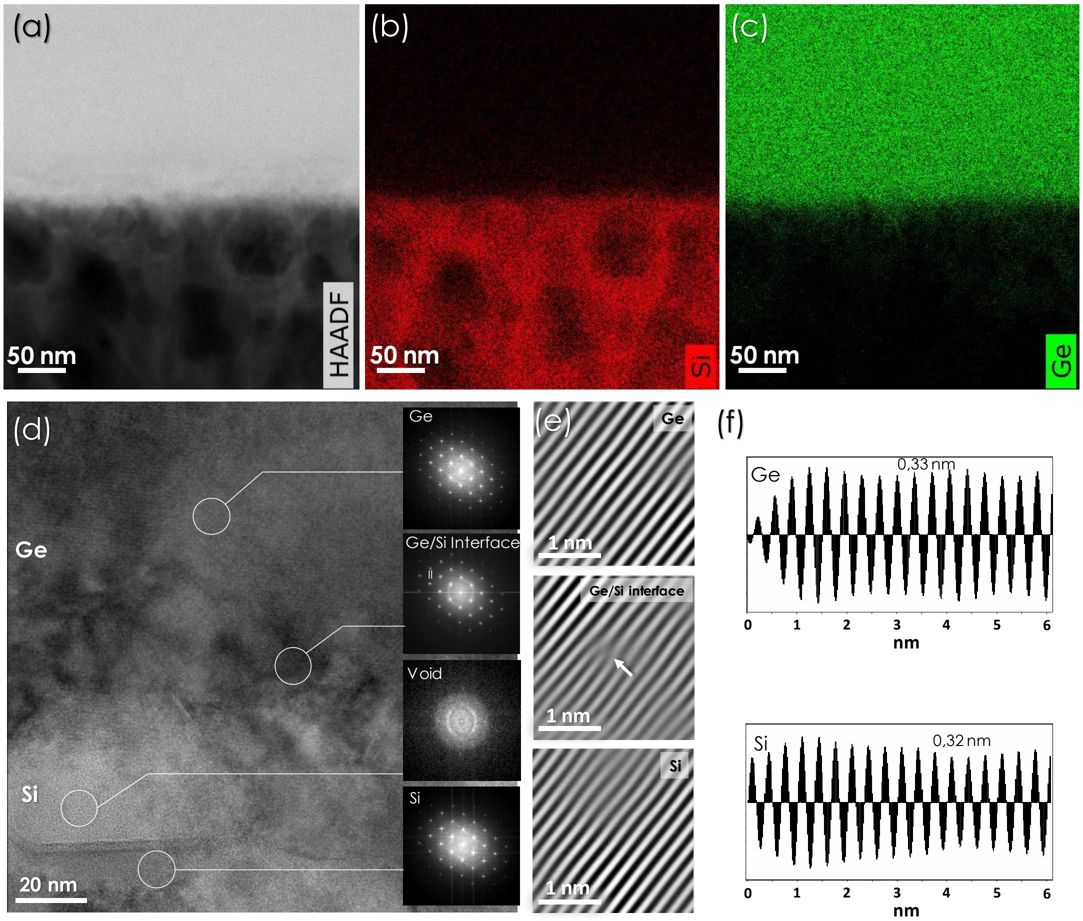

Figure VI 8: EDX mapping of the nanovoid based Si virtual substrate. (a) Cross section STEM image and the EDX element maps for (b) Si and (c) Ge elements. (d) High-resolution TEM image from the interface of the Ge/Si layer and FFT patterns (inset) of the marked Ge/Si heterostructure. (e,f) Numerical moiré of (11-1) plane from the Ge layer, and the Si substrate and their intensity profiles illustrating the Ge {111} and the Si {111} inter-planar spacing of ~3.3 Å and ~3.2 Å, respectively.

VI.9.3 Determination of TDD by etch-pit-density (EPD)

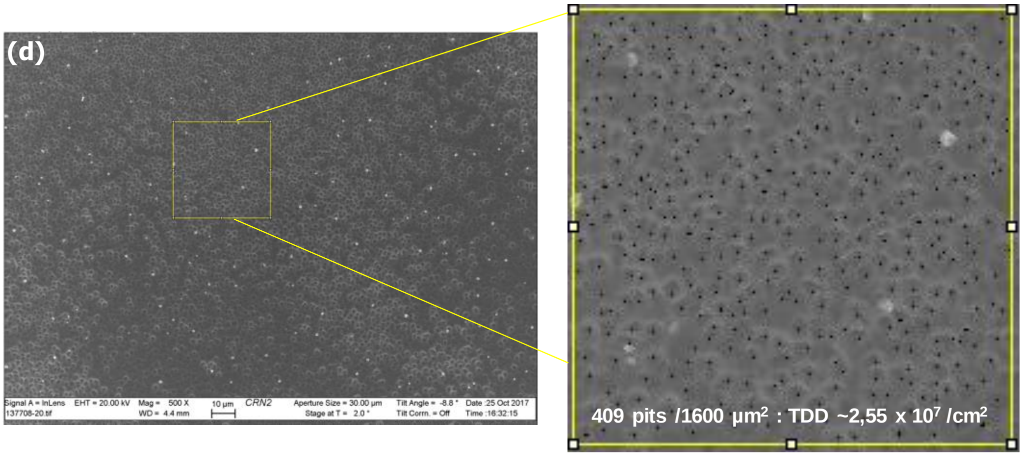

Figure VI 9: SEM images of different shapes of etch pits (e,b,c) and the computation of etch pit density using ImageJ software (d).

VI.9.4 Optimization of the chemical mechanical polishing (CMP) process

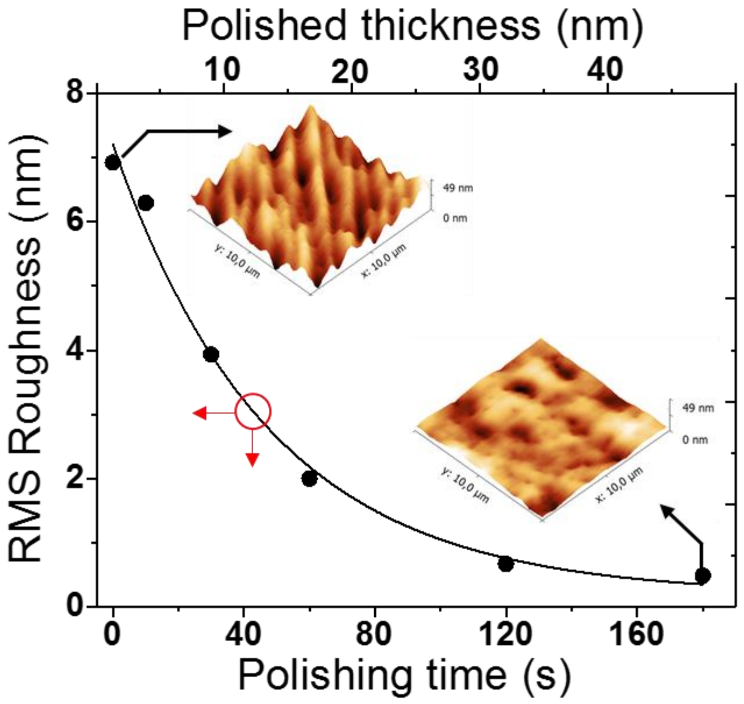

Figure VI 10: RMS surface roughness and polished thickness of Ge/Si dependence of CMP-polishing time, using a mixture of commercial CMP slurries, DI water dilution, and 1 wt% H_2O_2.

VI.9.5 Monte Carlo simulation of cathodoluminescence (CL) generated from GaAs/Ge

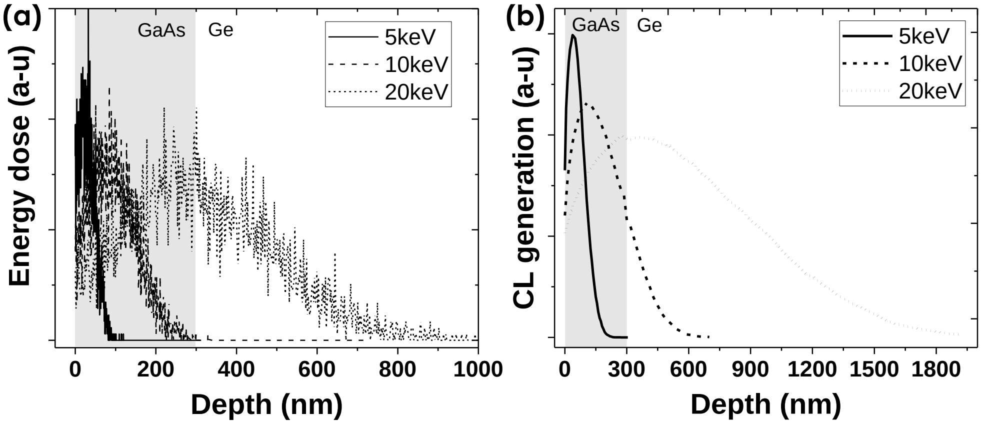

Figure VI 11: (a) Simulated total energy-dose profiles for a 300 nm GaAs epilayer grown on a Ge substrate calculated using the Monte Carlo simulation CASINO and (b) Simulated generation profiles for the measured near-edge CL signal for 5 keV, 10 keV and 20 keV beam energies.

VI.9.6 A model for reduction of threading dislocation density in Ge epilayer grown on Si substrate by introducing nanovoids

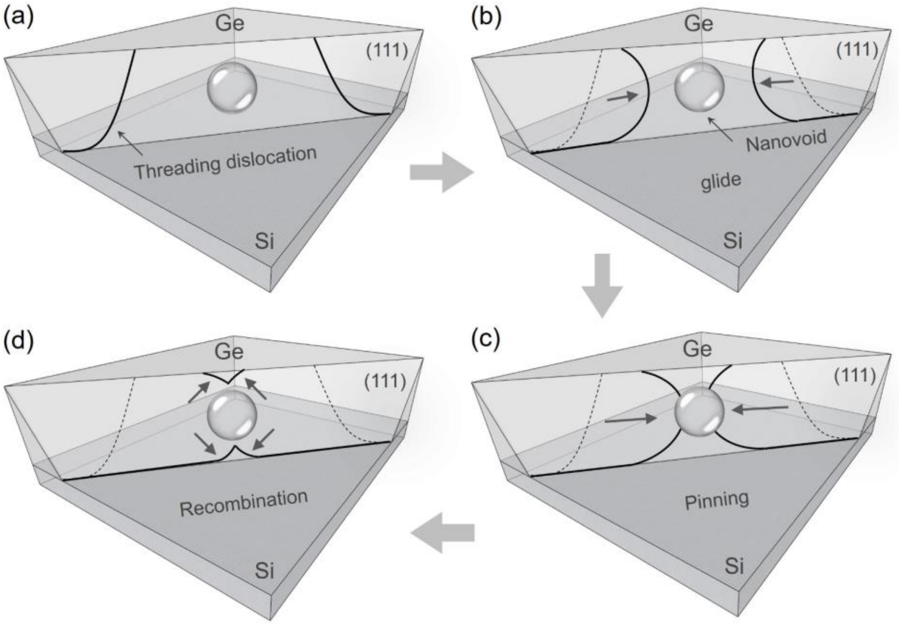

Figure VI 12: A model for reduction of threading dislocation density in Ge epilayer grown on Si substrate by introducing nanovoids. The dislocations with opposite Burgers vectors move easily on the {111} glide planes by the thermal stress during the high temperature annealing (a-b) and react with each other (c). Thus, the threading components disappear (d). By introducing nanovoids, the TDs have an interaction radius higher than the interaction radius in the conventional structure without voids, which in turn increases their recombination probability.

CHAPITRE VII CONCLUSION

Il est communément admis que l'électricité d'origine photovoltaïque constituera une des composantes majeures en apport énergétique, notamment domestique, et ce, dès les prochaines décennies. Les cellules solaires fabriquées à partir de silicium sont certes bas coût mais présentent des rendements énergétiques relativement bas. A contrario, les cellules solaires à base de semiconducteurs III-V présentent des records de rendements toujours plus élevés. Malgré l’engouement certain du grand public pour cette nouvelle technologie de pointe, cette dernière tarde à se démocratiser à cause du coût toujours trop prohibitif. En effet, le substrat de germanium s’élève à lui-seul, à plus de 50 % du prix de la cellule au complet alors que moins de 1% de ce substrat constitue la zone active du composant où le courant est généré. Une alternative serait donc d’intégrer une couche épitaxiale de Ge sur un support mécanique ou un substrat semi-conducteur à faible coût comme le silicium. Cependant, l’épitaxie de Ge sur substrat de Si présente des contraintes physiques et technologiques. Le fort désaccord en paramètre de maille engendre des dislocations et autres défauts structuraux lesquels dégradant le rendement des composants opto-électroniques et nuisent au bon fonctionnement des dispositifs élaborés à partir de ces couches.

Cette thèse passe en revue les différentes approches possibles pour pallier à ces obstacles, aussi bien celles qui ne sont pas compatibles avec les procédés standard de la microfabrication, que celles qui sont trop complexes et/ou trop couteuses.

L’approche proposée dans ces travaux consiste à empêcher la propagation des dislocations traversantes au moyen de cavités nanométriques, obtenues par un procédé de porosification thermo-électrochimique, et réalisées sur une couche hétéroépitaxiée en fort désaccord de maille avec le substrat. Ce procédé se termine par l’obtention d’une couche exempte de défauts structuraux sur laquelle est épitaxiée la cellule solaire. Ce socle à couches traitées sur substrat de silicium est communément appelé substrat virtuel. Ce dernier doit donc présenter des caractéristiques spécifiques : monocristallin en surface, epi-ready et réalisés sur substrat de grande taille (jusqu’à 100 mm dans le cadre de cette thèse) par un procédé faible coût pour une pré-industrialisation.

La réalisation de cellules solaires à base de matériaux III-V nécessite une couche de p-GaAs sur substrat de silicium. Cependant, la nanostructuration par anodisation électrochimique des semi-conducteurs binaires (p-GaAs) pour former les nano-cavités s'avère plus complexe et très limité à cause des conditions de nanostructuration non-stœchiométriques (Annexe 1).

L’alternative s’est orientée vers l’hétérostructure Ge sur substrat de Si pour laquelle le Germanium, semi-conducteur monoatomique du groupe 4, constitue un système modèle présentant de nombreux avantages:

- Stœchiométrie préservée durant le processus de porosification.
- Pseudo-substrat pour la croissance de cellules solaires III-V sur Si.
- Système modèle pour démontrer le concept de substrat virtuel.

L’approche suivie est d’optimiser les conditions expérimentales pour former des nano-cavités dans un substrat massif de Germanium avant de l’appliquer sur une hétérostructure Ge/Si.

Cependant, le verrou technologique important de la porosification électrochimique de Ge est la formation de couches épaisses de couches méso-poreuses ayant une morphologie ajustable et contrôlable. Dans le cadre de cette thèse, nous avons proposé une nouvelle technique de gravure électrochimique bipolaire rapide qui lève ce verrou. Cette technique consiste à alterner périodiquement la polarisation de l’électrode de travail, en introduisant une étape d’initiation anodique et en ajustant la fréquence de polarisation afin d’éviter l’électro-polissage et la destruction des pores formées par une gravure latérale. Il a été démontré que la morphologie, la vitesse de gravure et la porosité du Ge poreux dépend principalement des paramètres de porosifiation électrochimique tel que, la densité de courant et le degré de passivation de la surface.

Sur la base de ces résultats expérimentaux, un modèle de gravure électrochimique raffiné a été élaboré. Les caractérisations chimiques et électrochimiques confirment que la surface des pores est soit hydrogénée ou hydroxylée dépendamment du courant appliqué grâces à des réactions réversibles. L’hydrogénation de la surface sous l’injection de la charge négative permet une passivation des parois des pores et favorise une porosification en profondeur. Ce nouveau régime que l’on a nommé *Fast Bipolar Electrochemical Etching* a donc permis d’atteindre des vitesses de gravure très élevées (300 nm/min) avec une homogénéité autant surfacique que latérale sur de grandes tailles.

Subséquemment, nous avons analysé la reconstruction du volume et de la surface du Ge poreux induite par un traitement thermique. L’influence des paramètres de ce procédé de recuit (température et temps de recuit) sur la formation des nano-cavités, sur la structure cristalline et sur les propriétés électriques des couches recuites ont été étudiées.

Une fois l’ensemble des paramètres de porosification et de reconstruction du Ge poreux optimisés, le procédé a été ré-optimisé puis transféré sur des couches hétéroepitaxiées de Ge/Si.

Dans ce cas, deux architectures de substrats virtuels ont été proposées et développées pour répondre au cahier des charges:

- La première voie consiste à ne former de nano-cavités exclusivement que dans la couche de Ge. Cela est obtenu avec la formation de nanostructures poreuses de Ge/Si par gravure électrochimique sélective aux dislocations suivie d'une reprise épitaxiale de germanium monocristallin à haute température. Ces nano-cavités, présentes uniquement dans la couche de Ge, offrent des surfaces libres pour la terminaison et le piégeage des dislocations. Cette architecture a permis de réduire le taux de dislocations de plus de trois ordres de grandeur, de ~ 10^7 cm^{-2} à ~ 10^4 cm^{-2} sur des couches de Ge de 2 µm d’épaisseur produites sur des gaufres de 4 pouces.
- La seconde voie consiste à former des nano-cavités à l’interface de Ge/Si. Il s’agit de graver préférentiellement les dislocations traversantes par l'enfilage des noyaux de dislocations avec un taux de gravure élevé, jusqu'au déracinement complet des *misfit* dislocations. Une porosification anisotrope s’établie rapidement à l’interface Ge/Si côté silicium. Suite à un recuit spécifique, le Si poreux se transforme en nanocavités alors que la couche de Ge se cristallise et se referme à la surface. En conséquence, une couche de Ge continue est formée, dans laquelle une grande partie des dislocations traversantes présentent à l’origine, sont éliminées. La densité de ces dislocations traversantes est réduite en moyenne de plus de trois ordres de grandeur, de ~ 10^7 cm^{-2} à ~ 10^4 cm^{-2} pour des couches de Ge de 1,5 µm d'épaisseur.

Les analyses S/TEM sur ces substrats virtuels ont révélé différents types d'interactions dislocations-nano-cavités comme le pincement des segments de dislocations. Les mécanismes responsables de la réduction des dislocations traversantes par annihilation ou par fusion de dislocations sont exposés. Les résultats montrent clairement que l'introduction des nano-cavités dans le Ge favorise la recombinaison des dislocations en augmentant leur rayon d'interaction. Tandis que les cavités formées à l'interface Ge/Si agissent comme une surface libre qui attire les dislocations. Dans ce cas, ces TD se courbent vers les nano-cavités côté Silicium de manière à se stabiliser à moindre énergie. Les premiers tests sur ces structures montrent une luminescence bien supérieure des couches de GaAs élaborées sur ces substrats virtuels par rapport à celles élaborées sur des substrats Ge/Si commerciaux.

L'utilisation d'un de ces procédés simples et peu coûteux, par gravure électrochimique et recuit thermique adéquat, s'est révélée très efficace et innovant permettant de réduire significativement les défauts structuraux (Figure 1) et le coût d'une cellule photovoltaïque à base de III-V sur substrat silicium, permettant leur intégration probable dans le marché grand public.

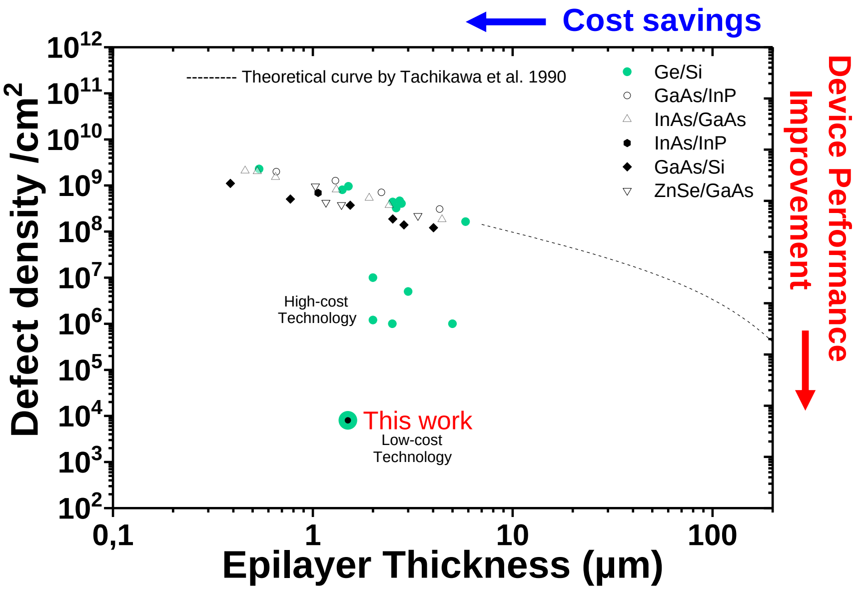

Figure VII 1: Threading dislocation vs. epitaxial layer thickness, for several mismatched heteroepitaxial material systems. The data from J. E. Ayers et al. "Heteroepitaxy of Semiconductors: Theory, Growth, and Characterization" pp 272.

L’ensemble des résultats obtenus dans le cadre de ce travail, laisse envisager de nombreux champs d’exploration dont les actions à mener pourraient être :

- Étudier les propriétés électriques et thermique (résistivité, mobilité, durée de vie des porteurs, conductivité et résistance thermique) des substrats virtuels à nano-cavités.
- Étudier la stabilité thermique de ces substrats virtuels à nano-cavités, notamment à haute température.
- Réaliser la croissance d’une cellule solaire à base de matériau III-V par épitaxie sur les substrats virtuels à nano-cavités afin de comparer les performances des cellules solaires ainsi élaborés avec des cellules réalisées sur substrats de Ge massif, Ge/Si et Si.
- Réaliser une étude de faisabilité technico-économique du procédé proposé dans un cadre industriel.

ANNEXE I
ANODISATION ÉLECTROCHIMIQUE DE P-GAAS ET NATURE CHIMIQUE

I.1 Avant-propos

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Revue : Nanoscale Research Letters

Référence : [53]

Titre français : Composition chimique d'une couche nanoporeuse de p-GaAs formée par gravure électrochimique

Contribution au document : Cet article contribue à la thèse en explorant le potentiel de la réalisation des substrats virtuels à partir de matériaux semi-conducteurs binaires utilisant l'anodisation électrochimique, ainsi qu'en démontrant la composition chimique de la couche poreuse obtenue.

Résumé français :

Une étude de caractérisation détaillée sur la gravure électrochimique de GaAs de type p dans un électrolyte à base d'acide fluorhydrique a été effectuée. Les échantillons ont été étudiés et caractérisés par cathodoluminescence (CL), diffraction des rayons X (XRD), spectroscopie à rayons X à dispersion d'énergie (EDX) et spectroscopie de photoélectrons à rayons X (XPS). Il a été démontré qu'après gravure électrochimique, la couche poreuse présentait une diminution importante de l'intensité de CL et une modification de la composition chimique et de la phase cristalline. Contrairement aux rapports précédents sur la porosification de p-GaAs, qui indiquaient que la couche formée est composée de GaAs poreux, nous rapportons la preuve que la couche poreuse est constituée principalement d'As_2O_3 poreux. Finalement, un modèle qualitatif pour expliquer la formation de la couche d'As_2O_3 poreuse sur le substrat de p-GaAs a été proposé.

Chemical composition of nanoporous layer formed by electrochemical etching of p-type GaAs

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Keywords: GaAs nanostructures - Porous GaAs - Electrochemical etching - Cathodoluminescence.

I.2 Abstract

We have performed a detailed characterization study of electrochemically etched p-type GaAs in a hydrofluoric acid-based electrolyte. The samples were investigated and characterized through cathodoluminescence (CL), X-ray diffraction (XRD), energy-dispersive X-ray spectroscopy (EDX), and X-ray photoelectron spectroscopy (XPS). It was found that after electrochemical etching, the porous layer showed a major decrease in the CL intensity and a change in chemical composition and in the crystalline phase. Contrary to previous reports on p-GaAs porosification, which stated that the formed layer is composed of porous GaAs, we report evidence that the porous layer is in fact mainly constituted of porous As_2O_3. Finally, a qualitative model is proposed to explain the porous As_2O_3 layer formation on p-GaAs substrate.

I.3 Introduction

GaAs nanostructures are becoming more widespread in many applications including optoelectronic devices [324], solar cells [325], light emitting diodes (LEDs) [326], tunnel field-effect transistors (TFETs) [327], thermoelectric devices [328] and biosensing [329]. *Top-down* and *bottom-up* methods are two approaches used to produce GaAs nanostructures by a variety of physical [7] and [8], chemical [332] and electrochemical etching techniques [333]. GaAs nanostructures can be obtained in different forms and shapes including quantum wells [334] nanowires [335], quantum dots (QDs) [336], quantum dot molecules [337], quantum rings (QRs) [338], nanodiscs [339], coupled ring/disks [340], nanopillars [341], nanoholes [342] and nanopores [343]. Electrochemically formed porous GaAs nanostructures are particularly attractive for many applications due to their unique nanoscale properties and high surface to volume ratio. Furthermore the applications of porous GaAs are very broad ranging from antireflective coating for GaAs solar cells [344], virtual substrate for InGaAs due to its weak elastic properties [345], temporary carrier to reduce the weight of the solar cell by layer transfer processes [23] and [24] . It was even shown that porous GaAs are good candidates to obtain fast response to humidity sensing [92]. So far, the porous morphologies obtained from the electrochemical etching of p-doped GaAs are quite different from that of the n-doped type. For n-GaAs, the material pore density, pore dimension and layer structure depend on the doping density and the crystallographic orientation of the wafer. High aspect ratio triangular pore arrays along the (111) crystallographic direction have been observed by several groups in n-GaAs [26] and [27]. However, for p-GaAs, uniformly distributed mesopores are obtained. The argument is that holes are the majority carriers in p-type substrates and are certainly omnipresent, which will lead to a uniform dissolution even without backside illumination [153]. It is generally believed in the literature that electrochemical etching of p-GaAs leads to porous GaAs formation as it produces nanometric crystallites [349]. However, until now, no detailed analysis of the chemical composition of such layers has been reported. In this work, we report such an analysis by using various characterization techniques to reveal the chemical nature of the porous p-GaAs layer. The spatial and spectral distribution of cathodoluminescence (CL) in bulk and porous samples is presented. Energy-dispersive X-ray spectroscopy (EDS) and X-ray photoelectron spectroscopy (XPS) analysis were performed to confirm the chemical composition. Finally; X-ray diffraction (XRD) was used to determine crystallographic properties of the porous layer.

I.4 Methods

Porous GaAs layers are formed by electrochemical etching on highly doped p-type wafers (Zn-doped, resistivity = 2.10^{-3} ohm.cm) with (001) crystal orientation supplied by AXT. After immersing the GaAs wafer in an electrolyte consisting of a 49% HF/water solution, the etching process is activated via direct current. The characteristics of the surfaces are extracted from SEM images using a Zeiss scanning electron microscope, operated from 1 to 20 kV and equipped with a field emission gun. Cross-section images are obtained by cleaving the samples. The bulk porosity is determined through gravimetric measurements, where the sample is weighed by a high precision scale (± 0.1 mg) before (m_1) and after (m_2) the etching process. Afterwards, the wafers are introduced for 10 s in H_2O:H_2O_2:H_3PO_4 (140:2.5:1) in order to selectively remove the porous layer. The remaining mass of the substrate is obtained by weighing the sample again (m_3). The porosity (P) is given by: $P\% = (m_1-m_2)/(m_1-m_3)$. The cathodoluminescence (CL) spectra and images are acquired at room temperature, in the same SEM setup as the one used for imaging the layers. Our CL system, in association with a spectrometer, allows monochromatic CL (GATAN MonoCL2) imaging as well as acquisition of CL spectra on localized spots of a sample with a spectral resolution of 0.5 nm. The accelerating voltage used in the CL characterization is 20KeV. Surface chemistry is analyzed by XPS Kratos Axis Ultra DLD with monochromatic Al Kα (1486.7 eV) X-ray source and an oval beam size of 300 x 700 microns in diameter. The electron take-off angle is fixed at 60° and the vacuum pressure is below 10^{-9} Torr during spectra data acquisition. Survey XPS data are acquired over 1200 eV with pass energy of 160 eV and a resolution of 1 eV. High resolution XPS spectra are obtained at Ga 3d, As 3d, O 1s, F 1s, and C 1s with a pass energy of 20 eV. Binding energies, peak areas and atom concentration ratios are obtained using CasaXPS. The chemical composition of the exposed surface is verified also by energy-dispersive X-ray (EDX) spectroscopy. Powder X-ray diffractograms have been measured with a Philips X'Pert diffractometer. Samples are prepared simply by crushing porous layer and measured on a standard single-crystal.

I.5 Results and discussion

I.5.1 Electrochemical calibration and morphology

Calibrations of the porous layer parameters such as porosity and etching rate have been done by varying the current density in the electrochemical process, all other conditions being the same. Fig (1.a.b) illustrates the dependence of the porosity and the etching rate on the current density. Similarly to porous Si and Ge [180], [350], the etching rate increases linearly with increasing current density. The porosity initially increases rapidly, until it gradually saturates at around 80%. During the drying process, cracks appear over the entire surface of the sample. The origin of the cracks can be attributed to the high mechanical stresses generated when the water is evaporated [26] and [27].

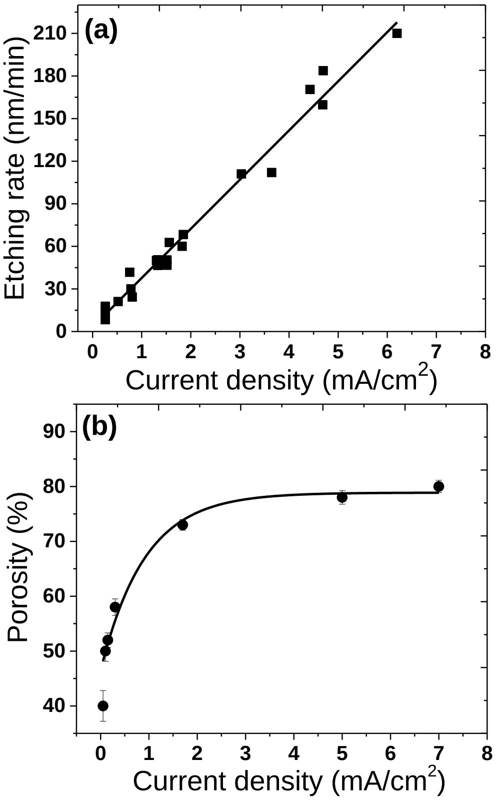

Figure ANX 1: Etching rate (a) and porosity evolution (b) versus the current density of anodically etched p-GaAs in a 49%HF solution.

The SEM image of GaAs after porosification is shown in Fig (2); we can see the presence of micro-crystallites, with sharp edges, dispersed on the surface of the porous layer and having sizes of several hundred nanometers that are attributed to As_2O_3 precipitates as it was already observed by Smeenk et al. [353]. The resulting clusters show the pyramidal and prismatic morphology with a preferential orientation along the (111) plane corresponding to tiny octahedra As_2O_3 crystals [354] and [355]. High resolution SEM image of the porous surface shows a randomly and uniformly distributed mesopores structure. The nanocrystallite size is estimated to be in the range of 10-20 nm.

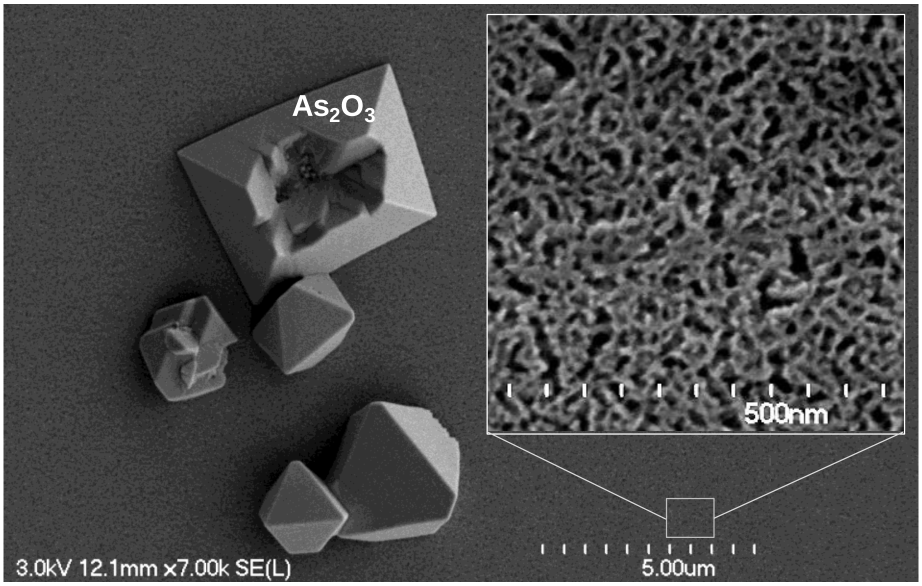

Figure ANX 2: (a) Planar-view SEM image of anodically etched p-GaAs layer formed in 49%HF solution at 2mA/cm^2. The Inset shows high-resolution SEM image on the porous surface.

I.5.2 Luminescence of porous layer

Because of the small crystallite size (in the range of 10-20 nm) that compose the porous layer, it is expected that such layer should emit radiation above the GaAs bandgap due to the quantum confinement effect [356]. In order to investigate this effect, we performed cathodoluminescence microanalysis of a GaAs sample before and after the porosification process. CL spectra from the reference sample shows luminescence in the near infrared region with a maximum intensity at 860nm as shown in Fig (3). The peak is correlated to the inter band recombination process of excited charge carriers across the direct bandgap of p-GaAs (1.43 eV) at room temperature [321]. After the porosification process, the CL intensity was considerably attenuated and no detectable shift in the peak was observed despite the low crystallite size of the porous material. This indicates that no quantum confinement effect is created within the crystallites. Which is in contrast with the results obtained by Lockwood et. al who observed luminescence in the infrared (~840 nm) and green (~540 nm) PL peak wavelengths after anodic treatment in HCl solution that are consistent with an assignment to quantum confinement effects in GaAs nanocrystallites. The previous observations suggest that the size distribution of the pores correlated qualitatively with the intensities and the positions of the PL peaks, whereas variations in the chemical composition at the surface show no systematic correlation [357] and [358].

The drastic decrease in the GaAs peak intensity could be due to different reasons, such as: i) The quenching of the CL due to surface state. ii) Fractional amorphization of material during anodization iii) Change in chemical composition. The later assumption will be verified in the following paragraphs. However, less attention has been paid to the investigation of the direct correlation between luminescence properties and morphology features of the porous GaAs layer. The morphology and CL characteristics of porous layers reported on the spatial mapping of the intensity (Fig (4)) reveals luminescence only around the location of cracks formed during the porosification process. The cross-sectional CL maps also show no luminescence coming from the porous layer. These results suggest that the CL signal is coming from the underlying bulk GaAs material, which is exposed directly in the cracked areas or by the penetration of some electrons through porous layer at high accelerating voltage (20KeV). The porous layer does not seem to generate detectable luminescence.

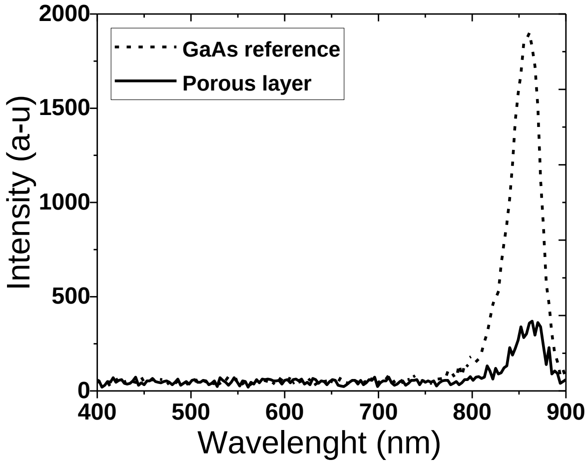

Figure ANX 3: Cathodoluminescence spectra at room temperature for the p-GaAs reference substrate and the porous p-GaAs with 20keV at room temperature formed in 49% HF solution at 2mA/cm^2.

I.5.3 Chemical compositions

The absence of size-related luminescence could be due to non-radiative recombinations, or to a drastic change in the chemical nature of porous material during anodization. We have investigated this question by verifying that the porous material stoichiometry remained similar to that of GaAs after porosification. Fig (5) shows EDX spectra of the GaAs bulk reference sample and the porous GaAs sample. We notice that the ratio between the Ga and As related emissions is changed for the porous layer. It seems that the porous material is enriched with As relative to the reference sample and there is an oxygen-related signal that appears as well. A similar EDX study shows a high decrease of Ga peak on crystalline particles during the anodic dissolution of GaAs in HF solution [359] and [360]. An oxygen peak is also present in the porous spectrum indicating a high concentration of oxygen in the film. The EDX mapping of the top of the porous sample confirms the presence of clusters with only As and O contents as shown in Fig (6). Since the EDX spectrum integrates signals coming from the whole field of view, it is unclear if the oxygen is present in the porous material, or only in the clusters on the surface.

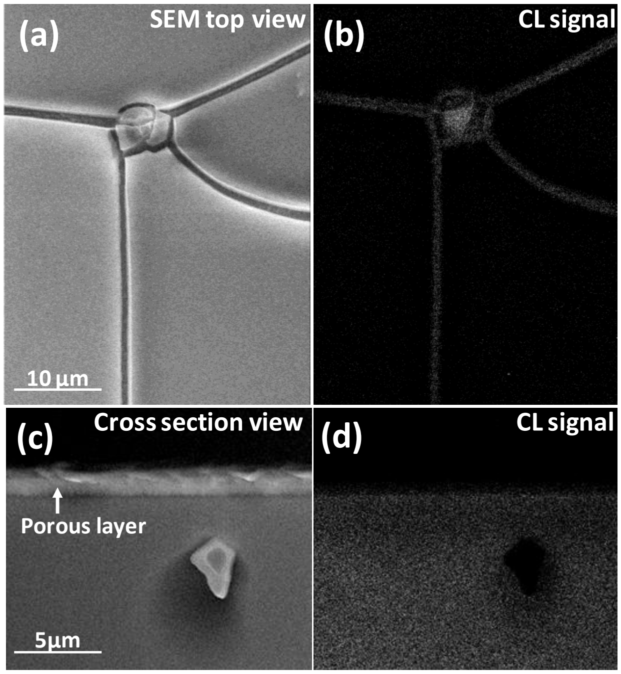

Figure ANX 4: SEM and CL micrographs taken from the top surface (a,b) and cross section (c,d) of porous p-GaAs with 20keV at room temperature formed in 49% HF solution at $2mA/cm^2$.

In order to determine the quantitative composition of the porous GaAs layer, we have performed XPS measurements before and after anodization. High resolution spectra from the As 3d and Ga 3d regions are shown in Fig (7). A small amount of Ga_2O_3 and As_2O_3 is detected on the surface of the reference sample (Fig 7.a and 7.b) due to air exposure [353]. The Ga and As signals appear in the reference sample, and are coming from both the base GaAs material as well as the oxides (Ga_2O_3 and As_2O_3). The XPS analysis of the porous material (Fig 7.c and 7.d) clearly shows that it consists only of As and arsenic oxide elements.

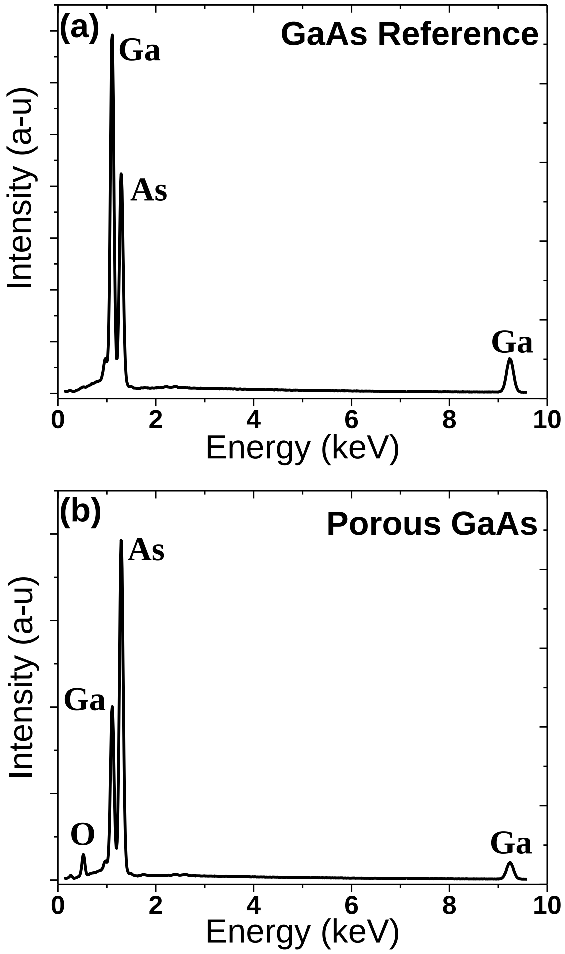

Figure ANX 5: EDX spectra of p-GaAs sample (a) and porous p-GaAs layer formed in 49%HF solution at $2mA/cm^2$ (b).

The Ga signal has completely disappeared. However, the Ga presence in EDX spectra is due to the sensitivity of this technique that offers to probe the sample within few microns contrary to XPS measurement with depth analysis of about 8-10 nm. The elemental concentration of the porous layer taken at different surface locations is summarized in Table 1 and indicates that only As and O atoms are present in detectable quantities. This is due to the preferential dissolution of Ga during anodization, leaving a significantly higher As/Ga ratio in the porous layer. This is in agreement with the work of Steer et al. who have shown that Ga dissolved faster than arsenic during polarization in phosphoric acid [359].

Name	**Binding Energy (eV)**	**FWHM (eV)**	**%At Conc**	**% Mass Conc**
O 1s	531,2	2,605	23,46	6,15
Ga 3d	23,2	2,335	0,58	0,66
As 3d	42,2	2,758	75,96	93,19

Table ANX 1: Chemical composition of the porous sample by XPS measurements taken at the surface.

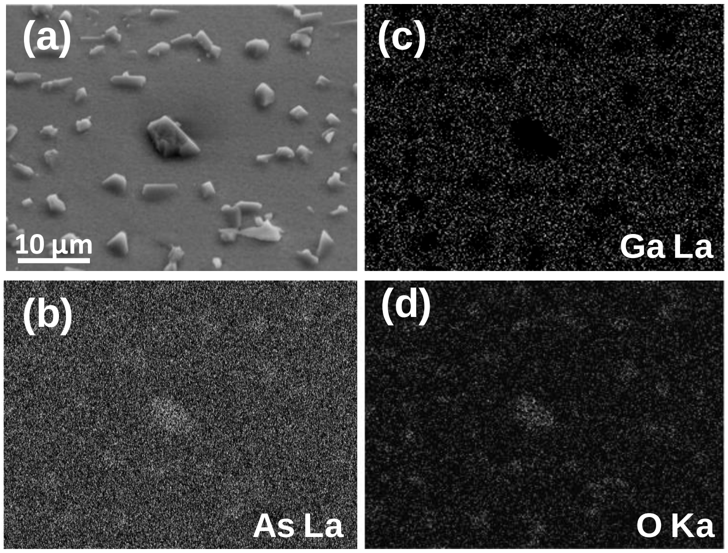

Figure ANX 6: EDX mapping of a porous p-GaAs layer formed in 49%HF solution at 2mA/cm^2. (a) The top view SEM image and the EDX element maps for (b) As, (c) Ga and (d) O elements.

I.5.4 Electrochemical mechanisms

In order to explain the behavior of GaAs transformation to porous arsenic oxide under anodic bias, we propose a qualitative model based on the decomposition of compound semiconductors in contact with electrolytes [361]. Fig (8) schematically illustrates the etching mechanism of GaAs in a HF solution. The electrochemical dissolution of semiconductors depends essentially on the symmetry of bi-functional etching agents [41]. The GaAs dissolution in HF is similar to InP in HCl [364]. The first step involves a synchronous exchange of bonds: Ga-F and As-H bonds replace the GaAs surface bonds [365]. The surface becomes H-passivated if the crystal was As-terminated or F-passivated if the crystal was Ga-terminated [366]. This reaction increases the bond polarity of goshawks atoms. Since the surface atoms are doubly bonded to the bulk in the (001) orientations and triply bonded to the bulk in the (111) orientations [367], two and three GaAs bulk bonds must be broken to remove each atom from the lattice following:

$$GaAs + 3HF \rightarrow GaF_3 + AsH_3 \quad (1)$$

Note that the last Ga-As bond should be broken without substitution to produce GaF_3 and AsH_3.

The second step consists in the formation of arsenic. The elemental arsenic (As) can be obtained by two ways: i) chemically: from the arsine molecules AsH_3 as shown in Fig (8.a). In this case a non-uniform As layer was obtained due to the difficulty of the nucleation [353] following:

$$2AsH_3 \rightarrow 2As + 3H_2 \quad (2)$$

ii) Electrochemically: by involving holes (Fig (8.b)) or protons (Fig (8.a)) in a redox reaction following a three-holes mechanism proposed for the etching of GaP [368] and InP [364]. For p-GaAs, an accumulation of majority charge carriers (holes) takes place at the surface [369]. In aqueous HF solutions, three holes are required to dissolve one Ga-As entity in which only the Ga element is oxidized. This highlights the increasing of the etch rate with the current density applied as shown in Fig (1). In this case, a uniform As layer was obtained due to the uniform injection of holes following:

$$GaAs + 3h^{+} \rightarrow Ga^{3+} + As \quad (3)$$

It was observed that a brown film of As was formed on the electrode during electrochemical etching [353]. The same behavior was revealed in the case of InP etching in HCl solution with a high content of Phosphorus but not Indium [364]. We suggest that the injection of the holes anodically speeds up this selective etching which explains the low Ga concentration obtained previously in the porous layer.

The last step consists in the formation of As_2O_3. The presence of water in the electrolyte solution oxidizes elemental As following:

$$As + 2H_2O + 3h^+ \rightarrow AsO_2^- + 4H^+$$

$$2AsO_2^- + H_2O \rightarrow As_2O_3 + 2OH^- \quad (4)$$

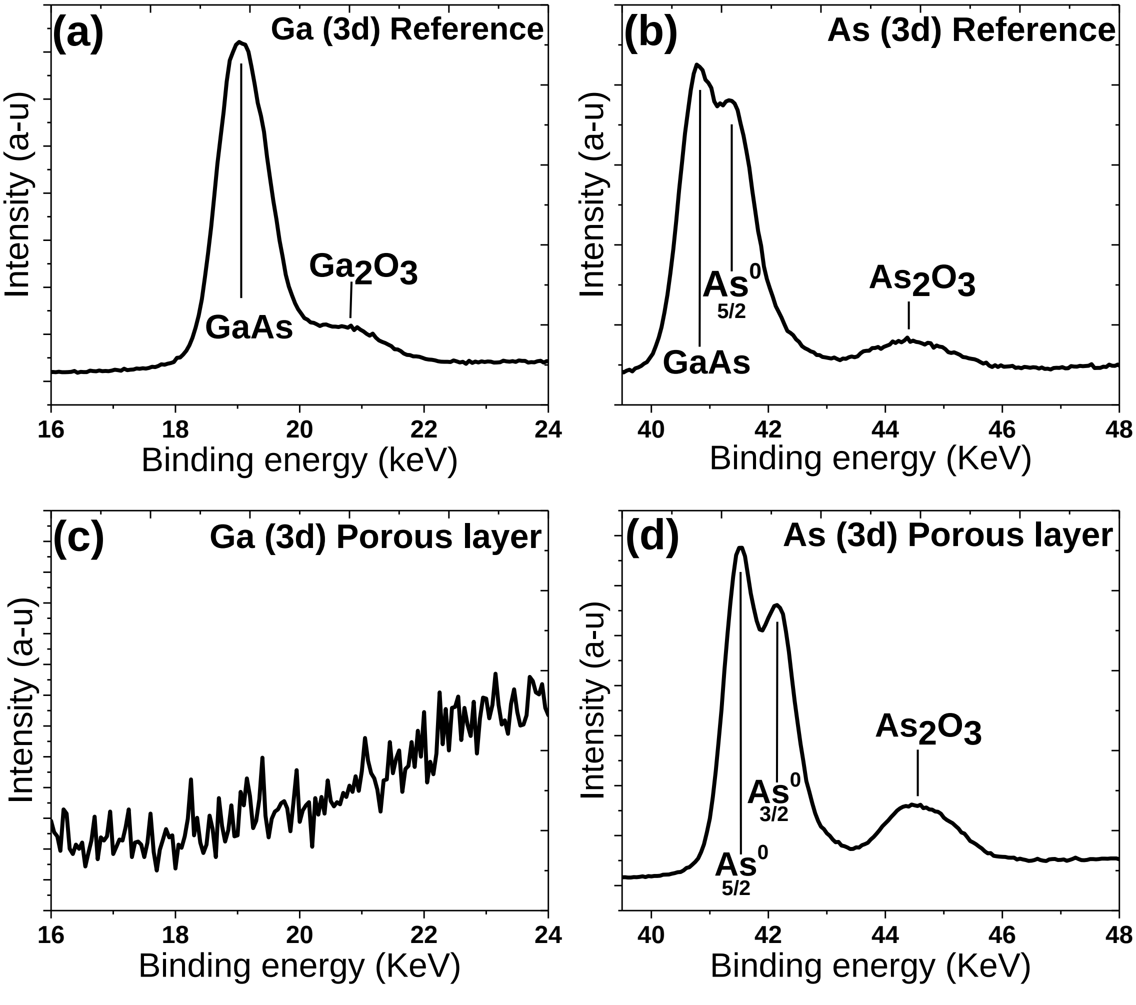

Figure ANX 7: Ga 3d and As 3d XPS spectra of p-GaAs reference (a,b) and porous p-GaAs samples (c,d) immediately after anodization in 49%HF solution at 2 mA/cm^2 showing that only the As and O are present in detectable quantities.

Fig (8.c) shows 3D structures of As_2O_3 obtained on the electrode surface following reaction (2) or reaction (3) via As transformation to As_2O_3 by convective diffusion [364], [365]. Additionally, the chemical formation of As_2O_3 and the porosification process can take place simultaneously, which produces a porous arsenic oxide layer as shown in Fig (8.d). The low crystallite dimension is obtained by the nucleation and the coalescence of the oxide layer formed on the wall pores, which will stop the reaction.

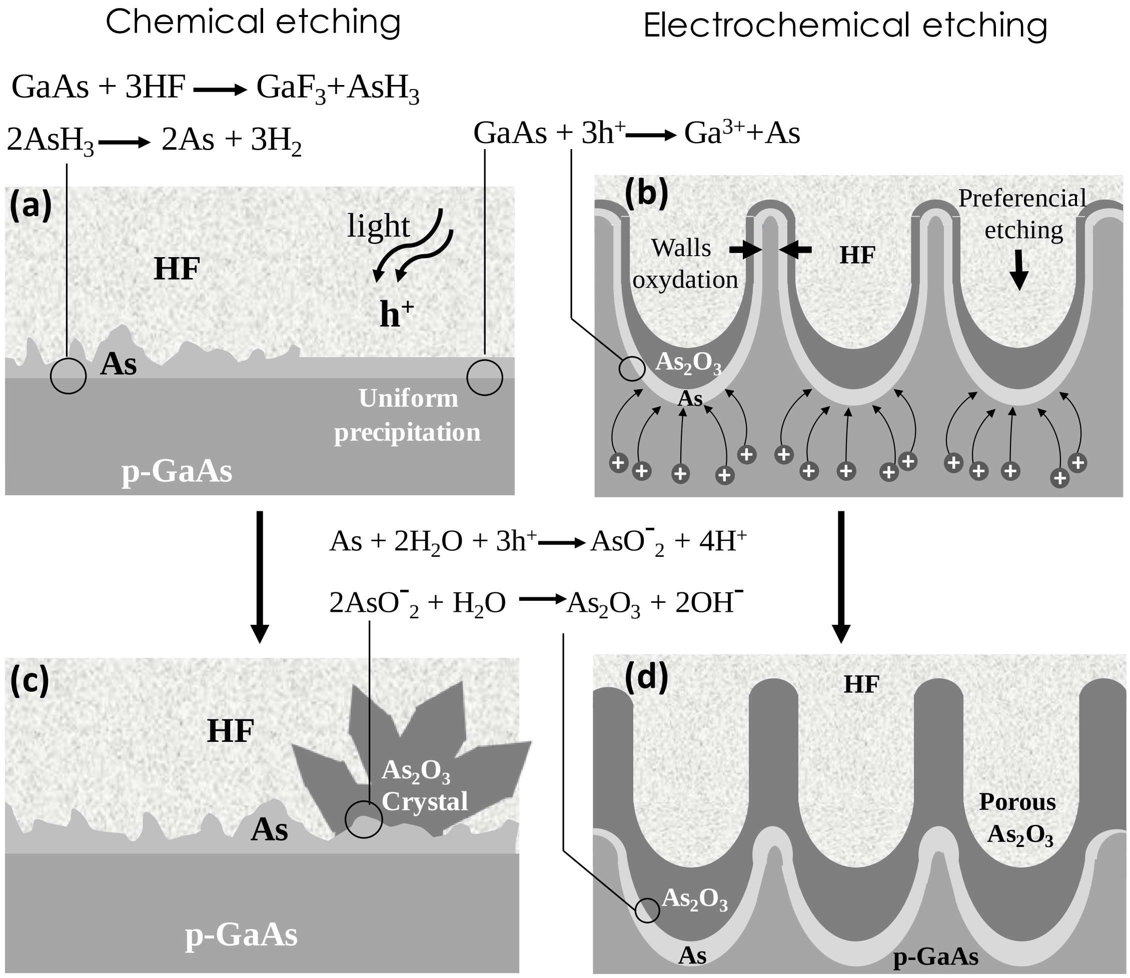

Figure ANX 8: Chemical and electrochemical etching mechanism of GaAs in HF solution.

I.5.5 Structural analyses

The last measurement was performed by powder XRD to investigate the crystal structure of the porous film. Fig (9) shows the diffractogram of a crushed porous layer obtained by scraping and grinding the porous sample to ensure that the measurement takes place on the porous layer and not on underlying GaAs substrate. The single-crystal X-ray diffraction measurement is obtained by mounting the crushed porous particles on the goniometer. All other diffraction peaks can be identified as the standard cubic of arsenolite structure (As_2O_3) with a lattice constant of 11.06 A°. No peaks from other expected phases such as GaAs (zincblende) or As_4O_6 (cubic) are observed within the detection limit of our technique. Effectively, all the peaks correspond to the reflections from (111), (222), (400) and (331) planes of the cubic phase of As_2O_3 [370]. Hence, the XRD patterns show that the As_2O_3 film is of a single phase. The intensity of the (111) peak is very strong and its width at half maximum is relatively narrow, indicating a good crystallization state through a large crystallites size.

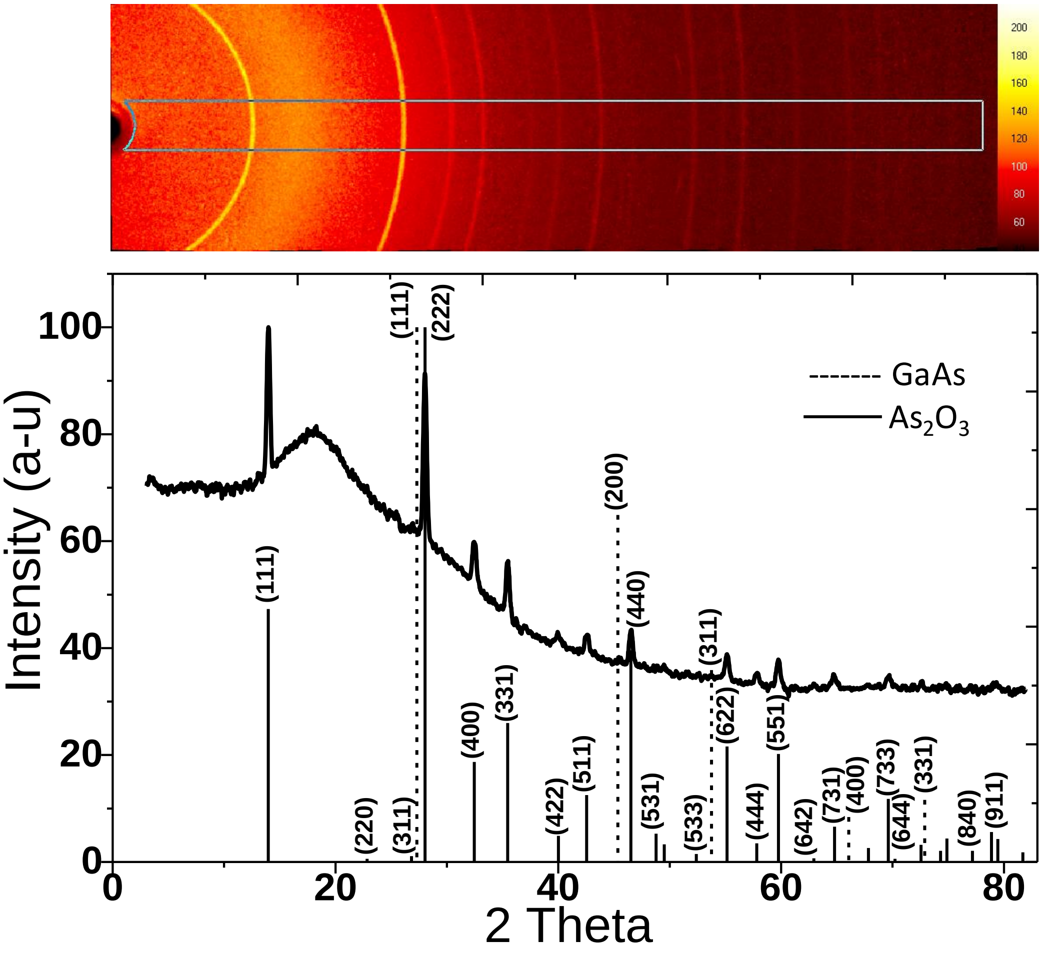

Figure ANX 9: Powder XRD of porous p-GaAs layer formed in 49%HF solution at 2mA/cm^2, which corresponds to As_2O_3 crystal.

I.6 Conclusions

The nano-structural and chemical nature of porous layers obtained by the anodic etching of p-type GaAs has been investigated. No detectable CL has been attributed to the chemical change of porous GaAs during anodization. Chemical analysis shows that the porous material is depleted of Ga atoms and contains significant amounts of oxygen. Structural data from XRD show that the porous material is composed essentially of crystalline As_2O_3. An electrochemical process is proposed to explain such a behavior.

I.7 Acknowledgements

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ANNEXE II LISTE DE PUBLICATIONS

- **Journal papers:**

- **In progress:**

Youcef. A. Bioud, Abderraouf Boucherif, Maksym Myronov, Ali Soltani, Gilles Patriarche, Dominique Drouin and Richard Arès, “Integration of Ge subcell on defect-free Ge/Si virtual substrates towards Inexpensive, High-performance Multi-Junction Solar Cells on Silicon”. Being drafted for **Solar Energy Materials and Solar Cells**.

- **Submitted (under review):**

Youcef. A. Bioud, Abderraouf Boucherif, Maksym Myronov, Ali Soltani, Gilles Patriarche, Nadi Braidy, Dominique Drouin and Richard Arès, “Dislocation-free, heteroepitaxy using highly scalable process” Under review - **Nature Communications**, 2018.

Youcef. A. Bioud, Abderraouf Boucherif, Maksym Myronov, Ali Soltani, Gilles Patriarche, Dominique Drouin and Richard Arès, “Ultra-low defect density by epitaxial Ge overgrowth on Porous Ge-on-Si engineered substrate”. Submitted in **APL Materials**, 2018.

- **Accepted:**

Meghan N. Beattie, Youcef A. Bioud, Abderraouf Boucherif, Dominique Drouin, Richard Arès, Christopher E. Valdivia, and Karin Hinzer, “Multi-Junction Solar Cells on Si Substrates with a Voided Ge Interface Layer: Effect of Substrate Doping on Simulated Cell Performance”. The 7th edition of the World Conference on Photovoltaic Energy Conversion (WCPEC-7), 2018, Waikoloa, Hawaii, USA. **IEEE Conference Proceeding**.

- **Online:**

Meghan N Beattie, Youcef A Bioud (co-first author), David G Hobson, Abderraouf Boucherif, Christopher E Valdivia, Dominique Drouin, Richard Arès and Karin Hinzer, “Tunable conductivity in mesoporous germanium” accepted in **Nanotechnology**, 2018.
http://iopscience.iop.org/article/10.1088/1361-6528/aab3f7/meta [278]

Youcef A Bioud, Abderraouf Boucherif, Ali Belarouci, Etienne Paradis, Simon Fafard, Vincent Aimez, Dominique Drouin, Richard Arès, “Fast growth synthesis of mesoporous germanium films by high frequency bipolar electrochemical etching” **Electrochimica Acta** 232 (2017) 422–430. *https://www.sciencedirect.com/science/article/pii/S0013468617303936* [204]

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- **Scientific activities:**

https://youcefbioud.wixsite.com/nanoart

- **Specialised Conferences:**

- **Invited:**

C. Valdivia, M. N. Beattie, Y. A. Bioud, D. G. Hobson, A. Boucherif, D. Drouin, R. Arès, K. Hinzer "Mesoporous Germanium for High Efficiency Photovoltaic Cells" The 42nd International Conference & Exposition on Advanced Ceramics & Composites (ICACC), **2018**, Daytona Beach, Florida, USA.

A. Boucherif, M. Jellit, Y. A. Bioud, A. R. Boucherif, R. Arès "Virtual substrate engineering with nanoporous semiconductors and graphene-based nanocomposites" Photonics North **2018**, Montreal, Canada.

- **Oral presentations:**

Y. A. Bioud, A. Boucherif, M. Jellit, A. Soltani, G. Patriarche, D. Drouin, R. Arès, "Defect-free Ge/Si Virtual Substrate for III-V multi-junction solar cells". SPIE Photonics West Opto Conference, **2019**, San Francisco, California, United States.

Y.A. Bioud, A. Boucherif, E. Paradis, A. Soltani, D. Drouin and R. Arès, "Defect-free, hetero-epitaxy through electrochemical etching of germanium for multijunction solar cells applications". The 11th Porous Semiconductors - Science and Technology, **2018**, La Grande Motte, France.

Youcef A. Bioud, Abderraouf Boucherif, Maksym Myronov, Ali Soltani, Gilles Patriarche, Nadi Braidy, Dominique Drouin and Richard Arès, (presented by M. Myronov) "High-quality Ge/Si virtual substrates fabricated by a low cost and scalable process". The 9th International SiGe Technology and Device Meeting (ISTDM) and the 11th International Conference on Silicon Epitaxy and Heterostructures (ICSI), **2018**, Potsdam, Germany.

Youcef A. Bioud, Abderraouf Boucherif, Dominique Drouin, Richard Arès, "Low cost Ge/Si virtual substrate engineering for III-V multi-junction solar cell" The 13th International Conference on Concentrator Photovoltaics, **2017**, Ottawa, Canada. [374]

Meghan N Beattie, David G Hobson, Christopher E Valdivia, Karin Hinzer, Youcef A Bioud, Abderraouf Boucherif, Dominique Drouin, Richard Arès, "Quasi-monocrystalline Ge as an interface layer for multi-junction solar cells on Si substrates: Electrical resistivity and device modelling", Photonics North (PN), **2017**, Ottawa, Canada. [375]

Meghan Beattie, Youcef Bioud, Abderraouf Boucherif, David Hobson, Richard Ares, Dominique Drouin, Christopher Valdivia, Karin Hinzer, "Electrical Resistivity of Mesoporous and Quasi-Monocrystalline Germanium", MRS Spring Meeting, **2017**, Phoenix, Arizona, United States.

- **Posters:**

Meghan N. Beattie, Youcef A. Bioud, Abderraouf Boucherif, Dominique Drouin, Richard Arès, Christopher E. Valdivia, and Karin Hinzer, "Multi-Junction Solar Cells on Si Substrates with a Voided Ge Interface Layer: Effect of Substrate Doping on Simulated Cell Performance". The 7th edition of the World Conference on Photovoltaic Energy Conversion (WCPEC-7), **2018**, Waikoloa, Hawaii, USA.

Youcef A. Bioud, Abderraouf Boucherif, Etienne Paradis, Ali Soltani, Dominique Drouin, Richard Arès, "Low cost Ge/Si virtual substrate through dislocation trapping by nanovoids" The 10th International Conference on Silicon Epitaxy and Heterostructures, **2017**, Coventry, UK.

Meghan N. Beattie, Youcef A. Bioud, Abderraouf Boucherif, David G. Hobson, Richard Arès, Dominique Drouin, Christopher E. Valdivia, Karin Hinzer, "Quasi-monocrystalline Germanium: Electrical Resistivity Characterization for Multi-junction Solar Cell Applications", The 13th International Conference on Concentrator Photovoltaics (CPV-13), **2017**, Ottawa, Canada.

Y. A. Bioud, A. Boucherif, A. Belarouci, E. Paradis, D. Drouin, R. Arès, "Mosoporous germanium by high frequency bipolar electrochemical etching for optical sensor applications". The 10th PSST - Porous Semiconductors - Science and Technology, **2016** Tarragona, Spain. *(Student Grant: Awarded by PSST)*. [376]

Youcef A. Bioud, Abderraouf Boucherif, Ali Belarouci, Etienne Paradis, Dominique Drouin, Richard Arès, "Chemical composition of anodically formed p-type porous GaAs in HF based electrolyte". The 10th PSST - Porous Semiconductors - Science and Technology, **2016,** Tarragona, Spain. *(Student Grant: Awarded by PSST)*. [377]

Y. A. Bioud, A. Boucherif, S. Fafard, V. Aimez, D. Drouin, R. Arès, "Porous germanium single- and multilayers for solar energy applications". Colloque - Laboratoire Nanotechnologies et Nanosystèmes (LN2), **2016**, Estrimont, Québec, Canada.

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Y. A. Bioud, A. Boucherif, S. Fafard, V. Aimez, D. Drouin, R. Arès, “Formation and optimization of mesoporous germanium by bipolar electrochemical etching”. 17th Canadian Semiconductor Science and Technology Conference (CSSTC), **2015**, Sherbrooke, Canada.

Y. A. Bioud, A. Boucherif, S. Fafard, V. Aimez, D.Drouin, R. Arès, “Systematic study of mesoporous germanium formation regimes by bipolar electrochemical etching”. The 9th International Conference on Silicon Epitaxy and Heterostructures (ICSI-9), **2015**, Montreal, Canada. [374]

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