A contribution to synchronization of the sliding-mode control-based integrated step-down DC/DC converter

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A contribution to synchronization of the sliding-mode control-based integrated step-down DC/DC converter

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Abstract

Mobile applications necessitate nowadays huge digital-resources. Power management of a digital System-On-Chip (SOC) is based on dynamic voltage scaling. DC/DC converters used to supply the digital SoCs are facing stringent constraints with respect to load-transients, line-transients and reference tracking. Hysteretic control is known as the most convenient control scheme with a fair trade-off between transient performances, analog implementation and power consumption, particularly for one-phase architecture. The thesis focuses on-board DC/DC with a significant constraint on footprint (i.e. on components count and values).

Fixed switching-frequency hysteretic control has been experimented with significant results. Transient performances are reduced due to latency introduced in the switching frequency control. The present study focuses on the improvement of the concept as well as its implementation and the analysis of stability.

A new analog implementation of the sliding-mode control is presented with switching-frequency control using a particular analog phase-locked-loop but preserve transient performances. The DC/DC converter is implemented in CMOS 130 nm by STMicroelectronics. The switching frequency range has been voluntarily limited and excludes the possible integration of passive components for the sake of silicon access. A hybrid demonstrator is presented with efficiency higher than 80% between 2.4 mW and 960 mW output power.

Résumé

Les téléphones et tablettes de dernière génération embarquent une puissance de calcul numérique très importante nécessitant une puissance électrique d'alimentation toute aussi significative. Afin de réduire la consommation énergétique des composants numériques complexes des terminaux mobiles, des techniques de modulation dynamique de la tension d'alimentation et de la fréquence de fonctionnement du cœur de calcul numérique sont utilisées.

Le convertisseur DC/DC qui assure l'alimentation du cœur numérique doit donc faire face à de forts transitoires de charge, de tension de référence et de tension de source. Le contrôle en mode glissant d'un convertisseur DC/DC permet un bon compromis entre les performances transitoires du convertisseur, la réalisation via des composants analogiques et la puissance dissipée par le contrôleur. C'est pourquoi ce type de contrôle apparait être adapté au contrôle de convertisseurs DC/DC alimentant des cœurs numériques. Cette thèse a pour objet l'étude des alimentations sur carte électronique où le contrôleur et l'étage de puissance sont intégrés sur puce tandis que les composants de puissance passifs sont montés sur le circuit imprimé.

Le contrôle en mode glissant à fréquence de découpage fixe d'un convertisseur DC/DC a été démontré avec des résultats significatifs. Cependant les performances transitoires d'un tel convertisseur sont amoindries en raison des délais introduits par une fréquence de découpage fixe. Une nouvelle structure de régulation de fréquence de découpage d'un convertisseur DC/DC contrôlé en mode glissant est proposée dans cette thèse. Cette structure régule la fréquence de découpage moyenne du convertisseur tout en maintenant la réponse transitoire du convertisseur asynchrone par rapport à l'horloge de référence. Une analyse de stabilité qui prend en compte les spécificités d'un tel système est aussi proposée.

Le convertisseur a été conçu sur un procédé CMOS 130nm de STMicroelectronics. La fréquence de découpage est maintenue volontairement faible pour conserver un rendement élevé avec des composants passifs externes. Le prototype présente un rendement supérieur à 80% entre 2.4mW et 960mW de puissance de sortie.

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Acronyms

AB Analog Baseband

AC Alternating Current

ACPI Advanced Configuration and Power Interface

ADC Analog to Digital Converter

AOT Adaptive On-Time

ASIC Application Specific Integrated Circuit

ATX Advanced Technology eXtended

BGA BallGrid Array

BOM Bill Of Material

CMFB Current-Mode FeedBack

CMOS Complementary Metal Oxide Semiconductor

CMSM Current-Mode Sliding-Mode

COT Constant On-Time or Constant Off-Time

CSM Current Sliding-Mode

D-flop Delay flop

DB Digital Baseband

DC Direct Current, equivalent to Continuous mode

DC/DC Direct Current to Direct Current

DCR Direct Current Resistance

DFT Design For Test

DUT Device Under Test

DVFS Dynamic Voltage and Frequency Scaling

EMI ElectroMagnetic Interference

ESL Equivalent Serial inductor (L)

ESR Equivalent Serial Resistor

EV² Enhanced V^2

FFT Fast Fourier Transform

FLL Frequency Locked Loop

GPIO General Purpose Input/Output

ICO Current Controlled Oscillator

IP Intellectual Property

LISN Line Input Stabilization Network

MIM Metal Insulator Metal

MIMO Multiple Input, Multiple Output

MLCC Multi-Layer Ceramic Capacitor

MSPS Mega Sample Per Second

OS Operating System

PCB Printed Circuit Board

PFD Phase Frequency Detector

PFM Pulse Frequency Modulation

PID Proportional Integral and Derivative

PLL Phase Locked Loop

PMU Power Management Unit

PSRR Power Supply Rejection Ratio

PWM Pulse-Width Modulation

RPM Ramp Pulse Modulation

RS-flop Reset or Set flop

SMPS Switched-Mode Power Supply

SOC System On Chip

TOC Time Optimal-Control

VCO Voltage-Controlled Oscillator

VSM Voltage Sliding-Mode

WFI Wait For Interrupt

Chapter 1

Introduction

With more than 7 billion mobile connections in 2013 and an annual 7% growth rate, the mobile market segment provides strong terminal delivery opportunities[1]. It is an opportunity for components manufacturers such as STMicroelectronics to sold large volume of high-end components. Furthermore, smartphones and tablets reach the same entertainment capability as computers and are no longer intended to be used only for voice call or text-messaging but they offer web-browsing, video broadcast decoding and gaming capabilities.

The required computing performance can only be provided by specialized hardware built around a low power embedded processor surrounded by specialized peripherals such as video decoders, 2D/3D graphic engines, communication interfaces etc... Silicon large scale integration permits the production of integrated circuits with billions of transistors necessary to integrate a lot of the required computation functions on a same silicon die. Such a circuit is called a System On Chip (SOC), Digital Baseband (DB) or Application Processor (AP) in the world of platform providers.

In order to offer a complete electronic solution for smartphones and tablets, the aforementioned AP is integrated in a multi-chip solution, soldered with many passive electronic components on a dedicated electronic board such as the one presented in Figure 1.1. The valuable circuits giving its functions to the platform require dedicated power supplies. Power components and associated passives are outlined by white dashed

[1] data from the GSMA association: www.gsma.com

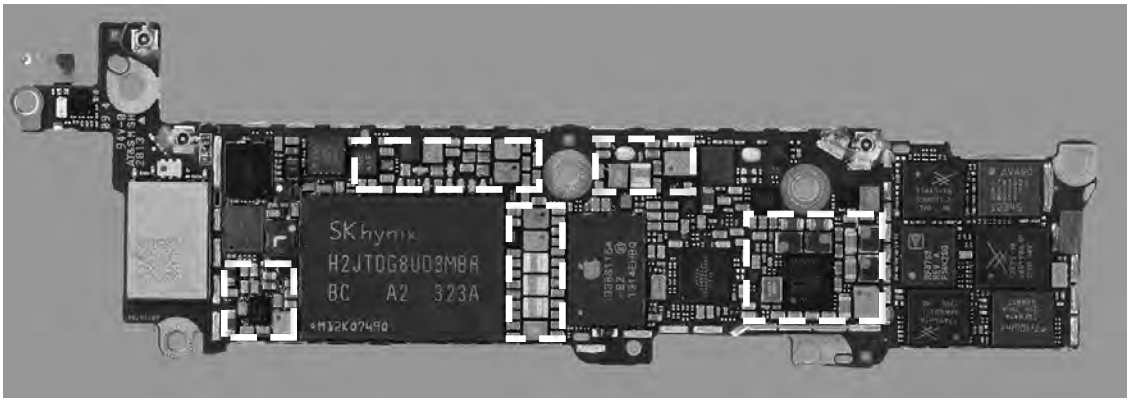


Figure 1.1 – Picture of a high-end smartphone board (Apple® iPhone® 5C)

line boxes. The relative board occupancy represented by power conversion components is large. Tremendous efforts are developed to reduce their footprint or even to integrate power-solutions on-chip. Various DC/DC converters are used to convert the battery voltage that is ranging from 4.5 V to 2.8 V for a single cell Li-Ion battery into an output voltage that can be either fixed or variable and higher or lower than the battery voltage. The processed power is ranging from a few μW to several W under a few volts. The digital components are designed with advanced silicon process that requires low voltage supply in the order of 1 V. Step-down converters are required to convert the battery voltage into a lower digital-supply voltage.

Step-down converter design involves many tradeoffs that are attempted to be illustrated in Figure 1.2 for a given non-isolated step-down architecture. All the listed converter characteristics depend on the size, the value and the performance of the power passive components.

- A small footprint is achieved at the expense of a larger output voltage ripple. The smaller the output capacitors the larger the output voltage ripple.
- Electro-Magnetic Interference (EMI) filters that prevent from unwanted malfunctions are generally bulky: small footprint can be achieved at the expense of increased generated EMI.
- The EMI filter degrades the converter efficiency with the addition of elements in the power distribution network and the transient performance as well since it damps the power-line currents.

- The efficiency is a key converter characteristic that not only depends on the silicon process but also depends on the transient performances, the footprint and the converter ratio of output voltage to input voltage.
- Large transient performances are generally achieved thanks to a high switching frequency that increases the switching losses compared to a reduced switching frequency or by adding decoupling capacitors that increase the board occupancy.
- Extreme conversion ratios make the power efficiency optimization of the converter difficult since at least one switch in the design conducts most of the time.
- Maintaining a low ripple under extreme conversion ratios requires a particular care since the output voltage has to be maintained constant while at least one inductor-current slope is high.

Taking into account the board-area occupied by power passive components outlined in Figure 1.1 and the design tradeoffs presented in Figure 1.2, one key issue is to diminish the passive elements' size without impact on the transient performances and the generated EMI at similar efficiency. At first sight this requires no significant changes in the switching frequency and in the power structure in order to keep the efficiency high but the DC/DC converter control needs a complete review. The MHz switching frequency range of the present time DC/DC converter permits to maintain the efficiency high[2] with small and low cost passive power components. Voltage mode control transient performances are limited by the switching frequency what does not permit a control bandwidth higher than a tenth of the switching frequency. It is required to think beyond the voltage-mode PWM to increase the transient regulation speed while keeping the switching frequency in the same order of magnitude.

In order to "think beyond PWM" the second chapter presents the power requirements of targeted digital circuits. Then the state-of-the-art of sliding-mode based control that can switches at low frequency but responds quickly is presented. In the third chapter the principle of operation of the proposed original circuit that adds a frequency regulation loop to a sliding-mode converter is analysed. In the fourth chapter a multi-input-multi-output stability analysis that uses a closed-loop sampled data approach is

[2]Higher than 80 % over a large output power range

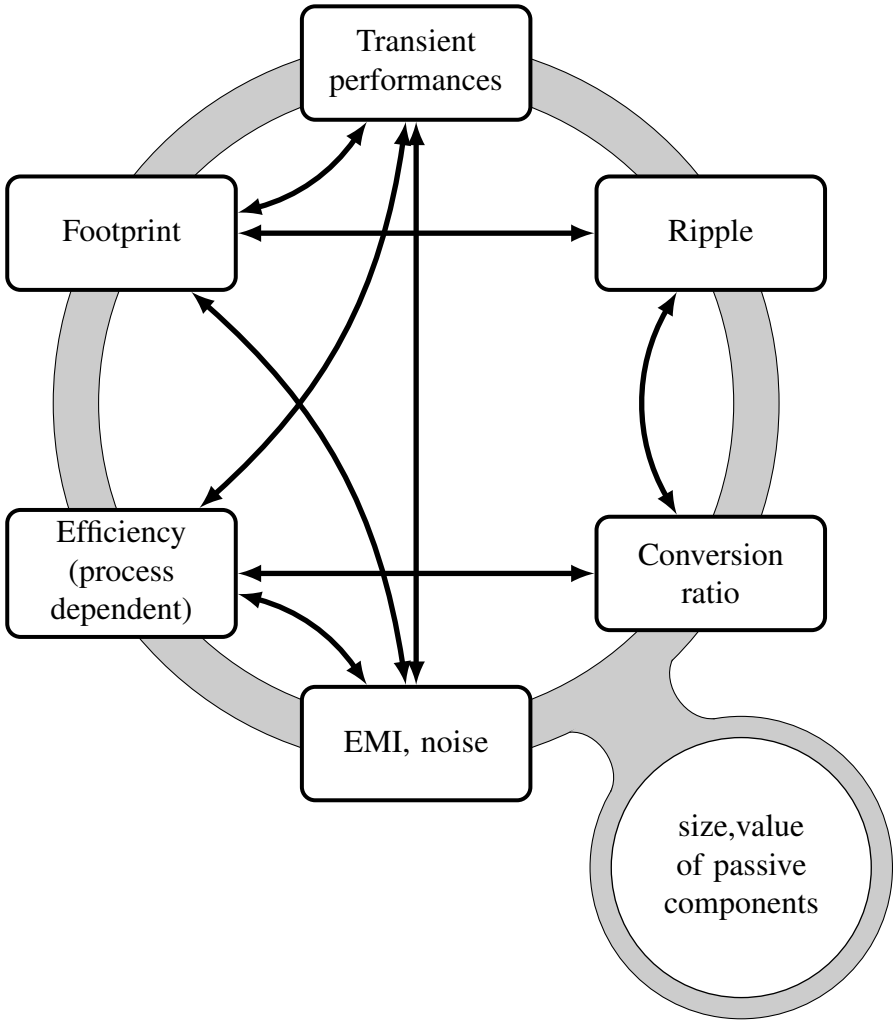


Figure 1.2 – Step-down design tradeoff hexagon

presented. Then the fifth chapter covers the most pertinent issues of CMOS design and the test-setup of the chip-prototype. Various results of the test-chips are gathered and commented in the sixth chapter and a general conclusion that includes proposal for short-term improvements and perspectives makes the seventh chapter.

Chapter 2

State of the Art

One may argue that power delivering for high demanding digital core is a widely covered topic. Since the beginning of the digital era, solutions to deliver the right amount of voltage to a digital core have been described and developed. Nevertheless the requirements of the low power embedded computing requires a deeper analysis ever. A qualitative analysis is the first part of this chapter. The behaviour of a smartphone suitable core is described in order to outline the need for a dedicated DC/DC converter. Latter architecture is mainly inductive to comply with the need for high efficiency and high output current.

As a starting point this chapter focuses on the voltage-mode Pulse-Width Modulation (PWM) control of a standard buck converter, operating in continuous conduction mode. This control principle has been widely covered since the beginning of Switched Mode Power Supply (SMPS) design [35]. Current-mode control is also presented. This control principle involves two different loops and exhibits behaviours that are quite common in non-linear converters. Finally the sliding-mode control of a buck converter is presented.

Only analog controllers are presented since digital control requires the use of an Analog-to-Digital Converter (ADC) that has been arbitrarily discarded at the beginning of this thesis due to power consumption considerations. **Nevertheless it is still worth to mention recent developments in the field of digitally controlled DC/DC converters as in [114]**

Within sliding-mode control, Time-Optimal Control (TOC) targets optimal transient responses [8, 25, 57, 58, 86, 88]. This control is intended to reach the best transient response that is allowed by the power filter. **At a given power-stage and passive-filter setting TOC control gives the best possible transient response where the only limitation is given by the current-slew rate limit of the inductor and the energy stored by the capacitor. This principle is detailed in [58] and a current-limited version is proposed in [25].** Nevertheless the theory faces practical challenges such as current limitation and transient detection. Digital control is used to perform such a regulation. However sliding-mode control with a proper sliding-surface selection is a good candidate to approximate the best in class transient response offered by a TOC approach.

Sliding-mode control is thus proposed to outperform the voltage-mode control transient performances. However sliding-mode control switching frequency is uncontrolled. The converter efficiency depends significantly on switching frequency as well as Electro-Magnetic Interferences (EMI). Thus ways to manage the switching frequency of a sliding-mode based control are studied. Differences between clock-based modulations and free running switching frequency adjustments are outlined by the use of a classification between a so-called hard synchronization paradigm and a so-called soft synchronization paradigm respectively.

1 Digital SOC requirements

Analysis of the power supply requirements of a microprocessor involves at least three different points of view. First the electrical characteristics and properties of the elementary components used in the System On Chip (SOC) define absolute voltage ratings and local losses. Second the digital design allows the usage of power reduction techniques such as clock and power gating that modulates the amount of active logic glue. Third the software adjusts the overall digital speed to the software workload.

For instance:

1. The use of Fully-Depleted Silicon-On-Insulator (FDSOI) process and proper body biasing techniques reduces the leakage currents through a single MOSFET [22, 33, 55, 59]. In [100] different transistor threshold voltages are used depending on

the application. A low threshold value for high and frequent switching and a high value for rare switching operation.

2. Parallel computing capability, clock tree optimization and multiple core management with Big-Little technique are ways to optimize the power efficiency of a large digital logic system by design.

3. Nowadays as described in [22], the available computing capability of a quad core device is not fully used by the software. A large amount of performance gain can be expected from this point of view by a better usage of the available computing hardware.

1.1 First level: Device properties

First-level action is linked to the semiconductor process options and elementary device optimization.

1.1.1 Leakage currents

The silicon process used to fabricate the digital SOC defines the voltage supply range and the associated leakage currents. These currents depend strongly on the device geometry, the process and the temperature. The three major leakage current sources in an advanced process device are [82]

- **sub-threshold current**: that is the current flowing from the drain to the source of a transistor when it is in the off state. With advanced process, the threshold voltage of the transistor is lowered and the sub-threshold current increases.

- **gate-oxide tunnelling current**: with the decrease in the gate oxide thickness a non negligible tunnelling current flows from gate to source and/or drain overlap or from channel to gate.

- **junction band-to-band current**: with a significant supply voltage a current flows through the junctions that results from the drain and source implementations and the substrate.

All these phenomena yield a global supply current which mainly depends on the operating temperature and supply voltage. Voltage supply reduction and substrate biasing are techniques used to reduce the leakage power at physical level while power gating technique is used at system level [32]. From the power supply point of view, the power gating technique adds a source of high variability in the load. By turning-off a large part of the SOC, the leakage current is totally suppressed and generates a load step [46]. Inversely when the subsystem is powered-on, the leakage current arises and produces a load step as well.

1.1.2 Switched currents

Managing the total amount of logic cells active at a time enables to control the equivalent capacitance, C_{eq}, represented by the logic cells. Dynamic power consumption as in (2.1) is reduced according to C_{eq}:

$$P_{load-sw} = \alpha C_{eq} V_o^2 f_{db} \tag{2.1}$$

where f_{db} is the clock frequency, V_o the supply voltage and α the activity factor of the digital chip. At each digital clock-cycle a variable amount of logic cells is switched, that produces a variable amount of charge transferred through the supply rail to the parasitic capacitors and through the parasitic capacitors to the ground. A well optimized device presents low switched parasitic capacitors in order to increase its switching speed and lower its power consumption. **Interconnect parasitic elements also play a major role in the process-related losses [99].**

1.2 Second level: Digital design

Digital design can also influence main terms in (2.1).

1.2.1 Reducing α:

The latter activity factor α is a highly random variable especially when dealing with a complex SOC like a smartphone digital baseband (DB) in which the number of internal

possible states is huge. Furthermore the activity factor is highly software dependent since each processor instruction leads to different switches to be activated depending on the previous instructions that define the previous cycle state of each gate.

For short duration a simple but efficient way to cut the power consumption is to gate the clock of unused logic block. The system clock is locally turned off and the considered logic is not switched. This solution does not avoid the leakage current effects at the expense of a ready-to-use logic block but increases the load variability. Large current spikes and steps are frequent when the clock is partially gated [40]. Thanks to an aggressive clock gating strategy, the average activity factor can be highly reduced. In [100] experiments show that more than 92% of the gates are clock-gated.

1.2.2 Reducing V_o:

Power gating is extensively used to diminish the power consumption in a complex SOC. The operation principle follows a simple concept: shutting down the unused logic blocs. When a complete digital block is unused for a large amount of time, turning-off its power supply avoids leakage currents as well as switching losses [59]. Unfortunately powering up a digital section requires a non-negligible amount of time and is not energy free.

Time delay of a digital signal through a gate depends on the supply voltage. The higher the supply voltage, the lower the transit time and as a result, the higher the feasible clock frequency. Thus the DB operates with a relatively high supply voltage value when the clock frequency is high (1.3 V) and a lower one when the clock frequency is low (e.g. 0.6 V).

1.2.3 Reducing f_{db}:

The maximal clock frequency is expected to rise for a while since it is the one of the few marketing data available to the general public to compare different DB chip. The best-seller Galaxy S3 from Samsung uses an ARM quad-core A9 processor that runs at 1.4 GHz while ST-Ericsson demonstrates a 2.5 GHz processor during the 2013-mobile world congress [22] and 3 GHz clock frequency is proposed in [55].

However the computing capability can be adjusted to the required one by a proper system clock reduction in order to save more energy. Depending on the software workload, the system clock of a processor is adjusted to meet with the computing requirement criterion and the power consumption criterion as shown in [54]. With a decrease in the system clock frequency, the supply voltage can be lowered and the dynamic losses are lowered in a cubic manner[1].

Dynamic Frequency Scaling (DFS) is a popular technique to lower the power consumption and can be used with its voltage counterpart, the Dynamic Voltage Saling (DVS). The combination of the two techniques is called Dynamic Voltage and Frequency Scaling (DVFS) [43, 55].

1.3 Third level: software optimization

A modern microprocessor uses the above-mentioned technique to perform "*Energy-Proportional Computing*" [41]. The adjustment of the computing capability of the SOC is now directly performed by software [60, 76]. The need for software-based power management or Advanced Power Management, offers a software access to the hardware tools used for power management. Advanced Configuration and Power Interface that were defined during the beginning of 2000's established the foundation of an operating-system-based power management scheme.

Linux kernel extensively uses DVFS strategies to reduce the power consumption in mobile devices with the use of "CPUfreq Governor" driver [60]. This software power management driver allows the use of multiple strategies to modulate the clock frequency of a digital core. Depending on the task management strategy, different operation strategies can be set such as a slow but progressive variation in the system clock or a fast jump to the higher system clock when a task requires more computing capability. In [60] an application-based power optimizer that extends the OS-governor software features is proposed. This demonstrates the software dependency of the power consumption.

To save power the computing capability has to be adjusted to closely match the requirements by quick changes between operation states. The higher the transient capability of the supplying converter, the higher the saved amount of energy. This is observed

[1] Quadratic for the supply voltage itself and one more order for the clock frequency

in [64]. The low frequency part of the running software generates large current pulses, while each instruction-sequence presents a high frequency signature.

2 The power delivery path

A typical power delivery path between the DC/DC output and the digital load is made up of various parasitic inductors and capacitors. A careful board layout is mandatory to limit the DC and AC power path impedance to low values. As multicore strategy becomes a standard, the power delivery network is modelled as a multidimensional network instead of a single filter [42]. The power path impedance models presented in [6, 42, 64, 87, 108, 123] are quite constant up to the switching frequency domain of conventional power converters (i.e. 0.5 to 5Mhz).

A simplified DC/DC to silicon-die impedance model is represented in Figure 2.1. Associated impedance and values are represented in Figure 2.2 and Table 2.1 respectively. These results are in-line with models presented before. The impedance remains constant up to approximately 1 MHz.

Low frequency regulation, below 1 MHz, is performed by the power supply. High frequency regulation is not intended to be provided by the power supply but by an array of decoupling capacitors. As a consequence the power delivery path is mainly resistive for the frequency range of interest. Furthermore, the power delivery path lowers the load current slope seen by the DC/DC converter. This relaxes transient regulation constraints since processor cycle variations described in 1 are filtered out by the power delivery path.

One way to get round the power delivery path limitations is to integrate the power supply on chip with the load. Then there is a reduced power delivery network between the DC/DC converter and the load since the load is directly connected to the converter. This approach is proposed in [43, 102, 105] where a DC/DC converter die is stacked onto a digital load or integrated on-chip. The fully integrated approach faces major technological challenges **and still requires a board-level DC/DC converter to lower the battery voltage to an intermediate voltage**. This option is not considered here and the presented work focuses on board-level DC/DC power supply.

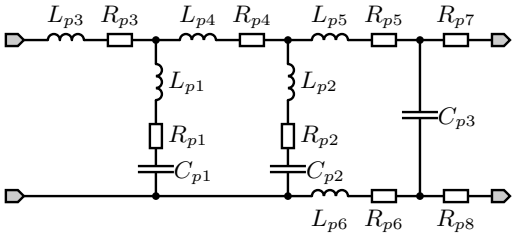


Figure 2.1 – Power path impedance model

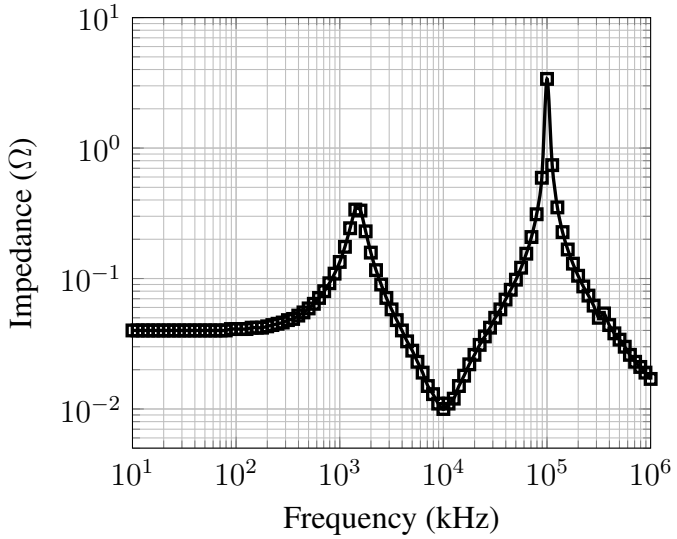


Figure 2.2 – Impedance model of the power delivery network

Table 2.1 – Power path impedance model - values

Component	Value	Unit
L_{p3}	10	nH
L_{p4}	1	nH
L_{p1}, L_{p2}	200	pH
L_{p5}, L_{p6}	25	pH
C_{p2}	1	uF
C_{p3}	10	nF
C_{p1}	200	pF
R_{p3}	30	mΩ
R_{p5}, R_{p6}	2.5	mΩ
R_{p7}, R_{p8}	2	mΩ
R_{p1}, R_{p2}, R_{p4}	1	mΩ

3 Power supply for digital systems

3.1 Relevant issues

Digital load analysis exhibits one major trend that is the high variability of the load, not only in term of current but also in term of output voltage. Figure 2.3 shows a core voltage and current measurements in a video decoding application. [42] classifies the processors current consumption in three categories:

- ”Step Currents”: a sudden change in the load current such as the first part of Figure 2.3.
- ”Pulse Currents”: repetitive current pulses such as the second part of Figure 2.3.
- ”Resonating Currents”: that are repetitive load patterns that may occur during the processor activity.

However no voltage and current dependent classification is proposed.

A considered worst case test vector is a wake-up from Wait For Interrupt (WFI) state. The processor is held in a retention mode with a minimal supply voltage such as 0.6 V and a minimal supply current of a few mA or nearly zero while waiting for an external interrupt. When the interrupt occurs, the processor jumps to a high computing capability state in a few clock cycles and requires the maximum allowed voltage close to 1.2 V and few amp current. In Figure 2.3 After a high demanding starting phase, the core operates alternatively with computing phase and WFI state. Sudden load transient between the lower core voltage with a quasi zero current and short but noticeable peak current and voltage occur each time the core leaves the WFI state.

The transient performance requirement that is related to the high variability of the load is outlined in Figure 2.4. The values used here are extracted from a ST-Ericsson internal document and represent the different operation margins used for the circuit behind Figure 2.3. The converter output-voltage must evolve between the maximum operating voltage and the minimum operating voltage. A too high voltage may engender irreversible damages thus the converter overshoot must be controlled. A too low voltage operation may lead to dysfunction of the DB. 44.4% of the down-margin is related to

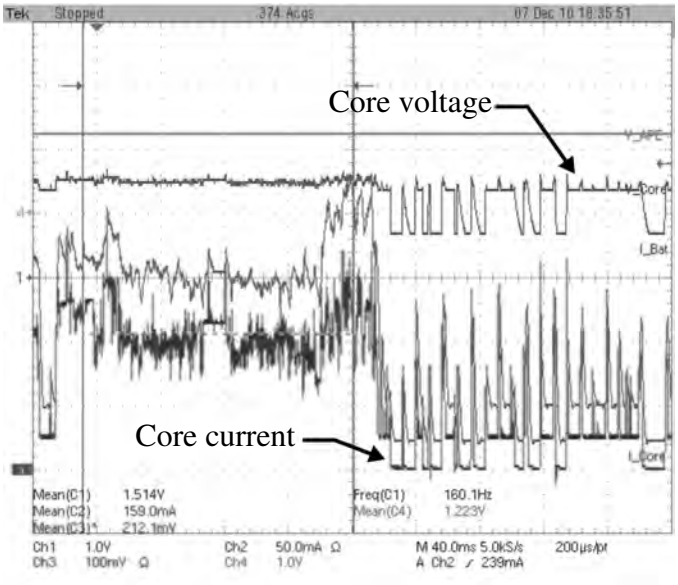


Figure 2.3 – Core voltage and current during a video decoding application, measurements performed on a ST-Ericsson U8500 platform decoding a H264-720p video

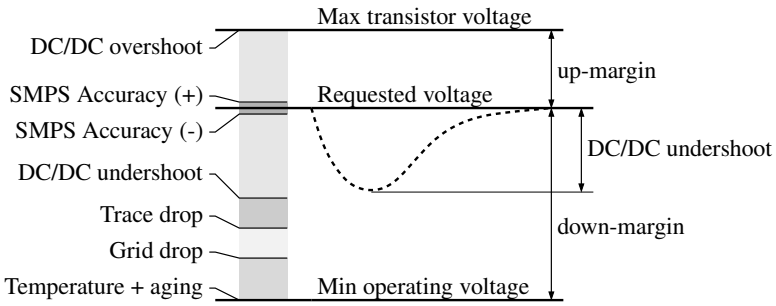


Figure 2.4 – Digital operation, voltage margins

the DC/DC converter transient operation. Reducing the transient undershoot allows to reduce the voltage-down margin, thereby the overall power consumption is reduced as well. There is probably a beneficial impact on the size of the components of the SMPS.

Low voltage regulation down to 0.6 V or 0.5 V leads to major design difficulties. The main one is the need of a low value inductor to go through the inductor current slope limitation that arises when only a low voltage has to be provided across the inductor during the falling current phase. The limited discharge slope of the inductor current engenders a non negligible overshoot and limits the small signal AC domain where the distortion of the inductor-current shall be low.

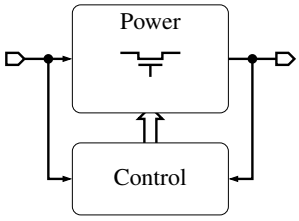
The high current requirement of a digital core leads to major design issues. Highest possible efficiency is targeted to preserve the system autonomy while a low cost[2] and low profile[3] solution is mandatory. Single phase converter that uses a single power stage is preferred to lower the Bill Of Material (BOM) cost and the solution board area.

3.2 Power conversion topologies

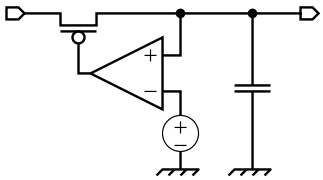
Non-isolated step-down converter topologies are presented in Figure 2.5. The first way to generate a lower output voltage than the input voltage is to create a drop across a resistive element such as a transistor operating in active region as represented in Figure 2.5a. A control circuit is used to modulate the pass-through element drop voltage, depending on the output voltage (feedback action) or the input voltage (feedforward action). Figure 2.5b represents the simplest way to design a Linear regulator. An amplifier compares the output voltage against the reference voltage and drives a P-channel MOSFET transistor in such a manner that the MOSFET operates in saturation mode and its drain to source voltage equals $V_{bat} - V_o$. Since the whole output current flows through the pass-through element, the power-efficiency is limited by:

$$\eta_{LDO_{max}} = \frac{V_o}{V_{bat}} \tag{2.2}$$

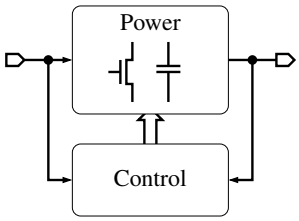
[2] silicon area penalty
[3] to cope with ever thin packages required to produce thin boards



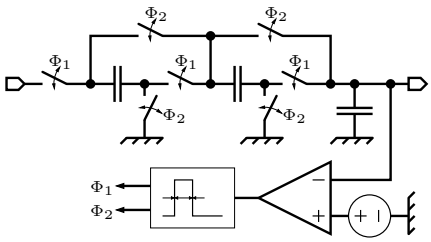
(a) Linear regulator (diagram)



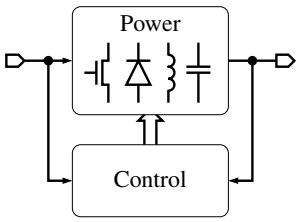
(b) Linear regulator (schematic)



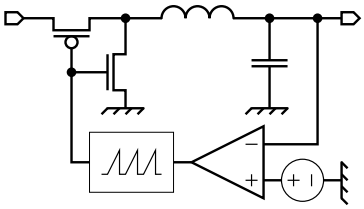
(c) Switched capacitors regulator (diagram)



(d) Switched capacitors regulator (schematic)



(e) Inductive regulator (diagram)



(f) Inductive regulator (schematic)

Figure 2.5 – Synoptic diagrams and principle schematics of considered DC/DC converters

This solution is obviously unsuitable for a high current load which can have a much lower supply voltage than the battery voltage and requires a high drop. For instance, when the operating voltage is down to 0.6 V and the supply current is around 100 mA, a 3.6 V battery supply yields an efficiency lower than 17%.

The linear regulator is still extensively used and developed in a no-capacitor configuration without external components but with fast transient response as in [121]. One key advantage of the linear regulator is the possible low power consumption of the controller that yields a high efficiency when the drop voltage is low as well as the output current. In [98] a linear regulator is used in parallel with a common DC/DC converter to extend the efficiency at low output current. The linear regulation scheme is best suited to generate a low noise output voltage since no switching noise is introduced in the output voltage. Noise rejection of linear regulators is still developed as in [45] where a feedforward action is proposed to extend the Power Supply Rejection Ration (PSRR) of the converter.

A switched-capacitor regulator switches an array of capacitors to generate the output voltage as presented in Figure 2.5c. By alternatively switching the capacitors array between different configurations, the converter modulates the battery voltage. A 3-to-1 switched capacitor converter is shown in Figure 2.5d. When the switching clock is in phase 2 ('Φ_2' switches are closed and 'Φ_1' switches are open) the three capacitors are in a parallel configuration and the voltage across them equals the output voltage. Switching to phase 1 configuration ('Φ_2' switches are open and 'Φ_1' switches are closed) each capacitor is charged through the R_{on} resistance of the switches to the battery voltage divided by three.

A low switch resistance yields a high charging speed but a high input current spike that requires a high supply decoupling for EMI control. Furthermore most voltage regulation schemes require to sense the voltage drop across a MOSFET. Variable switching frequency regulation can be used to modulate the amount of transferred charge that defines the DC output impedance of the converter as defined in [78, 90]. As a result, the switched-capacitor converter has a variable output impedance that limits its theoretical efficiency to [78]:

$$\eta = \frac{1}{1 + \frac{R_{out}}{R_o}} \tag{2.3}$$

where R_{out} is the DC output impedance of the converter. A multiple step ratio topology is proposed in [56, 78, 90] to extend the converter efficiency. Depending on the required conversion ratio, $\frac{V_o}{V_{bat}}$, the array of capacitors is switched in such a way to achieve the best available efficiency.

The maximum amount of deliverable charge highly depends on the capacitor values and the switching frequency. The higher the switching frequency and the capacitor value, the higher the power handling capability. Few amps to be delivered under a low voltage context requires the use of a high switching frequency as well as large capacitors. Nowadays such a design is not feasible with the required efficiency. Nevertheless this power conversion principle is a promising path toward full integration of the power converter [56, 93].

An inductive based regulator principle is represented in Figure 2.5e. The converter switches an array of passive elements made up of inductive and capacitive elements. Free-wheeling diodes are also used to avoid current discontinuities in the inductor that can lead to the system destruction. Researches for on-chip integration of passive components are presented in [10, 50]. For maturity reasons only external passive components are considered in this thesis **despite recent advances [10]**.

A common step-down buck regulator is presented in Figure 2.5f. An inductor and a capacitor form the passive network that is switched to the battery voltage by a P-MOSFET transistor while the N-MOSFET one is used as a free-wheeling diode. By alternatively switching the inductor to the battery voltage or to the ground, the output voltage is regulated thanks to the use of a control loop that generates switching control signals. If the power components are assumed to be ideal, the absolute limit efficiency is 100%. Thus inductive-based regulators are best suited when a high efficiency over a wide load range is mandatory and are widely used across semiconductor manufacturers for digital supply.

Combinations of linear and switched converters are presented in [20, 98]. Depending on the power requirement of the processor, the most efficient conversion topology is used to supply the load with respect to the instantaneous required current. However this solution requires the use of multiple redundant external components.

The following covers the control part of a single phase, step-down buck converter.

Hard switching scheme associated to a conventional switching frequency of a few MHz is preferred over a high frequency, zero-current or zero-voltage switching scheme for compatibility with existing power stage and passive components as proposed in [7]. Moreover no added resonant component is required that maintains the internal (on-chip) or external (on-board) solution area low along with a high efficiency [7, 29].

3.3 Inductive step-down converter control

Numerous control strategies coexist to supply digital embedded cores. However they are mainly derivatives of a few ones. First of all, the voltage-mode PWM is one of the most commonly used despite its complexity in modeling and control. The whole controller is integrated on-chip thanks to the passive integration capability of the CMOS process. Since it is the standard regulation methodology used by ST-Ericsson during this thesis, it is widely developed bellow.

The current-mode control strategy derives from the voltage-mode PWM one by the addition of an inner current loop. This secondary loop allows to achieve better load and line transient performances. As a drawback the modelling difficulty increases as well as the design one, especially with the current sensing at high frequency. Since these two control strategies use a clock synchronized modulation, they are considered as ”hard synchronized”, i.e. each cycle is synchronized in phase with respect to the reference clock. On the contrary, strategies where a conduction cycle can start out of phase with respect to a reference clock are considered as ”soft synchronized”.

Free-running topologies based on sliding-mode control are also widely used for core supply converters. Sliding-mode control is used to increase the transient performances of the converter. Direct output-voltage ripple control as well as enhanced ripple control are structurally asynchronous since their switching frequency varies in an uncontrolled but predictable manner. That behaviour is no longer an issue when the converter is used in an ATX desktop computer where the input and output voltages are closely bounded. However it leads to a wide switching frequency range when the controller is embedded into a platform. This is the result of a large possible battery voltage range as well as output voltage range. This variation prevents to maintain a good efficiency over the whole operating range. Furthermore when dealing with sliding-mode based converters,

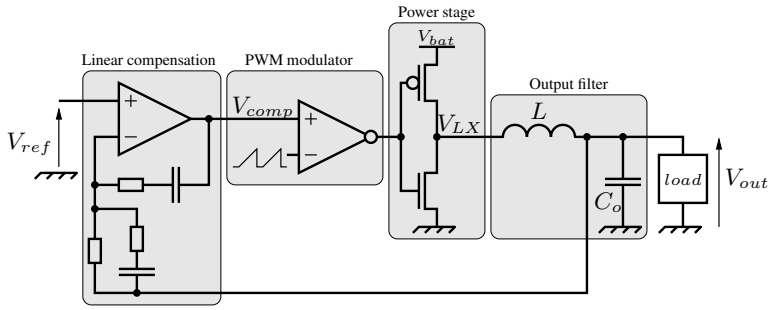


Figure 2.6 – voltage-mode controlled PWM converter - principle schematic

the standard average linear analysis does not provide sufficient insight to correctly determinate the stability of such a converter. Thus the sliding-mode theory is generally used to deal with this task. Free-running sliding-mode topologies are detailed in this chapter.

Synchronizations of a sliding-mode based controller have been proposed. It often leads to a control similar to a current-mode control, i.e. like most of the hard-synchronized structures. The soft-synchronized ones keep the intrinsic asynchronous nature of the sliding-mode controller. Synchronization proposals are also reviewed in this chapter in order to determine which way is preferable to synchronize a sliding-mode converter in the context of a battery-supplied platform.

4 PWM converters

4.1 Voltage-mode control

A voltage-mode controlled PWM buck converter is presented in Figure 2.6. A power stage formed by two complementary P and N MOSFETs switches the battery voltage, V_{bat}, to form a square wave. The filter formed by L and C_o shapes the square wave AC component and provides its average value to the load. Due to the finite amount of AC-component attenuation, a small AC ripple remains on the output voltage.

The power part is not sufficient to provide a regulated voltage within the specifications required to supply a high performance DB. Thus a control-part is associated to provide a power-stage input control signal, i.e. a duty cycle which depends on output

signals (feedback) and input signals (feedforward). Considering a voltage-mode PWM converter, the control part is built around a PWM modulator whose input is a linear compensation function as presented in Figure 2.6. The output of the modulator is directly fed to the power stage that switches the output external filter. Power MOSFET drivers are not represented nor the switching logic glue.

A model of the converter has to be defined in order to determine the linear compensation function. Since the power part characterization is outside the scope of this thesis, the power stage and output filter characteristics are assumed to be known. The methodology used is the small-signal AC characterization associated to phase-margin and gain-margin criteria. Widely used in conventional design, some limitations have been outlined in [113]. However this methodology offers a good "first-step" and provides sufficiently accurate results to properly model the converter behaviors.

4.1.1 Control-to-output model

PWM modulator signals are represented in Figure 2.7. The input signal is compared against an internally generated sawtooth and the output signal has a duty cycle proportional to the input signal. The higher the input signal, the wider the output pulse. A small change in the compensation voltage, $\hat{v}_{comp}$, induces a small change in the duty cycle, $\hat{d}$, as represented in Figure 2.7. The constant slope characteristic gives:

$$\frac{V_H}{T} = \frac{\hat{v}_{comp}}{\hat{d}T} \tag{2.4}$$

where V_H is the height of the ramp and T the ramp period. The small signal average increase in the power stage output voltage, $\hat{v}_{LX}$, with respect to a small change in the duty cycle is:

$$\hat{v}_{LX} = \hat{d}.V_{bat} \tag{2.5}$$

Using the two previous results yields:

$$\frac{\hat{v}_{LX}}{\hat{v}_{comp}} = \frac{V_{bat}}{V_H} \tag{2.6}$$

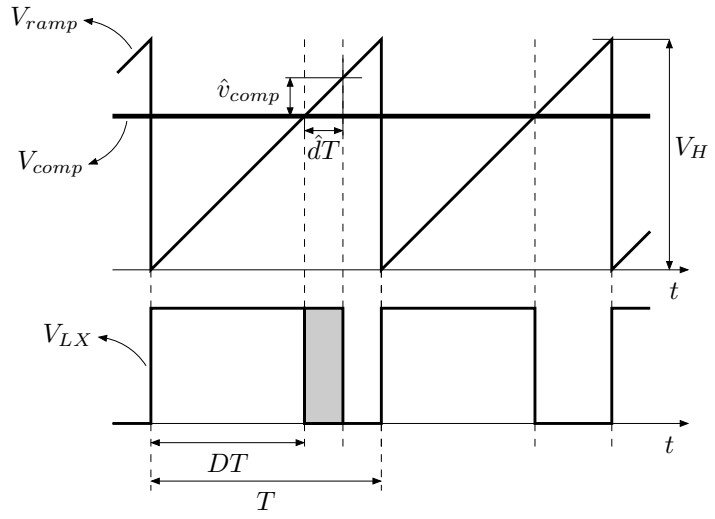


Figure 2.7 – voltage-mode controlled PWM converter - main waveforms

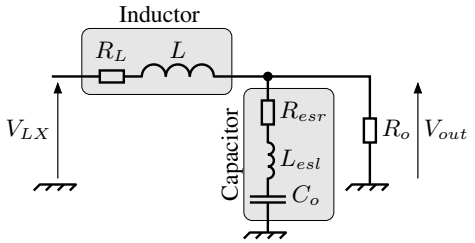


Figure 2.8 – Buck converter output filter model

The PWM modulator associated to the power stage can be modeled by a single gain. Using feedforward action on the power input voltage, the sawtooth height V_H can be adjusted to V_{bat}. Doing so, the PWM modulator and power stage gain become an unitary gain. This technique is commonly used to reduce the line-to-output sensitivity as well as simplify the compensation function design.

The considered output filter model for simulation is presented in Figure 2.8. The inductor and capacitor first order parasitic elements are represented. R_L is the equivalent serial resistance of the power inductor or Direct Current Resistor (DCR), R_{esr} and L_{esl} are respectively the capacitor equivalent serial resistor and inductor. These two parasitic elements mainly depend on package when small ceramic capacitors are used [87].

The capacitor resonance frequency is kept close to the switching frequency in order to maintain the output voltage ripple at acceptable levels. Thus capacitor parasitic

elements can be neglected since the small-signal analysis validity domain is limited to frequencies well below the switching frequency. Then the filter linear transfer function is:

$$\frac{V_{out}\left(s\right)}{V_{LX}\left(s\right)} = \frac{R_o}{R_o + R_L} \frac{1}{1 + \frac{L+R_L R_o C_o}{R_L+R_o} s + \frac{L R_o C_o}{R_L+R_o} s^2} \tag{2.7}$$

The inductor DRC is more than ten times below the output equivalent resistance in order to keep the efficiency high. Thus in a first step it can be neglected such as:

$$\frac{V_{out}(s)}{V_{LX}(s)} = \frac{1}{1 + \frac{L}{R_o} s + L C_o s^2} \tag{2.8}$$

when compared to a second order filter standard form:

$$H\left(s\right) = \frac{1}{1 + 2\xi \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \tag{2.9}$$

the characteristic frequency of the filter and the damping factor can be expressed as:

$$\omega_0 = \frac{1}{\sqrt{L C_o}} \quad , \quad \xi = \frac{1}{2R_o} \sqrt{\frac{L}{C_o}} \tag{2.10}$$

The combination of (2.6) and (2.8) gives the control-to-output transfer function:

$$\frac{V_{out}(s)}{V_{comp}(s)} = \frac{\frac{V_{bat}}{V_H}}{\frac{s^2}{\omega_0^2} + 2m \frac{s}{\omega_0} + 1} \tag{2.11}$$

Assuming a feedforward action on the PWM-modulator rising slope, the gain of the plant can be neglected. Then the plant model is a second order system whose damping factor is load-dependent. The damping remains uncontrolled and its range of values is wide when considering a high-end microprocessor as previously mentioned. Subsequently the linear compensation function has to provide key characteristics:

- A high DC-gain to diminish the static output error (or increase the DC-accuracy). This gain is provided by an integration action.
- Two zeroes to compensate the filter double pole.
- A wide small-signal bandwidth to provide large transient satisfying performances

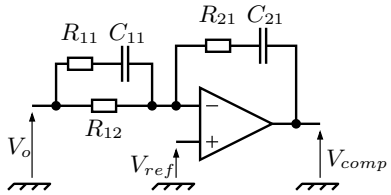


Figure 2.9 – Type-3 (or PID) compensation implementation using a voltage amplifier

Moreover the compensation function is designed in order to set the cut-off frequency five to ten times below the switching frequency. This widely used trade-off is set in order to average the switching effects while maximizing the regulation speed.

4.1.2 Type-3 linear compensation function

The previously described linear function is generally called "Type-3" (or PID) compensation function. A possible implementation is drawn in Figure 2.9. This implementation provides the above-mentioned integration action and zeroes plus two additional poles. One pole is determined by the limited phase boost provided by R_{11} and C_{11} and the second pole by the limited bandwidth of the amplifier. In order to compensate the power plant whose model is defined by (2.11), the compensation function is designed such that:

- The two zeroes are set at LC double pole
- A high frequency pole is set at the capacitor ESR zero
- The other high-frequency pole is set at the switching frequency or higher
- The integral pole is set to provide an open-loop bandwidth five to ten times lower than the switching frequency

This methodology for stability suffers from approximations. First the switching action is obviously non-linear. The open-loop bandwidth has to be an order of magnitude below the switching frequency to ensure the validity of the stability criterion. Second the stability analysis is valid for steady-state analysis only. It does not prevent from large scale instabilities that can result from a large output transient. Last but not least, it does not prevent from period doubling or chaotic behaviors as described in [113].

4.1.3 Output impedance

Quantifying the output transient performances is mandatory to benchmark different solutions when supplying a highly variable load such as a digital core. Undershoot and overshoot measurements using a generated current-step load-pattern is a common test vector. Unfortunately a digital core may introduce repetitive load patterns such as constant frequency pulses in which the harmonic content is different from a single step. Thus a frequency based transient performance criterion is required.

The output impedance aims to characterize the converter behavior when a small and repetitive output transient occurs. A small change in the output current yields a small change in the output voltage. The resulting output impedance is defined as:

$$Z_o(s) = \left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{ref}(s)=0,\hat{v}_{bat}(s)=0} \tag{2.12}$$

Without control the buck open-loop output impedance is simply the parallel combination of the passive output network [29, 94]:

$$\begin{aligned} Z_{o_{OL}}(s) &= R_o \parallel \frac{1}{C_o s} \parallel (R_l + Ls) && (2.13)\\ &= \frac{R_l R_o}{R_l + R_o} \frac{1 + \frac{L}{R_l}s}{1 + \left(\frac{L}{R_l+R_o} + \frac{R_l R_o C_o}{R_l+R_o}\right)s + \frac{R_o L C_o}{R_l+R_o}s^2} && (2.14) \end{aligned}$$

where R_o is the equivalent linearized load. Note that contrary to [29, 94] the inductor DRC is taken into account. The open-loop impedance exhibits a peak at the filter self-oscillation frequency that can degrade the load. A proper feedback control aims to divide the output impedance by its gain such as:

$$Z_o(s) = \frac{Z_{o_{OL}}(s)}{1 + T_{comp}(s)} \tag{2.15}$$

where $T_{comp}(s)$ is the compensation function. Thus a high DC gain feedback is best suited to compensate the uncompensated DC drop caused by the DRC and the power stage resistivity. The amount of high frequency gain, i.e. the compensation bandwidth, to apply to the feedback controller is more difficult to evaluate. One can consider that in-

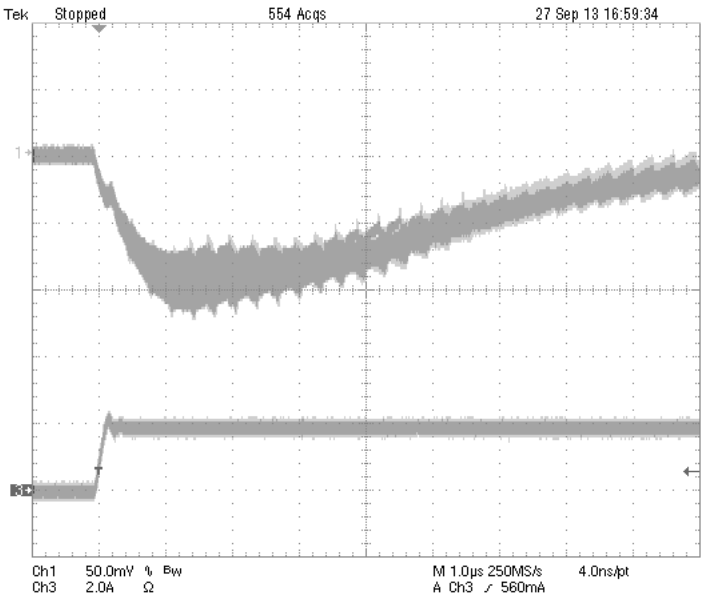


Fig. 2.10 – Load step-response of a general purpose voltage mode controlled PWM converter, up: output voltage (AC coupled), down: load current

creasing the controller bandwidth even within the switching frequency limit is sufficient to diminish the output impedance of the converter. Unfortunately such an approximation is no longer valid when supplying a digital core, due to the current slope limitation in the inductor. Because of the low supply voltage required by the digital core, the falling slope of the inductor current is strongly limited. Assuming a large but reasonable and high-frequency sinusoidal or square load may issue a strong current distortion in the inductor. Then the linear model is no longer valid and the converter seems to be unstable. To solve this issue the designer has to diminish the bandwidth of the controler or to lower the inductor value.

Furthermore sampling increases the transient variability as represented in Figure 2.10. The voltage response varies depending on the phase of the converter when a transient occurs. If a load transient occurs at the beginning of the conduction cycle the converter reacts as fast as allowed by the feedback loop. On the contrary if a load transient occurs at the beginning of the second sub-cycle, i.e. when the V_{LX} node is tied to the ground, the converter wait the beginning of the next conduction cycle to react. This behavior leads to a non negligible variability in the load transient response what reinforces the required performances to comply with worst case test vectors.

4.2 Current-mode control

A current-mode controlled PWM buck regulator is presented in Figure 2.11. An inner loop is used to regulate the inductor current while an outer loop regulates the output voltage. The represented current loop is a ”peak-current” type loop, where the inductor positive peak current is regulated. Other loop types exist such as ”valley-current” where the inductor negative-peak current is regulated or the average current. A peak-current loop works as follows: when the clock cycle starts, the clock rising edge sets an RS-type or a D-type flop, the V_{LX} node is tied to V_{bat} and the inductor current starts to rise. An artificial slope is sometimes added to the measured current and compared against the loop input voltage, V_{comp}, to stabilize the converter when the duty cycle is greater than 50%. A larger control voltage implies a larger inductor peak current that results in an larger average inductor current. Since the inductor current is regulated, the resulting current-loop can be considered as a voltage controlled current source. Then the output filter is now a first order system with a single pole formed by the output capacitor that is much easier to stabilize [34].

The line-to-output characteristic or line-perturbation rejection of the converter increases as a change in the battery voltage is directly reflected by the inductor current. Furthermore the control of the inductor current and the resulting unique output pole removes the peak response of the LC output tank that is responsible for the low performances of a voltage-mode controlled PWM converter. As a result a properly designed current-mode converter exhibits a wider regulation bandwidth and a lower output impedance.

The main issue when designing current-mode control is to sense the inductor current with a sufficient bandwidth. This issue becomes significant with the increase in the switching frequency and the output current. A common solution that preserves the converter efficiency is to sense the voltage drop across a switch [14]. Unfortunately a high current power stage presents a low drop and resistivity that requires a high current sense gain. Furthermore a few MHz switching frequency requires a sensor of much higher bandwidth and accuracy that is difficult to obtain [107]. Therefore a suitable current-sense amplifier needs a large and constant gain over a wide bandwidth that is not suitable for CMOS process integration.

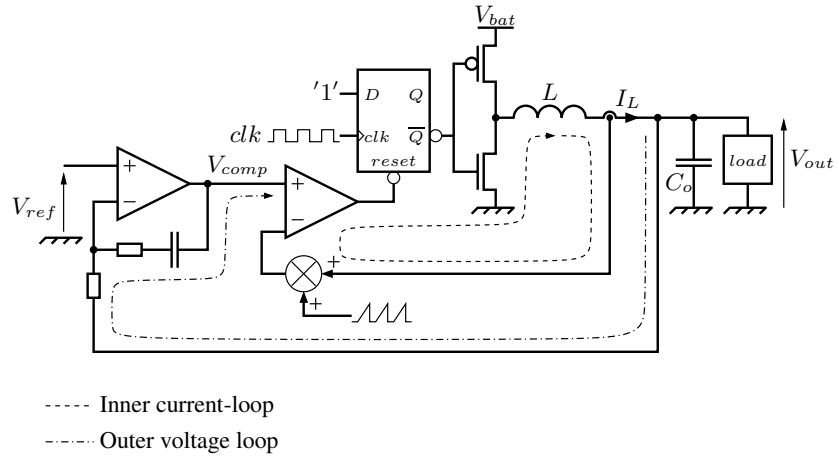


Figure 2.11 – current-mode PWM converter - simplified diagram

5 Voltage Sliding-mode and hysteretic regulators

Limitations of linear based control of a DC/DC converter make these solutions unsuitable when considering the trends of mobile device power ecosystem. First because of the difficulties to reduce the output filter of a voltage mode controlled PWM converter. Second because of the lack of fast and power friendly solution for current sensing in a current-mode controlled PWM converter. This thesis started with the simple observation that PWM control is a dead-end for single phase mobile ecosystem. To circumvent the limitations of linear-based analysis and design of DC/DC controllers, the simplest approach is to start from the other side of control theories, i.e. from the non-linear approach.

5.1 Ripple-based sliding-mode regulator

A common voltage-mode ripple-based regulator is shown in Figure 2.12. The output voltage is directly fed-back to the negative input of a comparator with an hysteresis cycle. Due to the presence of the hysteresis cycle, this control is usually called hysteretic control. When the output voltage hits or is below the required voltage, V_{ref}, minus a small offset, $\frac{\Delta V_h}{2}$, the V_{LX} node is pulled to V_{bat} otherwise when the output voltage hits or is above the required voltage plus a small offset, the V_{LX} node is tied to the ground. The passive filter remains as previously mentioned. An inductor L with an equivalent

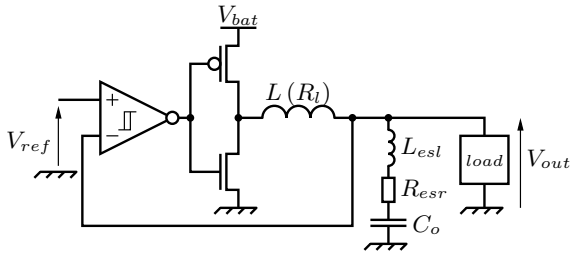


Figure 2.12 – ripple based hysteretic regulator - principle

DC resistance, R_L, feeds the DC current to the output load while a capacitor, C_o, with an equivalent serial resistance, R_{esr}, and an equivalent serial inductance, L_{esl}, filters the AC current.

In order to achieve stable operation, the output voltage must evolve within the limits defined by the reference voltage and the hysteresis cycle. To comply this requirement the converter has to directly converge toward the bang-bang threshold. For instance when the output voltage, V_o, hits the low limit, $V_{ref} - \frac{\Delta V_h}{2}$, the switching node voltage is pulled to V_{bat} and the inductor current rises. The output voltage, V_o, must directly rise to reach the high comparator limit, $V_{ref} + \frac{\Delta V_h}{2}$. This means that the passive filter dynamic is the one of a first order system compatible with the desired switching frequency and a large ESR is preferred as cited in [12, 16, 19, 27, 36, 51, 81, 104, 119, 122]. Only small multilayer ceramic capacitors (MLCC) are used as output capacitors in handset devices and unfortunately the equivalent serial resistance of these components is negligible. The capacitor has only two operating regions: the low-frequency region where it is mostly capacitive and the high-frequency region where the capacitor is mostly inductive [52]. Thus the output filter is equivalent to a second order LC filter in low frequency and a gain otherwise. To get round this issue, a small resistor can be serially added to the output capacitor at the expense of an increase in the solution price, area and losses [101, 122]. In [48] the sliding-function is a linear function of the output voltage. The error amplifier bandwidth is high (100MHz) to allow a fast switching frequency. Such an amplifier would be too power consuming and too slow to restart when fast wake-up is required.

A voltage-mode ripple regulator suitable to supply a modern digital core requires to operate with few mV ripple. This leads to a very difficult design issue with the design of a small but precise hysteresis cycle in the comparator. Furthermore, the noise immunity

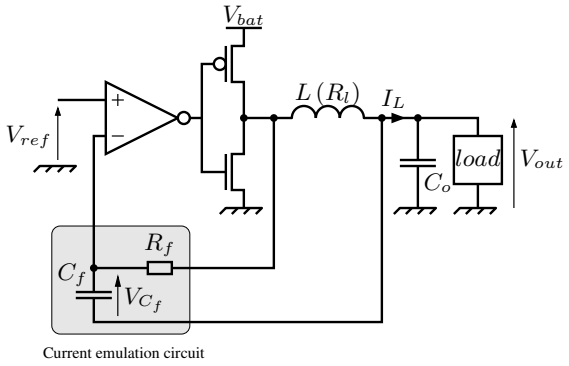


Figure 2.13 – current-mode sliding-mode converter - simplified diagram

of the whole solution is kept low by the requirement of a small output ripple.

5.2 Current-mode sliding-mode controller (CMSM control)

Many studies have been proposed to overcome the stability and noise immunity limitations of the ripple-based voltage sliding-mode controller under low output ESR condition. This approach converges with the theoretical sliding-mode approach by the use of a sliding function that mixes the output voltage and the inductor current. Represented in Figure 2.13 this control structure is simply called ”hysteretic regulator” or ”hysteretic PWM regulator” [11, 12, 44, 69–71, 83, 89, 110] and described as a way to increase the useful ripple. However the added RC network integrates the voltage across the inductor and produces a scaled representation of the inductor current [49]. The passive resistor can be replaced with a transconductance amplifier as in [79]. Thus ”current-mode sliding-mode converter” or ”hysteretic current mode converter” are more explicit descriptions of this control scheme [65, 125].

The inductor current ripple is equivalent to the output capacitor current since the output voltage is kept quasi-constant thanks to the output capacitor. Thus an other way to achieve current mode sliding-mode control is to measure or emulate the current through the output capacitor, C_o, as proposed in [16, 26, 53, 66, 84, 109, 124].

Considering the converter in Figure 2.13, the current-to-voltage transfer function of

the current emulation circuit made up with R_f and C_f is [49]:

$$\frac{V_{C_f}(s)}{I_L(s)} = R_l \frac{1+\frac{L}{R_L}s}{1+R_f C_f s} = R_L \frac{1+\tau_l s}{1+\tau_c s} \tag{2.16}$$

where R_L is the inductor equivalent series resistance, τ_l the inductive branch time-constant and τ_c the capacitive branch time-constant. The converter slides along a sliding surface S that can be expressed by zeroing the comparator input error and input error dynamics:

$$S(s) = V_{out}(s) + R_l \frac{1+\tau_l s}{1+\tau_c s} I_L(s) - V_{ref} = 0 \tag{2.17}$$

When considering a single conduction cycle, the observer becomes a single gain K_{obs} (i.e. the slope gain) since the two time-constants are larger than the switching period. Writing $i_L = I_L - I_o$, i_l being the AC current component in the inductor, this assumption yields:

$$S(t) = V_{out}(t) + R_l I_o(t) + K_{obs} i_L(t) - V_{ref} = 0 \tag{2.18}$$

Ideal sliding-mode operation implies that the converter switches with an infinite frequency in order to minimize the instantaneous error voltage. This chattering phenomenon is extensively described in [116]. A too high switching frequency is not suitable for power converters due to the switching losses. In practice the effective switching frequency of a sliding-mode converter is limited by delays in the control loop and finite switching speeds.

Neglecting the ripple in the inductor and averaging the converter behavior gives a simple model:

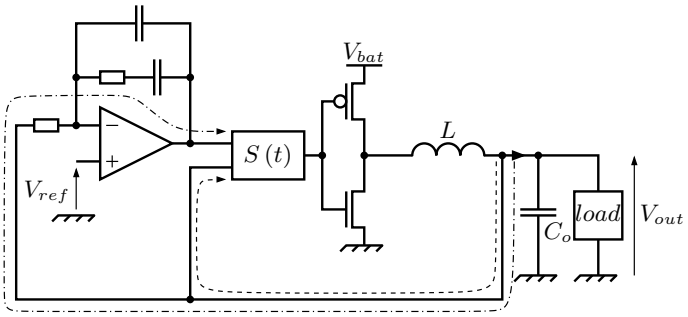
$$\overline{V}_{ref}(t) = \overline{V}_{out}(t) + R_l \overline{I}_o(t) \tag{2.19}$$

where $\overline{X}$ is the average value of X. It is obvious that the DC output impedance of the converter is non-negligible since the output voltage is load-dependent. This drop is used to perform so-called Adaptive Voltage Positioning (AVP) in [11, 30, 44, 65, 66, 69, 80]. Unfortunately the DRC value is highly inaccurate especially when the coil value and reference is subject to frequent changes due to the customers' choices [85]. Furthermore it is most of the time too high to be used to determine the amount of AVP suitable for the application. **A solution to control the amount of AVP is proposed in [80].**

5.3 V^2, quasi V^2 and V^2IC converters

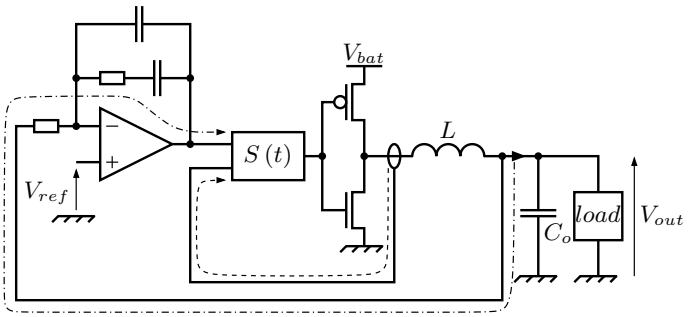
A high DC-gain compensation function can be added in order to get round the finite and unpredictable DC output impedance of the CMSM converter. The previous described topology is used to provide a fast transient response while the output compensation function improves the converter accuracy. This operation principle is proposed with or without synchronization in [3, 12, 19, 26, 27, 30, 31, 49, 51, 52, 65, 66, 81, 85, 89, 101, 104, 109–111, 119, 124] with "quasi V^2", V^2IC or V^2 term. A V^2 converter uses the output voltage in an accurate and slow loop in parallel with a fast loop that uses the output voltage ripple as represented in Figure2.14a. An enhanced or quasi V^2 converter is represented in Figure 2.14b. It uses the output voltage in an accurate and slow loop too but the inductor current is inserted in a fast loop. The fast loop of a V^2IC, that is presented in Figure 2.14c, uses the output capacitor voltage ripple. Despite these differences in the study approach, these converters are almost similar in essence. The main difference is the place where the fast varying signal is sensed. From a control point of view, it means that the sliding-function uses the output voltage and its derivative value.

The output voltage ripple is kept small so that a V^2 topology is unsuitable for integration due to the above-mentioned noise immunity and stability issues. Furthermore the output capacitor current reconstruction is difficult when the total amount of output capacitor is unknown and subject to change. Thus an inductor-current based strategy appears to be the most suitable solution when dealing with the mobile ecosystem. A more detailed operation principle of the enhanced V^2 converter is detailed in the following chapter. Models and design procedure are proposed. Control of a V^2 controller remains an important field of investigation for fully integrated converters where the passive components are known in value.



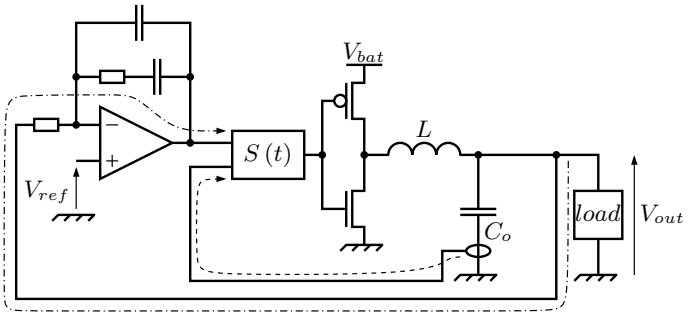
------ Fast loop
-·-·- Slow loop

(a) V^2



------ Fast loop
-·-·- Slow loop

(b) Enhanced V^2



------ Fast loop
-·-·- Slow loop

(c) V^2IC

Figure 2.14 – V^2, Enhanced V^2 and V^2IC converters principle schematic

6 Frequency control of a sliding-mode converter

6.1 Hard synchronization paradigm

The converter is considered to work in Hard Synchronization mode (HS mode) when each cycle is started by a reference clock. This synchronization paradigm does not allow asynchronous response but offers a better control of the generated EMI.

A first solution for phase synchronization in sliding-mode control is to use a RS or D-flop synchronization scheme to force each cycle as proposed in [2,26,81,84,89]. The reference clock starts the cycle by setting the flop in a positive state and the pulse is generated until the sliding function is reached. When the hitting condition occurs, i.e. the sliding-function reaches zero, the flop changes its state until the next clock change occurs. This operation mode is called ”Fixed frequency sliding-mode control” in [84] and ”Constant-frequency peak (or valley) voltage ripple regulator” in [89]. Nevertheless this synchronization scheme converts the sliding-mode controller into a current-mode like control with the drawback to require a significant slope compensation or a complex system to switch between peak and valley modes depending on the conversion ratio as proposed in [84]. Furthermore the intrinsic sliding-mode asynchronous transient response is transformed into a current-mode synchronous transient response.

A slope compensation circuitry has been proposed and patented during this thesis and a detailed analysis of its operating principle as well as the slope compensation requirement is given in [62]. The use of this compensation scheme does not provide a real breakthrough compared to a classical current-mode control. The only difference between this solution and a conventional current-mode control is the use of an observer-based current-sense instead of a direct measurement and a variable gain in the observer that increases slightly the transient response.

A hard synchronized converter is mandatory when the output spectrum has to be precisely controlled or when the application requires specific cases where reaching a controlled frequency with a free-running base approach is not feasible. Audio applications with a highly harmonic load can suffer from carrier frequency modulation as well as RF applications in which the switching harmonics have to be controlled. When dealing with digital core power supply, things are very different. The output voltage has to

be accurate and quickly modulated but no particular spectrum of the supply voltage is required.

In [2,12,44,85,89,102,111] the sliding function is modulated by a clock-synchronized ramp at the targeted switching frequency. Nevertheless such a circuit remains inaccurate and is not suitable when the reference voltage has to be kept away from pollution as in a complex AB. On the transient performances side, the higher the sliding-function modulation, the lower the sensibility of the converter. If the sliding-function is highly modulated, the transient has to highly impact the voltage error to produce a modulation variation, otherwise the duty cycle will not noticeably change and the perturbation will not be quickly rejected.

6.2 Soft synchronization: Compensated frequency control

In order to keep the advantage of asynchronous response, [2, 15–18, 23, 30, 51, 89, 122] propose to use the converter with a Constant On-Time or a Constant Off-Time (COT) configuration. When the converter hits the sliding surface, the switch connected to battery voltage is activated for a defined amount of time (On-Time of the switch connected to the battery). The switch connected to the ground is activated for a defined amount of time (Off-Time) respectively. The switching frequency is kept quasi-constant by adjusting the On or Off-Time using feedforward operation on both input voltage, output voltage and eventually load current as in [51]. A feedforward action on the potentially controllable delays, T_{don}, T_{doff}, or hysteresis cycle, V_{hyst}, based on the measured voltage, can compensate the switching frequency variation since the input voltage and the output voltage are the most prominent external terms in the switching frequency expression:

$$f_s = \left[\frac{V_{bat} V_{hyst}}{(V_{bat} - V_o) V_o} R_f C_f + \frac{V_{bat}}{V_{bat} - V_o} T_{don} + \frac{V_{bat}}{V_o} T_{doff} \right]^{-1} \tag{2.20}$$

In [30] the free-running switching frequency is in the range 500kHz to 3.88MHz with a duty cycle between 87% and 10%. The Adaptive On-Time (AOT) technique achieves a 1.75MHz to 1.98MHz switching frequency range. In [122] the switching frequency range is divided by approximately 7 for a duty cycle in the range 29% to 47%. In [51] the switching frequency varies from 1.05MHz to 0.65MHz without AOT.

Table 2.2 – AOT solutions comparison

Solution	[30]	[122]	[51]
f_{sw} without AOT	500kHz - 3.88MHz	290kHz - 440kHz	650kHz - 1.05MHz
f_{sw} with AOT	1.75MHz - 1.98MHz	395kHz - 410kHz	750kHz+/- 6%
Duty cycle	0.1 - 0.87	0.29 - 0.47	0.29 - 0.36
Δf_{sw} reduction	14.7	10	4.4

Using AOT, the range is reduced down to 47kHz width with a duty cycle that varies from 36% to 29%. These results are summarized in table 2.2.

AOT control is well suited when the converter operates as a stand-alone solution where no clock synchronization is required thanks to a dedicated battery decoupling network. The switching frequency is kept quasi-constant in a controlled band and preserved from unwanted drop in efficiency. The On-Time control degrades the falling transient performances but this can be improved by the use of a Ramp Pulse Modulation (RPM) strategy as related in [89]. Last but not least, the sliding-mode based asynchronous response is preserved.

The drawback that makes a feedforward synchronization based strategy unsuitable for integration in a PMU is the lack of phase synchronization. Instantaneous or average switching phase synchronization of the converters gathered in a PMU is mandatory to reduce the ripple current in the battery and avoid possible interactions between the different DC/DC converters that share the same power line.

6.3 Soft synchronization: Regulated frequency control

A more precise frequency control of the DC/DC switching frequency can be achieved by regulation of the free-running switching frequency. Frequency Locked Loop (FLL) synchronization scheme is proposed in [24, 31, 38, 47, 52, 72, 95, 124] and a principle schematic is given in Figure 2.15a. The natural switching frequency (f_{sw}) of the converter is sensed and converted into a voltage by a frequency-to-voltage converter. The reference clock (f_{ref}) is converted into a voltage which is compared against the observed switching frequency. The resulting error is then amplified and filtered by a compensation function prior to being use as a frequency-control input of the free-running DC/DC

converter. As a result, the whole DC/DC converter is used as a VCO in the frequency loop.

The frequency-to-voltage converters have to be properly matched to avoid unwanted offset in the frequency loop that generates a switching frequency error. The high DC gain provided by an arbitrary compensation function that stabilizes the frequency loop, helps to achieve no voltage error and consequently no frequency error. But FLL synchronization still does not offer phase synchronization effect. The converter would behave as an AOT control with a more accurate switching frequency thanks to the feedback regulation. Nevertheless a FLL synchronized converter requires a dedicated line filter due to the lack of switching phase control.

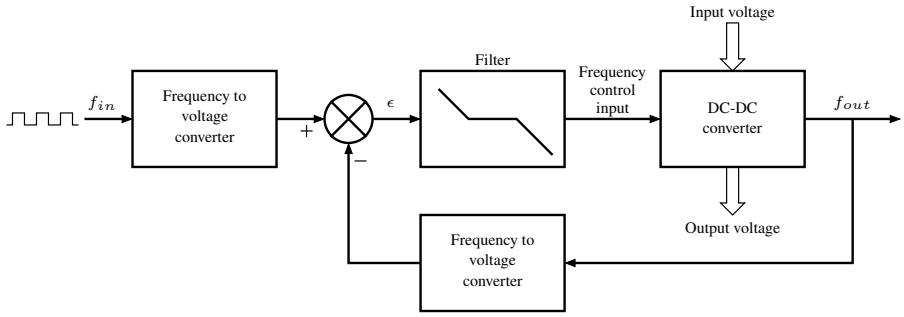
Thus Phase Locked Loop (PLL) synchronization scheme has been proposed in [2, 21, 23, 37, 38, 65, 66, 70, 71, 73, 74, 89, 106, 115, 119] and implemented in silicon in [23, 70, 71, 73, 74, 119]. PLL operation principle is represented in Figure 2.15b. The DC/DC converter operates as an oscillator in the frequency loop. The output phase is compared against the reference clock phase by a Phase Frequency Detector (PFD). The PFD output is filtered out and used to control the oscillator frequency. **In [73] the PLL synchronisation is used in a multi-output converter.**

A negligible phase error implies a negligible frequency error between the desired switching frequency, f_{ref}, and the effective switching frequency, f_{sw}. Moreover it is obvious that no phase error implies that the switching cycles start synchronously in steady state operation. This ensure a good overall phase control while transient operation can start asynchronously.

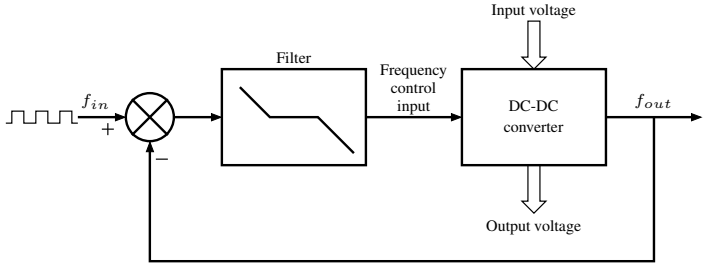
7 Commercial solutions

Low output-voltage solutions suitable for microprocessor supply are widely available across solution suppliers. Because of the unavailability of the data that concern the application specific integrated circuit market, this part focuses on standalone components that use a digital supply oriented control.

LM8801 from National Semiconductor® is a voltage-mode PWM regulator [97]. It switches with a 470nH inductor at 6MHz and reaches 16mV transient response under a



(a) FLL



(b) PLL

Figure 2.15 – Frequency regulated converters

350mA step with a 4.7μF output capacitor. This 600mA step-down converter is sensitive to the output inductor and capacitor values. The efficiency reaches 90% at half the maximum output current.

The replacement part from Analog Devices® (ADP2121) uses a 6MHz voltage-mode PWM control with the same typical output filter [4]. This circuit uses a "*hybrid proprietary voltage mode control scheme*" that is supposed to increase the stability of the converter. Indeed the transient performances are less than the previous proposed component with 25mV transient response under a 150mA step. The peak efficiency is close to 90% and higher than 85% over a wide range. ADP2126/ADP2127 are derivative devices that uses a higher inductor value but a smaller output capacitor. The control part remains the same as well as the performances.

Fairchild Semiconductor® proposes a higher current digitally-programmable converter chip designed to supply digital cores (FAN5365) [96]. This circuit embeds a "*very fast, non-linear control architecture*" that uses a typical 470nH inductor with a 10μF or 4.7μF output capacitor. FAN5361 datasheet [95] gives more detailed explanation about the operation principle of its controller. This chip uses a "*non-linear, fixed frequency*

PWM modulator" and the switching frequency is kept constant thanks to "*an internal frequency loop*". This chip presents a 25mV transient response under a 250mA step while the peak efficiency is above 90%.

A similar component made by Texas Instruments® (TPS6266x [24]), uses a non linear architecture with a FLL type synchronization. This component offers a 50mV transient response under a 600mA load step with a 1μH inductor and a 4.7μF capacitor.

A fair comparison between the aforementioned component is difficult to define because of the wide range of possible operations. First the transient test vector is not standardized in amplitude and rise time. Second a fair comparison must include an output filter size and cost parameter that is highly customer-dependent. In order to be competitive the proposed solution must comply with output filter standards and transient performances. Throughout the followings, the order of magnitudes of the previously cited components are used as references to set proposal.

8 Architecture Benchmark

The published solutions that implement a sliding-mode based control with a synchronization scheme are summarized in Table 2.3. The classical Voltage Sliding-Mode (VSM) is well developed and lot of synchronization schemes have been proposed. Unfortunately this regulation scheme is not suitable when a small output voltage ripple is required. A classic V^2 topology suffers from the same issue of a small output ripple. Since the output capacitor value and reference is subject to change, the V^2IC control is not suitable for an IP design as well as the CMSM topology that suffers from a lack of load regulation.

Thus an EV^2 topology appears to be a good trade-off between a small output voltage ripple and good load regulation. It is obvious when looking at Table 2.3 that the frequency regulation of such a converter is a widely covered topic. But due to the requirement of a global phase synchronization, AOT and FLL frequency controls are not suited for a complex PMUs. The requirement of a transient asynchronous response avoids the use of a simple Flop synchronization even if a cheap and efficient slope compensation mechanism has been proposed in [62]. Reference modulation has been

Table 2.3 – Tentative State-of-the-art classification

	VSM	CMSM	V^2	EV^2	V^2IC
Flop	[47, 89]		[81, 84, 104]	[89, 104]	[3, 26, 27]
Modulated reference	[110]	[44]		[12, 85]	
AOT	[16, 89, 122]			[19, 30, 51]	
FLL	[38, 72]	[125]		[31]	[52, 124]
PLL	[89, 103, 115] [38]	[67, 71] [23, 69, 70]		[14, 65, 66, 119] [21, 106]	

discarded because of accuracy issues.

Fixed-frequency voltage-mode PWM control is now mature and well documented. But it appears difficult to increase the transient response performance without impacting the stability. The high frequency gain of the compensation function that is required to obtain good transient performances degrades the stability as well as the noise margin. Then the IP is highly sensitive to ground planning and requires complex noise filtering. Increasing the switching frequency may help to reduce the apparent noise gain by pushing the noise frequency upwards where the amplifier cannot provide a sufficient gain. However this degrades the efficiency with an increase in the switching noise, especially when a large power stage is needed due to the high output current. An increase in the power stage size and switching frequency leads to a higher current sense complexity that makes a current-mode regulation unsuitable for supplying a large varying digital core.

These reasons explain the necessity of a sliding-mode but synchronized converter. The EV^2 control with phase-locked-loop seems to be the most suited topology to perform fast transient response, good accuracy, high efficiency and low noise operation if the penalty in silicon area is reasonable. This operation principle is proposed in [14, 21, 65, 66, 106, 119] with the use of a variable hysteresis cycle to control the switching frequency.

9 VCO operation of a sliding-mode converter

(2.20) outlines the prominent terms that define the free-running switching frequency of a CMSM loop. It is obvious that no change can be operated on the battery voltage and the output voltage to regulate the switching frequency. Therefore the switching frequency control can be performed by the use of the comparator input voltage hysteresis cycle and the commutation delays in the loop, respectively, V_{hyst}, T_{don} and T_{doff}. The use of each parameter is now detailed.

9.1 Hysteresis voltage control

Hysteresis cycle modulation is used in [2, 12, 12, 14, 37, 38, 47, 52, 65, 66, 75, 106, 122, 124, 125]. Two comparators and a small logic glue are used to perform an equivalent variable hysteresis comparator in [37, 47, 124]. This solution requires the use of two matched comparators and a circuitry to generate the up and down reference voltages that define the sliding-domain.

A complex hysteresis cycle generation is proposed in [122]. It performs feedforward action on the hysteresis cycle but requires a lot of amplifiers and comparators. The added silicon area and power consumption makes this solution unsuitable for a low power control.

Variable positive feedback is the solution used in [12, 52, 106, 125]. Modulating the rate of positive feedback applied to a standard comparator is a suitable way to control the amount of hysteresis cycle. It is a cheap solution that does not require a high biasing current.

When dealing with the design of a CMSM inner loop, the emulated current amplitude voltage is generally small, and so is the required hysteresis cycle. A small and variable hysteresis cycle yields to major design issues.

9.2 Time delay control

Time-delay modulation is proposed in [69–71, 103, 115]. A fast comparator drives a variable delay chain. The delay is adjusted to set the free-running switching frequency.

This method requires the use of a fast comparator that will be delayed by added power consuming elements.

A more power efficient method is to lower the speed of a medium speed comparator. Such a solution would require less silicon area since there is no added delay element and a lower biasing current because of the lower required speed. Furthermore dynamic biasing complexity is reduced as well and the same voltage comparator can be considered to perform continuous conduction mode and discontinuous conduction mode.

10 Discussion, wrap-up

This state-of-the-art gathers numerous works that deal with innovative controllers for power supply. By mixing the constraints of a handset device requirements becomes more stringent. Thus a lot of solutions are proposed to overcome the existing and well known limitations of classically controlled converters. Most of the limitations cited are sliding-mode oriented with an analog-type non-linear controller.

The three-loop architecture is not the most popular control way perhaps due to its complexity. Mixing a current-mode like controller and a phase-loop engenders unpredictable cross interactions that were not covered before (assumption of the non interaction criterion). A gap between the design and the modeling approach has to be covered in order to obtain predictable performances and a better understanding of the possible cross interactions between the three loops. Last but not least the implementation of a three-loop converter with a low power and silicon friendly VCO solution is still a large uncovered topic. The following issues are considered in the synthesis of the proposal covered in the thesis:

- Equivalent or better transient performances than the conventional voltage mode PWM converter with the smallest possible output capacitor
- Able to handle a lower coil value (lower than 1μH for 3 to 6MHz range)
- Fully integrated controller (active parts)
- Controlled switching frequency and phase, in the range 3 to 6MHz

- Analog and very low power design to obtain a satisfying peak efficiency ($> 80\%$) and efficiency flatness over a wide range of output power

Chapter 3

Proposed Solution

When supplying a microprocessor the designer focuses primarily on the current capability of the converter and the load transient characteristics. As seen previously a modern processor is mainly a dynamic load in which the DC characteristic is lumped in with the rest of the system. Thus a sliding-mode approach looks to be well suited for supplying a high demanding core. Asynchronous transient operation is preferred to diminish the transient phase dispersion effects with respect to the converter switching phase. With its two-loop architecture, an EV^2 architecture provides fast transient response thanks to its internal loop while maintaining a good DC accuracy thanks to the external voltage loop. By the addition of a frequency control solution, the converter achieves a synchronized switching frequency that is suitable to supply a digital core in an embedded platform.

In order to design a high current, single phase solution, the value of the inductor has to be selected in line with the technological manufacturing requirements and a sufficiently low switching frequency in order to minimize the switching losses. Furthermore a design methodology and associated models have to be defined to permit continuous development in an IP[1]-driven environment. Thus an EV^2 controller synchronized by the mean of a PLL design is proposed here. According to the chosen design methodology, top specifications are confronted to the architecture and developed into sub-level blocks until the CMOS front-end.

[1] Intellectual Property

1 Voltage regulation loops

1.1 Operation Principle

The proposed quasi-V^2 converter without synchronization loop is presented in Figure 3.1. As in the current-mode sliding-mode converter, the passive network formed by R_f and C_f integrates the voltage across the inductor to produce a scaled representation of the inductor current I_L. This representation is only pertinent in AC since the current-to-voltage transfer function is defined by (2.16) page 33. Note that the inductor model used here neglects some effects:

- the fabrication uncertainties
- the saturation in the core material that leads the real inductance value to drop under high inductor current.
- the AC equivalent resistance that is higher than the DC one
- the quality factor that makes the coil no longer inductive at high frequency

These uncertainties may lead to a non negligible shift between the two time-constants however an approximate setting of τ_C equal to τ_L can be sufficient to complies with the target as explained bellow. An outer loop integrates the output error to produce a compensation voltage, V_{comp}. An operational amplifier is used in an integrator configuration, the integral time-constant has the common expression:

$$\frac{V_{comp}(s)}{V_{ref} - V_o(s)} = \frac{1}{R_i C_i s} = \frac{1}{\tau_i s} \tag{3.1}$$

From a qualitative point-of-view the inner loop regulates the fast transient operation. When a load positive-step transient occurs, the resulting undershoot is fed-back to the negative input of the comparator through the current emulation capacitor (path 1 in Figure 3.1). As a result the comparator error, ϵ, increases suddenly and the power stage switches On if it is in Off-state, or keeps in On-state otherwise. Under a negative-step transient, the starting overshoot is fed-back through the capacitor, C_f. The comparator input error diminishes and the power stage ties the node V_{LX} to the ground if required.

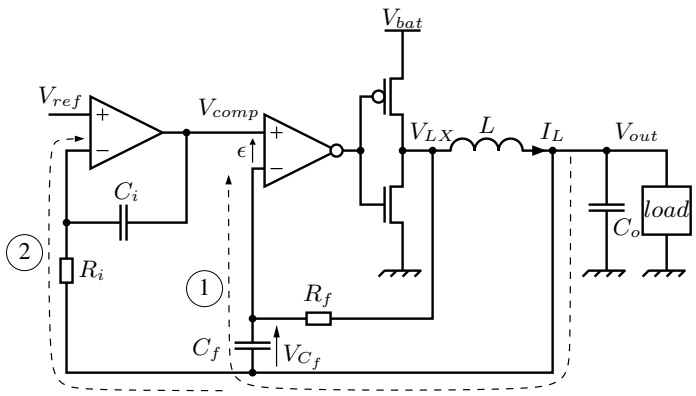


Figure 3.1 – Quasi-V^2 converter - simplified diagram

Since the fast transient regulation is mainly performed by the inner loop, the bandwidth of the outer loop (path 2 in Figure 3.1) can be relatively small compared to a voltage-mode PWM compensation function.

The comparator makes the inner loop DC feedback voltage, $\overline{V}_{C_f} + \overline{V}_o$, equal to the requested DC compensation voltage, $\overline{V}_{comp}$. The inner-loop feedback voltage is the DC value of the power-stage output voltage, $\overline{V}_{LX}$, such that:

$$\overline{V}_{comp} = \overline{V}_{C_f} + \overline{V}_o = \overline{V}_{LX} = R_l\overline{I}_o + \overline{V}_o \tag{3.2}$$

Using a high-gain amplifier with a DC-gain A_0 gives:

$$\overline{V}_o = \frac{A_0}{A_0 - 1}\left(\frac{R_l\overline{I}_o}{A_0} + \overline{V}_{ref}\right) \approx \overline{V}_{ref} \tag{3.3}$$

Contrarily to the simple inner-loop converter output voltage in (2.19), the proposed V^2 converter output voltage presents a theoretically negligible DC output resistance. Furthermore the comparator input offset is compensated by the integral action of the outer loop as well. This singularly relaxes design constraints on the comparator.

1.2 Sliding-Mode Analysis

In steady-state operation the inner loop feedback voltage is situated in the vicinity of the compensation voltage. When the comparator input error, $\epsilon\,(t)$, is positive, the V_{LX} node

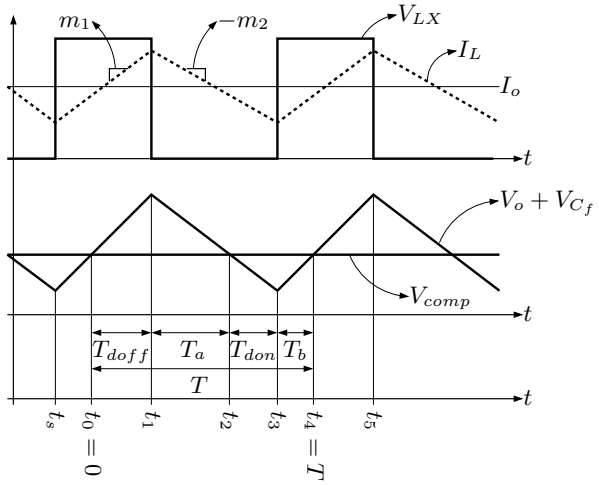


Figure 3.2 – Proposed solution chronograph

voltage is pulled to V_{bat} and the inductor current rises as well as the comparator negative input, until $\epsilon\,(t) = 0$ V. However due to the intrinsic deadtime and propagation delay of the power stage, a delay, T_{doff}, appears in the loop and the V_{LX} voltage is tied to zero after a small amount of time compared to the ideal time-event. The same phenomenon applies for the low-to-high transition that occurs after a delay, T_{don}, as represented in Figure 3.2. This limits the switching frequency to a low value.

According to the sliding-mode theory, the control law associated to the sliding function, $\epsilon = s\left(V_{comp}, V_{C_f}, V_o\right)$, is:

$$V_{LX} = \begin{cases} V_{bat} & \text{if } \epsilon > 0 \text{ V} \\ 0 & \text{if } \epsilon < 0 \text{ V} \end{cases} \tag{3.4}$$

Verifying the hitting condition is straightforward in this case: when operating in the subspace $\epsilon < 0$ V, the converter is associated to the control law $V_{LX} = 0$ V, so it asymptotically reaches $\epsilon = V_{bat}$, that is in the subspace $\epsilon > 0$ V, since the integral action of the outer voltage loop saturates and the output voltage asymptotically reaches 0 V. When operating in the subspace $\epsilon > 0$ V, the converter is associated with the control law $V_{LX} = V_{bat}$ and asymptotically reaches $\epsilon = -V_{bat}$, that is in the other subspace $\epsilon < 0$ V. In each case it is obvious that $\epsilon = 0$ V is reached.

Once the converter reaches the sliding surface $\epsilon = 0$ V, one has to ensure that the

trajectory of the converter is maintained on it, i.e. the system complies to the existence condition defined in [63, 109, 116]:

$$\epsilon\dot{\epsilon} < 0 \; V^2.s^{-1} \tag{3.5}$$

In the subspace $\epsilon > 0$ V, the existence condition implies $\dot{\epsilon} < 0$ V.s^{-1}, thus:

$$\dot{V}_{comp}(t) - \dot{V}_{C_f}(t) - \dot{V}_o(t) < 0 \; V.s^{-1} \tag{3.6}$$

Assuming that the triangle signal across C_f is small and globally centred on V_o, it comes:

$$\dot{V}_{C_f} = \frac{V_{bat} - V_o}{\tau_C} \tag{3.7}$$

Introducing (3.1) and (3.7) in (3.6) gives:

$$\frac{V_{ref}(t) - V_o(t)}{\tau_i} - \frac{V_{bat} - V_o(t)}{\tau_C} - \frac{I_L(t) - I_o(t)}{C_o} < 0 \; V.s^{-1} \tag{3.8}$$

Now let us consider the converter at the switching instant when $\epsilon > 0$ V. Then the inductor current, I_L, verifies:

$$I_L(t) - I_o(t) = -\frac{V_o}{L} T_{don} \tag{3.9}$$

where I_o is the output current. This leads the existence condition to become:

$$T_{don} < \frac{C_o L}{V_o} \left[\frac{V_{bat} - V_o}{\tau_C} - \frac{V_{ref} - V_o}{\tau_i} \right] \tag{3.10}$$

The integration time-constant, τ_i, is set approximately equal to the capacitive branch time-constant, τ_C, in the order of magnitude of a few switching cycles. Thereby since the output error is three order of magnitude smaller than the input-to-output voltage in typical conditions (a few mV compared to a few V), the existence condition can be approximated by:

$$T_{don} < \frac{LC_o}{\tau_C} . \frac{V_{bat} - V_o}{V_o} \tag{3.11}$$

Using the same methodology for the other sub-space $\epsilon < 0\ V$, yields:

$$T_{doff} < \frac{LC_o}{\tau_C}.\frac{V_o}{V_{bat} - V_o} \tag{3.12}$$

Depending on the conversion ratio, the most stringent conditions are defined in (3.11) or (3.12). Nevertheless in standard steady-state operation, these two conditions imply that the ideal output voltage ripple is non negligible with respect to the amplitude of the voltage across V_{C_f}. Operation outside the existence domain does not mean that the converter is strictly unstable but it does not follow a sliding-mode operation principle and does not operate with the delay-to-frequency characteristic used thereafter. Once the converter operates in sliding-mode, its average trajectory is and remains on the sliding-surface, i.e. $s = 0$ and $\dot{s} = 0$ respectively, where s is the average value of ϵ when neglecting the chattering[2] effects. Then averaging the sliding motion in (2.18) gives:

$$\overline{V}_{comp} = \overline{V}_{C_f} + \overline{V}_o \tag{3.13}$$

Higher-order development terms give the average dynamic control-to-output transfer function of the inner loop:

$$\frac{\overline{V}_o(s)}{\overline{V}_{comp}(s)} = \frac{1}{1 + \frac{R_L}{R_o}\frac{1+\tau_L s}{1+\tau_C s} + R_L C_o s \frac{1+\tau_L s}{1+\tau_C s}} \tag{3.14}$$

where R_o is the equivalent average load. (3.14) outlines the setting procedure of τ_C. By setting τ_C equal to τ_L, the inner loop becomes a first order loop whose transfer function is:

$$\frac{\overline{V}_o(s)}{\overline{V}_{comp(s)}} = \frac{R_o}{R_o + R_L}\frac{1}{1 + \frac{R_o R_L}{R_o + R_L} C_o s} \tag{3.15}$$

Equation (3.15) shows that the inner-loop behaves like a first order system. The output voltage tracks the compensation voltage with a static error and a first-order-type response. When noise immunity considerations force the designer to consider a higher ripple value on the negative comparator input, the single pole approximation is no longer

[2] in [116] *"Chattering, [...], describes undesired system oscillations with finite frequency caused by system imperfection."* In the considered application chattering is the ripple caused by the non-infinite switching frequency

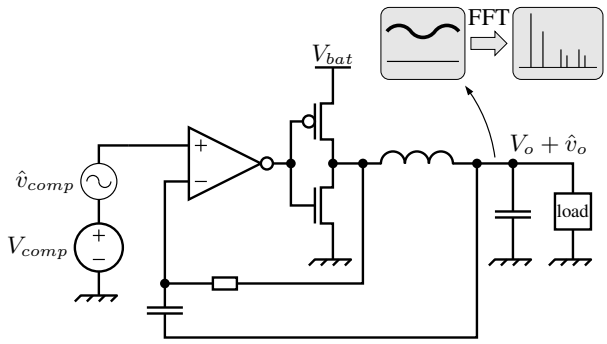


Figure 3.3 – Proposed validation method

valid and the full equation without simplification becomes:

$$\frac{\overline{V}_o(s)}{\overline{V}_{comp}(s)} = \frac{R_o}{R_o + R_l} \frac{1 + \tau_c s}{1 + \frac{R_o\tau_c + L + R_l R_o C_o}{R_o + R_l} s + \frac{R_o C_o L}{R_o + R_l} s^2} \tag{3.16}$$

This simple continuous-time model for the highly discontinuous inner loop is extensively used thereafter to set the components' values and to determine the design parameters. It remains valid while the converter evolves in the boundaries of the sliding function, i.e. the comparator input error is small. This is maintained by keeping the loop delay well below the sliding domain expressed by (3.11) and (3.12).

1.3 Validation of the inner-loop continuous average model and outer-loop setting

In order to validate the average model defined in (3.16), the inner-loop circuit is simulated with a full CMOS power stage model and the filter model proposed in section 2.8. Performing transient simulations, a small sinusoidal compensation voltage is applied and the output voltage is analyzed with the use of a 2048-point over 29 sinus-period FFT to determine the transfer gain as represented in Figure 3.3. Then the small-signal transfer gain is determined by the FFT amplitude ratio of $\hat{v}_o$ to $\hat{v}_{comp}$ at the considered frequency. A particular care is taken to use a small-signal AC source to keep the five first harmonics below 1% output distortion, thus results can be assumed to be linear.

The FFT analysis results fit with the proposed linear model for the different available

time constants. The 3dB-gain difference may come from the power stage parasitic elements. Simulations performed with an ideal power stage give no significant differences between the average model and the transistor level design.

The high DC-gain integrator with a time constant, τ_i, makes the control-to-output transfer function to become:

$$\frac{\overline{V}_o}{\overline{V}_{ref}} = \frac{R_o}{R_o + R_l} \frac{1 + \tau_c s}{\tau_i s + \frac{R_o\tau_c + L + R_l R_o C_o}{R_o + R_l}\tau_i s^2 + \frac{R_o C_o L \tau_i}{R_o + R_l} s^3} \tag{3.17}$$

The integration time-constant is set to provide sufficient gain and phase margins to insure stability according to standard linear compensation setting.

2 Toward the phase synchronization

2.1 Loop delay control

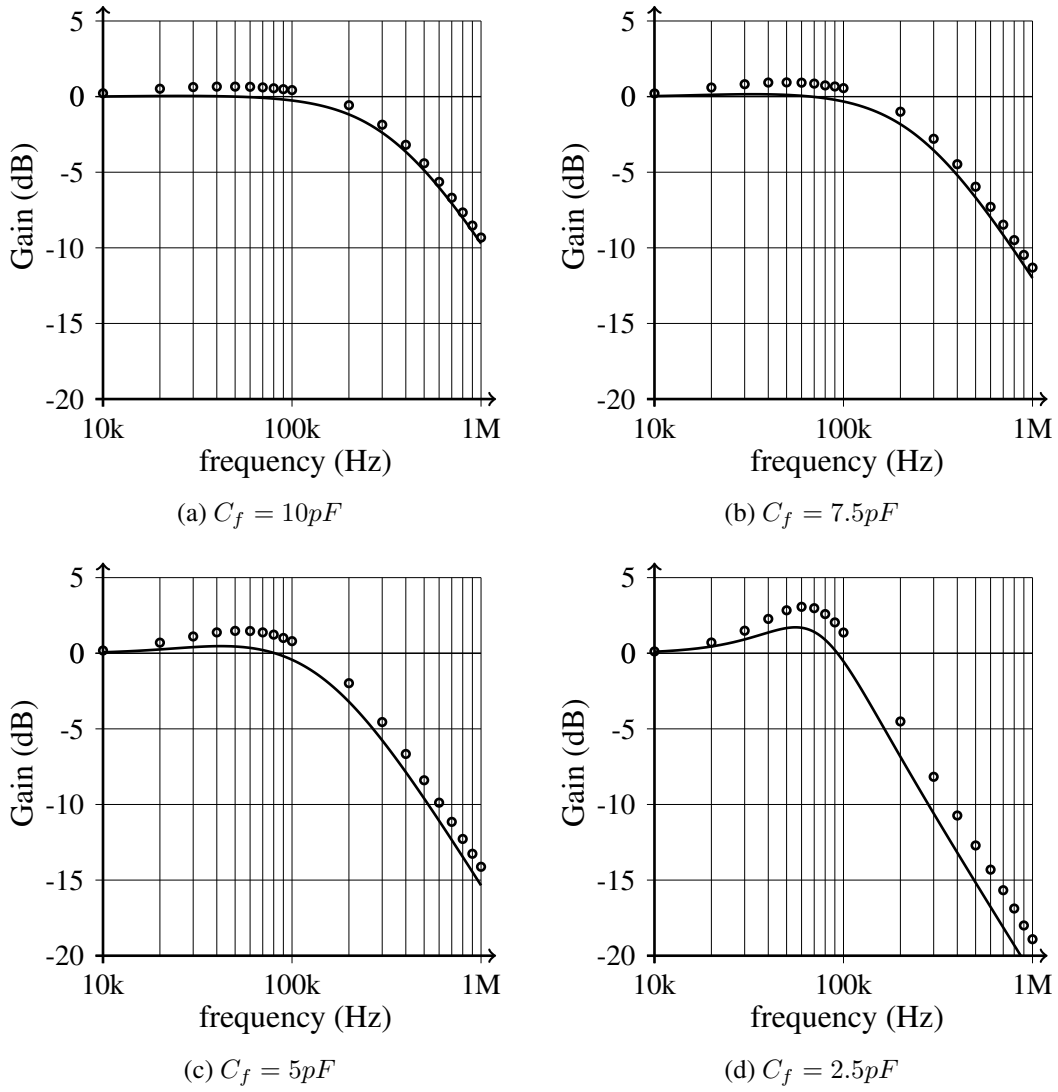
The switching frequency of the voltage regulation part is intrinsically uncontrolled. Moreover it is mainly dependent on input and output voltage and delays. Without using a voltage hysteresis cycle at the comparator input, the instantaneous switching frequency is derived from (2.20):

$$f_{sw} = \left[\frac{V_{vat}}{V_{bat} - V_o} T_{don} + \frac{V_{bat}}{V_o} T_{doff} \right]^{-1} \tag{3.18}$$

The key design idea of this thesis is to lower the speed of a fast comparator by reducing its differential input-pair bias current. The lower the bias current, the lower the overall comparison speed of the comparator. A principle schematic of the designed comparator is presented in Figure 3.5. The differential pair (M_1, M_2) splits the bias current I_b:

$$I_b = I_n + I_p \tag{3.19}$$

The current mirror (M_3, M_4) copies the negative branch current, I_n, and the current mirror (M_5, M_6) the positive branch current, I_p, respectively. The current mirror (M_7,



(a) $C_f = 10pF$

(b) $C_f = 7.5pF$

(c) $C_f = 5pF$

(d) $C_f = 2.5pF$

Figure 3.4 – Transistor level simulations (circles) and average linear model (continuous line) with different sets of time-constant

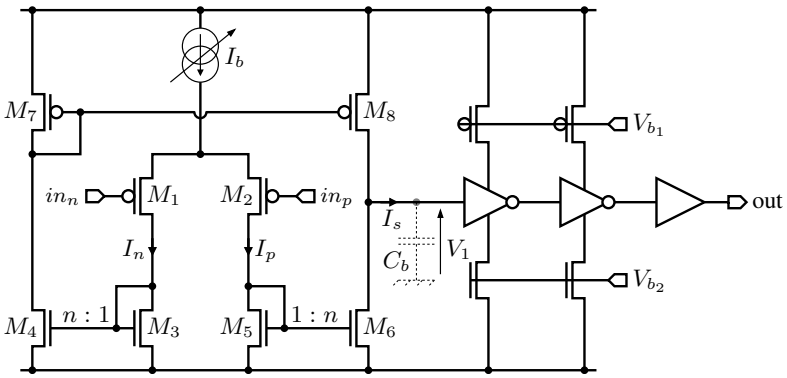


Figure 3.5 – Variable delay comparator principle schematic

M_8) copies the drain current of M_4 such that the first stage output current, I_s, follows:

$$I_s = n\,(I_n - I_p) \tag{3.20}$$

where $n = 2$ in the proposed design. Depending on the differential input voltage sign, the lumped parasitic capacitor, C_l, is charged or discharged.

Transistor ratios are set to impose sub-threshold operation for the differential pair (M_1, M_2) and active region operation otherwise. The gain of a saturated differential pair in an OTA configuration diminishes with an increase in the bias current. Subthreshold operation of the differential pair allows a stabilized or an increasing gain and an increasing bandwidth of the analog input stage while the bias current increases. No slew-rate limitation has been observed during simulation. This guarantees linear operation of the input stage. The transconductance of the differential pair MOSFETs depends on the bias point by:

$$g_{m_{1,2}} = \frac{I_D}{\xi V_T} \tag{3.21}$$

where ξ gathers process parameters, I_D is the drain-source current of the considered MOSFET and V_T is the thermal potential. MOSFETs operating in the active region present a transconductance that depends on the square-root of the bias current in a first order approximation:

$$g_{m_i} = \sqrt{2k'\frac{W_i}{L_i}I_D} \tag{3.22}$$

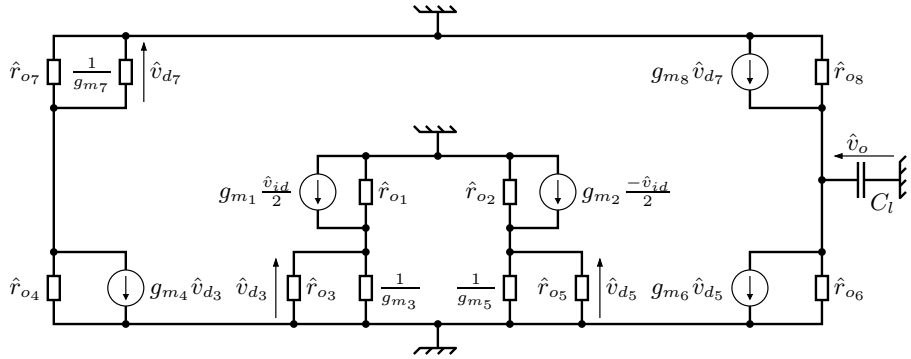


Figure 3.6 – Comparator input stage small signal model

where k' gathers process parameters. The channel length modulation makes the small-signal drain-source resistance of the MOSFETs dependent on the bias point too. The usual model equation is given by:

$$\hat{r}_o = \frac{1}{\lambda_i I_D} \tag{3.23}$$

However due to the small length of the MOSFETs in the selected technology, the channel length modulation parameter, λ_i, varies with the operating point. Inaccuracies in (3.22) and (3.23) lead to a non-negligible shift between the calculated values and simulation ones. Nevertheless trends remain valid. Intermediate voltages yields:

$$\hat{v}_{d_3} = g_{m_1}\frac{\hat{v}_{id}}{2}\frac{\hat{r}_{o_3}\hat{r}_{o_1}}{\hat{r}_{o_3}\hat{r}_{o_1}g_{m_3}+\hat{r}_{o_1}+\hat{r}_{o_3}} \tag{3.24}$$

$$\hat{v}_{d_5} = -g_{m_2}\frac{\hat{v}_{id}}{2}\frac{\hat{r}_{o_5}\hat{r}_{o_2}}{\hat{r}_{o_5}\hat{r}_{o_2}g_{m_5}+\hat{r}_{o_2}+\hat{r}_{o_5}} \tag{3.25}$$

$$\begin{aligned}\hat{v}_{d_7} &= g_{m_4}\hat{v}_{d_3}\frac{\hat{r}_{o_4}\hat{r}_{o_7}}{\hat{r}_{o_4}\hat{r}_{o_7}g_{m_7}+\hat{r}_{o_4}+\hat{r}_{o_7}} \\ &= g_{m_1}g_{m_4}\frac{\hat{v}_{id}}{2}\frac{\hat{r}_{o_3}\hat{r}_{o_1}}{\hat{r}_{o_3}\hat{r}_{o_1}g_{m_3}+\hat{r}_{o_1}+\hat{r}_{o_3}}\frac{\hat{r}_{o_4}\hat{r}_{o_7}}{\hat{r}_{o_4}\hat{r}_{o_7}g_{m_7}+\hat{r}_{o_4}+\hat{r}_{o_7}}\end{aligned} \tag{3.26}$$

The small signal output voltage, $\hat{v}_o(s)$, results in:

$$\hat{v}_o(s) = \frac{\hat{r}_{o_8}\hat{r}_{o_6}}{\hat{r}_{o_8}+\hat{r}_{o_6}}\frac{1}{1+\frac{\hat{r}_{o_8}\hat{r}_{o_6}}{\hat{r}_{o_8}+\hat{r}_{o_6}}C_l s}\left(g_{m_8}\hat{v}_{d_7}-g_{m_6}\hat{v}_{d_5}\right) \tag{3.27}$$

integrating (3.25) and (3.26) in (3.27):

$$\begin{aligned}\hat{v}_o(s) &= \frac{\frac{\hat{r}_{o8}\hat{r}_{o6}}{\hat{r}_{o8}+\hat{r}_{o6}}}{1+\frac{\hat{r}_{o8}\hat{r}_{o6}}{\hat{r}_{o8}+\hat{r}_{o6}}C_l s}\frac{\hat{v}_{id}}{2}g_{m_{1,2}}\frac{\hat{r}_{o_{3,5}}\hat{r}_{o_{1,2}}g_{m_{4,6}}}{\hat{r}_{o_{3,5}}\hat{r}_{o_{1,2}}g_{m_{3,5}}+\hat{r}_{o_{3,5}}+\hat{r}_{o_{1,2}}} \\ &\times\left[g_{m8}\frac{\hat{r}_{o_4}\hat{r}_{o7}}{\hat{r}_{o_4}\hat{r}_{o7}g_{m_7}+\hat{r}_{o_4}+\hat{r}_{o_7}}+1\right]\end{aligned} \tag{3.28}$$

using a normalized form:

$$\frac{\hat{v}_o(s)}{\hat{v}_{id}(s)} = \frac{A_v}{1+\tau s} \tag{3.29}$$

With results from (3.21), (3.22), (3.23) in (3.28), the gain expression, $A_v(0)$, is:

$$A_v = \frac{1}{2\xi n V_T(\lambda_8+\lambda_6)}\frac{\sqrt{nk'_n\frac{W_{4,6}}{L_{4,6}}}}{\sqrt{k'_n\frac{W_{3,5}}{L_{3,5}}}+\frac{\sqrt{I_b}}{2}(\lambda_{1,2}+\lambda_{3,5})}\left[\frac{\sqrt{k'_p\frac{W_8}{L_8}}}{\sqrt{k'_p\frac{W_7}{L_7}}+\frac{\sqrt{nI_b}}{2}(\lambda_4+\lambda_7)}+1\right] \tag{3.30}$$

Assuming an ideal current copy through the current mirrors, i.e. $\lambda_{3,5}=\lambda_4=\lambda_7=0$, and large output resistance of the differential pair MOSFETs ($\lambda_{1,2}=0$), the gain expression takes the standard form:

$$A_v = n.g_{m_{1,2}}(\hat{r}_{o_8}\parallel\hat{r}_{o_6}) = \frac{1}{\xi V_T(\lambda_8+\lambda_6)} \tag{3.31}$$

The time-constant expression follows:

$$\tau = \frac{\hat{r}_{o_8}\hat{r}_{o_6}}{\hat{r}_{o_8}+\hat{r}_{o_6}}C_l = \frac{2}{nI_b(\lambda_8+\lambda_6)}C_l \tag{3.32}$$

The input-stage differential voltage is the triangle waves, $V_{C_f}(t)$, minus the slow motion compensation voltage, $V_{comp}(t)$. Locally the input differential voltage is assumed to be a ramp which slope is the triangle voltage slope. The ramp response of the analog-part input is then:

$$\hat{v}_o(s) = \frac{A_v\alpha_r}{(1+\tau s)s^2} \tag{3.33}$$

where, α_r, is the input ramp slope. Using the partial fraction expansion yields:

$$\begin{aligned}\hat{v}_o(s) &= \frac{A_v\alpha_r}{(1+\tau s)\,s^2} = A_v\alpha_r\left(\frac{A}{1+\tau s}+\frac{B}{s}+\frac{C}{s^2}\right)\\ &= A_v\alpha_r\left(\tau\frac{1}{\frac{1}{\tau}+s}-\frac{\tau}{s}+\frac{1}{s^2}\right)\end{aligned} \tag{3.34}$$

using the inverse Laplace transform to go back to the time-domain:

$$V_o(t) = A_v\alpha_r\left(\tau e^{-\frac{t}{\tau}}-\tau+t\right)u(t) \tag{3.35}$$

The comparator variable time-delay part, t_d, is the solution of (3.35) when the output voltage equals the CMOS buffer logic threshold voltage, i.e. $V_{bat}/2$. Replacing exponential term in (3.35) with its power series-representation simplifies the calculation:

$$\begin{aligned}\frac{V_{bat}}{2} &\approx A_v\alpha_r\left(\left[\tau-t_d+\frac{t_d^2}{2\tau}\right]-\tau+t\right)u(t)\\ &= A_v\alpha_r\frac{t_d^2}{2\tau}\end{aligned} \tag{3.36}$$

t_d can be extracted as:

$$t_d = \sqrt{\frac{V_{bat}\tau}{A_v\alpha_r}} \tag{3.37}$$

introducing (3.31) and (3.32) in (3.37) yields:

$$t_d = \sqrt{\frac{2C_lV_{bat}}{n\xi V_T\alpha_r}}\frac{1}{\sqrt{I_b}} \tag{3.38}$$

(3.38) shows that the time delay decreases non-linearly with respect to the bias current. As expected the higher the bias current, the lower the input stage delay. Simulated values represented in Figure 3.7 differs from first-order model values but not in trends. This is mainly due to the non idealities and inaccuracies in the proposed small-signal models. Especially from output resistance and transconductance expressions of the current mirror transistors that differ from the simple first-order model.

The comparator buffer and the switching logic add a small amount of fixed delay,

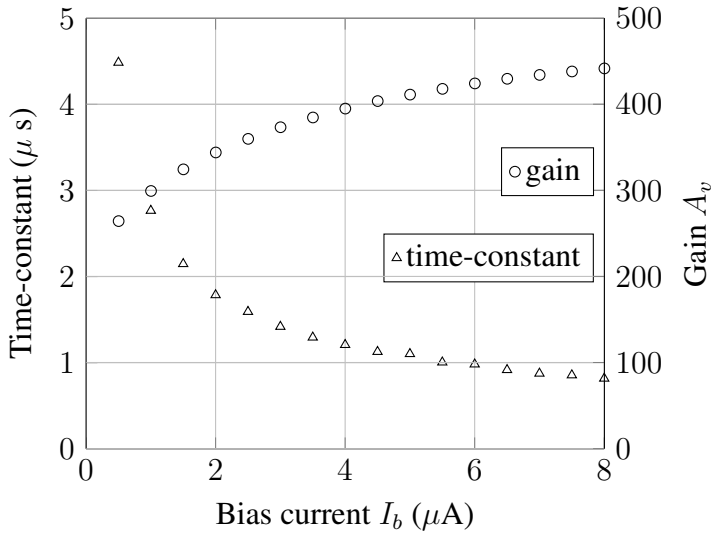


Figure 3.7 – Simulated comparator input-stage characteristics

t_{d_l}. Integrating the slope expression, the on-delay, $T_{d_{on}}$, first-order value becomes:

$$T_{d_{on}} = \sqrt{\frac{2C_l R_f C_f V_{bat}}{n\xi V_T V_o}} \frac{1}{\sqrt{I_b}} + t_{d_l} \tag{3.39}$$

and the off-delay, $T_{d_{off}}$:

$$T_{d_{off}} = \sqrt{\frac{2C_l R_f C_f V_{bat}}{n\xi V_T \left(V_{bat} - V_o\right)}} \frac{1}{\sqrt{I_b}} + t_{d_l} \tag{3.40}$$

Introducing (3.39) and (3.40) in (3.18) yields:

$$\begin{aligned} f_{sw}\left(I_b\right) = & \left[\frac{V_{bat}}{V_{bat} - V_o}\left(\sqrt{\frac{2C_l R_f C_f V_{bat}}{n\xi V_T V_o}} \frac{1}{\sqrt{I_b}} + t_{d_l}\right)\right. \\ & \left. + \frac{V_{bat}}{V_o}\left(\sqrt{\frac{2C_l R_f C_f V_{bat}}{n\xi V_T \left(V_{bat} - V_o\right)}} \frac{1}{\sqrt{I_b}} + t_{d_l}\right)\right]^{-1} \end{aligned} \tag{3.41}$$

that can be simplified with:

$$f_{sw}\left(I_b\right) = \frac{\sqrt{I_b}}{D + E\sqrt{I_b}} \tag{3.42}$$

where:

$$D = \sqrt{\frac{2C_l R_f C_f V_{bat}}{n\xi V_T}} \left(\frac{V_{bat}}{(V_{bat} - V_o)\sqrt{V_o}} + \frac{V_{bat}}{V_o\sqrt{V_{bat} - V_o}} \right) \tag{3.43}$$

and

$$E = \frac{V_{bat}^2}{(V_{bat} - V_o)\, V_o} \tag{3.44}$$

The first-order Taylor-series development is proposed to linearize the current-to-frequency characteristic:

$$f_{sw}\left(I_b + \hat{i}_b\right) \approx \frac{\sqrt{I_b}}{D + E\sqrt{I_b}} + \frac{D}{2\sqrt{I_b}\left(D + E\sqrt{I_b}\right)^2}\hat{i}_b \tag{3.45}$$

The equivalent current Controlled Oscillator (ICO) gain of the DC/DC converter yields:

$$G_{vco} = \frac{\partial f_{sw}\left(I_b + \hat{i}_b\right)}{\partial \hat{i}_b} = \frac{D}{2D^2\sqrt{I_b} + 4DEI_b + 2E^2 I_b^{\frac{3}{2}}} \tag{3.46}$$

(3.46) exhibits the variability of the gain with respect to the ICO center frequency. A voltage-to-current converter (i.e. a voltage-controlled current-source) is used to convert the ICO into a Voltage Controlled Oscillator (VCO). A solution to compensate the non-linear characteristic of the ICO is to use a non-linear voltage-controlled current-source. This solution faces major design challenges. First the need to properly models the variable delay elements, second the design in itself. Thus a linear voltage-controlled current-source is used at the expense of a non-linear VCO characteristic.

2.2 Analog Phase Locked Loop control

The DC/DC converter is inserted as a Voltage Controlled Oscillator (VCO) in a Phase Locked Loop (PLL) circuit. The proposed solution schematic is presented in Figure 3.8. The inner current-emulated loop is circled as the path (1) and the outer voltage loop as the path (2). These two loops form the voltage regulation part described in Section 1. The phase regulation loop is outlined as the path (3).

The voltage-controlled switching-frequency of the converter is sensed at the power bridge output and fed-back as an input of a Phase-Frequency-Detector (PFD) built with

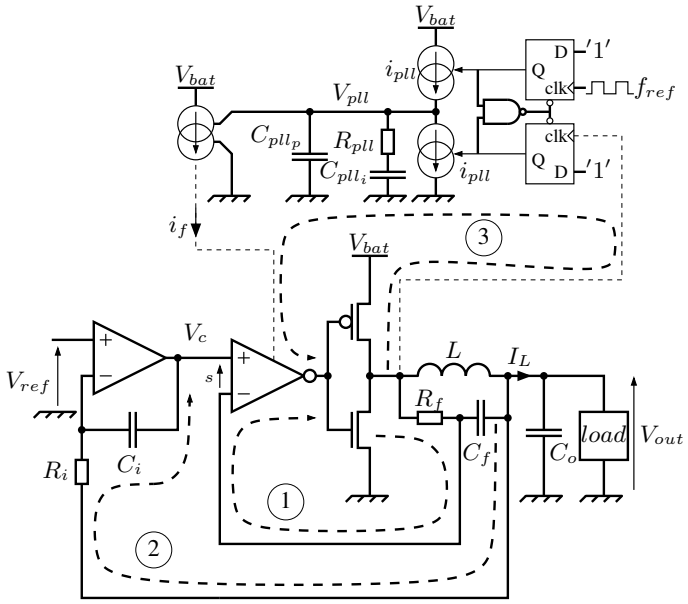


Figure 3.8 – Schematic of the implementation of the proposed phase-locked-loop frequency regulated sliding-mode converter

two standard logic D-flops and a NAND gate. The PFD three-state output drives a charge-pump circuit that is represented in Figure 3.8 by two controlled current-sources. When the reference-clock rising-edge is in advance with respect to the converter V_{LX} node rising-edge, the high-side current source is activated and a positive current, i_{pll}, flows through the PLL filter (R_{pll}, C_{pll_p}, C_{pll_i}) until a converter V_{LX} rising-edge occurs. Thereby the PLL-filter voltage, V_{pll}, rises and the voltage-controlled current source increases the comparator bias-current. The increased speed of the comparator yields a higher switching frequency. Contrarily when the converter power stage exhibits a rising-edge at its output voltage, V_{LX}, before the reference-clock rising-edge, the low side current source is activated until the clock rising-edge occurs. Thereby the PLL filter voltage, V_{pll}, decreases and the voltage-controlled current-source decreases the comparator bias current. The resulting lower speed of the comparator yields a lower switching frequency. When the converter operates in phase with the reference-clock, the two rising-edges arise synchronously, none of the flip-flop is set and the two current sources are deactivated. The filter remains in high impedance and holds its voltage value, V_{pll}.

The PFD average output is linear in phase. The larger the phase shift, $\Delta\Phi$, between

the reference clock and the switching converter switching phase, the wider the output pulse, α_{PFD}. The maximum value of α_{PFD} is reached when the phase shift is $\Delta\Phi = 2\pi$, i.e. the output is kept in a '1' logic state. The minimum value of α_{PFD} is reached when the phase shift is $\Delta\Phi = -2\pi$, i.e. the output is kept in a '-1' logic state. In between when there is no phase error, the PFD is never triggered and the average output, α_{PFD}, is zero. Consequently the average transfer-function of the PFD block is:

$$\frac{\alpha_{PFD}}{\Delta\Phi} = \frac{1}{2\pi} \tag{3.47}$$

The charge-pump transfer-function is then a single gain that converts the average PFD output into a current, i_{cp}, such that:

$$\frac{i_{cp}}{\alpha_{PFD}} = i_{pll} \tag{3.48}$$

The phase-loop-filter filters the charge-pump current with its impedance:

$$\frac{V_{pll}(s)}{i_{cp}(s)} = \frac{1}{\left(C_{pll_p} + C_{pll_i}\right)s} \cdot \frac{1 + R_{pll}C_{pll_i}s}{1 + \frac{C_{pll_p}C_{pll_i}}{C_{pll_p}+C_{pll_i}}R_{pll}s} \tag{3.49}$$

The filter provides an integral action to reject steady-state phase error. A phase-advance corrector is introduced with the addition of R_{pll}. This is used to stabilize the loop thanks to a transfer-function zero, without introducing spikes on the phase-loop filter voltage thanks to the high frequency pole.

3 Proposed system design

The proposed converter is designed using the following steps:

1. Power-part specification and design: this is not detailed thereafter due to the reuse of an existing standard buck power stage with an exception for the output filter, (L, C_o). Nowadays the design of a power output block is quite common [7].

2. Voltage regulation part design

Table 3.1 – Specifications for the prototype

V_{bat}	Input voltage	2.3 - 4.8 V / 3.6V typ
V_o	Output voltage	0.6 - 1.5 V / 1.2V typ
$I_{o_{max}}$	Max Output current	2 A
f_{sw}	Switching frequency	3.2 MHz
I_r	Max load current slope	6.44 MA/s

(a) Inner-loop setting: the current observer is set according to the power inductor. The comparator delay range is specified. The comparator CMOS design starts.

(b) Outer-loop (compensation function) setting: the integration time-constant is set according to the inner-loop specifications. The amplifier bandwidth is specified. The amplifier CMOS design starts.

3. Frequency-regulation part design: based on transistor-level simulations, the VCO characteristic is determined and the phase-loop filter is set. The PLL block design starts.

4. Validation: the whole converter is extensively simulated and optimized.

The design specifications are more diffuse since no clear digital load target was available along the thesis. As a starting-point, specifications gathered in Table 3.1 are used. This corresponds to the supply needs of a low-power ARM®-type based Cortex®A series processor.

3.1 Output passive components selection

The choice of a power inductor is a multivariable tradeoff that impacts the converter-efficiency and the transient performances. [94] defines the *"Current Ripple Ratio"*, r, as:

$$r = \frac{I_{pk-pk}}{I_{dc}} \tag{3.50}$$

where I_{dc} is the DC current through the inductor and I_{pk-pk} is the peak-to-peak AC current through the inductor. Then it is pointed out that as a rule of thumb a current ripple

ratio close to 0.4 is generally an optimum in terms of efficiency and size. Reducing the ripple factor, the size of the inductor increases in order to handle the energy surplus. Increasing the ripple factor, the output capacitor RMS current increases and the size of the inductor does not decrease significantly since the peak power to handle is higher than the proposed setting. Using this setting for the typical case at maximum current yields:

$$L \approx \frac{(V_{bat} - V_o)\, V_o}{0.4 I_o V_{bat} F_{sw}} = 312.5nH \tag{3.51}$$

This optimization suffers from vague specifications about the load-current distribution. Maximum current optimization is probably not the best solution to maximize the overall efficiency since the digital-core supply current is ranging over the whole load range. Selecting a standard 470 nH inductor appears to be a good tradeoff between the optimization point (which is lower than the maximum output current) and the coil commercial availability.

Under typical output voltage condition, the inductor current maximum negative slope is 2.5 five times lower than the apparent load one (2.55 MA/s versus 6.55 MA/s respectively). An ideal controller[3] would require a minimum amount of decoupling capacitor to absorb the energy that is left over the inductor otherwise the overshoot may exceed a high voltage limit for the technology. Lowering the minimum capacitor size in the sens of Time Optimal Control (TOC) can be done with the use of a smaller inductor. However the ripple factor increases unless the switching frequency is increased as well [8]. Higher switching frequency efficiency is not systematically worse than lower switching frequency efficiency since the losses distribution changes. Considering similar package, the lower the inductor, the lower its serial resistance. However the lower the inductor, the higher the optimal switching frequency, the higher the power-state switching losses. The best efficiency is reached at 5 MHz with a 240 nH inductor and 4 MHz with a 470 nH inductor.

Chosen components are MLP2016HR47M and MLP2016VR24M from TDK (respectively 470 nH and 240 nH). These multilayer ceramic inductors in small package (2 mm length, 1.6 mm width and 1 mm thickness) can handle[4] 1.7 Amps and 2 Amps

[3] in term of Time Optimal Control
[4] with a 30% drop in inductance value

respectively. The inductance remains constant up to 100 MHz, what makes a perfect choice for the 1 to 10 MHz switching frequency range. The output capacitor is set between 4.7 μF and 22 μF depending on the targeted transient performances. A 3.2 MHz switching frequency comes from the power stage design tradeoff (prior to the thesis) which is open to criticism. The Analog-Baseband (AB) circuit provides the reference clock.

3.2 Voltage regulation part design

The controller design starts with the choice of the current-observer time-constant. The chosen inductors' time constants are 8.5 μs and 8 μs respectively. A 10 μs observer time-constant, $R_f C_f$, is chosen with the combination of a 1000 kΩ resistor and a 10 pF capacitor. In a first approximation the typical condition voltage ripple, ΔV_{C_f}, across the observer capacitor, C_f, is:

$$\Delta V_{C_f} \approx \frac{V_{bat} - V_o}{R_f C_f} . \frac{V_o}{V_{bat}} T_r = \frac{V_o}{R_f C_f} \left(1 - \frac{V_o}{V_{bat}}\right) T_r \tag{3.52}$$

With the proposed values, the typical observer voltage ripple is 25.6 mV. In order to increase the ramp amplitude, the observer capacitor can be divided by 4 thereby the observer time-constant value can be lowered to 2.5 μs to increase the noise immunity. Nevertheless the effective inductor AC-resistance is frequency-dependent and higher than the DC one as presented in Figure[5] 3.9. Thereby using the DC resistance is a worst case condition that results in the higher observer time-constant.

The compensation-to-output voltage model in (3.16) or (3.15) with the minimal load resistance gives the maximal integration time-constant that meets the phase margin criterion. The 3dB-bandwidth of the inner-loop system is between 150 kHz ($C_f = 2.5$ pF) and 350 kHz ($C_f = 10$ pF). Hence the optimal integrator time-constant values are 1μs and 0.5μs. Values in the range of 2μs to 0.13μs are implemented.

[5]Downloaded in September 2013 from http://www.tdk-components.de

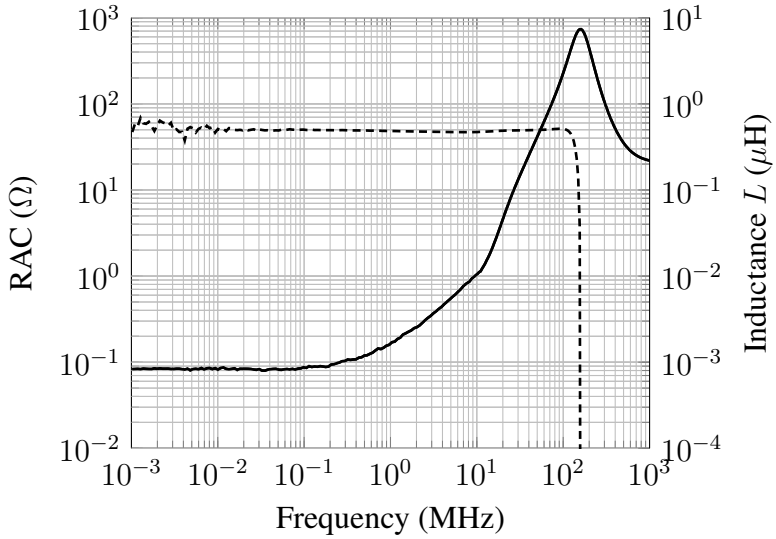


Figure 3.9 – 470 nH inductor manufacturer data-set, AC resistivity (continuous line) and Inductance (dashed line)

3.3 Frequency regulation part design

Once the voltage part is set, the current-to-frequency characteristic has to be determined. This is the main difficulty in the design process since proper time characterization depends on various parasitic elements. First the comparator current-to-delay function depends on the lumped parasitic capacitors that can only be estimated using post-layout extraction. The power stage delay is approximately known and assumed to be fixed. The output voltage ripple influences the delay as well with the addition of a step in the comparator input ramp voltage. The latter step amplidude depends on the ratio of the output capacitor Equivalent Serial inductance, R_{esl}, to the inductance, L. Thus the voltage-loop propagation delay is estimated using post-layout simulation of the comparator for which a constant compensation voltage is applied on the positive input and a representative triangle, plus a small square ripple, is applied on the negative input. A small fixed delay is added to model the power stage and driving logic delays. Furthermore the delay simulations strongly depend on the simulator accuracy. Thus simulating the whole converter is time consuming and gives no additional accuracy as with the proposed method.

According to the current-to-frequency model, the phase filter is determined using a standard PLL design methodology. The charge-pump is designed to provide the mini-

mum possible gain. This reduces the filter capacitor size. The main filter capacitor, C_{pll_i}, is set to cut the bandwidth one tenth lower than the voltage regulation part bandwidth. The zero resistor, R_{pll}, is set to provide a phase-boost at the open-loop 0-dB gain frequency. The high frequency filter capacitor, C_{pll_p}, is set ten times lower than the main capacitor, C_{pll_i}, in order to filter the charge-pump current pulses but preserving the zero resistor, R_{pll}, phase boost. This setting follows the so called non-interaction principle as will be discussed in Chapter 4 but is more intended to stabilize the loop at the cost of a small phase noise. Nevertheless the phase filter has been designed to provide flexibility in order to validate the stability analysis as proposed in Chapter 4.

The evaluated[6] ICO gain is ranging from 0.1 MHz/μA to 1 MHz/μA with a 470 nH inductor and 0.2 MHz/μA to 2 MHz/μA with a 240nH inductor. Simulation spread is wider depending on the integration algorithm and accuracy. The voltage-to-current converter has been designed to have a gain that is ranging from 10μA/V to 1μA/V. This compensates the gain variation of the ICO even if it was not primarily intended for. The PLL filter capacitor is set between 10 pF and 50 pF what sets the uncompensated open-loop 0-dB crossing frequency between 90 kHz and 600kHz. The zero resistor, R_{pll}, is set between 300 kΩ and 6.3 MΩ, what offers multiple compensation flavors in which the converter is stable and some cases in which the converter is unstable. The light-gray shaded area plot in Figure 3.10 presents the resulting uncompensated open-loop domain (i.e. without the phase boost provided by R_{pll}). The uncompensated phase-shift follows the -180 degree line that makes the loop unstable without compensation. The compensation resistor adds the phase boost represented in dark grey that increases the gain after the compensation zero. It is ranging from 1 kHz up to 200 kHz and some sets are expected to be unstable. The typical open-loop is represented in solid line. It presents a sufficient phase margin to ensure loop stability despite a low expected bandwidth (50kHz).

[6]results are gathered in chapter 6 and appendix D

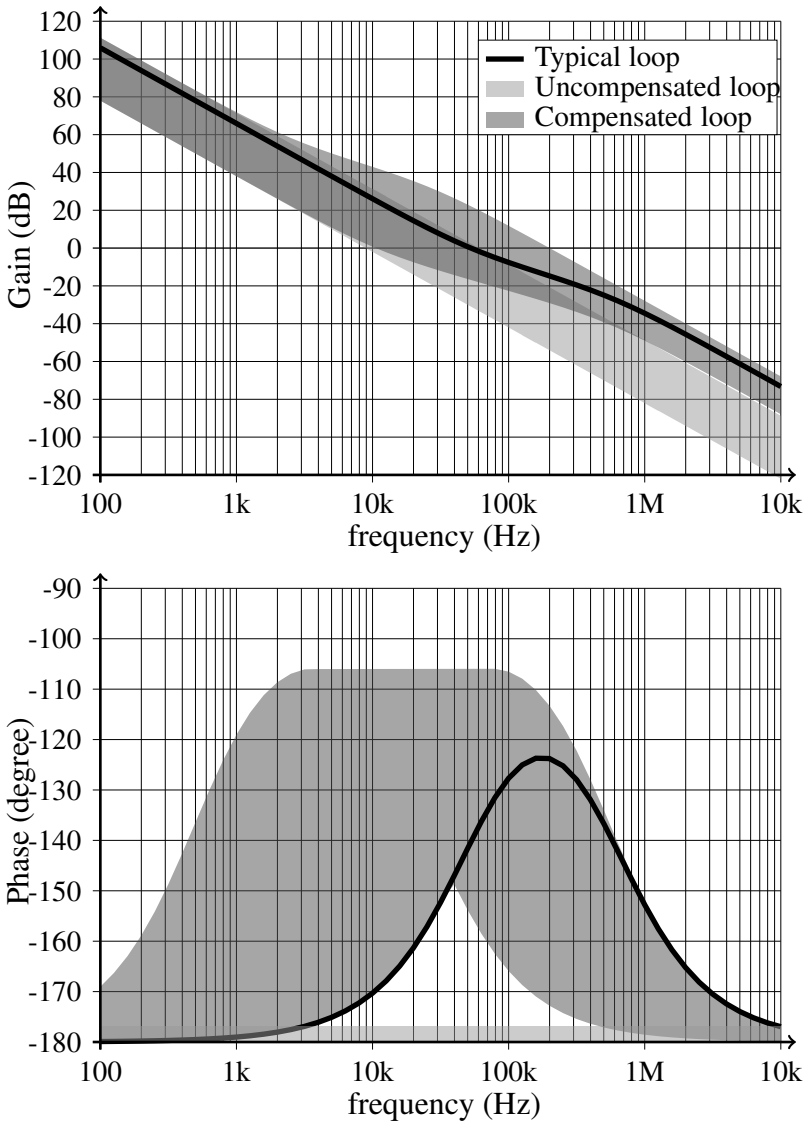


Figure 3.10 – Open-loop transfer function of the phase locked loop

4 Solution discussion

The proposed solution mainly consists in a replacement of fixed clock modulator by a self oscillating inner sliding-loop. The outer compensation function differs in the pole and zero number from a voltage or current-mode PWM converter compensation function however it remains a linear function of the output voltage error. The converter behaves more like a current mode control than a voltage mode control thanks to its two loop architecture: the inner loop is based on the average current loop but differs from the conventional current mode in the current measurement system. The proposed solution uses a passive estimation circuit to estimate the AC current instead of a direct measurement system. The frequency variability of the inner loop requires the use of a frequency locking scheme. A phase loop is used to clock not only the converter frequency but also its phase.

This solution is used to reduce the transient response variability which in mainly phase depend, the proposed solution counteracts a load transient asynchronously. This is the main advantage of a soft synchronized solution over the hard synchronized paradigm otherwise a simple slope compensation and a D-flop synchronization as presented in Appendix [62] is simpler and smaller than the proposed frequency locking scheme.

Simple models are developed in order to give simple but efficient tools to the designer. A design methodology that cope with simulation limitations is proposed. The compensation function is voluntarily kept simple but the designer can increase its order to increase the small-signal performances. However large transient characteristics that set the overall transient performance of the converter are not modeled by the proposed small-signal model and the mixed loop stability remains an open issue.

Efficiency is a main concern of power conversion. The effect of the proposed control architecture and specifically the phase-locked-loop circuit on the power conversion efficiency has to be pointed out. For large DC output current and CCM operations the efficiency mainly depends on the power stage design, the power passive components and the switching frequency since the controller power consumption is negligible. The proposed control scheme regulates the switching frequency to a controlled frequency. Therefore the efficiency is the same than a PWM controlled converter since the switch-

ing losses are equivalent[7] as well are the conduction losses since the duty cycle is the same otherwise the output voltage would not be properly regulated. During DCM operation the phase loop circuit is deactivated and its power consumption is negligible.

[7] the power stage switches at the same rate either in PWM control or with the proposed control scheme

Chapter 4

Sampled data mixed loop analysis

Models and analysis of the two regulation loops have been proposed in 1 and 2. This chapter aims to analyse whether the converter is stable or unstable without neglecting the possible cross-interactions between the frequency regulation loop and the other loops. More detailed analysis of the voltage loop using sliding mode based analysis is proposed in [109]. Linearised models are also provided in [11, 79, 83]. These more accurate models may provide additional accuracy however this does not significantly improve the voltage regulation design process. The phase regulation loop is also covered in [14,47,52,61,71,106,120,124] under the assumption of non-interaction between loops. This method converts the system in two independent Single-Input, Single-Output (SISO) systems. However no guarantee is provided that neglected off-diagonal elements of the system state-space matrix do not engender cross interactions. Furthermore delay-based controls such as Constant-On-Time (COT) control are subject to sub-harmonic instabilities that cannot be modelled from an average based analysis.

Sampled-data based stability analysis can predict sub-harmonic instabilities, period doubling and state bifurcations [28, 91, 92]. The method has been used to extensively cover the PWM control in [68,91,92,113]. An equivalent method is proposed for a variable switching frequency in [16, 77, 89]. Nevertheless these analyses cover the voltage regulation part but no frequency regulation loop is included in the model so far.

The inner sliding-mode loop behaves like a Multiple-Input Multiple-Output (MIMO) system as presented in Figure 4.1. The two control inputs are the compensation voltage,

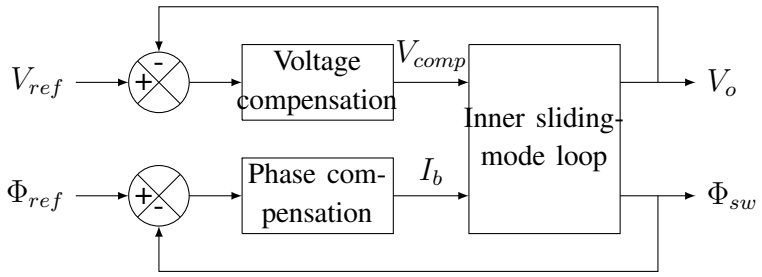


Figure 4.1 – MIMO model of the proposed solution

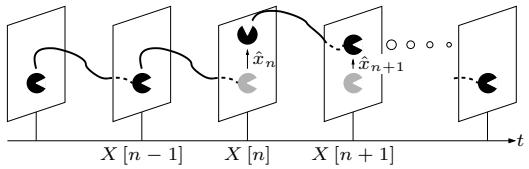


Figure 4.2 – Sampled data analysis - principle

V_{comp}, and the delay control current, I_b. The two outputs are the output voltage, V_o, and the switching phase, Φ_{sw}. An ideal compensation scheme would be a diagonal control in which each output variable is independently regulated. However the system model may present large off-diagonal elements that have not been determined prior to design and cross-interactions between loops may occur.

The proposed variable-rate sampled-data analysis principle is presented in Figure 4.2. The cycle initial steady-state vector $X\,[n]$ is modified by a small perturbation, unknown in type and source, $\hat{x}\,[n]$. Using a non-linear model (i.e. a set of non-linear differential equations), the end-cycle state vector, $X\,[n+1]$, is determined. **The first order perturbation rejection rate $\Phi = \hat{x}\,[n+1]\,\hat{x}\,[n]^{-1}$ is determined and the eigenvalues of Φ are analysed. If the modulus of an eigenvalue is higher or equal to one, the perturbation is amplified and the converter is unstable.**

This method presents the following advantages:

- Non-linear elements are modelled. This is an effective way to model the sliding-mode control which is nonlinear in essence.
- Delays are accurately modelled.

- Cross interaction are modelled since state variables of both the voltage regulation part and the frequency regulation part are gathered in one system state vector.

The converter state trajectory between two sampling instants is not covered by the method and the length of the cycle is undetermined. No guarantee is given that an undetermined perturbation leads to an infinite cycle (or at least very long cycle) in which the state trajectory goes in unwanted region (e.g. the output voltage goes up to V_{bat} or down to $0V$). The perturbation will be asymptotically rejected but the converter exhibits unwanted behaviours[1].

This chapter is organized as follow: section 1 presents the analysis method. The methodology is presented first with a general concept as it is applicable to any multi-loop converter. Section 2 presents the converter model used by the proposed methodology, section 3 presents the process used to determine the steady-state state-vector, then section 4 concludes the chapter.

1 Methodology

The converter steady-state trajectory can be modeled over one cycle, n, by a set of non-linear recurrence functions $f_{x_v} : \Re^{l+2} \rightarrow \Re^{l_v}$ and $f_{x_f} : \Re^{l+2} \rightarrow \Re^{l_f}$ with $l = l_v + l_f$:

$$\begin{cases} X_v[n+1] = f_{x_v}(X_v[n], X_f[n], \Sigma[n]) \\ X_f[n+1] = f_{x_f}(X_v[n], X_f[n], \Sigma[n]) \end{cases} \tag{4.1}$$

where X_v gathers the voltage regulation subsystem state-variables **(i.e. the energy stored inside the power components, the voltage across the observer capacitor and the voltage integrator state variables)** and X_f the frequency regulation subsystem state-variables **(i.e. the voltage across the phase loop filter and the phase error of the converter)**. $X[n]$ is the state vector at beginning of cycle and $X[n+1]$ the end-cycle state vector. Referring to the proposed converter chronograph presented in Figure 3.2 $X[n]$ is the converter state-vector at $t = t_0$ and $X[n+1]$ is the converter state-vector at $t = t_4$. $\Sigma[n]$ represents the hitting conditions, i.e. when the sliding function

[1] No kind of such case has been observed during experimental measurements.

reaches zero either at $t = t_2$ and $t = t_4$. The time origin is **arbitrarily** set when the sliding function reaches zero from the positive subspace. i.e. prior the reaching instant the comparator input error, ϵ, is positive. The cycle ends when the same condition occurs again. During the cycle, the sliding function is reached from the negative subspace, i.e. prior the reaching instant the comparator input error, ϵ, is negative and the converter switches after a small delay. This is modelled by the control input variable $\Sigma[n]$.

If the initial state vector presents a small displacement, $\hat{x}_n$, and a small change in the hitting conditions $\sigma\hat{[}n]$, (4.1) becomes:

$$\begin{cases} X_v[n+1] + \hat{x}_v[n+1] = f_{x_v}(X_v[n] + \hat{x}_v[n], X_f[n] + \hat{x}_f[n], \Sigma[n] + \hat{\sigma}[n]) \\ X_f[n+1] + \hat{x}_f[n+1] = f_{x_f}(X_v[n] + \hat{x}_v[n], X_f[n] + \hat{x}_f[n], \Sigma[n] + \hat{\sigma}[n]) \end{cases} \tag{4.2}$$

using a first-order linear approximation, (4.2) yields:

$$\begin{cases} X_v[n+1] + \hat{x}_v[n+1] &= f_{x_v}(X_v[n], X_f[n], \Sigma[n]) \\ & \quad + J_{f_v}(X_v[n], X_f[n], \Sigma[n]) . [\hat{x}_v, \hat{x}_f, \hat{\sigma}]^t \\ X_f[n+1] + \hat{x}_f[n+1] &= f_{x_f}(X_v[n], X_f[n], \Sigma[n]) \\ & \quad + J_{f_f}(X_v[n], X_f[n], \Sigma[n]) . [\hat{x}_v, \hat{x}_f, \hat{\sigma}]^t \end{cases} \tag{4.3}$$

where J_{f_v} and J_{f_f} are the Jacobian matrices of f_{x_v} and f_{x_f} respectively. Expanding the Jacobian expressions and eliminating the steady-state variables in (4.3) gives:

$$\begin{cases} \hat{x}_v[n+1] = \frac{\partial f_{x_v}}{\partial X_v[n]}\hat{x}_v[n] + \frac{\partial f_{x_v}}{\partial X_f[n]}\hat{x}_f[n] + \frac{\partial f_{x_v}}{\partial \Sigma[n]}\hat{\sigma}[n] \\ \hat{x}_f[n+1] = \frac{\partial f_{x_f}}{\partial X_v[n]}\hat{x}_v[n] + \frac{\partial f_{x_f}}{\partial X_f[n]}\hat{x}_f[n] + \frac{\partial f_{x_f}}{\partial \Sigma[n]}\hat{\sigma}[n] \end{cases} \tag{4.4}$$

The control equation is needed to solve (4.4) by eliminating $\hat{\sigma}$. Two hitting conditions are defined by $g : \Re^{l+2} \rightarrow \Re^2$:

$$[0]_{2,1} = g(X_v[n], X_f[n], \Sigma[n]) \tag{4.5}$$

introducing the small state deviation gives:

$$[0]_{2,1} = g\left(X_v\left[n\right], X_f\left[n\right], \Sigma\left[n\right]\right) + J_g\left(X_v\left[n\right], X_f\left[n\right], \Sigma\left[n\right]\right). \begin{bmatrix} \hat{x}_v\left[n\right] \\ \hat{x}_f\left[n\right] \\ \hat{\sigma}\left[n\right] \end{bmatrix} \tag{4.6}$$

where J_g is the Jacobian matrix of g. Expanding J_g and removing the steady-state terms in (4.6) gives:

$$[0]_{2,1} = \frac{\partial g}{\partial X_v\left[n\right]}\hat{x}_v\left[n\right] + \frac{\partial g}{\partial X_f\left[n\right]}\hat{x}_f\left[n\right] + \frac{\partial g}{\partial \Sigma\left[n\right]}\hat{\sigma}\left[n\right] \tag{4.7}$$

$\hat{\sigma}$ is easily extracted from (4.7):

$$\hat{\sigma}\left[n\right] = -\left[\frac{\partial g}{\partial \Sigma\left[n\right]}\right]^{-1}\left[\frac{\partial g}{\partial X_v\left[n\right]}\hat{x}_v\left[n\right] + \frac{\partial g}{\partial X_f\left[n\right]}\hat{x}_f\left[n\right]\right] \tag{4.8}$$

and injected in 4.4:

$$\begin{cases} \hat{x}_v\left[n+1\right] \approx \frac{\delta f_{x_v}}{\delta X_v[n]}\hat{x}_v\left[n\right] + \frac{\delta f_{x_v}}{\delta X_f[n]}\hat{x}_f\left[n\right] \\ \qquad\qquad -\frac{\delta f_{x_v}}{\delta \Sigma[n]}\left[\frac{\delta g}{\delta \Sigma[n]}\right]^{-1}\left[\frac{\delta g}{\delta X_v[n]}\hat{x}_v\left[n\right] + \frac{\delta g}{\delta X_f[n]}\hat{x}_f\left[n\right]\right] \\ \hat{x}_f\left[n+1\right] \approx \frac{\delta f_{x_f}}{\delta X_v[n]}\hat{x}_v\left[n\right] + \frac{\delta f_{x_f}}{\delta X_f[n]}\hat{x}_f\left[n\right] \\ \qquad\qquad -\frac{\delta f_{x_f}}{\delta \Sigma[n]}\left[\frac{\delta g}{\delta \Sigma[n]}\right]^{-1}\left[\frac{\delta g}{\delta X_v[n]}\hat{x}_v\left[n\right] + \frac{\delta g}{\delta X_f[n]}\hat{x}_f\left[n\right]\right] \end{cases} \tag{4.9}$$

(4.9) exhibits the cycle perturbation rejection matrix of the closed-loop converter that can be set in a matrix form as:

$$\begin{bmatrix} \hat{x}_v\left[n+1\right] \\ \hat{x}_f\left[n+1\right] \end{bmatrix} = \begin{bmatrix} \Theta_{vv} & \Theta_{fv} \\ \Theta_{vf} & \Theta_{ff} \end{bmatrix} \begin{bmatrix} \hat{x}_v\left[n\right] \\ \hat{x}_f\left[n\right] \end{bmatrix} \tag{4.10}$$

where Θ_{vv} and Θ_{ff} are respectively the voltage-loops and frequency-loop rejection matrices and Θ_{fv} and Θ_{vf} respectively the frequency-to-voltage and voltage-to-frequency loops' cross-interactions' matrices.

$$\Theta_{fv} = \frac{\delta f_{x_v}}{\delta X_f\left[n\right]} - \frac{\delta f_{x_v}}{\delta \Sigma\left[n\right]}\left[\frac{\delta g}{\delta \Sigma\left[n\right]}\right]^{-1}\frac{\delta g}{\delta X_f\left[n\right]} \tag{4.11}$$

$$\Theta_{vf} = \frac{\delta f_{x_f}}{\delta X_v\,[n]} - \frac{\delta f_{x_f}}{\delta \Sigma\,[n]} \left[\frac{\delta g}{\delta \Sigma\,[n]}\right]^{-1} \frac{\delta g}{\delta X_v\,[n]} \tag{4.12}$$

$$\Theta_{vv} = \frac{\delta f_{x_v}}{\delta X_v\,[n]} - \frac{\delta f_{x_v}}{\delta \Sigma\,[n]} \left[\frac{\delta g}{\delta \Sigma\,[n]}\right]^{-1} \frac{\delta g}{\delta X_v\,[n]} \tag{4.13}$$

$$\Theta_{ff} = \frac{\delta f_{x_f}}{\delta X_f\,[n]} - \frac{\delta f_{x_f}}{\delta \Sigma\,[n]} \left[\frac{\delta g}{\delta \Sigma\,[n]}\right]^{-1} \frac{\delta g}{\delta X_f\,[n]} \tag{4.14}$$

Rewriting (4.10) in a standard form gives:

$$X\,[n+1] = \Theta_J X\,[n] \tag{4.15}$$

where Θ_J is the overall system Jacobian matrix:

$$\Theta_j = \begin{bmatrix} \Theta_{vv} & \Theta_{fv} \\ \Theta_{vf} & \Theta_{ff} \end{bmatrix} \tag{4.16}$$

A proper study of the eigenvalues of Θ_j is performed to evaluate the stability of the closed-loop system. Each eigenvalue determines the amount of expansion or stretch of a perturbation following the associated eigenvector. If an eigenvalue module is higher than one (i.e. the eigenvalue is outside the unit circle), a small perturbation in the direction of the associated eigenvector is amplified, and the system is unstable. Contrarily eigenvalue modules lower than one (i.e. the eigenvalues are inside the unit circle) diminish the module of the perturbation. The Jacobian matrix calculation requires the determination of the system recurrence equations and the initial cycle vector $X\,[n]$.

2 Sampled data model

This section describe the recurrence equation development of the modeled converter, f_{x_v}, f_{x_f} and g. The recurrence function of the voltage regulation part, f_{x_v}, is developed in 2.1. The recurrence function of the frequency regulation part, f_{x_f}, is developed in 2.2. The hitting conditions' function, g, is developed in 2.3. Last the delay expressions that are used either in f_{x_v}, f_{x_f} and g are presented in 2.4.

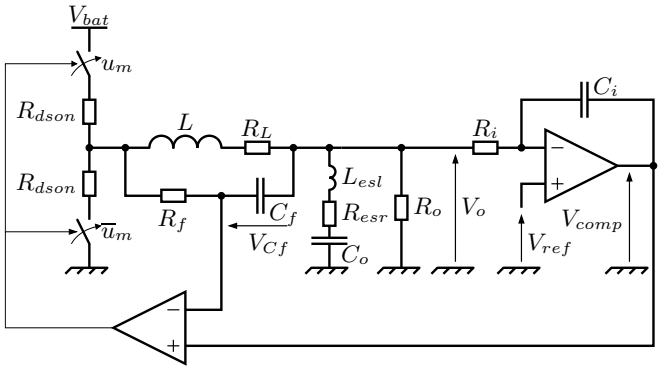


Figure 4.3 – Voltage part model of the proposed converter

2.1 Recurrence model of the voltage regulation part

Models of the proposed converter voltage-loops are represented in Figure 4.3. The MOSFETs are represented by ideal switches and a resistors R_{dson}. The proposed converter uses symmetrical power stage in which the top MOSFET on-resistance is the same as the bottom MOSFET one. This simplifies the equation system since whatever the input command, u_v, the state transition matrix remains the same. The operational amplifier is modelled by a finite gain and a dominant pole with a time-constant τ. The filter inductor is modelled by an ideal inductor and a series resistance, R_L. Even if the AC resistance is not constant at high frequency, the impedance model of the inductor fits the supplier impedance data-set up to 100 MHz **which is significantly above the average switching frequency**. The multilayer ceramic output capacitor is no longer capacitive at the switching frequency where the serial parasitic inductor, L_{esl}, dominates.

The state space model of the voltage regulation part converter is represented using a linear time-invariant form:

$$\dot{X}_v = A_v X_v + B_v u_v \tag{4.17}$$

with

$$X_v = \begin{bmatrix} V_o \\ I_l \\ V_{C_f} \\ V_{C_o} \\ V_{comp} \\ \dot{V}_{comp} \end{bmatrix} \tag{4.18}$$

and

$$u_v = \begin{bmatrix} u_m \\ V_{ref} \end{bmatrix} \tag{4.19}$$

where u_m represents the switches' state. A transistor is ON when $u_m = 1$ and OFF otherwise. The other matrices are:

$$A_v = \begin{bmatrix} -\frac{R_o}{L} - \frac{R_o+R_{esr}}{L_{esl}} & -\frac{R_o(R_{dson}+R_L)}{L} - \frac{R_oR_{esr}}{L_{esl}} & 0 & \frac{R_o}{L_{esl}} & 0 & 0 \\ \frac{-1}{L} & -\frac{R_{dson}+R_L}{L} & 0 & 0 & 0 & 0 \\ \frac{-1}{R_fC_f} & \frac{-R_{dson}}{R_fC_f} & \frac{-1}{R_fC_f} & 0 & 0 & 0 \\ \frac{-1}{R_oC_o} & \frac{1}{C_o} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ \frac{-A_0}{\tau R_iC_i} & 0 & 0 & 0 & \frac{-1}{\tau R_iC_i} & -\frac{\tau+(A_0+1)R_iC_i}{\tau R_iC_i} \end{bmatrix} \tag{4.20}$$

and

$$B_v = \begin{bmatrix} \frac{V_{bat}R_o}{L} & 0 \\ \frac{V_{bat}}{L} & 0 \\ \frac{V_{bat}}{R_fC_f} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{A_0}{\tau R_iC_i} \end{bmatrix} \tag{4.21}$$

Considering the cycle n as represented in Figure 3.2, which begins at $t = t_0 = 0$, and ends at $t = T$, the end cycle voltage loop state equation is the solution of the state space

model differential equation over the period:

$$X_v[T] = e^{A_v T} X_v[0] + \int_0^T e^{A_v(t-\tau)} B_v u_v(t)\, dt \tag{4.22}$$

where the input command vector $u_v(t)$ is:

$$u_v(t) = \begin{cases} u_1 = \begin{bmatrix} 1 & V_{ref} \end{bmatrix}^t & \text{if } t \in [t_0, t_1] \text{ and } [t_3, t_4] \\ u_2 = \begin{bmatrix} 0 & V_{ref} \end{bmatrix}^t & \text{otherwise} \end{cases} \tag{4.23}$$

The sampling period, T_n, may be variable since the conduction cycle ends when the sliding function reaches zero from the positive subspace and does not depend on a fixed time-reference such as a reference clock. Due to jitters and various noise sources, the experimental steady-state switching period is variable but finite since a sliding-mode operation is assumed. Segmenting and solving the integral gives:

$$\begin{aligned} X_v[T] \;=\; & e^{A_v\left(T_{doff}+T_a+T_{don}+T_b\right)} X_v[0] \\ & + \left(e^{A_v T_{doff}} + e^{A_v T_b} - 2I\right) A_v^{-1} B_v u_1 \\ & + \left(e^{A_v T_{don}} + e^{A_v T_a} - 2I\right) A_v^{-1} B_v u_2 \end{aligned} \tag{4.24}$$

where I is the identity matrix. The On and Off-Time delays are assumed to be a known function of the phase filter output voltage, V_{pll}, considered when the sliding function reaches zero. The delay functions are discussed in 2.4.

2.2 Recurrence model of the phase regulation part

2.2.1 VCO phase recurrence equation

The phase error, $\Delta\Phi$, of the equivalent VCO is the reference phase, Φ_r, minus the converter phase, Φ_c:

$$\Delta\Phi[t] = \Phi_r[t] - \Phi_c[t] \tag{4.25}$$

Over one switching cycle, the converter phase increase is one period, i.e. 2π. The reference clock phase increase is the ratio between the switching cycle, T, and the reference

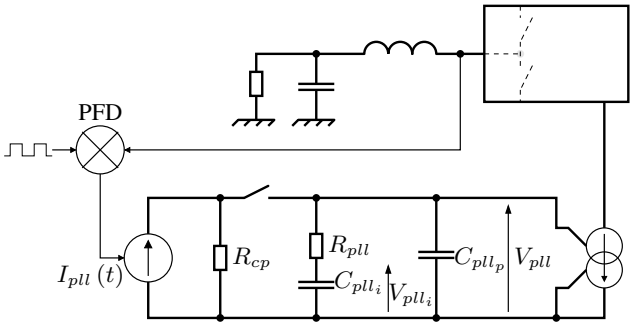


Figure 4.4 – Phase loop filter and charge pump model

period, T_r, multiplied by 2π. Then the end cycle phase error is:

$$\Delta\Phi[T] = \Delta\Phi[0] + \frac{T - T_r}{T_r} 2\pi \tag{4.26}$$

If the converter phase speed is lower than that of the reference phase one, the switching cycle period, T_n, is longer than the reference one and the phase error becomes positive. The converter operates with a phase delay with respect to the reference clock. Otherwise if the converter phase speed is higher than that of the reference clock one, the switching period is then smaller than the reference period. The phase error becomes negative and the converter operates in phase advance with respect to the reference clock. Notice that it is useful for linearisation calculus to determine the phase error at t_3 when the PFD may generates a pulse:

$$\begin{aligned} \Delta\Phi[t_3] &= \Delta\Phi[0] + \frac{T_{doff} + T_{don} + T_a}{T_r} 2\pi \\ &\quad - \frac{T_{doff} + T_{don} + T_a}{T} 2\pi \end{aligned} \tag{4.27}$$

2.2.2 Phase filter model

The proposed model of the phase loop filter and the charge pump is represented in Figure 4.4. The charge-pump circuit is modelled by a controlled current source, $I_{pll}(t)$, and a resistive output impedance, R_{cp}. The output impedance corresponds to the DC characteristic of the charge pump, i.e the current source accuracies. The state-space model of the phase-loop of the converter depends on the charge pump connection and

is:

$$\dot{X}_{pll} = \begin{cases} A_{pll_0} X_{pll} & \text{if disconnected} \\ A_{pll_1} X_{pll} + B_{pll_1} u_{pll} & \text{otherwise} \end{cases} \tag{4.28}$$

with:

$$A_{pll_0} = \begin{bmatrix} \frac{-1}{R_{pll} C_{pll_p}} & \frac{1}{R_{pll} C_{pll_p}} \\ \frac{1}{R_{pll} C_{pll_i}} & \frac{-1}{R_{pll} C_{pll_i}} \end{bmatrix} \tag{4.29}$$

and

$$A_{pll_1} = \begin{bmatrix} \frac{-1}{C_{pll_p}} \left(\frac{1}{R_{cp}} + \frac{1}{R_{pll}} \right) & \frac{1}{R_{pll} C_{pll_p}} \\ \frac{1}{R_{pll} C_{pll_i}} & \frac{-1}{R_{pll} C_{pll_i}} \end{bmatrix} \tag{4.30}$$

and

$$B_{pll_1} = \begin{bmatrix} \frac{I_{pll}}{C_{pll_p}} \\ 0 \end{bmatrix} \tag{4.31}$$

and

$$X_{pll} = \begin{bmatrix} V_{pll} \\ V_{pll_i} \end{bmatrix} \tag{4.32}$$

the input vector, u_{pll}, represents the switching state of the charge pump and can be either, 1 or -1.

2.2.3 Phase delay operation

If the converter operates with a delay with respect to the reference clock, the charge pump delivers a positive current to the filter during the interval $t \in [t_{up}, t_3]$. This operation mode is presented in Figure 4.5. The phase-filter state-vector equation at the rising edge of the PFD is:

$$X_{pll}\left[t_{up}\right] = e^{A_{pll_0}\left(T_{doff} + T_a + T_{don} - \frac{\Delta\Phi[t_3]T_r}{2\pi}\right)} X_{pll}\left[0\right] \tag{4.33}$$

Using the state-space model in (4.28) when the charge pump is connected gives:

$$\begin{aligned} X_{pll}\left[t_3\right] &= e^{A_{pll_1} \frac{\Delta\Phi[t_3]T_r}{2\pi}} X_{pll}\left[t_{up}\right] \\ &\quad + \int_{t_{up}}^{t_3} e^{A_{pll_1}(t-\tau)} B_{pll_1} dt \end{aligned} \tag{4.34}$$

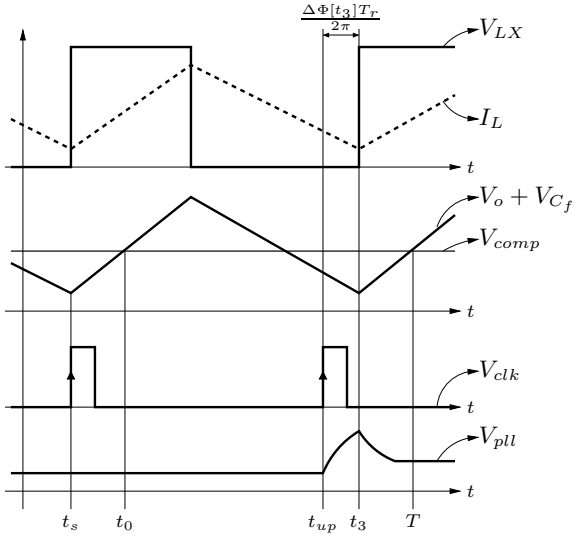


Figure 4.5 – Phase loop operation - phase delay

Solving the integral and developing terms give:

$$\begin{aligned} X_{pll}\left[t_3\right] &= e^{A_{pll_0}\left(T_{doff}+T_a+T_{don}\right)+\left(A_{pll_1}-A_{pll_0}\right)\frac{\Delta\Phi[t_3]T_r}{2\pi}} \\ &\quad \times X_{pll}\left[0\right]+\left(e^{A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}}-I\right)A_{pll_1}^{-1}B_{pll_1} \end{aligned} \tag{4.35}$$

Then the system follows the state space equations of the disconnected mode:

$$\begin{aligned} X_{pll}\left[T\right] &= e^{A_{pll_0}T_b}X_{pll}\left[t_3\right] \\ &= e^{A_{pll_0}T+\left(A_{pll_1}-A_{pll_0}\right)\frac{\Delta\Phi[t_3]T_r}{2\pi}}X_{pll}\left[0\right] \\ &\quad +e^{A_{pll_0}T_b}\left(e^{A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}}-I\right)A_{pll_1}^{-1}B_{pll_1} \end{aligned} \tag{4.36}$$

(4.37) is used to describe the recurrence equation of the phase filter state-space model in the sampled-data model when the converter switches at lower frequency than the reference clock.

2.2.4 Phase advance operation

In that case the charge pump circuit sinks a constant current between the power-stage output rising edge and the clock rising edge, i.e. $t \in [t_3, t_{dn}]$. This operation mode is

represented in Figure 4.6. The phase-filter state vector equation at the rising edge of the power-stage output is:

$$X_{pll}\left[t_3\right] = e^{A_{pll_0}\left(T_{doff}+T_a+T_{don}\right)} X_{pll}\left[0\right] \tag{4.37}$$

The same methodology applies for phase advance operation as for the phase delay operation:

$$\begin{aligned} X_{pll}\left[t_{dn}\right] &= e^{-A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}} X_{pll}\left[t_3\right] \\ &\quad - \int_{t_3}^{t_{dn}} e^{A_{pll_1}(t-\tau)} B_{pll_1} dt \end{aligned} \tag{4.38}$$

Notice that the phase error is negative. This justifies the minus sign that permits to recover a positive amount of time. Solving the integral gives:

$$\begin{aligned} X_{pll}\left[t_{up}\right] &= e^{-A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}} X_{pll}\left[t_3\right] \\ &\quad - \left(e^{-A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}} - I\right) A_{pll_1}^{-1} B_{pll_1} \end{aligned} \tag{4.39}$$

Then the end-cycle PLL filter state-vector becomes:

$$\begin{aligned} X_{pll}\left[T\right] &= e^{A_{pll_0}\left(T_b+\frac{\Delta\Phi[t_3]T_r}{2\pi}\right)} X_{pll}\left[t_{up}\right] \\ &= e^{A_{pll_0}T+\left(A_{pll_0}-A_{pll_1}\right)\frac{\Delta\Phi[t_3]T_r}{2\pi}} X_{pll}\left[0\right] \\ &\quad -e^{A_{pll_0}\left(T_b+\frac{\Delta\Phi[t_3]T_r}{2\pi}\right)} \\ &\quad \left(e^{-A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}} - I\right) A_{pll_1}^{-1} B_{pll_1} \end{aligned} \tag{4.40}$$

(4.40) is used to describe the recurrence equation of the phase filter state-space model in the sampled-data model when the converter switches at higher frequency than the reference clock.

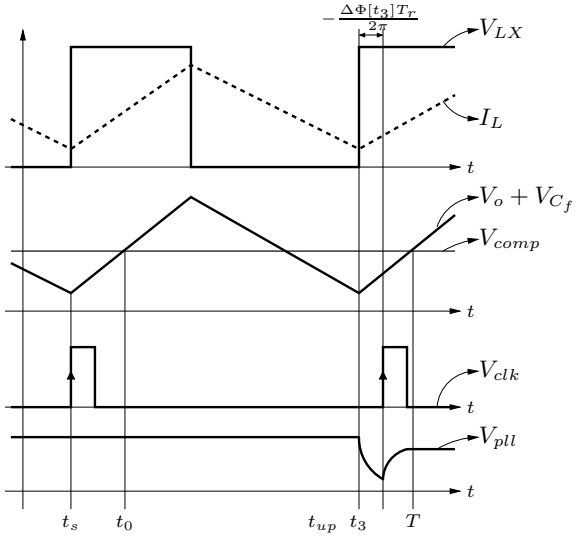


Figure 4.6 – Phase loop operation - phase advance

2.2.5 Steady-state limit operation

A small deviation in the steady-state boundaries is considered for stability analysis. It can be shown that:

$$\lim_{\Delta\Phi[t_3]\to 0^+} X_{pll}\left[T\right] = \lim_{\Delta\Phi[t_3]\to 0^-} X_{pll}\left[T\right] \tag{4.41}$$

and

$$\begin{aligned}\left.\frac{\partial X_{pll}\left[T\right]}{\partial \Delta\Phi\left[t_3\right]}\right|_{\Delta\Phi[t_3]>0} &= \left(A_{pll_1} - A_{pll_0}\right)\frac{T_r}{2\pi}e^{A_{pll_0}T + \left(A_{pll_1}-A_{pll_0}\right)\frac{\Delta\Phi[t_3]T_r}{2\pi}}X_{pll}\left[0\right] \\ &\quad + e^{A_{pll_0}T_b}A_{pll_1}\frac{T_r}{2\pi}e^{A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}}A_{pll_1}^{-1}B_{pll_1}\end{aligned} \tag{4.42}$$

and

$$\begin{aligned}\left.\frac{\partial X_{pll}\left[T\right]}{\partial \Delta\Phi\left[t_3\right]}\right|_{\Delta\Phi[t_3]<0} &= \left(A_{pll_0} - A_{pll_1}\right)\frac{T_r}{2\pi}e^{A_{pll_0}T + \left(A_{pll_0}-A_{pll_1}\right)\frac{\Delta\Phi[t_3]T_r}{2\pi}}X_{pll}\left[0\right] \\ &\quad - A_{pll_0}\frac{T_r}{2\pi}e^{A_{pll0}\left(T_b + \frac{\Delta\Phi[t_3]T_r}{2\pi}\right)}\left(e^{-A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}} - I\right)A_{pll_1}^{-1}B_{pll_1} \\ &\quad + e^{A_{pll_0}\left(T_b + \frac{\Delta\Phi[t_3]T_r}{2\pi}\right)}A_{pll_1}\frac{T_r}{2\pi}e^{-A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}}A_{pll_1}^{-1}B_{pll_1}\end{aligned} \tag{4.43}$$

(4.37) and (4.40) related time derivatives are expressed in (4.42) and (4.43) respectively. Furthermore assuming that R_{cp} is larger than R_{pll} (R_{cp} is modelled to allow A_{pll_1} inversion), then $A_{pll_1} \approx A_{pll_0}$ and:

$$\lim_{\Delta\Phi[t_3]\to 0^+} \frac{\partial X_{pll}\left[T\right]}{\partial \Delta\Phi\left[t_3\right]} = \lim_{\Delta\Phi[t_3]\to 0^-} \frac{\partial X_{pll}\left[T\right]}{\partial \Delta\Phi\left[t_3\right]} \tag{4.44}$$

(4.44) shows that assuming a small phase error, the phase advance or delay operations can be modelled by the same set of recurrence equations **without significant error**. In the following the phase delay equation expressions are retained. Conclusion are similar when working with phase advance expressions.

2.3 Hitting conditions

The recurrence equation system is under-determined due to the two delay variables: T_{don} and T_{doff}. Therefore hitting equations are used to obtain an equal number of equations and variables. The sliding surface is reached at t_2 and T such that the hitting conditions can be gathered in a single matrix equation:

$$0 = SX_v\left[t_2\right] \tag{4.45}$$

$$0 = SX_v\left[T\right] \tag{4.46}$$

Then the hitting conditions can be gathered in a single matrix equation:

$$\begin{aligned} \left[0\right]_{2,1} &= \begin{bmatrix} SX_v\left[t_2\right] \\ SX_v\left[T\right] \end{bmatrix} \\ &= \begin{bmatrix} g_1\left(X_v\left[0\right], X_f\left[0\right], \Sigma\left[0\right]\right) \\ g_2\left(X_v\left[0\right], X_f\left[0\right], \Sigma\left[0\right]\right) \end{bmatrix} \end{aligned} \tag{4.47}$$

Determining the voltage-loops' state vector at the first hitting instant, t_2:

$$X_v\left[t_2\right] = e^{A_v\left(T_{doff}+T_a\right)} X_v\left[0\right] + \int_0^{t_2} e^{A_v(t-\tau)} B_v u_v\left(t\right) dt \tag{4.48}$$

solving the integral results in:

$$\begin{aligned} X_v\left[t_2\right] &= e^{A_v\left(T_{doff}+T_a\right)}X_v\left[0\right] \\ &+ \left(e^{A_vT_{doff}} - I\right)A_v^{-1}B_vu_1 \\ &+ \left(e^{A_vT_a} - I\right)A_v^{-1}B_vu_2 \end{aligned} \tag{4.49}$$

(4.49) is then used in (4.47) to solve for g_1.

2.4 Switching loop delay model

The switching delays dependent on the phase filter output voltage. They characterise the effect of the phase-loop on the voltage-loops. For accurate modelling, expressions are fitted with post-layout simulations and open-loop measurement results. Delay functions differ from (3.39) and (3.40) mainly because of model approximations and the operation region of the transistors. Thereby proposed fitted delay expressions are:

$$T_{doff} = a_de^{b_dV_{pll}[0]} + c_de^{d_dV_{pll}[0]} \tag{4.50}$$

$$T_{don} = a_ue^{b_uV_{pll}[t_2]} + c_ue^{d_uV_{pll}[t_2]} \tag{4.51}$$

where a_d, b_d, c_d, d_d and a_u, b_u, c_u, d_u are fitting parameters. Assuming that $X_{pll}\left[n\right]$ is known, the phase loop filter state vector at t_2 follows:

$$X_{pll}\left[t_2\right] = e^{A_{pll_0}\left(T_{doff}+T_a\right)}X_{pll}\left[0\right] \tag{4.52}$$

The phase loop filter output voltage is then:

$$\begin{aligned} V_{pll}\left[t_2\right] &= \begin{bmatrix} 1 & 0 \end{bmatrix} X_{pll}\left[t_2\right] \\ &= \begin{bmatrix} 1 & 0 \end{bmatrix} e^{A_{pll_0}\left(T_{doff}+T_a\right)}X_{pll}\left[0\right] \end{aligned} \tag{4.53}$$

($V_{pll}\left[t_2\right]$) is used in (4.51) in order to determine the variable delay of the comparator.

3 Initial state determination

Due to the system non-linearities, the Jacobian matrix depends on the initial state vector. The initial state determination is performed using an open-loop iterative process as presented in Figure 4.7. The initial state must comply with frequency and voltage steady-state values and sliding-mode initial function (i.e. $SX_v\left[0\right] = 0$). Two assumptions are proposed:

1. No initial phase loop dynamic: the converter operates steadily at the desired switching frequency. The phase-loop charge-pump remains in tri-state condition and the voltage across both phase filter capacitors are equal.

2. An average output voltage error that complies with $\overline{v}_o = V_{ref} - \lambda\overline{I}_o$. This models the DC load regulation caused by the finite gain of the compensation function amplifier.

Under assumption #1, the frequency control steady-state current is found using the static VCO characteristic of the voltage regulator. The corresponding control voltage is then determined thanks to the voltage-controlled current-source reverse characteristic. Finally the frequency loop state-vector is determined by $V_{pll_i}\left[0\right] = V_{pll}\left[0\right]$ and $\Delta\Phi\left[0\right] = 0$. This calculation is performed with a dichotomous algorithm as presented in Figure 4.7. Once the initial frequency-loop state-vector is determined, the time delays are computed using the converter delay characteristics.

The second part of the initial state determination aims to find the values of $X_v\left[0\right]$ and λ that come from assumption #2:

$$\begin{cases} \overline{v}_o = V_{ref} - \lambda\overline{i}_o \\ SX_v\left[0\right] = 0 \end{cases} \tag{4.54}$$

The possible values of λ are bounded by 0 at the lower end. In that case, there is no load regulation phenomenon, i.e. the average output voltage exactly matches the reference voltage, and the compensation function presents an infinite DC open loop gain. The upper bound is arbitrarily set to R_o. This last case implies that the output voltage is half the desired one. Its quite far from conventional solutions but additional computation

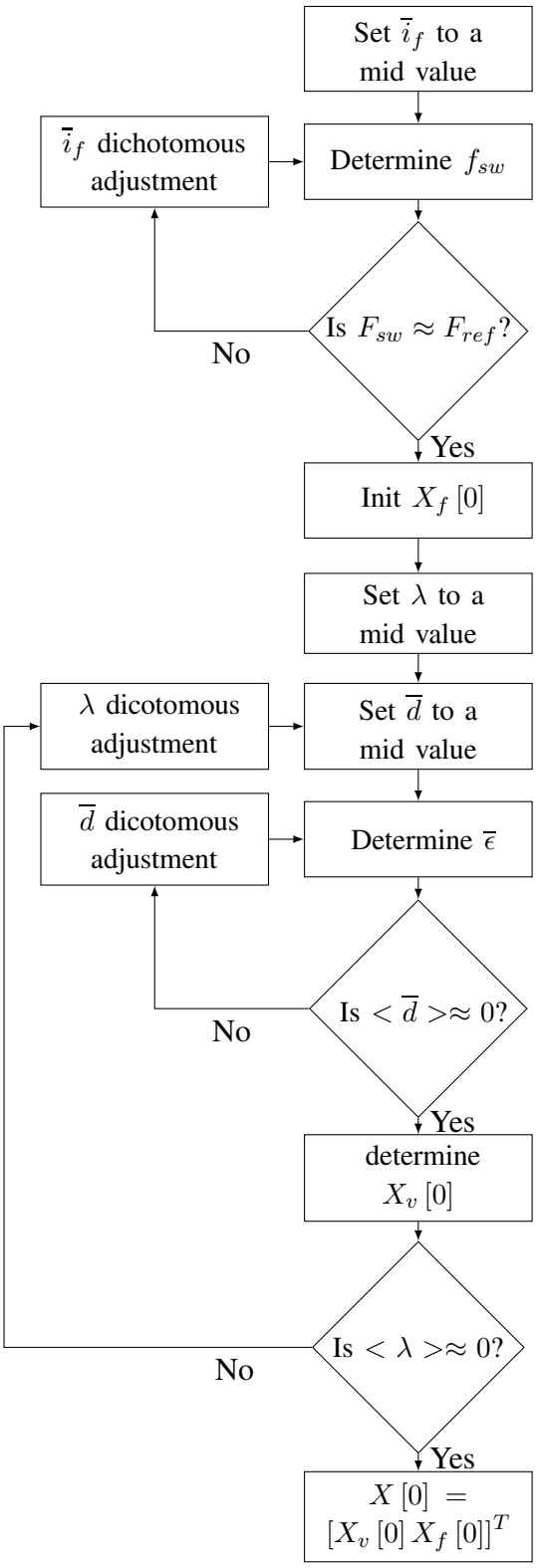


Figure 4.7 – Initial state determination flow

time is low. The corresponding converter duty-cycle is computed using a dichotomous algorithm and the λ confidence interval width, $< \lambda >$, is checked. Depending on the sliding-mode hitting condition, λ is adjusted and the confidence interval reduced.

4 Discussion wrap-up

Experimental validation and results for the proposed stability analysis are presented in chapter 6. Nevertheless the methodical aspects present several interesting points:

Advantages of the proposed methods The key advantage of the proposed method is to handle cross interactions. This allows the designer to investigate full multi-variable control that does not follow the non-interaction criterion and extends the regulation bandwidth of booth loops. The MIMO model appears to be a promising concept to model the inner loop to perform the latter control. Furthermore the converter non-linearities are modelled prior to linearisation. This permits to expect a better model of the intrinsic non-linear structure of the converter.

Limitations This methods remains a local stability analysis and its robustness is not guaranteed for large perturbations. It is difficult to estimate the validity domain of a small displacement of the initial state vector. The sliding-mode theory provides some tools such as the reaching domain concept where the converter converges to the sliding surface. This assumption seems to be a good one since during the reaching phase the phase loop will decrease the comparison time delay[2]. However a sliding mode model of the full voltage part is required to determine this reaching domain.

iterative Relative Gain Array Quantification of the cross interactions between the voltage and the frequency loops remains an uncovered topic so far. Relative Gain Array (RGA) and iterative Relative Gain Array (iRGA) matrices are approaches to quantify cross-interactions between mixed loops [9, 13]. However they are so far applicable to

[2]no switching will occur during the reaching time and the phase error is in fact expected to increase

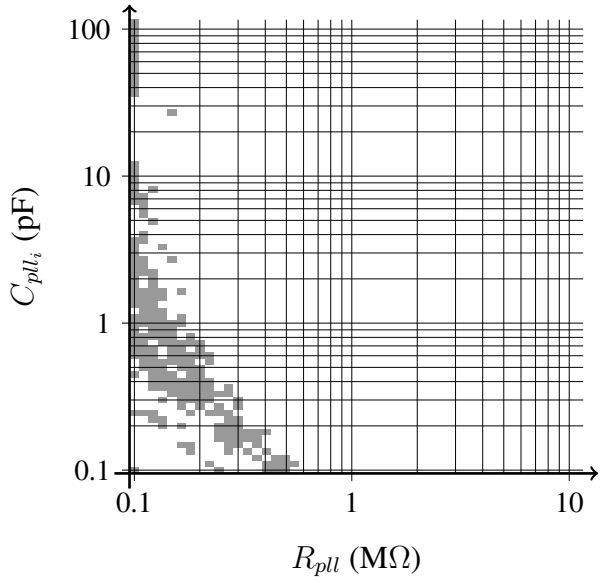


Figure 4.8 – iRGA map of the proposed DC/DC converter versus R_{pll} and C_{pll_i}

continuous models or averaged systems. Indeed RGA is used with a discrete time model in [117] nevertheless the switching frequency is constant. The validity of such a tool remains to explore for the variable-frequency sampled time domain. A preliminary calculation has been performed applying the iRGA as if the problem was with constant switching frequency. The iterative aspect means that RGA is applied repetitively until an asymptotic indication of cross correlation or not. Figure 4.8 pictures the result of the latter calculation where grey dots indicates the R_{pll}, C_{pll_i} settings for which the iRGA indicates a significant cross-correlation between loops. It may be observed that this area of significant cross-correlation is relatively small. The assumption of low cross correlation between loops is of importance from design point of view as each loop can be optimized separately.

Chapter 5

CMOS design

This chapter presents the main engineering constraints that are specific to the proposed solution. A voltage-mode PWM solution is taken as reference point (and referred as PWM).

The first prototype of the proposed controller (codename, Baby NoLiE) is embedded in a pre-commercial Analog-Baseband (AB) test-chip using a CMOS 130 nm double-oxide process by ST-Microelectronics and is presented in Figure 5.1. It drives a standard 2 A power stage that intends to supply the 1.8 V power rail of the mobile phone platform. Only Continuous Conduction Mode (CCM) is supported by this early demonstrator that has been manufactured at the end of the first year of this thesis. It embeds the proposed sliding mode modulator plus a phase loop circuitry. Furthermore the start-up strategy has been successfully tested on this early demonstrator. As a constraint the prototype is pin-to-pin compatible with the standard PWM controller from ST-Ericsson.

Although functional this early demonstrator is not developed hereafter. A second prototype shares the same package and test-environment as the first one but extends the features of the controller and solves minor defects. It embeds an improved Phase Locked Loop (PLL) circuitry, new sliding-mode modulator active elements and a Discontinuous Conduction Mode (DCM) handler. DCM control is implemented in order to maintain a good efficiency over the full load range. The SMPS prototype drives a 2 A standard power stage in which a part as low as a quarter of the MOSFETs is used to maximize low load efficiency. The controller design is detailed in this chapter. The design of the

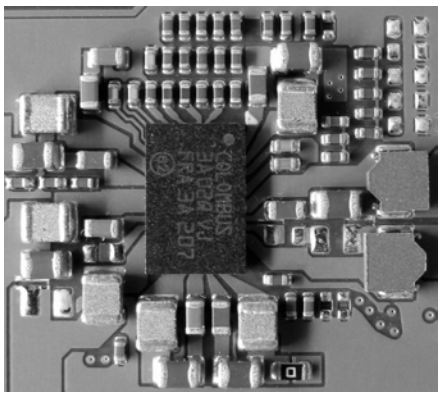


Fig. 5.1 – First test-chip

power stage is not covered in this thesis since it is a standard and commercial Intellectual Property (IP). The whole converter layout is presented in Figure 5.2. The three loop controller total silicon area is 0.185 mm^2 and the phase locked loop circuitry requires less than 0.022 mm^2 making it sufficiently small to be integrated without significant impact on the die cost.

The controller architecture is subdivided in elementary blocks that have been separately designed. The chosen subdivision is as follow:

- the sliding-mode modulator comprises the inner loop control function with the variable delay comparator and the outer compensation loop with the error amplifier.
- the start-up circuitry sequences the power-on of the whole circuit.
- the gate control generator is made up of few logic gates and a digital glitch filter that eliminates the possible noise from the sliding mode modulator.
- the DCM handler determines the conduction mode and generates the required control signals when DCM operation is preferred.
- the Phase Locked Loop synchronization circuit comprises the Phase Frequency Detector (PFD), the charge pump, the phase-loop filter and the voltage-to-current converter.

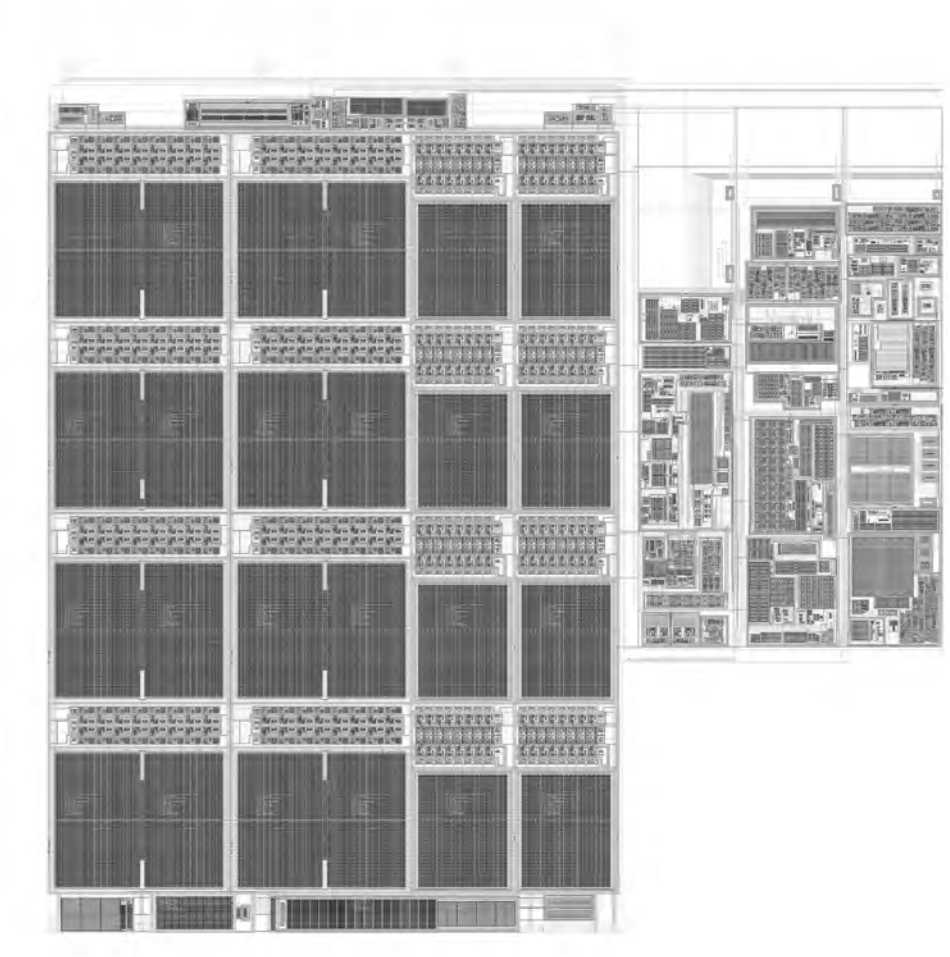


Figure 5.2 – DC/DC converter layout (code name Little NoLiE

- the reference voltage and current block that adapts the impedance of the on chip reference source for the control internal circuits. This block reuses an existing voltage amplifier mounted in a voltage-follower configuration and several current mirrors that generate the biasing current references for each sub-bloc from the main current reference. The latter block reuses also existing circuits.

Except standard circuits, each block is described now.

The test environment is described also. First the test-board set-up used to validate the operations of the whole prototype is described. This board has been designed prior to the thesis and optimized for short design time. Second a specific load transient test board that can handle high current and fast transients, has been designed to validate the fast transient capability of the proposed solution. Third, in order to perform correct FFT analysis of the switching frequency a high frequency low-pass filter that uses discrete components has been designed too. However test environment limitations are still partial causes of some unexplored features of the proposed solution such as the power input to output characteristics of the converter (line-regulation, PSRR etc. . .).

1 Synchronized Sliding-mode modulator

The sliding-mode modulator gathers the voltage compensation function, the current emulation circuit, and the inner-loop comparator. The latter is extensively developed in section 2.1 however a Design-For-Test (DFT) biasing scheme is detailed in this part. **The current-control of the switching frequency of the converter is a key-point of this thesis. Hence measurement of the open-loop current-to-frequency characteristic is required.** The voltage compensation function is built around an operational amplifier that was designed to solve specific issues of the proposed DC/DC converter. **The amplifier has a lower gain-bandwidth characteristic than its PWM counterpart because the compensation function is no-longer a PID function. Nevertheless power supply rejection of the amplifier is one of the key-specification for noise-immunity issues.** The amplifier design is developed hereafter also.

1.1 Inner loop comparator design

Figure 5.3 presents the comparator biasing scheme and the whole comparator layout is presented in Figure 5.4. (M_1, M_2) is the differential pair that operates in subthreshold region as described in section 2.1. In order to characterise the comparator current-to-delay function, the differential pair bias scheme incorporates a digitally controllable current source (DAC). The cascoded current-mirrors (M_9, $M_{9,1}$, $M_{9,2}$, $M_{9,3}$, $M_{9,4}$, $M_{9,5}$) and the switches N0 to N3 form the DAC that represents more than half the total comparator silicon area. Cascoded operation is preferred for accuracy. Switches activate the associated branch current. Each branch delivers a multiple of the reference branch current in order to convert the digital input word into a proportional current. The general bias block provides the reference current through the pin I_{ref}. The cascoded current mirror (M_{12},M_{13},M_{14}) copies the reference current in order to bias the DAC.

The variable bias current coming from the phase-locked-loop circuit flows through the pin I_b and is copied out by the current mirror (M_{10}, M_{11}). The switch ANA deactivates the phase-loop current action in order to characterise the open-loop current-to-frequency transfer function.

An analog blanking-mask is inserted between the comparator and the power-stage in order to avoid glitches and to extend the noise immunity of the inner-loop. A high frequency ringing or pulse might be present inside the chip when the power stage switches. This undesired noise is not totally rejected at the output of the error amplifier due to a finite amount of high frequency PSRR and can trigger the comparator again.

1.2 Voltage compensation amplifier

The DC/DC voltage error amplifier is designed to perform the outer-loop compensation function as defined in section 3.2. Moreover most of its characteristics influence the DC/DC converter performances. Thus it complies with the following requirements:

- sufficiently large bandwidth in order to accurately perform the compensation function
- low offset because the amplifier offset sets the DC/DC offset

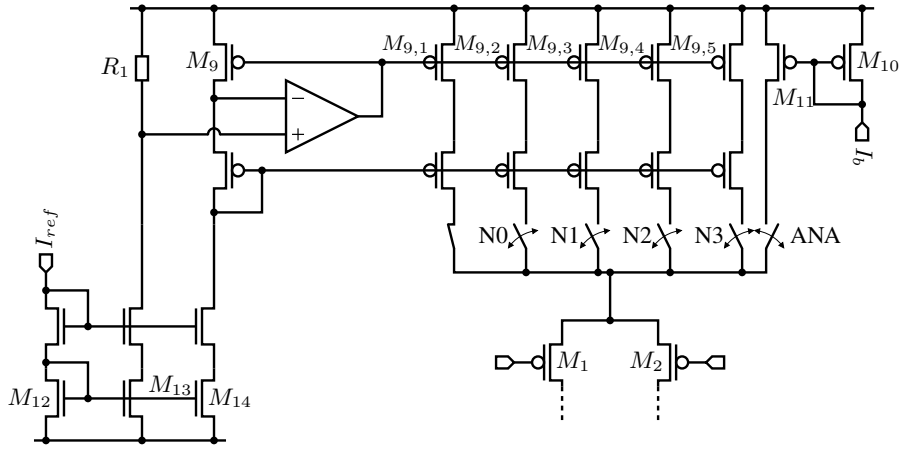


Figure 5.3 – Biasing scheme of the variable delay comparator

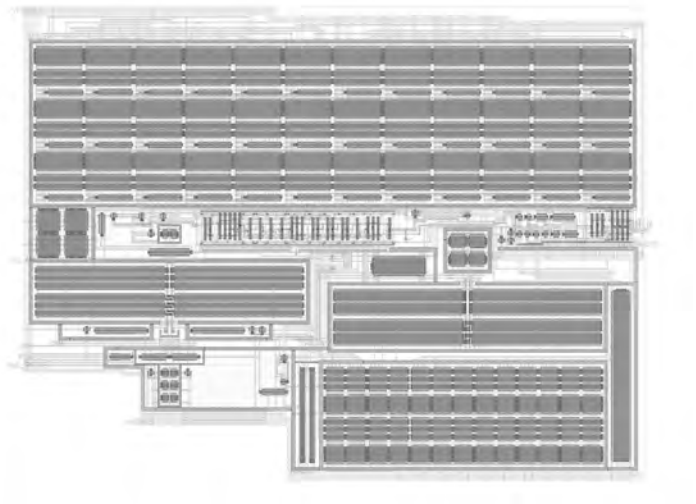


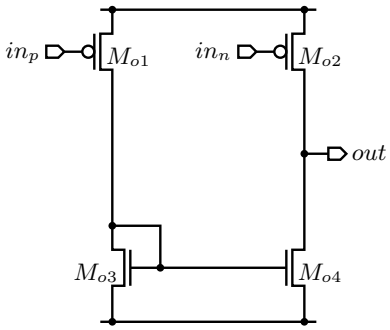
Figure 5.4 – Variable delay comparator layout

- high DC gain in order to increase the converter DC accuracy and to compensate steady-state error
- high Power Supply Rejection Ratio (PSRR) not only when dealing with positive supply rail perturbations (PSRR+) but also when the ground supply is noisy (PSRR-)

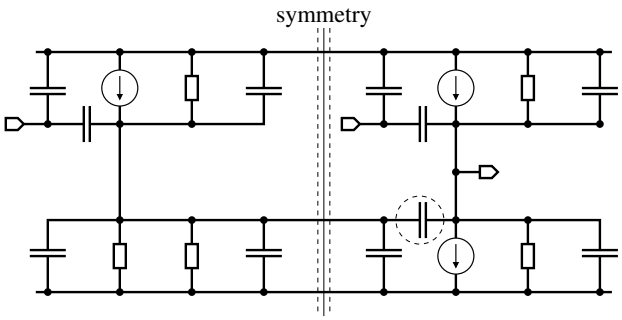
The requirements are common in CMOS design and the PSRR- requirement is the most challenging. The inner-loop slides along the sliding surface with fast response time and unity gain. A small undesired change in the compensation voltage leads to a similar change in the output voltage. Switching in DC/DC converter generates ground and substrate noise among other side-effects. If it is not properly rejected, it can generate unwanted switching action that produces ground and substrate noise. This closed-loop phenomenon can lead to the converter instability. A digital glitch filter included in the gate control block and a careful amplifier design and layout solve this issue.

In this way the chosen amplifier topology is based on a differential common-source architecture presented in Figure 5.5a and used as the output stage. The two matched P-MOSFETs, M_{o1} and M_{o2}, amplify the input differential signal, $in_p - in_n$. The N-MOSFET current-mirror, (M_{o3}, M_{o4}), copies the drain current of M_{o1} to the output such that the output pin current is the differential input voltage amplified by the P-MOSFET transconductance. Equivalent small signal schematic is presented in Figure 5.5b. The structure is symmetrical with the exception of the circled gate-drain capacitance of M_{o4}. Power or ground rail noise is a common mode noise that identically applies to the symmetric branches and the higher the symmetry the higher the common-mode rejection. Each independent branch presents the poor PSRR of a common-source amplifier. Nevertheless the transmitted noise is suppressed when the differential signal is converted into a single ended operation at the currents summation. In order to increase the overall gain and symmetry, each transistor is used in a cascode configuration. The output stage is no-longer fully linear for output voltages below 0.7 V. However the transistor M_{o4} remains in saturation while the output voltage is higher than an "overdrive" voltage increment[1] (i.e. ≈ 100 mV). Thereby good performance is maintained for the most of

[1]To guarantee active region operation the gate of the MOSFET transistor is driven approximately 100 mV higher (overdrive) than the transistor threshold voltage, it is a design rule of thumb [39]



(a) Output stage principle - large signal schematic



(b) Output stage principle - small signal schematic

Figure 5.5 – Output stage principle schematics

the operating conditions where the output voltage is higher than 0.7 V. The output stage looses the benefit of the low side cascode when the digital-core enters is very low power conditions and the voltage is lower than 700 mV but it is still functional. No impact on the DC/DC converter behaviour has been detected during tests.

The designed amplifier structure that uses the above-mentioned output stage principle is presented in Figure 5.6 and simplified schematic is presented in Figure 5.7. The two first amplifier elements, (AE_1, AE_2), are designed based on a folded cascode structure that permits differential output voltage and presents good overall characteristics. The input stage is a P-MOSFET differential-pair in order to operate close to the ground rail. The amplifier is not designed for rail-to-rail input operation since the maximum common-mode input voltage is supposed to be below 1.5 V (the maximum requested output voltage) and the minimum battery voltage is higher than 2.3 V. One threshold ($\approx 0.6V$) plus two "overdrive" voltage increments ($\approx 2 \times 100$ mV) drops between the common-mode voltage and the power supply voltage is provided. That guarantees

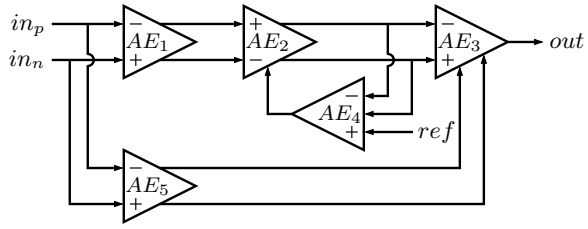


Figure 5.6 – Amplifier architecture

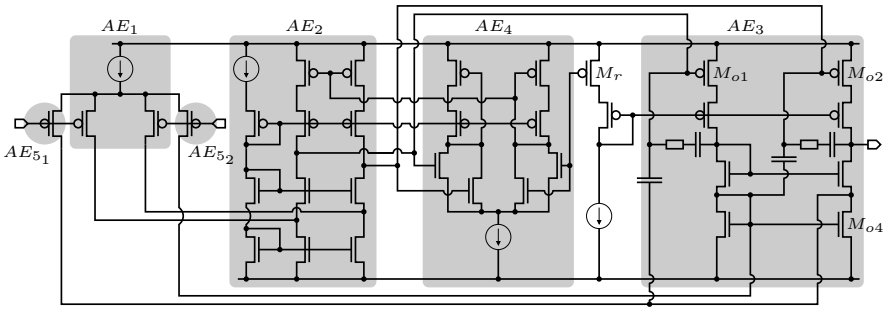


Figure 5.7 – Amplifier principle schematic

saturation operation of the transistors over the whole output voltage range.

Differential operation involves the use of a common mode feedback circuit which is the Amplifier Element 4 (AE_4), presented in Figure 5.6 and 5.7. It is built around a simple amplifier in which one input is divided in two parts in order to approximate the common mode voltage. It controls the folded-cascode bias current such that the output stage gain transistors, M_{o1} and M_{o2}, have the same common-mode gate-source voltage as the reference transistor, M_r. Matching the three transistors (M_{o1}, M_{o2}, M_r) yields the same current densities and the bias current of the reference-MOSFET, M_r, bias current controls the output stage .

Last a feed-forward stage, AE_5, extends the amplifier bandwidth. It consists in a differential pair, (AE_{5_1}, $AE_{5,2}$), in parallel with the first amplifier-element input pair that directly changes the output stage bias point. The feed-forward path, (AE_5, AE_3), provides fast response at the expense of a low gain while the main path, (AE_1, AE_2, AE_3), provides high gain and accuracy.

The amplifier layout it presented in Figure 5.8. A particular care has been taken to the differential line layout and the transistor matching. According to the team layout

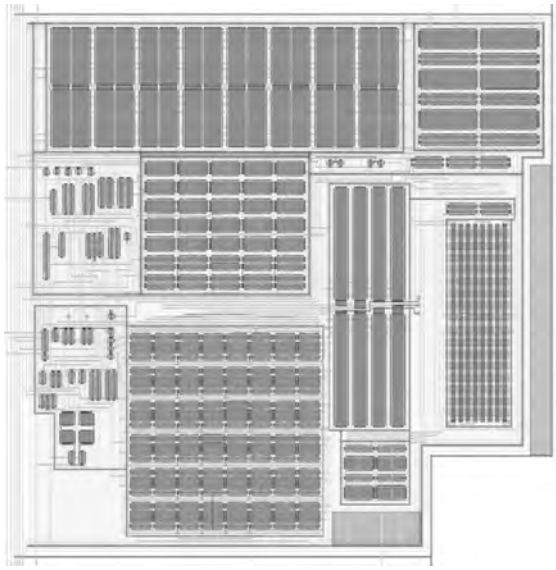


Figure 5.8 – Layout of the error amplifier

methodology, dummy elements are used to fill the matching matrices' free-spaces but no surrounding dummies have been used to increase the elements' matching.

2 Phase-locked-loop

The phase-locked-loop circuit uses only common circuit from frequency synthesis domain. In order to keep the passive filter area small, the charge-pump output current is set as low as possible, i.e. 1 μA. The cutoff capacitor value, C_{pll_p}, is in the range of a pF and charge injection during switching operation, i.e. when the charge pump switches from high impedance to sink or source current or vice versa is an issue with such low current and small capacitor. Charge-injection presented in Figure 5.9 results in an unwanted current flow through the phase filter that generates undesirable oscillator control noise. A careful design of the charge-pump is required to minimise the phase noise that results from the charge injection phenomenon. In addition the voltage-to-current input capacitance may lead to a non-negligible shift between the desired phase cut-off capacitor value, C_{pll_p}, and the practical one. Thus a small input capacitance voltage buffer drives the voltage-controlled current source. **The PLL filter capacitor is small in order to keep its silicon area negligible. This choice constraints the charge-pump current**

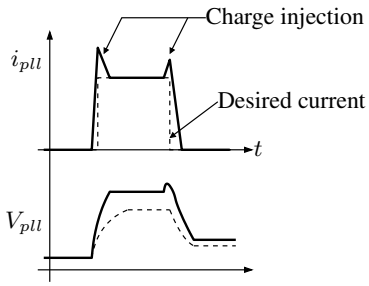


Figure 5.9 – Charge-injection of the charge pump circuit

to a low value and should have consequences on the phase noise of the frequency regulated converter. However the phase noise of the converter is not a real issue at system level and can be neglected. In start-up conditions the phase control voltage is pulled to the battery voltage in order to minimise the delay through the comparator. This decreases the instantaneous switching frequency but the phase locked loop recovers its steady-state operation after a non-linear reaching phase. This typical behaviour of a PLL is visible in Figures D.21 and D.22.

3 Discontinuous-Conduction-Mode

One objective of this thesis is to demonstrate the feasibility of a sliding-mode based controller that supports Discontinuous Conduction Mode (DCM) operation. The main challenge is to take into account the asynchronous nature of the controller that forbids reference-clock based operation. Inductor current sensing and switching node zero crossing detection are common methods to detect the inductor-current inversion phenomenon [5, 14, 118]. However the continuous detection of a small voltage requires a fast and accurate circuit that means large silicon area and bias current. A sensor-less digital controller method is used to optimize the inductor current zero-crossing point switching in [1]. This method minimizes the conduction timing error functions between the On-Time, the Off-Time and the High-Impedance-Time. Nevertheless the analog implementation of such an algorithm in a variable switching frequency context is inappropriate since it requires a fixed-time reference to compute the best operating point. The proposed system does not require a time-reference. Full asynchronous operation and mode switching is the main difference between the proposed solution and a standard

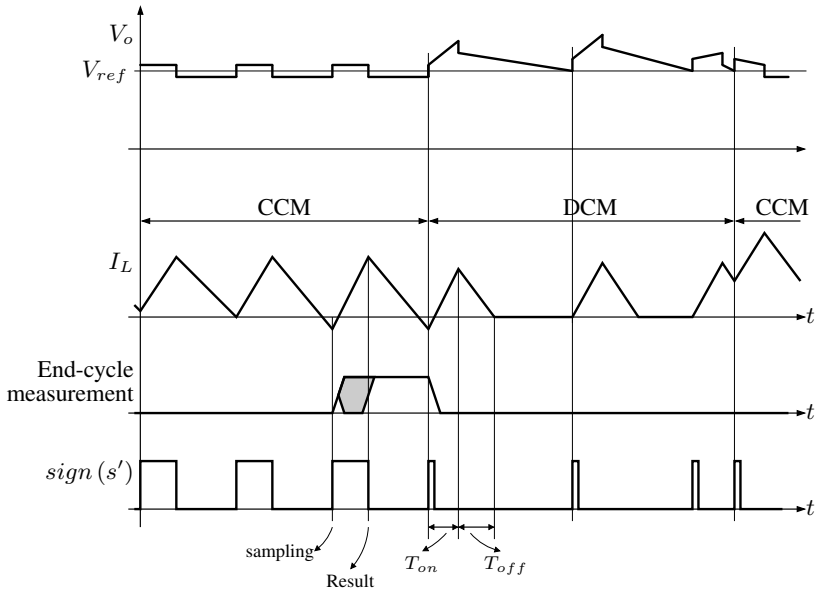


Figure 5.10 – Discontinuous conduction mode conduction cycle generator

PWM buck converter.

3.0.1 DCM control architecture

Timing diagram of the implemented solution is presented in Figure 5.10. It uses a proprietary end-of-cycle sensing circuit that samples the power bridge output voltage at the end of the conduction cycle when the converter operates in Continuous Conduction Mode (CCM). During the falling current phase, the power inductor current flows through the n-MOSFET which is mainly resistive. The sampled voltage is amplified and compared in order to determine if the end-of-cycle switching node voltage is negative (i.e. the inductor current is positive) or positive (i.e. the inductor current is negative). The end-of-cycle measurement system is designed such that the comparison result is valid for the modulation falling edge. Therewith a digital conduction-mode selection state-machine is synchronized on the sliding-mode rising-edge and determines the conduction-mode based on the sensor output.

Entering in DCM the inner loop comparator compares the current observer output

voltage to the input reference voltage. The sliding function s becomes:

$$s' = V_{ref} - V_{C_f} - V_o \tag{5.1}$$

The observer output voltage is close or equal to the output voltage while the power stage is in high impedance mode. Therefore the converter accuracy is kept good. Once the output voltage reaches the reference voltage, the comparator switches in high state and starts the DCM pattern generator that generates the On and Off conduction times (respectively, T_{on} and T_{off}) that permit to deliver a controlled amount of charge to the load. During DCM operation, the Phase-Locked-Loop circuit is deactivated and the converter operates with Pulse-Frequency-Modulation (PFM). Each time the output voltage reaches the reference voltage, the inner-loop comparator triggers the pattern generator that generates a conduction pattern. The output voltage increases.

Two DCM-to-CCM transition cases are distinguished. First the comparator triggers the DCM pattern generator while the power stage is not in high impedance mode as represented in Figure 5.10. Second the comparator pulse is wider than the On-Time, T_{on}. First condition means that two conduction patterns collide and the required output current is higher than the critical conduction one, i.e. when a cycle follows the previous cycle without high impedance duration. The second transition condition occurs when a large load transient requires a sudden increase in the load current.

A Mealy state-machine is used to implement the state transition algorithm. Unlike a synchronous Moore state-machine, the Mealy formal logic adds the asynchronous priority to the inner-loop comparator. The state machine uses the voltage regulation self-oscillation rising edge as a clock source. This guarantees a synchronized operation with the power conduction cycle. However setup and hold time conditions' compliance are not formerly guaranteed. Assuming that the duty-cycle does not reach high values when supplying a digital core, the falling-edge of the power modulation occurs some enough time before the next rising edge such that the end of cycle measurement is valid and the logic glue is set before the minimum register-flop setup time requirement. Asynchronous logic is a method that is well suited to handle such a problem [112]. However no asynchronous logic cells library was available during this thesis.

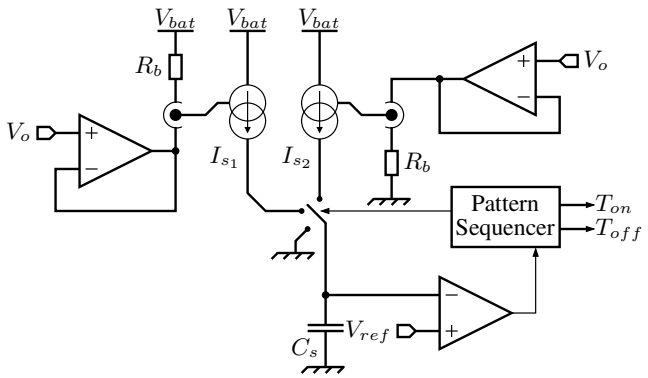


Figure 5.11 – Discontinuous conduction mode conduction cycle generator

3.0.2 DCM pattern generator

Once the discontinuous conduction mode occurs, the conduction pattern is generated by a proper module that emulates the inductor current as presented in Figure 5.11. An internal state machine which state transition diagram is presented in Figure 5.12, sequences the conduction subcycles, i.e. the On-conduction time, T_{on}, and the Off-conduction time, T_{off}. The sliding-mode comparator compares the output voltage to the reference voltage. When the output voltage is lower than required, the latter comparator triggers the pattern generator that starts the conduction cycle as presented in Figure 5.10. The pattern generator enters in state, E0. The power stage is pulled to the battery voltage and the high side current source, I_{s_1}, is activated and charges the current emulator capacitor, C_s. The voltage slope across the current emulator capacitor, C_s, is maintained proportional to the power inductor current, I_L, thanks to the current source, I_{s_1}. Once the current emulator capacitor voltage reaches the reference voltage, the DCM pattern generator comparator triggers the state-machine that enters in E1. During the state-transition, the capacitor C_s is discharged. While in state E1, the power bridge output is tied to the ground. The current source, I_{s_2}, is activated and the voltage across the capacitor, C_s, rises with a slope inversely proportional to the power inductor current slope. When the current emulator capacitor voltage reaches the reference voltage, the pattern generator comparator triggers the stage-machine that enters in E2. During the state-transition, the inductor current is zero thus the power half bridge output is set in high impedance mode.

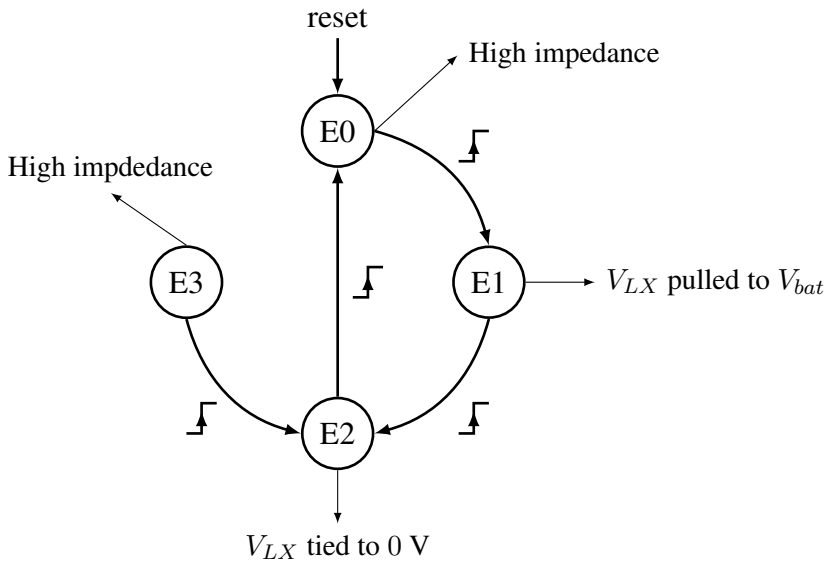


Figure 5.12 – DCM pattern sequencer state diagram

This circuit generates the On and Off-Time ratios that stops the conduction cycle when the inductor current is zero. The matching between the two resistors, R_b, sets the circuit accuracy since the capacitor, C_s, is shared for the rising slope and the falling slope emulation. Therefore current-balance reconstruction remains valid even with large process variation.

3.1 Start-up management

The sliding-mode DC/DC converter startup management faces to major design challenges. First the sliding-condition in (3.11) is not valid when the output voltage is zero. Second the voltage compensation function amplifier is not suitable for operation lower than 100 mV. Third the way to start the phase loop circuitry that synchronizes the DC/DC converter remains an open issue. **The first issue is new compared with a PMW converter. The average transfer function of a PWM converter is approximately linear and constant between 0 and 100 % duty cycle whereas the sliding-mode existence condition is not verified for extreme duty cycles and equation 3.15 is not applicable. The second issue is standard in CMOS design and the third is specific to the proposed circuit.**

The startup sequence of the circuit is decomposed in four phases as presented in Figure 5.13:

1. a digital computation phase: the digital circuits are resetted and the analog parts of the controller are biased but inactive

2. a so called "reaching" phase in which the reference voltage is positioned at[2] 100 mV: the comparator is fully biased in order to provide minimum time-delay and the outer voltage compensation loop integrator configuration is replaced by a reference follower configuration. The PLL starts its operations.

3. a so-called "rising" phase that follows the reaching phase: the reference voltage rises with a controlled slope.

4. a so-called "settling" phase succeeds to the rising phase when the output voltage is above the reference voltage minus a few tens of millivolts. The outer voltage compensation function is activated and the end-cycle inversion circuit is calibrated during a hundred cycles.

The inner loop does not operate in sliding-mode condition during the beginning of the reaching phase in Figure 5.13. However its trajectory remains bounded since the load is not powered and the only uncertain parameter is the battery voltage. Furthermore the reaching condition is valid since the compensation voltage[3] is higher than 0 V. Thereby once the converter reaches the sliding surface, it operates in sliding-mode if the T_{doff} condition in (3.12) is valid. This is ensured by pulling the switching frequency regulation filter to the battery voltage, V_{bat}. It follows thereby that the voltage controlled current source delivers its maximum current, hence the comparator delay is minimum.

During the "rising" phase, the reference rises thanks to a constant current charge of a capacitor. The inner-loop charges the output capacitor, C_o, in order to track the rising reference with a constant average current. While rising, the output voltage is compared against the steady-state requested voltage. When the output voltage is 10 mV below the targeted voltage, the converter enters in the "settling" phase. During the previous

[2] which is the amplifier minimum output voltage

[3] The compensation voltage follows the reference voltage which is set to 100 mV during this startup phase

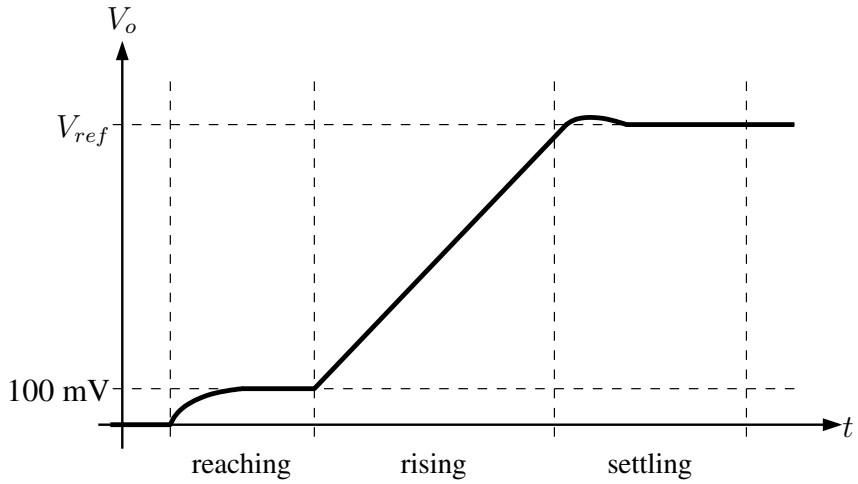


Figure 5.13 – Output voltage during startup

phases, the amplifier is connected in a follower configuration. The 10 mV margin helps to prevent small-output-voltage overshoots while the compensation function changes from a follower configuration to an integrator configuration. The ”settling” phase lasts a hundred cycles and is required to calibrate the zero-crossing detector that measures the power half bridge output voltage when a conduction cycle ends. Once the ”settling” phase finishes, DCM operation is allowed and startup operations ends.

4 Test tools

The designed test-chips are tested with a dedicated test environment. To overcome the standard test environment limitations , specific test boards have been designed during this thesis.

4.1 Circuit testability

To maximize the compatibility with the rest of the circuit in which the SMPS prototype is embedded, only digital registers are available for read and write operations. No invasive access to measure signals inside the circuit is implemented in order to maintain the internal regulation circuitry away from parasitic elements. Therefore only behavioural

external measurements were accessible, i.e. the output voltage, the power half bridge output, and the battery voltage.

In order to test the features of the controller as much as possible, elements can be configured through an I^2C. These elements are:

- The startup ramp slope
- The DCM pattern size
- The inner-loop current-observer time-constant, $R_f C_f$
- The outer-loop integration time constant, $R_i C_i$
- The phase locked loop pre-scaler value
- The phase locked loop post-scaler value
- The comparator digitally programmable bias current
- The phase locked loop filter set (C_{pll_i}, and R_{pll})
- The phase locked loop voltage to current converter gain

In addition the external reference can be set between 0.6 V and 1.55 V, with 5 mV steps and the reference clock phase from 0 to $\frac{7\pi}{4}$ with $\frac{\pi}{4}$ steps. These are common features of an AB.

4.2 Test board setup

An AB generic test setup structure is presented in Figure 5.14. The Device Under Test is soldered on a chip board that gathers the associated passive components. The chip board is then mounted on a specific socket which is soldered on the test motherboard. The motherboard gives access to the BGA device pins and ways to connect the power supplies. However the DC resistance between the laboratory power supply to the chip path has been measured at 500 mΩ for the battery power rail and 100 mΩ for the ground rail. These resistances degrade the measured DUT output characteristics since it adds a non-significant amount of line-to-output transfer ratio. For instance during a rising

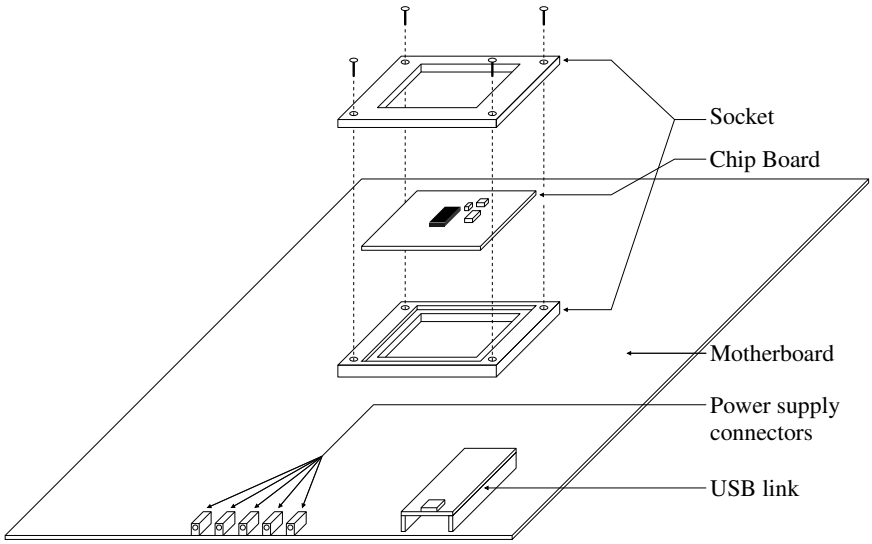


Figure 5.14 – Board-test setup for the AB family

load transient, the input current increases and generates a drop in the input voltage not only because the line is resistive but also because of the coupling between the line inductance and the decoupling input capacitor. The prototype chip-board provides direct supply connector in order to significantly reduce the access impedance. Nevertheless the supply path inductance remains high compared to the short printed circuit traces of a smartphone board.

An USB-to-I^2C converter controls the digital communication bus with a dedicated desktop interface control suite. **This communication bus and the communication sequence are widespread in complex analog components domain but are worth to mention for a good overview of the test-environment.** A program permits to start the chip using a specific procedure. A second program is used to start and stop DC/DC converters. It gives access to the reference voltage and the different operation modes, i.e. forced PWM, auto select mode between CCM and DCM. I^2C registers are set using a third and last program. The prototype uses a common protocol for AB devices with a large number of internal register. Considering a standard stand-alone converter, a master write transaction involves a three bytes transfer: first the slave address, second the register address, and third the data. A standard read is more complex with a four bytes transfer first the slave address is transferred, second the register address is sent. Then

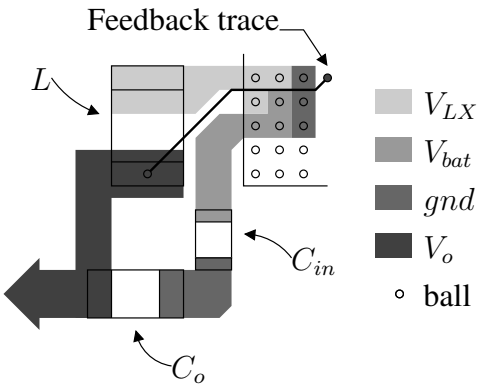


Figure 5.15 – Layout of the chip board

the master writes the slave address again after a repeated start condition and last the slave writes the data.

Starting the device requires a proper sequence of operations. First the test motherboard is supplied with a 5 V power supply and the USB cable that links the motherboard to the desktop computer is plugged. Second the 1.8 V power-rail rises, the I^2C bus is then available. The main power rail must be tied to 0 V and then it rises to the desired battery voltage. Last but not the least, a debug pin must be set from 0 V to the battery voltage in order to enter the debug mode. This latter mode gives full I^2C access to the user.

The chip-board layout principle is presented in Figure 5.15. Each power input and output occupies three package balls and the feedback requires an added ball. Traces are kept short but a small trace length is used to virtually increase the capacitor series inductance. This increases the fed-back output voltage ripple in order to increase the compare speed of the inner-loop comparator. **This design trick is used in the demonstration-board of [24].** The output voltage is directly provided at the comparator output while the feedback voltage is sourced at the inductor output-voltage pad. This guarantees low ripple supply voltage with a virtually increased ripple at the feedback point. Two internal copper planes connect the battery voltage and the ground.

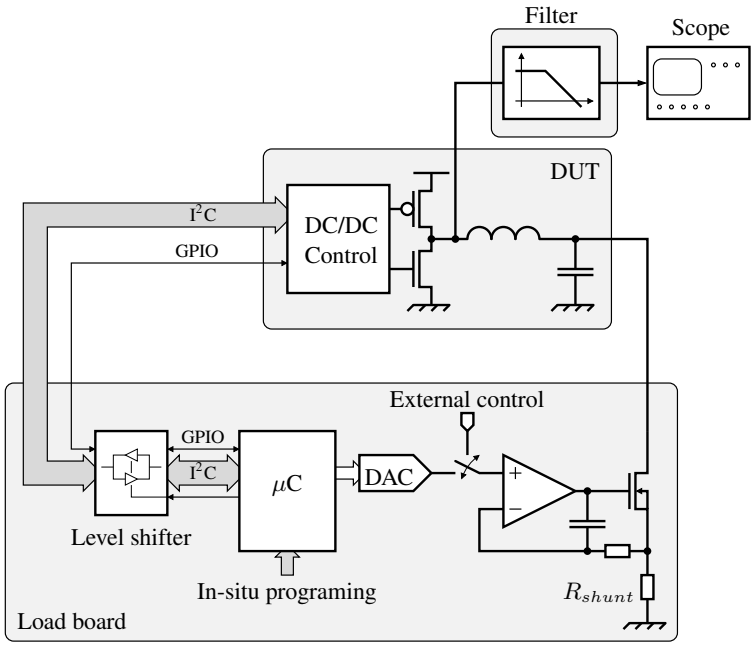


Figure 5.16 – Test bench board setup synoptic

4.3 Load transient

The main purpose of the load transient test-board is to act as a generic embedded processor sourcing current with variations of several MA/s. Furthermore it can handle power dissipation of several watts. Its synoptic diagram with the connection to the Device Under Test (DUT) is presented in Figure 5.16 and a picture of the board is presented in Figure 5.17. The active load can be externally controlled with a voltage generator or internally digitally controlled thanks to an embedded microcontroller. The board digital core controls an I^2C bus and two General Purpose Input/Output (GPIO) that were intended to emulate Dynamic Voltage Scaling (DVS) and the DC/DC converter configuration.

The board architecture is based on a voltage controlled current source. A power N-MOSFET sinks the DC/DC output current and dissipates the power. A shunt resistor, R_{shunt}, is connected between the MOSFET source and the ground. The voltage across the shunt resistor represents the loaded current and is fed back to an integrator that controls the MOSFET gate according to the desired input.

This test board achieves transient speed of several MA/s, up to 8 MA/s has been

Fig. 5.17 – Load transient test board

achieved, and can sink a sinusoidal current up to 1 MHz. A particular care must be put on the length of the wires between the DC/DC converter output and the load board. Long and inductive wires limits the transient speed even if the current sink is a closed loop system. Moreover 15 W static power dissipation has been tested at room temperature without performance degradation.

The software control of the current source permits higher transient speed and reduces the ground noise compared to an external voltage control. Due to the complexity in the configuration of the Analog Baseband under test and I^2C master management the DVS load digital emulation has not been tested on the proposed prototype. Nevertheless promising tests have been performed on stand alone components.

4.4 Low pass filter

FFT measurements are extensively used to quantify the frequency-loop behaviour of the proposed converter. Frequency measurements are performed on power half bridge output time-domain signal sampled at 25 Mega Samples Per Second (MSPS) to comply with economic and practical constraints.

The measured filter gain versus frequency diagram in Figure 5.18 shows that the design effectively filters frequencies higher than 10 MHz and practical measurements are in line with Spice simulations. For frequencies above 20 MHz the measured gain is far from simulation results. This is mainly due to ringing caused by the long wires

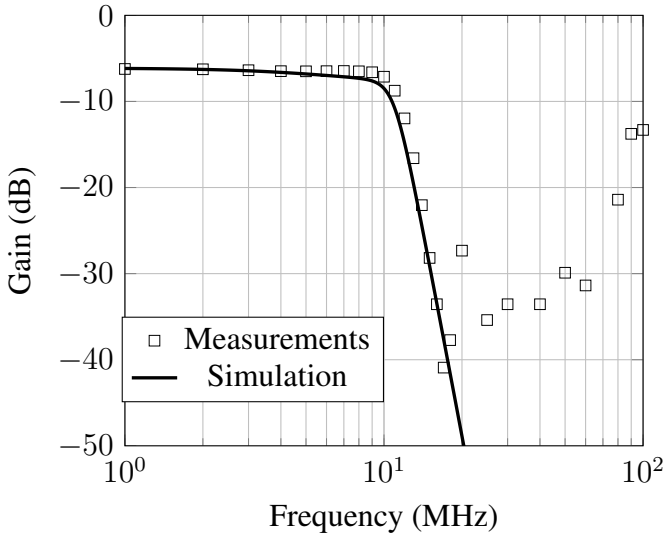
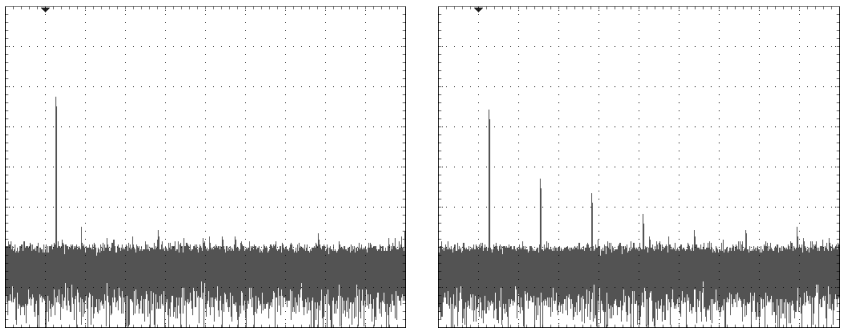


Figure 5.18 – Low pas filter gain vs frequency

used during the filter debug and high frequency output impedance which is probably not modelled by the manufacturer' Spice model.

Figure 5.19a represents the spectrum of a 3.2 MHz, 3.6 V peak-to-peak sinus signal measured at the filter-input and Figure 5.19b represents the spectrum of the output signal. The filter adds a non-negligible distortion to the filtered signal. The root cause of this large distortion is still undetermined. However distortion does not impact the fundamental frequency measurement which is the objective of the filter. Furthermore the input spectrum of an unfiltered 3.2 MHz, 30% duty-cycle, 3.6 V peak-to-peak signal is presented in Figure 5.19c and the output spectrum in Figure 5.19d. The input signal presents visible aliasing phenomena while the filtered signal is clean from visible aliasing. The use of the designed filters enables to measure the fundamental switching frequency of the designed converter and to determine its switching frequency and its frequency stability. Large harmonic content is part of the square-form input voltage and large distortion does not put a new light on everything.



(a) Sinus input spectrum

(b) Sinus output spectrum

(c) Square input spectrum

(d) Square output spectrum

Figure 5.19 – FFT of typical signals

Chapter 6

Results

Experimental results wish to verify the main proposals:

- operation of the converter
- contribution of each loops to performances
- stability analysis of the converter operation
- stroboscopic analysis of the converter operation

1 Introduction

It must first be explained why the proposed DC/DC architecture cannot be tested in open-loop and why it is not worth to try to separately test each regulation loop. The phase loop uses the inner sliding-mode loop as Voltage Controlled Oscillator (VCO) and regulates the whole converter switching frequency. Without line or load perturbation the voltage regulation part of the converter is a simple but noisy[1] VCO that is well suited to characterize the phase-loop. A VCO is required to close the loop and no other VCO with equivalent control-to-frequency behavior as the proposed DC/DC is practically available to enable open-loop tests. Moreover no sensitive signal can be sensed inside the chip because of noise and parasitics that would be added. Thus the voltage outer-loop cannot be characterized separately.

[1] The equivalent VCO presents a large phase noise that is presented thereafter

Nevertheless the voltage compensation function is a simple voltage amplifier mounted in an integrator-configuration for which simulations are assumed to be reliable especially with the selected CMOS process. Last but not the least the inner sliding-mode loop is a well known circuit that does not require further investigations so far.

Thus the test methodology uses two main loop-setups:

- First the phase loop circuit is deactivated. This permits to debug the voltage regulation part and to characterize the current-to-frequency characteristic of the DC/DC converter without impact from the phase-loop stability. The integrator filter is tuned in the range $[0.125\mu s, 2\mu s]$ of time-constant and the current observer time-constant is tuned in the range $[2.5\mu s, 10\mu s]$.

- Second the phase-loop is activated: this permits to validate the whole converter stability, cross-interactions and phase-loop characteristics. The phase-loop filter is tuned with resistance, R_{pll}, and capacitance, C_{pll_i}, in the range $[300k\Omega, 6300k\Omega]$ and $[10pF, 50pF]$ respectively.

Final measurements of the DC/DC converter performances are performed with the two regulation loops. This is the default measurement setup unless otherwise noted.

2 System validation

2.1 DC Voltage regulation

The voltage-loop regulates the output voltage within an acceptable range for stable compensation setup. The typical output voltage versus the load current is presented in Figure 6.1. The converter achieves 2.12mΩ DC output impedance and a no load accuracy close to 0.1% either at 1.2 V output voltage or 0.6 V output voltage. This measurement validates the amplifier functionality and the choice to add an outer-loop compensation integrator. Furthermore it is equivalent to measured commercial solutions. DCM accuracy is not as good as the CCM one. This is because the output voltage ripple is higher

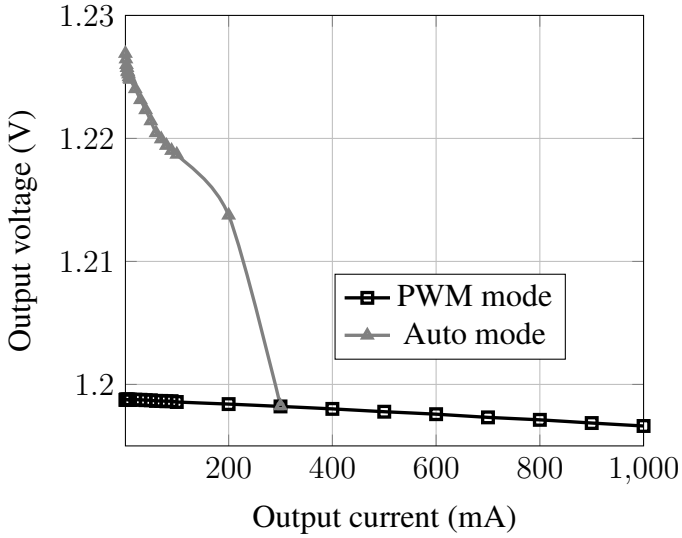


Figure 6.1 – DC output voltage vs load current ($L = 470$nH, $C_o = 10\mu$F, $V_{bat} = 3.6$V, $V_o = 1.2$V)

when the converter operates in DCM than in CCM and the output voltage is practically higher than the reference voltage[2]. Commercial solutions behave similarly.

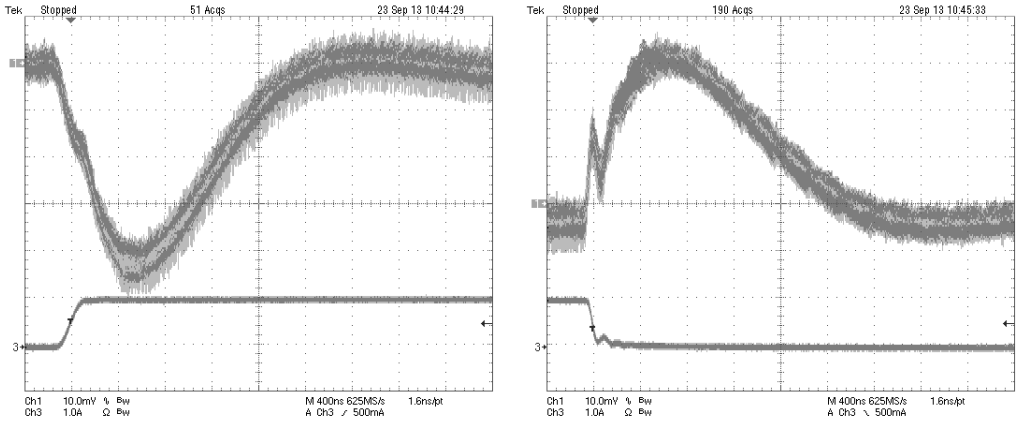
2.2 Response to a large transient

The transient dispersion effect outlined in Figure 2.10 (page 28) for PWM converters is no longer visible thanks to the asynchronous response of the controller. This diminishes the transient margin voltage since no specific margin is required to cope with transient dispersion. Large transient response of the prototype (2-Amp step) with near optimal setting is presented in Figure 6.3.

The current-observer time-constant is designed in order to match the inductor time-constant and the outer-compensation function closes the voltage regulation loop such that the phase margin is near 45 degrees. "Near optimal"[3] undershoot or overshoot are observed during the large transient and especially in Figure 6.3b. When the load transient occurs, the power half-bridge output voltage is set in the desired state until the output voltage slope is zero. Thus the large transient undershoot only depends on the

[2] a conduction pattern that increases the output voltage is generated each time the latter voltage reaches the reference voltage

[3] related to Time Optimal Control



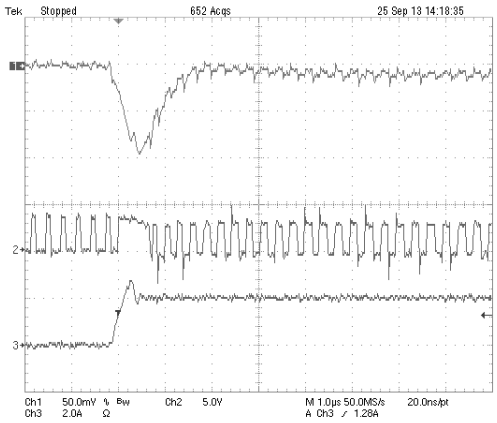
(a) Load rising step transient dispersion (b) Load falling step transient dipersion

Figure 6.2 – Cumulative transient response. In each figure, (top) output voltage (AC coupled, 10mV/div), (bottom) load current (DC coupled, 1A/div)

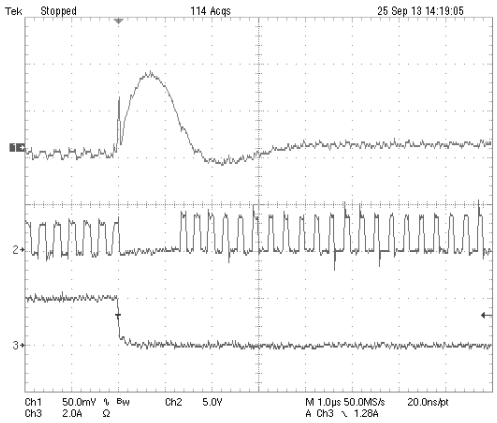
inner-loop that responds rapidly and the power filter that damps the transient effect. Then the recovery time mainly depends on the compensation integrator time-constant. A slow outer loop compensation function makes the recovery time long while a fast integrator results in an undamped response. A slow outer loop setting with a very low power error amplifier has been proposed for the first prototype however this yields a high sensitivity to line perturbations[4]. An ideal TOC response presents both minimal undershoot or overshoot and minimal recovery time. The proposed converter achieves near optimal transient displacement (i.e. undershoot or overshoot) but not a minimal recovery time since it requires a few switching cycles to recover the load transient.

Lowering the coil value increases the converter transient performances thanks to a greater current slope capability. During a large transient the power part keeps its output voltage, V_{LX}, low or high whether the load current is falling or rising respectively. Assuming the change in the output voltage is negligible compared to the voltage across the inductor, the current through the power coil follows the load current with a limited slope. When the load current suddenly rises (i.e. with an infinite slope) the inductor current is lower than the load current until it reaches the load current value. The deficit of carried charges is compensated by the output capacitor and the voltage decreases.

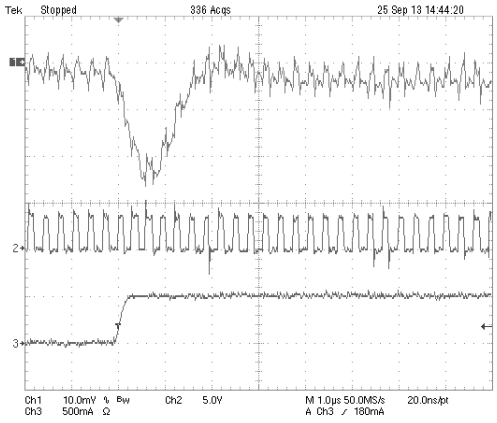
[4] which is assumed to come from the poor amplifier Power Supply Rejection Ratio and the high supply source resistance



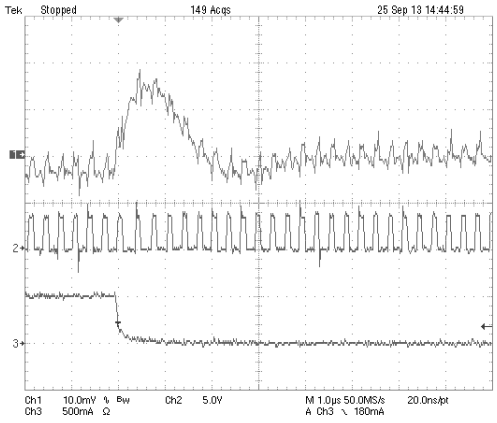
(a) Large load rising step ($R_fC_f = 10\mu s$, $R_iC_i = 0.75\mu s$, $L = 470nH$, $C_o = 10\mu F$)



(b) Large load falling step ($R_fC_f = 10\mu s$, $R_iC_i = 0.75\mu s$, $L = 470nH$, $C_o = 10\mu F$)



(c) Small load rising step ($R_fC_f = 10\mu s$, $R_iC_i = 0.75\mu s$, $L = 470nH$, $C_o = 10\mu F$)



(d) Small load falling step ($R_fC_f = 10\mu s$, $R_iC_i = 0.75\mu s$, $L = 470nH$, $C_o = 10\mu F$)

Figure 6.3 – Load transient with near optimal settings. In each figure (top) output voltage (AC coupled), (middle) power stage output voltage, (bottom) load current

When the load current suddenly decreases, the inductor current is higher than the load current and the charge surplus is absorbed by the capacitor and the output voltage rises. In Figure 6.3b the load current goes to 0 A and the inductor current decreases from 1 A to 0 A with a constant slope. During the load-current fall the inductor-current is higher than the load current thus the output capacitor current is positive and the output voltage rises. The output voltage rise stops when the inductor current equals the output current. In Figure 6.3b the output voltage is 1.2 V and the inductor 470 nH. The falling time required by the inductor current to go from 2 A to 0 A is theoretically $0.78\mu s$. The experiment in Figure 6.3b results in aproximately $0.7\mu s$ between the load transient and the maximum output voltage. The difference is assumed to come from the power half bridge and the inductor resistances.

With a 220 nH inductor the current slope is twice the previous one and the fall time is as much reduced. The transient undershoot and overshoot of the proposed converter with two different inductors are measured with a variable-amplitude square-load. Smaller inductor leads to better transient performances as presented in Figure 6.4. The transient response is linear up to 1 A. The small offset is caused by the ripple and the DC load regulation which is taken into account in this measurement. When the transient amplitude increases, after 1.5 A, the converter response becomes non-linear and the response slope increases.

2.3 Response to a limited transient

On the contrary the small transient response presented in Figures 6.3c and 6.3d remains in unsaturated operation region during transient and the widely covered output impedance can be used to determine the transient response. Therefore the load transient response can be predicted as intermediate between the linear small-signal output impedance response and the time-optimal control response. The limits between the two possible response-type is still unclear. However some hypotheses can be proposed:

- the current slope limitation in the power inductor that forces the converter to operate with a high current distortion. A similar method is used in [8] for a digital Proportional Integral Derivative controller.

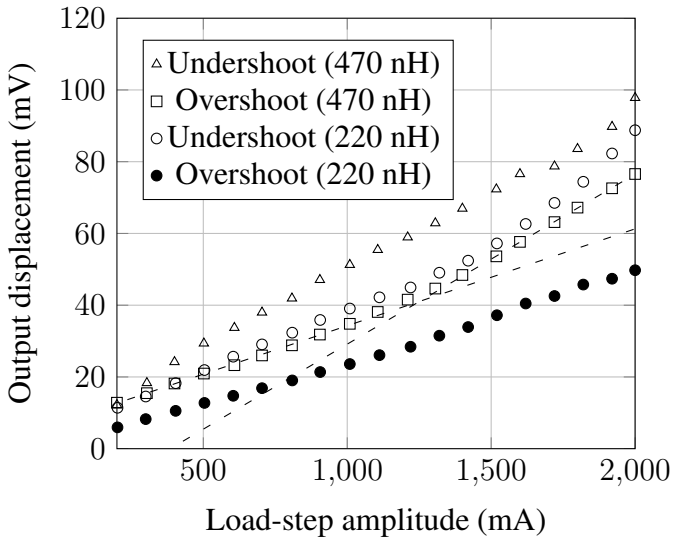


Figure 6.4 – Measurement of the output voltage displacement during transient for the converter with two different power inductors

- the sliding function existence condition is locally positive, i.e. the comparator input error increases instead of being continuously decreasing
- a mix between the two previous proposals and maybe a third unknown element...

The converter transient response meets the initial requirements. The output transient displacement is maintained low even with a small output capacitor and the transient dispersion has been minimized thanks to the asynchronous response of the controller.

2.4 VCO characteristic

Turning Off the frequency-loop and using the digitally controllable bias source of the comparator differential pair, the DC/DC converter current-to-switching frequency is presented in Figure 6.5. More experimental results are gathered in Figures D.6, D.7 and D.8 (Appendix D) and free running oscillation spectra are presented in Figure D.2, D.3, D.4 and D.5. The higher the comparator bias-current the higher the switching frequency nonetheless the equivalent oscillator is far from phase-noise free operation. The measured switching frequency versus the differential pair bias-current is non-linear and the gain is higher at lower bias current than at high bias-current as predicted in Section 2.1 page 52. Using a fitting algorithm the switching frequency versus the bias-current

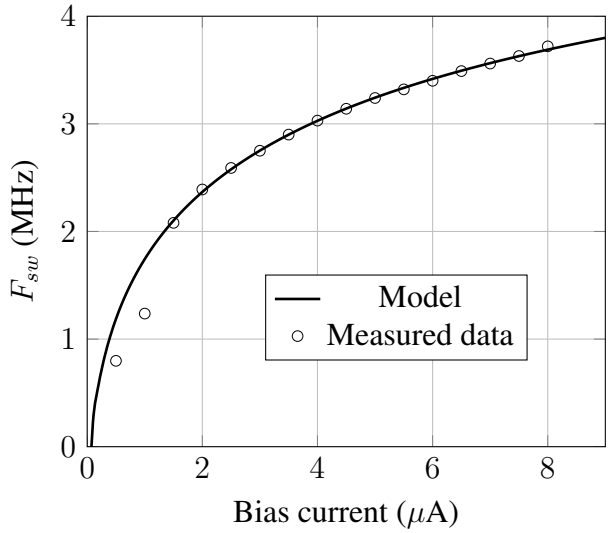
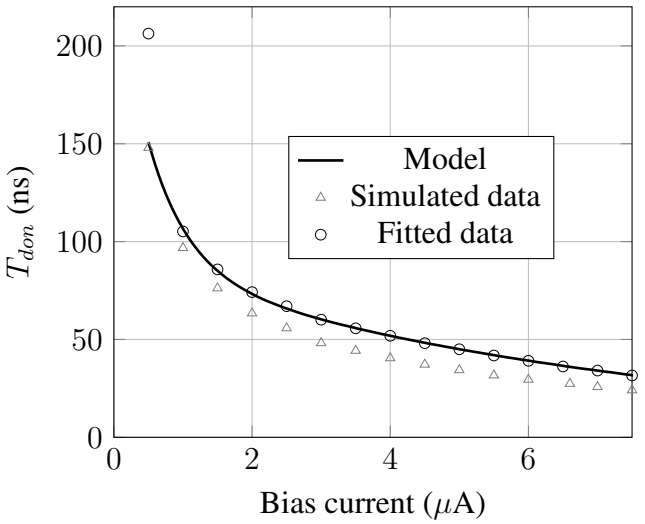


Figure 6.5 – F_{sw} model validation

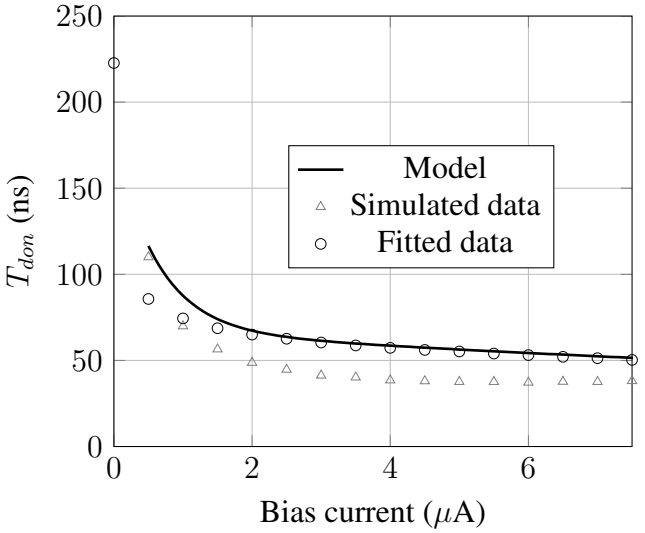
can be approximated by:

$$f_{sw} = \frac{6.881.10^{6}\sqrt{I_b} - 1653}{1.999.10^{-3} + \sqrt{I_b}} \tag{6.1}$$

what is the form of the predicted function (Figure 6.5). As predicted in (3.46) the current-to-frequency gain decreases with an increase in the bias current. Using a non-linear equation solver, the On and Off delays, $T_{d_{on}}$, and, $T_{d_{off}}$ are extracted. The solver algorithm uses simulated data as approximate initial solution in order to best fit the experimental curve. The identified results are presented in Figures 6.6a and 6.6b for the On and Off delay respectively. The fitted model is a sum of exponential functions that locally fits the experimental values better than the invert of the square root function proposed in Section 2.1 (52). This is mainly due to the electrical model approximations that change the root order. Frequencies at very low current-bias are lower than expected. This is probably because a too long delay makes the sliding-mode assumption no longer valid. The $T_{d_{off}}$ limit from (3.12) yields approximately 200 ns what is close to the obtained delay time values.



(a) $T_{d_{up}}$ fitting curves (see Figure 3.2 for definition)



(b) $T_{d_{dn}}$ fitting curves (see Figure 3.2 for definition)

Figure 6.6 – T_{don} and T_{off} delay-times' data (typical conditions)

2.5 Frequency loop

The switching frequency variation main parameters are the battery voltage, V_{bat}, and the output voltage[5], V_o. Switching frequency versus battery voltage is presented with and without the phase locked loop in Figures 6.7a and 6.7b for the first and the second prototypes respectively. The variation in the switching frequency is more visible for the first prototype than the second one. This is mainly due to the converters duty cycles. Experimental measurements validate the theoretical model of the operation of the proposed PLL-based scheme for switching frequency control. The phase loop effectively locks the switching frequency to the desired target frequency. The small drift in the regulated switching frequency value is assumed to come from the reference clock since voltage mode PWM converters that are gathered in the same PMU behave similarly. In low-drop conditions, the voltage-to-current converter output swing is not high enough to provide a sufficient current to obtain the required small delay in the PLL operation so that the switching frequency of the first prototype drops as presented in Figure 6.7a.

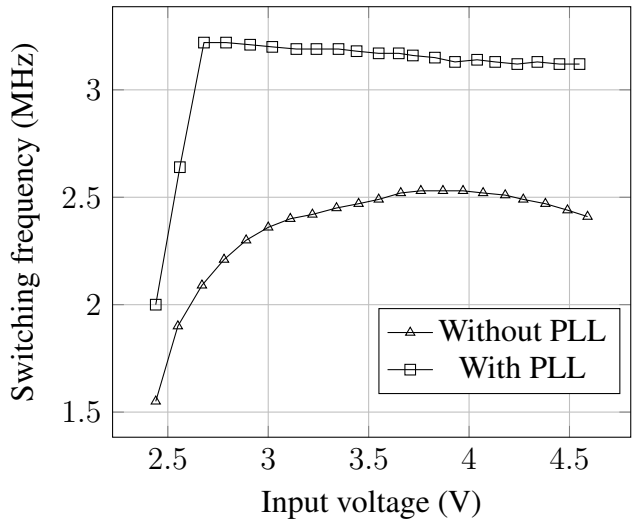
2.6 Closed frequency-loop operation

2.6.1 Load-step transient

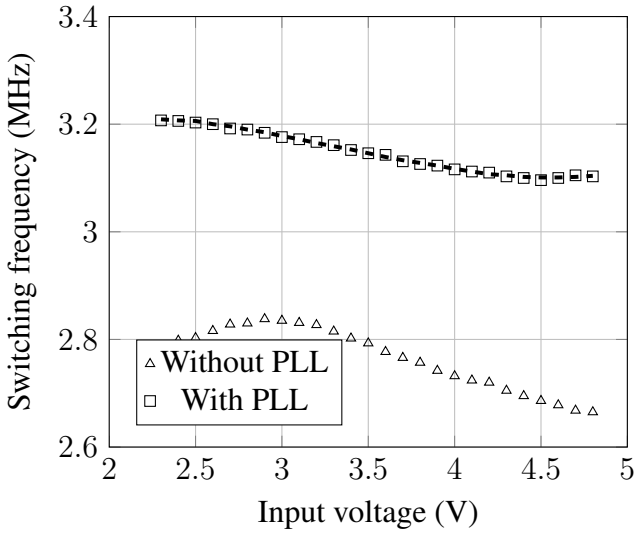
Stroboscopic maps of the converter output voltage and switching frequency under large load-step transients for stable PLL settings as the ones presented in Figures 6.3a and 6.3b are gathered in Figures 6.8 and D.13 D.14 D.15 D.16 D.17 D.18 D.19 D.20 (Appendix D, page 199). The output voltage, V_o, is sampled at each power stage output rising-edge. The instantaneous period of each switching cycle is measured and the corresponding frequency is plotted. When the transient step occurs either output both the voltage and the switching frequency deviate from steady-state values. The load-step is rejected by the fast voltage regulation loop. As expected a small DC offset occurs due to the finite loop gain. The fast disturbance rejection of the voltage-loop generates an impulse disturbance in the frequency-loop.

In Figure 6.8 a spike may be observed on the instantaneous value of the switching frequency. This spike indicates a fast increase in the switching frequency that witnesses

[5] see (3.18)



(a) Primary prototype converter



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(b) Second prototype. Dashed line is expected synchronized values from reference oscillator measurements

Figure 6.7 – Switching frequency (f_{sw}) versus input voltage (V_{bat}) of the two prototypes with and without the phase-loop

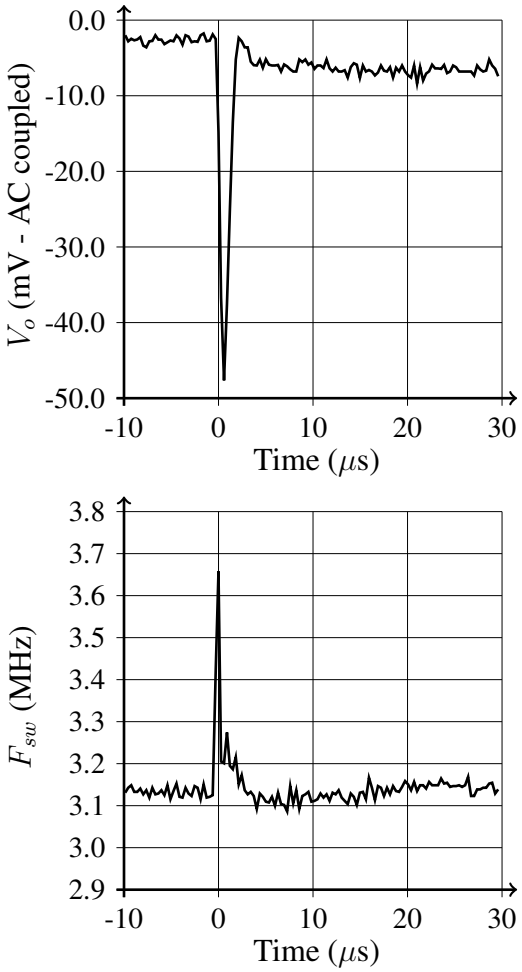


Figure 6.8 – Stroboscopic map for PLL setting: $R_{pll} = 300k\Omega$, $C_{pll_i} = 20pF$

the high velocity of the voltage-loop. Therefore the phase-loop counteracts the disturbance which is asymptotically rejected. The switching frequency value is then rapidly regulated toward the target clock reference value.

Figures D.13 D.14 D.15 D.16 D.17 D.18 D.19 D.20 exhibit different damping factors as expected in Section 3.3. This does not significantly impacts the DC/DC conversion efficiency since the frequency deviation is small.

2.6.2 DCM to CCM transition

Frequency-loop large step response occurs when the converter switches its operation mode from DCM to CCM operation as presented in Figure 6.9. Frequency stroboscopic

map of the converter when it recovers from DCM are presented in Figures D.21a, D.21b, D.21c, D.21d, D.22a, D.22b, D.22c, D.22d.

After exiting DCM, the phase-loop filter is initially pulled to the battery voltage and the converter operates at its maximum switching frequency until the phase filter voltage reaches the battery voltage minus 1.5 V. This drop voltage is required because of the finite input range of both the buffer and voltage-to-current converter. Then the converter switching frequency falls to the desired value with a constant slope that depends on the charge-pump current and the phase-loop filter capacitor value. This is common to any PLL operation in which large transient dynamics is saturated in phase due to the finite operation range of the PFD. The larger the capacitors the longer the reaching time because the filter voltage dynamics under saturated operation is bounded by the charge-pump constant current charge or discharge of the latter capacitors.

The phase-locked-loop settling-time is in the range of five tens of microseconds for the smaller capacitor value which is small compared to the DVSF algorithm typical steps and up to two or three hundred microseconds for the larger capacitance value (50 pF). If the correlation between the instantaneous current consumption of a digital core and its operating frequency is strong then the faster phase-loop settling-time is sufficient to provide globally synchronous operation. This is what suggests the operation picture in Figure 2.3 where the transition between digital operation states generates a large current step followed by a relative bounded current. Nonetheless no correlation data was available during this thesis.

2.6.3 Load-induced switching frequency variations

The harmonic content of the DC/DC converter switching frequency for a repetitive 500 mA square load is presented in Figure 6.10. The harmonic content of the load modulates the converter switching frequency. The presented three cases cover respectively the in-band case in Figure 6.10a where the load frequency is lower than the phase-loop bandwidth, the limit-band case in Figure 6.10b where the load frequency is close to the PLL bandwidth and the out-of-band case in Figure 6.10c in which the load fundamental frequency is higher than the loop bandwidth. For the in-band case the phase locked loop counteracts the frequency variation and no visible change on the overall switching

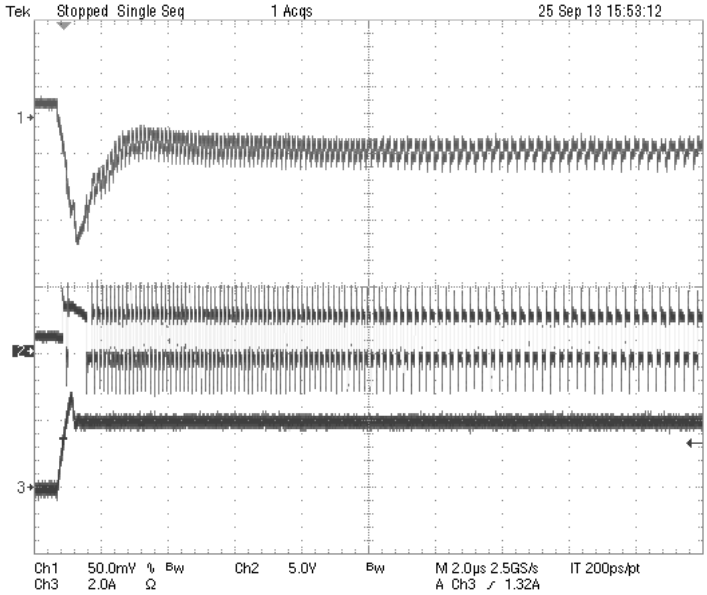
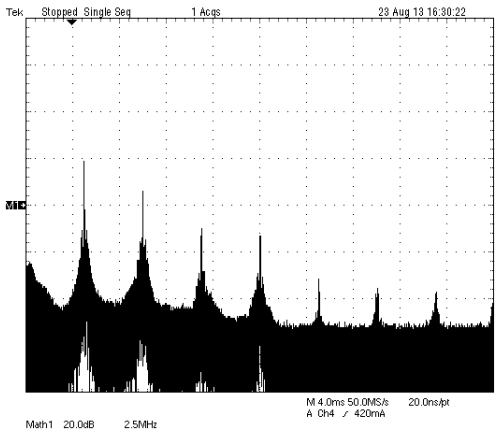


Figure 6.9 – DCM to CCM transition, (top) output voltage (AC coupled), (middle) power stage output, (bottom) load current

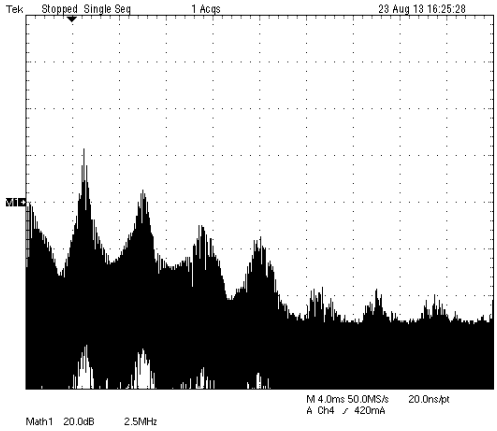
frequency spectrum is observed. For limit-band case the switching frequency is continuously modulated and a visible frequency spread occurs. The frequency variation is small what should not engender a significant drop in efficiency though the phase synchronization is lost since the frequency is continuously modulated. The out-of-band condition results in a load-modulated switching frequency and unwanted spectrum band are visible on the DC/DC switching-frequency spectrum. The average switching frequency remains the controlled one thus the efficiency shouldn't diminish noticeably.

3 Stability analysis validation

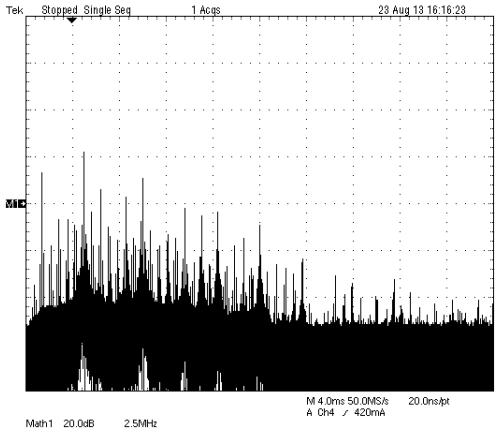
A stability map of the proposed converter with phase filter variation is presented in Figure 6.11a. The light-gray region covers the settings where no eigenvalue is outside the unit circle thereby the converter is supposed to be stable. The black trace represents the unit circle boundary. The dark-gray region settings at the right side of the black curve have at least one eigenvalue outside the unit circle and are supposed to be unstable. Stable experimental measurements are represented by a circle while experimental unstable settings are represented by a cross. The frequency loop stability is observed



(a) load frequency: 2.5 kHz



(b) load frequency: 41 kHz



(c) load frequency: 880 kHz

Figure 6.10 – Switching frequency harmonic content for a repetitive a square 500mA amplitude load

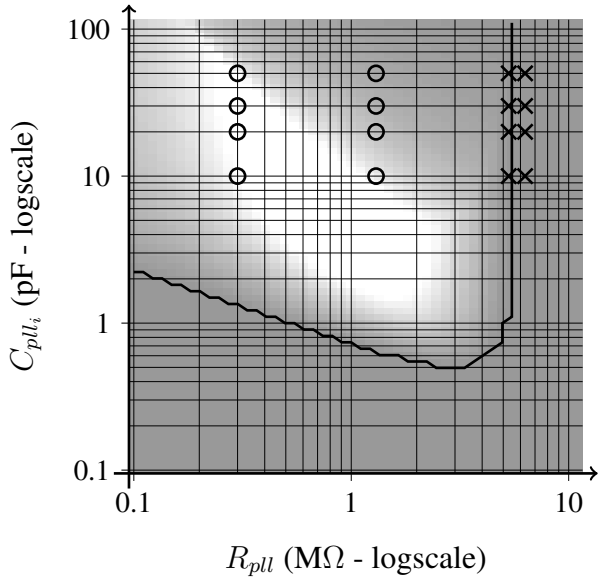
on the switching frequency spectrum presented in appendix D. The frequency loop is assumed stable when no major unwanted spectrum line is observed. The voltage loop is assumed stable if the output voltage does not oscillate[6] and the converter is exempt from period doubling or period tripling.

Unstable measured operations are close to the unit circle boundary presented in Figure 6.11a. Some cases of stable predicted but unstable observed operations occur. Nevertheless these are cases with an eigenvalue close to the unit circle. Accordingly to linear stability analysis some operation margins are required with this method too. Nevertheless the model accuracy, calculation approximation and process variations are possible causes of a small displacement of the stability area.

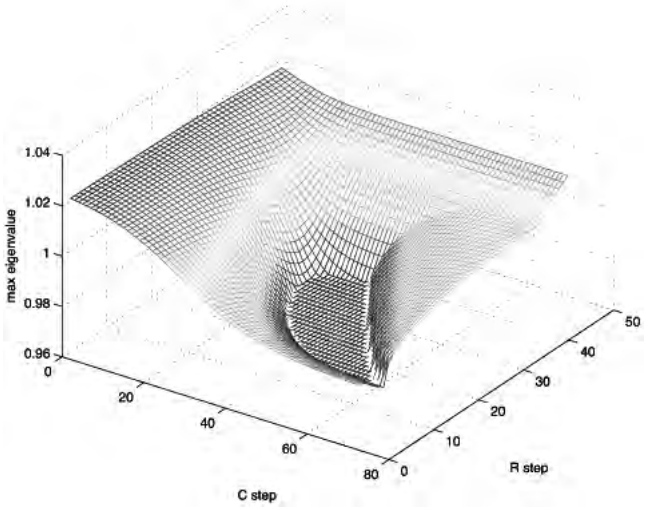
The white area of Figure 6.11a is the stability floor of the PLL filter with the considered settings of the other loops. The minimum eigenvalue module is 0.97 and is fixed by the other loops no change of the phase loop filter settings in this area increases the converter stability margin. **A possible root-cause of such a high value for a stable setting might be the low bandwidth of one of the three loop with respect to the cycle period. A small bandwidth loop takes a large number of cycle to reject the perturbation. This slow rejection speed is coherent with a small rejection ratio.** The designed filter is probably not the best possible setting since it appears that a stable operation point is possible with a smaller phase-loop main capacitor, $C_{pll_i} = 3$ pF, and the proposed 1.3 MΩ resistor.

The stability map for the voltage regulation settings are presented for a 470nH and a 220nH inductor in Figure 6.12 and 6.13 respectively. The overall stability domain is well defined despite rounding approximations in the map design that sharpen the unit circle boundary. For small integration time constant, R_iC_i, the compensation loop bandwidth matrix, A_v, is close to be singular and the eigenvalue calculation suffers from approximations. For a 1 μH inductor, small values of the current observer capacitor, C_f, lead to instability. This is the trend observed in Figures 6.12 and 6.13 where the stability floor for small values of current observer capacitor rises with the increase in the coil value.

[6] except the voltage ripple generated by the switching action



(a) Stability map of the proposed DC/DC converter with a change of R_{pll} and C_{pll_i}, Thick line is the stability domain boundary



(b) Maximum eigenvalues modules for the phase loop filter variation in Figure 6.11a

Figure 6.11 – Eigenvalues analysis of the proposed DC/DC converter with a change of R_{pll} and C_{pll_i}

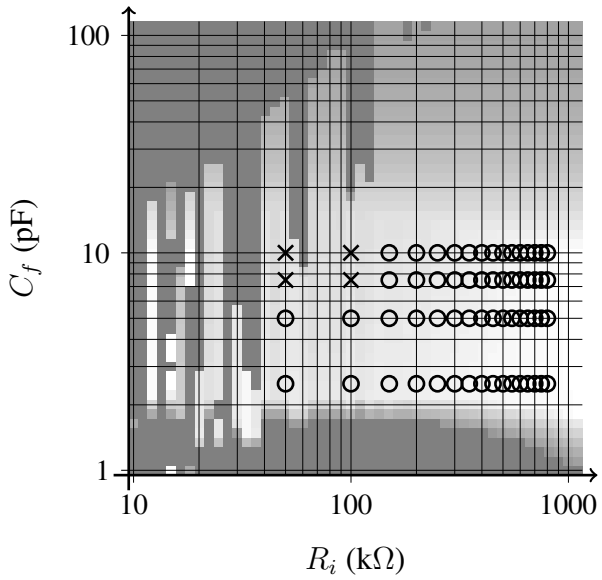


Figure 6.12 – Stability map of the proposed DC/DC versus a change of R_i and C_f, $L = 470$ nH.

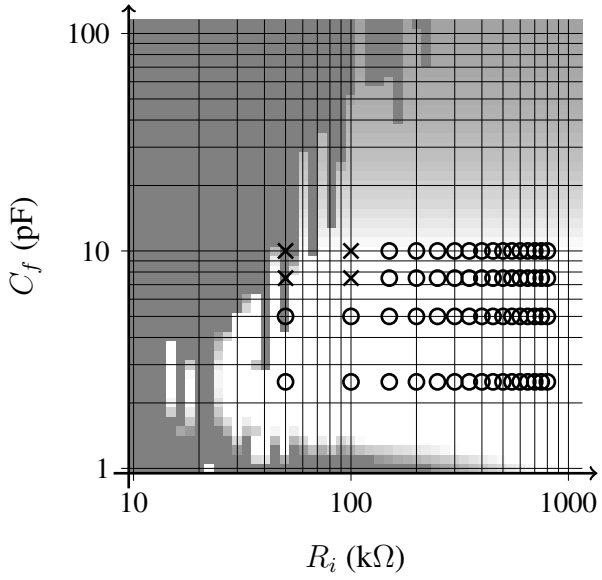


Figure 6.13 – Stability map of the proposed DC/DC versus a change of R_i and C_f, $L = 220$ nH

For time-domain observation, the transient responses of the converter for different settings of the voltage regulation part (R_i, C_i and R_f, C_f time constants) with an increase in the maximum eigenvalue modulus are presented in Fig. 6.14. As expected the converter tends to be unstable with an increase in the maximum modulus of the eigenvalues.

4 Efficiency

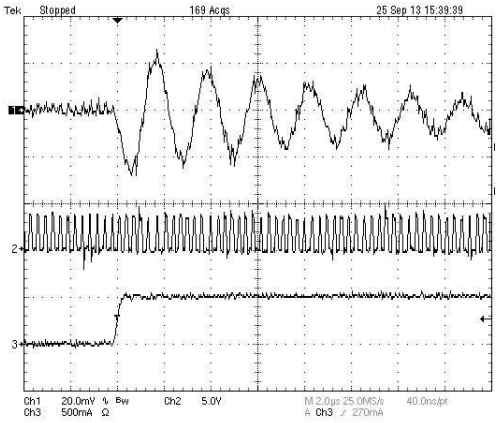
The converter power efficiency versus the load current is plotted in Figures 6.15 and D.23 and D.24. The peak efficiency is reached at 500 mA output current which is the power stage power rating[7]. The efficiency drops for higher output current because of the high power stage resistance. The controller does not implement any dynamic sizing function of the power stage that would enlarge the power transistors in order to reduce their On-resistance at the expense of higher switching losses. This enlargement increases the high current efficiency but the controller becomes more complex with this function.

The efficiency drops dramatically without DCM when current-reversal occurs in the inductor. The proposed DCM handler maintains the efficiency high for low output current. With the proposed implementation the efficiency is maintained higher than 80% between 3 mA and 800 mA output load which is in the line with equivalent commercial devices. Efficiency below 3 mA falls because of the power consumption of the controller that is no-longer negligible. There is no efficiency penalty associated to the phase-loop in sub-mA region since the frequency regulation circuit is disabled and the clocks are gated. The outer-loop error amplifier is maintained in high impedance and low power mode and its bias power consumption is 4-times less than in CCM.

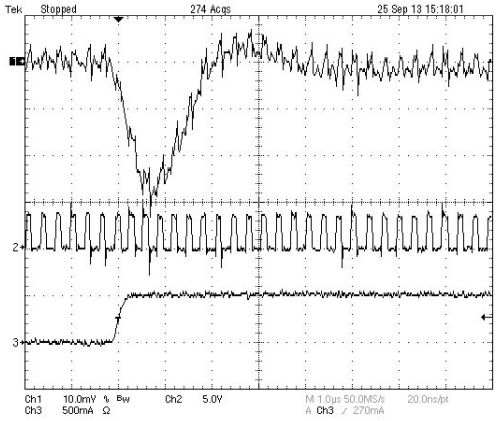
5 Side issues

Simulation versus measurements Circuit simulations have been extensively performed. As mentioned earlier in Chapter 5 there is a discrepancy between simulation

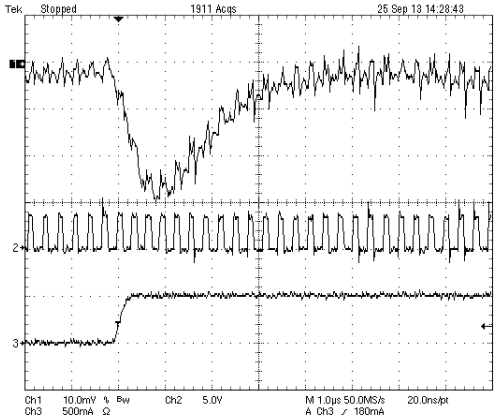
[7]The power stage is used with its 500 mA configuration



(a) $\max|\lambda_i| = 0.9792$



(b) $|\lambda_{max}| = 0.9749$



(c) $|\lambda_{max}| = 0.9711$

Figure 6.14 – Transient response of the prototype for different compensation settings. Top signal: output voltage (AC coupled), middle: power stage output, bottom: load current

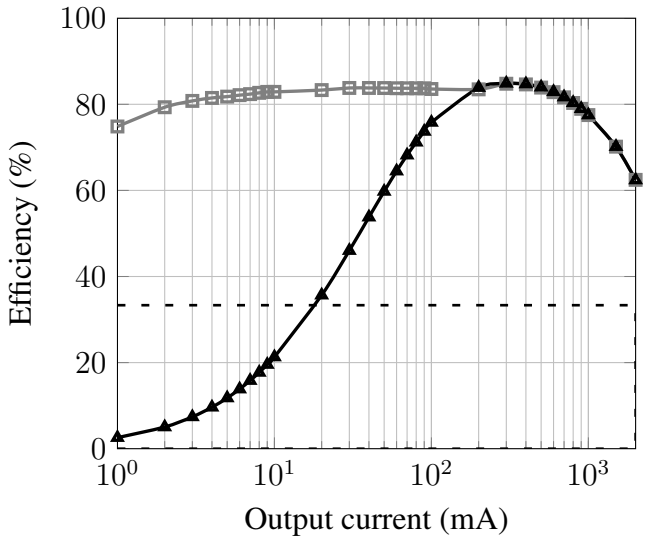


Figure 6.15 – Measured efficiency of the proposed converter in typical conditions ($V_{bat} = 3.6V$, $V_{out} = 1.2V$, $f_{sw} = 3.2MHz$) with (grey curve) and without (black curve) DCM implementation. The dashed line represents the maximum efficiency of a LDO

and experiment regarding time and frequency. Voltages and currents are generally in accordance. In fact simulation lacks many parasitic components and device models are not sufficiently accurate to predict delay-times in the frequency loop behavior. This is quite common in the world of PLL design. The next Chapter mentions that a final and decisive test-chip is required to ”close the loop” between simulation and experiment.

Line-to-output characteristic The line-to-output characteristic of the proposed converter has not been measured due to the measurement bench limitation. Thanks to the indirect current mode architecture the converter should present better line perturbation rejection than a voltage mode PWM converter [34] at the same switching frequency but this has not been quantified so far.

EMI Furthermore the EMI contribution of the converter remains an open issue. Attempts to measure the EMI contribution of the converter reaches limits since only the power supply of the whole chip can be sense. Differentiating the EMI contribution of each block requires accurate measurement tools that were not available particularly no Line Input Stabilization Network (LISN) was available. **Nevertheless the power stage**

of the proposed converter is a standard IP and the rising-edges of the power-stage output are independent from the modulation strategy. Hence one can expect a similar very high frequency spectrum for the frequencies above hundred MHz. The low frequency part of the EMI contribution of the DC/DC converter might be extrapolated from fundamental switching frequency spectrum of the converter measured in D.

Chapter 7

Conclusion

An embedded high performance digital core is a highly varying load that requires a specific power supply strategy in order to comply not only with the electric requirements of the processor but also with the power efficiency requirements of the embedded platform. DC/DC converter transient performances are a huge source of power saving capability. Better transient performances permit more aggressive Dynamic Voltage and Frequency Scaling (DVFS) strategy and a reduced transient margin in case of under voltage. The digital-load transient speed is higher than the transient response speed of a conventional Pulse Width Modulated (PWM) converters. It is noticed in Chapter 2 that the load bandwidth at the DC/DC converter output is at least 1 MHz while switching frequencies of conventional DC/DC are in the range of a few MHz. Therefore the DC/DC bandwidth is lower than the load one. A large output capacitor is used in order to damp the transient response of the converter at the expense of a lower possible DVFS speed. To circumvent the low switching frequency limitation, the chosen solution is to use an asynchronous control scheme. Thereby the average switching frequency is low what maintains a good efficiency while the transient response speed is high.

1 Summary of contributions

The proposed modified V^2 architecture synchronized by the mean of a Phase Locked Loop (PLL) is seemingly a good candidate to overcome PWM control limitations. The inner current-loop provides fast transient response, the outer voltage-loop provides accuracy and the frequency-loop yields the average switching frequency. Despite this simple principle of operation, a full design of such a converter reveals many challenges. Thereby some of them have been addressed:

- The design challenge is to constraint the controller silicon area but offer sufficient phase-control performances. This is the reason why the proposed variable delay control has been developed in Chapter 3 and patented. It adds no specific delay-controlled element and does not require large power consumption. The silicon area penalty is negligible.

- The second challenge is to provide simple models to set the converter and predict its performances throughout the design process. These models have been proposed in Chapter 3. More accurate but less intuitive models are gathered in references.

- The challenge with respect to control issues is to model the converter stability without neglecting the loop cross-interactions. The proposed method in Chapter 4 addresses this issue with some cited limitations.

- Last challenge is to demonstrate the industrial feasibility of such a converter. This required major design efforts to design a pre-commercial prototype and to prove that a sliding-mode based controller with a PLL synchronization system can comply with commercial requirements. The design of a startup procedure and a Discontinuous Conduction Mode (DCM) module address this issue.

Two prototypes have been designed and tested in order to address these challenges. The first one comprises the essence of the proposed converter with the three loops architecture and a startup module. The latter prototype presented in Chapter 5 adds the DCM feature and proves the commercial capability of the proposed concept. From

measurements analyzed in Chapter 6, it can be outlined that the controlled oscillator is silicon-area friendly but phase-noisy. Nevertheless the phase loop circuit achieves the regulation of the switching frequency. Synchronized switching frequency results are surprisingly good compared to the equivalent oscillator performances. Large voltage transient performances are near optimal with the proposed control scheme that permits either of diminishing the output capacitor to reduce the printed board footprint of the solution or of reducing the voltage margins of the core supply voltage.

Simple proposed models from Chapter 3 enable to represent the converter behaviors and the frequency and voltage compensation functions can be set prior a full CMOS design. Then the stability analysis method proposed in Chapter 4 permits to fine tune the functions in order to optimize the speed of the loops. As a main drawback this method requires a precise model of the converter controlled-delay that is difficult to obtain ante prototype. The delay analysis proposed in Chapter 3 faces the process model complexity that makes the calculation of the loop delay difficult with simple expressions.

The power conversion efficiency at low output current is high thanks to the DCM handler. The mechanism of state transition decision takes into account the asynchronous nature of the converter and does not rely on a reference clock. This proves the capability of such a controller to be used in a mobile platform environment without loss in efficiency.

2 Short-term improvements

Despite the absence of practical and industrial specifications, many issues had to be addressed. At design level the free-running oscillation noise can probably be optimized. A close study of the oscillator noise mechanism may engender new design requirements for the sliding-mode comparator. The phase loop design should be optimized as well with a better charge-pump circuit[1] and a full rail-to-rail circuit of the phase-filter buffer and the voltage controller current source. Then the DCM control state-machine should be improved with the addition of a rebias state between the DCM and the Continuous

[1] the used one can be improved with the design of high compliance current mirrors instead of simple current mirrors

Conduction Mode (CCM). Proposed design restarts the error amplifier as soon as the DCM to CCM transition occurs. However the amplifier requires more than a period to be fully operational and an unwanted transient occurs during the change event. An improved state-decision machine that generates an intermediate conduction type between the DCM and CCM has been successfully simulated and should solve the amplifier restart issue. Last but not the least a precise quantification procedure of the current-to-delay characteristic of the converter that does not requires an extracted-parasitic simulation of the comparator may significantly increase the design process speed.

At system level the output response model of the converter can be improved. The output impedance model of the converter is not developed in this thesis since it is widely covered in the literature. But a linear average-based tool appears to be inadequate to model the converter that operates strongly in non-linearity during large and fast load transient as well is the Time Optimal Control (TOC) model which is better theoretically than obtained results. Cross interactions between the phase loop and the voltage loop during transient operation has not been quantified but observed. The Relative Gain Array method is an path worth exploring. The guarantee that the phase loop does not significantly degrades the voltage transient response of the converter remains an open issue too.

System measurements with a real digital core as a load has not been performed so far. It is probable that unexplored feature of the converter may be discovered during such experimentation. The load transient board has been designed with a fast 10-bit, 240 MHz video digital-to-analog converter but its control is performed with a slow general purpose input/output port of an entry-level 8-bit microcontroller. This does not enable us to generate exactly the fast transient current required by a digital load but only stress-case equivalent in amplitude and rising-time. The test-motherboard is the bottleneck of the DC/DC measurement systems. Even with the latest improvements the board system does not provide the necessary features of a real power characterization that is required to measure a DC/DC converter. A complete redesign of this test environment is required to diminish the access resistance for example.

3 Perspectives

The proposed converter can be modeled as a Multi-Input-Multi-Output (MIMO) system with a voltage output and a frequency output. Extending this principle to a dual voltage output converter yields a MIMO system with three outputs. The most convenient way to regulate such a converter should be to control the common mode and the differential mode output voltage while switching frequency is regulated by the mean of a single phase loop. The proposed stability analysis principle may be extended to this more complex converter with the addition of hitting states and an extended state vector.

The proposed converter appears to be well suited for high frequency DC/DC converter. The inner loop operating at high frequency has been demonstrated in [71] and the addition of a lower bandwidth integrator and a phase-locked-loop circuit is a matter of engineering. The main limitation is to design a sliding-mode loop with a sufficiently low propagation delay that can sustain the desired switching frequency. This requires an adapted silicon process and high frequency passive components.

In [69] four inner loops are used in a multiphase configuration. Extending the proposed concept to a multiphase converter results in at least the following challenges:

- The current balance between the phase is complex without effective direct current sensing.
- Multiple solutions for synchronization between the phases and with respect to the reference clock are possible and need to be evaluated[2].
- How to quantify the loop cross-interactions?

As a last perspective we can reasonably propose to extend the principle to a step-up, single or multi-phase converter. Average current mode control and hysteretic current control are well known ways to control a step-up converter and the proposed phase control mechanism should be well suited to increase the control performances.

[2]For instance: is each phase synchronized to his own reference clock a better solution than a daisy chain clock configuration?

4 Do we really need it?

This question is all the more pertinent because of the closure of the industrial partner of this thesis. A two part answer can be proposed.

First the proposed converter regulates the output voltage and the switching frequency as expected. Transient performances are better than the PWM counterparts even with a smaller value output capacitor and the power efficiency of the converter is equivalent to the voltage mode PWM one. The total solution cost and board area have been diminished thanks to the reduction of the external passive components and more challenging digital core can be powered thanks to the proposed control. However the most important test that can't be performed during this thesis is the switching frequency behavior of the converter that supplies a real microprocessor. The frequency modulation induced by the load variation may degrades the phase noise of the switching frequency. Nevertheless is a fixed switching phase really useful to supply a digital core? Commercial SMPS use clock spreading to reduce the generated EMI peak frequency by spreading the EMI energy over a small frequency band. The load-induced frequency modulation of the converter switching frequency spreads the switching frequency spectrum as well as an intentional spreading. Thus despite this last validation process and few minor-bug corrections this IP-block is promising.

Second the main drawback of this control scheme is its complexity. First the development process requires a real silicon measurement of the oscillator characteristics unless the designer is lucky and anticipates the right trends between simulation and practical measurements. Second it is difficult to justify the need for three regulation loops when only one has been successfully used for decades. Third designing such a converter requires skills in DC/DC control as well as in frequency synthesis, CMOS design and power converters. Finally this means that developing the control principle is a long-term project (**possibly few silicon prototypes**) that involves **various skills that might be difficult to gather** in order to develop a complex solution. This is the opposite of what is expected by silicon manufacturers, a quick time-to-market development of a simple solution.

DC/DC control for digital supply it is a field of investigation that is probably infinite

and the main purpose of this thesis is not only to try to address a few issues but also mainly to convince the reader that an other way of thinking is possible. At the end of the thesis a lot of technical issues appeared and paves the path to new developments.

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Chapitre 8

Résumé étendu français

1 Introduction

Les téléphones et tablettes de dernière génération offrent des performances multimédia équivalentes aux ordinateurs de bureau et portables. La puissance de calcul nécessaire aux applications multimédias des appareils mobiles ne peut être délivrée qu'avec des composants dédiés regroupant des milliards de transistors sur une seule puce de silicium. Ces composants digitaux sont appelés « System-On-Chip » (SOC)[1], « Digital Baseband » ou « Application Processor » par les fabricants d'appareils mobiles.

L'alimentation électrique des SOC est réalisée par des composants intégrés dédiés qui mettent en œuvre de nombreux composants passifs assemblés sur la même carte électronique que le circuit digital. La Figure 1.1 (page 2) présente une carte électronique de téléphone de dernière génération (2013) où les composants passifs de puissance sont identifiés par des rectangles blancs. La surface occupée par les composants passifs des circuits d'alimentation du téléphone représente une partie non négligeable de la surface totale de la carte électronique. Il y a un intérêt économique à limiter cette surface mais ceci rencontre des verrous technologiques.

Lors de la conception d'un convertisseur de tension de nombreux compromis sont réalisés entre les différentes caractéristiques du convertisseur. Un essai de représentation de certain d'entre eux est proposé en Figure 1.2 (page 4). Cette thèse porte sur l'amélioration

[1] En français : Système Sur Puce

du compromis entre la taille des composants passifs de puissance du convertisseur DC/DC et ses performances transitoires sans dégradation du rendement global. Pour ce faire la solution proposée utilise un convertisseur en mode glissant dont la fréquence et la phase de découpage est régulée par une boucle de verrouillage de phase. Lorsque la charge varie brusquement le convertisseur compense rapidement la variation de charge grâce au fonctionnement asynchrone du modulateur en mode glissant et lorsqu'un régime établi est atteint, la boucle de verrouillage de phase fixe la fréquence de découpage du convertisseur tout en maintenant le rendement élevé à l'égal de celui d'un régulateur à fréquence fixe par modulation de largeur d'impulsion (PWM).

Lors de cette thèse, deux prototypes ont été réalisés en technologie CMOS 130 nm ainsi que les divers outils de test nécessaires à l'analyse du fonctionnement spécifique de ce mode contrôle. Deux brevets issus des travaux détaillés dans ce document ont été déposés et plusieurs articles internationaux. Cette thèse s'est déroulée dans un contexte difficile avec notamment la disparition du principal donneur d'ordre ST-Ericsson, qui résulte d'un manque de précision sur l'objectif visé. Ainsi ce manuscrit doit être lu en gardant en mémoire que l'objectif est l'amélioration du compromis entre la réponse transitoire et la taille des éléments passifs du convertisseur.

2 L'alimentation des cœurs numériques

2.1 Spécificités des cœurs numériques vues du régulateur de tension

Les spécificités de l'alimentation des cœurs numériques sont analysées plus en détail au Chapitre 2. Cette Section en reprend les principaux éléments. L'analyse proposée s'établit sur trois niveaux d'étude où une action à chaque niveau à des interactions sur les autres :

1. Le premier niveau est le composant lui même et les différentes optimisations qui peuvent être faites pour réduire la consommation du circuit digital.

2. Le second niveau est le circuit digital lui même qui assemble les composants élémentaires (transistors) pour en faire un processeur.

3. Le dernier niveau est le logiciel qui exploite le matériel réalisé au niveau précédent avec des composants du premier niveau.

2.1.1 Premier niveau : composant

Au niveau « composant », de nombreux efforts sont déployés par les fabricants de semi conducteurs pour diminuer les courants de fuite des transistors. Ces courants de fuite représentent une part non négligeable de la consommation électrique des circuits digitaux et augmentent avec la tension d'alimentation et la réduction des tailles des transistors. Pour réduire l'effet de ces courants de fuite, diverses techniques sont proposées comme l'utilisation de transistor sur substrat SOI[2] ou la polarisation du substrat.

Lorsque le transistor change d'état, diverses capacités parasites sont chargées ou déchargées. Ces pertes liées à la commutation des transistors s'additionnent aux pertes par les courants de fuites. Lorsque le transistor ne commute pas, ces pertes sont par essence inexistantes. La diminution des capacités parasites du composant peut se faire en diminuant la taille du transistor et par l'utilisation de transistor sur substrat SOI ou d'autres géométries optimisées.

2.1.2 Second niveau : circuit logique

La diminution des courants de fuite est réalisée en diminuant la tension d'alimentation au minimum et en coupant l'alimentation électrique des blocs inutilisés du circuit.

Au niveau « circuit », les principaux efforts pour réduire la consommation d'un circuit digital portent sur la réduction des commutations des transistors. Un processeur effectue d'autant plus d'opération par seconde que ses transistors commutent vite et il y a une forte corrélation entre les performances de calcul d'un processeur, son horloge de calcul et sa consommation représentée par l'équation 2.1 (page 10). Lorsqu'une partie du circuit n'effectue aucun calcul pour une courte période ; son horloge est désactivée ; les transistors ne commutent plus : les pertes par commutation sont pratiquement éliminées. Là encore une tension d'alimentation minimum permet de diminuer les pertes par commutation car les capacités parasites sont chargées à moindre tension.

[2]SOI : Silicon On Insulator, ou silicium sur substrat

2.1.3 Troisième niveau : logiciel

Le logiciel qui exploite le processeur de l'appareil mobile a une grande influence sur les performances énergétiques des processeurs embarqués. En ajustant continuellement la tension d'alimentation et la fréquence de calcul du processeur, les performances de calcul de ce dernier sont ajustées au minimum pour couvrir les besoins applicatifs. Ainsi le processeur fonctionne à la fréquence d'horloge et la tension d'alimentation les plus basses possibles qui permettent d'effectuer les opérations requises dans le temps imparti. Les pertes par commutations et par courants de fuite sont ainsi minimisées.

La combinaison de toutes les techniques mentionnées dans ce chapitre permettent de maintenir la puissance dissipée par le processeur la plus faible possible par rapport aux besoins applicatifs (qualité de service). Ces techniques modulent dynamiquement le fonctionnement du processeur et rendent sa consommation électrique grandement variable. Le pire cas considéré est un réveil sur interruption du processeur. Le processeur fonctionne initialement à tension d'alimentation la plus faible possible et nécessite un courant de fonctionnement très faible. Lorsque l'interruption survient, le cœur numérique requiert la tension de fonctionnement maximale et le courant d'alimentation maximum pour délivrer toute les performances de calcul du circuit.

2.2 Du régulateur de tension au cœur digital

La sortie du régulateur de tension est directement connectée aux circuits logiques via des pistes et plans sur le circuit imprimé, les divers éléments du boîtiers (pattes du composants, fils de connexion à la puce) et les niveaux de métaux de la puce. Ces éléments forment un circuit passif dont un modèle est présenté en Figure 2.1 (page 14). D'un point de vue fréquentiel, ces éléments parasites filtrent les variations de charge dont la fréquence équivalente est supérieure au MHz. Ainsi les variations de consommation électrique du processeur dues aux différentes instructions sont filtrées par des capacités de découplage tandis que la régulation basse fréquence de la charge est assurée par le DC/DC. Lors d'un réveil sur interruption, la dynamique du courant de charge est aussi limitée par le filtre passif équivalent formé par les éléments parasites du circuit à plusieurs MA/s. Maintenir de bonne performances transitoires permet de minimiser

la chute de la tension de sortie lors d'un fort transitoire de charge, ainsi la marge de tension d'alimentation présentée en Figure 2.4 (page 16) qui définit l'écart entre la tension minimale d'alimentation du cœur digital et la tension effectivement délivrée, peut être réduite à capacité de découplage constante ou alors la capacité de découplage du régulateur peut être réduite à marge de réponse transitoire identique.

2.3 Choix du convertisseur de tension et de son mode de contrôle

Un bref aperçu des diverses topologies de conversion de tension non-isolées permettant d'abaisser la tension de batterie qui évolue de 2.5 V à 4.5 V à la tension d'alimentation du processeur qui évolue de 0.6 V à 1.2V est proposé en Section 3.2 (page 17) et représenté en Figure 2.5 (page 18). Le convertisseur retenu est un régulateur abaisseur de tension de type « buck » monophasé qui permet d'obtenir un rendement maximum tout en maintenant la surface totale de la solution, faible.

2.3.1 Contrôle par modulation de largeur d'impulsion

Le contrôle d'un convertisseur de tension de type buck est généralement effectué en modulant en largeur d'impulsion, une fonction de compensation de type Proportionnel-Intégral-Dérivé (PID) comme présenté à la Figure 2.6 (page 22). Un autre mode de contrôle consiste à réguler le courant dans l'inductance de puissance du convertisseur et imbriquer cette boucle de courant dans une boucle de tension qui régule la tension de sortie à la tension désirée. Ce contrôle appelé « current-mode-control » en anglais[3] permet d'obtenir de meilleures performances transitoires que la régulation par modulation directe d'une fonction PID mais au prix d'une complexité accrue. Néanmoins ces deux modes de contrôle ne permettent pas des réponses transitoires asynchrones vis-à-vis de l'horloge de référence et sont limités à des vitesses de réaction bien en dessous de la fréquence de découpage.

[3] une traduction française pourrait être : contrôle en mode courant

2.3.2 Contrôle en mode glissant

La structure intrinsèquement discontinue d'un convertisseur à découpage s'adapte bien au contrôle en mode glissant dont la loi de commande est directement discontinue. La Figure 2.12 (page 31) représente un régulateur en mode glissant dont la loi de commande dépend directement de la tension de sortie. Lorsque la tension de sortie est inférieure à la tension de sortie désirée, l'étage de puissance est positionné à l'état haut pour augmenter le courant dans l'inductance. Lorsque la tension de sortie est inférieure à la tension de sortie désirée, l'étage de puissance est positionné à l'état bas pour diminuer le courant dans l'inductance. Ce mode de contrôle très simple offre des performances transitoires optimales puisque la contre-réaction à une variation de la tension de sortie est quasi instantanée, limitée seulement par délais de comparaison et de commutation de l'étage de puissance. Cependant ce convertisseur est instable si le condensateur de sortie ne présente pas une résistance équivalente série suffisante.

La structure présentée en Figure 2.13 (page 32) permet de résoudre le soucis d'instabilité du convertisseur précédent. Un circuit RC est connecté en parallèle avec l'inductance de puissance et la tension aux bornes du condensateur C_f offre une représentation du courant dans l'inductance. Ainsi la loi de commande en mode glissant est une fonction linéaire de la tension de sortie et d'une image du courant dans l'inductance. Cette structure offre de bonnes performances en transitoire puisque toute variation importante et rapide de la tension de sortie est directement ramenée à l'entrée négative du comparateur via la capacité C_f. Cependant la résistance de sortie du convertisseur est équivalente à la résistance DC de l'inductance et la précision statique de ce montage est insuffisante pour l'application visée.

Pour améliorer la précision statique du convertisseur présenté en Figure 2.13 (page 32), une boucle de compensation de la tension de sortie peut être utilisée comme présentée en Figure 2.14. Le convertisseur en mode glissant offre des performances transitoires élevées tandis que la fonction d'intégration de l'erreur de tension compense la résistance de sortie DC du convertisseur. La mesure du courant d'inductance s'effectue soit par mesure directe, soit en prélevant l'ondulation de sortie, soit en reconstituant l'ondulation de courant dans la capacité de sortie.

2.3.3 Fréquence de découpage d'un régulateur contrôlé en mode glissant

La fréquence de découpage d'un régulateur en mode glissant est structurellement incontrôlée. Elle dépend essentiellement de la tension d'entrée, de la tension de sortie, du délai de comparaison et de commutations des éléments actifs et d'un éventuel cycle d'hystérésis à l'entrée du comparateur. Ces éléments peuvent être fortement variables pour une alimentation dédiée aux cœurs numériques et peuvent mener à des fréquences de découpage éloignées de la fréquence de découpage désirée. C'est pourquoi de nombreux travaux portent sur le contrôle de la fréquence de découpage d'un convertisseur contrôlé en mode glissant.

La Section 6.1 (page 34) présente des solutions dans lesquelles chaque cycle est synchronisé sur l'horloge de référence. Cette solution n'apporte pas de réels avantages par rapport à un convertisseur contrôlé via une boucle de courant imbriquée dans une boucle de tension. La régulation de la fréquence de découpage du convertisseur par une boucle de régulation de fréquence ou de phase permet de conserver le comportement structurellement asynchrone du convertisseur contrôlé en mode glissant tout en fixant la fréquence de fonctionnement de ce même convertisseur en régime établi. Ce principe de fonctionnement est présenté en Figure 2.15 (page 39), le convertisseur DC/DC est utilisé en tant qu'oscillateur dans une boucle de fréquence ou de phase.

L'oscillateur équivalent est contrôlé en modulant soit un cycle d'hystérésis à l'entrée du comparateur soit le temps de délai de la boucle en mode glissant. Ce dernier mode de contrôle présente l'intérêt de ne pas significativement dégrader les performances transitoires du convertisseur contrairement à une modulation d'un cycle d'hystérésis en entrée du comparateur de la boucle interne.

La section suivante propose une solution permettant d'obtenir :

1. Des performances transitoires équivalentes ou meilleures qu'un convertisseur contrôlé par modulation de largeur d'impulsion d'une fonction PID, avec la capacité de sortie la plus petite possible.

2. la capacité d'utiliser des inductances les plus faibles possibles (moins de 1 μH pour des fréquences de découpage de 3 à 6 MHz).

3. Un contrôleur tout intégré sur puce.

4. Une fréquence de découpage contrôlée dans l'intervalle de 3 à 6 MHz.

5. Un contrôle analogique et une faible consommation du contrôleur pour obtenir un rendement élevé sur une large plage de courant de sortie.

3 Analyse et conception d'un régulateur de tension dédié à l'alimentation des cœurs numériques

Le convertisseur de tension étudié est représenté en Figure 3.1 (page 47). Un réseau passif constitué d'une résistance R_f et d'un condensateur C_f connectés en parallèle de l'inductance de puissance, émule la composante alternative du courant d'inductance I_L. Le comparateur en mode glissant maintient la tension moyenne d'erreur $\overline{\epsilon}$ nulle, telle que :

$$\overline{V}_{comp} = \overline{V}_{C_f} + \overline{V}_o = \overline{V}_{LX} = R_l\overline{I}_o + \overline{V}_o \tag{8.1}$$

L'impédance statique de sortie de la boucle interne du convertisseur est équivalente à la résistance série de l'inductance. Pour la diminuer et rendre la tension de sortie indépendante du courant moyen délivré à la charge, une boucle externe à grand gain statique est appliquée via l'amplificateur et le réseau R_iC_i qui forment une fonction d'intégration. Ainsi la résistance statique de sortie du convertisseur est divisée par le gain de la fonction externe. Elle est donc négligeable.

La boucle interne formée par l'étage de puissance, le filtre de puissance [L, C_o], la charge, le réseau R_fC_f et le comparateur fonctionnent en mode glissant si les conditions d'existence définie par les équations (3.11) et (3.12) sont valides (respectivement aux pages 49 et 50) . En pratique ces conditions sont valides pour les points de fonctionnement normaux du convertisseur. Ainsi lorsque la tension d'erreur $\epsilon\,(t)$ à l'entrée du comparateur de la boucle interne est positive, la sortie de l'étage de puissance est positionnée à la tension de batterie, V_{bat}, et le courant dans l'inductance augmente ainsi que la tension aux bornes du condensateur C_f, jusqu'à ce que la tension d'erreur en

entrée du comparateur soit nulle. Lorsque la tension d'erreur $\epsilon(t)$ est nulle, le comparateur commute et commande l'étage de puissance pour que sa tension de sortie, V_{LX} soit tirée à 0 V. Cette commutation se produit avec un temps de délai qui dépend du temps de comparaison du comparateur et de la vitesse de commutation de l'étage de puissance. Ainsi lors de la commutation, la tension d'erreur $\epsilon(t)$ est positive. Le courant dans l'inductance décroit, ainsi que la tension aux bornes du condensateur C_f, jusqu'à ce que la tension d'erreur $\epsilon(t)$ soit nulle. Là encore la commutation de l'étage de puissance aura lieu avec un délai et la tension d'erreur sera devenue négative comme présentée en Figure 3.2 (page 48).

Les conditions d'existence du mode glissant sont détaillées en Section 1.2 (page 47). Une fois le fonctionnement en mode glissant de la boucle interne établi son modèle équivalent en basse fréquence peut être calculé en considérant la tension d'erreur moyenne ϵ nulle ainsi que sa première dérivée[4]. Le modèle dits en petits signaux équivalent est proposé en équation 3.16 (page 51). Ce modèle a été validé en effectuant des analyses FFT[5] à partir de simulations au niveau transistor de la boucle interne du prototype, dont les résultats sont présentés en Figure 3.3 (page 51).

La fréquence de découpage du convertisseur sans système de synchronisation est incontrôlée et définie au premier ordre par l'équation (3.18). Une des principales idées de cette thèse est de contrôler les délais de comparaison de la boucle, T_{don} et T_{doff} en utilisant un courant de polarisation variable de la paire différentielle de l'étage d'entrée du comparateur de la boucle interne, dont un schéma de principe est présenté en Figure 3.5 (page 54). Les transistors de la paire différentielle sont dimensionnés pour fonctionner sous le seuil où leur gain est proportionnel au courant de polarisation. Ainsi, plus le courant de polarisation de la paire différentielle du comparateur de la boucle interne est important, plus le comparateur est rapide, et plus les temps de délais entre les instants où l'erreur $\epsilon(t)$ est nulle et les commutations de l'étage de puissance sont faibles. Plus les temps de délais sont faibles, plus la fréquence de découpage du convertisseur est élevée, et vice-versa. Un modèle au premier ordre de la fréquence de découpage du convertisseur est proposé par l'équation (3.45). Cette fonction est non linéaire et le gain

[4]D'un point de vue qualitatif, cela signifie que la surface de glissement est atteinte et que la trajectoire du convertisseur est maintenue sur cette surface.

[5]FFT : « Fast Fourier Transform » en français : Transformée de Fourier Rapide

de l'oscillateur équivalent calculé au premier ordre en (3.46) est fortement variable.

Le convertisseur de tension dont la fréquence de découpage est contrôlée par le courant de polarisation de la paire différentielle du comparateur de la boucle interne, est intégré en tant qu'oscillateur dans une boucle à verrouillage de phase. Le schéma de principe du convertisseur proposé avec les trois boucles de régulation est présenté en Figure 3.8 (page 60). Les éléments de la boucle de phase sont communs dans le monde de la synthèse de fréquence. L'analyse utilisée au Chapitre 3 utilise un modèle moyen des différents éléments et une linéarisation de l'oscillateur pour définir le réseau de compensation de la boucle de phase constitué par R_{pll}, C_{pll_i} et C_{pll_p}.

4 Analyse de la stabilité du convertisseur proposé

Un des objectifs de cette thèse est d'évaluer un outil d'analyse de stabilité du convertisseur qui prenne en compte les interactions entre les différentes boucles de régulation et puisse déterminer la présence de phénomènes sous-harmoniques, bifurcations et chaos. La méthode choisie est une analyse de type « sample-data analysis » où la relation de récurrence liant le vecteur d'état au début d'un cycle de conduction n et le vecteur d'état au début du cycle de conduction n+1 est déterminée puis perturbée et enfin linéarisée. Cette méthode est décrite en détail au Chapitre 4, seuls les points essentiels sont repris ici.

4.1 Analyse « échantillonnée, linéarisée tangent »

En régime établi le fonctionnement du convertisseur peut être décrit au cycle n par un système d'équation non-linéaires $f_{x_v} : \Re^{l+2} \rightarrow \Re^{l_v}$ et $f_{x_f} : \Re^{l+2} \rightarrow \Re^{l_f}$ avec $l = l_v + l_f$:

$$\begin{cases} X_v[n+1] = f_{x_v}(X_v[n], X_f[n], \Sigma[n]) \\ X_f[n+1] = f_{x_f}(X_v[n], X_f[n], \Sigma[n]) \end{cases} \tag{8.2}$$

où X_v regroupe les variables d'état de la boucle de tension et X_f les variables d'état de la boucle de fréquence. $X[n]$ est le vecteur d'état au début du cycle considéré, et $X[n+1]$ le vecteur d'état à la fin du cycle considéré. $\Sigma[n]$ modélise l'action de la loi

de commande en mode glissant lorsque la fonction de glissement est atteinte ($\epsilon(t) = 0$). Si le vecteur d'état du convertisseur est soumis à une faible perturbation, $\hat{x}[n]$, au début du cycle alors le système de récurrence (8.2) devient :

$$\begin{cases} X_v[n+1] + \hat{x}_v[n+1] = f_x(X_v[n] + \hat{x}_v[n], X_f[n] + \hat{x}_f[n], \Sigma[n] + \hat{\sigma}[n]) \\ X_f[n+1] + \hat{x}_f[n+1] = f_v(X_v[n] + \hat{x}_v[n], X_f[n] + \hat{x}_f[n], \Sigma[n] + \hat{\sigma}[n]) \end{cases} \tag{8.3}$$

En linéarisant le système d'équation (8.3) et en supprimant les termes de régime établi on obtient :

$$\begin{cases} \hat{x}_v[n+1] \approx \frac{\delta f_{x_v}}{\delta X_v[n]}\hat{x}_v[n] + \frac{\delta f_{x_v}}{\delta X_f[n]}\hat{x}_f[n] \\ \qquad\qquad -\frac{\delta f_{x_v}}{\delta \Sigma[n]}\left[\frac{\delta g}{\delta \Sigma[n]}\right]^{-1}\left[\frac{\delta g}{\delta X_v[n]}\hat{x}_v[n] + \frac{\delta g}{\delta X_f[n]}\hat{x}_f[n]\right] \\ \hat{x}_f[N+1] \approx \frac{\delta f_{x_f}}{\delta X_v[n]}\hat{x}_v[n] + \frac{\delta f_{x_f}}{\delta X_f[n]}\hat{x}_f[n] \\ \qquad\qquad -\frac{\delta f_{x_f}}{\delta \Sigma[n]}\left[\frac{\delta g}{\delta \Sigma[n]}\right]^{-1}\left[\frac{\delta g}{\delta X_v[n]}\hat{x}_v[n] + \frac{\delta g}{\delta X_f[n]}\hat{x}_f[n]\right] \end{cases} \tag{8.4}$$

(8.4) peut se mettre sous forme matricielle :

$$\begin{bmatrix} \hat{x}_v[n+1] \\ \hat{x}_f[n+1] \end{bmatrix} = \begin{bmatrix} \Theta_{vv} & \Theta_{fv} \\ \Theta_{vf} & \Theta_{ff} \end{bmatrix} \begin{bmatrix} \hat{x}_v[n] \\ \hat{x}_f[n] \end{bmatrix} = \Theta_j X[n] \tag{8.5}$$

où Θ_{vv} et Θ_{ff} sont les matrices de rejection de perturbation des boucles de tension et de fréquence respectivement et Θ_{fv} et Θ_{vf} caractérisent les interactions croisées entre les boucles. La stabilité du système est déterminée en calculant les valeurs propres de la matrice Θ_j. Les valeurs propres de module supérieur à un (hors du cercle unité) indiquent que le système est instable. Le modèle non linéaire du convertisseur est détaillé en Section 2 (page 76) et le processus de détermination du vecteur initial en Section 3 (page 87).

4.2 Commentaires sur la méthode proposée

Le principal intérêt de cette méthode d'analyse de stabilité est la prise en compte des interactions croisées entre les différentes boucles de régulation. Le concepteur d'un tel système peut ainsi s'affranchir des contraintes imposées par le principe de non-

interaction entre les boucles, qui limite volontairement la bande passante d'une boucle de régulation au profit d'une autre. Dans le cas présent, la régulation de phase n'est plus nécessairement beaucoup plus lente que la régulation de tension.

Cette méthode d'analyse de stabilité reste cependant une méthode locale limitée aux petites perturbations où la linéarisation reste valide. La robustesse du système aux fortes perturbations ne peut être déterminée. Il est difficile d'estimer le domaine de validité de cette analyse et de définir ce qui relève des faibles perturbations. L'analyse en mode glissant peut fournir quelques éléments comme le domaine d'existence du mode glissant où le convertisseur converge directement ver la surface de glissement.

L'analyse des interactions croisées entre la boucle de tension et la boucle de fréquence reste un domaine non exploré. Les méthodes dites « Relative Gain Array » (RGA) et la méthode dite « iterative Relative Gain Array » (iRGA) sont utilisées pour quantifier les interactions croisées dans les systèmes multi-entrées, multi-sorties (MIMO). Néanmoins elles sont applicables sur des systèmes continus ou moyennés et linéarisés et la validité de tels outils reste à formaliser pour un système échantillonné à fréquence variable.

5 Réalisation des prototypes

Deux prototypes de régulateur employant le principe de contrôle proposé ont été réalisés et testés pendant cette thèse. Ils ont été incorporés dans un prototype de système sur puce analogique commercial représenté en Figure 5.1 (page 92). L'implantation sur silicium du contrôleur et de l'étage de puissance associé est présenté en Figure 5.2. Les principaux défis techniques de conception de ce contrôleur sont décrits en Chapitre 5 ainsi que la structure retenue pour le fonctionnement en mode discontinu du convertisseur.

L'environnement de test du convertisseur est décrit en Section 4 du Chapitre 5. À l'environnement de test standard développé pour cette gamme de produits ST-Ericsson, deux cartes électroniques ont été ajoutées pendant cette thèse comme présenté en Figure 5.16 (page 111). Une première carte présentée en Figure 5.17 (page 112) vise à émuler la charge d'un processeur vue du convertisseur DC/DC. Elle consiste en une source de courant commandée qui émule la charge électrique et un cœur digital qui permet

d'envoyer des ordres I^2C au convertisseur. Ainsi des variations dynamiques de tension d'alimentation et des transitoires de charge rapides peuvent être émulés. La seconde carte de test présentée en Figure C.1 (page 197) permet de filtrer la tension de sortie de l'étage de puissance via un filtre passe bas d'ordre 8 dont la fréquence de coupure est de 10MHz. Cette carte permet d'effectuer des Transformées de Fourrier rapides sur la sortie de l'étage de puissance du convertisseur pour analyser le comportement de la boucle de fréquence sans soucis de repliement de spectre provoqué par l'échantillonnage du signal.

6 Mesures

Les mesures les plus significatives effectuées sur le prototypes sont rassemblées et commentées en Chapitre 6. Ces résultats permettent de valider le concept du régulateur proposé ainsi que l'analyse de stabilité proposée en Chapitre 4.

6.1 Régulation de la tension de sortie

Le convertisseur régule la tension de sortie égale à la tension de référence quel que soit le courant statique de charge comme présenté en Figure 6.1 (page 117). Lorsque le courant de charge est très faible, le convertisseur fonctionne en mode de conduction discontinu ce qui augmente l'ondulation résiduelle de la tension de sortie, mais maintient le rendement global du convertisseur. La réponse transitoire du convertisseur proposé est bien asynchrone par rapport à l'horloge de référence ainsi aucune dispersion significative liée à la phase des transitoires de charge n'a été observée comme présenté en Figure 6.2 (page 118). La réponse du convertisseur sur les grandes variations de charge s'approche d'une réponse de type « Time Optimal Control » où les dépassements transitoires sont limités uniquement par le filtre passif de sortie. A faible amplitude de transitoire de sortie la réponse du convertisseur est de type linéaire tandis qu'un transitoire de forte amplitude imposera une réponse de type non-linéaire comme présenté en Figure 6.3 (page 119). La limite de fonctionnement entre ces deux types de réponse transitoire n'est pas encore bien déterminée cependant elle engendre une courbure de la courbe

représentant le déplacement transitoire de la tension de sortie en fonction de l'amplitude du transitoire de charge représenté en Figure 6.4 (page 121).

6.2 Régulation de la fréquence de découpage

La fréquence de découpage du convertisseur en fonction du courant de polarisation de la paire différentielle du comparateur de la boucle interne est présentée en Figure 6.5 (page 122). Comme modélisée dans le Chapitre 3, la fréquence de fonctionnement du convertisseur augmente avec l'augmentation du courant de polarisation de la paire différentielle d'entrée du comparateur. Cette caractéristique n'est cependant pas linéaire et le gain de l'oscillateur équivalent tend à diminuer avec l'augmentation de la fréquence de découpage du convertisseur.

La boucle de fréquence régule la fréquence de découpage du convertisseur qui dépend principalement de la tension de batterie. C'est pourquoi la fréquence de découpage du convertisseur en fonction de la tension de batterie est présentée avec et sans boucle de régulation de fréquence et pour les deux prototypes, en condition de fonctionnement typique en Figure 6.7 (page 125). La fréquence de convertisseur est effectivement fixée à la fréquence de référence (environ 3.2 MHz). La variation résiduelle de fréquence de découpage en fonction de la tension de batterie étant due à l'oscillateur de référence.

6.3 Comportement transitoire

Le comportement des boucles lors des transitoires de charge est analysé en Section 2.6 du Chapitre 6 à l'aide de cartes stroboscopiques comme celles présentées en Figure 6.8 (page 126). La tension de sortie V_o est échantillonnée à chaque front montant de la tension de sortie de l'étage de puissance, V_{LX}, et chaque période correspondante est mesurée. Lorsqu'un transitoire survient, la tension de sortie et la fréquence de découpage du convertisseur dévient l'état stationnaire. La variation de tension de sortie est compensée par la boucle de tension ce qui produit une perturbation impulsionnelle sur la boucle de phase, elle-même rapidement rejetée. Cette mesure valide l'existence d'interactions croisées entre les boucles de régulation.

La transition entre le fonctionnement en mode discontinu où la boucle de régulation de phase est désactivée et le fonctionnement en mode continu où la boucle de régulation de phase est activée, permet d'observer l'établissement de la régulation de fréquence à l'aide des cartes stroboscopiques réunies en Figures D.21a, à D.21d et D.22a à D.22d. L'effet de la taille du condensateur d'intégration de la fonction de compensation de la boucle de phase sur le temps d'établissement est mise en évidence ainsi que la convergence de la fréquence de découpage vers la fréquence de référence. Les conséquences de ce temps d'établissement sur le fonctionnement du convertisseur lorsque la charge est un cœur numérique, sont présentées plus en détail en Section 2.6.2 du Chapitre 6.

Les variations harmoniques de la charge modulent la fréquence de découpage du convertisseur. Ce phénomène est présenté en Figure 6.10 (page 129) pour différentes fréquences de charge. Lorsque la fréquence de variation de la charge est inférieure à la bande passante de la boucle de phase, la modulation de fréquence par la charge est rejetée et aucune modulation significative n'est observée (Figure 6.10a, page 129). Lorsque la fréquence de la charge est proche de la fréquence de coupure de la boucle de phase, la fréquence de découpage du convertisseur DC/DC est modulée par la charge comme présenté en Figure 6.10b (page 129). De même lorsque la fréquence de la charge est largement supérieure à la fréquence de coupure de la boucle de phase, des raies harmoniques non négligeables apparaissent sur le spectre de la fréquence de découpage du convertisseur.

6.4 Stabilité

La stabilité du convertisseur pour différents points de fonctionnement possibles est observée expérimentalement et confrontée aux résultats théoriques de la méthode présentée au Chapitre 4. Ces résultats présentés sur les Figures 6.11, 6.12 et 6.13 (respectivement pages 131, 132 et 132) valident la méthode proposée et mettent en exergue certaines limitations de calcul. Plus de détails sont fournis en Section 3 du Chapitre 6.

6.5 Ce qui pose problème

Le premier problème constaté lors de la phase de mesure est la divergence entre la fréquence de fonctionnement du convertisseur simulé et la fréquence effectivement mesurée sur les différents prototypes. Alors que le fonctionnement des boucles de tension est simulé avec précision, le fonctionnement de la boucle de fréquence est difficilement simulé même avec des modèles prenant en compte les éléments parasites extraits de l'implantation physique.

Les effets de la modulation de la tension de batterie sur la tension de sortie n'ont pus être déterminés à cause des limitations introduites par l'environnement de test. Le fonctionnement de type « Current-Mode » avec la boucle interne en mode glissant et la boucle de compensation externe, devrait permettre d'obtenir des performances de réjection des transitoires de source supérieures au contrôle par modulation en largeur d'impulsion de fonction PID.

Enfin la régulation de fréquence de découpage permet de contrôler le rendement énergétique du convertisseur mais est aussi supposée permettre un contrôle des perturbations électromagnétiques conduites générées par le convertisseur. La mise en œuvre d'une telle mesure s'est avérée incompatible avec les moyens et les procédures du partenaire industriel.

7 Conclusion

Pour le convertisseur de tension, un cœur de processeur est une charge fortement variable qui requiert une stratégie spécifique d'alimentation. L'amélioration des performances transitoires du convertisseur de tension alimentant le cœur numérique est une source d'économie d'énergie non-négligeable pour un terminal mobile. Non seulement de meilleures performances transitoires permettent de réduire la marge de tension d'alimentation utile lors des transitoires, mais aussi d'améliorer la vitesse des variations dynamiques de tension d'alimentation. La fréquence des transitoires de la charge électrique du convertisseur DC/DC formée par le circuit digital, peut être plus rapide que la bande passante des convertisseurs fonctionnant en Modulation de Largeur d'Impulsion (MLI) généralement utilisés. C'est pourquoi de nombreux condensateurs sont utilisés pour

améliorer les performances transitoires du convertisseur en MLI mais réduisent la vitesse des changements de tension d'alimentation du cœur digital. L'utilisation d'un convertisseur utilisant un contrôle asynchrone permet de dépasser les limites introduites par le fonctionnement à fréquence fixe. La fréquence de fonctionnement du contrôleur est maintenue faible pour maintenir un rendement élevé tandis que la compensation des transitoires de charge est asynchrone pour maintenir de bonnes performances transitoires.

7.1 Résumé des contributions de cette thèse

Le contrôleur développé lors de cette thèse est un convertisseur de type V^2 synchronisé par une boucle à verrouillage de phase. La boucle interne offre de bonnes performances transitoires tandis que la boucle de compensation externe améliore la précision statique du convertisseur. Enfin, la boucle à verrouillage de phase régule la fréquence de découpage moyenne du convertisseur. Au delà de ce principe de fonctionnement finalement assez simple, la conception d'un tel contrôleur présente de nombreux défis dont plusieurs ont été adressés :

- Au niveau de la conception CMOS, le principal défi a été d'intégrer tous les circuits nécessaires en maintenant la surface de la puce faible. La solution apportée est de contrôler le délais de l'oscillateur équivalent par modulation du courant de polarisation de la paire différentielle du comparateur de la boucle interne comme présenté au Chapitre 3. Cette solution a fait l'objet d'un dépôt de brevet.

- Au niveau du flot de conception, le principal défi a été de proposer des modèles des différentes boucles qui restent simples et permettent de concevoir et spécifier les différents blocs du circuit. Ces éléments ont été développés dans le Chapitre 3.

- L'analyse de stabilité du convertisseur prenant en compte les interactions entre les boucles a été adressée au Chapitre 4.

- Le dernier défi est de démontrer la faisabilité d'un tel convertisseur dans un contexte industriel. La conception de différents blocs fonctionnels comme un circuit de démarrage et un système de contrôle du convertisseur en mode discontinu ont permis cette démonstration.

Deux prototypes ont été conçus puis testés. Le premier a permis de démontrer l'intérêt de la régulation en mode glissant avec une synchronisation par boucle à verrouillage de phase. Le second prototype présenté dans le Chapitre 5 a permis d'améliorer significativement les performances du premier et grâce à l'ajout d'un module de gestion du convertisseur en conduction discontinue et a permis de démontrer les possibilités d'un tel mode de contrôle en milieu industriel.

Les principales mesures effectuées sur les prototypes sont regroupées dans le Chapitre 6. Le convertisseur présente de bonnes performances transitoires qui permettent d'envisager soit une réduction de la capacité de filtrage de sortie du convertisseur soit de réduire les marges de tension d'alimentation et d'augmenter la vitesse des modulations dynamiques de la tension d'alimentation du circuit numérique. La boucle de verrouillage de phase permet de synchroniser le convertisseur sur une horloge de référence bien que l'oscillateur équivalent formé par la boucle de régulation de tension présente un fort bruit de phase.

Les modèles de boucle proposés dans le Chapitre 3 permettent de représenter le comportement du convertisseur et de définir les éléments des différentes fonctions de compensations requises pour stabiliser le convertisseur avant même la conception CMOS des différents blocs. Ensuite l'analyse de stabilité présentée dans le Chapitre 4 permet d'affiner les paramètres des réseaux de compensation pour optimiser les performances du circuit. Le principal inconvénient de cette méthode est qu'elle nécessite un modèle précis du délai variable introduit dans la boucle, qui est difficile à obtenir autrement que par mesure expérimentale.

Le rendement du convertisseur est maintenu élevé sur une large plage de puissance de sortie. Les transitions de mode de conduction s'effectuent de manière asynchrone ainsi que la régulation de tension en mode discontinu et ne nécessitent pas d'horloge de référence. Tous ces éléments démontrent la faisabilité d'un tel contrôle en environnement industriel.

7.2 Amélioration possible à court terme

Plusieurs points nécessiteraient de plus amples investigations pour améliorer le comportement global du convertisseur. Premièrement au niveau de la conception CMOS, une étude approfondie du bruit de phase sans synchronisation de l'oscillateur équivalent permettrait d'améliorer les performances de phase du circuit tout en générant de nouvelles spécifications pour le comparateur de la boucle interne. Les autres circuits de la boucle de phase nécessiteraient des améliorations comme l'utilisation de miroirs de courant cascodés à faible chute de tension pour la pompe de charge ou un nouvel étage d'entrée pour la source de courant commandée. La machine d'état qui détermine le mode de conduction devrait aussi être améliorée par l'ajout d'un état de conduction intermédiaire entre la conduction discontinue et la conduction continue qui permettrait de redémarrer l'amplificateur d'erreur. Ce système permettrait de supprimer les phénomènes transitoires indésirables qui peuvent survenir lors du changement de mode de conduction. Cette amélioration a été portée sur le schéma du contrôleur et simulée. Enfin une procédure fiable pour modéliser le temps de délai du comparateur reste à établir.

Au niveau système, la modélisation de la réponse transitoire du convertisseur peut être améliorée. L'impédance de sortie est un critère largement utilisé pour quantifier un convertisseur cependant il a été observé au Chapitre 6 que la réponse transitoire pour les forts sauts de charge n'est plus linéaire. Un critère qui prend en compte ce phénomène et permettrait de déterminer la limite entre les deux types de réponse (linéaire et saturée) reste à déterminer. Enfin des interactions entre la boucle de tension et la boucle de fréquence ont été observées. Elles sont prises en compte dans l'analyse de stabilité, cependant un critère de quantification des interactions permettant de déterminer si les interactions sont plus ou moins fortes reste à établir.

Enfin aucune mesure n'a pus être effectuée avec un vrai processeur. Il est fort probable que de nouvelles observations du comportement du convertisseur soient découvertes lors de l'expérience. Les mesures ont été effectuées grâce à une charge qui a été spécialement conçue pour s'approcher au plus près des caractéristiques d'un vrai processeur, cependant elle mériterait plusieurs améliorations pour pouvoir être considérée comme équivalente à un vrai processeur. De plus l'environnement de test est adapté à la mise au

point du composant analogique complexe qu'est un « Analog Baseband » d'une plateforme mobile mais n'est pas prévu pour effectuer des mesures quantitatives fiables des performances du composant notamment en régime transitoire. La conception d'un nouvel environnement de test dédié à la quantification des performances du convertisseur reste l'amélioration prioritaire de ce projet.

7.3 Perspectives

Le convertisseur est représenté sous le formalisme des système multi-entrées, multi-sorties au Chapitre 4 avec une sortie de tension et une sortie de fréquence. En étendant ce principe, la conception d'un convertisseur à trois sorties avec deux sorties de tension et une sortie de fréquence peut être envisagée. La régulation des tensions peut être envisagée en régulant le mode-commun d'une part, et le mode-différentiel d'autre part des tensions de sorties, tandis que la fréquence de découpage du convertisseur à deux sorties est régulée par une boucle de phase. L'analyse de stabilité d'un tel convertisseur peut être réalisée en étendant celle proposée dans cette thèse au Chapitre 4 par l'ajout de conditions de commutation supplémentaires.

Le principe de régulation proposé dans cette thèse semble bien adapté pour le contrôle de convertisseurs DC/DC avec de hautes fréquences de découpage. Le principal défi reste la conception d'un comparateur et d'un étage de puissance présentant un délai suffisamment faible.

L'utilisation du concept présenté dans cette thèse pour le contrôle d'un régulateur multi-phase présente a minima les défis suivants :

- La mise en œuvre d'un circuit d'équilibrage des courants dans les différentes phases, adapté au schéma de régulation proposé.
- De multiples solutions de synchronisation entre phase et sur l'horloge de références sont possibles et restent à évaluer[6].
- Comment quantifier les interactions croisées ?

[6]Par exemple, est-il plus judicieux de synchroniser chaque phase sur l'horloge de référence ou d'utiliser une configuration en chaîne ?

Enfin, il est envisageable d'étendre le principe de synchronisation d'un convertisseur en mode glissant à d'autres types de convertisseur, notamment à l'élévateur de tension ou convertisseur « boost » où le contrôle par hystérésis du courant dans ce convertisseur est déjà répandu.

7.4 Est-ce bien nécessaire ?

Cette question est d'autant plus pertinente que le partenaire industriel à l'origine de cette thèse a disparu. D'un point de vue technique le contrôleur proposé présente un réel avantage en terme de performances de régulation sur le contrôle en modulation de largeur d'impulsion. Dans le contexte de l'alimentation d'un processeur, les variations de la fréquence instantanée de découpage ne semblent pas être un point bloquant ni particulièrement critique. De plus malgré quelque défauts mineurs qui peuvent être rapidement corrigés et le manque de mesure sur certaines caractéristiques, le contrôlé développé pendant cette thèse semble prometteur.

Cependant le principal défaut de ce contrôleur est sa complexité. Il est difficile de justifier de l'intérêt de trois boucles de régulation là où une seule a été utilisée pendant de longues années. De plus le processus de conception de ce convertisseur est long et requiert des compétences variées en contrôle de convertisseurs de puissance, synthèse de fréquence et conception CMOS ce qui va à l'encontre des attentes des intérêts économiques où une solution simple, avec un temps de développement très court et qui ne nécessite pas de compétences particulières est préférée.

Néanmoins le principal objectif de cette thèse est de convaincre le lecteur qu'il est possible d'envisager le contrôle d'un convertisseur de tension autrement que par modulation d'une fonction de compensation continue et que la fréquence de découpage n'est pas une frontière infranchissable. A l'issue de cette thèse de nombreuses questions ont été soulevées qui mériteraient d'être investiguées.

Appendix A

List of publications

Journal papers

- Labbe, B. Allard, B. Lin-Shi, X. ”Design and stability analysis of a frequency controlled sliding-mode buck converter”, *IEEE Transactions on Circuits and systems - part 1* vol. 61, no. 9, pp.2761,2770, Sept. 2014

- Labbe, B. Allard, B. Lin-Shi, X. Chesneau, D. ”An Integrated Sliding-Mode Buck Converter With Switching Frequency Control for Battery-Powered Applications”, *IEEE Transactions on Power Electronics* vol. 28, no. 9, pp.4318,4326, Sept. 2013

International conference papers

- Labbe, B, Chesneau, D. Allard, B, Lin-Shi, X. ”Modeling and design of an integrated sliding-mode buck converter with regulated switching frequency suitable for mobile devices”, *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, pp.893.899, 3-6 June 2013

- Labbe, B. Chesneau, D. Allard, B. Lin-Shi, X. ”Feasibility of time-delay based frequency control of a sliding-mode buck converter”, *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011)*, Aug. 30 2011 - Sept. 1 2011

Patents

- ”Switching frequency control by adjusting comparator’s bias current” US patent application No: 14/353,991
- ”A new current-mode type modulator for Step-down (buck) converter” US patent application number 13/935 filed on 7/5/2013

National conference papers

- ”Conception d’un convertisseur Buck intégré à fréquence de découpage contrôlable par modulation de temps de délai”, *15ème Journées Nationales du Réseau Doctoral en Micro-Nanoélectronique - JNRDM* 2012
- ”Un convertisseur de type Buck en mode glissant avec commande par observateur pour l’alimentation de coeurs numériques” *Journées Électroniques Technologies émergentes et Green SoC-SiP*, 2011
- ”Etude d’un convertisseur intégré de type Buck en mode glissant synchronisé en phase et en fréquence.” *Journées des Jeunes Chercheurs en Génie Électrique - JCGE* 2011

Appendix B

Sampled data complements

1 Voltage-part regulation function f_{x_v}:

Voltage-part regulation function, f_{x_v}, versus voltage state vector $X_v[0]$

Immediately:

$$\frac{\partial f_{x_v}}{\partial X_v[0]} = e^{A_v T} \tag{B.1}$$

Voltage-part regulation function, f_{x_v}, versus frequency state vector $X_f[0]$

The derivate vector is:

$$\frac{\partial f_{x_v}}{\partial X_f[0]} = \left[\begin{array}{ccc} \frac{\partial f_{x_v}}{\partial V_{pll}[0]} & \frac{\partial f_{x_v}}{\partial V_{pll_i}[0]} & \frac{\partial f_{x_v}}{\partial \Delta\Phi[0]} \end{array} \right] \tag{B.2}$$

with:

$$\begin{aligned} \frac{\partial f_{x_v}}{\partial V_{pll}[0]} &= A_v \left(\frac{\partial T_{doff}}{\partial V_{pll}[0]} + \frac{\partial V_{don}}{\partial V_{pll}[0]} \right) e^{A_v T} X_v[0] \\ &+ A_v \frac{\partial T_{doff}}{\partial V_{pll}[0]} e^{A_v T_{doff}} A_v^{-1} B_v u_1 \\ &+ A_v \frac{\partial T_{don}}{\partial V_{pll}[0]} e^{A_v T_{don}} A_v^{-1} B_v u_2 \end{aligned} \tag{B.3}$$

and:

$$\begin{aligned}\frac{\partial f_{x_v}}{\partial V_{pll_i}[0]} &= A_v\left(\frac{\partial T_{doff}}{\partial V_{pll_i}[0]}+\frac{\partial V_{don}}{\partial V_{pll_i}[0]}\right)e^{A_vT}X_v[0]\\ &+A_v\frac{\partial T_{doff}}{\partial V_{pll_i}[0]}e^{A_vT_{doff}}A_v^{-1}B_vu_1\\ &+A_v\frac{\partial T_{don}}{\partial V_{pll_i}[0]}e^{A_vT_{don}}A_v^{-1}B_vu_2\end{aligned} \tag{B.4}$$

and:

$$\frac{\partial f_{x_v}}{\partial \Delta\Phi[0]}=0_{k,1} \tag{B.5}$$

Voltage-part regulation function, f_{x_v}, versus control action $\Sigma[0]$

$$\frac{\partial f_{x_v}}{\partial \Sigma}=\left[\begin{array}{cc}\frac{\partial f_{x_v}}{\partial T_a} & \frac{\partial f_{x_v}}{\partial T_b}\end{array}\right] \tag{B.6}$$

with:

$$\frac{\partial f_{x_v}}{\partial T_a}=A_ve^{A_vT}X_v[0]+A_ve^{A_vT_a}A_v^{-1}B_vu_2 \tag{B.7}$$

and

$$\frac{\partial f_{x_v}}{\partial T_b}=A_ve^{A_vT}X_v[0]+A_ve^{A_vT_b}A_b^{-1}B_vu_1 \tag{B.8}$$

2 Frequency part

Frequency-part regulation function, f_{x_f}, versus voltage state vector $X_v[0]$

immediately:

$$\frac{\partial f_{x_f}}{\partial X_v[0]}=0 \tag{B.9}$$

Frequency-part regulation function, f_{x_f}, versus frequency state vector $X_f\left[0\right]$

$$\frac{\partial f_{x_f}}{\partial X_f\left[0\right]} = \left[\begin{array}{c|c} \left[\frac{\partial f_{x_{pll}}}{\partial X_{pll}[0]}\right] & \left[\frac{\partial f_{x_{pll}}}{\partial \Delta\Phi[0]}\right] \\ \hline \left[\frac{\partial f_{\Phi}}{\partial X_{pll}[0]}\right] & 1 \end{array}\right] \tag{B.10}$$

with:

$$\begin{aligned} \frac{\partial f_{x_{pll}}}{\partial X_{pll}\left[0\right]} &= A_{pll_0}\left(\frac{\partial T}{\partial X_{pll}\left[0\right]} + \frac{T_r}{2\pi}\left(A_{pll_1} - A_{pll_0}\right)\frac{\partial \Delta\Phi\left[t_3\right]}{\partial X_{pll}\left[0\right]}\right) X_{pll}\left[0\right] \\ &+ e^{A_{pll_0}T + \frac{\Delta\Phi[t_3]T_r}{2\pi}\left(A_{pll_1} - A_{pll_0}\right)} \\ &+ e^{A_{pll_0}T_b} A_{pll_1}\frac{\partial \Delta\Phi\left[t_3\right]}{\partial X_{pll}\left[0\right]} e^{A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}} A_{pll_1}^{-1} B_{pll_1} \end{aligned} \tag{B.11}$$

and

$$\begin{aligned} \frac{\partial f_{x_{pll}}}{\partial \Delta\Phi\left[0\right]} &= \left(A_{pll_1} - A_{pll_0}\right)\frac{T_r}{2\pi} e^{A_{pll_0}T + \left(A_{pll_1} - A_{pll_0}\right)\frac{\Delta\Phi[t_3]T_r}{2\pi}} X_{pll}\left[0\right] \\ &+ e^{A_{pll_0}T_b} A_{pll_1}\frac{T_r}{2\pi} e^{A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}} A_{pll_1}^{-1} B_{pll_1} \end{aligned} \tag{B.12}$$

and

$$\frac{\partial f_{\Phi}}{\partial X_{pll}\left[0\right]} = \frac{2\pi}{T_r}\frac{\partial T}{\partial X_{pll}\left[0\right]} \tag{B.13}$$

Frequency-part regulation function, f_{x_f}, versus control action $\Sigma\left[0\right]$

$$\frac{\partial f_{x_f}}{\partial \Sigma} = \left[\begin{array}{c|c} \left[\frac{\partial f_{x_{pll}}}{\partial T_a}\right] & \left[\frac{\partial f_{x_{pll}}}{\partial T_b}\right] \\ \hline \frac{2\pi}{T_r} & \frac{2\pi}{T_r} \end{array}\right] \tag{B.14}$$

with:

$$\begin{aligned}\frac{\partial f_{x_{pll}}}{\partial T_a} &= \left(A_{pll_0}\left(1+\frac{\partial T_{don}}{\partial T_a}\right)+\left(A_{pll_1}-A_{pll_0}\right)\frac{\partial \Delta\Phi\left[t_3\right]}{\partial T_a}\frac{T_r}{2\pi}\right)\\ &\times e^{A_{pll_0}T+\left(A_{pll_1}-A_{pll_0}\right)\frac{\Delta\Phi[0]T_r}{2\pi}}X_{pll}\left[0\right]\\ &+e^{A_{pll0}T_b}A_{pll_1}\frac{\partial \Delta\Phi\left[t_3\right]}{\partial T_b}\frac{T_r}{2\pi}e^{A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}}A_{pll_1}^{-1}B_{pll_1}\end{aligned} \tag{B.15}$$

and:

$$\begin{aligned}\frac{\partial f_{x_{pll}}}{\partial T_b} &= \left(A_{pll_0}+\left(A_{pll_1}-A_{pll_0}\right)\frac{\partial \Delta\Phi\left[t_3\right]}{\partial T_b}\frac{T_r}{2\pi}\right)\\ &\times e^{A_{pll_0}T+\left(A_{pll_1}-A_{pll_0}\right)\frac{\Delta\Phi[t_3]T_r}{2\pi}}X_{pll}\left[0\right]\\ &+A_{pll_0}e^{A_{pll_0}T_b}\left(e^{A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}}-I\right)A_{pll_1}^{-1}B_{pll_1}\\ &+e^{A_{pll_0}T_b}A_{pll_1}\frac{\partial \Delta\Phi\left[t_3\right]}{\partial T_b}\frac{T_r}{2\pi}e^{A_{pll_1}\frac{\Delta\Phi[t_3]T_r}{2\pi}}A_{pll_1}^{-1}B_{pll_1}\end{aligned} \tag{B.16}$$

The last row is due to:

$$\frac{\partial f_\Phi}{\partial T_a}=\frac{2\pi}{T_r} \tag{B.17}$$

and:

$$\frac{\partial f_\Phi}{\partial T_b}=\frac{2\pi}{T_r} \tag{B.18}$$

3 Control action function g:

Control action function, g, versus voltage state vector, $X_v\left[0\right]$

Using the sliding mode function vector, S:

$$\frac{\partial g}{\partial X_v\left[0\right]}=\begin{bmatrix} S & \dots 0 \\ 0\dots & S \end{bmatrix}\begin{bmatrix} \frac{\partial X_v[t_2]}{\partial X_v[0]} \\ \frac{\partial X_v[T]}{\partial X_v[0]} \end{bmatrix} \tag{B.19}$$

with:

$$\frac{\partial X_v\left[t_2\right]}{\partial X_v\left[0\right]}=e^{A_v\left(T_{doff}+T_a\right)} \tag{B.20}$$

$\frac{\partial X_v[T]}{\partial X_v[0]}$ has been defined in (B.1).

Control action function, g, versus frequency state vector, $X_f\,[0]$

$$\frac{\partial g}{\partial X_f\,[0]} = \begin{bmatrix} S & \dots 0 \\ 0 \dots & S \end{bmatrix} \begin{bmatrix} \frac{\partial X_v[t_2]}{\partial X_f[0]} \\ \frac{\partial X_v[T]}{\partial X_f[0]} \end{bmatrix} \tag{B.21}$$

with:

$$\frac{\partial X_v\,[t_2]}{\partial X_f\,[0]} = \begin{bmatrix} \frac{\partial X_v[t_2]}{\partial V_{pll}[0]} & \frac{\partial X_v[t_2]}{\partial V_{pll_i}[0]} & \frac{\partial X_v[t_2]}{\partial \Delta\Phi[0]} \end{bmatrix} \tag{B.22}$$

which is composed by:

$$\begin{aligned} \frac{\partial X_v\,[t_2]}{\partial V_{pll}\,[0]} &= A_v \frac{\partial T_{doff}}{\partial V_{pll}\,[0]} e^{A_v\left(T_{doff}+T_a\right)} X_v\,[0] \\ &\quad + A_v \frac{\partial T_{doff}}{\partial V_{pll}\,[0]} e^{A_v T_{doff}} A_v^{-1} B_v u1 \end{aligned} \tag{B.23}$$

and:

$$\begin{aligned} \frac{\partial X_v\,[t_2]}{\partial V_{pll_i}\,[0]} &= A_v \frac{\partial T_{doff}}{\partial V_{pll_i}\,[0]} e^{A_v\left(T_{doff}+T_a\right)} X_v\,[0] \\ &\quad + A_v \frac{\partial T_{doff}}{\partial V_{pll_i}\,[0]} e^{A_v T_{doff}} A_v^{-1} B_v u_1 \end{aligned} \tag{B.24}$$

and:

$$\frac{\partial X_v\,[t_2]}{\partial \Delta\Phi\,[0]} = 0 \tag{B.25}$$

$\frac{\partial X_v[T]}{\partial X_f[0]}$ has been defined in (B.2).

Control action function, g, versus control action, $\Sigma\,[0]$

$$\frac{\partial g}{\partial \Sigma} = \begin{bmatrix} S & \dots 0 \\ 0 \dots & S \end{bmatrix} \begin{bmatrix} \frac{\partial X_v[t_2]}{\partial T_a} & \frac{\partial X_v[t_2]}{\partial T_b} \\ \frac{\partial X_v[T]}{\partial T_a} & \frac{\partial X_v[T]}{\partial T_b} \end{bmatrix} \tag{B.26}$$

with:

$$\begin{aligned} \frac{\partial X_v\,[t_2]}{\partial T_a} &= A_v e^{A_v\left(T_{doff}+T_a\right)} X_v\,[0] \\ &\quad + A_v e^{A_v T_a} A_v^{-1} B_v u_2 \end{aligned} \tag{B.27}$$

and:

$$\frac{\partial X_v\left[t_2\right]}{\partial T_b} = 0 \tag{B.28}$$

$\frac{\partial X_v[T]}{\partial T_a}$ and $\frac{\partial X_v[T]}{\partial T_b}$ have been defined in (B.7) and (B.8) respectively.

4 Delay and period functions

T_{doff} delay versus $X_{pll}\left[0\right]$:

$$\frac{\partial T_{doff}}{\partial X_{pll}\left[0\right]} = \begin{bmatrix} \frac{\partial T_{doff}}{\partial V_{pll}[0]} \\ \frac{\partial T_{doff}}{\partial V_{pll_i}[0]} \end{bmatrix} \tag{B.29}$$

Based on the fitted delay expression:

$$\frac{\partial T_{doff}}{\partial V_{pll}\left[0\right]} = a_d b_d e^{b_d V_{pll}[0]} + c_d d_d e^{d_d V_{pll}[0]} \tag{B.30}$$

and

$$\frac{\partial T_{doff}}{\partial V_{pll_i}\left[0\right]} = 0 \tag{B.31}$$

T_{don} delay versus $X_{pll}\left[0\right]$:

$$\frac{\partial T_{don}}{\partial X_{pll}\left[0\right]} = \begin{bmatrix} \frac{\partial T_{don}}{\partial V_{pll}[0]} \\ \frac{\partial T_{don}}{\partial V_{pll_i}[0]} \end{bmatrix} \tag{B.32}$$

direct calculus gives:

$$\frac{\partial T_{don}}{\partial V_{pll}\left[0\right]} = a_u b_u \frac{\partial V_{pll}\left[t_2\right]}{\partial V_{pll}\left[0\right]} e^{b_u V_{pll}[t_2]} + c_u d_u e \frac{\partial V_{pll}\left[t_2\right]}{\partial V_{pll}\left[0\right]} e^{d_u V_{pll}[t_2]} \tag{B.33}$$

and:

$$\frac{\partial T_{don}}{\partial V_{pll_i}\left[0\right]} = a_u b_u \frac{\partial V_{pll}\left[t_2\right]}{\partial V_{pll_i}\left[0\right]} e^{b_u V_{pll}[t_2]} + c_u d_u \frac{\partial V_{pll}\left[t_2\right]}{\partial V_{pll_i}\left[0\right]} e^{d_u V_{pll}[t_2]} \tag{B.34}$$

The partial derivates of the phase filter voltage at t_2 yields from their respective expressions:

$$\frac{\partial V_{pll}\left[t_2\right]}{\partial V_{pll}\left[0\right]} = \left[\begin{array}{cc} 1 & 0 \end{array}\right] \left(A_{pll_0} \frac{\partial T_{doff}}{\partial V_{pll}\left[0\right]} e^{A_{pll_0}\left(T_{doff}+T_a\right)} X_{pll}\left[0\right] + e^{A_{pll_0}\left(T_{doff}+T_a\right)} \left[\begin{array}{c} 1 \\ 0 \end{array}\right] \right) \tag{B.35}$$

and

$$\frac{\partial V_{pll}\left[t_2\right]}{\partial V_{pll_i}\left[0\right]} = \left[\begin{array}{cc} 1 & 0 \end{array}\right] \left(A_{pll_0} \frac{\partial T_{doff}}{\partial V_{pll_i}\left[0\right]} e^{A_{pll_0}\left(T_{doff}+T_a\right)} X_{pll}\left[0\right] + e^{A_{pll_0}\left(T_{doff}+T_a\right)} \left[\begin{array}{c} 0 \\ 1 \end{array}\right] \right) \tag{B.36}$$

T period versus $X_{pll}\left[0\right]$:

Immediately:

$$\frac{\partial T}{\partial X_{pll}\left[0\right]} = \left[\begin{array}{cc} \frac{\partial T_{doff}}{\partial X_{pll}[0]} & \frac{\partial T_{don}}{\partial X_{pll}[0]} \end{array}\right] \tag{B.37}$$

5 Phase shift functions

Phase shift, $\Delta\Phi\left[t_3\right]$, versus voltage state vector, $X_v\left[0\right]$:

Obviously:

$$\frac{\partial \Delta\Phi\left[t_3\right]}{\partial X_v\left[0\right]} = 0 \tag{B.38}$$

Phase shift, $\Delta\Phi\left[t_3\right]$, versus frequency state vector, $X_f\left[0\right]$:

$$\frac{\delta\Phi\left[t_3\right]}{\delta X_f\left[0\right]} = \left[\begin{array}{ccc} \frac{\partial\Delta\Phi[t_3]}{\partial V_{pll}[0]} & \frac{\partial\Delta\Phi[t_3]}{\partial V_{pll_i}[0]} & 1 \end{array}\right] \tag{B.39}$$

with:

$$\frac{\partial \Delta\Phi\left[t_3\right]}{\partial V_{pll}\left[0\right]} = 2\pi \left(\frac{1}{T_r} - \frac{T_b}{T_r}\right) \frac{\partial T_{doff}}{\partial X_{pll}\left[0\right]} \tag{B.40}$$

and:

$$\frac{\partial \Delta\Phi\left[t_3\right]}{\partial V_{pll_i}\left[0\right]} = 2\pi\left(\frac{1}{T_r} - \frac{T_b}{T_r}\right)\frac{\partial T_{doff}}{\partial X_{pll}\left[0\right]} \tag{B.41}$$

Appendix C

Design complements

1 Phase locked loop fractional operation

Phase-locked-loop circuit includes 4-bit input and output frequency dividers that permits to synthesize a broad range of frequency. Non-unity gain phase-loop regulation engenders lot of asynchronous events that makes the recurrence model complex. Furthermore it is reasonable to assume that the desired switching clock can be directly synthesized and does not require the use of a fractional phase-locked-loop circuit to synchronize the DC/DC converter. However the added complexity is negligible and this is helpful to validate the operation of the phase-locked-loop circuit. Radio-Frequency circuits may require different specifications of power-noise spectrum related to the different radio-frequency communication protocols. To do so, the DC/DC converter that supply the radio-frequency communication components changes its switching frequency depending on the radio-frequency band used. The use of pre-and-post dividers for the switching frequency regulation paves the path to dynamic switching frequency scaling where the switching frequency is dynamically adjusted. Nevertheless such a feature appears to be suitable only for niche markets.

2 Low pass filter design

Low-pass filtering is required to avoid aliasing. A 10 MHz eighth order Butterworth filter has been designed and is presented in Figure C.1. The cutoff frequency is set below half the sampling frequency but high enough to keep a good flatness in the range of interest, i.e. up to 6 MHz. The filter attenuation is higher than 9 dB at the Nyquist rate and falls with a -80 dB per decade slope. A 2^{nd} order Sallen Key topology is used to build the four filter stages. Current Mode Feedback (CMFB) operational amplifiers in a follower configuration are used. This topology requires 2 GHz bandwidth operational amplifiers and only few CMFB amplifier references can perform this operation.

High bandwidth CMFB amplifiers are generally designed for video or high speed signal applications where the signal amplitude is lower than the square wave output of the DC/DC converter power half-bridge. The ± 2.5 V common-mode voltage input range of the THS3202 from Texas-Instrument, selected in this design, cannot handle the full power half-bridge dynamic. Thus the input signal is divided by two and the filter bandpass gain is -6 dB as presented in Figure 5.18. Input and output buffers that use same CMFB operational amplifiers in a high-bandwidth follower configuration are used before and after the low-pass filter in order to adapt the impedance and drive the output respectively.

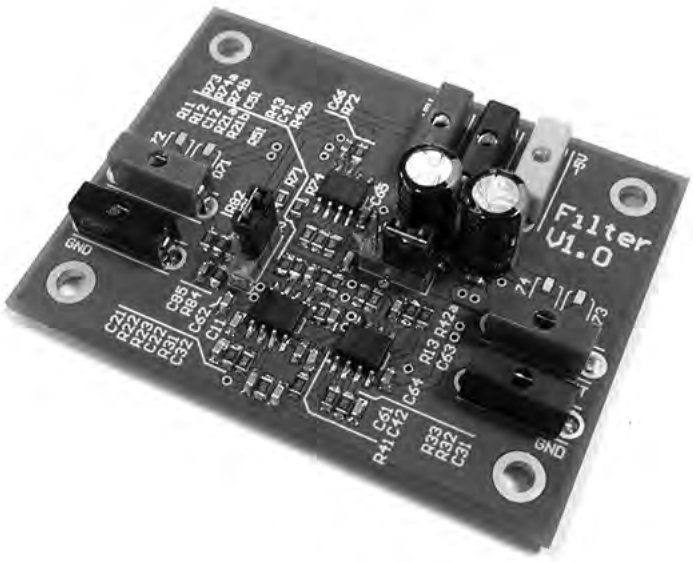


Fig. C.1 – Low-Pass filter board

Appendix D

Measurement complements

Frequency measurements

At a starting point the FFT measurement of the voltage mode PWM converter is presented in Figure D.1. The harmonic content differs from the sliding-mode converter because of the different duty cycle but the fundamental frequency is fixed at 3.2 MHz.

Figures D.2, D.3, D.4 and D.5 present the switching frequency of the DC/DC converter without phase locked loop synchronization for different bias currents.

Figure D.6, D.7 and D.8 present the switching frequency of the DC/DC converter without phase locked loop synchronization versus the comparator bias current.

Figures D.9, D.10, D.11 and D.12 present the switching frequency of the DC/DC converter with phase locked loop for the possible settings of the phase loop filter. Unstable parameters present large unwanted bands.

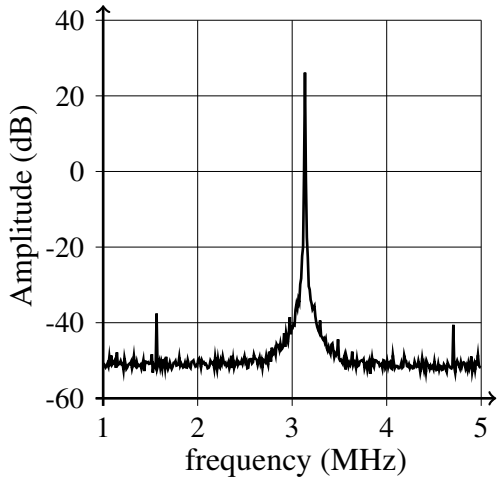
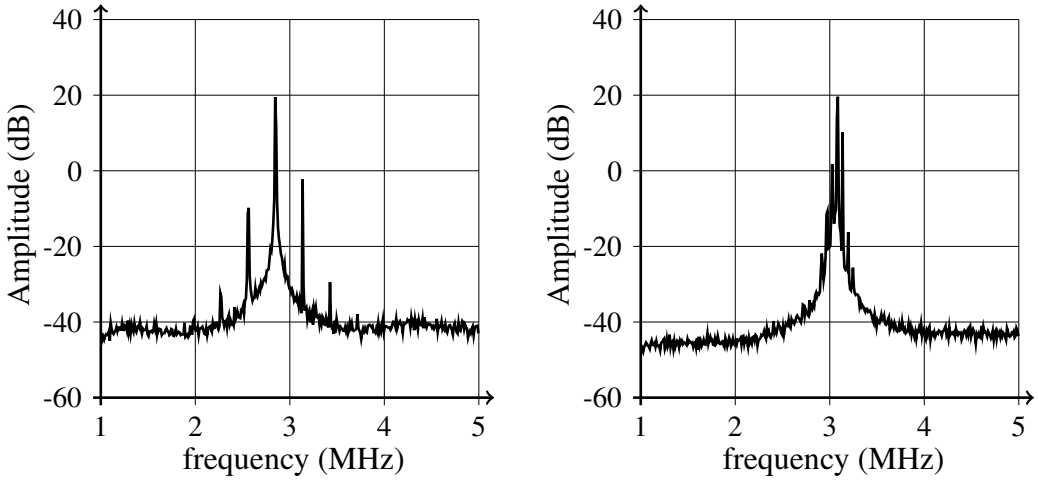
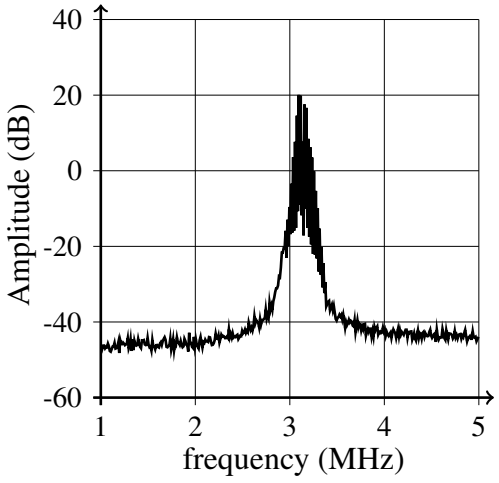


Figure D.1 – FFT measurement of the PWM voltage mode converter switching node

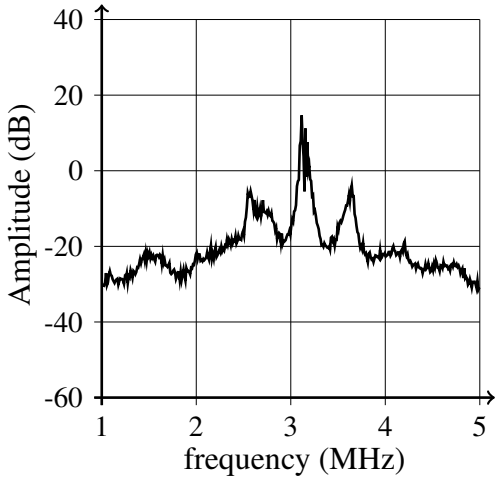


(a) $I_b = 0.5\mu A$

(b) $I_b = 1\mu A$

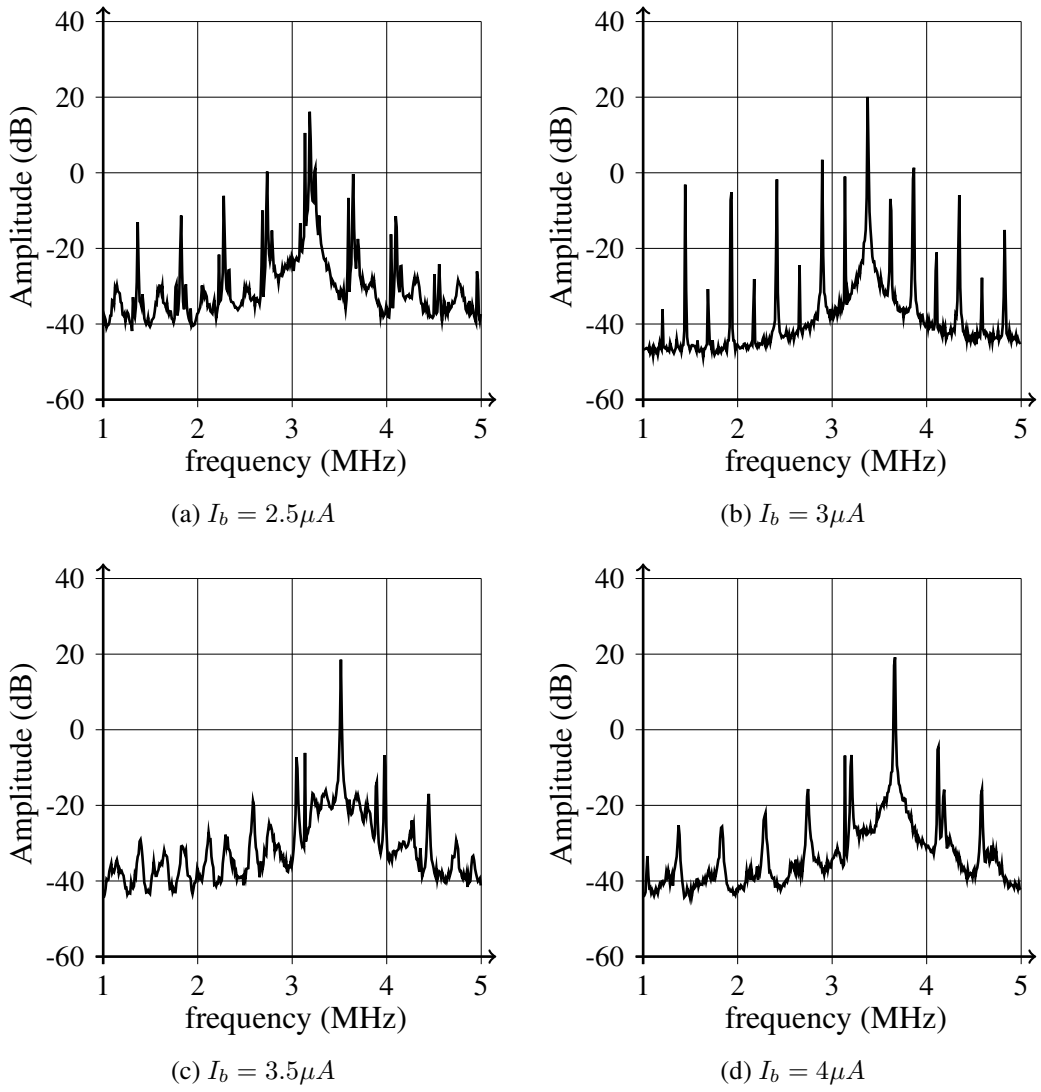


(c) $I_b = 1.5\mu A$



(d) $I_b = 2\mu A$

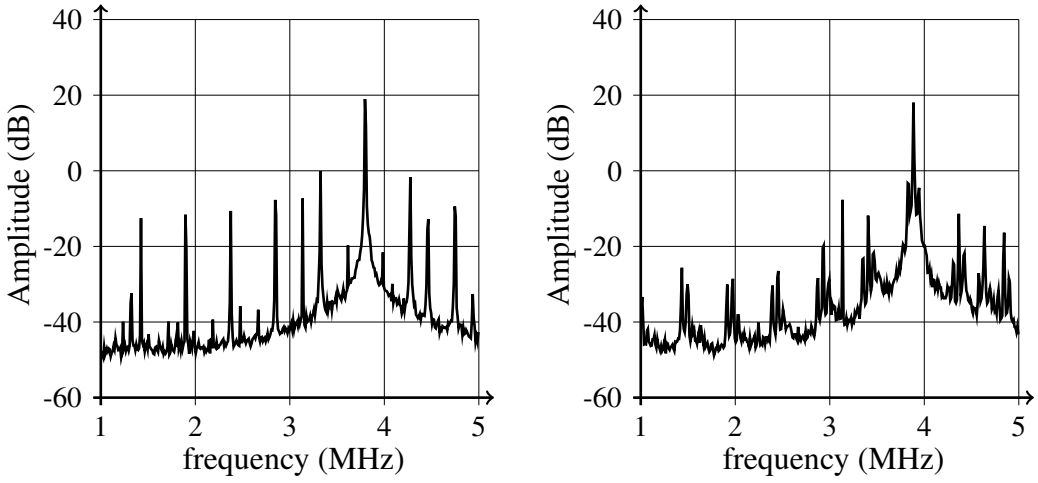
Figure D.2 – FFT measurements of the proposed converter switching node without phase loop synchronization (1)



(a) $I_b = 2.5\mu A$ (b) $I_b = 3\mu A$

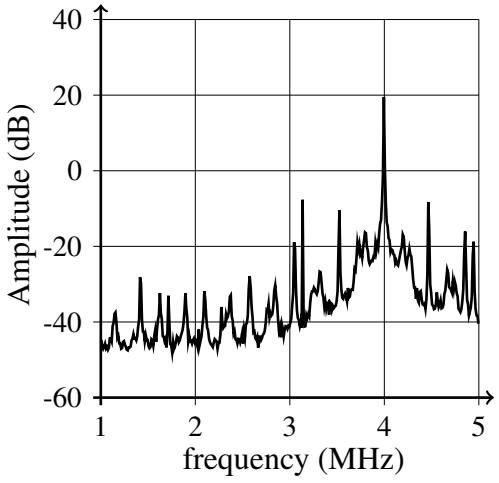
(c) $I_b = 3.5\mu A$ (d) $I_b = 4\mu A$

Figure D.3 – FFT measurements of the proposed converter switching node without phase loop synchronization (2)

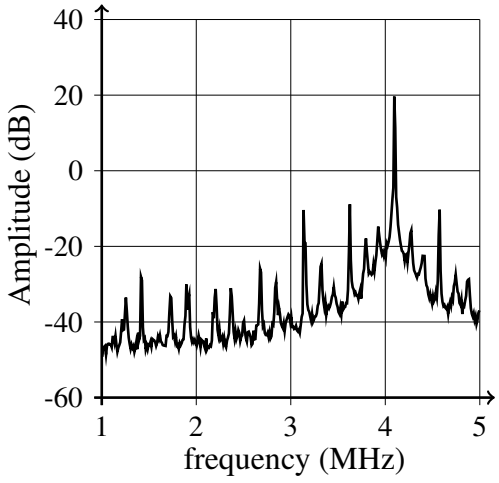


(a) $I_b = 4.5\mu A$

(b) $I_b = 5\mu A$

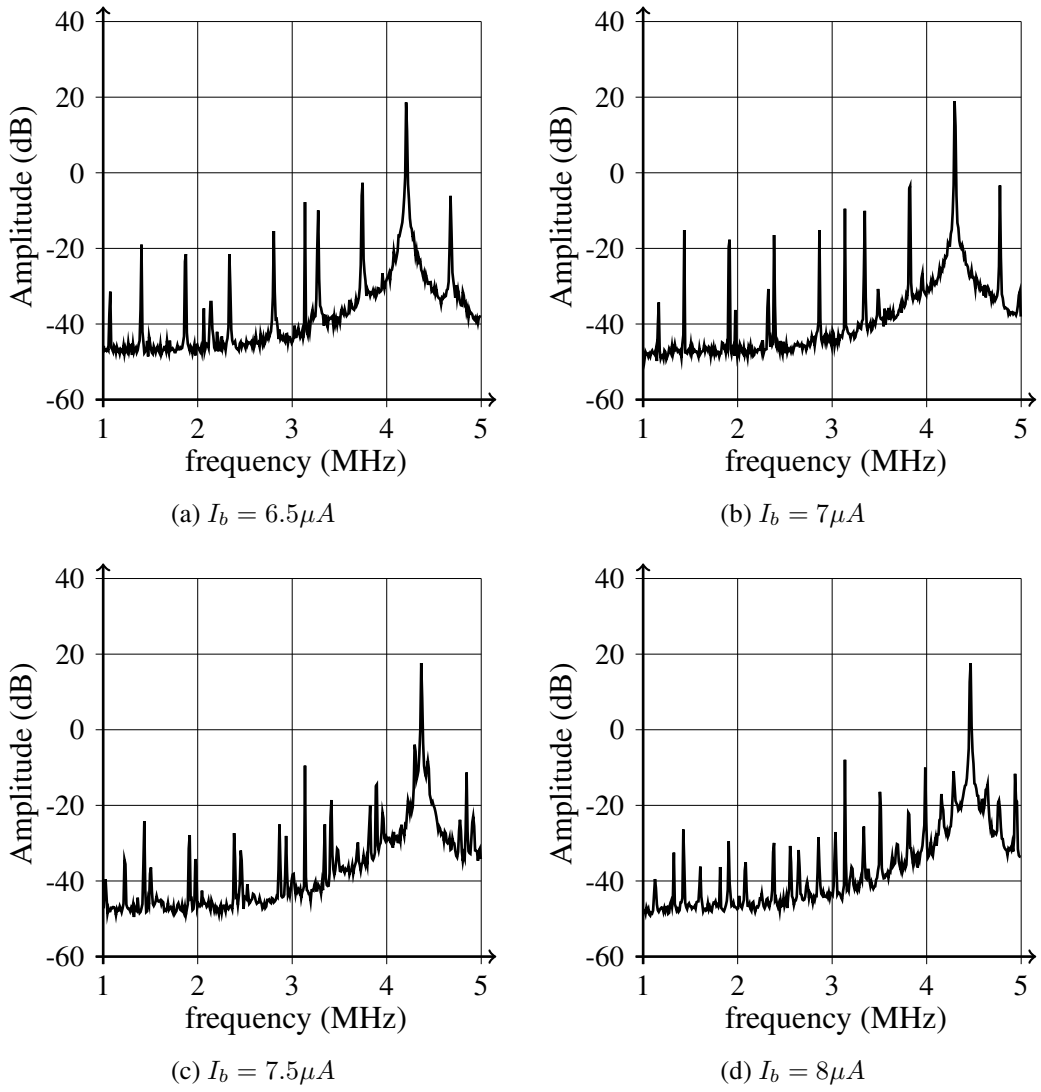


(c) $I_b = 5.5\mu A$



(d) $I_b = 6\mu A$

Figure D.4 – FFT measurements of the proposed converter switching node without phase loop synchronization (3)



(a) $I_b = 6.5\mu A$

(b) $I_b = 7\mu A$

(c) $I_b = 7.5\mu A$

(d) $I_b = 8\mu A$

Figure D.5 – FFT measurements of the proposed converter switching node without phase loop synchronization (4)

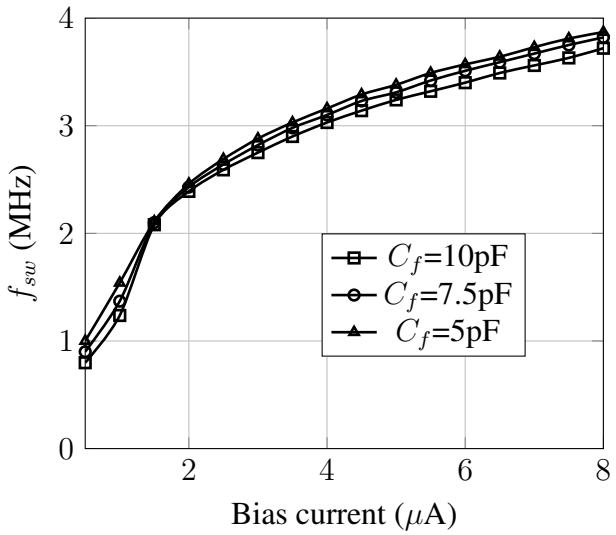


Figure D.6 – Unregulated switching frequency, f_{sw}, versus comparator static bias current, I_b. $V_{bat} = 3.6$V, $V_o = 1.2$V,$L = 470$nH, $C_o = 10\mu$F

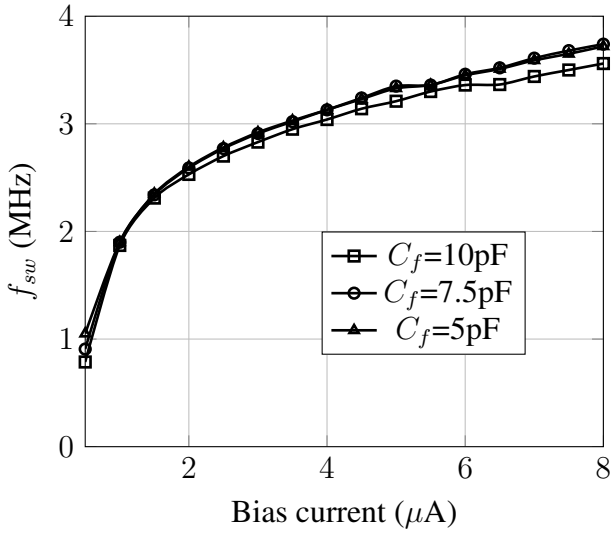


Figure D.7 – Unregulated switching frequency, f_{sw}, versus comparator static bias current, I_b. $V_{bat} = 2.3$V, $V_o = 1.2$V,$L = 470$nH, $C_o = 10\mu$F

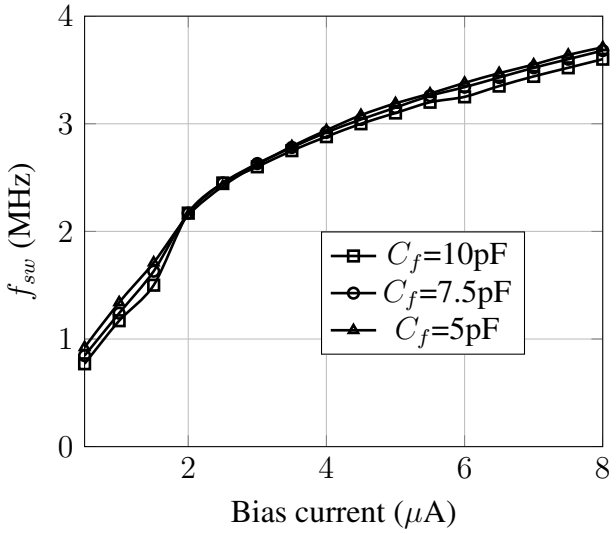
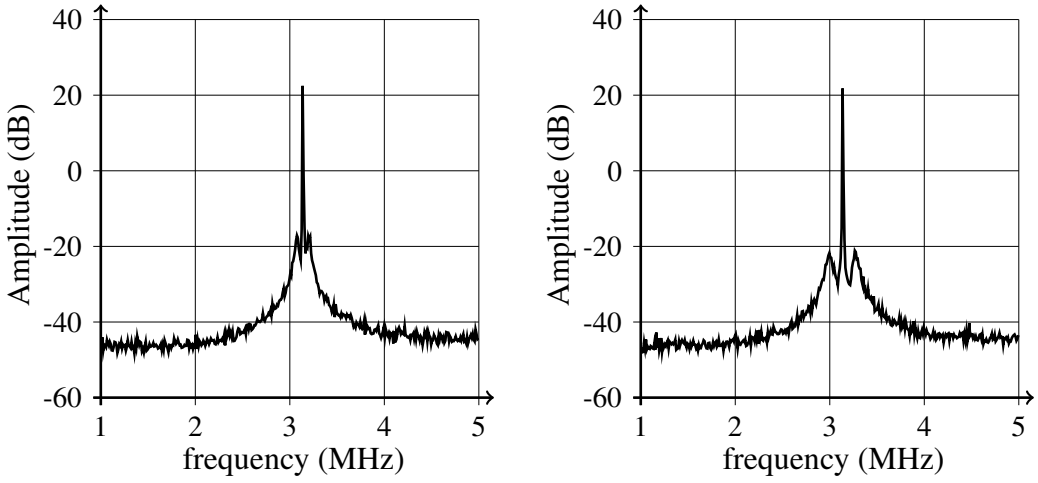


Figure D.8 – Unregulated switching frequency, f_{sw}, versus comparator static bias current, I_b. $V_{bat} = 4.8$V, $V_o = 1.2$V,$L = 470$nH, $C_o = 10\mu$F



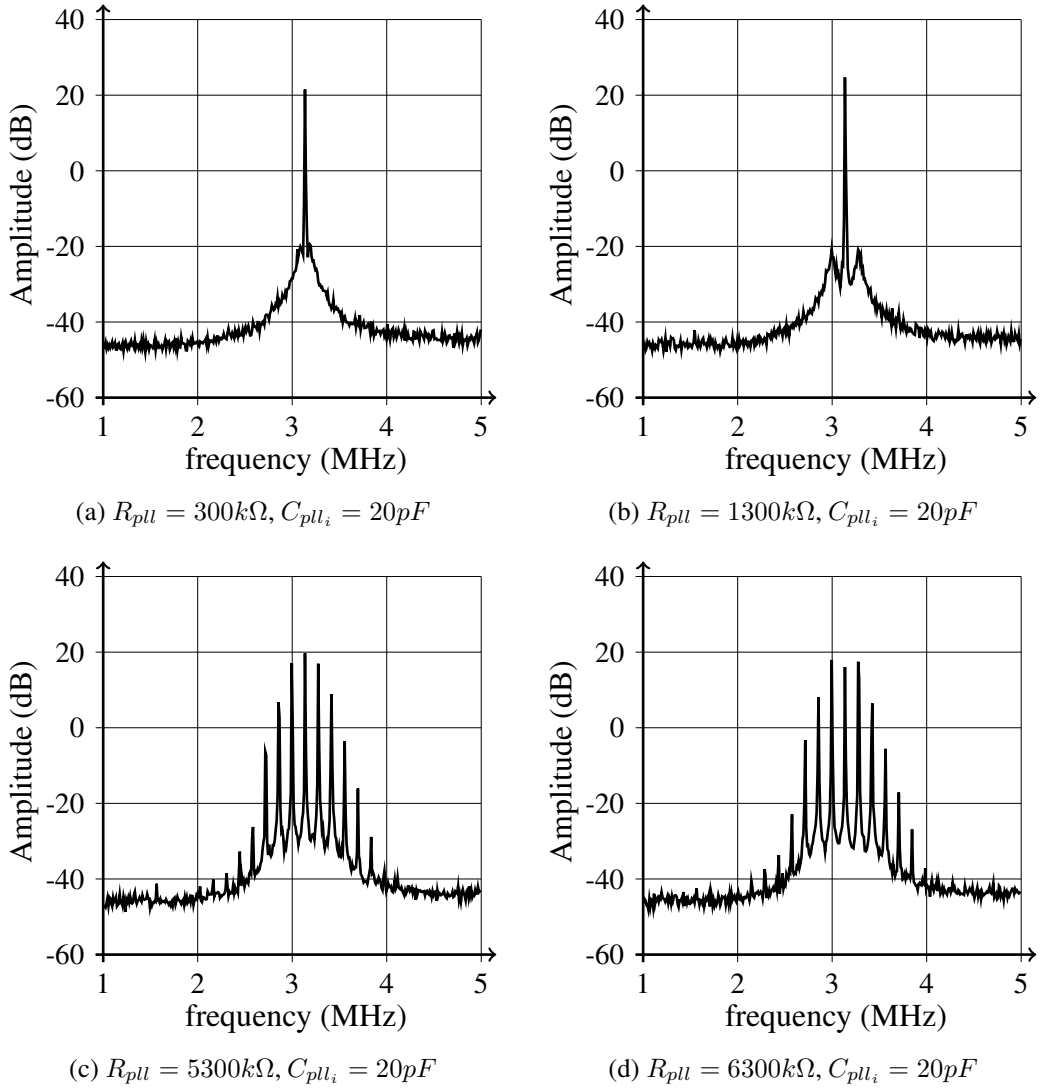
(a) $R_{pll} = 300k\Omega$, $C_{pll_i} = 10pF$

(b) $R_{pll} = 1300k\Omega$, $C_{pll_i} = 10pF$

(c) $R_{pll} = 5300k\Omega$, $C_{pll_i} = 10pF$

(d) $R_{pll} = 6300k\Omega$, $C_{pll_i} = 10pF$

Figure D.9 – FFT measurements of the proposed converter switching node with different phase loop filter settings ($C_{pll_i} = 10$pF)



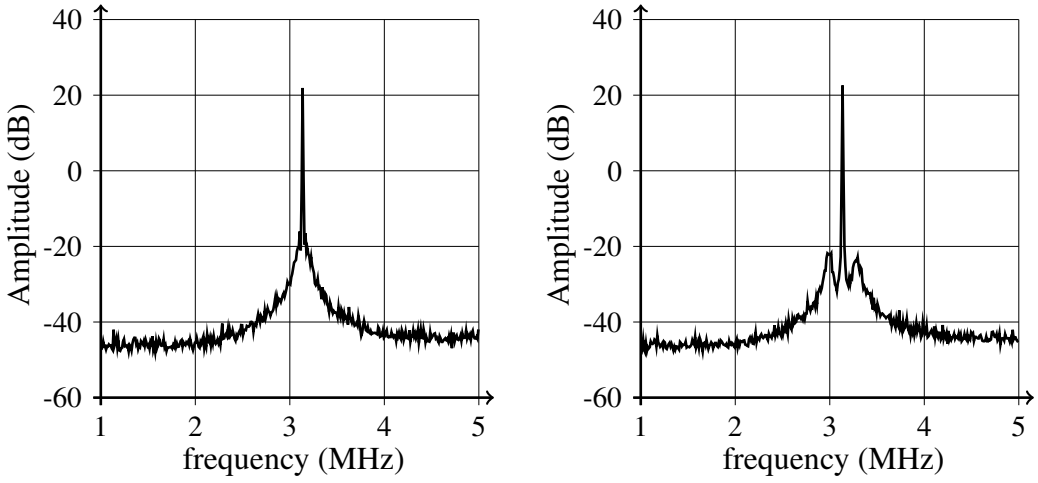
(a) $R_{pll} = 300k\Omega, C_{pll_i} = 20pF$

(b) $R_{pll} = 1300k\Omega, C_{pll_i} = 20pF$

(c) $R_{pll} = 5300k\Omega, C_{pll_i} = 20pF$

(d) $R_{pll} = 6300k\Omega, C_{pll_i} = 20pF$

Figure D.10 – FFT measurements of the proposed converter switching node with different phase loop filter settings ($C_{pll_i} = 20$pF)



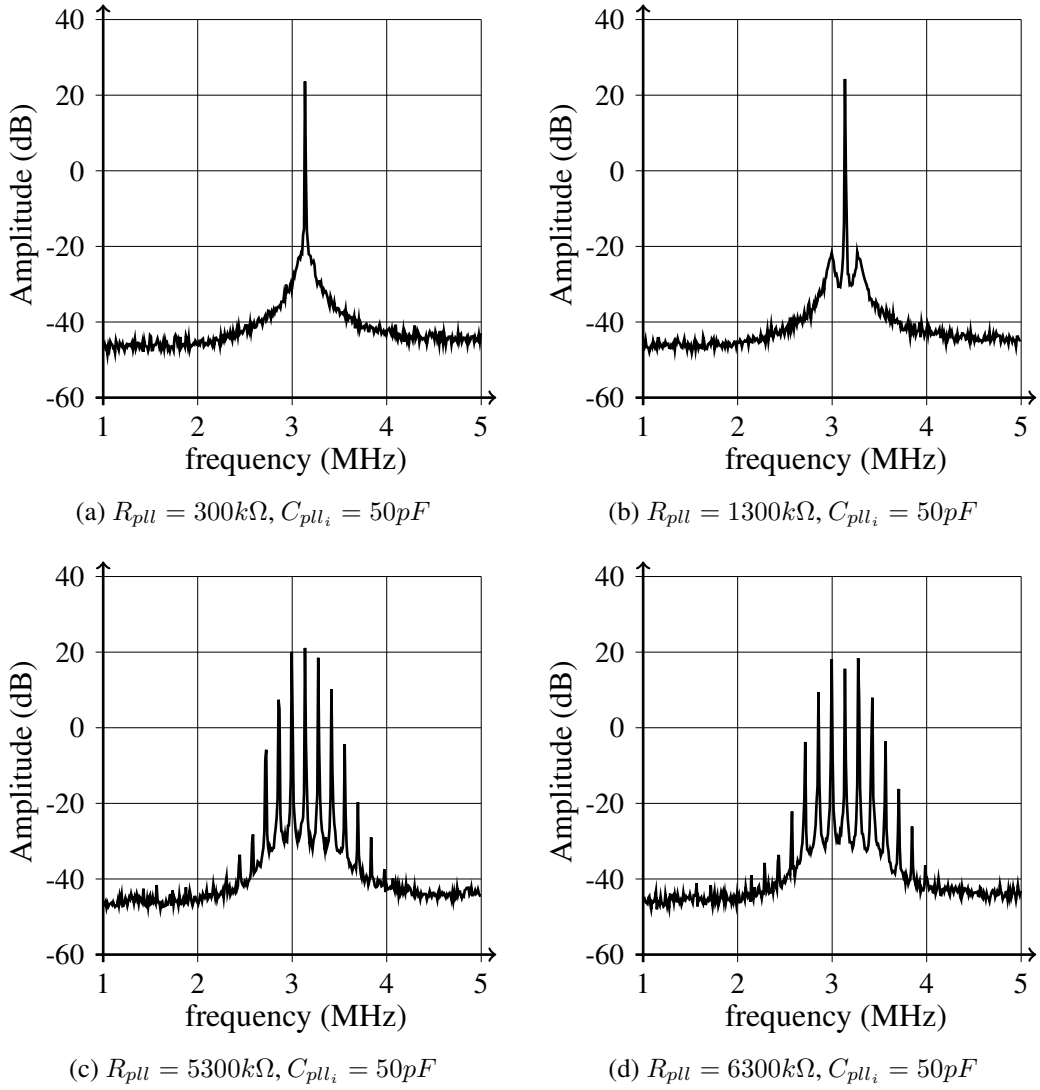
(a) $R_{pll} = 300k\Omega$, $C_{pll_i} = 30pF$

(b) $R_{pll} = 1300k\Omega$, $C_{pll_i} = 30pF$

(c) $R_{pll} = 5300k\Omega$, $C_{pll_i} = 30pF$

(d) $R_{pll} = 6300k\Omega$, $C_{pll_i} = 30pF$

Figure D.11 – FFT measurements of the proposed converter switching node with different phase loop filter settings ($C_{pll_i} = 30$pF)



(a) $R_{pll} = 300k\Omega, C_{pll_i} = 50pF$

(b) $R_{pll} = 1300k\Omega, C_{pll_i} = 50pF$

(c) $R_{pll} = 5300k\Omega, C_{pll_i} = 50pF$

(d) $R_{pll} = 6300k\Omega, C_{pll_i} = 50pF$

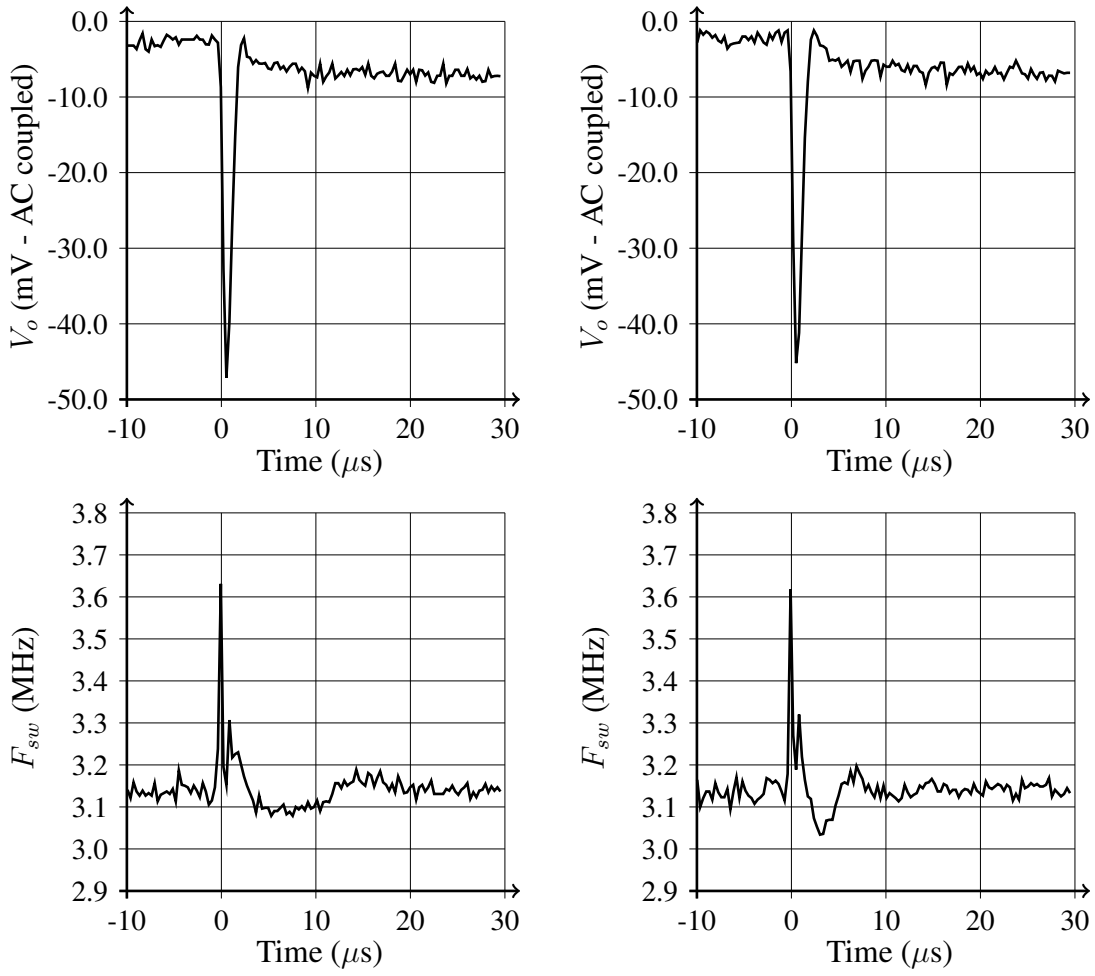
Figure D.12 – FFT measurements of the proposed converter switching node with different phase loop filter settings ($C_{pll_i} = 50$pF)

Stroboscopic maps

Stroboscopic maps are determine by sampling the output voltage at each power stage output rising edge (i.e. when the node V_{LX} rises) and each period is measured and the corresponding frequency is plotted. Figures D.13, D.14, D.15 and D.16 present the switching frequency and the output voltage trajectories of the DC/DC converter with phase synchronization during a load current rising step for different phase filter settings.

FiguresD.16, D.17, D.18 and D.19 present the switching frequency and the output voltage trajectories of the DC/DC converter with phase synchronization during a load current falling step for different phase filter settings.

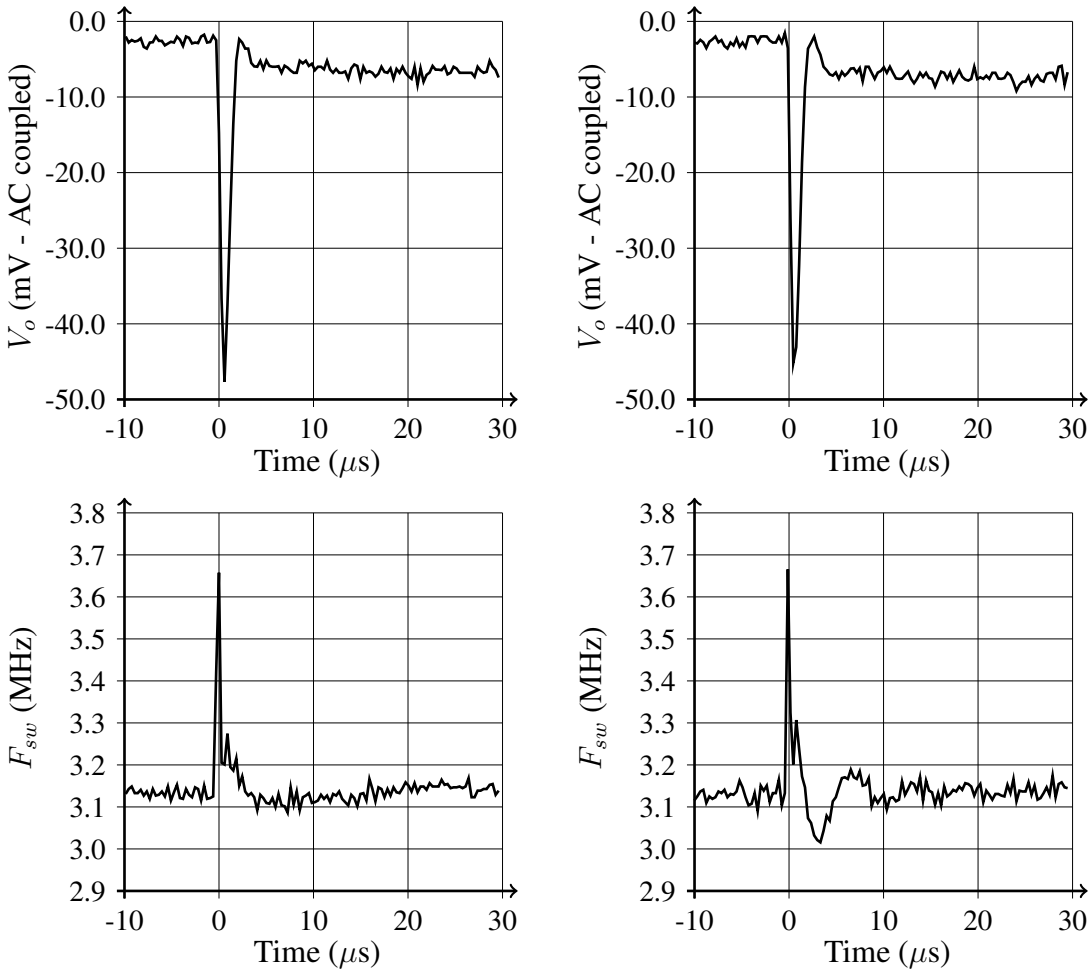
Figures D.21 and D.22 present the switching frequency of the proposed DC/DC converter with phase synchronization during a recovery from DCM operation for different phase filter settings.



(a) $R_{pll} = 300k\Omega, C_{pll_i} = 10pF$

(b) $R_{pll} = 1300k\Omega, C_{pll_i} = 10pF$

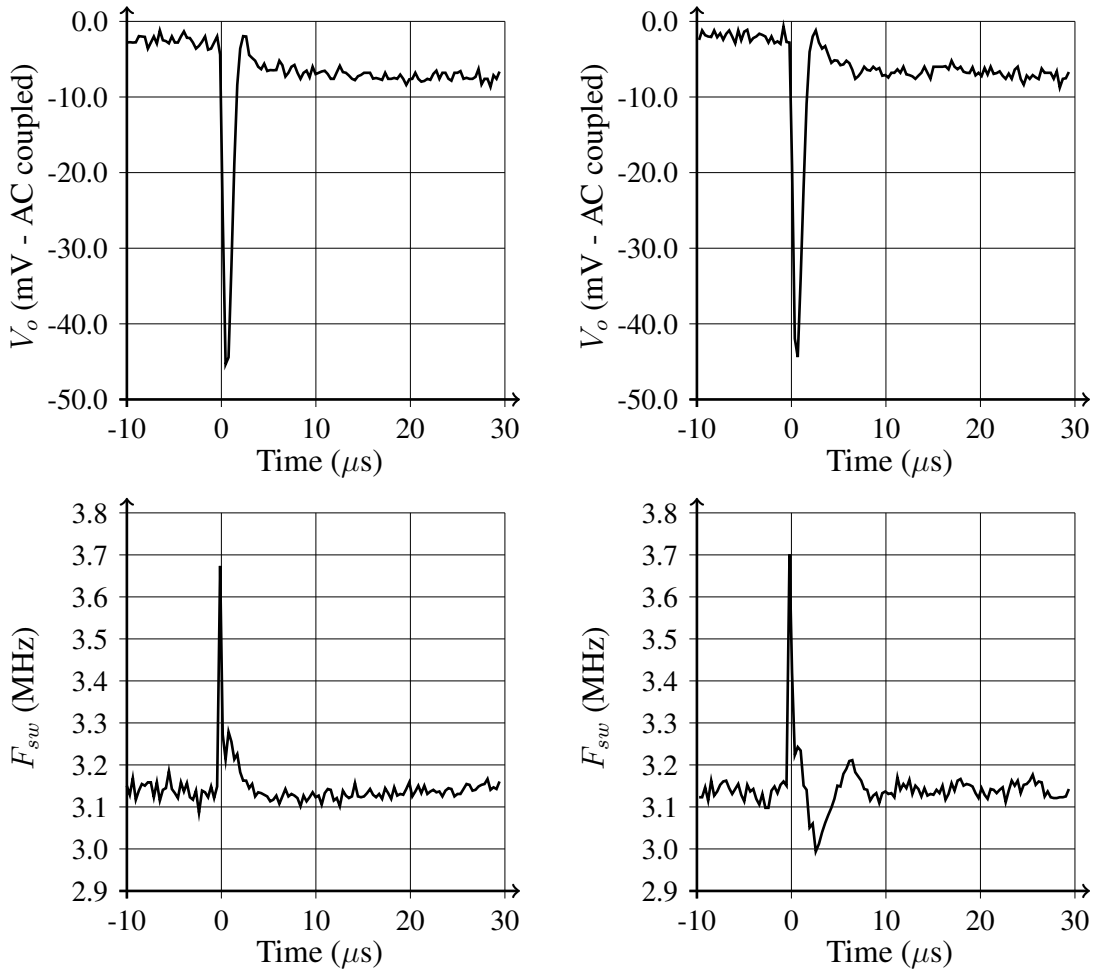
Figure D.13 – Stroboscopic plot of the output voltage (up) and switching frequency (down) during a load rising step ($C_{pll_i} = 10$pF)



(a) $R_{pll} = 300k\Omega$, $C_{pll_i} = 20pF$

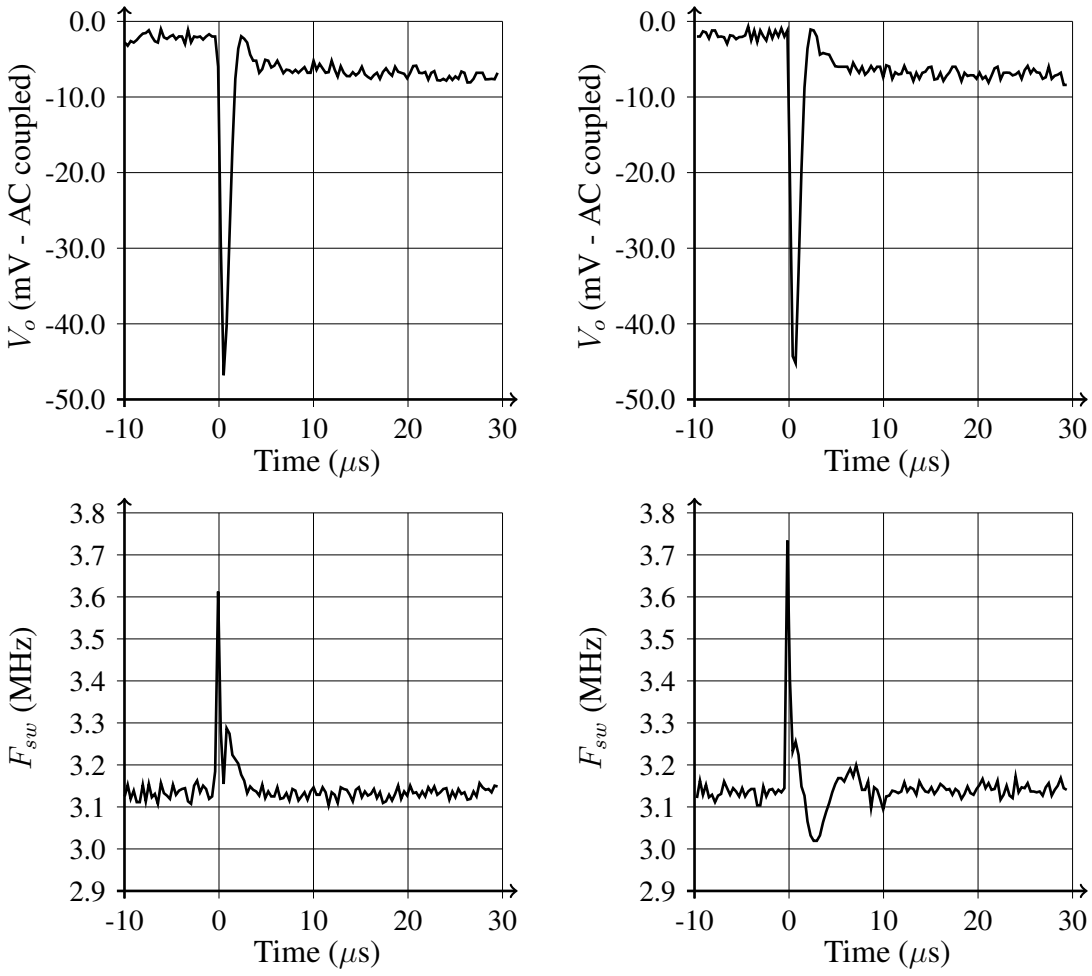
(b) $R_{pll} = 1300k\Omega$, $C_{pll_i} = 20pF$

Figure D.14 – Stroboscopic plot of the output voltage (up) and switching frequency (down) during a load rising step ($C_{pll_i} = 20$pF)



(a) $R_{pll} = 300k\Omega, C_{pll_i} = 30pF$ (b) $R_{pll} = 1300k\Omega, C_{pll_i} = 30pF$

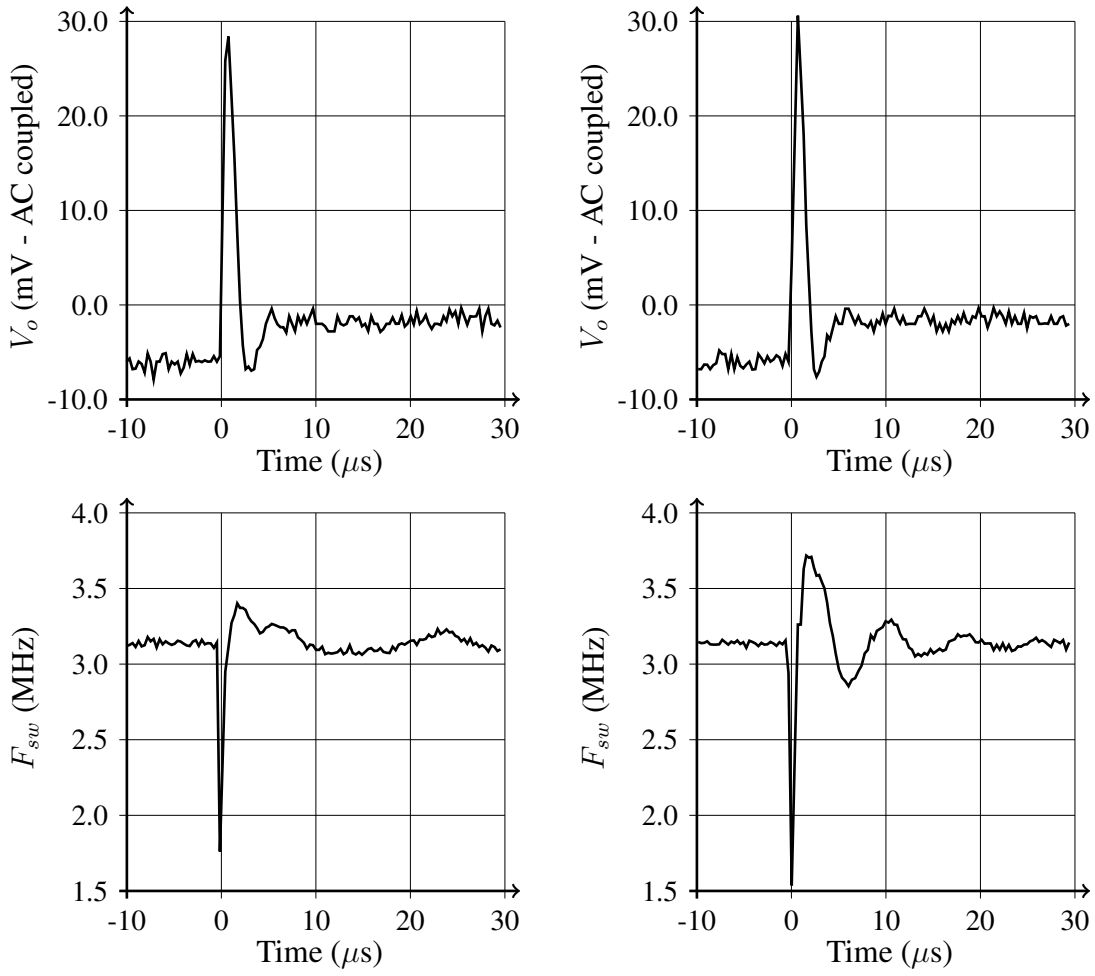
Figure D.15 – Stroboscopic plot of the output voltage (up) and switching frequency (down) during a load rising step ($C_{pll_i} = 30$pF)



(a) $R_{pll} = 300k\Omega$, $C_{pll_i} = 50pF$

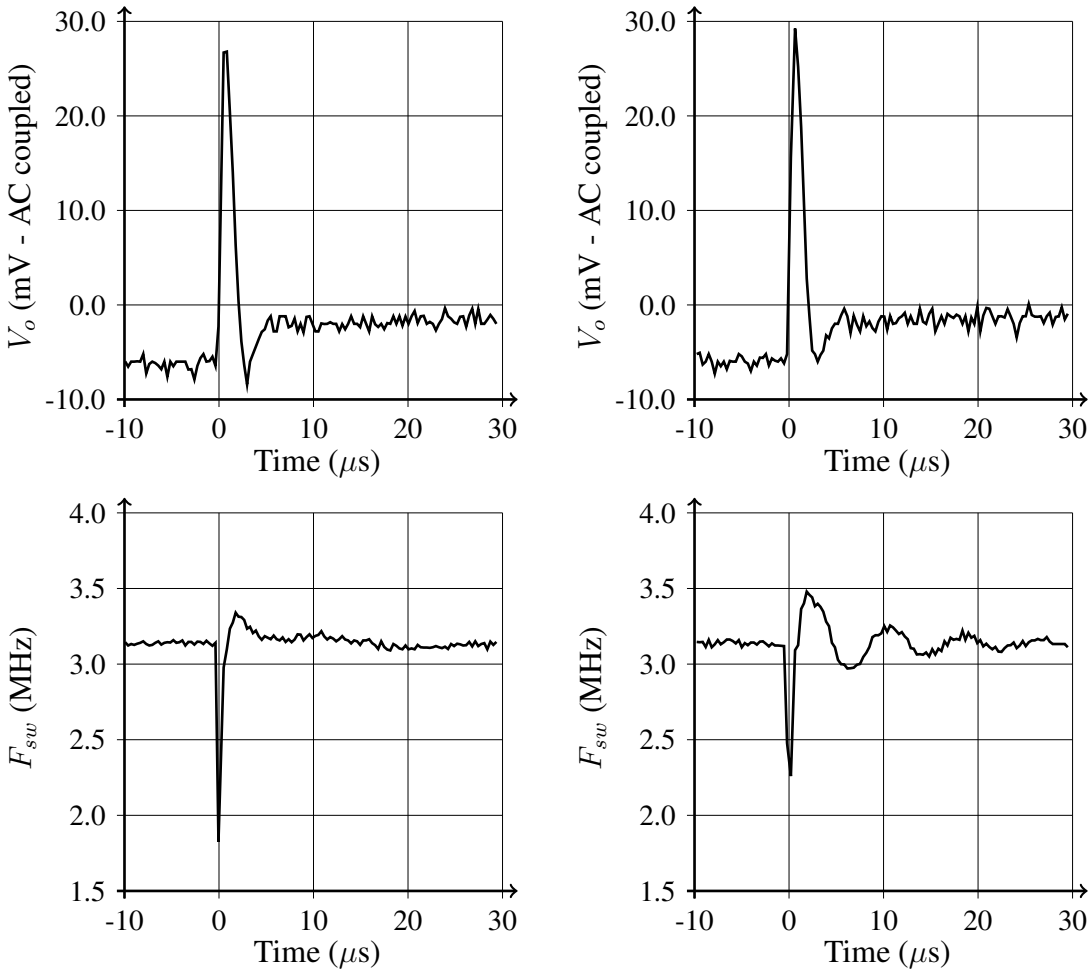
(b) $R_{pll} = 1300k\Omega$, $C_{pll_i} = 50pF$

Figure D.16 – Stroboscopic plot of the output voltage (up) and switching frequency (down) during a load rising step ($C_{pll_i} = 50$pF)



(a) $R_{pll} = 300k\Omega, C_{pll_i} = 10pF$ (b) $R_{pll} = 1300k\Omega, C_{pll_i} = 10pF$

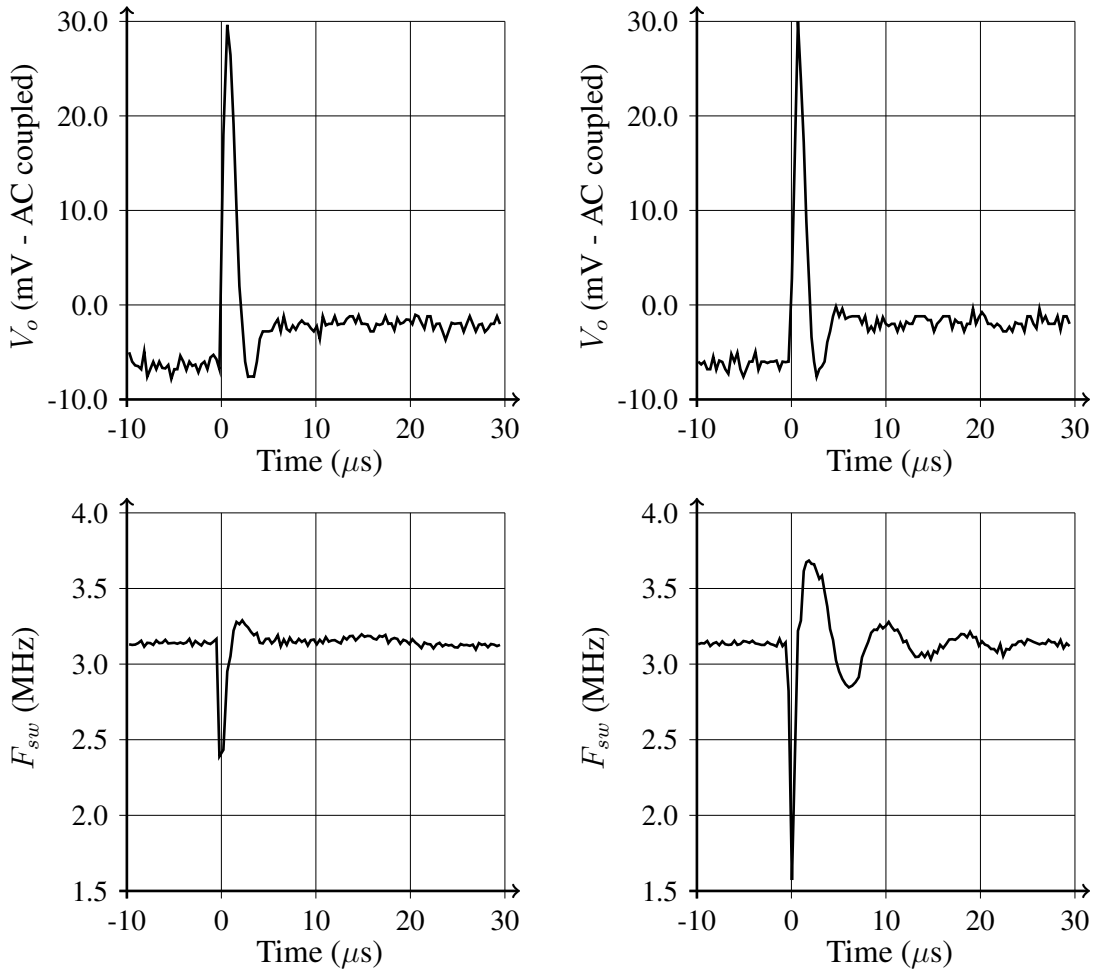
Figure D.17 – Stroboscopic plot of the output voltage (up) and switching frequency (down) during a load falling step ($C_{pll_i} = 10$pF)



(a) $R_{pll} = 300k\Omega$, $C_{pll_i} = 20pF$

(b) $R_{pll} = 1300k\Omega$, $C_{pll_i} = 20pF$

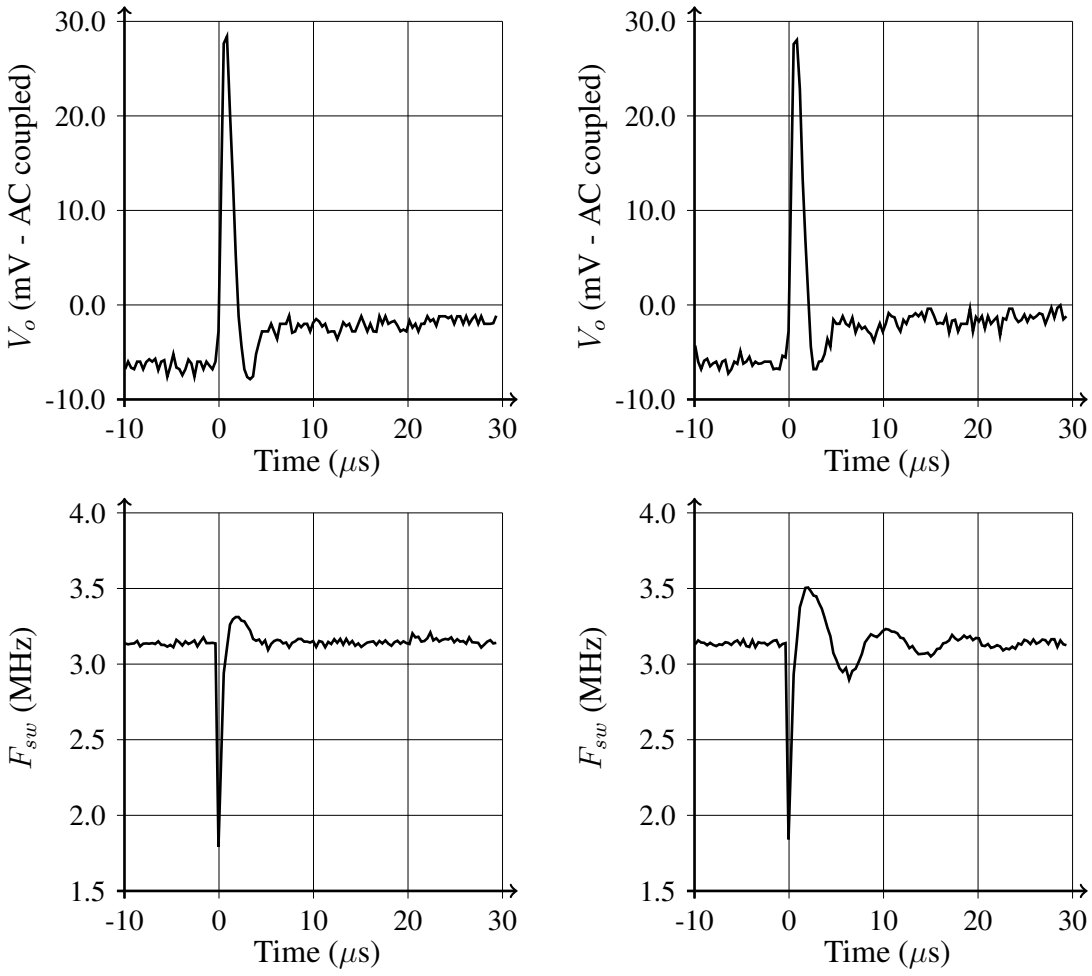
Figure D.18 – Stroboscopic plot of the output voltage (up) and switching frequency (down) during a load falling step ($C_{pll_i} = 20$pF)



(a) $R_{pll} = 300k\Omega, C_{pll_i} = 30pF$

(b) $R_{pll} = 1300k\Omega, C_{pll_i} = 30pF$

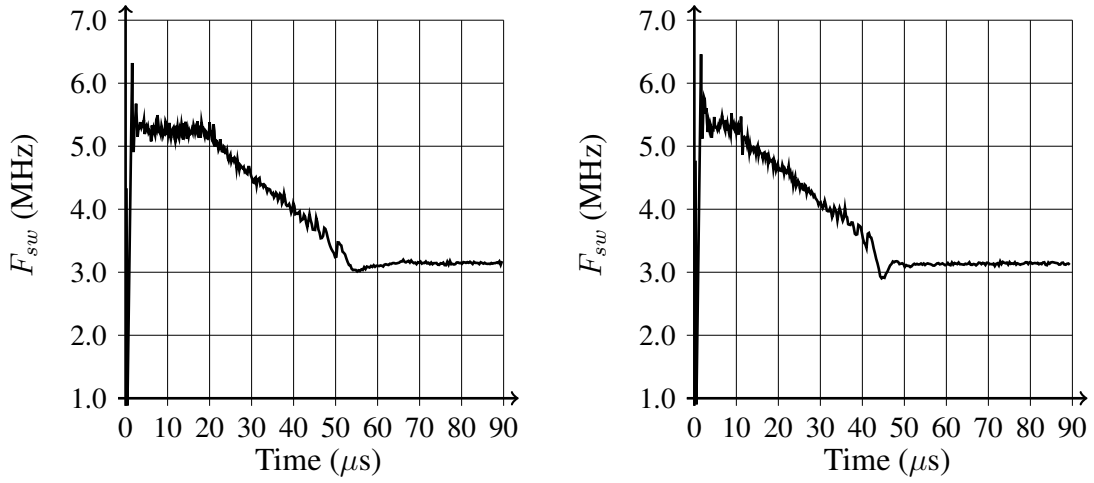
Figure D.19 – Stroboscopic plot of the output voltage (up) and switching frequency (down) during a load falling step ($C_{pll_i} = 30$pF)



(a) $R_{pll} = 300k\Omega$, $C_{pll_i} = 50pF$

(b) $R_{pll} = 1300k\Omega$, $C_{pll_i} = 50pF$

Figure D.20 – Stroboscopic plot of the output voltage (up) and switching frequency (down) during a load falling step ($C_{pll_i} = 50$pF)



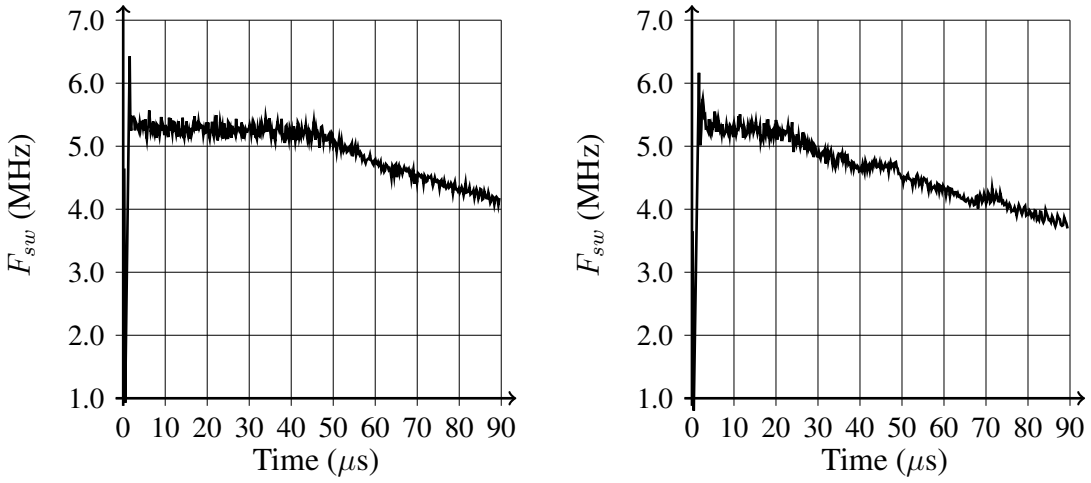
(a) $R_{pll} = 300k\Omega, C_{pll_i} = 10pF$

(b) $R_{pll} = 1300k\Omega, C_{pll_i} = 10pF$

(c) $R_{pll} = 300k\Omega, C_{pll_i} = 20pF$

(d) $R_{pll} = 1300k\Omega, C_{pll_i} = 20pF$

Figure D.21 – Switching frequency of the proposed converter when recovering from DCM mode operation - 1



(a) $R_{pll} = 300k\Omega, C_{pll_i} = 30pF$

(b) $R_{pll} = 1300k\Omega, C_{pll_i} = 30pF$

(c) $R_{pll} = 300k\Omega, C_{pll_i} = 50pF$

(d) $R_{pll} = 1300k\Omega, C_{pll_i} = 50pF$

Figure D.22 – Switching frequency of the proposed converter when recovering from DCM mode operation - 2

Other efficiency measurements

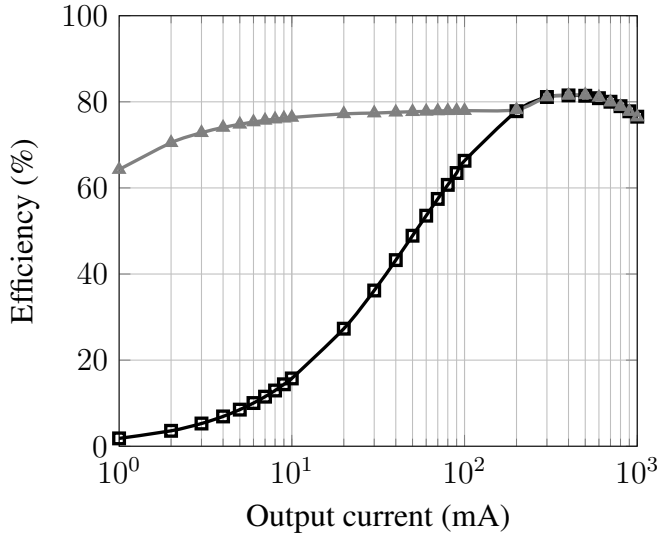


Figure D.23 – Measured efficiency of the proposed converter in typical conditions ($V_{bat} = 3.6V$, $V_{out} = 1.2V$) with (grey curve) and without (black curve) DCM implementation, $L = 240$ nH.

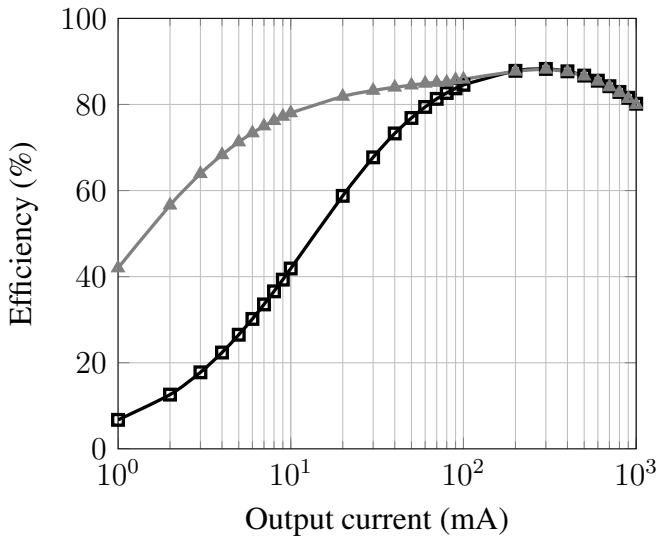


Figure D.24 – Measured efficiency of the proposed converter in typical conditions ($V_{bat} = 3.6V$, $V_{out} = 1.2V$, $f_{sw} = 3.2$) with (grey curve) and without (black curve) DCM implementation, $L = 1\mu$H