Modeling and Control of Modular Multilevel Converters (MMCs) for HVDC applications

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THÈSE

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Modélisation et Commande des Convertisseurs Modulaires Multiniveaux (MMCs) Destinés aux Réseaux HVDC

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DISSERTATION

In partial fulfillment of the requirements for the degree of

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Department: Electrical Engineering

Modeling and Control of Modular Multilevel Converters (MMCs) for HVDC applications

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Dédicace

A vous mes chers parents, mon frère Mehdi et mes deux sœurs Amira et Sana,

A mes deux beaux-frères Fouad, Hamza et toute la famille ZAMA et Loucif,

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Content

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Abstract

Common understanding today is that the challenges to develop the SuperGrid are huge at many levels (e.g.: political, societal, economical, financial, scientific, technical…). It is also commonly accepted that the SuperGrid will require novel technologies (breakers, cables, converters…) and operating principles (e.g.: transition from a more passive essentially AC-based power system to a more active AC/DC-based one). This thesis deals with the development of a key actor for SuperGrid technology, that is, AC/DC converters.

Recently, the Modular Multilevel Converter (MMC) has gained more and more importance for different applications, particularly for High Voltage Direct Current (HVDC). This topology, firstly proposed by Lesnicar and Marquardt in 2003, has many advantages compared to other Voltage Source Converter (VSC) topologies. As the name suggests, the topology is modular and easily scalable in terms of voltage levels: excellent AC output voltage and DC voltage can be easily increased by adding new cells. Moreover, thanks to the redundant cells, the MMC can also manage its internal degraded modes which are important technical and economic issues.

The development of a complex structure such as the MMC, requires a detailed analysis of its state variables and a depth understanding of its behavior when integrated. This necessitates developments of accurate models (detailed and/or simplified) and performant control systems. In 2014, when this work has started, many studies from academia as well as industry involving modeling and control of Modular Multilevel Converter have been carried out. In this thesis, these two aspects have been reviewed, analyzed and improved by proposing new models based on several implementation methods, in addition to develop innovative control algorithms in order to fulfill industrial requests by allowing fast MMC dynamics. Real time simulation as well as experimental tests have been carried out to validate our findings.

Résumé

La compréhension commune aujourd'hui est que les défis pour développer le réseau SuperGrid sont énormes et à plusieurs niveaux (p. Ex. : Politique, sociale, économique, financier, scientifique, technique ...). Il est également admis que le réseau SuperGrid nécessitera de nouvelles technologies (disjoncteurs, câbles, convertisseurs ...) et de nouveaux principes de fonctionnement (p. Ex. : transition d'un système d'alimentation passif essentiellement à base d'un réseau alternative (AC) à un système plus actif à base d'un réseau hybride alternative/continue (AC/DC)). Cette thèse porte sur la modélisation et le contrôle d'un élément clé pour les réseaux SuperGrid qui est le convertisseur AC / DC.

Récemment, et pour beaucoup d'application telle que le transport d'électricité en courant continu à très haute tension (HVDC), le Convertisseur Modulaire Multiniveau (MMC) semble devenir un élément incontournable. Cette topologie, proposée par Lesnicar et Marquardt en 2003, présente de nombreux avantages par rapport aux autres topologies de convertisseur à source de tension (VSC). Comme son nom l'indique, cette topologie est modulaire et facilement évolutive en termes de niveaux de tension : une excellente qualité de tension alternative en sortie et une tension continue qui peut être augmentée facilement en ajoutant des cellules en série. De plus, grâce aux cellules redondantes, le MMC peut également gérer ses modes dégradés internes qui peuvent donner lieu à des problèmes (techniques et économiques) importants.

Le développement d'une structure complexe telle que le MMC nécessite une analyse détaillée de ses variables d'état et une compréhension approfondie de son comportement avant son intégration. Cela nécessite des développements de modèles précis (détaillés et/ou simplifiés) et des systèmes de contrôle performants. En 2014, lorsque ce travail a débuté, une analyse de l'état de l'art des recherches et études menées par des chercheurs universitaires et industriels impliquant la modélisation et le contrôle-commande des MMC a été réalisée. Dans cette thèse, ces deux aspects principaux ont été revus, analysés et améliorés. D'abord en proposant de nouveaux modèles et méthodes de mise en œuvre, ensuite en développant des algorithmes innovants pour répondre aux demandes industrielles permettant une dynamique rapide pour le MMC. Des simulations en temps réel ainsi que des tests expérimentaux ont été réalisés pour valider ces résultats obtenus.

List of Publications

The publications resulting from this thesis are listed below:

Patents

- **A. Zama**, S. Bacha, A. Benchaib, D. Frey, and S. Silvant, “Procédé de simulation d’un convertisseur modulaire multiniveaux y compris dans l’état bloqué.” **Patent No FR3053494 - 2018-01-05 (BOPI 2018-01), Patent family FR3053494A1.**
- **A. Zama**, A. Benchaib, S. Bacha, D. Frey, and S. Silvant, “Procédé de contrôle d’un convertisseur modulaire multi-niveaux” **Patent No FR3054754 - 2018-02-02 (BOPI 2018-05), Patent family WO2018024977A1; FR3054754A1.**
- **A. Zama**, M. Romero, A. Benchaib, and B. Luscan: “Dispositif de contrôle d’un terminal pour le rétablissement de la puissance dans une installation”, **Applied for a patent, 20/04/2017.**

Journal papers

- **A. Zama**, S. Bacha, A. Benchaib, D. Frey, and S. Silvant, “A novel modular multilevel converter modeling technique based on semi-analytical models for HVDC application”. **Journal of Electrical Systems**, 12(4), (2016).
- **A. Zama**, A. Benchaib, S. Bacha, D. Frey, and S. Silvant, “High Dynamics Control for MMC Based on Exact Discrete-Time Model with Experimental Validation”. **IEEE Transactions on Power Delivery**.
- **A. Zama**, A. Benchaib, S. Bacha, D. Frey, and S. Silvant, “Discrete-Time Sliding Mode Control for Modular Multilevel Converters (MMCs): Validation under Fault Grid Operation mode”. **Submitted for IEEE Transactions on Industrial Electronics.**

Conferences papers

- **Ahmed Zama**, "A Review of Modular Multi-Level Converter (MMC) Modeling for HVDC Application." In Journée des jeunes chercheurs en génie électrique, Cherbourg, France. June 2015.

- **A. Zama**, S. Bacha, A. Benchaib, D. Frey, and S. Silvant, "A Novel Modular Multilevel Converter Modelling Technique Based on Semi-Analytical Models." In international Conference on Renewable Energy: Generation and Applications (2016).
- **A. Zama**, D. Frey, A. Benchaib, S. Bacha, B. Luscan, and S. Silvant, "Optimisation des Pertes par Commutation dans un Convertisseur Modulaire Multiniveaux (MMC)." In Symposium de Genie Electrique (SGE 2016), June. 2016, conference location : Grenoble.
- **A. Zama**, S. Ait Mansour, D. Frey, A. Benchaib, S. Bacha and B. Luscan,"A Comparative Assessment of Different Balancing Control Algorithms for Modular Multilevel Converter (MMC)", In press, the 18th European Conference on Power Electronics and Applications (EPE 2016), Sept. 2016, conference location: Karlsruhe.
- **A. Zama**, A. Benchaib, S. Bacha, D. Frey, and S. Silvant, "Advanced MMC Current Controllers with Experimental Validations Using OP1200 Test Bench". 9ème Conférence Internationale sur la Simulation Temps Réel par OPAL-RT Delivery (RT'17), Sept 2017, conference location : Montréal.

General Introduction

Thesis context

Nowadays, energy systems are facing many requirements and challenges which need a paradigm-shift. Political and public willingness to increase energy independency, reduce greenhouse gas emissions and increase exchange capabilities require urgent actions in order to meet such ambitious targets. To do so, it is highly expected that the integration of large amount of renewable energy systems will play a crucial role for future power systems. In addition, in order to increase the robustness of the actual systems and create a large electric network, the interconnection of different countries and continents can be considered as a good solution. In order to achieve a good power distribution, we cannot rely only on Kirchhoff laws. The insertion of power electronic devices associated to new control concept and the increase of the submarine links capacities will enhance the management of the energy fluxes. It is therefore necessary to look for an optimum transmission solution (economical, technical, financial…) to meet all these needs.

High Voltage Direct Current (HVDC) based on Voltage Source Converter (VSC) technology has broadly appeared as a good solution to answer this question. Several HVDC projects have been developed or currently planned around the world: Trans Bay Cable, (USA), INELFE (France-Spain), Rio Madeira (Brazil), Nanao multi-terminal VSC-HVDC (China)…This will lead to the development of meshed grids including Multi terminal DC grid (MTDC) which opens an opportunity for hybrid AC/DC transmission systems. For this purpose, new operation philosophies as well as sophisticated equipments to operate such new transmission systems are more and more required. Considerable researches are carried out today to meet these needs such as:

- Define new DC grid code.
- Investigate the interaction between AC and DC grids.
- Develop new equipment: cables, breakers, power converters, surge-arresters…

One of the key actors for HVDC technology development is the AC/DC converter. Various VSC topologies, including two-level, three-level and floating capacitor converters have been proposed in the literature. For further improvements of power quality and reliability, the Modular Multilevel Converter (MMC) has been gathering considerable attention since its

invention. Thanks to its scalability, performance and efficiency, this topology is considered as the most promising solution for AC/DC converter for HVDC applications.

This thesis deals with the development of models and associated controls of MMCs. The large number of switching elements and state variables inside of the MMC introduce modelling challenges especially when implemented in electromagnetic transient (EMT) programs for simulation purpose. Moreover, the control system for this structure is a bit different than other VSC topologies, since the storage management is not the same, which necessitates a special attention. More specifically, this thesis investigates these two aspects in order to well understand these challenges and propose new solutions.

The first contribution of this thesis is the development of new models (full order and reduced order), based on different implementation techniques. The obtained models allow to reduce the switching elements leading to facilitate their implementation in EMT programs and, hence, accelerate the simulations. The second contribution is to propose new control algorithms for current controllers. Two methods have been used to derive their control laws which allow to obtain the fastest response time.

Main objectives and thesis methodology

The focus of this thesis covers the modeling and control of MMC, its main objectives are:

- Investigate the existing MMC model types (detailed, equivalent and averaged).
- Propose new implementation techniques including analytical equations for existing models to reduce computational time.
- Identify the effect of Balancing Control Algorithm (BCA) regarding MMC operation as well as its dimensioning criteria.
- Propose new advanced control algorithms for current loops when the cascaded control approach is used.
- Integrate the sampling period of hardware control in the control algorithm of current loops to go further in term of response time.

- Explore the possibility of accelerating the outer layer such as the energy loop.

The obtained results in this thesis are mainly derived from theoretical analysis of the considered converter topology (MMC based on Half-Bridge Sub-Modules). This is achieved by, first, deriving different analytical expressions for several model types. After that, the simplified models are used to perform theoretical analysis of MMC operation which leads to propose new control algorithms. The obtained results, in term of modeling and control, are then validated either by offline/Real-time simulations or by experimental tests.

Thesis outline

This thesis is organized as follows:

Chapter 1: This chapter introduces the HVDC grid technology and its principle. First, the HVDC configurations are presented with their associated advantages and drawbacks. After that, the main AC/DC converter technologies which are Line-Commuted Converter (LCC) and Voltage Source Converter (VSC) are presented and compared. Finally, the advantage of MMC compared to other VSC topologies are shown in order to understand the motivation behind the focus of the thesis.

Chapter 2: This chapter deals with the modeling of MMC. In order to well understand this research axis, the problematic related to its dynamics modeling is addressed. After a state of the art based on recent bibliography references, three dynamic models are chosen to address thesis contributions in the field of MMC modeling which are: detailed, equivalent and averaged models. For the considered models, new implementation methods are developed, explained and validated.

Chapter 3 and chapter 4: These two chapters cover the problematic related to the control of MMC. Chapter 3 introduces the MMC control principle and its two main layers. These latter are explained and reviewed based on recent bibliography publications with the conclusion that the energy based control allows to obtain a better control of all MMC variables. The cascaded structure which is based on time scales assumption allows to handle the control objective in a decoupling manner. Such decoupling necessitates slow response time for outer loops (control objectives) in order to maintain the time ratio between the layers. Chapter 4 proposes high

dynamics controllers for inner loops in order to accelerate the response time of outer ones. Based on exact discretization of MMC state-space models, two control methods have been used to derive current control laws which are: pole placement method and discrete-time sliding mode control. Offline simulations have demonstrated that the proposed controls present many advantages in terms of performances on one hand and allow to accelerate the outer loops such as energy loop (5 ms) on the other hand.

Chapter 5: The aim of this chapter is to validate the previous results on real time simulation test bench. Before going to Rapid Control Prototyping (RCP) test, Hardware in the Loop (HIL) validation is used to anticipate some constrains such as measurements delay and noises. Small scale MMC has been sized in order to have the same dynamics as a real MMC which will be used for the RCP test. The experimental results show a good correlation with simulation ones.

CHAPTER I HVDC Technology and Architectures

1. Introduction

This chapter provides a brief introduction to HVDC transmission system followed by the chronological evolution of various AC/DC converter employed for such application. This permits to better understand the advantages carried with the Modular Multilevel Converter and the motivations behind the research works involving this topology. An overview of development trends regarding MMC topologies ends this chapter.

2. Needs for HVDC

Since the 19th century, the HVAC (High Voltage Alternating current) has been the dominant solution for transmitting electrical power over long distances; transferring power from generating stations to electrical substations. However, due to technological and stability constraints, the maximum transfer capability is limited. This is especially the case when the series and shunt compensations cannot be incorporated in the transmission system (e.g. submarine cables) [1].

With technological innovations, notably in power electronics, HVDC technology has emerged as a promising solution for such application. Compared to the HVAC solution, the HVDC allows to overcome several constraints related to the old solution [2, 3, 4]:

- Reduce the investment cost when the distance becomes higher than a specific one, so-called “break-even distance”: around 600 km for overhead lines and 50 km for submarine ones.
- No distance limitation regarding stability matter.
- Integration of renewable energy located far from consumption (e.g. wind farm energy).
- Great power transfer capability per conductor.
- Power factor is always unity: line does not require reactive compensation.
- Reduce line losses: skin effect is absent in DC technology.
- Asynchronous interconnection can be achieved which is not possible using HVAC.

- Low short circuit current.
- Less radio interference with nearby communication lines.
- Ground return can be used in some cases.

3. High voltage direct current

3.1. Concept

The HVDC system allows to transmit power in DC form. This is achieved through power converters which are able to convert electrical energy from AC to DC or vice versa.

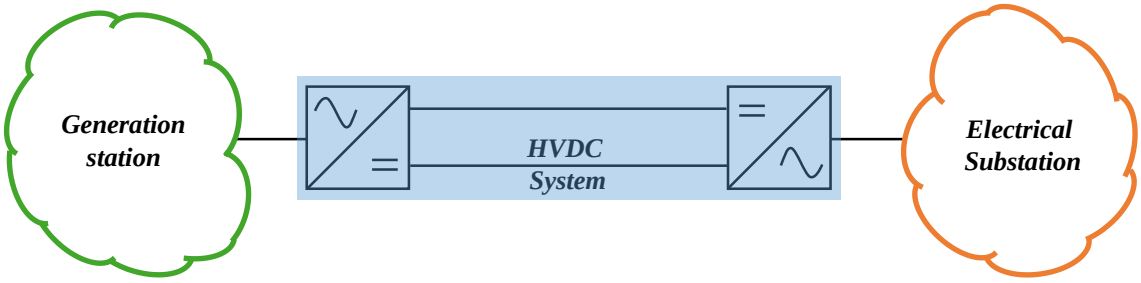

Figure I-1: HVDC system concept.

The vast majority of HVDC transmission system consists of three basic parts:

1) Converter station in rectifier mode to convert the power for AC to DC form.
2) Transmission line, it can be achieved using overhead lines or cables.
3) Converter station in inverter mode to convert the power for DC to AC form.

The power direction can be inversed using the associated control of converter stations. When the two converters are located in the same stations, the HVDC link is often called “Back-to-Back” configuration, see Figure I-2.

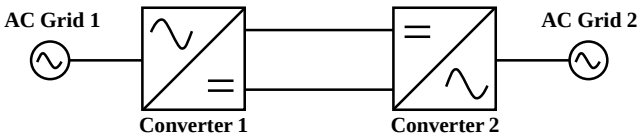

Figure I-2: Back-to-back scheme.

It is the simplest possible configuration and allows to connect two independent neighboring systems with different and incompatible electrical parameters (voltage, frequency, short-circuit power level). It can be also used to stabilize weak AC links in some cases.

3.2. Configurations

Depending on the nature of projects and stations location, a number of different HVDC configurations can be employed [5, 6]. Independently from the converter technology (see section 4), a short description of these configurations is presented below with their associated advantages and drawbacks. In the following, a point-to-point scheme is used to illustrate their schematic diagram but all of which can be extended to a Multi-Terminal DC (MTDC) grid.

3.2.1. Asymmetric monopolar scheme

The scheme of asymmetric monopolar is illustrated in Figure I-3, it includes two converter stations, single pole line (cable/line), and two grounded electrodes (one for each station). This configuration is the simplest and the advantageous one from a cost perspective. Another advantage is the possibility of expansion to a bipolar if necessary (to increase power rating). However, in many cases, the fact that the current return flows through the ground requires permission and can raise environmental concerns.

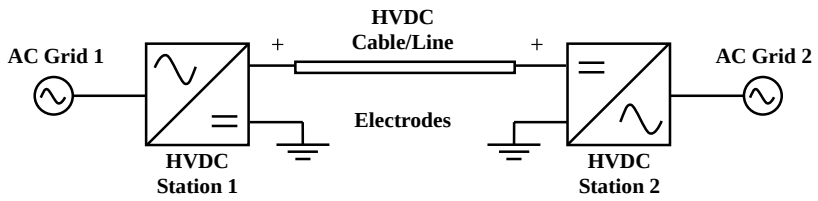

Figure I-3: Asymmetric monopolar scheme without metallic return.

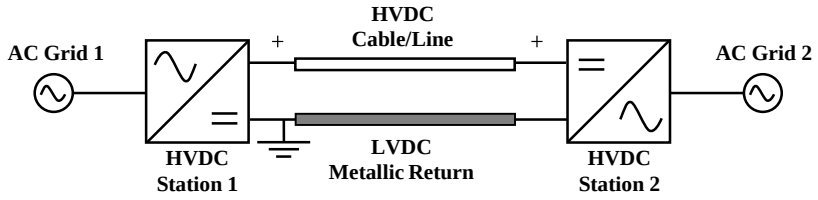

Figure I-4: Asymmetric monopolar scheme with metallic return.

To overcome this issue, another scheme is proposed which includes in addition to the previous scheme a small metallic return (see Figure I-4). The latter, which does not require high-voltage

insulation, is used to return the current and consequently no ground current is obtained. Many of HVDC transmissions with submarine connections use such configuration system.

3.2.2. Symmetric monopolar scheme

A symmetric monopolar configuration is shown in Figure I-5. It can be considered as an alternative monopole scheme that avoid a continuous ground current. The earth reference can be provided by a high impedance reactor on the AC side and in some cases by capacitor's mid-point for the DC grid. Due to its symmetry, this is the only topology where the AC transformer is not subjected to DC voltage stresses, which simplifies its design. However, it has higher cost since it requires two fully insulated conductors. In addition, it extension to bipolar scheme requires lot of modifications.

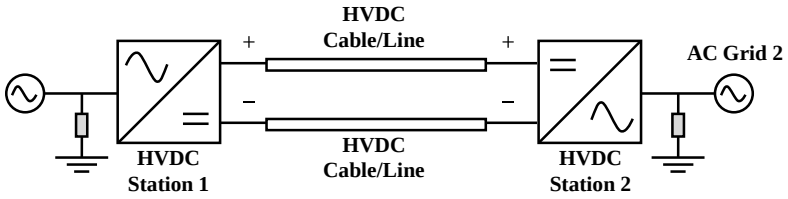

Figure I-5: Symmetric monopolar scheme.

A major drawback concerns all monopolar HVDC configurations is the lack of power in case of DC faults. Since there are no redundancy stations, the transferred power can be missed for a given period which vary depending to the used DC protection strategy.

3.2.3. Bipolar scheme

The bipolar configuration, shown in Figure I-6, can be seen as two monopolar configurations connected in parallel. Compared to the monopolar scheme, this configuration has higher cost since at least two stations at each terminal are needed and a transformer with two secondary windings or two different transformers groups (Yg-Δ and Yg-Y) are necessary to connect the two stations to AC grid [7].

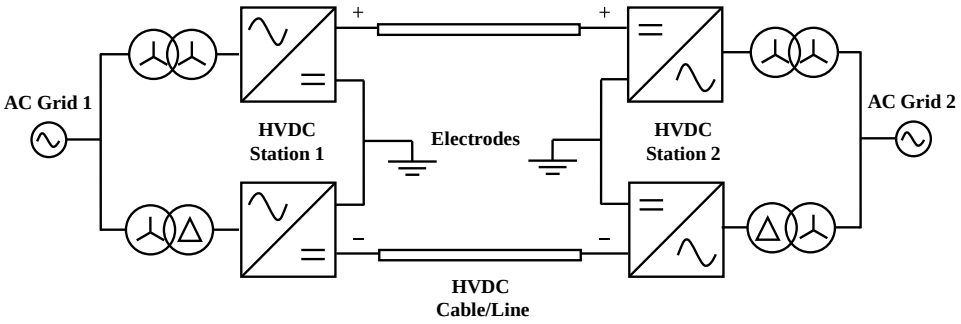

Figure I-6: Bipolar scheme without metallic return.

The main advantage of the bipolar configuration is its redundancy; one pole can be overloaded (if the dimensioning allows it) to compensate the lack of power when the other one is out of service for whatever reason (e.g. maintenance periods). In balanced operation, small/no current flows in the ground event without metallic return scheme. When the latter is employed (see Figure I-7), the bipolar scheme ensures that no current is flowing through the ground whatever the operation conditions are.

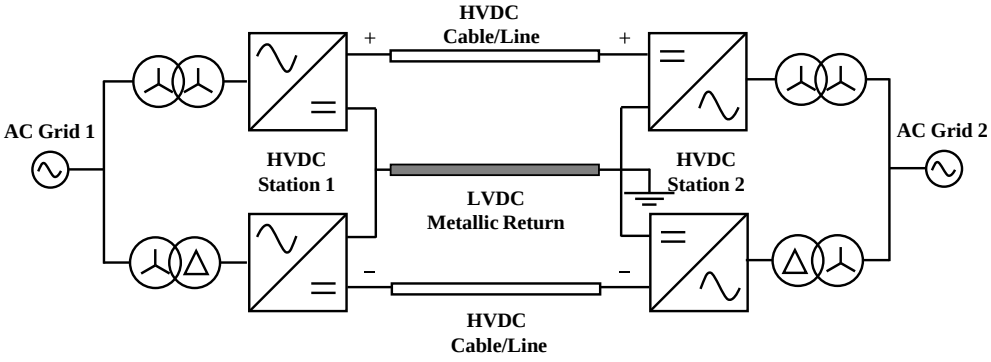

Figure I-7: Bipolar scheme with metallic return.

4. Converter technologies for HVDC application

After presenting the different schemes of HVDC transmission, it is necessary to review the converter topologies that have been or can be used for such application. There are basically two configuration types of power converters which are: Line-Commuted Converter (LCC) known also as Current Source Converters (CSC) and Self-Commuted Converter (SCC) known also as Voltage Source Converters (VSC). The principles of both technologies with their advantages and drawbacks are presented below.

4.1. Line-Commuted Converters (Current Source Converters)

Although the first development of power electronics for HVDC technologies back in 1930's, its first commercial application did not occur until 1954 [8]. Based on mercury-arc valves, a Current Source Converters (CSC) have been employed to build the world's first commercial HVDC transmission: "The Gotland HVDC link". Through submarine cable over 98 km, the latter relates Gotland island to Sweden with a power rating of 20 MW and a voltage rating of 100 kV [9]. With the appearance of the thyristor semiconductor in 1950, new HVDC systems using only solid-state devices have been proposed. The first complete HVDC scheme based on thyristor valves was the Eel River scheme in Canada in 1972. This technology is known as Line-Commutated Converters (LCC) since the AC grid voltage to which the converter is connected drives its commutation process and the presence of the large inductor on the DC side keeps the DC current constant with a small ripple. Thanks to its advantages regarding power rating, reliability, and size, CSC technology based on thyristor valves has dominated the HVDC industry. It has now become standard equipment for DC converter stations and considered as mature technology for HVDC systems [10].

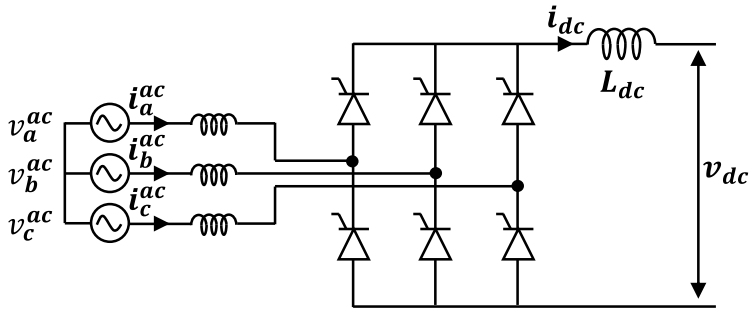

Figure I-8: Three phase Line-Commuted Converter (LCC).

The schematic diagram of basic LCC topology, known as the Graetz Bridge, is illustrated in Figure I-8. Because of thyristor commutation process, only turn-on capability, the commutation process of LCC generates voltage harmonics on the DC grid and current harmonics on the AC grid as it is shown in Figure I-9 .

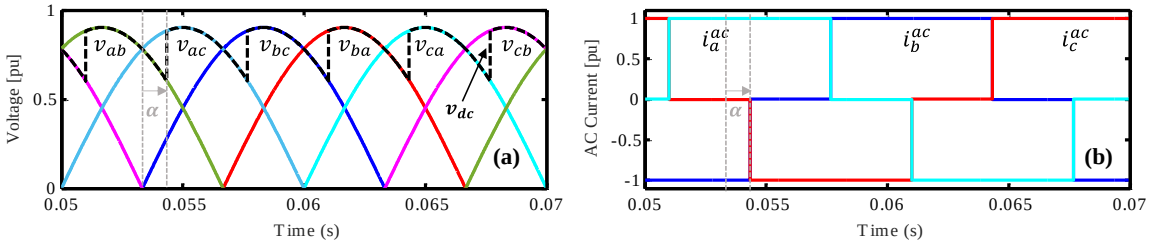

Figure I-9: (a) DC voltage waveform, (b) AC current waveform with LCC.

The LCC converter can be used for transmitting power in rectifier or inverter modes. This is possible by applying a firing angle α on the valves less or greater than 90 degrees respectively. Since the firing angle cannot be negative, the AC current is always delayed from the AC voltage. For this reason, the LCC is always consuming reactive power either in rectifier mode or in inverter one.

For HVDC application, each valve consists of multiple thyristors connected in series in order to support the high DC voltage rating and/or in parallel to support the high DC current (to increase the power for a given DC voltage). Most of HVDC projects employ two thyristor bridges, known as Twelve-Pulse Bridge, connected in series in order to reduce the harmonics in DC voltage as well as in AC currents. For this purpose, the secondary winding of AC transformers are different to create a displacement between the two connected AC grids (see Figure I-10).

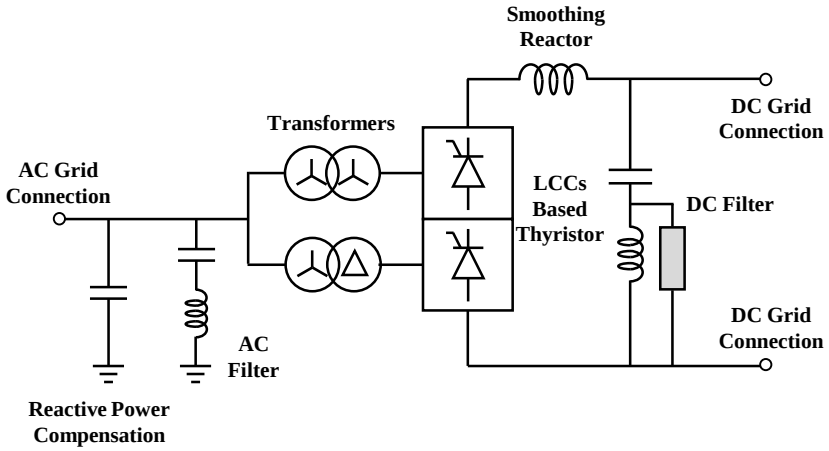

Figure I-10: LCC-HVDC station.

A typical LCC-HVDC station is presented in Figure I-10. In addition to LCC converter, its main component parts are [11]:

- DC Filter: The LCC topology requires harmonic filtering on the DC system. This is especially the case for overhead line applications.
- DC Smoothing reactor: The LCC topology requires a stiff current on the DC system.
- AC Transformers: Since the secondary windings see a standing DC offset, these transformers are manufactured specifically for HVDC applications.
- AC Filter: The LCC topology requires harmonic filtering on the AC system since low frequency harmonics are generated during commutation process.
- AC Reactive support: The LCC topology requires significant reactive power compensation.

An improved topology of the LCC system to overcome part of the above mentioned problems is the capacitor-commutated converter (CCC), where AC capacitors are inserted in series between the valves and converter transformers (see Figure I-11). It has been introduced for HVDC application in 1990 and was commercialized in 1999 [12].

The series connected capacitors not only supply the reactive power consumed by the thyristors, they also improve the dynamic performance of the HVDC system. However, the major drawback of the CCC concept is that the series capacitors increase the insulation costs of the valves. Moreover, since all the power passes through the employed capacitors, the latter have to be oversized which increase relatively the converter cost. Thus, the CCC has been so far only applied to back-to-back links, where the voltage level of the valves is much lower [10, 13].

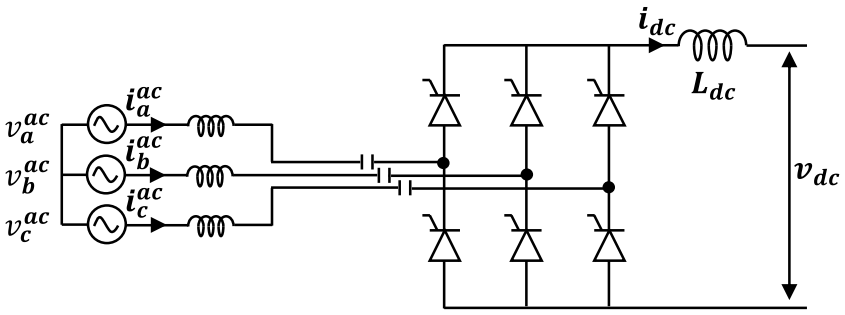

Figure I-11: Three phase Capacitor-Commutated Converter (CCC)

4.2. Self-Commuted Converters (Voltage Source Converters)

The continuous development of power switches leads to the emergence of self-commutated high-power switches such as Gate Turn-off Thyristors (GTOs), Insulated-Gate Bipolar Transistors (IGBTs), Integrated Gate-Commutated Thyristors (ICGTs)... Thanks to their turn-on/ turn-off capabilities, a new converters topology known as Self-Commuted Voltage Source Converter (SCC or VSC) has been employed for HVDC application [14]. Its first application was in 1997 for Hellsjön–Grängesberg project in Sweden. Contrary to the CSC technology, the VSC has a capacitor in DC side which behaves as a constant voltage. Moreover, this topology is self-commuted and doesn't based the commutation process on the AC grid voltage. It can take place by self-controlling ON/OFF actions of the switches.

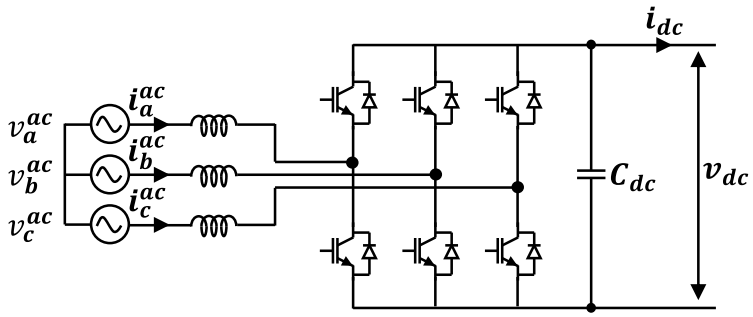

Figure I-12: Three-phase 2-level Voltage Source Converter (VSC).

The basic configuration of a three-phase two level VSC is presented in Figure I-12**.** It consists of six valves, each valve consists of a switching device (IGBT) and an anti-parallel free-wheeling diode. Thanks to turn-on/ turn-off capabilities of IGBTs, the AC voltage generated by a 2-level VSC is a square wave corresponding to the electrical positive and negative DC voltage ($+v_{dc}$ and $-v_{dc}$).

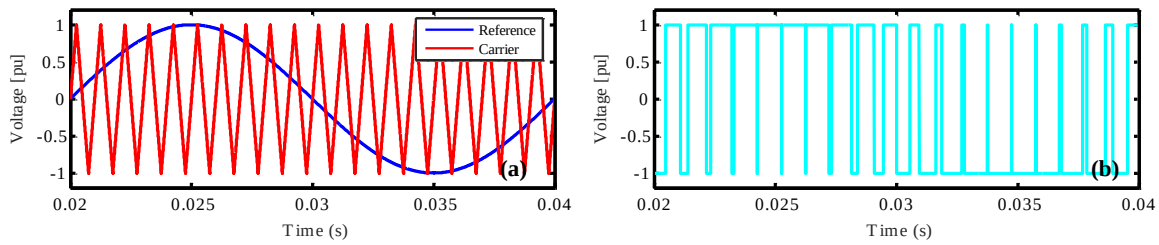

Figure I-13: (a) Requested AC voltage, (b) generated AC voltage with VSC.

With a predefined switching strategy such as Pulse-Width Modulation (PWM), it is possible to generate a sinewave AC voltage as it is shown in Figure I-13. To achieve a good voltage quality

without increasing the commutation losses, the VSC valves are typically switched at around 1-2 kHz [15].

The VSC topology can control the active power by controlling the shift angle between the generated AC voltage and AC grid voltage in the Point of Common Coupling (PCC). Moreover, it offers the possibility of providing or absorbing reactive power by controlling the amplitude of generated AC voltage compared to the AC grid one independently of the transmitted active power.

For high voltage applications such as HVDC, due to the voltage limits of IGBTs, series connection of several hundred is necessary. These latter have to be switched simultaneously that require specialized types of IGBT with sophisticated gate drive circuits in order to share properly the voltages across all the connected components.

To overcome the stress related to switch simultaneously IGBTs and high order harmonics filtering, technologies of VSC have been evolving. Different multilevel topologies were proposed such as 3-level VSC, also known as neutral-point diode-clamped (NPC) [16], Flying capacitor (FC) [17], Cascaded Multilevel Converter [18]… With such topologies, the switching frequency of individual semiconductors and harmonics can be reduced; however, their application for HVDC transmission is complicate due to the complexity in topology structure and control. Moreover, the failure of some devices can hinder the operation of the entire converter system.

In addition to VSC converter, the main components constitute VSC-HVDC station (see Figure I-14) are:

- DC Capacitors: The VSC topology requires a stiff voltage on the DC system.
- AC Reactor: The VSC topology requires AC reactor in order to limit the rate of rise of current seen by the IGBTs, to act as a low pass filter and to allow the control of the input currents.
- AC Transformer: Any transformer configuration can be used to set the secondary voltage rating. Standard transformers can be used with VSC which is not the case with LCC.

- AC Filter: The VSC topology generates high order harmonics which need to be filtered using a high pass filter [14].

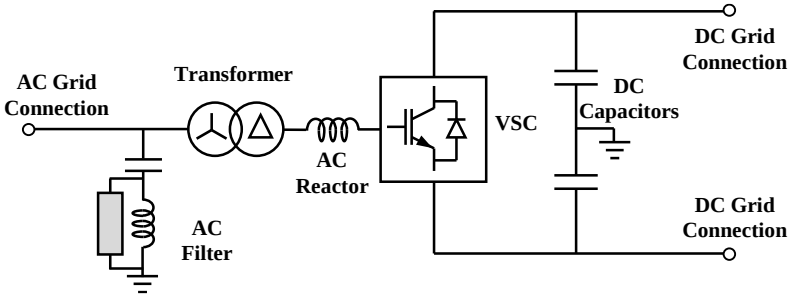

Figure I-14: VSC-HVDC station

4.3. Comparison between VSC and LCC

4.3.1. Advantages of LCC compared to VSC

- The typical losses using LCC is around 0.7%. Because of high switching frequency, the losses using VSC is relatively high (around 1.7%).
- High power and good overload capabilities for LCC compared to VSC.
- The LCC technology is cheaper than the VSC one.
- Low elements (higher reliability) employed with LCC compared to VSC [19].

4.3.2. Advantages of VSC compared to LCC

- The VSC can inject or absorb reactive power irrespective of the active power direction. On the other hand, depending on the firing angles, the reactive power consumption of an LCC is approximately 50 to 60% of the active power.
- LCC topology requires a stiff AC side voltage to avoid commutation failures (especially on the inverter side). The self-commuting capability of VSC allows to overcome this problem.
- Harmonics filtering is required on the AC and DC system with LCC. This requirement is reduced using VSC leading to reduce the size of filter elements.
- The LCC is limited on minimum power transfer, it is about 10% of the rated power transfer. Using an appropriated control, the VSC can operate with zero AC current (zero power).

- The reverse of power using LCC is based on changing the DC voltage polarity. For this purpose, specific cables such as Mass Impregnated (MI) or Oil-Filled (OF) cables are employed. Thanks to bidirectional switches used with VSC, the reverse of power is based on changing current direction while the DC voltage has the same polarity. This allows to use XLPE cables which present several advantages regarding operating temperature, higher mechanical strength and lower environmental risk [20].
- VSC is a suitable technology for mashed Multi-Terminal DC grid (MTDC).
- The LCC creates some voltage/power stability problems when connected to a weak AC system (low short circuit capacity). No restriction regarding short circuit capacity using VSC.
- The VSC station is more compact than the LCC one (40-50 % smaller).
- LCC requires a specific AC transformer (continuous DC Voltage stress). Conventional transformers are sufficient for symmetrical monopole scheme with VSC.
- Black star process can be achieved easily with VSC, it requires additional equipment with LCC [21].
- It is possible to eliminate the converter transformers in VSC-HVDC systems.

Although all the advantages cited before, HVDC markets are still dominated by the LCC since it is a mature technology. However, it is expected that the VSC technology will take place in the future since there are lot of researches involving this technology from academic researchers as well as industrial ones.

5. Modular Multilevel Converter (MMC)

In order to make the VSC technology more efficient and economic, it is necessary to establish new VSC topologies which should avoid connecting several switches in series, operate with a low switching frequency, and enable scaling to different power and voltage levels. In 2003, a revolutionary Multilevel VSC topology was proposed by Professor Marquart [22, 23]. This topology is called Modular multilevel converter (MMC) also known as MMC, M2C or M2LC in the literature publications. It consists of connecting several 2-level converters in cascade to generate an AC voltage output. Its first commercial application for HVDC was in the Trans Bay Cable project in 2010 [24]. Recently, there are several MMC projects being planning or in

development over the world: INELFE (France-Spain, 2015), south west-link (Sweden-Norway, 2014) and several projects in china…

Conceptually, the MMC has the same advantages of standard VSCs and does not have the drawbacks of the multilevel ones. Compared to them, the MMC offers the following advantages:

- Modularity and the scalability to different power and voltage levels.
- Simple capacitor voltage balancing which constitutes the main issue with other multilevel converters.
- Thanks to low switching frequency operation, the converter losses are reduced (around 1%).
- Ability to deliver a very high voltage with excellent harmonic performance. Thus, filtering requirements are reduced.
- High voltage insulation coordination between the capacitors.
- Robustness for component failures (high reliability), failure of one SM will not affect the functioning of MMC.
- Well management of external degraded modes.

Based on those advantages, lot of researches have proved that the MMC is a promising candidate for HVDC application and all the future projects will be based on such topology. This section intends to give a review of the actual state of the art of MMC technology.

5.1. Topology and principle

The general topology of a typical three-phase MMC is illustrated in Figure I-15. It consists of 3 legs, one leg per phase, each leg can be divided into an upper part and lower one called “arms”. These letter are connected in series between the DC poles while the AC output is placed at the middle of them. Each arm includes multiple cells called Sub-Modules (SMs) connected in series. The number of SM is determined according to the voltage rating of DC grid and

employed switches; e.g. 300~400 SMs per arm are required for 640 kV DC voltage rating with 3.3 kV switches voltage rating.

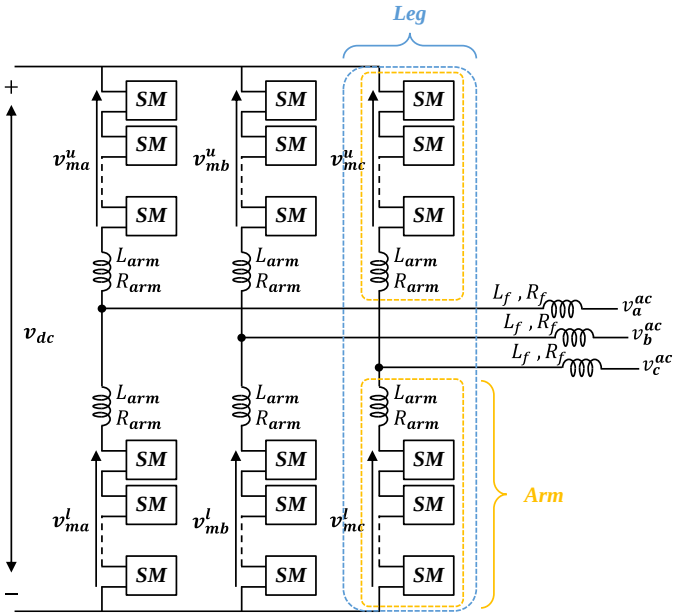

Figure I-15: Three-phase Modular Multilevel Converter (MMC).

In addition to SMs, the MMC arm includes a reactor that have two main functions:

- Limitation of arm current harmonics.
- Limitation of DC fault currents.

The size of arm inductance is based on those two functions. Generally, people use the second function since a small inductance value can satisfy the first one [25].

Generally, an individual SM is formed by capacitors and switches (IGBTs with their corresponding free-wheel diodes) connected with different configuration to obtain several topologies (see section 5.2). For a given SM configuration, the SM can insert or not capacitors between its two terminal branches. Hence, with a predefine control sequence, a modulated voltage can be created with the arm by connecting or not SMs sequentially [26]. The inserted voltage has to meet the criterion that the sum of upper and lower one has to be equal to the DC voltage on one hand and the difference of them has to generate an AC waveform voltage on the other hand. Consequently, if the value of the modulated upper arm voltage is increased, the modulated lower arm voltage should be decreased respectively and vice versa. Figure I-16 explains the previous principle for a 5-levels MMC.

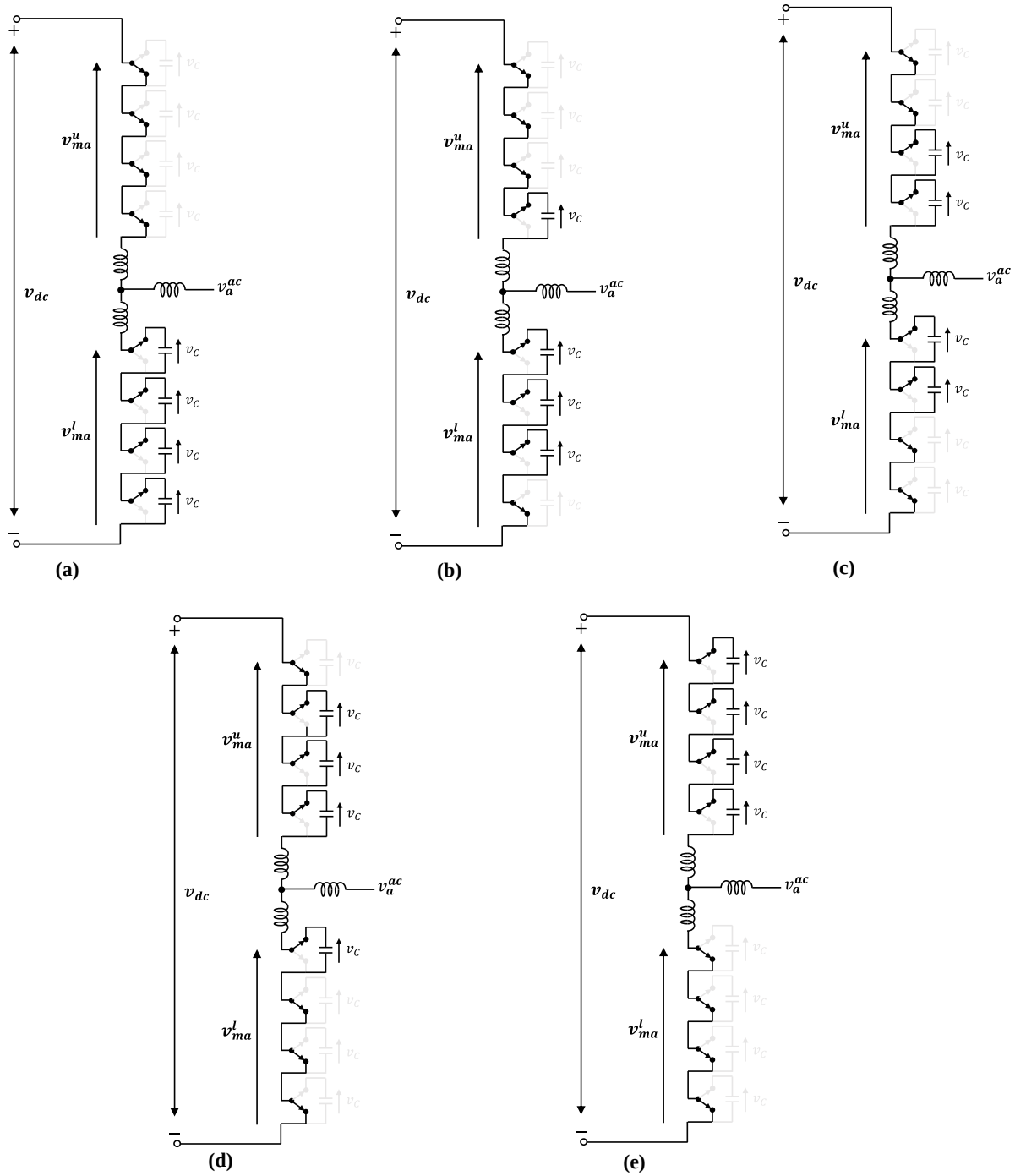

Figure I-16: Operation principle of 5-level MMC.

5.2. SM Topologies

The MMC has been firstly proposed based on a 2-level SM, known as Half-Bridge SM (see Figure I-17), it includes two IGBTs with their corresponding free-wheel diodes and one capacitor C. According to the state of S1 and S2, the SM can takes three different states (see Figure I-17).

- On-state SM: this state is achieved when S1 is turned on and S2 is turned off. The SM capacitor is connected to the arm circuit and the voltage across the SM branches is equal to capacitor one. Depending on current direction, the capacitor is charged through the diode D1 or discharged through S1.

- Off-state SM: this state is achieved when S1 is turned off and S2 is turned on. In this case, the SM capacitor is bypassed and the voltage across the SM branches is set to zero. The current flows through either S2 or D2 while the capacitor voltage remains constant.

- Blocked state: this state is a special one that can hold during some situations, faults for example. It is achieved by setting S1 and S2 to a turn off state. The SM capacitor may charge through D1 when the arm current flows from DC to AC grid, otherwise, it will be bypassed with D2.

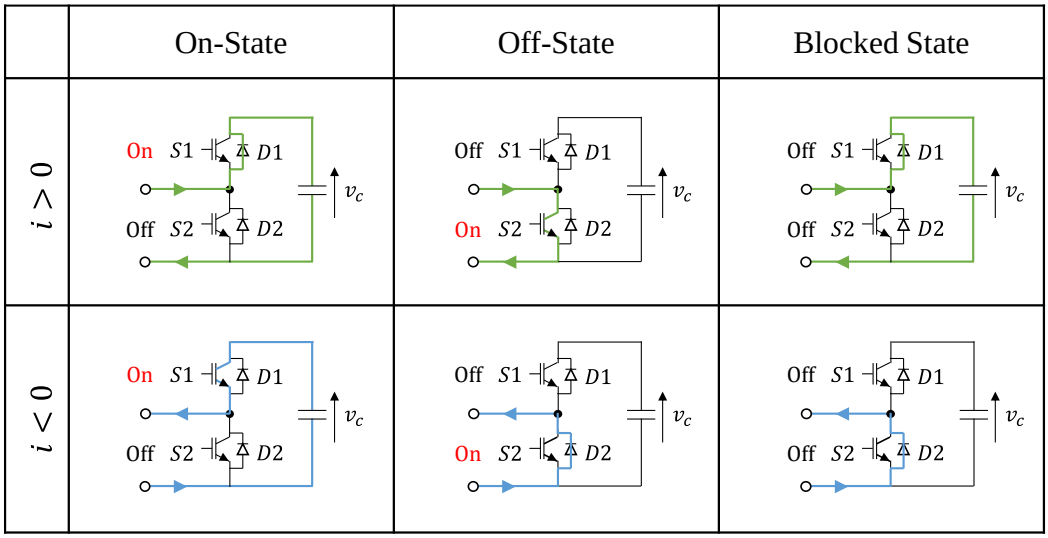

Figure I-17: Different states for Half-Bridge SM.

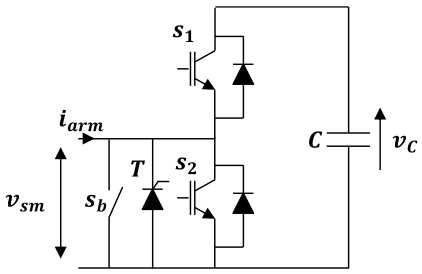

Figure I-18: Half-Bridge SM including protecting Thyristor and mechanical switch.

In practice, for reliability matter, a mechanical switch is need to bypass the SM in case of internal fault. Moreover, in order to protect the diodes against the high current in case of faults, a thyristor is placed in parallel of the SM (see Figure I-18).

In the literature, several SM topologies have been proposed to build the MMC cells. The main ones are: Full-Bridge SM (FBSM), Double-Clamped SM (DCSM) [27] and Cross-Connected Half-Bridge [28] (see Figure I-19). In addition to the configurations obtained with Half-Bridge, these topologies can generate a negative voltage (bipolar SMs) which can give operational advantages; DC fault current capability for example. On the other hand, they carry the disadvantage that they require more IGBTs, the cost of the converter as well as the power losses increase. Therefore, only the half-bridge topology is considered in the rest of the thesis.

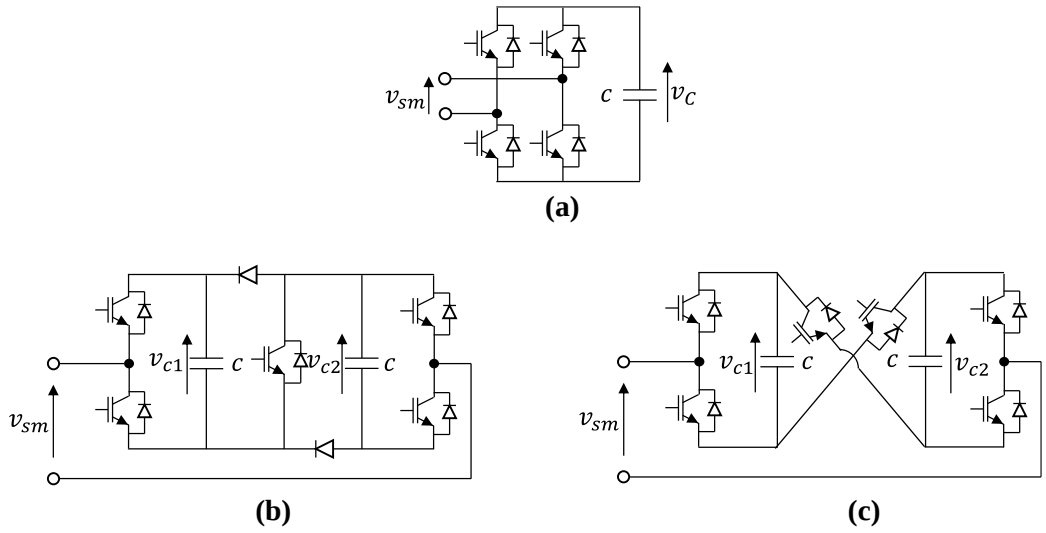

Figure I-19: Comparison of features of various SM topologies: (a) Full-Bridge, (b) Clamp-Double, (c) Cross-Connected.

Table I-1: Comparison of features of various SM topologies.

SM topology	***Output voltage level***	***DC fault blocking capability***	***Losses***
Half-Bridge	$0, v_c$	No	Low
Full-Bridge	$-v_c, 0, v_c$	Yes	High
Clamp-Double	$-v_c, 0, v_c, 2v_c$	Yes	Medium
Cross-Connected	$-2v_c, -v_c, 0, v_c, 2v_c$	Yes	Medium

5.3. MMC Topologies

Recent research has highlighted a number of interesting converter topologies [29]. Hybrid MMC topology proposed by Hitachi [30] represents a promising solution for future HVDC projects. It consists of using Half-Bridge and Full-Bridge SMs to form the MMC arm. It carries the advantage that it is more efficient and less costly than FB MMC and brings the DC current fault capability which is the main drawback of HB MMC. It offers also the possibility to operate the symmetric monopole as an asymmetric one during riding through point to ground DC fault [31].

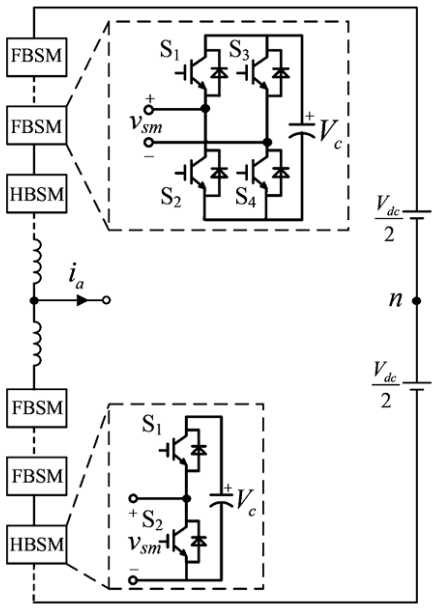

Figure I-20: Hybrid modular multilevel converter (FB+HB) SMs [30].

GE Grid Solution "Alstom Grid" has proposed a series of new converters which combine the advantages of both MMC and 2-level converters. The first proposed version consists of adding to a 2-level VSC a stack of Full-Bridge SMs in the AC line (see Figure I-21) in order to improve the quality of the generated AC voltage [32].

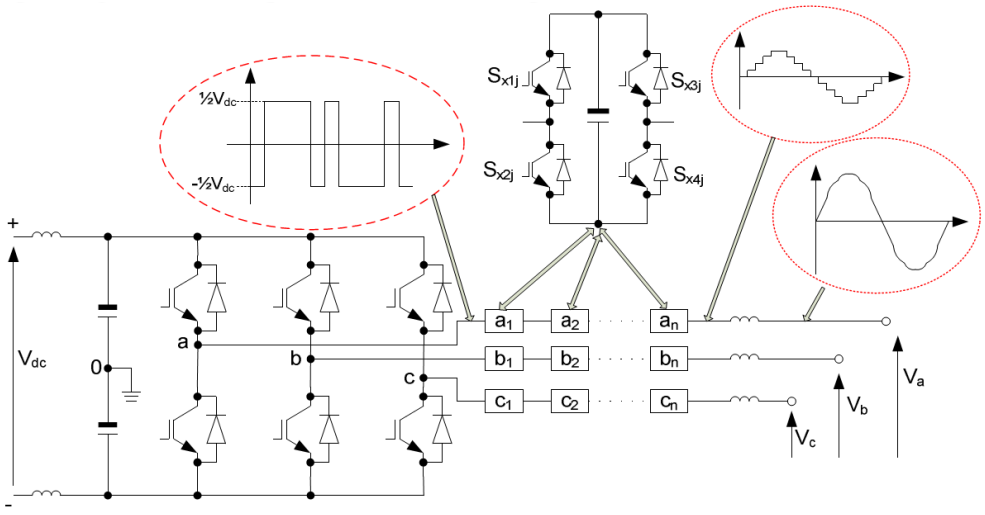

Figure I-21: New hybrid modular multilevel converter (2-level+FB SMs) [32].

The number of components is reduced compared to the standard MMC and the DC fault current can be blocked easily. However, even the commutation process of director switches (constituting 2-level converter) is based on low switching frequency, these letter are hard switched simultaneously which demands equalization of dynamic characteristics of the connected IGBTs. To overcome this problem, GE Grid Solution has propose a second version known as “Alternative Arm Converter” (AAC) [33, 34]. Contrary to the first version, the stack of Full-Bridge is placed in the arms and not in the AC lines. In addition to the previous advantage with the previous version (DC fault blocking capability, excellent AC voltage output), the switching constraint is reduced significantly. On the other hand, this topology requires more elements than the previous one.

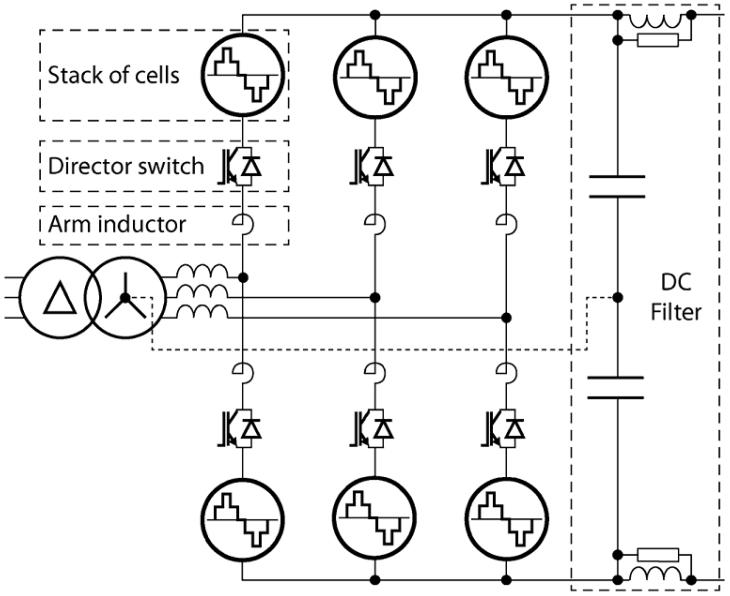

Figure I-22: Alternative Arm Converter (AAC) [34].

In partnership with university of Nottingham, GE Grid Solution has propose a novel MMC topology called "Series Bridge Converter" (SBC) [35, 36] (see Figure I-23). Based on a combination of Half-Bridge and Full-Bridge SMs, the number of required SMs is 30-35% reduced compared to an equivalent MMC.

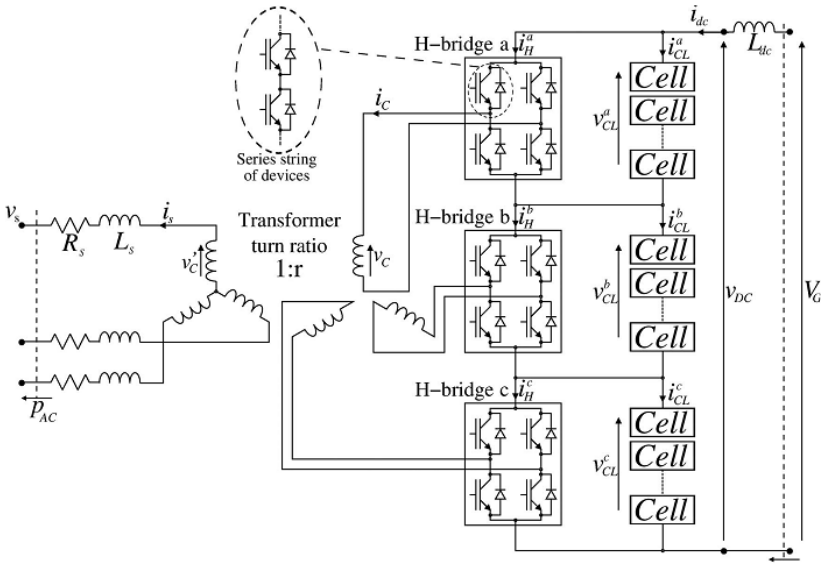

Figure I-23: Series bridge converter (SBC) [35].

All these topologies, despite the advantages they offer, their application in real projects will not be in the next decade. They require lot of researches in terms of control complexity, elements sizing and practical realization.

6. **Conclusion**

This chapter permits to better understand the thesis topic (HVDC system) and its chronological evolution. The advantages of MMC based VSC compared to other proposed solutions have shown that such topology is a promising solution for future HVDC projects. For this purpose, the principle of MMC as well as its SM topologies have been presented and compared. Other MMC topologies such as AAC, SBC and hybrid MMC are new topologies that have shown a great potential however their application for HVDC projects is still early.

Because it is the cheapest topology and most of HVDC projects are based on it, the Half-Bridge topology is considered as the focus of the following work. For this topology, the problematics involving its modeling and control are presented, discussed and improved in the following of this thesis.

CHAPTER II Modular Multilevel Converter Modeling

1. Introduction

Power converters are characterized by a variable structure behavior. The development of new conversion systems leads always to new modeling approaches or methodologies. One of the most important issue related to the MMC is concerning its modeling for different reasons: very huge number of state variables (large mathematical dimension), strong coupling of these variables and large set of dynamics behavior. This chapter is dedicated to the MMC modeling aspects. After a state of the art base on recent bibliography references, thesis contributions in the field of MMC general modeling are explained and developed. To finish, the proposed models are implemented, assessed and validated.

2. Model categories

A model is always a simplified representation of a given real process, system or object. The ideal and perfect model must be accurate, fast, and easy to build and to implement. However, this perfect model is not existing, it is always a compromise between all these requirements. The modeling step is essential to understand, to control, to design and/or optimize, to assess, to observe and to predict the behavior of a system [37, 38].

- **Understanding:** In power system, models can be used to explain and predict the behavior of real equipment or process.

- **Observing, predicting:** For the benefit of power system operation, there is a need to perform various measurements at different nodes of the network with the most possible accurate values. However, it is not possible economically to have measurement devices at any node in the grid. Hence, it is necessary to develop component models using state estimation method to get a good estimated value of the given variables.

- **Sizing/ optimizing:** A model is also required in order to design a component. In the same aim as above, the use of model allows the determination of the constraints applied to the component. Moreover, it allows engineers to reach a given objective by choosing an adapted set of decision variables.

- **Controlling:** The control design needs specific models. Depending on the control law type, these models can be linear or nonlinear; time domain or frequency domain,

continuous or discrete. They can be obtained from the system knowledge or from experiment tests.

According to how the model is interpreted and for which purpose it will be dedicated, the representation of a model may be different from one to another goal. For example, a model which is used for control purposes can be different to the ones used for circuit design or load flow calculation. Consequently, the users must narrow the type of models by identifying the requirements that must be fulfilled. To simplify, only the elements that are thought to play an important role and to reproduce the investigated phenomena must be considered.

When the models are developed for simulation purposes, the following criteria have to be considered [37]:

- The models have to reproduce all the possible system states with a good accuracy in steady state as well as for transient.
- The models have to be with an acceptable level of complexity.
- The models have to fulfill with the user needs: control, offline / real-time simulations and design process.
- The models have to be implemented with a technical manner in a dedicated software.
- The inputs and outputs models have to be defined according to the type of study and explicitly represented inside the models.
- The definition domain of simulation (time or frequency based variables).

Due to the focus on dynamic and transient performances, the study is enlightening more dynamic models rather than static ones. Different dynamic model categories can be obtained for power converters; they are summarized in the following table.

Table II-1: Model categories for power converters.

Model classification criteria	***Model Types***
Regarding the number of state variables	Full order models Reduced order models
Regarding time domain evaluation	Continuous models Sampled (Discrete) models
Regarding period evaluation	Switched models Averaged models
Regarding implementation techniques	Circuit models Mixed models Analytical models
Regarding control law	Linear models Nonlinear models
Regarding definition domain	Time domain models Frequency domain models

- **Full order models:** models where the number of explicit state variables is equal to the real system order.
- **Reduced order models:** models where the number of explicit state variables is less than the real system order.
- **Continuous models:** models that provide information with continuous set of differential equations.
- **Sampled (Discrete) models:** models that provide information about the evaluation of all state variables in a discrete manner.
- **Switched models:** models where the switching events are explicitly represented, i.e. represented by a set of differential equations with a discrete input vector.

- **Averaged models:** models where the state variables and the inputs are represented by their average values.

- **Circuit models:** models where the elements are implemented using their associated physical models available in program libraries.

- **Mixed models:** models where some elements are implemented using their analytical equations and others are implemented using their associated circuit models.

- **Analytical models:** models where all the information are given by analytical equations.

- **Linear models:** models where all the state variable equations can be written with a linear differential equations system.

- **Nonlinear models:** models which contains nonlinear differential equations.

- **Time domain models:** models where all the variables are represented as a function of time.

- **Frequency domain models:** models where all the variables are represented as a function of frequency, (e.g., Laplace transform, *z* transform…).

3. MMC modeling levels (state of the art)

This section describes the different modeling levels for the simulation of MMC which presents the key of future DC grid developments [39]. Since there are many variables and switch elements inside the MMC, different modeling approaches can be used according to the time domain of the study, investigated phenomena and required accuracy.

To facilitate the explanation of different MMC models, it is better to start with the most accurate model which is the closest to the physical system. It is usually named as the full physics model. In this model, the topology of the model is kept exactly the same as the real converter with respect of some basic simplifying hypotheses. Each IGBT is represented by an equivalent circuit based on their differential equations [40] (see Figure II-1). The latter depends on the switch type and its internal configuration when it is manufactured. Since the topology requires lot of SMs, this type of model cannot be used for DC grid simulation involving MMCs.

Generally, this type of modeling is used to simulate and/or design power system packages (Gate Drivers).

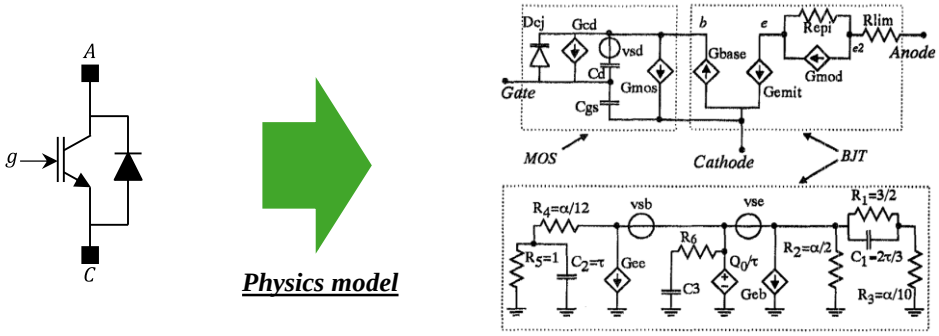

Figure II-1: Physics based model for IGBT [40].

By using simplified switch models, full detailed MMC models can be obtained [41]. Figure II-2-(a) shows a simplified IGBT model including one ideal switch and two non-linear diodes. The nonlinear behavior of the diodes can be tuned based on manufacturer data sheets or experimental measurements. Since the switch model introduces nonlinear elements, the simulation still takes a long time for a short time event.

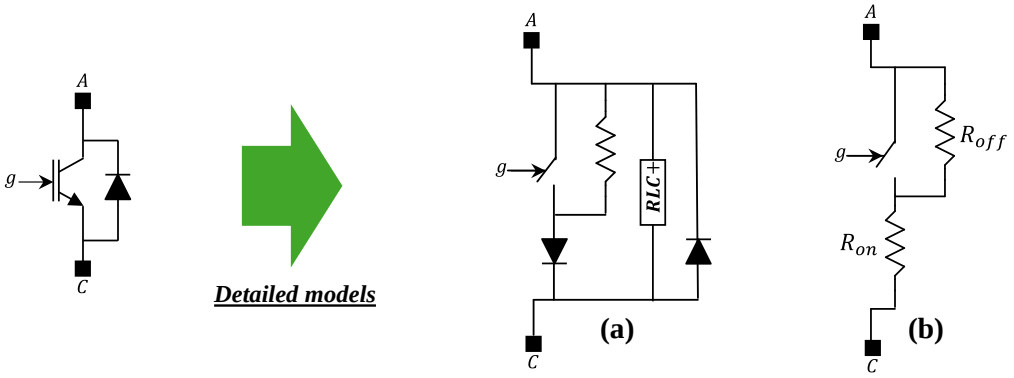

Figure II-2: Detailed based models for IGBT: (a) non-linear diodes model, (b) resistances equivalent model.

In order to accelerate the simulation, the IGBT model needs to be more simplified. For this purpose, the switches can be simulated as resistors with two values: R_{on} for closed state (milliohms) and R_{off} for opened state (megaohms) (see Figure II-2-(b)) [42]. The resistance value depends on the gate signal and arm current direction. Thanks to this simplified model (less elements), the simulation of MMC model is faster than the previous ones.

The advantages of full detailed based models are:

- Since the order of the model is same as the physical system, the model gives a good accuracy where all the phenomena can be seen including some degraded operation of SMs.
- The model can be used as a Benchmark to validate other MMC models.
- A current analysis inside the SMs can be easily performed allowing to have an accurate SMs losses estimation.

The main drawback of using full order model is related to the computational time. In fact, the simulation program creates an admittance matrix where the dimension is equal to the number of nodes in the system. This matrix has to be inverted at each switching operation which makes the simulation too slow.

Nodal analysis is one of various methods used by power system software to solve the electrical system circuit [43]. Based on Dommel's algorithm [44], it consists of transforming the elements constituting the electric circuit to an equivalent model based on resistances and voltage sources or conductances and current sources through the application of trapezoidal integration method. Since the MMC includes high number of nodes, applying such analysis allows decreasing the number of electrical nodes and consequently accelerate the simulation. To do so, each SM can be reduced to an equivalent (Thevenin or Norton) model (see Figure II-3) leading to obtain the full order equivalent model [45, 46]. This model will be presented with more details thereafter in this section.

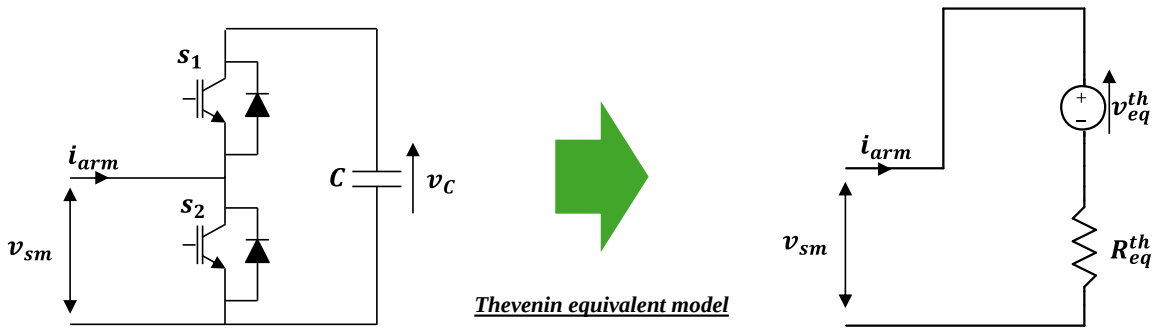

Figure II-3: Equivalent Thevenin model for one SM.

The advantage of this modeling approach is that less electrical nodes are introduced in the model (admittance system is reduced). Consequently, the simulation will be faster compared to

the other full order models. After its validation with full detailed models, it can be used for the validation of low level MMC control as well as for the validation of reduced order models.

To make the simulation of MMC more and more fast, reduced order models have been proposed in [47, 48, 49]. This modeling approach is already developed for standard converters and it has been extended to particular converter structures like MMC. It consists of reducing the number of state variables inside the model by making some hypotheses. For MMC topology, the number of state variables can be reduced by assuming that capacitor voltage of SMs within one arm are perfectly balanced by an external control. The accuracy and validity of this hypothesis increases when the number of SMs per arm is relatively large. Based on this assumption, the arm behavior can be modeled with the so-called reduced order averaged arm model [48, 50]. It is based on modeling the arms with two controlled sources, (current and voltage) coupled as it is shown in Figure II-4. The arm inductance remains the same but the capacitors are reduced to an equivalent one. The sources are controlled by an averaged switching function, known as modulation index, which is provided by an upper control level. This averaged model will be analyzed in details after.

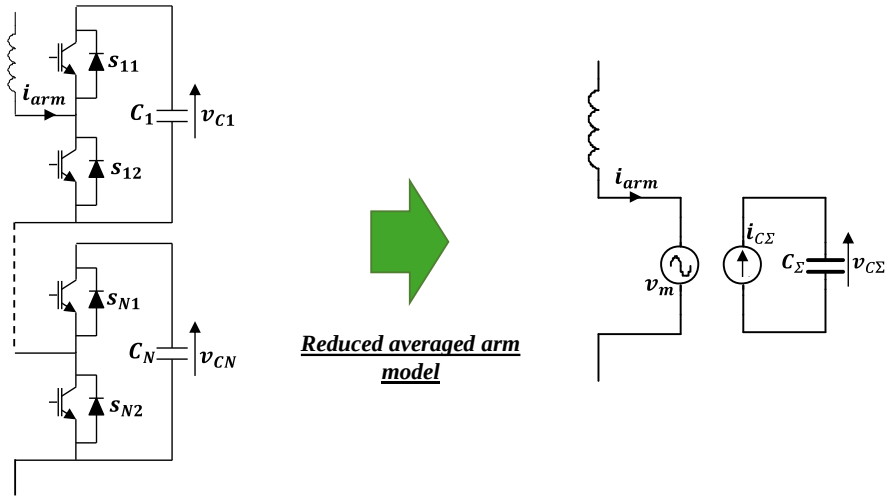

Figure II-4: Reduced averaged arm model.

Based on the hypothesis cited before and assuming that the averaged capacitor voltage of upper and lower arms within on leg are equal, the reduced order averaged leg model can be derived. In this model, the averaged behavior is developed for all the leg (see Figure II-5). This model can be simplified to a unique reduced averaged model by assuming that the averaged capacitor voltages of each leg are equal. More information about these averaged models can be found in [51].

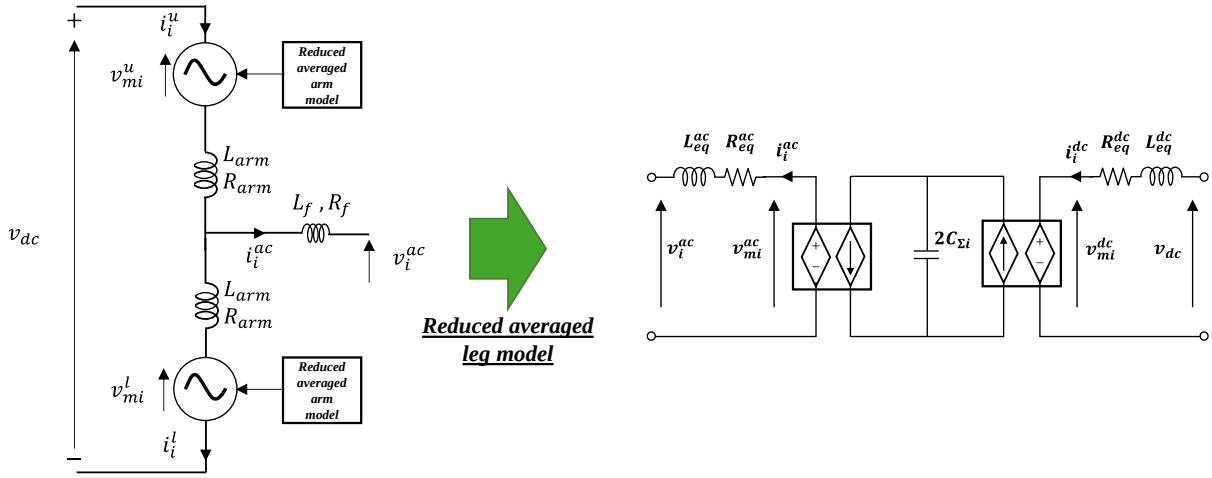

Figure II-5: Reduced averaged leg model.

In general, the reduced order models are suitable to derive control laws for high level control such as current, power and energy loops [52]. They can be used also for grid protection studies such as AC and DC grids fault when the blocking state is considered in the model.

Based on the averaged model proposed in [51], a phasor model (see Figure II-6) has been presented in [53]. This modeling methodology is based on a fundamental frequency approach and it is required for power flow studies when an electro-mechanical simulation tool is used to perform such study [54, 55]. Two hypotheses are taken in this modeling technique [56]:

- All harmonics are neglected.
- All variables are perfectly sinusoidal.

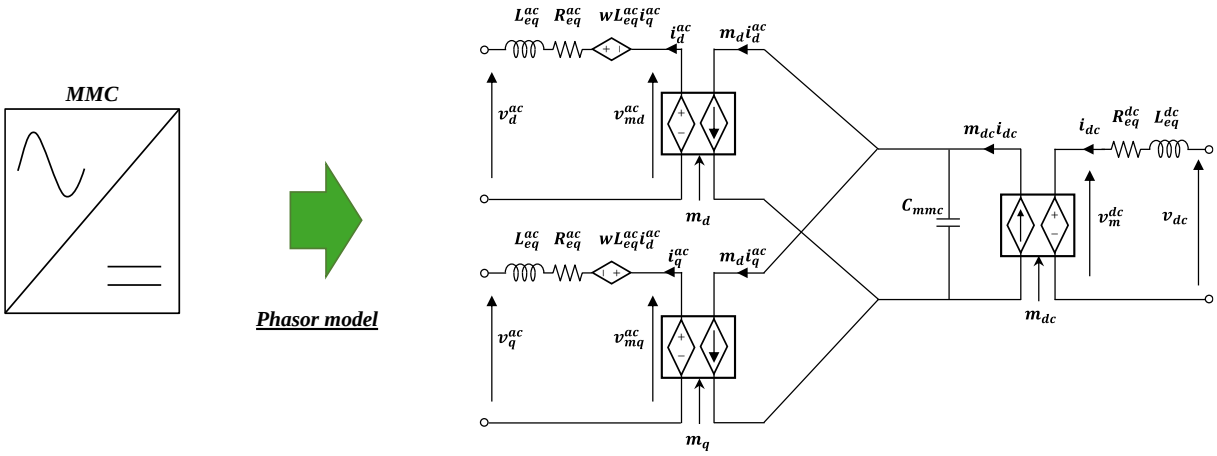

Figure II-6: Phasor MMC model.

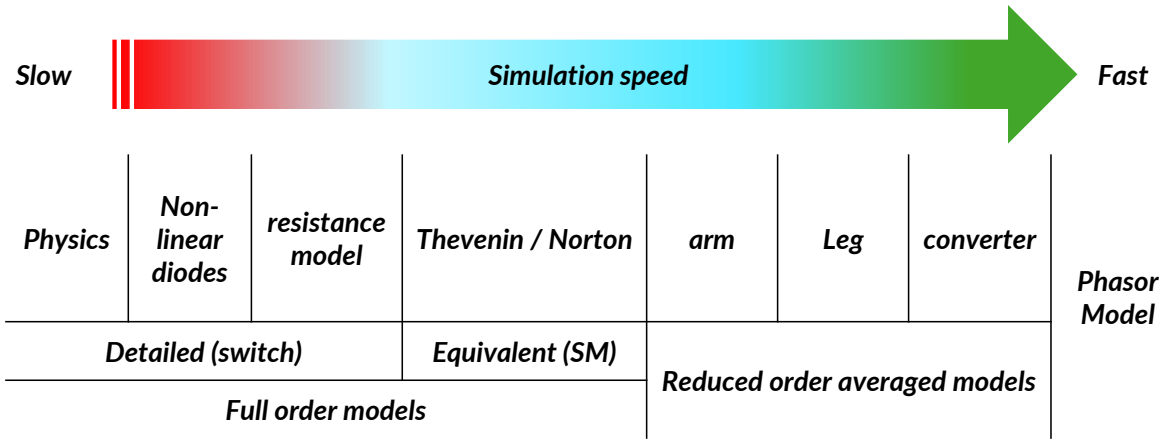

Figure II-7: Summary of different model types for MMC.

After presenting different MMC models proposed in the literature for simulation purposes (see Figure II-7), later, only the most interesting ones for EMT studies will be considered. A detailed analysis including the analytical equations and their implementation technique will be provided below.

The selected models are:

- ***The full order detailed model (DM).***
- ***The full order equivalent model (EM).***
- ***The reduced order averaged arm model (AVM).***

3.1. Full order detailed model (DM)

The full order detailed model is obtained by simplifying the IGBT with a resistor which takes two values: R_{on} for closed state (milliohms) and R_{off} for opened state (megaohms). This model will be considered as a Benchmark for our considered purposes. When the model is implemented in software programs, according to the classification of [37], it can be given as a circuit based model, see Figure II-8-(a). This modeling technique offers a high accuracy since the switches are explicitly represented, however, it introduces a high number of electrical nodes which makes the simulation too slow. Consequently, it is preferred to derive the equations system for this model type by exploiting its topology in order to obtain its analytical based model. As it can be observed in Figure II-8-(b), the analytical based model is more compact and introduces less electrical nodes in the arm compared to its circuit based model.

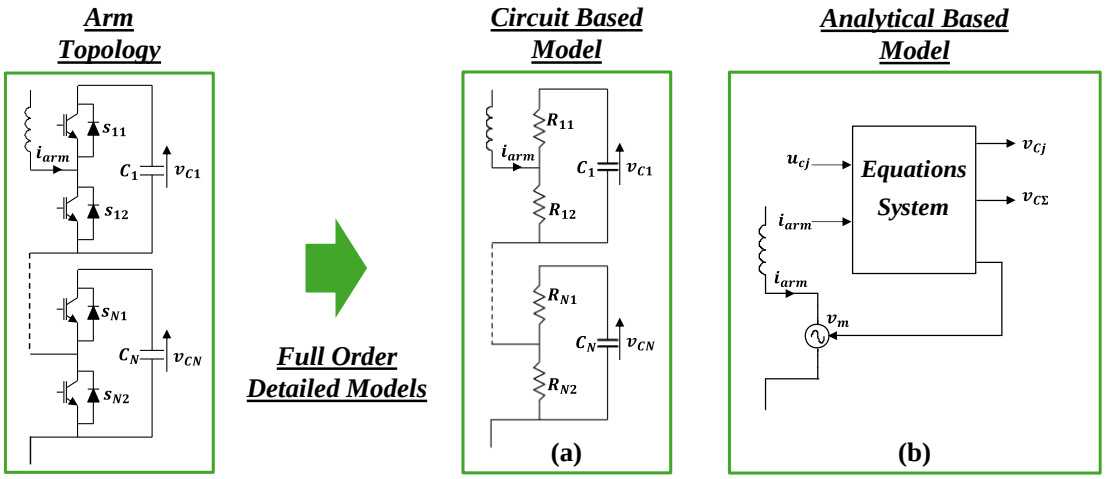

Figure II-8: Full order detailed models: (a) circuit based model, (b) analytical based model.

In order to simplify the process of obtaining the analytical model equations, at the beginning, only one SM is considered.

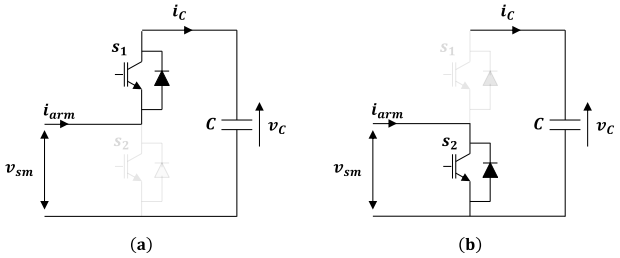

Figure II-9: SM configurations for controlled states.

According to Figure II-9, the SM state variable can be summarized in Table II-2.

Table II-2: State variables for SM in controlled states.

Switches states	***State variables***
Inserted SM $(s_1 = 1, s_2 = 0)$	$v_{sm} \approx v_C$ $i_C = i_{arm}$
Bypassed SM $(s_1 = 0, s_2 = 1)$	$v_{sm} \approx 0$ $v_C = cst$ $i_C = 0$

The equations describing the SM state variables can be derived using one switching function as follow.

$$v_C = \frac{1}{C} \int i_{arm}\, u_C$$
$$v_{sm} = R_{on} i_{arm} + v_C\, u_C \qquad \textit{(II-1)}$$

Where:

u_c: Switching function, 1 when the SM is inserted and 0 when it is bypassed.

C: SM capacitance (F).

i_{arm}: Arm current (A).

v_C: SM capacitor voltage (V).

R_{on}: Equivalent loss resistance (Ohm).

v_{sm}: Inserted SM voltage (V).

When the whole arm is considered, the inserted voltage by the stack can be seen as a modulated voltage. So the arm model can be reduced to a voltage source controlled by an equations system representing the arm equations model as shown in Figure II-8-(b).

For a MMC with $N + 1$ levels, the equations system can be written as follow:

$$for\ j = 1,2, \dots N$$
$$v_{cj} = \frac{1}{C_j} \int i_{arm}\, u_{cj}$$
$$v_{C\Sigma} = \sum_{j=1}^{N} v_{cj} \qquad \textit{(II-2)}$$
$$v_m = N R_{on} i_{arm} + \sum_{j=1}^{N} v_{cj}\, u_{cj}$$

Where:

$v_{C\Sigma}$: Sum of SM capacitor voltages (V).

N: Number of SM per arm.

v_m: Modulated arm voltage (V).

3.2. Full order equivalent model (EM)

As it was introduced previously, it is useful to have an equivalent (Thevenin or Norton) model for MMC since the most EMT programs use a nodal approach based solver. The equivalent model for MMC can be achieved by reducing the number of electrical nodes in the converter representation and keeping the same order as the real structure.

With trapezoidal integration method, each submodule capacitor can be replaced with an equivalent circuit (see Figure II-10). The latter can be a voltage source $v_{Ceq}(t - T_s)$ in series with a resistor R_C when an equivalent resistive circuit is used or a current source $i_{Ceq}(t - T_s)$ in parallel with a conductance G_C when an equivalent conductance circuit is used.

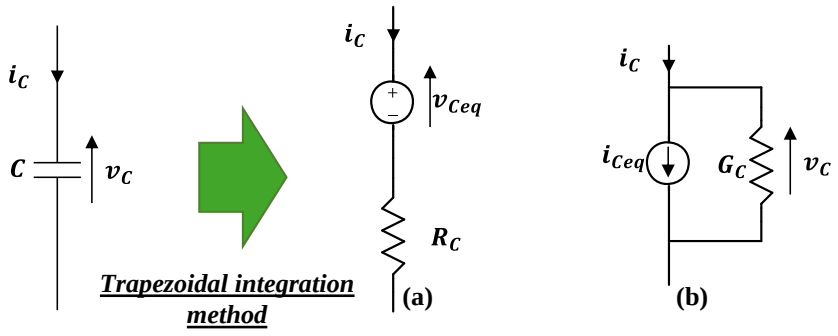

Figure II-10: Capacitor equivalent circuit: (a) resistive, (b) conductance.

Their values are given by the following equations [44]:

$$R_C = \frac{T_s}{2C}$$

$$v_{Ceq}(t) = R_C i_C(t - T_s) + v_{Ceq}(t - T_s) \qquad \text{(II-3)}$$

$$G_C = \frac{2C}{T_s}$$

$$i_{Ceq}(t) = -\left(G_C\, v_C(t - T_s) + i_{Ceq}(t - T_s)\right)$$

Where:

T_s: Simulation time-step (s).

$v_{Ceq}(t - T_s)$: History capacitor voltage (in the previous time-step) (V).

$i_{Ceq}(t - T_s)$: History capacitor current (in the previous time-step) (A).

Since the simulation time-step is relatively small and in order to avoid the division by a small value which can create some numerical problems, it is recommended to use the resistive circuit instead of using the conductance one. Therefore, the SM circuit can be simplified to one voltage source in series with impedance by calculating the equivalent Thevenin circuit as it is illustrated in Figure II-11.

$$R_1 = R_{on}\, u_c + R_{off}\, \overline{u_c}$$

$$R_2 = R_{off}\, u_c + R_{on}\, \overline{u_c}$$

$$R_{eq}^{th} = \frac{R_2\,(R_1 + R_C)}{R_2 + R_1 + R_c} \qquad \textit{(II-4)}$$

$$v_{eq}^{th} = v_{Ceq}\,\frac{R_2}{R_2 + R_1 + R_C}$$

Where:

u_c: Switching function, 1 when the SM is inserted and 0 when it is bypassed.

$\overline{u_c}$: Switching function, 0 when the SM is inserted and 1 when it is bypassed.

R_{eq}^{th}: Equivalent Thevenin resistor (Ohm).

v_{eq}^{th}: Equivalent Thevenin voltage (V).

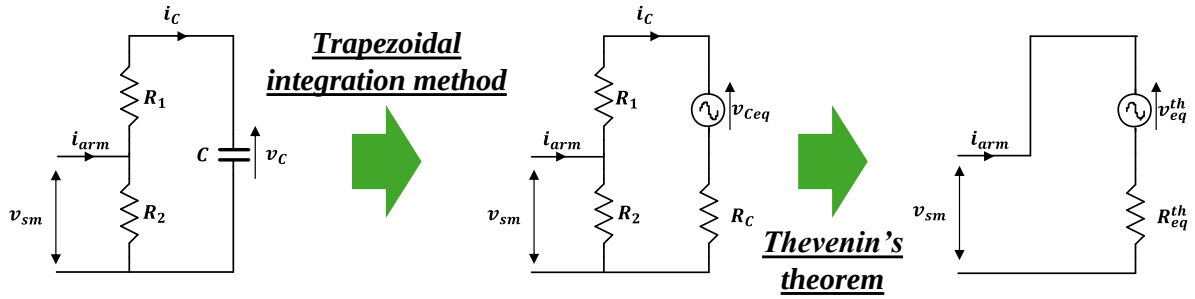

Figure II-11: From detailed to equivalent model.

The inserted SM voltage can be calculated by the following expression:

$$v_{sm} = R_{eq}^{th}\, i_{arm} + v_{eq}^{th} \tag{II-5}$$

When the whole arm is considered, the equations system describing the full order equivalent model can be expressed by equations (II-6):

$$\begin{gathered}
for\ j = 1,2, \dots N \\
R_{j1} = R_{on}\, u_{cj} + R_{off}\, \overline{u_{cj}} \\
R_{j2} = R_{off}\, u_{cj} + R_{on}\, \overline{u_{cj}} \\
i_{Cj} = i_{arm}(t - T_s)\, u_{cj} \\
R_{Cj} = \frac{T_s}{2C_j} \\
v_{Cj} = v_{Ceqj}(t) = R_{Cj}\, i_{Cj} + v_{Ceqj}(t - T_s) \\
v_{C\Sigma} = \sum_{j=1}^{N} v_{Cj} \\
R_{eqj}^{th} = \frac{R_{j2}\left(R_{j1} + R_{Cj}\right)}{R_{j2} + R_{j1} + R_{Cj}} \\
v_{eqj}^{th} = v_{Cj}\frac{R_{j2}}{R_{j2} + R_{j1} + R_{Cj}} \\
v_m = \sum_{j=1}^{N}\left(R_{eqj}^{th}\, i_{arm} + v_{eqj}^{th}\right)
\end{gathered} \tag{II-6}$$

A straightforward way to implement this arm model in EMT programs is to use an analytical based model (see Figure II-12). It can be observed that, by using an analytical based model, the EM and DM are quite equivalent.

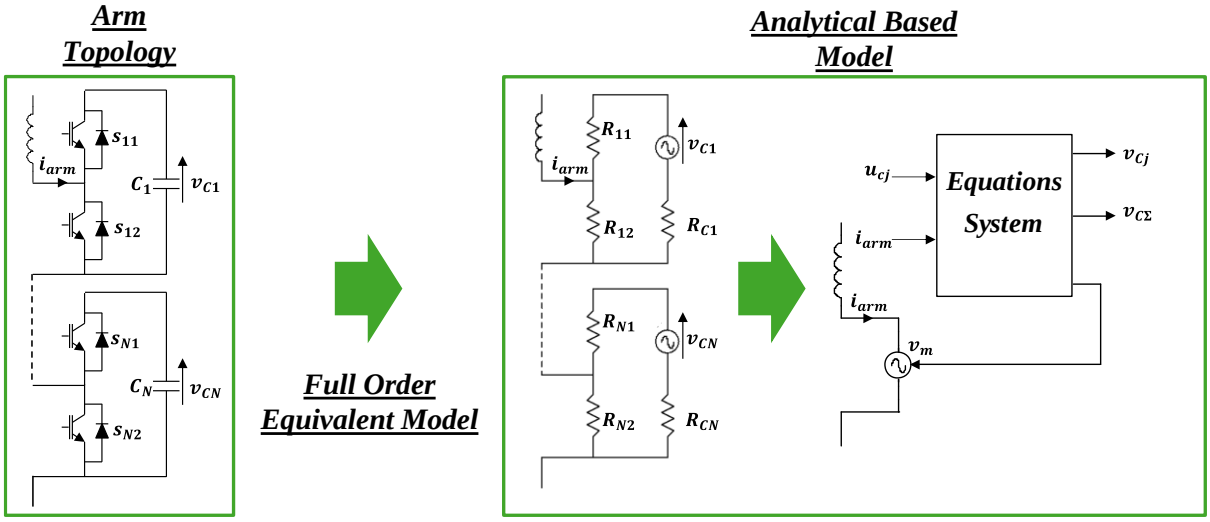

Figure II-12: Full order equivalent model.

3.3. Reduced order averaged arm model (AVM)

The aim of this type of modelling is to obtain the general behavior of MMC arm. In this model, each MMC arm is averaged using an averaged function so-called "modulation index". For this purpose, two assumptions, mentioned previously, are introduced to derive the global arm behavior. They are:

- The SM capacitors are identical for one arm.
- Their voltages are perfectly balanced by an external control.

To derive the arm behavior model, $v_{C\Sigma}$ is defined as the sum of the voltages of all the arm capacitors:

$$v_{C\Sigma} = v_{C1} + v_{C2} + \cdots + v_{CN} \qquad (II\text{-}7)$$

The evolution of $v_{C\Sigma}$ can be derived according to the switching states of SMs.

$$C\frac{dv_{C\Sigma}}{dt} = C\frac{dv_{C1}}{dt} + C\frac{dv_{C2}}{dt} + \cdots + C\frac{dv_{C_N}}{dt}$$

$$C\frac{dv_{C\Sigma}}{dt} = i_{C1} + i_{C2} + \cdots + i_{CN}$$

$$C\frac{dv_{C\Sigma}}{dt} = n\, i_{arm} \qquad \textit{(II-8)}$$

$$\frac{C}{N}\frac{dv_{C\Sigma}}{dt} = i_{arm}\frac{n}{N} = i_{arm}\, m$$

Where:

n: The number of connected SMs.

According to the equations above, the general behavior of the arm can be represented by an ideal DC/DC chopper controlled by the modulation index m.

$$i_{C\Sigma} = m\, i_{arm}$$

$$C_\Sigma = \frac{C}{N}$$

$$v_{C\Sigma} = \frac{1}{C_\Sigma}\int i_{C\Sigma} \qquad \textit{(II-9)}$$

$$v_m = NR_{on}i_{arm} + m\, v_{C\Sigma}$$

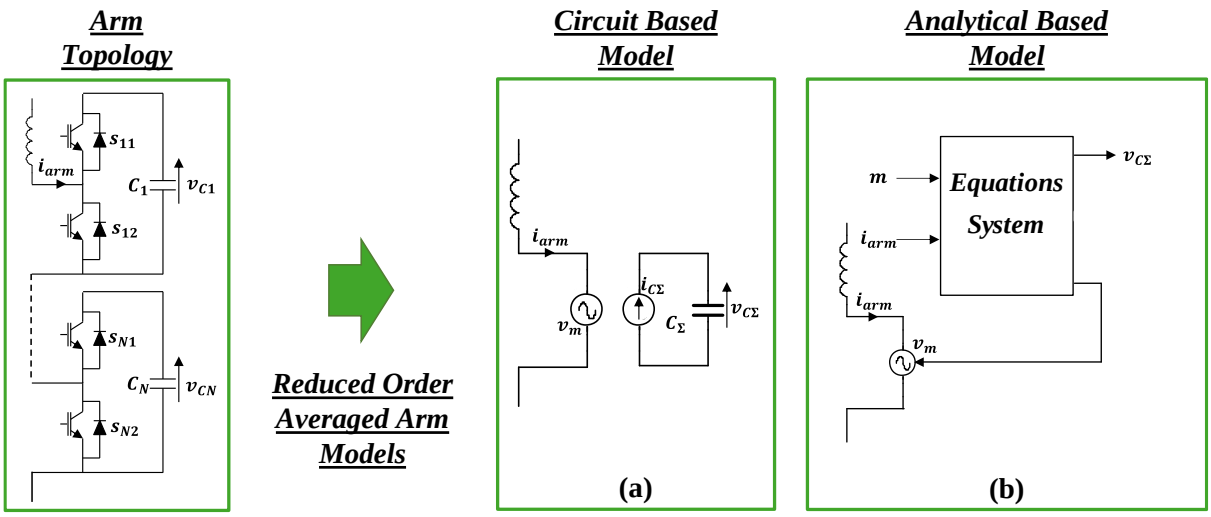

Figure II-13: Reduced order averaged arm models: (a) circuit based model, (b) analytical based model.

Consequently, the averaged model is obtained as duplicated in Figure II-13. Its implementation can be achieved by using a circuit based model (see Figure II-13-(a)) or by using an analytical based model where only one controlled voltage source is used (see Figure II-13-(b)).

3.4. MMC models including blocked state

Regarding the models presented in the previous section, it can be observed that only the controlled states are represented (except for circuit based model of DM). It means that, the presented models can reproduce the same behavior as a real MMC only when the SMs receive firing pulses from control level. However, in reality, the MMC can be requested to operate in other situations such as when internal and external faults occurring. For example, in order to protect the SM capacitors against over voltage, the SMs packaging can block the firing pulses coming from control layer. This state is known as "blocked state" in which the MMC will operate as a Diode-Bridge converter. This operation mode can take place in the following cases:

- **Start-up sequence:** Before starting the converter operation, it is mandatory to charge the SMs to a minimum value that allows starting the control. The industrial solution is based on charging the SMs through the diodes. This charging step is known as "Uncontrolled step" and can be operated with AC or DC grids depending on the grid conditions.

- **DC fault conditions:** DC Fault is one of the degraded modes that can occur at any time specially when there is an overhead line connection. The arm currents reach rapidly high values which can be 10 times higher than their nominal values. The IGBTs protections within the SM packages have to react as soon as possible in order to block their pulse signals. So diodes have to conduct the arm current for a short time before enabling the protection thyristor (see Figure I-18).

Moreover, in practice, the MMC arm contains some redundant SMs. Thanks to these cells, the converter can easily manage the internal degraded modes to remain itself available. When an internal fault occurs, the faulted SMs have to be bypassed with a mechanical switch leading to introduce some transients that have to be investigated and mitigated with converter control.

In order to reproduce easily and efficiently the previous cases by simulation, the MMC models have to take in consideration the normal, the blocked and bypassed states in the MMC modeling. An averaged model has been proposed in [57] including the blocking capability when a DC fault occurs (see Figure II-14). It has been proven that this model provides a good representation during DC faults however it is less accurate when AC faults occur. Moreover, startup sequence cannot be performed using this model.

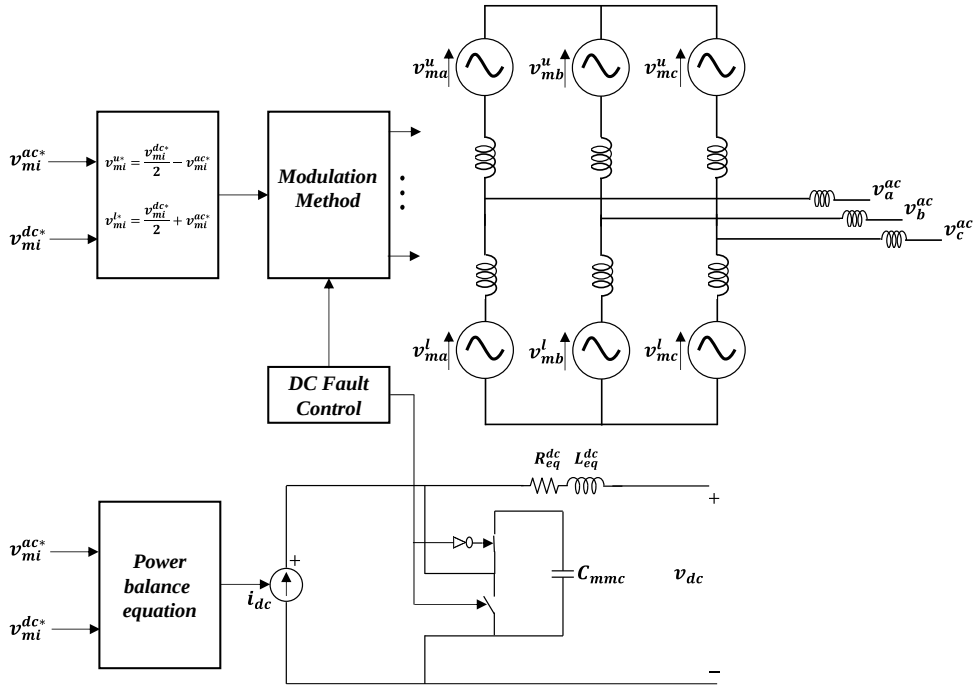

Figure II-14: Reduced order averaged model including blocking capability.

In [58], the blocked state has been integrated for the EM and AVM. The proposed solution consists in switching between two circuit models (controlled and blocked). By using a numerical solution (changing the time step of the simulation), the transients between these two circuits have been achieved. The drawback of using this solution is situated in their implementation method. The latter is based on an algorithm and not analytic equations which complicate their implementation in different EMT programs. Moreover, the transition between two circuits has to be adapted for each EMT program when this solution is considered.

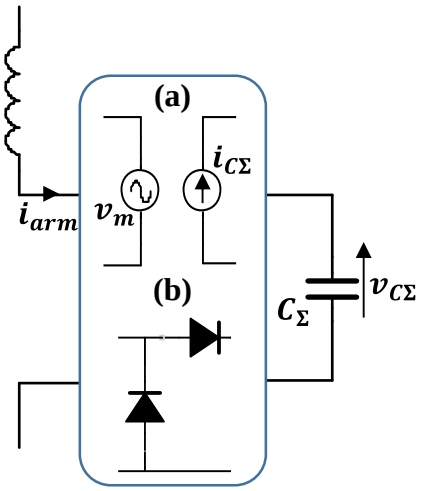

Figure II-15: Reduced order averaged arm model: (a) controlled state, (b) blocked state.

4. Scientific contributions

The main contribution of the following work is to propose a new modeling technique in order to integrate the previous functionalities; blocked and faulted conditions. The advantages of the proposed models is that all the possible states (controlled, blocked and faulted) are modeled using unique models to avoid the transition between two models as it was proposed in the first solution [58]. Furthermore, only simple functions are used to derive these models in order to facilitate their integration in EMT programs.

By adding the blocked and faulted states (see Figure II-16), the different SM configurations with their associated state variables are summarized in Table II-3.

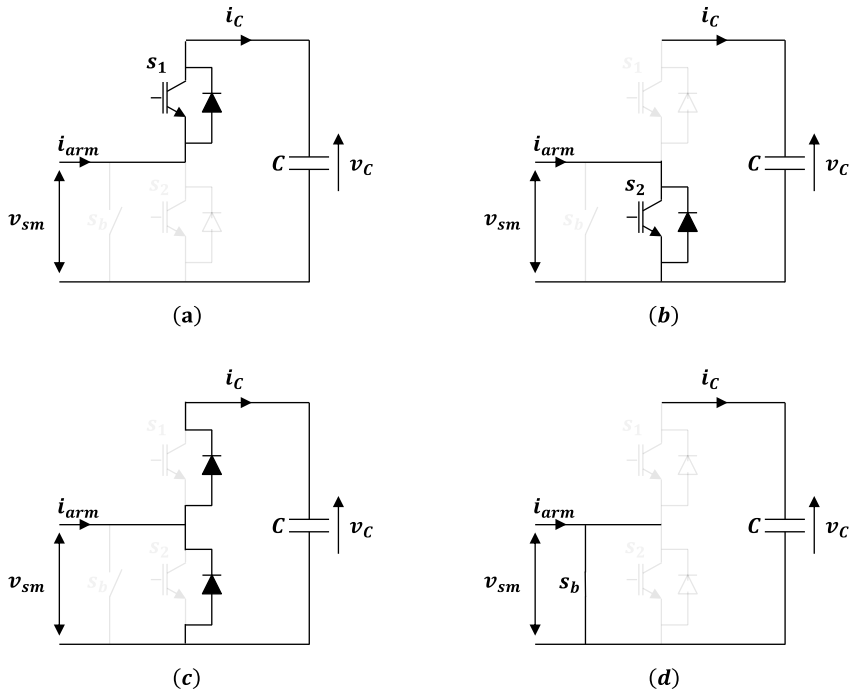

Figure II-16: SM Configurations including blocked and fault states.

Table II-3: State variables for SM configurations including controlled, blocked and faulted states.

Switches states	***State variables***	
Inserted SM (a) $(s_1 = 1, s_2 = 0, s_b = 0)$	$v_{sm} \approx v_c$ $i_c = i_{arm}$	
Bypassed SM (b) $(s_1 = 0, s_2 = 1, s_b = 0)$	$v_{sm} \approx 0$ $v_c = cst$ $i_c = 0$	
Blocked SM (c) $(s_1 = 0, s_2 = 0, s_b = 0)$	$i_{arm} > 0$ $v_{sm} \approx v_c$ $i_c = i_{arm}$	$i_{arm} \leq 0$ $v_{sm} \approx 0$ $v_c = cst$ $i_c = 0$
Faulted / out of order SM (d) $(s_1 = 0, s_2 = 0, s_b = 1)$	$v_{sm} \approx 0$ $v_c = cst$ $i_c = 0$	

4.1. Semi-analytical modeling technique

Based on a mixed (semi-analytical) modeling technique, a new implementation method has been proposed in [59] for the reduced order averaged arm model. In this thesis, novel full order model versions based on the same approach have been proposed [60, 61]. After that, this method has been extended to other MMC topologies such as the Full-Bridge [62] and Clamp-Double SM (CDSM) [63].

As indicated by its name, this technique is based on a circuit part and analytical one (see Figure II-17). The arm circuit is reduced to two controlled voltage sources and two diodes. The controlled source $v_{m,c}$ represents the inserted voltage by the SMs which are in controlled state. On the other hand, the controlled source $v_{m,b}$ represents the inserted voltage by the SMs when the IGBTs are blocked. Since the state variables change the value according to current direction when the blocked state is activated, the two diodes are used to obtain current direction. The analytic part contains the equations that describe the arm. It exchanges information with circuit part by receiving measurements (currents) and sending voltages values to the controlled sources. The inputs and outputs of this bloc change according to the type of models presented in the previous section.

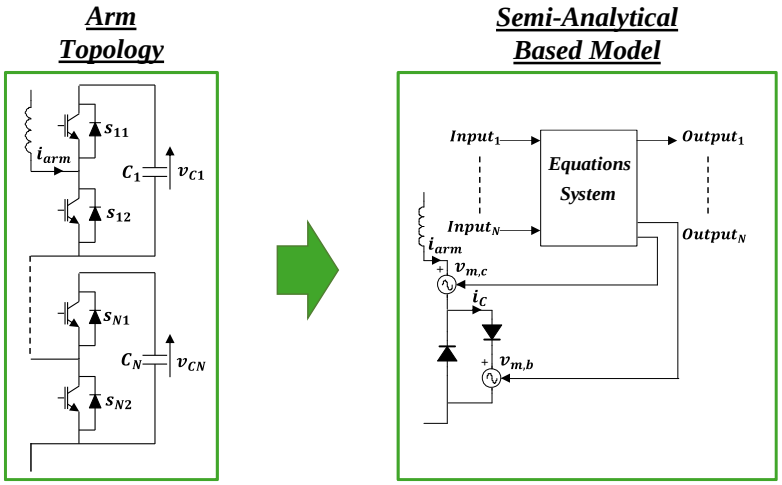

Figure II-17: Semi-analytical model proposed in [61].

Other semi-analytical based models have been presented in [64, 65]. In [64], the same approach as Figure II-17 has been used. The difference is situated in the position of controlled source (see Figure II-18). Another implementation method has been proposed in [65], it is based on one controlled voltage source, one controlled switch and two diodes. Although the difference

between these three models, they are supposed to reproduce the same behavior whatever the arm state is.

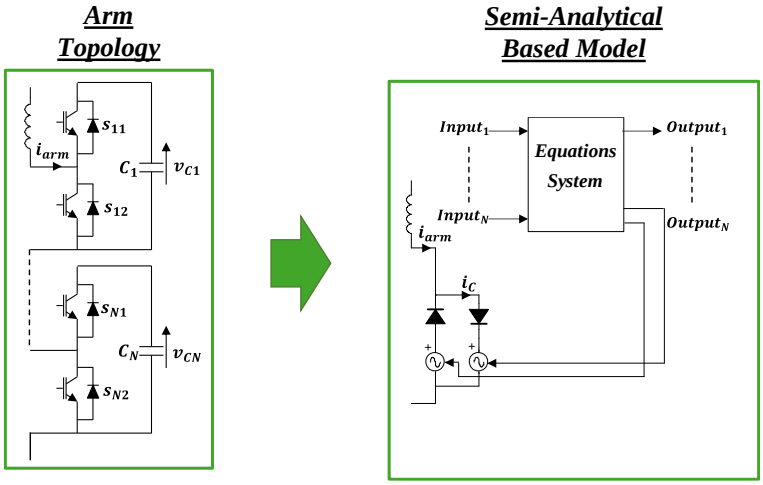

Figure II-18: Semi-analytical model proposed in [64]

4.1.1. Full order detailed model based on semi-analytical modeling technique

In order to derive the equations system for DM with this modeling technique, first, only one SM is considered. According to the Table II-4, three switching functions are necessary to represent SM configurations.

u_c: Switching function representing the controlled state, 1 when the SM is inserted and 0 when it is bypassed.

u_b: Switching function representing the blocked state, 1 when the SM is blocked and 0 when it is controlled.

u_f: Switching function representing the faulted state, 1 when the SM is out of order and 0 when it is available.

Table II-4: Switching functions used for semi-analytical modeling technique

<table>
<tr><th>Switches states</th><th colspan="2">State variables</th><th>Switching functions</th></tr>
<tr><td>Inserted SM
$(s_1 = 1, s_2 = 0, s_b = 0)$</td><td colspan="2">$v_{sm} \approx v_c$
$i_c = i_{arm}$</td><td>$u_c = 1$
$u_b = 0$
$u_f = 0$</td></tr>
<tr><td>Bypassed SM
$(s_1 = 0, s_2 = 1, s_b = 0)$</td><td colspan="2">$v_{sm} \approx 0$
$v_c = cst$
$i_c = 0$</td><td>$u_c = 0$
$u_b = 0$
$u_f = 0$</td></tr>
<tr><td rowspan="2">Blocked SM
$(s_1 = 0, s_2 = 0, s_b = 0)$</td><td>$i_{arm} > 0$</td><td>$i_{arm} \leq 0$</td><td rowspan="2">$u_c = 0$
$u_b = 1$
$u_f = 0$</td></tr>
<tr><td>$v_{sm} \approx v_c$
$i_c = i_{arm}$</td><td>$v_{sm} \approx 0$
$v_c = cst$
$i_c = 0$</td></tr>
<tr><td>Faulted / Out of order SM
$(s_1 = 0, s_2 = 0, s_b = 1)$</td><td colspan="2">$v_{sm} \approx 0$
$v_c \approx cst$
$i_c = 0$</td><td>$u_c = 0$
$u_b = 0$
$u_f = 1$</td></tr>
</table>

The equations describing the SM variables can be derived using the switching functions obtained above and current measurements as follow:

$$v_C = \frac{1}{C}\int (i_{arm}\, u_c\, \overline{u_b} + i_C\, u_b)\, \overline{u_f}$$

$$v_{sm,c} = (R_{on}\, i_{arm} + v_C\, u_c\, \overline{u_b})\, \overline{u_f} \qquad \textit{(II-10)}$$

$$v_{sm,b} = v_C\, u_b\, \overline{u_f}$$

Where:

i_C: Capacitor current (A).

$v_{sm,c}$: Inserted SM voltage when it is in controlled state (V).

$v_{sm,b}$: Inserted SM voltage when it is in blocked state (V).

When all SMs are considered, the detailed model can be reduced to the model of Figure II-19 by using three switching variables and 2 measurements.

For a MMC with N SMs per arm, the equations system can be written as follow:

$$for\ j = 1,2, \dots N$$

$$v_{Cj} = \frac{1}{C_j} \int \left(i_{arm}\, u_{cj}\, \overline{u_{bj}} + i_C\, u_{bj} \right) \overline{u_{fj}}$$

$$R_{loss} = \sum_{j=1}^{N} R_{on}\, \overline{u_{fj}}$$

$$C_{\Sigma} = \sum_{j=1}^{N} C_j\, \overline{u_{fj}} \qquad \textit{(II-11)}$$

$$v_{C\Sigma} = \sum_{j=1}^{N} v_{Cj}$$

$$v_{m,c} = R_{loss}\, i_{arm} + \sum_{j=1}^{N} v_{Cj}\, u_{cj}\, \overline{u_{bj}}$$

$$v_{m,b} = \sum_{j=1}^{N} v_{Cj}\, u_{bj}$$

The equations (II-11) show that the SMs states are modelled with a unique model using simple functions (mathematic and logic operations). This advantage simplifies its implementation in EMT programs. It is worth noting that, when the faulted state is considered, C_{Σ} and u_{fj} have to be communicate to the control system since the tuning of energy loops and balancing control algorithm (BCA) are based on these parameters respectively (see CHAPTER III).

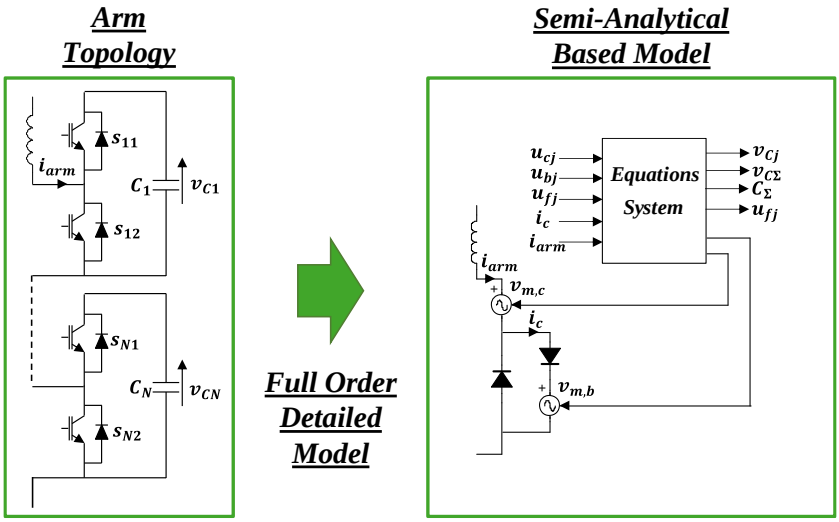

Figure II-19: Full order detailed model based on semi-analytical modeling technique.

4.1.2. Full order equivalent model based on semi-analytical modeling technique

To recall, the aim of this model type is to have an equivalent Thevenin or Norton circuit for each SM. For this purpose, each SM capacitor is replaced by an equivalent voltage source $v_{Ceq}(t)$ in series with an impedance R_C by using trapezoidal integration method. According to Table II-4, the variation of voltage source can be expressed by the following formula:

$$R_C = \frac{T_s}{2C}$$
$$v_C = v_{Ceq}(t) = R_C(i_{arm}(t-T_s)\, u_c\, \overline{u_b} + i_C(t-T_s)\, u_b)\, \overline{u_f} + v_{Ceq}(t-T_s) \quad \textit{(II-12)}$$

Including the blocking and faulted states, the expression of switch resistances can be expressed by:

$$R_1 = \left(R_{on}\left(u_c\, \overline{u_b} + \frac{|i_C|}{|i_{arm}|}u_b\right) + R_{off}\left(\overline{u_c}\, \overline{u_b} + \left(1 - \frac{|i_C|}{|i_{arm}|}\right)u_b\right)\right)\overline{u_f}$$
$$R_2 = \left(R_{off}\left(u_c\, \overline{u_b} + \frac{|i_C|}{|i_{arm}|}u_b\right) + R_{on}\left(\overline{u_c}\, \overline{u_b} + \left(1 - \frac{|i_C|}{|i_{arm}|}\right)u_b\right)\right)\overline{u_f} \quad \textit{(II-13)}$$

The inserted SM voltage can be derived using the equivalent Thevenin circuit (one voltage source in series with impedance).

$$R_{eq}^{th} = \frac{R_2\,(R_1 + R_c)}{R_2 + R_1 + R_c}$$

$$v_{eq}^{th} = v_C \frac{R_2}{R_2 + R_1 + R_c} \qquad \textit{(II-14)}$$

$$v_{sm_c} = \left(R_{eq}^{th}\, i_{arm} + v_{eq}^{th}\right) \overline{u_b}\; \overline{u_f}$$

$$v_{sm_b} = \left(R_{eq}^{th}\, i_{arm} + v_{eq}^{th}\right) u_b\; \overline{u_f}$$

When all SMs are considered, the modulated voltage inserted per arm can be obtained with the following equations system.

$$for\ j = 1,2, \dots N$$

$$R_{j1} = \left(R_{on}\left(u_{cj}\,\overline{u_{bj}} + \frac{|i_C|}{|i_{arm}|}u_{bj}\right) + R_{off}\left(\overline{u_{cj}}\,\overline{u_{bj}} + \left(1 - \frac{|i_C|}{|i_{arm}|}\right)u_{bj}\right)\right)\overline{u_{fj}}$$

$$R_{j2} = \left(R_{off}\left(u_{cj}\,\overline{u_{bj}} + \frac{|i_C|}{|i_{arm}|}u_{bj}\right) + R_{on}\left(\overline{u_{cj}}\,\overline{u_{bj}} + \left(1 - \frac{|i_c|}{|i_{arm}|}\right)u_{bj}\right)\right)\overline{u_{fj}}$$

$$R_{Cj} = \frac{T_s}{2\,C_j}$$

$$i_{Cj} = \left(i_{arm}(t - T_s)\,u_{cj}\,\overline{u_{bj}} + i_C(t - T_s)\,u_{bj}\right)\overline{u_{fj}} \qquad \textit{(II-15)}$$

$$v_{Cj} = v_{Ceqj}(t) = R_{Cj}\,i_{Cj} + v_{Ceqj}(t - T_s)$$

$$C_\Sigma = \sum_{j=1}^{N} C_j\,\overline{u_{fj}}$$

$$v_{C\Sigma} = \sum_{j=1}^{N} v_{Cj}\,\overline{u_{fj}}$$

$$R_{eqj}^{th} = \frac{R_{j2}\left(R_{j1} + R_{Cj}\right)}{R_{j2} + R_{j1} + R_{Cj}}$$

$$v_{eqj}^{th} = v_{Cj}\frac{R_{j2}}{R_{j2} + R_{j1} + R_{Cj}}$$

$$v_{m,c} = \sum_{j=1}^{N}\left(R_{eqj}^{th}\, i_{arm} + v_{eqj}^{th}\right)\overline{u_{bj}}\,\overline{u_{fj}}$$

$$v_{m,b} = \sum_{j=1}^{N}\left(R_{eqj}^{th}\, i_{arm} + v_{eqj}^{th}\right) u_{bj}\,\overline{u_{fj}}$$

Since the detailed and equivalent models are full order ones, the inputs and outputs of equations system are same for both (see Figure II-20).

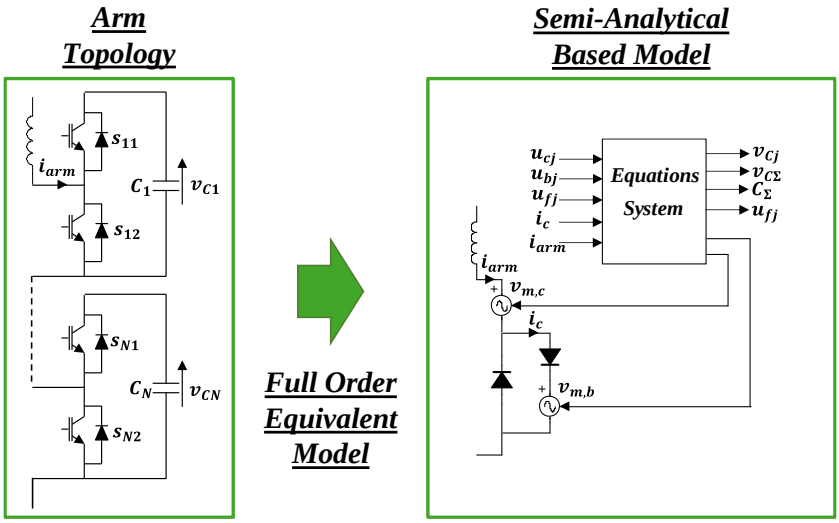

Figure II-20: Full order equivalent model based on semi-analytical modeling technique.

4.1.3. Reduced order averaged arm model based on semi-analytical modeling technique

The semi-analytical modeling technique has been firstly proposed for the averaged model in [59], however, the fault condition has not been considered.

Since the SMs are aggregated to one capacitor, all SMs have the same state. That means, the blocked and faulted states will concern the whole arm and not each SM as the full order models.

Taking into account the three MMC states, new parameters are used to derive the equations for averaged arm model:

f: Switching function for faulted state, 1 when the arm is faulted and 0 when it is available.

b: Switching function for blocked state, 1 when the arm is blocked and 0 when it is controlled.

m: Averaged function "modulation index"; m = [0,1].

Based on these functions and current measurements, the equations system for semi-analytical model can be written as follows:

$$i_{C\Sigma} = \left(m\,\bar{b}\,i_{arm} + b\,i_C\right)\bar{f}$$

$$C_\Sigma = \frac{C}{N}$$

$$v_{C\Sigma} = \frac{1}{C_\Sigma}\int i_{C\Sigma}\,\bar{f} \qquad \textit{(II-16)}$$

$$R_{loss} = N\,R_{on}\,\bar{f}$$

$$v_{m,c} = \left(R_{loss}\,i_{arm} + m\,\bar{b}\,v_{C\Sigma}\right)\bar{f}$$

$$v_{m,b} = b\,v_{C\Sigma}\,\bar{f}$$

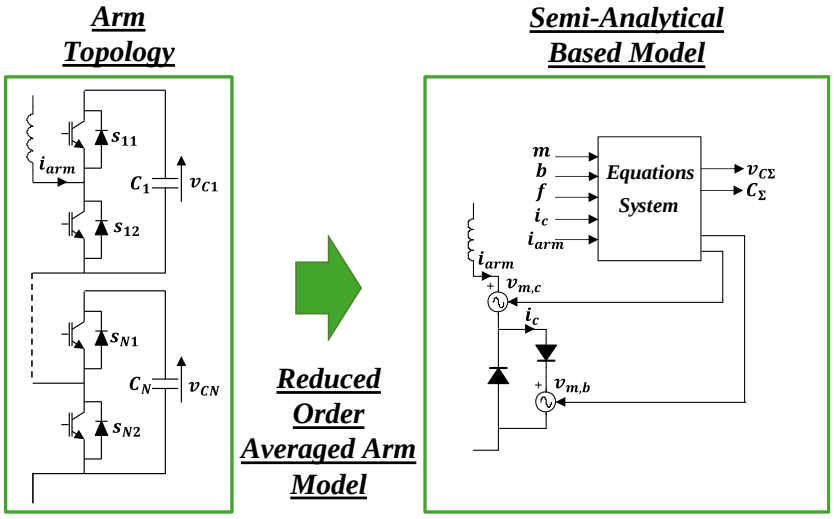

Figure II-21: Reduced order averaged arm model based on semi-analytical modeling technique.

4.2. Analytical modeling technique

Another modeling technique based on analytical based implementation can be used to obtain general MMC models. In this solution, only one controlled source is used as a circuit part as it is shown in Figure II-22. Theoretically, for the same simulation time-step, decreasing the

number of elements (switches and sources) in the model will accelerate the simulation time compared to the first solution. On the other hand, the equations system controlling the source has to adapt its output voltage to represent the three states which makes complicated the related equations building. It has been seen in the first solution that the current direction is important when the blocked state is activated. Since there are not switches inside the model using this solution, a new variable indicating current direction is used to derive the analytical equations [126].

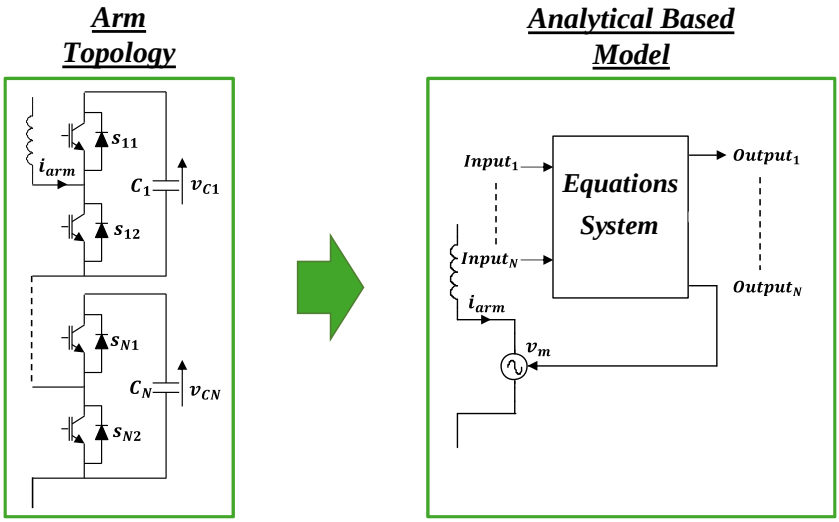

Figure II-22: Proposed analytical model.

4.2.1. Full order detailed model based on analytical modeling technique

Considering only one SM and according to Table II-5, the equations describing the SM state variables can be derived using four switching functions and current measurement:

$$v_C = \frac{1}{C}\int \left(u_c\ \overline{u_b} + \left(\frac{1 + sign(i_{arm})}{2}\right) u_b \right) i_{arm}\ \overline{u_f} \qquad (II\text{-}17)$$

$$v_{sm} = \left(R_{on}\ i_{arm} + \left(u_c\ \overline{u_b} + \left(\frac{1 + sign(i_{arm})}{2}\right) sign(i_{arm})\ u_b \right)\ v_C \right)\ \overline{u_f}$$

Where:

u_c: Switching function for controlled state, 1 when the SM is inserted and 0 when it is bypassed.

u_b: Switching function for blocked state, 1 when the SM is blocked and 0 when it is controlled.

u_f: Switching function for faulted state, 1 when the SM is in out of order state and 0 when it is available.

$sign(i_{arm})$: Switching function for current direction, 1 when the current is positive, 0 when it is null and -1 when it is negative.

i_{arm}: Arm current (A).

v_{sm}: Inserted SM voltage (V).

Table II-5: Switching functions used for analytical modeling technique.

<table>
<tr><th>Switches States</th><th colspan="3">State variables</th><th colspan="3">Switching functions</th></tr>
<tr><td>Inserted SM
$(s_1 = 1, s_2 = 0, s_b = 0)$</td><td colspan="3">$v_{sm} \approx v_c$
$i_c = i_{arm}$</td><td colspan="3">$u_c = 1$
$u_b = 0$
$u_f = 0$</td></tr>
<tr><td>Bypassed SM
$(s_1 = 0, s_2 = 1, s_b = 0)$</td><td colspan="3">$v_{sm} \approx 0$
$v_c = cst$
$i_c = 0$</td><td colspan="3">$u_c = 0$
$u_b = 0$
$u_f = 0$</td></tr>
<tr><td rowspan="2">Blocked SM
$(s_1 = 0, s_2 = 0, s_b = 0)$</td><td>$i_{arm} > 0$</td><td>$i_{arm} < 0$</td><td>$i_{arm} = 0$</td><td rowspan="2">$u_c = 0$
$u_b = 1$
$u_f = 0$</td><td rowspan="2">$u_c = 0$
$u_b = 1$
$u_f = 0$</td><td rowspan="2">$u_c = 0$
$u_b = 1$
$u_f = 0$</td></tr>
<tr><td>$v_{sm} \approx v_c$
$i_c = i_{arm}$</td><td>$v_{sm} \approx 0$
$v_c = cst$
$i_c = 0$</td><td>$v_{sm} \approx 0$
$v_c = cst$
$i_c = 0$</td></tr>
<tr><td>Faulted / Out of order SM
$(s_1 = 0, s_2 = 0, s_b = 1)$</td><td colspan="3">$v_{sm} \approx 0$
$v_c \approx cst$
$i_c = 0$</td><td colspan="3">$u_c = 0$
$u_b = 0$
$u_f = 1$</td></tr>
<tr><td></td><td></td><td></td><td></td><td>$sign(i_{arm}) = 1$</td><td>$sign(i_{arm}) = -1$</td><td>$sign(i_{arm}) = 0$</td></tr>
</table>

When all the SMs are considered, the arm model can be reduced to one voltage source (see Figure II-23). The equations system describing the detailed model can be expressed by:

$$for\ j = 1,2, \dots N$$

$$v_{Cj} = \frac{1}{C_j} \int \left(u_{cj}\, \overline{u_{bj}} + \left(\frac{1 + sign(i_{arm})}{2} \right) u_{bj} \right) i_{arm}\, \overline{u_{fj}}$$

$$R_{arm} = \sum_{j=1}^{N} R_{on}\, \overline{u_{fj}}$$

$$C_{\Sigma} = \sum_{j=1}^{N} C_j\, \overline{u_{fj}} \qquad \textit{(II-18)}$$

$$v_{C\Sigma} = \sum_{j=1}^{N} v_{Cj}\, \overline{u_{fj}}$$

$$v_m = R_{arm}\, i_{arm} + \sum_{j=1}^{N} \left(u_{cj}\, \overline{u_{bj}} + \left(\frac{1 + sign(i_{arm})}{2} \right) sign(i_{arm})\, u_{bj} \right) v_{Cj}\, \overline{u_{fj}}$$

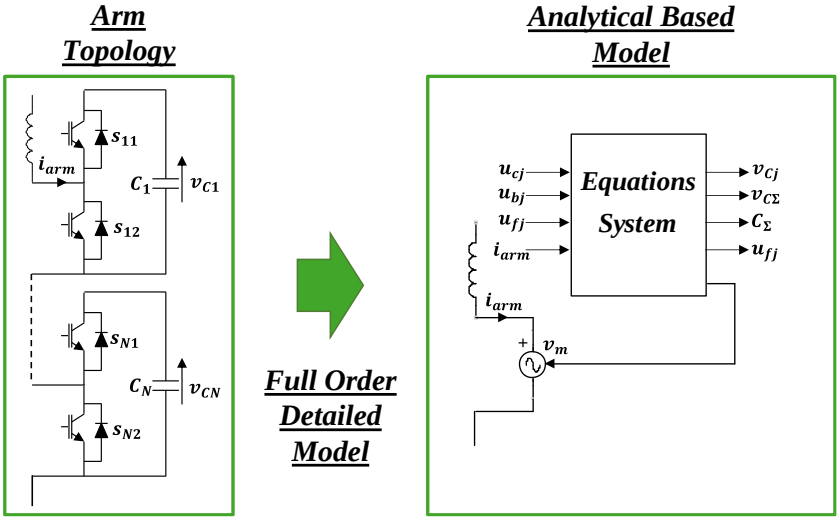

Figure II-23: Full order detailed model based on analytical modeling technique.

4.2.2. Full order equivalent model based on analytical modeling technique

The analytical model can be also applied to the equivalent model. The variation of voltage source can be derived using the following expression:

$$R_C = \frac{T_s}{2C}$$

$$v_{Ceq}(t) = R_C \left(u_c \, \overline{u_b} + \left(\frac{1 + sign(i_{arm})}{2} \right) u_b \right) i_{arm}(t - T_s) \, \overline{u_f} + v_{Ceq}(t - T_s) \quad \textit{(II-19)}$$

The equivalent Thevenin circuit for one SM can be calculate as follow:

$$R_1 = \left(R_{on} \left(u_c \, \overline{u_b} + \left(\frac{1+sign(i_{arm})}{2} \right) sign(i_{arm}) \, u_b \right) + R_{off} \left(\overline{u_c} \, \overline{u_b} - \left(\left(\frac{1-sign(i_{arm})}{2} \right) sign(i_{arm}) - (1 - |sign(i_{arm})|) \right) u_b \right) \right) \overline{u_f}$$

$$R_2 = \left(R_{off} \left(u_c \, \overline{u_b} + \left(\left(\frac{1+sign(i_{arm})}{2} \right) sign(i_{arm}) + (1 - |sign(i_{arm})|) \right) u_b \right) + R_{on} \left(\overline{u_c} \, \overline{u_b} - \left(\frac{1-sign(i_{arm})}{2} \right) sign(i_{arm}) \, u_b \right) \right) \overline{u_f} \quad \textit{(II-20)}$$

$$R_{th_{eq}} = \frac{R_2 \, (R_1 + R_c)}{R_2 + R_1 + R_c}$$

$$v_{th_{eq}} = v_c \frac{R_2}{R_2 + R_1 + R_c}$$

For MMC arm with *N* SMs, the equations system for equivalent model is given by the following expressions:

$$for \; j = 1,2, \dots N$$

$$R_{j1} = \left(R_{on} \left(u_{cj} \, \overline{u_{bj}} + \left(\frac{1+sign(i_{arm})}{2} \right) sign(i_{arm}) \, u_{bj} \right) + R_{off} \left(\overline{u_{cj}} \, \overline{u_{bj}} - \left(\left(\frac{1-sign(i_{arm})}{2} \right) sign(i_{arm}) - (1 - |sign(i_{arm})|) \right) u_{bj} \right) \right) \overline{u_{fj}}$$

$$R_{2j} = \left(R_{off} \left(u_{cj}\, \overline{u_{bj}} + \left(\left(\frac{1+sign(i_{arm})}{2} \right) sign(i_{arm}) + (1 - |sign(i_{arm})| \right) u_{bj} \right) + R_{on} \left(\overline{u_{cj}}\, \overline{u_{bj}} - \left(\frac{1-sign(i_{arm})}{2} \right) sign(i_{arm})\, u_{bj} \right) \right) \overline{u_{fj}}$$

$$R_{Cj} = \frac{T_s}{2\, C_j}$$

$$v_{Cj} = \left(R_{Cj} \left(u_c\, \overline{u_b} + \left(\frac{1+sign(i_{arm})}{2} \right) u_b \right) i_{arm}(t - T_s)\, u_{fj} + v_{ceqj}(t - T_s) \right) \overline{u_{fj}}$$

$$v_{C\Sigma} = \sum_{j=1}^{N} v_{Cj}\, \overline{u_{fj}} \qquad \textit{(II-21)}$$

$$R_{eqj}^{th} = \frac{R_{j2} \left(R_{j1} + R_{Cj} \right)}{R_{j2} + R_{j1} + R_{Cj}} \overline{u_{fj}}$$

$$v_{eqj}^{th} = v_{Cj} \frac{R_{j2}}{R_{j2} + R_{j1} + R_{Cj}} \overline{u_{fj}}$$

$$v_m = \sum_{j=1}^{N} \left(R_{eqj}^{th}\, i_{arm} + v_{eqj}^{th} \right) \overline{u_{fj}}$$

The obtained model is duplicated in Figure II-24.

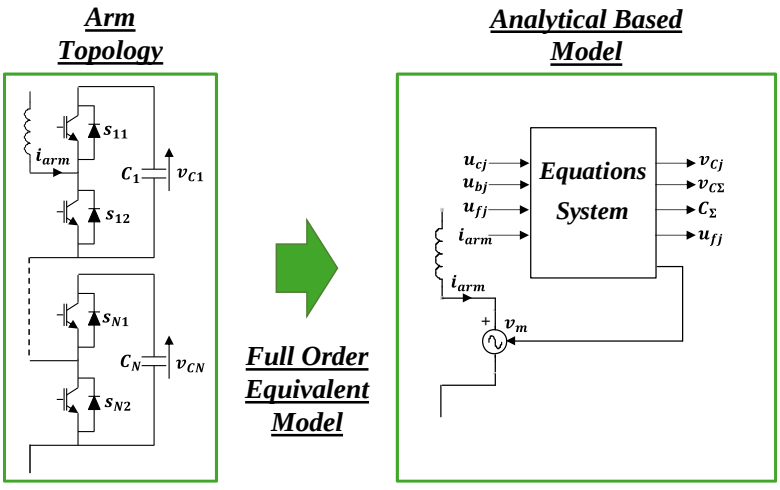

Figure II-24: Full order equivalent model based on analytical modeling technique.

4.2.3. Reduced order averaged arm model based on analytical modeling technique

In the averaged arm model, all SM voltages are considered to be well balanced and treated with the same manner. The switching functions used to derive the analytical model are:

f: Switching function for faulted state, 1 when the arm is out of order and 0 when it is available.

b: Switching function for blocked state, 1 when the arm is blocked and 0 when it is controlled.

m: Averaged function, modulation index. $m \in [0, 1]$.

$sign(i_{arm})$: Switching function for current direction, 1 when the current is positive, 0 when it is null and -1 when it is negative.

The averaged arm model can be reduced to one voltage source (see Figure II-25) controlled by the following system equations:

$$i_{C\Sigma} = \left(m\,\bar{b} + b\left(\frac{1 + sign(i_{arm})}{2}\right)\right) i_{arm}\,\bar{f}$$

$$C_{\Sigma} = \frac{C}{N}$$

$$v_{C\Sigma} = \frac{1}{C_{\Sigma}} \int i_{C\Sigma} \qquad \textit{(II-23)}$$

$$R_{loss} = N\,R_{on}\,\bar{f}$$

$$v_m = \left(R_{loss}\,i_{arm} + \left(m\,\bar{b} + b\left(\frac{1 + sign(i_{arm})}{2} sign(i_{arm})\right)\right) v_{C\Sigma}\right)\bar{f}$$

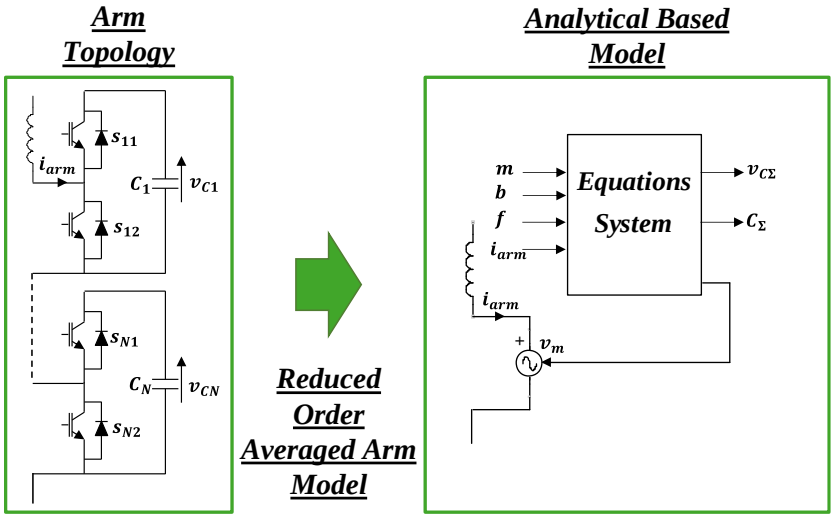

Figure II-25: Reduced order averaged arm model based on analytical modeling technique.

5. Validation of proposed models

In this section, the proposed models are compared and validated by simulation in order to assess their accuracy. The simulations have been carried out in Matlab/Simulink program with 5 µs time-step using Backward Euler/Tustin solvers. For each simulation case, the dynamics behaviors of semi analytical (SM) and analytical (AM) modeling for the three model types are compared regarding the benchmark model (detailed model based on circuit implementation (CM)) under different operation conditions. Since the obtained results are quite similar, only the simulation results for the detailed models are shown here; the equivalent and averaged models results are presented in APPENDICES (see section 1)

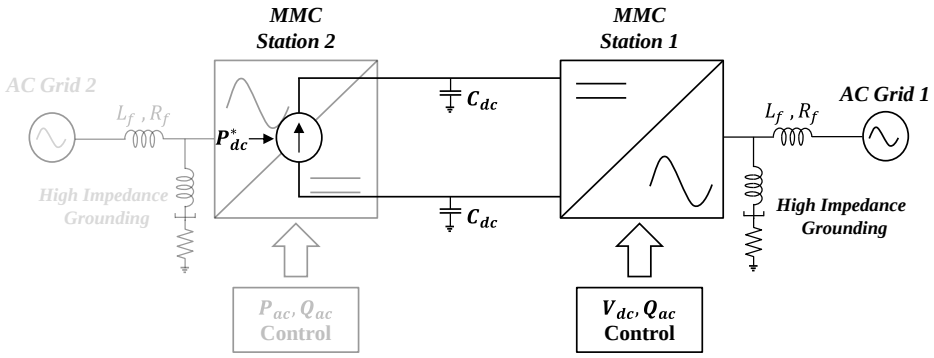

Figure II-26: Simulation circuit for models validation.

The case study is a point-to-point MMC based HVDC link where the parameters of the stations are presented in Table II-6. These parameters correspond to those available in EMTP-RV MMC

library. For simulation time reasons, the simulated MMC benchmark is reduced to 40 SMs instead of 400.

To simulate such system, it is necessary to design a dedicated control for each station. To do so, an energy based control (the next chapter discuss this MMC control in details) in DC voltage mode is employed to control the station 1.

In order to simplify the system, a DC current source is used to emulate the station 2 which is controlled in active power mode.

Table II-6: MMC station parameters for models validation.

Nominal power [MW]	*1000*
AC nominal voltage v_{ac}[kV]	*320 (rms line to line)*
DC nominal voltage v_{dc}[kV]	*640 (pole to pole)*
Number of SM	*40*
Inductance of the grid reactor L_f [pu]	*0.18*
Resistance of the grid reactor R_f [pu]	*0.005*
Arm resistance R_{arm}[pu]	*0.01*
Arm inductance L_{arm} [pu]	*0.15*
Electrostatic Constant H_c (ms)	*0.04*
Capacitor Cable C_{dc} [µF]	*48.4*

5.1. Controlled state tests

In this section, the validation of the dynamics response of the proposed models regarding two different step changes coming from the control layer is studied.

5.1.1. Step change in DC power reference

In the following test, the models are compared with a step change in DC current source. Initially the station does not exchange any power with AC and DC grids, at t=0.1 s, a step of 0.5 is applied to the DC current source reference. The obtained results are presented in Figure II-27 where the active power, the DC current and the average SM voltages for upper and low arms

for a given leg are presented in (a)-(c) respectively. The results show that the three models have the same behavior during transient as well as during the steady state.

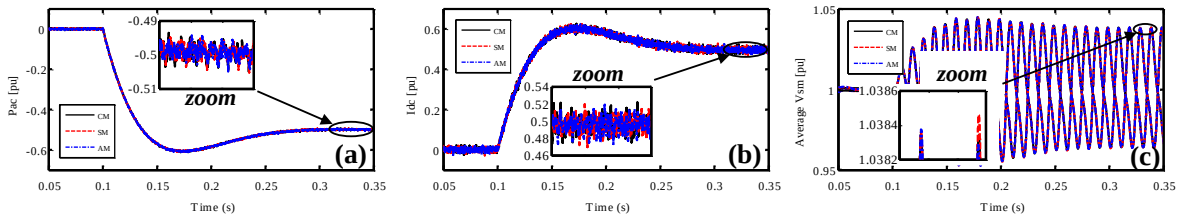

Figure II-27: Dynamics response of detailed models for a DC power step change: (a) active power, (b) DC current, (c) average SM voltages for upper and lower arms for phase a.

5.1.2. Step change in stored energy reference

One of the advantages using energy based control is the decoupling between the DC grid voltage and SM voltages. This degree of freedom is tested in the following test case; at 0.5 s, the reference of SM voltages is increased from 1 pu to 1.05 pu. The results, see Figure II-28 show that the proposed model appears to be a good representation of the benchmark model during energy change.

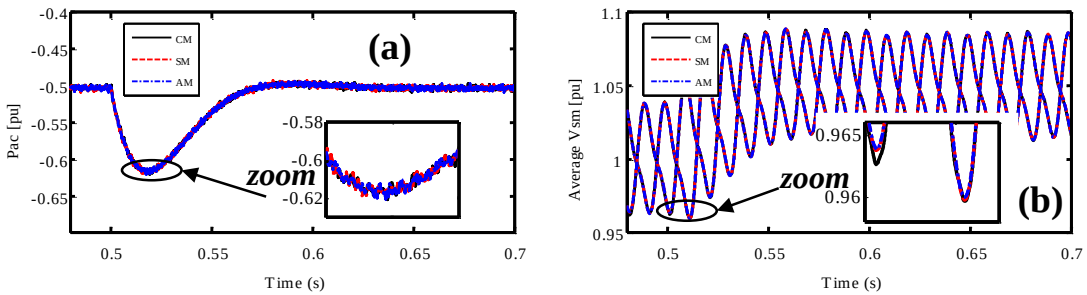

Figure II-28: Dynamics response of detailed models for a stored energy step change: (a) active power and (b) average SMs voltages for upper and lower arms for phase a.

5.2. Blocked state tests

In this section, the behavior in blocking mode of the proposed model is investigated. For this purpose, external disturbances are simulated.

5.2.1. Three phase AC fault

In this test, a three phase to ground fault is created. Initially, the converter sends 0.5 pu power to the DC current source when the AC voltage drop from 1 pu to 0.01 pu at t = 1s. After 10 ms,

the blocking signals for each SM are activated to enable diode bridge rectifier mode. The simulations results are shown in Figure II-29 for active power, Figure II-30 for arm currents, Figure II-31 for DC current and Figure II-32 for average SM voltages for upper and lower arms.

It can be observed that, the three phase fault causes a drop in active power. Thus, the AC currents increase to compensate this drop. When the blocking state is activated (t =1.01s), the AC power converges to zero.

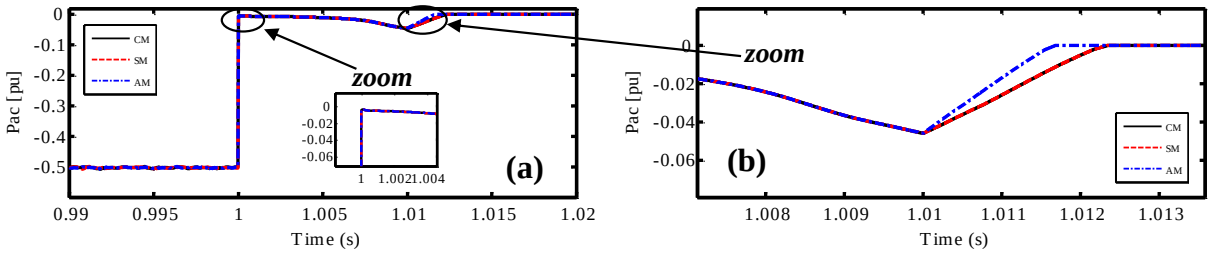

Figure II-29: Active power dynamics of detailed models for a three phase AC fault.

Thanks to the diodes represented as a circuit in the model, the semi analytical model gives the same dynamics as the benchmark model. Despite a small difference between the analytic model and the circuit one when the blocking state is activated, it allows a good representation without any circuit representation of switches. The differences are due to the presence of snubber in the switches for the benchmark models which is not well represented with the analytical model.

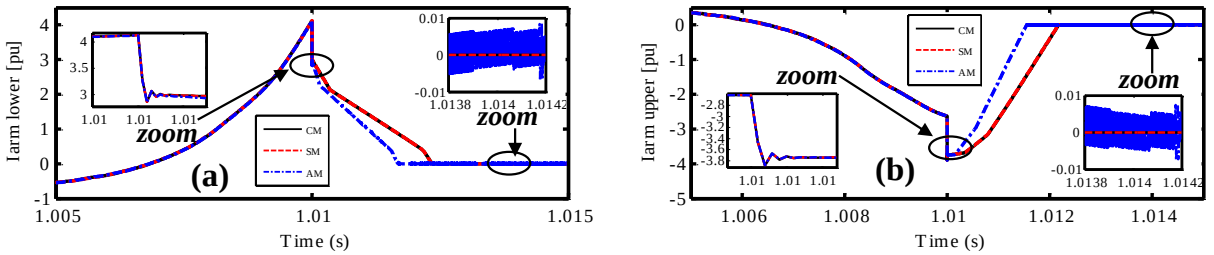

Figure II-30: Arm currents (phase a) dynamics of detailed models for a three phase AC fault.

Regarding the arm currents (see Figure II-30) and DC current (see Figure II-31) dynamics, the blocking activation is well represented with the proposed models. However, for the same reason as before, the convergence of arm currents to zero is a bit different for the analytical model. Moreover, some numerical oscillations can be observed in the steady state value of DC and arm currents. This phenomenon can be explained by the sign function used by the analytical model which is sensitive to the simulation time-step. By decreasing the time step those oscillations become smaller.

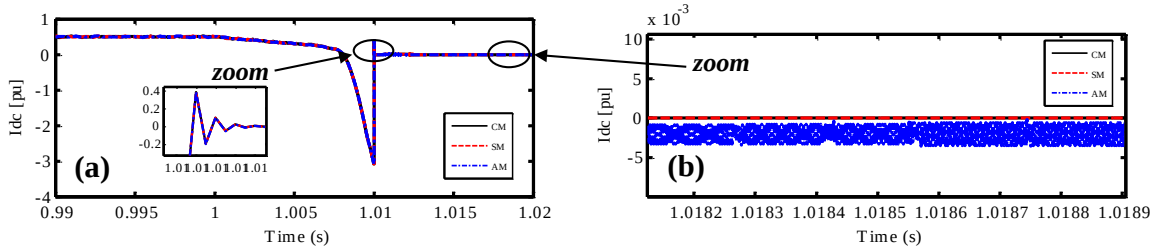

Figure II-31: DC current dynamics of detailed models for a three phase AC fault.

Due to the high value of the arm currents, the SM capacitors vary according to the currents directions. Once the blocking state is activated, they stay at a constant value as it is shown in Figure II-32.

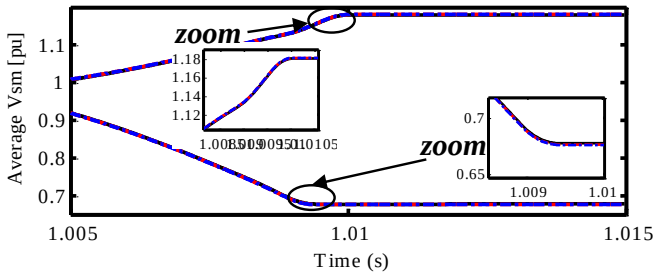

Figure II-32: Models dynamics of the detailed model for a three phase AC fault: average SMs voltages for upper and lower arm of phase a.

5.2.2. Pole to pole DC fault

In the following case, a permanent pole-to-pole DC fault is scheduled at t=1.5. The blocking state is activated after 0.5 ms to avoid a big discharge of SM capacitors. The dynamic responses produced by the three models are shown in Figure II-33 for DC current, Figure II-34 for active power, Figure II-35 for average SMs voltages for upper and lower arms and Figure II-36 for arm currents dynamics.

When the DC fault occurs, a high increase of DC current, due to the discharge of SMs and AC grid contribution, appears. When the blocking state is activated, the DC current takes a rectifier form with a peak and a steady state values around 12 pu and 8.5 pu respectively. It can be observed from Figure II-33 and Figure II-34 that the whole responses of the three models are quite equal.

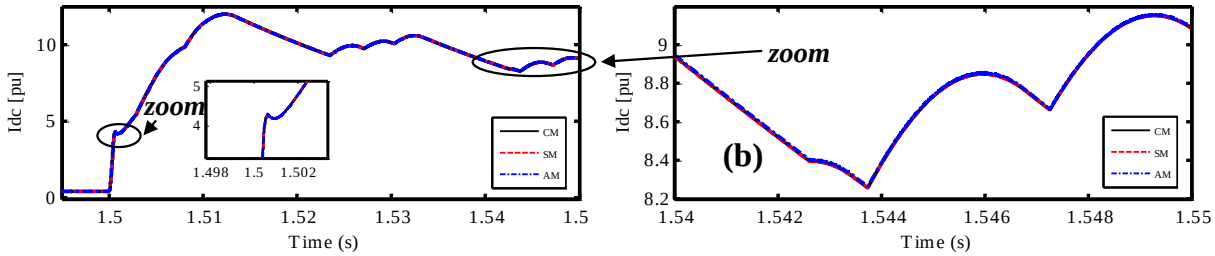

Figure II-33: DC current dynamics of detailed models for a pole-to-pole DC fault.

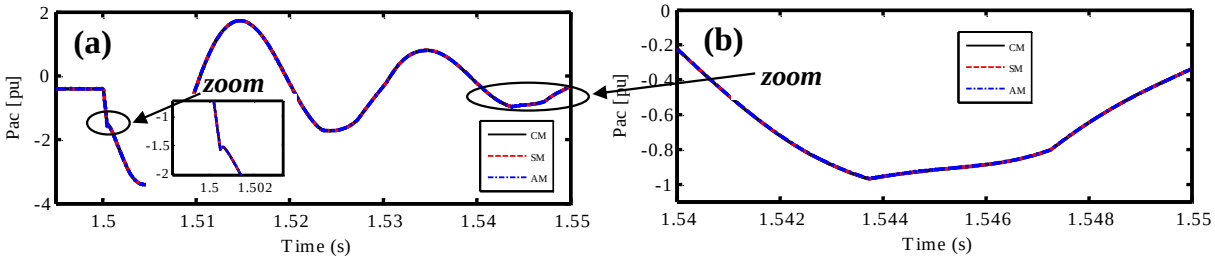

Figure II-34: Active power dynamics of detailed models for a pole-to-pole DC fault.

As indicated in Figure II-35, the blocking state allows stopping the SM capacitors discharging through the fault. This phenomenon is well represented with the semi analytical model as well as the analytical one.

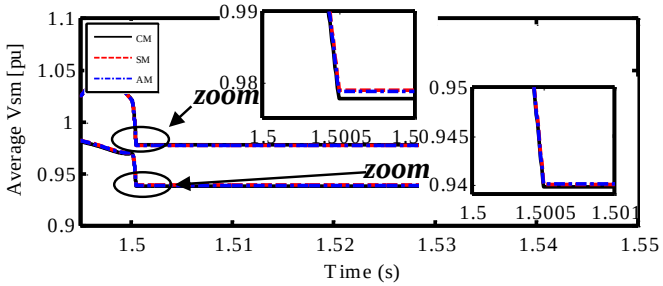

Figure II-35: Average SMs voltages for upper and lower arms dynamics of detailed models for a pole-to-pole DC fault.

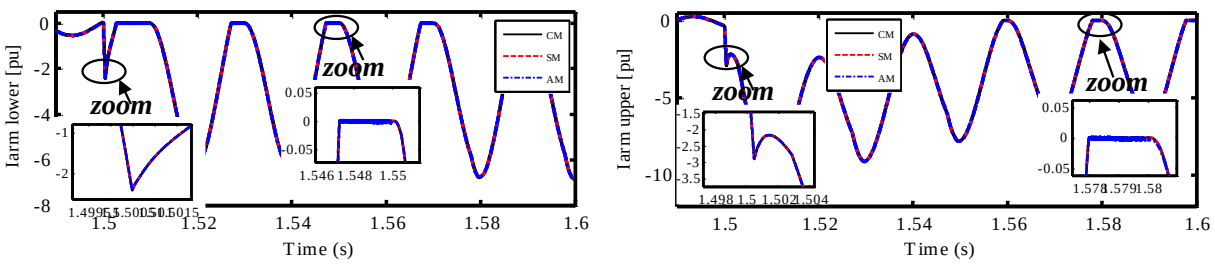

Figure II-36: Arm currents dynamics of detailed models for a pole-to-pole DC fault (phase a).

The sign function creates small numerical oscillations in the arms current when they are equal to zero, see Figure II-36. However, the results show a good agreement between the three models since the error introduced by the analytical model is less than 1%.

5.3. Faulted state tests

In this section, the dynamic behavior of the proposed models against SMs failure is investigated.

5.3.1. Loss of 10% SMs for one arm

The loss of 10% of SMs in upper arm for phase a is applied at t = 3 s. the transient response of the models are illustrated in Figure II-37-(a) for the active power and Figure II-37-(b) for average SM voltages for upper and lower arms. Thanks to the energy loops, the control detects this event and reacts by increasing the active power in order to compensate the lack of energy in the arm. It can be observed that the proposed models allow to simulation such transient operations.

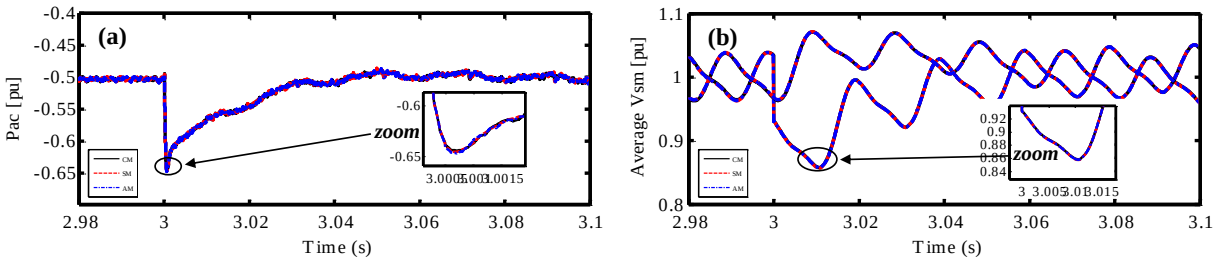

Figure II-37: Dynamics response of detailed models for a loss of 10% SMs in one arm: (a) active power, (b) average SM voltages for upper and lower arms for phase a.

5.3.2. Loss of one arm

In the following test, the loss of one arm is performed at t= 3.5 s. the corresponding results are shown in Figure II-38-(a) for the active power and Figure II-38-(b) for average SM voltages for upper and lower arms. It can be concluded that the proposed models are able to capture the transient of this operation condition with a good accuracy.

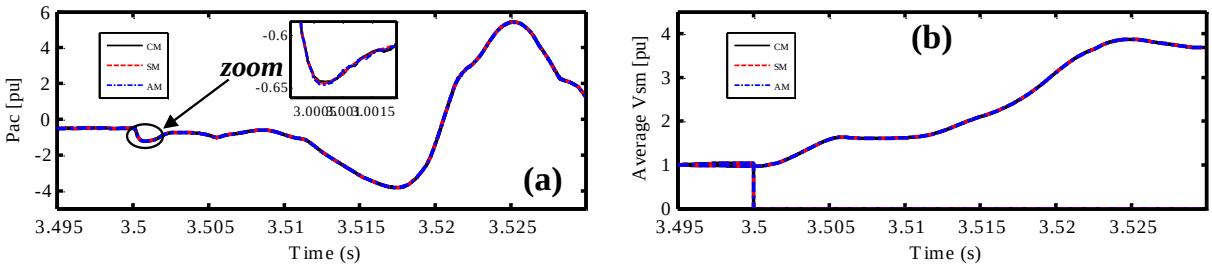

Figure II-38: Dynamics response of detailed models for a loss of one arm: (a) active power, (b) average SM voltages for upper and lower arms for phase a.

5.4. Simulation performances

To show the advantage of the proposed models in term of simulation performance, the simulation time of 1s for different MMC levels is calculated and compared. The simulations have been performed on a computer with a 3.6 GHz Intel Core XeonE5-1650V4 processor. The corresponding results are shown in Table II-7.

Table II-7: Simulation time of MMC models for 1 s effective time.

	Detailed Model			***Equivalent Model***			***Averaged Model***		
Number of SM	*400*	*100*	*40*	*400*	*100*	*40*	*400*	*100*	*40*
Benchmark (Circuit) model	*2100 s*	*308 s*	*160 s*	*/*	*/*	*/*	*/*	*/*	*/*
Semi-analytical	*87 s*	*38 s*	*18 s*	*85 s*	*33 s*	*17 s*	*12 s*	*12 s*	*12 s*
Analytical	*70 s*	*24 s*	*15 s*	*69 s*	*22 s*	*15 s*	*9 s*	*9 s*	*9 s*

As it is observed, the acceleration of the simulation with the proposed models is more important when the number of SM is relatively high. The semi analytical model allows reducing 2*N switches per arm to only two diodes keeping the same number of state variables. This allows reducing the size of system matrix created by the solver and consequently accelerating the simulation time. The system matrix is more reduced using analytical model since the switches are not employed as a circuit. Thus, the simulation is more accelerated.

6. Conclusion

In this chapter, the problems related to MMC modeling for HVDC application have been addressed. After a description of different MMC model types presented in the literature, the

implementation technique of some models including detailed, equivalent and averaged models has been analyzed and discussed. In order to improve and integrate the blocking and faulted states in these models, two new implementation methods have been proposed which are: Semi-analytical and Analytical methods. They allow obtaining unique models using simple functions to facilitate their integration in EMT programs on one hand and accelerate the simulation using less circuit elements on the other hand. The simulations with different operation conditions have proved that the proposed models give good accordance with the benchmark model. The proposed models will facilitate the integration of MMC in HVDC systems for different studies such as:

- Investigate the effect of low level control (full order models).
- Derive control laws for high level control (reduced order model) and their validations (full order models).
- Develop protection algorithms for large HVDC grids (reduced and full order models).

The various developed models will be used for simulations purposes as well as controls tuning in the next of this thesis.

CHAPTER III Modular Multilevel Converter Control

1. Introduction

As the MMC is a particular topology which involves huge number of state variables, the MMC control requires a special care. The aim of this chapter is to provide a literature review regarding this topic. The different layers constituting the whole control are presented, explained and discussed. Given that there are so many possibilities of MMC control structures, the considered control in this thesis will end this chapter.

2. MMC Control principle

In order to manage the exchanged powers between AC and DC grids through the MMC, it is necessary to develop a control system which can insure this purpose. However, in reality, the MMC control mission is to communicate the SMs configuration by sending the pulse signals for SM switches. It means that, the control objectives have to be transferred by the control system to a given arm configuration. To do so, two steps are necessary to calculate the corresponding pulse signals (see Figure III-1):

- First, a controller has to calculate the modulated voltage inserted by each arm according to the requested powers. This control layer is called "**High Level Control**".
- Then, another controller has to select the inserted and bypassed SMs in order to satisfy the requested voltage. This control is known as "**Low Level Control**".

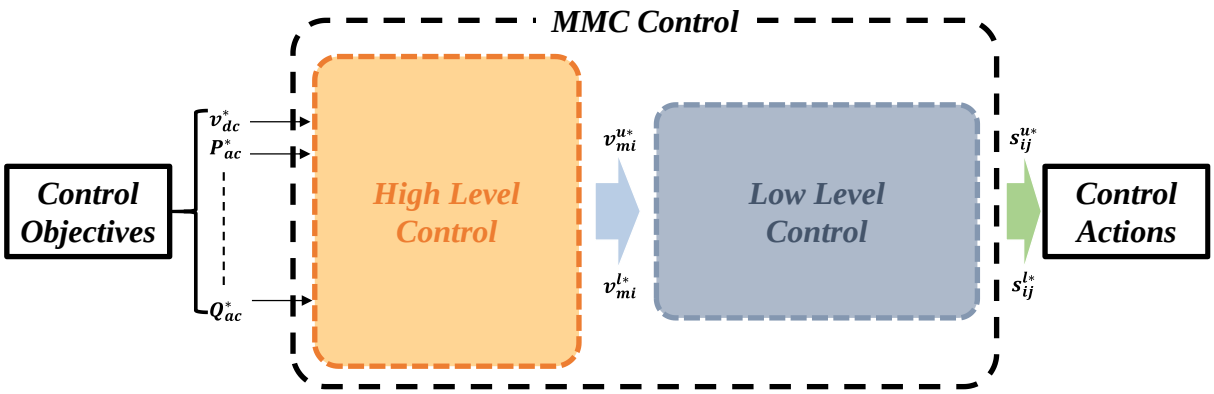

Figure III-1: General scheme of MMC control.

3. Low level control

The goal of this control is to generate arm voltages as requested by the high level control and ensure a balance of energy between the different SMs. For this purposes, the low level control will generate the IGBT control signals to select the appropriate SMs to be inserted in a manner to balance their voltages. The schematic diagram of low level MMC control can be separated in two distinguished parts as it is presented in Figure III-2.

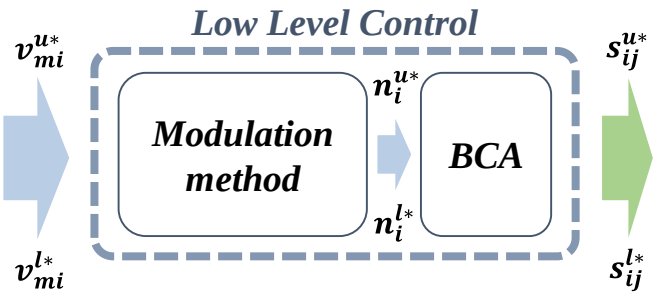

Figure III-2: Architecture of low level control.

3.1. Modulation technique

The aim of this bloc is to determine the number of SMs to be inserted according to the voltage references provided by the higher control layer (see Figure III-2). Two steps are necessary for this purpose:

- First, calculation of modulation indexes.
- Then, calculation of number of inserted SMs.

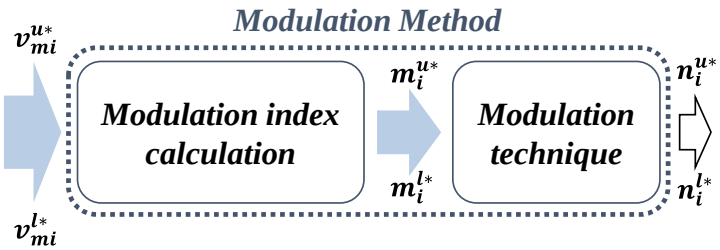

Figure III-3: Modulation method diagram.

3.1.1. Modulation index calculation

The objective of this bloc is to calculate the modulation indexes corresponding to the ratio between the inserted and the available SMs within one arm. Two approaches can be used to calculate the modulation indexes which are:

3.1.1.1. Direct modulation

When the direct modulation approach is used, the modulation indexes are calculated based on DC voltage value as for standard VSCs [23].

$$m_i^{u*} = \frac{v_{mi}^{u*}}{v_{dc}}$$
$$m_i^{l*} = \frac{v_{mi}^{l*}}{v_{dc}} \qquad \textit{(III-1)}$$

3.1.1.2. Indirect modulation

This modulation approach is based on the available total voltage for each arm. The modulation indexes are given by the following expressions.

$$m_i^{u*} = \frac{v_{mi}^{u*}}{v_{C\Sigma i}^{u}}$$
$$m_i^{l*} = \frac{v_{mi}^{l*}}{v_{C\Sigma i}^{l}} \qquad \textit{(III-2)}$$

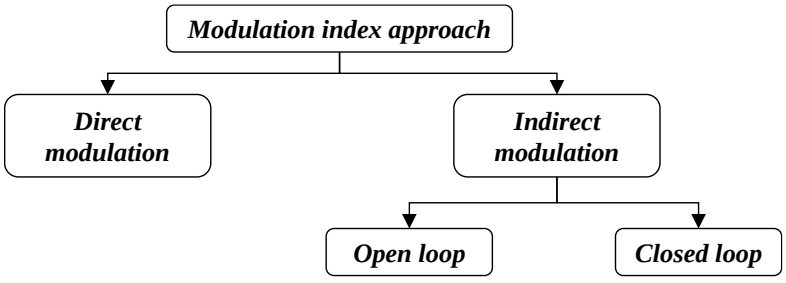

Figure III-4: Modulation index classification.

Two manners can be used to obtain the available total voltage in the arms. They can be measured and sent to the control system as a feedback signals, in this case, the modulation

approach will be considered as a closed loop modulation [66]. An open loop modulation can be obtained by using some estimation or prediction models for available arm voltages [67, 68].

The modulation index approach is a critical point in the overall MMC control since it changes the high level control architecture as well as the internal dynamics of MMC. This point will be covered when the high level part is addressed.

3.1.2. Modulation techniques

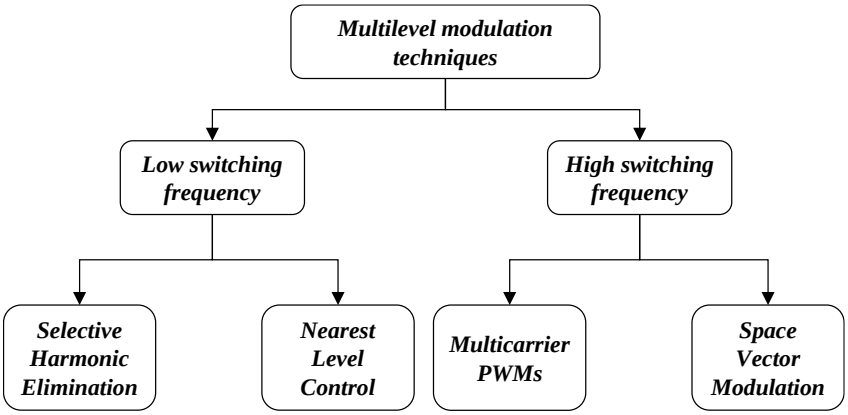

Figure III-5: Multilevel modulation classification.

For a normal operation, the obtained modulation index takes a sinewave signal varying between 0 and 1. Through a specific modulation method, they are transferred to a number corresponding to the inserted SMs (see Figure III-3). In general, the modulation techniques used for multilevel inverters such as MMC are usually an extension of the standard VSC modulations. According to their operation switching frequency, they can be classified to: high switching frequency modulations and low (fundamental) switching frequency modulations.

- When high switching frequency modulations are used, the converter introduce several commutations per cycle. It includes Multicarrier Pulse-Width Modulations (PWM), Space Vector Modulation (SVM)…
- Contrary to the first category, the low switching frequency modulations introduce only few commutations per cycle. For example: Selective Harmonic Elimination (SHE), Nearest Voltage Control (NLC)…

For HVDC application, when the losses are the most important selective factor, low-frequency modulation techniques are preferred due to the reduction of switching losses. Therefore, next, only these methods are explained and used for thesis contribution validations.

3.1.2.1. Multilevel Selective Harmonic Elimination (SHE)

The Selective Harmonic Elimination (SHE) method has been firstly introduced by [69] for 2-level VSC and extended to multilevel converters such as MMC by [70]. It has a theoretical potential tight control of the low order harmonics and work with low switching frequencies by using a programmed waveform reference.

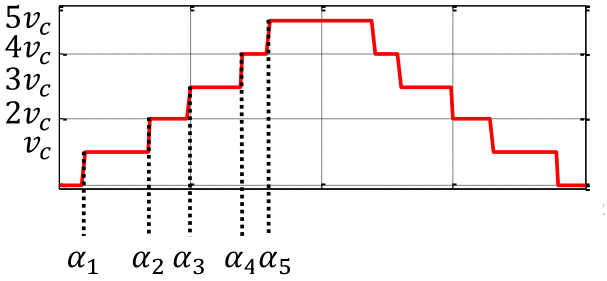

Figure III-6: Modulated arm voltage using SHE modulation technique.

Figure III-6 shows the inserted arm voltage for six levels MMC. The equation describing the inserted voltage can be expressed as Fourier series by the following equation:

$$v_m(wt) = \sum_{n=1}^{\infty} b_n \ sin(nwt)$$

$$b_n = \frac{4v_C}{n\pi}\left[\sum_{i=1}^{5} cos(n\alpha_i)\right] \qquad \textit{(III-3)}$$

Where:

n : The odd harmonic order.

By controlling the switching angles ($\alpha_1, \alpha_2 \ldots \alpha_5$), the fundamental output voltage as well as harmonics can be mastered. The number of harmonics that can be eliminate depends on the MMC level. For example, four harmonics (5^{th}, 7^{th}, 11^{th}, and 13^{th}) can be eliminated by controlling the switching angles of Figure III-6.

It has been proved in [70] that, in order to eliminate n harmonics, $n+1$ equations have to be solved. Generally, iteration methods such as Newton-Raphson and genetic algorithms are used to solve the nonlinear equations of (III-3). Once the switching angles are obtained, they are implemented and stored in a table in order to be interpolated according to the operating conditions. In case of HVDC, when the MMC includes numerous SMs, the application of SHE method is relatively complicated due to the high number of equations that should be solved and stored.

3.1.2.2. Nearest level control (NLC)

The principle of Nearest Level Control (NLC) method is based on finding the number of inserted SMs that can generate the closest voltage to the desired reference [71]. This method uses an assumption that the dispersion of SM voltages is low. Once the modulation references are received, they are multiplied by the number of available SMs N in order to get their corresponding inserted number $n_i^{u,l*}$. Thanks to the round function, only the nearest integer of the inserted numbers $n_i^{u,l*}$ will be considered (e.g., round of 2.6 = 3, round of 2.4 = 2). Consequently, the output signals take a staircase waveform as it is shown in Figure III-7.

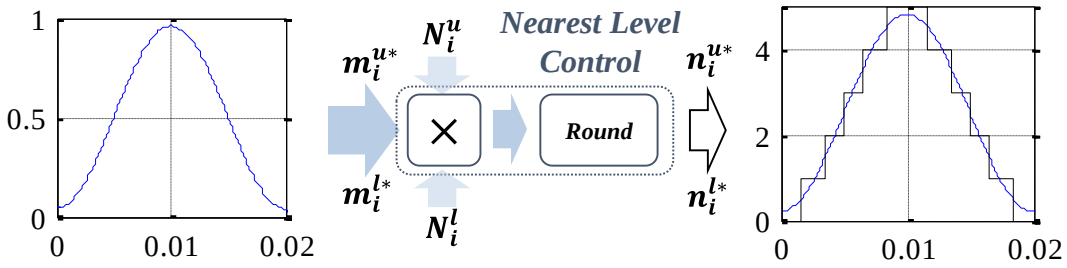

Figure III-7: Nearest level modulation scheme.

Thanks to the conceptual and implementation simplicity of NLC method, it will be used in this thesis for control algorithms validation: offline simulations, Hardware in the Loop (HIL) and experimental tests.

3.2. Balancing Control Algorithm (BCA)

The aim of this control algorithm is to choose the best arm configuration in order to maintain the voltages balanced between SM capacitors within one arm [72] . As it was introduced in CHAPTER I (see section 5.1), depending on the current flowing through the SMs and the switches state, the voltage across the SM capacitor v_C increases, decreases or stays constant.

So, without such controller, some SMs will be solicited more than others leading to charge some and discharge others. To overcome this problem, a controller called "Balancing Control Algorithm (BCA)" has to ensure that the powers flowing into/from different SMs are quite equal [73].

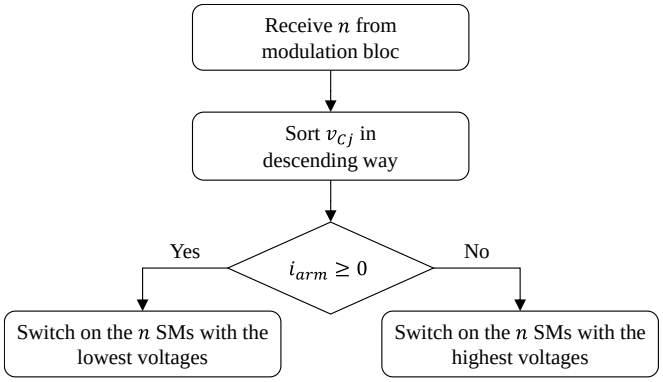

Figure III-8: Basic BCA flowchart.

The first (typical) BCA for MMC, so-called "Basic BCA", was introduced by [23]. At each BCA cycle, the SM capacitor voltages within one arm are measured, listed and sorted in descending order, and the number of SMs to be switched on n is received. If the arm current is positive or zero, the SMs with the lowest capacitor voltages will be switched on, otherwise, the highest capacitor voltages will be connected (see Figure III-8).

3.3. Classification of different BCAs

Four important factors and variables are impacted and/or impacting BCAs. They are: averaged switching frequency of SMs, operational point (P, Q), voltage ripple and voltage tolerance.

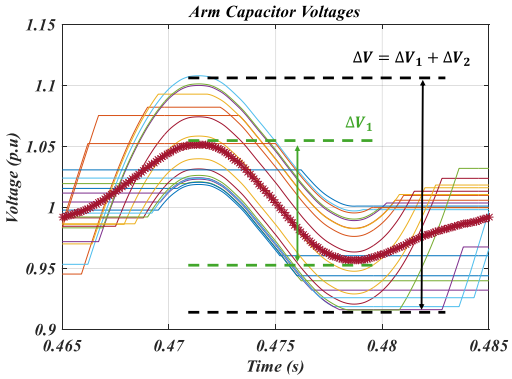

Figure III-9: Voltage ripple $\Delta V = \Delta V_1 + \Delta V_2$, average ripple ΔV_1 and voltage tolerance ΔV_2.

The averaged switching frequency is referred to the activation and deactivation of each SM. The operation point (P, Q) is corresponding to the transferred powers through the converter. The voltage ripple, voltage tolerance and natural ripple are explained in Figure III-9.

In [74], the authors have demonstrated that the circulating current which can be controlled with the high level control is highly coupled with the voltage ripple. Even those injected currents can reduce the average ripple on one hand, they increase the rms value of arm currents on the other hand. Consequently, reducing the ripple using the circulating current can be applied for some emergency situation however it is not the best solution since the conducting losses are directly affected.

A perfect BCA is an algorithm that can, reduce the switching frequency (less than 100 Hz), reduce the ripple voltage (<10 %) and eliminate the voltage tolerance between SMs for a maximum operation point $(P, Q)_{max}$. However, this algorithm does not exist since all these parameters are coupled. Each algorithm tries to minimize one parameter without much affecting the others. Following this philosophy, the BCA can be considered as a bloc where its inputs are the imposed parameters (according to algorithm objectives) and the outputs will be the impacted parameters (see Figure III-10).

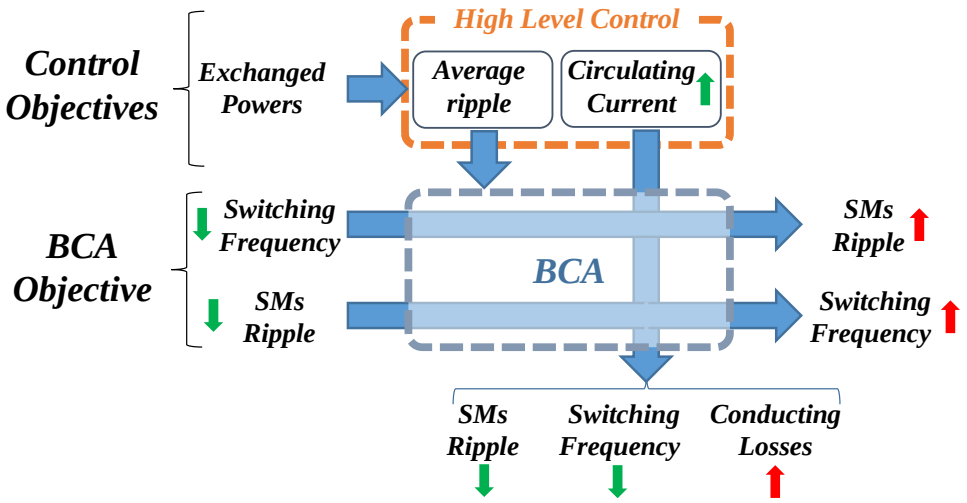

Figure III-10: Criteria and choices of balancing control algorithms.

Without considering explicitly the operating point (P, Q) and circulation current injection ($i_{cir} \approx 0$), it is proposed to classify BCAs in two categories (see Figure III-11): **BCAs with frequency mitigation and BCAs with voltage ripple mitigation [75].**

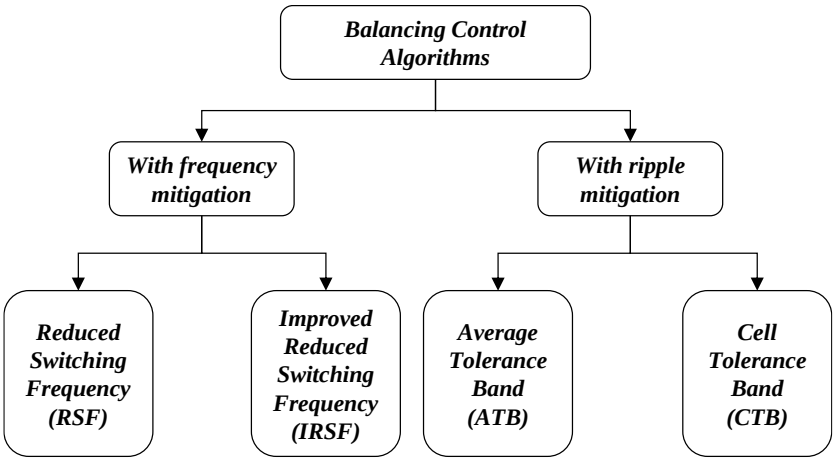

Figure III-11: Balancing control algorithms classification.

3.3.1. BCAs with frequency mitigation

The goal of these methods is to minimize the switching frequency. They depend only on the operating point of the MMC and the voltage ripple will be considered as a consequence. The main BCAs with frequency mitigation presented in the literature are:

3.3.1.1. Reduced Switching Frequency (RSF)

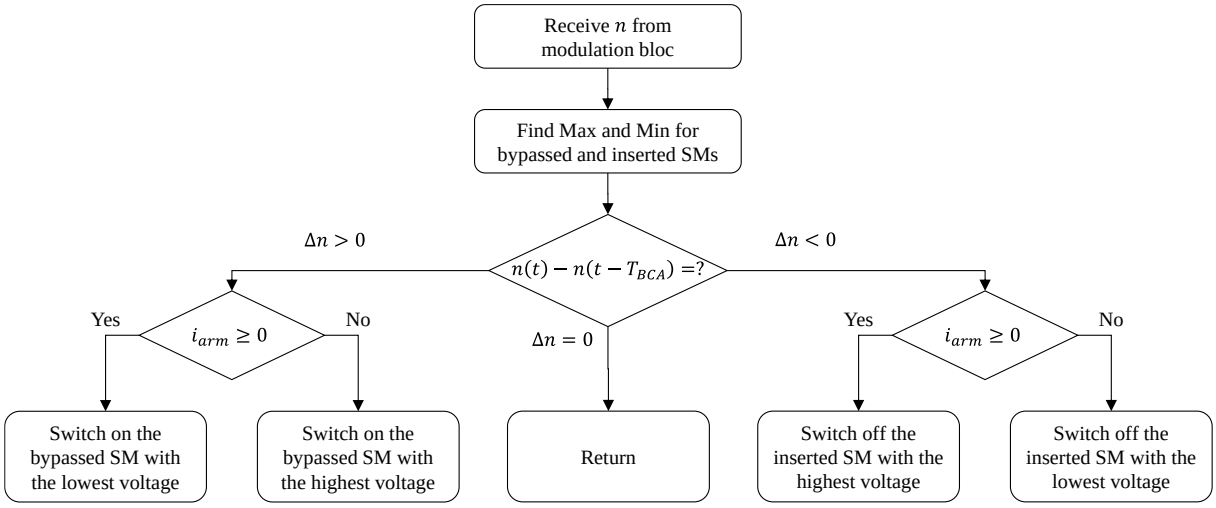

Figure III-12: Reduced switching frequency algorithm flowchart.

This technique reduces the switching frequency by changing the state of one SM each BCA cycle [76]. To do so, the algorithm distinguishes between inserted SMs and bypassed ones. By using MAX and MIN functions, the algorithm determines the maximum and minimum voltages for both inserted and bypassed SMs. Each BCA period, the difference between the new number of inserted SMs and the previous one (obtained at the previous cycle) is calculated.

$$\Delta n = n(t) - n(t - T_{bca}) \qquad \textit{(III-4)}$$

The algorithm chooses which SM has to be inserted or bypassed according to the algorithm presented in Figure III-12. It should be pointed out that the RSF method is not activated when $\Delta n = 0$.

3.3.1.2. Improved Reduced Switching Frequency (IRSF)

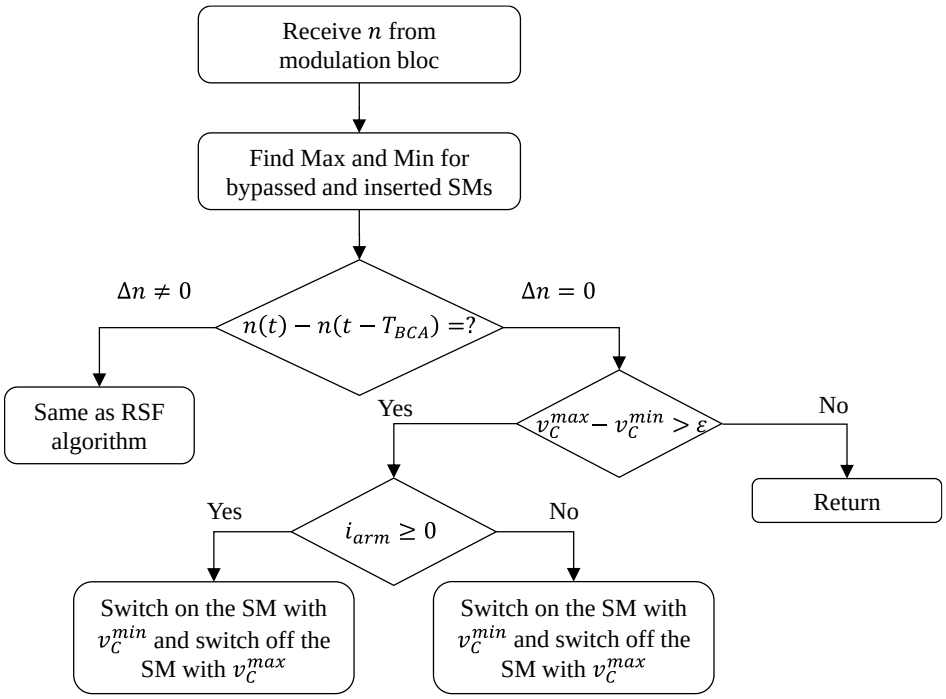

Figure III-13: Improved reduced switching frequency algorithm flowchart.

The principle of IRSF method is identical to the previous one (RSF) except when $\Delta n = 0$. For this case, the BCA permutes between one activated and one bypassed SMs when some conditions are satisfied [77]. When the voltage ripple becomes higher than the excepted one and according to the current direction, the BCA permutes between the MAX and the MIN of bypassed and activated SMs (see Figure III-13). The aim of this new case is to have a better balancing between SM and to reduce (not control) the voltage ripple.

3.3.2. BCAs with ripple mitigation

In this BCA category, the voltage ripple is mastered in order to reduce its value. For this purpose, an additional input which is a tolerance parameter is used in order to increase or decrease voltage ripple. By choosing an appropriate value for tolerance parameter, it provides a relatively low switching frequency and maintains an adequate fluctuation of SM voltages.

3.3.2.1. Average Tolerance Band (ATBsort)

It was introduced by [78], its corresponding flowchart is illustrated in Figure III-14. Compared with the basic BCA method, the manner how the sorting of SM voltages is made constitutes the main difference. Thanks to the tolerance parameter around the mean value, the sorting algorithm is activated only when it is necessary. This leads to a fluctuation of SM voltages without exceeding the limits set by the tolerance parameter.

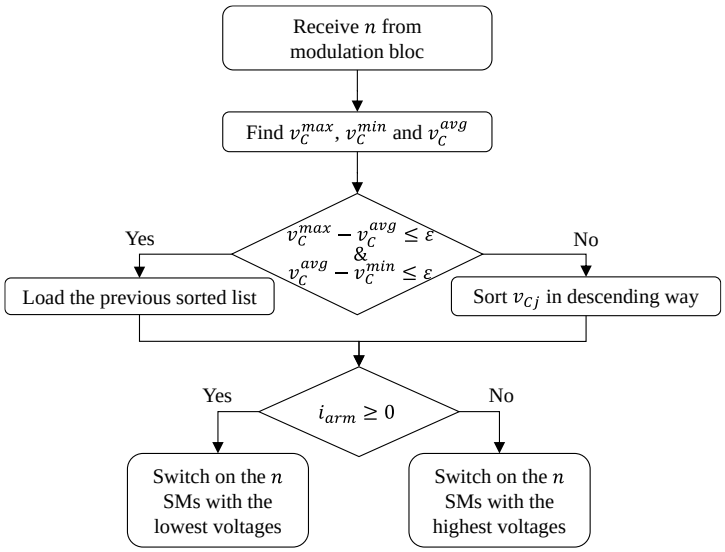

Figure III-14: Average tolerance band algorithm flowchart.

3.3.2.2. Cell Tolerance Band (CTBsort)

The principle which is very close to ATB method is presented in Figure III-15. The tolerance parameter is fixed around the nominal SM voltage (not the mean value as for ATB). At each BCA cycle, SM voltages are compared to $V_{min} = V_{Cn} - \varepsilon$ and $V_{max} = V_{Cn} + \varepsilon$. If one SM exceeds V_{max} or V_{min}, the sorting of SM voltages will be updated. If not, the algorithm keeps the previous one [78].

There is another Cell Tolerance Band which is based on sequential reversing, it uses a simple balancing approach rather than sorting method. However it has been demonstrated in [78] that, in some cases, the imposed tolerance band is not performed by this BCA.

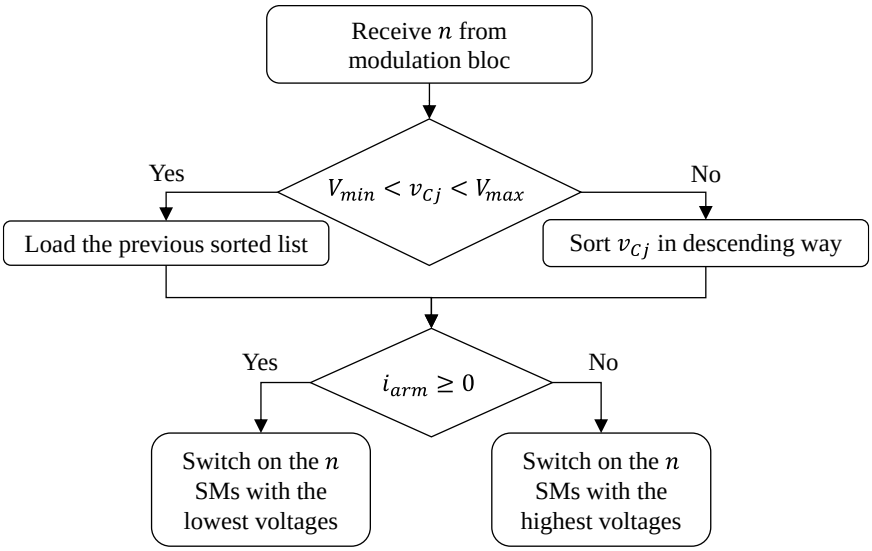

Figure III-15: Cell tolerance band algorithm flowchart.

3.4. Comparison

To evaluate and compare different BCAs presented in the previous section, some simulations with test cases are carried out. The detailed model based on semi analytical implementation is used to perform this comparison. The simulation time-step is set to 5 µs where the BCA sampling period is set to 100 µs in order to be in line with industrial system. The MMC parameters are the same as the used in CHAPTER II for models validation (see Table II-6) reduced to 20 SMs in order to well analyze the results. To perform such simulation, a high level control is needed. To do so, an energy based control is employed to generate the requested modulated arm voltages (it will be explained in the next of this chapter). For different transferred power values, the associated switching frequency and the voltage ripple (peak to peak) are calculated.

3.4.1. Basic BCA

The SM voltages for one arm are presented in Figure III-16. The results show that the SM voltages have almost same shape meaning that the energy is well balanced between the SMs. The associated switching frequency variation and the voltage ripple variations are shown in Figure III-17-(a) and Figure III-17-(b) respectively for different power transfer setpoints. It is observed that the ripple variation is linear regarding the transferred power where the switching frequency doesn't change.

Table III-1: Simulation results for discussed BCA methods with 1 pu power exchange.

BCA Methods		***Basic BCA***	***RSF***	***IRSF***	***ATB***
Ripple for the worst individual submodule (peak to peak) (%)		*9.65*	*40*	*22*	*17.3*
Switching frequency (Hz)	***mean***	*974*	*56*	*71*	*185*
	max	*983*	*67*	*80*	*215*
	min	*968*	*53*	*68*	*173*
Sorting frequency (Hz)		*Each BCA cycle (10kHz)*	*Max and Min Each BCA cycle (10kHz)*	*Max and Min Each BCA cycle (10kHz)*	*200*

The main drawback of this method is that the latter depends only on the BCA cycle frequency. Since the previous state is not taken into consideration, the BCA introduces several additional switches in order to have a perfect balance between SMs.

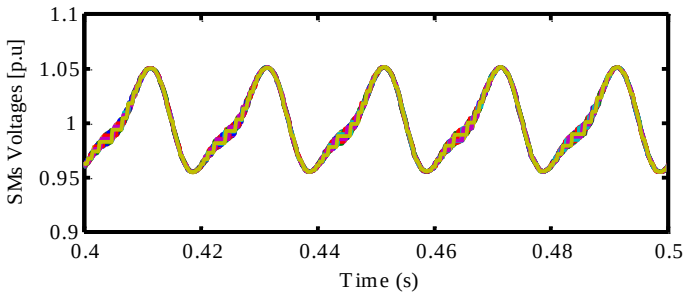

Figure III-16: SM voltages using Basic BCA with 1 pu transferred power.

Another inconvenient is the sorting technique which needs $N * log(N)$ iterations, it creates a big challenge for industrial applications (computational abilities, FPGA memory, data communication delay…). For this purpose, some optimized sorting algorithms such as the Bitonic sorting which is presented in [79] to optimize the computation speed for example.

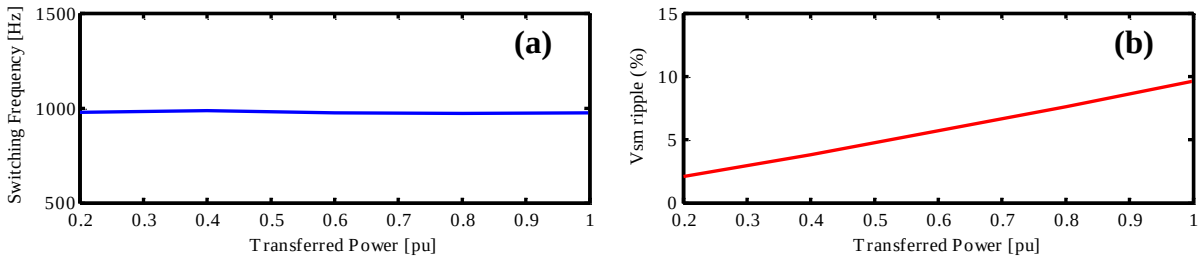

Figure III-17: (a) Switching frequency, (b) voltage ripple variations regarding transferred power level using Basic BCA.

3.4.2. Reduced Switching Frequency

According to the results presented in Figure III-18, this method operates the MMC with low switching frequency [50-60 Hz] leading to decrease the switching losses (see Figure III-19-(a)). Using MAX and MIN functions decreases also the constraints regarding the computational time for FPGA. On the other hand, the SM voltages are not perfectly balanced and the voltage ripple is four times higher than obtained for Basic BCA. It can cause insulated problem for IGBTs, increase the losses in SM capacitors and reduce the life time of the SMs (see Figure III-19-(b)).

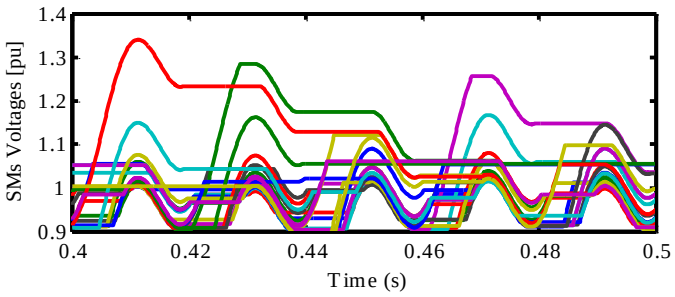

Figure III-18: SM voltages using RSF-algorithm with 1 pu transferred power.

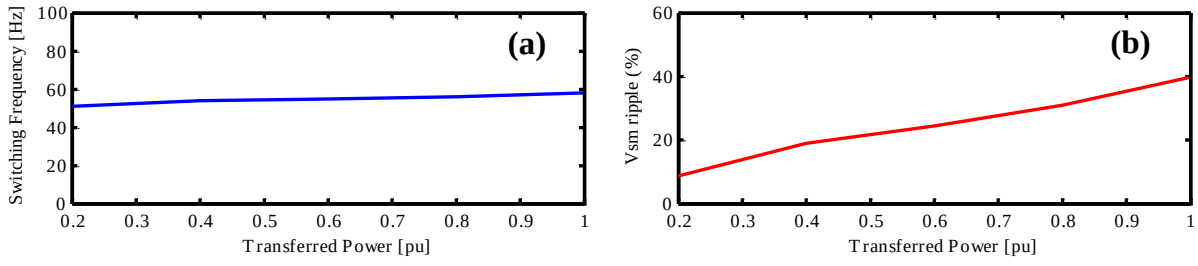

Figure III-19: (a) Switching frequency, (b) voltage ripple variations regarding transferred power level using RSF-algorithm.

3.4.3. Improved Reduced Switching Frequency

Switching between two SMs when $\Delta n = 0$ improves the quality of the voltage balancing (see Figure III-20). From Figure III-21-(a) it can be seen that this method has the same variation as the previous one in term of switching frequency when the transferred power is lower. The advantage of this method can be observed when the transferred power increases. Thanks to $\Delta N_{ON} = 0$ case, the ripple is decreased (see Figure III-21-(b)) to the half and the MMC is still working with low switching frequency $70\ Hz$.

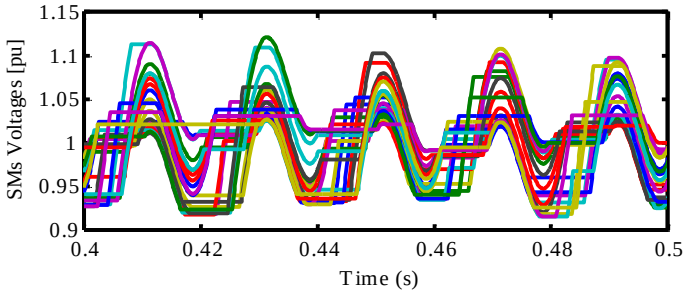

Figure III-20: SM voltages using IRSF algorithm with 1 pu transferred power.

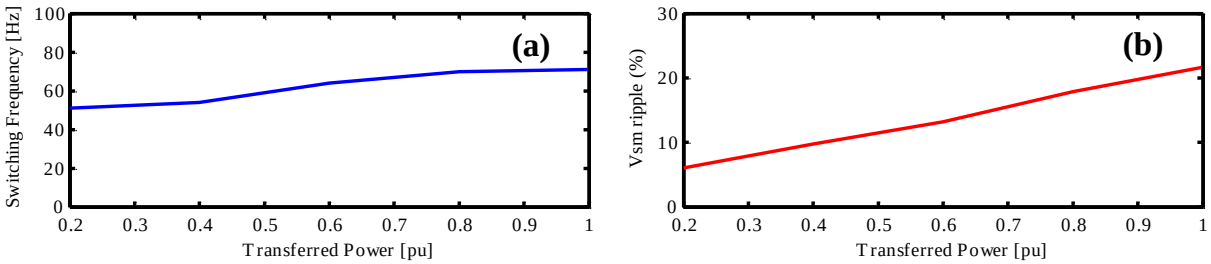

Figure III-21: (a) Switching frequency, (b) voltage ripple variations regarding transferred power level using IRSF algorithm.

3.4.4. Average Tolerance Band (Sorts)

The SM voltages for one arm and the variation of switching frequency with SMs ripple for different power levels are presented in Figure III-22 and Figure III-23 respectively. Those results have been obtained with tolerance parameter $\varepsilon = \mp 5\%$. Contrary to CTB method which allows to maintain the SMs voltages with the limits set by the tolerance parameter, the obtained ripple with ATB method depends on the transferred power. This difference can be attributed to the fact that the limits (V_{min} and V_{max}) are not calculated in the same manner for same tolerance parameter value. For this reason, the ATB method has to be improved in order to well control the voltage ripple.

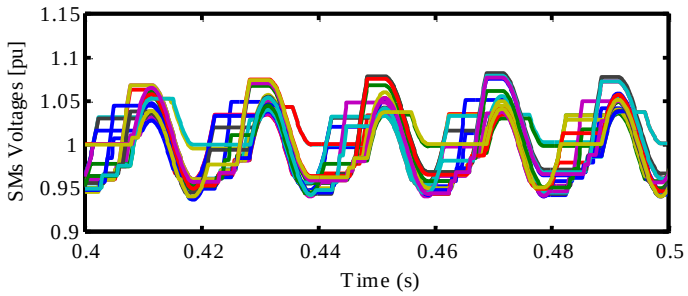

Figure III-22: SM voltages using ATB algorithm with 1 pu transferred power.

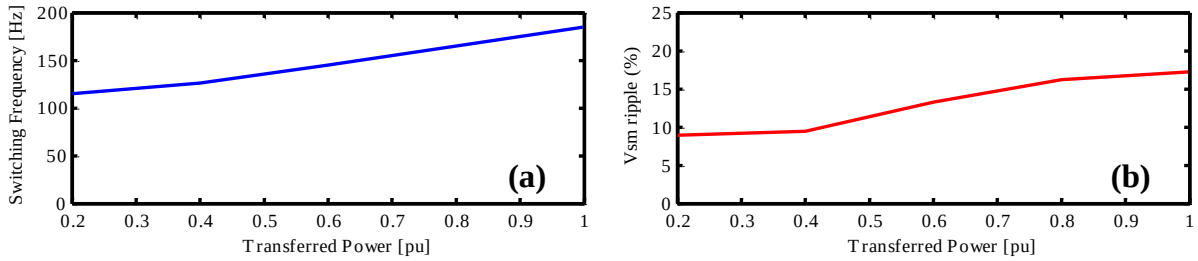

Figure III-23: (a) Switching frequency, (b) voltage ripple variations regarding transferred power level using ATB algorithm.

4. High level control

The goal of this control level is to provide voltage references for each arm to low level control according to control objectives and MMC operation mode (see Figure III-1). In general, this layer includes different control loops dedicated to manage the power exchange inside the MMC (i.e. AC and DC powers). To derive the control laws, it is necessary to exploit the MMC topology in order to obtain state-space equations describing MMC state variables.

4.1. State-space equations for MMC

As a reminder, in HVDC applications, where the MMC requires a high number of SMs (up to hundreds), analyzing each SM separately will become very complicated especially for control law synthesis. To avoid such complexity, it is recommended to use the reduced order averaged arm model for this purpose (see CHAPTER II, section 3.3)

Since the analysis in the three phases is the same, the MMC model can be reduced to one leg as it is shown in Figure III-24.

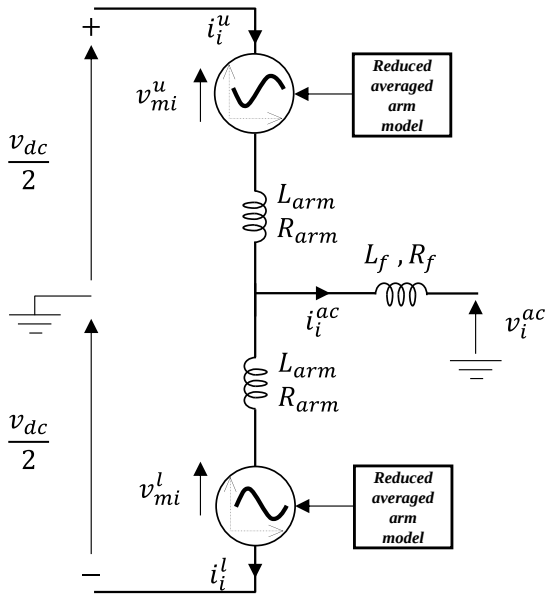

Figure III-24: Simplified circuit for one MMC leg.

By applying Kirchhoff's voltage law to Figure III-24, two voltage loops can be considered as it is duplicated in Figure III-25: one for the upper arm (green loop) and one for the lower part (yellow loop). Their associated equations can be written as:

$$\frac{v_{dc}}{2} - v_{mi}^{u} - L_{arm}\frac{di_i^u}{dt} - R_{arm}\, i_i^u = v_i^{ac} + R_f\, i_i^{ac} + L_f\frac{di_i^{ac}}{dt}$$
$$-\frac{v_{dc}}{2} + v_{mi}^{l} + L_{arm}\frac{di_i^l}{dt} + R_{arm}\, i_i^l = v_i^{ac} + R_f\, i_i^{ac} + L_f\frac{di_i^{ac}}{dt} \qquad \textit{(III-5)}$$

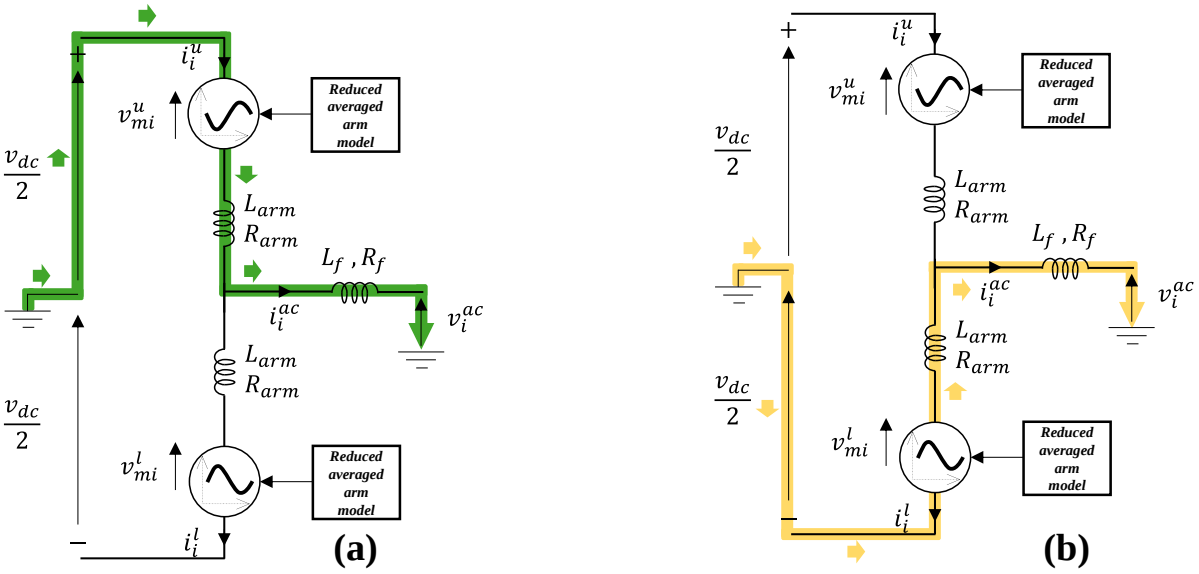

Figure III-25: Upper and lower voltage loops.

Regarding the chosen AC current direction, it can be expressed as a subtraction of arm currents.

$$i_i^{ac} = i_i^u - i_i^l \qquad \textit{(III-6)}$$

Then, the equations (III-5) can be written in form of matrix as follow.

$$\begin{bmatrix} -(L_{arm}+L_f) & L_f \\ -L_f & (L_{arm}+L_f) \end{bmatrix} \begin{bmatrix} \frac{di_i^u}{dt} \\ \frac{di_i^l}{dt} \end{bmatrix} = \begin{bmatrix} (R_{arm}+R) & -R \\ R & -(R_{arm}+R_f) \end{bmatrix} \begin{bmatrix} i_i^u \\ i_i^l \end{bmatrix} + \begin{bmatrix} v_{mi}^u \\ v_{mi}^l \end{bmatrix} + \begin{bmatrix} -\frac{v_{dc}}{2} + v_i^{ac} \\ \frac{v_{dc}}{2} + v_i^{ac} \end{bmatrix} \qquad \textit{(III-7)}$$

Arranging equations (III-7) leads to obtain the state-space equations for arm currents (see equations (III-8)).

$$\begin{bmatrix} \frac{di_i^u}{dt} \\ \frac{di_i^l}{dt} \end{bmatrix} = E \begin{bmatrix} i_i^u \\ i_i^l \end{bmatrix} + J \begin{bmatrix} v_{mi}^u \\ v_{mi}^l \end{bmatrix} + J \begin{bmatrix} -\frac{v_{dc}}{2} + v_i^{ac} \\ \frac{v_{dc}}{2} + v_i^{ac} \end{bmatrix} \qquad \textit{(III-8)}$$

Where:

$$E = \begin{bmatrix} -(L_{arm} + L_f) & L_f \\ -L_f & (L_{arm} + L_f) \end{bmatrix}^{-1} \begin{bmatrix} (R_{arm} + R) & -R \\ R & -(R_{arm} + R_f) \end{bmatrix}$$

$$J = \begin{bmatrix} -(L_{arm} + L_f) & L_f \\ -L_f & (L_{arm} + L_f) \end{bmatrix}^{-1}$$

4.1.1. AC power equation

The model given in equations (III-8) offers the possibility to derive the control laws for arm currents by controlling the values of v_{mi}^u and v_{mi}^l (input vector). However, in order to understand the behavior of MMC regarding the connected grids (AC and DC grids), it is recommended to derive dedicated models where the AC and DC currents constitute their state variables. This allows obtaining an explicit relationship between the control objectives and controlled variables. To do so, some mathematical approaches are applied to model (III-5).

Summing the upper and lower parts of the model (III-5) leads to obtain the following equation.

$$v_{mi}^l - v_{mi}^u + L_{arm}\left(\frac{di_i^l}{dt} - \frac{di_i^u}{dt}\right) + R_{arm}\left(i_i^l - i_i^u\right) = 2\left(v_i^{ac} + R_f\, i_i^{ac} + L_f \frac{di_i^{ac}}{dt}\right) \qquad \textit{(III-9)}$$

Taking into account equation (III-6) and dividing the equation (III-9) in two lead to obtain the following equation.

$$\frac{v_{mi}^l - v_{mi}^u}{2} - v_i^{ac} = \left(R_f + \frac{R_{arm}}{2}\right) i_i^{ac} + \left(L_f + \frac{L_{arm}}{2}\right)\frac{di_i^{ac}}{dt} \qquad \textit{(III-10)}$$

The equation (III-10) can be represented with the following equivalent circuit (see Figure III-26), it illustrates how the MMC looks like from the standpoint of AC grid.

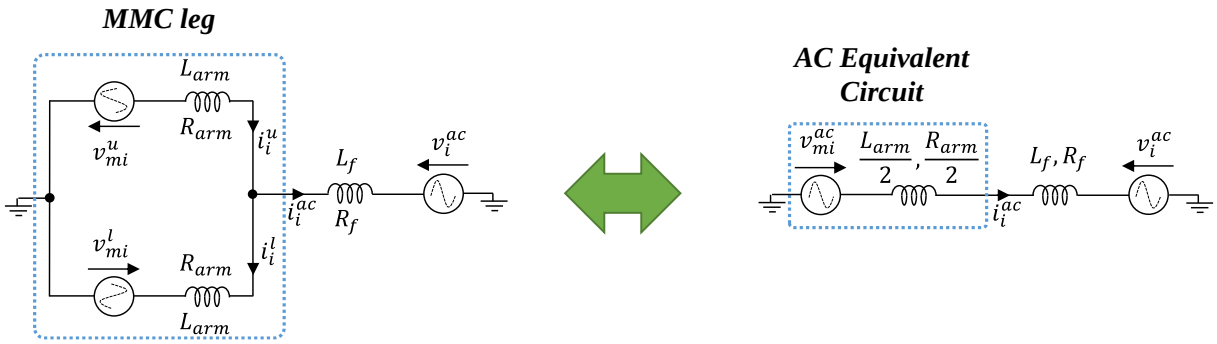

Figure III-26: MMC equivalent circuit from AC standpoint.

It can be concluded from Figure III-26 that, the half of the difference between the lower and upper arm voltages creates a modulated AC voltage v_{mi}^{ac}. By controlling v_{mi}^{ac}, it is possible to control the exchanged powers (AC current i_i^{ac}) between the MMC and the AC grid. Like standard VSCs, the active and reactive powers can be mastered by controlling, respectively, the phase shift and amplitude of v_{mi}^{ac} compared to v_i^{ac}. The equation (III-10) can be arranged as follow:

$$v_{mi}^{ac} - v_i^{ac} = R_{eq}^{ac}\, i_i^{ac} + L_{eq}^{ac} \frac{di_i^{ac}}{dt} \qquad \textit{(III-11)}$$

Where:

$$v_{mi}^{ac} = \frac{v_{mi}^{l} - v_{mi}^{u}}{2}$$

$$R_{eq}^{ac} = R_f + \frac{R_{arm}}{2}$$

$$L_{eq}^{ac} = L_f + \frac{L_{arm}}{2}$$

4.1.2. DC power equation

On the other hand, subtracting the upper and lower parts of model (III-5) leads to obtain the following equation where all the AC components are eliminated. Its equivalent circuit is illustrated in Figure III-27.

$$v_{dc} - \left(v_{mi}^{u} + v_{mi}^{l}\right) - L_{arm} \frac{d}{dt}\left(i_i^{l} + i_i^{u}\right) + R_{arm}\left(i_i^{l} + i_i^{u}\right) = 0 \qquad \textit{(III-12)}$$

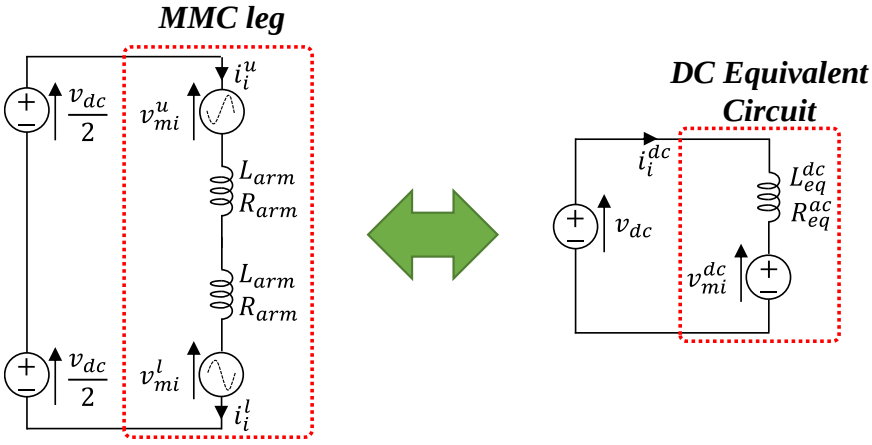

Figure III-27: MMC equivalent circuit from DC standpoint.

It can be observed that, according to the chosen direction for arm currents, the sum of arm currents is a current which flows between the MMC leg and DC grid (DC component). Equation (III-12) can be arranged as follow by introducing new variables.

$$v_{dc} - v_{mi}^{dc} = R_{eq}^{dc}\, i_i^{dc} + L_{eq}^{dc} \frac{di_i^{dc}}{dt} \qquad \textit{(III-13)}$$

Where:

$$v_{mi}^{dc} = v_{mi}^{u} + v_{mi}^{l}$$

$$i_i^{dc} = \frac{i_i^{l} + i_i^{u}}{2}$$

$$R_{eq}^{dc} = 2\, R_{arm}$$

$$L_{eq}^{dc} = 2\, L_{arm}$$

Equation (III-13) shows how the MMC behaves from the standpoint of DC grid. By controlling the modulated DC voltage v_{mi}^{dc} created by the MMC, the exchanged power between the MMC and the DC grid (DC current i_i^{dc}) can be mastered.

4.1.3. Energy global equation

Equations (III-11) and (III-13) show that, unlike standard VSCs, the AC and DC currents can be controlled independently using MMC. The difference between input and output powers appears as variation of the stored energy inside the MMC (see Figure III-28).

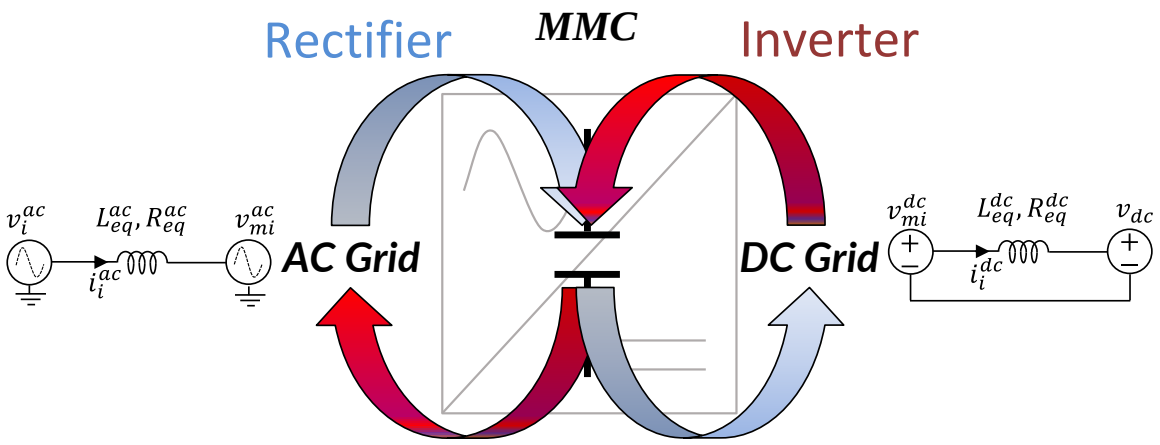

Figure III-28: Power exchange inside the MMC.

$$\frac{dW_{mmc}}{dt} = P_{dc} - P_{ac} - P_{loss} \qquad \textit{(III-14)}$$

The global energy is defined by the following expression:

$$W_{mmc} = \sum_{i=a}^{C} W_i^u + W_i^l \qquad \textit{(III-15)}$$

Where:

$W_i^{u,l}$: is the available energy in one arm (sum of all SMs energy within one arm).

Hence, since the MMC requires energy to operate properly, it is mandatory to have a controller to regulate the stored energy. Its objective is to ensure that the global energy stored inside the MMC allows operating the MMC in a good operation conditions. According to equation (III-14), this objective can be performed either by bringing power from AC grid or from DC side.

4.1.4. Energy balancing equations

Based on equation (III-15), it is obvious that controlling the global energy (W_{mmc}) is not a sufficient condition to ensure a good operation since the energy arms are not directly controlled. An unbalanced condition of stored energy between the arms can take place without being seen by the global energy controller (see Figure III-29). To solve this issue, it is necessary to derive

other controllers that can ensure a balanced energy sharing between the arms. To derive these controllers, the arm energy variation must be analyzed to obtain their state-space equations.

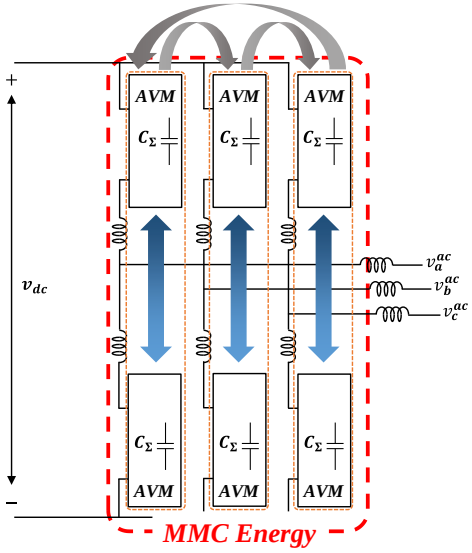

Figure III-29: Distribution of stored energy in the MMC.

The variation of stored energy in arms can be expressed by:

$$W_i^u = \frac{1}{2} C_{\Sigma i}^u (v_{C\Sigma i}^u)^2 = \int P_{mi}^u$$
$$W_i^l = \frac{1}{2} C_{\Sigma i}^l (v_{C\Sigma i}^l)^2 = \int P_{mi}^l \qquad \textit{(III-16)}$$

The exchanged power by the arm capacitors can be written as follow:

$$P_{mi}^u = v_{mi}^u \, i_i^u$$
$$P_{mi}^l = v_{mi}^l \, i_i^l \qquad \textit{(III-17)}$$

Equations (III-17) can be expressed using AC and DC components. That is:

$$P_{mi}^u = \left(\frac{v_{mi}^{dc}}{2} - v_{mi}^{ac}\right)\left(i_i^{dc} + \frac{i_i^{ac}}{2}\right) = \frac{v_{mi}^{dc}}{2} i_i^{dc} - v_{mi}^{ac} \frac{i_i^{ac}}{2} - v_{mi}^{ac} i_i^{dc} + \frac{v_{mi}^{dc}}{2} \frac{i_i^{ac}}{2}$$

$$P_{mi}^l = v_{mi}^l \, i_i^l = \left(\frac{v_{mi}^{dc}}{2} + v_{mi}^{ac}\right)\left(i_i^{dc} - \frac{i_i^{ac}}{2}\right) \qquad \textit{(III-18)}$$
$$= \frac{v_{mi}^{dc}}{2} i_i^{dc} - v_{mi}^{ac} \frac{i_i^{ac}}{2} + v_{mi}^{ac} i_i^{dc} - \frac{v_{mi}^{dc}}{2} \frac{i_i^{ac}}{2}$$

In one period, the average energy exchange in the arms are calculated as follow:

$$\langle \Delta W_i^u \rangle = \int_0^{2\pi} P_{mi}^u = \int_0^{2\pi} \frac{v_{mi}^{dc}}{2}\, i_i^{dc} - v_{mi}^{ac}\, \frac{i_i^{ac}}{2} - v_{mi}^{ac}\, i_i^{dc} + \frac{v_{mi}^{dc}}{2}\, \frac{i_i^{ac}}{2}$$
$$\langle \Delta W_i^l \rangle = \int_0^{2\pi} P_{mi}^l = \int_0^{2\pi} \frac{v_{mi}^{dc}}{2}\, i_i^{dc} - v_{mi}^{ac}\, \frac{i_i^{ac}}{2} + v_{mi}^{ac}\, i_i^{dc} - \frac{v_{mi}^{dc}}{2}\, \frac{i_i^{ac}}{2} \qquad \textit{(III-19)}$$

Under steady state operation, v_{mi}^{dc} and i_i^{dc} have a constant value while v_{mi}^{ac} and i_i^{ac} have a sinusoidal waveform with same frequency. It can be concluded from equations (III-19) that, the averaged arms energy can be changed by creating unbalance between AC and DC powers (first two components) in one period. The two last components cannot change the average arms energy during one period, however, they introduce a ripple in the instantaneous upper and lower arms energy with opposite direction.

Based on equations (III-19), two new variables are introduced in order to simplify the energy balancing control:

- Energy per leg (sum) W_i^{Σ}: represents the sum of lower and upper arm energies within one leg. $(W_i^{\Sigma} = W_i^l + W_i^u)$.
- Energy diff W_i^{Δ}: represents the difference between the lower and upper arm energies within one leg. $(W_i^{\Delta} = W_i^l - W_i^u)$.

4.1.4.1. Energy leg (sum) equation

Adding P_i^u and P_i^l in (III-18) leads to obtain the instantaneous energy sum expression which can be written as follow:

$$W_i^{\Sigma} = W_i^l + W_i^u = \int P_{mi}^l + P_{mi}^u = v_{mi}^{dc}\, i_i^{dc} - v_{mi}^{ac}\, i_i^{ac} \qquad \textit{(III-20)}$$

The average energy sum variation in one period is given by

$$\langle \Delta W_i^{\Sigma} \rangle = \int_0^{2\pi} v_{mi}^{dc}\, i_i^{dc} - v_{mi}^{ac}\, i_i^{ac} = P_{mi}^{dc} - P_{mi}^{ac} \qquad \textit{(III-21)}$$

Equation (III-21) shows that it is possible to regulate/change the averaged value of energy in leg i by changing the AC or DC currents (i_i^{ac}or i_i^{dc}). Nevertheless, in order to avoid an unbalanced AC operation, it is better to choose the second solution based on controlling the DC current (i_i^{dc}).

4.1.4.2. Energy Difference equation

Substituting P_i^l and P_i^u in (III-18) yields the instantaneous energy difference equation.

$$W_i^{\Delta} = \int P_{mi}^l - P_{mi}^u = 2\, v_{mi}^{ac}\, i_i^{dc} - \frac{v_{mi}^{dc}}{2}\, i_i^{ac} \qquad \textit{(III-22)}$$

The average energy difference variation in one period can be expressed as follow.

$$\langle \Delta W_i^{\Delta} \rangle = \int_0^{2\pi} P_{mi}^l - P_{mi}^u = 2\, v_{mi}^{ac}\, i_i^{dc} - \frac{v_{mi}^{dc}}{2}\, i_i^{ac} \qquad \textit{(III-23)}$$

By setting the equation (III-23) to none zero value, it is possible to control the difference between the lower and upper arms energy. To do so, an alternative component of i_i^{dc} which is in phase with v_{mi}^{ac} is injected by energy difference controller. Hence, the first component of equations (III-23) becomes none zero leading to change/ regulate the energy difference between the arms.

Taking into account all the previous analysis, equations (III-11), (III-13), (III-14), (III-21) and (III-23) provide a generalized dynamic model of MMC which can be used for control purposes. The following table recalls and summarizes what has been developed above.

Table III-2: MMC state-space equations.

Control objectives	***State variables***	***Control inputs***	***State space equations***
AC powers	i_{ac}	$v_{mi}^{ac} = \frac{v_{mi}^{l} - v_{mi}^{u}}{2}$	$L_{eq}^{ac} \frac{di_i^{ac}}{dt} = -R_{eq}^{ac}\, i_i^{ac} + v_{mi}^{ac} - v_i^{ac}$
DC power	i_{dc}	$v_{mi}^{dc} = v_{mi}^{u} + v_{mi}^{l}$	$L_{eq}^{dc} \frac{di_i^{dc}}{dt} = -R_{eq}^{dc}\, i_i^{dc} - v_{mi}^{dc} + v_{dc}$
Energy global	W_{mmc}	i_{ac} *or* i_{dc} *(depending to the control strategy)*	$\frac{dW_{mmc}}{dt} = v_{dc} i_{dc} - \sum_{i=a}^{c} v_i^{ac} i_i^{ac}$
Energy Sum (leg)	W_i^{Σ}	i_i^{ac} *or* i_i^{dc} *(it is recommended to use* i_i^{dc} *in order to avoid unbalanced AC operation)*	$\frac{dW_i^{\Sigma}}{dt} = v_{mi}^{dc}\, i_i^{dc} - v_{mi}^{ac}\, i_i^{ac}$
Energy diff	W_i^{Δ}	i_i^{dc}	$\frac{dW_i^{\Delta}}{dt} = 2\, v_{mi}^{ac}\, i_i^{dc} - \frac{v_{mi}^{dc}}{2}\, i_i^{ac}$

4.2. High level control structure

Based on the control objectives presented in the previous section different control schemes can be used to build the high level control. They can be classified into two control schemes which are:

- ***Multivariable control.***
- ***Cascaded control.***

4.2.1. Multivariable control

The obtained control law is derived using a nonlinear multivariable model which integrates the considered state-space equations describing the MMC behavior (see Figure III-30). This approach requires some advanced control strategies in order to derive its associated control laws and perform stability analysis which is necessary to prove the system stability.

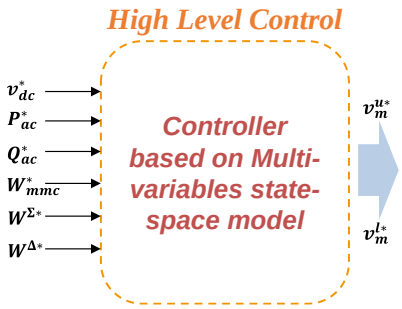

Figure III-30: Multivariable control diagram for MMC.

This approach has been applied to the MMC by [80, 81]. In [80], the authors propose a Periodic Linear Quadratic Regulator (PLQR) based on bilinear model which integrates currents, global energy and energy balancing models. Based on the same bilinear model, another controller based on Sum-Of-Squares (SOS) decomposition method has been presented in [81].

The advantage of using multivariable control approach is that, using only one controller, all the state variables are controlled simultaneous (same response time for all variables) which is not possible with other approaches. However, this approach presents several drawbacks such as:

- Stability matters since there is a strong coupling between the state variables. This is especially the case when the control is tested with a physical system (some elements are not integrated in the model).
- Some internal variables are not directly mastered.
- Complicate to debug when instabilities occur.

For all these reasons, only the cascaded control structure will be considered in this thesis.

4.2.2. Cascaded control

The second scheme which is based on time–scales decoupling assumptions, consists of a cascaded structure in which the control algorithm is built and tuned step by step taking into account the internal variable limits. Widely used among researchers [82, 83], this scheme is based on the decomposition of the system into interconnected subsystems and in which each control loop is associated with a response time. For example, when considering only two cascaded controllers (inner and outer loops) and taking into account the time-scales decoupling assumptions, the inner (or internal) loop response time must be set faster than the outer loop (see Figure III-31).

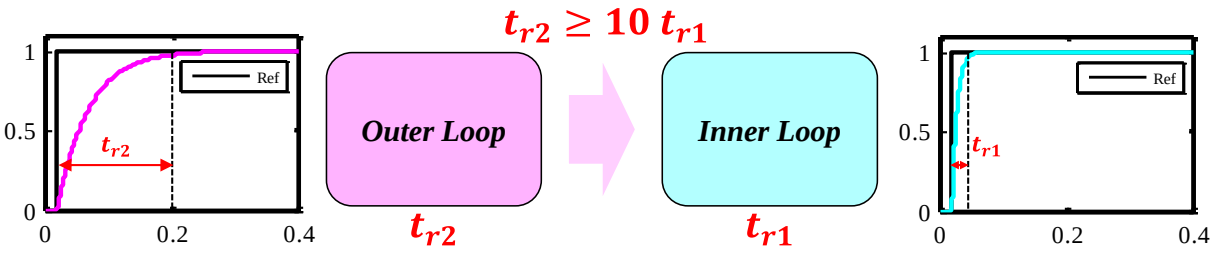

Figure III-31: Cascaded control principle.

The response time ratio between the two loops is not always easy to set, its limits can be often obtained from a rigorous stability analysis taking into account the whole control algorithm [84]. From a practical point of view, this ratio can be set to 10 in order to avoid any interference between the two loops regarding the stability.

The general diagram of MMC cascaded control is duplicated in Figure III-32. Depending to which controllers are considered and how there are connected, two controls schema can be obtained.

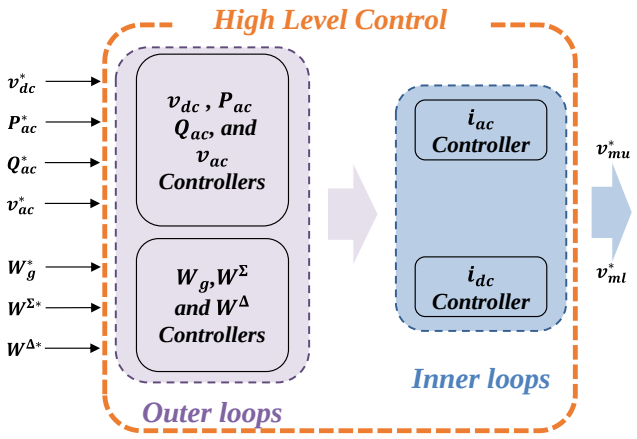

Figure III-32: Cascaded control scheme for MMC.

4.2.2.1. Non-energy based control

A basic control structure can be obtained by applying a standard VSCs control to the MMC. In the literature, this control schema is known as "Non-energy based control" [76], [52], [85], it allows to control the active power or DC voltage on one hand, and control the reactive power or AC voltage amplitude on the other hand. As it is shown in Figure III-33, the simplicity of this control constitutes its main advantage.

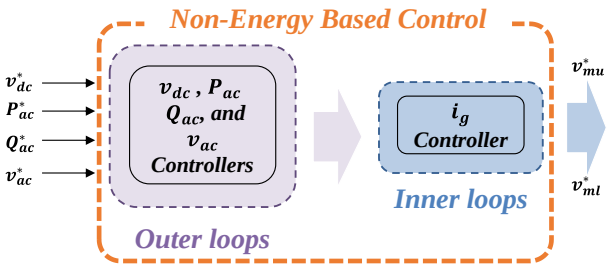

Figure III-33: Non-energy based control diagram.

According to MMC state space equations (see Table III-2), it has been demonstrate that, the stability of MMC control can be ensured by controlling the AC and DC currents (powers) as well as the stored energy. However, Figure III-33 shows that only the AC current is mastered when non-energy based control is used which is inconsistent with the previous analysis (see section 4.1.3).

In [66], it has been demonstrated that the stability of non-energy based control can be ensured only by using a direct modulation approach where the modulations indexes are calculated based on DC voltage measurement (see equation (III-1)). Since the inserted voltages in the physical system are based on the instantaneous arm voltages (see Figure III-34), a difference appears between the requested voltages (references) and the inserted ones leading to create uncontrolled DC current which flows between the DC grid and MMC. This current ensures a balanced power exchange between the AC and DC grids making the control stable.

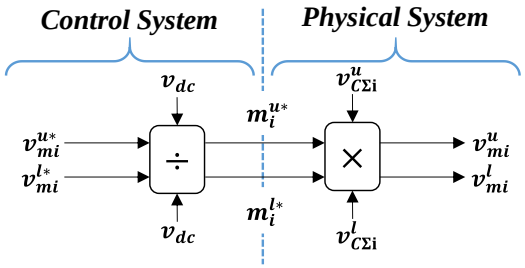

Figure III-34: Direct modulation indexes calculation.

Moreover, the voltage inequality between the legs generates some undesired currents, so-called "Circulating current", which flow between the arms in form of second harmonics. These currents increase the converter loss such conduction losses inside the switches and SM capacitors losses. To overcome this issue, a Circulating Current Suppressing Controller (CCSC) has been proposed in [76].

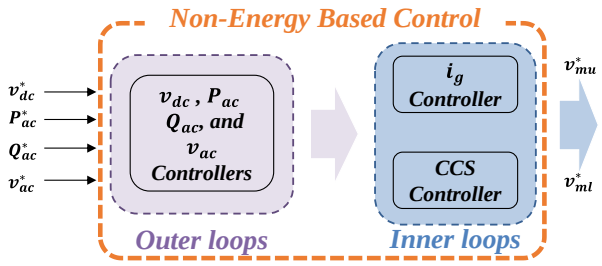

Figure III-35: Non energy based control diagram including CCSC.

The main drawback of non-energy based control concerns the system stability when the direct modulation is not used. Since there are no energy loops in the control structure, the stored energy in the arms diverges (increases or decreases).

4.2.2.2. Energy based control

In [66], the authors propose an improved control structure including energy loops to overcome the instability problem of MMC control. The outline of the proposed control, known as "Energy based control", is shown in Figure III-36.

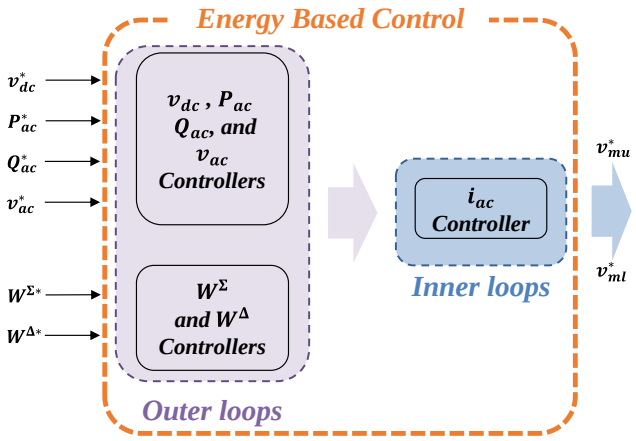

Figure III-36: Energy based control diagram (first version).

The results show that the proposed control is stable and allows to control the AC current as well as the stored energy in the arms. However, the arm currents are not well controlled especially during transients since the DC current is not directly controlled. For this purpose, a DC current controller has been added to the control structure by [86] in order to improve arm currents dynamics (see Figure III-37). Compared to the first version, the proposed control reduces the arm harmonics amplitude as well as the transient period when step changes are applied.

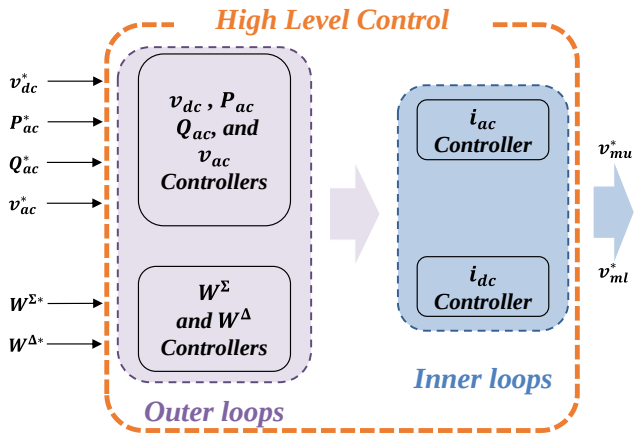

Figure III-37: Energy based control diagram (second version).

The control laws for each loop are derived based on the state-space equations summarized in Table III-2. Those state-space can be expressed in different reference frames: fixed frames (natural frame (abc), Alpha/Beta frame ($\alpha\beta 0$)) or rotating frame: Direct/quadrature frame ($dq0$). From theoretical aspects, these reference frames are equivalent as various configuration have been proposed in the literature. The choice criteria come from practical implementation aspects such as time delays, PLL performances… The following table summarize those configurations and their associated references.

Table III-3: Reference frames for MMC control loops.

	Natural frame (abc)	***Alpha/Beta frame (αβ0)***	***Rotating frame (dq0)***
AC current loop	[85] [87] [88]		[76] [52] [85]
DC current loop	[89]	[87]	[74]
Energy sum (leg)	[66]	[89] [87]	[74]
Energy diff	[66]	[89]	[74] [86]

5. Considered control structure for thesis contributions

Given that there are so many possibilities of MMC control structures, it is necessary to clarify the control structure that has been considered in this thesis before addressing its contributions in term of control design.

5.1. Low level control

In order to avoid unexpected internal dynamics inside the MMC, the closed loop indirect modulation is used to calculate the modulation index references. The nearest level control constitutes the modulation technique block to be in line with industrial system. When a detailed MMC model is used for control validations, the basic BCA ensures the balancing between the SMs. The schematic diagram of the used low level control is summarized in Figure III-38.

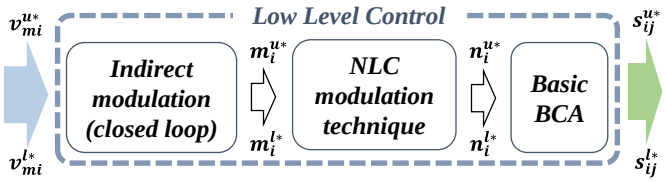

Figure III-38: Schematic diagram for the considered low level control for thesis contributions.

5.2. High level control

The schematic diagram of used high level control is illustrated in Figure III-39.

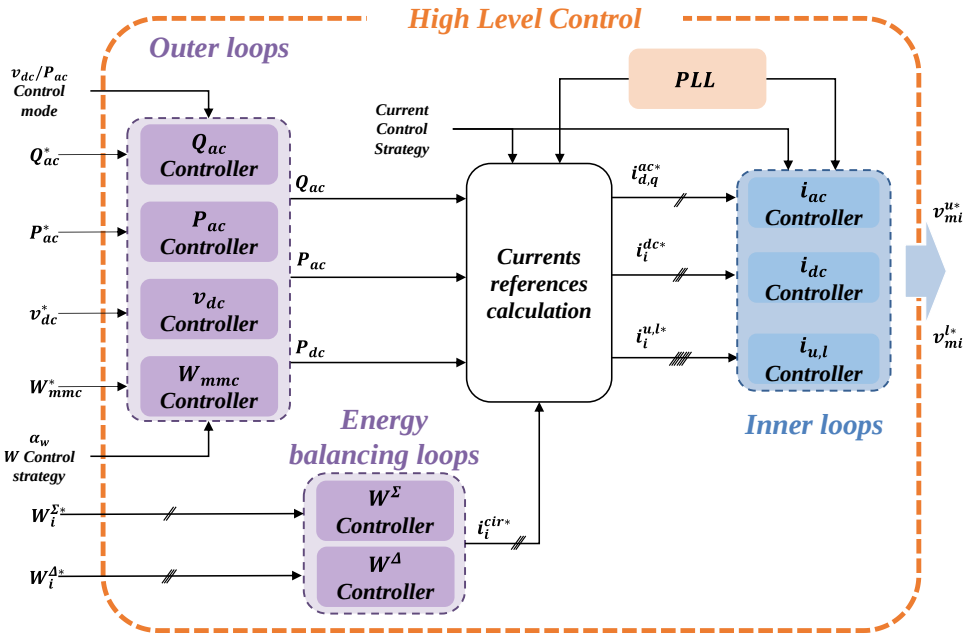

Figure III-39: Schematic diagram for the considered high level control for thesis contributions.

5.2.1. Outer loops

The proposed high level control is an energy based control where the following loops constitute its outer layer:

- DC voltage controller.
- Active power controller.
- Reactive power controller.
- Energy global controller.

For each loop, PI regulator is used to derive its control laws except for active and reactive power controllers where only proportional gain is used (P controller). The controller gains have been calculated to obtain the desired response times shown in Figure III-40. The manner how they are calculated is presented in APPENDICES, section 2.

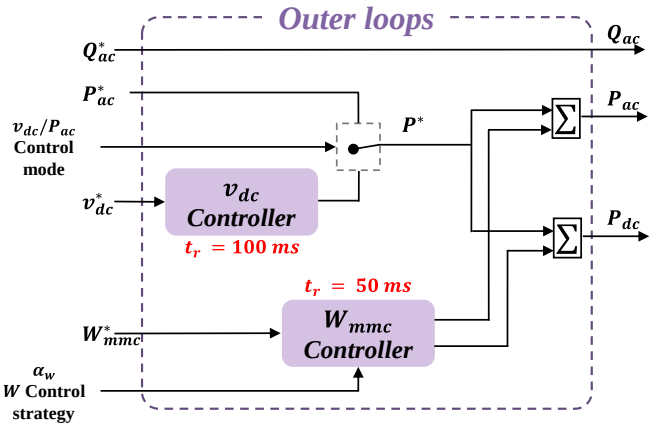

Figure III-40: Zoom on outer loops configuration.

In addition to the references for each loop, two inputs parameter are used to perform the control which are:

- v_{dc}/P_{ac}: Switch the operation mode of the station.
- α_w: Change the energy control strategy.

Energy parameter α_w allows to change the control strategy for energy loop. It takes 0 or 1 value, corresponding to respectively, AC grid and DC grid control strategy for energy loop. When α_w is set to a value between 0 and 1, the energy regulation will be shared between AC and DC grids.

The outputs are calculated as follow:

$$P_{dc} = P^* + \alpha_w P_w^*$$
$$P_{ac} = P^* + (1 - \alpha_w) P_w^* \qquad \textit{(III-24)}$$
$$Q_{ac} = Q_{ac}^*$$

Where:

P_w^* : Output of energy loop.

5.2.2. Energy balancing loops

According to the analysis given above (see section 4.1.4), it has been proven that the energy loop alone cannot ensure a balanced energy sharing between the arms. To avoid such situation, energy balancing loops (see equations (III-21) and (III-23)) are employed in the proposed high level control. They allow to control the energy sum (leg) and difference for the three legs. For energy sum, it is sufficient to control the energy in two legs only since that the third is a consequence of the energy balance.

$$W_3^{\Sigma} = W_{mmc} - W_1^{\Sigma} - W_2^{\Sigma} \qquad \textit{(III-25)}$$

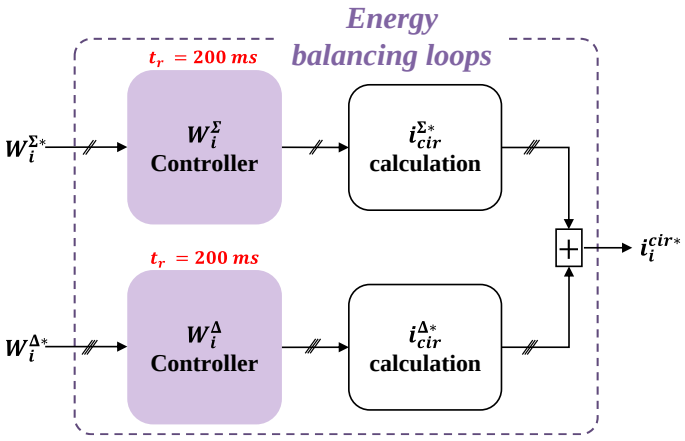

Figure III-41: Zoom on energy balancing loops configuration.

In this thesis, energy balancing loops are considered as an intern regulation. It means that their references are set to constant values: 1 pu for energy sum and 0 for energy difference. Their response times have been set four times slower than the energy loop one (see Figure III-41). This ratio allows to balance the internal energy between the arms without affecting the powers

flowing through the MMC. For this purpose, balanced circulating currents are created, based on energy balancing loops outputs as follows:

$$\begin{bmatrix} i_{cira}^{\Sigma*} \\ i_{cirb}^{\Sigma*} \\ i_{circ}^{\Sigma*} \end{bmatrix} = i_{mat}^{cir\Sigma} \begin{bmatrix} i_1^{\Sigma*} \\ i_2^{\Sigma*} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} i_1^{\Sigma*} \\ i_2^{\Sigma*} \end{bmatrix}$$

$$\begin{bmatrix} i_{cira}^{\Delta*} \\ i_{cirb}^{\Delta*} \\ i_{circ}^{\Delta*} \end{bmatrix} = i_{mat}^{cir\Delta} \begin{bmatrix} i_a^{\Delta} \\ i_b^{\Delta} \\ i_c^{\Delta} \end{bmatrix} = \begin{bmatrix} 1 & -0.5 & -0.5 \\ -0.5 & 1 & -0.5 \\ -0.5 & -0.5 & 1 \end{bmatrix} \begin{bmatrix} i_a^{\Delta} \\ i_b^{\Delta} \\ i_c^{\Delta} \end{bmatrix} \quad \textit{(III-26)}$$

Where:

- $i_{1,2}^{\Sigma*}$: Output of energy sum controller.
- $i_{a,b,c}^{\Sigma*}$: Output of energy difference controller.

It can be observed that, thanks to transformations given in equations (III-26) of energy balancing loops, the sum of i_{cir}^{*} requested by energy balancing loops is always equal to zero.

5.2.3. Current references calculation

In the proposed control, two control strategies can be adopted:

- ***AC and DC currents control.***
- ***Arm currents control.***

5.2.3.1. Inner loops based on AC and DC currents controller

When the first principle is employed, the reference frames for AC and DC current loops are ($dq0$) and (abc) respectively. The abc frame reference for DC current controller allows to control each phase independently since the reference of circulation currents coming from energy balancing loops are given for each phase. The advantage of using rotating frame ($dq0$) in control theory is that, the sinewave references become a continuous components. To do so, the AC currents are transferred to direct and quadrature components and compared to their references. This transformation needs to measure the phase angle of AC voltage using a Phase locked loop (PLL) (see APPENDICES, section 2.5) requesting high performances in terms of

convergence time and robustness. The current references using this current control strategy are given by the following expressions:

$$i_i^{dc*} = \frac{P_{dc}}{3\,v_{dc}} + i_i^{cir*}$$

$$i_d^{ac*} = \frac{P_{ac}}{v_d^{ac}} \qquad \textit{(III-27)}$$

$$i_q^{ac*} = \frac{-Q_{ac}^*}{v_d^{ac}}$$

The response time of current loops depends on the controller design. For example, when a *PI* controller is used, the response time can be set to 5 ms for AC current controller and 3 ms for DC one. Advanced controller design techniques are requested if the response time needs to be accelerated.

5.2.3.2. Inner loops based on AC and DC currents controller.

If equation (III-27) is considered, the first strategy will strongly depend on the PLL performances. In order to reduce its impact on the MMC control, an inner control strategy based on arm currents is proposed here. In this control strategy, the arm currents controller is derived in (abc) frame. Based on the inverse of alpha/beta transformation, the three phase AC currents can be calculated by the following expression:

$$\begin{bmatrix} i_a^{ac*} \\ i_b^{ac*} \\ i_c^{ac*} \end{bmatrix} = \sqrt{\frac{2}{3}} \frac{1}{\left(v_\alpha^{ac2} + v_\beta^{ac2}\right)} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{ac} v_\alpha^{ac} - Q_{ac} v_\beta^{ac} \\ P_{ac} v_\beta^{ac} + Q_{ac} v_\alpha^{ac} \end{bmatrix} \qquad \textit{(III-28)}$$

The relation between the arm currents, AC currents, circulating currents and DC current is given by the following equation:

$$\begin{bmatrix} i_i^{u*} \\ i_i^{l*} \end{bmatrix} = \begin{bmatrix} 0.5 & 1 & 1 \\ -0.5 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_i^{ac*} \\ i_i^{dc*} \\ i_i^{cir*} \end{bmatrix} \qquad \textit{(III-29)}$$

The response time of the inner loops has to be set as fast as possible when the arm currents control strategy is adopted in order to follow the arm current references sinewaves. Therefore, advanced control algorithms are needed to overcome the PI controller limitations.

6. Conclusion

This chapter has been reviewing the problematic related to MMC control. It has been shown that two control layers are necessary to transform the control objectives into signal pulses that are: High level control and Low level control.

The low level control has to choose the best arms configuration in order to balance the energy between the arms. The parameters impacting and/or impacted by this control layer have been investigated leading to propose a new classification of different BCAs proposed in the literature. A comparative assessment by simulation show that there is no perfect method since all the parameters (switching frequency, voltage ripple, tolerance parameter and operation point) are directly coupled.

The high level control has to calculate the modulated voltages for each arm according to control objectives. The state-space equations of the MMC system have been extracted to understand its behavior regarding the connected grids and design its associated control algorithms. A global consideration of the MMC system by handling its state space model as multivariable control problem and cascaded control formulation which is based on time scales assumption have been discussed; the latter (cascaded control) has been chosen in the proposed work. Thereafter, the energy based and non-energy based controls have been explained with conclusion that the first control allows to obtain a better control of all MMC variables which is not the case with non-energy based control.

The energy based control which has been considered in this thesis allows to control the active power, reactive power, DC voltage and stored energy simultaneously. The energy regulation strategy can be adapted using energy parameter α_w and enabling the control of MMC energy from AC grid, DC grid or a contribution of both with a chosen ratio. Finally, it has been shown that two control strategies can be employed to master the current references provided by the outer loops as well as energy balancing ones. The first strategy is based on controlling the output current (AC and DC currents) where the second one is based on controlling the internal currents (arm currents).

CHAPTER IV Contributions to MMC control

1. Introduction

The purpose of this chapter is to provide contributions for both high and low level layers. Regarding the lower level, the Average Tolerance Band (ATB) method is improved in order to obtain a desired ripple and reduce the switching frequency. In order to overcome the large response time for outer loops when a cascaded structure is considered, a high dynamics controllers are proposed for MMC currents. First, for both (AC and DC currents/MMC arm currents) control strategies, continuous-time controllers based on variable structure control "sliding mode control" are proposed and validated using simplified models. To go further in term of performances and in order to integrate the hardware constraints such as sampling period (T), explicit formulation based on novel discrete-time controllers have been derived considering exact discrete-time models. The obtained solutions have been compared to the known one based on Euler approximation. Finally, offline validation of proposed controllers for normal operations and against externals events are carried out to show their advantages.

2. A contribution to low level control: Improved Averaged Tolerance Band (IATB) method

2.1. Introduction

As a reminder, the proposed ATB method in [78] consists of mitigating the SMs ripple while maintaining a relatively low number of switching. Thanks to the tolerance band parameter ε, the ATB algorithm ensures that the SM voltages are kept inside a hysteresis band (dashed lines) as it is shown in Figure IV-1. The results presented in Table IV-1 have been calculated using the same simulation parameter in CHAPTER III (see section 3.4).

Table IV-1: Switching frequencies using ATB method with $\varepsilon = 5\%$.

Transferred power (pu)		***0.3 pu***	***0.6 pu***	***0.9 pu***
Ripple (%)		*9.2*	*13.81*	*17.1*
Switching frequency (Hz)	***Average***	*121*	*135*	*181*
	Max	*147*	*158*	*212*
	Min	*104*	*125*	*170*

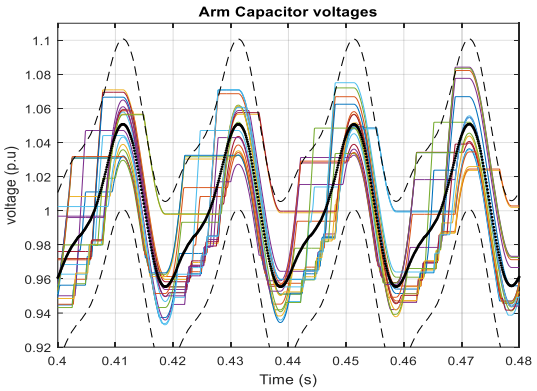

Figure IV-1: SM voltages variation using ATB algorithm.

According to Table IV-1, it can be concluded that the obtained ripple using ATB method depends on the transferred power. This can be attributed to the fact that the limits of hysteresis band are calculated based on the average ripple which is imposed by the operation point (transferred powers). In order to consider the ATB method as BCA with ripple mitigation, the presented ATB in [78] has to be improved to keep the SM voltages ripple equal to the desired one.

2.2. Improved ATB algorithm

Figure IV-2-(a) and Figure IV-2-(b) show the variation of voltage ripple and switching frequency with tolerance parameters for different power set points.

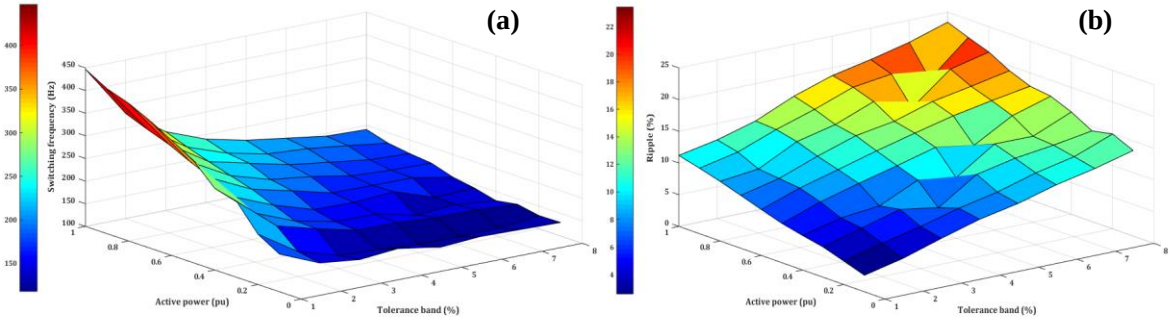

Figure IV-2: (a) Switching frequency, (b) voltage ripple variations regarding transferred power and tolerance band parameter.

By setting the tolerance parameter to a constant value, a given ripple and switching frequency are obtained according to the transferred power. From control point of view, we are concerned with the ripple of the voltages and the switching frequency (which have direct impacts on converter operation performances) and not the tolerance band parameter. For this purpose, a

new algorithm is proposed here where the tolerance parameter becomes a degree of freedom. The latter becomes a control parameter in order to:

- Maintain the ripple of SMs equal to the limits.
- Minimize the switching frequency and consequently the switching losses.

In the new ATB method (see Figure IV-3) and in addition to standard inputs (current direction, SM voltages and number of SMs to be inserted), the desired ripple value, operation point (P, Q) and the characteristics of Figure IV-2 are used to perform this BCA [90].

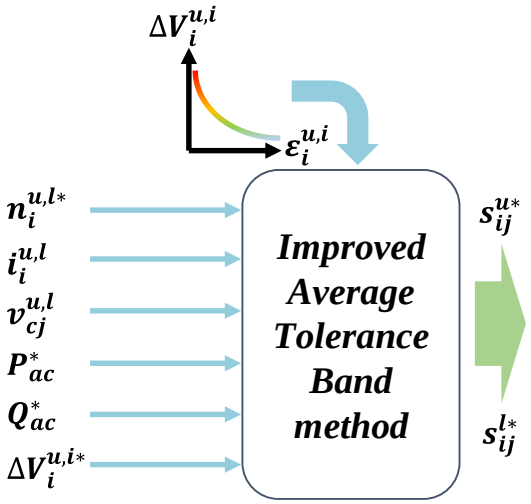

Figure IV-3: Proposed improved average tolerance band method diagram.

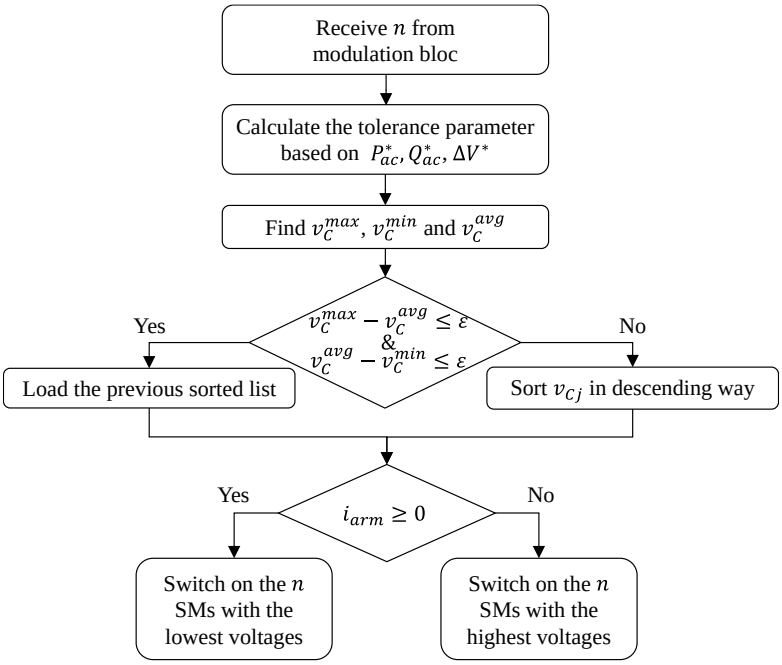

Figure IV-4: Proposed improved average tolerance band algorithm flowchart.

The tolerance parameter is calculated in real time according to the power setpoints and the desired ripple. This makes it possible to keep the MMC working with optimized switching frequencies according to the power exchanged while keeping the same ripple of the voltages.

2.3. Simulation and validation

In order to test the proposed method, the following simulations have been carried out. The same simulation circuit with same parameters used in CHAPTER III (see section 3.4) are employed to perform the following test cases. Initially, the exchanged power is set to zero where the ripple reference is set to 11%. The events are steps change in the active power reference, it takes different values as follows:

- At t=0, an increased step of 0.6 pu is applied.
- At t=0.2, a decreased step of 0.3 pu is applied.
- At t=0.4, an increased step of 0.6 pu is applied.

The simulation results are presented in Figure IV-5 where the SM voltages of upper arm for leg (a) and active power variation are illustrated in (a)-(b) respectively.

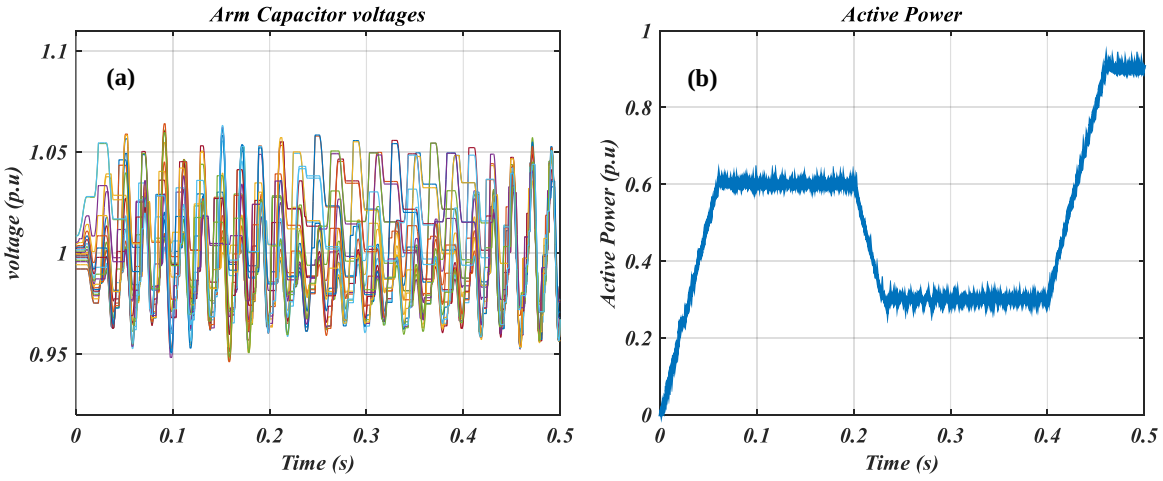

Figure IV-5: Simulation results: (a) SM voltage for one arm, (b) active power.

As it can be seen, the proposed BCA makes it possible to keep the voltage ripple less than the imposed value (11%) for different levels of exchanged power. Making the tolerance parameter as variable allows to decouple the obtained ripple from the transferred power level which was not possible with the first version of ATB method presented in [78]. A zoom on SM voltages is

shown in Figure IV-6. It can be observed that the switching frequency of IGBTs changes according to the transferred power level.

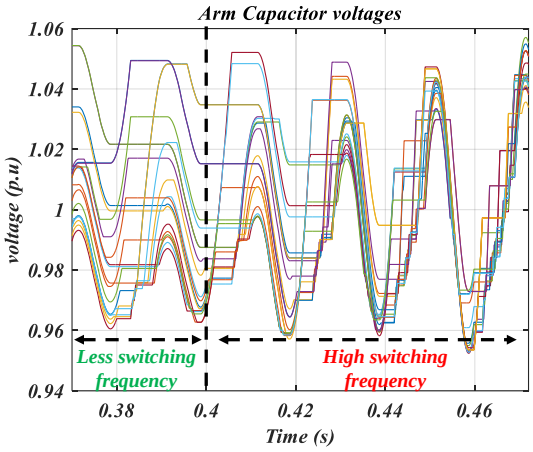

Figure IV-6: A zoom on SM voltages.

The proposed BCA enables the MMC to operate with low switching frequencies (100-150 Hz) at low power levels (0.3 pu) and medium frequencies with high power levels (0.9 pu) (see Table IV-2).

Another important point playing a crucial role in the voltage ripple is the capacitor value. The latter plays an important role in the voltage ripple. An oversizing of its value reduces the natural ripple of the voltages, thus allowing to switching frequency reduction. Consequently, a cost-benefit analysis (switching losses / SM sizing) is necessary in order to properly size the MMC capacitors.

Table IV-2: Switching frequencies using proposed BCA.

Transferred power (pu)		***0.3 pu***	***0.6 pu***	***0.9 pu***
Ripple (%)		*10.5*	*10.8*	*10.93*
Switching frequency (Hz)	***Average***	*111*	*186*	*342*
	Max	*135*	*213*	*373*
	Min	*102*	*151*	*302*

3. Contributions to high level control: high dynamics MMC control

3.1. Introduction

In cascaded control scheme configuration, the main hypothesis in order to decouple the system, is to establish control layers where the response time of each layer is set inside a time range. Knowing that our aim is to accelerate the whole control system, in such configurations, the response time of the outer loops is highly related to the inner loop ones. The outer loops cannot be accelerated beyond a critical value in order to not deteriorate the stability of the control system which conflict with the starting hypothesis of cascaded systems. From practical point of view which is often used in industry, the ratio between response time of outer and inner loops is set higher than 10. Moreover, the response time of the inner loops cannot be decreased indefinitely as it is limited by the physical limits of the converter and by the hardware technology in which the balancing control algorithm is implemented. Different control based techniques for MMC currents have been presented in the literature: *PI* controllers [74, 91], Proportional-resonant controllers [92], Internal Mode Control (IMC) [93] and optimal Linear Quadratic Regulator (LQR) controller [94]. These controllers have been obtained using continuous state-space models. They offer good dynamics if their response time requirement is large enough. However, reducing their response time can make the system unstable. Moreover, when they are implemented in digital signal processors, some simplifying assumptions have to be introduced. These assumptions can affect the desired dynamics and create instability in the control system. In the following, new controllers based on variable structure control are proposed which allow to accelerate the response time of current loops. In order to not burden the reading, it should be noted that all developments based design has been applied to the first current control strategy which is controlling the output currents (AC and DC currents). For the second control strategy (MMC arm currents), it is given in APPENDICES, section 3.

3.2. Variable structure MMC control: sliding mode control

Since the objective of this work is to accelerate the response time of inner loops and consequently the outer loops, sliding mode control based design has been chosen to derive their control laws. In addition to converge in finite time, the design of such variable-structure control

makes the derived control law insensitive to parameter uncertainties and external disturbances which is hardly possible with other fast controllers [95, 96, 97, 98]. In this section, the sliding mode approach is applied to the AC and DC continuous-time models in order to derive their associated control laws.

3.2.1. Sliding mode control for MMC

As a reminder, for a three-phase MMC, the continuous state-space AC and DC model in dq and abc references frame respectively can be written as:

$$\begin{bmatrix} \frac{di_d^{ac}}{dt} \\ \frac{di_q^{ac}}{dt} \end{bmatrix} = A \begin{bmatrix} i_d^{ac} \\ i_q^{ac} \end{bmatrix} + B \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix} \quad \textit{(IV-1)}$$

$$\begin{bmatrix} \frac{di_a^{dc}}{dt} \\ \frac{di_b^{dc}}{dt} \\ \frac{di_c^{dc}}{dt} \end{bmatrix} = C \begin{bmatrix} i_a^{dc} \\ i_b^{dc} \\ i_c^{dc} \end{bmatrix} + D \begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix} \quad \textit{(IV-2)}$$

Where:

$$A = \begin{bmatrix} \frac{-R_{eq}^{ac}}{L_{eq}^{ac}} & \omega \\ -\omega & \frac{-R_{eq}^{ac}}{L_{eq}^{ac}} \end{bmatrix},\ B = \begin{bmatrix} \frac{1}{L_{eq}^{ac}} & 0 \\ 0 & \frac{1}{L_{eq}^{ac}} \end{bmatrix},\ \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix} = \begin{bmatrix} v_{md}^{ac} - v_{d}^{ac} \\ v_{mq}^{ac} - v_{q}^{ac} \end{bmatrix}$$

$$C = \begin{bmatrix} \frac{-R_{eq}^{dc}}{L_{eq}^{dc}} & 0 & 0 \\ 0 & \frac{-R_{eq}^{dc}}{L_{eq}^{dc}} & 0 \\ 0 & 0 & \frac{-R_{eq}^{dc}}{L_{eq}^{dc}} \end{bmatrix} D = \begin{bmatrix} \frac{1}{L_{eq}^{dc}} & 0 & 0 \\ 0 & \frac{1}{L_{eq}^{dc}} & 0 \\ 0 & 0 & \frac{1}{L_{eq}^{dc}} \end{bmatrix} \begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix} = \begin{bmatrix} v_{dc} - v_{ma}^{dc} \\ v_{dc} - v_{mb}^{dc} \\ v_{dc} - v_{mc}^{dc} \end{bmatrix}$$

Based on equations (IV-1) and (IV-2), the current controllers have to calculate the control vector v_{rl}^{ac} and v_{rl}^{dc} to bring the currents to their references. For this purpose, two sliding surfaces for AC side and three for DC one can be chosen according to control target (reference requirements), that are:

$$s_{ac} = \begin{cases} s_1^{ac} = \varepsilon_1^{ac} \\ s_2^{ac} = \varepsilon_2^{ac} \end{cases}$$

$$s_{dc} = \begin{cases} s_1^{dc} = \varepsilon_1^{dc} \\ s_2^{dc} = \varepsilon_2^{dc} \\ s_3^{dc} = \varepsilon_3^{dc} \end{cases} \qquad \textit{(IV-3)}$$

Where:

$$\varepsilon_1^{ac} = i_d^{ac} - i_d^{ac*}$$

$$\varepsilon_2^{ac} = i_q^{ac} - i_q^{ac*}$$

$$\varepsilon_1^{dc} = i_a^{dc} - i_a^{dc*}$$

$$\varepsilon_2^{dc} = i_b^{dc} - i_b^{dc*}$$

$$\varepsilon_3^{dc} = i_c^{dc} - i_c^{dc*}$$

The time derivative of sliding surfaces can be written as follow taking in the account equations (IV-1) and (IV-2):

$$\frac{ds_{ac}}{dt} = \begin{cases} \dfrac{ds_1^{ac}}{dt} = \left(A_{11} i_d^{ac} + A_{12} i_q^{ac}\right) + B_{11} v_{rld}^{ac} - \dfrac{di_d^{ac*}}{dt} \\ \dfrac{ds_2^{ac}}{dt} = \left(A_{21} i_d^{ac} + A_{22} i_q^{ac}\right) + B_{22} v_{rlq}^{ac} - \dfrac{di_q^{ac*}}{dt} \end{cases}$$

$$\frac{ds_{dc}}{dt} = \begin{cases} \dfrac{ds_1^{dc}}{dt} = C_{11} i_a^{dc} + D_{11} v_{rla}^{dc} - \dfrac{di_a^{dc*}}{dt} \\ \dfrac{ds_2^{dc}}{dt} = C_{22} i_b^{dc} + D_{22} v_{rlb}^{dc} - \dfrac{di_b^{dc*}}{dt} \\ \dfrac{ds_3^{dc}}{dt} = C_{33} i_c^{dc} + D_{33} v_{rlc}^{dc} - \dfrac{di_c^{dc*}}{dt} \end{cases} \qquad \textit{(IV-4)}$$

Equations (IV-4) can be written in matrix form as follow:

$$\frac{ds_{ac}}{dt} = A \begin{bmatrix} i_d^{ac} \\ i_q^{ac} \end{bmatrix} + B \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix} - \begin{bmatrix} \dfrac{di_d^{ac*}}{dt} \\ \dfrac{di_q^{ac*}}{dt} \end{bmatrix} = \alpha_{ac} + \beta_{ac} \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix} \qquad \textit{(IV-5)}$$

$$\frac{ds_{dc}}{dt} = C \begin{bmatrix} i_a^{dc} \\ i_b^{dc} \\ i_c^{dc} \end{bmatrix} + D \begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix} - \begin{bmatrix} \frac{di_a^{dc*}}{dt} \\ \frac{di_b^{dc*}}{dt} \\ \frac{di_c^{dc*}}{dt} \end{bmatrix} = \alpha_{dc} + \beta_{dc} \begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}$$

Where:

$$\alpha_{ac} = A \begin{bmatrix} i_d^{ac} \\ i_q^{ac} \end{bmatrix} - \begin{bmatrix} \frac{di_d^{ac*}}{dt} \\ \frac{di_q^{ac*}}{dt} \end{bmatrix}$$

$$\beta_{ac} = B$$

$$\alpha_{dc} = C \begin{bmatrix} i_a^{dc} \\ i_b^{dc} \\ i_c^{dc} \end{bmatrix} - \begin{bmatrix} \frac{di_a^{dc*}}{dt} \\ \frac{di_b^{dc*}}{dt} \\ \frac{di_c^{dc*}}{dt} \end{bmatrix}$$

$$\beta_{dc} = D$$

Since the input vector appears explicitly in the time derivative of sliding surfaces, then, the transversality condition is satisfied for the considered system (equations (IV-5) [37].

Putting the input vectors as function of sign function of sliding surfaces, that are:

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_i = \begin{bmatrix} v_{id}^{ac} \\ v_{iq}^{ac} \end{bmatrix} = -{\beta_{ac}}^{-1} \, k_i^{ac} \, sign(s_{ac})$$

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_i = \begin{bmatrix} v_{ia}^{dc} \\ v_{ib}^{dc} \\ v_{ic}^{dc} \end{bmatrix} = -{\beta_{dc}}^{-1} \, k_i^{dc} \, sign(s_{dc}) \qquad \textit{(IV-6)}$$

Where:

$$k_i^{ac} = \begin{bmatrix} k_{i11}^{ac} & 0 \\ 0 & k_{i22}^{ac} \end{bmatrix}$$

$$k_i^{dc} = \begin{bmatrix} k_{i11}^{dc} & 0 & 0 \\ 0 & k_{i22}^{dc} & 0 \\ 0 & 0 & k_{i33}^{dc} \end{bmatrix}$$

Taking into account equations (IV-6), the time derivative of sliding surfaces (equations (IV-4)) becomes:

$$\begin{aligned} \frac{ds_{ac}}{dt} &= \alpha_{ac} + \beta_{ac}\left(-{\beta_{ac}}^{-1}\, k_i^{ac}\, sign(s_{ac})\right) = \alpha_{ac} - k_i^{ac}\, sign(s_{ac}) \\ \frac{ds_{dc}}{dt} &= \alpha_{dc} + \beta_{dc}\left(-{\beta_{dc}}^{-1}\, k_i^{dc}\, sign(s_{dc})\right) = \alpha_{dc} - k_i^{dc}\, sign(s_{dc}) \end{aligned} \qquad \textit{(IV-7)}$$

Then, the sliding surfaces are attractive if $s_{ac}\frac{ds_{ac}}{dt}$ and $s_{dc}\frac{ds_{dc}}{dt}$ are negative

$$\begin{aligned} s_{ac}\frac{ds_{ac}}{dt} &= s_{ac}\left(\alpha_{ac} - k_i^{ac}\, sign(s_{ac})\right) < 0 \\ s_{dc}\frac{ds_{dc}}{dt} &= s_{dc}\left(\alpha_{dc} - k_i^{dc}\, sign(s_{dc})\right) < 0 \end{aligned} \qquad \textit{(IV-8)}$$

The conditions given in equations (IV-8) are satisfied when the gains vector k_i^{ac} and k_p^{ac} satisfy the following conditions:

$$\begin{cases} |k_{i11}^{ac}| > \left|A_{11} i_d^{ac} + A_{12} i_q^{ac} - \frac{di_d^{ac*}}{dt}\right| \\ |k_{i22}^{ac}| > \left|A_{21} i_d^{ac} + A_{22} i_q^{ac} - \frac{di_q^{ac*}}{dt}\right| \end{cases}$$

$$\begin{cases} \left|k_{i11}^{dc}\right| > \left|C_{11} i_a^{dc} - \frac{di_a^{dc*}}{dt}\right| \\ \left|k_{i22}^{dc}\right| > \left|C_{22} i_b^{dc} - \frac{di_b^{dc*}}{dt}\right| \\ \left|k_{i33}^{dc}\right| > \left|C_{33} i_c^{dc} - \frac{di_c^{dc*}}{dt}\right| \end{cases} \qquad \textit{(IV-9)}$$

In addition to the attractivity conditions and in order to ensure that the sliding surfaces are invariant when the state variables are equal to their references (i.e. $s_{ac} = s_{dc} = 0$), the time derivative of sliding surfaces has to be equal to zero. The control derived from this condition is usually called “equivalent control” in sliding mode control theory. That are:

$$\frac{ds_{ac}}{dt} = 0 = \alpha_{ac} + \beta_{ac}\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{eq}$$

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{eq} = \beta_{ac}^{-1}\alpha_{ac}$$

$$\frac{ds_{dc}}{dt} = 0 = \alpha_{dc} + \beta_{dc}\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{eq} \qquad \textit{(IV-10)}$$

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{eq} = \beta_{dc}^{-1}\alpha_{dc}$$

Consequently, the control law based on sliding mode control for AC side is given by:

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix} = \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{i} + \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{eq}$$

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{i} = -{\beta_{ac}}^{-1}\, k_i^{ac}\, sign(s_{ac}) \text{ with } \begin{cases} |k_{i11}^{ac}| > \left|A_{11} i_d^{ac} + A_{12} i_q^{ac} - \frac{di_d^{ac*}}{dt}\right| \\ |k_{i22}^{ac}| > \left|A_{21} i_d^{ac} + A_{22} i_q^{ac} - \frac{di_q^{ac*}}{dt}\right| \end{cases} \qquad \textit{(IV-11)}$$

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{eq} = \beta_{ac}^{-1}\alpha_{ac}$$

For DC side, it is:

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix} = \begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{i} + \begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{eq}$$

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{i} = -{\beta_{dc}}^{-1}\, k_i^{dc}\, sign(s_{dc}) \text{ with } \begin{cases} \left|k_{i11}^{dc}\right| > \left|C_{11} i_a^{dc} - \frac{di_a^{dc*}}{dt}\right| \\ \left|k_{i22}^{dc}\right| > \left|C_{22} i_b^{dc} - \frac{di_b^{dc*}}{dt}\right| \\ \left|k_{i33}^{dc}\right| > \left|C_{33} i_c^{dc} - \frac{di_c^{dc*}}{dt}\right| \end{cases} \qquad \textit{(IV-12)}$$

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{eq} = \beta_{dc}^{-1}\alpha_{dc}$$

3.2.2. Validation

In this section, the control laws (IV-11) and (IV-12) are tested by simulation using the continuous-time models (see Figure IV-7) where the parameters are given in Table IV-3. To test the control algorithms with conditions that represent the real ones, the control loops are running with 200 µs sampling period (T) corresponding to the hardware time-step. The models are running with 10 µs simulation time-step (T_s) to have a good representation of physical system evolution.

Two step changes for active and reactive power references are tested in the following validation.

	Active Power reference [pu]	***Reactive power reference [pu]***
t= 0 s	*0.1*	*0*
t= 0.05 s	*0.5*	*0*
t= 0.1 s	*0.5*	*0.2*

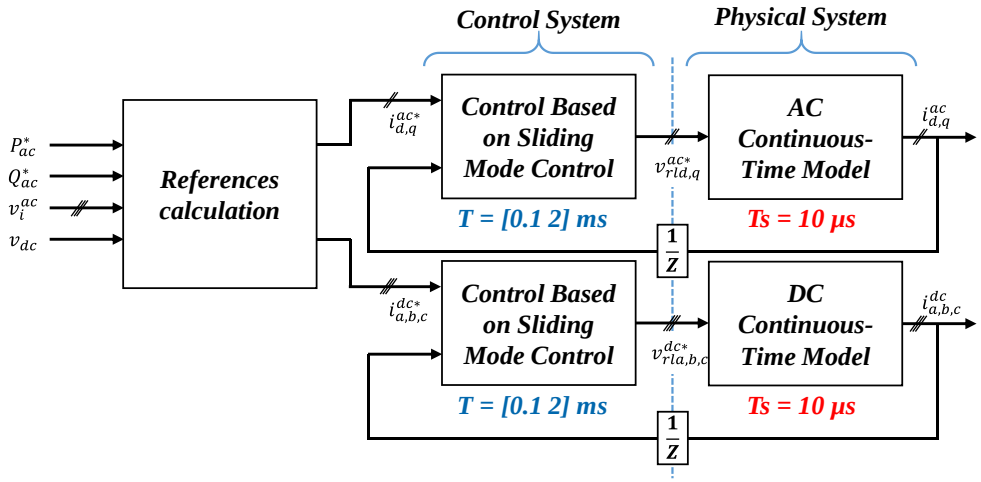

Figure IV-7: Simulation circuit for sliding mode control validation.

Since there is no method to set properly the sign function vector gain, different values are used to highlight its effects.

Table IV-3: MMC parameters for control validation.

Nominal power (MW)	*1000*
AC nominal voltage v_{ac}(kV)	*320 (rms line to line)*
DC nominal voltage v_{dc}(kV)	*640 (pole to pole)*
Number of SM	*40*
Inductance of the grid reactor L_f [pu]	*0.18*
Resistance of the grid reactor R_f [pu]	*0.005*
Arm resistance R_{arm}[pu]	*0.01*
Arm inductance L_{arm} [pu]	*0.15*
Electrostatic Constant H_c [pu]	*0.04*
Capacitor Cable C_{dc} [µF]	*48.4*
Simulation time-step T_s (µs)	*10*
Control Sampling period T (ms)	*[0.1, 1]*

At the beginning the gains are set to 10000 which satisfy the condition that has been derived from attractivity equations (see equations (IV-9)). The obtained results are presented in Figure IV-8 for active power step and Figure IV-9 for reactive power one.

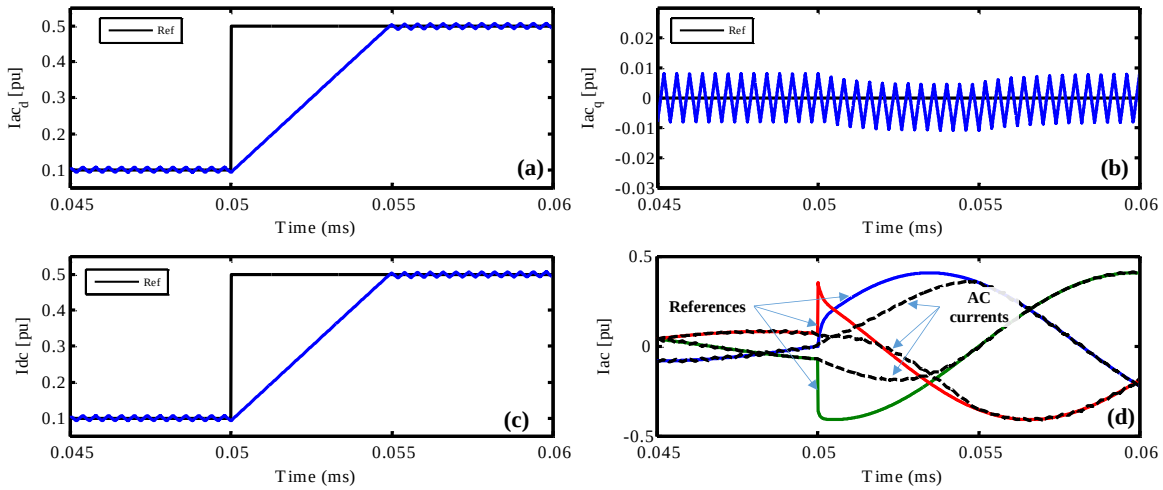

Figure IV-8: Simulation results for active power reference change (k_i^{ac}=k_i^{dc}=10000): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

As it can be observed the proposed control laws allow to bring the state variables to their associated references. For same gains value, it can be remarked that the obtained response time

depends on the step change value: 2 ms for 0.2 pu step change (reactive power step) and 5 ms for 0.5 pu step change (active power step).

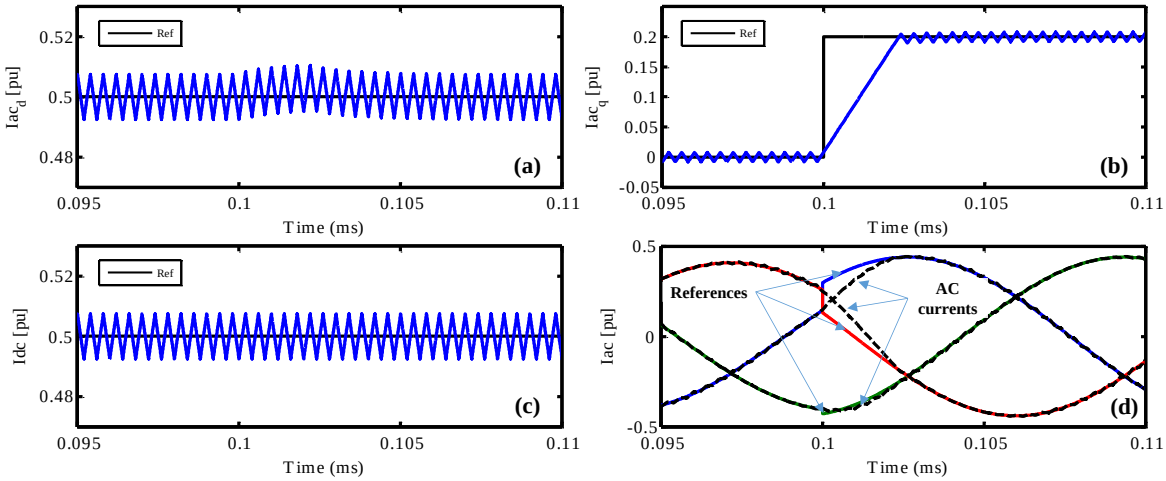

Figure IV-9: Simulation results for reactive power reference change (k_i^{ac}=k_i^{dc}=10000): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

However, it can be observed that undesirable oscillations with finite frequency and amplitude, well known as "Chattering phenomenon", take place on direct components as well as on the quadrature one. It can be attributed to the large gain of sign function on one hand and the discretization of controllers with large sampling period (200 µs) on the other hand. In sliding mode control theory, such problem can be prevented with different methods [99]. Choosing the interpolation solution [100], the sign function is replaced with a continuous function as follow:

$$sign(x) = \begin{cases} 1, & s > \sigma \\ -1, & s < -\sigma \\ \dfrac{x}{\sigma}, & |s| < |\sigma| \end{cases} \qquad \textit{(IV-13)}$$

Where: σ design parameter that can change boundary limits.

Taking in the account expression (IV-13), the control laws (IV-11) and (IV-12) are modified and tested with same simulation events as the previous test. The obtained results are presented in Figure IV-10 and Figure IV-11.

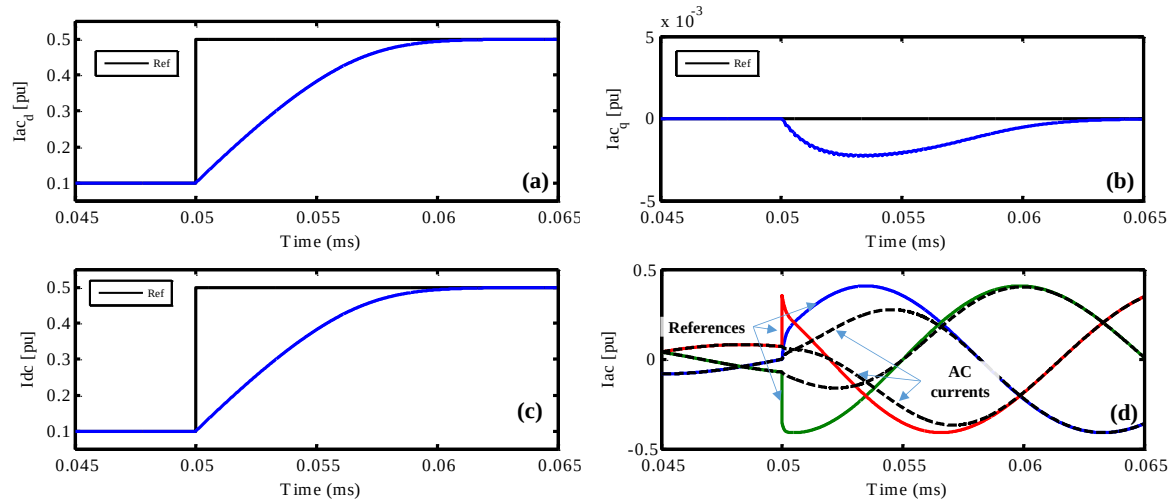

Figure IV-10: Simulation results for active power reference change (k_i^{ac}=k_i^{dc}=10000, σ=50): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

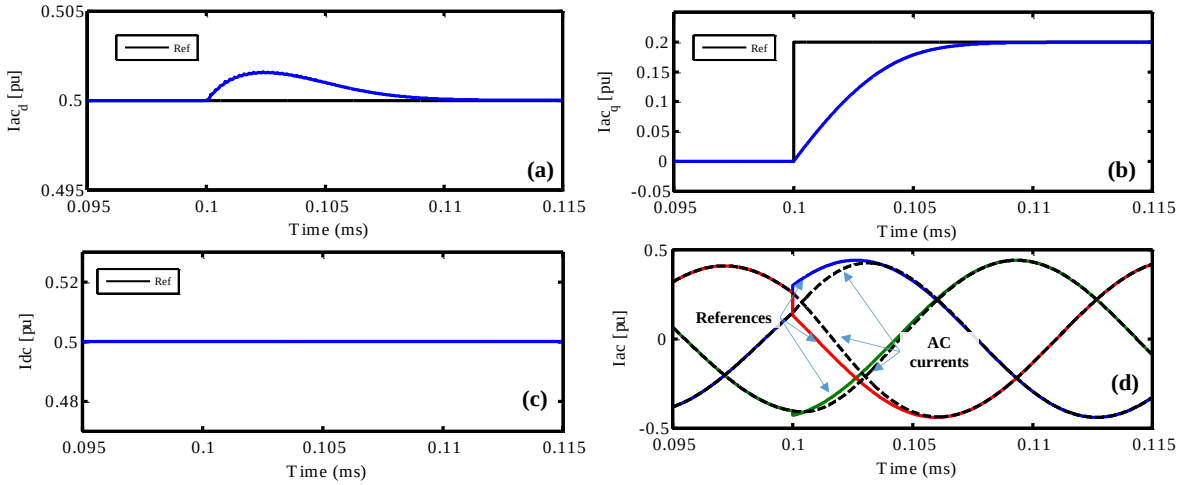

Figure IV-11: Simulation results for reactive power reference change (k_i^{ac}=k_i^{dc}=10000, σ=50): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

It can be observed from the obtained results that no chattering occurs in steady state and it is significantly reduced during transients. The currents quality is much better but at the cost of response time since the latter is increased even with same gain values as the previous test case.

In order to decrease the response time of current loops, the gain values have been increased three times bigger than the previous values.

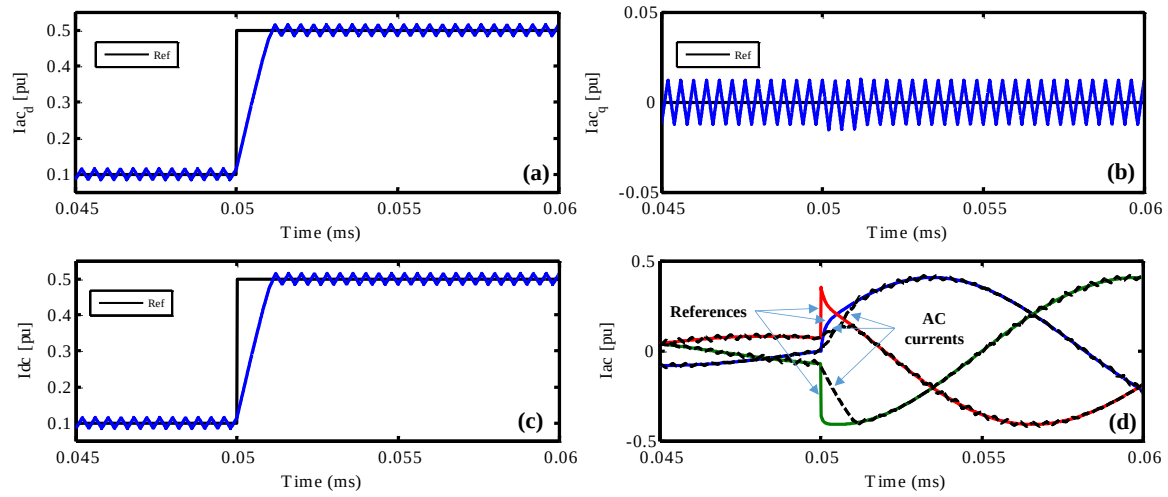

Figure IV-12: Simulation results for active power reference change (k_i^{ac}=k_i^{dc}=30000, σ=50): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

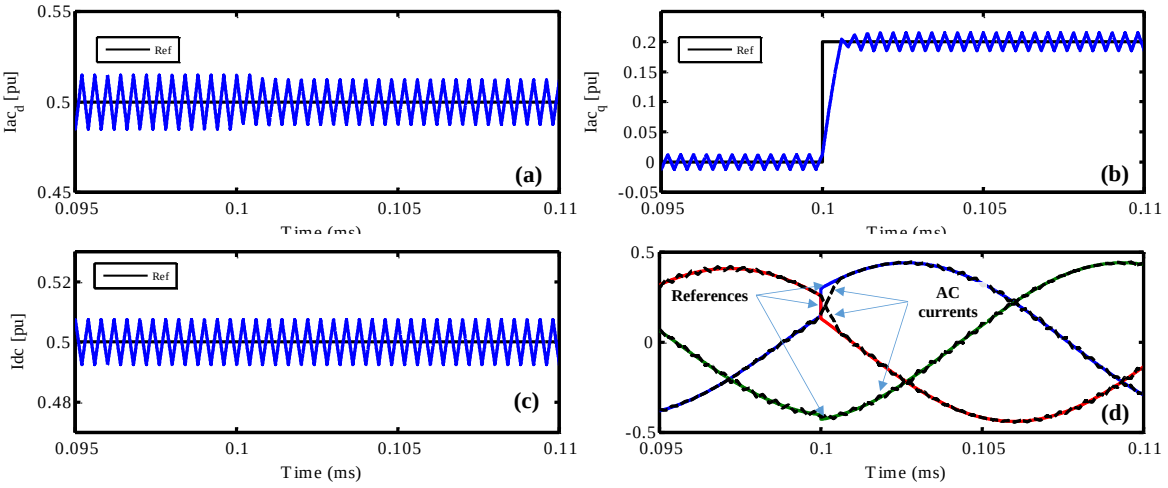

Figure IV-13: Simulation results for reactive power reference change (k_i^{ac}=k_i^{dc}=30000, σ=50): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

The results, presented in Figure IV-12 and Figure IV-13, show that the response time is relatively decreased however the chattering phenomena appears again even with the smooth continuous function.

It can be concluded from all these test cases that, the choice of gain vector for equations (IV-11) and (IV-12) is a trade-off between the response time and chattering phenomenon. Since the objective of this work is to obtain the highest dynamics without any current chattering, the actual control laws have to be improved.

3.2.3. Improved sliding mode control

In order to go further in term of currents loops performances, the obtained control laws (see (IV-11) and (IV-12)) are reworked. For this purpose, the control laws are modified as follow:

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_i = \begin{bmatrix} v_{id}^{ac} \\ v_{iq}^{ac} \end{bmatrix} = -{\beta_{ac}}^{-1} \left(k_i^{ac}\, sign(s_{ac}) + k_p^{ac}(s_{ac}) \right)$$

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_i = \begin{bmatrix} v_{ia}^{dc} \\ v_{ib}^{dc} \\ v_{ic}^{dc} \end{bmatrix} = -{\beta_{dc}}^{-1} \left(k_i^{dc}\, sign(s_{dc}) + k_p^{dc}(s_{dc}) \right) \qquad \textit{(IV-14)}$$

Where:

$$k_p^{ac} = \begin{bmatrix} k_{p11}^{ac} & 0 \\ 0 & k_{p22}^{ac} \end{bmatrix}$$

$$k_p^{dc} = \begin{bmatrix} k_{p11}^{dc} & 0 & 0 \\ 0 & k_{p11}^{dc} & 0 \\ 0 & 0 & k_{p11}^{dc} \end{bmatrix}$$

Taking into account equations (IV-14), the time derivative of sliding surfaces become:

$$\frac{ds_{ac}}{dt} = \alpha_{ac} - \beta_{ac}\,{\beta_{ac}}^{-1} \left(k_i^{ac}\, sign(s_{ac}) + k_p^{ac}(s_{ac}) \right)$$

$$\frac{ds_{ac}}{dt} = \alpha_{ac} - k_i^{ac}\, sign(s_{ac}) - k_p^{ac}(s_{ac})$$

$$\frac{ds_{dc}}{dt} = \alpha_{dc} - \beta_{dc}\,{\beta_{dc}}^{-1} \left(k_i^{dc}\, sign(s_{dc}) + k_p^{dc}(s_{dc}) \right) \qquad \textit{(IV-15)}$$

$$\frac{ds_{dc}}{dt} = \alpha_{dc} - k_i^{dc}\, sign(s_{dc}) + k_p^{dc}(s_{dc})$$

To ensure that the sliding surfaces are attractive, the product of $s_{ac}\frac{ds_{ac}}{dt}$ and $s_{dc}\frac{ds_{dc}}{dt}$ have to be negative. That are:

$$s_{ac}\frac{ds_{ac}}{dt} = s_{ac}\left(\alpha_{ac} - k_i^{ac}\, sign(s_{ac}) - k_p^{ac}(s_{ac})\right) = -s_{ac}\, k_p^{ac}(s_{ac}) + s_{ac}\left(\alpha_{ac} - k_i^{ac}\, sign(s_{ac})\right) < 0 \qquad \textit{(IV-16)}$$

$$s_{dc}\frac{ds_{dc}}{dt} = s_{dc}\left(\alpha_{dc} - k_i^{dc}\, sign(s_{dc}) - k_p^{dc}(s_{dc})\right)$$
$$= -s_{dc}\, k_p^{dc}(s_{dc}) + s_{dc}\left(\alpha_{dc} - k_i^{dc}\, sign(s_{dc})\right) < 0$$

The gains (k_i^{ac}, k_p^{ac}, k_i^{dc} and k_p^{dc}) that satisfy the previous conditions are given by the following expressions:

$$\begin{cases} |k_{i11}^{ac}| > \left|A_{11}i_d^{ac} + A_{12}i_q^{ac} - \dfrac{di_d^{ac*}}{dt}\right| \\ |k_{i22}^{ac}| > \left|A_{21}i_d^{ac} + A_{22}i_q^{ac} - \dfrac{di_q^{ac*}}{dt}\right| \\ k_{p11}^{ac} > 0 \\ k_{p22}^{ac} > 0 \end{cases}$$

$$\begin{cases} \left|k_{i11}^{dc}\right| > \left|C_{11}i_a^{dc} - \dfrac{di_a^{dc*}}{dt}\right| \\ \left|k_{i22}^{dc}\right| > \left|C_{22}i_b^{dc} - \dfrac{di_b^{dc*}}{dt}\right| \\ \left|k_{i33}^{dc}\right| > \left|C_{33}i_c^{dc} - \dfrac{di_c^{dc*}}{dt}\right| \\ k_{p11}^{dc} > 0 \\ k_{p22}^{dc} > 0 \\ k_{p33}^{dc} > 0 \end{cases} \qquad \textit{(IV-17)}$$

Similarly to the previous design, the new control law for AC current controller that satisfy the attractiveness and invariance conditions is obtained as:

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix} = \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_i + \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{eq}$$

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_i = -{\beta_{ac}}^{-1}\left(k_i^{ac}\, sign(s_{ac}) + k_p^{ac}(s_{ac})\right) \text{ with}$$
$$\begin{cases} |k_{i11}^{ac}| > \left|A_{11}i_d^{ac} + A_{12}i_q^{ac} - \frac{di_d^{ac*}}{dt}\right| \\ |k_{i22}^{ac}| > \left|A_{21}i_d^{ac} + A_{22}i_q^{ac} - \frac{di_q^{ac*}}{dt}\right| \\ k_{p11}^{ac} > 0 \\ k_{p22}^{ac} > 0 \end{cases} \qquad \textit{(IV-18)}$$

$$\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{eq} = \beta_{ac}^{-1}\alpha_{ac}$$

For DC current controller, the control law is given by:

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix} = \begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{i} + \begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{eq}$$

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{i} = -{\beta_{dc}}^{-1}\left(k_i^{dc}\, sign(s_{dc}) + k_p^{ac}(s_{dc})\right) \text{ with } \begin{cases} \left|k_{i11}^{dc}\right| > \left|C_{11}i_a^{dc} - \frac{di_a^{dc*}}{dt}\right| \\ \left|k_{i22}^{dc}\right| > \left|C_{22}i_b^{dc} - \frac{di_b^{dc*}}{dt}\right| \\ \left|k_{i33}^{dc}\right| > \left|C_{33}i_c^{dc} - \frac{di_c^{dc*}}{dt}\right| \\ k_{p11}^{dc} > 0 \\ k_{p22}^{dc} > 0 \\ k_{p33}^{dc} > 0 \end{cases} \quad \textit{(IV-19)}$$

$$\begin{bmatrix} v_{rla}^{dc} \\ v_{rlb}^{dc} \\ v_{rlc}^{dc} \end{bmatrix}_{eq} = \beta_{dc}^{-1}\alpha_{dc}$$

3.2.4. Stability analysis

For the stability proof, Lyapunov based method is employed. Only the stability prove for AC controller is considered in the following development, the same approach can be applied for DC one.

Consider the following positive definite function (Lyapunov function) for AC side defined as.

$$\psi_{ac} = \frac{1}{2}s_{ac}^{T}Q\, s_{ac} \quad \textit{(IV-20)}$$

Where:

$s_{ac} = \begin{bmatrix} i_d^{ac} - i_d^{ac*} \\ i_q^{ac} - i_q^{ac*} \end{bmatrix}$: Error vector.

$Q = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$: Identity matrix.

$s_{ac}^T = [i_d^{ac} - i_d^{ac*} \quad i_q^{ac} - i_q^{ac*}]$: Transposed vector of ε_{ac}.

The time derivative of Lyapunov function is then:

$$\frac{d\psi_{ac}}{dt} = \frac{1}{2}\left(\frac{ds_{ac}^T}{dt} Q\, s_{ac} + s_{ac}^T\, Q \frac{ds_{ac}}{dt}\right) = \frac{1}{2}\left(\frac{ds_{ac}^T}{dt} s_{ac} + s_{ac}^T \frac{ds_{ac}}{dt}\right) \qquad \textit{(IV-21)}$$

Noting that $\frac{ds_{ac}^T}{dt} s_{ac}$ and $s_{ac}^T \frac{ds_{ac}}{dt}$ are scalar functions, equation (IV-21) becomes:

$$\frac{d\psi_{ac}}{dt} = \frac{1}{2}\left(\frac{ds_{ac}^T}{dt} Q\, s_{ac} + s_{ac}^T\, Q \frac{ds_{ac}}{dt}\right) = s_{ac}^T \frac{ds_{ac}}{dt}$$

Taking in the account equation (IV-5), the time derivative of Lyapunov function is rewritten as follows:

$$\frac{d\psi_{ac}}{dt} = s_{ac}^T \frac{ds_{ac}}{dt} = s_{ac}^T \left(\alpha_{ac} + \beta_{ac} \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}\right) \qquad \textit{(IV-22)}$$

Replacing the input vector by its expression in equation (IV-18), equation (IV-22) becomes:

$$\frac{d\psi_{ac}}{dt} = s_{ac}^T \frac{ds_{ac}}{dt} = s_{ac}^T \left(\alpha_{ac} - \beta_{ac} \left(\begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_i + \begin{bmatrix} v_{rld}^{ac} \\ v_{rlq}^{ac} \end{bmatrix}_{eq}\right)\right) \qquad \textit{(IV-23)}$$

$$\frac{d\psi_{ac}}{dt} = s_{ac}^T \left(\alpha_{ac} - \beta_{ac} \left(-\beta_{ac}{}^{-1} \left(k_i^{ac}\, sign(s_{ac}) + k_p^{ac}(s_{ac})\right) + \beta_{ac}^{-1}\alpha_{ac}\right)\right)$$

The asymptotical convergence condition is one of the method that can prove control stability. It corresponds to prove that the time derivative of Lyapunov function is negative definite. That is:

$$\frac{d\psi_{ac}}{dt} = s_{ac}^T \frac{ds_{ac}}{dt} = s_{ac}^T \left(\alpha_{ac} - \left(k_i^{ac}\, sign(s_{ac}) + k_p^{ac}(s_{ac})\right) - \alpha_{ac}\right) \leq 0 \qquad \textit{(IV-24)}$$

$$\frac{d\psi_{ac}}{dt} = s_{ac}^T \left(-k_i^{ac}\, sign(s_{ac}) - k_p^{ac}(s_{ac})\right) \leq 0$$

It can be concluded that the asymptotic stability of the obtained control law (equation (IV-18)) can be guaranteed and the sliding motion can be ensured for the gain vector satisfying conditions of equation (IV-17).

3.2.5. Validation

After obtaining the new sliding model control laws and showing their stability, they are tested with simulation in the following.

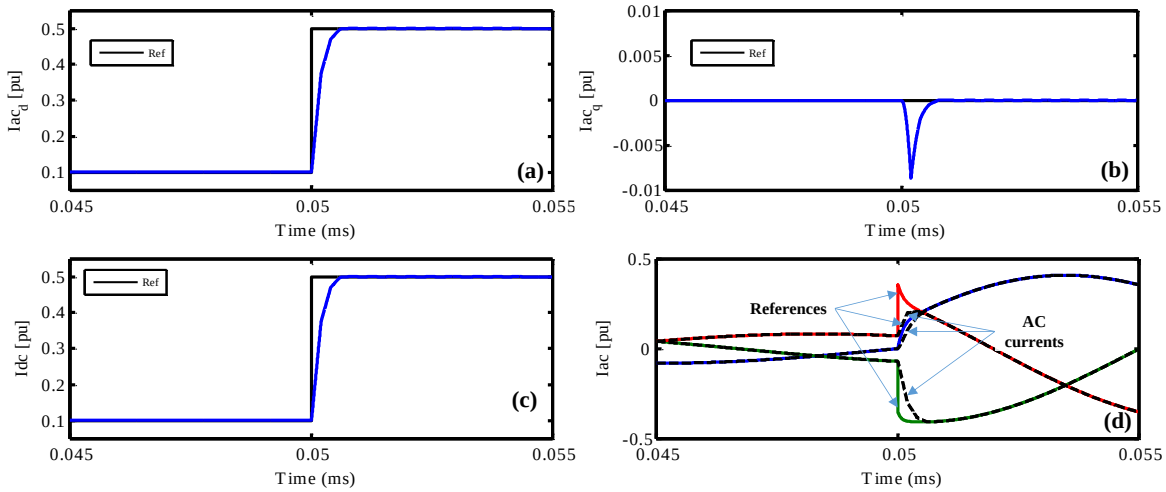

Figure IV-14: Simulation results for active power reference change (k_i^{ac}=k_i^{dc}=10000, σ=50, k_p^{ac}=k_p^{dc}=3200): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

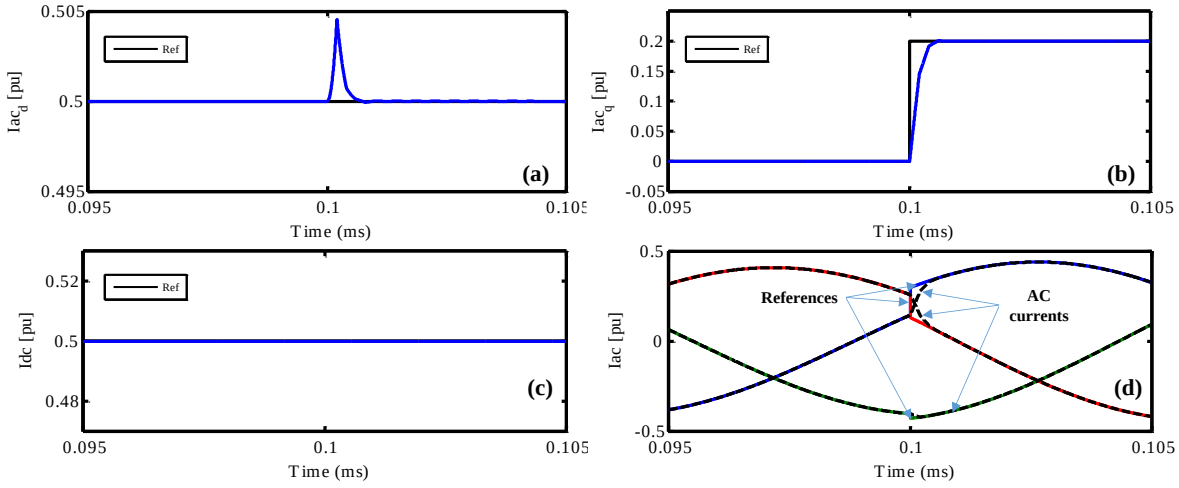

Figure IV-15: Simulation results for reactive power reference change (k_i^{ac}=k_i^{dc}=10000, σ=50, k_p^{ac}=k_p^{dc}=3200): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

To show the advantages brought by the new control laws, the same test cases with same control parameters ($k_i^{ac} = k_i^{dc} = 10000$, σ=50, T=0.2 ms) are used. The corresponding results are presented in Figure IV-14 and Figure IV-15. It can be observed from Figure IV-14-(a) and Figure IV-15-(b)) that the derived control laws allow to accelerate the current response time (~1 ms) which was not possible before. Thanks to proportional gains (k_p^{ac} and k_p^{dc}), the sign function gains (k_i^{ac} and k_i^{dc}) can be decreased without affecting the controllers performances that leads to suppress the chattering phenomenon during transient as well as in steady state (see Figure IV-14-(b) and Figure IV-15-(a)).

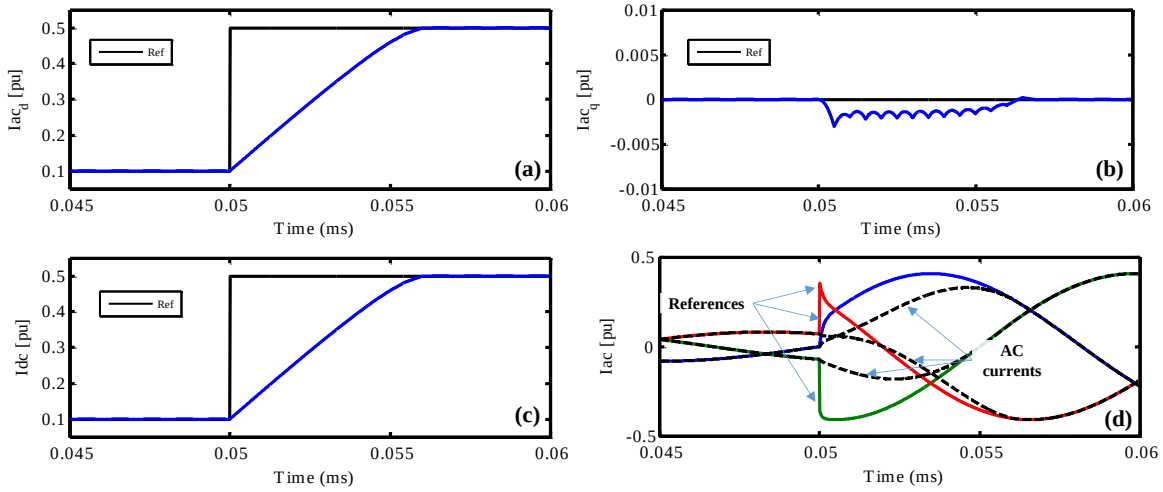

Figure IV-16: Simulation results for active power reference change with T=0.5 ms (k_i^{ac}=k_i^{dc}=10000, σ=50, k_p^{ac}=k_p^{dc}=3200): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

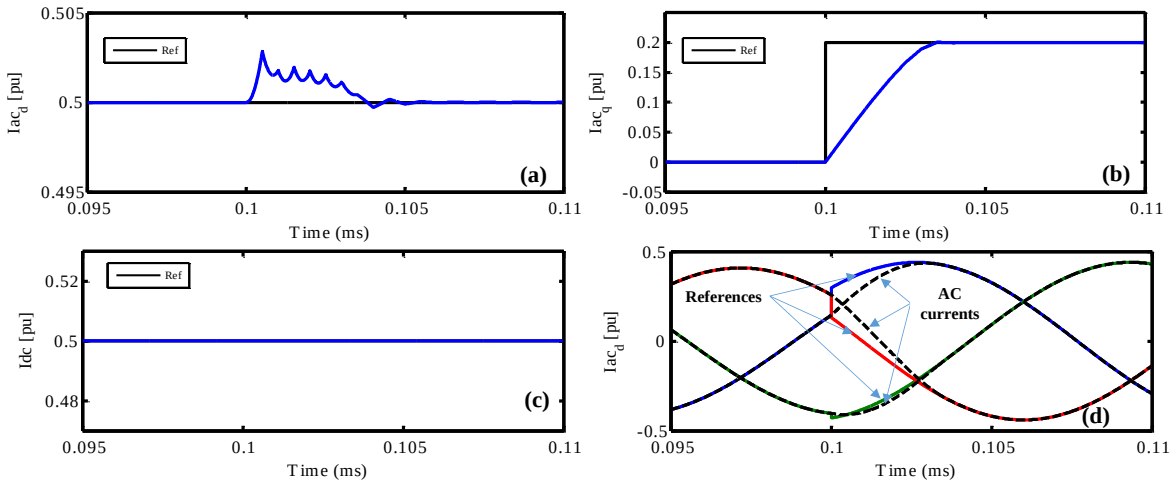

Figure IV-17: Simulation results for reactive power reference change with T=0.5 ms (k_i^{ac}=k_i^{dc}=10000, σ=50, k_p^{ac}=k_p^{dc}=3200): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

To highlight the effect of the sampling period (T), two different vaues have been used $T = 0.5\ ms$ and $T = 1\ ms$. The obtained results are presented in Figure IV-16 with Figure IV-17 for $T = 0.5\ ms$ and Figure IV-18 with Figure IV-19 for $T = 1\ ms$.

It can be observed from the results that, for same step changes and with the same gain values, the response time of controllers has been changed. It has been increased five times when the sampling period is equal to 0.5 ms (see Figure IV-16-(a) and Figure IV-17-(b)) and it can introduced undesirable oscillations leading to some instability for 1 ms sampling period (see Figure IV-18-(b) with Figure IV-19-(a)).

This means that, the derived control laws gains values have to be set according to the sampling period of controller when implemented. In order to well adjust the response time of current loops, it is better to consider à priori the sampling period in the control law derivation.

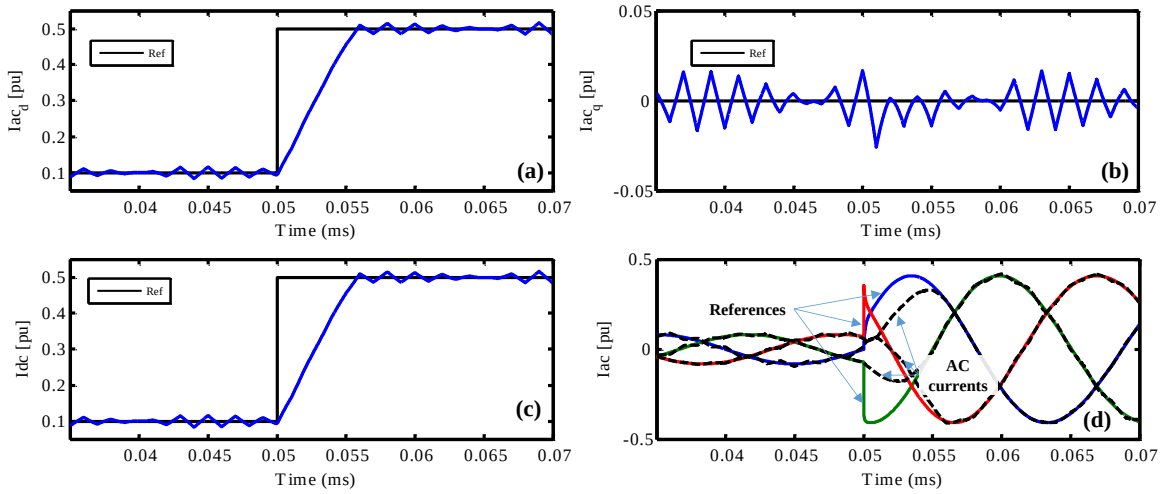

Figure IV-18: Simulation results for active power reference change with T=1 ms (k_i^{ac}=k_i^{dc}=10000, σ=50, k_p^{ac}=k_p^{dc}=3200): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

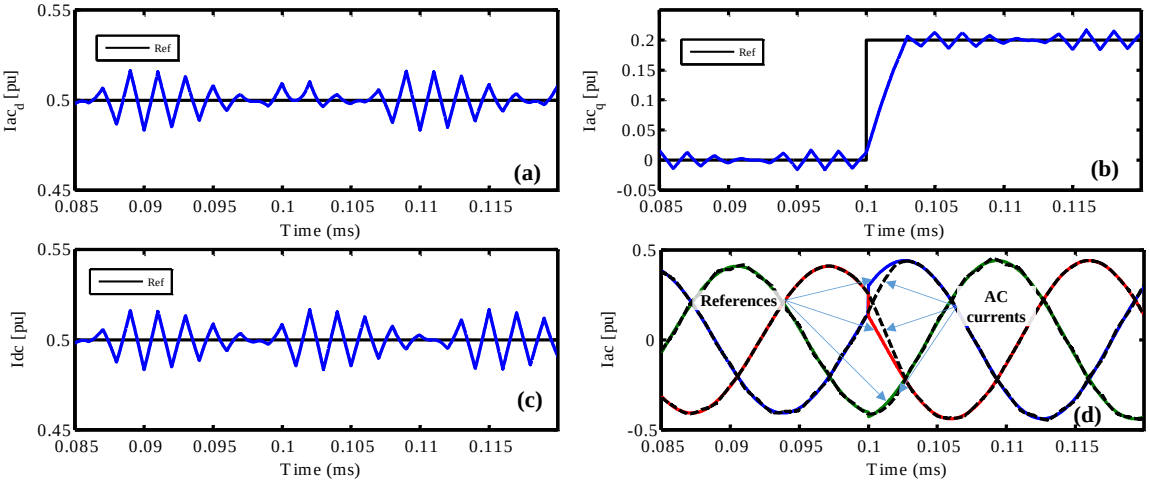

Figure IV-19: Simulation results for reactive power reference change with T=1 ms (k_i^{ac}=k_i^{dc}=10000, σ=50, k_p^{ac}=k_p^{dc}=3200): (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

3.3. Discrete-time MMC control

It has been concluded in the previous section that the sampling period has a major impact on the response of continuous-time controllers. To overcome this problem, a suitable discrete-time model taking into account a priori the sampling period of the hardware controller is proposed to derive the current control law. Following this philosophy, a discrete-time controller based on model predictive control has been proposed in [101]. To go further, the Dead-Beat controllers based on discrete-time model have been proposed in [102, 103, 104, 105]. In these papers, the authors have used simplified discrete-time models based on Euler approximation to derive these controllers. However, due to these assumptions, the desired response (one sampling period response) cannot be ensured accurately by these controllers especially when the sampling period is relatively large (i.e. 200~500 µs). In the following, a novel philosophy based on exact discrete-time models is adopted which allows the fastest dynamics as long as the system physical limits allow it and whatever the sampling period value is.

3.3.1. Exact discrete-time MMC modeling

For time discretization of a continuous state-space model, there are several numerical methods including Euler's forward method, Euler's backward method or Tustin's method [106].

Considering the following state-space model in continuous-time (t) representation.

$$\frac{dX(t)}{dt} = A\,X(t) + B\,U(t) \qquad \textit{(IV-25)}$$

The discrete-time model of equation (IV-25) can be derived using one of the methods cited before. Taking the Euler's backward method as example, the discrete-time model can be obtained using the following simplification:

$$\frac{dX(t)}{dt} = \frac{X\,(t_n + T) - X\,(t_n)}{T} \qquad \textit{(IV-26)}$$

Thus, the discrete-time model based on Euler method can be written as follows.

$$X\,(t_n + T) = (1 + A\,T)\,X(t_n) + B\,T\,U(t_n) \qquad \textit{(IV-27)}$$

Thanks to its simplicity, the model of equation (IV-27) is often used when a discrete-time controller is derived [102, 105]. However, the simplification given in equation (IV-26) is not always exact when the sampling period is increased. To overcome this problem and in order to make sure that the obtained discrete-time models are quite close to real MMC system (continuous-models), we propose to use an exact method to derive the MMC discrete-time models.

The exact discretization of the equation (IV-25) can be derived with the assumptions that the matrices A and B are time invariant between t_n and $t_n + T$ [107]. That is:

$$X\,(t_n + T) = F(T)\,X(t_n) + G(T)\,V \qquad \textit{(IV-28)}$$

Where V is the mean vector of U between t_n and $t_n + T$ and $F(T)$ and $G(T)$ are given by the following expressions:

$$\begin{aligned} F(T) &= e^{A\,T} \\ G(T) &= A^{-1}(e^{A\,T} - I)B \end{aligned} \qquad \textit{(IV-29)}$$

The Taylor expansion of $F(T)$ shows that, contrary to the Euler method, all the terms are taking in the account using the above discretization, see equation (IV-30).

$$F(T) = \overbrace{e^{A\,T}}^{\textit{Exact Method}} = \overbrace{1 + \frac{A\,T}{1!}}^{\textit{Euler Method}} + \overbrace{\frac{(A\,T)^2}{2!} + \cdots + \frac{(A\,T)^n}{n!}}^{\textit{Neglected Terms}} \qquad \textit{(IV-30)}$$

The main proposal here is to calculate $e^{A\,T}$ without any first order or second order approximations. In [108], the authors propose to diagonalize the matrix A enabling to find a new form for the discretized state-space representation. It is then possible to rewrite the discrete-time equation based on the eigenvectors of matrix A. That is:

$$e^{A\,T} = P\,e^{D\,T}\,P^{-1} \qquad \textit{(IV-31)}$$

Where D and P are, respectively, the diagonalized and transfer matrices of A. This approach will be used to derive the discrete-time models for MMC current [109] [127].

3.3.1.1. AC side modeling

Since the system of equation (IV-1) is being linear, it is possible to obtain its corresponding discrete-time model as:

$$\begin{bmatrix} i_d^{ac}(t_n+T) \\ i_q^{ac}(t_n+T) \end{bmatrix} = F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + G(T)\begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} \quad \textit{(IV-32)}$$

Based on the calculation of $e^{A\,T}$ with equation (IV-31), the matrices $F(T)$ (known as transition matrix) and $G(T)$ (known as input matrix) are given by:

$$F(T) = e^{A\,T} = \begin{bmatrix} e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)}\cos(T\omega) & e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)}\sin(T\omega) \\ -e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)}\sin(T\omega) & e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)}\cos(T\omega) \end{bmatrix}$$

$$G(T) = A^{-1}(e^{A\,T} - I)B = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix}$$

$$G_{11} = \frac{\omega L_{eq}^{ac}\,sin(T\omega)\,e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)} - R_{eq}^{ac}\,cos(T\omega)\,e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)} + R_{eq}^{ac}}{{L_{eq}^{ac}}^2\omega^2 + {R_{eq}^{ac}}^2}$$

$$G_{12} = -\frac{\omega L_{eq}^{ac}\,cos(T\omega)\,e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)} + R_{eq}^{ac}\,sin(T\omega)\,e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)} - \omega L_{eq}^{ac}}{{L_{eq}^{ac}}^2\omega^2 + {R_{eq}^{ac}}^2}$$

$$G_{21} = \frac{\omega L_{eq}^{ac}\,cos(T\omega)\,e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)} + R_{eq}^{ac}\,sin(T\omega)\,e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)} - \omega L_{eq}^{ac}}{{L_{eq}^{ac}}^2\omega^2 + {R_{eq}^{ac}}^2}$$

$$G_{22} = \frac{\omega L_{eq}^{ac}\,sin(T\omega)\,e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)} - R_{eq}^{ac}\,cos(T\omega)\,e^{-T\left(\frac{R_{eq}^{ac}}{L_{eq}^{ac}}\right)} + R_{eq}^{ac}}{{L_{eq}^{ac}}^2\omega^2 + {R_{eq}^{ac}}^2}$$

As said before and except the assumption that matrices A and B are time invariant between t_n and $t_n + T$, no additional simplifications or approximation are used unlike traditional method obtained by Euler or Tustin discretization.

3.3.1.2. DC side modeling

The same approach is applied to the continuous-time DC system (see equation (IV-2)). Using equation (IV-31), the exact discrete-time model can be extracted. That is:

$$\begin{bmatrix} i_a^{dc}(t_n+T) \\ i_b^{dc}(t_n+T) \\ i_c^{dc}(t_n+T) \end{bmatrix} = H(T) \begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} + K(T) \begin{bmatrix} v_{rla}^{dc}(t_n) \\ v_{rlb}^{dc}(t_n) \\ v_{rlc}^{dc}(t_n) \end{bmatrix} \qquad \textit{(IV-33)}$$

Where:

$$H(T) = e^{C\,T} = e^{-T\left(\frac{R_{eq}^{dc}}{L_{eq}^{dc}}\right)} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$K(T) = C^{-1}(e^{C\,T} - I)D = -\frac{e^{-T\left(\frac{R_{eq}^{dc}}{L_{eq}^{dc}}\right)} - 1}{R_{eq}^{dc}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

3.3.1.3. Models validation

The obtained discrete-time models as well as the approximated Euler based solution are compared by simulation to the continuous-time models which are considered here as reference test models, see Figure IV-20. The simulation has been carried out in Matlab/Simulink using Dormand-Prince (ode8) solver for continuous model with a fixed time-step (T_s) of 1 µs allowing to obtain the most accurate results.

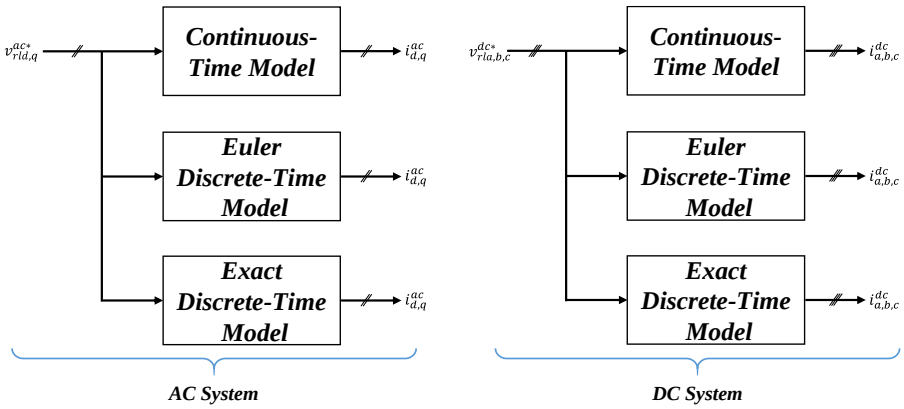

Figure IV-20: Simulation circuit for discrete-time models validation.

1) AC model validation

At the beginning, the time-step for the discrete models (Exact and Euler) is set to 10 µs. The test event is:

- Initially, v_{rlq}^{ac*} and v_{rld}^{ac*} are set to zero.
- At t=0.02 s, an increased step of 0.2 pu is applied to v_{rld}^{ac*}.

The corresponding results are duplicated in Figure IV-21 where the direct and quadrature components of AC current are illustrated in (a)-(b) respectively.

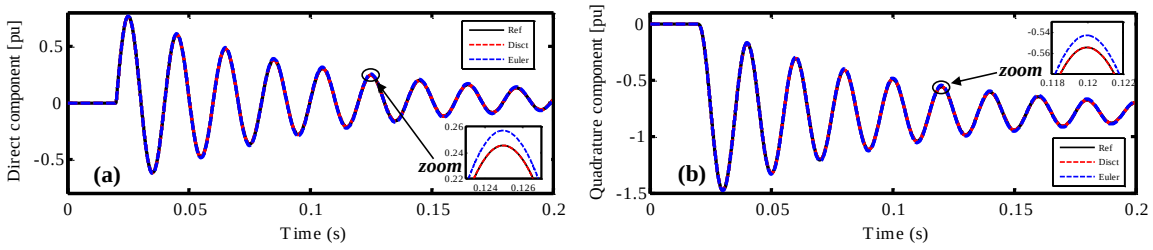

Figure IV-21: AC discrete-time models dynamics with 10 µs: (a) i_d^{ac}, (b) i_q^{ac}variations.

As it is observed in Figure IV-21, despite there is a small difference between Euler model and the reference one, no visible difference appears between the three simulated models.

Thereafter, the time-step for the discrete models (Exact and Euler) is increased while the reference continuous-time model is kept running with 1 µs time-step. The simulation results corresponding to 50 and 100 µs are presented in Figure IV-22 and Figure IV-23 respectively.

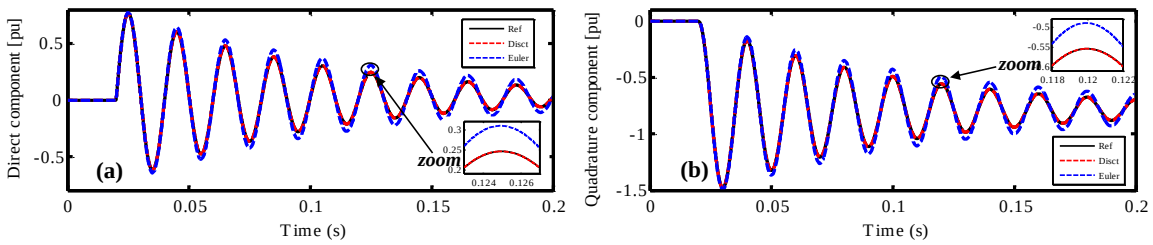

Figure IV-22: AC discrete-time models dynamics with 50 µs: (a) i_d^{ac}, (b) i_q^{ac}variations.

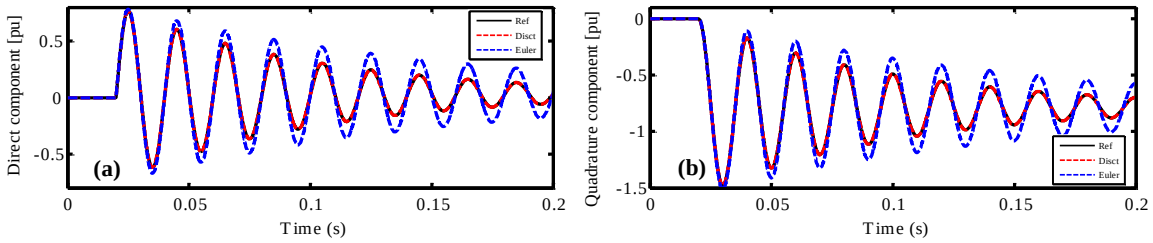

Figure IV-23: AC discrete-time models dynamics with 100 µs: (a) i_d^{ac}, (b) i_q^{ac} variations.

The obtained results in Figure IV-22 show that the response of the exact discrete-time model is identical to the reference one (continuous model) even for a large sampling period. This demonstrates a high degree of accuracy of the obtained discrete-time model with insensivity to the time-step increase. In contrast, the response of Euler discrete-time model is not sufficiently accurate. The difference between Euler discrete-time model and the reference one increases as the time-step becomes large (see Figure IV-23). This result reflects that the first or second order approximations are no longer valid when the sampling period increase. The risk with such approximate models is that the derived controls will be inaccurate highlighting unexpected behavior.

2) DC model validation

As before, different time-steps are chosen to validate the DC discrete-time models (10, 50 and 100 µs). The simulation event is a step change of 0.2 pu in v_{rla}^{dc*} at time t=0.02 s. The corresponding results for DC current of leg (a) are presented in Figure IV-24-(a) for 10 µs, Figure IV-24-(b) for 50 µs and Figure IV-24-(c) for 100 µs.

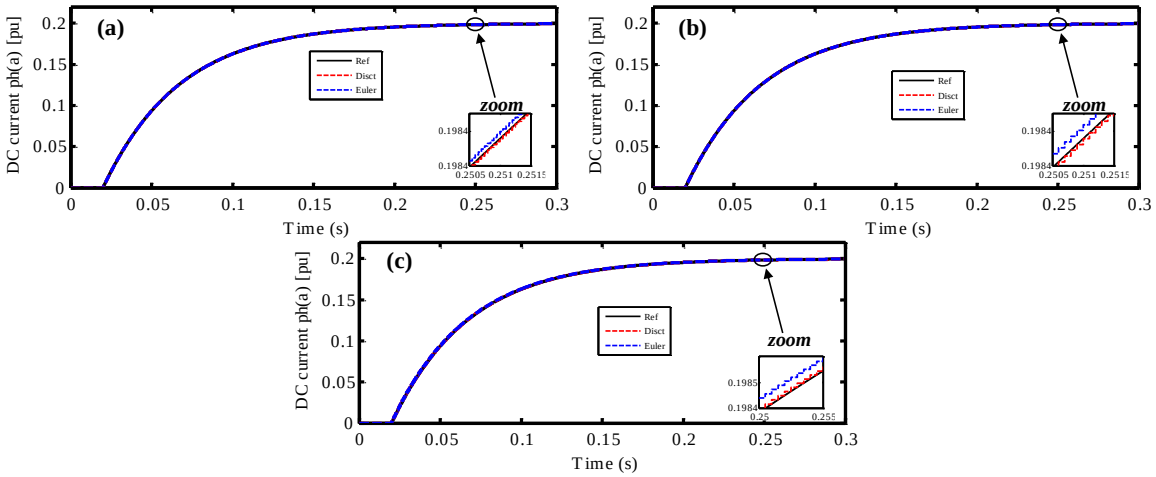

Figure IV-24: DC discrete-time models dynamics: i_a^{dc} variation with (a) 10 µs, (b) 50 µs and (c) 100 µs.

It can be concluded that both discrete-time models (Exact and Euler) give quite equivalent response as the reference one. Moreover, contrary to the results obtained with the AC discrete-time models, the error with Euler model is small enough even with a large time-step (100 µs). This result can be explained by the absence of coupling parameters in the state matrix C of the DC model making the transition matrix simple.

3.3.2. Discrete-time MMC control based on pole placement method

After obtaining the exact discrete-time models for MMC output currents and showing their accuracy, control laws can be derived using those models. It should be pointed out that all control laws can be used with those models. The objective here is to have the fastest current dynamics. To do so, pole placement control technique is used to derive the control law.

Considering the state-space model of equation (IV-28), the discrete-time controller based on pole placement method has to satisfy the following condition:

$$[X\,(t_n + T) - X^*] = K_g\,[X(t_n) - X^*] \qquad \textit{(IV-34)}$$

Where:

X^*: The reference value for state variable X.

K_g: Controller gain.

The controller gain K_g is chosen to place the poles in the unity circle as required for stability matters.

3.3.2.1. AC current control law

Based on the previous condition of equation (IV-34) and in order to force the tracking error to the origin, the discrete-time controller of the AC side has to satisfy the following condition:

$$\begin{bmatrix} i_d^{ac}(t_n + T) - i_d^{ac*} \\ i_q^{ac}(t_n + T) - i_q^{ac*} \end{bmatrix} = K_g^{ac} \begin{bmatrix} i_d^{ac}(t_n) - i_d^{ac*} \\ i_q^{ac}(t_n) - i_q^{ac*} \end{bmatrix} \qquad \textit{(IV-35)}$$

Where: K_g^{ac} is the tuning gain vector for AC system.

In order to set properly the tuning gain vector, the pole placement based stability analysis is presented below. Replacing $i_{d,q}^{ac}(t_n + T)$ by its expression (IV-32), equation (IV-35) becomes:

$$F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + G(T)\begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*} \\ i_q^{ac*} \end{bmatrix} = K_g^{ac}\begin{bmatrix} i_d^{ac}(t_n) - i_d^{ac*} \\ i_q^{ac}(t_n) - i_q^{ac*} \end{bmatrix} \quad \textit{(IV-36)}$$

Arranging (IV-36), the control law can be written as:

$$\begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} = G(T)^{-1}\left[-F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + K_g^{ac}\begin{bmatrix} i_d^{ac}(t_n) - i_d^{ac*} \\ i_q^{ac}(t_n) - i_q^{ac*} \end{bmatrix} + \begin{bmatrix} i_d^{ac*} \\ i_q^{ac*} \end{bmatrix}\right] \quad \textit{(IV-37)}$$

For control system theory, in particular for discrete-time control, stability analysis is mandatory to guarantee that all poles are in a suitable region of the complex plane. For this purpose, pole location is used to analyze the stability of the proposed controller in order to set the controller gains properly. In this analysis, only the dynamic of i_d^{ac} is presented. For the i_q^{ac} the same analysis can be derived using the same approach.

Using (IV-32) and (IV-37), the transfer function for i_d^{ac} in closed loop can be derived as follows.

$$TF_{i_d^{ac}}(Z) = \frac{i_d^{ac}(t_n + T)}{i_d^{ac*}} = \frac{1 - K_{g_{11}}^{ac}}{Z - K_{g_{11}}^{ac}} \quad \textit{(IV-38)}$$

Equation (IV-38) shows the active power dynamics regarding active power reference change. Using the same approach, the transfer function for active power dynamics regarding reactive power reference change can be written as follows:

$$TF_{i_d^{ac}}(Z) = \frac{i_d^{ac}(t_n + T)}{i_q^{ac*}} = \frac{1 - K_{g_{12}}^{ac}}{Z - K_{g_{12}}^{ac}} \quad \textit{(IV-39)}$$

For discrete-time domain, to ensure the stability of the system, all the poles have to be inside the unit circle. According to (IV-38) and (IV-39), the gain values which satisfy this condition are:

$$\begin{aligned} -1 \ll K_{g_{11}}^{ac} \ll 1 \\ -1 \ll K_{g_{12}}^{ac} \ll 1 \end{aligned} \quad \textit{(IV-40)}$$

By allocating the pole in the origin of equation (IV-38), the fastest dynamic response for i_d^{ac} can be ensured. The gain condition for Dead-Beat control is given by:

$$K_{g_{11}}^{ac} = 0 \tag{IV-41}$$

Since the equation (IV-37) allows to master the decoupling between active and reactive power, allocating the pole of equation (IV-39) in the origin allows to reduce the impact of reactive power reference change. That is:

$$K_{g_{12}}^{ac} = 0 \tag{IV-42}$$

The conditions (IV-41) and (IV-42) can be verified by replacing $v_{rld,q}^{ac}(t_n)$ in equation (IV-32) by their expressions obtained from equation (IV-37). That is:

$$\begin{bmatrix} i_d^{ac}(t_n+T) \\ i_q^{ac}(t_n+T) \end{bmatrix} = F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + G(T)\left[G(T)^{-1}\left[-F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + K_g^{ac}\begin{bmatrix} i_d^{ac}(t_n) - i_d^{ac*} \\ i_q^{ac}(t_n) - i_q^{ac*} \end{bmatrix} + \begin{bmatrix} i_d^{ac*} \\ i_q^{ac*} \end{bmatrix}\right]\right] \tag{IV-43}$$

By setting K_g^{ac} to zero, equation (IV-43) can be arranged as follows:

$$\begin{bmatrix} i_d^{ac}(t_n+T) \\ i_q^{ac}(t_n+T) \end{bmatrix} = \begin{bmatrix} i_d^{ac*} \\ i_q^{ac*} \end{bmatrix} \tag{IV-44}$$

Equation (IV-44) shows that the state variables i_d^{ac} and i_q^{ac} achieve the reference values after one sampling period as long as the control resources are sufficiently available.

When the Euler model is used to perform the control algorithm, the control law using pole placement method is given by the following expression:

$$\begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} = (B\,T)^{-1}\left[-(1+A\,T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + K_g^{ac}\begin{bmatrix} i_d^{ac}(t_n) - i_d^{ac*} \\ i_q^{ac}(t_n) - i_q^{ac*} \end{bmatrix} + \begin{bmatrix} i_d^{ac*} \\ i_q^{ac*} \end{bmatrix}\right] \tag{IV-45}$$

Taking in the account equation (IV-45), the expression of i_d^{ac} and i_q^{ac} becomes:

$$\begin{bmatrix} i_d^{ac}(t_n+T) \\ i_q^{ac}(t_n+T) \end{bmatrix} = F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + G(T)\left[(B\,T)^{-1}\left[-(1+A\,T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + K_g^{ac}\begin{bmatrix} i_d^{ac}(t_n)-i_d^{ac*} \\ i_q^{ac}(t_n)-i_q^{ac*} \end{bmatrix} + \begin{bmatrix} i_d^{ac*} \\ i_q^{ac*} \end{bmatrix}\right]\right] \quad \textit{(IV-46)}$$

By setting K_g^{ac} to zero, equation (IV-46) can be arranged as follows:

$$\begin{bmatrix} i_d^{ac}(t_n+T) \\ i_q^{ac}(t_n+T) \end{bmatrix} = \left(F(T) - G(T)(B\,T)^{-1}(1+A\,T)\right)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + G(T)(B\,T)^{-1}\begin{bmatrix} i_d^{ac*} \\ i_q^{ac*} \end{bmatrix} \quad \textit{(IV-47)}$$

Equation (IV-47) shows that the condition $K_g^{ac} = 0$ is not sufficient to obtain the fastest response. In addition to $K_g^{ac} = 0$, the following conditions have to be satisfied:

$$\begin{cases} G(T)(B\,T)^{-1} = I \\ F(T) - G(T)(B\,T)^{-1}(1+A\,T) = 0 \end{cases} \quad \textit{(IV-48)}$$

The conditions given in equations (IV-48) show that the sampling period has a big impact on the performance of the control algorithm derived from Euler discrete-time model. The proposed solution (exact discrete-time model) allows to solve this problem by ensuring the desired response.

3.3.2.2. DC current control law

As before and in order to satisfy the tracking conditions for DC side model, the following condition has to be satisfied:

$$\begin{bmatrix} i_a^{dc}(t_n+T) - i_a^{dc*} \\ i_b^{dc}(t_n+T) - i_b^{dc*} \\ i_c^{dc}(t_n+T) - i_c^{dc*} \end{bmatrix} = K_g^{dc}\begin{bmatrix} i_a^{dc}(t_n) - i_a^{dc*} \\ i_b^{dc}(t_n) - i_b^{dc*} \\ i_c^{dc}(t_n) - i_c^{dc*} \end{bmatrix} \quad \textit{(IV-49)}$$

Taking in the account the expression of $i_{a,b,c}^{dc}(t_n+T)$ (see equation (IV-33)), the control law for the DC system is given by the following expression:

$$\begin{bmatrix} v_{rla}^{dc}(t_n) \\ v_{rlb}^{dc}(t_n) \\ v_{rlc}^{dc}(t_n) \end{bmatrix} = K(T)^{-1} \left[-H(T) \begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} + K_g^{dc} \begin{bmatrix} i_a^{dc}(t_n) - i_a^{dc*} \\ i_b^{dc}(t_n) - i_b^{dc*} \\ i_c^{dc}(t_n) - i_c^{dc*} \end{bmatrix} + \begin{bmatrix} i_a^{dc*} \\ i_b^{dc*} \\ i_c^{dc*} \end{bmatrix} \right] \quad \textit{(IV-50)}$$

Using pole location analysis, the controller gains can be set properly. Taking the current i_a^{dc} as example, its transfer function in Z representation can be derived based on equations (IV-33) and (IV-50):

$$TF_{i_a^{dc}}(Z) = \frac{i_a^{dc}(t_n + T)}{i_a^{dc*}} = \frac{1 - K_{g_{11}}^{dc}}{Z + K_{g_{11}}^{dc}} \quad \textit{(IV-51)}$$

The stability of i_a^{dc} can be ensured by choosing the gain value according to the following conditions:

$$-1 \ll K_{g_{11}}^{dc} \ll 1 \quad \textit{(IV-52)}$$

The fast dynamics can be achieved by allocating the pole in the origin. That is

$$K_{g_{11}}^{dc} = 0 \quad \textit{(IV-53)}$$

The main advantage of pole placement technique is the possibility of setting the control gain within the unity circle but not necessary at the origin. This placement pole flexibility could be useful when the control outputs are saturated since that the proposed method does not take into account explicitly the limited resources of the control.

Consequently, a compromise between control dynamics and control resources (limitations) has to be taken into account in the gain tuning, especial when working at structural limitations. Of course, these limitations should be taken into account a priori in the control design. This work is not within the scope of the thesis and will be considered later.

Sliding mode discrete-time control could achieve this purpose without going deeply in the structural limitations analysis.

3.3.3. Discrete-time MMC control based on sliding mode control

In the following, the sliding mode control is applied to the discrete-time models given in equations (IV-32) and (IV-33). Considering the following sliding surfaces in instance t_n, defined as:

$$s_{ac}(t_n) = \begin{cases} s_1^{ac}(t_n) = \varepsilon_1^{ac}(t_n) \\ s_2^{ac}(t_n) = \varepsilon_2^{ac}(t_n) \end{cases}$$

$$s_{dc}(t_n) = \begin{cases} s_1^{dc}(t_n) = \varepsilon_1^{dc}(t_n) \\ s_2^{dc}(t_n) = \varepsilon_2^{dc}(t_n) \\ s_3^{dc}(t_n) = \varepsilon_3^{dc}(t_n) \end{cases} \quad \textit{(IV-54)}$$

Where:

$$\varepsilon_1^{ac}(t_n) = i_d^{ac}(t_n) - i_d^{ac*}(t_n)$$

$$\varepsilon_2^{ac}(t_n) = i_q^{ac}(t_n) - i_q^{ac*}(t_n)$$

$$\varepsilon_1^{dc}(t_n) = i_a^{dc}(t_n) - i_a^{dc*}(t_n)$$

$$\varepsilon_2^{dc}(t_n) = i_b^{dc}(t_n) - i_b^{dc*}(t_n)$$

$$\varepsilon_3^{dc}(t_n) = i_c^{dc}(t_n) - i_c^{dc*}(t_n)$$

The control laws can be obtained by setting the sliding surfaces in instance $t_n + T$ to zero, that are:

$$s_{ac}(t_n + T) = \begin{cases} s_1^{ac}(t_n + T) = i_d^{ac}(t_n + T) - i_d^{ac*}(t_n + T) = 0 \\ s_2^{ac}(t_n + T) = i_q^{ac}(t_n + T) - i_q^{ac*}(t_n + T) = 0 \end{cases}$$

$$s_{dc}(t_n + T) = \begin{cases} s_1^{dc}(t_n + T) = i_a^{dc}(t_n + T) - i_a^{dc*}(t_n + T) = 0 \\ s_2^{dc}(t_n + T) = i_b^{dc}(t_n + T) - i_b^{dc*}(t_n + T) = 0 \\ s_3^{dc}(t_n + T) = i_c^{dc}(t_n + T) - i_c^{dc*}(t_n + T) = 0 \end{cases} \quad \textit{(IV-55)}$$

Replacing $i_{d,q}^{ac}(t_n + T)$ and $i_{a,b,c}^{dc}(t_n + T)$ by their expressions (equations (IV-32) and (IV-33)), the equations (IV-55) in matrix form are given by:

$$F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + G(T)\begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n + T) \\ i_q^{ac*}(t_n + T) \end{bmatrix} = 0 \quad \textit{(IV-56)}$$

$$H(T)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} + K(T)\begin{bmatrix} v_{rla}^{dc}(t_n) \\ v_{rlb}^{dc}(t_n) \\ v_{rlc}^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix} = 0$$

Then, the control laws satisfying conditions (IV-56) are:

$$\begin{aligned} U_{ac}(t_n) &= \begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} = G(T)^{-1}\left[-F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix}\right] \\ U_{dc}(t_n) &= \begin{bmatrix} v_{rla}^{dc}(t_n) \\ v_{rlb}^{dc}(t_n) \\ v_{rlc}^{dc}(t_n) \end{bmatrix} = K(T)^{-1}\left[-H(T)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix}\right] \end{aligned} \quad \textit{(IV-57)}$$

It can be noted that, the control laws obtained with sliding mode control is a particular case ($k_g^{ac} = k_g^{dc} = 0$) of the obtained control laws with pole placement method (see equations (IV-37) and (IV-50)).

To be in line with sliding mode control design in continuous-time domain, the control law which ensures that the state variables are always equal to their references when the sliding motion is achieved, is stated "equivalent control" [110]. The obtained control laws of equations (IV-57) are rewritten as:

$$\begin{aligned} U_{ac}(t_n) = U_{eq}^{ac} &= \begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} = G(T)^{-1}\left[-F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix}\right] \\ U_{dc}(t_n) = U_{eq}^{ac} &= \begin{bmatrix} v_{rla}^{dc}(t_n) \\ v_{rlb}^{dc}(t_n) \\ v_{rlc}^{dc}(t_n) \end{bmatrix} = K(T)^{-1}\left[-H(T)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix}\right] \end{aligned} \quad \textit{(IV-58)}$$

Equations (IV-58) can be modified as function of sliding surfaces as follow:

$$\begin{aligned} U_{ac}(t_n) &= U_{eq}^{ac} + G(T)^{-1}s_{ac}(t_n) - G(T)^{-1}s_{ac}(t_n) \\ U_{dc}(t_n) &= U_{eq}^{dc} + K(T)^{-1}s_{dc}(t_n) - K(T)^{-1}s_{dc}(t_n) \end{aligned} \quad \textit{(IV-59)}$$

Replacing $s_{ac}(t_n)$, $s_{dc}(t_n)$, U_{eq}^{ac} and U_{eq}^{dc} by their expressions given in (IV-54) and (IV-58) respectively leads to the following expressions:

$$
\begin{aligned}
U_{ac}(t_n) &= -G(T)^{-1} s_{ac}(t_n) \\
&\quad - G(T)^{-1}\left[(F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n)\end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T)\end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n)\end{bmatrix}\right] \\
U_{dc}(t_n) &= -K(T)^{-1} s_{dc}(t_n) \\
&\quad - K(T)^{-1}\left[(H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n)\end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T)\end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n)\end{bmatrix}\right]
\end{aligned}
\qquad \textit{(IV-60)}
$$

As the control laws are constrained by structural limits of converter (control resources), the equivalent control cannot be higher than a given values "U_0^{ac}" and "U_0^{dc}". The bounds of equivalent control should be taken into account [110]

Taking in the account equations (IV-60), the following conditions have to be satisfied by the controllers. That are:

$$
\begin{aligned}
&\left\| -G(T)^{-1}\left[(F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n)\end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T)\end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n)\end{bmatrix}\right]\right\| \le U_0^{ac} \\
&\left\| -K(T)^{-1}\left[(H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n)\end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T)\end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n)\end{bmatrix}\right]\right\| \le U_0^{dc}
\end{aligned}
\qquad \textit{(IV-61)}
$$

When the previous conditions are not satisfied, a saturation of $U_{ac}(t_n)$ and $U_{dc}(t_n)$ takes place as follow:

$$
\begin{aligned}
U_{ac}(t_n) &= \begin{cases} U_{eq}^{ac} \; for \left\|U_{eq}^{ac}\right\| \le U_0^{ac} \\ U_0^{ac}\dfrac{U_{eq}^{ac}}{\left\|U_{eq}^{ac}\right\|} \; for \left\|U_{eq}^{ac}\right\| > U_0^{ac} \end{cases} \\
U_{dc}(t_n) &= \begin{cases} U_{eq}^{dc} \; for \left\|U_{eq}^{dc}\right\| \le U_0^{dc} \\ U_0^{dc}\dfrac{U_{eq}^{dc}}{\left\|U_{eq}^{dc}\right\|} \; for \left\|U_{eq}^{dc}\right\| > U_0^{dc} \end{cases}
\end{aligned}
\qquad \textit{(IV-62)}
$$

Using results of equations (IV-62), it should pointed out that the control outputs are saturated with control direction kept unchanged.

To prove the convergence of state variables to their references ($s = 0$), it is necessary to show that $\|s_{ac}(t_n + T)\| < \|s_{ac}(t_n)\|$ and $\|s_{dc}(t_n + T)\| < \|s_{dc}(t_n)\|$ for the two cases of equations (IV-62). For this purpose, based on equations (IV-56), the surfaces $s_{ac}(t_n + T)$ and $s_{dc}(t_n + T)$ are rewritten as function of $s_{ac}(t_n)$ and $s_{dc}(t_n)$ respectively. That are:

$$\begin{aligned} s_{ac}(t_n + T) = {} & F(T)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} + G(T)\begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n + T) \\ i_q^{ac*}(t_n + T) \end{bmatrix} - s_{ac}(t_n) + s_{ac}(t_n) \\ s_{dc}(t_n + T) = {} & H(T)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} + K(T)\begin{bmatrix} v_{rla}^{dc}(t_n) \\ v_{rlb}^{dc}(t_n) \\ v_{rlc}^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n + T) \\ i_b^{dc*}(t_n + T) \\ i_c^{dc*}(t_n + T) \end{bmatrix} - s_{dc}(t_n) + s_{dc}(t_n) \end{aligned} \quad \textit{(IV-63)}$$

Replacing $s_{ac}(t_n)$ and $s_{dc}(t_n)$ by their expressions (see equations (IV-54)) leads to:

$$\begin{aligned} s_{ac}(t_n + T) = {} & s_{ac}(t_n) + (F(T) - I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n + T) \\ i_q^{ac*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} \\ & + G(T)\begin{bmatrix} v_{rld}^{ac}(t_n) \\ v_{rlq}^{ac}(t_n) \end{bmatrix} \\ s_{dc}(t_n + T) = {} & s_{dc}(t_n) + (H(T) - I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n + T) \\ i_b^{dc*}(t_n + T) \\ i_c^{dc*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} \\ & + K(T)\begin{bmatrix} v_{rla}^{dc}(t_n) \\ v_{rlb}^{dc}(t_n) \\ v_{rlc}^{dc}(t_n) \end{bmatrix} \end{aligned} \quad \textit{(IV-64)}$$

Considering the worst case when $\|U_{eq}^{ac}\| > \|U_0^{ac}\|$ and $\|U_{eq}^{dc}\| > \|U_0^{dc}\|$, from equations (IV-62), the sliding surfaces $s_{ac}(t_n + T)$ and $s_{dc}(t_n + T)$ become:

$$\begin{aligned} s_{ac}(t_n + T) = {} & s_{ac}(t_n) + (F(T) - I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n + T) \\ i_q^{ac*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} \\ & + G(T)U_0^{ac}\frac{U_{eq}^{ac}}{\|U_{eq}^{ac}\|} \\ s_{dc}(t_n + T) = {} & s_{dc}(t_n) + (H(T) - I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n + T) \\ i_b^{dc*}(t_n + T) \\ i_c^{dc*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} \\ & + K(T)U_0^{dc}\frac{U_{eq}^{dc}}{\|U_{eq}^{dc}\|} \end{aligned} \quad \textit{(IV-65)}$$

Taking into account equations (IV-60) in equations (IV-65) leads to:

$$s_{ac}(t_n+T) = s_{ac}(t_n) + (F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} + G(T)U_0^{ac}\frac{-G(T)^{-1}s_{ac}(t_n) - G(T)^{-1}(F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix}}{\left\|U_{eq}^{ac}\right\|} + G(T)U_0^{ac}\frac{+G(T)^{-1}\begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix} - G(T)^{-1}\begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix}}{\left\|U_{eq}^{ac}\right\|}$$

$$s_{dc}(t_n+T) = s_{dc}(t_n) + (H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} + K(T)U_0^{dc}\frac{-K(T)^{-1}s_{dc}(t_n) - K(T)^{-1}\left[(H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix}\right]}{\left\|U_{eq}^{dc}\right\|} + K(T)U_0^{dc}\frac{+K(T)^{-1}\begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix} - K(T)^{-1}\begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix}}{\left\|U_{eq}^{dc}\right\|} \quad \textit{(IV-66)}$$

Arranging equations (IV-66) gives:

$$s_{ac}(t_n+T) = \left(s_{ac}(t_n) + (F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix}\right)\left(1 - \frac{U_0^{ac}}{\left\|U_{eq}^{ac}\right\|}\right)$$

$$s_{dc}(t_n+T) = \left(s_{dc}(t_n) + (H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix}\right)\left(1 - \frac{U_0^{dc}}{\left\|U_{eq}^{dc}\right\|}\right) \quad \textit{(IV-67)}$$

Calculating the norm of $s_{ac}(t_n+T)$ and $s_{dc}(t_n+T)$, that is:

$$\|s_{ac}(t_n+T)\| = \left\| s_{ac}(t_n) + (F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} \right\| \left(1 - \frac{U_0^{ac}}{\|U_{eq}^{ac}\|}\right)$$

$$\|s_{ac}(t_n+T)\| \leq \left\| s_{ac}(t_n) + (F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} \right\| + \left\| s_{ac}(t_n) + (F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} \right\| \frac{-U_0^{ac}}{\|U_{eq}^{ac}\|}$$

$$\|s_{dc}(t_n+T)\| = \left\| s_{dc}(t_n) + (H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} \right\| \left(1 - \frac{U_0^{dc}}{\|U_{eq}^{dc}\|}\right) \quad \textit{(IV-68)}$$

$$\|s_{ac}(t_n+T)\| \leq \left\| s_{dc}(t_n) + (H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} \right\| + \left\| s_{dc}(t_n) + (H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} \right\| \frac{-U_0^{dc}}{\|U_{eq}^{dc}\|}$$

According to equation (IV-60), the norm of $\|U_{eq}^{ac}\|$ and $\|U_{eq}^{dc}\|$can be written as:

$$\|U_{eq}^{ac}\| = \|G(T)^{-1}\| \left\| s_{ac}(t_n) + (F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} \right\| \quad \textit{(IV-69)}$$

$$\left\|U_{eq}^{dc}\right\| = \|K(T)^{-1}\| \left\| s_{dc}(t_n) + (H(T) - I) \begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n + T) \\ i_b^{dc*}(t_n + T) \\ i_c^{dc*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} \right\|$$

Combining equations (IV-69) and (IV-68) yields to:

$$\|s_{ac}(t_n + T)\| \leq \left\| s_{ac}(t_n) + (F(T) - I) \begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n + T) \\ i_q^{ac*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} \right\| - \frac{U_0^{ac}}{\|G(T)^{-1}\|}$$

$$\|s_{dc}(t_n + T)\| \leq \left\| s_{dc}(t_n) + (H(T) - I) \begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n + T) \\ i_b^{dc*}(t_n + T) \\ i_c^{dc*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} \right\| - \frac{U_0^{dc}}{\|K(T)^{-1}\|} \quad \textit{(IV-70)}$$

Rewriting equations (IV-70) leads to the following expressions:

$$\|s_{ac}(t_n + T)\| \leq \|s_{ac}(t_n)\| + \left\| (F(T) - I) \begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n + T) \\ i_q^{ac*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix} \right\| - \frac{U_0^{ac}}{\|G(T)^{-1}\|}$$

$$\|s_{dc}(t_n + T)\| \leq \|s_{dc}(t_n)\| + \left\| (H(T) - I) \begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n + T) \\ i_b^{dc*}(t_n + T) \\ i_c^{dc*}(t_n + T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix} \right\| - \frac{U_0^{dc}}{\|K(T)^{-1}\|} \quad \textit{(IV-71)}$$

In order to ensure that$\|s_{ac}(t_n + T)\| \leq \|s_{ac}(t_n)\|$ and $\|s_{dc}(t_n + T)\| \leq \|s_{dc}(t_n)\|$, the following conditions have to be satisfied:

$$\left\|(F(T)-I)\begin{bmatrix} i_d^{ac}(t_n) \\ i_q^{ac}(t_n) \end{bmatrix} - \begin{bmatrix} i_d^{ac*}(t_n+T) \\ i_q^{ac*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_d^{ac*}(t_n) \\ i_q^{ac*}(t_n) \end{bmatrix}\right\| - \frac{U_0^{ac}}{\|G(T)^{-1}\|} < 0$$

$$\left\|(H(T)-I)\begin{bmatrix} i_a^{dc}(t_n) \\ i_b^{dc}(t_n) \\ i_c^{dc}(t_n) \end{bmatrix} - \begin{bmatrix} i_a^{dc*}(t_n+T) \\ i_b^{dc*}(t_n+T) \\ i_c^{dc*}(t_n+T) \end{bmatrix} + \begin{bmatrix} i_a^{dc*}(t_n) \\ i_b^{dc*}(t_n) \\ i_c^{dc*}(t_n) \end{bmatrix}\right\| - \frac{U_0^{dc}}{\|K(T)^{-1}\|} < 0 \quad \textit{(IV-72)}$$

From equations (IV-61), it can be concluded that the above conditions are verified.

3.3.4. Control laws validation

In this section, the control laws (IV-37) and (IV-50) are tested by simulation using the continuous-time models (see Figure IV-25) where the parameters are given in Table IV-3.

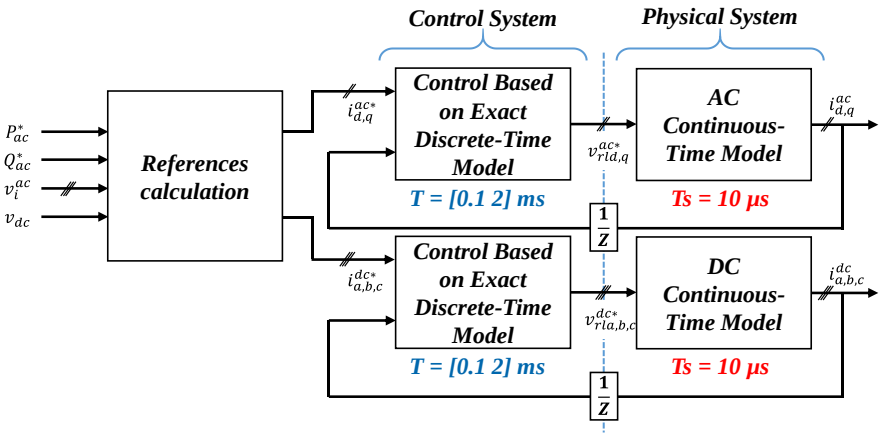

Figure IV-25: Simulation circuit for discrete-time controller validation.

3.3.4.1. Gain vector tuning

In this section, the response of the proposed controllers is investigated regarding the gain vector values. For the following test, the sampling period of the control algorithms is set to 0.5 ms.

The event is a step change of 0.2 pu in active power reference which is initially set to zero. Three values for gain vector elements (K_g^{ac}, K_g^{dc}) are used to highlight their effect: (-0.3,-0.3), (0,0) and (0.3,0.3).

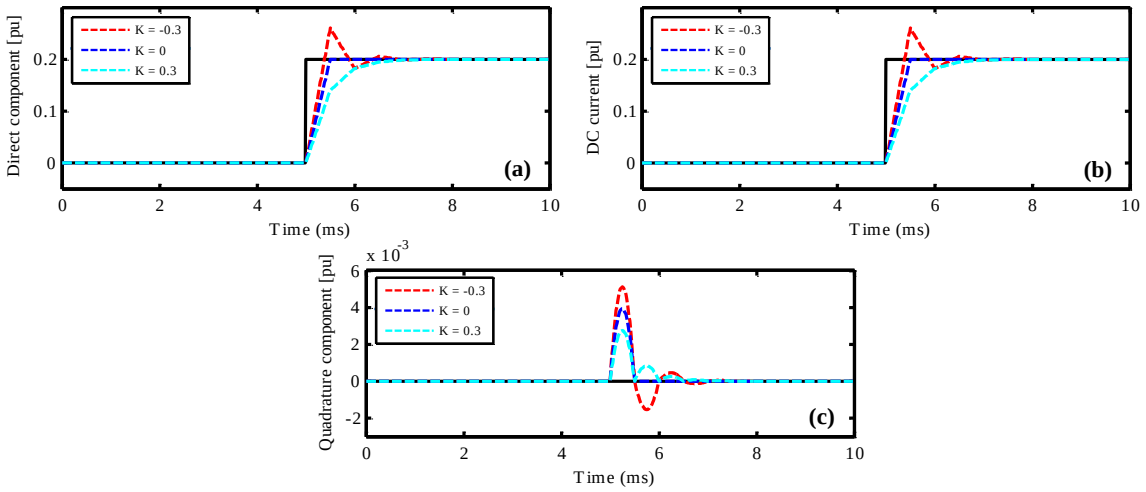

Figure IV-26: Proposed controllers dynamics with different gain values: (a) direct component for AC currents, (B) DC current, (c) quadrature component for AC currents.

The corresponding results; direct component of AC currents, DC current and quadrature component of AC currents are presented in Figure IV-26 (a)-(c) respectively. It can be observed that, when the gain is set to -0.3, the poles of system become negative leading to a second order response. For 0.3 and 0 values, the dynamics of system is a first order response. As it was proved in the theoretical analysis (see equations (IV-41) and (IV-53)), the high dynamics response (one sampling period) is obtained when the gain values are equal to zero.

3.3.4.2. Sampling period effect

To investigate the performances of the proposed controllers regarding the sampling period value, the following test cases are carried out.

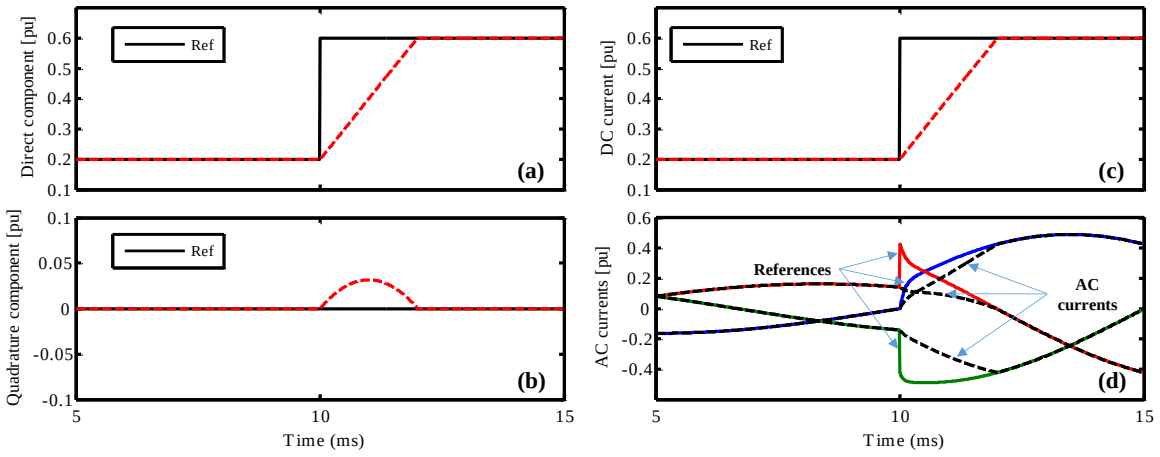

Figure IV-27: Proposed controllers dynamics with 2 ms sampling period: (a) direct component for AC currents, (b) quadrature component for AC currents, (c) DC current, (d) three phase AC currents.

The first test is to evaluate the AC and DC control laws with 2 ms sampling period to highlight the advantage of the proposed solution. Initially the reference of P_{ac}^{*} is set to 0.2 pu; at t= 10 ms it is increased to 0.6 pu. The corresponding results are presented in Figure IV-27, where the direct component, quadrature component, DC current and three phase AC currents variation are illustrated in (a)-(d) respectively.

The results show that the proposed control can ensure the desired dynamics which is one sampling period response (2 ms). The three phase components highlight disturbances until the direct component has achieved its reference.

Thereafter, to test the performances of the proposed controllers, the sampling period of the control algorithms is decreased. For this purpose, different values have been chosen: 0.1, 0.5 and 1 ms. The event is a step change in active power reference P_{ac}^{*}. Initially set to 0.2 pu, an increased step of 0.1 pu is applied at t= 0.1 s.

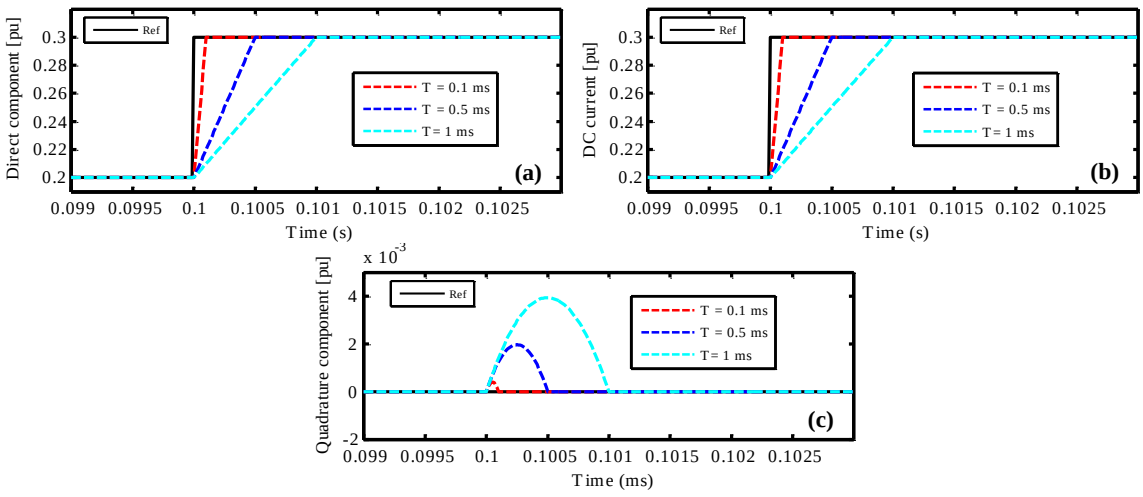

Figure IV-28: Proposed controllers dynamics with different sampling periods: (a) direct component for AC currents, (b) DC current, (c) quadrature component for AC currents.

The obtained results (see Figure IV-28) show the performances of the proposed control in terms of overshoots and dynamic responses. As the sampling period increases, the response time also increases while the control performances are kept equivalent (same response type).

3.3.4.3. Comparison with other solution

In this section, the proposed control algorithms are compared with a discrete-time controller based on Euler discrete-time model. For this purpose, two sampling periods (0.5 and 2 ms) have

been used to highlight the effects on control dynamics. The gain values have been set to ensure the fastest dynamics (i.e. poles located in the origin). The test case is a step increase of 0.1 pu in active power reference initially set to 0.2 pu.

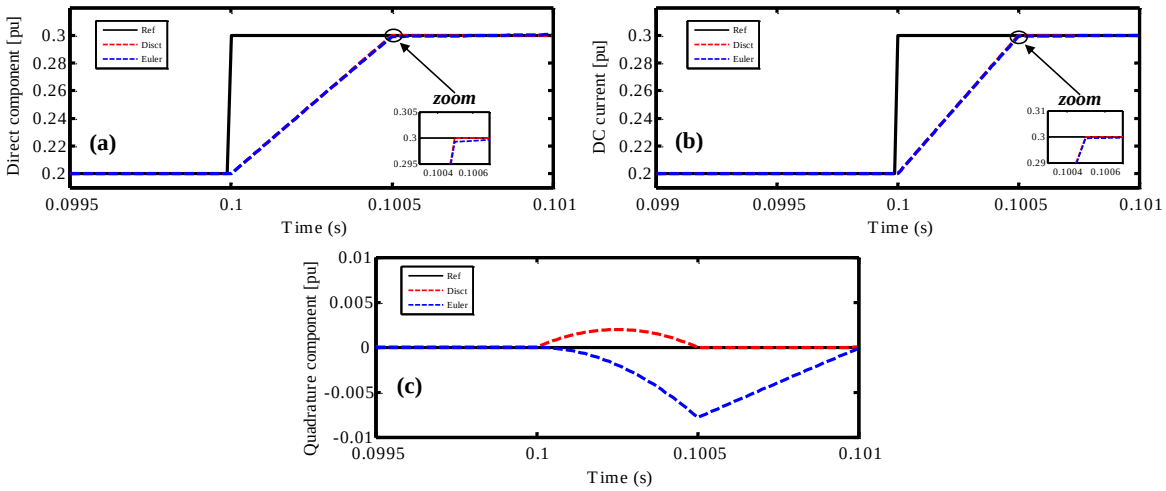

Figure IV-29: Discrete-time controllers performances with 0.5 ms sampling period: (a) direct component for AC currents, (b) DC current, (c) quadrature component for AC currents.

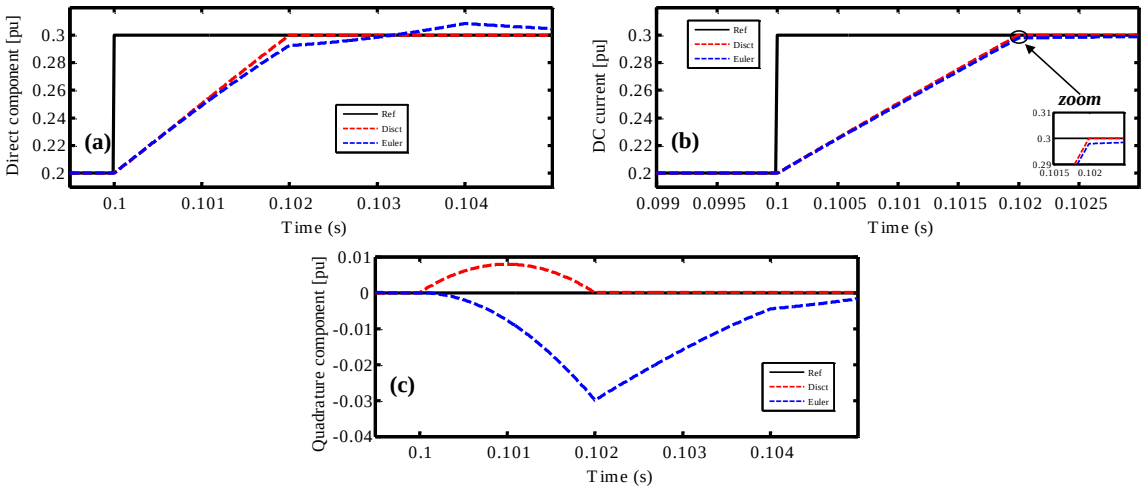

Figure IV-30: Discrete-time controllers performances with 2 ms sampling period: (a) direct component for AC currents, (b) DC current, (c) quadrature component for AC currents.

The corresponding results are presented in Figure IV-29 for 0.5 ms and Figure IV-30 for 2 ms sampling periods. It can be remarked that the dynamics of the controller derived from Euler model is close to the one derived from the exact discrete-time model when the sampling period is 0.5 ms. It means that, by decreasing more and more the sampling period, the dynamics of the two controllers is similar. However, a small sampling period cannot be used since it can interfere with low level control and consequently deteriorated the stability margins.

When the sampling period is increased (2 ms), the controller cannot perform high dynamics response (Dead-Beat response) when the Euler model is used. It achieves the reference after 3 sampling periods with an overshoot. On the other hand, the controller obtained from the exact discrete-time model converges in one sampling period. Moreover, the perturbation on quadrature component is well mitigated using the exact discrete-time model compared to the Euler model. This test shows that the approximation introduced by the Euler model affects the desired response and creates an unexpected behavior. The proposed controller allows to avoid such problems by ensuring the expected performances.

3.4. Offline validation of proposed controllers

After validation of proposed control algorithms on simplified models, in this section, they are incorporated in the whole control system (outer loops + low level control) presented in CHAPTER III, see section 5, to control MMC station represented with the full order detailed model using semi-analytical implementation (see section 4.1.1). The simulations have been carried out in Matlab/Simulink where its associated circuit is presented in Figure IV-31.

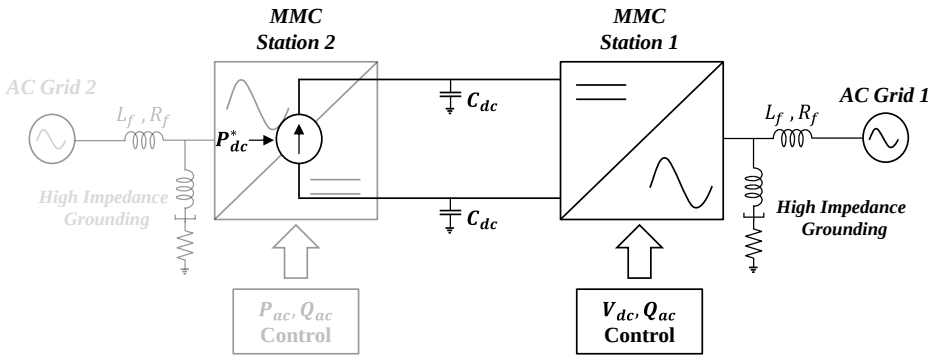

Figure IV-31: Simulation circuit for offline control validation.

3.4.1. Control in normal operation

3.4.1.1. High dynamics test (Step change of reactive power)

Since the reference of active power is given by DC voltage controller (PI) (see Figure III-40), it is better to test the high dynamics response of the proposed control on the reactive power reference. Initially, the converter is consuming 0.4 (pu) active power (power flows from AC to DC grids) and delivering 0.4 (pu) reactive power. At t=0.5 s, the reactive power reference is reversed from 0.4 to -0.4 pu. A sampling period of 200 µs has been chosen to perform this test.

The simulation results are shown in Figure IV-32, where the active and reactive powers, DC current with DC voltage, AC voltages, AC currents, upper arm currents, lower arm currents and averaged SM voltages for upper and lower arms are illustrated in (a)-(h) respectively.

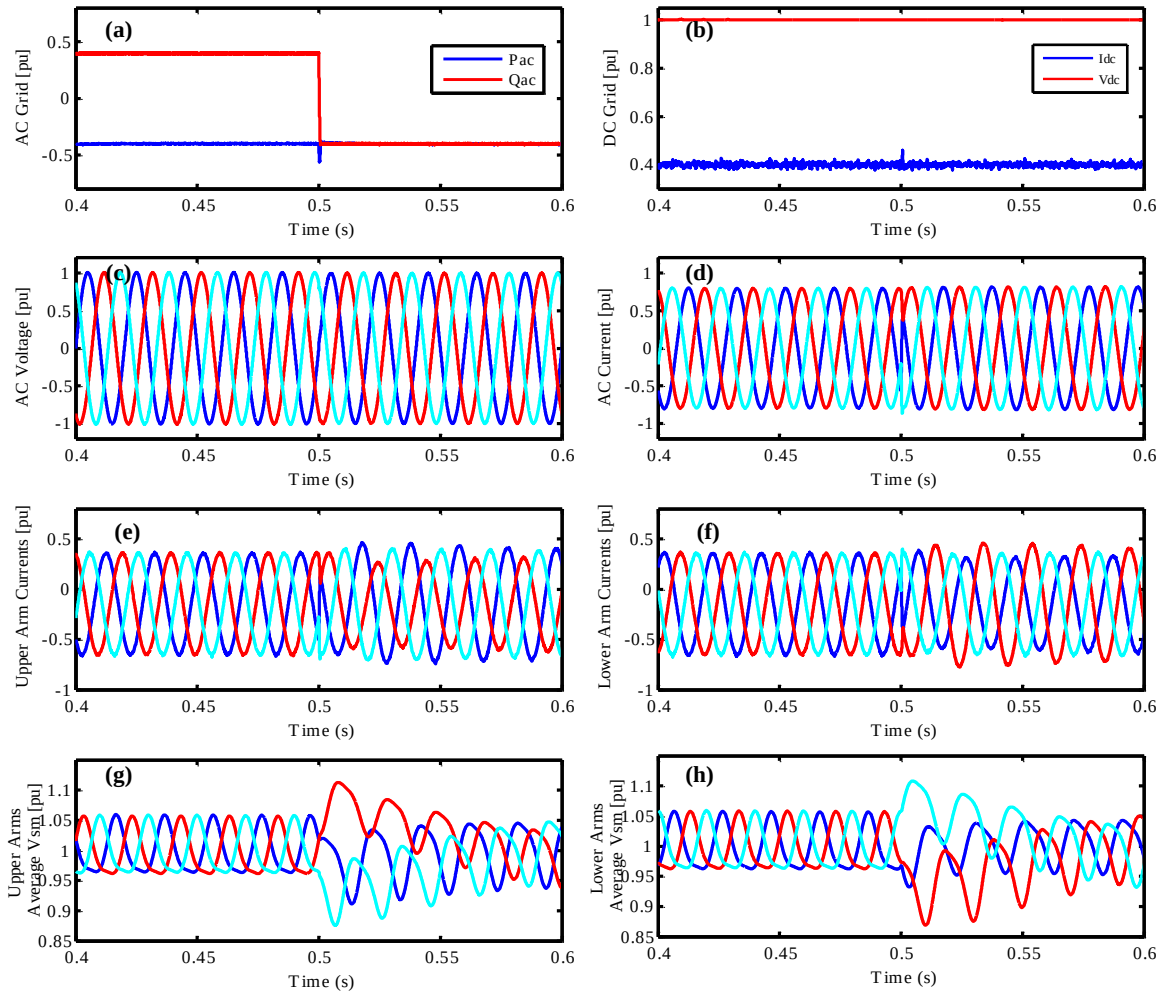

Figure IV-32: Simulation results with 0.2 ms sampling period: (a) active and reactive power, (b) DC current with DC voltage, (c) AC voltages, (d) AC currents, (e) upper arm currents, (f) lower arm currents, (g) average SM voltages for upper arms, (h) average SM voltages for lower arms.

Figure IV-32-(a) shows that the control changes rapidly the reactive power direction as it is requested by its reference. This result can be confirmed with AC current and AC voltage waveforms (see Figure IV-32-(d) and Figure IV-32-(c)). Thanks to the proposed control, no overcurrent is produced in the AC currents as well as the arm ones (see Figure IV-32-(e) and Figure IV-32-(f)). However, a small active power drop is observed during transient which could be attributed to the fact that the decoupling between active power and reactive one is related to the Phase Lock Loop (PLL) which will not hold during transient. This variation leads to a small perturbation in the DC current, see Figure IV-32-(b). Due to the high dynamics applied by the

current controllers, an unbalance condition has appeared on SM voltages when the step is applied (see Figure IV-32-(g) and Figure IV-32-(h)). Thanks to energy balancing loops, a balanced situation will be established after 100 ms.

A zoom on reactive power is illustrated in Figure IV-33-(a) where the reactive power seen by the control and the measurement coming from model are compared to the reference.

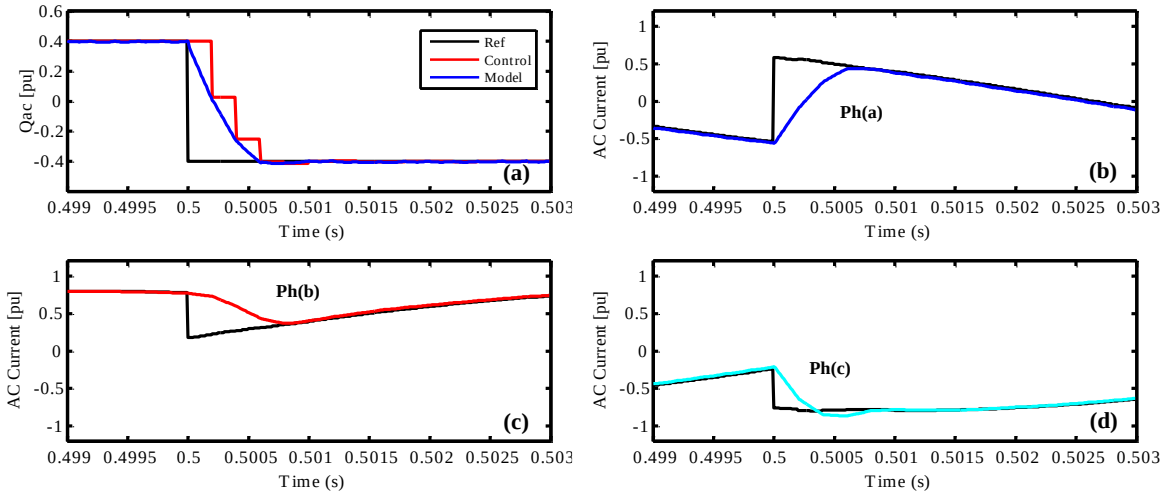

Figure IV-33 Zoom on simulation results with 0.2 ms sampling period: (a) reactive power, (b) AC current phase (a), (b) AC current phase (b), (b) AC current phase (c).

Thanks to the proposed controller, the converter changes its reactive power as it is required by the reference in a minimum time (less than 1 ms), the control requires four sampling periods to achieve the applied reference (-0.8 pu). On the other hand, the AC currents follow the references change and converge in four sampling period also (less than1 ms) as it is shown in Figure IV-33-(b), Figure IV-33- (c) and Figure IV-33-(d).

In order to assess our proposed control, it has been compared with the solution presented in the literature “Dead-beat” controller based on Euler discretized model. The simulation results, for the same event and same sampling period as previously, are shown in Figure IV-34 where the reactive power measurement and reactive power seen by control are illustrated in (a)-(b). Figure IV-34-(b) shows that the proposed controller gives a faster response than the other controller without overshoot. Figure IV-34-(a) shows that the Euler based controller takes more than 4 sampling periods to achieve the reference.

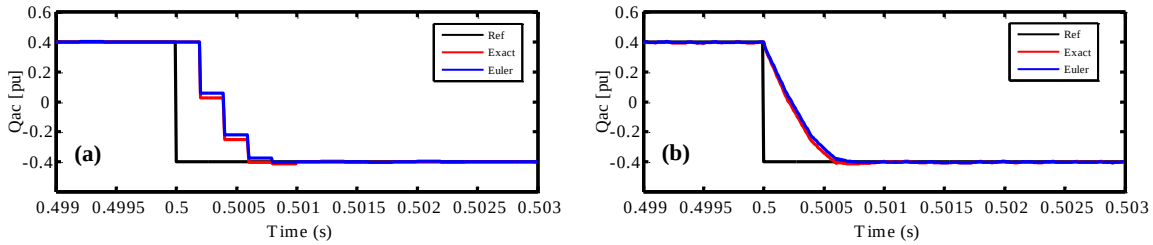

Figure IV-34: Reactive power for different controllers with 0.2 ms sampling period: (a) measurement, (b) seen by control.

The same event has been tested with 0.5 ms sampling period. The experimental results are illustrated in Figure IV-35. Since the sampling period increases, the difference between the proposed control and Euler based one becomes more and more important. It is also observed that the proposed discrete-time controller has the same response time (1 ms) to achieve the reference whatever is the control sampling period which is not possible using Euler based controller.

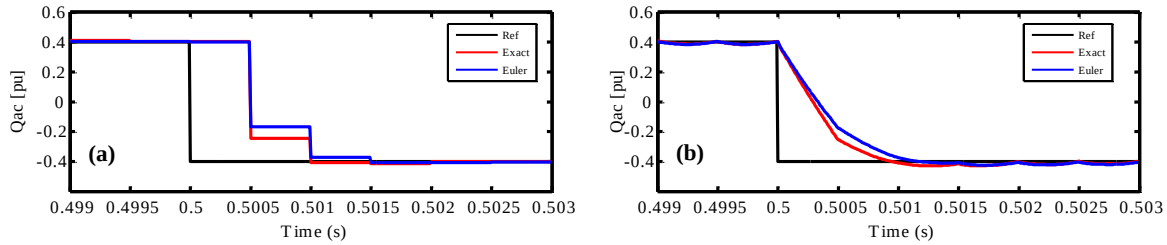

Figure IV-35: Reactive power for different controllers with 0.5 ms sampling period: (a) measurement, (b) seen by control.

3.4.1.2. Energy reference step

In this section, the time response of energy loop is investigated with the proposed current controllers. For this purpose, at t=1s the reference of energy loop is changed from 1 pu to 0.95 pu. The *PI* controller gains have been tuned for different response time values: 5, 10, 30 and 50 ms.

As a reminder, the considered high level control allows to manage the energy control strategy using energy parameter α_w. Two values are considered for this test: $\alpha_w = 0$ for AC grid control strategy and $\alpha_w = 1$ for DC grid control strategy (see section 5.2.1).

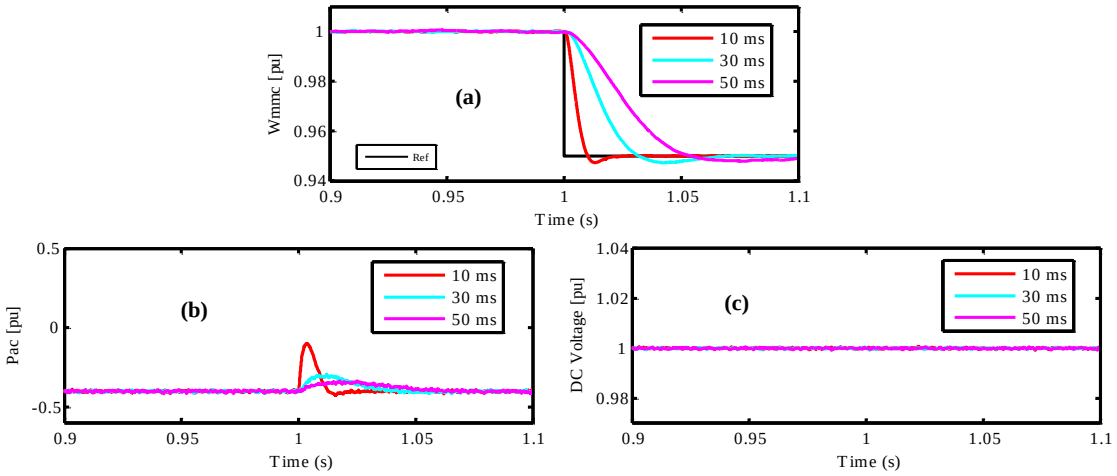

Figure IV-36: Simulation results with different energy loop time response ($\alpha_W = 0$): (a) MMC energy, (b) active power, (c) DC voltage.

The simulation results presented in Figure IV-36 have been obtained with $(\alpha_w = 0)$ corresponding to AC grid control strategy for energy loop. From these results, it is observed that the energy stored inside the arm decrease as it is requested by energy reference. The response time as well as the overshoot are well respected for all response time values. Since the response time decrease, the impact in the AC grid becomes bigger.

The same test case is applied with $(\alpha_w = 1)$ corresponding to DC grid control strategy for energy regulation. The simulation results with different energy loop response time are shown in Figure IV-37, where the MMC energy, active power and DC voltage are illustrated in (a)-(c) respectively. It can be noted that, whatever is the control strategy for energy loop, the dynamics of energy loop is well respected in term of response time and overshoot.

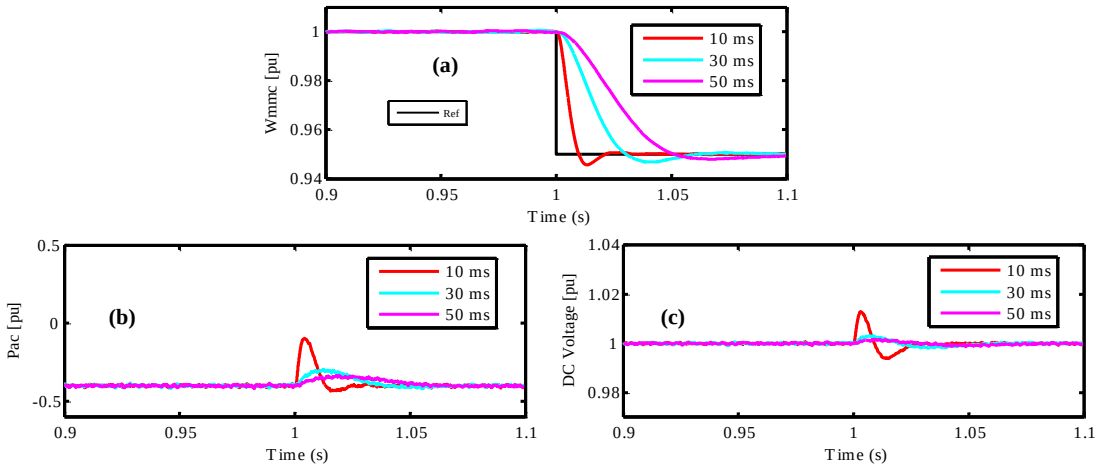

Figure IV-37: Simulation results with different energy loop time response ($\alpha_W = 1$): (a) MMC energy, (b) Active power, (c) DC voltage.

3.4.2. Control against external events

In this section, the behavior of the proposed control versus external disturbances is investigated.

3.4.2.1. Symmetric ac voltage dip

At t=1.5 s, in order to emulate a three phase fault located far from the station, the AC voltage amplitude is decreased by 50% during 100 ms. Before the event, the MMC is sending 0.2 pu active power to the DC source and doesn't exchange reactive power with the AC grid. The simulation results are shown in Figure IV-38, where the active with reactive powers, DC current with DC voltage, AC voltages, AC currents, upper arm currents, lower arm currents, average SM voltages for upper arms and average SM voltages for lower arms are presented in (a)-(h) respectively. Thanks to the high dynamics of inner loops, the MMC can increase rapidly its AC current (without any overcurrent in the arms) in order to maintain the same power requested by DC source. Since the current increases, the conduction losses inside the converter increase also leading to a small variation of active power and increasing of capacitor voltages ripple. It can be observed that no perturbations are seeing in the DC grid components (see Figure IV-38-(b)).

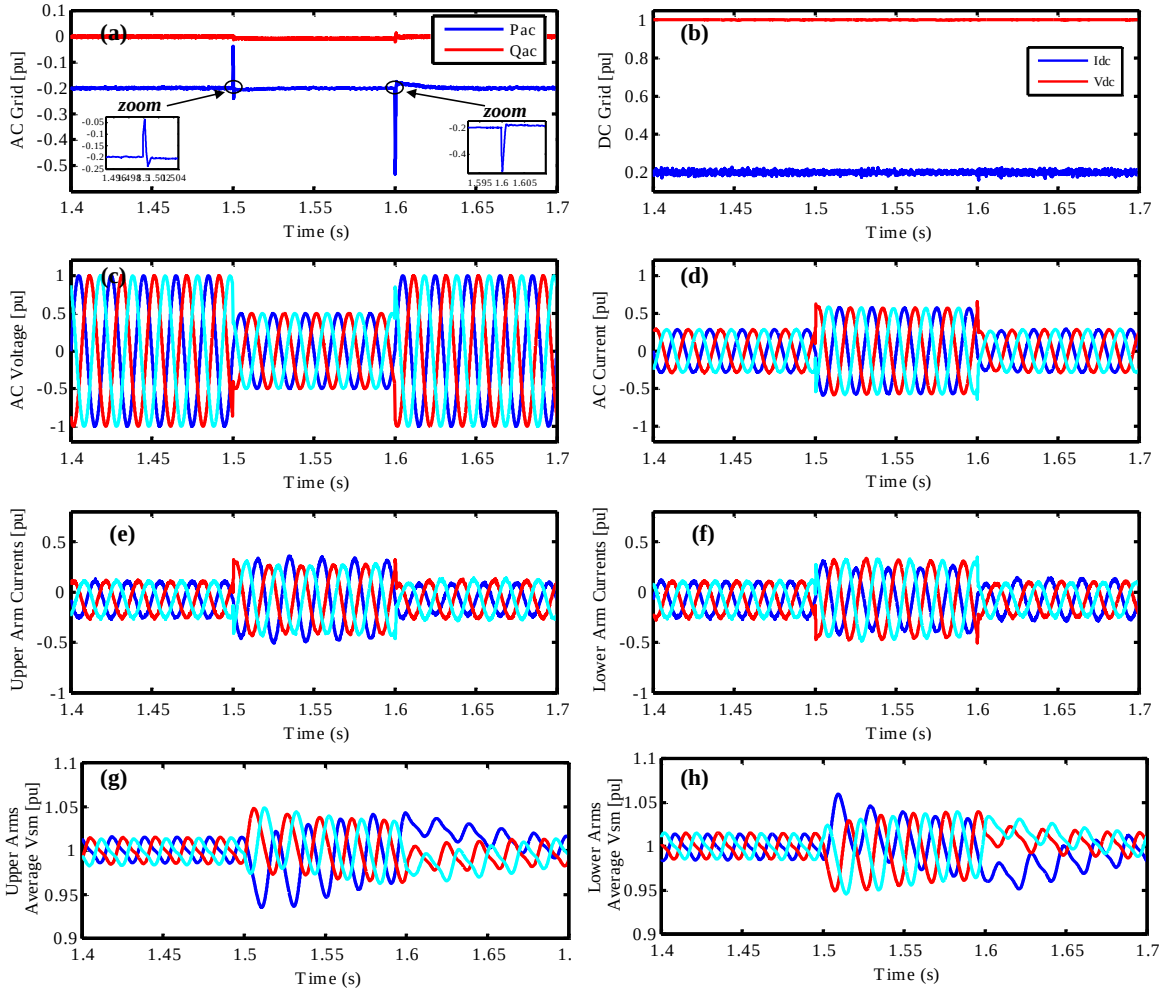

Figure IV-38: Simulation results for symmetrical AC voltage dip with 0.2 ms sampling period: (a) active and reactive power, (b) DC current with DC voltage, (c) AC voltages, (d) AC currents, (e) upper arm currents, (f) lower arm currents, (g) average SM voltages for upper arms, (h) average SM voltages for lower arms.

3.4.2.2. Asymmetric ac voltage dip

For asymmetric fault located far from the station, the AC voltage amplitude for two phases is decreased by 50% a t=2s during 100 ms. Initially, the MMC is sending 0.2 pu active power to the DC source and doesn't exchange reactive power with the AC grid.

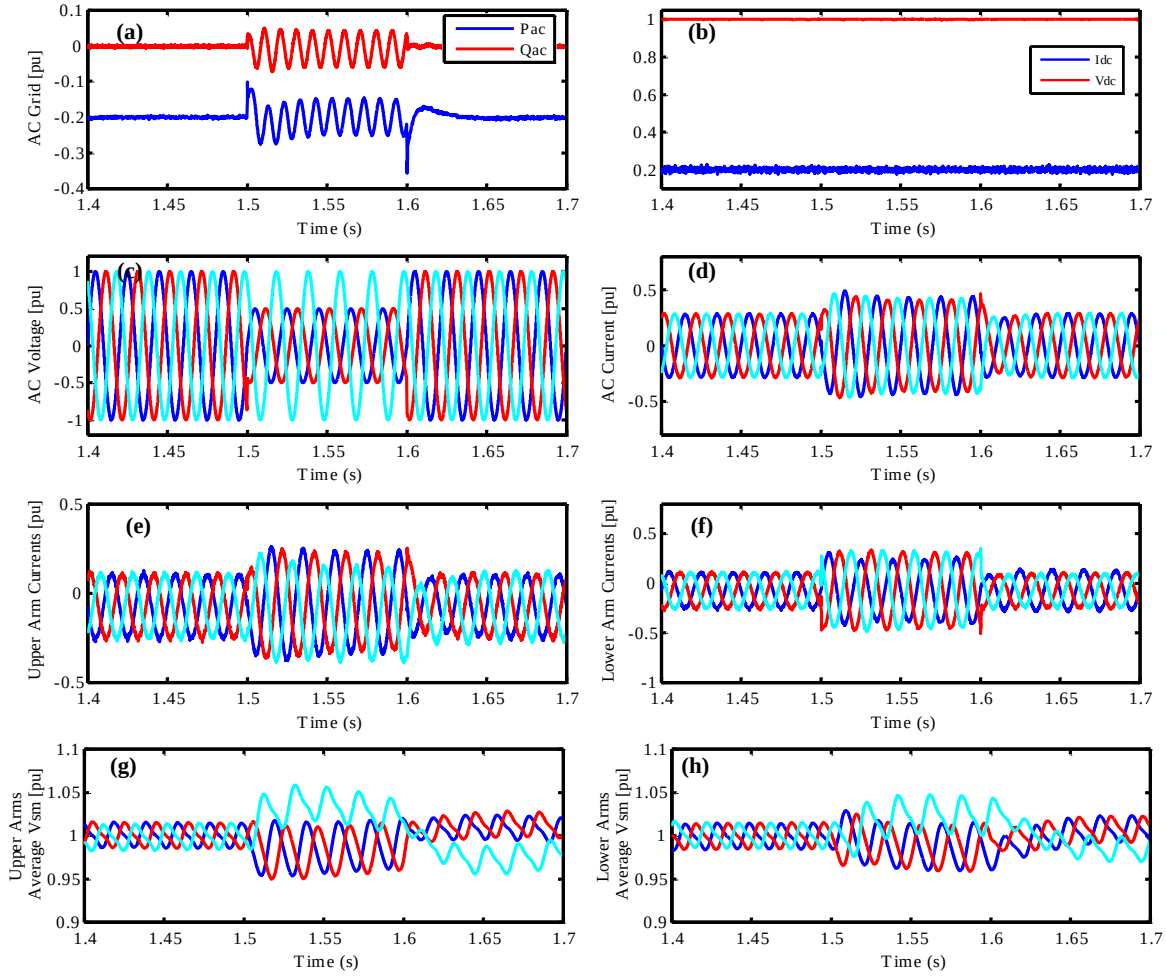

Figure IV-39: Simulation results for Asymmetrical AC voltage dip with 0.2 ms sampling period: (a) Active and reactive power, (b) DC current with DC voltage, (c) AC voltages, (d) AC currents, (e) Upper arm currents, (f) lower arm currents, (g) Average SM voltages for upper arms, (h) Average SM voltages for lower arms.

The simulation results are presented in Figure IV-39. It can be observed that the proposed current controllers allow maintaining power as requested by the DC current source during and after the event. Despite the unbalance of AC voltages, the AC current controller can balance the resulting AC currents (see Figure IV-39-(c) and Figure IV-39-(d)). As a result, the active as well as reactive powers start oscillating with double frequency of AC grid (see Figure IV-39-**(a)**). Thanks to the decoupling between the AC and DC grids, the applied event is damped by the stored energy inside the MMC (see Figure IV-39-(g) and Figure IV-39-(h)) and consequently doesn't disturb the DC grid components: current and voltage (see Figure IV-39-(b)).

It can be concluded from the previous tests that the proposed control algorithms can reduce the impact of external events such as symmetric and asymmetric faults.

4. **Conclusion**

In this chapter, the contributions regarding MMC control have been addressed. First, an improved Average Tolerance Band method has been proposed to reduce the switching frequency of MMC keeping the ripple value close to the desired one. Thereafter, advanced current controllers have been derived for high level control in order to obtain the fastest dynamics response. At the beginning, sliding mode control design based on continuous-time models has been chosen to synthetize the current control laws. It has been proved that the sampling period of control hardware has a major impact on the performances of the obtained controllers which requires its integration a priori in the derivation of control algorithms. Since discrete-time controllers allow such integration, they have been chosen for this purpose.

Based on exact discretization, discrete-time models for AC and DC as well as arm currents have been obtained and validated. Next, these discretized models have been used to derive the control laws for current loops using two control methods: pole placement based control and discrete-time sliding mode control. It has been demonstrated that the two methods allow to obtain the fastest response with a specific advantage for each method: i.e. integration of implicit structural limitations for sliding mode control and flexibility for pole placement method via the gain tunings. The off-line simulations have shown that the proposed control techniques present many advantages in terms of performances for references tracking in normal operations as well as for external disturbance rejections. Thanks to the high dynamics of the inner controller, the outer loops response time can be accelerated without affecting the stability margin which is mandatory in cascaded control philosophy between two successive layers (inner and outer in our case).

Motivated by the quite good performances of the proposed current controllers obtained in offline simulation, it has been decided to go deeper in the assessment by integrating real-time constraints before validation on experimental set-up. This is the aim of the next chapter

.

CHAPTER V Real-Time (HIL and RCP) Validations

1. Introduction

When new concepts (e.g. control algorithms) are developed and validated with offline simulations, the questions concerning their behavior with a real system arise since many real life situations are not then considered. One way to address these questions is to improve the model by emulating communication delays, including sensor models and measurement noises…. It necessitates in some cases new simulation tools as well as new infrastructures to be as close as possible to the final application on the real system. Hardware in the loop (HIL) and Rapid control prototyping (RCP) are two solutions which help satisfy such requirements. This type of simulation is usually used in the industry to test control algorithms performances and hardware implementation before the commissioning. In this chapter, the main results obtained throughout the thesis are validated using those two techniques involving real-time simulation.

2. Real-Time simulation

Real-Time (RT) simulation has become a mandatory step in control testing, allowing to demonstrate its performance in conditions close to real life [111] [112] [113]. Widely used in industry, it provides a mean to test the actual control software running on a dedicated hardware together with a virtual model or a prototype of the plant. This increases the realism of the simulation (real-time execution with real conditions) and provides access to hardware features that are currently not available in offline (non-real time) simulation [114] [115].

The real-time simulation has many advantages such as:

- RT simulation presents a good trade-off between traditional simulation and the real system regarding the cost and the time development [116].
- RT simulation combines the benefits of both computer simulation and experimentations to provide reliable testing results with minimum resources [117].
- RT simulation allows the simulation of some real operation conditions: communication delay, measurement noises…
- RT simulation is a safe test; it allows to simulate destructive events without any component damage.

Such simulation tests require high performances software and hardware technologies in order to execute the considered system with a small time-step (less than 20 micro seconds for power

electronics and electromagnetic transients). For our specific applications, systems involving CPU with real-time Operating System (OS) and Field-Programmable Gate Array (FPGA) cards are powerful enough to perform the real-time simulations with these requirements. During the simulation time-step, the real-time constraint requires to solve all equations and functions representing the system. When the number of equations and elements representing the system are relatively large or in order to speed up the simulation time-step, it may be necessary to use parallel computing using several CPU/ FPGAs.

Different manufacturers propose real-time simulation solutions (hardware and software) such as Speedgoat (MATLAB/Simulink), Opal-RT (eMEGAsim, HYPERSIM), RTDS (RSCad), National Instrument (LabVIEW), Typhoon… In this thesis, the real-time solution proposed by Opal-RT (RT-LAB software with OP4510 target) is chosen to perform the real-time validation.

3. Small scale MMC sizing

One of the objectives of the thesis was to size a small scale MMC for SuperGrid Institute real-time platform in order to be used for RCP and Power Hardware in the Loop (PHIL) validations. Given that there are many possibilities to size a given system, in our case, the main objective was to obtain the same dynamics as a real MMC station with the small scale one.

The real MMC station parameters are based on the data of INELFE-HVDC project, their values are given in Table V-1. The proposed MMC parameters are calculated based on the following inputs ($P_n = 6kW, V_{dc} = 400V, V_{ac} = 208\,V$).

3.1. Number of SMs

Once the input parameters (P_n, V_{dc} and V_{ac}) are fixed, the first dimensioning factor that should be defined is the number of SM per arm. Most of existing MMC prototypes are limited in term of number of levels (5 SMs per arm) due to prohibiting development costs [118, 119, 120, 121]. Their operation requires high switching frequency modulation methods in order to obtain an acceptable Total Harmonic Distortion (THD). Since the MMCs in HVDC applications operate with low switching frequency methods, it is necessary to increase the number of SMs in order to be able to work with such modulation strategies. Therefore, a trade-off has to be chosen in order to be representative in term of SMs number and to not increase the development costs.

For this purpose, some offline simulations for different MMC levels using NLC modulation strategy have been carried out.

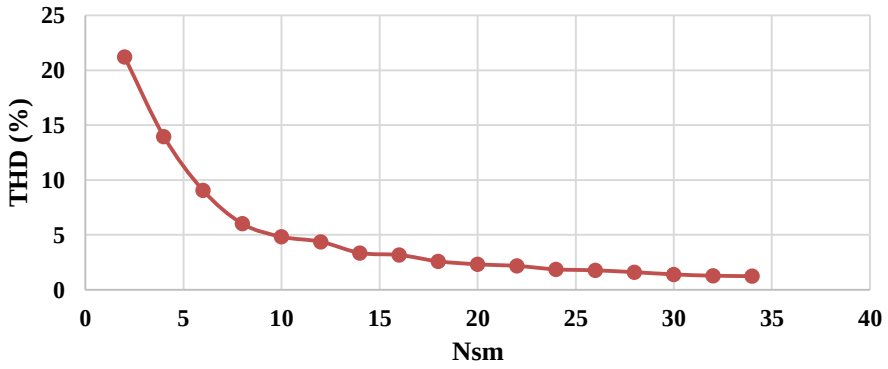

Figure V-1: The variation of voltage THD regarding the number of SMs.

From Figure V-1, it can be observed that with 5 SMs, the THD is relatively high (more than 10%). On another hand, increasing the number of SMs beyond 15 SM does not greatly improve the voltage quality and obviously increases the development cost. Figure V-1 shows that with 10 SMs per arm the obtained THD is less than 5% which is an acceptable value. Based on all this results, 10 SMs value has been chosen as a compromise for our MMC small scale prototype.

3.2. SM capacitor

In general, the sizing of the SMs capacitor has to meet two requirements: SM voltages rating and SMs capacitance value. The first requirement is directly calculated based on the DC voltage rating and the selected SMs number. That is:

$$v_{Cn} = \frac{V_{dc}}{N_{SM}} = \frac{400}{10} = 40\ V \qquad (V\text{-}1)$$

Since our objective is to represent the dynamics of the small scale MMC in a best possible way (the closest to a real MMC), the size of the SM capacitors can be obtained taking into account the ratio between the stored energy inside the SMs (the energy in arm inductances is neglected) and its nominal power. This parameter is known as electrostatic constant (H_c). It has been proved in [122] that, in order to obtain an averaged ripple of 10%, the electrostatic constant (H_c) has to be set between 30-40 ms.

According to [123], the SMs capacitor can be calculated by the following expression:

$$C_{sm} = \frac{2 * P_n * H_c}{6 * N_{SM} * V_{dc}^2} \quad (V\text{-}2)$$

For an electrostatic constant of 40 ms, the SMs capacitor is:

$$C_{sm} = \frac{2 * 6000 * 40 * 10^{-3}}{6 * 10 * 400^2} = 5\ mF$$

3.3. Arm inductance

The sizing of arm inductance depends on the rise of DC current fault and the circulating current within the legs [25]. In our dimensioning, the size of arm inductance has been calculated to be equal to the industrial MMC using per-unit approach. The obtained value is:

$$L_{arm}(pu) = 0.15 \ \rightarrow \ L_{arm}(SI) = \frac{V_{ac}^2}{P_n}\frac{L_{arm}(pu)}{w_n} = 3.44\ mH \quad (V\text{-}3)$$

The same approach is applied to the AC filter; the obtained value is:

$$L_f = 0.18\ pu \ \rightarrow \ L_f = 4.13\ mH \quad (V\text{-}4)$$

Table V-1: Small scale and INELFE MMC parameters.

	Small-scale MMC	***Real MMC (INELFE)***
Nominal power	*6 (kW)*	*1000(MW)*
Nominal AC voltage	*206 (V) (rms line to line)*	*320 (kV) (rms line to line)*
Nominal DC voltage	*400 (V) (pole to pole)*	*640 (kV) (pole to pole)*
Number of SMs per arm	*10*	*400*
SM capacitor/ H_c	*4.92 (mF) / 39.2 (ms)*	*13 (mF) / 40 (ms)*
AC filter impedance	*L_f = 0.22 [pu]* *R_f = 0.0036 [pu]*	*L_f = 0.18 [pu]* *R_f = 0.005 [pu]*
Arm impedance	*L_{arm} = 0.26 [pu]* *R_{arm} = 0.0049 [pu]*	*L_{arm} = 0.15 [pu]* *R_{arm} = 0.01 [pu]*

All these obtained values are adapted according to the available components (see Table V-1).

4. Hardware in the loop (HIL) validation

In this section, an HIL test setup is used to validate the control laws obtained in CHAPTER IV. This step allows to consider additional real time constraints such as delay and noises before going to RCP validation. In the following, we focus on the results for output MMC currents control (AC and DC currents) only. The results obtained using the control based on internal currents (arm currents) are exactly same.

4.1. HIL setup (configuration)

The overview of the HIL platform for testing MMC controls is presented in Figure V-2**.** The setup includes: the host computer, a real time target (OP4510) and IO communication links: PCI express to communicate between the FPGA card and different cores, DB37 to have access to digital and analog inputs/outputs.

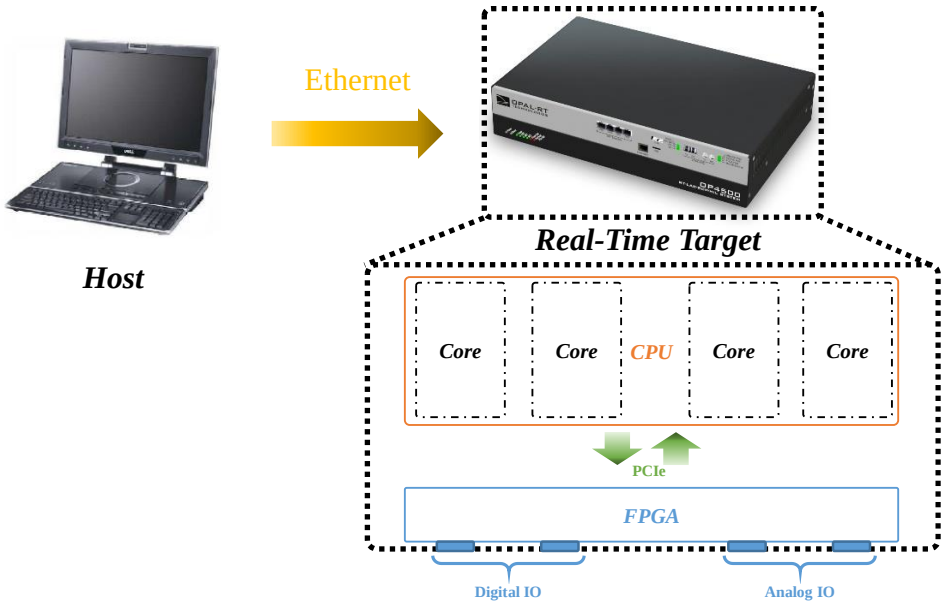

Figure V-2: Hardware in the loop simulation circuit.

Host: Thanks to its user friendly interface, RT-LAB allows to generate C code from a MATLAB/Simulink block diagram, compile and upload it on a dedicated hardware (OP4510 in our case). This process is achieved in 6 steps:

- Open the model which is already created in Matlab/Simulink (.mdl) with a supported version (2013a for example).
- Edit the open model to adapt it to the real-time computation constraints.
- Generate the real-time code for the model and prepare its transfer to the target.
- Specify exactly on which target will be executed each subsystem (model assignation).
- Allow the transfer of the code to the selected nodes; the different subsystems are loaded on each CPU and the communication is established.
- Allow to run the real-time simulation in parallel on all the nodes/targets.

Once the simulation is running, RT-LAB allows the user to change the simulation parameters, monitor the simulation (overrun, execution time…) and perform data acquisitions.

Real-time target OP4510: it is a compact real-time target with 4 core high performance processor from Intel that can run the simulation with a small time-step (down to less than 7 μs). This target also integrates a Field-Programmable Gate Array (FPGA) card for multi rate HIL applications and inputs/outputs management. The general specifications of OP4510 are:

- FPGA cards: Kintex-7 FPGA, 325T, 326,000 logic cells, 840 DSP slice (Multiplier-adder)
- RT-processor: 8GB RAM, Xeon E3 4 core CPU, 3.2 GHz, solid state hard disk 128 GB
- Fast optical interface: 4 sockets for optional Small Form-factor Pluggable (SFP&SFP+) 1 to 5 Gbits/s optical cable pairs (Rx/Tx)
- Software compatibility (CPU): RT-LAB multi-processors platform, LINUX, Simulink, SimPowerSystems, SimScape, ARTEMIS, RT-EVENT, HYPERSIM…
- FPGA: XILINX System Generator for Simulink, RT-LAB XSG, eHS FPGA electrical circuit solvers…
- Performance: Minimum time step of 7 microseconds for model subsystems executed on the INTEL CPU and 250 nanoseconds for models executed on the FPGA chips, 10 nanosecond timer resolution.

The system contains the following inputs/outputs ports for HIL applications:

- Digital output channels: 32 channels.
- Digital input channels: 32 channels.
- Analog input converter: 16 channels.
- Analog output converter: 16 channels.

4.1.1. Model implementation

In order to satisfy the real-time constraint regarding the execution time, it is necessary to parallelize the computation by separating the electrical system into several subsystems. In generally, the transmission lines and artificial short line "Stubline" allow performing this decoupling. RT-LAB provides specific solver known as Artemis/State Space Nodal (SSN) which derives the Norton equivalents of Matlab/Simulink models by dividing them into branches or groups [124]. It has been shown in [125] that such method allows to simulate the MMC with 100 SMs with 25 µs time-step.

In the following HIL test, the simulation circuit is the same as the one used through the whole thesis, see Figure IV-31. The model used for the MMC converter is the detailed model with semi-analytical implementation where the parameters correspond to the proposed small scale MMC (see Table V-1). For the DC side and in order to have a smoothed DC voltage, a capacitance of 6 mF has been added between the MMC station and the DC current source. The simulation circuit (AC grid, MMC and DC grid) is assigned to run on one core with 20 µs time-step (Ts).

4.1.2. Control implementation

The control structure presented in CHAPTER III (see section 5) is used in the following HIL validation. The high level control is assigned to run on one core (different than the one used for the model) with a control sampling period (T) where the low level control is running on a FPGA card with the BCA sampling period (T_{bca}) (see Figure V-3).

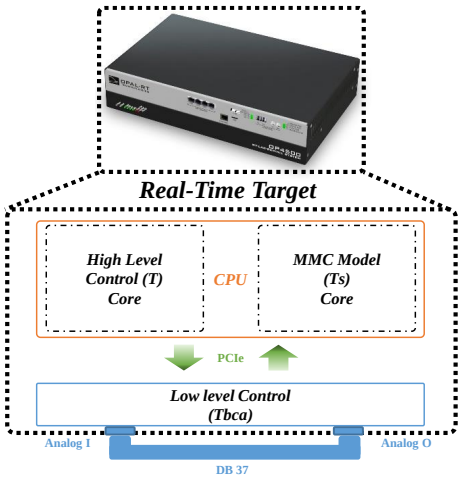

Figure V-3: Zoom on the HIL configuration.

4.1.3. HIL communication

Due to the high quantity of data exchanged between the model and its control system (60 pulse signals, 60 SM voltages, 6 arm currents, 3 AC voltages and one DC voltage), only few signals can be communicated via analog communications (16 signals). The send measurements have been chosen in order to obtain a complete loopback HIL test for one arm:

- 10*SM voltages of upper arm for leg (a).
- Arm current of upper arm for leg (a).
- 3*AC grid voltage.
- DC grid voltage.
- DC grid current.

The other SM voltages are communicated to the FPGA card using PCI express as it is shown in Figure V-3.

It should be pointed that, in addition to one-time step delay required for Software in the Loop (SIL) simulation (1 core for model, 1 core for control), the used HIL simulation necessitates one or two additional delays depending on the time-step ratio and FPGA communication type (synchronous or asynchronous).

4.2. HIL validation

4.2.1. Start-up sequence

The start-up process is given by the following steps:

- Connect the DC side in order to be able to charge the DC capacitor bus and SMs capacitor simultaneously during the next step (t=t_0).
- Close the AC breaker (connect the AC grid) to charge the system (t=t_1).
- Bypass the AC pre-insertion resistances (t=t_2).
- Activate the MMC control and increase the DC voltage as well as SM voltages to 1 pu (t=t_3).

The obtained results for all this process are shown in Figure V-4 where the active power, reactive power, DC voltage and average SM voltages are presented in (a)-(d) respectively.

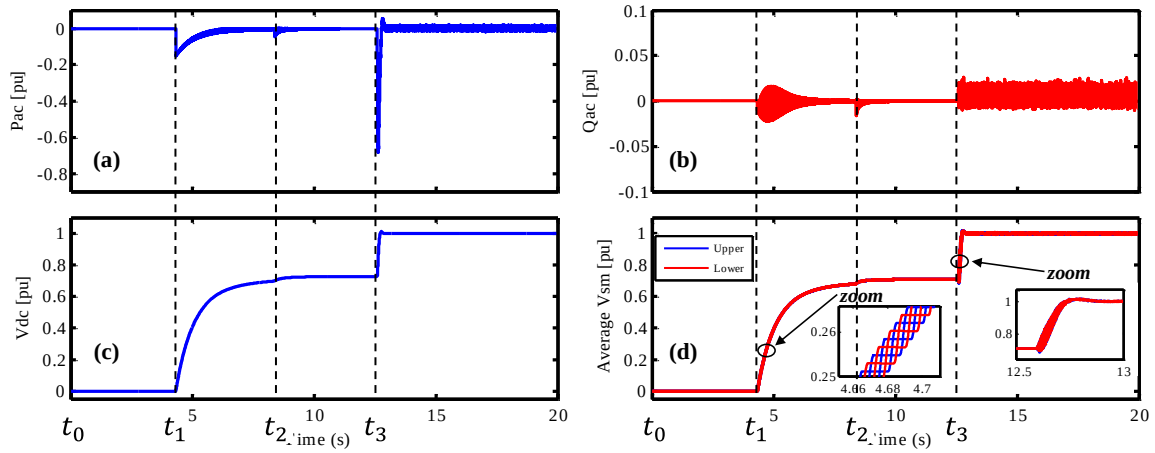

Figure V-4: HIL results for start-up sequence: (a) active power, (b) reactive power, (c) DC grid voltage, (d) average SM voltages for leg (a).

The obtained results for DC voltage and average SMs voltage have been compared to the offline simulation ones (see Figure V-5). It can be seen the results are quite similar.

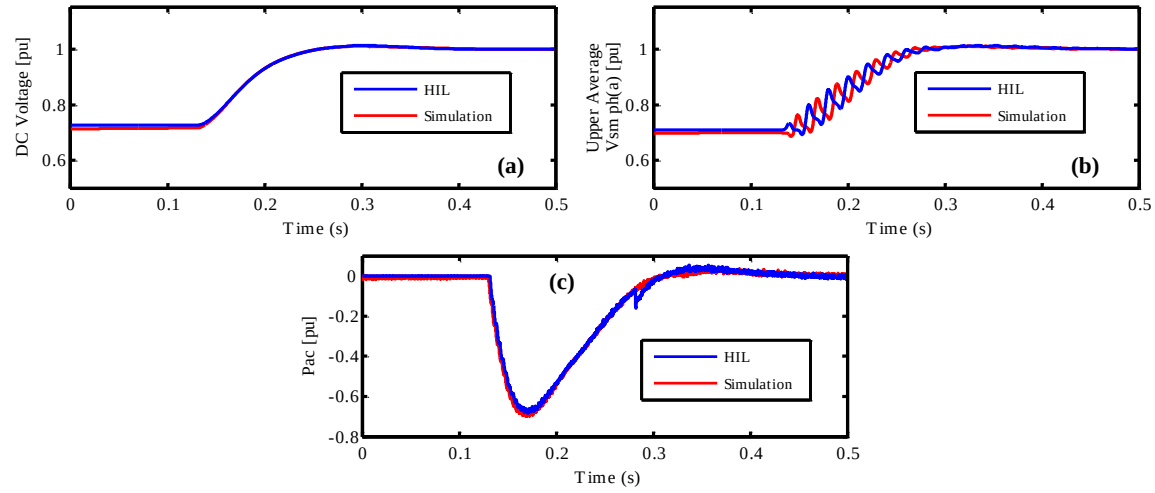

Figure V-5: Comparison between offline and HIL simulation results for control activation during the start-up process: (a) DC grid voltage, (b) upper arm average SM voltage for leg (a), (c) active power.

A zoom on steady state results after control activation is shown in Figure V-6. It can be observed that a small offset appears on reactive power. This offset can be attributed to the delay introduced by the HIL communication. It can be solved with one of the following methods:

- Add an integral term with a small gain to the control law given in equation (IV-37).
- Compensate the offset via the reactive power reference ($Q_{ac} = Q_{ac}^{*} - Q_{ac}^{offset}$).

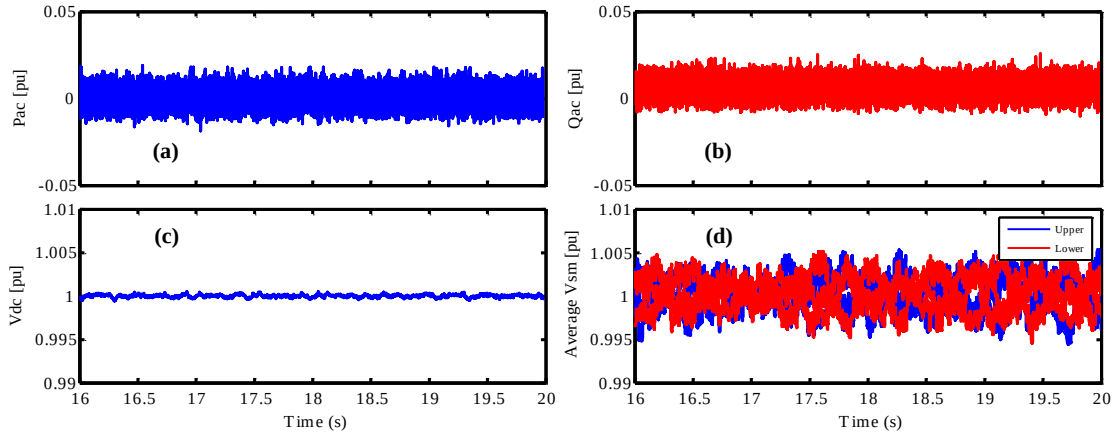

Figure V-6: Zoom on HIL results for start-up sequence: (a) Active power, (b) reactive power, (c) DC grid voltage, (d) average SM voltages for leg (a).

The second solution has been chosen in order to keep unchanged the obtained control law and consequently not to change its dynamic response.

4.2.2. High dynamics test

In this test, the reactive power reference is changed from 0.4 pu to -0.4 pu, the active power being set to -0.4 pu. The obtained results (see Figure V-7) show that the direction of reactive power changes as it is required by its reference.

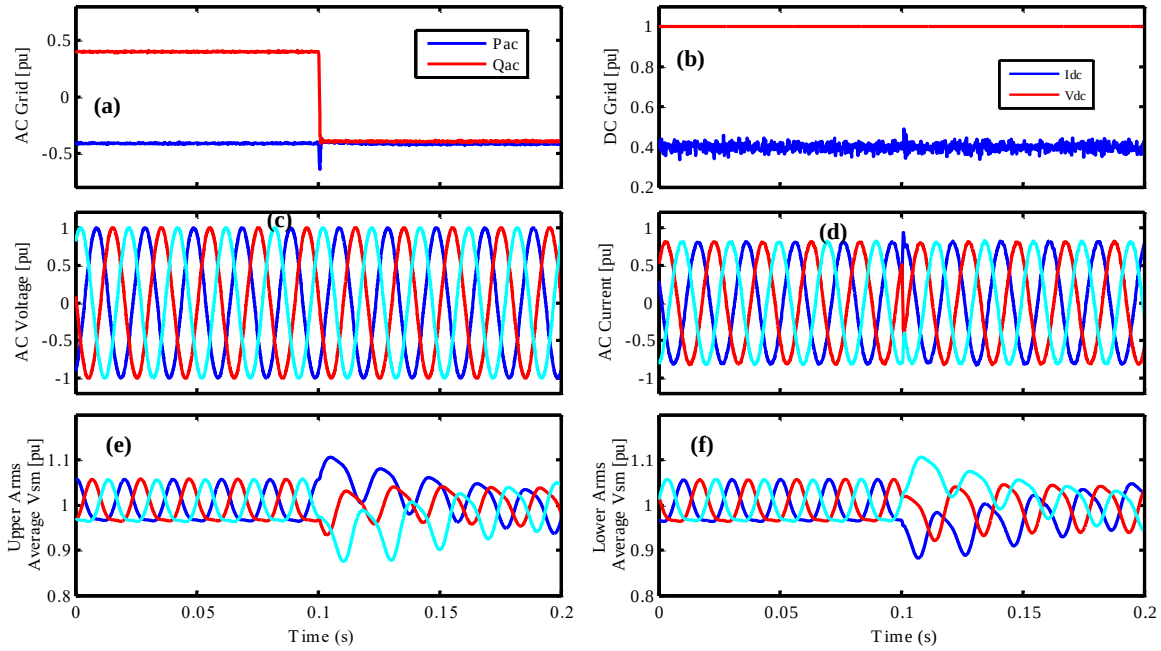

Figure V-7: HIL simulation results for reactive power step change: (a) active and reactive powers, (b) DC voltage with DC current, (c) AC voltage, (d) AC current, (e) upper average SM voltages, (f) lower average SM voltages.

5. Rapid Control prototyping (RCP) validation

Rapid Control Prototyping (RCP) systems are ideal for designing, prototyping and testing complex control system. They provide a fast and inexpensive way for control and signal processing engineers to verify designs early and evaluate design tradeoffs. In this section the test bench used for this validation test is described.

5.1. Mock-up description

Based on the proposed parameters in Table V-1, a prototype MMC has been built by Opal–RT engineers in the context of a collaboration between SuperGrid Institute and Opal-RT companies. A picture of the MMC rack is shown in Figure V-8 that includes:

Figure V-8: Small scale MMC station.

- 6 x OP1210: MMC arms [10 submodules].
- 1 x OP4510: real time simulator with 32DIN, 32 DOUT, 16AIN, 16AOUT, 12 SFP.
- 1 x OP1260: protection box.
- 1 x OP1261: measurement box.
- 1 x OP1262: inductance boxes.

5.2. Test bench structure

The experimental setup is presented in Figure V-9. It is composed of MMC rack with two power amplifiers connected in manner to emulate a point to point HVDC link. A capacitor is connected in parallel to emulate the DC cable (see Figure V-9).

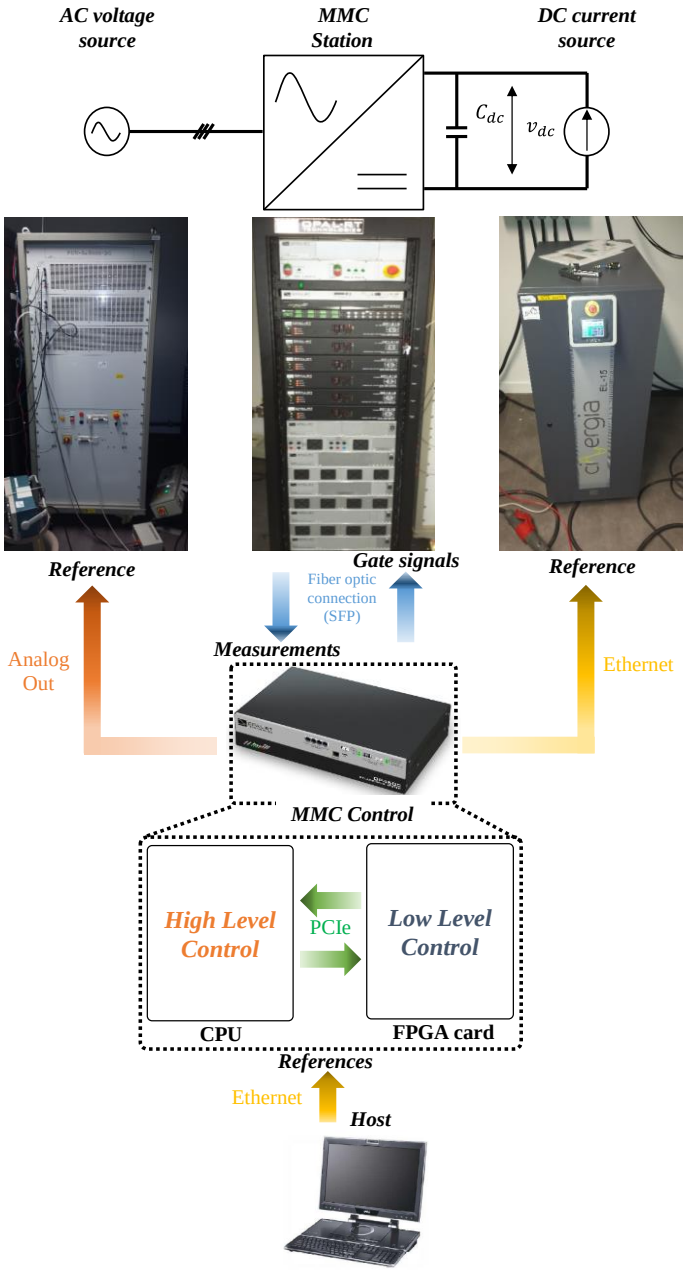

Figure V-9: Experimental test bench setup.

The amplifiers used are:

- Puissance+ PCU-3X5000-BC: high bandwidth linear power amplifier to emulate the AC grid.
- CINERGIA 15 kW: Switching power amplifier in DC control mode to emulate the DC grid.

Since the DC amplifier is used to emulate the DC grid perturbation (Power control mode), the MMC has to be controlled in DC voltage mode to ensure DC grid stability.

The Opal-RT hardware device (OP4510) is used to implement the control of the MMC station. Due to the high quantity of data exchanged between the station and its control, the OP4510 device communicates with the station via optical fiber links using FPGA card (Kintex7-TE0741). It receives measurements (arm currents and SM voltages) from sensors and sends the pulse signals for each SM. The OP4510 is also used to send the references to AC and DC amplifiers via analog outputs and Modbus communication respectively (see Figure V-9).

5.3. Experimental tests validation

In this section, the same events used for offline validation in the previous chapter (see section 3.4) are applied to the MMC station.

5.3.1. Start-up sequence

In order to start operating the MMC test bench, it is necessary to charge the SM capacitors as well as the DC grid one to their nominal values. For this purpose, the previous start-up process used in HIL validation (see section 4.2.1) is applied to the small scale MMC.

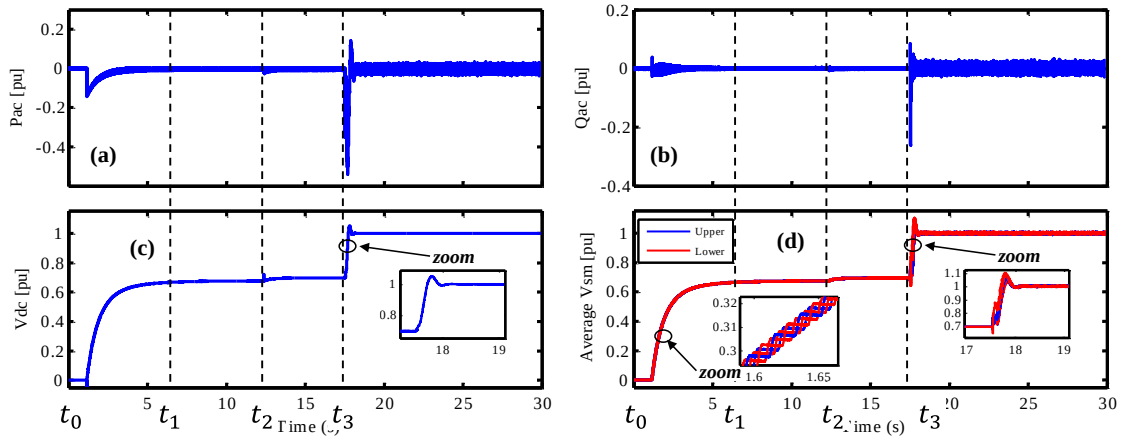

Figure V-10: Experimental results for start-up sequence: (a) Active power, (b) reactive power, (c) DC grid voltage, (d) average SM voltages for leg (a).

The obtained results are presented in Figure V-10 where the active power, the reactive power, DC grid voltage and the average SM voltages for leg (a) are shown in (a)-(d) respectively. It can be observed that the process is working well without creating any over voltages.

5.3.2. High dynamics test

In the following, the high dynamics response of the proposed control is tested on the reactive power. For a step change of 0.8 pu (from 0.4 to -0.4 pu), the obtained results are shown in Figure V-11. It can be observed that the proposed control ensures high dynamics without any over current in the arms neither on the AC and DC ones.

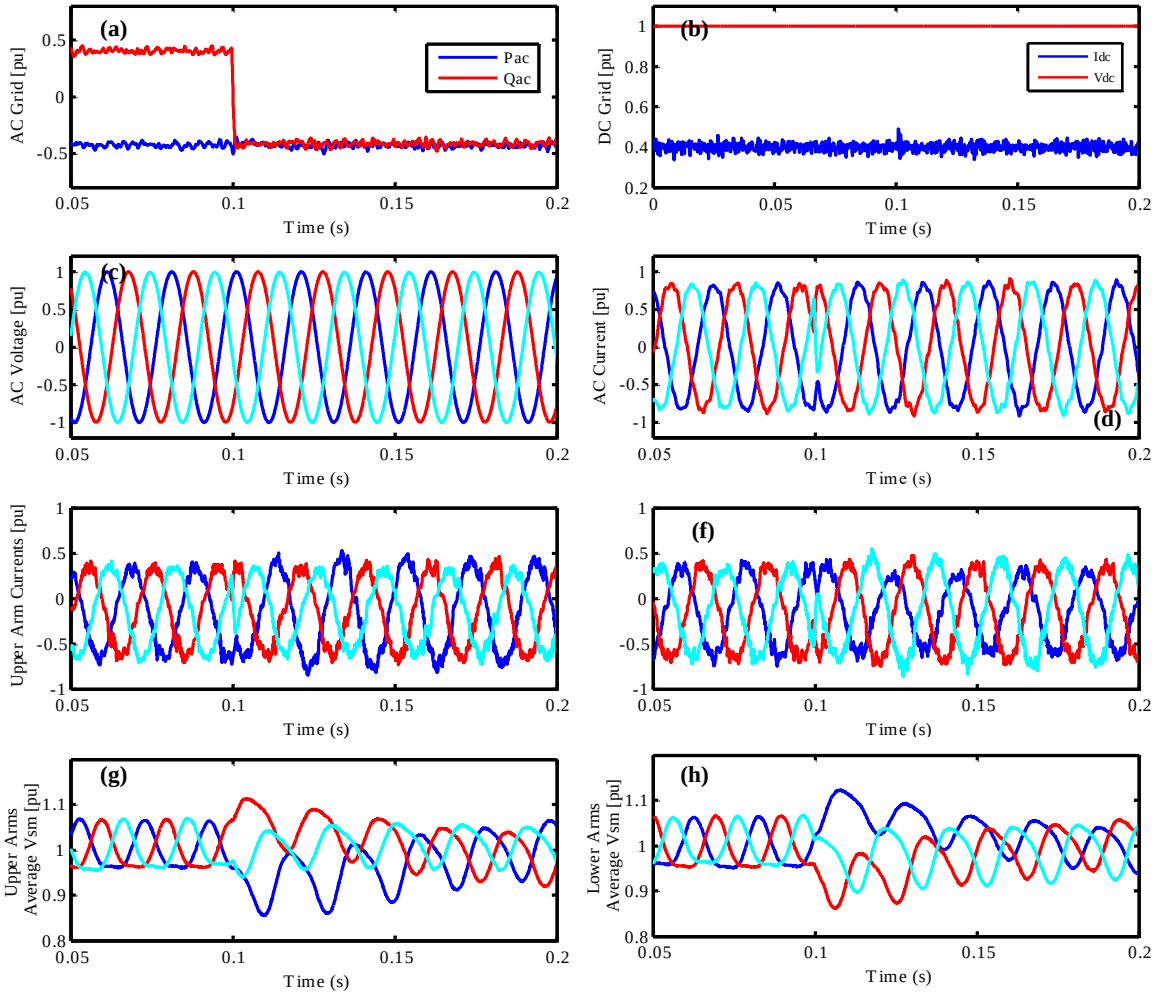

Figure V-11: Experimental results for reactive power step change: (a) active and reactive powers, (b) DC voltage with DC current, (c) AC voltage, (d) AC current, (e) upper arm currents, (f) lower arm currents, (g) upper average SM voltages, (h) lower average SM voltages.

The obtained results are compared to the offline ones for reactive power variation (see Figure V-12).

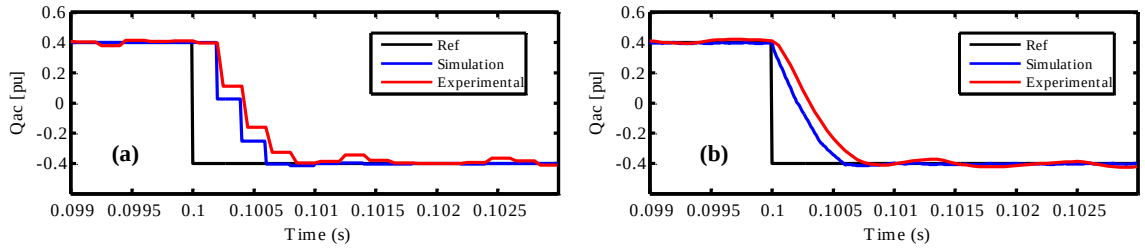

Figure V-12: Comparison between simulation and experimental results for reactive power step change: (a) seen by control, (b) measurements.

It can be observed that the experimental result is slightly different than the simulation one (one-time step delay). This difference can be attributed to delay introduced by the AC amplifier on one hand and the parameter errors such as the equivalent resistance of switches. However, the results show a high performances of the proposed control in term of response time (less than 1 ms) and overshoot.

5.3.3. Energy step

It has been shown with offline simulation that, thanks to the high dynamics response of the proposed current controllers, the response time of outer loops such as energy loop can be decreased. In this test, the energy reference is decreased from 1 pu to 0.95 pu, with the energy controller being set to different response time values.

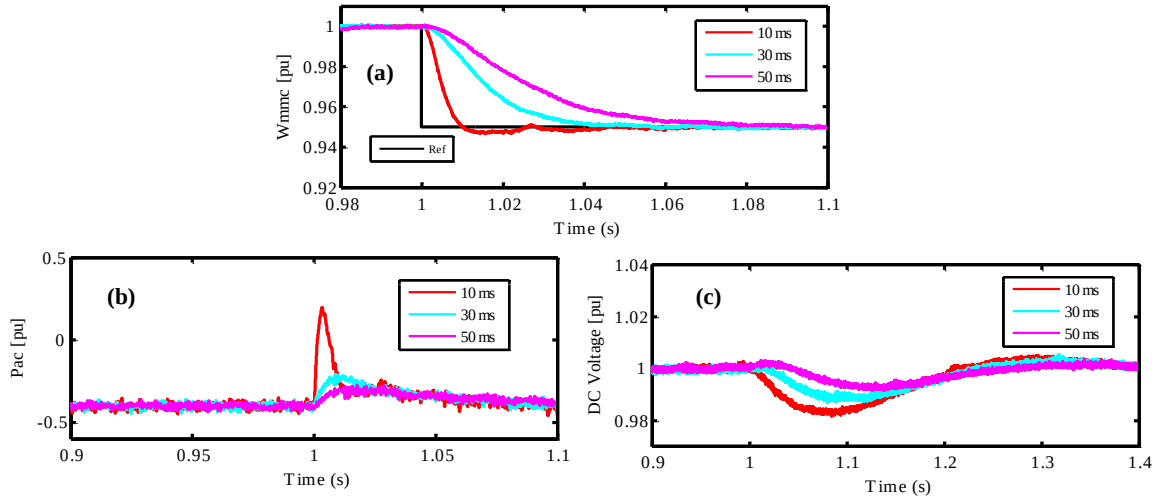

Figure V-13: Experimental results for energy step change with AC control strategy($\alpha_W = 0$): (a) MMC energy, (b) active power, (c) DC voltage.

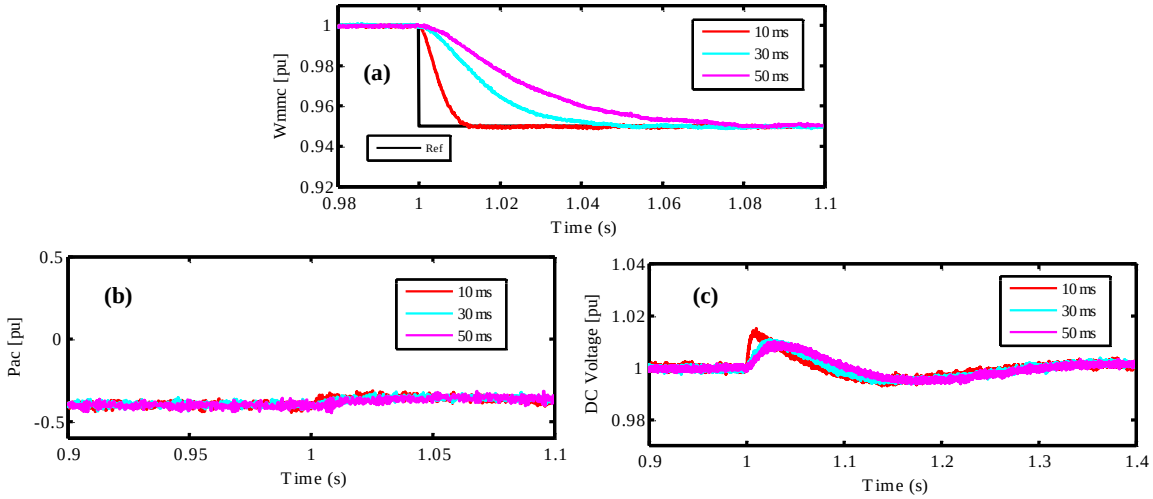

Figure V-14: Experimental results for energy step change with DC control strategy($\alpha_W = 1$): (a) MMC energy, (b) active power, (c) DC voltage.

The experimental results are presented in Figure V-13 where the energy is controlled with the AC side and in Figure V-14 where it is controlled with the DC side. For 10 ms response time, the experimental result is compared to the simulation one (see Figure V-15). It can be observed that the two obtained results have the same behavior.

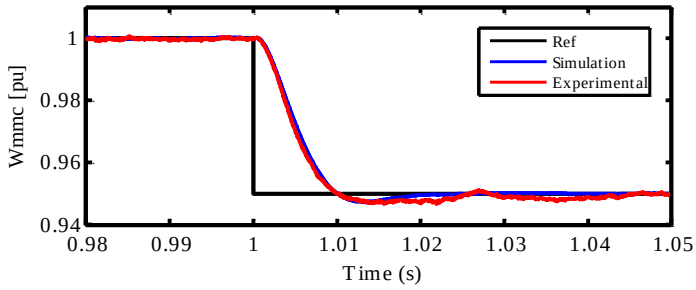

Figure V-15: Comparison between simulation and experimental results for energy step change with AC control strategy ($\alpha_w = 0$).

5.3.4. Symmetric AC dip

In this experimental test, a three phase AC voltage dip is applied to the MMC station. The obtained results are presented in Figure V-16 where the active and reactive powers, DC voltage with DC current, AC current, AC voltage, upper arms average SM voltages and lower arms average SM voltages are shown in (a)-(f) respectively.

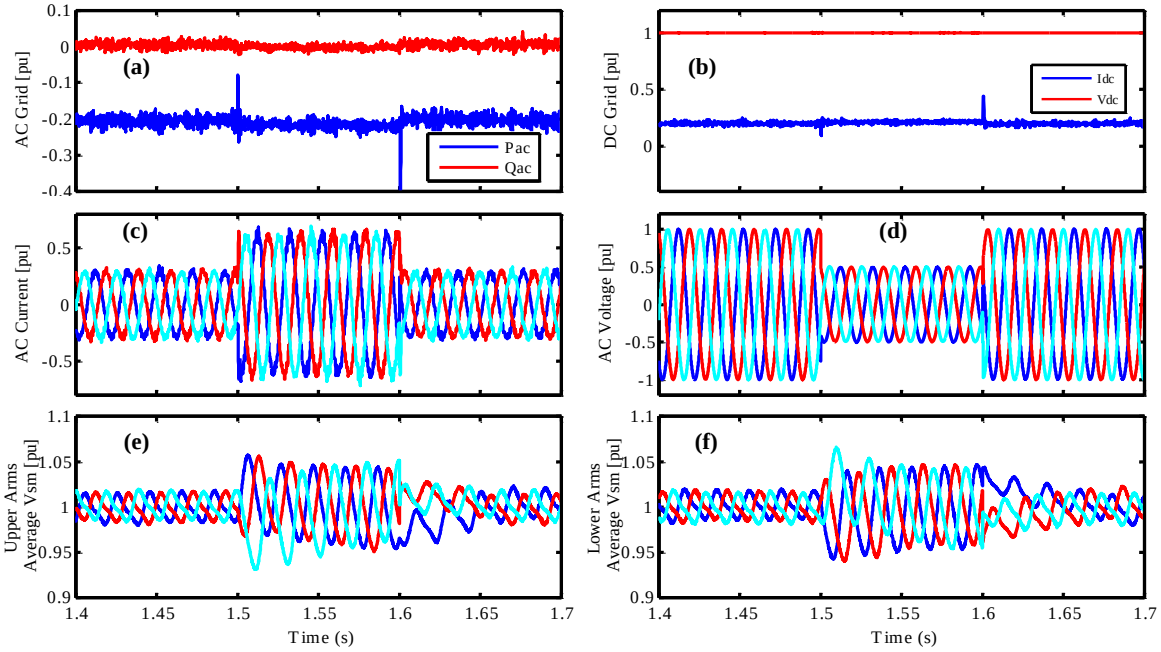

Figure V-16: Experimental results for symmetric AC voltage dip (50%): (a) active and reactive powers, (b) DC voltage with DC current, (c) AC current, (d) AC voltage, (e) upper average SM voltages, (f) lower average SM voltages.

The results show that the proposed control maintains the same power level during and after the event. The comparison between the experimental and simulation results show that the two results are quite similar (see Figure V-17).

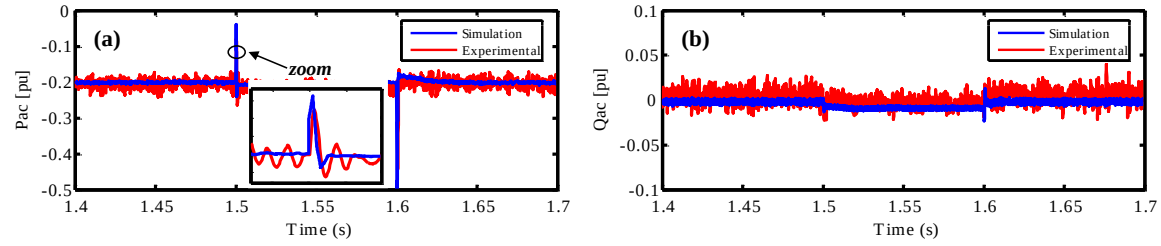

Figure V-17: Comparison between simulation and experimental results for symmetric AC voltage dip (50%): (a) Active power, (b) reactive power.

5.3.5. Asymmetric AC dip

To emulate a 2 phase AC fault located far from the station, a two phase AC voltage dip is applied to the MMC station (50%). The obtained results are presented in Figure V-18 where the active and reactive powers, DC voltage with DC current, AC current, AC voltage, upper arms average SM voltages and lower arms average SM voltages are shown in (a)-(f)

respectively. It can be seen from (Figure V-19) that there is a good correlation between the simulation and experimental results

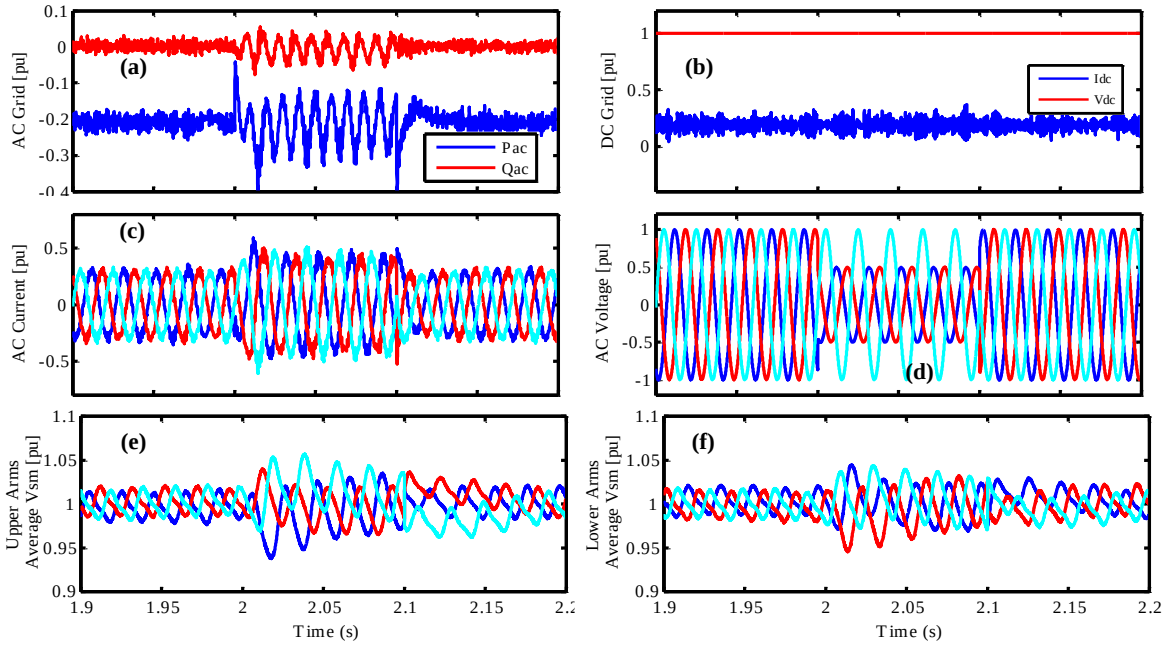

Figure V-18: Experimental results for asymmetric AC voltage dip (50%): (a) active and reactive powers, (b) DC voltage with DC current, (c) AC current, (d) AC voltage, (e) upper average SM voltages, (f) lower average SM voltages

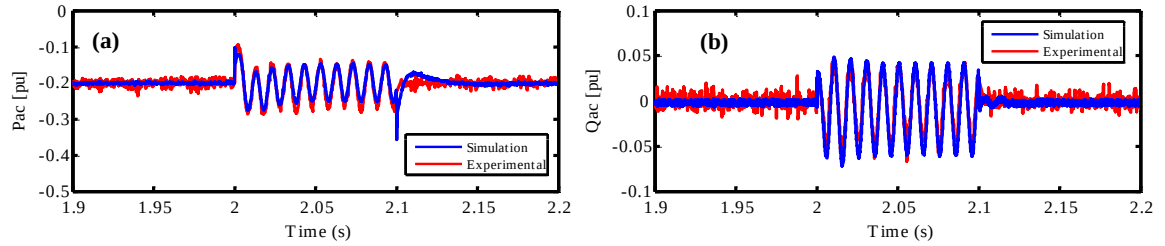

Figure V-19: Experimental results for symmetric AC voltage dip (50%): (a) active and reactive powers, (b) DC voltage with DC current, (c) AC current, (d) AC voltage, (e) upper average SM voltages, (f) lower average SM voltages

6. Conclusion

In this chapter, the proposed control in Chapter 4 is tested with HIL and RCP tests. For this purpose, a small scale MMC with 10 SMs has been sized and developed. Before going to experimental tests, HIL validation has been used to anticipate the RCP test. It has been shown that the delay introduced by the loop back leads to a small offset in the reactive power. This latter has been taken in the account in the reference calculation for reactive power in order to

cancel it. The experimental results show good performances of the proposed control and good correlation with the obtained results with offline simulation.

Conclusions and Perspectives

Conclusions

In the recent years, The HVDC has emerged as adequate solution for integration of renewable energy sources coming from wind farm or hydro power stations. Since its innovation, the modular multilevel converter (MMC) topology of VSC has been considered as a promising solution for such application. This thesis has carried out with the context of developing models and control system for this structure.

Before addressing the control and modeling problematics covered by this thesis, the topology of MMC with its operation principle have been presented. This allows to introduce the challenges of modeling and control due to the high number of switching elements and state variables, and clarify the motivation behind this thesis. Even if several research studies have been carried out on this problematic, there still exists many barriers and locks which have not been addressed in exhaustive manner.

The first objective was to remove the ambiguities regarding the implementation of MMC models proposed in the literature. New implementation techniques (analytical and semi-analytical) have been applied in order to add new functionalities (blocking capability and operation under endogenous faults conditions) to the MMC models. In addition, these techniques allow to simplify their implementation and reduce the elements constituting the models. The simulation results have shown a good correlation between the proposed models and the benchmark one (detailed model with circuit implementation) for controlled, blocked and faulted states.

The second objective of the present thesis was to investigate the control of the MMC using cascaded control methodology. For a good MMC operation, the low level control has to maintain a voltage balance between SMs within one arm. The average tolerance band method has been improved in order to reduce the switching frequency and impose the desired ripple whatever is the transferred power.

On the base of MMC topology and principle, its state space equations have been derived in order to be used for control purposes. Unlike standard VSCs, the MMC control has to regulate its internal energy in order to ensure the converter operation. Thanks to energy based control structure, the voltage of equivalent arm capacitor can take different value than the DC one. This opens the opportunity to use the MMC as a storage system which can be used as an additional

degree of freedom to provide some services such as oscillations damping. This necessitates a fast response time for the energy loop and consequently high dynamics controller for current loops since the cascaded control is based on time scaling principle. A special new control algorithms have been developed to address this issue.

At first, sliding mode control design for continuous-time models has been used to accelerate the response time of current controllers. Even if this control algorithm has shown very good performances in term of dynamic response and robustness, undesired oscillations (known as chattering when using sliding mode technique) have appeared making the choice of this type of control difficult to argue in front of other techniques presented in the literature. This chattering comes from the hypothesis that ideal sliding mode control considers infinite switching (sampling) periods. Therefore, our thoughts went to the necessity to integrate à priori the sampling period in the control design. In addition to the fast dynamics response requirement, it naturally leads to use discrete-time control techniques. To do so, discrete-time model of the MMC is required. In the literature, discrete-time based controllers are often derived using Euler approximation for the continuous-time model discretization. One of the main contributions of the present thesis is the derivation and the use of exact discrete-time model of the MMC. Discrete-time sliding mode control and pole placement method have shown a high dynamics tracking performances for normal operation as well as for external perturbations rejection. This results have been confirmed with real time validations such as hardware in the loop and rapid control prototyping tests.

Perspectives

To go beyond the work proposed in this thesis, several research topics can be carried out:

- Considering the structural limits à priori in control laws synthesis in order to well drive the dynamics response of MMC.
- Investigating the impact of measurement and control time-delays in the control system.
- Applying the proposed methodology regarding modeling and control for other MMC topologies such as Full-Bridge, Double-Clamped, Alternate Arm Converter…
- Including and studying the proposed MMC control with Multi terminal DC grid (MTDC).
- Considering the AC system dynamics especially in case of weak AC grids.

- Investigating the possibility of large buffer storage system inside the MMC for more flexibility and interaction with AC systems.

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Résumé Etendu en Français

Contexte de la thèse

De nos jours, les systèmes énergétiques sont confrontés à de nombreux défis et exigences qui nécessitent un changement de paradigme. Les volontés politique et publique d'accroître l'indépendance énergétique, de réduire les émissions de gaz à effet de serre et d'accroître les capacités d'échange exigent des actions urgentes pour atteindre ces objectifs ambitieux. Pour ce faire, il est prévu que l'intégration des énergies renouvelables à grande échelle jouera un rôle crucial pour le développement des futurs réseaux électriques. En outre, afin d'accroître la robustesse des réseaux actuels et de créer un grand réseau électrique, l'interconnexion des différents pays et continents peut être considérée comme une bonne solution. De ce fait, et afin d'obtenir une bonne distribution de puissance, nous ne pouvons pas compter uniquement sur les lois de Kirchhoff. L'insertion de dispositifs d'électroniques de puissance associés à un nouveau concept de contrôle et l'augmentation des capacités de liaison sous-marine amélioreront la gestion des flux d'énergie. Il est donc nécessaire d'adopter une solution de transmission optimale (économique, technique, financière ...) pour répondre à tous ces besoins.

Le transport d'électricité en courant continu et à haute tension (HVDC) basé sur la technologie de convertisseur à source de tension (VSC) est largement apparu comme une solution adéquate pour faire face à ces défis. Plusieurs projets HVDC ont été réalisés ou sont actuellement en cours de développement à travers le monde: *Trans Bay Cable* aux USA, *INELFE* entre la France et l'Espagne, *Rio Madeira* au Brésil, ou encore *Nanao multi-terminal VSC-HVDC* (Chine)... Cela donnera l'opportunité de pouvoir développer un grand réseau électrique fortement maillé dont les réseaux DC multi-terminaux font partie. Ce qui ouvre l'opportunité d'un nouveau concept basé sur un réseau de transmission hybride (AC / DC). À cette fin, de nouvelles philosophies opérationnelles ainsi que des équipements sophistiqués pour l'exploitation de ce nouveau système de transport d'électricité sont de plus en plus nécessaires. Des recherches considérables sont menées aujourd'hui pour répondre à ces besoins tels que:

- Définir des Grid codes pour les réseaux HVDC.
- Étudier l'interaction entre les réseaux à courant alternatif et les réseaux à courant continu.

- Développer de nouveaux équipements basés sur de nouvelles technologies comme des disjoncteurs, câbles, convertisseurs ou des parafoudres.

L'un des principaux acteurs contribuant au développement des futurs réseaux HVDC est le convertisseur AC/DC. Diverses topologies de convertisseurs VSC ont été proposées dans la littérature comme les convertisseurs à deux niveaux, à trois niveaux, et les « Flying Capacitor Convertisseur». Dans le but d'améliorer la qualité de la tension et la fiabilité du system, la topologie de convertisseur modulaire multiniveaux (MMC) a attiré beaucoup d'attention depuis son invention. Grâce à son évolutivité, ses performances et son efficacité, cette topologie est considérée comme la solution la plus prometteuse pour les applications HVDC.

Cette thèse traite le développement de modèles et de contrôle du convertisseur de type MMC. Le nombre élevé d'éléments de commutation et de variables d'état internes présentent des défis de modélisation, en particulier lorsqu'ils sont mis en œuvre dans des logiciels de type transitoires électromagnétiques (EMT). En outre, le contrôle de cette topologie diffère de celui des autres topologies de convertisseurs VSC vu que la gestion du stockage interne est différente, ce qui nécessite une attention particulière. Plus précisément, cette thèse étudie ces deux aspects (modélisation et contrôle) afin de bien comprendre ces défis et de proposer de nouvelles solutions.

La première contribution de cette thèse est de développer de nouveaux modèles (d'ordre complet et d'ordre réduit), en utilisant différentes techniques de mise en œuvre. Les modèles obtenus permettent de réduire le nombre des éléments de commutation dans la structure. Cela conduit à faciliter leur mise en œuvre dans les programmes EMT et accélérer les simulations. La deuxième contribution est de proposer de nouveaux algorithmes de contrôle pour les contrôleurs de courants actuels. Pour cela, deux méthodes ont été utilisées pour dériver leurs lois de contrôle qui permettent d'obtenir le temps de réponse le plus rapide.

Les objectives de la thèse et sa méthodologie

L'objectif de cette thèse porte sur la modélisation et le contrôle des MMCs, ci-dessous ces principaux objectifs:

- Étudier les différents modèles de MMC présentés dans la littérature (détaillé, équivalent et moyen) ;
- Proposer des versions améliorés des modèles existants en utilisant des nouvelles techniques de mise en œuvre ;
- Identifier l'effet d'algorithme d'équilibrage des sous-modules (SMs) concernant l'opération du MMC ainsi que ses critères de dimensionnement (dimensionnement des SMs) ;
- Proposer de nouveaux algorithmes de contrôle pour les boucles de courants pour une approche de boucles en cascade ;
- Prendre en compte la période d'échantillonnage du système de contrôle dans la synthèse de la loi de commande des boucles de courants afin d'améliorer leurs temps de réponses ;
- Explorer la possibilité d'accélérer les boucles externes ; la boucle d'énergie par exemple.

La méthodologie de la thèse

Les résultats obtenus dans cette thèse proviennent principalement de l'analyse théorique de la topologie du convertisseur (MMC basées sur des sous-modules (SMs) en demi-pont). Ceci est obtenu, d'abord, en dérivant les différentes expressions analytiques pour les modèles du MMC. Ensuite, son modèle simplifié est utilisé pour comprendre son principe de fonctionnement et obtenir ces équations d'états. Cela conduit à proposer de nouveaux algorithmes de contrôle pour les boucles de régulations des courants. Les résultats obtenus, en termes de modélisation et de contrôle, sont ensuite validés par des simulations offlines (hors temps réel), simulations en temps réel et par des tests expérimentaux.

La structure de la thèse

Cette thèse est organisée comme suit : Le premier chapitre est consacré à expliquer le principe des réseaux HVDC et la motivation derrière les recherches impliquant la topologie MMC. Le deuxième chapitre traite la problématique de modélisation et propose de nouveaux modèles avec des nouvelles fonctionnalités. Le contrôle commande de MMC avec ces deux étages de

contrôle est étudié dans le troisième chapitre. Cela permet de bien choisir la structure de contrôle utilisée dans la suite la thèse et de justifier ce choix. Le quatrième chapitre est dédié à présenter les contributions de la thèse en terme de contrôle-commande. La validation de ces contributions en temps réel et avec testes expérimentaux constitue le cinquième chapitre.

Un résumé de chacun de ces chapitres est présenté ci-dessous:

Chapitre 1: Les architectures et les technologies des réseaux HVDC

Ce chapitre présente la technologie du réseau HVDC et ses principes. Tout d'abord, les configurations HVDC sont présentées avec leurs avantages et inconvénients associés. Ensuite, les principales technologies de conversion AC/DC, que sont les LCC et les VSC, sont présentées et comparées. Enfin, l'avantage du MMC par rapport aux autres topologies VSC est montré afin de comprendre la motivation derrière l'objectif de la thèse.

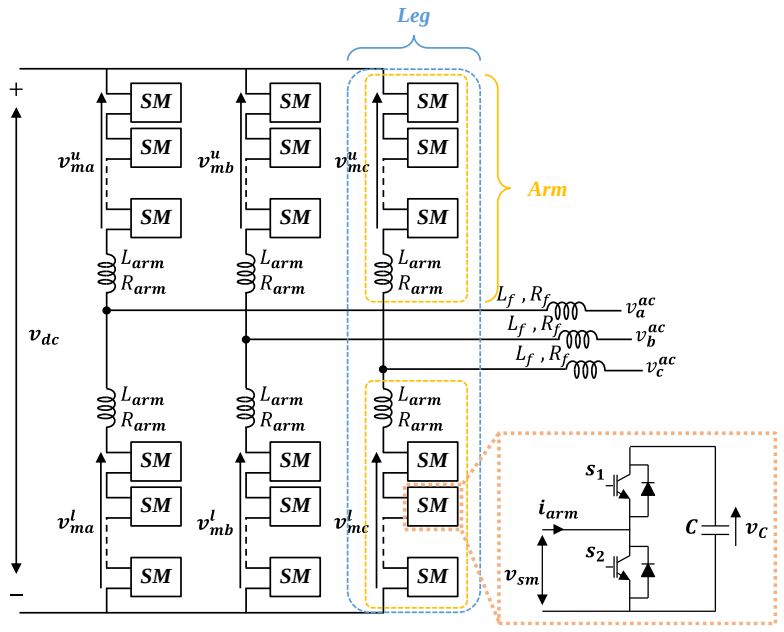

Figure-1: La structure du convertisseur MMC étudiée dans la thèse

Chapitre 2: La modélisation des convertisseurs MMCs

Ce chapitre traite la modélisation des convertisseurs MMC. Afin de bien comprendre cet axe de recherche, la problématique liée à sa modélisation dynamique est abordée. Après un état de l'art basé sur des références bibliographiques récentes, trois modèles dynamiques sont choisis afin de les améliorer. Ces modèles sont: le modèle détaillé, le modèle équivalent et le modèle moyen. Pour les modèles considérés, des nouvelles méthodes de mise en œuvre (analytique et semi-analytique) sont développées, expliquées et validées.

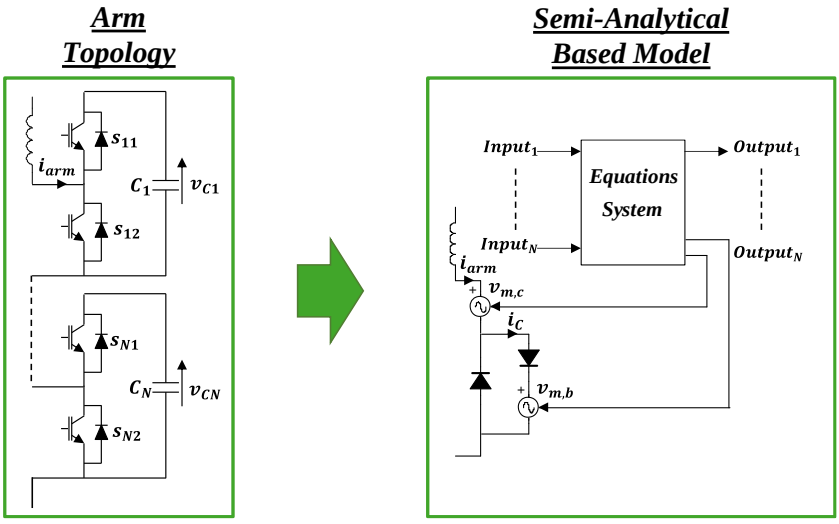

Figure-2: Le modèle semi-analytique proposé pour un bras du MMC.

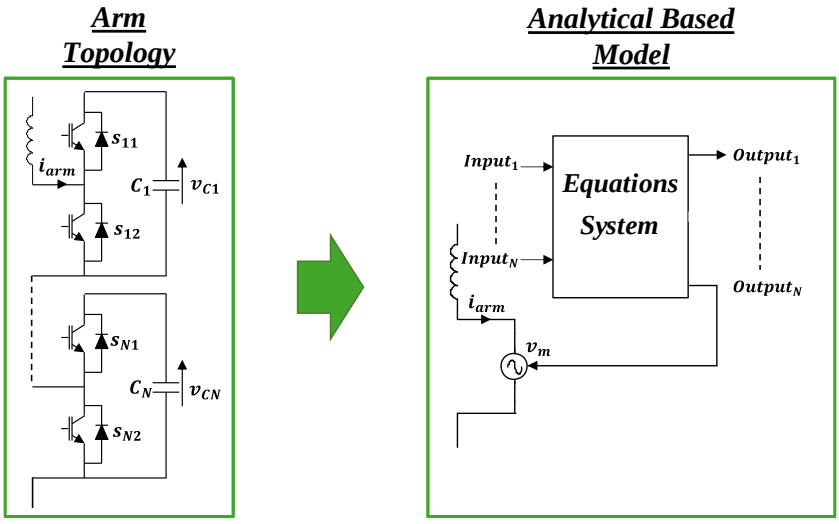

Figure-3: Le modèle analytique proposé pour un bras du MMC.

Chapitre 3: Le contrôle-commande des convertisseurs MMCs

Ce chapitre présente le principe de contrôle des convertisseurs MMCs avec ses deux couches principales. Ces dernières sont expliquées et revues sur la base de publications bibliographiques récentes, en concluant que le contrôle basé sur l'énergie permet d'obtenir un meilleur contrôle de toutes les variables d'états du MMC.

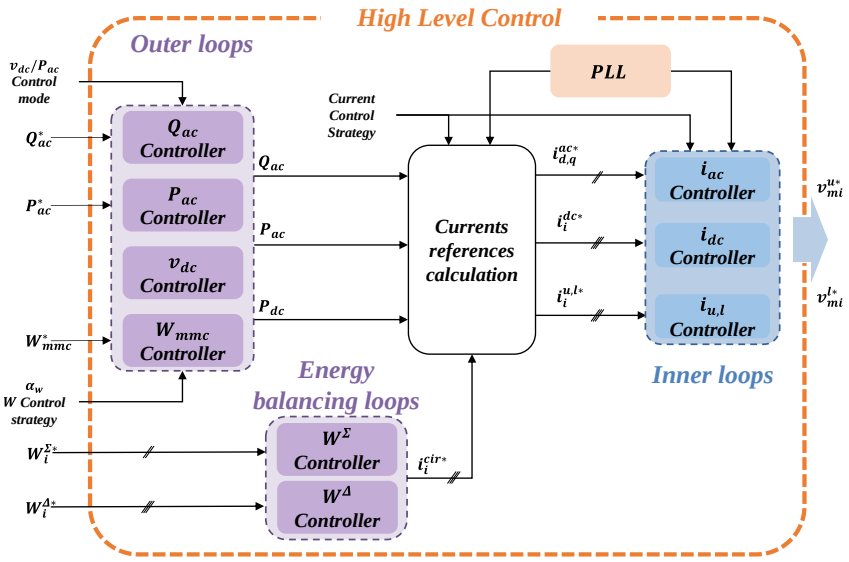

Figure-4: Schéma de contrôle retenu pour l'étage supérieur.

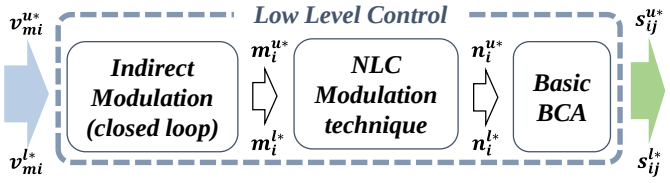

Figure-5: Schéma de contrôle retenu pour l'étage inférieur.

La structure du contrôle en cascade basée sur le principe des boucles imbriquées permet de contrôler les variables d'états du system d'une manière découplée. Un tel découplage nécessite un temps de réponse lent pour les boucles extérieures (objectifs de contrôle) afin de maintenir le rapport de temps de réponses entre les boucles.

Chapitre 4: Contributions au control des convertisseurs MMCs

Ce chapitre propose des contrôleurs de dynamique élevés pour les boucles internes afin d'accélérer le temps de réponse des boucles externes. Sur la base d'une discrétisation exacte des modèles d'état du MMC, deux méthodes de contrôle ont été utilisées pour synthétiser les lois de contrôle de courants qui sont: le placement de pôles et le contrôle en mode glissement à temps discret. Des simulations ont démontré que les contrôles proposés présentent de nombreux avantages en termes de performances d'une part et permettent d'accélérer les boucles extérieures telles que la boucle d'énergie (5 ms) d'autre part.

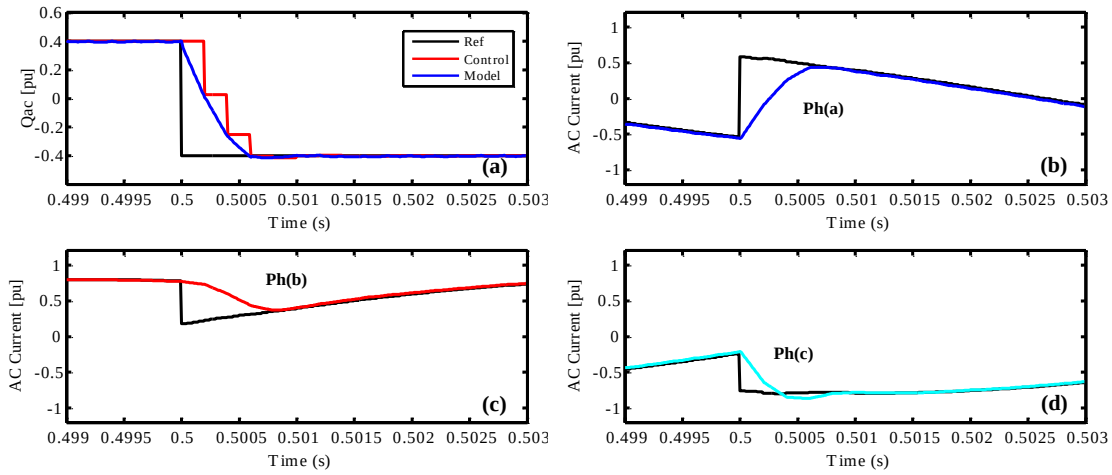

Figure-6: Résultats de simulation pour un échelon sur la puissance réactive avec une période d'échantillonnage de 0,2 ms: (a) puissance réactive, (b) courant alternatif dans la phase (a), (c) courant alternatif dans la phase (b), (d) courant alternatif dans la phase (c).

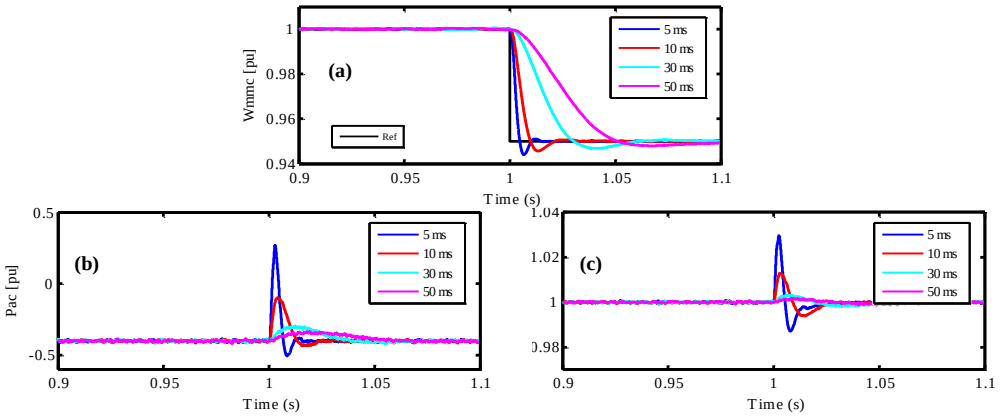

Figure-7: Résultats de simulation pour un échelon sur l'énergie interne du MMC: (a) énergie stockée dans le MMC, (b) la variation de la puissance active, (c) la variation de la tension du bus DC.

Chapitre 5: Validation HIL et RCP

Le but de ce chapitre est de valider les résultats précédents sur un banc de test. Pour se faire, un MMC à échelle réduit a été dimensionné et développée dans le but d'obtenir la même dynamique qu'un MMC réel. Avant d'aller directement vers les tests expérimentaux, la validation avec des simulations en temps réel (HIL) a permet d'anticiper certaines contraintes telles que les retards et les bruits de mesures. Les résultats expérimentaux ont montré une bonne corrélation avec les résultats obtenus en simulation hors temps réel.

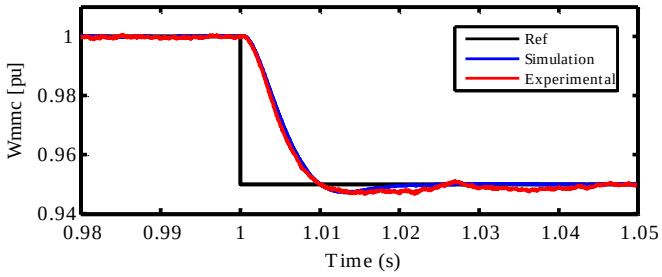

Figure-8: Comparaison entre les résultats de simulation et les résultats expérimentaux pour un échelon sur l'énergie interne du MMC.

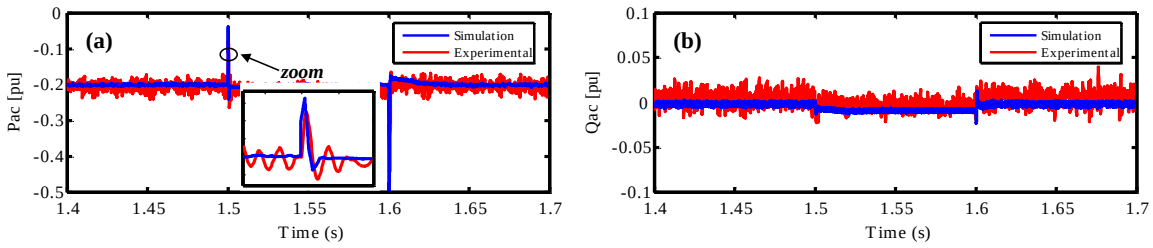

Figure-9: Comparaison entre les résultats de simulation et les résultats expérimentaux pour un creux symétrique de tension AC (50%): (a) la variation de la puissance active, (b) la variation de la puissance réactive.

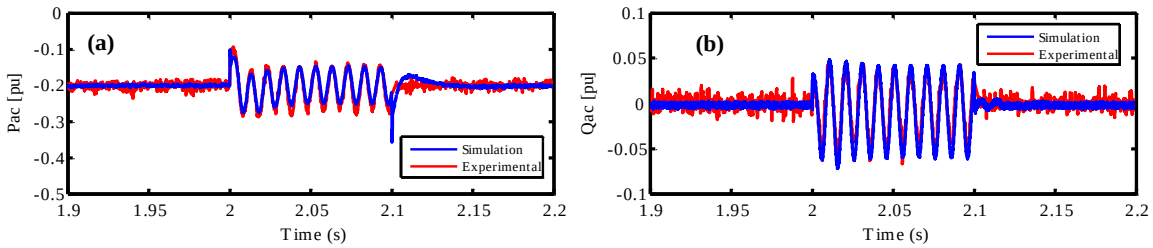

Figure-10: Comparaison entre les résultats de simulation et les résultats expérimentaux pour un creux asymétrique de tension AC (50%): (a) la variation de la puissance active, (b) la variation de la puissance réactive.

APPENDICES

1. Appendix A: Validation of proposed MMC models

1.1. Validation of proposed equivalent models

In this section, the semi-analytical as well as the analytical modeling techniques for the equivalent model are compared to the Benchmark model for all MMC states (controlled, blocked and faulted). As it can be observed from the results presented below, the proposed equivalent models give the same response as the Benchmark one.

1.1.1. Controlled state tests

1.1.1.1. Step change in DC power reference

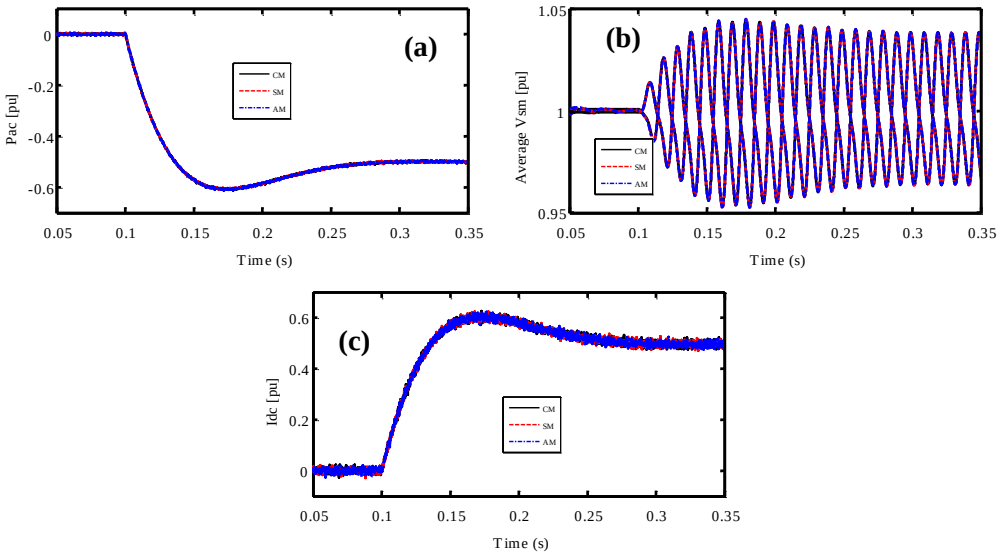

Figure A-1: Dynamics response of equivalent models for a DC power step change: (a) active power, (b) average SM voltages for upper and lower arms for phase a, (c) DC current.

1.1.1.2. Step change in stored energy reference

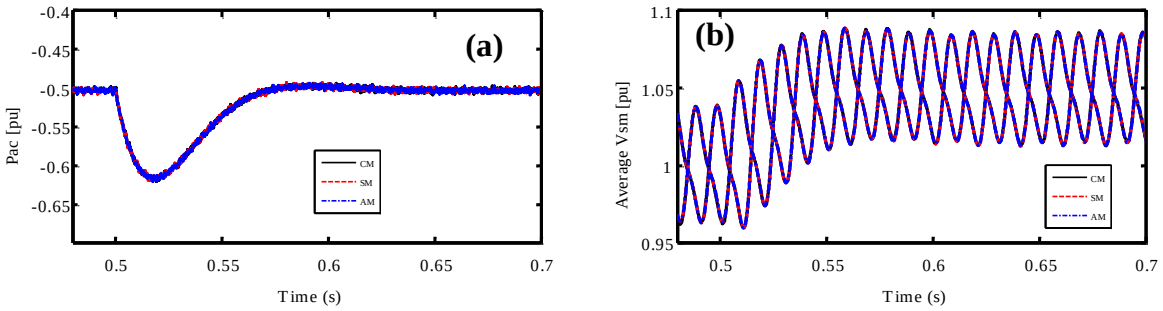

Figure A-2: Dynamics response of equivalent models for a stored energy step change: (a) active power, (b) average SM voltages for upper and lower arms for phase a.

1.1.2. Blocked state tests

1.1.2.1. Three phase AC fault

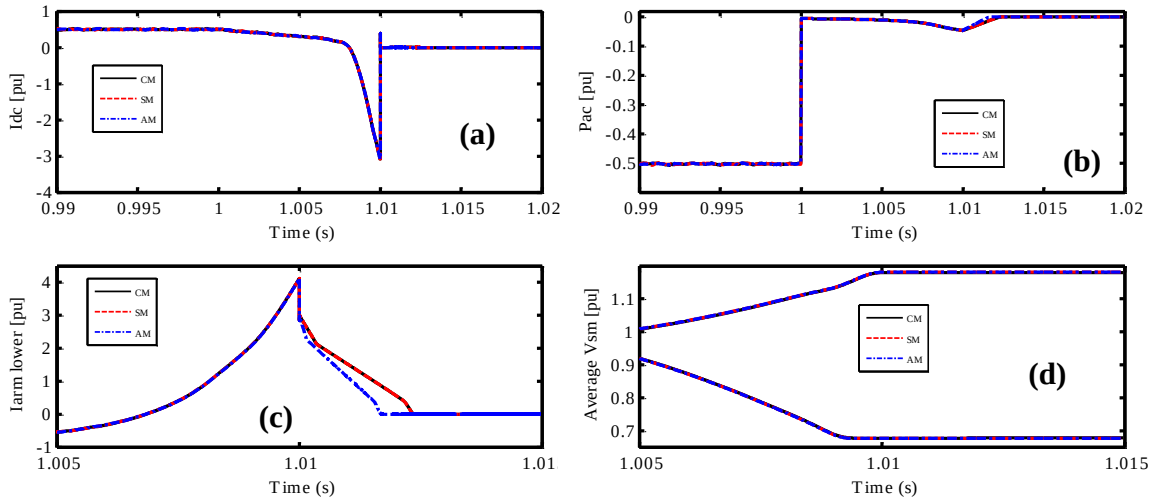

Figure A-3: Dynamics response of equivalent models for a three phase AC fault: (a) DC current, (b) active power, (c) lower arm current for phase (a), (d) average SM voltages for upper and lower arms for phase a.

1.1.2.2. Pole to Pole DC fault

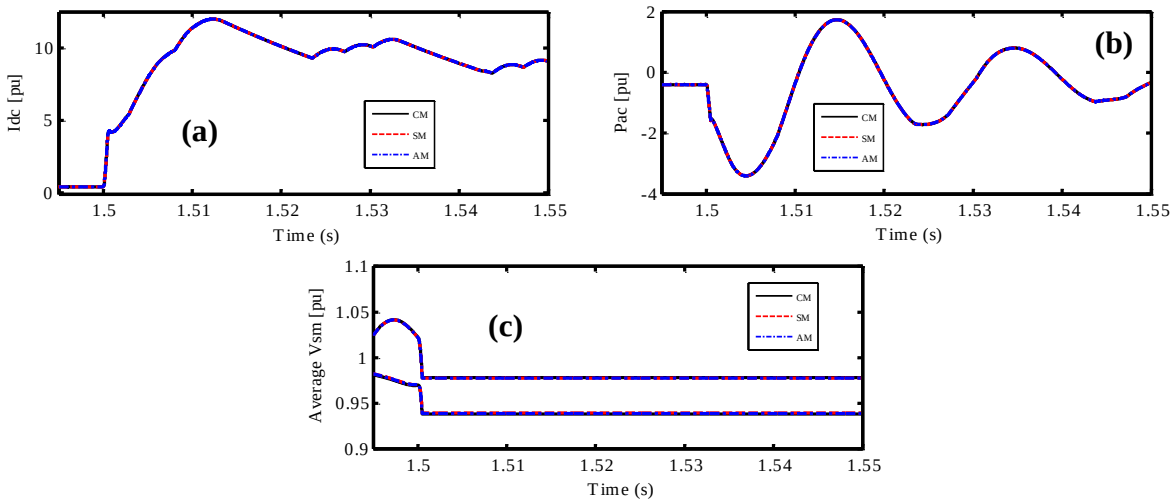

Figure A-4: Dynamics response of equivalent models for a pole-to-pole DC fault: (a) DC current, (b) active power, (c) average SM voltages for upper and lower arms for phase a.

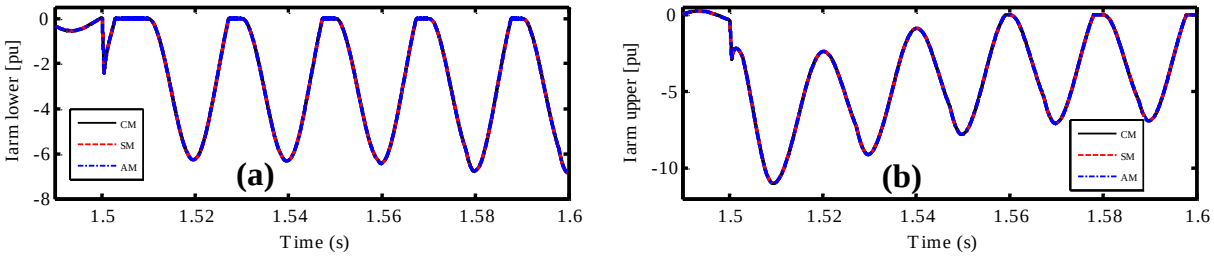

Figure A-5: Arm currents dynamics of equivalent models for a pole-to-pole DC fault.

1.1.3. Faulted state tests

1.1.3.1. Loss of 10% SMs for one arm

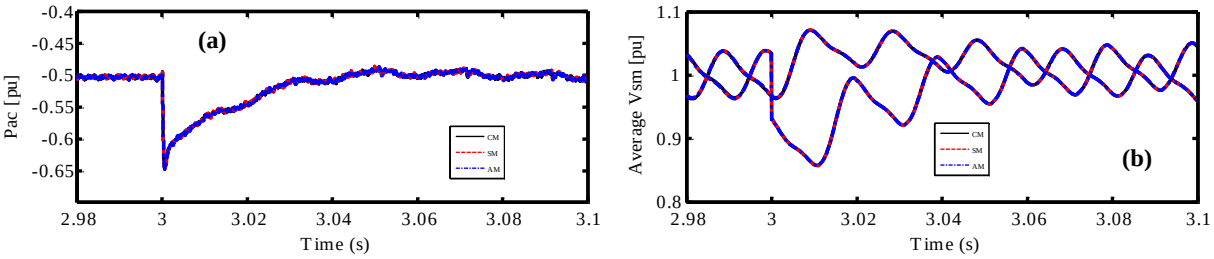

Figure A-6: Dynamics response of equivalent models for a loss of 10% SMs in one arm: (a) active power, (b) average SM voltages for upper and lower arms for phase a.

1.1.3.2. Loss of one arm

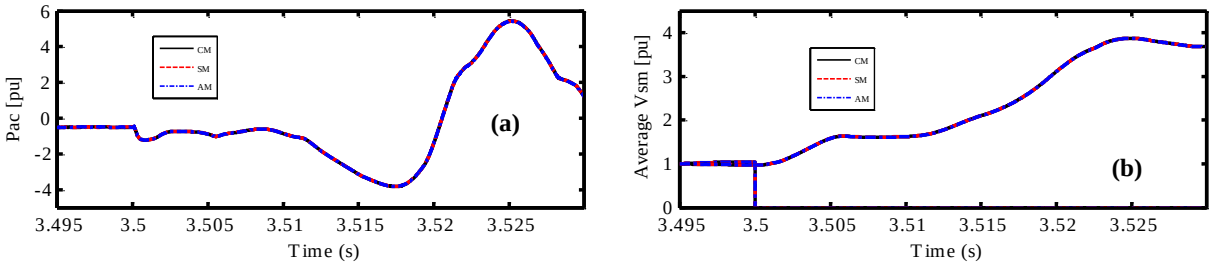

Figure A-7: Dynamics response of equivalent models for a loss of one arm: (a) active power, (b) average SM voltages for upper and lower arms for phase a.

1.2. Validation of proposed averaged models

In this section, the semi analytical as well as the analytical modeling techniques for the equivalent model are compared to the Benchmark model for all MMC states (controlled, blocked and faulted). As for the equivalent model, good correlation between the averaged and Benchmark models results.

1.2.1. Controlled state tests

1.2.1.1. Step change in DC power reference

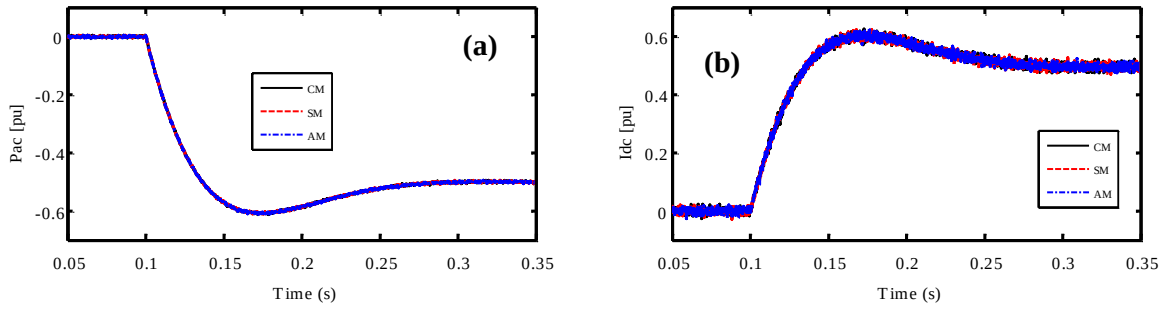

Figure A-8: Dynamics response of averaged models for a DC power step change: (a) active power, (b) DC current.

1.2.1.2. Step change in stored energy reference

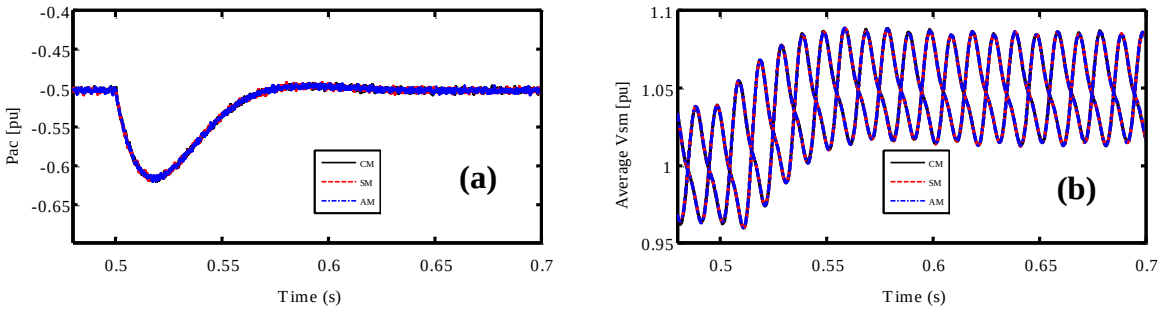

Figure A-9: Dynamics response of averaged models for a stored energy step change: (a) active power, (b) average SM voltages for upper and lower arms for phase a.

1.2.2. Blocked state tests

1.2.2.1. Three phase AC fault

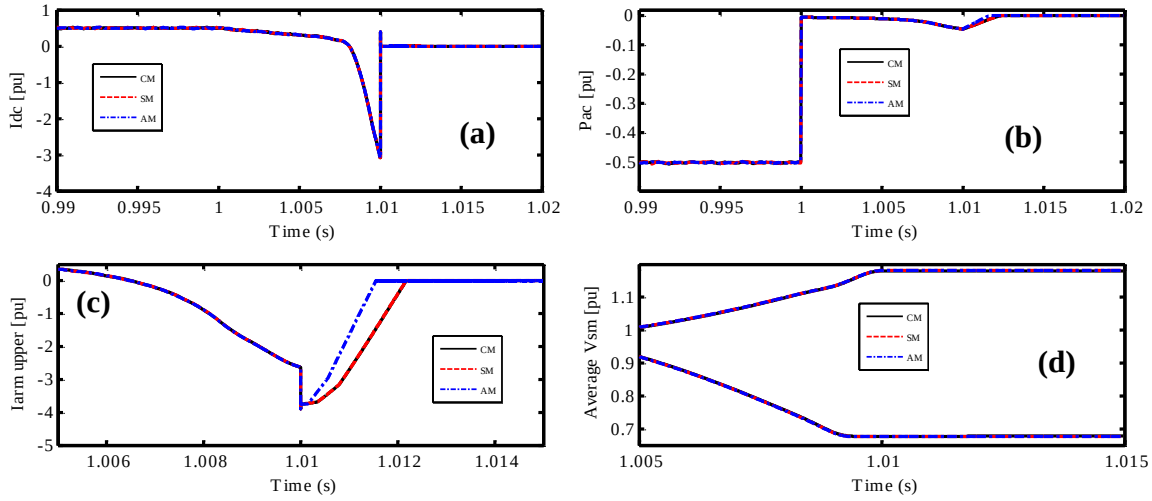

Figure A-10: Dynamics response of averaged models for a three phase AC fault: (a) DC current, (b) active power, (c) upper arm current for phase (a), (d) average SM voltages for upper and lower arms for phase a.

1.2.2.2. Pole to Pole DC fault

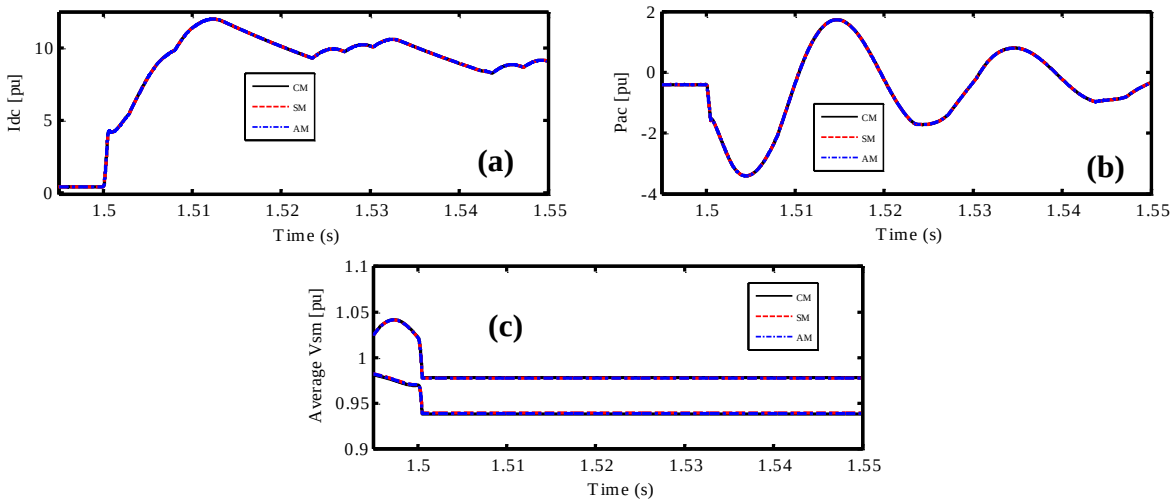

Figure A-11: Dynamics response of averaged models for a pole-to-pole DC fault: (a) DC current, (b) active power, (c) average SM voltages for upper and lower arms for phase a.

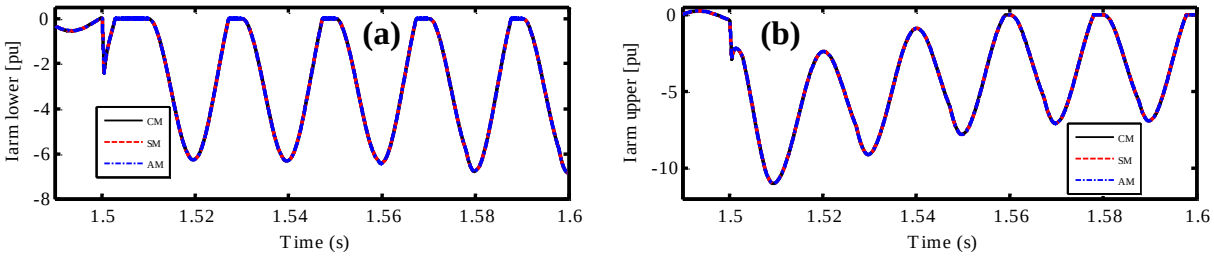

Figure A-12: Arm currents dynamics of averaged models for a pole-to-pole DC fault.

1.2.3. Faulted state tests

1.2.3.1. Loss of 10% SMs for one arm

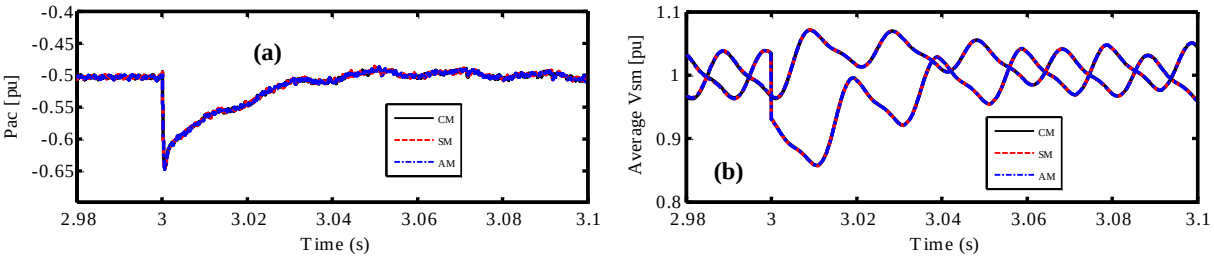

Figure A-13: Dynamics response of averaged models for a loss of 10% SMs in one arm: (a) active power, (b) average SM voltages for upper and lower arms for phase a.

1.2.3.2. Loss of one arm

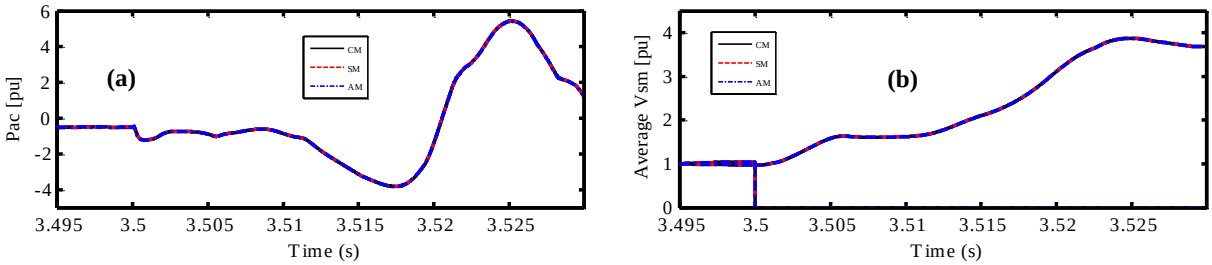

Figure A-14: Dynamics response of averaged models for a loss of one arm: (a) active power, (b) average SM voltages for upper and lower arms for phase a.

2. Appendix B: MMC controllers tuning

In this section, the tuning of MMC control loops are presented and explained.

2.1. DC voltage controller

For DC systems, the DC voltage has the same role as the frequency in AC system. It indicates the grid stability based on input and output powers. Generally, one or several stations have to be controlled in DC voltage mode in order to ensure this objective. For a given station, the equation describing the DC voltage grid variation can be written as follows.

$$C_{dc}\frac{dv_{dc}}{dt} = i_l - i_{dc} \qquad (B\text{-}1)$$

Where:

C_{dc}: The equivalent DC grid capacitor (cables capacitors).

i_l: DC current coming from other stations (DC grid).

When the MMC is controlled in DC voltage mode, the control system has to adapt the DC current (i_{dc}) in order to maintain the stored energy inside the DC grid equal to its reference. The block diagram of DC voltage model can be represented as shown in Figure A-15.

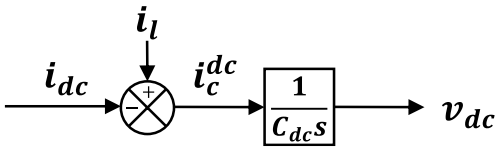

Figure A-15: Block diagram for DC voltage equivalent model.

Based on Figure A-15, a control law for DC voltage controller can be derive. Taking Proportional Integral (PI) as an example, the DC voltage control law is obtained as:

$$i_{dc}^{*} = (v_{dc}^{*} - v_{dc})C_v^{dc}(s) \qquad (B\text{-}2)$$

Where:

$$C_v^{dc}(s) = k_p^{v_{dc}} + \frac{k_i^{v_{dc}}}{s}$$

The gain parameters are tuned according to the closed loop transfer function as it is shown in Figure A-16.

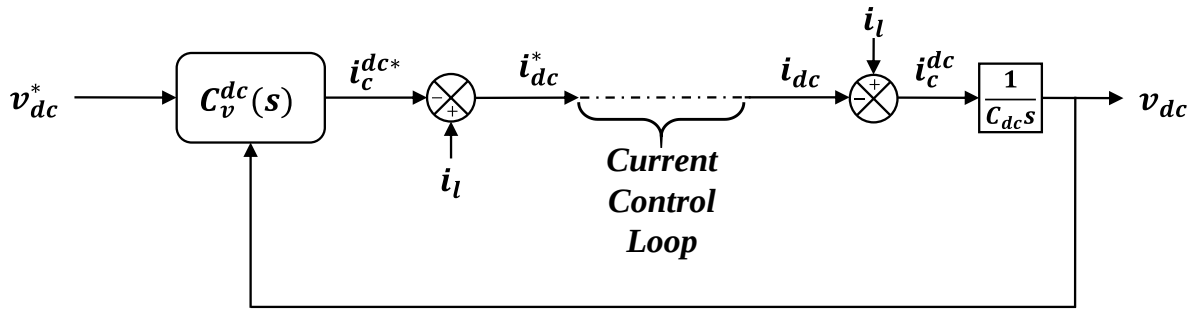

Figure A-16: Block diagram of DC voltage control in closed loop.

According to Figure A-16, the transfer function describing DC voltage variation regarding its reference is given by:

$$\frac{v_{dc}}{v_{dc}^{*}} = \frac{1 + \frac{k_p^{v_{dc}}}{k_i^{v_{dc}}} s}{1 + \frac{k_p^{v_{dc}}}{k_i^{v_{dc}}} s + \frac{C_{dc}}{k_i^{W}} s^2} \qquad (B\text{-}3)$$

Using pole placement method, the obtained dominator of equation (B-3) is compared to the second order characteristic equation known as:

$$P_c(s) = 1 + \frac{2\zeta}{\omega_n} s + \frac{1}{\omega_n} s^2 \qquad (B\text{-}4)$$

Where ω_n and ζ are, respectively, the natural frequency and the damping ratio. They are calculated based on the desired response time and overshoot:

$$\zeta = 0{,}707 \text{ for 5\% overshoot}$$
$$\omega_n = \frac{3}{t_r} \qquad (B\text{-}5)$$

Then, the gains of DC voltage controller are given by:

$$k_i^{v_{dc}} = C_{dc}\left(\omega_n^{v_{dc}}\right)^2$$
$$k_p^{v_{dc}} = 2\zeta C_{dc}\omega_n^{v_{dc}} \qquad (B\text{-}6)$$

2.2. Energy global controller

As a reminder, the state space equation representing the energy global variation is given by the following expression:

$$\frac{dW_{mmc}}{dt} = P_{dc} - P_{ac} \qquad (B\text{-}7)$$

Where the global energy is defined as follows:

$$W_{mmc} = \sum_{i=a}^{c} W_i^u + W_i^l \qquad (B\text{-}8)$$

Based on equations (B-7), the block diagram representing the energy global model is given in Figure A-17.

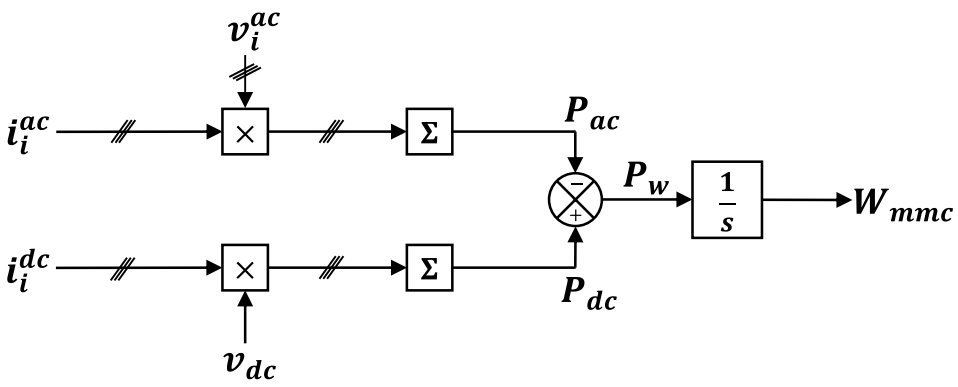

Figure A-17: Block diagram for MMC energy equivalent model.

It is worth noticing that the block diagram is given in SI system. The electrostatic constant needs to be considered when the block diagram is given in pu system.

It can be observed that the control objective (energy regulation) can be achieved by creating an unbalanced between AC and DC powers. Hence, two strategies can be employed for this purpose:

- DC Control strategy.
- AC Control strategy.

Taking the first case (DC control strategy) as an example, the energy controller has to adjust the DC power reference till the stored energy becomes equal to its reference value. The DC power reference in this case is given by the following expression:

$$P_{dc}^{*} = P_{ac}^{*} + P_{w}^{*} \tag{B-9}$$

Where P_{W}^{*} represents the output of energy loop controller.

$$P_{w}^{*} = (W_{mmc}^{*} - W_{mmc})C_{w}(s) \tag{B-10}$$

The block diagram of energy loop in closed loop is presented in Figure A-18.

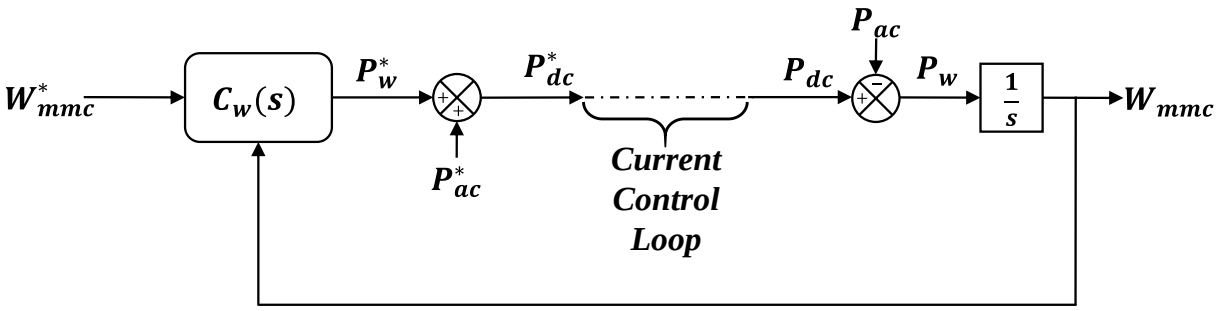

Figure A-18: Block diagram of energy control in closed loop.

When a PI regulator is used to derive the energy controller, its gains can be calculated using the transfer function of Figure A-18. That is:

$$\frac{W_{mmc}}{W_{mmc}^{*}} = \frac{1 + \frac{k_p^w}{k_i^w} s}{1 + \frac{k_p^w}{k_i^w} s + \frac{1}{k_i^w} s^2} \tag{B-11}$$

As before, using pole placement method, the denominator of this transfer function is compared to the desired characteristic equation. After calculation, the gains values are:

$$\begin{aligned} k_i^w &= (\omega_n^w)^2 \\ k_p^w &= 2\zeta\omega_n^w \end{aligned} \tag{B-12}$$

2.3. Energy leg (sum) controller

As a reminder, the state space equation representing the energy sum variation is given by the following expression where its block diagram is presented in Figure A-19:

$$\langle \Delta W_i^{\Sigma} \rangle = \int_0^{2\pi} v_{mi}^{dc}\, i_i^{dc} - v_{mi}^{ac}\, i_i^{ac} = P_i^{dc} - P_i^{ac} \qquad \text{(B-13)}$$

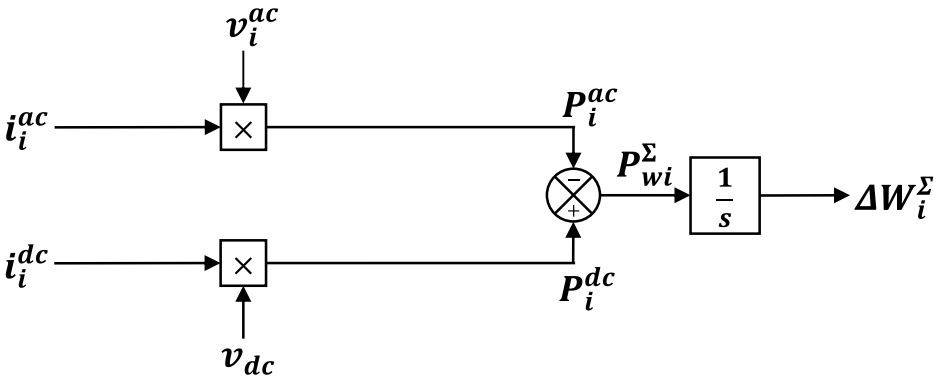

Figure A-19: Block diagram of energy leg (sum) equivalent model.

As for the global energy, the energy leg controller can be achieved either with the AC currents or with the DC one. In order to avoid an unbalanced operation conditions, it is better to use the DC current for this purpose.

The equation (B-13) shows that the instantaneous energy leg contains (2ω) frequency component. Since the aim is controlling the average value of the stored energy in the leg, it is necessary to eliminate this frequency using a filter (e.g Notch filter).

Once the signal is filtered, the energy leg controller can be derived as follows:

$$P_{wi}^{\Sigma *} = (\Delta W_i^{\Sigma *} - \langle \Delta W_i^{\Sigma} \rangle) C_{\Sigma}^{w}(s) \qquad \text{(B-14)}$$

The block diagram of energy leg loop in closed loop is presented in Figure A-20.

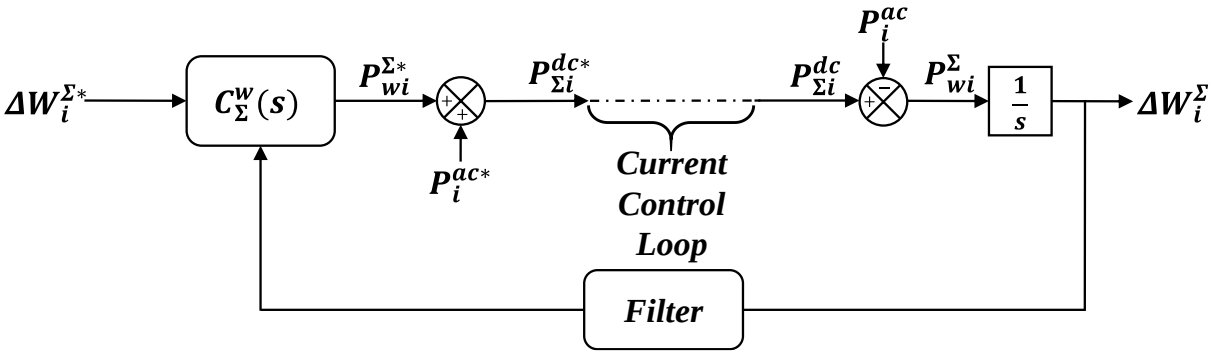

Figure A-20: Block diagram of energy leg (sum) control in closed loop.

The tuning of control gains can be obtained using the same approach as before.

2.4. Energy difference controller

As a reminder, the state space equation representing the energy difference variation is given by the following expression:

$$\langle \Delta W_i^{\Sigma} \rangle = \int_0^{2\pi} 2\, v_{mi}^{ac}\, i_i^{dc} - \frac{v_{mi}^{dc}}{2}\, i_i^{ac} \qquad \textit{(B-15)}$$

The equation (B-15) can be represented with a block diagram as follows:

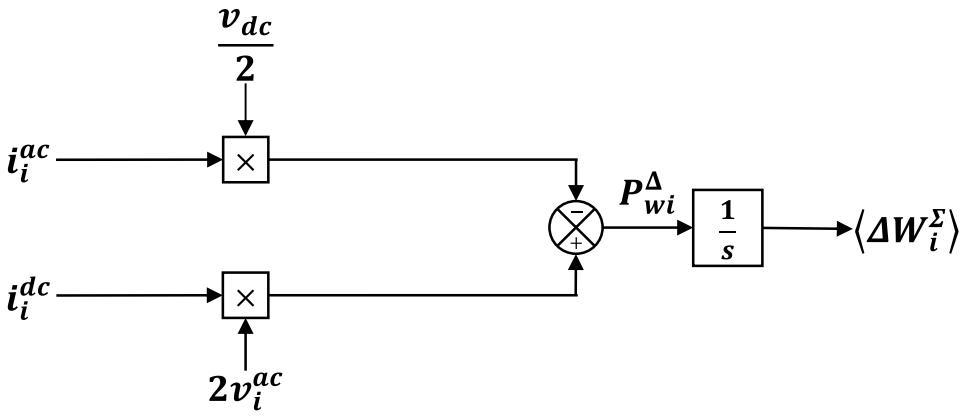

Figure A-21: Block diagram of energy difference equivalent model.

The block diagram in closed loop is then:

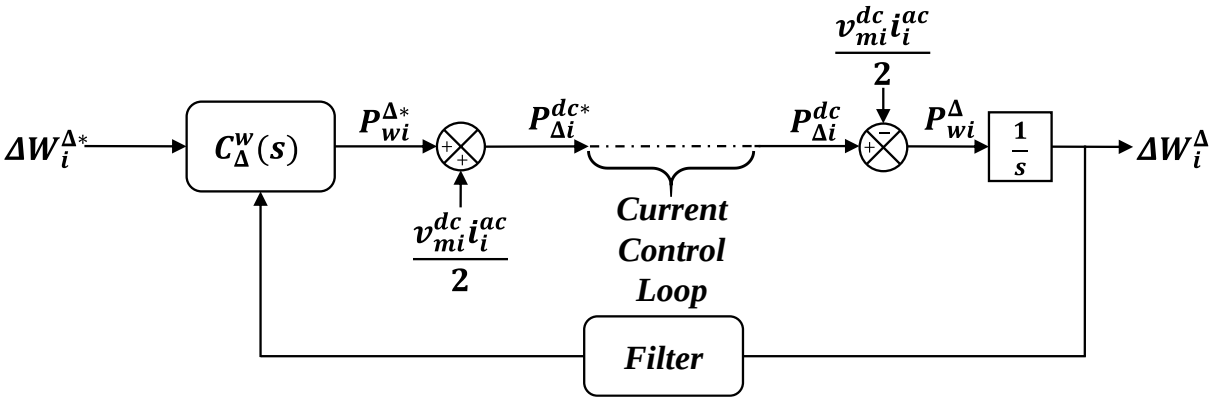

Figure A-22: Block diagram of energy difference control in closed loop.

2.5. Phase locked loop

In order to connect a MMC (VSC) to AC grid, the control has to detect the frequency as well as the angle of the connected grid. This step is performed using Phase Locked Loop (PLL). It can be also used to perform a vector control for AC currents based on a rotating frame ($dq0$). This control philosophy allows to control continuous components instead of sinewave ones. In this rotating frame, the active and reactive powers can be calculated using the following expressions:

$$P_{ac} = v_d^{ac} i_d^{ac} + v_q^{ac} i_q^{ac}$$
$$Q_{ac} = v_q^{ac} i_d^{ac} - v_d^{ac} i_q^{ac} \quad \textit{(B-16)}$$

In addition to calculate the direct and quadrature components of AC currents, the PLL allows to control the active and reactive powers independently. To do so, The PLL has to set the quadrature component of AC voltage to zero. The equations (B-16) then become:

$$P_{ac} = v_d^{ac} i_d^{ac}$$
$$Q_{ac} = -v_d^{ac} i_q^{ac} \quad \textit{(B-17)}$$

3. Appendix C: High dynamics MMC control based on MMC arm current controllers

3.1. Introduction

In this section, high dynamics controllers for internal MMC current (arm currents) are proposed. Since the analysis in the three phase is the same, only one phase is considered in the following development. Since the discrete-time controllers have shown several advantages compared to continuous ones, this control philosophy is used to derive arm current controllers.

As a reminder (see CHAPTER III, section 4.1), the state-space equation describing the MMC arm currents for phase i can be written as follows:

$$\begin{bmatrix} \frac{di_i^u}{dt} \\ \frac{di_i^l}{dt} \end{bmatrix} = E \begin{bmatrix} i_i^u \\ i_i^l \end{bmatrix} + J \begin{bmatrix} v_{rli}^u \\ v_{rli}^l \end{bmatrix} \qquad (C\text{-}1)$$

Where:

$$E = \begin{bmatrix} -(L_{arm} + L_f) & L_f \\ -L_f & (L_{arm} + L_f) \end{bmatrix}^{-1} \begin{bmatrix} (R_{arm} + R) & -R \\ R & -(R_{arm} + R_f) \end{bmatrix}$$

$$J = \begin{bmatrix} -(L_{arm} + L_f) & L_f \\ -L_f & (L_{arm} + L_f) \end{bmatrix}^{-1}$$

$$\begin{bmatrix} v_{rli}^u \\ v_{rli}^l \end{bmatrix} = \begin{bmatrix} v_{mi}^u - \frac{v_{dc}}{2} + v_i^{ac} \\ v_{mi}^l + \frac{v_{dc}}{2} + v_i^{ac} \end{bmatrix}$$

After calculation, the matrices E and J are given by the following expressions:

$$E = \begin{bmatrix} -\frac{L_{arm}R_{arm} + L_{arm}R_f + L_f R_{arm}}{L_{arm}(L_{arm} + 2\,L_f)} & \frac{L_{arm}R_f - L_f R_{arm}}{L_{arm}(L_{arm} + 2\,L_f)} \\ \frac{L_{arm}R_f - L_f R_{arm}}{L_{arm}(L_{arm} + 2\,L_f)} & -\frac{L_{arm}R_{arm} + L_{arm}R_f + L_f R_{arm}}{L_{arm}(L_{arm} + 2\,L_f)} \end{bmatrix}$$

$$J = \begin{bmatrix} -\dfrac{L_{arm}+L_f}{L_{arm}\left(L_{arm}+2\,L_f\right)} & \dfrac{L_f}{L_{arm}\left(L_{arm}+2\,L_f\right)} \\ -\dfrac{L_f}{L_{arm}\left(L_{arm}+2\,L_f\right)} & \dfrac{L_f}{L_{arm}\left(L_{arm}+2\,L_f\right)} \end{bmatrix}$$

The model (C-1) offers the possibility to derive the control laws for arm currents by controlling the values of v_{rli}^{u} and v_{rli}^{l} (input vector).

3.2. Exact discrete-time MMC modeling

Thanks to the linearity of equation, the exact discrete-time model for arm currents can be written as follows:

$$\begin{bmatrix} i_i^u(t_n+T) \\ i_i^l(t_n+T) \end{bmatrix} = L(T)\begin{bmatrix} i_i^u(t_n) \\ i_i^l(t_n) \end{bmatrix} + M(T)\begin{bmatrix} v_{rli}^u\,(t_n) \\ v_{rli}^l\,(t_n) \end{bmatrix} \qquad \textit{(C-2)}$$

After calculation of $e^{E\,T}$ using equation (IV-31), the matrices $L(T)$ and $M(T)$ are given by the following expressions:

$$L(T) = e^{E\,T} = \begin{bmatrix} \dfrac{1}{2}e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} + \dfrac{1}{2}e^{-T\left(\frac{R_{arm}+2\,R_f}{L_{arm}+2\,L_f}\right)} & \dfrac{1}{2}e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} - \dfrac{1}{2}e^{-T\left(\frac{R_{arm}+2\,R_f}{L_{arm}+2\,L_f}\right)} \\ \dfrac{1}{2}e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} - \dfrac{1}{2}e^{-T\left(\frac{R_{arm}+2\,R_f}{L_{arm}+2\,L_f}\right)} & \dfrac{1}{2}e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} + \dfrac{1}{2}e^{-T\left(\frac{R_{arm}+2\,R_f}{L_{arm}+2\,L_f}\right)} \end{bmatrix}$$

$$M(T) = E^{-1}(e^{E\,T} - I)\,J = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}$$

$$M_{11} = \frac{1}{2}\frac{R_{arm}\,e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} + 2\,R_f e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} + R_{arm}\,e^{-T\left(\frac{R_{arm}+2\,R_f}{L_{arm}+2\,L_f}\right)} - 2\,R_{arm} - 2\,R_f}{R_{arm}\left(R_{arm}+2\,R_f\right)}$$

$$M_{12} = -\frac{1}{2}\frac{R_{arm}\,e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} + 2\,R_f e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} - R_{arm}\,e^{-T\left(\frac{R_{arm}+2\,R_f}{L_{arm}+2\,L_f}\right)} - 2\,R_f}{R_{arm}\left(R_{arm}+2\,R_f\right)}$$

$$M_{21} = \frac{1}{2}\frac{R_{arm}\,e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} + 2\,R_f e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} - R_{arm}\,e^{-T\left(\frac{R_{arm}+2\,R_f}{L_{arm}+2\,L_f}\right)} - 2\,R_f}{R_{arm}\left(R_{arm}+2\,R_f\right)}$$

$$M_{22} = -\frac{1}{2}\frac{R_{arm}\,e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} + 2\,R_f e^{-T\left(\frac{R_{arm}}{L_{arm}}\right)} + R_{arm}\,e^{-T\left(\frac{R_{arm}+2\,R_f}{L_{arm}+2\,L_f}\right)} - 2\,R_{arm} - 2\,R_f}{R_{arm}\left(R_{arm}+2\,R_f\right)}$$

3.3. Discrete-time controllers based on pole placement method

In order to obtain the fastest dynamics for arm currents, a placement pole method is chosen to derive their control laws. Based on the convergence condition given in equation (IV-34), the arm discrete-time controller has to satisfy the following condition:

$$\begin{bmatrix} i_i^u(t_n+T) - i_i^{u*} \\ i_i^l(t_n+T) - i_i^{l*} \end{bmatrix} = K_g^{arm} \begin{bmatrix} i_i^u(t_n) - i_i^{u*} \\ i_i^l(t_n) - i_i^{l*} \end{bmatrix} \quad (C\text{-}3)$$

Replacing $i_i^{u,l}(t_n+T)$ by its equation (C-2), the condition (C-3) becomes:

$$L(T)\begin{bmatrix} i_i^u(t_n) \\ i_i^l(t_n) \end{bmatrix} + M(T)\begin{bmatrix} v_{rli}^u(t_n) \\ v_{rli}^l(t_n) \end{bmatrix} - \begin{bmatrix} i_i^{u*} \\ i_i^{l*} \end{bmatrix} = K_g^{arm} \begin{bmatrix} i_i^u(t_n) - i_i^{u*} \\ i_i^l(t_n) - i_i^{l*} \end{bmatrix} \quad (C\text{-}4)$$

Then, the control law for arm currents controller can be written as:

$$\begin{bmatrix} v_{rli}^u(t_n) \\ v_{rli}^l(t_n) \end{bmatrix} = M(T)^{-1}\left[L(T)\begin{bmatrix} i_i^u(t_n) \\ i_i^l(t_n) \end{bmatrix} + K_g^{arm}\begin{bmatrix} i_i^u(t_n) - i_i^{u*} \\ i_i^l(t_n) - i_i^{l*} \end{bmatrix} + \begin{bmatrix} i_i^{u*} \\ i_i^{l*} \end{bmatrix} \right] \quad (C\text{-}5)$$

3.4. Offline validation

The obtained control laws are tested with the simulation circuit of Figure IV-31. The same parameters with the same events are used in order to be in line with the obtained results in CHAPTER IV, section 3.4.

3.4.1. High dynamics test

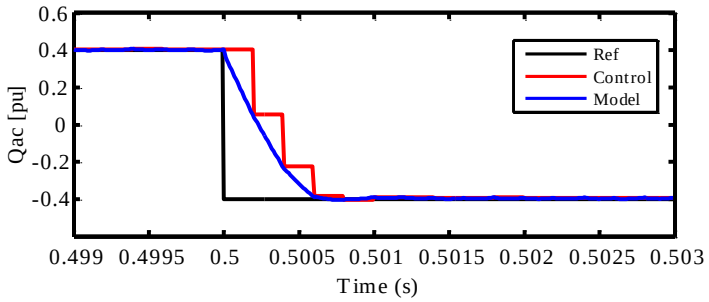

Figure A-23: Zoom on reactive power dynamics with 0.2 ms sampling period.

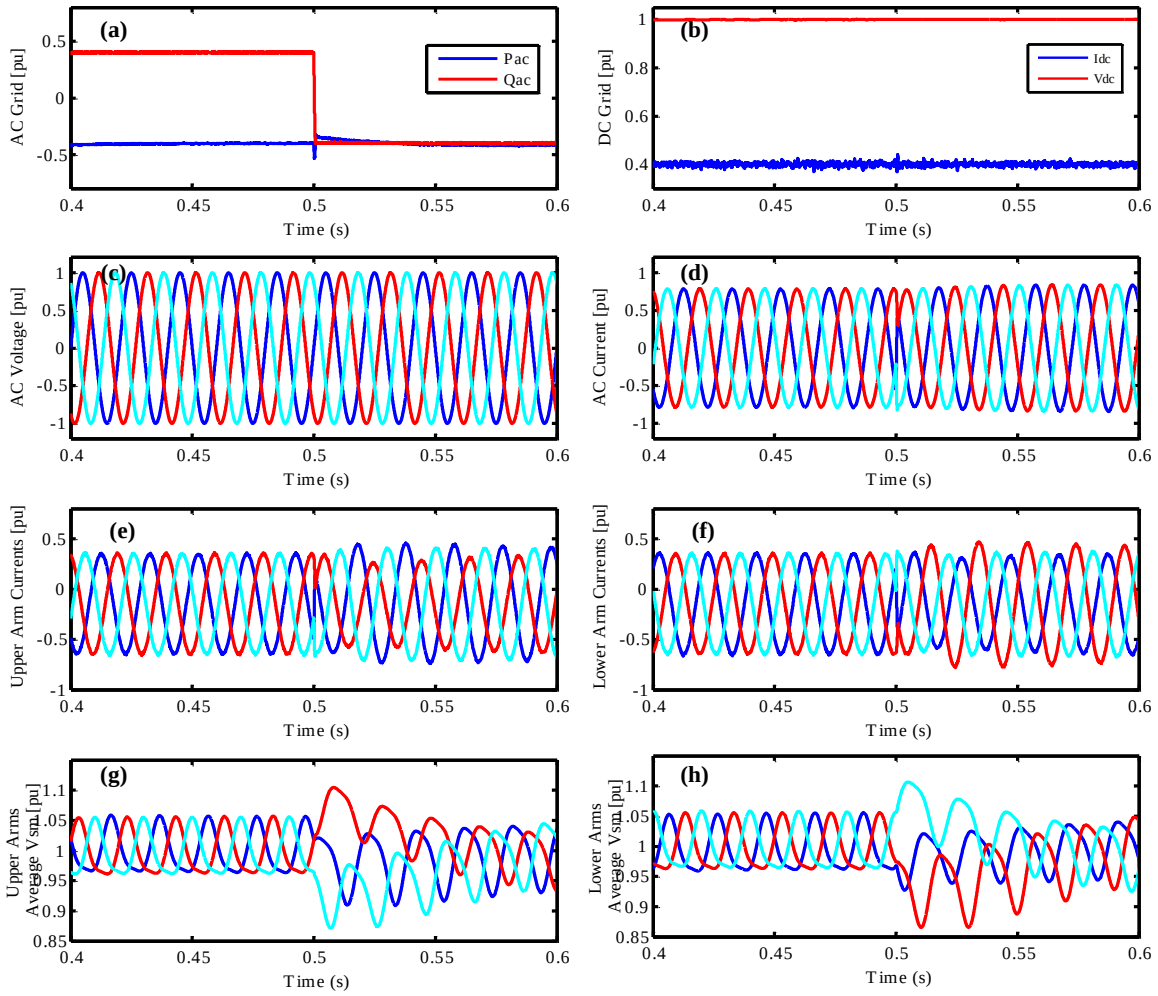

Figure A-24: Simulation results with 0.2 ms sampling period: (a) active and reactive power, (b) DC current with DC voltage, (c) AC voltages, (d) AC currents, (e) upper arm currents, (f) lower arm currents, (g) average SM voltages for upper arms, (h) average SM voltages for lower arms.

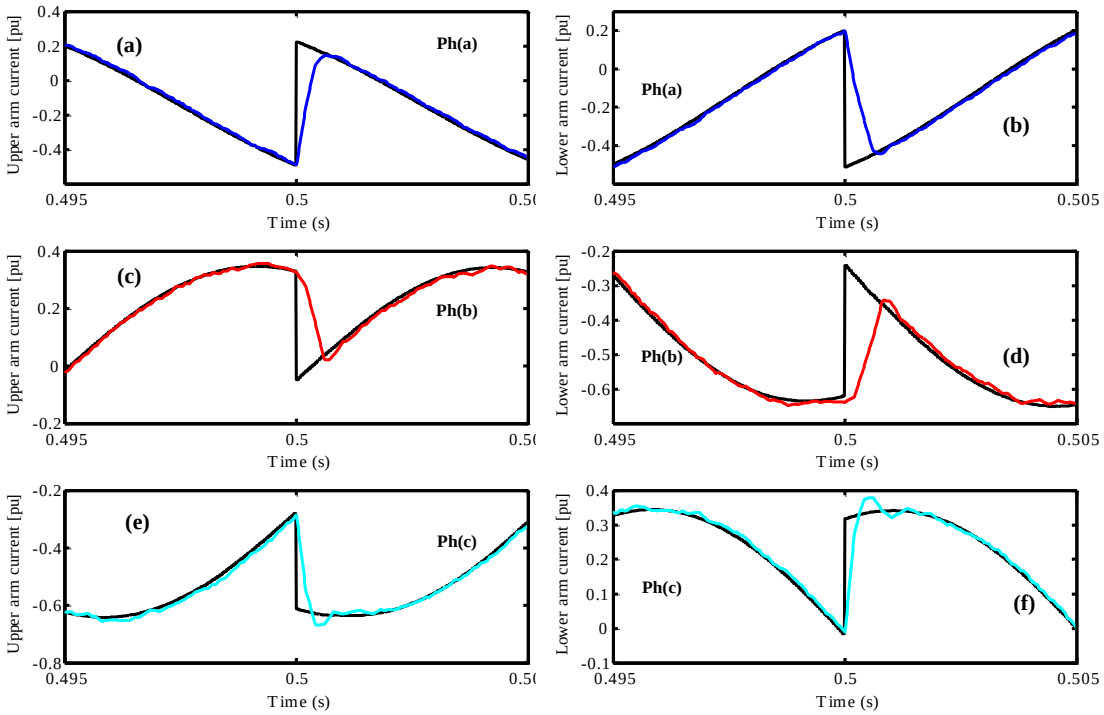

Figure A-25: Zoom on arm current results with 0.2 ms sampling period.

3.4.2. Symmetric ac voltage dip

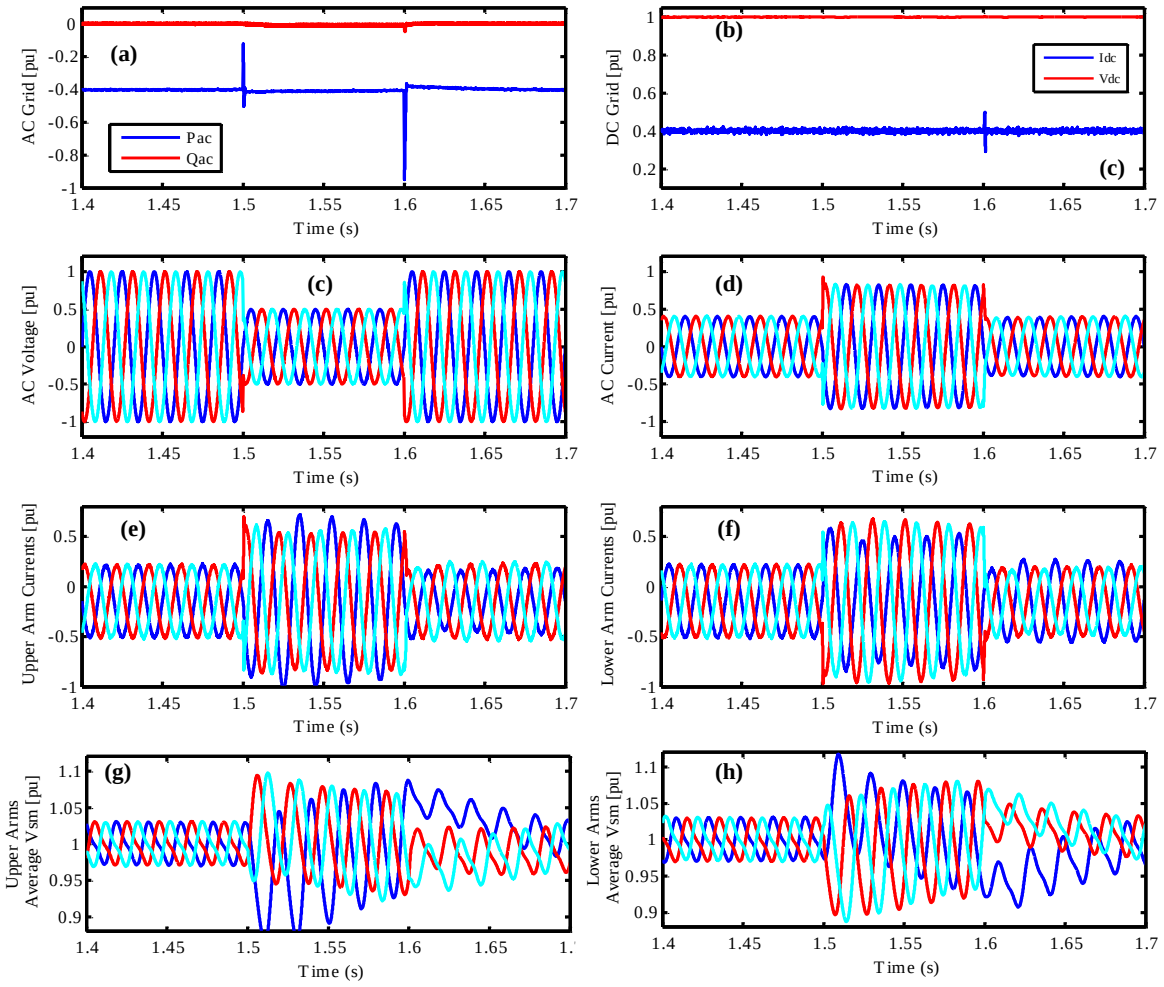

Figure A-26: Simulation results for symmetrical AC voltage dip with 0.2 ms sampling period: (a) active and reactive power, (b) DC current with DC voltage, (c) AC voltages, (d) AC currents, (e) upper arm currents, (f) lower arm currents, (g) average SM voltages for upper arms, (h) average SM voltages for lower arms.

3.4.3. Asymmetric ac voltage dip

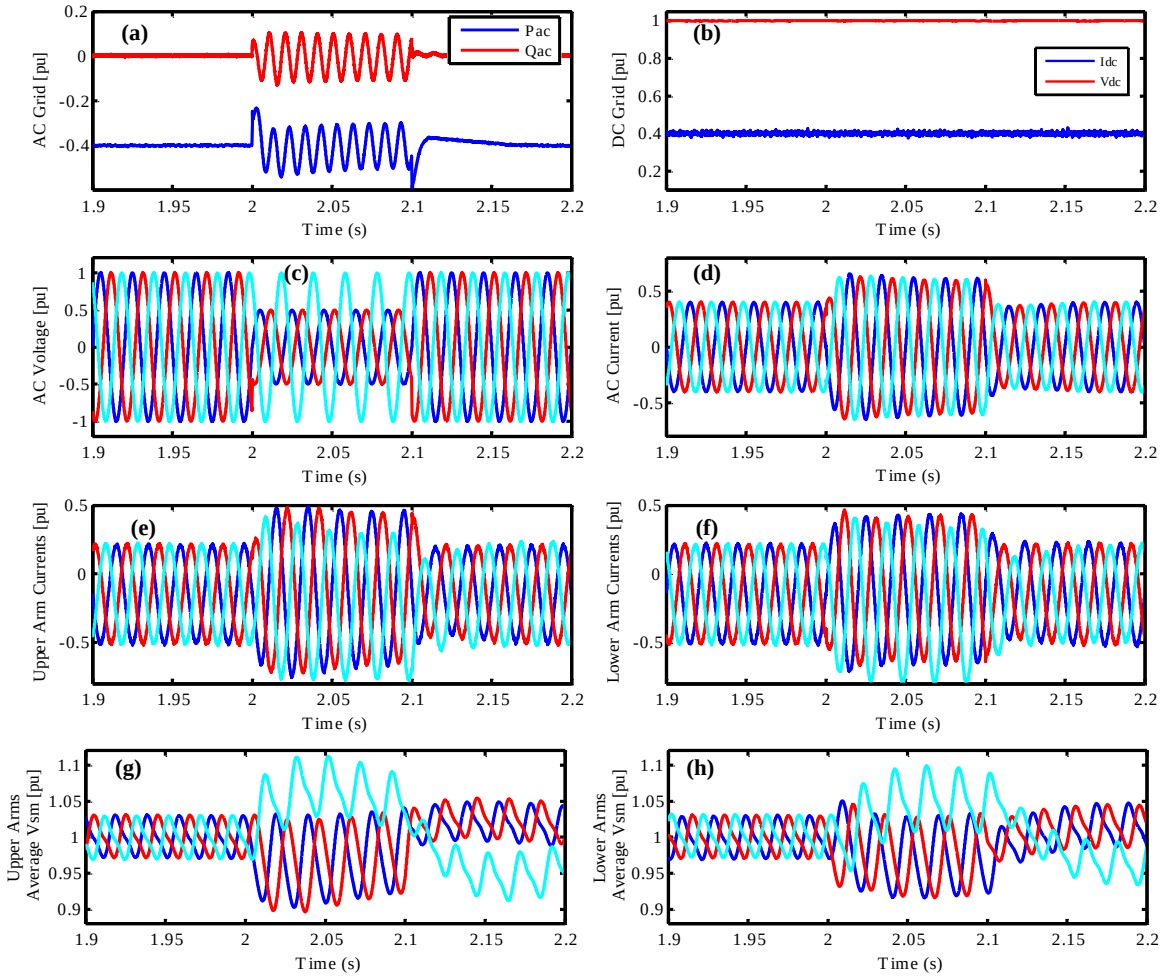

Figure A-27: Simulation results for asymmetrical AC voltage dip with 0.2 ms sampling period: (a) active and reactive power, (b) DC current with DC voltage, (c) AC voltages, (d) AC currents, (e) upper arm currents, (f) lower arm currents, (g) average SM voltages for upper arms, (h) average SM voltages for lower arms