First order Electro-thermal compact models and noise considerations for three-dimensional integration circuits

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Contents

Chapter 1: Introduction

AI (Artificial intelligence) is a very fresh and hot topic application area that can benefit from the 3D IC. Google AlphaGo and IBM Watson's Jeopardy defeat the best human Shogi player, but they all ran on server clusters, which are too difficult for widespread use. Today automatic driving technique uses more specialized processors, but the automobiles are not safe enough. The safety need will require more sophisticated control systems that are likely to increase computational requirements.

As we know from "von Neumann bottleneck", data moves between the separate MPU (microprocessor unit) and memory. In this case, latency is unavoidable. These years, processor speeds have increased significantly to about 4.2 GHz. But the memory improves mostly in the density, that's to say that the memory can store more data in a fixed space, rather than in the augmentation of transfer rates. As MPU working frequency has increased, the processor has spent an increasing amount of waiting time, in order to write and read from memory. So no matter how fast the MPU can work, it is limited by the memory transfer rate. [1], [2]

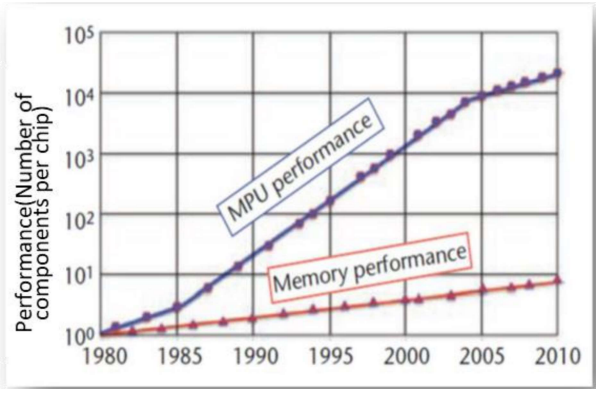


Figure 1 Performance (speed) gap between MPU and memory increasing with time[3] (Performance's unit is number of transistors per unit cm^2)

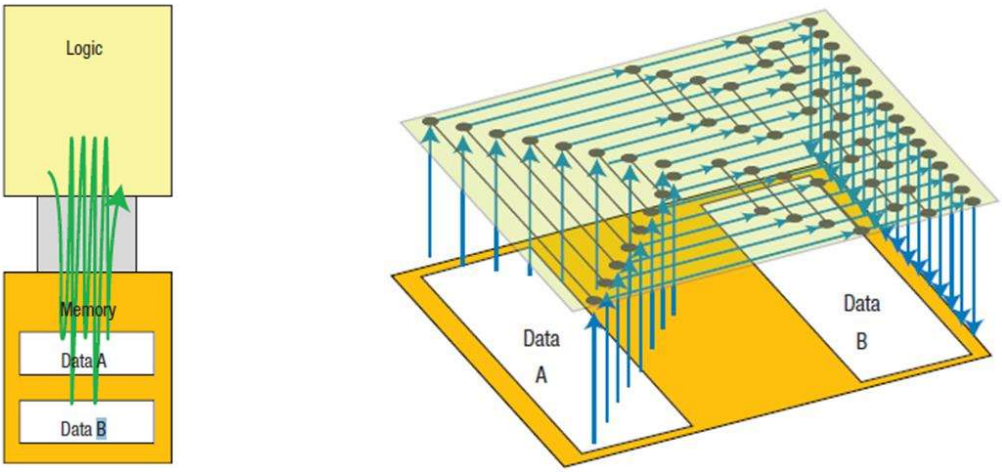
So the next generation of AI architectures is emerging the need for more densely integrated memory and processor. For example, the memory occupies a very big space in the IBM's TrueNorth neural network chip, Google TensorFlow and the new generation of GPUs used in automatic driving cars have huge memories.

1.1) From Two-Dimension (2D) IC to Three-Dimension (3D) IC

As Figure 2a illustrates, a traditional von Neumann computer system is the heterogeneous integration of logic cells (yellow), memory chips (orange), and the interconnections (gray). For example, here Data A saves the data from RF electronics, Data B saves data from camera sensors,

the dynamic random-access memory (DRAM) process has a 10× higher memory density than the same generation's logic cell. So the cache in the MPU is too small for the implementation of memory, and the data must inevitably be moved through the high-energy loss route between logic and memory, twice per communication (as shown in the green line).

Figure 2b shows the equivalent data-transmission route for one merge stage of a bitonic sort. The light yellow logic layer on top (with black points) shows the merging of four stages of bitonic sort. When applying the structure in Figure 2b, the comparisons and exchange can be placed on the logic layer. Data to be calculated (Data A) and a place of storage (Data B) are located in the bottom orange memory and connected through short wires crossing the large 2D plane, rather than a border.



(a) (b)

Figure 2 Advantage of 3D for interconnections. (a) 2D systems comprise logic and memory chips, with the green curve illustrating a mixed logic–memory calculation that's inefficient precisely because of this logic and memory partitioning. (b) 3D systems with tight coupling between logic and memory avoid high latency paths, bandwidth bottlenecks, and conversion of signals to high energy levels for off-chip interconnects. The blue curve shows a representative data-movement step in sorting.

For the 3D structure in Figure 2b, data can be read all at once from memory, and then compared and exchanged in hardware. A traditional computer will need to transport all the data from memory to the processor sequentially, so, the memory bottleneck becomes a principal issue when processing a huge amount of data and other low-level kernels in artificial intelligence (AI). So the 3D circuits has a better advantage.

Moore's Law seems to be showing down. Because of the physics limits, the technical challenges of continuously miniaturization are difficult to overcome, which is increasing the cost and slowing the pace of scaling. In addition, the benefits of scaling are decreased because of the mismatch between the scaling and the former performance advantages. So the future semiconductor industry focuses on two technical issues. Functional diversification is the first direction. It is the main driving force of System-In-Package (SiP) architecture. The second one is 3D IC, as shown in the Figure 3. This can gain the functionalities of one given node and also

increases performance and reduces power supply. There are several driving factors for 3D integration. The benefits include better performance, reduced power supply, reduced latency, lower cost and smaller size compared to 2.5D and 2D plane packaging. Some of the basic driving factors for 3D integration are presented in the Figure 4 below.[4]

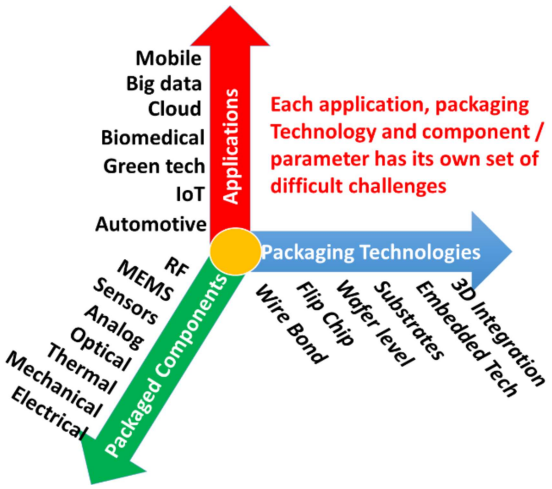


Figure 3 Elements incorporated into complex SiP packages through heterogeneous integration

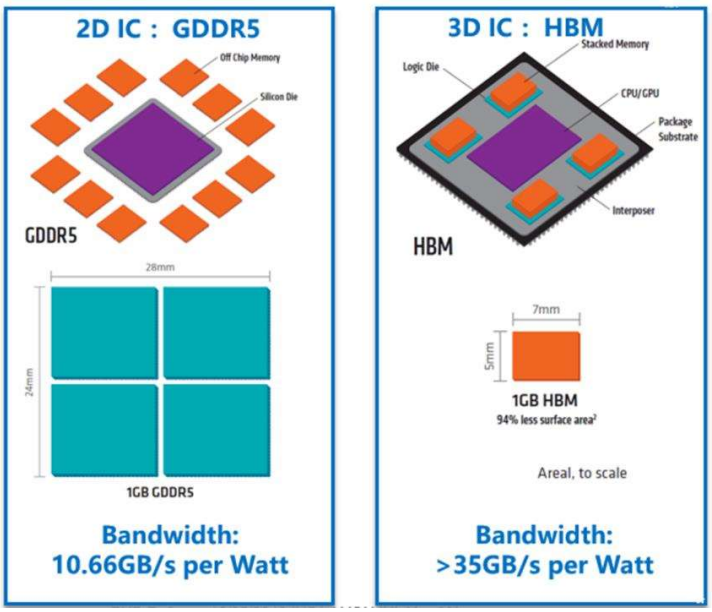


Figure 4 Driving forces for 3D Integration[5], [6]

3D IC leads to a revolution of potential new scale-up. The interconnections between logic and memory has restricted systems for decades. Solving this bottleneck could continue improving system performance and advancing semiconductor industry. However, in order to get the advances, it needs some more time to work through the engineering processes (as shown in Figure 4 and Figure 5). But every little breakthrough in the engineering processes will reduce the von Neumann

bottleneck's impact. For applications that could benefit from denser integration, this could offer continuous performance increases as linewidth scaling.

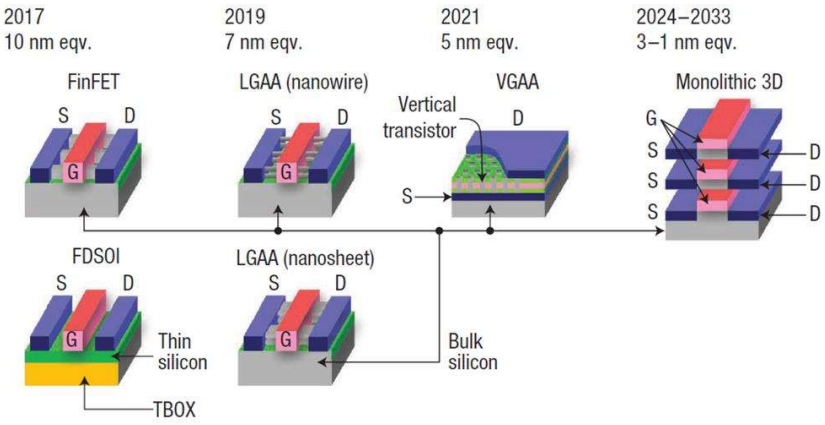


Figure 5 Preview of the 2017 International Roadmap for Devices and Systems' predictions for future 3D structures. D: drain; FDSOI: fully depleted silicon on insulator; G: gate; LGAA: lateral gate-all-around; S: source; TBOX: thin buried oxide; VGAA: vertical gate-all-around[2]

1.2) Roadmap of 3D Integrated Circuits

Computing performance can be substantially improved by monolithically integrating several new heterogeneous memory layers on top of logic layers powered by a combination of CMOS and "new switch" transistors. This new phase, called 3D power scaling, will continue to support an increase in transistor count at Moore's law pace well into the next decade. ——Computing in science & engineering March/ April 2017, vol.19, No.2.

The 2D integration will reach the point where no more 2D scaling will be possible, the death of Moore's law is spoken out everywhere, but the development of vertical integration of transistors and integration of layers of vertical transistors is on the way to continue increasing the transistors' density per cm^2 at a same or faster velocity than Moore's law in the future.

The 2017 IRDS (International Roadmap for Device and System) road map projects the development of integrated-circuit technology for the next 15 years. Figure 5 offers a preview[2]. As we can see, 2D planar scaling in accordance with Moore's law is predicted to end until the mid-2020s, after which further advances will come mainly from the stack of layers. This miniaturization will reduce die purchase fee, energy costs and operational benefits[7]. This evolution demonstrates that 3D VLSI offers the possibility to stack devices and enable high-density interconnects at device level (100 million "via" per mm^2), as Table 1 shows. 3D packaging has been available for decades in large scale, with interconnections, performance, and energy efficiency. Fully integrated 3D (3D Monolithic) is supposed to be available in less than one decade.

Table 1 Evolution of 3D integration options toward 3D VLSI[1]

Options	Links	Bandwidth	Latency	Power	Time frame
Wire-bond stack	100s	Low	High	High	Available for 30 years
Through silicon via (TSV) or microbump stack	1,000s	Medium	Medium	Medium	Available for 10 years
3D VLSI stack	100,000s	High	Low	Low	<10years

In the 1970s, two fundamental laws became the footstones for the whole industry: Moore's and Dennard's scaling laws. Dennard's scaling law presented how to improve transistor performance by means of geometrical scaling. At the beginning of the previous decade, physical scaling (the gate oxide thickness limit) came to a halt, and the advent of new transistor by reducing the horizontal dimensions and introducing new materials and new physical effects continues the Dennard's law. The new era is name equivalent scaling. And the vertical structures begin replace planar transistor. The predictive revolution date is 2021. At that moment, device built via 2D scaling will reach a fundamental manufacturing 2D physics limit, the transition to complete vertical device structures, heterogeneous integration in conjunction with reduced power consumption become the technology drivers.[2], [3]

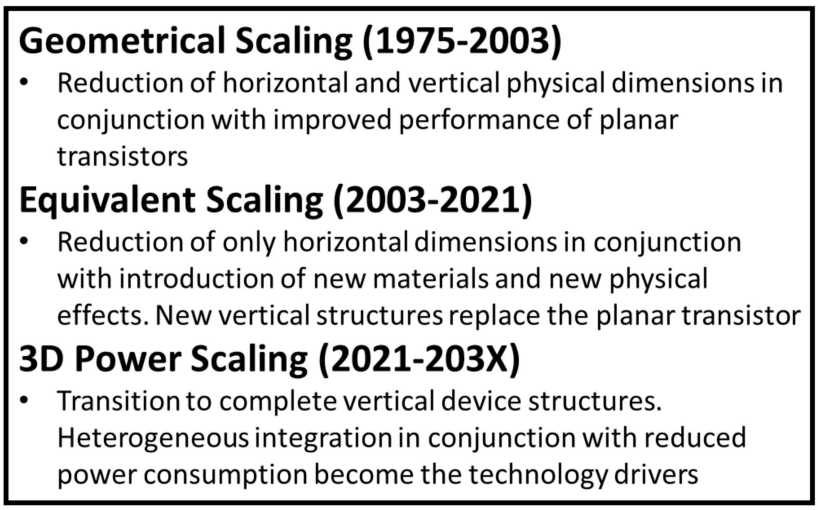


Figure 6 The different ages of scaling

The IRDS projects also five steps of functional transition from 2D to 3D VLSI: (here include the functional heterogeneous devices as sensors, new storage devices, alternative logic and memory devices or circuits)

- Two stacked layers with large scale components such as analog, I/O, and power management, MEMS in one layer and high-performance logic and memory in the other.
- Monolithic integration of two layers, where each layer contains one of the two fundamental transistor types in logic, NMOS and PMOS (n-channel and p-channel MOS), stacked on top of each other in order to increase logic density.
- Two layers: logic and memory.

- Analog, I/O, and RF connectivity as an extra layer, giving more freedom to include special devices in the design.
- 3D VLSI with fine-pitch logic-on-logic as well as special functional layers exploiting new architectures

1.3) Development of 3D IC

Today, memory producers, they are facing similar problems because they have no space in 2D, and the cost of producing memory circuits of small dimensions keeps rising while the number of stored electrons in the floating gate keeps decreasing. To solve these problems, memory producers have already worked out and announced several new architectures that stack multiple layers of memory on top of each other in a single IC. As many as 48 and 96 layers of flash memory have been reported. Table 2 shows the prediction of flash memory devices for more than 100 layers. So heat removal and reduction of power will be the two main issues in the 3D power scaling.

Table 2 Flash memory trends (source: www.itrs2.net)

NAND flash Year of production	2015	2016	2020	2022	2024	2028	2030
2D NAND flash uncontacted poly ½ pitch-F (nm)	15	14	12	12	12	12	12
3D NAND minimum array ½ pitch-F (nm)	80nm	80nm	80nm	80nm	80nm	80nm	80nm
Number of word lines in one 3D NAND string	32	32-48	64-96	96-128	128-192	256-384	384-512
Domain cell type (FG, CT, 3D, etc.)	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D
Product highest density (2D or 3D)	256G	384G	768G	1T	1.5T	3T	4T
3D NAND number of memory layers	32	32-48	64-96	96-128	128-192	256-384	384-512
Maximum number of bits per cell for 2D NAND	3	3	3	3	3	3	3
Maximum number of bits per cell for 3D NAND	3	3	3	3	3	3	3

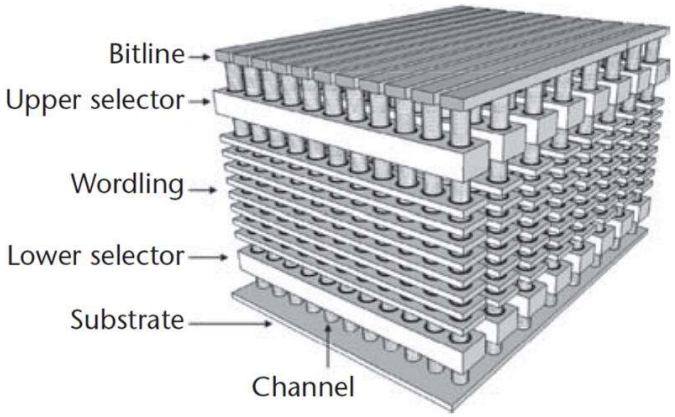


Figure 7 Example 3D architecture of future monolithic integrated circuits[3]

Beyond 2020, the future ICs architecture will change to a type of structure similar to the one in Figure 7. This new method of scaling, which is capable of stacking multi-layers in a 3D devices level, can substantially accelerate Moore's law. Research on new switches began in 2005. By 2010, the tunnel FET (TFET) seems a potential replacer of MOS as shown in the figure 8, because of its lower operating power. [8] Negative capacitance FET (NC FET) has also shown as another lower operating power devise than MOS. [9], [10] CNTs (Carbon nanotube) have become the most viable switch later in the next decade, because of its energy saving and performance improvement. [11] The number of transistors that can be integrated on a cm^2 of silicon will continue to increase at Moore's law pace for the next 10 or more years by means of 3D integration. Till now, transistor speed has continued to increase during this decade, and the operation frequency of transistor has already arrived at 100 GHz if power dissipation wasn't a bottleneck, but because of the power dissipation limits of ICs, today's MPU's operating frequency has been limited to a few GHz (CPU intel Core i9 4.2 GHz). So in the next decade, the goal of IC design has shifted from high frequency design to low power and better heat dissipation design.

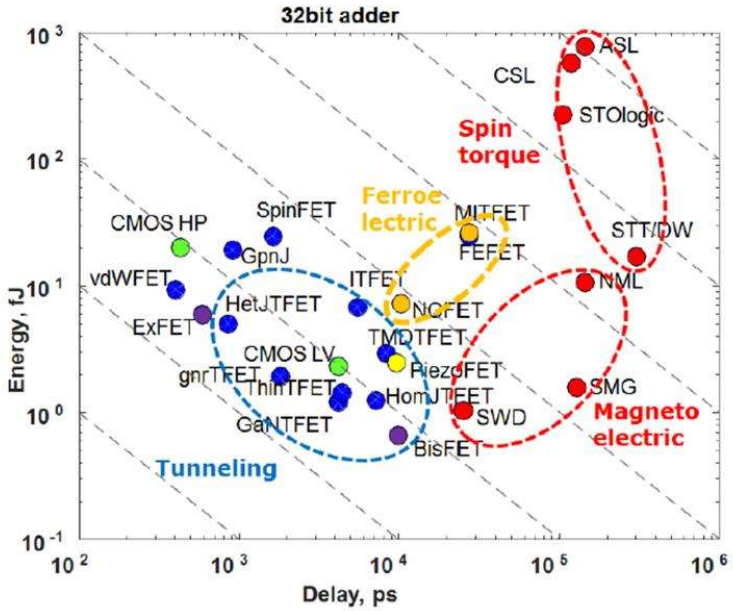


Figure 8 Switching energy vs. delay of a 32-bit adder[12]

Three Dimensional (3D) Integration and Packaging has been successful in mainstream devices to increase logic density and to reduce data movement distances. It solves the fundamental limits of scaling e.g. increasing delay in interconnections [13], development costs and variability [14]. Most memory devices shipped today have some form of chip-stacking involved. 3D integration have different technologies, with the development, they are wire bonding and flip chip for SiP (Silicon in Package), through silicon via (TSV) in bulk, TSV in SOI (Silicon on insulator), 3D parallel, 3D sequential (MIV monolithic inter via).

In the bulk level design (>2um), there have two stacked dies types, the interconnection via substrate, and direct connection between dice. The typical interconnection via substrate technology is wire-bonding stack. The wire bonding stack, as shown in the Figure 10(a), has a low density, low bandwidth, high latency and high power dissipation characteristic (the exact numbers can be found in the previous table 1). And TSV in bulk is the typical one of the direct connection between dice, which is the main stream of 3D interconnection because that they don't need substantial change to the existing fabrication flow, as shown in the Figure 10(b). The size in CMOS image sensors using "via last" approach has a diameter of about 50um. [15]–[19]. And it has smaller size for 3D stacked memory (NAND, DRAM …) and logic circuits (MPUs with cache memory). Stacking involves drilling holes through silicon chips to provide electrical connections between layers of stacked silicon chips. Chip stacks up to 40 layers deep are available that have lower engineering costs than adding layers lithographically or epitaxial deposition. TSV offers lower bandwidth and less efficient connectivity between chip layers than adding layers with photolithography processes, but far higher bandwidth and efficiency than using conventional chip packaging. It has an advantage of 10X more links in the circuit and better bandwidth, better latency, lower power supply[16], [20]–[22]. However, the keep-out zone (KOZ) [23]–[28] required for through-silicon via (TSVs) and limitations on the die alignment precision generate limits on the device integration density that can be designed using TSV-based 3D stacking [2], [26].

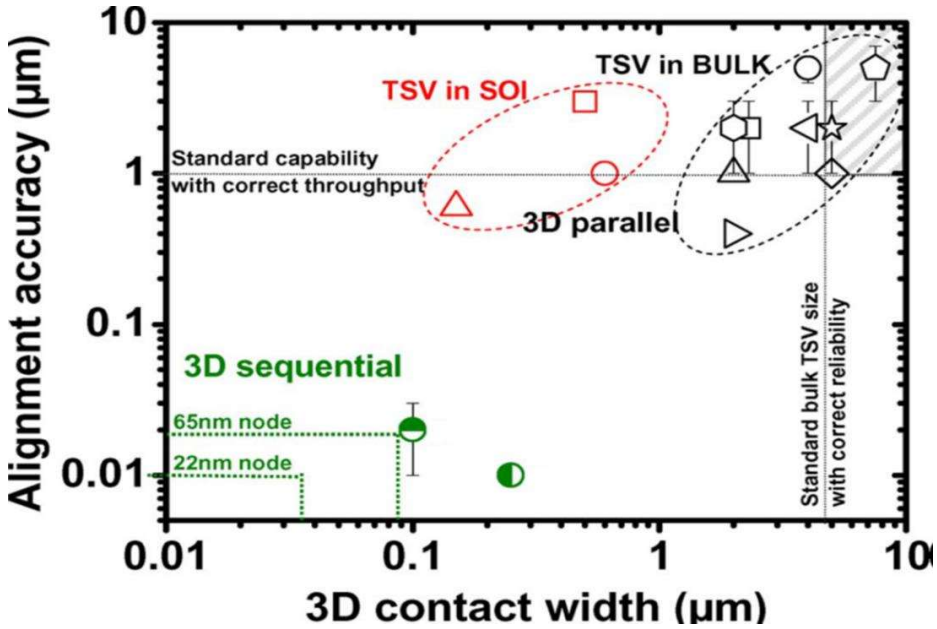


Figure 9 Alignment capability versus 3D contact width in parallel and sequential integration schemes[29]

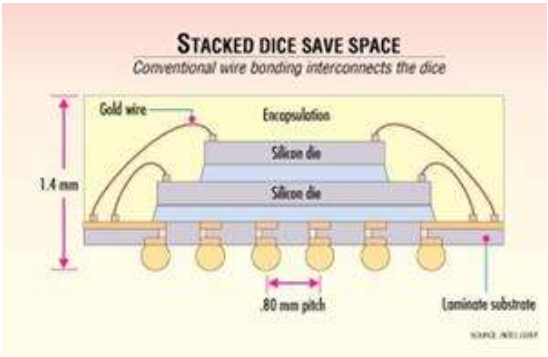
Below 1um, in this field, the 3D technology's interest stays at the transistor scale design. As observed in the Figure 9, which shows the alignment accuracy between the stacked transistor layers with regards to the 3D contact width (pitch), the 3D parallel integration [30], [31] as shown in the Figure 10(c), enables the continuously reduction after 3D TSV, the pitch reduction has been reduced to 1um. But even though some 3D SOI (silicon on insulator) architectures can reduce the

3D contact size, the 3D contact pitch remains however limited by the alignment performance, which is limited to about 1um, to guarantee a correct throughput.

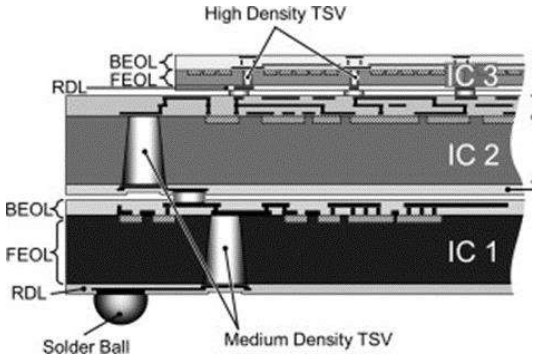
3D sequential integration is the next generation of 3D integration technologies, it's also named Monolithic 3D (M3D)[1]–[4], [7], [13], [15], [25], [27], [29], [32]–[60]. It has been demonstrated that 3D interconnections and planar contact pitches are matching even for advanced nodes [30] and it has the potential to achieve nano-scale device integration compared to TSV-based 3D stacking [60], and for the 3D parallel integration, one via has a connection of a few thousand transistors blocks [31], as shown in the table 3. That's too coarse-grained compared with monolithic inter-tier vias (MIVs)[29]. So that's why the 3D sequential integration is the only possibility to fully exploit the potential of the third dimension, especially at the transistor scale. There are three categories of M3D integration depending on the pitch of tier partitioning; transistor-level, gate-level and block-level M3D integration. In transistor-level M3D, P-channel transistors are placed on one tier and N-channel transistors on another tier, and connection between them is established by MIVs. In gate-level M3D, standard cells are split across multiple tiers, and inter-cell connections which cross tiers utilize MIVs. Block-level M3D design, which is the coarsest-grained design style, partitions functional blocks, and inter-block MIVs are deployed to deliver signals between functional modules in different tiers. Unfortunately, nowadays the commercial EDA tools to support 3D integration are temporally not available. So, various studies have been reported on M3D IC design using 3D commercial tools. M3D has also the disadvantage of device and interconnect performance mismatch between tiers, testing challenges, cost, etc.

Table 3 Ratio between 3D via and planar contact pitch in sequential and parallel case[29][30][42]

	Parallel		Sequential
Pitch	0.5um	1um	10nm
$D_{via3D}/D_{CONT,45nm}$	1/1000	1/10000	1/1



(a)



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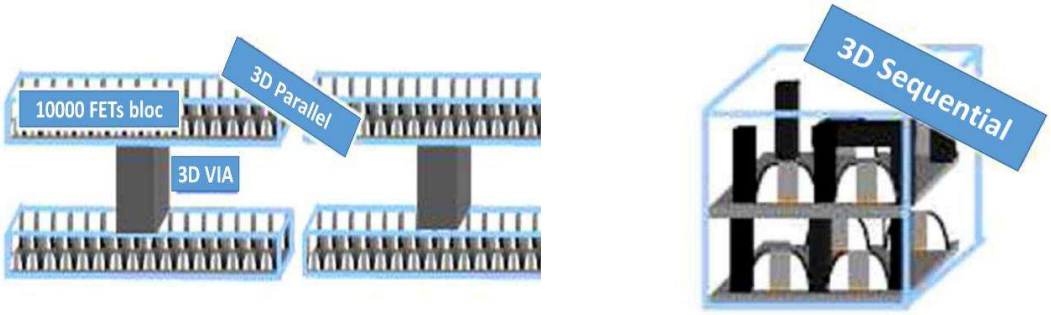


(c) (d)

Figure 10 Different 3D interconnection technologies (a) Wire-bonding (b) Through silicon via (high density TSV & Medium density TSV) (c) 3D parallel integration (d) 3D Sequential integration

Implementation of a 3D structure including CNFETs, resistive RAM (RRAM), and spin-transfer torque magnetic RAM (STT-MRAM) has already been proposed and analyzed by using N3XT (Nano-Engineered Computing Systems Technology) proposed by University of Stanford and University of California Berkeley.[61] The structure is shown in the Figure 11. The N3XT model has been demonstrated to have a 23X speedup and 37X energy reduction, that's to say, it will have a total energy-delay product benefit of 851.[61]

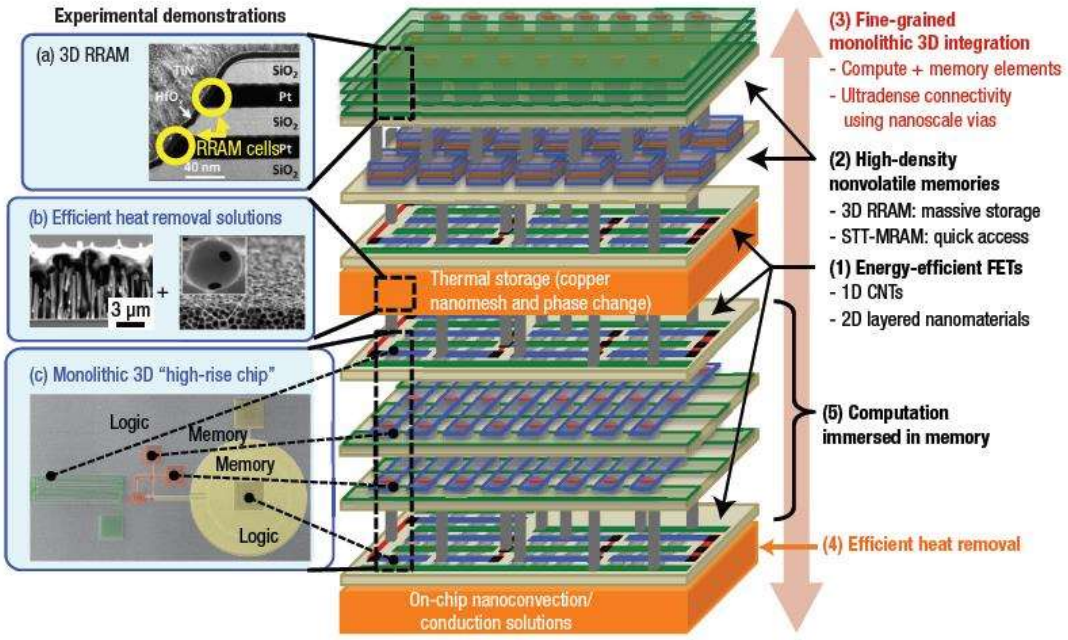


Figure 11 monolithically integrated 3D system enabled by Nano-Engineered Computing Systems Technology (N3XT). On the right are the five key N3XT components. On the left are images of experimental technology demonstrations: (a) transmission electron microscopy (TEM) of a 3D resistive RAM (RRAM) for massive storage, (b) scanning electron microscopy (SEM) of nanostructured materials for efficient heat removal (left: microscale capillary advection; right: copper nano-mesh with phase-change thermal storage), and (c) SEM of a monolithic 3D chip for high-performance and energy-efficient computation. CNTs: carbon nanotubes, FETs: field-effect transistors, and STT-MRAM: spin-transfer torque magnetic RAM.[61]

1.4) Background and outline

This new architecture shows that computing performance can still be improved in the next decade, and the main power will rely on 3D heterogeneous integration. So the future of semiconductor industry is quite bright, and future discoveries will continue to bring progress and bring new breakthrough.

This thesis is embedded in a very vast project, driven by ST Microelectronics crolles and CEA LETI in Grenoble, and in cooperation with 3IT (Interdisciplinary Institute for Technological Innovation) and University of Sherbrooke. This project has the goal to design and produce a 3D CMOS image sensor [62], and the design of cooling system of this equipment is very important; the heat dissipation issues in the 3D CMOS image sensor can be crippling. Another demonstrator is on the way. This demonstrator (Figure 12) applies the nuclear magnetic resonance (NMR) / magnetic resonance imaging technology in the micro/nano scale. In recent years, NMR/MRI portable devices have drawn attention of numerous researcher teams. They are used for variety of applications, especially for medical diagnosis. The 3D schematic of the micro/nano MNR chip is shown in the Figure 12. This project is driven by numerous hospitals, here include hospitals in Lyon and New York[63]. As we know, the coil receiver can be easily affected by the environmental noises; moreover, its self-noise is expressed as 4kRT; R is for instance, the resistance of the coil. So, reducing the coil self-noise means to reduce this resistance. And, in the same time, the quality factor Q of the coil, defined as $Q = \omega L/R$, will be increased. The SNR (signal noise ratio) in the coil design can be a crippling evaluator during the miniaturization of MNR/MRI.

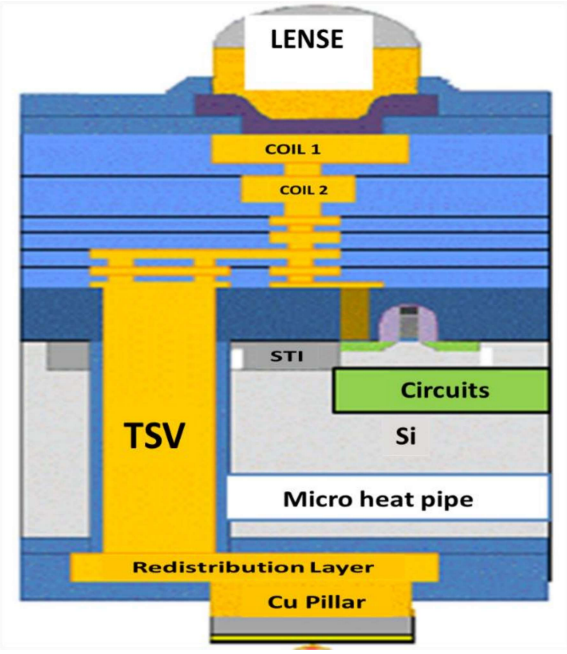


Figure 12 Connectivity relationship of MNR chip (TSV, RDL: Redistribution layer and circuits embedded into the substrate)

So the purpose of the thesis is to provide a global design method for the 3D integrated circuit in electrical, thermal, electro-thermal and also noise field. Due to the high density design of 3D IC, the passive heat management method is another important work of this thesis. Hereafter will be included simulation methods for substrate and also relative connectivity (TSV, RDL, Micro strip and circuits embedded into the substrate), thermal and electro-thermal modeling method, and also keep-out of zone calculation methods.

The chapter 2 presents some background knowledge on electrical parasitic effects of TSVs. Based on the parasitic effects, we programmed and generated in Matlab a substrate impedance extractor and a 3D TLE (3D transmission line extractor), which can automatically extract the impedance from any contacts with arbitrary shape and arbitrary material. The extractors are 100% compatible with SPICE core simulator, like ADS (Advanced design system) and can be used in the S parameters extraction and transient study in ADS. The extracted data is verified with measurement results and finite element method (FEM) simulation results. Based on the parasitic effects of TSV, a 26 GHz frequency and 2 GHz bandwidth RF filter is proposed in this work.

The chapter 3 presents the thermal and electro-thermal modeling method. So the chapter 3 implements an analytical solution for multi-layers substrate nonstationary temperature distribution. In the 3D circuits, the thermal issues are crippling issues in the 3D IC design, especially when we scale down to nanoscale. The electrical resistance increase with temperature, likewise the substrate resistance. Most of thermal simulation works are based on the steady regimes; few people work on the non-stationary case. Non-stationary effects are crippling, like hot spots, which can be enhanced by voltage ramps. We propose also a multi-layers 3D IC's 3D heat dissipation calculation method. This method is suitable for any 3D IC. A 4 core CPU heat dissipation case is studied in this chapter. The later part of this chapter presents how the electro-thermal simulation works. The electro-thermal simulator can be 100% compatible with SPICE (-like) simulator, and the electrical part is verified with ADS. This work constructs the framework of 3D IC electro-thermal analysis.

The chapter 4 presents the passive thermal dissipation method. As a solution to the local heat dissipation, the passive heat dissipation component, flat heat pipe (FHP) is proposed as a prospective component in the chapter 4. This chapter presents the FEM simulation approach of the FHP, and also the analytical modeling. The two results have good match, and an extensive study of the working performance's limiting condition has also been presented in this thesis.

The chapter 5 presents the noise issues of 3D IC. We firstly propose the analytical solution for the substrates noise distribution and present noise analysis methods. And this chapter investigates also the keep-out-of-zone (KOZ) of TSV to transistor. The investigation methods of electrical noise impact and thermal-mechanical noise impact are shown in this part.

Finally, the chapter 6 summarizes the contributions of these dissertation works, drawing conclusions of the manuscript.

Chapter 2: Electrical modeling of TSV

Integrating multiple functional layer in a single device is a major trend in the electronics field. Therefore, requiring a higher integration degree of equipment becomes more important today. 3D-IC technology based on vertical through silicon via (TSV), has been proposed as a prospective solution to the current 3D interconnection problem. Reduction of parasitic effects, higher interconnection density, faster inter-chip communication speed and less energy consumption are the main advantages of TSV interconnection [64]. In this way, the 3D-TSV technology is considered to be the main design object of 3D highly integrated technology. In the next few years, TSV structure can flourish in the field of chips. In addition, more chips will be integrated in the 3D-IC to meet the requirements for higher bandwidth, more I / O interfaces and smaller sizes. The multi-layer TSV will be the only technology to realize this structure [65]. Therefore, there is an urgent need for multi-layer TSV electrical characteristics and coupling problems in some researches.

For 3D stacked DRAM modules, some signals can be exchanged with other different chip signals (assuming the same layout of the chip), including the read control, address bus, data bus, write control, power supply [66]. Some structures have been completed by experimental tests [67]. Although the manufacturing process gets more attention, it should also emphasize more simulation analysis. Many research work has been completed, mainly focused on the study of different electrical characteristics of TSV and calculation of TSV electrical parasitic parameters formula [68]–[71]. However, the pre-layout study of electromagnetic modeling and analysis of TSV in multilayer substrates is critical before it enters production. The crosstalk becomes a key problem in reducing the TSV performance due to the fact that the silicon substrate with conductive properties, has parasitic capacitance effects on the insulating oxide (SiO2, isolation material surrounded by the TSV) and the isolation layer formed by the TSV metallization, especially in the TSV array. Many studies have focused on TSV crosstalk problems.

2.1) Single TSV analytical approach

2.1.1)Cylindrical TSV parasitic parameters

Cylindrical TSV is the most common TSV structure, as shown below. We can use copper, tungsten, polycrystalline silicon and so on, as the filling material, which depends on the adequate resistivity we need. Due to the simple structure, it's the easiest one to be simulated, so the research to this model has outdistanced the other TSV structures. And the thermal-mechanical and high-frequency characteristics are the main two emerging problems of TSV [72], [73]. And in following part, we will precisely introduce cylindrical TSV.

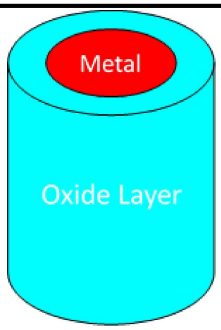


Figure 13 Cylindrical TSV

2.1.1.1) Cylindrical TSV Resistance:

In low frequency, cylindrical TSV resistance can be calculated by using the traditional wire resistance equation. When the current pass through the wire, the wire's resistance is inverse proportional to the cross-sectional area (A), and proportional to the wire's length, the resistance can be expressed by the following equation[46], [53], [62], [74]–[82]

$$R = \frac{\rho l}{A} \tag{2-1}$$

And ρ is the resistivity of the wire, l is the wire's length, A is the wire's cross section area. In the integrated circuit, we use normally the copper and aluminum as the interconnection material. In 3D IC design, interconnection delay has been the major influence factor of the circuit performance, so we usually use the copper (resistivity $1.68 \times 10^{-8}\Omega \cdot m$) instead of the aluminum (resistivity $2.83 \times 10^{-8}\Omega \cdot m$) to reduce the interconnection delay of via. For TSV radius r_{TSV}, cross sectional area πr_{TSV}^2's cylindrical TSV, it's resistance can be expressed as [44]

$$R_{TSV\_DC} = \frac{\rho l_{TSV}}{\pi r_{TSV}^2} \tag{2-2}$$

With the augmentation of the signal's frequency, the skin effects should be taken into consideration, that's to say, with the increase of the signal frequency in the metal, the current that passes through the via will tend to the conductor's surface. The skin effect will increase the effective resistance of the conductor and the skin effect will be more obvious as the frequency gets higher. And here we should introduce skin depth δ. It means that when the current density in the conductor gets down to the $\frac{1}{e}$ (e: Euler's number) times of the conductor's surface current density, the expression equation is [20]

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_m}} \tag{2-3}$$

Here, f is signal's frequency of the wire, μ_0 is the free space permeability (the value is $4\pi \times 10^{-7}\mathrm{H}/m$), μ_m is the metal's permeability. And through this equation, we can deduce the corner frequency if the skin effect, [20]

$$f_\delta = \frac{\rho}{\pi\mu_0\mu_m r_{TSV}^2} \quad (2\text{-}4)$$

So when the frequency f is smaller than the f_δ, the skin depth δ will be bigger than the TSV radius r_{TSV} of metal part, and at this case, the skin effect is negligible. So the resistance of TSV can be defined as a DC resistance, which can be expressed as shown in the $R_{TSV\_DC} = \frac{\rho l_{TSV}}{\pi r_{TSV}^2}$ (2-2); when the frequency f is bigger than the f_δ, the skin depth δ will be smaller than the TSV radius r_{TSV}, and at this case, the AC resistance introduced by the skin effect can be shown as following [83]

$$R_{TSV\_AC} = \frac{\rho l_{TSV}}{\pi[r_{TSV}^2 - (r_{TSV}-\delta)^2]} \quad (2\text{-}5)$$

As we can see here, the TSV parasitic resistance is composed of a DC resistance and a AC resistance, and can be expressed as following [83]

$$R_{TSV} = \sqrt{R_{TSV\_DC}^2 + R_{TSV\_AC}^2} \quad (2\text{-}6)$$

For a TSV with $60\mu m$ diameter and $100nm$ oxide layer thickness, the corner frequency can be 4.7 MHz, and for a TSV with $5\mu m$ diameter and $100nm$ oxide layer thickness, the corner frequency can be 681 MHz. So here means, if we don't want to see the skin effect, either use a conductive material with a higher conductivity or reduce the via's diameter.

2.1.1.2) Cylindrical TSV Capacitance:

The capacitance of TSV is defined as the capacitance between the metal conductor and silicon substrate, because the TSV insulation layer's thickness is usually less than 1μm, so this parasitic capacitance has a great influence to the transmission, in the study of 3D IC signal integrity and power dissipation, TSV's capacitance need more accurate simulation and analysis. Because of the insulation layer (SiO_2), which is used to insulate the TSV signal and the outside silicon substrate, the TSV structure forms a metal-oxide-semiconductor structure, which is MOS structure. We can get the analytical solution by solving the 1D poison equation in the cylindrical coordinate system. The TSV equivalent capacitance is composed of two parts, they are respectively oxide capacitance C_{ox} and capacitance of depletion C_{dep}.

C_{ox} is expressed as [84]

$$C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_{ox} l_{TSV}}{\ln(\frac{d_{TSV}+2t_{ox}}{d_{TSV}})} \quad (2\text{-}7)$$

Here, t_{ox} is the thickness of the oxide layer, ε_{ox} is the dielectric constant of SiO_2 (the value is 3.9), ε_0 is the free space absolute dielectric constant (the value is $8.854 \times 10^{-12}\mathrm{F}/m$)

The depletion capacitance is noted as C_{dep} which is shown as [84]

$$C_{dep} = \frac{2\pi\varepsilon_0\varepsilon_{ox}l_{TSV}}{\ln(\frac{d_{TSV}+2t_{ox}+W_{dep}}{d_{TSV}+2t_{ox}})} \quad (2\text{-}8)$$

And the depletion width W_{dep} can be calculated by the following relationship. [85]

$$W_{dep} = \sqrt{\frac{4\varepsilon_0\varepsilon_{si}V_{th}\ln(\frac{N_A}{n_i})}{qN_A}} \quad (2\text{-}9)$$

Here, N_A is the doping density, n_i is the intrinsic silicon carrier concentration (the value is $1.5 \times 10^{16}m^{-3}$), V_{th} is the thermal voltage, which can be expressed by the following equation [85]

$$V_{th} = \frac{kT}{q} \quad (2\text{-}10)$$

When T=300K, V_{th}'s value is 25.9mV, the k is the Boltzmann constant (the value is $1.38 \times 10^{-23}J/K$), q is the unit electron charge constant (the value is $1.6 \times 10^{-19}C$).

When the metal voltage and silicon substrate voltage are different, there will be MOS effect. In the analysis of the MOS effect, we should define the bias voltage, threshold voltage and flat band voltage. When the TSV is working, the voltage applied in the metal is called bias voltage of TSV (V_B); the threshold voltage (V_{TH}) is the voltage applied in the metal when the voltage in the Si/SiO_2 interface equals to $2\ln(N_A/n_i)$; And the flat band voltage (V_{FB}) is the voltage applied in the metal when the Si/SiO_2 turns to the flat band state, and the V_{FB} can be expressed in the following expression [85]

$$V_{FB} = \Phi_m - \Phi_{si} - \frac{r_{ox}qQ_f}{\varepsilon_{ox}\varepsilon_0}\ln(\frac{d_{ox}}{d_{TSV}}) \quad (2\text{-}11)$$

Here, Φ_m is the work function of TSV's metal conductor, Φ_{si} is the work function of the outside silicon substrate, Q_f is the surface charge of the Si/SiO_2 interface.

If the silicon substrate is P type substrate, when the metal's voltage is different from the silicon substrate, a lot of cavities will leave Si/SiO_2 interface, and then the carrier depletion appears. The following Figure 14 is the MOS structure, r_{dep} is the depletion radius, r_{ox} is the oxide radius, r_{TSV} is the metal's radius.

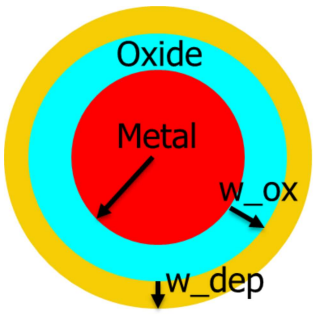


Figure 14 Cylindrical TSV top view (with depletion layer)

When $V_B < V_{FB}$, there will be depletion layer, and at this case, r_{dep} equals to the r_{ox}. And this area is named accumulation region, and the equivalent capacitance is C_{ox}.The expression is the same like (2-7).

$$C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_{ox}l_{TSV}}{\ln(\frac{d_{TSV}+2t_{ox}}{d_{TSV}})} \quad (2\text{-}12)$$

When $V_{FB} \le V_B < V_{Th}$, the depletion layer appears, with the increase of V_B, the W_{dep} increases, but C_{dep} decreases (see equation (2-8) and (2-9)). And this area is named depletion region, and the total capacitance is defined as following [85]

$$C_{dep} = \frac{2\pi\varepsilon_0\varepsilon_{si}l_{TSV}}{\ln(\frac{d_{TSV}+2t_{ox}+2W_{dep}}{d_{TSV}+2t_{ox}})} \quad (2\text{-}13)$$

$$W_{dep} = \sqrt{\frac{4\varepsilon_{si}V_B\ln(\frac{N_A}{n_i})}{qN_A}} \quad (2\text{-}14)$$

$$C_{TSV} = (\frac{1}{C_{ox}} + \frac{1}{C_{dep}})^{-1} = \frac{C_{ox}C_{dep}}{C_{ox}+C_{dep}} \quad (2\text{-}15)$$

When $V_B \ge V_{Th}$, the depletion width W_{dep} gets to its maximum, and it will not continue to increase with V_B, and this area is named inversion region, and at this moment, C_{dep} gets to its minimum, so the same as the C_{TSV}. [85]

$$C_{dep} = \frac{2\pi\varepsilon_0\varepsilon_{si}l_{TSV}}{\ln(\frac{d_{TSV}+2t_{ox}+2W_{dep}}{d_{TSV}+2t_{ox}})} \quad (2\text{-}16)$$

$$W_{dep} = \sqrt{\frac{4\varepsilon_{si}V_{th}\ln(\frac{N_A}{n_i})}{qN_A}} = \sqrt{\frac{4\varepsilon_{si}kT\ln(\frac{N_A}{n_i})}{q^2N_A}} \quad (2\text{-}17)$$

$$C_{TSVmin} = (\frac{1}{C_{ox}} + \frac{1}{C_{depmin}})^{-1} = \frac{C_{ox}C_{depmin}}{C_{ox}+C_{depmin}} \quad (2\text{-}18)$$

$$V_{Th} = V_{FB} + 2V_T\ln\left(\frac{N_a}{n_i}\right) + \frac{qN_a\pi(\left(\frac{d_{tsv}}{2}+t_{ox}+W_{dep}\right)^2-(\frac{d_{tsv}}{2}+t_{ox})^2)sin\alpha}{2\pi\varepsilon_{ox}}\ln(\frac{d_{tsv}+2t_{ox}+l_{tsv}cot\alpha}{d_{tsv}+l_{tsv}cot\alpha}) \quad (2\text{-}19)$$

Based on the TSV RC parasitic parameters' extraction model, the paper [86] gives a TSV RC parameters' extraction and Q3D simulation result in the 45nm CMOS background, as shown in the table below. The comparison shows that the average error between these parasitic parameters and Q3D simulation is about 5%, and the formulas can be used in TSV parasitic extractions.

Table 4 Different aspect ratio TSV RC parasitic parameters extraction comparison result in 45nm CMOS process from [86]

Aspect ratio	1	3	5
Diameter d/um	5		
Tox /nm	120		
NA /cm3	2E15		
Theorical resistance/mOhm	0.30	2.80	1.40
Q3D Resistance/mOhm	0.35	3.03	1.75

Resistance error/%	1.15	1.77	1.61
Theorical capacitor/fF	0.14	7.43	5.71
Q3D capacitor/fF	0.38	8.28	7.21
Capacitor error/%	2.56	3.10	3.28

2.1.1.3) Cylindrical TSV Inductance

The TSV's inductance is composed of self-inductance and mutual-inductance, here we use some simplifications, and assume that the current back path is in the infinite, so the inductance of TSV is, (d_{TSV} is the TSV's metal diameter), this formulae comes from publication [87] by taking taper angle to 0.

$$L_{TSV} = L_{inner} + L_{ext} = \frac{\mu_0\mu_m l_{TSV}}{8\pi} + \frac{\mu_0\mu_m}{2\pi} l_{TSV} \left[\ln\left(\frac{2l_{TSV}+\sqrt{d_{TSV}^2+4l_{TSV}^2}}{d_{TSV}}\right) + (d_{TSV} - \sqrt{d_{TSV}^2+4l_{TSV}^2})\right] \quad (2\text{-}20)$$

Normally the inner inductance is far smaller than the exterior inductance, so the inductance of TSV can be expressed as [87]

$$L_{TSV} = \frac{\mu_0\mu_m}{2\pi} l_{TSV}\left[\ln\left(\frac{2l_{TSV}+\sqrt{d_{TSV}^2+4l_{TSV}^2}}{d_{TSV}}\right) + (d_{TSV} - \sqrt{d_{TSV}^2+4l_{TSV}^2})\right] \quad (2\text{-}21)$$

Table 5 Different size TSV inductance

TSV diameter	TSV height	TSV oxide thickness	Ltsv
2um	20um	0.05um	13.827pH
2um	20um	0.1um	14.049pH
5um	20um	0.05um	10.185pH
5um	20um	0.1um	10.262pH
5um	50um	0.05um	34.262pH

2.1.1.4) Interconnection delay

Due to the longer and longer interconnection delay, it will decide the limit between system clock frequency and interconnection transmission. In order to reduce the interconnection RC delay, paper [86] propose a buffer inserted design.

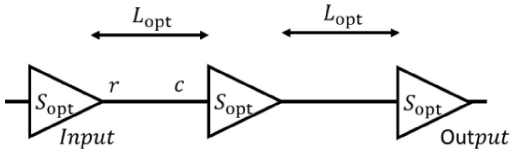


Figure 15 Interconnection model after inserting buffer

Figure 15 shows the interconnection model after inserting buffer, in the Figure 15, r and c are respectively the interconnection resistance and capacitance per unit length. The equivalent buffer resistance can be expressed as R_d/s_{opt}, and equivalent capacitance can be expressed as $C_0 * s_{opt}$, s_{opt} and L_{opt} are the buffer's best size and distance, R_d and C_0 are respectively the buffer's output resistance and input capacitance. And the longest interconnection delay D_{rep} can be expressed as following [88]

$$D_{rep} = 2.37 L_{longest} \sqrt{R_d C_0 rc} \tag{2-22}$$

And $L_{longest}$ is the overall longest interconnection line, and it can be expressed by the Davis random distribution model. [88]

$$L_{longest} = 2\left(\sqrt{\frac{N_t}{S}} - 1\right) + m(S-1) \tag{2-23}$$

N_t is the chip's total logic gate number, S is the silicon source layers number, m is the ratio between layer distance and gate distance. If $N_t \gg m$, $L_{longest} \propto \frac{1}{\sqrt{S}}$, so by reducing the silicon source layers number, it can reduce the time delay. But with the increase of the integration density, TSV RC delay becomes necessary. TSV's equivalent lumped II style RC model can be written as: [88]

$$D_{3D} = D_{rep} + N_{TSV} * D_{TSV} \tag{2-24}$$

And here N_{TSV} is the chip's TSV numbers along the interconnection line. And the buffer's TSV intrinsic delay is [88]

$$D_{TSV} = \frac{R_d}{s_{opt}} \cdot \frac{C_{TSV}}{2} + \left(\frac{R_d}{s_{opt}} + R_{TSV}\right) \times \left(\frac{C_{TSV}}{2} + s_{opt} C_0\right) \tag{2-25}$$

2.1.1.5) Power dissipation during interconnection

In the 3D system, the power dissipation is composed with the following parts. [89], [90]

$$P_{total} = P_{int} + P_{logic} + P_{rep} + P_{TSV} \tag{2-26}$$

Here P_{int} is the interconnection line dissipation, P_{logic} is the logic gate dissipation, P_{rep} is the inserted buffer dissipation, P_{TSV} is the TSV dissipation.

$$P_{int} = \frac{\alpha}{2} C_{int} L_{tot} V_{dd}^2 f \tag{2-27}$$

Here, V_{dd} is the supply voltage, α is the average gate active factor, f is the working frequency, C_{int} is the interconnection capacitance per unit length, L_{tot} is the total length of interconnection line, it's supposed to follow the random distribution model. [89], [90]

$$L_{tot} = \int_1^{2\sqrt{N_t}} l \cdot i(l) dl \quad (2\text{-}28)$$

$i(l)$ is the interconnection density function.

Logic gate and inserted buffer have the same dissipation model, they can be expressed as [89], [90]

$$P_{logic} = N_t \frac{\alpha}{2} C_{logic} V_{dd}^2 f \quad (2\text{-}29)$$

$$P_{rep} = n_{rep} \frac{\alpha}{2} C_{rep} V_{dd}^2 f \quad (2\text{-}30)$$

C_{logic} and C_{rep} are respectively the gate and buffer's equivalent capacitance, n_{rep} is the inserted buffer's number and N_t is the chip's total logic gate number.

And the TSV's RC model depends on the via's number. [89], [90]

$$P_{TSV} = N_{TSV} \frac{\alpha}{2} C_{TSV} V_{dd}^2 f \quad (2\text{-}31)$$

2.1.2)Taper TSV parasitic parameters

Taper TSV is proposed by MIT's Lincoln's laboratory[47], its structure is shown as Figure 16. Taper TSV is an inevitable manufacturing byproduct, due to the non-ideal Dry Reactive Ion Etching[91]. Paper[92] proposed a precisely controlled taper TSV fabrication process. But in compare with the cylindrical TSV, taper TSV has a higher parasitic resistance. And if it has a very high inclination, it's easy to generate a 'V' form TSV (which will be an error).[88]–[101]

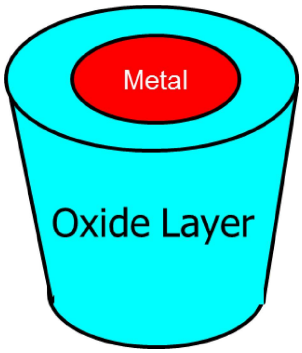


Figure 16 Taper TSV

2.1.2.1) Taper TSV Resistance:

Taper TSV resistance is also composed with a DC part and AC part[87].

$$R_{TSV\_DC} = \frac{\rho l_{TSV}}{\pi a(a+l_{TSV}\beta)}[1+\frac{1}{2}\beta^2] \quad (2\text{-}32)$$

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_m}} \quad (2\text{-}33)$$

$$f_\delta = \frac{\rho}{\pi \mu_0 \mu_m r_{TSV}^2} \quad (2\text{-}34)$$

$$R_{TSV\_AC} = \frac{\rho(2+\beta^2)}{4\pi\beta\delta}\log(1+\frac{2\beta l_{TSV}}{2a-\delta}) \quad (2\text{-}35)$$

$$R_{TSV} = \sqrt{R_{TSV\_DC}^2 + R_{TSV\_AC}^2} \quad (2\text{-}36)$$

Where $\beta = (b-a)/l_{TSV}$, b and a are respectively top surface and bottom surface radius. When $\beta = 0$, the model will change to cylindrical TSV model.

2.1.2.2) Taper TSV Capacitance:

When we change from cylindrical TSV to taper TSV

Cox will change to [87]

$$C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_{ox}l_{TSV}}{\sin\alpha\ln(\frac{d_{TSV}+2t_{ox}+l_{TSV}cot\alpha}{d_{TSV}+l_{TSV}cot\alpha})} \quad (2\text{-}37)$$

When $\alpha = 90°$, taper TSV will turn to a cylindrical TSV, and the formula will change back to the cylindrical TSV formulas

The depletion capacitance $Cdep$ will change to [87]

$$C_{dep} = \frac{2\pi\varepsilon_0\varepsilon_{ox}l_{TSV}}{\sin\alpha\ln(\frac{d_{TSV}+2t_{ox}+2W_{dep}+l_{TSV}cot\alpha}{d_{TSV}+2t_{ox}+l_{TSV}cot\alpha})} \quad (2\text{-}38)$$

And the depletion width $Wdep$ can be calculated by poisson's equation, but it's too complicated.

V_{FB} is the flat band voltage, which is the voltage applied at the via when the system stay in the flat band state. It can be expressed as [87]

$$V_{FB} = \Phi_m - \Phi_{Si} = \Phi_m - \mathrm{X} - \frac{E_g}{2q} - \mathrm{V}_T\log(\frac{N_a}{ni}) \quad (2\text{-}39)$$

Where Φm is the metal's work function, for copper, $\Phi m = 4.65V$, Φ_{Si} is the silicon substrate work function, $\mathrm{X} = 4.05\mathrm{V}$ is the electronic affinity for silicon substrate, the intrinsic carrier concentration $ni = 1.18e10\ cm^{-3}$, band gap $E_g = 1.12eV$, the unit charge $q = 1.6022e^{-19}C$, in the room temperature, the thermal voltage $V_T = \frac{kT}{q} = 0.026V$, $N_a = 1.25e15cm^{-3}$ is the ionized acceptor concentration, $Q_f = 5e14 * q\ \mathrm{C}/m^2$ is the Si/SiO2 surface charge density.

And for the W_{dep}, we have the following relationship. [87]

$$V_{TSV} = \mathrm{V}_{FB} + \Psi(R_{ox}) + U_{ox} \quad (2\text{-}40)$$

$$U_{ox} = \frac{Q_m}{C_{ox}} = \frac{qN_a\pi(R_{dep}^2 - R_{ox}^2)sin\alpha}{2\pi\varepsilon_{ox}}\log(\frac{2R_{ox}+ltsvcot\alpha}{2R_m+ltsvcot\alpha}) \quad (2\text{-}41)$$

$$\Psi(R_{ox}) = \frac{qN_aR_{ox}^2}{4\varepsilon_{si}} - \frac{qN_aR_{dep}^2}{2\varepsilon_{si}}\log(R_{ox}) + \frac{qN_aR_{dep}^2}{4\varepsilon_{si}}\left[2\log\left(R_{dep}\right) - 1\right] \quad (2\text{-}42)$$

And we can get the R_{depmax} by the following relationship

$$\frac{qN_aR_{ox}^2}{4\varepsilon_{si}} - \frac{qN_aR_{depmax}^2}{2\varepsilon_{si}}\log(R_{ox}) + \frac{qN_aR_{depmax}^2}{4\varepsilon_{si}}\left[2\log\left(R_{depmax}\right) - 1\right] = 2V_T\log(\frac{N_a}{ni}) \quad (2\text{-}43)$$

And the threshold for the minimum capacitance region is

$$V_{th} = V_{FB} + 2V_T\log\left(\frac{N_a}{ni}\right) + \frac{qN_a\pi(R_{depmax}^2 - R_{ox}^2)sin\alpha}{2\pi\varepsilon_{ox}}\log(\frac{2R_{ox}+ltsvcot\alpha}{2R_m+ltsvcot\alpha}) \quad (2\text{-}44)$$

When $V_B < V_{FB}$ accumulation region, there will not be depletion layer, and at this case, r_{dep} equals to the r_{ox}. And this area is named accumulation region, and the equivalent capacitance is C_{ox}.The expression is the same like (2-37).

$$C_{TSV} = C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_{ox}l_{TSV}}{\sin\alpha\ln(\frac{d_{TSV}+2t_{ox}+l_{TSV}cot\alpha}{d_{TSV}+l_{TSV}cot\alpha})} \quad (2\text{-}45)$$

When $V_{FB} \le V_B < V_{Th}$ depletion region, the depletion layer appears, with the increase of V_B, the W_{dep} increases, but C_{dep} decreases (see equation (2-8) and (2-9)). And this area is named depletion region, and the total capacitance is defined as following

$$C_{dep} = \frac{2\pi\varepsilon_0\varepsilon_{si}l_{TSV}}{\sin\alpha\ln(\frac{d_{TSV}+2t_{ox}+2W_{dep}}{d_{TSV}+2t_{ox}})} \quad (2\text{-}46)$$

$$C_{TSV} = (\frac{1}{C_{ox}} + \frac{1}{C_{dep}})^{-1} = \frac{C_{ox}C_{dep}}{C_{ox}+C_{dep}} \quad (2\text{-}47)$$

When $V_B \ge V_{Th}$ minimum capacitance region, the depletion width W_{dep} gets to its maximum, and it will not continue to increase with V_B, and this area is named inversion region, and at this moment, C_{dep} gets to its minimum, so the same as the C_{TSV}.

$$C_{dep} = \frac{2\pi\varepsilon_0\varepsilon_{si}l_{TSV}}{\sin\alpha\ln(\frac{d_{TSV}+2t_{ox}+2W_{depmax}}{d_{TSV}+2t_{ox}})} \quad (2\text{-}48)$$

$$C_{TSVmin} = (\frac{1}{C_{ox}} + \frac{1}{C_{depmin}})^{-1} = \frac{C_{ox}C_{depmin}}{C_{ox}+C_{depmin}} \quad (2\text{-}49)$$

As we can see, the taper TSV model has some similarities with cylindrical TSV, so it can be simplified.

$$C_{ox\_C} = \sin\alpha C_{ox\_T} \quad (2\text{-}50)$$

$$C_{dep\_C} = \sin\alpha C_{dep\_T} \quad (2\text{-}51)$$

So, the cylindrical and taper TSV's parasite capacitance have the following relationship

$$C_{TSV\_C} = \sin\alpha C_{TSV\_T} \quad (2\text{-}52)$$

So if we use error to present the relative error, when $1 - \sin\alpha < error$, that's when $\alpha > arcsin(1 - error)$, the Taper TSV can use the cylindrical TSV's model. If $\text{error} = 5\%$, we can get the limit inclination is 73 degree. So that means if the inclination of the taper TSV is less than 15 degree, we can use the cylindrical TSV model.

2.1.2.3) Taper TSV Inductance

When the taper TSV's inclination is less than 15 degree, the parasitic inductance can be expressed as, [87]

$$L_{TSV} = \frac{\mu_0\mu_m l_{TSV}}{8\pi} + \frac{\mu_0\mu_m l_{TSV}}{2\pi}\left[\ln\left(\frac{l_{TSV}+\sqrt{a^2+l_{TSV}^2}}{a}\right) + \left(2a - 2\sqrt{a^2+l_{TSV}^2}\right) + \frac{4\beta l_{TSV}(l_{TSV}^2-(l_{TSV}+a)(\sqrt{a^2+l_{TSV}^2}-a))}{(\sqrt{a^2+l_{TSV}^2}-l_{TSV})(4a+\beta l_{TSV})}\right] \quad (2\text{-}53)$$

2.1.3)Single Tapper TSV analytical result

In order to verify the taper TSV model, we use a standard TSV geometry, TSV metal radius $r_{TSV} = 2.5\mu m$, height $l_{TSV} = 10\mu m$, oxide layer thickness $t_{ox} = 0.1\mu m$. And here we study the different inclination angle's influences by considering tapper TSV skin effect. As we can see from the Figure 17, from 1MHz to 10MHz, this region is constant, this is the DC region. Beyond 1GHz, the total resistance increases monotonically with frequency. The region between 10MHz and 1GHz is quite complicated. For the taper TSV, due to the different top radius and bottom radius, we can always find out 2 skin frequency (equation 2-33), they match well with the two pics in the figure 17. The left pic match always with the skin frequency of the bigger radius, and right pic match with the skin frequency of smaller radius. When the inclination angle gets close to 90 degree, the two pics approach, when it equals to 90 degree, the two pics turn to one big pic. This comes back to the skin frequency of cylindrical TSV case. But the equations (2-32) and (2-35) are not valid outside of the skin effect boundary conditions. We found a more accurate model:

$$for\ \delta > \text{b and b} > \text{a},\ R_{TSV_{DC}} = \frac{\rho l_{TSV}}{\pi ab} \quad (2\text{-}54)$$

$$for\ \delta < \text{a and b} > \text{a},\ R_{TSV_{AC}} = \frac{\rho l_{TSV}}{2\pi(b-a)\delta}\log\left(\frac{2\text{b}-\delta}{2\text{a}-\delta}\right) \quad (2\text{-}55)$$

$$for\ a < \delta < \text{b and b} > \text{a},\ R_{TSV_{DCAC}} = \frac{\rho l_{TSV}(\delta-\text{a})}{\pi a\delta(b-a)} + \frac{\rho l_{TSV}}{2\pi(\text{b}-\text{a})\delta}\log\left(\frac{2\text{b}-\delta}{\delta}\right) \quad (2\text{-}56)$$

For the straight wire: $\text{r} = \sqrt{ab}$ [107]

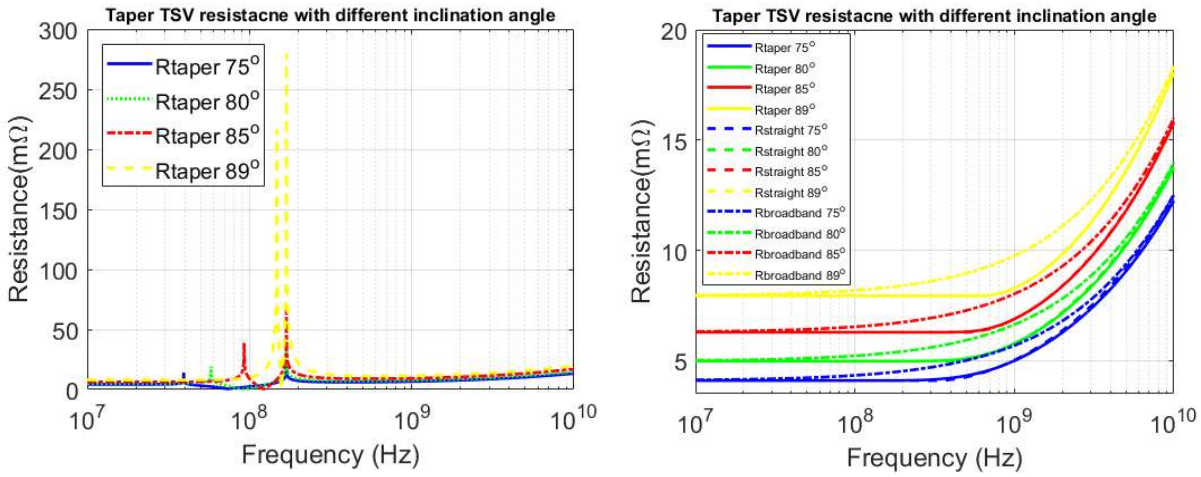
$$for\ \delta > \text{r},\ R_{TSV_{DC}} = \frac{\rho l_{TSV}}{\pi r^2} \quad (2\text{-}57)$$

$$for\ \delta < \text{r},\ R_{TSV_{AC}} = \frac{\rho l_{TSV}}{\pi(2r-\delta)\delta} \quad (2\text{-}58)$$

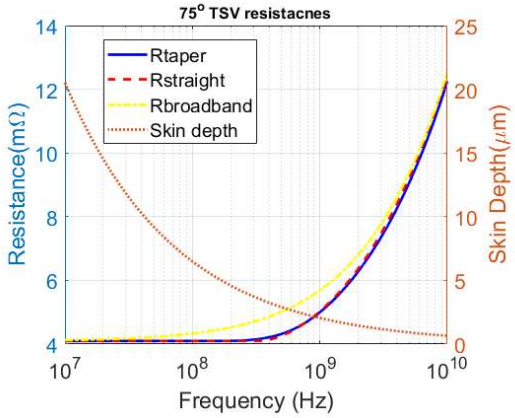
And the broadband model for cylindrical wires:

$$R_{TSV_{BB}} = \frac{\rho l_{TSV}}{\pi\delta(2r-\delta(1-e^{-r/\delta}))(1-e^{-r/\delta})} \quad (2\text{-}59)$$

We see some different results from Figure 17 (a) and (b), depending on the choice of different formula. The new formulas are more accurate. From Figure 17 (b) and (c) we can see that with the increase of inclination angle, the TSV resistances decreases. And the taper TSV models can be replaced by the straight wire model by assuming $r = \sqrt{ab}$.



(a) (b)



(c)

Figure 17 Taper TSV resistance with different inclination angle (a) original formula (b) new formula (c) 75° TSV resistances

TSV metal radius $r_{TSV} = 2.5\mu m$, height $l_{TSV} = 10\mu m$, oxide layer thickness $t_{ox} = 0.1\mu m$. And here we study the different inclination angle's influences by considering Cdep.

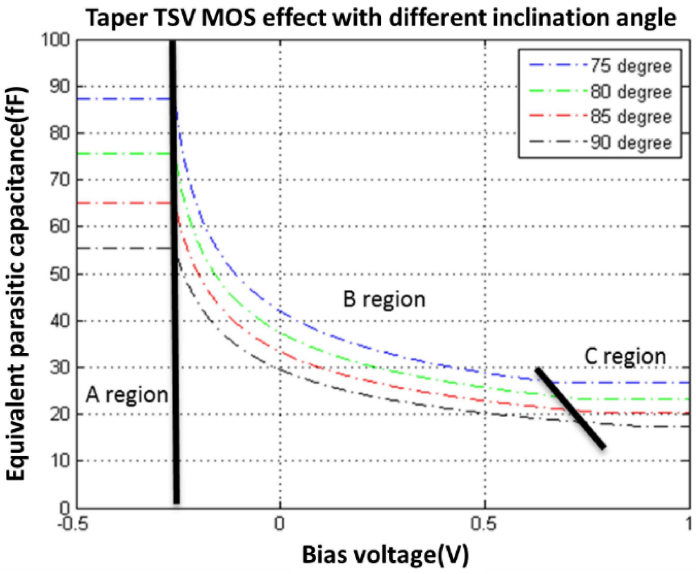


Figure 18 Taper TSV MOS effect with different inclination angle

Figure 18 shows the taper TSV's parasitic capacitance's change with the bias voltage, and different colors mean different inclination angle. When the bias voltage is less than the flat band voltage, TSV stay in the accumulation region, the parasitic capacitance is Cox (A region), with the increase of the voltage, TSV parasitic capacitance reduces due to the expansion of the depletion layer, this region is depletion region (B region). When the bias voltage arrives at the threshold voltage, the depletion width reaches the maximum and the capacitance will turn to the minimum and stay unchanged. From the Figure 18, we can see that the bigger angle the smaller capacitance, that's because that the bigger inclination angle will cause smaller capacitance contact surface. When the bias voltage is bigger than the flat band voltage, the depletion capacitance has a great influence to the TSV's final parasitic capacitance, especially when it arrives at the C region. If we neglect the influence of depletion region, it will cause big calculation error.

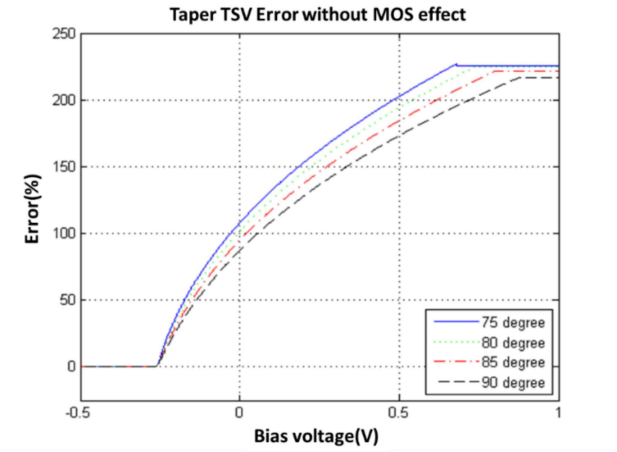


Figure 19 Taper TSV Error without MOS effect

Figure 19 gives the error when we don't take into account the MOS effect, with the increase of the bias voltage, the error increases. In the C region, all the 4 cases reach an error of more than 200%, so the depletion region's capacitance is non-negligible. Figure 20 shows that the inclination angle's influence to the TSV inductance, for a TSV of $r_{TSV} = 2.5\mu m \; and \; l_{TSV} = 10\mu m$, is almost null.

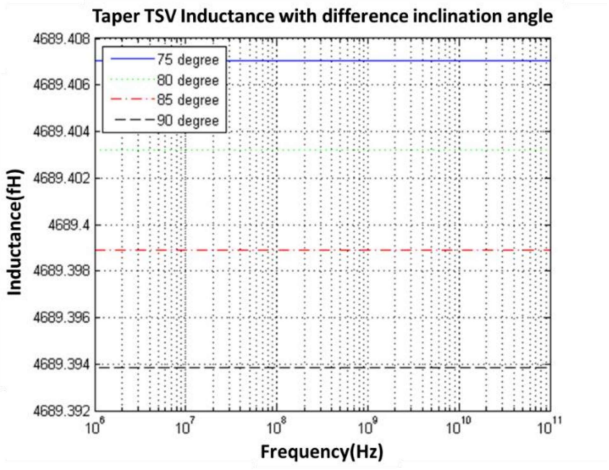


Figure 20 Taper TSV inductance with different inclination angle

2.2) Substrate modeling and verification by using coplanar wave model

2.2.1)CPW parasitic extraction

We used a CAD-based space mapping method to describe the fabricated CPW (coplanar wave model) lines. So, the dielectric constants of silicon are characterized in literature and hence were set as their standard value as 11.7. A simulation was done by using the value to compare with

measurement. CPW lines were set on an epitaxial layer and silicon substrate, the oxide isolation was then designed underneath.

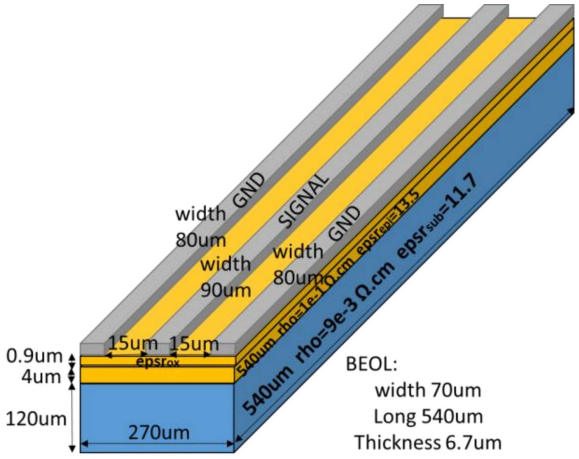


Figure 21 CPW model geometry

BEOL coplanar waveguides are copper made, with a thickness of 0.8µm, and ground planes width is equal to 80µm. Depending on the test structure, the signal line width is either 90µm with a slot of 15µm (CPW_W1) or 60µm with a slot of 30µm (CPW_W2). There are 3 different lines variation lengths: 60µm, 240µm and 540µm. The coplanar waveguides are realized in a highly conductive silicon substrate (rho=9mΩ.cm for low resistive, rho=62Ω.cm for high resistive, ε_r=11.7) with a thickness of 120µm. A thin epitaxial layer (thickness: 4.5µm, resistivity: 10Ω.cm, permittivity: 11.7) is deposited on the substrate. Lines are isolated from the substrate by an oxide layer (thickness: 0.9µm, permittivity: 5.2).[108]

Coplanar lines resistance, self and mutual inductances are calculated from experimental formulas. Resistance is calculated for a DC value, without taking into account the skin effect. And inductances (self and mutual) are calculated depending on the inductance analytical expressions [109].

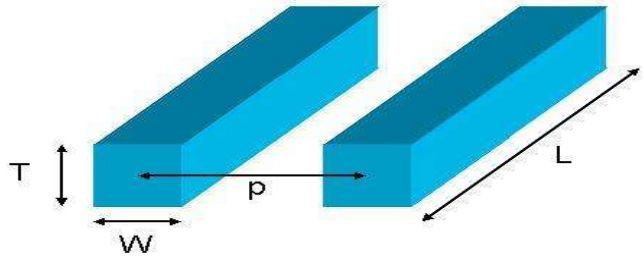


Figure 22 CPW line structure

$$R = \rho \frac{L}{W \cdot T} \quad (2\text{-}60)$$

$$L_{self} = \mu_0 \mu_r \frac{L}{2\pi} [\ln\left(\frac{2L}{W+T}\right) + 0.5 + \frac{0.447(W+T)}{2L}] \quad (2\text{-}61)$$

$$M = \mu_0 \mu_r \frac{L}{2\pi} [\ln\left(\frac{2L}{p}\right) - 1 + \frac{p}{L}] \quad (2\text{-}62)$$

where ρ is the metal resistivity (copper: 1.72e-8 Ω.m), μ_0 and μ_r the vacuum and the copper permeabilities, W, L, T and p respectively the line width, length, thickness and the pitch between two lines.

The interline/coupling capacitance C_{inter} between lines is calculated according to the equations defined by Nurmi in [110] from the concerned lines surfaces and the fringe capacitances C_f and C_f' taken at the boundaries and the middle of the coupled-lines. Cp is the coupling capacitance between the ground plane and the concerned line surface, which is also treated in the literature as the line's self-capacitance [109]

$$C_f = \varepsilon_0 \varepsilon_{ox} (0.075 \left(\frac{W}{H}\right) + 1.4 (\frac{T}{H})^{0.222}) \quad (2\text{-}63)$$

$$C_f' = \frac{C_f}{1+(H/S)} \quad (2\text{-}64)$$

$$C_p = \varepsilon_0 \varepsilon_{ox} \frac{W \cdot L}{H} \quad (2\text{-}65)$$

$$C_{inter} = C_f - C_f' + \frac{\varepsilon_0 \varepsilon_{ox} L}{100} (3\frac{W}{H} + 83\frac{T}{H} - 7(\frac{T}{H})^{0.222}) \cdot (\frac{H}{S})^{1.24} \quad (2\text{-}66)$$

Where ε_{ox} and ε_0 are the silicon oxide and the vacuum permittivity and S the lines gap. An average value of the width W is considered because signal and ground lines are geometrically different in width.

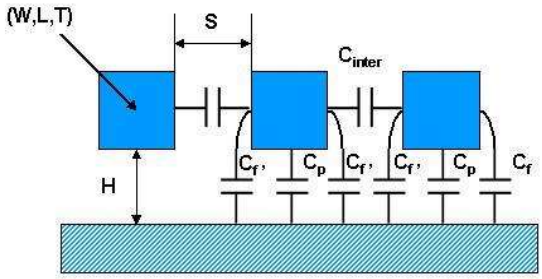


Figure 23 Illustration of the capacitive couplings between interconnect lines over a ground plane

In the case of the CPW, when the substrate is highly conductive, like in our test structures, Eddy currents can be neglected in low and medium frequency. The substrate can then be modelled as a very low resistance or a simple node. Vertical current in the epitaxial layer for each coplanar line is modelled by a resistance (Repi) in parallel with a capacitance (Cepi). The capacitances of the oxide layer (Cox) isolating the lines from the substrate are also included in the environment modelling.

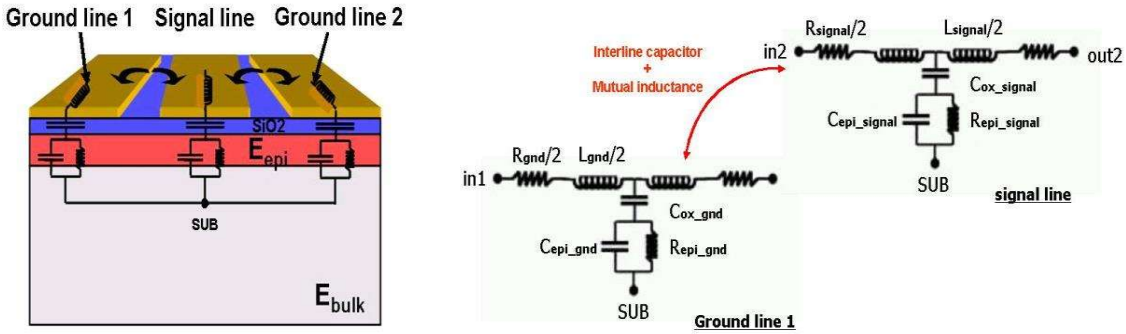


Figure 24 Coplanar lines front view (left figure). {RLCG} compact modelling of the signal line and one ground line of the coplanar waveguide (right figure).

Parameters are calculated from the expressions listed below: [109]

$$R_{epi} = \rho_{epi} \frac{T_{epi}}{W \cdot L} \tag{2-67}$$

$$C_{epi} = \frac{\varepsilon_0 \varepsilon_{epi} \cdot L \cdot W}{T_{epi}} \tag{2-68}$$

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} \cdot L \cdot W}{T_{ox}} \tag{2-69}$$

The coplanar waveguide model is shown in Figure 24 with all the lines connected in the substrate through a node SUB. Depending on the system physical and material data, the induction between the two ground lines can be neglected or not.

The assumption of modelling the conductive substrate as a simple node is only viable for low and medium frequencies. Substrate coupling effects require to be added in the system electrical modelling by describing the substrate as a {RLCG} network to evaluate precisely the IC's losses in high frequency.

From this perspective, an extraction demo is proposed relying on the Transmission Line Method for multi-layered substrate extraction. Basically, a current is applied on one contact pad which can be placed at the substrate surface or placed anywhere in the substrate. A voltage is then collected at another contact placed atop or within the substrate too, permitting to deduce a transfer impedance matrix [Z_T] which relies on the number of contacts. Substrate coupling effect between two contacts is generally modelled by a resistance in parallel with a capacitance. To extract the values of the overall resistances and capacitances constituting the substrate network from the elements of Z_T, the matrix is inverted to obtain a conductance matrix G_T and nodal analysis using Kirchhoff's Current Law (KCL) is applied. The method can be used for both high resistive or high conductive substrates being uniform (same resistivity and permittivity in all the considered volume) or not, explaining why a multi-layered approach has been considered. Moreover, values of the substrate electrical network can be given in DC or evolving in function of the frequency. The detailed method can be found in [111] in which it was validated for two contacts. Currently, the method is expanded on TSVs.

The method was applied in the example case of coplanar waveguides at the top of a high resistive substrate without epitaxial layer. Coplanar lines can hence be assimilated to three contacts. Material and technological data considered for the lines and oxide layers are the ones of the CPW test structure. Substrate height and permittivity are also kept and resistivity is fixed to 60Ω.cm. The following figure illustrates the corresponding substrate network.

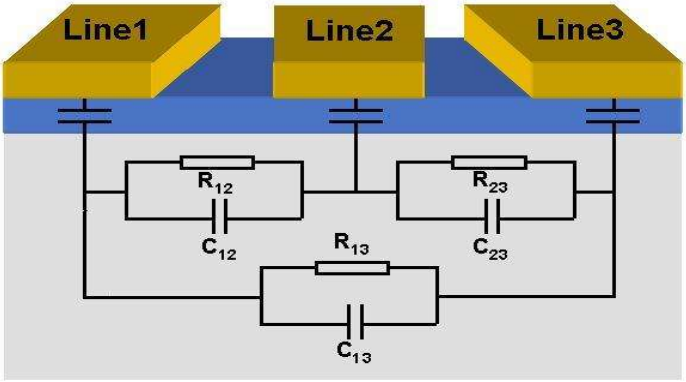


Figure 25: CPW substrate modelling.

Values of the resistances and the capacitances are derived from the transfer conductance matrix such that:

$$G_T = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} \quad (2\text{-}70)$$

$$G_T = \begin{bmatrix} g_{12}+g_{13} & -g_{12} & -g_{13} \\ -g_{12} & g_{12}+g_{23} & -g_{23} \\ -g_{13} & -g_{23} & g_{23}+g_{13} \end{bmatrix} \quad (2\text{-}71)$$

with g12 = (R12 // C12), g13 = (R13 // C13), g23 = (R23// C23)

2.2.2)Experimental de-embedding process for CPW

The first step is to extract the contribution of coplanar access to the measurement of the total test structure by using a vector network analyzer, as shown in Figure 26. A new method has been performed to rigorously extract access line effects. This method is presented with details in a recent publication [96].

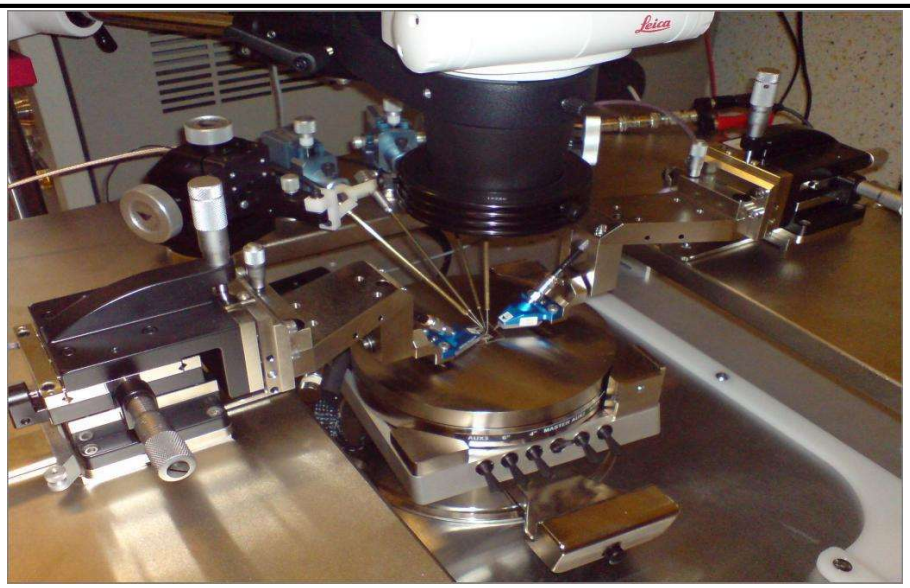


Figure 26 Measurements with a Vector Network Analyzer (VNA) for a frequency sweep [112]

Using this method we make first a measurement of a "Thru" test structure. This structure connects directly right and left coplanar access lines. Measurements of the ABCD matrix of this "Thru" structure give the ABCD matrix of the coplanar access line, named $ABCD_{\text{test fixture}}$. Next, we de-embedded the contribution of two test fixtures on the measurement of the total test structure using formula (2-71). $ABCD_{DUT}$ and $ABCD_{coplanar}$ are respectively the ABCD matrix of the "total test structure" and the part "CPW"

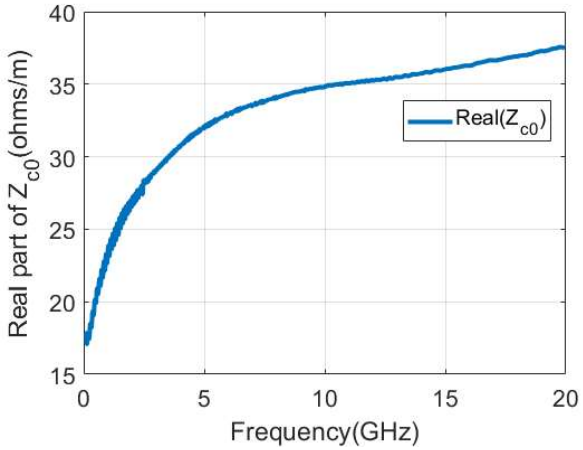
$$\begin{bmatrix} A_{coplanar} & B_{coplanar} \\ C_{coplanar} & D_{coplanar} \end{bmatrix} = \begin{bmatrix} A_{testfixture} & B_{testfixture} \\ C_{testfixture} & D_{testfixture} \end{bmatrix}^{-1} * \begin{bmatrix} A_{DUT} & B_{DUT} \\ C_{DUT} & D_{DUT} \end{bmatrix} * \begin{bmatrix} A_{testfixture} & B_{testfixture} \\ C_{testfixture} & A_{testfixture} \end{bmatrix}^{-1} \quad (2\text{-}72)$$

The propagation constant of the line and its characteristic impedance are derived from $ABCD_{coplanar}$ matrix according to the following equation (ANNEX 1).

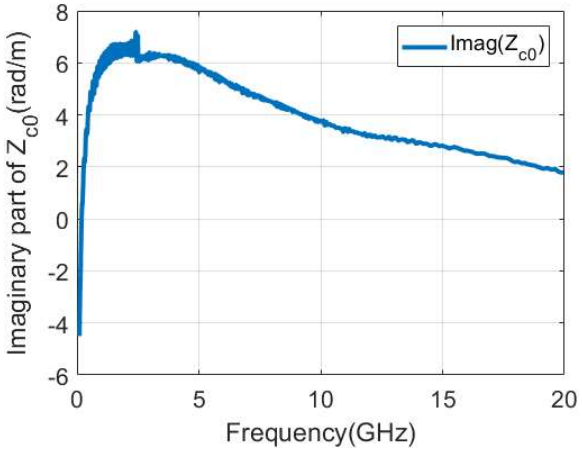
$$ABCD_{coplanar} = \begin{bmatrix} \cosh(\gamma_0 \Delta L) & Z_{c0}\sinh(\gamma_0 \Delta L) \\ \sinh(\gamma_0 \Delta L)/Z_{c0} & \cosh(\gamma_0 \Delta L) \end{bmatrix} \quad (2\text{-}73)$$

Once the ABCD-parameters of de-embedded CPW are known, its propagation characteristics can also be determined through the formulas in ANNEX 1.

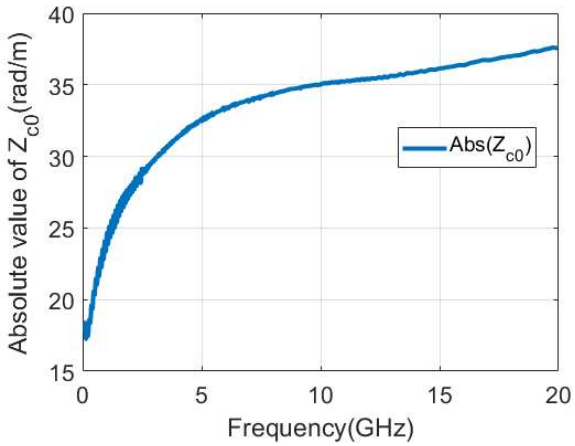
Real part of the characteristic impedance and imaginary part of the propagation constant are presented in Figure 27 as an example.



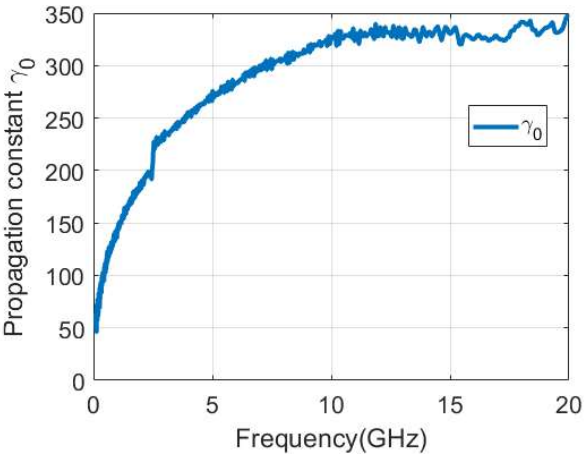
(a) real part of the Characteristic impedance



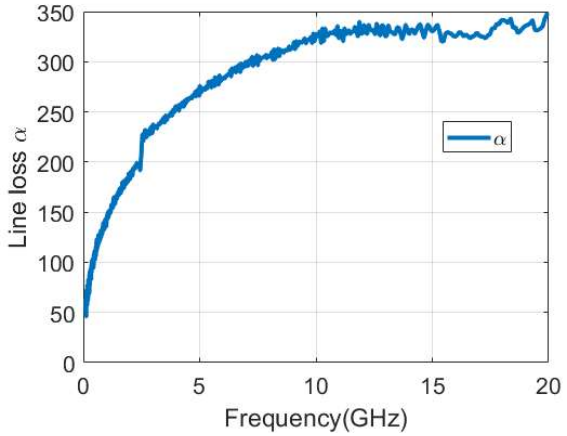
(b) imaginary part of the Characteristic impedance



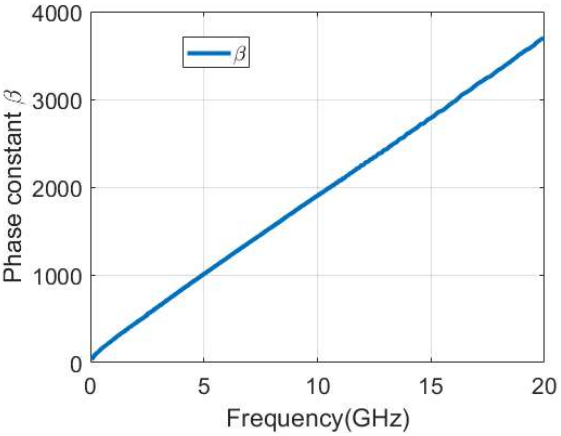
(c) absolute value of the Characteristic impedance



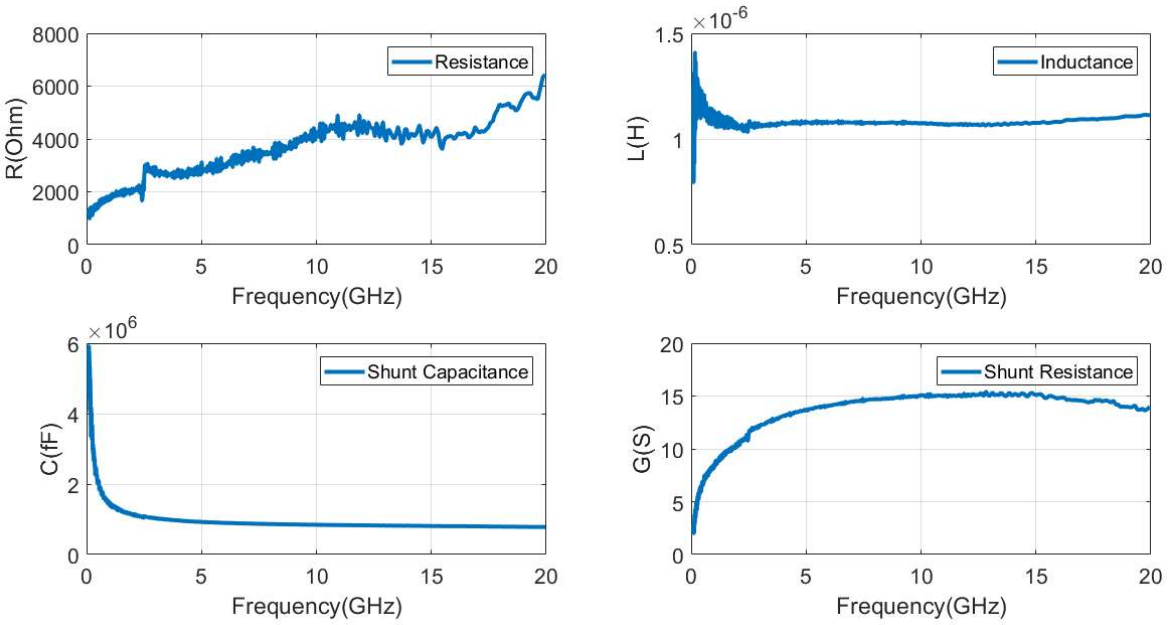
(d) the propagation constant



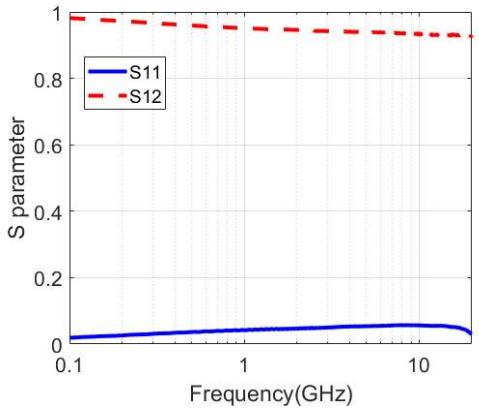
(e) the attenuation constant



(f) the phase constant



(g) RLCG parameters



(H) S parameters

Figure 27 Characteristic impedance Z_C and the propagation constant γ parameters of CPW model of High resistive substrate (a)real part of the Zc (b)imaginary part of the Zc (c)absolute value of the Zc (d)propagation constant gamma (e) attenuation constant alpha (f) phase constant beta (g)RLCG parameters (h)S parameters S11&S12 for the de-embedded experimental data

As we can see from figure 26, the measured data have a quite stable transmission characteristics between 5GHz and 20GHz. Because of the test bench's limit in (very) high frequency, the measured data is correct below 20GHz.

2.2.3)ADS Parameter extraction and model fitting on experimental data

The EDA software ADS can replace the value of one component (resistance or capacitance) by a variable. So we can predefine one variable arbitrarily by <Var> block, as shown in Figure 29. We can define the constraint of the variable, for example, we can restrict the variable in the interval

by giving the maximum and minimum value or giving a percentage of variation. If no restriction is fixed, ADS can freely vary the value of variables.

We replace the substrate and the epitaxial layer by a RC model. The complete circuit can be simulated in ADS as following.

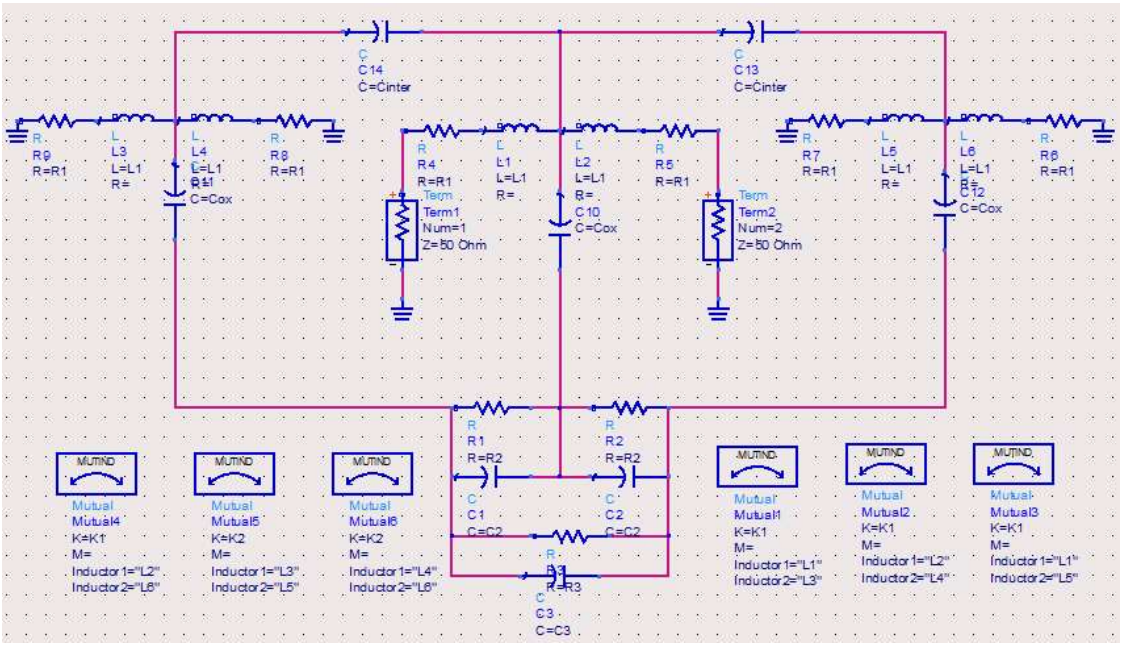


Figure 28 ADS setup for CPW model with low resistive substrate

Here we define all the variables and give them an initial value in the block <Var>.

Resistive substrate

Figure 29 ADS setup parameters for CPW model with low resistive substrate

INL (Lyon Institute of Nanotechnology) has developed a program whose name is 3D-TLE (3D Transmission Line Extractor). This program is developed in Matlab which can generate the

network SPICE (Simulation Program with Integrated Circuit Emphasis). We can compare the results of simulation and optimization ADS (Red line), measurement (Blue line) and 3D-TLE (Pink line).

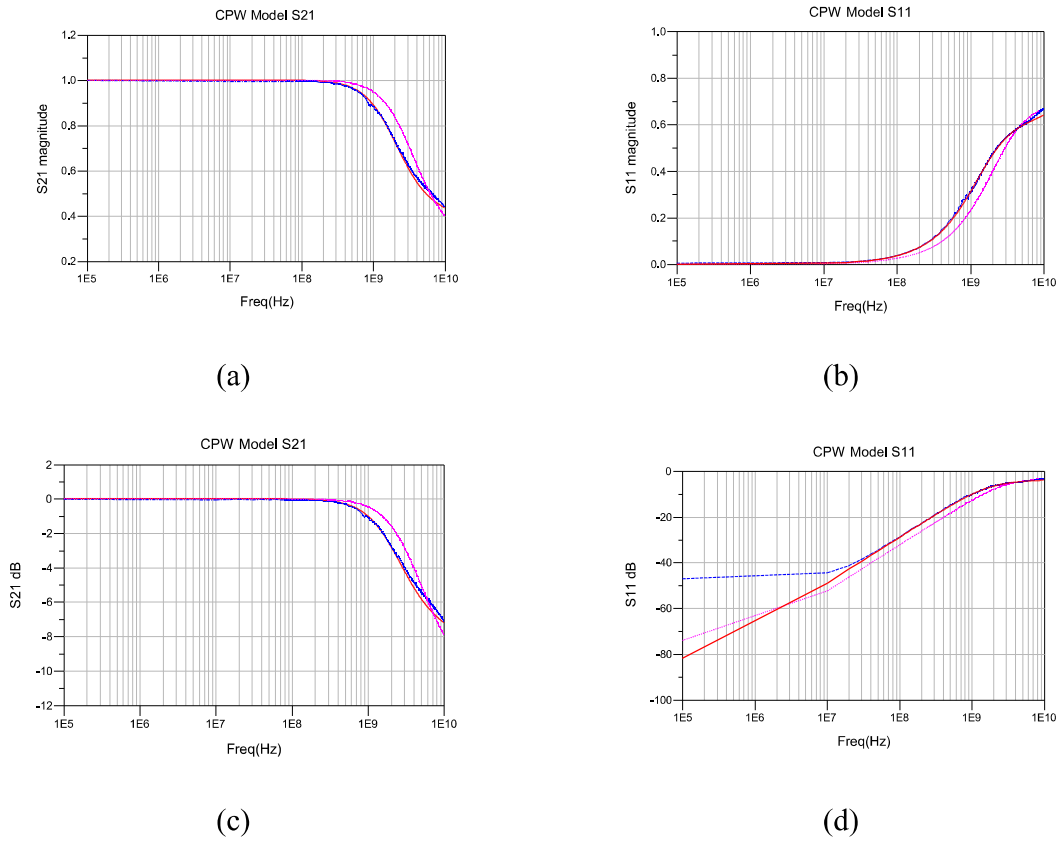


Figure 30 S parameters for CPW model (a) S21 magnitude (b) S11 magnitude (c) S21 in dB (d) S11 in dB (red line : optimiszation; blue line : mesurement; pink line : 3D-TLE)

The original parameters, optimized parameters and 3D-TLE extracted parameters

Table 6 Comparison between original parameters, optimized parameters and 3D-TLE

	Original parameter	**Optimized parameters**	**3D-TLE**
R1(ohm)	0.089126	0.000112646	0.011514
L1(H)	1.9372e-9	0.926605e-15	1.7145e-10
R2(ohm)	100000 ohm	197985	0.29467
C2(F)	0.6E-12	0.984205e-12	3.514e-14
R3(ohm)	100000 ohm	415.987	1.1906
C3(F)	0.6E-12	14.996e-15	8.6966e-15
Cox(F)	1.38e-11	5.98365e-12	4.0887e-12
Cinter(F)	5.4228e-14	6.10788e-14	1.174e-14
K1(H)	0.65818	0.588136	0.49259
K2(H)	0.52744	0.320655	0.33268

2.2.4)3D-TLE extraction (homemade extractor) results

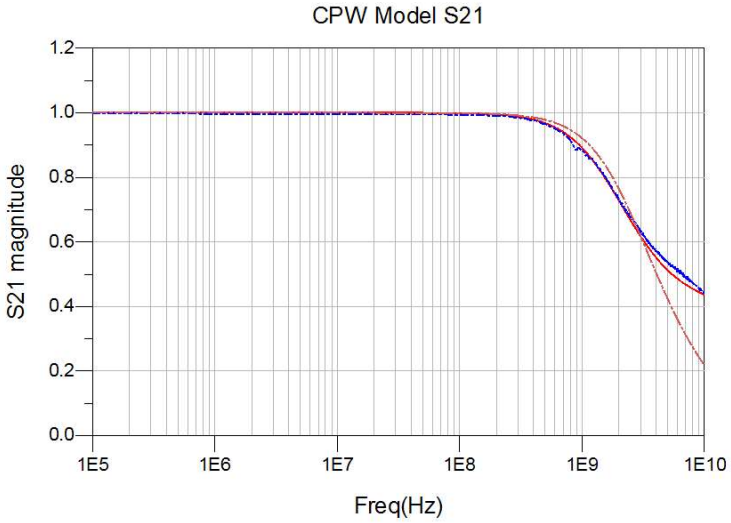


Figure 31 Extracted S parameters of CPW model for low resistive substrate (red line: optimization; blue line: measurement; pink line: 3D-TLE)

The extracted layers parameters:

Table 7 Restored layers physical parameters

	Conductivity(ohm*m)	Relative permittivity
SUBSTRATE	1e-4	11.7
EPITAXIAL	0.1	13.5
OXIDE		11
BEOL	2e-8	

If we change only the substrate, and in ADS, we can establish a substrate changeable circuit, shown as following

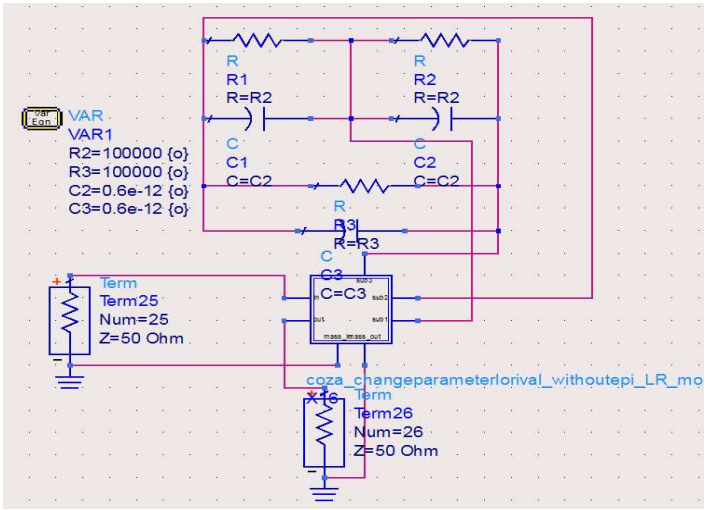


Figure 32 Importation in ADS of the extracted 3D-TLE CPW model

The result can be seen like following

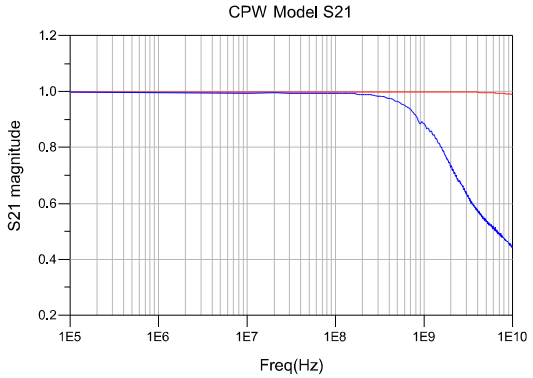
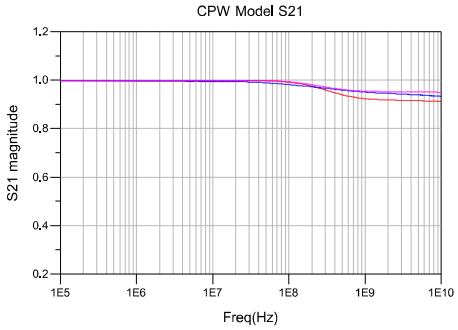
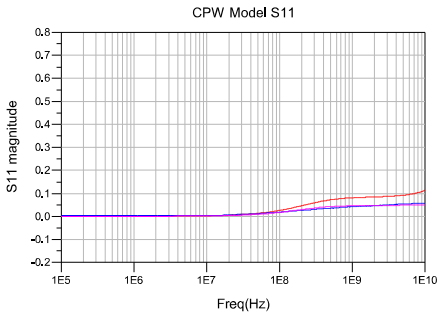


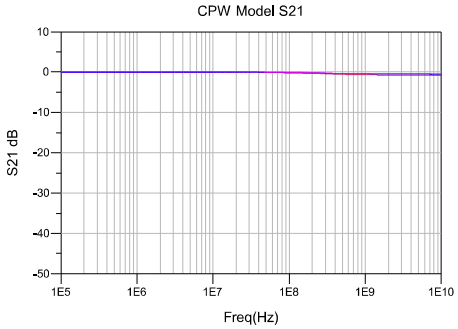
Figure 33 S21 magnitude by changing substrate conductivity (red line: optimization; blue line: measurement; pink line: 3D-TLE)

As we can see, if we change only the substrate conductivity, it will not match with the measurement. So we can see that the substrate conductivity has a great influence to the high frequency transmission. The higher is the substrate conductivity, the more obvious gets the signal attenuation.

2.2.5) High resistive substrate study







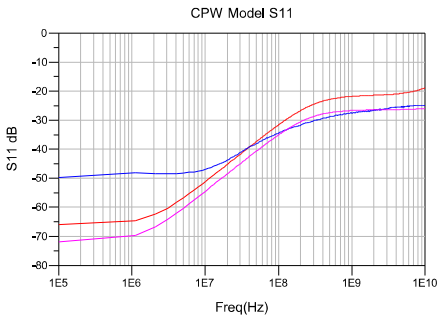


Figure 34 S parameters for CPW model of high resistive substrate (a) S21 magnitude (b) S11 magnitude (c) S21 in dB (d) S11 in dB (red line: optimization; blue line: measurement; pink line: 3D-TLE)

Table 8 Comparison between original parameters, optimized parameters and 3D-TLE for high resistive substrate

	Original parameter	**Optimized parameters**	**3D-TLE**
R1(ohm)	0.012665	0.02533	0. 012665
L1(H)	1.7145e-10	1.78984e-10	1.7145e-10
R2(ohm)	1473.3402	478.838	1473.3402
C2(F)	3.514E-14	6.91474e-14	3.514e-14
R3(ohm)	5953.2097	18.5399	5953.2097
C3(F)	8.6966E-15	4.95273e-17	8.6966e-15
Cox(F)	1.9328e-12	2.77256e-12	1.9328e-12
Cinter(F)	5.55e-15	6.10788e-14	5.55e-15
K1(H)	0.49259	0.49259	0.49259
K2(H)	0.33268	0.33268	0.33268

2.2.6)Transient study - Eye diagram

The eye diagram can be used to evaluate the extracted interconnection transmission's quality (3D-TLM). In order to simplify the simulation, we input a numeral signal and measure the output signal. And the output signal is more or less deformed according to the interconnection, which can be seen through a bigger or smaller eye diagram.[92]–[101]

We can get the eye diagram by using ADS's <Eye Probe> and <Simulation-Transient> study. We put a bit sequential voltage source at the input by accompanying a 50 ohm resistance at its output. We attach the under test numeral component in the circuit and add a 100 fF capacitance at the output. We can get the three different setting.

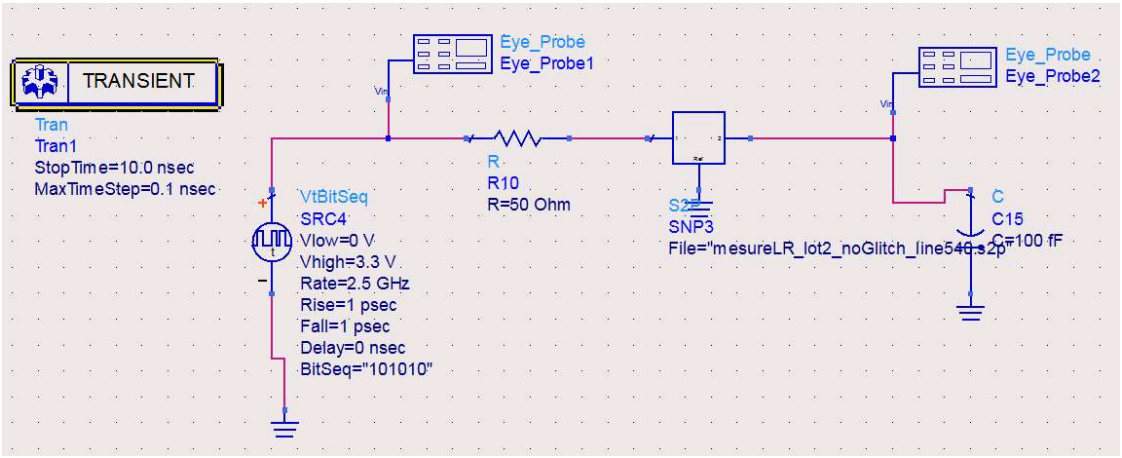


Figure 35 Measurements based transient ADS setup

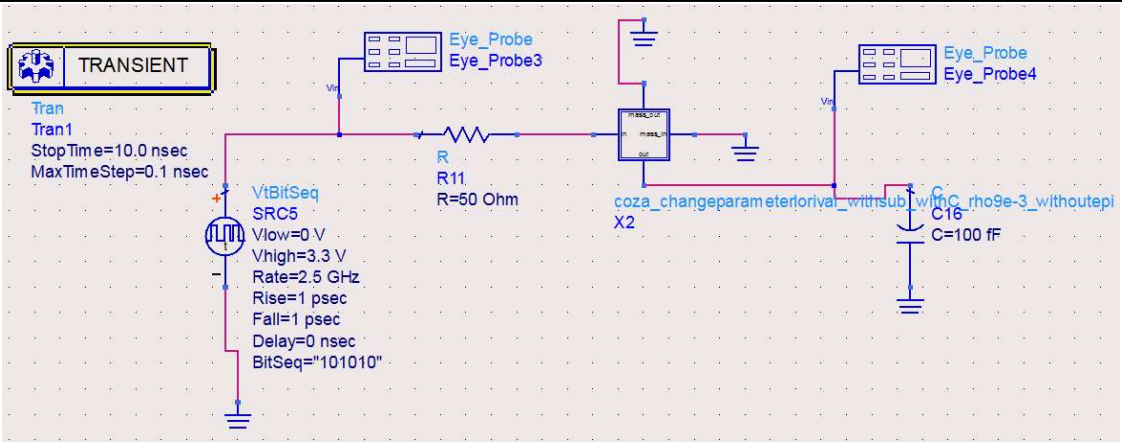


Figure 36 3D-TLE based transient ADS setup

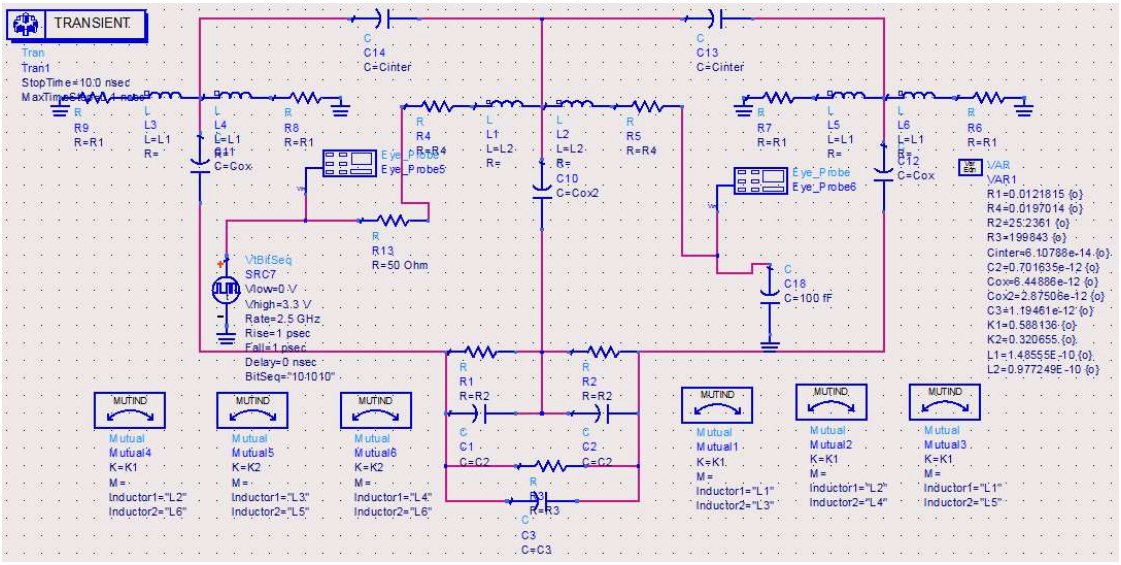
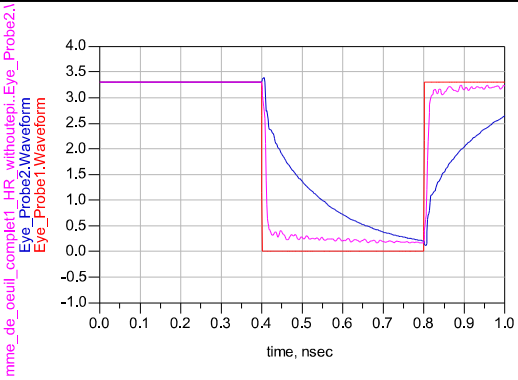


Figure 37 Transient Optimization circuit

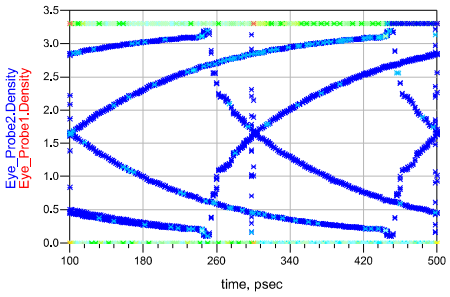
In our case, we use the following source setting

Vlow=0V and Vhigh=3.3V
Frequency=2.5GHz
Rise time 1 ps
Fall time 1 ps

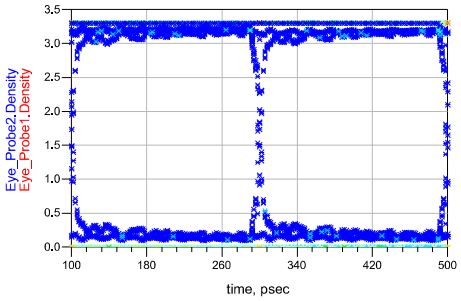
We can get the following result



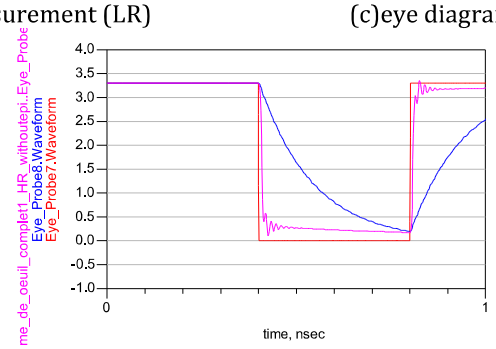
(a)waveform of measurement (red: original signal; blue: LR substrate result; pink: HR sub result)



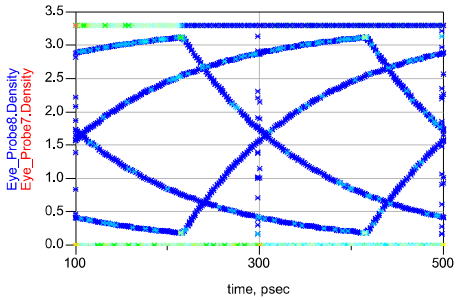
(b)eye diagram of measurement (LR)



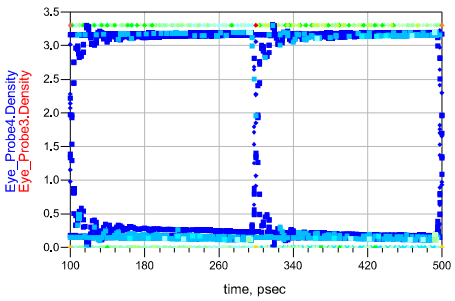
(c)eye diagram of measurement (HR)



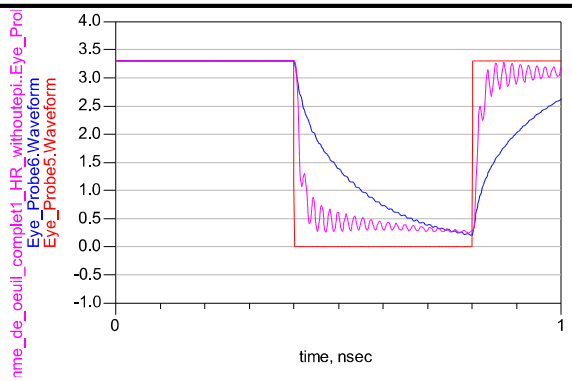
(d)waveform of 3D-TLM (red:original signal blue:LR substrate result pink: HR sub result)



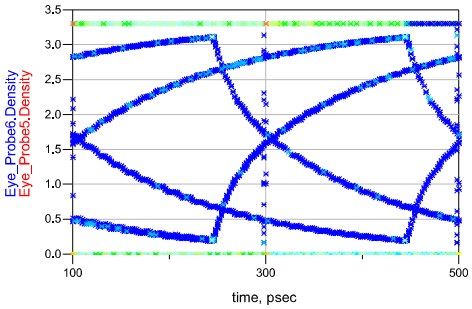
(e)eye diagram of 3D-TLM (LR)

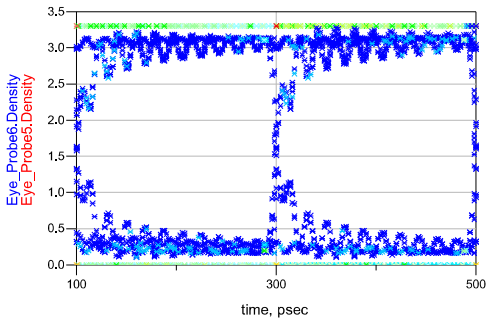


(f)eye diagram of 3D-TLM (HR)



(g)waveform of optimized circuit (red:original signal blue:LR substrate result pink: HR sub result)





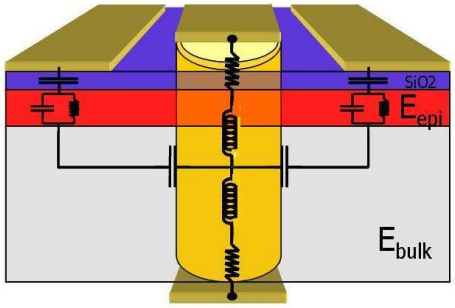
(h)eye diagram of optimized circuit (LR) (i)eye diagram of optimized circuit (HR)

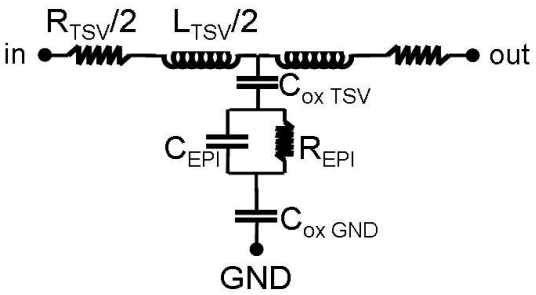
Figure 38 (a)(d)(h) show the input and output signal of the interconnection, (b)(e)(h) display the corresponding eye diagram for the low resistive substrate, (c)(f)(i) display the corresponding eye diagram for the high resistive substrate.

2.3) TSV models' parasitic extraction

2.3.1)Characterization and parameter extraction of two TSV model

Here, we present our own analytical expressions for the medium-density TSV compact model resistance and oxide capacitance. The expressions of TSV are deduced from the formula of a perfect cylindrical conductor, it depends on the conductor length, the thickness and radius. [108]





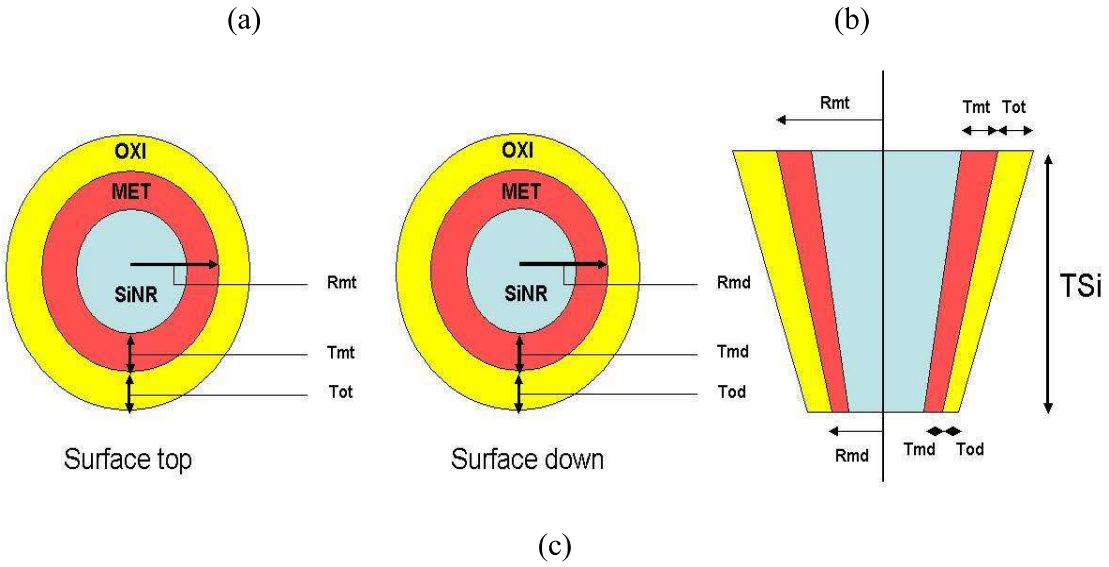


Figure 39 TSV schematic (a) cross section view (b) compact model (c) geometry parameters

$$R_{ot} = R_{mt} + T_{ot} \quad (2\text{-}74)$$

$$R_{od} = R_{md} + T_{od} \quad (2\text{-}75)$$

$$R_{TSV} = \frac{H}{\pi\sigma}\frac{1}{2(R_{mt}T_{md}-R_{md}T_{mt})}\ln\left(\frac{T_{md}}{2(R_{md}-T_{md})}\cdot\frac{2R_{mt}-T_{mt}}{T_{mt}}\right) \quad (2\text{-}76)$$

$$C_{ox(TSV)} = \frac{\varepsilon_0\varepsilon_{ox}2\pi H}{T_{ot}-T_{od}}\left[R_{ot} - R_{od} + \frac{R_{ot}\cdot T_{od}-R_{od}\cdot T_{ot}}{T_{ot}-T_{od}}\ln\left(\frac{T_{od}}{T_{ot}}\right)\right] \quad (2\text{-}77)$$

$$L_{TSV} = \frac{\mu_0\mu_r H}{2\pi}\left[sinh^{-1}\left(\frac{H}{R_a}\right) + \frac{R_a}{H} + 0.15 + \sqrt{\left(\frac{R_a}{H}\right)^2 + 1}\right] \quad (2\text{-}78)$$

$$M_{TSV} = \frac{\mu_0\mu_r H}{2\pi}\left[sinh^{-1}\left(\frac{H}{p}\right) + \frac{p}{H} - \sqrt{\left(\frac{p}{H}\right)^2 + 1}\right] \quad (2\text{-}79)$$

Where: *Rmt* and *Tmt* are the copper layer radius and thickness of the TSV top surface;

Rot and *Tot* the oxide layer radius and thickness of the TSV top surface;

Rmd and *Tmd* the copper layer radius and thickness of the TSV bottom surface;

Rod and *Tod* the oxide layer radius and thickness of the TSV bottom surface.

p is the pitch between two nearby TSVs and R_a the TSV average radius

TSV filing material does not significantly affect its RF behavior. Besides, the influences of the copper layer thickness and the TSV radius are very low. So, the self- and mutual- inductances can still use the analytical expressions of a filled cylindrical conductor.

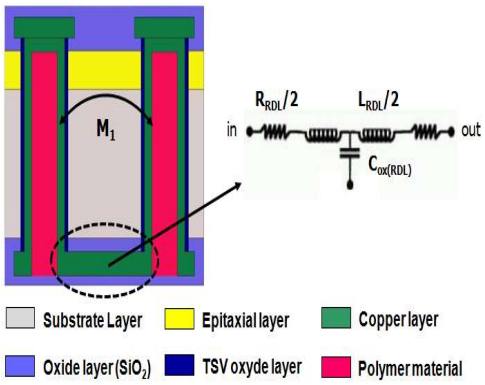
Since the substrate is highly conductive for the studied CPWs model, it can be modelled as a simple node. For each CPW line, the vertical current transmission path in the thin epitaxial layer has been treated as a parallelepiped shape and so it can be modelled by a resistance (Repi) in parallel with a capacitance (Cepi). The isolating lines from the epitaxial layer can be modelled by an oxide layer capacitances (Cox). [108]

$$R_{epi} = \rho_{epi} \frac{T_{epi}}{W \cdot L} \quad (2\text{-}80)$$

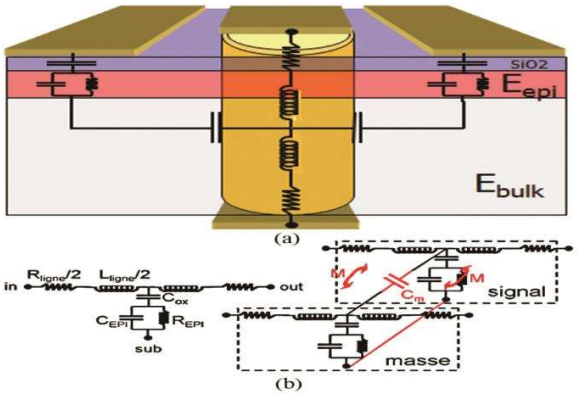
$$C_{epi} = \frac{\varepsilon_{epi}\varepsilon_0 W \cdot L}{T_{epi}} \quad (2\text{-}81)$$

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0 W \cdot L}{T_{ox}} \quad (2\text{-}82)$$

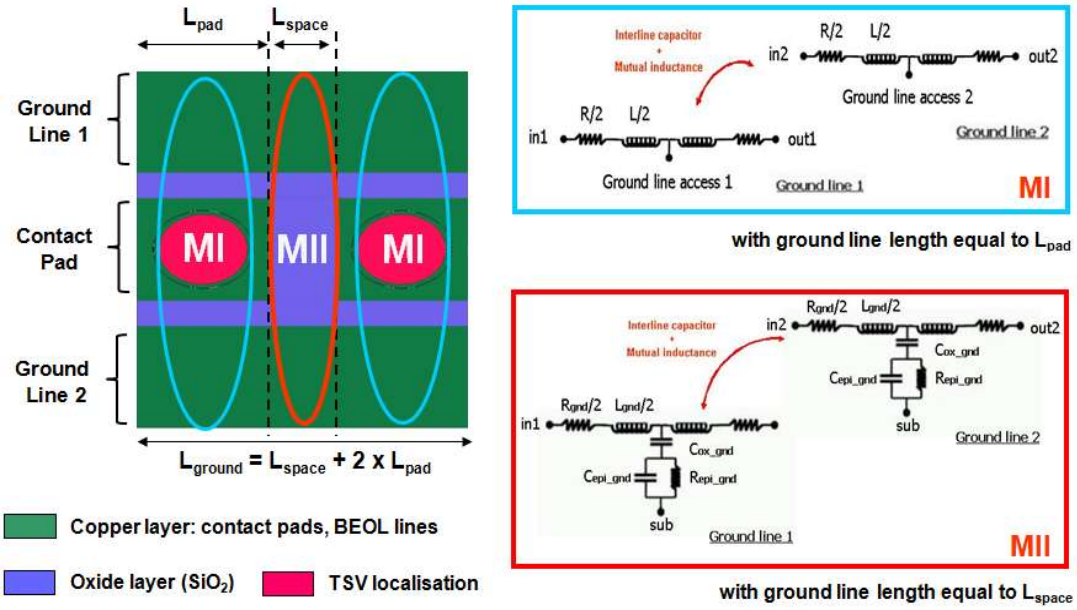
The electrical parameter values must be adjusted based on the distributed elementary cell length, width and height. For the TSV chain, the currents passes vertically by the epitaxial and the oxide layers and reach finally the BEOL level ground planes. The epitaxial and oxide layers electrical parameters (Repi(TSV), Cepi(TSV) and Cox(GND)) can be calculated by using the same expression as the coplanar waveguide. The substrate and TSVs couplings are considered with the geometrical capacitance Cox(TSV). The coupling effects of TSVs are considered. The TSV chain electrical model of the BEOL ground lines is divided into serial blocks on the overall surface. These surface parts have a length of the TSVs contact pads length Lpad. The epitaxial layer parameters (Repi(TSV), Cepi(TSV)) and the oxide capacitance (Cox(GND)) which model the current propagation to the ground line through the TSV, should then be calculated with L = Lpad. The width and the thickness are the same as the other line parts. The surface cells of ground lines included in the current paths can be simply modelled by a RL networks; otherwise they are modelled as shown in the following figures.



(a)



(b)



(c)

Figure 40 2xTSV chain (a) Medium density TSV front view (b) RLCG compact modeling of the medium-density TSV including the current path (c) Decomposition of the BEOL ground lines into RLCG serial blocks depending on the considered surface (MI and MII models)

As an illustration, the above figures show how the two top BEOL ground lines are changed into serial blocks for a 2xTSV U-chain. The interline current paths should also be considered, they have mainly two kinds, MI and MII. The total wire length, Lground, is equal to 2Lpad, plus the BRDL line length, Lspace. Lspace represents to the gap between two contact pads. The BRDL line connecting the two TSVs, the substrate coupling of which can be expressed by an oxide capacitance between the SUB node and BRDL, which is located in the contact pads gap (MII).

The 2xTSV has a form of "U". So for nxTSVs chains, there will be n/2 "U-shaped" structures connected at the BEOL surface by contact pads and 60µm access BEOL lines.

The following figure shows the structure of a 4xTSV chain; the coupling effects between the four TSVs are also represented. The BEOL ground line total length then equals: [108]

$$L_{BEOL} = nL_{pads} + \frac{n}{2}L_{space} + (\frac{n}{2} - 1)L_{access} \qquad (2\text{-}83)$$

It illustrates the ground lines total transmission line length (related to the transmission loss) for nxTSV chain.

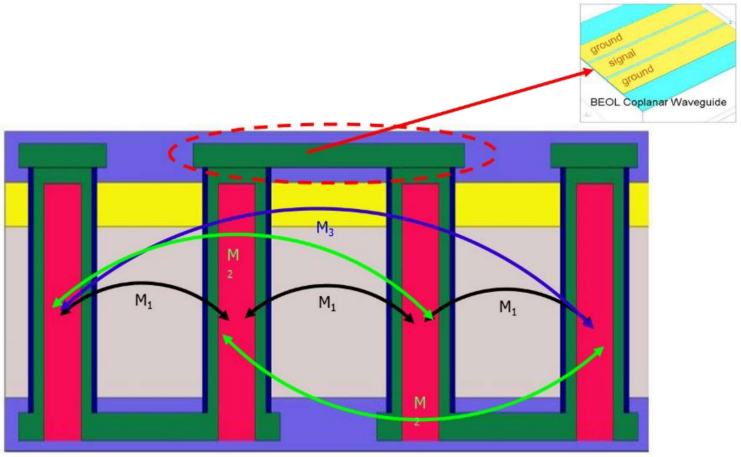


Figure 41 4xTSV chain side view: representation of the proximity effects between TSVs (inductive couplings). The two chains of 2xTSV are connected at the BEOL level with contact pads and an access interconnection line

2.3.2)Simulation and optimization of 2 TSVs U-model

We use the same simulation process. Firstly, we try to simulate the S parameters by using the netlist generated by the 3D-TLE extractor. And we compare it with the de-embedded experimental result (by using the test bench Figure 26).

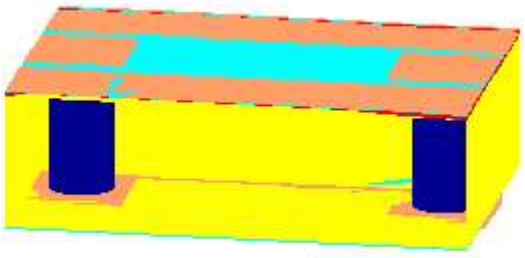


Figure 42 Physical geometry of 2 TSVs model

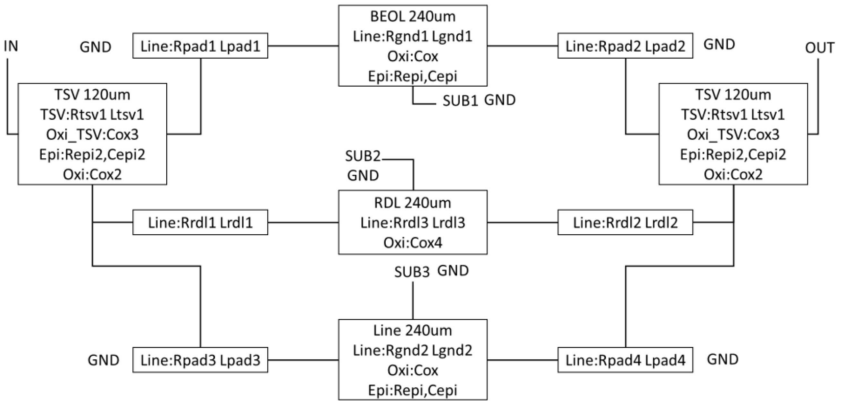


Figure 43 input script description

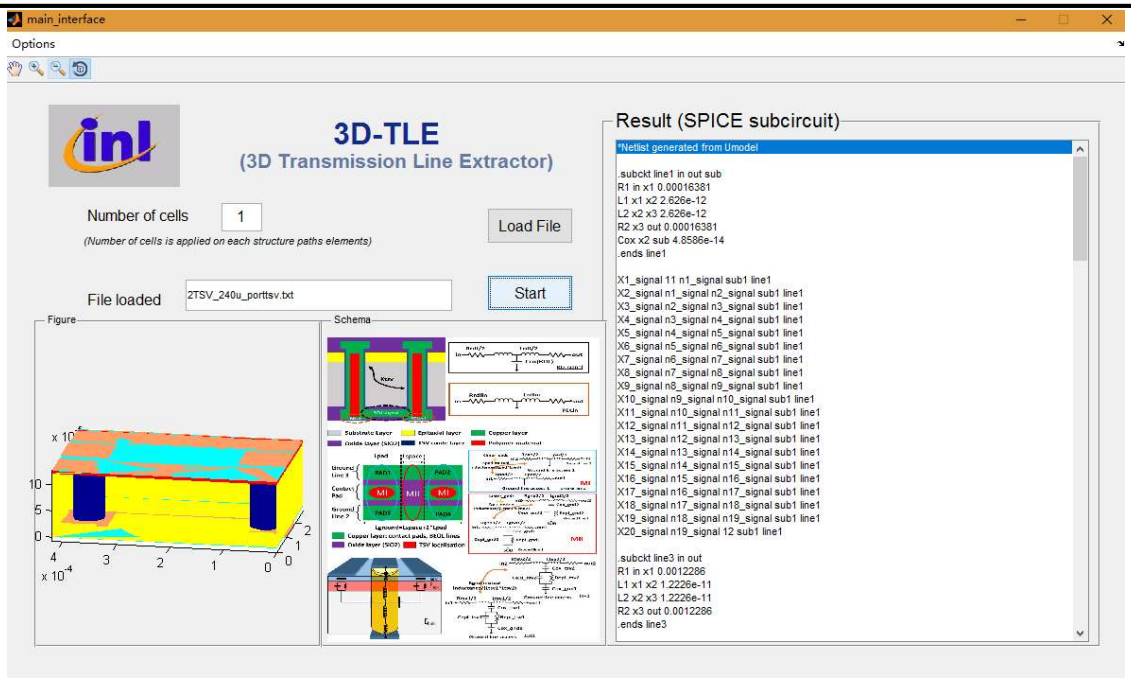


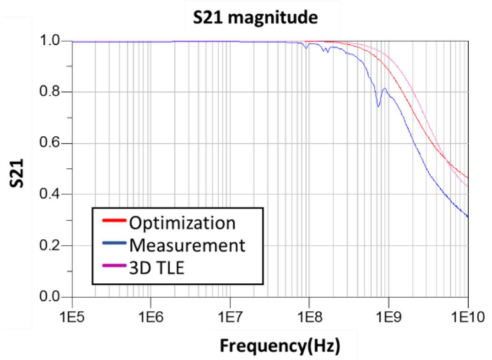
Figure 44 3D-TLE extractor setting

Through the pub [115], the substrate parasitic parameters can be expressed by a parallel of capacitance and conductance. And their expressions are shown as follow

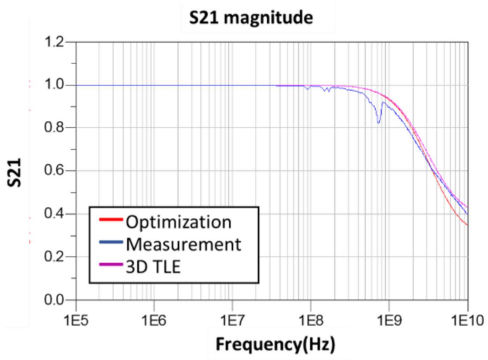
$$C_{Si\_sub} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,si}}{cosh^{-1}(\frac{p_{TSV}}{d_{TSV}})} \times h_{TSV}[F] \quad (2\text{-}84)$$

$$G_{Si\_sub} = \frac{\pi \times \sigma_{si}}{cosh^{-1}(\frac{p_{TSV}}{d_{TSV}})} \times h_{TSV}[S] \quad (2\text{-}85)$$

And here, when we extract the measurements, we must apply the de-embedding method, the following two figures show the difference between with and without de-embedding.



Measurements S21 result without de-embedding(blue line)



Measurements S21 result with de-embedding(blue line)

Figure 45 2xTSVs model S parameters (a) S21 magnitude without de-embedding (b) S21 magnitude with de-embedding

As we can see from the two figures, the result with de-embedding is more close to our simulated circuits.

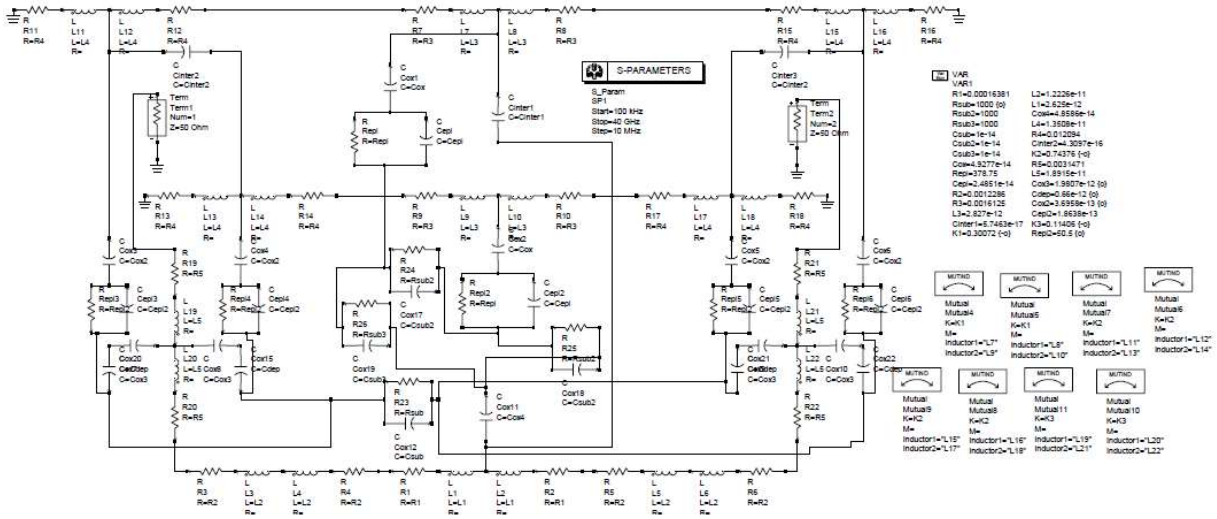


Figure 46 S parameters study setting for 2xTSVs model

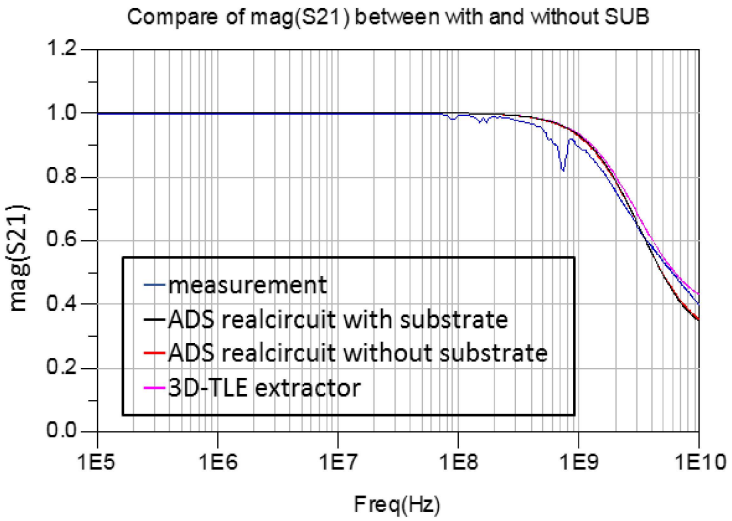
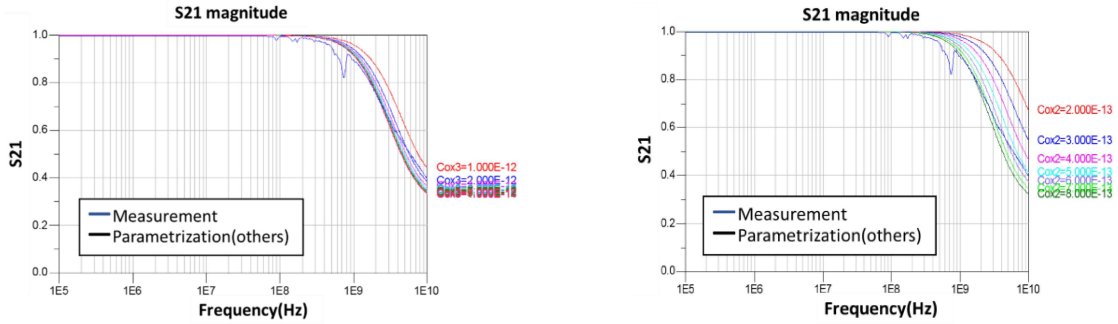
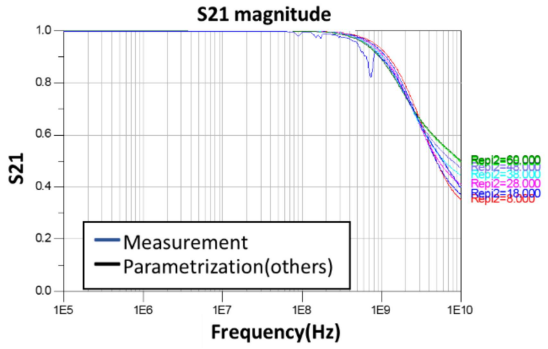


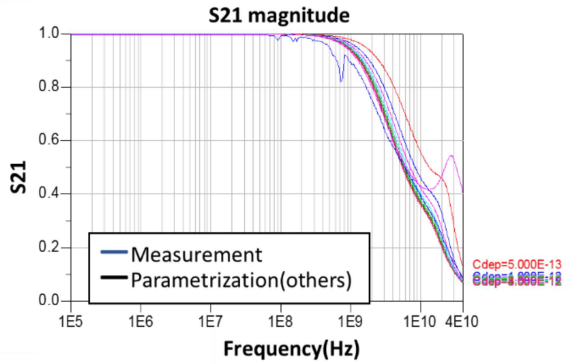
Figure 47 Comparison of S12 between 2TSV with and without SUB model, measurement(blue),optimized circuit result without SUB resistance(black), optimized circuit result with SUB resistance(red), 3D-TLE result(pink)



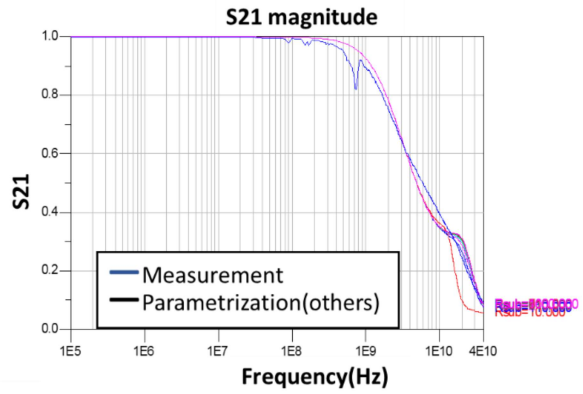
(a)Change Cox3(TSV oxide)



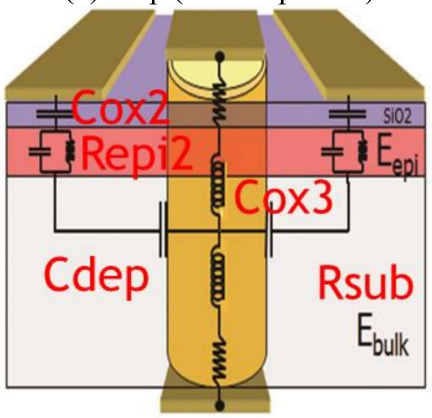
(b)Change Cox2(oxide layer capacitance close to TSV)



(c)Repi2 (TSV epi resistance)



(d)Cdep (TSV depletion)



(e)Rsub (TSV TSV direct connection)

(f)Parameters signification

Figure 48 Parametrizations (a) Cox3 (TSV oxide) (b) Cox2 (Oxide layer capacitance near TSV) (c) Repi2 (TSV epitaxial layer's resistance) (d) Cdep (TSV depletion capacitance) (e) Rsub (Substrate resistance) (f) Parameters' signification

As shown in (a), (b), when Cox3=2e-12F, the curve is much closer to measurements. And it corresponds to epsr_ox=3.28 (we use 5.8 originally at the 3D-TLE), and when Cox2=7e-13F, the curve is much closer to measurements. And it corresponds to a epsr_ox=10.98 (we use 5.8 originally at the 3D-TLE, Cox2=3.7e-13 originally), it has a very big influence to the final S parameter approximation. Repi2 has a big influence to the result. When Repi2=38ohms, the result is close to the measurements. And the 3D-TLE value is 50.5 ohms with a resistivity of 9.09e-2 ohm*m, now, with a Repi2=38ohms, the resistivity changes to 6.84e-2 ohm*m. The MOS depletion effect doesn't have a big influence to the S21 parameters, but at very high frequency, it has a slightly influence. Here the Cdep vary from 0.5e-13 F to 8e-12 F.

As we can see, after 10GHz, the substrate has a big influence to the S21 parameter. The best fit Rsub value is about 100 ohms, at this resistance, the substrate has a resistivity of about 0.108 ohm*m, which is 100 times bigger than the original 1e-4 ohm*m. But we don't see any difference at frequency below 10GHz. And R1,2,3,4,5 and L1,2,3,4,5, Cepi2 have slightly influence to the fitting curve. Repi Cepi Cox Cox4 Rsub2 Rsub3 Csub Csub2 Csub3 doesn't have influence. So the

2TSV model S21 parameter depends mostly on the Cox2(oxide layer close to TSV) Cox3(oxide TSV) Rsub (substrate resistance) Repi2 (epitaxial layer close to TSV)

So in all, the final influence factors are the substrate resistivity, oxide layer's permittivity, tsv isolation permittivity, and epitaxial layer resistivity.

So after the optimization of the only 4 parameters, we can get the final S21 parameter

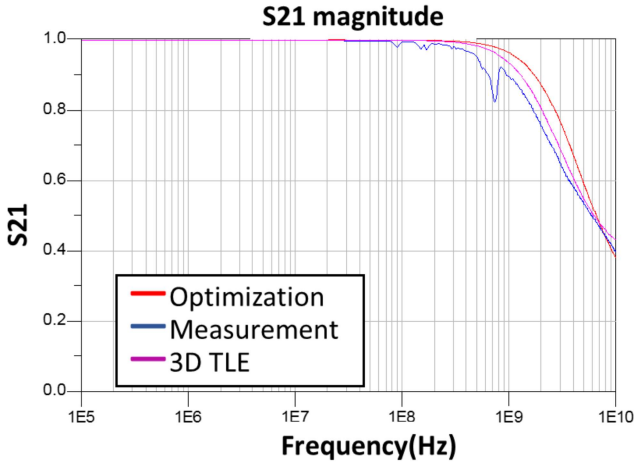


Figure 49 Optimized S parameters (blue: measurement, red: optimized, pink: 3D-TLE)

With our model, the extracted parameters are

Table 9 Comparison between original parameters and optimized parameters

Name	**Original value**	**Optimised value**
R1	0.00016381	0.00016381
R2	0.0012286	0.0012286
R3	0.0016125	0.0016125
R4	0.012094	0.012094
R5	0.0031471	0.0031471
L1	2.625e-12	2.625e-12
L2	1.2226e-11	1.2226e-11
L3	2.827e-12	2.827e-12
L4	1.3508e-11	1.3508e-11
L5	1.8915e-11	1.8915e-11
Repi	378.75	378.75
Cepi	2.4851e-14	2.4851e-14
Cox	4.9277e-14	4.9277e-14
Repi2	50.5	6.65094
Cepi2	1.8638e-13	1.8638e-13
Cox2	3.6958e-13	0.73916e-12
Cdep	0.66e-12	1.32e-12

Cox3	1.9807e-12	3.9614e-12
Cox4	4.8586e-14	4.8586e-14
Rsub	1000	1994.4
Rsub2	1000	1000
Rsub3	1000	1000
Csub	1e-14	1e-14
Csub2	1e-14	1e-14
Csub3	1e-14	1e-14

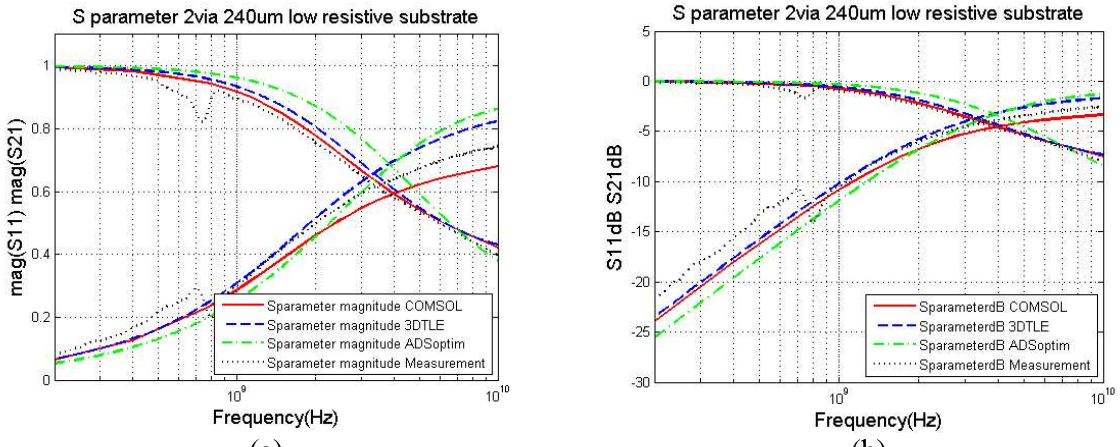
And with the optimized lumped parameters, we can find back the corresponding materials parameters, which are shown in the following table.

Table 10 Restored layers' material parameters

	Marked value	**Optimised Value**
Relative Permittivity TSV oxide layer	5.8	6.5001
Relative Permittivity oxide layer	5.8	11.6001
*Resistivity substrate (Ohm*m)*	1e-4	0.2154
*Resistivity epitaxial (Ohm*m)*	9.09e-2	1.2e-2

As we can see, the TSV oxide permittivity has changed from 5.8 to 6.5, that's close, so there may be some measurement's error, So is the resistivity of epitaxial layer. The oxide layer permittivity has doubled to 11.6, and the substrate is no more non resistive, its resistivity changes to 0.2154.

In order to verify our 3D-TLE extractor, a finite-element simulation (COMSOL Multiphysics) is realized. The simulation results are shown as following. They have a really good fit between 3D-TLE extractor, COMSOL simulation and measurement.



(a) (b)

Figure 50 3D-TLE verification by using FEM (COMSOL), ADS and measurements (a) Magnitude of S parameters (b) dB of S parameters

2.3.3)TSV matrix model

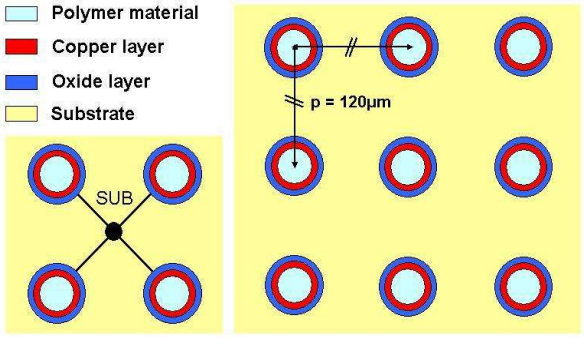


Figure 51 Medium-density TSVs regular matrices. Bottom left: all the TSVs' oxide capacitances join at a single node modeling the substrate (illustration for a 2x2 matrix). Right: 3x3 medium-density TSVs matrix considered for the timing domain analyses.

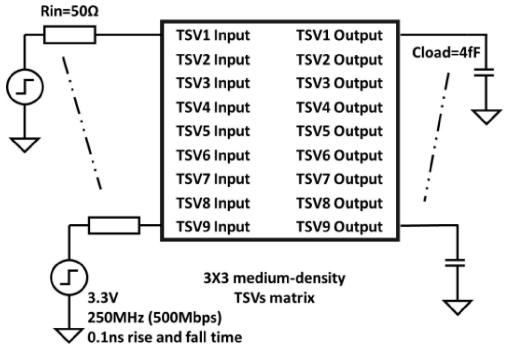


Figure 52 3x3 TSV matrix test bench used for Eye Diagram simulations.

Since the TSV electrical model has been verified in low and medium frequency, timing analyses are studied by using Eye Diagrams to check the signal integrity in the case of a 3x3 medium-density TSVs matrix [18], [50], [60], [114], [123]. We have modeled it using TSVs having the same dimensions used in their W1 configuration. The distance between the TSVs equals to 120 µm. Figure 51 shows this modelling consideration for a 2x2 TSVs matrix. The coupling effects among all the TSVs (inductive couplings) are once more evaluated in these studies. The Eye Diagrams are generated by Advanced Design System (ADS) by assuming a symmetrical test setting with 50 Ω input and output equivalent resistances Z_0. The TSVs are attached with a 100fF load capacitances (Figure 52).

Three configurations are studied and illustrated in Figure 53. The first configuration, all the TSVs are connected to ground except for the central TSV. The second configuration is a shielded arrangement for which only the matrix's inner TSV has data transmission; the others are grounded. For the third one, all the TSVs are signal TSVs.

Figure 54 shows the result of transmission parameters of configuration A, B and C. And (d) shows the result of comparison between configuration A, B and C. As we can see, the more TSVs the more signal interferences and the lower transmission parameters.

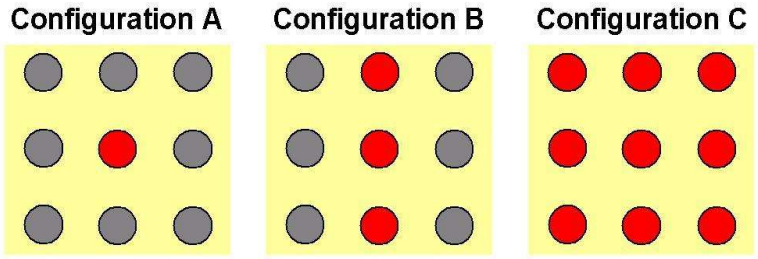


Figure 53 3x3 medium-density TSV matrix configurations for generating Eye Diagrams from simulations. Colour legend: grey for grounded TSV, red for signal. Configuration A: data is only transmitted through the matrix central TSV. Configuration B: shielded configuration. Configuration C: data is sent to all the TSVs.

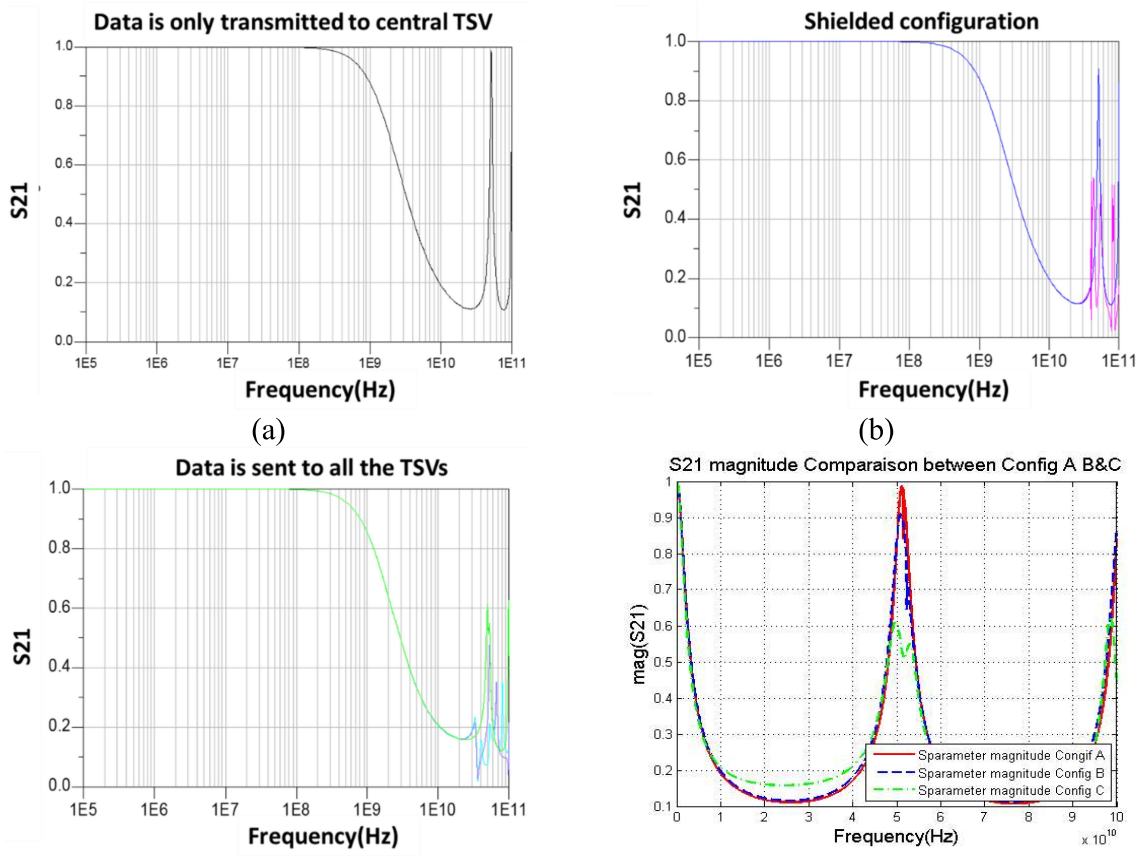


Figure 54 S21 magnitude of (a) configuration A (b) configuration B (c) configuration C (d) Comparison from 10-100 GHz between Configuration A, B&C

The generated Eye Diagrams are presented in Figure 55. When signals are transmitted in a "Source" TSV, crosstalk voltages can be observed on the neighboring "victim" TSV which is at a logic state (configuration A or B). A transmission delay can also be observed if the victim TSV is a signal TSV. The larger the distance between two TSVs, the more the coupling effects can be neglected. The interference due to the inductive coupling effects can be observed clearly in the configuration C.

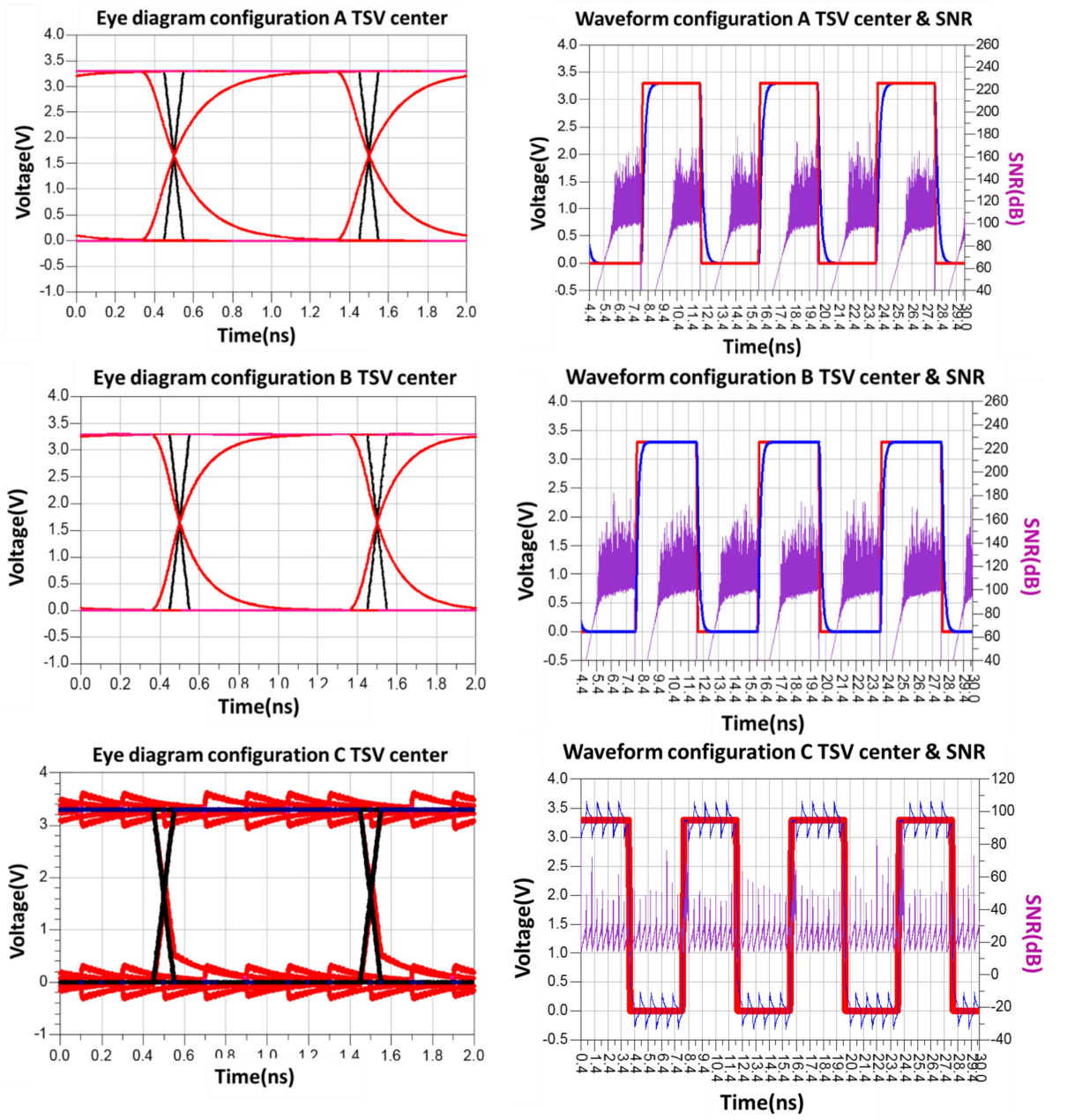


Figure 55 Generating Eye Diagrams from simulation based on the three studied configurations. TOP: A configuration. Middle: B configuration. Bottom: C configuration.

The rise time and propagation delay increase with the increase of the neighbouring signal TSVs number. As a consequence, the eye width is shortened. Compared with configuration A, the rise time in configuration C is 38 % longer. Besides, the voltage crosstalk changes respectively from 65 mV up to 250 mV in the configurations B and C. As the noise margins decrease with technological evolution, signal integrity in TSV matrices must be more fully quantified for cases in which signals propagate in the same direction, as in the presented analyses, or in opposite

directions. The compact model between the substrate and the TSVs should also be considered in the TSVs matrices' electrical models, in order to evaluate the impact of coupling effect to the signal integrity.

The previous results show that the 3D-TLE extractor can be easily integrated with a common EDA software and provide compact models for analyzing the performance of TSVs matrix for high speed data transmission.

2.4) A 26GHz TSV based 3D filter

Portable devices such as cellphones, PCs and so on, are required to be compact, high-speed, and multifunctional; moreover, they can work with a variety of communication standards such as GSM, WCDMA, LTE, GPS, WLAN, Bluetooth, and NFC. In order to solve such communication demands, advanced packaging technique, such as, system-in-package (SiP) and system-on-chip (SoC) technologies are fast developed, because they can miniaturize the communication systems. During the past few years, heterogeneous 3-D IC technique has been rapidly developed and commercialized, in order to simultaneously improve the performance and minimize the whole system size, this advanced packaging technology makes chips design not only in horizontal direction but also in vertical direction by adopting TSVs and interposers. Thanks to heterogeneous 3D IC technology, the packages are getting small and smaller.

However, traditional radio-frequency (RF) passive components, such as, filters, couplers, and antennas, are very difficult to be integrated into packages.

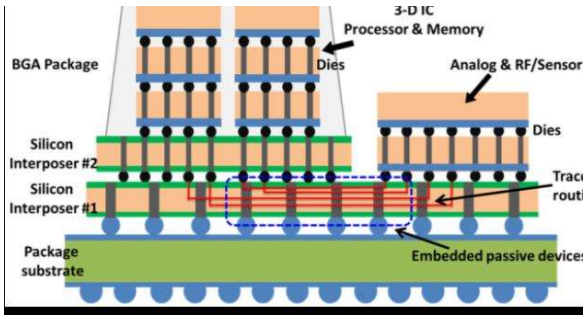


Figure 56 Schematic of heterogeneous 3-D IC technique. [132]

The sizes of RF passive components are usually proportional to several square wavelengths of working frequencies. As a consequence, RF passive components must be put outside packages and designed on PCB; but, as a disadvantage, a lot of PCB areas are taken.

To solve this problem, many researchers have invented advanced RF components by using passive fabrication processes. For example, miniaturized RF filters were designed by using integrated passive device (IPD), low-temperature co-fired ceramics (LTCC), liquid crystal polymer (LCP) processes, and so on [103], [133]–[137]. These techniques can continue minimize the sizes of RF filters, and give better quality factors in comparison to CMOS processes. Once the RF filters can be designed small enough and put into the packages, a huge area can be saved from PCB.

Besides, some RF filters are fabricated by using interposer technology such as silicon interposer and glass interposer [22], [138]–[140], these filters can be easily integrated into heterogeneous 3-D IC circuit as shown in Figure 56. For these filter designs, they can fully profit the 3-D IC technique.

In the following part, a wideband filter based on TSVs is designed. The filter design procedure, simulated results, and discussions are given in this part. Such TSV-based mini-bandpass filters demonstrate the advantages of 3D IC packaging technique.

Traditional coupled-resonator filter is a prospective option in the 3D RF filter design. The proposed filter is based on lumped elements: lumped inductors formed by TSVs' self-inductance and parallel-plate capacitors (TSVs' coupling capacitance). Thanks to the advanced silicon interposer process, the high-density TSV array can have a narrow wire pitch (200 um in our design). By properly designing the TSV in the silicon substrate, we don't need to put 2 capacitances and 2 inductances in the 2D plane and the size of filters can be largely miniaturized. In this part, a TSV-based bandpass filters are generated as examples using TSV parasitic effect. Figure 57 shows the lumped circuit topology of the proposed RF filter by using a single interposer.

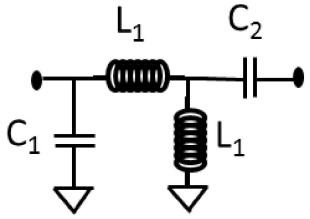


Figure 57 Lumped circuit topology of the single-interposer wideband filter.

Here the π-type filter cell is used, the resonant frequency and bandwidth can be expressed as: [132]

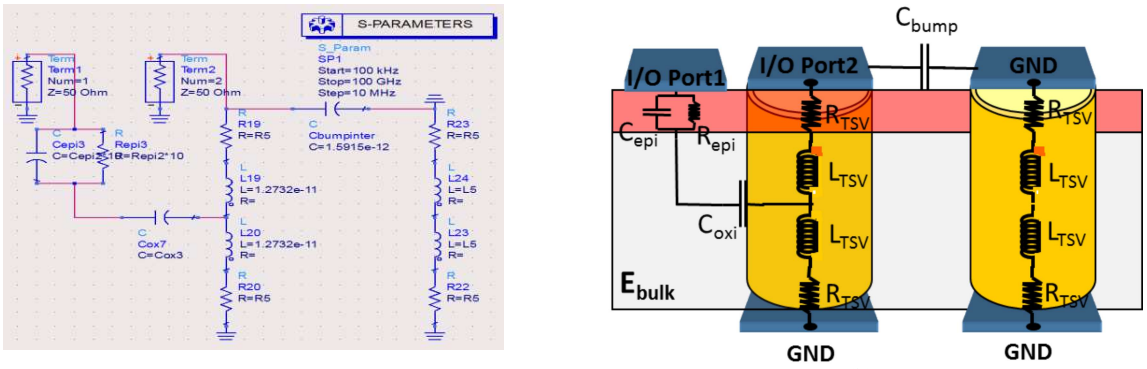
$$f_c = \frac{1}{2\pi\sqrt{2L_1C_1}} \quad (2\text{-}86)$$

$$\text{Bandwidth} = \frac{1}{2\pi R_{ref}C_1} = \frac{4\pi L_1 f_0^2}{R_{ref}} \quad (2\text{-}87)$$

The first step, we define the filter specifications, the coupled capacitances $C_{1/2}$ can be easily determined. But, in order to achieve wideband bandwidth (>20%), large-value capacitances of input/output are needed but that's not practical. To tackle this problem, we use a directly input/output setting as shown in Figure 57.

Once lumped values are chosen, the next step is to transform them to physical layouts. The layout of the proposed RF filter is shown in Figure 58. Inductors of resonators L_1 are the intrinsic inductance of TSV, which can be changed for meeting the design demands by adjusting the TSV's radius. And, the shunt-to-ground capacitor (C_{bump}) is generated by the parallel-cylindrical capacitance, which can be seen from Figure 58.

Through the proposed filter schema shown in Figure 57 and the corresponding circuit, the filter is almost finished. The parasitic effect of TSVs is added by considering the loss caused by the epitaxial layer. The equivalent model of TSV structure contains the resistive loss R_{TSV}, inductive loss L_{TSV}, epitaxial loss R_{epi}, and coupling parasitic capacitance C_{epi} between TSV and pad. And the substrate coupling effects can be neglected if low-loss substrate is used, for example, glass or high-resistivity material.



(a) (b)

Figure 58 Layout arrangement of the proposed single-interposer 25.6GHz/2GHz wideband filter (a) ADS layout (b) Physical Schematic for 2 TSVs model

The proposed TSV-based filter can be easily designed without much extra fabrication process. The single TSV-based silicon interposer filter was designed using commercial simulator (ADS). For the result of TSV-based filter shown in Figure 59, the maximal transmission coefficient ($|S_{21}|$) is 0.8, at the frequency of 25.6 GHz. The filter is very selective. The 20% range of simulated S21 coefficient is from 25 to 27 GHz.

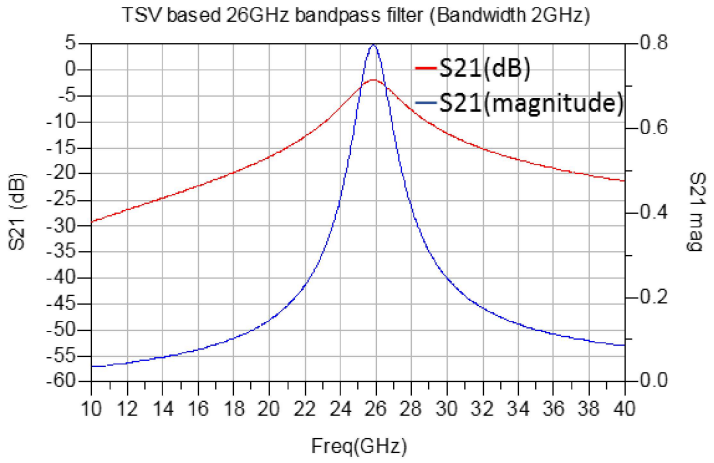


Figure 59 Simulated result of single-interposer bandpass filter (*S*-parameters).

By utilizing the 3D IC technology, we don't need to design the filter in 2D plane and the filter shows very good potential in circuit miniaturization and performance improvement. In all, the proposed TSV based filter can be easily embedded into the interposers, which can be linked to

other components in the 3-D IC packaging technique. So in the future, new RF passive components on 3-D IC, such as compact couplers and antennas, would be an interesting and valuable topic.

2.5) Conclusion

This chapter gives the cylindrical TSV, tapering TSV's electrical analytical model, qualitatively analyzes the taper TSV's parasitic parameters model by considering MOS capacitance effect, eddy current and substrate parasitic effect. Based on MATLAB GUI and according to the parasitic model, a 3D-TLE extractor is generated, which is designed for 3D ICs; the output of this extractor is saved in a SPICE netlist, which is compatible with every SPICE core simulator (ADS). The 3D-TLE extractor is verified by the common Micro-stripe model and 2 TSVs chain model of 3D ICs. For the CPW with substrate model, the 3D-TLE extractor fits well with the measured data, which need a de-embedding process. Reducing the substrate conductivity (reducing the doping concentration), can largely increase the substrate's resistivity, thus highly reduce the attenuation of S12 parameter in high frequency, and improve the transmission performance. For the 2xTSVs chain model, after the comparison with measurements, FEM (COMSOL Multiphysics [141]) verification, we find a good fit beyond 10 GHz. By using this model, we analyze the influence of TSV's parasitic parameters and generate the characteristic curves of five key factors: TSV oxide layer capacitance, depletion capacitance of MOS effect, substrate parasitic resistance, epitaxial layer's resistance, insolation layer's capacitance, and get the five key factor's influence to the high frequency transmission performance. But this study doesn't take backside passivation layer's positive charges into consideration[142]. We also study the transmission performance of TSV matrix in difference transmission mode. Based on the TSV and substrate's parasitic effect, we propose a 26 GHz filter. This chapter provides an important theoretical basis for improving the reliability and flexibility of the 3D ICs.

Further work will be developed, that will encompass accurate M3D (monolithic 3D) model and the co-design of transistors and M3D in nanoscale. The electro-thermal and thermo-mechanical modeling will be the key problem in the future M3D design. And the M3D analytical model should also be integrated in our simulator 3D-TLE. In order to get close to the future neuromorphic chip design, a CMOS based or new analogical/mixed signal M3D transistor should be designed.

Chapter 3: Electro-thermal modeling of 3D circuits

3.1) Introduction

In the past years, a lot of electro-thermal (ET) co-analysis methods have been proposed for IC design. In order to solve the temperature distribution, the heat equation is solved in 2D and 3D. Then, the electrical resistivity of the circuit will change with temperature, and the electrical solution is updated. Such process will be the starting point for updating the heat sources for the thermal issues. The iteration stops when the convergence reaches the fixed accuracy.

The current techniques are normally based on two major systems, depending on how the thermal problem is solved. The first method consists in solving the heat conduction equation, by using FEM, FVM or FDM methods, as shown in the standard multi-physics simulators. It can accurately simulate 3D geometries and/or add also other phenomena like micro-heat pipe cooling effects [143], with a very high computational cost. For the second one, the thermal problem is solved by using an equivalent circuit model, so both the thermal circuits can be simulated by using the electrical solver, like the SPICE-like ones (ADS). This method can largely reduce the computational cost, and handle strongly coupled high speed electro-thermal problems. Many of the ET methods have focused on the chip or PCB study using PDN analysis, but less on the device level design.[94], [95], [98], [101], [104], [143]–[146]. PDNs should be analyzed by considering different parts such as CPW, vias, C4 bumps, etc. Consequently, even though each simple models can be simplified as a single node, but the size of the total equivalent network for PDNs can easily overpass several millions nodes [113]–[125]. Hence, the major challenge to ET simulations of PDNs is how to reduce the computational cost. The traditional model reduction technique are more suitable for systems with a large number of poles, however, a PDN is usually composed of a huge number of nodes, which have a low number of poles. Therefore, the model reduction for PDN is not so obvious [56]. Recently, new reduction methods have been studied only for electrical networks, based on the concept of node reduction [100][157][158]. Once the reduction methods are suitable for the electrical and thermal study, the reduction strategies can be directly used, with a predefined accuracy, and reduce the network size [138]–[140].

This chapter will emphatically introduce the electro-thermal modeling method for substrate, 3D circuits and multi-cores system. In order to give a brief introduction to these phenomena, some simple models are presented here. we use the solving method in TSV level simulation (Modified Nodal Analysis method). The power distribution network will be a very interesting topic in future studies, but here in the thesis, we just use the simulation method. We interest only in the low voltage study.

3.2) Electro-thermal modeling of substrate

Substrate noise coupling in integrated circuits becomes a significant consideration in the circuit design. Nowadays, micro (nano) technology and the development of semiconductor technology enable designers to integrate multiple systems into a single chip, not only in 2-D (planar) but also in 3-D (in the bulk). This design technology reduces cost, while improving performance, and makes the possibility of a system to be on chip [162][163][13][164].

3-D Si integration seems to be the right way to go and compete with Moore's law (more than Moore versus more Moore). However, it is still a long way to go. In 2010, the question was why 3-D. Today, the questions are when and how is 3-D used. The 3-D chip stacking is well known to overcome conventional 2-D IC issues, using in-depth contacts or some through silicon for signal transmission.

The kind of silicon substrate in which 3-D interconnections are processed is an important parameter and has a strong impact on 3-D interconnection electrical behavior [164]. Electrical modeling methods are dependent on the substrate type of the application. Two different kinds of p silicon substrates are typically used in CMOS/BiCMOS processes: uniform lightly doped substrate (>1 Ω · cm) and heavily doped substrate (<1 Ω · cm) with lightly thinned doped (>1 Ω · cm) epitaxial layer. Other semiconductor substrates are used in micro/nanotechnologies and could embed 3-D interconnections (silicon on insulator technologies, microelectromechanical systems technologies, sensor technologies, etc.).

Indeed, we attempt to propose an analysis of dynamic electro-thermal phenomenon studies in 3-D layered circuits.

First of all, we solve Poisson's equation, using Green kernels [165][166][167][168][169] [170]. Here we show that this mathematical method is an analog to the transmission line matrix (TLM), based on reflection transmission of voltage and current through the layers, when adopting it to embedded contacts of any shape. Then, we work on the resolution of the unsteady 3-D heat equation that has been shown; during this, we use the algorithms developed for the electrical modeling, particularly when using the spreading impedance concept. Finally, we show that these electrical and thermal spreading impedances can be considered entangled. This approach drives us to start an attempt to model the more general problem of noise in 3-D ICs, using again, a transfer impedance paradigm.

3.2.1) Brief introduction of mathematical tools

In this part, Green functions are applied to homogeneous stacked layers for substrate circuit model extraction, as opposed to numerical methods; the resolution speed of the former method is much faster. Some basic recalls and concepts are first introduced. The use of discrete cosine transforms (DCTs), applying twice as fast a Fourier transform (FFT) in this model, will accelerate

and compute the speed. Then, an improved model, which can be applied on substrate with in-depth contacts (or via), is shown; it can treat the case of contacts lying in different layers. For verification, a finite element method is compared (FEM) [171].

3.2.1.1) Green Kernels

The high density integration and high system frequency make substrate noise coupling become one of the most significant considerations in the design due to its great impact on the performance of ICs. The aim of this 3D substrate analysis is, first of all, to efficiently extract the Z impedance parameters between any contacts (electrode and via) that are located on or into the silicon substrate. An efficient impedance extraction tool, for any two contacts, could help the designer to accelerate the design and optimize the final layout. Like in planar technologies, 3D interconnects can be built as a resistance, inductance, capacitance, and conductance (RLCG) equivalent electrical model, with a Π or a T network. Generally, a simple compact model is constructed by modeling the substrate as a simple node. However, this assumption is only viable when substrate is highly conductive, in low and medium frequency domains, and is not suitable for the multilayer substrates. That is the reason why, in this thesis, we propose a substrate extraction method relying on TLM method over multilayered substrate and/or Green functions to model these effects, in the bulk [166][167][168][169].

3.2.1.2) Substrate Analysis

The most well-known pioneering paper came from ref [163]: a layered 3-D substrate, with two surface contacts.

We present hereafter a 3-D substrate study with top or embedded contacts. The originality as we consider and apply here is to do all the calculations in the reciprocal domain, from the very beginning of the calculations to the end, to extract voltage or temperature.

In general, the Z parameters could be defined as [172], [173]

$$Z_{mn} = \frac{V_m}{I_n} | I_{k \neq n} \tag{3-1}$$

In practical operation, by injecting a unitary current as an excitation source, I at the n^{th} point, and a unitary current excitation source, -I (equivalent to a sink current I) at an m^{th} point and calculating the resulting voltage at the probe point, we can get the direct impedance Z_{mn} between the m and n contacts.

If we can get the resulting potential distribution in the substrate caused by the unitary current, we could easily get the Z parameters by (3-1).Under quasi-static conditions, the potential over the substrate satisfies Laplace's equation:

$$\nabla^2 \varphi(x, y, z) = 0 \tag{3-2}$$

It can also be written as:

$$\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}+\frac{\partial^2}{\partial z^2}\right)\varphi(x,y,z)=0 \quad (3\text{-}3)$$

Hereafter, for Poisson or heat diffusion equations, the analytical method is, first of all, based on the algorithm of variable separation, leading to solve an Eigen problem.

When assuming that φ=X(x, x') ▪ Y (y, y') ▪ Z(z, z'); (3-3) can be rewritten by defining [172], [173]

$$Z(z,z')=Z'(z,z')\cdot\cos\left(\frac{m\cdot\pi\cdot x'}{a}\right)\cdot\cos\left(\frac{n\cdot\pi\cdot y'}{b}\right) \quad (3\text{-}4)$$

And we get, for a potential due to a point charge, a simple equation [172], [173]

$$\frac{ab}{4}\cdot\left[\frac{d^2Z}{dz^2}-{\gamma_{mn}}^2\cdot Z\right]=-\frac{\delta(z-z')}{\varepsilon_N}\ \text{with}\ \gamma_{mn}=\sqrt{\left(\frac{m\cdot\pi}{a}\right)^2+\left(\frac{n\cdot\pi}{b}\right)^2} \quad (3\text{-}5)$$

For $z \neq z'$, $\delta(z-z') = 0$. The above equation, has a well-known general solution:

$$Z'=A\cdot e^{-\gamma_{mn}\cdot(d+z)}+B\cdot e^{\gamma_{mn}\cdot(d+z)} \quad (3\text{-}6)$$

This equation also invokes a transmitted wave and a reflected one.

For instance, for the case that both the point charge and the point of observation are in the same dielectric layer, on the surface with z = z' = 0, the Green function then changes to [172], [173]

$$\emptyset(x,y;x',y')_{z=z'=0}\,(G_0)_{z=z'=0}=\left(\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}f_{mn}C_{mn}\cos\left(\frac{m\pi x}{a}\right)\cos\left(\frac{m\pi x'}{a}\right)\cos\left(\frac{n\pi y}{b}\right)\cos\left(\frac{n\pi y'}{b}\right)\right) \quad (3\text{-}7)$$

Where C_{mn}= 0 for (m=n=0), C_{mn}=2 for m=0 or n=0 but m ≠ n and C_{mn}= 4 for all other m and n (m>0 and n>0).

The function f_{mn} is given by: [172], [173]

$$f_{mn}=\frac{1}{ab\gamma\varepsilon_N}\frac{\beta_N\tanh(\gamma_{mn}d)+\Gamma_N}{\beta_N+\Gamma_N\tanh(\gamma_{mn}d)} \quad (3\text{-}8)$$

β_N and Γ_N can be computed recursively from: [172], [173]

$$\begin{bmatrix}\beta_k\\ \Gamma_k\end{bmatrix}=\frac{1}{2}\cdot\begin{bmatrix}1+\frac{\varepsilon_{k-1}}{\varepsilon_k} & (1-\frac{\varepsilon_{k-1}}{\varepsilon_k})e^{2\theta_k}\\ (1-\frac{\varepsilon_{k-1}}{\varepsilon_k})e^{-2\theta_k} & 1+\frac{\varepsilon_{k-1}}{\varepsilon_k}\end{bmatrix}\times\begin{bmatrix}\beta_{k-1}\\ \Gamma_{k-1}\end{bmatrix} \quad (3\text{-}9)$$

Where $$\theta_k=\gamma_{mn}(d-d_k),\beta_0=1,\Gamma_0=1 \quad (3\text{-}10)$$

Then, after the derivation of some formal mathematical solutions from Poisson's equation, with boundary conditions, we will depict hereafter a more physical (and graspable) approach of the problem, using a TLM method, with some brief recalls. Note that, in our whole algorithm, from its beginning, we work on the reciprocal space. More precisely, for instance, it means that we also take the Fourier transform of the injected currents on the discretized contacts.

In practice, then, we can choose any shape for these embedded contacts, whereas, in all the few others works, to the best of our knowledge, all the contacts are rectangular, the integration over them being done in the real space. This last point seems to be crucial to us, and we should work with through silicon vias (TSVs) (cylindrical, tronconic, etc.) in our 3-D circuits.

After a bi-dimensional spatial Fourier transform in the x and y directions, (3-3) should be

$$\frac{\partial^2 \Phi}{\partial z^2} - k_x^2 \Phi - k_y^2 \Phi = 0 \tag{3-11}$$

Where Φ is the spatial-frequency domain potential and k_x, k_y are the spatial-frequency variables (m^{-1}).

Since the current density $J_Z = \sigma^* E_Z$ (σ* is the complex conductivity) and $E_Z = -\frac{\partial \varphi}{\partial z}$, we can write

$$J_z = -\sigma^* \frac{\partial \varphi}{\partial z} \tag{3-12}$$

In the spatial frequency domain, it changes to [172], [173]

$$J_z(k_x, k_y, z) = -(\sigma + j\omega\varepsilon) \frac{\partial \varphi(k_x, k_y, z)}{\partial z} \tag{3-13}$$

After derivative calculations of the above equation, we obtain [172], [173]

$$\begin{cases} \frac{\partial \varphi}{\partial z} = -\frac{J_z}{(\sigma + j\omega\varepsilon)} \\ \frac{\partial J_z}{\partial z} = -(\sigma + j\omega\varepsilon)(k_x^2 + k_y^2)\Phi \end{cases} \tag{3-14}$$

These equations indicate the relationship between current density in the z-direction and the potential distribution in the spatial frequency domain.

3.2.1.3) Transmission Line Analogy for Multilayered Media

In its simplest form, a transmission line is a pair of conductors linking together two electrical systems (source and load, for instance), with forward and return paths; for cases where the return path is floating, a third conductor (or more) is introduced as the grounding shield. For microwaves, they are waveguides. In our case, the propagation of EM waves and their interferences, through the silicon substrate, is among the most serious obstacles in the steady trend toward integration of the present day microelectronics. In fact, the TLM method has been established in some cases concerning substrate surfaces; TLM can be seen as a more physical interpretation of the mathematical developments presented above.

The principal strength of this method seems to be well dedicated to embedded contacts, irrespective of their number and shape.

Let us consider a plane wave through a multilayered medium, its plane of incidence being parallel to the <x, y> plane, providing the same boundary conditions as mentioned above.

Then, we consider the general case in which the line's impedance is not the same as that of the load. A wave-front A hits the load Z_L: a part of energy is absorbed by Z_L, and the remaining energy is reflected; in this case, voltage and current wave-fronts are not in phase. This reflected wave can meet another incident wave-front B.

The direction of the current flow depends on the polarity of the waveform at the time of observation; if two positive directed waveforms (one forward and one reflected) meet, the current waveforms subtract, but the voltage waveforms add. Likewise, if a positive directed waveform meets a negative directed waveform, the current will add and the voltage will subtract.

The expression for the apparent impedance is given as follows: [172], [173]

$$Z = \frac{V_{total}}{i_{t\,otal}} = \frac{V_F \pm V_R}{i_F \mp i_R} \tag{3-15}$$

Then, the general solution for voltage and current is [172], [173]

$$V(z) = V_f e^{\gamma z} + V_r e^{-\gamma z} \tag{3-16}$$

$$I(z) = Y_c(V_F e^{-\gamma z} - V_r e^{\gamma z}) \tag{3-16}$$

Where the propagation coefficient γ is the square root of the product Z by Y, the linear impedance and admittance, respectively,

$$\gamma = \alpha + j\beta; \alpha: \text{attenuation}, \beta = 360°/\lambda_{si}$$

Directly deriving from the chain matrix [172], [173]

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} cosh\,\gamma L & Z_c\,sinh\,\gamma L \\ Y_c\,sinh\,\gamma L & cosh\,\gamma L \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{3-17}$$

And from the output branch $V_2 = -Z_L I_2$, we get:

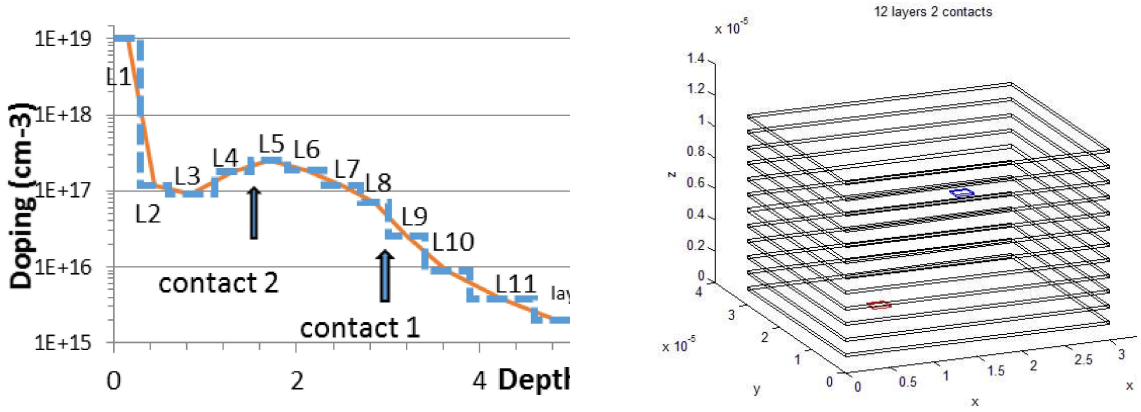
$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = -I_2 \begin{bmatrix} Z_L\,cosh\,\gamma L & Z_c\,sinh\,\gamma L \\ Z_L Y_c\,sinh\,\gamma L & cosh\,\gamma L \end{bmatrix} \begin{bmatrix} 1 \\ 1 \end{bmatrix} \tag{3-17}$$

Where $Zc = 1/Yc$ (square root of Z and Y ratio) is the characteristic impedance (electric and magnetic fields' modulus ratio), Z_L is the charge impedance, and L is the distance from the load. We can extract an input impedance, Z_l ($=V_l/I_l$), function of the load impedance Z_l+1 (l: layer number), as [172], [173]

$$Z_l = Z_c \frac{Z_{l+1} + Z_c\,tanh\,\gamma L}{Z_c + Z_{l+1}\,tanh\,\gamma L} \tag{3-18}$$

This well-known (TLM) equation Z_l is directly related to (3-8), where $Zc = \beta_N$ and $Z_L = \Gamma_N$ [165].

In fact, restarting from (3-7) and taking into account the limit or boundary conditions—continuity of potential and discontinuity of the electric field if there is a surface charge at the considered layer interface—it is easy to program this iterative solution against substrate depth, or the layers of (3-7). In fact, these calculations are made only one time, at each frequency.



(a) (b)

Figure 60 (a) Specific depth profile of a 35-µm technology (p+/p-region), (b) 3-D schematics of the structure

In our simulator, using MATLAB [174], we use a matric formalism, extending the impedance (Z) and the current (T) transmission from a layer l to its adjacent one [see (3-9) or (3-17)], starting from a k layer

$$\begin{bmatrix} Z_{k,l+1} \\ T_{k,l+1} \end{bmatrix} = \begin{bmatrix} A_k & -B_k \\ C_k & -D_k \end{bmatrix} \begin{bmatrix} Z_{k,l} \\ T_{k,,l} \end{bmatrix} \tag{3-19}$$

Where T addresses the derivation of the current (between two parallel regions).

Based on the transmission line method, a substrate extractor is programmed, shown in the following Figure 61.

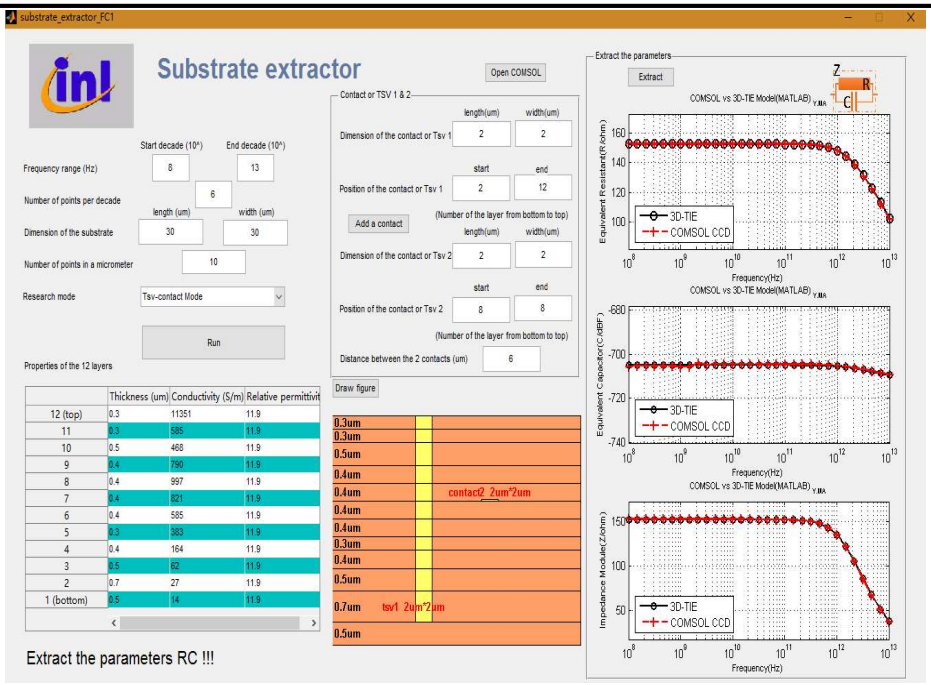


Figure 61 3D TLE substrate extractor, example: Impedance Z_{17}, capacitance and resistance C_{17} and R_{17} extracted between one contact and one TSV (valid for frequency lower than 20GHz and of quasi-static assumption)

The *ABCD* parameters are variously known as chain, cascade, or transmission line parameters. This cascade connection model is very suitable.

As mentioned earlier, all the calculations are done in the reciprocal space. For instance, the potential is derived from the (Kronecker) product of (sub) matrix *Z*, by a *DCT* of the matrix of the injected current, accomplished using two consecutive FFTs. In our algorithm, the contact voltage is the mean value of the voltage of the discrete contact elements, calculated via Millman's theorem, as [172], [173]

$$v = \frac{\sum_{n=1}^{N} j\omega c\varphi_n}{\sum_{n=1}^{N} j\omega c} = \frac{1}{N}\sum_{n=1}^{N} \varphi_n \qquad (3\text{-}20)$$

Where φ_n the substrate voltage at a node and N is the number of contact sub-areas. Therefore, in our modified algorithm, the contact voltage is then calculated by taking the average <Va> of the potentials of the substrate region, under the injecting contact.

3.2.2)Simulation Results by using Green/TLM

In this work, as a check, a typical process flow compatible Bi-CMOS 0.35µm technology is first considered. In Figure 60(a), a specific region (p+/p) of this process is presented.[170][80]

We approximate the actual profile by stacked layers of given thicknesses uniformly doped as shown in Figure 60(b).

First of all, we did some numerical experiences (not presented here) using COMSOL [171], a well-known Multiphysics (electrical, thermal, and mechanical couplings) simulator, for testing its robustness and accuracy. It is also a dedicated tool for full-wave electromagnetic analysis. It essentially uses Galerkin-like algorithms; typically, a 3-D simulation can use a few ten of minutes or more than 1h. Figure 62 shows the general algorithm of substrate impedance extraction. Figure 63 shows the extracted voltage and impedance.

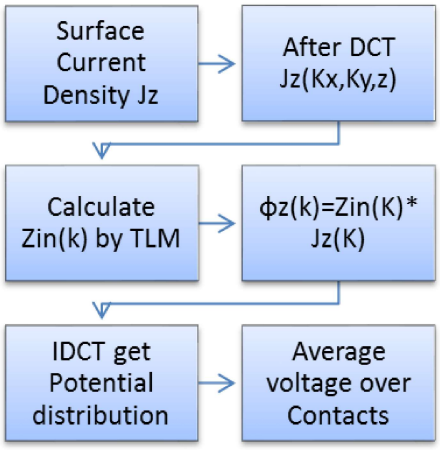
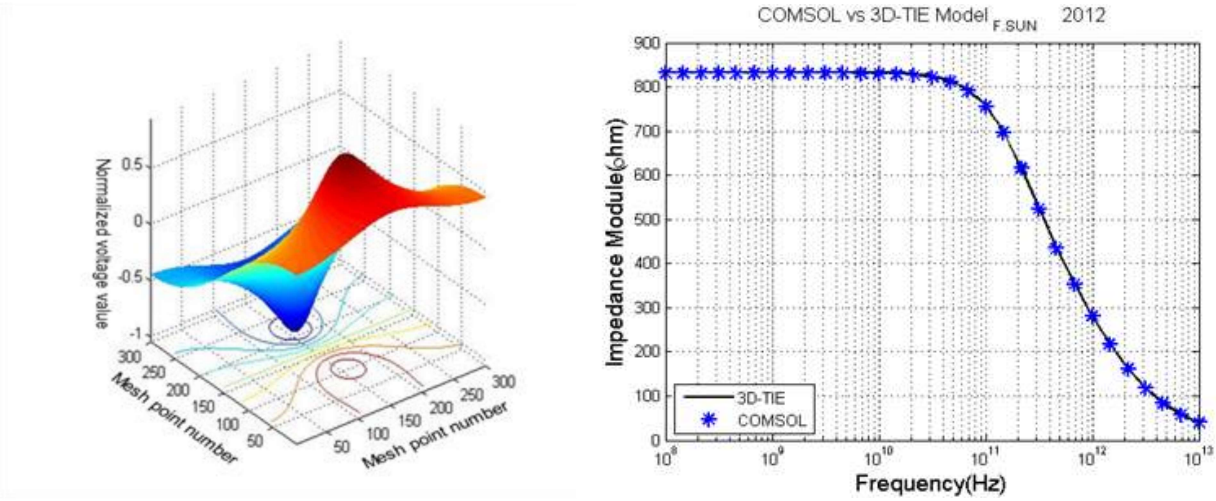


Figure 62 General steps of 3D-TLE algorithm



(a) (b)

Figure 63 (a) Voltage map (layer interfaces: L3/L4). (b) Impedance module of Figure 60 (b)

3.2.2.1) Contacts Embedded

Considering the general case where the contacts (previous works exist for surface contacts [163]), real or virtual, are totally embedded in Figure 60. Then, the substrate can be seen as an

actual parallel connection of two separated parts (current derivation). The current is injected on a contact of an i^{th} layer, so the substrate is divided in two parts, from this layer.

We write a synoptic model algorithm, all developed in the reciprocal spaces in Figure 62.

Now, it seems to be easy to calculate any transfer impedance by TLM. Possibly embedded in the substrate, contacts can be introduced into any layer; they can be real (e.g., metal like) or virtual, of any shape.

The surface die is typically 30 µm X 30 µm, with M = N = 300; surface contact: 20 by 20 points (the calculation points, M X N, are equidistributed).

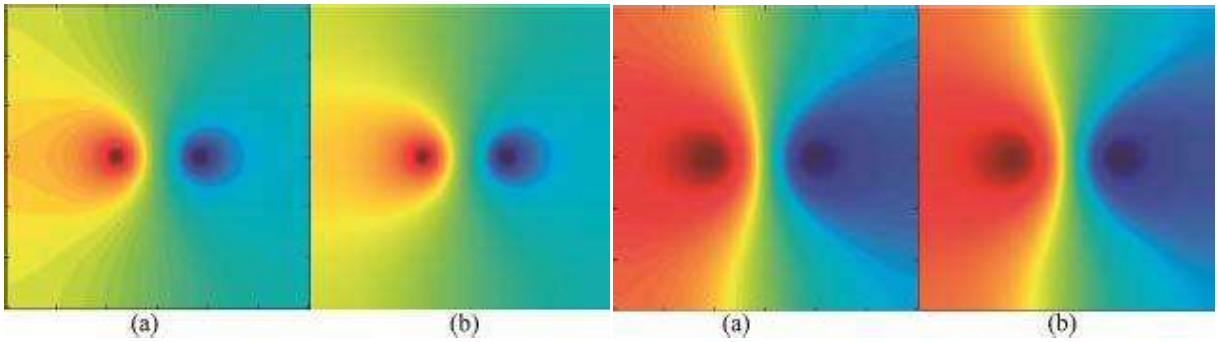


Figure 64 Frequency=100 GHz. (1) Left: top surface potential from 3D-TLE (a) and COMSOL (b) for 12 layers substrate, (2) Right - contacts embedded in layer 4 and layer 8 (see Figure 60).

We present in Figure 63(a) and (b) the voltage map and the impedance module, respectively, between some *Ci* and *Cj* contacts, at the interfaces L3/L4 and L7/L8. It is typical of a Lorentzian curve (R//C, with $R \cdot C = \rho\varepsilon$). The comparison between TLM/Green and COMSOL is quite good. Moreover, in Figure 63, surface potentials, from our 3-D transmission line extractor (TLE) simulator Figure 64(a) and COMSOL Figure 64(b) for a 12-layer substrate, at a frequency of 100 GHz, are quite similar. Still, a very good accordance was shown between FEM and TLM. Since calculations are made with current source, we get voltage variation under contacts.

From the above results, one can find that the comparison between TLM/Green and COMSOL is quite good. The proposal method's calculated results agree well with the COMSOL simulation ones, while our method uses comparatively less time (roughly 1/50–1/100).

Regarding the top surface potential distribution of the two-contact model in Figure 64, one can find that the potential on the contact surface is not uniform (high-voltage region). The non-uniform potential is caused by an injection of uniform current density instead of a uniform voltage. This non-uniform potential feature makes 3D-TLE very profitable when one calculates the impedance of two resistive regions rather than two metal contacts, for example, the oxide-insulated conductive regions (e.g., pads and coplanar waveguide) and junction insulated well regions (e.g., n-well regions over a p-type substrate). In these cases, the substrate plates could not be considered as an equipotential plate.

The simulation results obtained with Green/TLM implemented in MATLAB and compared with COMSOL are found to be practically equal. Indeed, we choose, in MATLAB, layers as perfect parallelepipeds (uniform thickness layers).

We are quite aware that the quasi-electrostatic modeling framework cannot work so perfectly up to 10 THz (versus experiments), which implies a wavelength of roughly tens of micrometers in Si. This wavelength is of the ten orders small compared to the contact-to-contact distance (3μm) used; in this work we use quasi-static assumption, not the full wave Maxwell equations.

Figure 60 shows the frequency to 10 THz, because we want to find out how to simulate parasitic effects at very high frequency, the typical RC model still works for substrate in our case with validation of FEM results, but which are no longer valid in a physical point of view; we should use a full wave method for the very high frequency (>10GHz). But it's still a way to compare FEM method (COMSOL) and our calculations. Moreover, for TSV cases, we should be more careful, we want to establish a valid compact model for frequency >10GHz, so that's why we do the optimization for TSV compact model, because at high frequency (>10GHz), if we keep the same RLCG model, by adjusting their values, we can still fit with the measurement data (c.f 2.3.2), up to 10GHz.

Currently, we did not explicitly take into account the permeability; it is not realistic to go beyond 20 GHz in this analysis (that is not so bad); but we think that it was interesting to compare the FEM in order to test the robustness of our algorithm.

3.2.2.2) Alteration of the Contacts' Shape and Their Number

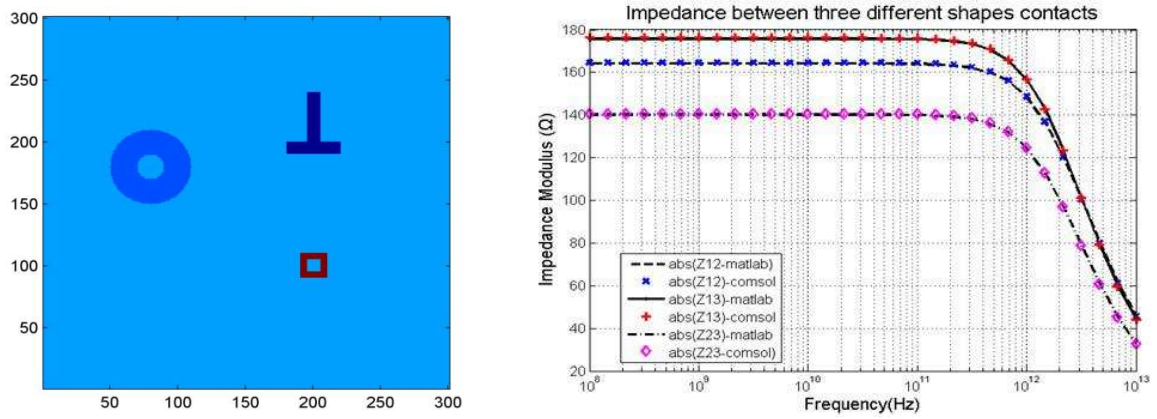
Unlike the pioneered method, based on Green's functions [163] that calculates only for rectangular contacts, our method can be used for any contact shape: circle, concentric circles, rectangle, loop, T-shape, etc. Figure 65 shows some examples from our 3-D TLE simulator. We test it by comparing with the results from COMSOL.

First, we apply our model, with three different contacts in Figure 65(a).

All the three contacts are on the top surface of the substrate. The square contact is contact 1, the T-shape contact is contact 2, and the circle one is contact 3.

The impedance modules between these three contacts, calculated from 3D-TLE and COMSOL, are shown together in Figure 65 (b), in which Z_{12} at the top is the impedance between contacts 1 and 2, the rest being of a similar manner.

We can see that these results, from the proposed methods, agree very well with the results calculated from COMSOL.



(a) (b)

Figure 65 (a) Some different shapes of contacts, which can be apprehended by 3D TLE (b) Impedances' comparison with COMSOL

3.2.3)Heat equation

A problem commonly encountered in the thermal analysis of electronic packages, or in 3-D ICs, is that of thermal spreading resistance. Thermal spreading resistance occurs as heat flows by conduction between a source and a sink with different cross-sectional areas. One example is that of a multilayer chip. Another one is that of a module package with a thermal grease path between a chip and the module cap. In either case, heat flows from the chip across a given area into the substrate or cap and spreads out to leave across another area. We are, here, in the case of (un)steady temperature due to one or multiple heat sources, using in this last case the principle of superposition. A thermal spreading resistance (still in the reciprocal domain) can be extracted from discrete heat source. Typical applications are cooling of device areas, at the package and at die level.[118], [172]

We consider 3-D transient heat conduction in a non-homogenous finite medium [175][70] [176][177].

We can write the heat equation as follows:[172], [173]

$$\frac{d^2T}{dx^2}+\frac{d^2T}{dy^2}+\frac{d^2T}{dz^2}-\frac{1}{\alpha}\frac{dT}{dt}=0 \qquad (3\text{-}21)$$

Where $\alpha = k/\rho c$ is the thermal diffusivity, k is is the effective isotropic thermal conductivity, and c is the isobar mass heat. For the steady state, the heat equation is resumed to the Laplace equation, similar to Poisson's equation when no electric charge is present.

As it can be seen, we get analogies with (3-2)-(3-8).

In the same way that for Poisson's equation, we extract an associated Green kernel, i.e., if we assume T = X(x, x') ▪ Y (y, y') ▪ Z(z, z')τ (t, t'), we can extend (3-21), thus resulting in

$$\frac{1}{X}\cdot\frac{d^2X}{dx^2}+\frac{1}{Y}\cdot\frac{d^2Y}{dy^2}+\frac{1}{Z}\cdot\frac{d^2Z}{dz^2}=-A^2\,\frac{\delta(x-x\prime)\cdot\delta(y-y\prime)\cdot\delta(z-z\prime)\cdot\delta(t-t\prime)}{\alpha} \quad (3\text{-}22)$$

Then [172], [173]

$$\frac{d^2X}{dx^2}+\lambda^2X=\frac{d^2Y}{dy^2}+\mu^2Y=\frac{d^2Z}{dz^2}-\gamma^2Z=\frac{d\tau}{dt}-\alpha(\lambda^2+\mu^2-\gamma^2)\,\tau=0 \quad (3\text{-}23)$$

Where λ, μ, and γ are the eigenvalues associated with the Green kernel of this heat equation with [172], [173]

$$\lambda^2+\mu^2-\gamma^2+\frac{A^2}{\alpha}=0 \quad (3\text{-}24)$$

The last equation in (3-23) has an evanescent solution versus time; for an ith layer, we can write

$$\tau_i=\tau_{i0}\cdot\exp(-(\lambda_{ix}^2+\mu_{iy}^2-\gamma_{iz}^2)\cdot\alpha\cdot t \quad (3\text{-}25)$$

Staying static in the reciprocal domain (so, we can also take advantage of the data compression, inherent to the DCT), equation (3-21) becomes [172], [173]

$$\frac{d^2X}{dx^2}+\frac{d^2Y}{dy^2}+\frac{d^2Z}{dz^2}-\frac{1}{\tau}\cdot\frac{d\tau}{dt}=-\lambda^2X-\mu^2Y+\gamma^2Z-\left(\frac{j}{\alpha}\right)\omega\tau=0\;(j^2=-1) \quad (3\text{-}26)$$

We can define a Fourier coefficients' spreading (transcendental) impedance function as the following ratio: [172], [173]

$$R_{FCSi}=A_i/B_i \quad (3\text{-}27)$$

Where A_i and B_i are the Fourier coefficients of the general ith solution for the temperature, in the z-direction perpendicular to the stacked layers

$$FCS_i=A_i\cdot\cosh(\gamma z)+B_i\cdot\sinh(\gamma z) \quad (3\text{-}28)$$

Boundary Conditions

The continuity of the thermal conductivity at interface layers leads to

$$k_i\;\frac{dT_i}{dz_i}=k_{i+1}\frac{dT_{i+1}}{dz_{i+1}}\;(Neumann\;condition) \quad (3\text{-}29)$$

We have also at interface

$$X_i(t)=X_{i+1}(t),Y_i(t)=Y_{i+1}(t)\;(Dirichlet\;condition) \quad (3\text{-}30)$$

$$k_i\;\frac{T_{i,z}}{T_{i+1,z}}=k_{i+1}\frac{R_{FCDS_{i,z}}}{R_{FCDS_{i+1,z}}} \quad (3\text{-}31)$$

See the analogy with the induction vector; at an interface without charge, we have

$$\varepsilon_iE_i=\varepsilon_{i+1}E_{i+1}\;(E:Electrical\;field) \quad (3\text{-}32)$$

If (3-29) and (3-30) are verified, it follows: [172], [173]

$$R_{FCS_{i,z}} \cdot Y_{i(y)} \cdot e^{-(-\gamma^2_{i,z} + \mu^2_{i,y} + \lambda^2_{i,x})t} = -B_{i,z} \cdot R_{FCS_{i+1,z}} \cdot Y_{i+1(y)} \cdot e^{-(-\gamma^2_{i+1,z} + \mu^2_{i+1,y} + \lambda^2_{i+1,x})t} \quad (3\text{-}33)$$

$$k_{i,z} \cdot R_{FCS_{i,z}} \cdot Y_{i(y)} \cdot e^{-(-\gamma^2_{i,z} + \mu^2_{i,y} + \lambda^2_{i,x})t} = -k_{i+1,z} \cdot B_{i+1,z} \cdot \gamma\lambda R_{FCS_{i+1,z}} \cdot Y_{i+1(y)} \cdot e^{-(-\gamma^2_{i+1,z} + \mu^2_{i+1,y} + \lambda^2_{i+1,x})t} \quad (3\text{-}34)$$

We have the same set (3-33) and (3-34), replacing Y by X. Moreover, (3-33) and (3-34) are verified if [172], [173]

$$\frac{B_{i,z}}{B_{i+1,z}} = \frac{R_{FCS_{i+1,z}}}{R_{FCS_{i,z}}} \quad (3\text{-}35)$$

$$\frac{k_{i,z}}{k_{i+1,z}} = \frac{R_{FCS_{i,z}}}{R_{FCS_{i+1,z}}} \quad (3\text{-}36)$$

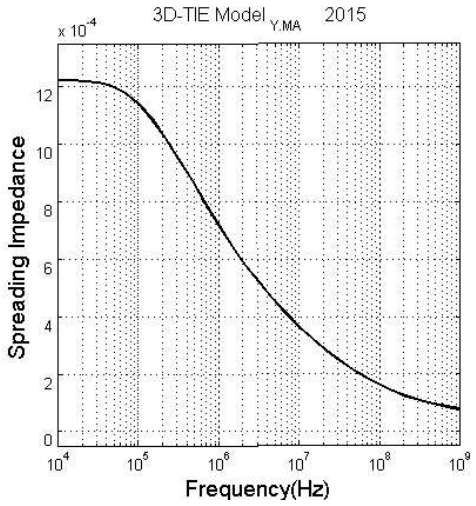


Figure 66 Temperature Fourier coefficients' spreading impedance

Note that for different thermal diffusivities or conductivities, in each layer, but with $k_{x,i} = k_{y,i}$ (see isotropy) [172], [173]

$$\gamma_{i+1,z} = \left[\frac{\alpha_i}{\alpha_{i+1}} \cdot \gamma^2_{i,z} + \left(\frac{\alpha_i}{\alpha_{i+1}} - 1\right) \cdot (\lambda^2_{i,x} + \mu^2_{i,y})\right]^{\frac{1}{2}} \quad (3\text{-}37)$$

We obtain [172], [173]

$$A_{iz} = B_{iz} \cdot R_{FCDS_{i,z}} \cdot (\gamma_{i,z}) \quad (3\text{-}38)$$

$$R_{FCS_{i,z}}(\gamma_n) = \frac{k_{i+1} R_{FCS_{i+1,z}}(\gamma_n) + k_i \cdot tanh(\gamma_{i,z} \cdot t_i)}{k_i \cdot R_{FCS_{i+1,z}}(\gamma_n) \cdot tanh(\gamma_{i,z} \cdot t_i)} \quad (3\text{-}39)$$

Here, γ_n refers to the eigenvalue in (3-24); t_i is the thickness of the i[th] layer.

The above development seems to be important because it does not have the classic form of previous works, especially in this thermal area. Furthermore, we get a shape analogous to the thermal impedance (3-39) and the recursive electrical impedance specific to the TLM method [see

(3-18)] also produced by Green kernels [see (3-8)]. Moreover, to the best of our knowledge, this triple analogy, working in the reciprocal field, is innovative.

The impedance associated with the Fourier coefficient ratio of temperature solution is presented in Figure 65. Using this low-pass filter, tuning a maximum frequency should permit us, for instance, to scrutinize the thermal flow behavior across each interface layer, for a frequency range domain. In addition, taking inverse Fourier transforms, we could compare the direct calculation of time-dependent heat profile (see FEM).

Finally, in general, the real solution of (3-21) takes the following expression:

$$\Delta T\,(x,y,x',y',z,z') = T - T_\infty = T_0 \cdot exp\left(-\left(\lambda_{i,x}^{2} + \mu_{i,y}^{2} - \gamma_{i,z}^{2}\right)\cdot\alpha\cdot t\right)\cdot \sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\left[\frac{2\left(A_N e^{-\gamma_{mn}(d+Z_l)} + B_N e^{\gamma_{mn}(d+Z_l)}\right)\left(e^{-\gamma_{mn}Z_h} + e^{\gamma_{mn}Z_h}\right)}{ab_N\gamma_{mn}\left(B_N e^{d} - A_N e^{-d}\right)}\right] cos\left(\frac{mx}{a}\right) cos\left(\frac{ny}{b}\right) \quad (3\text{-}40)$$

Where T_∞ is the stationary temperature.

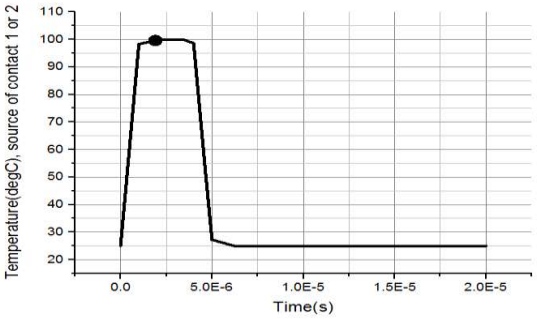
We built our simulator in order to make an efficient use of the analogies between, first of all, electrical and thermal models. In particular, if all the relevant variables' calculation (voltages/temperature, current density/thermal flow, noise power/current fluctuations) made in the reciprocal domains of space and frequency is done in the main program, we do develop a single special subroutine to calculate the impedance (electrical or thermal, or transfer impedances) [see hereafter] for noise extraction (between any two points into the bulk). Typically, we take 300 points X 300 points, and 12 layers [see the rectangle in Figure 61 and Figure 62: Zin(*k*) by TLM]. The first results are presented for temperature coming both from FEM algorithm and from our method, where the temperature source profile, applied to one or both the contacts, is depicted in Figure 66(a) and the temperature map in Figure 66(b) (FEM results (left) and Green's results (right)). We will go further, particularly with numerical experiences, to consolidate our algorithms.

We think these modellings can be efficient for the concerned industry, for instance, with 3-D electrical simulations. We can also seek hot points, involving drastic transient regimes, by the thermal approach. We should work on the placement routine of coolers, via investigations on the heat spreading, in three dimensions. A minimum, the electro thermal coupling can be done by the linear simple formula as [172], [173]

$$R = R_0(1 + \alpha_0\Delta T) \quad (3\text{-}41)$$

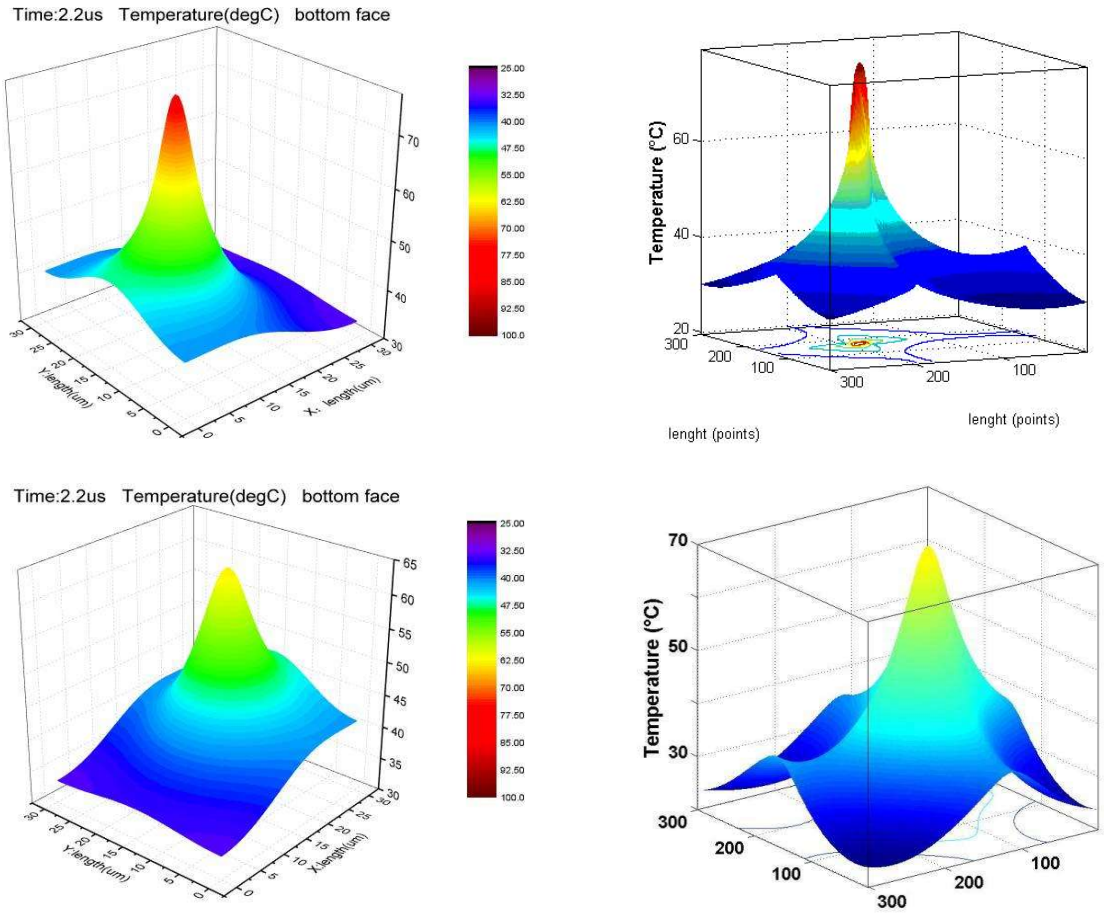
Finally, we will begin to study noise phenomena, fundamental for the nanoscale, for instance, the thermal noise, *4kRT*, coupling still electrical and thermal fields, or the generation-recombination (GR)-like one, as well as their coupling.

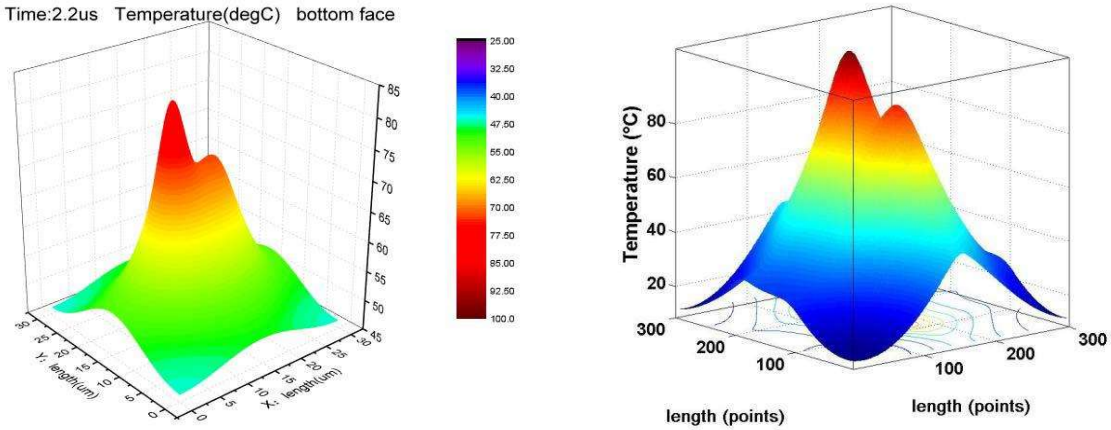
We present here a first modeling of second-order electrical phenomena for 3-D circuits.



(a)

COMSOL (FEM) Matlab (Green Kernels/TLM)





(b)

Figure 67 (a) Temperature source profile; measurement time point: 2.2 µs. (b) Temperature maps: (left) FEM results and (right) Green's results; t=2.3 µs [see Figure 63 (a)]

3.3) Thermal connection modeling

After a thermal substrate analysis, we inspect the thermal behavior of TSVs, the key elements of connections embedded in the substrate. 3D IC integration can effectively increase the system's integrity, but as a side effect, the following increase of system power density can cause serious heat dissipation problem [13][178][179][180][181][182][183][184][185]. It has become a bottleneck for the 3D IC. In this case, how to remove heat from the IC circuits and realize an effective heat management, becomes the key of the 3D IC technology. In order to solve the heat dissipation problem, researchers from all over the world have proposed some heat management solutions, such as conducting TSV, micro-pumps, using the new carbon nano-tube and graphene (which have a better heat conductivity than silicon) as the material. But all these technologies are based on the analysis of the heat transfer. The following part of this chapter will firstly give an accurate heat transfer analytical model of cylindrical TSVs, and study the temperature characters. And then, a study of a 4 cores single chip model is settled, in order to calculate multi-cores 3D-IC temperature characteristics.

Here, we did not consider the temperature-dependent material characteristics' change or we can also say that the temperature is fixed low, so the change of the material's characteristics is weak. Here, we just give a solution for each uniform layer and low temperature design.

In our study, we adopt linear model; we mean that the global effects of substrate and connections can be split. But, if the connections become very important, we cannot dissociate substrate with TSV, RDL, etc. Intercorrelation terms do intervene; the system can be approached by non-linear models.

3.3.1)3D IC heat analysis

3.3.1.1) 3D IC heat transfer compact model without TSVs

As shown in the following, Figure 68(a), 3D-IC is composed of n dies, and the bottom die is connected to a heat sink. Each die is connected by an adhesive coating layer, Si substrate and an oxide layer; the heat is generated by the heat source attached at each die, and the nth die's power dissipation is supposed here as Q_n.

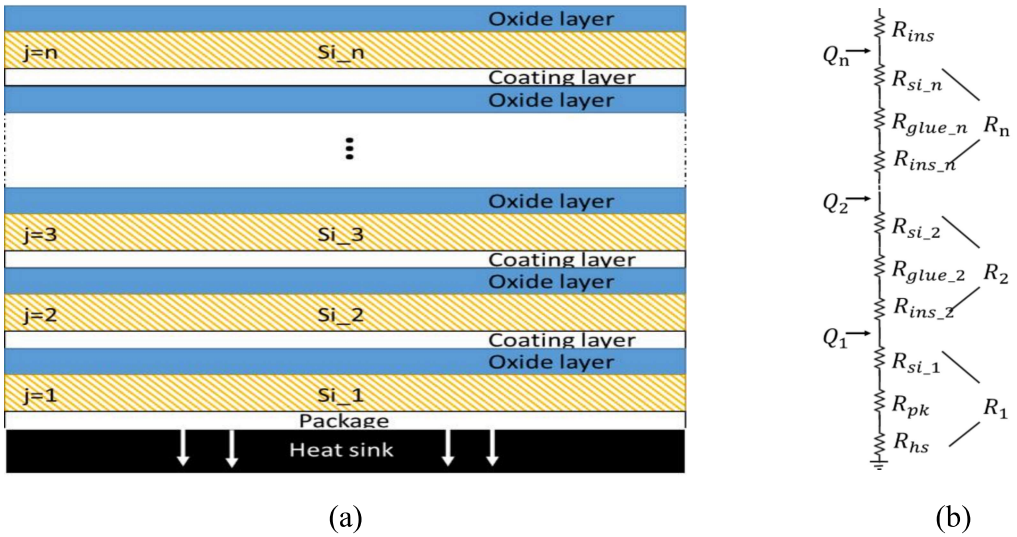
Because of the weak heat conductivity between oxide layer and coating layer, the heat conduction between dies becomes very hard, and compared with the dies' temperature change, the temperature exchange between dies can be neglected. Therefore, we can use one average temperature to define the temperature of each layer, and 3D chip is composed of n layers' 2D chips with different temperatures. According to the Fourier heat flow analysis, using the heat flow as an analogy of the current, temperature as an analogy of the voltage, heat resistance as an analogy of the resistance, we can get the jth layer's temperature. [182]

$$T_j = \sum_{i=1}^{j}[R_i(\sum_{m=i}^{n} Q_m)] \quad (3\text{-}42)$$

Here, n is the total layer number, R_m and Q_m are respectively the mth layer's heat resistance and power dissipation.[172]–[174]

Assuming that the each layer's power dissipation is the same, all Q, the first layer's thermal resistance is R_1, and the rest layers' thermal resistances are the same R, so for the n layers 3D IC, the top layer' temperature can be expressed as[182],

$$T_n = Q\left[\frac{R}{2}n^2 + (R_1 - \frac{R}{2})n\right] \quad (3\text{-}43)$$



(a) (b)

Figure 68 (a) Schematic of 3D IC structure (without Vias) (b) heat transfer model

From Figure 68(b), we can see that, the first die's thermal resistance R_1include the thermal resistance of S_{i_1} substrate, package and heat sink; the other dies' thermal resistance R include the thermal resistance of S_i substrate, coating layer and oxide layer. The thermal resistance is defined as $R = l/(kS)$, l is the heat flow length, k is the heat conductivity, S is the cross-section surface of heat flow; Q represents the power dissipation, so R_1 and R represent respectively [182]

$$R_1 = R_{si} + R_{pk} + R_{hs} = \frac{l_{si}}{k_{si}S} + R_{pk} + R_{hs} \quad (3\text{-}44)$$

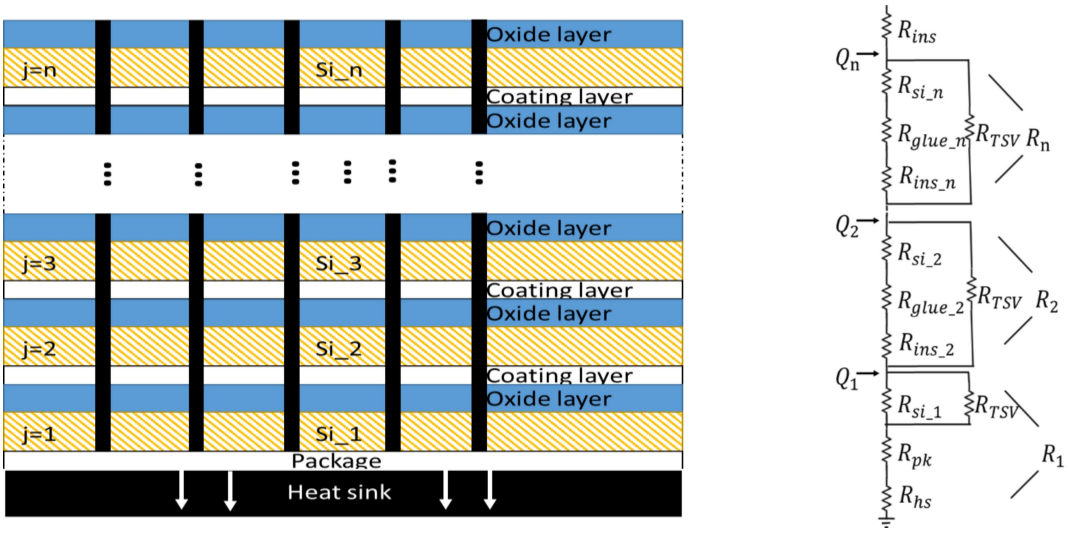
$$R = R_{si} + R_{glue} + R_{ins} = \frac{l_{si}}{k_{si}S} + \frac{l_{glue}}{k_{glue}S} + \frac{l_{ins}}{k_{ins}S} \quad (3\text{-}45)$$

where $R_{si}, R_{pk}, R_{hs}, R_{glue}, R_{ins}$ represent respectively, thermal resistance of each dies' silicon substrate, package , heat sink, coating layer and insulation layer, l_{si} , l_{glue} , l_{ins} represent respectively the thickness of silicon substrate, coating layer and insulation layer, $k_{si}, k_{glue}, k_{ins}$ represent the thermal conductivity of silicon substrate, coating layer and insulation layer, S is the chip's surface.

3.3.1.2) 3D IC top layer chip temperature analysis model by considering TSVs

In the 3D IC, TSV generally is filled with copper, because of its high thermal conductivity and strong heat dissipation power. If we neglect TSVs in the heat transfer model, it will lead to an over-estimation of the chip temperature, so it's necessary to consider TSV parasitic when analyzing 3D IC heat characteristics. And here we adopt a 3D IC top layer analytical model by considering TSVs.

After adding TSVs in the 3D IC, the structure will change to the following Figure 69(a) and Figure 69(b) is (a)'s heat transfer model.



(a) (b)

Figure 69 (a) Schematic of 3D IC structure with TSVs (b) Heat transfer model

Assuming that the total surface of each layer in the IC is S_{TSV}, the total chip surface is S, and TSV surface ratio is r, defined as:

$$r = \frac{S_{TSV}}{S} \tag{3-46}$$

When considering TSVs, the layer's thermal resistance will change to the parallel of TSV thermal resistance and the original thermal resistance, as shown in Figure 69(b). Assuming chip's surface stays unchanged, by adding TSV, the other parts' surface of the layer will be reduced, and that will be $(1-r)S$. So, the first layer's thermal resistance will change from R_1 to R_1'

$$R_1' = \frac{l_{si}}{k_{si}(1-r)S} || R_{TSV} + R_{pk} + R_{hs} = \frac{l_{si}}{k_{si}(1-r)S} || \frac{l_{si}}{k_{TSV}rS} + R_{pk} + R_{hs} \tag{3-47}$$

The other layers' thermal resistance will change from R to R'

$$R' = \left(\frac{l_{si}}{k_{si}} + \frac{l_{glue}}{k_{glue}} + \frac{l_{ins}}{k_{ins}}\right)\frac{1}{(1-r)S} || R_{TSV1} = \left(\frac{l_{si}}{k_{si}} + \frac{l_{glue}}{k_{glue}} + \frac{l_{ins}}{k_{ins}}\right)\frac{1}{(1-r)S} || \frac{l_{si}+l_{glue}+l_{ins}}{k_{TSV}rS} \tag{3-48}$$

So, after considering TSV in the 3D IC, top layer temperature analytical model can be written [182]

$$T_n = Q\left[\frac{\left(\left(\frac{l_{si}}{k_{si}} + \frac{l_{glue}}{k_{glue}} + \frac{l_{ins}}{k_{ins}}\right)\frac{1}{(1-r)S} || \frac{l_{si}+l_{glue}+l_{ins}}{k_{TSV}rS}\right)}{2} n^2 + \left(\left(\frac{l_{si}}{k_{si}(1-r)S} || \frac{l_{si}}{k_{TSV}rS} + R_{pk} + R_{hs}\right) - \left(\frac{\left(\frac{l_{si}}{k_{si}} + \frac{l_{glue}}{k_{glue}} + \frac{l_{ins}}{k_{ins}}\right)\frac{1}{(1-r)S} || \frac{l_{si}+l_{glue}+l_{ins}}{k_{TSV}rS}}{2}\right)n\right] \tag{3-49}$$

3.3.1.3) 3D IC Thermal modeling result

Here, we use an 8 dies 3D IC model, and we choose MATLAB to do the simulation. The following table gives the model parameters.

Table 11 8 dies 3D IC model's parameters

Q / (W)	Lsi / (um)	Lglue / (um)	Lins / (um)	ksi / (W/mK)	kglue / (W/mK)	kTSV / (W/mK)	kins / (W/mK)	Rhs / (K/W)	Rpk / (K/W)	S / (mm2)
2	50	2	8.8	150	0.25	390	0.07	2	20	10*10

Through the Matlab simulation, we can get the TSV top layer's temperature's change with the IC layer numbers, as shown in the following figure 10. We can see that, with the increase of number of layers, the chip top surface temperature increases linearly, the three colored lines represent r equals to 0.0001, 0.001, 0.01 and the black dotted line represents the dies without TSV. For the case without TSV, the top surface temperature can reach 427K, but after considering TSVs, the decrease of temperature is more obvious. The greater the r is, the lower the temperature is. So for a 8 layers 3D-IC, when r equals to 0.0001, the temperature of top layer decreases from 427K to 421K, when r=0.001, it decreases to 392K, when r=0.01, it's 360K, and this is because of the heat dissipation effect of TSV.

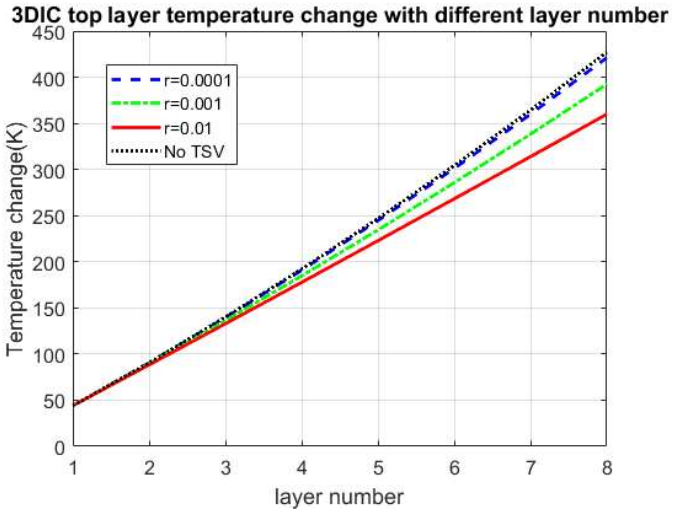


Figure 70 Different layer number's influence to the 3D IC top layer temperature

As shown in Figure 71, the 3D IC top layer's temperature change with TSV surface ratio r and dies' number n. For the same r, with the increase of dies' number n, r has more and more obvious influence to temperature. For a very high n, when we decrease r, at the beginning, the chip's temperature doesn't change, when r arrives enough small, the temperature T increases heavily.

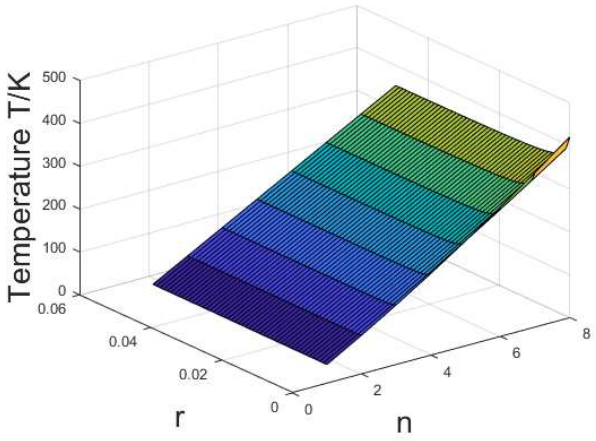


Figure 71 Surface ratio r and dies' number's influence to 3D IC top layer temperature

The following Figure 72 shows the temperature changes when n=8. When r equals to 0.0001, 3D IC top surface's temperature is 421K, with the increase of r, the temperature decreases. When r equals to 0.005, the temperature decreases to 366K, the decrease can reach 55K, about 13%; when r equals to 0.01, to compare with r equals to 0.005, the decrease is 6K, about 1.6%. When r equals to 0.015, the temperature is 357K, compared with r = 0.01, the decrease has only 3K, about 0.8%, and with the augmentation of r, the temperature doesn't have a significant change. Thus, in the 3D-IC design, for n=8, the best surface ratio of TSVs is 0.5%~1%. It can be adjusted with different demands. If the chip doesn't need so many interconnection signal line, the other TSVs can be

changed to thermal via and get a better heat transfer. 3D IC designer can read directly from the above Figure 71, the r value according to their temperature demand. When n equals to other value, r can also be calculated by this way.

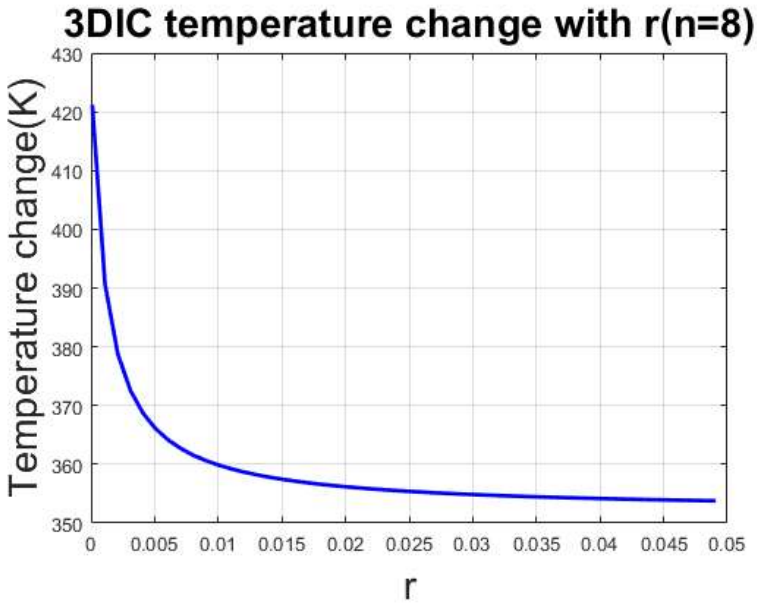


Figure 72 Temperature change with surface ratio r (n=8)

But if we want to get every point's temperature of the 3D IC, another 2D heat transfer solver should be used to generate accurately the temperature 2D distribution. Here, we adopt a finite volume method (FVM). The heat diffusion equation is in general used to describe the heat conduction in a chip and calculate the temperature profile:

$$\rho c_p \frac{\partial T(\vec{r},t)}{\partial t} = \nabla \cdot [k(\vec{r},T)\nabla T(\vec{r},t)] + g(\vec{r},t) \quad (3\text{-}50)$$

Which is subject to the general thermal conduction boundary condition.

$$k(\vec{r},T)\frac{\partial T(\vec{r},t)}{\partial n_i} = h_i(T_a - T(\vec{r},t)) \quad (3\text{-}51)$$

In the above equations, T is the temperature (K), k is the thermal conductivity [W/m/K], ρ is the density of the material (kg/m^3), c_p is the specific heat [J/kg/K], g is the power density of the heat sources (W/m^3), and h_i is the heat transfer coefficient in the direction of heat flow $\vec{\imath}$ on the boundary surface of the chip [W/m^2/K].

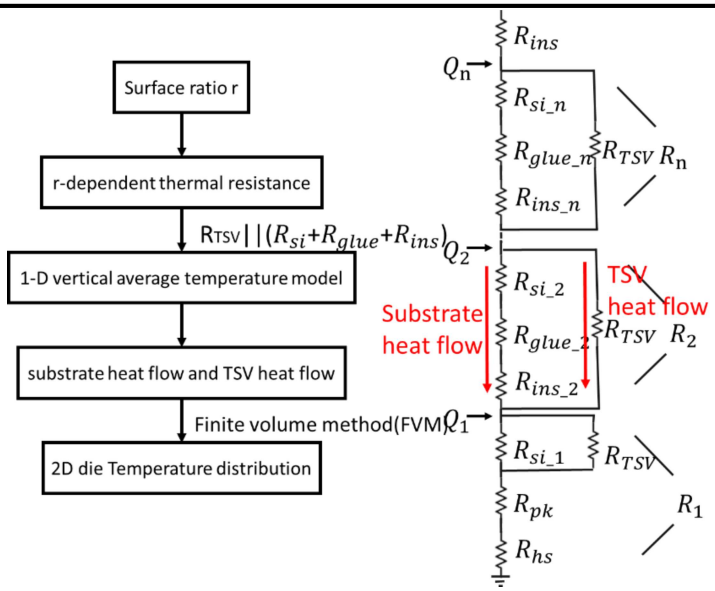


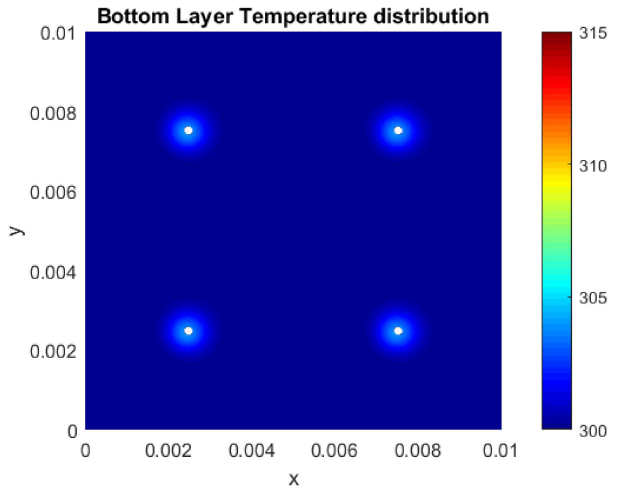
Figure 73 3D Thermal simulation work flow

Figure 73 shows our total 3D Thermal simulation work flow. In our case, we firstly get the surface ratio r, and calculate the r-dependent thermal resistance, such as R_{TSV}, R_{Si}, R_{glue}, R_{ins}. By using the analytical vertical model, the temperature vertical distribution can be obtained. With the temperature difference, which is similar (analog) to the electrical potential, and we can also directly calculate the heat which passes by the substrate and also heat which passes by TSVs, which can be calculated by the following equation:

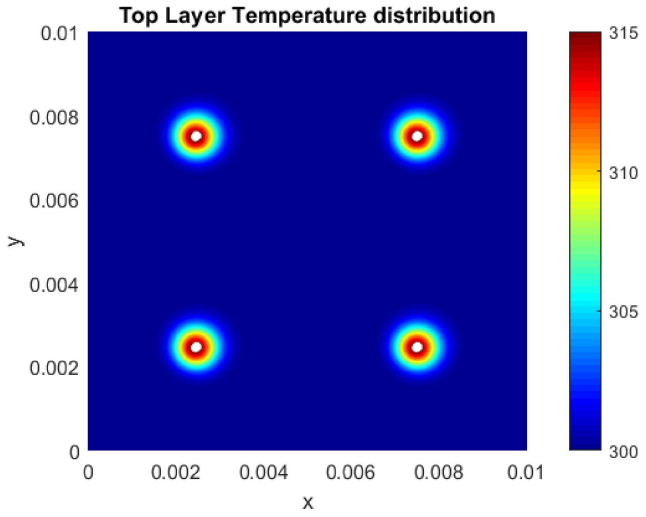
$$q_{TSV\_n} = \frac{(T_n - T_{n-1})}{R_{TSV}} \tag{3-52}$$

$$q_{sub\_n} = \frac{(T_n - T_{n-1})}{R_{si\_n} + R_{glue\_n} + R_{ins\_n}} \tag{3-53}$$

And finally, we come back to 2D thermal conduction with 2 different kinds of heat source, q_{TSV_n} and q_{sub_n}.Here, we adopt the finite volume method (FVM) to solve the problem. And then, a 2D thermal distribution is generated. The following figures show the bottom layer's and top layer's thermal temperature distribution in the substrate of an 8 dies model with r=0.01 and 4 TSVs. The bottom layer's TSV temperature is 344K and top layer's TSV temperature is 359.88K.



(a)



(b)

Figure 74 (a) Bottom and (b) Top layer temperature distribution of 4 TSVs with surface ratio r = 0.01

3.3.2)CMP (Chip multiprocessor) heat transfer

With the development of micro-processors, the traditional superscalar technology has slightly improved the CPU performance. Power dissipation issues have greatly restricted the gain of CPU clock frequency. Because of all these things, it needs a change of computer structure arrangement, and it needs a smaller distribution design of micro-processor, and a partially better cell structure. In this background, researchers proposed Chip multiprocessor technology (CMP) [150][189][152]–[163]. CMP means to integrate 2 or more CPU cores in one chip, in which every core can do a multi-thread calculation simultaneously. The main purpose of CMP is to gain the integrity and increase performance. Nevertheless, with the augmentation of integration level and

the reduction of feature size, chip internal interconnection line ratio increases continuously, especially when the chip feature size is reduced below 0.18μm, the interconnection delay has surpassed gate delay; this brings a serious challenge for the CMP's performance. By adopting 3D technologies, the different cores can be connected vertically, and it can solve effectively a lot of 2D CMP problems. However, due to the 3D CMP layers multi-heat source, CMP 3D IC faces a more serious heat dissipation issues than the other 3D IC. So the thermal study of the CMP 3D IC is very important.

For 3D CMP temperature characteristics, thermal resistance matrix is a very important parameter. It represents unit power dissipation's influence to temperature, once the thermal resistance matrix is obtained. Moreover we can get whichever core's power dissipation influence to the other core. This chapter gives the thermal resistance matrix expression. Based on the thermal resistance matrix, we study precisely the 3D CMP temperature characteristics, and analyze the heat capacitor, thermal resistance and power dissipation's influence on the temperature.

Multiple cores 3D CMP structure involves connecting the cores vertically. Thus, for 2 layers 3D CMP, the chip's internal heat transfer model can be shown as follows, assuming that, each layer has 2 cores. They can be expressed as A,B and C, D, ginter, gintra and ghs are the interlayer heat conductance, inner layer heat conductance and heat sink conductance, respectively. CH, CI, CJ and CK are the cores heat capacitors, respectively. PH, PI, PJ and PK are cores' power dissipation. Tamb is the environment temperature.

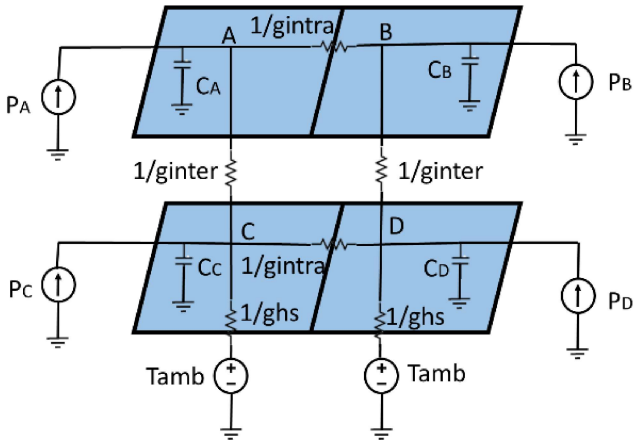


Figure 75 4 cores CMP model

According to current Fourier heat analysis theory, the heat flow as an analogy of the current, temperature as an analogy of the voltage, heat resistance as an analogy of the resistance, heat capacitor as an analogy of capacitance, and the CMP 2 layers model can be described as the following equation: [187], [188]

$$C\frac{dT(t)}{dt} + AT(t) = Pu(t) \tag{3-54}$$

Here, C is a 4X4 diagonal matrix, and every diagonal element is the core's heat capacitor. T(t) is a 4-dimensional vector, which represents the four cores temperature at time t. A is a 4X4 thermal conductance matrix. P is a 4 dimensional power vector. u(t) is a step function.

3.3.2.1) Thermal resistance matrix

For the stationary case, we neglect the heat capacitor matrix C's influence, and the heat conduction equation can be simplified to

$$T = A^{-1}P \tag{3-55}$$

Here, A^{-1} is the thermal resistance matrix. It describes unit power dissipation's influence to the temperature, so it can be called thermal influence matrix.[187], [188]

By using the nodal analysis, we use R_{ij} to represent the core i's influence resistance to core j, and the thermal resistance matrix can be expressed as

$$A^{-1} = \begin{pmatrix} R_{AA} & R_{AB} & R_{AC} & R_{AD} \\ R_{BA} & R_{BB} & R_{BC} & R_{BD} \\ R_{CA} & R_{CB} & R_{CC} & R_{CD} \\ R_{DA} & R_{DB} & R_{DC} & R_{DD} \end{pmatrix} \tag{3-56}$$

Because core A and core D do not have a direct thermal connection, the thermal influence between them can be neglected, so as the B, C. Then:

$$R_{AD} = R_{DA} = R_{BC} = R_{CB} = 0 \tag{3-57}$$

By using the nodal analysis, the thermal resistance matrix can be expressed as [187], [188]

$$A = \begin{pmatrix} g_{intra} + g_{inter} & -g_{intra} & -g_{inter} & 0 \\ -g_{intra} & g_{intra} + g_{inter} & 0 & -g_{inter} \\ -g_{inter} & 0 & g_{intra} + g_{inter} + g_{hs} & -g_{intra} \\ 0 & -g_{inter} & -g_{intra} & g_{intra} + g_{inter} + g_{hs} \end{pmatrix} \tag{3-58}$$

3.3.2.2) CMP Thermal modeling result

After getting the thermal resistance matrix, we can get the 3D CMP temperature characteristic equations [187], [188]

$$\begin{pmatrix} C_A & 0 & 0 & 0 \\ 0 & C_B & 0 & 0 \\ 0 & 0 & C_C & 0 \\ 0 & 0 & 0 & C_D \end{pmatrix} \begin{pmatrix} \frac{dT_A(t)}{dt} \\ \frac{dT_B(t)}{dt} \\ \frac{dT_C(t)}{dt} \\ \frac{dT_D(t)}{dt} \end{pmatrix} +$$

$$\begin{pmatrix} g_{intra}+g_{inter} & -g_{intra} & -g_{inter} & 0 \\ -g_{intra} & g_{intra}+g_{inter} & 0 & -g_{inter} \\ -g_{inter} & 0 & g_{intra}+g_{inter}+g_{hs} & -g_{intra} \\ 0 & -g_{inter} & -g_{intra} & g_{intra}+g_{inter}+g_{hs} \end{pmatrix} \begin{pmatrix} T_A(t) \\ T_B(t) \\ T_C(t) \\ T_D(t) \end{pmatrix} = \begin{pmatrix} P_A \\ P_B \\ P_C \\ P_D \end{pmatrix} u(t) \quad (3\text{-}59)$$

Assuming that every core has the same heat capacitor C, and their power dissipations are all P. By using Matlab differential equation solver, we can get 3D CMP temperature characteristics.

Table 12 Parameters[191]

P(W)	C(J/K)	gintra(W/K)	ginter(W/K)	gins(W/K)
25	5	0.41	6.67	0.82

When t=0, input a step heat source, 3D CMP temperature temporary character can be found below. Because core A and B stay in the same condition, so their temperature characteristics are the same. We can see that from the following Figure 76 and so is core C and D. From this figure, the change of the heat flow will increase the cores temperature at first. Then, the temperature will get to stationary. Core A and B's temperature is about 5K higher than that of core C and D, that's due to core C and D are a bit far away from the heat sink. Moreover, heat is not easy to be dissipated.

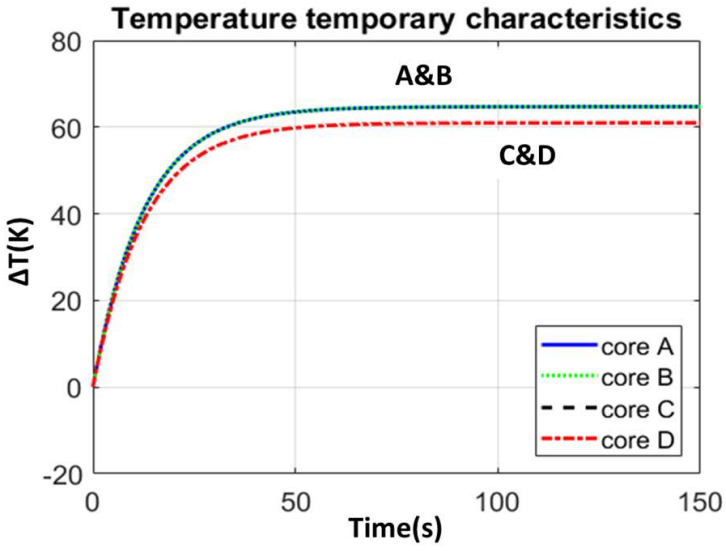
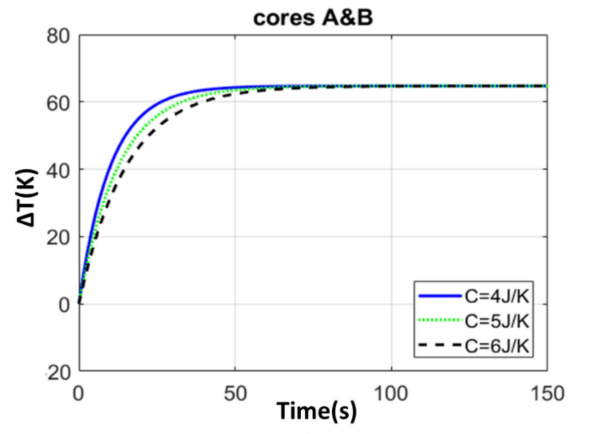
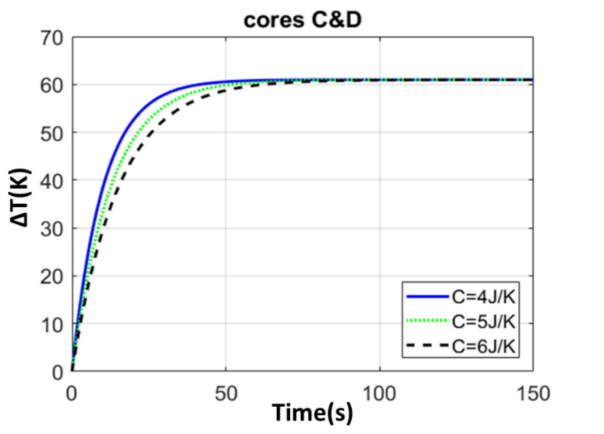


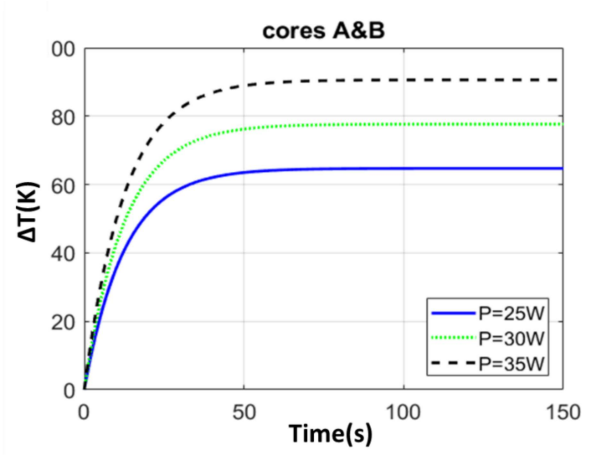
Figure 76 3D CMP temporary temperature characteristics


cores A&B
ΔT(K)
Time(s)
C=4J/K
C=5J/K
C=6J/K

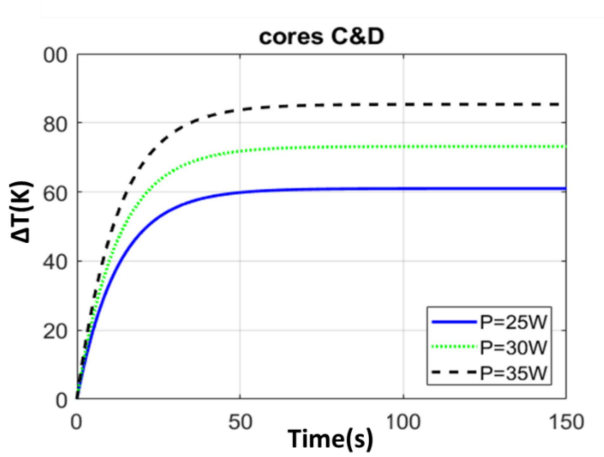
(a)


cores C&D
ΔT(K)
Time(s)
C=4J/K
C=5J/K
C=6J/K

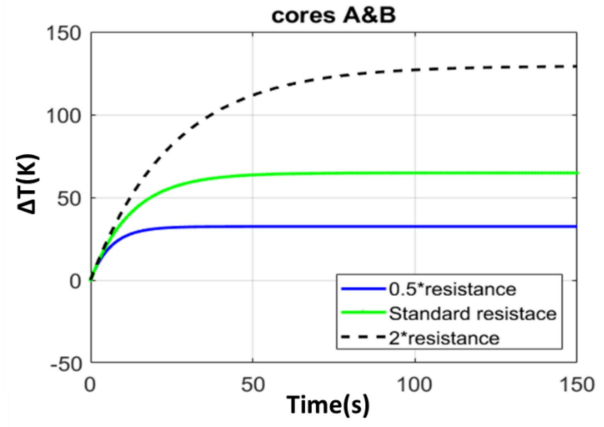
(b)


cores A&B
ΔT(K)
Time(s)
P=25W
P=30W
P=35W

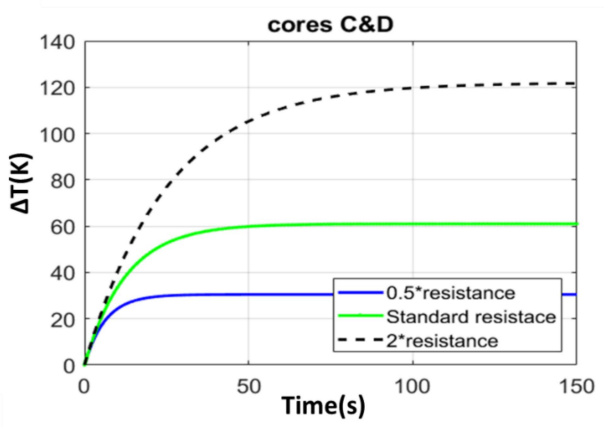
(c)


cores C&D
ΔT(K)
Time(s)
P=25W
P=30W
P=35W

(d)


cores A&B
ΔT(K)
Time(s)
0.5*resistance
Standard resistace
2*resistance

(e)


cores C&D
ΔT(K)
Time(s)
0.5*resistance
Standard resistace
2*resistance

(f)

Figure 77 Temperature temporary characteristics (a) of core A&B with different heat capacities (b) of core C&D with different heat capacities (c) of core A&B with different power inputs (d) of core C&D with different power inputs (e) of core A&B with different thermal resistances (f) of core C&D with different thermal resistances

For different heat capacities, the temperature characteristics of core A, B and core C, D are shown in the former Figure 77. The higher C is, the longer time the cores will need to attend the stationary temperature. However, it will not change the maximum temperature, thus we cannot change the CMP temperature by changing heat capacity.

Nevertheless, when the heat dissipation changes, core A&B, and core C&D's temperature character can be found in the former Figure 77. The three lines represent the heat dissipation of 20W, 25W and 30W. Once the heat dissipation increases 5W, core A&B and core C&D gain separately about 13.17K and 12.9K. The power dissipation has more influence on the core A&B, that's due to the longer distance to the heat sink comparing with the core C&D. The core's stationary temperature change linearly with power dissipation, so designers can adopt different low power technique to reduce core's power dissipation and then reduce the temperature. As we can see from the Figure 77 (e)(f), when the thermal resistance increase 50% of the standard value, the core A&B's temperature increase about 32.2K, and core C&D's temperature increase about 30.3K. So the stationary temperature increases linearly with the thermal resistance. Then, we can choose a higher thermal conductivity material or use more thermal via in the dies, in order to reduce the chip's thermal resistance, and control the chip's temperature.

3.3.2.3) CMP conclusion

Firstly, this part introduces some basic thermal analysis leading to a 3D IC top layer's temperature model, by introducing surface ratio r, correlate the 3D IC temperature analytical model. Based on the correlated temperature model, study the influence of TSV's surface ratio r to the temperature, finally give the best r factor's range of 8 dies 3D IC model. Based on the thermal resistance, we study the 3D CMP temperature characteristics, and analyze the heat capacity, thermal resistance and heat dissipation's influence on chip temperature. As shown above, thermal resistance and power dissipation can affect 3D CMP's stationary temperature, so we can adopt different low power design to reduce chip's power dissipation, and we can also choose a higher heat conductivity material to reduce the thermal resistance to control the chip temperature. The higher heat capacity is, the longer time 3D CMP will need to get to the stationary temperature. However, the change of heat capacity will not change the final stationary temperature. Furthermore, this part gives a very important basis for the 3D CMP heat management.

In fact, this part gives a simple total very prime view of 3D IC problems and a simple solution. We don't take so complicated case into consideration, but for the further study, we will consider electro-thermal effect of caches' and cores' interconnections.

3.4) Electro-thermal (ET) modeling of VLS circuits

As indicated in the roadmap for integrated circuits (ICs), the increasing power density needs the decreasing power supply voltage, which results in the need of larger current supply by the power delivery networks (PDNs) [4], [55]. Consequently, Joule heating and power switching [203] rise a lot the circuit temperature, which heavily influences the electrical performances, because of the heavily changed electrical temperature dependent resistivity[202]. So an efficient ET co-simulation PDN software is needed, for now, to calculate the effective IR drop, which is strongly related to the electrical resistivity. Moreover, ET co-simulations are inevitable in 3D IC design [106] [143].

We use a standard structure for ground and power networks as shown in the following Figure 78. The ground and power networks are separated by an insulation layer, and connected respectively with VDD and GND pins, through a series of impedance Z_{supply} .

The electrical and thermal issues should be solved together in the static and dynamic analysis. A device level thermal and electrical modeling method will be provided and justified, dedicated to CPW and TSVs. The main heat sources are the logic gates switching, as well as the Joule heating in the PDN interconnects. The thermal transport and electrical transport are very similar, the heat flow corresponding to the electrical current and the temperature difference plays the role of the electrical voltage [33]. By this way, the electro-thermal co-simulation can be exploited within the same circuit solver.[193]–[195]

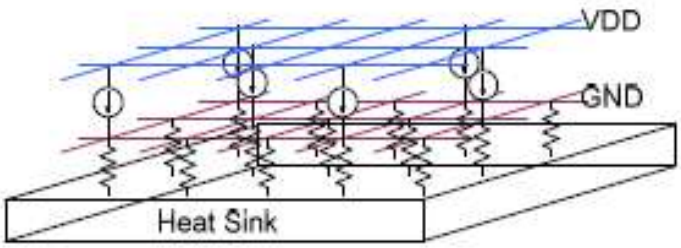


Figure 78 Structure for ground and power networks

3.4.1) Electrical modeling of VLS (Very Large Scale) circuits

The DC problem is modeled by two regular resistive grids and one internal node; the temperature-dependent resistors R(T) connect neighboring nodes of the same layer. The power and ground layer are interconnected by a current source I_0. The solution of the electrical problem can be expressed as the voltage drop at the node i:

$$V_d(i) = V_{DD} - (V_n(i) - V_g(i)) \quad (3\text{-}60)$$

Where $V_n(i)$ and $V_g(i)$ are the node potentials of power and ground planes, respectively.

A dynamic electrical model can also be carried out when parasitic dynamic circuit has been defined for this structure. We use the standard first order model for each physical cell, by considering the parasitic inductive effect L between adjacent nodes, and a parallel capacitive C between neighboring nodes on the VDD and GND grids. By this way, we draw a dynamic elementary cell schema as shown in Figure 79.

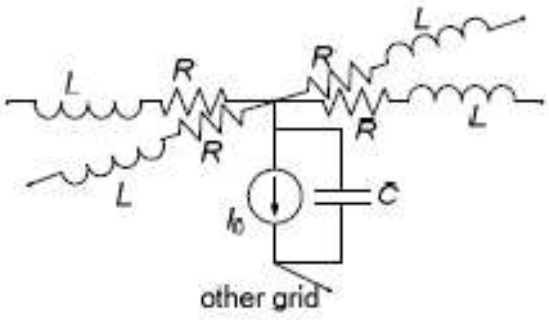


Figure 79 Dynamic electrical elementary cell

3.4.2)Electrical modeling result of 3D IC

3.4.2.1) Case I: Electrical modeling of 3xRLC segments model

The model can be described through a SPICE-like script

```
* Example RLC-3

Vin N_in1   0 PULSE 0 3 0.5m 0.5m  0.5m 4m  10m

X1  n_in1   n_in2   seg
X2  N_in2   N_in3   seg
X3  n_in3   n_out   seg
Cl  n_out   0       10u

.SUBCKT seg n_in    n_out
Rseg    N_IN    N_1     3.5
Lseg    n_1     N_OUT   1.2m
Cseg    N_OUT   0       7.3u
.ENDS seg

.TRAN   0.004m 20m
.PROBE  V(n_out)
.print V(n_out)
.end
```

Figure 80 3xRLC series model Spice script

The model describe a 3 segments RLC circuits. The electrical circuit is shown in the following figures

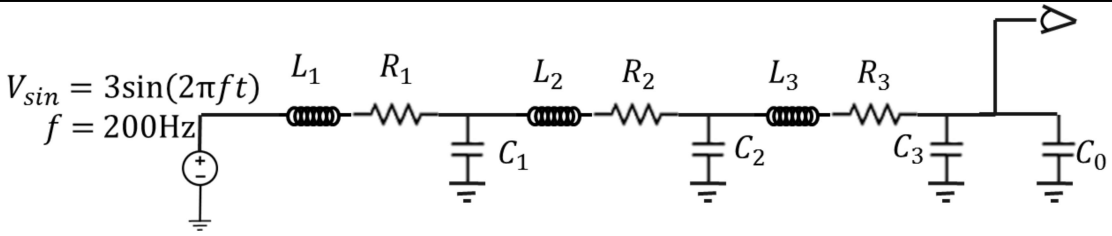
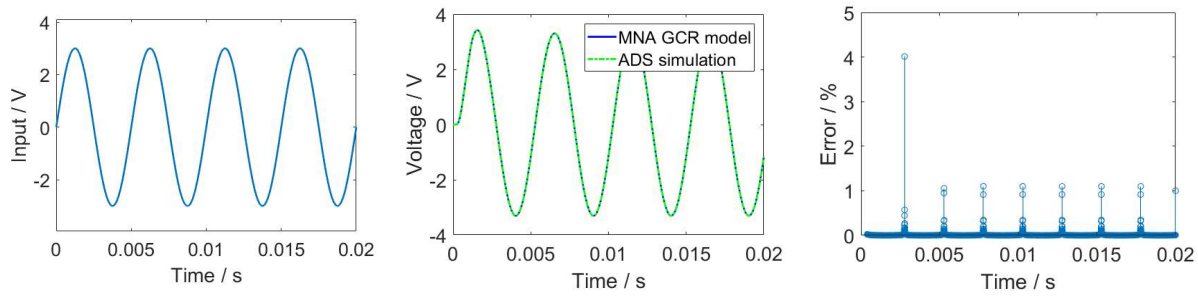


Figure 81 Compact model o 3 RLC segments model

The segments' resistance is 3.5 ohm, inductance is 1.2e-3 H, the capacitance is 7.3e-6 F, and the added capacitance at the probe side is 10e-6 F. The voltage source is a sine signal, with an amplitude of 3V, and working frequency 200Hz. Here we use the modified nodal analysis method (MNA) and generalized conjugate residual (GCR) solver and also sparse matrix technic to solve and accelerate the calculation of large scale differential matrix. The precise method description can be found in the annex. In order to verify the method's robustness, the same simulation is done with ADS (advanced design system by Keysight Technologies [207]). The signal is shown in the figure (a), the output signal comparison with ADS is shown in the Figure 82(b). And Figure 82(c) shows the relative error of the MNA+GCR method and ADS. As we can see from the Figure 82(c), our MNA+GCR method has a very good accuracy in compare with the ADS, the maximum error is about 4%.



(a) (b) (c)

Figure 82 (a) Input voltage source (b) Output comparison between MNA and ADS (c) Relative error between MNA and ADS for 3 RLC segments model

3.4.2.2) Case II: CPW (Coplanar Wave Model)

As the same, but a little different, we define the model's geometry and material parameters in one txt file [208], and then by using INL's 3D-TLE (3D Transmission line extractor), generate automatically a Spice compatible sp file. This file is shown in Figure 83.

```
*Netlist generated from Umodel
Vin in_real  0 PULSE 0 3 0.5m 0.5m  0.5m 4m 10m
.subckt gnd1_signal_gnd2 in1 out1 in2 out2 in3 out3

R1 in1 x1_gnd1 0.03225
L1 x1_gnd1 x2_gnd1 5.6541e-11
```

```
L2 x2_gnd1 x3_gnd1 5.6541e-11
R2 x3_gnd1 out1 0.03225
Cox_gnd1 x2_gnd1 nox_gnd1 1.3335e-12
Repi_gnd1 nox_gnd1 0 312.5
Cepi_gnd1 nox_gnd1 0 1.6567e-14

R3 in2 x1_signal 0.028667
L3 x1_signal x2_signal 5.3965e-11
L4 x2_signal x3_signal 5.3965e-11
R4 x3_signal out2 0.028667
Cox_signal x2_signal nox_signal 1.5002e-12
Repi_signal nox_signal 0 277.7778
Cepi_signal nox_signal 0 1.8638e-14

R5 in3 x1_gnd2 0.03225
L5 x1_gnd2 x2_gnd2 5.6541e-11
L6 x2_gnd2 x3_gnd2 5.6541e-11
R6 x3_gnd2 out3 0.03225
Cox_gnd2 x2_gnd2 nox_gnd2 1.3335e-12
Repi_gnd2 nox_gnd2 0 312.5
Cepi_gnd2 nox_gnd2 0 1.6567e-14

K1 L1 L3 0.42787
K2 L2 L4 0.42787
Cinter1 x2_signal x2_gnd1 6.7837e-15

K3 L3 L5 0.42787
K4 L4 L6 0.42787
Cinter2 x2_gnd2 x2_signal 6.7837e-15

K5 L1 L5 0.30072
K6 L2 L6 0.30072

.ends gnd1_signal_gnd2

X1_gnd1_signal_gnd2 0 0 1 2 0 0 gnd1_signal_gnd2
C1 2 0 100e-15
R1 in_real 1 50
.TRAN   0.004m 20m
.PROBE  V(2)
.print V(2)
.end
.end
```

Figure 83 CPW model Spice script

The model describe a coplanar wave model. The electrical circuit is shown in Figure 84.

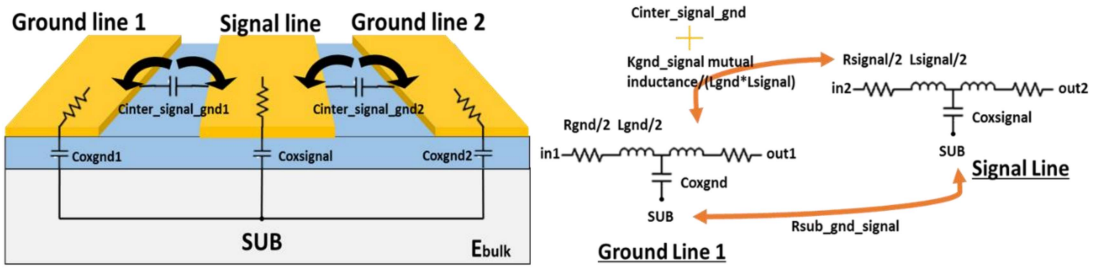
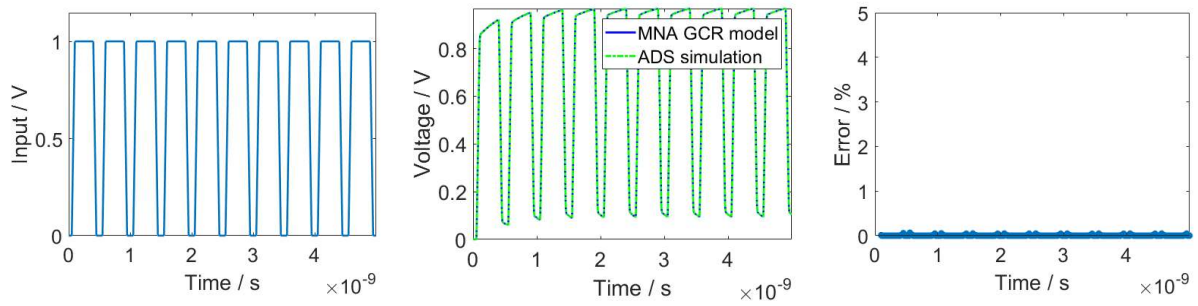


Figure 84 CPW geometry and compact model

We define two kinds of lines, one signal line, one ground line, and each line is treated as a T model. We define a C_{inter} between any two lines and each line is isolated from the substrate by an oxide layer. The voltage source is a pulse signal, with an amplitude of 1V, rise and down time of 0.05ns, duty cycle of 60%, and working frequency 2GHz. Here we also use the modified nodal analysis method (MNA) and generalized conjugate residual (GCR) solve. In order to verify the method's robustness, the same simulation is done in ADS. The signal is shown in the Figure 85(a), the output signal comparison with ADS is shown in the Figure 85 (b), and Figure 85 (c) shows the relative error of the MNA+GCR method and ADS. As we can see from the Figure 85 (c), our MNA+GCR method has a very good accuracy in compare with the ADS, the maximum error is about 3.5%.



(a) (b) (c)

Figure 85(a) Input voltage source (b) Output comparison between MNA and ADS (c) Relative error between MNA and ADS for CPW model

3.4.2.3) Case III: Two TSVs (through silicon via) U-model

As the same, we define the model's geometry and material parameters in one txt file, and then by using our (cf. chapter 2) 3D-TLE (3D Transmission line extractor), generate automatically a Spice compatible sp file. This file is shown as follows.

```
*Netlist generated from Umodel
Vin in_real  0 PULSE 0 3 0.5m 0.5m  0.5m    4m  10m
.subckt line1 in out
R1 in x1 0.0032762
L1 x1 x2 5.2519e-11
```

```
L2 x2 x3 5.2519e-11
R2 x3 out 0.0032762
Cox x2 0 9.7173e-13
.ends line1

X1_signal 11 12 line1

.subckt line3 in out
R1 in x1 0.0012286
L1 x1 x2 1.2226e-11
L2 x2 x3 1.2226e-11
R2 x3 out 0.0012286
.ends line3

X1_rdlin 1 11 line3

X1_rdlout 12 2 line3

.subckt gnd1_gnd2 in1 out1 in2 out2

R1 in1 x1_gnd1 0.03225
L1 x1_gnd1 x2_gnd1 5.6541e-11
L2 x2_gnd1 x3_gnd1 5.6541e-11
R2 x3_gnd1 out1 0.03225
Cox_gnd1 x2_gnd1 nox_gnd1 9.8554e-13
Repi_gnd1 nox_gnd1 0 18.9375
Cepi_gnd1 nox_gnd1 0 4.9702e-13

R3 in2 x1_gnd2 0.03225
L3 x1_gnd2 x2_gnd2 5.6541e-11
L4 x2_gnd2 x3_gnd2 5.6541e-11
R4 x3_gnd2 out2 0.03225
Cox_gnd2 x2_gnd2 nox_gnd2 9.8554e-13
Repi_gnd2 nox_gnd2 0 18.9375
Cepi_gnd2 nox_gnd2 0 4.9702e-13

K1 L1 L3 0.30072
K2 L2 L4 0.30072
Cinter1 x2_gnd2 x2_gnd1 1.1493e-15

.ends gnd1_gnd2

X1_gnd1_gnd2 3 4 5 6 gnd1_gnd2


.subckt pad1_pad3 in1 out1 accesstsv1 in2 out2 accesstsv2

R1 in1 x1_pad1 0.012094
L1 x1_pad1 accesstsv1 1.3508e-11
L2 accesstsv1 x2_pad1 1.3508e-11
R2 x2_pad1 out1 0.012094

R3 in2 x1_pad3 0.012094
```

```
L3 x1_pad3 accesstsv2 1.3508e-11
L4 accesstsv2 x2_pad3 1.3508e-11
R4 x2_pad3 out2 0.012094

K1 L1 L3 0.74376
K2 L2 L4 0.74376
Cinter1 accesstsv2 accesstsv1 4.3097e-16

.ends pad1_pad3

X1_pad1_pad3 0 3 101 0 5 102 pad1_pad3


.subckt pad2_pad4 in1 out1 accesstsv1 in2 out2 accesstsv2

R1 in1 x1_pad2 0.012094
L1 x1_pad2 accesstsv1 1.3508e-11
L2 accesstsv1 x2_pad2 1.3508e-11
R2 x2_pad2 out1 0.012094

R3 in2 x1_pad4 0.012094
L3 x1_pad4 accesstsv2 1.3508e-11
L4 accesstsv2 x2_pad4 1.3508e-11
R4 x2_pad4 out2 0.012094

K1 L1 L3 0.74376
K2 L2 L4 0.74376
Cinter1 accesstsv2 accesstsv1 4.3097e-16

.ends pad2_pad4

X1_pad2_pad4 4 0 201 6 0 202 pad2_pad4


.subckt tsv1_tsv2 in1 out1 side1 side2 in2 out2 side3 side4

R1 in1 x1_tsv1 0.0031471
L1 x1_tsv1 x2_tsv1 1.8915e-11
L2 x2_tsv1 x3_tsv1 1.8915e-11
R2 x3_tsv1 out1 0.0031471
Coxtsv1_tsv1 x2_tsv1 p1_tsv1 1.9807e-12
Coxtsv2_tsv1 x2_tsv1 p2_tsv1 1.9807e-12
Repi1_tsv1 p1_tsv1 epi1_tsv1 50.5
Cepi1_tsv1 p1_tsv1 epi1_tsv1 1.8638e-13
Repi2_tsv1 p2_tsv1 epi2_tsv1 50.5
Cepi2_tsv1 p2_tsv1 epi2_tsv1 1.8638e-13
Coxgnd1_tsv1 epi1_tsv1 side1 3.6958e-13
Coxgnd2_tsv1 epi2_tsv1 side2 3.6958e-13

R3 in2 x1_tsv2 0.0031471
L3 x1_tsv2 x2_tsv2 1.8915e-11
L4 x2_tsv2 x3_tsv2 1.8915e-11
R4 x3_tsv2 out2 0.0031471
```

```
Coxtsv1_tsv2 x2_tsv2 p1_tsv2 1.9807e-12
Coxtsv2_tsv2 x2_tsv2 p2_tsv2 1.9807e-12
Repi1_tsv2 p1_tsv2 epi1_tsv2 50.5
Cepi1_tsv2 p1_tsv2 epi1_tsv2 1.8638e-13
Repi2_tsv2 p2_tsv2 epi2_tsv2 50.5
Cepi2_tsv2 p2_tsv2 epi2_tsv2 1.8638e-13
Coxgnd1_tsv2 epi1_tsv2 side3 3.6958e-13
Coxgnd2_tsv2 epi2_tsv2 side4 3.6958e-13

K1 L1 L3 0.11406
K2 L2 L4 0.11406

.ends tsv1_tsv2

X1_tsv1_tsv2 in 1 101 102 2 out 201 202 tsv1_tsv2
R1_tsv1 in_real in 50
C1_tsv2 out 0 100e-15
.TRAN   0.004m 20m
.PROBE  V(out)
.print V(out)
.end
.end
```

Figure 86 2xTSVs chain U model

The model describes a coplanar wave model. The electrical circuit is shown in Figure 87.

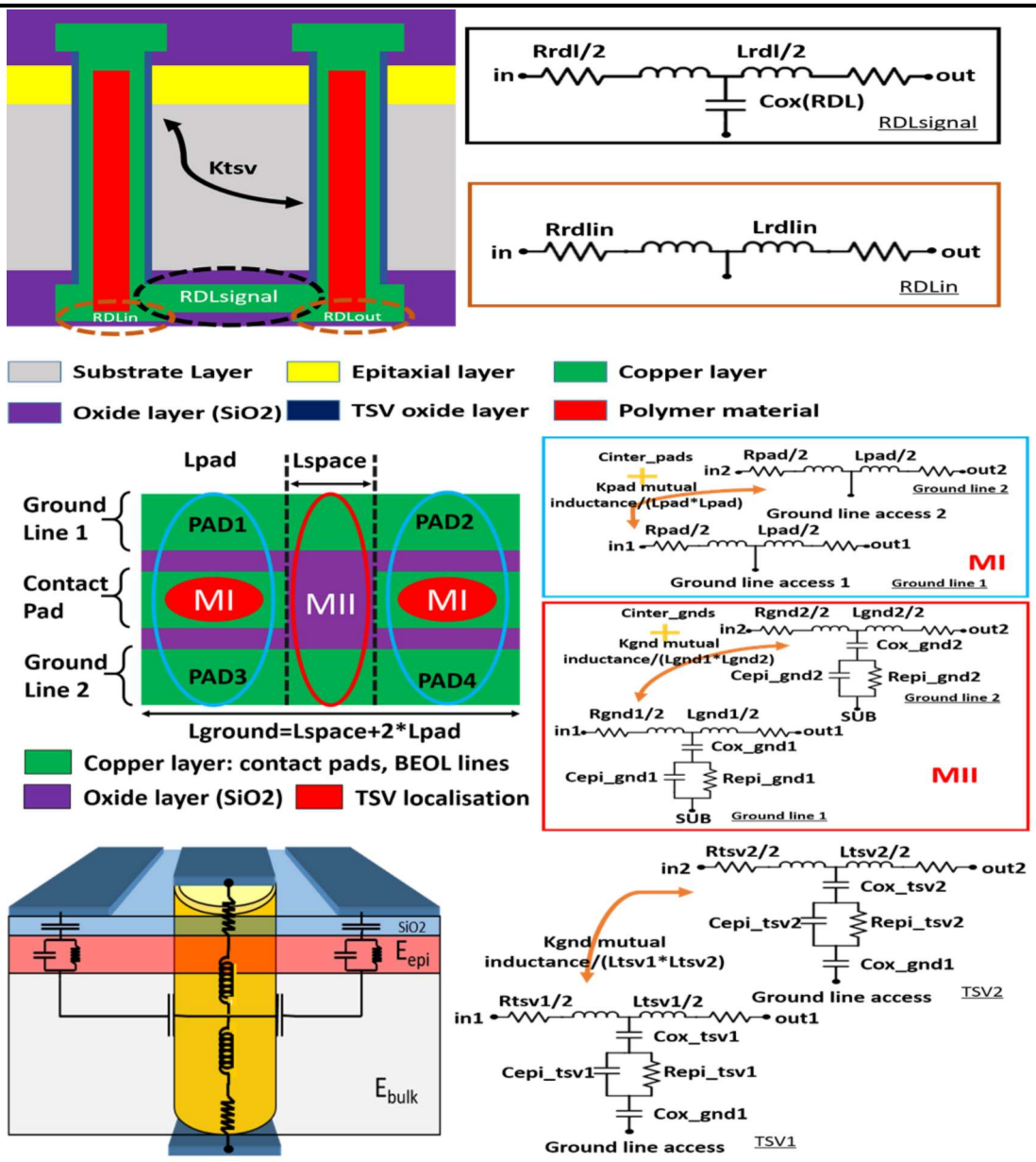
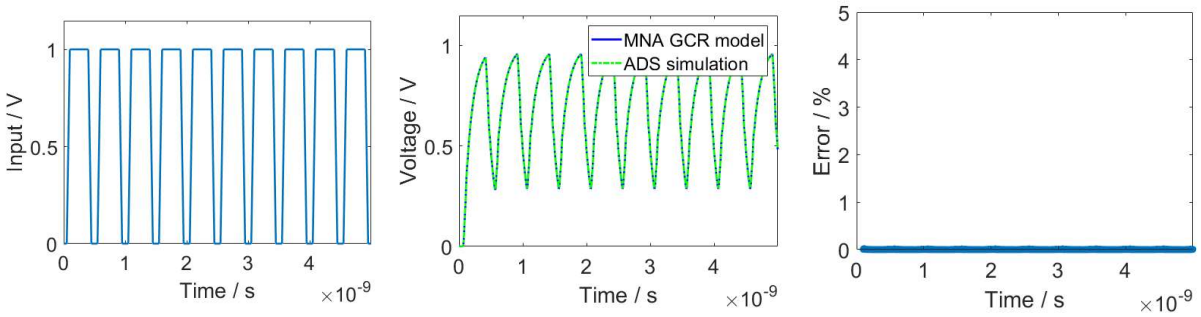


Figure 87 2xTSVs chain model geometry and compact model

We define two ground lines, two TSVs, and one redistribution layer (RDL). They are treated as a T model. The exact model is shown in the upper Figure 87. The voltage source is a pulse signal, with an amplitude of 1V, rise and down time of 0.05ns, duty cycle of 60%, and working frequency 2GHz. Here we also use the modified nodal analysis method (MNA) and generalized conjugate residual (GCR) solver. In order to verify the method's robustness, the same simulation is done in ADS. The signal is shown in the Figure 88(a), the output signal comparison with ADS is shown in the Figure 88(b), and Figure 88(c) shows the relative error of the MNA+GCR method and ADS.

As we can see from the Figure 88(c), our MNA+GCR method has a very good accuracy in compare with the ADS, the maximum error is about 1.6%.



(a) (b) (c)

Figure 88 (a) Input voltage source (b) Output comparison between MNA and ADS (c) Relative error between MNA and ADS for 2xTSVs chain model

In Figure 88, we can find out that the MNA+GCR method have the save accuracy with ADS simulator, and it can be integrated with 3D-TLE extractor without any difficulties. The general design process is shown in Figure 89.

This part gives a simple thermal modeling solution for 3D IC. This study method is viable for one CPW model, it can also be used for 20, 100 and more CPWs cases. A difficulty lies on that we could not consider a great number of CPWs, as simple sum of CPWs; we do consider non-linear models, which needs more physical studies.

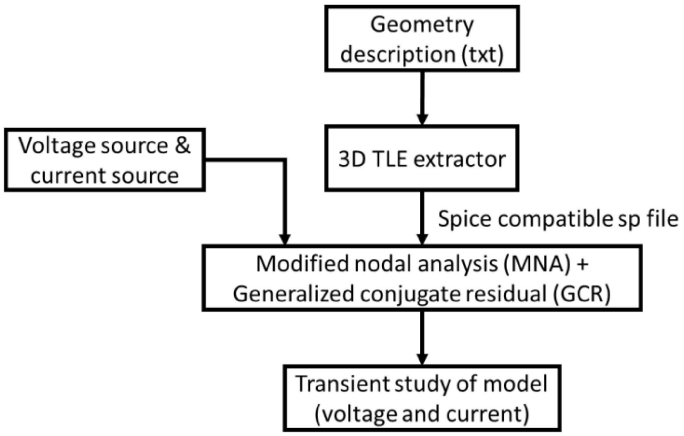


Figure 89 Our workflow for 3D device design

3.4.3)Thermal modeling of VLS circuits

Due to the negligible heat diffusion in the dielectric, the thermal model can be assumed steady. So the temperature distribution T(x) of metal interconnects can be solved by the 1-D heat diffusion equation: [104]

$$\frac{d^2T(x)}{dx^2} = -\frac{g(x,T)}{k_m} \quad (3\text{-}61)$$

Where k_m is the thermal conductivity of the metal [W/mK] and $g(x,T)$ is the heat sources term [W/m3].

Once the defined grid lengths are smaller than the heat characteristic length, the grid can be used to solve both electrical and thermal dissipation[100]. Figure 90 is a typical node of thermal network. It is composed of thermal resistances between neighboring nodes, and another thermal resistance linked to the heat-sink. The VDD layers and GND layers are connected by adding the heat sources P_s and P_J, P_s is the switching power, defined as $P_s(i) = I_0 V_d(i)$, related to the voltage drop at node "i" calculated by electrical equation and P_J is the Joule heating term coming from the power dissipation in the PDN: [104]

$$P_J(i) = \frac{1}{2}\sum_{k=1}^{4}\frac{v_{ik}^2}{R_{ik}} \quad (3\text{-}62)$$

Where k is the four neighboring nodes' index.

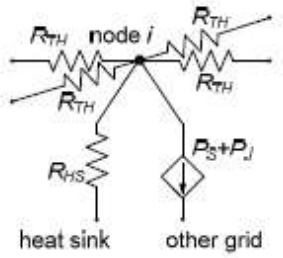


Figure 90 Dynamic thermal elementary cell

The electro-thermal coupling problem is solved in a classical approach: firstly solving the thermal network in room temperature, secondly calculating the temperature dependent electrical resistances R(T), thirdly solving the electrical network, and then getting the voltage. After calculating the thermal heat sources, we can repeat the first 3 steps, and so on. The final temperature and voltage distributions can be obtained when the relative error gets smaller than the predefined error value.

Further investigation of the dynamic analysis can be carried out from the previous static ET analysis by adding the following two steps. The first step is calculating the dynamic elements (capacitors, inductors, etc.…) related voltage drop. The second step is checking if the new thermal distribution is still compatible with the static electro-thermal equilibrium. Thus, with a predefined impedances circuit, a frequency analysis can be then carried out by using the dynamic analysis workflow.

3.4.4) Electro-thermal modeling of VLS circuits

3D integration gives a way to higher performance, increased functionality and heterogeneous implementation. Nevertheless, compared to 2D integration, due to the parasitic, large switching current and longer power delivery path, the power and thermal integrity issues are always the concerns for 3D integration. In this part, we provide an in-depth study of power and thermal issues of 3D integration, especially for the Through Silicon Vias (TSVs). Our study is based on a three layer's system using TSV based technologies. Based on the heat dissipation models, we present a power and thermal integrity analysis of 3-D ICs, especially TSV.

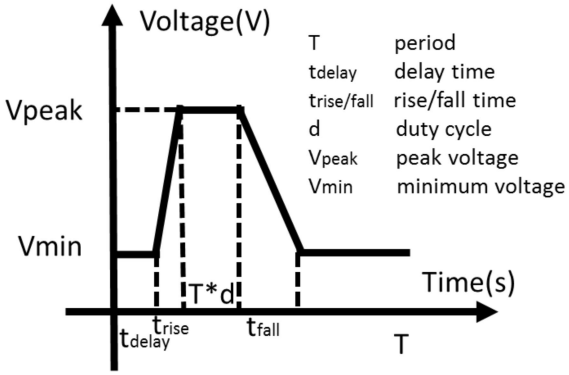


Figure 91 Pulse signal definition

Our study takes the dynamics power analysis into consideration by combining parasitic of the 3D multi-layers system. The extracted parasitic deals with the coplanar line, redistribution layer and TSVs. Coplanar line parasitic are modeled by resistance, capacitance and inductance. Redistribution layer is modeled by resistance, inductance and capacitance. The time dependent voltage sources can be represented by the electrical characteristics: 1) switching frequency; 2) rise and fall times; 3) duty cycle; 4) delay time and 5) peak voltage. Here, in our study, the switching circuits are directly replaced by rectangular waveforms, as shown in Figure 91.

Switching pulse-like voltage sources are expressed as

$$V(t) = \begin{cases} V_{min},\ 0 < t < t_{delay} \\ \left(t - t_{delay}\right) * \frac{V_{peak} - V_{min}}{t_{rise}},\ t_{delay} \le t < t_{delay} + t_{rise} \\ V_{peak},\ t_{delay} + t_{rise} \le t < t_{delay} + t_{rise} + T * d \\ V_{peak} - \left(t - t_{delay} - t_{rise} - T * d\right) * \frac{V_{peak} - V_{min}}{t_{fall}}, t_{delay} + t_{rise} + T * d \le t < t_{delay} + t_{rise} + T * d + t_{fall} \\ V_{min},\ t > t_{delay} + t_{rise} + T * d + t_{fall} \end{cases} \quad (3\text{-}63)$$

The analysis is established on a 3-D multi-layers structure. Models are constructed from 3D-TLE extractor which can extract and generate the SPICE compatible interconnects' model. The

key challenge of this analysis is to calculate simultaneously electrical and thermal analysis. Therefore, the temperature dependent resistivity is used in this analysis.

$$\rho = \rho_0[1 + \beta(T_{emperature} - T_0)] \quad (3\text{-}64)$$

Where ρ_0 (1.53265e-8 Ω m) is the electrical resistivity at T_0 which is 300K and β (0.0067) is the temperature coefficient for electrical resistivity [141]. The electrical resistivity of conductors goes up while temperature increases, and the power supply will be greatly influenced. Besides, the voltage drop and flowing current on the transmission line will cause Joule heating. After a sufficiently long time, the difference of temperature distribution will lead to electron-migration (EM) issues. By this method, electrical and thermal issues are coupled together.

To perform the 3-D multi-layers system for electrical analysis, we adopt Kirchhoff's law to solve the linear equations. These linear equations can be transformed together to one matrix. The matrix formulation follows the rules of modified nodal analysis (MNA) method which is often used for power grid analysis [104][106]. These matrices can be expressed as Laplace transform:

$$[G + sC]x(s) = I(s) \quad (3\text{-}65)$$

Where G is the n-by-n conductance matrix, C is the n-by-n capacitance and inductance matrix, and I is the n-by-1 vector of current sources and voltage sources. $x(s)$ is the n-by-1 vector that represents nodes' voltage and current. To get nodes' voltage drop and current distributions, we solve the electrical power network by inversing this matrix$[G + sC]$. For large system analysis, we use sparse matrix and generalize conjugate residual (GCR) method[209] to ease matrix computations.

As a heat conductor from one layer to another, TSVs can sometimes be very beneficial for dissipating heat away from a hot layer but sometimes they can be harmful to neighboring layers or components. In this work, by following the principle of electrical-thermal duality [106], the heat flow passing through a thermal resistor is equivalent to the current passing through the electrical resistance and temperature difference is equivalent to voltage difference.

Heat is normally generated from the upper layers, and transferred through TSVs and other layers (for example, isolation layers) to the silicon substrate. Isolation layers have much lower thermal conductivities than that of silicon, so they act as thermal barriers. The voltage changes in the switching circuits will contribute to the heat generation. TSVs, redistribution layers, coplanar lines and heat sink are modeled as thermal resistances in order to conduct the vertical and lateral heat flows in the 3D system. Due to the difference between TSVs' vertical thermal resistances and other material layers' thermal resistances, heat dissipates at different rates. The equivalent thermal resistances are represented as the parallel connection of TSVs' resistances and other layers' thermal resistances. The temperature of heat sink is assumed to be the ambient temperature. Thanks to the principle of electrical-thermal duality, the thermal network can also be solved by using MNA method. The nodes' thermal linear equations can be merge to the following equation:

$$G_{th}T_{emp} = Q \tag{3-66}$$

Where G_{th} is the thermal resistance matrix of size m-by-m and m is the number of nodes on the 3D system. T_{emp} is the m-by-1 vector of temperature nodes and Q is the m-by-1 vector for heat sources.

We develop an electrical and thermal analysis flow to calculate the electro-thermal coupling effect of a 3D system. The proposed method is an iterative process and Figure 92 shows the electrical and thermal analysis flow.

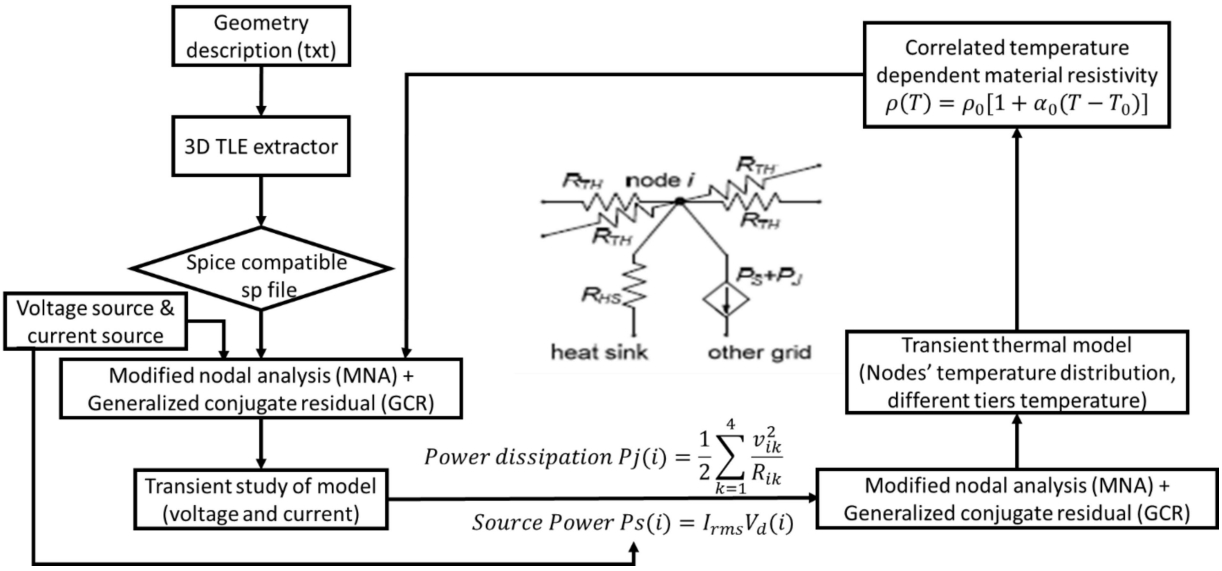


Figure 92 3D IC Electro-thermal coupling flow

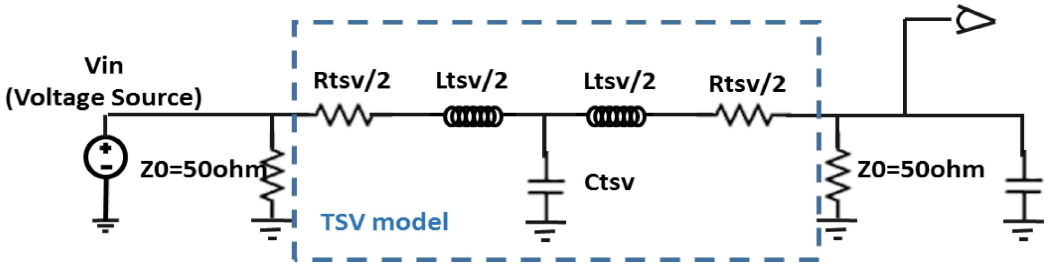
Electrical analysis is a transient analysis, the voltage drop on the metal tracks will result in an elevation of temperatures. The increase in temperature is then treated as a thermal source and applied to the thermal analysis step. Thermal analysis provides temperature distribution for the different layers and TSVs, where altered temperatures will change conductors' resistivity and then influence electrical analysis. The iterative calculation of resistivity and temperature will converge when there are no more changes on voltage drop and temperature distribution. Here, the thermal analysis is a steady state analysis which captures the temperature distribution from a given electrical network. This method is limited to capture the dynamic thermal distribution. However, as fast and accurate capturing of temperature distribution is always our purpose. The 1D static thermal analysis is a viable approach. We adopt the modified nodal analysis as described in the previous to perform efficient electrical and thermal networks analysis.

3.4.4.1) Case I: One via model

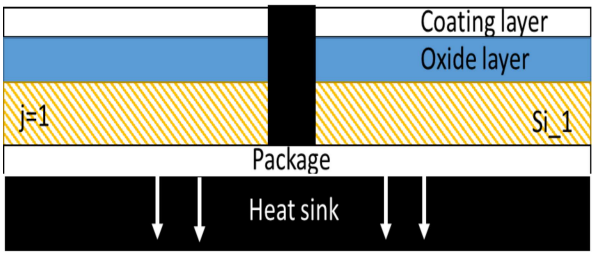
The one via model can be shown in Figure 93(b). The chip is composed of one coating layer, one oxide layer and one silicon layer, the center is a copper TSV. And the bottom is attached to a

package and outside the package, a heatsink is used. The chip's size is 10mmX10mm, the silicon layer's thickness is 50µm, the coating layer and insulation layer have respectively a thickness of 2µm and 8.8µm. TSV's surface ratio r is fixed to 0.01.

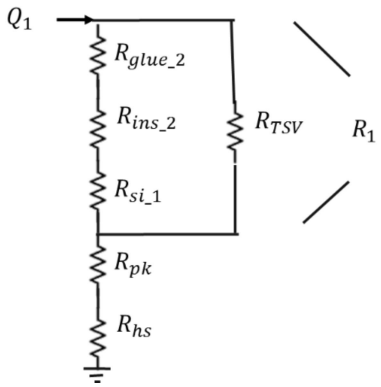
The electrical circuit and thermal circuit are shown in Figure 93(a) (c). We input a pulse signal (defined as previous part), and parallel a 50 ohm's resistance at the input and output, and a 150fF capacitance at output in order to see the output signal. Here, the resistance of TSV is about 0.0052e-4 ohm, so in compare with 50 ohm, the TSV resistance is too small. So the parallel circuit's effective resistance depends on the TSV resistance (frequency dependent straight wire formula (2-57) and (2-58)), and the parallel connection of 50ohm resistance will not change the output signal. The current will change to heat when passing by the resistance of TSV. And the generated heat is dissipated in the 3D geometry. The thermal path is composed of TSV conduction and the other 3 layers' serial heat conduction, the heat pass separately by the series of 3 layers and also by the TSV (because of the copper's nice heat conductivity). And then the heat is collected in the package level, and conducted through the package to the heatsink. The package and heatsink have also their own effective heat conductivities, especially for the heatsink, it has a very high heat conductivity and so a very low thermal resistance. And the ambient temperature is about 300K.



(a)



(b)



(c)

Figure 93 (a) Electrical compact mode (b) 2D Geometry (c) Thermal compact model of one via model

Table 13 One via model's geometry parameters

Geometry	
Silicon layer thickness (lsi)	50um
Glue layer thickness (lglue)	2um
Insulation layer thickness (lins)	8.8um
Length of chip (Lx)	10mm
Width of chip (Ly)	10mm
TSV number	1
TSV ratio (r)	0.01

As shown is the following Figure 94, the S parameter is calculated by using ADS simulator.

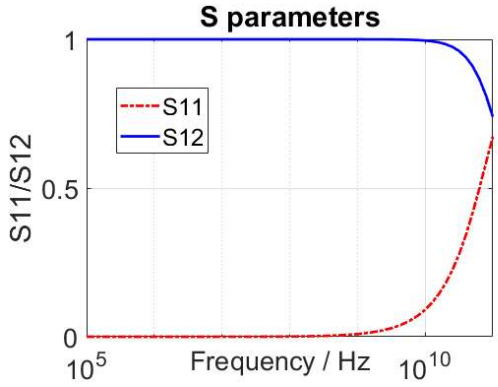


Figure 94 S parameters of 1-TSV model from ADS (valid for frequency below 20GHz and of quasi-static assumption)

Figure 95 shows the 2.5GHz's signal transmisison effects. Figure 95 (a) shows the comparison of input and output signal. Figure 95 (b) shows respectively the top of coating layer, the bottom of TSV and the bottom side of packaging's temperature. Figure 95 (c) shows the voltage transmission change when considering electro-thermal coupling effects between ADS (without Electro-thermal consideration), MNA method (with Electro-thermal consideration) and MNA (without Electro-thermal consideration). Figure 95 (d) is the output voltage error without considering electrothermal effect. As we can see from the result of 2.5GHz study, the output signal has almost the same waveform than the input signal, the temperature change in the circuit is 0K. The ADS simulated result has a good fit with our simulator, and after considering the electro-thermal effect, the maximum output change is 0.2%, which can be neglected.

The output voltage error Err can be defined as

$$\mathrm{Err} = \frac{\max(abs(V1-V2))}{Vmax\_in} \quad (3\text{-}67)$$

Where $Vmax\_in$ is the input maximum voltage, $V1$ is the first transient voltage, $V2$ is the second transient voltage.

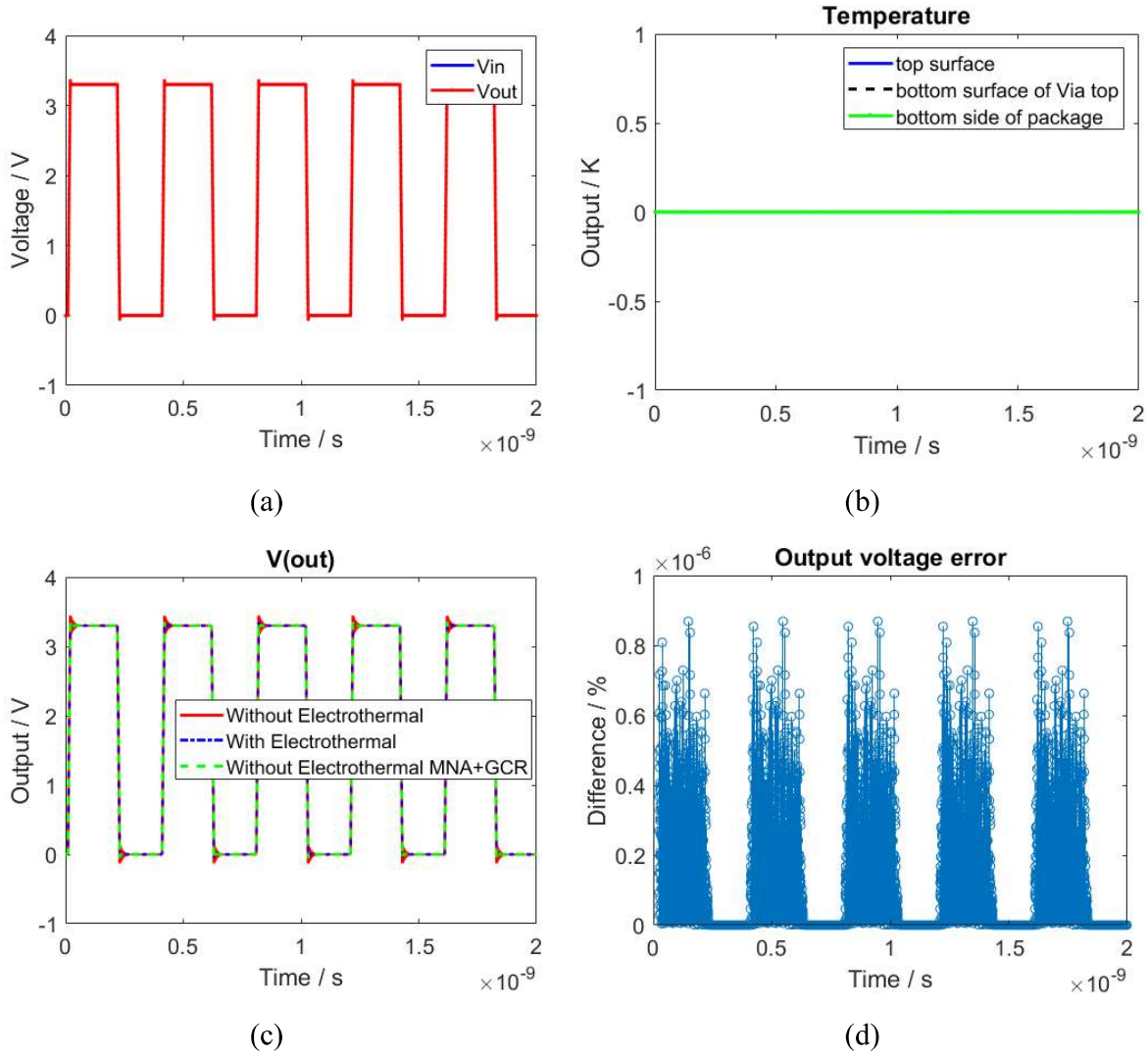
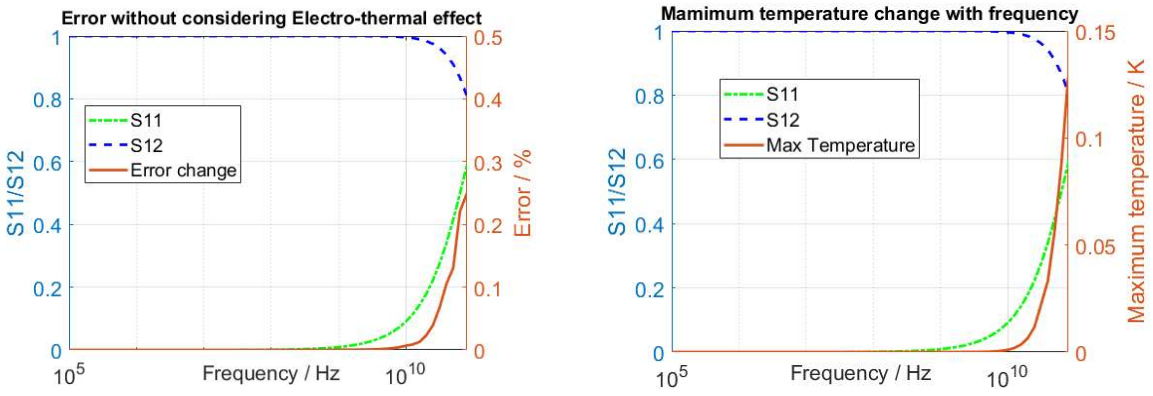


Figure 95 Signal transient Integrity analysis for 1-TSV model 2.5GHz (a) Input vs Output signal (b) Maximum temperature rise (c) Comparison between ADS(without Electro-thermal consideration), MNA method (with Electro-thermal consideration) and MNA (without Electro-thermal consideration) (d) Output Voltage Error

From the above results, the one TSV model does not have electro-thermal effect at very low working frequency. For some period of frequencies, the output frequency increase linearly, and it will generate a lot of heat and increase the via's temperature. Therefore, we find out that the electro-thermal effect has a relationship with the trend of S parameters. The S parameters stay stable at low frequency and very high frequency, but for a band of frequency, it changes dramatically. We can superpose the S parameters with the error curves and maximum temperature curve. The

following Figure 96 shows the result. But due to the non-linear system, from 20GHz to 10THz, the results are now should use full wave models for electrical study. The current result is not valid in this band of frequencies.

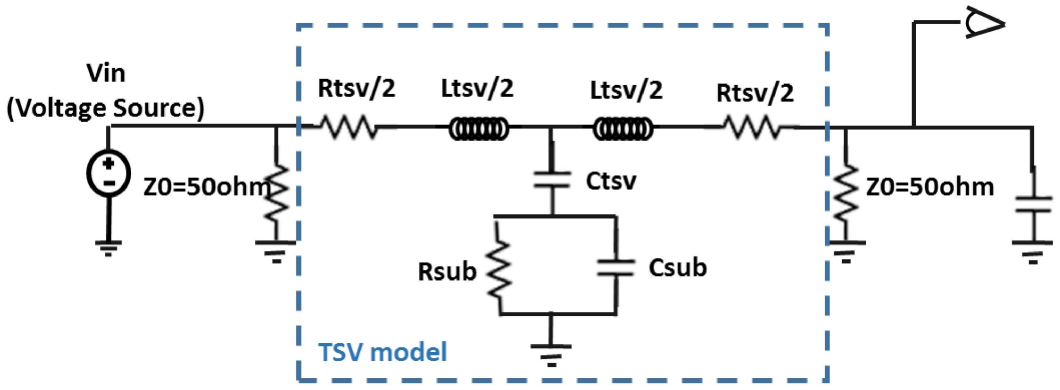


(a) (b)

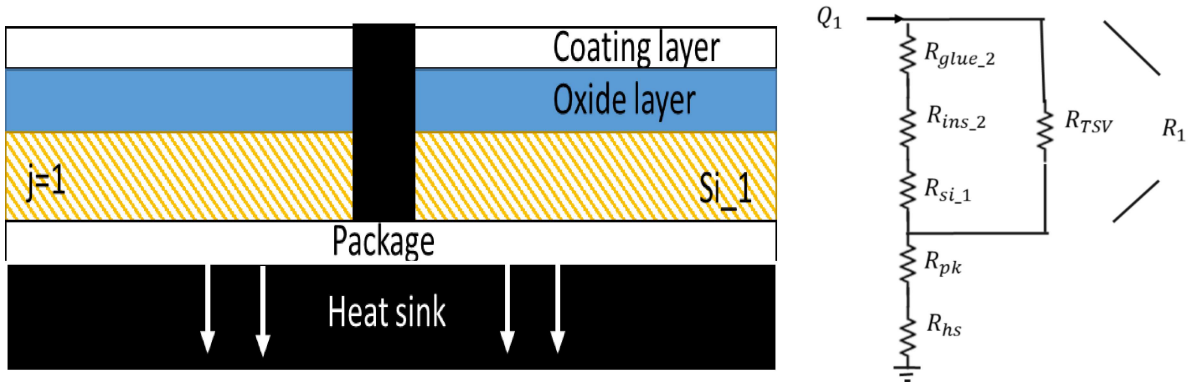
Figure 96 S parameters with (a) error curve (b) maximum temperature curve for one via model (valid for frequency below 20GHz and of quasi-static assumption)

As we imagined, the S parameters have really a good tendency with the electro-thermal effects. Strong electro-thermal effects appear while S parameters change.

3.4.4.2) Case II: One TSV model with substrate RC effect



(a)



(b) (c)

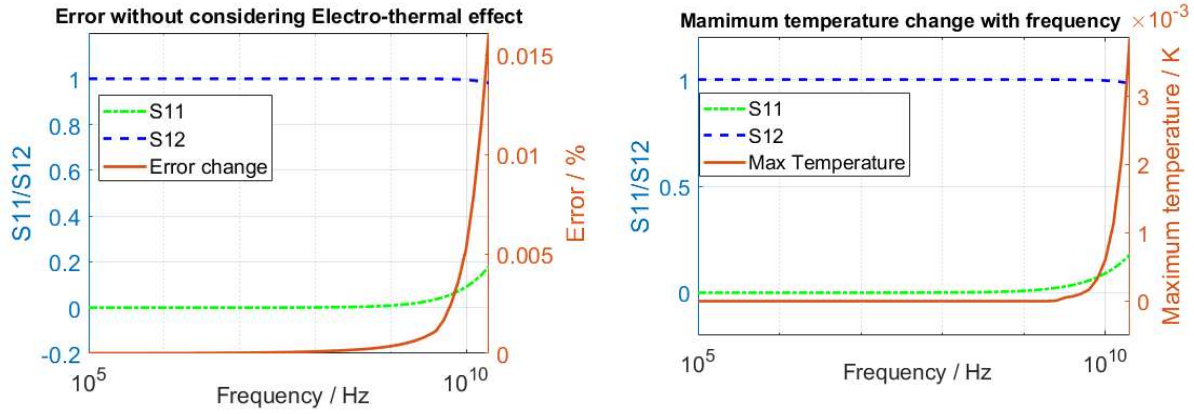
Figure 97 Figure 30 (a) Electrical compact mode (b) 2D Geometry (c) Thermal compact model of one via with substrate model

The only difference between this model and previous model is the substrate. In the previous model, the substrate is treated directly as a ground node. But in this model, the substrate is highly doped. It is treated as a conductor with a very low resistivity (1e-4 ohm·m). The substrate is expressed as a RC parallel model. The substrate resistance and capacitance can be expressed by the following equations[115]

$$C_{Si\_sub} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,si}}{cosh^{-1}(\frac{p_{TSV}}{d_{TSV}})} \times h_{TSV}[F] \quad (3\text{-}68)$$

$$G_{Si\_sub} = \frac{\pi \times \sigma_{si}}{cosh^{-1}(\frac{p_{TSV}}{d_{TSV}})} \times h_{TSV}[S] \quad (3\text{-}69)$$

Figure 98 shows the results. These two figures show that by adding a highly doped substrate, we can reduce the electro-thermal effect, especially in the band of frequency where S parameters change heavily. And the maximum temperature has been reduced to 5e-4K, which is about 3 times less than the one TSV model, and maximum error has been reduced to a half, about 1.5e-5%. Thus, by adding a highly doped substrate, the electro-thermal heating effect can be effectively reduced.

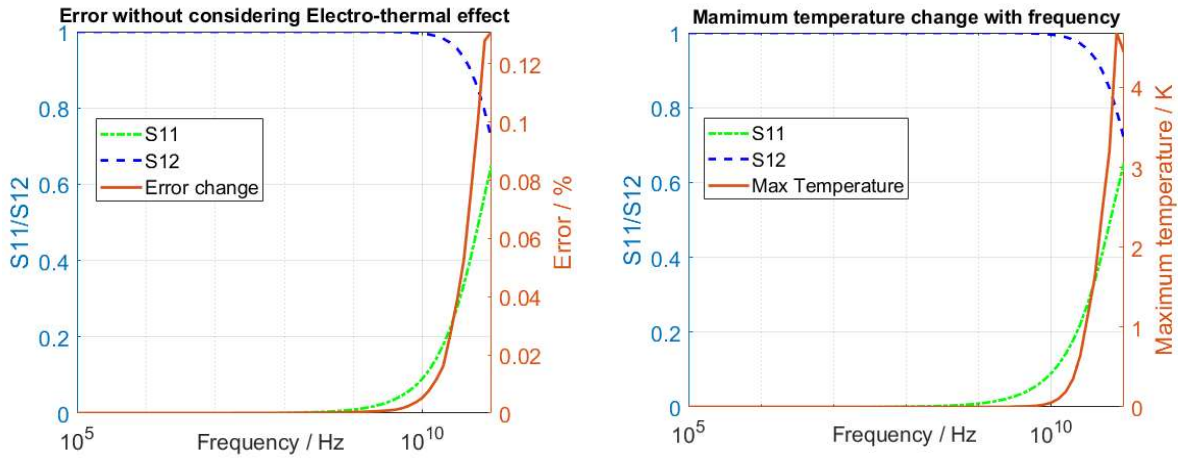


(a) (b)

Figure 98 S parameters with (a) error curve (b) maximum temperature curve for one via with substrate model (valid for frequency below 20GHz and of quasi-static assumption)

3.4.4.3) Case III: One TSV model with a very high thermal resistance

In order to get a higher temperature and see a more obvious difference of signal transmission, we set Rhs and Rpk in the Figure 93 (c) to 2000 K/W respectively.



(a) (b)

Figure 99 S parameters with (a) error curve (b) maximum temperature curve for one via with high thermal resistance model (valid for frequency below 20GHz and of quasi-static assumption)

From the above Figure 99, we can see that, the error curve and maximum temperature curve have always the same tendency. They keep stable at low frequency. Once the S parameters change, the two curves change dramatically. Even though we have studies the electro-thermal modeling until 10THz, due to the non-linear system, from 20GHz to 10THz, we should use full wave models for electrical study. But at least, it works for the frequencies less than 15GHz, sufficient for our industrial collaborator, for the next generation of mobile sample, for instance. Here, we will not speak on quantic interference of temperature, for nano devices. And this analysis method will be useful in analyze of thermo-mechanical effect, which will be introduced in the chapter 5.

3.5) Conclusion

In this work, 3D IC analytical models and electrical-thermal analysis technique, for substrate, thermal connections (3D via) and system level 3D PDN, are introduced and used to explore power and thermal integrity issues in 3D integration. The 3D IC analytical models consider also the electro-thermal effects of TSV parasitic. We provide an extensive study of power and thermal dissipation issues in 3D integration considering several aspects such as:

• Single and multi-layer auto-heating effects on 3D power and thermal dissipation;

• TSVs and substrate impact on power and thermal integrity and their design implications;

• Heat sink's thermal conductivity's influence to the electro-thermal effects.

We combine switching frequency and electro-thermal effects together. And by comparing with S parameters, we found out that the electro-thermal effects appear only when S parameters change, and the reduction of thermal resistance and the increase of doping concentration of substrate will restrain the electro-thermal signal integrity problem.

In fact, we can use more layers, then with lower thicknesses. Here, we did not consider the temperature-dependent material characteristics' change or we can also say that the temperature is fixed low, so the change of the material's characteristics is weak. Here, we just give a solution for each uniform layer and low temperature design.

In our study, we adopt linear model; we mean that the global effects of substrate and connections can be split. But, if the connections become very important, we cannot dissociate substrate with TSV, RDL, etc. Intercorrelation terms do intervene; the system can be approached by non-linear models.

Moreover, our extractor (3D-TLE) is now efficient, although some models are, by now, roughly simple. But, the industry wants simple compact models, and then, we should keep the simplicity, by considering, as well as possible, the in-depth physics.

Chapter 4: Heat pipe Simulation

Advances in the computational performance of electronic devices have created an urgent need for improved methods of passive thermal management, particularly in 3D systems. This has led to renewed interest in the use of vapor chambers as heat spreaders in applications ranging from mobile devices to high-performance-computing and power electronics systems. While detailed numerical models of vapor chamber operation have been developed, an easy modeling with low computational cost method has also been implemented for parametric study and quick assessment of vapor chamber performance in system-level models.[198], [202], [203], [207]–[212], [216]–[218], [219]–[226]

4.1) Introduction

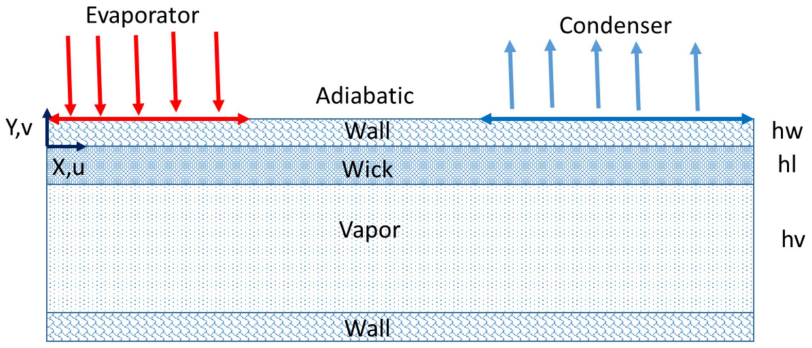
Micro/nano flat heat pipes (FHP) are an effective passive heat transfer technology for high heat flux electronic devices, especially CPU, MPU. Because of the high thermal conductivity, reliability and low weight penalty, they are treated as a very proficient high power cooling system. A FHP is an enclosed vapor chamber whose inner and outer surface is covered respectively with porous medium and thermal conductive materials. Heat sources and heat sinks are located on the outer surface of FHP, with the rest parts thermally insulated. The fluid in the wick is evaporated by the heat sources, the generated vapor increases locally the pressure, and the pressure difference pushes vapor from the evaporator to the condenser, where the vapor is condensed and changes to fluid in the wick. Once again, the condensed liquid increases the local pressure in the wick, and the pressure difference in the wick pumps the liquid back to the evaporation side. This phase-change circulation of FHP will continue until the heat sources disappear or capillary pressure cannot be offered by liquid [230]. For the working fluid, water, acetone, ethanol or methanol are more commonly used in the electronic devices. [215], [218], [220], [226], [228], [230], [234], [238], [239], [264]

Researches on FHP have been conducted to characterize the cooling performances of micro heat pipes. For pre-study the thermal performance of heat pipes, many researchers have suggested simplified 1D theoretical models [198], [213], [228], [231], [232], however, the simplified 1D model is no longer accurate for the extra-thin FHP.

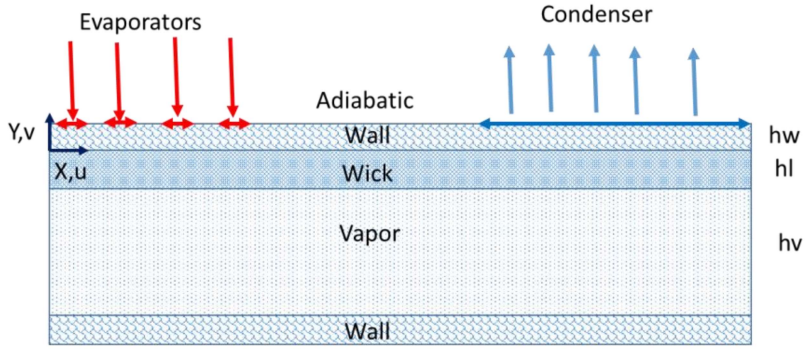
In the current work, a computational low-cost FHP model is developed, targeting the geometries and operating conditions. The model considers mass flow, momentum changes, and energy transport in the vapor chamber, wall, and wick, as well as phase change at the wick-vapor interface. [229]

The studied configurations of flat heat pipes are shown in Figure 100. Figure 100 a, b, c presents respectively the configurations of flat heat pipes with a single heat source, multiple heat sources, and a heat source on one side and a heat sink on the other side. All the studies are based on the

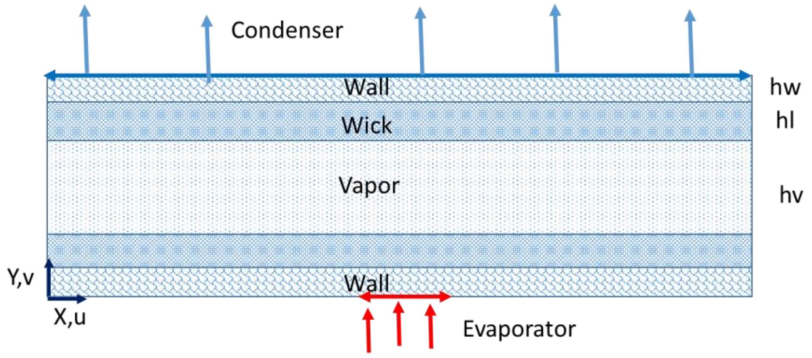
assumptions of steady-state and incompressible laminar flow. And the fluid of wick is treated as saturated, so as that the heat is directly evacuated through the liquid/vapor evaporation process.



(a) Configuration I



(b) Configuration II



(c) Configuration III

Figure 100 Flat heat pipe with different heating/cooling configurations: a) configuration I, single heat source and sink at the top; b) configuration II, multiple heat sources and sink at top; c) configuration III, heat source at the bottom and heat sink on the top.

4.2) Configuration I & II 2D simulation

4.2.1)2D heat pipe Analytical solution

- Thermal Conduction in wall[221]

The non-dimensional temperatureϑ and coordinates are defined as:

$$\vartheta = \frac{k_w}{q_e h_w}(T - T_{sat}) \tag{4-1}$$

$$\mathrm{X} = \frac{x}{l}; Y = \frac{y}{h_w}; H_w = \frac{h_w}{l}; H_l = \frac{h_l}{l}; L_e = \frac{l_e}{l}; L_c = \frac{l_c}{l}; \gamma = \frac{L_e}{L_c} \tag{4-2}$$

The dimensionless 2D steady-state heat conduction equation in the wall can be written as:

$$\frac{\partial^2\theta}{\partial X^2} + \frac{1}{H_w^2}\frac{\partial^2\theta}{\partial Y^2} = 0 \tag{4-3}$$

The boundary condition at the boundary (X=0 and X=1) are

$$\frac{\partial\theta}{\partial X} = 0 \tag{4-4}$$

At the wick/wall interface (Y=0), the thermal boundary condition can be determined by assuming linear temperature profile and constant saturation temperature at the liquid-vapor interface. The boundary condition can be written as

$$\frac{\partial\theta}{\partial Y} = \frac{k_{eff}H_w}{k_w H_l}\theta \tag{4-5}$$

The boundary condition at the outer wall (Y=0) are constant heat fluxes in the evaporators and the condenser, which can be located at different locations on the heat pipe, and a heat flux equal to zero in the adiabatic sections (the rest of the surface). This is shown as：

$$\frac{\partial\theta}{\partial Y} = \begin{cases} 1 \ evaporator \\ 0 \ adiabatic \\ -\gamma \ condenser \end{cases} \tag{4-6}$$

The non-dimensional temperature for configurations I and II can be expressed by an infinite Fourier series as:

$$\theta(X,Y) = \sum_{m=1}^{\infty} A_m(Y)\cos(m\pi X) \tag{4-7}$$

The non-dimensional input heat flux depends on the location of heat sources and sinks, and can be written as follows:

$$\frac{\partial\theta}{\partial Y} = \sum_{m=1}^{\infty} B_m\cos(m\pi X) \tag{4-8}$$

where

$$B_m = \frac{2}{m\pi}\{\sin(m\pi L_{2e}) - \sin(m\pi L_{1e}) + \sin(m\pi L_{4e}) - \sin(m\pi L_{3e}) + \sin(m\pi L_{6e}) - \sin(m\pi L_{5e}) + \sin(m\pi L_{8e}) - \sin(m\pi L_{7e}) - \gamma[\sin(m\pi L_{2c}) - \sin(m\pi L_{1c})]\} \tag{4-9}$$

In which $L_{1e}, L_{2e}, L_{3e}, L_{4e}, L_{5e}, L_{6e}, L_{7e}, L_{8e}, L_{1c}$ *and* L_{2c} express the locations of the heat sources and heat sink.

Substituting (4-7) and (4-8) into (4-3), (4-5) and (4-6), yields the following expression for coefficient Am:

$$A_m(Y) = B_m \frac{\left(m\pi+\frac{k_{eff}}{k_W H_l}\right)\exp(m\pi H_W Y)+(m\pi-\frac{k_{eff}}{k_W H_l})\exp(-m\pi H_W Y)}{m\pi H_W[\left(m\pi+\frac{k_{eff}}{k_W H_l}\right)\exp(m\pi H_W Y)-(m\pi-\frac{k_{eff}}{k_W H_l})\exp(-m\pi H_W Y)]} \quad (4\text{-}10)$$

- Vapor flow [221]

A parabolic velocity profile is used for vapor flow within the heat pipe. The vapor velocity The velocity distribution is represented by a product in the x and y directions:

$$u_v(x,y) = -6U_v(x)[\left(\frac{h_l}{h_v}\right)^2 + \frac{h_l}{h_v} + \left(1+2\frac{h_l}{h_v}\right)\left(\frac{y}{h_v}\right) + (\frac{y}{h_v})^2] \quad (4\text{-}11)$$

Where $U_v(x)$ is the local mean velocity along the x direction.

The continuity equation for the two-dimensional incompressible vapor flow can be integrated with respect to y to determine $U_v(x)$

$$\int_{-(h_l+h_v)}^{-h_l}(\frac{\partial u_v}{\partial x}+\frac{\partial v_v}{\partial y})dy = \int_{-(h_l+h_v)}^{-h_l}\frac{\partial u_v}{\partial x}dy + v_{v,I}(-h_l) - v_v(-(h_l+h_v)) \quad (4\text{-}12)$$

Where $v_{v,I}$ represents the vapor interfacial velocity. The heat flux normal to the liquid-vapor interface, q_I can be calculated from the conduction model with the assumption of linear temperature profile across the wick:

$$v_{v,I}(-h_l) = \frac{q_I}{\rho_v h_{fg}} = q_e \frac{k_{eff}h_w}{\rho_v h_{fg} k_w h_l}\sum_{m=1}^{\infty} A_m(0)\cos(\frac{m\pi x}{l}) \quad (4\text{-}13)$$

$$v_v(-(h_l+h_v) = 0 \quad (4\text{-}14)$$

Integrating (4-14) with respect to x and using the boundary condition at the beginning of the evaporator $u_v = 0$, will result in an expression for $U_v(x)$:

$$U_v(x) = q_e \frac{k_{eff}h_w}{\rho_v h_{fg} k_w h_l}\sum_{m=1}^{\infty}(\frac{l}{m\pi})A_m(0)\sin(\frac{m\pi x}{l}) \quad (4\text{-}15)$$

Therefore, the quasi-two-dimensional velocity profile is:

$$u_v(x,y) = -6q_e \frac{k_{eff}h_w}{\rho_v h_{fg} k_w h_l}\sum_{m=1}^{\infty}\left(\frac{l}{m\pi}\right)A_m(0)\sin\left(\frac{m\pi x}{l}\right) \times [\left(\frac{h_l}{h_v}\right)^2 + \frac{h_l}{h_v} + \left(1+2\frac{h_l}{h_v}\right)\left(\frac{y}{h_v}\right) + \left(\frac{y}{h_v}\right)^2] \quad (4\text{-}16)$$

The boundary layer form of the x direction momentum equation for steady-state incompressible laminar vapor flow can be integrated to obtain the vapor pressure distribution:

$$\rho_v \int_0^x \int_{-(h_l+h_v)}^{-h_l} \frac{\partial (u_v)^2}{\partial x} dxdy + \rho_v \int_0^x \int_{-(h_l+h_v)}^{-h_l} \frac{\partial (u_v v_v)}{\partial y} dxdy = \int_0^x \int_{-(h_l+h_v)}^{-h_l} -\frac{\partial p_v}{\partial x} dxdy + \mu_v \int_0^x \int_{-(h_l+h_v)}^{-h_l} \frac{\partial^2 (u_v)}{\partial y^2} dxdy \quad (4\text{-}17)$$

Assuming the constant vapor pressure at each cross-section, and utilizing the boundary conditions at the beginning of the evaporator, $u_v = 0$ and $p_v = p_{ref}$yields

$$p_v = p_{ref} + q_e \frac{k_{eff} h_w}{\rho_v h_{fg} k_w h_l h_v^3} \sum_{m=1}^{\infty} A_m(0) \left[\cos\left(\frac{m\pi x}{l}\right) - 1\right] + 18\rho_v U_v^2 \left[\frac{1}{5}\left(\frac{h_l}{h_v}\right)^5 + \frac{1}{30}\right] \quad (4\text{-}18)$$

Where U_v is obtained from (4-15).

The temperature drop in the vapor can be related to the pressure drop in the vapor region by applying the Clausius-Clapeyron equation and using the ideal gas law:

$$T_v = \frac{1}{\frac{1}{T_{ref}} - \frac{R}{h_{fg}} \log\left(\frac{p_v}{p_{ref}}\right)} \quad (4\text{-}19)$$

Where R is the ideal gas constant, h_{fg} is the latent heat, and p_v is the pressure drop obtained from (4-18).

- Liquid flow [221]

The continuity equation for the incompressible liquid flow can be integrated with respect to y to obtain the liquid axial velocity $u_l(x)$:

$$\int_{-h_l}^{0} \left(\frac{\partial u_v}{\partial x} + \frac{\partial v_v}{\partial y}\right) dy = -v_{l,I}(-h_l) - h_l \frac{du_l}{dx} \quad (4\text{-}20)$$

where $v_{l,I}$ represents the interfacial velocity (normal to the liquid vapor interface) for the liquid and is related to the vapor interfacial velocity by:

$$\rho_l v_{l,I} = \rho_v v_{v,I} \quad (4\text{-}21)$$

The axial liquid velocity can be calculated by integrating (4-20) with respect to x using the velocity boundary condition at the beginning of the evaporator (x = 0), $u_l = 0$:

$$u_l(x) = q_e \frac{k_{eff} h_w}{\rho_v h_{fg} k_w h_l^2} \sum_{m=1}^{\infty} \left(\frac{l}{m\pi}\right) A_m(0) \sin\left(\frac{m\pi x}{l}\right) \quad (4\text{-}22)$$

The one-dimensional steady-state conservation of momentum for incompressible liquid flow in the wick can be expressed by Darcy's law, assuming negligible inertial effects in comparison to viscous losses, as:

$$\frac{dp_l}{dx} = -\frac{\mu_l u_l}{K} \quad (4\text{-}23)$$

In which the permeability K is calculated for a mesh screen as:

$$K = \frac{d^2\varphi^3}{122(1-\varphi)^2} \quad (4\text{-}24)$$

$$\varphi \approx 1 - \frac{1.05\pi Nd}{4} \quad (4\text{-}25)$$

The liquid pressure is obtained by integrating (4-24) and utilizing the pressure boundary condition at the end of the condenser (x=l), $p_l = p_v$:

$$p_l = q_e \frac{\mu_l k_{eff} h_w}{\rho_l h_{fg} k_w K h_l^2} \sum_{m=1}^{\infty} \left(\frac{l}{m\pi}\right)^2 A_m(0) \left[\cos\left(\frac{m\pi x}{l}\right) - \cos(m\pi)\right] + p_{ref} + q_e \frac{12\mu_v k_{eff} h_w}{\rho_v h_{fg} k_w h_v^3 h_l} \sum_{m=1}^{\infty} \left(\frac{l}{m\pi}\right)^2 A_m(0)[\cos(m\pi) - 1] \quad (4\text{-}26)$$

- Capillary pressure [221]

$$p_{cap} = p_v - p_l \quad (4\text{-}27)$$

4.2.2)FEM simulation[141]

The numerical model employed here is adopted from [222]. In summary, the continuity, momentum, and energy equations are solved in the wall, wick, and vapor regions of the FHP. Evaporation and condensation at the interface follow a kinetic theory-based formulation that depends on the interface temperature calculated from a local energy balance. The vapor density is calculated from the vapor pressure and local temperature using the ideal gas law; the liquid mass is adjusted to conserve mass. All other properties are fixed to be constant. [214]

The liquid and vapor flow are considered to be laminar and incompressible. The continuity equation is as follows:

$$\varphi \frac{\partial \rho}{\partial t} + \rho \nabla \cdot \left(\vec{V}\right) = 0 (in\ stationary, no\ time\ term) \quad (4\text{-}28)$$

The term $\partial\rho/\partial t$ accounts for the increase or reduction of mass in the fluid. The momentum equations with a Brinkman–Forchheimer extended Darcy model for fluid flow in the wick region and the vapor core are:

$$\frac{1}{\varepsilon_p}\rho\frac{\partial \vec{V}}{\partial t} + \frac{1}{\varepsilon_p}\rho\left(\vec{V}\cdot\nabla\right)\vec{V}\frac{1}{\varepsilon_p} = \nabla\cdot\left[-pI + \mu\frac{1}{\varepsilon_p}\left(\nabla\vec{V} + \left(\nabla\vec{V}\right)^T\right)\right] - \left(\mu k^{-1} + \beta_F\left|\vec{V}\right|\right)\cdot\vec{V} \quad (4\text{-}29)$$

Or

$$\frac{1}{\varepsilon_p}\rho\frac{\partial u}{\partial t} + \frac{1}{\varepsilon_p}\rho\left(u\cdot\frac{\partial}{\partial x} + v\cdot\frac{\partial}{\partial y}\right)u\frac{1}{\varepsilon_p} = \frac{\partial p}{\partial x} + \nabla\cdot\left[\mu\frac{1}{\varepsilon_p}\left(\left(\frac{\partial u}{\partial x}, \frac{\partial u}{\partial y}\right) + \left(\frac{\partial u}{\partial x}, \frac{\partial v}{\partial x}\right)\right)\right] - \left(\mu k^{-1} + \beta_F\left|\vec{V}\right|\right)\cdot u$$

$$\frac{1}{\varepsilon_p}\rho\frac{\partial v}{\partial t}+\frac{1}{\varepsilon_p}\rho\left(u\cdot\frac{\partial}{\partial x}+v\cdot\frac{\partial}{\partial y}\right)v\frac{1}{\varepsilon_p}=\frac{\partial p}{\partial y}+\nabla\cdot\left[\mu\frac{1}{\varepsilon_p}\left(\left(\frac{\partial v}{\partial x}+\frac{\partial v}{\partial y}\right)+\left(\frac{\partial u}{\partial y}+\frac{\partial v}{\partial y}\right)\right)\right]-\left(\mu k^{-1}+\beta_F\left|\vec{V}\right|\right)\cdot v \quad (4\text{-}30)$$

In the vapor core, permeability $k=\infty$ and porosity $\varphi=1$.

The energy equation in the wall, wick and vapor core is

$$\frac{(\rho C)_m\partial T}{\partial t}+(\rho C)_m\vec{V}\cdot\nabla T=\nabla\cdot\left(k_{eff}\nabla T\right)+Q_{vd} \quad (4\text{-}31)$$

Where $(\rho C)_m$ assumes different values in the wall, wick, and vapor core

Wall: $(\rho C)_m=(\rho C)_s$
Wick: $(\rho C)_m=(1-\varphi)(\rho C)_s+\varphi(\rho C)_l$
Vapor core: $(\rho C)_m=(\rho C)_v$

All thermos-physical properties are assumed to be constant at a given time instant. The physical setting can be shown in the following Figure 101.

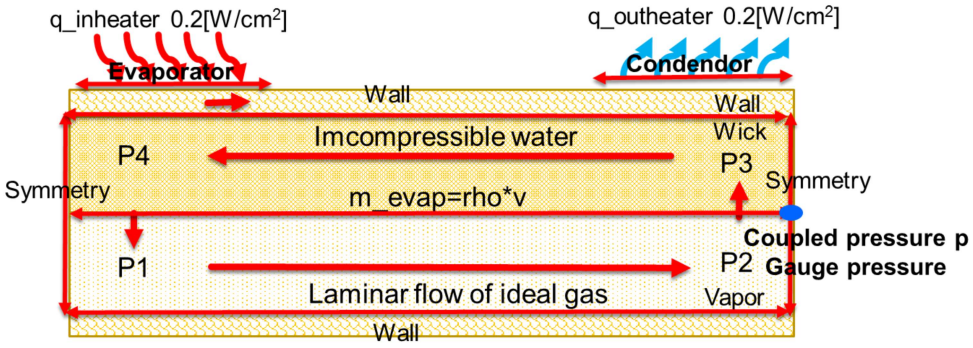


Figure 101 Laminar flow setting of the vapor core

The mass flux rate due to phase change at the wick/vapor interface is evaluated using the difference between the local interface temperature and the local vapor-core saturation temperature [222] as:

$$\dot{m}''=\frac{2\sigma}{2-\sigma}\frac{h_{fg}\rho_v}{T_v^{1.5}}\left(\frac{Mn}{2\pi R_{const}}\right)^{0.5}(T_{int}-T_{sat}) \quad (4\text{-}32)$$

$\dot{m}''>0$ for the evaporation part and contrary for the condenser part.

A positive value indicates evaporation, while a negative value indicates condensation. The value of σ is chosen to be 0.03[231]. The saturation temperature in the vapor core is computed using the Clausius-Clapeyron equation.

$$\frac{R\_const}{h_{fg}M_n}\ln\left(\frac{P_{vap}}{P_0}\right)=\frac{1}{T_0}-\frac{1}{T_{vap}} \quad (4\text{-}33)$$

Or, with the derivative form:

$$\frac{dP_{vap}}{dT_{sat}} = \frac{M_n h_{fg} P_{vap}}{R\_const T_{sat}^2} \quad (4\text{-}34)$$

The boundary conditions for the vapor core specify that there is no slip in velocity at the thermally insulated lateral sidewalls.

$$at\ x = 0, u = v = 0;\ \frac{\partial T}{\partial x} = 0 \quad (4\text{-}35)$$

$$at\ x = L_x, u = v = 0;\ \frac{\partial T}{\partial x} = 0 \quad (4\text{-}36)$$

$$at\ y = 0, u = v = 0;\ \frac{\partial T}{\partial y} = 0 \quad (4\text{-}37)$$

$$at\ y = L_y, u = v = 0;\ \frac{\partial T}{\partial y} = 0 \quad (4\text{-}38)$$

At the lateral and bottom face of the wall, a thermal insulation is set.

$$u = v = 0;\ \frac{\partial T}{\partial x} = \frac{\partial T}{\partial y} = 0 \quad (4\text{-}39)$$

At wick-vapor interface

$$u = v = 0; q_{evap} = \dot{m}'' \cdot h_{fg} \quad (4\text{-}40)$$

$$(\rho C_p \vec{V})_{wick} \cdot \nabla T + \nabla \cdot (k_{wick} \nabla T) = -q_{evap} + Q_{vd} \quad (4\text{-}41)$$

$$(\rho C_p \vec{V})_{v} \cdot \nabla T + \nabla \cdot (k_{v} \nabla T) = q_{evap} + Q_{vd} \quad (4\text{-}42)$$

At the upper wall: The evaporator section has a constant heat flux condition

$$k_{wall} \frac{\partial T}{\partial y} = q_e; 0 \le x \le L_e \quad (4\text{-}43)$$

In the adiabatic section

$$\frac{\partial T}{\partial y} = 0; u = v = 0; L_e \le x \le L_e + L_a \quad (4\text{-}44)$$

The condenser section has a convection condition with heat transfer coefficient h_c and ambient temperature T_c

$$-k_{wall} \frac{\partial T}{\partial y} = h_c (T - T_c); x > L_e + L_a \quad (4\text{-}45)$$

The thermal setting can be shown as Figure 102.

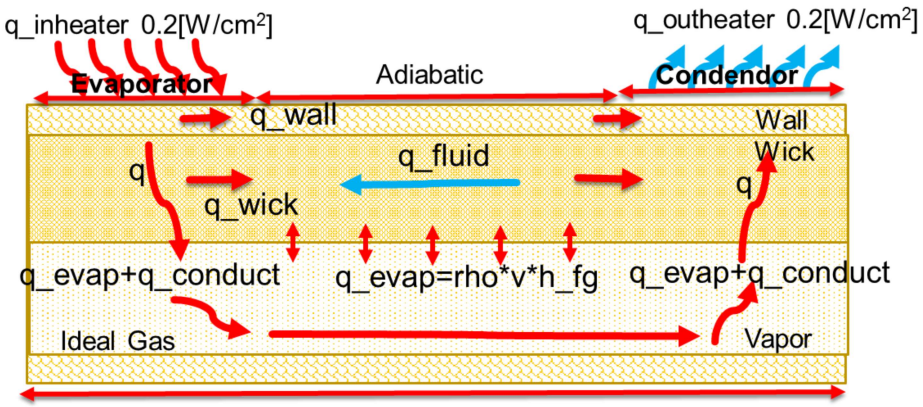


Figure 102 Heat transfer setting of the whole model

And the initial conditions are imposed:

$$T(x,y,0) = T_i; P_{op}(t=0) = P_{sat}(T_i) \tag{4-46}$$

At the lateral face of the vapor core, a symmetry is set

$$\mathrm{u} = \mathrm{v} = 0; \vec{\mathrm{K}} - \left(\vec{\mathrm{K}} \cdot \vec{\mathrm{n}}\right) \cdot \vec{\mathrm{n}} = 0, \vec{\mathrm{K}} = [\mu(\nabla\vec{\mathrm{u}} + (\nabla\vec{\mathrm{u}})^T)]\vec{\mathrm{n}} \tag{4-47}$$

The phase change at the wick and vapor interface is connected at the boundary at x and y limits by adding the following boundary conditions.

$$at\ x = L_x - d\_wall;\ P_{wick} = P_v \tag{4-48}$$

And the vapor is always treated as an ideal gas, so we have the following relationship:

$$\rho_v = \frac{P_{op} \cdot M_n}{R\_const \cdot T} \tag{4-49}$$

To improve the stability of the model, and account for the coupling of interface mass flow with temperature, the mass flow rate is linearized with respect to temperature. To prevent round-off errors in the computation of pressure gradients from pressure differences that are small compared with the absolute pressure, the pressure is split into two components: 1) a system operating pressure and 2) a hydrodynamic component. These implementation details are discussed further in [222] and [227].

The governing equations are discretized using the finite-element method and solved with the commercial solver COMSOL [171]. The maximum element mesh size of the wick is set to d_wick/16, and the vapor core is set to d_vapor/16, and the maximum and minimum mesh size of the rest of the model is set to 1.48mm and 5um. In this case, steady state is considered to be achieved when the heat transfer rate in the condenser section reaches within 0.1% of the value at the evaporator section. The solution at each time step is considered converged when the residuals are less than 0.0001 times of the equation's normal value for the continuity, momentum equations and energy equation. And the maximum number of iterations is set to 150.

4.2.3)Results and discussion

The schematic diagram of the simulated geometries is shown in the Figure 100.

The properties of the working fluid, copper and porous wick materials used in the vapor core chamber simulations are shown in the following Table 14. Vapor properties are shown at temperature of 40degC.

Table 14 Properties of the working fluid, copper and porous wick materials used in the heat pipe simulations.

PROPERTY	*VALUE*
Copper density(ρ_{wall})	8978kg/m^3
Water liquid density(ρ_{water})	992.3kg/m^3
Water vapor density(ρ_v)	0.05122kg/m^3
Copper thermal conductivity(k_{wall})	400W/mK
Wick effective thermal conductivity(k_{wick})	1.3W/mK
Water vapor thermal conductivity(k_v)	0.05W/mK
Copper specific heat capacity(C_p)	381 J/kgK
Water liquid specific heat capacity(C_p)	4182 J/kgK
Water vapor specific heat capacity(C_p)	1889 J/kgK
Water liquid viscosity(μ_l)	0.00065 Pa*s
Water vapor viscosity(μ_v)	0.0000096 Pa*s
Enthalpy of vaporization(h_{fg})	2473 kJ/kg
Specific gas constant(R_const)	8.3145 J/molK
Water vapor mean molar mass(M_n)	0.018015 kg/mol
Wick porosity(φ)	0.5
Wick permeability(K)	1*10^{-11} m^2

The temperature fields predicted by the modeling approaches are shown in Figure 103. Figure 103(a) shows the temperature profile comparison along the x direction of 50W heat source between FEM model (COMSOL Multiphysics) and publication of Maziar Agnvami [215] and the error between them, while Figure 103 (b) shows the COMSOL simulated temperature profile with 30W, 40W and 50W heat source. The temperature profile has a maximum temperature at the evaporation side in the top surface and a minimum temperature at the condenser side. The plots reveal a high-accuracy match between COMSOL and theoretical solution. The maximum error is about 6% for configuration I and 0.075% for configuration II. From Figure 103 (b) & (d) we can see that by increasing 10W at the heat source, the temperature gains about 3K for configuration I, and 4K for configuration II.

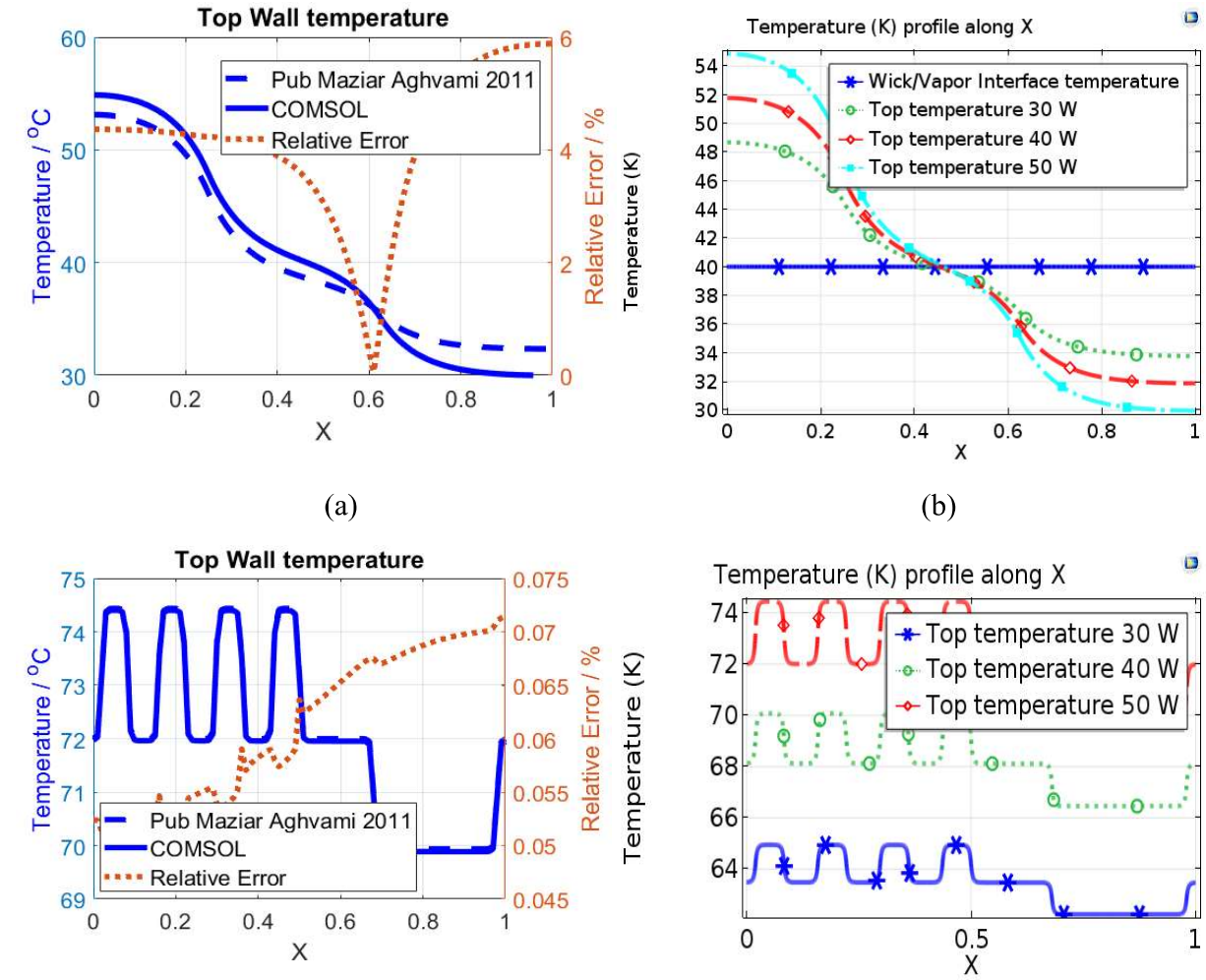


Figure 103 Temperature profile (a) comparison between COMSOL and pub with 50W heat source [215] in Matlab configuration I (b) parametrization of power in COMSOL configuration I (c) comparison between COMSOL and pub with 50W heat source [215] in Matlab configuration II (d) parametrization of power in COMSOL configuration II

The Figure 104 compares the velocities at the center of vapor chamber.

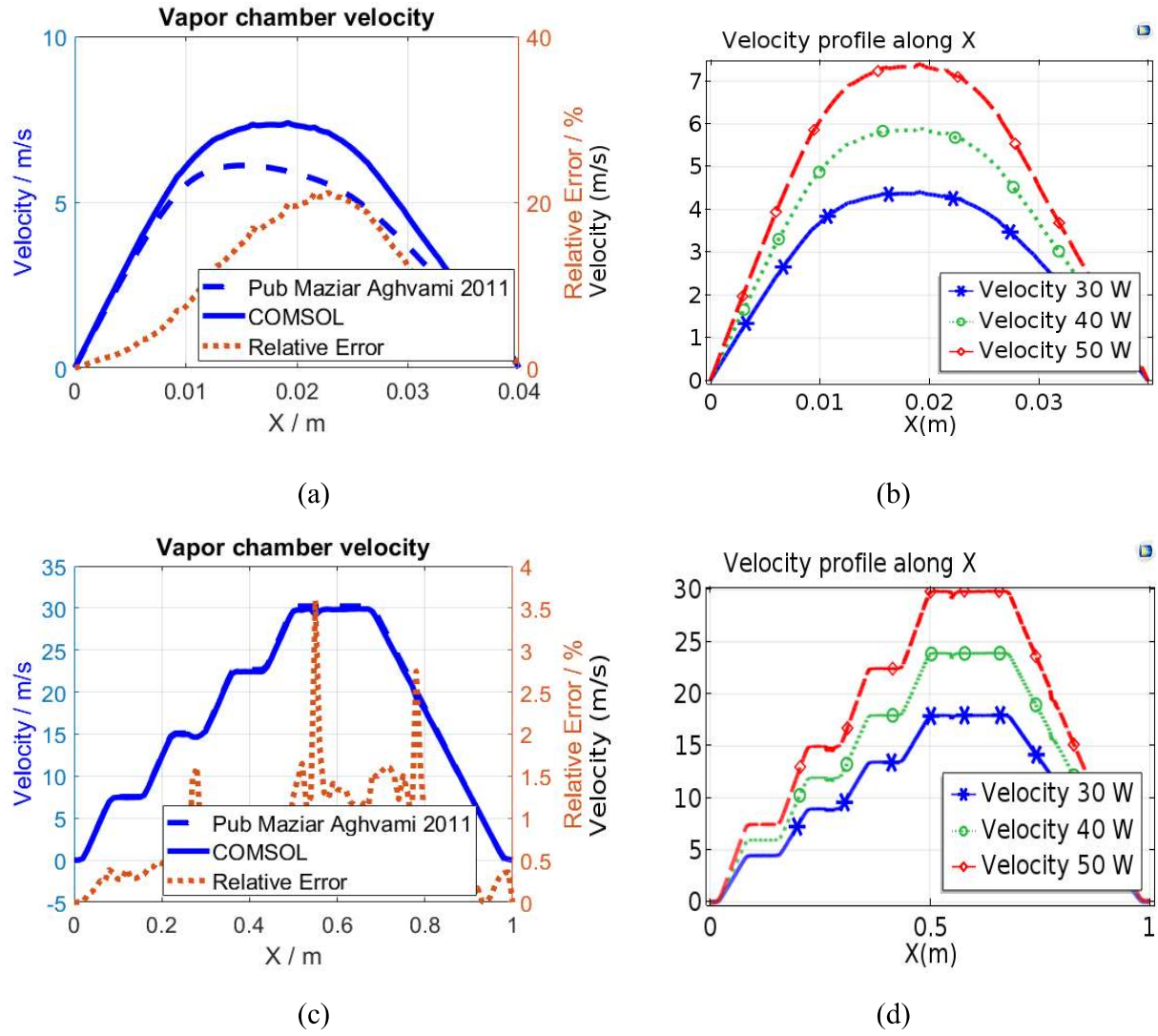


Figure 104 velocities at the center of vapor chamber (a) comparison between COMSOL and pub with 50W heat source [215] in Matlab configuration I (b) parametrization of power in COMSOL configuration I (c) comparison between COMSOL and pub with 50W heat source [215] in Matlab configuration II (d) parametrization of power in COMSOL configuration II

As we can see in the Figure 104, the vapor has a maximum velocity at the vapor core center and reduce to 0 when it attaches the wall. And for the COMSOL model, the maximum velocity is about 7 m/s, that's almost the same like the velocities of paper[215]. For configuration I, there is about 20% difference between analytical solution and COMSOL one, especially for the analytical solution, the velocity of configuration I has a non-symmetry form. But for configuration II, the difference in velocity is less than 4%. And by increasing 10W of the heat source, the velocity gains about 1.5 m/s for configuration I and 6 m/s for configuration II.

And finally, the most important part of the heat pipe is the capillary pressure in the vapor/wick interface. Figure 105 shows the capillary pressure at the wick/vapor interface. At the evaporation

side, the water is evaporated and the vapor has a maximum pressure gain at this side, but at the condenser side, the water is condensed and causes the water liquid's flow in the wick, so we can see a contrary process in the wick flow, the wick has a mass flow in at the condensation side, and has a mass flow out at the evaporation side, so the water flow from the condensation side to the evaporation side, but with a velocity much slower than the vapor core. And from Figure 105, we can see that the capillary pressures of configuration I of FEM simulation and publication [215] have at maximum 20% difference. But for configuration II, the capillary pressures are almost the same. And the error is less than 0.5%.

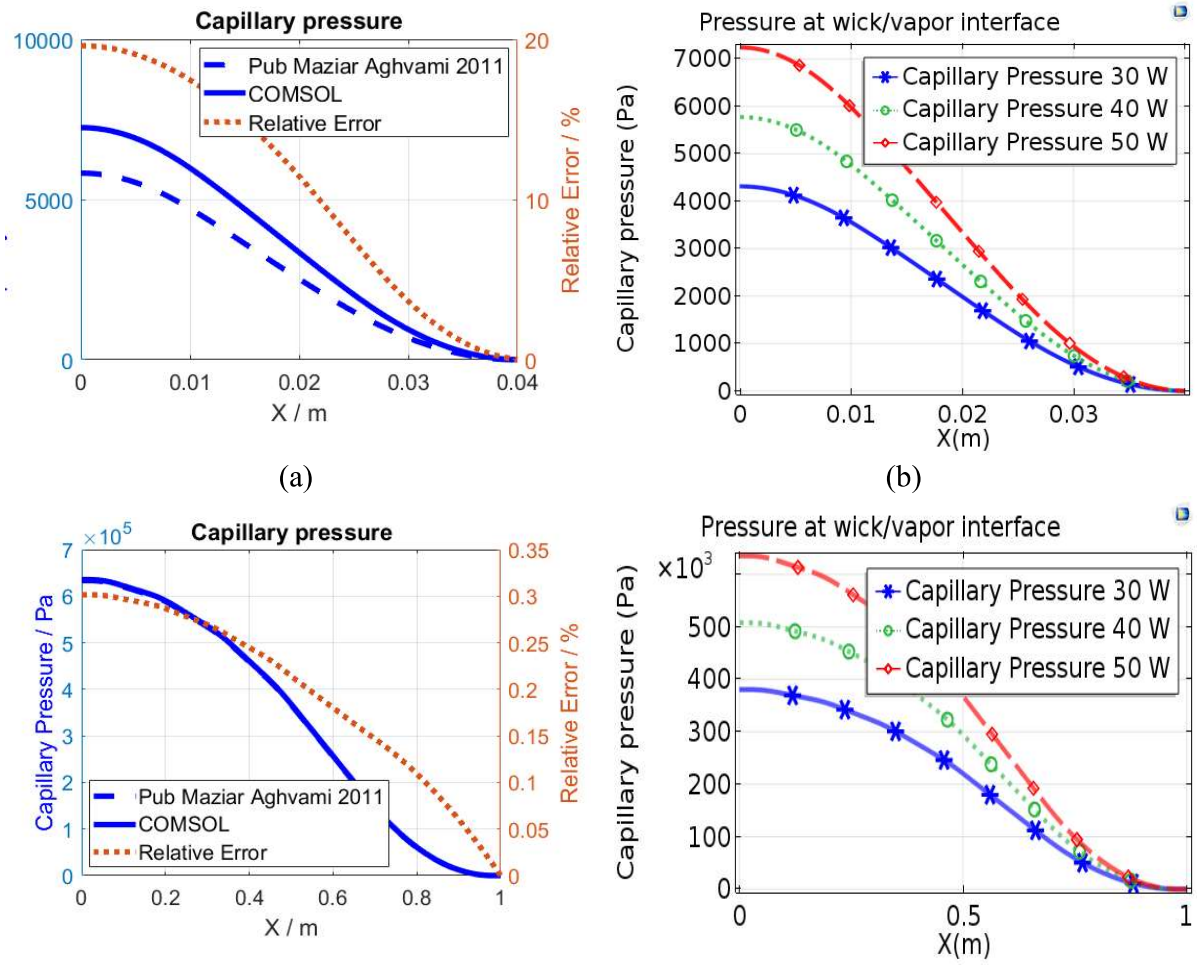


Figure 105 Capillary pressure at the wick/vapor interface (a) comparison between COMSOL and pub with 50W heat source [215] in Matlab configuration I (b) parametrization of power in COMSOL configuration I (c) comparison between COMSOL and pub with 50W heat source [215] configuration II (d) parametrization of power in COMSOL in Matlab configuration II

A stationary model for vapor chamber operation was developed that allows for multiple, arbitrarily shaped, heat inputs on the evaporator-side face; the model predicts 2D fields of temperature, pressure, and velocity in the vapor chamber, subject to assumptions regarding the

vapor chamber size, liquid and vapor flow, and the material properties. The governing mass, momentum, and energy equations in the wall, wick, and vapor core domains were established. The model is compared with a numerical model [215].

4.3) Configuration III 3D simulation

4.3.1)Effective thermal resistances for 3D flat heat pipes

The purpose of the simulation of heat pipe is to get the total effective thermal conductivity. Before study the configuration III, a first homogeneous 3D heat pipe should be studied. The studied flat heat pipe is heated on one side and cooled on the other side. The geometry of the model is shown as following.

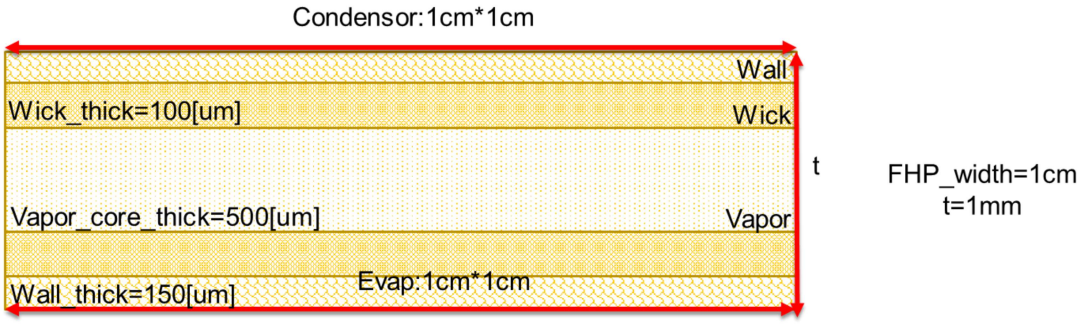


Figure 106 Geometry of heated on one side and cooled on the other side

Table 15 Physical properties of heat pipe

PROPERTY	*VALUE*
Copper density(ρ_{wall})	8960kg/m^3
Water liquid density(ρ_{water})	998.2kg/m^3
Water vapor density(ρ_v)	0.02kg/m^3
Copper thermal conductivity(k_{wall})	400W/mK
Wick effective thermal conductivity(k_{wick})	40W/mK
Water vapor thermal conductivity(k_v)	0.0189W/mK
Copper specific heat capacity(C_p)	381 J/kgK
Water liquid specific heat capacity(C_p)	4182 J/kgK
Water vapor specific heat capacity(C_p)	1889 J/kgK
Water liquid viscosity(μ_l)	1.79*10^{-5} Pa*s
Water vapor viscosity(μ_v)	1*10^{-3} Pa*s
Enthalpy of vaporization(h_{fg})	2473 kJ/kg
Specific gas constant(R_const)	8.3145 J/molK
Water vapor mean molar mass(M_n)	0.018015 kg/mol
Wick porosity(φ)	0.5
Wick permeability(K)	2.94*10^{-12} m^2

The properties of the working fluid, copper and porous wick materials used in the vapor core chamber simulations are shown in the upper table. Vapor properties are shown at temperature of 300K. The heat pipe is heated at the whole bottom face, and cooled at the whole top face. The heating power is set to 1W.

We simulate respectively the 1D, 2D and 3D heat transfer process in COMSOL, and compare the results with the first order heat thermal resistance method.

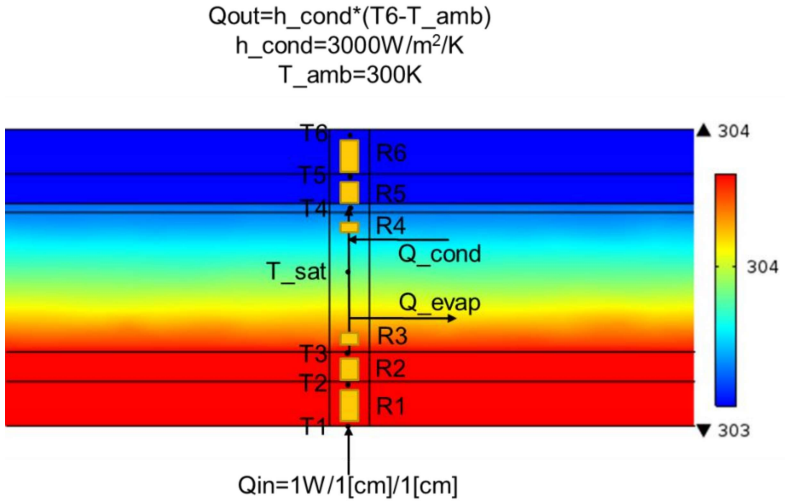


Figure 107 first order thermal resistance model

Due to the symmetry in the x and y directions of the flat heat pipe, the thermal path can be expressed along the Z direction. The heat flow from the wall to wick, and the heat is evaporated at the wick/vapor interface, the evaporated heat is equal to q_{evap}, and then at the other side of vapor chamber, the vapor is condensed and the heat is transferred from vapor to wick, and finally the heat flow to the wall and condensed by the air convection. As we can see from Figure 107, R1 to R6 are the relative thermal resistance during the heat flow process.

$$R_1 = R_6 = \frac{d_{wall}}{k_{copper}} \tag{4-50}$$

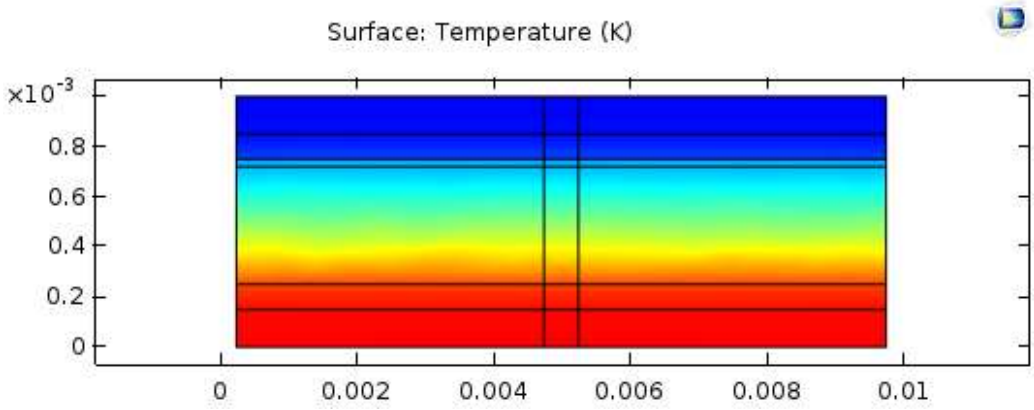
$$R_2 = R_5 = \frac{d_{wick}}{k_{wick}} \tag{4-51}$$

$$R_3 = R_4 = \frac{deltaT}{q_{evap}} = \frac{1}{h_{fg}{}^{*}\frac{2\sigma}{2-\sigma}\frac{h_{fg}\rho_v}{T_{sat}{}^{1.5}}\left(\frac{Mn}{2\pi R_{const}}\right)^{0.5}} \tag{4-52}$$

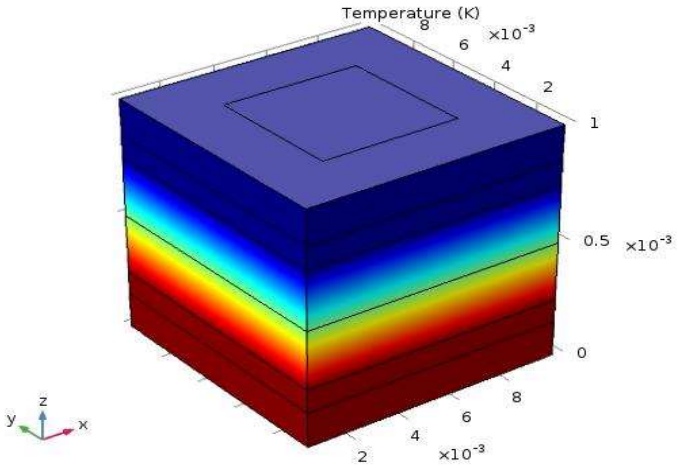
By using these thermal resistances, we can get the 1D analytical heat pipe model.

We also simulate a 1D, 2D and 3D model in FEM commercial software, the geometries are shown as following.

(a)1D model heat pipe



(b)2D model heat pipe



(c)3D model heat pipe

Figure 108 (a) 1D (b) 2D (c) 3D heat pipe model of FEM (COMSOL)

Figure 109 shows a comparison of the temperature variations of the 1D, 2D, 3D COMSOL model and the 1D analytical model. At the wall and wick, the thermal resistances are the same for the COMSOL and analytical one, but at the vapor chamber, they have a slightly difference. We can see from Table 16, the variation of the thermal resistances between COMSOL 1D model and Matlab analytical one is about 3.7%. So we can say that COMSOL matches better with the 1D thermal resistance method. And Figure 109 shows also that the 3D model is more close to the

analytical one, and the 3D model has less perturbations at the vapor chamber region, maybe 3D model's mesh is too large. And the 1D COMSOL model's maximum temperature is less than the others.

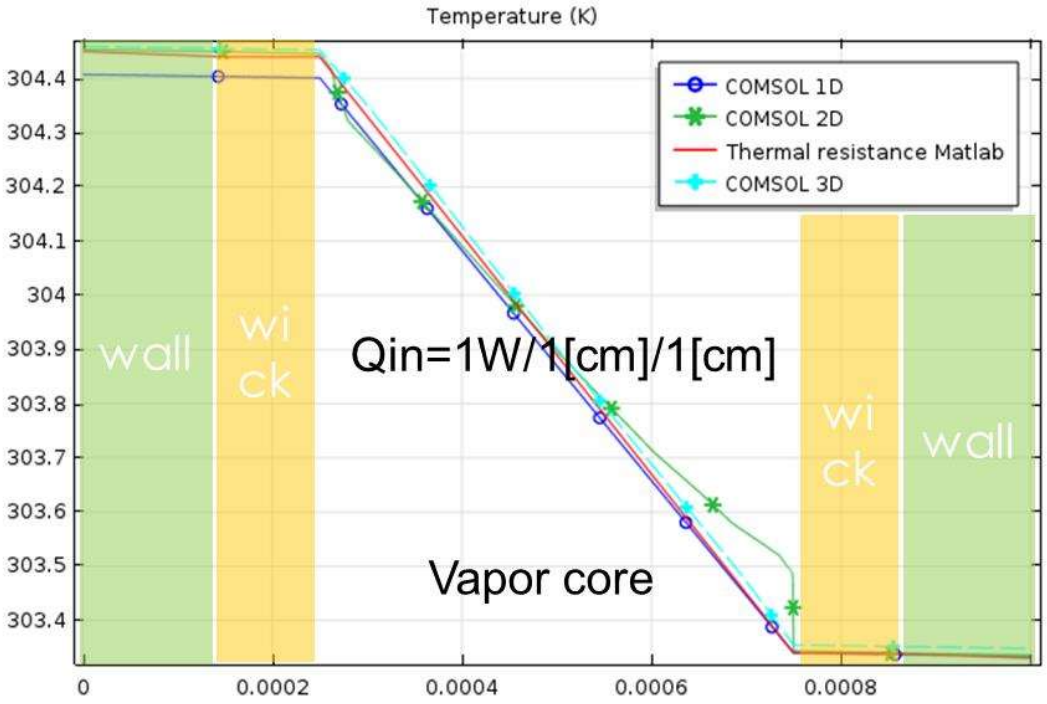


Figure 109 Temperature along the different layers of heat pipe with 1W heat source

Table 16 1D heat pipe thermal results of COMSOL and analytical one

K*m^2/W	R1	R2	R3	R4	R5	R6	R7
COMSOL	3.75e-7	2.5e-7	5.3079e-5	5.3079e-6	2.5e-7	3.75e-7	
MATLAB	3.75e-7	2.5e-7	5.5066e-5	5.5066e-5	2.5e-7	3.75e-7	3.3333E-4
W/m/K	K1	K2	K3	K4	K5	K6	K7
COMSOL	400	400	4.7099	4.7099	400	400	
MATLAB	400	400	4.54	4.54	400	400	
K	T1	T2	T3	T4	T5	T6	T7
COMSOL	304.4074	304.4037	304.4012	303.8704	303.3396	303.3371	303.3333
MATLAB	304.4472	304.4434	304.4409	303.8902	303.3396	303.3371	303.3333
W/m^2	1	2	3	4	5	6	7
Comsol	10000	10000	10000	0	10000	10000	10000
Q_evap			9629.7		9629.7		
Matlab	10000	10000	10000	0	10000	10000	10000

A little problem is that, when we add a heat flow Q_{evap} at wick/vapor interface (heater side) and Q_{cond} at wick/vapor interface (cooler side), they should create a short circuit of the vapor chamber, but in COMSOL simulation, we can see that the heat flow $Q_{evap} = Q_{cond} = 9629.7 W/m^2$, that's less

than the initial heat flow 10000 W/m^2. That is probably due to the heat conduction in the vapor chamber.

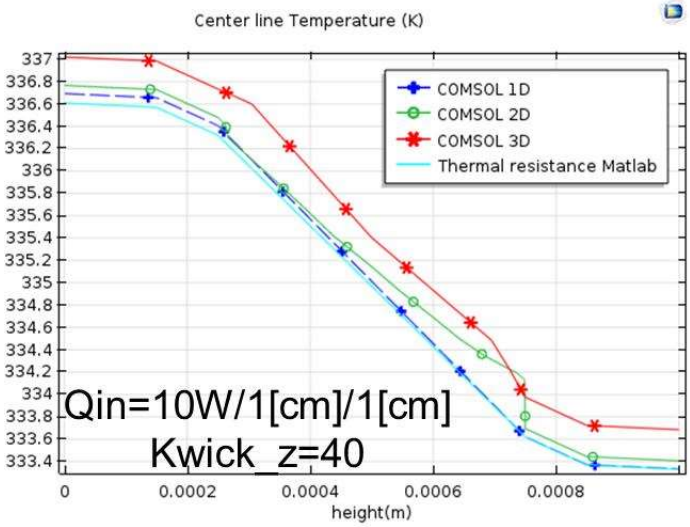


Figure 110 Temperature along the different layers of heat pipe with 10W heat source

When we increase the Qin to 10W, the difference between COMSOL 3D and thermal resistance model turns more obvious. Even if we have already set the thermal conductivity to zero in the X and Y direction, guess: the convective term in the energy equation no zero and have a very high influence to the result. By using the 3D COMSOL model, we can also find the 3D temperature map, 3D pressure map of the heat pipe model.

4.3.2)Analytical solution for 3D heat pipe (configuration III)

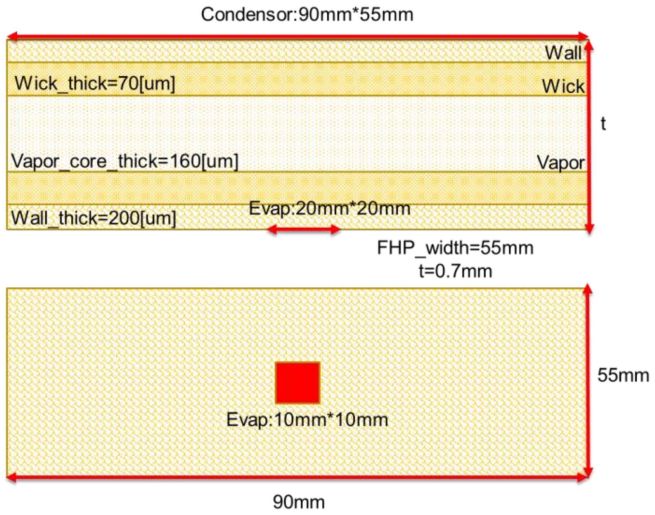


Figure 111 Double sides heat pipe model

The vapor chamber has a three-dimensional rectangular geometry; Figure 113 illustrates the wall, wick, and vapor core domains and their sizes in the x, y, and z coordinate directions. The

wall, wick and the vapor-core have dimensions of Lx and Ly, respectively, in the x and y directions. The vapor chamber is subjected to multiple arbitrarily shaped and time-varying heat inputs on one of its faces (z = 0), while the other face (z =hwall,1 + hwick,1 + hvap + hwick,2 + hwall,2) is subjected to a uniform convective boundary condition. The lateral walls are insulated. The thickness of the walls and wick along the sides at x = 0, x = Lx, y = 0 and y = Ly is assumed to be negligible.[229]

The governing equations solved for the vapor chamber are described below. The wick is assumed to be a homogeneous porous medium with saturated liquid. Flow in the wick and vapor core is assumed to be laminar and incompressible. The governing equations for mass, momentum and energy transport are

Mass conservation equation:

$$\frac{\partial \mathrm{u}}{\partial x}+\frac{\partial \mathrm{v}}{\partial x}+\frac{\partial \mathrm{w}}{\partial x}=0 \tag{4-53}$$

Momentum equation:

$$\rho\frac{\partial \vec{V}}{\partial t}+\frac{1}{\varepsilon_p}\rho\left(u\cdot\frac{\partial \vec{V}}{\partial x}+v\cdot\frac{\partial \vec{V}}{\partial y}+w\cdot\frac{\partial \vec{V}}{\partial z}\right)=-\nabla(\varepsilon_p P)+\mu(\frac{\partial^2 \vec{V}}{\partial x^2}+\frac{\partial^2 \vec{V}}{\partial y^2}+\frac{\partial^2 \vec{V}}{\partial z^2})-\mu K^{-1}\vec{V} \tag{4-54}$$

Energy equation:

$$\frac{(\rho C_p)_{eff}\partial T}{\partial t}+\left(\rho C_p\right)_l(u\cdot\frac{\partial T}{\partial x}+v\cdot\frac{\partial T}{\partial y}+w\cdot\frac{\partial T}{\partial z})=k_{eff}(\frac{\partial^2 \mathrm{T}}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}) \tag{4-55}$$

For wick,

$$(\rho C_p)_{eff}=\varepsilon_p(\rho C_p)_l+(1-\varepsilon_p)\,(\rho C_p)_s \tag{4-56}$$

For the wall,

$$(\rho C_p)_{eff}=(\rho C_p)_{wall} \tag{4-57}$$

For the vapor core,

$$(\rho C_p)_{eff}=(\rho C_p)_{vap} \tag{4-58}$$

Mass flux rate [239],

$$\dot{m}''=\frac{2\sigma}{2-\sigma}\frac{h_{fg}\rho_{vap}}{{T_{vap}}^{1.5}}\left(\frac{Mn}{2\pi R_{const}}\right)^{0.5}(T_{int}-T_{sat}) \tag{4-59}$$

The saturation temperature in the vapor core is computed using the Clausius-Clapeyron equation:

$$\frac{dP_{sat}}{dT_{sat}}=\frac{h_{fg}P_{sat}}{RT_{sat}^2} \tag{4-60}$$

Boundary conditions

At z = 0

$$(-k\frac{\partial T}{\partial z})_{wall} = q''_{in}(x,y) \tag{4-61}$$

At z = $h_{wall,1}$

$$u = v = w = 0 \tag{4-62}$$
$$(-k_{eff}\frac{\partial T}{\partial z})_{wall} = (-k_{eff}\frac{\partial T}{\partial z})_{wick} \tag{4-63}$$

At z = $h_{wall,1} + h_{wick,1}$

$$(\rho w)_{wick} = (\rho w)_{vap}; u = v = 0 \tag{4-64}$$
$$(-k_{eff}\frac{\partial T}{\partial z})_{wick} - \dot{m}''_1 h_{fg} = (-k\frac{\partial T}{\partial z})_{vap} \tag{4-65}$$

At z = $h_{wall,1} + h_{wick,1} + h_{vap}$

$$(\rho w)_{wick} = (\rho w)_{vap}; u = v = 0 \tag{4-66}$$
$$(-k_{eff}\frac{\partial T}{\partial z})_{wick} - \dot{m}''_2 h_{fg} = (-k\frac{\partial T}{\partial z})_{vap} \tag{4-67}$$

At z = $h_{wall,1} + h_{wick,1} + h_{vap} + h_{wick,2}$

$$u = v = w = 0 \tag{4-68}$$
$$(-k_{eff}\frac{\partial T}{\partial z})_{wall} = (-k_{eff}\frac{\partial T}{\partial z})_{wick} \tag{4-69}$$

At z = $h_{wall,1} + h_{wick,1} + h_{vap} + h_{wick,2} + h_{wall,2}$

$$u = v = w = 0 \tag{4-70}$$
$$(-k\frac{\partial T}{\partial z})_{wall} = h(T - T_\infty) \tag{4-71}$$

Energy and momentum equation:

At vapor core

$$h_{vap}, h_{wick,1}, h_{wick,2} \ll L_x, L_y \tag{4-72}$$

So

$$\frac{\partial^2}{\partial x^2}, \frac{\partial^2}{\partial y^2} \ll \frac{\partial^2}{\partial z^2} \tag{4-73}$$

And laminar incompressible flow,

$$\rho u\frac{\partial}{\partial x}, \rho v\frac{\partial}{\partial y}, \rho w\frac{\partial}{\partial z} \ll \mu\frac{\partial^2}{\partial z^2} \tag{4-74}$$
$$\rho C_{p,l} u\frac{\partial}{\partial x}, \rho C_{p,l} v\frac{\partial}{\partial y}, \rho C_{p,l} w\frac{\partial}{\partial z} \ll k\frac{\partial^2}{\partial z^2} \tag{4-75}$$

Based on these assumption, the energy and momentum equation can be reduced to:

$$\rho\frac{\partial\vec{V}}{\partial t} = -\nabla P + \mu\frac{\partial^2\vec{V}}{\partial z^2} \tag{4-76}$$

$$(\rho C_p)_{eff}\frac{\partial T}{\partial t} = k_{eff}\frac{\partial^2 T}{\partial z^2} \tag{4-77}$$

Assumption:

$$\bar{T}_{wall,1} = \bar{T}_{wick,1} = \bar{T}_1 \tag{4-78}$$

$$\bar{T}_{wall,2} = \bar{T}_{wick,2} = \bar{T}_2 \tag{4-79}$$

$$T = a\left(z - h_{wall,1} - h_{wick,1}\right)^2 + b\left(z - h_{wall,1} - h_{wick,1}\right) + c \tag{4-80}$$

$$a = \frac{3(\bar{T}_1+\bar{T}_2-2\bar{T}_{vap})}{h_{vap}^2}, a = \frac{6\bar{T}_{vap}-4\bar{T}_1-2\bar{T}_2}{h_{vap}}, \mathrm{c} = \bar{T}_1 \tag{4-81}$$

At wick, we have

$$\mu\frac{\partial^2}{\partial z^2}, \rho\frac{\partial}{\partial t} \ll \frac{\mu\varepsilon_p}{K} \tag{4-82}$$

So

$$\nabla(\varepsilon_p P) = -\mu K^{-1}\vec{V} \tag{4-83}$$

$$(\rho C_p)_{eff}\frac{\partial T}{\partial t} = k_{eff}\frac{\partial^2 T}{\partial z^2} \tag{4-84}$$

By combining all the above equations, and replace T by θ,

$$\theta = \begin{bmatrix} \bar{T}_1 \\ \bar{T}_{vap} \\ \bar{T}_2 \end{bmatrix} \tag{4-85}$$

$$\frac{\partial\theta}{\partial t} = A\left(\frac{\partial^2\theta}{\partial x^2} + \frac{\partial^2\theta}{\partial y^2}\right) + B\theta + C \tag{4-86}$$

$$C = \begin{bmatrix} \frac{q_{in}'' - \dot{m}_1'' h_{fg}}{\beta_1} \\ 0 \\ \frac{hT_\infty - \dot{m}_2'' h_{fg}}{\beta_2} \end{bmatrix} \tag{4-87}$$

$$\beta_1 = \left(\rho C_p\right)_{wall,1} h_{wall,1} + \left(\rho C_p\right)_{eff,wick,1} h_{wick,1} \tag{4-88}$$

$$\beta_2 = \left(\rho C_p\right)_{wall,2} h_{wall,2} + \left(\rho C_p\right)_{eff,wick,2} h_{wick,2} \tag{4-89}$$

$$A = \begin{bmatrix} \frac{k_{wall,1}h_{wall,1}}{\beta_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{k_{wall,2}h_{wall,2}}{\beta_2} \end{bmatrix} \tag{4-90}$$

$$B = \begin{bmatrix} \frac{-k_{vap}}{\beta_1 h_{vap}} & 0 & 0 \\ 0 & \frac{6k_{vap}}{h_{vap}^2(\rho C_p)_{vap}} & 0 \\ 0 & 0 & \frac{-k_{vap}}{\beta_2 h_{vap}} \end{bmatrix} \times \begin{bmatrix} 4 & -6 & 2 \\ 1 & -2 & 1 \\ 2 & -6 & 4 + \frac{h*h_{vap}}{k_{vap}} \end{bmatrix} \tag{4-91}$$

For the vapor core, another assumption

$$\rho\frac{\partial\vec{V}}{\partial t}=0 \tag{4-92}$$

$$\nabla P=\mu\frac{\partial^2\vec{V}}{\partial z^2} \tag{4-93}$$

So along with the boundary conditions, we have

$$\mathrm{u}=\frac{1}{2\mu}\frac{\partial P}{\partial x}(z^2-\left(2h_{wall,1}+2h_{wick,1}+h_{vap}\right)z+(h_{wall,1}+h_{wick,1})(h_{wall,1}+h_{wick,1}+h_{vap})) \tag{4-94}$$

$$\mathrm{v}=\frac{1}{2\mu}\frac{\partial P}{\partial y}(z^2-\left(2h_{wall,1}+2h_{wick,1}+h_{vap}\right)z+(h_{wall,1}+h_{wick,1})(h_{wall,1}+h_{wick,1}+h_{vap})) \tag{4-95}$$

So the mass conservation equation of the vapor core change to:

$$\frac{\partial^2P}{\partial x^2}+\frac{\partial^2P}{\partial y^2}=-\frac{12\mu}{\rho h_{vap}^3}(\dot{m}_1''+\dot{m}_2'') \tag{4-96}$$

With clausius-clapeyron equation

$$\frac{\partial P}{\partial T_{sat}}=\lambda=\frac{h_{fg}P_{ref}}{R(T_{sat}^2)_{mean}} \tag{4-97}$$

$$\lambda\left(\frac{\partial^2T_{sat}}{\partial x^2}+\frac{\partial^2T_{sat}}{\partial y^2}\right)=-\frac{12\mu_{vap}}{\rho_{vap}h_{vap}^3}\varepsilon_p(\bar{T}_1+\bar{T}_2-2T_{sat}) \tag{4-98}$$

Solution to the combined energy equation

$$\theta=\begin{bmatrix}\bar{T}_1\\ \bar{T}_{vap}\\ \bar{T}_2\end{bmatrix}=\sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(a_{lk}\cos\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)\right),where\ a_{lk}=\begin{bmatrix}a_1\\ a_{vap}\\ a_2\end{bmatrix}_{lk} \tag{4-99}$$

$$T_{sat}=\sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(c_{lk}\cos\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)\right) \tag{4-100}$$

$$c_{lk}=\frac{[1\quad 0\quad 1]a_{lk}}{(\frac{\lambda\rho_{vap}h_{vap}^3}{12\mu_{vap}\varepsilon_p}\pi^2(\frac{l^2}{L_x^2}+\frac{k^2}{L_y^2})+2)} \tag{4-101}$$

$$\sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(b_{lk}\cos\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)\right)=\begin{bmatrix}\frac{q_{in}''}{\beta_1}\\ 0\\ \frac{hT_\infty}{\beta_2}\end{bmatrix} \tag{4-102}$$

So the energy equation can change to

$$b_{lk}=\frac{\partial a_{lk}}{\partial t}+\mathrm{G}a_{lk} \tag{4-103}$$

with

$$G = A\pi^2\left(\frac{l^2}{L_x^2}+\frac{k^2}{L_y^2}\right) - B - \begin{bmatrix} \frac{-\varepsilon_P h_{fg}}{\beta_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{-\varepsilon_P h_{fg}}{\beta_2} \end{bmatrix} - \begin{bmatrix} \frac{\varepsilon_P h_{fg}}{\beta_1} \\ 0 \\ \frac{\varepsilon_P h_{fg}}{\beta_2} \end{bmatrix} \frac{[1 \quad 0 \quad 1]a_{lk}}{\left(\frac{\lambda\rho_{vap}h_{vap}^3}{12\mu_{vap}\varepsilon_p}\pi^2\left(\frac{l^2}{L_x^2}+\frac{k^2}{L_y^2}\right)+2\right)} \quad (4\text{-}104)$$

$$b_{lk} = \frac{\delta_{lk}}{L_x L_y}\int_0^{L_x}\int_0^{L_y}\begin{bmatrix} \frac{q_{in}''}{\beta_1} \\ 0 \\ \frac{hT_\infty}{\beta_2} \end{bmatrix}\cos\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)dxdy \quad (4\text{-}105)$$

$$\delta_{lk} = 4\ for\ l>0\ and\ k>0$$
$$\delta_{lk} = 2\ for\ l=0\ and\ k>0\ or\ l>0\ and\ k=0$$
$$\delta_{lk} = 1\ for\ l=0\ and\ k=0$$

$$a_{lk}^0 = \frac{\delta_{lk}}{L_x L_y}\int_0^{L_x}\int_0^{L_y}\begin{bmatrix} \overline{T}_1^0 \\ \overline{T}_{vap}^0 \\ \overline{T}_2^0 \end{bmatrix}\cos\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)dxdy \quad (4\text{-}106)$$

$$a_{lk}^{n+1} = (I_3 + \Delta t G)^{-1}(\Delta t b_{lk}^{n+1} + a_{lk}^n) \quad (4\text{-}107)$$

For the wick

$$\frac{\partial^2 P_{sum}}{\partial x^2}+\frac{\partial^2 P_{sum}}{\partial y^2} = \frac{\dot{m}_1''\mu}{\rho K_{wick,1}h_{wick,1}}+\frac{\dot{m}_2''\mu}{\rho K_{wick,2}h_{wick,2}} \quad (4\text{-}108)$$

$$\frac{\partial^2 P_{diff}}{\partial x^2}+\frac{\partial^2 P_{diff}}{\partial y^2} = \frac{\dot{m}_1''\mu}{\rho K_{wick,1}h_{wick,1}}-\frac{\dot{m}_2''\mu}{\rho K_{wick,2}h_{wick,2}} \quad (4\text{-}109)$$

$$P_{sum} = \sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(d_{sum,lk}\cos\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)\right) \quad (4\text{-}110)$$

$$P_{diff} = \sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(d_{diff,lk}\sin\left(\frac{l\pi x}{L_x}\right)\sin\left(\frac{k\pi y}{L_y}\right)\right) \quad (4\text{-}111)$$

With

$$d_{sum,lk} = \frac{\delta_{lk}\int_0^{L_x}\int_0^{L_y}\left(\frac{\dot{m}_1''\mu}{\rho K_{wick,1}h_{wick,1}}+\frac{\dot{m}_2''\mu}{\rho K_{wick,2}h_{wick,2}}\right)\cos\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)dxdy}{-\pi^2\left(\frac{l^2}{L_x^2}+\frac{k^2}{L_y^2}\right)L_x L_y} \quad (4\text{-}112)$$

$$d_{sum,lk} = \frac{4\int_0^{L_x}\int_0^{L_y}\left(\frac{\dot{m}_1''\mu}{\rho K_{wick,1}h_{wick,1}}+\frac{\dot{m}_2''\mu}{\rho K_{wick,2}h_{wick,2}}\right)\cos\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)dxdy}{-\pi^2\left(\frac{l^2}{L_x^2}+\frac{k^2}{L_y^2}\right)L_x L_y} \quad (4\text{-}113)$$

$$\nabla(\varepsilon_p P) = -\mu K^{-1}\vec{V} \quad (4\text{-}114)$$

$$u_{sum} = \frac{-K\varepsilon_p\partial P_{sum}}{\mu\partial x} = \frac{K\varepsilon_p l\pi}{\mu L_x}\sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(d_{sum,lk}\sin\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)\right) \quad (4\text{-}115)$$

$$v_{sum} = \frac{-K\varepsilon_p\partial P_{sum}}{\mu\partial y} = \frac{K\varepsilon_p k\pi}{\mu L_y}\sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(d_{sum,lk}\cos\left(\frac{l\pi x}{L_x}\right)\sin\left(\frac{k\pi y}{L_y}\right)\right) \quad (4\text{-}116)$$

$$u_{diff} = \frac{-K\varepsilon_p\partial P_{diff}}{\mu\partial x} = \frac{-K\varepsilon_p l\pi}{\mu L_x}\sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(d_{diff,lk}\cos\left(\frac{l\pi x}{L_x}\right)\sin\left(\frac{k\pi y}{L_y}\right)\right) \quad (4\text{-}117)$$

$$v_{diff} = \frac{-K\varepsilon_p\partial P_{diff}}{\mu\partial y} = \frac{-K\varepsilon_p k\pi}{\mu L_y}\sum_{l-0}^{\infty}\sum_{k=0}^{\infty}\left(d_{diff,lk}\sin\left(\frac{l\pi x}{L_x}\right)\cos\left(\frac{k\pi y}{L_y}\right)\right) \quad (4\text{-}118)$$

4.3.3)Comparison results with FEM simulation

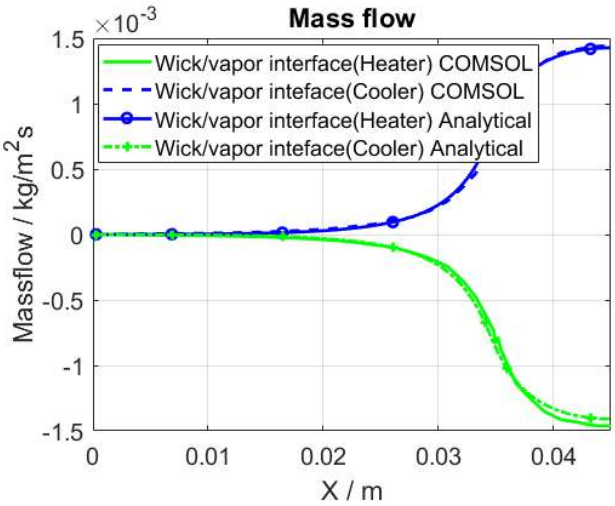


Figure 112 mass flow comparison between COMSOL and analytical method

The evaporated and condensed mass are shown in the above Figure 112. As we can see, at the center or the heater place, the evaporated mass has the maximum value, and it reduces along X direction. And we can see that, the simulation in COMSOL and analytical model have very good fit. (Error <1%)

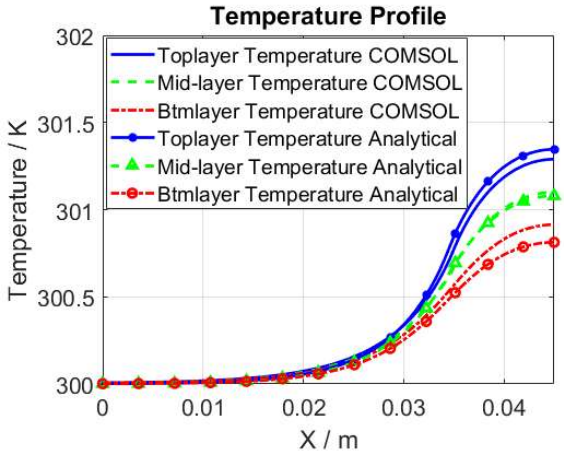


Figure 113 Temperature of the vapor chamber in the XZ surface

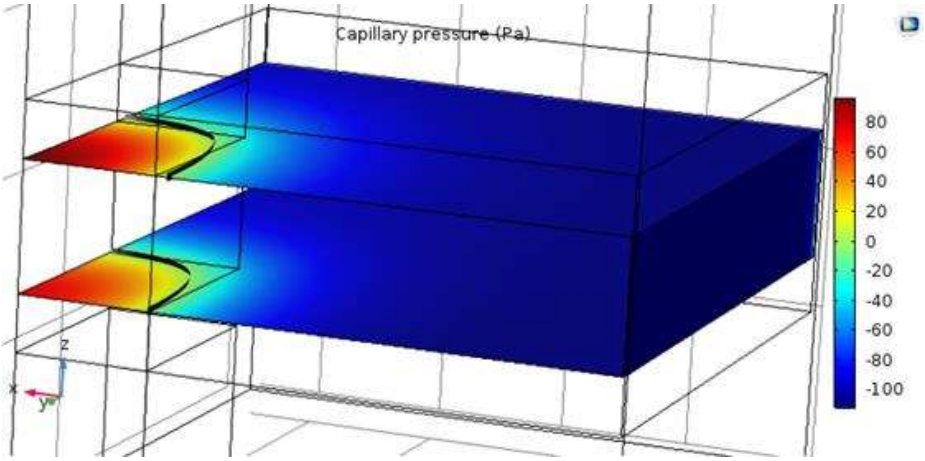
Figure 113 shows the temperature of heat-pipe along X. It shows the comparison between COMSOL and analytical model.

Table 17 Differences between COMSOL and analytical solution

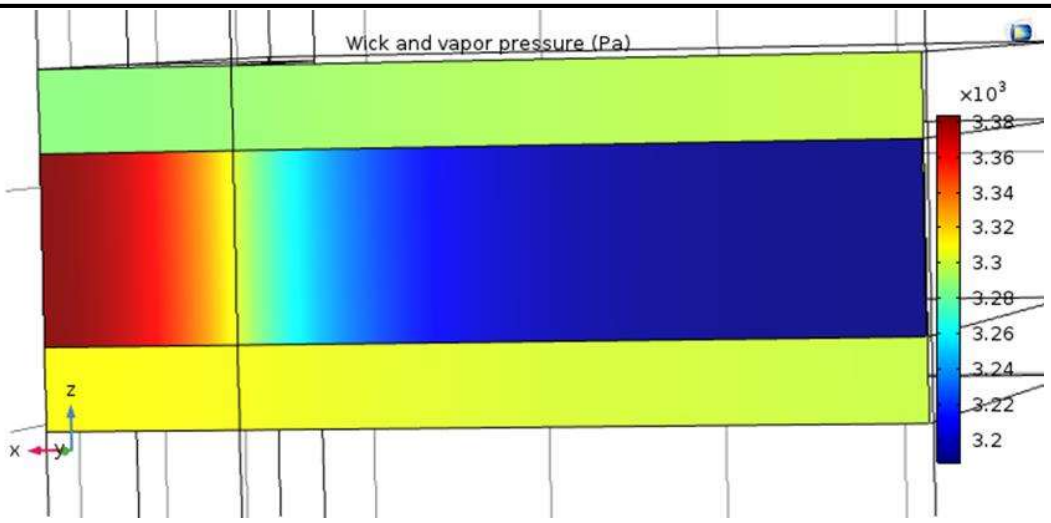
Top temperature	*Mid Temperature*	*Bottom Temperature*	*Heater side Mass flow*	*Cooler side Mass flow*

Difference	4.5e-2%	1.6e-2%	1.45e-2%	2.5%	2.17%

As we can see, here, we have a good fit in the mass flow between COMSOL and analytical model, the difference between FEM and the analytical model comes very probably from that the COMSOL calculates temperature map and pressure field iteratively, but the analytical model replace the mass flow by a temperature dependent formula, and the temperature is calculated only by temperature field. And the pressure field in the analytical model is dominated by temperature. So that's to say, by using FEM model, we can more accurately restore the temperature value, because the analytical model make an assumption that the evaporated mass depends only on the temperature. This will decrease the calculation accuracy. But, in all, the analytical model has also a good fit with FEM model which has a difference of about 2.5%. If the temperature gets higher, the difference will be more negligible.

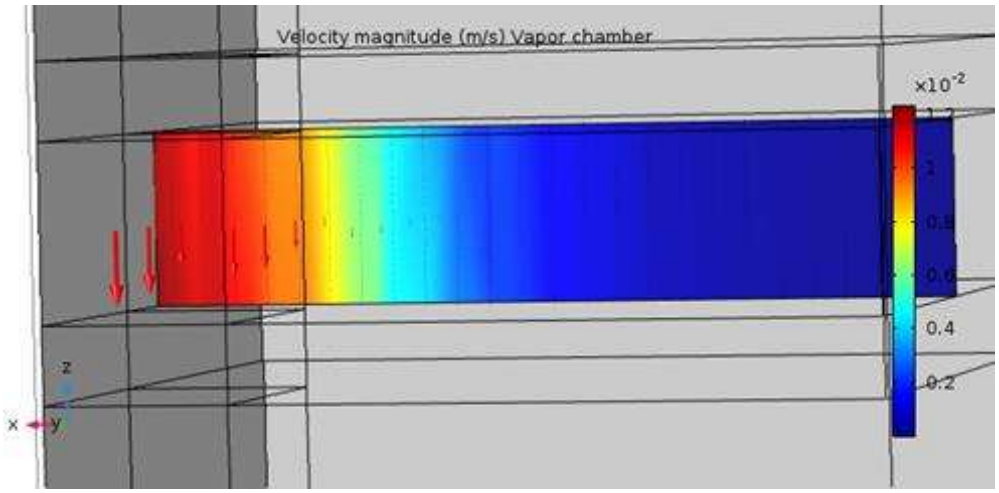


(a)

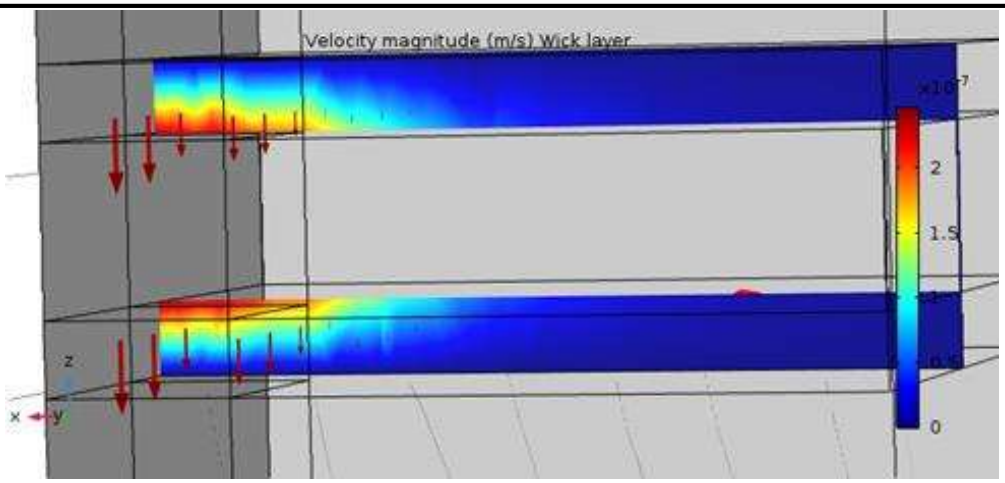


(b)

Figure 114 (a) Capillary pressure and (b) wick/vapor pressure



(a)



(b)

Figure 115 Velocity of vapor in the (a) vapor chamber and of water in (b) the wick

Besides, with FEM model, the velocity field and pressure field of wick and vapor chamber can be extracted, shown in the Figure 114 and Figure 115. From Figure 115, we can see the exact velocity of water and vapor, the water is evaporated at the heater part and turns to vapor, and then the vapor flows to the other side of the heat-pipe and then condensed, turns back to water. From Figure 114, we can extract also the capillary pressure at the wick/vapor interface. Here, in this case, the marge of capillary pressure is about 200 Pa.

As a conclusion, the analytical model is accurate in the estimation of the mass flow, but for the calculation of temperature, it needs some little improvement. And the FEM model is very accurate; it considers the pressure field in the calculation, and especially it can extract the capillary pressure from the model, which will be very useful in the future study of wick layer's capillary effects.

4.4) Performance-limiting Conditions

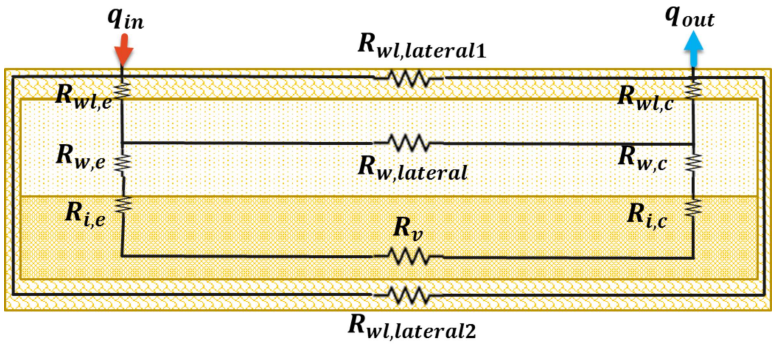


Figure 116 Schematic of approximate network of thermal resistance of configuration I

The temperature drop due to the thermal transfer mechanisms the flat heat pipe can be calculated using the above simplified effective thermal resistance network, as shown in Figure 116. The thermal resistances due to the vertical conduction along the thickness of the wall in the evaporation ($R_{wl,e}$) and condensation sides ($R_{wl,c}$) are negligible (because of the thin thickness of wall), which is viable only for ultrathin heat pipes with high conductive materials. Lateral conduction along the wall is represented as $R_{wl,lateral1}$ and $R_{wl,lateral2}$; the effective thermal resistances can be obtained using an effective length L_{eff} that considers the different heat load along the length of the evaporator and condenser, and is written as [219]

$$L_{eff} = L_a + \frac{L_e + L_c}{2} \tag{4-119}$$

Resistances vertically across the wick in the evaporation side ($R_{w,e}$), condensation side ($R_{w,c}$), and along the wick ($R_{w,lateral}$) are supposed to be conductive. The solid and fluid thermal convection in the wick is neglected, due to the low liquid flow velocities. Here, we use an effective saturated wick thermal conductivity to simplify the calculation of thermal conduction resistances. Lateral heat flow through the wick is neglected, because of the high thermal resistance that results from the low thermal conductivity and high aspect ratio of wick geometry. To simplify the simulation, heat loss due to surroundings' convection is neglected.

The wick/vapor phase-change thermal resistances are expressed by $R_{i,e}$ and $R_{i,c}$, respectively. They are normally small [217], so, neglected. The effective thermal resistance of the vapor core R_v, is calculated from an effective thermal conductivity of vapor [224], which is calculated by assuming that the vapor flow is laminar, incompressible, fully developed flow between parallel plates, and governed by continuum equation along the effective length of vapor core. The effective conductivity of vapor is shown as follow.

$$k_{eff,v} = \frac{h_{fg}^2 P_v \rho_v t_v^2}{12 R \mu_v T_v^2} \tag{4-120}$$

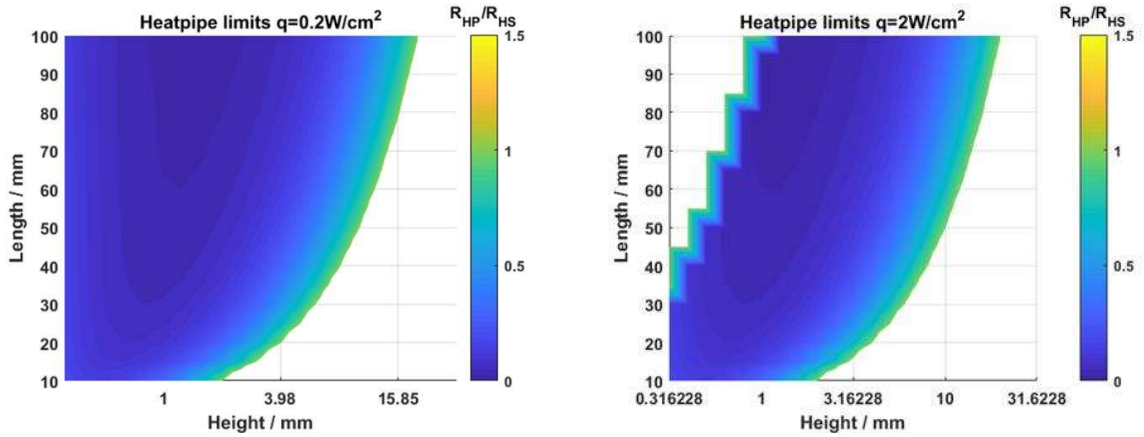
where the thermos-physical properties are those of ideal gas and the effective thermal conductivity depends on the local vapor temperature along the effective length of vapor core. To calculate temperature-dependent vapor thermal conductivity, the vapor effective thermal resistance is discretized along the flowing direction. This approach does not consider the vapor convection effects.

So the effective thermal resistance of the FHP configuration I can be expressed as

$$R_{HP} = \frac{1}{\frac{1}{R_{wl,lateral1}} + \frac{1}{R_{wl,lateral2}} + \frac{1}{(R_v + R_{w,e} + R_{w,c})}} \tag{4-121}$$

By generating the performance map through different input heat fluxes and for a range of geometries, it is possible to identify the advantageous region of small thickness and low input power FHP. Figure 117 shows a color map of the ratio between the heat pipe and copper heat spreader thermal resistances with the length and total thickness being varied. The colored region

represents the advantageous performance region of flat heat pipe, and white region indicates that the copper heat sink has a better thermal performance or the FHP reaches its limits. The performance threshold is set to 1, which means the FHP and heat sink have the same effective performance. A pressure of 2250 Pa is set as the maximum capillary pressure.



(a) (b)

Figure 117 Contour map of the resistance ratio R_{HP}/R_{HS} plotted as a function of length and thickness for an input heat flux of (a) 0.2 and (b) 2 W/cm^2 for length from 10mm to 100mm

Figure 117 (a) show the advantageous region for the FHP with a lower input heat flux of 0.2 W/cm^2. When the input heat fluxes stay low, the fluid velocities induced capillary pressure is sufficiently small, and the capillary limit moves to lower thicknesses and higher working lengths.

Figure 117(b) show the advantageous region for the FHP with a higher input heat flux of 2 W/cm^2. From the figure we can see, as the thickness is reduced to certain length, the minimum thickness for which R_{HP}/R_{HS} remains greater than 1 is governed by the capillary limit. That means that when the thicknesses reduce to a relatively small value and heat fluxes increase to a relatively high value, the pressure drop at the wick/vapor interface due to the higher mass flow gets higher than the maximum capillary pressure which is related to the liquid surface tension at the wick surface. The performance advantage of FHP comes from the small thermal resistances brought by liquid/vapor phase change between the evaporation and the condensation when heat is applied to the wick structure. However, this advantage will not exist while the FHP gets shorter and thicker, where the solid heat sinks with the same geometry can provide a more direct and higher conductivity than the FHP.

Except for the thickness-to-length ratio limit and the capillary limit, there is another limit, which is called vapor-resistance threshold. By calculating the equivalent thermal resistance of Figure 116, utilizing the assumption that R_{HP}/R_{HS} equals to 1, and representing the thicknesses of the vapor core, wick, and walls as fractions of the total thickness, i.e., $t_v = r_v t$, $t_w = r_w t$, and $t_{wl} = r_{wl} t$, the new limit can be denoted as [219]

$$\frac{r_w}{k_w}\left(\frac{1}{L_e}+\frac{1}{L_c}\right)t^4-\frac{L_{eff}}{k_s}\frac{1}{1-r_w}t^2+\frac{L_{eff}}{M_v r_v^3}=0 \qquad (4\text{-}122)$$

The equation have two positive roots representing the thickness limits where the R_{HP}/R_{HS} equals to 1. The minimum thickness limit governed by this equation is

$$t_{limit}=\left(\frac{\frac{L_{eff}}{k_s}a-\sqrt{\left(\frac{L_{eff}}{k_s}\right)^2-4\frac{r_w}{k_w}\left(\frac{1}{L_e}+\frac{1}{L_c}\right)\left(\frac{L_{eff}}{M_v r_v^3}\right)}}{2\frac{r_w}{k_w}\left(\frac{1}{L_e}+\frac{1}{L_c}\right)}\right)^{\frac{1}{2}} \qquad (4\text{-}123)$$

where $a = 1/(1-r_{wl})$ and M_v is the vapor properties related constant. The above limit depends only on the FHP geometry and material properties, it's independent of the heat input. Besides, this limit appears at the lower side of the thickness, so it should be considered in conjunction with the capillary limit, which depends on the heat inputs. For the FHP of low heat inputs, this limit depends on the single factor M_v, and it's also called vapor-resistance limit. The key factor M_v can be expressed by the following equation: [219]

$$M_v=\frac{h_{fg}^2\rho_v P_v}{R\mu_v T_v^2} \qquad (4\text{-}124)$$

which is independent of geometric parameters.

4.5) Conclusion

As a conclusion, the FEM based model (COMSOL Multiphysics) is very accurate in the 2D and 3D simulations of thin flat heat pipe. Precise boundary conditions can be found in the previous part; it considers the pressure field in the calculation, and especially it can extract the capillary pressure directly from the model, which will be very useful in the future study of wick layer's capillary effects.

As future work, the simplification for the evaporated mass should be changed to a temperature dependent parameters and a quantitative analysis of the model error, due to the employed simplifying assumptions, will be performed over a range of operating conditions. This model will be changed to a 3D model and then used to simulate the behavior of a vapor chamber subjected to multiple heat input boundary conditions to demonstrate the capability of the model in solving the 3D thermal real-applications. Before coming to the real-applications, some transfer mechanisms should be included in the model, for instance, the effects of external boundary conditions on the wick/vapor interfacial mass flux, the influence of inner vapor convections, and smearing effect of the interfacial mass flux into the heat insulation region by lateral thermal conduction. However, these effects should be considered only for detailed numerical models for the application-oriented design and optimization of ultrathin FHP.

Chapter 5: Noise in 3D circuits

The last chapter is interested in the noise in a much generalized way. Noise is a highly prominent and stochastic phenomenon, but from the other side of view, parasitic effects can be determinist effects in the 3D IC design. This chapter gives more possibilities on the domain of the noise, rather subtle which becomes prohibitive because of the miniaturization and the passage to the 2D through 3D, where reside strong conceptual problems. Noise is a universal phenomenon. Generally, micro-electronics and, of course, nano-electronics are domains where although autonomous noise sources can be dependent on each other due to their proximity, for example. Here, we will introduce concepts such as correlation of random variables, and noise spectral density. We will recall briefly the concept of transfer impedance; calculations at the unidimensional level have already been developed, but there are few in 2D and nothing considerable in 3D. Velocity fluctuations or generation-recombination, which can help quantifying certain noises by using master equations like the Boltzmann ones, can be taken into account in statistical methods like Monte Carlo ones.

5.1) Introduction

Laboratories work in the domain of background noise in semiconductors and devices, thus on fluctuation of physical or electrical quantities and *ad hoc* mathematical tools, thereby building a comprehensive and cooperative program via dialogue between researchers, students, post-graduates, devices and information. This covers fundamental studies as well as their application in modern submicronic devices (submicronic (SiGeC) silicon transistors, ultimate CMOS, high-speed III-V devices (HEMT: High Electron Mobility Transistor, Heterojunction Bipolar Transistor), and optoelectronic devices (lasers, photodiodes).[58], [173]

In electronic chips, semiconductor devices are immersed in a more or less noisy environment. From a microscopic point of view, fluctuations of physical and electronic quantities can be apprehended, for instance, using the Boltzmann equation, numerically or via Monte Carlo methods, and by calculating, for example, the speed fluctuation correlation function and its Fourier transform, which will give the noise spectral density. It was Shockley [240], inventor of the bipolar transistor (1948), who initiated these studies. Van der Ziel [241], [242] and Van Vliet [243], as well as other eminent researchers contributed to these studies [244][245].

Currently, related numerical methods, such as the very promising transfer impedance method, can lead to some results, but most of the time, it will lead to 1D.

- Random functions

A random variable is a real or complex number, the value of which depends on chance, (that is, *a priori*, unpredictable) meaning that it depends on a "proof". A random function is one for which the value is constantly dependent on chance. A simple random function depends on one or more random variables. To know the value of the function at a specific moment t, then, there is a random variable x (f) that can be described by its probability density p (x, t) or, briefer still, by certain moments: $<X^1(t)>$, $<X^2(t)>$, etc. (average values are also called expectations and marked E; thus: $E\{X(t)\}$, $E\{X^2(t)\}$ …)

It will also be interesting to look at properties at two given instants: a moment that plays a specifically important role is covariance or correlation: [172], [173], [246]

$$\Gamma\big(X(t_1,t_2)\big) =< X(t_1)X^*(t_2) > \tag{5-1}$$

$X^*(t_2)$ is the complex conjugate of $X(t_2)$

- Second order stationary random functions:

In numerous cases, we deal with at least second order random functions. These functions have the following properties: [172], [173], [246]

a) They are first-order stationary:

$$< X(t) >= m \tag{5-2}$$

b) Let us use second order stationarity

$$\Gamma\big(X(\tau)\big) =< X(t)X^*(t-\tau) > \tag{5-3}$$

For $\tau = 0, \Gamma\big(X(0)\big) =< |X(t)|^2 >$

From the stationarity, we directly get:

$$\Gamma\big(X(\tau)\big) = \Gamma\big(X^*(-\tau)\big) \tag{5-4}$$

- Wiener-Khinchin theorem

If the signal can be written as a Fourier-Stieltjes transform, complex exponentials on elementary growth dx(ν) :

$$X(t) = \int_{-\infty}^{\infty} e^{2i\pi\nu t}\, dx(\nu) \tag{5-5}$$

Taking (5-2) and (5-5) into consideration, the average, which is constant, can be written as:

$$m = \int_{-\infty}^{\infty} e^{2i\pi\nu t} < dx(\nu) > \tag{5-6}$$

From which we get

$$< dx(\nu) > = m\delta(\nu)d\nu \qquad (5\text{-}7)$$

Thus, $< dx(\nu) >$ is independent of ν and non-zero only when $\nu = 0$.

Now, if we take second order stationarity into account, that is, if we substituted $X(t)$ and $X^*(t-\tau)$ with their values:

$$\Gamma_X(\tau) = < \int_{-\infty}^{+\infty} e^{2i\pi\nu t}\, dx(\nu) \cdot \int_{-\infty}^{+\infty} e^{-2i\pi(t-\tau)}\, dx^*(\nu') > \qquad (5\text{-}8)$$

$$\Gamma_X(\tau) = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} < dx(\nu)dx^*(\nu') > e^{2i\pi(\nu\prime)\tau} e^{2i\pi(\nu-\nu\prime)\tau} \qquad (5\text{-}9)$$

$\Gamma_X(\tau)$ must be independent of t, and so all $\nu \neq \nu$ terms are zero. The integral (IV.18) must be zero. Thus, we can write:

$$< dx(\nu)\, dx^*(\nu') > = \delta(\nu - \nu')\gamma_X(\nu)d\nu d\nu' \qquad (5\text{-}10)$$

Thus, there is no correlation between different frequencies for second order stationary functions. The $\gamma_X(\nu)$ quantity is called spectral density of fluctuation of X. It is observed on the whole frequency spectrum, positive and negative. In general, we only take positive frequencies, and the measurable physical quantity S_X (f) is defined by: [172], [173], [246]

$$S_X(f) = S_X(f) = \gamma_X(\nu = f) + \gamma_X(\nu = -f) \qquad (5\text{-}11)$$

$$\Gamma_X(\tau) = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} \delta(\nu - \nu')\gamma_X(\nu) e^{2i\pi\nu\prime\tau} e^{2i\pi(\nu-\nu\prime)\tau}\, d\nu\, d\nu' \qquad (5\text{-}12)$$

After integrating on ν', [172], [173], [246]

$$\Gamma_X(\tau) = \int_{-\infty}^{+\infty} e^{2i\pi\nu\tau}\, \gamma_X(\nu)\, d\nu \qquad (5\text{-}13)$$

$\Gamma_X(\tau)$ is the Fourier transform of the spectral density: [172], [173], [246]

$$\gamma_X(\nu) = \int_{-\infty}^{+\infty} e^{-2i\pi\nu\tau}\, \Gamma_X(\tau)\, d\tau \qquad (5\text{-}14)$$

Equations (5-3) and (5-14) relate to the Wiener-Khinchin theorem.

- Properties of spectral density of fluctuation.

a) Complex conjugate of equation (5-14):

By taking (5-14) into consideration and adding $\theta = t - \tau$, we get: [172], [173], [246]

$$\gamma_X^*(\nu') = -\int_{-\infty}^{+\infty} \Gamma_X^*(-\theta)e^{-2i\pi\nu\theta}\, d\theta = \int_{-\infty}^{+\infty} \Gamma_x(\theta)e^{-2i\pi\nu\theta}\, d\theta = \gamma_X(\nu) \qquad (5\text{-}15)$$

Hence, $\gamma_X^*(\nu)$ is a real quantity. It is positive.

b) White noise: the noise is said to be white if $\gamma_X(\nu)$ is constant, irrespective of ν, equation (5-13) will be

$$\Gamma_X(\tau) = \int_{-\infty}^{+\infty} A\, e^{-2i\pi\nu t}\, d\tau = A\delta\tau \quad (5\text{-}16)$$

When a noise is white, it means that successive events are not correlated. In practice, correlation is nonzero on in small time intervals τ_0.

τ_0 is the relaxation time of the system and we get: $\Gamma_X(\tau) = 0$ si $\tau > \tau_0$. In other words, $\gamma_X(\nu)$ is constant when $\nu < 1/\tau_0$

5.2) Noise calculation using the Langevin method

- Principle of this Method [247]

Of a very general scope, the Langevin method, which is applied to electronic noise, involves replacing the real device with a no-noise device in series with a noise source.

If η is the noise source, then the linear Langevin operator applied to the random variable is the said noise source, i.e.: [172], [173], [246]

$$\hat{L}X(t) = \eta(t) \quad (5\text{-}17)$$

If the average value of X(t) is zero, then we get: [172], [173], [246]

$$\hat{L} < X(t) >=< \eta(t) >= 0 \quad (5\text{-}18)$$

And

$$X(t) = \int_{-\infty}^{\infty} e^{2i\pi\nu t}\, dx(\nu) \quad (5\text{-}19)$$

$$\eta(t) = \int_{-\infty}^{\infty} e^{2i\pi\nu t}\, d\varsigma(\nu) \quad (5\text{-}20)$$

Where $e^{2i\pi\nu t}$ is an eigenvector of $\hat{L}$, Z(ν) being its eigenvalue. Thus, we can write:

$$\hat{L}\, e^{2i\pi\nu t} = Z(\nu).e^{2i\pi\nu t} \quad (5\text{-}21)$$

So, the noise spectral densities are connected via:

$$S_\varsigma(f) = |Z'(\nu, f)^2| S_x(f) \quad (5\text{-}22)$$

We see that the phase does not interfere here, with regard to second order properties.

- Example: Generation—Recombination noise

In a semiconductor bar, we can generate ΔN number of new carriers, by lighting, for instance. If τ is the carrier lifetime, we can write: [172], [173], [246]

$$\frac{d\Delta n}{dt} = -\frac{\Delta n}{\tau} \quad (5\text{-}23)$$

If we focus on fluctuations:

$$\frac{d\Delta n}{dt} = -\frac{\Delta n}{\tau} + \mathrm{N}(t) \quad (5\text{-}24)$$

If the source is harmonic:

$$\mathrm{N}(t) = \mathrm{N}_0 e^{j\omega t} \quad (5\text{-}25)$$

Δn is also harmonic (cf. linearity):

$$\Delta n(t) = \Delta N e^{j\omega t} \quad (5\text{-}26)$$

Then, we get: [172], [173], [246]

$$\mathrm{S}_N(f) = \mathrm{S}_{\Delta n}(f)\left|\frac{1}{\tau} + j\omega t\right|^2 \quad (5\text{-}27)$$

$$\mathrm{S}_{\Delta N}(f) = \mathrm{S}_\eta(f)\frac{\tau^2}{1+\omega^2\tau^2} \quad (5\text{-}28)$$

If it is white noise, [172], [173], [246]

$$<\Delta \mathrm{N}^2> = \int_0^\infty \mathrm{S}_{\Delta N}(f)df = \mathrm{S}_\eta\,\tau^2\int_0^\infty \frac{1}{1+4\pi^2 f^2\tau^2}df = \mathrm{S}_\eta\frac{\tau}{4} \quad (5\text{-}29)$$

Thus:

$$\mathrm{S}_{\Delta N}(f) = 4<\Delta \mathrm{N}^2>\frac{\tau}{1+\omega^2\tau^2} \quad (5\text{-}30)$$

We know the spectrum if $<\Delta \mathrm{N}^2>$ is white; we then use a master equation that regulates microscopic phenomena.

- Quantities associated to Noise in Electricity

Let us take the Langevin theorem again: [172], [173], [246]

$$\mathrm{S}_V(f) = |Z(f)|^2\mathrm{S}_I(f) \quad (5\text{-}31)$$

$$Z(f) = \frac{\Delta V}{\Delta I} \quad (5\text{-}32)$$

ΔV is complex voltage (cf. sinusoidal regime), superimposed at the quiescent point, continuous and induced by ΔI.

We can then define an equivalent noise temperature T_n, such as: [172], [173], [246]

$$\mathrm{S}_V(f) = 4k\mathrm{T}_n(f)\mathrm{Re}(Z(f)) \quad (5\text{-}33)$$

Or

$$\mathrm{S}_I(f) = 4k\mathrm{T}_n(f)\mathrm{Re}(Y(f)) \quad (5\text{-}34)$$

Avec

$$Z(f) = 1/Y(f) \quad (5\text{-}35)$$

Finally, we can define an equivalent noise current, I_n, in the following manner:

$$\mathrm{S_I}(f) = 2q\mathrm{I_n}(f) \quad (5\text{-}36)$$

Thus, spectral densities are linked to the square modulus of the complex impedance. This concerns macroscopic fluctuations. If the source term is known, the fluctuation of the quantity studied can be deduced. It is also noted that even if the source has white noise, a normal assumption, the variable studied does not, in general, have white noise. Z depends on the frequency.

Observations:

1. To know one of the two terms, I (f) or S (f), we use microscopic conditions, via master equations (Boltzmann, Fokker-Planck equations, etc.),

2. We will see that it is absolutely necessary for the operator to be linear in order for the equation (5-26) to be applied; else, the Langevin description cannot be applied.

It is only when L is linear that we get a noise source with an average value of zero, and thus find the noiseless system equation.

If the system is not linear, equation (5-26) can be linearized, because, in general, we focus on the small fluctuations around the mean value. So, we can then use $\mathrm{X(t)} = X_0 + \Delta\mathrm{X(t)}$ and linearize equation (5-26), given that$< X_0 >= 0$.

- Example application: Thermal noise of a Resistor:

Let us take a circuit (L, R); we find the spectral density of the noise current in the circuit, through which a zero average current flows. For this, we insert a source $v(t)$ in the perfect circuit and the circuit obeys the equation [172], [173], [246]

$$L\frac{di}{dt} + Ri = v(t) \quad (5\text{-}37)$$

We get:

$$v = V_m e^{j\omega t} \quad (5\text{-}38)$$
$$i = I_m e^{j\omega t} \quad (5\text{-}38)$$

The result is well-known:

$$V_m = ZI_m \quad (5\text{-}39)$$
$$Z = R + j\omega L \quad (5\text{-}39)$$

Thus:

$$S_V(f) = |Z|^2 S_I(f) \quad (5\text{-}40)$$

$$S_I(f) = \frac{S_V(f)}{R^2+L^2\omega^2} \quad (5\text{-}40)$$

Now, let us consider the microscopic aspect and calculate $< i^2 >$. The average energy stored inside the coil is:

$$\frac{1}{2}Li^2 \quad (5\text{-}41)$$

In 1D, we can write: [172], [173], [246]

$$\frac{1}{2}Li^2 = \frac{1}{2}kT \quad (5\text{-}41)$$

Yet:

$$< i^2 >= \int_0^\infty S_i(f)\, df = \int_0^\infty \frac{df}{R^2+4\pi^2L^2f^2} = \frac{S_V}{4RL} \quad (5\text{-}42)$$

So:

$$S_V = 4kRT(\text{Nyquist theorem}) \quad (5\text{-}43)$$

$$S_I = 4kT\frac{R}{R^2+L^2\omega^2} \quad (5\text{-}44)$$

- Forms of Langevin Equations

Langevin equations often involve several coupled equations for $X_1(t), X_2(t)$ variables, the average value of which satisfy the relationship of the form: [172], [173], [246]

$$\frac{\partial < x_i(t) >_{cond}}{\partial t} + \sum_i M_{ij} < x_i(t) >_{cond} = 0 \quad (5\text{-}45)$$

$< x_i(t) >_{cond}$ is a conditional mean respecting the given initial conditions. This is the case, for example, with electric circuits where initial conditions must be set; these equations are valid around the polarization point for all nonlinear systems. If derivatives of an order higher than 1 appear, the order of the system is to be reduced; for example, for a second order system, we construct a new random variable, first derivative of the initial variable

It can be shown that these phenomenological equations are equivalent to a Langevin description, which is the set of unconditional regression equations

The related Langevin description is: [172], [173], [246]

$$\frac{\partial < x_i(t) >}{\partial t} + \sum_j M_{ij} < x_j(t) > = \varsigma(t) \quad (5\text{-}46)$$

Given that the source terms are mean zero and have white noise.

- Example: Electron injection in p area of a PN junction.

In an ohmic regime, the transport equation without generation-recombination: $-\partial n/\partial t$), is written as:

$$\frac{\partial <\Delta n(\vec{r},t)>_{cond}}{\partial t} = -\frac{<\Delta n(\vec{r},t)>_{cond}}{\tau} + \frac{1}{e}\nabla < \Delta \vec{j_n}(\vec{r},t) >_{cond} \quad (5\text{-}47)$$

And also: [172], [173], [246]

$$< \Delta j_n(\vec{r},t) >_{cond} = -e\,\mu_n < \Delta n(\vec{r},t) >_{cond} \vec{E} + e\,D_n < \Delta n(\vec{r},t) >_{cond} \quad (5\text{-}48)$$

$$\frac{\partial \Delta n(\vec{r},t)}{\partial t} = -\frac{\Delta n(\vec{r},t)}{\tau} + \frac{1}{e}\vec{\nabla}.\Delta \vec{j_n}(\vec{r},t) + \varsigma_n(\vec{r},t) \quad (5\text{-}49)$$

$$\Delta j_n(\vec{r},t) = -e\,\mu_n \Delta n(\vec{r},t)\vec{E} + eD_n < \Delta n(\vec{r},t) >_{cond} \vec{\eta}_n(\vec{r},t) \quad (5\text{-}50)$$

Analogously, for holes: [172], [173], [246]

$$\frac{\partial \Delta p(\vec{r},t)}{\partial t} = -\frac{\Delta p(\vec{r},t)}{\tau} - \frac{1}{e}\vec{\nabla}.\Delta \vec{j_{np}}(\vec{r},t) + \varsigma_p(\vec{r},t) \quad (5\text{-}51)$$

$$\Delta j_p(\vec{r},t) = +e\,\mu_p \Delta p(\vec{r},t)\vec{E} - e\,D_p\vec{\nabla}.\Delta n(\vec{r},t) >_{cond} + e\vec{\eta}_p(\vec{r},t) \quad (5\text{-}52)$$

ς_n *and* ς_p are noise sources.

5.3) Noise calculation using the impedance field method

- Principle of the method [248], [249]

The impedance field method was introduced by W. Shockley et al. [250]. This method differs from the Langevin method in the way it links the macroscopic quantity to elementary microscopic fluctuations. The spectral density of voltage fluctuations can be brought down to two basic calculations: that of the spectral density of voltage fluctuation and that of elementary fluctuations.

- Impedance fields:

Let us consider a polarized specimen between electrode N and the grounding. If we inject a little current ΔI, flowing out of N, at a coordinate point $\overrightarrow{r}$ in the volume the potential of N varies by $\Delta V(N,\overrightarrow{r})$.

Each noise course at the coordinate point $\overrightarrow{r}$ in the substrate (and also in the devices) produces a noise in another point of the volume and the surface (and electrodes).

The noise induced depends on its sources and its way of propagation via the impedance field. In order to study the noise between two contacts on the surface or in the substrate, we inject a little current (noise) that is complex, ΔI, at frequency f, at a coordinate point $\overrightarrow{r}(+/-\overrightarrow{dr})$ in the substrate, superimposed on a continuous current between the contacts. This little current produces a potential V(f) in another contact. Thus, we can write: [172], [173], [246]

$$\Delta V(r+dr) = Z(r+dr)\delta I \quad (5\text{-}53)$$

Z(r,f) is an impedance.

The resulting difference in voltage is:

$$\delta V = \Delta V(r+dr) - \Delta V(r) = \vec{\nabla} Z dr \Delta I \quad (5\text{-}54)$$

Where Green's function $\vec{\nabla} Z(\Delta I = 1)$ is called the impedance field .

$\delta I dr$ can be described by the current density $\delta j(r)$ in an infinitesimal volume dr^3:

$$\delta I dr = \delta j(r) dr^3 \quad (5\text{-}55)$$

δj is the current density (A.m^{-2})

By injecting (5-55) in (5-54) we get:

$$\delta V_f(r) = \big(Z(r,f) - Z(r-dr,f)\big)\delta I = \vec{\nabla} Z(r,f)\overrightarrow{dr}\delta I \quad (5\text{-}56)$$

$$\delta V_f(r) = \vec{\nabla} Z(r,f)\delta j(r) dr^3 \quad (5\text{-}57)$$

Equation (5-57) means that a current fluctuation in the dr^3 volume produces a voltage difference between two other contacts. Integrating on the domain considered, the total voltage produced by these currents is: [172], [173], [246]

$$\Delta V_f = \int \vec{\nabla}\, \mathrm{Z}\,(\mathrm{r},\mathrm{f})\delta j(r) dr^3 \quad (5\text{-}58)$$

In order to explicitly calculate the noise density of $S_V(f)$, we project devices, for example Cartesian, in x, y and z direction; in a direction, we get:

$$\Delta V_f = \sum_\alpha \left[\int \frac{\partial \mathrm{Z}(\mathrm{r},\mathrm{f})}{\partial \alpha} \vec{\nabla}\, \mathrm{Z}\, .\delta \mathrm{j}_\alpha(\mathrm{r}).\mathrm{dr}^3\right] \quad (5\text{-}59)$$

Thus, the voltage noise spectral density at the junctions becomes

$$\mathrm{S_v(f)} = 2\int_{-\infty}^{\infty} \Gamma_{\delta \mathrm{V}(}\mathrm{N},\vec{\mathrm{r}},\mathrm{t}).\mathrm{e}^{2\pi \mathrm{ift}}\mathrm{dt} \quad (5\text{-}60)$$

Where $\Gamma_{\delta \mathrm{V}(}\mathrm{N},\vec{\mathrm{r}},\tau))$ is the correlation function:

$$\Gamma_{\delta \mathrm{V}} = \big(\delta V_f(\mathrm{t}).\delta \mathrm{V_f^*(t+\tau)} \quad (5\text{-}61)$$

Density becomes: [172], [173], [246]

$$\mathrm{S_v(f)} = \sum_\alpha \sum_\beta \iint \frac{\partial \mathrm{Z'(r,f)}}{\partial \alpha}.\frac{\partial \mathrm{Z^*(r','f)}}{\partial \beta}.2.\int_{-\infty}^{\infty} \overline{\delta \mathrm{j}_\alpha \delta \mathrm{j}_\beta^*(\mathrm{r'},\mathrm{t}+\tau)}\, \mathrm{e}^{2\pi \mathrm{fi}\tau}\mathrm{d}\tau.\mathrm{dr}^3\mathrm{dr'}^3 \quad (5\text{-}62)$$

$$\mathrm{S_v(f)} = \sum_\alpha \sum_\beta \iint \frac{\partial \mathrm{Z'(r,f)}}{\partial \alpha}.\frac{\partial \mathrm{Z'(r',f)}}{\partial \beta}.\mathrm{S_{j\alpha\beta}(r,r'',f)}\mathrm{dr}^3\mathrm{dr'}^3 \quad (5\text{-}63)$$

$$\mathrm{S_v(f)} = \iint \vec{\nabla} \mathrm{Z'(r,f)} \cdot \mathrm{Sj(r,r'',f).'}\, \vec{\nabla} \mathrm{Z^*(r'',f)}\, \mathrm{dr}^3\mathrm{dr'}^3 \quad (5\text{-}64)$$

If K is a noise source:

$$\mathrm{S_{j\alpha\beta}(r,r'',f)} = \mathrm{K_{\alpha\beta}(r,f)}\delta(\mathrm{r'} - \mathrm{r}) \quad (5\text{-}65)$$

Equation (5-65) simplifies into: [172], [173], [246]

$$S_v(f) = \int \vec{\nabla} Z(r,f) \cdot K(r,f) \cdot \vec{\nabla} Z^*(r',f) \quad (5\text{-}66)$$

- Calculation of impedance field

Calculating the impedance field is easy in the case of homogenous samples. But in the casa of non-homogenous samples, in space charge regime, for instance, some precautions must be taken.

a) We determine the working regime that is the polarization point, by:

- Solving local equations (Poisson's equation, electric neutrality, phenomenological expression of current density, etc.)

- Taking boundary conditions into account, that is, for electrodes, to determine integration constants in the preceding differential equations.

Thus, we get the local mean field $E_0(r)$ based in the average current density j_0.

The average voltage at junctions in the sample is: [172], [173], [246]

$$V_0 = -\int_{N_0}^{N} \vec{E}_0(\vec{r}).d\vec{r} \quad (5\text{-}67)$$

Where N_0 and N are the electrodes. The average current is:

$$I_0 = \iint \overrightarrow{J_0}.\overrightarrow{D_S} \quad (5\text{-}68)$$

Where S is a slice of the sample, for instance, the surface of an electrode.

b) We calculate the fluctuations of the electric field resulting from introducing current ΔI at coordinate point $\vec{r}$. This $\Delta\vec{E}(\vec{r},\vec{r}')$ field is obtained as follow: [172], [173], [246]

$$\vec{E}(\vec{r}') = \overrightarrow{E_0}(\vec{r}') + \Delta\vec{E}(\vec{r},\vec{r}') \text{ and } \vec{j}(\vec{r}') = \overrightarrow{j_0}(\vec{r}') + \Delta\vec{j}(\vec{r},\vec{r}') \quad (5\text{-}69)$$

The Δ being considered as disturbances with regard to E_0 and I_0, these zero order terms give the equations for mean values, while the first order terms in ΔE and ΔI give linear equations. Local Langevin equations thus obtained are solved and the integration constants are determined by imposing the same boundary conditions on $\Delta\vec{E}$ as those applied on $\overrightarrow{E_0}$. For $\Delta\vec{E}$, these conditions are at the level of electrode N and the $\vec{r}$ point, and at N and No for $\overrightarrow{E_0}$. Thus, we get $\Delta\vec{E}(\vec{r},\vec{r}')$.

c) We then deduce the impedance gradient

- *Example application: noise in ohmic space charge regime (simple injection)*

The sample is assumed to be a parallelepiped; we are dealing with a longitudinal unidimensional case. The space charge is not negligible and can make the device's characteristics nonlinear.

We distinguish between the two different regimes:

a) when the space charge of the injected carriers is very weak to significantly affect the volume's conductivity, we get the ohmic regime, where the mean current is proportional to the voltage at the junctions of the sample: $I_0 \propto V_0$. [172], [173], [246]

$$j = -\mathrm{q}\mu\mathrm{n}\mathrm{E} + \varepsilon\frac{\partial \mathrm{E}}{\partial \mathrm{t}} \tag{5-70}$$

$$\frac{\partial \mathrm{E}}{\partial \mathrm{x}} = \frac{-\mathrm{q}}{\varepsilon}(\mathrm{n} - \mathrm{N_D}) \tag{5-71}$$

$$j_n(\vec{r},t) = e\,\mu_n E\left(\mathrm{N_{D+}}\frac{\varepsilon}{\mathrm{e}}\frac{\partial \mathrm{E}}{\partial \mathrm{t}}\right) + \varepsilon\frac{\partial \mathrm{E}}{\partial \mathrm{t}} \tag{5-72}$$

(q = -e, >0)

As for fluctuations: [172], [173], [246]

$$\mathrm{E} = E_0 + \Delta E e^{jwt} \tag{5-73}$$

$$\mathrm{n} = n_0 + \Delta n e^{jwt} \tag{5-74}$$

$$\mathrm{j} = j_0 + \Delta J e^{jwt} \tag{5-75}$$

$$\Delta j_n(\vec{r},t) = e.\mathrm{N_D}\,\mu\Delta E + \varepsilon\mu\mathrm{E_0}\frac{\partial \Delta \mathrm{E}}{\partial \mathrm{x}} + \varepsilon\mu\Delta\mathrm{E}\frac{\partial \mathrm{E_0}}{\partial \mathrm{x}} + \mathrm{i}\varepsilon\omega\Delta\mathrm{E} \tag{5-76}$$

Hence:

$$\varepsilon\mu\mathrm{E_0}\frac{\partial \Delta \mathrm{E}}{\partial \mathrm{x}} + (e\,\mu\mathrm{N_D} + \varepsilon\mu\frac{\partial \mathrm{E_0}}{\partial \mathrm{x}} + \mathrm{i}\varepsilon\omega)\Delta\mathrm{E} = \Delta j_n \tag{5-77}$$

If n=N_D

$$\varepsilon\mu\mathrm{E_0}\frac{\partial \Delta \mathrm{E}}{\partial \mathrm{x}} + (-e\,\mu_n + \mathrm{i}\varepsilon\omega)\Delta\mathrm{E} = \Delta j_n \tag{5-78}$$

$$\varepsilon\mu\mathrm{E_0}\frac{\partial \Delta \mathrm{E(x,x')}}{\partial \mathrm{x}} + (e\mu\mathrm{N_D} + \mathrm{i}\varepsilon\omega)\Delta\mathrm{E'x,x'}) = \Delta j_n \tag{5-79}$$

The solution is:

$$\Delta\mathrm{E(x,x')} = \frac{\Delta j_n}{-e\,\mu_n + \mathrm{i}\varepsilon\omega} + \mathrm{K(x)e}^{-\frac{e\,\mu_n\mathrm{N_D} + \mathrm{i}\varepsilon\omega}{\epsilon\mu_0\mathrm{E_0}}\mathrm{x'}} \tag{5-80}$$

$$\Delta\mathrm{E(x,x')} = \frac{\Delta j_n}{e\,\mu_n + \mathrm{i}\varepsilon\mu\omega} + (1 - \mathrm{e}^{\frac{e\,\mu\mathrm{N_D} + \mathrm{i}\varepsilon\mu\omega}{\epsilon\mu_0\mathrm{E_0}}(\mathrm{x} - \mathrm{x'})}) \tag{5-81}$$

The impedance gradient is defined by:

$$\frac{\partial Z(N,x)}{\partial x} = -\frac{1}{\Delta \mathrm{I}}\int_x^L \frac{\partial \Delta \mathrm{E}(x,x''))}{\partial x}dx' \tag{5-82}$$

Then if the diffusion length is much smaller than that of the sample, we can write:

$$\frac{\partial Z(N,x)}{\partial x} = \frac{\Delta j_n}{S(\mathrm{i}\varepsilon\omega^{\circ}\, e\,\mu_n)}.(1 - \mathrm{e}\frac{e\,\mu\mathrm{N_D} + \mathrm{i}\varepsilon\omega^{(\mathrm{x} - \mathrm{L})}}{\epsilon\mu_0\mathrm{E_0}}) \tag{5-83}$$

As for the noise,

$$\frac{\partial Z(N,x)}{\partial x} = \frac{\Delta j_n}{S(\mathrm{i}\varepsilon\omega \mp e\,\mu_n D)} \tag{5-84}$$

Using the Einstein relationship,

$$\frac{kT}{q} = D/\mu \tag{5-85}$$

We get:

$$S_v = 4e^2 D\mu . \frac{nL}{(S\varepsilon\omega)^2 + (Se\ \mu N_D)^2} \tag{5-86}$$

Finally,

$$S_v = 4kT \frac{R}{1+(\omega RC)^2} \tag{5-87}$$

It is the noise of the parallel RC circuit, where

$$C = \varepsilon S/L \tag{5-88}$$
$$R = L/(q\mu nS) \tag{5-88}$$

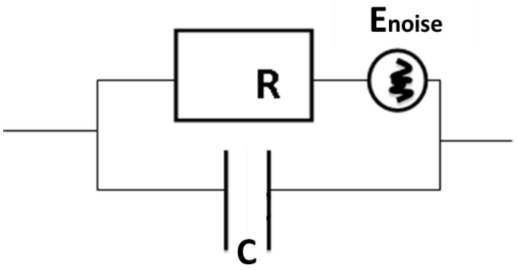


Figure 118 RC noise study circuit [172], [173]

$$Z_{eq} = (\frac{1}{R} + j\omega C)^{-1} = R(1 + j\omega RC)^{-1} c \tag{5-89}$$

Thus:

$$S_v = 4kRT \frac{1}{1+(\omega RC)^2} \tag{5-90}$$

5.4) Noise calculation using the transfer impedance method principle: formulation

We get seen in the impedance field method that a current generator in a dx slice induces a voltage variation at the junctions of the whole device. [248], [251], [252]

As we get suggested, Green's algorithm may be linked to a transfer impedance, considering the signal fluctuations. Injecting a current variation to a contact creates a potential variation at any other contract. Similarly, we must be able to analyze possible correlations between different noise sources autonomous *ab initio* but very close (cf. nano-electronics).

We consider another paradigm: the transfer impedance method (TIM); between two points, two slices, or two volume elements, via a linear relationship between the electric field response or the potential difference at a current disturbance, situated far away. Hence, we get the possibility of

calculating internal noise spectra that comes from these fluctuations. This method, generalizing the original impedance field method of Shockley et al., was widely used in recent decades to calculate noise and is only efficient in 1D. The important role of this method was, and still is, to calculate the entire range of voltage fluctuations between the device's junctions. Currently, the problem remains unsolved in 3D (even in 2D), not because of the numerical difficulties, but in a physical point of view.

- PRINCIPLE

A current generator induces a voltage variation in every dx slice. The result is that two distinct slices can be correlated. Thus, we cannot write that the spectral density (d.s.) of voltage at junctions of the whole set is the sum of d.s. of voltage of each separate slice (cf. Salami method).

The $\Delta v(x), \Delta v(x')$ cross terms must be added. More specifically, let us consider two slices, numbered as α and β. Microscopic noise sources, each sheltered by a noise current generator marked Si_α and Si_β, are untiled, but not the voltage fluctuations induced by these noise sources. Voltage induced at junctions of slice β by current i_α is $Z_{\beta\alpha}(w)i_\alpha$ where $Z_{\beta\alpha}$ is the transfer impedance between slices α and β. As a consequence, the total voltage induced at the junctions of β for all the current generators of different slices is: [172], [173], [246]

$$\Delta V_\beta = \sum_\alpha z_{\beta\alpha} i_\alpha \tag{5-91}$$

i_α *and* i_β are untiled, we get: [172], [173], [246]

$$S_v \Delta f = \sum_{\alpha\gamma}^{\infty} \overline{|i_\alpha{}^2|} z_{\beta\alpha} z^*_{\alpha\gamma} \tag{5-92}$$

$$\vec{E}(\vec{r}) = \vec{E_0}(\vec{r}) + \delta\vec{E}(\vec{r}, \omega)e^{i\omega t} \tag{5-93}$$

$$\vec{j}(\vec{r}) = \vec{j_0}(\vec{r}) + \delta\vec{j}(\vec{r}, \omega)e^{i\omega t} \tag{5-94}$$

The first order terms are linked via an operator $\hat{L}$: [172], [173], [246]

$$\hat{L}\, \delta\vec{E}(\vec{r}, \omega) = \delta\vec{j}(\vec{r}, \omega) \tag{5-95}$$

We can then introduce Green's functions of the operator $\hat{L}$

$$\hat{\vec{L}}\, \vec{\vec{z}}\left(\vec{r}, \vec{r'}, \omega\right) = \vec{\vec{1}}.\delta\left(\vec{r} - \vec{r'}\right) \tag{5-96}$$

Where $\vec{\vec{1}}$: unit matrix

$$\delta\vec{E}(\vec{r}, \omega) = \iiint \vec{\vec{z}}\left(\vec{r}, \vec{r'}, \omega\right) \delta\vec{j}(\vec{r'}, \omega) d^3r' \tag{5-97}$$

The ddp at junctions of a "dr" on an inter-electrode line can be written as:

$$\delta V^2 = -\int_0^L dr^T \iiint \vec{\vec{z}}\left(\vec{r}, \vec{r'}, \omega\right) \delta\vec{j}(\vec{r'}, \omega) d^3r' \tag{5-98}$$

And so, between 2 electrodes:

$$\delta V = -\int_0^L dr^T \iiint \vec{\vec{z}}\left(\vec{r},\vec{r'},\omega\right)\delta\vec{j}(\vec{r},\omega)d^3r' \quad (5\text{-}99)$$

Finally, for a material of L length, after some simple calculation that may be a little "heavy", we get: [172], [173], [246]

$$S_v\Delta f(\omega) = \int_0^L\int_0^L \iiint d^3r'' \iiint d^3r'''dr^T \vec{\vec{z}}\left(\vec{r},\vec{r''},\omega\right)\vec{J_N}\left(\vec{r''},\omega\right).\vec{J_N}'(\vec{r'''},\omega) \Rightarrow_{z^T}\left(\vec{r'},\vec{r'''},\omega\right)dr' \quad (5\text{-}100)$$

We also have the spectral density of current fluctuation:

$$\vec{J_N}\left(\vec{r''},\omega\right).\vec{J_N}'\left(\vec{r'''},\omega\right)=K\left(\vec{r''},\omega\right).\delta\left(\vec{r''}-\vec{r'''}\right)\Delta f \quad (5\text{-}101)$$

K is the noise source.

If we want to get "ddps" or impedance of the whole sample, curvilinear integrals must be calculated. Currently, some calculations can be carried out only in 1D, and this is a huge hurdle.

Equation (5-100) is written as: [172], [173], [246]

$$S_v(\omega) = \iint \vec{\nabla}Z(r,\omega)\cdot Sj(r,\omega)\nabla Z^T dr^3 \quad (5\text{-}102)$$

To be compared with ((5-78) - cf. impedance field).

Note: $S_v(\omega)$ is zero if the Z gradient is zero. Hence, we can create a (straight) strongly and uniformly doped slice between the noise source and a target to be protected.

- One-dimensional structures: Noise of a bar in ohmic regime in high frequencies.

$$E = E_0 + \Delta E e^{jwt} \quad (5\text{-}103)$$
$$n = n_0 + \Delta n e^{jwt} \quad (5\text{-}104)$$
$$j = j_0 + \Delta J e^{jwt} \quad (5\text{-}105)$$
$$j = -q\mu nE + \varepsilon\frac{\partial E}{\partial t} \quad (5\text{-}106)$$
$$\frac{\partial E}{\partial x} = \frac{-q}{\varepsilon}(n - N_d) \quad (5\text{-}107)$$

In high frequencies, we can write:

$$\frac{\delta v}{\delta E} = \frac{\mu_0}{1+i\omega\tau} \quad (5\text{-}108)$$

Note: In very low frequencies, $\frac{\delta v}{\delta E}$ tends towards μ_0 and in ohmic regime $\frac{\partial E}{\partial x}$ =0, thus, n=Nd

$$\delta I = -qA(n_0\delta v + v_0\delta n) + ieA\omega\delta E \quad (5\text{-}109)$$

Where A is a square section.

$$\delta I = (\frac{qAn_0\mu_0}{1+i\omega\tau} + i\omega A)\delta E - qAv_0\delta n \quad (5\text{-}110)$$

$$\delta I = (\frac{qAn_0\mu_0}{1+i\omega\tau} + i\omega A)\delta E - \epsilon A\mu_0 E_0 \frac{\partial \delta E}{\partial x} \quad (5\text{-}111)$$

As for transfer impedance: [172], [173], [246]

$$\epsilon A\mu_0 E \frac{\partial z(x,x,\omega)}{\partial x} + (\frac{qAn_0\mu_0}{1+i\omega\tau} + i\omega\epsilon A)z(x,x,\omega) = \delta'(x-x') \quad (5\text{-}112)$$

The solution for this differential equation is then:

$$z(x,x',\omega) = Ke^{\frac{qn_0\mu_0-\omega^2\tau\epsilon+i\omega\epsilon_0}{\epsilon\mu_0 E_0}x} \quad (5\text{-}113)$$

Via, for example, the variation of constants theorem, we get K [172], [173], [246]

$$K = -\frac{1+i\omega\tau}{AE_0\epsilon\mu_0} + i\omega\epsilon A e^{-\lambda x'} H(x-x') + C \quad (5\text{-}114)$$

Where H is the Heaviside step function;

And:

$$\lambda = \frac{qn_0\mu_0-\omega^2\tau\epsilon+i\omega\epsilon}{\epsilon_0\mu_0 E_0} \quad (5\text{-}114)$$

Introducing δI in x' results in x>x' if we ignore the diffusion.

In short:

$$z(x,x',\omega) = -\frac{1+i\omega\tau}{A\epsilon_0\mu_0 E_0} e^{\frac{(qn_0\mu_0-\omega^2\tau\epsilon+i\omega\epsilon)(x-x')}{\epsilon\mu_0 E_0}} H(x-x') \quad (5\text{-}115)$$

Hence, we have its gradient:

$$\vec{\nabla} z(x',\omega) = \frac{1+i\omega\tau}{A\epsilon_0\mu_0 E_0}(1 - e^{\frac{(qn_0\mu_0-\omega^2\tau\epsilon+i\omega\epsilon).(L-x')}{\epsilon\mu_0 E_0}}) \quad (5\text{-}116)$$

In ohmic regime (E constant, very weak): $\lambda \to \infty$ we get:

$$lim_{E_0\to 0}\vec{\nabla} z(x',\omega) = \frac{1+i\omega\tau}{A(qn_0\mu_0-\omega^2\tau\epsilon+i\omega\epsilon)} \quad (5\text{-}117)$$

Diffusion noise power is thus:

$$S_V = 4q^2 A\int_0^L n_0 D_0 |\nabla Z|^2 dx \quad (5\text{-}118)$$

Yet, in ohmic regime: $kT/q = D_0/\mu_0$ [172], [173], [246]

$$S_V = 4\frac{kT}{Aqn_0\mu_0}L = 4kT\frac{L}{\sigma_0 A} = 4kRT \quad (5\text{-}119)$$

σ_0 is the ohmic conductivity

We get the well-known Nyquist-Johnson relationship (5-119).

Note: The approach for calculating the impedance field, in practice, can be to force the AC sources at each mesh node of the device and evaluate the response at the device's electrodes.

A method derived from the system principle is simpler to implement; we calculate the trans-impedance Z_{ij}, where i is any node and j is an electrode. As a consequence, $Z_{ij} = Z_{ji}$; it can be checked by applying an AC source at a terminal and calculating the internal potentials at each node.

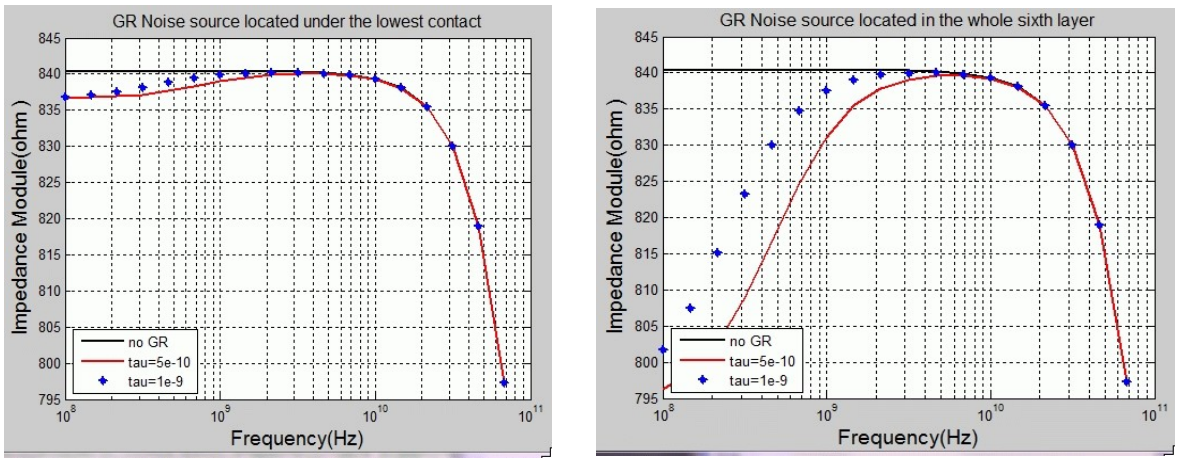
5.5) Substrate noise: towards 3D

The generation-recombination noise (G-R) represents a noise source that is typical and fundamental of a noise in semiconductor materials and related devices, where the carrier concentration can change the order of magnitude a lot. For electron density, fluctuations can happen between two levels: conduction band and donor impurity, or due to defects. Conductivity, associated with GR noise, can be written by relating it to an average carrier lifespan τ:

$$\sigma_{GR} = \frac{\sigma_0}{1+j\omega\tau} \qquad (5\text{-}120)$$

A typical compatible BiCMOS 0,35um process is considered. A specific region (P+/P) is represented. The real profile is modelled by a stack of layers of uniform thickness and uniformly doped.

Let us consider two places where we see this G-R. Modulations of impedance resulting in these GR noises are represented in Figure 119 (a) and (b). Our first results are qualitative, but also seem quantitatively realistic. For instance, we clearly see that in both cases, the influence of the additional GR current, reducing the resistance to low frequencies, before a cutoff frequency of $f_c = 1/(2\pi\tau)$. The impedance, for a lifespan of τ of 1ns, can be reduced by 5% if its reference value, sans GR.



(a) (b)

Figure 119 Introduction of a GR process. (a) defaults under contact C4; (b) defaults in 6th layer

Finally, Figure 120 presents the noise spectral densities of previous two GR cases. For this, we use the impedance transfer paradigm, applied to the multilayer substrate (cf. Figure 60 (b)), using equations like equation (5-102).

It should be possible to study current noise, induced by temperature fluctuations in the volume, with these methods.

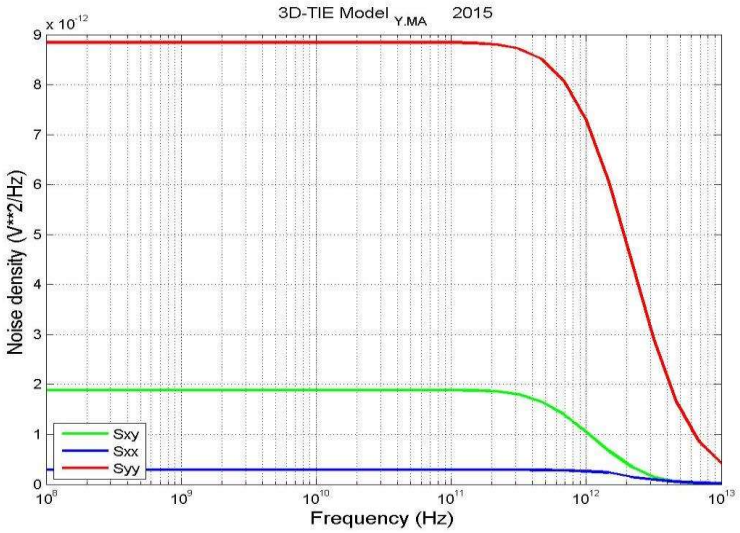


Figure 120 noise spectral densities

5.6) Electrical and thermo-mechanical noise impacts of through-silicon via (TSV) on transistor

From the point of view of electrical aspect, TSV-induced substrate noises that threaten the performance of neighboring transistors due to the parasitic path between TSV and transistor [253]. From the point of thermo-mechanical aspect, owing to the inherent mismatch in coefficient of thermal expansion (CTE) between metal and silicon, thermo-mechanical stress will emerge in the vicinity of TSV, when the system cools down from the possible localized high temperature to the room temperature [254]. The carrier mobility of neighboring transistors would be influenced by the TSVs-inducing thermomechanical stress due to piezo-resistive effect [255], [256], [257]. There are some papers focusing on the electrical impact and thermo-mechanical impact of TSV on transistor [24], [99], [258], [259]. In fact, the transistors in the vicinity of TSV are affected simultaneously by both the coupling noises and thermo-mechanical stress. There has been some reports on the crossing effect of the two aspects. We implement the combination effect of electrical and thermo-mechanical impacts of TSV on the saturation current of transistor by taking NMOSFET for instance [195]–[203]. The study method is also appropriate for PMOSFET. Models of NMOSFET and PMOSFET are calculated from predictive technology model of the site [267].

5.6.1) Investigation method of electrical noise

The saturation current can be impacted by the noise induced by TSV through the body effect. The saturation current I_{dsat} of NMOSFET can be calculated by

$$I_{dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \qquad (5\text{-}121)$$

where V_{GS} represents the voltage difference between gate and source of the NMOSFET; W and L are the width and length of gate, respectively; Cox is the capacitance between gate and carrier channel; μ_n is electron mobility; the threshold voltage V_{th} can be related to the body voltage V_B[261]

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\Phi_F - V_{BS}} + \sqrt{2\Phi_F}\right) \approx V_{th0} - \frac{\gamma}{2\sqrt{2\Phi_F}}V_{BS} \qquad (5\text{-}122)$$

Where V_{th0} is the threshold voltage at zero body voltage; γ represents the body-effect parameter; and $2\Phi_F$ represents the surface-potential parameter. V_{BS} is the body voltage.

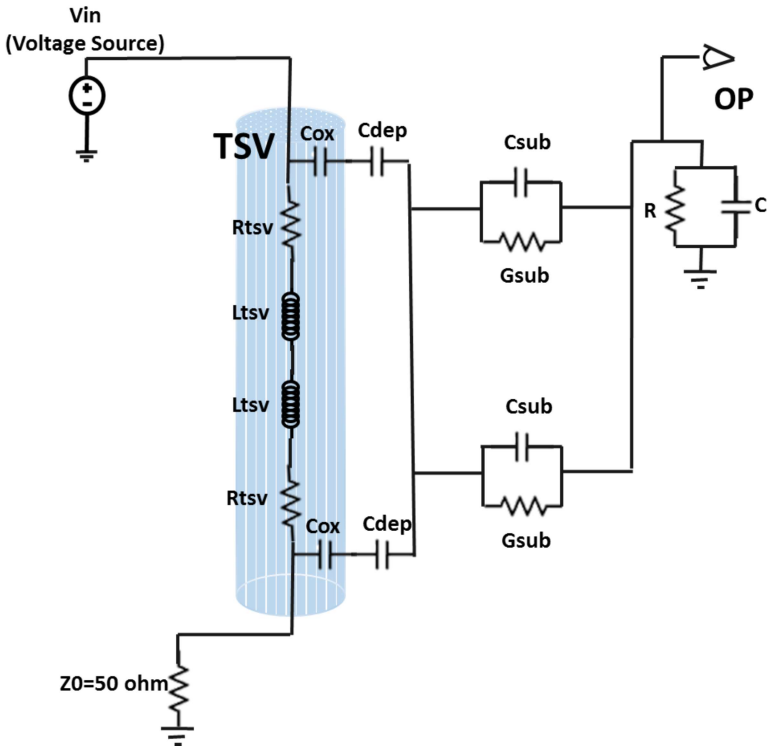


Figure 121 Equivalent circuit model and simulation setup of TSV-to-device noise

By using the previous 2 equations (5-121) and (5-122), the variation of saturation current can be expressed as

$$\Delta I_{sat} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \frac{\gamma}{2\sqrt{2\Phi_F}} V_{BS} \quad (5\text{-}123)$$

$$\frac{\Delta I_{sat}}{I_{sat}} = \frac{\gamma (V_{GS} - V_{th})}{\sqrt{2\Phi_F}(V_{GS} - V_{th})^2} V_{BS} \quad (5\text{-}124)$$

Without the coupling voltage noise, the body voltage would be zero. Therefore, the noise can result in the variation of saturation current.

In order to get the noise body voltage V_{BS}, MNA (modeified nodal analysis) is employed using the equivalent circuit model shown in the previous figure. As said in the second chapter, the TSV resistance Rtsv is calculated by

$$R_{TSV} = \sqrt{\left(\frac{\rho_{TSV} h}{\pi R_m^2}\right)^2 + \left(\frac{h}{\pi \sigma_{TSV} \delta (2R_m - \delta)}\right)^2} \quad (5\text{-}125)$$

Where

$$\delta = \sqrt{\frac{\rho_{TSV}}{\pi \mu_{TSV} f}} \quad (5\text{-}126)$$

δ is the skin depth; f is the frequency; ρ_{TSV}, h, $R_m$and σ_{TSV} are the resistance, height, radius and conductance of TSV; TSV inductance L_{TSV} is expressed as

$$L_{TSV} = \frac{\mu_0 h}{2\pi} \left[\ln\left(\frac{h + \sqrt{h^2 + R_m^2}}{R_m}\right) + R_m - \sqrt{h^2 + R_m^2}\right] \quad (5\text{-}127)$$

The oxide liner capacitance Cox, and MOS effect induced depletion capacitance Cdep are calculated by

$$C_{ox} = \frac{2\pi \varepsilon_{ox} h}{\ln\left(\frac{R_m + t_{ox}}{R_m}\right)} \quad (5\text{-}128)$$

$$C_{dep} = \frac{2\pi \varepsilon_{si} h}{\ln\left(\frac{R_m + t_{ox} + w_{dep}}{R_m + t_{ox}}\right)} \quad (5\text{-}129)$$

$$w_{dep} = \sqrt{\frac{4\varepsilon_{si} kT}{q^2 N_a} \ln\left(\frac{N_a}{n_i}\right)} \quad (5\text{-}130)$$

Where t_{ox} and ε_{ox} are respectively the thickness and permittivity of oxide liner; w_{dep} is the thickness of the depletion layer [93]; k is the Boltzmann's constant; T is the absolute temperature; q is the electronic charge; N_a is the doping concentration of silicon; n_i is the intrinsic carrier concentration.

The silicon substrate capacitance Csub and conductance Gsub can be calculated by [93]

$$C_{sub} = \frac{\pi \varepsilon_{si} h}{\ln(\frac{pitch}{R_m} + \sqrt{(\frac{pitch}{R_m})^2 - 1})} \quad (5\text{-}131)$$

$$G_{sub} = \frac{\sigma_{si}}{\varepsilon_{si}} C_{sub} \quad (5\text{-}132)$$

Where σ_{si} and ε_{si} are the conductivity and permittivity of silicon respectively; $pitch$ is the distance between TSV and transistor.

The time-domain simulation setup method is also given in Figure 121. Here, OP, the observing point, represents the body of transistor. Vin is the input pulse signal of 1 V and 1 Gb/s with rise time of 100 ps. Another end of TSV is terminated by a 50 ohms resistor. The load at OP is a resistance R of 225 ohms representing the on-resistance of an NMOS device in parallel with a capacitance C of 9.6 fF emulating the total capacitance including p-n junction, wire, and gate capacitances [122].

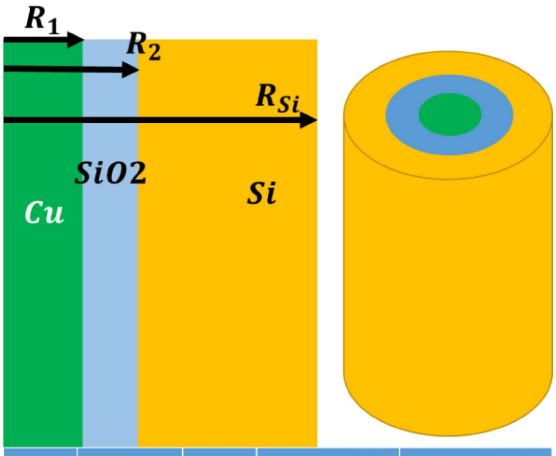
5.6.2) Investigations method of thermo-mechanical noise impact

TSV induced thermo-mechanical stress appears in surrounding silicon substrate due to the mismatch of CTE between TSV metal and silicon, when the structure is subjected to a thermal ramp in the process flow. The saturation current of transistors can be adversely affected by the TSV-induced thermomechanical stress, since the carrier mobility is modified due to piezo-resistive effect.

The work [24] [99] has studied the impacts of thermo-mechanical stress induced by TSV on carrier mobility. Here, we describe simple but enough updated information for the method of estimating thermomechanical impact of TSV. The saturation current change $\Delta I_{sat}/I_{sat}$ can be estimated by [197] [245] [253] [254]

$$\frac{\Delta I_{sat}}{I_{sat}} \approx \frac{\Delta \mu}{\mu}(r,\theta) = \Pi \times \sigma_{rr}^{si}(r) \times \beta(\theta) \quad (5\text{-}133)$$

where σ_{rr}^{si} is the TSV-induced radial stress; μ is the mobility of substrate. $\beta(\theta)$ represents orientation factor; θ is the angle between transistor channel and radial stress induced by TSV. $\theta = 0°$ and $90°$ mean the transistor Drain and Source channels are parallel and perpendicular to TSV-induced radial stress respectively[24]; Π is the piezo-resistive coefficient at $\theta = 0°$, which works as longitudinal stress. For nMOS, $\Pi = -31 \times 10^{-11} Pa^{-1}$, $\beta(0°) = 1$, $\beta(90°) = 0.5$, for pMOS, $\Pi = 71.8 \times 10^{-11} Pa^{-1}, \beta(0°) = 1, \beta(90°) = -0.6$.[23]



	μ(GPa)	ν	α (ppm/K)	Range(um)
Si	51	0.28	2.8	R2<r<Rsi
SiO_2	30	0.16	0.6	R1<r<R2
Cu	26	0.34	18	0<r<R1

Figure 122 Structure and material parameters of TSV filler (Cu), insulating layer (SiO2) and wafer (Si)

The considered linear elastic body in this model consists of TSV filler (Cu, labeled as M), an insulating layer (SiO_2, labeled as I), and a wafer (Si, labeled as W). The Cu filler is in $0 < r < R_1$, SiO2 is in $R_1 < r < R_2$, and Si is in $R_2 < r < R_{si}$. Due to the cylindrical form of TSV, we use the cylindrical coordinates (r, ϕ, z) in the analysis. The related parameters such as the shear modulus μ, Poisson's ratio ν, and the CTE (constant of thermal expansion) α are listed in the Figure 122. The following notations are used: u_i^P is the displacement vector; e_{ij}^P is the elastic strain tensor; σ_{ij}^P is the stress tensor; $P = M, I$ or W; $i, j = r, \varphi, z$. Due to the symmetry, the displacement vector u_i^P can be written as follows [268]

$$u_r^P(r) = u^P(r) + \propto_P (T_2 - T_1)r \quad (5\text{-}134)$$

$$u_z^P(r,z) = \frac{z}{h} w^P(r) + \propto_P (T_2 - T_1)z \quad (5\text{-}135)$$

$$u_\varphi^P(r) = 0 \quad (5\text{-}136)$$

where $r = 0.5 * D$ (D is the wafer thickness), and $u^P(r)$ and $w^P(r)$ are functions to be solved. The nonzero components of the elastic strain tensor e_{ij}^P are determined as follows:

$$e_{rr}^P = \frac{du^P}{dr}, e_{\varphi\varphi}^P = \frac{u^P}{r}, e_{zz}^P = \frac{w^P}{h}, e_{rz}^P = \frac{z}{2h}\frac{dw^P}{dr} \quad (5\text{-}137)$$

The stresses σ_{rr}^P are related with the elastic strains e_{ij}^P by Hooke's law

$$\sigma_{ij}^{P} = 2\lambda_P e_{ij}^{P} + \lambda_P (e_{rr}^{P} + e_{\varphi\varphi}^{P} + e_{zz}^{P})\delta_{ij} \quad (5\text{-}138)$$

Where $\lambda_P = 2\mu_P \upsilon_P (1 - 2\upsilon_P)^{-1}$ and δ_{ij} is the Kronecker delta. Based on the average over the wafer thickness, $u^P(r)$ and $w^P(r)$ are shown as follows: [268]

$$u^P(r) = a_P r + \frac{b_P}{r} + c_P I_1\left(\sqrt{A_P} r\right) - d_P K_1(\sqrt{A_P} r) \quad (5\text{-}139)$$

$$w^P(r) = -\frac{2\lambda_P h}{\lambda_P + 2\mu_P} a_P - \frac{(\lambda_P + 2\mu_P)h}{\lambda_P}\sqrt{A_P} \times [c_P I_0\left(\sqrt{A_P} r\right) + d_P K_0(\sqrt{A_P} r)] \quad (5\text{-}140)$$

Where I_l and K_l with $l = 0,1$, are the l^{th}-order modified Bessel functions of the first kind and the second kind, respectively; $A_P = 12(\mu_P + \lambda_P)(\lambda_P + 2\mu_P)^{-1} h^{-2}$; and a_P, b_P, c_P, d_P are 12 constants to determine the solution of the problem. For the infinite wafer ($R_{si} \gg R_2$), due to the boundedness of the elastic parts of the displacements u_r^W and u_z^W at infinity, a_W and c_W should be zero. Displacement u_r^M is zero at via center; b_V and d_V should be zero. The remaining eight constants are determined from the boundary conditions for the continuity of the displacements and stresses at interfaces r = R_1 and r = R_2 as follows: [268]

$$u_r^M(R_1) = u_r^I(R_1), u_Z^M(R_1) = u_r^I(R_1), \sigma_{rr}^M(R_1) = \sigma_{rr}^I(R_1), \sigma_{rz}^M(R_1) = \sigma_{rz}^I(R_1)$$
$$u_r^I(R_2) = u_r^W(R_2), u_z^I(R_2) = u_z^W(R_2), \sigma_{rr}^M(R_2) = \sigma_{rr}^W(R_2), \sigma_{rz}^I(R_2) = \sigma_{rz}^W(R_2)$$

Using the expression of u_r^P and u_z^P, σ_{rr}^P and σ_{rz}^P can expressed in terms of unknown 12 constants. With the previous relationships, one can solve the unknown 12 constants: a_P, b_P, c_P, d_P of the linear algebra system.

The solution for σ_{rr}^P, σ_{rz}^P, e_{rr}^P, $e_{\varphi\varphi}^P$ are [268]

$$\sigma_{rr}^P = 2\mu_P \frac{3\lambda_P + 2\mu_P}{\lambda_P + 2\mu_P} a_P - 2\mu_P \frac{b_P}{r^2} - 2\mu_P I_1\left(\sqrt{A_P} r\right)\frac{c_P}{r} + 2\mu_P K_1\left(\sqrt{A_P} r\right)\frac{d_P}{r} \quad (5\text{-}141)$$

$$\sigma_{rz}^P = -12\mu_P \frac{z}{h^2}\frac{\lambda_P + \mu_P}{\lambda_P} \times [I_1\left(\sqrt{A_P} r\right)c_P - K_1\left(\sqrt{A_P} r\right)d_P] \quad (5\text{-}142)$$

$$e_{rr}^P = a_P - \frac{b_P}{r^2} + \left[\sqrt{A_P} I_0\left(\sqrt{A_P} r\right) - I_1\left(\sqrt{A_P} r\right)\frac{1}{r}\right] c_P + \left[\sqrt{A_P} K_0\left(\sqrt{A_P} r\right) + K_1\left(\sqrt{A_P} r\right)\frac{1}{r}\right] d_P \quad (5\text{-}143)$$

$$e_{\varphi\varphi}^P = a_P + \frac{b_P}{r^2} + I_1\left(\sqrt{A_P} r\right)\frac{1}{r} c_P - K_1\left(\sqrt{A_P} r\right)\frac{1}{r} d_P \quad (5\text{-}144)$$

5.7) Results and discussion

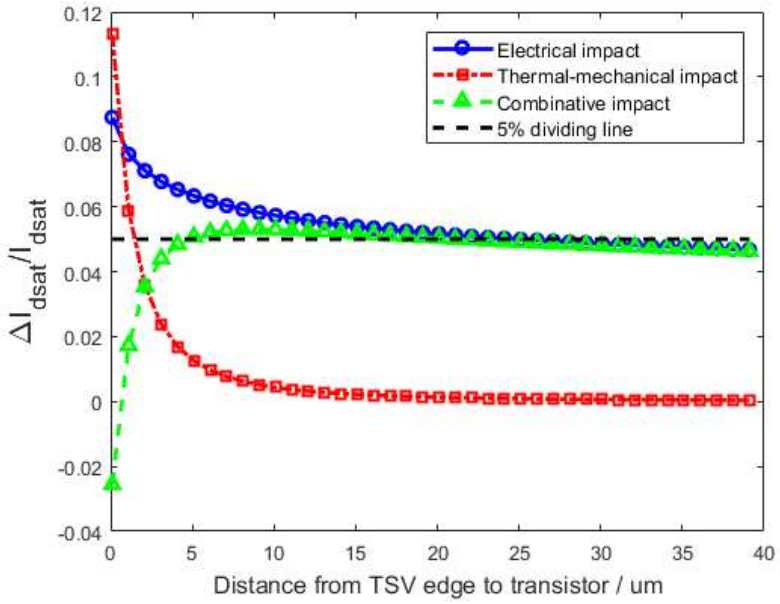
Based on the study method in the previous two sections, the relative changes of saturation current caused by the coupling noise, thermo-mechanical stress, and combination of the two aspects can be obtained, as shown in following Figure 123(a). According to the current technology, the parameters used in this simulation are selected as follows. The height and radius of TSV are 50um and 2.5um, respectively; the thickness of oxide liner around TSV is 0.1um; the conductivity of TSV is 5.8e7 S/m. The oxide liner and silicon have relative permittivity 3.9 and 11.9, respectively. The conductivity and doping concentration of the p-type silicon substrate is 10 S/m and 1.25e15 cm^{-3}, respectively. Here a 22nm nMOS is used. According to the predictive technology model

[269], the body doping concentration at the depletion region boundary between the channel and the body in a 22-nm technology node is 5.5e18 cm^{-3}, the thickness of gate oxide is 1.1nm, the environment temperature is fixed to 300K. The body effect γ and surface potential $2\phi_F$ can be expressed by: [269]

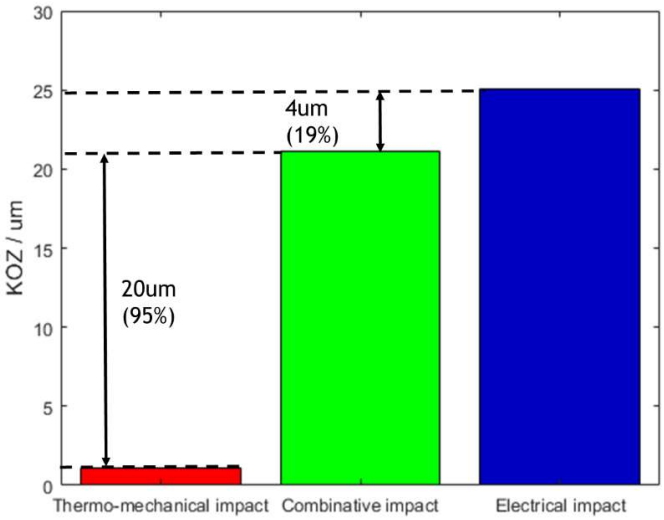
$$\gamma = \frac{tox\_nmos}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}Nsub} \quad (5\text{-}145)$$

$$2\phi_F = \frac{2kT_0}{q}log(\frac{Nsub}{ni}) \quad (5\text{-}146)$$

Because the piezo-resistive coefficient is negative for NMOS, the thermo-mechanical stress leads to a decrease of the saturation current. While the coupling noise has an opposite impact on the variation of saturation current. Therefore, the two aspects are counteracted each other to a certain extent. In order to compare the two impacts clearly, Figure 123(a) gives the absolute value of the thermo-mechanical impact on saturation current. It is shown in Figure 123(a) that, as the distance between TSV edge and transistor is smaller than 5um, the thermo-mechanical stress plays a major role in the variation of saturation current. As the distance is larger than 5um, the electrical coupling noise is major.



(a)



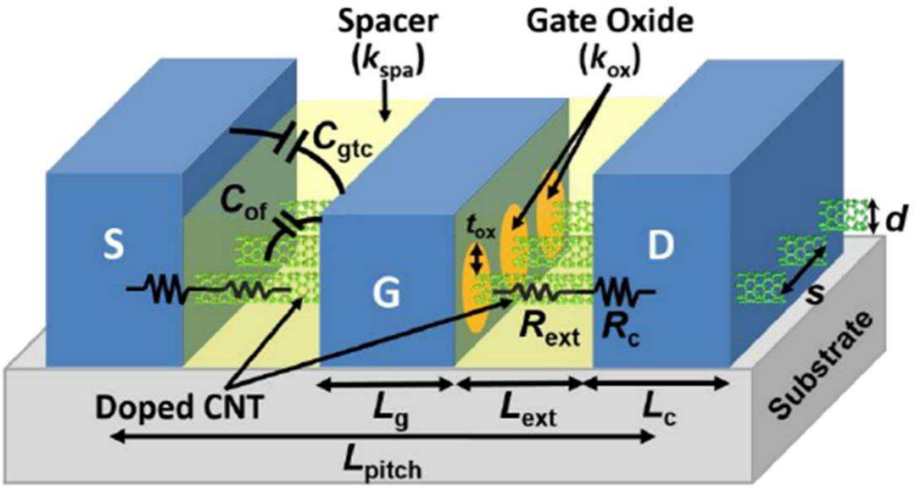
(b)

Figure 123 (a) Variation of saturation current with distance from TSV edge to transistor and (b) KOZ results caused by the coupling noise, thermo-mechanical stress, and combination of the two aspects.

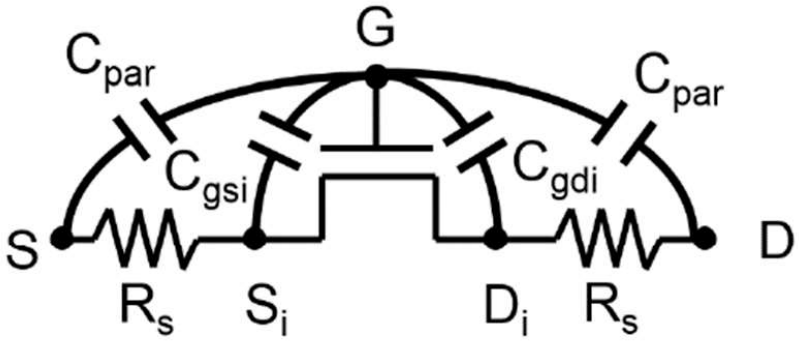
The Keep-out zone (KOZ) [255], [256], [270] is defined as the region with a change of saturation current over 5% [99], [191], [196], [202]–[205], meaning the region where devices cannot be made, since transistor performance is adversely affect. The KOZ results are summarized in Figure 123(b). It is shown that, KOZ is 25um and 1um for individual electrical impact and thermo-mechanical impact, respectively. Nevertheless, KOZ should be 21um considering the combination impact of the two aspects. The error reaches more than 50% if only individual electrical impact or thermo-mechanical impact is considered. Therefore, it is necessary to take both electrical and thermo-mechanical impacts into consideration for KOZ evaluation.

In this section, the research method is used for the typical situation, and it can also be applied to other conditions, such as, PMOSFET (and then CMOS imagers[60], [126], [157]), FinFETs, other parameters of NMOS, TSV and even CNFET (Carbon Nanotube FET, University Stanford [274]). But in compare with the CMOS components, TSV has slightly influence to CNFET.

A representative CNFET structure is shown in Figure 124(a): a cylindrical gate-all-around structure with heavily doped source/drain extensions. Throughout this part, Vgs(i) and Vds(i) denote the voltages across the gate to the (internal) source and the (internal) drain, respectively, as shown in the corresponding transistor schematic in Figure 124(b). P-type CNFETs are completely symmetric with n-type CNFETs, i.e. characteristics of I-V and C-V are the same for p-CNFETs and n-CNFETs given the same |Vgs| and |Vds|, due to the symmetry of CNT's conduction band and valance band.



(a)



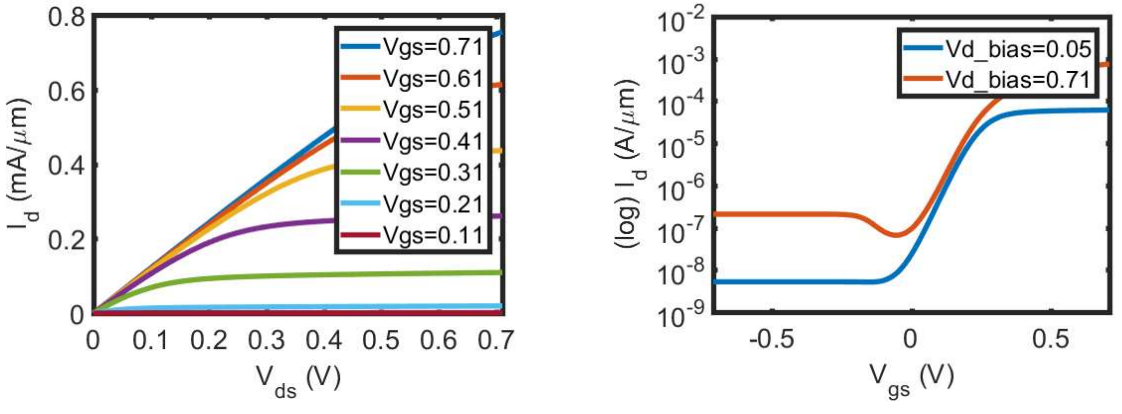
(b)

Figure 124 (a) 3D schematic of vs-CNFET (b) equivalent circuit

Table 18 Input parameters of vs-CNFET of Stanford University[275]

Name	**Value**	**Description**
Lg	11.7nm	Physical gate length
Lc	12.9nm	Contact length
Lext	3.2nm	Source/drain extension length
W	1um	Transistor width
tox	3nm	Gate oxide thickness
kox	23	Gate oxide relative dielectric constant
geo	1	Device geometry 1:cylindrical gate-all-around; 2:top-gate with charge screening effect 3:top-gate without charge screening effect
Hg	20nm	Gate height

kspa	7.5	Source/Drain spacer relative dielectric constant
dcnt	1.2nm	CNT diameter
cspa	10nm	Center-center distance between the adjacent CNTs
Efsd	0.258eV	Fermi-level at the source/drain minus to the Ec determined by the doping density
Vfb	0.015V	Flat-band voltage



(a) (b)

Figure 125 I-V curve of vs-CNFET (a) Id-Vds curve by changing Vgs (b) Id-Vgs curve by change Vd_bias

As shown in Figure 125, Id increases as Vgs becomes small due to the increase in inter-band direct source-to-drain tunneling current.

The KOZ noise consideration method can also be taken into account in the vs-CNFET model, but because that the CNTs sit on a thick insulator (e.g. SiO_2), so the body terminal is assumed to have no effects. So the TSV electrical parasitic has no influence to the Idsat of vs-CNFET, and the piezo-resistive effect has a great influence to the carrier mobility μ, as shown in the electro-mechanical part, which is directly related with the thermo-mechanical noise.

In order to have the same relationship:

$$\frac{\Delta I_{sat}}{I_{sat}} \approx \frac{\Delta \mu}{\mu} \tag{5-147}$$

we fix Vgs to 0.41V and Vd_bias to 0.71V, in this condition, the Id stays in saturation. We change the μ and get the following figure:

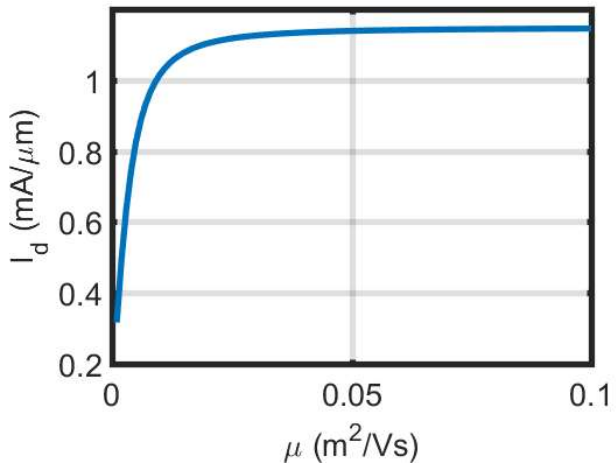


Figure 126 μ-Idsat curve

As we can see here, when the μ is below $200cm^2/Vs$, the Idsat change linearly with μ, but when μ gets higher, it has nearly no influence to Idsat. So that's to say, when the carrier mobility is below $200cm^2/Vs$, we will have the relationship of equation (5-147)

But the carrier is found in the CNTs, which are isolated from substrate by a layer of oxide. So one more time, the CNFET is isolated from the thermo-mechanical noise. That's to say that, even we put TSV very close to CNFET, it has no electrical and thermos-mechanical noises to the saturation current.

TSV has two aspects of impact on the saturation current of transistor. On one hand, TSV induces coupling noise to surrounding transistors due to current pathway composed by the parasitic parameters of the structure. On the other hand, TSV induces thermo-mechanical stress owing to the thermal ramp in the process flow. We don't limit to the CNFET, in this later part, we deal with a simple NMOS example, which is part of the CMOS imager of the final demonstrator, by taking NMOSFET for instance, the electrical impact of TSV on the saturation current of transistor is studied based on the equivalent circuit model, and the thermo-mechanical impact is analyzed based on the piezo-resistive effect. Then the combinative impact of the two aspects is investigated. It is shown that, the coupling noise and thermo-mechanical stress have opposite impacts on the variation of saturation current. KOZ has an error of more than 50% if only one aspect is considered. The study method is also appropriate for PMOSFET and other situations.

5.8) Conclusion

Modeling in 3D noise, even 2D, is, for the most part, a failure due to physical modeling problems: for example, discerning the hole and electron contribution to noise in devices. Master equations, like the Boltzmann equation, associated with second order instances, should be developed more for theoretical study of noise.

For submicronic devices, new effects, like non-stationary electro-thermal phenomena, crop up. By reducing the length of a device to some mean free paths, each carrier undergoes very few collisions on its path from one electrode to another. Another example is correlation of noise sources in space, which, are not independent, even though autonomous. Moreover, intensities of noise can increase during voltage ramp applied to a circuit. Other investigations must be made, in the case of the following points:

- Quantum phenomena: duration of carrier collisions versus energy exchange with phonons.
- Proposing rigorous techniques or methods of noise reduction, although it is subtler than it seems in this ambiguous domain.

The program, to be developed in the future, could focus on the following main areas:

- Continuing basic studies on microscopic behavior of noise sources up to 3D, with theories and experiments, in order to have a better understanding of phenomena.

In this configuration, connecters (especially TSVs), substrate and devices are deeply entangled. Study submicronic, nano-metric transistors, used for high speed logic in information technology. The objective is to study, for instance, the 1/f noise and the RTS (Random Telegraphic Signal) noise, in order to better understand ultimate (Bi-)CMOS, and develop compact electric models of device noise to correctly and fully simulate the behavior of these devices and the related circuits.

High speed III-V transistors (HEMT and HBT), as important elements of future high-frequency broadband telecommunication systems. Low frequency analyses (1/f and RTS noise) and high frequency noise (G-R) will be conducted on semiconductor devices and material (bulk, epitaxial layers, and flexible electronics).

Noise in photoelectric detectors and lasers, particularly in multi-quantum well structures, for high speed, optoelectronics and gigabit communications.

Sensors, in particular those using magnetic effects.

Chapter 6: General Conclusion

This thesis provides a global design method for the conception of 3D integrated circuit in electrical, thermal, electro-thermal and also noise field. Hereafter will be included simulation methods for single TSV, TSV matrix, multi-layers substrate, multi-processors and heat dissipation design.

We firstly present some background knowledge on electrical parasitic effects (for instance, MOS effect and Skin current) of TSV. Based on the parasitic effects, two EDA design tools, a substrate extractor and a 3D TLE extractor (3D transmission line extractor), are programmed, which can automatically extract from any contacts (embedded or not): impedance, of arbitrary shape and arbitrary material. The extractors are 100% compatible with SPICE core simulator, like ADS (Advanced design system, dedicated to RF). The extracted data are often verified with measurements and finite element method (FEM) simulation result for Micro-stripe model, 2xTSVs U model. Based on the parasitic effects of TSV, a 26GHz frequency and 2GHz bandwidth RF filter is proposed in this work.

The chapter 3 presents the thermal and electro-thermal modeling method. We propose an analytical thermal solution for multi-layers substrate nonstationary temperature distribution. In the 3D IC design, the thermal issues are crippling issues, especially when we scale down to nanoscale. The electrical resistance increase with temperature, likewise the substrate resistance. Most of thermal simulation works are based on the steady regimes; few people work on the non-stationary case. Non-stationary effects are crippling, like hot spots, which can be enhanced by voltage ramps. We combine 1D thermal compact model by using MNA (modified nodal analysis) and 2D finite volume method (FVM) to solve multi-layers 3D IC temperature calculation, which, comparing with 3D FEM simulation, reduces largely the calculation complexities. This method is suitable for any 3D IC. Besides, a 4 cores processors heat dissipation case is studied in this chapter. The later part of this chapter presents how the electro-thermal simulation works. The electro-thermal simulator can be 100% compatible with SPICE (-like) simulator, and the electrical part is verified with ADS. The MNA method is normally used for 3D PDN (power distribution network) VLSI design; but here, we apply it in the device level simulation. This point is somewhat original, up to our knowledge. This work constructs the electro-thermal analysis framework for substrate, thermal connections (3D via) and system level 3D PDN. We provide an extensive study of power and thermal dissipation issues in 3D integration considering several aspects such as:

- Single and multi-layer auto-heating effects on 3D power and thermal dissipation;
- TSVs and substrate impact on power and thermal integrity and their design implications;
- heat sink’s thermal conductivity’s influence on the electro-thermal effects.

We combine switching frequency and electro-thermal effects together. And, by comparing with S parameters, we found out that the electro-thermal effects appear only when S parameters change dramatically, and the reduction of thermal resistance and the increase of doping concentration of substrate will restrain the electro-thermal signal integrity problem.

The chapter 4 presents the flat heat pipe simulation. As a solution to the local heat dissipation, the passive heat dissipation component, flat heat pipe (FHP) is proposed as a prospective component in the chapter 4. The FEM based model (COMSOL Multiphysics) is very accurate in the 2D and 3D simulation of heat pipe. Precise boundary conditions can be found in this chapter; it considers the pressure field in the calculation, and especially it can extract the capillary pressure directly from the model, which will be very useful in the future study of wick layer's capillary effects. And an extensive study of the working performance limiting condition has been presented in this part.

The chapter 5 firstly proposes the analytical solution for the substrates non-stationary noise distribution and presents some noise analysis methods. And this chapter investigates also the keep-out-of-zone (KOZ) of TSV to transistor, like nMOS and CNFET. The investigation methods of electrical noise impact and thermo-mechanical noise impact show large influence to nMOS like device (pMOS, pFET and nFET). But for CNFET, due to the highly isolation between carbon nano-tube and substrate, the parasitic effect of TSV has no influence to it.

To conclude, this work can, in addition to realizing the electrical, thermal and electro-thermal modeling of single TSV, TSV matrix and multi-layers 3D IC, clarify the features constrains and coupling noise processes involved in multi-layers substrate, and also give the EDA design tools. But much remains to be done, a complex real case should be studied. (cf. CMOS imager, NMR system, etc.)

Extension of this work will concern a M3D (3D Monolithic) electro-thermal modeling, which can directly realize nanoscale device level design (a CMOS inverter can be obtained in nanoscale by connection of a pMOS and nMOS with a M3D). And more RF devices can be generated by using TSV or M3D technology in micro and nano scale; for example, micro RF antenna with TSV, TSVs based thermal coupler, TSV or M3D based logic cell, and other 3D sensors.

Recently the research of 3D IC has extended to optic-electrical design. So one of the future research interest will be the EDA co-design of optic-electronic. But this will be kind of useless, because that in the optical application, the substrate and transmission medium are always glasses, and in this case, the parasitic effects are always negligible, in micro scale. But due to the high speed transmission signal, the optical circuits can be easily overheated. So the optic-electrical-thermal co-design will be one important and interesting work in the future.

One of the hot subject in the research is the neuromorphic chip. Brain-inspired, spike-based computation in electronic systems is being investigated for developing alternative, non-conventional computing technologies. The AI (Artificial Intelligence) chip, which is the best way

to integrate learning algorithm with hardware design. The Neural Engineering Framework provides a method for programming these devices to implement computation. [276] The most interesting part for 3D IC design is that, if we can implement a mixed signal analog/digital neuromorphic multi-neuron VLSI chip into a 3D chip and imitate the brain structure, we will have a better understanding of human's learning system.

Appendix A: Extraction of the CPW propagation parameters

S-parameters extracted from a CPW through a vector network analyzer (VNA):

$$[S]=\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

S-parameters can be converted from Y-parameters by the following relationship:

$$S_{11}=\frac{(1+Z_0*Y_{22})*(1-Z_0*Y_{11})-Z_0^2*Y_{12}Y_{21}}{\Delta Y}$$

$$S_{12}=\frac{2*Z_0^2*Y_{12}Y_{22}}{\Delta Y}$$

$$S_{21}=\frac{2*Z_0^2*Y_{21}Y_{11}}{\Delta Y}$$

$$S_{22}=\frac{(1+Z_0*Y_{11})*(1-Z_0*Y_{22})-Z_0^2*Y_{12}Y_{21}}{\Delta Y}$$

$$\Delta Y=(1+Z_0*Y_{11})*(1+Z_0*Y_{22})-Z_0^2*Y_{12}Y_{21}$$

Where: $Z_0 = 50\ \Omega$ being the input and output impedance controlled by the VNA

S-parameters are next converted to $[ABCD]$ parameters [2] through the relations below:

$$A=\frac{1+S_{11}-S_{22}-\Delta S}{2*S_{21}}$$

$$B=\frac{1+S_{11}+S_{22}+\Delta S}{2*S_{21}}*Z_0$$

$$C=\frac{1-S_{11}-S_{22}+\Delta S}{2*S_{21}*Z_0}$$

$$D=\frac{1-S_{11}+S_{22}-\Delta S}{2*S_{21}}$$

$$A = \frac{(1+S_{11})*(1-S_{22})+S_{12}S_{21}}{2*S_{21}}$$

$$B = \frac{(1+S_{11})*(1+S_{22})-S_{12}S_{21}}{2*S_{21}} * Z_0$$

$$C = \frac{(1-S_{11})*(1-S_{22})-S_{12}S_{21}}{2*S_{21}*Z_0}$$

$$D = \frac{(1-S_{11})*(1+S_{22})+S_{12}S_{21}}{2*S_{21}}$$

Where: $Z_0 = 50\ \Omega$ being the input and output impedance controlled by the VNA

$\Delta S = S_{11} * S_{22} - S_{21} S_{12}$ is the determinant of the S-matrix

The relation between ABCD-parameters and CPW propagation parameters is:

$$ABCD_{CPW} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_C \sinh(\gamma l) \\ \sinh(\gamma l)/Z_C & \cosh(\gamma l) \end{bmatrix}$$

Where l is the length of CPW

The characteristic impedance is:

$$Z_C = \sqrt{\frac{B}{C}}$$

The propagation constant is:

$$\gamma = \frac{1}{l} * \cosh^{-1} A$$

Other parameters can also be calculated:

The phase constant

$$\beta = \mathrm{Im}(\gamma)$$

The line loss

$$\alpha = \mathrm{Re}(\gamma)$$

The line resistance of telegraph equations:

$$R_l = \mathrm{Re}(\gamma * Z_C)$$

The line inductance of telegraph equations:

$$L_l = \mathrm{Im}(\gamma * Z_C)/\omega$$

The shunt resistance of telegraph equations:

$$G_s = \mathrm{Re}(\gamma / Z_C)$$

The shunt capacitance of telegraph equations:

$$C_s = \mathrm{Im}(\gamma / Z_C)/\omega$$

With the new impedance characteristic Zc, we can recalculate the Y parameters by S parameters.

$$S_{11} = \frac{(1-S_{11})*(1+S_{22}) + S_{12}S_{21}}{\Delta S}$$

$$S_{12} = \frac{-2 * S_{12}}{\Delta Y}$$

$$S_{21} = \frac{-2 * S_{21}}{\Delta Y}$$

$$S_{22} = \frac{(1+S_{11})*(1-S_{22}) + S_{12}S_{21}}{\Delta Y}$$

$$\Delta S = Z_C\left((1+S_{11})*(1+S_{22}) - S_{12}S_{21}\right)$$

And then; we can recalculate the S parameter by using the formula above and the impedance of reference: 50 ohm.

Appendix B: Résumé en français

B.1) Introduction

AI (Intelligence Artificielle) est un nouveau domaine d'application passionnant qui peut bénéficier du passage aux puces 3D. Le produit Jeopardy d'IBM Watson et Google AlphaGo ont gagné le meilleur joueur de Go humain, mais tous deux ont fonctionné sur des grappes de serveurs, qui sont trop volumineuses pour être largement utilisées. Les voitures autonomes d'aujourd'hui utilisent des processeurs plus modestes, mais les voitures ne sont pas nécessairement sûres. Pour les rendre plus sûres, il faudra des systèmes de contrôle plus sophistiqués susceptibles d'augmenter les exigences de calcul.

Comme nous le savons depuis le "von Neumann bottleneck", le MPU (unité de microprocesseur) et la mémoire sont séparées et les données se déplacent entre les deux. Dans ce cas, la latence est inévitable. Au cours de ces années, les fréquences des processeurs ont largement augmenté et atteint environ 4,2 GHz. Mais la mémoire s'améliore dans la densité, c'est-à-dire que la mémoire peut stocker plus de données dans un espace fixe, mais pas dans l'augmentation des vitesses de transfert. Lorsque la fréquence du travail de MPU augmente, le processeur passe de plus en plus de temps d'attente pour écrire et lire depuis la mémoire. Donc, peu importe la rapidité avec laquelle le MPU peut fonctionner; il est limité par la vitesse de transfert de la mémoire. [1], [2]

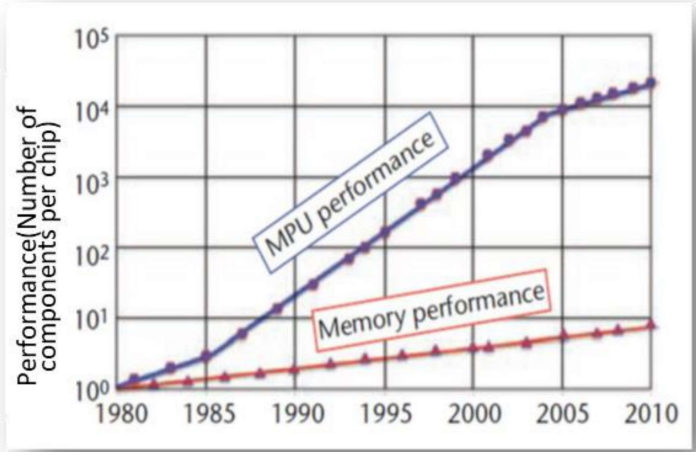


Figure B1 Écart de performance (vitesse) entre MPU et mémoire augmentant avec le temps, unité : nombre de transistors per cm^2 [3]

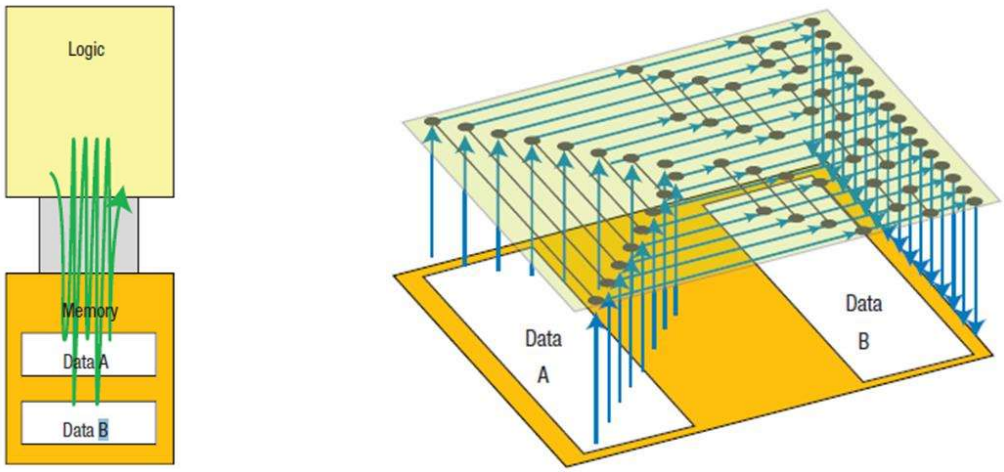
Ainsi, la nouvelle génération d'architectures AI (Intelligence Artificielle) fait émerger le besoin d'un processeur et d'une mémoire plus étroitement intégrés. Par exemple, la mémoire occupe une

très grande place dans la puce de réseau neuronal TrueNorth d'IBM, Google TensorFlow et les nouvelles versions des GPUs utilisés dans les voitures autonomes ont de très larges mémoires DDR5.

B.2) De 2D IC à 3D IC

Comme l'illustre la Figure B2 a, un système informatique traditionnel de von Neumann est en fait l'intégration hétérogène de puces logiques MPU (jaune), de puces de mémoire (orange) et d'interconnexions de puce à puce (grise). Par exemple, ici, la donnée A enregistre les données de l'électronique RF, la donnée B enregistre les données des capteurs de la caméra, le processus DRAM a une densité de mémoire 10 fois plus élevée que le processus logique de la même génération. Le cache dans l'unité MPU est donc trop petit pour l'implémentation de la mémoire, et les données doivent inévitablement être déplacées à travers l'interface à haute énergie entre la logique et la mémoire, deux fois par répétition (comme le montre la ligne verte).

La Figure B2 b montre le diagramme de dépendance de données équivalent pour une étape de fusion d'un tri binaire d'arborescence. La couche logique jaune en haut montre la fusion de quatre étapes de tri bitonique. Lors de l'application de la structure sur la Figure B2 b, les comparaisons et les échanges peuvent être disposés sur la surface de la couche logique. Les données à traiter (Données A) et un emplacement pour stocker le résultat (Données B) sont placés dans la mémoire orange immédiatement inférieure et connectés via des fils courts traversant la grande surface 2D, plutôt qu'un bord.



(a) (b)

Figure B2 Avantage de la 3D pour les interconnexions. (a) Les systèmes 2D comprennent des puces de logique et de mémoire, la courbe verte illustrant un calcul de mémoire logique mixte inefficace justement à cause de cette logique et du partitionnement de la mémoire. (b) Les systèmes 3D avec un couplage étroit entre la logique et la mémoire évitent les chemins de latence élevés, les goulots d'étranglement de la bande passante et la conversion des

signaux en niveaux d'énergie élevés pour les interconnexions hors puce. La courbe bleue montre une étape représentative du mouvement des données dans le tri.

Pour la structure 3D de la Figure B2 b, les données peuvent être lues en une seule fois à partir de la mémoire physiquement colocalisée, et comparées et échangées en matériel et en parallèle. En revanche, un ordinateur von Neumann aurait besoin de déplacer toutes les données de la mémoire vers le processeur de manière séquentielle, ainsi, le goulot d'étranglement devient un problème principal lors du traitement des grands graphiques de données et d'autres noyaux de bas niveau dans l'IA. Les circuits 3D ont donc un meilleur avantage.

La loi de Moore semble s'essoufler. Les défis techniques de la mise à l'échelle à mesure que nous atteignons les limites de la physique sont difficiles, ce qui ralentit le rythme et augmente le coût de la mise à l'échelle. En outre, les avantages de la mise à l'échelle sont réduits car elle n'est pas adaptée aux avantages de performances historiques. L'effort pour continuer le rythme de progrès pour l'industrie des semi-conducteurs a été concentré sur deux directions techniques; La diversification fonctionnelle du circuit, qui est appelée «plus que Moore», est la première technique. On intègre des modules de fonctionalités différentes dans un package. C'est le moteur de l'architecture System-In-Package (SiP). La deuxième est 3D IC, comme montre dans la Figure B3. Cela permet d'augmenter la densité fonctionnelle pour un nœud donné et améliore également les performances et réduit les besoins en énergie. Il existe plusieurs forces motrices pour l'intégration 3D. Les avantages potentiels comprennent des performances plus élevées, une consommation d'énergie réduite, une latence réduite, une taille plus petite et, finalement, un coût inférieur à celui des emballages 2D 2.5D et conventionnels. Certaines des forces motrices de base pour l'intégration 3D sont présentées dans la Figure B4 ci-dessous. [4]

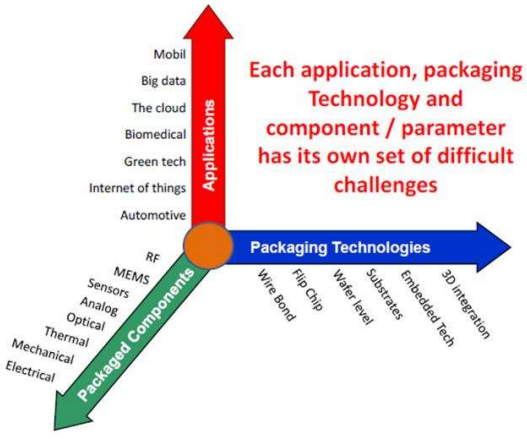


Figure B3 Eléments incorporés dans des packages SiP complexes *via* une intégration hétérogène

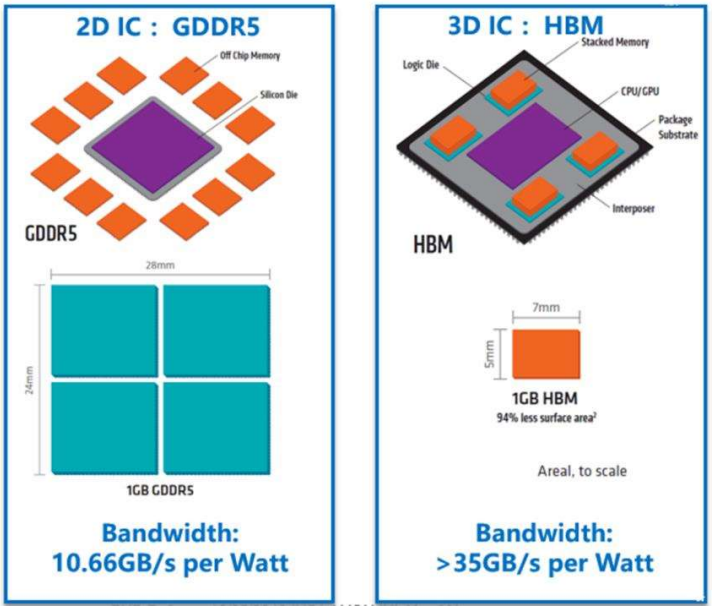


Figure B4 Forces motrices pour l'intégration 3D [4]

La combinaison des idées 3D IC conduit à un nouveau chemin d'échelle potentiel. L'interface entre la logique et la mémoire a restreint les systèmes pendant des décennies. La réduction de ce goulot Von Neumann pourrait permettre aux semi-conducteurs de continuer à améliorer les performances du système. Cependant, cela nécessitera des progrès (comme le montrent la Figure B4 et la Figure B5) dont les processus d'ingénierie prendront du temps. Mais chaque avance réduira un peu l'impact du goulot Von Neumann. Pour les applications qui bénéficieraient d'une intégration plus étroite, cela pourrait offrir une augmentation des performances de génération en génération.

B.3) Feuille de route pour les circuits intégré3D

Les dimensions horizontales atteindront le point où aucune réduction horizontale ne sera possible; les prédicteurs de la mort de la loi de Moore s'expriment, mais le développement des transistors verticaux et l'intégration des couches de transistors verticaux sont déjà complets. Le problème aujourd'hui est que on continue à augmenter la densité de transistors par cm^2 à la même vitesse ou à un rythme plus rapide que la loi de Moore à l'avenir.

La feuille de route IRDS 2017 (Feuille de route internationale pour le développement et le système) projette la technologie des circuits intégrés de pointe pour chaque année pour les 15 prochaines années. La Figure B5 en offre un aperçu [2]. Comme vous pouvez le voir, une échelle de densité 2D efficace selon la loi de Moore est prédite jusqu'au milieu des années 2020, après quoi les avancées viendront de la densité 2D multipliée par le nombre de couches ou la projection de la densité 3D sur une surface 2D. Cette mise à l'échelle réduira les coûts d'achat et de consommation d'énergie et fournira des avantages au niveau du système. [7] Cette évolution démontre que le point ultime de la mise à l'échelle est le 3D VLSI qui offre la possibilité d'empiler des dispositifs

permettant des contacts haute densité au niveau de VLSI du système (jusqu'à 100 millions de vias par millimètre carré), comme le montre le tableau 1. L'emballage 3D est disponible depuis des décennies sous des formes primitives, avec des connexions, des performances et une efficacité énergétique croissantes à mesure que la technologie progresse. La 3D entièrement intégrée devrait être disponible en moins d'une décennie.

Table 1 Evolution des options d'intégration 3D vers 3D VLSI [1]

Options	Links	Bandwidth	Latency	Power	Time frame
Wire-bond stack	100s	Low	High	High	Available for 30 years
Through silicon via (TSV) or microbump stack	1,000s	Medium	Medium	Medium	Available for 10 years
3D VLSI stack	100,000s	High	Low	Low	<10years

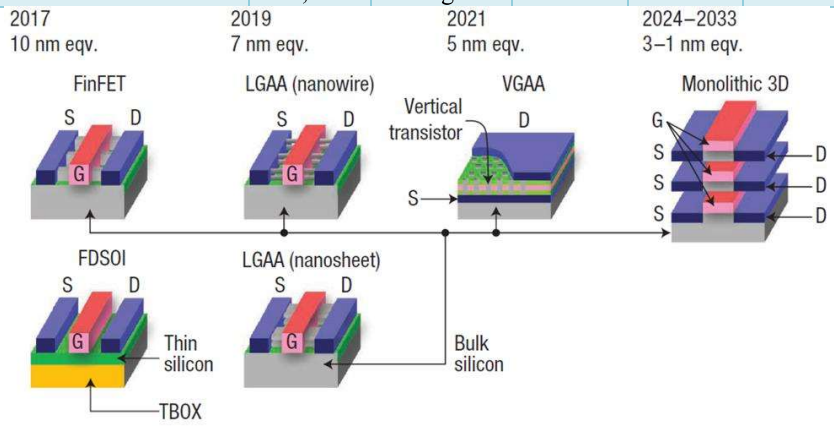


Figure B5 Aperçu des prévisions de la Feuille de route internationale pour les dispositifs et les systèmes 2017 pour les futures structures 3D. D: drainer; FDSOI: silicium sur isolant entièrement appauvri; G: grille; LGAA: grille latérale tout autour; S: source; TBOX: oxyde mince enterré; VGAA: grille vertical tout autour[2]

Dans les années 1970, deux lois fondamentales sont devenues les pierres angulaires de toute l'industrie: les lois d'échelle de Moore et Dennard. La loi d'échelle de Dennard a identifié comment améliorer les performances des transistors au moyen d'une méthodologie appelée mise à l'échelle géométrique. Au début de la décennie précédente, la mise à l'échelle physique (limite d'épaisseur d'oxyde de grille) s'est arrêtée et l'avènement du nouveau transistor en réduisant les dimensions horizontales et en introduisant de nouveaux matériaux et de nouveaux effets physiques continue la loi Dennard. Les structures verticales commencent à remplacer le transistor planaire. La date de révolution prédictive est 2021. A ce moment, le dispositif construit par l'échelle 2D atteindra une limite fondamentale de l'espace de fabrication 2D, la transition vers des structures de dispositifs verticales complètes, une intégration hétérogène et une consommation électrique réduite deviennent les moteurs technologiques. [2], [3]

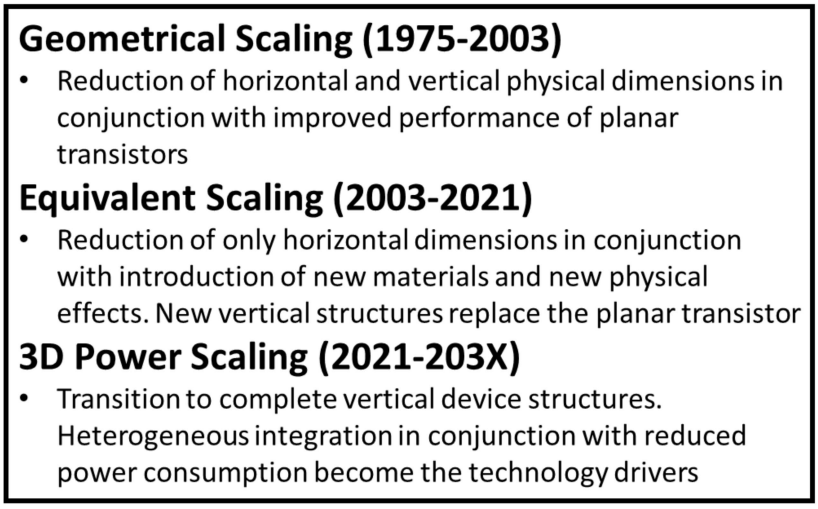


Figure B6 Les différents âges de mise à l'échelle

L'IRDS projette également cinq générations de transition fonctionnelle de la 2D à la 3D VLSI: (ici comprennent les dispositifs fonctionnels hétérogènes comme les capteurs, les nouveaux dispositifs de stockage, les circuits alternatifs logiques et de mémoire ou les circuits).

- Deux couches empilées avec des composants non mis à l'échelle, tels que l'analogique, les E/S et la gestion de l'alimentation dans une couche et la logique et la mémoire hautes performances dans l'autre.
- Intégration monolithique de deux couches, où chaque couche contient l'un des deux types de transistors fondamentaux en logique, NMOS et PMOS (semiconducteurs à oxyde métallique à canal n et à canal p) empilés les uns sur les autres pour une densité logique accrue.
- Deux couches: logique et mémoire.
- Connectivité analogique, E/S et RF en tant que couche supplémentaire, donnant plus de liberté pour inclure des périphériques spéciaux dans la conception.
- 3D VLSI avec logique-sur-logique à pas fin ainsi que des couches de fonctions spéciales exploitant de nouvelles architectures

B.4) Développement des circuits intégrés 3D

Aujourd'hui, les producteurs de mémoire flash font face à un problème similaire parce qu'ils manquent d'espace horizontal, et le coût de production de circuits mémoire intégrés de petites dimensions ne cesse d'augmenter tandis que le nombre d'électrons stockés dans la porte flottante ne cesse de diminuer. Pour éliminer ces problèmes, les producteurs de mémoire flash ont déjà démontré et annoncé plusieurs nouveaux produits qui empilent plusieurs couches de mémoire les unes sur les autres dans un seul CI. Jusqu'à 32 et 48 couches de mémoire flash ont été signalées.

Le Table 2 montre que les dispositifs de mémoire flash avec plus de 100 couches ont été prédits. L'élimination de la chaleur et la réduction de la puissance seront donc les deux principaux problèmes de la mise à l'échelle 3D.

Table 2 Tendances de la mémoire Flash (source: www.itrs2.net)

NAND flash Year of production	2015	2016	2020	2022	2024	2028	2030
2D NAND flash uncontacted poly ½ pitch-F (nm)	15	14	12	12	12	12	12
3D NAND minimum array ½ pitch-F (nm)	80nm	80nm	80nm	80nm	80nm	80nm	80nm
Number of word lines in one 3D NAND string	32	32-48	64-96	96-128	128-192	256-384	384-512
Domain cell type (FG, CT, 3D, etc.)	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D	FG/CT/3D
Product highest density (2D or 3D)	256G	384G	768G	1T	1.5T	3T	4T
3D NAND number of memory layers	32	32-48	64-96	96-128	128-192	256-384	384-512
Maximum number of bits per cell for 2D NAND	3	3	3	3	3	3	3
Maximum number of bits per cell for 3D NAND	3	3	3	3	3	3	3

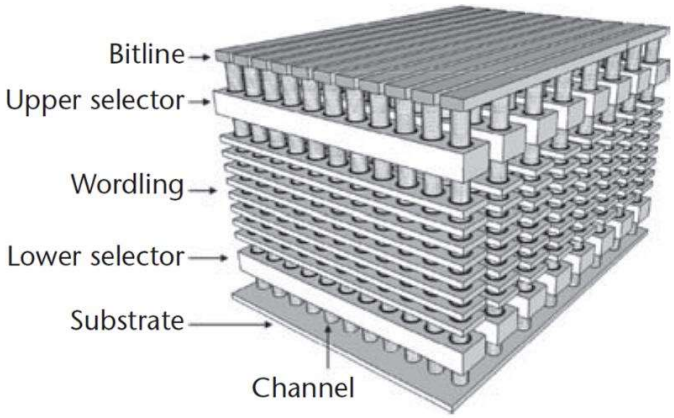


Figure B7 Exemple d'architecture 3D des futurs circuits intégrés monolithiques [3]

Au-delà de 2020, l'architecture des futurs IC changera en un type de structure similaire à celui de la Figure B7. Cette nouvelle phase de mise à l'échelle, capable d'ajouter des couches multiples au niveau des dispositifs 3D, peut considérablement accélérer la loi de Moore. La recherche sur de nouveaux commutateurs a débuté en 2005. En 2010, le tunnel FET (TFET) semble être un substitut potentiel des MOS, comme le montre la Figure B8, en raison de sa faible puissance de fonctionnement. [8] La capacité négative FET (NC FET) a également montré comme un autre concept qui a une performance de puissance plus large que MOS. [9], [10] Les nanotubes de carbone (nanotubes de carbone) sont devenus l'interrupteur le plus viable au cours de la prochaine décennie, en raison de ses économies d'énergie et de l'amélioration de ses performances. [11] Le nombre de transistors pouvant être intégrés sur un cm^2 de silicium continuera de croître au rythme de la loi de Moore pour les 10 prochaines années ou plus grâce à l'intégration 3D. Jusqu'à présent,

la vitesse du transistor a continué d'augmenter pendant cette décennie, et la fréquence de fonctionnement du transistor est déjà atteint 100 GHz si la dissipation de puissance n'était pas un problème, mais en raison des limites de dissipation de puissance des circuits intégrés, la fréquence de fonctionnement est limitée à quelques GHz (Intel Core i9 4.2 GHz). Ainsi, au cours de la prochaine décennie, l'objectif de la conception de circuits intégrés est changé de la conception de haute fréquence à la faible puissance et à une meilleure conception de la dissipation thermique.

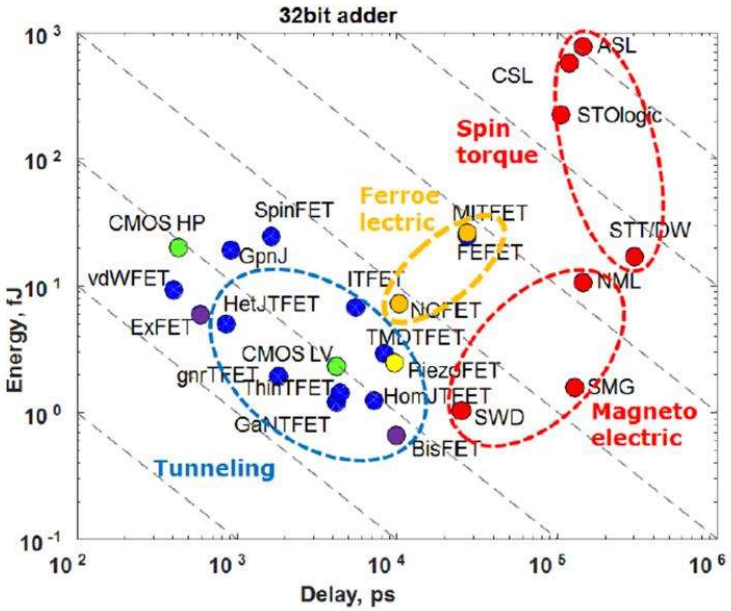


Figure B8 Commutation de l'énergie et du délai d'un additionneur 32 bits [12]

L'intégration et l'empaquetage tridimensionnels (3D) ont été couronnés de succès dans les dispositifs traditionnels pour augmenter la densité logique et réduire les distances de mouvement des données. Il résout les limites fondamentales de la mise à l'échelle, par ex. retard croissant dans les interconnexions [13], coûts de développement et variabilité [14]. La plupart des périphériques de mémoire livrés aujourd'hui comportent une forme 3D. L'intégration 3D a différentes technologies, avec le développement, ils sont wire-bonding et flip-chip pour SiP (Silicon in Package), TSV(Through Silicium Via) en substrat, TSV en SOI (Silicium sur isolant), 3D parallèle, 3D séquentiel (MIV inter-monolithique).

Dans la conception de niveau micro (> 2um), il existe deux types de méthode d'interconnection, wire-bonding et flip-chip. La typique technologie de l'interconnection est le wire-bonding. Le wire-bonding, comme représenté sur la Figure B10(a), a une faible densité, une faible bande passante, une latence élevée et une haute dissipation de puissance (les nombres exacts peuvent être trouvés dans le tableau 1 précédent). Et TSV est le via vertibal qui peut traverser le substrate directement. TSV en substrate est la technologie d'interconnection directe entre les puces, qui est la technologie principale dans l'industrie, car ils n'ont pas besoins de changement substantiel au flux de fabrication existant, comme le montre la Figure B10(b). La taille des capteurs d'image CMOS utilisant

l'approche "via last" a un diamètre d'environ 50 um. [15]–[19] Et il a une plus petite taille pour la mémoire 3D empilée (NAND, DRAM ...) et les circuits logiques (MPU avec mémoire cache). L'empilage consiste à percer des trous à travers des puces de silicium pour fournir des connexions électriques entre des couches différentes. TSV offre une bande passante plus faible et une connectivité moins efficace entre les couches de puces que l'ajout de couches avec des procédés de photolithographie, mais une bande passante et une efficacité bien plus élevées que l'utilisation d'un encapsulation de puces conventionnels. Il a un avantage de 10X plus de liaisons dans le circuit et une meilleure bande passante, une meilleure latence, une alimentation en moins [16], [20]–[22]. Cependant, la zone d'attente (KOZ) [23]–[28] requise pour les traversées en silicium (TSV) et les limites de précision d'alignement imposent des limites à la densité d'intégration de l'appareil qui peut être obtenue en utilisant l'empilage 3D TSV [2], [26].

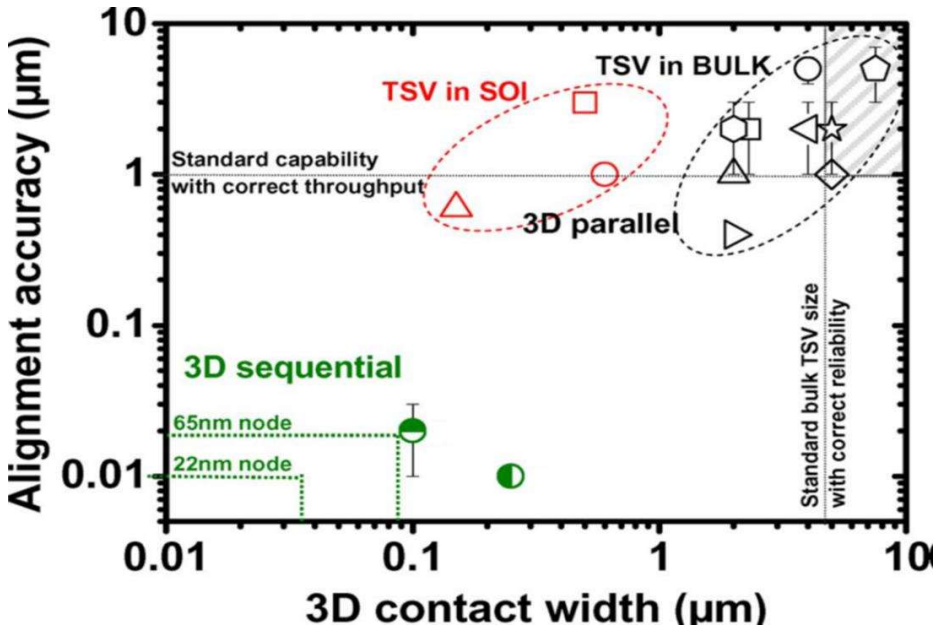


Figure B9 Capacité d'alignement par rapport à la largeur de contact 3D dans des schémas d'intégration parallèles et séquentiels [29]

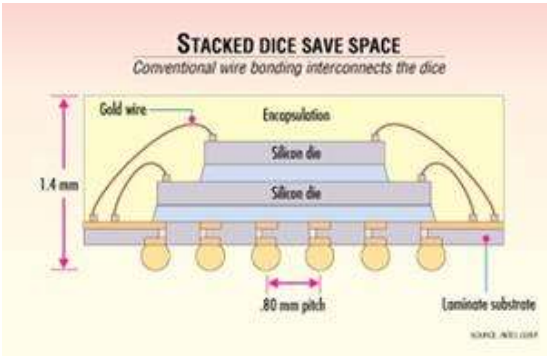
En dessous de 1um, dans ce domaine, l'intérêt de la technologie 3D reste à la conception de l'échelle des transistors. Comme observé sur la Figure B9, qui montre la précision d'alignement entre les couches de transistors empilés en ce qui concerne la largeur de contact 3D (pitch), l'intégration parallèle 3D [30], [31]comme montré dans la Figure B10(c), permet la réduction continue après 3D TSV, la réduction de la hauteur a été réduite à 1um. Mais même si certaines architectures 3D SOI (silicium sur isolant) peuvent réduire la taille de contact 3D, le pas de contact 3D reste toutefois limité par la performance d'alignement, limitée à environ 1um, pour garantir un débit correct.

L'intégration séquentielle 3D est la prochaine génération de technologies d'intégration 3D, elle est aussi appelée 3D monolithique (M3D) [1]–[4], [7], [13], [15], [25], [27], [29], [32]–[60]. Il a

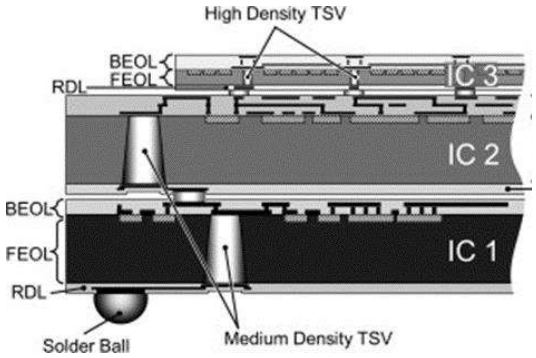
été démontré que les interconnexions 3D et les pas de contact planaires correspondent même pour les nœuds avancés [30] et il a le potentiel d'atteindre une densité de périphérique plus élevée comparée à l'empilement 3D basé sur TSV [60], et pour l'intégration parallèle 3D a une connexion de quelques milliers de blocs de transistors [31], comme indiqué dans le tableau 3. C'est trop grossier par rapport aux vias inter-niveaux monolithiques (MIVs) [29]. C'est pourquoi l'intégration séquentielle 3D est la seule possibilité d'exploiter pleinement le potentiel de la troisième dimension, notamment à l'échelle des transistors. Il existe trois catégories d'intégration M3D en fonction de la hauteur du partitionnement de niveau; intégration M3D au niveau des transistors, des portes et des blocs. Dans le transistor M3D, des transistors à canal P sont placés sur des transistors à un étage et à canal N sur un autre étage, et la connexion entre eux est établie par des MIV. Dans le M3D au niveau de la porte, les cellules standard sont réparties sur plusieurs niveaux, et les connexions inter-cellules qui traversent les niveaux utilisent des MIV. La conception M3D au niveau des blocs, qui est le style de conception le plus grossier, les blocs fonctionnels des partitions et les MIV inter-blocs sont déployés pour fournir des signaux entre les modules fonctionnels dans différents niveaux. Malheureusement, de nos jours, les outils commerciaux EDA pour soutenir l'intégration 3D ne sont pas disponibles temporairement. Ainsi, diverses études ont été rapportées sur la conception de circuits intégrés M3D en utilisant des outils commerciaux 3D. M3D a également l'inconvénient de l'incompatibilité des performances des périphériques et des interconnexions entre les niveaux, les tests de défis, les coûts, etc.

Table 3 Ratio entre le via 3D et le pas de contact planaire dans le cas séquentiel et parallèle [29][30][42]

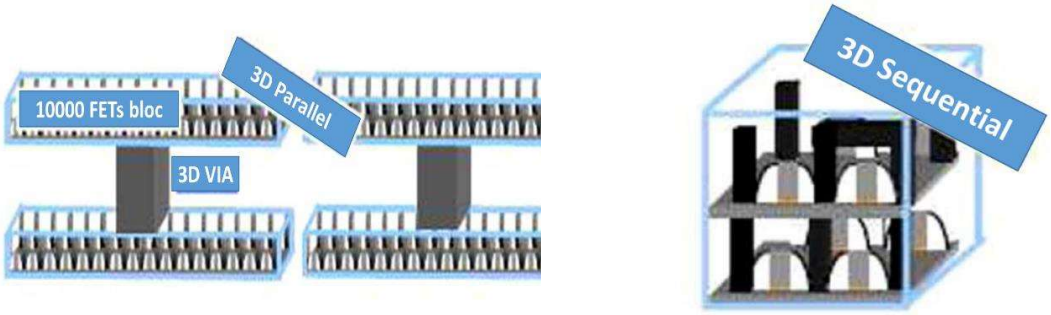
	Parallel		Sequential
Pitch	0.5um	1um	10nm
$D_{via3D}/D_{CONT,45nm}$	1/1000	1/10000	1/1



(a)



(b)



(c) (d)

Figure B10 Différentes technologies d'interconnexion 3D (a) Liaison filaire (b) Liaison via silicium (TSV haute densité et TSV moyenne densité) (c) Intégration parallèle 3D (d) Intégration séquentielle 3D

La mise en œuvre d'une structure 3D incluant CNFET, RAM résistive (RRAM) et RAM magnétique de transfert de spin (STT-MRAM) a déjà été proposée et analysée en utilisant N3XT (Nano-Engineered Computing Systems Technology) proposée par l'Université de Stanford et l'Université de Californie Berkeley. [61] La structure est montrée sur la Figure B11. Il a été démontré que le modèle N3XT avait une accélération de 23X et une réduction d'énergie de 37X, c'est-à-dire qu'il aurait un avantage de 851X en le produit énergie X retard.[61]

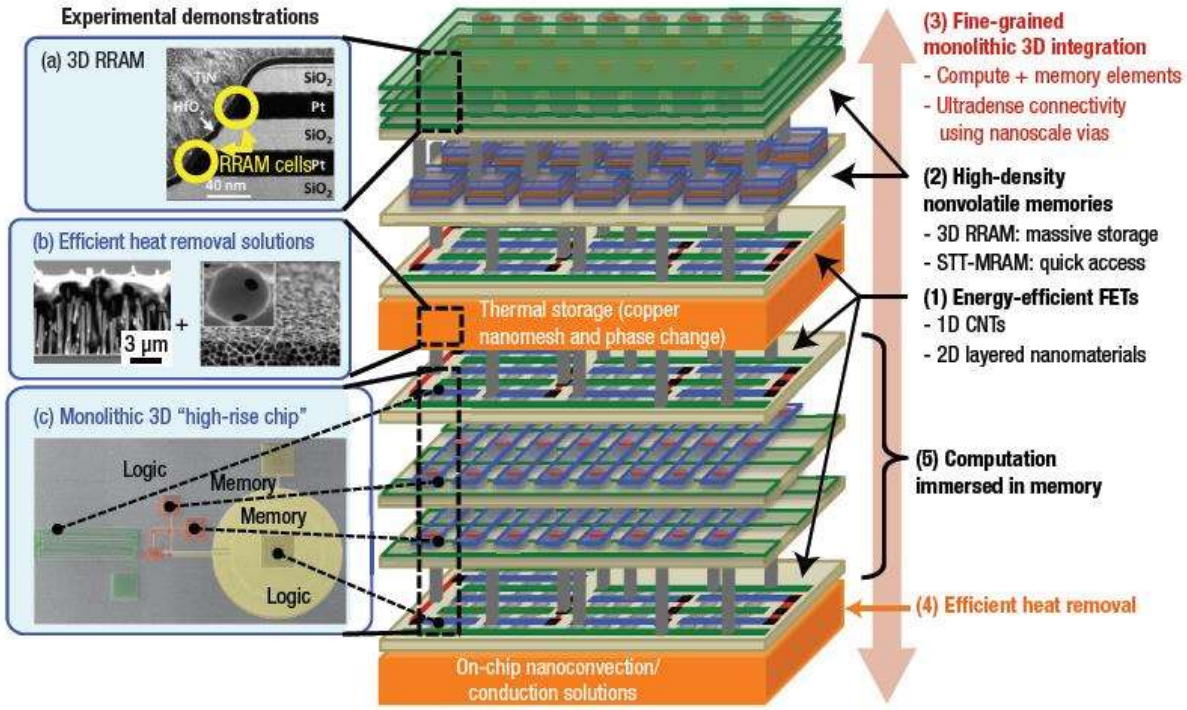


Figure B11 système 3D monolithique intégré activé par Nano-Engineered Computing Systems Technology (N3XT). Sur la droite sont les cinq composants clés N3XT. Sur la gauche sont des images de démonstrations de technologies expérimentales: (a) microscopie électronique à transmission (TEM) d'une RAM résistive 3D (RRAM) pour le stockage massif, (b) microscopie électronique à balayage (SEM) de matériaux nanostructurés pour une dissipation thermique efficace (gauche: advection capillaire microscopique, droite: nano-maillage cuivre avec

stockage thermique à changement de phase), et (c) SEM d'une puce 3D monolithique pour un calcul haute performance et économe en énergie. CNT: nanotubes de carbone, FET: transistors à effet de champ, et STT-MRAM: couple de transfert de spin RAM magnétique.[61]

B.5) Background and outline

Cette nouvelle architecture montre que les performances de calcul peuvent encore être améliorées dans la prochaine décennie, et la puissance principale dépendra de l'intégration hétérogène 3D. L'avenir de l'industrie des semi-conducteurs est donc prometteur, et les découvertes futures continueront à apporter des progrès et à apporter de nouvelles avancées.

Cette thèse s'inscrit dans un très vaste projet mené par ST Microelectronics crolles et le CEA LETI de Grenoble, en collaboration avec 3IT (Institut Interdisciplinaire d'Innovation Technologique) et l'Université de Sherbrooke. Ce projet a pour but de concevoir et de produire un capteur d'image CMOS 3D [62], et la conception du système de refroidissement de cet équipement est très importante; les problèmes de dissipation thermique dans le capteur d'image CMOS 3D peuvent être paralysants. Un autre démonstrateur (Figure B12) est en route. Ce démonstrateur applique la technologie de résonance magnétique nucléaire (RMN) / imagerie par résonance magnétique à l'échelle micro / nanométrique. Ces dernières années, les appareils portables RMN / IRM ont attiré l'attention de nombreuses équipes de chercheurs. Ils sont utilisés pour une variété d'applications, en particulier pour le diagnostic médical. Le schéma 3D de la puce micro / nano MNR est montré dans la Figure B12. Ce projet est piloté par de nombreux hôpitaux, ici des hôpitaux de Lyon et de New York [63]. Comme nous le savons, le récepteur de la bobine peut être facilement affecté par les bruits environnementaux; de plus, son bruit propre est exprimé en 4kRT; R est la résistance de la bobine. Donc, réduire le self-noise de la bobine signifie réduire cette résistance. Et, dans le même temps, le facteur de qualité Q de la bobine, défini comme $Q = \omega L/R$, sera augmenté. Le SNR (rapport de signal / bruit) dans la conception de bobine peut être un évaluateur pendant la miniaturisation de MNR / MRI.

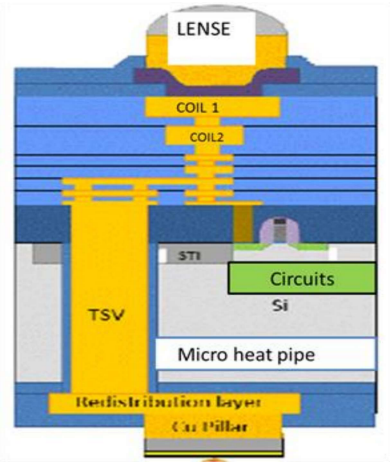


Figure B12 Relation de connectivité de la puce MNR (TSV, RDL: couche de redistribution et circuits intégrés dans le substrat)

Le but de la thèse est donc de fournir une méthode de conception globale pour le circuit intégré 3D dans le domaine électrique, thermique, électrothermique et aussi le bruit. Ci-après seront incluses des méthodes de simulation pour le substrat et également la connectivité relative (TSV, RDL(ligne de redistribution), Micro strip et circuits intégrés dans le substrat).

Le chapitre 2 présente quelques connaissances de base sur les effets parasitaires électriques des TSV. Basé sur des effets parasites, nous avons programmé dans Matlab un extracteur de substrat qui s'appele 3D-TLE (extracteur de ligne de transmission 3D), qui peut extraire automatiquement de tous les contacts; impédance, de forme arbitraire et de matériaux arbitraires. Cet extracteur est 100% compatible avec les simulateurs de noyau SPICE, comme ADS (Advanced design system). Les données extraites sont vérifiées avec des mesures et un résultat de simulation par la méthode des éléments finis (FEM). Basé sur des effets parasites du TSV, un RF filtre de fréquence 26 GHz et bande passante de 2 GHz est proposé dans ce travail.

Ainsi, le chapitre 3 propose une solution analytique pour la distribution de température non stationnaire du substrat multi-couches. Les problèmes thermiques sont des problèmes paralysants dans la conception de circuits intégrés 3D, en particulier lorsque nous réduisons à l'échelle nanométrique. La résistance électrique augmente avec la température, de même que la résistance du substrat. La plupart des travaux de simulation thermique sont basés sur les régimes stables; Peu de gens travaillent sur le cas non stationnaire. Les effets non stationnaires sont paralysants, comme les points chauds, qui peuvent être améliorés par des rampes de tension. Il propose également une méthode de calcul de dissipation thermique tridimensionnelle multi-couches 3D IC. Cette méthode est adaptée à tout circuit intégré 3D. Un cas de dissipation de chaleur CPU à 4 cœurs est étudié dans ce chapitre. La dernière partie de ce chapitre présente le fonctionnement de la simulation électrothermique. Le simulateur électrothermique peut être 100% compatible avec le simulateur SPICE (similaire), et la partie électrique est vérifiée avec ADS. Ce travail construit le cadre de l'analyse électrothermique 3D IC.

En tant que solution à la dissipation thermique locale, le composant dissipation de chaleur passive, caloduc plat (FHP) est proposé comme composante prospective dans le chapitre 4. Ce chapitre présente l'approche de simulation FEM du FHP, ainsi que la modélisation analytique. Les deux résultats ont une bonne correspondance.

Le chapitre 5 propose tout d'abord la solution analytique pour la distribution du bruit non stationnaire des substrats et présente des méthodes d'analyse du bruit. Et ce chapitre étudie aussi le keep-out-of-zone (KOZ) de TSV au transistor. Les méthodes d'investigation de l'impact du bruit électrique et de l'impact du bruit thermo-mécanique sont présentées dans cette partie.

Enfin, le chapitre 6 résume les contributions de ces travaux de thèse, tirant des conclusions du manuscrit.

B.6) TSV models modeling

B.6.1) Characterization and parameter extraction of two TSV model

Ici, nous proposons nos propres expressions analytiques pour le calcul de la résistance du modèle compact TSV de densité moyenne et de la capacité d'oxyde. Le TSV étant conique, les expressions sont dérivées des formules définissant un conducteur cylindrique parfait pour lequel nous avons appliqué, le long de la longueur du conducteur, des variations linéaires pour l'épaisseur et le rayon.

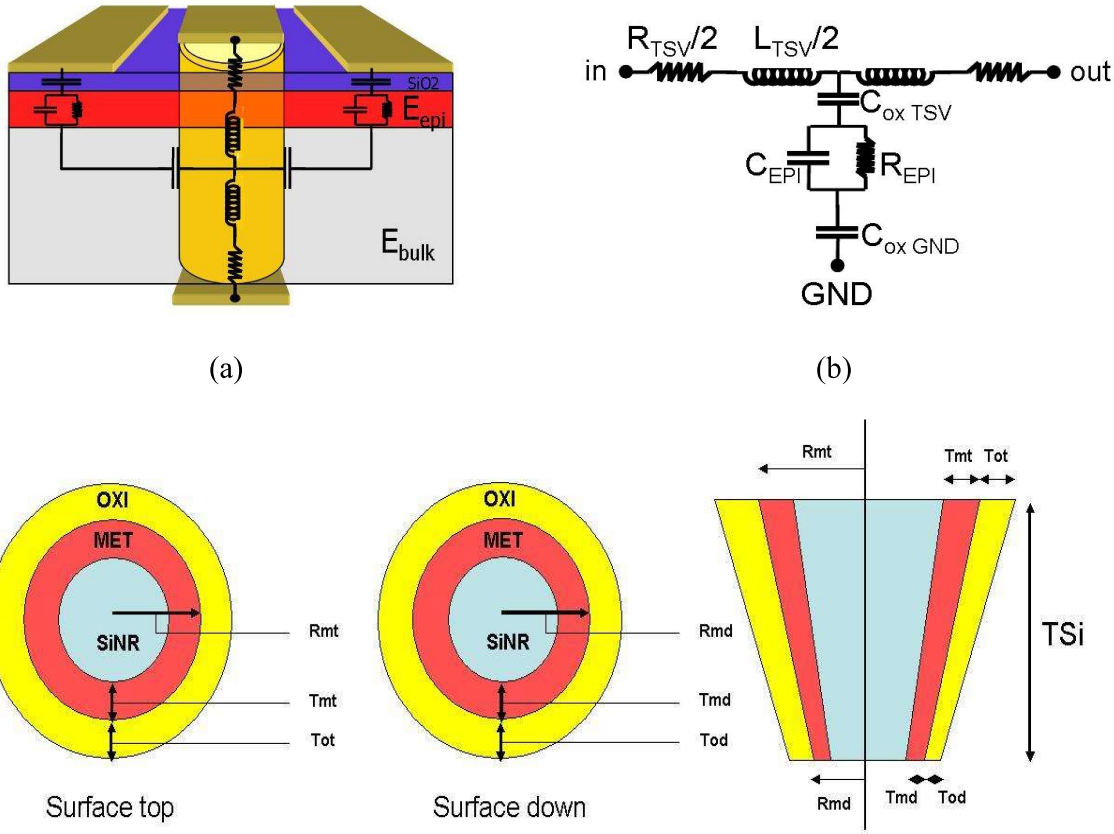


Figure B13 TSV schématique (a) vue en coupe transversale (b) modèle compact (c) paramètres de géométrie

$$R_{ot} = R_{mt} + T_{ot} \quad \text{(B-1)}$$

$$R_{od} = R_{md} + T_{od} \quad \text{(B-2)}$$

$$R_{TSV} = \frac{H}{\pi\sigma}\frac{1}{2(R_{mt}T_{md}-R_{md}T_{mt})}\ln\left(\frac{T_{md}}{2(R_{md}-T_{md})}\cdot\frac{2R_{mt}-T_{mt}}{T_{mt}}\right) \quad \text{(B-3)}$$

$$C_{ox(TSV)} = \frac{\varepsilon_0\varepsilon_{ox}2\pi H}{T_{ot}-T_{od}}\left[R_{ot} - R_{od} + \frac{R_{ot}\cdot T_{od}-R_{od}\cdot T_{ot}}{T_{ot}-T_{od}}\ln\left(\frac{T_{od}}{T_{ot}}\right)\right] \quad \text{(B-4)}$$

$$L_{TSV} = \frac{\mu_0\mu_r H}{2\pi}\left[sinh^{-1}\left(\frac{H}{R_a}\right) + \frac{R_a}{H} + 0.15 + \sqrt{\left(\frac{R_a}{H}\right)^2 + 1}\right] \quad \text{(B-5)}$$

$$M_{TSV} = \frac{\mu_0\mu_r H}{2\pi}\left[sinh^{-1}\left(\frac{H}{p}\right) + \frac{p}{H} - \sqrt{\left(\frac{p}{H}\right)^2 + 1}\right] \quad \text{(B-6)}$$

Où:

Rmt et *Tmt* sont le rayon de la couche de cuivre et l'épaisseur de la surface supérieure du TSV;

Rot et *Tot* sont le rayon de couche d'oxyde et l'épaisseur de la surface supérieure de TSV;

Rmd et *Tmd* le rayon de la couche de cuivre et l'épaisseur de la surface inférieure du TSV;

Rod et *Tod* le rayon de la couche d'oxyde et l'épaisseur de la surface inférieure du TSV.

p est le pas entre deux TSV voisins et Ra le rayon moyen TSV

Le matériau polymère qui remplit le TSV n'affecte pas significativement son comportement RF. Par ailleurs, les variations du rayon TSV et de l'épaisseur de la couche de cuivre sont très faibles. Par conséquent, les expressions analytiques d'un conducteur cylindrique rempli sont encore utilisées pour calculer les self et inductances mutuelles.

Puisque le substrat est hautement conducteur pour les CPW étudiés, il peut être modélisé comme une très faible résistance ou un nœud simple. Pour chaque ligne coplanaire, le trajet du courant vertical dans la couche épitaxiale mince est supposé présenter une forme parallélépipédique et donc modélisé par une résistance (Repi) en parallèle avec une capacité (Cepi). La modélisation de l'environnement contient également les capacités de couche d'oxyde (Cox) isolant les lignes de la couche épitaxiale.

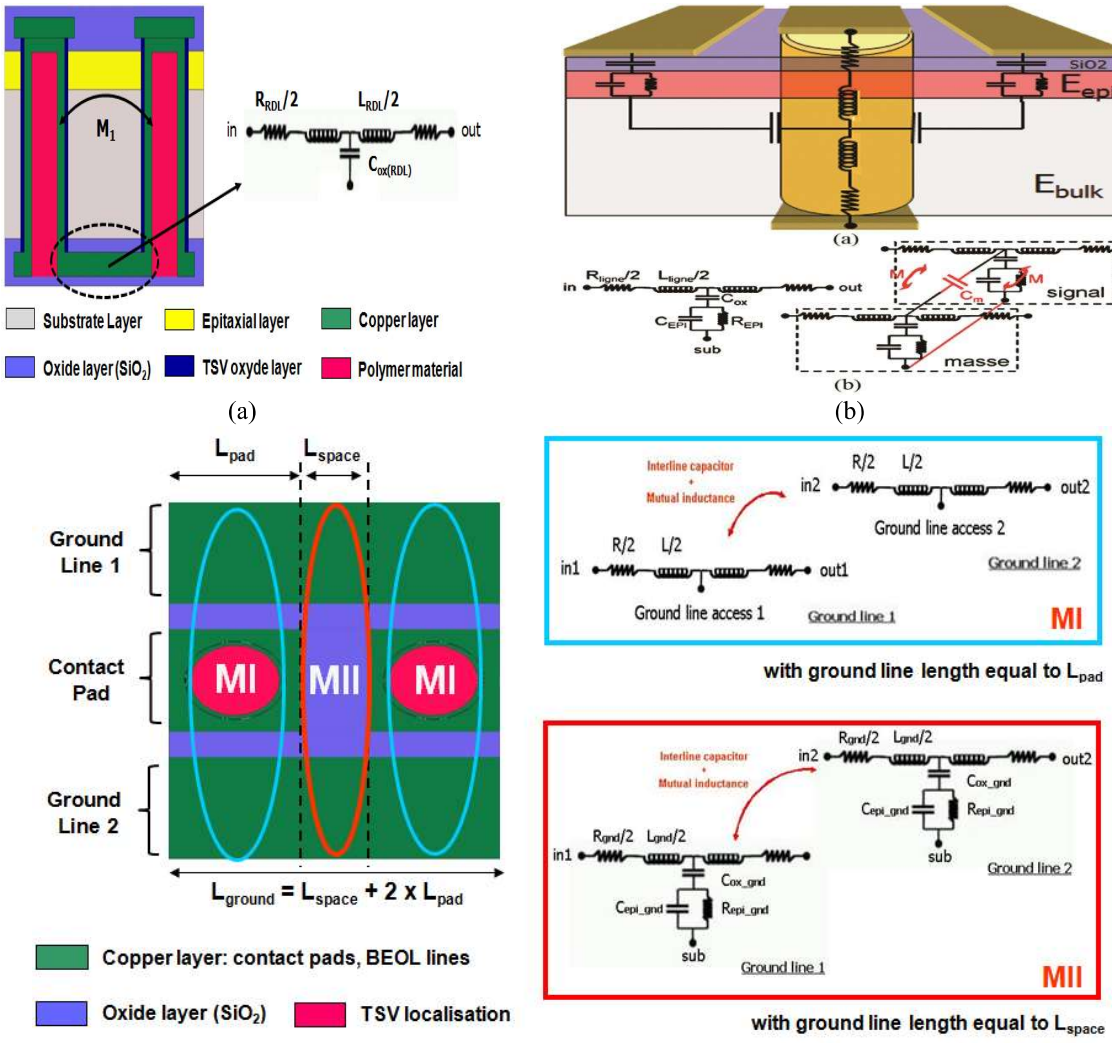
$$R_{epi} = \rho_{epi}\frac{T_{epi}}{W\cdot L} \quad \text{(B-7)}$$

$$C_{epi} = \frac{\varepsilon_{epi}\varepsilon_0 W\cdot L}{T_{epi}} \quad \text{(B-8)}$$

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0 W\cdot L}{T_{ox}} \quad \text{(B-9)}$$

Les valeurs des paramètres électriques doivent être adaptées selon que le modèle compact représente un modèle compact ou une cellule élémentaire d'un modèle distribué. Dans la chaîne TSV, les courants se propagent verticalement à travers l'épitaxie et les couches d'oxyde pour atteindre les plans de masse correspondant aux lignes de terrain de niveau BEOL. Les paramètres électriques des couches épitaxiales et des couches d'oxyde (Repi (TSV), Cepi (TSV) et Cox (GND)) sont calculés de la même manière que le guide d'ondes coplanaire en utilisant l'expression

précédente. Les couplages entre le substrat et les TSV sont pris en compte avec la capacité géométrique Cox (TSV). La capacité de la zone de déplétion de silicium est négligée car elle introduit un effet mineur dû au substrat hautement conducteur. Seuls les effets de proximité entre les TSV (couplages TSV / TSV) sont pris en compte. La modélisation du contexte électrique de la chaîne TSV consiste à diviser les lignes de masse BEOL en blocs sériels, en dissociant, sur la surface globale, les parties atteintes par le courant provenant des TSV. Ces pièces de surface ont une longueur correspondant aux plages de contact TSVs Lpad. Les paramètres de couche épitaxiale (Repi (TSV), Cepi (TSV)) et la capacité d'oxyde (Cox (GND)) qui modélisent la propagation du courant à la ligne de masse à travers le TSV, doivent donc être calculés pour L = Lpad. La largeur et l'épaisseur sont les mêmes pour toutes les parties de ligne tronquées. Les parties de surface des lignes de masse impliquées dans les chemins de courant sont simplement modélisées par des réseaux RL; sinon ils sont modélisés comme indiqué sur les figures suivantes.



(c)

Figure B14 Chaîne 2xTSV (a) Vue de face TSV moyenne densité (b) Modélisation RLCG compacte du TSV moyenne densité incluant le trajet du courant (c) Décomposition des lignes de masse BEOL en blocs série RLCG en fonction de la surface considérée (modèles MI et MII)

A titre d'illustration, les figures ci-dessus montrent comment les deux lignes de masse sont décomposées en blocs sériels pour une chaîne 2xTSV. Les parties des lignes concernées par le trajet actuel sont modélisées en MI et les surfaces restantes en MII. La longueur totale du câble, Lground, est égale à 2Lpad, plus la longueur de la ligne BRDL, Lspace. Notez que Lspace correspond également à l'écart entre les deux plages de contact. La ligne BRDL délimitant les deux TSV est décrite par une capacité d'oxyde atteignant le noeud de substrat SUB où se trouvent les surfaces de la ligne de masse BEOL, correspondant à l'entrefer des plots de contact (MII).

De la manière dont les TSV sont connectés, la chaîne 2xTSV peut être vue comme une structure en "U". Pour les chaînes nxTSVs, n / 2 structures en "U" sont connectées au niveau BEOL par des plages de contact et des lignes d'accès de longueur 60µm quelle que soit la configuration.

La figure suivante montre la vue de profil d'une chaîne 4xTSV; les effets de proximité entre les quatre TSV sont également représentés. La longueur totale de la ligne de masse BEOL est donc égale à:

$$L_{BEOL} = nL_{pads} + \frac{n}{2}L_{space} + (\frac{n}{2} - 1)L_{access} \qquad \text{(B-10)}.$$

Il illustre la décomposition des lignes de base en blocs de série dans le cas de la chaîne 4xTSV. La décomposition peut être étendue pour les chaînes comprenant un plus grand nombre de TSV.

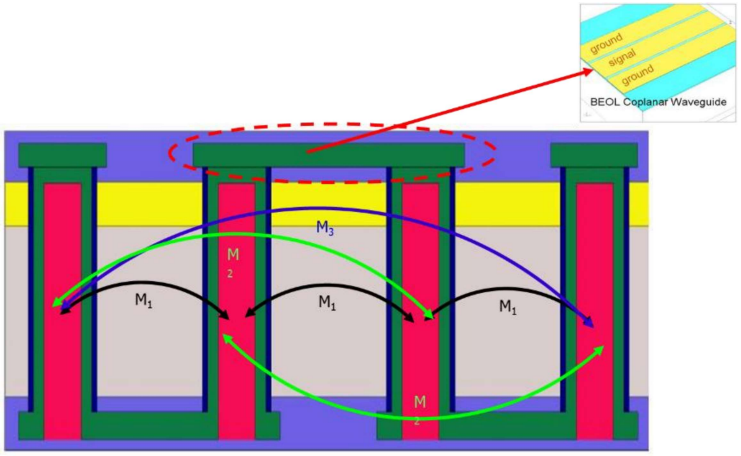


Figure B15 latérale de la chaîne 4xTSV: représentation des effets de proximité entre les TSV (couplages inductifs). Les deux chaînes de 2xTSV sont connectées au niveau BEOL avec des plages de contact et une ligne d'interconnexion d'accès

B.6.2) Simulation of 2 TSVs model

Nous utilisons le même processus de simulation. Tout d'abord, nous essayons de simuler les paramètres S en utilisant la Spice netlist générée par le 3D-TLE. Et nous le comparons avec les mesures de TSV Umodel (Figure B16).

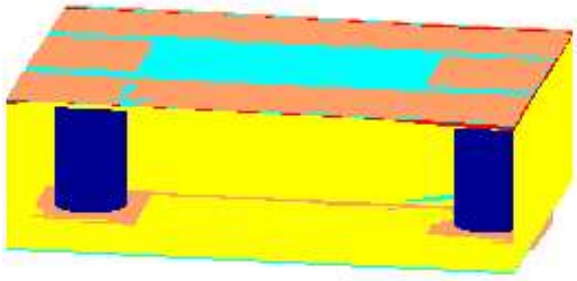


Figure B16 Géométrie physique du modèle 2 TSV

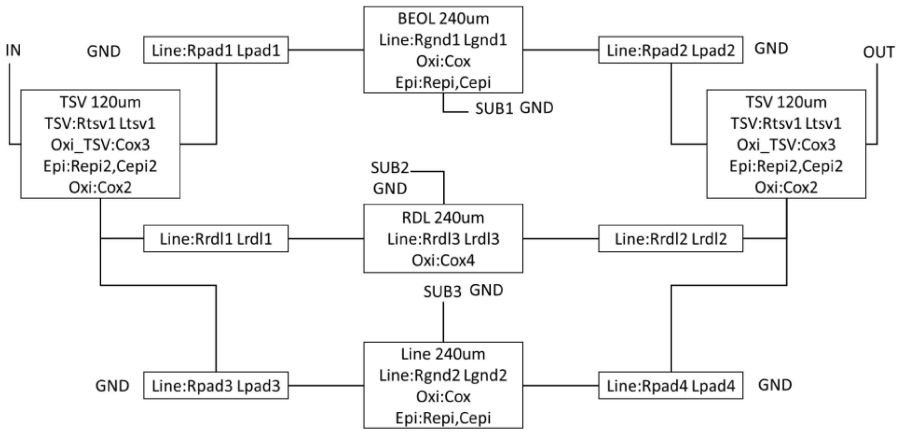


Figure B17 description du script d'entrée

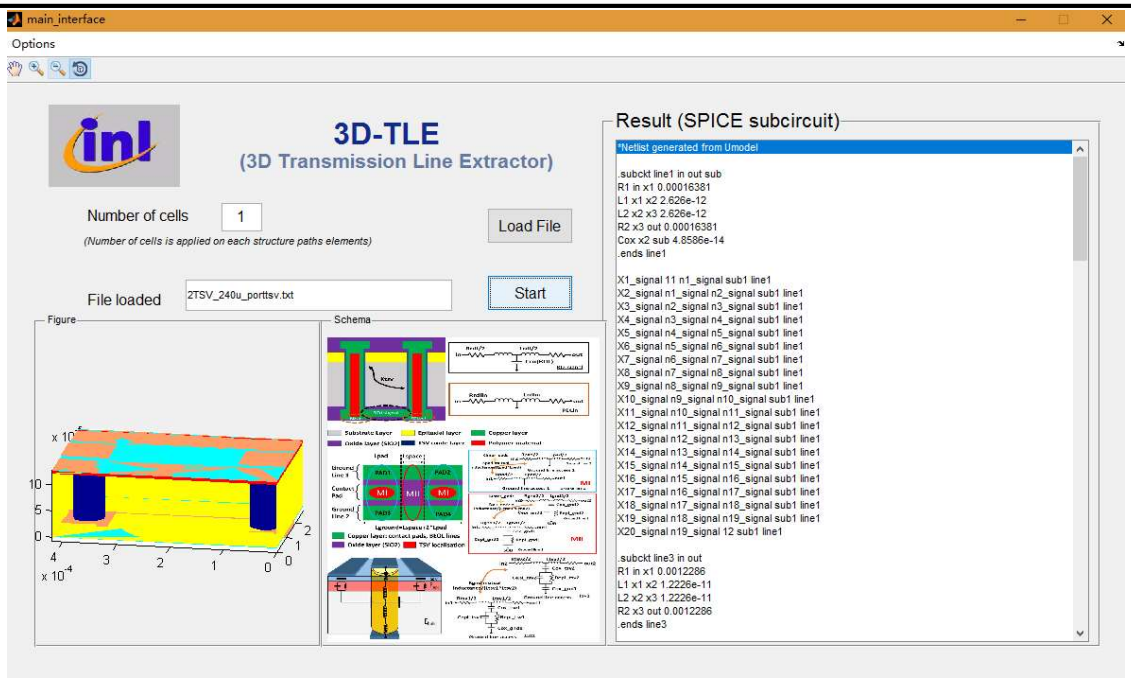


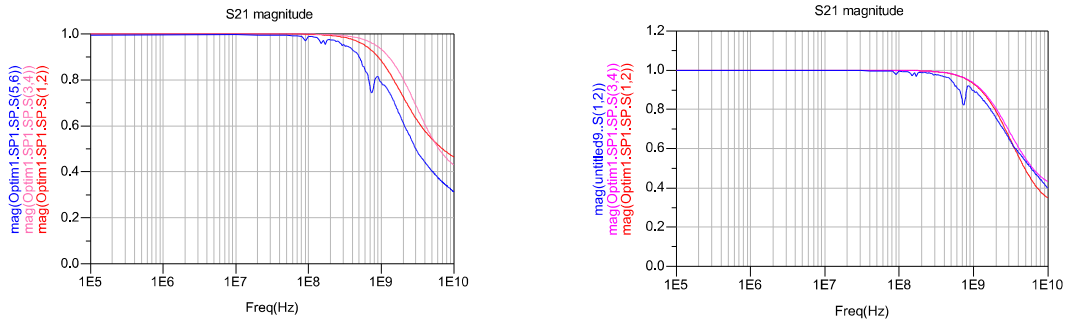
Figure B18 Réglage de l'extracteur 3D-TLE

A travers le pub [115], les paramètres parasites du substrat peuvent être exprimés par un parallèle de capacité et de conductance. Et leurs expressions sont montrées comme suit

$$C_{Si\_sub} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,si}}{cosh^{-1}(\frac{p_{TSV}}{d_{TSV}})} \times h_{TSV}[F] \quad \text{(B-11)}$$

$$G_{Si\_sub} = \frac{\pi \times \sigma_{si}}{cosh^{-1}(\frac{p_{TSV}}{d_{TSV}})} \times h_{TSV}[S] \quad \text{(B-12)}$$

Et ici, lorsque nous extrayons les mesures, nous devons appliquer la méthode de dés-inclusion, les deux figures suivantes montrent la différence.



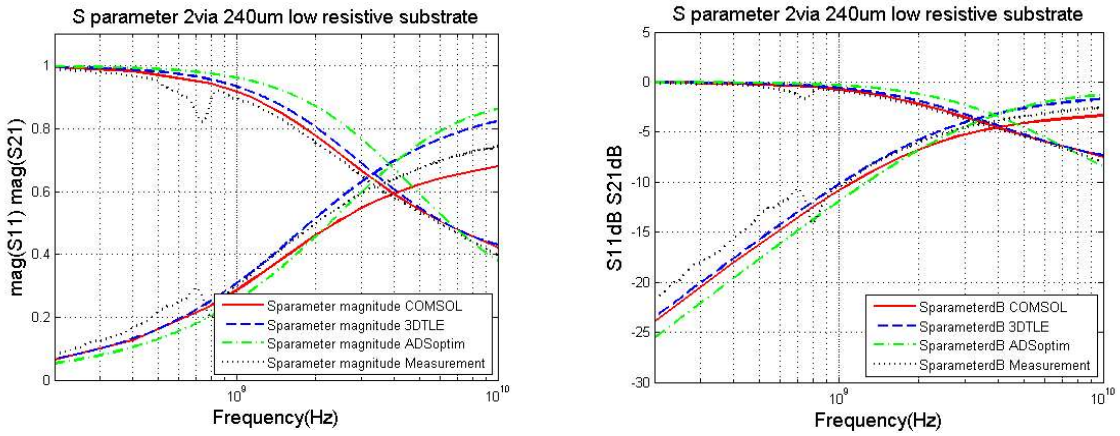
Mesures S21 résultat sans dés-enrobage (ligne bleue)

Mesures S21 résultat avec dés-enrobage (ligne bleue)

Figure B19 Paramètres du modèle S de 2xTSVs (a) amplitude de S21 sans désincrustation (b) amplitude de S21 avec désemboîtement

Comme on peut le voir sur les deux figures, le résultat avec dés-enrobage est plus proche de nos circuits simulés.

Afin de vérifier notre extracteur 3D-TLE, une simulation par éléments finis (comsol) est réalisée. Les résultats de la simulation sont présentés comme suit. Ils ont un très bon rapport entre l'extracteur 3D-TLE, la simulation COMSOL et la mesure.



(a) (b)

Figure B20 Vérification 3D-TLE en utilisant FEM (COMSOL), ADS et mesures (a) Magnitude des paramètres S (b) dB des paramètres S

B.7) Electro-thermal (ET) modeling of VLS circuits

La feuille de route pour les circuits intégrés (CI) impose une densité de puissance croissante et une tension d'alimentation décroissante, ce qui oblige les réseaux de distribution d'énergie (PDN) à fournir des courants plus importants [4], [55]. En conséquence, l'auto-échauffement dû à l'effet Joule et à l'activité de commutation de puissance [203] est responsable d'une élévation de température de plus en plus importante qui affecte dramatiquement les performances électriques, par exemple en raison de la dépendance de la température de résistivité électrique [202]. Par conséquent, une co-simulation électro-thermique (ET) efficace des grands PDN sur puce est aujourd'hui nécessaire, par exemple, pour donner une estimation correcte de la chute IR, fortement liée à la résistivité électrique. De plus, les co-simulations ET sont inévitables si l'intégration verticale 3D est envisagée, étant donné les courants croissants dans ces systèmes comparés aux 2D et la densité de flux thermique croissante due à l'empilement dans la direction verticale [143][106].

Dans ce travail, nous présentons des techniques de réduction d'ordre de modèle pour la co-simulation ET de grands PDN, sur la base du concept de clustering de nœuds. La stratégie de réduction est ensuite mise en œuvre en définissant des macro-nœuds, à partir d'un critère qui établit que les interactions locales entre deux nœuds du modèle original pourraient être négligées. Après avoir choisi une définition correcte des niveaux de quantification pour les plages de température et de chute de tension, les nœuds sont classés en sous-ensembles. Ensuite, les sous-ensembles sont réduits à des noeuds de macro, et les éléments de connexion entre eux sont calculés en conséquence.

Une telle procédure permet une réduction drastique de l'ordre du système, tout en assurant une bonne précision.

Nous considérons une structure standard pour les réseaux de masse et de puissance comme représenté sur la figure suivante 18. Les deux réseaux conducteurs sont séparés par une couche d'isolation, et connectés aux broches d'alimentation VDD et GND, respectivement, par une impédance série Zsupply aux quatre coins de l'élément de base (cachet) des noeuds nxn sur la grille. La puce entière est obtenue en tant que répliques mxm d'un tel tampon. La puce est connectée d'un côté à un dissipateur thermique, à des fins de dissipation thermique.

Les problèmes électriques et thermiques doivent être résolus conjointement dans l'analyse statique (et éventuellement dynamique). Une modélisation adéquate de la puce, du point de vue thermique et électrique, sera fournie et justifiée, en référence à toutes les possibilités technologiques envisagées tout au long du document. Les principales sources de chaleur dans la structure sont associées à l'activité du circuit (commutation des portes logiques), ainsi qu'aux effets Joule dans les interconnexions PDN. Il existe une dualité bien connue entre les modèles de transport thermique et électrique, où le flux de chaleur joue le rôle d'un courant électrique et la différence de température correspond à la tension électrique. De cette manière, l'équivalence électrothermique classique peut être exploitée de manière appropriée pour une co-simulation conjointe du problème physique, dans le même solveur de circuit. [193]–[195]

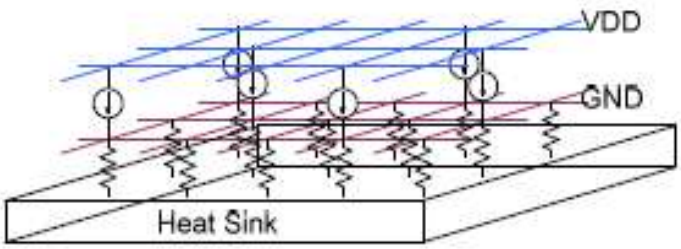


Figure B21 Structure pour les réseaux au sol et de puissanceElectrical modeling of VLS circuits

Une analyse électrique dynamique peut être réalisée une fois que des équivalents dynamiques parasites ont été définis et estimés pour la structure. Nous nous référons à la modélisation de premier ordre standard de chaque structure de structure concernée, en considérant une inductance parasite série L pour chaque connexion entre des nœuds adjacents de la même grille, et une capacité parallèle C entre des nœuds correspondants sur les deux grilles différentes. De cette façon, nous définissons une cellule élémentaire dynamique comme indiqué dans la Figure B22 suivante.

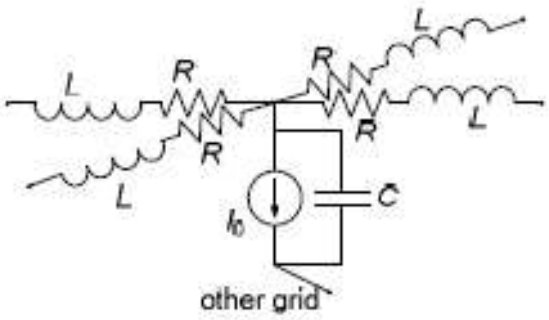


Figure B22 Cellule élémentaire électrique dynamique

B.7.1) Vérification du modèle électrique

B.7.1.1) Cas I: modélisation électrique du modèle de segments 3xRLC

Le modèle peut être décrit à l'aide d'un script Spice

```
* Example RLC-3

Vin N_in1   0 PULSE 0 3 0.5m 0.5m  0.5m 4m  10m

X1  n_in1   n_in2   seg
X2  N_in2   N_in3   seg
X3  n_in3   n_out   seg
Cl  n_out   0       10u

.SUBCKT seg n_in    n_out
Rseg    N_IN    N_1     3.5
Lseg    n_1     N_OUT   1.2m
Cseg    N_OUT   0       7.3u
.ENDS seg

.TRAN   0.004m 20m
.PROBE  V(n_out)
.print V(n_out)
.end
```

Figure B23 de Spice série 3xRLC

Le modèle décrit un circuit RLC à 3 segments. Le circuit électrique est représenté sur les figures suivantes

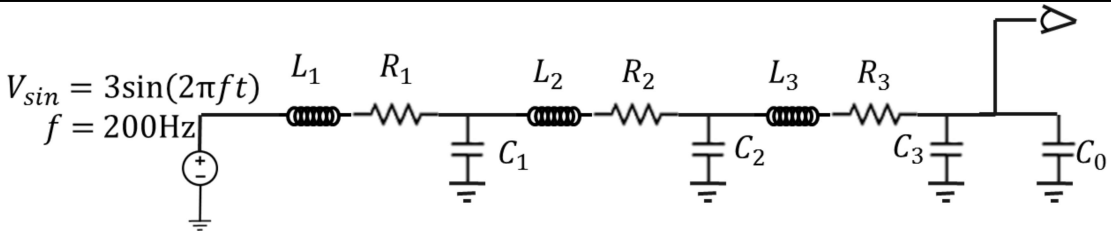
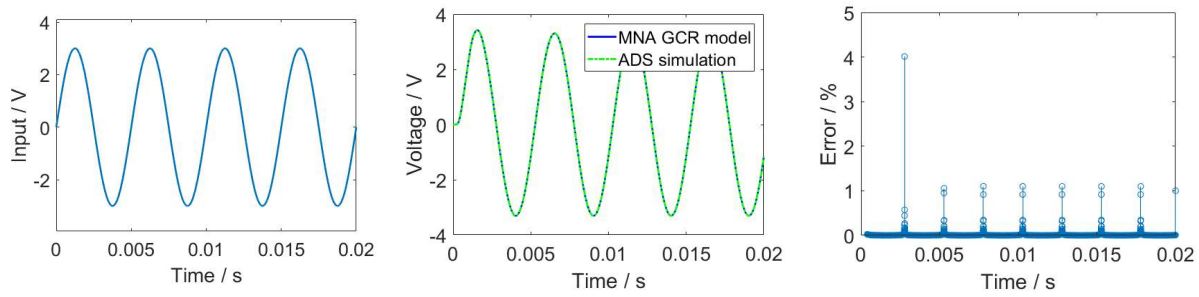


Figure B24 Modèle compact of 3 segments RLC

La résistance des segments est de 3,5 ohms, l'inductance est de 1,2e-3 H, la capacité est de 7,3e-6 F et la capacité supplémentaire du côté de la sonde est de 10e-6 F. La source de tension est un signal sinusoïdal d'amplitude de 3V, et fréquence de travail 200Hz. Ici, nous utilisons la méthode d'analyse nodale modifiée (MNA) et le résolveur général conjugué résiduel (GCR) et aussi la technique de la matrice clairsemée pour résoudre et accélérer le calcul de matrice différentielle à grande échelle, la description précise de la méthode peut être trouvée en annexe. Afin de vérifier la robustesse de la méthode, la même simulation est faite avec ADS (Advanced Design System de Keysight Technologies [207]). Le signal est représenté sur la figure (a), la comparaison du signal de sortie avec ADS est représentée sur la figure (b) et la figure (c) montre l'erreur relative de la méthode MNA + GCR et de l'ADS. Comme nous pouvons le voir sur la figure (c), notre méthode MNA + GCR a une très bonne précision par rapport à l'ADS, l'erreur maximale est d'environ 4%.



(a) (b) (c)

Figure B25 (a) Source de tension d'entrée (b) Comparaison de sortie entre MNA et ADS (c) Erreur relative entre MNA et ADS pour 3 modèle de segments RLC

B.7.1.1) Cas II: CPW (modèle d'onde coplanaire)

De la même manière, mais un peu différent, nous définissons les paramètres géométriques et matériels du modèle dans un fichier txt [208], puis en utilisant 3D-TLE d'INL (extracteur de ligne de transmission 3D), générons automatiquement un fichier sp compatible spice. Ce fichier est illustré dans la Figure B26 suivante.

```
*Netlist generated from Umodel
Vin in_real  0 PULSE 0 3 0.5m 0.5m  0.5m 4m 10m
.subckt gnd1_signal_gnd2 in1 out1 in2 out2 in3 out3

R1 in1 x1_gnd1 0.03225
```

```
L1 x1_gnd1 x2_gnd1 5.6541e-11
L2 x2_gnd1 x3_gnd1 5.6541e-11
R2 x3_gnd1 out1 0.03225
Cox_gnd1 x2_gnd1 nox_gnd1 1.3335e-12
Repi_gnd1 nox_gnd1 0 312.5
Cepi_gnd1 nox_gnd1 0 1.6567e-14

R3 in2 x1_signal 0.028667
L3 x1_signal x2_signal 5.3965e-11
L4 x2_signal x3_signal 5.3965e-11
R4 x3_signal out2 0.028667
Cox_signal x2_signal nox_signal 1.5002e-12
Repi_signal nox_signal 0 277.7778
Cepi_signal nox_signal 0 1.8638e-14

R5 in3 x1_gnd2 0.03225
L5 x1_gnd2 x2_gnd2 5.6541e-11
L6 x2_gnd2 x3_gnd2 5.6541e-11
R6 x3_gnd2 out3 0.03225
Cox_gnd2 x2_gnd2 nox_gnd2 1.3335e-12
Repi_gnd2 nox_gnd2 0 312.5
Cepi_gnd2 nox_gnd2 0 1.6567e-14

K1 L1 L3 0.42787
K2 L2 L4 0.42787
Cinter1 x2_signal x2_gnd1 6.7837e-15

K3 L3 L5 0.42787
K4 L4 L6 0.42787
Cinter2 x2_gnd2 x2_signal 6.7837e-15

K5 L1 L5 0.30072
K6 L2 L6 0.30072

.ends gnd1_signal_gnd2

X1_gnd1_signal_gnd2 0 0 1 2 0 0 gnd1_signal_gnd2
C1 2 0 100e-15
R1 in_real 1 50
.TRAN   0.004m 20m
.PROBE  V(2)
.print V(2)
.end
.end
```

Figure B26 Modèle CPW Spice script

Le modèle décrit un modèle d'onde coplanaire. Le circuit électrique est représenté sur la Figure B27 suivante.

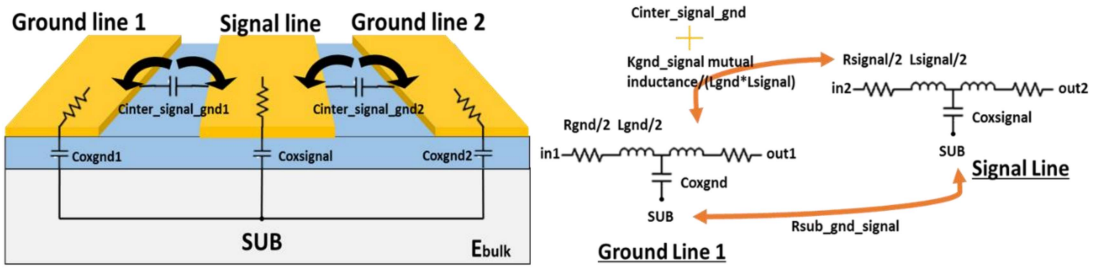
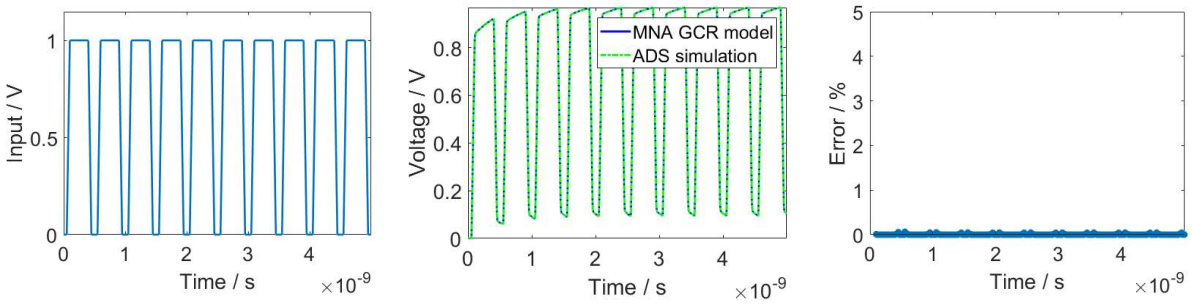


Figure B27 Géométrie CPW et modèle compact

Nous définissons deux types de lignes, une ligne de signal, une ligne de fond, et chaque ligne est traitée comme un modèle T. Nous définissons un Cinter entre deux lignes quelconques et chaque ligne est isolée du substrat par une couche d'oxyde. La source de tension est un signal impulsionnel, avec une amplitude de 1 V, des temps de montée et de descente de 0,05ns, un cycle de travail de 60% et une fréquence de travail de 2GHz. Ici, nous utilisons également la méthode d'analyse nodale modifiée (MNA) et la résolution résiduelle conjuguée généralisée (GCR). Afin de vérifier la robustesse de la méthode, la même simulation est effectuée dans ADS. Le signal est représenté sur la figure (a), la comparaison du signal de sortie avec ADS est représentée sur la figure (b) et la figure (c) montre l'erreur relative de la méthode MNA + GCR et de l'ADS. Comme nous pouvons le voir sur la figure (c), notre méthode MNA + GCR a une très bonne précision par rapport à l'ADS, l'erreur maximale est d'environ 3,5%.



(a) (b) (c)

Figure B28 (a) Source de tension d'entrée (b) Comparaison de sortie entre MNA et ADS (c) Erreur relative entre MNA et ADS pour modèle CPW

B.7.1.2) Cas III: Deux TSV (via le silicium via) Umodel

De la même manière, nous définissons les paramètres géométriques et matériels du modèle dans un fichier txt, puis en utilisant notre (voir chapitre 2) 3D-TLE (extracteur de ligne de transmission 3D), générons automatiquement un fichier sp compatible spice. Ce fichier est montré comme suit.

```
*Netlist generated from Umodel
Vin in_real  0 PULSE 0 3 0.5m 0.5m  0.5m    4m  10m
```

```
.subckt line1 in out
R1 in x1 0.0032762
L1 x1 x2 5.2519e-11
L2 x2 x3 5.2519e-11
R2 x3 out 0.0032762
Cox x2 0 9.7173e-13
.ends line1

X1_signal 11 12 line1

.subckt line3 in out
R1 in x1 0.0012286
L1 x1 x2 1.2226e-11
L2 x2 x3 1.2226e-11
R2 x3 out 0.0012286
.ends line3

X1_rdlin 1 11 line3

X1_rdlout 12 2 line3

.subckt gnd1_gnd2 in1 out1 in2 out2

R1 in1 x1_gnd1 0.03225
L1 x1_gnd1 x2_gnd1 5.6541e-11
L2 x2_gnd1 x3_gnd1 5.6541e-11
R2 x3_gnd1 out1 0.03225
Cox_gnd1 x2_gnd1 nox_gnd1 9.8554e-13
Repi_gnd1 nox_gnd1 0 18.9375
Cepi_gnd1 nox_gnd1 0 4.9702e-13

R3 in2 x1_gnd2 0.03225
L3 x1_gnd2 x2_gnd2 5.6541e-11
L4 x2_gnd2 x3_gnd2 5.6541e-11
R4 x3_gnd2 out2 0.03225
Cox_gnd2 x2_gnd2 nox_gnd2 9.8554e-13
Repi_gnd2 nox_gnd2 0 18.9375
Cepi_gnd2 nox_gnd2 0 4.9702e-13

K1 L1 L3 0.30072
K2 L2 L4 0.30072
Cinter1 x2_gnd2 x2_gnd1 1.1493e-15

.ends gnd1_gnd2

X1_gnd1_gnd2 3 4 5 6 gnd1_gnd2


.subckt pad1_pad3 in1 out1 accesstsv1 in2 out2 accesstsv2

R1 in1 x1_pad1 0.012094
L1 x1_pad1 accesstsv1 1.3508e-11
L2 accesstsv1 x2_pad1 1.3508e-11
```

```
R2 x2_pad1 out1 0.012094

R3 in2 x1_pad3 0.012094
L3 x1_pad3 accesstsv2 1.3508e-11
L4 accesstsv2 x2_pad3 1.3508e-11
R4 x2_pad3 out2 0.012094

K1 L1 L3 0.74376
K2 L2 L4 0.74376
Cinter1 accesstsv2 accesstsv1 4.3097e-16

.ends pad1_pad3

X1_pad1_pad3 0 3 101 0 5 102 pad1_pad3


.subckt pad2_pad4 in1 out1 accesstsv1 in2 out2 accesstsv2

R1 in1 x1_pad2 0.012094
L1 x1_pad2 accesstsv1 1.3508e-11
L2 accesstsv1 x2_pad2 1.3508e-11
R2 x2_pad2 out1 0.012094

R3 in2 x1_pad4 0.012094
L3 x1_pad4 accesstsv2 1.3508e-11
L4 accesstsv2 x2_pad4 1.3508e-11
R4 x2_pad4 out2 0.012094

K1 L1 L3 0.74376
K2 L2 L4 0.74376
Cinter1 accesstsv2 accesstsv1 4.3097e-16

.ends pad2_pad4

X1_pad2_pad4 4 0 201 6 0 202 pad2_pad4


.subckt tsv1_tsv2 in1 out1 side1 side2 in2 out2 side3 side4

R1 in1 x1_tsv1 0.0031471
L1 x1_tsv1 x2_tsv1 1.8915e-11
L2 x2_tsv1 x3_tsv1 1.8915e-11
R2 x3_tsv1 out1 0.0031471
Coxtsv1_tsv1 x2_tsv1 p1_tsv1 1.9807e-12
Coxtsv2_tsv1 x2_tsv1 p2_tsv1 1.9807e-12
Repi1_tsv1 p1_tsv1 epi1_tsv1 50.5
Cepi1_tsv1 p1_tsv1 epi1_tsv1 1.8638e-13
Repi2_tsv1 p2_tsv1 epi2_tsv1 50.5
Cepi2_tsv1 p2_tsv1 epi2_tsv1 1.8638e-13
Coxgnd1_tsv1 epi1_tsv1 side1 3.6958e-13
Coxgnd2_tsv1 epi2_tsv1 side2 3.6958e-13

R3 in2 x1_tsv2 0.0031471
```

```
L3 x1_tsv2 x2_tsv2 1.8915e-11
L4 x2_tsv2 x3_tsv2 1.8915e-11
R4 x3_tsv2 out2 0.0031471
Coxtsv1_tsv2 x2_tsv2 p1_tsv2 1.9807e-12
Coxtsv2_tsv2 x2_tsv2 p2_tsv2 1.9807e-12
Repi1_tsv2 p1_tsv2 epi1_tsv2 50.5
Cepi1_tsv2 p1_tsv2 epi1_tsv2 1.8638e-13
Repi2_tsv2 p2_tsv2 epi2_tsv2 50.5
Cepi2_tsv2 p2_tsv2 epi2_tsv2 1.8638e-13
Coxgnd1_tsv2 epi1_tsv2 side3 3.6958e-13
Coxgnd2_tsv2 epi2_tsv2 side4 3.6958e-13

K1 L1 L3 0.11406
K2 L2 L4 0.11406

.ends tsv1_tsv2

X1_tsv1_tsv2 in 1 101 102 2 out 201 202 tsv1_tsv2
R1_tsv1 in_real in 50
C1_tsv2 out 0 100e-15
.TRAN   0.004m 20m
.PROBE  V(out)
.print V(out)
.end
.end
```

Figure B29 Chaîne 2xTSVs U modèle

Le modèle décrit un modèle d'onde coplanaire. Le circuit électrique est représenté sur la Figure B30 suivante.

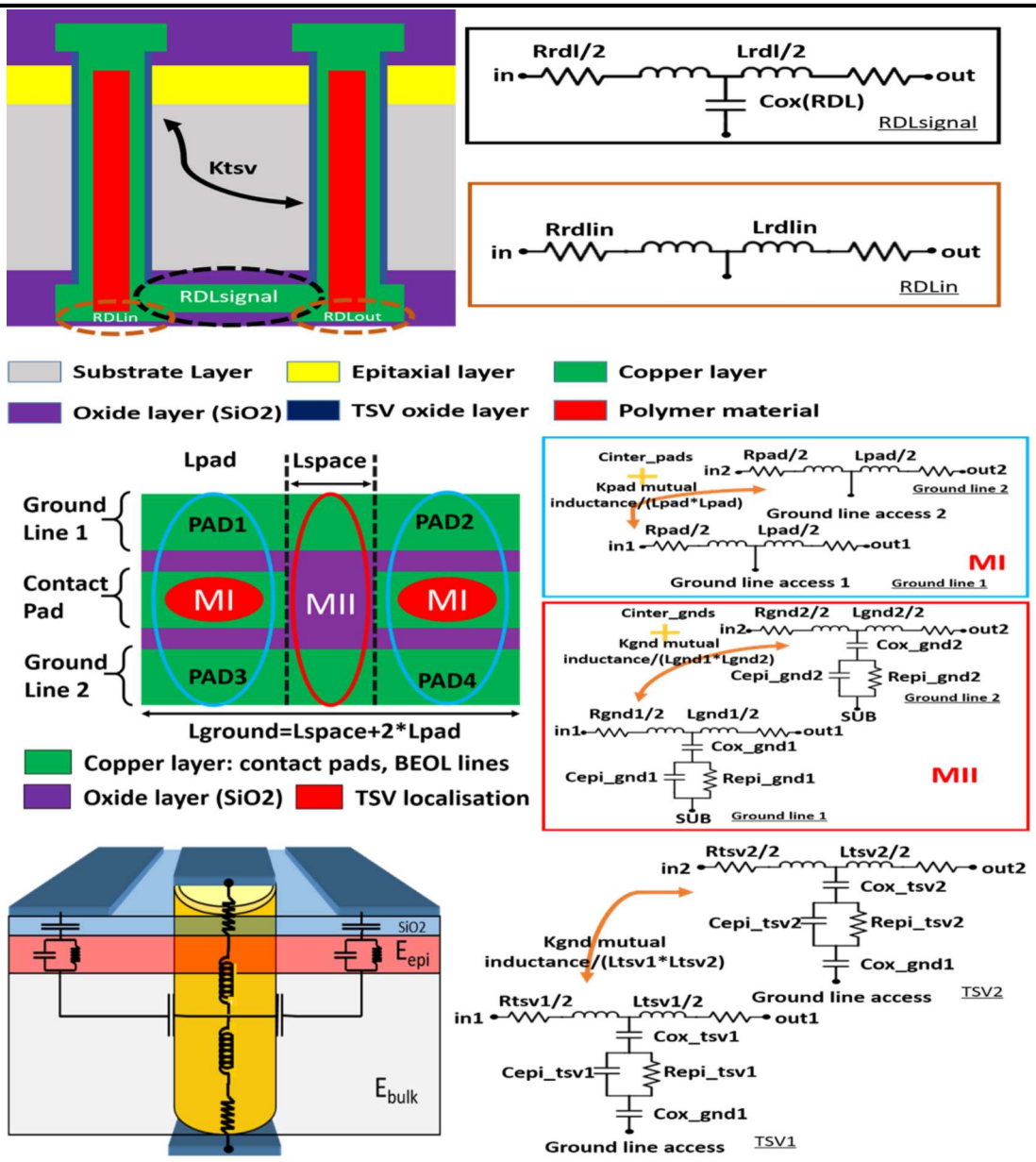
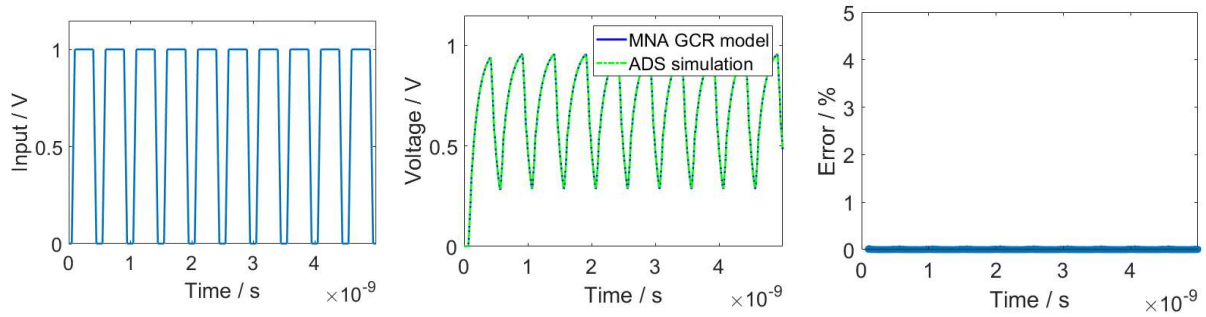


Figure B30 du modèle de chaîne 2xTSVs et modèle compact

Nous définissons deux lignes de masse, deux TSV et une couche de redistribution (RDL). Ils sont traités comme un modèle T. Le modèle exact est représenté sur la figure supérieure 25. La source de tension est un signal impulsionnel, avec une amplitude de 1 V, des temps de montée et de descente de 0,05ns, un rapport cyclique de 60% et une fréquence de travail de 2GHz. Ici, nous utilisons également la méthode d'analyse nodale modifiée (MNA) et le solveur de conjugué généralisé (GCR). Afin de vérifier la robustesse de la méthode, la même simulation est effectuée dans ADS. Le signal est représenté sur la figure (a), la comparaison du signal de sortie avec ADS est représentée sur la figure (b) et la figure (c) montre l'erreur relative de la méthode MNA + GCR

et de l'ADS. Comme nous pouvons le voir sur la figure (c), notre méthode MNA + GCR a une très bonne précision par rapport à l'ADS, l'erreur maximale est d'environ 1,6%.



(a) (b) (c)

Figure B31 (a) Source de tension d'entrée (b) Comparaison de sortie entre MNA et ADS (c) Erreur relative entre MNA et ADS pour le modèle de chaîne 2xTSVs

De la figure ci-dessus, nous pouvons découvrir que la méthode MNA + GCR a la précision de sauvegarde avec simulateur ADS, et il peut être intégré avec l'extracteur 3D-TLE sans aucune difficulté. Le processus de conception général est représenté par la figure suivante.

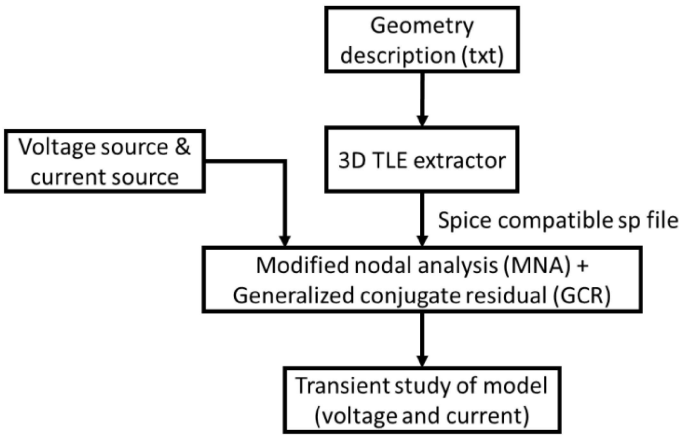


Figure B32 notre flux de travail pour la conception d'appareils 3D

B.7.1.3) Electro-thermal modeling of VLS circuits

Le problème électrothermique couplé est résolu dans une approche de relaxation classique: le problème thermique est d'abord résolu à température ambiante, obtenant la distribution de T. Puis les résistances électriques R (T) sont mises à jour et le circuit électrique est résolu, obtenant la tension drop distribution. Après la mise à jour des sources thermiques P_s (i), le problème thermique est à nouveau résolu, et ainsi de suite. En établissant la convergence entre les problèmes, les distributions finales de température et de chute de tension sont obtenues.

Une analyse dynamique est ensuite effectuée (à la température donnée par la solution du modèle électrothermique statique précédent) pour étudier plus en détail: (i) les effets de la chute de tension supplémentaire due aux éléments dynamiques; (ii) si le niveau de puissance thermique supplémentaire dans la structure est toujours compatible avec l'équilibre thermique statique supposé. Il est réalisé via une approche classique d'analyse de domaine fréquentiel, en considérant le circuit d'impédances correspondant à une fréquence donnée.

Cette approche est basée sur deux faits fondamentaux: (i) en raison de la linéarité du (sous-) modèle électrique, la superposition s'applique aux tensions et aux courants évalués à différentes fréquences (y compris DC); (ii) les puissances moyennes électriques calculées à différentes fréquences peuvent être additionnées, en raison de leur "orthogonalité". En réglant correctement la gamme de fréquences d'intérêt pour le cas considéré, une analyse de fréquence exhaustive est facilement réalisée, à un temps de calcul abordable.

Enfin, on peut noter qu'une analyse dynamique électrothermique totalement cohérente, si nécessaire, peut être poursuivie dans les mêmes hypothèses de modélisation, en exploitant la linéarité de chaque (sous-) modèle, dans un nouveau cycle de relaxation, où le DC et La contribution AC à la puissance thermique moyenne est prise en compte en même temps.

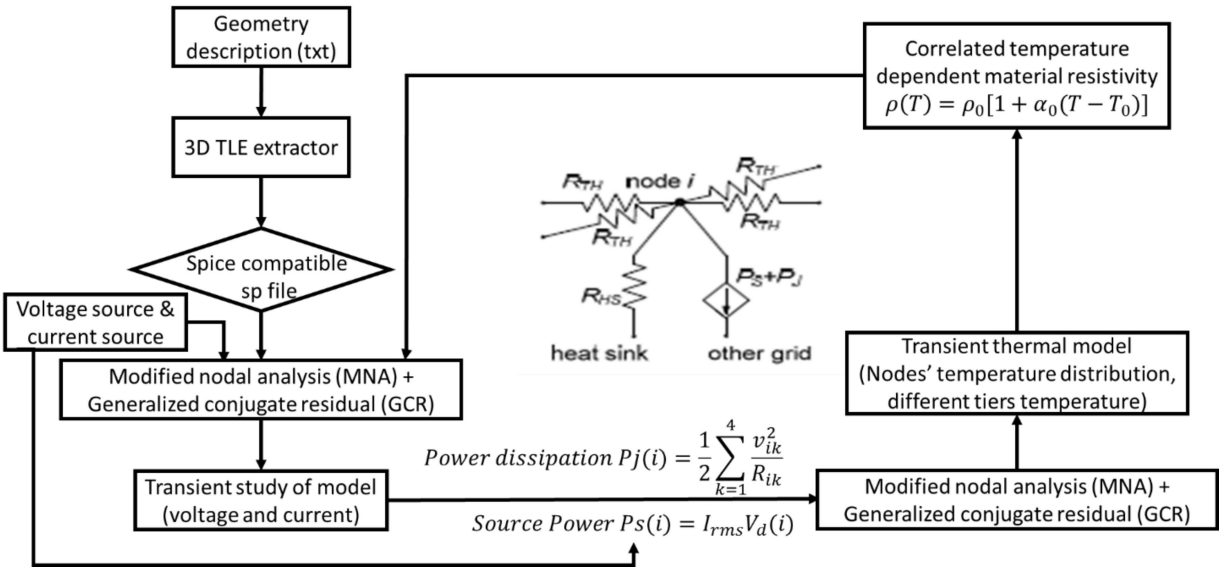


Figure B33 Flux de couplage électro-thermique 3D IC

L'analyse en puissance est basée sur une analyse transitoire qui dérive la distribution de la chute de tension pour chaque niveau où une chute excessive entraîne des températures élevées sur les pistes métalliques. L'augmentation de la température est appliquée pour mettre à jour les modèles thermiques pour l'étape d'analyse thermique. L'analyse thermique est basée sur l'analyse statique 1-D et fournit la distribution de la température pour chaque niveau et TSV, où les températures élevées modifient la résistivité des conducteurs et sont incluses dans l'étape d'analyse de puissance.

Les changements de résistivité et de température se traduisent par un processus itératif, qui converge lorsqu'il n'y a plus de changement de tension et de distribution de température. Veuillez noter que l'analyse thermique est basée sur une analyse thermique en régime permanent pour capturer la distribution de température sur chaque niveau pour un profil de puissance donné. Il est limité à capturer la distribution thermique dynamique à des profils de puissance variables. Cependant, comme nous visons à capturer rapidement et avec précision la distribution de température sur chaque niveau pour un profil de puissance donné, l'analyse thermique 1-D est une approche viable. Nous utilisons des modèles mathématiques tels que décrits dans la partie précédente et des méthodes avancées d'analyse numérique pour réaliser des analyses efficaces de réseaux puissance / sol et thermique.

B.8) Simulation de micro-caloduc

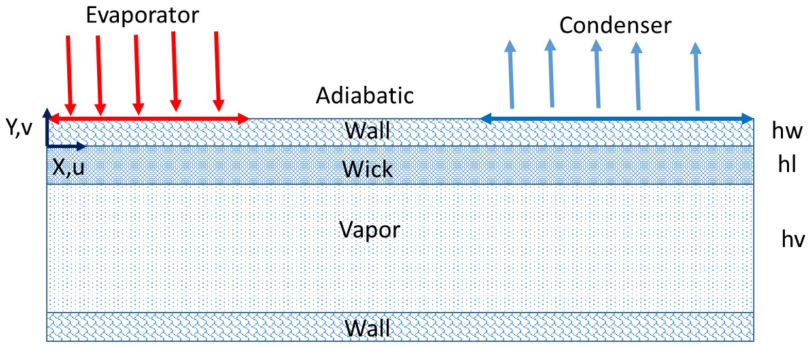
Les caloducs plats micro / nano sont une technologie de transfert de chaleur passive efficace dans le refroidissement du flux thermique élevé dans les appareils électroniques tels que les puces informatiques, en raison de leur conductivité thermique élevée, de leur fiabilité et de leur faible poids. Un caloduc plat est une chambre fermée dont la surface interne est recouverte d'une structure de mèche capillaire, le volume restant contenant la vapeur. Les sources de chaleur et les puits de chaleur sont situés sur la chambre, les autres parties étant isolées thermiquement. Le fluide de travail est vaporisé par la source de chaleur au niveau de l'évaporateur, et la différence de pression générée conduit la vapeur de l'évaporateur au condenseur, où elle se condense et pénètre dans les structures de mèche. La pression capillaire dans la mèche refoule le liquide condensé vers l'évaporateur où il est vaporisé. Cette circulation de changement de phase interne continuera tant que le passage d'écoulement n'est pas bloqué et qu'une pression capillaire suffisante est maintenue [230]. Pour le refroidissement des appareils électroniques, les fluides de travail les plus couramment utilisés sont l'eau, l'acétone, l'éthanol ou le méthanol [215], [218], [220], [226], [228], [230], [234], [238], [239], [264]

Des investigations sur les caloducs plats ont été menées pour caractériser les performances thermiques et hydrodynamiques des micro-caloducs utilisés pour le refroidissement de l'électronique. Pour prédire les caractéristiques thermiques des caloducs, de nombreux chercheurs ont proposé des modèles théoriques simplifiés unidimensionnels [201], [216], [234], [236], [238].

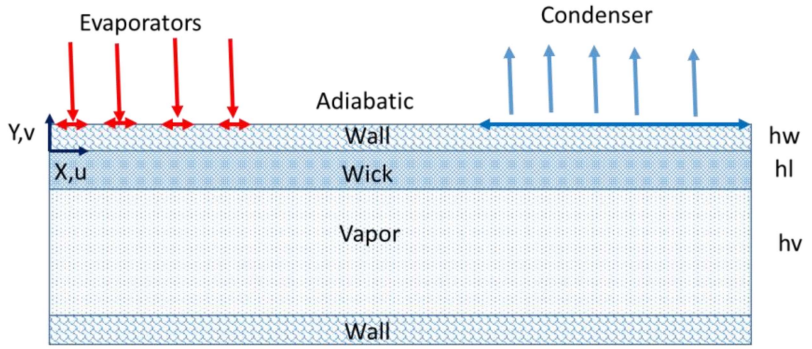
Dans le travail actuel, un modèle de chambre à vapeur à faible coût est développé, ciblant les géométries et les conditions de fonctionnement typiques des applications de gestion thermique. Le modèle prend en compte le transport de masse, de quantité de mouvement et d'énergie dans la paroi de la chambre de vapeur, la mèche et le noyau de vapeur, ainsi que le changement de phase à l'interface vapeur-vapeur. [229]

Les configurations proposées des caloducs plats, constitués de la paroi, des mèches poreuses saturées de fluide de travail et de l'espace vapeur, sont illustrées à la Figure B34. La Figure B34a, b, c présente les quatre configurations de caloducs plats avec un seul source de chaleur, plusieurs

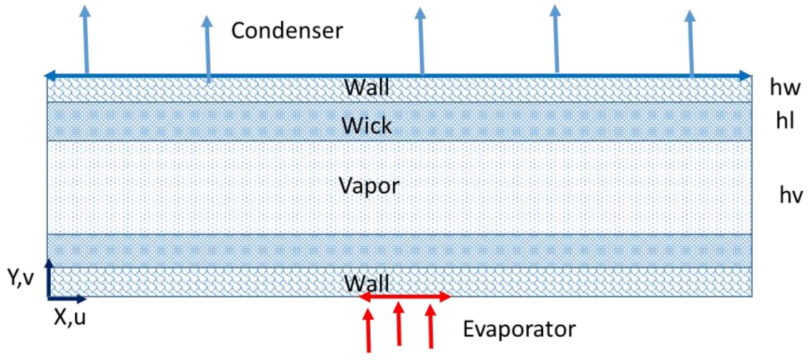
sources de chaleur, une source de chaleur au fond et un dissipateur de chaleur sur le dessus du caloduc, et de multiples sources de chaleur avec des conditions aux limites symétriques, respectivement. Les hypothèses sous-jacentes sont: température de paroi bidimensionnelle et flux de vapeur, à l'équilibre, écoulement incompressible et laminaire, mèche saturée, propriétés de matériau constantes, température de saturation constante et profil de température linéaire à travers la structure de mèche fine.



(a) Configuration I



(b) Configuration II



(c) Configuration III

Figure B34 Caloduc plat avec différentes configurations de chauffage / refroidissement: a) configuration I, source de chaleur unique et évier en haut; b) configuration II, sources de chaleur multiples et puits en haut; c) configuration III, source de chaleur au fond et dissipateur de chaleur au sommet.

Le diagramme schématique des géométries simulées est représenté sur la Figure B34.

Les propriétés du fluide de travail, du cuivre et des matériaux de mèche poreuse utilisés dans les simulations de la chambre à noyau de vapeur sont présentées dans le tableau 14 suivant. Les propriétés de la vapeur sont montrées à une température de 40 °C.

Table 4 Properties of the working fluid, copper and porous wick materials used in the heat pipe simulations.

PROPERTY	*VALUE*
Copper density(ρ_{wall})	8978kg/m^3
Water liquid density(ρ_{water})	992.3kg/m^3
Water vapor density(ρ_v)	0.05122kg/m^3
Copper thermal conductivity(k_{wall})	400W/mK
Wick effective thermal conductivity(k_{wick})	1.3W/mK
Water vapor thermal conductivity(k_v)	0.05W/mK
Copper specific heat capacity(C_p)	381 J/kgK
Water liquid specific heat capacity(C_p)	4182 J/kgK
Water vapor specific heat capacity(C_p)	1889 J/kgK
Water liquid viscosity(μ_l)	0.00065 Pa*s
Water vapor viscosity(μ_v)	0.0000096 Pa*s
Enthalpy of vaporization(h_{fg})	2473 kJ/kg
Specific gas constant(R_const)	8.3145 J/molK
Water vapor mean molar mass(M_n)	0.018015 kg/mol
Wick porosity(φ)	0.5
Wick permeability(K)	1*10^{-11} m^2

Les champs de température prédits par les approches de modélisation sont présentés à la Figure B35. La Figure B35 (a) montre la comparaison du profil de température le long de la direction x de la source de chaleur 50W entre COMSOL et la publication Maziar Agnvami [215]. Figure B35b montre le profil de température simulé COMSOL avec une source de chaleur de 30W, 40W et 50W. Le profil de température a une température maximale du côté de l'évaporation dans la surface supérieure et une température minimale du côté du condenseur. Les graphiques révèlent une correspondance de haute précision entre COMSOL et la solution théorique. L'erreur maximale est d'environ 6% pour la configuration I et de 0,075% pour la configuration II. D'après les Figure B35 (b) et (d), nous pouvons voir qu'en augmentant de 10W à la source de chaleur, la température gagne environ 3K pour la configuration I, et 4K pour la configuration II.

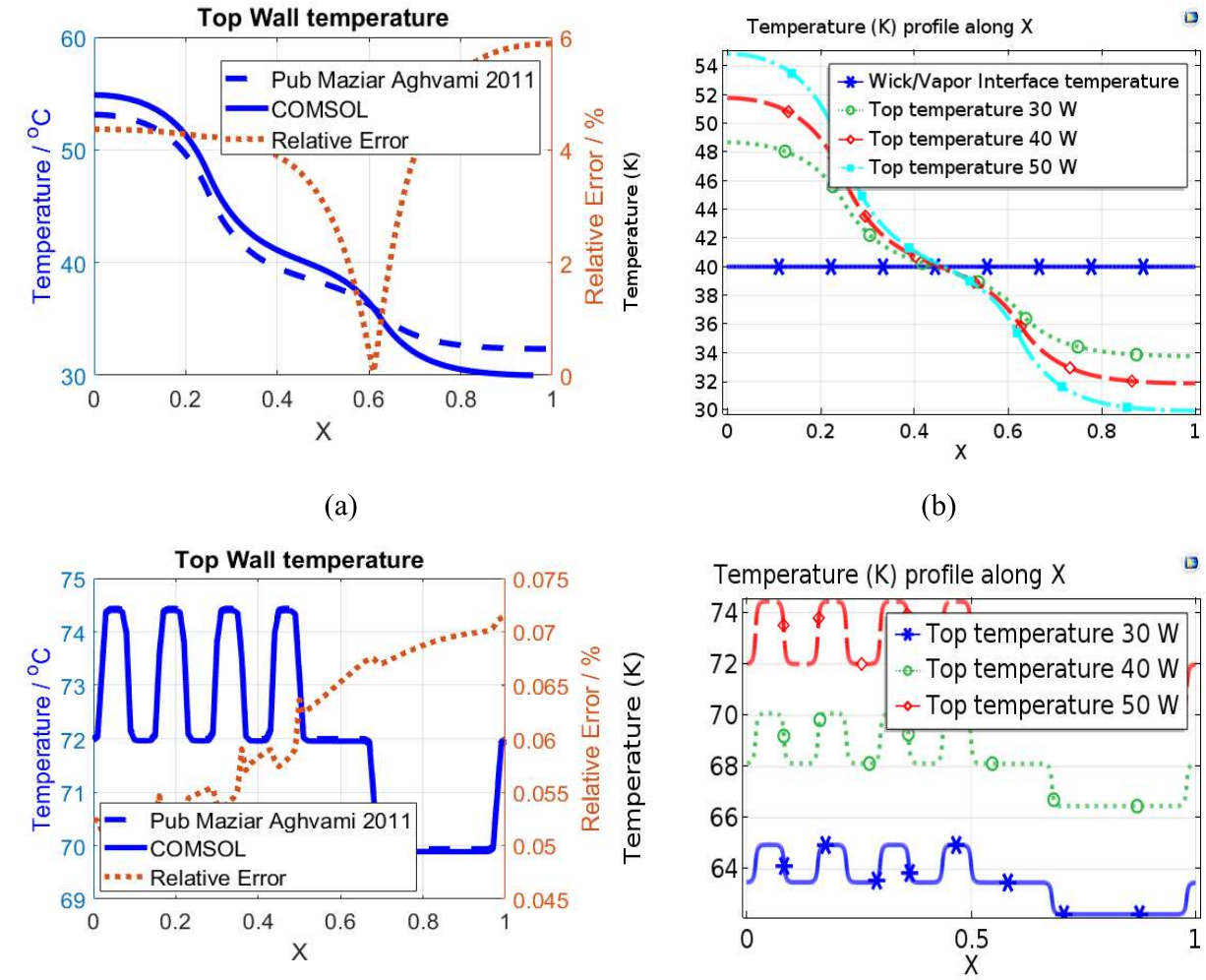


Figure B35 Comparaison du profil de température (a) entre COMSOL et pub avec source de chaleur 50W [200] en configuration Matlab I (b) paramétrisation de puissance en configuration COMSOL I (c) comparaison COMSOL et pub avec source de chaleur 50W [200] en configuration Matlab II (d) paramétrage de la puissance dans la configuration COMSOL II

La Figure B36 compare les vitesses au centre de la chambre de vapeur.

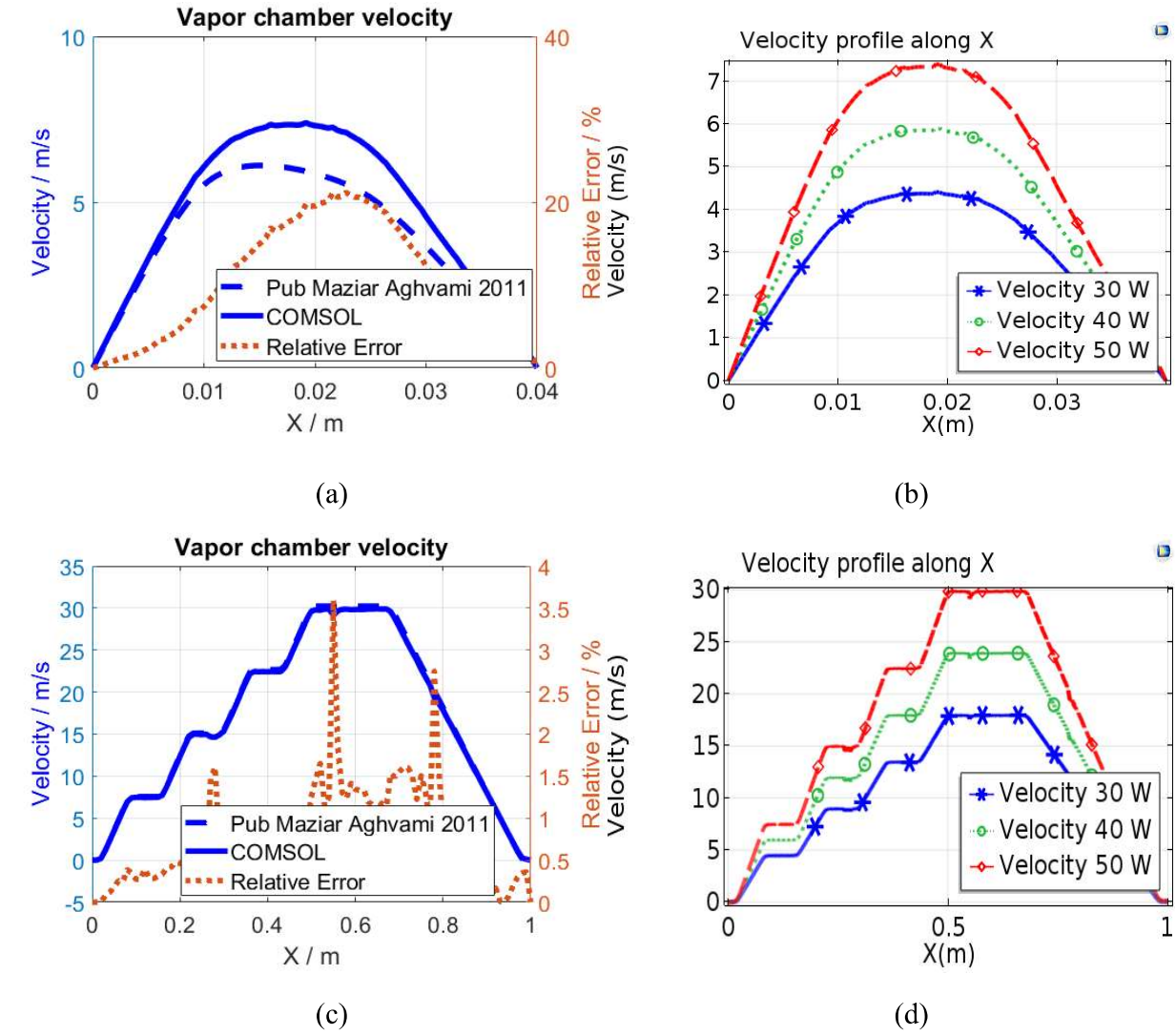


Figure B36 Vélocités au centre de la chambre de vapeur (a) Comparaison entre COMSOL et pub avec source de chaleur 50W [200] en configuration Matlab I (b) paramétrisation de la puissance en configuration COMSOL I (c) comparaison COMSOL et pub avec source de chaleur 50W [200] dans la configuration Matlab II (d) paramétrisation de la puissance dans la configuration COMSOL II

Comme on peut le voir sur la Figure B36, la vapeur a une vitesse maximale au centre du noyau de vapeur et se réduit à 0 lorsqu'elle attache la paroi. Et pour le modèle COMSOL, la vitesse maximale est d'environ 7m / s, c'est presque la même chose que les vélocités du papier [215]. Pour la configuration I, il y a environ 20% de différence entre la solution analytique et COMSOL, en particulier pour la solution analytique, la vitesse de la configuration I a une forme non-symétrique. Mais pour la configuration II, la différence de vitesse est inférieure à 4%. Et en augmentant 10W de la source de chaleur, la vitesse gagne environ 1,5m / s pour la configuration I et 6m / s pour la configuration II.

Et enfin, la partie la plus importante du caloduc est la pression capillaire dans l'interface vapeur / mèche. La Figure B37 montre la pression capillaire à l'interface mèche / vapeur. Du côté de l'évaporation, l'eau est évaporée et la vapeur présente un gain de pression maximal de ce côté, mais du côté du condenseur, l'eau se condense et provoque l'écoulement de l'eau dans la mèche, ce qui nous permet de voir un processus contraire. La mèche présente un débit massique du côté de la condensation et une masse s'écoule du côté de l'évaporation, de sorte que l'eau s'écoule du côté de la condensation vers le côté d'évaporation, mais avec une vitesse beaucoup plus lente que le noyau de vapeur. Et à partir de la figure 6, nous pouvons voir que les pressions capillaires de la configuration I de la simulation et de la publication COMSOL [215] ont une différence maximale de 20%. Mais pour la configuration II, les pressions capillaires sont presque les mêmes. Et l'erreur est inférieure à 0,5%

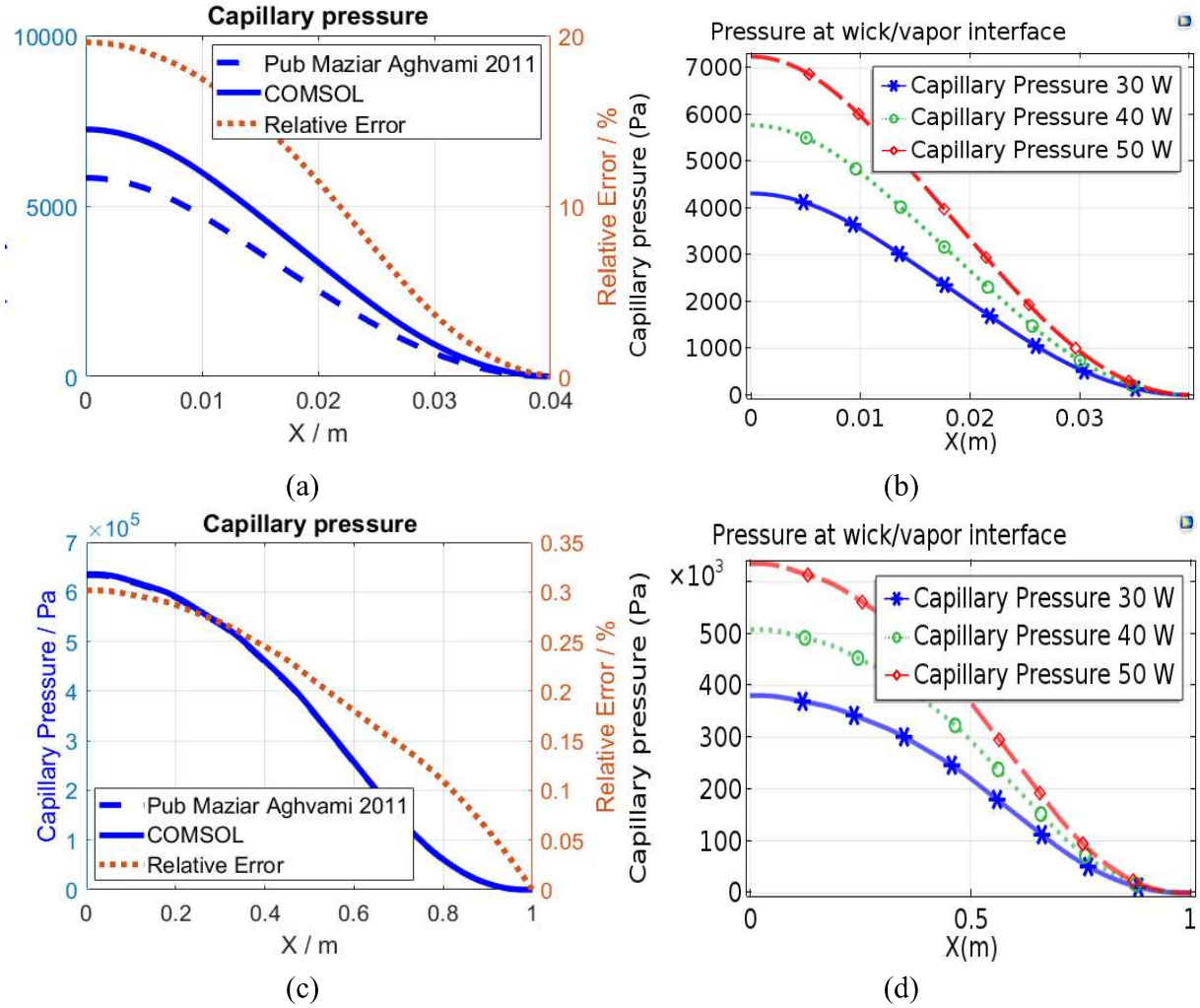


Figure B37 Pression capillaire à l'interface mèche / vapeur (a) comparaison entre COMSOL et pub avec source de chaleur 50W [215]en configuration Matlab I (b) paramétrisation de puissance en configuration COMSOL I (c) comparaison entre COMSOL et pub avec source de chaleur 50W [215] configuration II (d) paramétrisation de la puissance dans COMSOL dans la configuration Matlab II

Un modèle pour le fonctionnement de la chambre à vapeur a été développé qui permet de multiples entrées de chaleur de forme arbitraire sur la face de l'évaporateur; le modèle prédit les champs 2D de la température, de la pression et de la vitesse dans la chambre à vapeur, sous réserve d'hypothèses concernant la taille de la chambre à vapeur, le débit de liquide et de vapeur et les propriétés du matériau. Les équations régissant la masse, le momentum et l'énergie dans les domaines de la paroi, de la mèche et de la vapeur ont été établies. Le modèle est comparé à un modèle numérique [215].

B.9) Electrical and thermo-mechanical noise impacts of through-silicon via (TSV) on transistor

Du point de vue de l'aspect électrique, on s'intéresse aux bruits de substrat induits par les TSVs qui menacent la performance des transistors voisins en raison de chemins parasites entre TSV et transistor [253]. Du point de vue thermomécanique, en raison de l'inadéquation inhérente du coefficient de dilatation thermique (CTE) entre le métal et le silicium, des contraintes thermomécaniques apparaîtront au voisinage de TSV, lorsque le système se refroidit à partir de la température maximale localisée possible à la température ambiante [254]. La mobilité des porteurs des transistors voisins serait influencée par la contrainte thermomécanique induite par les TSV due à l'effet piézorésistif [257]. Certains articles portent sur l'impact électrique et l'impact thermo-mécanique du TSV sur le transistor [24], [99], [258], [259]. En effet, les transistors au voisinage de TSV sont simultanément affectés à la fois par les bruits de couplage et par les contraintes thermomécaniques. Il n'y a pas eu de rapport sur l'effet de croisement de ces deux aspects. Nous étudions la combinaison des impacts électriques et thermo-mécaniques de TSV sur le courant de saturation du transistor en prenant un NMOSFET, par exemple [195]–[203]. La méthode d'étude est également appropriée pour le PMOSFET.

B.9.1) Investigation method of electrical noise

Le courant de saturation peut être affecté par le bruit induit par TSV à travers l'effet du bulk. Le courant de saturation I_{dsat} de NMOSFET peut être calculé par

$$I_{dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \qquad \text{(B-13)}$$

Où V_{GS}représente la différence de tension entre la porte et la source du NMOSFET; W et L sont la largeur et la longueur de la porte, respectivement; Cox est la capacité entre la porte et le canal porteur; μ_n est la mobilité des électrons; la tension de seuil V_{th} peut être liée à la tension du bulk V_B[261]

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\Phi_F - V_{BS}} + \sqrt{2\Phi_F}\right) \approx V_{th0} - \frac{\gamma}{2\sqrt{2\Phi_F}} V_{BS} \quad \text{(B-14)}$$

Où V_{th0} est la tension de seuil du bulk; γ représente le paramètre d'effet de corps; et $2\Phi_F$ représente le paramètre de potentiel de surface. V_{BS} est la tension du corps.

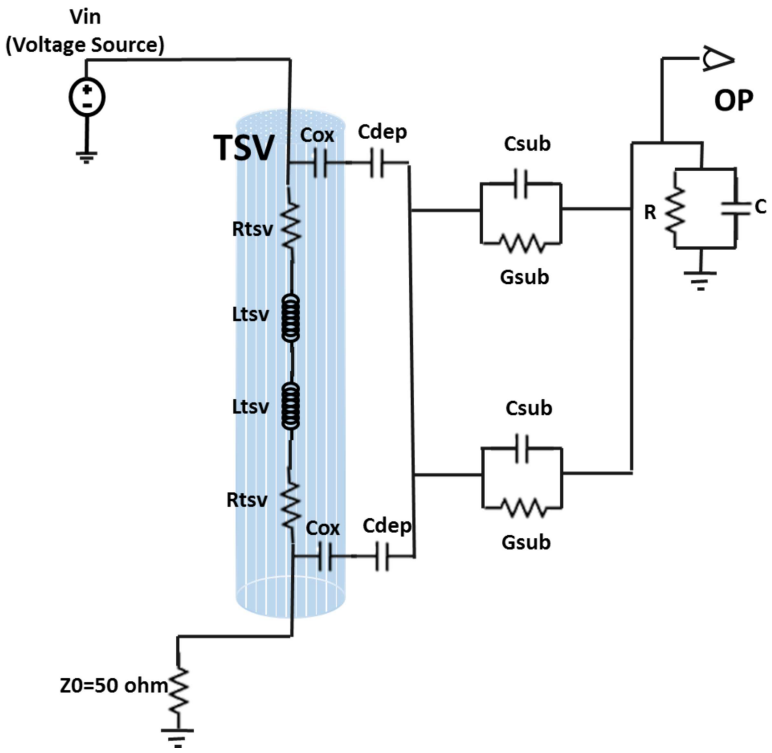


Figure B38 Equivalent circuit model and simulation setup of TSV-to-device noise

En utilisant les 2 équations (B-13) et (B-14), la variation du courant de saturation peut être exprimée comme suit:

$$\Delta I_{sat} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \frac{\gamma}{2\sqrt{2\Phi_F}} V_{BS} \quad \text{(B-15)}$$

$$\frac{\Delta I_{sat}}{I_{sat}} = \frac{\gamma (V_{GS} - V_{th})}{\sqrt{2\Phi_F}(V_{GS} - V_{th})^2} V_{BS} \quad \text{(B-16)}$$

Sans le bruit de tension de couplage, la tension du corps serait nulle. Par conséquent, le bruit peut entraîner la variation du courant de saturation.

Afin d'obtenir la tension du corps de bruit V_{BS}, MNA (analyse nodale modifiée) est employée en utilisant le modèle de circuit équivalent montré sur la figure précédente. Comme indiqué dans le deuxième chapitre, la résistance TSV Rtsv est calculée par

$$R_{TSV} = \sqrt{\left(\frac{\rho_{TSV} h}{\pi R_m^2}\right)^2 + \left(\frac{h}{\pi \sigma_{TSV} \delta (2R_m - \delta)}\right)^2} \quad \text{(B-17)}$$

Où

$$\delta = \sqrt{\frac{\rho_{TSV}}{\pi \mu_{TSV} f}} \quad \text{(B-18)}$$

δ est la profondeur de la peau; f est la fréquence; ρ_{TSV}, h, R_m and σ_{TSV} sont la résistance, la hauteur, le rayon et la conductance de TSV; L'inductance TSV L_{TSV} est exprimée en

$$L_{TSV} = \frac{\mu_0 h}{2\pi}\left[\ln\left(\frac{h+\sqrt{h^2+R_m^2}}{R_m}\right) + R_m - \sqrt{h^2+R_m^2}\right] \quad \text{(B-19)}$$

La capacité de revêtement d'oxyde Cox, et la capacité d'appauvrissement induite par l'effet MOS Cdep sont calculées par

$$C_{ox} = \frac{2\pi\varepsilon_{ox} h}{\ln(\frac{R_m+t_{ox}}{R_m})} \quad \text{(B-20)}$$

$$C_{dep} = \frac{2\pi\varepsilon_{si} h}{\ln(\frac{R_m+t_{ox}+w_{dep}}{R_m+t_{ox}})} \quad \text{(B-21)}$$

$$w_{dep} = \sqrt{\frac{4\varepsilon_{si} kT}{q^2 N_a}\ln(\frac{N_a}{n_i})} \quad \text{(B-22)}$$

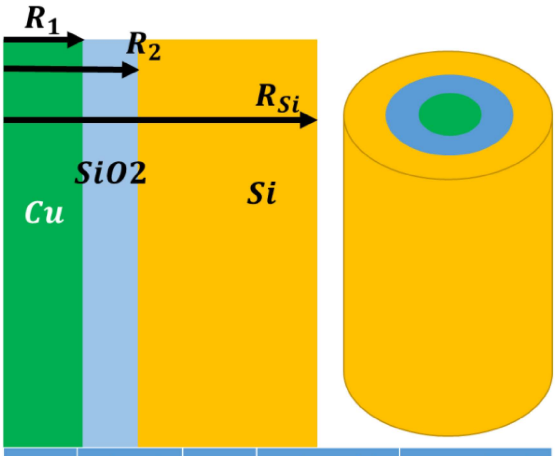
B.9.1.1) Investigations method of thermo-mechanical noise impact

La contrainte thermomécanique induite par le TSV apparaît dans le substrat de silicium environnant en raison du décalage de CTE entre le métal de TSV et le silicium, lorsque la structure est soumise à une rampe thermique dans le flux de processus. Le courant de saturation des transistors peut être affecté négativement par la contrainte thermomécanique induite par le TSV, puisque la mobilité du porteur est modifiée en raison de l'effet piézorésistif.

Le travail [99][24] a étudié les impacts du stress thermo-mécanique induit par le TSV sur la mobilité des porteurs. Ici, nous décrivons des informations simples mais suffisamment à jour pour la méthode d'estimation de l'impact thermomécanique de TSV. Le changement de courant de saturation $\Delta I_{sat}/I_{sat}$ peut être estimé par [197]

$$\frac{\Delta I_{sat}}{I_{sat}} \approx \frac{\Delta\mu}{\mu}(r,\theta) = \Pi \times \sigma_{rr}^{si}(r) \times \beta(\theta) \quad \text{(B-23)}$$

Où σ_{rr}^{si} est la contrainte radiale induite par le TSV; μ est la mobilité du substrat. $\beta(\theta)$ représente le facteur d'orientation; θ est l'angle entre le canal du transistor et la contrainte radiale induite par TSV. $\theta = 0°$ and $90°$ signifient que les canaux de drain et de source du transistor sont parallèles et perpendiculaires à la contrainte radiale induite par le TSV, respectivement [24]; Π est le coefficient piezo-résistif à at $\theta = 0°$, qui agit comme une contrainte longitudinale. Pour nMOS, $\Pi = -31 \times 10^{-11} Pa^{-1}$, $\beta(0°) = 1$, $\beta(90°) = 0.5$, for pMOS, $\Pi = 71.8 \times 10^{-11} Pa^{-1}$, $\beta(0°) = 1, \beta(90°) = -0.6$.[23]



	μ(GPa)	ν	α (ppm/K)	Range(um)
Si	51	0.28	2.8	R2<r<Rsi
SiO_2	30	0.16	0.6	R1<r<R2
Cu	26	0.34	18	0<r<R1

Figure B39 Structure et paramètres du matériau de la charge TSV (Cu), de la couche isolante (SiO2) et de la plaquette (Si)

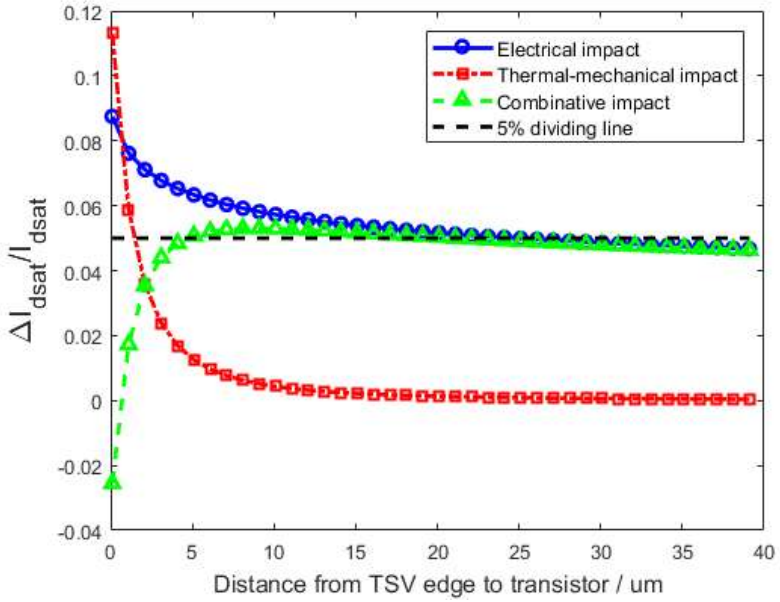
Sur la base de la méthode d'étude dans les deux sections précédentes, les changements relatifs de courant de saturation provoqués par le bruit de couplage, la contrainte thermomécanique et la combinaison des deux aspects peuvent être obtenus, comme illustré à la Figure B40(a). Selon la technologie actuelle, les paramètres utilisés dans cette simulation sont sélectionnés comme suit. La hauteur et le rayon de TSV sont 50um et 2.5um, respectivement; l'épaisseur du revêtement d'oxyde autour de TSV est de 0,1 um; la conductivité de TSV est de 5,8e7 S / m. La couche d'oxyde et le silicium ont une permittivité relative de 3,9 et 11,9, respectivement. La conductivité et la concentration de dopage du substrat de silicium de type p sont de 10 S / m et de 1,25e15 cm-3, respectivement. Ici, un nMOS 22nm est utilisé. Selon le modèle de technologie prédictive [269], la concentration de dopage corporel à la limite de la zone d'appauvrissement entre le canal et le corps dans un nœud de technologie 22 nm est de 5,5e18 cm-3, l'épaisseur de l'oxyde de grille est de 1,1 nm la température est fixée à 300K. L'effet du corps γ et le potentiel de surface 2φ_F peuvent être exprimés par

$$\gamma = \frac{tox\_nmos}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}Nsub} \quad \text{(B-24)}$$

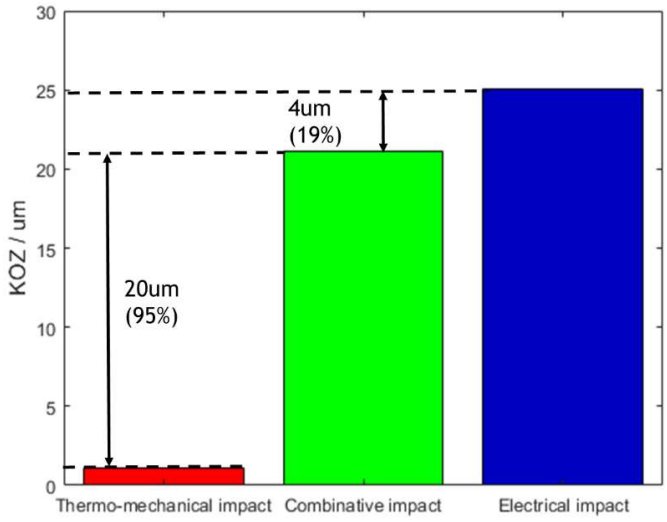
$$2\phi_F = \frac{2kT_0}{q}log(\frac{Nsub}{ni}) \quad \text{(B-25)}$$

Le coefficient piezo-résistif étant négatif pour nMOS, la contrainte thermomécanique entraîne une diminution du courant de saturation. Alors que le bruit de couplage a un impact opposé sur la variation du courant de saturation. Par conséquent, les deux aspects sont contrecarrés dans une certaine mesure. Afin de comparer clairement les deux impacts, la Figure B40 (a) donne la valeur

absolue de l'impact thermomécanique sur le courant de saturation. La Figure B40 (a) montre que, comme la distance entre le bord TSV et le transistor est inférieure à 0,5 um, la contrainte thermomécanique joue un rôle majeur dans la variation du courant de saturation. Comme la distance est supérieure à 0.5um, le bruit de couplage électrique est majeur.



(a)



(b)

Figure B40 Variation du courant de saturation avec la distance du bord TSV au transistor et (b) résultats KOZ causés par le bruit de couplage, la contrainte thermosomécanique et la combinaison des deux aspects.

La zone Keep-out (KOZ) est définie comme la région avec un changement de saturation de plus de 5% [191], [99], [196], [202]–[205], ce qui signifie la région où les périphériques ne peuvent pas être , puisque la performance du transistor est affectée. Les résultats de KOZ sont résumés dans la Figure B40 (b). Il est montré que KOZ est 25um et 1um pour l'impact électrique individuel et l'impact thermo-mécanique, respectivement. Néanmoins, KOZ devrait considérer l'impact combiné de ces deux aspects. L'erreur atteint plus de 50% si seul un choc électrique individuel ou un impact thermo-mécanique est pris en compte. Par conséquent, il est nécessaire de tenir compte des impacts électriques et thermomécaniques pour l'évaluation de KOZ.

B.10) Conclusion générale

La thèse fournit une méthode de conception globale pour la conception de circuits intégrés 3D dans le domaine électrique, thermique, électrothermique et aussi le bruit. Ci-après seront incluses des méthodes de simulation pour un seul TSV, une matrice TSV, un substrat multicouche, des multi-processeurs et une conception de dissipation thermique.

Nous présentons d'abord quelques connaissances de base sur les effets parasites électriques (effet MOS et effet de peaux) du TSV. Basé sur des effets parasites, nous avons programmé dans Matlab un extracteur de substrat qui s'appele 3D-TLE (extracteur de ligne de transmission 3D), qui peut extraire automatiquement de tous les contacts; impédance, de forme arbitraire et de matériaux arbitraires. Cet extracteur est 100% compatible avec les simulateurs de noyau SPICE, comme ADS (Advanced design system). Les données extraites sont vérifiées avec des mesures et un résultat de simulation par la méthode des éléments finis (FEM). Basé sur des effets parasites du TSV, un RF filtre de fréquence 26 GHz et bande passante de 2 GHz est proposé dans ce travail.

Le chapitre 3 propose une solution thermique analytique pour la distribution de température non stationnaire du substrat multi-couches. Dans la conception 3D IC, les problèmes thermiques sont des problèmes paralysants, en particulier lorsque nous réduisons à l'échelle nanométrique. La résistance électrique augmente avec la température, de même que la résistance du substrat. La plupart des travaux de simulation thermique sont basés sur les régimes stables; Peu de gens travaillent sur le cas non stationnaire. Les effets non stationnaires sont paralysants, comme les points chauds, qui peuvent être améliorés par des rampes de tension. Nous combinons le modèle compact thermique 1D en utilisant MNA (analyse nodale modifiée) et la méthode de volume fini 2D (FVM) pour résoudre le calcul de température IC multicouche 3D, qui, en comparaison avec la simulation 3D FEM, réduit considérablement les complexités de calcul. Cette méthode est adaptée à tout circuit intégré 3D. En outre, un cas de dissipation de la chaleur des processeurs à 4 noyaux est étudié dans ce chapitre. La dernière partie de ce chapitre présente le fonctionnement de la simulation électrothermique. Le simulateur électrothermique peut être 100% compatible avec le simulateur SPICE (similaire), et la partie électrique est vérifiée avec ADS. La méthode MNA est normalement utilisée pour la conception de 3D PDN VLSI, mais ici, nous l'appliquons dans la simulation au niveau de l'appareil, ce point est quelque peu original, à notre connaissance. Ce

travail construit le cadre d'analyse électrothermique pour le substrat, les connexions thermiques (via 3D) et le PDN 3D au niveau du système. Nous fournissons une étude approfondie des problèmes de puissance et de dissipation thermique dans l'intégration 3D en considérant plusieurs aspects tels que:

- effets de commutation à un ou plusieurs niveaux (auto-échauffement) sur la puissance 3D et la dissipation thermique;
- l'impact des TSV et du substrat sur la puissance et l'intégrité thermique et leurs implications en termes de conception;
- Influence de la conductivité thermique du dissipateur de chaleur sur les effets électrothermiques.

Nous combinons la fréquence de commutation et les effets électrothermiques ensemble. Et en comparant avec les paramètres S, nous avons découvert que les effets électrothermiques n'apparaissent que lorsque les paramètres S changent, et la réduction de la résistance thermique et l'augmentation de la concentration de dopage du substrat limiteront le problème d'intégrité du signal électrothermique.

En tant que solution à la dissipation thermique locale, le composant passif de dissipation thermique, caloduc plat (FHP) est proposé comme un composant potentiel dans le chapitre 4. Le modèle basé sur FEM (COMSOL Multiphysics) est très précis dans la simulation 2D et 3D de caloduc. Les conditions aux limites précises peuvent être trouvées dans ce chapitre; il considère le champ de pression dans le calcul, et surtout il peut extraire la pression capillaire directement du modèle, ce qui sera très utile dans l'étude future des effets capillaires de la couche de mèche.

Le chapitre 5 propose tout d'abord la solution analytique pour la distribution du bruit non stationnaire des substrats et présente des méthodes d'analyse du bruit. Et ce chapitre étudie aussi le keep-out-of-zone (KOZ) de TSV à transistor, comme nMOS et CNFET. Les méthodes d'investigation de l'impact du bruit électrique et de l'impact du bruit thermo-mécanique montrent une grande influence sur le dispositif de type nMOS (pMOS, pFET et nFET). Mais pour le CNFET, en raison de l'isolement élevé entre le nanotube de carbone et le substrat, l'effet parasitaire du TSV n'a aucune influence sur celui-ci.

En conclusion, ce travail peut, en plus de réaliser la modélisation électrique, thermique et électrothermique de simples TSV, TSV matrix et multicouches 3D IC, clarifier les contraintes de caractéristiques et les processus de bruit de couplage impliqués dans le substrat multicouche, et aussi donner les outils de conception EDA. Mais il reste beaucoup de choses à faire, et un cas réel et complexs doit être étudié.

L'extension de ce travail concernera une modélisation électro-thermique M3D (3D Monolithic), qui permet de réaliser directement une conception de niveau nanométrique (un inverseur CMOS peut être obtenu à l'échelle nanométrique par connexion d'un pMOS et nMOS avec un M3D). Et

plus de dispositifs RF peuvent être générés en utilisant la technologie TSV ou M3D à l'échelle micro et nanométrique, par exemple, antenne micro RF avec TSV, coupleur thermique à base de TSV, cellule logique basée sur TSV ou M3D et autres capteurs 3D.

Récemment, la recherche de 3D IC s'est étendue à la conception optique-électrique. L'un des futurs intérêts de recherche sera le co-design EDA de l'optique-électronique. Mais ce sera un peu inutile, car dans l'application optique, le substrat et le milieu de transmission sont toujours du verre, et dans ce cas, les effets parasites électriques sont toujours négligeables, à l'échelle microscopique. Mais en vue de la haute fréquence, les circutis optiques ont beaucoup de problèmes thermiques. Donc les effects opto-electrique-thermiques doivent être considéré ensemble.

L'un des sujets brûlants dans la recherche est la puce neuromorphique. Le calcul basé sur le cerveau et basé sur les pointes dans les systèmes électroniques est étudié pour le développement de technologies informatiques alternatives non conventionnelles. La puce AI, c'est la meilleure façon d'intégrer l'algorithme d'apprentissage avec la conception matérielle. Le cadre d'ingénierie neurale fournit une méthode de programmation de ces dispositifs pour mettre en œuvre le calcul. [276] La partie la plus intéressante pour la conception 3D IC est que si nous pouvons implémenter une puce VLSI multi-neurones neuromorphique analogique / numérique à signaux mixtes dans une puce 3D et imiter la structure cérébrale, nous aurons une meilleure compréhension du système d'apprentissage humain.

Reference

[1] E. P. Debenedictis, M. Badaroglu, A. Chen, T. M. Conte, and P. Gargini, "Sustaining Moore's Law with 3D Chips," *Computer (Long. Beach. Calif).*, vol. 50, no. 8, pp. 69–73, 2017.

[2] P. Gargini, "IRDS 2017," 2017.

[3] P. A. Gargini, "How to Successfully Overcome Inflection Points, or Long Live Moore's Law," *Comput. Sci. Eng.*, vol. 19, no. 2, pp. 51–62, 2017.

[4] ITRS, "International Technology Roadmap for Semiconductors 2.0 2015 Edition Heterogeneous Integration," pp. 1–92, 2015.

[5] AMD, "High-Bandwidth Memory (HBM) reinventing memory technology industry standards On-die GPUs," 2015.

[6] D. U. Lee, K. W. Kim, K. W. Kim, H. Kim, J. Y. Kim, Y. J. Park, J. H. Kim, D. S. Kim, H. B. Park, J. W. Shin, J. H. Cho, K. H. Kwon, M. J. Kim, J. Lee, K. W. Park, B. Chung, and S. Hong, "25.2 A 1.2V 8Gb 8-channel 128GB/s high-bandwidth memory (HBM) stacked DRAM with effective microbump I/O test methods using 29nm process and TSV," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 432–433.

[7] M. B. and J. Xu, "Interconnect-Aware Device Targeting from PPA Perspective," *IEEE/ACM Int'l Conf. Comput. Des. (ICCAD 16)*, 2016.

[8] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, 2010.

[9] K.-S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Lin, C.-C. Cheng, C.-C. Chen, Y.-J. Wei, Y.-F. Hou, M.-H. Liao, M.-H. Lee, M.-C. Chen, J.-M. Sheih, W.-K. Yeh, F.-L. Yang, S. Salahuddin, and C. Hu, "Sub-60mV-Swing Negative-Capacitance {FinFET} without Hysteresis," *IEEE Int. Electron Devices Meet.*, pp. 22.6.1–22.6.4, 2015.

[10] K. Ashraf, S. Smith, and S. Salahuddin, "Electric field induced magnetic switching at room temperature: Switching speed, device scaling and switching energy," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 601–604, 2012.

[11] M. M. Shulaker, G. Hills, N. Patil, H. Wei, H. Y. Chen, H. S. P. Wong, and S. Mitra, "Carbon nanotube computer," *Nature*, vol. 501, no. 7468, pp. 526–530, 2013.

[12] D. E. Nikonov and I. A. Young, "Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, no. c, pp. 3–11, 2015.

[13] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submieroraeter interconnect performance and systems-on-chip integration

and systems-on-chlp integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–632, 2001.

[14] S. Jung, Y. Rah, T. Ha, H. Park, C. Chang, S. Lee, J. Yun, W. Cho, H. Lim, J. Park, J. Jeong, B. Son, J. Jang, B. Choi, H. Cho, and K. Kim, "Highly Cost Effective and High Performance 65nm S 3 (Stacked Single-crystal Si) SRAM Technology with 25F 2 , 0.16um 2 Cell and Doubly Stacked SSTFT Cell Transistors for Ultra High Density and High Speed Applications," vol. 3, pp. 2004–2005, 2005.

[15] P. Ramm, A. Klumpp, J. Weber, and M. M. V. Taklo, "3D System-on-Chip technologies for More than Moore systems," *Microsyst. Technol.*, vol. 16, no. 7, pp. 1051–1055, 2010.

[16] M. J. Wolf, K. Zoschke, A. Klumpp, R. Wieland, M. Klein, L. Nebrich, A. Heinig, I. Limansyah, W. Weber, O. Ehrmann, and H. Reichl, "3D integration of image sensor SiP using TSV silicon interposer," *Proc. Electron. Packag. Technol. Conf. EPTC*, pp. 795–800, 2009.

[17] I. Limansyah, M. J. Wolf, A. Klumpp, K. Zoschke, R. Wieland, M. Klein, H. Oppermann, L. Nebrich, A. Heinig, A. Pechlaner, H. Reichl, and W. Weber, "3D image sensor SiP with TSV silicon interposer," *Proc. - Electron. Components Technol. Conf.*, pp. 1430–1436, 2009.

[18] M. Motoyoshi and M. Koyanagi, "3D-LSI technology for image sensor," *J. Instrum.*, vol. 4, no. 3, 2009.

[19] J. Charbonnier, D. Henry, F. Jacquet, B. Aventurier, G. Enyedi, N. Bouzaida, V. Lapras, and N. Sillon, "Wafer Level Packaging Technology Development for CMOS Image Sensors Using Through Silicon Vias M1 pad on front side," *IEEE Electron. Syst. Integr. Technol. Conf.*, pp. 141–148, 2008.

[20] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, "Electrical modeling and characterization of through silicon via for three-dimensional ICs," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 256–262, 2010.

[21] G. Katti, M. Stucchi, J. Van Olmen, K. De Meyer, and W. Dehaene, "Through-silicon-via capacitance reduction technique to benefit 3-D IC performance," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 549–551, 2010.

[22] J. Yook, J. C. Kim, S. Park, J. Ryu, and J. C. Park, "High D ensity and Low-cost Silicon Interposer using Thin-film and Organic Lamination Processes," vol. 2, pp. 274–278, 2012.

[23] F. Wang, Z. Zhu, Y. Yang, X. Yin, X. Liu, and R. Ding, "An effective approach of reducing the keep-out-zone induced by coaxial through-silicon-via," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2928–2934, 2014.

[24] X. Yin, Z. Zhu, Y. Yang, and R. Ding, "Metal Proportion Optimization of Annular Through-Silicon via Considering Temperature and Keep-Out Zone," *IEEE Trans. COMPONENTS, Packag. Manuf. Technol.*, vol. 5, no. 8, pp. 1093–1099, 2015.

[25] K. Chang, A. Koneru, K. Chakrabarty, and S. K. Lim, "Design Automation and Testing of Monolithic 3D ICs : Opportunities , Challenges , and Solutions," no. 1, pp. 805–810, 2017.

[26] S. Kannan, R. Agarwal, A. Bousquet, G. Aluri, and H. S. Chang, "Device performance analysis on 20nm technology thin wafers in a 3D package," *IEEE Int. Reliab. Phys. Symp. Proc.*, vol. 2015-May, pp. 4C41–4C45, 2015.

[27] A. Koneru, S. Kannan, and K. Chakrabarty, "Impact of Electrostatic Coupling and Wafer-Bonding Defects on Delay Testing of Monolithic 3D Integrated Circuits," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 13, no. 4, pp. 1–23, 2017.

[28] Y. Yang, C. Wang, N. Yu, and F. Wang, "Combination of electrical and thermo-mechanical impacts of through-silicon via (TSV) on transistor," in *Proceedings of the 2017 19th International Conference on Electromagnetics in Advanced Applications, ICEAA 2017*, 2017, no. 3, pp. 881–884.

[29] P. Batude, T. Ernst, J. Arcamone, G. Arndt, P. Coudrain, and P. E. Gaillardon, "3-D sequential integration: A key enabling technology for heterogeneous Co-integration of new function with CMOS," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 2, no. 4, pp. 714–722, 2012.

[30] A. Topol, D. C. La Tulipe, L. Shi, S. M. Alam, D. J. Frank, S. E. Steen, J. Vichiconti, D. Posillico, M. Cobb, S. Medd, J. Patel, S. Goma, D. DiMilia, M. T. Robson, E. Duch, M. Farinelli, C. Wang, R. A. Conti, D. M. Canaperi, L. Deligianni, A. Kumar, K. T. Kwietniak, C. D'Emic, J. Ott, A. M. Young, K. W. Guarini, and M. Ieong, "Enabling SOI-based assembly technology for three-dimensional (3d) integrated circuits (ICs)," *IEEE Int. Devices Meet. 2005. IEDM Tech. Dig.*, pp. 352–355, 2005.

[31] P. R. Philip Garrou, Christopher Bower, *Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits*. 2008.

[32] H. An, M. A. Ehsan, Z. Zhou, and Y. Yi, "Electrical Modeling and Analysis of 3D Neuromorphic IC with Monolithic Inter-tier Vias," pp. 87–90, 2016.

[33] K. Chang, S. Das, S. Sinha, B. Cline, G. Yerie, and S. K. Lim, "Frequency and Time Domain Analysis of Power Delivery Network for Monolithic 3D ICs."

[34] S. H. Tseng, C. Y. Yeh, A. Y. Chang, Y. J. Wang, P. C. Chen, H. H. Tsai, and Y. Z. Juang, "A Monolithic Three-Axis Accelerometer with Wafer-Level Package by CMOS MEMS Process," *Proceedings*, vol. 1, no. 4, p. 337, 2017.

[35] S. Du, "Design of High Efficiency Monolithic CMOS Class-E Power Amplifier for WLAN Application," 2017.

[36] K. Chang, B. W. Ku, S. Sinha, and S. K. Lim, "Full-chip Monolithic 3D IC Design and Power Performance Analysis with ASAP7 Library," pp. 991–996, 2017.

[37] P. Batude, M. Vinet, A. Pouydebasque, C. Le Royer, B. Previtali, C. Tabone, J. M. Hartmann, L. Sanchez, L. Baud, V. Carron, A. Toffoli, F. Allain, V. Mazzocchi, D. Lafond, S. Deleonibus, and O. Faynot, "3D monolithic integration," *Proc. - IEEE Int. Symp. Circuits Syst.*, pp. 2233–2236, 2011.

[38] S. a. Panth, K. Samadi, Y. Du, and S. K. Lim, "Design and CAD methodologies for low power gate-level monolithic 3D ICs," *Proc. 2014 Int. Symp. Low power Electron. Des. -*

ISLPED '14, vol. 1, pp. 171–176, 2014.

[39] B. W. Ku, P. Debacker, D. Milojevic, and P. Raghavan, "Physical Design Solutions to Tackle FEOL / BEOL Degradation in Gate-level Monolithic 3D ICs," pp. 1–6, 2016.

[40] S. Panth, K. Samadi, Y. Du, and S. K. Lim, "Placement-Driven Partitioning for Congestion Mitigation in Monolithic 3D IC Designs," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 34, no. 4, pp. 540–553, 2015.

[41] A. Koneru and K. Chakrabarty, "Analysis of electrostatic coupling in monolithic 3D integrated circuits and its impact on delay testing," *Proc. Eur. Test Work.*, vol. 2016-July, pp. 0–5, 2016.

[42] P. Batude, M. Vinet, A. Pouydebasque, L. Clavelier, C. LeRoyer, C. Tabone, B. Previtali, L. Sanchez, L. Baud, A. Roman, V. Carron, F. Nemouchi, S. Pocas, C. Comboroure, V. Mazzocchi, H. Grampeix, F. Aussenac, and S. Deleonibus, "Enabling 3D Monolithic Integration," *ECS Trans.*, vol. 16, no. 8, pp. 47–54, 2008.

[43] T. E. Sarvey, Y. Zhang, L. Zheng, P. Thadesar, R. Gutala, C. Cheung, A. Rahman, and M. S. Bakir, "Embedded cooling technologies for densely integrated electronic systems," *Proc. Cust. Integr. Circuits Conf.*, vol. 2015-Novem, 2015.

[44] H. An, M. A. Ehsan, Z. Zhou, and Y. Yi, "Electrical Modeling and Analysis of 3D Synaptic Array using Vertical RRAM Structure," pp. 1–6, 2017.

[45] A. Danideh and R. A. Sadeghzadeh, "Cpw-fed slot antenna for mimo system applications," *Indian J. Sci. Technol.*, vol. 6, no. 1, pp. 3872–3875, 2013.

[46] M. F. Jhong, C. Y. Ho, P. C. Pan, H. H. Cheng, S. C. Hsieh, C. C. Wang, and L. T. Hwang, "Scalable Modeling and Measurement of TSV Applied for Efficiency Improvement of a RF PA," *Proc. - Electron. Components Technol. Conf.*, vol. 2016-Augus, pp. 1477–1482, 2016.

[47] R. Yarema, "Development of 3D Integrated Circuits for HEP," pp. 71–75.

[48] Z. Xu, X. Gu, M. Scheuermann, K. Rose, B. C. Webb, J. U. Knickerbocker, and J. Q. Lu, "Modeling of power delivery into 3D chips on silicon interposer," *Proc. - Electron. Components Technol. Conf.*, pp. 683–689, 2012.

[49] Y. Zhang, T. E. Sarvey, and M. S. Bakir, "Thermal Evaluation of 2.5-D Integration Using Bridge-Chip Technology: Challenges and Opportunities," *IEEE Trans. Components, Packag. Manuf. Technol.*, pp. 1–10, 2017.

[50] U. Kang, H. J. Chung, S. Heo, D. H. Park, H. Lee, J. H. Kim, S. H. Ahn, S. H. Cha, J. Ahn, D. M. Kwon, J. W. Lee, H. S. Joo, W. S. Kim, D. H. Jang, N. S. Kim, J. H. Choi, T. G. Chung, J. H. Yoo, J. S. Choi, C. Kim, and Y. H. Jun, "8 Gb 3-D DDR3 DRAM using through-silicon-via technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 111–119, 2010.

[51] R. Li, C. Jin, S. C. Ong, T. G. Lim, K. F. Chang, and S. W. Ho, "Embedded wafer level packaging for 77-GHz automotive radar front-end with through silicon via and its 3-D

integration," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 3, no. 9, pp. 1481–1488, 2013.

[52] M. S. Bakir, C. King, D. Sekar, H. Thacker, B. Dang, G. Huang, A. Naeemi, and J. D. Meindl, "3D heterogeneous integrated systems: Liquid cooling, power delivery, and implementation," *Proc. Cust. Integr. Circuits Conf.*, no. Cicc, pp. 663–670, 2008.

[53] T. S. V Interconnects, "2.5D interposer, 3DIC and TSV Interconnects," 2012.

[54] W. Wahby, L. Zheng, Y. Zhang, and M. S. Bakir, "A Simulation Tool for Rapid Investigation of Trends in 3D IC Performance and Power Consumption," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 6, no. 2, pp. 192–199, 2016.

[55] I. S. Devised, I. For, T. Assessment, I. S. Without, R. To, A. N. Y. Commercial, C. Pertaining, T. O. Individual, P. Or, O. For, and I. N. K. To, "ITRS for semiconductor 2015," 2015.

[56] S. Wünsche, C. Clauß, P. Schwarz, and F. Winkler, "Electro-thermal circuit simulation using simulator coupling," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 5, no. 3, pp. 277–282, 1997.

[57] M. Amimul Ehsan, Z. Zhou, L. Liu, and Y. Yi, "An Analytical Through Silicon Via (TSV) Surface Roughness Model Applied to a Millimeter Wave 3-D IC," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 4, pp. 815–826, 2015.

[58] and C. G. Yue Ma, Olivier Valorge, J. R. Cárdenas-Valdez, Francis Calmon, J.C. Núñez-Pérez, J. Verdier, "3-D Interconnects with IC's Stack Global Electrical Context Consideration," in *Noise Coupling in System-on-Chip*, Thomas noulis, Ed. CRC Press, 2017, pp. 63–92.

[59] W. M. Holt, "Moore's law: A path going forward," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 59, pp. 8–13, 2016.

[60] K. Arabi, K. Samadi, and Y. Du, "3D VLSI: A scalable integration beyond 2D," *Int. Symp. Phys. Des.*, pp. 1–7, 2015.

[61] M. M. S. Aly, M. Gao, G. Hills, C. S. Lee, G. Pitner, M. M. Shulaker, T. F. Wu, M. Asheghi, J. Bokor, F. Franchetti, K. E. Goodson, C. Kozyrakis, I. Markov, K. Olukotun, L. Pileggi, E. Pop, J. Rabaey, C. Ré, H. S. P. Wong, and S. Mitra, "Energy-efficient abundant-data computing: The N3XT 1,000," *Computer (Long. Beach. Calif).*, vol. 48, no. 12, pp. 24–33, 2015.

[62] P. Coudrain, D. Henry, A. Berthelot, J. Charbonnier, S. Verrun, R. Franiatte, N. Bouzaida, G. Cibrario, F. Calmon, I. O'Connor, T. Lacrevaz, L. Fourneaud, B. Flechet, N. Chevrier, A. Farcy, and O. Le-Briz, "3D Integration of CMOS image sensor with coprocessor using TSV last and micro-bumps technologies," *Proc. - Electron. Components Technol. Conf.*, pp. 674–682, 2013.

[63] TREJO ROSLLO Josué, "Contribution à l'amélioration de la Sensibilité d'un Micro-récepteur RMN Implantable," 2014.

[64] J. Knickerbocker and P. Andry, “3D silicon integration,” in *ECTC 2008*, 2008, pp. 538–543.

[65] L. Cadix, A. Farcy, C. Bermond, C. Fuchs, P. Leduc, M. Rousseau, M. Assous, A. Valentian, J. Roullard, E. Eid, N. Sillon, B. Flechet, and P. Ancey, “Modelling of Through Silicon Via RF performance and impact on signal transmission in 3D integrated circuits,” *2009 IEEE Int. Conf. 3D Syst. Integr.*, pp. 1–7, 2009.

[66] Y. Zhu, S. Ma, X. Sun, R. Fang, X. Zhong, Y. Bian, M. Chen, J. Chen, M. Miao, W. Lu, and Y. Jin, “Development and characterization of a through-multilayer TSV integrated SRAM module,” *Proc. - Electron. Components Technol. Conf.*, pp. 885–890, 2013.

[67] J. S. Kim, C. S. Oh, H. Lee, D. Lee, H. R. Hwang, S. Hwang, B. Na, J. Moon, J. G. Kim, H. Park, J. W. Ryu, K. Park, S. K. Kang, S. Y. Kim, H. Kim, J. M. Bang, H. Cho, M. Jang, C. Han, J. B. Lee, K. Kyung, J. S. Choi, and Y. H. Jun, “A 1.2V 12.8GB/s 2Gb mobile wide-I/O DRAM with 4x128 I/Os using TSV-based stacking,” *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 11, no. 6, pp. 496–497, 2011.

[68] K. Yoon, G. Kim, W. Lee, T. Song, J. Lee, H. Lee, K. Park, and J. Kim, “Modeling and analysis of coupling between TSVs, metal, and RDL interconnects in TSV-based 3D IC with silicon interposer,” *Proc. Electron. Packag. Technol. Conf. EPTC*, vol. 3, pp. 702–706, 2009.

[69] K. J. Han, M. Swaminathan, and J. Jeong, “Modeling of Through-Silicon Via (TSV) Interposer Substrate Layer Thickness Effects,” vol. 5, no. 1, pp. 108–118, 2015.

[70] I. Ndip, K. Zoschke, K. Löbbicke, M. J. Wolf, S. Guttowski, H. Reichl, K. D. Lang, and H. Henke, “Analytical, numerical, and measurement-based methods for extracting the electrical parameters of through silicon vias (TSVs),” *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 4, no. 3, pp. 504–515, 2014.

[71] Z. Xu, A. Beece, D. Zhang, Q. Chen, K. Rose, and J. Q. Lu, “Characterization and modeling of solder balls and through-strata-vias (TSVs) in 3D architecture,” *2010 IEEE 19th Conf. Electr. Perform. Electron. Packag. Syst. EPEPS 2010*, pp. 37–40, 2011.

[72] N. H. Khan, S. M. Alam, and S. Hassoun, “Through-Silicon Via(TSV)-induced Noise Characterization and Noise Mitigation using Coaxial TSV,” in *Computer*, 2009, pp. 1–7.

[73] M. Rousseau, O. Rozeau, G. Cibrario, G. Le Carval, M. Jaud, P. Leduc, A. Farcy, A. Marty, and M. Crolles, “Through-silicon via based 3D IC technology : Electrostatic simulations for design methodology,” *Structure*, no. March, pp. 1740–1763, 2008.

[74] J. S. Pak, C. Ryu, and J. Kim, “Electrical Characterization of Trough Silicon Via (TSV) depending on Structural and Material Parameters based on 3D Full Wave Simulation,” 2011.

[75] A. E. Engin and N. S. Raghavan, “Modeling of coupled TSVs in 3D ICs,” *IEEE Int. Symp. Electromagn. Compat.*, no. 2, pp. 7–11, 2012.

[76] T. Bandyopadhyay, K. J. Han, D. Chung, R. Chatterjee, M. Swaminathan, and R. Tummala, “Rigorous electrical modeling of through silicon vias (TSVs) with MOS

capacitance effects," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 1, no. 6, pp. 893–903, 2011.

[77] K. Y. Chen, Y. A. Sheu, C. H. Cheng, J. H. Lin, Y. P. Chiou, and T. L. Wu, "A novel TSV model considering nonlinear MOS effect for transient analysis," *2012 IEEE Electr. Des. Adv. Packag. Syst. Symp. EDAPS 2012*, no. 1, pp. 49–52, 2012.

[78] W. A. Vitale, M. M. López, A. M. Ionescu, A. Klumpp, R. Merkel, and J. Weber, "3D TSV Based High Frequency Components for RF IC and RF MEMS Applications," pp. 8–11.

[79] K. J. Han, M. Swaminathan, and T. Bandyopadhyay, "Electromagnetic modeling of through-silicon via (TSV) interconnections using cylindrical modal basis functions," *IEEE Trans. Adv. Packag.*, vol. 33, no. 4, pp. 804–817, 2010.

[80] C. G. Yue MA, Francis CALMON, "Electric compact model of TSV and an associated developed tool," in *6th Electronic System-Integration Technology Conference*, 2016.

[81] K. J. Han and M. Swaminathan, "Consideration of MOS Capacitance Effect in TSV Modeling Based on Cylindrical Modal Basis Functions," vol. 2, pp. 41–44, 2012.

[82] L. Yu, H. Yang, T. T. Jing, M. Xu, R. Geer, and W. Wang, "Electrical Characte rization of RF TSV for 3D Multi- Core a nd Heterogeneous ICs," pp. 686–693, 2010.

[83] S. H. Hall, G. W. Hall, and J. A. McCall, *High speed digital system design: a handbook of interconnect theory and design practices*. 2000.

[84] S. R. XU CA, LI, "Compact AC Modeling and Performance Analysis of Through-Silicon Vias in 3D-ICs," *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3405–3417, 2010.

[85] I. Savidis and E. G. Friedman, "Closed-form expressions of 3-D via resistance, inductance, and capacitance," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1873–1881, 2009.

[86] Y. Y.-T. Qian Li-Bo, Zhu Zhang-Ming, "Through-slicon-via-aware interconnect prediction model for 3D integrated circuit," *Acta Phys.Sin*, vol. 61, no. 6, 2012.

[87] Y. Liang and Y. Li, "Closed-form expressions for the resistance and the inductance of different profiles of through-silicon vias," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 393–395, 2011.

[88] K. Banerjee and A. Mehrotra, "Analysis of on-chip inductance effects for distributed RLC interconnects," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 21, no. 8, pp. 904–915, 2002.

[89] L.-B. Qian, Z.-M. Zhu, and Y.-T. Yang, "Three-dimensional global interconnect based on a design window," *Chinese Phys. B*, vol. 20, no. 10, p. 108401, 2011.

[90] D. C. Sekar, A. Naeemi, R. Sarvari, J. A. Davis, and J. D. Meindl, "IntSim: A CAD tool for optimization of multilevel interconnect networks," *IEEE/ACM Int. Conf. Comput. Des. Dig. Tech. Pap. ICCAD*, no. 1, pp. 560–567, 2007.

[91] T. Lu and A. Srivastava, "Detailed electrical and reliability study of tapered TSVs," *2013*

IEEE Int. 3D Syst. Integr. Conf. 3DIC 2013, 2013.

[92] P. Dixit, H. Viljanen, J. Salonen, T. Suni, J. Molarius, and P. Monnoyer, "Fabrication, electrical characterization and reliability study of partially electroplated tapered copper through-silicon vias," *Proc. Tech. Pap. - Int. Microsystems, Packag. Assem. Circuits Technol. Conf. IMPACT*, pp. 190–193, 2013.

[93] A. E. Engin and S. R. Narasimhan, "Modeling of crosstalk in through silicon vias," *IEEE Trans. Electromagn. Compat.*, vol. 55, no. 1, pp. 149–158, 2013.

[94] A. Todri-Sanial, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, and A. Virazel, "Worst-case power supply noise and temperature distribution analysis for 3D PDNs with multiple clock domains," *2013 IEEE 11th Int. New Circuits Syst. Conf. NEWCAS 2013*, pp. 0–3, 2013.

[95] N. H. Khan, S. M. Alam, and S. Hassoun, "Power delivery design for 3-D ICs using different through-silicon via (TSV) technologies," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 19, no. 4, pp. 647–658, 2011.

[96] A. P. Nguyen, "Through Silicon Via Interconnections for High Reliability Applications," 2016.

[97] B. Kim, C. Sharbono, T. Ritzdorf, and D. Schmauch, "Factors affecting copper filling process within high aspect ratio deep vias for 3D chip stacking," *Proc. - Electron. Components Technol. Conf.*, vol. 2006, pp. 838–843, 2006.

[98] A. Todri-Sanial, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, and A. Virazel, "Worst-case power supply noise and temperature distribution analysis for 3D PDNs with multiple clock domains," *2013 IEEE 11th Int. New Circuits Syst. Conf. NEWCAS 2013*, no. June 2013, 2013.

[99] F. Wang, Z. Zhu, Y. Yang, X. Liu, and R. Ding, "Thermo-mechanical performance of Cu and SiO2 filled coaxial through-silicon-via (TSV)," *IEICE Electron. Express*, vol. 10, no. 24, pp. 1–6, 2013.

[100] A. Magnani, M. De Magistris, A. Maffucci, and A. Todri-Sanial, "A node clustering reduction scheme for power grids electrothermal analysis," *SPI 2015 - 19th IEEE Work. Signal Power Integr.*, 2015.

[101] A. Todri-sanial and Y. Cheng, "A Study of 3-D Power Delivery Networks With Multiple Clock Domains," vol. 24, no. 11, pp. 3218–3231, 2016.

[102] C. Aobo, L. Feng, W. Gaofeng, and W. Bing-Zhong, "Closed-form impedance model for annular through-silicon via pairs in three-dimensional integration," *IET Microwaves, Antennas Propag.*, vol. 9, no. 8, pp. 808–813, 2015.

[103] R. Vyas, A. Rida, S. Bhattacharya, and M. M. Tentzeris, "Liquid Crystal Polymer (LCP): The ultimate solution for low-cost RF flexible electronics and antennas," *IEEE Antennas Propag. Soc. AP-S Int. Symp.*, no. 1, pp. 1729–1732, 2007.

[104] A. Magnani, M. De Magistris, A. Todri-Sanial, and A. Maffucci, "Electrothermal analysis

of carbon nanotubes power delivery networks for nanoscale integrated circuits," *IEEE Trans. Nanotechnol.*, vol. 15, no. 3, pp. 380–388, 2016.

[105] R. Nagarajan, E. Liao, D. Lee, C. S. Soh, K. Prasad, and N. Balasubramanian, "Development of a novel deep silicon tapered via etch process for through-silicon interconnection in 3-D integrated systems," *Proc. - Electron. Components Technol. Conf.*, vol. 2006, pp. 383–387, 2006.

[106] A. Todri, S. Kundu, P. Girard, A. Bosio, L. Dilillo, and A. Virazel, "A study of tapered 3-D TSVs for power and thermal integrity," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 21, no. 2, pp. 306–319, 2013.

[107] M. Rack, J. P. Raskin, X. Sun, G. Van Der Plas, P. Absil, and E. Beyne, "Fast and Accurate Modelling of Large TSV Arrays in 3D-ICs Using a 3D Circuit Model Validated Against Full-Wave FEM Simulations and RF Measurements," *Proc. - Electron. Components Technol. Conf.*, vol. 2016-Augus, pp. 966–971, 2016.

[108] J. E. Lorival, F. Calmon, F. Sun, F. Frantz, C. Plossu, M. Le Berre, I. O'Connor, O. Valorge, J. Charbonnier, D. Henry, and C. Gontrand, "An efficient and simple compact modeling approach for 3-D interconnects with IC's stack global electrical context consideration," *Microelectronics J.*, vol. 46, no. 2, pp. 153–165, 2015.

[109] E. B. Rosa, "The self and mutual-inductances of linear conductors," *Bulletin of the Bureau of Standards*, vol. 4, no. 2. p. 301, 1908.

[110] T. N. Osborn, "All-Copper Chip-To-Substrate Interconnects for High Performance Integrated Circuit Devices," 2009.

[111] O. Valorge, F. Sun, J.-E. Lorival, M. Abouelatta-Ebrahim, F. Calmon, and C. Gontrand, "Analytical and Numerical Model Confrontation for Transfer Impedance Extraction in Three-Dimensional Radio Frequency Circuits," *Circuits Syst.*, vol. 03, no. 02, pp. 126–135, 2012.

[112] S. Fengyuan, "Analyse et Caractérisation des Couplages Substrat et de la Connectique dans les Circuits 3D: vers des Modèles Compacts," INSA-LYON, 2013.

[113] J. Kim, J. S. Pak, J. Cho, E. Song, J. Cho, H. Kim, T. Song, J. Lee, H. Lee, K. Park, S. Yang, M. S. Suh, K. Y. Byun, and J. Kim, "High-frequency scalable electrical model and analysis of a through silicon via (TSV)," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 181–195, 2011.

[114] K. Morot, A. Farcy, T. Lacrevaz, C. Bermond, P. Artillan, B. Fléchet, H. Jacquinot, and P. Scheiblin, "3D Interconnect Optimization for Single Channel 100-GBps Transmission in a Photonic Interposer," vol. 2, pp. 4–7.

[115] J. Kim, J. Cho, J. Kim, J. M. Yook, J. C. Kim, J. Lee, K. Park, and J. S. Pak, "High-frequency scalable modeling and analysis of a differential signal through-silicon via," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 4, no. 4, pp. 697–707, 2014.

[116] A. Ehsan, Z. Zhou, and Y. Yi, "Analytical Modeling and Analysis of Through Silicon Vias (TSVs) in High Speed Three-Dimensional System Integration," vol. 42, no. April, pp.

49–59, 2015.

[117] C. Ics, C. Cheng, S. Member, and T. Wu, “An Ultracompact TSV-Based Common-Mode Filter,” vol. 58, no. 4, pp. 1–8, 2016.

[118] and C. G. Yue Ma, Olivier Valorge, J. R. Cárdenas-Valdez, Francis Calmon, J.C. Núñez-Pérez, J. Verdier, “Electro-Thermal Considerations Dedicated to 3-D Integration; Noise Coupling,” in *CRC Press*, Thomas noulis, Ed. CRC Press, 2017, pp. 445–484.

[119] W. S. Zhao, J. Zheng, S. Chen, X. Wang, and G. Wang, “Transient Analysis of Through-Silicon Vias in Floating Silicon Substrate,” *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 1, pp. 207–216, 2017.

[120] M. Lee, J. S. Pak, and J. Kim, *Electrical design of through silicon via*, vol. 9789401790. 2014.

[121] H. Kim, J. Cho, S. Member, J. Kim, S. Member, S. Choi, S. Member, K. Kim, J. Lee, K. Park, J. S. Pak, and J. Kim, “A Wideband On-Interposer Passive Equalizer Design for Chip-to-Chip 30-Gb / s Serial Data Transmission,” vol. 5, no. 1, pp. 28–40, 2015.

[122] X. Gu, J. A. Silberman, A. M. Young, K. A. Jenkins, B. Dang, Y. Liu, X. Duan, R. Gordin, S. Shlafman, and D. Goren, “Characterization of TSV-induced loss and substrate noise coupling in advanced three-dimensional CMOS SOI technology,” *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 3, no. 11, pp. 1917–1925, 2013.

[123] E. Buitrago, M. F. B. Badia, Y. M. Georgiev, R. Yu, O. Lotty, J. D. Holmes, A. M. Nightingale, and A. M. Ionescu, “Functionalized 3D 7×20-array of vertically stacked SiNW FET for streptavidin sensing,” in *Device Research Conference - Conference Digest, DRC*, 2013, no. SUPPL., pp. 6–7.

[124] C. L. Ayala, D. Grogg, A. Bazigos, M. F. B. Badia, U. T. Duerig, M. Despont, and C. Hagleitner, “A 6.7 MHz nanoelectromechanical ring oscillator using curved cantilever switches coated with amorphous carbon,” in *European Solid-State Device Research Conference*, 2014, pp. 66–69.

[125] A. Bazigos, C. L. Ayala, M. Fernandez-Bolaños, Y. Pu, D. Grogg, C. Hagleitner, S. Rana, T. T. Qin, D. Pamunuwa, and A. M. Ionescu, “Analytical Compact Model in Verilog-A for Electrostatically Actuated Ohmic Switches,” *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2186–2194, 2014.

[126] E. A. Casu, M. M. Lopez, W. A. Vitale, and A. Mihai, “Design and Fabrication of High-K Filled Sub-IOO nm Gap Resonators with Embedded Dielectric Field Effect Transistor for Ultra High Frequency Applications,” vol. 58, no. 7, pp. 9–10, 2011.

[127] H. Le Poche, H. Guerin, R. Pohle, M. Fernández-Bolaños, J. Dijon, and A. . Ionescu, “resistive gas sensors fabricated by wafer-scale, in-situ integration of horizontal carbon nanotube membranes,” in *Transducers*, 2013, no. June, pp. 2584–2587.

[128] W. A. Vitale, M. Fernández-Bolaños, R. Merkel, A. Enayati, I. Ocket, W. De Raedt, J. Weber, P. Ramm, and A. M. Ionescu, “Fine pitch 3D-TSV based high frequency components for RF MEMS applications,” *Proc. - Electron. Components Technol. Conf.*,

vol. 2015-July, pp. 585–590, 2015.

[129] W. A. Vitale, M. Fernández-Bolaños, A. Bazigos, C. Dehollain, and A. M. Ionescu, "RF MEMS power sensors for ultra-low power wake-up circuit applications," in *European Solid-State Device Research Conference*, 2013, pp. 288–291.

[130] W. A. Vitale, M. Fernandez-Bolanos, A. Klumpp, J. Weber, P. Ramm, and A. M. Ionescu, "Ultra fine-pitch TSV technology for ultra-dense high-Q RF inductors," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2015, vol. 2015-Augus, pp. T52–T53.

[131] W. A. Vitale, M. Fernández-Bolaños, and a. M. Ionescu, "High-Q 3D Embedded Inductors using TSV for RF MEMS Tunable Bandpass Filters (4.65-6.8 GHz)," *Eur. Microw. Conf. 2012*, pp. 1–4, 2012.

[132] Y. C. Tseng, P. S. Chen, W. C. Lo, S. H. Wu, and T. L. Wu, "Compact TSV-based wideband bandpass filters on 3-D IC," *Proc. - Electron. Components Technol. Conf.*, pp. 2083–2088, 2013.

[133] T. Yang, M. Tamura, and T. Itoh, "Super compact low-temperature co-fired ceramic bandpass filters using the hybrid resonator," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 11 PART 1, pp. 2896–2907, 2010.

[134] M. M. Tentzeris, J. Laskar, J. Papapolymerou, S. Pinel, V. Palazzari, R. Li, G. DeJean, N. Papageorgiou, D. Thompson, R. Bairavasubramanian, S. Sarkar, and J. H. Lee, "3-D-Integrated RF and millimeter-wave functions and modules using liquid crystal polymer (LCP) system-on-package technology," *IEEE Trans. Adv. Packag.*, vol. 27, no. 2, pp. 332–340, 2004.

[135] D. Shariff, P. C. Marimuthu, K. Hsiao, L. Asoy, C. L. Yee, A. K. Oo, K. Buchanan, K. Crook, T. Wilby, and S. Burgess, "Integration of fine-pitched Through-Silicon Vias and Integrated Passive Devices," *Proc. - Electron. Components Technol. Conf.*, no. 2, pp. 844–848, 2011.

[136] Y. T. Lee, K. Liu, R. Frye, H. T. Kim, G. Kim, and B. Ahn, "Ultra-wide-band (UWB) band-pass-filter using integrated passive device (IPD) technology for wireless applications," *Proc. - Electron. Components Technol. Conf.*, pp. 1994–1999, 2009.

[137] M. Hoft and T. Shimamura, "Design of symmetric trisection filters for compact low-temperature Co-fired ceramic realization," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 1, pp. 165–175, 2010.

[138] T. Mori, M. Yamaguchi, S. Kuramochi, and Y. Fukuoka, "Development of a new interposer including embedded thin film passive elements," *IEEE Trans. Adv. Packag.*, vol. 32, no. 2, pp. 503–508, 2009.

[139] V. Sridharan, S. Min, V. Sundaram, V. Sukumaran, S. Hwang, H. Chan, F. Liu, C. Nopper, and R. Tummala, "Design and fabrication of bandpass filters in glass interposer with through-package-vias (TPV)," *Proc. - Electron. Components Technol. Conf.*, pp. 530–535, 2010.

[140] Z. Wu, Y. Shim, M. Rais-zadeh, and A. Arbor, "Miniaturized UWB Bandpass Filters

Integrated with Notch Filters Using a Silicon-based Integrated Passive Device Technology," in *IEEE MTT-S International Microwave Symposium*, 2011, pp. 1–4.

[141] C. Multiphysics, "COMSOL multiphysics." .

[142] M. Stucchi, J. De Vos, A. Jourdain, Y. Li, G. Van Der Plas, K. Croes, and E. Beyne, "Anomalous C-V Inversion in TSVs: The Problem and Its Cure," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1473–1479, 2018.

[143] J. Xie and M. Swaminathan, "Electrical-thermal co-simulation of 3D integrated systems with micro-fluidic cooling and joule heating effects," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 234–246, 2011.

[144] J. Xie, D. Chung, M. Swaminathan, M. Mcallister, A. Deutsch, L. Jiang, and B. J. Rubin, "Electrical-thermal co-analysis for power delivery networks in 3D system integration," *2009 IEEE Int. Conf. 3D Syst. Integr. 3DIC 2009*, no. 3, pp. 3–6, 2009.

[145] Y. Zhang and M. S. Bakir, "Integrated thermal and power delivery network co-simulation framework for single-die and multi-die assemblies," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 7, no. 3, pp. 434–443, 2017.

[146] L. Zheng, Y. Zhang, and M. S. Bakir, "Full-Chip Power Supply Noise Time-Domain Numerical Modeling and Analysis for Single and Stacked ICs," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1225–1231, 2016.

[147] A. Todri and A. Bosio, "Electro-Thermal Analysis of 3D Power Delivery Networks," in *49th Design Automation Conference Work-in-Progress (WIP) Track*, 2012, no. 1, pp. 3–4.

[148] A. Shayan, X. Hu, H. Peng, M. Popovich, W. Zhang, C. K. Cheng, L. Chua-Eoan, and X. Chen, "3D power distribution network co-design for nanoseale stacked silicon ICs," *Electr. Perform. Electron. Packag. EPEP*, pp. 11–14, 2008.

[149] M. Amimul Ehsan, Z. Zhou, and Y. Yi, "Modeling and Optimization of TSV for Crosstalk Mitigation in 3D Neuromorphic System," in *IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2016, pp. 621–626.

[150] J. Xie and M. Swaminathan, "Fast electrical-thermal co-simulation using multigrid method for 3D integration," *Proc. - Electron. Components Technol. Conf.*, no. 2, pp. 651–657, 2012.

[151] R. FANG, H. Liu, M. Miao, X. Sun, and Y. Jin, "stabilization and utilization of coupling MOS Capacitance between TSVs," in *IEEE 18th Electronics Packaging Technology Conference (EPTC)*, 2016, pp. 347–350.

[152] A. Todri-Sanial, "Frequency domain power and thermal integrity analysis of 3D power delivery networks," *2013 17th IEEE Work. Signal Power Integr.*, pp. 1–4, 2013.

[153] T. Bandyopadhyay, R. Chatterjee, D. Chung, M. Swaminathan, and R. Tummala, "Electrical modeling of through silicon and package vias," *2009 IEEE Int. Conf. 3D Syst. Integr. 3DIC 2009*, 2009.

[154] T. Aida, B. Alberto, D. Luigi, G. Patrick, and V. Arnaud, "Electro-Thermal Analysis of 3D

Power Delivery Networks," in *49th Design Automation Conference Work-in-Progress (WIP) Track*, 2011, no. 1, pp. 3–4.

[155] L. Hou, J. Fu, J. Wang, N. Gong, W. Zhao, and S. Geng, "A thermal-aware distribution method of TSV in 3D IC," in *IEEE 11th International Conference on ASIC (ASICON)*, 2015, pp. 1–3.

[156] V. Viswanathan, "Modeling and design of 3D Imager IC," 2013.

[157] Z. Zhang, X. Hu, C. Cheng, and N. Wong, "A block-diagonal structured model reduction scheme for power grid networks," *2011 Des. Autom. Test Eur.*, pp. 1–6, 2011.

[158] Y. Zhong and M. D. F. Wong, "Fast Algorithms for IR Drop Analysis in Large Power Grid," *Proc. IEEE/ACM Int. Conf. Comput. Des. Des.*, pp. 351–357, 2005.

[159] A. Todri-Sanial, "Electro-thermal characterization of Through-Silicon Vias," in *2014 15th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2014*, 2014.

[160] A. Todri-sanial, "Electro-Thermal Characterization of Through-Silicon Vias," *15th Int. Conf. Therm. Mech. Multi-Physics Simul. Exp. Microelectron. Microsystems, EuroSimE 2014*, pp. 2–7, 2014.

[161] A. Todri-Sanial, A. Bosio, L. Dilillo, P. Girard, and A. Virazel, "Fast and accurate electro-thermal analysis of three-dimensional power delivery networks," *2013 14th Int. Conf. Therm. Mech. Multi-Physics Simul. Exp. Microelectron. Microsystems*, pp. 1–4, 2013.

[162] L. Di Cioccio et al, "3D at CEA LETI MINATEC," in *3D at CEA LETI MINATEC*, 2006, p. 455.

[163] R. Gharpurey and S. Hosur, "Transform Domain Techniques for Efficient Extraction of Substrate Parasitics 2 : Theory : The Substrate Green Function," 1997.

[164] P. Leduc, L. Di Cioccio, B. Charlet, M. Rousseau, M. Assous, D. Bouchu, A. Roule, M. Zussy, P. Gueguen, A. Roman, O. Rozeau, M. Heitzmann, J. P. Nieto, L. Vandroux, P. H. Haumesser, R. Quenouillère, A. Toffoli, P. Sixt, S. Maitrejean, L. Clavelier, and N. Sillon, "Enabling technologies for 3D chip stacking," *Int. Symp. VLSI Technol. Syst. Appl. Proc.*, pp. 76–78, 2008.

[165] H. Utsuno and T. Fujikawa, "Transfer function method for measuring characteristic impedance and propagation constant of porous materials," *J. Acoust. Soc. Am. theakustical*, vol. 86, no. 2, pp. 637–643, 1989.

[166] N. Ahmed, T. Natarajan, and K. R. Rao, "Discrete Cosine Transform," *Comput. IEEE Trans.*, vol. C–23, no. 1, pp. 90–93, 1974.

[167] A. M. Niknejad, R. Gharpurey, and R. G. Meyer, "Numerically stable green function for modeling and analysis of substrate coupling in integrated circuits," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 17, no. 4, pp. 305–315, 1998.

[168] N. Verghese, D. J. Allstot, and S. Masui, "Rapid simulation of substrate coupling effects in mixed-mode ICs," *Proc. IEEE Cust. Integr. Circuits Conf. - CICC '93*, pp. 1–4, 1993.

[169] A. Torabian and Y. Leonard Chow, "Simulated image method for Green's function of multilayer media," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 9 PART 2, pp. 1777–1781, 1999.

[170] C. Gontrand, F. Sun, J. Ricardo Cardenas-Valdez, Y. Ma, C. Plossu, F. Calmon, J. Cruz Nunez-Perez, and J. Verdier, "3D substrate modeling; From a first order electrical analysis, towards some possible signal fluctuations consideration, for radio frequency circuits," *Microelectronics J.*, vol. 45, no. 8, pp. 1061–1068, 2014.

[171] C. Software, "User-Driven COMSOL Software Updates Now Available in Version 5.2a," *http://www.comsol.com/*, 2016. .

[172] Y. Ma, L. Fakri-Bouchet, F. Calmon, and C. Gontrand, "Electrothermal modeling for 3-D nanoscale circuit substrates: Noise," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 6, no. 7, pp. 1042–1052, 2016.

[173] Y. Ma, F. Calmon, J. Verdier, and C. Gontrand, "A Possible Way to Grasp Electronic Noise, via some Transfer Impedance Methods, in Three-Dimensional Nanoscale Circuit Substrates," *Glob. Adv. Res. J. Eng. Technol. Innov.*, vol. 4, no. 4, pp. 2315–5124, 2015.

[174] Academic Press London, "Matlab," in *The Lichens*, 1990.

[175] Y. Tamene, C. Bougriou, and R. Bessaïh, "Thermal behaviour of a multilayer media in transient regime," *Rev. Energies Renouvelables*, vol. 10, no. 3, pp. 397–405, 2007.

[176] Y. S. Muzychka, K. R. Bagnall, and E. N. Wang, "Thermal spreading resistance and heat source temperature in compound orthotropic systems with interfacial resistance," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 3, no. 11, pp. 1826–1841, 2013.

[177] M. Ferraiuolo and O. Manca, "Heat transfer in a multi-layered thermal protection system under aerodynamic heating," *Int. J. Therm. Sci.*, vol. 53, pp. 56–70, 2012.

[178] A. Jain, R. E. Jones, R. Chatterjee, and S. Pozder, "Analytical and numerical modeling of the thermal performance of three-dimensional integrated circuits," *IEEE Trans. Components Packag. Technol.*, vol. 33, no. 1, pp. 56–63, 2010.

[179] G. Y. Tang, S. P. Tan, N. Khan, D. Pinjala, J. H. Lau, A. Bin Yu, K. Vaidyanathan, and K. C. Toh, "Integrated liquid cooling systems for 3-D stacked TSV modules," *IEEE Trans. Components Packag. Technol.*, vol. 33, no. 1, pp. 184–195, 2010.

[180] S. G. Singh and C. S. Tan, "Thermal mitigation using thermal through silicon via (TTSV) in 3-D ICs," *IMPACT Conf. 2009 Int. 3D IC Conf. - Proc.*, pp. 182–185, 2009.

[181] C. Zhu, Z. Gu, L. Shang, R. P. Dick, and R. Joseph, "Three-dimensional chip-multiprocessor run-time thermal management," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 27, no. 8, pp. 1479–1492, 2008.

[182] S. Im and K. Banerjee, "Full chip thermal analysis of planar(2-D)and vertically integrated(3-D)high performance ICs," *Int. Electron Devices Meet. 2000. Tech. Dig. IEDM (Cat. No.00CH37138)*, vol. 94305, pp. 727–730, 2000.

[183] T. Challenges and a T. Nanoscale, "Thermal management of nanoelectronics and 3-D

electronics.," *2011*, no. December, pp. 15–19, 2011.

[184] I. Soga, D. Kondo, Y. Yamaguchi, T. Iwai, M. Mizukoshi, Y. Awano, K. Yube, and T. Fujii, "Carbon nanotube bumps for LSI interconnect," *Proc. - Electron. Components Technol. Conf.*, pp. 1390–1394, 2008.

[185] J. Li, M. Qiu, J. Niu, Y. Zhu, and T. Chen, "Real-time constrained task scheduling in 3D chip multiprocessor to reduce peak temperature," *Proc. - IEEE/IFIP Int. Conf. Embed. Ubiquitous Comput. EUC 2010*, pp. 170–176, 2010.

[186] H. Qian, H. Liang, C. H. Chang, W. Zhang, and H. Yu, "Thermal simulator of 3D-IC with modeling of anisotropic TSV conductance and microchannel entrance effects," *Proc. Asia South Pacific Des. Autom. Conf. ASP-DAC*, pp. 485–490, 2013.

[187] C. Santos, P. Vivet, J.-P. Colonna, P. Coudrain, and R. Reis, "Thermal performance of 3D ICs: Analysis and alternatives," *2014 Int. 3D Syst. Integr. Conf. 3DIC 2014 - Proc.*, 2014.

[188] Y. Zhang, T. E. Sarvey, and M. S. Bakir, "Thermal challenges for heterogeneous 3D ICs and opportunities for air gap thermal isolation," *2014 Int. 3D Syst. Integr. Conf. 3DIC 2014 - Proc.*, vol. 2, 2014.

[189] E. Haritan, H. Yagi, W. Wolf, T. Hattori, P. Paulin, A. Nohl, D. Wingard, and M. Muller, "Multicore design is the challenge! What is the solution?," *Des. Autom. Conf. 2008. DAC 2008. 45th ACM/IEEE*, pp. 128–130, 2008.

[190] C. McDonough, B. Backes, Wei Wang, and R. E. Geer, "Thermal and spatial profiling of TSV-induced stress in 3DICs," *IEEE Int. Reliab. Phys. Symp. Proc.*, no. 11, pp. 527–532, 2011.

[191] J. L. Ayala, A. Sridhar, and D. Cuesta, "Thermal modeling and analysis of 3D multi-processor chips," *Integr. VLSI J.*, vol. 43, no. 4, pp. 327–341, 2010.

[192] M. S. Gupta, J. L. Oatley, R. Joseph, G. Y. Wei, and D. M. Brooks, "Understanding voltage variations in chip multiprocessors using a distributed power-delivery network," *Proc. -Design, Autom. Test Eur. DATE*, vol. 1, pp. 624–629, 2007.

[193] V. H. Duong, N. X. Hieu, H. S. Lee, and J. W. Lee, "A Battery-Assisted Passive EPC Gen-2 RFID Sensor Tag IC with Efficient Battery Power Management and RF Energy Harvesting," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7112–7123, 2016.

[194] L. Yu, H. Yang, J. Zhang, and W. Wang, "Performance evaluation of air-gap-based coaxial RF TSV for 3D NoC," *2011 IEEE/IFIP 19th Int. Conf. VLSI Syst. VLSI-SoC 2011*, pp. 94–97, 2011.

[195] G. Pares, "Image sensor evolution and enabling 3D technologies."

[196] T. Wang, J. Cap, Q. Wang, H. Zhang, and Z. Wang, "Design and realize of 3D integration of a pressure sensor system with through silicon via (TSV) approach," *ICEPT-HDP 2011 Proc. - 2011 Int. Conf. Electron. Packag. Technol. High Density Packag.*, pp. 40–43, 2011.

[197] K. Athikulwongse, J. S. Yang, D. Z. Pan, and S. K. Lim, "Impact of mechanical stress on

the full chip timing for through-silicon-via-based 3-D ICs," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 32, no. 6, pp. 905–917, 2013.

[198] J. Van Olmen, A. Mercha, G. Katti, C. Huyghebaert, J. Van Aelst, E. Seppala, Z. Chao, S. Armini, J. Vaes, R. C. Teixeira, M. Van Cauwenberghe, P. Verdonck K Verhemeldonck, A. Jourdain, W. Ruythooren, M. De Potter De Ten Broeck, A. Opdebeeck, T. Chiarella, B. Parvais, I. Debusschere, T. Y. Hoffmann, B. De Wachter, W. Dehaene, M. Stucchi, M. Rakowski, P. Soussan, R. Cartuyvels, E. Beyne, S. Biesemans, and B. Swinnen, "3D stacked IC demonstration using a through silicon via first approach," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 10–13, 2008.

[199] Y. C. Huang, P. T. Huang, S. L. Wu, Y. C. Hu, Y. H. You, M. Chen, Y. Y. Huang, H. C. Chang, Y. H. Lin, J. R. Duann, T. W. Chiu, W. Hwang, K. N. Chen, C. Te Chuang, and J. C. Chiou, "An ultra-high-density 256-channel/25mm2 neural sensing microsystem using TSV-embedded neural probes," *Proc. - IEEE Int. Symp. Circuits Syst.*, vol. 2016-July, pp. 1302–1305, 2016.

[200] A. Heryanto, W. N. Putra, A. Trigg, S. Gao, W. S. Kwon, F. X. Che, X. F. Ang, J. Wei, R. I Made, C. L. Gan, and K. L. Pey, "Effect of copper TSV annealing on via protrusion for TSV wafer fabrication," *J. Electron. Mater.*, vol. 41, no. 9, pp. 2533–2542, 2012.

[201] S. J. Kim, J. K. Seo, and K. H. Do, "Analytical and experimental investigation on the operational characteristics and the thermal optimization of a miniature heat pipe with a grooved wick structure," *Int. J. Heat Mass Transf.*, vol. 46, no. 11, pp. 2051–2063, 2003.

[202] M. Pedram and S. Nazarian, "Thermal Modeling, Analysis, and Management in VLSI Circuits: Principles and Methods," *Proc. IEEE*, vol. 94, no. 8, pp. 1487–1501, 2006.

[203] L. R. Zheng and H. Tenhunen, "Fast modeling of core switching noise on distributed LRC power grid in ULSI circuits," *IEEE Trans. Adv. Packag.*, vol. 24, no. 3, pp. 245–254, 2001.

[204] K. O. Petrosyants and N. I. Ryabov, "Quasi - 3D electro-thermal simulation of integrated transistor structures, IC chips and packages," *2016 Int. Sib. Conf. Control Commun. SIBCON 2016 - Proc.*, no. 1, pp. 0–5, 2016.

[205] K. Tewari, S. R.Doss, B. Chen, Q.Huang.A, S. Bhattacharya, and Z. Du, "Electro-Thermal Design of a Heat Pipe Based High Power Voltage Source Converter Using Emitter Turn-Off Thyristor," in *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, 2006, vol. 2, pp. 785–790.

[206] A. Driss, S. Maalej, and M. C. Zaghdoudi, "Electro-Thermal Modeling of Power IGBT Modules by Heat Pipe Systems," 2017.

[207] Keysight Technologies, "Advanced Design System." .

[208] C. Multiphysics, C. Software, and L. Agreement, "Signal Integrity and TDR Analysis of Adjacent Microstrip Lines."

[209] Wikipedia, "Generalized Conjugate Residual Method." [Online]. Available: https://en.wikipedia.org/wiki/Conjugate_residual_method.

[210] D. Li, S. Joshi, J. H. Kim, and S. Ogrenci-Memik, "End-to-End Analysis of Integration for Thermocouple-Based Sensors Into 3-D ICs," *IEEE Trans. Very Large Scale Integr. Syst.*, pp. 1–14, 2017.

[211] M. Magnini, B. Pulvirenti, and J. R. Thome, "Numerical investigation of hydrodynamics and heat transfer of elongated bubbles during flow boiling in a microchannel," *Int. J. Heat Mass Transf.*, vol. 59, no. 1, pp. 451–471, 2013.

[212] M. Lacroix, "Caracterisation du transport fluidique et thermique dans les mousses metalliques capillaires en cuivre Characterization of fluid and thermal transport in copper metal foam wicks," 2013.

[213] M. R.S.Shiraz, "Analytical and Numerical Modeling of Flat Heat Pipes," 2017.

[214] L. U. M. R. Cnrs, "COMSOL simulation of heat pipe," 2017.

[215] M. Aghvami and A. Faghri, "Analysis of flat heat pipes with various heating and cooling configurations," *Appl. Therm. Eng.*, vol. 31, no. 14–15, pp. 2645–2655, 2011.

[216] J. P. Longtin, B. Badran, and F. M. Gerner, "A One-Dimensional Model of a Micro Heat Pipe During Steady- State Operation," *J.Heat Transf.*, vol. 116, no. 3, pp. 709–715, 1994.

[217] D.Reay and P.Kew, *Heat Pipes: Theory, Design, and Applications*, 5th ed. London,U.K., 2006.

[218] Y. Yadavalli, J. A. Weibel, and S. V. Garimella, "Flat heat pipe performance thresholds at ultra-thin form factors," *Thermomechanical Phenom. Electron. Syst. -Proceedings Intersoc. Conf.*, pp. 527–534, 2014.

[219] Y. Yadavalli, Y. Yadavalli, J. A. Weibel, and S. V Garimella, "Performance-Governing Transport Mechanisms for Heat Pipes at Ultra-thin Form Factors," vol. 5, no. 11, pp. 1618–1627, 2015.

[220] Z. J. Zuo and A. Faghri, "A network thermodynamic analysis of the heat pipe," *Int. J. Heat Mass Transf.*, vol. 41, no. 11, pp. 1473–1484, 1998.

[221] S. Lips and F. Lefèvre, "A general analytical model for the design of conventional heat pipes," *Int. J. Heat Mass Transf.*, vol. 72, pp. 288–298, 2014.

[222] U. Vadakkan, J. Y. Murthy, and S. V Garimella, "Transient Analysis of Flat Heat Pipes," in *ASME Summer Heat Transfer Conference*, 2003, pp. 1–11.

[223] H. Li, Y. Tang, Y. Jin, B. Li, and T. Zou, "Experimental Analysis and FEM Simulation of Antigravity Loop-Shaped Heat Pipe for Radio Remote Unit," pp. 1–9, 2017.

[224] R. S. Prasher, "A Simplified Conduction Based Modeling Scheme for Design Sensitivity Study of Thermal Solution Utilizing Heat Pipe and Vapor Chamber Technology," *J. Electron. Packag.*, vol. 125, no. 3, p. 378, 2003.

[225] A. P. Investigation, O. F. Operating, L. In, H. Pipes, N. Metal, and F. As, "a Parametric Investigation of Operating Limits in Heat Pipes Using novel metal foams as wicks," in *ASME 2010*, 2010, pp. 1–9.

[226] A. Faghri, "Review and Advances in Heat Pipe Science and Technology," *J. Heat Transfer*, vol. 134, no. 12, p. 123001, 2012.

[227] U. Vadakkan, S. V. Garimella, and J. Y. Murthy, "Transport in Flat Heat Pipes at High Heat Fluxes From Multiple Discrete Sources," *J. Heat Transfer*, vol. 126, no. 3, p. 347, 2004.

[228] Y. Luo, B. Yu, X. Wang, and C. Li, "A novel flat micro heat pipe with a patterned glass cover," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 6, no. 7, pp. 1053–1057, 2016.

[229] G. Patankar, J. A. Weibel, and S. V Garimella, "A Time-Stepping Analytical Model for 3D Transient Vapor Chamber Transport," in *16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2017, pp. 1075–1087.

[230] A. Faghri, *Heat Pipe Science and Technology*. Washington DC: Taylor and Francis, 1995.

[231] R. Marek and J. Straub, "Analysis of the evaporation coefficient and the condensation coefficient of water," *Int. J. Heat Mass Transf.*, vol. 44, no. 1, pp. 39–53, 2001.

[232] H. Oh, Y. Zhang, T. E. Sarvey, G. S. May, and M. S. Bakir, "TSVs embedded in a microfluidic heat sink: High-frequency characterization and thermal modeling," *2016 IEEE 20th Work. Signal Power Integrity, SPI 2016 - Proc.*, pp. 1–4, 2016.

[233] A. Halder, A. Dhall, and A. K. Datta, "Modeling Transport in Porous Media With Phase Change: Applications to Food Processing," *J. Heat Transfer*, vol. 133, no. 3, p. 031010, 2011.

[234] R. Hopkins, A. Faghri, and D. Khrustalev, "Flat Miniature Heat Pipes With Micro Capillary Grooves," *J. Heat Transfer*, vol. 121, no. 1, pp. 102–109, 1999.

[235] Y. Zhang, A. Dembla, Y. Joshi, and M. S. Bakir, "3D stacked microfluidic cooling for high-performance 3D ICs," *Proc. - Electron. Components Technol. Conf.*, pp. 1644–1650, 2012.

[236] G. P. P. and D. W. B.R. Babin, "Steady-State Modeling and Testing of a Micro Heat Pipe," *J Heat Trans-T Asme*, vol. 112, no. August, pp. 595–601, 1990.

[237] S. Bories, M. Prat, and M. Quintard, "Transferts de chaleur dans les milieux poreux - Conduction, convection, rayonnement," in *Techniques de l'ingénieur*, 2008, pp. 6–10.

[238] L. Lin, R. Ponnappan, and J. Leland, "High performance miniature heat pipe," *Int. J. Heat Mass Transf.*, vol. 45, no. 15, pp. 3131–3142, 2002.

[239] Carey and V.P., "Liquid-vapor phase-change phenomena." 1992.

[240] R. P. J. W.Shockley, J.A.Copeland, *Quantum Theory of Atoms, Molecules and Solid State*. Academic Press New York, 1966.

[241] A.van der ziel, *Noise in solid state devices and circuits*. John wiley & sons, 1986.

[242] Van Der Ziel. A, *Noise. Sources, Characterisation, Measurement*. 1970.

[243] B. Picinbono, *Introduction à l'étude des signaux et phénomènes aléatoires*. .

[244] E. Beyne, "Reliable Via-Middle Copper Through-Silicon Via Technology for 3-D Integration," pp. 1–10, 2015.

[245] E. Beyne, "Electrical, thermal and mechanical impact of 3D TSV and 3D stacking technology on advanced CMOS devices - Technology directions," *2011 IEEE Int. 3D Syst. Integr. Conf. 3DIC 2011*, 2011.

[246] S. L. and C. G. Yue Ma , Samir Labiod, Latifa Fakri-Bouchet, Jacques Verdier, Francis Calmon, "Noise theoritical investigations for tri-dimmensional NMR circuit: towards the nanoscale," *EPH Int. J.*, vol. 4, no. 2, 2018.

[247] K. Thornber, C. T, and A. N. M, "Solid-State Electron," *Solid-State Electron*, vol. 17, no. 107, 1974.

[248] P.Nougier, *IV-V Microelectronics*. Elsevier Science Publishers, 1991.

[249] V. D. Z. A. Van Vliet, K. M., Friedmann, A., Zulstra, R.J;J; , Gisolf, A., "Noise in single injection diodes. I. A survey of methods," *J. Appl. PhysicsApplied Phys.*, 1975.

[250] L. Vandamme, "Electronic Devices," *IEEE Trans*, vol. 41, 1994.

[251] F. Filicori and G. Ghione, "A computationally efficient unified approach to the numerical analysis of the sensitivity and noise of semiconductor devices," *IEEE Trans. CAD*, p. 425, 1993.

[252] R. Rohrer, L. Nagel, Meyer.R, and Weber.L, "Computationally efficient electronic-circuit noise calculations," *IEEE J. Solid-State Circuits*, vol. 6, no. 4, pp. 204–213, 1971.

[253] R. D. X. Yin, Z. Zhu, Y. Yang, "Effectiveness of p+ Layer in Mitigating Substrate Noise Induced by Through-Silicon Via for Microwave Applications," *IEEE Microwave. Wirel. Component.Letter*, vol. 26, pp. 687–689, 2016.

[254] N. Y. F. Wang, "Study on thermal stress and keep-out zone induced by Cu and SiO2 filled coaxial-annular through-silicon via," *IEICE Electron. Express*, 2015.

[255] W. Guo, V. Moroz, G. Van Der Plas, M. Choi, A. Redolfi, L. Smith, G. Eneman, S. Van Huylenbroeck, P. D. Su, A. Ivankovic, B. De Wachter, I. Debusschere, K. Croes, I. De Wolf, A. Mercha, G. Beyer, B. Swinnen, and E. Beyne, "Copper through silicon via induced keep out zone for 10nm node bulk FinFET CMOS technology," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 340–343, 2013.

[256] W. Guo, M. Choi, A. Rouhi, V. Moroz, G. Eneman, J. Mitard, L. Witters, G. Van Der Plas, N. Collaert, G. Beyer, P. Absil, A. Thean, and E. Beyne, "Impact of 3D integration on 7nm high mobility channel devices operating in the ballistic regime," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2015-Febru, no. February, pp. 7.1.1–7.1.4, 2015.

[257] and Y. Y. F. Wang, N. Yu, Z. Zhu, X. Yin, "Effects of coaxial through-silicon via on carrier mobility along [100] and [110] crystal directions of (100) silicon," *IEICE Electron. Express*, 2015.

[258] L. J. H. Lin and Y. P. Chiou, "3-D transient analysis of TSV-induced substrate noise: Improved noise reduction in 3-D-ICs with incorporation of guarding structures," *IEEE Electron Device Lett.*, vol. 35, no. 6, pp. 660–662, 2014.

[259] K. Do Kim, B. J. Jun, J. B. Kim, K. S. Choi, S. Y. Cha, J. H. Lee, J. G. Jeong, S. H. Lee, and J. H. Lee, "Effectiveness of a guard ring utilizing an inversion layer surrounding a through silicon via," *IEEE Electron Device Lett.*, vol. 36, no. 3, pp. 268–270, 2015.

[260] C. Xu, R. Suaya, and K. Banerjee, "Compact modeling and analysis of coupling noise induced by through-Si-vias in 3-D ICs," *Electron Devices Meet. (IEDM), ...*, pp. 178–181, 2010.

[261] C. Xu, R. Suaya, and K. Banerjee, "Compact modeling and analysis of through-Si-Via-induced electrical noise coupling in three-dimensional ICs," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 4024–4034, 2011.

[262] H. Hovsepyan and M. Nakamoto, "Carrier Mobility Shift in Advanced Silicon Nodes Due to Chip-Package Interaction," vol. 139, no. June, pp. 1–11, 2017.

[263] T. T. Chiang, P. T. Huang, C. Te Chuang, K. N. Chen, J. C. Chiou, K. H. Chen, C. T. Chiu, H. M. Tong, and W. Hwang, "On-chip self-calibrated process-temperature sensor for TSV 3D integration," *Int. Syst. Chip Conf.*, pp. 370–375, 2012.

[264] A. Soni and R. Chandel, "Performance analysis of bulk driven MOSFET and CNFET for low voltage applications," *2013 Nirma Univ. Int. Conf. Eng. NUiCONE 2013*, pp. 1–6, 2013.

[265] S. Kannan, M. Sadi, and L. England, "Power Delivery in 3D Packages: Current Crowding Effects, Dynamic IR Drop and Compensation Network Using Sensors (Invited Paper)," *Proc. 35th Int. Conf. Comput. Des.*, pp. 55:1–55:6, 2016.

[266] G. V. der Plas, G. Eneman, and P. Marchal, "Tsv Induced Stress Modeling," 2010. [Online]. Available: www.sematech.org/meetings/archives/3d/8996/pres/Marchal.pdf.

[267] A. Nanoscale Integration and Modeling (NIMO) Group, "PTM(predictive technology model)," 2007. [Online]. Available: http://ptm.asu.edu/.

[268] F. Berto, P. Lazzarin, and C. H. Wang, "Three-dimensional linear elastic distributions of stress and strain energy density ahead of V-shaped notches in plates of arbitrary thickness," *Int. J. Fract.*, vol. 127, no. 3, pp. 265–282, 2004.

[269] A. Nanoscale Integration and modeling (NIMO) Group, "Predictive technology model." [Online]. Available: http://ptm.asu.edu/.

[270] I. De Wolf, K. Croes, and E. Beyne, "Expected Failures in 3-D Technology and Related Failure Analysis Challenges," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 8, no. 5, pp. 711–718, 2018.

[271] S. Jan, T. Chou, C. Yeh, C. W. Liu, S. Member, R. V Goldstein, V. A. Gorodtsov, and P. S. Shushpannikov, "A Compact Analytic Model of the Strain Field Induced by Through Silicon Vias," vol. 59, no. 3, pp. 777–782, 2012.

[272] Y. Zhong and M. D. F. Wong, “Thermal-aware IR drop analysis in large power grid,” in *9th International Symposium on Quality Electronic Design*, 2008, pp. 194–199.

[273] S. Bories and M. Prat, “Transferts de chaleur dans les milieux poreux,” 1995.

[274] Stanford University, “Stanford Virtual-Source Carbon Nanotube Field-effect Transistors Model,” 2015. [Online]. Available: http://nanohub.org/publications/42/2.

[275] C. Lee, “Virtual-Source Carbon Nanotube Field-Effect Transistors Model Technical User ’ s Manual,” 2015.

[276] F. Corradi, C. Eliasmith, and G. Indiveri, “Mapping arbitrary mathematical functions and dynamical systems to neuromorphic VLSI circuits for spike-based neural computation,” *Proc. - IEEE Int. Symp. Circuits Syst.*, pp. 269–272, 2014.

List of personal publications

Journals

[1] Christian GONTRAND, Fengyuan SUN, JR Cardenas-Valdez, *Yue MA*, Carole PLOSSU, Francis CALMON, José Cruz NP, Jacques VERDIER. “3D substrate modeling; From a first order electrical analysis, towards some possible signal fluctuations consideration, for radio frequency circuits.” *Microelectronics J.* **45,** 1061–1068 (2014).

[2] *Yue MA*, Francis CALMON., Jacques VERDIER, Christian GONTRAND. “A Possible Way to Grasp Electronic Noise, via some Transfer Impedance Methods, in Three-Dimensional Nanoscale Circuit Substrates.” *Glob. Adv. Res. J. Eng. Technol. Innov.* **4,** 2315–5124 (2015).

[3] *Yue MA*, Latifa FAKRI-BOUCHET, Francis CALMON, Christian GONTRAND. “Electro-thermal modeling for 3-D nanoscale circuit substrates: Noise.” *IEEE Trans. Components, Package. Manuf. Technol.* **6,** 1042–1052 (2016).

[4] *Yue Ma*, Samir Labiod, Latifa Fakri-Bouchet, Jacques VERDIER, Francis Calmon, S. L. and Christian GONTRAND. “Noise theoretical investigations for tri-dimensional NMR circuit: towards the nanoscale.” *EPH International Journal.* **4,** (2018).

International Conferences

[1] *Yue MA*, Francis CALMON, Christian GONTRAND. “Electric compact model of TSV and an associated developed tool”. In *6th Electronic System-Integration Technology Conference* (ESTC 2016, 2016).

Book Chapters

[1] *Yue Ma*, Olivier VALORGE, J. R. Cárdenas-Valdez, Francis CALMON, J.C. Núñez-Pérez, J. VERDIER, and Christian GONTRAND., “Electro-Thermal Considerations Dedicated to 3-D Integration; Noise Coupling” in *Noise Coupling in System-on-Chip* (ed. Thomas NOULIS) 445–484 (CRC Press, 2017).

[2] *Yue Ma*, Olivier VALORGE, J. R. Cárdenas-Valdez, Francis CALMON, J.C. Núñez-Pérez, J. VERDIER, and Christian GONTRAND., “3-D Interconnects with IC’s Stack Global Electrical Context Consideration” in *Noise Coupling in System-on-Chip* (ed. Thomas NOULIS) 63–92 (CRC Press, 2017).

FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : MA
(avec précision du nom de jeune fille, le cas échéant)

DATE de SOUTENANCE : 16 Mai 2018

Prénoms : Yue

TITRE :
Modèles compacts électro-thermiques du premier ordre et considération de bruit pour les cirrcuits 3D

NATURE : Doctorat

Numéro d'ordre : AAAALYSEIXXXX

Ecole doctorale : EEA

Spécialité :
Micro/Nano electronique

RESUME :
Three Dimensional (3D) Integration and Packaging has been successful in mainstream devices to increase logic density and to reduce data movement distances. It solves the fundamental limits of scaling e.g. increasing delay in interconnections, development costs and variability. Most memory devices shipped today have some form of chip-stacking involved. But because of the power dissipation limits of ICs, today's MPU's operating frequency has been limited to a few GHz.
The aim of the thesis is to provide a global design method for the 3D integrated circuit in electrical, thermal, electro-thermal and also noise field. To this end, the research question is as follows: How to realize the 3D IC design, how to manage VLS 3D IC and how to solve the thermal issues in the 3D IC. In this context, the simulation methods for substrate and also relative connectivity (TSV, RDL, Micro strip and circuits embedded into the substrate) are proposed.
In order to satisfy the research demand, a 3D-TLE and a substrate impedance are programmed in Matlab, which can automatically extract from any contacts; impedance, of arbitrary shape and arbitrary material. The extractor is 100% compatible with SPICE core simulator, and verified with measurement results and FEM simulation results. And as for a demo, a 25 GHz frequency and 2GHz bandwidth RF filter is propose in this work. Another electro-thermal simulator is also programmed and verified with ADS. As a solution to the local heat dissipation, flat heat pipe (FHP) is proposed as a prospective component. The heat-pipe model is verified with FEM simulation. The substrates noise analysis method and electrical and thermos-mechanical keep-out-of-zone (KOZ) calculation methods are also presented.

MOTS-CLÉS :
TSV, 3D IC, 3D-TLE, electro-thermal, noise, FHP, KOZ

Laboratoire (s) de recherche :
INL (Institute of nanotechnology of Lyon)

Directeur de thèse:
Christian GONTRAND

Président de jury :

Composition du jury : Eric BEYNE, Aida TODRI-SANIAL, Anne KAMINSKI, Latifa FAKRI-BOUCHET, Catherine BRU-CHEVALLIER, Abdelkader SOUIFI, Jean-Philippe COLONNA