INNOVATIVE NUMERICAL PROTECTION RELAY DESIGN ON THE BASIS OF SAMPLED MEASURED VALUES FOR SMART GRIDS

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To my father, Daniel,
To my mother, Rose,
To my little sister, Christelle.

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Acronyms

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AC:	Alternative Current
ADC:	Analogue-to-Digital Converter
ASCI:	Abstract Communication Service Interface
CPU:	Central Processing Unit
CT:	Current Transformer
CVT:	Capacitive Voltage Transformer
DA:	Data Attribute
DAQ:	Data Acquisition System
DC:	Direct Current
DFS:	Discrete Fourier Series
DFT:	Discrete Fourier Transform
DG:	Distributed Generator
DO:	Data Object
DSP:	Digital Signal Processor
DTFT:	Discrete Time Fourier Transform
EEPROM:	Electrically-Erasable Read Only Memory
EMS:	Energy Management System
EPRI:	Electric Power Research Institute
FE:	Frequency Error
FIR:	Finite Impulse Response
FS:	Fourier Series
FT:	Fourier Transform
GPS:	Global Positioning System
HMI:	Human Machine Interface
IEC:	International Electrotechnical Commission
IED:	Intelligent Electronic Device
IEEE:	Institute of Electrical and Electronics Engineers
IIR:	Infinite Impulse Response
I/O:	Input and Output
IpDFT:	Interpolated-Discrete Fourier Transform
IT:	Instrument Transformer

LD: Logical Device
LES: Least Error Squares
LN: Logical Node
LSB: Least Significant Bit
MCAA: MultiCast Application Association
MMS: Manufacturing Message Specification
MU: Merging Unit
NIPS: National Interconnected Power System
ONS: Operator of the National electricity System
OSI: Open Systems Interconnection
PDC: Phasor Data Concentrator
PMU: Phasor Measurement Unit
PPS: Pulse-Per-Second
PTP: Precision Time Protocol
RAM: Random Access Memory
RFE: Rate-Of-Change-Of-Frequency Error
RMS: Root Mean Square
ROCOF: Rate-Of-Change-Of-Frequency
ROM: Read Only Memory
SAMU: Stand-Alone Merging Unit
SAS: Substation Automation System
SCADA: Supervisory Control And Data Acquisition System
SCDR: Symmetrical Component Distance Relay
S/H: Sample and Hold
SMV: Sampled Measured Value
SNTP: Simple Network Time Protocol
SPMS: SynchroPhasor Measurement System
TC: Technical Committee
TCP/IP: Transmission Control Protocol/Internet Protocol
TPAA: Two Party Application Association
TVE: Total Vector Error
UCA: Utility Communications Architecture
UDP: User Datagram Protocol
UTC: Coordinate Universal Time
VT: Voltage Transformer
WAMPAC: Wide Area Measurement Protection And Control
WAMPS: Wide Area Measurement and Protection System
WAMS: Wide Area Measurement System

General introduction

Power systems consist of the involvement of all apparatus working together with a view to producing, transferring, distributing, and consuming the electricity from the production means to the farthest consumers. In their conventional structure, the electricity generation is made possible through centralized large power stations located at a relatively small number of sites. The electrical energy is first transmitted over long distances through a highly interconnected high voltage transmission networks. Then, the subtransmission networks supply the primary substations as well as the large industrial consumer high voltage centers. Finally, the distribution networks, architected mainly in a radial way, are aimed at feeding the electricity to medium and low voltages passive end users [AH09].

Large generating stations, transformers, high-voltage lines, each of these components are designed, sometimes operated, and linked to each other to supply the consumer the exact amount of energy required at any given instant of time in the most cost-effective way. Indeed, the electricity cannot be generally stored in an efficient way. It is thus mandatory to ensure a balance between generation and consumption of electrical powers in real time every day of the year. Otherwise, dramatic outages such as cascading events leading to blackouts may occur. It has been determined, following the Northeast blackout of August 2003, that the cost of a blackout, even if variable, could arise 1% of the Gross Domestic Product of a particular country [Aeg11]. Under normal operating conditions, the power systems are rather seldom in an ideal state because the generation-demand balance is never perfect as load fluctuates by nature. Many other usual situations can occur in the electrical grid whose resulting voltages and currents waveforms shift from the perfect three-phase balanced system of 50 Hz, as for instance, switching operations, inrush currents due to power transformers energization, asymmetric loads and start of large induction motors.

Furthermore, abnormal phenomena can occur in power systems. Those situations are due to either internal or external influences which cannot be avoided by essence. Among them, climatic disasters, physical accidents, equipment failure, misoperation owing to human error illustrate some of the original issues related to electrical networks. Many of these result in faults whose consequences may be the destruction of apparatus, the death of human beings, or even losses of system stability and blackouts [RSW11a]. Despite the fact that primary, secondary, and tertiary controls are definitely useful to overcome instability issues, they are however helpless against massive disturbances.

When abnormal conditions, or faults, happen, it is necessary to involve items with the aim of detecting and minimizing the extent and time of the outage. One of them is called protective relay and is defined as "a relay whose function is to detect defective lines or apparatus or other power system conditions of an abnormal or dangerous nature and to initiate appropriate control circuit action" [JLB14] of an associated circuit breaker. Protection relays are unnecessary during normal operations of the power systems. However, when a fault occurs, their use becomes necessary. They cannot prevent the disturbances from happening, but rather react after the fault appearance. Obviously, protection relays are designed to sense faults based on the increases of the currents and the decreases of the voltages which, most of the time, attest a fault condition. Actually, the sensitivity is one of the four general requirements whose every protection relays have to fulfill. The three others are designated as selectivity, reliability, and operating speed. They are all explained below:

The sensitivity is the ability to react to very small deviations of quantities of interest following the fault appearance.

The selectivity represents the aptitude to isolate only the defective parts of the power systems from the remaining healthy segments.

The reliability is the ability to trigger, or trip, only when a fault occurs to avoid false tripping condition and isolate healthy sections of the electrical grid.

The operating speed is the ability to react in the shortest possible period of time.

These four requirements represent the cornerstones of the design of a protection relay. It is up to the designer to emphasize one particular element to the detriment of others. For instance, the reliability and the operating speed are two targets diametrically opposed, so that a tradeoff between them is most often made. The most reliable relay will never be used if it needs an excessively long period of time to detect a fault because that fault could lead to damage equipment before the relay reacts. Conversely, the fastest relay may be useless as well if the slightest disturbances cause unwanted tripping.

Today, protection relays are widely deployed in both the transmission and the distribution networks. However, the protection algorithms involved are different and depend on the nature of the network where the relay is installed. Indeed, the transmission network, considered as the backbone of the electrical grid, is already well instrumented due to its specific role in the generation-demand balance and the safety imperatives of the whole electrical system. In addition to the advanced protection algorithms, the transmission networks involve measurement, supervision, and control-command cutting-edge technologies unlike the distributions networks, designed with a different philosophy for economic reasons intrinsically related to their widespread and distributed nature. Thus, transmission networks are protected by highly sophisticated protection algorithms which are, sometimes, communicating. Conversely, as there is a lack of sophisticated instrumentation in the distribution networks, they are protected with basic protection algorithms. Nevertheless, the distribution grids architecture is currently changing [EAR+09] to be adapted to the fast growing of distributed generation share at the distribution level which not only breaks the traditional decoupling between transmission and distribution grids but puts

emphasis on the need for advanced protection system [Jec11]. The modernization of electricity transmission and distribution grids is the foundation of the Smart Grids where new protection relays will be the cornerstone to cope with new paradigms.

The first generation of protection relays was born in 1905 and consisted of a simple overcurrent and undervoltage electromagnetic apparatus. Then, the invention of transistors in 1947 has made possible the mutation of relay technology from electromechanical to static or solid-state, introduced into service in the mid fifties. Around 1980, with the advent of the digital era, the technology employed to construct such devices has been significantly improved and has led to the era of digital protection relays. Compared to static devices, digital relays have access to the analogue-to-digital conversion, microprocessors to implement their protective algorithms, and communication features to send information to a remote computer. However, within the next five years, this technology has been superseded by numerical relays, often considered as the natural development of digital relays, mainly due to the very fast evolution of microprocessors. Specifically, they use a Digital Signal Processor (DSP) optimized for signal processing applications. Obviously, each change of technology has brought with it reductions of relays size and weight, and improvements in terms of functionality and reliability as the same time. Today, numerical relays widen the gap with respect to anterior technologies by offering remarkable features such as the capability to include a large number of protection algorithms, to record waveforms of the power systems in case of fault, and to monitor the circuit breaker state.

Numerical relays involve digital processing techniques to detect power system abnormal conditions. To reach this target, five basic steps are performed [RSW11b]:

1. filtering of the input analogue signals to remove the high frequency components corrupting the digital signals ;
2. sampling and converting the analogue signals into trains of samples through the use of an Analogue-to-Digital Converter (ADC) ;
3. digital filtering of the sample streams to extract the exact frequency component of interest ;
4. measuring of the parameters that are used by protection algorithm like magnitude and phase angle ;
5. generating the protection decisions which are based on comparing criteria values with pre-set thresholds or other characteristics.

The internal clock of the ADC can be connected to a external time source so that synchronization of measurements can be achieved over great distance. This concept has been introduced in 1988 with the invention of the phasor measurement units by Arun G. Phadke and James S. Thorp at Virginia Tech University [Bhi14]. The synchronization of the measurements makes possible monitoring of the grid in real-time and other applications related to the protection field such as islanding detection and adaptive protection system might also be envisaged. It is the area of Wide-Area Measurement and Protection Systems (WAMPS) which combine advanced digital processing methods with the fast and reliable exchange of information via telecommunication links [RSW11b] in view of detecting and further counteracting grid instabilities.

The communication technology is part of the smart grid cornerstones to manage electricity in a more reliable, secure and sustainable manner. To reduce installation costs and promote competition among manufacturers of relays, it is necessary that protection, measurement and control devices of various vendors must communicate and understand each other. The introduction of common communication standard such as IEC Standard 61850 for communication within and intra-substation(s) can solve the issue [RSW11b]. Among the communication services offered by the product family standard, the Sampled Measured Values (SMVs), absolute time-stamped digitized analogue values transmitted through an Ethernet network, substitute the traditional hard copper wires which establish the link between instrument transformers and the protection, measurement, and control devices. These frames are produced by specific equipments called Merging Units (MUs). Protection relays using SMV frames as input signal must deal with data generated through a fixed sampling clock whereas they traditionally track the power system frequency and continuously adjust their internal sampling clock to exact multiples of the system frequency so that to maintain calculation accuracy during frequency excursions. Furthermore, the latter are of main concern in the context of massive penetration of distributed generation in the distribution grids. Indeed, frequency and Rate-Of-Change-Of-Frequency (ROCOF) relays are, nowadays, the most commonly employed anti-islanding methods but their performance is not satisfactory because they are not able to provide accurate frequency and ROCOF estimations under dynamics.

In the light of the above, the general objective of this dissertation is to design an innovative protection relay on the basis of SMV frames to deal with the Smart Grid paradigm. To achieve this target, several steps should be taken. They are listed below:

1. Investigate the behavior of the Merging Unit and its consequences on the protection relaying field ;
2. Propose a method to design a Merging Unit capable of generating SMV frames with high accuracy ;
3. Compare methods able to measure accurately the power system current and voltage magnitude and phase angle information ;
4. Improve the accuracy with which protection relays estimate the frequency and the ROCOF ;
5. Determine the conditions required to provide protection relays the capability to compute synchrophasors.

To fulfill the aforementioned objectives, this thesis is organized as it follows. Chapter I essentially relies on the understanding of the methods of operation in used within modern numerical protection relays, from the acquisition chain to the signal processing methods. Most of the relays involve the Discrete Fourier Transform (DFT) to estimate parameters of interest of the power systems through phasors so that it becomes possible to process the protection algorithms. The main drawbacks of the DFT are reviewed and the traditional techniques used to minimize the undesirable effects of the DFT are also presented. Finally, a detailed description of the phasor measurement unit (PMU) is provided. Chapter II is structured around the main problematic related to the use of SMV by protection relays and

PMUs from the signal processing perspective. The issues are raised from a deep analysis of the IEC Standard 61850 and its evolutions. A new data acquisition chain, considering the requirements imposed by the aforementioned standards, is then proposed to compute SMV frames with high accuracy. On the basis of these SMV frames, three innovative algorithms are then proposed to estimate phasors under static and dynamic conditions with an emphasis put on frequency excursions (Chapter III). This chapter ends with an analysis of simulation results to assess the performance of the proposed algorithms. Finally, Chapter IV aims at proposing a synchronized phasor measurement algorithm for the next generation of protection relays. This algorithm is merged into the signal processing path dedicated to protection functions so that to optimize the computational burden required to execute the synchrophasor algorithm. The algorithm is tested via simulation and the results obtained compared to the exigencies of the PMU standard. Finally, a general conclusion is provided at the end of this manuscript summarizing the main outcomes obtained.

Chapter I

The phasor estimation process and its current applications: state of the art

Contents

Abstract

This chapter gives an overview of protection relays and phasor measurement units from the signal processing perspective to estimate phasors in an accurate manner. The overview concerns the signal processing algorithms as well as the data acquisition chain. The main issues encountered to obtain accurate estimation of phasors are described in details and the solutions widely employed to tackle these issues are presented.

1 Introduction

Accurate estimation of phasors is the foundation of protection relays and phasor measurement units. For relays, they are given to protection algorithms which detect abnormal system operations. For PMUs, the measurements are time-stamped to a common time synchronization signal which permits, by aligning the timestamps, to obtain a coherent picture of the state of the power system [DCPI04].

Advances in electronic engineering and high-speed communications have made precise time synchronization in the power grid more practical and cost-effective. The emergence of Global Positioning System (GPS) technology brought the solution to the power system wide area measurement. It is shown that the GPS offers the most effective way of synchronization power system measurements over great distances. Through the use of GPS, time synchronization of better than 1 microsecond is now performed [HJYZ14].

The numerical nature of relays and PMUs highlights that they involve a sampling process to allow phasor representation of their input signals. The sampling strategy differs from one device to another. Indeed, the internal time clock of the PMU must be connected to the GPS to have time synchronization, which means that the input will be sampled at constant time interval, and this time interval will be the same for all of the PMUs. However, sampling the input data at constant time intervals is typically not the preferred solution for protection relays because it can introduce errors in their protection functions [BSG04]. Most of the protective relays change the sampling frequency to be synchronized with the measured off-nominal frequency, which means that the sampling rate is constantly changing as the power frequency varies. In addition, synchronization to the GPS is not necessary for relays since the protection algorithms can operate without it.

In the light described above, this chapter starts to describe the main method employed by numerical protection relays to estimate the phasors. A brief overview of common relays architecture is then given so that to highlight the main challenges they faced to accurately estimate the phasors. One of these challenges relies on accurate phasor estimations during frequency excursions. The impacts of off-nominal frequencies on phasor estimation algorithms are mathematically explained and illustrated. A review of the two main methods typically used by relays to estimate phasors with high accuracy under frequency deviations is then given. These methods require that the power system frequency is measured in real-time. Consequently, two common frequency estimation techniques employed by relays are explained. The last section of this chapter is structured around the PMU, starting with the description of the evolution of its related standard and ending with signal processing approaches that are used to obtain synchronized phasor measurements.

2 Mathematical background for the phasor estimation process

Protection relays incorporate several protective algorithms which are designed to respond to specific power system frequency components (fundamental and/or harmonics) brought by their input signals. Most of the protection elements react to the fundamental frequency (overcurrent, undervoltage, distance...) but some others require particular harmonic measurements (2^{nd} harmonic for transformer inrush protection, 3^{rd} harmonic for stator ground fault protection,...) or an estimate of the harmonic content on a large band (for thermal protection). Obviously, the measurement of the relevant information shall be accurate enough as it is further used by the protection elements in charge of discriminating normal system operations against faulty operations. Indeed, protection relays have to operate following the occurrence of a fault during which, in case of short-circuit, the sine wave of fundamental frequency can be corrupted by Direct Current (DC) offset, harmonics, and high frequency components. Thus, to increase the accuracy of their estimates and make sure that the useful information is not corrupted by the other signal components, protection relays generally involve a filtering process that preserves the quantity of interest while rejecting other components.

Once the signals have been properly filtered, numerical relays typically compute their phase vectors, or phasors, which remain the dominating tool over the years. Phasors, conceptualized by Charles Proteus Steinmetz in 1893 [Ste94], is a complex number that gives the magnitude and the phase angle of a sinusoidal signal whose amplitude, frequency, and phase are time invariant. Under this definition, the sinusoidal signal:

$$x(t) = X_m \cos(\omega t + \varphi) \tag{I.1}$$

where:

X_m	is the peak value of the signal $x(t)$
ω	is the angular frequency, $\omega = 2\pi f$ being f the frequency
φ	is the initial phase angle of $x(t)$

can be written as:

$$x(t) = \Re\{X_m e^{j(\omega t+\varphi)}\} = \Re\{e^{j\omega t} X_m e^{\varphi}\} = \Re\{X_m e^{\varphi}\} \tag{I.2}$$

Reminding that the Root Mean Square (RMS) values are useful to compute the electrical power flows, the phasor $\overline{X}$ of $x(t)$ is expressed as shown:

$$\overline{X} = \frac{X_m}{\sqrt{2}} e^{j\varphi} \tag{I.3}$$

It is important to note that the concept of phasor remains valid for any invariant frequency. It is therefore particularly useful for microprocessor-based relays since it is applicable for the fundamental frequency and the harmonics. This is the reason why numerical relays typically compute phasors for most of their protection algorithms. On the

other hand, the filtering process can be coupled with the phasor computation in such a way that both operations are performed one after the other. The pairing is called phasor estimation algorithm. A phasor estimation algorithm is evaluated with respect to several criteria which are commonly:

— the immunity to harmonics,
— the immunity to off-nominal components,
— the immunity to frequency shifts,
— the immunity to noise,
— the immunity to DC offset,
— the response time which has to be short,
— the transient behaviour which is expected to be good,
— the computational burden which should be minimal [Ben95].

Of course, the perfect phasor estimator that can handle all the aforementioned criteria does not exist. The selection of such estimator is often a matter of compromise between the responsiveness of the protection relay, its reliability and its precision. Today, phasors estimation of marketed relays is widely based on the Discrete Fourier Transform.

2.1 The Discrete Fourier Transform

On December 21, 1807, Jean Baptiste Joseph Fourier, French mathematician and physicist, presented his paper "On the Propagation of Heat in Solid Bodies" to the *Institut de France* to defend his studies related to heat flow [New10]. In this paper, he claimed that any continuous periodic signal can be decomposed into an infinite summation of sine and cosine waves [Fou22]. This is based on the assumption that a signal is composed of a fundamental frequency and its harmonics. Such decomposition is called Fourier Series (FS) and is part of the Fourier Transform (FT) family. The FT is actually a general term which can be split up into four categories ; each category belonging to one of the four basic types of signals encountered in many applications:

Periodic-Continuous: As discussed previously, the Fourier Transform of a periodic-continuous signal is called the Fourier Series.

Aperiodic-Continuous: The technique of expressing any continuous time function, non necessarily periodic, as a sum of sine and cosine waves is simply called the Fourier transform.

Periodic-Discrete: Following the same logic of its continuous pair, the FT is named here the Discrete Fourier Series (DFS) and is applied for discrete signals.

Aperiodic-Discrete: This type of FT designates the Discrete Time Fourier Transform (DTFT).

In order to understand the DFT approach, let us start with the FT. In its formulation, the FT regroups the sine and cosine trigonometric functions into a simple exponential term by the use of Euler's formula. By doing this, the FT can be written as:

$$X(\omega) = \int_{-\infty}^{+\infty} x(t) e^{-j\omega t} \, \mathrm{d}t \tag{I.4}$$

where:

$X(\omega)$ is the spectrum of the signal $x(t)$

The numerical nature of modern protection relays involves digital signal processing techniques. The computations are thus performed in the discrete-time domain, considering some data obtained through the sampling process as deeply explained in Section 3.4. Up till now, it is sufficient to admit that a discrete signal is created by taking *snapshots* of a given continuous signal at specific, discrete, instants of time. The snapshots are called samples and represent a sequence of number which can be processed by digital signal processing techniques. Based on that, it is clear that Eq. (I.4) cannot be used by protection relays as the FT does not consider discrete signals whereas DTFT is defined for that purpose. Considering an infinite length of samples $x_i[n]$, the DTFT is expressed as:

$$X(\omega) = \sum_{n=-\infty}^{+\infty} x_i[n] e^{-j\omega n} \tag{I.5}$$

where:

n is the sample index, $n \in \mathbb{Z}$

Naturally, it is unrealistic for a given processor to perform an infinite summation of samples which means that the implementation of Eq. (I.5) into a microprocessor-based relay is not possible. To overcome this issue, along the infinite length of samples $x_i[n]$, a small portion of the signal must be extracted. This extraction is performed by the use of a discrete windowing function $w[n]$. The finite length sequence $x[n]$ now exists for a duration N. The truncation of the sequence $x_i[n]$ into a limited number of samples $x[n]$ yields the DFT whose general formulation is given in Eq. (I.6).

$$\overline{X(k)} = \frac{1}{G} \sum_{n=0}^{N-1} w[n] x[n] e^{-j\frac{2\pi}{N}nk}, \qquad 0 \leq k \leq N-1 \tag{I.6}$$

where:

k is the harmonic number under analysis
G is the gain of the observation window, $G = \sum_{n=0}^{N-1} w[n]$

The general formulation of the DFT points out several important characteristics. First of all, it is not necessary that the sample set $x[n]$ to be periodic to compute its representation in the frequency domain. However, as discussed in Section 4, errors are introduced in the DFT estimates if the signal is not periodic in the data window. In the following explanation, without loss of generality, the signal under analysis is assumed to be a pure cosine wave of fundamental frequency. Thus, the DFT shall be tuned to the fundamental frequency, that is $k = 1$, to estimate the phasor of fundamental. Based on this, a DFT

expressed as Eq. (I.6) is also known as a full-cycle DFT where N samples have been generated over 1 full cycle of cosine wave. Moreover, in the specific case where the simplest rectangular windowing function is used, defined as,

$$w[n] = \begin{cases} 1 & \text{if } 0 \leq n \leq N-1, \\ 0 & \text{otherwise} \end{cases} \tag{I.7}$$

the gain G is equal to N and the exact phasor computation can be obtained by multiplying Eq. (I.6) by the factor $\sqrt{2}$ (the DFT bins of the cosine sequence in such a configuration is equal to $X_m/2$). Now, if the cosine wave in Eq. (I.1) is sampled N times per fundamental cycle, its representation in the discrete-time domain is given by the sample set

$$x[n] = X_m \cos(\frac{2\pi}{N}n + \varphi) \tag{I.8}$$

and, considering a rectangular window, the phasor of the fundamental frequency is computed using Eq. (I.6) with $k = 1$ and the factor $\sqrt{2}$ as shown:

$$\begin{aligned} \overline{X(1)} &= \frac{\sqrt{2}}{N}\sum_{n=0}^{N-1} x[n]\cos(\frac{2\pi}{N}n) - j\frac{\sqrt{2}}{N}\sum_{n=0}^{N-1} x[n]\sin(\frac{2\pi}{N}n) \\ &= X_{\Re} - jX_{\Im} \end{aligned} \tag{I.9}$$

where:

$$X_{\Re} = \frac{\sqrt{2}}{N}\sum_{n=0}^{N-1} x[n]\cos(\frac{2\pi}{N}n) = \frac{X_m}{\sqrt{2}}\cos\varphi \tag{I.10}$$

$$X_{\Im} = \frac{\sqrt{2}}{N}\sum_{n=0}^{N-1} x[n]\sin(\frac{2\pi}{N}n) = -\frac{X_m}{\sqrt{2}}\sin\varphi \tag{I.11}$$

Substituting Eq. (I.10) and Eq. (I.11) in Eq. (I.9) gives the expected phasor $\overline{X(1)} = (X_m/\sqrt{2})e^{j\varphi}$. In other words, for a cosine wave of fundamental frequency, the phasor of the fundamental is obtained simply by applying the DFT coefficients on the input samples.

From the protection relays perspective, the DFT-based algorithm is implemented by using Finite Impulse Response (FIR) filters [Yal97]. The idea is to perform the computation at sample m on the basis of N historical samples (samples which have been stored in the memory). For the k^{th} order harmonic, the response $y_k[m]$ of the FIR filter with coefficients $h_k[n]$ is given by the following expression:

$$y_k[m] = \sum_{n=0}^{N-1} h_k[n]x[m-n] \tag{I.12}$$

where:

$y_k[m]$	is the output sample for harmonic k
$x[m-n]$	is the input sample set (stored samples)
$N-1$	is the filter order (N number of taps)
$h_k[n]$	are the filter coefficients

The coefficients $h_k[n]$ are directly related to the real and imaginary parts of the complex exponential of the DFT: they approximate the cosine and sine functions. Thus, two orthogonal FIR filters are required to perform the DFT filtering operation for the k^{th} order harmonic. For a given harmonic k, the expression of the orthogonal filters are given below:

$$h_{k,c}[n] = \frac{\sqrt{2}}{N} \sum_{n=0}^{N-1} \cos(\frac{2\pi}{N} nk) \tag{I.13}$$

$$h_{k,s}[n] = \frac{\sqrt{2}}{N} \sum_{n=0}^{N-1} \sin(\frac{2\pi}{N} nk) \tag{I.14}$$

The FIR filters expressed in Eqs. (I.13) and (I.14) are respectively called "full-cycle cosine filter" and "full-cycle sine filter". Their frequency response can be evaluated for each harmonic by multiplying Eqs. (I.13) and (I.14) by the complex exponential $e^{-j\omega n}$ as shown:

$$H_{k,c}(e^{j\omega}) = \frac{\sqrt{2}}{N} \sum_{n=0}^{N-1} \cos(\frac{2\pi}{N} nk) \cdot e^{-j\omega n} \tag{I.15}$$

$$H_{k,s}(e^{j\omega}) = \frac{\sqrt{2}}{N} \sum_{n=0}^{N-1} \sin(\frac{2\pi}{N} nk) \cdot e^{-j\omega n} \tag{I.16}$$

By taking the absolute values of $H_{k,c}(e^{j\omega})$ and $H_{k,c}(e^{j\omega})$, it is possible to plot the magnitude response for each harmonic. An example is given in Fig. I.20 for $k = 1$ (phasor of the fundamental component) and $N = 48$, a common number of samples per cycle found in protection relays. It should be noted that the pulse frequencies have been converted to harmonic number for sake of simplicity. The magnitude responses are continuous since they have been evaluated for pulse frequencies with a step of 2π rad/s.

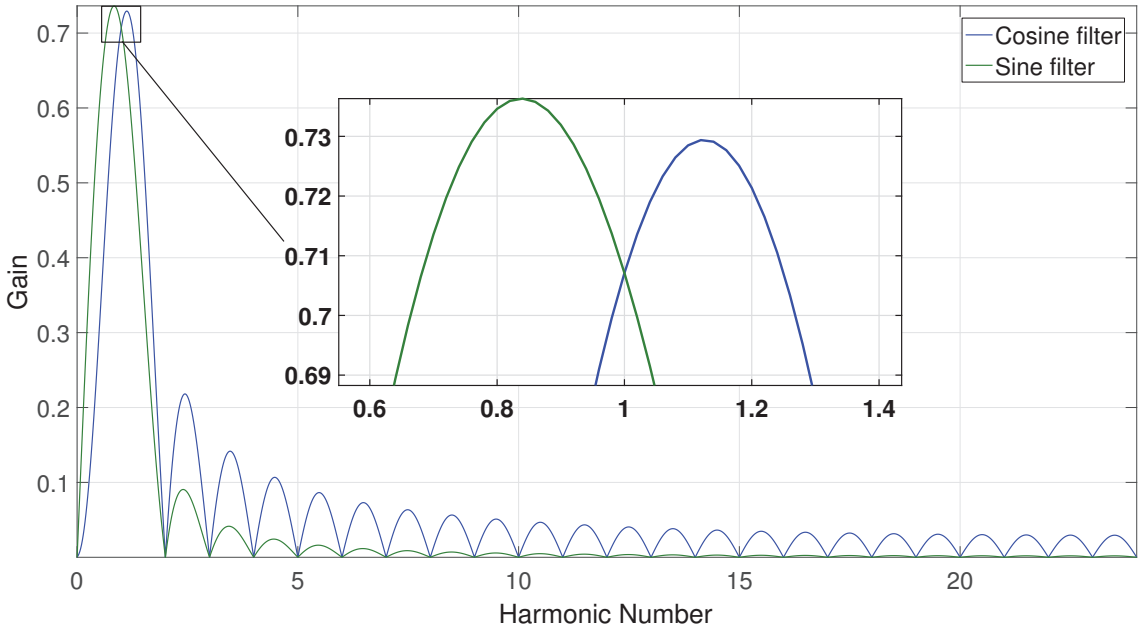

FIGURE I.1 – Cosine and sine filters magnitude responses

Figure I.20 shows that the cosine and sine filters have band-pass magnitude responses with a gain equal to $1/\sqrt{2}$ exactly for the fundamental frequency. Moreover, since the gain is exactly 0 at DC (supposed to be a constant) and harmonics levels, the filters are able to reject this unwanted components if they are superimposed to the fundamental frequency. Once the inputs signals have been passed through the full-cycle sine and cosine filters, the magnitude and the phase angle can be computed as shown in Figs. I.2 and I.3, adapted from [Wan99].

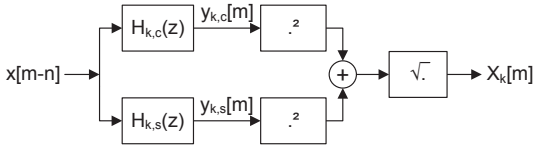

FIGURE I.2 – Microprocessor-based relay magnitude estimation algorithm

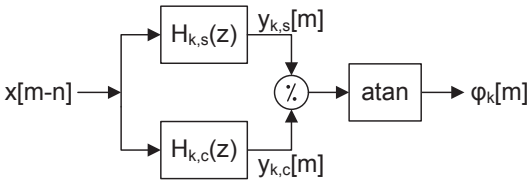

FIGURE I.3 – Microprocessor-based relay phase estimation algorithm

2.2 Non-DFT phasor estimators review

The full-cycle DFT filter is widely used in modern relays for several reasons. First, it is able to reject the DC and all harmonics. Then, it can tolerate small frequency excursions as reflected in its bandpass characteristics. Finally, it is fast, accurate and presents a good transient response. Several other algorithms have been proposed over the years to challenge the performances of the DFT-based algorithm. Among them, the Infinite Impulse Response (IIR), Least Error Squares (LES), and Kalman filters have been proposed. These non-conventional filters have been extensively compared to the DFT but no one has succeeded in replacing it. A brief overview of the weaknesses of the aforementioned methods is given below.

IIR filters: In contrast to FIR filters, the outputs of IIR filters depends, by nature, on the entire input history. Thus, in case fault, the IIR filter will be less sensitive than the FIR filter is as the IIR filter window always contains pre-fault data. This, in fine, will inevitably delay the detection of the fault and jeopardy the stability of the power system.

LES filters: The basic idea of the LES technique consists in minimizing the mean-square error between the actual waveform and a mathematical model of this waveform. Most often, the model includes the decaying DC offset, the fundamental frequency component, and the harmonics of specified orders [SN91]. If the considered waveform corresponds to its mathematical model, then the LES algorithm is very accurate. However, as shown in [Wan99], the frequency response of a LES-based filter depicts that its upper boundary is higher than the one of DFT filter which means that more errors are introduced in the phasor estimates.

Kalman filters: The Kalman filter can be seen as a generalized version of the LES filters and therefore needs a signal model. In its model, all possible unwanted components that are intended to be filtered out by the Kalman filter must be considered to obtain accurate phasor measurements. If a component has not been properly modeled, then

this component will be squeezed into the fundamental and the harmonics by the filter which results in degrading phasor estimations. Moreover, the Kalman filter requires a high computational effort compared to the DFT as stated in [SH93] where the modeling of the noise, DC, and 2^{nd} and 3^{rd} harmonics have cost 13 times more basic operations than the DFT.

Following the above description, it can be concluded that alternatives of DFT-based algorithms exist but are not adapted to protection relaying. This is the reason why the study will focus on the DFT only.

3 Microprocessor-based relays architecture

Microprocessor-based relays are aimed at detecting faults and other abnormal power system operations by analyzing the voltage and current waveforms brought to their inputs. Once the fault is recognized, the relays send a trip signal to the circuit breaker(s) which open its pole(s) according to the signal received. The isolating operation is thus physically performed by the circuit breaker which is part of the protection system in which the numerical relay is the "brain". Naturally, such numerical devices cannot process the hundreds of kilovolts and kiloamperes at which the overhead lines and underground cables are functioning. Instead, these signals are stepped-down in levels suitable for the relays by instrument transformers (ITs) which are installed in the substations. Voltage transformers (VTs) or capacitive voltage transformers (CVTs) reduce the voltage to typically 67 V rms (phase-to-ground) whereas current transformers (CTs) decrease the current to 1 or 5 A rms at nominal operation. The protection system, involving the three aforementioned main components, that is numerical relay, ITs, and circuit breaker, is depicted in Fig. I.4, adapted from [Ste09] where the basic architecture of the microprocessor-based relay is also shown. The architecture of microprocessor-based relay can be split into 3 major categories. The very first category relies on the accurate measurement of the power system voltages and currents through the acquisition chain starting from the interposed CTs and VTs, discussed in Section 3.1, and ending to the ADC in charge of converting and representing the analogue signals into a sequence of numbers called samples. After being converted, the samples can be processed by digital signal processing techniques during which specific estimations of the power system state are performed (computation of phasors) and protection algorithms are executed. The set of the numerical programs where all protective decisions are performed is called the firmware. Finally, the last category belongs to the communication with the external world through which digital Inputs and Outputs (I/Os), the Human Machine Interface (HMI), and specific communication protocols are used. The opto-isolators can be used to give the status of the circuit breaker to the relay whereas digital outputs are mapped to the output contacts to send tripping signals to the circuit breaker. The HMI allows the relay user having a quick access to various relay parameters like configuration settings and status of digital I/Os and to measurements performed by the device. The necessity of communication protocols will be greatly discussed in Chapter II where the major problematic of this study is highlighted. In a nutshell, protection relays are an essential component of the Substation Automation System (SAS) because they contain valuable data which are required by many user groups within the utility. As

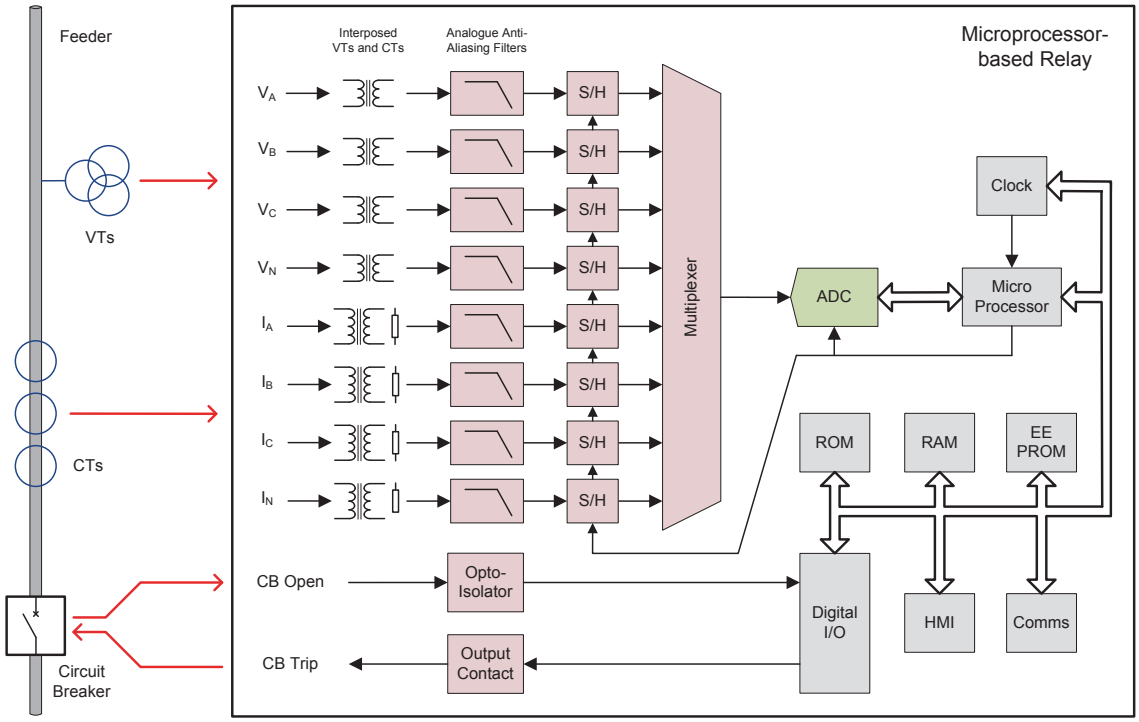

FIGURE I.4 – Microprocessor-based relay involved in the protection system

such, protection relays, like the other Intelligent Electronic Devices (IEDs) of the SAS, integrate several communication protocols in order to exchange their data with the Supervisory Control And Data Acquisition (SCADA) system mainly.

Since this study mostly deals with the algorithmic part of the future numerical protection relay, a few words about the firmware is useful to get the general idea about its organization. The central component of the relay firmware, and even the relay itself, is the microprocessor because it is responsible for the execution of protection algorithms and communicating with its peripheral equipment. The three types of memories which have been represented in Fig. I.4 are essential elements of the relay because each of them responds to a particular demand. The Read Only Memory (ROM) contains the relaying programs to be executed. These algorithms are stored permanently and cannot be erased even if the relay is not turned on. Their execution can be performed directly from there if the memory access is suitable for real-time execution. If not, the program instructions are copied from the ROM into the Random Access Memory (RAM) during an initialization process (shadowing) where they are executed. This is usually done because the RAM is faster than the ROM, sometimes as much as more than 15 times. Additionally, the RAM is used to store the samples coming from the ADC before they are processed by the algorithms. Moreover, microprocessor-based relays need to be configured prior to their installation in the substation. The configuration process is performed through the setting file which must be adjusted according to the network topology. Naturally, once the relay is configured, it is expected that the settings are kept in memory to avoid the reconfiguration of the relay in case it is turned off. To do so, the setting file is stored in the Electrically-Erasable ROM (EEPROM), a non-volatile programmable memory. It should

be noticed finally that the clock shown in Fig. I.4 is of primary concern and the backbone of this study. Synchronizing this clock with an absolute time reference is a base for several applications like the PMU discussed in Section 7.

The following subsections describe the Data Acquisition System (DAQ) and the main challenges to overcome when dealing with DFT-based estimator.

3.1 Interposed current and voltage transformers

Interposed (or auxiliary) current and voltage transformers are the primary elements of the protection relay DAQs. There are used for two main reasons. Firstly, their transformer ratio scales down the primary signal levels to admissible values required by the ADC. Indeed, ADCs typically works at a voltage level of ±10 volts which is 10 times below the secondary of the conventional VTs of the power system. Furthermore, the outputs of auxiliary CTs need to be converted to voltages before being processed by the ADC. The transformation of current into voltage is performed through a resistive shunt connected to the secondary of auxiliary CTs as shown in Fig. I.4. Secondly, interposed ITs provide galvanic isolation. Such an analogue isolation protects the ADC from transient or high voltages but adds a nonlinear gain and some offset errors to the signal before being converted [Ins15]. To understand the impacts of the distortions introduced on the analogue signals, let us focus on the interposing CT equivalent circuit referred to secondary side illustrated in Fig. I.5 [1].

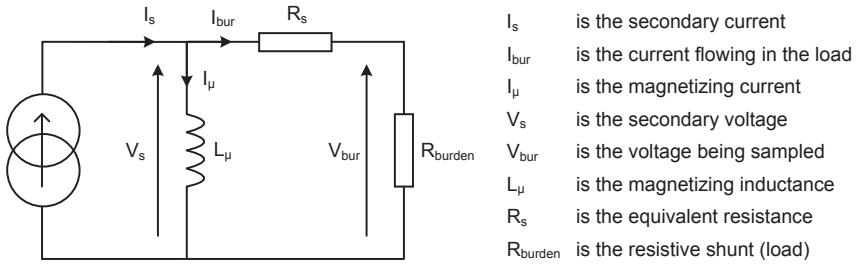

FIGURE I.5 – Interposed CT equivalent circuit referred to secondary side

Let $R_t = R_s + R_{burden}$. The transfer function $H_{CT}(s)$, associated to the schematic of the interposed CT shown in Fig. I.5, can be computed as following:

$$H_{CT}(s) = \frac{V_s(s)}{V_{bur}(s)} = \frac{sL_\mu}{R_t + sL_\mu} = \frac{\frac{s}{\omega_c}}{1 + \frac{s}{\omega_c}} \tag{I.17}$$

where:

ω_c is the cutoff frequency in rad/s

In first approximation, Eq. (I.17) shows that the auxiliary CT can be assimilated to a 1^{st} order high-pass filter whose cutoff frequency is $f_c = R/(2\pi L_\mu)$ Hz. Therefore, the number of windings and the load should be carefully selected so that the cutoff frequency

1. The secondary side inductance and the core loss equivalent resistance have been neglected

is as low as possible to avoid notching out frequencies of interest. Interestingly, R_{burden} is a key differentiator used to reject the DC component in the fault current. This is a benefit to maintain accurate phasor measurements under faulty conditions. An example of the frequency response representation is given in Figs. I.6 and I.7 where $R_s = 42.5\Omega$, $R_{burden} = 5.5\Omega$, and $L_\mu = 390$ mH. These values correspond to the characteristics of one auxiliary CT found in the study performed in [CG13].

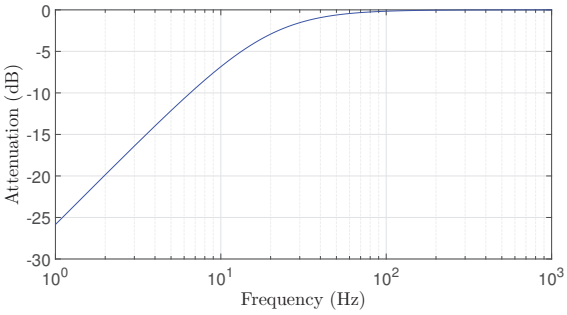

FIGURE I.6 – Example of CT auxiliary magnitude response

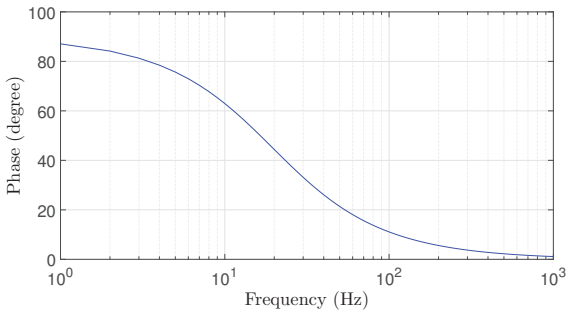

FIGURE I.7 – Example of CT auxiliary phase response

Referring to Figs. I.6 and I.6, the attenuation is about 0.9311 at 50 Hz and the phase shift introduced in 21.39 degrees. Similarly, at 60 Hz, the attenuation is approximately 0.9506 while the phase shift is 18.08 degrees. Since the errors can be characterized, they can be corrected during a calibration procedure. Typically, the calibration procedure is performed at the fundamental frequency (50 and 60 Hz) for each harmonic used by protection algorithms. Regarding the phase shift, assuming that the auxiliary CTs are identical for the three-phase currents, there is no need to apply compensation as the current waveforms are shifted by the same amount. If the CTs are not exactly the same, it is necessary to perform a phasor rotation in software to ensure a phase shift of 120 degrees between the phases. Clearly, if the cutoff frequency is set as low as possible, the errors introduce in the magnitude and phase angle are minimized and can be disregarded. Once the signals have been properly adapted to the admissible voltage levels and calibrated, they are sampled for the digital processing.

3.2 The sampling process and its consequences

The sampling process consists in taking samples on an analogue continuous-time signal ; the samples representing the amplitude of the signal at the instant when the samples have been taken. This is performed by Sample and Hold (S/H) circuits. In most cases, the samples are obtained with a fixed periodicity T_s called the sampling period. The number of samples generated in 1 second refers to the sample rate, or sampling frequency, $F_s = 1/T_s$, expressed in Hz. Clearly, the continuous variable t cannot be used anymore in the discrete-time domain as the resulting samples exist only at specific instant related to the sampling interval as shown:

$$t = nT_s, \qquad n \in \mathbb{Z} \tag{I.18}$$

This points out the fact that the sampling process ignores what happens between two consecutive samples. Thus, reminding that it is impractical to sample to an arbitrary high sample rate the input signal, one may naturally wonder whether the samples obtained are enough representative of the analogue signal or not. In other words, what should be the minimum value of F_s to guarantee that the information brought by the analogue signal is kept after being sampled ? Actually, the response of this question can be formulated as it follows: is it possible, from the samples, to reconstruct the analogue signal without loss of information ? To answer this question, the start point is the mathematical model of the sampling process.

First, let us assume that the signal $x(t)$ has a spectrum which is naturally band-limited to the frequency f_{max}, that is: $X(f) = 0$ for $f > f_{max}$. This limitation may be also artificial by the use of specific filters as shown later in Section 3.3. In the time-domain, the sampling process is tantamount to multiplying the signal $x(t)$ by series of unit impulses. As a result, the signal obtained is composed of successive impulses whose amplitude is modulated by the amplitude of the sampled signal. Besides, the aforementioned series of unit impulses is called the Dirac comb (or impulse train) which consists of an infinite series of Dirac delta functions δ equally spaced by the sampling interval T_s, that is:

$$\text{Ш}_{T_s} \overset{\text{def}}{=} \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{I.19}$$

Based on Eq. (I.19), considering that the sampling process is ideal, i.e. the samples are generated instantaneously at $t = nT_s$ ("Hold" function is disregarded), the sampled signal $x_s(t)$ can be written as shown:

$$\begin{aligned} x_s(t) &= x(t) \times \text{Ш}_{T_s} \\ &= x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \\ &= \sum_{n=-\infty}^{\infty} x(nT_s)\delta(t - nT_s) \end{aligned} \tag{I.20}$$

An ideal sampling process involving infinitely small pulses can only be partially achieved. In practice, the pulses exist for a small duration of time τ_p during which the signal is held at a constant amplitude ("Hold" function is considered). The "real" sampled signal will be thus composed of an impulse train periodic with a period T_s and a pulse width τ_p. The amplitude of these pulses is function of the sampling procedure employed, whether regular or average. The regular sampling process is characterized by amplitudes equal to the input signal at the instant it has been sampled during the duration τ_p (see Fig. I.8). The average sampling process involves amplitudes equal to the mean of the input signal in the time interval τ_p (see Fig. I.9). The consequences of both sampling procedures on the spectrum are analyzed in Appendix A. In particular, if the pulse width is small compared to the highest frequency component of the input signal, the regular and average sampling procedures can be approximated by the ideal sampling process. Assuming that this hypothesis is fulfilled, the analysis can be pursued considering the ideal sampling process.

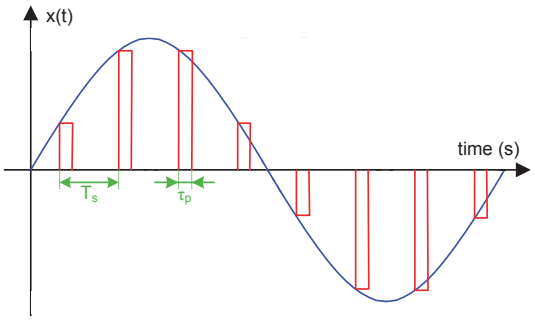

FIGURE I.8 – Regular sampling procedure example

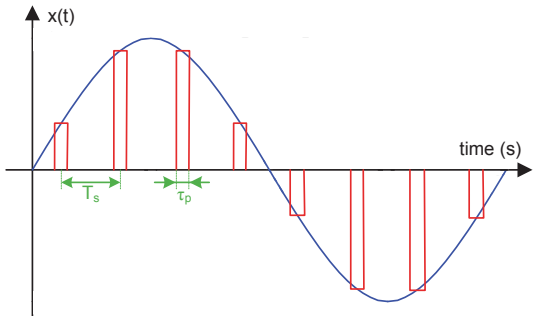

FIGURE I.9 – Average sampling procedure example

In Eq. (I.20), the sampling process has been defined in the time-domain. Nevertheless, it is necessary to write Eq. (I.20) in the frequency-domain to understand the impact of the sampling on the spectrum. By doing this, the spectrum of the sampled signal $X_s(f)$ can be compared to the one of the input signal $X(f)$. If the spectrum are identical, it means that the sampled signal contains the same information as the input signal. To do so, the use of the DTFT is required. Reminding that the DTFT of the Dirac comb is also a Dirac comb in the frequency-domain, the spectrum of the sampled signal can be written as:

$$\begin{aligned}\mathcal{F}\{x_s(t)\} = X_s(f) &= \mathcal{F}\{x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s)\} \\ &= X(f) * [F_s \cdot \sum_{m=-\infty}^{\infty} \delta(f - mF_s)] \\ &= F_s \cdot \sum_{m=-\infty}^{\infty} X(f - mF_s) \end{aligned} \tag{I.21}$$

where:

$*$ denotes the convolution product

Thus, Eq. (I.21) shows that the spectral content of a signal sampled ideally is composed of the signal spectrum at $f = 0$ and its replicas shifted by F_s in the positive and negative frequency sides. This phenomenon is known as periodization of the spectrum. For $f = 0$, the spectrum is called the baseband portion of $X_s(f)$ while the remaining spectra are the frequency-translated portions of $X_s(f)$. Figure I.10 represents in both the time-domain and the frequency-domain, the process of sampling the signal $x(t) = 2\cos(2\pi f_{max} t)$ to a frequency $F_s = 6 \times f_{max}$ [2]. In contrast to the spectrum $X(f)$, band-limited to the frequency f_{max}, the spectrum of the sampled signal $x_s(t)$ is unbounded since the periodization of the spectrum is defined for $f \in]-\infty; +\infty[$. Moreover, as shown in Fig. I.10, the initial information contained in $x(t)$ is kept after the sampling process as the baseband portion and the frequency-translated portions have the same spectrum shape. This is actually made possible because F_s is high enough to avoid any overlapping between the patterns.

2. The synchronous sampling condition is satisfied

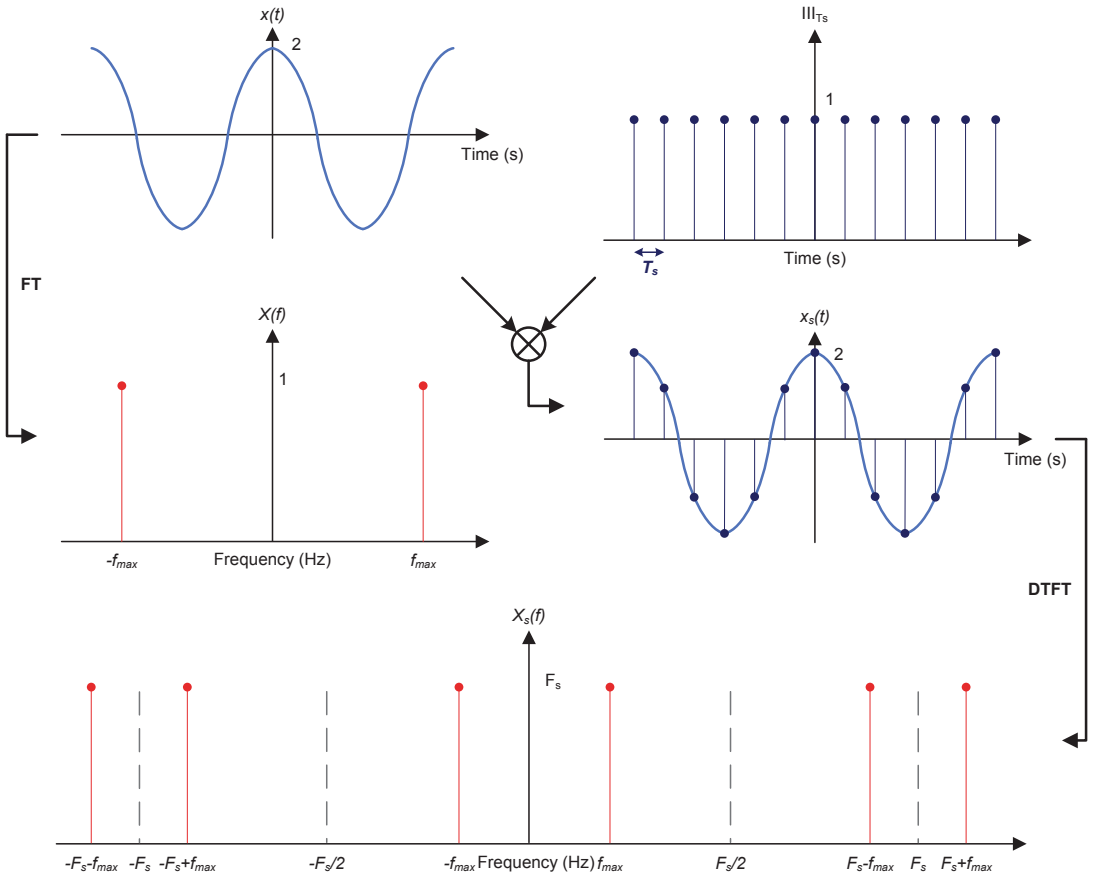

FIGURE I.10 – Illustration of the periodization of the spectrum

A deeper look on the X-axis points out that it exists a minimum value of F_s for which the periodization of the spectrum is performed without overlapping. This condition refers to the famous *sampling theorem* also known as *Nyquist-Shannon theorem* which is given below:

Theorem 1. *Consider a periodic continuous signal $x(t)$ band-limited to a bandwidth $\Omega_{max} = 2\pi f_{max}$ rad/s. The sampling rate must be greater than twice the highest frequency to permit the perfect reconstruction of the signal $x(t)$ without loss of information, that is:*

$$F_s \geq 2 \cdot f_{max} \tag{I.22}$$

As said previously, if the initial signal $x(t)$ may be retrieved from $x_s(t)$, then it means that the sampling theorem is fulfilled. Actually, the reconstruction of the signal $x(t)$ may be obtained by isolating the baseband portion $X_{sb}(f)$ from the frequency-translated portions and then performing an inverse Fourier transform computation. The process of isolation is done by the use of an ideal low-pass filter whose cut-off frequency f_c is equal to $F_s/2$. The frequency $F_s/2$ is called the Nyquist frequency (or Shannon frequency). The function performed by such a filter, assimilated to the rectangular window, is mathematically written $\Pi_{F_s}(f)$. Based on that, $x(t)$ can be recovered by following the mathematical derivation of

the sampling process but in the reverse order starting from the baseband of $X_s(f)$:

$$\begin{aligned}\mathcal{F}^{-1}\{X_{s,b}(f)\} = x_{s,b}(t) &= \mathcal{F}^{-1}\{X_s(f)\cdot\Pi_{F_s}(f)\}\\ &= x_s(t) * \left[F_s\cdot\mathrm{sinc}(\pi F_s t)\right]\\ &= F_s\cdot\left[x_s(t) * \frac{\sin(\pi F_s t)}{\pi F_s t}\right]\\ &= F_s\cdot\left[\sum_{n=-\infty}^{\infty} x(nT_s)\delta(t-nT_s)\right] * \frac{\sin(\pi F_s t)}{\pi F_s t}\\ &= F_s\cdot\left[\sum_{n=-\infty}^{\infty} x(nT_s)\cdot\frac{\sin(\pi F_s(t-nT_s))}{\pi F_s(t-nT_s)}\right]\end{aligned} \tag{I.23}$$

where:

$$x(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\cdot\frac{\sin(\pi F_s(t-nT_s))}{\pi F_s(t-nT_s)} \tag{I.24}$$

Equation (I.24) is also known as the Whittaker-Shannon interpolation allowing a perfect reconstruction of the analogue signal $x(t)$ from samples taken at $t = nT_s$. To sum up, in case of ideal sampling, the entire information contained in the initial signal $x(t)$ is maintained after being sampled if the Nyquist theorem is fulfilled. However, what can be the consequences on the spectrum if it is not the case ? The answer to this question can be provided by means of a graphical representation as shown in Fig. I.11 where $F_s = 1.8\times f_{max}$. Figure I.11 illustrates that the spectral lines at f_{max} and $-f_{max}$ are out of the area delimited by the Nyquist frequency, $[-F_s/2; F_s/2]$. As a consequence, f_{max} and $-f_{max}$ are mapped on to frequencies below the above-mentioned interval, that is $F_s - f_{max}$ and $-F_s + f_{max}$ respectively. In general, whenever the sampling theorem is not fulfilled, a given frequency f_{alias} comprised in the interval $[F_s/2; F_s]$ is mapped on to the frequency $F_s - f_{alias}$. This overlapping phenomenon is called *aliasing* or *folding* and is responsible for spectrum distortions. Due to aliasing, the spectral line of f_{alias} will appear as an actual spectral line of the analogue signal despite the fact that the former does not exist in reality. Now, if the aliased spectral line falls into a frequency that a DFT-based algorithm cannot reject, the phasor estimate will be wrong. The most critical frequency for a DFT-based estimator is $F_s - f_k$, being f_k is the frequency of interest.

3.3 Analogue anti-aliasing filtering process

Numerical protection relays are designed to operate for a particular bandwidth in which each frequency used for measurement and protection applications is estimated. Frequencies outside this bandwidth which can be encountered in power systems are considered as interfering signals and must be removed for two reasons. First, they are not used by the relay. Second, they may result in aliasing phenomenon. Therefore, there is a need to artificially band-limited the analogue signals. To do so, the conventional solution consists in using an analogue low-pass anti-aliasing filter before sampling the signal. The magnitude response of the ideal anti-aliasing filter as the same shape as the rectangular window and is known as “brick-wall low-pass filter”. It permits a full transmission without distortion in the passband, a perfect attenuation in the stopband, with abrupt transitions between these bands. However, such filters cannot be physically performed but approximated based

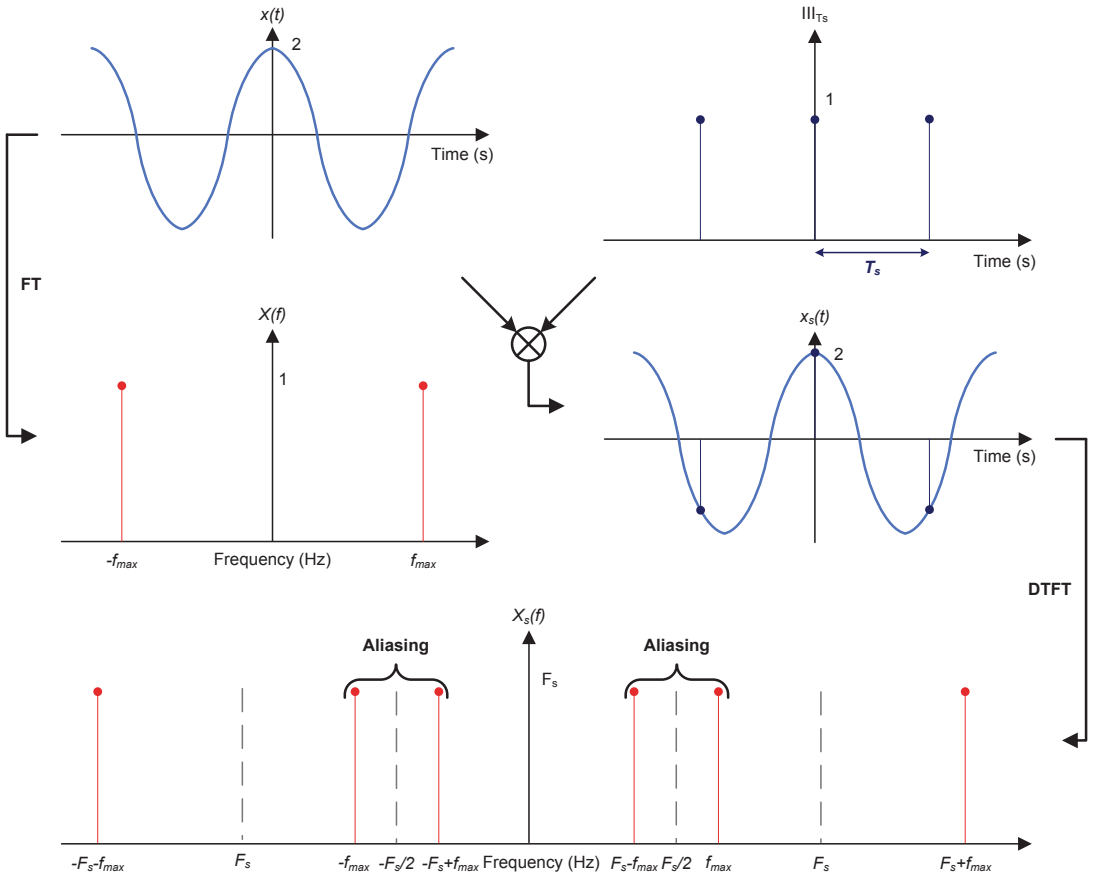

FIGURE I.11 – Principle of the aliasing effect on the spectrum

on the following specifications:

— passband gain, G_{pass}
— stopband gain, G_{stop}
— passband edge frequency (or cut-off edge), F_{pass}
— stopband edge frequency, F_{stop}

A general magnitude response of such a filter is given in Fig. I.12 where the frequency range is defined from DC to a value of frequency infinitely large. Along the X-axis are represented the three regions (or bands) of the filters called “passband”, “transition band”, and “stopband”. These regions are defined based on the aforementioned four parameters. Within the passband, the gain of the filter may vary from 0 dB to G_{pass}. Similarly, the attenuation of the filter in the stopband may fluctuate between G_{stop} and $-\infty$ dB. In both cases, the variations in the passband and the stopband are called ripples. Ripples in the passband are responsible for introducing some magnitude errors in the output of the filter on the whole frequency range of interest. These ratio errors need to be compensated in software because they degrade the accuracy with which phasors are computed.

Another important metric is the filter order which determines the sharpness of the transition band, also called the roll-off. As a rule of thumb, the filter roll-off is designed to achieve the desired gain at the first frequency which is mapped on to the frequency

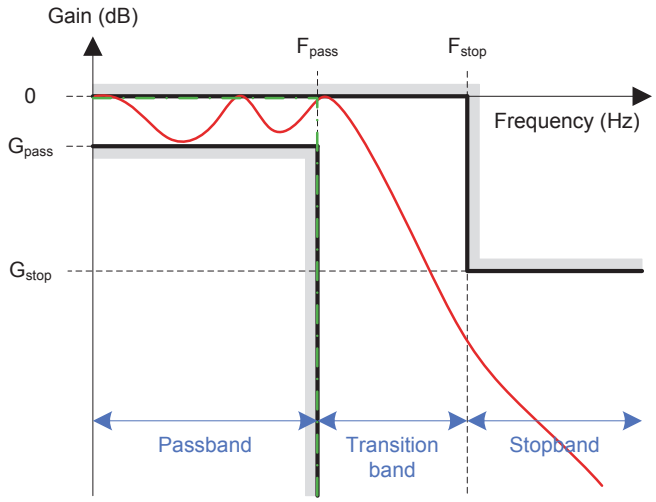

FIGURE I.12 – Ideal (green) and practical (red) anti-aliasing low-pass filter magnitude responses

of interest. Assuming a linear roll-off, it can be shown that the roll-off is related to the attenuation, the sampling frequency, and the frequency of interest as shown [Cot00]:

$$\Delta R = \frac{A \log 2}{\log\left[\frac{F_s - f_k}{f_k}\right]} \tag{I.25}$$

where:

ΔR	is the roll-off in dB/decade
A	is the desired attenuation in dB
f_k	is the frequency of interest in Hz

In general, a high order filter provides a very sharp cut-off but produces a slow response time and introduces a greater delay than a low order filter. *In fine*, such high order filter will negatively impact the responsiveness of the protection device. The group delay, G_d, expressed in second, is directly related to the phase response by the formula following [ET08]:

$$G_d = -\frac{1}{2\pi} \cdot \frac{d\varphi(f)}{df} \tag{I.26}$$

where:

$\varphi(f)$	is the phase response of the filter

The effect of the phase response is that it changes the respective phase of the different frequency components of a signal. Now, if the phase response is a linear function of frequency, then its derivative is a constant. Consequently, G_d is a constant as well for all frequencies where the phase response is linear in accordance to Eq. (I.26). This property is particularly useful because the shape of the signal is preserved for a wide range of frequency: the output signal is a "copy" of the input signal, delayed by G_d. Therefore, the compensation of the phase shift is straightforward and remains valid even if the system is

operating at off-nominal frequencies.

In addition to the cut-off frequency and the filter order, the parameters G_{pass}, G_{stop}, F_{pass}, and F_{stop} are used to determine the transfer function of the filter and consequently, the plotting of its frequency response. Several approximation functions have been studied over the years with the aim of approaching the ideal filter response while maintaining the filter order as small as possible. Butterworth, Chebychev, and Bessel filters are part of such approximation functions. Butterworth filters are designed to have maximally flat response in the passband. On the contrary, the optimization criterion of Bessel filters concerns the group delay which must be as constant as possible in the passband. For this reason, Bessel filters are often called maximally linear phase response filters. The main drawback of Bessel approximation is that the transition band is larger than Butterworth and Chebycheb filters. Finally, the Chebychev approximation makes possible a faster transition between the passband and the stopband at the expense of ripples in the passband. Traditionally, protection relays uses one of these three approximations as they provide optimal time and frequency responses. Nevertheless, preferences are given to the Butterworth filter for their constant gain in the passband [PT09].

3.4 Analogue-to-digital conversion and oversampling process

Analogue-to-digital converters require a stable and constant voltage level at its input to get accurate conversion results. This is be achieved by the use of S/H circuits which perform two operations. First of all, the signal magnitude is kept as it is at the instant the signal has been sampled. Then, the signal is held for a duration τ_p during which the conversion function is performed (see Figs. I.8 and I.9). The process of converting the signal being sampled into its corresponding digital code is called quantization. The main objective of quantization is to best approximate the infinitely accurate analogue signal with a finite number of bits. To do so, the full scale voltage range of the ADC is divided into a number of sub-ranges of identical amplitude called step or Least Significant Bit (LSB). Each step corresponds to a specific number which, in the case of protection relays, is a signed integer. The number of discrete values that can be generated over the full scale range is called the resolution, generally expressed in bits. Due to this fact, the number of steps is most of the time a power of two for convenience. As an example, an ADC having a resolution of 16 bits can encode an analogue value to one in $2^{16} = 65,536$ different levels, ranging from -32,768 to 32,767. Moreover, the accuracy with which an analogue value is encoded can best be estimated by expressing the resolution as function of the full scale and the number of bits as it follows:

$$R = \frac{V_{fs}}{2^{N_{bits}} - 1} \tag{I.27}$$

where:

R	is the ADC resolution (in Volt)
V_{fs}	is the full scale range (in Volt)
N_{bits}	is the bit word length

Based on Eq. (I.27), assuming that the aforementioned ADC has a full scale range of ±10 V, its resolution R is around 0.305 mV. Now, if the ADC input voltage is 0.2 mV, it is clear that the digitized output will be wrong as the resolution is not small enough. The error introduced is called the quantization error or the quantization noise. Assuming that the analogue signal spans more than a few LSBs, the quantization noise is a time-varying error, having a saw-tooth profile and a zero mean value, and uniformly distributed between $-1/2$LSB and $1/2$LSB [3] (see Fig. I.13) [Ben48]. Thus, the quantization

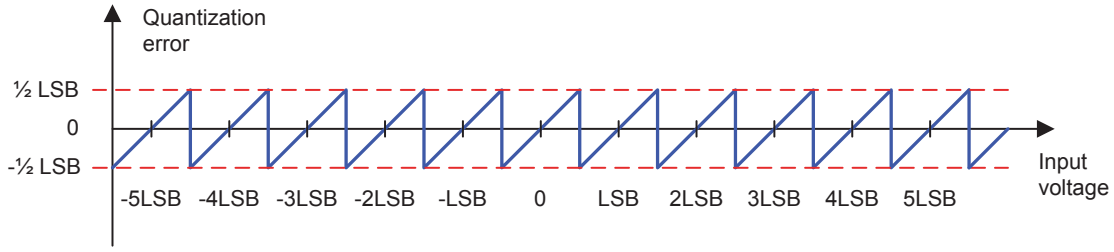

FIGURE I.13 – Evolution of the quantization error

process superimposes a noise approximately Gaussian to the input signal. Based on these assumptions, the average power, P_ϵ, of such a noise is given below [Ben48]:

$$P_\epsilon = \frac{LSB^2}{12} \tag{I.28}$$

In fact, in the frequency domain, P_ϵ is more or less uniformly distributed over the Nyquist bandwidth, that is from DC to $F_s/2$ and its spectral power density, D_ϵ, is given by [Ben48]:

$$D_\epsilon(f) = \frac{2P_\epsilon}{F_s} \tag{I.29}$$

Let the analogue signal band of interest be the frequency range $[0; f_{max}]$. In accordance with Eq. (I.22), its Nyquist rate is $2f_{max}$. If such an analogue signal is sampled at a rate equal to the Nyquist rate, a white noise of spectral density $(2P_\epsilon)/F_s$ will spread over the whole passband. Now, if the sampling frequency is multiplied by a factor L, that is $L \cdot 2f_{max} = L \cdot F_s$ with $L > 1$, the white noise density is reduced by the same factor L and fans out over $[0; (LF_s)/2]$. As a consequence, the noise in the passband is decreased also by $1/L$ as shown in Fig. I.14. The process of sampling to a rate much higher than the Nyquist rate is called oversampling [Hau91].

In addition to the reduction of noise, oversampling simplifies the characteristics of the analogue low-pass anti-aliasing filter. Indeed, reminding Fig. I.10, the spectrum replicas are now shifted by LF_s instead of F_s which means that there is no need to design an analogue anti-aliasing filter with a sharp cutoff in its frequency response and a stopband at $F_s/2$. Instead, the stopband is at $(LF_s)/2$ and is far away from the passband. Therefore, the transition band rolls off gradually resulting in a reduced order filter. Nevertheless, the

3. Errors of magnitude $1/2$LSB occur whenever the analogue value is exactly at the center of a given step

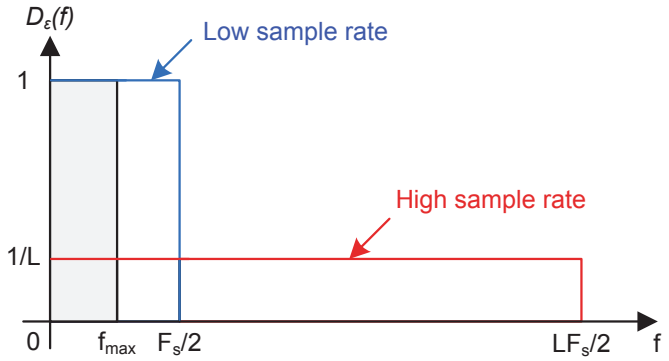

FIGURE I.14 – Spectral density of quantization noise with and without oversampling

frequency values within the range $[F_s/2; (LF_s)/2]$ must be filtered in software since not rejected by the analogue anti-aliasing filter. This phenomenon is illustrated in Fig. I.15.

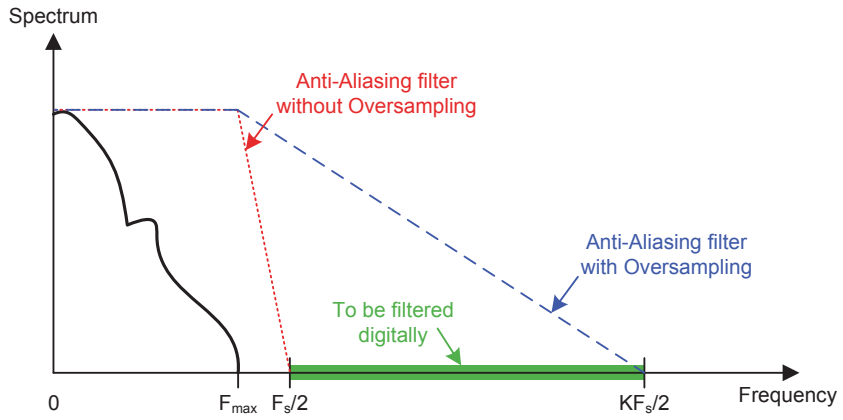

FIGURE I.15 – Anti-aliasing filter characteristics with and without oversampling

3.5 Multi-channel structures

In the three previous subsections, the descriptions were given considering a single input signal. However, several measurements are required to be analyzed and processed by the numerical relay. To cope with this requirement, two multi-channel structures are most often employed: the non-multiplexed structure and the multiplexed structure.

To acquire more than one signal, the most straightforward way consists in duplicating each of the basic element of the DAQ m times, being m the number of input signals to be converted. This results in the structure shown in Fig. I.16 where the interposed CTs and VTs have been disregarded for sake of simplicity.

With such a structure, the filtering, sampling and quantization operations are performed in parallel on all channels. Now, if the S/H functions are controlled by the same signal, it means that the input signals are sampled simultaneously. Thanks to this characteristic, there is no phase shift between the channels. This is a real benefit in case a

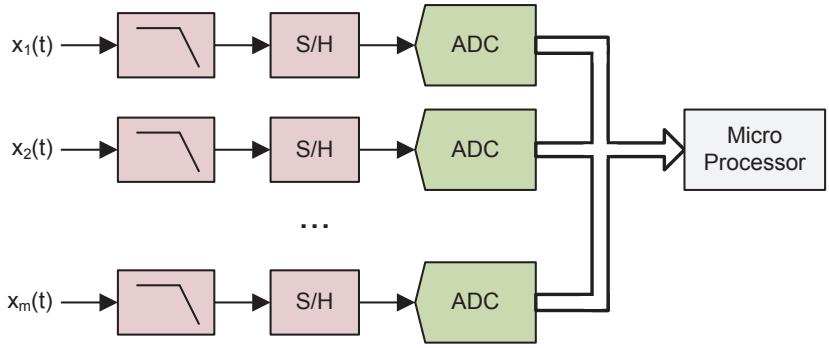

FIGURE I.16 – Non-multiplexed DAQ structure

given protection algorithm compares the phase angles of multiple channels as is the case in directional protection. The main inconvenience of the non-multiplexed structure is its cost as the ADC is generally the most expensive component of the DAQ [Ant06a].

To decrease the cost and the complexity of the structure, the DAQ may incorporate a multiplexor as shown in Fig. I.4. In this configuration, the input signals are multiplexed before being sequentially directed to a single ADC. To avoid phase error, S/H circuits must be used on each channel. Indeed, if a single S/H circuit is used immediately before the ADC, there will be a phase error. Such a structure is therefore particularly interesting for industrial applications.

4 Off-nominal frequencies and their impacts on DFT-based algorithms

To study the impacts of frequency excursions on the DFT-based estimators, let us start with the sinusoidal signal $x(t)$ of frequency f_0 expressed as it follows:

$$x(t) = X_m \cos(2\pi f_0 t + \varphi_x) \tag{I.30}$$

where:

X_m is the peak value of $x(t)$
φ_x is the initial phase angle of $x(t)$

The signal established in Eq. (I.30) is based on the assumption that the power system is operated at its nominal frequency. For correct phasor estimation through the DFT, it is necessary to establish the relationship between the sampling frequency F_s and the nominal frequency as shown below:

$$F_s = N \times f_0 \tag{I.31}$$

Sampling the signal $x(t)$ based on the fixed sampling frequency F_s yields the sample set $x[n]$ expressed in Eq. (I.8) where N samples are acquired in exactly one signal fundamental cycle. In this configuration, assuming that aliasing has been properly corrected by means of anti-aliasing filter, the phasor of fundamental frequency can be estimated without errors

through the full-cycle DFT algorithm as shown in Eq. (I.9). However, the power system is not always operated exactly at its fundamental frequency. Indeed, the frequency f fluctuates constantly due to changes in load and generation imbalances, especially with the wide use of renewable energy sources and distributed generation. In such a context, the sampling frequency defined in Eq. (I.31) is not suitable in all cases. To highlight this fact, let us assume the sinusoidal signal $y(t)$ of off-nominal frequency f be written as:

$$y(t) = Y_m \cos(2\pi f t + \varphi_y) \tag{I.32}$$

where:

Y_m	is the peak value of $y(t)$
φ_y	is the initial phase angle of $y(t)$

Its sample set $y[n]$, obtained through the sampling process based on Eq. (I.31), is given below:

$$y[n] = Y_m \cos(\frac{2\pi f}{N f_0} n + \varphi_y) \tag{I.33}$$

The sampling frequency F_s is not anymore an integer multiple of f as Eq. (I.33) cannot be simplified. Such a way of sampling is called asynchronous sampling and is characterized by an observation window that contains a non-integer number of cycles. Recall the DFT theory assumes that the discretized signal is periodic with a period equal to the length of the data window of N samples. Due to asynchronous sampling, the assumed periodic waveform is not a pure cosine wave and has end-point discontinuities. The abrupt truncations of the off-nominal signal yield wrong phasor estimations. This pernicious phenomenon is well known as leakage effect [Vas07]. It is depicted in Fig. I.17 where the full-cycle DFT analysis has been applied. Figure I.17 involves two signals, $m(t) = \sqrt{2}\cos(2\pi f_0 t)$ and $n(t) = \sqrt{2}\cos(2\pi(f_0 + 5)t)$, sampled at a fixed sample rate of 2400 Hz and processed by the DFT algorithm at $t = 0.04$ s. The data windows considered have been highlighted and their DFT spectra have been represented in the interval $[0; F_s/2]$ for sake of clarity. Regarding the signal $m(t)$, 48 samples have been acquired in exactly 1 cycle and the Fourier analysis shows that the amplitude of the fundamental phasor is obtained without error as expected. On the contrary, the 48 samples have been gathered in more than 1 cycle for $n(t)$. Consequently, the Fourier analysis reveals that the energy of the spectrum decreases at the fundamental and extends over other frequency bins.

The consequences of the leakage phenomenon on the phasor of interest can be shown mathematically and interpreted graphically. Let us assume a cosine wave of off-nominal angular frequency ω expressed as:

$$x(t) = X_1 \cos(\omega t + \phi_1) \tag{I.34}$$

where:

X_1	is the peak amplitude of the fundamental component
ω	is the off-nominal angular frequency, $\omega = 2\pi f = \omega_0 + \Delta\omega$
ϕ_1	is the initial phase angle of the fundamental component

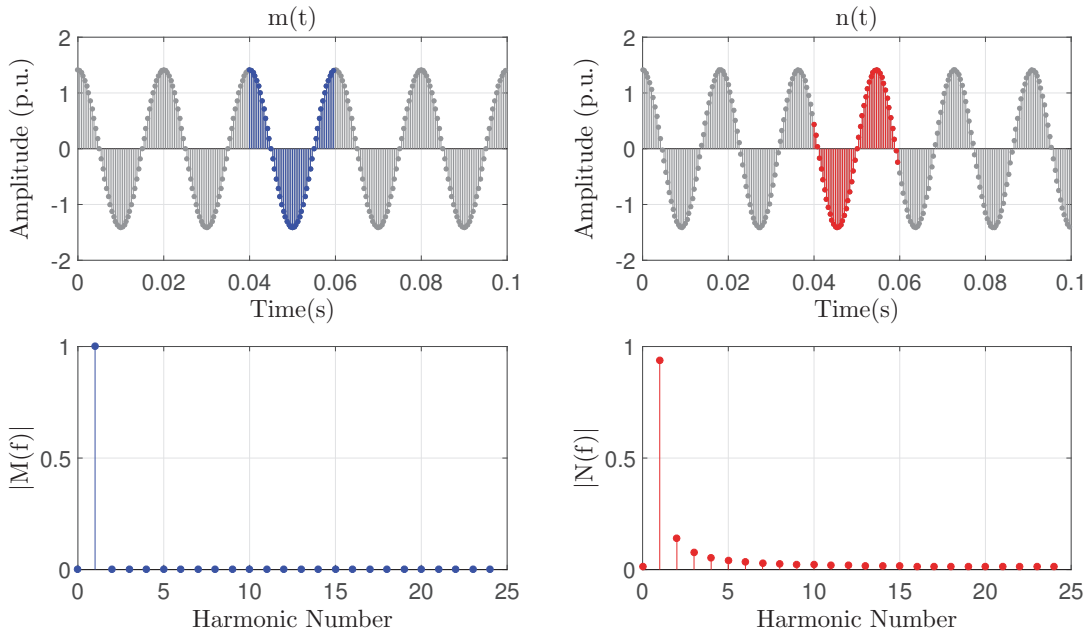

FIGURE I.17 – Leakage phenomenon example

The resultant phasor of fundamental frequency, $\overline{X}^{(r)}$, computed at sample time r, is reported below (See Appendix B for mathematical proof where a cosine wave of off-nominal angular frequency ω superimposed with m^{th} harmonics has been considered to show the relation between the correct phasor and the resultant one):

$$\overline{X}^{(r)} = \overline{P_1}^{(r)}\overline{X_1} + \overline{Q_1}^{(r)}\overline{X_1^*} \tag{I.35}$$

with:

$$\overline{P_1}^{(r)} = \frac{\sin\left(\frac{\pi\Delta f}{f_0}\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}\right)} e^{j\pi\frac{(N-1)}{N}\frac{\Delta f}{f_0}} e^{j\frac{2\pi\Delta f}{Nf_0}r} \tag{I.36}$$

$$\overline{Q_1}^{(r)} = \frac{\sin\left((\frac{\pi}{f_0})(\Delta f + 2f_0)\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0} + \frac{2\pi}{N}\right)} e^{-j\pi\frac{(N-1)}{Nf_0}(\Delta f+2f_0)} e^{-j\frac{2\pi}{Nf_0}(\Delta f+2f_0)r} \tag{I.37}$$

where:

Δf is the frequency deviation, $\Delta f = f - f_0$

Equation (I.35) gives the wrong estimated phasor $\overline{X}^{(r)}$ as function of the correct phasor $\overline{X_1}$. To better understand the errors introduced on the correct phasor of fundamental frequency, let us assume first that the input signal is estimated at sample time $r = 0$. In such a configuration, Eq. (I.35) could be rewritten as:

$$\overline{X}^{(0)} = \frac{\sin\left(\frac{\pi\Delta f}{f_0}\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}\right)} e^{j\pi\frac{(N-1)}{N}\frac{\Delta f}{f_0}}\overline{X_1} + \frac{\sin\left((\frac{\pi}{f_0})(\Delta f + 2f_0)\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0} + \frac{2\pi}{N}\right)} e^{-j\pi\frac{(N-1)}{Nf_0}(\Delta f+2f_0)}\overline{X_1^*} \tag{I.38}$$

The resultant phasor estimate can be splitted into a phasor and its complex conjugate rotating in opposite directions in the complex plane. The phasor $\overline{X_1}$ rotates in the anticlockwise direction at a angular speed of $\Delta\omega$ rad/s while its complex conjugate in the clockwise one at $\Delta\omega + 2\omega_0$ rad/s. Moreover, each of the two phasors $\overline{X_1}$ and $\overline{X_1^*}$ are multiplied by a complex factor, $\overline{P_1}^{(0)}$ and $\overline{Q_1}^{(0)}$ respectively, whose values are dependent on the frequency deviation. Qualitatively, the complex gains attenuate and shift in the complex plane the phasors $\overline{X_1}$ and $\overline{X_1^*}$ as drawn in Fig. I.18.

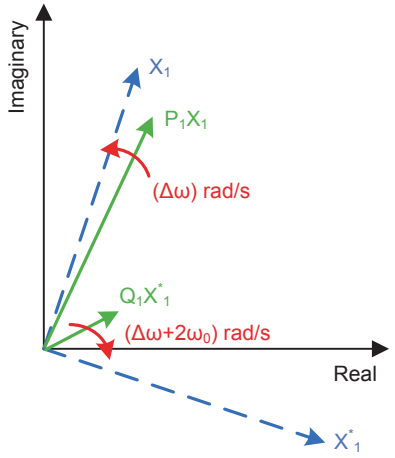

FIGURE I.18 – Qualitative representation of DFT-based estimators at off-nominal frequency

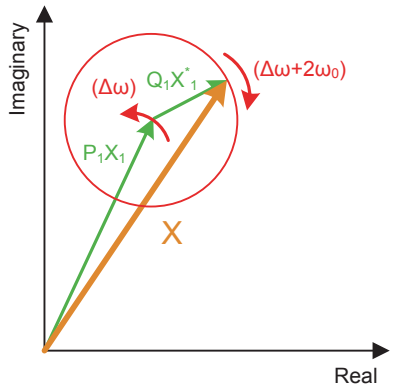

FIGURE I.19 – Combined error of DFT-based estimators at off-nominal frequency

The red circle depicted in Fig. I.19 represents the combined error of the two complex factors $\overline{P_1}^{(0)}$ and $\overline{Q_1}^{(0)}$ on $\overline{X}^{(0)}$. The position of the phasor $\overline{X}^{(0)}$ on the circle, which rotates at an angular speed of $\Delta\omega$ rad/s, depends on the instant of measurement "r". The trajectory of the phasor $\overline{X}^{(r)}$ is an ellipse whose orientation is function of the initial phase angle of $\overline{X_1}$. To demonstrate this fact, let us write Eq. (I.38) in a more recognizable form by means of real and imaginary components:

$$\left(\frac{\Re\{\overline{X}^{(0)}\}}{(\Re\{\overline{P_1}^{(0)}\}+\Re\{\overline{Q_1}^{(0)}\})|\overline{X_1}|}\right)^2+\left(\frac{\Im\{\overline{X}^{(0)}\}}{(\Re\{\overline{P_1}^{(0)}\}-\Re\{\overline{Q_1}^{(0)}\})|\overline{X_1}|}\right)^2=1 \qquad \text{(I.39)}$$

where:

$(\Re\{\overline{P_1}^{(0)}\}+\Re\{\overline{Q_1}^{(0)}\})|\overline{X_1}|$ is the major radius
$(\Re\{\overline{P_1}^{(0)}\}-\Re\{\overline{Q_1}^{(0)}\})|\overline{X_1}|$ is the minor radius

Equation (I.39) shows that the ellipse eccentricity worsens as the frequency deviation grows.

Graphically, the leakage phenomenon prevents the phasor from rotating in a circular pattern inscribing a circle whose radius is equal to the RMS value of the input signal.

Instead, the locus of all phasor estimates is an ellipse indicating that the magnitude of the estimations is constantly changing and is function of the sample time. This conclusion is true only if the input signal is not corrupted by harmonics. The impact of harmonics during frequency excursions can be studied by means of a figure, especially in the light of the frequency response of the full-cycle DFT. To do so, the method proposed in [Wan99] is used. Reference [Wan99] demonstrated that the DFT-based estimator is a non-linear algorithm because both the magnitude and phase estimates include non-linear operations as shown in Figs. I.2 and I.3. These non-linear operations are the square root and the arctan. According to Fig. I.2, and considering the cosine wave in Eq. (I.8), that is $x[n] = X_m \cos((2\pi n)/N+\varphi)$, the magnitude estimate of the fundamental phasor $\overline{X_1[n]}$ can be expressed as it follows:

$$\overline{X_1[n]} = \frac{1}{\sqrt{2}}(H_{1,c}^2 + H_{1,s}^2 + \sqrt{H_{1,c}^4 + H_{1,s}^4 + 2.H_1 1, c^2.H_{1,s}^2.\cos\left(2(\theta_{1,c} - \theta_{1,s})\right)} \cdot \cos(2\omega n T_s + \theta))^{\frac{1}{2}} \cdot \overline{X_1} \quad \text{(I.40)}$$

where:

$$H_{1,c} = |H_{1,c}(z)| \quad \text{(see Eq. (I.15))}$$
$$H_{1,s} = |H_{1,s}(z)| \quad \text{(see Eq. (I.16))}$$
$$\theta_{1,c} = \underline{/H_{1,c}(z)}$$
$$\theta_{1,s} = \underline{/H_{1,s}(z)}$$
$$\theta = \arctan\left(\frac{H_{1,c}^2 \sin(2(\varphi + \theta_{1,c})) + H_{1,s}^2 \sin(2(\varphi + \theta_{1,s}))}{H_{1,c}^2 \cos(2(\varphi + \theta_{1,c})) + H_{1,s}^2 \cos(2(\varphi + \theta_{1,s}))}\right)$$

Here also, Eq. (I.40) shows that the magnitude estimate varies as function of the sample "n". The maximum value is obtained by letting $\cos(2\omega n T_s + \theta) = 1$ whilst the minimum is reached when $\cos(2\omega n T_s + \theta) = -1$. Therefore, the magnitude response of a full-cycle DFT can be analyzed by looking at the variation range of the magnitude estimate which is delimited by two boundaries. The normalized upper and lower envelopes are respectively given below:

$$\frac{max(\overline{X_1[n]})}{\overline{X_1}} = \frac{1}{\sqrt{2}}\left(H_{1,c}^2 + H_{1,s}^2 + \sqrt{H_{1,c}^4 + H_{1,s}^4 + 2.H_{1,c}^2.H_{1,s}^2.\cos(2(\theta_{1,c} - \theta_{1,s}))}\right)^{\frac{1}{2}} \quad \text{(I.41)}$$

$$\frac{min(\overline{X_1[n]})}{\overline{X_1}} = \frac{1}{\sqrt{2}}\left(H_{1,c}^2 + H_{1,s}^2 - \sqrt{H_{1,c}^4 + H_{1,s}^4 + 2.H_{1,c}^2.H_{1,s}^2.\cos(2(\theta_{1,c} - \theta_{1,s}))}\right)^{\frac{1}{2}} \quad \text{(I.42)}$$

The upper and lower boundaries of the DFT-based algorithm are shown in Fig. I.20 where a nominal system frequency of 50 Hz has been considered. An important point to highlight is that, although not obvious at first glance, the magnitude response of the DFT algorithm is slightly different from the gain of cosine and sine filters.

Moreover, the gray area illustrates the magnitude estimate offered by the algorithm for any signal frequency (leakage). In case the input signal is at fundamental frequency,

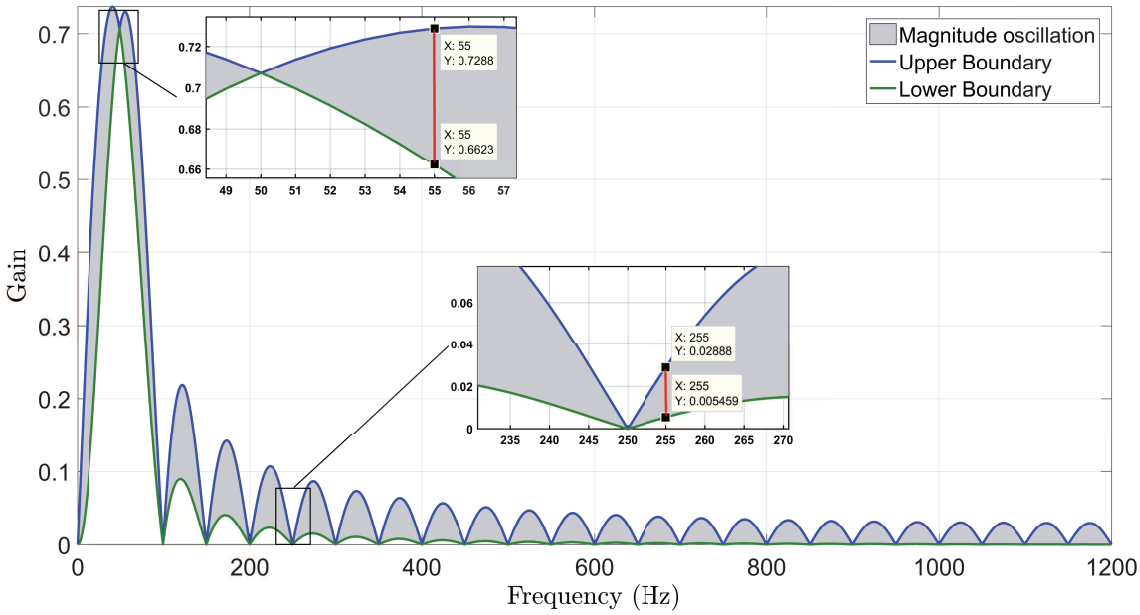

FIGURE I.20 – Example on the effects of off-nominal signal frequency on phasor estimates

the gain remains at $1/\sqrt{2}$ and correct phasor estimation is achieved. Whenever frequency excursions occur, the magnitude exhibits oscillations whose angular frequency is equal to $\omega_0 + \Delta\omega$ rad/s for the fundamental component. Besides, if the off-nominal input signal is superimposed by harmonics, the magnitude variation of each of the harmonic can be estimated graphically. For instance, as depicted in Fig. I.20, the magnitude of the fundamental phasor fluctuates between about 93.66% (momentary underestimation) and about 103.07% (momentary overestimation) of its true value for a frequency deviation of +5 Hz. These under- and over-estimations may either prevent the relay from tripping in case of fault or makes the relay trips during normal system operations. Indeed, an instantaneous overcurrent relay with a threshold of 1 p.u. (reach of the relay) will issue a tripping signal whenever the wrong magnitude estimates exceed 100%. In this context, the relay overreaches of $1 - 1/1.0307 \approx 2.98\%$ beyond its pre-set value. Similarly, the relay has $1/0.9366 - 1 \approx 6.78\%$ underreach at 55 Hz. Now, if the 5^{th} harmonic is superimposed to this off-nominal signal, the magnitude estimates of the former oscillate between about $5.46 \cdot 10^{-3}$ p.u. and about $28.88 \cdot 10^{-3}$ p.u. instead of being notched out (see Fig. I.20). In accordance to Appendix B, the wrong magnitude estimates of the harmonic adds more errors in the fundamental phasor.

To conclude, the DFT-based phasor algorithm is the most popular technique used in marketed relay as it is accurate, elegant, and provides accurate estimation of phasors. However, the leakage problem affects the accuracy with which phasors can be measured and this phenomenon occurs whenever the frequency deviates from its nominal value. With respect to Fig. I.20, although the errors introduced in the phasor estimates are small for minor frequency excursions, they become however significant for large frequency drifts. Large frequency drifts may be encountered in generator applications. For instance, hydrogeneration machines can operate at a speed that can reach 1.5 times its nominal frequency

during load rejection whereas during the start time of combustion gas turbines and pumped storage units the frequency can be as low as 0.3 times the nominal [TKF+14]. Thus, protective relays dedicated to protect generators shall provide accurate phasor measurements to maintain the relay reliability during large frequency deviations and avoid any over- and under-reaches.

5 Minimizing leakage effect on DFT estimators

5.1 Frequency tracking

There are two main traditional approaches in relays to solve the leakage problem of the DFT during frequency deviations: frequency tracking and frequency error compensation. The most famous technique is the frequency tracking firstly introduced in [Ben89] whose principle is illustrated in Fig. I.21 where the classical oversampling method discussed in Section 3.4 is considered.

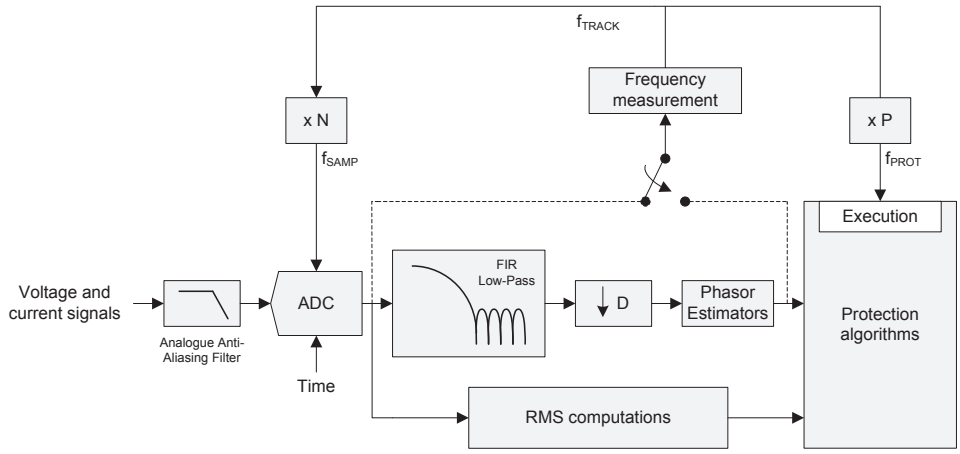

FIGURE I.21 – Simplified frequency tracking principle implementation of a numerical relay

To successfully implement the frequency tracking method, the first step consists in accurately measuring the actual power system frequency. This can be performed by the use of one of the algorithm discussed in Section 6. If we assume that the frequency algorithm is accurate enough, then the estimated frequency can be used to synchronize the sample rate simply by multiplying this estimate by the number of samples N to obtain f_{SAMP}. This is done by changing the sampling frequency of the clock. As an example, assuming $N = 48$ and $f_0 = 50$ Hz, the relay will sample at a frequency of $F_s = 48 \times 55 = 2,640$ Hz instead of $2,400$ Hz in case the system frequency becomes 55 Hz. Consequently, the number of samples per cycle is kept constant whatever the power system frequency is which means that the DFT can accurately estimates phasors. Graphically, the frequency tracking shifts the frequency response of the full-cycle DFT in such a way that the gain $1/\sqrt{2}$ is locked to the new system frequency. The execution of the protection elements is performed at a particular frequency f_{PROT} which is traditionally related to the tracked frequency, f_{TRACK}. This permits to execute the protection functions each time the desired number of

samples have been gathered. For instance, if P is equal to 2, the protection elements, the logic schemes and the output contacts are updated twice per cycle, that is each $N/2$ samples.

The implementation of the frequency tracking described in Fig. I.21 has evolved over the years taking advantages of the improvements in DSP processing power. The new methods are based on the full-digital frequency tracking implementation. An example of such implementation can be found in [SAGC+03]. The objective of such methods is to mimic the frequency tracking with drivable ADC implementation by means of interpolations (resampling schemes). With respect to Fig. I.22, the sampling clock of the ADC is henceforth fixed and may be synchronized to an absolute time reference. The sample rate of the ADC f_{SAMP} can be set high compared to the one used for running the protection algorithms (f_{RESAMP}) in order to increase the resolution of the embedded digital fault recorder function.

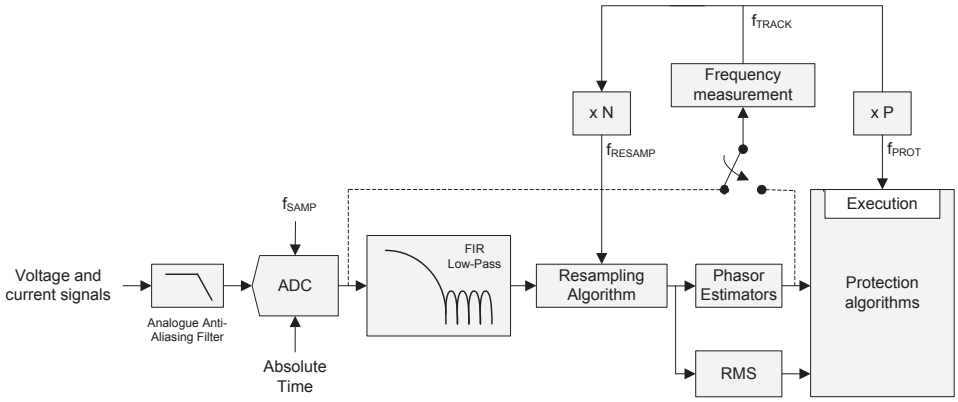

FIGURE I.22 – Simplified frequency tracking principle implementation through resampling algorithm

5.2 Frequency error compensation

The frequency error compensation method is based on the uniform sample rate architecture. The basic idea consists in estimating the prevailing system frequency to correct the effect of the leakage phenomenon using calibration factors as illustrated in Fig. I.23. One of the possible implementation of the method can be found in [Ben05]. This method involves a post-processing layer to compute the exact phasor through the complex gain $\overline{P_1}^{(r)}$ and $\overline{Q_1}^{(r)}$ in Eqs. (I.36) and (I.37). From Eq. (I.35), the correction factors along with the wrong estimated phasor $\overline{X}^{(r)}$, the correct one $\overline{X_1}$ and its complex conjugate $\overline{X_1}^*$ are first expressed with their real and imaginary parts. The Cartesian components are then laid out in a $2x2$ matrix form as shown:

$$\begin{bmatrix} \Re\{\overline{X_1}\} \\ \Im\{\overline{X_1}\} \end{bmatrix} = \begin{bmatrix} \Re\{\overline{P_1}^{(r)}\} + \Re\{\overline{Q_1}^{(r)}\} & \Im\{\overline{Q_1}^{(r)}\} - \Im\{\overline{P_1}^{(r)}\} \\ \Im\{\overline{P_1}^{(r)}\} + \Im\{\overline{Q_1}^{(r)}\} & \Re\{\overline{P_1}^{(r)}\} - \Re\{\overline{Q_1}^{(r)}\} \end{bmatrix}^{-1} \cdot \begin{bmatrix} \Re\{\overline{X}^{(r)}\} \\ \Im\{\overline{X}^{(r)}\} \end{bmatrix} \tag{I.43}$$

with:

$$\Re\{\overline{P_1}^{(r)}\} = \frac{\sin\left(\frac{\pi\Delta f}{f_0}\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}\right)}\cos((\frac{\pi\Delta f}{Nf_0})(N-1+2r)) \tag{I.44}$$

$$\Im\{\overline{P_1}^{(r)}\} = \frac{\sin\left(\frac{\pi\Delta f}{f_0}\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}\right)}\sin((\frac{\pi\Delta f}{Nf_0})(N-1+2r)) \tag{I.45}$$

$$\Re\{\overline{Q_1}^{(r)}\} = \frac{\sin\left((\frac{\pi}{f_0})(\Delta f+2f_0)\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}+\frac{2\pi}{N}\right)}\cos((-\frac{\pi(\Delta f+2f_0)}{Nf_0})(N-1+2r)) \tag{I.46}$$

$$\Im\{\overline{Q_1}^{(r)}\} = \frac{\sin\left((\frac{\pi}{f_0})(\Delta f+2f_0)\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}+\frac{2\pi}{N}\right)}\sin((-\frac{\pi(\Delta f+2f_0)}{Nf_0})(N-1+2r)) \tag{I.47}$$

The correction matrix of Eq. (I.43) can be pre-computed for several frequency excursions Δf, stored in memory through a look-up table and then used directly to correct the wrong phasor. By doing this, there is no need to compute the correction matrix each time an exact phasor is determined which results in saving some computational effort. The aforementioned procedure can be repeated for the phasor of harmonics but this will need new correction matrices dedicated to each harmonic considered. By the way, frequency error compensation methods are based on the underlying assumption that the input signal does not contain harmonics or any other undesirable components. Consequently, the input signal is expected to be properly filtered in such a way that the input signal contains just the frequency of interest.

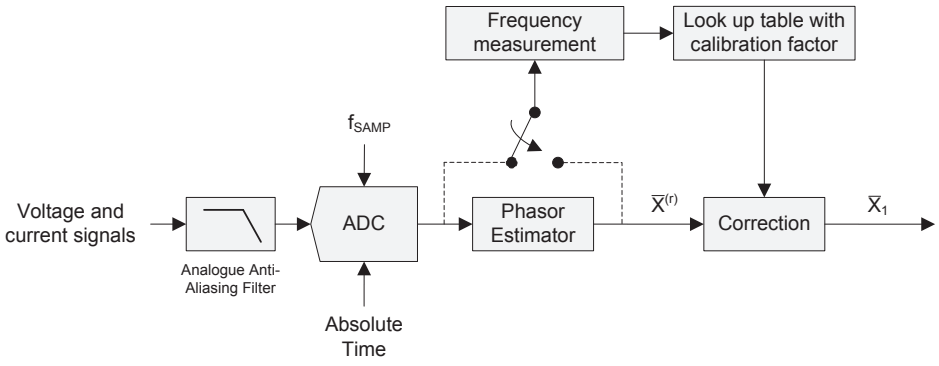

FIGURE I.23 – Simplified frequency error compensation implementation

6 Power system frequency estimation methods review

In Section 4, it has been highlighted that the DFT is sensitive to frequency deviations and the leakage phenomenon has been characterized. Subsequently, in Section 5, the two traditional techniques in used in protection relays to deal with the leakage, namely frequency tracking and frequency compensation, have been described. On the one hand, the frequency tracking uses the frequency estimates either to adjust the sample rate or to run the software resampling algorithm. On the other hand, frequency compensation methods

utilize the measured frequency to apply correction factors on DFT estimates. In both cases, the estimation of the power system frequency is the common denominator. This is one of the reason explaining why protection relays must accurately measure the system frequency. Furthermore, a variety of protection and control algorithms based on frequency measurements are typically used to protect the power systems under various conditions. For example, under-frequency algorithms can be used for automatic load-shedding [MFT91] while over-frequency algorithms are applied as overspeed protection [Rob90].

Protection relays must provide fast real-time fundamental frequency estimations in a noisy environment operating under dynamic conditions. In such a context, the best frequency measurement method would be the one that is accurate, easy to implement, converges quickly to the expected value, provides noise rejection, and requires low computational power [Akk97]. Several frequency measurement methods have been proposed in the literature to try to reach the aforementioned objectives. Some of them are listed here without being exhaustive: zero-crossing [BDDP93], least error square [GS89], demodulation [Akk97], Kalman filters [GP90], and phasor-based [PTA83]. Among them, the two approaches commonly implemented in protection relays are zero-crossing and phasor-based due to their simplicity and their low computing cost [Kas16]. Both methods are explained hereafter. In general, the voltage waveforms are preferred to estimate the frequency since the voltage levels are higher are less affected by noise, harmonics, and DC component compared to the current waveforms [RVZ11].

6.1 Frequency measurement based on zero-crossings

The zero-crossing method is a time domain technique based on the time difference between two zero-crossings, i.e. instants in time where the sign of two consecutive samples changes. Since the time is inversely proportional to the frequency, the later can be calculated from the measurement of the former. Mathematically, considering the sample set $x[n]$, the number of zero-crossings in a given data window of M samples can be expressed as it follows:

$$ZC = \sum_{n=r}^{r+M-1} |\operatorname{sgn}(x[n]) - \operatorname{sgn}(x[n-1])| \tag{I.48}$$

where:

ZC	is the number of zero-crossings
sgn	denotes the *sign* function

In Eq. (I.48), the zero-crossings are counted in any direction, both negative-to-positive and positive-to-negative. Thus, the time between two consecutive zero-crossings is one-half the time of the input signal period. Other variations of this approach are possible like timing full cycles between zero-crossings in the same direction only. Once ZC has been determined, the frequency is computed as shown below [MS09].

$$f = \frac{1}{2} \cdot \frac{ZC - 1}{t_m - t_1} \tag{I.49}$$

where:

f	is the estimated frequency
t_m	is the time where the last zero-crossing occurs in the observation window
t_1	is the time where the 1^{st} zero-crossing occurs in the observation window

The instants of time t_1 and t_m are provided from the timestamps of the samples by means of linear interpolation as illustrated in Fig. I.24. Other interpolation methods can be applied but they necessitate higher processing burden than the simple linear interpolation. Since the sample time T_s is fixed, the time t_1 is computed as it follows:

$$t_1 = t[n-1] - \frac{x[n-1]}{x[n] - x[n-1]} T_s \tag{I.50}$$

The main drawback of zero-crossing algorithm is that it is entirely dependent on the shape

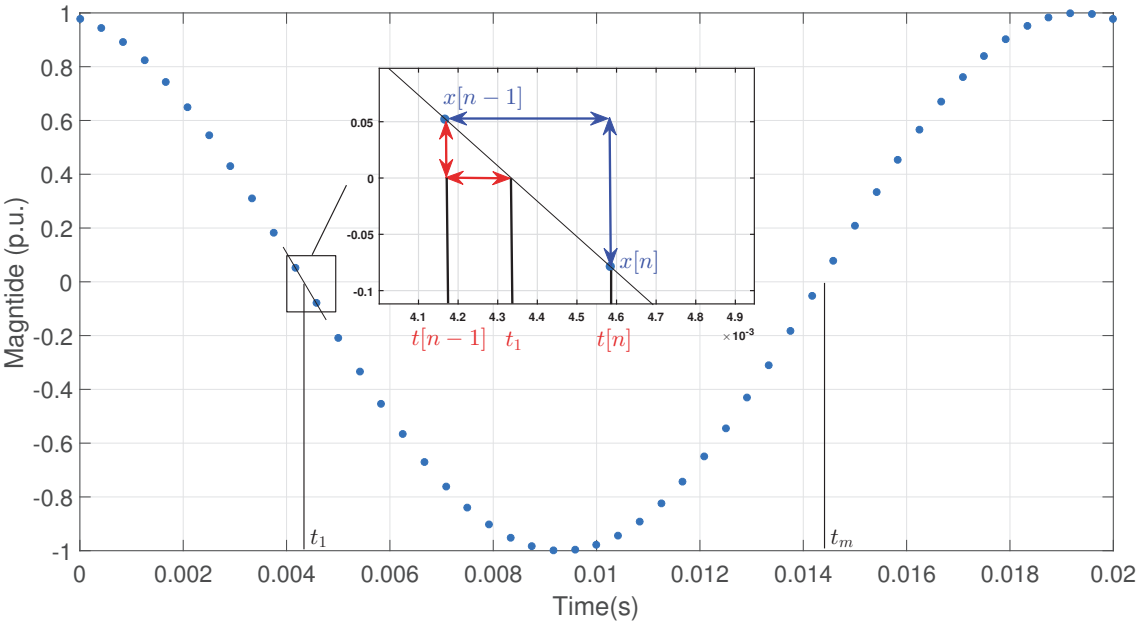

FIGURE I.24 – Zero-crossing timestamp computation

of the waveform. If a spurious frequency is superimposed to the fundamental, multiple spurious zero-crossings will occur. Thus, the input waveform must be filtered before being processed by the algorithm. This is performed in two steps. First, a pre-filtering level is employed to reject some unwanted components in the waveform. Pre-filtering is done using either a low-pass or a band-pass filter. Then, to increase the robustness of the algorithm, an additional post-filtering is commonly applied. It consists in using either an averaging of several consecutive estimates or applying a specific non-linear filter to remove spurious zero-crossings which have not been pre-filtered [MS09].

6.2 The Phasor-based method

The phasor-based method mimics the mechanical analogy of generator frequency by computing, in the complex plan, the rate of angular rotation of a phasor that has been measured [Kas16] as depicted in Fig. I.25. This technique has been originally introduced in [PTA83] where it has been applied on the DFT-based phasor of the positive sequence of the three phase voltages. The use of such a symmetrical component is beneficial as it has a natural property of filtering during frequency excursions. Indeed, if the system is balanced, it can be shown that the effect of the $\overline{Q_1}^{(r)}$ factor in Eq. (I.35) can be removed using the phasor of the positive sequence [PT08a]. Based on this, Eq. (I.35) can be written as shown:

$$\overline{X}^{(r)} = \frac{\sin\left(\frac{\pi\Delta f}{f_0}\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}\right)} e^{j\pi\frac{(N-1)}{N}\frac{\Delta f}{f_0}} e^{j\frac{2\pi\Delta f}{Nf_0}r}\overline{X_1} = \overline{P_1}^{(r)}\overline{X_1} \tag{I.51}$$

The angular speed of the phasor $\overline{X}^{(r)}$ is given by the factor $\overline{P_1}^{(r)}$. Now, if the N-point DFT is performed once every n samples, then $\overline{X}^{(r+n)}$ can be given by Eq. (I.52).

$$\overline{X}^{(r+n)} = \frac{\sin\left(\frac{\pi\Delta f}{f_0}\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}\right)} e^{j\pi\frac{(N-1)}{N}\frac{\Delta f}{f_0}} e^{j\frac{2\pi\Delta f}{Nf_0}(r+n)}\overline{X_1} \tag{I.52}$$

The phase angle difference between $\overline{X}^{(r+n)}$ and $\overline{X}^{(r)}$ is computed as following:

$$\Phi_{r+n} - \Phi_r = \frac{2\pi\Delta f}{Nf_0}n \tag{I.53}$$

In Eq. (I.53), Φ_{r+n} and Φ_r are obtained through the arc-tangent operation performed on the phasors $X^{(r+n)}$ and $X^{(n)}$ respectively. Remind $\Delta f = f - f_0$, the prevailing system frequency is calculated based on the phase shift between two phasors $\Delta\Phi_r = \Phi_{r+n} - \Phi_r$ as shown:

$$f = (\frac{N\Delta\Phi_r}{2\pi n} + 1)\cdot f_0 \tag{I.54}$$

In contrast to the zero-crossing techniques, the phasor-based method is less sensitive to harmonics or DC offset because the phasors are estimated through the DFT filter. For this reason, the pre- and post-filtering levels are not mandatory. As a consequence, preferences are given to the phasor-based method to estimate the frequency.

7 The Phasor Measurement Unit

By definition, the PMU is an IED which provides real-time measurements of voltage and/or current waveforms by means of phasors. Historically, the birth of the PMU was preceded by the invention of the Symmetrical Component Distance Relay (SCDR) by Arun G. Phadke and James S. Thorp in the 1980s [Pha02]. The SCDR was able to measure one of the fundamental metric of the power system: the positive sequence component of the three-phase voltages. This component provides meaningful information about the power system state and has therefore a major role to play in state estimation [PTK86]. Moreover, it has been recognized that making simultaneous measurements of phasors offer the

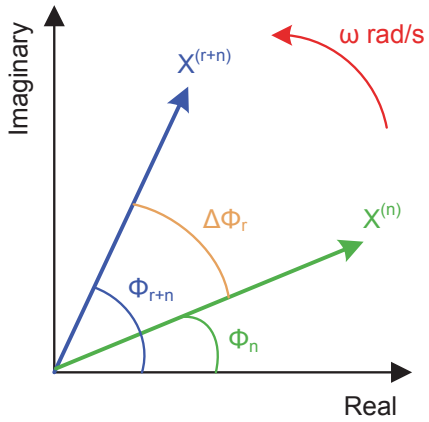

FIGURE I.25 – Rotation of phasors for frequency estimation

opportunity to take consistent "snapshots" across the system. This means that the measurements performed at different substations across the system can be compared directly since they are based on the same time axis. By doing this, the power system monitoring, protection, operation and control is improved [Pha93, PT06].

Simultaneous measurements can be achieved by synchronizing the sampling clock of the devices deployed in the power system. The synchronization of the sampling clock of all IEDs across the power system must be achieved with a certain precision. The degree of accuracy is determined based on the targeted applications. The study performed in [PPA+94] has pointed out that accuracy better than 1 μs, corresponding to about 0.02 degrees for a 60 Hz system, is necessary for synchronized estimation of phasors. Such an accuracy can be achieved with the GPS technology. The GPS is an absolute time reference with optimal time accuracy of ± 0.2 μs. It is able to provide the 1 Pulse-Per-Second (1 PPS) signal for synchronization. In addition, a time-tag including the year, day, hour, minute and second is also transmitted allowing precise time stamping of samples generated by PMUs. These time marks are referenced to the Coordinate Universal Time (UTC) [Pha02].

Since all PMUs may theoretically provide synchronized phasors at specific instants of time, the question of transmitting the phasors for their exploitation naturally arises. The transmission of phasors involves message encoding and communication infrastructures. The very first PMU applications where dedicated to exchange the assembled messages between PMUs located at different sites. To cope with these applications, early studies have proposed to transmit the data streams over a dedicated communication line through modems [Pha02]. Originally, the proposed message format contained the minimum data to be shared and was structured in a binary format. This choice was influenced by the available communication means and bandwidth. A 4,800-baud rate data channel was commonly used, allowing transmission of a single phasor message in about 30 ms [AAB+06].

7.1 Brief historical review of PMU standards

The concept of a power system synchronized phasor was standardized for the first time with the Institute of Electrical and Electronics Engineers (IEEE) Standard 1344 which was completed in 1995 [94395]. In 2003, the IEEE began the effort to transition from IEEE Standard 1344 to IEEE Standard C37.118 in order to improve the accuracy of the time-synchronized phasor measurements. The need for this improvement was based on a post-mortem analysis of the 2003 North American blackout which has affected about 50 million people in the United States and two Canadian provinces [ADF+05]. In 2005, [94395] was superseded by the IEEE synchrophasor Standard C37.118-2005 [16106]. This later introduced the basic compliance test criterion known as Total Vector Error (TVE) which gives the measurement accuracy of synchronized phasors. To check the compliance with [16106], steady-state conditions tests have been defined. Additionally, [16106] has defined the message structure to encode phasor data.

In 2005, the Operator of the National electricity System (ONS), the Independent System Operator for Brazilian Interconnected National Power System (NIPS), has led a major effort for the Brazilian electric power industry by deploying a large scale PMU system, SynchroPhasor Measurement System (SPMS), for NIPS. The SPMS requirements were: post-event analysis, wide-area monitoring, and Energy Management System (EMS)/SCADA enhancement. As part of the SPMS deployment planning, all PMUs to be purchased and installed for SPMS must be certified in order to ensure the global performance of the SPMS. Subsequently, in 2009, ONS has organized a workshop to test and certify PMUs supplied by 8 vendors: ABB, Arbiter, Areva, General Electric, Qualitrol, Reason, Schweitzer Engineering Laboratories, and Siemens. The ONS PMU certification program was based on IEEE Standard C37.118-2005 steady-state tests with additional ONS requirements related to dynamic performance tests. For the first time, PMUs from multiple manufacturers have been tested in dynamic conditions. To ensure the performance of the SPMS, it has been expected that the 8 PMUs behaved in an identical manner for the test cases considered. However, it was not the case and three significant conclusions have been drawn from the results obtained [MHS+12]:

- Most of the PMUs tested met a majority the steady-state performance requirements,
- Behavior of PMUs under dynamic conditions were drastically different,
- Revision of the IEEE Standard C37.118-2005 expected to take into account dynamic performances of PMUs.

Following this workshop, [16106] was split into two standards called IEEE Standard C37.118.1-2011 [C3711b] and IEEE Standard C37.118.2-2011 [C3711a], both published in December 2011. The needs for this separation are explained by two reasons. First, with the rapid evolution of communication means compared to the power system technology, the two entities need to be treated individually. Second, the IEEE has recognized that there is a need to harmonize the real-time message format defined in [C3711a] with the International Electrotechnical Commission (IEC) communication standards 61850 which has been adopted by the industry. The harmonization facilitates the integration of synchronized estimation of phasors into substations using IEC 61850 [Mar15]. An overview of [C3711b] and [C3711a] is described below:

IEEE Standard C37.118.1-2011: Synchronized phasor (synchrophasor) measurements for power systems are presented. This standard defines synchrophasors, **frequency**, **ROCOF** measurement under all operating conditions. It specifies methods for evaluating these measurements and requirements for compliance with the standard under both steady-state and dynamic conditions. Time tag and synchronization requirements are included. Performance requirements are confirmed with a reference model, provided in detail. This standard does not specify hardware, software, or a method for computing phasors, frequency, or ROCOF.

IEEE Standard C37.118.2-2011: A method for real-time exchange of synchronized phasor measurement data between power system equipment is defined. It specifies messaging that can be used with any suitable protocol for real-time communication between PMUs, phasor data concentrators (PDC), and other applications. It defines message types, contents, and use. Data types and formats are specified. A typical measurement system, as well as communication options and requirements are described.

Following the publication of the standards, deep analysis of the signal processing reference model defined in [C3711b] have shown that it cannot fulfill most of the frequency and ROCOF performance requirements. Additionally, manufacturers of PMUs complained the exigencies of [C3711b] are too difficult to met, in particular those related to frequency and ROCOF measurements [Mar15]. To cope with the issues cited above, the 2011 version of the standard has been amended by IEEE Standard C37.118.1a-2014 [68014]. The steady-state and dynamic performance requirements have been relaxed to ease the deployment of fully compliant PMUs.

Finally, both IEEE and IEC are nowadays working together on the publication of an international IEC standard for PMUs where several changes have been adopted against the previous IEEE version and new items included. The IEC/IEEE standard is known as IEC Standard 60255-118-1 and exists today as a draft version [IEC15]. The major revisions are listed below:

— Higher reporting rates allowed,
— Definition of frequency reconsidered,
— Deletion of phase angle test,
— Clarification of step response tests,
— PMU having sampled values as inputs signals (instead of analogue inputs) considered.

In this work, the requirements specified in the draft version of the IEC Standard 60255-118-1 are considered since it will supersede the amended version of the PMU standard once completed.

7.2 Definition of synchronized phasor measurements

The synchronized phasor, or simply synchrophasor, of the signal $x(t)$ is the phasor expressed in Eq. (I.3) where φ is the instantaneous, or absolute, phase angle synchronized to UTC. Under this definition, the cosine function of nominal frequency synchronized to UTC has been chosen as reference. This convention stipulates that φ is equal to 0 whenever the UTC second rollover (1 PPS time signal) occurs that is when the cosine wave $x(t)$ has

a maximum value as shown in Fig. I.26. Now, if a positive zero-crossing occurs at $t = 0$ as it is the case for the sinus waveform $y(t)$, the synchrophasor angle is -90 degrees at that time.

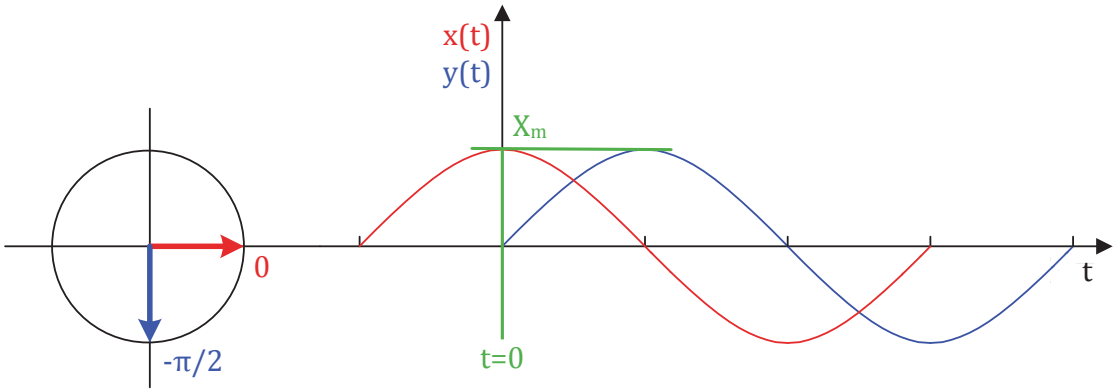

FIGURE I.26 – Illustration of synchrophasors

Moreover, several reporting rates have been defined in the PMU standard. These reporting rates, annotated F_R in frames per second (fps), give the number of time-tagged phasors estimated within a time frame of 1 second (between two consecutive 1 PPS signal). The reporting rates are fixed values, multiples of the fundamental cycles of the network (50/60 Hz). They are reported in the Table I.1 below:

TABLE I.1 – REPORTING RATES ALLOWED BY THE PMU STANDARD

System frequency (Hz)	**50**				**60**						
Reporting rates (fps)	10	25	50	100	10	12	15	20	30	60	120

As a rule of thumb, high reporting rates are suitable for protection and control applications where fast tracking of power system dynamics is required whereas low reporting rates may be useful for SCADA systems reporting, such as state estimation and power flow [Mar15]. In order to exemplify, a reporting rate of 50 fps means that the time stamped synchrophasors must represent the observed signal at intervals $k = \{0, T_R, 2T_R, 3T_R, ...50T_R, ...\}$, being $T_R = 1/F_R$ in seconds. Based on this, if the input signal is a pure cosine wave of 50 Hz, the estimated phase angles will be equal to 0 degree each T_R. However, this statement is wrong if the cosine wave is held to an off-nominal frequency f. Indeed, since the synchrophasors are reported at a fixed rate F_R, the phase angles of the off-nominal signal will drift at a constant rate of $2\pi(f - f_0)T_R$ radians as depicted in Fig. I.27 where the bullet • symbolizes the instant of estimation. An important point to mention is that the phase angles are commonly wrapped to the interval $[-180; 180]$ degrees as stated in the standard [IEC15].

The definition of synchrophasor is valid for both classes of performance which are specified in the standard. These classes are called P-Class and M-Class and stands for protec-

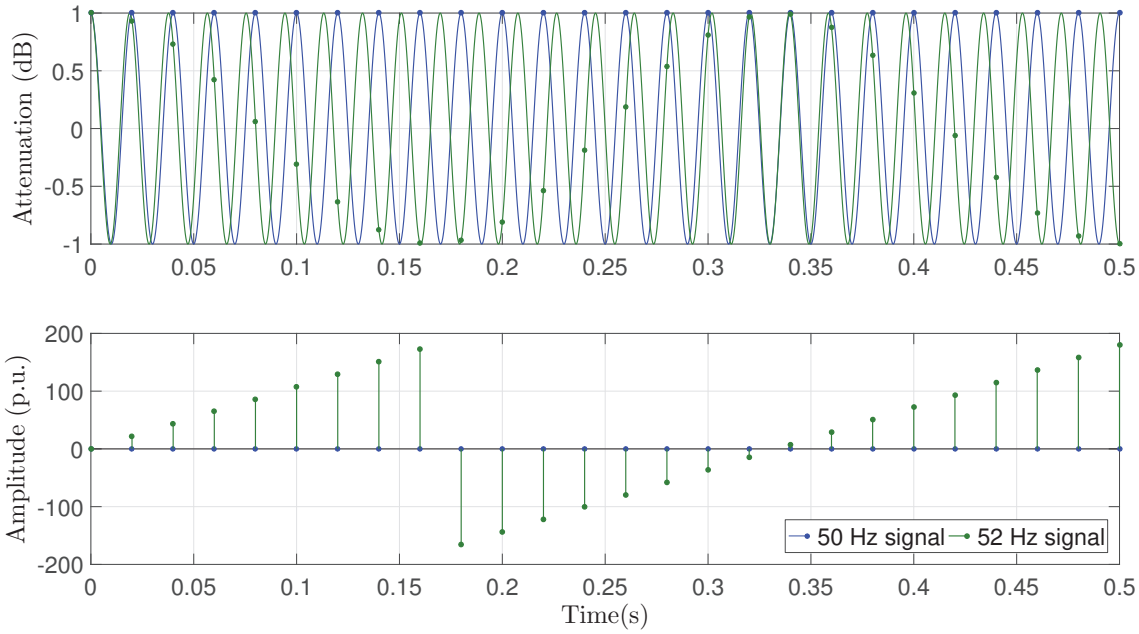

FIGURE I.27 – Drift in phase angle representation for a 52 Hz signal

tion applications and measurement applications respectively. The main difference between these classes of performance concerns the ability of properly notching out spurious tones that may be superimposed to the fundamental component. In general, applications that are sensitive to harmonics and inter-harmonics but tolerate longer delays necessitate the use of M-Class PMUs where high levels of filtering are performed. Otherwise, applications requiring small delay in responding to dynamic changes should involve P-Class PMUs. Nevertheless, this rule of thumb establishing a link between the letters P and M and the applications may not be valid for all possible PMU applications. As carefully precised in [IEC15], it is up to the system designer to select the performance class that best cope with its specific application. Finally, there is no obligation to design a PMU that can handle both performance classes: a vendor is authorized to provide a device that claims only 1 of the two standardized classes.

7.3 Measurement requirements for PMUs

The estimation of the parameters of the grid (magnitude, phase angle, frequency, and ROCOF) are subject to measurement accuracy requirements. Like any measuring device, the PMU cannot estimate the quantities of interest without errors. For the estimation of phasors, the differences between a perfect theoretical synchrophasor and its estimation are regrouped into a common term, previously identified as TVE. The TVE is a quantity which includes the errors in terms of both magnitude and phase angle. Since the phase angle is determined from the time synchronized reference, any timing error translates directly to a phase error. For example, a mismatch of 1 μs is equivalent to an error of 0.018 degrees considering a 50 Hz system while it is equal to 0.0216 degrees for a 60 Hz system. Therefore the TVE criterion reflects also the timing errors which depends on the fundamental system frequency. According to its definition in [IEC15], the TVE, given in percentage, is expressed

based on the real and imaginary parts of the theoretical and estimated phasors:

$$TVE(k) = \sqrt{\frac{\left(\hat{X}_r(k) - X_r(k)\right)^2 + \left(\hat{X}_i(k) - X_i(k)\right)^2}{X_r(k)^2 + X_i(k)^2}} \times 100 \tag{I.55}$$

where:

k	denotes the instant of the measurement
$\hat{X}_r$	is the real part of the estimated synchrophasor
X_r	is the real part of the theoretical synchrophasor
$\hat{X}_i$	is the imaginary part of the estimated synchrophasor
X_i	is the imaginary part of the theoretical synchrophasor

In most of the test cases defined in the standard, the synchrophasor must be estimated with a maximum TVE of 1%. A 1% TVE is obtained if the magnitude is estimated with an error of ±1% assuming that no errors are made in the phase angle. Similarly, a phase angle of ±0.01 radian will cause by itself a TVE of 1% while synchronization errors of ±31 μs and of ±26 μs at respectively 50 and 60 Hz leads to the same TVE error.

Since theirs definitions have been included in [C3711b], the concepts of frequency and ROCOF have been precised in the latest PMU standard version where an effort has been made to clarify the concept of instantaneous frequency. The adopted definitions are based on the derivatives of the phase angle. To explain the reason of this choice, let us remind that phase angle estimations are time-tagged. If the frequency and ROCOF estimates are derived from the phase angles, it simplifies the time alignment of all three measurements. The definitions of frequency and ROCOF are given by [IEC15] as following:
"Given a sinusoidal signal:

$$x(t) = X_m \cos[\psi(t)] \tag{I.56}$$

Frequency is defined:

$$f(t) = \frac{1}{2\pi}\frac{\mathrm{d}\psi(t)}{\mathrm{d}t} \tag{I.57}$$

The rate of change of frequency (ROCOF) is defined:

$$ROCOF(t) = \frac{\mathrm{d}f(t)}{\mathrm{d}t}\text{"} \tag{I.58}$$

Frequency and ROCOF measurement errors, named FE are RFE respectively, are computed as the difference between the estimated values and those theoretical for the same instant of time. The new definitions, compared to those defined in previous standard version, do not consider the absolute values in their expression. There are given below:

$$FE(k) = f_{est}(k) - f_{th}(k) \tag{I.59}$$

where:

FE	is expressed in Hz
f_{est}	is the estimated frequency
f_{th}	is the theoretical frequency

$$RFE(k) = \frac{f_{est}(k2) - f_{est}(k1)}{t_{k2} - t_{k1}} - \frac{f_{th}(k2) - f_{th}(k1)}{t_{k2} - t_{k1}} \tag{I.60}$$

where:

RFE	is expressed in Hz/s
t_{k1}	is the time-tag at the instant $k1$ related to the phase angle at $k1$
t_{k2}	is the time-tag at the instant $k2$

Now, assuming that the frequency is a function of time, the deviation between the actual and the nominal frequency can be denoted by the function $g(t) = f(t) - f_0$. Based on that, the cosine wave $x(t)$ in Eq. (I.56) is written as:

$$\begin{aligned} x(t) =& X_m \cos[2\pi \int f(t)\mathrm{d}t + \varphi] \\ x(t) =& X_m \cos[2\pi f_0 t + (2\pi \int g(t)\mathrm{d}t) + \varphi] \end{aligned} \tag{I.61}$$

The synchrophasor representation of this waveform, taking into account the instantaneous frequency $f(t)$, is:

$$\overline{X(t)} = \frac{X_m}{\sqrt{2}} e^{j(2\pi \int g(t)\mathrm{d}t + \varphi)} \tag{I.62}$$

Under the definition given in Eq. (I.61), the computation of instantaneous synchronized phasors is possible if the observation window is composed of 1 sample only. Park's transform applied in the digital domain performs such rapid estimations as it has been deeply demonstrated and extensively tested in [Fra15]. Nevertheless, in most cases, the phasor estimation is performed after sampling the input signal during some time as it is the case for the DFT-based algorithm. Therefore, in such a configuration, the phasor estimates combine in a single quantity the dynamics taking place inside the window and represent an *average* of these dynamics. The same analysis applies for frequency and ROCOF measurements, so that truly instantaneous estimations of these parameters is not possible in practice. The 2011 version of the PMU standard has clearly mentioned this point and has recommended to time-stamp exactly at the middle of a given data window. This means that, the phase angle is correlated with a cosine function centered around the window as shown in Fig. I.28 where the window is delimited by the vertical green lines ($N = 9$ samples).

An interesting conclusion can be drawn from Fig. I.28. Despite the fact the synchrophasor time-tag is at $T_R = 0.02$ s, the computation of the synchrophasor estimate can only be performed when $\lceil N/2 - 1 \rceil$ [4] samples are generated from this time-tag to fill the considered window. The $\lceil N/2 - 1 \rceil$ samples introduce a delay equal to $(\lceil N/2 - 1 \rceil \times \Delta t_0)$ seconds which is added to the latency of the PMU. As a rule of thumb, any synchrophasor algorithm which incorporates a specific window to estimate the phasor introduces a delay equals to half that window length. Now, the IEC Standard 60255-118-1 defines the time interval as PMU reporting latency. For P-Class PMU, the maximum PMU reporting

4. $\lceil . \rceil$ denotes the round up mathematical operation

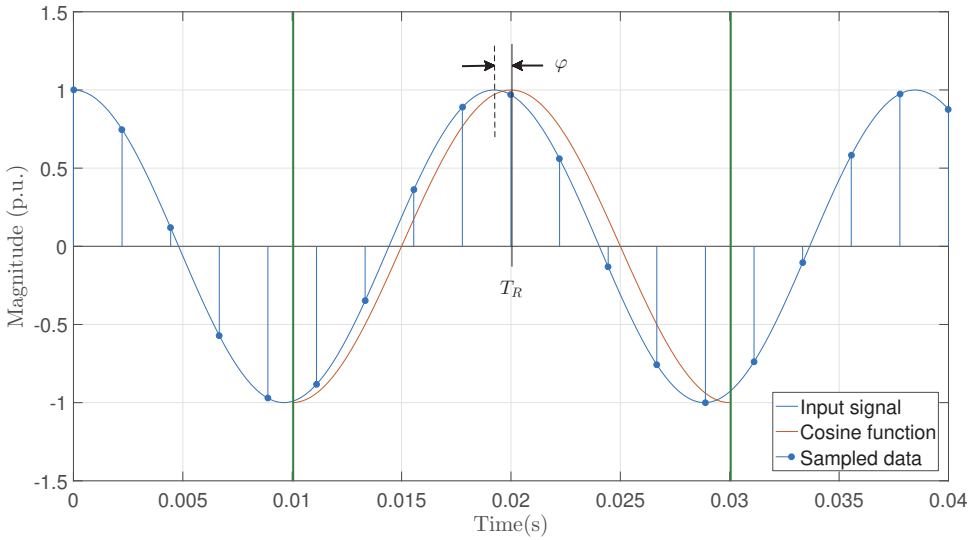

FIGURE I.28 – Illustration of the timestamp concept at the middle of a given window

latency, expressed in second, is

$$t_{lat} = \frac{2}{F_s}, \text{ being } F_s = f_{nom} \text{ for } F_s > f_{nom} \tag{I.63}$$

Clearly, Eq. (I.63) shows that synchrophasor-based algorithms must be designed in such a way that no more than 2 cycles of data of fundamental frequency are generated following the data report time T_R.

7.4 Reference signal processing model

To cope with the steady-state and dynamic test cases imposed by the PMU standard, two detailed signal processing models have been described in the appendix B in [IEC15], one is for P-Class PMU and the other for the M-Class. The principle of the algorithm of reference models is identical for both classes. It is based on the quadrature demodulation (or correlation) technique which consists in multiplying the input signal by a complex exponential locked to f_0 and filtering the interference term at frequency $2f_0$. By doing this, a perfect synchrophasor representation of the signal is obtained directly if the input signal is a pure cosine wave of fundamental frequency. The PMU model, adapted from [IEC15], is illustrated in Fig. I.29 where the complex exponential term is split into its cosine part and its sine part.

The model proposed by the standard assumes that the samples generated by the ADC are a perfect representation of the analogue signal and all the delays introduced by the acquisition chain are properly compensated. By ignoring the impact of the front end of the PMU, the algorithmic part is the relevant information that describes the synchrophasor estimation model. Based on this, the synchrophasor is measured directly from a given set

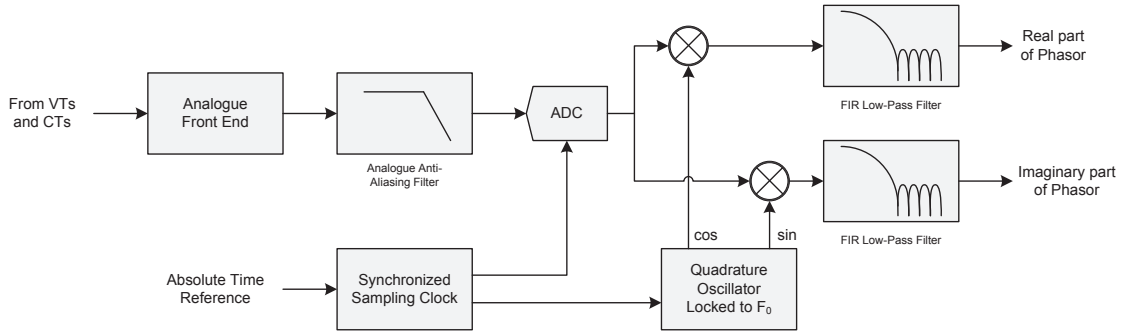

FIGURE I.29 – Simplified single phase PMU signal processing model

of samples x_k through the following formula:

$$\overline{X(k)} = \frac{\sqrt{2}}{G} \sum_{n=-N/2}^{N/2} x[k+n] \cdot w_{[}n] \cdot e^{-j\frac{2\pi}{N}(k+n)} \tag{I.64}$$

where:

N	is the order of the FIR low-pass filter
$w_{[}n]$	represents the coefficients of the FIR filter which depend on the performance class
G	is the gain of the filter, computed as $G = \sum_{n=-N/2}^{N/2} w_{[}n]$

Based on Eq. (I.64), the whole art of the reference model is precisely designing filters in such a way that the estimated synchronized phasors, frequency, and ROCOF are compliant with the requirements of the performance classes. Moreover, a particular attention must be paid to the way the phasor is computed. In particular, since the filter has a finite impulse response (symmetrical coefficients), its group delay is equal to $G_d = N/2$ samples in the passband. Since the delay shifts the samples to the right of a considered window, the phasor resulting from the shifted samples will be wrong if the time-stamp is at places other than that of the middle of that window. To counteract this phenomenon, the estimate $\overline{X(k)}$, given at the synchronized sample time k, is obtained by taking the $N/2$ "oldest" samples and the $N/2$ "newest" samples from the sample $x[k]$. This is shown in Fig. I.28 where 9 samples have been collected in exactly 1 fundamental cycle, that is $N = 8$ (9 taps). Now, if the estimation is performed at sample index $x[k + N/2]$ while the time-stamp is located exactly at the center of the observation window, then a natural compensation of the filter group delay is made and the resultant synchrophasor is correct. It should be noticed that this approach inevitably delays the estimation of the phasors by $(N/2)T_s$ seconds. In other words, a synchrophasor representation of the power system at the instant t is available at the PMU output at $(t + (N/2)T_s)$ seconds, excluding all other delays.

7.5 Implementation of synchronized phasor measurement in practice

Synchronized phasor measurements ensure an effective way to monitor the real-time operation status of a Wide-Area Measurement System (WAMS) improving substantially its reliability, observability, integrity and security [Pha08]. When a WAMS is associated to

monitoring, protection, and control functions, it is considered as a Wide-Area Monitoring, Protection, And Control (WAMPAC) system [TVC+11]. WAMPAC applications require the deployment of several PMUs across sufficient nodes of the electrical grid to achieve its complete observability [FCC13]. However, utilities have identified that the average overall cost for the deployment of synchrophasor systems ranges from 40 to 180 thousand dollars per PMU. The labor, including installation and commissioning, as a significant cost element whereas the PMU itself represents typically less than 5% of the average overall cost [oEEDR14]. In this context, widespread deployment of the PMUs may be slowed and utilities may look for other cheaper solutions. The integration of the PMU function into existing digital relays, already installed everywhere in the power systems, is part of them. Such dual-function devices avoid the additional cost associated with the wiring, engineering, and testing of standalone, or dedicated, PMUs which is a real benefit [ZKM+11].

A priori, it would appear at first glance that there is a gap between the synchrophasor reference model and the traditional architecture of numerical protection relays, despite the fact that both IEDs share a common task with the phasor estimation process. The former is based on the demodulation technique and a uniform sampling scheme whereas the latter commonly use the frequency tracking together with the DFT-based algorithm. It is therefore reasonable to wonder how implementations of synchronized phasor measurements are performed into products found in the market. Moreover, the question might be asked whether other synchrophasor algorithms may fulfill the exigencies of the standard. The answers to each of these questions are given in this subsection.

The first idea that comes in mind is to implement synchrophasors without altering the sampling process (adaptive sampling) to minimize the risk of affecting all other functions of the relay (protection, control and metering). If the samples are timestamped by the use of a combined Central Processing Unit (CPU) and DSP architecture, the target can be achieved as deeply explained in [KPA08]. This approaches is therefore particularly useful for relay signal processing schemes based on drivable ADC (Fig. I.21). First, the DSP drives the sampling clock of the ADC which is used to generate samples asynchronously with respect to the absolute time reference (samples at the output of the ADC in Fig. I.21). Then, the synchrophasor algorithm is processed. The first step consists in computing the center of the data window by averaging the timestamps based on the DSP time reference. Afterward, the CPU, synchronized to the 1 PPS signal, positions the instant when the synchrophasor shall be reported somewhere in the window. Subsequently, a first wrong synchrophasor is estimated through a *four-parameter model*, obtained through a first order Taylor's expansion, that has been designed to increase the accuracy of the classical Fourier algorithm under dynamic system conditions [KPA08]. The time difference between the averaged timestamps and the absolute time reference is finally computed to compensate the estimated synchrophasor through a phasor rotation.

The synchrophasor algorithm based on the four-parameter model may be substituted by another algorithm like the convolution synchrophasor algorithm described in [ZKM+11]. The main idea consists in mimicking the demodulation-based reference algorithm and adapting it to an asynchronous sampling scheme by means of convolution integrals. Here

also, the samples are generated asynchronously and the CPU provides an absolute time-mark to each of the samples. The input signal is convolved with a particular FIR low-pass filter using the corresponding timestamps to estimate the synchrophasor. The samples generated asynchronously are taken as they are whereas the values of the filter are estimated dynamically to match the unevenly spaced time-stamps. This can be made since the shape of the filter has been defined during its design. The value of the filter at each time-step is determined through a numerical approximation like the linear interpolation. An interesting point to mention regarding the algorithms found in [KPA08, ZKM+11] is the fact that the same variable sample streams are used to feed algorithms dedicated to protection and those related to synchrophasor estimation. The later is simply a new software which is included in parallel to the existing protection algorithms. Thus, the changes in the hardware platform are minimal and the cost saving is maximal.

Another possibility to integrate synchronized phasor measurements into a protection relay is the use of the fixed sample rate as showed in Figs. I.22 and I.23. Since the ADC sample rate is fixed, it can be synchronized to the absolute time reference so that the timestamped samples can be used directly by a synchrophasor algorithm. This concept has been introduced in [SAGC+03] where the synchrophasors have been estimated through the demodulation-based method recommended by the PMU standard. Moreover, in contrast to the two above-referenced algorithms, the synchrophasors have been used together with the line differential protection algorithm (ANSI 87L). In fact, the protection relay is equipped by a communication board that allows exchanges of synchronized phasors with another similar relay. Now, if the two relays are located at each end of the line while exchanging synchrophasors between each other, the line differential protection can be established.

Most of the state-of-the-art PMU algorithms are based on the uniform sample rate architecture because it simplifies the data acquisition process and the signal-processing analysis [DCV+13]. Thus, a protection relay resting on a fixed sampling frequency has a wide range of options to implement synchrophasor algorithms. The estimation of synchrophasors build around this architecture is divided into two groups: DFT-based algorithms and non-DFT algorithms. Among them, the DFT is the most common method used as it provides simple, elegant and accurate estimation of phasors [PT08a]. DFT-based algorithms suffer mainly from the leakage problem and many papers found in the literature propose various solutions to solve it. There are three main families of solution to give back the DFT its inherent robustness to estimate the parameters of interest.

The first solution consists in using a variable DFT window length to reduce the leakage error by synchronizing the DFT window to the estimated frequency [BPHS98, NL06]. However, the procedure is applicable only for discrete fundamental frequencies. An error will occur in the phasors estimate obtained through the DFT for other fundamental frequencies which is a serious drawback of the technique.

The second solution consists in exploiting the combination between windowing functions [Har78] with the Interpolated-Discrete Fourier transform (IpDFT), first introduced in [JCD79]. In this approach, both long-range and short-range leakages can be reduced, as

presented in [Gra83], where the Hanning window has been selected to show the superiority of the IpDFT with tapering over the classical IpDFT algorithm. Consequently, this solution has been applied to estimate synchrophasors and the performance of the algorithm has been evaluated through the TVE criterion in both steady-state and dynamic conditions following the IEEE Standard C37.118.1-2011 for the M-Class PMU in [BP12]. Subsequently, a lot of investigations have been performed for better characterization of the tapered IpDFT in terms of windowing functions [BP13] and size of the observation interval [BMP14] for both performance classes ; P-Class and M-Class PMU. Furthermore, [RP14a] has proposed an enhanced-IpDFT (e-IpDFT) to compensate for the spectral interference introduced by the negative image of the DFT spectrum and has shown very promising performances through real-time implementation. To conclude, most of these references solve the leakage problem of the DFT for off-nominal frequencies under both steady-state and dynamic conditions, making IpDFT algorithms very promising techniques. However, the aforementioned IpDFT algorithms, based on Hanning window, require a sampling rate much higher than the fundamental frequency (typically some tens of kHz) to avoid aliasing effect and make possible specific approximation needed by the algorithm [RPAP13]. Additionally, a minimum window length of 2 cycles is required to ensure that the distance between spectral lines suffices to allow effective leakage reduction by windowing [RP14b].

The third solution is the resampling techniques. These techniques aim at modifying the input samples towards an ideal signal sample sequence, whose sampling frequency is synchronized to the power system frequency. Phasor estimation is then performed using the resampled data. Reference [PT08a] shows that resampled data phasors have very little errors of estimation. The resampling technique cited above is based on trigonometric function which does not include the effect of the harmonics, that is why a high order filter is needed to send a pure sinusoidal signal to the algorithm. If the phasors of the harmonics are required, then a bank of FIR filters is needed. The use of high order filter introduces a delay which will make the system response slower.

There are number of alternative non-DFT-type algorithms for estimating the phasors. The most recent proposed algorithms adopt a dynamic phasor model whose foundation relies on the first order Taylor's expansion described above. This method has been extended to a second order Taylor's expansion in [PKA08] (six-parameter models) that is to improve measurement accuracy during large frequency drifts. Synchrophasors can be estimated with higher accuracy by using a least squares error optimization of Taylor's series coefficients [dlOS07] and a spectral window [aJPGdlOS10]. In particular, the LES approach over four cycles is one the most promising technique over Taylor's series as demonstrated by simulation in [BMP13]. Since such methods consider complex-valued data, high computational burden is required [BP14] which is a significant drawback for implementation.

8 Conclusion

In this chapter, the state of the art of the phasor estimation process applied to protection relays and phasor measurement units have been presented. Despite the fact that the DFT is applied by default in the protection field for phasor estimation, several alternatives of the DFT are proposed today to improve the accuracy of synchrophasor computations. Most often, these variants require higher computational burden and are more complex to implement than the simplest DFT-based algorithm for a slight improvement of accuracy. For these reasons, this study will propose signal processing solutions based on the DFT algorithm.

Nevertheless, the DFT suffers mainly from two pernicious phenomena: the aliasing and the leakage. Both have been mathematically formulated, described, and explained. Moreover, solutions to tackle the issues of both the aliasing and leakage effects have been presented from the relay and PMU perspectives. Aliasing can be reduced by the use of an anti-aliasing filter in the acquisition chain. Regarding the leakage, it is overcome differently depending on the IED considered, protection relay or PMU, as the sampling strategies involved are different. Indeed, the former typically samples at a rate synchronized to the power system frequency (frequency tracking) to solve the leakage problem. Instead, the latter must sample at a fixed rate synchronized to the GPS and uses methods belonging to one of the three main methods exposed in Section 7.5 to reduce the leakage. Most often, these methods require the knowledge of the power system frequency. In this context, two classical methods that are commonly employed have been highlighted, namely the zero-crossing technique and the phasor-based method. Preferences are given to the phasor-based method as it is based on the Fourier filter and thus takes advantage of its filtering property.

The successful implementation of a phasor estimation algorithm is obviously function of the robustness of the algorithm itself in accurately computing the phasors in a stringent environment. Nevertheless, the data acquisition chain is also of primer concern since it gives to the signal processing algorithms the digital representation of its analogue inputs. In this chapter, the data acquisition chain is an integral part of the IED and is designed according to the IED manufacturer objectives. However, with the evolution of power systems with smart grid paradigm and with more and more complex communication network, protection relays and PMUs need to reconsider the way to process electrical signals.

In this study, the proposed works are engaged to develop a new generation of signal processing algorithms for protection relays and PMUs on the basis of data flowing through communication network. For accomplishing this task, it is necessary to firstly understand what are the new trends taking place within the substations, especially in terms of communication protocols. These communication protocols are subject to standards that need to be analyzed and understood to clearly identify the breakthroughs with current technology and the related problematic. This is the core objective of Chapter II.

Chapter II

Future challenges of protection relays with the emergence of new standards related to Smart Grids

Contents

Abstract

Protection engineers now have available to them a large range of new communication technologies. Among them, standardized data protocols have been defined in the IEC Standard 61850 product family to allow interoperability between the various numerical relays within the substation. Particularly, IEC Standard 61850-9-2 has introduced the Process Bus concept which permits sending of, amongst others, time-stamped digitized

analogue values from the instrument transformers from the field to numerical relays. The Ethernet-based digital link substitutes hard copper wires but raises new problems related to the signal processing performed by protection relays. Indeed, few relays typically uses the frequency tracking for accurate estimation of phasors during frequency excursions whilst the time-stamped digitized analogue values flowing in the digital link are obtained using a fixed sample rate. Phasor Measurement Units can also use these sampled measured values as input signal to process their algorithms which can be based on either a fixed or variable sample rate. The core objective of this chapter is thus to highlight the new challenges of the sampled measured values from the signal processing perspective.

1 Introduction

Numerical protection relays belong to the IED family. In essence, they incorporate one or more microprocessors allowing them to exchange profitable data between equipments located on the field and or to the SCADA system. These data may be the instantaneous values of power system voltage, current, power flows as well as circuit breakers status and switches position [McD07]. From a protective relaying perspective, a traditional substation is typically structured around three levels called the equipment level, the bay (or cubicle) level, and the substation level. The equipment level consists of all primary equipments of the field, that is, for instance, CTs/VTs, switches and circuit breakers. The bay level involves the several IEDs of the substation ensuring their functions of protection, measurement, and control. The substation level contains the substation controller and the substation HMI. The former may be a remote terminal unit or a programmable logic controller and is responsible of collecting the data from the IEDs and presenting them to the remote clients in a standardized way. The HMI provides the window through which operator and maintenance personnels have access to a global view of the current state of the substation. In traditional substations, the link between the equipment level and the bay level is established through parallel hardwired connection whereas serial communication protocols are commonly implemented to permit the exchanges between the IEDs and the substation level equipments [PTD02].

Typically, legacy communication protocols used in the industry were developed with a view to minimizing the number of bytes flowing on the communication wire and providing all the functions necessary to control the power system. The optimization of the amount of data transmitted was necessary since early communication systems were limited in terms of bandwidth [Mac06]. Among the communication protocols used for telecontrol, some of them were issued from independent standards like IEC Standard 60870 and Distributed Network Protocol (DNP) while others were proprietary protocols such as Modbus and Profibus [XYN11]. Numerical relays have therefore two capabilities that utilities must consider: their capability to correctly detect faults in the power system and their capability to be integrated into the substation automation system. The integration capability involves both the physical interface, such as RS-232 and Ethernet, and the communication protocols implemented. In the past, it was common to choose relays for the performance of their protection functions only [McD07]. This resulted in substation automation systems where various protocols were involved as depicted in Fig. II.1.

In fact, proprietary and standardized protocols can coexist but this option usually requires communication gateways to convert the different protocols and enable the different pieces of equipment to communicate between each other. Thus, the integration of several IEDs from different manufacturers in the same SAS as well as the overall configuration of the system becomes a complex task. To reduce the installation costs and promote competition among manufacturers, end-users demand more interoperability between the devices. Interoperability can be achieved by using a unique standardized communication protocol. This is how was issued the IEC Standard 61850 [ABE03].

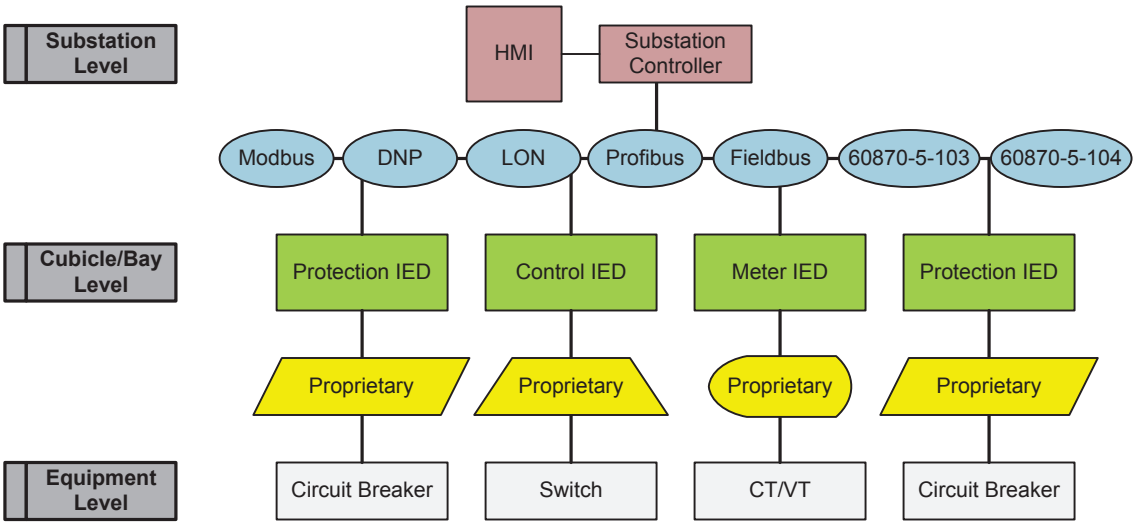

FIGURE II.1 – Traditional SAS architecture with various communication protocols

In this chapter, an overview of the IEC Standard 61850 is first given in Section 2 where the main features and benefits are highlighted. Since the standard is built around real-time exchange of data, it is obvious that time synchronization plays a crucial role in the deployment of smart substation. The synchronization issue is addressed in Section 2.3. Furthermore, the IEC Standard 61850-9-2, part of the IEC Standard 61850, introduces the Process Bus concept which permits sending of, amongst others, time-stamped digitized analogue values from the instrument transformers from the field to numerical relays, through merging units. These digitized values are used as input signals for the next generation of protection relays and must be thus consider to develop new signal processing methods. As a consequence, an explanation about the communication protocol defined in this specific part is given thereafter (Section 3). In addition, the Section 3 describes the evolution of this portion of the standard since its first release and its impact on the instrument transformers standardization community. The new version of the instrument transformer standard, called IEC Standard 61869, defines the updated requirements for instrument transformers while incorporating the communication protocol defined in IEC Standard 61850-9-2. The new requirements are discussed and analyzed in Section 4. Finally, on the basis of the conclusions drawn from this section, a merging unit design is proposed in Section 5 to deal with the measurement accuracy imposed by the PMU standard (Total Vector Error criterion).

2 Getting smart in the substation: IEC Standard 61850

In the early 1990s, the Electric Power Research Institute (EPRI) and the IEEE initiated to define an Utility Communications Architecture (UCA) for inter control center and substation to control center communications. In 1994, the EPRI and the IEEE continued to work on the UCA by starting to define the communication between the IEDs and the station computer. A similar work began by the Technical Committee (TC) 57 of the IEC in 1996. The next year, in 1997, the three entities agreed to combine and harmonize the efforts made to define a common international standard known as IEC Standard 61850.

The first edition of the standard, often referred to IEC Standard 61850 Edition 1, was initially composed of 10 main parts and was released in 2003. Since the product family standard is designed to evolve to accommodate future system growth and cover the entire suite of power utility domain, the majority of the standard has been tagged Edition 2 in 2009. In addition, some parts are still under review and will be published Edition 2.1 in the near future [MAG09].

The communication architecture reference model built in Fig. II.1 shows a vertical communication, that is the information is flowing from the equipment level to the substation level. The IEC Standard 61850 replaces this traditional vertical communication by an hybrid one which is both vertical and horizontal as shown in Fig. II.2. The latter is made possible since the standard is designed to offer interoperability between devices in the substation. This means that devices are able to exchange information directly because they understand each other.

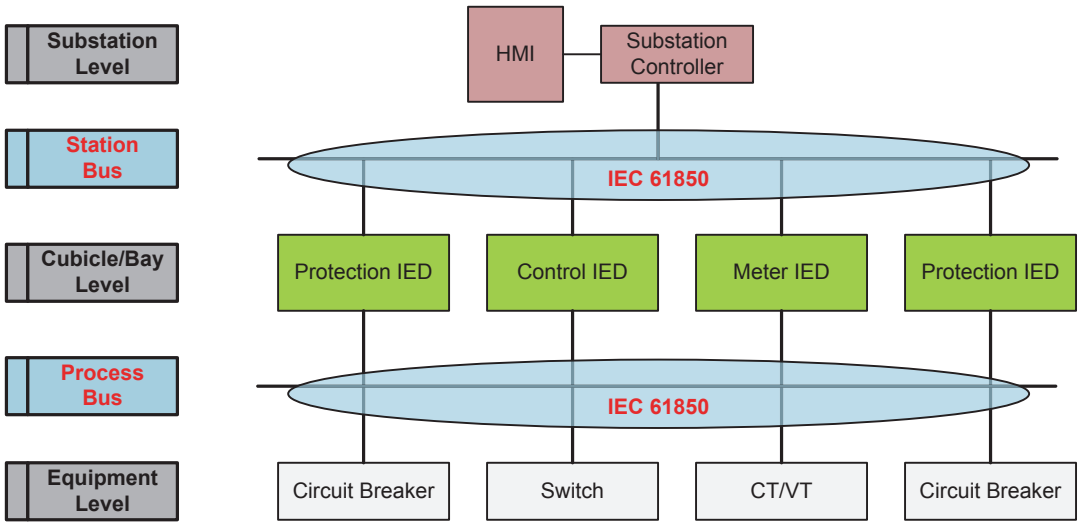

Figure II.2 – IEC Standard 61850 intention in the SAS

As shown in Fig. II.2, the IEC Standard 61850 introduces two architectural components called the Station Bus and the Process Bus. On the one hand, the Station Bus transmits information between the IEDs, and between the station level and the bay level. On the other hand, the Process Bus is used to carry streams of process data between the apparatus of the field and between the equipment level and the bay level. The concept of numerical protection relays is thus going to evolve as they will have to process data frames instead of analogue values to run their algorithms. In accordance with this thesis objectives, namely the design of new signal processing algorithms for numerical relays, the data transferred through the Station Bus are disregarded in this manuscript. Instead, it is necessary to characterize the data flowing through the Process Bus from the signal processing perspective building on the standardized relevant information. To do so, let us start by providing a brief description of three main key elements contained in the IEC Standard 61850 so that to ease the understanding of the communication principle described in the IEC Standard 61850-9-2, known as Process Bus [smaie11]. These key elements

are the data model, the communication services and the time synchronization.

2.1 The data model

The IEC Standard 61850 is more than just a communication protocol which defines how bytes are transmitted on the communication network. It is based on a object-oriented data model (virtualized model) that is used to represent an automation system. In what it follows, the automation system will be considered as a protection IED. The objective of the data model is to provide an abstract view of the IED and its objects. To do so, the data model is structured in a hierarchical way starting from the physical device (IED) that is connected to the network and identified by its network address. Each physical device regroups one or several Logical Device(s) (LD) which allow the IED to act as a gateway. LDs are containers of Logical Nodes (LN). A LN is one of the elementary functions performed by a given IED and transmitted on the network. Each LN has a unique name ; as an example, the Logical Node **XCBR** denotes the breaker elementary function and is reserved for this purpose. LNs not only specify the interfaces of the process like circuit breakers, switches, and current and voltage transformers but also model the software functions such as the distance protection of a protection relay. The detailed definitions of LNs can be found in IEC Standard 61850-7-4 [smaie10b]. LNs are commonly broken down to a collection of Data Objects (DO) which have a unique name as well. DOs are often considered as the center of the data model because it defines the semantic and brings the valuable information. **XCBR** is composed, for instance, of Data Objects **Pos** and **NamPlt** which gives the breaker position and the device nameplate respectively. The characteristics of the Data Object **Pos** are called Data Attributes (DA). To exemplify, the DA **stVal** of the DO **Pos** can be "true" or "false" depending on the actual status of the breaker position, close or open respectively [AES]. The hierarchical structure of the data model is depicted in Fig. II.3.

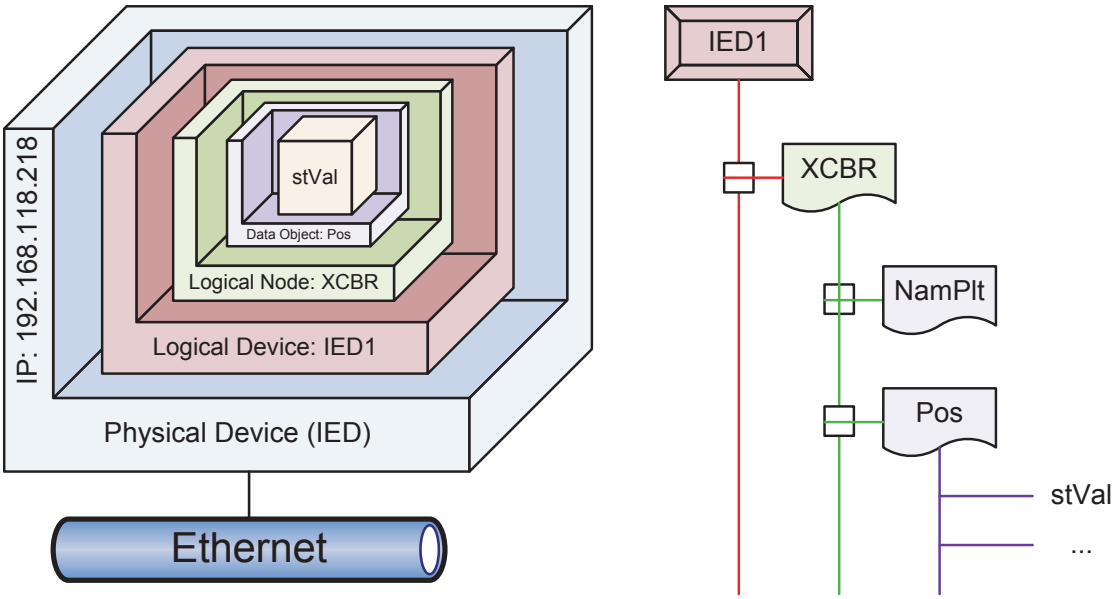

FIGURE II.3 – Modeling approach adopted by the IEC Standard 61850

2.2 The communication services

As stated earlier, the LNs are the information to be exchanged. The next step is to define how to exchange them. The information exchange services are introduced in the IEC Standard 61850-7-2 [smaie10a]. As it is the case for the data model, [smaie10a] adopts also the abstract definition of the services. For this reason, [smaie10a] is often known as Abstract Communication Service Interface (ASCI). On the overall, the different services are based on two types of exchanges: on request, and spontaneous. The former is based on the request-response principle which is commonly deployed in client-server architectures. This method involves a requestor (server) which sends a request message for some data to a replier (client). The client receives the message, processes it, and returns a message in response to the requestor. In 61850 terms, the association model related to this type of exchange is called Two Party Application Association (TPAA). TPAA is used by almost all services provided by [smaie10a]. Nevertheless, the Sampled Measured Values (SMV) service, used for real-time exchange of data through the Process Bus, is based on the association model called MultiCast Application Association (MCAA) which is nothing more than peer-to-peer communication. MCAA rests on the publisher-subscriber messaging pattern where the publishers broadcast [1] their data in the network and the subscribers express interest (subscribe) in one or more messages. These SMV frames are the data which must be used as input signals by the future generation of IEDs.

The communication services described in the ASCI part are virtual. However, exchange of data are made possible only if the services are implemented into a real protocol that can meet the data and services requirements. This mapping is discussed in the Specific Communication Services Mapping in the IEC Standard 61850-8-1 [smaie10c]. The standard Open Systems Interconnection (OSI) seven layer model has been chosen to meet the basic requirements of the standardization process, that is interoperability and future-proof (must be able to follow the progress in communication technology as well as evolving system requirements). The IEC 61850 data models and services are built over the application layer (7^{th} layer) of the OSI model (see Fig. II.4) which means that they are independent of any real protocol. In other words, the IEC 61850 data model and services may be theoretically mapped to any protocol. However, among the protocols that are practical to implement and that can operate within the computing environment found in the industry, the Manufacturing Message Specification (MMS) has been originally chosen because it supports complex named objects and most of the services proposed by IEC 61850 (not only read, write, and report services). In the OSI model, the MMS protocol suits has a Transmission Control Protocol/Internet Protocol (TCP/IP) stack above the Ethernet layer. This MMS mapping profile is used for all the client-server services which provides the guarantee to the delivery information [RM13]. However, the MMS stack over TCP/IP profile cannot be used for time critical communications because it makes the transfer time too slow. Indeed, a mapping to the application layer requires that the services must passed through each communication protocol stack before being conveyed to the wire. Messages resulting from this mapping are typically transferred in the range of $[100; 500]$ ms and are therefore suitable for SCADA applications [PD15]. On the flip side, the SMV frames,

1. The messages are not conveyed to a specific receiver

used for protection and control purposes, must be transmitted in less than 10 ms for the distribution networks and in less than 3 ms for the transmission networks [PD15]. Thus, to eliminate processing of any middle layers, the SMV messages are mapped directly to the link layer of the Ethernet [60112] as shown in Fig. II.4.

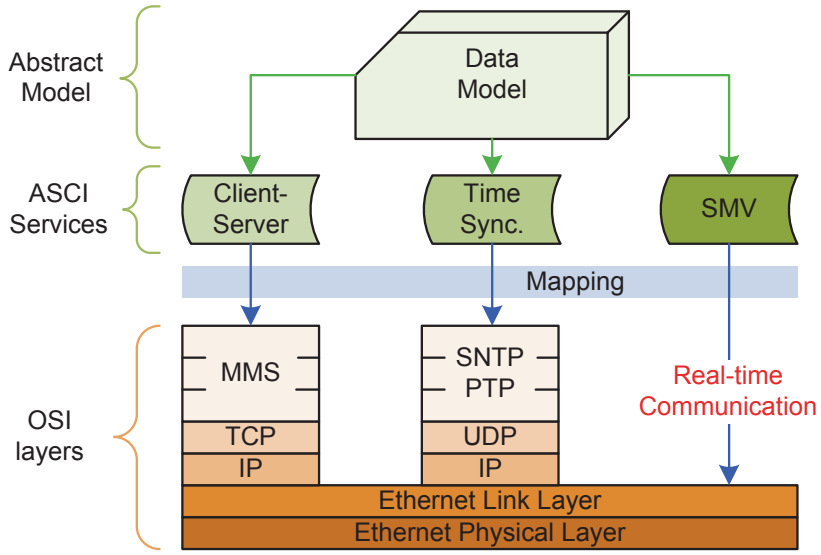

FIGURE II.4 – Mapping profile under IEC Standard 61850

2.3 Synchronization within smart substations: Precision Time Protocol

The mapping of time synchronization is also reported in Fig. II.4. Time synchronization, denoted as "Time Sync." in Fig. II.4, brings the local clocks of servers and other instrumentation in a network into phase so that their time differences will be zero. A precise time synchronization is necessary among devices in substations to reduce the effort involves with comparing event information from digital disturbance recorders [BFL06]. IEC Standard 61850 supports, in essence, the time information: each DO and DA can be timestamped. The standard series defined in Part 5 [smaie13] the components of the model for time synchronization between two devices. The model is based on the association model TPAA where the server is externally synchronized to an absolute time reference which is the GPS. Two protocols may be used for transmission of synchronization messages: Simple Network Time Protocol (SNTP) and Precision Time Protocol (PTP). Both protocols are mapped to a User Datagram Protocol (UDP) layer which permits a fast transmission of the timestamp with minimal cost. Finally, in contrast to the TCP point-to-point connection, UDP supports multicast allowing the server to transmit simultaneously the time synchronization message to multiple clients.

For distributing the time synchronization signals, the IEC 61850 standard series have initially proposed SNTP because it operates on the same Ethernet-based network infrastructure as 61850-based protocols and provides a time accuracy in the millisecond range. Such a time accuracy is suitable for most of the current measurement and control applications like disturbance recorders or sequence-of-events. However, some specific communication services offered by IEC Standard 61850 require an absolute accuracy better than

1 μs. SMV and synchronized phasor measurements are part of them [SEZL07]. A time accuracy of 1 μs or better may be achieved with PTP which has been standardized in the IEEE Standard 1588-2008 after being first voted a standard in 2002 [2] [45708]. Unlike time synchronization methods like Inter-Range Instrumentation Group B (IRIG-B) requiring a dedicated wire to transmit the timestamps, PTP can use Ethernet to reach the same goal. In other words, PTP provides time synchronization suitable for all timing applications in SAS while using the existing network infrastructure [BRR16].

The basic idea of PTP is to synchronize a *slave* clock **S** to a *master* clock **M** in such a way that both clocks share the *same* time information. The master clock is determined automatically by the best master clock algorithm which is a specific feature of the IEEE Standard 1588-2008. The master clock is unique in the Ethernet network and all other clocks (slaves) synchronize their time to the master's one. The principle of the synchronization algorithm is to measure the time derivation t_{MS} between the two clocks as shown on Fig. II.5. To do so, the clock **M** sends a packet, referred to as synchronizing message *Sync*, to a slave clock through the Ethernet network and notes the time t_1 at which the *Sync* message was sent. This time information t_1 is conveyed to the slave clock by encoding it in a *Follow_Up* message which is sent following the synchronizing packet. The slave clock receives the *Sync* message after an elapsed time t_D, called Master-to-Slave Time, which is caused by both the cabling and the network components like switches. Following the receipt of the *Sync* message, the slave **S** generates another timestamp t_2 based on its own clock. Now, the objective is to measure the Slave-to-Master time by reversing the process. The slave clock sends a *Delay_Req* packet to the master clock and notes the timestamp t_3 in the meantime. The master clock receives this message at a time t_4, embeds the time information in a *Delay_Resp* message, and sends the later to the clock **S**. Now, the slave clock has four timestamp values and uses them to compute t_{MS} based on the Eq. (II.1) following [WAA+15]:

$$t_{MS} = \frac{t_2 - t_1 - t_4 + t_3}{2} \tag{II.1}$$

The clock of the slave is corrected based on the computation of t_{MS}. Typically, this correction is performed continuously once per second to ensure the timing accuracy forever. The computation of t_{MS} relies on the assumption that the propagation delays (Master-to-Slave and Slave-to-Master delays) are identical. However, this assumption is not true in practice since the Ethernet switches store the packets some times before forwarding them. The duration of time the packet spends passing through the switch is called the residence time. The residence time is function of a variety of parameters such as the network load and the architecture of the switch. Due to the residence time, the computation of the propagation delays will be wrong. To overcome this issue, PTP has introduced the concept of Transparent Clock. Transparent Clocks referred to switches which have the capability to measure the residence time Δ and encode it into the corresponding PTP packet that is currently flowing through the switch. In IEEE 1588 version 2 a new message field has been added for this purpose, the so called Correction Field (denoted "corr" in Fig. II.5). The slave clock receiving this packet accounts for both the origin timestamp (t_1 or t_3) and the residence time during the computation of t_{MS} [WAA+15].

2. The standard of 2008 is often called IEEE 1588 v2 and the protocol PTP v2

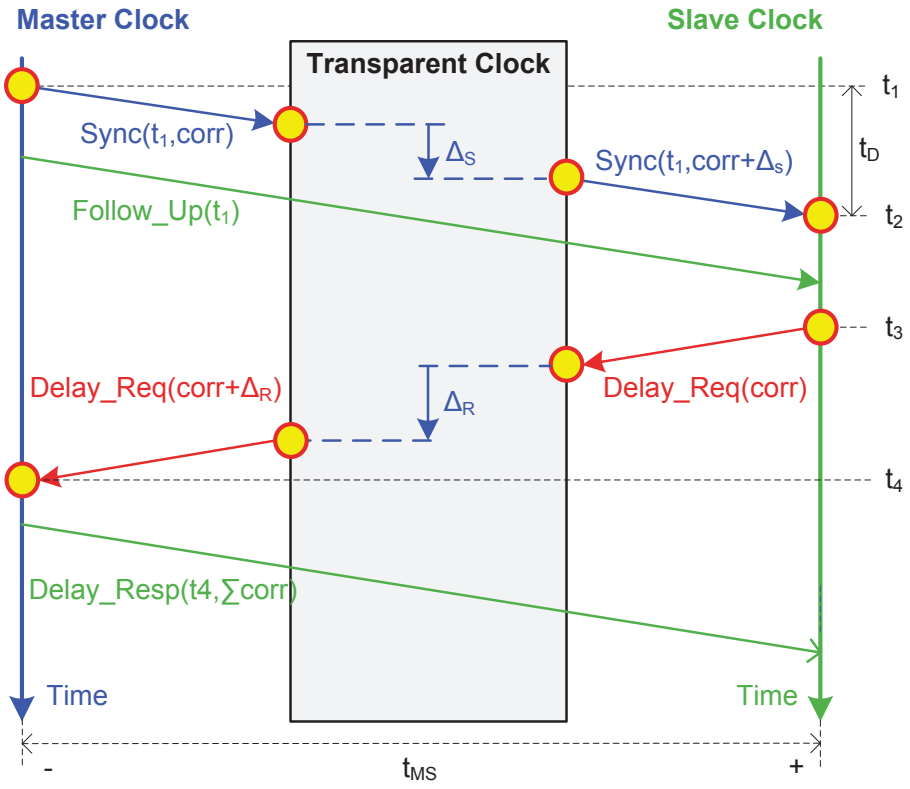

FIGURE II.5 – Precision Time Protocol synchronization principle

The description of three important aspects of the IEC Standard 61850 has just been given: the data model, the communication service, and the time synchronization. In a nutshell, the SMV messages are encapsulated Ethernet frames of data, synchronized to an absolute time reference, transmitted through the Process Bus, and used by the next generation of IEDs. They have been introduced for the first time in the IEC Standard 61850-9-2 before being considered in greater details in subsequent standards. The objective of the next section is thus to describe the evolution of the IEC Standard 61850-9-2 while highlighting the relevant information that will be used to analyze the impact of SMV frames on the relay signal processing.

3 IEC Standard 61850-9-2 and its evolution

3.1 IEC Standard 61850-9-2: an overview

The Process Bus concept has been defined in IEC Standard 61850-9-2 [smaie11]. It puts emphasis on the decoupling between the power system signals acquisition and the exploitation of data by protection relays or others devices like PMUs. The Process Bus permits sending of digitized analogue and binary input/output values from the equipment level to the bay level. The Merging Unit (MU) is the interface between the primary equipment (instrument transformers, switches, and circuit breakers for instance) and the Process Bus.

It acquires analogue signals as well as digital data from the primary equipment, digitizes them and sends the Ethernet frames to the Process Bus through a fiber optic link. The use of such a digital link reduces copper wiring and eliminates high energy signals coming from conventional instrument transformers which makes the maintenance the IEDs safer and easier [CYW+11]. Process Bus communication protocol specifies a configurable dataset which can be transmitted on a multicast basis from one publisher (MU) to multiple subscribers (IEDs). The digitization of the analogue signals stipulates that the MU incorporates an acquisition chain. According to [smaie11], the sample rate is not specified, but shall be synchronized to an absolute time reference. The synchronization of MUs is mandatory since it allows a given IED to align in the same time basis the *samples* coming from different MUs. With synchronized SMV, applications like differential protection, synchronized phasor measurements and digital fault recorder are made possible. Without loss of generality, the Process Bus concept is illustrated in Fig. II.6.

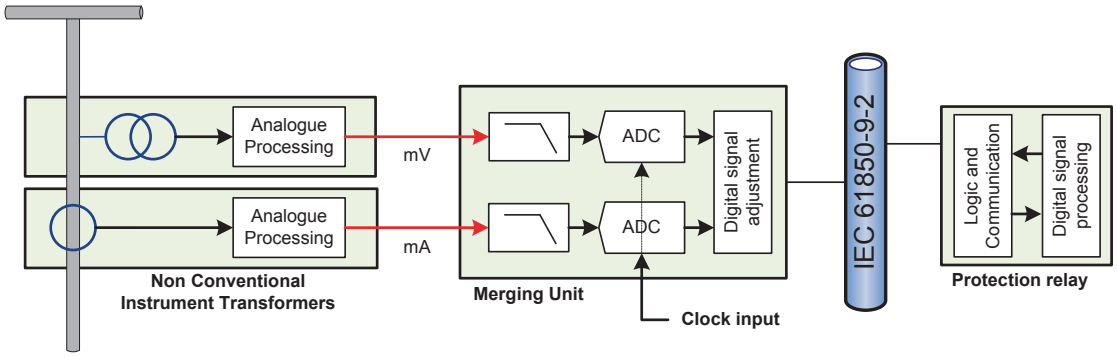

FIGURE II.6 – Process Bus concept

3.2 Utility Communications Architecture guideline: IEC Guideline 61850-9-2LE

IEC Standard 61850-9-2 is, in essence, a protocol largely open to the future. Because of this, many parameters such as the dataset elements contained in the SMV frames, the sample rate, and the publishing rate are not fixed. Since neither the dataset nor the sample rate are specified (basically no information about the samples), it is difficult for IEDs to process SMVs and design any signal processing algorithm. An interoperability issue between MU and IEDs has to be solved. To overcome this issue and speed up the deployment of the Process Bus technology, the IEC 61850-9-2LE guideline document [Gro04] has been released from the joint efforts of several major manufacturers under the UCA International Users Group [TS08]. It specifies the dataset *PhsMeas1* containing eight elements: the three-phase voltages and currents and their associated neutral. In addition, the sample rate for protection application has been set to 4,000 Hz whatever the power system frequency is (80 samples even if the nominal frequency is 50 or 60 Hz). Each set of current and voltages samples are coded in a single Ethernet packet which is sent to the Process Bus at a rate of 4,000 frames per second. Finally, the 1 PPS synchronization method has been recommended for synchronizing MU clocks.

3.3 IEC Standard 60044 and its substitute: IEC Standard 61869

In addition to the work driven by the Technical Committee 57 responsible for IEC Standard 61850, efforts have been made by TC 38 to restructure the IEC Standard 60044 series which defines requirements for instrument transformers. The new set of standard is a product family standard and is known as IEC Standard 61869. This product family standard supersedes the IEC Standard 60044 series. It defines a method for digital communications of instrument transformer measurements based on the IEC Standard 61850 and introduces the notion of Stand-Alone Merging Unit (SAMU) which will be discussed in details in Section 4.3. Nevertheless, it is important to mention that the SAMU, defined in the IEC Standard 61869-13 [Tra16a], is considered as interface for Process Bus in this study.

4 Signal processing requirements imposed by IEC 61869 standard series

The product standard family takes the form of “Russian doll" where its parts are nested within each other. In such an arrangement, the SAMU shall not only be compliant with the IEC Standard 61869-13 [Tra16a] but it has also to fulfill the general requirements for instrument transformer specified in IEC Standard 61869-1 [Tra07], the additional general requirements for Low Power Instrument Transformers (LPITs) in IEC Standard 61869-6 [Tra16b], and the digital interface for instrument transformers in IEC Standard 61869-9 [Tra16c]. In the forthcoming subsections, the requirements of the instrument transformer product family standard related to the signal processing field are be first described and analyzed.

4.1 IEC Standard 61869-6: anti-aliasing filter requirements and harmonic measurements

This part of IEC Standard 61869 covers only additional general requirements for low power instrument transformers. For the signal processing field, the main objective of this part of the standard is to characterized the behavior of the MU in terms of its frequency response. Therefore, the requirements are related to the attenuation of the anti-aliasing filter and the measurement accuracy of harmonics in terms of amplitude and phase angle. These requirements are applicable for a specific rated range of frequency which is from 96% to 102% of the nominal frequency f_0 (48 to 51 Hz for a 50 Hz system) and depends on the MU accuracy class as discussed below.

MUs, like any measuring device, are not free from errors and these errors deteriorate the accuracy with which the IED estimates parameters of interest like synchrophasors. In a nutshell, the measurement accuracy of a given IED involves the MU accuracy class and the IED algorithms. Typically, two sources of error exist in instruments transformers and are called ratio error and phase error ; the former changes the amplitude of the signal while the latter introduces a phase shift. These two errors are merged into a single criterion in this study for simplicity, namely the combined error. The purpose of accuracy classes is

to classify instrument transformers as function of the combined errors. For MUs, accuracy classes represent all of the errors introduced between the input analogue signals and the SMV frames published in the Process Bus, including time synchronization errors. In other words, accuracy classes could be seen as a criterion describing how accurate is the timestamped encoded output message compared to the analogue signal.

As pointed out in the IEC Standard 61869-6, accuracy classes are distinguished between protection accuracy classes and measurement accuracy classes. On the one side, protection accuracy classes are used to operate protection relays and shall have *good* accuracy during short-circuit conditions. On the other side, measurement accuracy classes are designed to have an extremely high precision around the nominal operating conditions. IEC Standard 61869-6 defines four measurement classes which are called 0.1, 0.2, 0.5, and 1. All the requirements imposed by the product family standard differ according to these accuracy classes. The strictest requirements are associated with the accuracy class 0.1 whereas those weakest apply for accuracy class 1. Furthermore, the exigencies are identical for all protection classes. In what it follows, the requirements will be presented step by step throughout this study.

According to the IEC Standard 61869-6, the anti-aliasing filter attenuation depends on the first frequency aliasing on the nominal frequency defined as $F_s - f_0$, where F_s corresponds to the digital output sample rate. This parameter is set in the IEC Standard 61869-9 as discussed in the next subsection and is equal to 4,800 Hz. The minimum attenuation is given in Table II.1 below.

Table II.1 – Anti-aliasing minimum attenuation as function of accuracy classes

Accuracy class	**Anti-aliasing filter attenuation (dB)** ($f \geq F_s - f_0$)
0.1	≥ 34
0.2	≥ 28
0.5	≥ 20
1	≥ 20
All protection classes	≥ 20

Harmonics are of interest for protection purposes as discussed in Section 2 of Chapter I. Therefore, MUs should introduce light distortions to harmonics so that reliable data are available to the inputs of IEDs. The magnitude and phase error are specified in this part of the standard for each accuracy class mentioned earlier. They are listed in Table II.2 and Table II.3 for measuring and protection accuracy classes respectively. The limits apply equally to both current and voltage channels.

Table II.2 – Harmonics ratio and phase errors as function of measuring accuracy classes

Accuracy class at f_0	Ratio error at low frequency (%)		Ratio error at harmonics (%)					Phase error at low frequency (degrees)	Phase error at harmonics (degrees)			
	DC	1 Hz	2^{nd} to 4^{th}	5^{th} and 6^{th}	7^{th} to 9^{th}	10^{th} to 13^{th}	$> 13^{th}$	1 Hz	2^{nd} to 4^{th}	5^{th} and 6^{th}	7^{th} to 9^{th}	10^{th} to 13^{th}
0.1	+1 −100	+1 −30	1	2	4	8	+8 −100	45	1	2	4	8
0.2	+2 −100	+2 −30	2	4	8	16	+16 −100	45	2	4	8	16
0.5	+5 −100	+5 −30	5	10	20	20	+20 −100	45	5	10	20	20
1	+10 −100	+10 −30	10	20	20	20	+20 −100	45	10	20	20	20

Table II.3 – Harmonics ratio and phase errors as function of protection accuracy classes

Accuracy Class	Ratio error at harmonics (±%) 1^{st} to 5^{th}	Phase error at harmonics (± degrees) 1^{st} to 5^{th}
All protection classes	10	10

4.2 IEC Standard 61869-9: digital interface for instrument transformers

The IEC Standard 61869-9 defines requirements for digital communications of instrument transformers having a digital output. The communication profile adopted is a subset of the IEC 61850 standard series. The latter specify a large set of communication models and services which are not used in MUs. Only a few of them need to be implemented and are defined in terms of conformance classes. The conformance classes are distinguished by a simple letter, being **a**, **b**, **c**, and **d**. The class **a** defines the minimal set of services required to transmit MU data using SMVs whereas the class **d** supports all optional services defined in [Tra16c] which are not considered in this study. This is why the analysis of this part of the standard series is performed for the class **a**.

This part of the standard extends the work started with the IEC 61850-9-2LE guideline by introducing more requirements and superseding those of the guideline. These requirements are listed in Table II.4.

The first major change is related to the output sample rate. Instead of defining the sample rate in terms of number of samples per cycle (s/c), the new standard expresses the sampling rate in hertz. 80 s/c is independent of the power system nominal frequency and is therefore applicable for 50 and 60 Hz systems. Based on that, the equivalent sample rate is 4,000 Hz and 4,800 Hz for a 50 Hz and a 60 Hz system respectively. Now, expressing the sampling rate in Hertz modifies the number of samples acquired in exactly 1 power

Table II.4 – Differences between IEC 61850-9-2LE and IEC Standard 61869-9

Requirements on	**IEC 61850-9-2LE**	**IEC 61869-9**
Sample rate	80 s/c	4,800 Hz
Synchronization	1 PPS	PTP
Dataset	4 I + 4 U	FfSsIiUu
Delay time	none	2 ms

system fundamental cycle. Indeed, considering the rate 4,800 Hz, 80 samples are gathered in 1 cycle of a 60 Hz system whereas 96 samples are acquired in 1 cycle of a 50 Hz system. As clearly specified in the standard, the preferred rate for general measuring and protective applications is 4,800 Hz and this is not fully compatible with the 9-2LE guideline. To ensure backward compatibility with the 9-2LE guideline, another sample rate of 4,000 Hz is permitted for use on 50 Hz systems even if not recommended. **Thus, this study considers the preferred sample rate for the design of signal processing algorithms** in the current chapter as well as in Chapter III and Chapter IV.

Whatever the sample rate is, it shall be synchronized to an external time source. Despite the fact that 1 PPS synchronization method have been first recommended by [TS08], preference is given to PTP in [Tra16c]. MUs can claim any of the two synchronization methods, or both. In any case, the accuracy shall be better than 1 μs. Moreover, a sample counter (SmpCnt) is used to identify the samples within the present second and to code their sample times. SmpCnt increments from 0 to 4799 then repeats. The sample times are obtained by dividing the value contains in SmpCnt by the preferred sample rate. Therefore, if the MU is synchronized to the GPS, SmpCnt is zero at the top of the second mark.

Furthermore, in contrast to the guideline, several dataset variants are permitted in the new standard series. These variants are given in a human readable notation which describes the MU capabilities as shown below:

$$\mathrm{F}f\mathrm{S}s\mathrm{I}i\mathrm{U}u$$

where:

f	is the digital output sample rate expressed in samples per second
s	is the number of dataset contained in each SMV frame
i	is the number of current quantities contained in each SMV frame
u	is the number of voltage quantities contained in each SMV frame

Let us assume that a given MU has 1 current and no voltages at its input channels and publish SMV frames compatible with the new standard. Based on the above-mentioned notation, the MU shall be described as F*4800*S*2*I*1*U*0*. In this configuration, the two datasets consist of 1 sample each, but are identified by a different value of SmpCnt. This means that each SMV frame regroups two consecutive samples, each sample is obtained at a specific sample rate. By doing this, the MU publishes 1 SMV frame after acquiring two samples. Therefore, the publishing rate is 2,400 frames per second. Moreover, MUs could

implement variants with other numbers of currents and voltages. The minimum number of current plus voltage allowed is 1. The maximum number of quantities is 24. However, MU claiming compliance to the new standard shall be configurable to implement the preferred rate and at least one of the two backward compatible variants defined in the standard. Backward compatibility with the 9-2LE guideline has been requested by manufacturers which have already implemented SMV frames capability in their products following the recommendation of the guideline. Backward compatible variants are described as F*4000*S*1*I*4*U*4* and F*4800*S*1*I*4*U*4*, for a 50 Hz and a 60 Hz nominal system frequency respectively. In accordance with these namings, the SMV frames contain only 1 dataset. This means that the publishing rate is 4,000 or 4,800 frames per second depending on the nominal frequency. It is therefore straightforward to conclude that, for an identical dataset, the 9-2LE guideline implementation requires at least around 1.67 more communication bandwidth than IEC Standard 61869-9.

The 9-2LE guideline defines the communication profile. However, the maximum amount of time required to pass the analogue signals through the MU acquisition chain and create the SMV frames is not indicated. Thus, the messages can effectively appear at the digital output after an elapsed time of 1 s, 1 hour, or even 1 year. In contrast to instrument transformers with analogue outputs, this delay adds to the relay fault detection time (operating time). To overcome this issue, the notion of processing delay time t_{pd} has been introduced in the new product family standard. It is defined as the difference between the time encoded by SmpCnt and the time the message appears at the digital output. Among the acquisition chain of the MU, the major delay time components are:

— the anti-aliasing filter that introduces a time delay, constant or variable depending of the structure employed, prior to the ADC
— the constant conversion delay of the ADC
— the message assembly and processing which may introduce a variable delay between the acquisition of the sample and its availability as a SMV packet at the MU output

The summation of all of these delays forms the processing delay time. It does not include any delays that occur after the SMV frames leave the MU output such as the Process Bus network delay. The maximum processing delay time allowed for protection purpose is 2 ms. However, MUs are allowed to publish SMV frames with less than 2 ms, if capable. The maximum processing delay time can be determined as illustrated in Fig. II.7, adapted from [Tra16c].

In this example, the sample identified by SmpCnt 0000, which encodes a time of xxx.0000 s, reaches the MU output at time xxx.0009 s, so the processing delay time for this sample is 0.9 ms. As no longer processing delay time exists in this example, 0.9 ms is also the maximum processing delay time. Notice that the ADC sample instants are shifted slightly to the right from the absolute sample times to take into account for the ADC conversion delay. Finally, the last point to highlight concerns the position of the sample counter SmpCnt against the absolute time marks. Taking SmpCnt 0000 as example, it is not aligned with the 1 PPS synchronization signal but is delayed by approximately 0.4 ms. This delay is mainly introduced by the anti-aliasing filter and must be compensated

during the timestamping process, as performed in Fig. II.7. To exemplify, suppose that the 1 PPS synchronization signal occurs at a peak of a cosine wave. This cosine wave will be first filtered, so subject to the filter group delay, and then sampled. Now, the timestamping process must consider this group delay and assign the correct timestamp to the filtered signal in such a way that, when SmpCnt values are aligned with their corresponding absolute sample times, SmpCnt 0000 is located exactly at the peak of the analogue cosine wave.

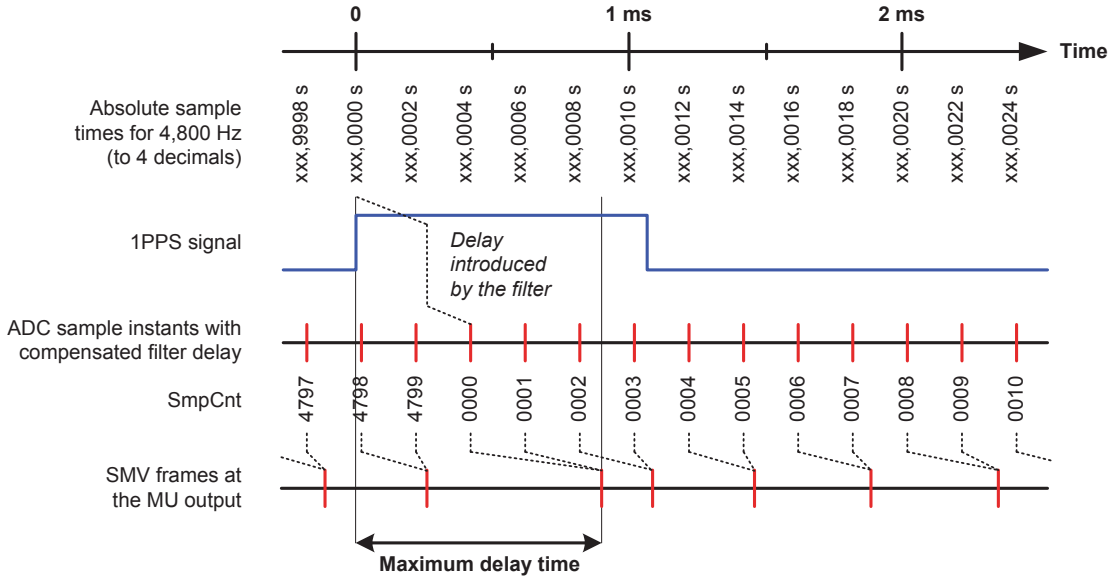

FIGURE II.7 – Measurement of the maximum processing delay time

4.3 IEC Standard 61869-13: Stand-Alone Merging Unit

Merging Units are designed for a specific Non-Conventional Instrument Transformer (NCIT). NCITs provide a low power current (mA) or voltage (mV) signal at their output and MUs interface to NCITs through this low power link. Unlike MUs, SAMUs are used to convert the secondary signal of **any conventional instrument transformer** into SMV frames compliant with the IEC Standard 61869-9. SAMUs have started to be defined in Part 13 of the IEC 61869 product standard family. A first draft version of this part of the standard was released in March 2016 [Tra16a]. IEC Standard 61869-13 introduces some preliminary definitions for SAMU which will could be changed and/or superseded by others in the future. Nevertheless, in this study, the current definitions of the standard are considered. Today, the definition of SAMUs applies only for conventional instrument transformers and for Alternative Current (AC) applications. NCITs producing low-level signals are considered out of the scope of this part of the standard. The input channels of SAMUs could be current signals having typically 1 A and 5 A, and/or voltage signals having typically 100 V phase-to-phase. A SAMU concept example is shown in Fig. II.8 where the three-phases current and voltage signals have been considered with their respective neutral. Of course, depending on the targeted application(s), the signal arrangement can be different and may consist of current signals only, voltage signals only, or any current and voltage signals combination. In any arrangement, the SAMU must be compliant with

IEC Standard 61869-9. Instrumentation based on conventional instrument transformers and NCITs with their related MU are reported in Fig. II.8 for comparison.

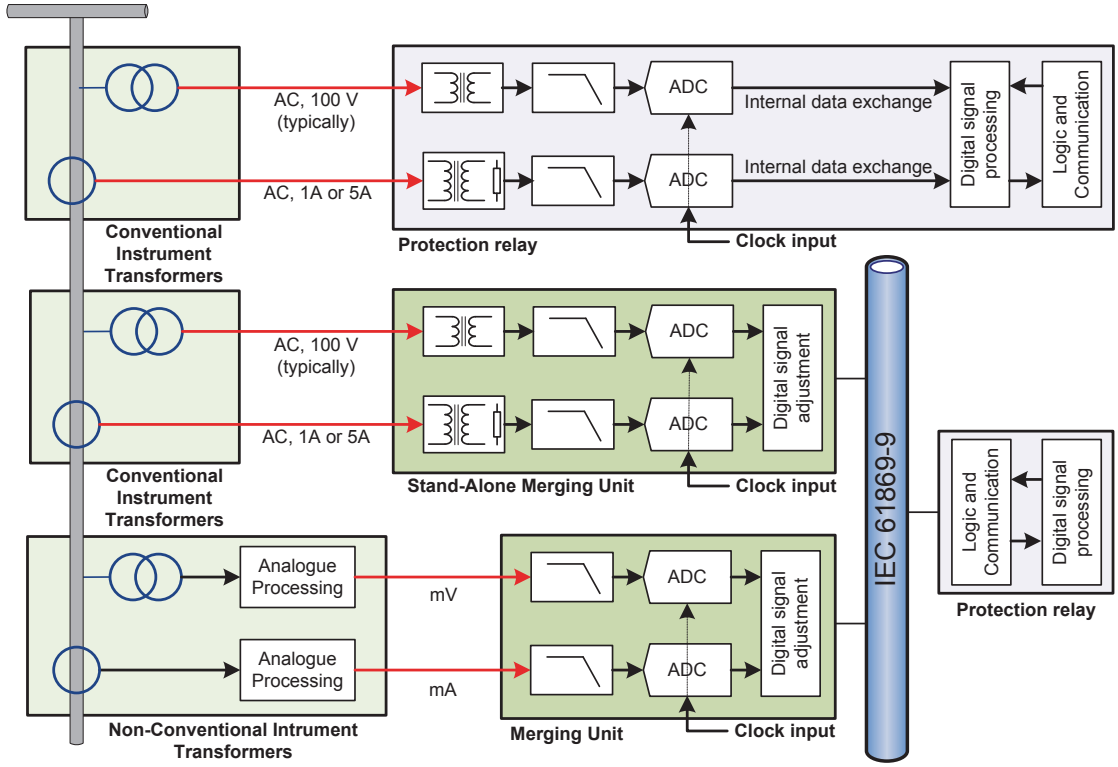

FIGURE II.8 – SAMU concept in contrast to NCITs and their associated MU and to traditional instrumentation

The use of MU/SAMU brings an interesting point: the relay manufacturer is no more responsible for the acquisition chain. When it was the case, the errors introduced by the DAQ in the analogue input signals were known and compensated in software. See the Section 3 of Chapter I to remind the impacts of each of the main components of a given DAQ on the input signals. Thus, the protection relay algorithms were designed to compensate for the deficiencies that occurs within the known DAQ. Now, the new generation of signal processing and protection algorithms must be based on the samples produced by MUs/SAMUs and encoded into Ethernet frames. Despite the fact that the IEC Standard 61869 product family imposes the most important signal processing constraints, the MU/SAMU is, from the relay designer perspective, a kind of "blackbox" since its detailed characteristics are not known. The purpose of this section is thus to provide firsts analysis about the measurement accuracy of SAMUs and its impact on the signal processing operations performed by intelligent electronic devices.

4.3.1 Accuracy classes with dual rating and dynamic range limits consideration

SAMUs are classified in terms of accuracy classes which incorporate all errors between SAMUs input channels and the digital output. With regards to accuracy classes, SAMU

channels are split into two groups which are measuring channels and protection channels. Now, theses accuracy classes, whatever the application is, are specified according to the nature of the SAMU input channel, that is voltage or current. For SAMU voltage channels, the accuracy classes apply equally on measuring and protection channels and are segregated as follow: 0.1, 0.2, 0.5, 1, and 3 [Tra16a]. Table II.5 presents the current error ($\epsilon(\%)$) and phase error (Δ_φ) for various voltage accuracy classes.

Table II.5 – Limits of voltage ratio error and phase error for SAMU voltage channels

Accuracy Class	**Ratio error** ($\epsilon(\%)$) ($\pm\%$)	**Phase error** (Δ_φ) $\pm$ centiradians
0.1	0.1	0.15
0.2	0.2	0.30
0.5	0.5	0.60
1	1.0	1.20
3	3.0	Not specified

For SAMU current channels, measuring accuracy classes are called 0.1, 0.2, 0.5, 1, 3, and 5. In contrast to voltage channels, the standard has introduced the notion of dynamic range specification for current channels. Dynamic range specification states the range of current over which the stated accuracy applies. The range of current is delimited by I_{min} and I_{max} which are respectively the lower limit and the upper limit of the range, expressed in percent of rated current. The preferred values for the dynamic range limits are $I_{min} = 1, 5, 10, 20, 50$ and $I_{max} = 120, 150, 200, 400$. They can be chosen independently and can be freely combined. Table II.6 lists the maximum allowed ratio and phase errors as function of metering accuracy classes [Tra16a].

Table II.6 – Limits of current error and phase error for SAMU measuring accuracy current channels

Accuracy Class	**Current ratio error** ($\pm\%$) **at current (% of rated)**			**Phase error ($\pm$ centiradians) at current (% of rated)**		
	I_{min}	100	I_{max}	I_{min}	100	I_{max}
0.1	0.1	0.1	0.1	0.15	0.15	0.15
0.2	0.2	0.2	0.2	0.3	0.3	0.3
0.5	0.5	0.5	0.5	0.9	0.9	0.9
1	1	1	1	1.8	1.8	1.8
3	3	3	3	5.4	5.4	5.4
5	5	5	5	9	9	9

From Table II.6, it can be noticed that the class designation of metering instrument transformers refers to the ratio error at the rated condition, that is for the specified dynamic range. Thus, a Class 1 has a 1% ratio error over its dynamic range while a Class 0.1

has only 0.1% ratio error. Phase errors are not considered in the class designation. Moreover, for current channel only, there are two protection accuracy classes which are named respectively 1TPE and 5TPE. Protection classes introduce the composite error criterion to classify CTs. The composite error regroups the ratio error and the phase error into a single parameter. Historically, the introduction of the composite error has been done to witness the beginning of the magnetic core saturation of the protection CT. Saturation may occur during strong short-circuit conditions involving relatively long primary time constant. Unlike measuring classes defining the ratio errors at rated condition, the composite errors apply on a larger current level range to take into account for the short-circuit current level. This range is called accuracy limit factor which can take the values 5, 10, 15, 20, and 30 [Tra16a]. Under this definition, the protection class 1TPE with an accuracy limit factor of 20 shall introduce a maximum of 1% total error at 20 times the rated current.

On top of that, IEC Standard 61869 Part 9 and Part 13 impose dual accuracy class rating. Dual rating means that a given protection instrument transformer has measurement capability conforming with a specific measurement accuracy class. So, protection channels shall deal with both measuring and protection applications. Conversely, metering channels of SAMUs are used only for measuring applications since they do not have protection capability. **Hence, for protection channels, the accuracy over the dynamic range limits is expressed using the metering part of the dual rating pair** and this metering part gives better accuracy.

Analogue instrument transformers whose secondary are linked to the SAMU inputs have also their own measuring accuracy class which may be different to the one of the SAMU. It is clear that these ITs distort the analogue voltage and current signals before the SAMU use them for SMV publishing. This means that each of the components of the instrumentation channel, from the primary analogue signals to the SAMU outputs, is playing its part in adding errors. The accumulation of these inaccuracies reduces the allowable margin of error for the signal processing algorithms performed inside the IED, especially for synchrophasor estimates. For the purpose of this study, the analogue signals available at the SAMU inputs are considered as a perfect representation of the voltage and current signals flowing in the power system. As a consequence, the errors introduced by the analogue ITs are disregarded so that to highlight the impact of SAMU combined errors on the relay-based PMU algorithms and more particularly on the synchrophasor estimates. The reason why the analysis is done for synchrophasors is because they have to be estimated according to the standardized TVE criterion as defined in the PMU standard. Protection functions, however, are not subject to standardized thresholds so that manufacturers of relays are free from claiming any accuracy for these functions. However, as a rule of thumb, it is common to find accuracies varying from 1% to 5% in relay manuals, that is above the 1% TVE criterion.

4.3.2 Impact of the combined error on the Total Vector Error criterion

As seen above, the IEC Standard 61869-13 defines metering ITs and protection CTs using the ratio error, the phase error, and the composite error criteria. However, the IEC

Standard 60255-118-1 uses the TVE criterion to evaluate synchrophasor estimates. Thus, to quantify the error introduced by instrumentation in a given synchrophasor estimation algorithm, it is necessary to rewrite the accuracy criterion in order to bring them to the same basis. The definition of the TVE involves the real and imaginary parts of a given estimated phasor $\hat{X}(k) = \hat{X}_r(k) + j\hat{X}_i(k)$ which is compared to its theoretical value $X(k) = X_r(k) + jX_i(k)$. By writing $\hat{X}_r(k)$, $\hat{X}_i(k)$, $X_r(k)$, and $X_i(k)$ in their polar form, it is possible to express the TVE in terms of ratio error and phase error as shown in Eq. (II.2).

$$\begin{aligned} TVE(k) &= \sqrt{\frac{\left(\hat{X}_r(k) - X_r(k)\right)^2 + \left(\hat{X}_i(k) - X_i(k)\right)^2}{X_r(k)^2 + X_i(k)^2}} \times 100 \\ &= \sqrt{\left(\frac{\hat{X}(k)}{X(k)}\cos(\hat{\varphi}(k)) - \cos(\varphi(k))\right)^2 + \left(\frac{\hat{X}(k)}{X(k)}\sin(\hat{\varphi}(k)) - \sin(\varphi(k))\right)^2} \times 100 \\ &= \sqrt{\left(\frac{\hat{X}(k)}{X(k)}\right)^2 - 2\frac{\hat{X}(k)}{X(k)}\left(\cos(\hat{\varphi}(k) - \varphi(k)) + 1\right.} \times 100 \\ &= \sqrt{\left((1 \pm \epsilon(k)) - \cos(\Delta_\varphi(k))\right)^2 + \sin^2(\Delta_\varphi(k))} \times 100 \end{aligned} \tag{II.2}$$

where:

$\epsilon(k)$	is the ratio error in percentage
$\Delta_\varphi(k)$	is the phase error in radian

Equation (II.2) expresses the TVE as a function of the ratio error and the phase error and is therefore useful for metering accuracy classes analysis. It can be noticed from Eq. (II.2) that the TVE gives identical results whatever the sign of Δ_φ is. Moreover, if $\pm 1\%$ ratio error is introduced on a given signal of magnitude 1, that is a magnitude of 0.99 or 1.01, the results of the TVE will be different. Figure II.9 illustrates the relationship between TVE, ratio error, and phase error for $\epsilon(\%)$ and Δ_φ ranging from -5% to $+5\%$ and from -10 centiradians (crad) to +10 crad respectively. Figure II.10 provides a two dimensional view of Fig. II.9 and draws the TVE criterion as function of the phase error for various ratio errors. Similarly, Fig. II.11 depicts the TVE as function of the ratio error for various phase errors.

The first conclusions emerging from Figs. II.10 and II.11 is that the combined error shall be located at the pointed-end of the cone-shaped so that the equivalent TVE introduced in synchrophasors are below the 1% threshold. The two conditions to fulfill to ensure that the SAMU does not cause by itself a TVE of 1% are:

— The ratio error $\epsilon(\%)$ must be less than 1%
— The phase error Δ_φ must be less than 1 crad

Therefore, in accordance with Tables II.5 and II.6, voltage channels claiming for accuracy class 1 are not suitable for synchrophasor applications while current accuracy classes 1, 3, and 5 must be equally avoided. Now, the objective is to highlight the equivalent TVE introduced by voltage and current measuring accuracy classes 0.1, 0.2 and 0.5 on Fig. II.9.

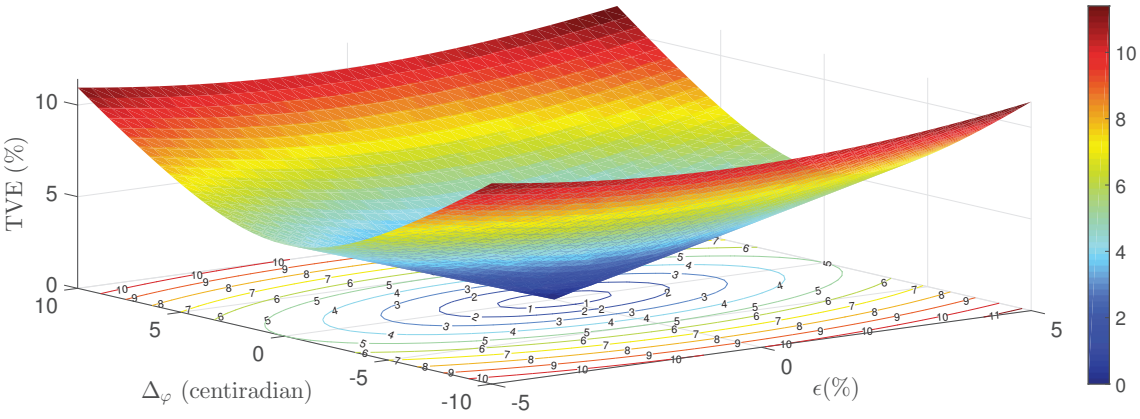

FIGURE II.9 – TVE as function of $\epsilon(\%)$ and Δ_φ - 3D view

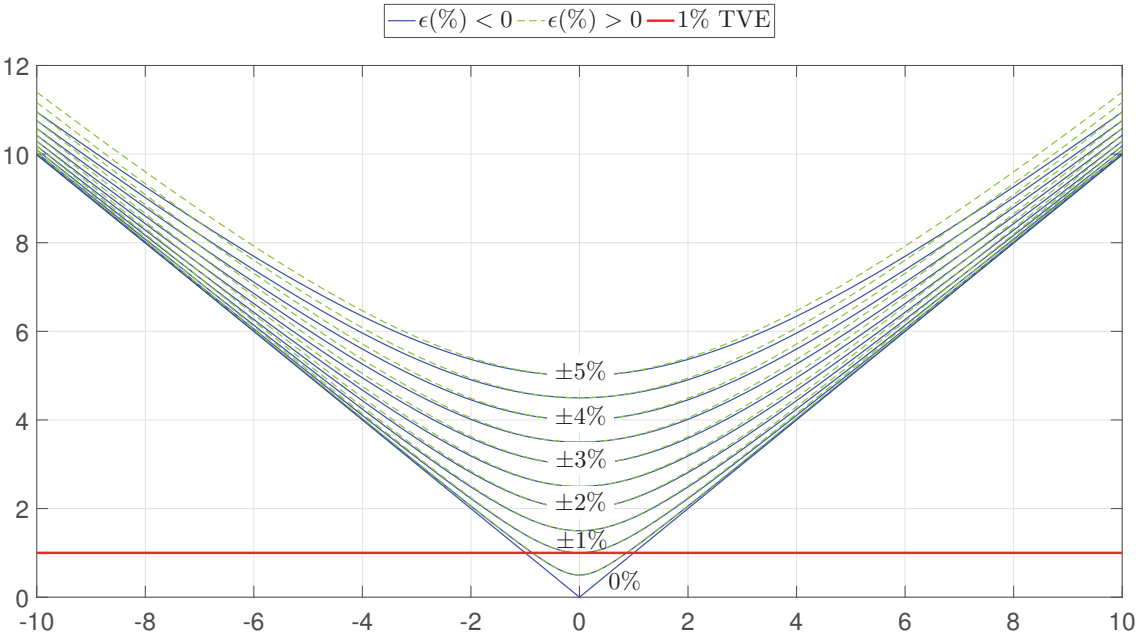

FIGURE II.10 – TVE as function of Δ_φ for various $\epsilon(\%)$

Figures II.12 and II.13 illustrate the projection of TVE values on the XY plane (top-down view of Fig. II.9) for voltage and current metering accuracy classes respectively.

These figures show that accuracy classes 0.1, 0.2, and 0.5 may be used for estimation of synchrophasors since none of these classes cross the 1% threshold. The limits of each zone represent the maximum permissible TVE for each class. This means that a SAMU claiming Class 0.1 accuracy for its voltage channel shall introduce a combined error falling somewhere within the area delimited by the Class 0.1 blue ellipse of Fig. II.12. Now, if this SAMU makes any measurement error outside this area, then this SAMU cannot claim for Class 0.1 accuracy. Same remarks apply for any other voltage or current accuracy class.

On the other hand, the composite error and the TVE share some similarities because each of them reflect the combination of the errors committed on the estimates. Actually,

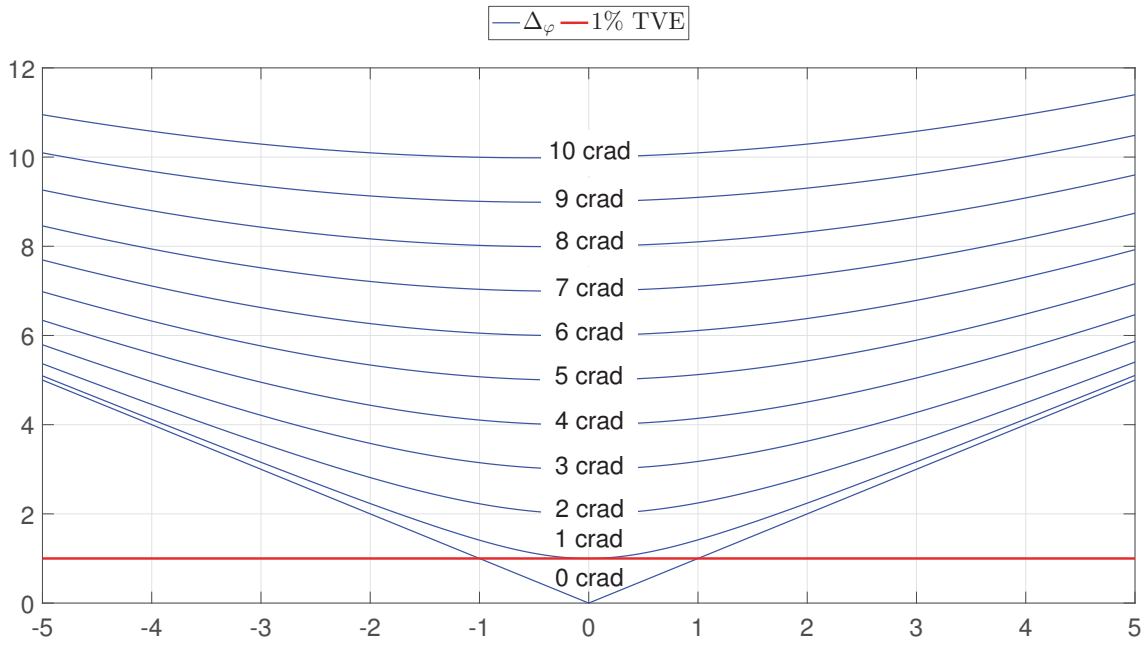

FIGURE II.11 – TVE as function of $\epsilon(\%)$ for various Δ_φ

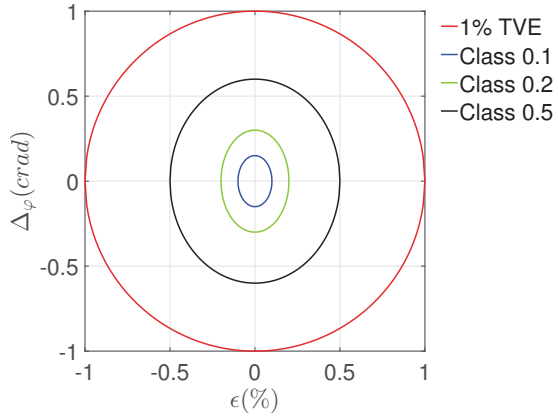

FIGURE II.12 – TVE introduced by voltage metering accuracy classes

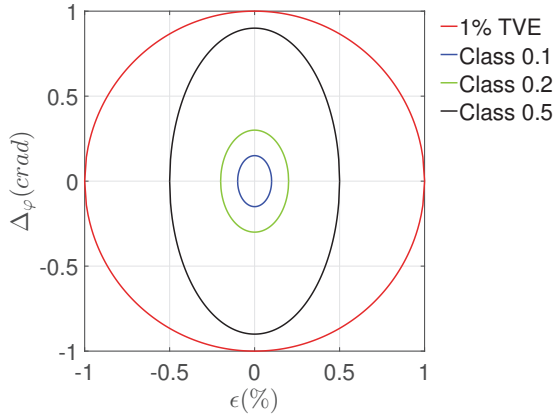

FIGURE II.13 – TVE introduced by current metering accuracy classes

it can be demonstrated that the composite error and the TVE have exactly the same meaning for sinusoidal signals [dBRdRAJT13]. So, a protection accuracy class 1TPE may introduce TVE values ranging from 0% to 1%. Clearly, neither class 1TPE nor class 5TPE are suitable for synchronized phasor measurements. However, in accordance to the dual rating pair requirement, a given protection channel guarantees a metering accuracy class capability over the specified dynamic range. As a consequence, protection channels can be used to estimate synchrophasors only over the dynamic range selected.

In this section, the studies performed have demonstrated that the selection of the SAMU metering accuracy class is of primer concern for the design of signal processing algorithms since they introduced errors in both magnitude and phase angle. In the next section, a SAMU accuracy class 0.1 is designed on the basis of the standardized requi-

rements that have been presented. A class 0.1 is chosen since it gives better accuracy than other classes while maximizing the allowable margin of error for the signal processing algorithms performed for synchrophasor estimations. The design has the double objective of proposing signal processing methods with minimal errors and anticipating future applications arising from the adoption of the Process Bus as explained below.

5 Proposition of signal processing methods for class 0.1 Stand-Alone Merging Unit

The study performed in [Lei16] pointed out a transition phase during which substations using conventional instrument transformers and substations adopting the Process Bus approach will cohabit in the future. For applications like line differential protection, it is anticipated that configurations mixing SAMU-based Process Bus at one line end and with analogue inputs at the other line end will be frequently encountered. Thus, the new generation of protection relays should consider this transitional period and propose a solution suitable to cover configurations where only digital substations are used, only conventional substations are used, or both are used at the same time. Such a solution could be based on the coexistence of a SAMU integrated into the numerical relay to deal with copper wires and an optical port dedicated to collect SMVs from the Process Bus as depicted in Fig. II.14. The use of an integrated SAMU eases the design of signal processing algorithms for protection functions and synchrophasor measurements since they will have to process samples generated in a standardized way.

Moreover, assuming that the integrated SAMU is compliant with the IEC Standard 61869, the samples it generates can be assembled into SMV frames, sent to the Process Bus, and used by other IEDs having SMVs as input. Obviously, there is no need to convert samples generated by the integrated SAMU into SMV frames if they are used directly by the signal processing algorithms. This brings the advantage to save the computational effort related to the communication required to create the Ethernet frames and decode these frames before using the valuable information they contain by the signal processing algorithms.

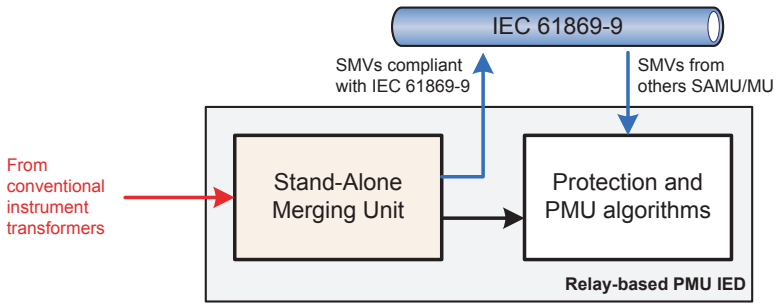

Figure II.14 – Relay-based PMU design principle

To simplify reading the choices made for the design of the SAMU, a reminder of the signal processing requirements of SAMU measuring class 0.1 is presented in Table II.7.

The ratio and phase errors reported in Table II.7 apply for the rated range of frequency also specified in the same table. Errors allowed outside this frequency range have been already specified in Table II.2.

TABLE II.7 – REMIND OF MAIN REQUIREMENTS FOR THE DESIGN OF THE SAMU

Requirement on	**Value**	**IEC 61869 Part**	**Subclause**
Current and voltage ratio errors (±%)	0.1	13	5.6.1301
Current and voltage phase errors (± crad)	0.15	13	5.6.1301
Maximum processing delay time	2 ms	9	6.902.2
Digital output sample rate	4,800 Hz	9	6.903.3
Rated frequency range (Hz)	96% to 102% of f_0	6	5.6 and 6.904
Anti-aliasing filter attenuation $f \geq F_s - f_0$	$\geq$ 34 dB	6	6A.3 (Appendix)
Accuracy for harmonics and low frequencies	See Table II.2	6	6A.4 (Appendix)

The last point to mention is that, since the gain is generally expressed in dB, it is necessary to convert the ratio error values. To do so, the formula following may be used:

$$X(dB) = 20\log(1 + X) \tag{II.3}$$

where:

$X(dB)$	is the gain in dB
X	is the ratio error value in %

In Eq. (II.3), if $X = -100\%$, the value $X(dB)$ is considered to be $-\infty$. Based on this, the magnitude response and the phase error masks of the SAMU accuracy class 0.1 can be plotted as shown in Figs. II.15 and II.16 where a fundamental frequency of 60 Hz has been considered without loss of generality.

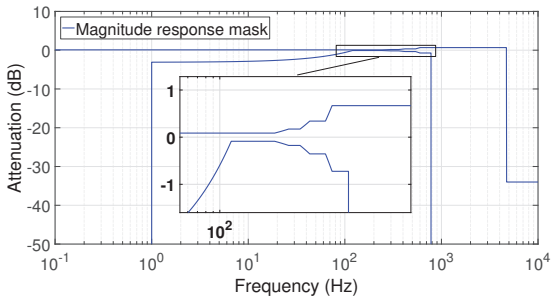

FIGURE II.15 – Magnitude response mask

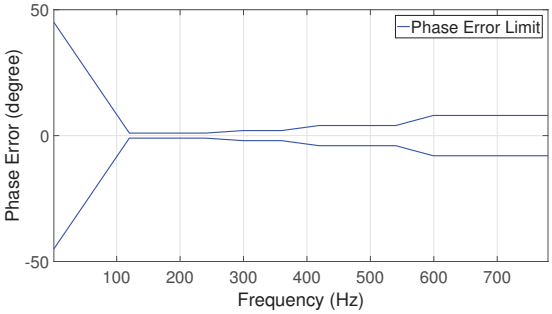

FIGURE II.16 – Phase error mask

5.1 General overview of the SAMU accuracy class 0.1

Typically, to design a merging unit, two main approaches could be found in the literature regarding the sampling strategy: either the ADC samples the input signals at the fixed digital output sample rate such as [WmXyY11], or an oversampling process followed by a

downsampling operation to produce the required data rate is used as done in [HKZN13]. However, none of the references found considers the new signal processing requirements imposed by the IEC Standard 61869, unlike the work presented below.

As defined in the IEC Standard 61869-9 subclause 6.903.3, the preferred sampling rate for protection applications is 4,800 Hz. However, it does not mean that the ADC of the SAMU shall sample the analogue signals at this specific sampling rate. Different sampling rates may be used along the signal processing path, the only constraint relies on the digital output sampling rate of the SAMU which has to be equal to 4,800 Hz. This allows the use of the well-known oversampling process, whose benefits have been presented in Section 3.2 of Chapter I. Of course, when the samples are obtained, digital filters and downsampling must be applied to respectively filters out alias frequencies (as the signal bandwidth is equal to 2,400 Hz) and create the 4,800 Hz sample streams. The sampling rate of the ADC is fixed to 28,800 Hz (the input signals are oversampled by a factor of 6). With such a sampling rate, the proposed SAMU design could also be suitable for further development of power quality applications in the future, whose preferred sampling rate is 14,400 Hz. The simplified signal processing diagram of the proposed SAMU is depicted in Fig. II.17 where the 8 channels of voltage and current signals specified in the 9-2LE guideline have been selected as input signals without loss of generality. It is also assumed that the current signals shown in this figure are passed through idealized interposed CTs and converted to voltage signals prior to being further converted into numbers.

Furthermore, the "Message Assembly" block is represented for indication purpose only and is not considered in this study since it deals with data encapsulation to create Ethernet frames. Data of interests from the algorithmic perspective are the value of a given sample and its corresponding timestamp. Thus, as the scope of this thesis is focused on innovative signal processing techniques rather than the creation of SMV frames, there is no need to define this block. Finally, it should be noticed that the choices made for this design will be progressively explained thereafter.

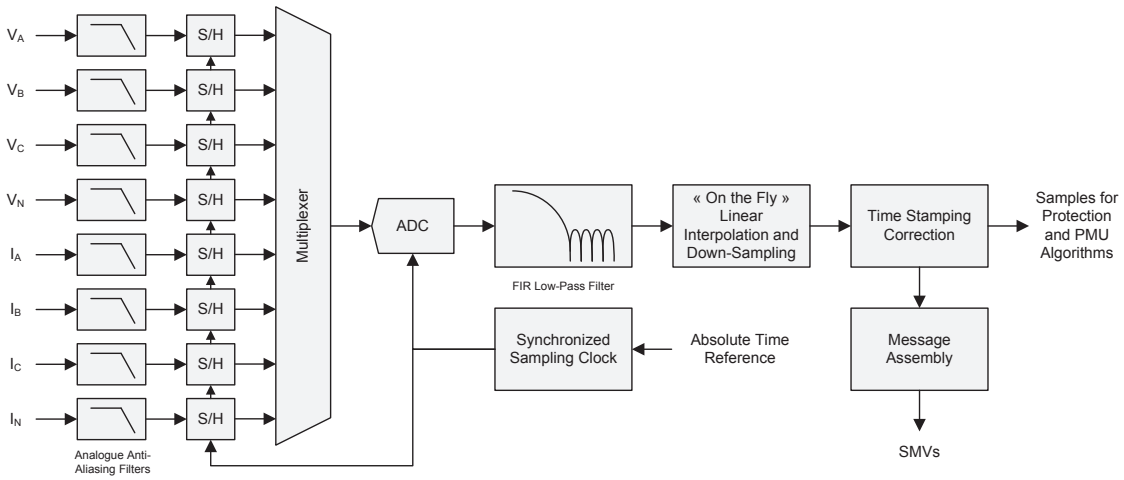

FIGURE II.17 – Simplified signal processing principle for SAMU

Since the SAMU inputs are supposed to be the three-phase voltages plus neutral and the three-phase currents plus neutral, it is obvious that several conversions should be performed at each sampling instant, synchronized to the absolute time reference. If the conversions are performed exactly at the same time on each of the eight channels, the samples are obtained simultaneously allowing them to be combined directly and enabling at the same time synchrophasor computations on different channels. In order to obtain simultaneous samples, the multiplexed structure presented in Section 3.5 of Chapter I is chosen because of its low-cost potential. Although the use of S/H circuits ensure simultaneous sampling for all input signals, care should be taken about the relationship between the total time necessary to acquire 1 sample on all 8 channels, store them into memory and process them and the sampling frequency.

Most of the components of the multiplexed structure introduce a delay in the data flow, in particular:

— The S/H circuit introduces a delay t_{ch} corresponding to the charging time of the hold capacitor,
— The ADC introduces a delay t_{ADC} corresponding to the time required to convert the analogue input into its digital representation (sample),
— The memory introduces a delay called the memory access time t_m which corresponds to the time required to store the sample in the data memory (buffer) before executing the algorithms.

In addition to these three delays, the processing time t_p needed to execute the algorithms involved to produce the SMV frames must be considered for real-time operations. The summation of all of these delays is the total time T_t and, according to the proposed multiplexed structure, is given by:

$$T_t = t_{ch} + 8 \times (t_{ADC} + t_m) + t_p \tag{II.4}$$

Equation (II.4) corresponds also to the minimum duration of time to wait between two complete processing cycles (for the eight channels) and is part of the maximum processing delay time. In other words, when the sample acquisition process starts for the first channel, it is necessary to wait at least T_t seconds before starting a new acquisition cycle. Therefore, the sampling period of the ADC must be higher than the total time in order to acquire the samples of all input channels in a sequential manner and deal with real-time operations constraint to create the SMV frames. In this thesis, it is assumed that this condition is fulfilled, that is the fixed sampling frequency of 28,800 Hz is suitable for the design of the SAMU metering class 0.1. Last but not least, despite the fact that the 8 samples are generated sequentially within the same cycle of conversion, their associated timestamps are identical thanks to the S/H circuits.

5.2 Analogue anti-aliasing filter design

Like any acquisition chain, each analogue input must have an analogue anti-aliasing filter prior to sample the signals to minimize aliasing effect. The analogue anti-aliasing filter may change the magnitude and phase angle of the input signal. Consequently, the

ADC samples a distorted signal before the timestamping process occurs (see Fig. II.17) which means that the samples obtained are not a perfect representation of the analogue input signals. In order to minimize the errors introduced during the sampling, the best filter would be the one which has a maximally flat magnitude response and a constant group delay (linear phase shift) in the passband. Unfortunately, as seen in Section 3.3 of Chapter I, the two aforementioned criteria are diametrically opposed and could not exactly be achieved at the same time. Indeed, a Butterworth design responds to the first request while a Bessel filter is ideal for obtaining a constant group delay. However, a Butterworth filter with a cut-off frequency set relatively high in relation to the nominal frequency yields a phase shift very linear around the fundamental and can be thus fruitful. Based on that, a 2^{nd} order Butterworth filter with a cut-off frequency of 3,000 Hz is proposed. With such a filter, an attenuation better than 40 dB is ensured for frequencies which are mapped on the rated frequency. The frequency response of this filter is given in Fig. II.18 for the frequency range [1 - 28,800] Hz.

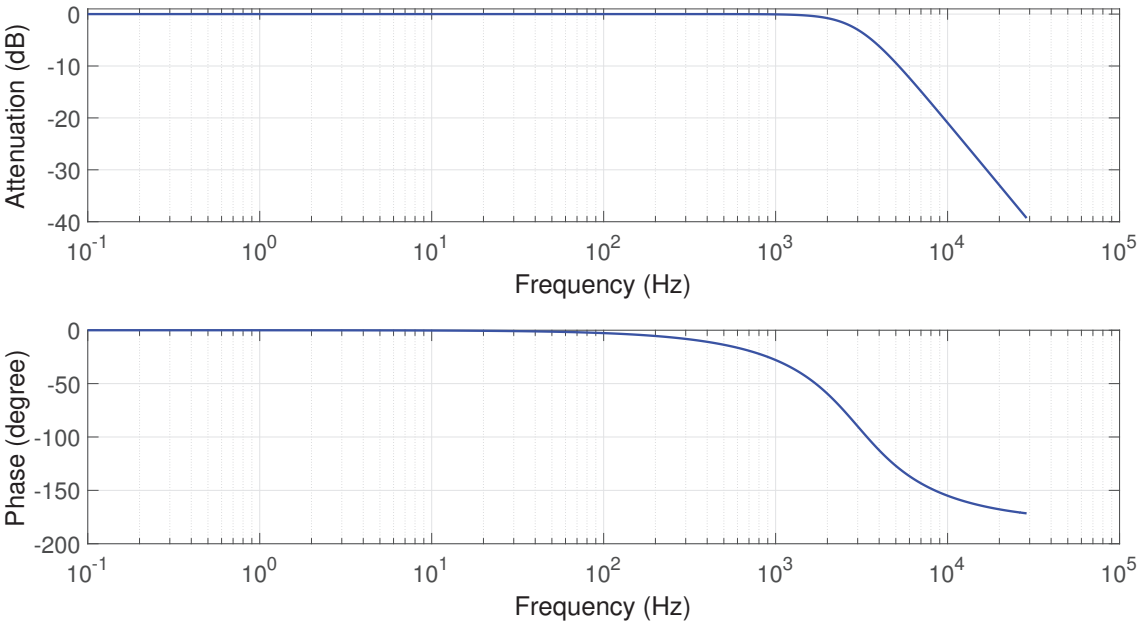

FIGURE II.18 – 2^{nd} order Butterworth filter

To clearly see the impact of this filter around the nominal, a “zoom" of Fig. II.18 from DC to 100 Hz is given in Fig. II.19.

As shown in Fig. II.19, no compensation is required for magnitude as there is no attenuation introduced by the filter. Anyway, compensation for phase shift is still necessary for two reasons. First, as at a rated frequency of 60 Hz, the phase shift is equal to -1.621 degrees, or -2.829 crad, the threshold of 0.15 crad for SAMU accuracy class 0.1 is exceeded for both voltage and current channels. Second, this same phase shift value will cause by itself 2.829% of error in the TVE computation. State-of-the-art PMUs having analogue input signals solve this issue by applying calibration factors on the synchrophasor estimates but this require the knowledge of the power system frequency as the phase shift

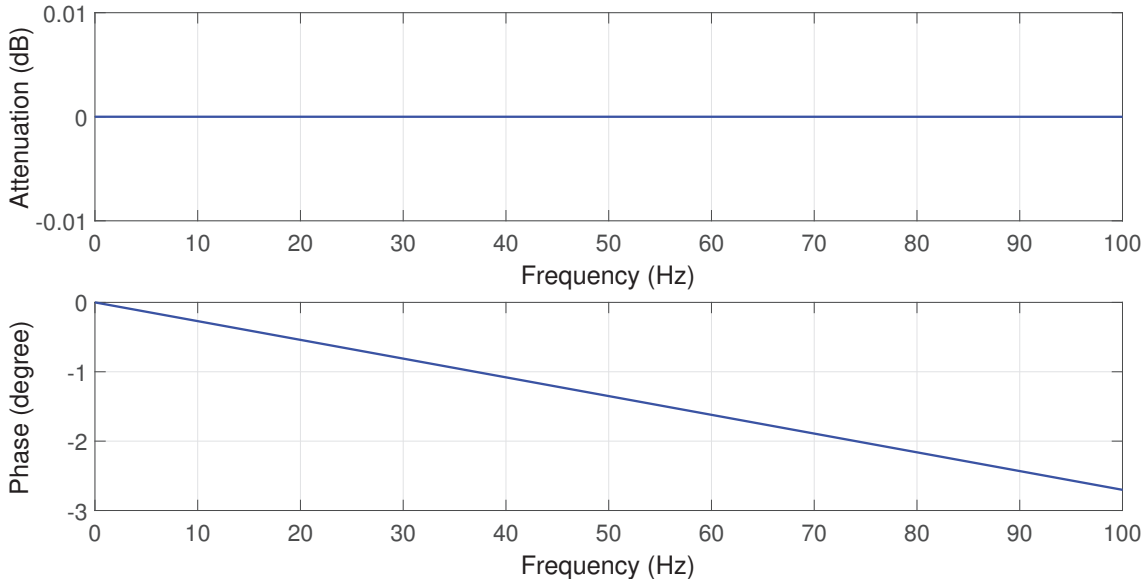

FIGURE II.19 – 2^{nd} order Butterworth filter - zoom on [0 - 100] Hz

is function of the frequency. In this configuration, PMUs take advantage of the frequency measurements to correct all phase shifts introduced by all analogue and digital filters once the synchrophasor have been computed. However, SAMUs shall publish SMV frames without having access to the power system frequency because SAMU are not intended to perform frequency measurements. Consequently, the compensation principle used by PMUs cannot be applied for SAMUs and an other principle shall be proposed to deal with linear phase response filters. Since the group delay $G_{d,Butter}$ is constant within the range [0 - 100] Hz and is equal to 75.054 μs (see the analytical expression Eq. (I.26) of Chapter I to obtain this value), this group delay can be compensated during the linear interpolation and down-sampling process as deeply discussed in Section 5.4.

5.3 Finite Impulse Response low-pass filter design

Besides, a FIR low-pass filter that meets anti-aliasing requirements imposed by the IEC Standard 61869-6 (Annex A) shall be used before the linear interpolation algorithm. Let us remind first from Section 3.4 of Chapter I that, in such an oversampling scheme, the signal bandwidth is equal to half the digital output rate, that is $F_s/2$ where F_s is the output sample rate (4,800 Hz). In this configuration, the very first alias frequency which is mapped on to the fundamental is $(F_s - f_0)$ where f_0 is the power system nominal frequency. For accuracy class 0.1, the minimum anti-aliasing filter attenuation is 34 dB for all of frequencies above $(F_s - f_0)$, including $(F_s - f_0)$. This constraint does not allow to reject all frequencies above the Nyquist frequency. Thus, if the input signal contains frequency ranging from $(F_s/2)$ to $(F_s - f_0)$, these frequencies will be mapped on the lowest frequency components, that is from f_0 to $F_s/2$. Since harmonic levels above 2,400 Hz are very small in power systems, IEC Standard 61869-6 has neglected their impact on the frequency range from $F_s/2$ to $(F_s - f_0)$. However, as it will be seen in Section 5, the PMU standard imposes a specific test where several high order harmonic components (from the 2^{nd} to the 50^{th} order) are superimposed to the fundamental. Thus, in this context, considering

a 50 Hz system, harmonic order 48 through 50 will be mapped on lower frequencies and this phenomenon could degrade the measurements performed on lower frequencies. In particular, the 49^{th} order harmonic alias is the fundamental frequency, parameter of interest for synchrophasors and most of protection functions. Therefore, the minimum attenuation defined as per IEC Standard 61869-6 is not suitable with respect to this thesis objectives. **Consequently, the request on the anti-aliasing filter has been changed into an attenuation better than 34 dB (minimal constraint of the standard) above the Nyquist frequency associated to the whole system (2,400 Hz).**

The impacts of the maximum processing delay time (t_{pd}) on the signal processing must be carefully understood prior to design digital filters. Remind that, along the acquisition chain, the main delays include the filtering process, the analogue-to-digital conversion process and the algorithmic part necessary to create SMV frames. The preferred publishing rate of 2,400 frames per second imposes that 1 SMV packet shall be created and published in less than approximately 0.417 ms as soon as the pairs of samples, with corrected timestamps, are made available at the FIR filter output. If this condition is not respected, then some SMV packets cannot be created and this is forbidden by the IEC Standard 61869-9. So, all of the delays introduced by the acquisition chain shall be lower than about 1.583 ms to fulfill the maximum processing delay time requirement. Thus, the order of the FIR filter, responsible for most of the delay time, should be low enough. For information purpose, a 92 order FIR filter, designed for a sampling frequency of 28,800 Hz, will cause by itself an equivalent group delay of about 1.597 ms.

The Parks-McClellan optimization method [MP05] is used to design the FIR filter because it brings several benefits. First, this method makes possible the design of optimal linear phase filters having symmetrical coefficients. Consequently, a constant group delay is obtained in the passband which means that all frequency components of the input signal are shifted by the same amount. Second, the error between the desired frequency response and the achieved frequency response is minimized. Finally, the filter length is minimized for a given set of constraints. For the Parks-McClellan algorithm, these constraints are related to the band edges defined in Section 3.3 of Chapter I. For a low-pass filter design, the specification is depicted in Fig. II.20 and is mathematically expressed as:

$$-G_{pass}/2 \leq H(f) \leq G_{pass}/2 \qquad \text{in the passband } 0 < f \leq F_{pass} \tag{II.5}$$

$$H(f) \leq G_{stop} \qquad \text{in the stopband } F_{stop} < f \leq F_s/2 \tag{II.6}$$

This digital anti-aliasing filter is designed for the fundamental frequency (50/60 Hz) and meets the following characteristics:

Stopband edge frequency: As stated earlier, the stopband edge frequency F_{stop} is set to 2,400 Hz.

Stopband gain: For the reasons already given above, a 34 dB attenuation in the stopband is chosen.

Passband edge frequency: Based on marketing requirements, accurate measurements of the 15^{th} harmonic are expected. The fundamental frequency of 60 Hz must be considered to fix F_{pass} since it encompasses the passband of the 50 Hz system.

Therefore, F_{pass} would be equal to 900 Hz.

Passband gain: The passband gain is imposed by the requirement on the ±0.1% ratio error, equivalent to ±0.00868 dB.

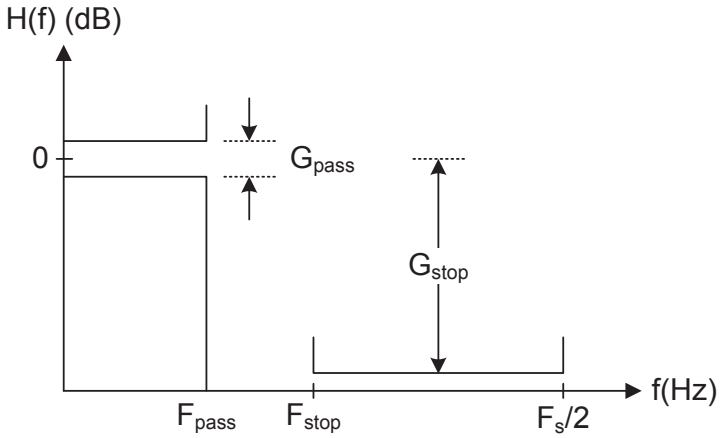

FIGURE II.20 – FIR low-pass filter specification for the Parks-McClellan algorithm

Based on the aforementioned specification, a 50 order filter has been obtained through the Parks-McClellan algorithm. This filter introduces a delay $G_{d,FIR}$ of 50 samples which is equivalent to approximately 0.868 ms for a sampling frequency of 28,800 Hz. The frequency response, plotted in Fig. II.21, shows that the cut-off frequency is about 1,638 Hz.

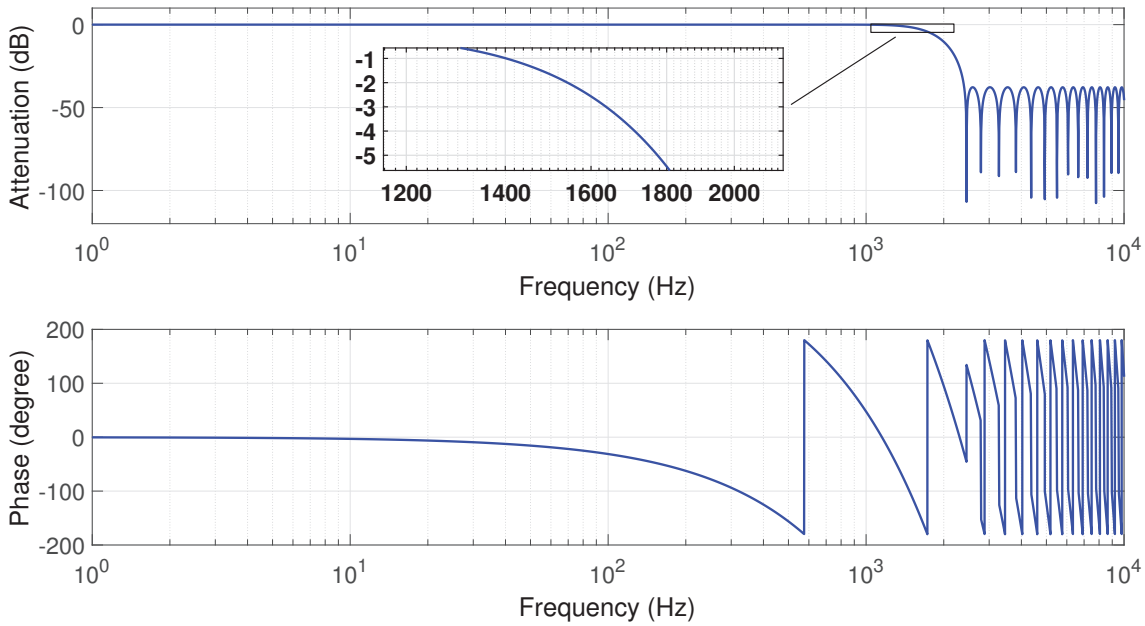

FIGURE II.21 – 50^{th} order FIR filter frequency response

Regarding the attenuation of this filter, the zoom provided in Fig. II.22 on [DC - 100] Hz shows that the gain is very closed to 0 dB around the nominal frequency. The filter is tuned to have a gain exactly equal to 0 dB at 60 Hz while a negligible attenuation of -0.000 019 07 dB exists at 50 Hz. A magnitude compensation factor should be thus applied

in software to compensate the gain introduced at 50 Hz. Moreover, the phase shifts of -15.62 degrees (≈ -27.27 crad) and -18.75 degrees (≈ -32.72 crad) for 50 Hz and 60 Hz respectively introduced by the filter are intolerable for the phase error requirement (± 0.15 crad) and must be compensated. The logic of the compensation method is different to the one proposed to compensate the phase shift introduced by the analogue Butterworth filter. The digital nature of the FIR filter permits to discuss the group delay in terms of samples. As the amount of samples shifted remains the same in the passband and is equal to 25, the compensation can be performed during the timestamping compensation process simply by subtracting $25/28800 \approx 868.05$ μs to the initial absolute timestamps.

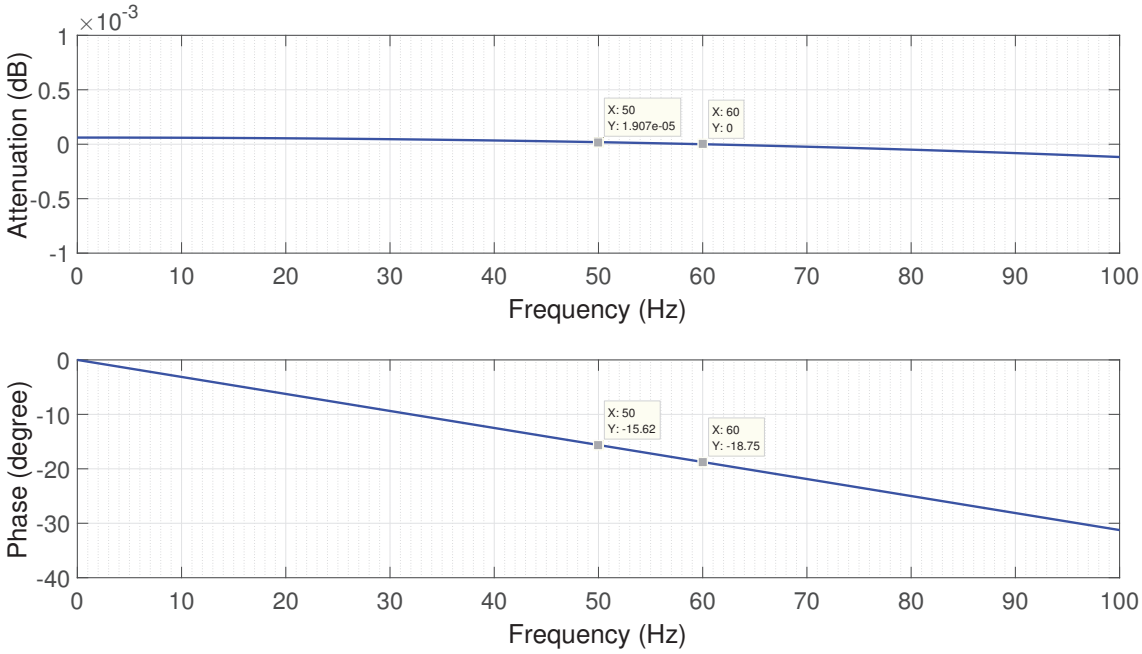

FIGURE II.22 – 50^{th} order FIR filter frequency response - zoom on [0 - 100] Hz

5.4 "On the fly" linear interpolation and down-sampling algorithm

The next step of the design consists in writing the "on the fly" linear interpolation and down-sampling algorithm (chronological direction). This algorithm is aimed at computing the 4,800 Hz sample stream on the basis of the 28,800 Hz sample set generated by the ADC. With such a high sampling frequency, it can be assumed that the portion of signal between two consecutive samples is a straight line. Thus, the linear interpolation could be used in this case. Furthermore, the relationship between the processing time t_p and the sampling frequency (see Eq. (II.4)) justifies the use of simple algorithms in order to achieve their implementation in a microprocessor and enable real-time operations.

To understand the operation principle of the algorithm, let us first remind that the analogue front ends of the SAMU channels introduce a specific phase shift which must be compensated during the timestamping compensation process because the phase error must be below ± 0.15 crad. Figure II.23 illustrates the impact of the analogue front end on the input signal for a given channel where the blue bullets represent the samples obtained

by sampling the input signal at a frequency of 28,800 Hz, synchronized to the GPS time marks, bypassing the Butterworth filter. As shown in Fig. II.23, two issues must be solved. First, due to the Butterworth filter group delay, the magnitude of the samples obtained during the sampling process (green bullets) is not the one expected (blue bullets). Second, if a straightforward timestamp compensation is performed based on the filter group delay, the superimposition of the perfect sample set and the compensated one shows that the compensated samples are no more referenced to the absolute time reference. Otherwise, the reference samples and those generated would be overlapped. Instead, a kind of periodic jitter appears and such a jitter shall be corrected by the interpolation algorithm to maximize measurement accuracy.

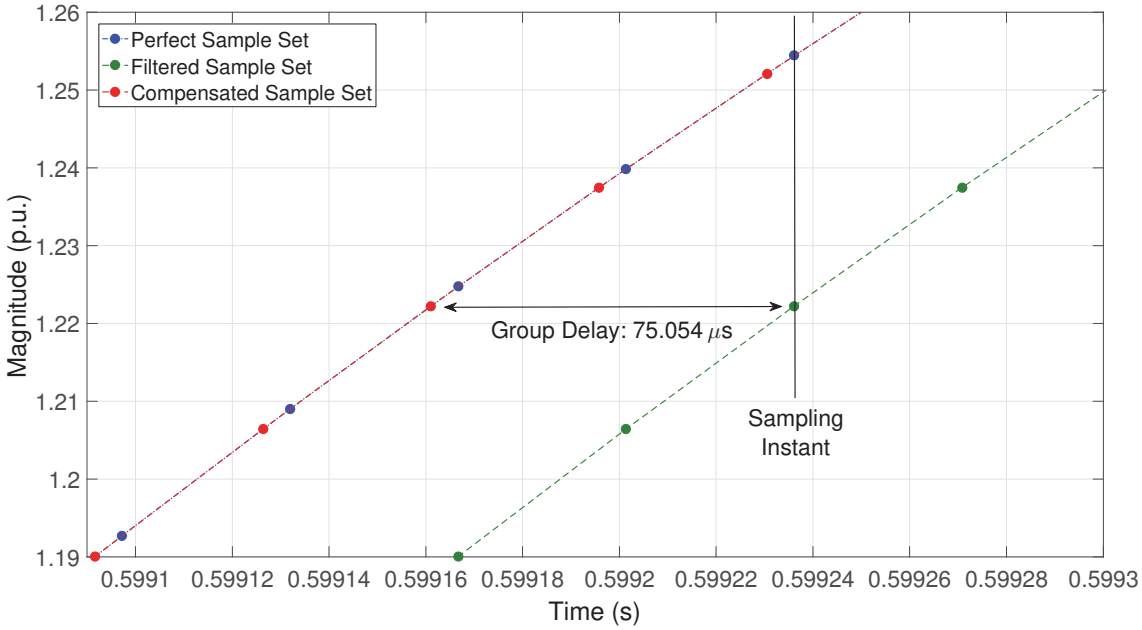

FIGURE II.23 – Front end impacts on analogue signal

Worse, since a 50 order FIR filter is involved in the data flow prior to the linear interpolation algorithm, the green sample stream in Fig. II.23 will be delayed by 25 sample times (about 868.05 μs). The principle of the algorithm is thus to interpolate the filtered samples in such a way that the computed sample stream has exactly the same magnitude as the perfect one (blue signal in Fig. II.23) but drifted by a time equal to the total filter group delay (analogue and digital). Since the interpolated sample stream is generated at 28,800 Hz, it is necessary to discard some samples so that to keep those associated to the timestamps of the SMV frames in order to obtain a 4,800 Hz signal. This process is performed by the down-sampling operation by taking 1 sample out of 6. Based on that, by superimposing the computed 4,800 Hz signal over the expected one which is synchronized to the absolute time reference, it can be seen that the periodic jitter is eliminated (see Fig. II.24).

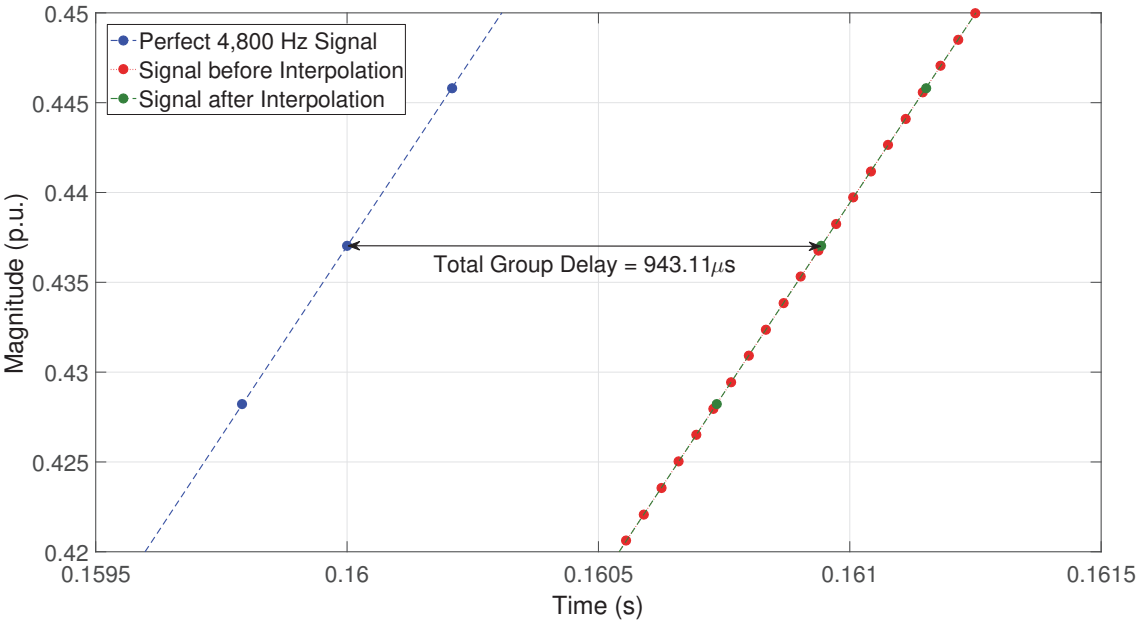

FIGURE II.24 – Linear interpolation principle applied on the 28,800 Hz filtered signal

5.5 Timestamping correction process

Finally, the design ends with the timestamping correction process. As the generated samples shall refer to the analogue input signals, their corresponding timestamps shall be coincident with both the exact time at which the analogue signals are made available at the SAMU input channels and the absolute time reference. In a nutshell, if plotted on a same time axis, the analogue signal and the samples synchronized to the UTC time scale must be aligned. As discussed in the previous subsection, the first timestamp values associated to the samples are wrong due to the use of filters and must be thus corrected. The correction of the timestamps is straightforward thanks to the benefits of the linear interpolation algorithm and is done as it follows:

$$timeStamp(n) = t_{low}(n) - G_{d,Butter} - G_{d,FIR} \tag{II.7}$$

where:

$timeStamp(n)$	is the corrected timestamp of sample indexed n
$t_{low}(n)$	is the initial wrong time stamp of sample indexed n

5.6 Validation of the proposed SAMU accuracy class 0.1

Based on the requirements defined in Table II.7, the validation of the proposed SAMU metering accuracy class 0.1 can be split into 3 parts:

Measurement Accuracy: The ratio error and the phase error have to be measured and compared with their corresponding thresholds on the entire frequency range of interest. To do so, a sine-wave of a single frequency ranging from 5 Hz to 72 Hz with steps of 0.1 Hz is generated and passed through the 8^{th} channel of the SAMU. This specific

range of frequency is determined based on a marketing requirement and denotes the operating range of the relay in the network covering generator applications. For each frequency, the computed sample set is recorded and a Sliding DFT of 1 cycle length is used to extract the phase angle and the magnitude of the 4,800 Hz signal available at the SAMU output. A reference signal of 4,800 Hz is also generated and successive DFTs are also applied on this signal. Then, the DFT estimates are compared to compute the ratio error and the phase error at each sample. The duration of the test is variable and related to the frequency of the sine-wave.

Frequency response: The frequency response of the SAMU shall be computed, plotted, and compared to the frequency response masks given in Figs. II.15 and II.16 to check if both amplitude and phase responses are within the standardized limits.

Maximum processing delay time: This constraint should be normally measured following an actual design of the SAMU. However, preliminary assessments can be given to verify if the proposed method can be implemented in practice.

Regarding the measurement accuracy, the mathematical definitions of the ratio error and the phase error should be first given. In accordance with IEC Standard 61869-6, the ratio error in percentage, for digital output, is expressed by the formula:

$$\epsilon(\%) = \frac{k_r Y_s - X_p}{X_p} \times 100 \tag{II.8}$$

where:

k_r	is the rated interposed transformer ratio (equal to 1 here as not considered)
X_p	is the RMS value of the primary analogue signal, computed by DFT
Y_s	is the RMS value of the digital output, computed by DFT

Similarly, IEC Standard 61869-6 defines the phase error as:

$$\Delta\varphi = \varphi_s - \varphi_p \tag{II.9}$$

where:

φ_s	is the secondary phase (digital output), computed by DFT
φ_p	is the primary phase (analogue input), computed by DFT

Based on Eqs. (II.8) and (II.9) and following the DFT-based measurement process described above, the measurement accuracy can be estimated in terms of ratio error and phase error. Without loss of generality, the magnitude of the input signal is chosen to be 1 p.u. while its initial phase angle is chosen to be 30 degrees. The results are shown in Figs. II.25 and II.26 where the maximum, the average, and the minimum errors are plotted for the frequency range of interest. Clearly, both the ratio error and the phase error are closed to 0% and 0 crad respectively for the whole frequency range. This highlights the fact that the proposed method can accurately estimate the magnitude and the phase angle of the analogue input signal while correcting the timestamp of each sample at the same time.

The second step of the validation concerns the frequency response of the SAMU. From the SAMU perspective, the frequency response involves the gain introduced by the overall

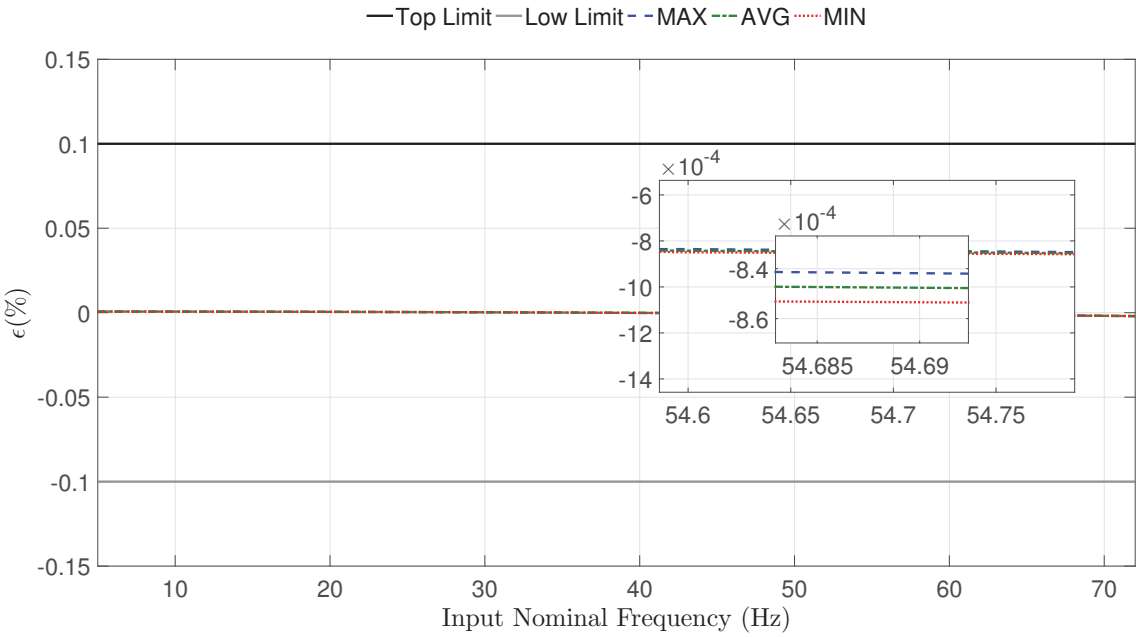

FIGURE II.25 – Ratio error for various frequencies

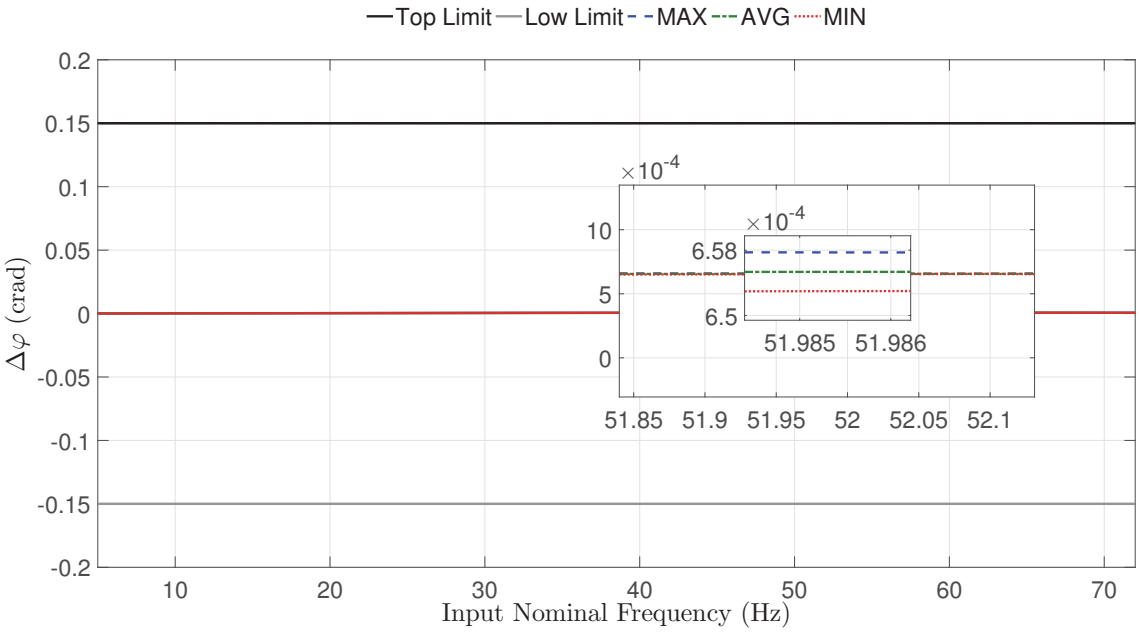

FIGURE II.26 – Phase error for various frequencies

filtering process and the phase error $\Delta\varphi$ (not the so-called phase response of the filters) in accordance with the IEC Standard 61869-6. The frequency response of the proposed SAMU metering class 0.1 is depicted in Figs. II.27 and II.28 for a 60 Hz system. In contrast to Figs. II.25 and II.26 focusing on the accuracy for the operating range of the device ([5 - 72] Hz), Figs. II.27 and II.28 are aimed at providing the accuracy for harmonics and low frequencies. Last but not least, the phase error is plotted on a linear scale for sake of clarity, since the errors allowed above the 13^{th} harmonic and below 1 Hz are not specified in the standard.

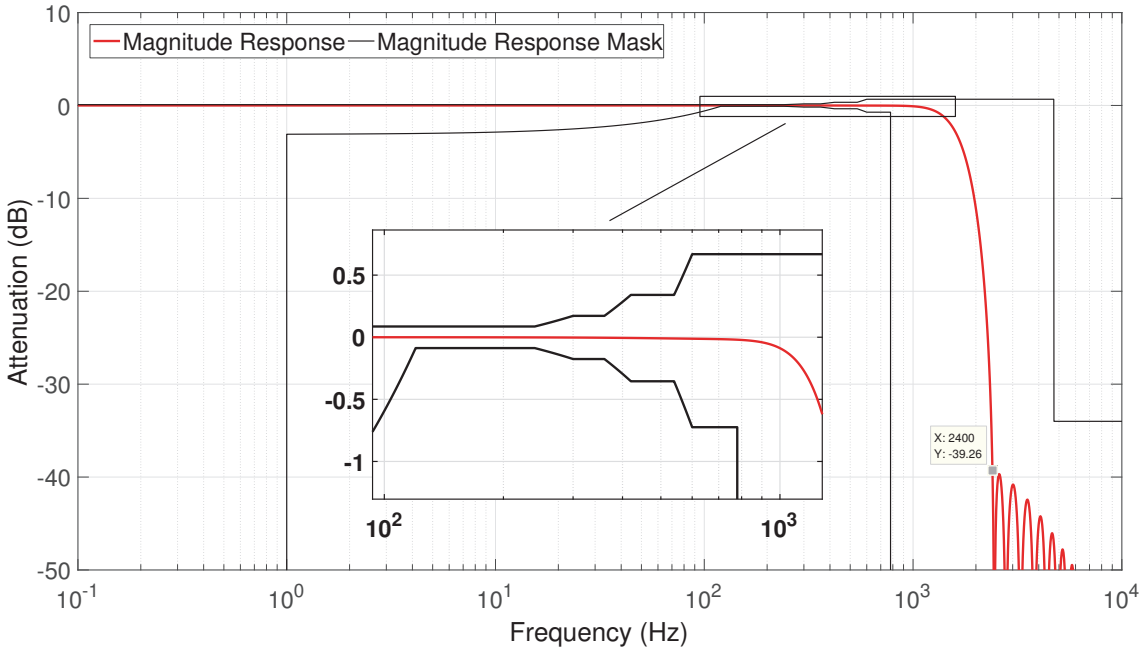

FIGURE II.27 – SAMU metering class 0.1 magnitude response

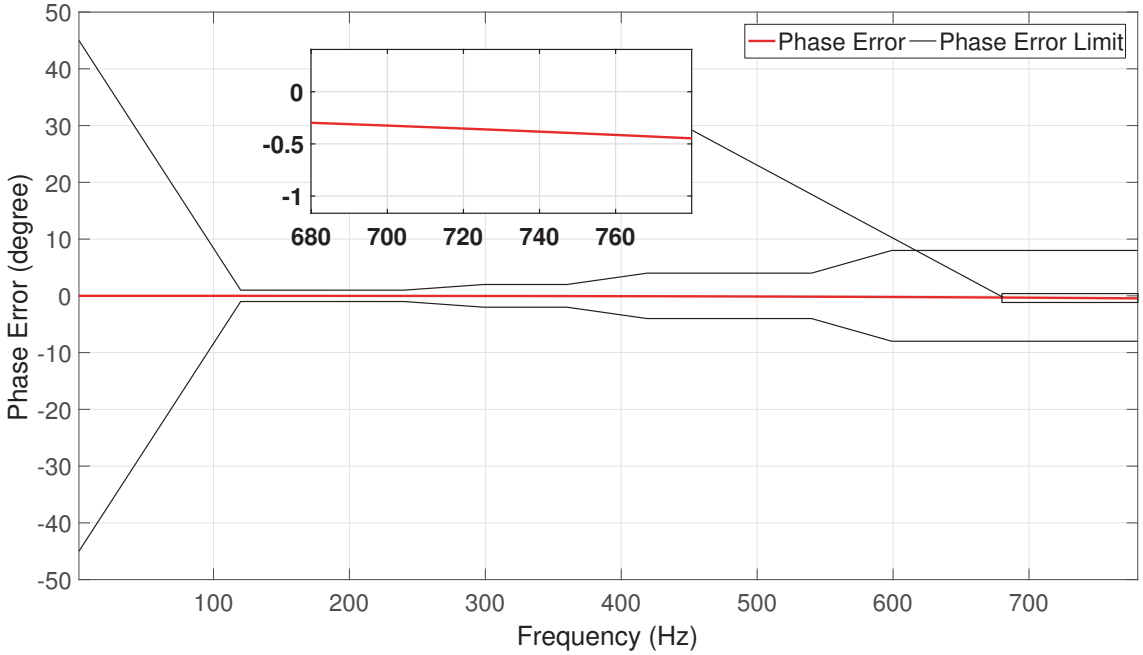

FIGURE II.28 – SAMU metering class 0.1 phase error

Several conclusions can be drawn from Figs. II.27 and II.28. First of all, the magnitude frequency response and the phase error of the SAMU are within the standardized limits listed in Table II.7. Moreover, it can be seen from Fig. II.27 that the minimum attenuation of 34 dB is ensured for frequencies above 2400 Hz. Furthermore, Fig. II.28 shows that absolute phase errors of less than 0.5 degrees are introduced in the harmonics within the

passband. Based on this analysis, the results indicate that the proposed SAMU metering class 0.1 is compliant with the IEC Standard 61869-6. These conclusions apply equally to a 50 Hz system.

The last step of the validation process relies on the estimation of the maximum processing delay time which has to be below 2 ms. To do so, the delays to consider are $G_{d,Butter} \approx 0.075$ ms, $G_{d,FIR} \approx 0.868$ ms and the creation of 1 SMV frame which has to be performed in less than 0.417 ms as stated in Section 5.3. The result is about 1.36 ms, that is roughly 0.64 ms less than the imposed limit.

The validation of the proposed SAMU metering class 0.1 permit to conclude that it has shown compliance with the product family standard for the signal processing part. Furthermore, the study has shown that the ratio error and the phase error would be affected only in a very limited way by the signal processing algorithms involved in the data flow. From the author's perspective, most of the ratio and phase errors introduce in the input signals are due to the accuracy of the components involved in the DAQ (hardware part). In particular, the tolerance range of the components, the quality of the magnetic core of the interposed current and voltage transformers, and the temperature effects could be some potential avenues to be explored.

6 Conclusion

The current chapter has addressed the main challenges of protection relays and phasor measurement units in correlation with the IEC Standard 61850. After introducing the needs for a new international standard in the SAS, it has been shown that its benefits, such as interoperability and reduction of wiring, have huge impacts in technical committees:

— TC57 has proposed a communication method to ease implementation of Process Bus in substations,
— TC38 has integrated Process Bus communications into IEC Standard 61869 while extending the concept of SMVs,
— TC95 has introduced the concept of PMUs having SMVs as inputs and defined the synchrophasor measurement requirements.

Furthermore, the IEC 61869 product family standard characterizes new exigencies for MUs and SAMUs. To respond to the first objective of this dissertation related to the investigation of the Merging Unit behavior, the requirements related to the signal processing field have been described and their impact on IEDs identified and characterized.

MUs/SAMUs must provide to numerical relays accurate information on primary signals [3]. The level of accuracy is expressed through the accuracy classes. SAMUs are allowed to introduce limited random combined errors in their output and such errors cannot be compensate due to their hazardous nature. Therefore, SAMUs, like conventional instrument transformers, must be selected to cope with the measurement accuracy required for a specific application. In particular, it has been shown that SAMU classes are not

3. analogue signals at the inputs of MU channels

all suitable for estimation of synchrophasors. Preferences are given for metering accuracy classes 0.1, 0.2 and 0.5 for voltage and current input channels. Nevertheless, to maximize the allowed margin of errors introduced by the PMU itself on the TVE, the metering class 0.1 should be used for synchrophasor measurements.

On the basis of this selection, a proposed SAMU metering class 0.1 has been proposed. This SAMU is integrated into the protection relay as a dedicated board so that to consider the transition period during which digital and conventional substations will cohabit. The proposed SAMU algorithm is able to compute samples with magnitude and phase error very near 0% which permits the hardware part of the DAQ to be designed with the maximum error range allowed. This meets the second objective of this thesis.

Another issue emerging from the use of SAMUs is the impossibility for using power system frequency tracking with drivable ADC as shown in Fig. I.21 of Chapter I since Process Bus and SAMUs are designed to output a constant sampling rate. So any adaptive sampling scheme must be implemented digitally in the relay software as it is the case in Fig. I.22 of Chapter I. Another option consists in designing new signal processing techniques based the fixed sample scheme as shown in Fig. I.23 of Chapter I. However, improved signal processing algorithms are expected here because the frequency error compensation relies on an accurate modeling of phasor estimation errors and such a model is impossible to build in practice. Indeed, too much different phenomenon occur in the power system and each of them needs to be considered by the phasor error model to ensure an accurate compensation. On the other hand, synchrophasor-based algorithms are commonly designed on the basis of a stream of samples generated uniformly. From this, it seems that more options are available for PMU algorithms than for algorithms dedicated to protection relays. Nevertheless, for both applications, the signal processing must deal with the high sample rate imposes by IEC Standard 61869-9 (4,800 Hz).

Consequently, in Chapter III, three new algorithms for computing phasors are proposed, analytically formulated, simulated, tested and compared.

Chapter III

Propositions of innovative algorithms for accurate phasor estimations in protection relays

Contents

Abstract

In this chapter, three solutions are provided to estimate phasors with high level of accuracy during static and dynamic conditions. The focus is on phasors dedicated to protection algorithms only. Synchrophasors are disregarded in this chapter. The proposed algorithms involves the discrete Fourier transform to compute the magnitude and phase angle on the basis of Sampled Measured Values. To avoid the pernicious leakage phenomenon occurring during asynchronous sampling conditions, three methods are proposed to efficiently track the prevailed power system frequency. Two of the three methods are based on distinct resampling schemes while the third one interpolates the discrete Fourier transform bins in the frequency domain. Since the frequency is tracked in a effective way, the ROCOF can be estimated accurately in real-time which is a real benefit especially with the wide penetration of distributed generations in the distribution system. Indeed, accurate ROCOF estimates improve considerably the performance of ROCOF relays widely employed as anti-islanding protection method. Today, such relays suffer from unwanted tripping and this is unacceptable. Simulation results are provided at the end of this chapter to illustrate the performance of the proposed solutions.

1 Introduction

As highlighted in Chapter I, it exists a fundamental distinction between phasors and synchrophasors: they are computed based on 2 different data windows. Indeed, the phasors are computed by taking the N most recent samples stored in the memory commonly generated through an adaptive sampling rate. However, the synchrophasors are estimated by taking the $N/2$ most recent samples stored in the memory commonly obtained through a uniform sample rate and the next $N/2 - 1$ samples that will be generated uniformly following the synchrophasor time-tag. That is why protection relays integrating the PMU function typically involve two streams of samples. One is generated synchronously with the power system frequency and is used to estimate phasors. The other is obtained by a fixed sample rate synchronized to the absolute time reference and is dedicated for synchrophasor measurements. In this chapter, signal processing techniques are proposed with a view to computing phasors with high accuracy on the basis of samples generated by the SAMU metering accuracy class 0.1 design in Chapter II. Nevertheless, even not studied in what is follows, it should be noticed that the methods can be also applicable to Sampled Measured Values coming from the Process Bus. The proposed techniques involve the DFT algorithm only as method for computing the phasors.

In the light of the aforementioned points, two main families of algorithms have been proposed for the design of next generation protection relays. These algorithms apply equally to each of the input channel considered in the SAMU metering class 0.1 of Chapter II.

The first family is the resampling techniques which have been introduced in Section 7.5 of Chapter I. From the IED perspective, resampling techniques bring the advantage of reducing the sampling rate, and therefore the computational burden required by the phasor estimator. In addition, they allow the implementation of a digital frequency tracking algorithm which counters the leakage phenomenon.

The second family is the interpolated discrete Fourier transform (IpDFT) methods also presented in Section 7.5 of Chapter I. In this approach, the samples are taken as they are, filtered, processed by the DFT algorithm and finally interpolated in the frequency domain. This interpolation tackles the inaccuracies introduced by the leakage phenomenon. The IpDFT algorithm is therefore an interesting alternative to the classical resampling algorithm since it is designed to deal with uniformly generated samples without requiring any frequency tracking implementation.

The rest of this chapter is organized as follows. Section 2 describes two resampling algorithms which are based on two distinct concepts. The first resampling scheme is built around the simple linear interpolation which changes both the magnitude and the sample time of the generated samples whereas the second one alters only the amplitude of the samples. The second method is called improved-Sampled Value Adjustment (i-SVA). As resampling schemes require the knowledge of the power system frequency, a new method for accurately tracking the frequency is proposed in Section 3 and employed as function of the resampling method used. Moreover, Section 4 develops a phasor estimator on the basis

of IpDFT methods. Finally, the performances of the proposed algorithms are analyzed and compared in Section 5.

2 Development of resampling technique schemes

Resampling algorithms convert a stream of samples obtained at frequency f_1 to a stream of samples generated at the desired frequency f_2. Considering f_1 higher than f_2, the resampling decreases the sample rate which results in reducing the processing power required by the algorithms. The first step of the resampling consists in adding samples between existing samples of a data stream with frequency f_1 using an interpolation algorithm. This results in a data stream with a frequency $(L \times f_1)$ Hz, that is the input signal is oversampled by a factor L called interpolation coefficient. Then, as seen in Section 3.4 of Chapter I, an anti-aliasing filter needs to be applied prior the downsampling process. This downsampling to the desired frequency f_2 is performed by taking 1 sample every M^{th} sample, where M is called the downsampling coeffient.

The choice of the frequency f_2 depends on the relay operating time criterion. A numerical relay can sense faulty conditions after waiting until the next time that the samples are processed by its algorithm. From Fig. I.21 of Chapter I, the algorithm is executed $P \times f_{track}$ which means that for a sample rate of 12 s/c and $P = 2$, the algorithm is run each 2 sample times ; thus each 3 new samples. Assuming that a fault occurs just after the relay has completed a protection scan, the relay will begin to respond to the fault (not necessarily issuing a trip signal) the next protection scan. Therefore, in this condition, the operating time is delayed by approximately 3.33 ms for a 50 Hz system. Now, for a relay that samples 48 times per 50 Hz cycle and $P = 2$, the operating time is delayed by about 0.83 ms, that is 4 times lower than the previous example. As a rule of thumb, higher sampling rates mean lower operating times but the gain obtained is weighted by the full-cycle DFT which requires 1 cycle of samples to correctly compute the phasor. Moreover, doubling the sample rate results in doubling the number of computation performed by digital filtering. Therefore, the choice of the sample rate is often a matter of tradeoff between speed, digital filtering involved and computational effort. Most of the time, high-speed protection relays commercialized by the Schneider Electric company perform a 48-points DFT to estimate the phasors ; that is a sample rate of 48 s/c. Since this sample rate has given satisfactory to both relay designers and customers, it is used in this study as well.

A sample rate of 48 s/c means that 48 samples must be generated in exactly 1 power system cycle whatever the frequency is. In other words, the goal of the resampling strategies developed in this study is to modify the stream of samples such that a new stream synchronized with the power system frequency can be obtained while decreasing the sampling frequency. In this light, two resampling algorithms are proposed: the backward linear interpolation and the i-SVA. For both methods, the design of the digital anti-aliasing filter is necessary and the power system frequency must be determined by a frequency estimation algorithm.

2.1 Digital anti-aliasing filter for the decimation process

As stated in Section 3.4 of Chapter I, the digital filter is required during the decimation process to remove frequencies from $f_2/2$ to $f_1/2$ and avoid aliasing. The Parks-McClellan optimization method [MP05] has been chosen here also to design a linear phase filter (with symmetrical coefficients). This digital anti-aliasing filter is designed for the fundamental frequency (50/60 Hz) and meets the following characteristics:

Passband edge frequency: Following the same reasoning described in Section 5.3 of Chapter II, F_{pass} should be equal to 900 Hz.

Stopband edge frequency: The stopband edge frequency shall be selected based on the fundamental frequency of 50 Hz since it encompasses the stopband of the 60 Hz system. For such a fundamental, 48 s/c is equivalent to 2,400 Hz and the Nyquist frequency is 1,200 Hz. As a consequence, F_{stop} is set to 1,200 Hz.

Passband gain: Based on F_{pass} and F_{stop}, the transition band is equal to 300 Hz. In this configuration, a high order filter could be obtained if G_{pass} is small. However, high order filters introduce long delays which make the time response of numerical protection relays slower. This is why the constraint on the passband gain should be light. It has been set to 1 dB.

Stopband gain: The analysis given for the passband gain is also applicable for the desired attenuation in the stopband: the higher the attenuation, the higher the filter order and the slower the relay time response. As a result, a 20 dB attenuation in the stopband has been chosen.

Based on the above-mentioned specification, a 8^{th} order filter has been designed through the Parks-McClellan algorithm. Such a filter introduces a group delay of $N/2 = 4$ samples, which, for a sampling frequency of 4,800 Hz, is equivalent to about 0.83 ms. This delay is suitable for protection relays since it is negligible compared to the traditional DFT-based filter which requires 20 ms to estimate the phasor. Moreover, the frequency response is depicted in Fig. III.1 while a zoom on the frequency range [5 - 72] Hz is given in Fig. III.2. Finally, Fig. III.1 shows that the optimization algorithm has computed a filter whose attenuation is better than 25 dB for frequencies above the Nyquist frequency, fulfilling the desired stopband requirement. As shown in Fig. III.2, the gain of the filter varies as function

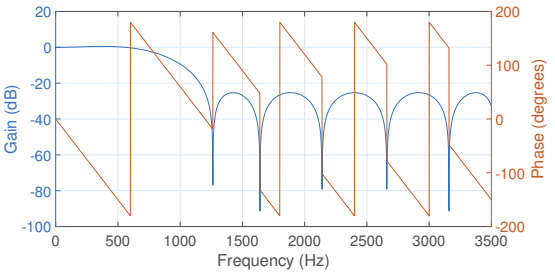

FIGURE III.1 – 8^{th} order FIR filter magnitude response

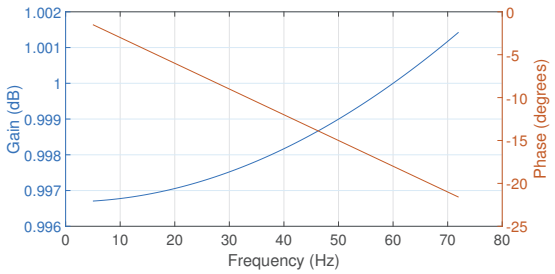

FIGURE III.2 – 8^{th} order FIR filter magnitude response - zoom on [5 - 72] Hz

of the actual frequency of the power system. Hence, a magnitude compensation factor dependent on the estimated frequency must be applied so that the phasors of fundamental frequency are insensitive to the filter gain on the whole frequency range of interest. To

correct the magnitude, a cubic spline approximation has been performed on the range [5 - 72] Hz. This leads to the formula:

$$MCF(n) = \big(-6.0452 \times 10^{-10} \times F_{clean}^{3}(n) + 9.6675 \times 10^{-7} \times F_{clean}^{2}(n) - 6.0118 \times 10^{-7} \times F_{clean}(n) + 0.99669\big)^{-1} \quad \text{(III.1)}$$

where:

$MCF(n)$	is the magnitude correction factor indexed n
$F_{clean}(n)$	is the clean frequency estimated indexed n

The same magnitude correction process can be performed for phasors of harmonics.

2.2 Resampling the magnitude of the samples: improved Sampled Values Adjustment

For the development of the i-SVA method, a fundamental system frequency of 50 Hz is considered without loss of generality. The idea of the resampling based on amplitude correction is to alter the magnitude of the samples. The re-computed samples will have the same magnitude as if the signal was sampled based on sampling frequency that is matched to the off-nominal frequency. This technique acts as the sampling period has been changed so that the sampling frequency matches the power system frequency. However, it is important to notice that the sample rate does not change properly speaking ; the timestamps of the samples remain unchanged after being virtually resampled. Thus, this method shall be coupled with a resampling scheme to reduce the sample rate to 48 s/c so that the algorithm can be applied on the decimated signal and a 48-points DFT can be performed as expected. The 2,400 Hz signal can be obtained through the use of the decimator function. This decimator consists of the digital anti-aliasing filter designed in Section 2.1 and the downsampling operation which decreases the sampling rate by a factor of 2.

As shown for instance in Fig. III.3, the goal is to alter the magnitude of asynchronous samples generated from sampling the signal $x(t) = \cos(2\pi 55t + \pi/4)$ at asynchronous sampling frequency 2,400 Hz ($N \times f_0 = 48 \times 50$) to be as the magnitude of the synchronous samples generated from sampling the same signal at synchronous sampling frequency 2,640 Hz ($N \times f = 48 \times 55$). The basic idea of the algorithm is to convert the asynchronous samples set $x[n]^* = A\cos(\frac{2\pi n}{Nf_0}f + \varphi^*)$, being φ^* the phase angle of $x[n]^*$, to the synchronous samples set $x[n] = A\cos(\frac{2\pi n}{N} + \varphi)$, where φ is the phase angle of $x[n]$, by altering the magnitude of the samples solely. To do so, an equation has to be derived that expresses $x[n]$ as function of $x[n]^*$. Assuming that the time drift between the asynchronous sampling period ΔT_0 and the synchronous sampling period ΔT_s is given by Eq. (III.2):

$$\Delta T_0 - \Delta T_s = \frac{1}{F_{s0}} - \frac{1}{F_s} = e \quad \text{(III.2)}$$

where:

F_{s0}	is the asynchronous sampling frequency, $F_{s0} = N \times f_0$
F_s	is the synchronous sampling frequency, $F_s = N \times f$

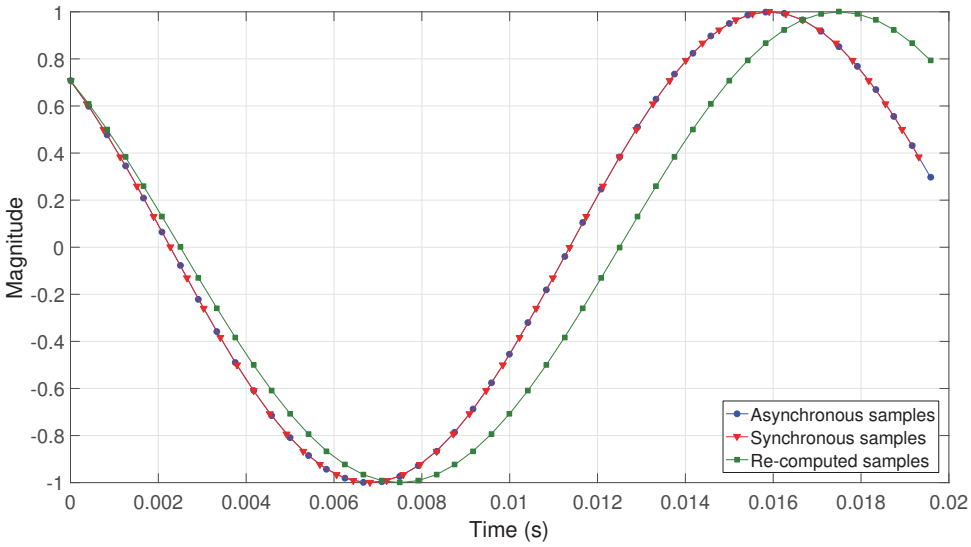

FIGURE III.3 – Basic idea of the resampling algorithm

To modify the magnitude of the asynchronous sample set, $x[n]$ and $x[n]^*$ has to be rewritten using the sampling periods ΔT_s and ΔT_0 as shown:

$$x[n] = x[n\Delta T_s] = A\cos(2\pi n\Delta T_s + \varphi) \tag{III.3}$$

$$x[n]^* = x[n\Delta T_0] = A\cos(2\pi n\Delta T_0 + \varphi^*) \tag{III.4}$$

Based on Eq. (III.2), $x[n\Delta T_s]$ can be expressed as

$$x[n] = x[n\Delta T_s] = x[n\Delta T_0 - ne] \tag{III.5}$$

Reference [XC96] uses the first order Taylor Series around the point $n\Delta T_0$ to find an equation that gives $x[n]$ as function of $x[n]^*$. Reference [AT10] has modified the concept by extending the Taylor series till the second derivative. This technique has been called Sampled Value Adjustment (SVA). Applying a DFT-based algorithm on the recomputed samples, a maximum magnitude error of less than 0.1% for frequency deviations up to 10% from nominal can be obtained, even if the second order harmonic is superimposed to the fundamental frequency. However, in case of higher order harmonics, the magnitude error will be near 1% during steady-state conditions. This study proposed an improved version of the SVA method, called i-SVA. It uses the third order Taylor series that is to increase the accuracy of phasor estimations over wider range of off-nominal frequencies. The i-SVA method is formulated below.

Using Taylor Series till the third derivative around the point $n\Delta T_0$, Eq. (III.5) can be written as

$$x[n\Delta T_0 - ne] = x[n\Delta T_0] - (ne)x'[n\Delta T_0] + \frac{1}{2}(ne)^2 x''[n\Delta T_0] - \frac{1}{6}(ne)^3 x'''[n\Delta T_0] \tag{III.6}$$

Substituting e by its expression given in Eq. (III.2) and simplifying Eq. (III.6) yields:

$$x[n] = x[n]^* - (n(\frac{F_s - F_{s0}}{F_s})\Delta T_0)x'[n]^* + \frac{1}{2}(n(\frac{F_s - F_{s0}}{F_s})\Delta T_0)^2 x''[n]^* - \frac{1}{6}(n(\frac{F_s - F_{s0}}{F_s})\Delta T_0)^3 x'''[n]^* \quad \text{(III.7)}$$

Let $\alpha = n\Delta f = n(\frac{F_s - F_{s0}}{F_s})$ and $h = \Delta T_0$. Based on this, Eq. (III.7) can be rewritten in a simpler form:

$$x[n] = x[n]^* - (\alpha h)x'[n]^* + \frac{1}{2}(\alpha h)^2 x''[n]^* - \frac{1}{6}(\alpha h)^3 x'''[n]^* \quad \text{(III.8)}$$

Clearly, the derivatives of Eq. (III.8) shall be approximated and expressed as function of the asynchronous samples set $x[n]^*$. In such a way, each synchronous sample can be computed using asynchronous samples. The approximation can be performed through the use of the finite difference methods [Kiu05]. Applying a backward finite difference on Eq. (III.8) leads to:

$$x[n] = b_0 x[n]^* + b_1 x[n-1]^* + b_2 x[n-2]^* + b_3 x[n-3]^* \quad \text{(III.9)}$$

where (see Appendix C for mathematical proof):

$$b_0 = 1 - \frac{11}{6}\alpha + \alpha^2 - \frac{1}{6}\alpha^3 \quad \text{(III.10)}$$

$$b_1 = 3\alpha - 2.5\alpha^2 + 0.5\alpha^3 \quad \text{(III.11)}$$

$$b_2 = -1.5\alpha + 2\alpha^2 - 0.5\alpha^3 \quad \text{(III.12)}$$

$$b_3 = \frac{1}{3}\alpha - 0.5\alpha^2 + \frac{1}{6}\alpha^3 \quad \text{(III.13)}$$

Equation (III.9) shows that to recompute N samples, $(N+3)$ samples need to be stored. It should be noted also that higher order accuracies will require a bigger buffer. Furthermore, when $n = 0$, all the coefficients disappear except b_0 which is equal to 1, this means $x[0] = x[0]^*$. In other words, the synchronous sample is exactly the same as the asynchronous sample when $n = 0$ while other resampled data are affected by variable coefficients, altering their amplitudes. This means that the phase angle information of the asynchronous sample set $x[n]^*$ is kept after resampling only for $n = 0$. Now, if the backward finite difference coefficients are applied on the whole observation window, taking the most recent sample ($x[0]$) as it is, then $x[0]$ remains unchanged. As a result, performing a N-point DFT on the basis of N recomputed samples using Eq. (I.12) of Chapter I gives the phase angle located at the end of the data window.

The previous derivation is applicable only for frequencies below the nominal value. The computation is slightly different for off-nominal frequencies above the fundamental. For frequencies higher than 50 Hz, considering α as $[n(\frac{f - f_0}{f}) + 2]$ instead of $[n(\frac{f - f_0}{f})]$ gives better accuracy [AT10]. In this case, the estimation is made around the point $2\Delta T_0$ which means that the algorithm requires that two additional samples have to be generated. This delays the transient response of the algorithm by 2 samples times for frequencies above the nominal.

To illustrate the i-SVA algorithm principle, two examples applied on the signal $x(t) = cos(2\pi 45t)$ and $y(t) = cos(2\pi 55t)$, sampled at a sampling rate of $F_{s0} = 48 \times 50$ Hz, at $t = 0.025$ s, are given in Fig. III.4 and Fig. III.5 respectively. Clearly, the amplitude of the samples $n = 0$ at $t = 0.025$ s remain unchanged while the other asynchronous samples are recomputed in such a way that the resampled signals appear to have exactly 48 samples per period, reducing significantly the leakage phenomenon. In Fig. III.5, it can be seen that the computation is performed at $t = 0.025 + 2\Delta T_0$ s to estimate the phasor at $t = 0.025$ s since the frequency is above the nominal value as discussed above.

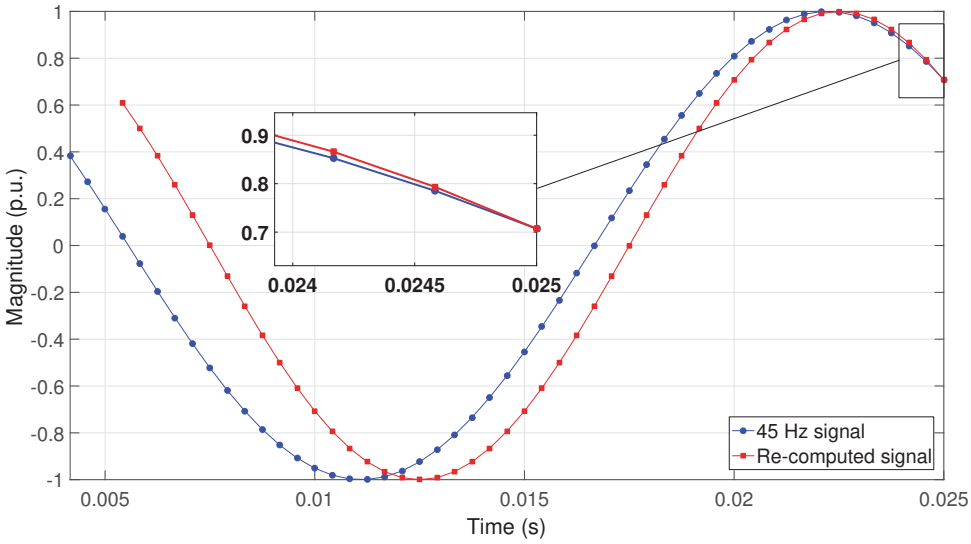

FIGURE III.4 – i-SVA method applied on a 45 Hz signal at $t = 25$ ms

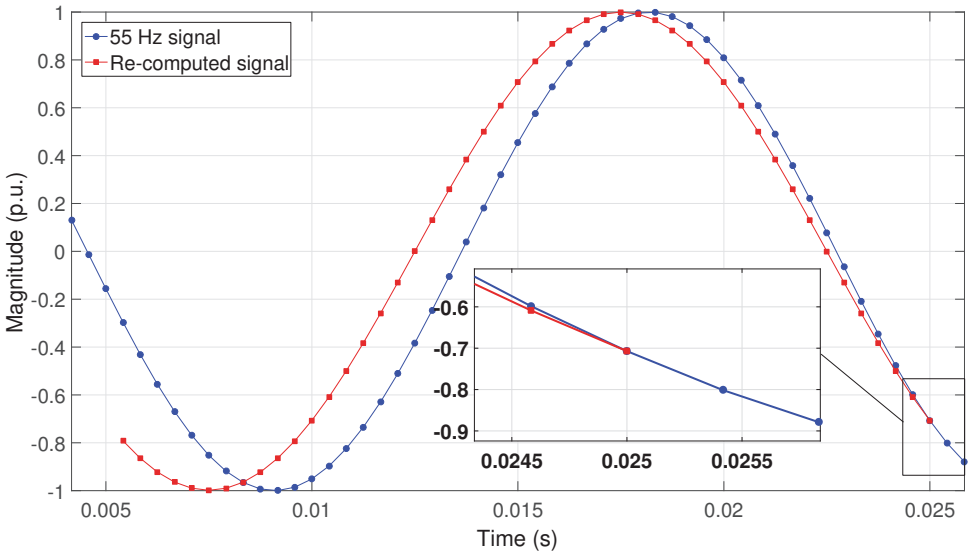

FIGURE III.5 – i-SVA method applied on a 55 Hz signal at $t \approx 25.83$ ms for phasor estimation at $t = 25$ ms

In the current subsection, the i-SVA method has been mathematical derived and illustrated through two examples. The interpolation principle is performed in the time domain as it is the case for the backward linear interpolation method described in the next subsection.

2.3 Backward linear interpolation and frequency-based downsampling

Since the Sampled Measured Values are generated at a high sample rate of 4,800 Hz, the curve between two consecutive samples can be approximated by a straight line. This assumption allows the use of the linear interpolation algorithm. Based on the frequency estimation, the samples of the original signal at the estimated frequency can be calculated using the linear interpolation formula so that the new sampling rate corresponds to the estimated frequency. Phasor estimation is then performed using the resampled data. Now, if the linear interpolation and the downsampling can be merged together, so that one algorithm can do the two functions together, downsampling plus synchronization with the estimated frequency, that algorithm will be a novel solution.

The principle of this algorithm is to compute the magnitude of the sample number k, related to the sample stream after downsampling, and its associated timestamp $t_{low}(k)$ **which is function of the estimated frequency** f. This timestamp is computed as shown:

$$t_{low}(k) = \frac{k}{f \times N_{low}} \tag{III.14}$$

where:

N_{low} is the number of samples per cycle after downsampling, 48 s/c.

Then, a linear interpolation is performed between the two nearest samples $(n-1)$ and n obtained from the process bus, such that:

$$t_{high}(n-1) < t_{low}(k) < t_{high}(n) \tag{III.15}$$

where:

$t_{high}(n)$ is the timestamp associated to the SMV number n.

Based on Eq. (III.14) and Eq. (III.15), the magnitude of the computed sample k is obtained through the following formula:

$$X_{low}(k) = X_{high}(n-1) + (t_{low}(k) - t_{high}(n-1)) \times \left(\frac{X_{high}(n) - X_{high}(n-1)}{t_{high}(n) - t_{high}(n-1)} \right) \tag{III.16}$$

where:

$X_{low}(k)$	is the magnitude of the computed sample k
$X_{high}(n)$	is the magnitude of the sample n from the process bus
$X_{high}(n-1)$	is the magnitude of the sample $(n-1)$ from the process bus

Traditionally, in protection relays, the linear interpolation algorithm is performed "on the fly" which means that the recomputed samples are obtained as time goes by. If it is the case, the recomputed samples may loose the notion of absolute time reference, especially during frequency excursions. Indeed, the linear interpolation generates a new sample stream whose sampling frequency matches the actual power system frequency. Consequently, the timestamps of the new sample stream are related to the estimated frequency, not anymore with the GPS time marks. The "on the fly" linear interpolation and down-sampling algorithm principle is illustrated in Fig. III.6.

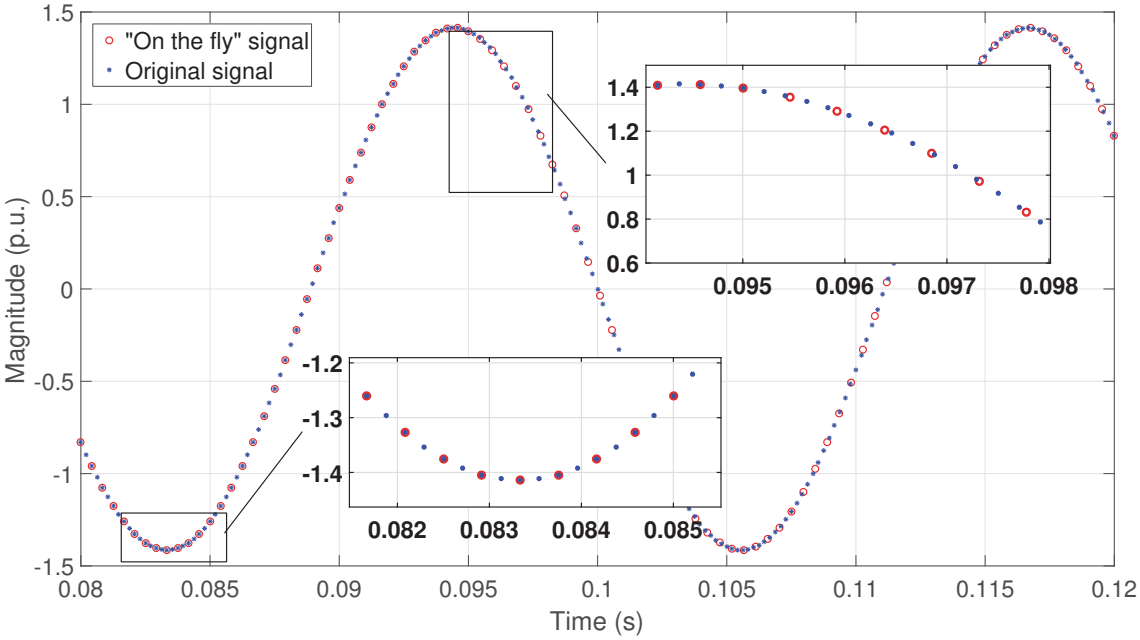

FIGURE III.6 – On the fly interpolation algorithm result, 4,800 Hz to 48 s/c, with an off-nominal frequency of 45 Hz. The sample frequency is updated at $t = 0.095$ s

The frequency is initialized to the nominal one when the algorithm is first executed. In such a condition, the recomputed samples are synchronized to the GPS and the algorithm can be assimilated to a simple down-sampling process. The sampling frequency is updated at $t = 0.095$ s without loss of generality. Subsequently, synchronized sampling is achieved to overcome the leakage problem at the expense of loosing synchronized phase angle. Indeed, the recomputed samples do not match anymore with the input signal sampled at 4,800 Hz.

To counteract this issue, the resampling algorithm can be performed following a reverse (backward) direction. The basic idea consists in keeping the most recent SMV stored in memory as it is and to perform the linear interpolation from the most recent SMVs to the oldest ones. By doing this, both the magnitude and the timestamp of the most recent sample remains unchanged which means that absolute phase angle can be estimated. Moreover, each time the backward interpolation is executed, 48 samples are recomputed on the basis of the 4,800 Hz signal. On the opposite, the "on the fly" interpolation is aimed at computing a single sample during its execution. An example of results obtained for the backward algorithm applied at $t = 0.095$ s is illustrated in Fig. III.7.

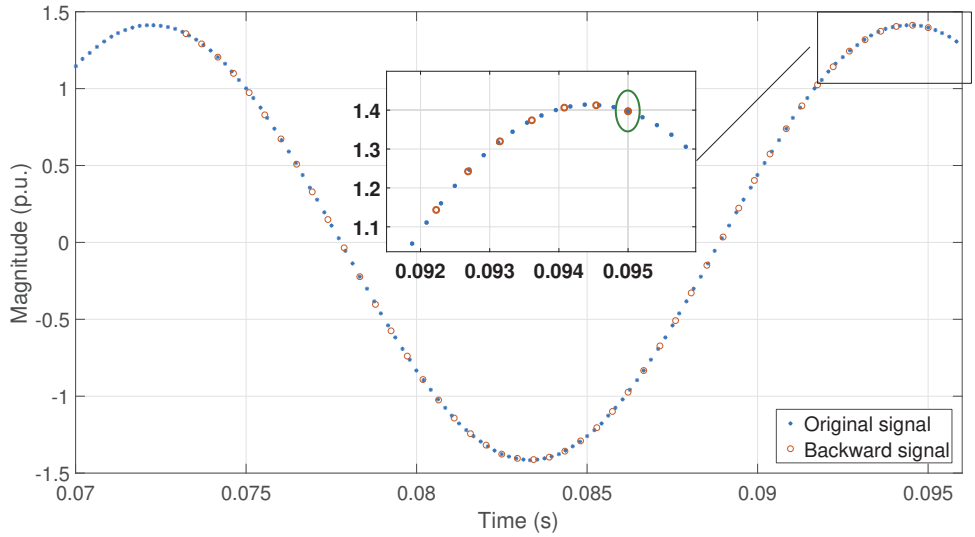

FIGURE III.7 – Backward interpolation algorithm result, 4,800 Hz to 48 s/c, with an off-nominal frequency of 45 Hz. The sample frequency is updated at $t = 0.095$ s

Clearly, at $t = 0.095$ s, the sample is taken as it is and this sample is referred to the GPS time mark. If a 48-points DFT is performed to estimate the phase angle at $t = 0.095$ s, then the phase angle is still synchronized to the absolute time reference. The next time the backward algorithm is executed, the most recent sample of the 4,800 Hz signal will be taken as it is as well which means that the phase angle will be still synchronized with the GPS. Such a method of computation is particularly useful to compute synchrophasors as discussed in Chapter IV.

Since oldest samples are required, a buffer is used to store the samples which will be processed by the backward linear interpolation algorithm. Unlike the i-SVA method, the size of the buffer is directly related to the minimum frequency that is required to be estimated because the sample time depends on the estimated frequency. The less is the frequency, the larger is the buffer size to recompute 1 cycle of data, as shown below:

$$L_{buffer} = \left(\frac{F_s}{f_{min}} \times N_s \right) \tag{III.17}$$

where:

L_{buffer}	is the length of the buffer
f_{min}	is the smallest frequency to be estimated
N_s	is the number of samples contained in 1 SMV frame

For instance, considering a SAMU described as *F4800S1I0U3* (see Section 4.2), that is $N_s = 3$ samples of the three-phase voltages encoded in a single SMV frame generated at $F_s = 4,800$ Hz, the size of the buffer is 2,880 since 5 Hz is the minimal frequency, f_{min}, to be tracked by the algorithm.

3 Improved frequency tracking principle and accurate ROCOF estimations

In the previous section, it is has been clearly specified that the i-SVA and backward linear interpolation methods require a precise estimation of the system frequency to perform the recomputation of samples. The main objective of this section is thus to propose a new frequency tracking principle which remains accurate in various static and dynamic conditions. Now, if the prevailed system frequency is estimated with high accuracy, the ROCOF can be directly computed based on the frequency estimates with high level of accuracy as well which is of utmost importance with the increasing penetration of Distributed Generators (DG) into the distribution network.

3.1 ROCOF estimations in the context of Dispersed Generation

The wide penetration of DG units may lead to the well-known islanding situation in which a part of the distribution system is still energized by DG units despite the fact that this portion has been disconnected from the main source. For safety reasons, these DGs must be isolated from the distribution grid by proper anti-islanding protections. One of the most commonly employed anti-islanding detection method is frequency relays which involved over- and/or under-frequency criteria. However, these frequency-based protection functions typically suffer from a "blind zone" called the non-detection zone in which the relay cannot detect the islanding because the frequency excursion is too small [BCR+15]. To overcome this issue, a ROCOF criterion can be used as a complement to the frequency criteria [KA16]. When islanding occurs, the equilibrium between the generation and the load of the island no longer exists. This mismatch yields a frequency that changes over time as shown in Eq. (III.18) where the governor action has been neglected [TC08]:

$$\frac{\mathrm{d}f}{\mathrm{d}t} = -\left(\frac{P_L - P_G}{2H \times S} \times f_0\right) \tag{III.18}$$

where:

P_L	is the load in the island
P_G	is the output power of the DG unit
H	is the inertia constant of generating plant
S	is the DG unit rating power

However, utility members often complain that the performance of ROCOF relays is not satisfactory today. Indeed, they are sensitive to transient events and this may yield unwanted trippings of DG units. In case of a system involving several DG units, such unwanted tripping can jeopardize the integrity of the system [WM02]. Worse, as stated in [TC08], ROCOF relays available on the market today may respond differently to the same event even if the same setting is used for their configuration. This is due to the fact that these relays employ different algorithms to estimate the ROCOF. The performance of these algorithms depends on the several criteria including the frequency determination method and the size of the window considered over which the ROCOF is estimated [TC08].

In the light of the above-mentioned points, there is a need for improving the accuracy of ROCOF measurement algorithms especially in the smart grid paradigm. To do so, the performance of the classical frequency tracking algorithm used in marketed relays is first analyzed in dynamic conditions. This analysis concerns the accuracy of both the frequency estimates and the ROCOF estimates. Then, a new frequency tracking principle that drastically improves the accuracy of ROCOF estimates is proposed and finally tested under various test cases.

3.2 Classical frequency tracking formulation

Figure III.8 shows the typical frequency tracking algorithm principle. Let us remind that the main goal of this technique is to ensure a synchronization between the sample rate and the actual power system frequency so that the phasor estimates remain accurate in case of frequency excursions. In this figure, it is assumed that the input signals has been already passed through a low-pass FIR filter to reject unwanted frequency components. If the three-phase voltages are considered, the DFTs can be applied on each of the three resampled data windows and the positive sequence component phasor can be subsequently deduced using the operator $\alpha = e^{j\frac{2\pi}{3}}$. Since the positive sequence voltage phasor is already computed, the frequency of the system can be estimated by evaluating the variation of its phase angle over time (phasor-based method). In this study, this angular deviation is computed each half a cycle corresponding to $48/2 = 24$ samples.

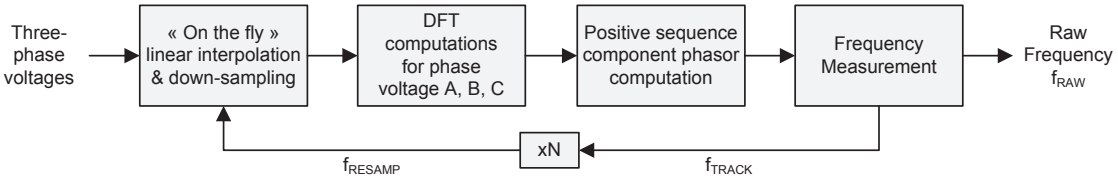

FIGURE III.8 – Typical frequency tracking algorithm principle

The input signals are first processed by the "on the fly" linear-interpolation and down-sampling technique. The down-sampling is driven by the estimated frequency and allows to resample the samples obtained at 4,800 Hz to a fixed number of samples per cycle; $N = 48$ s/c. Then, a 48-points DFT is performed on the last 48 samples for each phase voltage and the power system frequency is determined by computing the phase angle difference between the phasor of the positive sequence and a previous positive sequence phasor estimated 24 samples before. This means that, when the power system frequency and the sample rate are synchronized, the angular deviation is exactly 180 degrees. If it is not the case, then it exists a mismatch between the system frequency and the sample rate and a new sampling frequency is determined based on the new angle (see Eq. (I.54) in Chapter I for mathematical proof). This new sampling frequency is then given to the resampling algorithm which starts to downsample the signal based on the new sample rate. However, the modification of the sampling frequency yields two transient effects during which wrong measurements are obtained as explained below.

The first inaccuracy is directly related to the DFT theory. Remind that the DFT-based estimator requires a unique sampling frequency in the observation window to estimate a given phasor. Since a new sampling frequency has been computed, it is necessary to wait 1 power system cycle to obtain a correct phasor value. If not, the samples of the data window will not be evenly spread out and the associated DFT-based phasor will be wrong. This phenomenon is illustrated in Fig. III.9 where a 48-points DFT is performed at each sample so that to smooth the waveform obtained. Only the output of the "on the fly" linear interpolation and down-sampling algorithm is shown for sake of clarity. It is assumed that synchronous sampling condition is achieved for $N = 48$ s/c. Moreover, it is also assumed that the DFT window is filled with 0 values before it starts to "see" the signal. This is the reason why the DFT transient response of 1 cycle is present at the beginning.

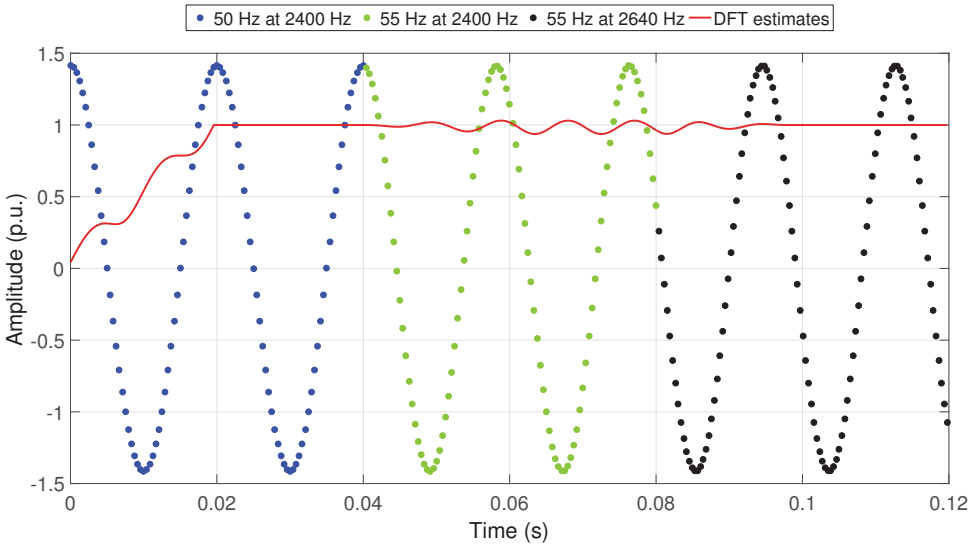

FIGURE III.9 – Example of errors introduced on the magnitude of the DFT estimates when two distinct sampling frequencies are used in a same window

As shown through the blue and black waveforms (see Fig. III.9), there is no error in the magnitude of the DFT estimates in case of synchronous sampling conditions as expected. However, following the frequency jumps from 50 Hz to 55 Hz at $t = 0.04$ s, oscillations occur in the DFT estimates because the sample rate is not an integer multiple of the power system frequency (see Section 4 of Chapter I for mathematical proof). Now, suppose that the frequency tracking algorithm has detected the new frequency of the signal (55 Hz) at $t = 0.08$ s. The new sampling frequency is thus $48 \times 55 = 2,640$ Hz and the signal is being sampled at this rate from $t = 0.08$ s. The oscillations of the amplitude of the DFT estimates start to decrease from this point and finally completely disappear after 1/55 ms, that is 1 cycle of a 55 Hz signal. Indeed, due to the sliding window, the samples obtained following the asynchronous sampling are progressively superseded by samples taken at the correct time (synchronous sampling) which results in less error introduced in the amplitude of the DFT estimates.

The second inaccuracy is the direct consequence of the first one. When the sampling frequency has changed, it is necessary that $N + N/2$ samples (1.5 cycles) are recomputed based on the new sampling frequency before changing the sample rate f_{RESAMP} once again. Notice that $N + N/2$ samples is exactly equal to the window length that is used to estimate the frequency. If this condition is not respected, it means that the computations for estimating the frequency are performed from samples generated by 2 distinct sampling frequencies. This results in wrong phase angle measurements and therefore in wrong frequency estimations f_{RAW} during this transient period of 1.5 cycles. Since the frequency is wrong, the computation of the ROCOF is necessary wrong. In particular, the errors introduced in the ROCOF estimates are higher and last longer than those introduced in the frequency estimates because the ROCOF is the derivative of the frequency. In this study, the ROCOF, $ROCOF[n]$, is computed based on a backward finite difference method to approximate the derivative in its formulation (see Eq. (I.58) of Chapter I). A first-order approximation is chosen to minimize its impact on the ROCOF response time:

$$ROCOF[n] = \frac{f_{RAW}[n] - f_{RAW}[n-1]}{t_{f_{RAW}}[n] - t_{f_{RAW}}[n-1]} \tag{III.19}$$

where:

$t_{f_{RAW}}[.]$ denotes the time at which the $f_{RAW}[.]$ is computed

A delay of exactly 1 cycle has been chosen to compute the ROCOF, that is the size of the window length for estimation of the ROCOF is 2.5 cycles. So, following a modification of the sample rate, the ROCOF estimates are wrong for 2.5 cycles.

Waiting that $N+N/2$ samples are recomputed before estimating a new frequency f_{RAW} is typically not used by fast numerical protection relays. Indeed, remind from Fig. I.22 of Chapter I that the protection pass is related to the estimated frequency. High-speed protection relays typically perform a protection pass every $N/4$ samples to decrease their operating time. This means that a new value of phasor, frequency and ROCOF is available every 12 samples. In such a context, it is clear that the transient errors introduced by the modifications of the sampling rate will occur. To avoid the relay to track a wrong frequency value, it is necessary that the sample rate remains unchanged after being updated for at least 1.5 cycles. In other words, the new f_{TRACK} value must remain the same at least until the errors introduced in the f_{RAW} estimates disappear. All the above explanation about the second inaccuracy is summarized in Fig. III.10 and Fig. III.11 where the input signal is slowly varying according to the time, with a ROCOF of 0.1 Hz/s and a protection pass of $N/4$ samples.

In Fig. III.10, the frequency tracking values f_{TRACK} are updated each 3.5 cycles. This means that correct frequency estimates are performed for 2 cycles. Consequently, the correct ROCOF estimates of 0.1 Hz/s can be measured for 1 cycle only as shown on Fig. III.11. The errors introduced in the ROCOF measurements fluctuate between approximately -0.2 Hz/s and about 0.4 Hz/s following a modification of the sampling frequency. These errors must be disregarded by ROCOF-based protection algorithms to prevent the relay from nuisance tripping. To do so, one option could be to disable the ROCOF-based protection

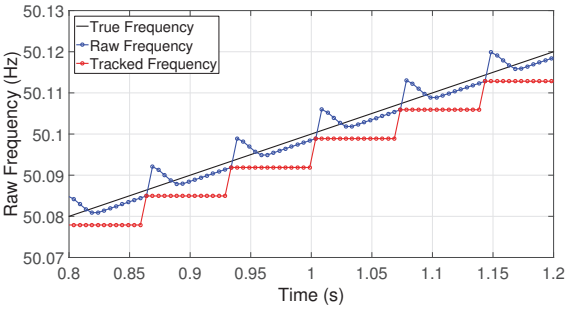

FIGURE III.10 – Example of the "on the fly" frequency tracking algorithm - frequency errors

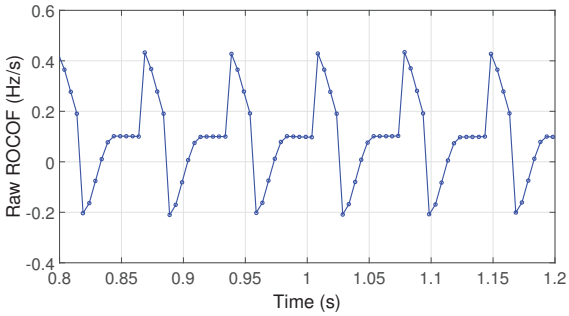

FIGURE III.11 – Example of the "on the fly" frequency tracking algorithm - ROCOF errors

algorithm for 2.5 cycles immediately after the sampling frequency has been updated. This permits to make the algorithm operates only when accurate ROCOF estimates are computed. Another option commonly used to increase the security of ROCOF relay is to increase the size of the measuring window as discussed in [TC08] where windows of 40 ms, 100 ms, and 200 ms are compared. However, in both cases, the improvement of the sensitivity of the relay results in longer operation of the protection function and a compromise between relay security and dependability has to be made by relay designer. To avoid relay designer facing such a situation, a new frequency tracking principle is proposed in the next subsection.

3.3 Improved frequency tracking algorithm design

The objective of the improved frequency tracking algorithm is to eliminate the main cause of the wrong ROCOF measurements, that is the transient error occurring after the modification of the sampling frequency. The challenge is to fix the issue without delaying the tracking of the frequency to avoid the increase of the response time of the relay. The solution is based on the retroactive resampling principle as depicted in Fig. III.12. This retroactive resampling may be based on either the i-SVA method or the backward linear interpolation and down-sampling algorithm.

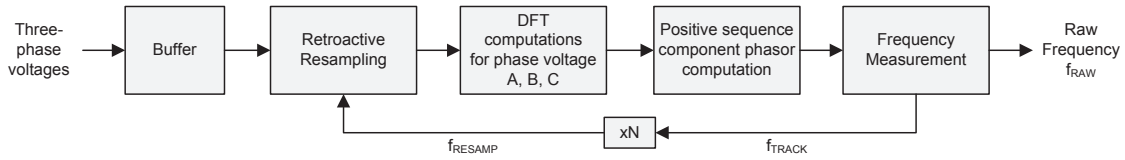

FIGURE III.12 – Backward linear frequency tracking algorithm principle

Remind from Sections 2.2 and 2.3 that the phasors are computed after having resampled the input signals in a retroactive manner. Now, if the retroactive computation is performed for a longer window of data so that estimation of the ROCOF is made possible, then the recomputed samples are obtained with a unique sample rate. Consequently, the DFT estimates obtained on the basis of these recomputed samples are all computed for a unique sampling frequency. This permits to avoid the conditions during which the phasor-

based frequency algorithm uses phasors that are computed based on 2 distinct sampling frequencies. Since the "spikes" in Fig. III.10 are eliminated, the accuracy with which the ROCOF is estimated is considerably improved. To demonstrate the performances of the new frequency tracking algorithm, the same test case applied with the previous method will be used.

Assuming that two phasors delayed by half a cycle are required to estimate the frequency f_{RAW} and that the ROCOF is computed based on 2 frequencies delayed by a cycle, it is clear that the retroactive algorithm must recompute 2.5 cycles of samples to enable the ROCOF estimation. In Fig. III.13, the 2.5 cycles of samples are obtained through the linear interpolation procedure for a system frequency of 45 Hz. The depth of the windows has been reported in Fig. III.13 for better understanding of the method. The backward resampling shall be performed for the three-phase voltages but only 1 phase is represented in Fig. III.13 for sake of clarity. Once the 2.5 cycles are obtained, four 48-points DFT computations are performed for each phase voltage. The delay between two consecutive DFT windows is equal to 24 sample times. Then, four positive sequence phasors are computed and these phasors are used to estimate two frequency values. The first frequency is estimated by computing the phase angle difference between the positive sequence phasors deduced from DFTs denoted 1 and 2. The second frequency estimate is obtained through DFTs denoted 3 and 4. Finally, the ROCOF is measured based on these two frequency estimates (see Eq. (III.19)).

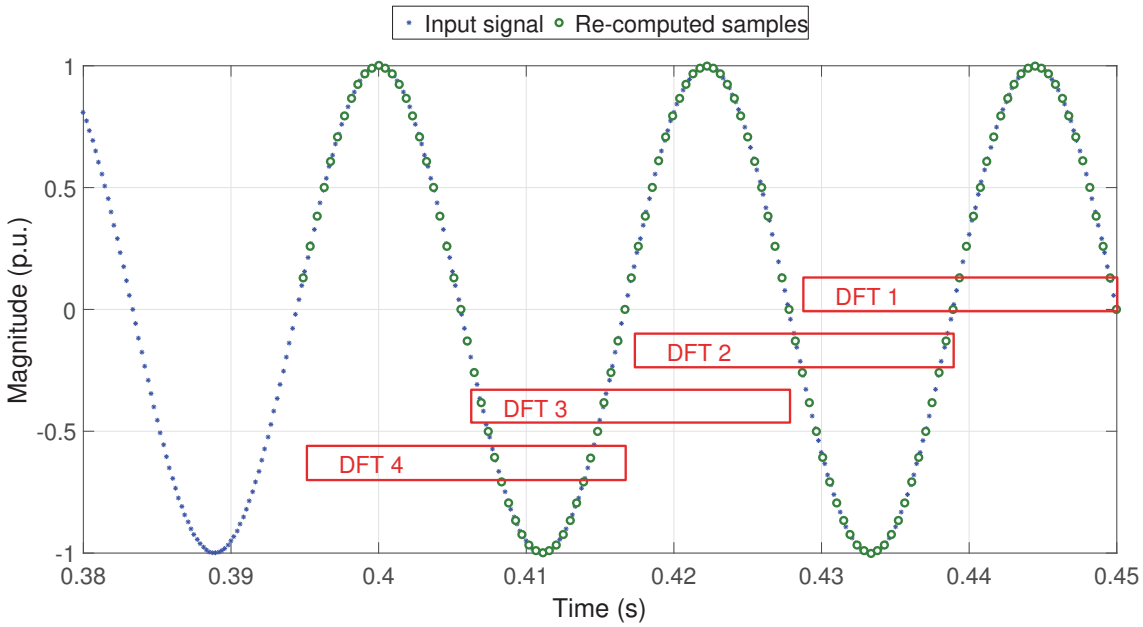

FIGURE III.13 – Linear backward computation for ROCOF estimation - example with a 45 Hz signal

The size of the buffer is another important aspect of this method, especially if the backward linear interpolation is used. In contrast to the i-SVA technique which requires that $N + 3$ samples are stored, being N the window length to compute the ROCOF, the

backward linear interpolation method involves a buffer whose size is function of the minimum frequency wanted to be tracked as discussed in Section 2.3. Since it is required that 2.5 cycles of samples are recomputed at a frequency of 5 Hz, the length of the buffer for the three-phase voltages is 7,200.

Figure III.14 and Fig. III.15 show the results obtained for frequency and ROCOF estimations respectively where the backward linear interpolation and downsampling algorithm is used for the same test case as Section 3.2 to illustrate the superiority of the proposed method against the previous described method.

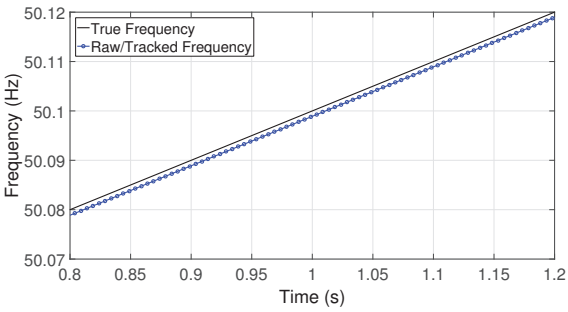

FIGURE III.14 – Example of backward frequency tracking - frequency errors

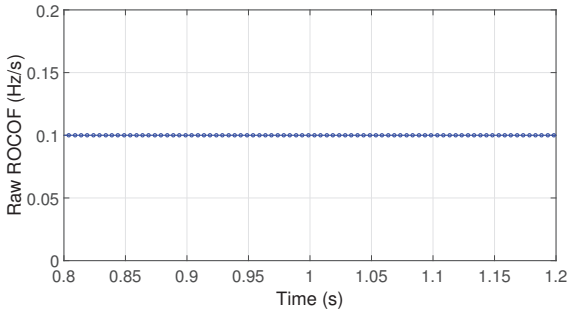

FIGURE III.15 – Example of backward frequency tracking - ROCOF errors

As seen in Fig. III.14, the transient errors in the frequency estimates have been properly eliminated thanks to the backward computation. Since the f_{RAW} values are correct, they can be used directly to change the sample rate f_{TRACK} of the resampling algorithm which ensures a better tracking of the system frequency without degrading the speed of the tracking. Finally, the ROCOF can be evaluated with high accuracy and contains no more errors.

Figure III.16 and Fig. III.17 illustrate the general overviews of the i-SVA and backward linear interpolation methods respectively considering the three-phase voltage as input signals without loss of generality. The compensation of the gain of the FIR anti-aliasing filter can be performed in software since the system frequency is determined.

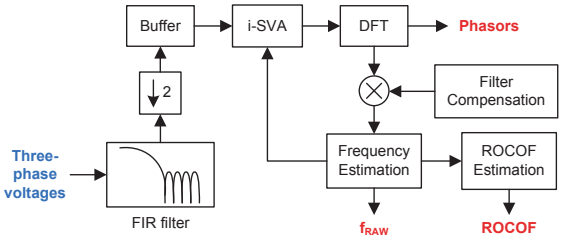

FIGURE III.16 – i-SVA method for estimating phasors, frequency and ROCOF on the basis of SMV coming from the process bus

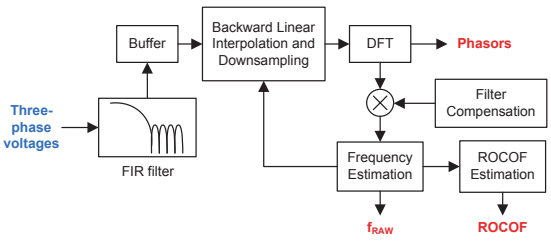

FIGURE III.17 – Backward linear interpolation method for estimating phasors, frequency and ROCOF on the basis of SMV coming from the process bus

In Sections 2 and 3, two solutions based on time-domain resampling methods have been proposed for accurate phasor, frequency, and ROCOF estimations. In the next section, a frequency-domain interpolation method is presented to challenge the performances obtained through the two time-domain algorithms.

4 Interpolated-DFT with tapering

The interpolated-DFT with tapering technique is aimed at reducing the two main errors introduced in phasor estimations: aliasing and leakage effects. Among the papers cited in Section 7.5 of Chapter I, the aliasing problem is solved by sampling the input signal at a rate much higher than the highest frequency component contained in the input signal (typically some tens of kHz). This avoids using an anti-aliasing filter and compensates for the errors it introduces in software. Moreover, the pernicious leakage phenomenon is minimized by using a windowing function and an interpolation scheme. The windowing function deals with the effect of long-range leakage errors caused by the side-lobes of the Fourier transform of the adopted window. The interpolation scheme is used to mitigate the effect of short-range leakage errors introduced in the main frequency of the spectrum which is located at the main lobe of the adopted window [Ant06b].

The IpDFT with tapering method has been extensively studied and applied for synchrophasor estimations as discussed in Section 7.5 of Chapter I with a sampling frequency of some tens of kHz to maximize the measurement accuracy. In what it follows, the IpDFT with Hanning window formulation described in [Gra83] is used and applied for phasors of fundamental frequency with a fixed sampling frequency of 4,800 Hz.

Let us remind from Section 7.5 of Chapter I that a minimum of 2 cycles of samples are necessary in the formulation of the IpDFT algorithm to estimate the phasor. This means that the IpDFT technique has a response time at least twice slower than the full-cycle DFT algorithm which is commonly used for protection algorithms. A slower response time yields a reduction in responsiveness of the relay. To avoid too long operating times, it is clear that the IpDFT method shall be formulated considering a window length of 2 cycles.

To explain the main idea of the interpolation process, let us first remind that the window length is related to the frequency resolution Δf, that is the distance in Hertz between two adjacent DFT bins, as

$$\Delta f = \frac{F_s}{M} \tag{III.20}$$

For $F_s = 4,800$ Hz and $M = 96$ (window length of 1 cycle), the frequency resolution is 50 Hz. Since 2 cycles are used by the IpDFT method developed in this study, the resolution becomes 25 Hz which means 1 DFT bin can be estimated each 25 Hz. In Fig. III.18, the signal $x(t) = \sqrt{2}A\cos(2\pi(47)t)$ is processed by a 2-cycle DFT algorithm with a rectangular window and after being sampled at a rate of 4,800 Hz. This DFT is performed for the whole frequency spectrum with a frequency resolution of 25 Hz. Nevertheless, only a zoom around the actual frequency is shown. The DFT spectrum is tuned to the frequency 47 Hz

to depict the expected position of the main lobe to obtain exact phasor values. The term δ is used to show the gap between the highest DFT bin and the DFT maximum spectrum value at 47 Hz. Because of the leakage, the frequency of interest is located between the two highest DFT bins of the spectrum which are contained within the main lobe. Now, the basic idea of the IpDFT algorithm is to determine δ to find the position of the main frequency component of the input signal by means of interpolation. This interpolation is performed between the two highest DFT bins of the spectrum which are located at 25 Hz and 50 Hz in Fig. III.18.

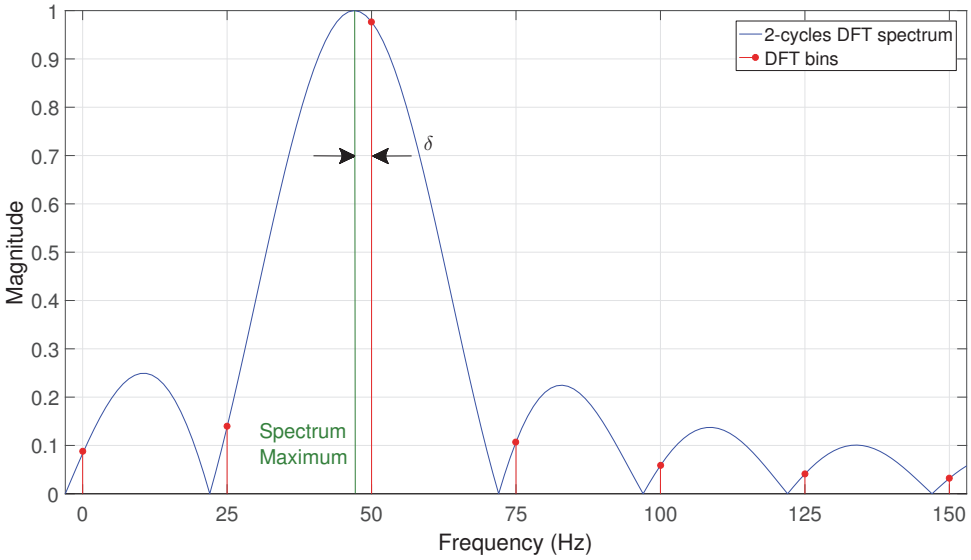

FIGURE III.18 – Basic idea of the interpolation in the frequency domain through the IpDFT method

The IpDFT with Hanning window algorithm is composed of three main steps:

1. Filtering of the input signal through the Hanning window,
2. Computation of the DFT bins through the 2-cycles DFT algorithm,
3. Interpolation in the spectrum domain between the two highest DFT bins.

To formulate the IpDFT method, the finite sequence of samples $x[n]$ is considered:

$$x[n] = A\cos(2\pi\frac{f}{F_s}n + \varphi), \quad 0 \leq n \leq M-1 \tag{III.21}$$

where:

F_s is the sample rate of the SMV ; 4800 Hz
M is the number of samples acquired in exactly 2 cycles, that is 192

The relationship between the system frequency f and the frequency resolution Δf can be expressed as [Gra83]:

$$f = (l+\delta)\Delta f = \lambda\Delta f \tag{III.22}$$

where:

l is the index of the DFT bin with the highest amplitude
δ is the deviation of f from the relative DFT maximum $l\Delta f$

A Hanning window is commonly used for its simplicity to derive an IpDFT algorithm. It can be written in the discrete domain as:

$$w_H[n] = \frac{1 - \cos(\frac{2\pi n}{M})}{2}, \quad 0 \leq n \leq M-1 \tag{III.23}$$

The signal $x[n]$ is multiplied by the Hanning function $w_H[n]$ and the DFT of the windowed signal $x_w[n] = x[n] \cdot w_H[n]$ is computed as (see Appendix E for mathematical proof):

$$\begin{aligned} \overline{X_w(k)} &= \frac{1}{G_H} \sum_{n=0}^{M-1} x_w[n] e^{-j\frac{2\pi}{M}nk} \\ &= \overline{X_w^+(k)} + \overline{X_w^-(k)} \end{aligned} \tag{III.24}$$

where:

G_H	is the gain of the Hanning window, that is $G_H = \sum_{n=0}^{M-1} w_H[n]$
$\overline{X_w^+(k)}$	is the positive image of the DFT bins
$\overline{X_w^-(k)}$	is the negative image of the DFT bins

In Eq. (III.24), the long-range leakage error produced by the negative spectrum image on the positive one can be neglected assuming that the Hanning window has properly mitigated this error. This means that the DFT spectral lines are generated in the positive frequency range through the positive image $\overline{X_w^+(k)}$ solely [Gra83]. In accordance with the derivation performed in Appendix E, the positive spectrum image is expressed as it follows:

$$\begin{aligned} \overline{X_w^+(k)} = \frac{Ae^{j\varphi}}{4G_H} [& \frac{\sin(\pi(\lambda-k))}{\sin(\frac{\pi}{M}(\lambda-k))} e^{ja(\lambda-k)} \\ & - 0.5(\frac{\sin(\pi(\lambda-1-k))}{\sin(\frac{\pi}{M}(\lambda-1-k))} e^{ja(\lambda-1-k)} + \frac{\sin(\pi(\lambda+1-k))}{\sin(\frac{\pi}{M}(\lambda+1-k))} e^{ja(\lambda+1-k)})] \end{aligned} \tag{III.25}$$

where $a = \pi(M-1)/M$. The interpolation between the two highest bins is possible if they are correctly identified in the spectrum. One of the two maximum spectral lines corresponds to the highest spectral line of the spectrum, indexed l, and can be therefore easily identified. The second highest bin is one of the bins adjacent to the maximum bin, indexed $(l-1)$ and $(l+1)$. As a consequence, the determination of the second highest DFT bin can be found by comparing the magnitude of the spectral lines adjacent to the maximum bin as shown:

$$\epsilon = \text{sgn}(|\overline{X_w^+(l+1)}| - |\overline{X_w^+(l-1)}|) \tag{III.26}$$

Thus, to correct the errors introduced in the spectral line of fundamental frequency, two additional DFTs need to be performed to estimate the spectral lines positioned at $(l-1)$ and $(l+1)$ so that the interpolation process can be applied. Indexes $(l-1)$ and $(l+1)$ correspond to the frequencies 25 Hz and 75 Hz according to the selected frequency resolution. Based on Eq. (III.26), the ratio between the two highest bins is computed as:

$$\alpha = \frac{|\overline{X_w^+(l+\epsilon)}|}{|\overline{X_w^+(l)}|} \tag{III.27}$$

where:

$$\begin{aligned}\overline{|X_w^+(l)|} = |\frac{Ae^{j\varphi}}{4G_H}[\frac{\sin(\pi\delta)}{\sin(\frac{\pi}{M}\delta)}e^{ja\delta} \\ - 0.5(\frac{\sin(\pi(\delta-1))}{\sin(\frac{\pi}{M}(\delta-1))}e^{ja(\delta-1)} + \frac{\sin(\pi(\delta+1))}{\sin(\frac{\pi}{M}(\delta+1))}e^{ja(\delta+1)})]|\end{aligned} \tag{III.28}$$

$$\begin{aligned}\overline{|X_w^+(l+\epsilon)|} = |\frac{Ae^{j\varphi}}{4G_H}[\frac{\sin(\pi(\delta-1))}{\sin(\frac{\pi}{M}(\delta-1))}e^{ja(\delta-\epsilon)} \\ - 0.5(\frac{\sin(\pi(\delta-2))}{\sin(\frac{\pi}{M}(\delta-2))}e^{ja(\delta-\epsilon-1)} + \frac{\sin(\pi\delta)}{\sin(\frac{\pi}{M}\delta)}e^{ja(\delta-\epsilon+1)})]|\end{aligned} \tag{III.29}$$

To process further and compute Eq. (III.27) in a cost-effective way, an approximation needs to be made. Since M is high (and equals to 192), the sinus terms in the denominators of Eqs. (III.28) and (III.29) may be substituted by their respective arguments. Based on this, it can be shown, by substituting Eqs. (III.28) and (III.29) in Eq. (III.27), that δ is related to α and ϵ through the following equation [Gra83]:

$$\delta = \frac{2\alpha - 1}{\alpha + 1} \times \epsilon \tag{III.30}$$

Since δ is known, it can be used to correct the wrong magnitude and phase angle values initially obtained as shown [Gra83]:

$$A_c = \sqrt{2}|\overline{X_w^+(l)}| \cdot \frac{\pi\delta(1-\delta^2)}{\sin(\pi\delta)} \tag{III.31}$$

$$\varphi_c = \angle\overline{X_w^+(l)} - \pi\delta \tag{III.32}$$

where:

A_c	is the magnitude estimation of the theoretical magnitude A in Eq. (III.21)
φ_c	is the phase angle estimation of the theoretical phase angle φ in Eq. (III.21)

Finally, the prevailed frequency is estimated based on Eq. (III.22) and the ROCOF can be deduced subsequently on the basis of the first-order backward approximation formula defined in Eq. (III.19). Figure III.19 depicts the diagram of the IpDFT algorithm using a Hanning window considering the three-phase voltage signals as inputs without loss of generality.

In this section, the IpDFT with Hanning window technique has been presented. In the next section, simulation results are provided to compare the performances of the IpDFT technique with the two time-domain algorithms described in Sections 2 and 3.

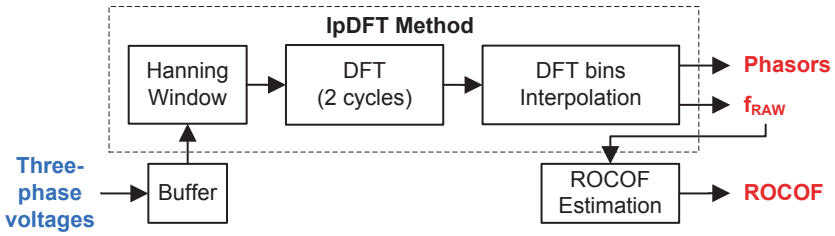

FIGURE III.19 – IpDFT algorithm coupled with a Hanning window for estimating phasors, frequency and ROCOF on the basis of SMV coming from the process bus

5 Simulation and results analysis

This section presents the simulation and result analysis for a power system with 50 Hz nominal frequency. The parameters under analysis are the magnitude of the phase A voltage phasor, the phase angle difference between the phase A and the phase B, the frequency estimates obtained through the voltage positive sequence and the ROCOF measurements. The magnitude and the phase angle are assessed by computing their corresponding relative error in comparison to their ideal value. The three algorithms, i-SVA, backward linear interpolation and IpDFT with Hanning window have been implemented using the MATLAB environment. The digital FIR filter designed in Section 2.1 is not considered in this section so that to highlight the response times of the frequency and ROCOF estimation algorithms involved in the time-domain resampling solutions. Nevertheless, the FIR filter will be taken into account in the simulation results presented in Chapter IV. Four different scenarios are presented below to test the performance of the algorithms:

1. Steady state signals at off-nominal frequency with harmonics
2. Very slow ramp of frequency
3. Fast ramps of frequency
4. Frequency jump

These test cases have been chosen to demonstrate the performance of the methods under frequency variations. A protection scan of 5 ms is considered, that is a new phasor, frequency, and ROCOF estimates are computed every 5 ms. For magnitude and phase angle estimations, the errors expected to be introduced by the algorithms should be close to 0%. Similarly, errors near 0 Hz and 0 Hz/s are expected in steady-state condition for frequency and ROCOF estimations. In dynamic condition, since a closed-loop system is used to estimate the frequency for the time-domain algorithms, there will be always an error called the tracking error. This error depends on both the window length used to compute the frequency and the ROCOF involved during the tracking. Long windows will delay the tracking which results in an increase of the tracking error. Fast ROCOF values will also add more tracking errors as it will be shown in Sections 5.2 and 5.3. Since the tracking error is dependent of the ROCOF, it is difficult to define a maximum permissible error for frequency estimation during dynamics. However, for the ROCOF measurements, the maximum permissible error can be defined in dynamics by essence and is set to 0 Hz/s.

5.1 Steady-state signals at off-nominal frequency with harmonics

Let us consider the balanced three-phase voltages distorted by high order harmonic components be expressed as:

$$V_a(t) = A_1 \cos(2\pi f t) + \sum_{m=2}^{M} A_m \cos(2\pi f_m t) \tag{III.33}$$

$$V_b(t) = A_1 \cos(2\pi f t - \frac{2\pi}{3}) + \sum_{m=2}^{M} A_m \cos(2\pi f_m t - \frac{2\pi}{3}) \tag{III.34}$$

$$V_c(t) = A_1 \cos(2\pi f t + \frac{2\pi}{3}) + \sum_{m=2}^{M} A_m \cos(2\pi f_m t + \frac{2\pi}{3}) \tag{III.35}$$

where:

A_1	is the magnitude of the fundamental, $A_1 = \sqrt{2}$
f	is the off-nominal steady-state frequency, $f = 51$ Hz
A_m	is the magnitude of the m^{th} harmonic component
f_m	is the m^{th} harmonic frequency, multiple of 51 Hz

The harmonic content of the signals defined in the above equations is reported in Table III.1. This harmonic content has been specified in [fp02] where it is used to check the compatibility levels for harmonics in industrial plants. The total harmonic distortion is equal to about 14%. Last but not the least, the harmonics are contained in the passband of each algorithm and no filter has been used to remove them.

TABLE III.1 – Harmonic content of the input signals

Harmonic number	2	3	4	5	6	7	8	9	10	11	12
Amplitude (% of A_1)	3%	6%	1.5%	8%	1%	7%	1%	2.5%	1%	5%	1%

The simulation runs for 2 seconds. Nevertheless, only a zoom is provided on each figure because the responses are repeating in the same pattern. As shown in Figs. III.20 and III.21, the three algorithms show stability in presence of harmonics at off-nominal frequency and error near 0% in both magnitude computation and phase angle computation. The best performances are obtained with the i-SVA method whilst IpDFT gives less accuracy in terms of phase angle estimation with errors that can reach 0.25% approximately.

Regarding the frequency and ROCOF estimations, the i-SVA and backward linear interpolation algorithms give the best results with errors less than 1 mHz and 0.18 Hz/s respectively. The IpDFT method is the less accurate technique in such a configuration since the errors introduced in the frequency estimates may vary from -0.42 to 0.44 Hz approximately while the ROCOF measurements fluctuate between about -2.7 Hz/s and 2.7 Hz/s. The ROCOF measurements obtained are the results of the successive derivative computations performed on the frequency estimates delayed by 20 ms. Since errors are introduced in the frequency estimates, the ROCOF measurements, computed based on

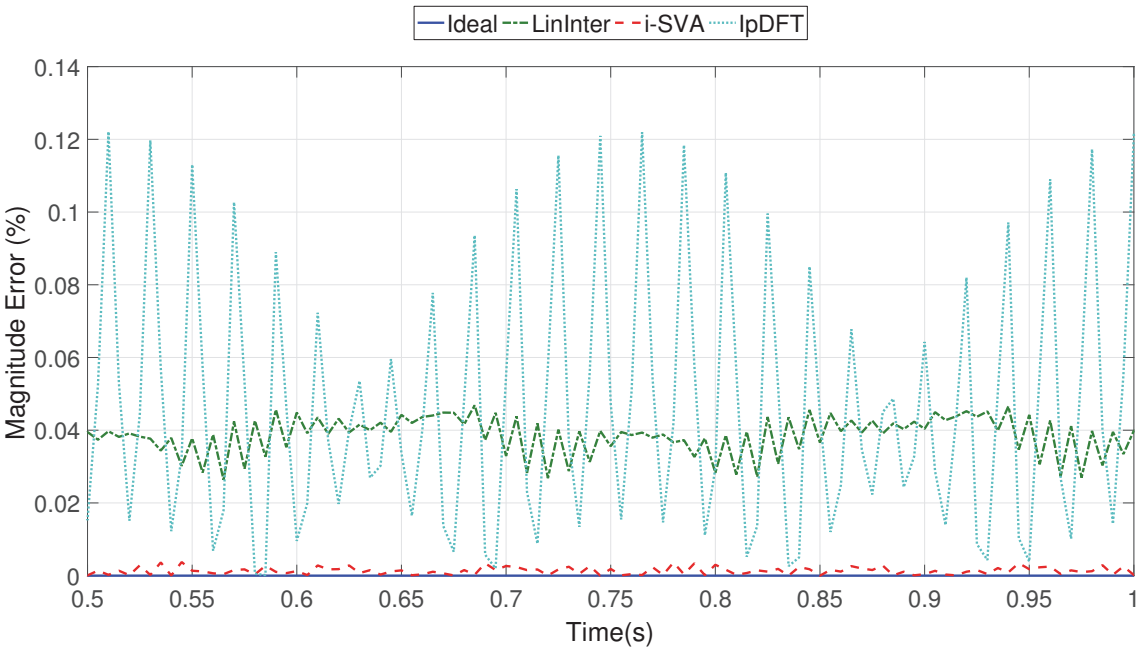

FIGURE III.20 – Magnitude computation response of steady-state signals at off-nominal frequency with harmonics

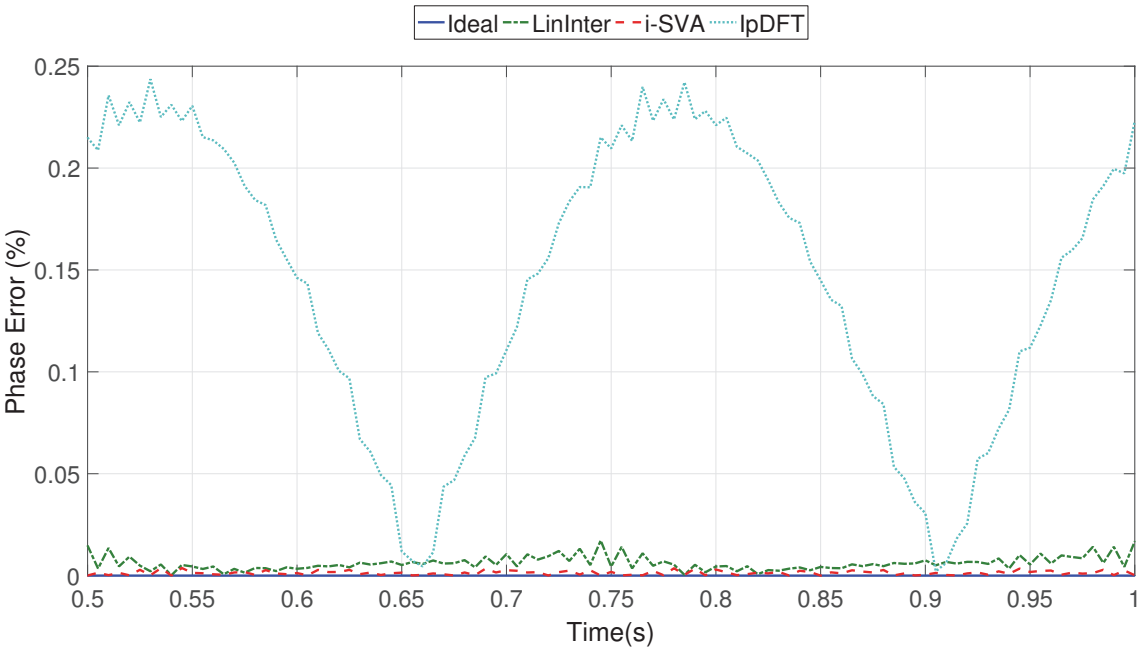

FIGURE III.21 – Phase angle computation response of steady-state signals at off-nominal frequency with harmonics

the backward first-order approximation, are estimated with low accuracy.

The sensitivity of the IpDFT algorithm in this test case can be explained by the assumptions performed to derive the algorithm. The IpDFT assumes that the spectral interference produces by both the bins of harmonics and those related to the negative image

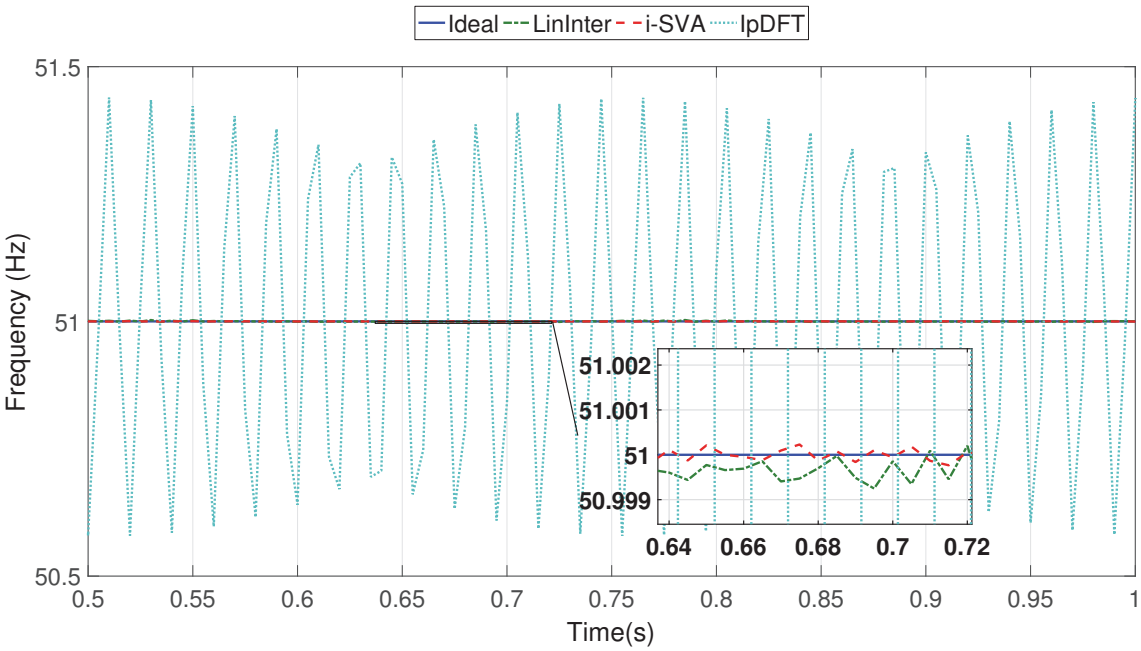

FIGURE III.22 – Frequency computation response of steady-state signals at off-nominal frequency with harmonics

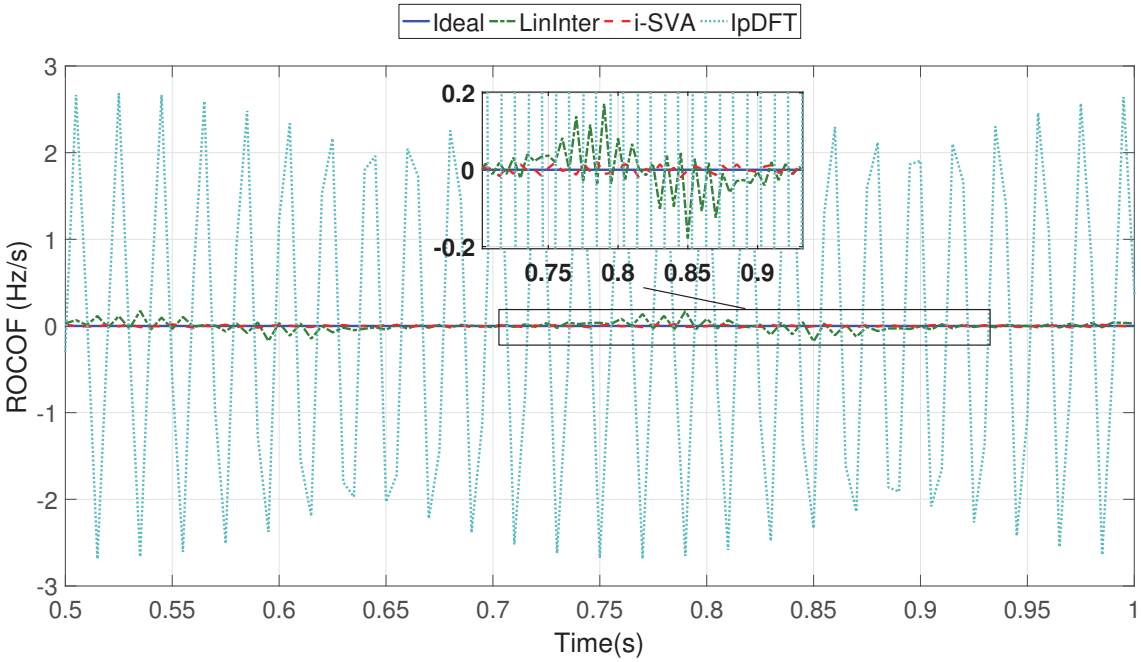

FIGURE III.23 – ROCOF computation response of steady-state signals at off-nominal frequency with harmonics

of the DFT spectrum is negligible since the Hanning window is used. However, since several low order harmonics are superimposed to the fundamental frequency (contained in the main lobe), the negative image of the DFT spectrum may generate a high spectral interference on the positive one resulting in measurements with low accuracy.

The i-SVA and backward interpolation algorithms do not suffer from harmonics even if the system frequency is held at an off-nominal value because the frequency is estimated with high accuracy. Due to this fact, the resampling can be performed with almost no error which lead to accurate estimations of magnitude and phase angle.

5.2 Very slow ramp of frequency

Considering a three-phase balanced system, a ramp of frequency can be mathematically represented by the following equation:

$$V_a(t) = A_1 \cos(2\pi f t + \pi R_f t^2) \tag{III.36}$$

$$V_b(t) = A_1 \cos(2\pi f t + \pi R_f t^2 - \frac{2\pi}{3}) \tag{III.37}$$

$$V_c(t) = A_1 \cos(2\pi f t + \pi R_f t^2 + \frac{2\pi}{3}) \tag{III.38}$$

where:

f	is the initial frequency
R_f	is the frequency ramp rate in Hz/s

In a first step, a very slow ramp of frequency of 0.1 Hz/s is applied at $t = 0.2$ s. The initial frequency is set to 50 Hz and the duration of the simulation is 1 s. Figures III.24 and III.25 show excellent accuracy for the three algorithms with errors near 0% for both magnitude and phase angle computation for the phasor of phase voltage A.

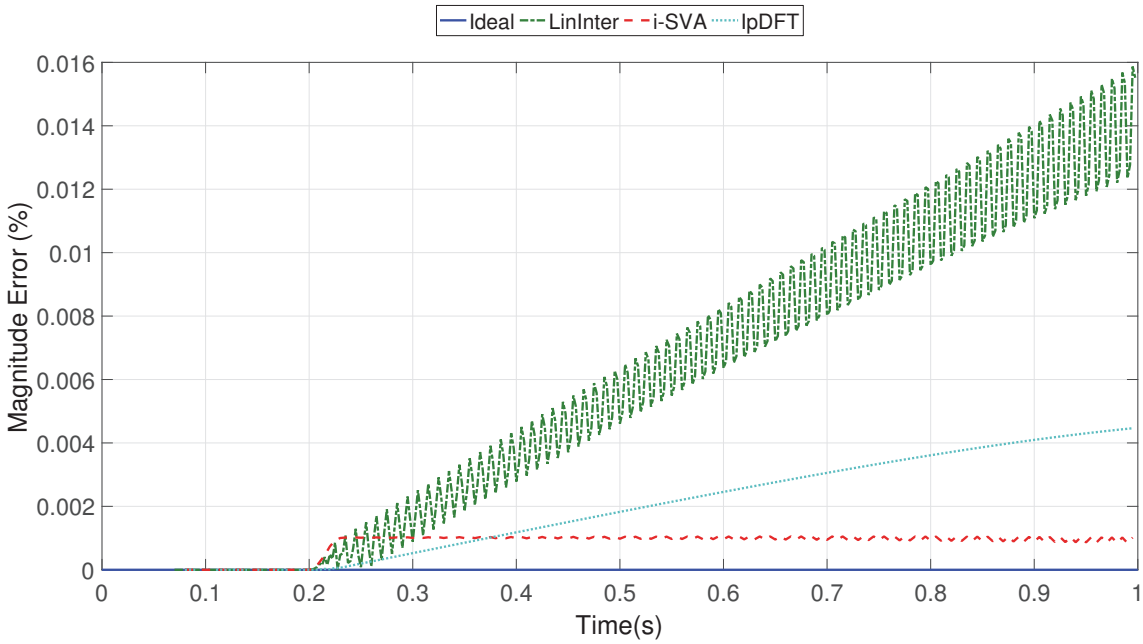

FIGURE III.24 – Magnitude computation response of very slow ramp of frequency

Figure III.26 depicts the frequency estimates obtained through the three methods. Clearly, the frequency tracking is very accurate for the three algorithms. A zoom has

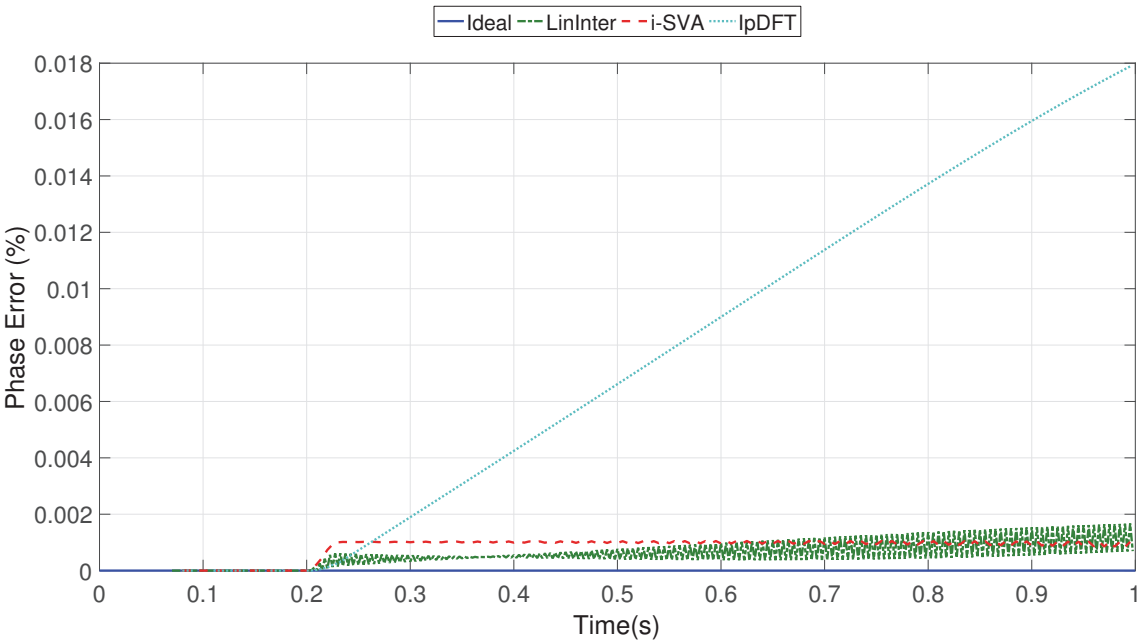

FIGURE III.25 – Phase angle computation response of very slow ramp of frequency

been provided to illustrate the speed of the tracking for each method. It can be seen that both the backward linear interpolation and i-SVA methods are able to track the real frequency value with a delay of 15 ms and $(15 + 2\Delta T_0)$ ms [1], with $\Delta T_0 = 1/1200 \approx 0.833$ ms, respectively whereas the IpDFT method requires 20 ms to retrieve the actual system frequency. The delay introduced by the tracking is directly related to half the window length considered to perform the frequency estimation.

Figure III.27 illustrates the ROCOF estimates with a focus on the occurrence of the step from 0 Hz/s to 0.1 Hz/s at $t = 0.2$ s. This makes it possible to measure the ROCOF algorithm transient response for the three methods. As expected, the duration of the transient is equal to 50 ms for the backward linear interpolation, that is 2.5 cycles of a 50 Hz system, 50.833 ms for the i-SVA method and 60 ms for the IpDFT algorithm. Finally, the static error is very near to 0.

5.3 Fast ramps of frequency

For this test scenario, two fast ramps of frequency are applied to the inputs signals. First, the signals are held to the frequency 40 Hz for a duration of 0.5 s. Then, a positive ramp of frequency of +30 Hz/s starts and lasts during 0.5 s so that the frequency reaches a value of 60 Hz. After, the signals remain at 60 Hz for 0.5 s. At $t = 1.5$ s, the frequency ramps down to the rated frequency with a ROCOF of −20 Hz/s for 0.5 s. Finally, the signals are held to the nominal frequency (see Fig. III.30).

Figures III.28 and III.29 show the magnitude and phase responses respectively where the better accuracy is obtained with the backward linear interpolation algorithm with er-

1. Since $f > f_0$ a delay of $2\Delta T_0$ is added.

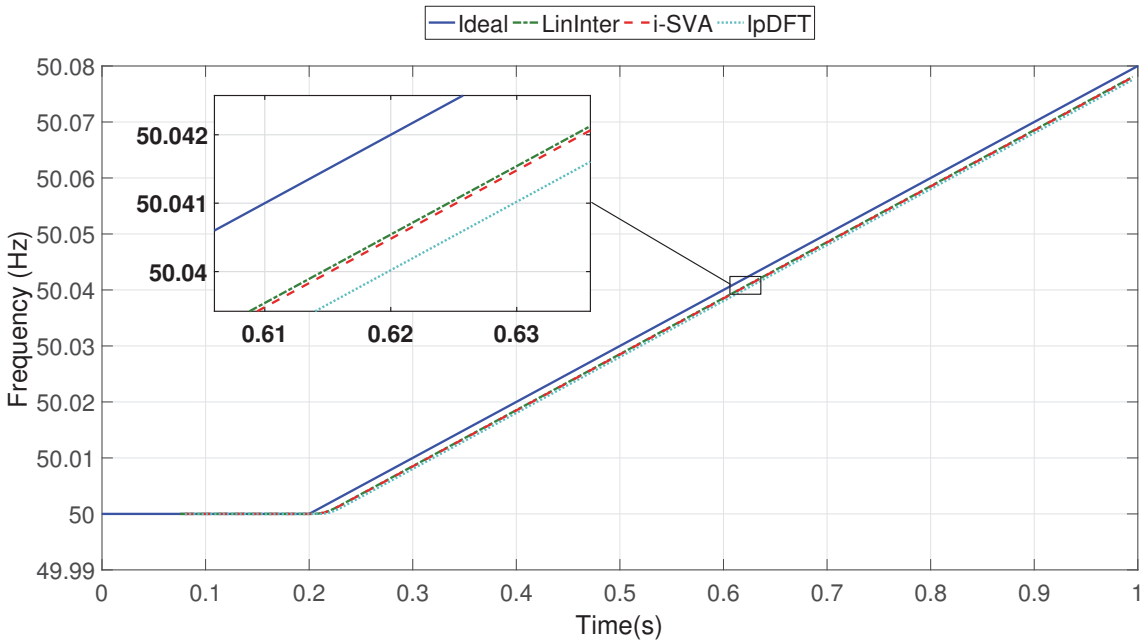

FIGURE III.26 – Frequency computation response of very slow ramp of frequency

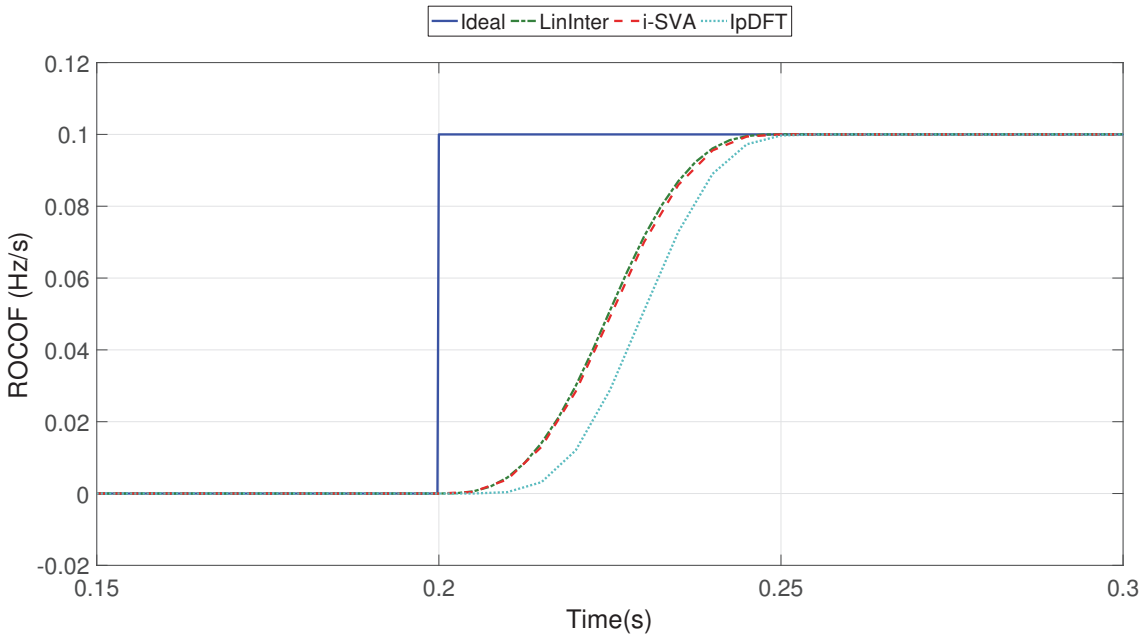

FIGURE III.27 – ROCOF computation response of very slow ramp of frequency

rors less than 0.5% in both magnitude and phase angle on the whole duration of the test. For static frequency deviations of ±10 Hz, the i-SVA method is not accurate for estimating the magnitude and the phase angle of the input signal since the errors can exceed 1%. This could be explained by the fact that the order of the Taylor series chosen (third order) to derive the algorithm is probably too small for large frequency excursions. Better accuracy are expected if higher orders are used but this will also require more computational burden.

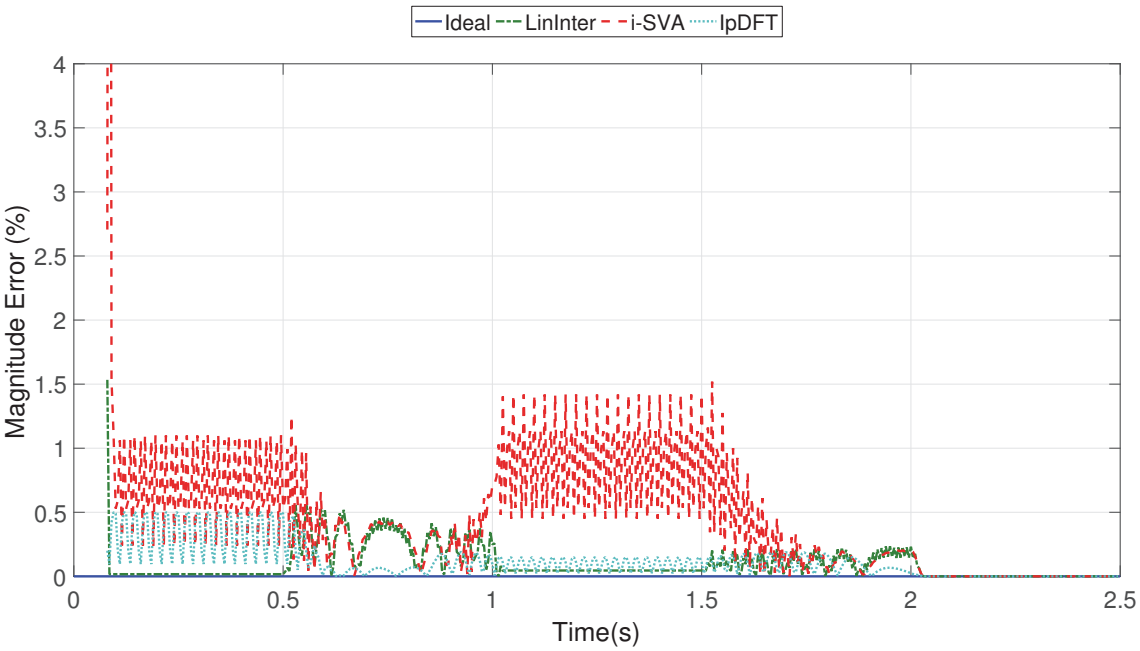

FIGURE III.28 – Magnitude computation response of fast ramps of frequency

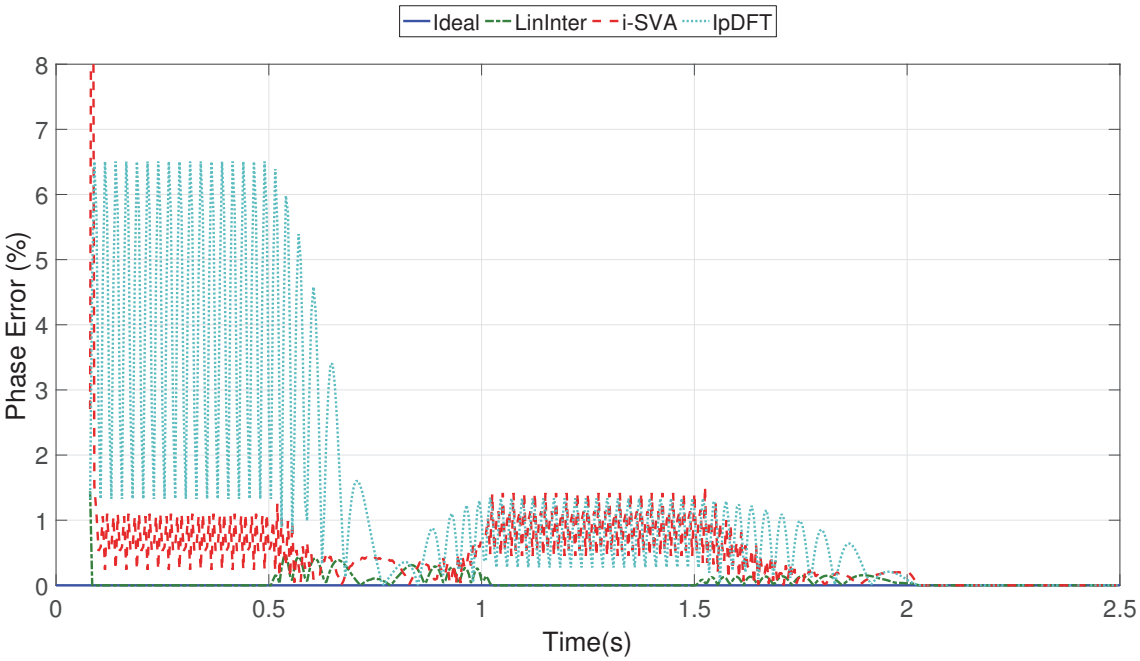

FIGURE III.29 – Phase angle computation response of fast ramps of frequency

Moreover, the IpDFT technique gives low accuracy in phase angle estimation with errors fluctuating between about 1.33% and 6.51% when a frequency of 40 Hz is applied. Since the frequency excursion is high, the term δ in Eq. (III.22) increases and becomes less negligible in front of the M in Eqs. (III.28) and (III.29). Therefore, substituting the sinus terms in the denominators of Eqs. (III.28) and (III.29) by their respective arguments becomes a less reliable approximation and the term α is estimated with low accuracy. Subsequently, δ is also wrong which results in poor magnitude and phase angle measurements.

Finally, the high errors that can be seen at $t = 0.08$ s are directly related to the frequency tracking. Indeed, since the input signals are held at 40 Hz and the i-SVA and backward linear interpolation algorithms are initialized at 50 Hz, errors are introduced in the phasors up till the frequency estimate converges to the correct value. This phenomenon can be better understood by looking at Fig. III.30.

Figure III.30 illustrates promising performance of the frequency tracking algorithms and the IpDFT technique during fast ramps. For the backward linear interpolation and IpDFT methods, the speeds of the tracking are identical to those obtained during the slow ramp test case whatever the nature of the ROCOF is, that is positive or negative. However, as it can be seen through the zooms provided in Fig. III.30, when the i-SVA technique is used, the speed of the tracking is delayed by 2 sample times for frequencies higher than the nominal as expected. For frequencies lower than the nominal, the speed is exactly equal to 15 ms as expected. Moreover, for the ROCOF estimates, the performance are also remarkable as depicted in Fig. III.31. It should be noticed that, even if it is not obvious on the zoom provided in the aforementioned figure, the error in the ROCOF estimate reaches exactly 0 after 60 ms following the step for the IpDFT technique as expected.

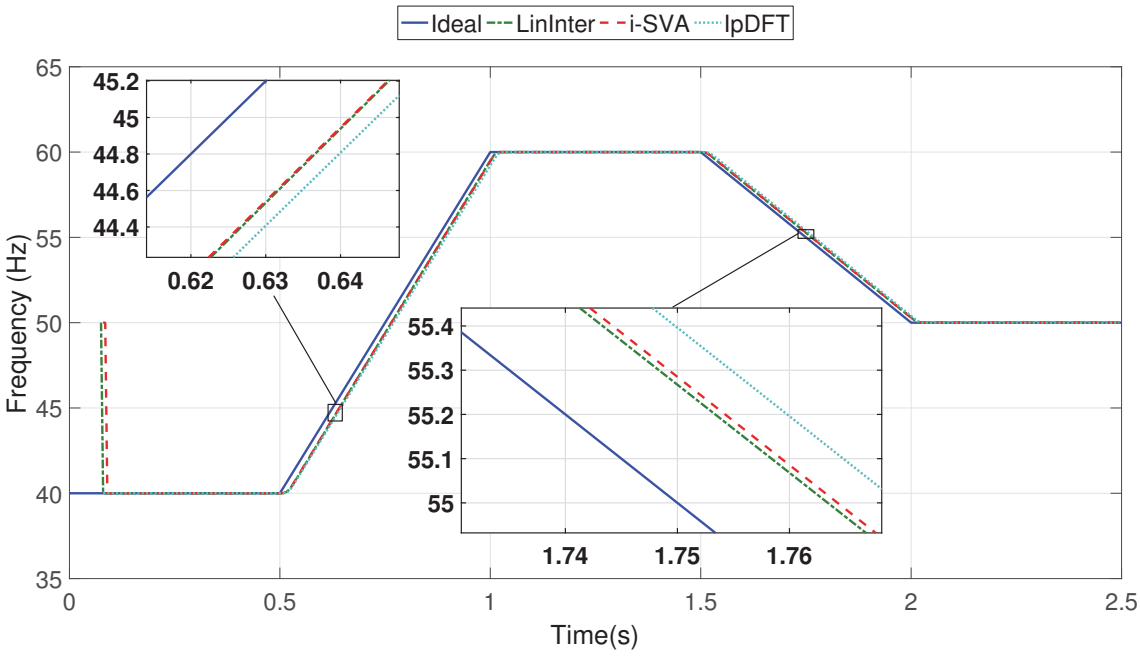

FIGURE III.30 – Frequency computation response of fast ramps of frequency

5.4 Frequency Jump

A jump of the power system frequency is an important test to carry out because it permits to measure the transient response of the frequency estimation algorithms. Let consider a three-phase balanced voltage system under which the frequency jump is applied.

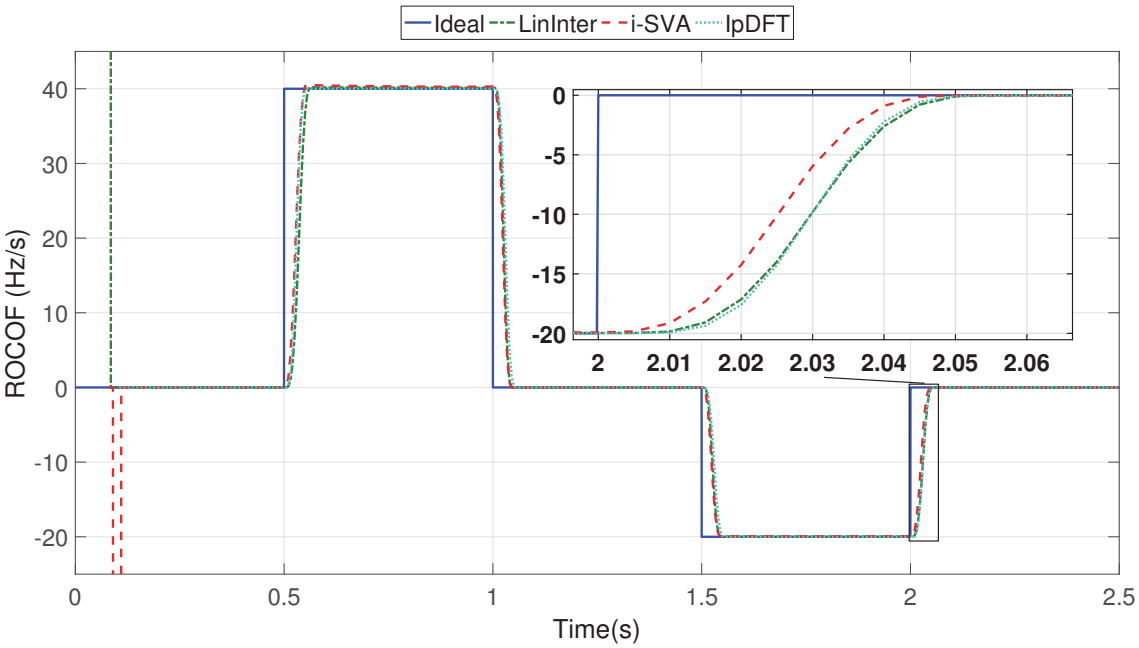

FIGURE III.31 – ROCOF computation response of fast ramps of frequency

Mathematically, this phenomenon can be expressed as:

$$V_a(t) = A_1 \cos(2\pi(f_0 + \Delta f \cdot u(t))t) \tag{III.39}$$

$$V_b(t) = A_1 \cos(2\pi(f_0 + \Delta f \cdot u(t))t - \frac{2\pi}{3}) \tag{III.40}$$

$$V_c(t) = A_1 \cos(2\pi(f_0 + \Delta f \cdot u(t))t + \frac{2\pi}{3}) \tag{III.41}$$

where:

Δf	is the frequency deviation from nominal in Hz
$u(t)$	is the unit step function

The test is conducted as it follows. The three-phase voltages are initially set to the nominal frequency, that is 50 Hz. At $t = 0.2$ s, the frequency jumps from 50 Hz to 55 Hz and remains at 55 Hz for 0.2 s.

Figures III.32 and III.33 illustrate the errors introduced in the phasor estimates in terms of magnitude and phase angle respectively. Regarding the magnitude, the errors can reach 2.5% for the two time-domain resampling algorithms whilst they are below 0.25% for the IpDFT method. For phase angle estimation, the backward linear interpolation gives better accuracy with a maximum error introduced equal to about 1%. The duration of these errors is equal to 30 ms for the backward linear interpolation-based solution following the occurrence of the frequency jump. Similarly, the errors last for $(30 + 2\Delta T_0)$ ms for the i-SVA method. Actually, these durations are exactly equal to the transient response times of the frequency estimation algorithms involved (see Fig. III.34). Since the frequency estimates are wrongs during these periods of time and since these same frequencies are used to resample the signals before the DFT is applied, it is clear that the magnitude and

the phase angle will be wrong.

The IpDFT technique is less sensitive to such a phenomenon because the frequency estimation does not form a closed-loop system with the phasor estimation process. The parameters of interest are estimated independently and no interaction exists between them. However, when the system frequency reaches 55 Hz, the errors are higher than those obtained through the time-domain resampling methods.

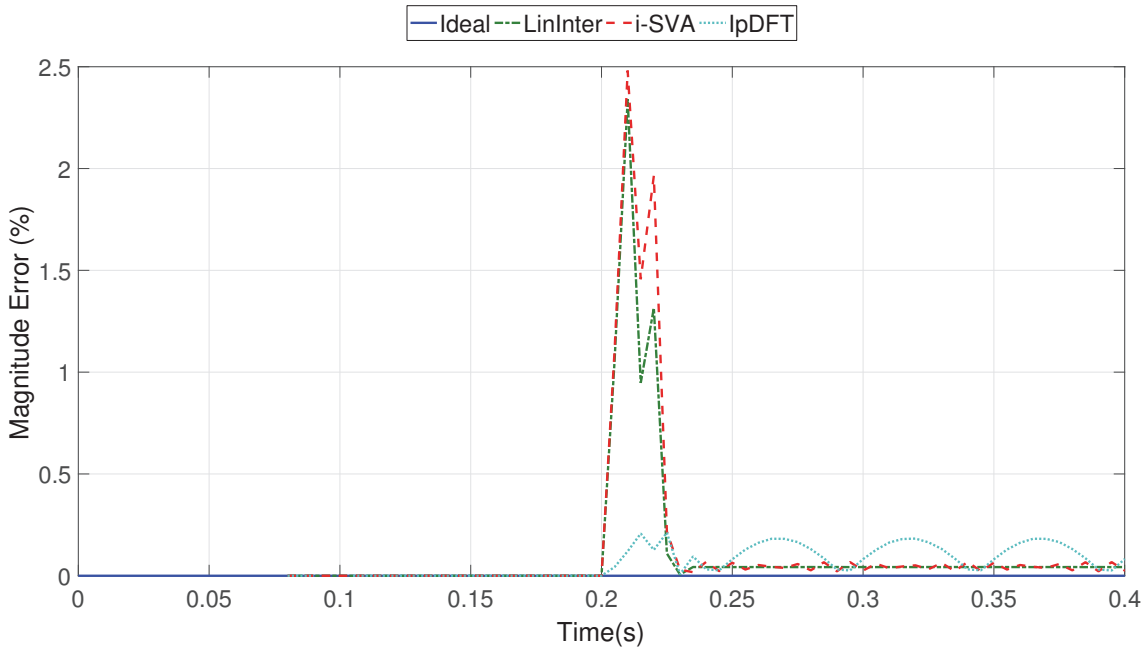

FIGURE III.32 – Magnitude computation response of frequency jump

Furthermore, the response time of the frequency estimation algorithm is exactly equal to the window length considered to perform the measurement as expected. For the linear interpolation, the response time is equal to 1.5 cycles whereas it is equal to 1.5 cycles plus 2 sample time for the i-SVA method. For the IpDFT, the frequency estimation response time is slower since equal to 40 ms (equivalent 2 cycles of nominal frequency considered by the algorithm).

Finally, Fig. III.35 highlights the fact that the simple finite-difference formula that is used to estimate the ROCOF is very sensitive to abrupt changes in frequency as expected.

6 Conclusion

In order to fulfill the third objective of this thesis, in the present chapter, three methods have been first presented to compute phasors with high accuracy on the basis on samples generated by SAMUs. These methods apply equally to each of the input channels of the SAMU considered in Chapter II. Two methods interpolate the signal in the time

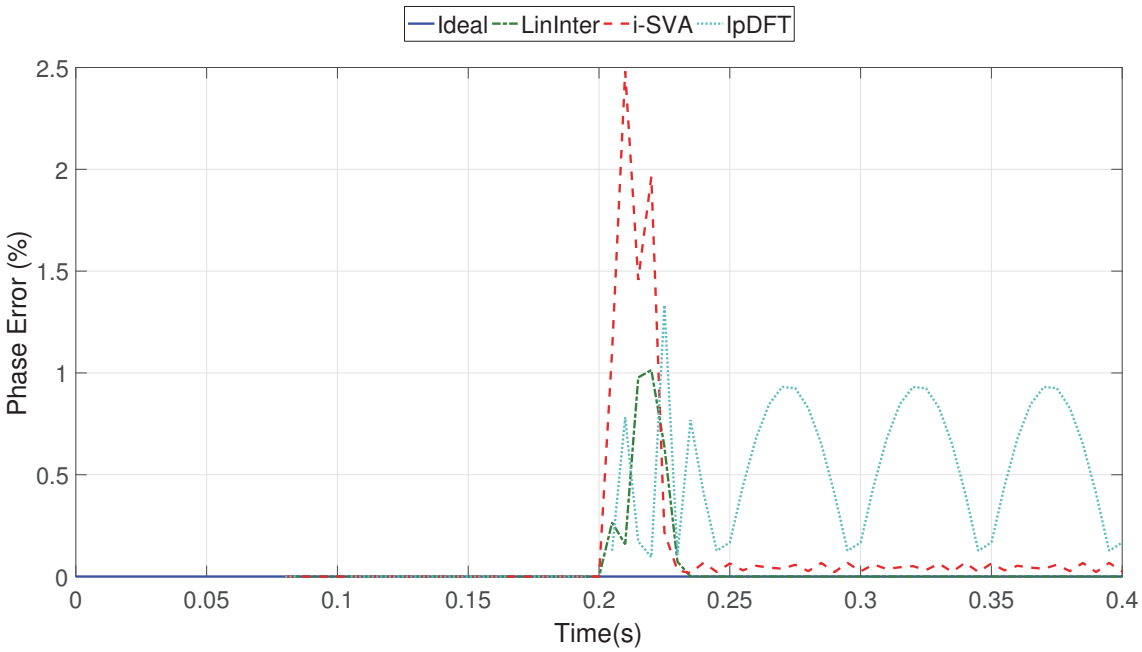

FIGURE III.33 – Phase angle computation response of frequency jump

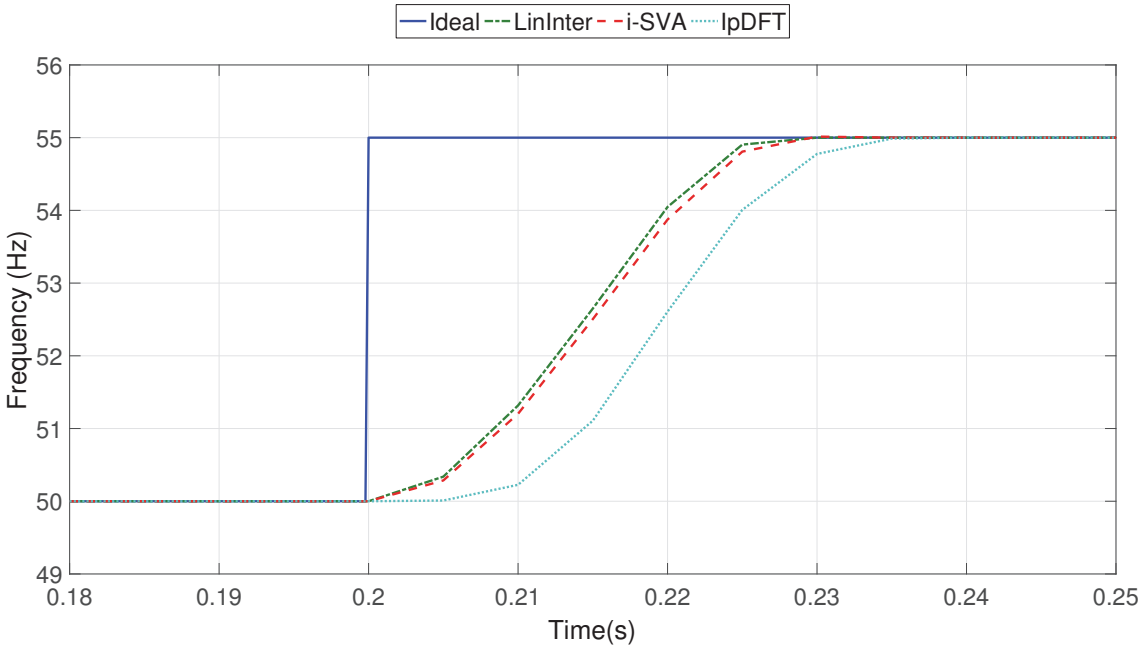

FIGURE III.34 – Frequency computation response of very slow ramp of frequency

domain (i-SVA and backward linear interpolation) whereas the last one interpolates the DFT frequency bins in the frequency domain (IpDFT with Hanning window). Regarding the time domain algorithms, the three-phase voltage channels play an essential role since they are used to design an innovative frequency tracking algorithm which can be applied together with either the i-SVA method or the backward linear interpolation method. This innovative algorithm is able to provide accurate frequency estimates which are further used to compute ROCOF estimates with almost no error under dynamics. This conclusion is in

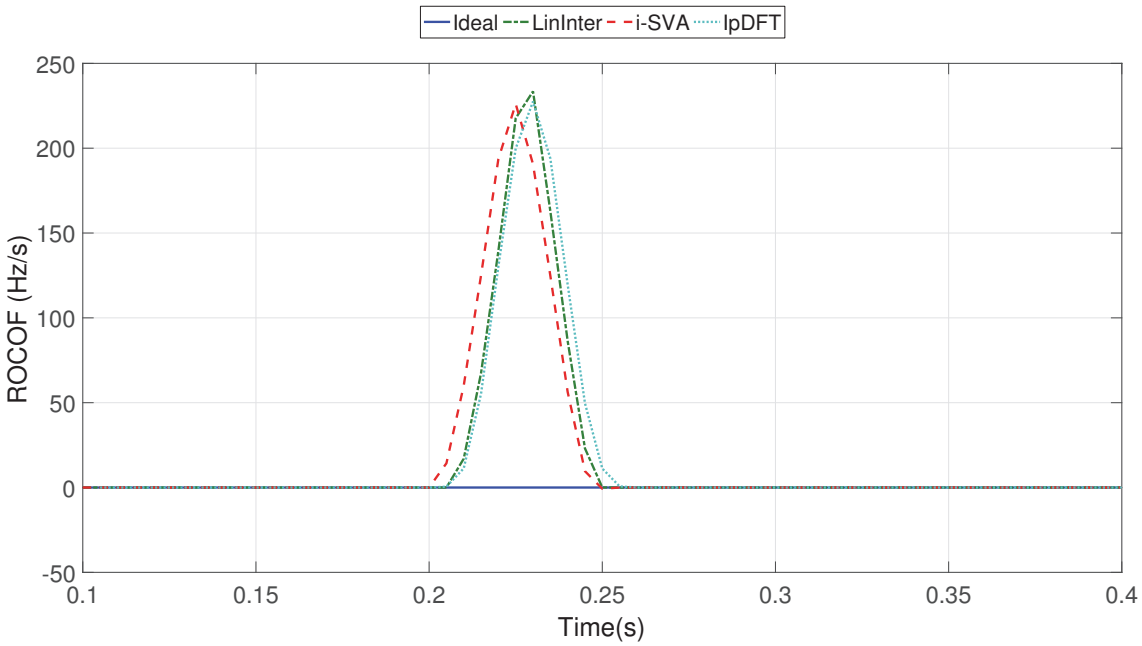

FIGURE III.35 – ROCOF computation response of very slow ramp of frequency

line with the fourth main objective of this thesis. Moreover, the frequency estimates are then used to compute the sampling frequency which is given to the time domain interpolation methods, involved in all input channels, forming a closed-loop system. Conversely, the IpDFT technique operates in open loop and is, in essence, capable of providing frequency estimates.

The three overall solutions are aiming to accurately estimate phasors, frequencies and ROCOFs in static and dynamic conditions. The simulation results show that the backward linear interpolation-based solution outperforms the algorithms based on i-SVA and IpDFT with tapering in terms of accuracy and transient response **for large frequency excursions**. However, when the input signals are distorted by harmonics and subject to small frequency drifts, the i-SVA algorithm gives better accuracy. Nevertheless, in such a configuration, the benefits in terms of accuracy are small. This is the reason why this thesis recommends to use the backward linear interpolation for the future generation of protection relays. Now, the objective is to incorporate a synchronized phasor measurement algorithm into the initial proposed signal processing with minimal computational effort. To do so, the backward linear interpolation algorithm must be the backbone of the work. This is the core objective of the next chapter.

Chapter IV

A computational-efficient synchronized phasor measurement algorithm for protection relays

Contents

Abstract

This chapter presents a new generation of protection relay integrating stand-alone merging units metering accuracy class 0.1 and synchronized phasor measurements. A proposition of signal processing algorithms for such a stand-alone merging unit is first given. Then, the integration of the frequency tracking into such a device subjects to synchronization constraints is then discussed. Afterward, a proposed synchrophasor algorithm with low computational effort is described and integrated into the initial algorithm. The whole solution is finally tested following the test plan imposed by the PMU standard.

1 Introduction

In the previous chapter, phasor, frequency and ROCOF estimates were computed without taking into account of the synchrophasor time-tags, that is these measurements cannot be compared with those performed by other PMUs and PMU-enabled IEDs. Furthermore, it is worth remembering once again that the synchrophasor time-tags must be located at the center of the observation window before estimating the synchrophasors (see Section 7.3 of Chapter I). The latter are thus computed following a different logic from phasors. Therefore, there is a need to design an algorithm dedicated to compute synchrophasors and, in accordance to this thesis objective, this algorithm must be merged into the signal processing defined in Chapter III.

Successful integration of the synchrophasor measurement algorithm can be achieved if running computations for protection functions are coincident with the synchrophasor time-tags. To obtain synchronized measurements, the use of the timestamps coded in the SMV frames is mandatory. Indeed, by correlating the timestamps with a given synchrophasor reporting rate, it is possible to identify the samples including the absolute phase angle information and these samples represent the starting point to enable synchrophasor estimations. In this thesis, the PMU performance class P is considered as it deals with protection applications which require fast time responses. Last but not the least, the design of the PMU algorithm is performed considering a 50 Hz system.

In the light of the above, this chapter is organized as it follows. First, the frequency tracking method described in Section 3 of Chapter III is modified to take into account for the absolute time synchronization issue. This modification is fruitful for the design of the synchrophasor algorithm because it provides accurate frequency and ROCOF estimates and those measurements need to be reported in addition to the synchrophasors. Next, an algorithm minimizing the impact of frequency excursions on synchrophasor estimates is proposed in Section 3. One important characteristic of this algorithm is that it is capable of providing synchrophasors with high reporting rate (200 frames per second), that is twice higher than the maximum reporting rate imposed by the standard for a 50 Hz system frequency. Afterward, Section 4 discusses about emerging trends, related to the use of SMV frames, affecting the latest version of the PMU standard. Finally, in Section 5, the proposed algorithm is tested by simulation following the test cases imposed by the standard for the PMU performance class P.

2 Synchronization of the frequency tracking algorithm to the synchrophasor time-tags

As stated in Section 7.3 of Chapter I, PMUs must provide frequency and ROCOF measurements in addition to synchrophasor estimates. Since the innovative frequency tracking algorithm described in the previous chapter is able to perform such estimations, it is clear, by synchronizing the computations with a given synchrophasor reporting rate, that the frequency and ROCOF estimates obtained can be coincident with the GPS second marker.

This GPS second marker is included in particular SMV frames; those timestamped with SmpCnt = 0x0000. Therefore, when this condition is met, it denotes the starting point from which synchronized phasor measurements, frequency, and ROCOF estimates can be computed. Most importantly, it also represents the instant of time where the frequency tracking algorithm must be executed. Fig. IV.1 shows an example result of the backward linear interpolation and down-sampling algorithm applied to a sine-wave of fundamental frequency at a sample time-stamp coincident with the 1 PPS pulse marker. The several observation windows showed for the frequency tracking algorithm have been drawn in order to make easier the understanding of proposed method.

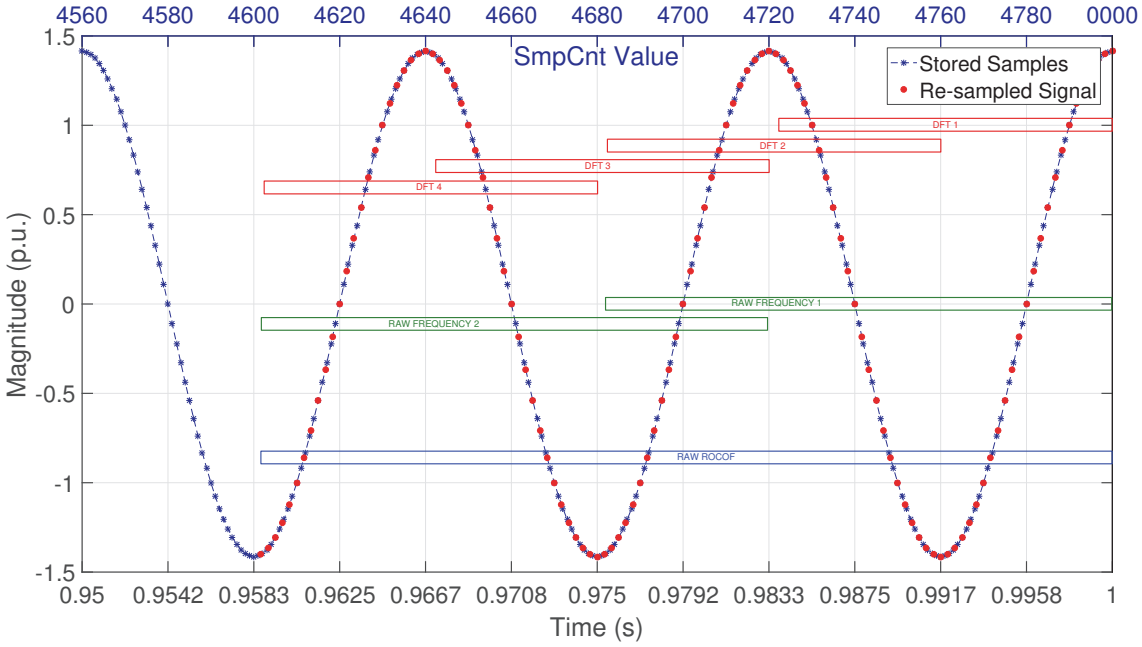

FIGURE IV.1 – Frequency tracking main tasks execution

In Fig. IV.1, DFT 1 and DFT 2 are used to extract the phase angle at SmpCnt = 0000 and SmpCnt = 4752 respectively. Then, the frequency estimate is computed based on the obtained phase angles. Similarly, the angles derived from DFT 3 and DFT 4 are used to compute the second frequency estimate. These 2 frequency measurements, delayed by 96 samples, are then used to compute the ROCOF estimate.

Based on that, the question becomes: when to execute the next measurements with respect to SmpCnt values? To answer this question, let first remind from Section 3.3 of Chapter III that, for a given sine-wave of fundamental frequency, a new value of frequency and ROCOF is computed each quarter of fundamental cycle. This means that the frequency tracking is processed each 1/200 s, that is each 5 ms. The values of SmpCnt corresponding to such an execution cycle are those multiple of 24 since the SMV frames are generated at a sampling frequency of 4,800 Hz. In a nutshell, the frequency tracking algorithm must be executed every 24 samples generated by the SAMU, starting at SmpCnt = 0000.

However, it can be recognized that this execution cycle is not compatible with the reporting rates specified in the PMU standard. Indeed, the highest rate defined is 100 frames per second (fps) for a 50 Hz system (see Table I.1 of Chapter I). Consequently, synchrophasor, frequency and ROCOF estimates must be computed every 10 ms, that is twice slower than the execution cycle of the frequency tracking algorithm. Of course, it is inconceivable to decrease the execution cycle of the frequency tracking algorithm because this will lead to slow down the operating time of the protection functions. Nevertheless, two options are still possible: either a decimation is performed to keep estimates related to the reporting time (1 estimate out of two) or the synchrophasor reporting rate is increased to 200 fps. This second option does not only fill the gap between the frequency tracking execution cycle and the synchrophasor reporting rate but, most importantly, it permits to anticipate future evolution of the standard. Indeed, let us remind that the highest reporting rate imposed by the PMU standard has already evolved in the past to accommodate for growing communication bandwidth while enhancing the observability of the system. For information, the highest reporting rate has doubled between IEEE Standard C37.118.1 and IEC Standard 60255-118-1, from 50 fps to 100 fps. For these reasons, and to be in line with the next generation standard, **this thesis will consider reporting rates of 200 fps.**

The "new" frequency tracking algorithm is based on the backward frequency tracking method presented in Section 3 of Chapter III and integrates the synchronization constraints. The flowchart of the frequency tracking algorithm is given in Fig. IV.2 where new developments are highlighted in yellow.

The input signals consist of the samples of the three-phase voltages plus neutral and three-phase current plus neutral. A circular buffer continuously stores the samples before running the backward interpolation and down-sampling algorithm which can be executed only if two conditions are satisfied.

The first condition is related to the number of samples stored in the buffer. Let us remind from Section 3 of Chapter III that 7,200 samples of three-phase voltages are required to measure an accurate ROCOF value for a 5 Hz input signal. Based on that, if the power system frequency is less than 5 Hz or if the frequency measurement algorithm computes a value below 5 Hz, then a crash program will occur because the retroactive algorithm will require more samples to be stored in order to generate the recomputed 48 s/c signals (see Eq. (III.17) of Chapter III for mathematical proof). To overcome this issue, a low threshold is used and takes the value of 5 Hz. Similarly, a high threshold can be used to avoid the algorithm to track any high frequency values and limits the measurements to the maximum frequency under which the relay shall operates ; 72 Hz in this design. Last but not least, there is no need to store 7,200 samples for the three-phase currents and the neutral signals because they are not used to drive the frequency estimation process. Instead, 960 samples of each of these input channels are necessary to re-compute 1 cycle of a 5 Hz signal. In a nutshell, the circular buffer is full when 12,000 samples are stored.

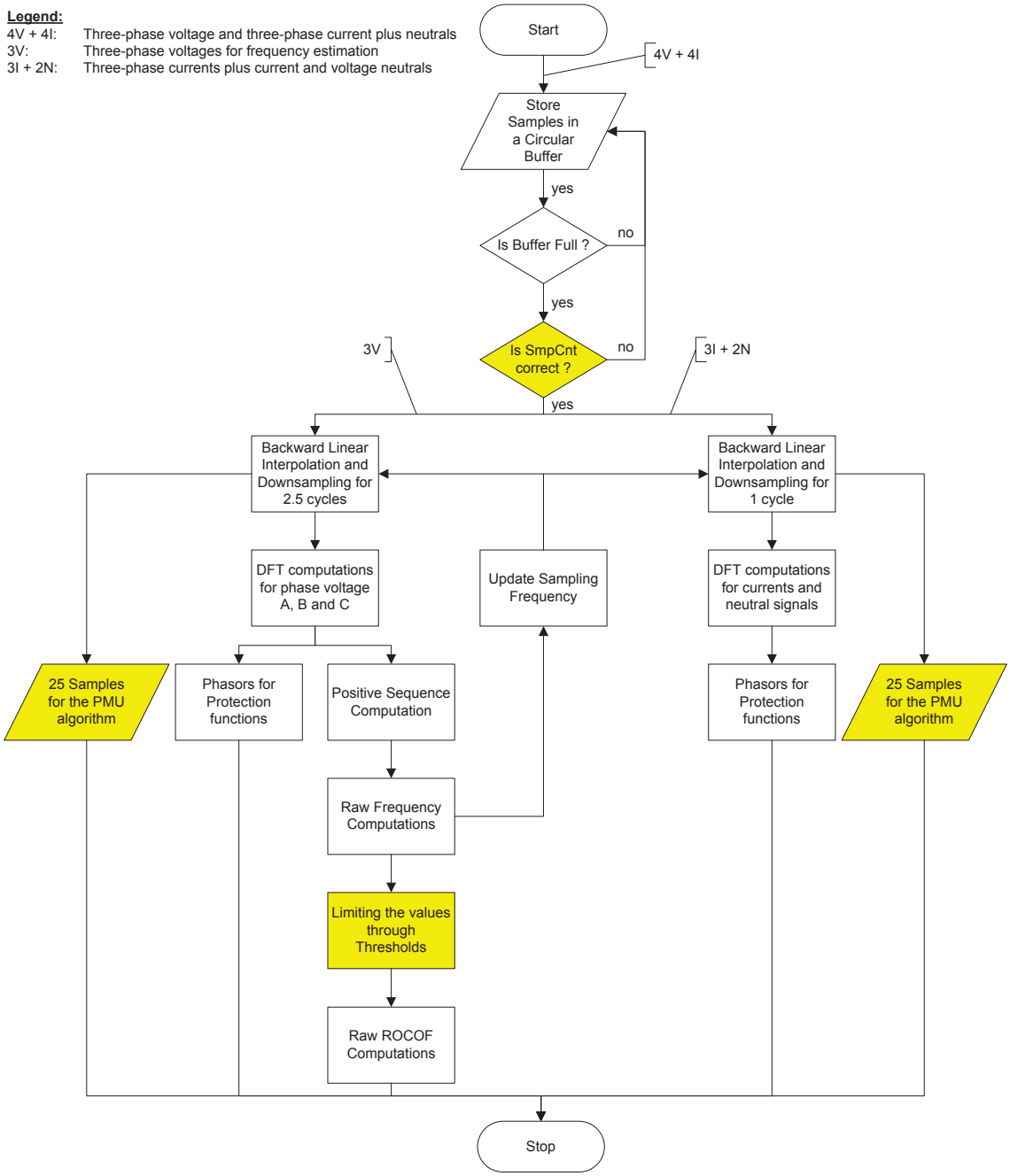

FIGURE IV.2 – Flowchart of the frequency tracking block algorithm

The second condition refers to the value of the counter SmpCnt which has to be coincident with the synchrophasor reporting rate as discussed above. Based on that, the algorithm can be executed. The most important parts are described below.

Each of the eight signals is resampled to a fixed number of samples per power cycle, 48 in this study, through the backward linear interpolation and down-sampling algorithm. So, whatever the power system frequency is, the outputs of the backward algorithm are always 48 s/c signals. Moreover, the interpolation algorithm is applied as function of the nature of the input signals. For voltages, 2.5 cycles (120 samples) must be generated for ROCOF

estimations whereas only 1 cycle is required for other signals to estimate phasors used for protection functions. Regarding the voltages, the DFT denoted 1 (see Fig. IV.1) is not only used by the frequency tracking algorithm but it is also given to protection functions as well. The DFTs are tuned to extract the phase angle information carried by the most recent sample in a given data window. And, since these phase angle are synchronized to the synchrophasor time-tags, they are referenced to the GPS as well (remind that the most recent sample is taken as it is).

Despite the fact that the DFT 1 is able to compute the absolute phase angle, the resulting phasor is not a synchrophasor with respect to the latest version of the PMU standard because the synchrophasor time-tag is located at the end of the data window. This highlights the need for designing a synchrophasor algorithm. This synchrophasor algorithm can be designed by taking advantage of the recomputed samples obtained through the backward linear interpolation technique as shown in Fig. IV.2 where the 25 most recent recomputed samples of each channel are given to the synchrophasor algorithm. This allows the integration of synchronized phasor measurements with minimal processing cost into the signal processing path and tackles the issue of developing a synchrophasor algorithm from scratch.

3 A proposed synchrophasor algorithm merged into the initial signal processing

The idea of the synchrophasor algorithm is to displace the observation window of the DFT 1 in such a way that the synchrophasor time-tag is located at/near the center of that window while keeping the correct phase angle given by the most recent sample. The position of the timestamp in relation to the center depends on the parity of N. If N is an odd integer, then it exists a sample which is exactly at the center of the window and this sample has the synchrophasor time-mark. Conversely, if N is even, a drift of half a sampling period is introduced between the center of the window and the sample timestamped by the synchrophasor time-tag. Furthermore, the less errors are introduced in synchrophasor estimates by timestamping at the center of the observation window. It is thus clear that N should be an odd integer. Based on that, since 25 samples are gathered from the frequency tracking algorithm, 24 samples must be computed so that to fill the right part of the observation window.

To compute the 24 samples, one possibility could be to use a resampling scheme driven by the frequency tracking algorithm because the 25 samples coming from the frequency tracking algorithm are computed synchronously with the power system frequency. By doing this, the 49 samples are always evenly spread out inside the observation window whatever the system frequency is. To reach this target, the “on the fly” linear interpolation and downsampling algorithm is the best option. Indeed, this will lead to obtain a data window composed of samples recomputed on a unique algorithm foundation despite this algorithm is applied either in a retroactive or in a chronological manner. The “on the fly” linear interpolation and downsampling algorithm share some similarities with the one

involved in the algorithmic part of the SAMU metering class 0.1 described in Section 5 of Chapter II. However, instead of computing a 4,800 Hz sample stream on the basis of a 28,800 Hz sampled signal, the algorithm is applied to compute the 24 samples based on the samples available at the SAMU output. Naturally, the samples produced by the SAMU and considered to generate the 24 samples are those timestamped by values above the time-tag of the observation window. Now, to deal with the new PMU standard, the magnitude of the sample exactly at the center of the window shall remain unchanged after the "on the fly" resampling process in order to keep the absolute phase angle information. An example of the method applied on the signal $x(t) = \sqrt{2}\cos(2\pi 45t)$, resampled at a sampling rate of $F_s = 48 \times 45$ Hz, at the synchrophasor time-tag 0.02 s, is shown in Fig. IV.3. In this figure, the magnitude of the sample located at the synchrophasor time-tag remains unchanged while the other 48 samples are generated on the basis of the 4,800 Hz signal.

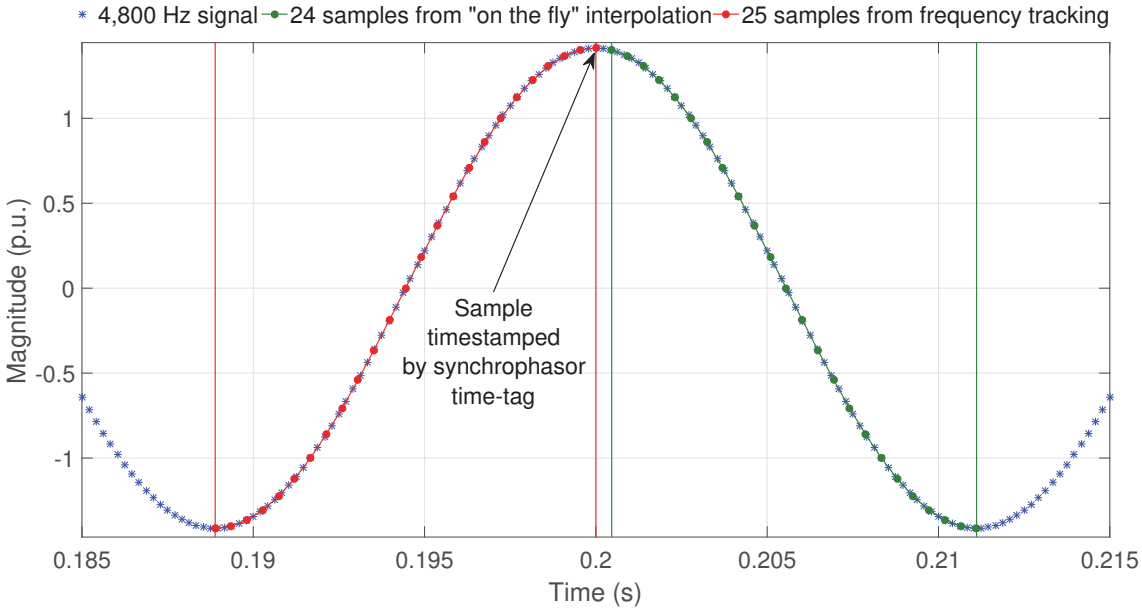

FIGURE IV.3 – Basic idea of the resampling process involved in the synchrophasor algorithm

Now, the challenge becomes to correctly estimate the synchrophasor on the basis of the 49 recomputed samples. Since the observation window is composed of samples which have been generated synchronously with the power system frequency, the DFT algorithm could be applied without a care about the pernicious leakage phenomenon. However, it is not the case because the 49 recomputed samples represents a complete cycle of the power system plus a sample of the next cycle. Hence, a sample must be discarded so that to avoid the leakage effect and perform a 48-points DFT.

Obviously, the possibility of selecting 48 consecutive samples exists but this will lead to waste the advantages of having a sample exactly centered on the window as N will become even is this case. Therefore, in order to perform a 48-points DFT, there is a need for generating 48 equally spaced sample based on the window length of 49 samples while keeping the sample timestamped by the synchrophasor time-tag at the middle of that window as it

is. To do so, the 49 samples are passed through a synchronous linear trigonometric interpolation method. This resampling algorithm is adapted from the theory proposed in [PT08a].

The general idea of the algorithm described in [PT08a] is to perform a linear interpolation between two consecutive samples obtained through **a fixed sample rate locked to the nominal frequency** while taking into account for the sinusoidal shape of the signal. The interpolation method requires the measurement of the prevailed system frequency so that to generate a sequence of samples synchronous with that frequency. The principle of the method is depicted in Fig. IV.4 where the signal $x(t) = \sqrt{2}\cos(2\pi 55t)$, sampled at a rate of 2,400 Hz, is considered.

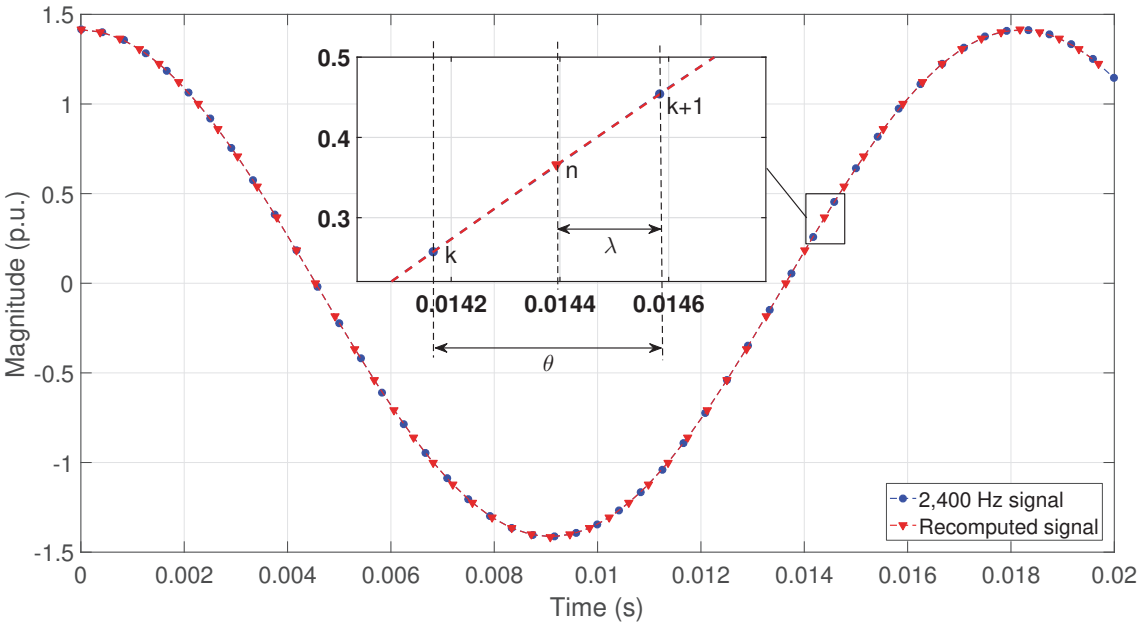

FIGURE IV.4 – Basic idea of the linear trigonometric interpolation method

In Fig. IV.4, the variable θ denotes the sampling interval of nominal frequency while λ represents the time shift between the sample obtained using this sampling interval $(k+1)$ and the one which should be obtained if the clock was locked to the system frequency (n). To compute the sample indexed n, Eq. (IV.1) following must be used [PT08a]:

$$x_n = x_k \times \left[\frac{\sin(\theta - \lambda)}{\sin\theta}\right] + x_{k+1} \times \frac{\sin\lambda}{\sin\theta} \tag{IV.1}$$

where:

x_n	is the recomputed sample indexed n
x_k	is the sample obtained at the sampling index "k"
x_{k+1}	is the sample obtained at the sampling index "$k+1$"
θ	can be expressed as $\theta = \frac{2\pi}{N}$ rad
λ	can be rewritten as $\lambda = \frac{2\pi(f_0 - \Delta f m)}{N f_0}$ rad, with $\Delta f = f_0 - f$ and $m = 0, 1, 2, 3...$

Equation (IV.1) shows that the algorithm requires $N+1$ samples to compute N samples and is therefore suitable for designing the synchrophasor algorithm. Furthermore, since the input signal is supposed to be sampled at a fixed rate locked to the nominal frequency, x_n is related to λ so that to compute a sample set synchronous with the system frequency. However, as shown in Fig. IV.3, the 49 samples generated by the linear interpolation and down-sampling algorithm are already synchronous with the actual system frequency. In this context, there is no need to recompute 48 samples based on the prevailed frequency which means that λ is a constant. Instead, the algorithm is used to keep the sinusoidal shape of the signal while shifting the samples by half a sampling time in a chronological manner in such a way the resulting 48 samples are evenly spread out inside the window. The shifting operation is performed by setting $\lambda = \frac{\theta}{2} = \frac{\pi}{N}$. By doing this, Eq. (IV.1) can be rewritten as it follows:

$$x_n = \frac{\sin(\pi/N)}{\sin(2\pi/N)}(x_k + x_{k+1}) \tag{IV.2}$$

Since N is equal to 48, the coefficient $\frac{\sin(\pi/N)}{\sin(2\pi/N)}$ can be computed off-line and stored in memory so that to ease the implementation of the algorithm and reduce the computational effort. An example of the synchronous linear trigonometric interpolation algorithm applied on the data window illustrated in Fig. IV.3 is depicted below.

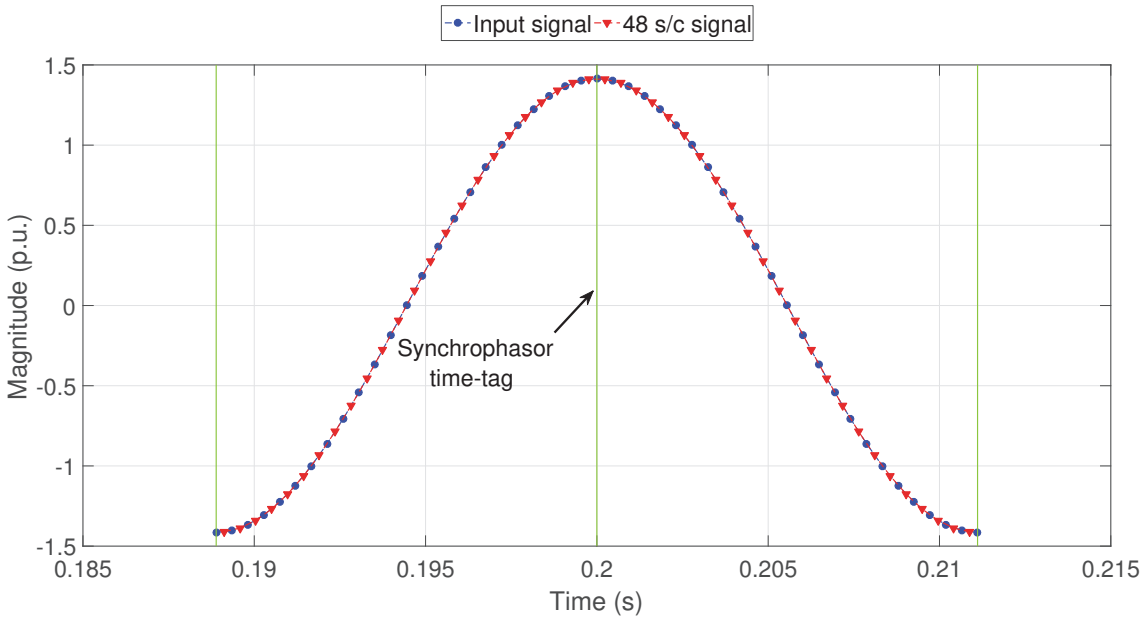

FIGURE IV.5 – Example application of the synchronous linear trigonometric interpolation method

Through Figs. IV.4 and IV.5, it can be concluded that the combination of the two resampling methods enables the computation of a 48 s/c signal synchronous with the power system frequency and perfectly centered around the synchrophasor time-tag. Based on that, the full-cycle DFT algorithm can be applied to estimate the corresponding synchrophasor. The coefficients involved in the DFT formulation have to be adapted to extract the correct phase angle information from the 48 s/c signal. Consequently, the synchrophasor

estimate at a reporting tag T_R is computed as it follows:

$$\overline{X_{T_R}} = \frac{\sqrt{2}}{N} \sum_{n=T_R-\frac{N}{2}}^{T_R+\frac{N}{2}-1} x_n e^{\frac{-j2\pi(n+1/2)}{N}} \tag{IV.3}$$

Equation (IV.3) is applied to the eight input signals of the SAMU metering class 0.1. Afterward, the synchrophasors of the positive sequence component of the voltage and the current signals can be derived through the Fortescue transform. The operations involved in the computation of synchrophasors are depicted in Fig. IV.6.

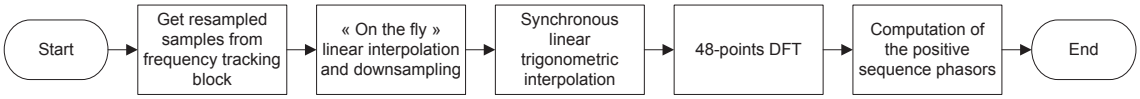

FIGURE IV.6 – Signal processing principle of the PMU algorithm

Another point to discuss concerns the relationship between the modification of the sample rate and the size of the observation window considered to estimate the synchrophasor. To do so, let us first remind from Section 3 of Chapter III that a new sampling frequency is computed each 5 ms by the frequency tracking algorithm. Moreover, since the "on the fly" linear interpolation operation of the PMU algorithm adjusts its sample time according to the most recent sample rate, the sample time changes each 1/200 s. This rate is twice faster than the time required to generate the 24 samples located at the right of the synchrophasor time-tag. Therefore, these 24 samples could be generated with different sample rates, especially during dynamic conditions like ramps of frequency. In this condition, the DFT will wrongly estimate the synchrophasors.

To overcome this issue, it is necessary that only a single sample rate is kept during the computation of the 24 samples. Nevertheless, during the computation of this sample set, another frequency is estimated by the frequency tracking algorithm which means that the new 25 samples computed following a retroactive way have been obtained based on this new frequency. In this light, it is necessary that the "on the fly" algorithm generates a new sample set on the basis of the new frequency as well. This can be done only if another "on the fly" interpolation algorithm is executed in parallel with the first one, each of which uses a different sampling frequency. Last but not least, it is important to highlight that the "on the fly" interpolation process ends when 24 samples are obtained.

Actually, four different sample streams are necessary for the proposed design to avoid overlapping of recomputed samples in the both direction: reverse and forward. Clearly, the interpolation operations are executed sequentially and are driven by the instant when a new frequency is estimated by the frequency tracking algorithm. Since this algorithm is synchronized to the synchrophasor reporting rate through the 1 PPS time-mark, the counter SmpCnt can be used as stimulus to select which one of the four "on the fly" interpolation shall be launched as depicted in Fig. IV.7.

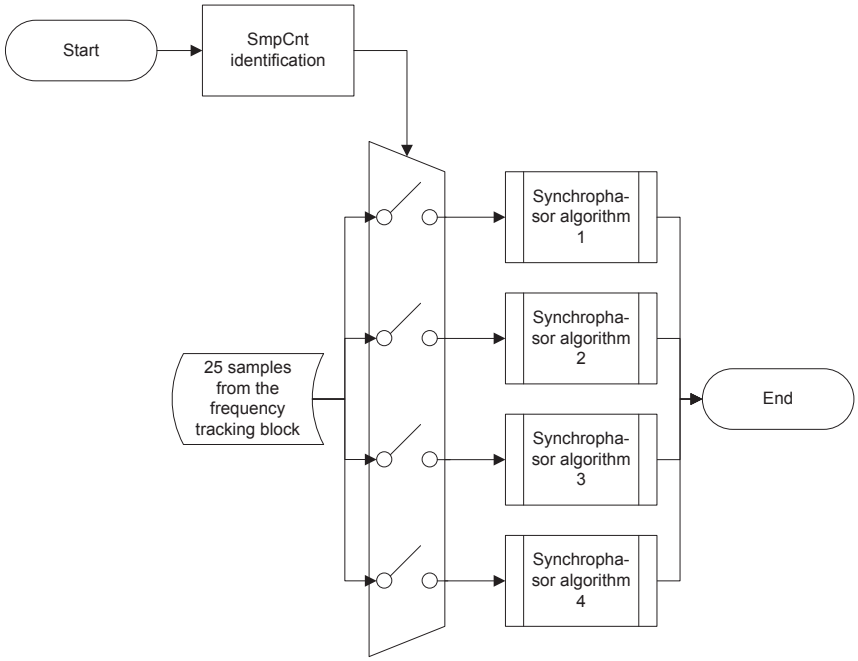

FIGURE IV.7 – Parallelization of synchrophasor estimations

As seen in Fig. IV.7, depending on the value of SmpCnt, the 25 most recent samples generated by the frequency tracking algorithm will be passed through one of the four "Synchrophasor algorithm" processes. These processes are identical in terms of signal processing operations performed and are composed of the blocks described in Fig. IV.6. Based on that, if SmpCnt is equal to 0000, then the first synchrophasor algorithm is executed. The other processes are executed sequentially, from 1 to 4, each time SmpCnt is increased by 20.

The last point to describe concerns the frequency and ROCOF estimates computed through the innovative frequency tracking method. During ramp of frequency conditions, the frequency estimates follow the expected frequency values and the delay introduced is equal to half the window length, that is 15 ms (see Section 5.2 of Chapter III). This means that, for a given instantaneous system frequency at the synchrophasor time-tag T_R, the frequency tracking will measure this instantaneous frequency at $t_f = (T_R + 15)$ ms. Furthermore, for a reporting rate of 200 fps, it can be recognized that 15 ms is exactly equal to $3T_R$. Therefore, as explained previously for synchrophasor estimation, there is also a need to displace the synchrophasor time-tag at the center of the data window used for frequency measurement so that to compensate the tracking error. This compensation is straightforward: instead of reporting the frequency estimated at $t = T_R$, the one obtained at $t_f = 4T_R$ shall be used. Similarly, a ROCOF value estimated at $t = T_R$ must be reported at $t_r = (T_R + 5T_R) = 6T_R$ in order to take into account the response time of the ROCOF estimation algorithm. By doing this, the synchrophasor time-tag will be located at the center of the ROCOF observation window. Delaying the report of values is equivalent to add delays in the PMU reporting latency defined in Eq. (I.63) of Chapter I. As a PMU message must contain the ROCOF estimate, it is clear that $5T_R = 25$ ms must be added to the PMU reporting latency. However, this extra time is consistent with the

standard which allows a maximum latency of 40 ms.

In this section, a synchrophasor algorithm with a high reporting rate and merged to the initial signal processing has been presented. Now, the objective is to validate by simulation the algorithm, using the test cases defined in IEC Standard 60255-118-1. Before that, it is important to discuss emerging trends and evolutions stemming from this PMU standard.

4 IEC Standard 60255-118-1 with Sampled Measured Values consideration

The Technical Committee 95, in charge of the IEC Standard 60255-118-1, is currently working on an informative note to define performance requirements of PMUs having Sampled Measured Values as inputs instead of classical analogue signals. This information note should appear in the Annex S of the IEC Standard 60255-118-1 [rpe15].

PMUs interfacing directly to analogue power system signals incorporate an acquisition chain mainly consisting of interposed transformers, anti-aliasing filters and an ADC. As seen in Section 3 of Chapter I, each of these components introduce errors which are related to the scaling ratio errors, the filter roll-off, and the delays involved during the sampling process. These errors affect mostly the magnitude and the phase angle and therefore the TVE. In addition to these errors, the quantization effect introduces noise which degrades the frequency and ROCOF estimates. Now, if a given PMU uses SMVs as inputs, there is no need for any acquisition chain inside the relay-based PMU which means that the aforementioned errors are not taken into account in this device but apply to the SAMU. Without the front end, the errors introduced on the synchronized phasor measurements only include the algorithmic part of the PMU. Consequently, [rpe15] has proposed to reduce the initial performance requirements which allocate both the front end errors and the signal processing errors. The updated requirements are only applicable for PMUs having SMVs as inputs and consider only the signal processing errors.

Now, to reduce the initial requirements, [rpe15] has identified the contributions of MU and PMU algorithm errors introduced in the TVE, FE, and RFE criteria for each test case imposed by the standard. On the overall, the PMU algorithm is the main source of errors for all steady-state and dynamic tests except for the steady-state off-nominal frequency test. For this specific test, the measurement requirements (TVE, FE, and RFE) have been reduced by a factor of 2 for the whole range of frequency apart from the nominal frequency where the TVE has been decreased to 0.01%. For this specific requirement, [rpe15] explains that most of the PMU algorithms are very precise and contribute to almost no error on the phasor estimates at nominal amplitude and frequency. Finally, concerning the other test cases, the initial performance requirements remain applicable.

5 Tests and assessment based on IEC Standard 60255-118-1

This section presents the simulation and result analysis of P-Class synchrophasor measurements for a power system with 50 Hz nominal frequency. The TVE, FE, and RFE defined in Section 7.3 of Chapter I have been chosen as criteria of assessment to demonstrate the performances of the synchrophasor, frequency, and ROCOF estimation algorithms under both steady-state and dynamic conditions. To do so, the proposed technique has been implemented using the MATLAB environment.

The simulations are carried out following the test cases defined in IEC 60255-118-1 for the reporting rates 200 frames per second. The results are given for the positive sequence voltage which is computed based on the three-phase voltage signals having a magnitude of 1 p.u. When possible, the maximum (MAX), average (AVG), and minimum (MIN) values of the TVE, the FE, and the RFE criteria are reported as requested by the standard. In order to facilitate the interpretation of the results, a unique legend is applicable for the three criteria for all the test plan of the P-Class PMU except for step changes and ramps of frequency test cases. Indeed, for these two specific test cases, the synchrophasor, frequency, and ROCOF estimates can be computed only once each synchrophasor time-tag during the whole simulation duration.

The legend is given below:

where:

Limit	is the threshold imposed by the standard which may be different from one test to another
MAX	is the maximum value computed by the algorithms
AVG	is the average value computed by the algorithms
MIN	is the lowest value computed by the algorithms

Last but not least, the error requirements for compliance with the standard are given progressively for each test case. Moreover, the analogue front end effects of the SAMU metering class 0.1 can be disregarded as they have not been considered in the model. Based on that, the performance requirements for the PMU-enabled protection relay having SMV frames as inputs will be considered in the subsections following.

5.1 Steady-state synchrophasor, frequency, and ROCOF measurement requirements

The steady-state measurement requirements are based on two distinct test cases. The first one covers off-nominal frequencies whereas the second one considers the effect of harmonic distortions. The performance requirements for these two test cases are summarized in Table IV.1.

Table IV.1 – Performance requirements for steady-state conditions

Test Case	**Range of Influence Quantity**	**TVE** (%)	**Max |FE| (Hz)**	**Max |RFE| (Hz/s)**
Frequency Deviation	±2.0 Hz	0.5 0.01 at nominal	0.0025	0.2
Harmonic Distortion	±1% up to 50^{th} harmonic	1	0.005	0.4

5.1.1 Steady-state with off-nominal frequencies

For this test, let us consider the balanced three-phase voltages held at a particular off-nominal frequency, given to the SAMU voltage inputs, be expressed as:

$$V_a(t) = A_1 \cos(2\pi f t) \tag{IV.4}$$

$$V_b(t) = A_1 \cos(2\pi f t - \frac{2\pi}{3}) \tag{IV.5}$$

$$V_c(t) = A_1 \cos(2\pi f t + \frac{2\pi}{3}) \tag{IV.6}$$

where:

A_1 is the magnitude of the fundamental, $A_1 = \sqrt{2}$
f is the off-nominal steady-state frequency, varying from 48 to 52 Hz with a steepness of 0.1 Hz

The tests have been conducted on the whole frequency range described above for a duration of 5 s. The results have been summarized in Fig. IV.8 where the AVG, MIN, and MAX curves are almost perfectly superposed. As shown, the TVE is far away from the limit imposed by the standard on the whole range of off-nominal frequencies with values always below 0.04%. The minimal value obtained occurs at the nominal frequency where the TVE is equal to $4.127 \cdot 10^{-4}$%. Similarly, the worst FE and RFE values computed by the algorithm are respectively $5.67 \cdot 10^{-5}$ Hz and $5.86 \cdot 10^{-3}$ Hz/s.

Clearly, the synchrophasor algorithm is almost insensitive to frequency excursions. The accuracy with which the frequency tracking algorithm is able to estimate the frequency in real-time enables the resampling schemes to correctly recompute the samples. Consequently, the full-cycle DFT-based estimator involves data windows that contain exactly 1 cycle of data which means that leakage phenomenon is avoided.

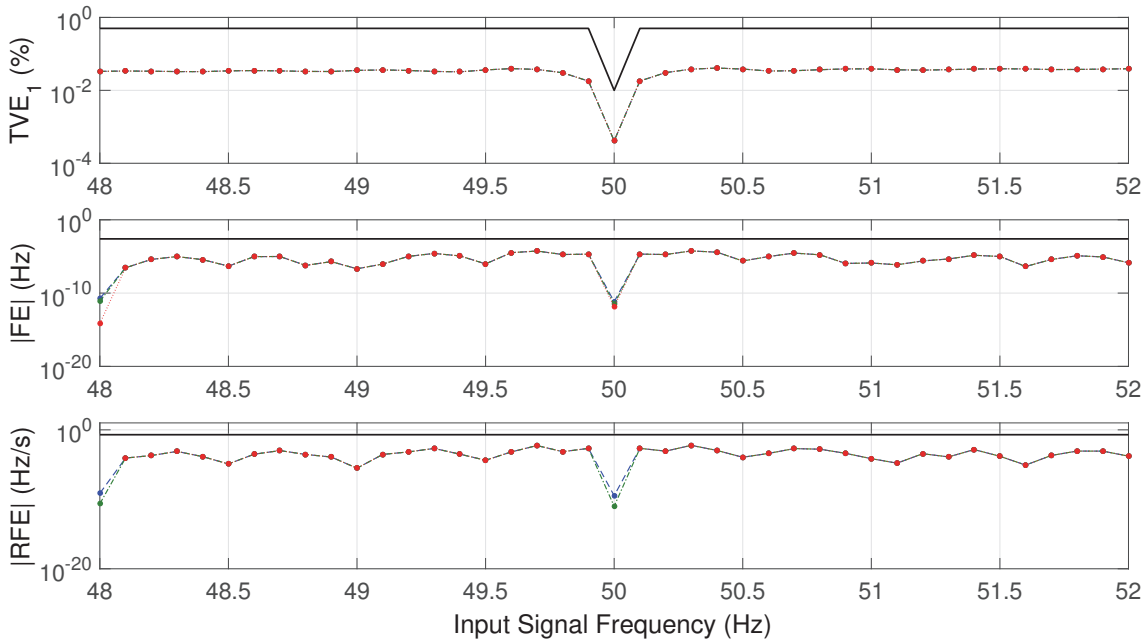

FIGURE IV.8 – Frequency deviation test results for a 50 Hz system

5.1.2 Steady-state with harmonic distortions

A balanced three-phase voltages of nominal frequency corrupted with a single harmonic component can be written as:

$$V_a(t) = A_1 \cos(2\pi f_0 t) + A_m \cos(2\pi m f_0 t) \tag{IV.7}$$

$$V_b(t) = A_1 \cos(2\pi f_0 t - \frac{2\pi}{3}) + A_m \cos(2\pi m f_0 t - \frac{2\pi}{3}) \tag{IV.8}$$

$$V_c(t) = A_1 \cos(2\pi f_0 t + \frac{2\pi}{3}) + A_m \cos(2\pi m f_0 t + \frac{2\pi}{3}) \tag{IV.9}$$

where:

A_1	is the magnitude of the fundamental, $A_1 = \sqrt{2}$
f_0	is the nominal frequency, $f_0 = 50$ Hz
A_m	is the magnitude of the m^{th} harmonic component, $A_m = 1\% \cdot A_1$
m	is the harmonic order, ranging from the 2^{nd} to the 50^{th} harmonic

The results are shown in Fig. IV.9 for a simulation duration of 5 s. Clearly, the estimates never cross the standardized threshold which means that compliance with harmonic distortions for P-Class PMU is confirmed. The TVE is almost 0% on the whole harmonic range except for the 49^{th} harmonic where it is around 0.052%. This harmonic corresponds to the frequency 2,450 Hz which will alias on the negative frequency -50 Hz, that is exactly where the main lobe of the DFT spectrum is located in the negative side. This means that the DFT is not able to reject this harmonic. Among the filters designed, the 8 order FIR filter defined in Section 2.1 of Chapter III is the only filter capable of providing a significant attenuation of 25.72 dB, that is a gain of about 0.052, at 2,450 Hz. In a nutshell, the magnitude of the 49^{th} harmonic is multiplied by 0.052 which matches with the TVE

value obtained at 2,450 Hz.

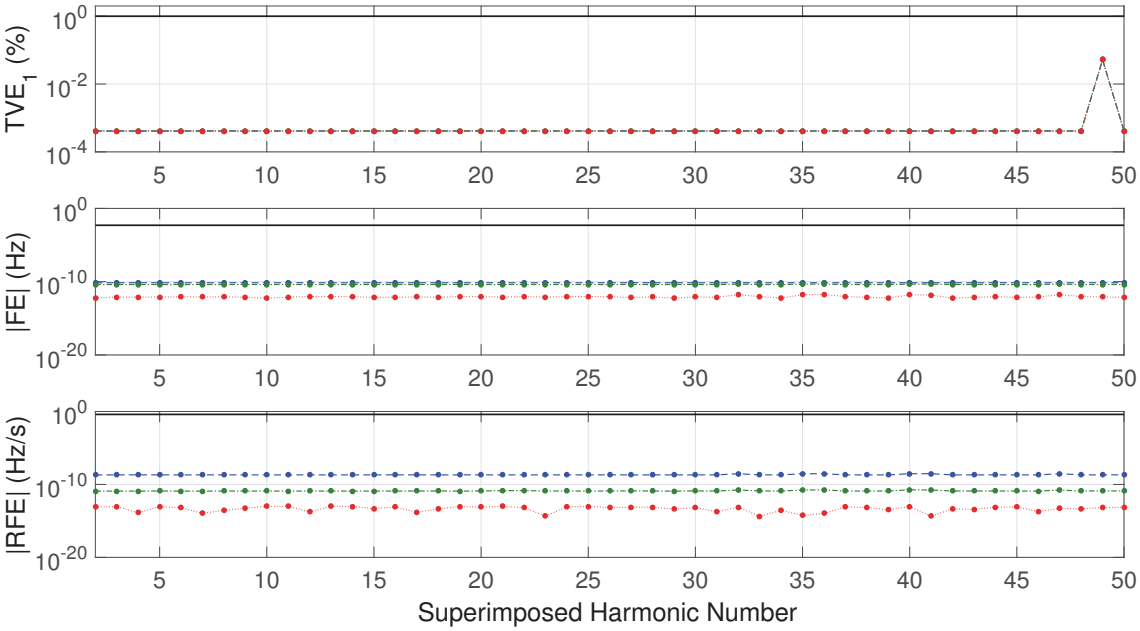

FIGURE IV.9 – Harmonic test results for a 50 Hz system

It can be recognized that, despite the fact the 47^{th} harmonic (2,350 Hz) is not rejected by the 48-points DFT filter by essence, it does not alias on the 50 Hz component as it should be. Otherwise, a spike would also appear at the 47^{th} harmonic in Fig. IV.9. Actually, this specific harmonic is part of the negative sequence harmonics and, as a consequence, does not appear on the positive sequence component. This is the reason why the TVE remains very low when the fundamental is superimposed with the 47^{th} harmonic.

Finally, FE and RFE and very near 0 Hz and 0 Hz/s respectively, demonstrating the performance of the algorithm to deal with harmonics.

5.2 Dynamic synchrophasor, frequency, and ROCOF measurement requirements

Dynamic compliance with IEC Standard 60255-118-1 is based on three distinct test programs to carry out: measurement bandwidth, ramp of system frequency, step changes in phase and magnitude. Concerning the first two points, synchrophasor, frequency, and ROCOF estimates must be below the standardized limits which are listed in Table IV.2. For the step change test scenarios, specific requests shall be achieved and will be reported in Section 5.2.3 where simulation results are given.

5.2.1 Measurement bandwidth

The balanced three-phase voltages are swept with sinusoidal amplitude and phase modulation for a duration of three full cycles of modulation. Mathematically, the input

Table IV.2 – Measurement bandwidth and ramps of frequency requirements as per IEC Standard 60255-118-1

Test Case	**Range of Influence Quantity**	**TVE** (%)	**Max |FE| (Hz)**	**Max |RFE| (Hz/s)**
Magnitude Modulation (Bandwidth)	Modulation level: 0.1 p.u. Modulation frequency: $[0.1 - 2]$ Hz in steps of 0.1 Hz	3	0.06	2.3
Phase Modulation (Bandwidth)	Modulation level: 0.1 rad Modulation frequency: $[0.1 - 2]$ Hz in steps of 0.1 Hz	3	0.06	2.3
Positive & Negative Ramps of Frequency	Rate of frequency: ± 0.1 Hz/s	1	0.01	0.4

signals may be represented by:

$$V_a(t) = A_1 \cdot (1 + k_m \cos(2\pi f_M t)) \cdot \cos(2\pi f_0 t + k_a \cos(2\pi f_M t - \pi)) \tag{IV.10}$$

$$V_b(t) = A_1 \cdot (1 + k_m \cos(2\pi f_M t)) \cdot \cos(2\pi f_0 t - \frac{2\pi}{3} + k_a \cos(2\pi f_M t - \pi)) \tag{IV.11}$$

$$V_c(t) = A_1 \cdot (1 + k_m \cos(2\pi f_M t)) \cdot \cos(2\pi f_0 t + \frac{2\pi}{3} + k_a \cos(2\pi f_M t - \pi)) \tag{IV.12}$$

where:

A_1 is the magnitude of the fundamental, $A_1 = \sqrt{2}$
f_M is the modulation frequency in Hz
k_m is the magnitude modulation factor
k_a is the phase angle modulation factor

With respect to the standard, the amplitude and phase modulation tests are performed separately, which means that the modulation signal shall contain either the amplitude factor or the phase factor. As the modulation frequency varies from 0.1 Hz to 2 Hz in steps of 0.1 Hz, the duration of the simulation varies also from 30 s to 1.5 s. A settling time of 1 cycle of modulation has been considered to make sure that synchrophasor, frequency and ROCOF estimates are measured without taking into account for the transient effects that occurs when the modulation is applied. In these specific test cases, the errors allowed by the standard are high compared to those in steady-state or even during ramps of frequency. This is due to the fact that the measurements follow the modulated signal and therefore represent the combined effect of the fundamental signal and the modulation. The simulation results are depicted in Figs. IV.10 and IV.11 for magnitude modulation and phase angle modulation respectively.

The simulation results are satisfactory as the estimates are below the standardized thresholds. The worst cases occur when the input signal is modulated with a modulation frequency of 2 Hz. Nevertheless, the synchrophasor algorithm is less sensitive to phase modulation than to amplitude modulation. Conversely, the frequency and ROCOF estimates

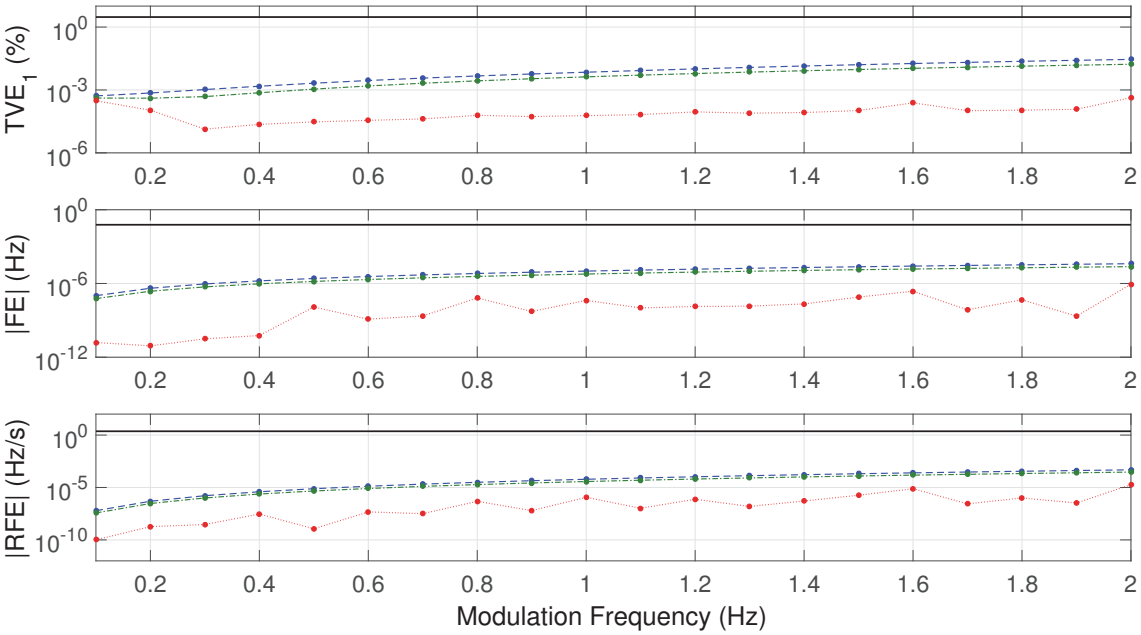

FIGURE IV.10 – Amplitude modulation test results for a 50 Hz system

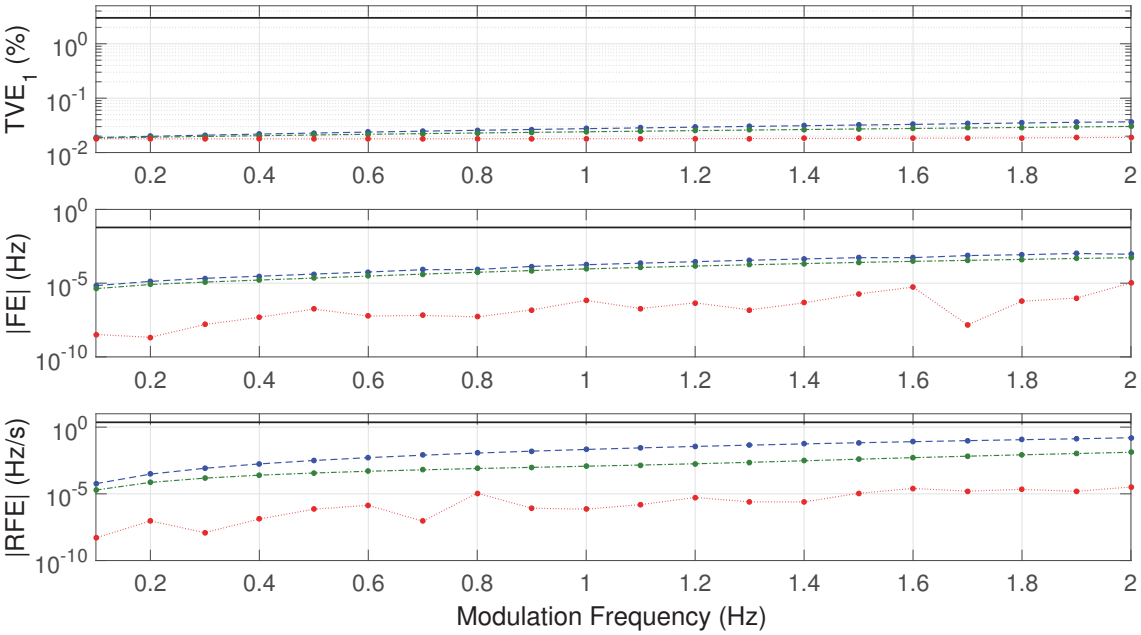

FIGURE IV.11 – Phase modulation test results for a 50 Hz system

are more sensitive to phase modulation, especially regarding the ROCOF measurements. As the absolute phase angle, backbone data of the frequency and ROCOF estimation algorithms, is affected by the modulation factor, it is clear that this will tend to degrade the accuracy of these two algorithms.

5.2.2 Ramps of frequency

In accordance with the PMU standard, the ramp of frequency test scenarios shall be carried out in a specific way. The balanced three-phase voltage system is initially generated at a frequency of 48 Hz and lasts for 0.5 s. Then, a linear ramp rate of 1.0 Hz/s is applied for a duration of 4 s until the frequency reaches the value 52 Hz and remains at this frequency for 0.5 s. Equally, for the negative ramp test, the frequency is initially set to 52 Hz, a linear ramp rate of -1.0 Hz/s is then applied until the frequency reaches the value 48 Hz. Furthermore, the standard defined an exclusion interval during which measurements shall be excluded. This exclusion interval is "the time interval after the ramp leaves or before the ramp reaches a frequency range limit or a point where ROCOF changes" [IEC15]. It is used to prevent wrong estimations performed when the ROCOF is applied from being considered to determine compliance. The exclusion interval $t_{exclusion}$, expressed in second, is computed for P-Class PMU as it follows:

$$t_{exclusion} = \frac{2}{F_R} \tag{IV.13}$$

where:

F_R is the reporting rate, in frames per second

Based on Eq. (IV.13), for a reporting rate of 200 fps, the exclusion interval is 10 ms which means that all measurements performed below 0.51 s and above 4.49 s are disregarded. The simulation results for ramps of frequency are given in Figs. IV.12 and IV.13. Let us remind that, as the frequency is constantly changing and the estimates have to be given at specific instant of time, only 1 measurement can be performed at a given reporting rate. Consequently, it is not possible in this configuration to report the maximum, average, and minimum values of the measurements.

As expected, Figs. IV.12 and IV.13 depict very good measurement accuracy for each of the parameter of interest. The robustness of the frequency tracking algorithm in efficiently dealing with positive and negative ramps of frequency enables accurate synchrophasor and ROCOF measurements. The TVE values are all below 0.08% during the range $[0.51 - 4.49]$ s. Equally, the maximum FE value obtained is approximately 0.77 mHz while the worst RFE value is about 0.061 Hz/s.

5.2.3 Step changes in magnitude and phase angle

In contrast with the previous dynamic tests, the test cases related to step changes in magnitude and phase angle phenomena are aimed at measuring the specific metrics following:

— the synchrophasor, frequency, and ROCOF response times
— the synchrophasor delay time
— the synchrophasor maximum overshoots and undershoots

Table IV.3 gives the synchrophasor performance requirements for input step changes. Equally, Table IV.4 lists the requirements for frequency and ROCOF estimates. The standard imposes both positive and negative step changes. However, in this thesis, only the

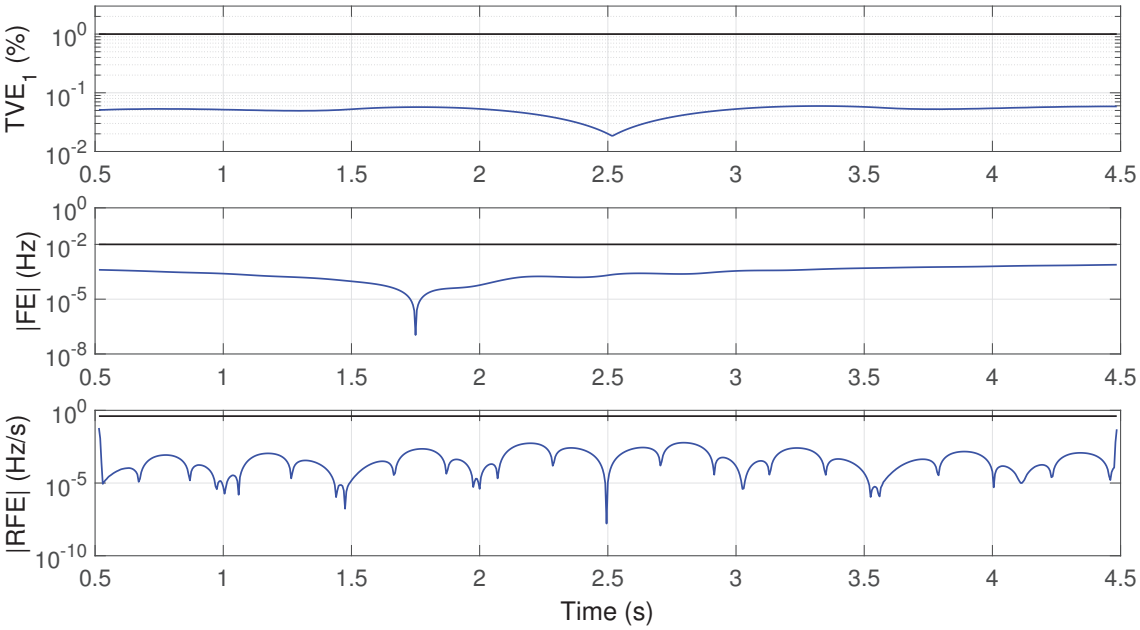

FIGURE IV.12 – Positive ramp test results for a 50 Hz system

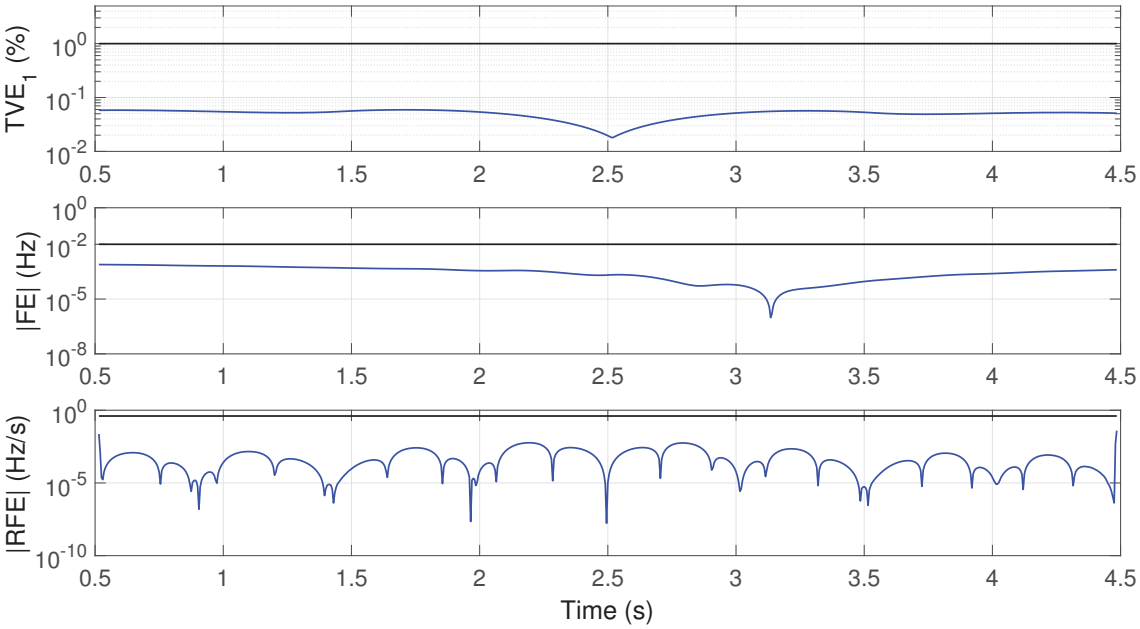

FIGURE IV.13 – Negative ramp test results for a 50 Hz system

results related to positive step changes are presented as the results obtained through simulations for both cases share similarities.

Table IV.3 – Synchrophasor performance requirements for input step change test scenarios [IEC15]

Test Case	Range of Influence Quantity	Response Time (ms)	|Delay Time| (ms)	Max Overshoot/ Undershoot
Step Change in Magnitude	Step Value: 0.1 p.u.	40	1.25	0.005 p.u.
Step Change in Phase angle	Step Value: 10 degrees	40	1.25	0.5 degrees

Table IV.4 – Frequency and ROCOF performance requirements for input step change test scenarios [IEC15]

Test Case	Frequency Response time (ms)	ROCOF Response time (ms)
Step Change in Magnitude	90	120
Step Change in Phase angle	90	120

Let us consider the balanced three-phase voltage system subjects to step changes applied to the SAMU voltage inputs be expressed as:

$$V_a(t) = A_1 \cdot (1 + k_m u(t)) \cdot \cos(2\pi f_0 t + k_a u(t)) \tag{IV.14}$$

$$V_b(t) = A_1 \cdot (1 + k_m u(t)) \cdot \cos(2\pi f_0 t - \frac{2\pi}{3} + k_a u(t)) \tag{IV.15}$$

$$V_c(t) = A_1 \cdot (1 + k_m u(t)) \cdot \cos(2\pi f_0 t + \frac{2\pi}{3} + k_a u(t)) \tag{IV.16}$$

where:

$u(t)$	is a unit step function
k_m	is the magnitude step size
k_a	is the phase angle step size

Figure IV.14 gives the simulation results obtained for the step change in magnitude, applied at $t = 0$ s, and is used to determine the synchrophasor algorithm maximum pre- and post-transition overshoots, minimum pre- and post-transition undershoots as well as the delay time. To do so, several definitions must be fist given:

The pre-transition period is the period of time before t_{pre}.

***t*$_{pre}$** is the instant of time at which the waveform last crosses the initial state level's upper state boundary.

The post-transition period is the period of time after t_{post}.

***t*$_{post}$** is the instant of time at which the waveform first crosses the final state level's lower state boundary.

The maximum pre- and post-transition overshoots are the maximum values above the upper state boundaries reached during the pre- and post-transition periods respectively.

The minimum pre- and post-transition undershoots are the maximum values above the lower state boundaries reached during the pre- and post-transition periods respectively.

The delay time is the time difference between the instant of time the step change is applied and the instant of time the estimate reaches a value which is half way between the initial and final steady state values.

On the basis of these definitions, it is clear that the synchrophasor magnitude estimates neither overshoot nor undershoot the ±0.005 p.u. limits imposed by the standard. Furthermore, the delay time is about 80 μs which is more that 15 times below that the maximum tolerated delay time of 1.25 ms. As the delay time obtained is very near zero, it can be concluded that the timetag is located very closed to the center of the observation window and that the filtering system group delay is properly compensated.

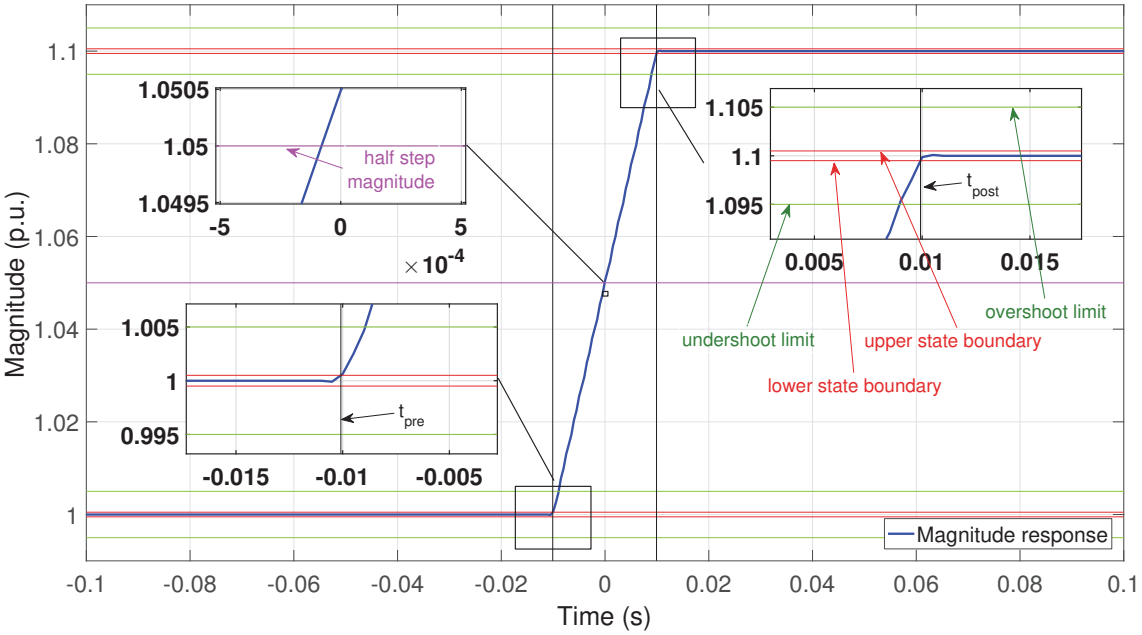

FIGURE IV.14 – Magnitude step change test result - Determination of the synchrophasor algorithm delay time and maximum overshoot and undershoot

To determine the response times of the algorithms, the standard imposes to use the steady-state error limits 1% TVE, 0.005 Hz |FE|, and 0.4 Hz/s |RFE|. As shown in Fig. IV.15, the synchrophasor algorithm response time is about 15.97 ms, that is more than twice lower than the 40 ms standardized limit. This result can be explained by reminding that the response time of the synchrophasor algorithm is the summation of the response time of the full-cycle DFT estimator (20 ms) and the one of the 8 order FIR filter (about 1.67 ms) used before the backward linear interpolation process (see Section 2.1). Based on that, as the 1% TVE threshold is involved, less than 21.67 ms are considered for determining the response time as shown in Fig. IV.15. Finally, it can be observed that the TVE response represents a spike-shaped waveform. This is due to the fact that, when the step occurs, there is a series of observation windows which contain samples before and after the step. Since the window is sliding, that window will progressively contain more

samples after the step, increasing the error introduced in the TVE. The maximum error occurs at $t = 0$ s, that is when the window contains as many samples before as after the step.

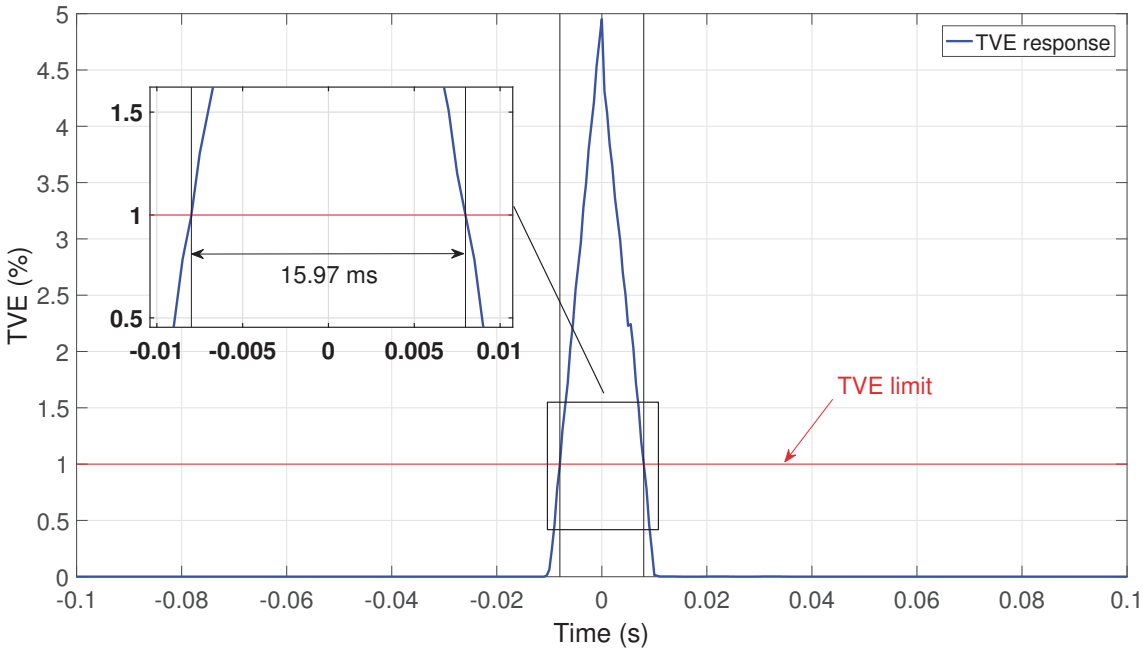

FIGURE IV.15 – Magnitude step change test result - Determination of the synchrophasor algorithm response time

Figures IV.16 and IV.17. Due to the very small values obtained for frequency and ROCOF errors, it is not possible to use the standardized thresholds 0.005 Hz |FE| and 0.4 Hz/s |RFE| for determining the frequency and ROCOF estimation algorithms response times. Instead, these response times are obtained by measuring the interval of time delimited by those instants of time at which the estimates leave the "zero error". The values obtained illustrate the robustness of the methods in case of magnitude steps. Furthermore, the response times are about 31.5 ms and about 51.5 ms for the frequency and ROCOF measurement algorithms respectively. These values are consistent with the response times of the 8 order FIR filter (1.67 ms), the frequency estimation method (30 ms as explained in Section 5.4) and the ROCOF measurement algorithm (50 ms as shown in Section 5.2).

Similar studies are now made for the positive phase angle step change. Figure IV.18 depicts the simulation result for determining the pre- and post-transitional overshoots and undershoots and the delay time. Here also, there is neither overshoot nor undershoot and the DFT-based algorithm is able to provide the exact phase angle information following the step that occurs at $t = 0$ s. Regarding the delay time, the conclusions to be drawn are the same as those given for the magnitude step test case because this delay time is equal to approximately 29.4 μs.

Figure IV.19 illustrates the response time of the synchrophasor algorithm which is equal to approximately to 18.83 ms. Equally, Figs. IV.20 and IV.21 are plotted to determine the

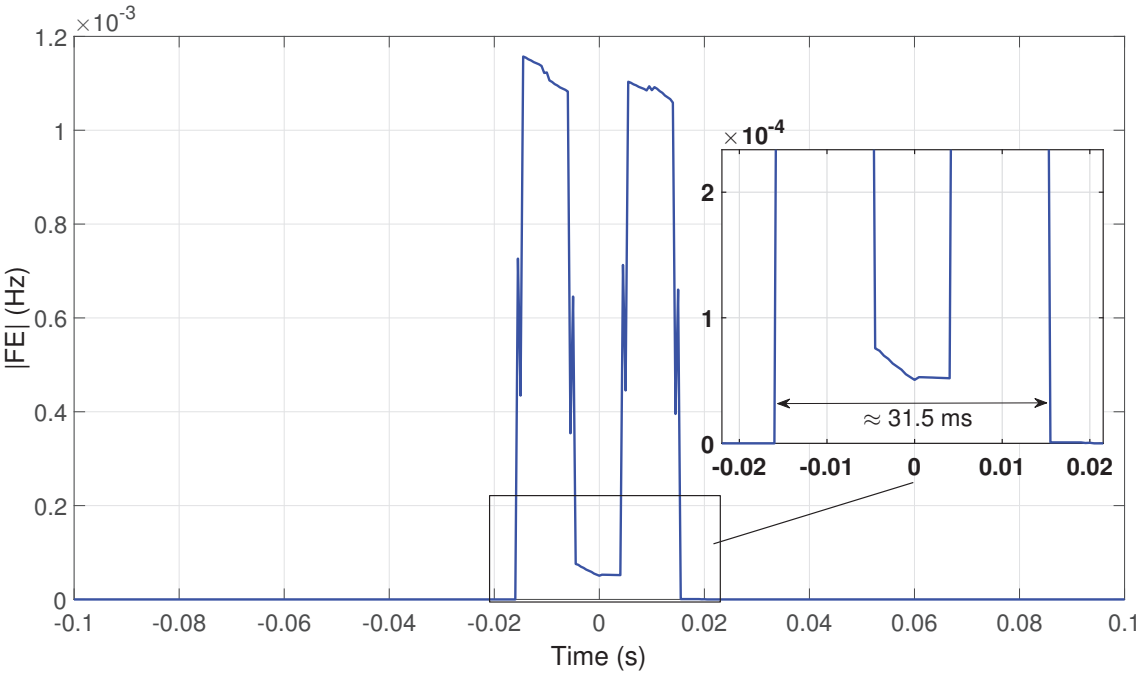

FIGURE IV.16 – Magnitude step change test result - Determination of the frequency algorithm response time

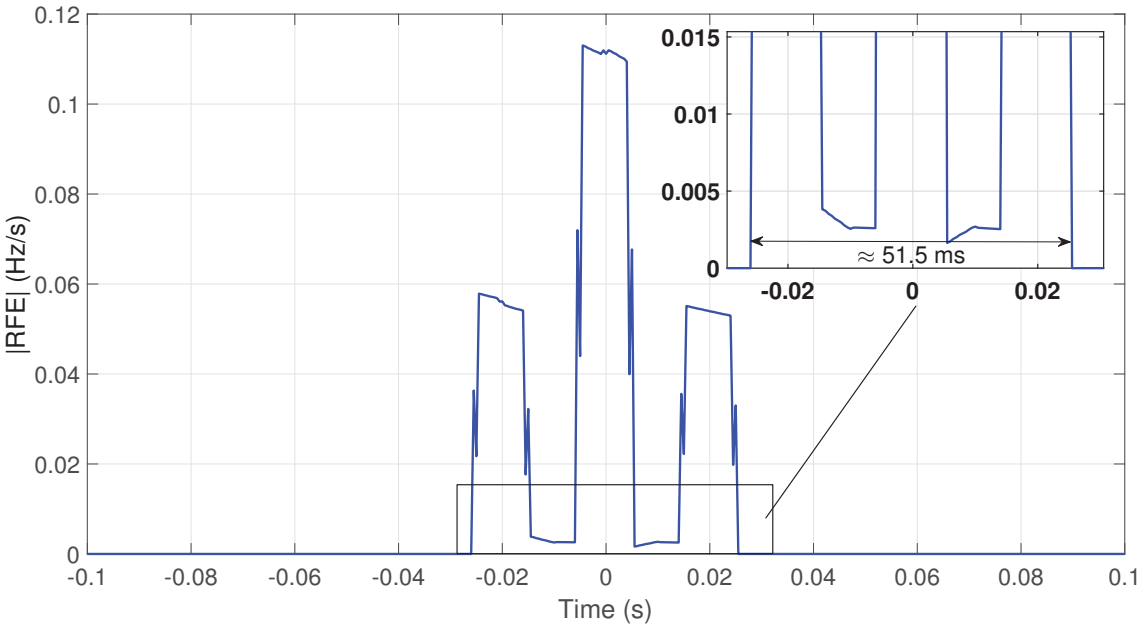

FIGURE IV.17 – Magnitude step change test result - Determination of the ROCOF algorithm response time

response time of the frequency and ROCOF estimation algorithms which are of about 29.9 ms and 50.4 ms respectively. In contrast to the magnitude test case, the estimates cross their standardized thresholds in all cases which means that these limits are involved to determine the three response times. Clearly, with respect to Tables IV.3 and IV.4, compliance with the standard is confirmed in this case as well.

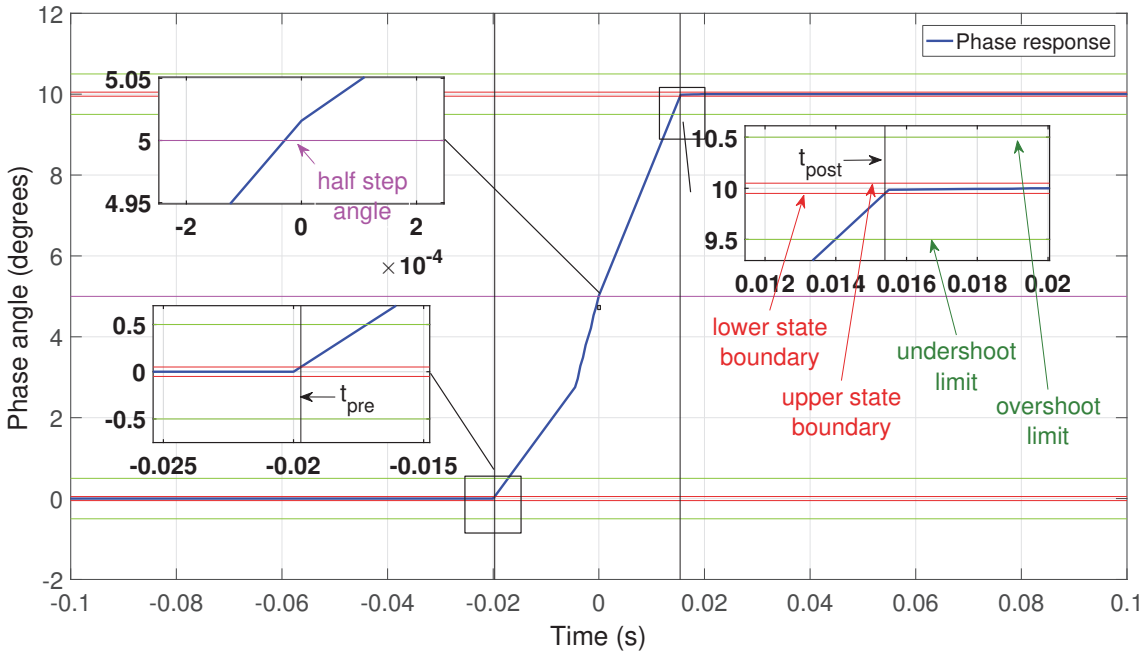

FIGURE IV.18 – Phase angle step change test result - Determination of the synchrophasor algorithm delay time and maximum overshoot and undershoot

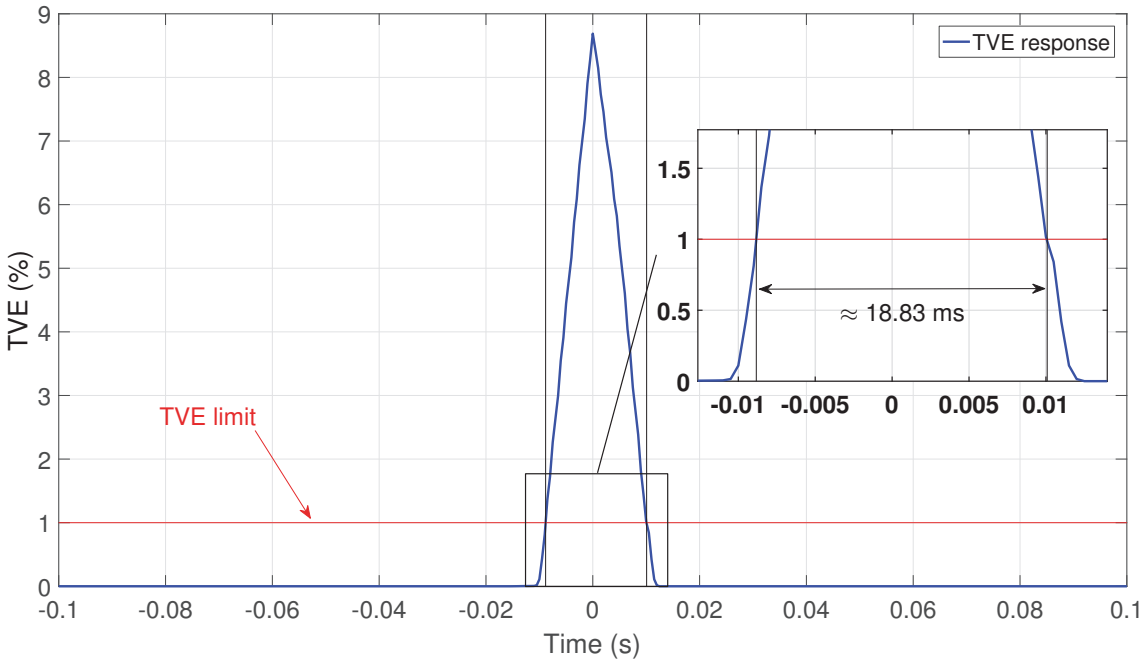

FIGURE IV.19 – Phase step change test result - Determination of the synchrophasor algorithm response time

An interesting point to highlight is that the proposed algorithms are sensitive to step change in phase angle. Particularly, the ROCOF estimation algorithm computes values that can reach 70 Hz/s. Theoretically, the value of the derivative of such a step function

is infinity at the instant of time at which the step occurs. Based on this, let us remind that the methods employed to estimate the frequency and the ROCOF are based on the derivative of the phase angle (see Eq. (I.54)) and the derivative of the frequency (see Eq. (III.19)) respectively. This explains the high values obtained.

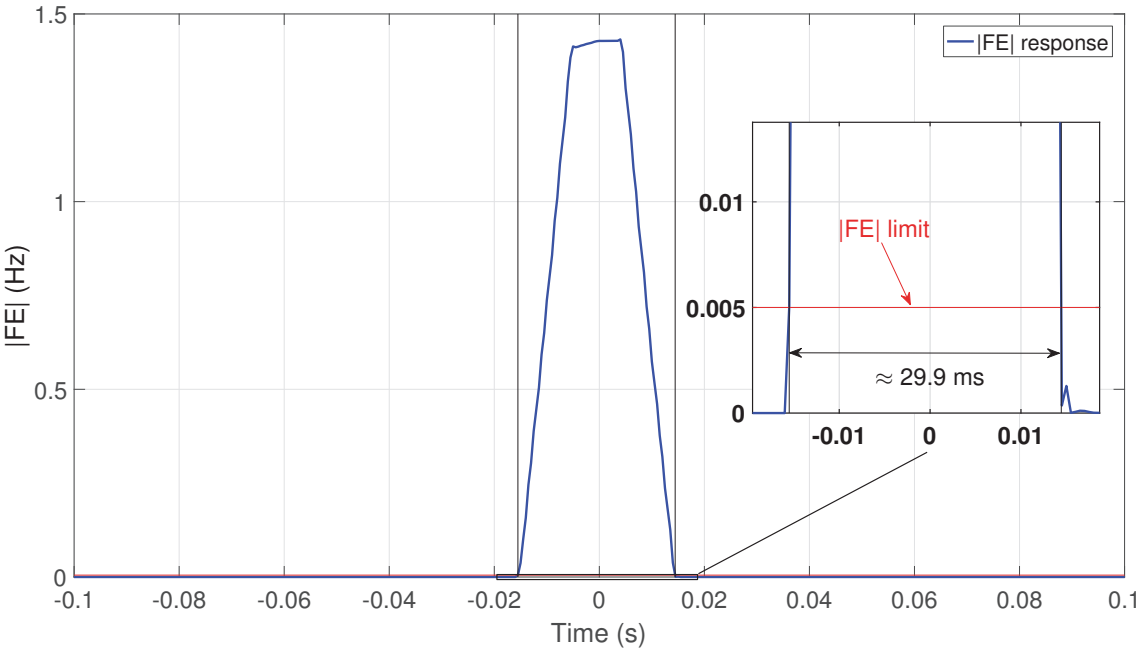

FIGURE IV.20 – Phase step change test result - Determination of the frequency algorithm response time

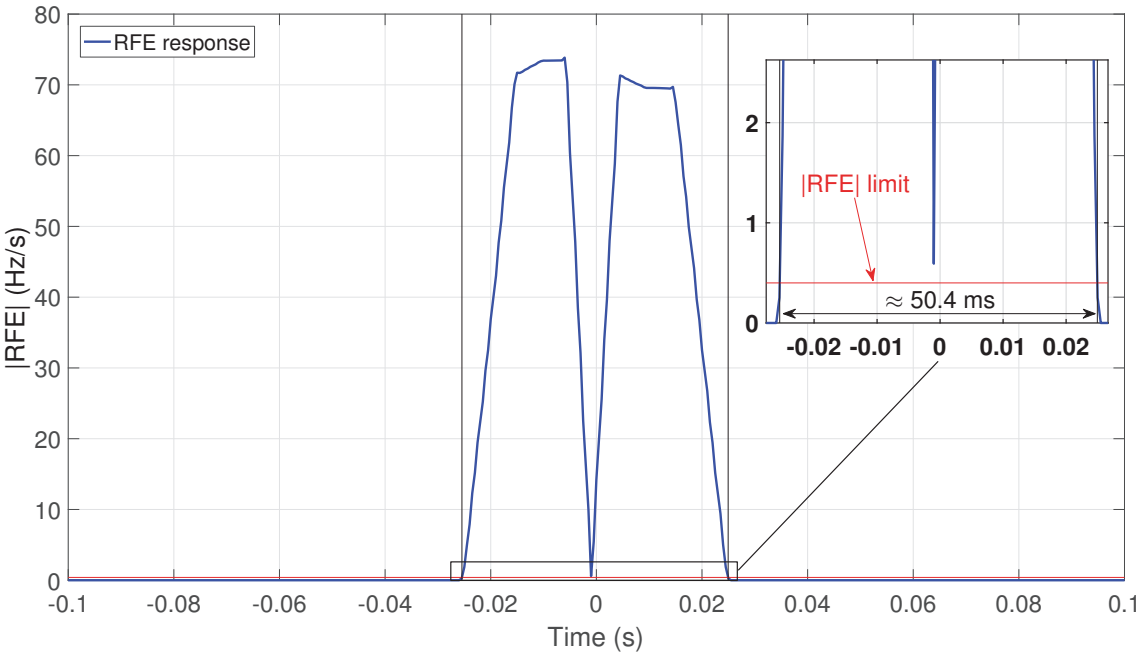

FIGURE IV.21 – Phase step change test result - Determination of the ROCOF algorithm response time

6 Conclusion

To fulfill the last main objective of this dissertation, determine the conditions required to provide protection relays the capability to compute synchrophasors, this chapter starts to analyze the relationship between the computations performed by the protection relay and the synchronization to the absolute time reference. Subsequently, a DFT-based algorithm, based on resampling strategies, have been presented to estimate synchrophasors with high accuracy for P-Class PMUs. This algorithm is capable of providing estimates at a reporting rate of 200 frames per second, that is twice faster than the maximum reporting rate specified in the PMU standard for a system frequency of 50 Hz. The algorithm is merged to the signal processing based on the backward linear interpolation technique described in Chapter III to minimize the computational effort. For example, the frequency and ROCOF estimates provided by the innovative frequency tracking algorithm can be used without any changes for PMU data reporting, which is a real benefit.

The simulations results, conducted following the IEC Standard 60255-181-1, have demonstrated that the proposed solution is compliant with P-Class PMU accuracy class. Nevertheless, the algorithm used to compute the ROCOF, based on the derivative of the phase angle, is very sensitive to abrupt changes in phase angle.

General conclusion and perspectives

The work reported in the present study covers the subject concerning the design of an innovative protection relay, incorporating the phasor measurement unit function, and having sampled measured values as input signals. These data frames substitute the traditional analogue signals provided by conventional instrument transformers and raise new challenges for the protection relays. For example, these SMV frames are produced with a fixed sampling frequency whereas protection relays sample their analogue input signals at a variable rate, multiple of the power system frequency. To deal with the smart grid paradigm, the new signal processing methods must be able to provide accurate estimates of the quantity of interest such as phasor, frequency, and ROCOF within a wide frequency range and during slow and fast ROCOF conditions. Indeed, the distribution grids are currently facing a huge penetration of distributed generators and there is need to improve the accuracy of frequency and ROCOF relays which are employed today as anti-islanding detection methods so that to avoid unwanted tripping conditions.

Consequently, several objectives were undertaken to propose signal processing algorithms for the design of the next generation of protection relays on the basis of SMV frames, able to operate over a wide frequency range, and capable of providing with high accuracy phasor, synchrophasor, frequency, and ROCOF estimates under several static and dynamic conditions, in particular:

1. The Stand-Alone Merging Unit was studied in details by taking into account the requirements imposed by the related standards and the impact of accuracy classes on the PMUs was highlighted ;
2. A metering class 0.1 SAMU was designed ;
3. Three solutions were proposed, compared and tested through simulation to estimate phasors on the basis of SMV frames ;
4. An innovative frequency tracking algorithm which considerably improves the computation of the frequency and the ROCOF was designed ;
5. A synchrophasor estimation algorithm, integrated into the protection relay signal processing, was designed and tested by simulation.

The phasor estimation algorithm is the cornerstone of such intelligent electronic devices for different reasons. The reliability of the relay protective functions depends on accurate phasor estimations. Wrong phasor measurements may lead to unwanted tripping which may jeopardize the integrity of the system. For phasor measurement units, the phasors

must be estimated with an accuracy better than 1% in accordance to the TVE criterion in order to fulfill the standard requirements. To obtain accurate estimation of phasors, this study has chosen the powerful Fourier analysis which has been presented in Chapter I, with an emphasis on the discrete Fourier transform.
The discrete Fourier transform is still widely applied in marketed devices since it is simple and provides accurate phasor estimates. However, two main pernicious effects compromise its accuracy: aliasing and leakage. These phenomena have been mathematically explained and graphically illustrated to better understand their impacts on the phasor estimations. Subsequently, traditional solutions that are used to minimize their detrimental effects have been described.
Chapter I ends with a description of the characteristics and features of the PMUs. The relevant information of the IEC Standard 60255-118-1 has been presented, from the measurements requirements to the reference signal processing model which is proposed to deal with them. In practice, others methods can be employed to comply with the standard measurements requirements. In this context, a review of these methods which can be found in the literature and which have been implemented in devices has been conducted.

In Chapter II, the future challenges of protection relays and phasor measurement units within the scope of digital substations have been presented. A special attention to the process bus problematic have been paid through an analysis performed on the IEC Standard 61850 and the IEC Standard 61869 product families. In particular, the new requirements related to the signal processing field have been highlighted and the characteristics of the sampled measured values presented. These encapsulated data frames are produced by merging units and stand-alone merging units at a fixed and standardized sample rate, synchronized to the GPS system. These electronic interfaces are subject to accuracy classes classifying them according to the errors introduced by the data acquisition chain in the sampled measured values.
The errors introduced have been related to the TVE criterion to study the impacts of the measurement inaccuracies on the synchronized phasor measurement. The results obtained have shown that not all accuracy classes are compatible with the PMU exigencies. Specifically, the protection accuracy classes and the metering accuracy class 1 must not be used as they may cause by themselves errors above 1%. Other metering classes introduces errors below the threshold. From the system perspective, the total errors introduced by the merging units/stand-alone merging units and the PMU phasor estimation algorithm must fulfill the TVE criterion, leaving a reduced margin error for the estimation algorithm. This is the reason why, for PMU applications, preferences are given to metering accuracy class 0.1.
On the basis of these conclusion, a signal processing model for designing a SAMU metering class 0.1 has been proposed and validated through simulation test cases. The model has integrated the most relevant effects of the data acquisition chain components, like the conversion time of the ADC. Nevertheless, the interposed CTs and VTs have not been studied. The results obtained show that the proposed algorithm introduced errors very closed to 0%, that is the output sample streams are almost a perfect representation of the IED input channels. In this light, it can be concluded that the influencing factor of MU/SAMU data acquisition system for determining its accuracy class is its hardware part

rather than the algorithms involved.

In Chapter III, three algorithms have been proposed for estimating phasors in the protection relay perspective, under static and/or dynamic conditions. They are based on the three different interpolation processes to increase the robustness of the DFT in case of frequency excursions. Two of them resample the signals to a lower rate in the time-domain and require the knowledge of the power system frequency to perform the decimation operation. The system frequency is tracked by computing the phase angle deviation of the fundamental positive sequence voltage phasor. Finally, the last proposed interpolation method involves DFT bins spectrum interpolation and does not require any frequency estimation as input. The first time-domain algorithm described in Chapter III, called i-SVA, alter the magnitude of the samples to generate a sample stream whose frequency is synchronized to the power system frequency. To achieve this goal, a cubic spline interpolation is performed on the input samples. The second time-domain algorithm is based on the simple linear interpolation and down-sampling process. In contrast to the i-SVA interpolation method, this second algorithm generates a new stream of samples whose timestamps correspond to those obtained in case of synchronous sampling frequency condition. The last proposed algorithm is based on the interpolated DFT methods using a Hanning window. It uses the samples coming from the process bus directly without decimating the signal since the algorithm requires a high sample rate to give accurate results. In addition to the phasor estimation, the interpolated DFT is able to provide frequency estimation as well.
The i-SVA and linear interpolation algorithms have been coupled with the frequency estimation algorithm forming a closed-loop system. Analysis demonstrated that such a system faces some issues during ramps of frequency if the resampling strategy is performed following the time axis. Each time the sampling frequency is adjusted according to the estimated system frequency, it follows immediately a transient period during which raw frequency measurements are wrong yielding to wrong ROCOF estimations. Protection functions related to these frequency and ROCOF estimations may issue some unwanted tripping. In connection with massive penetrations of distributed generators in the distribution grids, these nuisance tripping are not acceptable. In this context, a new frequency tracking principle has been proposed. It is based on retroactive computation of samples and makes insensitive the frequency measurement method to changes of the sample rate.
An extensive range of signal models have been used to test the three proposed solutions under static and/or dynamic conditions with an emphasis on frequency excursions. The test cases include off-nominal steady-state signals corrupted by harmonics, slow and fast ramp of frequencies, and frequency jump. Whatever the method employed, the frequency and ROCOF algorithms have shown almost similar behaviors with good accuracies. However, preferences are given for the linear interpolation and down-sampling solution since the frequency tracking speed is faster than the two other methods. The main issue has been detected for ROCOF estimates during the frequency step test case with values up to 200 Hz/s. For estimation of phasors, the linear interpolation algorithm-based solution remains the most accurate in all cases except for the off-nominal steady-state signal corrupted by harmonics.

Since the backward linear interpolation-based signal processing model gave satisfactions to obtain accurate phasor, frequency and ROCOF estimates, it has been used as starting point to design a synchrophasor algorithm in Chapter IV. This algorithm takes advantage of some computations already performed for protection functions so that the synchrophasor algorithm is merged into the "initial" signal processing model. By doing this, some CPU processing power is reduced. The most important point for a successful integration of the synchrophasor algorithm is the synchronization between the instant of computations of the signal processing algorithms dedicated to protection and the PMU reporting rate. Once this is performed correctly, the synchrophasor, frequency, and ROCOF estimates can be computed with a reporting rate of 200 for a 50 Hz system and of 240 for a 60 Hz system, that is twice higher than the reporting rates defined in the latest version of the PMU standard. Finally, the whole solution has been tested using the PMU standard with a reporting rate of 200. The simulation results obtained have demonstrated that the complete signal processing design cope with the measurement exigencies of the PMU standard which are the TVE, FE, and RFE criteria.

The backward linear interpolation-based signal processing algorithms presented in the current study have been characterized, modeled, and validated in a simulation environment. Therefore, future short-term prospects are related to a feasible deployment of the proposed algorithms on a real protection relay having SMV frames as inputs. The objective of such implementation is to validate of both the new frequency tracking algorithm and the synchrophasor algorithm. To do so, the Real-Time Digital Simulator (RTDS) can be useful as it is capable of simulating many smart grid- and renewable energy-related concepts [Tec16]. As such, it can act as a merging unit and has facilities for simulating distributed generation. Once the distribution grid has been modeled, the protection relay having synchrophasor capability and SMV as inputs can be connected to the simulator in order to carry out closed-loop testing.
The performance of the new frequency tracking principle can be assessed using a ROCOF-based protection function to detect islanding. The idea is to compare the performances obtained with the classical frequency tracking algorithm and those obtained with the new one using two different relays ; each one using a different frequency tracking strategy. Today, the prototype is validated, the proposed algorithms translated into source codes and implemented into the relay. Nevertheless, the firmware shall be modified so that to extract frequency and ROCOF estimates computed by the device.
For the synchrophasor algorithm, the test cases imposed by the standard can be simulated with the RTDS and the associated waveforms directly injected to the relay using SMV frames. The estimates can be stored in memory and extracted for comparison to the theoretical estimate values.
The validation of the behavior of proposed algorithms in real-time condition is the cornerstone in a longer time perspective. Specifically, the algorithms may be implemented into the next generation of protection relays under development in the company whose features can cope with the new challenges of tomorrow, mainly related to the large penetration of distributed generations in the distribution grid. In particular, better frequency and ROCOF measurements are expected to improve the islanding detection and avoid nuisance tripping. Finally, the proposed synchrophasor estimation algorithm can be used in the

distribution network for exchanging data between protections improving their response time. For instance, quicker reclose operations may be achieved with absolute phase angle information, reducing the inconvenience of momentary power interruptions.

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Journal papers

1. C. Ghafari, H. Almasalma, N. Hadjsaid, R. Caire, B. Raison and E. Martin, "Phasors Estimation at Off-Nominal Frequencies through enhanced-SVA method with Fixed Sampling Clock", IEEE Transactions on Power Delivery, vol. PP, no. 99, pp. 1-1, Aug. 2016 *(accepted for publication)*

Patents

1. J. Mécréant, C. Ghafari, R. Caire and B. Raison, "Calculation of an alternative signal frequency", Schneider Electric Industries SAS, Aug. 2016 *(under review)*

Conference papers

1. C. Ghafari, H. Almasalma, N. Hadjsaid, R. Caire, B. Raison and E. Martin, "Phasors Estimation at Off-Nominal Frequencies through enhanced-SVA method with Fixed Sampling Clock", PowerTech, 2017 IEEE Manchester, vol. PP, no. 99, pp. 1-1, Aug. 2016 *(accepted for presentation)*

Appendix A

Analysis of the regular and average sampling processes

The main objective of this study is to mathematically demonstrate if the feasible sampling processes (using "Hold" circuit function) yield distortions in the spectrum in comparison to the ideal sampling process. Recall that the latter allows to retrieve the baseband portion of the spectrum by a low-pass filter assimilated to a boxcar function of width F_s.

The regular and average sampling processes can be analyzed starting with the natural sampling process. In this case, the amplitude of each pulse "follows" the amplitude of the input signal during the pulse width τ_p. This natural sampling process is not feasible in practice but constitutes an intermediate calculation step which is necessary for understanding the two others sampling processes.

The impulse train periodic with a period T_s and of pulse width τ_p can be mathematically modeled through the use of gate function $\Pi_{\tau_p}(t)$ as shown:

$$i_{T_s,\tau_p}(t) = \sum_{n=-\infty}^{\infty} \Pi_{\tau_p}(t - nT_s) \tag{A.1}$$

The signal $i_{T_s,\tau_p}(t)$ can be rewritten in a most suitable form by using the periodization property of the Dirac comb and the convolution product:

$$i_{T_s,\tau_p}(t) = \Pi_{\tau_p}(t) * \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{A.2}$$

The spectrum of the signal Eq. (A.2) can be thus expressed as:

$$\begin{aligned} I_{T_s,\tau_p}(f) &= [\tau_p \cdot \frac{\sin(\pi\tau_p f)}{n\pi\tau_p f}] \cdot F_s \cdot \sum_{n=-\infty}^{\infty} \delta(f - nF_s) \\ &= \tau_p \cdot F_s \cdot \sum_{n=-\infty}^{\infty} \frac{\sin(n\pi\tau_p F_s)}{n\pi\tau_p F_s} \cdot \delta(f - nF_s) \end{aligned} \tag{A.3}$$

In case of natural sampling process, the sampled signal $x_{s,n}(t)$ is obtained by multiplying the periodized gate function defined in Eq. (A.2) by the input signal $x(t)$:

$$x_{s,n}(t) = x(t) \cdot i_{T_s,\tau_p}(t) = x(t) \cdot \Pi_{\tau_p}(t) * \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{A.4}$$

By using the relation established in Eq. (A.3), the spectrum $X_{s,n}(f)$ of the signal $x_{s,n}(t)$ is derived as shown:

$$\begin{aligned} X_{s,n}(f) &= X(f) * I_{T_s,\tau_p}(f) \\ &= \tau_p \cdot F_s \cdot \sum_{n=-\infty}^{\infty} \frac{\sin(n\pi\tau_p F_s)}{n\pi\tau_p F_s} \cdot X(f - nF_s) \end{aligned} \tag{A.5}$$

Based on Eq. (A.5), the relation between the baseband of the sampled signal $X_{s,n,b}$ and the spectrum of the input signal $X(f)$ is:

$$X_{s,n,b} = \tau_p \cdot F_s \cdot X(f) \tag{A.6}$$

Equation (A.6) shows that, in case of natural sampling process, it is possible to obtain the initial spectrum with an ideal low-pass filter. The proportionality relationship between the two spectrums highlights that the natural sampling does not introduce distortions. Such a sampling method corresponds simply to a growth of the period during which the signal is being observed. Since this kind of sampling is not feasible practically, the study should focus on cases where the pulse width τ_p is considered together with an approximation of the amplitude of the signal which has been "blocked" during that interval of time.

The regular sampling process can be mathematically expressed as:

$$x_{s,r}(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\Pi_{\tau_p}(t - nT_s) \tag{A.7}$$

Equation (A.7) shows that performing such a sampling on the input signal $x(t)$ is equivalent to apply the gate function periodically while keeping the amplitude of this input signal at $t = nT_s$ for a duration τ_p. It can be rewritten as:

$$x_{s,r}(t) = [x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s)] * \Pi_{\tau_p}(t) \tag{A.8}$$

The spectrum of the signal $x_{s,r}(t)$ is expressed as:

$$\begin{aligned} X_{s,r}(f) &= [X(f) * (F_s \cdot \sum_{n=-\infty}^{\infty} \delta(f - nF_s))] \cdot [\tau_p \cdot \frac{\sin(\pi\tau_p f)}{\pi\tau_p f}] \\ &= \tau_p \cdot F_s \cdot \frac{\sin(\pi\tau_p f)}{\pi\tau_p f} \cdot \sum_{n=-\infty}^{\infty} X(f - nF_s) \end{aligned} \tag{A.9}$$

As done previously, the baseband portion of $X_{s,r}(f)$ is extracted by a low-pass filter assimilated to the rectangular function $\Pi_{F_s}(f)$, resulting in:

$$X_{s,r,b} = \tau_p \cdot F_s \cdot \frac{\sin(\pi\tau_p f)}{\pi\tau_p f} \cdot X(f) \tag{A.10}$$

In addition to the factor $\tau_p F_s$, the baseband portion is not identical to the the spectrum

$X(f)$ because its amplitude is modulated by the $\mathrm{sinc}(\tau_p f)$ function. Therefore, the regular sampling process introduces distortions in the spectrum. These distortions are minors if the ratio τ_p/T_s is small.

The same process can be applied for the average sampling process. In this configuration, since the samples $x_{s,a}(nT_s)$ correspond to the mean value of $x(t)$ during the time τ_p, the sample n is expressed as:

$$x_{s,a}(nT_s) = \frac{1}{\tau_p} \cdot \int_{nT_s-\tau_p/2}^{nT_s+\tau_p/2} x(t)\mathrm{d}t \tag{A.11}$$

By using the boxcar function in Eq. (A.11), the following relation can be obtained:

$$x_{s,a}(nT_s) = \frac{1}{\tau_p} \cdot \int_{nT_s-\tau_p/2}^{nT_s+\tau_p/2} \Pi_{\tau_p}(t - nT_s)x(t)\mathrm{d}t \tag{A.12}$$

Equation (A.12) represents the convolution product of $x(t)$ and $\Pi_{\tau_p}(t)$, hence:

$$x_{s,a}(nT_s) = \frac{1}{\tau_p} \cdot [\Pi_{\tau_p}(t) * x(t)] \cdot \delta(t - nT_s) \tag{A.13}$$

Based on Eq. (A.13), the sampled signal $x_{s,a}(t)$ is expressed as:

$$x_{s,a}(t) = \frac{1}{\tau_p} \cdot \sum_{n=-\infty}^{\infty} [\Pi_{\tau_p}(t) * x(t)] \cdot \delta(t - nT_s) \tag{A.14}$$

The spectrum $X_{s,a}(f)$ of $x_{s,a}(t)$ is obtained through the DTFT by using the Plancherel theorem:

$$\begin{aligned} X_{s,a}(f) &= \frac{1}{\tau_p} \cdot [\tau_p \cdot \frac{\sin(\pi\tau_p f)}{\pi\tau_p f} \cdot X(f)] * [F_s \cdot \sum_{n=-\infty}^{\infty} \delta(f - nF_s)] \\ &= F_s \cdot \sum_{n=-\infty}^{\infty} \frac{\sin(\pi\tau_p(f - nF_s))}{\pi\tau_p(f - nF_s)} \cdot X(f - nF_s) \end{aligned} \tag{A.15}$$

As done previously, the extraction of the baseband portion of $X(f)$ yields:

$$X_{s,a,b}(f) = F_s \cdot \frac{\sin(\pi\tau_p f)}{\pi\tau_p f} \cdot X(f) \tag{A.16}$$

The result obtained is very closed to the one obtained for the regular sampling process (see Eq. (A.10)). In addition to the factor F_s, the spectrum is distorted by the $\mathrm{sinc}(\pi\tau_p f)$ function.

As a conclusion, the regular and average sampling processes can be assimilated to the ideal sampling process if the pulse width τ_p is small compared to the period of the sampled signal, that is the maximal frequency component it contains.

Appendix B

Phasor estimation at off-nominal frequency based on full-cycle DFT algorithm

The impact of the leakage phenomenon on the DFT-based phasor estimator can be shown mathematically. To do so, let us consider a sinusoidal input signal of off-nominal angular frequency $\omega = 2\pi f$, where $\omega = \omega_0 + \Delta\omega$, with m^{th} harmonic given by:

$$x(t) = X_1 \cos(\omega t + \phi_1) + X_m \cos(m\omega t + \phi_m) \tag{B.1}$$

By taking the real part of the exponential function, Eq. (B.1) can be expressed as:

$$x(t) = \sqrt{2} Re\left\{ \frac{X_1}{2} e^{j\phi_1} e^{j\omega t} \right\} + \sqrt{2} Re\left\{ \frac{X_m}{2} e^{j\phi_m} e^{jm\omega t} \right\} \tag{B.2}$$

Based on Eq. (B.2), the correct phasor representation of the fundamental is $\overline{X_1} = \frac{X_1}{\sqrt{2}} e^{j\phi_1}$. Similarly, the m^{th} harmonic phasor representation is $\overline{X_m} = \frac{X_m}{\sqrt{2}} e^{j\phi_m}$. By using the two above-mentioned expressions, Eq. (B.2) can be rewritten as:

$$x(t) = \sqrt{2} Re\left\{ \overline{X_1} e^{j\omega t} \right\} + \sqrt{2} Re\left\{ \overline{X_m} e^{jm\omega t} \right\} \tag{B.3}$$

Expressing the real value as the average of a complex number and its complex conjugate leads to the following:

$$x(t) = \frac{\sqrt{2}}{2} \{ \overline{X_1} e^{j\omega t} + \overline{X_1^*} e^{j\omega t} \} + \frac{\sqrt{2}}{2} \{ \overline{X_m} e^{jm\omega t} + \overline{X_m^*} e^{jm\omega t} \} \tag{B.4}$$

On the other hand, the non-recursive DFT phasor estimate tuned to a particular harmonic m at sample time r can be written as shown:

$$\overline{X_m}^{(r)} = \frac{\sqrt{2}}{N} \sum_{n=r}^{r+N-1} x(n\Delta t) e^{-jnm\omega_0 \Delta t} \tag{B.5}$$

Through the use of the sampling process on the input signal given by Eq. (B.4), that is $t = n\Delta t$ with $\Delta t = \frac{1}{N f_0}$, the fundamental phasor of $x(t)$ can be computed using the non-recursive DFT formula as derived:

$$\overline{X}^{(r)} = \frac{1}{N} \sum_{n=r}^{r+N-1} \{ \overline{X_1} e^{j\omega n\Delta t} + \overline{X_1^*} e^{-j\omega n\Delta t} \} e^{-jn\omega_0 \Delta t} + \frac{1}{N} \sum_{n=r}^{r+N-1} \{ \overline{X_m} e^{jm\omega n\Delta t} + \overline{X_m^*} e^{-jm\omega n\Delta t} \} e^{-jnm\omega_0 \Delta t}$$

$$\overline{X}^{(r)} = \frac{1}{N}\sum_{n=r}^{r+N-1}\{\overline{X_1}e^{j(\omega-\omega_0)n\Delta t} + \overline{X_1^*}e^{-j(\omega+\omega_0)n\Delta t}\} + \frac{1}{N}\sum_{n=r}^{r+N-1}\{\overline{X_m}e^{jm(\omega-\omega_0)n\Delta t} + \overline{X_m^*}e^{-jm(\omega+\omega_0)n\Delta t}\}$$

$$\overline{X}^{(r)} = \frac{1}{N}\sum_{n=r}^{r+N-1}\overline{X_1}e^{j\frac{2\pi\Delta f}{Nf_0}n} + \frac{1}{N}\sum_{n=r}^{r+N-1}\overline{X_1^*}e^{-j\frac{2\pi(\Delta f+2f_0)}{Nf_0}n} + \frac{1}{N}\sum_{n=r}^{r+N-1}\overline{X_m}e^{j\frac{2\pi\Delta f}{Nf_0}mn} + \frac{1}{N}\sum_{n=r}^{r+N-1}\overline{X_m^*}e^{-j\frac{2\pi(\Delta f+2f_0)}{Nf_0}mn} \quad \text{(B.6)}$$

Equation (B.6) could be simplified by substituting n per k, with $k = n - r$, as written below:

$$\begin{aligned}\overline{X_r} &= \frac{1}{N}\overline{X_1}e^{j\frac{2\pi\Delta f}{Nf_0}r}\sum_{k=0}^{N-1}e^{j\frac{2\pi\Delta f}{Nf_0}k} + \frac{1}{N}\overline{X_1^*}e^{-j\frac{2\pi(\Delta f+2f_0)}{Nf_0}r}\sum_{k=0}^{N-1}e^{-j\frac{2\pi(\Delta f+2f_0)}{Nf_0}k} \\ &= \frac{1}{N}\overline{X_m}e^{j\frac{2\pi\Delta f}{Nf_0}r}\sum_{k=0}^{N-1}e^{j\frac{2\pi\Delta f}{Nf_0}mk} + \frac{1}{N}\overline{X_m^*}e^{-j\frac{2\pi(\Delta f+2f_0)}{Nf_0}r}\sum_{k=0}^{N-1}e^{-j\frac{2\pi(\Delta f+2f_0)}{Nf_0}mk} \quad \text{(B.7)}\end{aligned}$$

The geometric series on the exponential function is derived below:

$$\sum_{k=0}^{N-1}e^{jk\theta} = \frac{1-e^{jN\theta}}{1-e^{j\theta}} = \frac{\sin\frac{N\theta}{2}}{\sin\frac{\theta}{2}}e^{\frac{j(N-1)\theta}{2}} \quad \text{(B.8)}$$

Thus, from Eq. (B.8), the phasor estimate $\overline{X}^{(r)}$ could be expressed as function of the phasors of the fundamental and the m^{th} harmonic and theirs complex conjugates ; each of them multiplied by a particular complex factor as shown:

$$\overline{X}^{(r)} = \overline{P_1}^{(r)}\overline{X_1} + \overline{Q_1}^{(r)}\overline{X_1^*} + \overline{P_m}^{(r)}\overline{X_m} + \overline{Q_m}^{(r)}\overline{X_m^*} \quad \text{(B.9)}$$

with:

$$\overline{P_1}^{(r)} = \frac{\sin\left(\frac{\pi\Delta f}{f_0}\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}\right)}e^{j\pi\frac{(N-1)}{N}\frac{\Delta f}{f_0}}e^{j\frac{2\pi\Delta f}{Nf_0}r} \quad \text{(B.10)}$$

$$\overline{Q_1}^{(r)} = \frac{\sin\left((\frac{\pi}{f_0})(\Delta f+2f_0)\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}+\frac{2\pi}{N}\right)}e^{-j\pi\frac{(N-1)}{Nf_0}(\Delta f+2f_0)}e^{-j\frac{2\pi}{Nf_0}(\Delta f+2f_0)r} \quad \text{(B.11)}$$

$$\overline{P_m}^{(r)} = \frac{\sin\left(\frac{\pi\Delta f}{f_0}\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}\right)}e^{j\pi\frac{(N-1)}{N}\frac{\Delta f}{f_0}m}e^{j\frac{2\pi\Delta f}{Nf_0}r} \quad \text{(B.12)}$$

$$\overline{Q_m}^{(r)} = \frac{\sin\left((\frac{\pi}{f_0})(\Delta f+2f_0)\right)}{N\sin\left(\frac{\pi\Delta f}{Nf_0}+\frac{2\pi}{N}\right)}e^{-j\pi\frac{(N-1)}{Nf_0}(\Delta f+2f_0)m}e^{-j\frac{2\pi}{Nf_0}(\Delta f+2f_0)r} \quad \text{(B.13)}$$

Now, in case the frequency is slightly moving from its nominal value, which is most of

the time true in power systems, that is $\Delta f = f - f_0 \approx 0$, the value of the resultant phasor $\overline{X}^{(0)}$ at sample time $r = 0$ could be simplified. To do so, let us compute the limit of the $\overline{P_1}^{(0)}$ factor in the aforementioned, where Δf approaches 0:

$$\begin{aligned}
\lim_{\Delta f \to 0} \overline{P_1}^{(0)}(\Delta f) &= \lim_{\Delta f \to 0} \left(\frac{\sin\left(\frac{\pi \Delta f}{f_0}\right)}{N \sin\left(\frac{\pi \Delta f}{N f_0}\right)} e^{j\pi \frac{(N-1)}{N} \frac{\Delta f}{f_0}} e^{j \frac{2\pi \Delta f}{N f_0} r} \right) \\
&= \lim_{\Delta f \to 0} \left(\frac{\sin\left(\frac{\pi \Delta f}{f_0}\right)}{N \sin\left(\frac{\pi \Delta f}{N f_0}\right)} e^{j\pi \frac{(N-1)}{N} \frac{\Delta f}{f_0}} e^{j \frac{2\pi \Delta f}{N f_0} r} \right) \\
&\approx \frac{1}{N} \times \frac{\left(\frac{\pi \Delta f}{f_0}\right)}{\left(\frac{\pi \Delta f}{N f_0}\right)} \times 1 \times 1 \\
&\approx 1
\end{aligned} \tag{B.14}$$

The same calculation could be realized for the $\overline{Q_1}^{(0)}$ factor. The result is given below:

$$\begin{aligned}
\lim_{\Delta f \to 0} \overline{Q_1}^{(0)}(\Delta f) &= \lim_{\Delta f \to 0} \left(\frac{\sin\left((\frac{\pi}{f_0})(\Delta f + 2f_0)\right)}{N \sin\left(\frac{\pi \Delta f}{N f_0} + \frac{2\pi}{N}\right)} e^{-j\pi \frac{(N-1)}{N f_0} (\Delta f + 2f_0)} e^{-j \frac{2\pi}{N f_0} (\Delta f + 2f_0) r} \right) \\
&\approx \frac{\pi \Delta f}{N f_0 \sin\left(\frac{2\pi}{N}\right)}
\end{aligned} \tag{B.15}$$

In a word, the $\overline{P_1}^{(0)}$ factor could be disregarded only for very small frequency deviations. On the contrary, $\overline{Q_1}^{(0)}$ shall be taken into account as soon as the power system frequency drifts. Based on this fact, Eq. (B.9) is reduced to:

$$\overline{X}^{(0)} = \overline{X_1} + \frac{\sin\left((\frac{\pi}{f_0})(\Delta f + 2f_0)\right)}{N \sin\left(\frac{\pi \Delta f}{N f_0} + \frac{2\pi}{N}\right)} e^{-j\pi \frac{(N-1)}{N f_0} (\Delta f + 2f_0)} \overline{X_1^*} \tag{B.16}$$

The qualitative analysis of the effect of the complex gains $\overline{P_1}^{(0)}$ and $\overline{Q_1}^{(0)}$ have been presented, but this study does not highlight whether or not a small frequency deviation impacts drastically the estimation of the phasor of interest. Moreover, these factors are also influenced by the sampling rate as justified by equations Appendices B and B. Thus, the two aforementioned factors shall be assessed separately by fixing one of them while varying the other and conversely. First of all, let us set the power system nominal frequency f_0 at 50 Hz, sampled at a fixed sampling rate of $F_s = 2,400$ Hz, so N, the number of samples per nominal cycle, is 48. In such a configuration, the magnitude and phase response of both complex gains can be plotted, considering a frequency deviation of ± 10 Hz:

Regarding the P_1 factor, it appears that the more the frequency deviation is, the more the attenuation is. Anyway, within the range ± 2 Hz, the magnitude is almost equal to 1, with a maximum attenuation around about 99,8% for $\Delta f = 2$ Hz. As a consequence, for practical power systems frequency excursions, the P_1 factor has no impact on the magnitude of $\overline{X_0}$, as shown in equation (B.15). Despite this fact, for the same range of frequency

deviation, the phase angle of P_1 factor, varying linearly, introduces a phase shift to the resultant phasor which has to be considered.

For the Q_1 factor, the conclusions to be drawn are slightly different. First, its magnitude tends to vary linearly and increases according to the frequency deviation. Then, the phase shift introduced is bigger that the P_1 factor, with a phase angle of 15 degrees at the nominal frequency and varies linearly. Lastly, in spite of the small values of magnitude, the Q_1 factor cannot be ignored as it is the case for its homologue pair. Indeed, the complex gain Q_1, which has a frequency near the 2^{nd} harmonic, introduces oscillations at an angular speed of $2\omega_0$ rad/s in both magnitude and phase angle on the phasor $P_1\overline{X_1}$. The amplitudes of these oscillations are depicted in the figure. For example, a frequency deviation of 0.5 Hz only will introduce ripples of amplitudes 0.0042 p.u., so corresponding to a peak-to-peak value of 0.0084 p.u., on the resultant phasor $\overline{X_0}$ while the P_1 factor effect is insignificant.

Last of all, let us select, for instance, a frequency deviation of $+1Hz$ to draw the effect of the sampling rate on both complex gains P_1 and Q_1. Plotting the magnitude and the phase angle as function of the number of samples N yields to

As depicted by the previous figure, on the one hand, P_1 is almost unaffected by the sampling rate even if its phase angle tends to increase with it. However, the variations introduced are in the order of a few mili degrees for a wide range of sampling rate, that is to say that the phase shift will nearly remain the same whatever the sampling frequency is. On the other hand, the Q_1 factor is much more sensitive to the sampling frequency in terms of phase angle only.

Appendix C

Backward finite difference method for i-SVA method

This annex gives the mathematical proof to obtain the coefficients b_0, b_1, b_2 and b_3 used by the i-SVA method described in Chapter II.

Recall that $x[n]$ is related to $x[n]^*$ and its derivatives as shown:

$$x[n] = x[n]^* - (\alpha h)x'[n]^* + \frac{1}{2}(\alpha h)^2 x''[n]^* - \frac{1}{6}(\alpha h)^3 x'''[n]^* \tag{C.1}$$

The derivatives are approximated using the backward finite difference method. Several orders of accuracy can be used to approximate a given derivative. The higher the order is, the better the accuracy is, but more samples are necessary for approximation. To ease the i-SVA algorithm design, the number of samples is kept constant for every derivatives resulting in approximations of different orders. In this study, 4 samples have been selected to perform the approximation process.

To get the coefficients of the backward approximations, the tables given in [Wik16] have been used. Based on these coefficients, the derivatives are approximated as follow:

$$x'[n]^* \approx \frac{\frac{11}{6}x[n]^* - 3x[n-1]^* + \frac{3}{2}x[n-2]^* - \frac{1}{3}x[n-3]^*}{h} + \mathcal{O}(h^3) \tag{C.2}$$

$$x''[n]^* \approx \frac{2x[n]^* - 5x[n-1]^* + 4x[n-2]^* - x[n-3]^*}{h^2} + \mathcal{O}(h^2) \tag{C.3}$$

$$x'''[n]^* \approx \frac{x[n]^* - 3x[n-1]^* + 3x[n-2]^* - x[n-3]^*}{h^3} + \mathcal{O}(h^1) \tag{C.4}$$

where:

h	is the uniform asynchronous sampling period
$\mathcal{O}$	denotes the "Big O" notation referred to as order of approximation

Substituting Eqs. (C.2) to (C.4) in Eq. (C.1) leads to:

$$\begin{aligned} x[n] = (1 - \frac{11}{6}\alpha + \alpha^2 - \frac{1}{6}\alpha^3)x[n]^* + (3\alpha - 2.5\alpha^2 + 0.5\alpha^3)x'[n]^* \\ + (-1.5\alpha + 2\alpha^2 - 0.5\alpha^3)x''[n]^* + (\frac{1}{3}\alpha - 0.5\alpha^2 + \frac{1}{6}\alpha^3)x'''[n]^* \end{aligned} \tag{C.5}$$

From Eq. (C.5), the coefficients b_0, b_1, b_2 and b_3 used by the i-SVA algorithm can be immediately recognized.

Appendix D

enhanced-Sampled Value Adjustment for estimation of synchrophasors

The enhanced-SVA (e-SVA) resampling algorithm is designed to deal with dynamic performances introduced by the latest version of the PMU standard. It is based on the i-SVA method. The idea of e-SVA is to displace the window in such a way that the timestamp is located at/near the center of that window while keeping the correct phase angle given by $x[0]$. The position of the timestamp in relation to the center depends on the parity of N. If N is an odd integer, then it exists a sample which is exactly at the center of the window and this sample has the synchrophasor time-mark. Conversely, if N is even, a drift of half a sampling period is introduced between the center of the window and the sample timestamped by the synchrophasor time-tag. Now, to cope with the new synchrophasor dynamic performances, the magnitude of the sample $x[0]^*$ shall remain unchanged after the resampling process. To do so, in addition to the backward computation, the e-SVA algorithm uses the forward finite difference methods whose general equation could be written as

$$x[n] = b_n x[n]^* + b_{n+1} x[n+1]^* + b_{n+2} x[n+2]^* + b_{n+3} x[n+3]^* \tag{D.1}$$

Thus, for a given synchrophasor reporting time, the data of the window on the left of the synchrophasor time-tag (see time-tag $T_R = 0.14$ s in Fig. D.1) will be resampled following the backward method described above while the samples on the right will be recomputed using forward finite difference. Basically, the coefficients of the forward finite difference are obtained by giving the opposite sign $(-)$ to all backward coefficients of odd derivatives, which are $x'[n]^*$ and $x'''[n]^*$. However, such a rule will unequivocally lead to changes in the coefficients defined in Eqs. (III.10) to (III.13) making them unusable for the forward finite difference as shown below

$$b_0 = 1 + \frac{11}{6}\alpha + \alpha^2 + \frac{1}{6}\alpha^3 \tag{D.2}$$

$$b_1 = -3\alpha - 2.5\alpha^2 - 0.5\alpha^3 \tag{D.3}$$

$$b_2 = 1.5\alpha + 2\alpha^2 + 0.5\alpha^3 \tag{D.4}$$

$$b_3 = -\frac{1}{3}\alpha - 0.5\alpha^2 - \frac{1}{6}\alpha^3 \tag{D.5}$$

Through the e-SVA method, the resampling is mirrored on both sides of the timestamp, which means that the reverse computation with backward finite difference coefficients could be seen as a computation following the time axis with forward coefficients. Indeed, substituting α by $-\beta$ in Eqs. (III.10) to (III.13) leads to the same coefficients given by Eqs. (D.2) to (D.5). The only difference for the backward computation lies on the values of n in the

expression $\alpha = n\Delta f$ which has to be given with the opposite sign, that is $\beta = -n\Delta f$. As a result, Eqs. (D.2) to (D.5) are valid in both cases. Following the above discussion, considering that N is an even integer, the time-reversal backward resampling is applied for $n = 0, -1, -2, \ldots - N/2$ while the forward resampling is done for $n = 0, 1, 2, \ldots N/2 - 1$. The size of the buffer is equal to $(N + 6)$, where 3 more samples are necessary for each resampling method as shown in Eq. (III.9) and Eq. (D.1). An example of e-SVA method applied on the signal $x(t) = cos(2\pi 45t)$, sampled at a sampling rate of $f_{s0} = 48 \times 50$ Hz, at a synchrophasor time-tag $T_R = 0.14$ s, is shown in Fig. D.1. Clearly, the amplitude of the sample $n = 0$ at $T_R = 0.14$ s remains unchanged while the other asynchronous samples are recomputed in such a way that the resampled signal appears as a synchronous 50 Hz signal. The previous derivation is applicable only for frequencies below the nominal value.

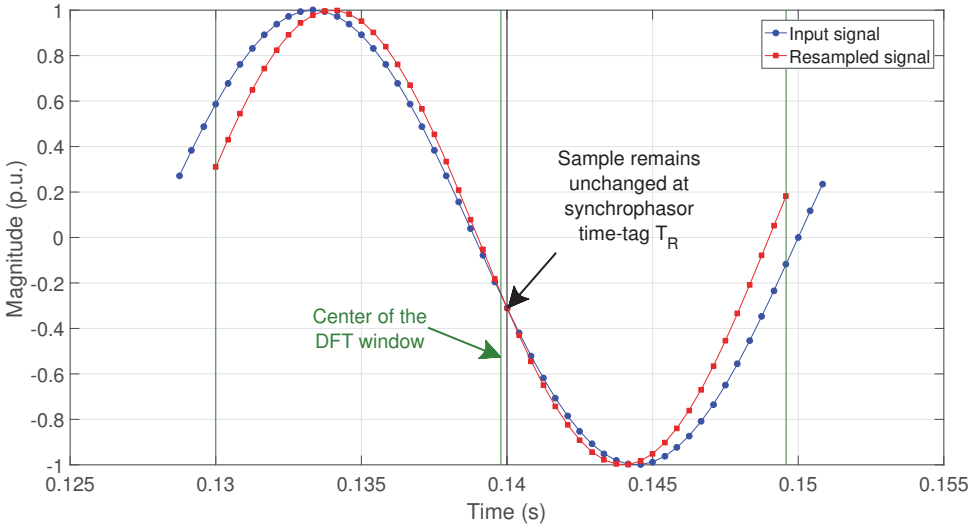

FIGURE D.1 – e-SVA method of a 45 Hz signal, at $T_R = 0.14$ s

The computation is slightly different for off-nominal frequencies above the fundamental. Following the same reasoning described in [AT10], for frequencies higher than 50 Hz, considering α as $[n(\frac{f-f_0}{f}) + 2]$ gives better accuracy.

Finally, another important point to mention concerns the computation of the Full-Cycle DFT whose coefficients have to be adapted to extract the correct phase angle information from the resampled signal. To do so, Eq. (D.6) must be used:

$$\overline{X(T_R)} = \frac{\sqrt{2}}{N} \sum_{n=-\frac{N}{2}}^{\frac{N}{2}-1} x[T_R - n] e^{-j\frac{2\pi}{N}n} \tag{D.6}$$

Appendix E

DFT derivation of the Hanning window applied to a cosine sample set

The main objective of this study is to derive the discrete Fourier transform of a cosine sample set tapered with a Hanning window. To do so, let us assume that the signal under analysis is defined as:

$$x[n] = A\cos(2\pi\frac{f}{F_s}n + \varphi), \quad 0 \leq n \leq M-1 \tag{E.1}$$

where:

f	is the actual power system frequency
F_s	is the sampling frequency
M	is the number of samples acquired in exactly 2 cycles

Remind that the relationship between the system frequency f and the frequency resolution Δf is expressed as:

$$f = (l+\delta)\Delta f = \lambda\Delta f \tag{E.2}$$

where:

l	is the index of the DFT bin with the highest amplitude
δ	is the deviation of f from the relative DFT maximum $l\Delta f$

Based on Eq. (E.2), Eq. (E.1) can be rewritten in a simpler form as shown:

$$x[n] = A\cos(\frac{2\pi\lambda}{M}n + \varphi), \quad 0 \leq n \leq M-1 \tag{E.3}$$

Reminding that the Hanning window is defined in the discrete domain as

$$w_H[n] = \frac{1-\cos(\frac{2\pi n}{M})}{2}, \quad 0 \leq n \leq M-1 \tag{E.4}$$

the tapered time function $x_w[n] = x[n] \cdot w_H[n]$ is computed as:

$$\begin{aligned} x_w[n] &= A\cos(\frac{2\pi\lambda}{M}n + \varphi) \cdot \frac{1-\cos(\frac{2\pi n}{M})}{2} \\ &= \frac{A}{2}[\cos(\frac{2\pi\lambda}{M}n + \varphi) - 0.5(\cos(\frac{2\pi(\lambda-1)}{M}n + \varphi) + \cos(\frac{2\pi(\lambda+1)}{M}n + \varphi))] \end{aligned} \tag{E.5}$$

The discrete Fourier transform of the signal $x_w[n]$ is expressed as it follows:

$$\overline{X_w(k)} = \frac{1}{G_H}\sum_{n=0}^{M-1} x_w[n]e^{-j\frac{2\pi}{M}nk} \tag{E.6}$$

where:

G_H denotes the gain of the Hanning window, $G_H = \sum_{n=0}^{M-1} w_H[n]$

Substituting Eq. (E.5) in Eq. (E.6) and using Euler's formula to express the cosine terms as complex exponential functions, Eq. (E.6) can be expressed as:

$$\begin{aligned}\overline{X_w(k)} &= \frac{A}{2G_H}\sum_{n=0}^{M-1}\Big(\frac{e^{j(\frac{2\pi\lambda}{M}n+\varphi)}+e^{-j(\frac{2\pi\lambda}{M}n+\varphi)}}{2} - 0.5\Big(\frac{e^{j(\frac{2\pi(\lambda-1)}{M}n+\varphi)}+e^{-j(\frac{2\pi(\lambda-1)}{M}n+\varphi)}}{2} \\ &\qquad + \frac{e^{j(\frac{2\pi(\lambda+1)}{M}n+\varphi)}+e^{-j(\frac{2\pi(\lambda+1)}{M}n+\varphi)}}{2}\Big)\Big)\cdot e^{-j\frac{2\pi}{M}nk} \\ &= \frac{A}{4G_H}\Big[\sum_{n=0}^{M-1}\big(e^{j(\frac{2\pi}{M}(\lambda-k)n)} - 0.5\big(e^{j(\frac{2\pi}{M}(\lambda-1-k)n)} + e^{j(\frac{2\pi}{M}(\lambda+1-k)n)}\big)\big)e^{j\varphi} \\ &\qquad + \sum_{n=0}^{M-1}\big(e^{-j(\frac{2\pi}{M}(\lambda+k)n)} - 0.5\big(e^{-j(\frac{2\pi}{M}(\lambda-1+k)n)} + e^{-j(\frac{2\pi}{M}(\lambda+1+k)n)}\big)\big)e^{-j\varphi}\Big] \qquad \text{(E.7)}\end{aligned}$$

Reminding that

$$\sum_{n=0}^{M-1} e^{jxn} = \frac{1-e^{jxM}}{1-e^{jx}} = \frac{e^{jx\frac{M}{2}}(e^{-jx\frac{M}{2}}-e^{jx\frac{M}{2}})}{e^{j\frac{x}{2}}(e^{-j\frac{x}{2}}-e^{j\frac{x}{2}})} = \frac{\sin(x\frac{M}{2})}{\sin(\frac{x}{2})}e^{jx\frac{M-1}{2}} \qquad \text{(E.8)}$$

Eq. (E.7) can be rewritten as:

$$\begin{aligned}\overline{X_w(k)} &= \frac{Ae^{j\varphi}}{4G_H}\Big[\frac{\sin(\pi(\lambda-k))}{\sin(\frac{\pi}{M}(\lambda-k))}e^{ja(\lambda-k)} \\ &\quad - 0.5\Big(\frac{\sin(\pi(\lambda-1-k))}{\sin(\frac{\pi}{M}(\lambda-1-k))}e^{ja(\lambda-1-k)} + \frac{\sin(\pi(\lambda+1-k))}{\sin(\frac{\pi}{M}(\lambda+1-k))}e^{ja(\lambda+1-k)}\Big)\Big] \\ &\quad + \frac{Ae^{-j\varphi}}{4G_H}\Big[\frac{\sin(\pi(\lambda+k))}{\sin(\frac{\pi}{M}(\lambda+k))}e^{-ja(\lambda+k)} \\ &\quad - 0.5\Big(\frac{\sin(\pi(\lambda-1+k))}{\sin(\frac{\pi}{M}(\lambda-1+k))}e^{-ja(\lambda-1+k)} + \frac{\sin(\pi(\lambda+1+k))}{\sin(\frac{\pi}{M}(\lambda+1+k))}e^{-ja(\lambda+1+k)}\Big)\Big] \\ &= \overline{X_w^+(k)} + \overline{X_w^-(k)} \qquad \text{(E.9)}\end{aligned}$$

where $a = \pi(M-1)/M$. $\overline{X_w^+(k)}$ and $\overline{X_w^-(k)}$ denote the positive image and the negative image of the DFT bins respectively. They are defined as it follows:

$$\begin{aligned}\overline{X_w^+(k)} &= \frac{Ae^{j\varphi}}{4G_H}\Big[\frac{\sin(\pi(\lambda-k))}{\sin(\frac{\pi}{M}(\lambda-k))}e^{ja(\lambda-k)} \\ &\quad - 0.5\Big(\frac{\sin(\pi(\lambda-1-k))}{\sin(\frac{\pi}{M}(\lambda-1-k))}e^{ja(\lambda-1-k)} + \frac{\sin(\pi(\lambda+1-k))}{\sin(\frac{\pi}{M}(\lambda+1-k))}e^{ja(\lambda+1-k)}\Big)\Big] \qquad \text{(E.10)} \\ \overline{X_w^-(k)} &= \frac{Ae^{-j\varphi}}{4G_H}\Big[\frac{\sin(\pi(\lambda+k))}{\sin(\frac{\pi}{M}(\lambda+k))}e^{-ja(\lambda+k)} \\ &\quad - 0.5\Big(\frac{\sin(\pi(\lambda-1+k))}{\sin(\frac{\pi}{M}(\lambda-1+k))}e^{-ja(\lambda-1+k)} + \frac{\sin(\pi(\lambda+1+k))}{\sin(\frac{\pi}{M}(\lambda+1+k))}e^{-ja(\lambda+1+k)}\Big)\Big] \qquad \text{(E.11)}\end{aligned}$$

Résumé de la thèse en Français : Conception de relais de protection numérique innovants à base d'échantillons horodatés pour les réseaux intelligents

1 Introduction : les défauts dans les réseaux électriques

Les réseaux électriques consistent en l'implication de tous les équipements coopérant pour produire, transférer, distribuer et consommer l'électricité depuis les moyens de production jusqu'aux consommateurs les plus éloignées. Dans leur structure classique, la production d'électricité est rendue possible grâce aux grandes unités de production centralisées situées dans un petit nombre de sites. L'énergie électrique est d'abord transmise sur de longues distances grâce à un réseau de transmission haute tension fortement interconnecté. Ensuite, les réseaux de répartition alimentent les grands consommateurs industriels en haute tension. Enfin, les réseaux de distribution, principalement architecturés de manière radiale, sont destinées à fournir l'électricité aux utilisateurs passifs finaux en moyenne et basse tensions.

Grandes unités de production centralisées, transformateurs, lignes à haute tension, chacun de ces composants est conçu, quelquefois exploité et connecté entre eux pour fournir au consommateur la quantité exacte d'énergie électrique nécessaire à tout instant et de la manière la plus rentable possible. En effet, l'électricité ne peut généralement pas être stockée de manière efficace. Il est donc nécessaire d'assurer un équilibre entre la production et la consommation des puissances électriques à chaque instant. Dans le cas contraire, de graves pannes comme des événements en cascade conduisant à des pannes généralisées peuvent se produire. Il a été déterminé lors de l'incident de Aout 2003 aux Etats-Unis que le coût d'une panne d'électricité, bien que variable, peut atteindre 1% du produit intérieur brut (PIB) d'un pays. Dans les conditions normales de fonctionnement, les réseaux électriques n'opèrent que très rarement en régime établi parce que l'équilibre production-consommation n'est jamais parfait, la charge fluctuant par essence. Beaucoup d'autres situations habituelles se produisent dans les réseaux électriques entrainant des formes d'ondes de tensions et courants qui s'écartent du système triphasé équilibré parfait, comme par exemple, les opérations de commutation, les courants d'enclenchement générés par la mise sous tension des transformateurs, les charges asymétriques ou encore le démarrage de gros moteurs à induction.

Il peut arriver aussi des phénomènes extrêmes dans les réseaux. Ces situations catastrophiques sont dues à des influences internes ou externes qui ne peuvent être évitées. Parmi elles, les catastrophes climatiques, les accidents physiques, les défaillances des équipements, les dysfonctionnements résultant de l'erreur humaine illustrent quelques origines

de problèmes liés aux réseaux électriques. La plupart d'entre elles génèrent des défauts pouvant aller jusqu'à la destruction d'équipements, la perte de la stabilité du système, la mort d'êtres humains ou encore des pannes généralisées. Malgré le fait que les contrôles primaires, secondaires et tertiaires peuvent surmonter une majorité de problèmes d'instabilité, ils ne sont cependant d'aucunes utilités contre les perturbations qui dépassent les spécifications maximales de ces derniers.

2 Les relais de protection : dispositifs efficaces de lutte contre les défauts

Lorsque des conditions extrêmes, ou des défauts, se produisent, il est nécessaire d'impliquer des équipements particuliers dont le but est de détecter et de minimiser l'ampleur et la durée de la panne. L'un d'eux est appelé relais de protection et est défini comme un dispositif de calcul dont la fonction est de détecter les lignes défectueuses ou les équipements ou toute autre condition de nature anormale ou dangereuse se produisant dans les réseaux pour initier une action appropriée sur le circuit de commande du(des) disjoncteur(s) associé(s). Les relais de protection ne sont pas nécessaires en cas de fonctionnement normal des réseaux. Cependant, dès lors qu'un défaut se produit, leur utilisation devient nécessaire. Ces derniers ne peuvent pas empêcher les perturbations de se produire, mais réagissent plutôt à l'apparition du défaut. Ainsi, les relais de protection sont conçus pour détecter (ressentir) les défauts sur la base des modifications des niveaux/formes des courants et/ou les diminutions des niveaux de tensions qui, la plupart du temps, attestent d'une condition de défaut. En fait, la sensibilité est l'une des quatre exigences générales que chaque relais de protection doit remplir. Les trois autres sont désignées comme étant la sélectivité, la fiabilité et la vitesse de fonctionnement. Elles sont toutes expliquées ci-dessous :

La sensibilité est la capacité de réagir à de très faibles écarts des quantités mesurées après l'apparition du défaut.

La sélectivité représente l'aptitude à isoler uniquement les pièces défectueuses des réseaux des tronçons sains.

La fiabilité est la capacité de déclencher uniquement en cas de défaut pour éviter les phénomènes de déclenchement intempestif et d'isoler des tronçons sains du réseau.

La vitesse de fonctionnement est la capacité de réagir dans les plus brefs délais possibles.

Ces quatre exigences représentent les piliers de la conception d'un relais de protection. Il appartient au concepteur de privilégier un élément particulier, souvent au détriment des autres. Par exemple, la fiabilité et la vitesse de fonctionnement sont deux cibles à atteindre diamétralement opposées, si bien qu'un compromis entre ces deux critères est très souvent choisi. Le relais le plus fiable ne sera jamais utilisé s'il opère trop lentement suite à l'apparition d'un défaut parce que ce défaut pourrait conduire à endommager l'équipement avant que le relais ne réagisse. A l'inverse, le relais le plus rapide serait également inutilisable si les moindres perturbations du réseau provoquent des déclenchements intempestifs.

Aujourd'hui, les relais de protection sont largement déployés tant au niveau des réseaux de transport qu'au niveau des réseaux de distribution. Cependant, les algorithmes de protection mis en jeu sont différents et dépendent de la nature du réseau dans lequel le relais est installé. En effet, le réseau de transport, considéré comme l'épine dorsale du réseau électrique, est bien instrumenté en raison de son rôle spécifique dans l'équilibre production-consommation et les impératifs de stabilité et de sécurité de l'ensemble du réseau électrique. Outre les algorithmes de protection avancés, les réseaux de transport impliquent, la protection, la mesure, la surveillance et les technologies de contrôle-commande de pointe à la différence des réseaux de distributions, conçus avec une philosophie différente pour des raisons économiques intrinsèquement liées à leur caractère généralisé et distribué. Ainsi, les réseaux de transports sont protégés par des algorithmes de protection très complexes et quelquefois communicants. A contrario, et tout comme il existe un manque d'instrumentation sophistiquée dans les réseaux de distribution, ces derniers sont protégés avec des algorithmes de protection basiques. Néanmoins, l'architecture des réseaux de distribution est en train de changer pour s'adapter à la croissance rapide de la part de la production décentralisée au niveau de la distribution, qui non seulement rompt le découplage traditionnel entre transport et distribution, mais met l'accent sur la nécessité d'un système de protection avancée. La modernisation des réseaux de transport et de distribution d'électricité est la fondation des réseaux électriques intelligents où de nouveaux relais de protection seront la pierre angulaire pour faire face à des nouveaux paradigmes.

La première génération de relais de protection est née en 1905 et consistait en un appareil électromagnétique simple de surintensité et de sous-tension. Ensuite, l'invention des transistors en 1947 a rendu possible la mutation de la technologie électromécanique en statique, mise en service vers 1955. Vers 1980, avec l'avènement de l'informatique, la technologie utilisée pour construire de tels dispositifs a été considérablement améliorée et a conduit à l'ère des relais de protection numériques. Par rapport aux dispositifs statiques, les relais digitaux ont accès à la conversion analogique-numérique, aux microprocesseurs pour mettre en oeuvre leurs algorithmes de protection, et des fonctions de communication pour envoyer des informations à un ordinateur distant. Cependant, durant les cinq années suivantes, cette technologie a été remplacée par les relais numériques, souvent considérés comme le naturel développement des relais digitaux, principalement en raison de l'évolution très rapide des microprocesseurs. En particulier, ils utilisent un processeur de signal numérique (*Digital Signal Processor* - DSP) optimisé pour les applications de traitement du signal. De toute évidence, chaque changement de technologie a apporté avec lui des réductions de taille et de poids du dispositif, ainsi que des améliorations en termes de fonctionnalité et de fiabilité. Aujourd'hui, les relais numériques creusent l'écart par rapport aux technologies antérieures car ils offrent des caractéristiques remarquables telles que la capacité d'inclure un grand nombre d'algorithmes de protection, l'enregistrement des formes d'onde du réseau en cas de défaut, et la surveillance de l'état du disjoncteur.

Les relais numériques utilisent des techniques de traitement du signal pour détecter les conditions anormales de fonctionnement du réseau. Pour atteindre cet objectif, cinq opérations de base sont effectuées :

1. le filtrage des signaux d'entrée analogiques pour supprimer les composantes hautes fréquences corrompant les signaux numériques ;
2. l'échantillonnage et la conversion des signaux analogiques en échantillons par l'utilisation d'un convertisseur analogique-numérique (CAN) ;
3. le filtrage numérique des échantillons pour en extraire la composante fréquentielle exacte recherchée (fondamental ou harmonique) ;
4. la mesure des paramètres utilisés par les algorithmes de protection, comme l'amplitude et l'angle ;
5. les prises de décisions de protection fondées sur des critères de comparaison des valeurs mesurées avec des seuils prédéfinis ou d'autres caractéristiques.

3 Les nouveaux paradigmes des relais de protection

L'horloge interne du CAN peut être connectée à une source temporelle externe de sorte à synchroniser la mesure sur de grandes distances. Ce concept a été introduit en 1988 avec l'invention de l'unité de mesure de phaseur (*Phasor Measurement Unit* - PMU) par Arun G. Phadke et James S. Thorp à l'université Virginia Tech. La synchronisation des mesures rend possible la surveillance du réseau en temps réel et d'autres applications liées aux domaines de la stabilité et de la protection telles que la détection des oscillations de puissance, la détection d'îlotage et le système de protection adaptative sont également envisageable. C'est l'ère du système de mesure et de protection à zone étendue (*Wide Area Measurement and Protection System* - WAMPS) qui combinent des méthodes avancées de traitement numérique du signal avec des échanges rapides et fiables de données via des liaisons de télécommunication à plus ou moins grande distance pour détecter et continuer à lutter contre les instabilités du réseau.

Les technologies de communication font partie des piliers des réseaux intelligents pour gérer l'électricité d'une manière plus fiable, sûr et durable. Pour réduire les coûts d'installation et encourager la compétition entre les constructeurs de relais, il est nécessaire que les dispositifs de protection, de mesure et de contrôle des différents fournisseurs communiquent et se comprennent mutuellement. L'introduction d'une norme de communication standardisée, comme la norme CEI 61850 pour la communication inter et intra poste sources permet de résoudre ce problème. Parmi les services de communication offerts par la norme, les valeurs échantillonnées mesurées (*Sampled Measured Values* - SMV), encapsulées dans des trames de données Ethernet, remplacent les fils de cuivre traditionnels qui établissaient le lien entre les transformateurs de mesure et les dispositifs de protection, de mesure et de contrôle. L'utilisation de SMV apporte de nouveaux défis pour les appareils électroniques intelligents et des avancées scientifiques et techniques majeures sont nécessaires dans le domaine du traitement du signal pour traiter ces nouvelles trames SMV. C'est l'objectif de cette étude.

4 Vers un nouveau relais de protection pour les réseaux intelligents

L'estimation précise des phaseurs est le fondement des relais de protection et des PMUs. Pour les relais, les phaseurs sont fournis aux algorithmes de protection qui détectent les opérations anormales du système. Pour les PMUs, les mesures sont horodatées à un signal de synchronisation temporelle commun à tous les appareils qui permet, en croisant diverses mesures distantes ainsi synchronisées, d'obtenir une image cohérente de l'état du réseau. Ces mesures sont appelées phaseurs synchronisés, ou synchrophaseurs. Les synchrophaseurs assurent un moyen efficace de surveiller l'état de fonctionnement d'un réseau en temps réel. Ainsi un système de mesures à zone étendue (*Wide Area Measurement System* - WAMS) améliore sensiblement la fiabilité, l'observabilité, l'intégrité et la sécurité d'un réseau électrique. Quand un WAMS est associé aux fonctions de mesure, de protection et de contrôle, il est considéré comme un système de mesure, protection et contrôle à zone étendue (*Wide Area Measurement Protection and Control system* - WAMPAC). Les applications WAMPAC nécessitent le déploiement de plusieurs PMU à travers un nombre suffisant de noeuds du réseau électrique pour permettre une observabilité complète. Cependant, le coût moyen global des systèmes de synchrophaseur est un obstacle sérieux au déploiement à grande échelle des PMU si bien que les gestionnaires des réseaux de transport et de distribution sont à la recherche de solutions alternatives moins coûteuses. L'intégration de la fonction PMU dans les relais numériques déjà installés sur le réseau pour des besoins de protection en fait partie.

4.1 Problématiques liées aux méthodes de traitement du signal

La nature numérique des relais souligne qu'ils impliquent un processus d'échantillonnage pour permettre de calculer les phaseurs associés aux signaux présentés à leurs entrées. La stratégie d'échantillonnage diffère d'un appareil à un autre. En effet, l'horloge interne du PMU doit être synchronisé à une horloge atomique, telle que celles émettant des satellites de l'armée américaine, le Géo-Positionnement par Satellite (*Global Positionning System* - GPS), pour avoir la synchronisation temporelle, ce qui signifie que l'entrée est échantillonnée à intervalle de temps constant, et cet intervalle de temps sera la même pour tous les PMUs (voir Fig. E.1). Toutefois, échantillonner à pas fixe n'est généralement pas la solution préférée pour les relais de protection. En effet, cela peut introduire des erreurs dans leurs fonctions de protection, notamment dans l'estimation des phaseurs. Pour pallier ce problème, la plupart des relais de protection change la fréquence d'échantillonnage du CAN pour qu'elle soit synchronisée avec la fréquence réelle du réseau mesurée. Cela signifie que la fréquence d'échantillonnage varie en fonction de la fréquence du réseau (voir Fig. E.2). Enfin, la synchronisation par GPS n'est pas nécessaire pour les relais étant donné que ceux-ci sont autonomes et que les algorithmes de protection peuvent fonctionner sans elle. Néanmoins, elle devient obligatoire pour intégrer un algorithme de mesure de synchrophaseurs.

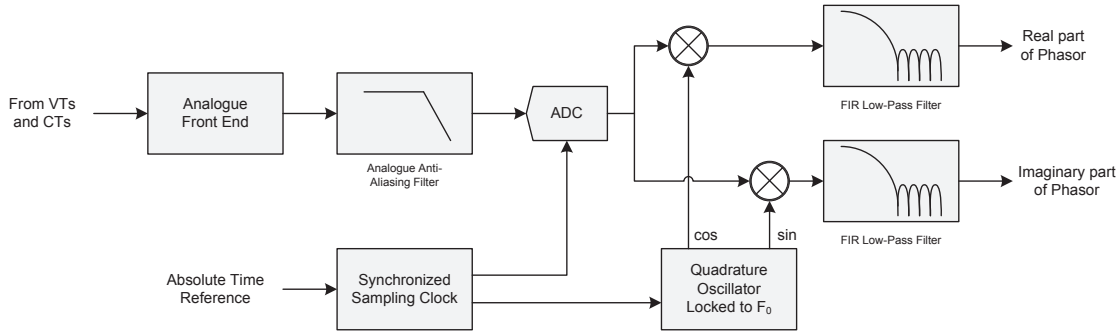

FIGURE E.1 – Principle d'échantillonnage à pas fixe appliqué au PMU

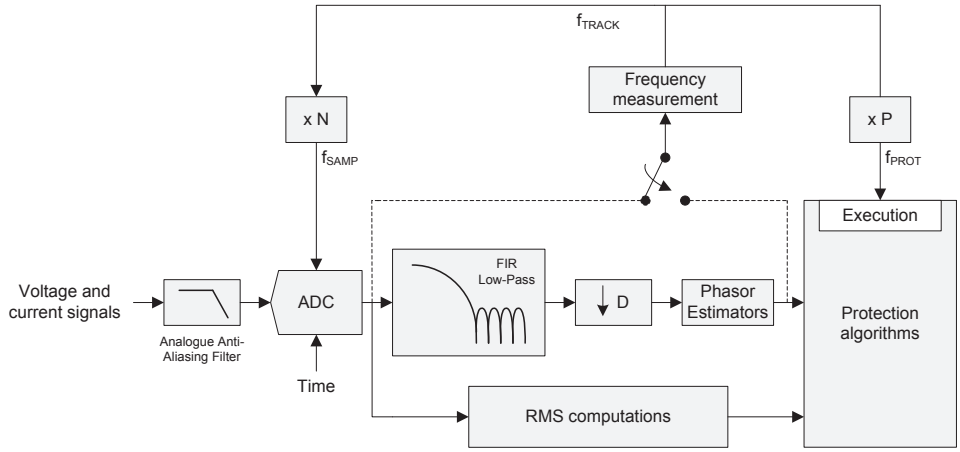

FIGURE E.2 – Principe d'échantillonnage à pas variable appliqué au relais de protection

Au vu de ce qui précède, la thèse commence par un état de l'art visant à décrire la principale méthode employée par les relais de protection numériques pour estimer les phaseurs. Cette méthode est connue sous le nom de Transformée de Fourier discrète (*Discrete Fourier Transform* - DFT). Néanmoins, le DFT souffre principalement de deux phénomènes pernicieux : le repliement de spectre et la fuite spectrale. Le premier introduit dans un signal échantillonné des fréquences qui ne devraient pas s'y trouver et engendre des distorsions spectrales. Ce phénomène a lieu lorsque la fréquence d'échantillonnage n'est pas supérieure à deux fois la fréquence maximale contenue dans le signal échantillonné. Le second phénomène, dit de fuite spectrale, se produit lorsque la fenêtre d'observation utilisée par la DFT ne contient pas un nombre entier de période du signal échantillonné. Dans ce cas, le signal observé présente des discontinuités par rapport aux formes d'ondes sinusoïdales conduisant à de mauvaises estimations de phaseurs. Les solutions mises en oeuvre par les relais de protection et les PMUs pour lutter efficacement contre les problèmes de repliement de spectre et de fuite spectrale sont également présentées. L'utilisation d'un filtre anti-repliement dans la chaîne d'acquisition permet de minimiser les effets du repliement spectral. En ce qui concerne la réduction des fuites spectrales, il existe des solutions distinctes en fonction du dispositif intelligent considéré, relais de protection ou PMU, puisque les stratégies d'échantillonnage mises en jeu sont différentes. En effet, une grande partie des relais échantillonnent typiquement à une fréquence synchronisée avec la fréquence du réseau (méthode de suivi de fréquence) pour résoudre le problème de fuite.

Au lieu de cela, les PMU prélèvent des échantillons à fréquence fixe synchronisée avec le GPS et utilise principalement trois méthodes pour réduire les fuites: DFT à fenêtre d'observation variable, méthode d'interpolation dans le domaine fréquence, et méthode de ré-échantillonnage temporelle. Le plus souvent, ces méthodes nécessitent la connaissance de la fréquence du réseau pour opérer. Dans ce contexte, les deux méthodes couramment utilisées ont été présentées, à savoir la technique de détection de passage à zéro et la méthode des phaseurs. La méthode des phaseurs est généralement la plus employée car elle repose sur le filtre de Fourier et tire ainsi parti de sa propriété de filtrage, contrairement à la technique de passage par zéro, sensible aux harmoniques et aux composantes continues qui sont redoutés dans le monde des protections.

4.2 Caractérisation des *Sampled Measured Values*

Le succès de la mise en oeuvre d'un algorithme d'estimation de phaseur est évidemment fonction de la robustesse de l'algorithme lui-même à calculer avec précision les phaseurs dans un environnement contraint. En outre, la chaîne d'acquisition est également de première importance puisqu'elle donne aux algorithmes de traitement du signal la représentation numérique de ses entrées analogiques. Classiquement, la chaîne d'acquisition fait partie intégrante du dispositif intelligent et est conçue en fonction des objectifs du fabricant dudit dispositif. Cependant, avec l'évolution des réseaux électriques qui utilisent des technologies de télécommunication de plus en plus complexe, les relais de protection et les PMUs ont besoin de reconsidérer la façon d'acquérir les signaux électriques. En effet, les ingénieurs spécialisés dans la protection des réseaux électrique ont maintenant à leur disposition une large gamme de nouvelles technologies de communication. Parmi elles, des protocoles de données normalisées ont été définies dans la famille de normes CEI 61850 pour permettre l'interopérabilité entre les différents relais numériques au sein de la sous-station. En particulier, la norme CEI 61850-9-2 a introduit le concept de bus local (*process bus*) qui permet la transmission de valeurs horodatées analogiques numérisées (SMV) à partir des transformateurs de mesure à des relais numériques par l'intermédiaire d'unité d'acquisition et de communication (*Merging Units* - MU) comme représenté sur la Fig. E.3. L'utilisation de *Merging Units* soulève néanmoins un point intéressant : le fabricant de relais n'est plus responsable de la chaîne d'acquisition. Auparavant, les erreurs introduites par la chaine d'acquisition sur les signaux d'entrée analogiques étaient connues et compensées par logiciel. Ainsi, les algorithmes de relais de protection étaient conçus pour compenser les approximations engendrées par la chaîne d'acquisition propriétaire. Aujourd'hui, la nouvelle génération d'algorithmes de traitement du signal doit être basée sur les échantillons à fréquence fixe produits par les *Merging Units* et codées sous format Ethernet pour faire face au paradigme des réseaux intelligents.

Cependant, la caractérisation des trames SMV est une étape importante et nécessaire en vue de concevoir de nouveaux algorithmes. La famille de normes CEI 61869 vise à caractériser, entre autres, la précision avec laquelle les *Merging Units* se doivent de coder les signaux présentées à leurs entrées. En effet, du point de vue du constructeur de relais, les *Merging Units* sont une sorte de boite noire puisque ses caractéristiques détaillées ne sont

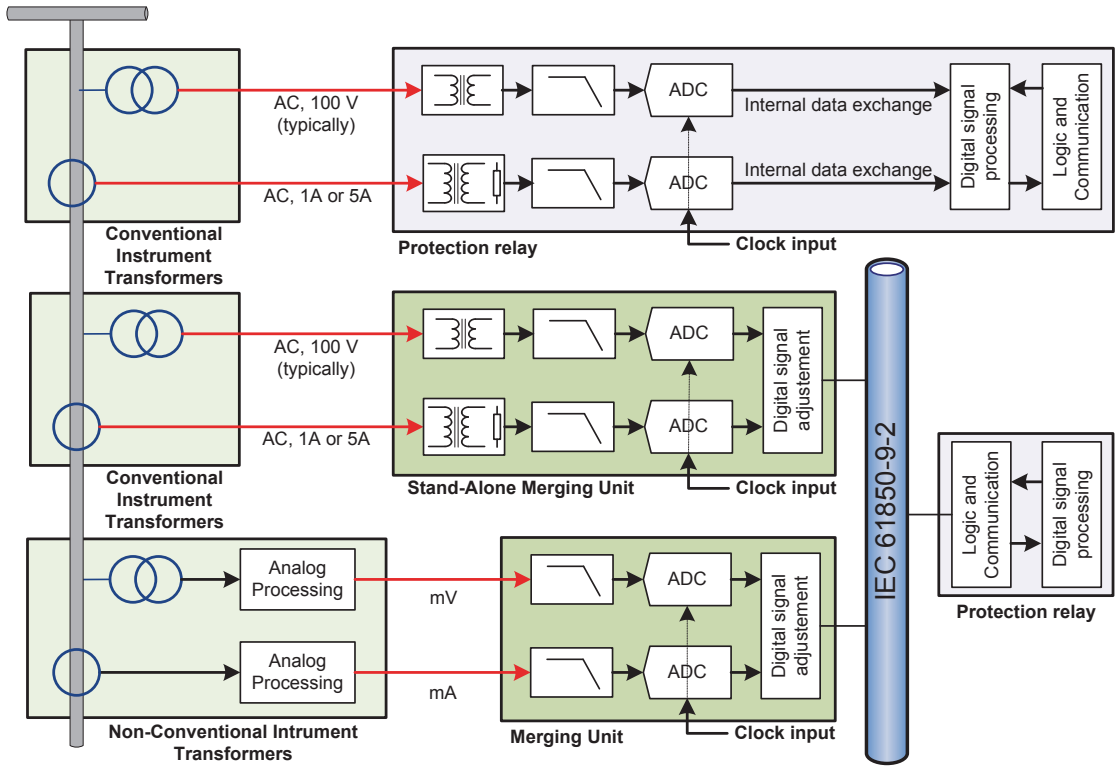

FIGURE E.3 – Concept de *Merging Unit* en comparaison avec les transformateurs de mesure conventionnels

pas définies. Par exemple, la réponse fréquentielle des *Merging Units* n'est pas connue, mais doit plutôt être comprise entre des limites imposées par la norme CEI 61869-6. Par conséquent, la compensation des erreurs introduites par les *Merging Units* ne peut pas être réalisée par les relais de protection ou autre dispositif intelligent. Pire encore, comme détaillé par la norme CEI 61869-13, les *Merging Units* sont autorisés à introduire des erreurs aléatoires bien que sujettes à des seuils imposés et de telles erreurs ne peuvent pas être compensées en raison de leur nature aléatoire. Ainsi, les erreurs liées à l'instrumentation impactent directement les algorithmes utilisés par les dispositifs intelligents en termes de précision. Par exemple, dans le cas du PMU, les synchrophaseurs doivent être estimées avec une erreur maximale de 1% suivant un critère normalisé (*Total Vector Error* - TVE). Et, puisque les *Merging Units* introduisent des erreurs de mesure, cela réduit la marge d'erreur que les algorithmes de PMU sont autorisés à introduire pour respecter le critère Total Vector Error. Les études menées dans le Chapitre II de la thèse ont mis en évidence le fait que, parmi les classes de précisions autorisées par la norme, uniquement 3 classes de précision de mesure peuvent convenir pour la mesure de synchrophaseur, avec une préférence pour la classe 0.1. De plus, la proposition de méthodes de traitement de signal pour la conception d'un *Merging Unit* de classe 0.1 a permis de conclure que le facteur déterminant dans ce type d'appareillage pour obtenir des mesures précises est la qualité des transformateurs de courants et de tensions situées à l'intérieur de ces équipements.

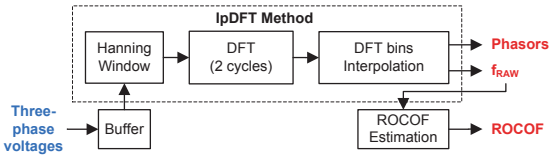

FIGURE E.4 – Méthode de DFT interpolé couplée à une fenêtre *Hanning* pour estimer les phaseurs, fréquences et dérivées de fréquence

4.3 Proposition d'algorithmes de traitement du signal sur la base de *Sampled Measured Values*

Dans le Chapitre III, trois algorithmes sont proposés pour estimer des phaseurs destinés aux fonctions de protection, dans des conditions statiques et/ou dynamiques, sur la base des trames SMV. Puisque ces trames sont produites à fréquence fixe, le phaseur calculé par méthode DFT sera faux lorsque la fréquence dévie du nominale. Ainsi, trois procédés d'interpolation différents sont proposés pour minimiser les erreurs introduites sur le phaseur dues au phénomène de fuite spectral. Deux d'entre eux ré-échantillonnent les signaux à une fréquence plus faible dans le domaine temporel et exigent la connaissance de la fréquence du réseau pour effectuer l'opération de décimation. La fréquence du réseau est suivie par le calcul de l'écart angulaire du phaseur de la composante directe la tension (méthode des phaseurs). Enfin, la dernière méthode d'interpolation proposée met en oeuvre des interpolations des raies du spectre obtenu par DFT et ne nécessite pas d'estimation de fréquence comme pré-requis.

Le premier algorithme du domaine temporel, appelé i-SVA, modifie l'amplitude des échantillons pour générer une séquence d'échantillons dont la fréquence est synchronisée avec la fréquence du réseau. Pour atteindre cet objectif, une interpolation cubique est réalisée sur les échantillons d'entrée. Le second algorithme du domaine temporel repose sur le processus d'interpolation linéaire et de sous-échantillonnage. Contrairement à la méthode d'interpolation i-SVA, ce second algorithme génère un nouveau flux d'échantillons dont les horodatages correspondent à ceux obtenus en cas d'échantillonnage synchrone à la fréquence du réseau. Le dernier algorithme proposé est fondé sur les méthodes de DFT interpolées couplées à une fenêtre de pondération *Hanning*. Il utilise les échantillons provenant du bus de procédé directement, sans décimer le signal, puisque l'algorithme nécessite un taux d'échantillonnage élevé pour donner des résultats précis. En plus de l'estimation du phaseur, la DFT interpolée est en mesure de fournir une estimation de fréquence en même temps (voir Fig. E.4).

Les algorithmes i-SVA et interpolation linéaire ont été couplés avec un algorithme d'estimation de fréquence formant un système en boucle fermée. L'analyse a démontré qu'un tel système est confronté à des problèmes de précisions lorsque des rampes de fréquence sont appliquées si la méthode de ré-échantillonnage est réalisée de manière chronologique. En effet, chaque fois que la fréquence d'échantillonnage est ajustée en fonction de la fréquence du réseau estimée, il suit immédiatement une période transitoire pendant laquelle

les mesures de fréquence brutes sont fausses conduisant à des estimations de dérivée de fréquence également erronées. Les fonctions de protection liées à ces estimations de fréquence et de dérivée de fréquence peuvent émettre des déclenchements intempestifs, ce qui est inacceptable. Dans ce contexte, un nouveau principe de suivi de fréquence a été proposé. Il repose sur le calcul rétroactif d'échantillons et rend insensible la méthode de mesure de fréquence aux changements de la fréquence d'échantillonnage. Les deux algorithmes sont representés sur les Figs. E.5 and E.6 ci-dessous.

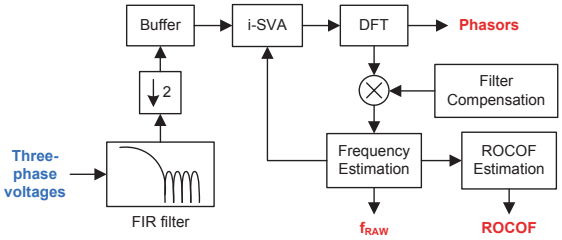

FIGURE E.5 – Méthode i-SVA pour estimer les phaseurs, fréquences et dérivées de fréquence

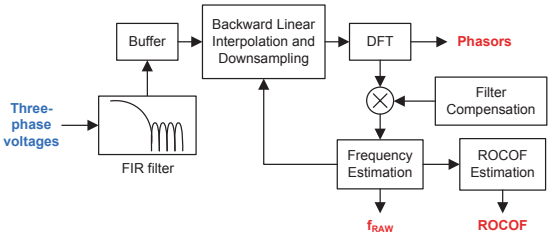

FIGURE E.6 – Méthode interpolation linéaire rétroactive pour estimer les phaseurs, fréquences et dérivées de fréquence

Une vaste gamme de modèles de signaux a été utilisée pour tester les trois solutions proposées dans des conditions statiques et/ou dynamiques en mettant l'accent sur les excursions de fréquence. Les cas de test comprennent :

— des signaux en régime établi, corrompus par les harmoniques, et à fréquence hors-nominale ;
— des rampes de fréquence lente et rapide ;
— et un saut de fréquence.

Quelle que soit la méthode utilisée, les algorithmes de mesure de fréquence et de dérivée de fréquence ont montré des comportements pratiquement similaires avec de bonnes précisions. Cependant, les préférences sont données pour la solution d'interpolation linéaire et de sous-échantillonnage rétroactive car la vitesse de suivi de fréquence est plus rapide que les deux autres méthodes. Le principal problème a été détecté pour l'estimation de la dérivée de fréquence pour le cas de test du saut de fréquence avec des valeurs pouvant atteindre 200 Hz/s. Pour l'estimation des phaseurs, la solution fondée sur l'algorithme d'interpolation linéaire rétroactive reste néanmoins la plus précise dans la plupart des cas testés.

4.4 Proposition d'un algorithme de mesure de synchrophaseurs intégré dans le traitement du signal initial

Comme le traitement du signal fondé sur l'interpolation linéaire rétroactive permet d'obtenir des mesures de phaseurs, de fréquence et de dérivée de fréquence précises, il a été utilisé comme point de départ pour concevoir un algorithme de synchrophaseur dans le Chapitre IV. Cet algorithme prend avantage de certains calculs déjà effectués pour les

fonctions de protection de manière à intégrer et fusionner l'algorithme d'estimation de synchrophaseurs dans le traitement du signal de base. En faisant cela, la puissance nécessaire pour faire fonctionner l'algorithme de calcul de synchrophaseur est minimale. Le point le plus important pour une intégration réussie de l'algorithme de synchrophaseur est la synchronisation entre l'instant de calcul des algorithmes de traitement du signal dédié aux fonctions de protection et celui dédié aux synchrophaseurs. Pour faire simple, l'échantillon horodaté à l'instant de mesure du synchrophaseur doit être pris tel qu'il est pour conserver l'information d'angle absolue. Une fois que ceci est effectué correctement, les estimations de synchrophaseur, fréquence, et dérivée de fréquence peuvent être calculées avec un taux de déclaration de 200 trames par seconde pour un système de 50 Hz et de 240 trames par seconde pour un système de 60 Hz, soit deux fois plus élevé que les taux de déclaration définies dans la dernière version de la norme PMU. L'ensemble de la solution a été testée par simulation en utilisant les cas de test définis dans la norme PMU avec un taux de déclaration de 200 trames par seconde. Les résultats de simulation obtenus ont démontré que la solution complète de traitement de signal proposée fait face aux exigences de mesure de la norme PMU en termes de précisions de calcul de synchrophaseur, fréquence, et dérivée de fréquence.

5 Conclusions et perspectives

La solution de traitement du signal fondée sur l'interpolation linéaire rétroactive présentée dans cette thèse a été caractérisée, modélisée et validée dans un environnement de simulation dans un premier temps. Par conséquent, les perspectives d'avenir à court terme sont liées à un déploiement possible des algorithmes proposés dans un relais de protection réel ayant des trames SMV comme signal d'entrée. L'objectif de cette mise en oeuvre est de valider à la fois le nouvel algorithme de suivi de fréquence et l'algorithme de synchrophaseur. Pour ce faire, le simulateur temps-réel RTDS peut être utile car il est capable de simuler de nombreux concepts liés aux réseaux intelligents et aux énergies renouvelables. Par exemple, il peut agir comme *Merging Unit* et peut également simuler la production décentralisée. Une fois que le réseau de distribution a été modélisé, le relais de protection capable de calculer des synchrophaseurs et ayant des trames SMV comme signal d'entrée pourra être connecté au simulateur afin d'effectuer des essais temps-réel en boucle fermée.

La performance du nouveau principe de suivi de fréquence peut être évaluée à l'aide d'une fonction de protection reposant sur la mesure de la dérivée de fréquence pour détecter les situations d'îlotage. L'idée est de comparer les performances obtenues avec l'algorithme de suivi de fréquence classique et ceux obtenus avec le nouvel algorithme à l'aide de deux relais différents ; chacun utilisant une stratégie de suivi de fréquence différente. Aujourd'hui, le prototype a été validé, les algorithmes ont été traduis en code source et implémentés dans le relais. Néanmoins, la partie logicielle doit être modifiée pour permettre l'extraction des valeurs de fréquence et de dérivée de fréquence calculées par le prototype.

Pour l'algorithme de mesure de synchrophaseurs, les cas de test imposés par la norme peuvent être simulés avec le RTDS et les formes d'onde associées directement injectées

dans le relais en utilisant des trames SMV. Les estimations peuvent être stockées en mémoire et extraites pour comparaison avec les valeurs théoriques de synchrophaseurs.

La validation du comportement des algorithmes proposés en condition temps-réel constitue une perspective à plus long terme. Plus précisément, les algorithmes peuvent être mis en oeuvre dans la prochaine génération de relais de protection en cours de développement dans l'entreprise dont les caractéristiques peuvent faire face aux nouveaux défis de demain, principalement liés à la grande pénétration des générations distribuées dans le réseau de distribution. En particulier, les mesures plus précises de fréquence et de dérivée de fréquence devraient permettre d'améliorer la détection d'îlotage et éviter les déclenchements intempestifs. Enfin, l'algorithme de calcul de synchrophaseur proposé peut être utilisé dans le réseau de distribution pour l'échange de données rapide entre les protections permettant d'améliorer leur temps de réponse. Par exemple, les opérations plus rapides des fonctions de ré-enclenchement peuvent être obtenues avec des mesures d'angle absolu, ce qui réduit les inconvénients liés aux interruptions momentanées d'alimentation.

INNOVATIVE NUMERICAL PROTECTION RELAY DESIGN ON THE BASIS OF SAMPLED MEASURED VALUES FOR SMART GRIDS

Abstract: With the Smart Grid paradigm, protection engineers now have available to them a large range of new communication technologies. Among them, IEC Standard 61850-9-2 has introduced the process bus concept which permits sending of absolute time-stamped digitized analogue values from the instrument transformers of the field to numerical relays. The latter can incorporate the phasor measurement unit function which can be used for exchanging synchrophasors between protection functions and for new anti-islanding protection. Frequency and rate-of-change-of-frequency relays are, nowadays, the most commonly employed anti-islanding methods but their performance is not satisfactory. In this context, a new generation of signal processing techniques for protection relays having time-stamped digitized analogue values as input signal with synchrophasors measurement capability is required. This thesis first studies the impact of sampled measured values on the signal processing. Three solutions are then proposed to compute phasor, frequency and rate-of-change-of-frequency estimates under various static and dynamic conditions, and tested via simulation. Finally, a synchronized phasor measurement algorithm incorporated into the initial signal processing is proposed. This algorithm has been tested following the latest version of the phasor measurement unit standard and the results obtained comply with the measurement requirements.

Key words: Protection Relay; Phasor Measurement Unit; Signal Processing; IEC 61850; Frequency Estimation; Rate-of-Change-of-Frequency Estimation

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CONCEPTION DE RELAIS DE PROTECTION NUMERIQUE INNOVANTS A BASE D'ECHANTILLONS HORODATES POUR LES RESEAUX INTELLIGENTS

Résumé : Avec le paradigme réseau intelligent, les ingénieurs de protection ont maintenant à leur disposition une large gamme de nouvelles technologies de communication. Parmi elles, la norme CEI 61850-9-2 a introduit le concept de bus de procédé qui permet l'envoi de valeurs échantillonnées horodatées à un temps absolu depuis les transformateurs de mesure du terrain jusqu'aux relais de protection numériques. Ces derniers peuvent intégrer la fonction d'unité de mesure de phaseur qui peut être utilisé pour échanger des synchrophaseurs entre les fonctions de protection et pour une nouvelle protection anti-îlotage. Les relais de fréquence et de dérivée de fréquence sont, de nos jours, les méthodes anti-îlotage les plus couramment employées, mais leurs performances ne sont pas satisfaisantes. Dans ce contexte, une nouvelle génération de techniques de traitement du signal pour les relais de protection ayant des échantillons horodatées comme signal d'entrée et intégrant la mesure de synchrophaseurs est nécessaire. Cette thèse étudie d'abord l'impact des valeurs échantillonnées sur le traitement du signal. Trois solutions sont ensuite proposées pour calculer les phaseurs, les fréquences et les dérivées de fréquence dans diverses conditions statiques et dynamiques, puis testées par simulation. Enfin, un algorithme de mesure de synchrophaseurs incorporé dans le traitement de signal initial est proposé. Cet algorithme a été testé par simulation selon la dernière version de la norme d'unité de mesure de phaseur et les résultats obtenus sont conformes aux exigences de mesure.

Mots clé: Relais de Protection; Unité de Mesure de Phaseur; Traitement du Signal; CEI 61850; Mesure de Fréquence ; Mesure de Dérivée de Fréquence

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