Conception et implémentation d'algorithmes de traitement numérique de réception pour le lien UWB dans les réseaux BAN

Houcine Chougrani

UNIVERSITE
BRETAGNE
LOIRE

THÈSE / Télécom Bretagne
sous le sceau de l'Université Bretagne Loire

pour obtenir le grade de Docteur de Télécom Bretagne
En accréditation conjointe avec l'Ecole Doctorale Sicma
Mention : Sciences et Technologies de l'Information et de la Communication

présentée par
Houcine Chougrani

préparée dans le département Electronique
Laboratoire Labsticc

Conception et implémentation d'algorithmes de traitement numérique de réception pour le lien UWB dans les réseaux BAN

Thèse soutenue le 08 juillet 2016
Devant le jury composé de :

Sylvain Bourdel
Professeur, Grenoble INP / président

Geneviève Baudoin
Professeur, ESIEE – Noisy le Grand / rapporteur

Laurent Fesquet
Maître de conférences (HDR), Grenoble INP / rapporteur

Jean Schwoerer
Directeur de programme de recherche, Orange Labs – Meylan / examinateur

Pierre-Henri Horrein
Maître de conférences, Télécom Bretagne / examinateur

Amer Baghdadi
Professeur, Télécom Bretagne / directeur de thèse

Benoit Denis
Ingénieur de recherche, CEA-Leti – Grenoble / invité

N ° d'ordre : 2016telb0405

Sous le sceau de l'Université de Bretagne Loire

Télécom Bretagne

En accréditation conjointe avec l'École Doctorale Sicma

Conception et implémentation d'algorithmes de traitement numérique de réception pour le lien radio UWB dans les réseaux BAN

Thèse de Doctorat

Mention : STIC (Sciences et Technologies de l'Information et de la Communication)

Présentée par **Houcine Chougrani**

Département : Electronique

Laboratoire : Lab-STICC Pôle : CACS

Directeur de thèse : **Amer Baghdadi**

Soutenue le *08 juillet 2016*

Jury :

Mme. Geneviève Baudoin,	Professeur à l'ESIEE	Rapporteur
M. Laurent Fesquet,	Maître de Conférences HDR à Grenoble INP	Rapporteur
M. Sylvain Bourdel,	Professeur à Grenoble INP	Examinateur, Président
M. Jean Schwoerer,	Directeur de programme de recherche à Orange Labs	Encadrant
M. Pierre-Henri Horrein,	Maître de Conférences à Télécom Bretagne	Encadrant
M. Amer Baghdadi,	Professeur à Télécom Bretagne	Directeur de thèse
M. Benoit Denis,	Ingénieur de recherche - Chef de projet au CEA-Leti	Examinateur Invité

Contents

List of Figures

List of Tables

Acknowledgements

The achievements of this PhD thesis could not have been accomplished without the guidance of my advisors Amer, Jean, and Pierre-Henri. I would like to express my sincere appreciation to them for giving me the opportunity of following my PhD work, for their encouragements and availability throughout the three years of my stay, for their insightful direction, for their patience, and for their total support. I consider myself to be truly fortunate to have had the opportunity to work so closely with such talented persons.

I would like to express my gratitude for all the members of the jury, my reviewers Prof. Geneviève Baudoin and Prof. Laurent Fesquet for dedicating part of their valuable time to evaluate my work. I appreciate their insightful remarks and valuable questions that helped me to build a bigger picture of the perspectives of the achieved results.

I would like to dedicate the achievements of this work to my parents, Houria and Abdelkader, and my wife Khadidja who always believed in me. I also express my gratitude for their total and unlimited support and for being always there for me. I would like to thank all my siblings and close relatives for their constant encouragements and patience.

I take this opportunity to thank all my colleagues and friends at Orange Labs that I have known during my three years stay. I recall many moments where we have shared many constructive discussions and great laughters.

Finally, I would like to express my appreciation towards all engineers and partners within the RUBY project. Many thanks as well, to all the people with whom I have worked directly or indirectly.

Introduction

THE last few years have seen an increased interest in the research of practical and efficient implementations for impulse radio ultra wideband (IR-UWB) systems. One of the main recent drivers for this interest is the introduction in 2012 of the IEEE 802.15.6 standard for wireless Body Area Networks (BAN). A very wide range of applications is foreseen as the standard targets short-range wireless devices for in-body, on-body, and around-the-body communications. Besides the very significant medical and healthcare application domain, the standard offers a huge opportunity for non-medical applications [3] belonging to a variety of fields including personal audio or video, gaming, entertainment, wearable computing, ambient intelligence, and many others. These different application domains and the related communication scenarios lead to different technical requirements and challenges that need to be met through efficient implementations: (1) very low power consumption as some applications require devices with battery life of several months or even several years, (2) minimal short range, (3) variable data rate, (4) small factor form allowing portability of BAN devices, and (5) robust communication quality between the BAN devices.

IEEE 802.15.6 standard for wireless BAN

The IEEE 802.15.6 standard, published in February 2012, aims to provide an international standard for low power, short range, and extremely reliable wireless communication within the surrounding area of the human body. It specifies a vast range of data rates for different applications which can be either medical or non-medical. The standard defines a Medium Access Control (MAC) layer and three Physical (PHY) layers: (1) body channel communication for signal propagation on the skin surface, (2) narrowband PHY mainly for healthcare applications using the various available license free band, and (3) ultra wideband (UWB) PHY able to address higher data rates. The selection of each PHY layer depends on the application requirements.

UWB technology, and particularly IR-UWB which is the focus of this thesis work, presents significant advantages to address the large span of BAN applications compared to narrowband solutions in industrial scientific medical (ISM) bands. This radio technology consists in sending short pulses in time domain, and thereby spreading the energy over a large bandwidth ($>$ 500 MHz) in frequency domain. It allows high robustness in case of narrowband fades, protection against ISM band interferers, bit rate scalability from 400 kbps to 12.6 Mbps with the same hardware, ultra low radiated power well below -10 dBm, and to its potential for ultra low power implementations. The specification of the UWB PHY layer in IEEE 802.15.6 standard opens new opportunities both in terms of implementation and communication performances.

RUBY research project

In the context of the IEEE 802.15.6 standard for wireless BAN, a French collaborative research project, namely *RUBY* (Radio UWB for BodY area network), has been initiated (*years 2012 to 2015*). This project is coordinated by Orange Labs, and constitutes the main framework of the proposed contributions in this thesis. In addition to Orange Labs, several academic and industrial partners were involved in RUBY project (CEA-Leti, Thales Communications & Security, IM2NP and LEAT CNRS laboratories).

The goal of the project is to propose and implement an innovative IR-UWB system that will be particularly suited to BAN applications. The original idea is based on the proposal of an hybrid architecture that combines coherent and non-coherent receivers (Figure 1) in order to compensate the weaknesses of one by the forces of the other and vice versa. The coherent receiver exploits both the amplitude and the phase information to detect the signal whereas the non-coherent one exploits only the amplitude information.

In fact, as the IEEE 802.15.6 PHY frame structure specifies very short preamble, the synchronization cannot be achieved by serial-parallel search as would performs a coherent receiver with low frequency analog-to-digital converter (ADC) which requires long preamble [4]. On the other hand, as the non-coherent receiver structure provides fast sampling (< 2 ns) of the received signal [5], the capture of a complete channel impulse response (CIR) is ultimately possible within a single preamble symbol, and thus a rapid synchronization and channel estimation can be quickly acquired.

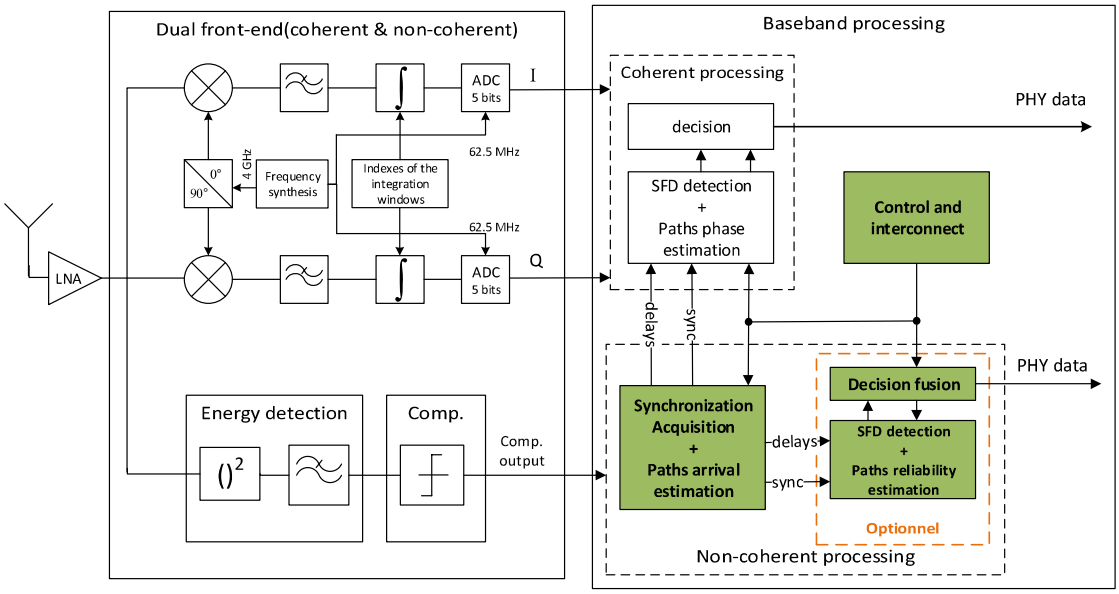


Figure 1 — Dual receiver architecture as proposed in RUBY project

Practically, the target hybrid (or dual) architecture performs preamble detection, synchronization and initial channel estimation in a very short time using a low-complexity low-power non-coherent front-end, and then moves to a higher sensitivity coherent front-end which completes the channel estimation and performs high data rate symbol detection and demodulation.

RUBY project aims to design a complete IR-UWB communication system, including all

analog and digital processing components. This includes an innovative radio frequency (RF) dual front-end integrated in single chip transceiver, very constrained analogue to digital conversion, event-driven digital baseband who will be able to efficiently drive the new RF front end, and miniaturized UWB antenna designed to be used in the close vicinity of a human body. The RF circuits and baseband designed during the project are planned to be integrated into a real hardware prototype that will demonstrate over-the-body wireless video streaming from a worn mass storage device to a video glasses display.

In this context, signal synchronization is a very hard task to accomplish. This is true in any communication system, and particularly in IR-UWB systems. In fact, the extremely low-power and narrow pulses of the IR-UWB signals require very accurate time acquisition, since even a slight misalignment (lack of energy capture) can severely degrade the system performance.

Furthermore, the very large bandwidth that dispose the IR-UWB signals allows the separation and the characterization of a large number of echoes or *paths* (high resolution power) due to the multipath propagation phenomena. The exploitation of these echoes offers a diversity gain, and enhances therefore the receiver performance. As for synchronization, having an accurate channel estimation can be quite complex task in IR-UWB systems.

Previous related research activities at Orange Labs

Several research activities have been conducted at Orange Labs on the topic of IR-UWB communication systems. The thesis of Jean Schwoerer [6], *years 2002 to 2005*, was the first initiative in this context. The objective was to specify an IR-UWB PHY layer in low data-rate context and to study the issues of signal detection and synchronization acquisition. The outcome was the proposal of (1) a very low-complexity non-coherent receiver based on energy detection over a very short time and (2) an original algorithm to acquire synchronization between the receiver and transmitter. Firstly, the proposed receiver relies on comparing the collected energy during a pulse-time ($<$ 2ns) and then comparing it to a prefixed threshold to decide the presence or absence of signal in asynchronous manner. Secondly, the proposed synchronization algorithm exploits a specific preamble structure composed from non modulated symbols. The idea is based on comparing the arrival of the received pulses with the temporal distances in the preamble symbol.

This research activity has been continued then through the thesis work of Jérémy Hamon [7], *years 2006 to 2009*, to investigate the use of asynchronous logic design in the implementation of the proposed synchronization algorithm. The idea was, on one hand to match with the asynchronous aspect of the aforementioned non-coherent receiver, and on other hand to decrease the dynamic power consumption thanks to intrinsic feature of asynchronous logic design. Moreover, the absence of clock signal in asynchronous circuits allows low electromagnetic noise, which is beneficial when processing low power signals as the IR-UWB ones. The time basis needed to process the IR-UWB signals was ensured by using a looped asynchronous structures, called *asynchronous rings*.

In the same period, another thesis work (Benoît Miscopein [8], *years 2007 to 2010*) has been initiated to enhance the performances of the proposed non-coherent IR-UWB receiver. The idea was to exploit the multipath diversity of the UWB channel in the demodulation of On-Off Keying

(OOK) IR-UWB modulated signals. The proposed method relies on fusion and recombination of different paths by computing their sum, weighted by their reliability. The obtained results illustrated significant improvement and the possibility to reach a performance level close to the optimal receiver.

Indeed, the low-complexity non-coherent receiver proposed in the previous works at Orange Labs is used to design the non-coherent front-end in the RUBY project. However, the previous proposed synchronization algorithm is not applicable as it is based on specific preamble structure which is not compliant with the one defined in IEEE 802.15.6 standard. Therefore, specific adaptations should be proposed.

Similarly, in order to complete the non-coherent reception chain, a demodulation algorithm supporting the Pulse Position Modulation (PPM) specified in the standard is required. In this regard, the use of a multipath process with weighted coefficients has shown its efficiency in [8]. However, a practical low-complexity approach to calculate the weighted coefficients is still missing and needs further investigations.

Finally, the proposal of low-complexity digital baseband architectures that implement efficiently the new non-coherent standard-compliant reception techniques constitutes a crucial requirement in order to build a complete hardware proof-of-concept. The available literature in this regard is rather scarce. Such validation target is highly valuable to demonstrate the feasibility of IR-UWB systems in real channel conditions encountered in BAN applications.

Objectives and scope of the thesis

In the above described context, the objective of this thesis work is to propose, implement, and validate through system simulations and hardware experimentations a complete non-coherent IR-UWB baseband receiver for BAN applications. The proposed techniques should be compliant with the recent IEEE 802.15.6 standard.

In the context of the RUBY research project targeting a hybrid coherent/non-coherent receiver architecture, the first objective of this thesis work is to propose a non-coherent flexible and rapid synchronization algorithm which can address any of the IR-UWB preambles specified in the IEEE 802.15.6 standard. Then, the second objective is to propose an efficient channel estimator to provide the channel impulse response to the coherent receiver. The remaining processing (symbol detection and demodulation) is done by the coherent part of the receiver in the context of the RUBY project, targeting high data rate BAN applications. This part is out of the scope of this thesis.

However, in case of low data rate applications, it can be envisaged to use only the non-coherent receiver and to switch off the coherent front-end and related database processing which will lead to significant energy saving. However this requires to complete the non-coherent baseband reception chain by proposing a non-coherent demodulation algorithm as well as a technique to detect the Start-of-Frame Delimiter (SFD) which is used to determine the starting of the data field in the IEEE 802.15.6 PHY frame. This represents an additional objective which we decided to explore in the scope of this thesis, beyond the objectives of the RUBY project.

Finally, one of the main objectives of this work is to propose low-complexity digital baseband architectures that implement efficiently all the proposed algorithms. The ultimate objective

is to build a complete real-time hardware demonstrator that implements a complete non-coherent IR-UWB receiver and than manages the interconnection between this non-coherent receiver and the combined coherent one.

Thesis contributions

Towards the above mentioned objectives, the contributions of this thesis work can be summarized in algorithmic domain and hardware implementation domain as follows:

Contributions in algorithmic domain:

Non-coherent IR-UWB baseband algorithms for BAN applications:

- Proposal and design of a flexible and rapid synchronization technique which targets IEEE 802.15.6 standard, with possibility to address other preambles.
- Proposal of a simple SFD detection technique that can, in addition to detecting the starting of data field, estimate the error probability of the received signal. This technique allows to have an alternative metric of the signal energy that the system can not estimate.
- Proposal of a path selection estimator which is used both for detecting the multipath components and the estimation of their reliability.
- Proposal of a fusion decision algorithm which supports PPM modulation scheme.
- Testing and validating the whole non-coherent baseband through system simulations using the IEEE 802.15.6 BAN channel models.

Contributions in hardware implementation domain:

Hardware implementation and prototyping of the proposed non-coherent baseband:

- Proposal and design of low-complexity architectures that implement the proposed synchronization and SFD detection techniques.
- Proposal and design of an optimized parallel architecture that implements the proposed path selection estimator.
- Proposal and design of a low-complexity architecture that implements the proposed fusion decision technique.
- Integration and on-board validation of the proposed architectures for synchronization and path selection estimation in a complete IR-UWB real-time hardware prototype. Successful experiments and measures were conducted with real wireless transmissions and channel conditions.

Manuscript Outline

This thesis manuscript is composed of four chapters as follows:

Chapter 1 provides an overview of the UWB technology and its evolution over time, as well as an overview of the main concepts and architectures of IR-UWB communication systems. This is done first by presenting the historical context of UWB, by highlighting its regulations worldwide, its benefits that have pushed its standardization, and the development of its applications. After this introduction, current state-of-the-art techniques for baseband processing are presented. These techniques encompass transmitter and receiver sides of the UWB links, and serve as basis for the presented contributions in this PhD thesis. In order to provide a comprehensive introduction to the work described in this manuscript, the chapter presents then the UWB PHY layer as specified in the RUBY project, along with the different use cases defined in this project. Finally, the channel models for the considered transmission system are described.

Chapter 2 presents the PhD thesis contributions related to the proposal of non-coherent IR-UWB baseband algorithms for BAN applications. The proposed algorithms are compliant with IEEE 802.15.6 standard and target the requirements of RUBY project, as described in Chapter 1. In order to implement a non-coherent receiver, several issues must be solved. Towards this target, the chapter presents first a flexible and efficient synchronization algorithm based on inter-pulse time interval detection. Then, a simple SFD detection technique that relies on a correlation method is presented. In addition to detecting the starting of data field, the proposed technique enables to estimate the error probability of the received signal. Furthermore, an efficient path selection estimator is proposed and used both for detecting the multipath components and the estimation of their reliability by exploiting the resolution of the adopted non-coherent receiver. Finally, the chapter introduces a fusion decision algorithm based on multipath processing and supporting PPM modulation scheme. The achieved performance of each proposed algorithm is evaluated independently, and then the whole non-coherent baseband is simulated using the IEEE 802.15.6 BAN channel models.

Chapter 3 presents the thesis contributions related to hardware architecture design of non-coherent IR-UWB baseband receiver. It regroups the different proposed low-complexity architectures that implement the algorithms presented in the previous chapter for synchronization, SFD detection, path selection and fusion decision algorithm based on multipath processing. The chapter starts by providing an overview of the target digital baseband transceiver and the related interfaces with the radio frequency front-end and the application board. Then for each proposed architecture a detailed description is provided. This includes the defined input/output signals, the main constituent components, and the control unit as a finite state-machine that schedules the different operations of the proposed architecture. The chapter presents in addition the design of a serial-to-parallel converter to handle the high speed input data stream, together with a global control unit for operation scheduling. The proposed complete digital baseband has been implemented targeting a Xilinx Spartan 6 FPGA. The chapter ends with the presentation of the results in terms of required logic resources that illustrate the hardware efficiency of the proposed architectures.

Chapter 4 presents the last major contribution of this thesis work regarding on-chip prototyping and the integration of the proposed architectures into a real hardware demonstration platform. This demonstration platform has been developed in the context of the research project

RUBY. It consists of an FPGA-based board that integrates the proposed architectures described in the previous chapters, a radio frequency board implementing the analog front-end, and a microcontroller-based application board. The chapter presents first the context and the general architecture of the proposed hardware demonstration platform. Then, detailed description of the different constituent boards and test environment is provided. Finally, measured performance results under real wireless transmissions and channel conditions are presented and discussed.

CHAPTER

1 Impulse Radio UWB communication systems

THE Impulse Radio Ultra Wide Band (IR-UWB) communication technique is characterized by radiating short pulses in the time domain, and thereby spreading the energy over a wide bandwidth in frequency domain. This characteristic leads to new constraints in the design and the hardware implementation of IR-UWB communication systems compared to the widely used narrowband communication systems.

This first chapter provides a historical overview of the UWB technology and its evolution over time, as well as an overview of the main concepts and architectures of IR-UWB communication systems. This is done first by presenting the historical context of UWB, by highlighting its regulations worldwide, its benefits that have pushed its standardization, and the development of its applications. After this introduction, current state-of-the-art techniques for baseband processing are presented. These techniques encompass transmitter and receiver sides of the UWB links, and serve as basis for the presented contributions in this PhD thesis. In order to provide a comprehensive introduction to the work described in this manuscript, the chapter presents then the UWB PHY layer as specified in the RUBY project, along with the different use cases defined in this project. Finally, the channel models for the considered transmission system are described.

1.1 Context and evolution of UWB

1.1.1 Impulse communication & ultra wideband signals historic

Although the denominations "Ultra WideBand" (UWB) and "Impulse Radio" (IR) are recent, IR communications can be seen as the first transmitted wireless signal. This goes back to the last century, when *Marconi* used his spark-gap (pulsed signals of 500 kHz) to communicate over 13 km between Lavernock (Wales) and Brean (England) in 1897. However, narrow band communication was then preferred, since its limited bandwith eases signal processing, and simplifies the control and regultation of government agencies.

More recently, in the 60s, UWB was once again considered as an alternative, with pioneering work done by Dr. Gerald Ross at the Sperry Research Center and Dr. H.F. Harmuth at Catholic University of America [9]. In 1973, the Ross and Robbins patents pioneered the use of UWB signals under other names: carrier-free, baseband, time domain, non-sinisoidal, orthogonal function, and large-relative-bandwidth radio/radar signals [9]. These UWB signals are then used in wide range of applications, including both communication and radar by the late 1970s. These applications include: pulse train generators, pulse train modulators, switching pulse train generators, detection receivers and wideband antennas.

In the 90s, research on the impulse signals for purposes of radio communication is revisited by Win and Scholtz, and UWB impulse radio was proposed (Milcom conference) [10]. By this time, the name ultra-wideband became popular.

1.1.2 UWB regulation

In 1998, the Federal Communication Commission (FCC), which is the agency responsible for the regulation of non-military spectrum in United States of America (USA), begun the process of regulating UWB. This procedure was completed in 2002, the FCC authorized the use of ultra-wideband signals for communication purposes [11], in the band from 3.1 GHz to 10.6 GHz, provided it complies with some constraints. The first constraint to be met by a signal to be considered as UWB is: a bandwidth at -10 dB of at least 20% of its center frequency, or a minimum of 500 MHz instantaneous bandwidth. The second constraint concerns the Power Spectral Density (PSD), which is limited to -41.3 dBm/MHz, in order to limit the impact of the new UWB devices on already existing services in the same frequency bands. However, this spectral mask depends on applications and regions. Regulations for UWB are being established worldwide, and are often updated. Figure 1.1 summarizes the frequency bands as well as the PSD masks provided by several regulation agencies for different regions.

In Europe and Asia, regulation tends to be more strict when compared to relatively relaxed in USA. In Europe (EU), the European Communications Commission (EEC) has divided the available spectrum of 7.5GHz in two sub-bands to take into account the interference and coexistence with other systems that may reside in the UWB band as the UNII band which is centered at frequency 5 GHZ. The first sub-band called *low band* ranges between 3.1 and 4.8 GHz, whereas the second one, called *high band*, is between 6 and 8.5 GHz. The ECC has set a PSD mask at -41.3 dBm/MHz in high band , and at -70 dBm/MHz in the low band (blue line in Figure 1.1). When implementation of interference mitigation techniques is used (Detect And Avoid noted

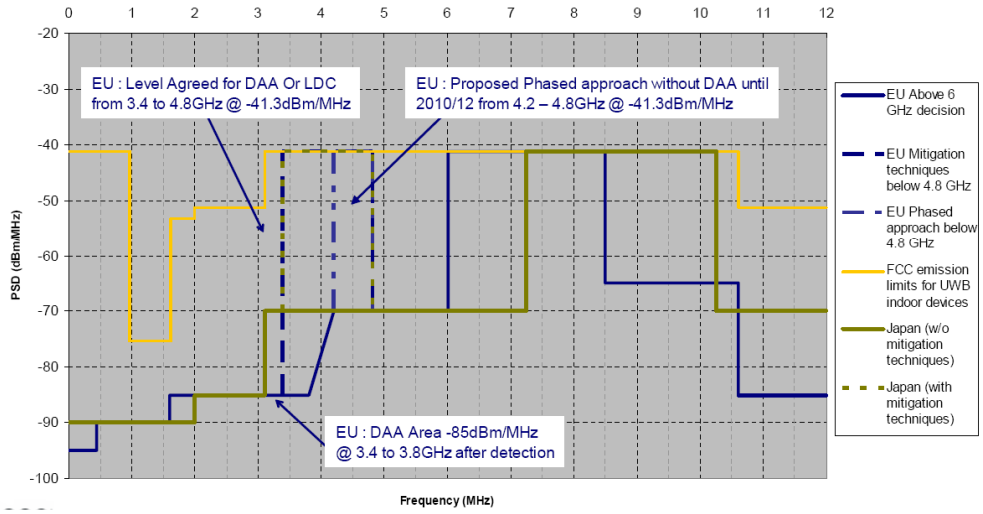


Figure 1.1 — UWB bands and PSD masks for different regions

DAA or Low Duty Cycle noted LDC), low band is permitted to operate with -41.3 dBm/MHz (blue dotted line). These choices were adopted to protect the existing and future mobile services (such as IMT-advanced), especially at 2.7 GHz or in the band 3.4-3.6 GHz.

In Japan, the Ministry of Internal Affairs and Communications (MIC) completed the proposal draft in 2005. Similar to ECC, the MIC proposal has two sub-bands, but the low band is from 3.4 GHz to 4.8 GHz and the high band from 7.25 GHz to 10.25 GHz. Interference mitigation techniques are also required for the low band to permit the PSD mask of -41.3 dBm/MHz [12].

In Singapore to stimulate the study and development of UWB usage, a technical park is considered as an UWB Friendly Zone (UFZ) and allows the much more relaxed PSD limit of -35.3dBm/MHz from 2.2 GHz to 10.6 GHz [13].

1.1.3 UWB principle and characteristics

The UWB signal is defined (FCC definition) as any signal whose absolute bandwidth at - 10 dB is at minimum 500 MHz, or its relative bandwidth is more than 20% of its center frequency. Currently, there are two technical approaches for UWB system development [1]:

- the multi-band (MB) Orthogonal Frequency Division Multiplexing (OFDM) UWB approach which combines two sub-approaches: the MB, which consists in dividing the available UWB spectrum into several sub-bands, each one occupying approximately 500 MHz (to relax the system [2] comparing to the single-band), and the well known OFDM. This combination allows UWB transmission to inherit all the strength of OFDM technique which has already been proven for wireless communications as Digital Video Broadcasting (DVB), 802.11a,802.16.a, Long Term Evolution (LTE), ... [14]. The MB-OFDM UWB approach

[1] Other approaches exists using less conventional waveforms, namely chirp and frequency hopping (FH) waveforms

[2] less speed ADCs, and low complexity when processing a multipath

can achieve a very high data rate, but generally, it is not suitable for energy constrained applications.

- the Impulse Radio (IR) UWB approach consists in sending short pulses in the time domain, and thereby spreading the energy over a wide bandwidth in frequency domain to reach at minimum the required 500 MHz (a narrower pulse in time occupies a larger bandwidth). This approach can be designed with relatively low-complexity and low power consumption, this is why it is amenable to the energy-constrained application. This thesis will focus on the IR-UWB approach, details on the communication chain are presented in the next sections

The main characteristics of UWB signals are related to their large bandwidth:

- **High channel capacity**: this can be affirmed by the Shannon criterion, that relates the channel capacity (C) to the bandwidth (B) and SNR in Additive White Gaussian Noise (AWGN), as shown in equation 1.1:

$$C = Blog_2(1 + SNR) \tag{1.1}$$

  The expression shows that the capacity grows linearly with the bandwidth but only logarithmically with signal power, making UWB amenable to large data rates. UWB system can provide more than 500 Mbps.

- **Low power spectral density** : UWB signals have a low PSD (regulation limit: -41.3 dBm/MHz), which allows not only to coexist with other signals, but also to have the opportunity to make very low-consumption systems. Moreover, this low PSD makes the UWB signals inherently covert and extremely difficult to intercept or to detect (low probability of interception/detection).

- **High time resolution**: larger bandwidths allow better timing resolution, so echoes of an UWB signal arrive separately to the receiver. This ensures a high resistance to fading [3], and allows multipath combination to enhance the system performance [15]. Furthermore, this good time resolution has an interesting side effect: it allows high precision range estimation. The distance between emitter and transmitter can be determine by using the variance of the delay of transmitted signals. This variance is inversely proportional to the bandwidth of the signal: the higher it is, the more precise the estimation is [16]

- **Robustness against interferences**: the wide bandwidth available for UWB signals enables them to leverage a large frequency diversity, therefore having an interferer in the whole channel is very unlikely.

1.1.4 UWB Standards

Several attempts at standardization for UWB PHY layers have been made in the past few years. The IEEE Standards Committee has attempted to standardize a UWB-based PHY layer for the first time in 2003, with the IEEE802.15.3a task group. This PHY was seen as an alternative of

[3]The phenomenon in which several echoes of the same signal arrive close enough, and combine together either constructively or destructively

the standard IEEE 802.15.3 for Wireless Personal Area Networks (WPAN). Different modes of transmission for various ranges are specified by The IEEE 802.15.3a: 110 Mbps at 10 m, 220 Mbps at 4 m, and an optional mode at 480 Mbps at 1 m.

After several proposals, each supported by different industrial partners, the IEEE802.15.3a group has converged to two proposals that met the high data-rate criteria: the aforementioned MB-OFDM UWB approach directed by Intel, and the Direct Sequence (DS) UWB approach which relies on a DS spread spectrum proposed by Motorola. After several years of disagreement, the standardization group was disbanded without generating a standard.

In March 2004, the IEEE 802.15.4a task group has started to work on a new standard that include UWB-PHY and aimed at low-data-rate and low-power UWB applications. This potential standard was also an alternative to the standard IEEE802.15.4 which was designed to deal with relatively short range WPAN and which formed the basis for the Zigbee devices. After three years of work, IEEE 802.15.4a standard was published in 2007. The UWB-PHY proposed in this standard was based on IR-UWB. It is compatible with both coherent and non-coherent receivers, and allows four different data rates: 110 kbps, 850 kbps, 6.8 Mbps and 27 Mbps. However, large distances can be achieved, when low data rates are used, this is why ranging applications has appeared since.

The last standard that includes UWB is the IEEE 802.15.6, describing Body Area Networks (BANs) and published in March 2012. A very wide range of applications is foreseen as the standard targets short-range wireless devices for in-body, on-body, and around-the-body communications. Besides the very significant medical and healthcare application domain, the standard offers a huge opportunity for non-medical applications [3] belonging to a variety of fields including personal audio or video, gaming, entertainment, wearable computing, ambient intelligence, and many others. Given that the present thesis targets the IEEE 802.15.6 standard, the UWB-PHY of this latter will be discussed into more details in this chapter.

1.1.5 UWB applications

UWB can have a wide range of applications. It is mainly used for communication, radar systems, and localization.

Figure 1.2 shows the current trends in applications for UWB technology. On one side we have very high-data-rate, very low-distance applications such as WPAN. On the other side, we find low/medium data rate, low/medium/long distance applications such as Wireless BAN, radar, or localization.

Several applications in the high data rate WPAN communications were targeted initially, such as Internet access, PC peripheral connectivity, and multimedia services (*eg.* video streaming). With time, the WPAN UWB was abandoned, mainly due to the dissolution of the IEEE 802.15.3a, and to the UWB chipsets prices which were relatively high compared to existing solutions such as Wi-Fi or Bluetooth. Most companies that were interested by UWB technology announced their withdrawal from the UWB development such as Intel and WiQuest. Nevertheless, a few companies continued the development of UWB-WPAN , such as Alereon [17], which proposes its *AL5350* chipset that enables a different high data rate transmissions (up to 480 Mbps), or Pulse Link [18] which proposes its *PL3120* chipset that achieves a data rate of 675 Mbps.

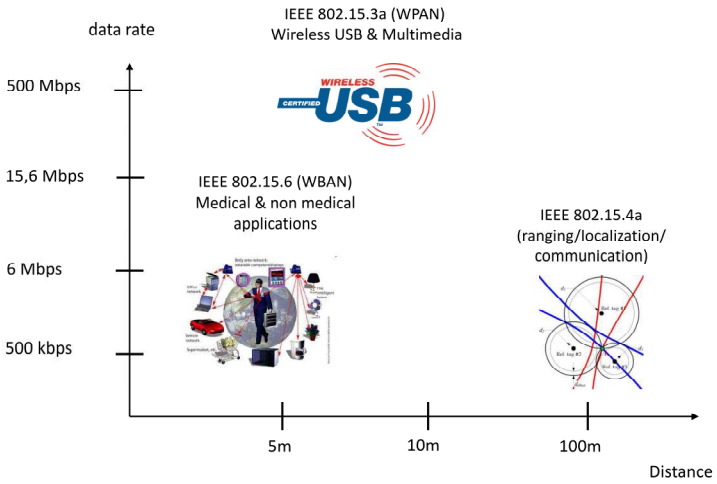


Figure 1.2 — UWB applications

Regarding the low/medium data rate communication, UWB was also in competition with some existing wireless technologies such as ZigBee, bluetooth, and Wi-Fi. However, UWB has incorporated new improvements on top of its original advantages. UWB can outperform the other solutions in its class that were developed solely for communications, but it also opens a possibility for new applications as indoor localization which can be applied mutually with Global Positioning Satellite System (GPS) for outdoor use, to have a complete location devices. Regarding performances, UWB currently provides throughputs around 7 Mbps, while providing precise localization with a resolution of a few centimeters for positioning applications. Several companies currently work in this promising field. *Decawave* [19] proposes a UWB chipset (*DW1000*) compliant with IEEE 802.15.4.a standard which enable joint localization of tagged objects and communication with throughputs up to 6.8 Mbps. A precision of 10 cm at a distance of up to 300 m in Line-of-Sight (LOS) is achieved, with possible communication at up to 110 kbps at this distance. We also find in these applications: (1)*Time domains* company ([20]), which commercializes a ranging chipsets that enable real-time localization in the most difficult environments with precision of roughly 2 cm, and (2) BeSpoon [21] that provides its UWB-chip on a wide range of form factors and with possibility to drop it in any hardware system.

1.2 IR-UWB transmission principle

This section starts by describing the elementary IR-UWB pulse, and then provides an overview of the main techniques used at the transmitter side of an IR-UWB communication systems. Different state-of-the-art techniques for pulse generation, modulation types, and multiple access are presented. However, the antenna study is not covered in this chapter as it exceeds the scope of this thesis work.

1.2.1 IR-UWB pulse shape

In IR-UWB approach the required large bandwidth ($\geq$ 500 MHz) is obtained by using a very short pulses in the range of sub-nanosecond duration. This comes from the fact that a narrower

pulse in time occupies a larger bandwidth as illustrated in Figure 1.3. These pulses were initially [15, 22] either Gaussian pulses, Gaussian monocycles (first derivative of Gaussian pulse) or the second derivative of the Gaussian pulse. This choice was related to the fact that Gaussian pulse has smaller side lobes and a sharper roll-off in the frequency domain [23]. However, it turned out that these type of pulses do not meet the FCC requirement in term of spectral mask and targeted band. Other solutions are investigated to satisfy these requirements. It is either by increasing the derivative of the Gaussian pulses, or by other recent techniques, as such modulating a baseband pulse (*cf.* 1.2.4). In an IR-UWB system, the pulses are transmitted with a very low duty cycle ($\leq 1\%$) relative to the symbol duration. This also impacts the PSD by decreasing its value, when the symbol duration is high. In this case, repetition of pulses within the symbol is performed to compensate this effect.

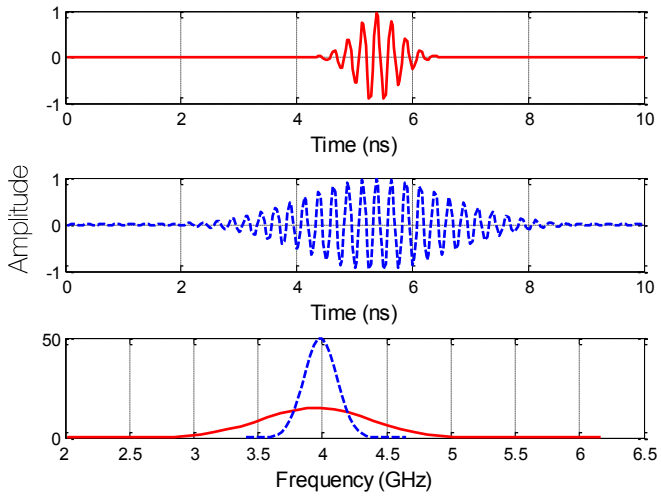


Figure 1.3 **—** Example of an elementary IR-UWB pulse

1.2.2 Modulation schemes

As in narrowband communications, information in IR-UWB system can be encoded in the phase, the frequency, or the amplitude of the transmitted signal. In addition to these types of information coding, IR-UWB has more specific encoding formats, such as position, as it uses pulses to convey information. Below, a description of the different modulations commonly used in IR-UWB is given in ascending order of their complexity and performance.

1.2.2.1 On-Off Keying (OOK)

The OOk modulation scheme is the most intuitive modulation, where symbol ”1” is represented by transmitting a pulse, and ”0” by transmitting nothing. Mathematically, this modulation scheme can be expressed as follows:

$$s(t) = \sum_{j} b_j w(t - jT_f) \tag{1.2}$$

where b_j is the associated amplitude to the j^{th} frame.

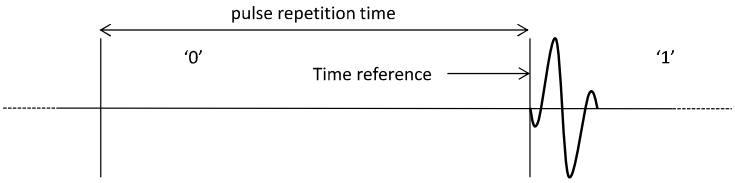


Figure 1.4 — OOK modulation scheme

It is simple to implement both in transmitter and receiver, and it is particularly well suited for non-coherent energy detection receivers. However, because OOK sends less pulses than other modulations (in fact, half as much), the peak power of OOK pulses can be doubled to reach the same average power, and in some cases the same performance (subject to have equal distribution of symbols). In such configuration, OOK pulses become easy to detect comparing to other modulated pulses.

1.2.2.2 Pulse Position Modulation (PPM)

The PPM scheme [10,24] relies on shifting the emitted pulse(s) in time depending on the symbol value. This shift can be either in the same order of the pulse duration, or larger [6]. The PPM IR-UWB signal can be formulated as follows:

$$s(t) = \sum_{j} w_{tr}(t - jT_f - \delta d_{[j/Ns]}) \tag{1.3}$$

where w_{tr} is the transmitted pulse waveform, T_f is the pulse repetition time, $d_{[j/Ns]} \in \{0, M-1\}$ where M is the modulation level, and δ is the PPM time-shift.

Figure 1.5 illustrates a 2-PPM modulation scheme (M = 2).

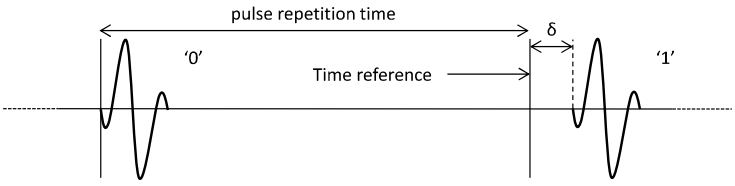


Figure 1.5 — 2-PPM modulation scheme

In the 2-PPM, when the symbol value to be transmitted is '0', no additional time shift is modulated on the pulse ($d_j = 0$), while when the symbol value is '1', time shift of δ is added to the pulse ($d_j = 1$) relative to the time reference. In fact, PPM can be generalized to M

modulation levels. One only need to introduce a set of shift time where each of them corresponds to one modulation level. This will improve the spectral efficiency of the radio link. Beyond this interest, PPM modulation allows a good distribution of energy in the frequency band. This lies on the fact that pulses change continuously the position from a symbol to another, which breaks the periodicity of the transmitted signal, and thereby smooths the spectrum (provided that the data to be transmitted do not have a long sequences of identical symbols). Moreover, it presents a good trade-off between implementation complexity (simple control of transmission time) and performance (limited to 3 dB degradation compared to BPSK for 2-PPM).

1.2.2.3 Pulse Amplitude Modulation (PAM)

In this type of modulation, the information is encoded by varying the amplitude of the pulse. Mathematically, this modulation scheme can be expressed as follows:

$$s(t) = \sum_{j} b_j w(t - jT_f) \tag{1.4}$$

where b_j is the associated amplitude to the j^{th} frame.

As PPM modulation, PAM can also be extended to M modulation levels for improving the spectral efficiency. A special case of PAM is the Binary Phase Shifting Keying (BPSK), which is the most commonly used modulation in IR-UWB system beside the PPM and OOK modulation. It consists on multiplying the pulse by b_j = 1, or -1 (Figure 1.6), according to the symbol value (”1” or ”0”), and it is limited to coherent receivers. However, PAM presents good performance compared to PPM when M is low (for M= 2, 2-PAM or BPSK has 3 dB advantage over PPM and OOK at the same transmitting average power). On the other side, when M increases, PAM performance becomes worse compared to PPM [25].

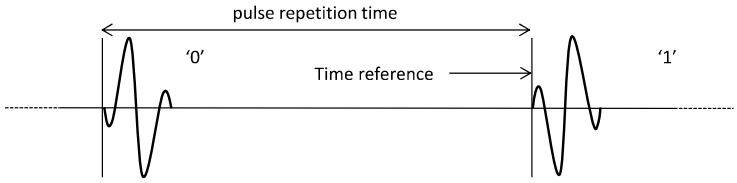


Figure 1.6 — 2-PAM (BPSK) modulation scheme

1.2.2.4 Other modulation schemes

The selection factor of the modulation scheme depends on several criteria and target requirements in terms of complexity, data rate, maximum transmit power, channel capacity, and receiver topologies (coherent, non-coherent, differential) of an IR-UWB system. Beside the above presented modulations, novel or hybrid modulations are proposed in the literature targeting to improve specific performance metrics of IR-UWB systems. Some of such modulations can be found in references [26], [27], and [28]. The first reference [26] proposed a novel modulation called QBOK (quadrature binary orthogonal keying) to increase capacity of simultaneous users

in a multi-user context, while the second [27] presented the termed PIM (Pulse Interval Modulation) modulation to simplify the receiver structure. In reference [28], an hybrid modulation that consists of a mixture of PPM-BPSK modulations has been proposed. About 2.7 dB improvement was obtained over other existed hybrid modulation schemes in a coherent receiver.

1.2.3 Techniques for multiple access in IR-UWB

When important set of users (devices) communicate in the same environment and share independently the same channel, recovering the useful signal among the set of received signals by each user becomes a hard task. Various techniques are used to manage this multiple access problem in UWB systems [22,29], such as Frequency Division Multiple Access (FDMA), Time Division Multiple Access(TDMA), Space Division Multiple Access (SDMA), and Code Division Multiple Access (CDMA) [30]. In IR-UWB, two techniques are usually employed: the Time hopping (TH) which is TDMA or CDMA method, and Direct Sequence (DS) which belongs to CDMA techniques.

1.2.3.1 Time Hopping for multiple access

TH is a technique that attributes to each user a unique pseudo-random time-shift pattern named TH code to minimize the probability of collisions due to multiple access [22]. This is possible, thanks to the very low duty cycle of the IR-UWB communication, which allows the possibility of hopping pulses on the frame duration. If we consider a PPM modulation, the TH-output signal for the k_{th} transmitter can be written as follows [22]:

$$s^k(t^k) = \sum_j w_{tr}(t^{(k)} - jT_f - c_j^{(k)}T_c - \delta d_{[j/Ns]}^{(k)}) \tag{1.5}$$

where $t^{(k)}$ refers to the time of the k^{th} transmitter clock, and T_f is the pulse repetition time. In this access technique, each frame is subdivided into N_h chips of duration T_c. Considering the time-shift related to the PPM modulation ($\delta d_{[j/Ns]}^{(k)}$), each pulse undergoes a new additional time-shift of $c_j^{(k)}T_c$ due to the TH code $c_j^{(k)}$. Each TH code is an integer in the range $0 \geq c_j^{(k)} \leq N_h$ with $N_h.T_c \leq T_f$. We note that the time-shift introduced by the TH code affects only the pulse within the frame and not the frame itself, and hence each user is identified by matching its own TH code at the receiver.

Figure 1.7 illustrates an example of TH multiple access for two users without modulation. In this example, the TH code are $c_j^{(1)} = \{0, 4, 2, 0\}$ for user 1 and $c_j^{(2)} = \{2, 0, 4, 2\}$ for user 2 with $N_h = 5$.

It should be noted here that beside the interest of managing users access, the use of TH code allows also to flatten the spectrum of the transmitted signal by randomizing the pulse train in time, and thereby assimilate the IR-UWB signal to a white Gaussian noise in the band it occupies. Furthermore, it ensures a good level of privacy for the transmitted data, by the fact that the receiver needs to know the pseudo-random sequence used by the transmitter to decode a UWB signal.

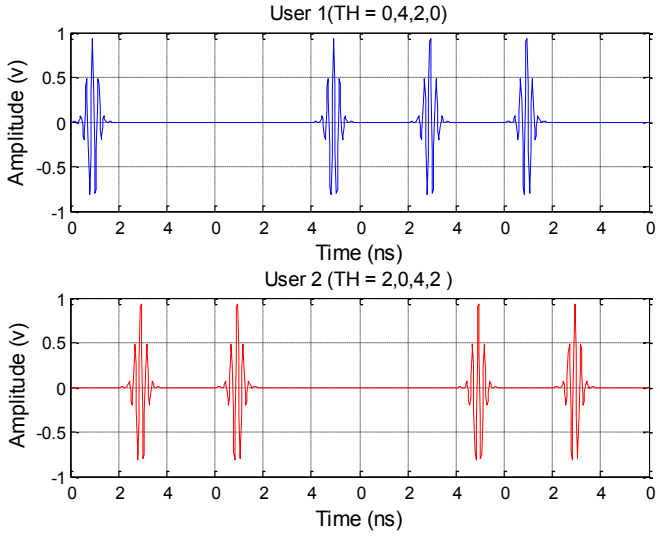


Figure 1.7 — Example of TH-UWB access multiple for 2-users

However, the TH technique can introduce Inter Symbol Interferences (ISI) if the distance between two consecutive pulses is less than the CIR. To mitigate this effect, previous works [6–8] require a minimum distance (between two pulses) depending on channel spreading with the OOK modulation when TH is used. TH technique may also causes multi-user interference (MUI) if the number of users is high and/or located at close range. This is due to the multipath effect that breaks the orthogonality of the TH codes between users. The vast number of paths resulting from each user multiple paths can create an overlap between users, which leads to MUI. Several references have investigated this issue, the interested reader can refer to [31, 32].

1.2.3.2 Direct-Sequence for multiple access

Well-known in cellular radio, the DS technique ([33]) is considered as the alternative multiple access to TH in IR-UWB [34]. The DS technique relies on providing to each user its own pseudo-random code, to be further used as user-identifying in multiple access. The pseudo-random codes are orthogonal, and thereby interference between users in multiple access can be mitigated. If we consider a PAM modulation, the DS-output signal for the k_{th} transmitter's can be written as follows:

$$s^k(t^k) = \sum_j b_j \sum_{i=0}^{N_c-1} c_i^{(k)} w_{tr}(t^{(k)} - jT_f - iT_c) \tag{1.6}$$

where $t^{(k)}$ refers to the time of the k^{th} transmitter's clock, T_f is the pulse repetition time, T_c is the chip duration, and Nc is the number of chips used to represent one frame with $N_c.T_c = T_f$.

In this type of multiple access, each user is differentiated from the others by its *coded* frame. The DS-UWB system generates a train of high duty-cycle pulses (analogous to chips) whose polarities follow the pseudo-random code. A data bit is then used to modulate this train of

UWB pulses [35]. Figure 1.8 gives an example of DS-UWB multiple access for two users when BPSK (2-PAM) modulation scheme is employed. The PR codes are $c_i^{(1)} = 1, 1, -1$ for user 1 and $c_i^{(1)} = -1, -1, 1$ for user 2, and $Nc = 3$. To avoid pulses overlapping and reduce the effect of ISI, the chip duration is usually chosen greater than the pulse width ($T_c > T_w$). DS technique allows the different users to share the same bandwidth and time to transmit signals, thus it increases the user capacity and data rate.

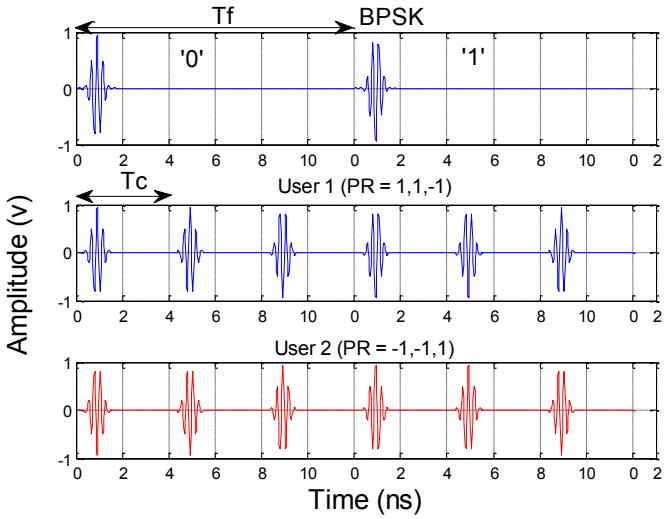


Figure 1.8 — Example of DS-UWB access multiple for 2-users with a BPSK modulation scheme

1.2.3.3 FDMA multiple access

The FDMA technique is less used in IR-UWB systems because of the large spectrum of the UWB signal (minimum 500 MHz). In this multiple access scheme, the frequency is divided into multiple sub-bands called channels, each of what is allocated to an user. The most important advantage of this technique is that it minimizes the interference among users when the frequency ranges of users are adequately separated and the guard band is wide enough. Nevertheless, this access scheme allocates each channel for a specific user, and other users are not allowed to share the same frequency resource even if the channel is idle, which leads to a very low spectral efficiency. This is why FDMA can not provide enough number of users.

1.2.4 Pulse generator

In IR-UWB system, the pulse generator is the most critical block as its power consumption dominates the total power of the transmitter. Considerable efforts in the literature have focused on the design of efficient pulse generation and its optimization. Three main architectures (depicted in Figure 1.9) are commonly used in this context:

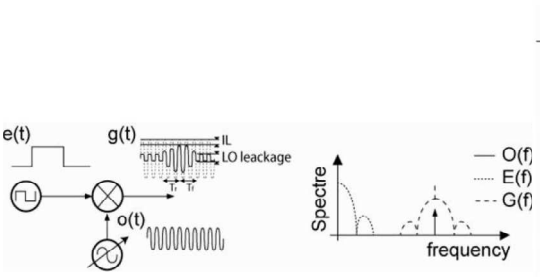
- **Baseband pulse transposition**: this architecture is based on signal transposition technique, where the pulse is generated at baseband and up-converted to a center frequency in the UWB band by mixing it with a Local Oscillator (LO) [36–38] (Figure 1.9a). However, the LO leakage caused by the mixer produces a high spectral line at LO frequency. Moreover,

the power consumption of the mixer stages increases the overall consumption of this topology. This is why recently, ON/OFF LO techniques are used [39–42] to overcome these limitations.

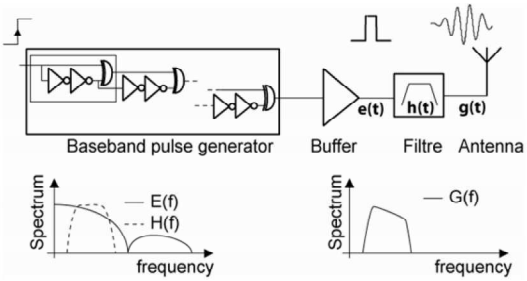
- **Baseband pulse filtering**: the principle used for this architecture is described in Figure 1.9b. The targeted pulse spectrum is fixed by the filter frequency response since the baseband pulse has a high frequency band (very narrow pulse in time). Implementation of this technique can be analog [43, 44] or digital [45, 46].

  Baseband pulse filtering is appropriate for System in Package (SiP) integration technique which allows the use of high performance filters [43]. It is well suited to high output dynamic (higher than 1Vpp) and low power consumption systems [47]. Unfortunately, the output filter integration is one of the main drawbacks of this technique. First, it is difficult to implement reconfigurable filter in the targetted frequency (3-10 GHz) and then, multi-channel generators are out of the scope of this technique.

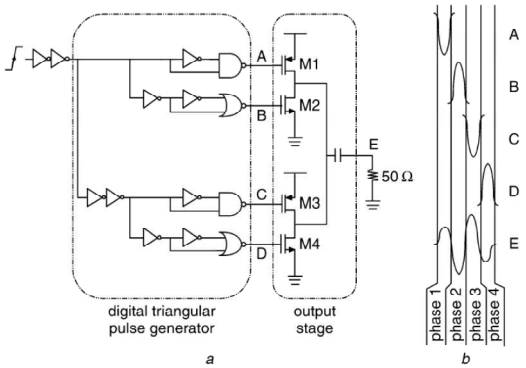
- **Synthesis by pulse combination**: in this architecture the pulse (complex pulse: E in Figure 1.9c) is generated directly in UWB band by combining digitally different path delays (elementary pulses: A, B, C, and D in Figure 1.9c) [48–50]. This technique allows pulse shape reconfiguration which can be used for compensation of the Process, Voltage, and Temperature (PVT) variations [51]. This is why this technique is well suited to industrial process. Here, the magnitude and the width can be precisely tuned, this topology is limited by the need of Power Amplifier (PA) which dramatically impacts the consumption and the bandwidth [44, 49].



(a) Banseband pulse transposition principle [47]



(b) Baseband pulse filtering technique [47]



(c) Pulse synthesis principle [48]

Figure 1.9 — Different pulse generation techniques

After this description of the different blocks and techniques used in IR-UWB transmitter, we review in the next section existing receiver structures and reception techniques.

1.3 IR-UWB receivers

Receiver structures in IR-UWB systems fall in three topologies, namely coherent, non-coherent and differential receivers. The implementation of an IR-UWB receiver can be done in different manners as described thereafter.

1.3.1 IR-UWB receiver topologies

Coherent receivers exploit the phase of the pulse in addition to its magnitude to demodulate information bits. The first commonly proposed implementation in this context follows the *analog correlation* architecture (Figure 1.10).

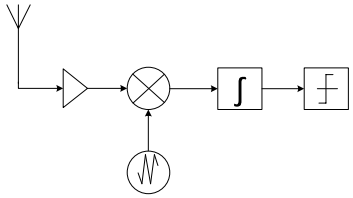


Figure 1.10 — *Coherent receiver: analog correlation architecture*

In this architecture, the received IR-UWB pulse is correlated with locally generated template pulse to decide later the received bit by exploiting the correlation result. However, this architecture requires an accurate phase synchronization (in the 100 ps range) to correlate the received pulse with the template. Furthermore, the transmitted pulse is severely distorted by the channel environment, and hence it is unlikely that the received pulse corresponds to the template one. This template can be adapted according to the channel, by creating a composite template that reflect the image of impulse response, but this solution needs a precise channel estimation.

The second type of architectures used in coherent receivers is the traditional *direct-conversion* architecture (Figure 1.11).

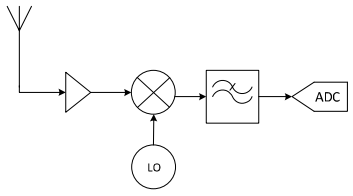


Figure 1.11 — *Coherent receiver: direct conversion architecture*

Similar to the narrowband receiver system, this architecture uses a LO to convert directly the IR-UWB pulse to the baseband frequencies. The received signal is then filtered and converted to digital domain by an analog-digital converter (ADC). This approach typically implies a relatively high power consumption and complexity, due to the presence of high frequency LO.

The last architecture commonly used in coherent receivers is the *direct over-sampling* architecture (Figure 1.12).

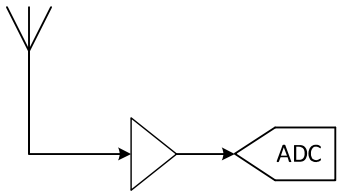


Figure 1.12 — *Coherent receiver: direct over sampling architecture*

It consists of quantifying the received pulse directly by the ADC, moving thereby the demodulation to digital baseband. This type of architectures is the most straightforward, as the pulse input is directly quantized, but it requires a very high speed ADC (multi-gigahertz, medium resolution), which consumes a significant amount of power, and may substantially increase the system cost as it requires advanced Complementary Metal Oxide Semiconductor (CMOS) technologies [52]. Moreover, this type of receiver grows the digital baseband complexity as all receiver functions are performed digitally.

In summary, coherent receivers can achieve higher data rate, sensitivity and robustness against interferers, but they require high power consumption, high cost, and accurate time acquisition compared to the non-coherent receivers described thereafter. Some of these impediments can be mitigated by using I/Q reception [53, 54].

Non-coherent receivers exploit only the magnitude of the signal without exploiting the phase information. The most prominent implementation of these receivers is based on energy detection architectures (Figure 1.13). The energy detection is performed by squaring the received signal and then integrating it over a window duration T typically in the same order of the channel response duration.

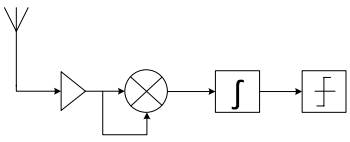


Figure 1.13 — *Non-coherent receiver: energy detection architecture*

But such receivers are very sensitive to noise, so using a long integration window causes greater noise accumulation which leads to decreased receiver performance. On the other hand, the use of a short window prevents the path diversity exploitation, which also leads to a performance loss, as all the channel energy is not taken into account. Moreover, this will require more synchronization accuracy in order to determine the best instant to trigger the time integration for optimal energy collection. The difficulty of such receivers is in the determination of integration time T that offers a tradeoff between the energy capture and the acquired noise power.

It was shown in reference [55] that there is an optimal value of T that depends on the desired error rate performance and the channel spreading. This optimal T can lead to the desired error

rate performance with a minimum SNR value. Below or above this value T, it is necessary to maintain a higher SNR to get the same performance. Some references [56–58] choose T = 30 ns; reference [59] set it to 16 ns. Reference [60] concludes that it is appropriate to set T about one and a half to two times the τ_{rms}. This value is the root mean square (RMS) delay spread of the channel, where 80-85% of the received energy can be found. This is because it was observed that this energy portion, provides a bit-error probability close to the minimum one.

However, there are some references that use a short integration interval of few nano-seconds [6, 61–63], or divide the whole integration interval T to M short sub-intervals, each collecting a portion of the received energy [64].

Other implementations have been proposed for non-coherent receivers [65, 66]. For example, reference [65] proposes an architecture called super-regenerative for the 3-5 GHz band. The architecture includes a Low-Noise Amplifier (LNA), transconductor, oscillator, and buffer stages. This architecture is based on the transient response of oscillators to filter and amplify the received signal. LNA and transconductor are used to reduce the noise factor of the overall architecture and to achieve high isolation to prevent signals at the oscillator output from being re-emitted when the output buffer enables external connection to other blocks of the system [65].

Non-coherent receivers are straightforward solution to implement an IR-UWB system featuring low complexity, low cost and low power consumption. Unfortunately, performances are decreased when compared to the coherent receivers as phase information is not exploited. Furthermore, these receivers are more sensitive to noise and interference as simple energy detection does not allow to discriminate between noise, interferer and transmitted data.

In **differential receivers** for transmitted reference modulations [67], the information lies in the phase difference between two consecutive pulses which are close in time, as shown in Figure 1.14.

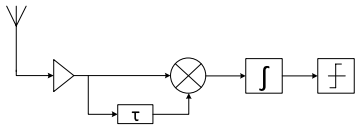


Figure 1.14 — *Differential receiver*

The idea is to send pairs of pulses: the first one is an unmodulated pulse called reference pulse while the second one is modulated and called data pulse (or simple differential modulation). Both pulses experience the same channel conditions and hence the reference pulse can be used as the template signal needed for correlation with the data pulse at the receiver. The constraint is therefore much less than in coherent receivers, yet the performance is close to the non coherent receiver in the Gaussian channel. This is due to the use of noisy template waveform (which degrades the system performance) and the usage of RF wideband delay lines, which are very difficult to implement in current CMOS technologies [68].

1.3.2 Baseband processing and digital architectures

Synchronization

Synchronization or timing acquisition aims to track the beginning of the transmitted symbol, i.e get a common reference time between transmitter and receiver. The synchronization is typically performed by exploiting a sequence shared between the transmitter and the receiver, this sequence is concatenated by the transmitter to the data frame. The added sequence is called *synchronization header* and it is usually a pseudo-random sequence. Synchronization is tracked at the receiver by identifying the synchronization header. Several techniques can be used to perform this identification. These techniques depend on the type of receiver and on the other receiver's processing blocks that come after the synchronization block. They can be implemented either in digital or analog domain. Synchronization is not a new issue in general, but in IR-UWB systems it reprensents a major issue in the receiver design. This is mainly due to the very low power density and to the ultra-short width of the conveyed pulses.

For coherent receivers, and particularly in analog correlation architecture, synchronization is based on the sliding correlation technique [69–71]. The receiver generates locally a template signal and then performs sliding correlation with the received signal. The correlation peak instant indicates the shift time between the two signals: the received, and the transmitted one, and thereby a synchronization is found. However, the above exhaustive search takes a long time to acquire synchronization. In order to speed up synchronization, a solution is to use an algorithm [71] which divides the pulse repetition period (PRP) which represents the frame time upon N time windows called *bins*, then selects randomly a *bin* to compare the correlation result within the *bin* to a predefined threshold. If it exceeds the threshold, a verification phase is then performed to confirm that it was a correlation peak and not a false alarm, otherwise another *bin* is selected for the same operation. The acquisition time improvement is shown to be about a factor of 33 compared to the exhaustive search methods. We must note here, that the correlation techniques in a coherent receiver can be moved to the digital domain when using the appropriate receiver (such as the direct over-sampling architecture).

Since the bandwidth of IR-UWB signals allows the separation and characterization of a large number of components of the received channel, an appropriate solution is to use a Rake receiver in order to compensate for the multipath and also to take advantage of the multipath diversity gain to boost the SNR. However, the exploitation of the channel diversity needs an estimation of this latter. Several contributions in the literature have dealt with the problem of channel parameters estimation in IR-UWB communications. In reference [72], the estimation method is based on the maximum-likelihood (ML) criterion. This can be used with a training symbol which can help to estimate the channel. The problem with these algorithms is that they require the computation of a very large number of paths, which make it unsuitable for practical implementation. Another proposed technique uses a joint timing synchronization and channel estimation based on least squares (LS) approach [73]. Essentially, it looks for the minimum euclidean distance between the received samples and a local replica of their noiseless components. More recently, reference [74] proposed a simultaneous synchronization and channel estimation for a coherent receiver. The proposed timing synchronizer consists of coarse and fine timing estimation to find the frame-level synchronization. Once this later is found, four iterative cross-correlations between the received frame and a reference frame are performed, and thus four paths are esti-

mated.

When non-coherent receivers are adopted, the channel information becomes unnecessary most of the time, especially for energy-detection receivers with long integration time. Only frame-level synchronization is required in this case. This issue was addressed in several works. The authors in [75] propose a scheme with serial search using a sliding window. The integration window is shifted through the entire frame and the energy is collected at the same time. The shift that identifies to the maximum collected energy corresponds to the synchronization point. The drawback of this scheme is that it requires a large number of preamble symbols and significant iterative process. Another approach is to use autocorrelation methods. These methods consist of applying autocorrelation between the received signal and the predefined preamble to identify the presence of this later by detecting a correlation peak. This is done either by a comparison to a threshold [76], or through a verification step of the peak index location [77]. Another idea is proposed in [78] which consists of converting the serial search presented in [75] to a parallel one, thus dividing the frame into multiple integration subintervals. Each integrator output is weighted and combined to maximize the SNR, and then compared to a threshold in order to decide which subinterval is containing the signal. The problem with such synchronization schemes is that their complexity increases greatly when they are applied in practice. Similar to the work in [75], the work presented in [79] has recently proposed an optimized version of the serial search method. It consists of using a fast binary serial search algorithm instead of the multiple serial shifts through the entire frame. The algorithm has a low complexity and fast synchronization speed, but it allows only a moderate accuracy.

Demodulation

As it has been mentioned above, the received data can be demodulated in a coherent scheme (phase information is exploited) or in non-coherent scheme (no phase information is exploited, only the magnitude of the signal). The demodulation depends on both the employed modulation at the transmitter side and the receiver architecture. For coherent receivers, the data is demodulated by exploiting the correlation result, i.e. the amplitude and the sign of the correlation for phase modulation, In fact, the amplitude is compared to a threshold to ensure the presence of signal while the sign indicates either the bit data is '1' or '0'. For non-coherent receivers, often the collected energy is compared to a threshold to decide the bit value. When PPM modulation scheme is employed, the demodulation is based on energy comparison between the possible positions of the pulse.

Several works have investigated the exploitation of multipath effect in UWB channel to increase the receiver performance. Such a technique can be implemented by the so called *Rake* receiver [80]. This latter can exploit the high degree of diversity that results from a large number of multipath components and can combine them in constructive way to decide on the received bit [81]. The *Rake* receiver serves as a basis for several other approaches [66, 82–86]. A *Rake* receiver consists of a bank of matched filters, called a *Rake* fingers, each of which matches to one multipath component of the desired signal (cf. Figure 1.15). Reference [85] presents a comprehensive analysis together with performance results of several different implementations of the *Rake* receiver, namely All-Rake (*ARake*), Partial-Rake (*PRake*) and Selective-Rake (*SRake*). The *ARake* receiver captures all the energy carried by a very large number of different mul-

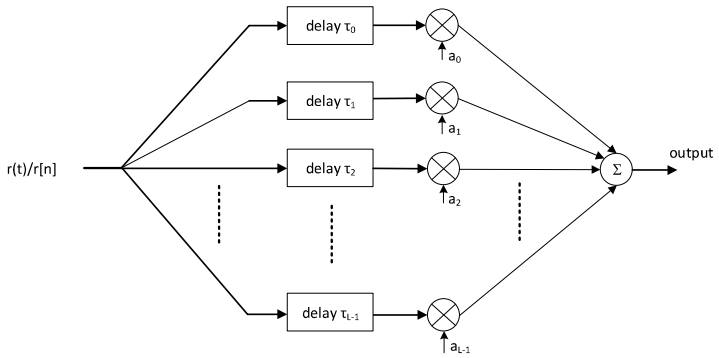


Figure 1.15 — Block diagram of a *Rake* receiver

tipath signals. This type of receiver needs in theory an infinite number of *Rake* fingers, and its implementation is limited by power consumption and complexity constraints. To reduce its complexity, the *PRake* structure is proposed as partial combining of the energy. It combines the first received paths out of the available resolved multipath components, assuming that these first paths are the strongest (i.e. containing the most of the received power). This assumption is not necessary true as strongest paths can be found at later delays depending on the propagation environment. Collecting only the strongest paths is possible by using the *SRake* structure which combines selectively the energy carried out by the strongest multipath components. In term of performance, reference [85] concludes that the *ARake* outperforms the *SRake*, which typically outperforms the *PRake*. However, when the strongest paths are in the beginning of the CIR, the *SRake* and the *PRAke* exhibit the same performance.

The *Rake* receiver algorithms can be implemented either in a coherent or non-coherent manner. Some of these algorithms are reported in [87]. Equal gain combining (EGC) and maximum ratio combining (MRC) are typically used in coherent detection to combine the output of the *Rake* fingers. On the other hand, for non-coherent detection, absolute combiner (AC) with or without power estimation is used. It is worth noting here that the Rake receiver structure is based on the IR-UWB receiver topologies presented above (Section 1.3. Depending on the detection scheme (coherent or non-coherent), the implementation of the Rake receiver will be done either through a bank of analog/digital matched filters [66, 86].

It is important to note that some studies have shown that there is a threshold above which increasing the number of Rake fingers does not significantly improve performance. Reference [88] shows that a Rake with 8, 16, 32 fingers can achieve up to 10 dB gain compared to one finger. It shows also, that improvement between 8-Rake and 16-Rake is 2 dB, whereas the improvement between 16-Rake and 32-Rake is only 1 dB, and thereby increasing the number of fingers beyond 16 is often not profitable when compared with the increase in size.

Reference [89] analyses the optimal number of fingers of an S-Rake for several UWB systems for coherent and non-coherent detection. It concludes that the required optimal number of fingers generally increases with Eb/N0, and depends on channel model conditions if it is LOS (lower required optimal number) or non LOS (higher required optimal number). It concludes also that the optimal number of fingers depends on the nature of detection (coherent or non-coherent) and used algorithm (EGC, MRC, or AC). The results shows that this required optimal number has lower values in non-coherent detection (maximum optimal number is 16) compared

to the coherent one (maximum optimal number is 20)

1.4 Context of this work: the RUBY project

The aim of this work is to develop non-coherent reception techniques in the context of a French collaborative research project, namely RUBY (Radio UWB for BodY area network) [90], coordinated by Orange Labs. RUBY aims at proposing and implementing an innovative UWB impulse radio system particularly suited to Body Area Network and compliant with the IEEE 802.15.6 standard. A description of this standard is given in Appendix A. In this section, we describe the specific parameters that have been considered for the UWB PHY layer in the RUBY project. We also present the different use cases defined in this project. This gives an overview of the specific requirements which needed to be supported by the proposed contributions in this PhD work.

1.4.1 Pulse generator

In the RUBY project, a pulse generator is implemented for the low band. It is partially compliant with the standard, and derived from an existed circuit (presented in reference [91]) designed for IEEE 802.15.4a standard. The main characteristics of this generator is given in Table 1.1.

Peak to peak voltage	2.63 v
-10 dB bandwidth	1.8 GHz
pulse duration	1.2 ns
Central frequency	4 GHz
PRF	120 MHz

Table 1.1 — Main characteristics of the adopted pulse generator

As shown in Table, the generator produces a 2.63 v pulse with duration of 1.2 ns. The generated pulse is centered at 4 GHz and has a bandwidth of 1.8 GHz at -10 dB. However, the generator can provide successive pulses with a maximum repetition frequency of 120 MHz, i.e. pulses can be generated every $\approx$ 8 ns.

Regarding the compliance with the IEEE 802.15.6 standard, the above described pulses do not fully match the specifications. There are two main differences: the generated pulse occupies a wider bandwidth (1.8 GHz) compared to the 499.2 MHz bandwidth specified in the standard, and it has 1.2 ns duration instead of the specified T_w = 2 ns (ChapterA - Table A.8). This comes from the fact that a pulse generator was already available, and in order to get preliminary results faster, this existing design was used. In what follows, pulses with characteristics of Table 1.1 are used.

1.4.2 UWB PHY frame format

In the RUBY project, the 802.15.6 frame format is used. A complete description can be found in Appendix A. The UWB PHY frame format or physical layer protocol data unit (PPDU) specified in the IEEE 802.15.6 standard [1] is illustrated in Figure A.1. It consists of a Synchronization

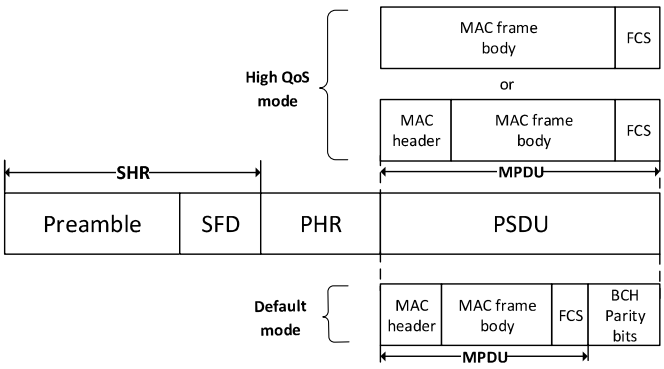


Figure 1.16 — IR-UWB frame format (PPDU) [1]

header (SHR), a Physical-layer Header (PHR), and a Physical-layer Service Data Unit (PSDU). This latter represents the payload of the frame. The PHR contains information about the radio link such as modulation, datarate, ...etc. The SHR consists of the preamble and the SFD. The preamble is used for timing synchronization, packet detection, and carrier frequency offset recovery, while the SFD is used for frame synchronization.

Targeting a specific applications, and a point to point network, one can see that the PHR bits have a prefixed values, and it is useless in these conditions. Nevertheless, we kept it in order to maintain a reasonable degree of compliance with the BAN standard. However, the standard specifies that the PHR frame shall be protected against transmission errors by adding 12 parity bits and a 4-bit CRC. Since there is no entropy in the present PHR, there is no need to protect the data it contains. For the sake of simplicity, no PHR error correction mechanism were set up. Because of the non-necessity (point to point network), the time hopping is also not considered in this work. A summary of PHY layer and its specifications in this work compared to standard one is reported in Table 1.2, and commented below.

Specification		Standard [1]	this work
SHR	number of SHR symbol	4 (preamble) + 1 (SFD)	8 (preamble) + 1 (SFD)
	Modulation	OOK (classical)	OOK (classical)
	PRP	128 ns	64 ns
PSDU	number of data symbol	2048	2048
	Modulation	2PPM (specific OOK)	2PPM (specific OOK)
	PRP	64 ns (for 15.6 Mbps)	64 ns (for 15.6 Mbps)
	Multipl access	Time hopping	non

Table 1.2 — Comparison of physical specifications between the standard and this work

1.4.2.1 SHR construction

As presented above, the pulse generator provide pulses with 1.2 ns duration, and has a 120 MHz as maximum PRF[4]. So generating 8 ns-burst pulse for SHR as specified in the standard is not possible. We must consider that T_w is 8 ns but only the first 2 ns of T_w have a non-null amplitude pulse. Of course, reducing the duration of pulse to 2 ns leads to the reduction

[4]PRF: pulse repetition frequency of the pulse generator, if it is 120 MHz, it means that pulse generator can convey consecutive pulses at minimum period of $\approx$ 8 ns

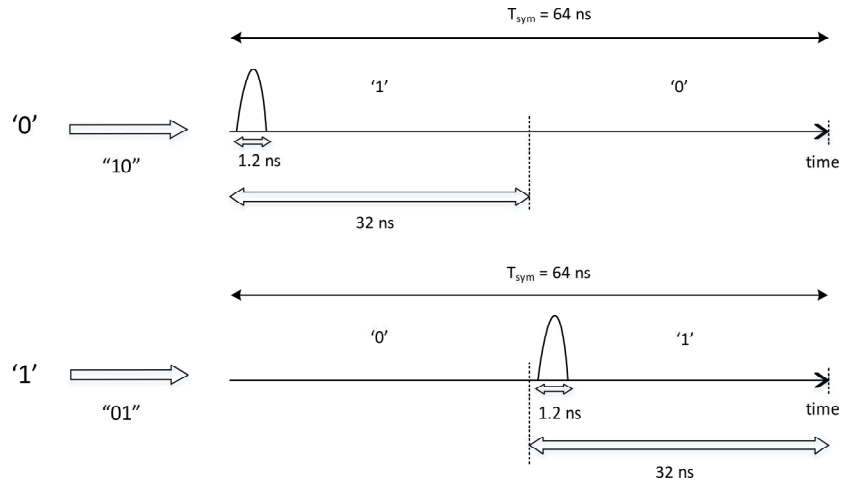


Figure 1.17 — Pulse generator output when 2-PPM schemes is employed

of mean power in SHR symbol. To maintain a right level of this mean power, we decide first to reduce the PRP within the SHR symbol from $LT_w = 128ns$ (chapter A - sub-section A.8) to $LT_w = 64ns$, and to transmit twice the number of SHR symbols. In this configuration, when sending a 1, the transmitter sends a pulse of $T_w{\sim}2ns$ and stays inactive for $63ns$. When sending a 0, the transmitter stays inactive for $64ns$ (classical OOK modulation). Considering these modifications, the SHR field will be specified as follows:

- The SHR consist on 8 preamble symbols and 1 SFD symbol: we decide to keep one SFD symbol.

- The PRP within the SHR symbol is $LT_w = 64ns$ instead of $LT_w = 128ns$ in original specification.

1.4.2.2 PSDU construction

The use of a non-coherent receiver in this work limits our choice in term of PSDU symbol modulation, since the phase information is not exploitable. Thus, only on-off signaling fits the design requirements. On-off signaling also allows higher data rates (15.6 Mbps) which gives us the possibility to address all the targeted applications (Table 1.4). However, the highest data rate of on-off signaling modes is obtained with mapping one data bit on a 2 digit code word (d_0, d_1), i.e, (1,0) for bit '0' and (0,1) for bit '1' (mapping k = 1 and M= 2, see Chapter A - Table A.5). One can see that the on-off signaling mode actually corresponds to a 2-PPM modulation. Figure 1.17 shows the output of the pulse generator for PSDU part. If the data symbol is '0', a pulse will be transmitted in the first of the symbol duration, else ('1') it will be transmitted in the middle of the symbol.

1.4.3 Non-coherent receiver structure

A low complexity non-coherent receiver based on energy detection over a short integration period is considered in this work. Figure 1.18 illustrates the structure of this receiver which was proposed in [5]. This structure embeds a low pass filter with short integration duration, in the order of the pulse duration (T_p). The goal is to obtain the envelop of the received signal as a baseband pulse. This envelop is then compared to a predefined threshold in order to determine whether a pulse is being received or not. The result of this comparison is then used as an input to the digital baseband. It should be noted that using a comparator avoids the need for an analog-to-digital converter (ADC), which significantly decreases the complexity and the cost of the receiver. Consequently, such a low complexity structure allows to detect the presence/absence of the signal rather than a more accurate amplitude information (energy estimation).

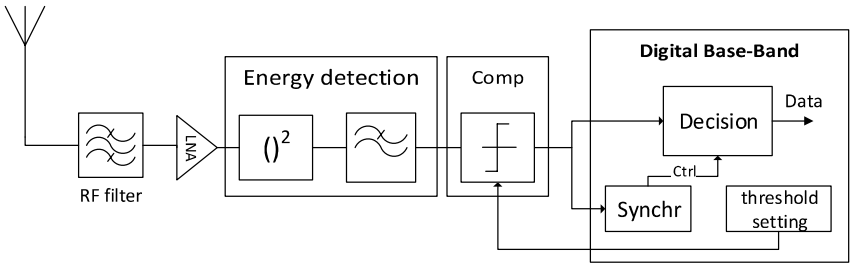


Figure 1.18 — Block diagram of the non-coherent receiver

1.4.3.1 Comparison threshold

The threshold used in comparator is set with a Constant False Alarm Rate (CFAR) method [92]. Used widely in radar applications [93–95], CFAR principle relies on setting a constant number of triggers due to the noise peaks (false alarm) that the system can tolerate with respect to the target performances. In other words, the threshold corresponding to the desired constant number of triggers namely *CFAR threshold* consists on the maximum sensitivity of the receiver for a fixed error rate. Depending on the modulation scheme, a relation can be derived to connect the BER to a false alarm probability.

The CFAR threshold is set by a calibration phase that the receiver can performs when only noise is present, either when the channel is not busy or when the antenna is disconnected. In practice, receiver starts counting the noise triggers for a fixed duration[5] and then shifts the threshold value upwards or downward if number of triggers is high or low to the desired one. This phase of calibration continues until the intended CFAR threshold is determined.

We note here that, enabling an important number of false alarms (low threshold) enhances the sensitivity of the receiver, and good performances can thus be obtained in low SNR. But, in high SNR this important number will produce an error floor, since errors will be introduced (high constant number of false alarms) even if the SNR is high. In contrast, when the number of false alarms is low (high threshold), the sensitivity of receiver decreases, therefore performances

[5] the longer it is, the better the precision acquisition

degrade in low SNR (lot of missed detections), and they improve in high SNR (low constant number of false alarms).

1.4.3.2 Determining the target CFAR

In order to set the CFAR threshold, relation between the BER and the false alarm probability must be determined. The Table 1.3 shows all possible events in AWGN channel (single path) that leads to a symbol error when taking a decision for a 2-PPM.

first PPM part event	second PPM part event	decision
missed detection (0)	good detection (0)	undefined
missed detection (0)	false alarm (1)	error
false alarm (1)	missed detection (0)	error
false alarm (1)	good detection (1)	undefined

Table 1.3 — The events leading to symbol error

The decision is made by comparison of the two PPM parts. The right decision on the symbol is reflected by the presence of signal ('1') in the part that corresponds to the transmitted symbol. Therefore, the error occurs when an event for those presented in Table 1.3 happens. In this case, the symbol error probability in AWGN channel (P_{err_sym}) is expressed as follows:

$$\begin{aligned} P_{err\_sym} &= P_m.P_0 + P_m.P_{fa} + P_{fa}.P_m + P_{fa}.P_1 \\ &= 2P_{fa}.P_m + P_m.P_0 + P_{fa}.P_1 \end{aligned} \tag{1.7}$$

where P_m is the missed detection probability ($P_{0|1}$), P_{fa} is the false alarm probability ($P_{1|0}$), P_0 is a-priori probability of no transmitted pulse "0", and P_1 is a-priori probability of transmitted pulse "1".

However, the a-priori probabilities of transmitting bits are 1/2, since the transmission of a pulse or not are equiprobable. In this case the equation 1.7 becomes:

$$P_{err\_sym} = 2P_{fa}.P_m + 1/2(P_{fa} + P_m) \tag{1.8}$$

We consider that the threshold has been set according to a CFAR criterion, P_m converge towards 0 as long as SNR is high enough. This is not the case for the P_{fa}, which is a constant value (CFAR criteria). So, even if the SNR takes a very high value, the error symbol probability will converge to a constant value of $1/2P_{fa}$, causing thereby an error floor. In this work, the P_{fa} was chosen to be 10^{-3}. This choice is made to reach a BER better than 10^{-3} to be complaint with the technical requirements of the most target applications (minimum BER = 10^{-3}, Table 1.4).

1.4.4 The targeted BAN use cases

In a typical BAN context, a wide range of applications are envisioned. When some of them imply only sensor and low volume communications, multimedia applications are dealing with audio and video transfers. Various scenarios related to consumer electronics are envisaged, that

may be classified between two categories, according to the quantity of information exchanged through the network:

- Medium data rate applications: generally include audio and commands transfers, for example audio and voice transfer between the mobile phone/PDA and the headphone/headset (audio case); or multimedia player control by the watch (commands case).
- High data rate applications: include a video transfer, for example, Tablet/phone video transfer to video glasses or the car LCD.

In RUBY project, technical requirements have been set for the above type of applications in term of different parameters, such as data rate, Bit Error Rate (BER) or quality of service. Table 1.4 summarizes these requirements for three kinds of application: control, data transfer, audio and video streaming.

Service	**Device: mobile, car, glasses...**		
Parameter	Data sharing, and control	Audio flow	visio call, video streaming
device output bit rate	$\leq$ 1 Mbps	32 kbits/s - 512 kbits/s	2 - 8 Mbits/s
Mean power consumption	Very low	Medium	High
QoS sensitivity to error	Moderate, BER = 10^{-3}	High, BER = 10^{-5}	Medium, BER = 10^{-3} - 10^{-5}
Range	5 m	2 m	2 m

Table 1.4 — General technical requirement of control commands, audio, and video applications

Although most of the elements implied for those applications must consume as little power as possible, they have different battery life constraint as they can be recharged. The command and control data stream is mostly constituted by data coming from the various sensors or to/from user interface elements. Those applications have a strong requirements on ultra low power consumption but also on reliability and low latency. However, the audio and video data stream have slightly relaxed battery life constraint due to the amount of power available in multimedia devices. In fact, video streaming is identified as the most demanding application, from the performances of the PHY, as it presents the same kind of requirements (reliability, latency) than the other plus the need for a stable data rate of several Mbits/s (up to 12 Mbps or even more for certain public safety scenarios) over a long period of time, despite any changes (interferers, shadowing) that may occur in the propagation channel during streaming duration. Only the power consumption constraint is a bit relaxed. This work seeks to propose a digital baseband algorithms that can meet these application challenge with a respect to the IEEE 802.15.6 PHY specifications.

1.5 UWB channel models

Accurate and realistic channel models are mandatory in order to evaluate the performances of a physical link. This is particularly important for the IR-UWB PHY as the algorithms and the architecture of the receiver must be adapted to the power delay profile of the channel. This is necessary for example for the choice of the paths used by Rake receiver.

The modeling of UWB channel constitutes a recent research area. This is because the narrow band channel models cannot be generalized to UWB channels given their various characteristics (*cf.* 1.1.3), particularly the large spectrum of the UWB signal. Several contributions are proposed in the literature addressing UWB channel modeling [2, 96–99]. The most important UWB channel models were published by the IEEE 502.15 task group for the IEEE 802.15.4a and IEEE 802.15.6 standards [2, 96].

1.5.1 IEEE 802.15.4a channel models

The IEEE 802.15.4a task group provides UWB models in reference [96] for the following environments in the frequency range from 2 to 10 GHz : indoor residential, indoor office, industrial, outdoor, and open outdoor environments (usually with a distinction between LOS and Non-LOS (NLOS) properties). It also provides a model for BAN's from 2 to 6 GHz frequency range. The channel models rely on Saleh-Valuenzela (S-V) model [100] which is considered as a reference of the indoor channels modeling. The model assumes that the multipath components arrive in clusters, which each of them composed of a set of paths that have a complex attenuation and delay. The expression of Channel Impulse Response (CIR) can be formulated as follows:

$$h(t) = \sum_{l=0}^{L} \sum_{k=0}^{K} a_{k,l} \exp(j\phi_{k,l}) \delta(t - T_l - \tau_{k,l}) \tag{1.9}$$

where $a_{k,l} \exp(j\phi_{k,l})$ and $\tau_{k,l}$ is respectively the complex attenuation and delay of the k^{th} component in the l^{th} cluster. T_l is cluster arrival time.

The formation of the clusters is related to the indoor environment structure, while the components within the cluster are formed by multiple reflections from objects in the vicinity of the transmitter and the receiver. The main characteristics of the proposed IEEE 802.15.4a channel models can be summarized as follows:

- The number of clusters L assumed to be Poisson-distributed with parameter mean $\bar{L}$.
- The distributions of the cluster arrival times are given also by a Poisson processes with parameter Λ_l.
- The path arrival times is modelled with mixtures of two Poisson processes with parameters λ_1 and λ_2, and a mixture probability β.
- The mean energy of the l^{th} cluster follows in general an exponential decay.
- The Power Delay Profile (PDP) is exponential within each cluster.
- The cluster decay rates are found to depend linearly on the arrival time of the cluster T_l.

However, for a BAN channel model, some modifications on the above model were necessary to accurately model a body area network scenario. This is due to the fact that in body-centric communications, devices are close to (or inside) the human body. The body is not an ideal

Scenario	Description	Frequency Band	Channel Model
S1	Implant to Implant	402-405 MHz	CM1
S2	Implant to Body Surface	402-405 MHz	CM2
S3	Implant to External	402-405 MHz	CM2
S4	Body Surface to Body Surface (LOS)	13.5, 50, 400, 600, 900 MHz 2.4, 3.1-10.6 GHZ	CM3
S5	Body Surface to Body Surface (NLOS)	13.5, 50, 400, 600, 900 MHz 2.4, 3.1-10.6 GHZ	CM3
S6	Body Surface to External (LOS)	900 MHz 2.4, 3.1-10.6 GHZ	CM4
S7	Body Surface to External (NLOS)	900 MHz 2.4, 3.1-10.6 GHZ	CM4

Table 1.5 — Propagation scenarios for BANs [2]

medium for radio frequency wave transmission due to its partial conductivity. This partial conductivity implies significant absorption of the electromagnetic energy propagated through the human body. Moreover, such medium is characterized by inherent mobility, variations in local environment, and body shape caused by movement and physiological processes (e.g. respiration). These facts illustrate the diversity of BAN channel models and the complexity of the modeling task. Reference [96] recommends for BAN channel model the following features:

- Exponential path loss around the body.
- Correlated log normal amplitude distributions.
- The number of clusters is fixed to 2 (one for the on-body and another for the ground reflection).
- Fixed inter-cluster arrival time (0.5 ns)
- Fixed inter-path arrival time (7-8 ns)
- Three scenarios - corresponding to the receiver position on the front, side and back of the body - specified with different parameters.

For more technical details, the reader can refer to [96].

1.5.2 IEEE 802.15.6 channel models

The channel modeling subgroup within TG-IEEE802.15.6 has developed channel models to evaluate the performance of PHY layers in the BAN context. As mentioned above, the results of this activity are summarized in [2]. Different frequency bands have been studied as well as different scenarios in the BAN context (Table 1.5).

These scenarios are determined based on the locations of BAN nodes: (1) inside the human body (implant), (2) in direct contact with the skin or within 2 cm distance (Body surface), and (3) beyond 2 cm and up to 5 m from the body surface (external). S1, S2, and S3 correspond to implant nodes in a BAN. The propagation in these scenarios is characterized by CM1 and

CM2 channel models, with allocated frequency band 402-405 MHz that belongs to medical implant communication services (MICS) bands. CM1 and CM2 are not used to model UWB channels, and will not be used in this PhD work. S4, S5, S6, and S7 correspond to body surface and external nodes. Two different channel models, CM3 and CM4, are used to characterize the propagation in these scenarios. Different frequency bands have been allocated for these scenarios including the UWB band.

1.5.2.1 CM3 channel model: body surface to body surface

The CM3 channel model defines a body surface to body surface link for both LOS and NLOS scenarios. CM3 is intended to operate in seven different bands, including the UWB band (3.1 to 10.6 GHz). Three approaches were proposed to model the CM3 channel but only one gives a Power Delay Profile (PDP), *ie.* the delays and amplitude of each multipath components. The other approaches provide only a Path-Loss (PL) model which means that no assumptions can be made on the time-distribution of the overall received energy.

For a realistic PHY simulation, a channel model with multipath components is necessary to estimate the main paths and to combine them (RAKE receiver). Table 1.6 summarizes the expression and the different parameters of the considered path-loss model where a and b are coefficients of linear fitting, d is Tx-Rx distance in mm, and N is normally distributed variable with zero mean and standard deviation σ_N, which represents the contribution of shadowing in the variation of the path loss. These parameters are based on measurements that have been conducted in an anechoic chamber and a hospital room, covering the frequencies of the UWB band (3.1 to 10.6 GHz). More information about the measurement settings can be found in [101].

	Hospital Room	Anechoic Chamber
Path loss model	$PL(d)[dB] = a.log_{10}(d) + b + N$	
a	19.2	34.1
b	3.38	-31.4
σ_N	4.40	4.85

Table 1.6 — Path-loss model and corresponding parameters [2]

A corresponding PDP of this approach is given in Table 1.7. This PDP expresses the CIR. The description of the corresponding parameters implied in the expression is also provided:

- a_l: path amplitude for the l^{th} path
- t_l: path arrival time for the l^{th} path
- ϕ_l: phase for the l^{th} path
- L: the number of the arrival paths
- $\delta(t)$: the Dirac function
- Γ: an exponential decay with a Rician factor γ_0
- S: a normal distribution with zero-mean and standard deviation of σ_s

- λ: path arrival rate

- $\bar{L}$: the average number of the L

PDP Model		$h(t) = \sum_{l=0}^{L-1} a_l \exp j\phi_l \delta(t - t_l)$ $10log_{10}\|a_l\|^2 = \gamma_0 + 10log_{10}(\exp(\frac{-t_l}{\Gamma})) + S \;\; l \neq 0$ $p(t_l\|t_{l-1}) = \lambda \exp(-\lambda(t_l - t_{l-1}))$ $p(L) = \bar{L}^L \frac{\exp(\bar{L})}{L!}$ ϕ_l is modeled by a uniform distribution over [0,2π]
a_l	γ_0	-4.60 dB
	Γ	59.7
	σ_s	5.02 dB
t_l	$1/\lambda$	1.85 ns
L	$\bar{L}$	38.1

Table 1.7 — Power delay profile for CM3 [2]

As every measurement-based model, the validity of this PDP model is related to the experimentation conditions and the quantity of data acquired to develop the model.

1.5.2.2 CM4 channel model: body surface to external

CM4 determines a body surface to external link for both LOS and NLOS. It is applied to three different frequency bands, including the UWB band. As for the CM3 case, only one approach provides a PDP. Derived model and corresponding parameters are given in Table 1.8, where:

- $h(t)$: Complex impulse response

- L: Number of arrival paths, modeled as Poisson random variable with mean $L = 400$

- α_m: Amplitude of each path

- $\tau_{m=1...L-1}$: Timing of path arrivals, modeled as Poisson random process with arrival rate $\lambda = 1/(0.50125ns)$

- k: Effect of K-factor (NLOS)

- ω_0: Path loss (can be assumed as free space)

- d: Tx-Rx distance

- c: Velocity of light

These parameters are based on measurements that have been conducted in office environment. Tx antenna was static close to a wall while Rx antenna was placed on body surface (waist). Human body was moved in the room, but also rotated, 0° being the case where Rx and

Model	$h(t) = \sum_{m=0}^{L-1} \alpha_m \delta(t - \tau_m)$ $\alpha_m^2 = \Omega_0 \exp(\frac{-\tau_m}{\Gamma} - k[1 - \delta_m])\beta$ $k = \Delta k(ln10/10)$ $\tau_0 = d/c$ $\beta \sim lognormal(0, \sigma)$		
Direction of Body	$\Gamma[ns]$	$k(\Delta k$ [dB])	σ [dB]
0	44.6346	5.111 (22.2)	7.30
90	54.2868	4.348 (18.8)	7.08
180	53.4186	3.638 (15.8)	7.03
270	83.9635	3.983 (17.3)	7.19

Table 1.8 — Power delay profile for CM4 [2]

Tx antennas are face to face. More information about the measurement settings can be found in [102].

It was noted in [102] that in 0° case (front-of-body), the direct path component can be seen as the first impulse response and the other multi-path responses became a cluster. On the other hand, in side-of-body case (90° and 270°) the direct path component was attenuated, while it was vanishing in backside-of-body case (180°).

1.5.2.3 UWB-BAN channel conclusion

The knowledge of the propagation channel can predict the wave behavior in the human body environment. The presence of this latter being the essential element that differentiates BAN channel from the previous UWB channels.

From the four channel models provided by IEEE802.15.6 channel model subgroup, only two channels include UWB (CM3 and CM4). UWB was excluded from scenarios requiring implant devices for the reason that the transmitted signals from implant nodes undergo significant attenuation as they propagate through various tissues and organs. In fact, for this category of communications, the MICS band is already known and experienced, and it seems better suited.

The description of the CM3, and CM4 channel models is not sufficiently refined compared with what is provided for the other frequencies (ISM). Moreover, large dispersion of results and models was observed in particular with regard to the path loss. This is partially due to the fact that each measurement has been carried out with different methodologies and approaches, resulting in models which are too specific.

Nevertheless, since the publication of the standard, some UWB-BAN channel modeling studies have been performed ([103, 104]) in order to improve the channel model accuracy. Furthermore, the feasibility of UWB transceivers for implantable devices shown in reference [105] has encouraged the research to model the propagation channel for UWB implantable devices [106–108]. This should also improve UWB-BAN channel modeling.

1.6 Summary

This first chapter provided the required background on IR-UWB communication systems in general, and more specifically on the RUBY project requirements, in order to present the specific contributions of this PhD work in the next chapters.

Regarding IR-UWB communication systems, both transmitter and receiver architectures are outlined. At the transmitter side, different state-of-the-art techniques in terms of modulation types, multiple access, and pulse generation were presented. At the receiver side, coherent, non-coherent and differential receiver topologies were detailed together with state-of-the-art related signal processing techniques.

Regarding the work context, the chapter has focused on the presentation of the specific UWB PHY layer parameters and the target receiver structure that have been considered in the RUBY project. The adopted pulses, together with the PHY frame format and the non-coherent receiver were detailed. Different use cases defined in this project were also presented in order to give an overview of the specific requirements needed to be supported by the proposed contributions in this PhD work.

Finally, the chapter ended with the presentation of few relevant BAN channel models, defined in the context of the IEEE 802.15.6 standard. Accurate and realistic channel models with corresponding parameters are presented for the target scenarios of body surface to body surface and body surface to external. Such models are crucial for the proposal of appropriate algorithms at the receiver side and for accurate performance evaluation. They will be used in the next chapters to validate the contributions of this PhD work.

CHAPTER

2 Non-coherent receiver baseband algorithms

THIS chapter presents the PhD thesis contributions related to the proposal of non-coherent IR-UWB baseband algorithms for BAN applications. The proposed algorithms are compliant with IEEE 802.15.6 standard and target the requirements of RUBY project, as described in Chapter 1. In order to implement a non-coherent receiver, several issues must be solved. Towards this target, the chapter presents first a flexible and efficient synchronization algorithm based on inter-pulse time interval detection. Then, a simple SFD detection technique that relies on a correlation method is presented. In addition to detecting the starting of data field, the proposed technique enables to estimate the error probability of the received signal. Furthermore, an efficient path selection estimator is proposed and used both for detecting the multipath components and the estimation of their reliability by exploiting the resolution of the adopted non-coherent receiver. Finally, the chapter introduces a fusion decision algorithm based on multipath processing and supporting PPM modulation scheme. The achieved performance of each proposed algorithm is evaluated independently, and then the whole non-coherent baseband is simulated using the IEEE 802.15.6 BAN channel models.

2.1 Non-coherent receiver issues: proposed receiver

Before describing in more details the proposed digital baseband, we provide an overview to clarify the interaction between the proposed algorithms. This interaction is shown in Figure 2.1.

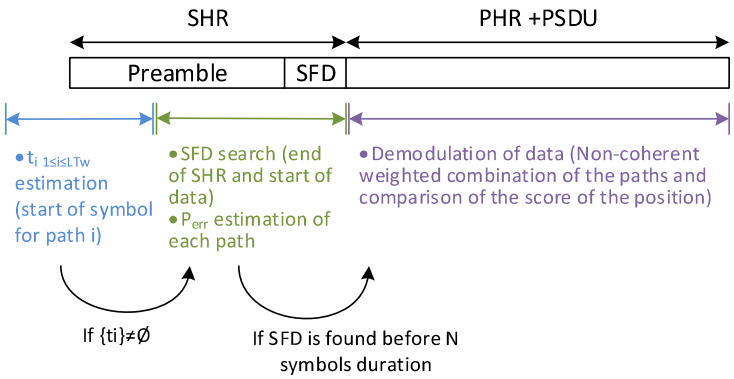


Figure 2.1 — Digital baseband algorithm interaction scheme

When receiving data, the first action of the receiver is to acquire synchronization. This is possible during the preamble, and the receiver can then estimate the position of the preamble symbol, as well as the position of incoming paths (path selection estimation) resulting from multipath propagation. Synchronization information is then given to the SFD detector. The aim of the detector is to estimate the error probability (P_{err}) of each detected path by exploiting the remaining SHR symbols, and to track at the same time the SFD symbol. If the SFD is detected, useful data are being received, and the receiver will start demodulation, otherwise the packet will be missed.

2.2 Synchronization algorithm

2.2.1 General principles

The aim of the synchronization algorithm is to determine precisely if we are currently receiving useful data, and which part of the packet is currently being processed. The algorithm is based on the time interval between pulses in the synchronization symbol. In order to illustrate the algorithm and its principles, the fourth Kasami sequence (C_4) will be used. This sequence can be represented using its binary values, depicted in the upper part of Figure 2.2. During the transmission, a bit of value '1' corresponds to the sending of a pulse, while a bit of value '0' corresponds to the absence of sending a pulse. The notion of slot is used here to simplify the explanation of the algorithm, so one slot is a time quantity which represents the duration of one bit. Thus, when C_4 is sent, a pulse will be transmitted in the second slot, then 3 slots will stay unused, before having a new slot with a pulse, and so on. On the receiver side, this means that there will be a time interval of four slots between the first two pulses. This sequence can thus be represented using a time interval representation, as presented in the lower part of Figure 2.2

The use of time distances has first been described for a specifically designed synchronization symbol in [5]. This symbol had no repeating time intervals, which allowed straightforward

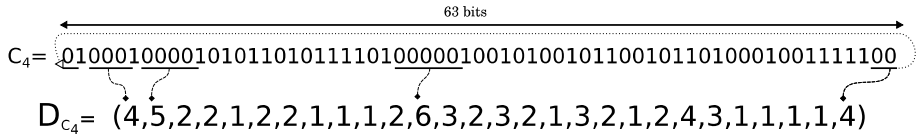


Figure 2.2 — Representations for Kasami sequence C_4

operation. However, in the IEEE 802.15.6 case, the Kasami sequence has many distances which are not unique. The new flexible technique proposed in this work is designed to process any synchronization sequence.

2.2.2 Detailed description

The proposed algorithm is based on the use of a finite state machine which checks the correlation between the received symbol and the expected one. It uses a time distance computation. When a pulse is received, a time counter is reset, and incremented at each time slot. Its value when the next pulse is received gives the time interval between the two pulses. The detection of a pulse corresponds to a threshold crossing of the integrated power over a time slot length. When no threshold crossing happens in a time slot, this means that no pulse has been received.

Algorithm 1 Transition function for the finite state machine

procedure TRANSITION
  compute distance with previous pulse
  switch $state$ **do**
    case $State_0$
      if distance $==$ d_j **then**
        if $d_j \in$ repetitive distances **then**
          $state \leftarrow State_{Int}$
        else
          $state \leftarrow State_{corr}$
          position $\leftarrow j$
          detected_impulse(j) $\leftarrow 1$
        end if
      end if
    case $State_{Int}$
      if one possible subsequence remaining **then**
        $state \leftarrow State_{corr}$
        position $\leftarrow j$
        $detected\_impulse(j) \leftarrow 1$
      else if multiple subsequences **then**
        $state \leftarrow State_{Int}$
      else
        $state \leftarrow State_0$
        detected_impulse $\leftarrow (0, \ldots, 0)$
      end if
    case $State_{corr}$
      if distance $==$ d_{j+1} **then**
        position $\leftarrow j + 1$
        $state \leftarrow State_{corr}$
        detected_impulse($j + 1$)$\leftarrow 1$
      else
        $state \leftarrow State_0$
        detected_impulse $\leftarrow (0, \ldots, 0)$
      end if
  end switch
  if detected_impulse $== (1, \ldots, 1)$ **then**
    synchronization acquired
    position
  end if
end procedure

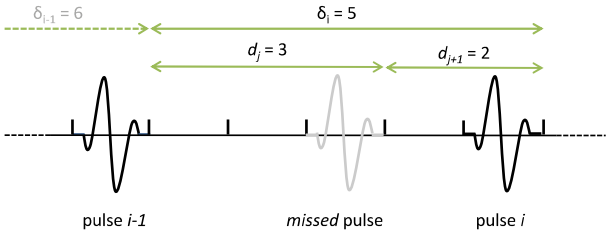
Algorithm 1 describes the transition function of the finite state machine. The description below refers to the line numbers in Algorithm 1. State transitions occur when a pulse is received. The aim of this state machine is to detect a correlation between the sequence being received and the expected sequence (in this case, the fourth Kasami sequence). Three different state types are defined. The idle state, named $State_0$ (line 4) in Algorithm 1, represents the case when no correlation has been detected. For example, if two pulses with distance $\{25\}$ are received, they obviously do not belong to the sequence.

The correlation state, named $State_{corr}$ (line 25, represents the case when the received sequence is currently (partly) correlated with the expected sequence. In this state, the complete sequence has not yet been found, but a part of it has been detected, and we want to know if the next pulse is still in the sequence. The position in the expected sequence, defined as the distance index in the sequence, is stored in the "position" variable. The previously detected positions are also stored, in the "detected_impulse" vector. When the state machine is in state $State_{corr}$, with position j and the new computed distance matches the distance $j+1$ (line 26), the position is updated to $j+1$, and the "detected_impulse" vector is updated. If it does not match (line 30), the state machine goes back to idle state $State_0$, since the sequence being received does not match the expected sequence. When all positions have been detected, the "detected_impulse" vector is filled with 1 in the algorithm, and the synchronization is acquired (line 35). The last position that enabled this synchronization is also provided by the position index.

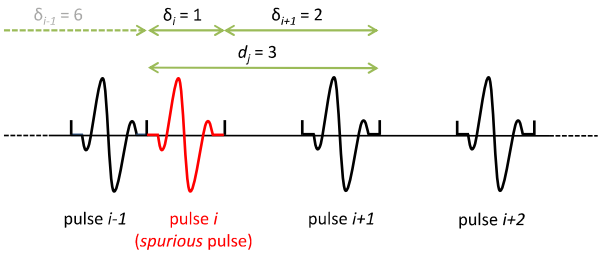
The last state type is the intermediate state or $State_{int}$ (line 14), which represents cases when the correlation with the sequence can not be immediately decided. This occurs when a distance is received which can represent more than one position in the expected sequence. These distances are called repetitive distances in the algorithm. In this case, the state machine stays in this temporary state as long as no decision can be taken. For example, if the algorithm finds a distance 3, there are many possible combinations ($\{3,2,3\}, \{3,2,1,3\}, \{3,2,1,2\}, \{3,1\}$), and the position can not be decided. When the next distance is received, if it is $\{2\}$, the case of $\{3,1\}$ is discarded, but the sequence may still match the expected one (line 19). If it is a $\{1\}$, then only the $\{3,1\}$ sequence matches, and the state becomes $State_{corr}$ (line 15). The positions are updated accordingly. If it is neither a $\{2\}$ nor a $\{1\}$, no correlation has been found and the algorithm goes back to state $State_0$ (line 21).

In this simple version, the algorithm is very sensitive to missed or spurious pulses. Optimizations have been made to better take into account these errors. For the sake of clarity, these optimizations have not been represented in Algorithm 1. The main idea behind these modifications is that when a detected distance δ differs from the expected one d_i, it is not discarded immediately. Therefore, the comparisons to decide whether a distance matches the expected one is less strict, and can be made with the sum of expected distances (missed pulse case) or the sum of received distances (spurious pulse case). An example of such optimizations is shown in Figure 2.3

For example, if a distance $\delta_{i-1} = \{6\}$ is received, expected next distance is a $d_j = \{3\}$. However, if the next pulse is missed, the next distance might be a $\{5\}$, which could be the sum of $d_j = \{3\}$ and $d_{j+1} = \{2\}$, the two distances following $\{6\}$ (Figure 2.3a). If a $\delta_i = \{5\}$ is received, the algorithm will not stop, and the decision will be according to the next distance. On the opposite, the two next received distances could be $\delta_i = \{1\}$ and $\delta_{i+1}\{2\}$, which should be discarded. However, the sum of the received distances is $\{3\}$, and this error could be caused by



(a) example of missed pulse case



(b) example of spurious pulse case

Figure 2.3 — Example of optimizations to handle missing and spurious pulses

noise. This sequence can be kept if the subsequent distances match (Figure 2.3b).

The number of acceptable spurious and missed pulses between two valid pulses can be set in the above described algorithm. However, the system model affects the choice of the aforementioned number of acceptable spurious and missed pulses. When the CFAR threshold is high, the number of spurious pulses will be very low in the received bit stream. In this case, it is useless to manage an important number of spurious pulses in the algorithm, since this case is very unlikely in typical transmission. The best choice in this case is to accept an important number of missed pulses to have good performance in low SNR. On the opposite, when the CFAR threshold is low, missed pulses are unlikely, but the probability of spurious pulses increases. A bigger number of spurious pulses should thus be accepted.

Independently of the system model, tolerating a small number of spurious and missed pulses will reduce the probability to effectively synchronize on relatively low power signals. This will reduce the algorithm sensitivity by the fact that higher SNR is required to synchronize. But at the same time, such small numbers will increase the synchronization reliability. On the opposite, tolerating a high number of spurious and missed pulses can increase the algorithm sensitivity, however it can lead also to have many false synchronizations, which weakens thus the algorithm reliability.

In this work, we decided to accept 3 spurious pulses and one missed pulse between two valid pulses. These values are the outcome of a study of the channel, and based on the front-end parameters (mainly the CFAR setting). In fact, performing extensive simulations shows that above 3 spurious pulses, or 1 missed pulse, the transmissions were increasingly erroneous because of the important rate of false synchronizations. This means that using higher threshold values would have decreased the reliability of the synchronization algorithm. The simulations also show that below 3 spurious pulses, or 1 missed pulse, the transmission needs higher SNR values to be detected (less acquired synchronization), reducing the sensitivity of the algorithm.

Practically, if the state machine validates the *pulse i*, it waits the next pulse to validate or

not the detection of the *pulse i+1*. If the next detected pulse is not the $i + 1^{th}$ one (checked as described above), the state machine will first check if there was a missed pulse and that the actual pulse corresponds to the $i + 2^{th}$ one, else, it considers that the actual pulse is the first spurious pulse. If it is the latter case, the state machine waits again the next pulse, once occurs; it checks it. At this stage there is two possibilities: either the new occured pulse is the $i + 1^{th}$ one, or it is the second spurious pulse. This process is repeated until we detect the $i + 1^{th}$ pulse, or reach the limit of three spurious pulses. If the detection of $i + 1^{th}$ pulse failed, the state machine would consider that all prior validated pulses are not correct, goes back to the initial state $State_0$, and restarts a new synchronization research.

2.3 SFD detection algorithm

The detection of the SFD symbol is necessary both to detect the start of the packet data and to validate the acquired synchronization. In this section, SFD detection technique based on correlation method and targeting a non-coherent receiver is proposed. The technique is selected among two possible techniques after analyzing their performances.

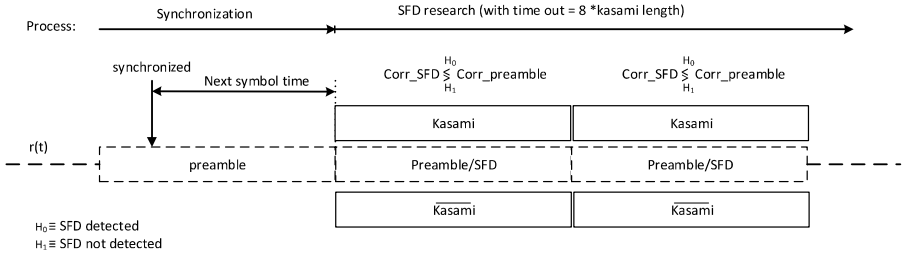
In the RUBY project, as in the IEEE 802.15.6 standard, the SFD symbol is the inversion of the Kasami sequence used in the preamble (*cf.* Chapter 1 and Appendix A). This choice is taken to minimize the correlation between the SFD and preamble fields.

When the synchronization is acquired by the receiver, the symbol boundary can be deducted, and the beginning of the next symbol will be known. This is possible thanks to the state machine that provides the position of the last detected pulse within the Kasami sequence. Based on this, a solution to detect the SFD is to perform a cross-correlation between the received signal and a local Kasami sequence, and decide then the SFD based on the correlation result (Figure 2.4). Using this approach, two methods can be used for SFD detection: a *score comparison* or a *peak detection*. When using *score comparison* (Figure 2.4a), both Kasami (preamble symbol) and inverted Kasami sequences are correlated with the received signal. Simply comparing the correlation scores indicates if the current received signal is a preamble symbol or a SFD one. When implementing *peak detection*, only one correlation is performed (Figure 2.4b), it is the correlation between the Kasami sequence and the received signal. The correlation result is then compared to a threshold (which needs to be defined *a priori*) to decide whether the SFD is detected or not.

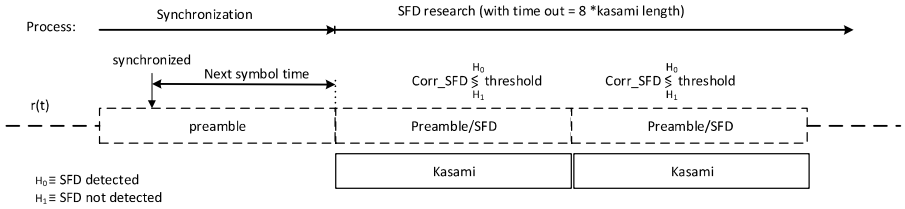
The aforementioned cross-correlation can be modeled as follow:
$C = (c_0, c_1, ..., c_{62})$
$\bar{C} = (\bar{c}_0, \bar{c}_1, ..., \bar{c}_{62})$

$$corr_{preamble}(r[n], C) = 63 - \sum_{j=0}^{j=62} [(2r_j - 1).(2c_j - 1) + 1]/2 \tag{2.1}$$

$$corr_{SFD}(r[n], \bar{C}) = 63 - \sum_{j=0}^{j=62} [(2r_j - 1).(2\bar{c}_j - 1) + 1]/2 \tag{2.2}$$



(a) Correlation score comparison



(b) Peak correlation detecting

Figure 2.4 — Cross-correlation methods for detecting SFD

where $corr_{preamble}$ is the score of correlation between the received signal and Kasami sequence in a window of 63 bits (Kasami length) used to detect the presence of preamble symbol, $corr_{SFD}$ is the score of correlation between the received signal and inverted Kasami sequence in a window of 63 bits (Kasami length) used to detect the presence of SFD, C is the Kasami sequence, $\bar{C}$ is the inversion of Kasami sequence, and $r[n]$ is the received signal. It is interesting to note that $corr_{preamble} = 63 - corr_{SFD}$, since computation is done on inverted reference sequences. As a result, when implementing the algorithm, only a single correlation needs to be computed. The other correlation can be obtained with a subtraction, or by inverting the expected range for both correlation values. For example, correlation for the SFD will be maximum when $corr_{SFD} = 0$, and minimum when it is 63, while correlation for preamble will be minimum when $corr_{preamble} = 0$, and maximum when it is 63. However, these are implementation details that are the focus of Chapter 3. In this chapter, we consider that a correlation score of 0 means that the correlation is maximum, and 63 means that there is no correlation. For both proposed detection techniques (*peak detection* and *score comparison*), three cases are considered below.

2.3.1 Ideal reception with a valid synchronization

The ideal reception corresponds to the case where there is no false alarm or missed detection during the signal detection. In such condition, and assuming that the detected synchronization is valid, $corr_{preamble}$ and $corr_{SFD}$ of the equation 2.1 will have respectively a value of 0 and 63, if the received signal belongs to the preamble field. Else, if the signal belongs to the SFD field, $corr_{preamble}$ will have a value 63 and $corr_{SFD}$ a value 0. In this first case, both techniques can easily detect the SFD symbol. Comparison results is easy and reliable, and any realistic threshold value will be sufficient for peak detection to give the correct result.

2.3.2 Real reception with a valid synchronization

In real reception, it is expected to have false alarms and missed detections on the detected signal. This impacts the correlation score, as these false alarms and missed detections insert errors when receiving the signal. If we preserve the assumption that synchronization is well detected, the values of $corr_{preamble}$ and $corr_{SFD}$ will depend on the number of errors, and they become:

$$corr_{preamble} = \begin{cases} N_{fa} + N_m & if \;\; r(t) \in \{preamble\} \\ 63 - (N_{fa} + N_m) & if \;\; r(t) \notin \{preamble\} \end{cases} \tag{2.3}$$

$$corr_{SFD} = \begin{cases} N_{fa} + N_m & if \;\; r(t) \in \{SFD\} \\ 63 - (N_{fa} + N_m) & if \;\; r(t) \notin \{SFD\} \end{cases} \tag{2.4}$$

where: N_{fa} is the number of false alarm in window of 63 bits, and N_m is the number of missed detection in window of 63 bits.

For example, if the current received window (63 bits) has one missed detection ($N_m = 1$) and two false alarms ($N_{fa} = 2$), the number of errors is 3 ($N_{fa} + N_m$), and the correlation score will have a value of 3 or 60 depending on the current SHR fields. For the *score comparison* technique, even in the presence of errors, the difference between $corr_{preamble}$ and $corr_{SFD}$ remains obvious, and the SFD can be detected even if the number of bit errors takes important values (theoretically up to 31, which would prevent synchronization). For the *peak detection* technique, setting a threshold on correlation score depends on the number of error that can be accepted.

2.3.3 Real reception with invalid synchronization

When invalid synchronization is acquired, the SFD detection technique should be able to detect the error. This will improve the reliability of the system, and avoid processing when it is not necessary since the receiver will not process an incorrectly detected packet. Such a prevention technique may save the system energy.

When the receiver acquires a false synchronization, the deducted symbol boundary will be wrong, and the correlation window will not be correctly aligned with the SHR symbol. As a result, the local sequence will be correlated either by noise (synchronization on noise), interferer (synchronization on interferer), or shifted SHR symbol (bad synchronization). In such case, it is not easy to predict the behavior of both techniques with respect to SFD detection. Performance comparison must be performed to understand this behavior. Such comparison is done below.

2.3.4 Selection of the best technique

In order to select the best technique, we have to estimate the wrong decision probability of the SFD in both techniques. To achieve that, simulations were performed in CM3 and CM4 channel models, and in the absence of signal (noise case). The wrong decision probability is similar to

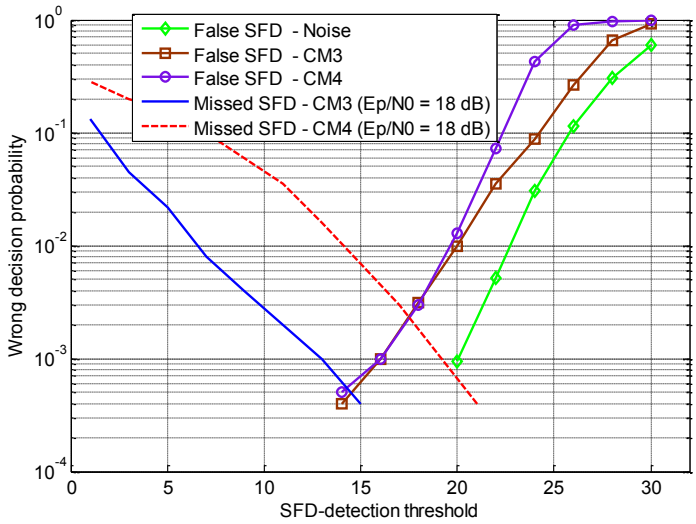


Figure 2.5 — Probability of false and missed SFD detection in different cases - peak detection technique

false SFD detection probability (P_f^{sfd}) when we are outside the SFD and missed SFD detection probability (P_m^{sfd}) when we are inside the SFD.

First, for the *score comparison* technique, it was observed that false synchronization almost implies systematically a false SFD detection in all cases (multipath and noise), with a probability (P_f^{sfd}) of 0.96. In the case of a valid synchronization, P_m^{sfd} depends of course on the SNR values. At Ep/N0 of 18 dB, P_m^{sfd} was found to be less than 0.004. This means that almost no missed SFD detection will happen when the synchronization is valid. This technique has a good performance when the synchronization is correctly detected, but we can not count on it to stop false detection.

For the *peak detection* technique, the wrong decision probability on the SFD depends on the SFD-threshold detection value. So, we have to jointly estimate the SFD-threshold detection and the wrong decision probability. Figure 2.5 shows simulation results for this technique in function of SFD-threshold detection. The different SFD-threshold values represent the error bit number ($N_{fa} + N_m$) in a window of size 63 bits.

A P_f^{sfd} of 0.001 is observed at threshold value of 16 in multipath channels, while the same probability is obtained at 20 when only noise is present at the receiver. However, if we must set a threshold value to minimize the false SFD detection, the judicious choice would to select a threshold value from the interval [0 - 16].

For the missed SFD detection, CM4 case looks worse than CM3 case for an Ep/N0 of 18 dB. This is mainly because CM4 paths have less energy than the CM3 case. CM4 delay spread is longer compared to CM3, and it has a high number of paths ($\approx$ 400 paths) when in CM3 this number is kept relatively low ($\approx$ 38 paths) (see Chapter 1, Table 1.7 and 1.8). Thus, there is more missed bits in CM4 than CM3 which leads to less bit errors in CM3, and consequently lower P_m^{sfd}. In CM3, P_m^{sfd} is less than 0.001 when threshold value exceed 13. In CM4, when threshold value exceed 14, P_m^{sfd} is less than 0.01.

From what precedes, it is clear that the *peak detection* technique outperforms the *score comparison* one if appropriate threshold value is chosen. We decide in this work to choose

the peak detection technique with threshold value of 14 (tradeoffs between false and missed SFD detection performances). This means that our system can tolerate up to 14 bit errors when detecting the SFD. This choice is taken to avoid the false and the missed SFD detection at the same time. The *peak detection* technique is also chosen to minimize resource and energy consumption when a hardware implementation is targeted as the receiver processing is avoided when false synchronization is detected.

Concerning the number of acceptable bit errors, we can show that accepting 14 bit errors will not impact the system performance. Technical requirements for the IEEE 802.15.6 IR-UWB BAN targets a 10% Packet Error Rate (PER). This rate is dependent on the complete receiver, however, in order to avoid problems due to SFD detection, wrong SFD decision probability must be at most 10% (or SFD success rate at least 90%). With a threshold of 14 bit errors, the wrong SFD decision value is clearly negligible compared to the required PER value, so it will not impact the link performances. Furthermore, a SFD threshold setting at 14 bit errors will improve the receiver sensitivity when detecting SFD compared to lower threshold values (less bit errors), as the system tolerates more missed detections (N_m).

2.4 Channel estimation and path selector

Both synchronization and SFD detection algorithms described above are valid for any IR-UWB non-coherent receiver. These algorithms just need a bit stream at their input that represent the received signal (1: detected signal, '0': absence of signal). From this stage, the algorithms are applicable.

Here, we propose a parallel scheme to take advantage of multipath diversity of the IR-UWB signal. In other words, we propose a non-coherent CIR estimation. This is possible in our RUBY context, since the adopted receiver provide a fast sampling (1 GHz) of the received signal (*cf.* section receiver). The proposed parallel scheme consists on multiple branches, typically LT_w branches, each of them embedding one synchronizer cascaded with one SFD detector (Figure 2.6). The number of branches is related to the fact that the transmitted pulse has a PRP of LT_w ns, which means that we can detect up to LT_w paths (with 1 ns resolution) for a transmitted pulse. Certainly, a such scheme will be complex compared to the serial one, but this complexity is compensated by an improvement of performance as appear clearly in performance section 2.6.

Figure 2.6 describes the transmitted SHR symbol, as well as the aforementioned parallel architecture. Each synchronizer is responsible to detect a synchronization on its own branch. If a synchronization is acquired in the branch, the synchronizer conveys the synchronization information to the SFD detector which in turn validates (if the SFD is detected) or not (SFD not detected) the detection of a path in this branch. In other words, one detected path corresponds to an acquired synchronization, followed by a detected SFD on one branch. Practically, when synchronization is acquired on the i^{th} synchronizer, this latter provides the position of the last detected pulse within the preamble symbol to the i^{th} SFD detector. Based on the position information, the detector computes the instant of the start of the next SHR symbol (symbol boundary). From this instant, the SFD detector starts the research of SFD, as explained in previous section. In fact, the result of the correlation that performs the SFD detector is stored for further use for computing error probability. Thus, having multiple parallel branches, multiple

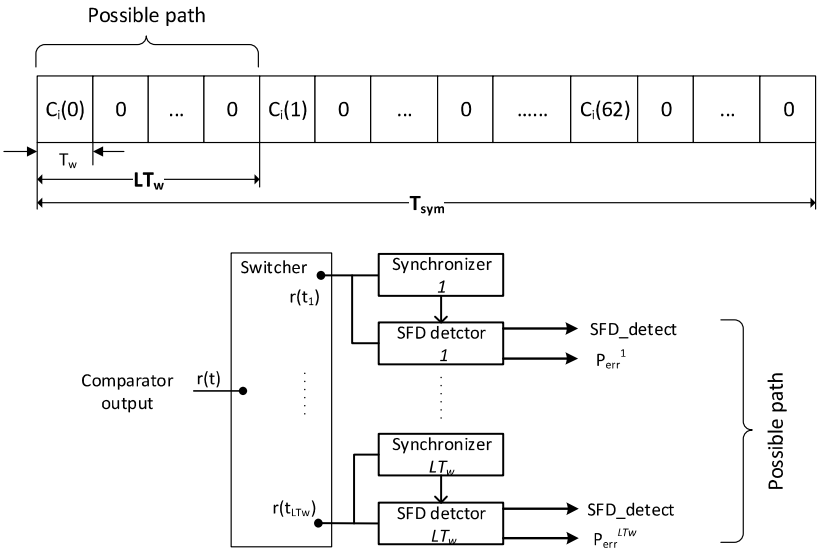


Figure 2.6 — Multipath estimator structure

paths can be detected, performing a CIR estimation.

The SFD detector can be used to sort the validated paths according to their reliability. The principle consists in exploiting the number of bit errors measured by the SFD detector during the SFD research (cf.2.3) as reliability criterion of the detected path. In other words, this number of bit error is used to compute the bit error probability P_{err}. This P_{err} can be computed for each detected path as the ratio between the measured number of bit errors and the total number of measured bit. In such configuration, when the P_{err} of the path is low it is considered more reliable than the path having a higher probability. Thus, an important weight is assigned to the reliable path, against of a smaller weight to the less reliable path when performing a decision.

However, in order to make a reliable estimation of the number of errors, estimation should be done for a long stream. This is possible if synchronization is quickly acquired, since enough time (i.e. SHR symbols) is saved to perform reliable estimation. For real-time and hardware implementation reasons (see Chapter 3, sub-section 3.2.2.1), this estimation will be carried out over 2 SHR symbols for each detected path (126 bits).

To have an idea on the reliability of this estimation, we must compute the confidence interval or error margin for this estimation. First, the vector resulting from the correlation contains a set of bits, each of them has a Bernoulli distribution with value '1' represents an error, and '0' no error. Thus, the sum of these bits which is the number of errors $(N_{fa} + N_m)$ is a random variable that follows a binomial distribution (sum of Bernoulli random variable) with parameters P_{err} and N noted $\beta(P_{err}, N)$ where $P_{err} = N_{fa} + N_m/N$ and N is the sample size (126 bits). Since N is large enough (126), the binomial distribution $\beta(P_{err}, N)$ can be approximately assigned to a normal distribution according to the central limit theorem. In this case, the empiric mean P_{err} follows a normal distribution with variance σ^2/N noted $\mathcal{N}(P_{err}, \sigma^2/N)$, where $\sigma^2 = P_{err}(1 - P_{err})$. The error margin in a normal distribution is defined to be $e = 1.96.\sqrt{P_{err}(1 - P_{err})/N}$ at 95% confidence level. One can see that the larger N is, the better the estimation precision. Table 2.1 gives error margins for some number of errors that belongs to the acceptable error interval [0 - 14]. We note here that when no event is detected (*ie* no error), the error margin is

error number	P_{err}	error margin(95% confidence interval)
0	0	$\approx 2\%$
1	1.6%	$\approx 2\%$
7	11%	$\approx 5\%$
14	22%	$\approx 7\%$

Table 2.1 — Error margin of some number of errors

computed as follows: if no events are observed in a sample of size N, the error margin is 3/N at 95% confidence interval [109].

The performed estimation allows to differentiate probabilities of cases fairly spaced as the case of $P_{err} = 1.6\%$ and 11% with respectively a confidence interval of [0% - 3.6%] and [6% - 16%] (no overlap). Nevertheless, overlaps exist between close values of P_{err}. This can cause a biased estimate, such as in the case where P_{err} = 11% and 22% with confidence intervals of [6% - 16%] and [15% - 29%]. However, small under- or over-estimates occur more frequently than large under- or over-estimates. This means that when we estimate P_{err}, we are more likely to obtain value close to the mean value (center of confidence interval) than to get a value far from the mean. Therefore, the previous estimation mostly gives reliable P_{err} values.

2.5 Decision fusion algorithm

Demodulation of the received signal means that a decision must be taken regarding the transmitted signal: was it a '1' or a '0'? A simple way to take a decision in multipath processing is the majority vote on the number of detected path. However, this is not necessarily the best way to proceed, because such a method gives the same importance to paths that have different reliability, and consequently, the technique will be more sensitive to noise and interferer when taking a decision.

The decision technique proposed here can be assimilated to a *SRake* receiver with MRC combination method. Based on a multipath processing, the technique consists in a combination of a weighted paths and comparison targeting a M-PPM modulation scheme. Paths and their weighted coefficients are estimated thanks to the synchronization task. The weighted coefficient represents the reliability of the path. The advantage of such a technique is that it discriminates between a reliable path and another which is less reliable. Thus, it gives more consideration to the reliable path when making a decision. This can mitigate the noise and interferer effects.

Several works deal with multipath processing with weighted coefficient. For example, the work described in reference [110] proposes an energy detection weighted technique which rely on weighting each path with a coefficient that represents its power level. In our non-coherent approach, energy estimation is not possible, this is why we propose an alternate method that relies on probability estimation. Such a technique was proposed in Radar field [111], and adapted to the field of sensor networks by [112]. Taking into account the adopted physical (IEEE 802.15.6 standard), receiver structure, and target objectives in term of low complexity and low cost architectures, we propose here a decision algorithm that aims at demodulating M-PPM scheme.

The schematic of the proposed decision method for M-PPM scheme is illustrated in Figure 2.7. When the SFD symbol is detected, the next symbol will be the first data bit, in this stage, the

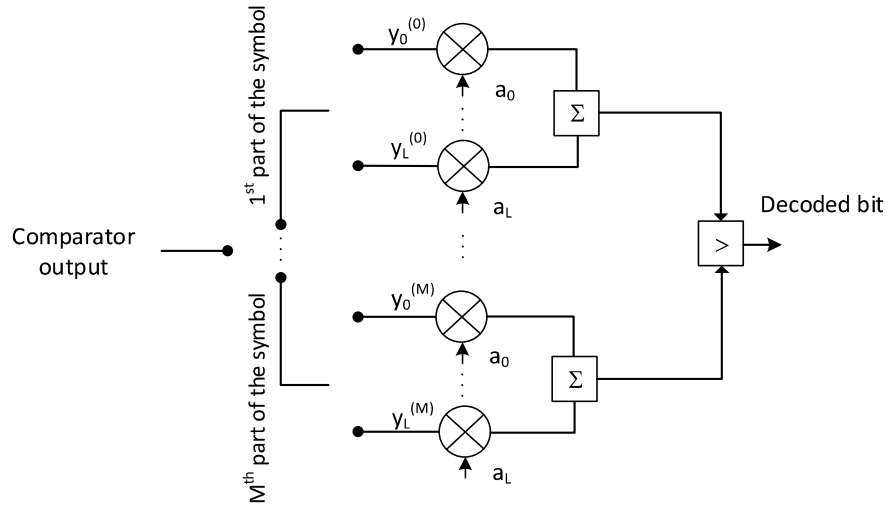


Figure 2.7 — Weighted multipath decision structure

received signal will be delivered to the demodulator input. The demodulator will also receive the CIR information from the SFD detector, *ie.* position of each detected path and its error probability. The main goal of the demodulator is to track the position of the transmitted pulse within the data symbol. In M-PPM modulation, the data symbol is divided in M parts, each part corresponds to a value of a data symbol ('0' or '1') called *PPM-symbol part*. The demodulator integrates the signal only where a path is expected for each PPM-symbol part. The resulting bits (RF-comparator output) are then weighted with a predefined coefficient, and combined linearly. The result of the combination for each part constitutes the decision variable. Ultimately, we end up with M decision variables, which can be described as follows:

$$y^i = \sum_{l=0}^{L-1} a_l y_l^i \tag{2.5}$$

where: i is the index of PPM part, i $\in \{0,...,M-1\}$, y^i is the decision variable of the i^{th} PPM-symbol part, L is the number of detected paths, a_l is the weight coefficient of the l_{th} path, and y_l is the local decision (RF-comparator output) of the l_{th} path, which is 1 when signal is detected, or 0 otherwise.

The comparison of the variables is formulated as follows:

$$y^i \underset{\mathrm{H_i}+1}{\overset{\mathrm{H_i}}{\gtrless}} y^{i+1} \tag{2.6}$$

$$\sum_{l=0}^{L} a_l y_l^i \underset{\mathrm{H_i}+1}{\overset{\mathrm{H_i}}{\gtrless}} \sum_{l=0}^{L-1} a_l y_l^{i+1} \tag{2.7}$$

$$\sum_{l=0}^{L} a_l y_l^i - \sum_{l=0}^{L-1} a_l y_l^{i+1} \underset{\mathrm{H_i}+1}{\overset{\mathrm{H_i}}{\gtrless}} 0 \tag{2.8}$$

$$\sum_{l=0}^{L} a_l (y_l^i - y_l^{i+1}) \underset{\mathrm{H_i}+1}{\overset{\mathrm{H_i}}{\gtrless}} 0 \tag{2.9}$$

where H_i is the hypothesis that pulse is transmitted in the i^{th} PPM-symbol part, $H_i + 1$ is the hypothesis that a pulse is transmitted in the $i + 1^{th}$ PPM-symbol part. The final decision is done once the pulse position within the symbol is found. For example, when the 2-PPM scheme is employed, if the score of the first part of the symbol duration is greater than the second one, the transmitted data symbol is supposed to be 0, else it is supposed to be 1 (Chapter 1, *cf* Table A.5).

The weighted coefficients a_l are based on the estimated error probability (P_{err}) during the SHR (thanks to the SFD detector). As explained in Section 2.3, the number of errors depend on SFD detection threshold. This threshold was set at 14, which means that our system can tolerate up to 14 errors in a window of 63 bits. The weight coefficient a_l varies from 2^n to 2^0, with n a parameter that can be adapted. Based on experimental results, it was dedided to use $n = 11$, meaning that 2^{11} is the weight of the best path (error = 0), and 2^0 is the weight for paths having more than 10 errors. This is an empirical choice, but this decision comes from observing that paths having more than 10 errors have negligible difference between them when taking a decision.

2.6 Algorithms performances

In order to evaluate the performance of the proposed algorithms, an efficient simulator is required. It has to model the real system in particular: (1) the channel models, which are important to take into account the radio propagation in a BAN environment, (2) the radio front-ends (transmitter and receiver) to have realistic signals, and (3) digital algorithms close to an implementable version to allow tests and facilitate specifications. The simulator has been developed in collaboration with CEA-LETI for the RUBY project. It is based on Matlab, with the following characteristics:

- Evaluating system performance in a realistic environment. More precisely, the performance of a PHY, radio-front-ends and digital base-band algorithms are thus jointly evaluated.
- Developing and testing digital base-band algorithms. The importance of this aspect will appear clearly in this study with the issue of ISI and the choice of timing parameter within the packet.

- Organization and testing the tasks repartition between the non-coherent front-end and the coherent one, when the dual architecture is applied.

The simulator operates at sampling frequency of 32 GHz, and integrates all blocks and specifications of the IR-UWB system, i.e: transmitter, IEEE 802.15.6 channel models, and the whole non-coherent receiver with its digital baseband algorithms.

2.6.1 Performances of synchronization and path selection estimation algorithms

The algorithms have been evaluated in different environments: an AWGN channel, a IEEE 802.15.6 CM3 channel model [113], which represents a body surface to body surface communication, and a IEEE 802.15.6 CM4 channel model [113], representing a communication between the body surface and an external device as mentioned in chapter 1.

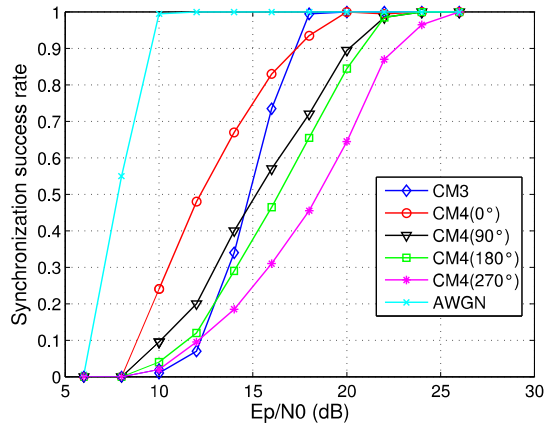
The different curves have been obtained for an average of 1000 channel realizations. For each channel model, the studied performance was the synchronization success rate, the number of detected paths, and the time required to acquire synchronization. Performance results are presented in Figure 2.8a.

Figure 2.8a illustrates the synchronization success rate of the proposed synchronization technique. As can be seen, the difference between all channels is not negligible. For the AWGN channel, the 99.9% synchronization success rate is obtained when pulse energy to noise ratio (Ep/N0) reaches 10 dB. This success rate is degraded, as can be expected, in the case of the IEEE 802.15.6 channel models. The main reason is the multipath effect introduced by the CM3/CM4 channel models which reduces the available energy in each single path, compared to the case of the AWGN channel.

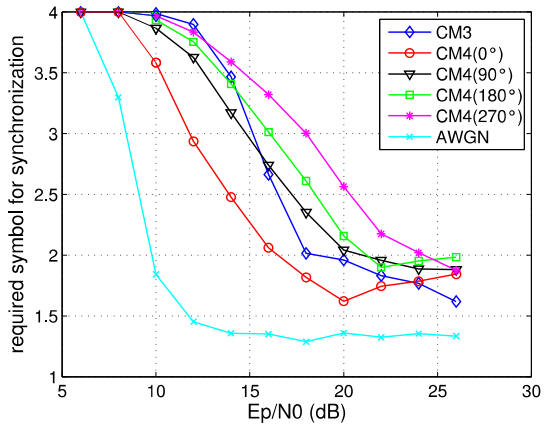
The worst cases correspond to CM4 channel model for angles other than 0°. CM4 (0°) is a LOS channel, with a strong main path. CM4 with angles other than 0°are either LOS or Non-LOS (NLOS) channels, depending on the position of the body. Similarly, CM3 may be either LOS or Non-LOS (NLOS), depending on whether a part of the body is located between devices or not. However, the distance between devices is higher in CM4 than in CM3: up to 5 meters in CM4 versus 2 meters in CM3. Thus, the spreading of paths over time is more important in CM4, which explains the reduced performances compared to CM3.

This analysis is confirmed by the results in terms of number of detected paths in CM3 and CM4, depicted in Figure 2.8c. In fact, about 18 paths are detected in CM3 when Ep/N0 reaches 26 dB, whereas the maximum number of detected paths in CM4 at the same Ep/N0 is about 8 paths. This confirms that the low delay spread of CM3 leads to more energy in the received paths (and thus more detectable paths) when compared to the case of CM4. Figure 2.8c illustrates also, as expected, how the number of identified paths increases with Ep/N0.

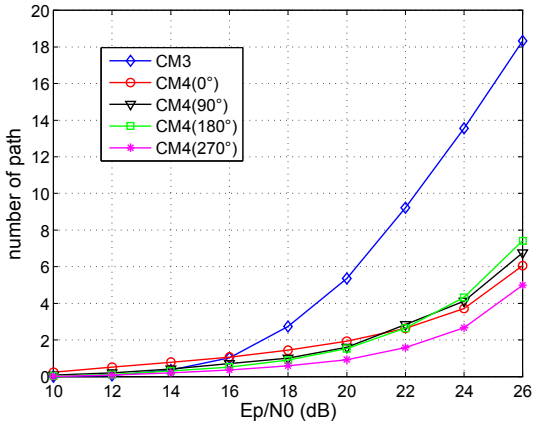
Another interesting result of the proposed synchronization technique concerns the number of symbols required to acquire synchronization. Figure 2.8b shows that less than 2 symbols are required to acquire synchronization at Ep/N0 corresponding to 99.9% success rate. This leaves enough time for further processing, such as ISI minimization or probabilities estimation, to improve the received signal quality. In this work, this time is exploited to estimate the bit error probability which constitutes the core of the demodulation algorithm.



(a) Synchronization success rate



(b) Time before synchronization



(c) Number of detected path

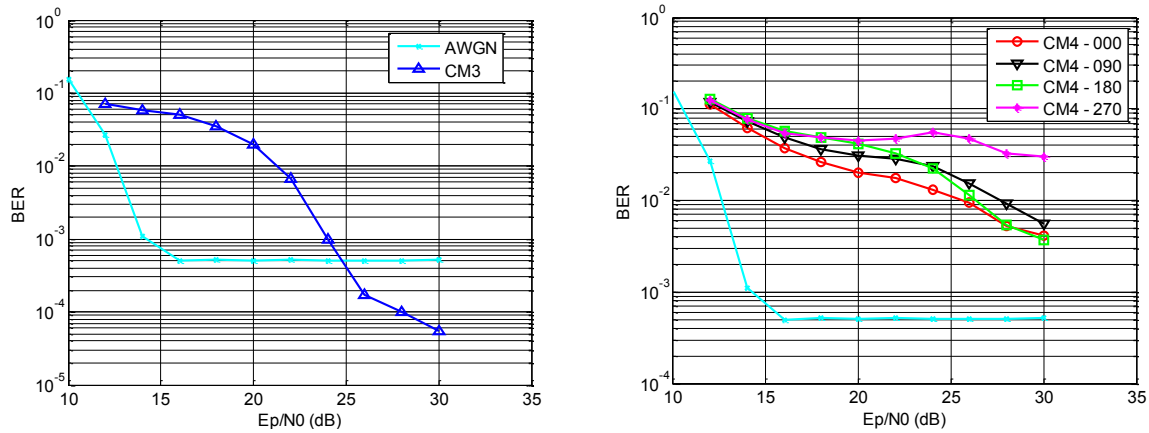
Figure 2.8 — Performance of the synchronization and path detection algorithms

2.6.2 Fusion decision performances

We evaluate in this sub-section the performance of the proposed Fusion decision algorithm. The evaluation was performed with a perfect synchronization (i.e. beginning of symbol and the position of each paths is known a-priori), in order to evaluate the algorithm performance independently of the synchronization technique. Nevertheless, the SFD algorithm is applied here to estimate the weight coefficients (during the SHR time), which are needed by the decision algorithm.

The algorithm was tested in the same environments of the synchronization one (AWGN, CM3 and CM4), and its performances are given in term of BER. The Figure 2.9 shows the performance in the different environments.

At first glance, we see that AWGN channel has an error floor at BER $\approx 10^{-3}$ when Ep/N0 reaches 16 dB, which is not the case for the CM3 and CM4 channel. In CM3, BER reaches the 10^{-4} at Ep/N0 $\approx$ 28 dB, whereas in CM4 angle other then 270° and 90°, it cross the 6x10^{-3} at the same Ep/N0. For CM4 90° and 270° angles, BER reaches respectively 6x10^{-3} and 3x10^{-2} at Ep/N0 = 30 dB.



(a) BER performance in AWGN and CM3

(b) BER performance in AWGN and CM4

Figure 2.9 — Performance of fusion decision algorithm in AWGN and BAN channel models with perfect synchronization

The error floor in AWGN is an expected result, and it is a consequence of the CFAR criteria. We have shown in section 1.4.3.1 that $P_{err\_sym} = 2P_{fa}.P_m + 1/2(P_{fa} + P_m)$, and that it will converge to $1/2.P_{fa}$ when the SNR is high enough. This can be noticed in the Figure 2.9.

A point worth noticing is that multipath detection mitigates the effect of the CFAR threshold. In other words, the error floor decreases when detecting several paths. When N paths are used to take a decision, each path is represented by a sub-symbol that has the same characteristics as the AWGN symbol. As a result, when dealing with multipath in CM3 and CM4 channels, an error can only occur when more than half the selected paths have an error. In general, the error can be expressed as follows:

$$P_{err\_sym-mpath} = P^{N}_{err\_sym} + P^{N-1}_{err\_sym} + ... + 1/2.P^{N/2}_{err\_sym} \tag{2.10}$$

Where $P_{err\_sym-mpath}$ is the symbol error probability in multipath channel, and P_{err_sym} is the symbol error probability in AWGN channel.

From the equation, and with $P_{fa} = 10^{-3}$, we can conclude that the $P_{err\_sym-mpath}$ depends largely of the last term of the equation ($1/2.P^{N/2}_{err\_sym}$). From above, we can conclude that when $N \to \infty$, $P_{err\_sym-mpath} \to 0$, and thus the error floor is mitigated.

The above analysis explains the CM3 results. Regarding the CM4 channel, the error floor is not present, but the CM4 performance are very degraded when compared to CM3. This unexpected degradation is caused by a strong ISI that occur during the payload. Channel delay spread is more than 32 ns, but with 2-PPM modulation, pulses can be separated by only 32 ns in the worst case (transmission of: 1;0), which causes a strong ISI basically damaging part of the data transmission (Figure 2.10).

This ISI is not taken into account during the synchronization, because pulses are separated by 64 ns in SHR. According to the performance results, this ISI impacts the CM4 channel more than the CM3 one. This makes sense, since the CM4 delay spread is longer compared to CM3, and also because, as stated before, the number of paths for CM4 is higher than for CM3.

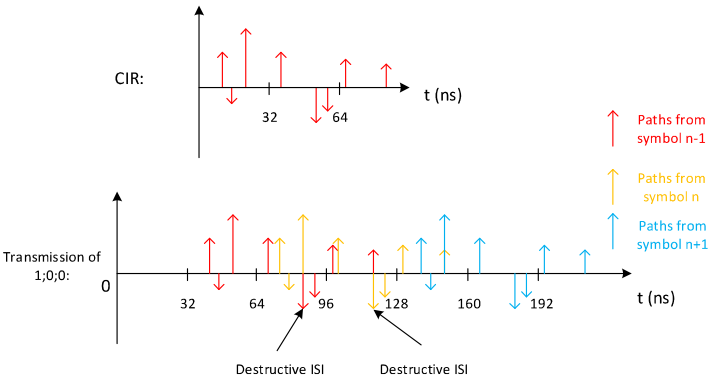


Figure 2.10 — Example of ISI with data transmitted (1;0;0)

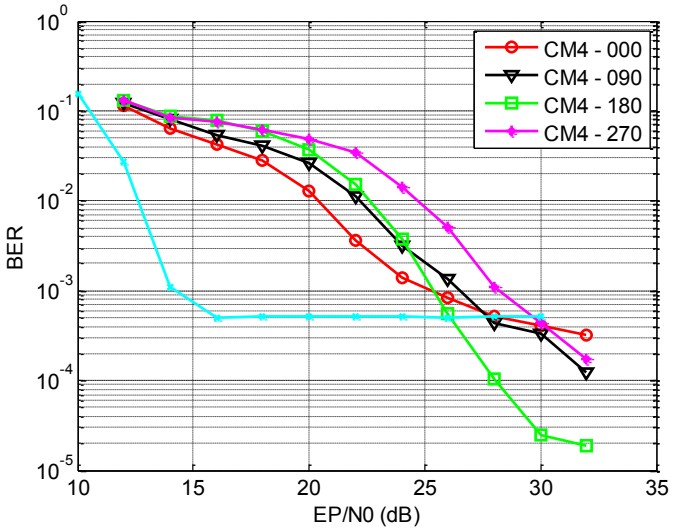


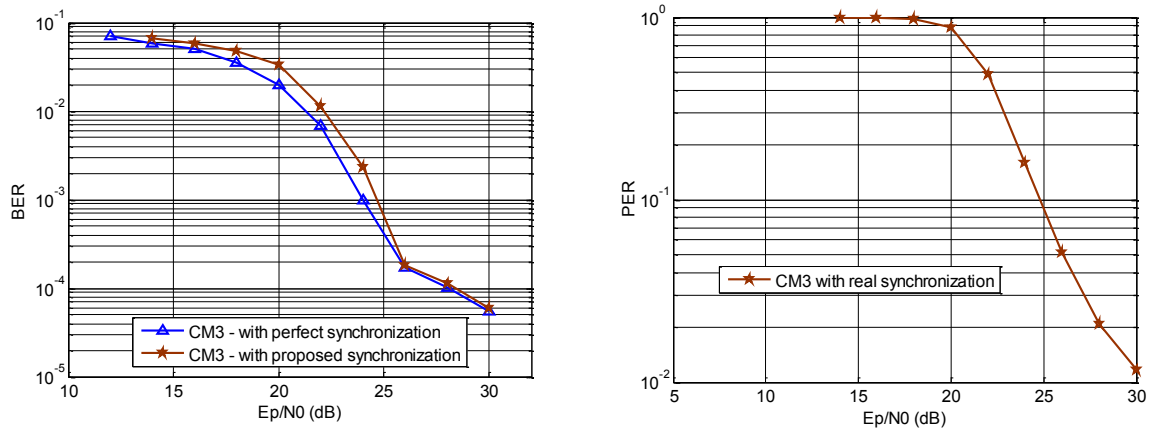
Figure 2.11 — BER performance of the CM4 channel model with $T_{sym} = 128ns$

In order to check the ISI effect, simulations are carried out with symbol duration (T_{sym}) of 128 ns instead of 64 ns in the previous case, and thereby, PPM pulses can be separated by 64 ns in the worst case (transmission of: 1;0).

The Figure 2.11 shows the obtained results. We clearly see a significant improvement for all the sub-cases of the CM4. A BER less then 10^{-3} is reached for all sub-cases, whereas in the previous case, the best attainable BER was more than $\approx 10^{-3}$. Moreover, a BER of 2.5x10^{-5} was reached by the CM4 $180°$ sub-case. These results confirm the impact of ISI in CM4 channel model. It also shows that given the constraints, $T_{sym} = 64ns$ is not the best parameter for the system when targeting the actual CM4 channel model. Since results with perfect synchronization are not satisfying, they will not improve when dealing with real, potentially faulty synchronization. From now on, we will not present reults for CM4. This is not to hide anything, it is only because given the T_{sym} value, results will never reach the required performance. The proposed solution is still interesting, at least for CM3, but would benefit from a longer T_{sym}, when lower data rates are targeted .

2.6.3 Performance of the proposed digital baseband

After evaluating separately the proposed reception algorithms, we evaluate now the performance of our proposed non-coherent digital baseband algorithms. Performance are presented in term of BER and Packet Error Rate (PER), and then validated taking into account the compatibility with the target applications. Figure 2.12 illustrates the BER and PER of the proposed non-coherent digital baseband.



(a) BER performance with perfect and real synchronization

(b) PER Performance with real synchronization

Figure 2.12 — Performance of non-coherent digital baseband in CM3 channel model

A BER of 10^{-4} is reached at Ep/N0 $\approx$ 28 dB. However, Figure 2.12 also illustrates that the proposed synchronization technique achieves BER performance which are very close to the ideal synchronization. The performance degradation compared to the ideal synchronization does not exceed $\approx$ 1 dB for all considered Ep/N0 values. This also leads to validation of the proposed synchronization technique.

Now, we have to check if the performances of the whole non-coherent digital baseband are compatible with the scenarios defined in the RUBY project (*cf* Chapter 1) and their technical requirements. Table 2.2 gives the link budget of the radio link under the PHY specifications.

From the table, we observe that Ep/N0 of 22 dB is available at the receiver. In the CM3 case, with a distance of 2m (worst case for an on-body link), the required Ep/N0 is $\approx$25 dB to reach a BER of 10^{-3}. This is not enough according to the requirements for the video streaming use case where a BER between 10^{-5} and 10^{-3} is required. But two things must be taken into account. First, a BCH(51,63) error correction code is used in the transmission. It can correct up to 2 errors for each codeword of length 51 bits, which allows correction of all errors for a BER below 4.10^{-2} in ideal conditions. The other element that we have to take into account is the non-uniformity of bits errors. Starting from the PER of 5x10^{-1} (see Figure 2.12), if we suppose a uniform repartition of bit errors, BER would be 2.4x10^{-4} (packet has 2048 bits). The remaining use cases (data sharing and control, Audio streaming) required a low data rate (respectively $\leq$ 1 Mbps ,$\leq$ 512 kbps), so 10 dB of sensitivity improvement could be retrieved by lowering the data rate. Thus, the use cases technical requirement defined in the RUBY project (presented in the previous chapter) can be met.

Parameter	Value	Unit
Power spectral density	-41.3	dBm/Mhz
Bandwidth	1800	MHz
Maximum Tx Power	-8.7	dBm
Data rate (R_b)	15.6	Mb/s
distance	2	m
Path Loss	66.7	dB
Rx Power (P_{rx})	-75.4	dBm
Rx Noise figure (N_f)	5	dB
Average noise power per bit: ($N = -174 + 10log10(R_b)$)	-102	dBm
Available Ep/N0 (Ep/N0 = $P_{rx} - (N_f + N)$)	22	dB

Table 2.2 — Radio budget link

2.7 Summary

This chapter has presented the PhD thesis contributions related to the proposal of non-coherent IR-UWB baseband algorithms for BAN applications and to the evaluation of their simulation performances. The proposed algorithms are compliant with IEEE 802.15.6 standard and target the requirements of RUBY project.

The synchronization algorithm is based on a dedicated finite state machine, which detects the sequence of time intervals between pulses and compares it to the synchronization symbol based on a Kasami sequence. The algorithm has been adapted to accommodate for possible transmission errors, and can be parameterized to support any synchronization symbol. A correlation method for SFD detection was also proposed. It especially allows to minimize conjointly the false synchronization and the missed SFD detection. The good resolution (1 ns) offered by the adopted non-coherent receiver was exploited to design a parallel architecture in order to detect the different resolvable paths available in the IR-UWB signal, thus benefiting from the multipath propagation phenomena instead of only suffering from it. A channel estimation architecture was also proposed. The decision fusion algorithm relies on a weighted multipath processing method targeting the PPM modulation.

With these algorithms, the receiver is able to meet the requirements of the hybrid coherent/non-coherent receiver architecture targeted by the RUBY project. In addition, if the sensitivity of the non-coherent front-end is sufficient for the target application, the receiver allows to fully process the received signal in a non-coherent manner, thus reducing the need for a complex and costly coherent front-end.

The simulation results presented in this chapter show the efficiency of the proposed techniques. Synchronization performances show success rates with different Ep/N0 values depending on the channel model and its nature (LOS or NLOS). The algorithm also allows a short synchronization time. Less than 2 symbols are required to reach 99.9% synchronization rate. Moreover, the proposed algorithm can deal with any IEEE 802.15.6 sequence (preamble symbol) and can be extended to other sequences.

The decision fusion algorithm performance is presented in term of BER. The algorithm takes

advantage of multipath processing, and the performance improvement has been demonstrated in the results. Error floor was mitigated when using more than one path to take a decision. Two main results are observed depending on the channel model. In CM3 channel model, good BERs are obtained. BER of 10^{-4} was reached at Ep/N0 $\approx$ 28dB. Results were not as good in CM4 channel. This channel is very aggressive, and very strong ISI are introduced due to the selected symbol time in the standard. The digital baseband performances are provided in terms of BER and PER in CM3 channel model. Considering the specified use cases of the RUBY project, the proposed solution is sufficient to meet the target data rate and sensitivity requirements.

CHAPTER

3 Digital baseband architectures and FPGA implementation

THIS chapter presents the PhD thesis contributions related to the hardware design of a low-complexity digital baseband for non-coherent IR-UWB receiver. It regroups the different proposed low-complexity architectures that implement the algorithms presented in the previous chapter for synchronization, SFD detection, path selection and demodulation.

The chapter starts by providing an overview of the target digital baseband transceiver and the related interfaces with the radio frequency front-end and the application board. Then for each proposed architecture a detailed description is provided. This includes the defined input/output signals, the main constituent components, and the control unit as a finite state-machine that schedules the different operations of the proposed architecture.

In addition, in order to have a complete functional digital baseband receiver, a serial-to-parallel converter is designed to handle the high speed input data stream, together with a global control unit for operation scheduling. The proposed complete digital baseband has been implemented targeting a Xilinx Spartan 6 FPGA. In addition to the behavioral and post-synthesis simulations, on-board validation was performed. The obtained results in terms of required logic resources illustrate the hardware efficiency of the proposed architectures and constitute a reference in this domain where the available literature is rather scarce.

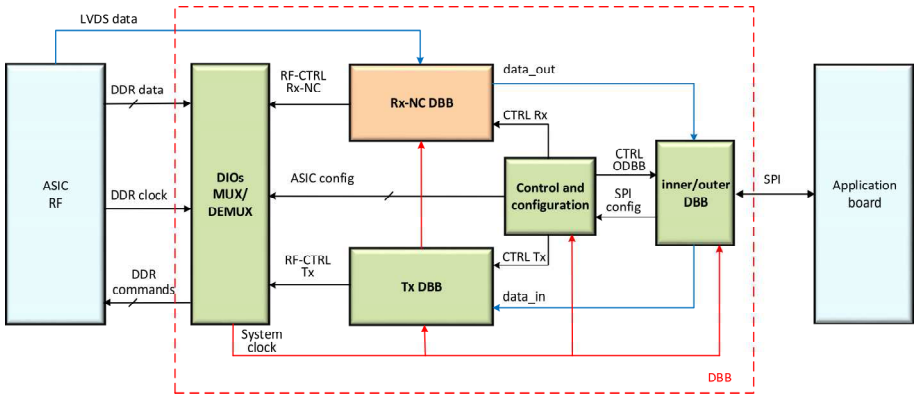


Figure 3.1 — Overall representation of the digital baseband (DBB) transceiver

3.1 Overview of the digital baseband transceiver

The overall representation of the target digital baseband (DBB) transceiver and its interfaces with the radio frequency (RF) front-end and an application board is depicted in Figure 3.1. In the context of the RUBY project [90], the RF front-end is designed as a single ASIC chip that implements an IR-UWB transmitter and combines coherent and non-coherent reception architectures. The application board is built mainly around a microcontroller (connected to a host computer for control and monitoring during the prototyping phase). More details about the complete platform are provided in the next chapter which presents hardware prototyping and on-board demonstration.

The digital baseband processing, which is the focus of this PhD work, is done to process the baseband signal in non coherent manner and is composed of five main blocks. Each block is responsible for a specific part of the overall processing chain.

The *Rx-NC DBB* block implements the digital baseband processing of the non-coherent receiver. It integrates the main contributions of this PhD work regarding synchronization, path selection, SFD detection, and symbol decision. The proposed architectures for these functions are detailed in the subsequent sections of this chapter.

The *Tx DBB* block implements the baseband transmitter. When the digital baseband is in transmission mode, it receives data from the *inner DBB* block. It then builds the outgoing frame which consists of the payload (PSDU) and the different headers of synchronization and physical layer (SHR, PHR).

The *inner and outer DBB* implements mainly the channel coding and decoding, in addition to (de)scrambling and (de)interleaving functions. Several forward error correction schemes (several BCH encoder types) are specified in the IEEE 802.15.6 standard to improve the communication performance in terms of BER. The design and the implementation of this block have been done through an engineering internship supervised by this PhD thesis. Details on the proposed and developed architecture can be found in [114]. In addition to this main function, the block integrates a serial communication controller based on the SPI (Serial Peripheral Interface) protocol. This controller allows to implement the main interface for data exchange with the application board.

The *control and configuration* block is designed to manage the processing chain configu-

ration and control. It manages the RF front-end configuration *via DIOs MUX/DMUX* block, according to commands from the application board. It also manages communication between the different digital baseband blocks.

Finally, the *DIOs MUX/DMUX* block manages the communication between the digital baseband and the RF fron-end in Double Data Rate (DDR) mode. This DDR mode allows data transfers on both the rising and falling edges of the clock signal to interface with a memory device. The memory device in this context is a set of registers which are located both in the RF front-end and the digital baseband. The RF front-end registers are dedicated to receive the RF configuration and control signals from the digital baseband, as the LNA gain, detection threshold, transceiver configuration mode (Tx or Rx), etc. As this RF front-end combines coherent and non-coherent receivers, two different interfaces are implemented. For the coherent front-end, the outputs of the analog-to-digital converters are conveyed to the digital board in DDR mode using a 62.5 MHz clock. For the non-coherent front-end, the outputs of a threshold comparator are conveyed through multiplexed low-voltage differential signaling (LVDS) at 1 GHz frequency. For all digital baseband processing blocks, a clock signal *Ep* of 62.5 MHz provided by the RF front-end is used as reference for the performed operations.

3.2 Proposed digital baseband architectures for non-coherent IR-UWB receiver

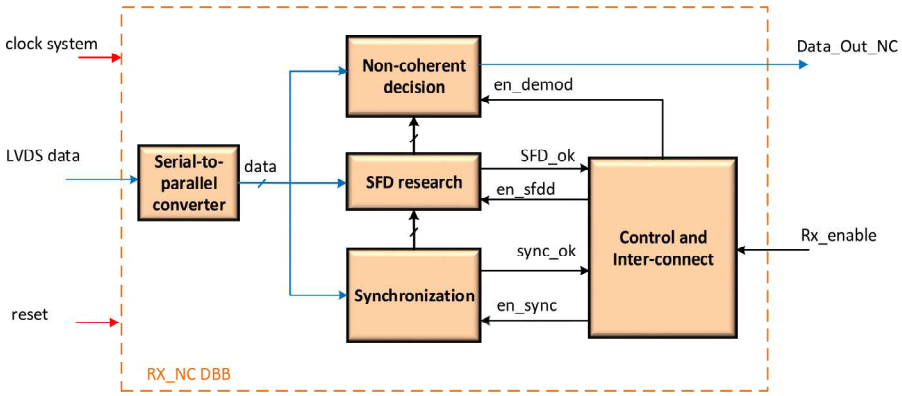


Figure 3.2 — Overview of the proposed non-coherent IR-UWB receiver architecture

The overall proposed architecture for the *Rx-NC DBB* is shown in Figure 3.2. It is composed of four main modules that process the received data from the RF front-end. First, the data must be deserialized. In fact, the interface between the RF front-end (analog) and the digital baseband is a fast LVDS link at 1 GHz, which is too high for FPGA processing. The Serial-to-Parallel converter block processes this serial data, and outputs parallel data at a much slower rate. Once the received data rate is slowed down, the synchronization module is used to acquire synchronization, and to track the multiple paths resulting from the propagation phenomena. This is performed by trying to match the received data with the expected preamble.

When a preamble has been detected and synchronized on, the SFD module is then used to detect the SFD symbol that tags the end of the preamble and the start of the payload data. The payload is sent then to the non-coherent decision module for demodulation. This module

implements a multipath processing demodulation algorithm. All these operations are controlled using a specific control module as illustrated in Figure 3.2.

While proposed non-coherent reception techniques for these four modules were presented in the previous chapter, the next sub-sections will present the proposed low complexity architectures that implement these techniques.

3.2.1 Synchronization architecture

3.2.1.1 Synchronization module overview

Figure 3.3 provides a general overview of the proposed architecture to implement the synchronization algorithm described in Chapter 2. The input/output signals of this module are summarized in Table 3.1. The proposed architecture integrates the following main components: *distance_counter*, *noise_counter*, *FSM* and *register_memory*. As for the proposed synchronization algorithm presented in the previous section, the proposed architecture is built around an original FSM design that checks the correlation between the received symbol and the expected one, and allows to count the distance between two consecutive received pulses.

Name	Input/Output	Signal width	Description
reset	I	1	asynchronous reset
clk	I	1	system clock
data_enable	I	1	indicates the validity of the input data
en_sync	I	1	enables the synchronization search task
data	I	1	input data
sync_ok	O	1	indicates that the synchronization is acquired
last_pulse	O	5	indicates the position of the last detected pulse

Table 3.1 — Input/output signals of the *synchronization* module

The components *distance_counter* and *noise_counter* are simple counters. The first one, (*distance_counter*), is used to compute the distances between the received pulses, whereas the second one, (*noise_counter*), computes the number of spurious pulses when encountered. The *FSM* component checks the different distances delivered by the *distance_counter* as described in Section 2.2, and the *register_memory* component is used to check the identified pulses.

When the control part of the receiver detects an activity in the channel , it activates the *en_sync* signal to trigger the synchronization acquisition process. Once *en_sync* is activated, the *synchronization* module starts taking into account the pulse detected from the RF front-end (output of the threshold comparator) through the *data* signal.

When no pulse is detected (*data* = 0), *distance_counter* is incremented. Once a pulse is received (*data* = 1), the FSM reads the *distance_counter* value which represents the distance between two consecutive pulse detections. At this state, if the distance corresponds to one of the expected distances (according to the synchronization sequence), the FSM changes its state and resets the *distance_counter* by activating the *clear* signal. As a result, one pulse has been detected and the distance computation with the next pulse is started. If the distance does not correspond to the expected one, the detected pulse is considered as a noise, and the *FSM* increments the *noise_counter* in order to verify the tolerated spurious pulses. If the tolerated

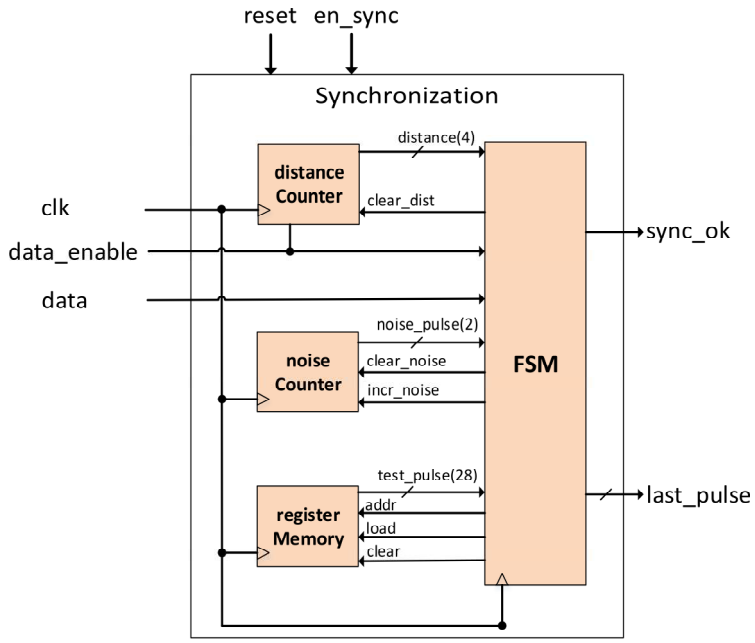


Figure 3.3 — Proposed architecture for the synchronization module

spurious pulses number is not exceeded, the above process continues until the identification of an expected distance. If it is not the case, the process is restarted.

When a pulse j is identified, the register j of the *register_memory* component changes its value to 1, indicating that the j^{th} pulse was identified. The process described above is repeated until all the pulses are identified (*register_memory* is full of 1). Once this happens, the FSM converges to the final state, activates the *Sync_ok* signal to indicate that synchronization is acquired, and provides the position of the last detected pulse through the *last_pulse* signal. This *last_pulse* signal is used to indicate the position of the current pulse, based on received distances. This position is given in binary coded decimal form.

3.2.1.2 Synchronization FSM

Figure 3.4 provides a simplified view of the implemented synchronization finite state machine.

The FSM architecture is designed with 4 different types of states, in addition to an initial state:

- ***state 0***: This is the initial state, where all variables of the state machine are reset. When the computed distance matches one of the expected distances, the next state has two possible states: *I_state j* or *state j*.
- ***I_state j***: This is the j^{th} intermediate state, it corresponds to the case when the computed distance matches more than one expected distance (repetitive distances, cf. 2.2). The number of states of this type depends on the considered synchronization sequence. The goal of these states is to find the position of the pulse within the sequence. The next state has three possible states: *I_state j+1*, *state j*, *I_noise j*. The first possibility (*I_state j+1*) occurs when

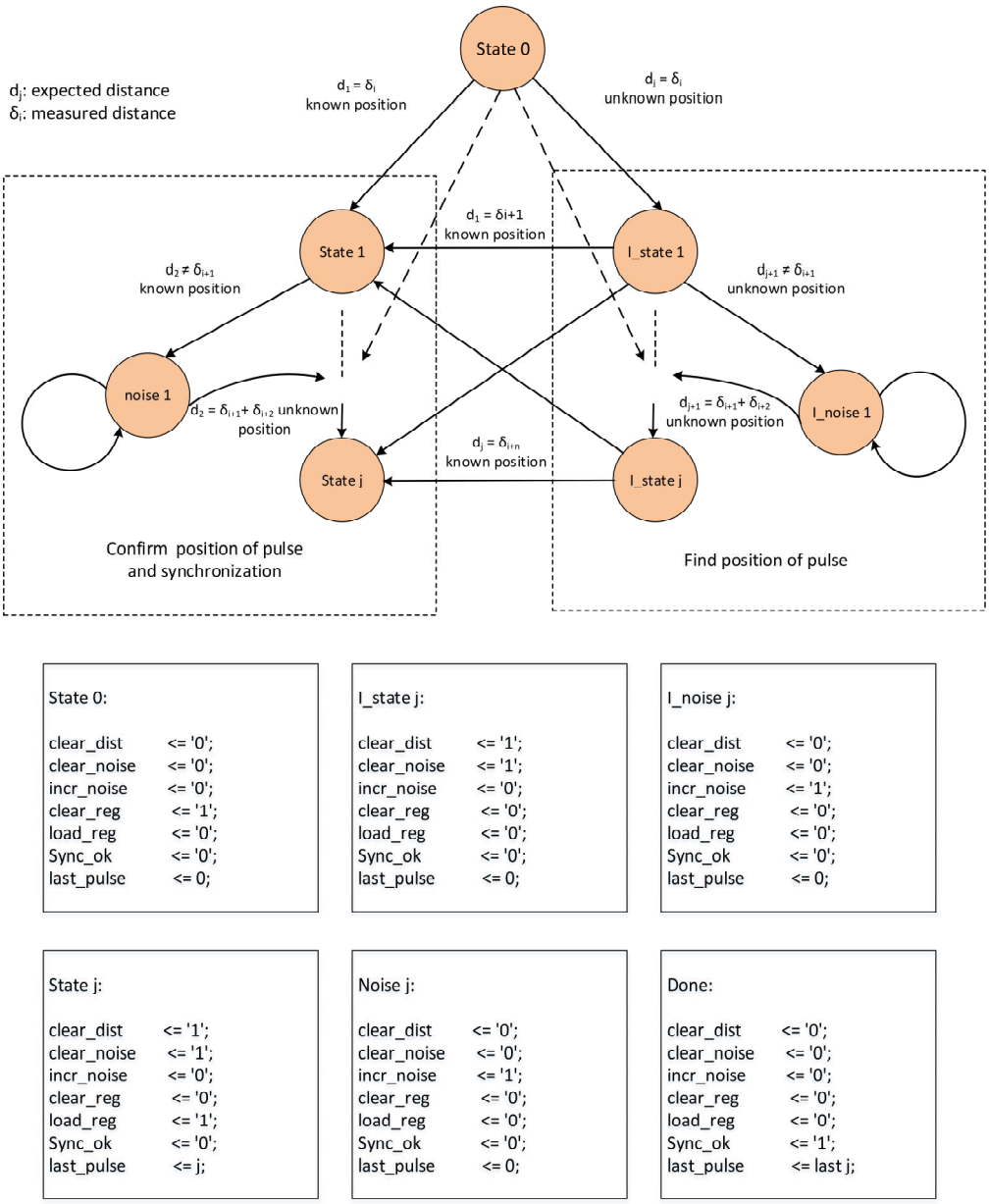


Figure 3.4 — Simplified view of the synchronization finite state machine

the next distance matches the expected one, but no decision can be taken on the position of the current pulse because we are still in the case of a repetitive distance. The second possibility (*state j*) occurs when the next distance matches the expected one, and the position of the pulse is found (j^{th} position). In this case, we leave the intermediate states, since we can now determine precisely the position of the received stream in the expected sequence. The last possibility (*I_noise j*) occurs when the distance does not match any expected distance.

- ***I_noise j***: This type of states are used to handle the spurious pulses occurred due to noise in the transmission. The last identified pulse is considered as a spurious pulse. The noise counter is incremented (*incr_noise* = 1). The current distance is not cleared, and the search task continues. The next state will then be decided based on the distance between the previous pulse and the next one (the current one is discarded). If this distance matches an expected one, we select the next state according to this detection. Otherwise, the process

is repeated until reaching the threshold of tolerated spurious pulses. When this limit is reached without acquiring the synchronization, the execution goes back to the initial state.

- ***state j***: This state represents the case where the position of the current pulse is found within the sequence. In such state, register j is set to 1 (*load_reg* = 1), and *last_pulse* signal takes the value j. The number of these states is equal to the number of pulses (N_{pulses}) in the sequence. In general, the next state should be *state j+1* when next pulse occurs. However, the FSM allows a transition to a state *noise j* if a spurious pulse occurs, or *state j+2* in the case of a missed pulse. If the FSM proceeds correctly after such transition, then we assume that there was an erasure in the input stream. Otherwise, it was a mistake (the already identified pulses were erroneous), the FSM will not converge (no synchronization will be acquired), and the process must be restarted in such case.

- ***noise j***: This is the same kind of states as *I_noise j*, except that the position of the pulse is known (no ambiguity in the received distances). The next state should be either *state j* or *state j+2*.

3.2.2 SFD detector architecture

3.2.2.1 SFD detector overview

The SFD detector module is in charge of three tasks: (1) finding the position of the first data bit in the received frame, (2) validating the acquired synchronization, and (3) computing the number of errors over a period of time (used later to estimate the detection probability). The input/output signals of this module are summarized in Table 3.2.

Name	Input/Output	Signal width	Description
reset	I	1	asynchronous reset
clk	I	1	system clock
data_enable	I	1	indicates the validity of the input data
en_sfd	I	1	enables the SFD search task
data	I	1	input data
sync_ok	I	1	indicates that the synchronization is acquired
last_pulse	I	5	indicates the position of the last detected pulse
sfd_ok	O	1	indicates that the SFD is detected
Nb_err	O	6	indicates the mean number of errors in a Kasami period

Table 3.2 — Input/output signals of the *SFD detector* module

The proposed architecture for this module is presented in Figure 3.5. When the synchronization is acquired by the receiver, the control module triggers the *SFD detector* module (Figure 3.5) by activating the *en_sfd* signal.

When the *SFD detector* module is activated, the *FSM* triggers the *time_counter* component, which is a simple counter. The *elaps_time* value starts incrementing. At the same time, the symbol boundary shift (*next_symb*) is deducted thanks to a simple *LUT* component and to the position of the current pulse (*last_pulse*). The symbol boundary shift is the time between the position of the last detected pulse (within the SHR symbol) and the SHR symbol boundary. It indicates the time delay to get the beginning of the next SHR symbol. If this time is miscalculated, the synchronization will be wrong and therefore the packet will be lost.

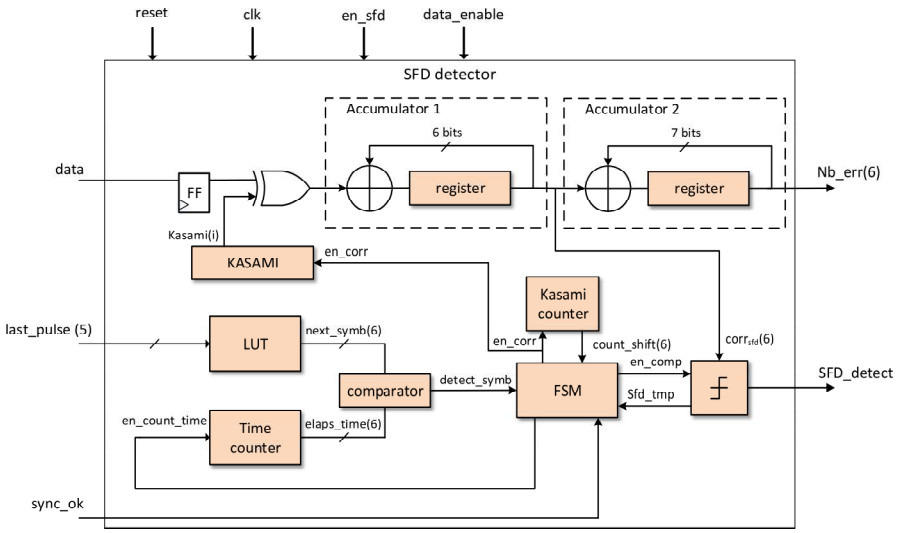


Figure 3.5 — Architecture of the SFD detector module

Once the *time_counter* value matches the symbol boundary shift, the *detect_symb* signal indicates to the *FSM* that the next bit belongs to the new SHR symbol. At this time, the *FSM* enables the correlation between the incoming bits and the pre-defined Kasami sequence. This correlation is performed using a *XOR* operator and an accumulator during a Kasami period (using the *kasami_counter*). The result is then compared to a pre-defined threshold (cf. 2.3) to decide if the SFD is detected or not. This operation is performed in iterative way until the SFD is detected or the allowed search time is over.

Due to the simple correlation scheme used, the result represents directly the number of errors in the stream during a Kasami period. In order to estimate the mean number of errors, which is needed to estimate the bit detection probability, 2 successive correlation results are taken into account. This number of required results is dictated by hardware implementation considerations. In order to compute the mean value, a division operation is required. Such operation is very costly in terms of hardware resources if the divisor is not a power of 2. Finally, the mean number of errors is delivered through the *Nb_err* signal in binary coded decimal form.

3.2.2.2 SFD detector FSM

The control part of the above described architecture is implemented by a simple finite state machine depicted in Figure 3.6.

The different states of this FSM are described below:

- ***Init***: this is the initial state, all variables of the state machine are reset. As soon as the module is activated, the next state will be *bound_detect*.
- ***bound_detect***: this state is used to detect the beginning of the symbol. When this happens (*detect_symb* = 1), the next state will be *shift* state.
- ***shift***: in this state the shift of the input data is enabled (*shift_en* = '1'). The FSM stays in this state as long as *sfd_tmp* is not equal to 1. When *sfd_tmp* = 1, the next state will be the *done* state. However, if *en_sfd* = 0 the FSM goes back to the *Init* state.

- ***done***: this state indicates that the SFD is detected by activating the *SFD_ok* signal.

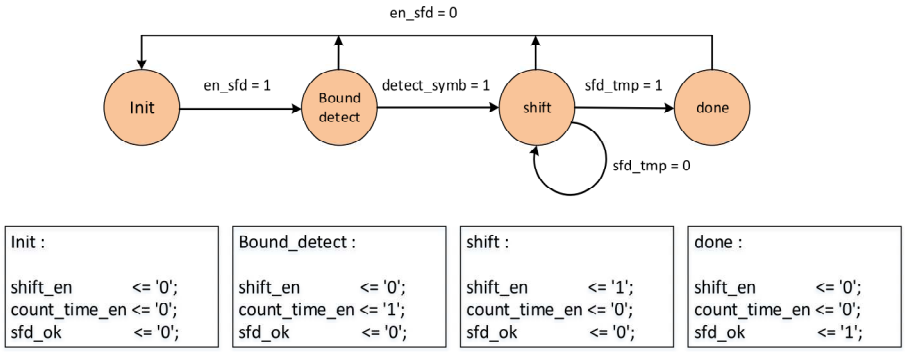


Figure 3.6 — SFD finite state machine

3.2.3 Parallel approach: path selection estimator architecture

The previously presented modules can be used to process a single path. However, over a real channel, UWB signal almost still require a multipath processing. Therefore, channel estimation is needed to allow efficient multipath processing. This is possible thanks to the adopted non-coherent receiver that provides a fast sampling (1 GHz) of the received signal.

A parallel architecture is proposed here to implement the path selection technique described in Chapter 2 - Section 2.4. In this case, the synchronization module and SFD detector presented before can be used to estimate a single path, and these modules can then be duplicated in order to process multiple paths simultaneously. Each instantiation of these modules is called a *branch*, and is responsible for processing one path in the incoming stream.

A first *direct* implementation of the *path_selector* module would be a simple concatenation of branches, enough for all possible paths. In the system requirements considered in this work, such implementation would mean LT_w parallel branches, i.e. 64 in our case. Theses branches would then be used to detect the 64 possible paths. In addition, in order to design such fully parallel architecture, a serial-to-parallel converter at the input which is able to deliver parallel data of width LT_w is needed.

Although such an implementation can be direct and conceptually simple, in practice it is not quite feasible as it requires much hardware resources, especially when LT_w becomes high.

In order to reduce the hardware resource usage, specific optimizations are required. The proposed idea is to reduce the parallelism degree of the *path_selector*, i.e to switch from a fully parallel architecture to a partially parallel one. This transition to a partially parallel architecture would be beneficial in terms of reduction of area and logic resources, especially when targeting low complexity devices. Decreasing the parallelism level is possible since the aim of the synchronization module is not to process the received data as fast as possible. In fact, it should only be able to support the rate of the incoming data.

In this context, if the digital baseband processing can run at a higher clock frequency than the incoming data rate, this means that several clock cycles are available to process each data symbol. Therefore, these clock cycles can be used to process several paths sequentially in a

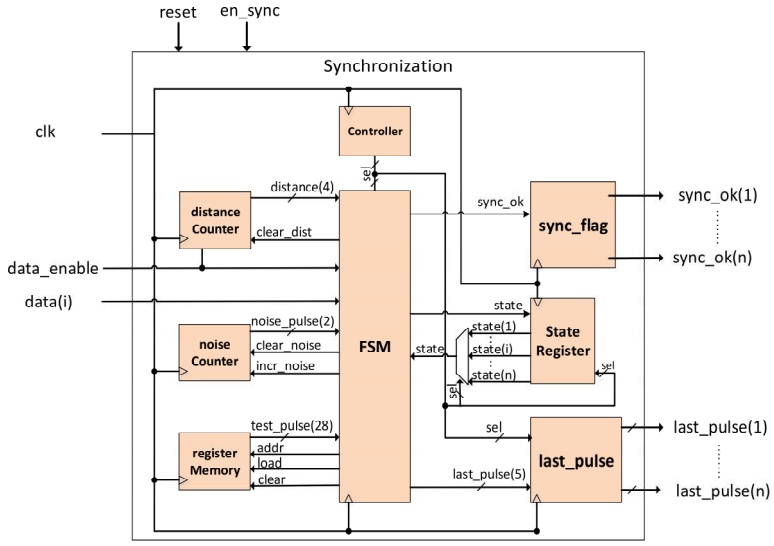


Figure 3.7 — Partially-parallel architecture for the synchronization module

single branch, resulting in a lower required number of branches, i.e lower hardware resources than the fully parallel architecture.

In this case, the number of paths processed by one synchronization module depends on the number of parallel branches. For example, if we reduce the number of parallel branches by two, i.e. $LT_w/2$ branches, each *synchronization* module must process sequentially 2 paths to cover the LT_w paths. In general, the *synchronization* module must process sequentially n paths when the number of parallel branches is reduced by a factor of n.

However, this approach implies to modify the architecture of the synchronization module in order to be able to process multiple paths. Regarding the SFD detector, a fully-parallel architecture is envisaged due to the very low-complexity of this module. Figure 3.7 illustrates the new partially-parallel architecture for the synchronization module. It integrates new components compared to the initial architecture (Figure 3.3), namely: *controller*, *state_register*, *sync_flags*, and *last_pulse*. The *state_register* component is used to store the current state of the n_{th} processed path. The *controller* component consists of a simple $log_2(n)$ bits counter. It is used to indicate which path is currently processed among the n paths. Finally, the *sync_flags* and *last_pulse* components are used to register and to output the synchronization results (*sync_ok* and *last_pulse* signals).

The *synchronization* module starts to process the 1^{st} path during one clock cycle: depending on the input data the FSM changes or not its state. This state is then stored in the *state_register* as the current state of the 1^{st} path. The same operation is performed with the remaining $n-1$ paths. Once finished, the FSM retrieves the saved state of the 1^{st} path and continues to process this path based on the saved state and the current input data. The resulting state is once again saved in the *state_register*, and the module processes the next paths. This modulo n loop is run in all the N_{branch} *synchronization* modules, and the order of the paths is known and controlled using the *controller* component.

Name	Input/Output	Signal width	Description
reset	I	1	asynchronous reset
clk	I	1	system clock
data_enable	I	1	indicates the validity of the input data
en_demod	I	1	enables the demodulation task
data	I	64	input data
SFD_table	I	LT_w	provides the multipath detection result
index	I	6	indicates the position of the first detected path
NB_err_table	I	6* LT_w	provides mean number of errors of the detected paths
bit	O	1	demodulated bit
valid_data	O	1	indicates the validity of the output demodulated bit

Table 3.3 — Input/output signals of the *Decision* module

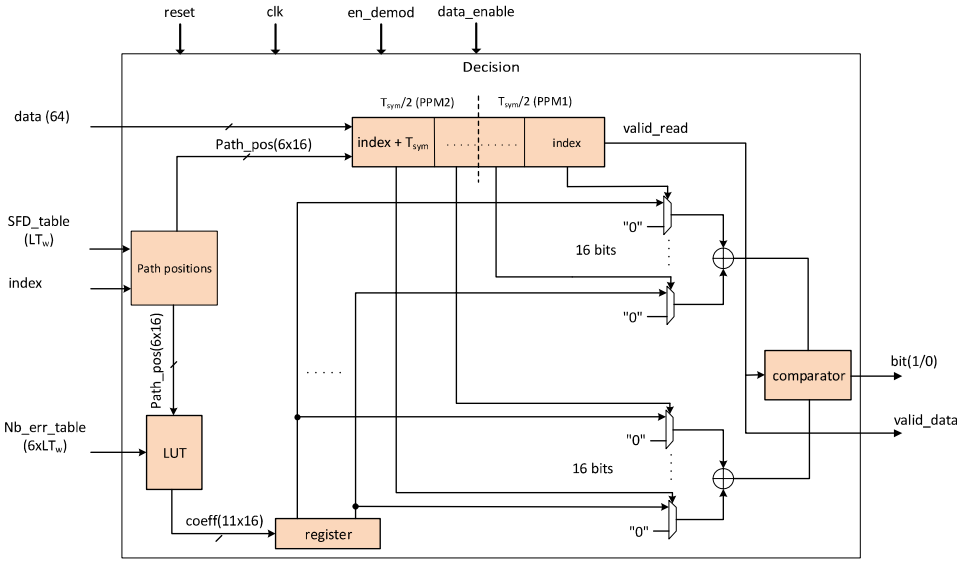


Figure 3.8 — Proposed architecture for the *decision* module

3.2.4 Decision architecture

The *Decision* module performs the data demodulation. Its role is to decide whether a received symbol represents a 1 or a 0. The proposed architecture for this module is presented in Figure 3.8, and its input/output signals are depicted in Table 3.3

When the SFD is detected, the demodulation is triggered by activating the *en_demod* signal. The *decision* module reads the path list provided by the *path_selector* module through the *SFD_table* signal. This information is given using a bit vector of size 64 (LT_w = 64 ns), with each bit representing the state of a path (i.e. 0 = no path, 1= path detected). The *path_position* component sorts then the position of the identified paths based on the *index* signal. This latter provides the position of the first detected path (in the range 0 to 63) within the *SFD_table*. This is due to the fact that the first detected path is not necessarily the first appeared '1' in the *sync_table* vector ranging from 0 to 63. In fact, the channel delay can create a shift when acquiring and parallelizing data.

In order to illustrate how this works, we use the following example for which LT_w has a value of 64. Assuming the MSB = 63 and the LSB = 0, i.e. the first acquired bit by the receiver

will be at position 0 and the last one at position 63. If the actual frame is the n^{th} frame, and the processed *index* is 30, this means that the data from position 0 to 29 belongs to the $(n-1)^{th}$ frame, and only the data from 30 to 64 belongs to the n^{th} frame. In other words, the data is shifted by 30, and the processing window is not aligned with the frame.

At the next frame $(n+1)$, we find the remaining 30 bits of the n^{th} frame at the position indexes 0 to 29. This shift is created by the serial-to-parallel data. It prevents proper synchronization and requires to take into account this shift in order to get correct results.

In parallel, the weighted coefficients of each path are deducted (using the *LUT* component) based on the estimated errors (*Nb_err*) during the SFD search. In fact, the weight coefficients vary from 2^{11} to 2^0, meaning that 2^{11} is the weight of the best path (error = 0), and 2^0 is the weight for paths having more than 10 errors (see Chapter 2 - Section 2.5).

The last remaining step is the decision process. Data registered in *shift_register* is combined according to the computed coefficients (*coeff*) and compared to estimate the received bit value. It takes 4 clock cycles to estimate a bit value, a validity flag (*valid_data*) is generated as an output of the *decision* module to indicate when the bit value is valid.

3.2.5 Serial-to-parallel converter

As mentioned in Section 3.2 above, the data is provided by the RF front-end to the non-coherent digital baseband through a fast LVDS link at 1 GHz. The serial-to-parallel converter is the first block that receives the RF front-end signal in the digital baseband side. This latter receives also the *Ep* clock at 62.5 MHz from the analog front end through the DDR interface (cf. Section 3.2). In fact, all the above described modules of the digital baseband are derived by this clock signal.

Name	Input/Output	Signal width	Description
reset	I	1	asynchronous reset
clk	I	1	system clock
rx_enable	I	1	enables the reception process
RF_data	I	1	RF data received from the RF threshold comparator
data	O	4,8,16,...	digital data
data_enable	O	1	indicates the validity of the output digital data

Table 3.4 — Input/output signals of the *deserializer* module

The proposed architecture of the serial-to-parallel converter or *deserializer* module is divided in two main parts as illustrated in Figure 3.9:

- Clock management part: represented by the *clock_generator* component in Figure 3.9. It is designed to provide proper clocks to the different parts of the system.
- Parallelization part: represented by the components *ISERDES* and *shift_register* and used to transform the serial input data into an output parallel stream.

This converter is technology dependant since it requires to manage high frequency communication. In order to further describe this module, a target specific implementation for Xilinx FPGAs is proposed here. The input/output signals of this module are given in Table 3.4. The

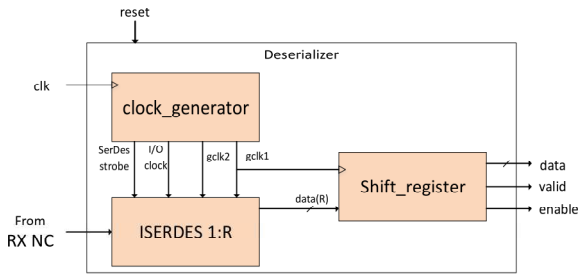


Figure 3.9 — Proposed architecture fir the *deserializer* module

selected target is a Xilinx Spartan-6 FPGA. The *clock_generator* component is based on one of the FPGA Digital Clock Manager (DCM) units.

Xilinx Spartan-6 devices contain input SerDes (ISERDES) and output SerDes (OSERDES) blocks that simplify the design of serializing and deserializing circuits for high operational speeds. T The ISERDES block is used in the proposed architecture. It implements SERDES ratios of 1:2, 1:3, and 1:4, where the SERDES ratio is defined as the ratio between the high speed I/O clock that is capturing data, and the slower internal global clock used for outputting the parallel data [115]. However, the SERDES ratio can be extended to 1:8 with cascaded ISERDES [116].

The *clock_generator* component uses the *Ep* clock as input of its internal Phase-Locked Loop (PLL) to generate a clock for the *ISERDES* component with a frequency matching the input data rate (1 GHz). Represented by I/O clock in Figure 3.9, this high speed clock is then used to sample the received serial data on the input of *ISERDES* component. In the adopted non-coherent receiver, the data is sent from the analog front-end to the digital part through an LVDS link, with no clock signal. This prevents the possibility to synchronize on an input clock signal. However, since the data rate is known, and the aim is to sample the input data at each clock cycle, we use the ISERDES component as an analog-to-digital converter. The output of the threshold comparator in the RF front-end is sent directly as data signal, and the I/O clock can be seen as a sampling clock. The I/O clock frequency is set to match the data rate in order not to oversample or subsample the signal. As this clock signal is used as a sampling clock, a timing shift up to the pulse width (1 ns) is tolerated. Furthermore, acquiring synchronization for each new packet allows to cope with any possible clock drift over time. In case of a significant clock drift within the packet period, implying any missed or duplicated sample, this will be processed by the receiver as a transmission error. However, a short payload size (as typically targeted in IR-UWB applications) reduces highly the probability of this latter event.

To allow a 1:16 SERDES ratio, an intermediate clock is generated by the *clock_generator* at 125 MHz (*gclk2*). From that clock, two ISERDES with 1:8 ratio are cascaded, forming a 16 bits word at the output of the ISERDES (*data_out*) with a frequency of 62.5 MHz (*gclk1*).

Depending on the number of parallel branches in the *path_selection estimator*, the output size of the *deserializer* module can be greater than 16, and thus a ratio of 1:16 in this case will not be sufficient. Therefore, in order to allow important ratios (greater than 16), a *shift_register* component is added to the two others (*clock_generator* and *ISERDES* components). It is a simple shift register that takes as input the 10, 12, 14, or 16 bits words sent by *ISERDES* and outputs words with a width multiple of the one taken in the input. This does not change the deserializing

factor. It only buffers the data as long as the required number of bits has not been received. While such technique does not decrease the clock frequency, it increases the latency, and thus the number of cycles that can be used to process the received data.

3.2.6 Control and interconnect architecture

The *control and interconnect* module is in charge of the overall scheduling of the non-coherent digital baseband modules. The proposed architecture for this module is depicted in Figure 3.10 and its inputs and outputs are listed in Table 3.5.

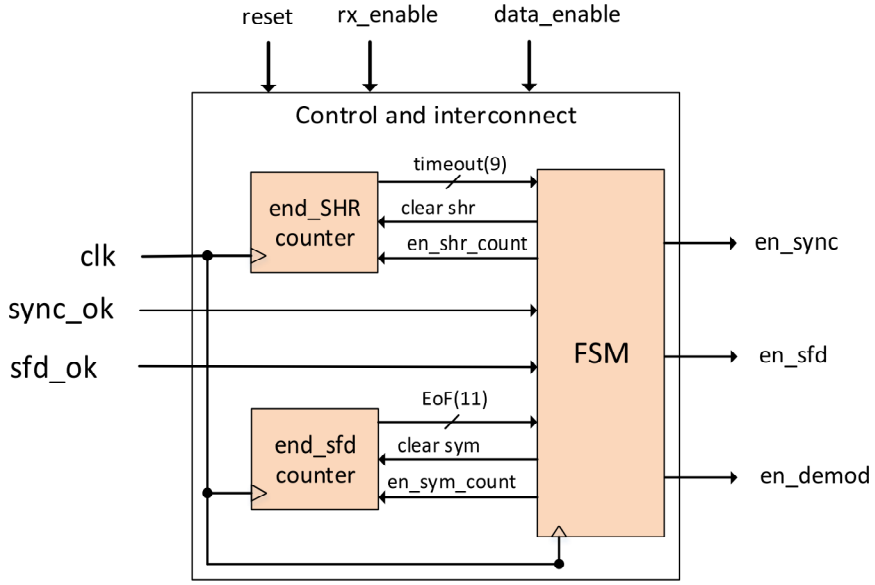


Figure 3.10 — Proposed architecture for the *control and interconnect* module

Name	Input/Output	Signal width	Description
reset	I	1	asynchronous reset
clk	I	1	system clock
rx_enable	I	1	enables the reception process
data_enable	I	1	indicates the validity of the input data
sync_ok	I	1	indicates that the synchronization is acquired
sfd_ok	I	1	indicates that the SFD is detected
en_sync	O	1	enables the synchronization search task
en_sfd	O	1	enables the SFD search task
en_demod	O	1	enables the demodulation task

Table 3.5 — Input/output signals of the *control and interconnect* module

The architecture is composed of 3 components: *FSM*, *end_shr_counter*, and *PSDU_counter*. The *FSM* component provides the global control signals for the different modules of the non-coherent digital baseband receiver presented above. It can enable or disable these modules according to intermediate results or to orders from the Medium Access Control (MAC) layer. Each module can be controlled through the use of a specific enable signal. If the signal is set to 1, the corresponding task is enabled and can be performed. Otherwise, it is disabled.

In order to store information on the processed data flow, two counters are also managed

by the FSM. Both counters (*end_shr_counter* and *PSDU_counter*) are incremented according to input data. The *end_sync_counter* is used to compute and store the processing time. It allows the *FSM* to reacts if too much time is spent on a task, usually by disabling it and restarting the reception process.

The *PSDU_counter* is used to count the number of demodulated bits. As soon as a packet is processed (*EoF* = 1), the FSM stops the demodulation process (*en_demod* = 0).

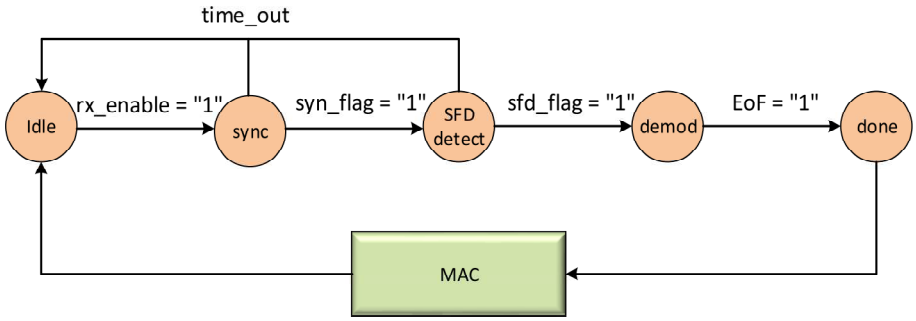


Figure 3.11 — FSM of the *control and interconnect* module

When the MAC layer decides to start the reception process, it triggers the reception block by activating the *rx_enable* signal. The proposed FSM for this module is presented in Figure 3.11. This FSM is composed of five states:

- ***Idle***: in this idle state the receiver waits for the RF board to be configured and for the instruction from the MAC layer to start the reception. Once this instruction is received (*rx_enable* = 1), the FSM goes to *Sync* state, and the receiver starts the search of synchronization.

- ***Sync***: this state corresponds to the synchronization search. Two cases can occur, the first one is when a synchronization is acquired. In this case, the *sync_flag* signal is switched to 1 (active), signalling that a synchronization was acquired and that SFD search must be started (*SFD detect* state). The second case is when the synchronization is failed (timeout); here, the FSM goes back to the *Idle* state. However, due to the path tracking two approaches can be adopted to continue the process. The first approach is to wait for the duration of a given number of symbols noted N, after the detection of the first path (which enables synchronization). N must be lower than the size of the preamble (8 SHR symbols considered in this work). When N symbols have been received after the synchronization time, we start SFD search. This approach limits the number of detected paths and it does not guarantee that the SFD symbol will be found since we do not know where in the input stream the synchronization has been found. If the SNR is sufficiently high, the synchronization may be acquired during the first symbol of the preamble. However, this first approach is simple to implement and greatly reduces the complexity. The second approach keeps trying to synchronize (for path tracking) and activate at the same time the SFD search. This allows more paths to be identified, since the synchronization process is continuous. However, this approach leads to a higher complexity than the first one. Given the better BER performance of this second approach, it has been selected in the final implementation.

- ***SFD detect***: this state activates the SFD search step. When completed, the FSM goes to

the *Demod* state if the SFD is detected, otherwise to the *Idle* state if SFD search timeout occurs. Timeout value for synchronization or SFD search is set to the duration of 8 SHR symbols (the size of the preamble). It is a simple threshold and can be easily configured.

- ***Demod***: at this state the demodulation is performed. A flag is generated when one symbol is demodulated in order to compute the number of demodulated symbols, this allows the generation of EoF signal.

- ***Done***: this state is introduced for proper communication with the MAC (or upper) layer. There is no particular reason to consider that PHY and MAC layers are perfectly synchronized (e.g. with clock cycle precision). For this reason, once a frame is completely processed (either on Rx or Tx datapath), it is necessary for the PHY layer to wait for a proper acknowledgement from the MAC layer before restarting.

3.3 FPGA implementation results

The different architectures presented above, composing the proposed non-coherent digital baseband receiver, have been fully implemented in VHSIC Hardware Description Language (VHDL) including the input interface with the *deserializer* module. In addition to the behavioral and post-synthesis simulations, on-board validation was performed using the development board AES-S6DEV-LX150T-G from Avnet which integrates a Xilinx Spartan 6 LX150T FPGA circuit. Table 3.6 summarizes the synthesis results targeting this FPGA circuit.

Hierarchical Unit	**FPGA** (Xilinx Spartan6(Lx 150T))		
	Slice regs. Available: 184304	**LUTs** Available: 92152	F_{max} (MHz)
Synchronization (1 path)	127 (0%)	431 (0%)	123.7
SFD detector	25 (0%)	110 (0%)	182.6
Fully-parallel path_selector	10474 (5%)	34735 (37%)	102.9
Synchronization (4 paths)	259 (0%)	954 (1%)	92.3
Partially-parallel path_selector	5635 (3%)	18832 (20%)	90.3
Control and interconnect	27 (0%)	51 (0%)	262.7
Decision	450 (0%)	932 (1%)	185.2
Proposed DBB (fully parallel)	10932 (6%)	35618 (38%)	119.1
Proposed DBB (partially parallel)	6102 (3%)	19811 (21%)	72.8

Table 3.6 — FPGA synthesis results

The results illustrate, at first glance, the hardware efficiency of the proposed synchronization and SFD detector architectures. Both modules require very low resources utilization: 127 Flip-Flops (FF) and 431 Look-Up Tables (LUT) for the *synchronization* module, in addition to 25 FFs and 110 LUTs for the *SFD* detector. Moreover, it can be noticed that the proposed architecture does not require any multiplier (DSP resources). This information is not provided in Table 3.6 since all blocks require zero DSP resources.

Regarding the *path_selector* module before optimization, i.e. fully-parallel architecture with 64 branches, the overall resources utilization in terms of Flip-Flops and LUTs is almost multiplied by 64 when compared with a single synchronization module and SFD detector. About 10K

Flip-Flops (∼5% of the available resources) and 35K LUTs (∼37% of the available resources) are needed to implement this module.

If we analyse now at the optimized partially-parallel architecture, we notice significant reduction in resource occupation. In this case, given the deserializer implementation, each branch is able to process 4 paths. As it was explained in the previous section, this requires an operation clock frequency of 62.5 MHz, which is attainable given the synthesis results. The modified multipath synchronization module uses about twice the resources when compared to a single path module. This is justified by the additional control and storage requirements. However, since 4 paths are processed within one module, it results in an overall resources usage divided by almost 2 for this partially-parallel architecture that requires 16 branches rather than 64 for the fully-parallel architecture. The obtained maximum clock frequency is 92.3 MHz, which is above the requirement (62.5 MHz). Thus, the proposed optimization allows to almost halve the hardware complexity without limiting the input data rate. This is in addition to the increased communication performance when the multiple paths are recombined to take a decision.

Considering the total resource occupation of proposed non-coherent digital baseband:

- when no optimization is applied (fully-parallel architecture): 10K FF (∼5% of the available resources) and 35k LUTs (∼36% of the available resources).
- optimized partially-parallel architecture: 6K FF (∼2% of the available resources) and 19k LUTs (∼18% of the available resources).

Taking into account the low resource utilization of the decision module (450 FF and 932 LUTs) and control and interconnect module (27FF and 51 LUTs), the overall complexity fits mostly in the *path_selector* module.

Overall, the proposed low-complexity architecture of non-coherent IR-UWB baseband processing offers good opportunities for integration in low-cost low-power BAN devices. These digital baseband architectures have also been designed to be flexible to allow their use with any non-coherent front-end. Regardless the detection method, the proposed implementation needs simply an input bit stream that corresponds to the detection or no of the received signal.

Finally, it is worth to highlight the lack of detailed hardware implementations related to IR-UWB systems in the literature. The few published contributions in this regard present a complete receiver and often focus on the presentation of the analog front-end. This is particular true in the context of the recent IEEE 802.15.6 standard and the critical synchronization issue which is a hard task to accomplish in any communication system, especially in IR-UWB systems where the adoption of very narrow pulses demands very high accuracy. In this context, the presented results in this work constitute a reference in this domain where the available literature is rather scarce.

In order to illustrate this issue, among the few available published contributions we can cite reference [117] which presents an FPGA and ASIC implementation of an IR-UWB baseband transceiver for the standard IEEE 802.15.4a. In fact, the UWB-based specification of this standard presents strong similarities with that of IEEE 802.15.6 standard. However, the paper presents FPGA resources occupation and ASIC area in mm^2 for the complete transceiver (Tx and Rx). The individual results of each module is unfortunately not provided. In addition,

several system parameters are different which makes the conducting of a direct comparison or through technology normalization meaningless. For instance, the transmitter baseband in reference [117] integrates a convolutional and Reed-Solomon channel coders with BPSK and binary position modulation.

3.4 Summary

In this chapter the different proposed architectures that implement the algorithms presented in the previous chapter have been presented. Original low-complexity architectures have been proposed for synchronization, SFD detection, path selection estimation, and decision modules for non-coherent IR-UWB receiver in the context of low-complexity low-power BAN devices. These digital baseband architectures have also been designed to be flexible to allow their use with any non-coherent front-end providing an input bit stream that corresponds to the detection or no of the received signal.

The chapter provided first an overview of the target digital baseband transceiver and the associated interfaces with the dual front-end and the application board in the context of the RUBY project. The non-coherent front-end provides the outputs of a threshold comparator through multiplexed LVDS link at 1 GHz frequency. A serial-to-parallel converter transforms the serial input data into an output parallel stream for digital processing at reasonable clock frequency for the target FPGA circuit.

Detailed description of each proposed architecture is provided with input/output signals, main constituent components, and the finite state-machine that schedules the different operations. The FPGA implementation demonstrates the very low complexity of the proposed multiplier-less architectures for synchronization, SFD detection, and decision modules. The main complexity of the digital baseband lies in the path selection estimator and multipath processing which constitute a crucial requirement in IR-UWB system and BAN application context. For this module, novel optimisation is proposed with a partially-parallel architecture that reduces significantly the implementation complexity and allows for multipath processing. The proposed architecture, with respect to the fully-parallel architecture, allows to reduce the number of parallel branches by a factor of 4 (from 64 to 16) at the cost of increasing the complexity of each branch by almost a factor of 2. In fact, when targeting a Xilinx Spartan 6 FPGA, the architecture of the synchronization module processing one path occupies 127 FFs and 431 LUTs, while the one processing 4 paths occupies 259 FFs and 954 LUTs thanks to the proposed adequate resource sharing. Thus, the proposed optimisation allows to almost halve the hardware complexity without limiting the input data rate. This is also confirmed by the obtained maximum clock frequency for the proposed partially-parallel architecture (92.3 MHz) which is still above the target requirement (62.5 MHz).

These results illustrate the hardware efficiency of the proposed architectures and offer good opportunities for integration in low-cost low-power BAN devices. It is worth to highlight in this context the lack of detailed hardware implementations related to IR-UWB systems in the literature, in particular for the recent IEEE 802.15.6 standard.

CHAPTER

4 Hardware prototyping and on-board demonstration

THE last two chapters have presented the main contributions of this PhD work regarding algorithm and architecture design for IR-UWB wireless communication systems. This chapter presents another major contribution regarding on-chip prototyping and the integration of these contributions into a real hardware demonstration platform.

On-chip prototyping is a crucial step to fully validate the proposed algorithms and architectures on a dedicated hardware platform and under real channel conditions. It also generally leads to valuable feedbacks to the architecture design particularly regarding radio-frequency and system-level interfacing. However, it is a complex task in the context of IR-UWB systems where the adoption of very narrow pulses demands very high accuracy and implies strengthen constraints in the design, integration and test experiments at both chip and board levels. This is particularity true in the context of this work targeting synchronization and signal detection issues using a mixed analog-digital front-end with a hybrid coherent/non-coherent receiver structure.

The chapter presents first the context and the general architecture of the proposed hardware demonstration platform. Then, detailed description of the different constituent boards and test environment is provided. Finally, measured performance results under real wireless transmissions are presented and discussed.

4.1 Context and general architecture

As it has been introduced in the starting of this manuscript, the presented contributions were performed in the context of a French collaborative research project, namely *RUBY* (Radio UWB for BodY area network) [90], coordinated by Orange Labs. The goal of this project is to propose and implement an innovative UWB impulse radio system particularly suited to Body Area Network. A proof-of-concept was planned through a complete hardware prototype that integrates RF and digital circuits designed during the project. The target system is based on the following contributions:

- An innovative RF front end, establishing pioneering receiver architecture, inspired by and taking benefits of both coherent and non-coherent receiver architectures, that will permit to reach promising RF performances without harming complexity and power consumption.
- A fully integrated (single chip) transceiver, operating in the low UWB band, able to demonstrate the feasability of such an integration.
- A pionnering RF design, optimized to allow efficient UWB operation on the higher UWB band (6-8.5 GHz), were BAN can be used in conformance with European UWB regulation.
- A very constrained analogue to digital conversion.
- An event-driven digital baseband who will be able to efficiently drive this new RF front end, that opens the way to a power-efficient design that is driven by events instead of a high speed clock signal.
- Miniaturized UWB antenna designed to be used in the close vicinity of a human body.

The original idea is based on the proposal of an hybrid architecture (Figure 4.1) that combines coherent and non-coherent receivers in order to compensate the weaknesses of one by the forces of the other and vice versa. Practically, the hybrid (or dual) architecture performs preamble detection, synchronization and initial channel estimation in a very short time using a low-complexity low-power non-coherent front-end, and then moves to a higher sensitivity (low Eb/N0 requirement) coherent front-end which completes the channel estimation and performs high data rate symbol detection and demodulation.

In fact, in this approach, the first part of the received preamble is processed by the non-coherent receiver which detects the incoming of a packet and estimates the position of the preamble symbols as well as the position of incoming paths resulting from the propagation phenomenon. The identified paths are then delivered to the coherent receiver for estimating the complex amplitude of each detected path and to select the best two paths minimizing the inter symbol interference (ISI) criterion during the rest of the preamble. Selecting two paths arises from the fact that the coherent receiver embeds a 2-Rake 2 ns integrator. Once the two best candidates are found, the phase of SFD research starts by exploiting the SFD symbol. If the SFD is detected, the receiver demodulates the following received data symbol.

Therefore, this dual front-end receiver approach is suitable for energy-efficient high data-rate applications. However, in case of a low data rate application, a simple non-coherent receiver can

be used. To that end, SFD detection and fusion decision algorithms were proposed (Chapter 2) and associated architectures were designed (Chapter 3) to complete the non-coherent reception chain. In this case, the coherent receiver can be switched off leading to significant energy saving.

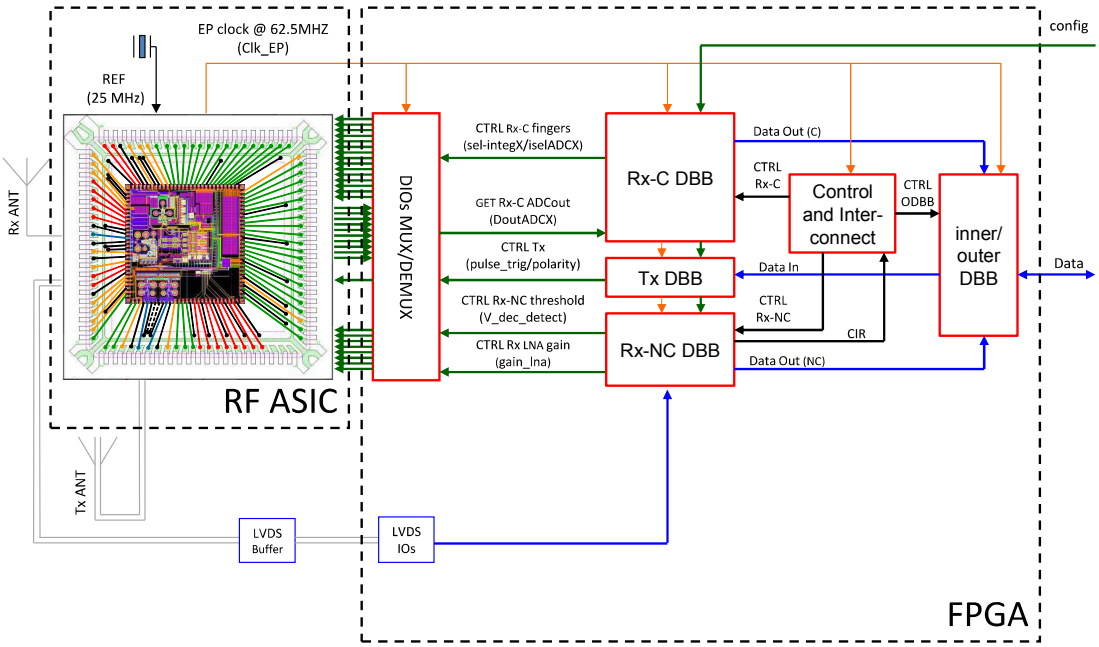


Figure 4.1 — Hybrid architecture proposed by the RUBY project, combining coherent and non-coherent receivers

As illustrated in Figure 4.1, the proposed baseband architecture is composed of 5 main parts: (1) the transmitter, (2) the coherent receiver, (3) the non-coherent receiver, (4) the control and interconnection part, and (5) the inner/outer baseband part. In addition to the main transceiver blocks presented in the previous chapters, the inner/outer baseband consists of two sub-blocks, the *inner* baseband and the *outer* basband. The purpose of the inner baseband block, at the transmitter side, is to implement the processes of scrambling, encoding, and interleaving data, as defined by IEEE 802.15.6 standard in order to provide robustness against transmission errors. The *outer* baseband, at the receiver side, refers to the bit-level processing block that executes once either the non-coherent or the coherent baseband has performed the demodulation. It is composed of 3 components, which are the descrambler (Descr.), the de-interleaver (Deinterl.) and forward error decoder (Decoder) that perform the inverse operation of scrambling, interleaving, and encoding. The control and interconnection part has 2 main functions: (1) it manages the interconnection between the baseband blocks and between the analogue and the digital domains, and (2) it controls the baseband configuration and execution tasks.

Regarding the validation flow of the digital baseband concerned by this PhD work, the proposed algorithms have been validated first through Matlab software simulations (Chapter 2). The algorithms have been integrated into a complete Matlab UWB simulator and adequate BAN channel models, as specified in the IEEE802.15.6, have been used. Such software-level simulations allowed to test, correct, improve and estimate the performance of the proposed algorithms. This developed Matlab software model and the associated results constitute in addition a ref-

erence for the subsequent steps related to the hardware implementation. In a second step, low complexity hardware architectures have been proposed. Validation and performance evaluation of these architectures have been performed through a dedicated implementation targeting an adequate FPGA circuit and associated evaluation board (Chapter 3). Then in the last step, presented in this chapter, real-time validation is conducted with real signals and wireless transmissions through a complete hardware platform that integrates in addition RF and application boards.

To that purpose, two hardware platforms have been built using the same RF board, yet different FPGA and application boards. The first one was intended for the test and the debug of the UWB transceiver. The second one was intended for system-level performance analysis and real-time video streaming demonstration. This second platform was in debugging phase at the writing of this manuscript due to an important delivery delay of a power adapter board. However, we succeeded to use the first platform, assembled at CEA-Leti, in order to validate the proposed architectures for synchronization and path selection. The proposed architectures have been integrated in the FPGA board and real-time measurements have been conducted through the integration of Xilinx ChipScope logic analyzer to the designed architectures. Xilinx ChipScope logic analyzer allows to probe and visualize the internal signals of the design inside the FPGA during the wireless transmission experiments. The rest of this chapter provides detailed description of the different constituent boards of the first functional hardware platform, in addition to the measured performance results under real wireless transmissions.

4.2 IR-UWB hardware prototype

In the above described context, this section describes the functional hardware prototype designed for on-board validation. It consists mainly of a radio frequency board implementing the analog front-end, an FPGA board for digital processing that integrates the proposed architectures described in the previous chapters, and a microcontroller-based application board.

4.2.1 Analog front-end and radio frequency board

The radio frequency (RF) board is designed around a single CMOS 130 nm chip operating in the 4 GHz band [4]. This chip implements an IR-UWB transmitter and a dual-front-end combining coherent and non-coherent receivers. The dual front-end receiver allows to perform preamble detection, synchronisation and initial channel estimation in a very short time with a low-complexity low-power non-coherent receiver and then moves to a higher sensitivity coherent receiver which completes the channel estimation and performs symbol detection and demodulation, either in a coherent or non coherent manner. The RF board integrates in addition a 25 MHz clock oscillator (used to generate the 62.5 MHz clock frequency needed by the system) and the Rx and Tx antennas (or SMA coaxial RF connectors for testing and measurements).

Regarding the coherent front-end, the outputs of the analog-to-digital converters are conveyed to the digital board in DDR mode using a 62.5 MHz clock (Figure 4.2). A stacking board connector (QSH high-speed family) is used to vehicle these signals, in addition to other configuration signals, test, reset, clocks, and power supply. However, for the non-coherent front-end, the outputs of the threshold comparator are conveyed through multiplexed LVDS link using a dedicated connector (Figure 4.3).

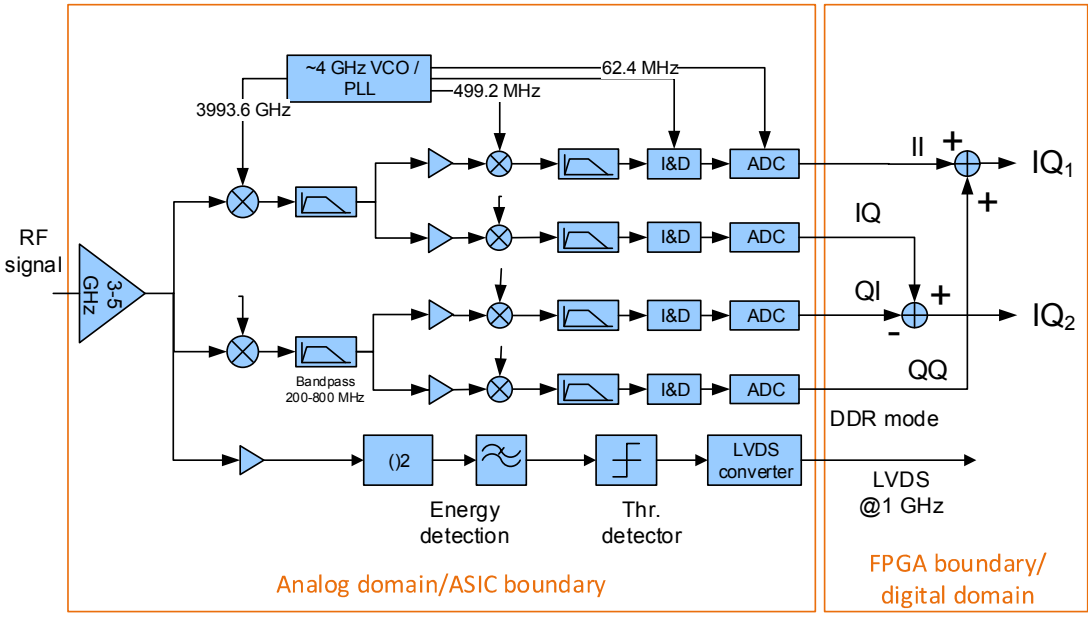


Figure 4.2 — Dual front-end: coherent and non-coherent receivers on a single ASIC chip

In fact, two versions of this board have been developed as illustrated in Figure 4.3. One integrating antennas (Figure 4.3a) for on-air wireless transmissions and the second rather integrating SMA connectors (Figure 4.3b) for test and debugging purposes.

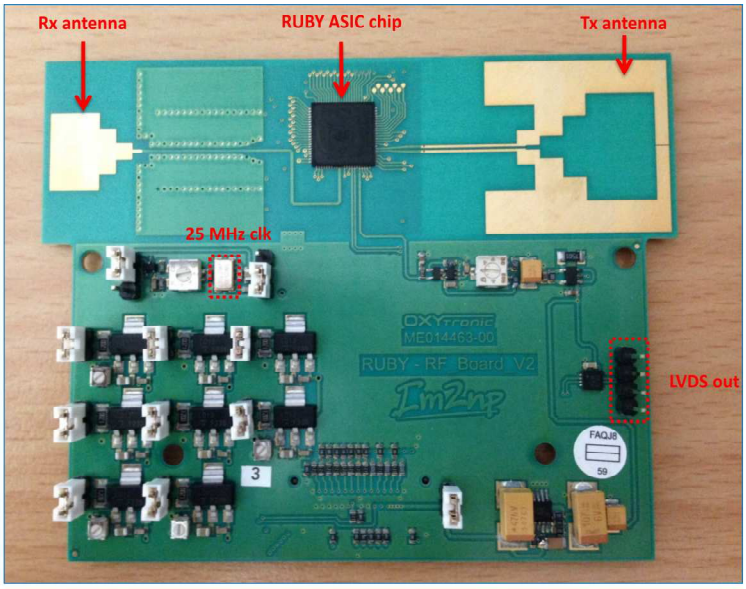
4.2.2 Digital front-end board

Regarding the digital board (Figure 4.4), it integrates a Xilinx FPGA Spartan6 LX100 which features enough resources to meet the design requirement. For FPGA configuration, a non-volatile FLASH memory and a JTAG interface are also integrated. Moreover, two QSH stacking board connectors are used to connect the digital board to the RF board and to a PXI adapter board. This latter allows to connect the demonstrator to a host computer through a PXI platform from *National Instruments* for measurement, control, and test purposes. The digital board integrates in addition an 18 pins connector used to input, output, and visualize the main signals during the debugging step.

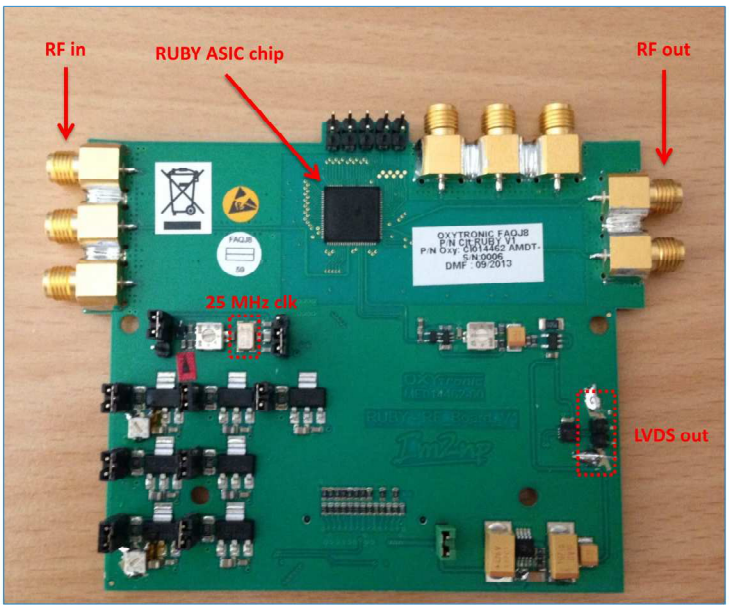
4.2.3 Application board and platform setup

The application board is an internal development board based on the Atmel AT91SAM9261 microcontroller that have been modified to meet the target prototype requirements. Two serial communication peripherals are used in the context of this demonstrator. A UART peripheral is used to *run* or *stop* the demonstrator while an SPI peripheral is used for data and control transfers.

When the demonstrator is powered-up, the application board configures the digital board in transmitter or receiver mode and sends the initial configuration to the RF board through the FPGA. This initial configuration allows to program the different parameters of the front-end CMOS chip (such as LNA gain, non-coherent receiver's comparator threshold, activating ADCs



(a) RF board with antennas



(b) RF board with SMA connectors

Figure 4.3 — Radio frequency board of the IR-UWB demonstrator

for the coherent front-end). Once both digital and RF boards are configured, the application board starts sending or receiving data through its interface with the digital board.

Frames that matches the IEEE 802.15.6 standard specification are transmitted in loop: 8 preamble symbols, one SFD symbol, and 256 bytes of data symbol. The above described boards are stacked together as illustrated in Figure 4.5 to form the on-board prototype for validation and demonstration purposes.

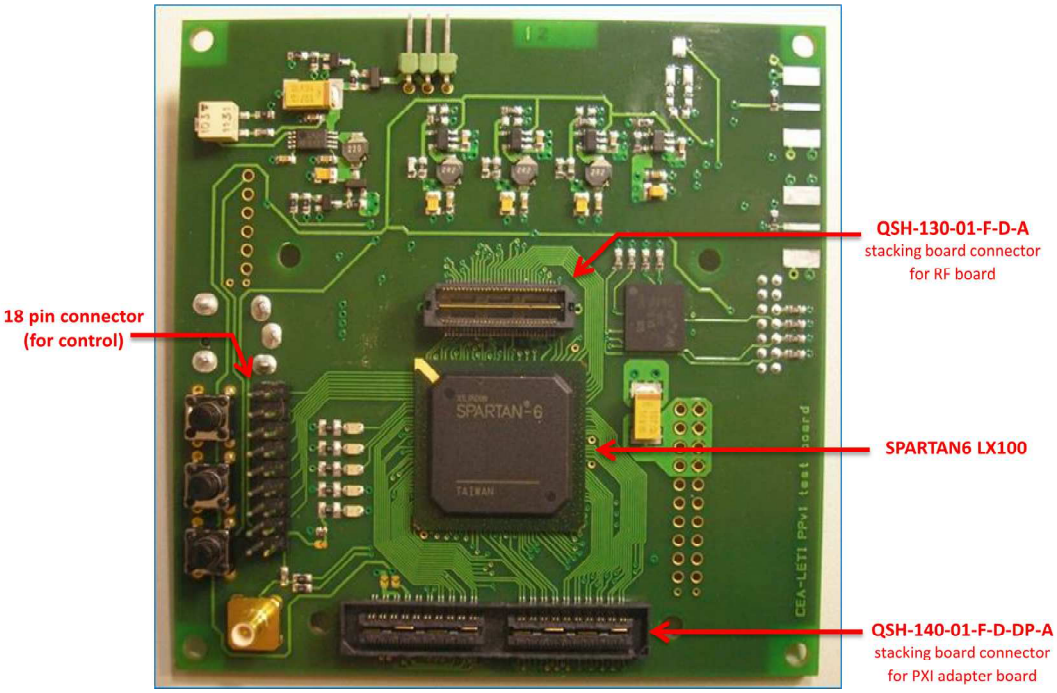


Figure 4.4 — Digital front-end board of the IR-UWB demonstrator

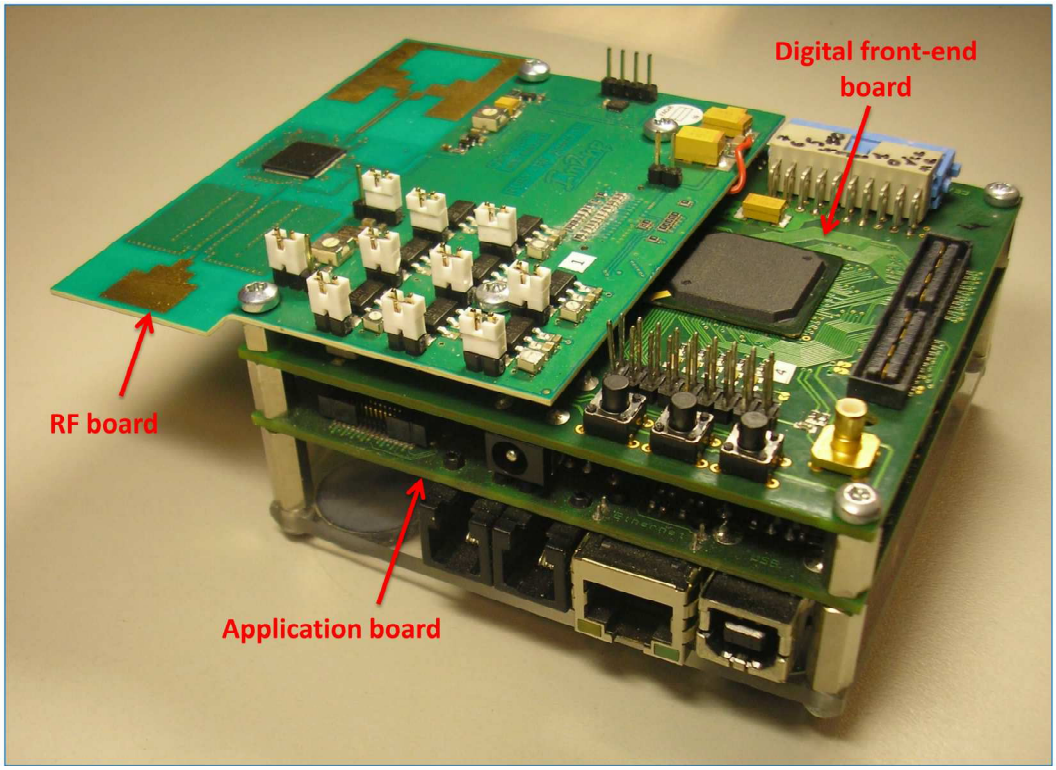


Figure 4.5 — Assembled boards of the IR-UWB demonstrator

4.3 Experiment results with real wireless transmissions

Using the above described hardware prototype, real wireless transmissions between one Tx and one Rx configured boards have been conducted in laboratory environment.

The considered radio link parameters are summarized in Table 4.1.

Parameter	**Value**
Bandwidth	1800 GHz
Central frequency	4 GHz
Number of SHR symbols	9 (8 preamble + 1 SFD)
T_w	1.2 ns
L	64
Kasami sequence	4^{th} sequence
Modulation	OOK (SHR), 2-PPM (payload)

Table 4.1 — Radio link parameters for the experiments with real wireless transmissions

Conducted experiments have been done in LOS channel conditions with a distance range of $\approx$ 1 meter. For NLOS channel transmissions, a human hand was placed in the direct line between Tx and Rx. For each experiment, an acquisition of 1024 frames was performed. Xilinx ChipScope logic analyzer has been integrated to the designed architectures for synchronization and path selection estimation. It allows to probe and visualize the internal signals of the design inside the FPGA.

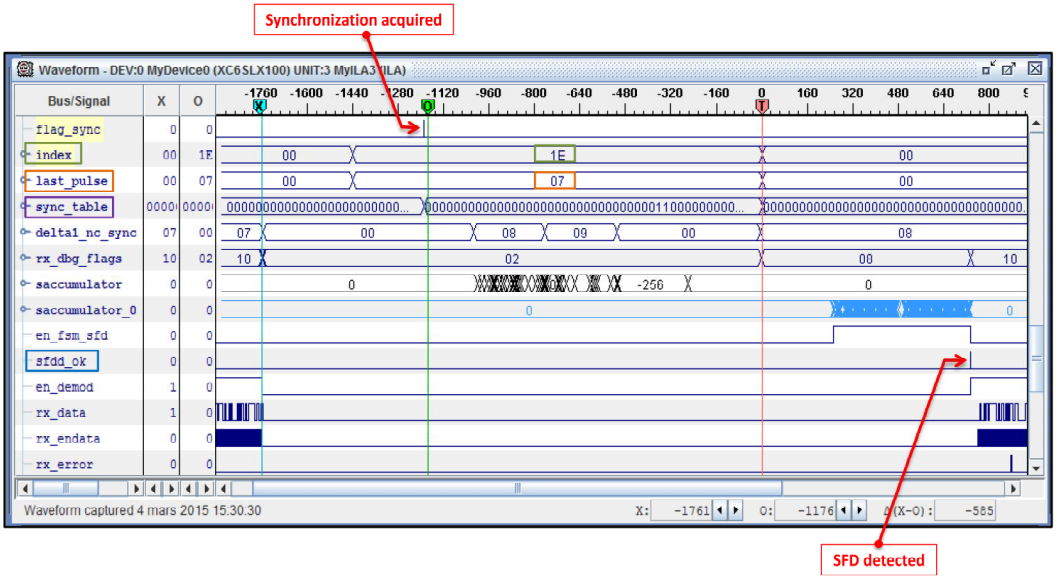
4.3.1 Synchronization and multipath identification measurement

The obtained results show that the number of detected paths range from 1 to 4 for all conducted experiments. In most cases two or three paths are identified: two paths have been detected in 46.9% of the received frames and three paths in 44.4%. On the other hand, only 6.1% of the received frames correspond to one detected path and 2.6% to four detected paths.

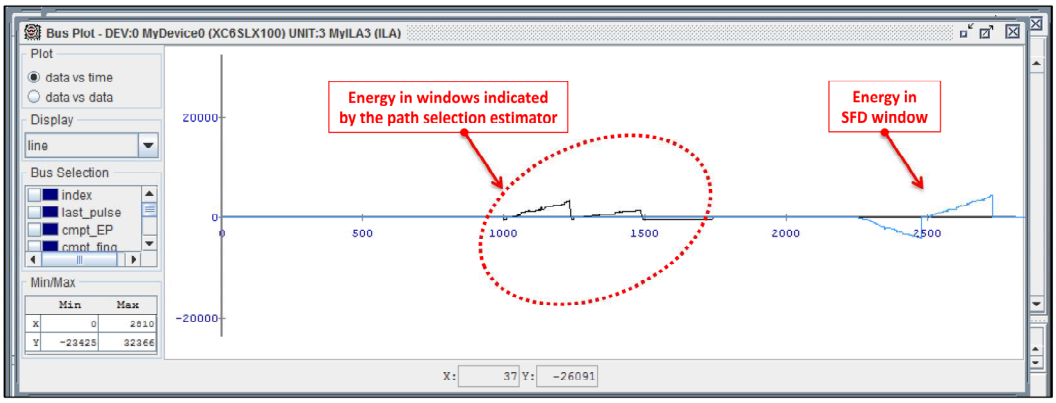
An example of the measured results using ChipScope logic analyzer is illustrated in Figure 4.6. This example corresponds to the case where two paths are identified. Figure 4.6a captures main signals of the complete digital baseband receiver, while Figure 4.6b depicts the collected energy by the coherent receiver in the window that corresponds to the identified paths by the non-coherent path selection estimator.

The figure highlights four signals for the synchronization and path selection estimation: *flag_sync*, *index*, *last_pulse*, and *sync_table*. The *flag_sync* signal indicates the acquisition of a synchronization. In fact, when the synchronization is acquired (first detected path), the receiver continues for one symbol duration before activating the *flag_sync* signal. This is done in order to leave enough time for the other branches to converge and thus to identify other possible paths. Once the *flag_sync* goes to '1', the synchronization task is stopped and the different results from the non-coherent synchronization and path selection estimator are provided to the coherent part of the dual front-end receiver for SFD detection and bit decision. These provided results are:

- The *sync_table* signal which indicates the positions of the detected paths in the pulse repetition period (PRP). It consists of a bit vector of size 64 (LT_w = 64 ns), with each bit



(a) Main signals of the complete digital baseband



(b) Collected energy by the coherent receiver

Figure 4.6 — Example of the hardware measured results with real wireless transmissions using ChipScope logic analyzer

representing the state of a path (i.e. 0 = no path, 1= path detected).

- The *index* signal which provides the position of the first detected path (in the range 0 to 63) within the *sync_table*, i.e. within a PRP. In fact, the first detected path is not necessarily the first appeared '1' in the *sync_table* vector. This is due to the channel delay that creates a shift when acquiring and parallelizing the data. This crucial result (*index*) constitutes a reference for the other paths, and provides the delay between the transmitter and the receiver.

- The *last_pulse* signal which indicates the pulse that allows the synchronization within the Kasami sequence (Chapter 3, cf. Section 3.2.1) for the first path. This result allows to deduce the starting of the next symbol (symbol boundary).

In the example of Figure 4.6 two paths are detected with the first path at the 30^{th} branch (0x1E).

4.3.2 SFD detection measurement

The acquired synchronization as well as the identified paths are confirmed by the coherent part of the receiver which allows to discard false alarms. For the acquired synchronization, the well detection of the SFD validates the non-coherent synchronization result (*sfdd_ok* activated, i.e. SFD window contains energy). For the identified paths, the energy is measured by the coherent receiver in windows that correspond to the identified path positions. As it can be seen in Figure 4.6b, these windows contain energy confirming thereby the results of the non-coherent path selection estimator.

4.3.3 Channel impulse response measurement

In order to further analyze the hardware prototype results, the channel impulse response was measured using the coherent receiver. Figure 4.7 illustrates the obtained results of 2 measured CIR examples. The first one corresponds to a LOS channel transmission, while the second CIR example corresponds to a NLOS case.

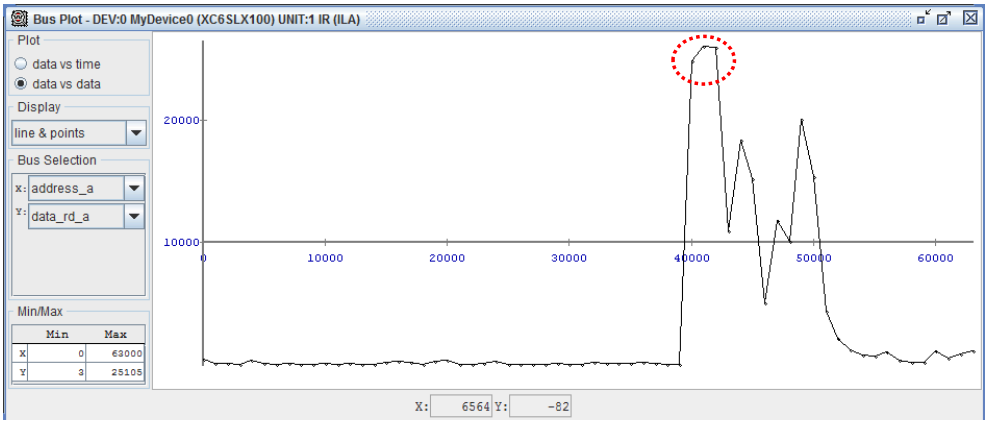
In LOS channel conditions, several paths are identified and the strongest path is in the first position. However, this is not the case for the NLOS experiment example where $\approx$ 5 paths are observed and the strongest path comes at the second position. This behaviour has been confirmed through many conducted experiments. In fact, as expected in the case of NLOS transmission, a time delay between the first path and the strongest one is observed. During the different conducted experiments, it was observed that the CIR has mostly a maximum time spread of 10 ns, with an observed number of paths ranging from 2 to 5, and a rapidly decreasing energy both in LOS and NLOS channel conditions.

The rapidly decreased power delay profile (PDP) leaves only the first paths accessible to the non-coherent receiver as the adopted receiver approach relies on threshold comparator. This confirms the obtained results of the non-coherent path selection estimator in terms of detected paths (from 1 to 4, cf. Section 4.3.1) and illustrates the effectiveness of the proposed approach.

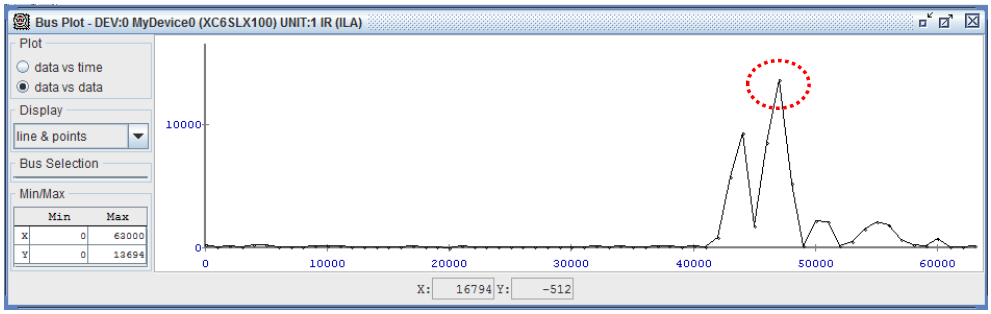
4.4 Summary

In this chapter a complete real-time hardware prototype has been presented for on-board validation and demonstration using real wireless transmissions and channel conditions. This prototype consists of an FPGA-based board that integrates the proposed architectures described in the previous chapters, a radio frequency board implementing the analog front-end, and a microcontroller-based application board. It has been developed in the context of the French collaborative research project RUBY, coordinated by Orange Labs, which constitutes the framework of this PhD contribution. Several successful experiments have been conducted with LOS and NLOS BAN channel conditions and typical radio link parameters. The internal signals of the FPGA circuit integrating the proposed architectures have been probed and visualized using Xilinx ChipScope logic analyzer.

In the available time and due to important delivery delay of a power adapter board, only the architectures for non-coherent synchronization and path selection have been integrated in this



(a) Case of LOS channel conditions



(b) Case of NLOS channel conditions

Figure 4.7 — Examples of measured channel impulse response in LOS and NLOS channel conditions

prototype. The receiver has been completed by the available coherent part of the dual baseband receiver. Measured results illustrated the rapid acquisition of synchronization and the effectiveness of the path selection estimator to identify the main paths using the proposed low-complexity non-coherent receiver. These results have been confirmed by the coherent part of the dual front-end receiver through SFD detection and the collected energy in the windows corresponding to the identified path positions. Channel impulse response was also measured in the conducted experiments using the coherent receiver in order to further analyze and validate the hardware prototype results.

In fact, hardware prototyping is a complex task in the context of IR-UWB systems where the adoption of very narrow pulses demands very high accuracy and implies strengthen constraints in the design, integration and test experiments at both chip and board levels. However, it is still a crucial step to fully validate the proposed algorithms and architectures under real channel conditions, including the effects of RF impairments and board-level integration. In this context, the presented contribution in this chapter constitutes a valuable proof-of-concept of the proposed algorithms and architectures and the obtained results constitute a reference in this domain where the available literature is rather scarce.

Conclusions and perspectives

THE theoretical capacity of UWB technology to address low-complexity low-power devices has reached a large maturity, thanks to its intrinsic flexibility, its ultra-low radiated power and to its potential for ultra low power implementations. This is confirmed by its adoption in the recent IEEE 802.15.6 standard for wireless BAN. This adoption stimulates the research in this domain and offers new opportunities for standard-compliant algorithms and hardware architectures.

This thesis work has investigated the design of low-complexity non-coherent IR-UWB baseband receiver, compliant with IEEE 802.15.6 for BAN applications. The main context concerns the French collaborative research project RUBY which targets the proposal of an hybrid architecture that combines coherent and non-coherent receivers in order to combine low-complexity, low-power, and high data rates.

Several contributions have been proposed in the algorithmic domain and in the associated hardware implementation domain.

In *algorithmic domain*, several non-coherent reception techniques have been proposed: (1) rapid and flexible synchronization algorithm, (2) simple SFD detection technique, (3) path selection estimator, and (4) fusion decision algorithm which supports PPM modulation scheme.

The synchronization algorithm is based on a dedicated finite state machine, which detects the sequence of time intervals between pulses and compares it to the synchronization symbol based on a Kasami sequence. The algorithm has been adapted to accommodate for possible transmission errors, and can be parameterized to support any synchronization symbol. A correlation method for SFD detection was also proposed. It especially allows to minimize conjointly the false synchronization and the missed SFD detection. The good resolution (1 ns) offered by the adopted non-coherent receiver was exploited to design a parallel architecture in order to detect the different resolvable paths available in the IR-UWB signal, thus benefiting from the multipath propagation phenomena instead of only suffering from it. A channel estimation architecture was also proposed. The decision fusion algorithm relies on a weighted multipath processing method targeting the PPM modulation.

With these algorithms, the receiver is able to meet the requirements of the hybrid coherent/non-coherent receiver architecture targeted by the RUBY project. In addition, if the sensitivity of the non-coherent front-end is sufficient for the target application, the receiver allows to fully process the received signal in a non-coherent manner, thus reducing the need for a complex and costly coherent front-end.

The simulation results presented in this chapter show the efficiency of the proposed techniques. Synchronization performances show success rates with different Ep/N0 values depending on the channel model and its nature (LOS or NLOS). The algorithm also allows a short

synchronization time. Less than 2 symbols are required to reach 99.9% synchronization rate. Moreover, the proposed algorithm can deal with any IEEE 802.15.6 sequence (preamble symbol) and can be extended to other sequences.

The decision fusion algorithm performance is presented in term of BER. The algorithm takes advantage of multipath processing, and the performance improvement has been demonstrated in the results. Error floor was mitigated when using more than one path to take a decision. Two main results are observed depending on the channel model. In CM3 channel model, good BERs are obtained. BER of 10^{-4} was reached at Ep/N0 $\approx$ 28dB. Results were not as good in CM4 channel. This channel is very aggressive, and very strong ISI are introduced due to the selected symbol time in the standard. The digital baseband performances are provided in terms of BER and PER in CM3 channel model. Considering the specified use cases of the RUBY project, the proposed solution is sufficient to meet the target data rate and sensitivity requirements.

In *hardware implementation domain*, original low-complexity architectures have been proposed to implement the algorithms presented above for synchronization, SFD detection, path selection and fusion decision algorithm. These digital baseband architectures have also been designed to be flexible to allow their use with any non-coherent front-end providing an input bit stream that corresponds to the detection or no of the received signal.

In fact, the non-coherent front-end provides the outputs of a threshold comparator through multiplexed LVDS link at 1 GHz frequency. A serial-to-parallel converter transforms the serial input data into an output parallel stream for digital processing at reasonable clock frequency for the target FPGA circuit.

Detailed description of each proposed architecture was provided in the manuscript with input/output signals, main constituent components, and the finite state-machine that schedules the different operations. The FPGA implementation demonstrates the very low complexity of the proposed multiplier-less architectures. The main complexity of the digital baseband lies in the path selection estimator and multipath processing which constitute a crucial requirement in IR-UWB system and BAN application context. For this module, novel optimisation is proposed with a partially-parallel architecture that reduces significantly the implementation complexity and allows for multipath processing. The proposed architecture, with respect to the fully-parallel architecture, allows to reduce the number of parallel branches by a factor of 4 (from 64 to 16) at the cost of increasing the complexity of each branch by almost a factor of 2. In fact, when targeting a Xilinx Spartan 6 FPGA, the architecture of the synchronization module processing one path occupies 127 FFs and 431 LUTs, while the one processing 4 paths occupies 259 FFs and 954 LUTs thanks to the proposed adequate resource sharing. Thus, the proposed optimisation allows to almost halve the hardware complexity without limiting the input data rate. This is also confirmed by the obtained maximum clock frequency for the proposed partially-parallel architecture (92.3 MHz) which is still above the target requirement (62.5 MHz).

These results illustrate the hardware efficiency of the proposed architectures and offer good opportunities for integration in low-cost low-power BAN devices. It is worth to highlight in this context the lack of detailed hardware implementations related to IR-UWB systems in the literature, in particular for the recent IEEE 802.15.6 standard.

Finally, a complete real-time hardware prototype has been presented for on-board validation and demonstration using real wireless transmissions and channel conditions. This prototype

consists of an FPGA-based board that integrates the proposed architectures described above, a radio frequency board implementing the analog front-end, and a microcontroller-based application board. It has been developed in the context of the RUBY project, which constitutes the main framework of this PhD contributions. Several successful experiments have been conducted with LOS and NLOS BAN channel conditions and typical radio link parameters. The internal signals of the FPGA circuit integrating the proposed architectures have been probed and visualized using Xilinx ChipScope logic analyzer.

In the available time and due to important delivery delay of a power adapter board, only the architectures for non-coherent synchronization and path selection have been integrated in this prototype. The receiver has been completed by the available coherent part of the dual baseband receiver. Measured results illustrated the rapid acquisition of synchronization and the effectiveness of the path selection estimator to identify the main paths using the proposed low-complexity non-coherent receiver. These results have been confirmed by the coherent part of the dual front-end receiver through SFD detection and the collected energy in the windows corresponding to the identified path positions. Channel impulse response was also measured in the conducted experiments using the coherent receiver in order to further analyze and validate the hardware prototype results.

In fact, hardware prototyping is a complex task in the context of IR-UWB systems where the adoption of very narrow pulses demands very high accuracy and implies strengthen constraints in the design, integration and test experiments at both chip and board levels. However, it is still a crucial step to fully validate the proposed algorithms and architectures under real channel conditions, including the effects of RF impairments and board-level integration. In this context, the developed hardware prototype constitutes a valuable proof-of-concept of the proposed algorithms and architectures and the obtained results constitute a reference in this domain where the available literature is rather scarce.

Perspectives

Regarding work perspectives, several ideas can be investigated:

- Regarding the synchronization algorithm, a fine-grained stopping criteria can be investigated such as the detection of a significant consecutive distances rather than all distances. A major challenge in this context is to determine the minimum required number of identified distances that allows to keep the communication performance unaltered. If this number can be reduced, even dynamically depending on channel conditions for example, this would allow for further reductions in synchronization time, hardware complexity, and energy consumption.

- Adjusting dynamically the threshold comparator by introducing a metric related to SNR. This can be possible if we exploit the bit error probability estimated by the *SFD detector*. The number of errors during a time interval can provide an idea of the SNR or the channel quality. In the case when the SNR is high (low bit error probability), the threshold can be shifted upward during the demodulation task. This will mitigate the false alarm of noise,

and thereby improves BER. In the same way, if the SNR is low (high bit error probability), the threshold can be shifted downward, and therefore increasing the sensitivity of the receiver.

- Evaluating the energy consumption of the complete dual RF front-end and digital baseband receiver for an ASIC target technology and maximum achievable data rates. The proposed hybrid architecture allows different configurations and the proposed complete non-coherent receiver offers good potential for significant energy reductions. It would be interesting in this context to evaluate the maximum achievable data rate for the complete non-coherent receiver and propose dynamic configuration approach of the hybrid receiver depending on the channel conditions and target application.

APPENDIX

A IEEE802.15.6 IR-UWB PHY preview

We provide in this appendix a preview of the IEEE 802.15.6 BAN standard. This preview is part of the background of this PhD work which adopts largely IEEE 802.15.6 standard specifications and models.

A.1 Spectrum usage

The standard specifies two frequency bands: low band, and high band, which characteristics are highlighted in Table A.1.

Each band includes operating frequency channels; three in the low band (channels 0-2) and

Band group	**Channel number**	**Central frequency (MHz)**	**Bandwidth (MHz)**	**Channel attribute**
Low band	0	3494.4	499.2	Optional
	1	3993.6	499.2	Mandatory
	2	4492.8	499.2	Optional
High band	3	6489.6	499.2	Optional
	4	6988.8	499.2	Optional
	5	7488.0	499.2	Optional
	6	7987.2	499.2	Mandatory
	7	8486.4	499.2	Optional
	8	8985.6	499.2	Optional
	9	9484.8	499.2	Optional
	10	9984.0	499.2	Optional

Table A.1 — UWB Physical layer band plan [1]

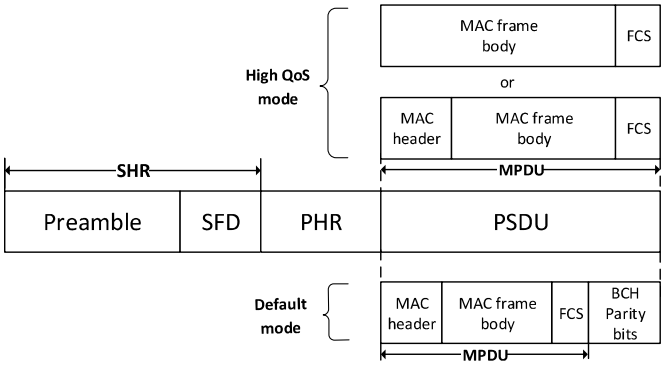


Figure A.1 — IR-UWB frame format (PPDU) [1]

eight in the high band (channels 3-10). All these channels are characterized by a bandwidth of 499.2 MHz. The channel 1 has a central frequency of 3993.6 MHz and is considered a mandatory channel for the low band, where channel 6 with a central frequency 7987.2 MHz is mandatory for the high band. All other channels are optional. An IR-UWB device shall supports at least one of the mandatory channels

A.2 Operation mode

The standard specifies two mode of operations: default mode and high quality of service (QoS) mode. The default mode is designated for medical and non-medical application, while the QoS mode is used for high-priority medical applications.

A.3 IR-UWB PHY Frame Format

The UWB PHY frame format or physical layer protocol data unit (PPDU) specified in the IEEE 802.15.6 standard [1] is illustrated in Figure A.1. It consists of a Synchronization header (SHR), a Physical-layer Header (PHR), and a Physical-layer Service Data Unit (PSDU). This latter represents the payload of the frame. The PHR contains information about the radio link as modulation, datarate, ...etc. The SHR consists of the preamble and the SFD. The preamble is used for timing synchronization, packet detection, and carrier frequency offset recovery, while the SFD is used for frame synchronization.

A.4 PSDU Construction

The PSDU content depends on the operation mode (Figure A.1). In the default mode, the PSDU consists of the MAC protocol data unit (MPDU) and Bose, Ray-Chaudhuri, Hocquenghem (BCH) channel code parity bits. In the high QoS mode, it contains either the MPDU or BCH parity bits. The MPDU consists of the MAC header, the MAC frame body, and the frame check sequence (FCS). To generate the PSDU for transmission, the MPDU data bits should be scrambled, block encoded, padded if needed, and interleaved as depicted in the Figure A.2

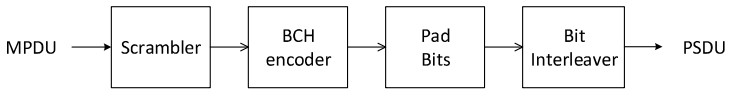


Figure A.2 — PSDU construction process [1]

A.4.1 Scrambling

The scrambler purpose is to eliminate possible long strings of '1's or '0's contained in the PHY payload, and so to eliminate the dependency of the signal's power spectrum upon the actual data (i.e. to randomise the data stream). For this reason, an additive or synchronous scrambler with generator polynomial $x[n]$ given below shall be employed ($\oplus$ denotes modulo-2 addition)

$$x[n] = x[n-2] \oplus x[n-12] \oplus x[n-13] \oplus x[n-14] \tag{A.1}$$

The scrambler shall be initialized accordingly to Table A.2

Scrambler seed (SS)	**Initialization vector** $x_{init} = x[-1]x[-2]...x[-14]$
0	0 0 1 0 1 1 1 1 0 0 1 1 0 1
1	0 0 0 0 0 0 0 1 0 0 1 1 1 1

Table A.2 — Scrambler seed selection [1]

A.4.2 Channel coding

The BCH channel code ($n = 63, k = 51$) shall be used for the default mode. Another BCH code $(126, 63)$ is defined for high QoS mode. The generator polynomial for the BCH encoder ($n = 63, k = 51$) is given below:

$$g(x) = 1 + x^3 + x^4 + x^5 + x^8 + x^{10} + x^{12} \tag{A.2}$$

Stuff bits need to be added to the last block of the frame to get an integer number of code blocks.

A.4.3 Interleaving

To provide robustness against error propagation, bit interleaving should be applied. The algebraic interleaver that should be used is defined as follows:

$$\Pi(n) = nb_s Mod N_I \tag{A.3}$$

where:
N_i is the interleaver length (shall be 192),
$\Pi(n)$ denotes the new position to which index n is permuted,

$ModN_i$ represents modulo N_i arithmetic,
b is the seeding parameter (shall be 37).

If the last block is shorter than the interleaver length, this latter should be shortened to the length of the last block.

A.5 PHR Construction

The PHR frame is composed of 24 bits designed to sum-up the content of the payload bits. In order to reach this goal, the PHR bits notably describe the following information (see Table A.3):

- Data Rate ($R_0 - R_2$): the first 3 bits of the PHR are dedicated to indicate the data rate of the payload bits, the pulse repetition frequency (PRF), the symbol length, the BCH coding rate, the pulse waveform duration and other modulation-related parameters (see Tables A.8 and A.9).
- Length of the MAC frame body ($L_7 - L_0$): 8 bits are used to indicate the frame length (0-255 bytes).
- Burst mode (B): one bit is used to indicate if the frame is a part of a burst or not.
- Pulse shaped (W_0 - W_1): indicates the used pulse shape among the three pulse shapes specified by the UWB-PHY: chirp pulse, chaotic pulse, and short pulse shapes.
- Hybrid Automatic Repeat request (HARQ[1]): 2 bits are used to indicates if HARQ is activated or not.
- Scrambler Seed (SS): selects the initial state of the scrambler registers among the two available initial states (see TableA.2).
- The on-off constellation mapper (K_m): indicates the symbol mapper of the On-Off modulation (see sub-setion (A.8)).

The PHR is protected against transmission errors by adding 4 bits of a CRC-4 ITU errors detection schemes, and 12 parity bits from short BCH (40,28) derived from BCH(63,51) code.

Bit																
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
R_0	R_1	R_2	r	L_0	L_1	L_2	L_3	L_4	L_5	L_6	L_7	r	r	B	W_0	W_1
Data rate				MAC frame body length											Pulse type	

17	18	19	20	21	22	23
H_0	H_1	SS	K_m	r	r	r
HARQ						

Table A.3 — PHR structure [1]

[1]HARQ is used to permit the repetition of the transmission of certain packets in case an error occurs during the transmission

A.6 SHR Construction

The preamble is constructed based on a Kasami sequence of length 63. The standard defines eight different Kasami sequences which are indexed by C_i for $i = 1, ..., 8$, presented in Table A.4. The set of sequences shall be divided into two pools, where each pool has a set of four preamble sequences. The first pool (C_1 to C_4) shall be used for odd numbers of physical channels. The second pool (C_5 to C_8) shall be used for even numbers of physical channels

C_1	1 1 1 1 1 1 0 1 0 1 0 1 1 0 0 1 1 0 1 1 1 0 1 1 0 1 0 0 1 0 0 1 1 1 0 0 0 1 0 1 1 1 1 0 0 1 0 1 0 0 0 1 1 0 0 0 0 1 0 0 0 0 0
C_2	0 0 0 1 1 0 0 0 1 0 0 1 0 0 1 0 0 0 1 0 1 1 0 0 0 1 1 0 0 1 1 1 1 0 0 1 1 0 0 1 0 1 0 1 1 1 0 0 0 1 1 0 1 0 1 0 1 0 1 0 0 1 0
C_3	1 0 0 0 1 1 1 1 1 1 0 1 1 1 1 0 0 0 1 1 1 0 0 0 0 1 1 0 1 1 1 1 0 1 1 1 0 1 0 1 1 1 0 1 1 1 0 0 1 1 0 1 0 0 0 0 1 0 0 1 1 0 0 1
C_4	0 1 0 0 0 1 0 0 0 0 1 0 1 0 1 1 0 1 0 1 1 1 1 1 0 1 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 0 1 0 1 1 0 0 1 0 1 1 0 1 0 0 0 1 0 0 1 1 1 1 1 0 0
C_5	1 0 1 0 0 0 0 1 1 1 1 0 0 0 0 0 0 1 1 0 0 1 0 0 1 1 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 0 1 1 1 0 0 1 0 0 0 1 1 0 1 1 0 0 0 0 0 1 1 1 0
C_6	1 1 0 1 0 0 1 1 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 1 1 1 0 1 1 0 0 1 0 0 0 0 0 0 0 0 1 0 1 1 1 0 1 0 0 0 1 1 1 1 0 1 1 0 1 1 1
C_7	0 1 1 0 1 0 1 0 0 1 1 1 0 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 0 0 0 0 1 0 1 1 0 1 1 1 0 0 0 0 0 0 0 0 1 1 0 1 0 0 1 1 1 1 0 1 0 1 1
C_8	0 0 1 1 0 1 1 0 1 1 0 0 1 1 1 0 1 0 0 1 0 1 0 1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 0 1 1 1 1 1 1 1 1 1 1 0 1 1 0 0 0 1 0 1

Table A.4 — Eight Kasami sequences used for preamble construction [1]

The preamble consists of $N_{sync} = 4$ repetitions of the symbol S_i. The symbol S_i is obtained by a Kasami sequence of Table A.4 zero-padded by $L-1$ zeros. It should be computed as shown below, where $\delta_L = (1, 0, ..., 0)_{1xL}$

$$S_i = C_i \otimes \delta_L \tag{A.4}$$

Figure A.3 illustrates the construction of symbol S_i, where the zero-padding period is LT_w and the pulse waveform duration is T_w. The standard specifies a duty cycle of 3% to be employed for the transmission of the synchronization symbol S_i. Hence, the values of T_w and L depend on the modulation employed.

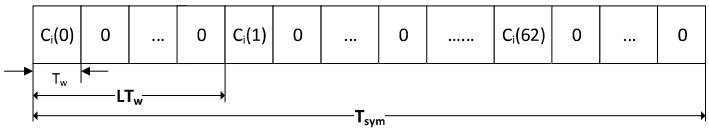


Figure A.3 — Construction of synchronization symbols from a Kasami sequence [1]

After the preamble, the SFD is formed based on the symbol $\bar{S}_i$. The symbol $\bar{S}_i$ represents an inversion of the i^{th} Kasami sequence bits ($0 \rightarrow 1, 1 \rightarrow 0$) in the symbol S_i of Equation (A.4). This choice allows to minimize the correlation between the two fields of the synchronization header (SHR) in order to improve the detection accuracy of the SFD.

A.7 Data symbol structure

The IR-UWB symbol structure is illustrated in Figure A.4. Each symbol time T_{sym} consists of an integer number N_w of pulse waveform positions, each of duration T_w (pulse waveform duration). These positions ($N_w - 1$ for DPSK modulation, and $(N_w/2) - 1$ for on-off modulation)

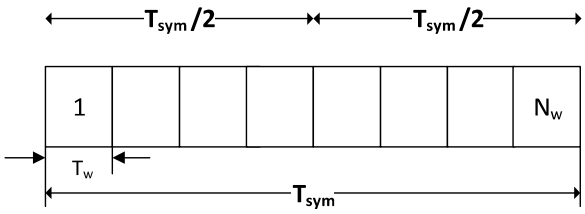


Figure A.4 — IR-UWB symbol structure [1]

are used for time hopping in order to support multi-BANs for coexistence. The symbol duration is divided into two intervals of duration $T_{sym}/2$ in order to enable on-off modulation. The duty cycle factor during a symbol time is given by the ratio $\eta = T_w/T_{sym}$. Such duty cycle shall be kept to 3.125% for every data rate and modulation type in order to maintain low power consumption and constant pulse power for a given PSD. A pulse waveform $w(t)$ of duration T_w can correspond to one of the two following options:

- A single pulse $p(t)$ of duration T_w
- A burst pulse of N_{cpb} pulses $p(t)$ of duration Tp with $T_w = NcpbTp$

In the burst pulse option, the standard requires the use of spectral shaping through scrambling in order to reduce spectral lines due to long strings of pulses with the same polarity.

Regarding the multi-BAN coexistence, the standard require the use of a time hopping (TH) as a multiple access scheme. TH is provided through an LFSR (also used for scrambling) that shall be clocked one time in case of single pulse option or shall be clocked N_{cpb} times in case of burst pulse option.

A.8 IR-UWB Modulation

Two modulation schemes are supported for the IR-UWB PHY, the On-Off modulation and Differentially encoded BPSK/QPSK (DBPSK/DQPSK).

A.8.1 On-Off modulation

On-Off signaling implies the use of a symbol mapper of size K. To a group of K information bits, the mapper associates a group of M = 2 x K symbols. Each device shall support a symbol mapper with K set to 1 that corresponds to M = 2. Thus, the transmitting symbol is given by the mapping indicated in Table A.5. Optionally, devices may support a symbol mapper with K set to 4 that corresponds to M = 2^4.

For the PHR as well as for the PSDU part of the frame, the pulse shaping shall place a pulse waveform according to the IR-UWB symbol structure. Thus, the transmitting signal corresponding to the m^{th} symbol shall be given by:

Data symbol decimal	**Data symbol binary** b_0	**Codeword** d_0, d_1
0	0	10
1	1	01

Table A.5 — Symbol mapper table for K = 1 [1]

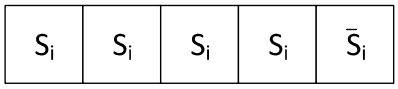


Figure A.5 — SHR structure [1]

$$x^m(t) = \begin{cases} \sum_{n=0}^{2k-1} d_n^m p(t - n(T_{sym}/2) - mkT_{sym} - h^{(2km+n)}T_w) & \text{Single pulse option} \\ \sum_{n=0}^{2k-1} d_n^m w_{2km+n}(t - n(T_{sym}/2) - mkT_{sym} - h^{(2km+n)}T_w) & \text{Burst pulse option} \end{cases} \tag{A.5}$$

where $m \geq 0$, d_n^m is the n^{th} codeword component over the m^{th} symbol, T_{sym} is the symbol time, $h(j)$ is the time-hopping sequence, and $w_n(t)$ is the burst of pulse waveform after scrambling.

In case of single pulse option, $T_w = T_p$, where T_p is the duration of $p(t)$. In case of burst pulse option, $T_w = N_{cpb}T_p$, where $N_{cpb} > 1$ and T_p is the duration of $p(t)$.

For the SHR and SFD part of the frame, data bit are not involved in symbol generation. Thus, the pulse shaping process operates as follows:

- The SHR symbol S_i uses OOK modulation with a zero-padding period of LT_w = 128 ns, according to the SHR symbol structure illustrated in Figure A.3. Every element of the i^{th} Kasami sequence $C_i(n)$ shall be transmitted with a pulse waveform of duration T_w = 8 ns, which corresponds to L = 16. For the burst pulse option, the static scrambling sequence corresponding to $N_{cpb} = 4$ is employed.
- The preamble consists of N_{sync} = 4 repetitions of the symbol S_i and the SFD consists of the symbol $\bar{S}_i$ as illustrated in Figure A.5.

A.8.2 Differentially encoded PSK modulation

In this type of modulation, The PPDU bits are differentially encoded such that the information is contained in the phase changes of consecutive PSK symbols. In such configuration, the DPSK transmitting symbols are given by:

$$c_m = c_{m-1}exp(j\phi_m). \tag{A.6}$$

where c_m represents the m^{th} DBPSK or DQPSK symbol, $m = (0, 1, ..., N)$, $c_{-1} = 1$ and ϕ_0 is an arbitrary phase. The symbol c_0 serves as phase reference to the differential encoding of the first bit (DBPSK) or first 2 bits (DQPSK).

The standard requires that the number of symbols shall be $N = P$ for the DBPSK modulation, where P is the number of bits in the PPDU $(g_0, ..., g_{P-1})$. For DQPSK, it requires that number of symbols shall be $N = [P/2]$, where P is the number of bits in the PHR plus PSDU $(g0, ..., g_{P-1})$.

The symbol c_m carries either one bit of information (DBPSK) that corresponds to M = 2 or two bits of information (DQPSK) that corresponds to M = 4. The mapping between information bits onto ϕ_m is given in Tables A.6 and A.7 respectively for DBPSK and DQPSK.

g_m	ϕ_{m+1}
0	0
1	π

Table A.6 — DBPSK mapping bit information [1]

g_{2m}	g_{2m+1}	ϕ_{m+1}
1	1	$\pi/2$
0	1	π
0	0	$-\pi/2$
1	0	0

Table A.7 — DBPSK mapping bit information [1]

For the PHR as well as for the PSDU part of the frame, after the generation of DBPSK/DQPSK symbols, the pulse shaping shall place a pulse waveform according to the UWB symbol structure. Thus, the transmitting signal is given as follows:

$$x(t) = \sum_{m=0}^{N} c_m w(t - mT_{sym} - h^{(m)}T_w) \tag{A.7}$$

- For the SHR and SFD part of the frame, data bits are not involved in symbol generation. Thus, the pulse shaping process operates as follow: the SHR symbol S_i uses DBPSK modulation with zero-padding period of LT_w = 256 ns, according to the SHR symbol structure illustrated in Figure A.3. Every bit of the i^{th} Kasami sequence $C_i(n)$ is transmitted with a pulse waveform of duration $T_w = 8$ ns, which corresponds to $L = 32$. In case of burst pulse option, the static scrambling sequence corresponding to $N_{cpb} = 4$ shall be employed.
- The preamble consists of N_{sync} = 4 repetitions of the symbol S_i and the SFD is made of the symbol $\bar{S}_i$ as described above.

A.9 IR-UWB timing parameters

The PSDU timing and data rate parameters are defined according to the standard in Table A.8 for On-Off modulation and in Table A.9 for phase modulation where:

- R0, R1, R2 refer to the data rate. For both modulations types, the mandatory data rate correspond to (R0,R1,R2) = (0,0,0)
- PRF is the Pulse Repetition Frequency.

R0,R1 R2	PRF (MHZ)	N_w	N_{hop}	T_w (ns)	T_{sym} (ns)	Uncoded bit rate (Mbps)	FEC rate	Coded Bit rate (Mbps)	N_{cpb}	Peak PRF (MHz)
0 0 0	0.4875	32	16	64.103	2051.3	0.4875	0.81	0.39487	32	499.2
0 0 1	0.975	32	16	32.051	1025.6	0.975	0.81	0.78975	16	499.2
0 1 0	1.95	32	16	16.026	512.82	1.95	0.81	1.5795	8	499.2
0 1 1	3.9	32	16	8.0128	256.41	3.9	0.81	3.159	4	499.2
1 0 0	7.8	32	16	4.0064	128.21	7.8	0.81	6.318	2	499.2
1 0 1	15.6	32	16	2.0032	64.103	15.6	0.81	12.636	1	499.2

Table A.8 — Data rates for on-off modulation [1]

R0,R1 R2	PRF (MHZ)	N_w	N_{hop}	T_w (ns)	T_{sym} (ns)	Mod	Uncoded bit rate (Mbps)	FEC rate	Coded Bit rate (Mbps)	N_{cpb}	Peak PRF (MHz)
0 0 0	0.487	32	32	64.103	2051.3	DBPSK	0.487	0.5	0.243	32	499.2
0 0 1	0.975	32	32	32.051	1025.6	DBPSK	0.975	0.5	0.457	16	499.2
0 1 0	1.95	32	32	16.026	512.82	DBPSK	1.950	0.5	0.975	8	499.2
0 1 1	3.9	32	32	8.0128	256.41	DBPSK	3.900	0.5	1.950	4	499.2
1 0 0	7.8	32	32	4.0064	128.21	DBPSK	7.800	0.5	3.900	2	499.2
1 0 1	7.8	32	32	4.0064	128.21	DQPSK	15.600	0.5	7.800	2	499.2
1 1 0	3.906	32	32	8.0128	1794.9	DBPSK	0.557	0.5	0.278	4	499.2
1 1 1	3.906	32	32	8.0128	1794.9	DQPSK	1.114	0.5	0.557	4	499.2

Table A.9 — Data rates for DBPSK/DQPSK modulations [1]

- N_w indicates a number of possible pulse waveform positions within a symbol time.
- N_{hop} is the number of pulse waveform positions that can contain an active pulse for time hopping.
- T_w is the pulse waveform duration.
- T_{sym} is the symbol duration.
- FEC rate is the channel coding rate that should be 0.81 in default mode and 0.5 in high QoS mode.
- N_{cpb} indicates the number of pulses that form a pulse waveform in burst option.

The standard enables to have variable data rates by alternating the symbol duration, the higher the data rate is, the shorter the symbol duration is. However, the number of pulses per symbol N_{cpb} (in burst option) and the duration of pulses T_w (in single pulse option) are adjusted depending on the data rate and modulation. For on-off modulation, N_{cpb} ranges from 1 to 32 and T_w from $\approx$ 2 ns to 64 ns for uncoded data rate that varies from 15.6 Mbps to 0.4875 Mbps. In case of DPSK modulation, the values of N_{cpb} and T_w range respectively from 2 to 32 and 4 ns to 64 ns for the same uncoded data rate that varies from 15.6 Mbps to 0.4875 Mbps.

In summary, the standard offers good scalability in terms of data rate, modulation, and operation mode. It also provides frequency bands compliant with the UWB communication regulatory authorities over the world divided in 11 operating frequency channels. These specifications offer to the designers a possibility to use either coherent or non-coherent architectures, to meet different tradeoffs between performance and complexity, and to address several applications with different constraints.

Résumé en français

Les dernières années ont vu un intérêt accru dans la recherche d'implémentations pratiques et efficaces de systèmes basés sur la radio impulsionnelle ultra large bande (IR-UWB). Cette technologie a été retenue récemment, en 2012, pour la nouvelle norme IEEE 802.15.6 dédiée aux réseaux Body Area Network (BAN), en particulier pour les communications entre objets à la surface ou à proximité du corps. Elle est apriori très attractive pour des objets nomades aux ressources énergétiques limitées, de par sa flexibilité en termes de débit, de complexité et de capacité à être économe en énergie. On peut cependant constater qu'il n'existe que peu d'implémentations réelles de systèmes UWB pour les BAN.

Ce travail de thèse apporte une contribution dans ce domaine. L'étude est centrée sur le traitement numérique en bande de base pour les récepteurs non-cohérents de faible complexité et porte d'abord sur la conception d'algorithmes de réception UWB pour les BAN puis sur leur implémentation matérielle efficace sur cible FPGA.

Dans un premier temps, une chaine de réception non-cohérente en bande de base complète a été proposée, testée, puis validée par simulation. Par la suite, une architecture matérielle de faible complexité a été conçue pour implémenter cette chaine puis l'intégrer dans une plateforme à base de circuit FPGA. Enfin, la faisabilité du système de communication complet a été confirmée par la réalisation d'expérimentations de transmissions réelles sans fil avec un démonstrateur matériel complet, confirmant ainsi la viabilité technique de l'approche retenue pour la mise en œuvre de la technologie IR-UWB pour les réseaux BAN.

La norme IEEE 802.15.6 pour les réseaux BAN

Le standard IEEE 802.15.6, publié en Février 2012, vise à établir une norme internationale qui permet d'adresser les besoins de systèmes de communications sans fil extrêmement fiables, à faible puissance énergétique et à courte portée à l'échelle du corps humain. Cette norme spécifie une large variété de débits de données pour différentes applications qui peuvent être médicales ou non médicales. Elle définit une couche de contrôle d'accès au support (MAC) et trois couches physiques (PHY) : (1) à bande étroite (NB: Narrowband) principalement pour des applications médicales en utilisant les différentes bandes disponibles sans licence, (2) à bande ultra large (UWB) en mesure d'adresser des débits de données importants et (3) une couche physique pour la communication au sein du corps humain (HBC: Human Body Communications). La sélection de chaque couche PHY dépend des exigences de l'application.

La technologie UWB, et en particulier la radio impulsionnelle IR-UWB qui est l'objet de ce travail de thèse, présente des avantages significatifs par rapport aux solutions basées sur la technologie de bande étroite pour adresser la large gamme d'applications BAN. Cette technologie est basée sur l'envoi de courtes impulsions dans le temps, répartissant ainsi l'énergie sur une large bande passante ($>$ 500 MHz) dans le domaine fréquentiel. Elle permet une grande robustesse en cas d'évanouissements à bande étroite, une protection contre les interférences en bande ISM (Industrial Scientific Medical), un débit binaire évolutif de 400 kbps à 12,6 Mbps avec le même matériel, une puissance rayonnée bien en dessous de -10 dBm et un potentiel important pour des implémentations de très faible consommation énergétique.

La spécification de la couche PHY UWB dans la norme IEEE 802.15.6 ouvre de nouvelles opportunités à la fois en termes d'implémentation et de performance de communication.

Projet de recherche RUBY

Dans le cadre du standard IEEE 802.15.6 pour les BAN, un projet de recherche national multi-partenaire nommé RUBY (Radio UWB for BodY area networks) a été lancé en 2012 pour une durée de trois ans. Ce projet, coordonné par Orange Labs, constitue le cadre principal des contributions proposées dans cette thèse. En plus d'Orange Labs, plusieurs partenaires académiques et industriels ont été impliqué dans le projet RUBY (CEA-Leti, Thales Communications & Security et les laboratoires CNRS IM2NP et LEAT).

RUBY avait pour ambition de développer un système de radio communication innovant basé sur la technologie IR-UWB et conçu pour les réseaux BAN. Le concept proposé dans ce projet consistait à disposer d'une architecture hybride combinant un récepteur cohérent et un récepteur non-cohérent afin de compenser les faiblesses de l'un par les forces de l'autre et vice versa. L'objectif est de permettre d'optimiser la consommation énergétique pendant la phase de synchronisation grâce à une détection non-cohérente et de bénéficier de la grande sensibilité du récepteur cohérent durant la phase de démodulation des données. En effet, comme la structure de la trame spécifiée dans la norme IEEE 802.15.6 adopte un préambule très court, la synchronisation ne peut pas être acquise par une recherche série-parallèle telle que effectuée avec un récepteur cohérent avec un convertisseur analogique-numérique basse fréquence, qui nécessite un long préambule. D'autre part, la structure du récepteur non-cohérent fournit un échantillonnage rapide ($<$ 2ns) du signal reçu. Ainsi, la capture d'une réponse impulsionnelle de canal (CIR) complète est possible avec un seul symbole de préambule, permettant ainsi l'acquisition rapide de la synchronisation et de l'estimation du canal.

En pratique, l'architecture hybride ciblée effectue d'abord la détection de préambule, la synchronisation et une estimation initiale du canal dans un temps très court en utilisant un front-end non-cohérent qui implique une complexité réduite et une faible consommation énergétique, puis elle passe au front-end cohérent qui a une plus grande sensibilité pour affiner l'estimation du canal et effectuer une démodulation de donnée à haut débit.

En effet, le projet RUBY vise à concevoir un system de communication IR-UWB complet, en intégrant tous les composants analogiques et numériques. Cela comprend un circuit de radio fréquence (RF) pour le front-end hybride (cohérent et non-cohérent), un convertisseur analogique-numérique très contraint, une bande de base numérique qui sera en mesure de

contrôler le nouveau front-end et de traiter les données reçues efficacement et une antenne UWB miniature conçue pour être utilisée dans le voisinage immédiat d'un corps humain. Le circuit RF et la bande de base numérique conçus durant ce projet sont prévus pour être intégrés dans un véritable prototype matériel afin de mettre en œuvre une démonstration réelle pour la preuve du concept.

Dans ce contexte, la synchronisation est une tâche très difficile à accomplir. Cela est vrai dans tout système de communication, et en particulier dans les systèmes IR-UWB. En fait, les impulsions extrêmement étroites et de faible puissance énergétique d'un signal IR-UWB nécessitent une synchronisation très précise dans le temps, car même un léger défaut d'alignement (manque de capture d'énergie) peut dégrader sévèrement les performances du système.

En outre, la très grande bande passante dont disposent les signaux IR-UWB permet la séparation et la caractérisation d'un grand nombre d'échos ou « trajets » (haute résolution de puissance) à cause du phénomène de propagation multi-trajets. L'exploitation de ces échos offre un gain de diversité et améliore donc les performances du récepteur. Tout comme la synchronisation, avoir une estimation de canal précise peut être une tâche assez complexe dans un système IR-UWB.

Travaux antérieurs à Orange Labs

Plusieurs activités de recherche ont été menées à Orange Labs sur le thème des systèmes de communication IR-UWB. La thèse de Jean Schwoerer (années 2002 à 2006) a été la première initiative dans ce contexte. L'objectif était de spécifier une couche PHY IR-UWB dans un contexte d'applications nécessitant un débit faible et d'étudier les problèmes de synchronisation et de détection du signal. Les travaux de cette thèse ont aboutis à la proposition : (1) d'un récepteur non-cohérent très faible complexité basé sur la détection d'énergie sur un temps très court temps et (2) un algorithme original pour acquérir la synchronisation entre l'émetteur et le récepteur. Tout d'abord, le récepteur proposé se base sur la comparaison entre l'énergie captée pendant un temps d'impulsion (¡ 2ns) et un seuil préfixé pour décider de la présence ou de l'absence de signal de manière asynchrone. D'autre part, l'algorithme de synchronisation proposée exploite une structure de préambule spécifique composée de symboles non modulés. L'idée est basée sur la comparaison entre les temps d'arrivée des impulsions reçues et les distances temporelles dans le symbole de préambule.

Cette activité de recherche a été poursuivie ensuite par le travail de thèse de Jérémy Hamon (années 2006 à 2009) pour étudier l'utilisation de la logique asynchrone dans la mise en œuvre de l'algorithme de synchronisation proposé. L'idée était, d'une part de s'adapter avec l'aspect asynchrone du récepteur non-cohérent précité, et d'autre part de diminuer la consommation énergétique dynamique grâce à la caractéristique intrinsèque de la logique asynchrone. De plus, l'absence du signal d'horloge dans les circuits asynchrones permet de réduire le bruit électromagnétique, ce qui est bénéfique lors du traitement de signaux de faible puissance comme ceux de l'IR-UWB. La base de temps nécessaire pour traiter les signaux IR-UWB a été assurée en utilisant des structures asynchrones rebouclées, appelées *anneaux asynchrones*.

Dans la même période, un autre travail de thèse (Benoît Miscopein, années 2007 à 2010) a été

lancé pour améliorer les performances du récepteur non-cohérent IR-UWB précité. L'idée était d'exploiter la diversité multi-trajet du canal UWB dans la démodulation des signaux modulés en tout-ou-rien (OOK). La méthode proposée repose sur la fusion et la recombinaison des différents trajets en calculant leur somme pondéré par leur fiabilité. Les résultats obtenus illustrent une amélioration significative et la possibilité d'atteindre un niveau de performance proche du récepteur optimal.

En effet, le récepteur non-cohérent proposé dans les travaux antérieurs à Orange Labs est utilisé pour concevoir le front-end non-cohérent dans le projet RUBY. Cependant, l'algorithme de synchronisation déjà proposé n'est pas applicable car il est basé sur une structure de préambule spécifique qui n'est pas conforme à celui défini dans la norme IEEE 802.15.6. Par conséquent, des adaptations spécifiques devraient être proposées.

De même, afin de compléter la chaîne de réception non-cohérente, un algorithme de démodulation supportant la modulation en position d'impulsions (PPM) spécifiée dans la norme est requis. À cet égard, l'utilisation du traitement multi-trajet par pondération a montré son efficacité dans la thèse de Benoît Miscopein. Cependant, une approche pratique à faible complexité pour calculer les coefficients de pondération est encore manquante et nécessite de nouvelles investigations.

Enfin, la proposition d'architectures de traitement numérique en bande de base à faible complexité qui mettent en œuvre efficacement les nouvelles techniques de réception non-cohérente conformes à la norme constitue une exigence cruciale pour construire une preuve de concept matérielle complète. La littérature disponible à cet égard est plutôt rare. Cet objectif de validation est très précieux pour démontrer la faisabilité des systèmes IR-UWB dans des conditions réelles de canal, telles que rencontrées dans les applications de réseaux BAN.

Objectifs et portée de la thèse

Dans le contexte décrit ci-dessus, ce travail de thèse vise à proposer, implémenter, puis valider par simulation et par des expérimentations matérielles un ensemble d'algorithmes de réception non-cohérente compatibles avec la norme IEEE 802.15.6 afin d'en faire une preuve de concept.

Dans le contexte du projet RUBY visant une architecture de réception hybride cohérente/non-cohérente, le premier objective de ce travail de thèse est de proposer un algorithme de synchronisation assez flexible et rapide pour pouvoir adresser tous les préambules spécifiés par la norme. Puis, le deuxième objective est de proposer une technique d'estimation de canal afin de fournir la réponse impulsionnelle du canal au récepteur cohérent. Le reste du traitement numérique (détection de symboles et démodulation) est effectué par la partie cohérente dans le cadre du projet RUBY visant des applications BAN à haut débit. Cette partie est hors de la portée de cette thèse.

Cependant, dans le cas d'applications à bas débit, il peut être envisageable d'utiliser uniquement la partie non-cohérente du récepteur et d'éteindre la partie cohérente ce qui va permettre un gain considérable en terme de consommation énergétique. Cela toutefois nécessite de compléter la chaine de réception non-cohérente en proposant un algorithme de démodulation ainsi qu'une technique de détection du délimiteur de début de trame (SFD). Le SFD est utilisé pour déterminer

le début du champ de données dans la trame de la norme IEEE 802.15.6. Cette approche constitue un objectif additionnel que nous avons décidé d'explorer dans ce travail de thèse, au-delà des objectifs du projet RUBY.

Finalement, l'un des principaux objectifs de ce travail est de proposer et de mettre en œuvre une architecture matérielle à complexité réduite capable d'implémenter efficacement les algorithmes proposés. L'objectif ultime étant de construire un démonstrateur matériel temps-réel complet qui implémente un récepteur IR-UWB non-cohérent et qui gère l'interconnexion entre ce récepteur non-cohérent et le récepteur cohérent combiné.

Contributions

Par rapport aux objectifs mentionnés ci-dessus, les contributions de ce travail de thèse peuvent être résumées dans le domaine algorithmique et dans le domaine des implémentations matérielles comme suivant:

Contributions dans le domaine algorithmique

Dans le domaine algorithmique, plusieurs techniques de réception non-cohérente ont été proposées pour des applications de réseaux BAN:

- Proposition et conception d'une technique de synchronisation rapide et flexible qui cible la norme IEEE 802.15.6, avec la possibilité de supporter d'autres préambules.
- Proposition d'une technique simple de détection de délimiteur de début de trame (SFD) qui peut, en plus de détecter le début du champ de données, estimer la probabilité d'erreur du signal reçu. Cette technique permet d'avoir une métrique alternative à la mesure de l'énergie du signal que le système ne peut pas estimer.
- Proposition d'un estimateur non-cohérent de la réponse impulsionnelle du canal qui est utilisé à la fois pour détecter les composants de trajets multiples et pour estimer de leurs fiabilités.
- Proposition d'un algorithme de décision par fusion qui prend en charge la modulation PPM.
- Test et validation de l'ensemble du traitement non-cohérent en bande de base à travers des simulations du système en utilisant les modèles de canaux de communication de la norme IEEE 802.15.6.

Contributions dans le domaine des implémentations matérielles

Dans le domaine des implémentations matérielles, plusieurs contributions ont été proposées :

- Proposition et conception d'architectures de faible complexité qui mettent en œuvre les techniques de synchronisation et de détection de SFD proposées.

- Proposition et conception d'une architecture parallèle optimisée qui implémente l'estimateur de canal proposé.
- Proposition et conception d'une architecture à faible complexité qui met en œuvre la technique de décision par fusion proposée.
- Intégration et validation sur carte des architectures de synchronisation et d'estimation de canal proposées dans un démonstrateur matériel temps-réel complet du système IR-UWB compatible avec la norme IEEE 802.15.6. Des expériences et des mesures réussies ont été menées avec des transmissions sans fil et des conditions réelles de canal de transmission.

Structure du manuscrit de thèse et résumé des chapitres

Le manuscrit de thèse est composé de quatre chapitres comme suit:

Chapitre 1

Le premier chapitre donne un aperçu sur la technologie UWB et sur son évolution au fil du temps, ainsi qu'un aperçu des principaux concepts et architectures de systèmes de communication IR-UWB. Le chapitre commence par une présentation des principes, des caractéristiques et des applications de ces systèmes ainsi que de l'évolution de la régulation et de la normalisation. Après cette introduction, un état de l'art sur les techniques actuelles pour le traitement en bande de base est présenté. Ces techniques concernent aussi bien l'émetteur que le récepteur des liens radio UWB, et servent de base pour positionner et présenter les contributions de cette thèse. Afin de fournir une introduction complète aux travaux décrits dans cette thèse, le chapitre présente ensuite la couche physique UWB comme spécifié dans le projet RUBY, ainsi que les différents cas d'utilisation définis dans ce projet. Le chapitre se termine par une description des principaux modèles de canaux UWB, tels que spécifiés dans les normes IEEE 802.15.4a et IEEE 802.15.6.

Chapitre 2

Le deuxième chapitre présente les différentes contributions de la thèse dans le domaine algorithmique. Dans ce contexte, plusieurs techniques de réception non-cohérente ont été proposées pour des applications de réseaux BAN. Le chapitre présente d'abord un algorithme flexible et efficace de synchronisation basé sur la détection d'intervalles de temps entre les impulsions. Ensuite, une technique de détection de SFD qui repose sur une méthode de corrélation est présentée. En plus de la détection du début du champ de données dans la trame, la technique proposée permet d'estimer la probabilité d'erreur du signal reçu. Par ailleurs, un estimateur de canal efficace est proposé et utilisé à la fois pour détecter les composants de trajets multiples et pour estimer leurs fiabilités en exploitant la résolution du récepteur non-cohérent adopté. Enfin, le chapitre présente un algorithme de décision par fusion basé sur le traitement multi-trajets et qui support une modulation de type PPM. Les performances réalisées de chaque algorithme proposé sont évaluées de façon indépendante, puis l'ensemble de la bande de base non-cohérente est simulée en utilisant les modèles de canaux spécifiés dans la norme IEEE 802.15.6.

Chapitre 3

Le troisième chapitre présente les contributions de thèse liées à la conception d'architectures matérielles de traitement numérique en bande de base pour un récepteur IR-UWB non-cohérent. Le chapitre regroupe les différentes architectures de faible complexité proposées qui mettent en œuvre les algorithmes présentés dans le chapitre précédent, à savoir la synchronisation, la détection SFD, l'estimateur de canal et l'algorithme de décision par fusion basé sur un traitement multi-trajets. Le chapitre commence par présenter l'architecture générale du système et les différentes connexions entre ses différents constituants. Ensuite, pour chaque architecture proposée une description détaillée est fournie. La première étape est la dé-sérialisation des données d'entrée pour réduire le rythme des données à traiter. La seconde étape est la synchronisation et l'estimation de la réponse impulsionnelle du canal. La dernière étape est la détection des données. Pour chacun de ces blocs de traitement, une description détaillée de l'architecture proposée est fournie en termes de signaux d'entrée/sortie, de différents composants constituants et de l'unité de contrôle basée sur une machine à états finis qui ordonnance toutes les opérations. Le chapitre présente en plus la conception d'un convertisseur série-parallèle pour gérer le flux de haut débit des données d'entrée, avec une unité de contrôle global pour ordonnancer les opérations. Le chapitre se termine par la présentation des résultats de synthèse logique en termes de ressources matérielles utilisées qui illustrent l'efficacité matérielle des architectures proposées.

Chapitre 4

Le quatrième chapitre présente la dernière majeure contribution de ce travail de thèse concernant le prototypage sur FPGA et l'intégration des architectures proposées dans une véritable plateforme de démonstration matérielle. Cette plateforme de démonstration a été développée dans le cadre du projet de recherche RUBY. Elle se compose d'une carte à base de circuit FPGA qui intègre les architectures proposées décrites dans les chapitres précédents, une carte de radio fréquence mettant en œuvre le front-end analogique et une carte d'application basée sur un microcontrôleur. Le chapitre présente d'abord le contexte et l'architecture générale de la plateforme de démonstration matérielle proposée. Ensuite, une description détaillée des différentes cartes intégrées et de l'environnement de test est fournie. Enfin, les résultats de performance mesurés avec des transmissions sans fil et des canaux de propagation réels sont présentés et discutés.

Conclusion

Le manuscrit se termine par un chapitre de conclusions et de perspectives qui récapitule les résultats obtenus et les contributions proposées et fournit quelques perspectives à ce travail de recherche.

Ce travail de thèse a étudié la conception d'un récepteur non-cohérent IR-UWB avec un traitement numérique en bande de base de faible complexité, supportant les spécifications de la norme IEEE 802.15.6 pour les applications de type BAN. Le contexte principal concerne le projet de recherche collaboratif RUBY qui vise la proposition d'une architecture hybride qui

combine un récepteur cohérent et un récepteur non-cohérent afin de compenser les faiblesses de l'un par les forces de l'autre et vice versa. Plusieurs contributions ont été proposées dans le domaine algorithmique et dans le domaine de la conception d'architectures matérielles associées. Dans le domaine algorithmique, les contributions portent essentiellement sur les algorithmes de synchronisation, sur une technique d'estimation non cohérente de la réponse impulsionnelle du canal et sur un algorithme de type Rake non-cohérent pour la détection (décision par fusion de multi-trajets). Dans le domaine de l'implémentation matérielle, des architectures originales de faible complexité ont été proposées pour mettre en œuvre les algorithmes proposés. Ces architectures numériques ont également été conçues pour être flexible pour permettre leur utilisation avec tout type de front-end non-cohérent fournissant un flux de bits qui correspond à la détection ou non du signal reçu. Enfin, la validation sur carte FPGA a été intégrée dans un prototype système comprenant un front-end RF et une carte d'application à base de microcontrôleur. Plusieurs expériences réussies ont été menées avec différentes conditions de canal de transmission en vue directe (LOS) et non directe (NLOS). Les signaux internes du circuit FPGA intégrant les architectures proposées ont été sondés et visualisés en utilisant un analyseur logique intégré au FPGA (Xilinx ChipScope logic analyzer). Les résultats mesurés ont illustré l'acquisition rapide de la synchronisation et l'efficacité de l'estimateur de canal en utilisant le récepteur non-cohérent proposé à faible complexité. Ces résultats ont été confirmés par la partie cohérente de l'architecture hybride par la détection du SFD et la collection d'énergie dans les fenêtres correspondant aux positions des trajets identifiés. La réponse impulsionnelle du canal a été également mesurée dans les expériences menées à l'aide du récepteur cohérent afin d'analyser et de valider les résultats de démonstration.

Enfin, le prototypage matériel est une tâche complexe dans le contexte des systèmes IR-UWB où l'adoption d'impulsions très étroites dans le temps exige une précision très haute et implique un renforcement des contraintes dans la conception, l'intégration et les expérimentations de test. Cependant, il reste une étape cruciale pour valider tous les algorithmes et les architectures proposés dans des conditions de canaux réels. Dans ce contexte, le prototype matériel développé constitue une preuve de concept précieuse des algorithmes et architectures proposés et les résultats obtenus constituent une référence dans ce domaine où la littérature est plutôt rare

Glossary

3GPP	3rd Generation Partnership Project
AC	Absolute Combiner
ADC	Analog-to-Digital Converter
ADSL	Asymmetric Digital Subscriber Line
ASIC	Application Specific Integrated Circuit
AWGN	Additive White Gaussian Noise
BAN	Body Area Network
BCH	Bose, Ray-Chaudhuri, Hocquenghem code
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CFAR	Constant False Alarm Rate
CIR	Channel Impulse Response
CMOS	Complementary Metal Oxide Semiconductor
CRC	Header Check Sequences
DAA	Detect And Avoid
DBB	Digital BaseBand
DBPSK	Differential (or differentially encoded) Binary Phase-Shift Keying
DCM	Digital Clock Management
DDR	Double Data Rate
DS	Direct Sequence
DSP	Digital Signal Processor
DPSK	Differential Phase-Shift Keying
DQPSK	Differential (or differentially encoded) Quadrature Phase-Shift Keying
DVB	Digital Video Broadcasting
ECG	ElectroCardioGraphy
EEC	European Communications Commision
EGC	Equal Gain Combining
EMG	ElectroMyoGraphy

FCC	Federal Communication Commission
FCS	Frame Check Sequence
FDMA	Frequency Division Multiple Access
FEC	Forward Error Correction
FF	Flip-Flop
FH	Frequency Hopping
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GPS	Global Positioning Satellite System
HARQ	Hybrid Automatic Repeat request
IEEE	Institute of Electrical and Electronic Engineers
IR	Impulse Radio
ISI	Inter Symbol Interference
LAN	Local Area Network
LDC	Low Duty Cycle
LFSR	Linear Feedback Shift Register
LNA	Low-Noise Amplifier
LO	Local Oscillator
LOS	Line-of-Sight
LS	Least Squares
LUT	Look-Up Table
LVDS	Low Voltage Differential Signaling
MAC	Medium Access Control
MAN	Metropolitan area network
MB	Multi-Band
MIC	Internal Affairs and Communications
ML	maximum-likelihood
MPC	Multi-Path Components
MPDU	MAC Protocol Data Unit
MRC	Maximum Ratio Combining
NLOS	Non Line-Of-Sight
OFDM	Orthogonal Frequency Division Multiplexing
OOK	On-Off Keying
PA	Power Amplifier
PAM	Pulse Amplitude Modulation
PDP	Power Delay Profile
PER	Packet Error Rate

PHR	Physical-layer Header
PHY	Physical layer
PL	Path-Loss
PLL	Phase-Locked Loop
PPDU	Physical layer Protocol Data Unit
PPM	Pulse Position Modulation
PRF	Pulse Repetition Frequency
PRP	Pulse Repetition Period
PSD	Power Spectral Density
PSDU	Physical-layer Service Data Unit
PSK	Phase Shift Keying
PVT	Process, Voltage, and Temperature
PXI	PCI eXtensions for Instrumentation
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RUBY	Radio UWB for BodY area network
SERDES	SERializer/DESerializer
SFD	Start-of-Frame Delimiter
SHR	Synchronization Header
SiP	System in Package
SMA	Sub-Miniature version A
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TDMA	Time Division Multiple access
TH	Time Hopping
UART	Universal Asynchronous Receiver Transmitter
UFZ	UWB Friendly Zone
UMTS	Universal Mobile Telecommunications System
UWB	Ultra WideBand
VHDL	VHSIC Hardware Description Language
WPAN	Wirless Personal Area Networks

Bibliography

[1] *Part 15.6: Wireless Body Area Networks*, IEEE Standard for Local and metropolitan area networks Std., 29 February 2012.

[2] K. Y. Yazdandoost, K. Sayrafian-Pour *et al.*, "Channel model for body area network (BAN)," *IEEE P802*, vol. 15, 2009.

[3] S. Drude, "Requirements and Application Scenarios for Body Area Networks," in *Mobile and Wireless Communications Summit, 2007. 16th IST*, 1-5 July 2007.

[4] L. Ouvry, G. Masson, M. Pezzin, B. Piaget, B. Caillat, S. Bourdel, N. Dehaese, O. Fourquin, J. Gaubert, S. Meillere *et al.*, "A 4GHz CMOS 130 nm IR-UWB dual front-end transceiver for IEEE802. 15 standards," in *Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on*. IEEE, 2014, pp. 798–801.

[5] B. Miscopein and J. Schwoerer, "Low Complexity Synchronization Algorithm for Non-Coherent UWB-IR Receivers," in *Proc. of the IEEE 65th Vehicular Technology Conference (VTC2007-Spring)*, April 2007, pp. 2344–2348.

[6] J. Schwoerer, "Études et implémentation d'une couche physique UWB impulsionnelle à bas débit et faible complexité," Ph.D. dissertation, Institut National des Science Appliquees INSA-Rennes, 2006.

[7] J. Hamon, "Oscillateurs et architectures asynchrones pour le traitement des signaux radio impulsionnelle UWB," Ph.D. dissertation, Institut National Polytechnique de Grenoble-INPG, 2009.

[8] B. Miscopein, "Systemes UWB impulsionnels non cohérents pour les réseaux de capteurs: coexistence et coopération," Ph.D. dissertation, INSA de Lyon, 2010.

[9] T. W. Barrett, "History of ultrawideband (UWB) radar & communications: pioneers and innovators," in *Proc. Progress in Electromagnetics Symposium*, 2000, pp. 1–42.

[10] R. Scholtz, "Multiple access with time-hopping impulse modulation," in *Milcom*, vol. 93, no. 1993.2. Citeseer, 1993, pp. 447–450.

[11] F. C. Commission *et al.*, "Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems," *First Report and Order*, pp. 02–48, 2002.

[12] Y. Rahayu, T. A. Rahman, R. Ngah, and P. Hall, "Ultra wideband technology and its applications," in *Wireless and Optical Communications Networks, 2008. WOCN'08. 5th IFIP International Conference on*. IEEE, 2008, pp. 1–5.

[13] J. R. Fernandes and D. Wentzloff, "Recent advances in IR-UWB transceivers: An overview," in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*. IEEE, 2010, pp. 3284–3287.

[14] S. Sadough, A. Mahmood, E. Jaffrot, and P. Duhamel, "Multiband–OFDM: A new physical layer proposal for ultra wideband communications," *Journal of Iranian Association of Electrical and Electronics Engineers (IAEEE)*, 2007.

[15] M. Z. Win, R. A. Scholtz *et al.*, "On the robustness of ultra-wide bandwidth signals in dense multipath environments," *IEEE Communications Letters*, vol. 2, no. 2, pp. 51–53, 1998.

[16] C. Nguyen and J. Han, *Time-Domain Ultra-Wideband Radar, Sensor and Components: Theory, Analysis and Design*. Springer Science & Business Media, 2014.

[17] Alereon company, "Alereon's AL5350 MAC/BBP," http://www.alereon.com, 2004.

[18] pulselink company, "pulselink's PL3120 Ultra-Wideband Transceiver," http://www.pulselink.com, 2014.

[19] decawave company, "decawave's DW1000," http://www.decawave.com, 2013.

[20] Time Domain company, "Time Domain's PulsON 330/440," http://www.timedomain.com, 2015.

[21] bespoon company, "bespoon's UPosition IR-UWB Module," http://www.bespoon.com, 2013.

[22] M. Z. Win and R. A. Scholtz, "Impulse radio: How it works," *IEEE communications letters*, vol. 2, no. 2, pp. 36–38, 1998.

[23] F. Delong, H. Lu, C. Li, and L. Fujiang, "A 3–5 GHz BPSK transmitter for IR-UWB in 0.18 μm CMOS," *Journal of Semiconductors*, vol. 31, no. 9, p. 095005, 2010.

[24] F. Ramirez-Mireles, R. Scholtz *et al.*, "Multiple-access performance limits with time hopping and pulse position modulation," in *Military Communications Conference, 1998. MILCOM 98. Proceedings., IEEE*, vol. 2. IEEE, 1998, pp. 529–533.

[25] O. Abedi and M. C. Yagoub, "Performance Comparison of UWB Pulse Modulation Schemes under White Gaussian Noise Channels," *International Journal of Microwave Science and Technology*, vol. 2012, 2012.

[26] J. Perez-Duenas, J. G. Wanguemert-Perez, and I. Molina-Fernandez, "Novel modulation scheme and six-port based RAKE receiver for DS-UWB," *Wireless Communications, IEEE Transactions on*, vol. 8, no. 7, pp. 3628–3633, 2009.

[27] M. Herceg, T. Švedek, and T. Matić, "Pulse interval modulation for ultra-high speed IR-UWB communications systems," *EURASIP Journal on Advances in Signal Processing*, vol. 2010, p. 48, 2010.

[28] S. Ji, S. Lee, and J. Kim, "Efficient hybrid modulation with phase-directed pulse position estimation for UWB-IR systems," *Communications, IEEE Transactions on*, vol. 61, no. 3, pp. 1171–1177, 2013.

[29] J. Foserter, "The performance of a direct sequence spread spectrum ultra-wide band system in the presence of multipath, narrow band, interference and multi user interference," in *IEEE. Conference on Ultra Wide Band Systems Technologies*, 2002, pp. 2246–2255.

[30] R. De Lacerda, A. Hayar, and M. Debbah, "Channel division multiple access: The access solution for UWB networks," in *Ultra-WideBand (ICUWB), 2014 IEEE International Conference on*. IEEE, 2014, pp. 309–314.

[31] A.-L. Deleuze, C. J. Le Martret, and P. Cibla, "Time-hopping code characterization for multiuser interference mitigation in ultra wide band impulse radio," in *Signals, Systems and Computers, 2004. Conference Record of the Thirty-Eighth Asilomar Conference on*, vol. 1. IEEE, 2004, pp. 617–621.

[32] D. J. Young and N. C. Beaulieu, "Multiuser interference mitigation in time-hopped ultra-wideband Receivers," in *Ultra-Wideband (ICUWB), 2012 IEEE International Conference on*. IEEE, 2012, pp. 125–129.

[33] M. K. Simon, J. K. Omura, R. A. Scholtz, and B. K. Levitt, *Spread spectrum communications handbook*. Citeseer, 1994, vol. 2.

[34] R. Roberts, "XtremeSpectrum CFP document," *IEEE P802*, vol. 15, pp. 15–03, 2003.

[35] Y. Issa, "Contributions to cooperative dIversity in multiple access UWB systems," Ph.D. dissertation, Université de Valenciennes et du Hainaut-Cambresis, 2013.

[36] D. D. Wentzloff and A. P. Chandrakasan, "Gaussian pulse generators for subbanded ultra-wideband transmitters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 4, pp. 1647–1655, 2006.

[37] P. K. Datta, X. Fan, and G. Fischer, "A transceiver front-end for ultra-wide-band applications," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 54, no. 4, pp. 362–366, 2007.

[38] D. Barras, G. Von Bueren, W. Hirt, and H. Jaeckel, "A multi-modulation low-power FCC/EC-compliant IR-UWB RF transmitter in 0.18-μm CMOS," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, 2009.

[39] D. Barras, F. Ellinger, H. Jäckel, and W. Hirt, "Low-power ultra-wideband wavelets generator with fast start-up circuit," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 5, pp. 2138–2145, 2006.

[40] J. R. Fernandes, H. B. Gonçalves, L. B. Oliveira, and M. M. Silva, "A pulse generator for UWB-IR based on a relaxation oscillator," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 3, pp. 239–243, 2008.

[41] A. T. Phan, J. Lee, V. Krizhanovskii, Q. Le, S.-K. Han, and S.-G. Lee, "Energy-efficient low-complexity CMOS pulse generator for multiband UWB impulse radio," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 55, no. 11, pp. 3552–3563, 2008.

[42] S. Diao, Y. Zheng, and C.-H. Heng, "A CMOS ultra low-power and highly efficient UWB-IR transmitter for WPAN applications," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 56, no. 3, pp. 200–204, 2009.

[43] J. Lee, Y.-J. Park, M. Kim, C. Yoon, J. Kim, and K.-H. Kim, "System-on-package ultra-wideband transmitter using CMOS impulse generator," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 4, pp. 1667–1674, 2006.

[44] S. Bourdel, J. Gaubert, M. Battista, Y. Bachelet, and G. Bas, "CMOS UWB transceiver for impulse radio," in *Ultra-Wideband, 2007. ICUWB 2007. IEEE International Conference on*. IEEE, 2007, pp. 188–193.

[45] L. Smaïni, C. Tinella, D. Hélal, C. Stoecklin, L. Chabert, C. Devaucelle, R. Cattenoz, N. Rinaldi, and D. Belot, "Single-chip CMOS pulse generator for UWB systems," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 7, pp. 1551–1561, 2006.

[46] D. D. Wentzloff and A. P. Chandrakasan, "A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS," in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Feb 2007, pp. 118–591.

[47] S. Bourdel, R. Vauché, and J. Gaubert, "Pulse generator design," *Ultra Wideband*, pp. 137–158, 2010.

[48] H. Kim, D. Park, and Y. Joo, "All-digital low-power CMOS pulse generator for UWB system," *Electronics Letters*, vol. 40, no. 24, pp. 1534–1535, 2004.

[49] T. Norimatsu, R. Fujiwara, M. Kokubo, M. Miyazaki, A. Maeki, Y. Ogata, S. Kobayashi, N. Koshizuka, and K. Sakamura, "A UWB-IR transmitter with digitally controlled pulse generator," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 6, pp. 1300–1309, 2007.

[50] R. Vauche, S. Bourdel, N. Dehaese, O. Fourquin, and J. Gaubert, "Fully tunable UWB pulse generator with zero DC power consumption," in *Ultra-Wideband, 2009. ICUWB 2009. IEEE International Conference on*. IEEE, 2009, pp. 418–422.

[51] J. Radić, A. Djugova, L. Nagy, and M. Videnović-Misić, "A Low-Complexity and Energy-Efficient IR-UWB Pulse Generator in 0.18 μm technology," *Electronic Components and Materials*, vol. 43, no. 3, pp. 179–184, 2013.

[52] J. Hu, Y. Zhu, S. Wang, and H. Wu, "Energy efficient, reconfigurable, distributed pulse generation and detection in UWB impulse radios," in *Ultra-Wideband, 2009. ICUWB 2009. IEEE International Conference on*. IEEE, 2009, pp. 773–777.

[53] N. Van Helleputte and G. Gielen, "A 70 pJ/pulse analog front-end in 130 nm CMOS for UWB impulse radio receivers," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 7, pp. 1862–1871, 2009.

[54] M. Verhelst, N. Van Helleputte, G. Gielen, and W. Dehaene, "A reconfigurable, 0.13μm CMOS 110pJ/pulse, fully integrated IR-UWB receiver for communication and sub-cm ranging," in *Solid-State Circuits Conference-Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*. IEEE, 2009, pp. 250–251.

[55] S. Dubouloz, B. Denis, S. de Rivaz, and L. Ouvry, "Performance analysis of LDR UWB non-coherent receivers in multipath environments," in *Ultra-Wideband, 2005. ICU 2005. 2005 IEEE International Conference on*. IEEE, 2005, pp. 6–pp.

[56] D. D. Wentzloffe, F. S. Lee, D. C. Daly, M. Bhardwaj, P. P. Mercier, and A. P. Chandrakasan, "Energy Efficient Pulsed-UWB CMOS Circuits and Systems," in *Ultra-Wideband, 2007. ICUWB 2007. IEEE International Conference on*, 24-26 Sept. 2007, pp. 282 – 287.

[57] F. S. Lee and A. P. Chandrakasan, "A 2.5 nJ/bit 0.65 V Pulsed UWB Receiver in 90 nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 42 Issue:12, pp. 2851 – 2859, Dec 2007.

[58] M. Crepaldi, M. R. Casu, M. Graziano, and M. Zamboni, "A low-power CMOS 2-PPM demodulator for energy detection IR-UWB receivers," in *Ultra-Wideband, 2007. ICUWB 2007. IEEE International Conference on*. IEEE, 2007, pp. 461–466.

[59] D. Kreiser and S. Olonbayar, "Improvements of IEEE 802.15. 4a for non-coherent energy detection receiver," in *Signals, Systems, and Electronics (ISSSE), 2012 International Symposium on*. IEEE, 2012, pp. 1–5.

[60] K. Witrisal, G. Leus, G. J. Janssen, M. Pausini, F. Trösch, T. Zasowski, and J. Romme, "Noncoherent ultra-wideband systems," *Signal Processing Magazine, IEEE*, vol. 26, no. 4, pp. 48–66, 2009.

[61] M. Flury, R. Merz, J.-Y. Le Boudec, and J. Zory, "Performance evaluation of an IEEE 802.15. 4a physical layer with energy detection and multi-user interference," in *Ultra-Wideband, 2007. ICUWB 2007. IEEE International Conference on*. IEEE, 2007, pp. 663–668.

[62] A. Gerosa, S. Soldà, A. Bevilacqua, D. Vogrig, and A. Neviani, "An energy-detector for noncoherent impulse-radio UWB receivers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 5, pp. 1030–1040, 2009.

[63] Y. Zheng, S.-X. Diao, C.-W. Ang, Y. Gao, F.-C. Choong, Z. Chen, X. Liu, Y.-S. Wang, X.-J. Yuan, and C. H. Heng, "A 0.92/5.3 nJ/b UWB impulse radio SoC for communication and localization," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*. IEEE, 2010, pp. 230–231.

[64] X. Cheng, Y. L. Guan, and S. Li, "Optimal BER-Balanced Combining for Weighted Energy Detection of UWB OOK Signals," *Communications Letters, IEEE*, vol. 17, no. 2, pp. 353–356, 2013.

[65] M. Pelissier, D. Morche, and P. Vincent, "Super-regenerative architecture for UWB pulse detection: From theory to RF front-end design," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 7, pp. 1500–1512, 2009.

[66] D. Lachartre, B. Denis, D. Morche, L. Ouvry, M. Pezzin, B. Piaget, J. Prouvée, and P. Vincent, "A 1.1 nJ/b 802.15. 4a-compliant fully integrated UWB transceiver in 0.13μm CMOS," in *Solid-state circuits conference-digest of technical papers, 2009. ISSCC 2009. IEEE International*. IEEE, 2009, pp. 312–313.

[67] R. Hoctor and H. Tomlinson, "Delay-hopped transmitted-reference RF communications," in *Ultra Wideband Systems and Technologies, 2002. Digest of Papers. 2002 IEEE Conference on*. IEEE, 2002, pp. 265–269.

[68] M. Herceg, J. Milanovic, and M. Vranjes, "Coded M-ary Pulse Position Modulation for Transmitted Reference UWB Communication System," *Elektronika ir Elektrotechnika*, vol. 20, no. 10, pp. 62–68, 2014.

[69] L. W. Fullerton and I. A. Cowie, "Ultrawide-band communication system and method," Feb. 29 2000, uS Patent 6,031,862.

[70] R. Blázquez, P. Newaskar, and A. Chandrakasan, "Coarse acquisition for ultra wideband digital receivers," in *Acoustics, Speech, and Signal Processing, 2003. Proceedings.(ICASSP'03). 2003 IEEE International Conference on*, vol. 4. IEEE, 2003, pp. IV–137.

[71] R. Fleming, C. Kushner, G. Roberts, and U. Nandiwada, "Rapid acquisition for ultra-wideband localizers," in *Ultra Wideband Systems and Technologies, 2002. Digest of Papers. 2002 IEEE Conference on*. IEEE, 2002, pp. 245–249.

[72] V. Lottici, A. D'Andrea, and U. Mengali, "Channel Estimation for Ultra-Wideband Communications," *JOURNAL ON SELECTED AREAS IN COMMUNICATIONS*, vol. 20, no. 09, pp. 1638–1645, 9, December 2002.

[73] C. Carbonelli and U. Mengali, "Synchronization algorithms for UWB signals," *Communications, IEEE Transactions on*, vol. 54, no. 2, pp. 329–338, 2006.

[74] S. Kwon, S. Lee, and J. Kim, "A joint timing synchronization, channel estimation, and SFD detection for IR-UWB systems," *Communications and Networks, Journal of*, vol. 14, no. 5, pp. 501–509, 2012.

[75] A. Rabbachin and I. Oppermann, "Synchronization analysis for UWB systems with a low-complexity energy collection receiver," in *Ultra Wideband Systems, 2004. Joint with Conference on Ultrawideband Systems and Technologies. Joint UWBST & IWUWBS. 2004 International Workshop on*. IEEE, 2004, pp. 288–292.

[76] M. Flury, R. Merz, and J.-Y. Le Boudec, "Robust non-coherent timing acquisition in IEEE 802.15. 4a IR-UWB networks," in *Personal, Indoor and Mobile Radio Communications, 2009 IEEE 20th International Symposium on*. IEEE, 2009, pp. 1642–1646.

[77] D. Kreiser and S. Olonbayar, "Efficient synchronization method for IR-UWB 802.15. 4a non-coherent energy detection receiver," in *Proceedings of the 2010 IEEE/ACM Int'l Conference on Green Computing and Communications & Int'l Conference on Cyber, Physical and Social Computing*. IEEE Computer Society, 2010, pp. 521–526.

[78] F. Wang, Z. Tian, and B. M. Sadler, "Weighted energy detection for noncoherent ultra-wideband receiver design," *Wireless Communications, IEEE Transactions on*, vol. 10, no. 2, pp. 710–720, 2011.

[79] Q. Zhou, Z. Zou, H. Tenhunen, and L.-R. Zheng, "Adaptive synchronization and integration region optimization for energy detection IR-UWB receivers," in *Ultra-Wideband (ICUWB), 2012 IEEE International Conference on*. IEEE, 2012, pp. 62–66.

[80] R. Price and P. Green Jr, "A communication technique for multipath channels," *Proceedings of the IRE*, vol. 46, no. 3, pp. 555–570, 1958.

[81] M. Z. Win, R. Scholtz *et al.*, "Energy capture vs. correlator resources in ultra-wide bandwidth indoor wireless communications channels," in *MILCOM 97 Proceedings*, vol. 3. IEEE, 1997, pp. 1277–1281.

[82] J. R. Foerster, "The effects of multipath interference on the performance of UWB systems in an indoor wireless channel," in *Vehicular Technology Conference, 2001. VTC 2001 Spring. IEEE VTS 53rd*, vol. 2. IEEE, 2001, pp. 1176–1180.

[83] A. G. Klein, D. Brown III, D. Goeckel, and C. Johnson Jr, "RAKE reception for UWB communication systems with intersymbol interference," in *Signal Processing Advances in Wireless Communications, 2003. SPAWC 2003. 4th IEEE Workshop on*. IEEE, 2003, pp. 244–248.

[84] X. Peng, F. Chin, S. H. Wong, K. Y. Sam, and L. Zhongding, "A RAKE combining scheme for an energy detection based noncoherent OOK receiver in UWB impulse radio systems," in *Ultra-Wideband, The 2006 IEEE 2006 International Conference on*. IEEE, 2006, pp. 73–78.

[85] D. Cassioli, M. Z. Win, F. Vatalaro, and A. F. Molisch, "Low complexity rake receivers in ultra-wideband channels," *Wireless Communications, IEEE Transactions on*, vol. 6, no. 4, pp. 1265–1275, 2007.

[86] G. Masson, D. Morche, H. Jacquinot, P. Vincent, F. Dehmas, S. Paquelet, A. Bisiaux, O. Fourquin, J. Gaubert, and S. Bourdel, "A 1 nJ/b 3.2-to-4.7 GHz UWB 50 Mpulses/s double quadrature receiver for communication and localization," in *ESSCIRC, 2010 Proceedings of the*. IEEE, 2010, pp. 502–505.

[87] I. Oppermann, M. Hämäläinen, and J. Iinatti, *UWB: theory and applications*. John Wiley & Sons, 2005.

[88] R. A. Scholtz and M. Z. Win, "Impulse radio," in *Wireless Communications*. Springer, 1997, pp. 245–263.

[89] R. Tesi, M. Hämäläinen, and J. Iinatti, "Impact of the number of fingers of a selective rake receiver for UWB systems in modified Saleh-Valenzuela channel," in *The 4th Finnish Wireless Communication Workshop, Oulu, Finland*. Citeseer, 2003.

[90] RUBY, ANR French collaborative research project, "Radio UWB for BodY area network," http://www.agence-nationale-recherche.fr/?Project=ANR-11-INFR-0004, 2012-2015.

[91] S. Bourdel, Y. Bachelet, J. Gaubert, R. Vauché, O. Fourquin, N. Dehaese, and H. Barthélemy, "A 9-pJ/pulse 1.42-Vpp OOK CMOS UWB pulse generator for the 3.1–10.6-GHz FCC band," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, no. 1, pp. 65–73, 2010.

[92] J. Dugundji and E. Ackerlind, "Automatic bias control for a threshold detector," *Information Theory, IRE Transactions on*, vol. 3, no. 1, pp. 65–70, 1957.

[93] V. G. Hansen, "Constant false alarm rate processing in search radars(receiver output noise control)," *Radar- Present and future*, pp. 325–332, 1973.

[94] A. R. Elias-Fuste, A. Broquetas-Ibars, J. P. Antequera, and J. Yuste, "CFAR data fusion center with inhomogeneous receivers," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 28, no. 1, pp. 276–285, 1992.

[95] A. Zaimbashi and Y. Norouzi, "A robust CFAR detector in non-homogenous environment," in *Radar Conference, 2008. RADAR'08. IEEE*. IEEE, 2008, pp. 1–4.

[96] A. F. Molisch, K. Balakrishnan, D. Cassioli, C.-C. Chong, S. Emami, A. Fort, J. Karedal, J. Kunisch, H. Schantz, U. Schuster *et al.*, "IEEE 802.15. 4a channel model-final report," *IEEE P802*, vol. 15, no. 04, p. 0662, 2004.

[97] A. F. Molisch, D. Cassioli, C.-C. Chong, S. Emami, A. Fort, B. Kannan, J. Karedal, J. Kunisch, H. G. Schantz, K. Siwiak *et al.*, "A comprehensive standardized model for ultrawideband propagation channels," *Antennas and Propagation, IEEE Transactions on*, vol. 54, no. 11, pp. 3151–3166, 2006.

[98] R. D'Errico and L. Ouvry, "Time-variant BAN channel characterization," in *Personal, Indoor and Mobile Radio Communications, 2009 IEEE 20th International Symposium on*. IEEE, 2009, pp. 3000–3004.

[99] S. Van Roy, C. Oestges, F. Horlin, and P. De Doncker, "A comprehensive channel model for UWB multisensor multiantenna body area networks," *Antennas and Propagation, IEEE Transactions on*, vol. 58, no. 1, pp. 163–170, 2010.

[100] A. A. Saleh, R. Valenzuela *et al.*, "A statistical model for indoor multipath propagation," *Selected Areas in Communications, IEEE Journal on*, vol. 5, no. 2, pp. 128–137, 1987.

[101] T. Aoyagi, J.-i. Takada, K. Takizawa, N. Katayama, T. Kobayashi, K. Y. Yazdandoost, H.-b. Li, and R. Kohno, "Channel models for wearable and implantable WBANs," *IEEE 802.15 WPAN Document IEEE P802. 15-08-0416-04-0006*, pp. 1–57, 2008.

[102] H. Sawada, T. Aoyagi, J.-i. Takada, K. Y. Yazdandoost, and R. Kohno, "Channel models between body surface and wireless access point for UWB band," *IEEE 802.15 WPAN Document IEEE 802.15-08-0576-00-0006*, pp. 1–14, 2008.

[103] X. Chen, X. Lu, D. Jin, L. Su, and L. Zeng, "Channel modeling of UWB-based wireless body area networks," in *Communications (ICC), 2011 IEEE International Conference on*. IEEE, 2011, pp. 1–5.

[104] R. Di Bari, Q. H. Abbasi, A. Alomainy, and Y. Hao, "An advanced UWB channel model for body-centric wireless networks," *progress in electromagnetics research*, vol. 136, pp. 79–99, 2013.

[105] A. Khaleghi, R. Chávez-Santiago, and I. Balasingham, "Ultra-wideband pulse-based data communications for medical implants," *Communications, IET*, vol. 4, no. 15, pp. 1889–1897, 2010.

[106] J. Wang and Q. Wang, "Channel modeling and BER performance of an implant UWB body area link," in *Applied Sciences in Biomedical and Communication Technologies, 2009. ISABEL 2009. 2nd International Symposium on*. IEEE, 2009, pp. 1–4.

[107] A. Khaleghi, R. Chávez-Santiago, and I. Balasingham, "Ultra-wideband statistical propagation channel model for implant sensors in the human chest," *Microwaves, Antennas & Propagation, IET*, vol. 5, no. 15, pp. 1805–1812, 2011.

[108] R. Chavez-Santiago, K. Sayrafian-Pour, A. Khaleghi, K. Takizawa, J. Wang, I. Balasingham, and H.-B. Li, "Propagation models for IEEE 802.15. 6 standardization of implant communication in body area networks," *Communications Magazine, IEEE*, vol. 51, no. 8, pp. 80–87, 2013.

[109] J. A. Hanley and A. Lippman-Hand, "If nothing goes wrong, is everything all right?: interpreting zero numerators," *Jama*, vol. 249, no. 13, pp. 1743–1745, 1983.

[110] Z. Tian and B. M. Sadler, "Weighted energy detection of ultra-wideband signals," in *Signal Processing Advances in Wireless Communications, 2005 IEEE 6th Workshop on*. IEEE, 2005, pp. 1068–1072.

[111] Z. Chair and P. K. Varshney, "Optimal Data Fusion in Multiple Sensor Detection Systems," *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-22, no. 1, pp. 98–101, Jan 1986.

[112] B. Miscopein, J. Schwoerer, and J.-M. Gorce, "Multipath decision fusion for low complexity UWB-IR non-coherent receivers," in *Personal, Indoor and Mobile Radio Communications, 2009 IEEE 20th International Symposium on*. IEEE, 2009, pp. 1632–1636.

[113] K. Y. Yazdandoost and K. Sayrafian-Pour, "Channel Model for Body Area Network (BAN)," *IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)*, vol. Document IEEE802.15-08-0780-05-0006, 2009.

[114] L.-A. DUFRENE, "Réalisation du codeur/décodeur de canal pour un démonstrateur de transmission haut débit pour réseaux BANs," Institue MinesTelecom - Telecom Bretagne, Tech. Rep., 2014.

[115] Xilinx Inc., "Spartan-6 FPGA SelectIO Resources," Xilinx, Tech. Rep., February 14, 2014.

[116] N. Sawyer, "Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)," XILINX, Tech. Rep., June 3, 2010.

[117] S. Olonbayar, D. Kreiser, and R. Kraemer, "FPGA and ASIC implementation and testing of IR-UWB baseband transceiver for IEEE802. 15.4 a," in *Ultra-WideBand (ICUWB), 2014 IEEE International Conference on*. IEEE, 2014, pp. 456–461.

List of publications

International Conferences

[1] H. Chougrani, J. Schwoerer, P-H. Horrein and A. Baghdadi. Efficient Synchronization Technique for Non-coherent IR-UWB Receiver Targeting IEEE 802.15.6 Wireless BAN. In *Proceedings of the 8th International Conference on Body Area Networks (BodyNets), pp. 181 - 184*, Boston, Massachusetts, United States, September 30-October 2, 2013.

[2] H. Chougrani, J. Schwoerer, P-H. Horrein and A. Baghdadi. Hardware implementation of a non-coherent IR-UWB receiver synchronization algorithm targeting IEEE 802.15.6 wireless BAN. In *IEEE International Conference on Ultra-Wideband (ICUWB 2014)*, Paris, France, 1-3 September, 2014.

[3] H. Chougrani, J. Schwoerer, P-H. Horrein and A. Baghdadi. UWB-IR digital baseband architecture for IEEE 802.15.6 wireless BAN. In *Proceedings of the 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), PP. 866 - 869*, Marseille, France, 7-10 December, 2014.

Ready for Submission

[4] H. Chougrani, J. Schwoerer, P-H. Horrein and A. Baghdadi. Design and implementation of a flexible and rapid synchronization technique for non-coherent IR-UWB receivers. *In preparation for submission to IEEE Transactions on Wireless Communications*, 2016.

[5] H. Chougrani, J. Schwoerer, P-H. Horrein and A. Baghdadi. A non-coherent IR-UWB digital baseband architecture for IEEE 802.15.6 wireless BAN. *In preparation for submission to IEEE Transactions on Signal Processing*, 2016.

Résumé

La radio impulsionnelle ultra large bande (IR-UWB) a été retenue récemment pour la nouvelle norme IEEE 802.15.6 dédiée aux réseaux Body Area Network (BAN), en particulier pour les communications entre objets à la surface ou à proximité du corps. Cette technologie est apriori très attractive pour des objets nomades aux ressources énergétiques limitées, de par sa flexibilité en termes de débit, de complexité et de capacité à être économe en énergie. On peut cependant constater qu'il n'existe que peu d'implémentations réelles de systèmes UWB pour les BAN. Ce travail de thèse apporte une contribution dans ce domaine. L'étude est centrée sur le traitement numérique en bande de base pour les récepteurs non-cohérents de faible complexité et porte d'abord sur la conception d'algorithmes de réception UWB pour les BAN puis sur leur implémentation matérielle efficace sur cible FPGA.

Dans un premier temps, une chaine de réception non-cohérente en bande de base complète a été proposée, testée, puis validée par simulation. Par la suite, une architecture matérielle de faible complexité a été conçue pour implémenter cette chaine puis portée sur une cible FPGA. Enfin, la faisabilité du système de communication complet a été confirmée par la réalisation d'expérimentations de transmissions réelles sans fil avec un démonstrateur matériel complet, confirmant ainsi la viabilité technique de l'approche retenue pour la mise en œuvre de la technologie IR-UWB pour les réseaux BAN.

Mots-clés : UWB, radio impulsionnelle, BAN, IEEE 802.15.6, traitement numérique de réception, synchronisation, détection, démodulation, architecture numérique, FPGA.

Abstract

The impulse radio ultra-wideband (IR-UWB) technology has been recently adopted in the new IEEE 802.15.6 standard for Body Area Networks (BAN), in particular for communications between devices on or near the body surface. A priori, this technology is very attractive for mobile devices with limited energy resources, due to its flexibility in terms of throughput, complexity, and capacity for energy savings. However, the number of existing real implementations of UWB systems for BAN is very limited. In this context, the current Ph.D. thesis proposes a novel contribution in this area. The study focuses on digital baseband processing design for low-complexity non-coherent IR-UWB receivers. It concerns both the design of IR-UWB reception algorithms for BAN applications and their efficient hardware implementation.

First, a complete non-coherent baseband reception chain has been proposed, tested, and validated through system simulations. Afterward, low-complexity hardware architectures have been designed to implement the proposed algorithms targeting an FPGA prototype. Finally, the feasibility of the complete communication system has been confirmed through practical experiments of real-time wireless transmissions with a complete hardware demonstrator. The obtained results demonstrate the technical viability of the proposed approach to implement efficiently IR-UWB technology for body area networks.

Keywords : UWB, impulse radio, BAN, IEEE 802.15.6, digital processing, receiver, synchronization, detection, demodulation, digital architecture, FPGA.

TELECOM Bretagne

n° d'ordre : 2016telb0405

Télécom Bretagne
Technopôle Brest-Iroise - CS 83818 - 29238 Brest Cedex 3
Tél : + 33(0) 29 00 11 11 - Fax : + 33(0) 29 00 10 00