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UNIVERSITÉ GRENOBLE ALPES

THÈSE

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préparée au sein du **Laboratoire IMEP-LAHC**
dans **l'École Doctorale EEATS**

Caractérisation et modélisation électrique de substrats SOI avancés

Thèse soutenue publiquement le **24 Novembre 2015**,
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To my family
and to my girlfriend

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Abstract/Résumé

Title: Electrical characterization and modeling of advanced SOI substrates

Silicon-on-insulator (SOI) substrates represent the best solution to achieve high performance devices. Electrical characterization methods are required to monitor the material quality before full transistor fabrication. The classical configuration used for SOI measurements is the pseudo-MOSFET. In this thesis, we focused on the enrichment of techniques in Ψ-MOSFET for the characterization of bare SOI and III-V wafers. The experimental setup for static I_D-V_G was improved using a vacuum contact for the back gate, increasing the measurement stability. Furthermore, this contact proved to be critical for achieving correct capacitance values with split-CV and quasi-static techniques (QSCV). We addressed the possibility to extract Dit values from split-CV and we demonstrated by modeling that it is impossible in typical sized SOI samples because of the time constant associated to the channel formation. The limitation was solved performing QSCV measurements. Dit signature was experimentally evidenced and physically described. Several SOI structures (thick and ultra-thin silicon films and BOX) were characterized. In case of passivated samples, the QSCV is mostly sensitive to the silicon film-BOX interface. In non-passivated wafers, a large defect related peak appears at constant energy value, independently of the film thickness; it is associated to the native oxide present on the silicon surface. For low-frequency noise measurements, a physical model proved that the signal arises from localized regions surrounding the source and drain contacts.

Keyword: Silicon-on-insulator (SOI), pseudo-MOSFET (Ψ-MOSFET), static I_D-V_G, split-CV, quasi-static capacitance (QSCV), low-frequency noise (LFN), III-V materials.

Titre: Caractérisation et modélisation électrique de substrats SOI avances

Les substrats Silicium-sur-Isolant (SOI) représentent la meilleure solution pour obtenir des dispositifs microélectroniques ayant de hautes performances. Des méthodes de caractérisation électrique sont nécessaires pour contrôler la qualité SOI avant la réalisation complète de transistors. La configuration classique utilisée pour les mesures du SOI est le pseudo-MOFSET. Dans cette thèse, nous nous concentrons sur l'amélioration des techniques autour du Ψ-MOFSET, pour la caractérisation des plaques SOI et III-V. Le protocole expérimental de mesures statiques I_D-V_G a été amélioré par l'utilisation d'un contact par le vide en face arrière, permettant ainsi d'augmenter la stabilité des mesures. De plus, il a été prouvé que ce contact est essentiel pour obtenir des valeurs correctes de capacité avec les méthodes split-CV et quasi-statique. L'extraction des valeurs de D_{it} avec split-CV a été explorée, et un model physique nous a permis de démontrer que ceci n'est pas possible pour des échantillons SOI typiquement utilisés, à cause de la constante de temps reliée à la formation du canal. Cette limitation a été résolue un effectuant des mesures de capacité quasi-statique (QSCV). La signature des D_{it} a été mise en évidence expérimentalement et expliquée physiquement. Dans le cas d'échantillons passivés, les mesures QSCV sont plus sensibles à l'interface silicium-BOX. Pour les échantillons non passivés, un grand pic dû à des défauts d'interface apparait pour des valeurs d'énergie bien identifiées et correspondant aux défauts à l'interface film de silicium-oxyde natif. Nous présentons des mesures de bruit à basses fréquences, ainsi qu'un model physique démontrant que le signal émerge de régions localisées autour des contacts source et drain.

Mots cles: Silicium-Sur-Isolant (SOI), pseudo-MOSFET (Ψ-MOSFET), statique I_D-V_G, split-CV, capacité quasi-statique (QSCV), bruit basse fréquence (LFN), semiconducteurs III-V.

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Chapter I:

General introduction

In this chapter, the recent trends in microelectronics will be presented. The interest on using silicon-on-insulator (SOI) substrates will be pointed out. SOI fabrication process, typical properties, related defects and characterization methods are discussed. The general objectives of the thesis are detailed.

Contents Chapter I

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I.1 MOS transistors: state of art and trends

The concept for a Field Effect Transistor (FET) was invented by Lilienfeld [1] in 1930. It did not immediately catch the attention of the research community and the idea was not applied until 1948, when the first device was fabricated at Bell Labs [2]. After the fabrication of the first integrated circuit (IC) in the 1958 [3], the topic became hot and a lot of industrial companies and researches focused their attention on transistors.

Nowadays, MOS transistors are the base of all the integrated circuits which constitute the electronic devices largely present in our life: computers, cars, phones, etc., leading to huge market place that changed our social behavior [4].

Metal-oxide-semiconductor field effect transistor

The microelectronics world is based on simple devices that can operate together to compute complex functions. In general, these devices are classified according to their operation principle. We focus here on the metal-oxide-semiconductor field effect transistor (MOSFET), the primary device for circuits.

Figure I-1a shows the structure. It is easier to analyze it along the vertical (x) and horizontal (y) axis separately [5]:

- Along the x-axis we have a metal-oxide-semiconductor (MOS) structure. The semiconductor is typically nearly doped silicon (in the example, it is p-type, thus a n-MOSFET is obtained). On top of it, a silicon-dioxide layer is fabricated and serves as gate oxide. A conductive gate is placed on the top interface of the SiO_2. The gate bias V_G controls the electronic bands bending in the silicon, at the interface with the gate oxide. A conduction channel made of electrons is induced if $V_G > V_T$ (threshold voltage). For low values of gate bias, no free carriers are present in the channel;
- Along the y-axis two highly doped regions (source and drain) are made by implantation of the silicon next to the conduction channel. Considering the case of p-type silicon film, the source and drain contacts are n^{++} type. The source is grounded, while a bias is applied on the drain side (drain bias, V_D). For $V_G << V_T$, no carrier flow is possible and the transistor is off. For gate bias values higher than the threshold voltage, a large current of electrons flows between source and drain contacts (drain current, I_D), making the device "*on*".

Figure I-1b shows a schematic of drain current in logarithmic scale versus gate bias for standard n-type transistor. The characteristic has a clear switch behavior. Three regions related to the state of the device can be identified:

- Off-state: $V_G << V_T$ and no current flow is possible. The current measured for $V_G = 0$, labeled I_{off}, governs the static power consumption. The off-state current has to be as small as possible to reduce power dissipation [5];
- On-state: for $V_G > V_T$ the conduction channel is completely created. The measured drain current at given V_G and V_D is labeled I_{on};

- Subthreshold region: the channel starts to be created, but it is not yet complete. The slope of the I_D in logarithmic scale versus V_G (identified as subthreshold swing, $S_s = 1/slope$) defines the speed at which the device can switch between on-state and off-state. High transistor performances are obtained for steep slope (fast on-off transition) [5].

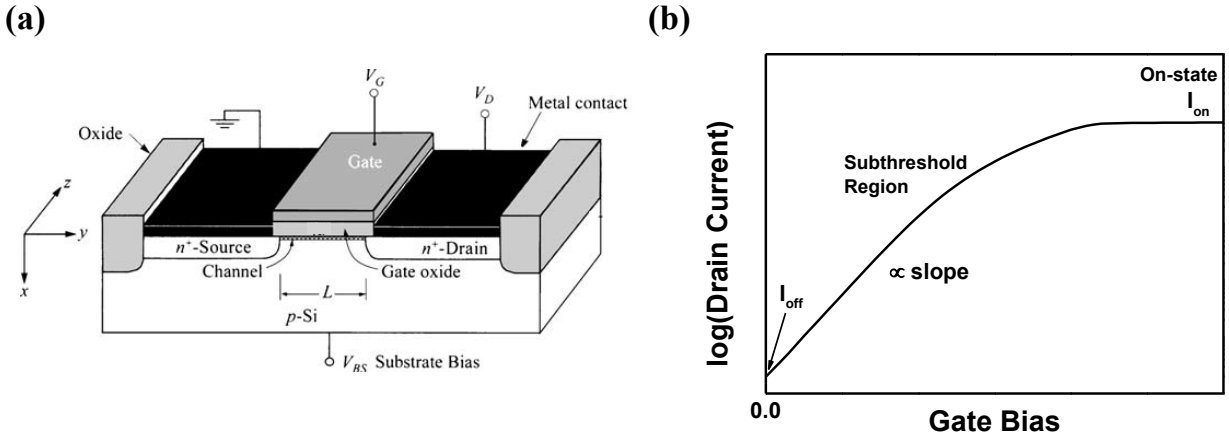

Figure I-1: (a) Schematic view of n-type MOSFET [5]. (b) Example of drain current in logarithmic scale versus gate bias for n-MOSFET.

One of the main advantages of MOSFET is the possibility to co-integrate p-type and n-type devices on the same substrate, thanks to the use of implanted wells (CMOS technology) (Figure I-2). This allows the fabrication of integrated logic circuits which are small and fast.

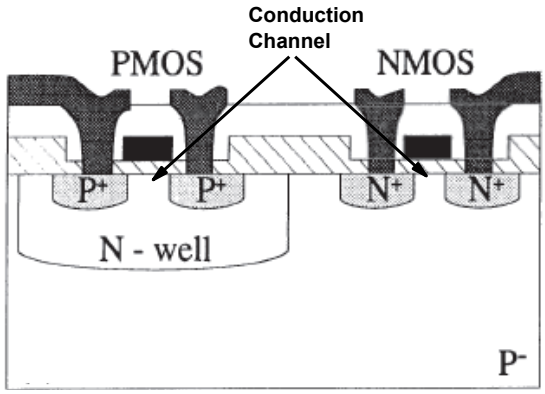

Figure I-2: Example of co-integration of p-type and n-type bulk MOSFET [6].

Microelectronics trends

The transistor scaling down and performance improvements are the main topics of microelectronics industry and research. The mainstream is defined by the well-known "Moore's law" [7]: every decade of technology evolution corresponds to an extra order of magnitude in transistor density (Figure I-3). In order to drive the microelectronics research & development, the International Technology Roadmap for Semiconductors (ITRS) presents the state-of-art and provides guidelines and targets for the following years. Today the fabricated transistors have *22-30 nm* gate length. The last updated report of IRTS in 2014 predicts that the logic industry will have transistors with sub-*10 nm* gate length in 2017 (*7 nm* node) [8].

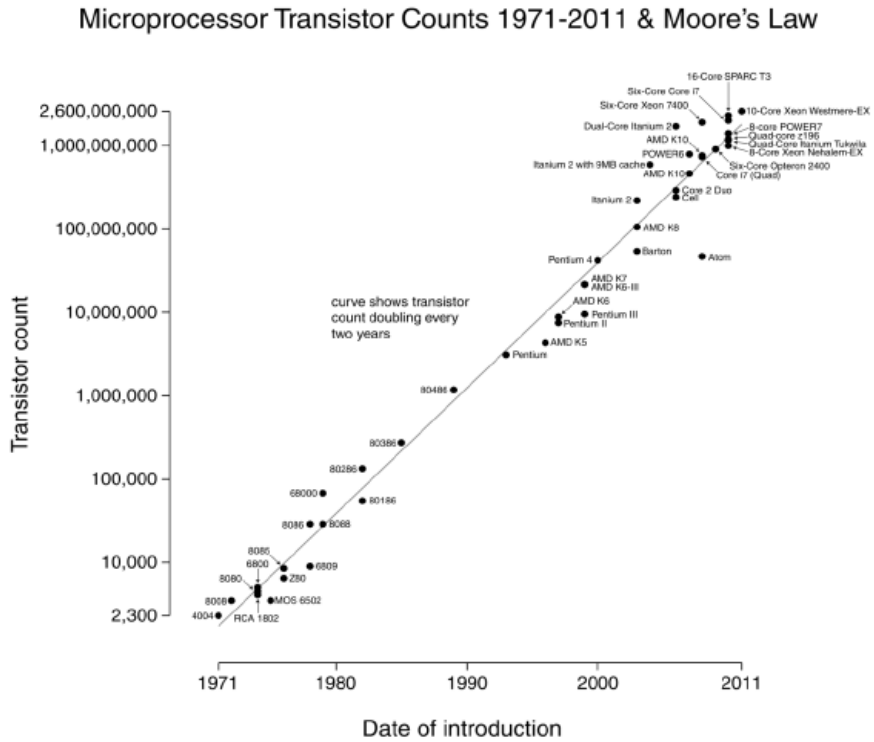

Figure I-3: Evolution of microprocessor transistors count (Moore's law) [7].

However, physical limitations can compromise the device scaling down and limit the MOSFET performances:

- The decrease of the gate oxide thickness leads to an exponentially increase of the leakage current through the oxide (gate current, I_G) with consequent loss of transistor-like behavior [9];
- Decreasing the MOSFET dimensions, mobility degradation is due to limitations of fabrication process [10], [11]. The mobility degradation is smaller structures drastically limits the transistor speed;
- In high quality Si-SiO_2 interface, the subthreshold slope is not controlled by the transistor dimensions but is mainly a function of the temperature. Thus, at room temperature in the best case (SOI) it can be ≈ *66 mV/dec* [5]. To obtain faster on-off transitions, new device architecture are demanded;
- Short-channel effects (SCE): around source and drain contacts, depletion regions are present [5]. When the device becomes smaller, the two depleted regions can overlap, leading to loss of electrostatic control of the gate bias. In order to fabricate faster and smaller transistors, new architectures are required such as multi-gate (MG) structures.

Several solutions were proposed to overcome the problems, such as the replacement of polyscristalline Si used as gate with metal [12], the use of high-κ dielectric material instead of silicon-dioxide [13], the replacement of the silicon channel with new materials with high performances [14], [15], etc. Table I-1 reports the challenge for *near-term 2013-2020* according to ITRS predictions.

Near-Term 2013-2020	Summary of Issues
Scaling Si CMOS	• Scaling of fully depleted SOI and multi-gate (MG) structures • Implementation of gate-all-around (nanowire) structures • Controlling source/drain series resistance within tolerable limits • Further scaling of EOT with higher κ materials (κ > 30) • Threshold voltage tuning and control with metal gate and high-κ stack • Inducing adequate strain in advanced structures
Implementation of high-mobility CMOS channel materials	• Basic issues same as for Si devices listed above • High-κ gate dielectrics and interface state (D_{it}) control • CMOS (n- and p-channel) solution with monolithic material integration • Epitaxy of lattice-mismatched materials on Si substrate • Process complexity and compatibility with significant thermal budget limitations

Table I-1: Near-term 2013-2020 challenges defined by ITRS 2013. Table adapted from the document [8].

The short-channel effects that strongly affect the performances of small devices can be limited by particular transistor architectures. Two main ways were explored:

- STMicroelectronics®, Samsung® and GlobalFroundries® moved to MOSFET fabricated on silicon-on-insulator (SOI technology) (Figure I-4a). Fully-depleted (FDSOI) transistors lead to several practical advantages like the reduction of short-channel effect [16], [17], the possibility to use multiple threshold voltage [18], [19] and the capability to achieve high performances (*e.g.*, avoid mobility degradation) [20]–[22]. The transistor structure is still planar (*i.e.*, the conduction channel is on a two-dimensional planes, as in Figure I-1a);
- Fin-shaped FET, called FinFET, is the architecture adopted by Intel®, Samsung®, TSMC and Global Foundries (Figure I-4b). In this case the gate surrounds 3 sides of the silicon film which acts as conduction channel (3D structure). This allows a better electrostatic control. However, the fabrication process is very different to the planar structure and huge economic effort was required to implement it. Note also that the FinFET fabrication is easier on SOI substrate [5]. The use of SOI improves the electrostatic isolation of the conduction channel and decreases the leakage current [6]. The feasibility and the interest of FinFET on SOI is documented in [23]–[27].

Hence, independently of the implemented MOSFET architecture (planar or 3D), it is clear that SOI substrates are superior for improving device performances. Thus, in this thesis we focus on SOI technology and, in the next sub-sections, after showing the schematic of SOI structure, a description of the main advantages and drawbacks arising from the use of SOI technology will be presented.

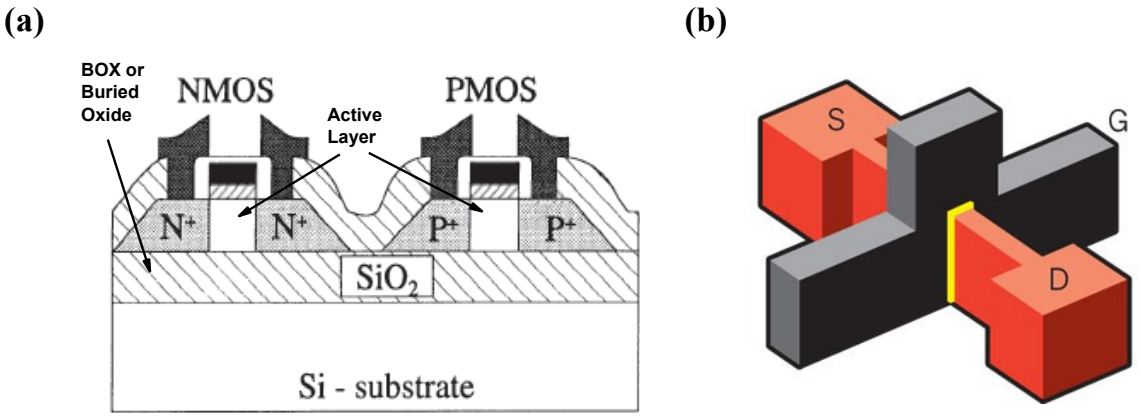

Figure I-4: (a) Example of p-type and n-type MOSFET co-integrated using silicon-on-oxide substrate [6]. (b) FinFET structure [28].

Silicon-on-insulator structure

The SOI substrate is a multi-layer stack with a top silicon film, that acts as active layer for the devices, a buried oxide (BOX) used to isolate the active layer from the substrate and a low-doped p-type substrate used as mechanical support of the structure [6] (see Figure I-5).

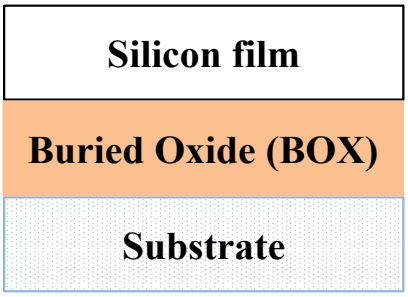

Figure I-5: Schematic of silicon-on-insulator (SOI) substrate.

Advantages of SOI technology

In MOSFET on bulk silicon (see Figure I-2) the conduction channel is confined close to the oxide interface. Most part of the thickness of the silicon substrate is not used but it is subject to parasitic effects such as current leakage, latch-up. Placing an oxide (called BOX or buried oxide) between the active layer and the substrate (see Figure I-4a), the conduction channel is isolated from the substrate, improving the transistor characteristics. This is the key point of SOI technology. Examples of benefits are:

- *Reduction of parasitic capacitances*; for example capacitances between source/drain contacts and the substrate are drastically reduced thanks to the presence of the BOX. Hence, devices fabricated on SOI work at higher frequencies than bulk technology [6];
- *Reduction of short-channel effects*: the surfaces of the source and drain junctions are now defined by the silicon film thickness. Thus, the depletion regions are spatially limited by the presence of the buried oxide and consequently they are reduced compared to a MOSFET on bulk silicon. In case of FDSOI, the gate has a better electrostatic control on the channel [16], [17];

- *Improved device isolation*: the buried oxide leads to better device isolation. Thus, phenomena like latch-up disappear leading to higher fabrication density [29];
- *Improvement of subthreshold swing*: in FDSOI devices, the depletion region is confined in the top silicon film leading to smaller associated capacitance. Hence, the slope of drain current in weak inversion is improved. Values close to the theoretical *66 mV/dec* can be achieved at room temperature [30], [31]. This allows the use of smaller threshold voltage and operating voltage, thus reducing the power consumption [32], [33];
- *Immunity against radiations*: devices fabricated on SOI substrate are less affected by external radiations. Since the active layer (top silicon film of the SOI structure) is isolated from the bulk substrate by the buried oxide, the impact of transient effects or ionization phenomena are drastically attenuated [30].

Issues with SOI technology

Despite the large numbers of advantages associated to SOI substrates, some drawbacks are still present:

- *SOI quality*: device performance improvements are obtained only in case of high quality SOI substrates. Thus, the carrier mobility in the silicon film has to be high and the density of defects low at silicon film-BOX interface;
- *Production costs*: SOI substrates are more expensive than bulk silicon. However, their use for mass production decreases the impact of the substrate price on the IC;
- *Interface coupling*: in FDSOI device, two silicon-SiO_2 interfaces are present: one between the conduction channel and gate oxide, and the second one between the Si layer and the buried oxide. In case of ultra-thin silicon films, electrical coupling can be present between the two interfaces. The models to describe the characteristics have to be adapted to the FDSOI case;
- *Floating-body effect*: the holes present in the channel are confined by the buried oxide and cannot be evacuated, affecting the device performances. An example is the enhancing of leakage current [34]–[36];
- *Self-heating effects*: the buried oxide has smaller thermal conductivity than bulk silicon material. Thus, for high current flow, the generated heat remains confined in the conduction channel decreasing the device performances. The problem is negligible for dynamic operation of the device [37].

I.2 SOI substrates

SOI fabrication

The SOI technology started with Silicon-on-Sapphire wafers (SOS) [38]. SOS substrates improved the resistance of the integrated circuits against radiations. Consequently, this technology was very appealing for space and military applications. However, the high fabrication costs and insufficient crystal quality limited the market.

A step forward was the fabrication of devices on implanted oxygen layer which formed an insulating film under the transistor [39]. This opened the way to new fabrication processes like Separation by Implantation of Oxygen (SIMOX) [40], Bond-and-Etch-Back SOI (BESOI) [41] and Epitaxial Layer Transfer Wafer (ELTRAN) [42]. However, the interface quality was not high enough to introduce the SOI substrates in large-scale market.

The development of Smart-Cut™ process [43] completely changed the SOI production. Today, the use of this technology allows the highest quality of silicon-on-insulator substrate [44].

The main steps involved in the Smart-Cut™ fabrication process are (see Figure I-6):

- Two silicon wafers are required: a 'donor wafer' labeled A and a 'handle wafer' B;
- Thermal oxidation is performed on the wafer A, to growth SiO_2, that will be the BOX of the final SOI substrate. The oxidation process allows a precise control of SiO_2 quality and thickness;
- Hydrogen implantation is performed through the fabricated oxide. This induces micro-cavities that define the future plan of fracture (dash line in Figure I-6 at step 3_oxidation);
- The donor and handle wafers are cleaned. The surfaces are made hydrophilic;
- The two wafers are put in contact and annealed, in order to increase the pressure of hydrogen molecules in the micro-cavities. This leads to H_2 propagation which induces an horizontal fracture in the wafer A;
- The two wafers are thus separated. The wafer B is now an SOI substrate suitable for device fabrication, while the wafer A can be reused for another SOI fabrication process.

The Smart-Cut™ technology has several advantages which justify its industrial interest:

- Low density of defects is present at the interface between the top silicon film and BOX;
- High quality silicon films are obtained;
- Conventional implantation and annealing tools are used;
- The top silicon film and BOX thickness can be easily adjusted to the wanted values.

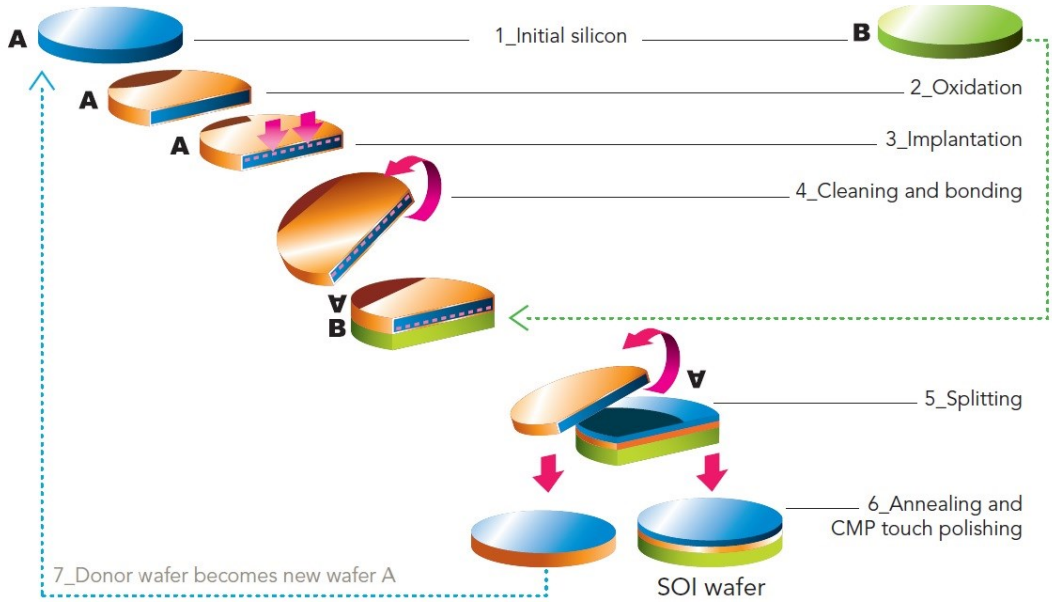

Figure I-6: Schematic of Smart-Cut™ process for SOI fabrication [45].

SOI characterization

SOI substrates are clearly an asset for high quality devices but they must be of high quality. The huge fabrication progress achieved thanks to Smart-Cut™ leads todays to excellent quality substrates. However, as expressed by ITRS report, further developments on the SOI characterization (and monitoring) are required for two reasons [8]:

- Support the research and drive the next improvements on the fabrication processes;
- Monitor the fabricated substrates and their quality during mass production.

Structural characterization techniques for SOI substrates can be divided into two groups, according to their capability to investigate geometrical dimensions or defects of the material. The characterization of SOI substrates is more complex than standard bulk silicon. The presence of a supplementary oxide (the BOX) with an additional Si-SiO_2 interface requires adapted characterization methods and new approaches when the standard techniques fail.

Focusing on the geometrical dimensions, the key properties which require very accurate measurements are:

- *BOX* and *silicon film thickness*: a small variation of their values drastically affects the electrical performances of the fabricated devices. Thus, they are monitored with variable-angle single-wavelength reflectometry, single-wavelength ellipsometry and spectroscopic ellipsometry [30], [46];
- *Wafer flatness* is mandatory to make the SOI substrate compatible with all the tools required for MOSFET fabrication (especially for lithography steps).

Structural defects are also present in the SOI substrate and they can degrade the performance of the future transistors [33]. The most important are (see the schematic in Figure I-7):

- *Dislocations* and *stacking faults* are found as in standard bulk silicon;
- *Surface roughness*: it is a critical parameter because it can decrease the breakdown voltage on the fabricated device;
- *Voids* can be present at the BOX interface especially due to dust. Today this type of defects is very rare;
- *"Pipes"*: are conductive vias which can be present in the oxide or in the silicon film. They act as a parallel resistor, increase the off-current and reduce the device immunity against radiations;
- *Metal or alkaline ions contaminations*: they can affect the fabrication process (metal contaminations) or the electrical properties of the structure (alkaline ions contaminations). They decrease the minority carrier lifetime and the mobility;
- *The level of residual oxygen or carbon in the silicon film*: I_{off} is increased and the breakdown voltage is decreased if these impurities are present;
- *Fixed charges in the BOX*: they affect the transistor threshold voltage and the leakage current;
- *Interface traps density* (D_{it}): these defects are due to the silicon-silicon dioxide interface and they can limit the electric properties of the transistor: poor subthreshold swing and low carrier mobility.

All these defects have to be minimized in a high quality SOI substrate. This is possible only improving the fabrication processes and monitoring the SOI production. Some examples of characterization methods for structural aspects of SOI are: AFM (Atomic Force Microscope), TRXF (Total Reflection at X Fluorescence) and SIMS (Secondary Ion Mass Spectroscopy).

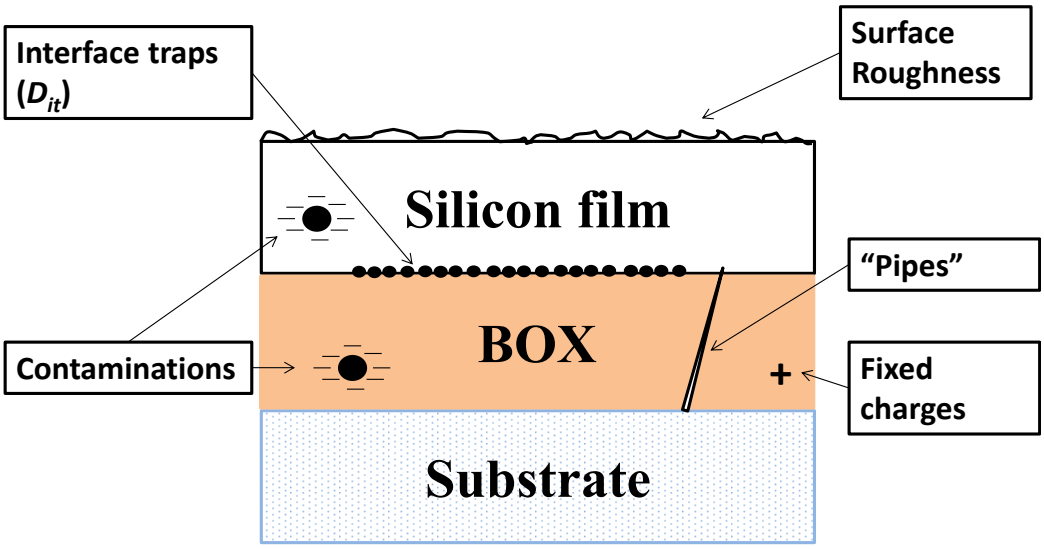

Figure I-7: Example of defects on SOI structure.

Electrical characterization

The SOI substrate serves to fabricate a MOSFET and if the SOI substrate is low quality, the final transistor will have poor performance. Thus, the key point is to evaluate the electrical impact of the listed defects. The best configuration to electrically characterize a bare SOI wafer without fabrication of the entire device is the pseudo-MOSFET [6].

I.3 Objectives and organization of the thesis

The previous section clearly showed the necessity to electrically characterize the SOI substrates after their fabrication and before the transistor production. The pseudo-MOSFET (see Sec. II.2) is the solution used ever since 1992. Its capability to measure carrier mobility and interface traps density was proved using I_D-V_G curves [6]. However, the reduction of the top silicon film and BOX thicknesses complicates the characterization and new techniques are required [46]–[52].

The objective of this thesis is to enrich the characterization techniques suitable for bare SOI substrates in pseudo-MOSFET configuration, mostly focusing on the investigation of the quality of the interface between the top silicon film and the BOX:

- Chapter II reviews the pseudo-MOSFET principle. The importance of measurement setup will be largely detailed. Some precautions on the setup will provide their benefits for stable and reproducible I_D-V_G analysis. The possibility to characterize new materials like InGaAs will be addressed.
- In Chapter III, the split-CV technique will be revisited. The capability to measure the effective carrier mobility with split-CV was already proved [53], [54]. Some aspects concerning the die surface which contributes to the whole signal are here clarified. The possibility to extract the interface traps density will be discussed from experimental and modeling point of view.
- Chapter IV presents the quasi-static capacitance measurements performed for the first time on bare SOI wafers to achieve interface characterization. After discussing the measurement setup, a physical model will be derived and validated in different configurations. A suitable procedure to compute interface traps density will be presented, tested and applied to characterize several SOI geometries, from thick to ultra-thin films and BOXs.
- The low-frequency noise measurements performed in pseudo-MOSFET configuration will be addressed in Chapter V. This technique was expected to allow the characterization of interface traps density. Diab *et al.* [55] already applied it in pseudo-MOSFET configuration but the extracted values of traps were not realistic and required explanations. Thanks to modeling, we explain the previous results. The capability to extract D_{it} in Ψ-MOSFET is discussed through model and experiments.
- Chapter VI summarizes our results and addresses perspectives for future work.

Chapter II:

Pseudo-MOSFET for SOI characterization

This chapter presents the characterization of bare SOI wafers performed using static drain current measurements in pseudo-MOSFET configuration. The principle of operation and measuring setup will be discussed. The impact of the quality of back contact and the role of the probes on the characteristics will be addressed. The characterization of III-V layers at different fabrication steps (from bulk material to fully fabricated device) is also shown.

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II.1 The state-of-art in SOI electrical characterization

Accurate electrical characterization techniques are required to monitor the SOI material quality before pursuing device fabrication process. High transistor performances can be expected only if the carrier mobility in the top silicon film is high and the density of defects at Si film-buried oxide interface is low. In this context, we review here the electrical methods for SOI.

The simplest way to investigate the electrical properties of a material is the *4*-probe resistivity measurement. In case of SOI, four needles are directly placed on the top surface of the Si film. A current *I* is imposed between the two external probes and the potential difference between the two inner probes is measured (ΔV_{diff}) (Figure II-1). Knowing the inter-probe distance (*d*), it is possible to directly compute the material resistivity [56]:

$$\rho = 2 \cdot \pi \cdot d \cdot F \cdot \frac{\Delta V_{diff}}{I} \qquad \text{(II.1)}$$

where *F* is a correction factor taking into account the probe location with respect to the sample edges, the sample thickness and the probe diameter. Equation (II.1) is only valid if all the needles have the same inter-probe distance *d* [56]. In case of large semiconductor samples, where the probes are placed far from the edges and *in-line* configuration is used (see Figure II-1), Eq. (II.1) can be re-written as a function of the sheet resistance R_{SH}:

$$\rho = 4.532 \cdot t_{Si} \cdot \frac{\Delta V_{diff}}{I} = t_{Si} \cdot R_{SH} \qquad \text{(II.2)}$$

where t_{Si} is the silicon film thickness. The carrier mobility can be determined if the doping level is known. However, with this configuration the interface traps density, that qualifies the quality of the BOX-film interface, cannot be measured.

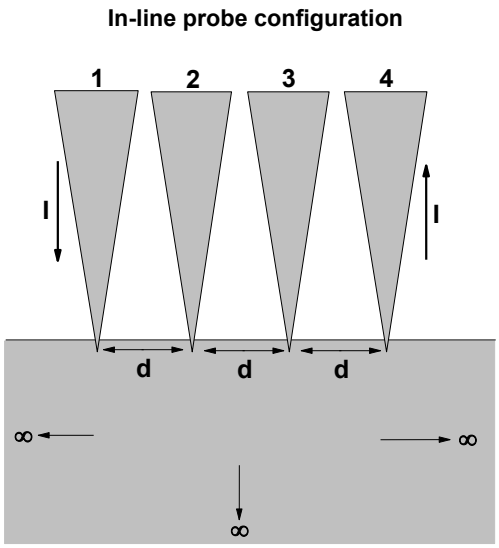

Figure II-1: *4*-probes measurement on infinite layer. 4 *in-line* needles are used.

To overcome these limitations, a new method for SOI structure was proposed in 1992: the so-called pseudo-MOSFET (Ψ-MOSFET) (see Figure II-2a) [47], [57]. The silicon substrate is biased and used like a gate to create a conduction channel at the interface between the top Si and SiO_2 layers. Two probes with controlled pressure are directly placed on the top silicon surface to access the channel; they act as source and drain contacts. The structure is an upside-down MOSFET. Thus, the same characterization techniques classically used for standard MOSFET can be adopted to measure carrier mobility and D_{it} in SOI substrate.

There are two key issues with Ψ-MOSFET:

1 The dimensions of the conduction channel are generally not well defined;

2 The quality of the source and drain contacts and therefore the access resistance is dependent on the probe penetration into the silicon film. Thus, they are sensitive to the pressure applied on the probes.

A variant of the standard Ψ-MOSFET technique was proposed in 1997: the HgFET [58]. In this case, Hg circular contacts in Corbino configuration were used instead of adjustable pressure probe (see Figure II-2b). The channel geometry (length, width) is now clearly identified. However, in order to obtain good ohmic contacts, the silicon surface has to be cleaned to remove any existing oxide, such as the native oxide on the top silicon film. Furthermore the characterization will be time dependent because the contacts quality evolves in time.

Another possibility to characterize SOI substrates is to deposit metal contacts (source and drain) on the top of the silicon film (see Figure II-2c) [59], [60]. In this case the channel dimensions are also well defined. However, the configuration has several drawbacks: it requires fabrication steps, the contacts may not be ohmic, making the extraction procedure more complex.

In order to avoid contact related issues or uncertain channel definition, Ionescu *et al*. [61] and Van Den Daele *et al*. [62] merged the standard pseudo-MOSFET configuration with the *4*-probes technique. This made the configuration pressure independent, leading to the characterization of ultra-thin SOI structures [62]. However, the interface traps density could be determined only through simulations.

Among all these variants, the standard pseudo-MOSFET with pressure probes remains the most suitable configuration for the characterization of bare SOI wafers, because it does not need fabrication steps for the contacts and it adapts easily to any type of measurement already existing in MOSFETs. We will see in the next sections and chapters how the use of optimized measurement setup and different techniques can lead to parameter extractions, suitable for SOI quality monitoring.

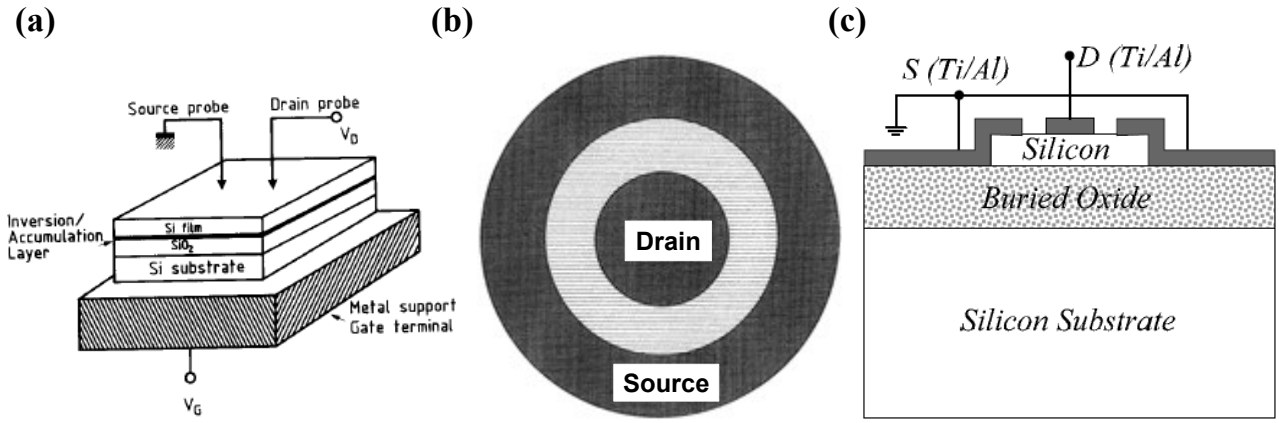

Figure II-2: (a) SOI structure characterized using standard pseudo-MOSFET configuration [47]. (b) Top view of HgFET contacts [63]. SOI wafer with fabricated source and drain contacts [64].

II.2 Principle of Ψ-MOSFET and parameter extraction methods

A detailed description of the Ψ-MOSFET and extraction methods for electrical parameters (μ, D_{it}) from I_D-V_G characteristics will be provided in this section.

Sample preparation (between film and BOX via the sidewalls)

The pseudo-MOSFET configuration with pressure probes does not need contact process. Nevertheless, in order to avoid parasitic leakage currents, the SOI wafer needs a lithography step followed by etching to create square silicon islands (mesas) separated by *2 mm* oxide (Figure II-3a). *L* is the side size of a mesa. These mesas define the dies or the tested regions on the SOI. Most of the analyses were performed on structures with $25\ mm^2$ effective area (*i.e.*, the mask size was *5 mm x 5 mm*). However, other areas are available: $4.4\ mm^2$, $9.6\ mm^2$, $16.8\ mm^2$ and $65.6\ mm^2$. Their use for some specific tests will be clearly indicated in the manuscript.

Figure II-3b shows the vertical cross-section of a silicon island. The Si thickness will be labeled t_{Si}. It is non-intentionally doped (NID) p-type: $N_a \approx 5 \cdot 10^{14}\ cm^{-3}$. Two kinds of samples with different top interface quality were available:

- Passivated samples: the top silicon surface is covered with *4 nm* dry silicon dioxide;
- Non-passivated samples: native oxide is present on the top of the Si layer.

The buried oxide will be labeled BOX and its thickness t_{OX}. The substrate of the SOI structures is made of p-type NID silicon.

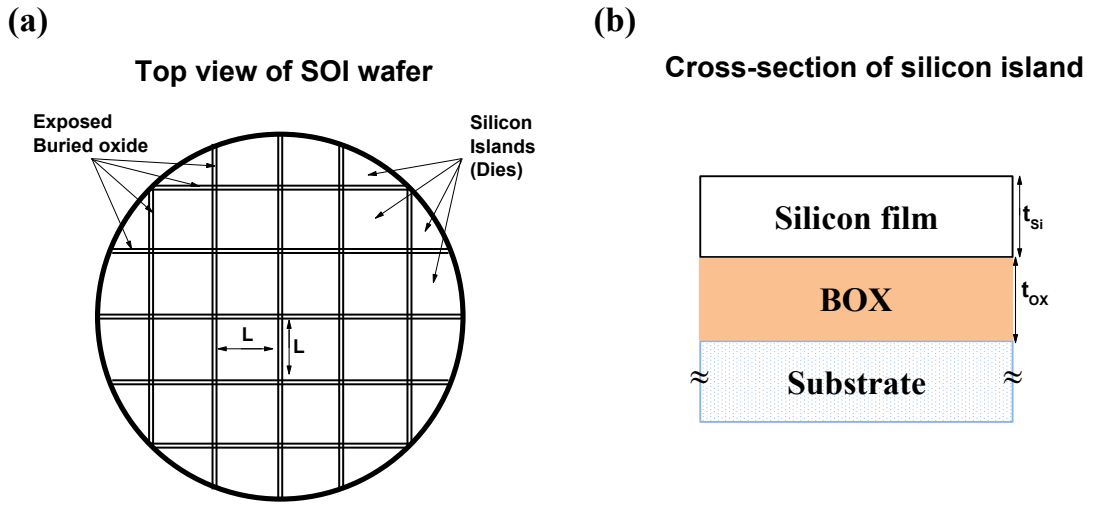

Figure II-3: (a) Top view of the SOI wafer after etching process. *L x L* isolated mesas separated by *2 mm* distance were obtained. (b) Vertical cross-section of a SOI island.

Operation principle

The electrical characterization was achieved using probe stations. Ψ-MOSFET is commonly performed using the adjustable pressure probe station from Jandel®. Four *in-line* needles with *1 mm* inter-distance are present. The pressure (p) can be precisely controlled between *0 g* and *100 g*, for each probe. Since we have no direct information concerning the effective surface where p is applied, the word "*pressure*" may sound incorrect. However, note that it is just a reference to better adjust (and repeat) the probe penetration into the silicon film and no direct physical meaning is given to p magnitude. The probe radius typically used was *40 µm*. The probe was made of WC.

Manual probe stations with micromanipulators can be also used, but the pressure cannot be precisely controlled.

In the following pages the principle to perform static drain current measurements (I_D-V_G and I_D-V_D) will be explained. The particular setups required for capacitance or low-frequency noise measurements will be detailed in the corresponding chapters.

The SOI wafer is placed on a metallic chuck. Assuming that the top silicon film is grounded, the SOI substrate is polarized by V_G applied through the chuck and it *acts* as a gate.

For $V_G = 0\ V$, the electronic bands of the top silicon layer are already bent due to the different Fermi levels between the gate and the top Si film, to D_{it} and to fixed charges in the BOX. The flat band condition is achieved for $V_G = V_{FB}$ (flat-band voltage). For $V_{FB} < V_G < V_T$, the electronic bands bend down with respect to the flat band condition, depleting the p-type Si film. Beyond V_T (threshold voltage), a conduction channel made of electrons is obtained (Figure II-4a). In case of $V_G < V_{FB}$, the conduction channel will be made of accumulated holes (electronic bands bent upwards) (Figure II-4b).

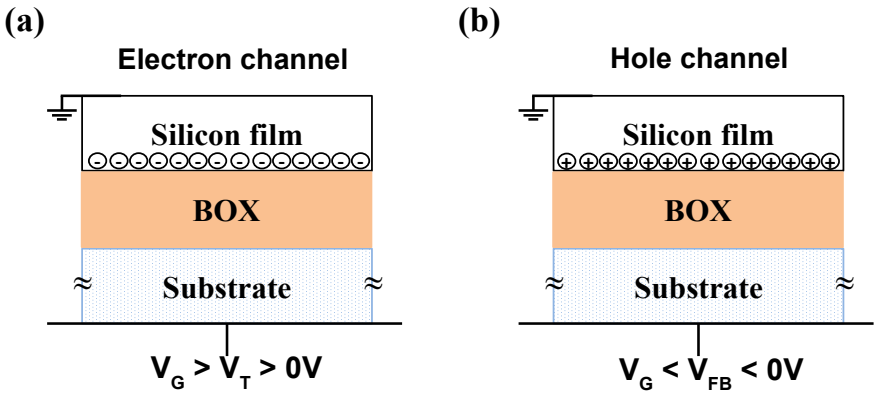

Figure II-4: SOI structure with positive (a) and negative (b) gate biases applied. Hole and electron channels are induced, respectively.

To perform current measurements, one of the two adjustable pressure probes placed on the silicon surface will act as drain, while the second one will be grounded. For symmetry reasons, the two probes have the same pressure. *p* is a major parameter to achieve good characteristics: if it is too small, Schottky barriers are obtained. In case of too large pressures, the probes can reach the BOX, damaging it and making the die not suitable for any further analysis [65].

The drain current (I_D) between the source and the drain contacts is obtained applying a bias ($V_D > 0\ V$).

The first step is to verify if the contacts are Schottky or ohmic. In Figure II-5a, the drain current is measured as a function of V_D in case of positive ($V_G - V_T > 0\ V$, plain symbols) and negative ($V_G - V_{FB} < 0\ V$, empty symbols) overdrive gate voltage. Linear I_D-V_D dependency is found in both cases confirming the presence of ohmic contacts for both electrons and holes. Most of the extraction techniques (such as I_D-V_G or low-frequency noise) require measurements in the linear region, where V_D has no impact on the extracted parameters. However, to avoid parasitic effects due to too large electric field in the channel, we always used drain bias between *100 mV* (low-frequency noise analysis) and *200 mV* (static I_D-V_G) (see again Figure II-5a).

For material parameter extractions, I_D-V_G measurements are required. Figure II-5b shows an example of I_D measured as a function of gate bias (empty symbols). Since the source and drain are metallic (instead of highly doped regions as in MOSFET) electrons (for $V_G > 0$) and holes (for $V_G < 0$) can be collected. The analysis of both types of carriers is therefore possible.

The transconductance ($g_m = dI_D/dV_G$) as function of gate bias (line) is also traced in Figure II-5b. The shape is similar to the one in MOSFETs.

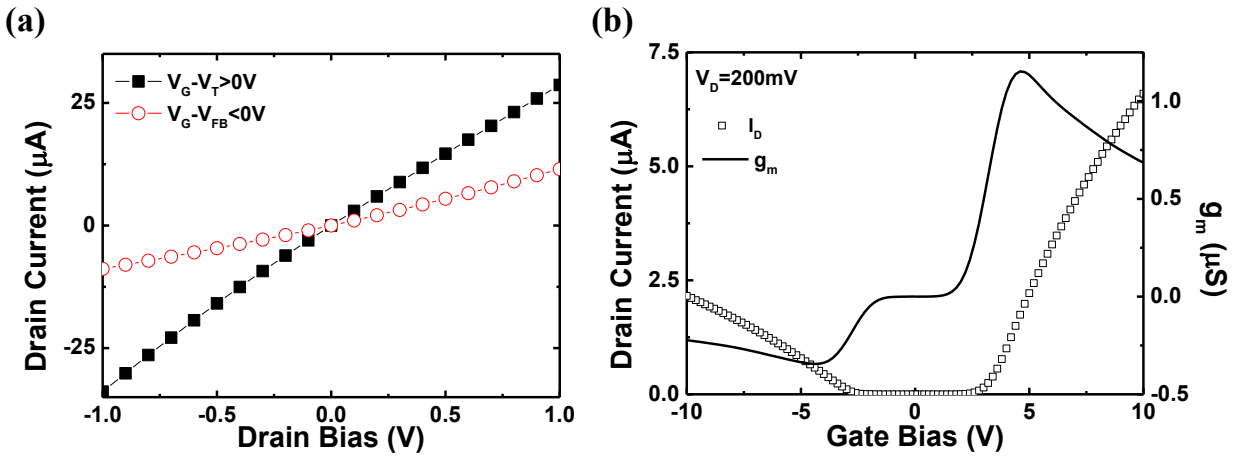

Figure II-5: (a) I_D versus V_D performed on the same die in case of positive (plain symbols) and negative (empty symbols) overdrive bias. (b) Drain current (empty symbols) and transconductance (line) as a function of gate bias. The SOI structure had *88 nm* top silicon film thickness and *145 nm* BOX thickness and it was non-passivated.

Parameter extraction procedure

In case of fabricated transistors with width W and length L, the drain current measured in linear regime is directly proportional to the applied V_G and V_D [5]:

$$I_D = \frac{W}{L} \cdot C_{OX} \cdot \mu_{eff} \cdot (V_G - V_T) \cdot V_D \tag{II.3}$$

where C_{OX} indicates the gate oxide capacitance defined as ε_{OX}/t_{OX}, with ε_{OX} the oxide permittivity. The effective mobility μ_{eff} takes into account the first order attenuation factor θ_1 due to access resistance R_{SD} impact [56]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 \cdot (V_G - V_T)} \tag{II.4}$$

where μ_0 is the low-field mobility. The transconductance g_m is defined as:

$$g_m = \frac{dI_D}{dV_G} = \frac{W}{L} \cdot C_{OX} \cdot \frac{\mu_0}{\left[1 + \theta_1 \cdot (V_G - V_T)\right]^2} \cdot V_D \tag{II.5}$$

To extract the low-field carrier mobility from I_D-V_G characteristics, erasing the effect of access resistance, the Y function method is largely used in MOSFET [66]. Using Eqs. (II.3) and (II.5), the Y function can be written as:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L} \cdot \mu_0 \cdot C_{OX} \cdot V_D} \cdot (V_G - V_T) \tag{II.6}$$

The same equations are valid also in Ψ-MOSFET with two adjustments:

- The *W/L* ratio is defined by the so called geometrical factor f_G obtained by comparison of *4*-probes and two needles configuration [47]:

$$f_G = \frac{W}{L} = 0.75 \tag{II.7}$$

  Recent works have shown that small die areas could lead to f_G variation [67]–[69]. In this work, large dies with respect to the inter-probe distance were used to avoid geometrical factor incertitude [70]. They will be detailed in the next section.
- In case of $V_G < 0\ V$, a hole channel is induced (Figure II-5). The same equations remain valid but V_{FB} must replace V_T; μ_0 and μ_{eff} represent the hole mobility.

Figure II-6a presents the Y function computed from the data in Figure II-5b. In strong inversion (or accumulation) regime, the Y function is linearly dependent with respect to V_G (Eq. (II.6)).From the linear fit, the intercept with the *x*-axis yields V_T or V_{FB}, while the slope is directly proportional to the square root of the low-field mobility.

As for MOSFET, the attenuation factor θ is defined as [66]:

$$\theta = \frac{\dfrac{I_D}{g_m \cdot (V_G - V_T)} - 1}{V_G - V_T} \tag{II.8}$$

θ should be constant in strong inversion (or accumulation) regime (see Figure II-6b) and the limit to high gate bias values leads to the calculation of the first-order attenuation factor θ_1. This allows the computation of the access resistance [66]:

$$R_{SD} \cong \frac{\theta_1}{f_G \cdot C_{OX} \cdot \mu_0} \tag{II.9}$$

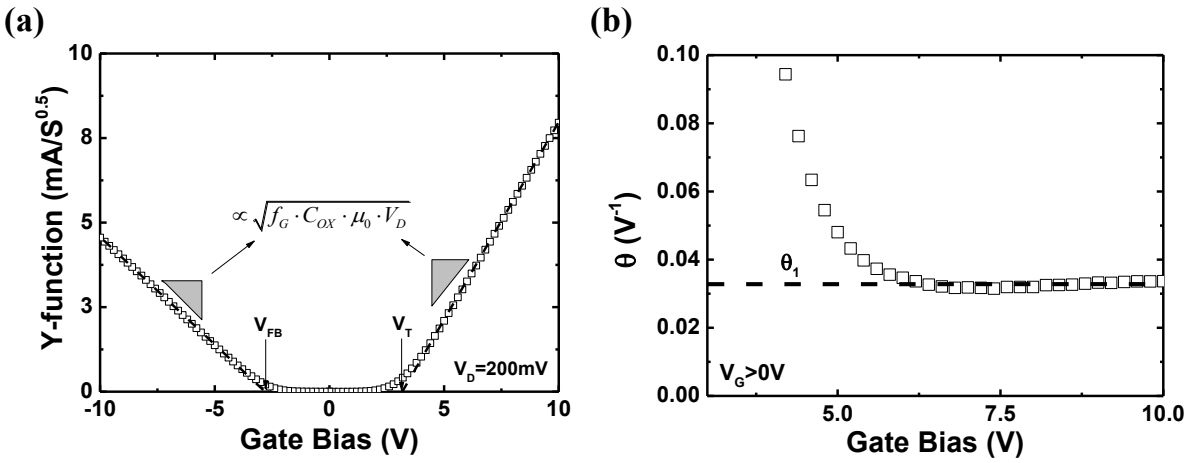

Figure II-6: (a) Y function versus gate bias (data from Figure II-5a). The slope of the linear fit allows μ_0 calculation, while the intercepts with the *x*-axis lead to V_T and V_{FB}, respectively. (b) θ as a function of V_G; in strong inversion regime the constant value θ is θ_1.

The slope of I_D in logarithmic scale versus gate bias under threshold voltage (or $V_G > V_{FB}$ for holes channel) leads to the subthreshold swing (S_s) which gives access to D_{it} (interface traps density) [5]:

$$S_s = 2.3 \cdot \frac{k \cdot T}{q} \cdot \left(1 + \frac{C_{Si} + q \cdot D_{it}}{C_{OX}}\right) \tag{II.10}$$

where the top silicon film capacitance is $C_{Si} = \varepsilon_{Si}/t_{Si}$. ε_{Si} is the silicon permittivity. Note that in SOI structures, two interfaces are present: one between the top silicon film and the BOX (called bottom interface) and a second one at the top surface of the silicon film (called top interface). Both of them can contribute to D_{it} via coupling effects. In case of thick t_{Si}, the coupling is low and D_{it} is dominated by the contribution of the bottom interface. In ultra-thin silicon layers (< *20 nm*) stronger coupling is present and D_{it} gives an effective value of the contribution of both interfaces. Some models [49], [71], based on the double gate approach [72], were proposed to separate the defects contribution coming from the top silicon film-BOX interface and the traps placed on the surface of the Si layer.

Before applying these extraction procedures to evaluate material properties (μ_0, V_T, V_{FB}, D_{it}, etc.), we must define the best measurement setup and experimental parameters.

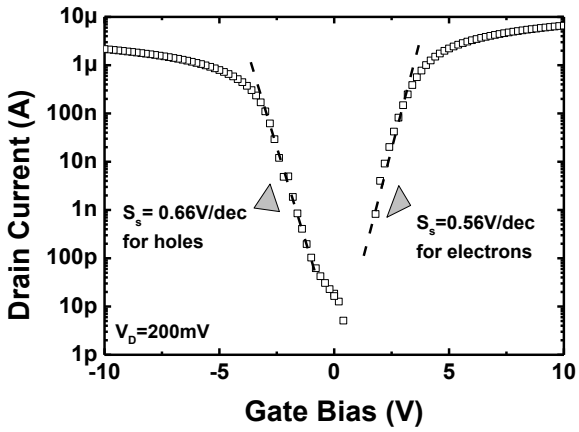

Figure II-7: Drain current in semi-logarithmic scale versus gate bias. The slopes of the linear regions lead to the estimation of subthreshold swing for holes and electrons. Same data as in Figure II-5a.

II.3 Impact of measurement

In this section we discuss the precautions on the measurement setup that may reduce parasitic effects. The importance of choosing good measurement times is presented in Sec. II.3.1. The role played by the back contact is addressed in Sec. II.3.2, while the impact of adjustable pressure probes on the characteristics is pointed out in Sec. II.3.3. Section II.3.4 shows the role of the quality of the top silicon film surface.

II.3.1 Measurement time setup

In order to avoid transient effects and reduce noise, some measurement parameters have to be optimized [33]:

- *Hold time*: it is the time before starting the first measurement point and it must be long enough so that the structure is in equilibrium conditions at the beginning of the characterization. Used values range: *1-100 s*;
- *Delay time*: it is the time between two consecutive measurement points and it must be long enough to avoid any transient effects due to out-of-equilibrium state. A too long delay time can stress the device. All our measurements were obtained using a delay time between *0.4 s* and *2 s*.
- *Integration time*: the value obtained for each bias point is computed by integrating several measurements performed by the instrument at the same biasing condition. "*Short*" integration time means very short integration time range. The analysis is fast but usually the curves are noisy due to trapping/detrapping phenomena induced by surface defects. The use of "*long*" integration time reduces the noise on the characteristics becaue the structure is close to equilibrium condition; but the measurement is more time consuming. In this work, "*medium*" integration time was used for SOI structure with $t_{Si} = 88\ nm$, while "*long*" integration time was adopted in case of ultra-thin Si layers ($t_{Si} < 20\ nm$).

II.3.2 Quality of back contact

In Ψ-MOSFET configuration, V_G is directly applied on the structure through the chuck. Hence, the quality of the "*back contact*" (contact between the back of the SOI substrate and the metallic chuck) may affect the obtained characteristics. This problem never arises in case of fully fabricated transistors, because metallic contacts are used.

Two different cases will be investigated:

- *Air contact*: the wafer is just placed on the metallic chuck. No particular precautions are used to improve the contact;
- *Vacuum contact*: a vacuum system is used to "*stick*" the SOI to the metallic surface. This avoids any possible parasitic contributions due to poor contact.

Figure II-8a shows the drain current versus gate bias on SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness. The top surface was non-passivated. The characterization was performed with (empty symbols) and without (plain symbols) vacuum system. The results obtained on SOI structure with the same t_{OX} but thinner silicon layer (*12 nm*) are presented in Figure II-8b. Variation of V_T and S_s are obtained in both cases, and there are stronger for the thinner silicon film. Vacuum system will be always used to avoid parasitic effects. In the chapter of split-CV measurements we will show that the vacuum contact is even more critical.

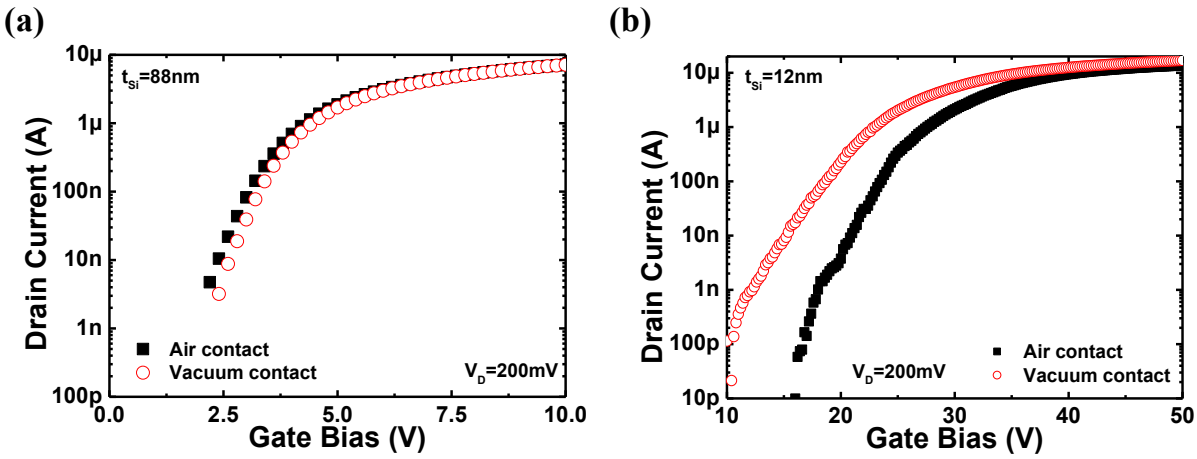

Figure II-8: Measured drain current versus gate bias in *88 nm* (a) and *12 nm* (b) thick SOI film. The buried oxide was in both cases of *145 nm* and the top surface non-passivated. Analysis performed without (plain symbols) and with (empty symbols) vacuum for the back contact.

II.3.3 Role of the probes

The probes have an important role on the obtained Ψ-MOSFET characteristics. It was proved that R_{SD} is directly related to the probe pressure [65]. Furthermore, the probe position on the silicon surface can affect f_G value [67], [68]. Several aspects will be addressed to clarify these effects and how they limit the extraction.

Probe choice

The Jandel® station has four *in-line* probes. In Ψ-MOSFET configuration only two probes are used, thus it is possible to choose among the four needles. We mainly considered the case with $d = 1\ mm$.

Figure II-9a shows the measured I_D as a function of V_G using different needles. Curves match for low V_G but for very large gate bias some differences are present. In this region, R_{SD} (which is probe related) becomes relevant, inducing I_D variations. The corresponding Y functions are shown in Figure II-9b. The impact of access resistance is removed in this case (see Eq. (II.6)) and the curves superpose. Thus, the choice of the probe is not critical in case of I_D-V_G characterization analyzed using the Y function.

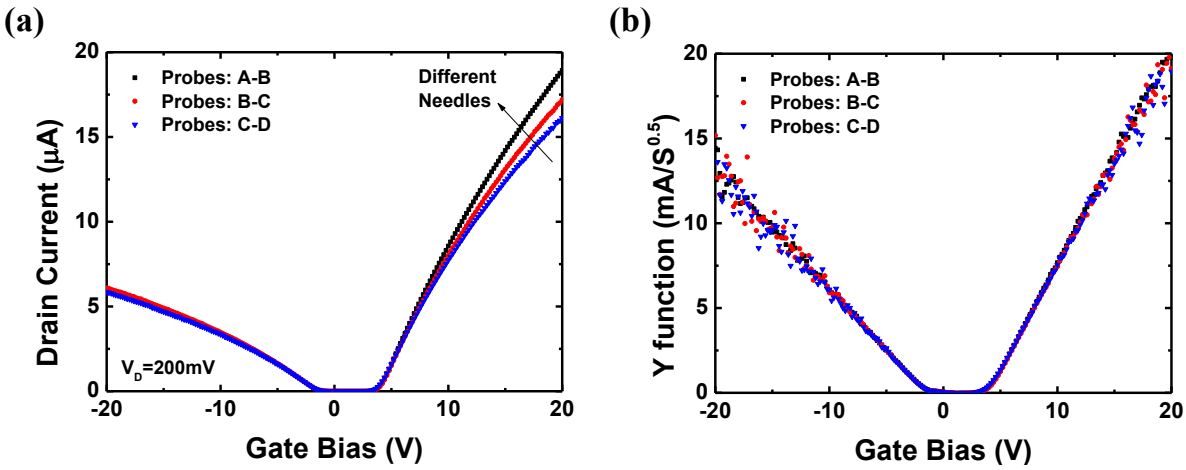

Figure II-9: Measured drain current (a) and Y function (b) versus gate bias on the same SOI structure as in Figure II-8a. Different combinations of probes were used for the analysis. The inter-probe distance was kept constant to *1 mm*.

Probes position

Border effects influence the pseudo-MOSFET measurements because they can affect f_G [67]–[69]. To verify if the use of vacuum system attenuates their impact, several characterizations were performed on the same die changing the position of the probes. The same needles with the same pressure were used. The obtained I_D versus V_G are shown Figure II-10a. The corresponding positions on the silicon surface are represented schematically in the inset. Very close to the edges, the current flow is affected by border effects decreasing the measured I_D value [67]. The corresponding Y functions versus gate bias are shown in Figure II-10b and the computed low-field mobilities are reported in Table II-1. In case of $V_G > 0\ V$, the mobility measured close to the edges is underestimated. In the worst case, the impact is lower than *10 %*. Even smaller impact is found in case of hole mobility.

μ_0 cannot change in an homogenous material according to the contacts position. The different values of μ_0 are due to variation of the geometrical factor (lower than *10 %*). In conclusion, placing the probes at the center of the structure, makes f_G variation negligible.

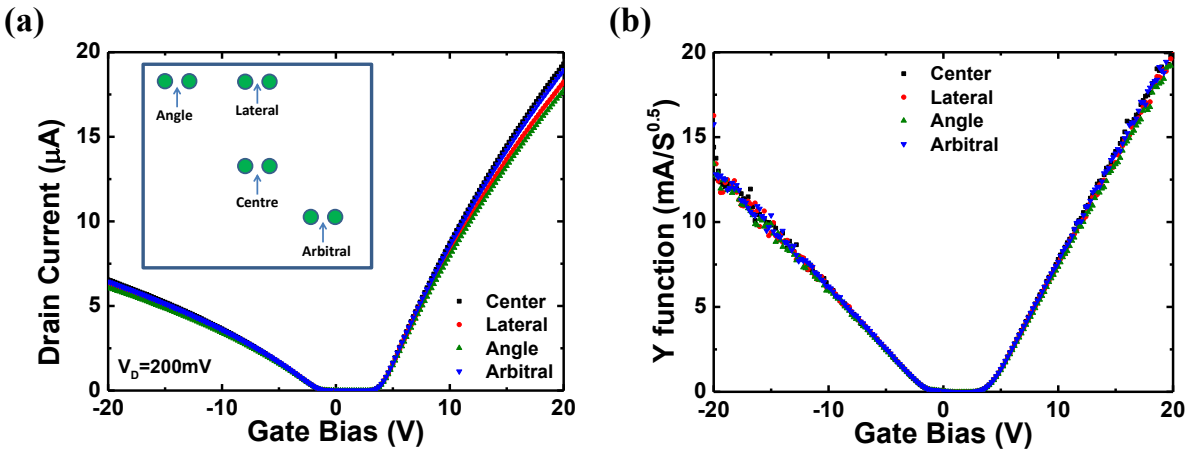

Figure II-10: Drain current (a) and Y function (b) versus gate bias for different probe positions. The SOI structure had *88 nm* thick top silicon film and *145 nm* BOX. The top surface was non-passivated. The die size *L* was *8 mm*. The inset in Figure II-10a presents the corresponding probe position on the silicon surface.

Position	μ_0 *electron* (cm^2/Vs)	μ_0 *hole* (cm^2/Vs)
Center	460	150
Lateral	442	149
Angle	431	143
Arbitral	460	152

Table II-1: Low-field mobility for electrons and holes computed from data in Figure II-10b for different needle positions.

Probes pressure

The impact of probes pressure was already studied in pseudo-MOSFET [65], [68], but without vacuum. Figure II-11 shows the measured I_D (a) and Y function (b) as a function of V_G for different p. The needles were placed on the top silicon film using the lowest pressure. Next, p was gradually increased step by step, without moving the probes. Larger pressure leads to stronger probe penetration into the silicon film [65]. The higher the pressure, the higher the measured drain current due to an improved contact (lower R_{SD}). Y functions superpose and are stable as soon as the pressure is sufficient to have an acceptable contact (here $p > 60\ g$).

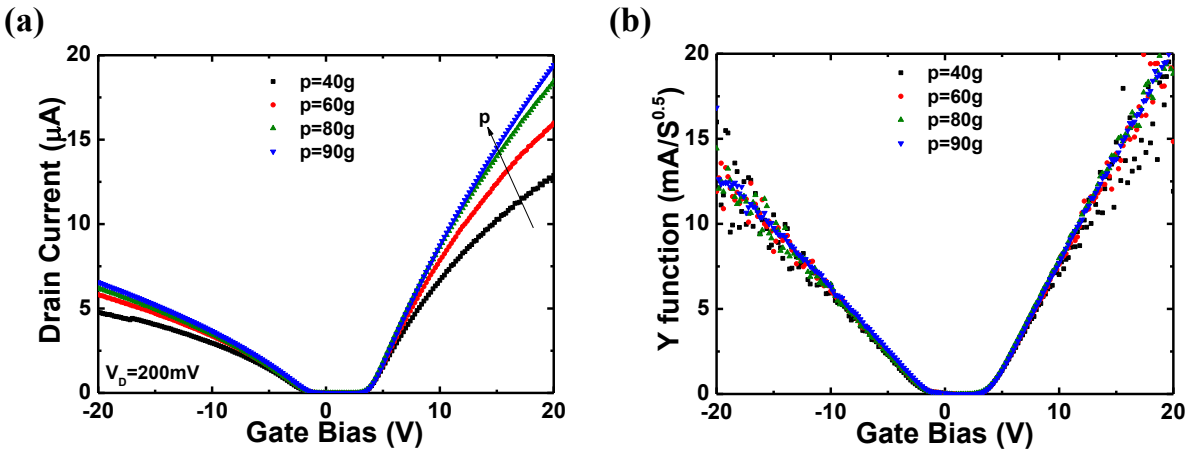

Figure II-11: (a) I_D versus gate bias in case of different probe pressure. The SOI structure had *88 nm* top silicon film and *145 nm* BOX. Non-passivated top surface was used and *L = 5 mm*. The corresponding Y function is computed in Figure II-11b.

Mobility and R_{SD} variation with p are reported in Table II-2, for electrons and holes. Note that pressure effect is much stronger in case of $V_G > 0\ V$ (electrons) than for the holes, where only one point ($p = 60\ g$) is slightly different from the other values. However, despite a pressure variation higher than $\approx 40\ \%$, the mobility change is less than $\approx 10\ \%$. Once the needles have sufficiently penetrated into the silicon film to contact the channel ($p = 60\ g$ in this case), p has only a low impact on μ_0 thanks to the Y function method that removes R_{SD} effects.

Pressure (g)	μ_0 *electron* (cm^2/Vs)	R_{SD} *electron* ($k\Omega$)	μ_0 *hole* (cm^2/Vs)	R_{SD} *hole* ($k\Omega$)
40	420	7.5	147	22
60	449	5.1	128	11
80	460	3.3	150	13
90	461	2.6	153	12

Table II-2: Low-field mobility of electrons and holes computed from Figure II-11b and corresponding R_{SD} for different probe pressures.

Pressure of the probe and vacuum contact

In the previous section (Se. II.3.1) it was proved that the use of vacuum contact is mandatory in case of ultra-thin silicon film. Does the vacuum affect also the mobility-pressure trend?

To answer the question, SOI structure with ultra-thin silicon film (*12 nm*) and thick BOX (*145 nm*) was characterized using different probe pressure. Table II-3 shows the extracted low-field electron mobility obtained from characteristics measured with and without vacuum back contact for different probe pressure. p variation of $\approx 40\ \%$ induces almost $20\ \%$ μ_0 shift using vacuum back contact. In case of standard configuration, the variation is higher than $70\ \%$, proving the importance of using the vacuum system, especially for ultra-thin films.

Pressure (g)	μ_0 (cm^2/Vs) *vacuum*	μ_0 (cm^2/Vs) *no vacuum*
40	443	195
50	462	309
60	426	454
70	509	713

Table II-3: Measured low-field mobility for different *p* and $V_G > 0\ V$. Characterization performed on SOI wafer with *12 nm* top silicon film and *145 nm* BOX. The top surface was non-passivated. Comparison between measurements obtained with and without vacuum.

Radius and probe material

Our Jandel® station has tungsten carbide (WC) probes. Their radius is of *40 µm*. To investigate the impact of the probe radius R_0, we used a manual probe station. The needles were made of WC and they had $R_0 = 12\ \mu m$. The inter-probe distance was kept constant: $d \approx 1mm$.

Figure II-12 shows the measured drain current (a) and corresponding Y function (b) versus gate bias in case of Jandel® station (plain symbols) and manual probe station (empty symbols). The corresponding parameters extracted using Y function method are reported in Table II-4. The obtained electron and hole mobilities are lower in case of sharper tip, due to possible f_G and R_{SD} variation. Note that in manual probe station the probe pressure cannot be precisely adjusted. Agreement is found for threshold voltage, while a V_{FB} shift is measured. Thus, the probe radius has a sizeable effect on the characteristics and the extracted physical parameters [33], [68].

Additionally, we show the results obtained using tips made of different material, osmium (Os) in this example. The probe radius was *12 µm*. The corresponding measured current is shown in Figure II-12 (continuous line) and the extracted values are reported in Table II-4. The highest access resistance was found in this case. For $V_G < 0\ V$, non-realistic low μ_0 mobility is measured, probably due to a non-ohmic contact. A clear shift of V_T and V_{FB} is also present. Thus, the extracted parameters are influenced by the probe material work function.

To perform wafer monitoring, it is important to use all the time tips with the same properties and adapted to the characterized material [73]. In this work, all the measurements performed on Si-SiO_2 wafers were obtained using WC tips with $R_0 = 40\ \mu m$.

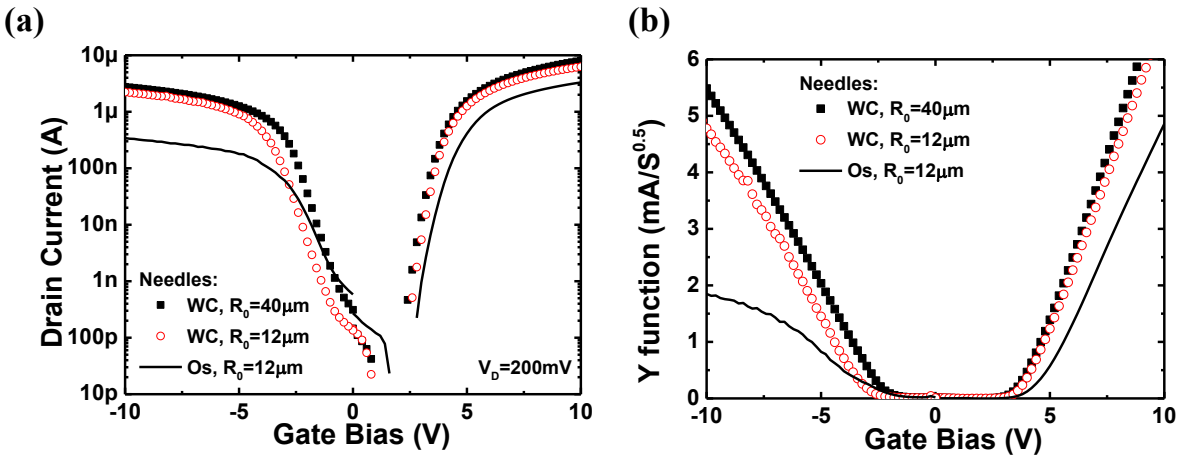

Figure II-12: Drain current (a) and Y function (b) versus gate bias on SOI structure with *88 nm* top silicon film and *145 nm* BOX. The top surface was non-passivated and *L = 2 mm*. Different tips were used: WC with $R_0 = 40\ \mu m$ from Jandel® station (plain symbols), WC (empty symbols) and Os (line) tips with radius $R_0 = 12\ \mu m$ from manual probe station. The inter-probe distance *d* was ≈ *1 mm*.

	WC $R_0 = 40\ \mu m$ *Jandel® (p = 80 g)*	*WC* $R_0 = 12\ \mu m$ *Manual st.*	*Os* $R_0 = 12\ \mu m$ *Manual st.*
μ_0 electron (cm^2/Vs)	412	349	220
V_T (V)	3.9	3.9	4.5
μ_0 hole (cm^2/Vs)	154	137	29
V_{FB} (V)	-2.3	-2.9	-2.3
θ_1 electron (1/V)	0.018	0.033	0.054
θ_1 hole (1/V)	0.089	0.01	-

Table II-4: Extracted parameters from Figure II-12b for different needle properties.

Reproducibility of tests

In pseudo-MOSFET configuration, the source and drain contacts are obtained using probes directly placed on top of the silicon surface. This can be a new source of variability added compared to standard transistors with fabricated metal contacts. In this section we investigated the reproducibility of material characterization (*i.e.*, parameter extraction) obtained using the Y function method on static $I_D(V_G)$ curves. We also defined the order of magnitude of error bars of calculated μ_0 and V_T.

The fitting range of Y function can affect the obtained results: a maximum variation of ± *4.5 %* is obtained for μ_0 and ± *3 %* for V_T.

Figure II-13 shows the extracted low-field mobility (plain symbols) and threshold voltage (empty symbols) for different dies present on the same SOI wafer. The maximum incertitude of μ_0 is around ± *5 %*. Lightly lower variation is found for V_T (± *3 %*). Thus, total error bars around *15 %* represent a good estimation for the measurement technique.

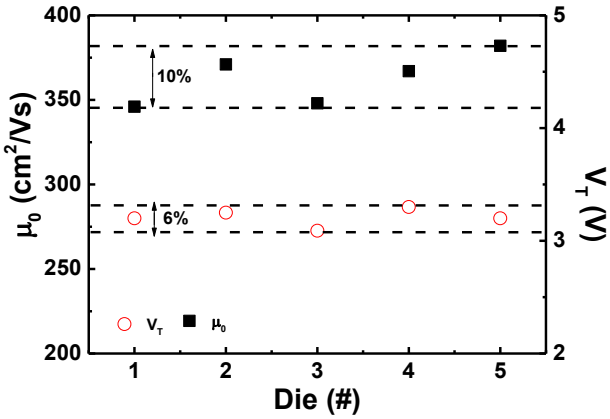

Figure II-13: Extracted μ_0 (plain symbols) and V_T (empty symbols) from different dies present in the same SOI wafer with *88 nm* thick Si film and *145 nm* thick BOX. The top surface was non-passivated.

II.3.4 Passivated top silicon film

In the literature, one of the most frequent approaches to identify to which interface the characterization technique is sensitive, is the comparison between passivated and non-passivated SOI structures. *4 nm* dry oxide grown on the top silicon film improves the corresponding interface quality. Thus, the D_{it} associated to this interface decreases. Figure II-14 shows an example of the measured I_D versus V_G for passivated (plain symbols) and non-passivated (empty symbols) wafers. The different density of defects induces remarkable shifts of V_T, V_{FB} and S_s.

Note that the penetration through the top oxide is easier in case of non-passivated sample (native SiO_2) than passivated one (thermal SiO_2). Thus, different probe pressures have to be used to achieve similar access resistance. In this example, $p = 80\ g$ for non-passivated sample leads to $R_{SD} = 3.4\ k\Omega$, while $p = 100\ g$ on the passivated yields $R_{SD} = 4.5\ k\Omega$.

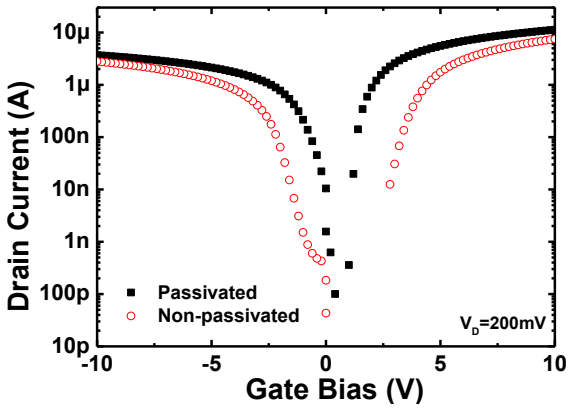

Figure II-14: Drain current as a function of gate bias for SOI structure with *88 nm* top silicon film and *145 nm* BOX. The passivated structure (plain symbols) was measured using $p = 100\ g$, while in non-passivated sample (empty symbols) the tip pressure was *80 g*.

Furthermore, we analyzed by AFM the tip signature left on the silicon surface (see Figure II-15) in passivated (a) and non-passivated (b) samples. The same needle was used but with different pressures: $p = 100\ g$ for passivated and $p = 80\ g$ for non-passivated Si surface. The images were taken with the same scale ($10\ \mu m\ x\ 10\ \mu m$). The measured fingerprints show comparable dimensions ($R_0 \approx 5\text{-}6\ \mu m$) which explains the analogous R_{SD} values. In conclusion, to perform suitable data comparison it is important to measure the characteristics with similar access resistance. p is not directly related to physical quantities.

With time, the probe station may become old and the tips can oxidize. However, adapting the probe pressure, it is possible to achieve low access resistance, thus robust material characterization.

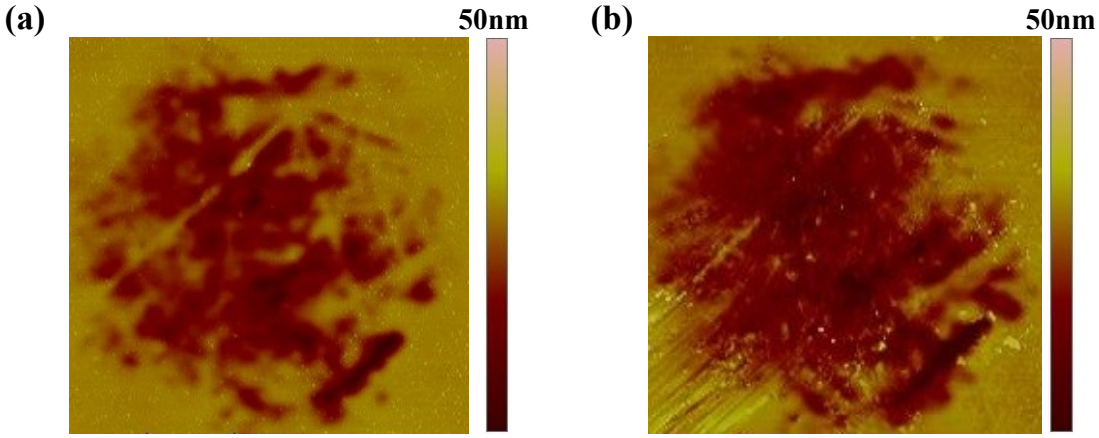

Figure II-15: *10 µm x 10 µm* AFM image for passivated (a) and non-passivated (b) SOI samples. The same tip was used with different pressure: *100 g* in case of passivated and *80 g* for the non-passivated one.

II.4 Extension of Ψ-MOSFET to new materials: III-V-on-insulator

To pursue the transistor scaling down, the use of new materials instead of silicon channel is one of the mainstream topics [28], [74], [75]. Recent researches focus on the fabrication of $In_{53\%}Ga_{47\%}As$ (Indium-Gallium-Arsenide, labeled InGaAs) transistors thanks to their high electron mobility. InGaAs is a compound of elements of IIInd and Vth group, usually labeled as III-V. Different studies have proved the capability to fabricate III-V devices with good performances; high carrier mobility (*2000-3000* cm^2/Vs) and low subthreshold swing S_s (*80-70 mV/dec*) were measured [76]–[80]. However, more research is required to make the fabrication processes of high quality III-V layer compatible with the silicon technology.

In this section, InGaAs layers will be characterized during the several fabrication steps:

- Before film transfer on oxide in Sec. II.4.1 (using Van der Pauw and Hall effects);
- After the transfer on oxide (III-V-OI) using Ψ-MOSFET-like configuration with pressure probes (Sec. II.4.2) and with deposited metal contacts (Sec. II.4.3);
- Fully fabricated transistor (Sec. II.4.4).

II.4.1 Material characterization before bonding

In order to validate the quality of the fabricated III-V before any fabrication process, Hall effect measurements were performed on bulk material. The technique is described in Appendix I. The structure used is shown in Figure II-16a. The InGaAs layer thickness ($t_{III\text{-}V}$) was *160 nm* and it was n-type. It was grown on InP substrate Fe p-doped. The dies had square shapes. Indium (In) droplets were used to contact the III-V layer.

The impact of doping concentration (N_D) on the carrier mobility was investigated. Note that N_D always indicates the electrically active doping concentration (obtained using Hall effect technique, see Appendix I) and not the fabrication target doping. The measured μ_{Hall} versus N_D is shown Figure II-16b. As expected, lower N_D leads to higher mobility. In the literature [81], thicker films were characterized after transfer on xide ($\mu_{Hall} \approx 8000\ cm^2/Vs$ for $t_{III\text{-}V} \approx 450\ nm$). We obtained prominsing mobility values also for thinner films ($t_{III\text{-}V} = 160\ nm$); confirming the reasonable quality of the fabricated layer.

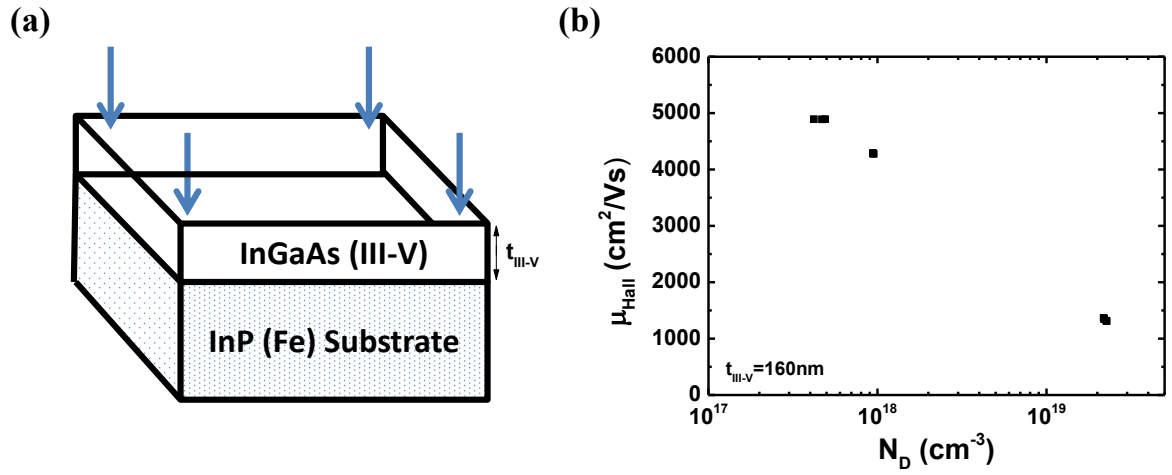

Figure II-16: (a) General shape of III-V layer on InP substrate before bonding. (b) Measured μ_{Hall} versus doping concentration on *160 nm* InGaAs with different doping concentrations.

The impact of $t_{III\text{-}V}$ was also investigated. Three samples of InGaAs were fabricated on InP substrate. The same doping target was implanted: $5{\cdot}10^{17}cm^{-3}$. As previously, the contacts were made of Indium droplets. The measured μ_{Hall} (plain symbols) and doping concentration (empty symbols) are reported in Figure II-17 as a function of $t_{III\text{-}V}$. N_D is also affected by the III-V thickness variation and further research is in progress to explain why the effective doping is smaller in thinner sample.

The Hall mobility decreases with the III-V thickness, due to the stronger coupling between the bottom and top interface [82], [83]. A mobility higher than *3000 cm²/Vs* is measured even in ultra-thin films.

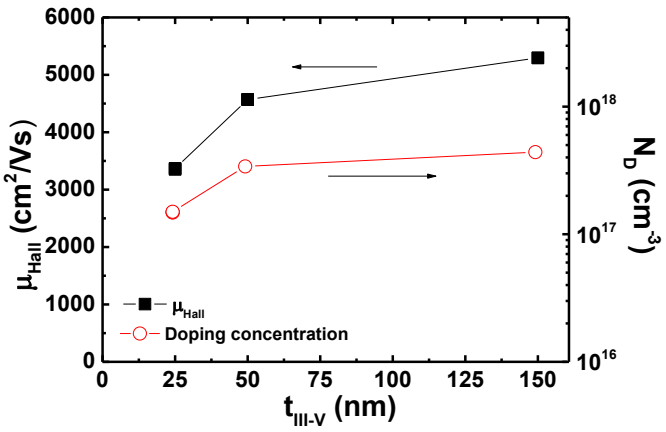

Figure II-17: μ_{Hall} (plain symbols) and doping concentration (empty symbols) as a function of $t_{III\text{-}V}$ for InGaAs layer on InP.

II.4.2 Ψ-MOSFET with pressure probes on III-V-on-insulator (III-V-OI)

In this section, III-V films were characterized after transfer on oxide (III-V-on-insulator). The III-V layer was non-intentionally doped (NID). *5 mm x 5 mm* mesas were fabricated on all the wafers, as described in Figure II-3a. The measurements were performed using the adjustable pressure probe Jandel® station.

In order to verify the capability to characterize InGaAs substrate using Ψ-MOSFET technique, Figure II-18a presents the drain current versus V_D for different gate bias values. The structure had *10 nm* top layer thickness and *110 nm* SiO_2 thickness. I_D changes linearly with V_D for low drain bias and then it saturates. V_G variation induces a normal increase of the measured current. However, even if the curve shapes are similar to the ones obtained in MOSFET, I_D is very low (≈ *nA*) (see Figure II-5a for example). On the same die, the drain current was measured as a function of V_G for different V_D (Figure II-18b). Despite the large magnitude of applied biases (V_D and V_G), the currents measured are still small, suggesting that the Ψ-MOSFET configuration might not be easily adapted to III-V layer.

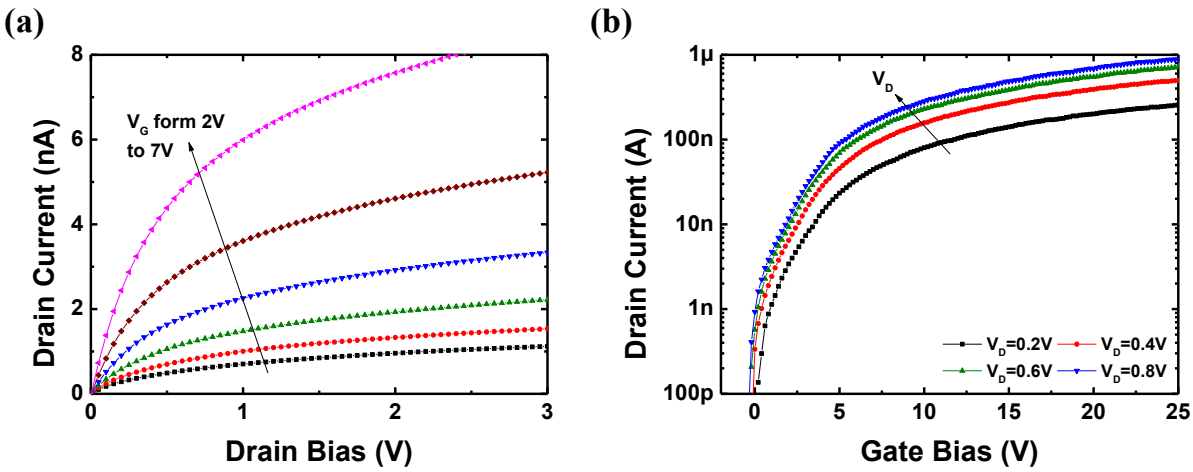

Figure II-18: Measured drain current versus V_D (a) and V_G (b) for different gate and drain bias values, respectively. The structure had *10 nm* III-V layer thickness and *110 nm* SiO_2 BOX thickness.

A low I_D magnitude may be due to high access resistance R_{SD}. In Ψ-MOSFET, the increase of the probe pressure leads to better probe penetration into the silicon film, thus lower R_{SD} (see Sec. II.3.3). Figure II-19a shows I_D versus gate bias for different *p*. The SOI structure had *50 nm* InGaAs thick film and *30 nm* Al_2O_3 BOX. No clear trend is visible.

The limitations may be due to a non-ohmic contact between films and probes. Thus, Figure II-19b presents $I_D(V_D)$ curves obtained with Os needles of *12 µm* radius. The same structure as in Figure II-18 was studied. Thanks to its work function, Osmium is expected to lead to better contacts with the III-V layer [73]. The drain current magnitude still remains very low, making the characterization of III-V in standard Ψ-MOSFET configuration not possible with pressure probes. Consequently, III-V-OI substrates with metal contacts on top were fabricated and their characterization is shown in the next section.

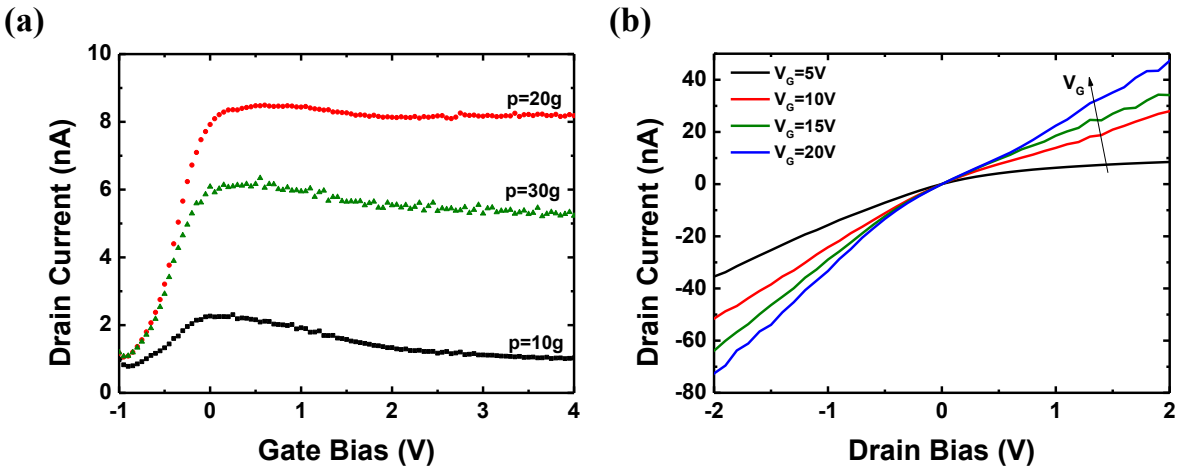

Figure II-19: (a) Drain current versus gate bias for different probe pressure. Structure with *50 nm* III-V layer thickness and *30 nm* Al_2O_3 thickness. (b) I_D versus V_D for different V_G values. Os tips were used on the same structure as in Figure II-18.

II.4.3 Ψ-MOSFET with metal contacts on III-V-OI

Impact of fabrication annealing temperature

In this section, several III-V layers on oxide were characterized to find the best annealing temperature. To succeed on the analysis, one wafer was fabricated (Figure II-20a) and cut in several pieces before annealing. Each piece was annealed using different temperature (T_{an}): *500 ºC* and *600 ºC*. To overcome the limitations found on the characterization of III-V material using the standard Ψ-MOSFET configuration, metal contacts were deposited on the top of the InGaAs layer (alloy of Ti/Au). No particular passivation was performed on top of the III-V film.

Figure II-20b presents the mask used for the lithography. μ_{Hall} and the low-field mobility (μ_0) were measured using the Hall effect and the Corbino configuration, respectively. In case of Corbino contacts the drain contact was placed at the center and the source on the circle surrounding the first contact (Figure II-20c). Applying a back gate bias, the conduction channel is created at the interface between the InGaAs and the BOX. Consequently, I_D can be measured versus V_G (same principle and extraction procedure as for standard Ψ-MOSFET). The Y function method was used to extract μ_0. Using a Corbino structure, the geometrical factor is well defined by the radius of drain contact (R_1) and the distance from the source contact to the center (R_2) [56], [58], [60] (see Figure II-20c):

$$f_G = \frac{2\cdot\pi}{\ln\left(\frac{R_2}{R_1}\right)} = \frac{2\cdot\pi}{\ln\left(\frac{500\mu m}{250\mu m}\right)} = 9.06 \qquad \text{(II.11)}$$

In order to reduce parasitic leakage currents which can limit the characteristics, each structure was isolated by the others through mesa fabrication (lithography and etching of III-V film).

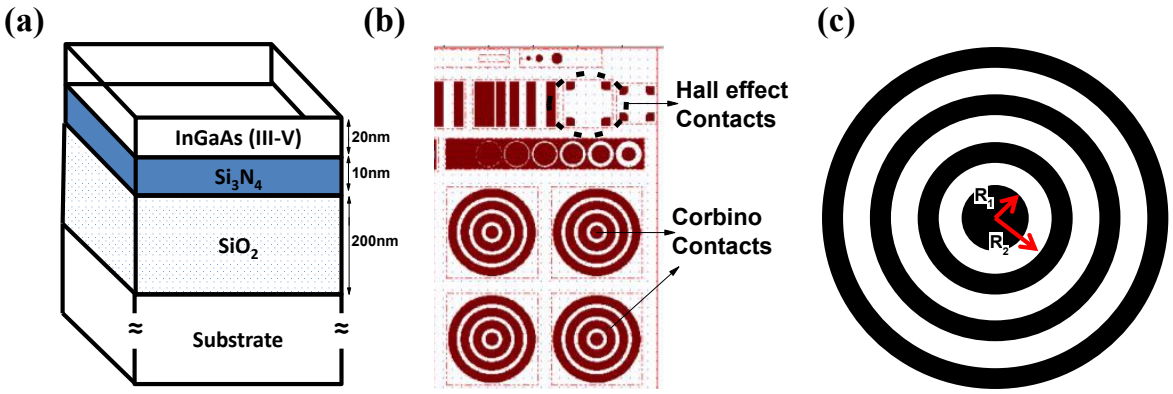

Figure II-20: (a) III-V substrate structure used in this section. Different annealing temperatures were performed on pieces of material coming from the same starting wafer. (b) Layout of the mask fabricated on the III-V layer. (c) Zoom of Corbino structure.

Figure II-21 presents the measured resistivity (empty symbols) and doping concentration (plain symbols) as a function of T_{an}. After low annealing temperature (*500 °C*), the III-V layer is very resistive, while for high T_{an}, ρ abruptly decreases. The doping concentration shows the corresponding trend. Since the samples come from the same wafer, with the same implanted dose, a higher annealing temperature simply activates more dopants.

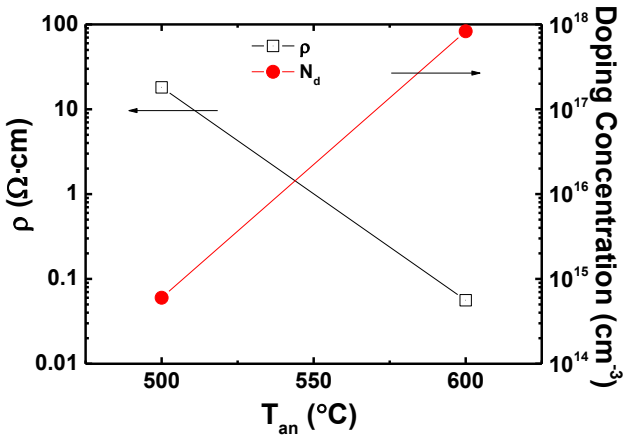

Figure II-21: Measured ρ (empty symbols) and doping concentration (plain symbols) as a function of annealing temperature. Values with ≈ *15 %* of incertitude.

The corresponding Hall mobility (empty symbols) and μ_0 (plain symbols) values as functions of annealing temperature are reported in Figure II-22. The low-field mobility was extracted using the Y function method performed on I_D-V_G characteristic. Unfortunately no working die was found applying V_G on the wafer with T_{an} = *600 °C*. Thus, it was not possible to measure μ_0.

The Hall mobility was obtained without field effect and represents an average value in the film. On the other hand, μ_0 is the electron mobility in the channel which is notoriously smaller than the volume mobility [6].

μ_0 and μ_{Hall} are related by the Hall scattering factor [5], [6]:

$$r_H = \frac{\mu_{Hall}}{\mu_0} \tag{II.12}$$

which depends on the carrier mean free time between collisions. In silicon samples, it is *1.18* when phonon scattering is present and $r_H = 1.93$ for Coulomb scattering.

In our case, the Hall scattering factor is non-realistic (> *100*) due to the leakage current through the BOX. New samples are in preparation to duplicate the experimental results.

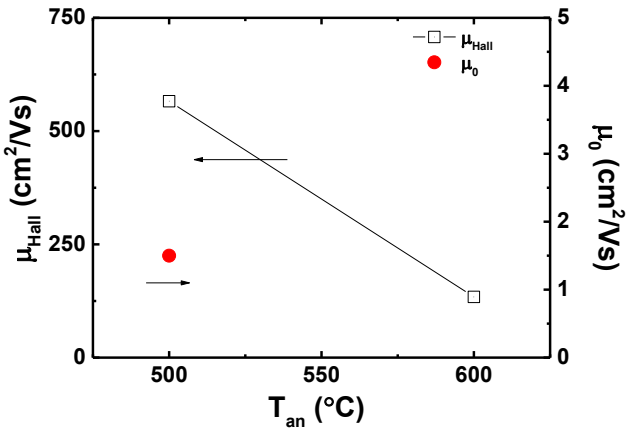

Figure II-22: μ_{Hall} (empty symbols) and μ_0 from Y function (plain symbols) measured as a function of annealing temperature. Measurements performed at ambient temperature.

Mobility evolution with the measurement temperature

In this section we investigated the carrier mobility variation with temperature *T*. The tested structure is shown in the inset of Figure II-23b. The wafer was annealed at *600 ºC* and no passivation was performed in the III-V surface. Note that even if the tested structure is similar to the ones characterized in the previous section, the fabrication process was quite different. Thus, a direct comparison of the obtained values is not possible.

μ_{Hall} and the low-field mobility obtained at room temperature from three different dies are reported in Table II-5. Again, a strong difference between the two characterization techniques is found. In this case the calculated r_H is between *2.7* and *3*, which is still large but more reasonable. Since μ_0 is mostly proportional to $1/t_{III\text{-}V}$, it is dominated by phonon scattering.

Die	N_d (cm^{-3})	μ_{Hall} (cm^2/Vs)	μ_0 (cm^2/Vs)
A	$6.4\cdot10^{17}$	775	285
B	$6\cdot10^{17}$	760	246
C	$6.1\cdot10^{17}$	737	248

Table II-5: Measured N_d, Hall and low-field mobility for three different dies on the same wafer. Structure schematic in the inset of Figure II-23b. T_{an} = *600 ºC*. The measurements were performed at ambient temperature.

To perform the measurements at different temperature T, the contacts prepared for the Hall effects were used. The two needles (source and drain) were placed in two diagonal corners. Thus, I_D flow was measured. Figure II-23a shows the results. Note that the thick BOX requires very large gate bias values to achieve full characterization. However, the range V_G supported by the instrument is $\pm$ *10 V*, thus the characteristics are not complete.

The low-field mobility can be extracted using the Y function method on the measured I_D-V_G characteristics. The geometrical factor is derived comparing the resistivity measured with two probes placed in diagonal contacts and the Van der Pauw technique (Appendix I). Equation (II.2) can be rewritten in a general form as:

$$\rho = f_G \cdot \frac{\Delta V}{I} \tag{II.13}$$

where f_G is a general geometrical factor. The material resistivity is determined using Van der Pauw technique. Hence, applying a current between two diagonal probes and measuring the differential potential ΔV, Eq. (II.13) allows the calculation of f_G. In this case we obtained:

$$f_G = 0.26 \tag{II.14}$$

The mobility measured at *77 K* ($\mu_{0_T=77K}$) are equal to *489* cm^2/Vs, *753* cm^2/Vs and *675* cm^2/Vs for the die A, B and C, respectively. However, since the main interest is to investigate the mobility trend with temperature, the obtained μ_0 were normalized with respect to $\mu_{0_T=77K}$.

The results are presented in Figure II-23b as a function of temperature in logarithmic scale for the three different dies. T decrease leads to higher mobility. In order to identify which scattering phenomena dominates the mobility variations, a linear fit was performed (dashed lines). The slope is between *1.54 dec* and *1.64 dec*. In case of phonon scattering, $\mu_0 \propto T^{-n}$, where n is between *1* and *2* [84]. These results confirm that in our case the measured mobility variation is due to phonon scattering.

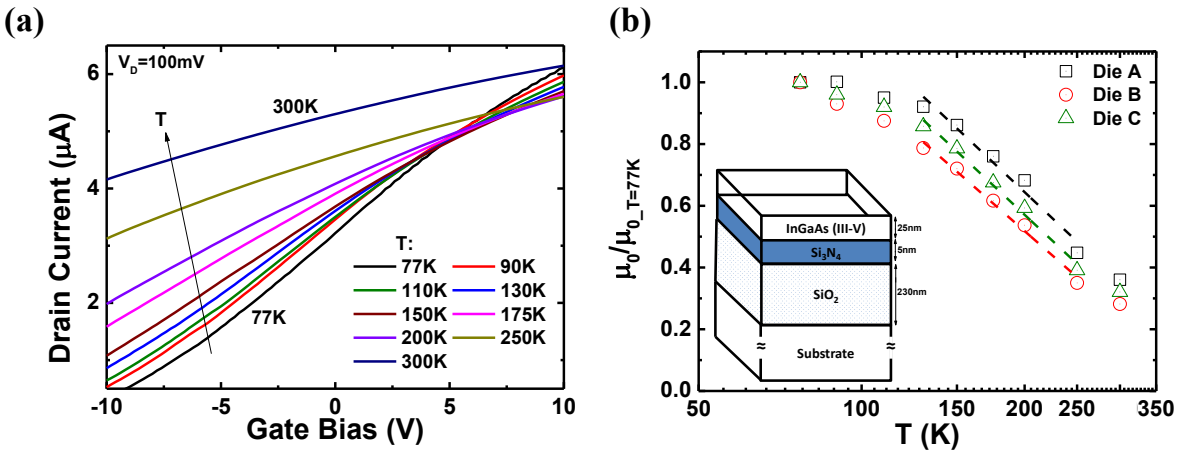

Figure II-23: (a) Measured drain current versus gate bias for different temperatures. (b) Low-field mobility normalized by $\mu_{0_T=77K}$ as a function of T in logarithmic scale for three different dies. Linear fit performed at high temperatures (dashed lines). Inset: schematic of measured III-V-OI structure. T_{an} = 500 ºC.

II.4.4 Preliminary results of III-V transistors

During COMPOSE[3] project [85], preliminary transistors were fabricated on III-V-OI substrate by IBM. Figure II-24 presents an example of measured drain current (plain symbols) and transconductance (empty symbols) versus V_G. The structure was a FinFET on SiO_2, with $L = 40\ nm$ and $W = 2\ \mu m$. The extracted parameters ($\mu_0 = 34\ cm^2/Vs$ and $S_s = 90\ mV/dec$) are not yet good enough from the industrial point of view to integrate the III-V in CMOS production.

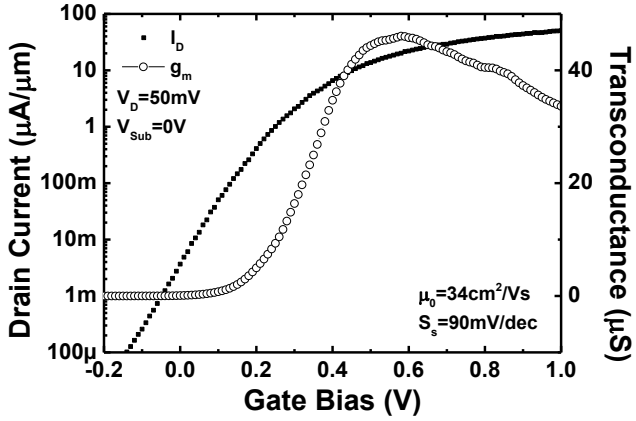

Figure II-24: Drain current and g_m measured versus gate bias obtained from FinFET on oxide. $L = 40\ nm$ and $W = 2\mu m$. The top oxide has ≈ $1.7\ nm$ EOT while the back-oxide was $30\ nm$ of Al_2O_3.

One possibility given by the presence of a buried oxide is the capability to tune the conduction channel with the back gate (V_{back}). Figure II-25a shows the measured I_D versus V_G applying different V_{back}. Remarkable V_T and S_s variations are found due to the strong coupling effect.

Figure II-25b presents the obtained low-field mobility normalized with respect to μ_0 for $V_{back} = 0\ V$ ($\mu_{0_at_0V} = 33\ cm^2/Vs$) versus back gate bias. Using $V_{back} < 0\ V$, the conduction channel is more confined and closer to the interface with the top oxide. Thus, the carriers are more sensitive to the interface defects and the mobility is lowered. On the contrary, for $V_{back} > 0\ V$ the density of free carriers present in the channel is larger and the electron flow is more localized at the middle of the III-V layer, reducing the interface influence. This variation confirms that the poor device performances (low μ_0 and poor S_S) are due to high density of interface defects.

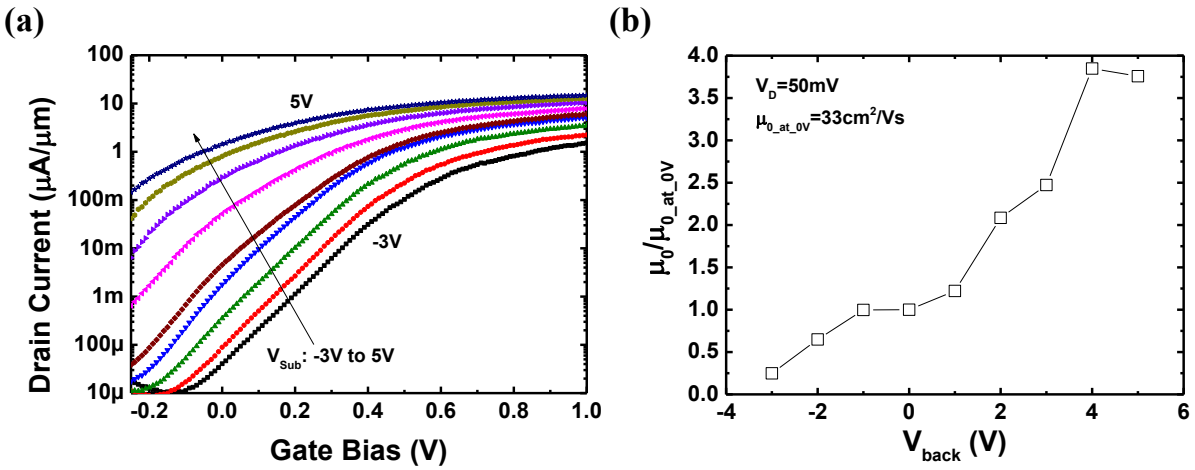

Figure II-25: (a) Measured drain current versus V_G for different back-gate bias. The FinFET on oxide had L = *500 nm* and W = *100 nm*. (b) The corresponding low-field mobility normalized by $\mu_{0_at_0V}$ as function of V_{back}.

II.5 Conclusions and perspectives

This chapter was divided into two main parts: one addressing the standard pseudo-MOSFET characterization of silicon-on-insulator and the second one focused on III-V layers.

The first part contains an exhaustive investigation of Ψ-MOSFET configuration and measurement setup. According to our setup, to achieve sound material characterization it is mandatory to use:

- A proper measurement time setup, in order to avoid out-of-equilibrium state and reduce noise. It is dependent on the characterized SOI structure. Ultra-thin films necessitate longer measurement time than $t_{Si} = 88\ nm$.
- A vacuum back contact, to reduce the presence of parasitic effects. Its use is necessary in case of ultra-thin films. Thanks to this result, it maybe interesting to try new characterization techniques, such as chanrge pumping, and verify the effective impact of substrate capacitance, already investigated in characteristics obtained without using the vacuum system [49], [62].
- The correct probe configuration. The adjustable pressure probes have an important role on static I_D-V_G characterization. The pressure has to be large enough to achieve low access resistance. p can be different in case of passivated and non-passivated samples. Probe choice and position in the silicon film affect I_D-V_G characteristics but the use of Y function method attenuates R_{SD} effects.

III-V materials were also characterized during several fabrication steps: before and after bonding on oxide and fully fabricated transistors. The results show that the unprocessed III-V film quality is high ($\mu_{Hall} > 3000\ cm^2/Vs$), also in case of ultra-thin films. However, the fabrication steps (transfer on oxide and device fabrication) degrade the carrier mobility, probably due to the high density of defects present at the interfaces.

Chapter III:

Split-CV in Ψ-MOSFET

In the previous chapter, a detailed investigation of static characterization on SOI wafers has been performed. This chapter presents the split-CV capacitance technique. The impact of measurement setup will be addressed. Capacitance and conductance curves as a function of gate bias and angular frequency will be shown. A model based on physical equations will be examined to understand the experimental results and important questions concerning the possibility of D_{it} extraction will be answered.

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III.1 Introduction

Characterization methods based on static drain current measurements are powerful but they can have some limitations. For example, the extracted low-field mobility in very short MOSFETs is proportional to the gate length and the two parameters cannot be separately obtained without making hypothesis; this is inconvenient especially for advanced MOSFETs in which the effective electric length is not the design length [86]. Furthermore, static characterization does not allow direct measurement of effective carrier mobility (μ_{eff}). Split-CV configuration is largely used to overcome these problems. Originally, the configuration has been proposed by Koomen [87] to characterize interface trap density and substrate doping concentration in silicon MOSFET devices. Next, it has been applied for the study of carrier mobility by Sodini *et al.* [88]. Nowadays it is used for the investigation of the fabrication process impact on μ_{eff} [89]. The technique is based on two capacitance measurements (gate-to-channel C_{GC} and gate-to-substrate C_{GS}) plus the I_D-V_G characteristic. Each of the capacitance terms gives access to different parameters/information: effective carrier mobility and effective electric field (E_{eff}).

III.1.1 Split-CV in MOSFET devices

Gate-to-channel capacitance and effective carrier mobility

For standard silicon n-type MOSFETs, the measurement setup for C_{GC} capacitance is shown in Figure III-1a. The gate is connected to high potential while the source and the drain contacts are connected together to low potential. The substrate is grounded. Static bias (V_G) is applied to the gate in order to create the conduction channel at silicon-oxide interface. The capacitance measurements require a small *a.c.* bias variation (δV_G) of a frequency (f) added to V_G. Figure III-1b shows typical low frequency C_{GC} shape as a function of gate bias on a n-type transistor. Note that the definition of low or high frequency is mostly related to the properties of the device under test. For low values of gate bias, the obtained capacitance is negligible, since no free carriers are present in the conduction channel. Close to V_T, the capacitance starts to increase until it saturates in the strong inversion regime.

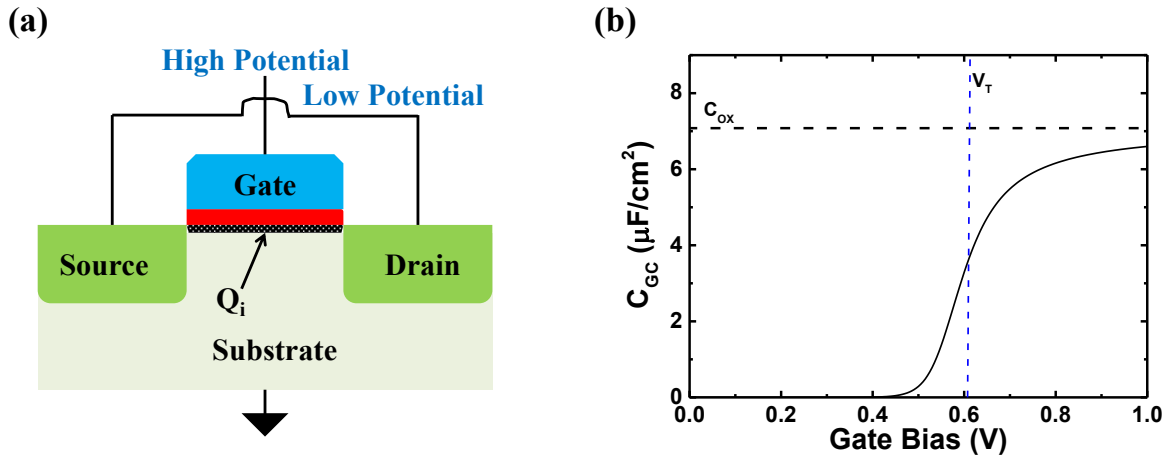

Figure III-1: (a) Split-CV setup in case of gate-to-channel capacitance for MOSFET device. (b) Typical low frequency C_{GC} shape versus gate bias in case of n-type transistor. C_{OX} added as eye-guide.

The saturation value (C_{GC_max}) corresponds to the device area ($S = W{\cdot}L$) times the gate oxide capacitance (C_{OX}), which is inversely proportional to the oxide thickness (t_{OX}) [56]:

$$C_{GC_max} = C_{OX} \cdot S = \frac{\varepsilon_{OX}}{t_{OX}} \cdot S \qquad \text{(III.1)}$$

where ε_{OX} is the silicon dioxide permittivity. The integration of C_{GC} leads to the calculation of the inversion charge density (Q_i) present in the channel:

$$Q_i(V_G) = \frac{1}{S} \cdot \int_{V_{gacc}}^{V_G} C_{GC}(u)du \qquad \text{(III.2)}$$

where V_{gacc} is the low limit of gate bias, usually taken in the accumulation regime (when $C_{GC} \approx 0\ F$).

Furthermore, a static I_D-V_G characterization on the same device allows calculating the effective carrier mobility:

$$\mu_{eff}(V_G) = \frac{I_D(V_G)}{\frac{W}{L} \cdot Q_i(V_G) \cdot V_D} \qquad \text{(III.3)}$$

This result emphasizes the main interests of split-CV technique: μ_{eff} extracted by direct measurement instead of the recalculated values typically obtained from Y function method.

Besides the interests of this technique, two precautions need to be taken [90]:

- Device surface: if the device is too small, the characterization instruments reach the resolution limits and they cannot measure the channel capacitance;
- Eventual V_T shift between capacitance and current measurements: this is a measurement artefact and it requires shift adjustment between C-V and I-V characteristics for μ_{eff} calculation. The subject is still under investigation in the micro-electronic community [90].

Gate-to-substrate capacitance and effective electric field

In order to measure the gate-to-substrate capacitance C_{GS}, source and drain contacts have to be grounded, the substrate is connected to low potential and the gate to the high one (Figure III-2a). C_{GS} contribution comes from the depletion charges (Q_{Dep}). Q_{Dep} is directly proportional to the doping concentration (N_a) and the depletion width of the silicon film (x_{Dep}):

$$Q_{Dep} = q \cdot N_a \cdot x_{Dep} \tag{III.4}$$

C_{GS} can be mathematically obtained by the derivative of the depletion charge with respect to the gate bias:

$$C_{GS} = \frac{\delta Q_{Dep}}{\delta V_G} = q \cdot N_a \cdot \frac{\delta x_{Dep}}{\delta V_G} \tag{III.5}$$

Figure III-2b shows the typical gate-to-substrate capacitance shape versus gate bias for n-type transistor (p-type substrate). Before flat-band voltage, the accumulation charges dominate and $C_{OX} \cdot S$ is measured. No depletion region is present. For $V_G > V_{FB}$, no free charges are present in the channel and the x_{Dep} changes proportionally to V_G until C_{GS} becomes negligible at V_T [5].

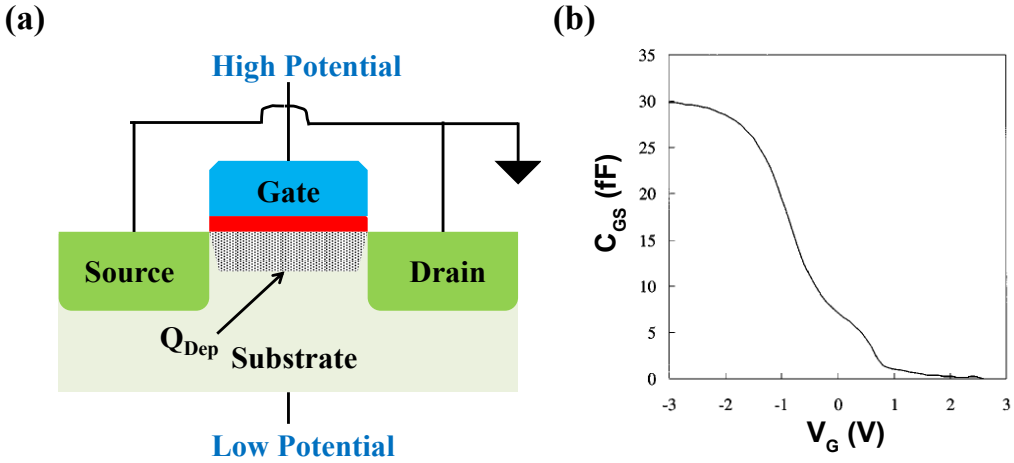

Figure III-2: (a) Setup for gate-to-substrate capacitance measurement. (b) Typical C_{GS} versus gate bias in case of n-type transistor [91].

Following the same approach as in Eq. (III.2), the integration of C_{GS} leads to the depletion charge density magnitude:

$$Q_{Dep}(V_G) = \frac{1}{S} \cdot \int_{V_{FB}}^{V_G} C_{GS}(u)du \tag{III.6}$$

where V_{FB} is the flat-band voltage.

Using the inversion charge Q_i in Eq. (III.2) and the depletion charge in Eq. (III.6), it is possible to obtain the effective electric field E_{eff} [92]:

$$E_{eff} = \frac{\eta \cdot Q_i + Q_{Dep}}{\varepsilon_{Si}} \tag{III.7}$$

where η is the ideality factor. It is equal to *1/2* in case of electrons and to *1/3* in case of holes [93].

III.1.2 Split-CV in pseudo-MOSFET configuration: state of the art

The capability to directly measure the effective carrier mobility in fully fabricated MOSFETs makes split-CV technique very interesting also to monitor the quality of bare SOI substrates. Nayak *et al.* [94] have presented characteristics obtained on high resistive wafers. Their use of metal contacts on the film inducing Schottky barriers makes the mobility extraction complicated. Diab *et al.* [53] and Fernandez *et al.* [54] have demonstrated that split-CV capacitance measurements can be performed using pseudo-MOSFET configuration. In this case, pressure probes lead to ohmic contacts between the conduction channel and the source and drain. Thus, the extraction of material properties becomes easier.

The following sections will focus on split-CV characteristics performed with Ψ-MOSFET. A description of measurement setup is presented below.

Measurement configuration

Two types of probe stations already presented for static characterization measurements are used here: Jandel® station with pressure control probes and a classical probe station from Karlsuss® with manual probes, without pressure control. The SOI wafer is positioned on a metallic chuck that acts as a gate. One (or more) adjustable pressure probe is (are) placed on the top silicon film and connected to low potential (Figure III-3a). All the measurements have been performed using either the Agilent E4980A® or the Agilent 4284® LCR meter. The chosen equivalent electric circuit configuration is a capacitance (C_{m_split}) in parallel with a conductance (G_{m_split}). In this way it is possible to separate the dispersive effects of the resistance ($1/G_{m_split}$) from the capacitance characteristics [95], [96]. Figure III-3b shows the applied gate bias signal required to perform capacitance measurements. The LCR meter sets a static bias value to the device under test. An *a.c.* sinusoidal signal δV_G which is frequency f dependent, is added to V_G. For all the measurements we have chosen $\delta V_G = 26\ mV$. This value is close to thermal potential fluctuations ($k{\cdot}T/q$) in case of ambient temperature. δV_G induces charge variation in the conduction channel, which is detected by the LCR meter thanks to a Wheatstone bridge. In order to achieve correct characteristics, open and short circuit corrections must be performed before any measurement. This avoids effects due to parasitic capacitances of the cables and the probe station [95], [96].

After the presentation of the measurement setup, the next section shows capacitance characteristics as a function of gate bias obtained in pseudo-MOSFET configuration.

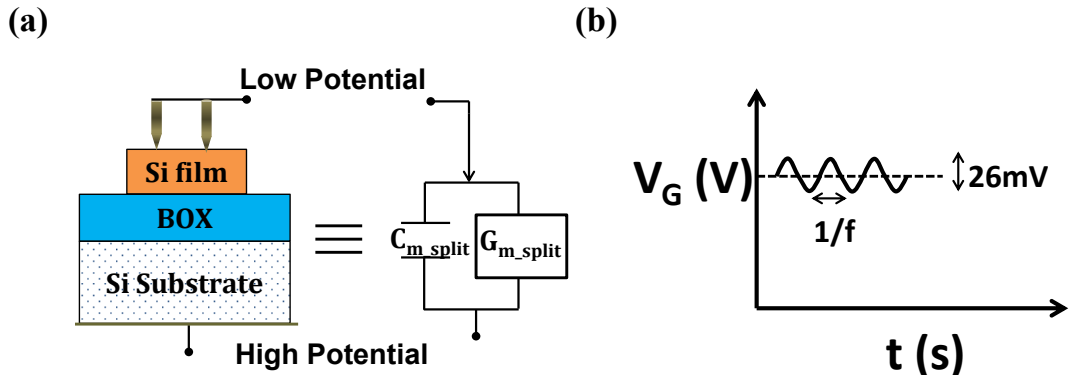

Figure III-3: (a) Measurement setup and equivalent electric circuit for split-CV capacitance in pseudo-MOSFET configuration. (b) Schematic of applied gate bias in split-CV as a function of time.

Capacitance versus gate bias

Figure III-4 shows the measured split-CV capacitance as a function of gate bias for different frequencies. For low V_G magnitude, C_{GC} is negligible before the conduction channel formation. Above V_T (or V_{FB}) free carriers are induced by V_G and the capacitance sharply increases until it saturates. Note that in case of pseudo-MOSFET, the probes placed on the top silicon surface can bring both types of carriers: positive gate bias induces electrons in the conduction channel, while $V_G < 0\ V$ leads to holes accumulated at the interface between the top silicon film and the buried oxide. The curves behavior is similar to MOSFET device characteristics [89], validating the technique for SOI wafers.

In the next section, we will show how there results were used to directly access the effective mobility.

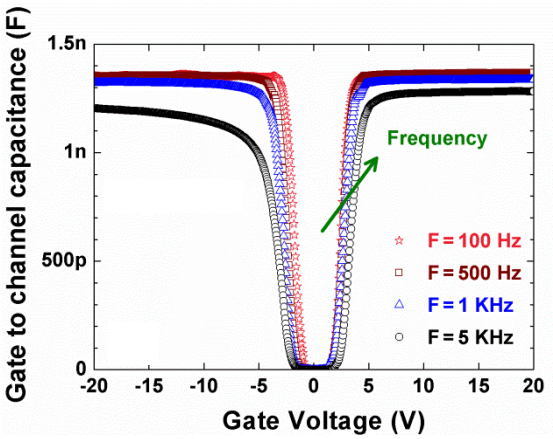

Figure III-4: C_{GC} as a function of gate voltage for different measurement frequencies. SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness. The die area was *24 mm²* [53].

Effective mobility extraction

Following the approach described in Sec. III.1.1, the effective carrier mobility can be computed using Eq. (III.3). In pseudo-MOSFET, *W/L* ratio is given by the geometrical factor f_G (see Sec. II.2) [47], [67]. μ_{eff} values require also the calculation of inversion (or accumulation) charge density (Eq. (III.2)). Note that the measured maximum capacitance ($C_{GC_mac} \approx 1.35\ nF$) obtained in Figure III-4 is much lower than the oxide capacitance (*5.7 nF*). Fernandez *et al.* [54] proposed to introduce a fitting parameter called effective surface (S_{eff}) and defined as:

$$S_{eff} = \frac{C_{GC_max}}{C_{OX}} \tag{III.8}$$

S_{eff} replaces the actual sample surface *S* in the computation of Eq. (III.2). It is determined from the maximum capacitance value and BOX thickness. Figure III-5 shows the obtained effective mobility (empty symbols) versus gate bias for electrons (a) and holes (b). To validate the obtained values, μ_{eff} reconstructed from Y function method is also added in plain symbols [66]:

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1(V_G - V_T)} \tag{III.9}$$

The curves perfectly overlap. The results show that effective carrier mobility can be measured using split-CV technique in pseudo-MOSFET configuration as for standard MOSFET devices.

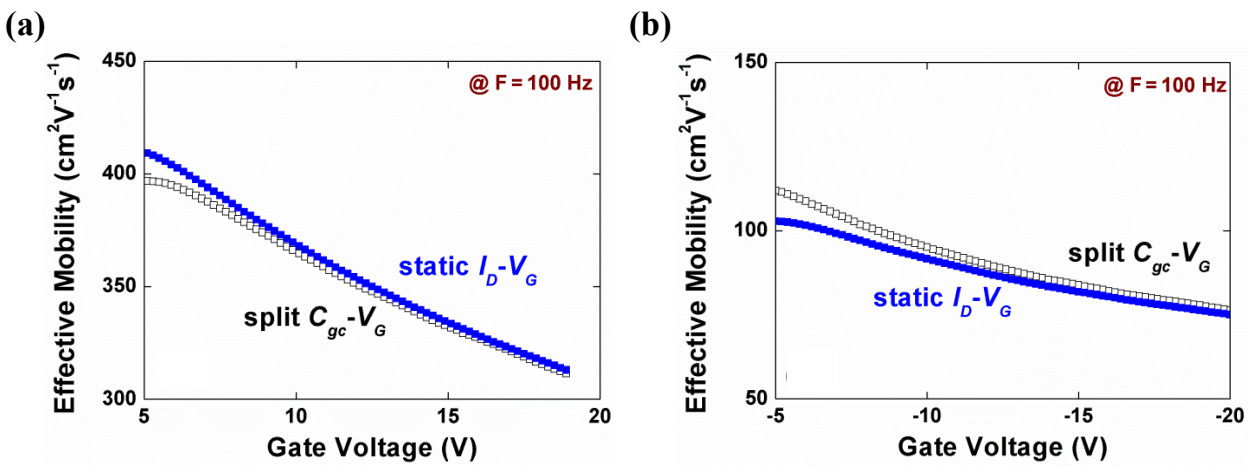

Figure III-5: Effective mobility as a function of gate bias obtained from Figure III-4 in case of electrons (a) and holes (b). The reconstructed values from Y function method (plain symbols) are also shown [53].

Besides the possibility of μ_{eff} extraction, two questions still remain open:

- What is the physical meaning of the effective surface?
- Is it possible to characterize the interface quality using the conductance term from split-CV measurements?

The answers will be given in the following sections. We will start analyzing the reasons behind the use of S_{eff}.

III.2 Effective surface and improved measurement setup

The first characteristics obtained in pseudo-MOSFET configuration [53], [54] have shown that contrary to standard MOSFET devices, the measured maximum capacitance is much lower than the expected value $C_{OX} \cdot S$. However, the use of a fitting parameter (S_{eff}) leads to correct effective mobility curves. In order to investigate the physics explanation behind this term, we study the impact of SOI die area, silicon film and BOX thicknesses.

III.2.1 Dependency of S_{eff}

The effective surface was considered as issued from the area around the probes that "responds" during the split-CV measurements [54]. If this is the case, S_{eff} should be somehow related to the geometry of the sample.

Figure III-6a shows the measured capacitance as a function of gate bias at low frequency *20 Hz*, on SOI structures with *88 nm* thick silicon film and *145 nm* thick BOX. Different die areas have been used (values added on the curves). The higher the die area, the higher the measured maximum capacitance (C_{max_air}). The *y*-axis scale shows that the increasing of C_{max_air} for larger surface is not linear. The effective surface values divided by the surface *S* corresponding to each curve are plotted as a function of die area in Figure III-6b. Using small size sample (*i.e.*, *4 mm*^{2}), S_{eff}/S is close to unity. Thus, the measured capacitance is close to the expected value. Increasing the die dimensions, the surface ratio S_{eff}/S sharply decreases. This dependency is unexpected and difficult to explain. For standard MOSFET devices, the scaling of the maximum measured capacitance is directly proportional to the die area.

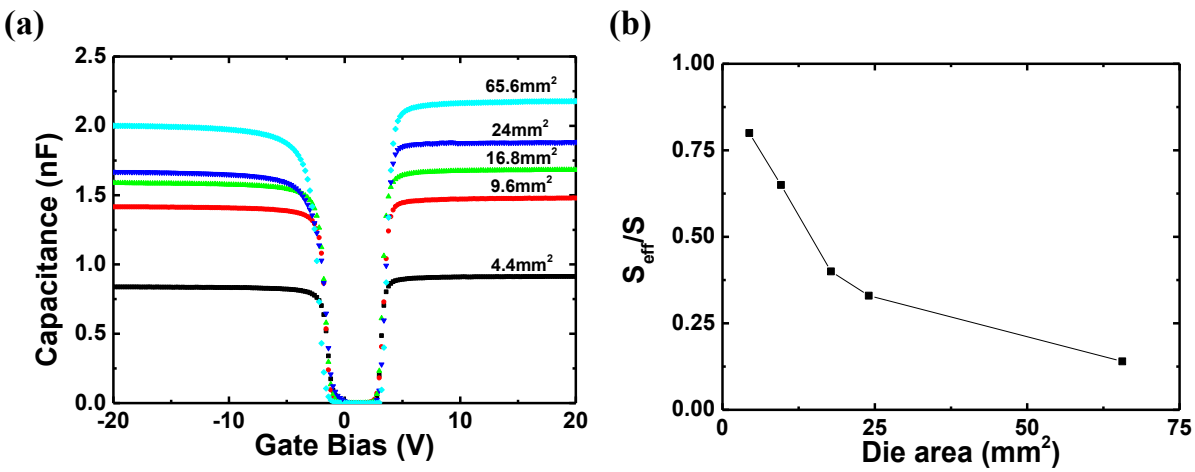

Figure III-6 (a) Measured capacitance versus gate bias for different die sizes at low frequency (*f = 20 Hz*). The corresponding S_{eff}/S calculated using Eq. (III.8) as a function of die area is reported in Figure III-6b. The SOI structure had *88 nm* top silicon film thickness and *145 nm* BOX thickness. The top surface was non-passivated.

Table III-1 compares $C_{OX} \cdot S$ and the measured maximum capacitance on SOI structure with different Si film and BOX thicknesses. The corresponding effective surface is also reported. In case of thick buried oxide, S_{eff} is independent of the top silicon film thickness. In case of ultra-thin SOI structures, however, the effective surface becomes very small and related to the properties of the top silicon film. This relation is not obvious, because the measured maximum capacitance should be independent of the film thickness and only related to the BOX characteristics (*i.e.*, area and thickness).

In end, no clear scaling was observed leading to the idea that this effective surface is rather a measurement artefact (parasitic effects) than an actual meaningful parameter. In the next section we will present a better measurement setup that leads to proper characteristics with $S_{eff}/S = 1$.

Silicon film/BOX (*nm/nm*)	$C_{OX} \cdot S$ (*nF*)	C_{max_air} (*nF*)	$S_{eff} = C_{max_air}/C_{BOX}$
88/145	5.7	1.9	0.33
12/145	5.7	1.9	0.33
83/25	33.1	2.1	0.06
12/25	33.1	2.6	0.08

Table III-1: Calculated oxide capacitance ($C_{OX} \cdot S$) with Eq. (III.1) for different SOI structure with passivated top surface. The measured capacitance values are shown (C_{max_air}). The corresponding S_{eff} is calculated with Eq. (III.8) for each structure.

III.2.2 Improved measurement setup

In case of static characteristics (see Sec. II.3.2), the quality of the back contact between the wafer and the metallic chuck plays a minor role. On the contrary, for the split-CV measurements, the quality of this contact, so called "*back contact*", plays a remarkable role. Figure III-7 shows the obtained capacitance (a) and conductance (b) versus gate bias from SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness. All measurements have been performed at $f = 20\ Hz$, in order to avoid any impact due to frequency attenuation [97]. The characteristics have been recorded using either special precautions for the back contact (*i.e.*, vacuum contact) or without any precaution (*i.e.*, air contact). Note that all the results present in the literature [53], [54] have been obtained using air back contact. The expected maximum capacitance (dashed line in Figure III-7a) represents the BOX capacitance and it is calculated by Eq. (III.1). In case of vacuum back contact, the measured maximum capacitance (C_{max}) is very close to oxide one. On the contrary, without using any particular precaution on the back contact quality, the measured maximum capacitance (C_{max_air}) is much lower than $C_{OX} \cdot S$ for both electrons and holes. The difference is due to parasitic effects that act as an added capacitance term placed in series with the BOX capacitance [98]. Their impact is not removed by the open and short circuit corrections because they appear only in presence of the sample. The threshold and flat-band voltages, which are related to the static bias, are the same for both

characteristics. This result was predictable since the quality of the back contact has no influence on the static I_D-V_G curves.

For the conductance term (Figure III-7b), a perfect overlap is obtained before the channel formation. However, the measurements performed using vacuum back contact show two sharp peaks after V_T and V_{FB}, followed by rapid conductance decrease after channel creation. For air contact, the peaks are smaller and the conductance does not decrease as rapidly. For V_G higher than V_T or V_{FB}, there should be no current flow through the structure (*i.e.*, low G_{m_split} values). Thus, the characteristic obtained using vacuum back contact is closer to what is expected for standard MOSFET devices [56].

The next natural step is to check if the measured maximum capacitance using vacuum back contact scales with the real surface.

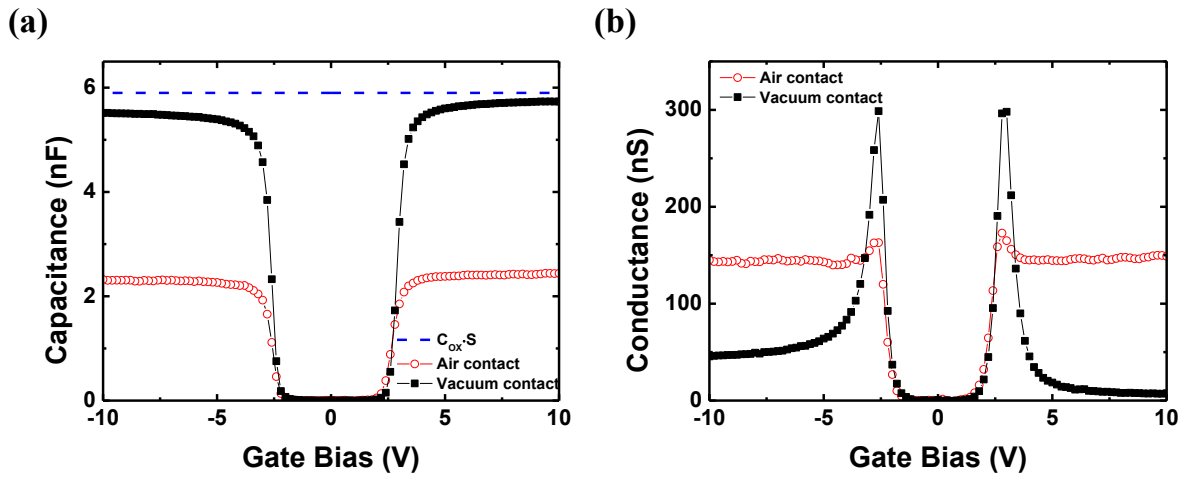

Figure III-7: Capacitance (a) and conductance (b) versus gate bias measured at low frequency (*f = 20 Hz*). Two different types of back contact have been used: vacuum back contact (plain symbols) and air back contact (empty symbols). The dashed line represents the BOX capacitance. SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness. The die had non-passivated top surface and *24 mm²* area.

Effective surface versus real surface

Different die area samples were tested. Figure III-8 shows the results obtained using vacuum back contact. The SOI structure has *88 nm* Si film and *145 nm* BOX. All the characteristics present similar threshold and flat-band voltage. C_{max} appears to be proportional to the oxide capacitance.

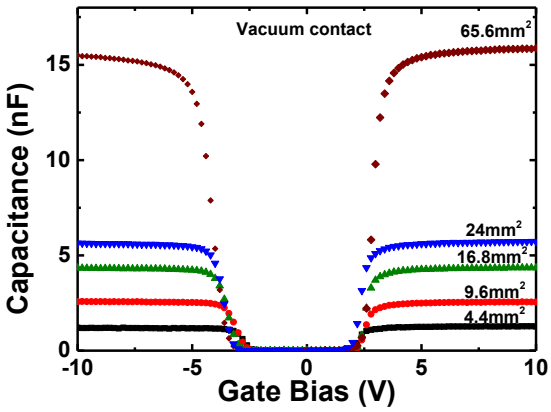

Figure III-8: Capacitance versus gate bias measured at low frequency (*f = 20 Hz*) using different die areas in case of vacuum back contact. The same SOI structures as in Figure III-6 have been used.

To better evaluate the obtained results, Table III-2 compares the calculated $C_{OX} \cdot S$ by Eq. (III.1) with C_{max} and C_{max_air} extracted from Figure III-8 and Figure III-6a, respectively. In case of vacuum contact, the measured maximum capacitance is given by the oxide capacitance. On the contrary, C_{max_air} is always lower than the expected one. For larger die surfaces, the difference between the measured maximum capacitance using back air contact and C_{OX} becomes stronger.

Die area (mm^2)	$C_{OX} \cdot S$ (nF)	C_{max} (nF) *Vacuum contact*	C_{max_air} (nF) *Air contact*
4.4	1.1	1.3	0.9
9.6	2.3	2.6	1.5
17.8	4.2	4.4	1.7
24	5.7	5.8	1.9
65.6	15.6	16.1	2.2

Table III-2: Calculated oxide capacitance ($C_{OX} \cdot S$) using Eq. (III.1) for different die areas, compared with the measured maximum electron capacitance obtained from Figure III-8 using vacuum (C_{max}) and air back contact (C_{max_air}) from Figure III-6a.

Using air contact, the results for different SOI thicknesses were not clear. To pursue with the investigation, Table III-1 has been enriched with the maximum capacitance obtained with vacuum back contact on the same structures (see Table III-3). C_{max} is always close to $C_{OX} \cdot S$, for all top-silicon film thicknesses and BOX thicknesses.

In conclusion, the use of vacuum back contact allows the measurement of the capacitance associated to the whole die as for standard MOSFET devices.

The natural question becomes: does the quality of the back contact affect μ_{eff} extraction?

Silicon film/BOX (*nm/nm*)	C_{OX}·S (*nF*)	C_{max_air} (*nF*) *Air contact*	C_{max} (*nF*) *Vacuum contact*
88/145	5.7	1.9	5.8
12/145	5.7	1.9	5.8
83/25	33.1	2.1	32.2
12/25	33.1	2.6	32.9

Table III-3: Table III-1 enriched with the corresponding maximum capacitance C_{max} obtained performing the characteristics on the same structure using vacuum back contact.

Effective mobility extraction

Figure III-9 shows the effective mobility as a function of gate bias obtained from Figure III-7a in case of electrons (a) and holes (b). The values are computed from characteristics measured with (plain symbols) and without (empty symbols) using vacuum back contact. For comparison, effective carrier mobility reconstructed by Y function method (Eq. (III.9)) is also added (dashed lines). Remarkable agreement is found between the three curves for both types of carriers. Thus, even if the quality of the back contact could limit the measured maximum capacitance, using a fitting parameter, S_{eff}, it is possible to extract realistic μ_{eff} values.

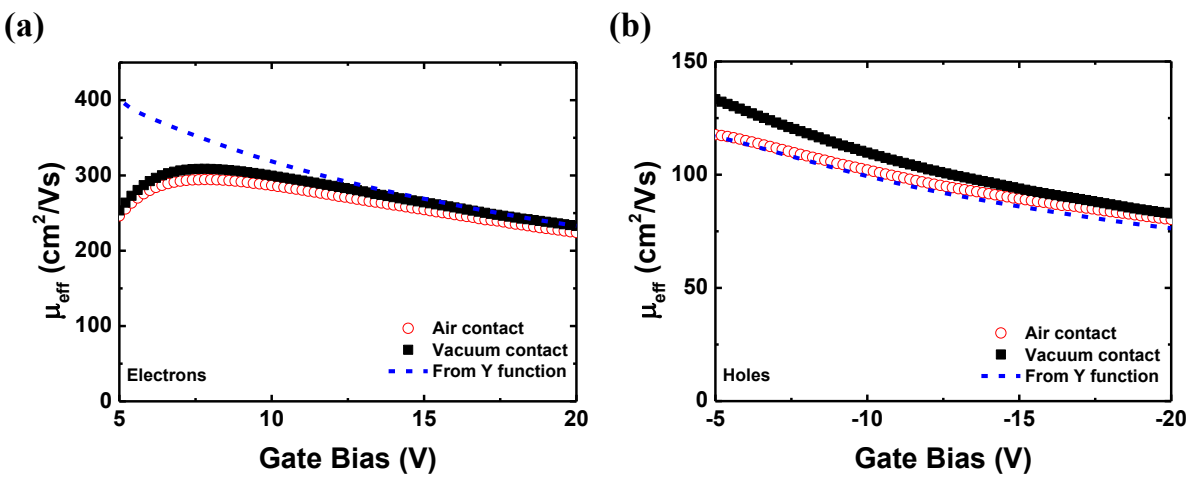

Figure III-9: Effective carrier mobility as a function of gate bias obtained from Figure III-7a in case of electrons (a) and holes (b) using vacuum (plain symbols) and air (empty symbols) back contact. Reconstructed value from Y function method (dashed line) using Eq. (III.9).

In conclusion, using split-CV technique for mobility investigation, the characteristic could be performed using air vacuum back contact, since S_{eff} can lead to the correct μ_{eff}. On the contrary, if one needs to perform reliable capacitance monitoring or to investigate the conductance term contribution, the use of vacuum back contact is required.

In the next sections, all the measurements performed in split-CV configuration have been obtained using vacuum back contact. This allowed tracing each time the capacitance (C_{m_split}) and conductance (G_{m_split}) curves normalized by the whole die area.

III.2.3 Robustness of the technique (probe effects)

In the case of static characterization, the control of the probe quality contact is the major parameter to achieve low access resistance and perform good characteristics suitable for parameter extractions (see Sec. II.3.3). The probes position is also critical for f_G [67]. Are similar effects present also in case of split-CV technique?

Probes pressure

Figure III-10 shows C_{m_split} (a) and G_{m_split} (b) curves versus gate bias performed at low frequency using different probe pressures. The inset shows the corresponding drain current characteristics as a function of gate bias. Remarkable overlap between the curves was found for both capacitance and conductance terms. Using split-CV technique the adjustable pressure probes are connected to low potential and the contact quality with the Si film plays a minor role. Even if the access resistance is high (*i.e.*, low probe pressure), the measured capacitance is the same as for low access resistance (high probe pressure).

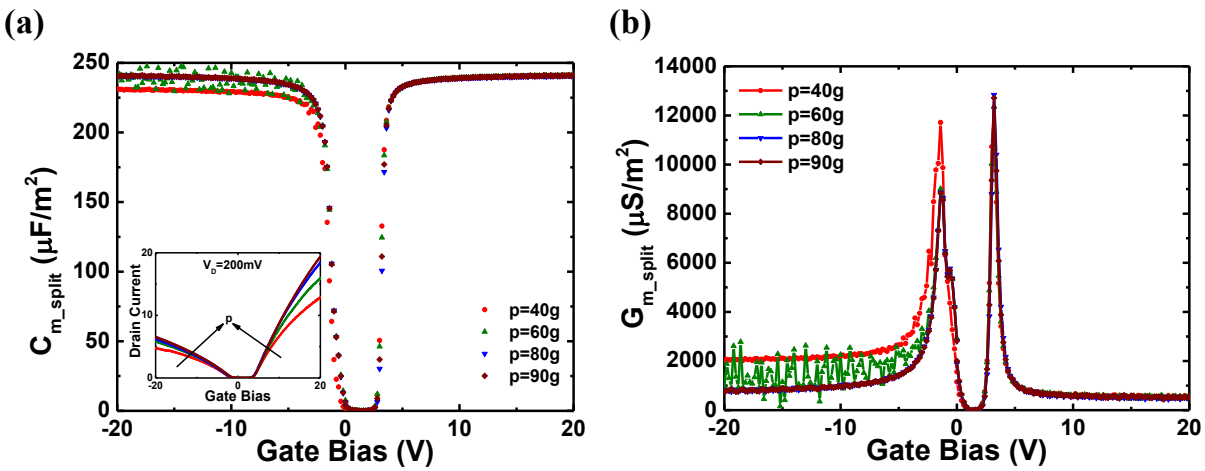

Figure III-10: Measured C_{m_split} (a) and G_{m_split} (b) versus gate bias using split-CV technique at low frequency (*20 Hz*) on SOI wafer with *88 nm* top silicon film thickness and *145 nm* thick BOX. Non-passivated top surface. Measurements performed using different probe pressures. Inset of (a): corresponding drain current as a function of gate bias.

Capacitance characteristics are not limited by the probe pressure. The measured effective carrier mobility should also be pressure independent. Figure III-11 shows μ_{eff} as a function of V_G in case of electrons (a) and holes (b) for different probe pressures. The reconstructed values from Y function method obtained at high pressure (*80 g*) were also added (dashed line). Using low probe pressures, μ_{eff} is underestimated. For high enough probe pressure, the measured effective carrier mobility overlaps with the reconstructed values from Y function method. The physical explanation is given by Eq. (III.3): μ_{eff} depends on capacitance measurements as well as on I_D-V_G characteristics. Even if the measured C_{GC} is pressure independent, the drain current is still limited by the access resistance and consequently the obtained effective mobility is also pressure dependent.

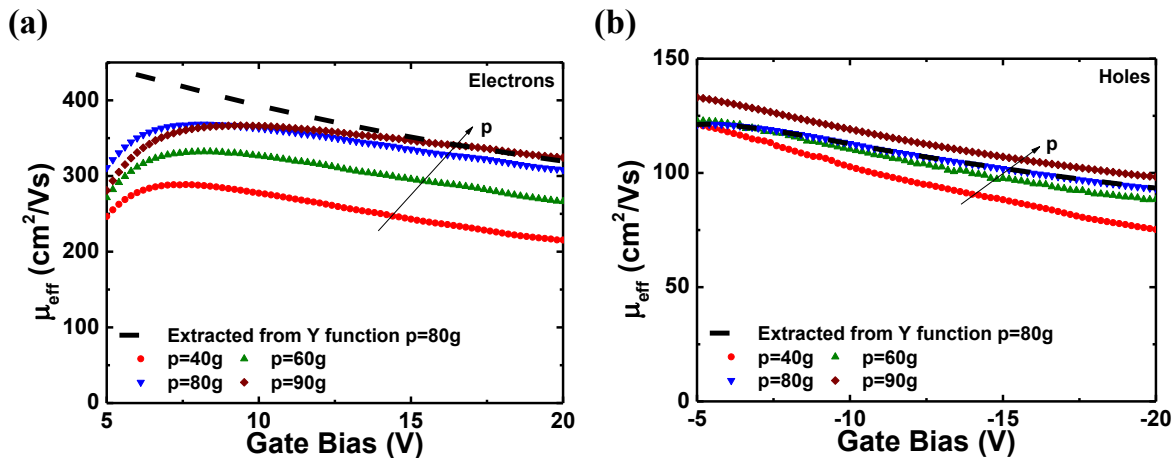

Figure III-11: Effective carrier mobility versus gate bias in case of electrons (a) and holes (b). Characteristics obtained with different probe pressures. μ_{eff} reconstructed from Y function method (*p = 80 g*) is also shown (dashed line) for comparisons.

Probe position

In order to achieve the best measurement setup, the effect of probe position on the top silicon film has to be investigated. The measured capacitance (a) and conductance (b) curves as a function of V_G for different probe positions are shown in Figure III-12. The corresponding drain current versus gate bias and the probe position on the silicon wafer are shown in the insets of Figure III-12a and Figure III-12b, respectively. Perfect overlap between the different characteristics was found for C_{m_split} and G_{m_split}. In case of split-CV, the probe placement on the die surface is not effecting the measurements.

In conclusion, we have seen that the access resistance (*i.e.*, probe pressure) and border effects (*i.e.*, probe position) have smaller impact on capacitance measurements than on current characteristics.

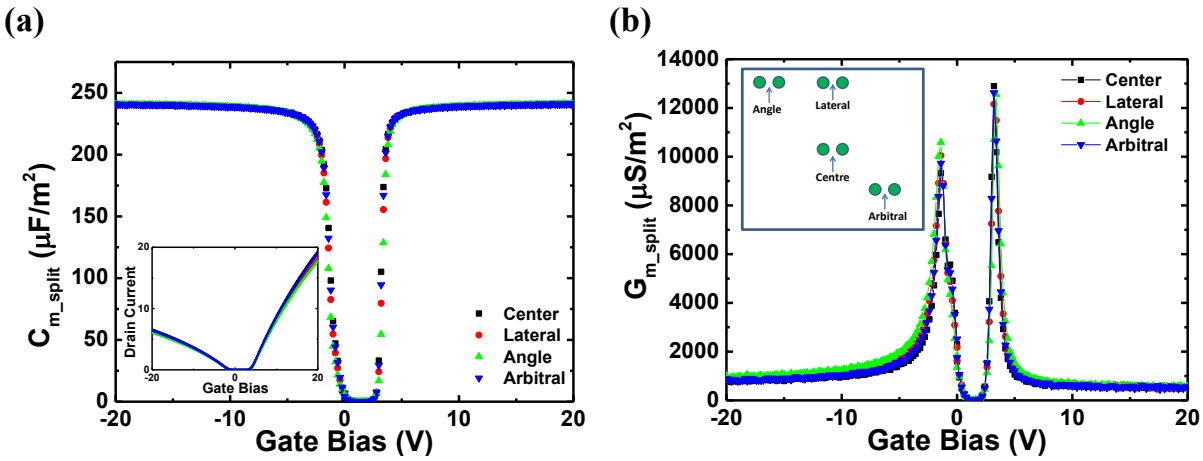

Figure III-12: Measured capacitance (a) and conductance (b) in split-CV configuration for different probe positions on the silicon film (inset Figure III-12b). Same SOI structure as in Figure III-11. The corresponding drain current versus gate bias curves are also presented in the inset of Figure III-12a.

Number of probes

Finally, the role played by the number of probes (N_{probe}) was also investigated. Split-CV technique allows the use of more than one needle placed on top silicon film and connected to the low potential of the LCR meter. It was shown that S_{eff} is dependent on N_{probe} [54].

Figure III-13a shows the measured capacitance versus gate bias using different numbers of probes. Perfect overlap between the several characteristics is found. Similar results are also obtained for the conductance terms (Figure III-13b). In conclusion, at low frequency, the oxide capacitance dominates the characteristics and effects due to the number of probes play a minor role.

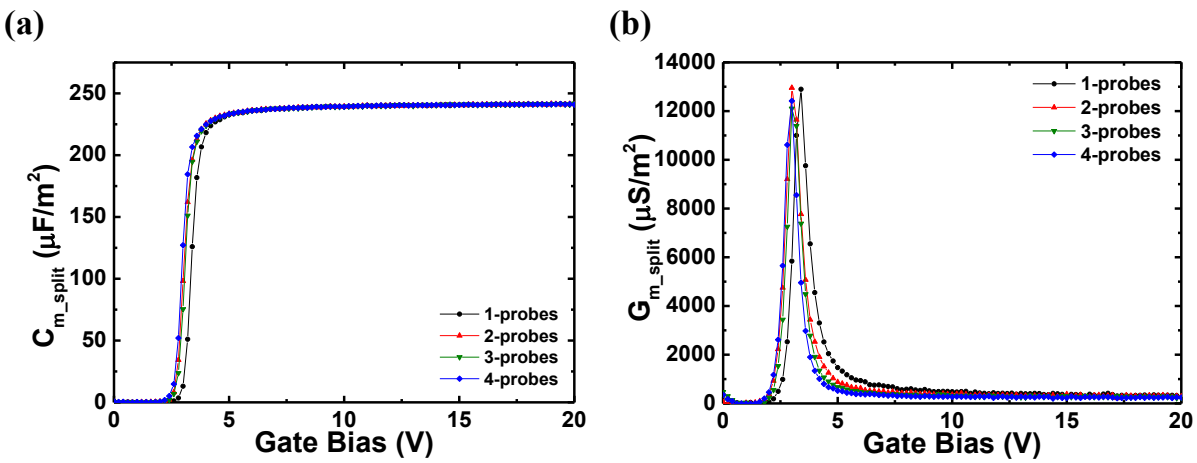

Figure III-13: Measured C_{m_split} (a) and G_{m_split} (b) as a function of gate bias at low frequency (*20 Hz*). Characteristics performed using different number of probes placed on the top-silicon film. The SOI structure was the same as in Figure III-11.

In these sections we have discussed about the experimental setup of split-CV and shown how it could affect the measurements. In the next section we will investigate the impact due to frequency effects and point out the possibility to characterize the interface quality.

III.3 Frequency effects

Experimental evidences show clear frequency effects on the C-V characteristics (Figure III-14a). Increasing *f*, the measured maximum capacitance becomes smaller than C_{OX}. Figure III-14b presents the measured capacitance as a function of angular frequency ($\omega = 2 \cdot \pi \cdot f$) in strong inversion regime for three different V_G. Capacitance attenuation is found at high ω magnitude. Diab *et al.* [97] have proposed a physical model based on RC electric circuit to explain the C_{m_split} -V_G curves in Ψ-MOSFET configuration. Even if it was initially developed only for C-V characteristics obtained with back air contact, we will discuss its validity also for measurements performed using vacuum back contact. It will be further enriched with the conductance term and the C-ω analysis will be performed. Its mathematical derivation will be also presented in the next section.

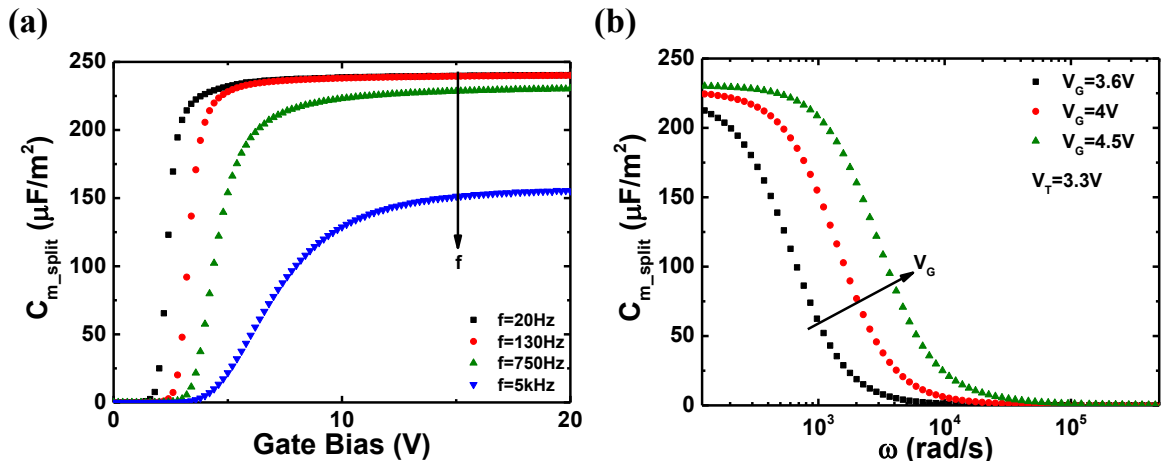

Figure III-14 (a) C_{m_split} versus gate bias for different frequency values. (b) Normalized capacitance as a function of angular frequency for different V_G. Measurements performed on the same SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness. Non-passivated top surface.

III.3.1 Model derivation

The equivalent electric circuit of pseudo-MOSFET structure is shown in Figure III-15a. Note that no contribution due to interface trap density is taken into account. The oxide capacitance (C_{OX}) is in series with the inversion (or accumulation) channel capacitance (C_{Inv}). Knowing t_{OX} and the whole die surface, C_{OX} can be calculated by Eq. (III.1). Furthermore, the inversion (or accumulation) charge density Q_i [99] allows C_{Inv} calculation:

$$C_{Inv} = \frac{\delta Q_i}{\delta V_G} \qquad \text{(III.10)}$$

Finally, the channel resistance R_{CH} represents the path required by one carrier to go from one probe to any point in the conduction channel. It is proportional to the sheet resistance (R_{SH}) and the number of probes placed on the top silicon surface N_{probe} [97]:

$$R_{CH} = \frac{R_{SH}}{N_{probe} \cdot f_g} = \frac{1}{N_{probe} \cdot f_g \cdot \mu_{eff} \cdot Q_i} \tag{III.11}$$

Thus, the complete SOI equivalent impedance becomes:

$$Z_{EQ} = R_{CH} + \frac{1}{j \cdot \omega \cdot \frac{C_{Inv} \cdot C_{OX}}{C_{Inv} + C_{OX}} \cdot S} \tag{III.12}$$

where j is the complex unit. In case of air back contact, the model equations remain the same, except that S_{eff} has to be used instead of S.

The LCR meter analyzer measures the SOI structure through a parallel equivalent circuit C_{m_split}-G_{m_split} (Figure III-15b). The obtained impedance has to be the same as Z_{EQ}. Thus, the imaginary and real terms of the equivalent admittance ($1/Z_{EQ}$) allow writing C_{m_split} and G_{m_split} as a function of device parameters:

$$C_{m_split} = \frac{1}{\omega \cdot S} \cdot \mathrm{Im}\left[1/Z_{EQ}\right] = \frac{\frac{C_{Inv} \cdot C_{OX}}{C_{Inv} + C_{OX}}}{1 + \left[\omega \cdot R_{CH} \cdot \frac{C_{Inv} \cdot C_{OX}}{C_{Inv} + C_{OX}} \cdot S\right]^2} \tag{III.13}$$

$$G_{m_split} = \frac{1}{S} \cdot \mathrm{Re}\left[1/Z_{EQ}\right] = \frac{R_{CH} \cdot \left(\omega \cdot \frac{C_{Inv} \cdot C_{OX}}{C_{Inv} + C_{OX}}\right)^2 \cdot S}{1 + \left[\omega \cdot R_{CH} \cdot \frac{C_{Inv} \cdot C_{OX}}{C_{Inv} + C_{OX}} \cdot S\right]^2} \tag{III.14}$$

In order to validate the proposed model, experimental results will be systematically compared to calculated curves for different measurement configurations (see next section).

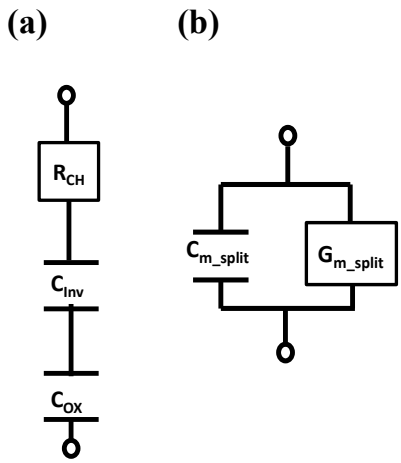

Figure III-15: (a) Equivalent electric circuit of SOI structure (Z_{EQ}). (b) Equivalent electric circuit used by the LCR meter.

III.3.2 Model validation

Equations (III.13) and (III.14) are dependent of gate bias as well as of angular frequency. The complete validation of the physical model requires the comparison of measured and calculated characteristics as a function of V_G (Sec. III.3.2.1) and of ω (Sec. III.3.2.2). Furthermore, the impact of N_{probe} and of S will be addressed in Sec. III.3.2.3. The capability to characterize ultra-thin SOI structures will be shown in Sec. III.3.2.4.

III.3.2.1 *C_{m_split} and G_{m_split} versus gate bias*

Figure III-16 shows the measured (empty symbols) capacitance as a function of gate bias for different frequencies in case of holes (a) and electrons (b). The calculated curves by Eq. (III.13) were also added (dashed line). Measurements have been performed on non-passivated SOI wafer using two probes on the silicon surface. Good agreement was found between the measured curves and the calculated ones. Small differences are present for high frequency in case of holes, probably due to higher access resistance. Note that no fitting parameters were used. For low frequency (*i.e.*, $f = 20\ Hz$) the measured capacitance at high V_G is dominated by the oxide capacitance, since C_{Inv} is much higher than C_{OX}. Increasing the measurement frequency, the carriers have less time to go from the probes to the channel, so the measured capacitance decreases. The same behavior is also obtained in case of standard MOSFET devices [5].

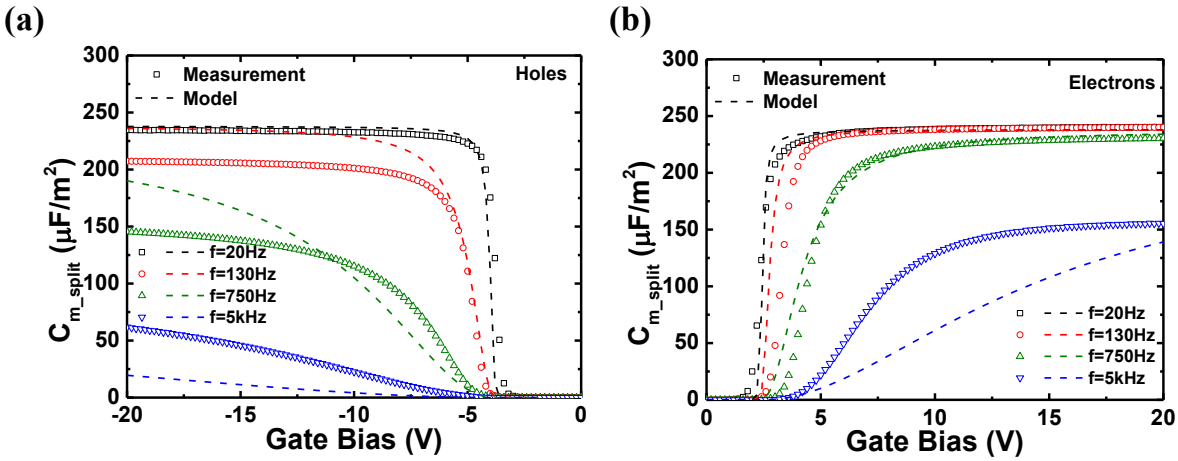

Figure III-16: Measured (empty symbols) and calculated (dashed line, from Eq. (III.13)) capacitance versus gate bias in case of holes (a) and electrons (b) for different frequencies. Measurements performed using two probes on non-passivated SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness.

Figure III-17 shows the corresponding conductance versus gate bias obtained from Figure III-16 at $f = 20\ Hz$: measured (empty symbols) and calculated (dashed line) characteristics. The light difference in the peak height is due to possible V_T mismatch between the computed R_{CH} obtained from I_D-V_G analysis and split-CV measurements. Diab *el al.* [97] have shown how the RC model can explain only capacitance characteristics using air back contact and S_{eff}. The use of vacuum back contact allows completing C_{m_split} and G_{m_split} modeling without using any fitting parameter.

In the next section, characteristics obtained as a function of ω will be addressed.

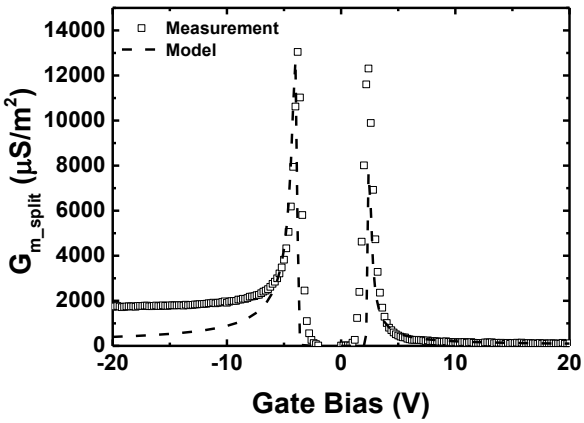

Figure III-17: Conductance versus gate bias corresponding to the capacitance measured (empty symbols) and calculated (dashed line) in Figure III-16 for *f = 20 Hz*.

III.3.2.2 *C_{m_split} and G_{m_split} versus angular frequency*

To further validate the frequency dependence, capacitance and conductance characteristics as function of ω for fixed V_G were measured. Figure III-18 shows the results for holes (a) and electrons (b) using different gate bias. The same SOI structure of Figure III-16 was used. The measured capacitance (plain symbols) are in good agreement with the calculated ones (lines) from Eq. (III.13). In case of slow angular frequency, the channel has enough time to reach equilibrium state and the maximum capacitance is dominated by C_{OX}. Increasing ω, the free carries do not have enough time to follow the *a.c.* signal and the measured C_{m_split} decreases. This is typical RC filter behavior. Note that the capacitance attenuation is delayed in case of high V_G magnitude, thanks to lower R_{CH} in strong inversion regime.

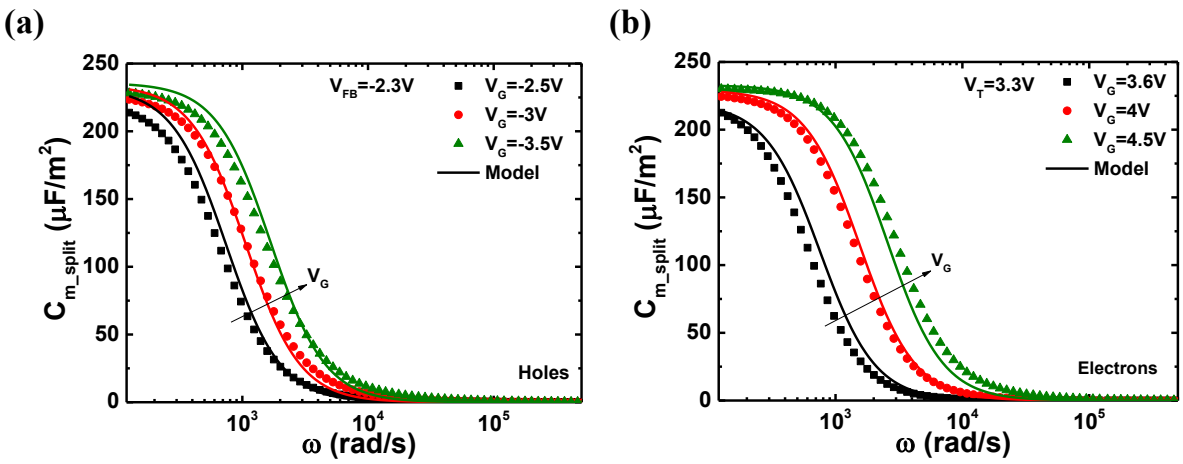

Figure III-18: Hole (a) and electron (b) capacitance as a function of angular frequency for different gate bias. Measurement performed with two probes placed on top silicon film. SOI with *88 nm* thick top silicon film and *145 nm* thick BOX. The top surface was non-passivated.

The corresponding conductance terms of Figure III-18 are shown in Figure III-19 in case of holes (a) and electrons (b). The experimental results (plain symbols) are compared with the calculated values (lines) from Eq. (III.14). Also in this case, typical RC shape is obtained and the modeled characteristics are in good agreement with the measured ones.

In the next section, the impact on the characteristics due to die area and number of probes will be addressed.

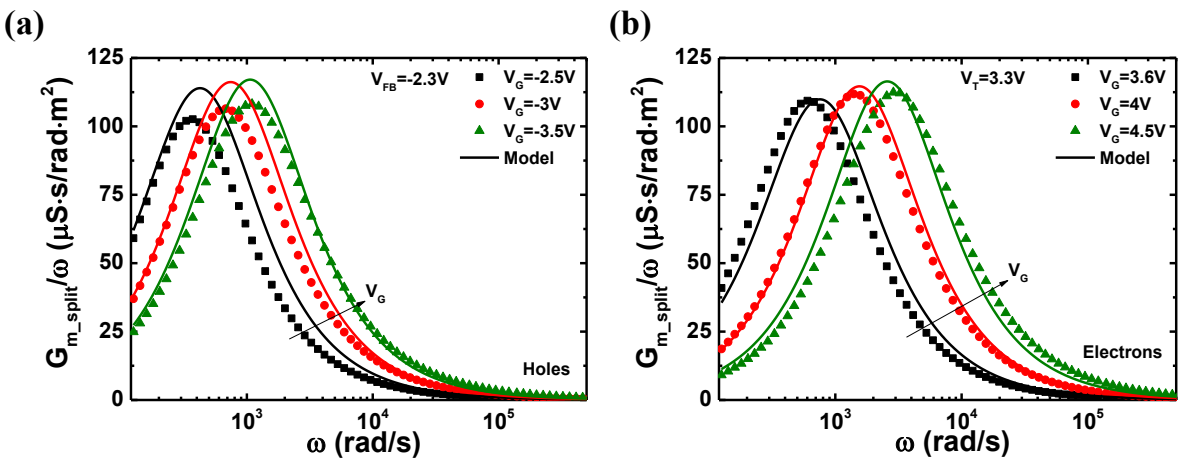

Figure III-19: Conductance over angular frequency versus *ω* associated to the capacitance in Figure III-18 for $V_G < 0\ V$ (a) and $V_G > 0\ V$ (b).

III.3.2.3 *Effects of die area and number of probes*

Equations (III.13) and (III.14) are clearly dependent on die area. Thanks to the use of vacuum back contact, it was already shown that the whole surface participates to capacitance measurements. Figure III-20 shows the normalized C_{m_split} (a) and G_{m_split}/ω (b) as a function of angular frequency for different S at the same overdrive voltage (V_G-V_T). The calculated values (lines) are added for comparison. At low ω, the maximum surface capacitance is the same for all die areas, since it is dominated by C_{OX}. The smaller the die area, the higher the cut-off frequency, as predicted in Eqs. (III.13) and (III.14). The RC model is always capable to predict well the curves behavior. The differences in the G_{m_split}/ω curves, present in case of small die areas and large ω magnitude, are due to parasitic effects that are still under investigation.

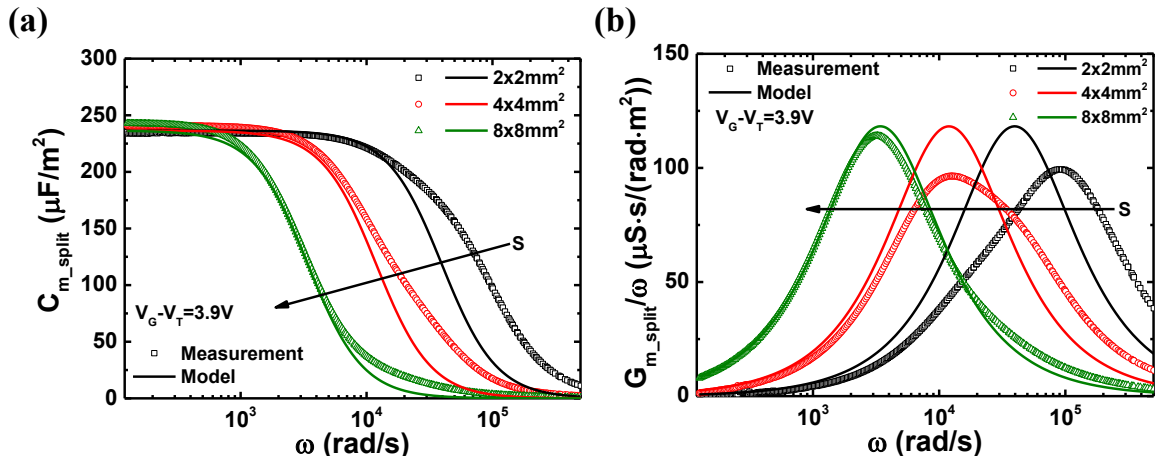

Figure III-20: C_{m_split} (a) and G_{m_split}/ω (b) as a function of angular frequency for different die areas. Same SOI structure as in Figure III-18.

Another important parameter to take into account during split-CV characteristics is the number of probes placed on the top silicon surface. N_{probe} determines the channel resistance R_{CH} magnitude (see Eq. (III.11)). Thus, C_{m_split} and G_{m_split} will change proportionally to the number of probes. All the results discussed above have been obtained using two probes. Figure III-21 shows the capacitance and G_{m_spit}/ω versus ω obtained using one probe on the top silicon film. Measurements (empty symbols) and modeled results (lines) are compared. Also in this case a remarkable agreement was found. Finally, we will discuss about the possibility to characterize ultra-thin SOI structures.

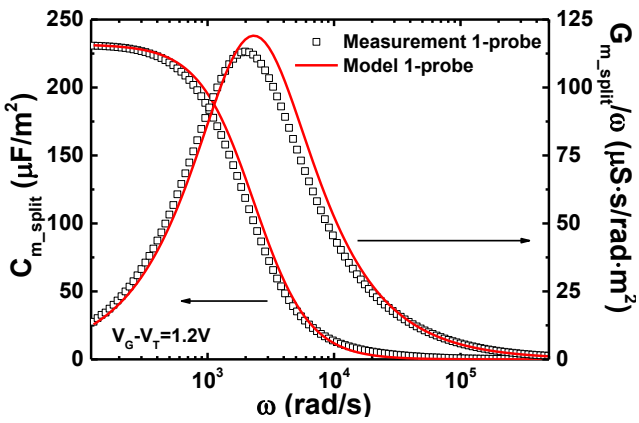

Figure III-21: C_{m_split} and G_{m_split}/ω curves versus angular frequency obtained with one probe on the top silicon film. Experimental results (empty symbols) and calculated curves (line) are shown. Same SOI structure as in Figure III-18.

III.3.2.4 *Ultra-thin SOI structure*

In the previous sections it has been shown that the RC model gives a realistic representation of split-CV characteristics, independently of the regime under analysis, the surface of the die and the number of probes used for the characterization. Here we want to extend split-CV technique to ultra-thin SOI structures. The results obtained for SOI wafer with *12 nm* non-passivated top silicon film and *25 nm* BOX are presented in Figure III-22. The measured (empty symbols) capacitance and G_{m_split}/ω terms are compared to the calculated ones (lines) in strong inversion (a) and accumulation (b) regime. Even if the silicon film is ultra-thin and strong coupling between the top and bottom silicon interfaces is present, the model can well fit the experimental results without any D_{it} contribution. In the next section the possibility to characterize interface quality in split-CV will be addressed.

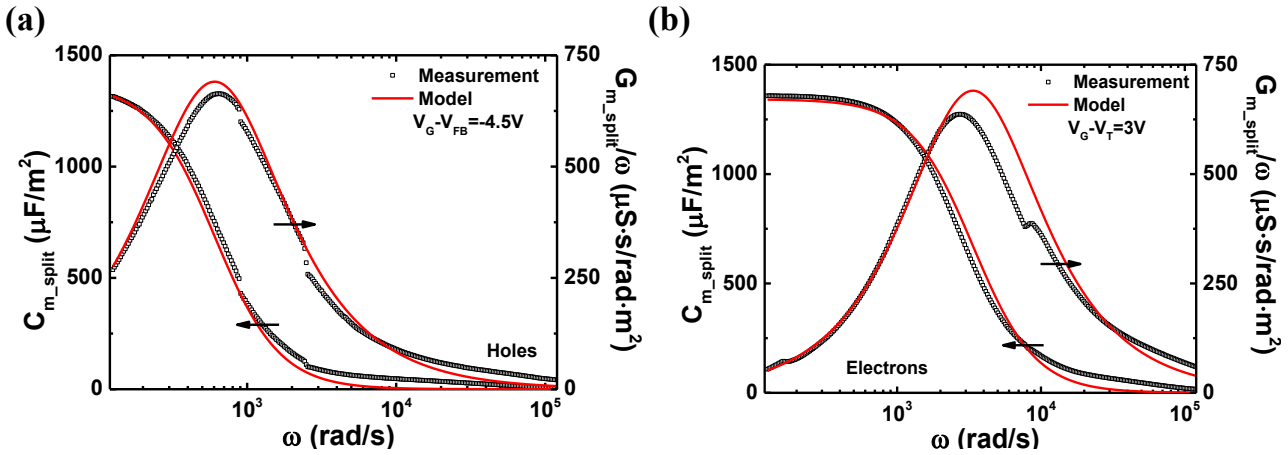

Figure III-22: Capacitance and conductance G_{m_split}/ω characteristics obtained versus angular frequency in accumulation (a) and strong inversion (b) regime on SOI structure with *12 nm* top silicon film thickness and *25 nm* BOX thickness. Non-passivated SOI structure. The experimental results (empty symbols) are compared to the calculated curves using our RC model (lines).

III.3.3 D_{it} signature

In the literature the capacitance and the conductance measurements are largely used for D_{it} investigation [100]–[102]. The results obtained in the previous section show that a RC model without any interface traps contribution can reproduce the measured characteristics in strong inversion and accumulation regime. This suggests that the D_{it} are not "*visible*". We performed split-CV measurements with different top surface (after HF treatment, with native and passivation oxide). The aim is to see whether the surface state affects the curves.

One possibility to induce a lot of dangling bonds on the top silicon surface is to perform HF treatment on the wafer [63]. The native oxide is etched and the surface becomes very reactive. Figure III-23 shows the capacitance versus gate bias measured before (line) and after (symbols) HF treatment. The SOI structure had *88 nm* thick non-passivated silicon film and *145 nm* thick BOX. Clear peak appears on the curve obtained after the chemical procedure, probably due to the high density of dangling bonds induced on the surface. The V_T and V_{FB} variations are due to the variation of top charge density as already seen by Hovel [63]. After channel formation the characteristics perfectly overlap because the high density of free carriers masks any possible effects due to traps or dangling bonds. Thus, the best region to look for D_{it} signature is before channel formation.

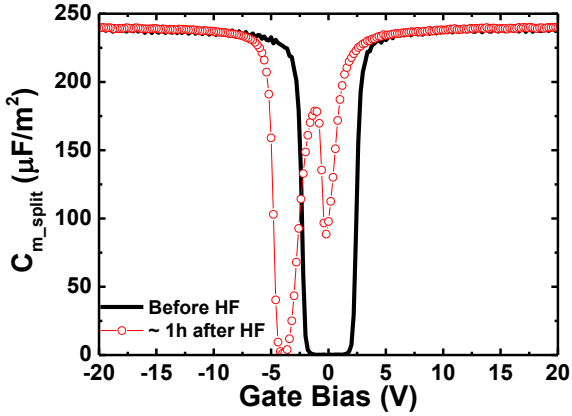

Figure III-23: Capacitance as a function of gate bias measured at low frequency (*20 Hz*) before (continuous line) and after (symbols-line) HF treatment. Non-passivated SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness.

In order to verify that the capacitance peak is related to HF treatment, the wafer was characterized at different moments after the cleaning procedure. In ambient condition, the native oxide grows back decreasing the density of active bonds present on the Si surface. The capacitance terms as a function of gate bias are shown in Figure III-24a. The threshold voltage shifts towards the initial value (continuous line). The peak decreases sharply with time. Almost *16* hours after the treatment, effects due to dangling bonds have become very small. The behavior obtained more than one week after the chemical treatment is very similar to the one measured before the HF clean.

The conductance term versus gate bias shown in Figure III-24b suggests the same remarks: V_T shift, supplementary peak after HF treatment, recovery of the shape after one week.

These experiments clearly demonstrate that split-CV capacitance measurements can detect information concerning surface quality. Consequently, including D_{it} effects in the RC model could be interesting for a future extraction procedure.

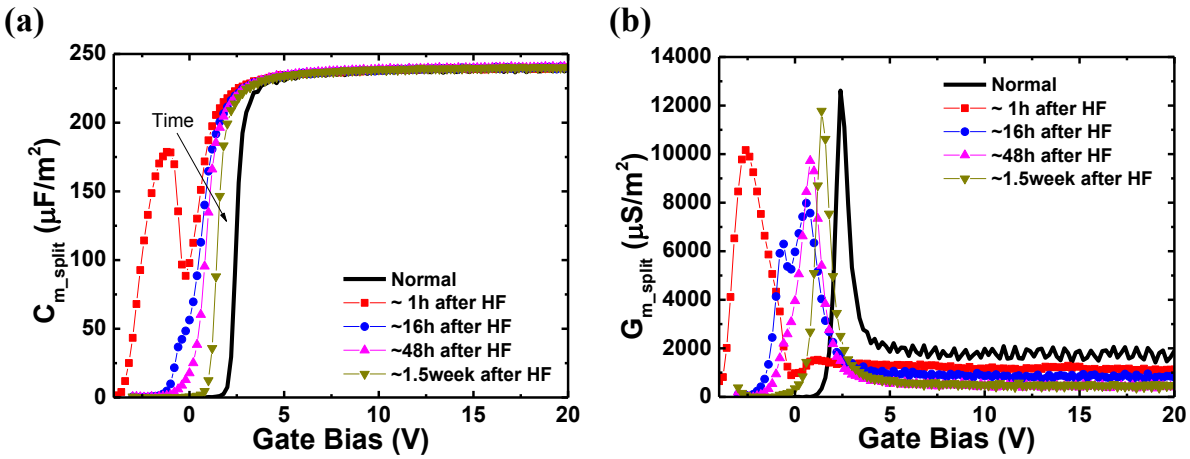

Figure III-24: Capacitance (a) and conductance (b) as a function of gate bias measured at low frequency (*20 Hz*) at different moments after HF treatment. The characteristic obtained before the chemical process is also shown (continuous line). Same structure as in Figure III-23.

III.3.3.1 *RC model including D_{it} contribution*

Schroder [56] proposed to introduce the D_{it} contribution in parallel to the inversion (or accumulation) capacitance (Figure III-25a). The traps are modeled by a capacitor (C_{Dit_c}) in series with a conductance (G_{Dit_c}) due to trap lossy process. In case of continuum level of interface traps, one gets [56]:

$$C_{Dit_c} = q \cdot D_{it} \tag{III.15}$$

$$G_{Dit_c} = \frac{q \cdot D_{it} \cdot \omega^2 \cdot \ln\left[1 + \left(\omega \cdot \tau_{Dit}\right)^2\right]}{2 \cdot \omega \cdot \tau_{Dit}} \tag{III.16}$$

where τ_{Dit} is the trap effective lifetime [50]. The electrical equivalent circuit is typically rearranged in order to separate the capacitance and conductance contribution (Figure III-25b).

As done for the RC model derivation (Sec. III.3.1), the total equivalent impedance, including also D_{it} contribution, has to be the same as the measurement equivalent impedance (Figure III-25c). Thus, it is possible to rewrite C_{m_split} and G_{m_split} as:

$$C_{m_split} = \frac{C_{OX} \cdot G_p^2 + \omega^2 \cdot C_{OX} \cdot \left(C_p + C_{OX}\right)}{G_p^2 + \omega^2 \cdot \left[C_p^2 + C_{OX}^2 \cdot \left(1 + R_{CH} \cdot G_p\right)^2 + 2 \cdot C_p \cdot C_{OX}\right] + \omega^4 \cdot C_{OX}^2 \cdot C_p^2 \cdot R_{CH}^2} \tag{III.17}$$

$$G_{m_split} = \frac{\omega^2 \cdot C_{OX}^2 \cdot \left[\omega^2 \cdot C_p^2 \cdot R_{CH} + G_p \cdot \left(1 + R_{CH} \cdot G_p\right)\right]}{G_p^2 + \omega^2 \cdot \left[C_p^2 + C_{OX}^2 \cdot \left(1 + R_{CH} \cdot G_p\right)^2 + 2 \cdot C_p \cdot C_{OX}\right] + \omega^4 \cdot C_{OX}^2 \cdot C_p^2 \cdot R_{CH}^2} \tag{III.18}$$

In the next sections, the analysis of C_{m_split}-V (Sec. III.3.3.2) and G_{m_split}-ω (Sec. III.3.3.3) characteristics will be addressed looking for D_{it} signature.

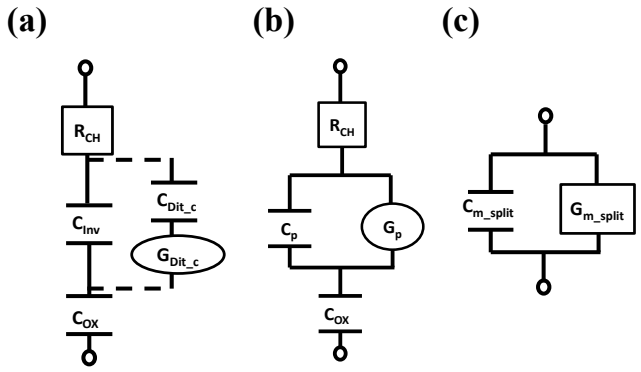

Figure III-25: (a) Equivalent electric circuit for SOI structure where D_{it} contribution was added. (b) Rearranged equivalent circuit. (c) Parallel electric circuit used during the measurements with the LCR meter.

III.3.3.2 *C-V characteristics*

To investigate the possibility of D_{it} detection through *C-V* analysis, measurements performed on passivated and non-passivated samples are compared. It is well known that for passivated top surface the surface trap density is much lower than for non-passivated one [83]. Note that the two samples present similar top film-BOX interface quality. Figure III-26 shows the measured C_{m_split} (a) and G_{m_split} (b) as a function of gate bias in case of passivated (empty symbols) and non-passivated (plain symbols) SOI structure, obtained at low frequency ($f = 20\ Hz$). Beside the typical shifts in V_T and V_{FB} [83], no D_{it} signature is detected, since the curves have the same behavior.

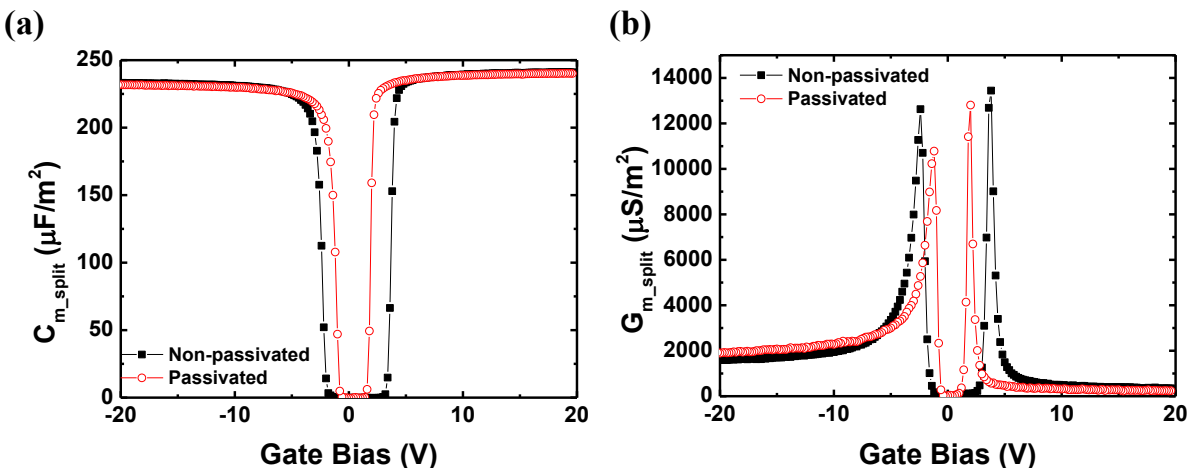

Figure III-26: C_{m_split} (a) and G_{m_split} (b) versus gate bias measured at low frequency (*20 Hz*). Comparison between passivated (empty symbols) and non-passivated (plain symbols) SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness.

Figure III-27 shows the calculated capacitance (a) and conductance (b) terms versus gate bias. The dashed line represents the curves obtained using the RC model without interface trap contribution calculated with Eq. (III.13) and Eq. (III.14). The continuous line shows the results including $D_{it} = 10^{13} cm^{-2} eV^{-1}$ in the RC model (Eq. (III.17) and Eq. (III.18)). The overlap between the characteristics confirms that *C-V* analysis performed on standard SOI wafer in pseudo-MOSFET configuration cannot lead to D_{it} detection even if abnormally large traps density has been used.

Another possibility to achieve D_{it} detection arises from frequency measurements. They will be discussed in the next section.

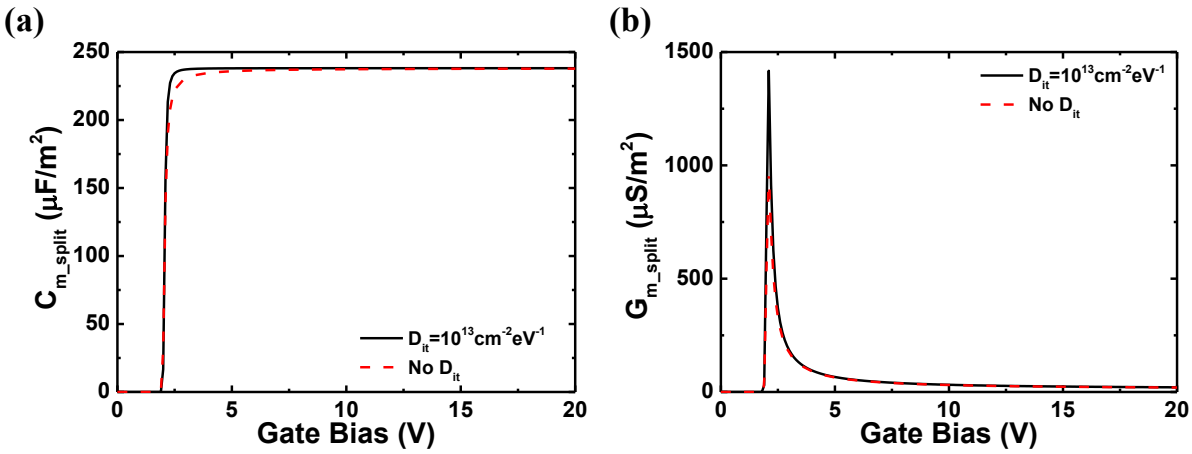

Figure III-27: Calculated capacitance (a) and conductance (b) versus gate bias with $D_{it} = 10^{13} cm^{-2} eV^{-1}$ (continuous line) and without (dashed line) D_{it} in case of low frequency (*20 Hz*). Same SOI structure as for the measurements.

III.3.3.3 *Frequency characteristics in depletion regime*

It has been already pointed out that the most sensible regime for D_{it} detection is the depletion one [100]. In order to evidence the traps signature in the conductance term, the contribution of the channel resistance and the oxide capacitance are removed from the measured conductance. Reversing Eq. (III.18), G_p is expressed as a function of C_{m_split} and G_{m_split}:

$$G_p = \frac{\omega^2 \cdot C_{OX}^2 \cdot G_{m_split} \cdot \left[1 - R_{CH} \cdot G_{m_split}\right] - \omega^3 \cdot C_{OX}^2 \cdot C_m^2 \cdot R_{CH}}{\left(G_{m_split} - \omega^2 \cdot C_{OX}^2 \cdot C_m \cdot R_{CH}\right)^2 + \omega^2 \cdot \left[C_{OX} \cdot R_{CH} \cdot G_{m_split} - C_{OX} + C_m\right]^2} \qquad \text{(III.19)}$$

G_p/ω characteristics versus ω have been obtained by standard G_{m_split}-ω measurement performed on non-passivated sample (Figure III-28). Since the low quality of top silicon interface with native oxide, strong impact due to D_{it} was expected. Before the channel formation, the signal is very small and after V_{FB} the creation of accumulation channel covers any possibility of D_{it} detection.

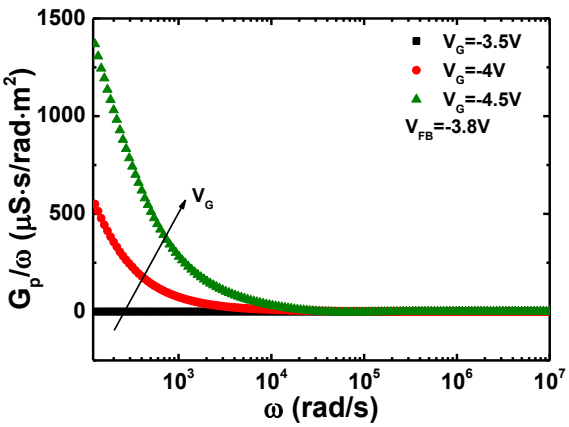

Figure III-28 G_p/ω as a function of ω for different gate bias values on non-passivated SOI structure (same structure as Figure III-25a).

Validation of experimental results comes from modelled curves. Figure III-29a shows the G_p/ω obtained without (plain symbols) and with (empty symbols) D_{it} contribution for different gate biases before and after channel formation. The SOI structure was the same as in Figure III-27. The die area was *25 mm²*. The characteristics with and without D_{it} always overlap and no signature due to interface traps is present. The effect due to R_{CH} is very strong and masks any possible signature of interface traps even for large density.

In order to attempt to reveal the D_{it} influence, the size of the die needs to be reduced. According to Eqs. (III.17) and (III.18), the RC response of the SOI layer should then be attenuated. We simulated the same system as in Figure III-29a but with decreased die area by a factor of *1000* (*0.025 mm²* instead of *25 mm²*). The full symbols in Figure III-29b represent the simulation obtained with D_{it} while the empty symbols are computed without interface trap density. We now note a pronounced influence of D_{it} for gate bias values around flat-band voltage (*-3.5 V*). In contrast, for gate bias exceeding the flat-band voltage, the effect of interface trap density disappears and the system response becomes again dominated by the RC model. In accumulation regime the curves calculated with and without D_{it} overlap.

These simulations indicate that the D_{it} extraction, even for quite large traps density, is not possible in our relatively large SOI samples with *10-50 mm²* area. Detection of larger D_{it} magnitude is limited by oxide capacitance.

The pseudo-MOSFET technique is used for in situ characterization and it should be able to evidence D_{it} signature of $\approx 10^{10}$-$10^{11} cm^{-2} eV^{-1}$. In principle, this is possible using very small dies. Unfortunately, the pseudo-MOSFET characterization of small SOI samples with area in the order of *100 µm x 100 µm* cannot be performed because the probe size is ≈ *40 µm*.

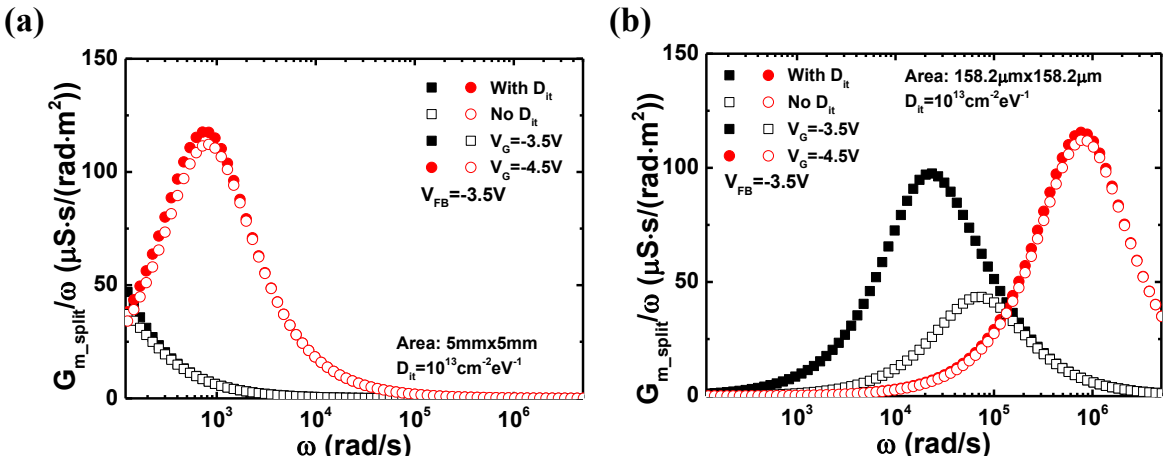

Figure III-29 (a) Modeled G_{m_split}/ω versus ω for different V_G around V_{FB} without (empty symbols) and with (plain symbols) D_{it} contribution. The same SOI structure as in Figure III-27 was used. Die area of $25\ mm^2$. (b) The same SOI structure as in Figure III-29a has been used with die area equal to $25 \cdot 10^{-3}\ mm^2$.

III.4 Conclusions and perspectives

Diab *et al.* [53] and Fernandez *et al.* [54] have proposed for the first time the split-CV technique for the characterization of bare SOI wafers in pseudo-MOSFET configuration. Their work focused on the effective mobility extraction and thanks to a fitting parameter which was the effective surface (S_{eff}), they have obtained realistic results.

In this chapter, a further investigation of the measurement setup has been performed. The quality of the contact between the wafer and the metallic chuck plays a major role. In order to avoid parasitic capacitances, the use of vacuum contact is mandatory. In this way the active area is the whole die area and the extraction of effective mobility becomes straightforward. It has been also proved the secondary role played by the quality of probe contact. Pressure, position and number of probes on the top silicon film do not limit the characteristics.

Moreover, Diab *et al.* [97] have also presented a RC model to describe the frequency effects on C-V characteristics. During our work, the model validity has been validated using vacuum back contact and for different measurements: C_{m_split}-V_G, G_{m_split}-V_G, C_{m_split}-ω and G_{m_split}/ω-ω. In all the cases, a remarkable agreement has been found. The model was also tested on ultra-thin SOI structures and it can also predict the impact of different number of probes or die area.

The possibility to extract interface trap density has also been investigated. D_{it} contribution was included in the RC model. Experimental and simulation results showed that neither C_{m_split}-V nor G_{m_split}-ω characteristics can help to interface quality evaluation. The analysis has pointed out that the detection limit is due to high τ_{RC} magnitude. The use of smaller dies could make D_{it} extraction possible in split-CV configuration, but this is difficult to achieve in a practical case, due to the probe dimensions.

There are two possible perspectives of this work:

Double G_{m_split}/ω peak

The RC model predicts well the measured G_{m_split}/ω curves before and after the channel formation. Nevertheless, an interesting effect was obtained for higher gate bias (V_G much higher than V_T or much lower than V_{FB}). Figure III-30 shows an example of the measured C_{m_split} (a) and G_{m_split}/ω (b) versus angular frequency on a SOI wafer with *88 nm* top silicon film thickness and *145 nm* BOX thickness for different gate bias after V_T. In case of low V_G, the capacitance and G_{m_split}/ω curves are similar to the model. Increasing the gate bias magnitude, a "*shoulder*" rises up in the measured characteristic. At the same time, G_{m_split}/ω peak decreases and for high V_G (*i.e.*, $V_G = 15\ V$) a second peak appears at higher angular frequency values. According to the RC model, after the channel formation the gate bias should only induce a peak shift towards higher angular frequency values, but not a height decrease. It is may be due to self-heating or substrate drop potential effects [103].

Overcome RC model limitations

It has been shown that split-CV technique cannot address the study of interface quality in pseudo-MOSFET configuration due to τ_{RC} limits. The theoretical possibility to overcome the problem suggested in Sec. III.3.3.3 was the use of smaller die area. This is not possible since physical probing limitations. Another possibility is the use much lower measurement frequency. The channel should be very close to equilibrium condition and τ_{RC} will not affect the characteristics anymore. The lowest measuring frequency in split-CV configuration is around *20 Hz* and it is not enough. The quasi-static capacitance technique allows the capacitance measurement at equivalent frequency around *0.1 Hz* or lower. A detailed discussion of this technique, its measurement setup and the possibility to extract interface trap density will be presented in the next chapter.

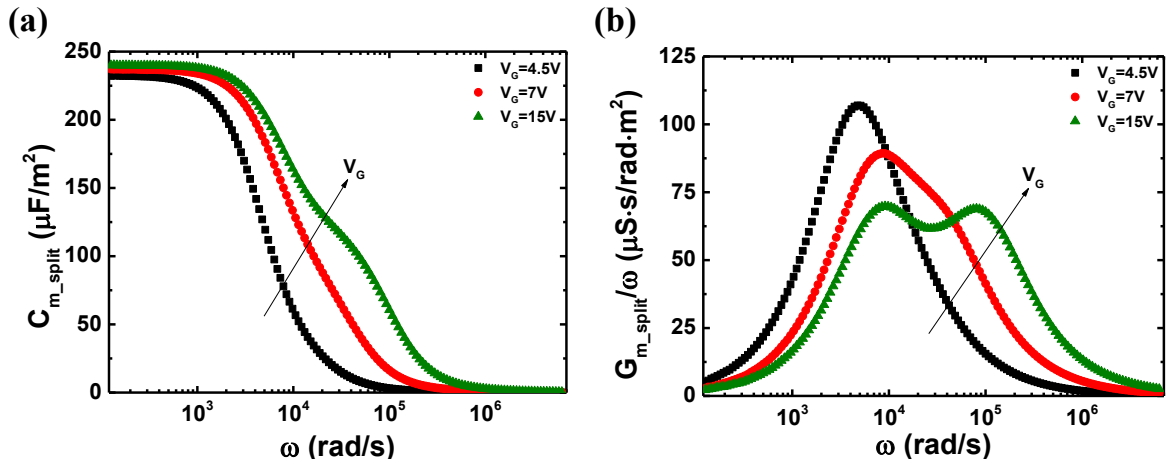

Figure III-30 C_{m_split} (a) and G_{m_split}/ω (b) versus angular frequency for different gate bias. The SOI structure had *88 nm* top silicon film thickness and *145 nm* BOX thickness and non-passivated top surface.

Chapter IV:

Quasi-static capacitance in Ψ-MOSFET

In the previous chapter we have proved that D_{it} detection cannot be achieved using standard LCR meters (split-CV). Nevertheless, the investigation of capacitance measurements for interface quality still remains an interesting goal. A reduced frequency could turn the CV into a successful method: this is the quasi-static CV.

In this chapter, small signal quasi-static technique will be applied to pseudo-MOSFET for the characterization of bare SOI wafers. After the optimization of the measurement setup, a physical model will be presented to describe the characteristics. A procedure to extrapolate the interface trap density, based on experimental results is discussed. Several types of wafers (geometry, passivation) will be characterized and the nature of the obtained D_{it} will be evidenced.

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IV.1 Introduction: quasi-static CV in MOS structures

In MOS capacitors the detection of deep traps is difficult to achieve. Standard C-V analysis performed using LCR meter is limited by frequency effects [104]. Small signal quasi-static capacitance (QSCV) technique may overcome the problem [98], [105]–[107].

The measurement setup requires connecting the device substrate to low potential. The gate contact is linked to the high potential and it is polarized by static bias (V_G). A small linear *a.c.* ramp signal (ΔV_{ramp_ac}) is added to V_G [104]. ΔV_{ramp_ac} induces charge variations in the conduction channel; ΔI is measured and leads to capacitance values [108]. This configuration allows performing characteristics at slow equivalent frequency f (*i.e.*, few *mHz*). To perform correct analysis, it is important to verify that leakage currents are negligible through the oxide of the device under test.

Typical examples of low frequency (C_{lf}) and high frequency (C_{hf}) capacitance traced as a function of gate bias are reported in Figure IV-1a [56]. The interface traps induce a shift between the two curves between accumulation and inversion regimes. The difference between the two capacitance terms (fast and slow) leads to D_{it} estimation (high-low frequency method). This procedure is largely used for the characterization of interface traps density in case of standard MOS capacitors [56], [100].

QSCV also allows computing the surface potential, thus the corresponding D_{it} energy in the silicon band gap. Performing the measurement at slow frequency (C_{LF_MOS}), the device is close to equilibrium condition and the whole channel response is obtained. Dividing C_{LF_MOS} by C_{OX} and integrating the results over V_G, one obtains [98], [106], [107]:

$$\Psi_S(V_G) = \int_{V_{FB}}^{V_G} \left(1 - \frac{C_{LF_MOS}(V_G)}{C_{OX}}\right) dV_G - \Psi_b \qquad \text{(IV.1)}$$

where Ψ_b is the bulk potential deduced from the doping concentration. Note that Eq. (IV.1) is not valid in case of gross non-homogeneities present at silicon interface [106].

Figure IV-1b shows the traps distribution as a function of energy measured on MOS in case of (111) (A) and (100) (B) silicon crystal orientation [56]. Conductance method (squares) and QSCV technique (circles) were used. Obviously, the quasi-static measurement gives access to deep traps, close to the mid-gap, while the conductance technique is more sensitive to the edge of the band gap.

Besides its attractive features, the QSCV has also some drawbacks:

- It is only sensitive to charged defects [98];
- The characteristic may be affected by potential fluctuations due to detrapping effects that lead to instability on the measurements [56];
- It is not adapted for D_{it} located at the edges of the band gap [56].

QSCV in Ψ-MOSFET may become very interesting if it can lead to similar results concerning the interface quality of bare SOI wafers.

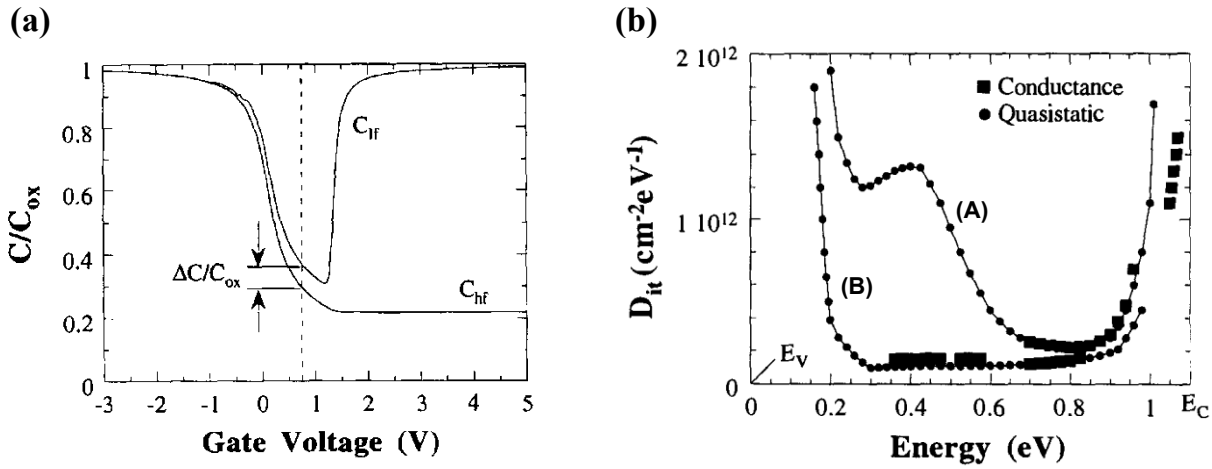

Figure IV-1: High and low frequency capacitance measurements performed on MOS capacitor. D_{it} extracted as a function of energy in a MOS capacitor in case of (111) (A) and (100) (B) p-Si. Conductance (square symbols) and quasi-static (circle symbols) techniques were used [56].

IV.2 Quasi-static capacitance in pseudo-MOSFET

The previous chapter demonstrated that the conductance method is not suitable in Ψ-MOSFET configuration but also suggested that D_{it} characterization on bare SOI wafers could be achieved by low frequency measurements (corresponding to QSCV). In Sec. IV.2.1 we will show the setup of QSCV in Ψ-MOSFET. Sec. IV.2.2 compares measurements performed using quasi-static technique and LCR meter on the same SOI sample.

IV.2.1 Basics of QSCV for Ψ-MOSFET

The samples are probed by Jandel® station. The SOI wafer is placed on a metallic chuck. The substrate is connected to the high potential acting as a gate (similar to LRC meter setup). The low potential is applied on the top silicon film through one (or more) probe (Figure IV-2a). Small signal quasi-static measurements are performed using the Agilent B1500A® [107].

A particular polarization is required to perform the analysis (see Figure IV-2b). Static gate bias V_G is applied to the metallic chuck and the vertical current (I) between the high and the low potential is measured. A small linear *a.c.* ramp bias is added to V_G and a new I is measured at half ramp period. Integrating the current-time evolution leads to the charge and then to the capacitance value for a given V_G.

Two important parameters define the *a.c.* signal: the bias amplitude ΔV_{ramp_ac} and the time period over which it is applied (t_m). Thus, the *a.c.* scan speed is estimated by:

$$v_{ramp_ac} = \frac{\Delta V_{ramp_ac}}{t_m} \qquad \text{(IV.2)}$$

For simplicity reasons we have chosen to keep $\Delta V_{ramp_ac} = 50\ mV$ for all the characteristics. Hence, different v_{ramp_ac} are obtained using different t_m. Therefore, slow *a.c.* scan speed is given by long time ramp t_m and it is equivalent to slow measurement frequency ($f = 1/t_m$). The static polarization (V_G step and delay time) is kept constant when changing v_{ramp_ac} on the same SOI structure.

QSCV configuration requires neither open nor short circuit corrections. The characterization is performed by current measurements and at very slow *f*. Thus, parasitic capacitances play a minor role, unlike the case of LCR meter [108]. Effects due to possible leakage terms are reduced thanks to the comparison of the measured current before and after applying v_{ramp_ac} [108].

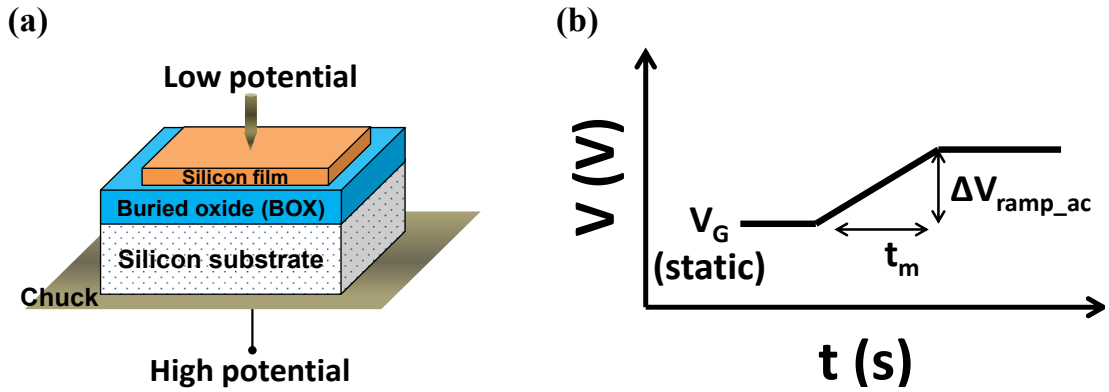

Figure IV-2: (a) Measurement setup of QSCV technique for bare SOI wafers in pseudo-MOSFET configuration. (b) Schematic of the gate bias required to achieve QSCV capacitance measurements.

Preliminary results of quasi-static characterization performed in pseudo-MOSFET configuration are reported in Figure IV-3. The capacitance (C_{m_QST}) is obtained as a function of V_G using slow (plain symbols) and fast (empty symbols) *a.c.* scan. In strong inversion or accumulation regimes both measured characteristics reach the C_{OX} value. Around $V_G \approx 0\ V$, two "*shoulders*" rise up for slow *f*. These signatures may lead to the investigation of traps present at the interfaces of the top silicon film.

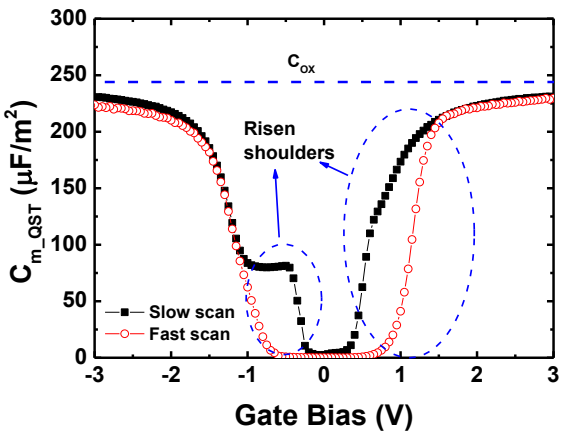

Figure IV-3: Measured QSCT capacitance C_{m_QST} as a function of gate bias measured in case of slow (*10 mV/s*) (plain symbols) and fast (*1 V/s*) (empty symbols) v_{ramp_ac}. SOI structure with *88 nm* top silicon film thickness, *145 nm* BOX thickness, and passivated top surface.

IV.2.2 Comparison with LCR meter measurements

Both split-CV and QSCV techniques lead to capacitance measurements. Thus, one expects that, even if the bias schemes are different (*i.e.*, sinusoidal *a.c.* bias for LCR meter and linear *a.c.* ramp polarization for QSCV technique), similar characteristics should be obtained when using comparable frequencies. Figure IV-4 shows the measured capacitance versus gate bias in split-CV (plain symbols) and quasi-static (empty symbols) technique on the same die. Split-CV characterization has been performed using the slowest frequency available on the LCR meter ($f = 20\ Hz$). The equivalent ramp speed can be roughly estimated considering the signal amplitude (δV_G) of the LCR meter and the period over which it is applied ($1/f$):

$$v_{ramp_ac} = f \cdot \delta V_G = 20 \cdot 26 \cdot 10^{-3} \approx 0.5\,V/s \qquad \text{(IV.3)}$$

This corresponds to a fast *a.c.* scan performed in QSCV (empty symbols). For the quasi-static experiment, $v_{ramp_ac} = 1\ V/s$ was used. The two curves behave similarly. For high gate bias, the oxide capacitance dominates in both cases. Furthermore, before channel formation, no traps signature is evidenced. Small variations of threshold and flat-band voltages are found, probably due to the different setups. In general, however, QSCV characteristics performed using fast *a.c.* scan lead to similar LCR meter curve. This continuity between quasi-static CV and split-CV technique allows us to use most of the modeling results discussed in the previous chapter.

D_{it} signature is expected only in absence of the channel (see Figure IV-3). Thus, in the following sections we will focus on the region where the conduction channel is only partially or not yet created.

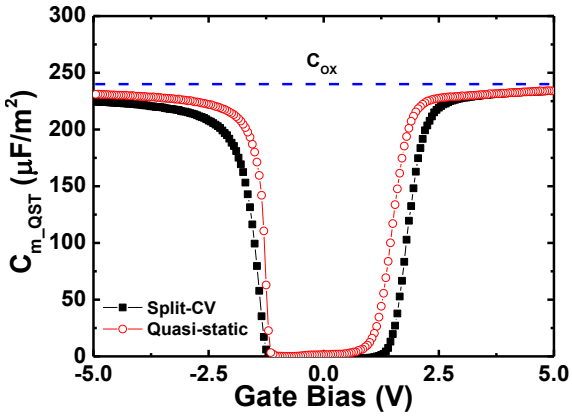

Figure IV-4: Measured capacitance versus gate bias obtained using LCR meter (plain symbols) and quasi-static technique (empty symbols) on passivated SOI structure with *88 nm* thick Si film and *145 nm* thick BOX using similar v_{ramp_ac}: *0.5 V/s* and *1 V/s*, respectively.

IV.3 Impact of measurement parameters

Before proceeding to any modeling and D_{it} extraction, we need to find the appropriate QSCV experimental setup. Quality of the back contact and probe role will be discussed in Sec. IV.3.1 and Sec. IV.3.2, respectively. Afterwards, the importance of scan direction will be clarified (Sec. IV.3.3).

IV.3.1 Impact of back contact quality

The quality of the back contact was critical in split-CV to avoid parasitic capacitances which were reducing C_{max} values [70]. Is this the case here for quasi-static CV?

Figure IV-5a shows the measured capacitance using fast *a.c.* scan speed (*1 V/s*) without (empty symbols) and with (plain symbols) vacuum. A parasitic capacitance appears in absence of vacuum. Thus, the obtained maximum value is much lower than C_{OX}. On the contrary, when the vacuum was used on the back contact, C_{m_QST} after channel formation is very close to the expected C_{OX} value. Furthermore, V_T differs, much more than in case of measurements performed using LCR meter.

Figure IV-5b shows QSCV characteristics in case of slow *a.c.* ramp speed (v_{ramp_ac} = *10 mV/s*). Curve overlap is obtained. v_{ramp_ac} is very slow and the parasitic terms do not affect the results. This conclusion further validates the hypothesis that the use of vacuum system becomes mandatory only in case of rapid time dependent signals. In case of static polarization or for very slow V_G variation close to equilibrium, the parasitic effects become negligible. Similar results have also been demonstrated for standard MOS capacitors [98]; note that the vacuum contact was related to the silicon substrate and not to the gate.

Even if the curves measured using slow *a.c.* scan speed are almost independent of the back contact quality, all the characteristics of this chapter were performed using the vacuum system. This increases reproducibility and erases any doubt on possible parasitic capacitance effects.

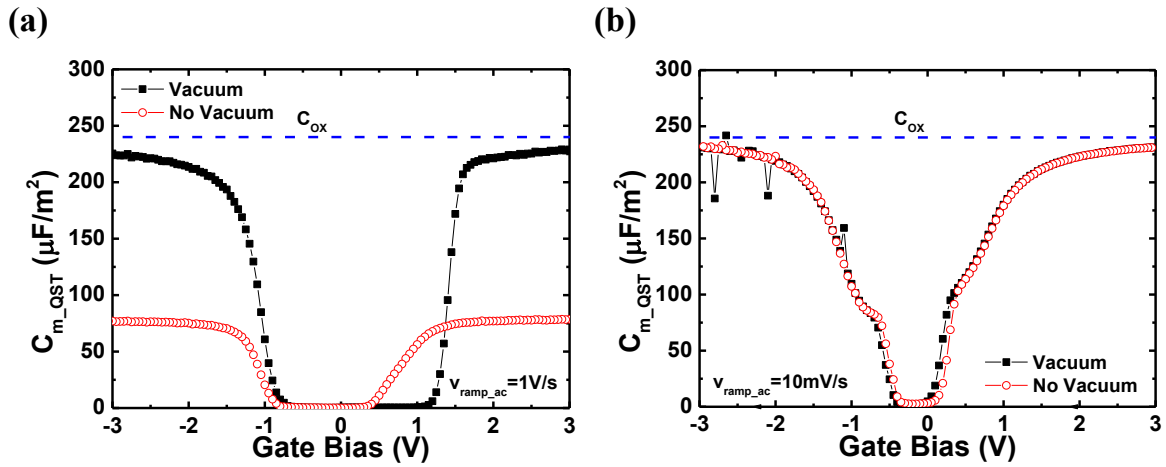

Figure IV-5: C_{m_QST} as a function of V_G in QSCV configuration. Characteristics obtained with (plain symbols) and without (empty symbols) using the vacuum system. Analysis performed using two different *a.c.* ramp speeds: v_{ramp_ac} = *1 V/s* (a) and v_{ramp_ac} = *10 mV/s* (b). SOI structure with *88 nm* thick Si film and *145 nm* thick BOX. The top silicon film was passivated.

IV.3.2 Impact of the probes

While performing static characteristics in pseudo-MOSFET configuration, the quality of the probe contact is a major parameter to achieve low access resistance and reliable parameter extraction (Sec. II.3.3). In case of split-CV measurements, however, R_{SD} had only a minor impact on the obtained characteristics (Sec. III.2.3). It is mandatory to verify the importance of R_{SD} during QSCV characterization.

Pressure effects

Figure IV-6 shows the C_{m_QST} versus V_G in case of different probe pressures. Superposition is obtained, showing that, as for the split-CV, in quasi-static configuration the probe pressure plays a minor role [70]. The "*shoulders*" representing the D_{it} are therefore pressure independent. This indicates that D_{it} extracted in QSCV are not due to only defects induced by probe penetration. Furthermore, good QSCV characteristics can be obtained without particular precautions on the pressure value. Consequently, even very low pressures lead to accurate capacitance curves which is not the case for I_D-V_G. This fact makes the QSCV more adapted for ultra-thin films than the current measurements. Results on the ultra-thin films and BOX will be discussed in Sec. IV.8.

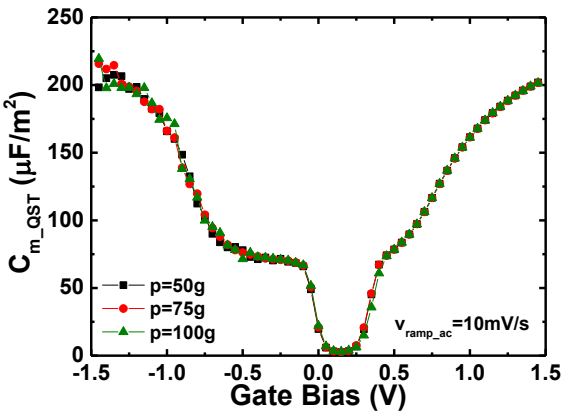

Figure IV-6: QSCV capacitance versus gate bias for different probe pressures. The SOI structure had *88 nm* top silicon film thickness and *145 nm* BOX thickness. Passivated top surface.

Different probe quality and number

Figure IV-7a shows the measured QSCV capacitance versus gate bias obtained using two different needles on the silicon surface with the same pressure: probe A (plain symbols) and probe B (empty symbols). The curves superposition confirms that the obtained "*shoulders*" are independent of the top contact quality.

The number of probes placed on the top silicon film changed the frequency response of the SOI structure in split-CV. The higher the measurement frequency, the stronger the impact on the characteristics (Sec. III.3). On the contrary, in quasi-static configuration, *f* is sufficiently low and no frequency attenuation is expected. This is confirmed by the measurements in Figure IV-7b performed using one and three probes on the Si film.

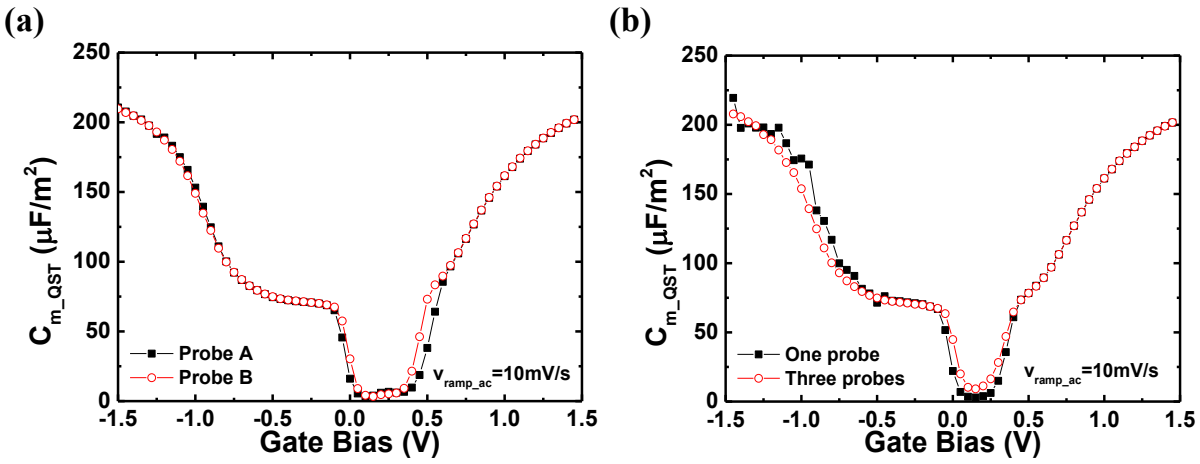

Figure IV-7: (a) Measured QSCV capacitance as a function of gate bias using slow v_{ramp_ac}. Two different probes from the same station were used: A (plain symbols) and B (empty symbols). (b) Measured QSCV capacitance as a function of gate bias using one (plain symbols) and three (empty symbols) probes placed on the top silicon film. Characterization performed on the same SOI structure as in Figure IV-6.

IV.3.3 Impact of scan direction

In standard MOS capacitor the scan direction is a major parameter for interface characterization [109]. Starting the measurement from accumulation or strong inversion regime leads to different information [105]. When performing the sweep from accumulation regime, the device may enter the out-of-equilibrium deep depletion regime instead of the inversion regime. Alternatively, a scan started from strong inversion regime makes D_{it} investigation more fruitful, since more defects will be charged.

Figure IV-8a shows the measured capacitance as a function of gate bias using slow *a.c.* scan speed in Ψ-MOSFET configuration. The analysis of SOI structure with *88 nm* thick Si film and *145 nm* thick BOX has been started respectively from accumulation (empty symbols) and from strong inversion (plain symbols) regime. After channel formation, the two characteristics overlap at C_{OX}. Between V_{FB} and V_T the curve measured from positive V_G shows larger instability than for the curve started from accumulation regime. The effects are amplified in case of thin top silicon film (Figure IV-8b for SOI structure with *12 nm* Si thickness, *145 nm* BOX thickness and non-passivated surface). The characteristic started from strong inversion regime (empty symbols) shows two "*shoulders*" when the conduction channel is not yet created. On the contrary, the measurement performed from negative gate bias (plain symbols) presents no D_{it} signature. Before threshold voltage, the curve started from $V_G < 0\ V$ becomes very noisy, probably because of the lack of carriers [5]. The potential is pinned above V_T and just after it the capacitance jumps directly to C_{OX}. This explains the presence of capacitance values higher than C_{OX} which are not physical [110]. Clear hysteresis is also found between the two characteristics probably due to the effects of surface defects or mobile charge [6], [111].

In conclusion, measurements started from strong inversion regime represent the more favorable condition to evidence D_{it} signature. All the characteristics shown in this chapter were obtained starting from strong inversion regime ($V_G > 0\ V$).

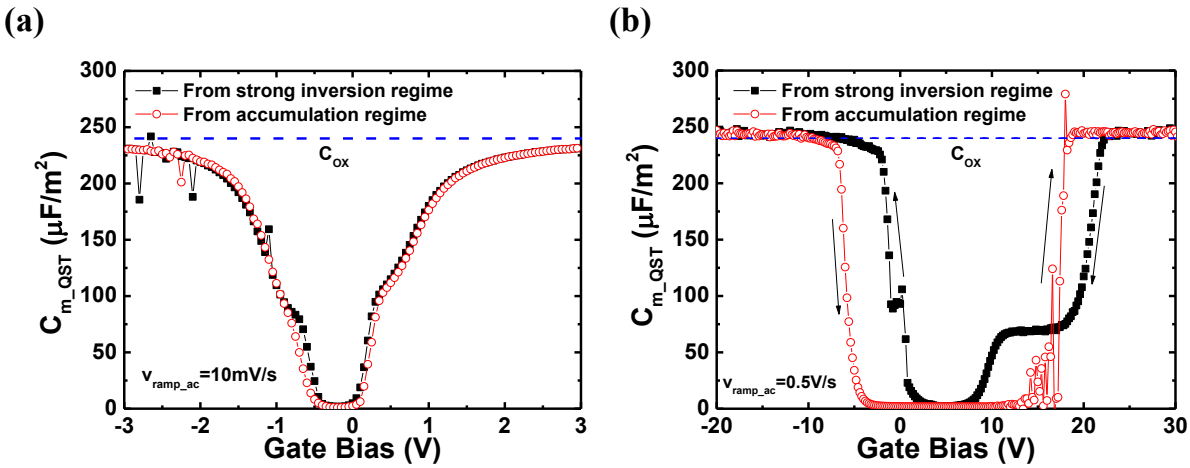

Figure IV-8: Measured QSCV capacitance versus V_G with two different sweep directions: starting from accumulation (plain symbols) and from strong inversion (empty symbols) regime. Two samples were tested: one with *88 nm* top silicon film thickness (a) and another with t_{Si} = *12 nm* (b). In both cases the buried oxide was *145 nm* thick.

IV.4 D_{it} model

Before pursuing with D_{it} extraction, a physical model is required to describe the phenomenon giving rise to the capacitance "*shoulders*" (Sec. IV.4.1). The model will represent the base to achieve correct parameters extraction. It is validated by comparisons between experimental and calculated results (Sec. IV.4.2). For simplicity reasons, all the analyses in this section were performed on SOI structure with *88 nm* thick top silicon film and *145 nm* thick BOX. The top surface was passivated.

IV.4.1 Model derivation

The derivation will be divided in three sections. Initially the equations will be presented for a single energy level of interface traps. The model will then be extended to the continuum-like energy distribution of defects and finally the frequency effects will be included.

The experimental quasi-static capacitance will be labeled as C_{m_QST} and the computed one as C_{QST}.

Single energy level of interface traps

The measured peaks obtained before channel formation can be modeled deriving the whole C_{QST} expression. The total density of charges induced by the gate bias (Q_{ch}) is distributed between the free charges present in the channel Q_i and the charges trapped in the defects (Q_{itrap}) [100]:

$$Q_{ch} = Q_i + Q_{itrap} \tag{IV.4}$$

For a single traps energy level, the filled charges at the interface are given by:

$$Q_{itrap} = Q_{itrap_s} = q \cdot D_{it_s} \cdot f_T \tag{IV.5}$$

where f_T is the probability that the traps are charged. D_{it_s} is the density of defects for a single energy level expressed in cm^{-2} and associated to a precise value of surface potential (Ψ_S), thus to V_G.

The derivation of the total charge with respect to the gate bias leads to the QSCV capacitance for a single energy level of D_{it} (C_{QST_s}):

$$C_{QST_s} = \frac{\delta Q_{ch}}{\delta V_G} = \frac{\delta Q_i}{\delta V_G} + \frac{\delta Q_{itrap_s}}{\delta V_G} \tag{IV.6}$$

Charge calculations are usually performed as a function of Ψ_S. Hence, it is possible to re-write Eq. (IV.6) as:

$$C_{QST_s} = \frac{\delta Q_i}{\delta \Psi_S} \cdot \frac{\delta \Psi_S}{\delta V_G} + \frac{\delta Q_{itrap_s}}{\delta \Psi_S} \cdot \frac{\delta \Psi_S}{\delta V_G} \tag{IV.7}$$

To make the derivation easier to follow, the two terms will be discussed separately and the final capacitance will be shown at the end.

In standard MOS capacitor, Q_i is proportional to $exp(\beta \cdot \Psi_S)$, where $\beta = q/(k \cdot T)$ [5]. Thus, the first term present in Eq. (IV.7) becomes:

$$\frac{\delta Q_i}{\delta \Psi_S} \cdot \frac{\delta \Psi_S}{\delta V_G} = \beta \cdot Q_i \cdot \frac{\delta \Psi_S}{\delta V_G} \tag{IV.8}$$

The derivative of the trapped charges with respect to the surface potential leads to the capacitance associated to a single energy level of D_{it}:

$$C_{it_s} = \frac{\delta Q_{itrap_s}}{\delta \Psi_S} \tag{IV.9}$$

In order to complete the derivation of C_{QST_s}, the expression of the surface potential with respect to the gate bias is required. V_G is distributed between Ψ_S, the flat-band voltage and the potential drop due to the inversion charges and Q_{itrap_s} [5]. Ψ_S is written as:

$$\Psi_S = V_G - V_{FB} - \frac{Q_i + Q_{itrap_s}}{C_{OX}} \tag{IV.10}$$

Deriving Eq. (IV.10) with respect to V_G one obtains:

$$\frac{\delta \Psi_S}{\delta V_G} = 1 - \frac{1}{C_{OX}} \cdot \frac{\delta Q_i}{\delta V_G} - \frac{1}{C_{OX}} \cdot \frac{\delta Q_{itrap_s}}{\delta V_G} = 1 - \frac{1}{C_{OX}} \cdot \frac{\delta Q_i}{\delta \Psi_S} \cdot \frac{\delta \Psi_S}{\delta V_G} - \frac{1}{C_{OX}} \cdot \frac{\delta Q_{itrap_s}}{\delta \Psi_S} \cdot \frac{\delta \Psi_S}{\delta V_G} \tag{IV.11}$$

Using Eqs. (IV.8) and (IV.9), the derivative of the surface potential with respect to the gate bias becomes:

$$\frac{\delta \Psi_S}{\delta V_G} = \frac{C_{OX}}{C_{OX} + \beta \cdot Q_i + C_{it_s}} \tag{IV.12}$$

Thus, the total channel capacitance with a single energy level of interface traps is (Eq. (IV.6)):

$$C_{QST_s} = \frac{C_{OX} \cdot \left(\beta \cdot Q_i + C_{it_s}\right)}{C_{OX} + \beta \cdot Q_i + C_{it_s}} \tag{IV.13}$$

QSCV technique is only sensitive to the charged defects, so the filling probability needs to be included in C_{it_s}. The probability that electrons (or holes) are trapped by D_{it} can be derived using Shockley-Read-Hall approach [112], [113]. It is usually expressed as a function of the electron density present in the channel (n_S), which is proportional to $exp(\beta \cdot \Psi_S)$, as Q_i. Hence, it is possible to perform the derivation using the inversion (or accumulation) charge density instead of n_S. In case of small signal variation, the probability f_T that the traps are charged is given by the balance between the free charges present in the conduction channel filling the traps $Q_i \cdot (1-f_T)$ and the filled defects discharging towards the channel $Q_{itrap_s} \cdot f_T$ [114]:

$$\frac{\partial f_T}{\partial t} = \frac{\vartheta}{q} \cdot Q_i \cdot (1 - f_T) - \frac{\vartheta}{q} \cdot Q_{itrap_s} \cdot f_T \tag{IV.14}$$

where ϑ is given by the product between the traps cross section σ_T and the frequency f_s at which the electrons oscillate between the conduction channel and the traps [112]:

$$\vartheta = \sigma_T \cdot f_s \tag{IV.15}$$

In case of steady-state condition ($\delta f_T/\delta t = 0$), f_T becomes:

$$f_T = \frac{Q_i}{Q_i + Q_{itrap_s}} \tag{IV.16}$$

Thus, the capacitance associated to a single energy level of traps is:

$$C_{it_s} = q \cdot D_{it_s} \cdot \frac{\delta f_T}{\delta \Psi_S} = q \cdot D_{it_s} \cdot \frac{Q_{itrap_s}}{\left(Q_i + Q_{itrap_s}\right)^2} \cdot \beta \cdot Q_i \tag{IV.17}$$

In the next section, the model will be extended to the continuum-like energy distribution of traps in the silicon band gap case.

Continuum-like energy distribution of D_{it}

In case of a single energy level of interface traps, the defects are located only at one precise value of gate bias (*i.e.*, surface potential). As shown also from the QSCV preliminary results (Figure IV-1b and Figure IV-3), D_{it} energy is more homogenously distributed in the silicon band gap instead of a peak at a certain value [100]. In order to emulate this effect from the mathematical point of view, a sum of several C_{it_s} in the silicon band gap will lead to the continuum-like D_{it} capacitance [115]. This corresponds to an integral in the silicon band gap. Since we control the Fermi level in the silicon film with V_G (back gate bias), the integral is performed as a function of bias between V_{FB} and a certain value smaller than V_T:

$$C_{it_c}(V_G) = \int_{V_{FB}}^{V_G} C_{it_s}(x)dx = \int_{V_{FB}}^{V_G} q \cdot D_{it} \cdot \frac{Q_{itrap_s}(x)}{\left(Q_i(V_G) + Q_{itrap_s}(x)\right)^2} \cdot \beta \cdot Q_i(V_G) \cdot dx \tag{IV.18}$$

Since we are considering a continuum-like energy distribution of traps, D_{it} is expressed in $cm^{-2}eV^{-1}$. C_{it_c} is the defects capacitance term which replaces C_{it_s} in Eq. (IV.13). Thus, the quasi-static channel capacitance (C_{QST_c}) is as a function of C_{OX}, $\beta \cdot Q_i$ and C_{it_c}:

$$C_{QST_c} = \frac{C_{OX} \cdot \left(\beta \cdot Q_i + C_{it_c}\right)}{C_{OX} + \beta \cdot Q_i + C_{it_c}} \tag{IV.19}$$

Figure IV-9 shows the simulated QSCV capacitance versus V_G in three different configurations: without any defect contribution (continuous line), with a single energy level (dashed line) and a continuum-like energy distribution (point-dashed line) of interface traps density. The used D_{it} magnitude was $10^{11}cm^{-2}$ in Eq. (IV.13) and $10^{11}cm^{-2}eV^{-1}$ for Eq. (IV.19). As for the experimental results, the calculated curves superpose after channel formation. In case of single energy level of defects, a sharp peak is obtained in absence of conduction channel. For this calculation, the defects were placed at $V_G = 0\ V$. Using a continuum-like energy distribution of interface traps density (point-dash line), a "*plateau*", similar to the experimental results (see Figure IV-3), is obtained. Even if the traps magnitude was similar for the single energy level and the continuum-like energy case, the height of the "*plateau*" is much lower than the sharp peak. The same trends were also obtained for standard MOS capacitors [100].

To complete the derivation, frequency effects have to be also included in C_{QST}.

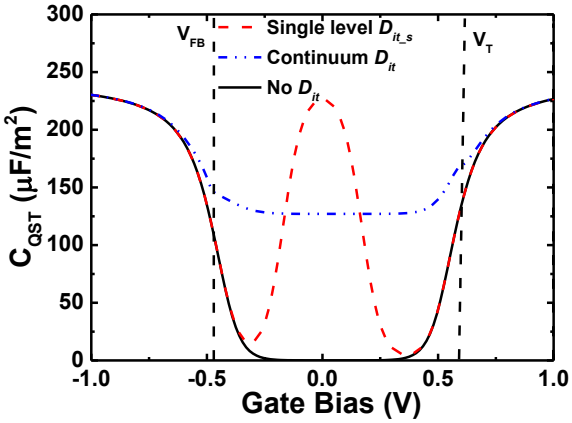

Figure IV-9: Simulated C_{QST} versus gate bias without (continuum line) and with interface traps contribution. A single energy level ($D_{it_s} = 10^{11}cm^{-2}$, dashed line) and continuum-like ($D_{it_c} = 10^{11}cm^{-2}eV^{-1}$, point-dash line) traps energy distribution were used. SOI with *88 nm* thick top silicon film and *145 nm* thick BOX.

Frequency effects

In time, the defects can be filled by free carriers present in the conduction channel or they can discharge. Thus, it is important to include the traps time constant τ_{Dit} in the capacitance term. For a given value of surface potential, τ_{Dit} is related to the density of filled D_{it} (n_{it}) and the density of free charges present in the channel (n_S) [116]. As for a MOS capacitor, τ_{Dit} can be written as [100], [117]:

$$\tau_{Dit} = \frac{1}{\sigma_T \cdot v_{th} \cdot n_S + \sigma_T \cdot v_{th} \cdot n_{it}} \qquad \text{(IV.20)}$$

where v_{th} is the thermal velocity. The carrier cross section σ_T was kept the same for filling and discharging processes. Note that before channel formation $n_S = n_i$ and it is much lower than n_{it}. Thus, all the free carriers are trapped by the defects.

The capacitance contribution due to interface traps containing the defects time constant contribution becomes [56], [118]:

$$C_{it_c_\tau} = \frac{C_{it_c}}{1+\omega^2 \cdot \tau_{Dit}^2} \tag{IV.21}$$

In order to include the filling/discharging traps effects, Eq. (IV.21) must be used in the computation of C_{QST}:

$$C_{QST_c_\tau} = \frac{C_{OX} \cdot \left(\beta \cdot Q_i + \frac{C_{it_c}}{1+\omega^2 \cdot \tau_{Dit}^2} \right)}{C_{OX} + \beta \cdot Q_i + \frac{C_{it_c}}{1+\omega^2 \cdot \tau_{Dit}^2}} \tag{IV.22}$$

Extension to split-CV

In the split-CV chapter, it was demonstrated that the free carriers need time to go from the probes to a certain point of the channel (τ_{RC}) (Sec. III.3.1). Thus, one needs to include also τ_{RC} effects in order to have a full capacitance expression:

$$C_{QST_LCR} = \frac{1}{1+\left(\omega \cdot \tau_{RC}\right)^2} \cdot \frac{C_{OX} \cdot \left(\beta \cdot Q_i + \frac{C_{it_c}}{1+\omega^2 \cdot \tau_{Dit}^2} \right)}{C_{OX} + \beta \cdot Q_i + \frac{C_{it_c}}{1+\omega^2 \cdot \tau_{Dit}^2}} \tag{IV.23}$$

As explained in the split-CV chapter, only traps with $\tau_{Dit} > \tau_{RC}$ can be detected. Note that in quasi-static configuration, even the characteristics measured with "*fast*" *a.c.* ramp speed are actually equivalent to "*slow*" analysis performed using LCR meter, where τ_{RC} had no impact. Consequently, in QSCV, thanks to its slow equivalent frequency, τ_{RC} can be safely neglected and Eq. (IV.22) will be sufficient for modeling the measured capacitance.

This model will be validated in the next section.

IV.4.2 Model validation

In this section, the derived equations will be constantly compared to experimental results in order to confirm the robustness of our model. Note that the aim of this part is not to perfectly fit the curves, but to verify the trends. Frequency effects and characteristics performed at different temperatures will be investigated. Equation (IV.22) is used to compute the total capacitance. Q_i is calculated using Lambert equation [99]. C_{OX} is obtained from experimental capacitance measured in strong inversion (or accumulation) regime. D_{it} was equal to 10^{11} $cm^{-2}eV^{-1}$, which is a typical order of magnitude for these types of samples [49], [62], [83].

Frequency effects

As discussed in the introduction, fast *a.c.* ramp scan (v_{ramp_ac} = *1 V/s*) hides the traps contribution while v_{ramp_ac} = *10 mV/s* reveals them. Figure IV-10a shows C_{m_QST} versus gate bias obtained using different v_{ramp_ac}. Again, the use of slower *a.c.* ramp speed enhances the D_{it} signature. Figure IV-10b presents the calculated $C_{QST_c_\tau}$ capacitance using Eq. (IV.22) for different frequencies. Very similar trends to the experimental results are obtained, validating the evolution with *f* (or *a.c.* ramp scan).

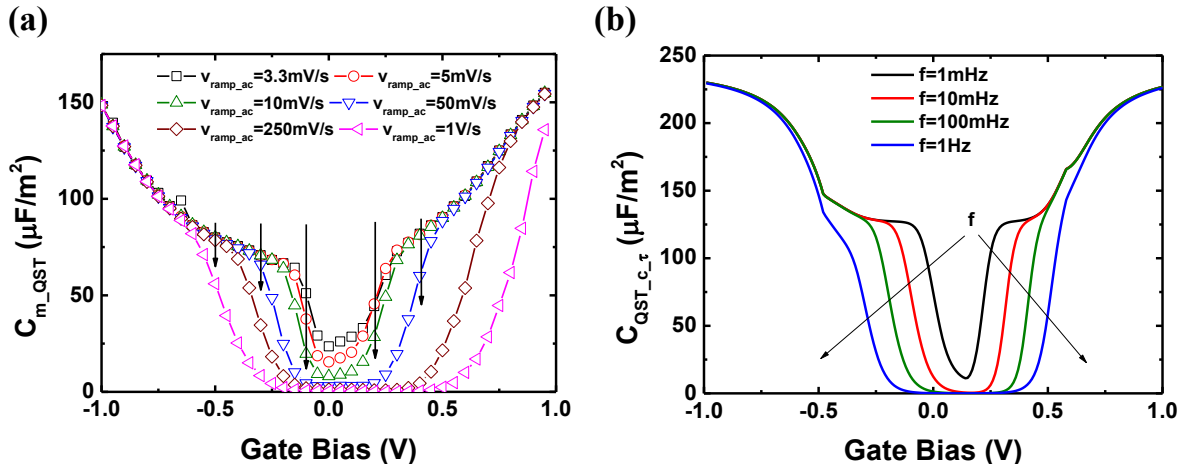

Figure IV-10: Measured (a) and calculated (b) quasi-static capacitance versus gate bias for varius *a.c.* ramp speed and frequency, respectively. The passivated SOI structure had t_{Si} = *88 nm* and *145 nm* BOX. The arrows in Figure IV-10a represents the gate bias values chosen to compute the quasi-static capacitance as a function of *a.c.* ramp time t_m (labeled $C_{m_QST_Vg}$).

At constant V_G, the filling (or discharging) D_{it} kinetics should have an exponential dependency as a function of *a.c.* ramp time t_m [117], [119]:

$$C_{m_QST_Vg} = C_{m_QST_sat} \cdot \left(1 - e^{-t_m / \tau_{Dit}}\right) \tag{IV.24}$$

where $C_{m_QST_sat}$ is the quasi-static saturation capacitance, when the whole density of traps responds to the applied signal. In order to verify if this relation is also valid in our case, we extracted the measured C_{m_QST} for some fixed V_G (*-0.5 V*, *-0.3 V*, *-0.1 V*, *0.2 V* and *0.4 V*) from Figure IV-10a (vertical arrows). $C_{m_QST_Vg}$ identifies the capacitance values obtained at constant gate bias and they are traced as a function of the *a.c.* ramp time t_m (symbols in Figure IV-11a). t_m is computed dividing the bias amplitude $\Delta V_{ramp_ac} = 50\ mV$ by the *a.c.* ramp speed (see Figure IV-2b). The exponential fit (dashed line) well matches with the experimental data. Note that for high magnitude of gate bias the characteristics saturate and $C_{m_QST_Vg}$ becomes equal to $C_{m_QST_sat}$. On the contrary, for $V_G = -0.1\ V$ and $0.2\ V$ the experimental curve is not yet complete. In this region not all D_{it} are charged. Thus, partially traps detection is obtained. The time scaling is in the order of seconds, which are typical values for deep traps time constants [109], [119], [120].

Figure IV-11b shows the measured τ_{Dit} (plain symbols) obtained from the fitting performed in Figure IV-11a as a function of gate bias. The carriers time constants computed using Eq. (IV.20) are also presented (dashed line). These values were calculated using $v_{th} = 10^7\ cm/s$ and $\sigma_T = 10^{-21}\ cm^{-2}$, which are typical orders of magnitude for deep traps [119]. The two characteristics have similar behavior. For large V_G magnitude, τ_{Dit} sharply decreases. In this region, the traps respond fast. Between V_T and V_{FB}, τ_{Dit} increases implying that deep traps are hard to detect. In case of experimental results (plain symbols) the curve saturates at $V_G \approx 0\ V$. The lowest *a.c.* measurement ramp is *3 mV/*s. Hence, traps with time constant larger than *16 s* (*50/3 = 16 s*) cannot be detected. Contrary, the computed τ_{Dit} (dashed line) increases to very large values that cannot be measured.

In conclusion, however, general agreement was found between experimental and calculated results. In the next section, we discuss the temperature dependency.

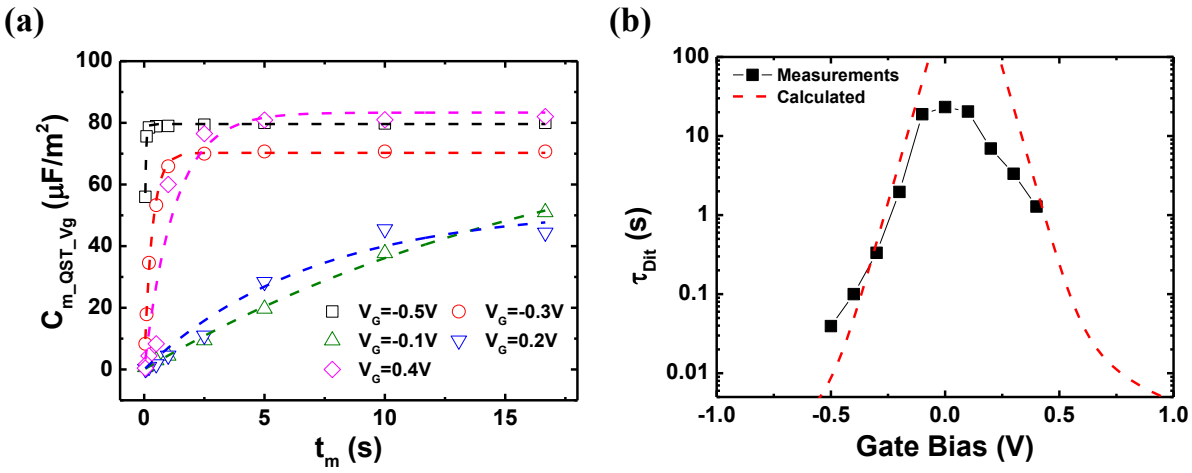

Figure IV-11: (a) $C_{m_QST_Vg}$ versus t_m for different gate bias: V_G = *-0.5 V*, *-0.3 V*, *-0.1 V*, *0.2 V* and *0.4 V*. Experimental data (symbols) from Figure IV-10a and exponential fit (dashed lines). (b) Corresponding traps time constants obtained from the exponential fit performed in Figure IV-11a (symbols) versus gate bias. Calculated values using Eq. (IV.20) are also reported (dashed line).

Temperature dependency

In order to further validate the physical model, quasi-static measurements were performed at low temperature (*T*). Figure IV-12 shows the measured capacitance at *T = 90 K* versus gate bias for different *a.c.* ramp speed. At high V_G the characteristics overlap and the obtained capacitance is always close to C_{OX}. The use of different *a.c.* scan rate has a much lower impact than at room temperature (compare Figure IV-12a and Figure IV-10a). At *T = 90 K* no clear signature due to interface traps is visible.

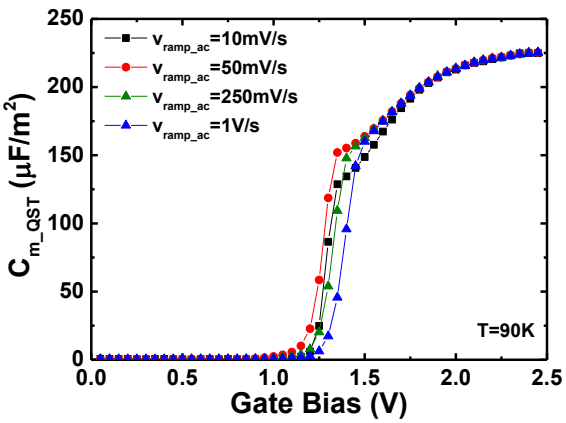

Figure IV-12: Measured quasi-static capacitance versus gate bias at *T = 90 K* for different *a.c.* ramp speed. The passivated SOI structure had *88 nm* thick Si film and *145 nm* thick BOX.

Figure IV-13a clarifies the mechanism: C_{m_QST} was measured versus V_G using the same v_{ramp_ac} = *10 mV/s* and different temperatures. Typical V_T shift as a function of T is observed [84]. The signature due to interface traps is stronger in case of higher temperatures.

In our model the temperature effects are present in the following terms:

- $\beta(T) = q/k{\cdot}T$;
- $Q_i(T)$: the inversion charge density Q_i in Eq. (IV.22) is calculated using Lambert equation [99], which contains $\beta(T)$ and $V_T(T)$. The variation of threshold voltage with respect to the temperature is determined by $\beta(T)$ and the intrinsic carrier concentration $n_i(T)$ [5], [84]:

$$n_i(T) = \sqrt{N_C \cdot N_V \cdot \left(\frac{T}{300}\right)^3} \cdot \exp^{\frac{-E_G}{2\cdot k\cdot T/q}} \qquad \text{(IV.25)}$$

  where N_C and N_V are the effective state density at T = *300 K* in conduction and valence band, respectively.
- The traps cross sections $\sigma_T(T)$ present in τ_{Dit} (see Eq. (IV.20)) is assumed constant, since the minimum temperature used is still too high for ionization effects to occur [5].

In order to check if the derived model can explain the temperature dependency, Figure IV-13b shows $C_{QST_c_\tau}$ versus gate bias in case of different temperatures. Equation (IV.22) was used, where the T effects were included in β and n_i, thus on Q_i. Comparing Figure IV-13b with the experimental results (Figure IV-13a), similar trends are obtained: V_T and the traps response vary with T.

In the next section, the proposed model will act as base to perform suitable D_{it} extraction.

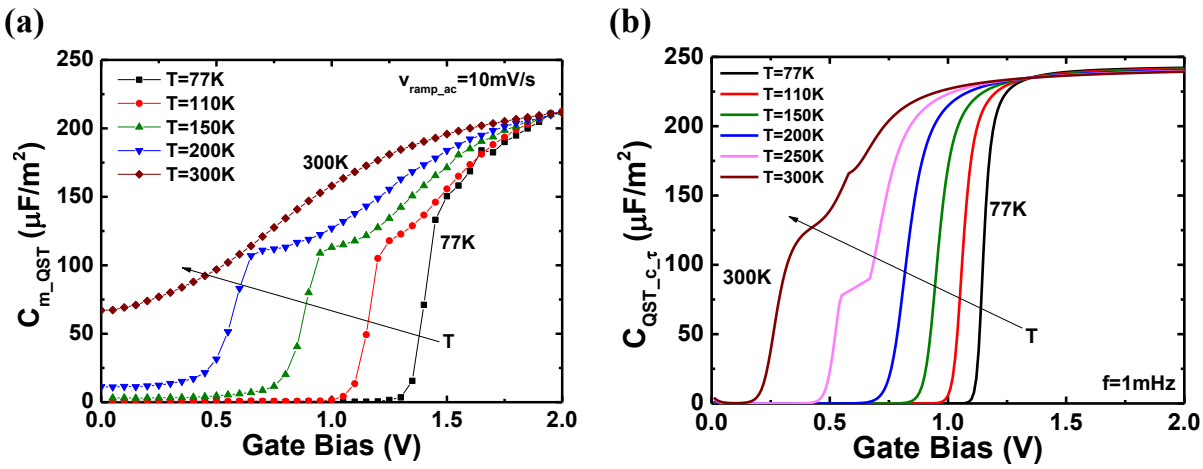

Figure IV-13: (a) C_{m_QST} obtained on the same wafer as in Figure IV-12 as function of V_G. Measurements performed using slow v_{ramp_ac} (*10 mV/s*) and different temperatures. (b) Computed $C_{QST_c_\tau}$ versus gate bias for different temperatures.

IV.5 D_{it} extraction procedure

After the validation of our model for the quasi-static capacitance, here we propose a procedure to D_{it} extraction. Limitations and possible improvements will be also pointed out.

Physical approach

In the previous sections it was proved that the measured quasi-static capacitance behavior is well predicted by Eq. (IV.22) where the defects capacitance contribution was calculated using Eq. (IV.18). In a practical case the traps are continuously distributed in energy in the silicon band gap and the associated capacitance can be written as [56]:

$$C_{it_QST} = q \cdot D_{it} \tag{IV.26}$$

We use C_{it_QST} instead of C_{it_c} in Eq. (IV.22). Equation (IV.22), even though complete from the modeling point of view, is quite complicated to directly use for traps extraction. Two reasonable assumptions can simplify it:

- $\beta \cdot Q_i$ is neglected in Eq. (IV.22). This is acceptable because D_{it} extraction is performed before channel formation, when the density of free carriers in the channel is negligible.
- τ_{Dit} is neglected. The assumption implies that the traps extracted have a time constant much lower than the *a.c.* ramp time t_m.

Consequently, Eq. (IV.22) is rewritten in a simpler way:

$$C_{QST_c_\tau} \approx C_{QST_c} = \frac{C_{OX} \cdot C_{it_QST}}{C_{OX} + C_{it_QST}} = C_{m_QST} \tag{IV.27}$$

Performing one QSCV measurement on SOI structure, the maximum measured capacitance in strong inversion (or accumulation) regime yields C_{OX}. Using Eq. (IV.27) it is possible to compute C_{it_QST} before channel formation, thus to extract D_{it}.

Robustness of the extraction procedure

Figure IV-14a shows the D_{it} profile as a function of V_G obtained using our approach (plain symbols) and the high-low frequency method (empty symbols) [56], [118] in which no assumption concerning $\beta \cdot Q_i$ is performed. The data presented in Figure IV-3 was used. Two measured capacitance curves are required for the high-low *f* technique: one at high frequency where the traps do not have time to respond (*e.g.*, *1 V/s*), and a second one at a much lower *a.c.* scan speed (*e.g.*, *10 mV/s*). Remarkable agreement is found between the two extraction procedures. This result confirms the validity of our approach, which is preferable to the standard high-low frequency because it only requires one QSCV characteristic.

Figure IV-14b shows the extracted interface trap density obtained from Figure IV-10a (plain symbols) for v_{ramp_ac} = *5 mV/s* as a function of gate bias. Slow ramp speed was used to reduce attenuation effects due to frequency impact. U-shape defects distribution is found (similar to Figure IV-1b). A valley appears around *0 V* because the corresponding traps are too slow to be completely detected (τ_{Dit} too long).

In order to confirm the assumption of negligible $\beta \cdot Q_i$ term, the dashed line in Figure IV-14b shows the equivalent free carrier density expressed in $cm^{-2}eV^{-1}$. $\beta \cdot Q_i/q$ was calculated using Lambert equation [99]. Its contribution becomes relevant only close to V_{FB} and V_T, where the extraction procedure may overestimate D_{it}. However, these results confirm the possibility to neglect $\beta \cdot Q_i$ contribution during D_{it} extraction.

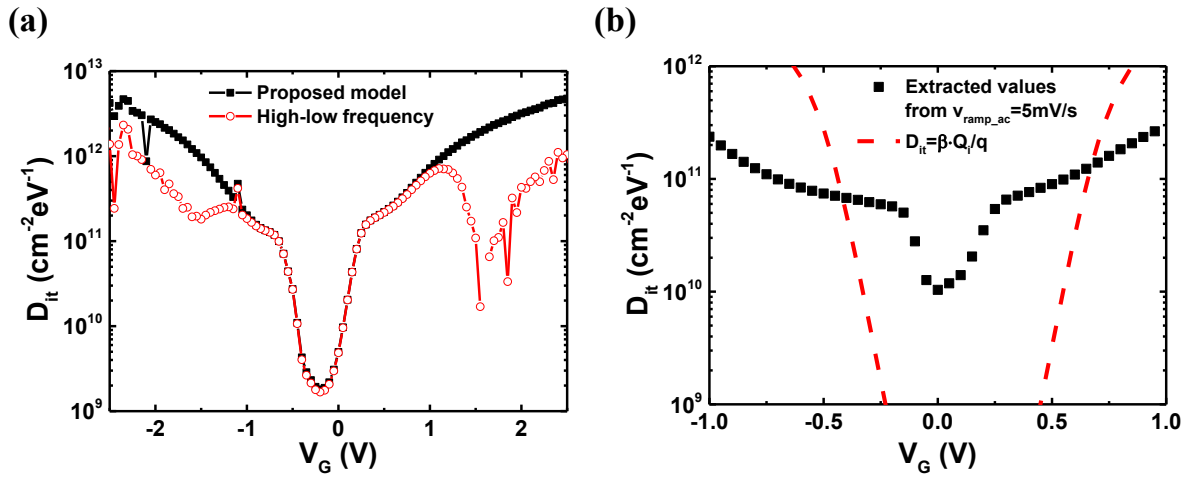

Figure IV-14: (a) Extracted traps profile as a function of gate bias using our procedure (plain symbols) and the high-low frequency method (empty symbols). Data from Figure IV-3. (b) D_{it} versus V_G extracted from slow (v_{ramp_ac} = *5 mV/s*) QSCV measurement discussed in Figure IV-10a using our approach (Eq. (IV.27)) (plain symbols). The dashed line represents the density of free charges induced by V_G expressed in $cm^{-2}eV^{-1}$.

Frequency effects on extracted D_{it} (exponential fit procedure)

In order to analyze the impact of the neglecting τ_{Dit}, Figure IV-15a shows the interface trap density as a function of V_G for different v_{ramp_ac}. The characteristics from Figure IV-10a were used. For a given value of V_G, curve superposition is obtained below a certain frequency at which all the defects respond. Hence, τ_{Dit} effect is really negligible. This condition is fulfilled for high gate bias magnitude. On the contrary, far from V_T and V_{FB} (*e.g.*, $V_G \approx 0$ *V*), the traps are more difficult to detect because their associated τ_{Dit} are too large to be neglected.

One possibility to overcome the underestimation of slow traps magnitude arises from the exponential fit discussed in Figure IV-11a, where the capacitance measured at constant gate bias values $C_{m_QST_Vg}$ where exponentially fitted as a function of *a.c.* ramp time t_m. 5-steps procedure is required:

- Perform quasi-static measurements with different v_{ramp_ac} (see inset in Figure IV-15a);
- Extract the capacitance values at fixed gate bias (arrows in the inset in Figure IV-15a);
- Trace the measured capacitance at constant V_G ($C_{m_QST_Vg}$) as a function of t_m (inset in Figure IV-15b);
- Exponentially fit the results (Eq. (IV.24)) as a function of t_m (dashed line in the inset in Figure IV-15b);

- Use $C_{m_QST_sat}$, which is frequency independent, instead of C_{m_QST} in Eq. (IV.27) to compute D_{it} values.

Figure IV-15b shows the obtained interface trap density versus V_G in case of slow *a.c.* measurement ramp speed (empty symbols) and D_{it} computed using $C_{m_QST_sat}$ (plain symbols) from Figure IV-11a. Note that the curves overlap far from $V_G = 0\ V$. A light difference is present close to $0\ V$, when the measurement v_{ramp_ac} was not slow enough to avoid τ_{Dit} effects, leading to D_{it} underestimation.

In summary, for rapid D_{it} characterization, one measurement performed using slow *a.c.* ramp speed is sufficient for the detection of traps far from the mid-gap (empty symbols in Figure IV-15b). To better detect the whole defect distribution, including also very deep traps, an exponential fit based on different v_{ramp_ac} characteristics is necessary (plain symbols in Figure IV-15b, 5-steps procedure). This procedure can be limited by noise. Furthermore, it can only predict traps that contribute, at least partially, during the scan. In the next sections of this chapter, the D_{it} extrapolated using this exponential fit will be labeled "*projected* D_{it}".

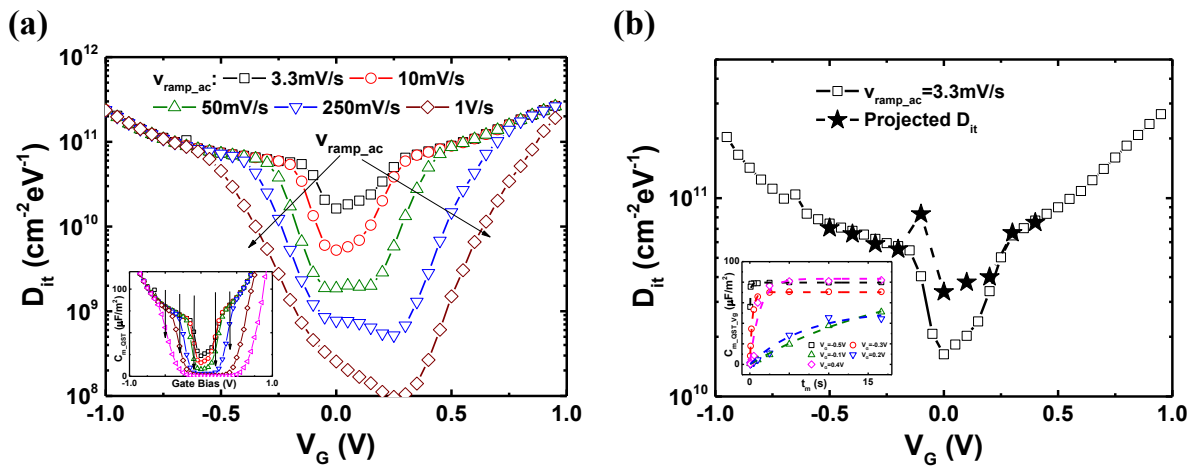

Figure IV-15: (a) D_{it} extracted from Figure IV-10a as a function of V_G for different v_{ramp_ac}. (b) D_{it} profile computed from slow *a.c.* ramp speed (*3.3 mV/s*) (empty symbols) versus gate bias. The plain symbols represent the traps profile obtained using the 5-steps procedure (Figure IV-11a). Figure IV-10a and Figure IV-10b are shown as insets in Figure IV-15a and Figure IV-15b, respectively, to clarify the computation of projected D_{it}.

IV.6 Characterization of non-passivated samples

The previous section focused on the characterization of passivated samples with *4 nm* dry oxide on the top silicon layer. To further investigate the technique capabilities, it is important to characterize non-passivated SOI wafers (different top interface quality with respect to the passivated ones). This will allow evaluating the sensitivity of QSCV and understanding to which interface the technique is more sensitive (BOX-top silicon film or top silicon film-native oxide).

Figure IV-16 shows several $C_{m_QST}(V_G)$ curves measured on non-passivated SOI structure with *88 nm* thick silicon film and *145 nm* thick BOX using the same v_{ramp_ac}. Each characteristic was started from different positive gate bias values. Changing the starting point obviously affects the peak present at $V_G < 0\ V$. Which of these measurements should be used for D_{it} extraction?

A procedure is needed to obtain stable curves that could permit a reliable material investigation. The physical origin behind this phenomenon needs to be understood.

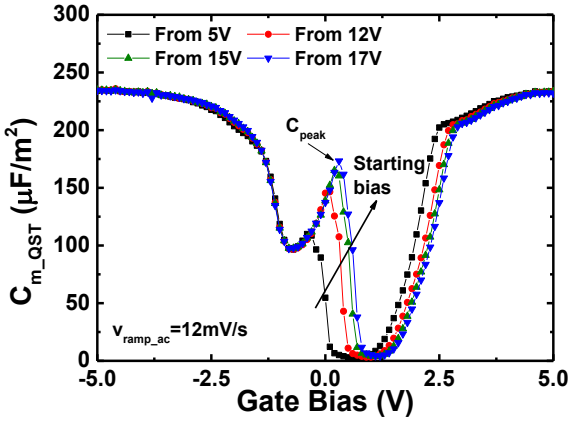

Figure IV-16 C_{m_QST} as a function of V_G for slow *a.c.* scan speed. The characteristics were started from different positive gate bias values. The SOI structure had *88 nm* top silicon film thickness and *145 nm* BOX thickness. The top surface was non-passivated. C_{peak} identifies the measured capacitance peak obtained before channel formation.

IV.6.1 Traps charging procedure

Thick silicon film

Figure IV-16 shows that the starting point mostly affects C_{peak} while the right part of the characteristic slightly shifts. In this section we will focus our attention on this measured peak labeled C_{peak}.

The dependency with the initial gate bias let us think that a possible stress during the characterization induces new defects in the oxide. To deeper investigate this phenomenon, a standard stress procedure was performed and the capacitance versus time evolution was monitored as in MOSFETs [121], [122]. The investigated sample had *88 nm* thick silicon film and *145 nm* thick BOX. One probe was placed on the silicon surface and connected to ground. V_G stress (labeled "*charging bias*" V_{G_charge}) was applied to the SOI substrate for a certain time ("*charging time*" t_s), and afterwards a QSCV measurement using slow *a.c.* scan speed was immediately performed.

Figure IV-17 shows the results for passivated (a) and non-passivated (b) top surface. V_{G_charge} had no impact on the characteristics of passivated samples showing that no new defects were created. In case of non-passivated top surface, however, the longer the applied *charging bias*, the higher the C_{peak}. t_s around *3000-4000 s* leads to the peak height saturation.

The procedure is obviously not affecting the film-BOX interface since the passivated samples show no variations. It is only active for the non-passivated surfaces. However, it is still not clear, if new defects are generated or only charged.

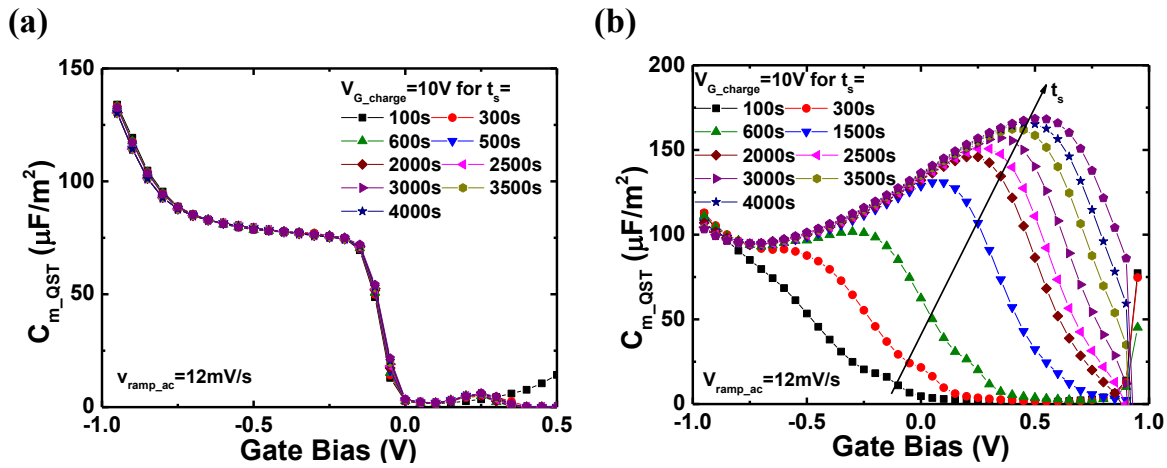

Figure IV-17: C_{m_QST} versus gate bias for slow *a.c.* scan speed. V_{G_charge} = *10 V* was applied for different t_s on SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness. Passivated (a) and non-passivated (b) top surface.

One possibility to verify if the procedure is degrading the oxide (stress) or not (charging), consists of the characterization of the sample before and after applying the *charging bias* (Figure IV-18). The SOI structure has been initially characterized using $v_{ramp_ac} = 10\ mV/s$ (line). Then, $V_{G_charge} = 10\ V$ was set for *3000 s* and the quasi-static capacitance was measured again (plain symbols). C_{peak} increases, while around V_{FB} and V_T the curves superpose. A stress procedure generates new charges in the oxide which should result in a clear shift of V_T and V_{FB} [123]. Our result suggests the presence of charging effects rather than permanent damage (stress).

Additionally, a third measurement was performed on the same structure *6* hours after the end of the second measurement (empty symbols). The characteristic superposes with the initial one. This confirms that the procedure does not induce new defects but only charges the already present D_{it}. Supported by the results of Figure IV-17, it is reasonable to assume that the defects filled during the procedure are located on top of the silicon surface (confirmed also in Sec. IV.8).

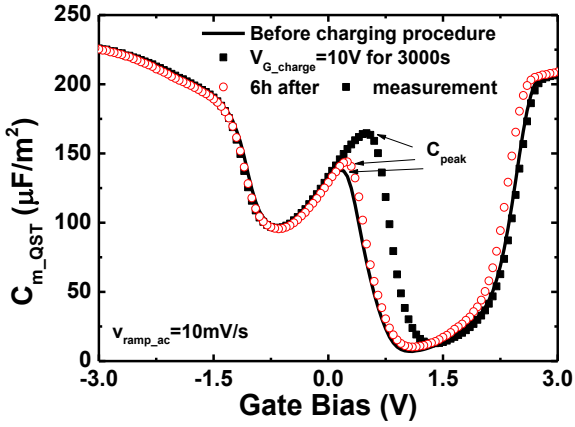

Figure IV-18: C_{m_QST} as a function of gate bias before (line) and after (plain symbols) applying $V_{G_charge} = 10\ V$ for *3000 s*. The characterization performed *6* hours after the end of the second measurement is shown (empty symbols). The SOI structure had *88 nm* thick Si film, *145 nm* thick BOX and non-passivated top surface.

If the applied *charging bias* only fills defects that are already present on the SOI wafer, the measured capacitance should be independent of the applied voltage. On the contrary, if V_{G_charge} is inducing new traps, the use of larger values should lead to stronger C_{peak}.

Three different V_{G_charge} were applied for different t_s on a non-passivated SOI structure: *10 V*, *20 V*, and *30 V*. A quasi-static capacitance measurement was performed after each bias condition. C_{peak} and the corresponding bias position (V_{G_peak}) were identified for each characteristic. Figure IV-19a shows the obtained peak magnitude and Figure IV-19b the corresponding V_{G_preak} versus t_s. The initial points are not the same, because after changing V_{G_charge} magnitude, the SOI structure did not have enough time to completely recover its initial state. For long t_s, however, the three curves overlap regardless of the applied voltage. This is a supplementary confirmation of traps charging effects and not actual damage procedure.

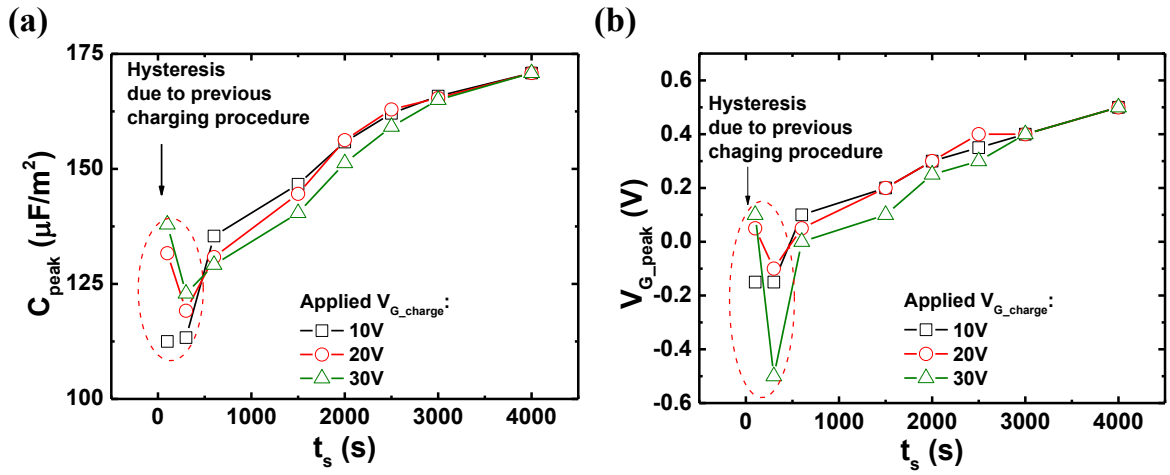

Figure IV-19: Measured C_{peak} (a) and corresponding bias value V_{G_peak} (b) as a function of t_s on the same SOI structure as in Figure IV-17b. Three different *charging biases* V_{G_charge} were applied for different t_s: *10 V*, *20 V* and *30 V*.

Ultra-thin silicon film

In order to test the validity of the charging procedure on ultra-thin films, SOI structure with *12 nm* top silicon film thickness, *145 nm* BOX thickness and non-passivated surface was investigated. Figure IV-20 shows the measured quasi-static capacitance using slow *a.c.* scan speed for different t_s. The *charging bias* was *10 V*. In case of $V_G > 0$ *V*, the risen "*shoulder*" is almost constant. On the contrary, C_{peak} increases proportionally to the charging time, as for thick silicon film.

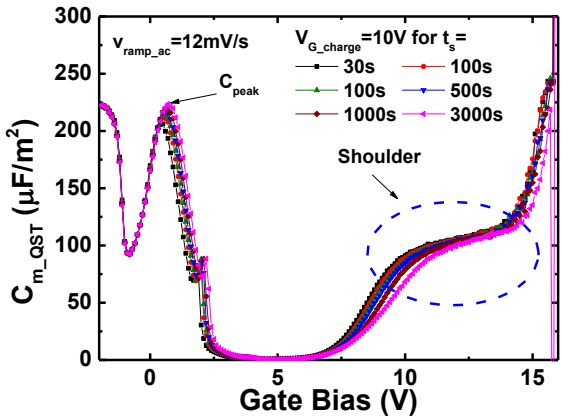

Figure IV-20: C_{m_QST} versus gate bias for different t_s and V_{G_charge} = *10 V*. The SOI structure had *12 nm* thick Si film and *145 nm* thick BOX. Non-passivated top surface.

Similar analysis as for thick SOI structure was performed in case of ultra-thin Si layer. Different *charging biases* were consecutively applied on the same die for different t_s: *5 V*, *10 V* and *15 V*. C_{m_QST} was measured and C_{peak} and V_{G_peak} were identified for each characteristic. Figure IV-21a shows the obtained peak magnitude as a function of t_s. A larger *charging bias* induces higher peak. In case of $V_{G_charge} = 15\ V$, the measured value saturates at C_{OX} ($238\ \mu F/m^2$). Figure IV-21b presents V_{G_peak} as a function of t_s. The bias value associated to C_{peak} saturates for $V_{G_charge} = 5\ V$ and *10 V* but no clear overlap is obtained. On the contrary, the characteristic measured after *15 V charging bias* constantly increases. This is typical for stress procedure during which new defects are created [111].

In conclusion, in case of ultra-thin film, separating the charging and defects generation effects is challenging. However, this is not a limitation for traps investigation because in case of $t_{Si} = 12\ nm$ the coupling with the conduction channel is stronger. Thus, the defects become more accessible even without charging them (see Sec. IV.8).

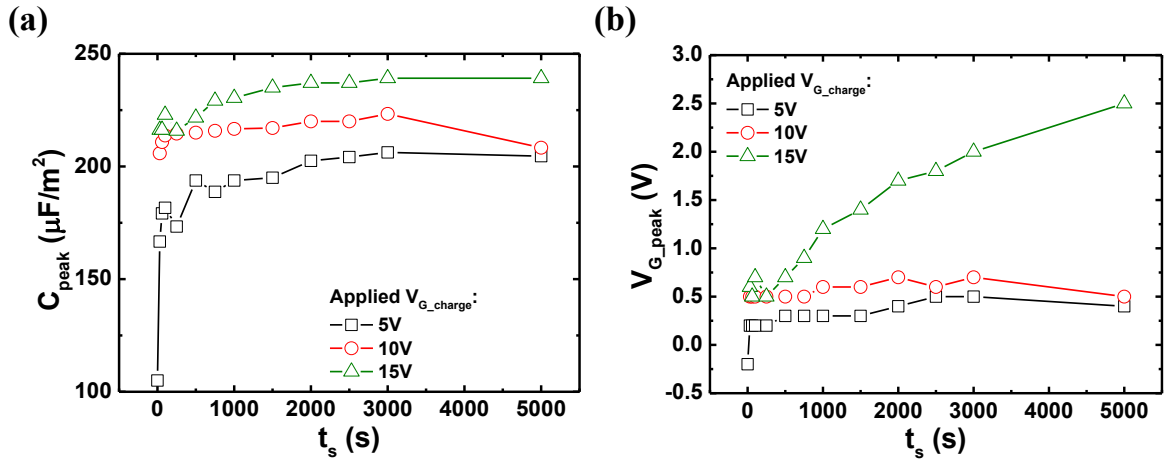

Figure IV-21: C_{peak} (a) and V_{G_peak} (b) as a function of t_s. Three different *charging biases* were applied: *5 V*, *10 V* and *15 V*. Same SOI structure as in Figure IV-20.

IV.6.2 Example of D_{it} extraction for non-passivated samples

The interface traps profile for non-passivated samples can be extracted following the procedure proposed in Sec. IV.5. However, it is important to evaluate the effects of the *charging bias* on the obtained D_{it}.

Figure IV-22 shows the measured C_{m_QST} as a function of gate bias before (a) and after (b) filling the traps on non-passivated SOI structure. The capacitances were measured using different v_{ramp_ac}. The use of lower *a.c.* scan speed reveals more defects, as for passivated samples (see Figure IV-10a). After the charging procedure ($V_{G_charge} = 10\ V$ for $3000\ s$) the impact of v_{ramp_ac} is smaller for $V_G < 0\ V$, as shown in Figure IV-22b.

In the next two sections the traps profile will be extracted in both configurations: before and after charging the defects. The exponential fit procedure describe in Sec. IV.5 will be used to extrapolate the D_{it} profile (projected D_{it}) and compute the corresponding τ_{Dit}.

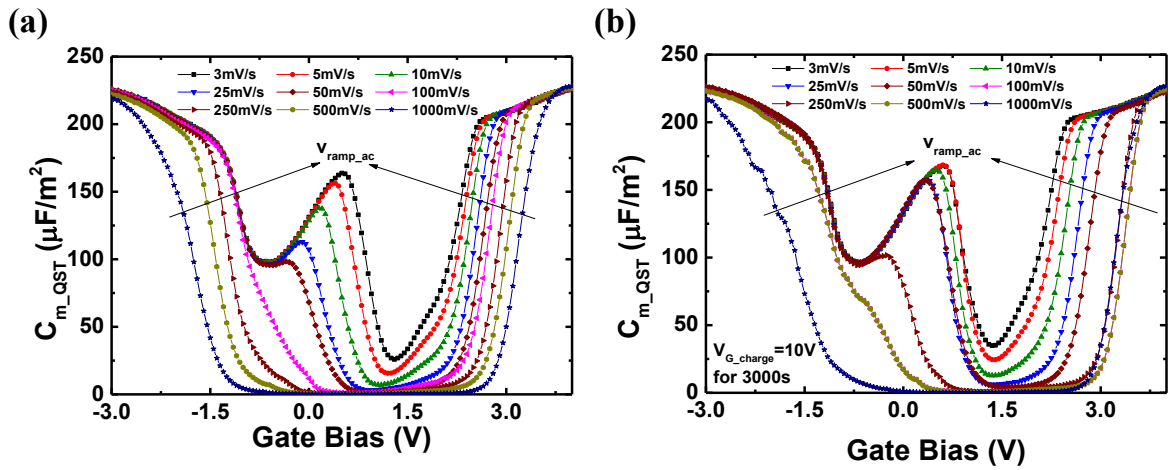

Figure IV-22: C_{m_QST} versus gate bias before (a) and after (b) charging procedure obtained using different v_{ramp_ac}. Non-passivated SOI structure with *88 nm* thick silicon film and *145 nm* thick BOX.

D_{it} profile extracted before charging the defects

Figure IV-23a shows the measured capacitance at constant gate bias $C_{m_QST_Vg}$ as a function of *a.c.* ramp time t_m in case of positive V_G. The data discussed in Figure IV-22a are used (no charging procedure was performed). An exponential trend is found for large gate bias. For $V_G = 1\ V$ and $V_G = 1.5\ V$ no exponential fit is possible. The defects are too slow to be detected. Figure IV-23b presents the extracted D_{it} as a function of V_G. The traps profile obtained from $v_{ramp_ac} = 3\ mV/s$ (square empty symbols) is compared with the projected defects density (plain stars) calculated from Figure IV-23a. General agreement is present between the two curves. For V_G around $0.5\ V - 1\ V$ no D_{it} can be extrapolated. Furthermore, τ_{Dit} is traced as a function of gate bias (empty circles in Figure IV-23b). The general trend is similar to the one measured in case of passivated sample (see Figure IV-11b) but the failure of the fit leaves the analysis incomplete around $0.5\ V - 1\ V$.

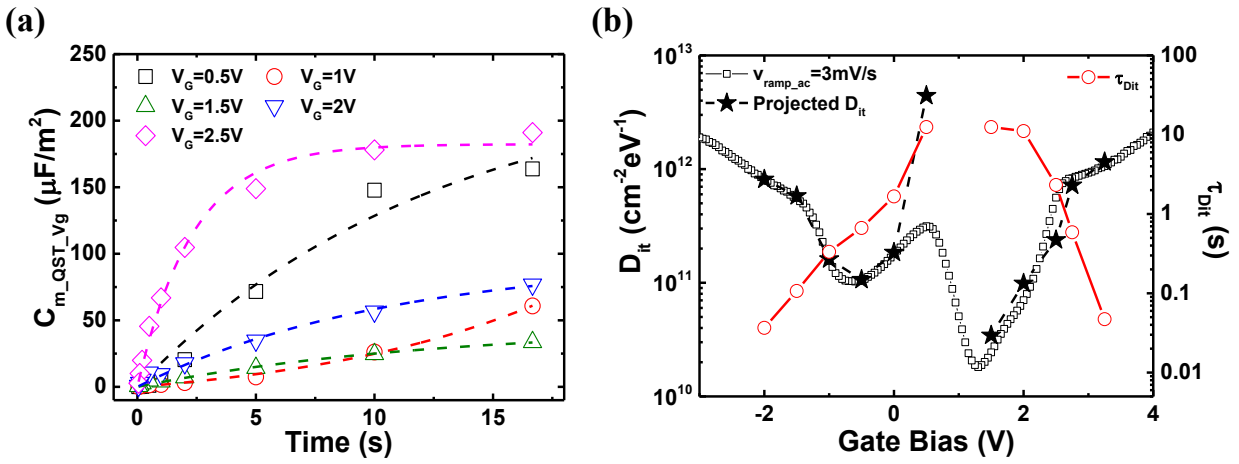

Figure IV-23: (a) $C_{m_QST_Vg}$ versus t_m for different V_G obtained from Figure IV-22a in case of positive gate bias. (b) D_{it} profile extracted from slow *a.c.* ramp speed (empty square symbols) versus gate bias. The exponential fit performed in Figure IV-23a (see Eq. (IV.24)) leads to the calculation of projected D_{it} profile independent from the used *a.c.* scan detection (plain star symbols) (see Sec. IV.5) and the corresponding τ_{Dit} (empty circles symbols).

D_{it} obtained after charging the defects

Figure IV-24a presents the obtained D_{it} profile versus V_G computed on measured QSCV characteristics (v_{ramp_ac} = *3 mV/s*) after charging procedure (empty symbols). The defects profile obtained before filling the traps are also reported for comparison (plain symbols). The curves overlap. No clear effects due to filled traps is evidenced.

Figure IV-24b shows the projected D_{it} versus V_G obtained from characteristics measured before (plain symbols) and after (empty symbols) charging the traps. The extraction was performed using the exponential fit discussed in Sec. IV.5. The defects profile obtained after applying V_{G_charge} = *10 V* for *3000 s* is larger than the one computed before filling the defects. The charging procedure made accessible slow traps which could not be predicted before.

The analysis is supported by the computed τ_{Dit} versus gate bias (inset in Figure IV-24a). After filling the traps, τ_{Dit} decrease and the analysis can be performed on all the V_G range (no exponential fit failure). The charging procedure makes D_{it} prediction easier.

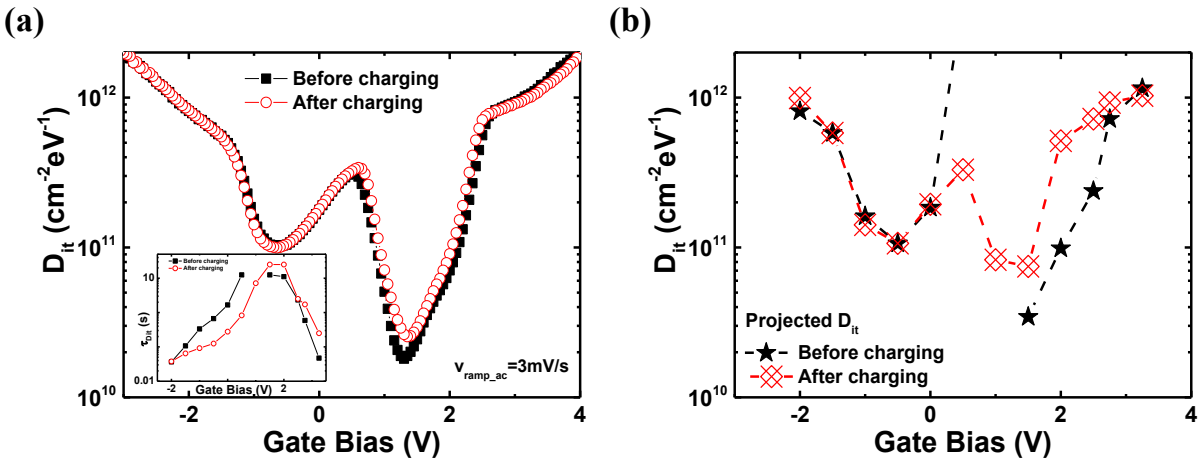

Figure IV-24: D_{it} profile versus gate bias obtained after charging procedure (empty symbols) with v_{ramp_ac} = *3 mV/s* (a) and projected D_{it} (b) from Figure IV-22b using the exponential fit (Eq. (IV.24)) explained in Sec. IV.5. The corresponding characteristics computed before charging the defects are added (plain symbols). The same data as in Figure IV-23b were used. The associated τ_{Dit} versus gate bias is reported in the inset in Figure IV-24a before (plain symbols) and after (empty symbols) having applied *10 V* for *3000 s*.

Comparison of D_{it} extracted from passivated and non-passivated samples

The charging procedure gives us useful information about the characterization setup required for non-passivated samples. The next natural step is the comparison of the obtained traps profile in case of different interface qualities. Figure IV-25 presents the extracted D_{it} versus gate bias for passivated (empty symbols) and non-passivated (plain symbols) SOI structures. Measurements were performed using v_{ramp_ac} = *3 mV/s* and no charging procedure was applied. Despite the large difference in traps density, a detailed comparison is not possible because the different interface quality induces V_T and V_{FB} shifts. For comparative analysis, the characteristics must be traced versus surface potential (or energy). This aspect will be investigated in the next section.

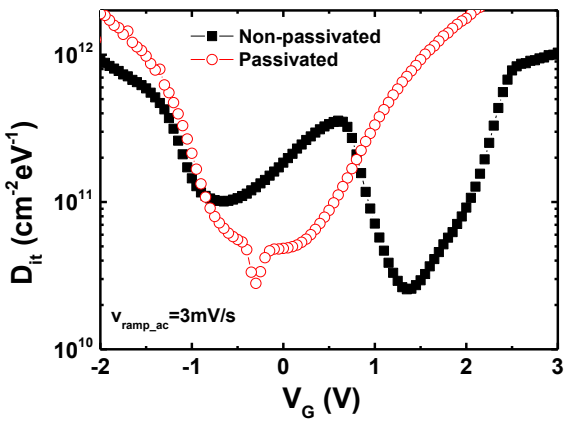

Figure IV-25: Extracted D_{it} versus gate bias in case of passivated (empty symbols) and non-passivated (plain symbols) silicon layer. The SOI structure had *88 nm* top silicon film and *145 nm* BOX. QSCV measurements performed using v_{ramp_ac} = *3 mV/s* and without charging procedure.

IV.7 Surface potential computation

MOS-like surface potential computation and its limitation for Ψ-MOSFET

Equation (IV.1) is used for Ψ_S calculation in case of standard MOS capacitor [124]–[126]. Thus, it should be also suitable for the pseudo-MOSFET configuration. Three steps are required to determine the surface potential:

1 Perform one capacitance measurement C_{m_QST} at slow *a.c.* ramp speed;

2 Calculate $\delta\Psi_S/\delta V_G$ term:

$$\frac{\delta\Psi_S}{\delta V_G} = 1 - \frac{C_{m_QST}}{C_{OX}} \tag{IV.28}$$

3 Integrate $\delta\Psi_S/\delta V_G$ between V_{FB} and V_G, where $V_G \leq V_T$.

Figure IV-26a shows $1\text{-}C_{m_QST}/C_{OX}$ (step *2*) measured in case of different v_{ramp_ac}. The curves have a general bell-shape. The presence of a second peak rising up in some characteristics (see for example $v_{ramp_ac} = 3\ mV/s$ and $10\ mV/s$) evidences the presence of deep traps that are not completely detected.

Integrating $1\text{-}C_{m_QST}/C_{OX}$ (step *3*, Eq. (IV.1)), the surface potential as a function of V_G can be computed (Figure IV-26b). Ψ_S for silicon should be around $1.1\ V$ [5]. The values obtained from experimental results are higher than expected. In case of fast *a.c.* ramp speed the situation becomes even worse.

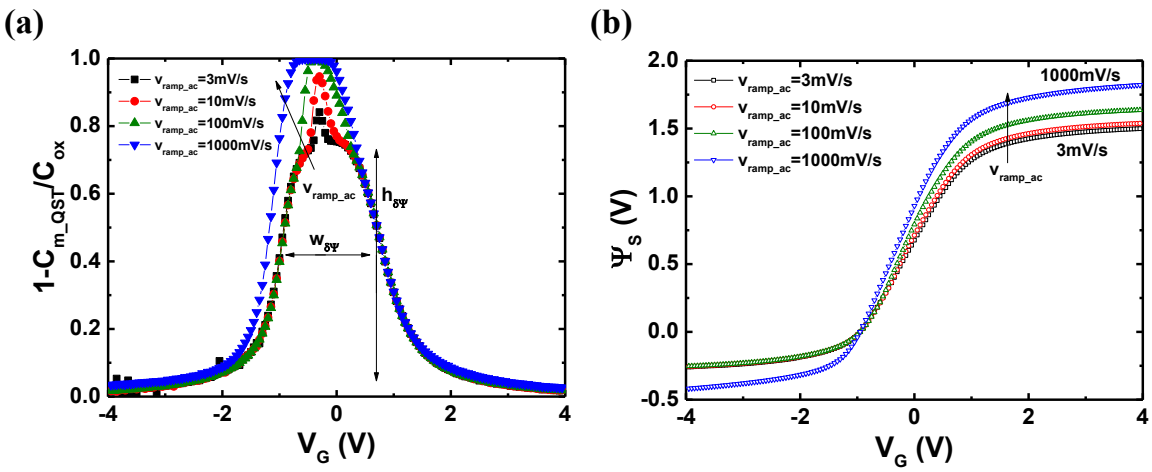

Figure IV-26: (a) $1\text{-}C_{m_QST}/C_{OX}$ versus gate bias obtained for different *a.c.* ramp speed (step *2*). (b) The corresponding surface potential computed using Eq. (IV.1) is traced as function of V_G. $w_{\delta\Psi}$ and $h_{\delta\Psi}$ identify the peak width and height, respectively.

To identify the sources of this problem, we have numerically calculated the expected surface potential including a continuum distribution of D_{it}. Differential equations solver FlexPDE® was used. The structure is shown in Figure IV-27a. The defects were added at the interface between the top silicon film and the BOX. Poisson equation leads to the computation of the potential distribution over the whole structure. Thus, the variation of the surface potential with respect to the gate bias can be determined ($\delta\Psi_S/\delta V_G$).

Figure IV-27b shows the calculated $\delta\Psi_S/\delta V_G$ as a function of V_G for different D_{it} density. Higher defect concentrations lead to smaller and wider peak ($w_{\delta\Psi}$ increases while $h_{\delta\Psi}$ decreases).

Comparing calculated and experimental results, two problems rise up:

- In case of experimental results (see Figure IV-26a), slower *a.c.* ramp leads to smaller $h_{\delta\Psi}$ but the measured $w_{\delta\Psi}$ is almost constant;
- Including in the simulations $w_{\delta\Psi}$ measured from experimental results (es. from Figure IV-26a), the obtained peak height is much smaller than the measured $h_{\delta\Psi}$.

These problems may explain why Ψ_S calculated using Eq. (IV.1) is overestimated. One of the main assumptions of Eq. (IV.1) is that the semiconductor is at equilibrium condition and all the charges (*i.e.*, free carriers and defects) respond during the measurements. This is obviously not the case in all the experimental v_{ramp_ac}.

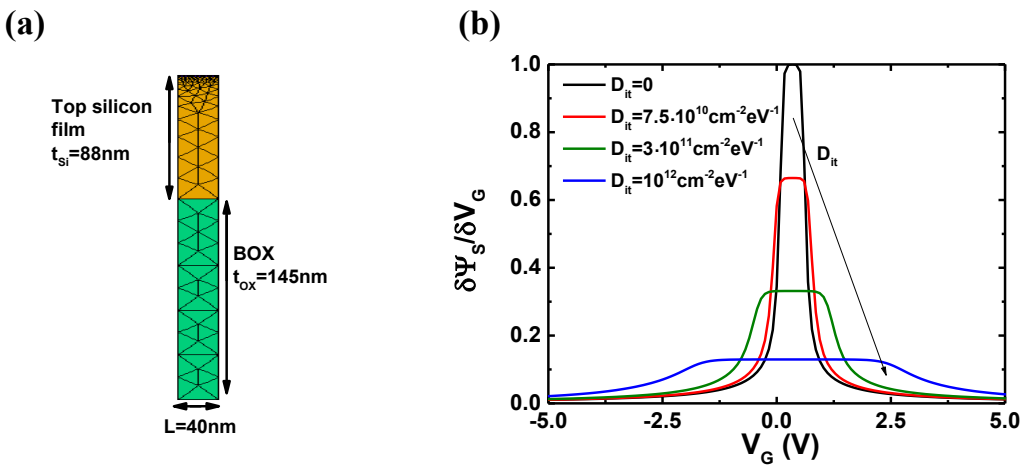

Figure IV-27: (a) Mesh of the vertical SOI structure used in FlexPDE®. (b) Computed $\delta\Psi_S/\delta V_G$ versus gate bias in case of different D_{it} placed at the interface between the top silicon film and the BOX.

Computation of surface potential

Since it is not possible to obtain Ψ_S directly from experimental results, a mix between measurements and calculation was proposed to overcome the limitations. It is based on the following steps:

1 QSCV measurement is performed using the slowest v_{ramp_ac} (*3 mV/s* in our case). Figure IV-28a shows C_{m_QST} versus gate bias (empty symbols) for the same measured structure as in Figure IV-26a. From this curve we calculated ($1-C_{m_QST}/C_{OX}$) (see Figure IV-26a).

2 Next, $w_{\delta\Psi}$ is required and we need a reproducible procedure to measure it. This is possible computing the derivative of $1-C_{m_QST}/C_{OX}$ with respect to the gate bias. The distance between the maximum and the minimum values leads to unambiguous $w_{\delta\Psi}$ (see $w_{\delta\Psi}$ obtained in Figure IV-28a).

3 For given top silicon film and BOX thicknesses, the width of $\delta\Psi_S/\delta V_G$ is calculated using FlexPDE® in case of different D_{it} magnitude. Figure IV-28b shows an example of $w_{\delta\Psi}$ versus traps density for SOI with *88 nm* top silicon film thickness and *145 nm* BOX thickness (symbols). The trend is clearly linear and a good fit is given by:

$$w_{\delta\Psi} = 4.15 \cdot 10^{-12} \cdot D_{it} + 0.6 \quad \text{(IV.29)}$$

The intercept with *y*-axis (*0.6 V* in this case) is determined by the curve width obtained without any traps contribution.

4 Using Eq. (IV.29) and $w_{\delta\Psi}$ obtained from step *2*, an equivalent D_{it} magnitude is then calculated:

$$D_{it_eq} = \frac{w_{\delta\Psi} - 0.6}{4.15 \cdot 10^{-12}} \quad \text{(IV.30)}$$

This procedure supposes that all the traps have the same magnitude, they are continuously distributed in energy in the silicon band gap and they respond to the QSCV signal.

5 Performing one simulation with FlexPDE® where D_{it_eq} from step *4* is placed at the BOX-top silicon film interface, the surface potential is finally obtained.

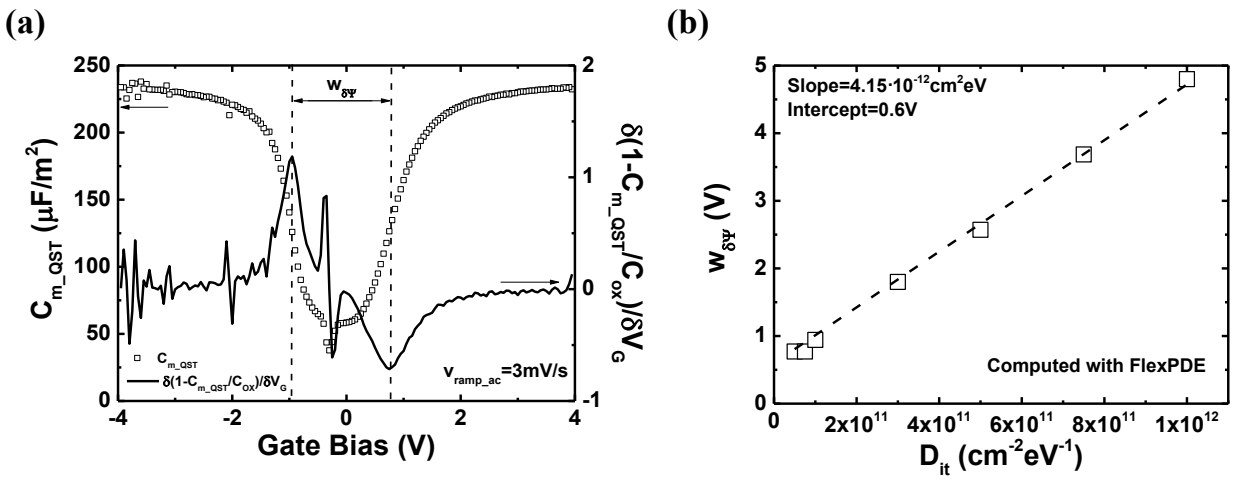

Figure IV-28: (a) Measured C_{m_QST} and corresponding derivative of $1\text{-}C_{m_QST}/C_{OX}$ with respect to the gate bias traced as a function of V_G. The associated $1\text{-}C_{m_QST}/C_{OX}$ as a function of V_G is shown in Figure IV-26a. The inter-pads distance yields $w_{\delta\Psi}$. (b) $w_{\delta\Psi}$ (symbols) and corresponding fit (line) versus D_{it} computed using FlexPDE® for the same SOI structure as in Figure IV-28a.

Figure IV-29 shows Ψ_S versus gate bias computed from Eq. (IV.1) (plain symbols) and using our procedure (line). The data in Figure IV-28a was used. More realistic potential values are obtained with the proposed approach. Ψ_S saturates for large V_G (strong inversion and accumulation regime), while it is directly proportional to the gate bias in the linear region.

Note that the surface potential is directly proportional to the traps energy level in the silicon band gap (*E*). The *0* of the energy will be placed at the maximum of the valence band (E_V). Hence, the energy in *eV* can replace V_G, thus Ψ_S, on the D_{it} profile curves.

In the next sections, all the surface potential values, thus the energy $E\text{-}E_V$, were computed using this procedure. This approach will give the defects location in the silicon band gap. The extracted D_{it} magnitude is not affected by Ψ_S and $E\text{-}E_V$ calculation. Only an error in their effective energy level could eventually result from Ψ_S miscalculation.

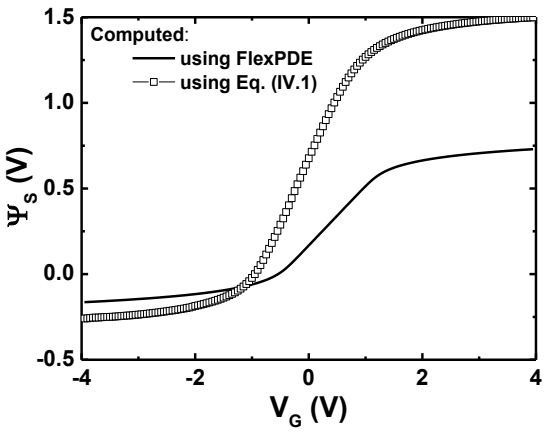

Figure IV-29: Ψ_S versus gate bias computed from experimental results in Figure IV-28a using Eq. (IV.1) (empty symbols) and using our procedure (line).

IV.8 Comparison of D_{it} profiles for different samples

In this last part of the chapter, we focus on the characterization of SOI structures with different interface qualities and geometries. In order to perform suitable comparisons, all the extractions were performed using $v_{ramp_ac} = 3\ mV/s$. No charging procedure is necessary at such low *a.c.* ramp speed and tested ultra-thin t_{Si}. Ψ_S was calculated using our approach (mix of experimental and calculated results) and the D_{it} profile will be traced versus energy.

Thick BOX

Figure IV-30 shows the extracted D_{it} versus energy in case of *88 nm* (empty symbols) and *12 nm* (plain symbols) thick silicon film. The samples have *145 nm* BOX thickness. Passivated (a) and non-passivated (b) SOI were tested. To simplify the comparison, the same data are replotted in Figure IV-30c and Figure IV-30d for the same SOI film thickness but with different top surface quality.

D_{it} for passivated samples (Figure IV-30a) present the typical U-shape behavior [125]. The two traps magnitudes are similar despite the variation of t_{Si} thickness, underlining that the technique is actually mostly sensitive to the silicon film-BOX interface. However, the detection is not complete, since some deep defects cannot be measured (valleys in the curves of Figure IV-30a)

Higher density of traps was measured for the non-passivated samples (Figure IV-30b). In the lower part of the band gap the measured D_{it} shows a peak absent in case of passivated surface. This peak is sharper for ultra-thin silicon film (empty symbols in Figure IV-30b), probably due to the stronger coupling between the top surface and the conduction channel. The shape is in agreement with P_b centers studied in the literature for oxidized silicon with too low annealing temperature (see Figure IV-31a). Also in that case very large D_{it} magnitude ($> 10^{12} cm^{-2} eV^{-1}$) was measured [125], [127]. Furthermore, the energy position of the obtained peaks suggests the presence of acceptor-type defects (+/0) [31].

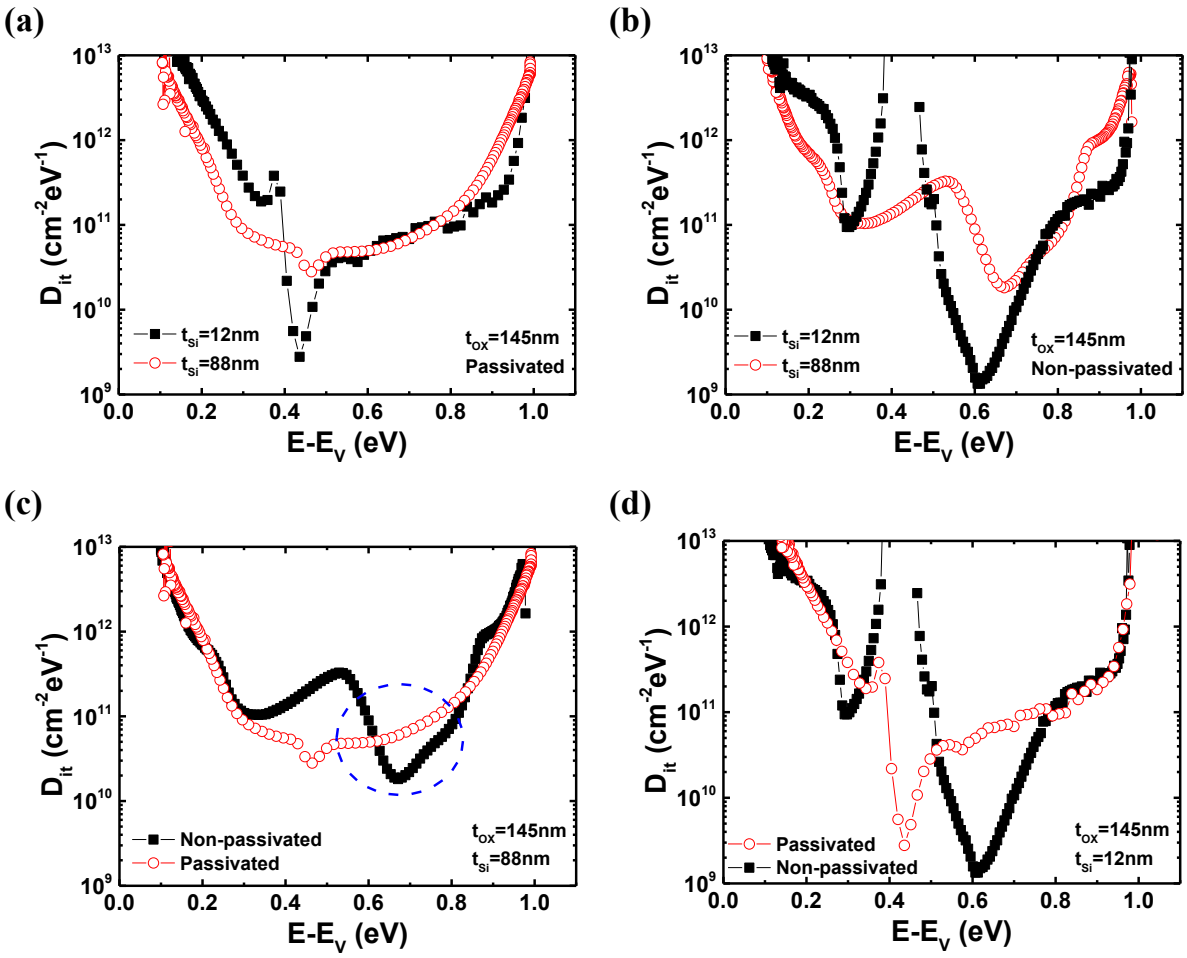

Figure IV-30: D_{it} computed versus E-E_V in case of *88 nm* (empty symbols) and *12 nm* (plain symbols) top silicon film thickness. The BOX thickness was *145 nm*. Passivated (a) and non-passivated (b) top surface, (c) thick Si film and (d) thin silicon layer.

Comparing the D_{it} density obtained around mid-gap in Figure IV-30c and Figure IV-30d (E-$E_V \approx 0.6V$), it seems that the non-passivated surface has lower defects density than the passivated one (es. dashed line in Figure IV-30c). To investigate the reason behind this measurement artefact, Figure IV-31b shows the calculated interface time constants versus energy in case of passivated (empty symbols) and non-passivated (plain symbols) SOI structure (t_{Si} = *88 nm*). The non-passivated curves have much higher τ_{Dit}. Thus, the traps are more difficult to detect. As a result, almost full D_{it} response is obtained on passivated wafers while it is only partial in case of non-passivated ones, explaining the defects underestimation.

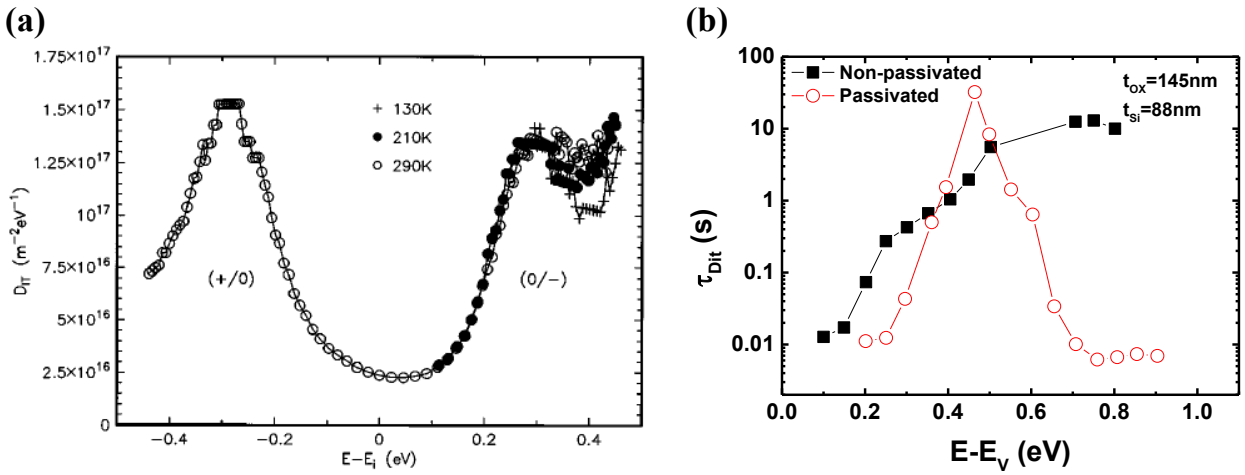

Figure IV-31 (a) Example of D_{it} behavior due to P_b centers obtained on MOS capacitor using QSCV as function of energy, which is referred to the intrinsic level E_i [124]. (b) τ_{Dit} versus E-E_V for passivated (empty symbols) and non-passivated (plain symbols) SOI structure. Extraction performed in the data discussed in Figure IV-30c.

UTBB structure

QSCV technique does not require high probe pressure to achieve good characterization (Sec. IV.3.2). This makes the procedure suitable for the characterization of UTBB structures.

Figure IV-32 shows the extracted D_{it} level versus energy in case of passivated (empty symbols) and non-passivated (plain symbols) silicon surface. SOI structures with *25 nm* thick BOX were used. The top silicon film had (100) (a) and (110) (b) crystal orientation and *12 nm* thickness.

The passivated wafers (empty symbols) show again the U-shaped behavior. A valley before mid-gap is obtained, resulting from the difficulty to characterize slow defects located in this region.

The wafers with non-passivated top surface (plain symbols), for both crystal orientations, evidence P_b center peaks in the lower part of the energy band associated to poor top SiO_2 quality (native oxide).

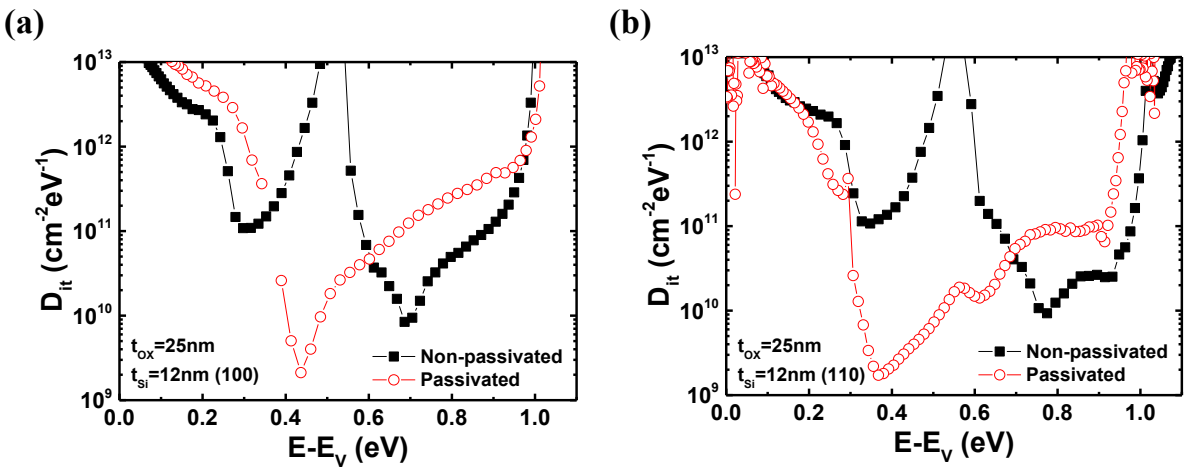

Figure IV-32: D_{it} versus E-E_V in case of passivated (empty symbols) and non-passivated (plain symbols) top silicon surface. The top silicon film had (100) (a) and (110) (b) crystal orientation and it was *12 nm* thick. *25 nm* BOX.

Impact of BOX thickness

We compare wafers fabricated at the same period and with similar processes but different BOX thickness. Figure IV-33 shows the results for non-passivated (a) and passivated (b) top silicon film. The structures had the same t_{Si} = *12 nm*. The BOX was *145 nm* (empty symbols) and *25 nm* (plain symbols) thick.

Agreement on traps distribution is found in case of non-passivated samples. A large peak at similar energies appears. For passivated top silicon layer, the measured D_{it} distributions superpose. This infers that the decreasing of the BOX thickness has hardly affected the density of deep traps located at the interface between the buried oxide and the top silicon film interface.

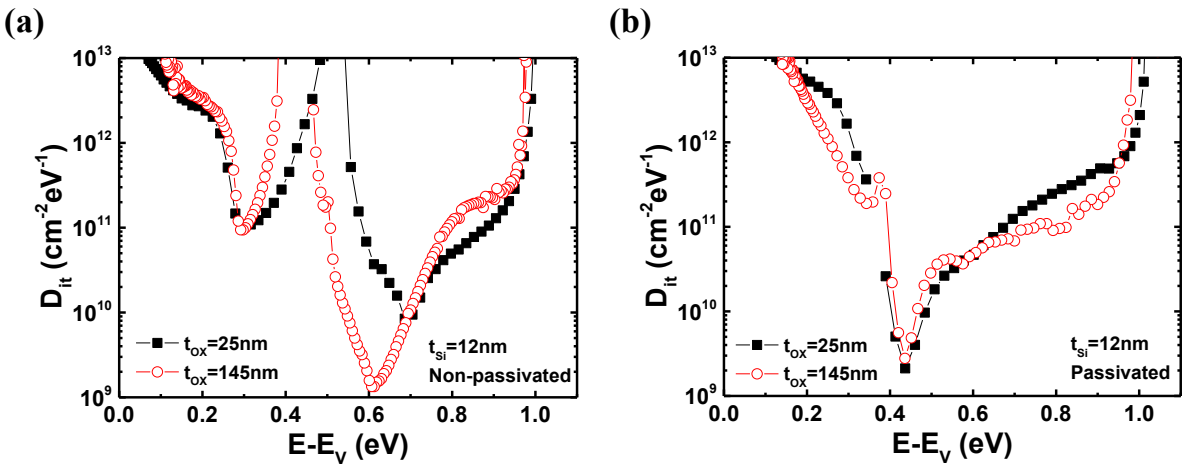

Figure IV-33: D_{it} extracted versus energy for non-passivated (a) and passivated (b) SOI surface. The structures had *12 nm* top silicon film. The buried oxide was *25 nm* (plain symbols) and *145 nm* (empty symbols) thick.

IV.9 Conclusions and perspectives

In this chapter, quasi-static capacitance measurements were performed for the first time in pseudo-MOSFET configuration.

We showed that the QSCV measurements are like an "*extension*" of the LCR meter (split-CV) case to lower frequencies (even though the measurement principles are not the same). The back side contact of Ψ-MOSFET is very important for fast *a.c.* ramp speeds, similar to the split-CV. The probes effect, however, is not very strong implying that the access resistance is only a minor parameter. Consequently, QSCV on ultra-thin silicon films using very low probe pressure is feasible while the same pressure for I_D-V_G does not give appropriate results because too large access resistance.

A physical model capable to explain the measured characteristics, including frequency and temperature effects, was proposed and validated.

One limitation of QSCV technique is that it can only detect traps that are already filled or that can be charged during the scan. If the defects are at too deep energy levels in the silicon band gap and if the measurement is not slow enough, some defects cannot be detected. To overcome the problem, however, it is possible to fill the traps before the detection (charging procedure).

A D_{it} extraction procedure was proposed. The comparison between different SOI structures and interface properties evidenced that in passivated samples we characterize mostly the top silicon film-BOX interface. We proved that for non-passivated surface, larger densities of defects are measured. A sharp D_{it} peak associated to P_b center was evidenced. In all the studied cases, D_{it} profile was mostly independent of t_{Si} and t_{OX}.

QSCV stands as a promising technique for the monitoring of interface quality performed with Ψ-MOSFET. Future developments could be:

- The effective mobility can be also calculated using quasi-static analysis. The measurement of inversion (or accumulation) charge density can be computed with the same approach presented in the split-CV chapter (Sec. III.1.2). The obtained effective mobility will coincide with the one measured using LCR meter. Thus, performing one QSCV characteristic, interface traps density can be studied. Measuring also the drain current on the same device will lead to μ_{eff}.
- The role of substrate capacitance has to be investigated and in case of strong impact on the characteristics, it must be taken into account in the equivalent electric circuit.
- Improvement of Ψ_S extraction, if possible only based on experiments.
- Further investigation of UTBB structures and the impact of charging procedure in case of non-passivated top silicon film.
- Application to new materials as III-V. In case of QSCV the quality of the top contact is much less relevant than for current measurements. Thus, QSCV could become a suitable technique to investigate the interface quality, even for alternative film materials that are normally difficult to contact.

Chapter V:

Low-frequency noise in Ψ-MOSFET

In this thesis several methods for electrical characterization of interface traps have been discussed. Their capability to access D_{it} and their limits have been constantly pointed out. Another technique used in microelectronics to investigate interface quality is the low-frequency noise (LFN). It has already been applied to Ψ-MOSFET configuration but the D_{it} values extracted were too high to be realistic. In this chapter, after a fast review of LFN theory, the impact of experimental conditions will be evaluated. A physical model will be derived and it will be used to explain the measured trends. The limitations of LFN in Ψ-MOSFET configuration will be pointed out and some possibilities for improvement will be presented.

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V.1 Introduction to low-frequency noise

The subthreshold swing is a powerful technique for the characterization of interface traps density [6]. However, the decreasing of the top silicon film thickness t_{Si} and the subsequent increase of the associated capacitance may mask the defects signature, making interface quality monitoring problematic. Furthermore, the defects that respond during static characterization are identified as fast traps (D_{it}) while slow traps (N_t) are partially (or not) detected. Low-Frequency Noise (LFN) offers the opportunity to overcome these limitations and to pursue defects characterization even in case of ultra-thin silicon film.

The word "*noise*" is largely used in microelectronics and it can be associated to different domains. Generally, it indicates random fluctuations of a physical characteristic around its average value during time. Noise is usually something to avoid because it affects the experimental results, and it is also difficult to control. A good example is the "*background*" noise. Considering an integrated circuit, one area can distort the output signal of another one because of coupling effects. This modifies the signal integrity and limits the circuit performances [128], [129].

Looking at one single resistor under constant polarization, the current (or voltage) magnitude is not really constant but fluctuates around an average value. Figure V-1 shows an example of the current (I) measured as a function of time. I should be equal to $1\mu A$ but in reality it oscillates. This is due to the presence of noise sources. To overcome the problem, conventional tools like amperemeter, LCR meter or Source Measurement Unit (SMU) give averages of the measured quantities (see Integration time in Sec. II.2). Consequently, the fluctuations are masked and stable results are obtained.

However, the investigation of noise sources could enrich the knowledge about the transistor quality. Signal fluctuations can be classified into two families according to their origin: they can be due to "*external*" factors, thus not related to the device properties, or due to "*internal*" characteristics of the structure. External sources of noise cannot bring any fruitful information concerning the device quality; they just limit the analysis. Noise due to internal factors can also limit I_D-V_G or quasi-static capacitance techniques, but in case of low-frequency noise measurements, they can be used to extrapolate information concerning the interfaces quality [130].

LFN has been widely applied for the characterization of FD-SOI transistors [131]–[133]. It was also used to characterize high resistive SOI wafers with evaporated metal contacts [64], [134]. However, the presence of Schottky barriers made the extraction long and complicated. Diab *et al.* performed first LFN characterization on SOI substrates using pseudo-MOSFET but the obtained D_{it} were not coherent with the expected quality of the fabrication process ($> 10^{13} cm^{-2} eV^{-1}$ instead of $< 10^{12} cm^{-2} eV^{-1}$) [55].

After a review of the basic theory of low-frequency noise (Sec. V.1.1 and Sec. V.1.2), we will focus on the pseudo-MOSFET configuration (Sec. V.1.3). In Sec. V.2 results obtained using different experimental conditions will be presented. A physical model supported by numerical calculations will be discussed in Sec. V.3 and compared with the measured trends (Sec. V.4). In conclusion, Sec. V.5 addresses the impact of defects induced by the probe penetration in the silicon film.

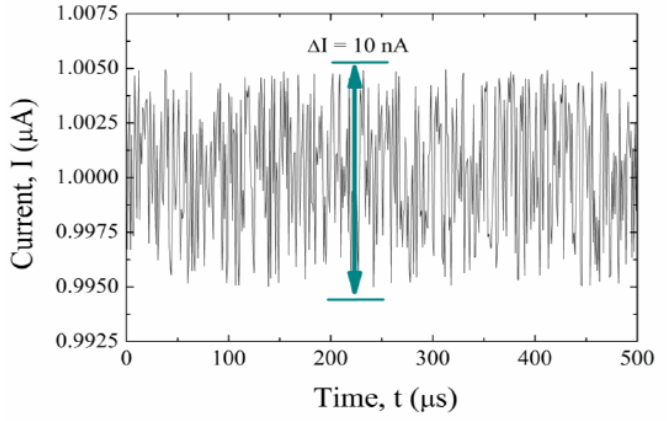

Figure V-1: Example of noise fluctuations in a resistor under constant current flow *I* [135].

V.1.1 Noise parameters: the Power Spectral Density of a signal

As shown in Figure V-1, the current through one resistor is not constant but it fluctuates in time. Independently of the source, I can be modeled as the sum of a median value I_0 and the contribution due to fluctuations (δI) [136]:

$$I(t) = I_0 \pm \delta I(t) \tag{V.1}$$

Equation (V.1) is expressed in the time domain and two main limitations arise from experimental point of view:

- Low δI amplitudes are difficult to detect;
- The investigation of any possible periodicity is problematic, especially in case of different phenomena that interact at the same time.

The best way to overcome these issues is to perform a Fast Fourier Transform (FFT) and work in the frequency domain [137]. A sum of different harmonics with adapted frequencies and amplitudes can recompose any signal expressed in the time domain (Figure V-2).

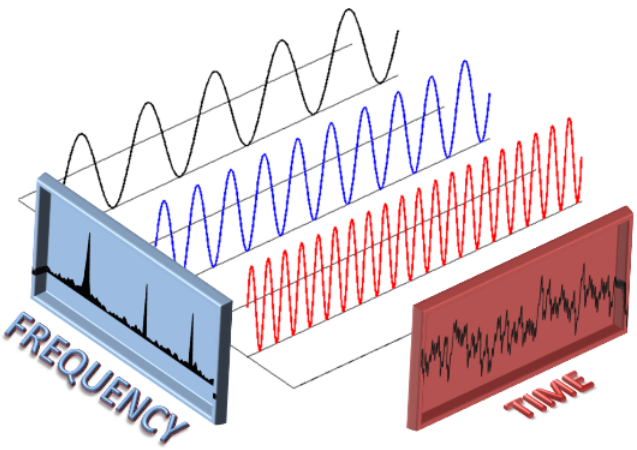

Figure V-2: Representation in the time domain of a signal modeled by several harmonics in the frequency domain [138].

In case of LFN characterization, the Power Spectral Density (PSD) of a signal becomes the main parameter. It quantifies the dissipated power on a *1Ω* resistive load integrated in time and its unit is *W/Hz*. For any function *R(t)* expressed in the time domain, its PSD is computed suing the Fourier transform:

$$S(f) = \int_{-\infty}^{+\infty} R(t) \cdot e^{-2 \cdot \pi \cdot j \cdot f \cdot t} dt \tag{V.2}$$

For LFN analysis on MOSFETs, the PSD is measured either for current or voltage characteristics. Thus, *S(f)* can be associated to the current oscillations (S_{Id}) or to the voltage ones (S_{Vd}). The units are A^2/Hz and V^2/Hz, respectively. In a practical case, the S_{Id} is computed using the Fast-Fourier Transform (FFT) of the measured signal.

The noise is a statistical phenomenon and in order to perform suitable transformation from time to frequency domain, it is required to measure many samples of the signal. Thus, LFN measurements are longer than the static ones.

Next section shows a brief overview of the main internal sources of noise detected in MOS transistors.

V.1.2 LFN in MOSFETs

The "*internal*" noise sources in a MOSFET can be classified in two main families:

- *White noise*: it is a fundamental noise intrinsic to semiconductor materials and it is frequency independent. Thermal and shot noise are part of this group.
- *Excess noise*: it is frequency dependent and it is mostly visible at low frequency. The main contributions arise from generation-recombination (G-R) and *1/f* (flicker) noise.

Thermal noise

Thermal noise is due to random and uncorrelated thermal fluctuations in the material. Consequently, the power spectrum is frequency independent for any applied voltage or current [139]. Hence, it is classified as white noise. Note that in all the conductive materials, even in absence of applied bias or current, the room temperature induces electron oscillations which lead to continuous current fluctuations. Consequently, every resistor generates thermal noise. The associated current power spectrum is:

$$S_{Id} = \frac{4 \cdot k \cdot T}{R} \tag{V.3}$$

where *R* is the resistance value.

Shot noise

The shot noise is due to non-uniformity of the current flow through a junction. The electrons cross it independently and at random times [140]. The carrier flow leads to broadband white noise. Its power spectrum is proportional to *I*:

$$S_{Id} = 2 \cdot q \cdot I \tag{V.4}$$

Generation-recombination (G-R) noise

Generation-recombination (G-R) noise is due to random fluctuations induced by:

- A pair of free electron and hole which recombines (or is generated);
- Trapping of electrons by empty defects;
- Trapping of holes by discharging traps filled with electrons.

The PSD associated to the G-R noise due to carrier number (*N*) fluctuations induced by their interaction with traps (empty and filled) is [141]:

$$S_{Id}(f) = \frac{4 \cdot \overline{\Delta N^2} \cdot \tau_{Dit}}{1 + (2 \cdot \pi \cdot f)^2 \cdot \tau_{Dit}{}^2} \tag{V.5}$$

where ΔN is the average fluctuation of carrier number and τ_{Dit} is the traps time constant. The corresponding current power spectrum as a function of frequency (*f*) is shown in Figure V-3a. "*Lorentzian*" behavior versus *f* is found [142]. For low frequency values, S_{Id} exhibits a plateau, while after a corner frequency f_c, the characteristic decreases proportional to $1/f^2$.

The study of the defects time constant (τ_{Dit}) leads to fruitful information concerning the traps spatial location and energy distribution. τ_{Dit} is independent of the gate bias in case of uniform defects distribution in the device channel [143]. In contrast, when V_G induces a variation of traps time constant, with maximum around V_T, the associated D_{it} are located at interface of silicon film-oxide or in a thin depletion layer [137].

When all the traps have the same time constant, the spectrum generated in the time domain is known as Random Telegraph Signal (RTS). Long and tedious RTS measurements lead to the investigation of capture and emission time constants and traps location [144]. However, the random telegraph signal analysis can only be performed in very small area devices with few individual traps [145].

In case of standard MOSFET a more homogeneous traps distribution is present at oxide interface. Each group of traps with the same τ_{Dit} shows RT-signal in the time domain (Lorentzian spectrum in the frequency domain). Thus, the whole current spectrum will be given by the sum of several Lorentzian characteristics resulting in *1/f* behavior in the frequency domain (Figure V-3b).

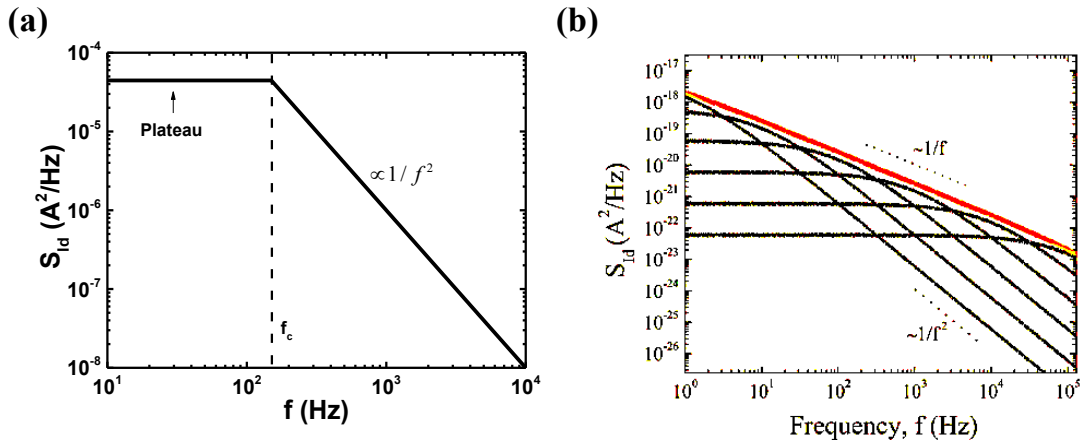

Figure V-3: (a) General trend of S_{Id} versus frequency in case of generation-recombination noise (Lorentzian-like behavior from Eq. (V.5)). (b) S_{Id} as a function of f where different Lorentzian characteristics were added together leading to flicker noise [135].

1/f (flicker) noise

The flicker noise (*1/f*) arises from the sum of different "*Lorentzian*" spectra. It is assumed that the defects are located at the oxide interface or very close to it (*3 nm* maximum distance inside the oxide) [146]. In a general case, the power spectral density has $1/f^{\gamma}$ dependency. Uniform traps distribution leads to $\gamma = 1$. In case of non-uniform N_t ($\gamma \neq 1$), γ is larger than *1* when the traps density is increasing deeper into the oxide, otherwise $\gamma < 1$ [147].

Even if no universal explanation exists today, it is commonly accepted that flicker noise in MOSFET originates from conductivity σ variation ($\delta\sigma$) [148]. $\delta\sigma$ can be due to carrier number fluctuations (model proposed by McWhorter [149]) or mobility fluctuations (Hooge's approach [150]). Both sources of noise are present in standard transistors, but a dominant one can usually be identified [148].

Mobility fluctuation (HMF) model

Hooge proposed that the conductance fluctuations are only due to the variation of the carrier mobility [141] induced by phonon scattering [151]. Hence, the current power spectrum is given by:

$$S_{Id} = \frac{I_D^2 \cdot q \cdot \alpha_H}{f \cdot S \cdot Q_i} \tag{V.6}$$

where α_H is the Hooge parameter dependent to the crystal quality, S is the die surface and Q_i is the inversion charge density.

Carrier number fluctuations (CFN) model

McWhorter proposed that the conductance fluctuations are due to the variation of the mobile charge density induced by trapping or detrapping phenomena taking place in a MOSFET [149]. A change of fixed defects produces flat-band voltage (δV_{FB}) oscillations [148], which are detected on the current measurement. The current power spectrum is:

$$S_{Id} = g_m^2 \cdot S_{Vfb} \tag{V.7}$$

where S_{Vfb} is the power spectrum associated to flat-band voltage oscillations. S_{Vfb} is defined in the McWhorter's model as [152]:

$$S_{Vfb} = \frac{q^2 \cdot \lambda \cdot k \cdot T \cdot N_t}{f^{\gamma} \cdot S \cdot C_{OX}^2} \tag{V.8}$$

λ is the tunneling attenuation length calculated using Wentzel-Kramers-Brillouin (WKB) theory [25]. Its value is usually ≈ *1 Å*. N_t is the density of slow traps per unit volume ($cm^{-3}eV^{-1}$).

Carrier number with correlated mobility fluctuations (CNF+CMF) model

The two models describe $\delta\sigma$ using two different physical phenomena. However, recent studies [148], [153] have proved that a correlation exists between the two approaches.

Assuming that trapping or detrapping phenomena are the dominant sources of noise, a change of flat-band voltage impacts the electric field in the channel, thus the carrier mobility. A universal expression of S_{Id} can take into account both effects: the fluctuations of carrier concentration (McWhorter's model) and the associated impact on the mobility term ($\alpha_{sc} \cdot \mu_{eff} \cdot C_{OX}$) [148]:

$$S_{Id} = g_m^2 \cdot S_{Vfb} \cdot \left(1 \pm \alpha_{sc} \cdot \mu_{eff} \cdot C_{OX} \cdot \frac{I_D}{g_m}\right)^2 \tag{V.9}$$

where α_{sc} is the Coulomb scattering coefficient [154]. The sign ± identifies the defects type: "+" in case of donor-like traps and "–" in case of acceptor-like N_t. Defining $\Omega_C = \alpha_{sc} \cdot \mu_{eff} \cdot C_{OX}$ and the gate bias power spectrum as $S_{Vg} = S_{Id}/g_m^2$, Eq. (V.9) can be written as [155]:

$$S_{Vg} = S_{Vfb} \cdot \left(1 \pm \Omega_C \cdot \frac{I_D}{g_m}\right)^2 \tag{V.10}$$

The mobility contribution becomes important only in strong inversion (or accumulation) regime, while in the subthreshold region its impact is negligible ($S_{Vg} \approx S_{Vfb}$).

V.1.3 State of art of LFN in pseudo-MOSFET

Kushner *et al.* [64], [134] have analyzed the LFN generated in high resistive SOI substrates using ground-signal-ground and circular contacts. The characterization succeeded but the Schottky barriers make the extraction procedure complicate and tedious to apply. Diab *et al.* [55] have performed LFN in pseudo-MOSFET configuration. Figure V-4a shows the measured S_{Id} versus f for different V_G. Clear $1/f$ trend was obtained, proving that flicker noise can be detected also in SOI substrates using adjustable probe pressure contacts. Figure V-4b shows the S_{Id}/I_D^2 versus drain current. A plateau is present for low I_D (in weak inversion regime) followed by $1/I_D$ decrease for higher drain current. This behavior is specific to the CNF model.

The extracted D_{it} values were surprisingly large (*i.e.*, $\approx 2 \cdot 10^{13} cm^{-2} eV^{-1}$ instead of a maximum of $\approx 10^{12} cm^{-2} eV^{-1}$ in case of non-passivated samples). Additionally, the S_{Id} signal was higher for passivated than for non-passivated SOI. No clear explanation for these results was provided.

Was there an issue of the experimental setup? Do we only need to correctly adapt the models for the Ψ-MOSFET configuration in other to obtain reasonable D_{it} values?

The aim of our work on LFN characterization was to find the answers to these questions. We approched the topics with both experiments and modeling.

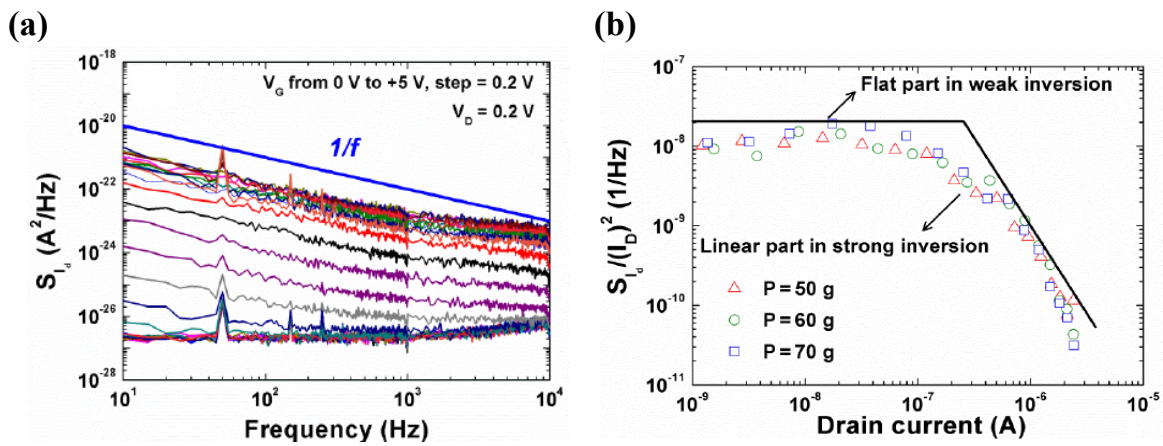

Figure V-4: (a) S_{Id} versus frequency for different gate bias values. (b) S_{Id}/I_D^2 versus drain current for different probe pressure. The same SOI structure with *88 nm* thick silicon film and *145 nm* thick BOX was used in both cases. The top surface was non-passivated [55].

V.2 LFN characterization in Ψ-MOSFET

To understand if the obtained large density of interface traps was due to measurement setup issues, in this section we focus on experiments using different configurations. After presenting the setup (Sec. V.2.1), we will discuss the reproducibility (Sec. V.2.2) and the role of the pressure needles (Sec. V.2.3). Finally, in Sec. V.2.4 the impact of inter-probe distance and die area variations will be addressed.

V.2.1 Measurement setup

Low-frequency noise measurements were performed using adjustable probe pressure Jandel® station. In order to reduce as much as possible the external noise, the probing tool was placed inside an isolated box, built for this type of analysis. The SOI wafer was contacted using similar configuration as for I_D-V_G measurements (see Sec. II.2). The source was grounded while V_D was applied using a Programmable Biasing Amplifier (PBA) and a low-noise amplifier [156]. All the results presented in this section were obtained using $V_D = 100\ mV$. The PBA was remotely controlled by a PC and simultaneous measurements of the *d.c.* drain current I_D and the *a.c.* term δI over a large frequency range (*1 Hz* to *500 kHz*) were performed. The software automatically computes the FFT and releases the $S_{Id}(f)$ term [156].

Programmable bias amplifier characterizes the Device Under Test (DUT) as a resistor where a constant current is applied (Figure V-5). In case of high resistive materials, to minimizes the impact of the experimental tools on the DUT, the best configuration to measure the noise is at constant current I [136].

To apply the gate bias, the PBA has a second source but it is limited at ± *5 V*. Diab *et al.* [55] have overcome the problem using a battery in series with the PBA. This setup is not so accurate. To improve it, a Keithley 236® bias source was preferred to control V_G. We have chosen this instrument because the voltage can be swept between *-100 V* to *100 V* with *100 µV* step and it generates low noise. In this way, higher V_G resolution is obtained albeit the measurement setup becomes more complex and time consuming. The programmable biasing amplifier has to work in parallel with the Keithley 236® and manual (V_G) sweep is required. Figure V-5 summarized our setup.

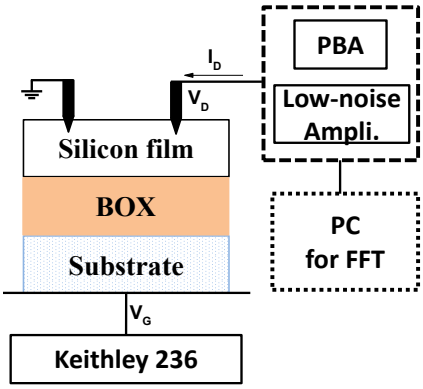

Figure V-5: Measurement setup for LFN in SOI structure. The source is grounded. The drain bias V_D was applied using the PBA and low-noise amplifier while V_G was controlled by Keithley 236® bias source.

Figure V-6a shows the measured power spectrum versus f in case of constant drain current ($I_D = 107\ nA$) (line) and at $I_D = 0\ A$ (dashed line). S_{Id} at zero current represents the system noise. $1/f$ behavior is added as eye-guide. The obtained spectrum is clearly dominated by flicker noise. For low frequency values, S_{Id} obtained using $I_D > 0$ is much higher than S_{Id} at $I_D = 0$. Thus, the LFN signal induced by trapping/detrapping effects can be unambiguously identified. Increasing f, the two curves merge so the flicker noise cannot be isolated. As for standard MOSFET, it is not possible to perform the extraction in the high frequency range [135].

The steps necessary to compute S_{Id}/I_D^2 and determine the interface traps density are:

- Perform several S_{Id} versus f measurements using different I_D values. In case of Ψ-MOSFET configuration, the drain current was swept by changing the applied V_G (V_D was kept at $100\ mV$);
- Chose an extraction frequency f_{ext}, the same for all the characteristics; S_{Id} at f_{ext} are collected for different I_D;
- S_{Id}/I_D^2 is then calculated and traced versus I_D.

In order to reduce the impact of system noise, $S_{Id}\ (I_D = 0\ A)$ was subtracted from $S_{Id}\ (I_D > 0\ A)$ before any further data treatment.

To pursue defects extraction, it is required to relate the LFN and the static characterization. Dividing both terms of Eq. (V.7) by I_D^2, the equation becomes:

$$\frac{S_{Id}}{I_D^2} = \frac{g_m^2}{I_D^2} \cdot S_{Vfb} \qquad \text{(V.11)}$$

Equation (V.11) clearly shows that S_{Id}/I_D^2 is proportional to two terms: $(g_m/I_D)^2$ and S_{Vfb}. The static characteristic $(g_m/I_D)^2$ is dominated by the subthreshold slope, therefore, it is sensitive to fast traps called D_{it} in this chapter. On the contrary, the flat voltage power spectrum (S_{Vfb}) is directly proportional to N_t (deep traps in Eq. (V.8)). Thus, on the S_{Id}/I_D^2 curve, both contributions of fast and slow traps are present. In order to separate them, $(g_m/I_D)^2$ is evaluated from static measurements. After performing noise measurements, S_{Vfb} is computed from the ratio $(S_{Id}/I_D^2)/(g_m/I_D)^2$. Consequently, it only contains N_t term as shown in Eq. (V.8) [156].

To perform correct interface quality extraction, S_{Vfb} thus N_t, has to be independent of the extraction frequency f_{ext}. Figure V-6b shows $S_{Id}/I_D^2 \cdot f_{ext}$ versus drain current for different f_{ext}. In case of low current values, small differences are visible between the curves. On the contrary, remarkable overlap is obtained for large I_D. We conclude that the extraction frequency does not limit the analysis.

For comparing the obtained results with what is present in the literature, all the extracted characteristics were performed using $f_{ext} = 10\ Hz$.

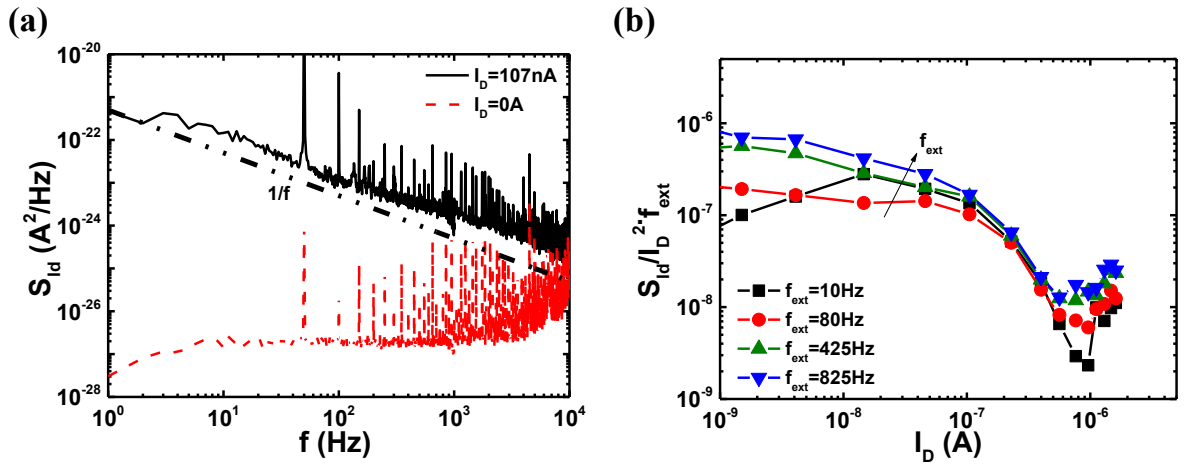

Figure V-6: (a) Measured S_{Id} versus f in case of constant drain current (line) and $I_D = 0\ V$ (dashed line). $1/f$ is also added as eye-guide. (b) $S_{Id}/I_D^2 \cdot f_{ext}$ versus I_D for different extraction frequencies. The SOI structure had *88 nm* silicon film thickness and *145 nm* BOX thickness. The top surface was non-passivated and positive gate bias was applied.

An example of defects extraction procedure is shown in Figure V-7a. S_{Id}/I_D^2 is traced as a function of drain current obtained from the data in Figure V-6b. The characteristic reconstructed from static drain current multiplied by S_{Vfb} is also added (empty symbols). Good overlap is achieved for $S_{Vfb} \approx 2.5 \cdot 10^{-9}\ V^2/Hz$.

Equation (V.8) leads to N_t calculation. All the terms are known, except for the surface, S. In case of pseudo-MOSFET, the surface which contributes to the current is apparently given by the inter-probe distance d and the geometrical factor $f_G = W/L$ [55]:

$$S = W \cdot L = \frac{W}{L} \cdot L^2 = f_G \cdot d^2 \qquad (V.12)$$

Thus, one gets $N_t = 1.3 \cdot 10^{22} cm^{-3} eV^{-1}$. This value is clearly too large and not realistic but it is comparable to what was previously found [55].

For large gate bias values, $(g_m/I_D)^2$ differs from S_{Id}/I_D^2. This is due to mobility variations. To perform a better extraction, Figure V-7b shows S_{Vfb} calculated using Eq. (V.11) versus drain current (plain symbols). The flat-band voltage power spectrum is almost constant for low values of drain current and decreases when I_D increases, confirming the presence of mobility variation effects. A better representation is obtained computing the flat voltage power spectrum using Eq. (V.9) (empty symbols). A good fit was found in case of $\alpha_{SC} = 5 \cdot 10^4\ Vs/C$ and acceptor-like defects [148]. Using CNF+CMF model, S_{Vfb} has a constant value on a larger I_D interval. The sharp increase obtained for high I_D is due to the impact of access resistance (see the plain symbols in Figure V-7a) [157].

This extraction procedure will be used in the next sections because it allows to separate fast and slow traps contributions, taking into account also the mobility fluctuations.

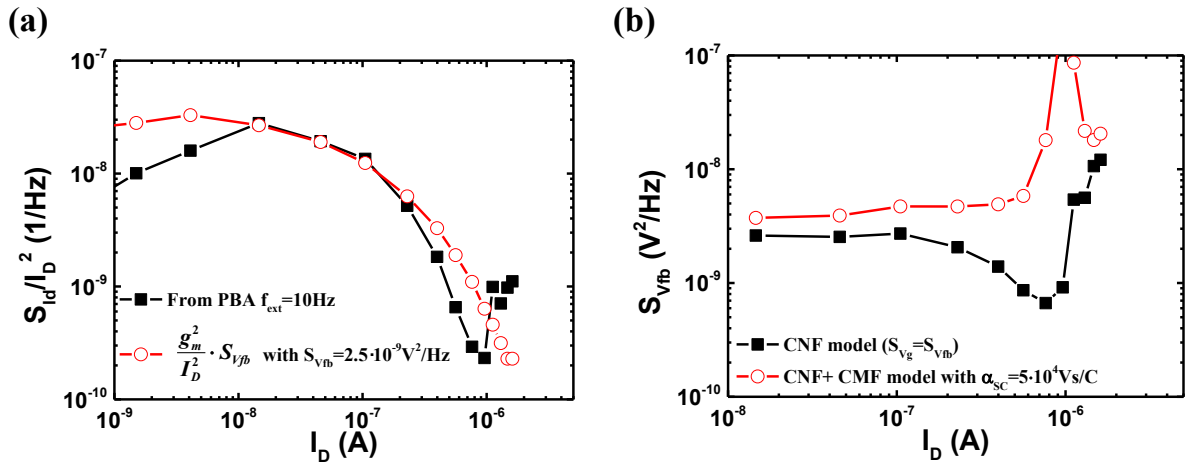

Figure V-7: S_{Id}/I_D^2 versus drain current obtained from Figure V-6 (plain symbols). The characteristic computed from static I_D-V_G and multiplied by S_{Vfb} was added (empty symbols). Good overlap is found using $S_{Vfb} = 2.5 \cdot 10^{-9}\ V^2/Hz$. The inter-probe distance was $d = 1\ mm$. (b) S_{Vfb} was calculated as a function of I_D using Eq. (V.11) (plain symbols) and Eq. (V.9) (empty symbols), respectively. The data presented in Figure V-7a was used.

V.2.2 Reproducibility issues

As in case of capacitance measurements (see Sec. III.2.2) the quality of the back contact may limit the characterization and consequently the extracted interface traps density. Is this happening for LFN?

Figure V-8 shows S_{Id}/I_D^2 versus drain current with (dashed line) and without (line) using the vacuum system on the metallic chuck in case of positive (a) and negative (b) V_G. The corresponding $(g_m/I_D)^2$ as a function of I_D are presented in the insets. Even if S_{Id}/I_D^2 characteristics are lightly different, it is possible to conclude that the quality of the back contact cannot be the main reason behind the large D_{it} values obtained previously. V_G is only used to polarize the substrate, while δI is generated by the current flow between source and drain contacts. However, the use of vacuum system increases the reproducibility, thus it will always be applied to the metallic chuck.

Additionally, the dashed-dot line in Figure V-8 represents the measured S_{Id}/I_D^2 obtained using different probes on the same SOI die. Even if the shape is similar, more than one order of magnitude difference is found in the plateau height, which implies a factor of *10* of difference in the extracted N_t (since the corresponding $(g_m/I_D)^2$ superpose as shown in the inset). Thus, the probe choice seems to have a tremendous impact for LFN analysis, unlike in the other characterization techniques.

For negative gate bias, the behavior of S_{Id}/I_D^2 does not follow the static $(g_m/I_D)^2$ trend (inset in Figure V-8b) which makes the data inappropriate for any extraction. Hence, in the following sections we only focus on positive gate bias.

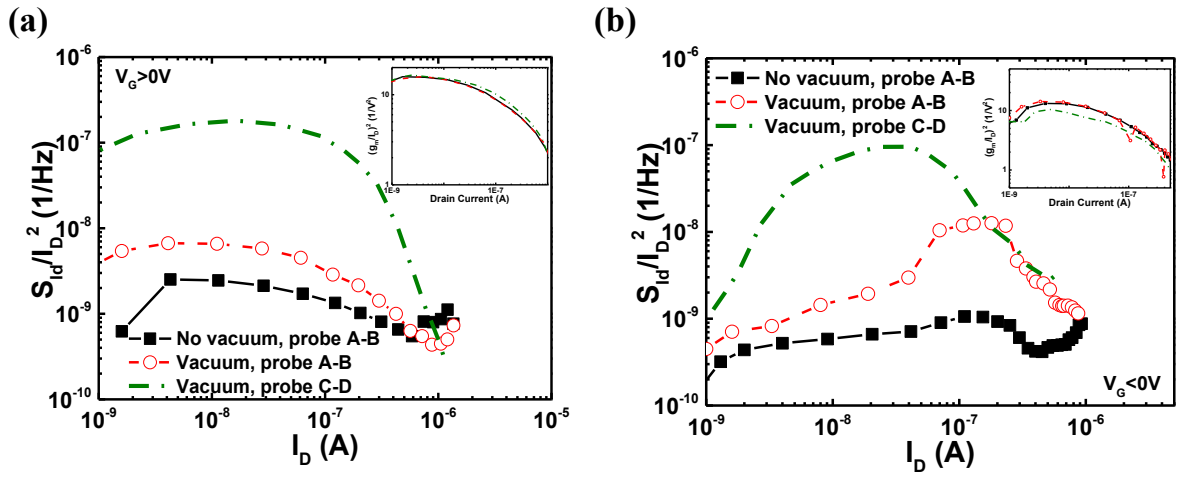

Figure V-8: S_{Id}/I_D^2 versus drain current in case of electrons (a) and holes (b). The characteristics obtained without (line) and with (dashed line) the vacuum system are compared. Measurements performed using different needles of the same Jandel® station are also shown (dash-dot line). SOI structure with non-passivated *88 nm* top silicon film thickness and *145 nm* BOX thickness. The corresponding measured $(g_m/I_D)^2$ versus drain current are shown in the insets.

The probes affect the obtained S_{Id}/I_D^2. Is the reproducibility between measurements responsible? The negative answer is documented in Figure V-9. Three different dies on the same SOI structure were tested. The curves clearly overlap. Even if the probe quality affects the characteristics (see Figure V-8), the use of the same needles ensures good reproducibility of measurements. Thus, in the following sections all the comparisons will involve only curves obtained with same probes.

The needles contact looks critical, so the natural next step requiring investigation is the impact of the pressure applied on the tips.

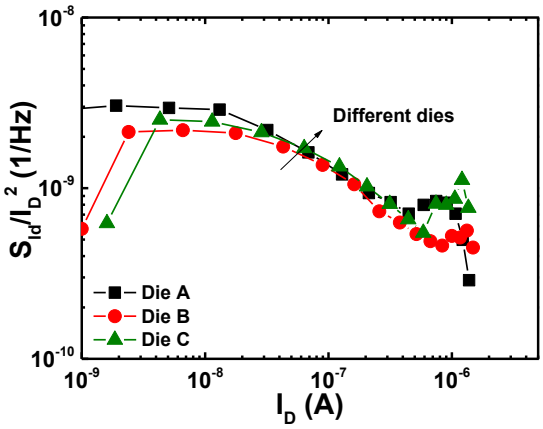

Figure V-9: S_{Id}/I_D^2 versus I_D obtained from different dies coming from the same wafer. Same SOI as in Figure V-8.

V.2.3 Probe pressure impact

The increase of the pressure applied on the probes is known to change the access resistance for I_D-V_G measurements (Sec. II.3.3). At the same time the craters generated by the probes are larger [65]. Could this be related to the obtained N_t magnitude? To investigate this aspect, pressure impact was studied on both passivated and non-passivated SOI.

Figure V-10a shows the measured S_{Id}/I_D^2 versus drain current in case of electrons for non-passivated surface. Different probe pressures were tested. The SOI structure had *88 nm* top silicon film thickness and *145 nm* BOX thickness. To isolate only the pressure impact, the probes were placed on the silicon surface and the pressure was increased step by step, without moving them. The characteristics are almost pressure independent, after $p = 50\ g$.

The same analysis was performed on a passivated sample (Figure V-10b). The pressure values are different because in case of passivated top silicon film the *4 nm* dry oxide requires higher p for good ohmic contact. Stronger pressure dependency is obtained in this case. The higher the pressure, the lower the measured S_{Id}/I_D^2 plateau. Note also that for *100 g* the curve does not show the typical CNF behavior anymore.

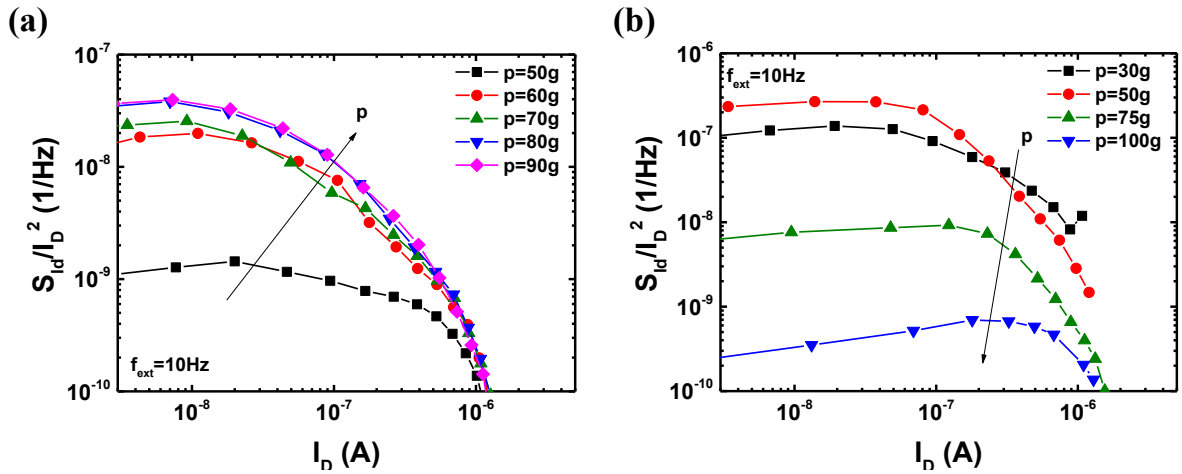

Figure V-10: S_{Id}/I_D^2 versus drain current for positive gate bias. Characteristics obtained using different probe pressures. The SOI structure had *88 nm* thick silicon film and *145 nm* thick BOX. Non-passivated (a) and passivated (b) top silicon surfaces were used.

In order to isolate the N_t contribution from the fast traps, S_{Vfb} was calculated using Eq. (V.9) in case of non-passivated and passivated top silicon surface (Figure V-11). The data presented in Figure V-10a and Figure V-10b were used. S_{Vfb} obtained in case of non-passivated surface is almost independent of I_D and p, making it suitable for N_t extraction. On the contrary, for the passivated samples, the flat-band voltage power spectrum is not constant and strongly dependent to p.

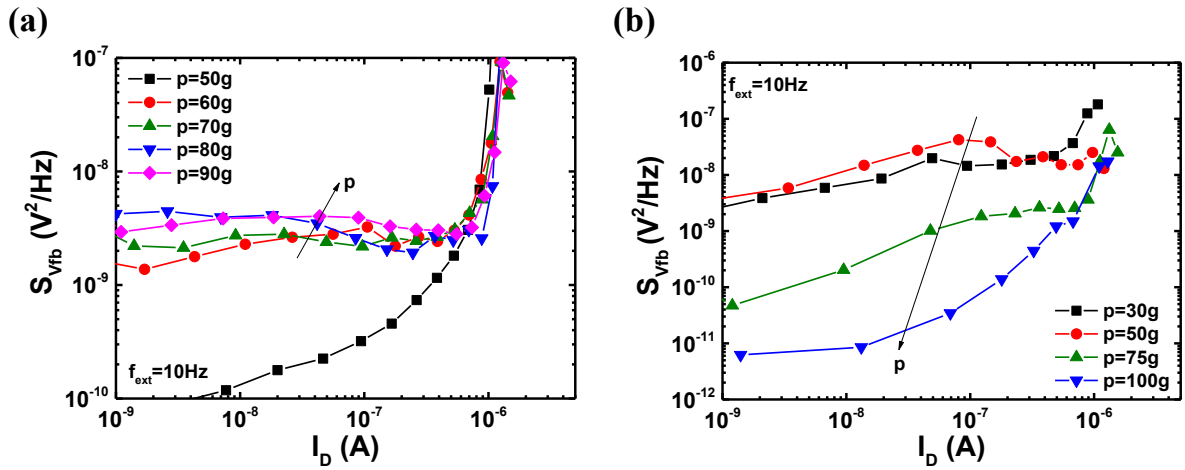

Figure V-11: S_{Vfb} versus drain current computed using Eq. (V.9). The analysis was performed in case of non-passivated (a) and passivated (b) top silicon film. Data from Figure V-10.

Before concluding this part, we compare the characteristics obtained on passivated and on non-passivated samples. One of the open questions in [55] concerned the higher measured S_{Id} versus f in case of high quality passivated substrate than for non-passivated one (inset Figure V-12a). Since the probe pressure was proved to have a crucial impact on LFN measurements, the comparison between passivated and non-passivated samples needs precautions. Two configurations are possible:

- Same access resistance. Higher pressure is needed in case of passivated samples which may induce large density of defects in the silicon film;
- Same probe pressure, which should lead to similar defects concentration induced by the probe in the silicon surface but different R_{SD}.

Figure V-12a shows the measured S_{Id}/I_D^2 versus drain current in case of non-passivated (plain symbols) and passivated (empty symbols) SOI wafers. The characteristic on non-passivated sample was performed using the optimum pressure ($p = 80\ g$). In case of passivated surface, the measurements were obtained using similar probe pressure ($p = 75\ g$, circle symbols) and comparable access resistance ($p = 100\ g$, triangle symbols). For large I_D, the current power spectrum obtained for passivated samples is larger than for non-passivated one. Note that S_{Id}/I_D^2 term contains both D_{it} and N_t contributions. Figure V-12b shows the corresponding S_{Vfb}. The conclusion is not clear. However, comparing the curves with similar pressure, the large difference obtained in the S_{Id} spectrum between passivated and non-passivated samples is reduced, especially for large I_D. Two conclusions arise from here:

- The defects related to the probe pressure play an important role;
- Passivated surface seems more complicated to analyze, so we focus on the non-passivated wafers for the next sections.

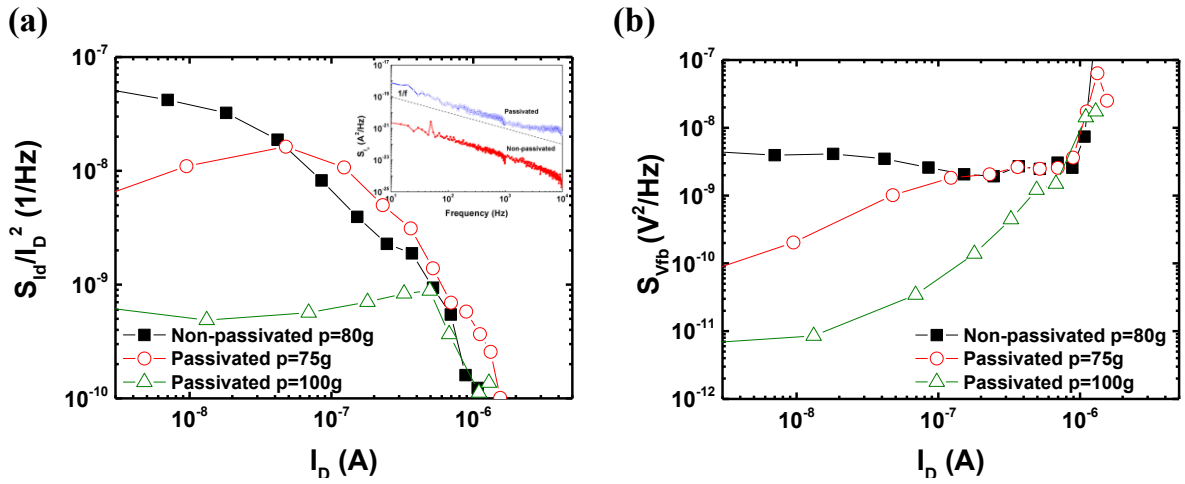

Figure V-12: (a) S_{Id}/I_D^2 versus drain current in case of non-passivated (plain symbols) and passivated (empty symbols) SOI structure. The data discussed in Figure V-10 were used. (b) The corresponding S_{Vfb} extracted using Eq. (V.9) are shown. Inset: Measured S_{Id} versus f in case of passivated and non-passivated samples [55].

V.2.4 Impact of inter-probe distance and die area

In case of Ψ-MOSFET configuration, the surface S is not well defined. The LFN needs S for N_t extraction: S_{Vfb} is proportional to $1/S$ (Eq. (V.8)). In this context, experimental effects of the inter-probe distance or the whole die area should be visible.

Figure V-13a compares S_{Id}/I_D^2 versus drain current obtained for different inter-probe distance: *1 mm*, *2 mm* and *3 mm*. To perform these characteristics we were forced to use different needles, because it is not possible to change the probe position in the Jandel® station. The curves present similar behavior and the plateau position is in the same interval. Only for large drain current values significant variations are present, probably due to different access resistance impact [158]. The corresponding S_{Vfb} as a function of drain current is shown in Figure V-13b. Light S_{Vfb} variation is found.

Table V-1 shows the S_{Vfb} values obtained at constant I_D (dashed circle in Figure V-13b) and the calculated S using Eq. (V.12): $S = f_G \cdot d^2$. The flat-band voltage power spectrum variation is very small with respect to the real surface variation. Consequently, the inter-probe distance plays a secondary role on LFN characteristics.

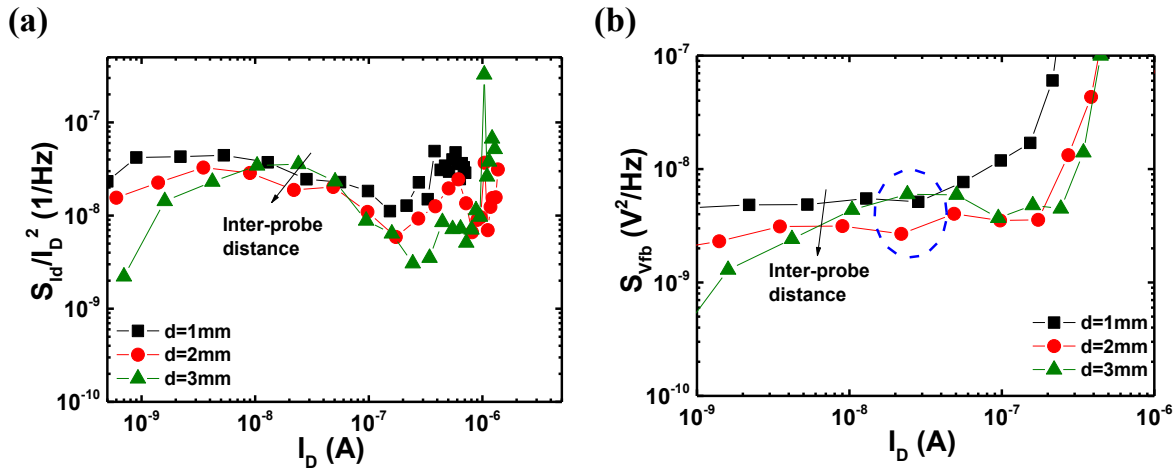

Figure V-13: (a) Measured S_{Id}/I_D^2 versus drain current in case of different inter-probe distance. The tests were performed on the same SOI wafer with *88 nm* top silicon film thickness and *145 nm* BOX thickness. The corresponding S_{Vfb} versus drain current is shown in Figure V-13b.

d (mm)	*S (mm²)*	S_{Vfb} (V^2/Hz)
1	0.75	$5\cdot10^{-9}$
2	3	$2.7\cdot10^{-9}$
3	6.75	$6\cdot10^{-9}$

Table V-1: S_{Vfb} obtained from Figure V-13b for $I_D \approx 250\ nA$ (dashed region). Computed surface using $S = f_G \cdot d^2$.

Figure V-14 compares S_{Id}/I_D^2 (a) and corresponding S_{Vfb} (b) versus drain current measured using different die areas. Despite a significant variation of real die surfaces, the obtained S_{Vfb} values are close. Only very large die (*8 x 8 mm²*), where parasitic factors limit the analysis, has a lower noise.

No clear explanation or trends emerged from the experimental parameters. However, the conclusion is that *S* is clearly not well defined for the case of Ψ-MOSFET. Modeling is necessary to understand the physical phenomena and identify the surface representative for the noise measurements.

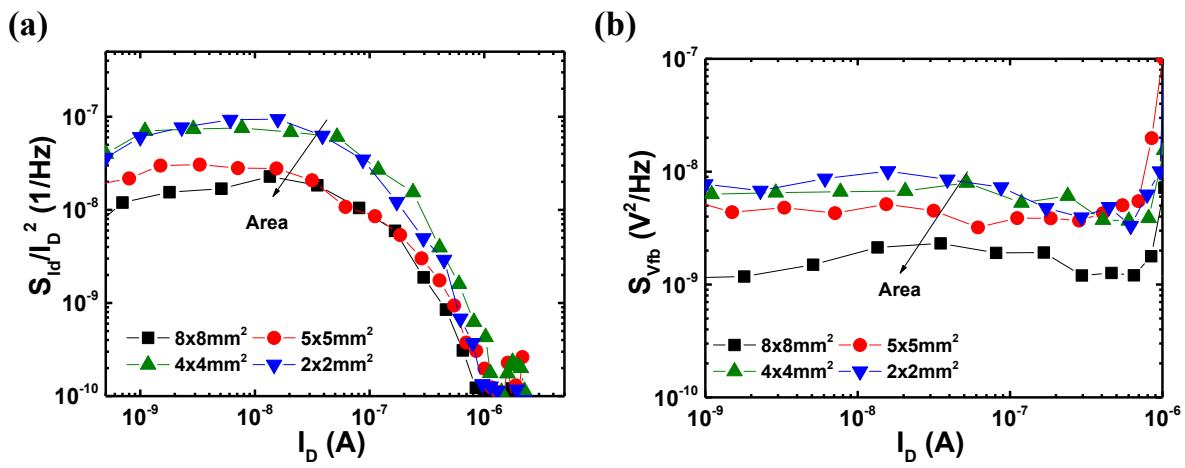

Figure V-14: S_{Id}/I_D^2 (a) and corresponding S_{Vfb} (b) as function of drain current in different die areas. The same SOI structure as in Figure V-13 was used.

V.3 LFN in inhomogeneous material

Trefan *et al.* [136] have derived the LFN generated in a resistor under constant bias using the power density. The equations will be adapted to the case of constant current flow and the δI source will be associated to the variation of the carrier density (CFN model) (Sec. V.3.1). In Sec. V.3.2, the LF-noise will be computed using a differential equation solver (FlexPDE®) to explain the experimental trends discussed in Sec. V.2.

V.3.1 Physical model

Considering a resistor with a constant current I applied, the dissipated power P is proportional to I and the bias V measured across the resistor:

$$P = I \cdot V \tag{V.13}$$

Consequently, P is proportional to the material conductivity σ and the electric field ξ:

$$P = I \cdot V = \int_{\Omega} \sigma \cdot \xi^2 \cdot d\Omega \tag{V.14}$$

where Ω is the resistor volume.

Using Tellegen theorem [159], it is possible to show that in a network where constant current I is applied, the current fluctuations δI are due to the sum of conductivity oscillations $\delta\sigma$:

$$\delta I = \frac{1}{V} \int_{\Omega} \delta\sigma \cdot \xi^2 \cdot d\Omega \tag{V.15}$$

Thus, the associated current power spectrum becomes:

$$S_{Id} = \overline{\delta I^2} = \frac{1}{V^2} \int_{\Omega} \overline{\delta\sigma^2} \cdot \xi^4 \cdot d\Omega \tag{V.16}$$

The Ohm law relates the conductance G with V and I: $I = V \cdot G$. Using Eq. (V.13), G can be expressed as a function of power density:

$$G = \frac{P}{V^2} = \frac{1}{V^2} \int_{\Omega} \sigma \cdot \xi^2 \cdot d\Omega \tag{V.17}$$

Hence, I^2 becomes:

$$I^2 = (V \cdot G)^2 = \frac{1}{V^2} \left[\int_{\Omega} \sigma \cdot \xi^2 \cdot d\Omega \right]^2 \tag{V.18}$$

Merging Eq. (V.16) and Eq. (V.18), it is possible to write S_{Id}/I_D^2 expression:

$$\frac{S_{Id}}{I_D^2} = \frac{1}{\sigma^2} \cdot \frac{\int_{\Omega} \overline{\delta\sigma^2} \cdot \xi^4 \cdot d\Omega}{\left[\int_{\Omega} \xi^2 \cdot d\Omega \right]^2} \tag{V.19}$$

To complete the derivation, it is required to include also the conductivity fluctuations. $\overline{\delta\sigma^2}$ associated to carrier number variation (CNF model) is [135]:

$$\overline{\delta\sigma^2} = \left(\frac{\delta\sigma}{-\delta V_{FB}}\right)^2 \cdot S_{Vfb_area} \tag{V.20}$$

where S_{Vfb_area} is the normalized flat-band voltage spectrum density: $S_{Vfb_area} = S_{Vfb}/S$. The effective volume (Ω_{eff}) in Eq. (V.19) represents the region where the noise is concentrated:

$$\Omega_{eff} = \frac{\left[\int_{\Omega} \xi^2 \cdot d\Omega\right]^2}{\int_{\Omega} \xi^4 \cdot d\Omega} \leq \Omega \tag{V.21}$$

In case of SOI substrates characterized in pseudo-MOSFET configuration, the inversion (or accumulation) channel induced by V_G is very close to the silicon film-BOX interface. Thus, Ω_{eff} can be replaced by the effective surface term (S_{eff_LFN}):

$$S_{eff_LFN} = \frac{\left[\int_{S} \xi^2 \cdot d\Omega\right]^2}{\int_{S} \xi^4 \cdot d\Omega} \leq S \tag{V.22}$$

where S is the whole die area. S_{eff_LFN} will be equal to S only for uniform current density [136], which is not the case of pseudo-MOSFET. Using Eq. (V.20) and Eq. (V.22), S_{Id}/I_D^2 becomes:

$$\frac{S_{Id}}{I_D^2} = \left(-\frac{1}{\sigma} \cdot \frac{\delta\sigma}{\delta V_{FB}}\right)^2 \cdot \frac{S_{Vfb_area}}{S_{eff}} \tag{V.23}$$

In the next section the distribution of the surface potential Ψ_S on the silicon film will be obtained numerically by solving the drift-diffusion equation in the top silicon film and Eq. (V.23) will be used to compute the LFN generated in the Si layer.

V.3.2 Computation of LF-noise

Configuration of the differential equation solver (FlexPDE®)

In order to compute the low-frequency noise obtained in case of bare SOI wafers, a differential equation solver (FlexPDE®) was used. A *2*-dimensional plane structure emulates the top silicon surface of the die (Figure V-15). Source and drain are included as a perfect metal contacts with given radius (R_0) and placed at defined distance (d).

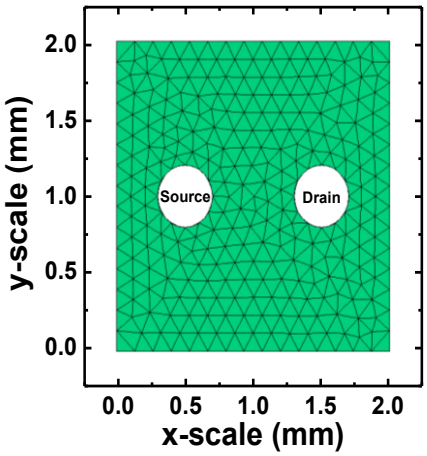

Figure V-15: Mesh of the computed structure with source and drain contacts. R_0 = *200 µm* and die surface equal to *2 mm* x *2 mm*. The inter-probe distance is *1 mm*. 3000 nodes were used for meshing.

Lambert equation is used to calculate the charge density induced by V_G at the interface between the buried oxide and the top silicon film [99]. Consequently, Ψ_S on the whole surface of the Si layer is obtained numerically solving the Laplace equation:

$$\mathrm{div}\cdot\left(\sigma\cdot\mathrm{grad}(\Psi_S)\right)=0 \tag{V.24}$$

The electric field is directly computed from Ψ_S:

$$\xi=\mathrm{grad}\left(\Psi_S\right) \tag{V.25}$$

Equation (V.17) leads to the silicon film conductance and consequently to the drain current between the two contacts. Furthermore, Eq. (V.23) allows the LF-noise calculation.

Table V-2 summarizes the main input parameters used in FlexPDE®, knowing that:

- The chosen magnitudes (t_{OX}, t_{Si}, μ …) are close to the realistic values measured in pseudo-MOSFET configuration;
- The interface trap contributions are included using two different terms: D_{it} (fast traps) in the current computation and N_t (slow traps) which is present only in the LFN term (Eq. (V.23));
- The computation part will focus on SOI structure with *88 nm* top silicon film thickness and *145 nm* BOX thickness. The LFN signal is calculated for $V_G > 0\ V$, as in the experiments.

Parameters		Value / Range
BOX thickness	t_{OX}	145 nm
Top silicon film thickness	t_{Si}	88 nm
Low-field carrier mobility	μ_0	450 cm^2/Vs
Interface trap density (fast traps)	D_{it}	10^{10}-$10^{12}cm^{-2}eV^{-1}$
Deep traps used for LFN computation	N_t	10^{18}-$10^{20}cm^{-3}eV^{-1}$
Traps added in a localized region for LFN calculation	N_{t_added}	10^{18}-$10^{22}cm^{-3}$ eV^{-1}
Tunneling attenuation length	λ	1 Å
Die length, square samples ($L = W$)	L	1 mm – 10 cm
Probe radius	R_0	1-200 µm
Radius added to R_0 to generate a corona region	ΔR_0	1-200 µm
Inter-probe distance	d	1-3 mm
Drain bias	V_D	100 mV

Table V-2: Summary of input parameters required for FlexPDE® computation.

Preliminary results

Preliminary simulation results are shown in Figure V-16a. S_{Id}/I_D^2 is computed as a function of drain current for different N_t values. Note that D_{it} term was kept constant. The three curves have the same shape but higher N_t induces higher S_{Id}/I_D^2 plateau level. This is in agreement with Eq.(V.23). Keeping constant D_{it}, the change of N_t induces only a S_{Vfb} variation, thus a S_{Id}/I_D^2 vertical shift.

Figure V-16b presents the computed S_{Id}/I_D^2 versus I_D using different probe radius R_0: *1 µm*, *5 µm* and *10 µm*. For low I_D, more than one decade difference is found between the characteristics. Comparing Figure V-16a and Figure V-16b, it is obvious that R_0 induces S_{Id}/I_D^2 plateau shift comparable to N_t effects.

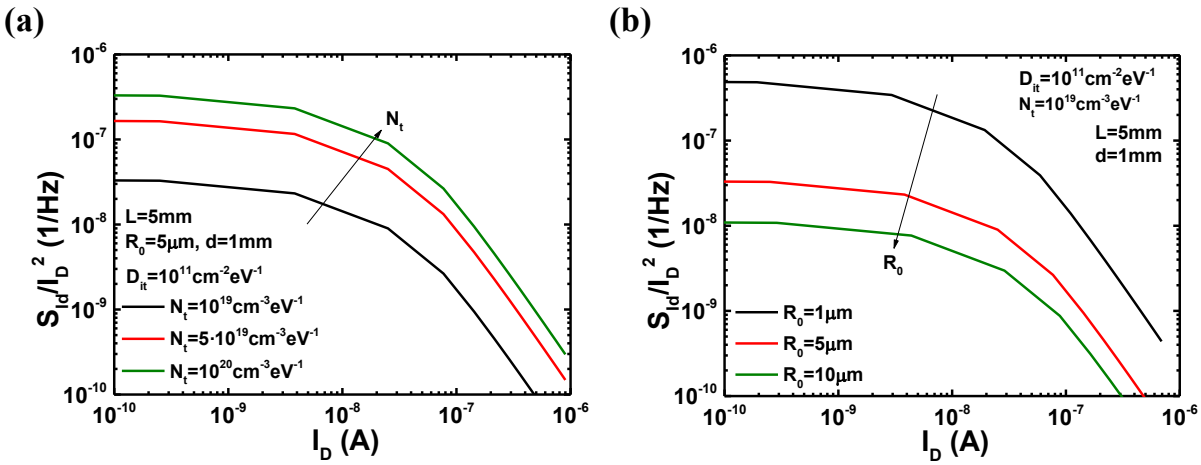

Figure V-16: Computed S_{Id}/I_D^2 versus drain current for different N_t (a) and R_0 (b) values.

Figure V-17a shows the AFM image of tip crater on non-passivated silicon surface. The vertical cross section taken at the line in Figure V-17a is presented in Figure V-17b. The probes leave a trace on the silicon surface with radius ≈ *5-6 μm*. In reality, however, the effective contact dimensions should probably take into account the irregular tip penetration depth (Figure V-17b). This is more complicated to evaluate. For simplicity reasons, we assume R_0 to be given by the crater radius on the surface, and we will perform the main comparisons with the experimental trends using $R_0 = 5\ \mu m$.

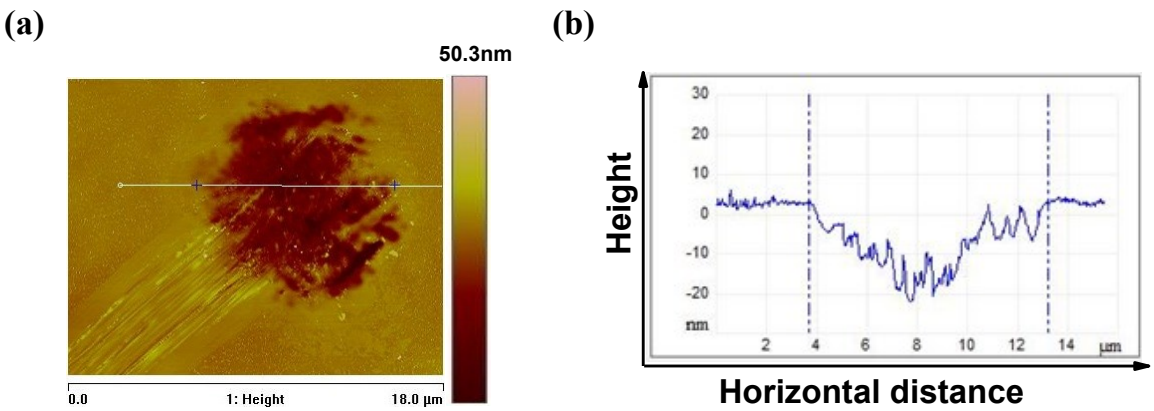

Figure V-17: (a) AFM image of tip crater on non-passivated SOI surface. The corresponding vertical cross section taken at half of the crater (line in Figure V-17a) is shown in Figure V-17b. Note the irregular probe penetration in the silicon surface.

Impact of interface quality

It is known from the literature [83] that passivated and non-passivated top silicon surface have different density of defects placed at the interfaces. Thus, not only N_t will change, but also the fast traps D_{it}, which determine the subthreshold swing.

Figure V-18a shows the computed S_{Id}/I_D^2 versus I_D for different N_t and D_{it}. In this case, the fast and slow traps are directly related by $D_{it} = \lambda \cdot N_t$. The lowest plateau is achieved for $N_t = 10^{18} cm^{-3} eV^{-1}$. The increase of the defects density ($N_t = 10^{19} cm^{-3} eV^{-1}$) leads to higher plateau position. $N_t = 10^{20} cm^{-3}\ eV^{-1}$ represents the largest amount of defects, hence we would expect the highest S_{Vfb} magnitude. This is not the case because the D_{it} variation also induces a shift of the current PSD. Figure V-18b shows the corresponding $(g_m/I_D)^2$ versus drain current for the same structure. The larger the D_{it} value, the lower the plateau position. As a result, the S_{Vfb} increase proportional to N_t is masked on the S_{Id}/I_D^2 characteristics by D_{it} effects, confirming the importance to analyze the S_{Vfb} spectrum instead of S_{Id}/I_D^2.

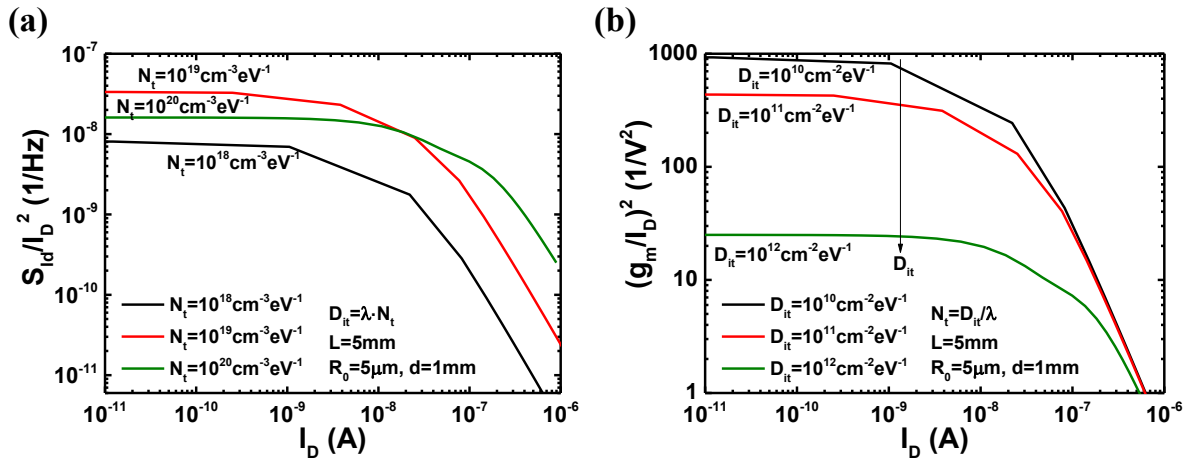

Figure V-18: (a) Computed S_{Id}/I_D^2 versus I_D for different N_t values. The calculations were performed using $D_{it} = \lambda \cdot N_t$. The corresponding $(g_m/I_D)^2$ as a function of drain current is shown in Figure V-18b. In this case the characteristics represent only the static contribution, thus N_t has no impact.

Impact of inter-probe distance and die area

The experimental results presented in Figure V-13 and Figure V-14 showed only small variations of the measured S_{Id}/I_D^2 with the inter-probe distance d and die surface. Figure V-19 presents the computed S_{Id}/I_D^2 versus I_D in case of different inter-probe distances (a) and die surfaces (b). A slight decrease of plateau height is observed for higher d. In case of experimental results (Figure V-13), reproducibility problems due to the use of different needles may have masked the trend.

Furthermore, the variation of the die surface has almost no effect on the characteristics (Figure V-19b). Both parameters, d and S, play a secondary role in LF-noise of Ψ-MOSFET, as confirmed by simulations and experiments.

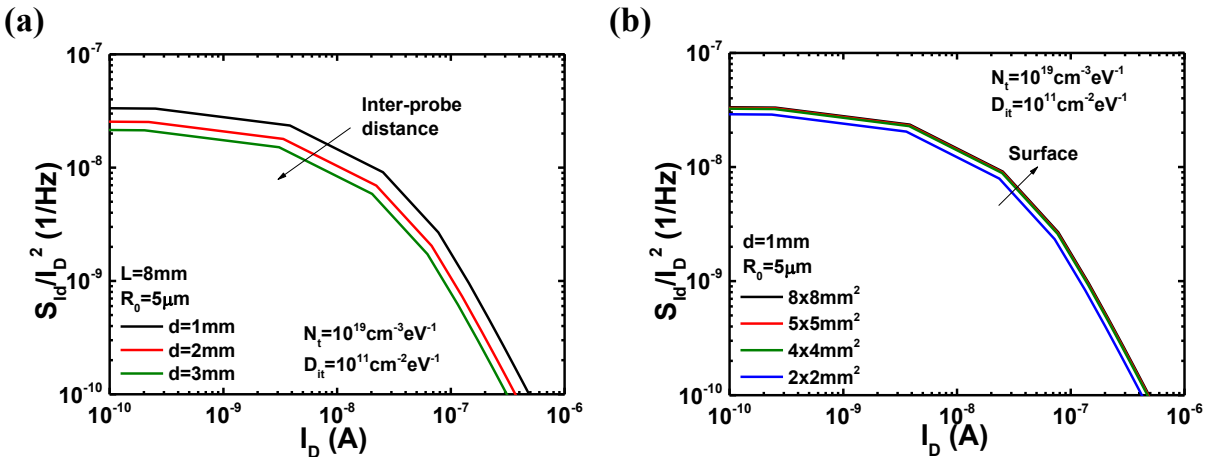

Figure V-19: Computed S_{Id}/I_D^2 versus drain current in case of different inter-probe distance (a) and die area (b).

V.4 Effective surface in LF-noise

The experimental and computed results clearly show that the geometry (inter-probe distance or die area) is not relevant for LFN. Where is the noise really coming from in this case?

We investigate the region where most of LF-noise is generated (effective surface, S_{eff_LFN}) in Sec. V.4.1 and quantified it in Sec. V.4.2.

V.4.1 Why an effective surface?

Figure V-20 shows the whole die area (dashed line) computed as a function of L (die length of square die). S_{eff_LNF} is calculated with Eq. (V.22) and added to the graph (line). A huge difference between S and the effective surface is found. Figure V-20 proves that the LNF signal measured in the silicon film is generated in a reduced region which is much smaller than S (*2* to *3* orders in magnitude difference). This explains why the inter-probe distance and especially the die surface variation have almost no impact on the obtained characteristics.

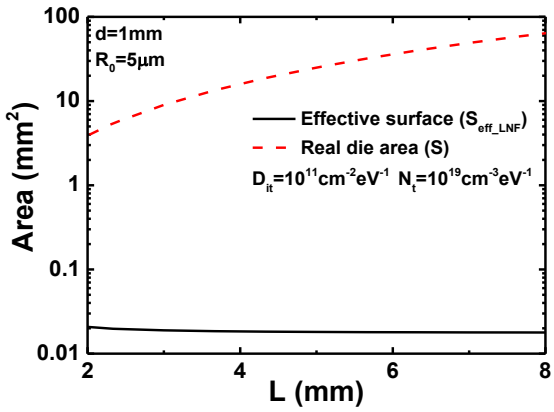

Figure V-20: Calculated whole die area (dashed line) and S_{eff_LNF} (line) versus die length.

The detailed explanation is given in Figure V-21a, where the distribution of the current power density ($\sigma \cdot \xi^2$) on the silicon surface is shown. In order to enhance the effects, small sample surface (*2 mm* x *2 mm*) and large probe radii (R_0 = *200 µm*) were used. Most of the LFN signal arises from the regions around the two contacts where the power current density is localized. Consequently, for LFN in Ψ-MOSFET, only a small percentage of the silicon surface delivers most of the S_{Id}/I_D^2 signal. Figure V-21b presents the current density ($\sigma \cdot \xi$) distribution for the same sample. Contrary to the LFN distribution, $\sigma \cdot \xi$ is much more homogenous over the whole die area, confirming that I_D-V_G characterization is less sensitive to the region around the contacts.

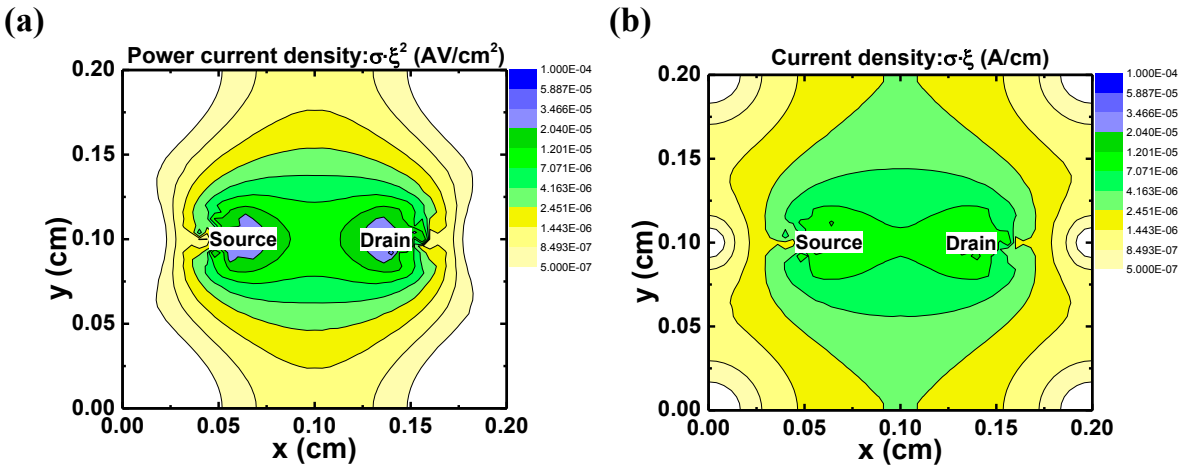

Figure V-21: Power current density (a) and current density (b) computed on the same die. The sample surface was *2 mm x 2 mm* and $R_0 = 200\ \mu m$. The unnatural behavior at the edges of the structure is due to border effects coming from meshing.

V.4.2 Quantification of effective surface

In order to quantify the surface which dominates the noise (S_{Id}/I_D^2), we compared the total LFN with the signal obtained from two reduced regions. The structure used is represented in Figure V-22a. Two corona surfaces with ΔR_0 thickness were added around the source and drain contacts. The corresponding "*reduced noise*" $S_{Id}/I_{D_red}^2$ is calculated dividing the LFN obtained only from these regions by the whole drain current I_D. Figure V-22b shows $S_{Id}/I_{D_red}^2$ divided by S_{Id}/I_D^2 versus ΔR_0. In case of $R_0 = 5\ \mu m$, more than *80 %* of the whole signal is concentrated in less than *10 µm* distance from the contact edges. This result underlines that the LFN noise is localized around the source and drain; the use of sharp probes enhances the effect.

Moreover, the "*reduced noise*" for fixed radius is exponentially dependent on the thickness of the corona structure ΔR_0:

$$\frac{S_{Id}}{I_{D_red}^2} = \frac{S_{Id}}{I_D^2}\left(1 - e^{\frac{-\Delta R_0}{R_0/2}}\right) \qquad \text{(V.26)}$$

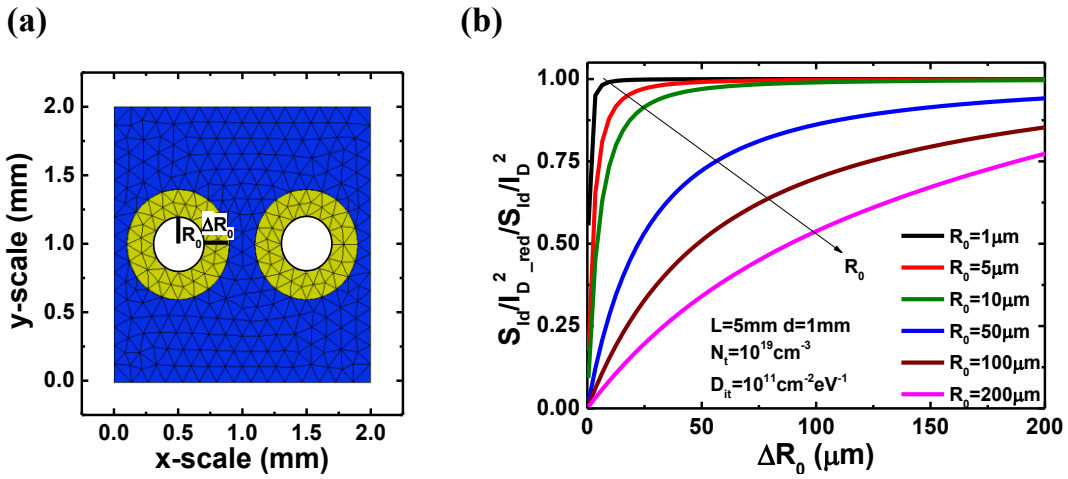

Figure V-22: (a) Mesh for the computation of LFN with contact radius R_0. A second region with radius $R_0 + \Delta R_0$ is added around the source and drain to measure the localized LFN ($S_{Id}/I_D^2{}_{red}$). (b) Relative ($S_{Id}/I_D^2{}_{red}$)/(S_{Id}/I_D^2) versus ΔR_0 for different contact radius.

Using Eq. (V.22) it is possible to compute S_{eff_LFN} as a function of ξ on the Si film for different R_0. S_{eff_LFN} versus R_0 is shown in Figure V-23 for four different die surfaces: *2 mm* x *2 mm*, *4 mm* x *4mm*, *8 mm* x *8 mm* and *16 mm* x *16 mm*. In case of very small die area (*2 mm* x *2 mm*), border effects limit the analysis.

The effective surface is directly proportional to R_0 in case of sharp probes (*region A*). Thus, a small variation of the probe radius will strongly affect the obtained LFN signal (*i.e.*, variation of tip crater). This explains the important S_{Id}/I_D^2 shift obtained using different probes (see Figure V-8). The use of large contacts leads to constant S_{eff_LFN} magnitude (*region B*) independent of R_0. Thus, S_{Vfb} extraction will be less related to the probe diameter and therefore relevant for substrate characterization. After a preliminary calibration to determine the effective surface, continuous monitoring could be performed on samples using always the same probes.

One of the main conclusions of this section is that the obtained LF-noise arises from localized regions around the source and drain contacts and the effective area S_{eff_LFN} is much smaller than S. This explains why the N_t calculated using S (Eq. (V.12)) had such unrealistic, overestimated values.

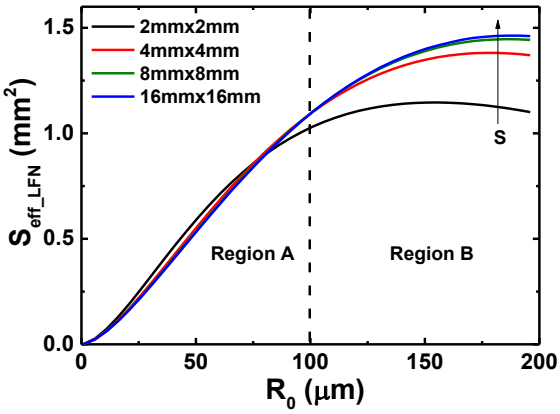

Figure V-23: S_{eff_LFN} versus R_0 for different die areas.

V.5 Probe penetration effects

After proving that the LFN mostly arises from small regions localized around the probe contacts (S_{eff_LFN}), some questions still remain:

- Is the noise related to defects generated by probe penetration in the Si film?
- Is the LFN in pseudo-MOSFET configuration sensitive to the sample quality?

Experimental results in Sec. V.5.1 and calculations with FlexPDE® (Sec. V.5.2) will try to answer these questions.

V.5.1 Experimental evidences

HF treatment

We still need to understand if the measured signal is related to the interface defects or not. S_{eff_LFN} proved that for sharp probes, as in our case, the signal arises from small regions around the source and drain contacts. Quantifying the effective surface is quite complicated for small R_0. From the practical point of view it was possible to imagine an experiment in which everything related to the probe contacts is fixed while the samples have a variation of the interface quality.

This is achieved by the use of a sample after HF treatment. The native oxide of non-passivated wafer plunged in *HF* solution (diluated at *5 %*) is etched of. The native oxide grows back within hours until the surface will become stable again. Thus, the top interface traps density changes during the re-oxidation [63].

LF-noise was performed on this sample at different moments after etching. The probes were initially placed on the surface of the die and not moved during the tests. This allows assuming that the contacts and thus the effective surface are the same for all the measurements.

Figure V-24a shows the evolution in time $I_D(V_G)$ curves. The corresponding V_T, subthreshold swing and D_{it} (extracted from I_D-V_G) are reported in Table V-3. Clear variations of both quantities are detected. Immediately after the treatment many free carriers and dangling bonds are present on the top silicon surface [63], inducing strong V_T lowering and poor subthreshold slope. The regrowth of the native oxide gradually attenuated these effects: a V_T shift is measured, accompanied by subthreshold swing improvement. LFN characterization was performed in parallel and S_{Id}/I_D^2 versus drain current curves are shown in Figure V-24b. A general overlap between the curves is observed. Contrary to static characterization, no appreciable variation of the curves in time is found. LFN is clearly "*blind*" to this evolution of the top surface.

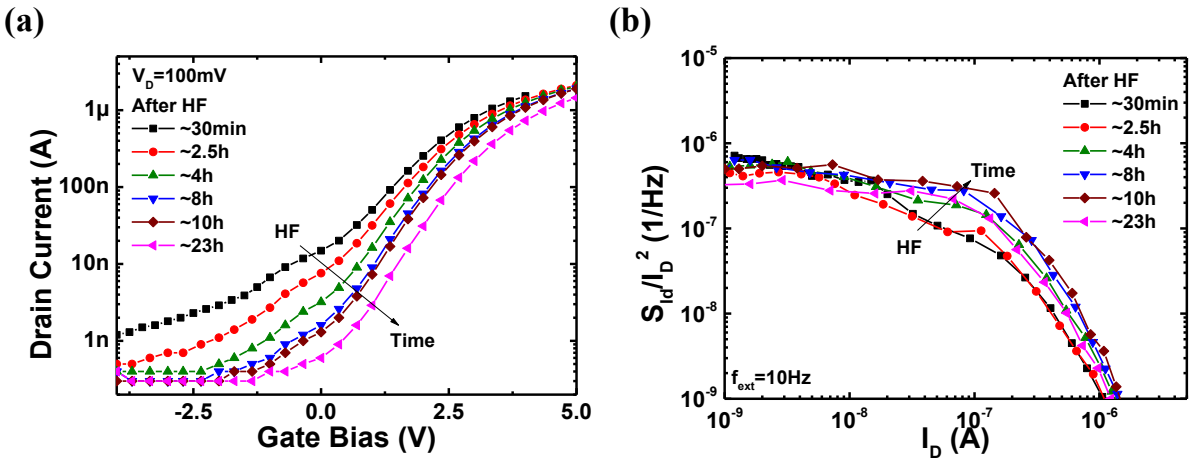

Figure V-24: (a) Drain current versus gate bias performed at different moments after HF treatment. The corresponding S_{Id}/I_D^2 as a function of I_D are shown in Figure V-24b. Non-passivated SOI structure with *88 nm* thick top silicon film and *145 nm* thick BOX.

Time after end of HF process	V_T (V)	S_s (V/dec)	D_{it} ($cm^{-2}eV^{-1}$)
~30min	1.5	1.5	$4.4\cdot10^{12}$
~2.5h	2	1.4	$4\cdot10^{12}$
~4h	2.1	1.2	$3.6\cdot10^{12}$
~8h	2.3	1.1	$3.4\cdot10^{12}$
~10h	2.4	1.1	$3.3\cdot10^{12}$
~23h	2.5	1.0	$3.1\cdot10^{12}$

Table V-3: V_T and subthreshold swing extracted from Figure V-24a. The corresponding D_{it} values are obtained using Eq. (II.10), as for MOSFET.

To complete the analysis, Figure V-25 shows the computed S_{Vfb} versus drain current immediately after the HF treatment (fully symbols) and when the top surface started to stabilize after *23* hours (empty symbols). The differences at low I_D magnitude are due to the effects of traps only present in the static characteristic and not on the S_{Id}/I_D^2 spectrum (D_{it} and not N_t, see the differences in Figure V-24a and the overlap in Figure V-24b). For higher drain current values, the two curves show similar S_{Vfb} values. Thus, the HF treatment does not affect N_t but only the fast traps (D_{it}), as evidenced in Table V-3.

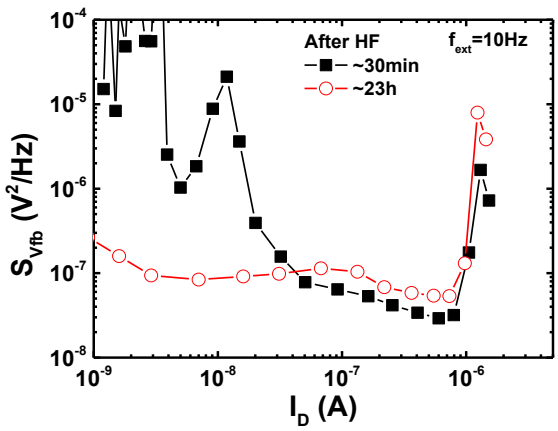

Figure V-25: S_{Vfb} computed form Figure V-24 versus drain current immediately after the HF treatment (plain symbols) and after surface stabilization (empty symbols).

Charging procedure

Since the re-oxidation was not visible by LFN, a possibility to modify the quantity of slow traps present on SOI wafer could be the charging procedure discussed in case of QST measurements (see Sec. IV.6).

Figure V-26a presents the drain current versus V_G before (plain symbols) applying V_G of *10 V* for *3000 s*. The characterization was repeated after the end of the procedure (empty symbols). The filled traps induce a V_T shift of about *0.4 V*. Furthermore, the subthreshold swing remains almost constant: *0.61 V/dec* before charging and *0.613 V/dec* after it. The corresponding detected noise signal versus I_D is shown in Figure V-26b. Before charging (plain symbols), the S_{Id}/I_D^2 plateau is lightly higher than after it (empty symbols).

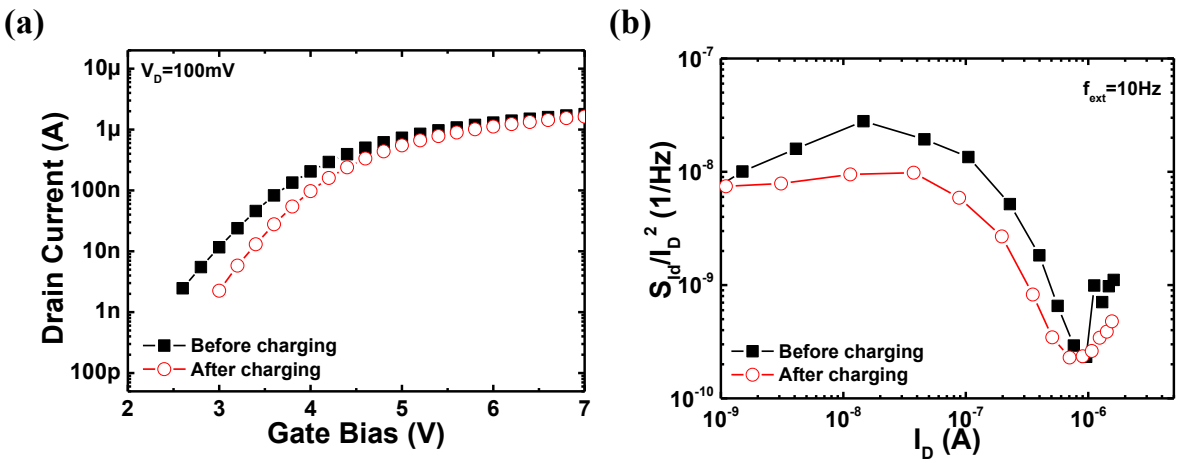

Figure V-26: Drain current as a function of gate bias (a) and S_{Id}/I_D^2 versus I_D before (plain symbols) and after (empty symbols) charging procedure. Characteristics performed without moving the probes. The same SOI structure as in Figure V-24 was used.

To remove any possible impact due to D_{it} (fast traps), Figure V-27 shows the corresponding S_{Vfb} computed as function of drain current. The flat-band voltage power spectrum is higher before charging procedure (plain symbols) than after it (empty symbols). One expects an increase of the N_t density after charging, while a light decrease is obtained. One possibility to explain the phenomenon is that the charged defects are "*masked*" during the analysis. They require long time to release the captured electrons, thus they will not respond to the applied input, if they are still filled … or, again, the LFN is actually not sensitive to what is happening in the sample.

These two tests (HF clean and charging procedure) show that even if the impact of effective surface was experimentally stabilized, the signature due to interface quality is too small to be convincing. The parameter which seems to mostly impact the experiments is explained in the next section.

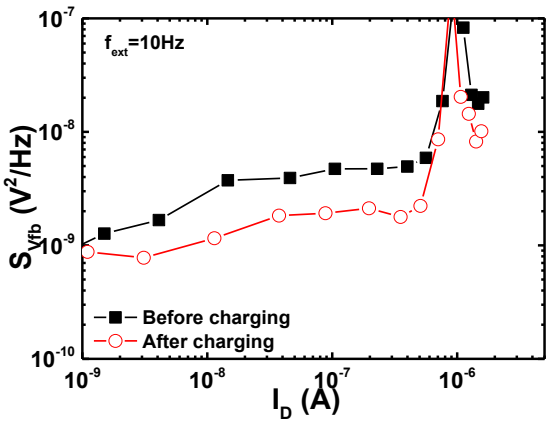

Figure V-27: Computed S_{Vfb} versus drain current before (plain symbols) and after (empty symbols) charging procedure. The data shown in Figure V-26 was used.

V.5.2 Computation of induced defects by probe penetration

A possible explanation of the measured trends is given by the study of the defects induced by probe penetration in the silicon film. In order to investigate this phenomenon, we used the same structure presented in Figure V-22a. Localized defects (N_{t_added}) were added only in the corona regions between R_0 and ΔR_0, to mimic the supplementary defects generated by needle penetration inside the film. The whole LF-noise signal ($S_{Id}/I_D^2{}_{_tot}$) will be the sum of the noise term arising from the silicon film (S_{Id}/I_D^2) and the contribution of the defects due to the probe penetration: $S_{Id}/I_D^2{}_{_red}$. Figure V-28a shows the computed $S_{Id}/I_D^2{}_{_tot}$ as a function of drain current for different N_{t_added} magnitudes. $D_{it} = 10^{12} cm^{-2}eV^{-1}$ and $N_t = 10^{20} cm^{-3}eV^{-1}$ were used. The contact radius was $5\ \mu m$, while $\Delta R_0 = 500\ nm$. It is noted that an increased density of defects induced by probes leads to higher LFN plateau. This means that the interface trap density extracted from the plateau value is not representative of the actual density of traps in the SOI material (here $D_{it} = 10^{12}\ cm^{-2}eV^{-1}$). For example, N_t is oversestimated by $173\ \%$ for $N_{t_added} = 10^{21}\ cm^{-2}eV^{-1}$.

Figure V-28b presents the total noise power spectral density S_{Id}/I_D^2 and its componets versus N_{t_added}. The continuous horizontal line shows the genuine LFN spectrum without tip induced defects ($N_{t_added} = 0$) in case of $N_t = 10^{19} cm^{-3}eV^{-1}$ and $N_t = 10^{20} cm^{-3}$, respectively. $S_{Id}/I_D^2{}_{_red}$ term increases linearly with the density

of added defects (dashed line). The total signal $S_{Id}/I_D^2{}_{tot}$ (dotted line) cumulats the two sources of noise. $D_{it} = \lambda \cdot N_t$ was used in both cases. For small density of probes induced defects, $S_{Id}/I_D^2{}_{tot}$ is dominated only by the noise arising from the silicon film. Large N_{t_added} magnitude, however, completely masks the contribution of the native interface traps of the sample ($S_{Id}/I_D^2{}_{tot} \approx S_{Id}/I_D^2{}_{red}$).

Considering $N_t = 10^{20} cm^{-3} eV^{-1}$, $S_{Id}/I_D^2{}_{red}$ dominates the whole LFN signal for higher N_{t_added} than for low density of traps present on the SOI structure ($N_t = 10^{19} cm^{-3} eV^{-1}$). Thus, in higher quality passivated substrates, the LFN is probably more probe damage related than for the non-passivated ones (low quality of top silicon interface).

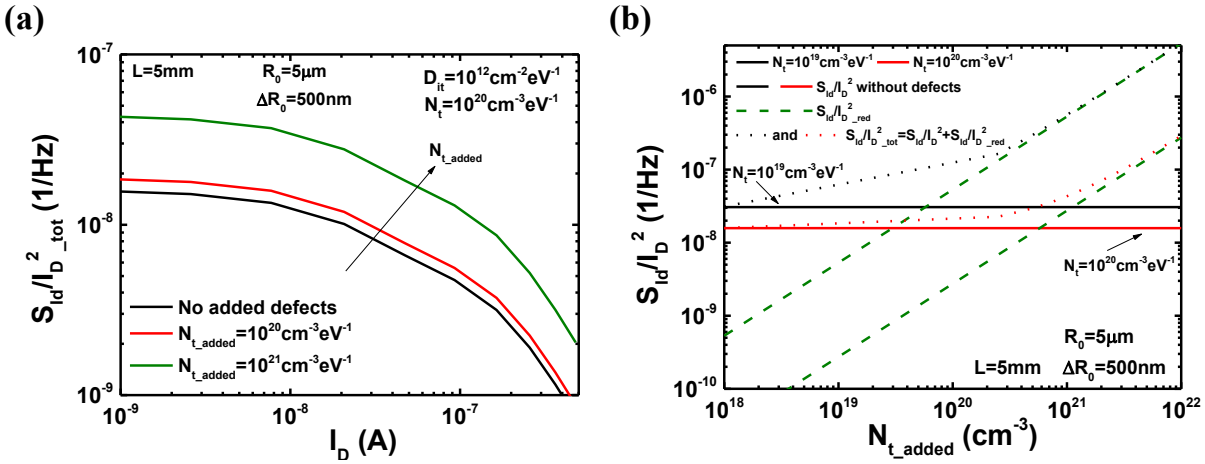

Figure V-28: (a) The total $S_{Id}/I_D^2{}_{tot}$ versus I_D obtained from the Si film when different induced defects densities N_{t_added} were added around R_0. (b) S_{Id}/I_D^2 is traced as function of N_{t_added} in two different configurations: $N_t = 10^{19} cm^{-3} eV^{-1}$ (black line) and $N_t = 10^{20} cm^{-3} eV^{-1}$ (red line). The noise power spectrum only due to N_{t_added} term is also shown (dashed line). $S_{Id}/I_D^2{}_{tot}$ is computed versus N_{t_added} for both N_t cases (red dotted line): $S_{Id}/I_D^2{}_{tot} = S_{Id}/I_D^2 + S_{Id}/I_D^2{}_{red}$.

As shown in Sec. V.4.2, higher R_0 radius might stabilize S_{eff_LFN}. It is also known from the literature that larger tips induce a smaller amount of defects on the SOI structure [62].To further evaluate this solution, Figure V-29 presents relative contribution $(S_{Id}/I_D^2{}_{red})/(S_{Id}/I_D^2{}_{tot})$ and $(S_{Id}/I_D^2)/(S_{Id}/I_D^2{}_{tot})$ versus contact radius for two different probe induced defects density: $N_{t_added} = 10^{20} cm^{-3} eV^{-1}$ (continuous line) and $N_{t_added} = 10^{21} cm^{-3} eV^{-1}$ (dashed line). The impact of the generated defects is very strong but it exponentially decreases as a function of needle radius. In case of $N_{t_added} = 10^{20} cm^{-3} eV^{-1}$ (line), using very large contacts (*i.e.*, $R_0 \approx 100\ \mu m$ - $200\ \mu m$) the contribution due to induced defects is almost negligible ($(S_{Id}/I_D^2{}_{red})/(S_{Id}/I_D^2{}_{tot})$ term tends to 0). Unfortunately, high N_{t_added} (dashed line) still dominates the whole LF-noise signal also in case of large R_0, making the interface quality characterization not possible.

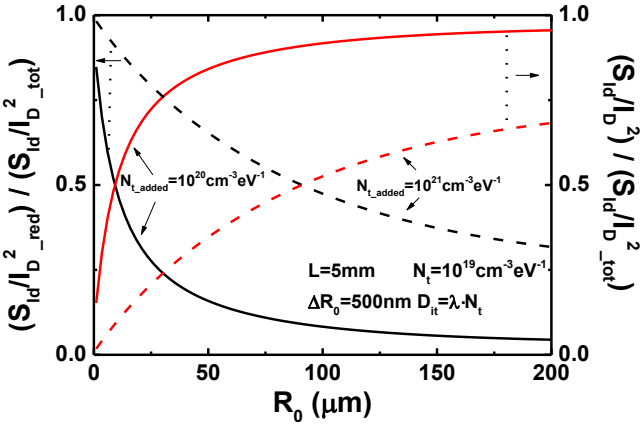

Figure V-29: $(S_{Id}/I_D^2{}_{red})/(S_{Id}/I_D^2{}_{tot})$ **and** $(S_{Id}/I_D^2)/(S_{Id}/I_D^2{}_{tot})$ **versus** R_0 **for** $N_{t_added} = 10^{20}cm^{-3}eV^{-1}$ **(line) and** $N_{t_added} = 10^{21}cm^{-3}eV^{-1}$ **(dashed line).**

V.6 Conclusions and perspectives

In this chapter, a detailed investigation of low-frequency noise in pseudo-MOSFET was performed. The aim was to explain the abnormally large D_{it} values previously extracted by LFN in Ψ-MOSFET.

We discussed about the improvements due to the use of vacuum system and we demonstrated that the geometry of the sample has little importance, while the probes have a high impact on the experiments.

A physical model was proposed to explain the LFN in a material in case of inhomogeneous current flow. Simulations were performed and good agreement between experimental and computed trends was found. It was proved that the noise signal arises from small surface localized around the contacts and this is why it is mostly independent of the whole die area or inter-probe distance.

Obviously, this small surface is mostly determined by the probe. The needle radius R_0 plays a major role for LF-noise characterization. Furthermore, the impact of defects induced by probe penetration was studied. It was extensively discussed that using standard Jandel® station with needle radius of *40 μm*, the obtained S_{Id} signal is almost independent of the quality of the SOI wafer; the defects induced by the probes dominate the whole detected noise, making the LFN characterization not suitable for interface monitoring.

Using particular precautions it could be possible to increase the sensitivity of noise analysis to the SOI interfaces. Two possible approaches can be envisaged:

- The use of larger probe sizes ($R_0 \approx 150\ \mu m$- $200\ \mu m$) makes S_{eff_LFN} almost constant and the noise signal will be less localized around the contacts. Furthermore, the needles will less penetrate into the silicon film. This should induce less defects [62] and the signal due to N_t might be revealed.
- Perform low-frequency noise in *4*-probe configuration. This technique should decrease the impact of contacts and make visible the contribution due to the interface defects.
- The LFN technique may be used to characterize the contact between the probe and the silicon film leading to a better knowledge of defects induced by tips penetration.

Chapter VI:

General conclusions and perspectives

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VI.1 Conclusions

The pseudo-MOSFET is a powerful measurement method for the characterization of bare SOI wafers [47]. Several studies pointed out the capability to extract carrier mobility, oxide defects and interface quality using static I_D-V_G analysis [48], [49], [62], [160]. However, this measurement shows limits for the material characterization [33], [68], especially for advanced SOI substrates with ultra-thin silicon film. Consequently, new techniques were developed. For example, low-frequency noise measurements were performed in Ψ-MOSFET by Diab *et al.* [55], but the obtained values of interface state density were not convincing. The effective carrier mobility was successfully extracted using split-CV technique [53], [54]. Nevertheless, the method needed a fitting parameter named effective surface, that was not clearly explained. Furthermore, capacitance measurements were not extended for D_{it} extraction.

In this thesis, we addressed same of these opened topics and we enriched the characterization methods of bare SOI substrates. Starting from the well-known static I_D-V_G analysis, three other techniques were discussed, from both experimental and modeling point of view: split-CV, quasi-static capacitance and low-frequency noise. The main results can be summarized by *3* topics: improved measurement setup, effective surface and D_{it} extraction.

Improved measurement setup

We proved that a good measurement setup increases the robustness of the characterization technique, leading to more stable analysis. Note that in Ψ-MOSFET, the critical setups are not the same for all the measurement techniques.

In case of capacitance analysis (split-CV and quasi-static CV), the quality of the back contact between the substrate and the metallic chuck is the major parameter. The use of vacuum system leads to stable characteristics and avoids parasitic capacitance contributions. The adjustable pressure probes play only a minor role. Hence, the possibility to characterize also ultra-thin silicon films and BOX using capacitance analysis makes the technique very promising for the quality monitoring of bare SOI wafers.

The opposite situation was found for the techniques based on drain current measurements (static I_D-V_G and LFN): here the probes have a dominant role on the experimental characteristics. The use of vacuum for the back contact, even if not critical, is highly recommended in order to attenuate the effect of parasitic terms. The vacuum becomes mandatory in case of ultra-thin SOI structures.

Additionally, in case of low-frequency noise the probes have a supplementary role because they induce defects in the silicon film increasing the measured D_{it}. Reproducible analysis requires systematic precautions.

The Ψ-MOSFET setup was also used for III-V layers where we found that the probe material is critical.

Effective surface

One of the main problems of the standard pseudo-MOSFET configuration is that the conduction channel is not well defined, as for fabricated transistor. The actual geometry responsible for a measured signal (drain current, LFN, capacitance) was investigated and we proved that the effective areas were not the same from one technique to another.

Thanks to the use of improved setup and to modeling studies, we demonstrated that in capacitance measurements the whole die area responds during the characterization. This means that border effects are not present.

As for I_D-V_G measurements, the current density is more localized and the width over length ratio of Ψ-MOSFET is classically defined by f_G [47]. Note that placing the source and drain probes too close to the edge of the device, the electrical field distribution on the silicon surface is limited by the die borders and f_G is modified. To obtain correct mobility values, the probes must be placed in the middle of the tested die.

For LFN, we proved that the signal mostly arises from small regions surrounding the probes, and this effect is enhanced for sharp tips (as the ones we were using). In order to perform suitable D_{it} extraction, the effective surface must be computed using the physical model discussed in Sec. V.4.2.

D_{it} extraction

Static I_D-V_G characterization leads to interface traps evaluation. However, its capability is more limited as the thickness of the silicon film decreases. For this reason we investigated other techniques for D_{it} characterization.

Unfortunately, we proved that the LFN signal is mostly affected by the defects induced by the probes and almost independent of the material quality. Larger probes could allow overcoming this issue.

Furthermore, even if capacitance measurements performed using LCR meter lead to correct effective mobility values, information concerning the quality of the interfaces is masked by the RC time constant of the channel (τ_{RC}). τ_{RC} is associated to the time needed for the carriers to go from the probes to any point in the conduction channel. The minimum measurement frequency ($f = 20\ Hz$) was not slow enough to avoid τ_{RC} effects because of large die areas ($S \approx 4\text{-}60\ mm^2$). Consequently, neither capacitance-voltage nor conductance technique could reveal D_{it} signature.

The problem was solved using quasi-static capacitance measurements, which we introduced for the first time in the Ψ-MOSFET configuration. Performing very slow analysis, the signature of deep traps was detected. A physical model was derived and validated for different measuring frequencies and temperatures. A simple extraction procedure was proposed. Its validity, limitations and extensions were addressed from a practical point of view. Several SOI geometries and surface qualities were tested. In samples with passivated top surface, the obtained D_{it} profiles overlapped, independently of the top silicon film and BOX thicknesses, proving that the measurements mainly reflect the quality of film-BOX interface. In non-passivated samples, larger density of defects was measured. D_{it} peaks at precise energy values were found for non-passivated top surface.

VI.2 Perspectives

In this thesis, we answered some critical questions concerning the split-CV or LFN technique, we introduced the QSCV technique in Ψ-MOSFET and we characterized a variety of SOI films and also III-V layers. However, some aspects need further investigation:

- The setup improvements (quality of back contact) open the way for other new techniques in Ψ-MOSFET configuration, such as charge pumping or the analysis of transitory phenomena.
- The impact of substrate capacitane has to be investigated for measurements performed using vacuum contact. This term can play a role for static I_D-V_G analsysis and capacitance measurements.
- Other passivated samples can be tested using QSCV technique in order to investigate the impact of the crystal orientation and better separate the contributions due to the several interfaces.
- The D_{it} profile measured using QSCV in non-passivated samples requires deeper investigation, especially for UTBB structures (tests of charging procedure for samples with $t_{OX} = 25\ nm$).
- The use of *4*-probes configuration or larger needles could make the LFN technique suitable also in Ψ-MOSFET configuration.
- The low-frequency nosie can be a fruitful technique for the characterization of the contact between the pressure probes and the silicon film. For sharp tips, the signal is mostly determined by defects induced by probe penetration. Thus, its analysis may enrich the knoldge about source and drain contacts.
- The III-V materials clearly represent a possible future for microelectronics. The material characterization is challenging. The standard I_D-V_G in Ψ-MOSFET configuration did not work, probably because of contact problems. However, the low dependency on the probe penetration makes QSCV a promising technique for D_{it} extraction in III-V layers.

… but I leave all these topics to the next generation of students.

Appendix I

During this thesis, the Hall mobility (μ_{Hall}), the material resistivity (ρ) and the active doping concentration (N_D or N_a) were measured on a "*home-made station*", totally dedicated to these experiments [6]. The setup is made of a probe station that can be placed inside a magnetic coil. All the tools required for the characterization (amperometers, voltemeters, etc.) are controlled by computer. The whole experiment consists of three consecutive steps:

1 Contact tests: these tests are required to verify if the contacts between the metallic probes and the material are ohmic. If this is not the case, all the other measurements are useless. A current is applied between two contacts and the corresponding voltage is measured. Linear I-V dependency must be obtained to pursue the characterization;

2 The Van Der Pauw measurement is performed to obtain the material resistivity ρ;

3 Hall effect measurement leads to the Hall mobility μ_{Hall}. The active doping concentration is computed at the end of the characterization, using μ_{Hall} and ρ.

The next two sections describe the working principle of Van Der Pauw and Hall effect measurements.

Van Der Pauw experiments

In order to perform Van Der Pauw measurements, the sample is placed on a metallic chuck and four manual probes (labeled *1*, *2*, *3* and *4*) are used to contact it. Figure AI-1 shows an example. To succeed the characterization, the tested material must have an uniform thickness.

The measurement is performed setting the current between two adjacent probes (for example between probes *1* and *2*) and measuring the potential drop between the two others (V_{34}) (see Figure AI-1a). The corresponding resistance can be computed as:

$$R_{12,34} = \frac{V_{34}}{I_{12}} \tag{AI.1}$$

In order to average the obtained resistance value and to reduce effects due to a not perfectly symmetric sample geometry, other measurements are performed shifting the contacts by a quarter turn (see Figure AI-1b). $R_{23,41}$ is obtained. The material resistivity is computed as a function of the film thickness (t_{Si}):

$$\rho = \frac{\pi \cdot t_{Si}}{\ln(2)} \cdot \frac{R_{12,34} + R_{23,41}}{2} \cdot f_{conf} \tag{AI.2}$$

where f_{conf} is a configuration coefficient given by [6]:

$$2 \cdot \exp\left(-\frac{\ln(2)}{f_{conf}}\right) \cdot \cosh\left(\frac{R_{12,34}/R_{23,41} - 1}{R_{12,34}/R_{23,41} + 1} \cdot \frac{\ln(2)}{f_{conf}}\right) = 1 \tag{AI.3}$$

In case of perfectly symmetrical samples ($R_{12,34} = R_{23,41}$), $f_{conf} = 1$. To increase the accuracy of the analysis, the procedure is repeated injecting the currents I_{34} and I_{41} and measuring the corresponding voltages V_{12} and V_{23}. The final resistivity value results from averaging all the obtained ρ.

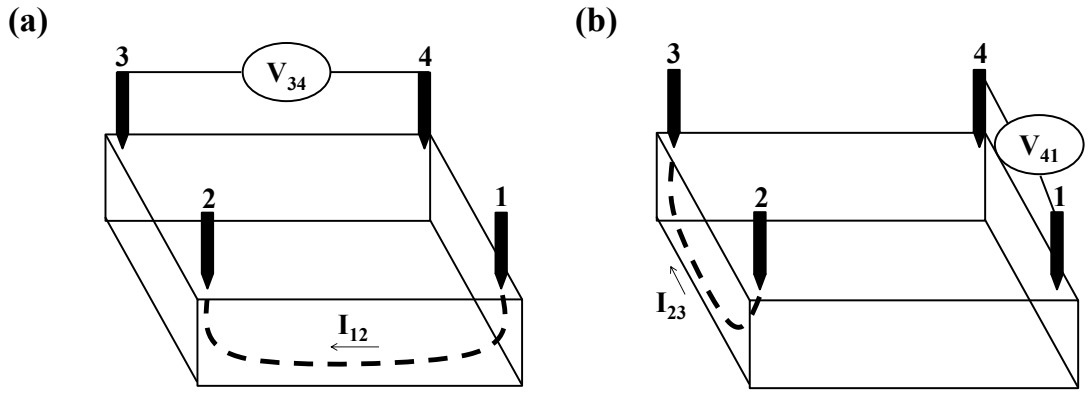

Figure AI-1: Schematic of Van Der Pauw measurement. The current I_{12} (a) and I_{23} (b) are injected and the voltage V_{34} and V_{41} are measured, respectively.

Hall effect measurement

For the Hall effect measurements, the same sample used during Van Der Pauw characterization is gently moved into the center of a magnetic gap. *0.5 T* are applied perpendicular to the die surface (+*B*). The field direction can also be reversed (-*B*) (see Figure AI-2). The current is set between two diagonal probes and the potential drop is measured between the two other needles.

In a practical case the current is applied between the probes *1* and *3* (I_{13} if the current is inject in *1* while I_{31} if it is reversed) while the tips *2* and *4* are used to measure the potential (V_{24}). Four different voltage values can be obtained changing current and magnetic field direction: $V_{24}(I_{13},+B)$ where the current is injected in *1* and the applied magnetic field is +*B*; $V_{24}(I_{31},+B)$ where the current is reversed (I_{31} instead of I_{13}) and the magnetic field direction is kept constant; $V_{24}(I_{13},-B)$ and $V_{24}(I_{31},-B)$ where the same characterizations are repeated using I_{13} and I_{31} but he magnetic field applied is reversed (-*B*). Hence, the corresponding Hall voltage is:

$$V_{H,24} = \frac{V_{24}(I_{13},+B) - V_{24}(I_{31},+B) + V_{24}(I_{31},-B) - V_{24}(I_{13},-B)}{4} \qquad \text{(AI.4)}$$

Knowing the current direction, the sign of $V_{H,24}$ allows to determine the doping type of the material. The Hall voltage $V_{H,24}$ and Hall current I_H (average between I_{31} and I_{13}) lead to the calculation of the Hall coefficient [6]:

$$R_{H,24} = -\frac{V_{H,24} \cdot t_{Si}}{I_H \cdot B} \qquad \text{(AI.5)}$$

To improve the measurement accuracy, the procedure is repeated injecting the current between *2* and *4* contacts (I_{24} and I_{42}) and measuring V_{31}. The average of all the obtained results leads to Hall coefficient R_H. R_H and the material resistivity ρ (obtained from Van Der Pauw technique) allow the calculation of the Hall mobility [6]:

$$\mu_{Hall} = \frac{|R_H|}{\rho} \tag{AI.6}$$

In conclusion, the doping concentration is computed by:

$$N_{D,a} = \frac{1}{q \cdot \mu_{Hall} \cdot \rho} \tag{AI.7}$$

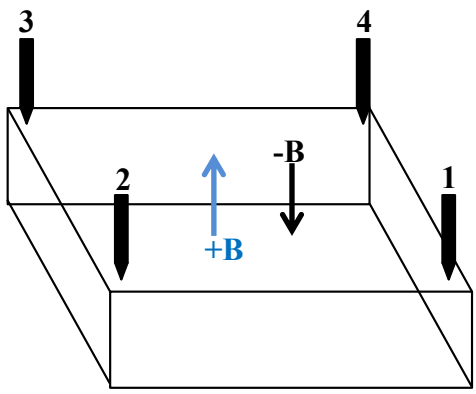

Figure AI-2: Schematic of direct (+*B*) and reversed (-*B*) magnetic field applied on the same structure as in Figure AI-1.

Table of Acronyms

Acronym	Nomination
a.c.	Alternative signal
AFM	Atomic Force Microscope
Al	Aluminum
As	Arsenic
Au	Gold
BOX	Buried oxide
CMOS	Complementary MOS technology
CNF	Carrier number fluctuation (model)
CMF	Carrier mobility fluctuation (model)
d.c.	Constant bias term
div	Divergence
DUT	Device under test
FDSOI	Fully depleted SOI transistor
FET	Field Effect Transistor
FFT	Fast Fourier Transform
Ga	Gallium
Ge	Germanium
grad	Gradient
HgFET	Mercury contacts FET
HF	Hydrofluoric acid
In	Indium
HMF	Hooge mobility fluctuation (model)
InGaAs	$In_{53\%}Ga_{47\%}As$, Indium-Gallium-Arsenide alloy
LFN	Low-frequency noise
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field effect transistor
NBTI	Negative bias temperature instability
Ni	Nickel
NID	Non-intentionally doped
Os	Osmium
PBA	Programmable Biasing Amplifier
PDSOI	Partially depleted SOI transistor
PSD	Power spectral density

Acronym	Nomination
QSCV	Quasi-static capacitance measurements
RC	Resistance – capacitance (model)
RTS	Random telegraph signal
Si	Silicon
SiO_2	Silicon-dioxide
SOI	Silicon-on-insulator
Ti	Titanium
UTBB	Ultra-thin body and buried oxide
WC	Tungsten carbide alloy
III-V	Label for $In_{53\%}Ga_{47\%}As$ layer
III-V-OI	III-V film on insulator
Ψ-MOSFET	Pseudo-MOSFET

Table of Constants

Symbol	Value / Unit (in SI)	Description
k	1.38×10^{-23} m^2 kg s^{-2} K^{-1}	Boltzmann constant
j	-	Complex unit
q	$1.6 \cdot 10^{-19}$ C	Unit charge
v_{th}	10^7 cm/s	Thermal velocity
ε_0	$8.85 \cdot 10^{-12}$F/m^2	Vacuum permittivity
ε_{OX}	$3.9 \cdot \varepsilon_0$ F/m^2	SiO_2 permittivity
ε_{Si}	$11.8 \cdot \varepsilon_0$ F/m^2	Silicon permittivity

Table of Symbols

Symbol	Unit (in SI)	Description
B		
B	T	Applied magnetic field
C		
C_{OX}	F/m^2	Oxide capacitance
C_{Si}	F/m^2	Silicon film capacitance
C_{Inv}	F/m^2	Inversion channel capacitance
C_{GC}	F	Gate-to-channel capacitance
C_{GC_max}	F	Maximum measured C_{GC}
C_{GS}	F	Gate-to-substrate capacitance
C_{m_split}	F/m^2	Measured parallel capacitance for split-CV measurements
C_{max}	F	Measured maximum capacitance in case of Ψ-MOSFET configuration
C_{max_air}	F	Measured maximum capacitance in case of Ψ-MOSFET configuration with air back contact
C_{Dit_c}	F/m^2	Capacitance due to D_{it} in split-CV configuration for continuous energy traps distribution
C_p	F/m^2	Parallel capacitance between C_{Inv} and C_{Dit} in case of split-CV technique
C_{LF_MOS}	F/m^2	Low frequency capacitance measured in MOS structure with QSCV technique
C_{m_QST}	F/m^2	Measured QSCV capacitance
C_{QST}	F/m^2	General expression for QSCV calculated capacitance
C_{QST_s}	F/m^2	Total quasi-static capacitance for single energy level of interface traps
C_{it_s}	F/m^2	Interface traps capacitance in case of single energy level of defects distribution (QSCV technique)
C_{it_c}	F/m^2	Interface traps capacitance in case of continuum energy distribution of defects (QSCV technique)
C_{QST_c}	F/m^2	Total quasi-static capacitance for continuum-like energy distribution of interface traps
$C_{it_c_\tau}$	F/m^2	Interface traps capacitance for continuum-like energy distribution of defects taking into account frequency effects
$C_{QST_c_\tau}$	F/m^2	Total QSCV for continuum-like energy distribution of interface trap density including frequency effects
C_{QST_LCR}	F/m^2	Complete expression of capacitance term measured in pseudo-MOSFET configuration taking into account traps time constant and τ_{RC}

Symbol	Unit (in SI)	Description
$C_{m_QST_Vg}$	F/m^2	Measured quasi-static capacitance at constant V_G
$C_{m_QST_sat}$	F/m^2	Saturation QSCV capacitance obtained by exponential fit of $C_{m_QST_Vg}$
C_{it_QST}	F/m^2	Capacitance of D_{it} obtained from experimental results
C_{peak}	F/m^2	Peak of measured capacitance value obtained during charging procedure in case of non-passivated surface
D		
D_{it}	cm^{-2}eV^{-1}	Interface trap density
D_{it_s}	cm^{-2}	Density of traps for a single energy level of defects
D_{it_eq}	cm^{-2}eV^{-1}	Equivalent interface traps density computed using FlexPDE®
E		
E	eV	Energy
E_{eff}	V/cm	Effective electric field
E_G	eV	Band gap
E_V	eV	Maximum energy value of valence band in case of silicon film
F		
F	-	Correction factor in *4*-probe measurements for non-infinite layer dimensions
f	Hz	Frequency
f_G	0.75	Geometrical factor in pseudo-MOSFET configuration
f_s	Hz	Frequency at which carriers oscillate between the conduction channel and the traps
f_T	-	Probability that the interface traps are filled
f_c	Hz	Corner frequency in case of Lorentzian spectrum
f_{ext}	Hz	Extraction frequency in case of LFN analysis
f_{conf}	-	Configuration coefficient for Van Der Pauw measurements
G		
G_{m_split}	S/m^2	Measured parallel conductance in case of split-CV measurements
G_p	S/m^2	Parallel conductance in case of split-CV measurements including also D_{it} contribution
G_{Dit_c}	S/m^2	Conductance due to lossy processes of D_{it} in split-CV technique
G	S	Conductance
g_m	S	Transconductace; $g_m = dI_D / dV_G$
H		
$h_{\delta\Psi}$	-	Height of $1\text{-}C_{m_QST}/C_{OX}$ curve versus V_G
I		

Symbol	Unit (in SI)	Description
I_D	A	Drain current
I_0	A	Constant current value time independent
δI	A	Current oscillations
I_{off}	A	Off current in case of transistor characteristic
I_{on}	A	On current in case of transistor characteristic
I_H	A	Hall current
L		
L	m	Die size
N		
N_D	cm^{-3}	Doping concentration in case of n-type material
N_a	cm^{-3}	Doping concentration in case of p-type material
N_{probe}	-	Number of probes
ΔN	-	Average fluctuation of carrier number
N_t	$cm^{-3}eV^{-1}$	Density of traps per unit volume
N_{t_added}	$cm^{-3}eV^{-1}$	Density of traps added in localized regions
N_C	cm^{-3}	Effective density of states in the conduction band
N_V	cm^{-3}	Effective density of states in the valence band
n_{it}	cm^{-3}	Density of filled traps
n_S	cm^{-3}	Electron density at surface
n_i	cm^{-3}	Intrinsic carrier concentration
P		
P	W	Power
p	g	Probe pressure for Jandel® station
Q		
Q_i	C/m^2	Inversion charge density
Q_{acc}	C/m^2	Accumulation charge density
Q_{Dep}	C/m^2	Depletion charge density
Q_{ch}	C/m^2	Total density of charge induce by gate bias
Q_{itrap}	C/m^2	Trapped charges by defects in case of continuum energy traps distribution
Q_{itrap_s}	C/m^2	Trapped charges by defects in case of single energy level of traps distribution
R		
R_{SD}	Ω	Access resistance
R_{CH}	Ω	Channel resistance
R_{SH}	Ω/square	Sheet resistance

Symbol	Unit (in SI)	Description
R_0	m	Probe radius
ΔR_0	m	Added radius to R_0
R_H	m^3/Ω	Hall coefficient
r_H	-	Hall scattering factor
S		
S	m^2	Die area: S = W·L
S_{eff}	-	Effective surface for capacitance measurements
S_{Id}	A^2/Hz	Drain current power spectral density
S_{Vd}	V^2/Hz	Voltage power spectral density
S_{Vfb}	V^2/Hz	Flat-band voltage power spectral density
S_{Vfb_area}	$V^2/(Hz \cdot m^2)$	Flat-band voltage power spectral density per unit area
S_{Vg}	V^2/Hz	Power spectral density associated to the gate bias (input-inferred noise)
S_{eff_LFN}	m^2	Effective surface of LFN technique
$S_{Id}/I_D^2{}_{_red}$	1/Hz	Reduced S_{Id}/I_D^2 obtained in smaller regions surrounding the probe contacts
$S_{Id}/I_D^2{}_{_tot}$	1/Hz	Whole current spectrum given by $S_{Id}/I_D^2 + S_{Id}/I_D^2{}_{_red}$
S_s	V/dec	Subthreshold swing
T		
T	K	Temperature
T_{an}	ºC	Annealing temperature
t_{OX}	m	Oxide thickness
t_m	s	Measurement time period of QSCV small signal ramp (*a.c.* ramp time)
t	s	Time
t_{Si}	m	Silicon film thickness
t_s	s	Charging time
$t_{III\text{-}V}$	m	III-V film thickness
V		
V_D	V	Drain bias
V_G	V	Gate bias
δV_G	V	Small gate bias variation
V_{gacc}	V	Lower limit of integral to compute μ_{eff}, in accumulation region
V_{G_peak}	V	Gate bias associated to C_{peak_h}
V_{G_charge}	V	V_G applied for a certain time t_S (*charging bias)*
ΔV_{ramp_ac}	V	Small signal ramp added to V_G to perform QSCV measurements
V_{back}	V	Back gate bias in case of transistors
V_{FB}	V	Flat-band voltage

Symbol	Unit (in SI)	Description
δV_{FB}	V	Small flat-band voltage variation
V_T	V	Threshold voltage
ΔV_{diff}	V	Differential potential measured between two probes
V_H	V	Hall voltage
v_{ramp_ac}	V	*a.c.* scan speed in case of QSCV measurements
W		
$w_{\delta\Psi}$	-	Width of $\delta\Psi_S/\delta V_G$ curve versus V_G
Y		
Y	$(V/A)^{0.5}$	Y function
X		
x_{dep}	m	Depletion region
Z		
Z_{EQ}	Ω	Equivalent impedance

Name	Unit (in SI)	Description
Greek Symbols		
α_H	-	Hoogle parameter
α_{sc}	Vs/C	Coulomb scattering coefficient
β	eV^{-1}	$\beta = q/(k \cdot T)$
γ	-	Slope of 1/f ($S_{Id}(f)$ characteristic)
η	F/cm^2	Ideality factor constant; 1/2 for electron, 1/3 for holes
ϑ	$m^{-2}s^{-1}$	Constant given by: $\sigma_T \cdot f_s$
θ_1	1/V	First order mobility attenuation factor
λ	m	Tunneling attenuation length calculated using Wentzel-Kramers-Brillouin (WKB)
μ_0	cm^2/Vs	Low-field carrier mobility
μ_{eff}	cm^2/Vs	Effective carrier mobility
$\mu_{0_T=77K}$	cm^2/Vs	Low-field mobility measured at $T = 77\ K$
$\mu_{0_at_0V}$	cm^2/Vs	Low-field mobility measured with $V_{back} = 0\ V$
ξ	V/cm	Electric field
ρ	$\Omega \cdot m$	Material resistivity
σ_T	m^{-2}	Carrier cross section
σ	S/m	Conductivity
$\delta\sigma$	S/m	Conductivity fluctuations
σ_{Dit}	m^{-2}	Traps cross section
τ_{Dit}	s	Trap effective life time
τ_{RC}	s	RC time constant
Ψ_S	V	Surface potential
Ψ_b	V	Bulk potential deduced from the doping concentration
Ω_C	V	Term for low-frequency noise analysis defined as: $\alpha_{sc} \cdot \mu_{eff} \cdot C_{OX_cm}$
Ω	m^3	Die volume
Ω_{eff}	m^3	Effective Volume
ω	rad/s	Angular frequency

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Caractérisation et modélisation électrique de substrats SOI avancés

(*Résumé en français*)

Les substrats Silicium-sur-Isolant (SOI) représentent la meilleure solution pour réaliser des dispositifs microélectroniques performants [1], [2]. La caractérisation électrique pour contrôler la qualité des substrats-sur-isolant (SOI) avant la fabrication complète des transistors est une étape indispensable [3]. La configuration classique utilisée pour les mesures du SOI est le pseudo-MOFSET (Ψ-MOSFET) [4]–[6]. Dans cette thèse, nous nous concentrons sur l'amélioration des techniques Ψ-MOFSET, pour la caractérisation des plaques SOI. Cette thèse est composée de 6 chapitres, incluant introduction et conclusions générales. Les principaux résultats concernant la caractérisation statique I-V, split-CV, CV en quasi-statique ou encore bruit basse fréquence sont décrits dans des chapitres dédiés.

- Chapitre II : ce chapitre décrit les améliorations apportées à la configuration de mesure pseudo-MOSFET utilisée pour la caractérisation statique de substrats SOI. L'impact de la configuration et des paramètres de mesure, et la possibilité de caractériser des nouveaux matériaux sont discutés. La Fig. 1a représente le courant de drain I_D mesuré en fonction de la tension de grille V_G en configuration Ψ-MOSFET (schéma de la configuration de mesure en insertion). Pour $V_G > 0$, le canal de conduction est formé par des électrons, alors que pour $V_G < 0$, il est constitué de trous. Les caractéristiques ont été évaluées sans et avec l'utilisation du vide, l'utilisation du vide visant spécifiquement à l'amélioration du contact entre le SOI et le porte-échantillon métallique (chuck) [7]. Une variation de la tension de seuil V_T est observée pour les différents types de contact face arrière. Pour des structures ultra-minces, l'utilisation du vide s'est avérée obligatoire, car il permet d'augmenter la stabilité des mesures.

Des nouveaux matériaux comme le InGaAs ont également été caractérisés en configuration Ψ-MOSFET et avec des mesures d'effet Hall. La Fig. 1b représente un exemple du courant de drain mesuré sur des échantillons III-V avec *25 nm* d'InGaAs et *30 nm* d'oxyde (Al_2O_3). Les mesures ont été réalisées avec différentes tensions de drain V_D. La résistance d'accès au canal étant très grande dans cette configuration, elle limite l'extraction des paramètres comme la mobilité des porteurs, μ. Pour ces raisons, nous nous sommes focalisés sur des substrats III-V avec des contacts métalliques déposés. Des valeurs de mobilité très prometteuses ont été obtenues, même pour des films ultra-minces ($\mu \approx 750\ cm^2/Vs$ pour $t_{III\text{-}V} = 20\ nm$).

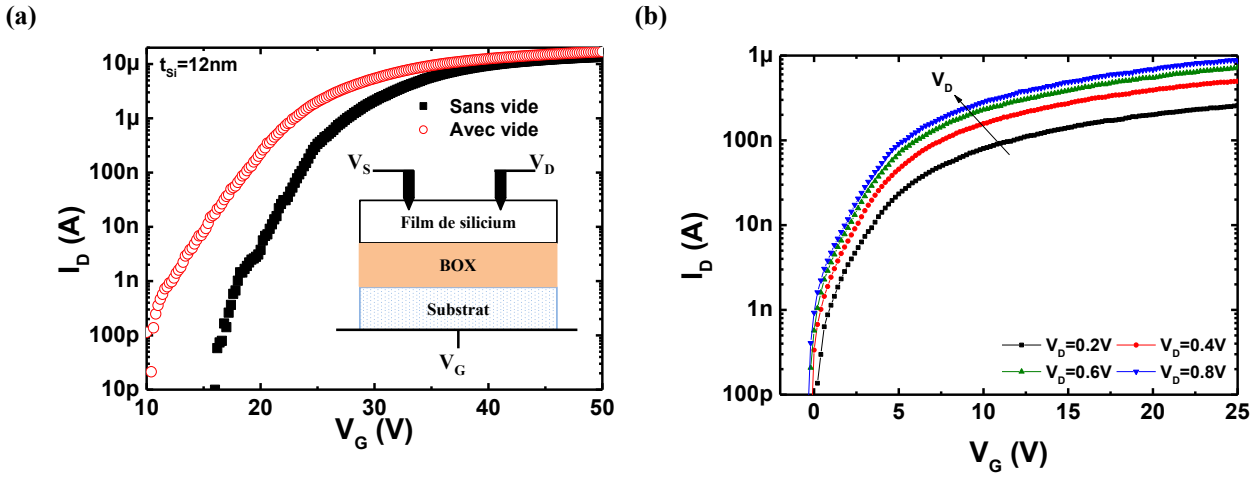

Fig. 1 : (a) Courant de drain I_D en fonction de la tension de grille V_G mesuré en configuration Ψ-MOSFET sur SOI sans (symboles pleins) et avec (symboles vides) l'utilisation du vide pour le contact arrière. L'insertion montre la configuration de mesure pseudo-MOSFET. (b) Caractéristiques $I_D(V_G)$ mesurées sur des échantillons III-V sur isolant, pour différentes valeurs de tension de drain V_D.

- Chapitre III : ce chapitre présente la technique de mesure split-CV, adaptée pour le pseudo-MOSFET. Nous discutons les possibilités d'amélioration du setup de mesure et d'extraire la densité d'états d'interface D_{it} en utilisant la mesure de conductance en fonction de la fréquence. Le contact avec le vide en face arrière est ici en particulier essentiel pour obtenir des valeurs correctes de capacité maximale (égale à la capacité de l'oxyde enterré) avec le split-CV. La Fig. 2a montre la capacité en fonction de V_G, mesurée sans (symboles vides) et avec (symboles pleins) l'utilisation du vide. Sans vide, des capacités parasites limitent la valeur maximale mesurée, alors qu'avec vide, la capacité maximale mesurée est très proche sa valeur théorique (traie en pointillé). En conséquence, l'extraction de la mobilité effective des porteurs devient plus simple et les paramètres d'ajustement comme la surface effective ne sont plus nécessaire [8], [9]. La dernière partie de cette étude concerne l'évaluation de la qualité des interfaces (D_{it}) en utilisant la méthode de conductance en fonction de la fréquence. Nos mesures ne montrent pas les pics typiques associés aux D_{it} [10]. Pour mieux en comprendre la raison physique, nous avons effectué des simulations numériques. La Fig. 2b montre la conductance (G_m) divisée par la pulsation (ω), calculée en fonction de ω. Les symboles pleins sont obtenus pour une structure SOI avec D_{it}, alors que les symboles vides sont associés aux simulations sans D_{it}. Après la création du canal de conduction (symboles rouges), les deux courbes se superposent. Dans ce régime, la mesure n'est pas sensible aux défauts d'interface, comme dans les transistors à effet de champ [11]. Pour $V_G \approx V_{FB}$ (tension de bandes-plates), les deux courbes se superposent également (symboles noires).

Nous avons montré qu'en configuration Ψ-MOSFET, la surface des échantillons utilisés est trop grande (≈mm^2) et elle masque la détection des défauts d'interface [12]. Donc, la méthode de conductance ne peut pas être utilisée pour évaluer la qualité des interfaces pour les structures SOI typiquement utilisées pour le pseudo-MOSFET. Cette limitation sur la détection des D_{it} peut être dépassée en effectuant des mesures de capacité en quasi-statique (QSCV) [10].

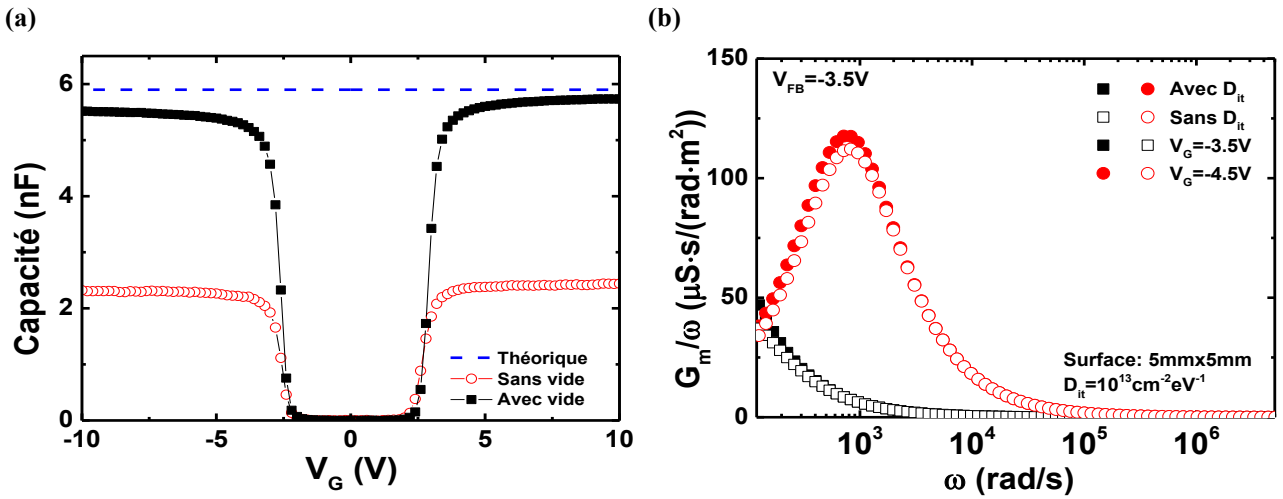

Fig. 2 : (a) Capacité mesurée avec (symboles pleins) et sans (symboles vides) l'utilisation du vide entre la structure SOI et le chuck métallique. Le traie en pointillés représente la valeur théorique de capacité. (b) G_m/ω versus ω calculée en régime d'accumulation (symboles rouges) et pour $V_G = V_{FB}$ (symboles noires).

- Chapitre IV : nous montrons la technique QSCV utilisée pour la première fois en configuration pseudo-MOSFET. Une procédure d'extraction de D_{it} est validée et utilisée pour caractériser les substrats SOI. Comme pour le split-CV, une pointe est posée sur la surface du silicium et reliée à la masse et le chuck métallique est polarisé. Contrairement au split-CV, la mesure de capacité est réalisée avec une rampe rajoutée sur la tension de grille V_G. La Fig. 3a montre la capacité quasi-statique mesurée en fonction de de V_G. La courbe tracée avec symboles vides a été obtenue avec une rampe rapide et elle est semblable aux mesures obtenues en basse fréquence en split-CV (symboles pleins dans la Fig. 3a). Une mesure à faible vitesse de balayage a été aussi réalisée sur les mêmes échantillons (symboles pleins). On peut noter la présence de deux *'épaules'* qui apparaissent autour de $V_G = 0\ V$, de toute vraisemblance dues aux défauts d'interface. Après validation de la configuration de mesure [13], un modèle physique basé sur la présence des D_{it} a été proposé pour expliquer les courbes expérimentales. Grâce à ces résultats, nous avons proposé une méthode d'extraction de D_{it} à partir des caractéristiques mesurées. La Fig. 3b représente des D_{it} en

fonction de l'énergie dans le gap du silicium. Les mesures ont été réalisées sur des couches de passivation de SOI (*4 nm* de SiO_2 obtenus par oxydation thermique sur la surface du film de silicium, pour améliorer la qualité de la interface supérieure [14]). Deux différentes épaisseurs d'oxyde enterré ont été utilisées : *25 nm* (symboles pleins) et *145 nm* (symboles vides). La superposition des deux courbes confirme que la variation de l'épaisseur de l'oxyde enterré a un faible impact sur la densité des défauts lents présents dans les structures SOI. Pour les échantillons non passivés, un grand pic dû à des défauts d'interface apparait pour des valeurs d'énergie bien identifiées et correspondant aux défauts à l'interface film de silicium-oxyde natif [15], [16].

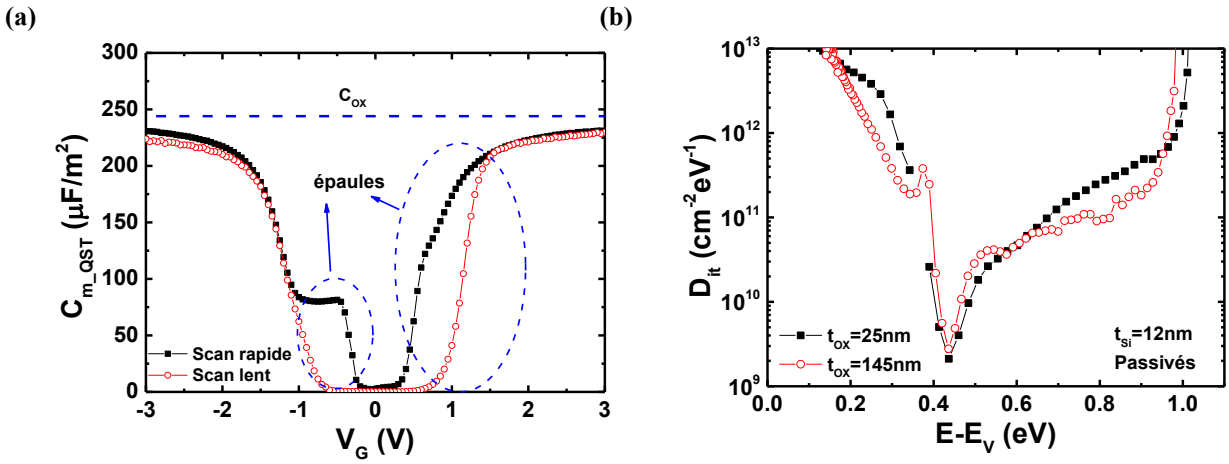

Fig. 3 : (a) Capacité quasi-statique mesurée en fonction de la tension de grille V_G avec vitesse de balayage rapide (symboles vides) et lente (symboles pleins). (b) D_{it} en fonction de l'énergie dans de échantillons passivés avec une épaisseur de BOX de *25 nm* (symboles pleins) et *145 nm* (symboles vides).

- Chapitre V : nous présentons dans ce chapitre, les mesures de bruit à basse fréquence (LFN) en configuration Ψ-MOFET. Le bruit a été déjà utilisé pour caractériser les interfaces des substrats SOI, mais les valeurs de D_{it} obtenues ont été très grandes et pas représentatives de la qualité du matériau [17]. Pour comprendre l'origine physique de ces résultats, nous avons validé la configuration de mesure et la procédure d'extraction. La Fig. 4a représente le spectre de la densité de courant de drain (S_{Id}) sur I_D^2 multiplié pour la fréquence d'extraction (f_{ext}) en fonction de I_D. Différentes valeurs de f_{ext} ont été utilisées pour vérifier la présence de 1/f trend. Les courbes superposées impliquent la présence du 'flicker noise *1/f*' [18]. Pour extraire la densité des pièges à l'interface D_{it} *nous avons* développé un model physique permettant d'expliquer le signal obtenu. Il a été validé pour différentes surfaces et distances entre les pointes. Grâces à ce modèle, nous avons démontré que le bruit à basse fréquence est principalement généré par une petite

surface de silicium autour des contacts. La Fig. 4b représente la distribution de la densité de puissance de courant sur la surface de silicium ; elle est clairement très localisée proche des pointes. Pour cette raison, nous avons introduit un paramètre (S_{eff}) qui quantifie la surface effective de silicium dominant le bruit. Grâce à S_{eff}, des valeurs plus raisonnables des D_{it} ont été extraites. De plus, grâces à des simulations et mesures, nous avons prouvé que le bruit à basse fréquence est limité par les défauts induits pendant la pénétration des pointes dans la surface de silicium. En conclusion, l'extraction des D_{it} n'est pas possible en utilisant la configuration standard de mesure, car la signature obtenue est dominée par les défauts introduits par las pointes. Pour améliorer l'analyse, des pointes plus larges et/ou la configuration de mesure 4-pointes pourrait être utilisés.

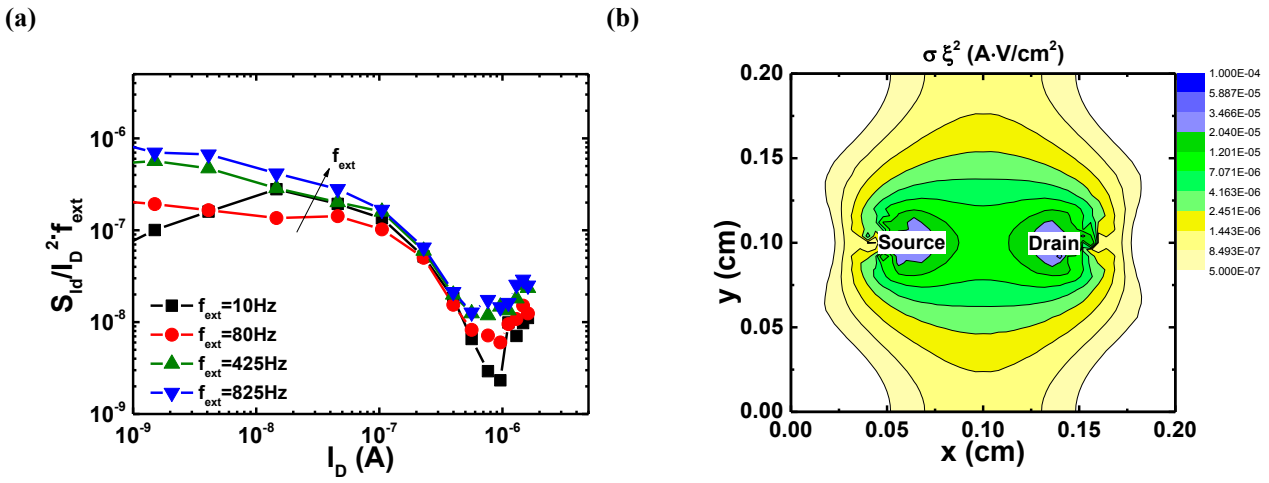

Fig. 4 : $S_{Id}/I_D^2 \cdot f_{ext}$ en fonction du courant de drain I_D pour différentes fréquences. (b) Distribution de la densité de puissance de courant sur le film de silicium.

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