Design of an analog waveform generator dedicated to software radio transmission

Yoan Veyrac

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université de BORDEAUX

Thèse

présentée à

L'Université de Bordeaux

Ecole doctorale des Sciences Physiques et de l'Ingénieur

par **Yoan VEYRAC**

Pour obtenir le grade de

Docteur

Spécialité : électronique

Contribution a l'etude et a la realisation d'un generateur de signaux radiofrequences analogiques pour la radio logicielle integrale

---

Soutenue le : 4 Décembre 2015

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"I don4t knoz if this keyboqrd is in qwerty"
Ray Charles

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List of Abbreviations

AD	Analog-to-Digital
AC	Alternating current
ADC	Analog-to-Digital Converter
AlGaN	Aluminium Gallium Nitride
ASIC	Application-Specific Integrated Circuit
BW	Bandwidth
CA	Carrier Aggregation
CMOS	Complementary Metal Oxyde Semiconductor
CW	Continuous Wave
DA	Digital-to-analog
DAC	Digital-to-analog converter
DC	Direct Current
DD	Digital to Digital
DFF	Delay Flip Flop
DK	Design Kit
DNL	Differential Non-Linearity
DPCM	Differential Pulse Code Modulation
DSP	Digital Signal Processor
DUT	Device Under Test
EM	Electro-Magnetic
ENOB	Effective Number of Bits
EVM	Error Vector Magnitude
FDSOI	Fully Depleted Silicon On Insulate
FIFO	First In First Out
FIR	Finite Impulse Response
FM	Frequency Modulation
FPGA	Field Programable Gate Array
FT	Fourier Transform
GaN	Gallium Nitride

HEMT	High Electron Mobility Transistor
HSTL	High Speed Transceiver Logic
IC	Integrated Circuit
IF	Intermediate Frequency
INL	Integral Non-Linearity
I/O	Input/Output
IoT	Internet of Things
IQ	In-phase & Quadrature
JTRS	Joint Tactical Radio System
LNA	Low Noise Amplifier
LTE	Long Term Evolution
LPF	Low-Pass Filter
LSB	Less Significant Bit
LUT	Look-Up Table
MIPS	Million Instructions Per Second
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
NSR	Noise Shaping Riemann
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PLL	Phase Locked Loop
PLS	Post Layout Simulation
PPA	Pre-Power Amplifier
PSD	Power Spectral Density
QFN	Quad Flat No-lead
QPSK	Quadrature Phase Shift Keying
QAM	Quadrature Amplitude Modulation
RADAR	RAdio Detection And Ranging
RC	Resistance-Capacitance
RF	Radio-Frequency
SDM	Sigma-Delta Modulation
SDR	Software-Defined Radio

SFDR Spurious-Free Dynamic Range

SMA SubMiniature version A

SR Software Radio

SNR Signal to Noise ratio

SQNR Signal to Quantization Noise ratio

TSMC Taiwan Semiconductor Manufacturing Company

UMS United Monolithic Semiconductors

VHDL Very high-speed integrated circuits Hardware Description Language

List of Notations

f_{max}	Maximum frequency of a useful signal
f_{nyq}	Nyquist frequency
f_s	Sampling frequency of a DA conversion
N	Number of bits involved in a DA conversion
P_n	Power of the noise
P_s	Power of a useful signal
q	Quantum of a DA conversion scheme
r	Oversampling factor: $OSR = 2^r$
V	Voltage amplitude of a CW

Introduction

The air interface that connects the mobile terminals to the wired network is subject to a rigorous regulation enforced through various communication standards. Next generation wireless communications require a smart and agile use of the spectral resources to increase the data handling capacity of the network.

This trend put severe constraints on the design of mobile device transceivers. They should deal with high data rates, multiple carrier frequencies and various modulation schemes within a very restricted power budget imposed by the limited energy storage of handset terminals.

Chapter 1 exposes the radio communication paradigm and the evolution of radio transmitter architectures. It underlines the trend to increase the flexibility of the wireless transmitters through an increasing use of digital electronics according to the Software Radio principle. The major gain in flexibility is contrasted by a prohibitive energy consumption, especially within the digital to analog conversion operation. The classical conversion schemes are studied and challenged.

Chapter 2 proposes the theoretical study of disruptive conversion schemes together with a suited digital to analog converter topology. It borrows the principle of Delta modulation involved in some data compression systems. The data conversion process deals with the temporal variations of the signal through a differentiating digital coding to significantly improve the conversion efficiency. The signal reconstruction is performed thanks to a custom integrating digital-to-analog converter named the Riemann Pump. The performances of the proposed system are assessed toward radio frequency signal generation.

Chapter 3 describes the design of the Riemann Pump in two targeted integrated technologies. The first one is a GaN technology dedicated to military applications. The second one is a 65 nm silicon technology adapted to the consumer electronics market. The design of the two circuits is detailed and post-layout simulations are presented to validate the compatibility of the proposed architecture with the chosen technologies and to assess its performances

Chapter 4 presents the measurements carried out on the demonstrator realized in the 65 nm silicon technology. The obtained results bring a physical proof of concept. An extension of the test bench testing capabilities is required to go further in the characterization of the prototypes. Prospects are envisioned to develop a complete transceiver based on the Riemann Pump.

Chapter

1 Transmitters for ubiquitous network

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Chapter 1 presents the architectural trends for next generation RF transmitters. The first part introduces the wireless communication paradigm. It highlights the forthcoming requirements for handset terminal transceivers and the associated technological bottleneck. The second part presents the tracks which tend to overcome this stumbling block, in relation with the state of the art of flexible transmitters. Finally, the associated conversion schemes efficiency is questioned, claiming for disruptive approaches.

Key words: RF transmitters, Data conversion schemes, Software radio, 5G

" The very small value of 10^{-16} of negentropy required per bit of information plays, however, a very important role in modern life, and it makes possible to communicate information at a negligible cost. "

Leon Brillouin, Science and Information theory, 1956

In the 50s, Brillouin stated that modern life relies on the possibility to deal with large quantities of information for a minimal cost. In the same decade, the development of the transistor in Bell laboratories led to a physical media allowing to get closer to the theoretical cost of information described by Brillouin. After several decades during which the electronic industry endeavored to follow the Moore's law, standalone devices that can exchange a billion of bits per second fit in one's hand. However, conventional transceiver architectures cannot support the pressing digital convergence while satisfying customer expectations in terms of quality of service, device cost and battery life.

1.1 Wireless communication paradigm

In the 2010s, the global amount of information exchanged is still in huge growth, even though it tends to decelerate. In the same time, the proportion of mobile data is rapidly increasing; the connection to the internet becomes more and more nomadic.

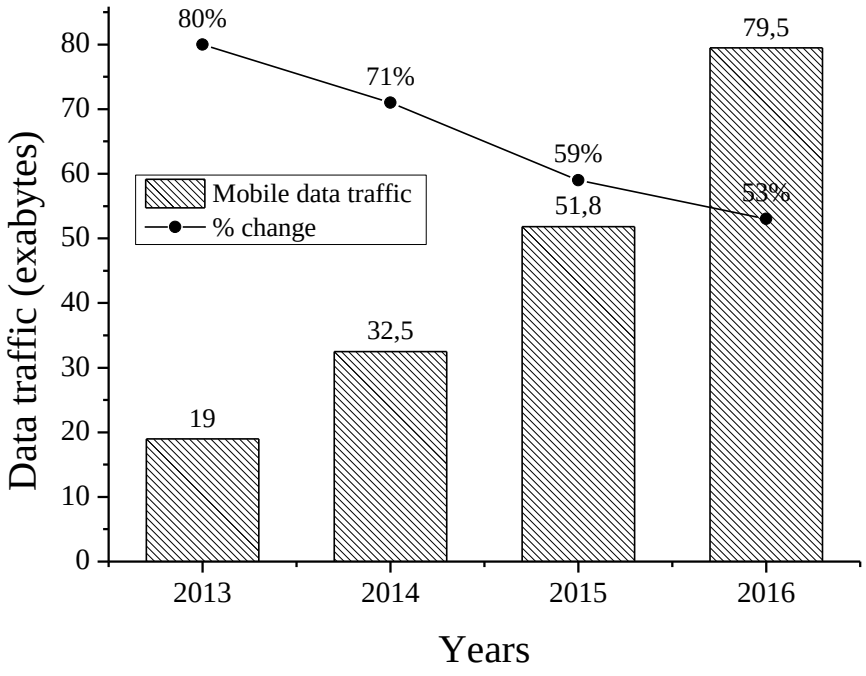

Figure 1.1: Global mobile data traffic (source: Gartner 2015)

1.1.1 Radio frequency transceivers architecture

The connection of wireless terminals to the network is provided by the mean of radio-frequency (RF) electromagnetic waves. Those terminals are able to transmit and receive information carried at high frequencies, while ensuring the compatibility to various standards which set the traffic rules. The data to be transmitted is conditioned within the transmitter chain to be radiated by the antenna, while the receiver chain recovers the data from the signal picked up by the antenna. The classical simplified architecture of RF direct conversion transceivers is represented in Fig. 1.2.

The transmission chain is composed of four main blocks:

- A baseband processor
- A digital to analog converter (DAC)
- A mixer to convert the signal up to the carrier frequency
- A power amplifier

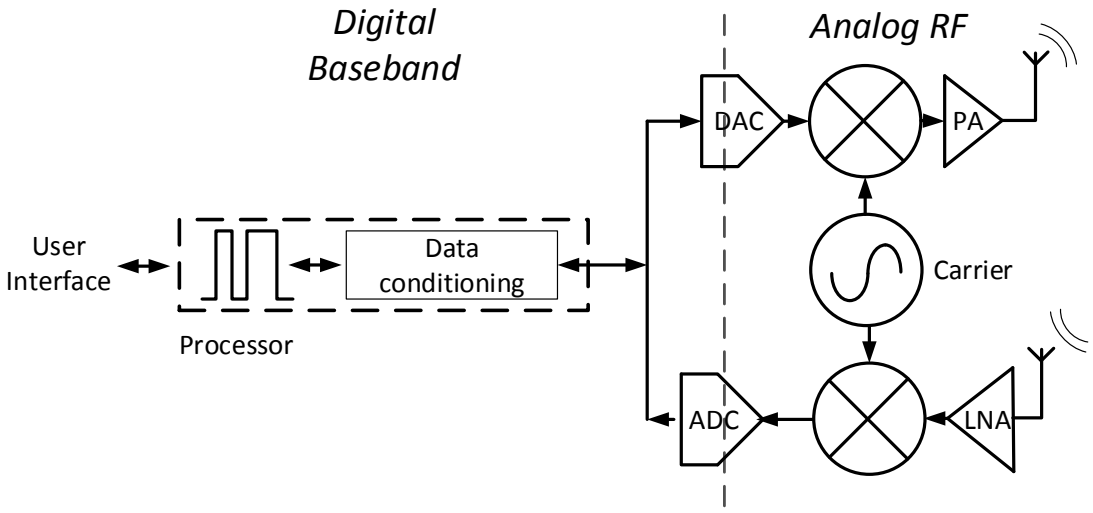

Figure 1.2: Classical direct conversion transceiver architecture

The baseband processor encodes the user digital information which is then converted into the analog domain thanks to the DAC. The analog signal is up converted to RF within the analog front-end, and then amplified and transmitted through the antenna.

The receiver chain is composed of dual blocks:

- A low noise amplifier
- A mixer to down convert the signal to baseband
- An analog to digital converter (ADC)
- A baseband processor

The RF signal is picked up by the antenna, and amplified by the low noise amplifier. It is then mixed with the carrier frequency so as to recover the baseband data, which is computed by the processor and sent to the user interface. This transceiver architecture is commonly used and implemented in mobile terminals to provide a link to the network.

The growing number of connected terminals and the increasing amount of exchanged data raise congestion issues in the wireless communication space.

1.1.2 Wireless communication media capacity

The medium used to convey wireless data is the air. This medium is shared between users along three principal axes, to avoid interferences:

- **Geographic areas**: the wireless data transmission uses radiofrequency signals transmitted thanks to antennas. The received power decreases with the distance to the transmitter. The network is organized with a cellular pattern, to isolate geographic areas.
- **Frequency allocation**: the frequency spectrum is divided into channels dedicated to specific services. Several frequency bands are allocated to mobile communications, and those ones are subdivided into channels to handle different users at the same time.
- **Time sharing**: communications on the same channel in the same area can occur by sharing the time. Different portions of time are assigned to users.

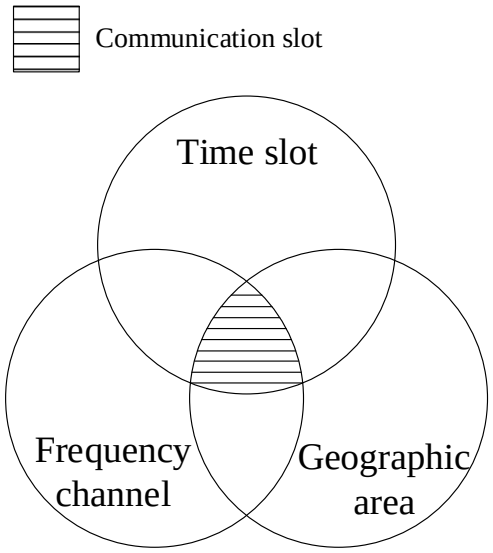

Figure 1.3: Venn diagram of the 3-dimensions wireless communication space

The intersection of those three axes defines a communication slot, depicted in Fig. 1.3. To avoid interferences, communication slots must be allocated only once. The capacity and the efficiency of a network depend on the number of communication slots offered, and its adequacy with the local needs. In order to enhance the handling capacity of the wireless network, improving the use efficiency of those three resources will be needed.

- The **geographic areas** obviously depend on the local density of users; cities need a finer mesh than countryside areas. The setting of cells of different size, associated with different transmitting power, allows to locally adapt the capacity of the network to the need.

- The **frequency** allocation is the key resource, controlled and delivered by dedicated authorities. Within the whole spectrum, only a few RF bands are allocated to mobile communications. Those bands are shared between several mobile access providers. Those successive divisions result in relatively narrow bands available for users, in the range of several MHz. The re-allocation of frequency bands will help to meet the need of mobile data communications.

- The **time** is the last dimension to be shared between users. In a same channel, multiple communications can occur thanks to time allocation. However, in the case of intense exchange of data at a given moment, the channel can be saturated. The dynamic allocation of frequency resources along time could improve the traffic fluidity. Instead of the stringent partitioning of frequency bands, those resources could be dynamically re-allocated when needed. It would grant much wider bands when the traffic is sparse, and help to fully use the resources when it is crowded.

Such a radio network is based both on smart network supervision and adaptive radio transceivers.

1.1.3 Mobile terminal transceivers compatibility

The classical transceiver architecture depicted in Fig. 1.2 suffers from a lack of flexibility inherent to the conversion performed in the analog front-end. Such a transceiver usually addresses a given standard, corresponding to a relatively narrow frequency band. However, the increase of the access bandwidth relies on the use of large frequency bands distributed all over the RF spectrum. Their introduction comes regularly with new standards and their own requirements. Mobile terminals use different transceivers to address the various standards. This trend to increase the number of parts in the chipset of mobile terminals faces pressing limits related to the industry directions and the consumer expectations.

- **Bandwidth**: transceivers for handsets have to support more and more data rate, on various frequency bands distributed over a multi-GHz frequency range. They have to ensure an adequate resolution over a very wide frequency band.

- **Energy consumption**: transceivers are one of the most power hungry part of mobile terminals. They must operate at low power to improve battery life of handsets.

- **Cost**: to address mass market, the transceivers should be low cost. The cost of a chip is related to the die area and the technology used.

The stacking of chips involved in the handset terminals to address different frequency bands and gather data bandwidth cannot conciliate the previous constraints. The cumulated die area of all

the transceivers turns out large, which impacts the total price of the chips and their integrability in the small volume of a handset terminal. Furthermore, enhancing the total bandwidth thanks to the addition of transceivers would substantially increase the energy consumption since the analog front-end is duplicated for each transceiver. Classical transceivers architectures suffer from a lack of flexibility and they are no more suitable for the expected ubiquitous network. Our purpose is to develop a disruptive architecture of radio transmitter that can take up the challenge.

The next section describes the evolution of wireless transmitter architectures in the past few decades, and the state-of-the-art trends and realizations that tend to overcome the requirements of tomorrow. Then, a come back to the basics of digital to analog conversion will help to apprehend the limits of the commonly used conversion schemes. It raises the need to develop innovative architectures of transmitters.

1.2 Software radio transmitters

1.2.1 Software radio background

1.2.1.1 Principle

In order to meet the need of versatility raised by the new wireless communication perspectives, [1] proposed a new paradigm with the notion of software radio (SR) twenty years ago. The idea is to move the limit between the baseband domain and the RF domain within the digital processor, so as to get rid of the rigid analog front-end. The corresponding ideal architecture is depicted in Fig. 1.4.

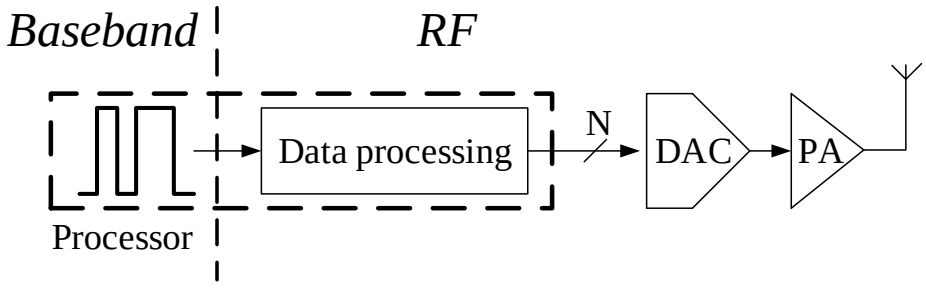

Figure 1.4: Software radio transmitter architecture

The ideal SR architecture is composed of 3 blocks:

- A baseband/RF processor
- A wideband digital to analog converter (DAC)
- A wideband power amplifier

This architecture proposes to directly compute the modulated signal (or even a combination of multiple signals) within the digital processor, and to convert the whole transmitting band of several GHz to the analog domain thanks to a wideband converter. The output of the converter then needs to be amplified before transmission through the antenna. Software radio offers a perfect flexibility, since it is virtually compatible with all the existing standards falling into the RF domain, and any new standard can be supported thanks to a simple software update. Furthermore, it allows concurrent transmission of different standards and agile reconfiguration.

1.2.1.2 Applications

The works on software radio transceivers are motivated by many applications, involving huge markets.

Military market

The flexibility of SR transceivers finds a lot of military applications.

- **Interoperability**: the US military has been seeking a way to improve the ease and flexibility of communications within and between the services. A huge program called joint tactical radio systems (JTRS) has been launched, without success at the time [2].
- **Secure communications**: the intrinsic flexibility of SR transceivers offers a perfect support to operate dynamic changes of the standards to secure communication links in the battlefield.
- **Radar**: SR transmitters are able to generate various waveforms, including radar signals. The accurate control of the waveforms allows to enhance the performances of detection [3].
- **Electronic Warfare**: To control the electro-magnetic spectrum in a battlefield, the use of versatile transceivers is an asset. A lot of applications rely on the use of agile signals generation (jamming, stealth, countermeasures) [4].

Civil market

The next generation of wireless communication standards (5G) is expected to offer ubiquitous immersive connectivity, relying on a software upgradable platform. Several researches on the network and communication architectures and techniques are led at the moment [5],[6]. The infrastructures would rely on an heterogeneous network with cells of different sizes [7]. The use of device to device communication is envisioned to virtually densify the network [8], and content caching to reduce data duplication [9]. As for frequency resources, 5G is expected to use as much spectrum as possible [10], divided into 3 frequency ranges for different applications (Fig. 1.5).

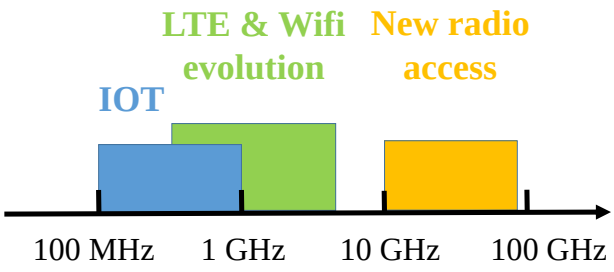

Figure 1.5: Technology tracks of 5G era

The sub-6 GHz frequency range ensures a favorable transmission in the air; a data rate higher than 1 Gbps is expected on this band thanks to carrier aggregation. It will be based on an extension of the LTE standard and used by all the devices.

The mmW band has a reduced range and could serve in smaller cells [11], giving access to wide data bandwidth.

The internet of things (IoT) will be deployed in the same time, using the sub-GHz frequency band. The number of connected wireless devices will be in huge growth. Equipping those devices with reconfigurable and low-power transceivers presents a major industrial asset [12].

SR transceivers are in agreement with the implementation of those various techniques which necessitate a high flexibility. Sub-6 GHz and IoT applications are privileged targets for full software radio transmitters. Wireless communication handsets represent the most lucrative market, involving billions of units. It also constitutes one of the most challenging applications.

[13] reminds the technical and technological difficulties to reach high bandwidth and high performances at a reduced power to ensure a longer battery life, and above all with a low cost solution.

A lot of researches are oriented toward the evolution of wireless transmission architectures in the direction of flexible solutions.

1.2.2 Directions of research for flexible transmitters

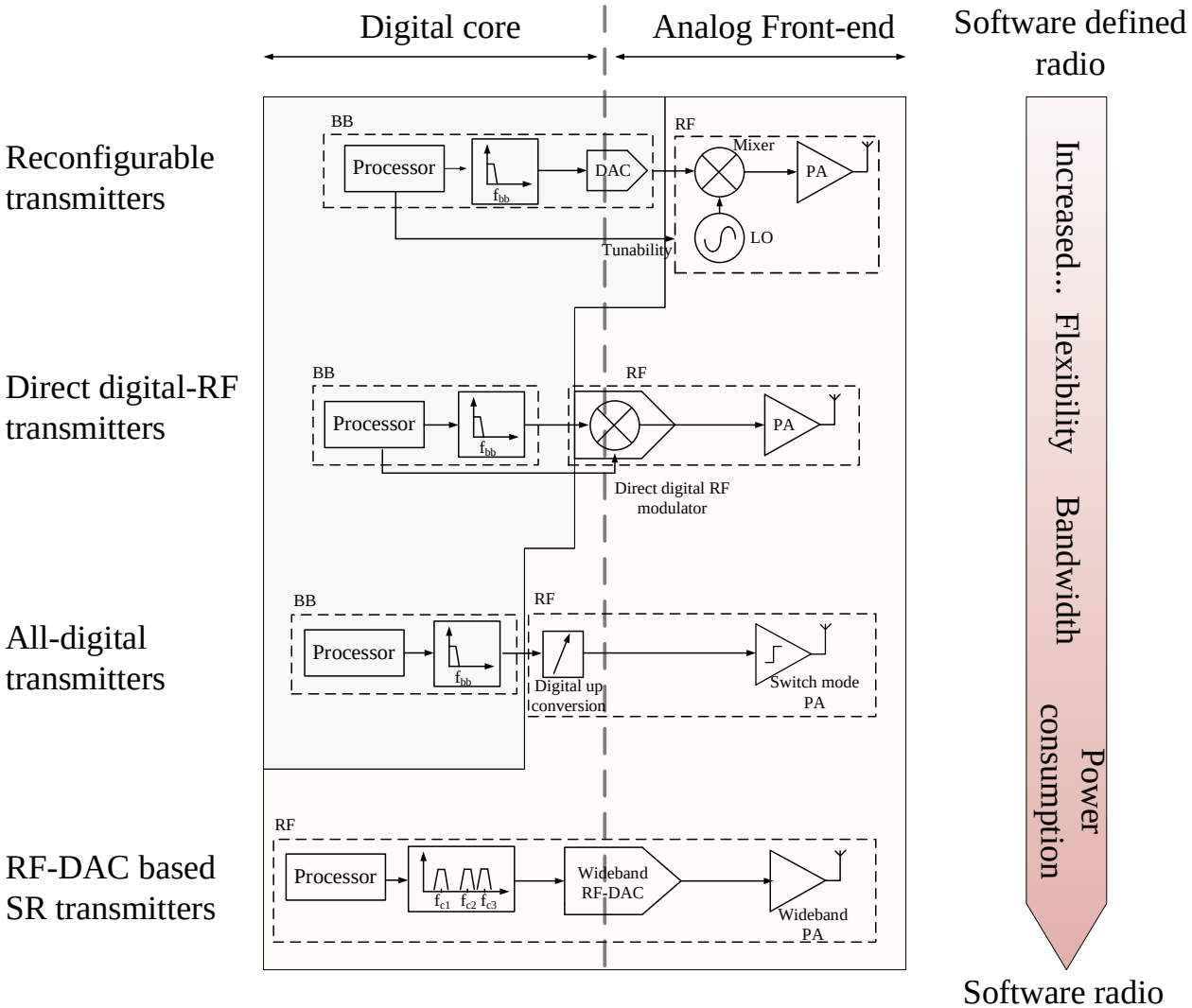

Figure 1.6: From software defined to software radio transmitters

1.2.2.1 Reconfigurable transmitters

An intermediate step toward SR is software defined radio (SDR), where the analog front-end is reconfigurable thanks to a digital command. SDR transmitters are based on a baseband or intermediate frequency digital to analog conversion, before a final up-conversion in the analog domain. In those architectures, the reconfigurability of the analog front-end is the tricky point [14]. Various realizations of SDR transmitters are reported in the literature.

[15] proposes a software defined radio transceiver based on direct conversion with a fractional PLL, enabling carrier frequency reconfiguration. The channel bandwidth is tuned up to 16 MHz thanks to reconfigurable low-pass filters.

[16] exhibits a multiband multimode transmitter dedicated to several wireless communication standards. Multiple paths are specifically tailored to meet the precise requirements of the 2G, 3G and 4G standards; only one band group is activated at once.

[17] presents a reconfigurable monolithic transceiver working over [50 MHz - 6 GHz] frequency band. The transmitter operates with direct up conversion for the highest part of the band, and two-step up conversion for the lower part, to filter the local oscillator harmonics.

[18] exposes a SDR transmitter covering the [100 MHz - 6 GHz] band thanks to two distinct paths. The maximal signal bandwidth of 100 MHz can be used to support intra-band dual carrier aggregated signals.

Table 1.1: Performances of reconfigurable transmitters.

	Bandwidth (MHz)	**RF range (GHz)**	**Consumption (mW)**	**CMOS node (nm)**
[15]	16	0.15 – 6	100	130
[16]	20	0.7 – 2.7	200	90
[17]	40	0.05 – 6	900	130
[18]	100	0.1 – 6	103	65

1.2.2.2 Direct digital-RF transmitters

Direct digital-RF transmitters try to merge the DAC and the mixer operation, with only digital inputs. It simplifies the analog front-end and tries to give more flexibility through the increased

use of digital signals. A lot of silicon chips realizations confirm the feasibility to integrate it into handset terminals.

[19] proposes a direct digital to RF modulator to up-convert a 200 MHz sigma-delta coded base-band signal at 5.25 GHz. An auto-tuned passive band-pass reconstruction filter is placed at the output to cancel the digital images.

[20] implements an all-digital RF signal generator using low pass sigma delta modulation and digital mixing. It employs redundant logic and non-uniform quantization, and also proposes to use image bands to reach higher frequencies.

[21] discloses a fully digital multimode polar transmitter. It implements a cartesian to polar converter and a RF-DAC made of current-mode mixers. The local oscillator is generated thanks to a digital PLL.

[22] presents an all-digital quadrature transmitter where I and Q paths are up-converted within power cells thanks to a digital local oscillator. The two paths are then combined into a differential load.

[23] addresses the issue of full duplex operation within an RF IQ transmitter. It proposes an embedded FIR filtering of out of band quantization noise to ease full duplex operation.

[24] employs a digital IQ transmission scheme with 13 bits resolution on each path. The base-band digital signals are digitally mixed and converted into the analog domain thanks to digital to RF amplitude converters.

Table 1.2: Performances of direct digital-RF transmitters.

	Bandwidth (MHz)	**RF range (GHz)**	**Consumption (mW)**	**Implementation**
[19]	200	5.25	187	130 nm CMOS
[20]	50	0.05 – 1	120	90 nm CMOS
[21]	4	0.9 & 1.9	250	–
[22]	80	2.2	510	40 nm CMOS
[23]	20	2.4	515	65 nm CMOS
[24]	150	0.06 – 3.5	560	65 nm CMOS

Most of the presented works target specific standards. They propose fully integrated solutions, including the power amplification operation. However, the flexibility of the system remains limited and the bandwidth and consumption performances are not sufficient to address forthcoming applications like 5G.

1.2.2.3 All-digital transmitters

Another trend consists in removing most of the analog front-end to propose all-digital architectures. The advancement of CMOS technologies makes digital architectures attractive [25]. The development of FPGA motivated a lot of works on the digital architectures.

[26] uses a pulse width modulation scheme to process the baseband signal and a digital IQ up-conversion to carry the signal at 800 MHz. This transmitter architecture is implemented on a FPGA and outputs a 1-bit waveform.

[27] implements an innovative digital architecture and assesses it on a very high speed data signal generator. The idea is to represent a given modulation thanks to a finite state machine and to store all the possible symbol transitions in look-up tables. The baseband bit stream moves within the state machine and triggers the right sequences that are outputted as a 1-bit sequence. A sigma-delta like scheme is employed to perform noise shaping. This approach relies on heavy computational optimizations, but it supposes that the signal is representable by a finite state machine, which limits its applicability.

[28] describes an FPGA-based 1-bit all-digital transmitter using a sigma-delta modulator before digital up-conversion. It demonstrates real-time processing on an FPGA for a signal bandwidth of 2 MHz centered at 0.8 GHz.

[29] implemented a transmitter architecture with sigma-delta baseband processing and digital up-conversion. The baseband scheme is performed with an FPGA which outputs are fed to a multiplexer, together with a high speed clock generated with an external clock generator. The output is then amplified with a switched mode power amplifier.

Most of the presented architectures rely on the use of a digital 1-bit FPGA output to drive a switch-mode power amplifier, with the implementation of different kinds of digital signal conditioning. They demonstrate the interest of such digital techniques to address reconfigurable radiofrequency transmission.

Table 1.3: Performances of all-digital transmitters.

	Bandwidth (MHz)	**RF range (GHz)**	**Architecture**	**Implementation**
[26]	20	0.8	PWM	FPGA
[27]	–	1 – 13	SDM-LUT	Instrumentation
[28]	2	0.8	SDM	FPGA
[29]	2	2.5	SDM	FPGA + instrumentation

On those all-digital transmitters, the digital up-conversion is performed with a multiple of the baseband or intermediate frequency clock, so that the output RF frequency has an integer relationship with the working frequency. This issue has been noticed by [30]; in this reference, a sampling rate adapter is proposed. This constraint of sampling rate and carrier frequency mitigates the flexibility of the system, especially when it comes to multi-standard and multi-band concurrent transmission. Furthermore, the total available bandwidth is limited because the conversion before the digital up-sampling is performed at baseband or intermediate frequency, often involving sigma-delta modulation.

All digital transmitters are attractive because they remove most of the analog components. The proposed architectures are easily implementable and portable to new technological nodes. However, the signal bandwidth is still limited to several tens of MHz, and most of the presented circuits are dedicated to a specific standard. The consumption of the transmitters is difficult to assess because of their implementation on an FPGA.

1.2.2.4 RF–DACs

Even though reconfigurable analog and all-digital transmitters turn out to exhibit features of software defined radio, that is, digital reconfigurability and a relative flexibility, they do not manage to deal with wideband modulated signals or concurrent transmission of a large number of signals in different bands. Those features could be offered by full software radio transmitters, giving an ideal platform to develop large cognitive radio networks [31].

To achieve this kind of architecture, the digital to analog stage has to convert the whole band of transmission, of several GHz. In this way, the complete RF waveform is transmitted, containing any combination of signals with any kind of modulation schemes and bandwidth. Referring to the software radio transmitter basic architecture (Fig. 1.4), it needs a performant digital pro-

cessing core, a wideband digital to analog converter, and a power amplification stage.

The digital to analog converter is particularly critical since it has to ensure a good signal quality over the whole RF spectrum with a low power operation. Plethora of DACs are presented in the literature, with diverse operating frequency and number of bits in the conversion.

[32] implements a 12b current-steering DAC, with specific circuit implementation to limit the mismatching and keep the non-linearities under the LSB level. A segmented architecture is chosen, with 6 binary and 6 unary weighted input bits.

[33] proposes a pseudo segmented current-steering DAC working at 28 GSps, with 6 bits, that implements a time-interleaving technique. This is one of the highest switching frequencies of the state-of-the art. The ENOB falls down to 4.6 bits for the highest part of the band.

[34] uses a 14 bits segmented architecture implemented in a BiCMOS process. Each resampling switch operates on an equivalent current source. A weighting of the 10 LSBs is done through an R-2R ladder.

[35] proposes a current steering DAC architecture, with 14 bits. It implements digital signal conditioning and high speed serialization to control the current array which outputs the differential RF analog signal into resistive loads.

[36] presents a 13 bits current steering DAC working at 9 GSps. It uses specific techniques within the current cells array to reduce code-dependant output capacitance, and a pre-distortion look-up table to improve INL performances.

[37] exhibits a multimode transmitter based on a segmented current steering DAC. The high speed digital interface is embedded to feed the DAC with high speed data.

All the presented DACs except one are designed in CMOS technologies. They all implement current-steering topologies, mostly with segmented architectures. Current steering topology is known to be best suited to high speed operation [38].[39] studied the limitations of this architecture in terms of accuracy and speed, the two main characteristics of DACs. The use of time interleaving is an interesting track [40][31][41] to relax the speed of each single path.
The large majority of the DACs presents a too elevated consumption for handset applications,

Table 1.4: Performances of RF-DACs.

	Data rate (Gsps)	**Resolution (bits)**	**Consumption (mW)**	**Efficiency (mW.s/Gbit)**
[36]	9	13	360	3.1
[32]	2.9	12	188	5.4
[35]	6	14	600	7.1
[37]	5	9	375	8.3
[33]	28	6	2250	13.4
[34]	7.2	14	4600	45.6

ranging from hundreds of milliWatts to the Watt level. The consumption efficiency (mW.s/Gbit) is displayed in Fig. 1.7 versus the Nyquist bandwidth of the listed DACs. It corresponds to the power consumption divided by the data rate involved in the conversion.

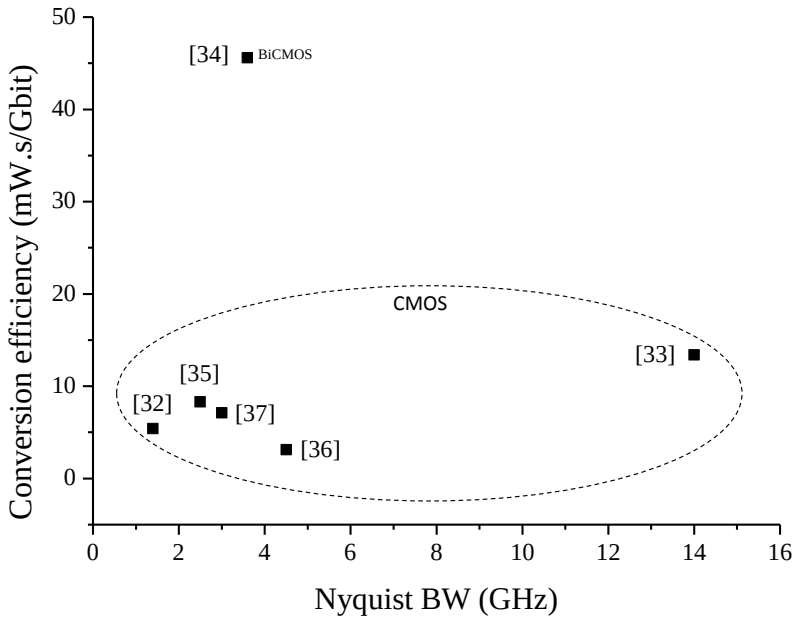

Figure 1.7: Wideband DAC SotA – Conversion efficiency Vs Nyquist bandwidth

The DAC realized in BiCMOS process exhibits a substantially higher consumption. The DACs realized in CMOS process are much more efficient, and they have an average conversion efficiency of several mW.s/Gbit. The resulting consumption for a 5 GHz bandwidth 12 bits DAC is around 500 mW, which is far too much for the DAC alone. The power budget of the DAC should be limited to a few tens of mW.

The broadband DAC approach to convert the whole transmitting band is still not integrable in handset terminals, because of a too high power consumption of the DAC itself.

1.2.2.5 Conclusion

Transmitter architectures tend to move from reconfigurable systems still relying on a complex analog front end to more digital solutions. Direct digital-RF transmitters and all-digital transmitters are in constant evolution, and they address present standards. However, the bandwidths are still bounded to several tens of a few hundreds of MHz, and the flexibility is limited. Multi-band concurrent transmission is not always supported.

The development of full SR transmitters would provide the bandwidth and agility required for the future standards. Those systems are based on high speed data processing and a suited RF-DAC. The consumption of state-of-the-art DACs is unfortunately too high to allow the implementation of a full SR transmitter in a handset device. A new kind of RF-DAC is needed to lower the power consumption. It requires an innovative digital to analog conversion scheme to lower the cost of conversion in terms of energy.

In the next section, we propose to come back to digital/analog conversion theory basics. The most classical conversion schemes, involved in the referenced state of the art works, are studied to underline their features toward multi-GHz operation.

1.3 Data conversion schemes

Quantization is the operation which separates the analog world from its digital counterpart. An analog signal evolves in a 2 dimensions continuous environment, where one is the time. A digital signal is made of a collection of points with discrete coordinates, thus allowing easy representation and storage. The discretization of time is associated with the notion of clock; changes can occur only on clock events. When the clock frequency is constant, the time vector can simply be an index. The binary representation of discrete quantities appears to be the most suitable to electronic implementation. The discretization of quantities thus relies on the use of bits (Fig. 1.8).
The accuracy of the digital representation of an analog signal is tightly related to the involved coding scheme. The two key parameters that drive the accuracy of a conversion are:

- the sampling frequency f_s
- the resolution (number of bits used in the conversion) **N**

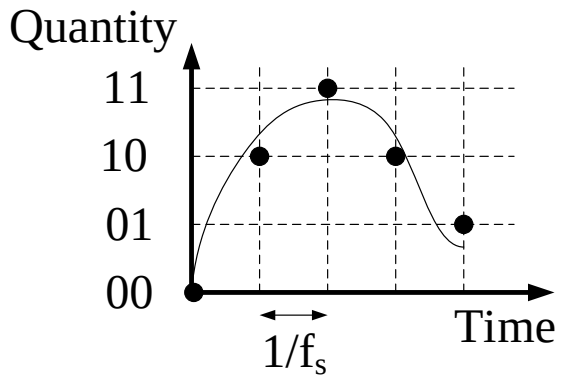

Figure 1.8: Quantization – the DA interface

Increasing those two parameters may result in an enhancement of the accuracy of the conversion, at the cost of a higher complexity of the system. As for the electronic implementation, this complexity induces higher component count, energy consumption, die area and design subtlety. A bandwidth limited analog signal of maximum frequency f_{max} can be perfectly described by an infinite resolution digital signal sampled at the Nyquist frequency ($f_s = f_{Nyquist}$) which is twice f_{max} (Nyquist-Shannon theorem). That is to say the original analog signal can be recovered without any additive noise; provided the digital signal has a perfect accuracy and the sampling images are ideally filtered (Fig. 1.9). This is theoretically achievable with an infinite number of bits to code the sampled analog levels. Such a signal would exhibit an infinite signal to noise ratio (SNR).

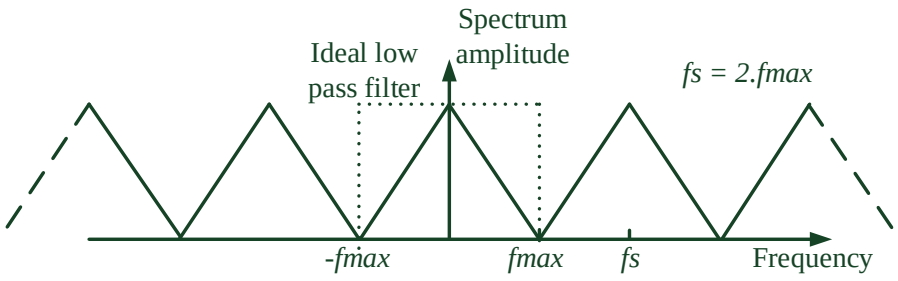

Figure 1.9: Spectrum of an ideally sampled signal

An actual DA conversion obviously involves a digital signal with a limited number of bits to drive the DAC. The overall DA conversion can thus be split into two distinct operations (Fig. 1.10):

- **a digital-to-digital (DD) conversion** that transforms the ideal digital signal into a resolution-limited digital signal at the working frequency f_s

- **a digital to analog converter (DAC)** together with an additional low pass filter to retrieve the desired signal

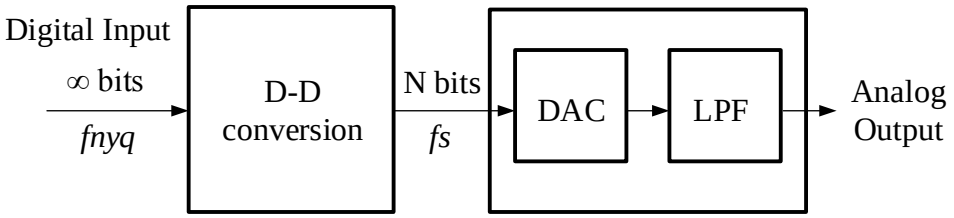

Figure 1.10: Architecture of overall digital to analog conversion

The most popular data coding schemes used for digital-to-analog conversion will be presented hereafter, together with the related quantization noise. Those two widespread techniques are:

- **Pulse code modulation (PCM)**
- **Pulse density modulation (PDM)**

1.3.1 Pulse code modulation

1.3.1.1 Nyquist rate pulse code modulation

The most spontaneous way to encode an ideal digital signal with a finite number N of bits is to quantize each sample thanks to a N-bit word at the Nyquist frequency, with a pulse code modulation (PCM) scheme (Fig. 1.11).

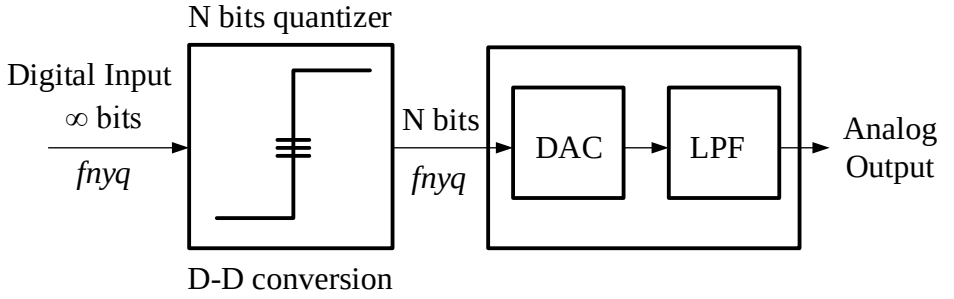

Figure 1.11: Nyquist PCM DAC architecture

Such a quantizer disposes of 2^N steps over the whole dynamic $[-V, +V]$. Considering a uniform repartition of quantization levels, the dynamic is split into $2^N - 1$ intervals of length $\frac{2V}{(2^N-1)}$, this

length being called the quantum q. Thus, the error e_q made when quantizing an input sample belongs to $[-q/2, +q/2]$. The assumption that the probability density function of eq is uniform over this interval is done, which is generally acceptable for full scale signals (e.g modulated signals) [42]. The quantization error can thus be seen as a noise with a power given by:

$$\sigma_e{}^2 = \int_{-\infty}^{\infty} e_q{}^2.p(e_q)\,\mathrm{d}e_q = \int_{-\frac{q}{2}}^{\frac{q}{2}} e_q{}^2.\frac{1}{q}\,\mathrm{d}e_q = \frac{q^2}{12} \tag{1.1}$$

For a large enough N, the quantum q is approximated by $\frac{2V}{2^N}$, so that the power of the quantization noise is expressed as:

$$\sigma_e{}^2 \approx \frac{V^2}{3.2^{2N}} \tag{1.2}$$

This noise is in the general case considered as a white noise lying on the $[\frac{-f_s}{2}, \frac{+f_s}{2}]$ frequency band [43]. For further calculations, we consider that the digital input signal represents a full scale sine wave, carrying a power $\sigma_x{}^2$ of $\frac{V^2}{2}$ once reconstructed in the analog domain. The maximum signal to quantization noise ratio (SQNR), is then calculated:

$$SNR_{dB} = 10log_{10}(\frac{\sigma_x{}^2}{\sigma_e{}^2}) \approx 6.02N + 1.76 \tag{1.3}$$

This well-known formula is used as a reference to calculate the effective number of bits (ENOB) of converters. Such a SNR could be achieved on the analog output signal with an ideal DAC and an ideal LPF that cuts the frequencies over f_{max}.

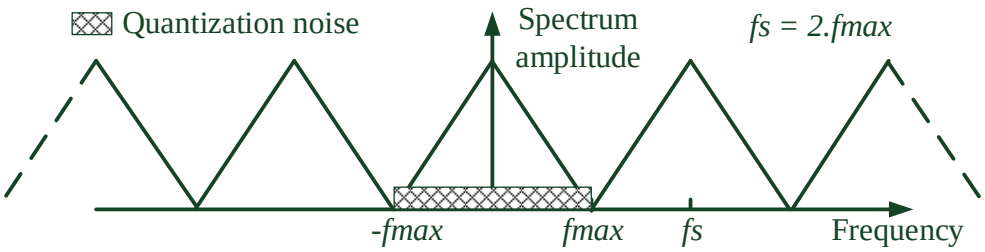

Figure 1.12: Spectrum of a Nyquist rate quantized signal

Most common DAC architectures operate as zero-order holds which generate a staircase signal [44]. From the frequency viewpoint, the zero-order hold multiplies the digital signal spectrum by the cardinal sine function whose first zero is $2.f_{Nyquist}$. This has the beneficial effect of providing a first low pass filtering which helps cutting high frequency images. However, it also causes a mild roll-off of gain at the highest frequencies of the desired band, thereby degrading the SNR. An analog low-pass filter is generally added to further attenuate the out-of-band signal, with the same harmful effect on the wanted signal. The technique of oversampling tackles this problem,

through the use of a higher sampling frequency; this opens a frequency gap between f_{max} and $\frac{f_s}{2}$ which enables, inter alia, cleaner filtering.

1.3.1.2 Oversampling

Compared to the previously described Nyquist-rate-DD conversion, the oversampled version involves an up-sampling filter that adds samples up to a rate of $2^r.f_{Nyquist}$ [45]. This operation is considered as ideal, so that it provides samples with infinite resolution without adding any kind of noise.

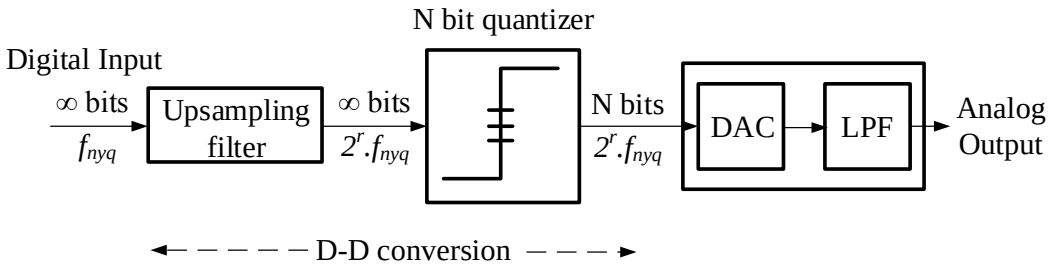

Figure 1.13: Oversampled PCM DAC architecture

The quantization noise generated by this structure has exactly the same power as before, since the quantizer exhibits the same characteristics and produces the same quantization errors. The difference comes from the repartition of the noise over the spectrum; as mentioned previously, the quantization noise behaves like a white noise for non-peculiar signals. The quantization noise power is thus uniformly distributed over the band $[\frac{-f_s}{2}, \frac{+f_s}{2}]$.

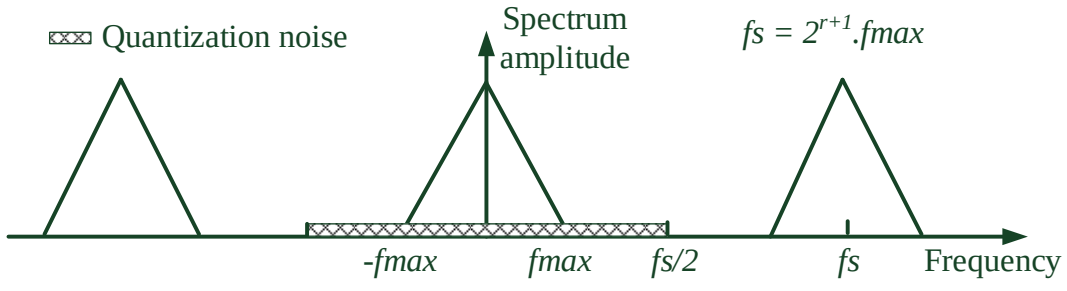

Figure 1.14: Spectrum of an oversampled quantized signal

A part of the quantization noise power stands outside the wanted signal band, and is likely to be filtered out. The in-band quantization noise power is its total power divided by the oversampling ratio (OSR = 2r). Assuming an ideal low pass filtering, the maximum achievable SNR is:

$$SNR_{dB} = 10log_{10}(\frac{{\sigma_x}^2.OSR}{{\sigma_e}^2}) \approx 6.02N + 3.01r + 1.76 \quad (1.4)$$

Oversampling thus allows a slight enhancement of the SNR by partial removal of quantization noise. It also relaxes the constraints on the analog low pass filter since it makes room to filter sampling images without altering the wanted signal; however, in this case, it reduces the amount of quantization noise filtered.

The widespread PCM DAC architecture is able to convert large frequency bands (cf. Tab. 1.4), but it turns out resource intensive to achieve a sufficient SNR, both as far as power consumption and die area are concerned. The reason is that the SNR grows preferentially with the number of bits N used to code quantized levels, and a high N implies a high component count, thereby requesting resources.

1.3.2 Pulse density modulation

Another way to encode signals is pulse density modulation (PDM), where the relative density of pulses over time represents the amplitude of the corresponding analog signal. Such a modulation can be implemented through the sigma-delta process [46]. It generally uses a one-bit quantizer that outputs a stream of ones and zeros depending on the input signal. A high density of ones corresponds to a high value of the signal and vice versa.

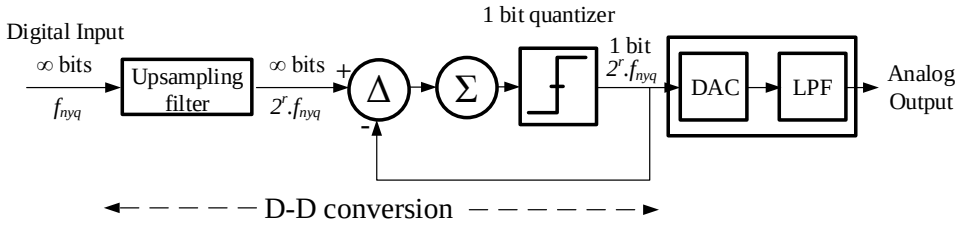

Figure 1.15: First order sigma delta block diagram

The quantization error produced is fed back in the sigma-delta process so that every error is taken into account into the next sample quantization. This results in the averaging out of the quantization error, so called noise shaping. The description of this phenomenon for a DD sigma-delta modulator is usually done thanks to a linear z-transform block diagram.

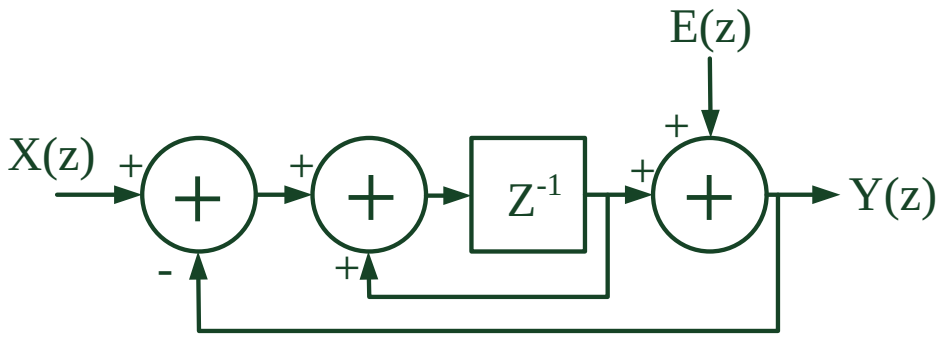

Figure 1.16: First order sigma delta z–transform diagram

The input signal X corresponds to the output of the up-sampling filter, which is considered ideal as above; this signal is at a rate of $2^r.f_{Nyquist}$, with a virtually infinite resolution. The integrator that sums the difference between X and Y is represented as an adder associated with a delay element. The quantizer is modeled by an additive noise E. The output Y can be calculated versus the two inputs, respectively the wanted signal X and the quantization noise E:

$$Y(z) = X(z).z^{-1} + E(z).(1 - z^{-1}) \tag{1.5}$$

The wanted signal is simply delayed by a sample period, whereas the quantization noise is shaped by a high pass transfer function. The total quantization noise of the system is the one of a one-bit quantizer of dynamic $[-V, +V]$; it exhibits a quantum q of 2V. The quantization noise power equals $\frac{q^2}{12}$, i.e:

$${\sigma_e}^2 = \frac{q^2}{12} = \frac{V^2}{3} \tag{1.6}$$

The spectral distribution $S_e(f)$ of this noise power for the open loop version would be uniform in the range $[\frac{-f_s}{2}, \frac{+f_s}{2}]$.

$$S_e(f) = \frac{{\sigma_e}^2}{f_s} \tag{1.7}$$

In the sigma-delta configuration, this noise is shaped instead, with the previously calculated noise transfer function. This transfer function can be expressed in the frequency domain as:

$$NTF(f) = 1 - e^{-j2\pi\frac{f}{f_s}} \tag{1.8}$$

It leads to:

$$|NTF(f)|^2 = (1 - e^{-j2\pi\frac{f}{f_s}})(1 - e^{j2\pi\frac{f}{f_s}}) = 4sin^2(\pi\frac{f}{f_s}) \tag{1.9}$$

The in-band quantization noise, i.e the part of the noise which lies on the frequency band $[-f_{max}, f_{max}]$, is given as:

$${\sigma_n}^2 = \int_{-f_{max}}^{f_{max}} S_e(f).|NTF(f)|^2 \,\mathrm{d}f = \frac{{\sigma_e}^2}{f_s}\int_{-f_{max}}^{f_{max}} 4sin^2(\pi\frac{f}{f_s})\,\mathrm{d}f = 2.{\sigma_e}^2[\frac{1}{OSR} - \frac{1}{\pi}sin(\frac{\pi}{OSR})] \tag{1.10}$$

Assuming a large enough OSR, the Taylor series expansion of the sinus function can be used, so as to simplify the previous equation:

$$sin(x) \approx x - \frac{x^3}{3!} + \frac{x^5}{5!} + ... + \frac{(-1)^N x^{2N+1}}{(2N+1)!} \tag{1.11}$$

And,

$${\sigma_n}^2 \approx {\sigma_e}^2(\frac{\pi^2}{3.OSR^3}) \tag{1.12}$$

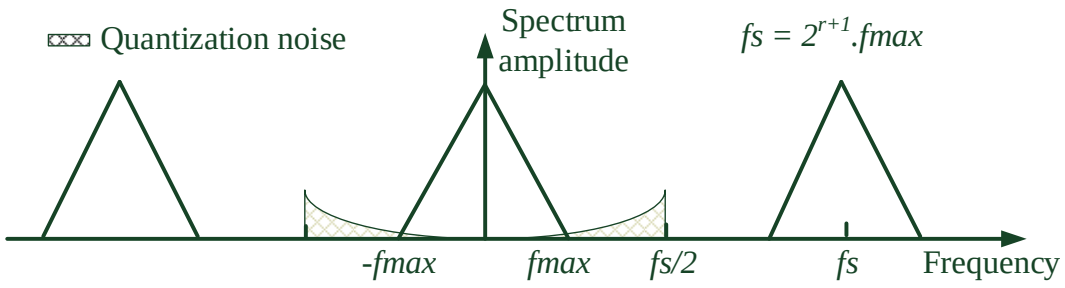

Figure 1.17: Spectrum of a SDM quantized signal

The maximum SNR theoretically achievable with an ideal low pass filtering – when the input corresponds to a full scale sine wave – is thus given as:

$$SNR_{dB} = 10log_{10}(\frac{{\sigma_x}^2}{{\sigma_x}^2}) \approx 9.03r - 3.41 \tag{1.13}$$

It is to note that using an N-bit quantizer has the same effect as on the PCM architecture, that is enhancing the maximum SNR of 6 dB per additional bit. Compared with the PCM architecture, the maximum SNR highly improves with the OSR. However, this works only under the

assumption of a high enough SNR. Indeed, in the in-band quantization noise calculation, the inversely proportional to OSR term can be cancelled by the first term of the sinus Taylor series only if the argument of the sinus is small enough. In the case of a low to moderate SNR, this assumption falls and the resulting term lowers the SNR compared with the calculated formula. This observation is relevant with all the more reason for higher order sigma-delta modulators - where the SNR depends even more on the OSR - since their principle is based on the cancellation of the successive terms of the sinus Taylor series.

This architecture is likely to be efficient for baseband signals conversion, up to several tens or hundreds of MHz (cf. Tab. 1.3). Large frequency band conversion (over the GHz range) implies a relatively low OSR because of technological limitations. As a consequence, the frequency gap between f_{max} and $\frac{f_s}{2}$ is likely to be thinner than a decade, which makes it difficult to fully benefit from noise shaping. The major problem of this topology under these conditions is that the total quantization noise does not wane as OSR is increasing, it remains constant instead.

1.3.3 Conversion efficiency

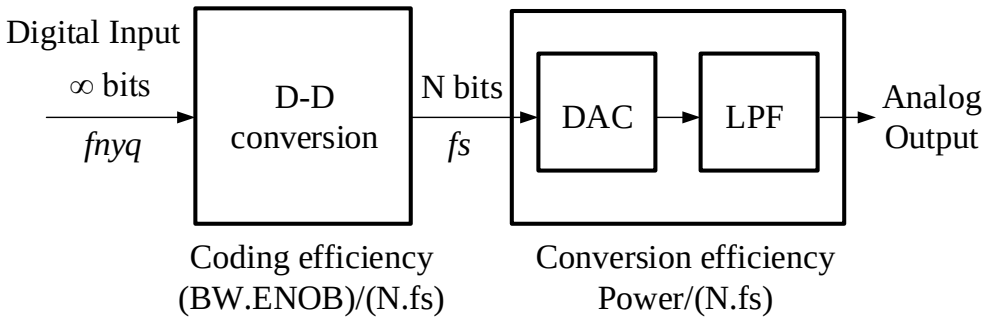

Figure 1.18: Efficiency of global digital to analog conversion

The global efficiency of a digital to analog architecture mainly comes from two origins:

- **The coding scheme**: the efficiency of a coding scheme can be assessed through the quotient of the actual information content of the encoded signal ($ENOB.bandwidth$) by the data rate involved in this code ($N.f_s$). The global data rate directly impacts the consumption and complexity of the digital processing block.
- **The digital to analog conversion**: the efficiency of the conversion mainly depends on the DAC topology and implementation. It can be described by the ability of the DAC to

convert a given digital data volume into an analog signal. The efficiency is thus the ratio of the power consumption and the input total data rate ($N.f_s$).

The global efficiency of the digital to analog conversion is then the multiplication of the two described efficiencies. It is representative of the tradeoff between conversion performances (bandwidth, resolution), and power consumption.

The two major conversion methods are related to the two dimensions associated with quantization: time resolution and amplitude resolution.

- **PDM** takes advantage of time resolution; it needs a high oversampling ratio to reach the requirements in terms of resolution. It faces technological limitations in terms of maximum working frequency. Furthermore, the use of a high oversampling ratio rapidly degrades the coding efficiency.
- **PCM** is associated with high resolution RF-DACs. The conversion efficiency of state-of-the art DACs remains a stumbling block for handset applications.
- **A combination** of these approaches can be implemented with a multi-bit sigma-delta architecture. It combines the features of the two conversion schemes, with the same bottlenecks.

Table 1.5: Key features of the classical conversion schemes.

Conversion scheme	**Key axis**	**Key parameter**	**SNR dependance (dB)**	**Coding efficiency**
PCM	Amplitude	N	6N	$\frac{1}{2}$
PDM – 1 bit SDM	Time	r	9	$\frac{1+\frac{3r}{2}}{2^{r+1}}$

1.4 Conclusion

The media convergence, the user habits and the density of devices induce a huge increase of wireless data volume. Changes must occur on the network structure to bear this appetite for data. In order to ensure the compatibility with an upcoming heterogeneous and ubiquitous network, mobile terminals transceivers should satisfy the 3 major constraints:

- **Low cost** solution to address mass market. The flagship technology is CMOS.
- **Low power** operation, to cope with the electrical energy storage constraints.
- **High bandwidth** capabilities, to enable transmission of high data rates, and to dynamically address existing and forthcoming standards.

SR transmitters based on the direct conversion of a wide frequency band appear as good candidates to provide an absolute flexibility; however, the consumption of RF-DACs prevents this solution from being integrable in portable devices. The realization of a suitable transmitter needs a disruptive approach of digital to analog conversion, to improve the conversion efficiency and to overcome the bottlenecks associated with the handsets stringent requirements.

We propose to explore a disruptive approach of digital to analog conversion, involving both the coding scheme and the DAC topology.

Chapter

2

The Riemann Pump

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Chapter 2 presents conversion schemes based on the digital differentiation of the encoded signal and their integration within the DAC operation. Theoretical features of those conversion schemes are studied and modeling SNR equations are obtained. The Riemann Pump is presented as the integrating DAC needed to recover the analog signal. Its reconstruction characteristics are exposed. Finally, system simulations are led to assess the validity of the theory with respect to the key parameters of the architecture. The application to sub-6 GHz 5G transmission schemes is highlighted and a suited sizing of the architecture parameters is proposed.

Key words: Carrier aggregation, Concurrent transmission, Differential Pulse Code Modulation (DPCM), Quantization noise, Riemann Pump, Signal to Noise Ratio (SNR), Sub-6 GHz 5G

2.1 Differential digital to analog conversion

The conversion efficiency introduced in the conclusion of Chapter 1 reflects the ability of a conversion architecture to describe an analog signal accurately with the most optimized number of digital information. All the classical conversion architectures used in the state of the art converters and transmitters rely on the absolute digital encoding of the wanted signal. We propose to encode the relative variations of the signal instead of the signal itself in order to alleviate the quantity of digital information required for the coding. It consists in operating the conversion through the derivative of the signal. The conversion scheme involved in this architecture is described in this section.

2.1.1 Differential Pulse Code Modulation (DPCM): Riemann

Differential coding schemes, such as differential PCM (or delta modulation in the case of a 1-bit quantization) are sometimes used in data compression for imaging and audio applications [47], [48]. Nevertheless, this technique remains barely used in communication systems [49], and even less in SR applications. The principle of DPCM is to quantify with N bits the relative variations of the input signal instead of its absolute value. The coded output thus represents the derivative of the signal and has to be integrated in order to recover the wanted signal.

- A first option consists in quantifying at each step the difference between the current input sample and the previous one (Fig.2.1). This simple structure presents an important drawback: the quantization error is cumulative and once recovered after decoding (a simple integration), the output signal may drift.

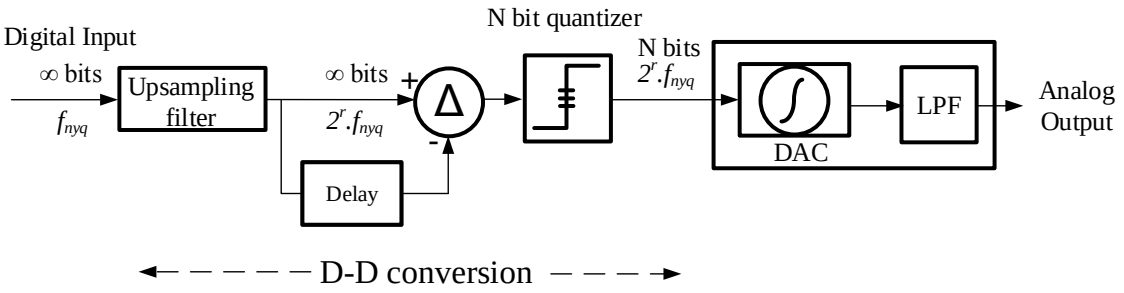

Figure 2.1: Open loop DPCM diagram

- A second option consists in quantifying the difference between the current input sample and the output of a local digital decoder that represents the estimated value of the previous sample. It ensures the compensation of quantization errors so that no drift is observable in the recovered signal. This last version will be considered in the following; the corresponding scheme is represented in Fig. 2.2.

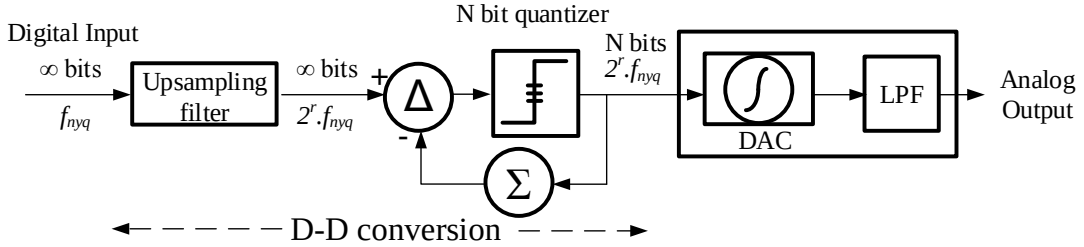

Figure 2.2: Closed loop DPCM diagram

The quantizer does not need to cover the whole signal dynamic since the quantity to be quantized is related to the difference between successive samples. Indeed, it simply has to follow the maximum variations of the input signal to avoid overload distortion. The quantizer dynamic is thus closely related to the input signal maximum frequency.

In order to convert any bandwidth limited signal (of maximum frequency f_{max}) with an N-bit DPCM scheme operating at the frequency f_s, the dynamic of the quantizer must fulfill the mentioned constraint. The largest level of the quantizer has to be larger than the maximum variation of the said signal so as to follow the input signal variations.

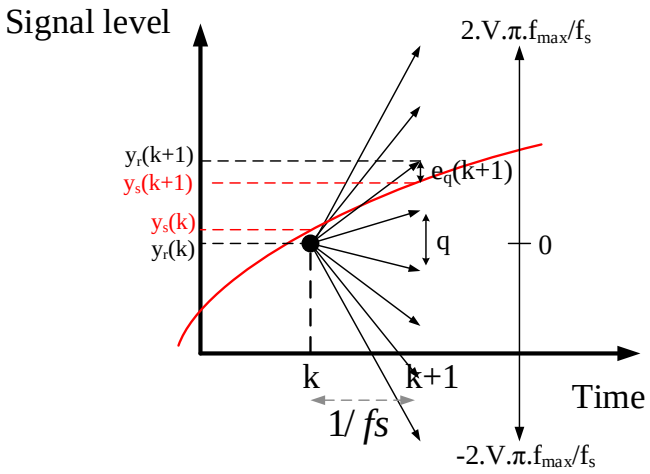

Figure 2.3: Quantization error for DPCM

The calibration of the slopes set is represented in Fig. 2.3. Taking a full-scale ($[-V, +V]$) sine wave at the maximum allowed frequency f_{max}, the maximum of the derivative equals $2V\pi f_{max}$; the maximum potential variation over a time step is $2V\pi\frac{f_{max}}{f_s}$. The largest positive level is thus set at this value. The larger negative level is then set at the opposite value $-2V\pi\frac{f_{max}}{f_s}$. SR applications deal with modulated signals that cover a significant part of the dynamic range $[-V, +V]$, and with high enough frequency components. Under these conditions, the quantization error power is minimal when the quantization levels are uniformly distributed between the extreme ones (see Annex 4.1). The quantization error $e_q(k)$ corresponds at each step to the difference between the ideal sample of the input signal $y_s(k)$ and the estimated value of this signal $y_r(k)$ at the output of the decoder. The interval of length $4V\pi\frac{f_{max}}{f_s}$ is subdivided into $2^N - 1$ intervals of identical length q.

$$q = \frac{4V\pi f_{max}}{(2^N - 1)f_s} = \frac{2\pi V}{(2^N - 1)OSR} \tag{2.1}$$

The quantization error can be considered as a quantization noise with a total power:

$$\sigma_e{}^2 = \frac{q^2}{12} \approx \frac{3V^2}{(2^{2N} - 2^{N+1} + 1).OSR^2} \tag{2.2}$$

It is to note that this power is inversely proportional to the OSR squared, which comes from the differential coding. The z-transform block diagram of the described conversion scheme (Fig. 2.4) enables to assess the frequency distribution of the quantization noise.

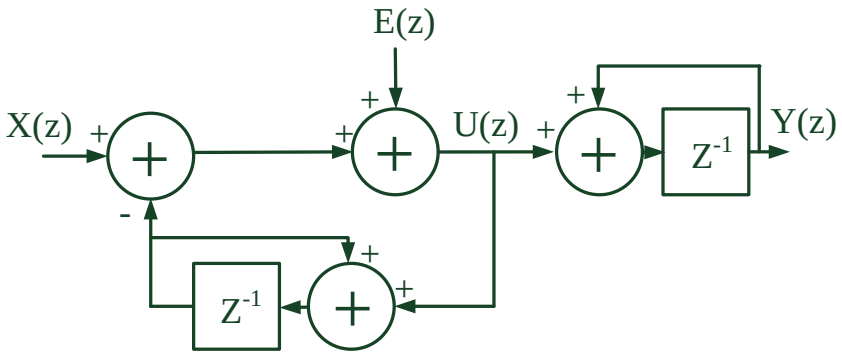

Figure 2.4: DPCM z-transform block diagram.

The quantizer is modeled as an additive noise, and is followed both on the feedback path and on the forward path by adders. The one on the forward path corresponds to the signal recovery integration performed by the DAC, and it is necessary to model it so as to evaluate the transfer function with respect to the signal and not its derivative. The calculations give:

$$U(z) = X(z)(1 - z^{-1}) + E(z)(1 - z^{-1}) \tag{2.3}$$

And with a further integration:

$$Y(z) = X(z)z^{-1} + E(z)z^{-1} \tag{2.4}$$

The transfer function is the same with respect to the signal $X(z)$ and to the noise $E(z)$ and it simply operates as a delay; no noise shaping is performed. Thus the quantization noise calculated

previously can be considered as an unshaped white noise lying on the frequency band $[-\frac{f_s}{2}, \frac{f_s}{2}]$. Assuming the out-of-band noise (i.e. the noise over f_{max}) could be filtered out perfectly, the remaining in-band quantization noise is:

$$\sigma_n{}^2 = \frac{\sigma_e{}^2}{OSR} \tag{2.5}$$

The signal to quantization noise ratio (SQNR) for a full scale sine wave is thus calculated as:

$$SQNR_{dB} \approx 6.02N + 9.03r - 7.78 + 10log_{10}(1 - \frac{1}{2^{N-1}} + \frac{1}{2^{2N}}) \tag{2.6}$$

In formula 2.6, the dependence of the SQNR on the OSR has a double origin. The main effect comes from the differential coding. Any doubling of the sampling frequency divides by 2 the range to be covered by the quantizer, as well as the quantum. Thus, it brings a factor $6.02r$ in the SQNR, corresponding to a decrease of the total quantization noise generated. The additional factor $3.01r$ comes from the filtering out of the noise lying on the band $[f_{max}, \frac{f_s}{2}]$. Considering RF applications, the OSR is inherently low and its effect does not mainly depend on the filtering of the out-of-band quantization noise; the requirements on the analog output filter are thus relaxed. This topology of DA conversion is optimized for low OSR applications, in order to cover a large frequency band without a complex and resource intensive architecture.

In the following sections, the **Riemann** conversion refers to the DPCM DD conversion architecture presented in this paragraph.

2.1.2 Noise Shaping Riemann conversion (NSR)

Starting from the Riemann architecture, it is possible to add a quantization error compensation feature, by taking into account the error made in any sample to calculate the next one. Given the ideal samples $y_s(k)$ and $y_s(k+1)$, and the step-k-calculated sample $y_r(k)$, it is now to determine the next quantized sample $y_r(k+1)$. The principle of error compensation is to aim a corrected sample $y_{s,corr}(k+1)$ instead of the real sample $y_s(k+1)$ (Fig. 2.5). The corrected sample integrates the previous error.

$$y_{s,corr}(k+1) = y_s(k+1) - e_q(k) \tag{2.7}$$

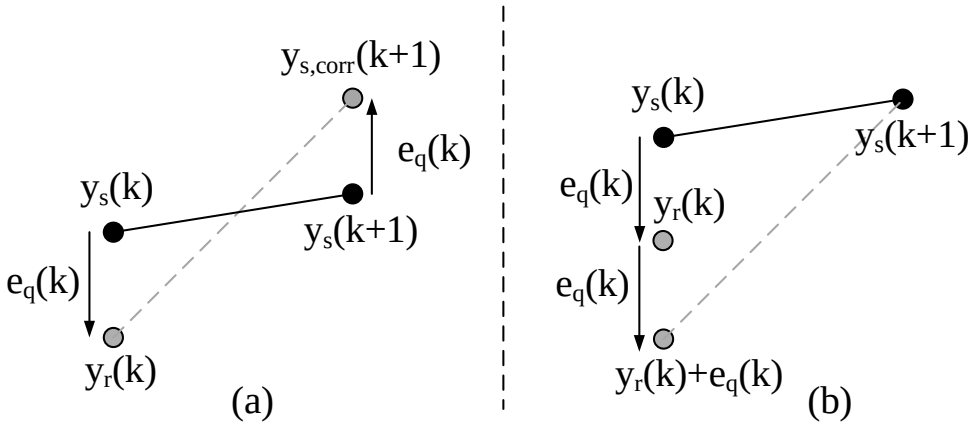

Figure 2.5: Noise Shaping Riemann conversion process.

In this way, when the effective sample $y_r(k+1)$ is calculated (as an approximation of $y_{s,corr}(k+1)$), the average error done between two successive samples is lowered. Considering the DD conversion principle, the value to be quantized to produce the $y_r(k+1)$ sample is now $y_s(k+1) - (y_r(k) + e_q(k))$. The Z-transform block diagram of this version of DD conversion can thus be drawn by adding the quantization error within the feedback loop.

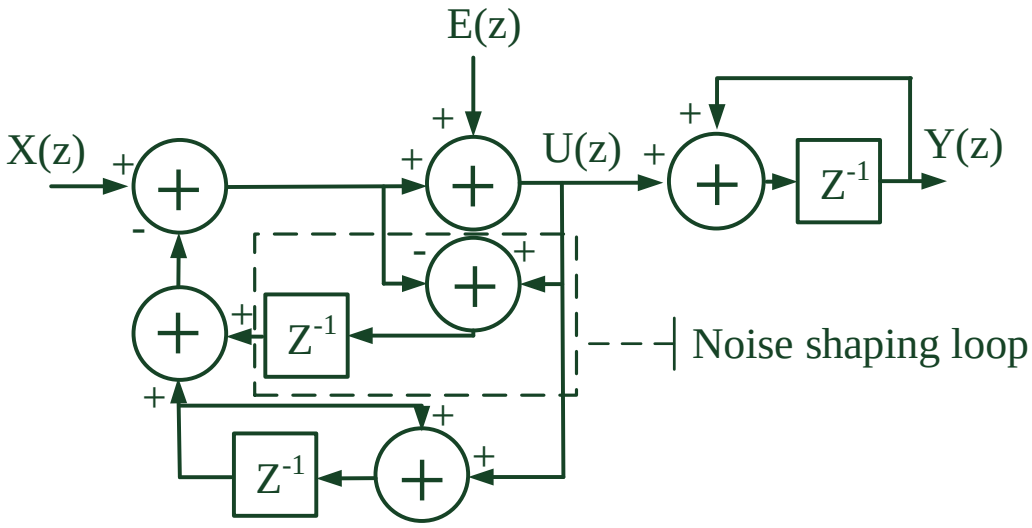

Figure 2.6: Noise Shaping Riemann Z-transform block diagram.

The transfer function of the derivative U with respect to the input signal X and to the quantization error E can thus be calculated, giving:

$$U(z) = X(z)(1 - z^{-1}) + E(z)(1 - z^{-1})^2 \tag{2.8}$$

And, when referring to the output signal Y:

$$Y(z) = X(z).z^{-1} + E(z).z^{-1}.(1 - z^{-1}) \tag{2.9}$$

The signal path simply presents a unit delay, whereas the noise transfer function corresponds to a delay and a high pass characteristic. The latter exhibits exactly the same modulus as the first order sigma delta topology and thus the same noise shaping is performed. Assuming an ideal analog low-pass filtering, the quantization noise power can be reduced by a factor proportional to the OSR cubed. The in-band quantization noise is determined by the same equation:

$${\sigma_n}^2 \approx {\sigma_e}^2 \frac{\pi^2}{3.OSR^3} \tag{2.10}$$

i.e:

$${\sigma_n}^2 \approx \frac{V^2.\pi^2}{(2^{2N} - 2^{N+1} + 1).OSR^3} \tag{2.11}$$

The expression of the corresponding SNR in dB is given by:

$$SNR_{dB} \approx 6.02N + 15.05r - 13 + 10log_{10}(1 - \frac{1}{2^{N-1}} + \frac{1}{2^{2N}}) \tag{2.12}$$

The filtering of out of band noise thus improves the OSR by 9.03r instead of 3.01r in the case of non-shaped white noise. The overall SNR in dB depends on the OSR through the term 15.05r,

the first part (6.02r) being related to the reduction of the quanta within the quantizer and the additional 9.03r coming from the filtering out of the shaped noise. Referring to equation 2.10, the noise shaping loop adds a $\frac{\pi^2}{3}$ factor in the expression of the in band quantization noise; the negative constant term in the expression of the SNR is thus emphasized up to -13 dB. This offset is easy to compensate in the case of a large OSR, or for a medium OSR and a sharp analog filtering.

One can notice this topology exhibits a first order noise shaping function. It is also possible to implement higher order noise shaping topologies by adding feedback loops that take into account more samples of the input signal. The result would be exactly the same than on sigma delta topologies: a high improvement of the SNR with respect to the OSR, but only in the case of high enough OSR. Furthermore, it would increase the system complexity, and degrade the stability of the conversion.

The Noise Shaping Riemann architecture described in this paragraph will be referred as **NSR** in the following sections of the manuscript.

2.1.3 RF conversion schemes summary

The differentiating conversion schemes presented in this section are compared together with the conventional schemes used in literature, in the domain of high speed DACs and flexible transmitters. Those schemes are decomposed according to their constitutive techniques, namely oversampling, noise-shaping and differentiating. The impact of the number of bits N involved in the conversion is the same for all the exposed schemes: an improvement of 6 dB in the SNR per extra bit. However, the effects of the OSR are different for all of them, and they are listed in Table 2.1. The conversion schemes can be decomposed according to 3 methods:

- **Oversampling**: it provides a slight improvement of the SNR and eases the filtering of the digital replicas by spreading the quantization noise floor on a larger frequency band.
- **Noise shaping**: it shapes the quantization noise out of the band of interest and provides a high improvement of the SNR, but it works properly with a high enough OSR and an efficient filtering. Only first order noise shaping is considered because the drawbacks are even more penalizing for higher order in the case of low OSR. Oversampling is a prerequisite to use noise shaping techniques.
- **Differentiating**: it brings an additional benefit that is compatible with the oversampling and noise shaping techniques. The only cost is a slight change in the quantization process and several precautions in the quantization and reconstruction process.

Table 2.1: Modulation features involved in the presented conversion schemes and the related impact of the OSR on the SNR.

	Oversampling	1^{st} **order Noise Shaping**	**Differentiating**	**TOTAL (dB)**
Impact on the SNR (dB)	3r	6r	6r	
Pros	Ease the filtering of the replicas	High impact on the SNR	Reduction of the total quantization noise	
Cons		Need of a minimum OSR and efficient filtering	Potential overload distortion and output drift	
PCM	x			3r
SDM	x	x		9r
Riemann	x		x	9r
NSR	x	x	x	15r

The use of differential codes is totally missing in the RF wireless transmitters field. The benefits of this kind of coding can help to reduce the complexity of the DAC for a given accuracy, so as to meet SR transmitter constraints in terms of power consumption. The OSR that is affordable is related to the technology used and the wanted bandwidth. Depending on its value, noise shaping can be added in the conversion. The implementation of this technique simply impacts the digital computation block; it remains compatible with the same topology of DAC. For all these reasons, we propose an architecture which relies on differentiating codes. The next section considers DAC features that are induced by the choice of this architecture and exposes the development of a suited RF-DAC topology, called the Riemann Pump.

2.2 The Riemann Pump: an integrating DAC

2.2.1 Implementation of the digital to analog integration

The presented differentiating conversion schemes generate bit streams that are representative of the derivative of the wanted signal. In the overall digital to analog conversion architecture, the DAC has to generate an analog version of the wanted signal by integration of its input digital signal. From an electronic point of view, the relation integral/derivative is embodied by the basic reactive passive components: capacitor and inductance. Those components are modeled by first order differential equations between the current i and the voltage v. Capacitors are easier to implement in integrated technologies and show better quality factors. Their fundamental equation is:

$$i = C\frac{dv}{dt} \tag{2.13}$$

Or:

$$\Delta v = \frac{1}{C} i \Delta t \tag{2.14}$$

Considering a low consumption system in recent integrated technologies, a coarse estimation of the range of the different terms in equation 2.14 gives:

- Δv # V
- **C** # pF
- **i** # mA
- Δt # ns (GHz)

Those orders of magnitude are compatible with the integrated technologies capabilities. It is then possible to reconstruct an RF voltage signal by integration of a current into a capacitor in this kind of technologies. In order to generate a varying signal, either the capacitance value or the current value can change. The integration of capacitors remains cumbersome with respect to active devices, especially as advanced technologies are considered. The generation of varying currents thus constitutes the most favorable solution (Fig. 2.7).

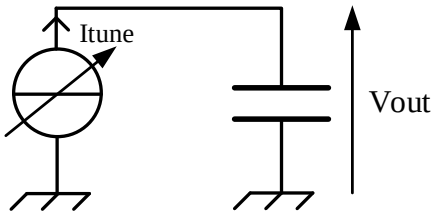

Figure 2.7: Signal integration principle.

The developed DAC architecture relies on the integration of a digitally controlled current generator and a capacitive load. The current generator is composed of binary weighted complementary switched current sources. The corresponding topology of the digital to analog conversion architecture is depicted in Fig. 2.8; it is composed of 2 main parts.

- **a DD** conversion block, where a differentiating coding is performed onto a digital representation of the wanted signal.
- **a DAC** which converts the digital bit streams representative of the derivative of the signal into a proportional analog current thanks to complementary switched current sources. The resulting current is integrated into a capacitor to generate the wanted signal.

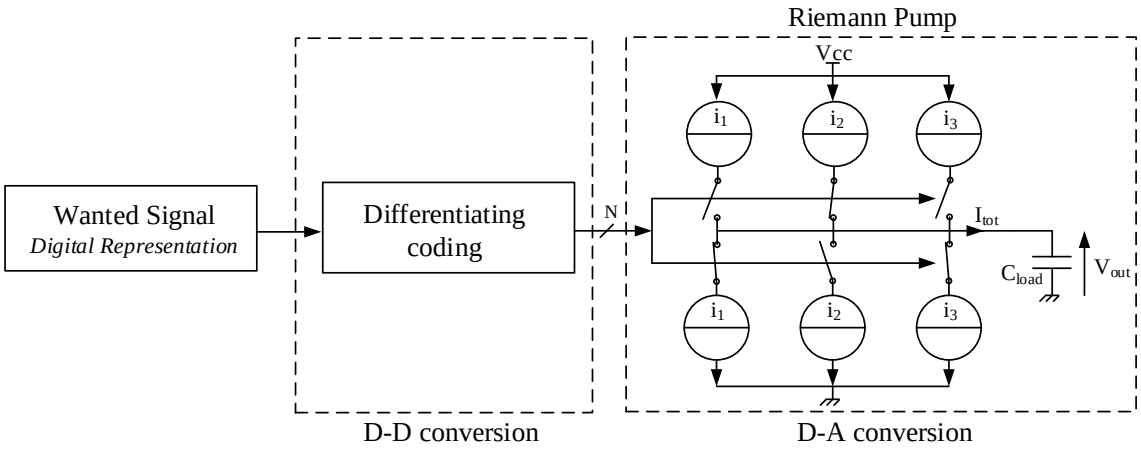

Figure 2.8: Riemann Pump Architecture.

This topology proposes to integrate constant current steps into a capacitive load. The resulting voltage across the load is thus a piecewise linear approximation of the wanted signal. The generation of a sine wave made of 8 slopes is illustrated in Fig. 2.9. The N bits digital stream is converted into a staircase current profile I_{out}, which is integrated into the output capacitor to produce the piecewise linear voltage V_{out}.

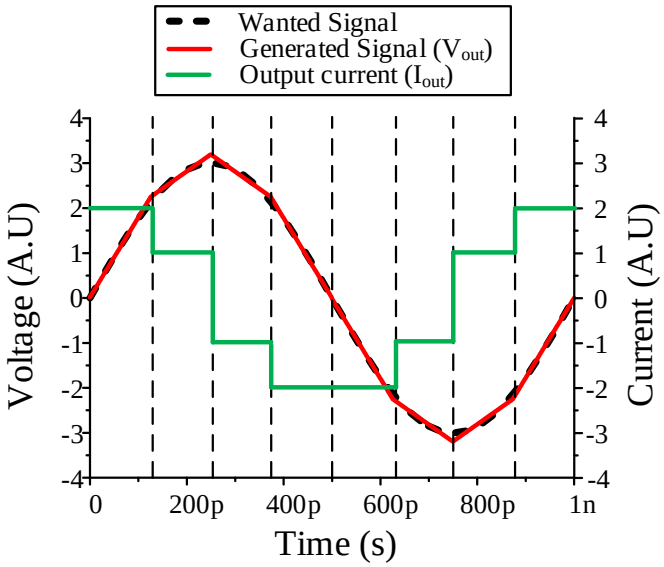

Figure 2.9: Generation of a sine wave with 8 slopes.

2.2.2 Analog reconstruction features

The spectrum of a digital signal is made of the baseband signal and replicas centered in the multiples of the sampling frequency f_s. The operation of digital to analog conversion acts as a reconstruction filtering, with most of the time a low pass characteristic. The impact on the spectrum is represented in Fig. 2.10.

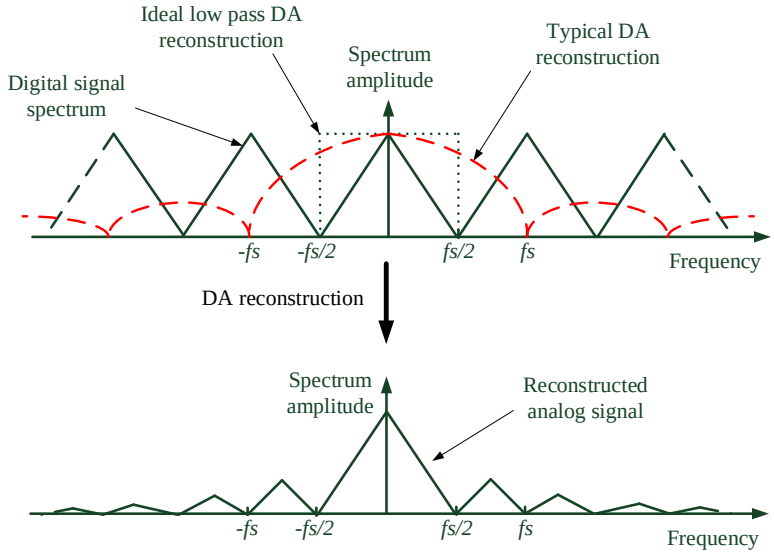

Figure 2.10: Impact of the DA reconstruction on the spectrum.

An ideal low-pass DA reconstruction would cancel all the replicas and preserve the baseband signal without any alteration. Actual low-pass DA reconstruction presents a non-ideal characteristic. It results in a reconstructed analog signal which is composed of the partially attenuated baseband signal and residues of the replicas. The characteristics of the filtering depend on the reconstruction method.

In the presented architecture, the Riemann Pump operates a linear interpolation to reconstruct the analog signal. The reconstruction process corresponds to a first-order hold, whose impulse response is represented in Fig. 2.11.

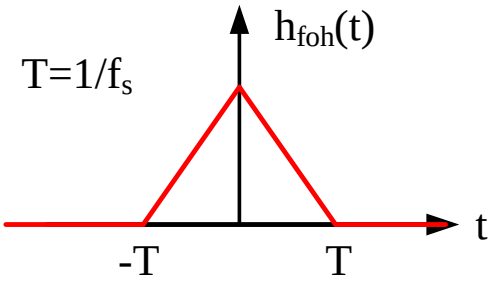

Figure 2.11: Impulse response of the equivalent first-order hold reconstruction.

The frequency response of this reconstruction scheme is the Fourier Transform of the impulse response, illustrated in Fig. 2.12.

$$H_{foh}(f) = F\{h_{foh}(t)\} = (\frac{e^{i\pi fT} - e^{-i\pi fT}}{i2\pi fT})^2 = sinc^2(\frac{f}{f_s}) \tag{2.15}$$

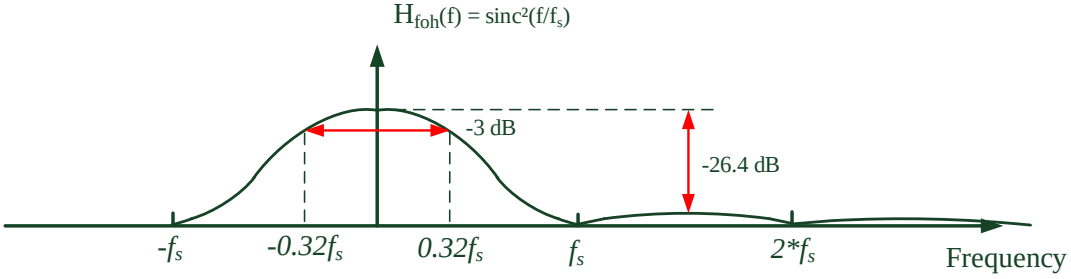

Figure 2.12: Frequency response of the first-order hold.

The first order hold reconstruction process performed by the Riemann Pump results in a squared cardinal sinus filtering. Most common DAC architectures operate as zero-order holds which generate a staircase signal. A comparison between zero order and first order holds is presented in Fig 2.13, and summarized in Table 2.2.

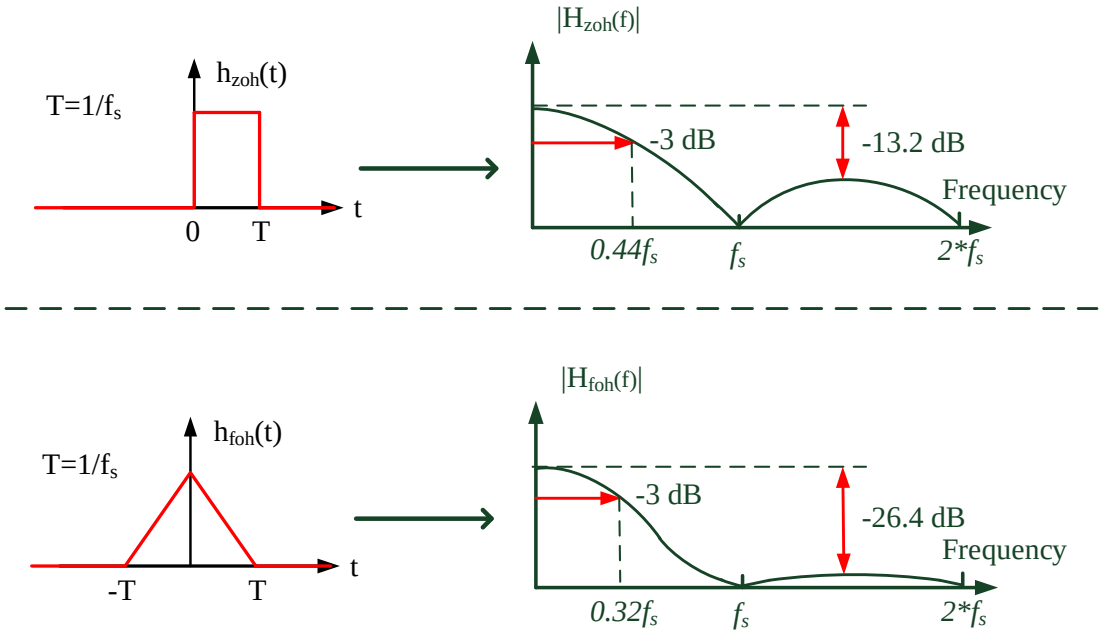

Figure 2.13: zeroth and first-order holds impulse and freuency responses.

Table 2.2: Features of the zeroth and the first-order holds.

	Zero order	**First order**
Impulse response	Square	Triangle
Frequency response	$sinc(\frac{f}{f_s})$	$sinc^2(\frac{f}{f_s})$
$-3dB$ **bandwidth**	$0.44f_s$	$0.32f_s$
$-1dB$ **bandwidth**	$0.26f_s$	$0.18f_s$
Corresponding r	0.94	1.5
1^{st} **lobe level**	$-13dB$	$-26.4dB$

The first-order hold provides a sharper filtering than the zero order hold; it results in a slightly reduced bandwidth. To limit the roll-off of the highest frequency components of the wanted signal (near f_{max}), a high enough OSR is to be used. The OSR parameter r should be higher than 1.5 to ensure an attenuation lower than 1 dB. The filtering profile of the first order hold however provides a better filtering of the out of band noise and of the digital images. It results in a cleaner output spectrum and relaxes the constraints on a further low-pass filtering.

2.3 Simulation of the Riemann Pump architecture

The theoretical expressions of the SNR calculated previously are reminded, both for the Riemann and for the NSR conversion.

$$SNR_{Riemann} \approx 6.02N + 9.03r - 7.8 + 10log_{10}(1 - \frac{1}{2^{N-1}} + \frac{1}{2^{2N}}) \tag{2.16}$$

$$SNR_{NSR} \approx 6.02N + 15.05r - 13 + 10log_{10}(1 - \frac{1}{2^{N-1}} + \frac{1}{2^{2N}}) \tag{2.17}$$

The theoretical features of the presented architectures encompass both the conversion scheme (DD) and the analog reconstruction (DA) process; they are listed in Table 2.3. Those characteristics are to be validated thanks to system simulations.

Table 2.3: Conversion architectures theoretical features summary.

Coding scheme	**Dependence of the SNR**			**Reconstruction filter**
	Total noise	/	**In-band noise**	
Riemann	6N	6r	3r	$sinc^2(\frac{f}{f_s})$
NSR	6N	6r	9r	$sinc^2(\frac{f}{f_s})$

In the following section, the system simulation flow is presented, including the signal generation process and the SNR calculation method. The simulation results are then compared to the theoretical performances, both for the Riemann and the NSR coding schemes. Finally, the ability to address concurrent transmission will be assessed through the application to sub-6 GHz 5G transmission schemes.

2.3.1 System simulation flow

2.3.1.1 Signal generation process

The system simulations are performed thanks to digital calculations, with the software Matlab. Fig. 2.14 presents the Matlab signal generation flow, which is decomposed in 4 steps.

- **Ideal signal generation**: the wanted signal is generated with a high digital resolution and a short time step, so that it can be considered as an ideal analog signal.

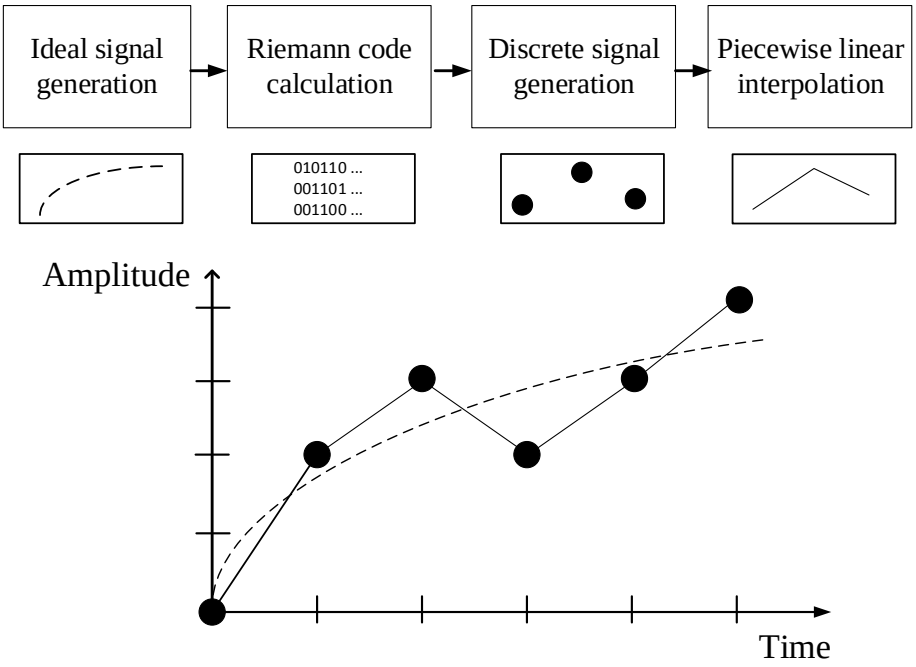

Figure 2.14: Matlab signal generation.

- **Riemann code calculation**: the Riemann (or NSR) algorithm is applied to the wanted signal, with a resolution of N bits at the working frequency f_s. This block generates the N bit streams corresponding to the sequence of slope which represents a piecewise linear approximation of the wanted signal.

- **Discrete signal generation**: this signal is the sampled version of the wanted signal. It corresponds to the discrete values of the piecewise linear signal at the sampling times. The spectrum of this signal contains the unfiltered quantization noise generated by the coding algorithm

- **Piecewise linear interpolation**: it corresponds to the linear interpolation of the previous discrete signal. It is representative of the voltage obtained by the ideal integration of the current steps into the output capacitor. This operation is equivalent to a first-order hold. It operates as a squared cardinal sine filter on the discrete signal spectrum.

2.3.1.2 SNR calculation

The SNR is the key metric to assess the signal generation performances. It is expressed as the ratio of the power of the useful signal P_s divided by the power of the noise P_n, with a logarithmic scale.

$$SNR_{dB} = 10log(\frac{P_s}{P_n}) \tag{2.18}$$

Temporal dimension

As far as signal generation is concerned, the noise can be considered as the error between temporal representations of the wanted signal y and the actually generated signal y_r. In this case, the power of the noise P_n is the power of the error signal $e = y - y_r$ (Fig. 2.15).

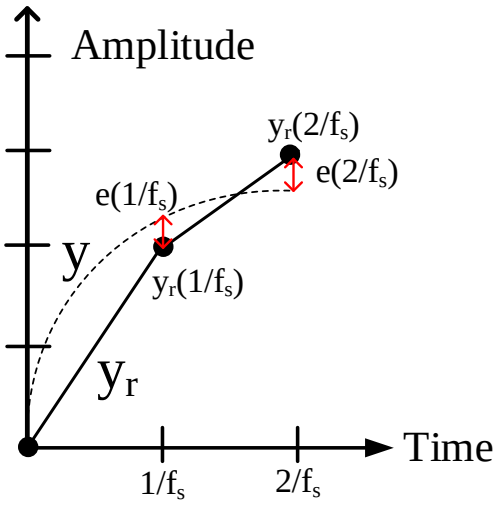

Figure 2.15: Temporal calculation of the SNR.

The power of the signal P_s over a time interval T is given by:

$$P_s = \frac{1}{T}\int_T y^2 dt \tag{2.19}$$

The power of the noise P_n is calculated as:

$$P_n = \frac{1}{T}\int_T (y - y_r)^2 dt \tag{2.20}$$

The resulting SNR equals:

$$SNR_{dB} = 10log(\frac{P_s}{P_e}) \tag{2.21}$$

For a sampled signal, the integral is replaced by a discrete sum:

$$SNR_{dB} = 10log\frac{\sum_{k=1}^{k_{max}} y(\frac{k}{f_s})^2}{\sum_{k=1}^{k_{max}} (y(\frac{k}{f_s}) - y_r(\frac{k}{f_s}))^2} \tag{2.22}$$

This formula of the SNR calculates the overall quantization noise. This temporal approach is used to determine the total quantization noise of the presented conversion schemes. However, it does not allow to assess the spectral distribution of the quantization noise and to distinguish the in-band from the out-of-band noise.

Frequential dimension

The usual conversion between the time and the frequency domain is performed by the Fourier transform (FT). It allows to obtain the spectrum of time varying signals (Fig. 2.16), which is noted:

$$X(f) = FT\{x(t)\} \tag{2.23}$$

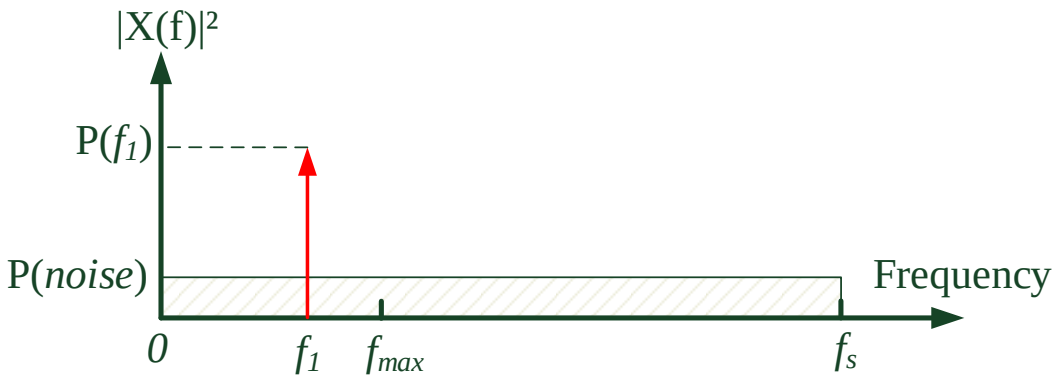

Figure 2.16: Spectral representation of a CW signal.

The energy of a signal does not depend on the chosen representation: temporal or frequential. This assertion is known as the Parseval identity, and is expressed as follows:

$$E = \int (|x(t)|^2 dt = \int (|X(f)|^2 df \tag{2.24}$$

The SNR of a signal which represents a continuous wave can thus be calculated as its power at the fundamental frequency divided by the power at all the other frequencies. Let y_r be the temporal approximation of a sine wave at the frequency f_1, and $Y(f)$ its FT. The SNR of this signal can be calculated as:

$$SNR = \frac{|Y(f_1)|^2}{\int_{[0,\infty]\setminus f_1} |Y(f)|^2 df} \tag{2.25}$$

It is also possible to calculate the SNR with respect to the in-band quantization noise only, by limiting the upper boundary of integration interval to f_{max}.

$$SNR_{inband} = \frac{|Y(f_1)|^2}{\int_{[0,f_{max}]\setminus f_1} |Y(f)|^2 df} \tag{2.26}$$

This frequential approach is used to determine the quantization noise of a generated signal within a given frequency band. It allows to get rid of the out-of-band noise in the calculation of the SNR.

2.3.2 SNR performances: simulation results versus theory

The SNR is calculated for the generation of a full scale sine wave of frequency f_{out}. It is assessed for different values of the key parameters (r, N and f_{out}), as represented in Fig. 2.17.

SNR versus the number of bits N

The resolution of a converter is usually expressed in effective number of bits (ENOB). 1 effective bit corresponds to 6.02 dB in the SNR. Usual converters exhibit a SNR which depends on 6.02N.

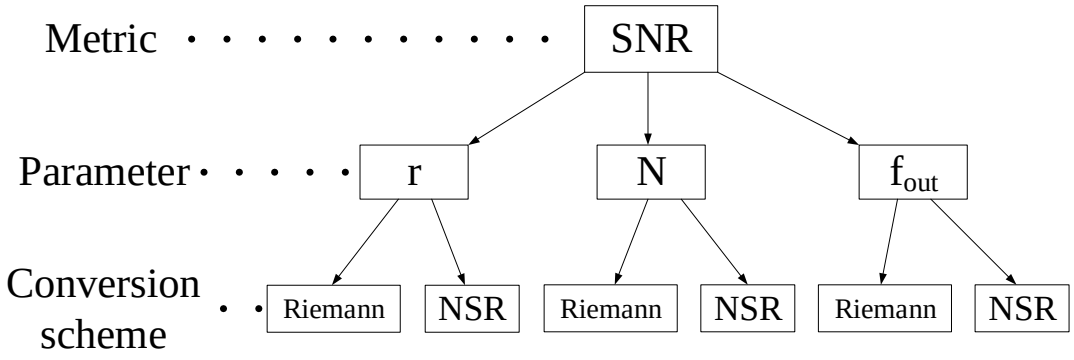

Figure 2.17: SNR Simulation chart.

The two presented conversion schemes (Riemann and NSR) present a similar dependence, plus an additional $10log_{10}(1 - \frac{1}{2^{N-1}} + \frac{1}{2^{2N}})$. This extra term becomes negligible when N is greater than 3.

- **Riemann**

  A sine wave is generated thanks to the Riemann algorithm, with an OSR set to r=2 and a variable number of bits N. Results exposed in Fig. 2.18 compare the simulations to the theoretical formula of the SNR established previously for the Riemann algorithm.

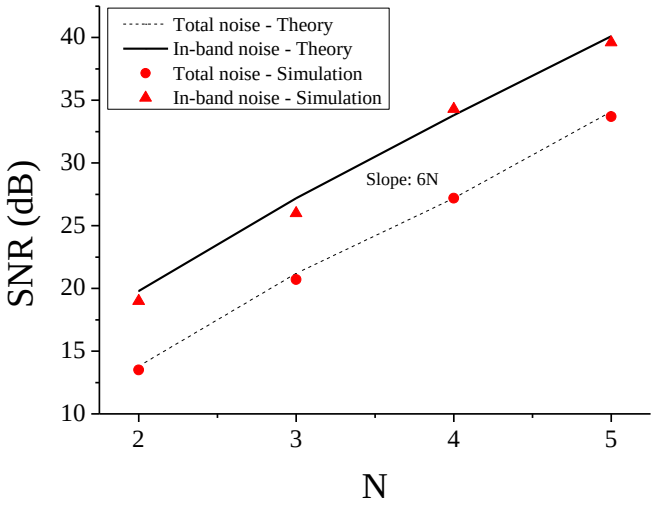

Figure 2.18: SNR of the Riemann conversion versus N / r=2.

The total quantization noise is calculated onto the discrete signal with samples given at the frequency f_s. The in-band noise is calculated onto the piecewise linear reconstructed

signal by integration of the spectral power density up to f_{max}. The SNR including the total quantization noise perfectly fits the theoretical formula. The in-band noise related SNR is also consistent with the formula. It confirms the claims about the uniform distribution of the quantization noise over the frequencies.

- **NSR**

  Fig. 2.19 exposes the same study for the NSR algorithm.

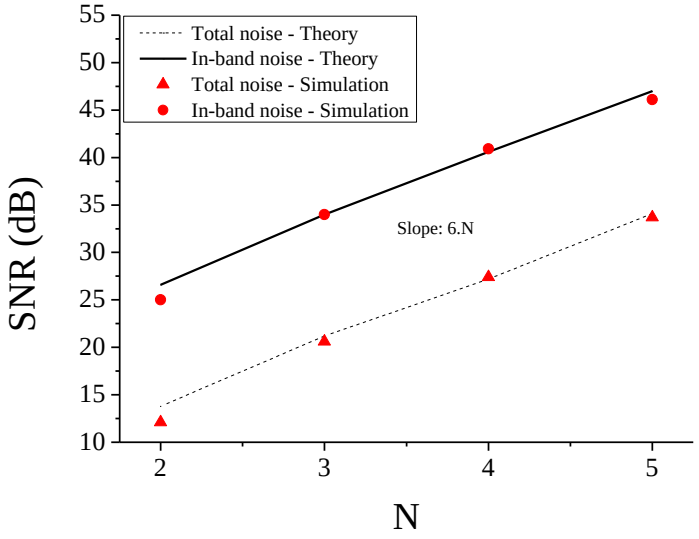

Figure 2.19: SNR of the NSR conversion versus N / r=2.

The impact of N on the SNR is also consistent with the theory for the NSR algorithm, both considering the total and the in-band noise.

The slope of $6.02N$ is common to all the classical conversion schemes. The actual benefit of the presented ones is related to the OSR.

SNR versus the oversampling factor r

- **Riemann**

  The Riemann conversion benefits from the differential coding through a term 6.02r, plus an additional 3.01r when restricting to the in-band noise.

  The discrete signal reaches the expected value of SNR (Fig. 2.20). The in-band noise results in a SNR which has the same behavior as in theory. It is comprised in a $+/-1dB$ interval.

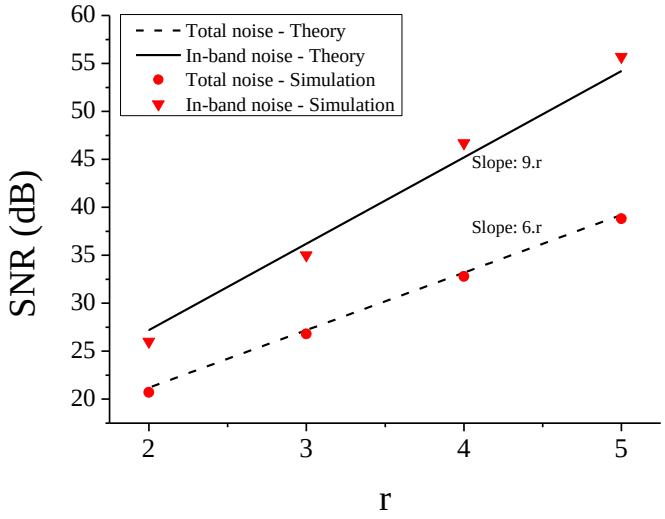

Figure 2.20: SNR of the Riemann conversion versus r / N=3.

- **NSR**

  The impact of the oversampling on the SNR is expressed through the term 15.05r in the SNR theoretical formula. This behavior is confirmed by the simulations presented in Fig. 2.21.

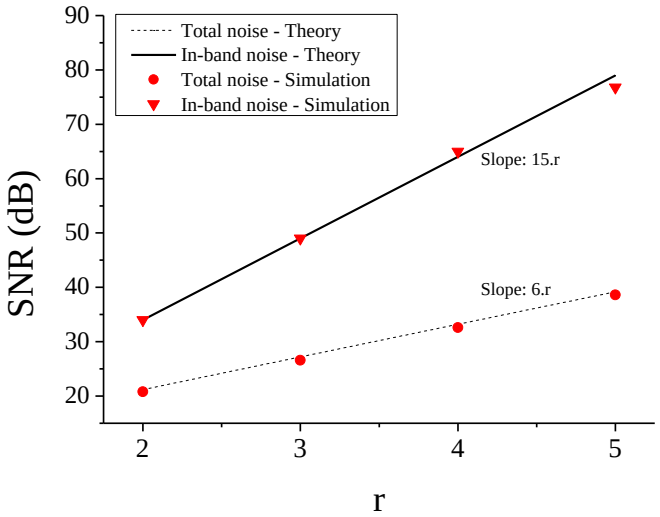

Figure 2.21: SNR of the NSR conversion versus r / N=3.

Both the total noise and the in-band noise lead to SNR values which fit the theoretical formulas. The in-band noise validates the noise shaping model used in the theoretical description of the NSR conversion scheme.

The system simulations confirm the expected impact of the OSR on the conversion performances in terms of SNR; it validates the claims of conversion efficiency.

SNR versus output frequency

For a given set of parameters (r,N), the output bandwidth is $f_{max} = \frac{f_s}{2^{r+1}}$. The SNR is calculated for the generation of sine waves up to f_{max} in order to assess the performances of the system versus frequency. It is assessed for the generated signal at 3 stages:

- **Discrete signal**: it contains all the quantization noise.
- **Piecewise linear signal**: it contains all the quantization noise filtered by a first order hold reconstruction filter ($sinc^2$).
- **Band limited piecewise linear signal**: it contains only the quantization noise in the [0 - f_{max}] band.

This study is led both for the Riemann and NSR conversion schemes.

- **Riemann**

  Fig. 2.22 presents the results for the Riemann conversion.

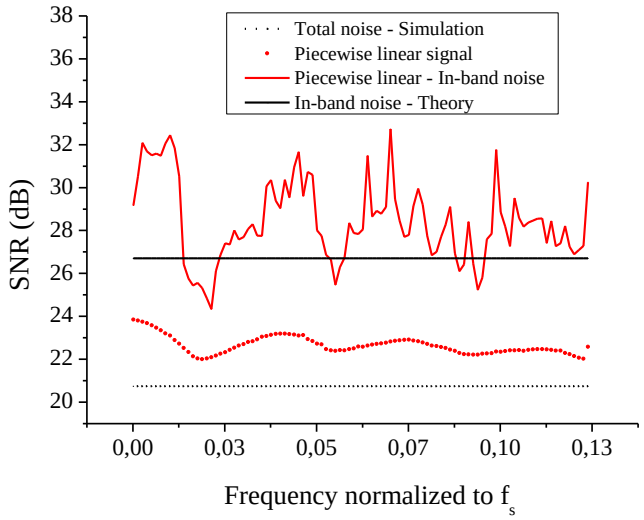

Figure 2.22: SNR of the Riemann conversion versus frequency (r,N)=(2,3).

The total quantization noise is constant over the whole band; it results in a constant SNR which matches with the theoretical value of barely 21 dB. The piecewise linear reconstructed signal has a slightly higher SNR, from 1 to 3 extra dB with respect to the

discrete signal. It is due to a first filtering of the quantization noise performed by the piecewise linear interpolation. It multiplies the discrete signal spectrum by a $sinc^2(\frac{f}{f_s})$ filter, as shown in Fig. 2.23.

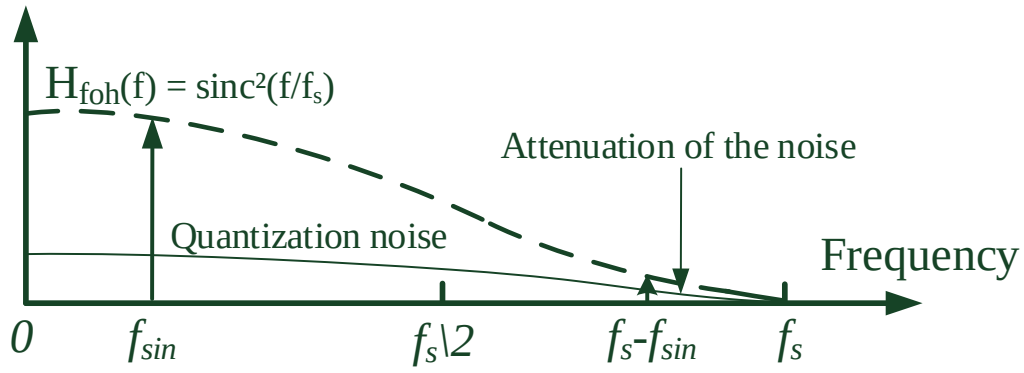

Figure 2.23: Piecewise linear CW spectrum – Riemann conversion.

The quantization noise is distributed over the whole sampling frequency band and the noise situated near f_s is significantly attenuated. As a result, the SNR of the linearly interpolated signal is significantly higher than the one of the discrete signal. Furthermore, this SNR is not constant over the whole band but it varies along the frequency axis. It is related to the nature of the generated signal: a continuous wave (CW). The quantization noise could be uniformly distributed over the frequencies for a random signal but CW are all but random. The arithmetic relationship between the sampling period $t_s = \frac{1}{f_s}$ and the output CW period $T_{out} = \frac{1}{f_{out}}$ plays an important role in the spectral repartition of the quantization noise. If there is an integer relationship, a greater part of the global power is located at the harmonic and intermodulation frequencies. The amount of spurious tones filtered by the reconstruction operation thus depends on the frequency of the CW.

The in-band noise depends even more on the frequency, because the spurious are likely to be situated inside and/or outside of the band of interest. Nevertheless, the simulations lead most of the time to more favorable results than the theoretical formula, while being situated around the expected level of SNR.

- **NSR**

Fig. 2.24 presents the similar study for the NSR conversion.

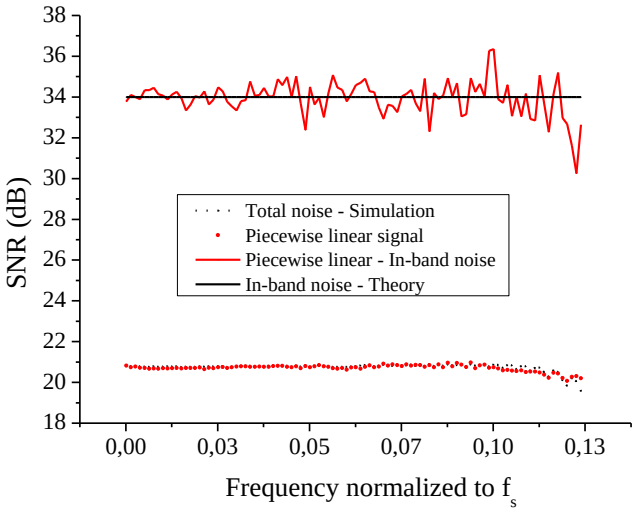

Figure 2.24: SNR of the NSR conversion versus frequency (r,N)=(2,3).

For the NSR conversion, the discrete signal and the piecewise linear signal exhibit a similar SNR, almost constant over the whole frequency band and close to the theoretical value of 21 dB.

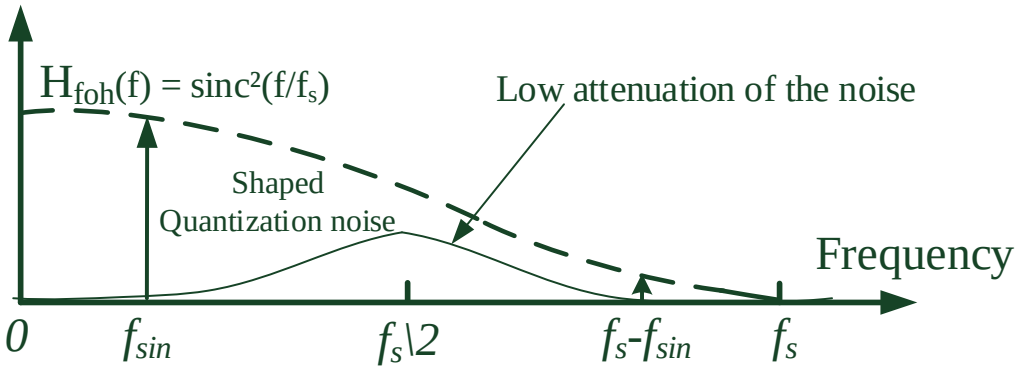

Figure 2.25: Piecewise linear CW spectrum – NSR conversion.

The quantization noise is pushed to the highest frequency (i.e $\frac{f_s}{2}$) as represented in Fig. 2.25. The sampling image centered in f_s has also a shaped quantization noise close to $\frac{f_s}{2}$. The major part of the quantization noise is thus situated around this frequency, where the $sinc^2(\frac{f}{f_s})$ filtering is not severe. The reconstruction step does not significantly improve the SNR with respect to the discrete signal.

When considering only the in-band noise, the SNR jumps around 34 dB over the whole frequency band, which is the theoretical value. The dependence in frequency is weaker than in the previous case, because it is masked by the noise shaping.

Conclusion

The SNR performances have been assessed through the generation of CW. Matlab simulations of signal reconstruction validate the theoretical study developed previously, both for the Riemann and the NSR conversion. It endorses the proposed formulas of SNR for those two architectures. It helps to set the parameters of the system -namely N and r- to reach the specifications of potential standards.

2.3.3 Concurrent transmission

This section proposes to assess the ability of the developed architectures to address concurrent transmission of modulated signals. The case of sub-6 GHz 5G carrier aggregation schemes is considered in the following. The performances of the Riemann and the NSR are compared toward this application.

Sub-6 GHz 5G technical features

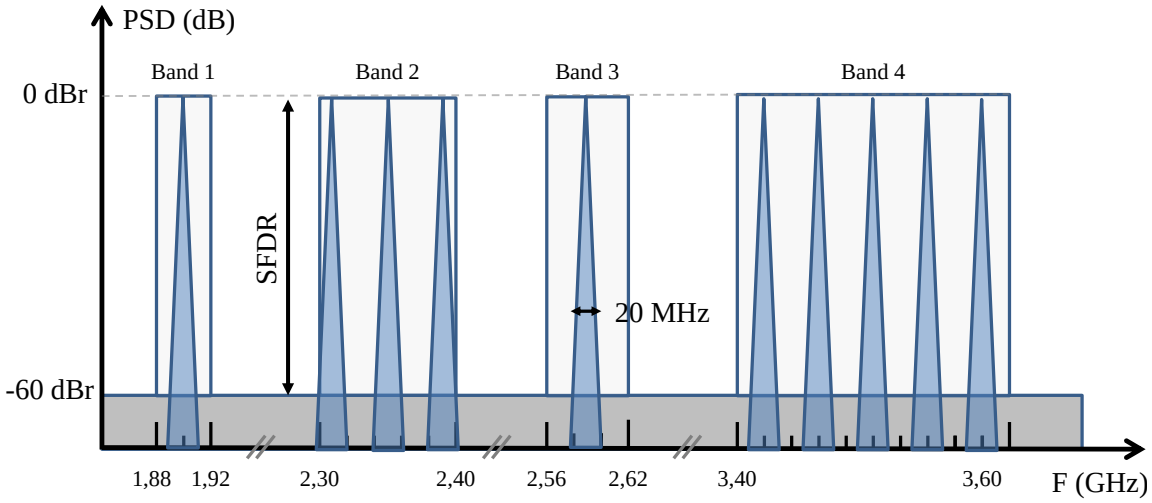

Figure 2.26: First phase of the sub-6 GHz 5G spectral mask.

The 5G infrastructures will rely on a densification of the cells, with different level of granularity, i.e different sizes. It will use different frequency bands, respectively the sub-6 GHz band which is

an evolution of the LTE standard, and also mmW bands above 10 GHz for short-range communications. The target of our system is to address the first phase of sub-6 GHz communications. The spectrum assignment is expected to be divided into 4 disjoint bands, represented in Fig. 2.26.

So as to increase the data rate, carrier aggregation technique will be used. It consists in sending a digital signal over multiple carriers, possibly located in different frequency bands. The useful data is divided onto those carriers and all the signals have to be synchronized to preserve the data integrity. The transmitted signal could combine up to 10 aggregated carriers, using 64 to 256 QAMs in 20 MHz width channels. The transmission mask should respect a spurious-free dynamic range (SFDR) of 60 dB over the whole band. The suitability of our signal generation architectures will be assessed for this application.

Generation of 10 aggregated carriers

A reference signal composed of 10 aggregated carriers modulated with 64-QAMs is generated with Matlab. The piecewise linear approximation of this composite signal is then computed, either with the Riemann or the NSR algorithm, with a given set of parameters (r,N). The synchronization of the carriers is inherently ensured because the modulated signals are generated all together in a single waveform. The spectrum is then computed to collect the SFDR; it is given by the difference of level in dB between the modulated signals and the noise floor. The 10 modulated signals can be demodulated with a suitable chain coded with Matlab to obtain their constellation and the associated error vector magnitude (EVM).

- **Riemann conversion**

  The spectrum obtained with the Riemann conversion for a sampling frequency of 50 GHz and a number N of 6 bits is displayed in Fig. 2.27.

  The noise floor is flat over the whole band and located at 55 dB under the level of the channels, the SFDR for this signal is thus 55 dB. The constellation obtained after the demodulation of the channel centered at 3.5 GHz is presented in the same figure. The obtained EVM is approximately 1%, which represents a good figure for usual modulations used in wireless communications.

  Fig. 2.28 displays the SFDR obtained with the Riemann algorithm versus the number of bits N and the sampling frequency f_s.

  The behavior of the SFDR for the generated signal is exactly the same as the SNR, i.e an improvement of 6 dB per additional bit and 9 dB per doubling of the sampling frequency. The assumption of a uniform distribution of the quantization noise floor over the

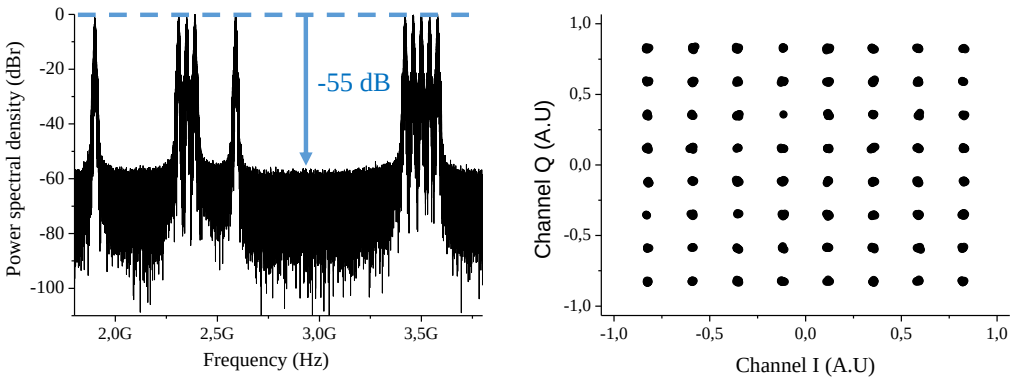

Figure 2.27: Spectrum of 10 aggregated channels – Riemann conversion (f_s, N)=(50 GHz, 6).

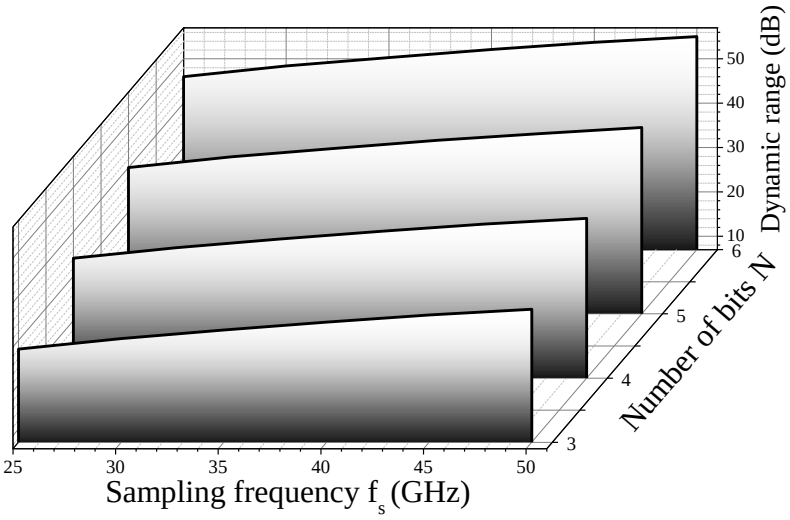

Figure 2.28: SFDR for 10 aggregated channels – Riemann conversion.

frequencies is validated by simulation (see Fig. 2.27). In this case the SFDR and the SNR evolve similarly; the noise floor is repelled while the SNR increases. The figure of 60 dB of SFDR is barely reachable with the maximum simulated settings, f_s=50 GHz and N=6.

- **NSR conversion**

  The same study has been led with the NSR algorithm. The obtained spectrum and constellations are displayed in Fig. 2.29. The spectrum matches with the 5G requirements in terms of SFDR with 67 dB of SFDR. The EVM is approximately 0.9%.

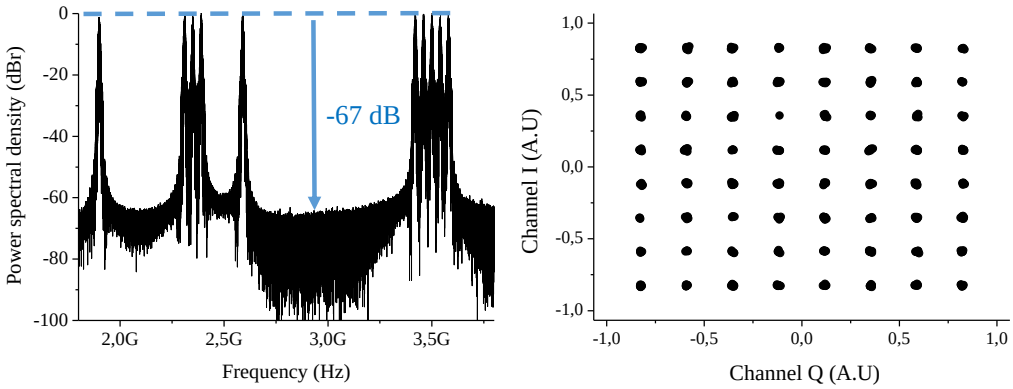

Figure 2.29: Spectrum of 10 aggregated channels – NSR conversion (f_s, N)=(50 GHz, 6).

The sweep of the sampling frequency f_s and the number of bits N is exposed in Fig. 2.30. The obtained SFDR values also fit the theoretical SNR behavior with a dependance in 6N and 15r. The noise shaping provides a significantly better SFDR than the classical Riemann conversion for the highest sampling frequencies.

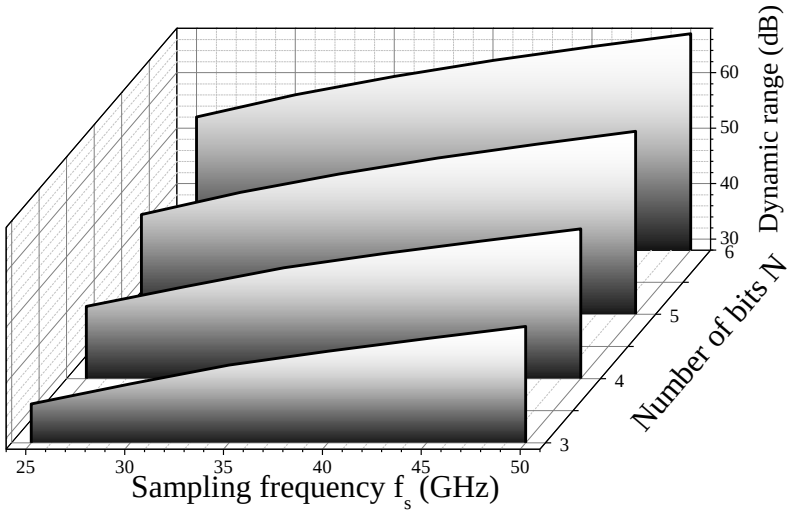

Figure 2.30: SFDR for 10 aggregated channels – NSR conversion.

Variation of the number of carriers

The configuration with 10 carriers is the worst case; the system could operate with an arbitrary number of carriers. The SFDR is reported versus the number of carriers, for both the Riemann and the NSR conversions with the parameters (f_s, N)=(50 GHz, 6).

Table 2.4: SFDR versus the number of aggregated carriers - (f_s, N)=(50 GHz,6).

Number of carriers	**2**	**4**	**6**	**8**	**10**
$SFDR_{Riemann}$ (dB)	62	59	57	56	55
$SFDR_{NSR}$ (dB)	74	71	69	68	67

The power of the useful signal is shared between the channels. The SFDR is improved by 3 dB when the number of channels is halved. The improvement of the SFDR in dB with respect to the 10 carriers configuration follows the equation 2.27.

$$SFDR_{Mchannels} = SFDR_{10channels} + 10log(\frac{10}{M}) \tag{2.27}$$

The simulations are consistent with the theoretical features; it enables to adjust the parameters of the system to address the requirements of the application. In the case of sub-6 GHz 5G, the NSR conversion with a number of 6 bits is needed, with a working frequency between 40 GHz and 50 GHz.

2.4 Conclusion

Efficient DA conversion schemes based on differentiating coding have been exposed. They take advantage of a relative coding, eventually combined with noise shaping, to improve the conversion performances. It leads to a more favorable trade-off between system complexity and conversion performances than usual conversion schemes implemented in state of the art RF DACs. The underlying theory has been developed, and validated thanks to system simulations; it allows to set the key parameters of the system, namely the number of bits N and the OSR, for a given application with its own specifications.

The system has been assessed for the expected sub-6 GHz 5G stringent requirements. The generation of 10 intrinsically synchronized aggregated carriers with a SFDR of 60 dB could be addressed with the following characteristics:

- **Conversion scheme**: Noise Shaping Riemann
- **Number of bits**: 6
- **Conversion frequency**: f_s=40 GHz

Those features could be compatible with the latest CMOS technologies capabilities. However, our purpose is to bring a proof of concept. Chapter 3 exposes the design flow of Riemann Pump demonstrators implemented in different technologies. It presents the schematic and layout design, with the associated simulation results.

Chapter

3 Circuits design and Implementation

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Chapter 3 presents the integration of the Riemann Pump in two technologies. The first one is a GaN technology, dedicated to military applications. The second one is a 65 nm CMOS technology, dedicated to address the mobile market requirements. For each target technology, the design of the Riemann Pump is exposed from the topology to the layout. Post layout simulations are exhibited to assess the impact of the implementation and determine the key performances in terms of area and consumption.

Key words: Circuit design, CMOS, GaN, Layout, Post-layout simulations, RF-DAC

3.1 Integration in GaN technology

The generation of specific waveforms is of particular interest for RADAR applications. A signal generator based on the Riemann Pump architecture would provide an absolute flexibility for the generated waveform.

3.1.1 GaN technology

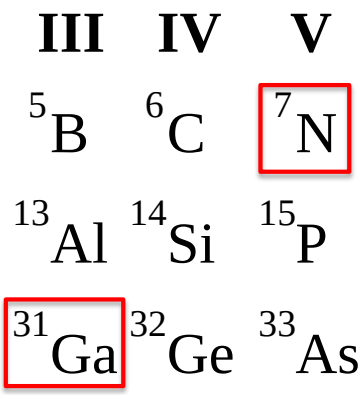


Figure 3.1: GaN atomic composition

GaN is a III-V semi-conductor (Fig. 3.1) with features of interest for the electronic industry.

Table 3.1: GaN principal features for RF electronics.

Features	**Assets**
High mobility	High speed, low losses
High bandgap	High power, EM robustness
High breakdown voltage	Supports high voltages
High thermal conductivity	Heat evacuation

The realization of heterostructures AlGaN/GaN enables the development of HEMT transistors [50] [51] [52]. The heterojunction forms a Schottky contact and spontaneous piezoelectric polarization induces the accumulation of a 2 degrees electron gas. It forms a channel close to the interface, in the GaN layer as represented in Fig. 3.2.

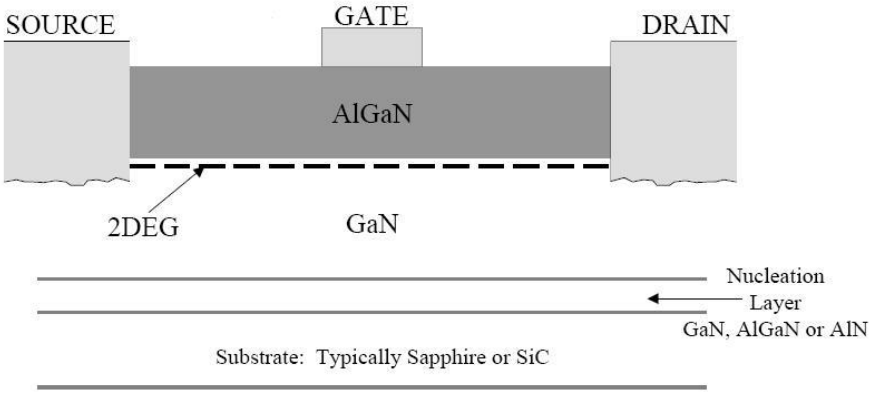


Figure 3.2: GaN HEMT sectional view

This layer is doping free. It ensures a low resistivity and thus a limited heat dissipation. High voltage operation is allowed by the high breakdown voltage; the natural application of those transistors is turned to high frequency power amplification [53] [54] [55]. Furthermore, the high bandgap gives resilience toward radiations and temperature [56] [57]. The robustness of GaN devices is suited to operation in harsh environments. It applies to military applications where reliability is a major constraint.

The transistors available on the used technology are only N-type HEMTs, there is no complementary P-type transistor. They are normally on, with a negative pinch off voltage, and they can handle more than 10 V between the drain and the source.

Typical characteristics of N-type HEMT transistors are displayed in Fig. 3.3.

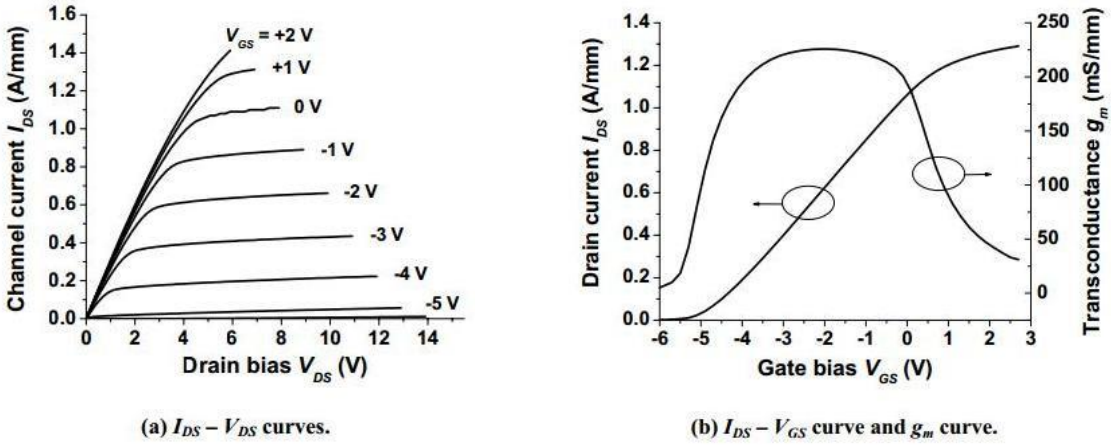


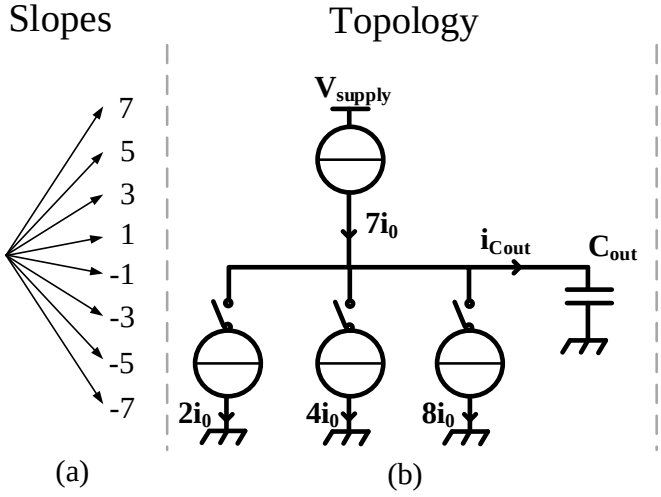
Figure 3.3: Electrical characteristics of N-type HEMTs

3.1.2 Riemann Pump in GaN technology

A first version of the Riemann Pump is designed in GaN with a technology from UMS, using ADS simulation environment. The purpose is to drive a Power Amplifier (PA) directly with the pump in order to integrate the whole analog part of the transmitter into a single chip. In this configuration, the capacitive input impedance of the power amplifier replaces the output capacitor of the Riemann Pump. The circuit described herein solely corresponds to the Riemann Pump alone.

Regarding circuit design techniques, the most important feature is related to the nature of the transistors. Only normally-on N-type transistors are available which impacts the circuit design. Furthermore, those transistors have a negative threshold of several Volts and a consequent size, limiting their switching speed. Those constraints help us to choose the parameters r and N that will be used for the GaN circuit. A trade-off between circuit complexity and conversion performance leads to a number N of 3 bits. The frequency limitations enable a switching frequency of 8 GHz, allowing the generation of signals up to 1 GHz with an OSR of 4 (i.e. r=2).

In the following, the couple of parameters (r,N) = (2,3) will be used. 3 coding bits enable to define a set of 8 slopes corresponding to the values of the DPCM quantizer. The steepest ones (respectively positive and negative) are calibrated with respect to the wanted dynamic and the switching frequency used. The 6 intermediate slopes are then distributed uniformly in between.



$8.i_0$	$4.i_0$	$2.i_0$	Slope
0	0	0	7
0	0	1	5
0	1	0	3
0	1	1	1
1	0	0	-1
1	0	1	-3
1	1	0	-5
1	1	1	-7

Figure 3.4: Slope set generation

The relative value of the slopes is represented in Fig. 3.4(a). They observe a constant step between them. The circuit architecture implemented to generate those slopes is presented in Fig. 3.4(b). The absence of P-type transistors in the targeted technology makes the realization of switches on the top rail inefficient. The developed Riemann Pump topology thus uses only switches on bottom rail current sources, whereas the top rail supplies a constant current. The current i_0 is used as a reference that depends on the calibration of the maximum slopes. The top supply rail delivers a current $7i_0$, while the bottom rail pulls a current depending on the state of the 3 switches controlled by the 3 coding bits. The resulting current which equals the sum of the pushed current and the pulled current goes into the output capacitor. The lower current sources are calibrated in order to generate the wanted slope distribution described above. Respective values of $2i_0$, $4i_0$ and $8i_0$ lead to the wanted slope set, depicted in Fig. 3.4(c).

The Riemann Pump topology is exposed more precisely in Fig. 3.5. The bottom current sources are derived from a unique source which pulls $14i_0$, while the top source is mirrored from another bottom source that generates $7i_0$. Differential switches are placed on the 3 current branches, so as to pull the corresponding current either from the output capacitor (when the switch is closed), or from the supply (when the switch is open). The current $7i_0$ is pushed continuously

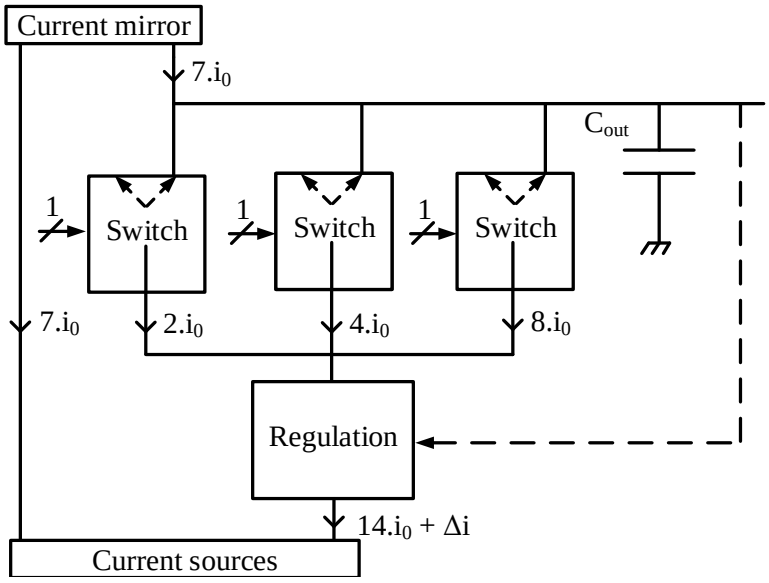


Figure 3.5: Riemann Pump topology in GaN

from the top supply rail. The output capacitor voltage represents the reconstructed signal. It results from the integration of the constant current steps. Since the system is pumping charges into the capacitor, any imbalance between the rails could cause a drift of the output voltage. To prevent this effect, a regulation block is inserted onto the bottom current source; it ensures the mean voltage across the output capacitor remains constant by balancing the bottom rail current generation with respect to the top rail current. It provides robustness to temperature and technological dispersion. The generation of constant or low frequency signals when the regulation is on is excluded, because the regulation loop filters the low frequencies. Nevertheless, this is not inconvenient for modulated signals generation.

3.1.3 Transistor level design

The transistor level schematic is depicted in Fig. 3.6. This representation can be divided into 4 main blocks.

- **Top rail current generation**
- **Bottom rail current generation**
- **Switching stage**
- **Mean voltage regulation**

Input buffers are required to ensure the interface between the bit stream generator and the switches of the Riemann Pump.

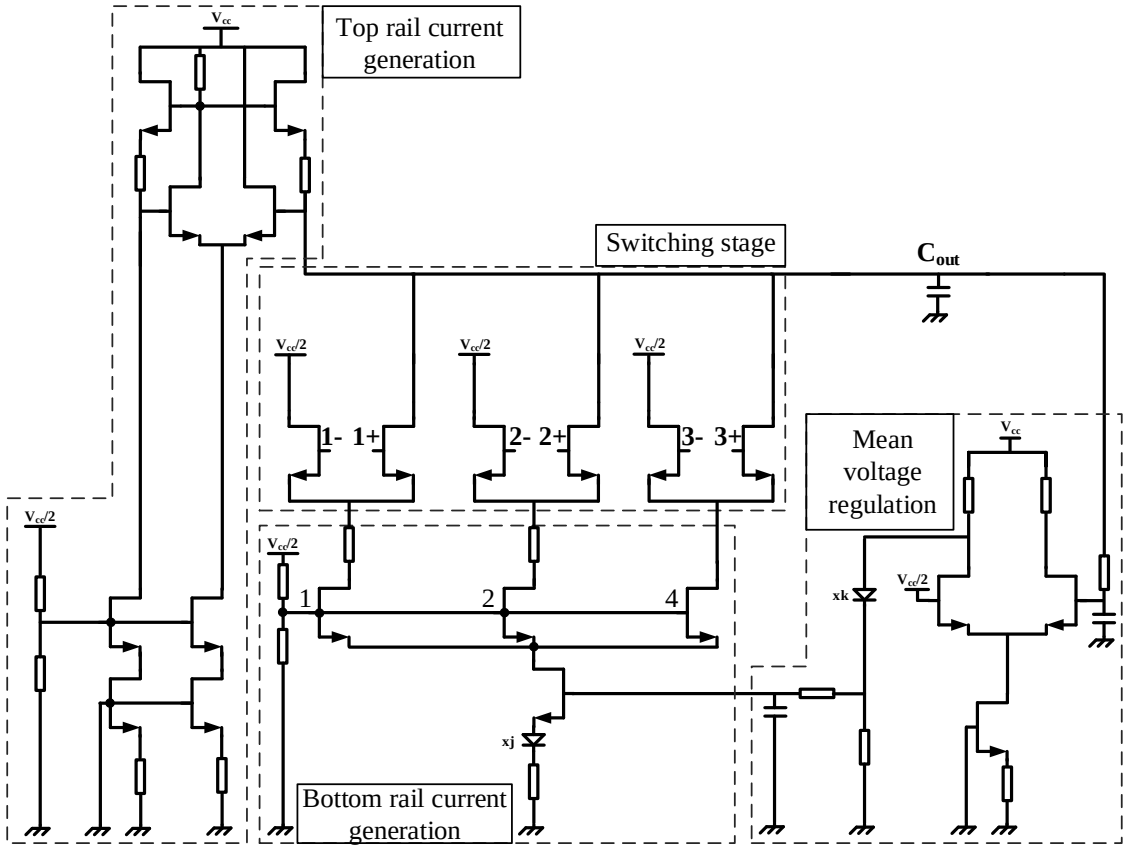


Figure 3.6: GaN circuit schematic view

Top rail current generation

The top rail current generation block is depicted in Fig. 3.7. The goal of this block is to generate a constant current i_{out} for any output voltage V_{out} (within the wanted dynamic centered in $\frac{V_{cc}}{2}$). The lower part of the block is dedicated to the generation of current through 2 cascoded current sources (respectively formed by Tr_1, Tr_2 and Tr_3, Tr_4). The resistors R_1 and R_2 provide the appropriate gate voltage for the cascode stage. The resistors R_3 and R_4 give the right gate to source voltage so as to generate the wanted current in each of the 2 branches. The left branch pulls a constant reference current iref. The upper part realizes the function of a current mirror with only N-type transistors. The differential pair (Tr_5, Tr_6) has a large enough gain so that the voltage V_{ref} remains almost equal to the voltage V_{out} when this latter varies. The 2 branches (R_5, Tr_7) and (R_6, Tr_8) being symmetric, the current iout turns out to be constantly equal to the reference current iref in the desired range of the output voltage V_{out}.

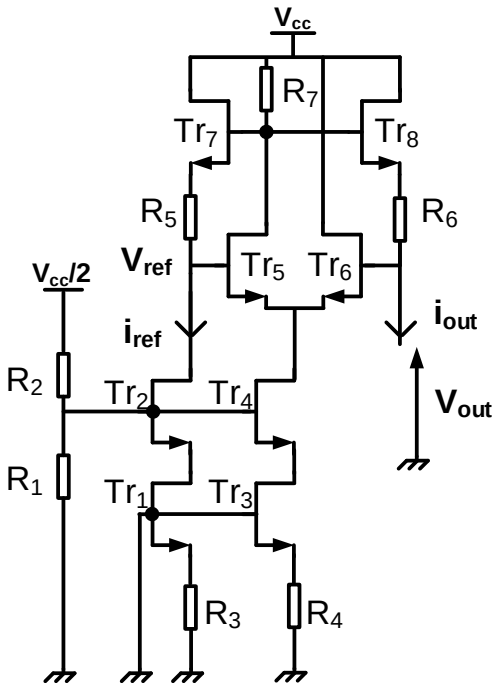


Figure 3.7: Top rail current generation

Bottom rail current generation

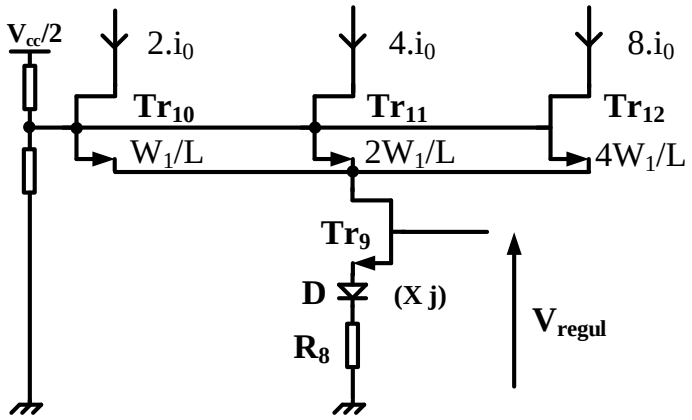


Figure 3.8: Bottom rail current generation

The total bottom rail current is determined by the gate polarization of the transistor Tr_9. A set of diodes is associated in series with the resistor R_8 to set the right polarization for the source. The ad-hoc generated current is then split into 3 paths, consisting of the transistors Tr_{10}, Tr_{11}, and Tr_{12}, of relative width 1, 2, and 4 respectively. Those currents then go through a switching

stage (Fig. 3.9).

Switching stage

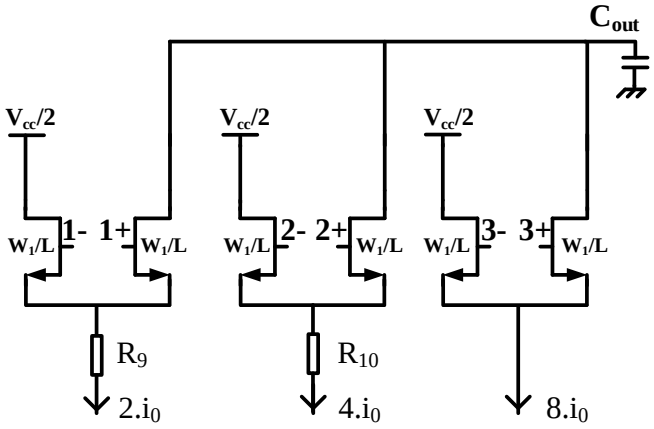


Figure 3.9: Switching stage

Depending on the state of the differential switches, which consist of differential pairs, the currents are pulled from the output capacitor or from the power supply source. This stage converts the differential input bit streams (1, 2, and 3) into the corresponding current, which is integrated together with the top rail current in order to reconstruct the wanted signal. The 3 differential switches are all sized with the minimum width W1 to minimize the loading capacitance of the digital command and optimize the switching speed. However, the 3 branches are pulling a different current, thus the voltage drops induced over the repective switches are different. To compensate for these discrepancies, resistors R_9 and R_{10} are added to balance the voltage drops on the 3 branches and ensure a proper splitting of the current. The mean value of the output voltage is then regulated to avoid any low drift of the capacitor charge. This is the role of the block presented in Fig. 3.10.

Mean voltage regulation

The output voltage is averaged thanks to the low pass filter (R_{11}, C_1). The obtained voltage is compared to the middle value $\frac{V_{cc}}{2}$ through a differential pair (Tr_{14}, Tr_{15}), polarized with the current source formed by the transistor Tr_{13} and the resistor R_{12}, and charged by the resistors R_{13} and R_{14}. The output voltage of the differential pair is shifted via a bridge formed by several diodes and the resistor R_{15}. This voltage then passes through a loop filter (C_2, R_{16}) calibrated to ensure stability of the regulation. When the mean value of the output signal increases, the output of the differential pair increases too; and the regulation voltage V_{regul} raises as well. It

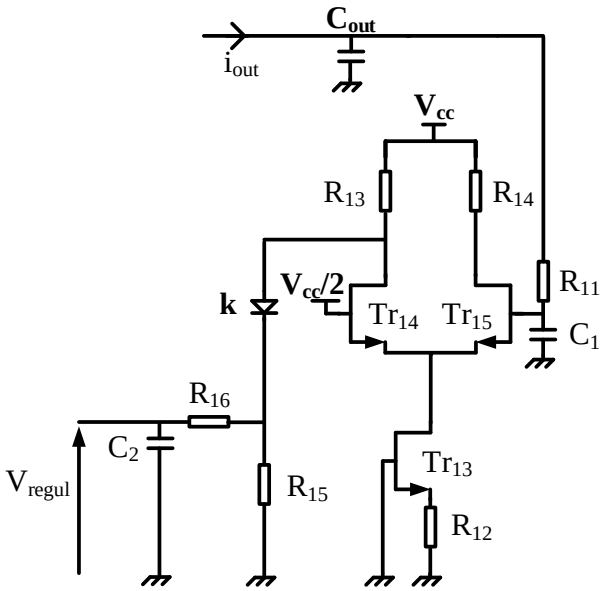


Figure 3.10: Regulation loop

induces an increase of the current pulled by the bottom rail, which lowers the average charge injected into the output capacitor, thereby reducing its mean voltage. The regulation block operates as a feedback loop.

Input buffers

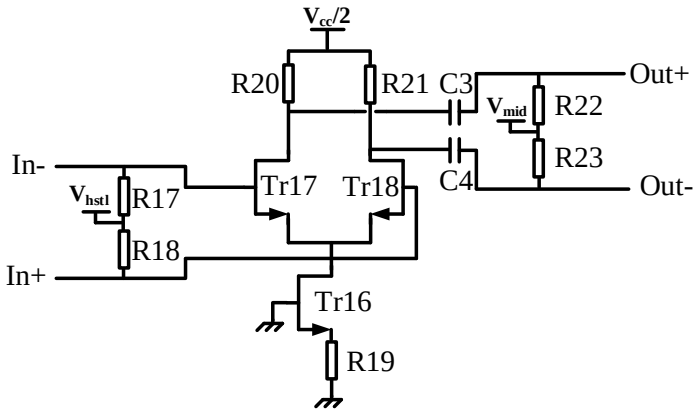


Figure 3.11: Input buffer

The inputs of the circuit are the gate of the differential switches. The required input levels are in the range of several Volts; it needs an intermediate stage to be compatible with FPGA bit

stream generators. Input buffers are then designed as an interface between the digital input bit streams which corresponds to a 1.8V HSTL standard and the switches of the Riemann Pump. The circuit is shown in Fig. 3.11. The pair of resistors (R_{17}, R_{18}), together with the common voltage V_{hstl} constitute an HSTL termination load. This differential signal is amplified through a differential pair made of the transistors (Tr_{17}, Tr_{18}), biased by (Tr_{16}, R_{19}), and loaded by (R_{20}, R_{21}). The amplified signal is then DC shifted thanks to series capacitors (C_3, C_4), and the common mode voltage V_{mid}, imposed through the resistors (R_{22}, R_{23}).

Circuit layout

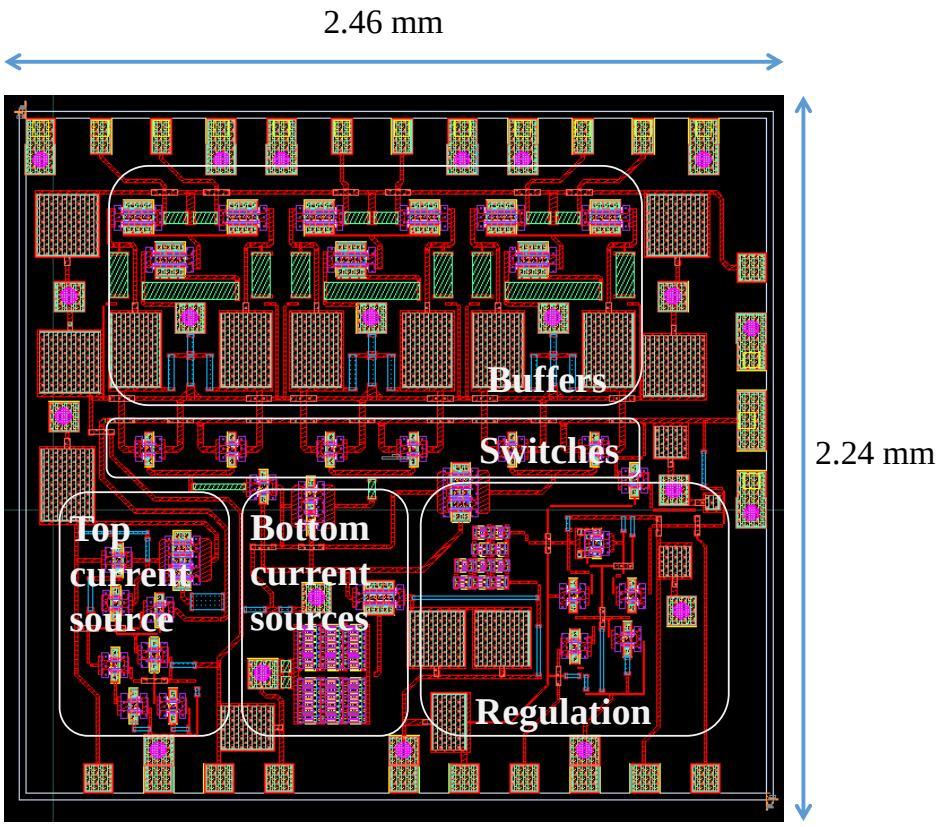


Figure 3.12: Layout view of the GaN circuit

The circuit layout is disclosed in Fig. 3.12, detailing all previously presented blocks. The overall die area is 5.5 mm^2 and the consumption of the core pump (without interface buffers) is slightly lower than 200 mW from a 15 V supply voltage. The routing of the circuit is ensured by a single metal layer, and the use of air-bridges allows crossroads. The components assembly is optimized to fit this constraint of interconnections. The graph of the circuit (where the components are

the vertices and the interconnection lines are the edges) is thus designed to be as planar as possible. It reminds the design of monolayer printed circuits boards which should be described by a planar graph, with additional local exceptions allowed by air bridges. EM models of the lines are calculated thanks to ADS tools and taken into account for circuit simulations.

3.1.4 Simulation results

Robustness

The output voltage is proportionnal to the charge of the output capacitor. Technological dispersion and temperature changes can cause mismatching between the current sources and induce an imbalance between the rails. The errors being cumulative, the output voltage can drift and provoke the saturation of the signal. The regulation block is in charge of balancing those discrepancies and ensure a proper operating point for the pump. The impact of temperature and technological dispersion on the output average voltage is assessed through the generation of a sine wave. The temperature is swept from -25^oC to $+75^oC$. As for technological dispersion, a Gaussian distribution is applied over the typical values, with respect to the parameters provided with the DK. Different runs corresponding to a random selection of all the parameters are then launched. The output average voltage dispersion is reported, with and without the regulation loop.

Table 3.2: Deviation of the output mean voltage with and without regulation loop.

$\Delta V/V$	**Without regulation**	**With regulation**
Temperature $[-25^oC - 75^oC]$	33%	1%
Technological dispersion	14%	0.6%

The addition of a regulation loop counteracts efficiently the implementation and temperature discrepancies. The output voltage drift is as low as 1% in the whole temperature range. This is an important feature as soon as the applications targeted with this GaN technology are due to operate in harsh environments.

Signal generation

The performances of the circuit in terms of signal quality is assessed thanks to the generation of a signal of interest for RADAR applications: a linear chirp. Those kind of signals are generated

to perform pulse compression; the general equation of a linear chirp waveform is given by the equation 3.1.

$$x(t) = Asin(2\pi(f_0 - \frac{\Delta f}{2} + \frac{\Delta f}{2T}).t), \quad t \in [0;T] \tag{3.1}$$

The following parameters are used:

- **Central frequency** $f_0 = 625$ MHz
- **Frequency dynamic** $\Delta f = 2$ MHz
- **Chirp duration** T = 250 μs

The Riemann code corresponding to the wanted chirp is computed with Matlab. The 3 bit streams corresponding to the slopes sequence are set as inputs for the circuit designed with ADS. The pump is calibrated to generate a maximum frequency of 1 GHz with an input frequency of 8 Gbps, which corresponds to an oversampling parameter r=2. The output waveform generated onto the capacitor is then saved and the corresponding spectrum is displayed in Fig. 3.13.

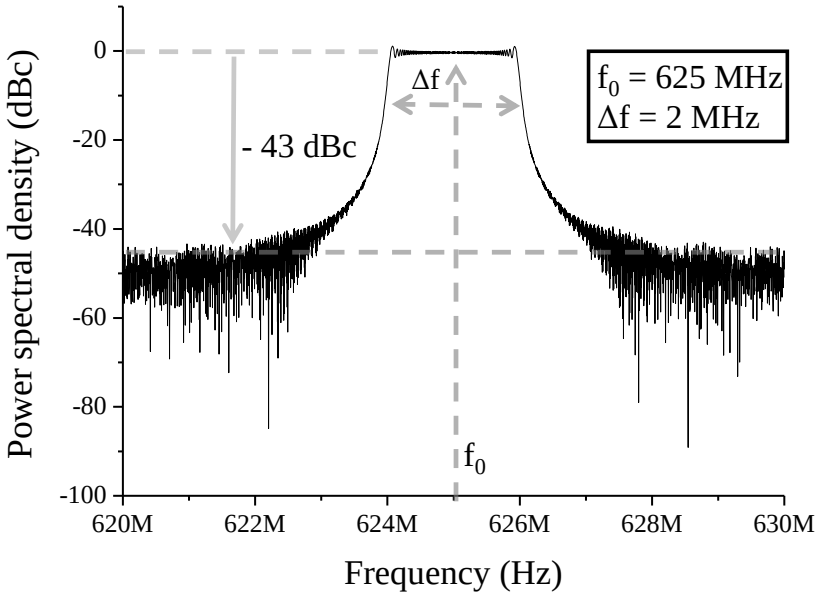


Figure 3.13: Power spectral density of the generated chirp

The spectrum corresponds to the wanted signal, i.e a linear frequency sweep of 2 MHz centered in 625 MHz. The slight ringings observed at the bounds of the chirp frequency interval are consistent with the theoretical spectrum of a linear chirp. The noise floor lays at -43 dB under the chirp power level. The power of the chirp itself is comparable to the power of a CW. It is

then possible to derive the SNR calculation thanks to the spectrum characteristics. The noise floor PSD is roughly constant over the complete bandwidth of the pump, i.e [0 - 1 GHz]. The signal level is also constant over a 2 MHz bandwidth. The PSD of the chirp is normalized to 0 dB, while the one of the noise floor equals -43 dBc. The SNR can simply be calculated thanks to the ratio of the chirp and the noise bandwidth, and their difference of PSD level.

$$SNR = \frac{P_s}{P_e} = 10log(\frac{BW_{signal}}{BW_{noise}}) + 43 = 26dB \tag{3.2}$$

The theoretical SNR for the set (r,N)=(2,3) equals 27 dB for the Riemann conversion. The actual SNR achieved with the circuit simulation is solely 1 dB under the theoretical formula including layout related effects. It suggests that the practical implementation will not significantly affect the signal quality; the quantization noise remains the main contributor to the overall noise.

Conclusion

The design of a prototype of the Riemann Pump in a GaN technology presents a significant interest for the generation of peculiar waveforms in harsh environments. It simplifies greatly the traditional circuitry and performs the generation of any kind of signal within a reduced power budget, with the potential of a direct co-integration with a PA in the same technology. The intrinsic resilience of GaN devices to EM disturbances, high voltages and heating is combined with circuit design techniques to ensure robustness of the system in harsh environment. It finds natural applications in the military domain where the reliability is mandatory and the flexibility a strategical asset. Post-layout simulations validate the integrability of the Riemann Pump in a GaN technology.

3.2 Integration in CMOS technology

The major target for the developed architecture is the mobile devices market and the associated consumer electronic products. The constraints of these applications are radically different from the military applications. Handset terminals need high bandwidth to support high data rates, low consumption to respect the limited energy budget imposed by the battery capacity and low cost to address a mass market. All these requirements should be met, eventually at the expense of durability and robustness: CMOS technologies are the most appropriate.

3.2.1 Architecture in CMOS technology

Sizing

The target technology is a 65 nm CMOS low power from the foundry TSMC. The sizing of the system is tightly related to the performances of this technology. The targeted features are the following:

- Number of bits N=3
- Sampling rate f_s=25 GHz
- Output BW > 3 GHz (r=2)

The core pump is an integrating RF-DAC. The proposed architecture (Fig. 3.14) takes advantage of the specificities offered by the target CMOS technologies to optimize the performances in terms of working frequency, power consumption and dynamic range. The designed Riemann Pump has an integrating complementary differential current steering topology.

- **Integrating**: the capacitive load of the pump is made of a differential PPA stage. It allows to perform an integration of the output current of the pump while amplifying the signal and feeding 50Ω differential loads.
- **Differential current steering**: the generated currents are steered to one side or the other of the differential load. It doubles the dynamic range compared to a single ended topology and provides inherent cancellation of even order harmonics.
- **Complementary**: complementary current branches optimize the current use. All the current flows carry information.

The current steering topology is extremely common in the field of RF-DACs. It allows to reach the highest performances in terms of speed because the generated currents are not cut but

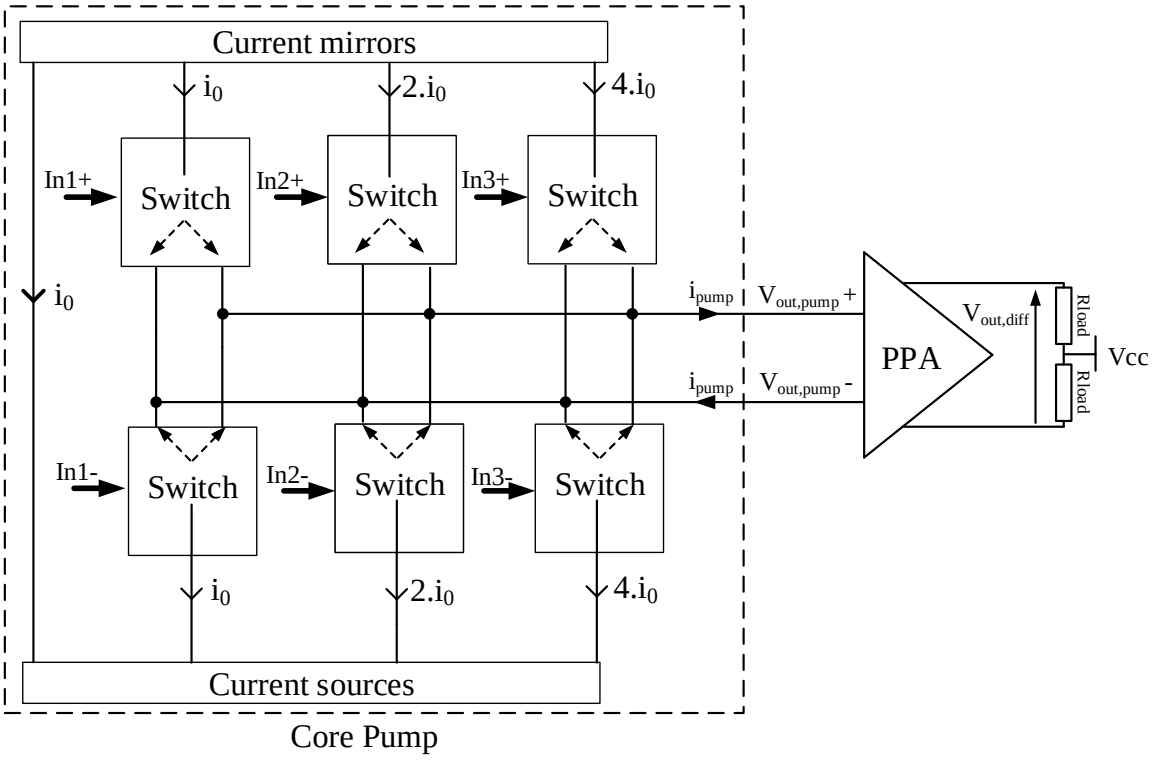


Figure 3.14: Topology of the Riemann Pump in CMOS technology

just steered in one side or the other [39]. A topology which relies on switching on and off the current sources would result in a lower power consumption but a lower working frequency. The constraints of the targeted application require a very high switching speed. Hence, the current steering topology is privileged.

3.2.2 Core pump circuit design

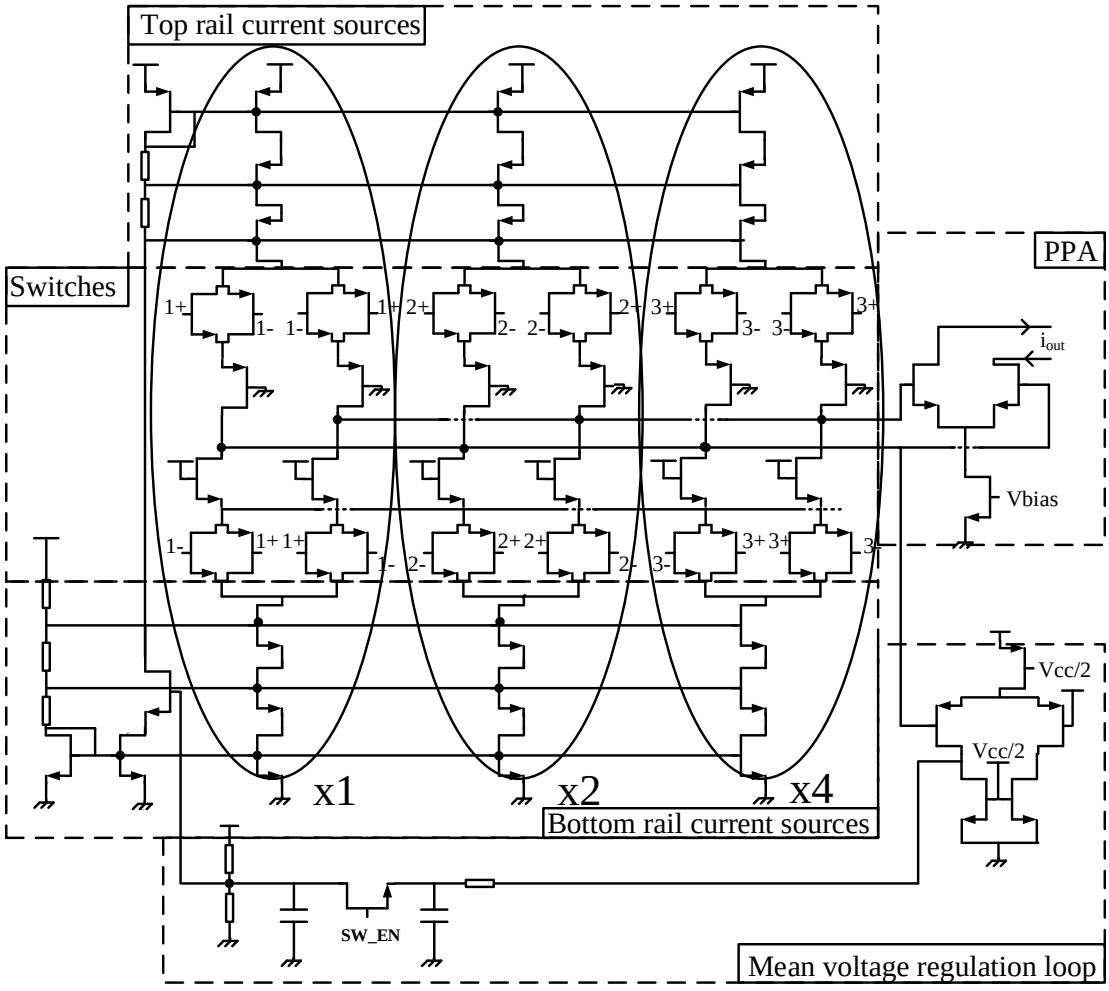


Figure 3.15: Schematic view of the core Riemann Pump in CMOS technology

The overall circuit is presented in Fig. 3.15. Its sizing and design start from the output stage, namely the PPA.

3.2.2.1 Pre-Power Amplifier (PPA)

The PPA is a simple differential pair with 50Ω loads (Fig. 3.16). The target is to ensure a differential 1 V_{pp} output voltage on those loads. The size of the transistors is thus set in accordance with this goal. The size of the switches sets the output capacitance of the current pump. The normalized capacitance of those transistors is plotted versus frequency in Fig. 3.17.

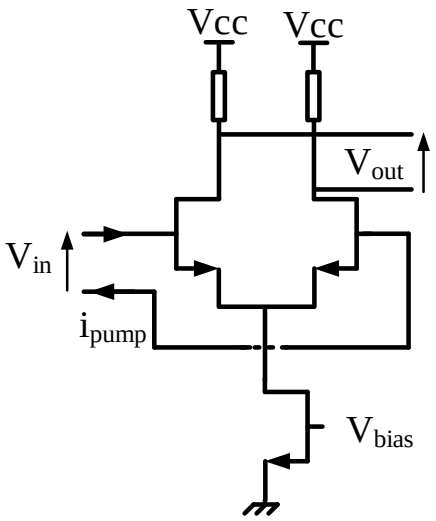


Figure 3.16: PPA schematic

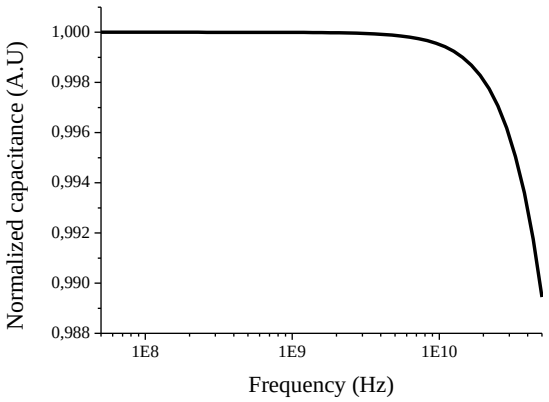


Figure 3.17: Normalized gate capacitance of the PPA differential pair

The capacitance value is almost constant until several tens of GHz. The integration of the switched currents into this equivalent capacitance does not bring significant frequency distortion. The static transfer function of the PPA (Fig. 3.18) shows the output differential voltage with respect to the input voltage. The PPA is biased in class A to perform a linear amplification and avoid additional distortion. A 1 V_{pp} differential output voltage is developed across the 50Ω loads in the linear region. It corresponds to a 300 mV_{pp} differential input voltage. The equivalent capacitance of the switches is in the range of the pF.

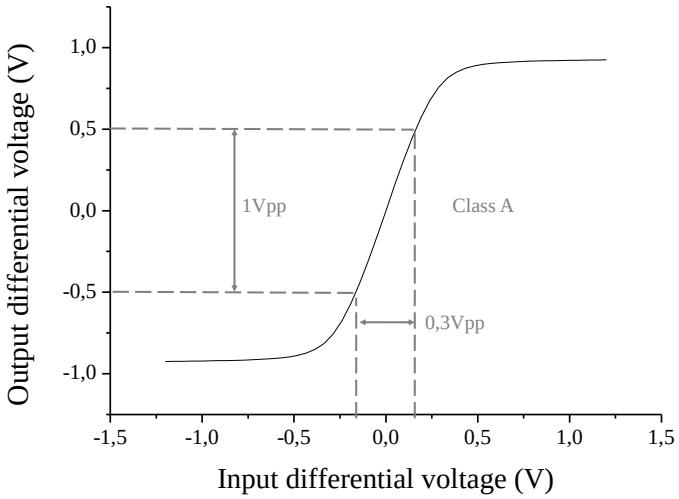


Figure 3.18: Static voltage characteristic of the PPA

3.2.2.2 Current sources

The current sources are derived from a reference branch via current mirrors, so that both the top and bottom rail current sources depend on a same reference (Fig. 3.19).

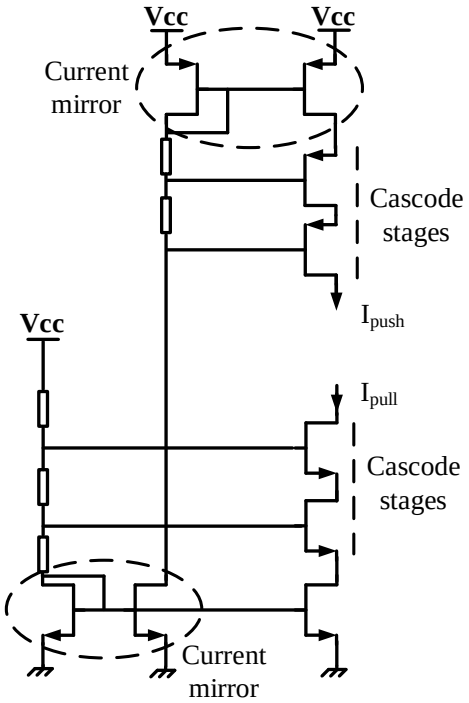


Figure 3.19: Bottom and top rail current sources

Current sources matching

Matching issues in current steering DACs have been studied in [38]. In particular, the formula used to describe the relative variance $\frac{\sigma I}{I}$ of the current source due to random process mismatch is given by:

$$\frac{{\sigma_I}^2}{I^2} = \frac{1}{2WL}({A_\beta}^2 + \frac{4{A_{Vt}}^2}{V_{od}^2}) \tag{3.3}$$

A_β and A_{Vt} are the mismatch process constants for the transistor gain and threshold voltage respectively. V_{od} is the overdrive voltage, it equals $V_{gs} - V_t$. W and L are the width and length of the transistor. The mismatch constants are fixed by the process, the overdrive voltage depends on the design but it cannot be tuned significantly because the output voltage dynamic of the current sources is constrained. The only design levers are (W, L) of the transistors. The area is to be maximized so as to limit the mismatch between the sources. Hence, W and L of the involved transistors are large. In particular, the highest possible channel L is chosen for those transistors. W is then set to obtain the target current. This current is calibrated with respect to the target bandwidth and the output capacitance. The system is intended to address approximately 3 GHz bandwidth. The output capacitance is set by the PPA and is in the pF range. The signal dynamic is fixed by the input dynamic range of the PPA, so as so operate in linear region; it is approximately 300 mV_{pp}.

Referring to the equation 2.1 in Chapter 2, the voltage quantum is determined thanks to the signal dynamic, the number of bits and the OSR. The calculation of the unit current quantum is then set by the loading capacitance, fixed by the size of the PPA differential pair.

$$I_q = q f_s C_{load} \tag{3.4}$$

The current quantum is thus calculated and the corresponding unit current source transistor width is consequently set.

Current sources I-V curves

The Riemann Pump is based on the integration of currents in an output capacitance whose voltage is varying. The current sources must present a high enough output impedance to ensure a proper operation over the wanted output dynamic. For this purpose, the designed current sources entail two cascode stages. The obtained current source characteristic (for the bottom rail) is displayed in Fig. 3.20 and compared with two other configurations, with only one and without cascode transistor, respectively.

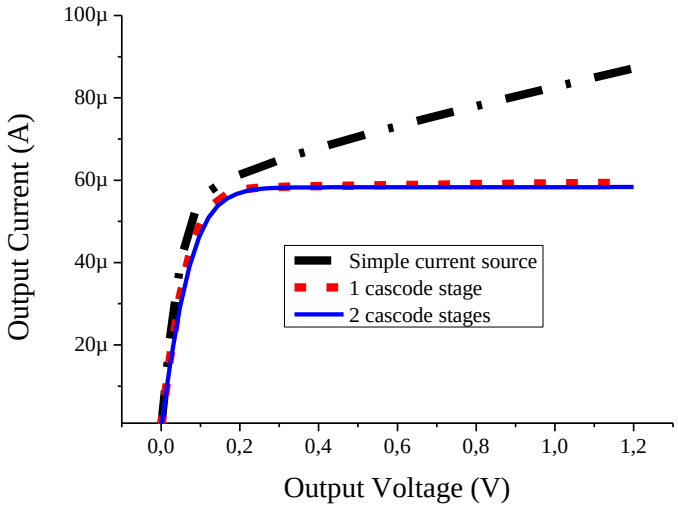


Figure 3.20: Current sources characteristics

The simple source without cascode stage is obviously too much dependent on the output voltage. The output impedance in the saturated region is:

$$R_{out} = r_{ds,on} \approx 40k\Omega \tag{3.5}$$

Where $r_{ds,on}$ is the channel resistance. The adjunction of cascode transistors biased in saturation on the current source increases the output impedance. All the transistors are designed with the same W and L for matching purposes between the current cells. A first order approximation of the output impedance for a single cascoded current source is given by the following approximation.

$$R_{out} \approx g_m r_{ds,on}^2 \tag{3.6}$$

Where g_m is the transconductance of the cascode transistor. For the considered transistor size and under the biasing conditions, $g_m \in [0.2mS, 0.5mS]$ The output impedance for the simple cascoded structure is increased by a factor $g_m r_{ds,on}$, i.e approximately a decade. The adjunction of a second cascoded stage has a similar effect; it increases again the output impedance of a factor $g_m r_{ds,on}$, resulting in an output impedance of several $M\Omega$. The total dropout voltage of the structure remains under 300 mV. The relative variations of the current in the middle of the output dynamic and the corresponding output impedances of the structures are reported in Table. 3.3

Table 3.3: Output impedance of various current source structures.

	Relative variations of I $V_{out} \in [0.4V - 0.8V]$	**Output impedance**
Simple source	15.2%	$40k\Omega$
1 cascode stage	1%	$640k\Omega$
2 cascode stages	0.12%	$8M\Omega$

The 2 stage cascoded structure is then implemented, both on the bottom rail with NMOS transistors and on the top rail with PMOS transistors. The 2 current source characteristics are displayed together in Fig. 3.21.

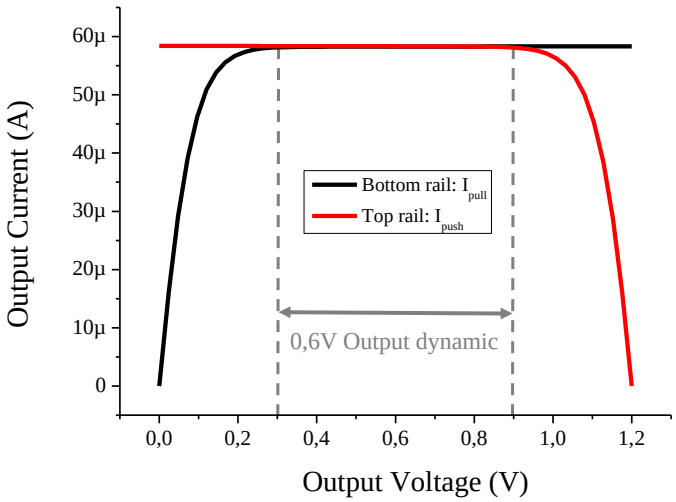


Figure 3.21: Top and bottom rails current source characteristics

The output voltage dynamic is restricted to $[0.3V - 0.9V]$ for a proper operation of the 2 current sources rails. It covers the needed output dynamic of 0.3 V_{pp} and ensures extra room for the addition of the switching stage.

3.2.2.3 Switches

The designed switches (Fig. 3.22) have the following characteristics :

- **Differential**: the current steering topology imposes the use of differential switches to steer the current toward one way or the other. It improves the working frequency.

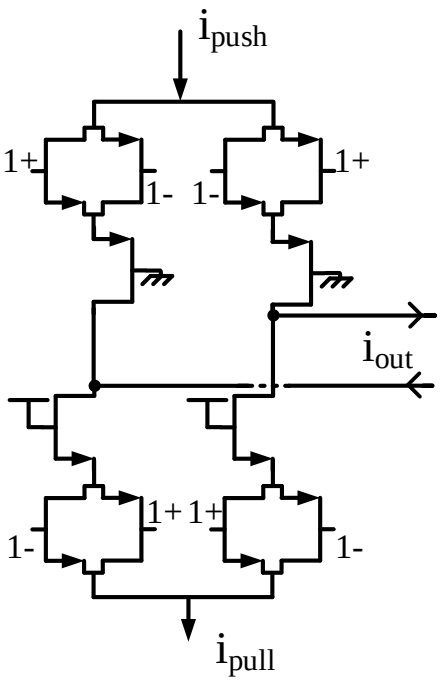


Figure 3.22: Switching stage

- **Cascoded**: An additional cascode stage is added on top of the switches to provide a better isolation between the input digital bit streams and the output nodes

- **Complementary**: Each switch is composed of an NMOS associated in parallel with a PMOS to compensate charge injection.

Fig. 3.23 exhibits the temporal evolution of the output current when the inputs are switched. The implemented structure with complementary switches is compared with a non-complementary structure, composed of only NMOS on the bottom rail and PMOS on the top rail.

The simple structure suffers from the phenomenon of charge injection during the switching; it causes large spikes in the output current which are integrated in the loading capacitance. Charge injection occurs when a switched transistor is turned off; the carriers released from the channel induce a charge transfer. In the designed complementary MOS switches, an NMOS and a PMOS of same width are associated in parallel. When they are turned off, the negative charges released by the NMOS are compensated by the positive charges released by the PMOS.

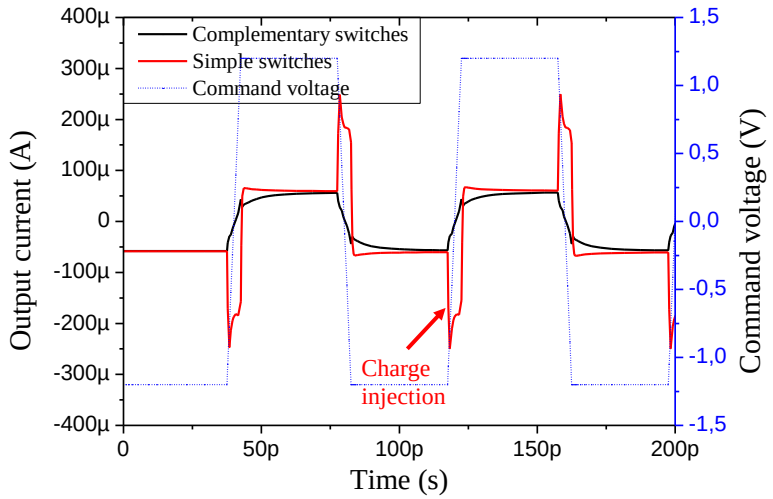


Figure 3.23: Transient behavior of the switches

3.2.2.4 Regulation loop

The current sources and the switches are designed to be as balanced as possible. Nevertheless, any imbalance of the rails can cause a drift of the output common mode voltage through the integration of an error current in the output capacitance. The output voltage would drift toward one rail or the other until it stifles the corresponding current sources to reach an equilibrium point. This scenario is not desirable since it would cause extra distortion in the Riemann Pump and the PPA. To avoid such a drift, a regulation loop (Fig. 3.24) is added to regulate the common mode of the output voltage. It is based on a dynamic balancing of the top rail current sources with respect to the bottom rail current sources.

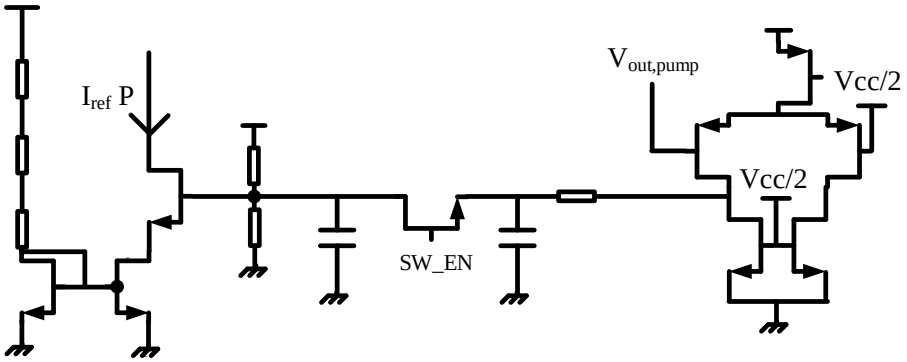


Figure 3.24: Common mode regulation loop

The loop works as follows:

- The voltage of a branch of the output is sensed and compared to the wanted common mode $\frac{V_{cc}}{2}$ thanks to a differential pair.
- The output of the comparator is filtered through an RC filter and biased with a decoupled resistor bridge.
- This voltage controls the gate of a transistor placed into the current reference branch of the top rail current sources in order to balance the pushed and the pulled currents.
- A pass gate transistor enables to open or close the regulation loop.

The regulation loop is presented by the following block diagram (Fig. 3.25).

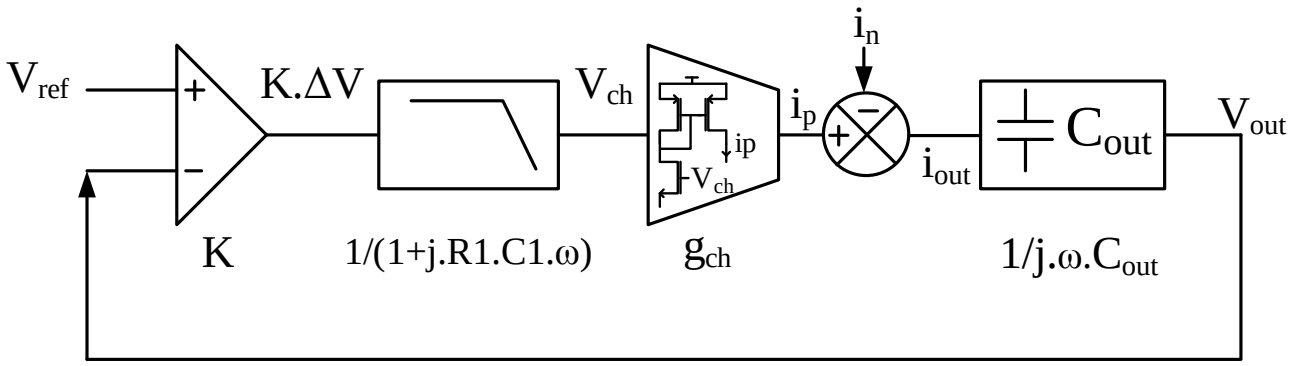


Figure 3.25: Block diagram of the regulation loop

The loop is composed of a comparator of static gain K, a first order low pass filter, a choking transistor acting as a transconductance and an integrator corresponding to the output capacitance. The overall open loop transfer function can be written as:

$$H(j\omega) = K.g_{ch}.\frac{1}{Cj\omega}.\frac{1}{1+jRC\omega} \tag{3.7}$$

The static gain is infinite due to the presence of a pure integrator. The static output current of the top rail i_p with respect to the output voltage V_{out} is plotted in Fig. 3.26 and compared to the current generated by the bottom rail.

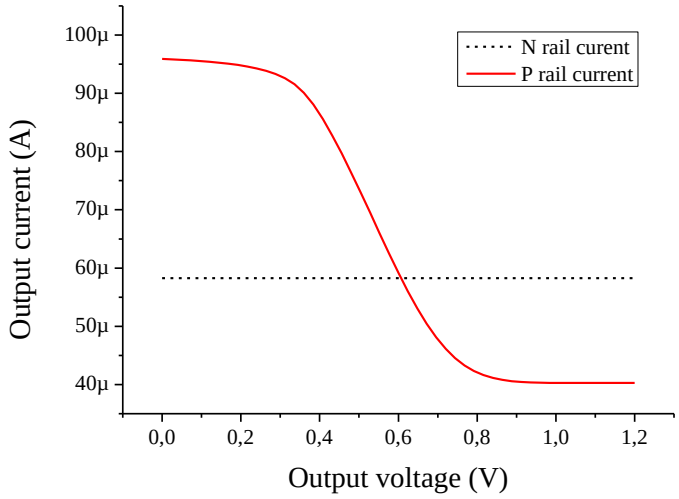


Figure 3.26: Loop transconductance gain

The loop transconductance gain $\frac{\Delta I_{out}}{\Delta V_{out}}$=K.gch can be determined. The overall open loop transfer function gain and phase are presented in Fig. 3.27.

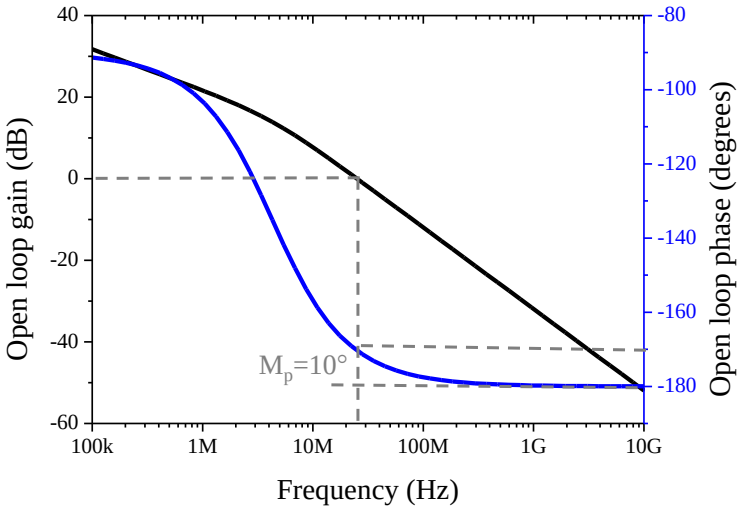


Figure 3.27: Bode diagram of the open loop transfer function

The phase margin is approximately 10 degrees. This relatively low phase margin is mainly due to the capacitive output impedance which behaves like a pure integrator. Nevertheless, the stability has been ensured thanks to transient response to pulses. Furthermore, the pass gate transistor inserted in the loop allows to decrease the gain of the loop by controlling its gate voltage, thereby increasing the phase margin of the system. This transistor can also be completely cut off to virtually open the loop.

3.2.3 Riemann Pump layout

The layout of the core pump is presented in Fig. 3.28.

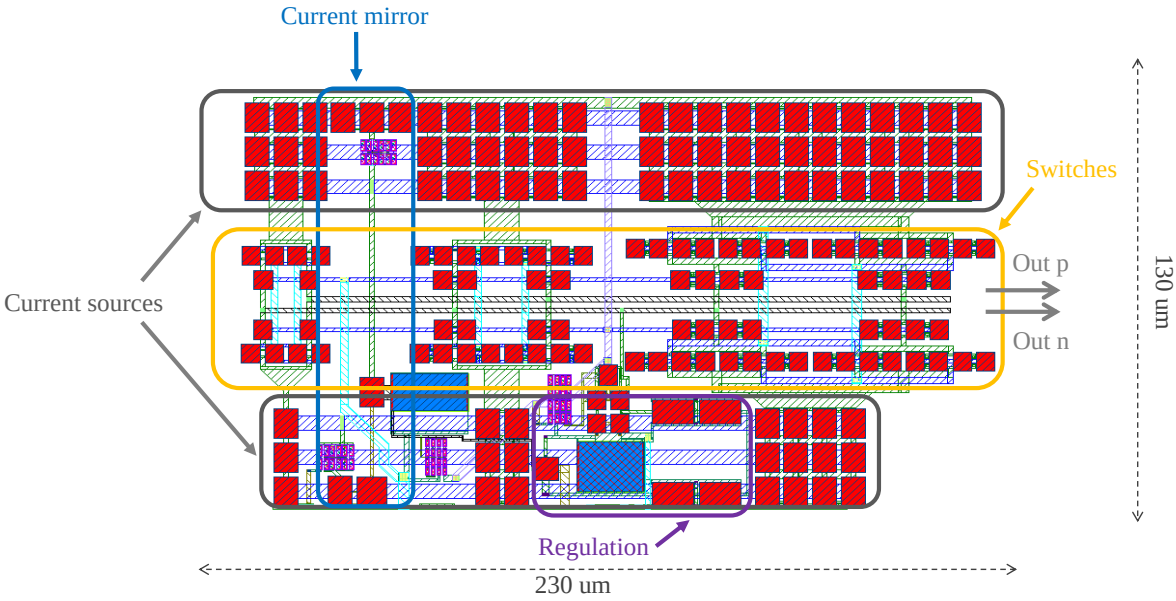


Figure 3.28: Layout of the core pump

The layout is constrained by numerous rules, mainly concerning electrical and mechanical reliability. The compliance of the layout with these rules is ensured by a Design Rule Check (DRC) tool. Besides these compulsory geometrical rules, a lot of design issues can occur. To achieve a high accuracy, the design of the current sources and the associated switches consists of three branches, of respective weight 1, 2 and 4. Each branch corresponds to a symmetric duplication of the previous one; the use of identical transistors and identical unit switched current cells favors a good matching between the 3 branches. The resistors are designed with a common centroid topology based on a single unit resistor to provide a good relative matching between their resistance values [58]. DC paths are routed with the lowest metal layers (M1-M5), including the current sources. The highest metal layers (M6-M9) are used for the RF output signals and the input high frequency bit streams. The RF differential traces are routed symmetrically and the parasitic capacitances are minimized, while ensuring a low resistance. The crossings between lines are perpendicular to avoid crosstalk.

The layout of the PPA is presented in Fig. 3.29. The overall differential pair structure is split in two symmetric halves. The transistors and the metal paths are sized with respect to the

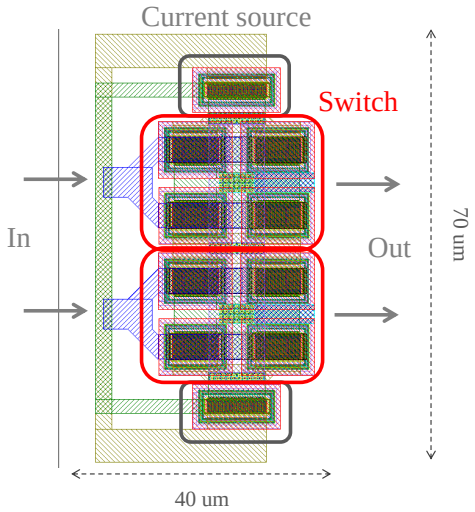


Figure 3.29: Layout of the PPA

expected current density. The PPA is implemented in open drain configuration. The 50Ω loads are not included into this layout as they will be placed off chip.
The core pump and the PPA are associated and RC parasitic elements are extracted from the overall circuit, to take into account the layout implementation.

3.2.4 Post-Layout Simulations (PLS)

The performances of the designed circuit are assessed thanks to PLS. The simulation flow is described in Fig. 3.30.

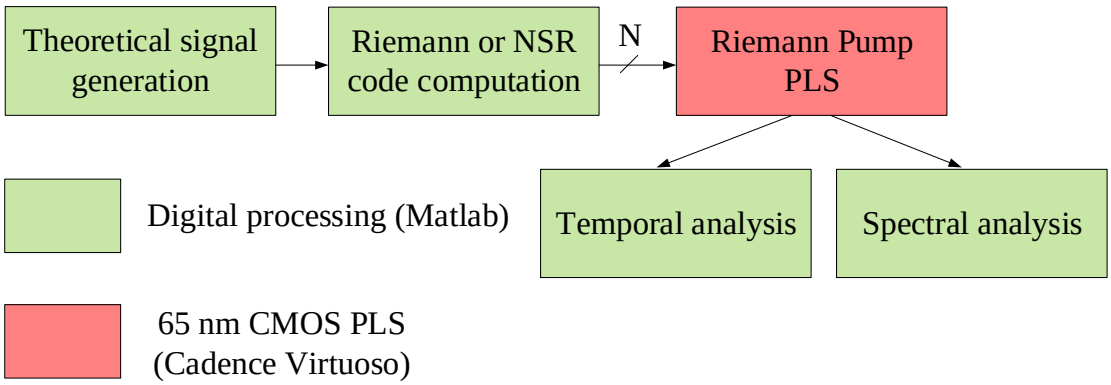


Figure 3.30: PLS flow

The wanted signal is generated with Matlab and the Riemann (respectively NSR) algorithm is computed to determine the sequence of slopes giving the best approximation of this signal.

These N bit streams serve as inputs for the designed circuit, clocked at 25 GHz. PLS is done with Virtuoso and the output voltage of the PPA is saved and analyzed with Matlab. CW generation is simulated to assess the impact of the circuit design with respect to the theoretical performances. Simulations of modulated signals concurrent transmission are then carried out.

3.2.4.1 CW generation

Spectra

The generation of CW at different frequencies is simulated with both the Riemann and the NSR algorithm. The spectra of 3 GHz generated CW are plotted in Fig. 3.31

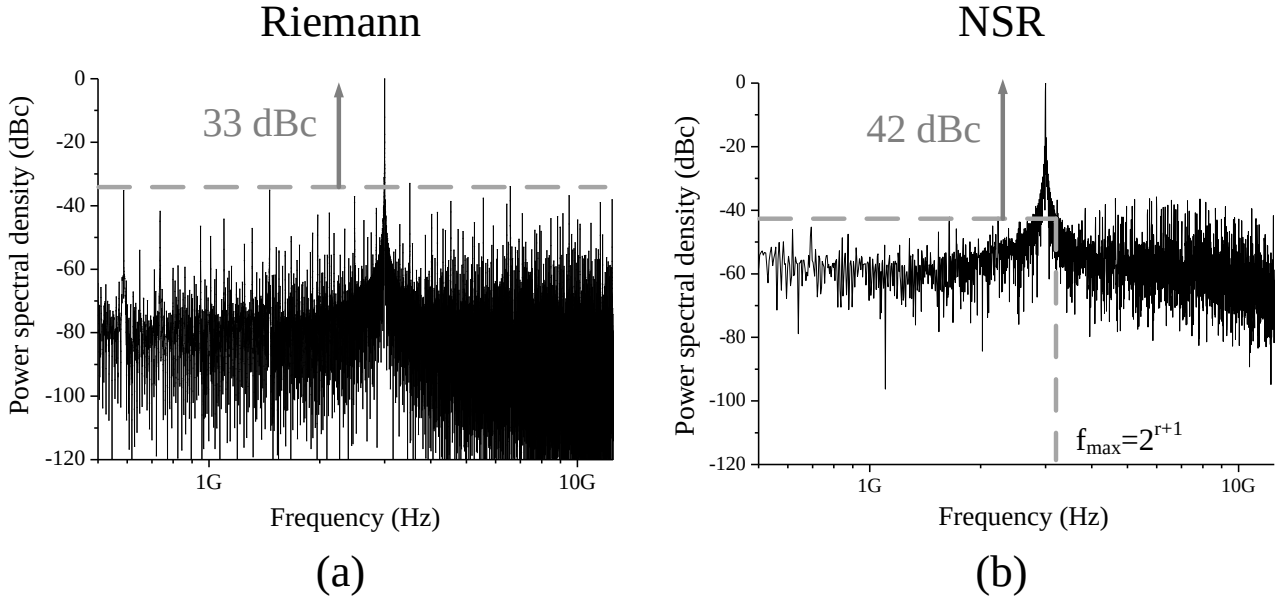


Figure 3.31: 3 GHz generated CW - PLS - (a) Riemann and (b) NSR

- The **SFDR** corresponds to the difference of level between the CW and the strongest spurious in the band of interest. This parameter enables to spot inter-modulation products or distortion due to circuit non-linearities at specific frequencies.

- The **SNR** is calculated as the ratio of the CW power and the noise power, integrated over the [0 - 3.125 GHz] band. This metric is representative of the overall noise generated by the system.

The SFDR and SNR are extracted for the generation of CW of various frequencies, distributed over the [750 MHz - 3 GHz] range.

SFDR

The SFDR values are compared with the SFDR obtained for an ideally generated piecewise linear approximation with the same parameters (r,N), for the two algorithms. The results are reported in Fig. 3.32.

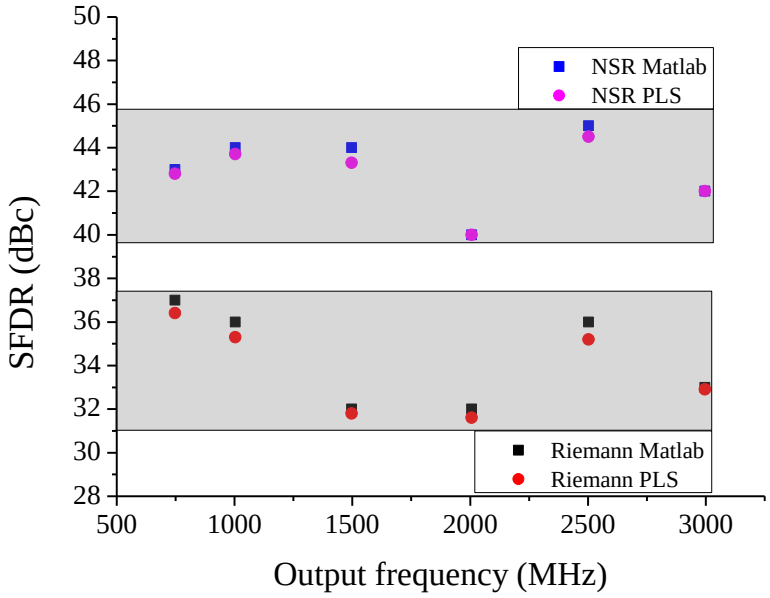


Figure 3.32: SFDR - PLS Vs theory - Riemann and NSR

For CW generation, the SFDR values are frequency dependent, but the PLS results are close to the ideal results for the two algorithms. The degradation related to the implementation is smaller than 1 dB for the whole frequency band.

SNR

The SNR values are reported and compared with the theoretical formulas in Fig. 3.33. Values obtained with PLS are consistent with the theoretical values: the PLS SNR are included in a $+/-$ 1 dB interval with respect to the theoretical formulas for both of the 2 conversion schemes.

PLS of the Riemann Pump does not result in a noteworthy degradation of the key performances. They are still limited by the quantization noise.

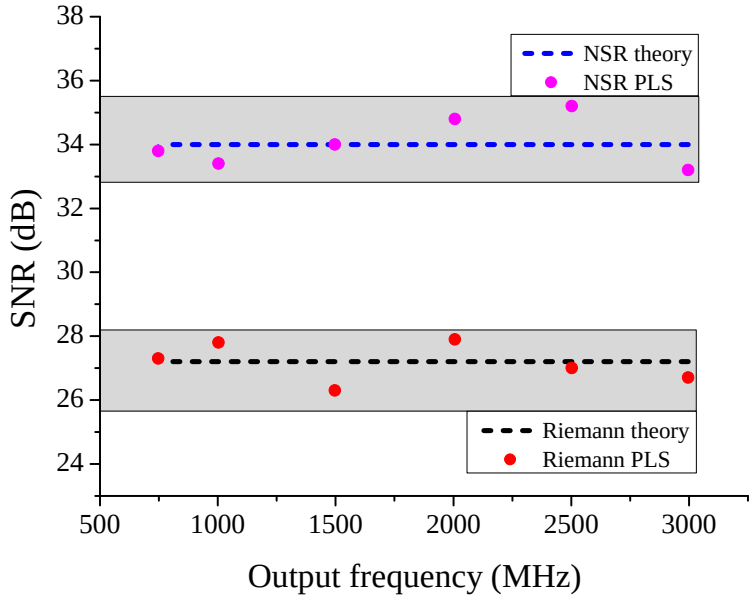


Figure 3.33: SNR - PLS Vs theory - (a) Riemann and (b) NSR

3.2.4.2 Modulated signal concurrent generation

The simulation of 10 carrier aggregated 5G signals modulated with 64-QAMs would be too long for the time consuming transient simulations, especially as parasitic elements are taken into account. The ability of the system to handle concurrent transmission is thus demonstrated with a combination of 3 modulated signals distributed over the [0 - 3 GHz] band corresponding to several standards with the characteristics listed in Table. 3.4

Table 3.4: Features of the concurrently generated modulations.

Modulation	**Carrier frequency**	**Data rate**	**Associated standard**
QPSK	900 MHz	10 Mbps	GSM
QPSK	2450 MHz	20 Mbps	Wifi
16-QAM	2600 MHz	40 Mbps	LTE

The spectra of the composite signals corresponding to the sum of the 3 modulated signals reconstructed with respectively the Riemann and the NSR coding scheme are displayed in Fig. 3.34. For the **Riemann** conversion, the noise floor is flat over the whole band and it is located at 42

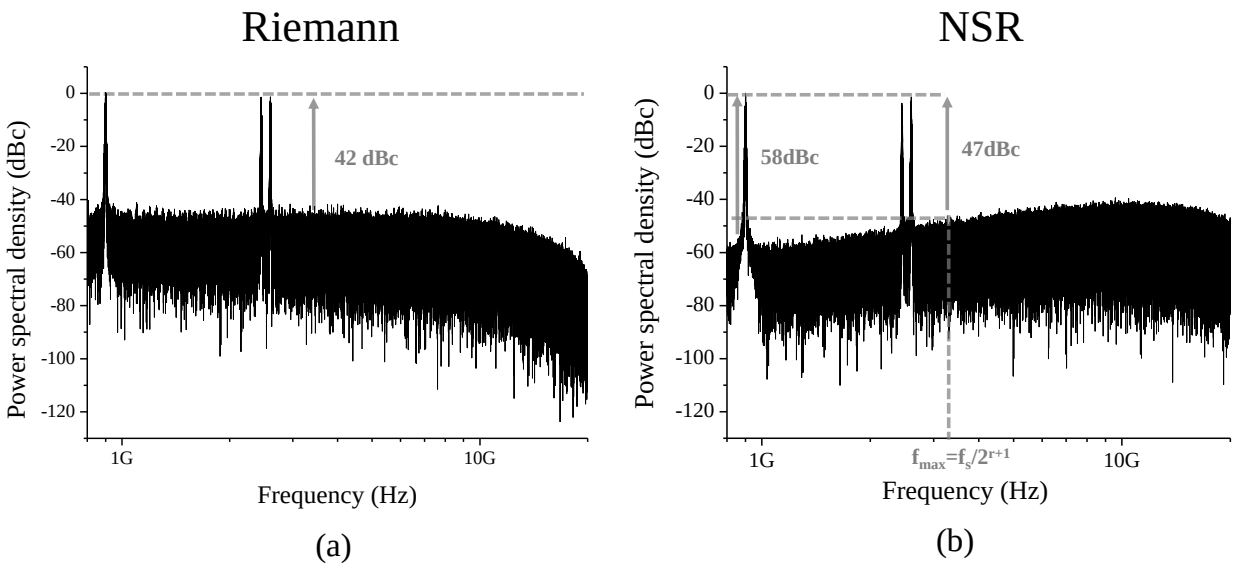
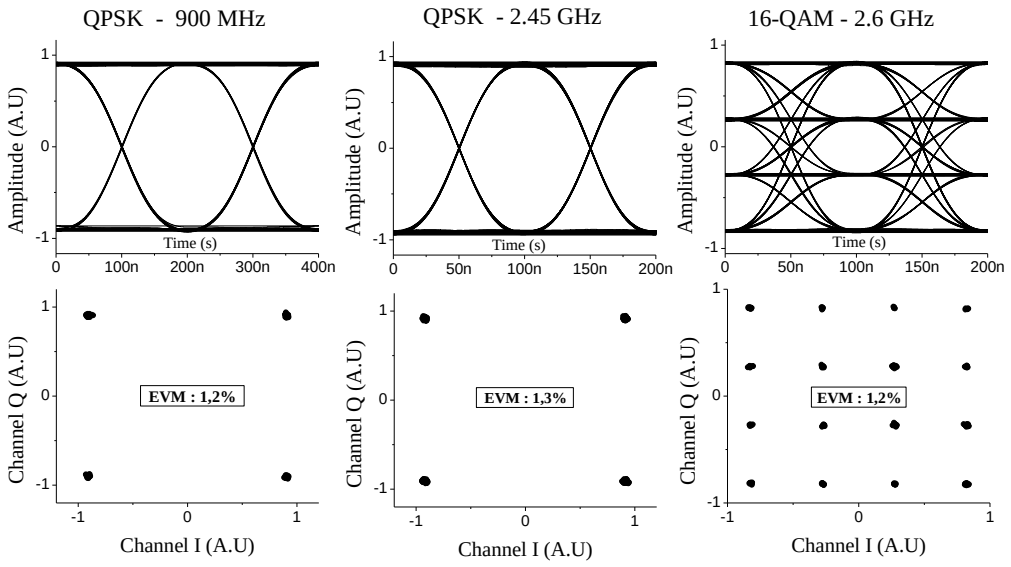


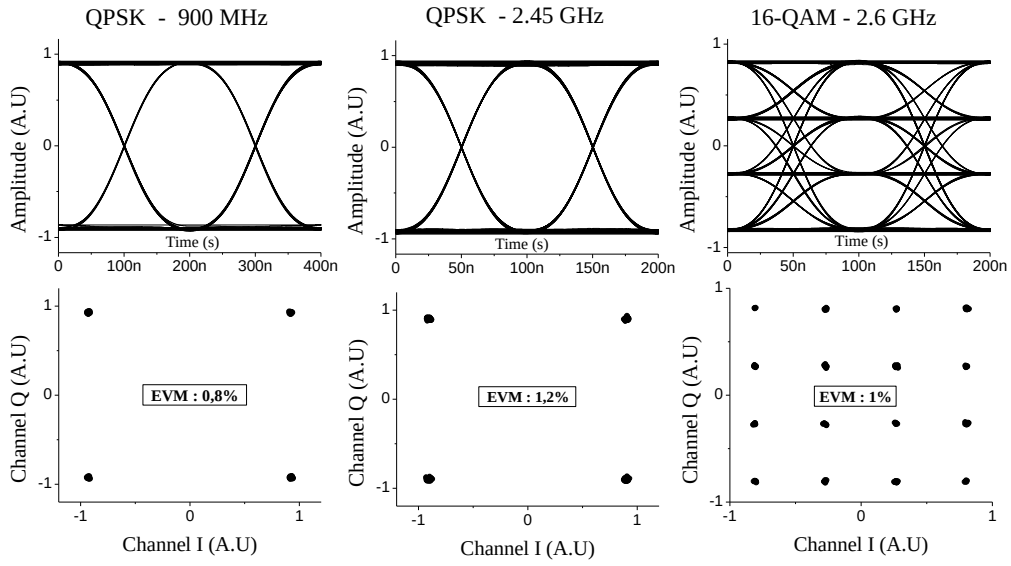
Figure 3.34: Spectra of the concurrently transmitted signals - (a) Riemann and (b) NSR

dB under the level of the modulated signals. The noise floor exhibits a high pass characteristic for the **NSR**; it is not uniformly distributed over the whole band but it turns out lower than the **Riemann** case in the band of interest.

The 3 signals are then demodulated independently for the two conversions. The obtained eye patterns and constellations are displayed in Fig. 3.35. The obtained EVM values for the **Riemann** conversion are slightly higher than 1%, which is below the requirements for the most common standards, with maximum EVM in the range of several percents. There is room for the command circuit and the power amplification imperfections. The EVM values for **NSR** are improved with 0.1% to 0.4% with respect to the **Riemann** algorithm. The modulation carried at the lower frequency benefits from the highest improvement, in accordance with the position of the noise floor.



(a)



(b)

Figure 3.35: Eye patterns and constellations for the concurrent modulated signals - (a) Riemann and (b) NSR

3.2.4.3 Conclusion

The design and implementation of the Riemann Pump in a 65 nm CMOS technology and the associated PLS simulations confirm the feasibility of the overall architecture. The overall performances should be limited by the parameters (r,N) of the implemented circuit and the associated quantization noise rather than the circuit non-idealities. However, all previous simulations are led to assess the performances of the Riemann Pump itself, i.e the DAC. The control bit streams are considered ideals so far. Nevertheless, an actual implementation of a global transmitter would require the generation of high speed bit streams to control the Riemann Pump, and the adequate interfaces. The following section deals with the realization of the chip which implements several environments for the Riemann Pump, with various digital interfaces.

3.2.5 Chip design - PAULINA

A chip called PAULINA (**P**umping **A**ggregative **U**niform **LIN**ear **A**pproximation) was designed. As hinted by the layout techniques relative to the core pump and the PPA design, the chip layout considers additional factors, regarding the device, the block, and the chip scale. Those considerations have an important impact on the layout design.

- **Current density**: the interconnections have to respect maximum current densities, to limit self-heating effects and ensure reliability. It impacts the width of metal traces, the one of transistor's fingers, and the number of vias.
- **Path length matching**: differential signals are to be conveyed by symmetric and precisely matched traces. Furthermore, the length of the 3 differential input traces has to be matched.
- **Parasitic elements**: all the parasitic elements related to the interconnections should be taken into account. It impacts especially the high speed digital blocks which are sensitive to parasitic capacitances and resistances.
- **Ground return**: the paths should be carefully placed and distributed to ensure a proper cold ground.
- **Decoupling**: the decoupling of the cold points filters out the noise induced by the current flows. The cohabitation of digital and analog blocks imposes an efficient decoupling. Supply and ground planes provide a distributed decoupling over a wide frequency band.
- **Cross talk**: when signal paths are coupled by parasitic elements, cross talk can occur between them. To limit these effects, differential signals are isolated by supply/ground planes and are as little contiguous as possible.

The prototyped chip global layout is shown in Fig. 3.36. 4 circuits are embedded, 1 per corner of the chip, each one corresponding to the implementation in a specific I/O environment.

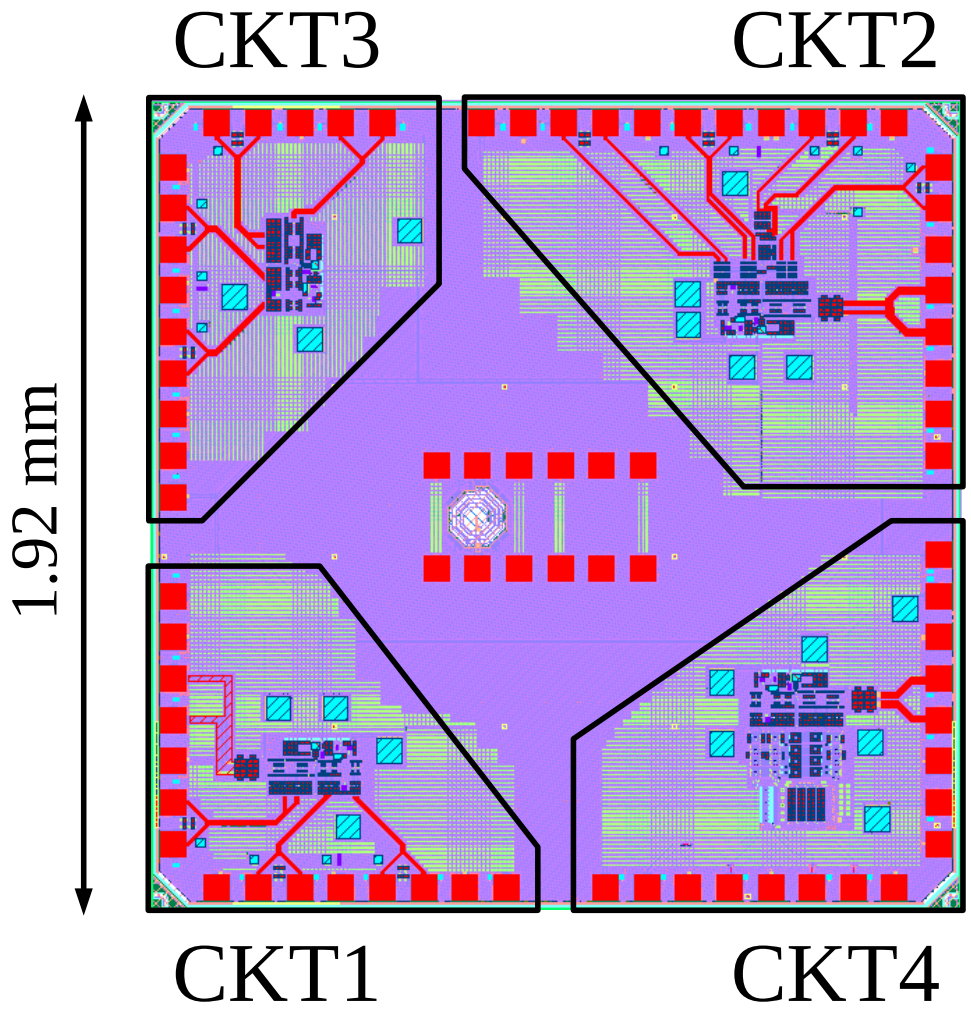


Figure 3.36: PAULINA layout view

The same design of the core pump is implemented in the 4 circuits. The differences are related to the input and/or output interfaces. The specificities of the 4 circuits are intended to evidence various phenomena. They rely on different overall architectures.

CKT1: Standard pump

The standard version of the pump is embodied into the chip by CKT1. The corresponding overall architecture is displayed in Fig. 3.37. The command bit streams are generated thanks to an FPGA equipped with high speed serial transceivers, using HSTL standard. The differential 50Ω termination is designed on-chip, with a common mode voltage of $\frac{V_{cc}}{2}$. This first circuit is not limited in terms of frequency height, provided the input bit streams can be generated at a very high speed.

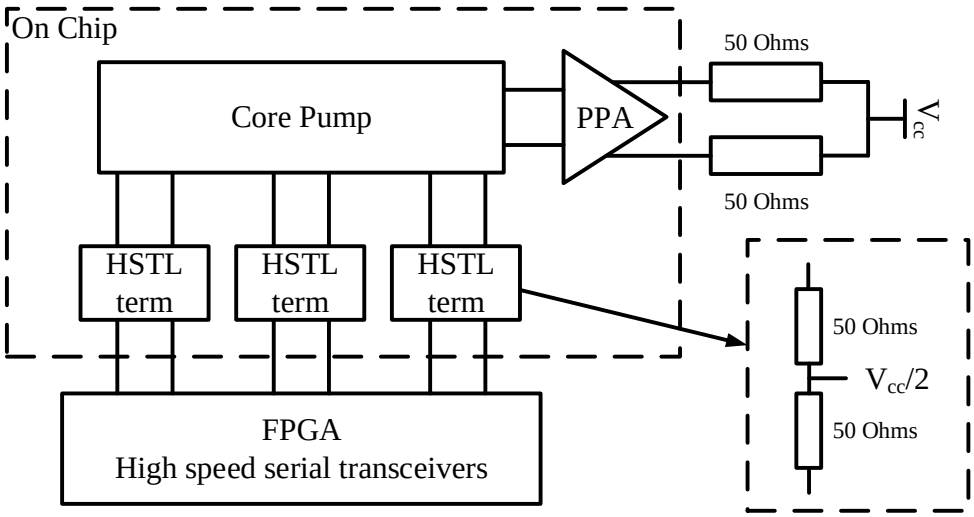


Figure 3.37: CKT1 Architecture

Table 3.5: CKT1 operating currents.

Block	**Current**
Pump	$700\mu A$
PPA	$20mA$

CKT2: Re-clocked pump

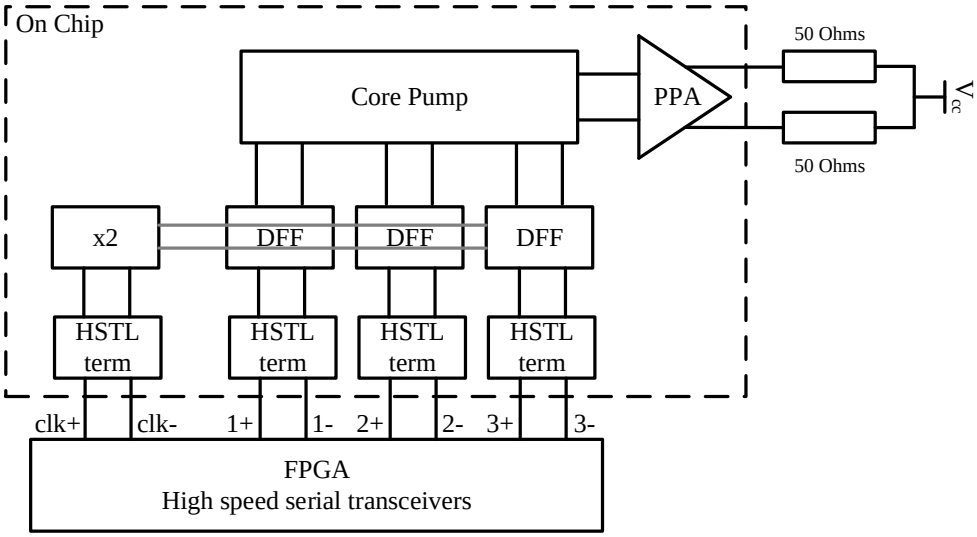


Figure 3.38: CKT2 architecture

The lengths of the high speed input traces are matched, but the channel (PCB, package) can induce disparities. To tackle this issue, a re-synchronization interface is implemented in CKT2. It uses a fourth input channel which is a clock from the FPGA, at the same frequency as the 3 input bit streams. A frequency doubler allows to create a new clock signal on chip which is used to synchronize the 3 inputs thanks to differential DFFs.

Table 3.6: CKT2 operating currents.

Block	**Current**
Pump	$700\mu A$
PPA	$20mA$
Digital interface	$20mA$

The design of the high speed digital interface is sensitive to the parasitic elements related to the layout. More precise block diagrams, transistor level circuits and layout views of the digital blocks are provided in Annex 5.2.1.

CKT3: Stand alone pump

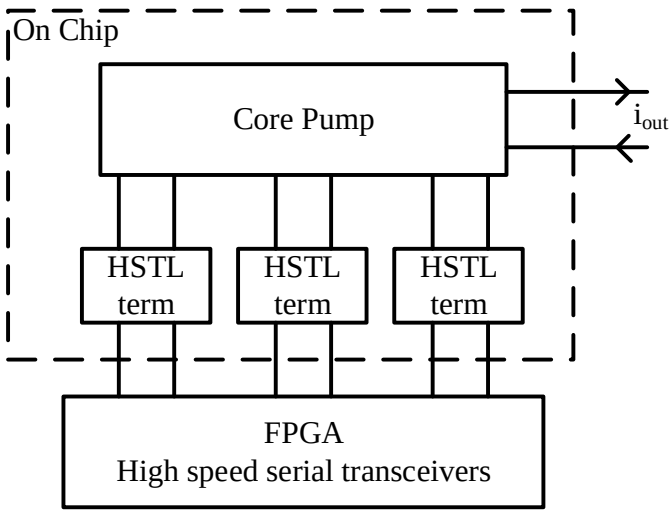


Figure 3.39: CKT3 Architecture

The implementation of the core pump together with the PPA sets a minimum frequency for the input. Indeed, the loading capacitance of the pump is fixed by the size of the PPA and a minimum frequency is needed to avoid saturation. CKT3 implements a non-frequency-limited version of the pump. The input frequency range is determined by the off-chip load.

Table 3.7: CKT3 operating currents.

Block	Current
Pump	$700\mu A$

This version allows to assess the behavior of the pump over several frequency decades and eventually to replace the capacitive load by a resistive load to measure the mismatching between the current sources.

CKT4: Autonomous pump

A last version of the Riemann Pump is associated with an on-chip high speed digital generator in CKT4. Each data lane has an 8 bits LUT which is perpetually read and fed to the pump switches. The LUTs are loaded thanks to a FIFO which operates as a serial to parallel interface.

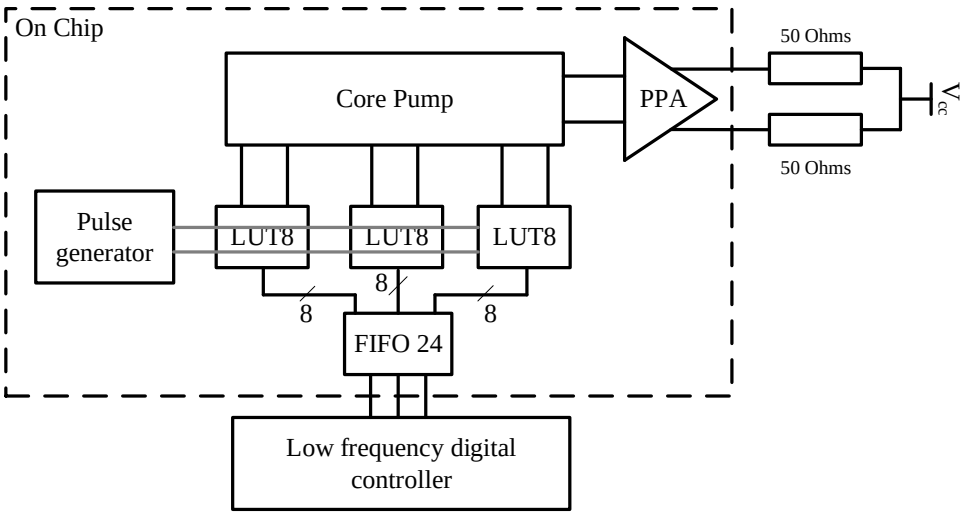


Figure 3.40: CKT4 Architecture

Table 3.8: CKT4 operating currents.

Block	Current
Pump	$700\mu A$
PPA	$20mA$
Pattern generator	$10 - 25mA$

The pulse generator frequency is tunable within almost an octave around 10 GHz. It allows to store simple 8 slopes patterns and to output the resulting signal. Details about the design of the pulse generator, the FIFO and the LUTs are available in Annex 5.2.2.

3.3 Conclusion

The Riemann pump has been designed in 2 completely different technologies for different applications. RADAR applications are targeted by the GaN design which has high power capabilities and robustness. Wireless communication massive market is targeted by the CMOS circuit which benefits from low power devices, high integrability and high speed to face the stringent requirements of next generation mobile terminals.

A lot of techniques have been used and developed in the two designed chips, covering both the analog and digital domains. PLS evidence a virtually transparent impact of the physical implementation since the performances are not distinctly degraded with respect to the theory. It confirms the adequacy between the proposed architectures and the electrical implementation. It also suggests that more complex versions of the Riemann Pump should be designed in the targeted technologies, with higher parameters (r,N) to improve the performances and address next generation standards.

Among the 2 designed chips, only the CMOS version has been manufactured. Chapter 4 presents the measurement results carried out on PAULINA.

Chapter

4 Measurement results and prospects

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Chapter 4 presents the experimental results obtained with the chip. The prototypes are presented together with the test bench developed to perform the characterization. Several aspects are validated, both concerning the theoretical aspects of the DA conversion and the implementation of the circuit in silicon. The co-integration of the Riemann Pump with a digital control interface and an amplification stage is also demonstrated. Prospects toward the development of a complete transmitter are discussed. System level topologies and the implementation in advanced silicon technologies are envisioned.

Key words: Characterization, Chip, DAC, Measurement, Prototype

4.1 Measurement results

4.1.1 Prototypes Realization

Packaging

The prototyped chip PAULINA was designed in a 65 nm CMOS low power technology from TSMC. Chips are packaged in 64-pin sealed lids QFN package. A picture of the chip in an open QFN64 package is presented in Fig. 4.1, together with a microphotograph of the chip and the associated pinout.

Printed circuit board (PCB)

A custom two layer PCB has been designed for measurement purposes. Different versions of a single generic PCB are derived for each of the circuits. They differ by the filing of the component footprints. The PCB designed for the test of the standalone circuit is presented in Fig. 4.2 together with the experimental setup.

The supplies are provided through voltage regulators, and decoupled with banks of capacitors as close as possible to the chip. Reference and control voltages are tunable thanks to potentiometers. RF lines are routed differentially, with 50 Ω grounded coplanar wave guide topology. All the input differential pairs are matched in length so as to insert an equivalent delay.

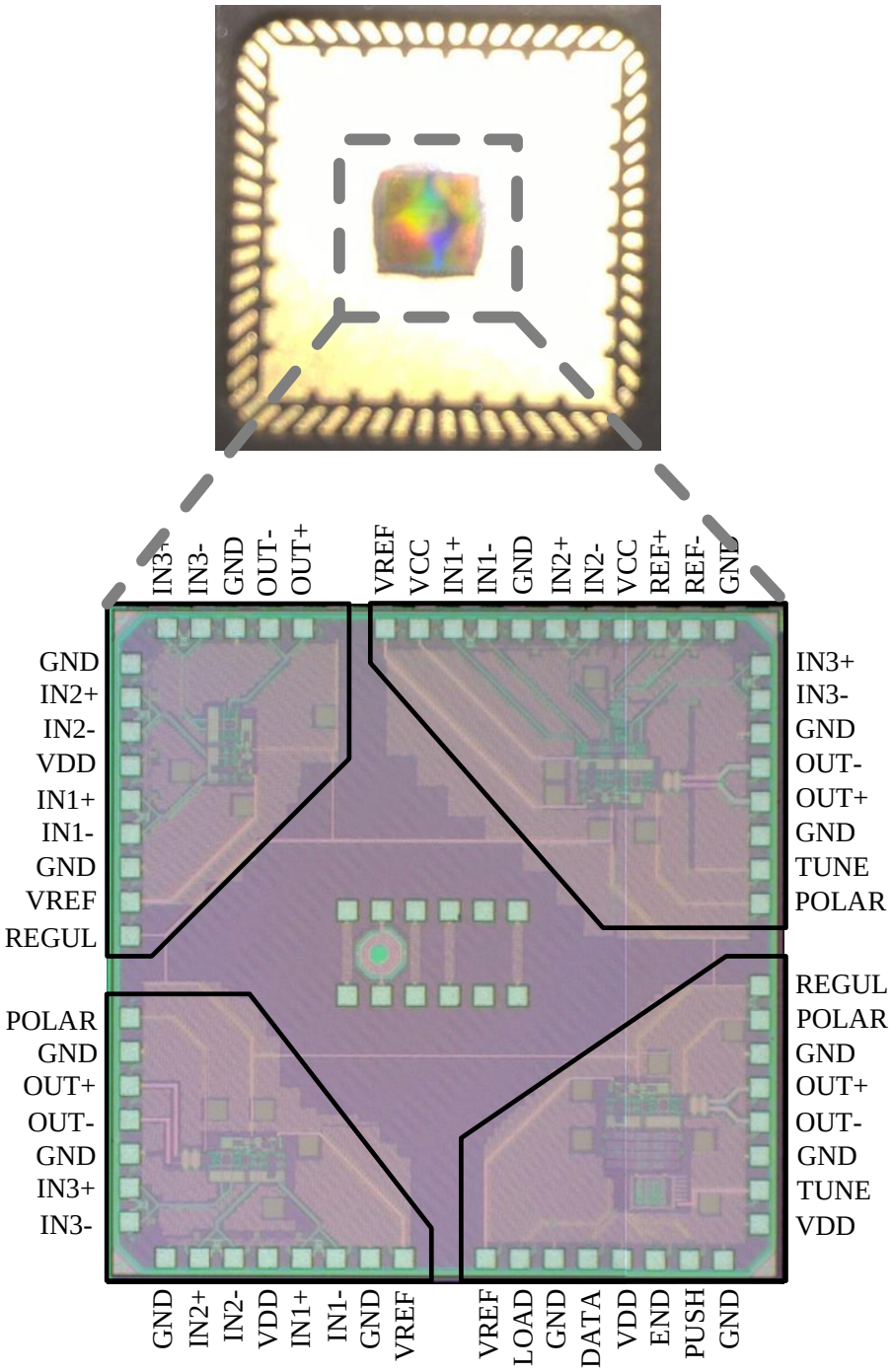

Figure 4.1: Micro photogaph of PAULINA

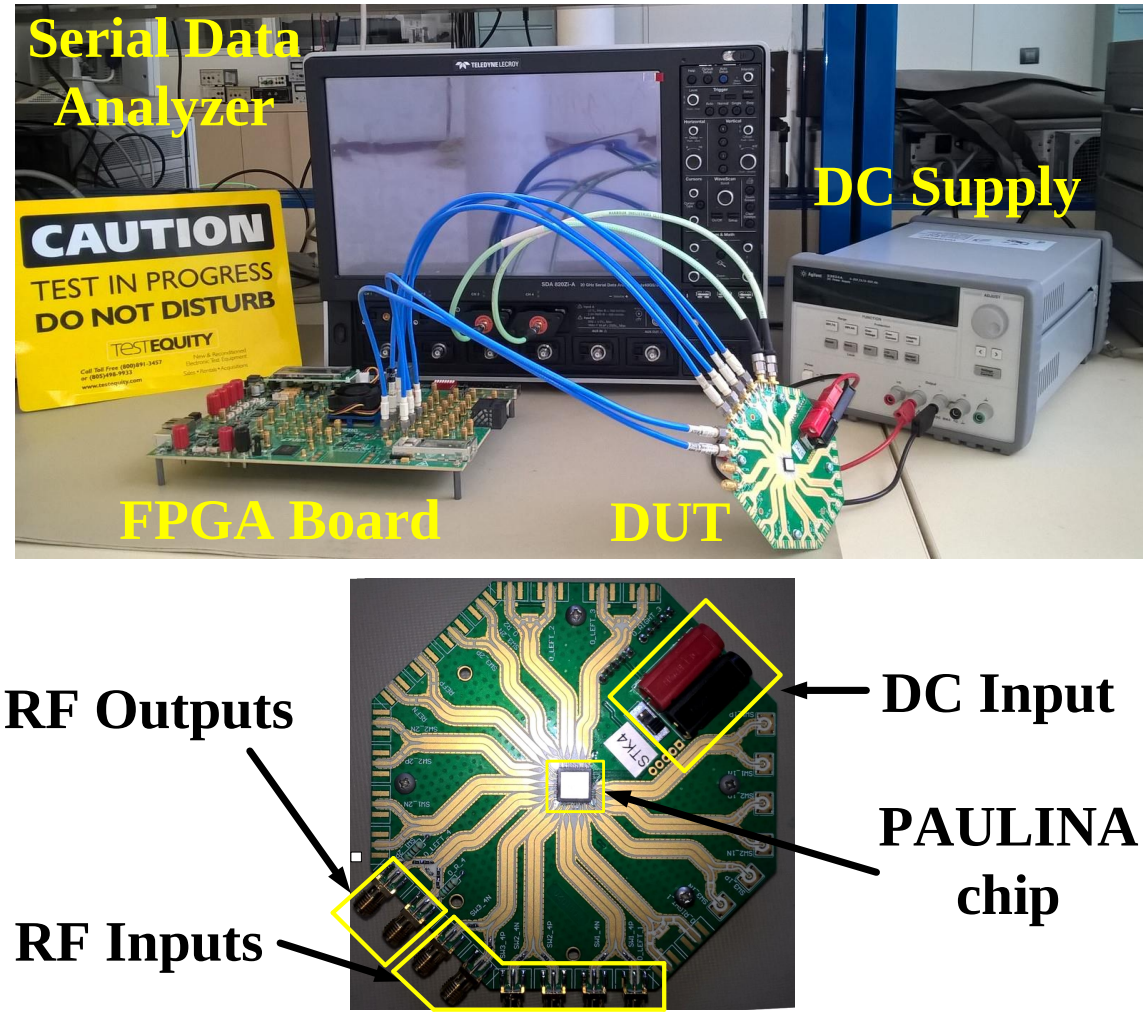

Figure 4.2: Photograph of the test board and the experimental setup

4.1.2 Characterization of the prototypes

The characterization of the Riemann Pump is done along 2 axes associated to 2 different circuits:

- Characterization of the **standalone pump** (CKT3) is done to assess the performances of the Riemann Pump itself.

- Measurements on the **autonomous Pump** (CKT4) evaluate the potentiality of a co-integration of the Riemann Pump with an input digital logic stage and an output amplifier stage.

4.1.2.1 Standalone pump measurements

Test Bench

The test setup of the standalone pump is illustrated in Fig. 4.3.

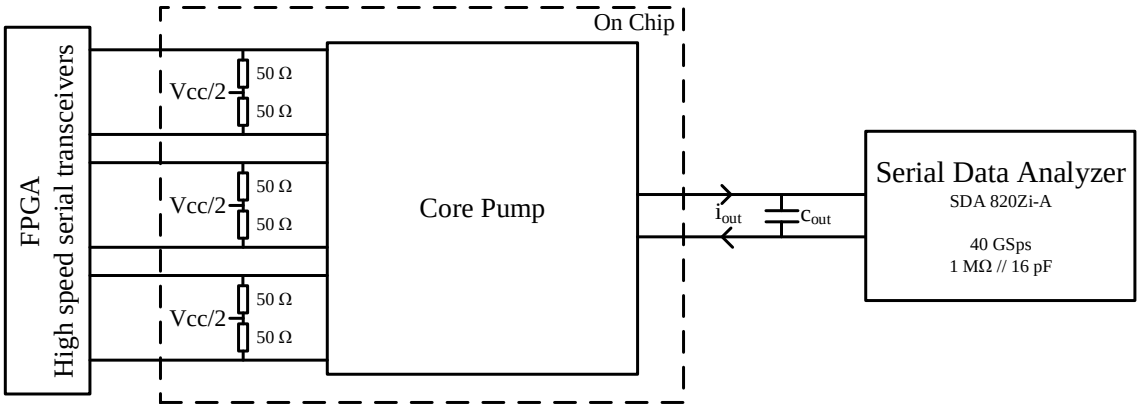

Figure 4.3: Test bench of the standalone pump

FPGA

Stratix V GT signal integrity board has been used to generate the inputs of the Riemann Pump. This board is dedicated to high speed serial transceivers. High speed bit streams are generated as inputs for the Riemann Pump circuits. The implemented configuration allows to set 40-bit depth user defined patterns. A simplified architecture of the pattern generator architecture is described in Fig. 4.4. The hardware configuration and the 40-bit user defined patterns are described in VHDL. The high speed serial transmitters perform the serialization of the bit streams at high speed, based on a frequency obtained thanks to a PLL. The bit stream data rate is set to 12 times the reference frequency, i.e. 7.73475 Gbps.

The interface between the high speed serial transmitters and the test board is depicted in Fig. 4.5. The data channels are connected to the test board through 50 Ω SMA connectors and coaxial cables. The PCB lines are 50 Ω differential traces designed in a coplanar wave guide configuration. The on-chip terminations are 50 Ω resistors connected to a $\frac{V_{cc}}{2}$ common point.

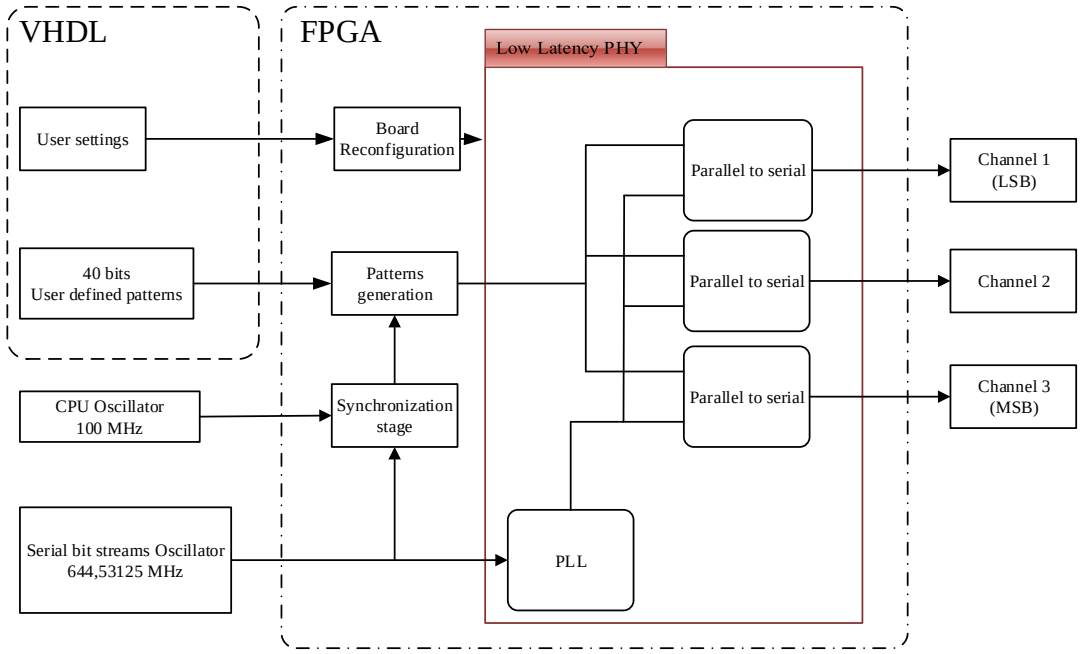

Figure 4.4: FPGA bit stream generator architecture

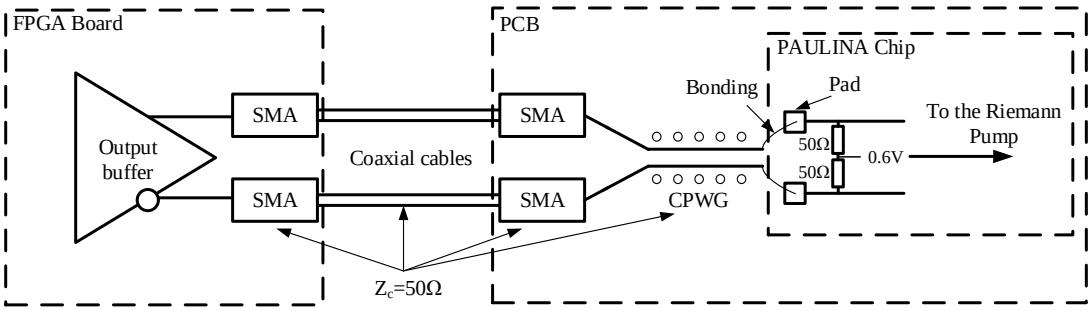

Figure 4.5: FPGA-to-chip physical channel

Serial data analyzer

The output signal of the tested circuit is monitored thanks to a 40 GSps serial data analyzer. The acquisition of the differential outputs of the circuit is performed independently. The two channels are recombined through a mathematical subtraction within the analyzer. The skew between the 3 bit streams generated by the FPGA is measured on the serial data analyzer in a plane corresponding to the input of the test board. The edges of the 3 bit streams are included in a 30 ps interval.

Power consumption

Table 4.1: Standalone pump operating current.

Supply voltage	1.2 V
Simulated operating current	700 μA
Measured operating current	570 μA

The consumption of the pump is approximately 680 μW, which is barely 20% lower than expected. An overall reduction of the operating current within the pump can be explained by a technological shift of the transistors and resistors, especially in the current source reference branch.

Matching of current sources

The static DAC characteristics of the Riemann Pump are assessed thanks to DC measurements. The output capacitor of the Riemann Pump is bypassed by an 82 Ω resistor added in the PCB as depicted in Fig. 4.6. The DC current resulting of the input configuration of the 3 input bits induces an output current which flows through the bypass resistor. The voltage measured across this resistor is directly proportional to the output current.

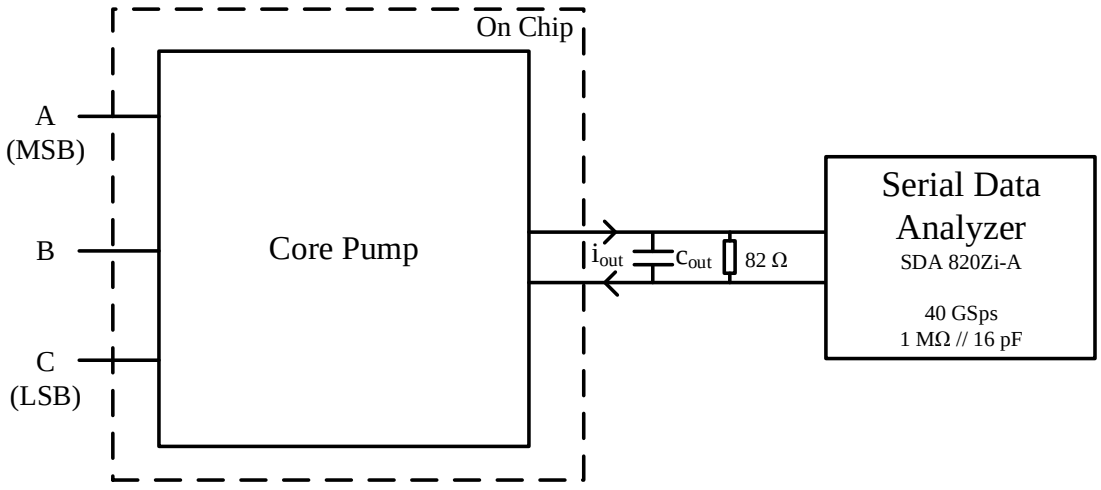

Figure 4.6: DC measurement test bench

Depending on the configuration of its differential input, each input channel has 3 possible states as exposed in Fig. 4.7.

- **+1 level:** a high level on the positive branch and a low level on the negative branch results in a +1 level. The current source controlled by the corresponding bit has a positive contribution on the output current.
- **-1 level:** a low level on the positive branch and a high level on the negative branch results in a -1 level. The current source controlled by the corresponding bit has a negative contribution on the output current.
- **0 level:** if there is a high impedance on both inputs, the two branches are balanced and the corresponding contribution on the output current is null.

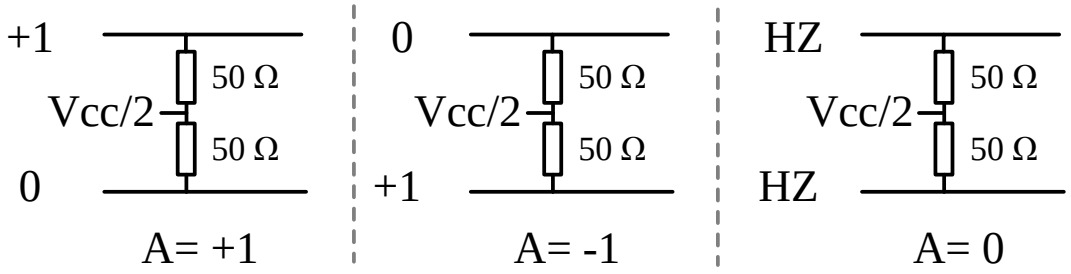

Figure 4.7: DC measurement input configuration

The system is supposed to work only with the +1 and -1 levels for each of the 3 bits, so as to define 8 distinct output currents. However, the third state allows to generate extra levels between the expected output levels. It gives additional information on the matching of the current sources and the linearity of the system. Different input codes have been tested in order to generate levels from -6 to +6 by step of 1; it is to note that the actual LSB corresponds to 2 steps. The results are reported in Table. 4.2 and the DAC transfer characteristic is plotted in Fig. 4.8.

The worst case DNL is approximately 0.25 LSB, while the worst case INL is as low as 0.13 LSB. The matching of the current sources results in a linearity which does not degrade significantly the static ENOB.

Table 4.2: Standalone pump DC linearity.

A(MSB)	B	C(LSB)	Code	Current (μA)	INL	DNL
1	1	0	6	223	0.13	0.15
1	0	1	5	178	-0.02	0.106
1	0	0	4	148	0.03	0.04
1	0	-1	3	110	-0.01	0.08
1	-1	0	2	70	-0.09	0.01
0	1	-1	1	34	-0.11	0.02
0	0	0	0	-1.6	-0.12	-0.25
0	-1	1	-1	-18.3	0.13	0.2
-1	1	0	-2	-67	-0.07	-0.05
-1	0	1	-3	-97	-0.02	-0.14
-1	0	0	-4	-121	0.13	0.08
-1	0	-1	-5	-162	0.05	0.06
-1	-1	0	-6	-201	-0.02	0

Note: Each configuration contains at least one high impedance input. Only two inputs could be forced (at a +1 or -1 level) at the same time because of hardware issues with the FPGA outputs.

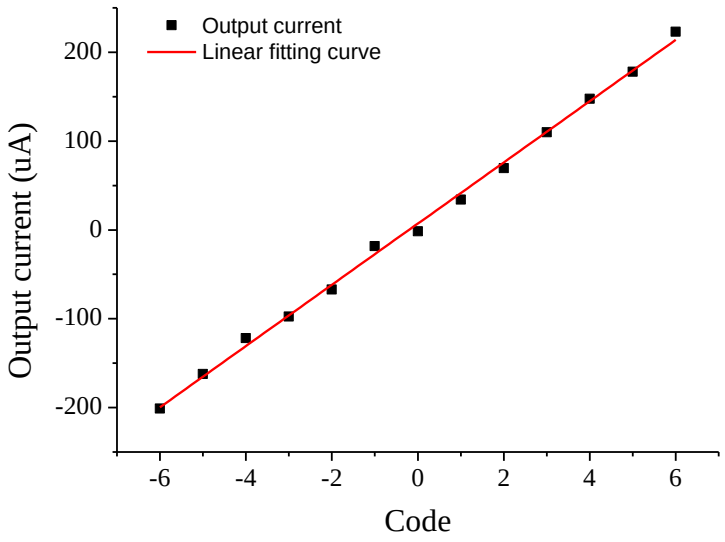

Figure 4.8: Standalone pump transfer function

Dual carriers

The carrier aggregation principle is assessed with the concurrent generation of 2 sine waves. The test bench is the same:

- **FPGA:** 40-bit patterns outputted at $f_s \approx 8GHz$: $f_{max} = 1GHz$ for an oversampling factor $r = 2$. The generated signal periods must have an integer relationship with the 40-bit pattern.
- **Serial data analyzer:** $1M\Omega//16pF$ analyzer input impedance. The high input impedance mode is to be used to sense the output voltage with as low as possible disturbances. However, it results in a limited analog bandwidth ($\approx 1GHz$).

Taking into account these limitations and constraints, the frequency of the generated sine waves is set to $\frac{2f_s}{40}$ ($\approx$ 400 MHz) and $\frac{3f_s}{40}$ ($\approx$ 600 MHz) respectively.

The Riemann code of the wanted signal is processed and the 3 resulting bit stream patterns are set in the VHDL code. The 40-bit depth patterns are then outputted continuously and the waveform is sampled and monitored by the analyzer (Fig. 4.9).

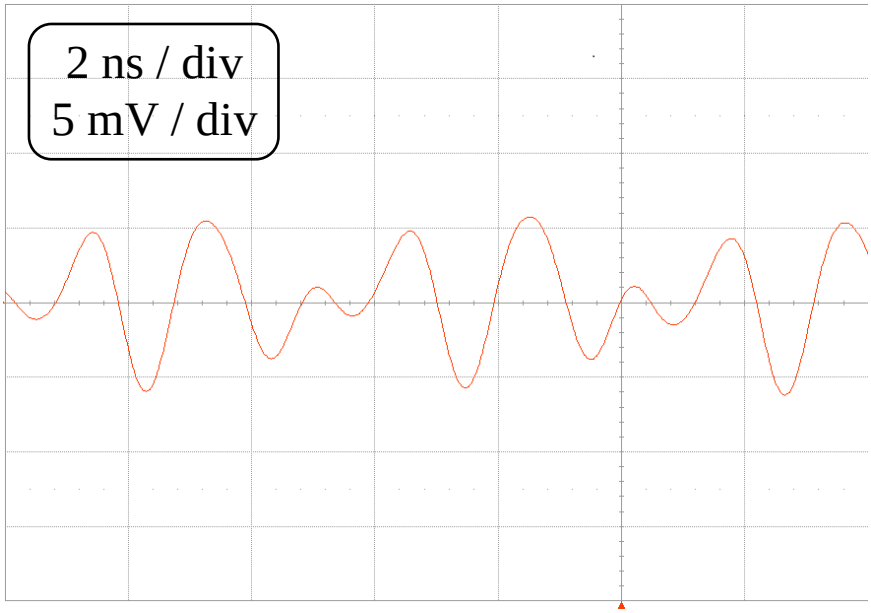

Figure 4.9: Dual carrier transient waveform

The corresponding spectrum is displayed and compared with the equivalent signal generated with the Matlab simulation of the Riemann Pump in Fig. 4.10.

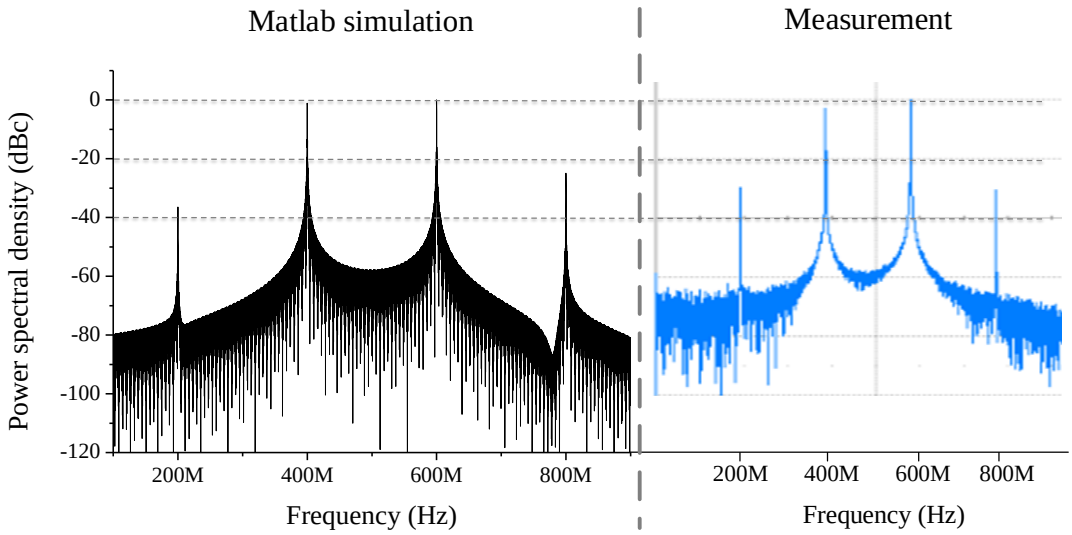

Figure 4.10: Dual carrier spectrum

Table 4.3: Dual carrier spectral components - measurements versus theory.

Frequency (MHz)	**Theoretical level (Matlab)**	**Measured level**
200	-35 dBc	-30 dBc
400	-2 dBc	-2 dBc
600	0 dBc	0 dBc
800	-25 dBc	-30 dBc

The comparison of the simulated signal and the measured signal in the band of interest underlines the similarity of the results. The relative level of the two carriers is concordant with their theoretical level. The 200 MHz and 800 MHz spurious tones exhibit a similar level, with a slightly different balance. The 800 MHz component might be attenuated by the analyzer.

Variation of the oversampling factor r

The impact of the oversampling factor on the signal generation quality is assessed. The test bench imposes the same limitations as previously:

- Limited analog frequency for the HZ analyzer inputs
- 40-bit patterns outputted at 8 Gbps for the input streams

The generation of a 400 MHz CW is chosen as the reference to assess the impact of the over-

sampling factor r. The Riemann code of such a sine wave is computed with Matlab in two configurations:

- $f_s = 8GHz$ and $f_{max} = 1GHz$, $OSR = \frac{f_s}{2.f_{max}}$ and $r = 2$.
- $f_s = 8GHz$ and $f_{max} = 400MHz$, $r = 3.32$.

The output spectrum of the two signals generated with Matlab are plotted in Fig. 4.11.

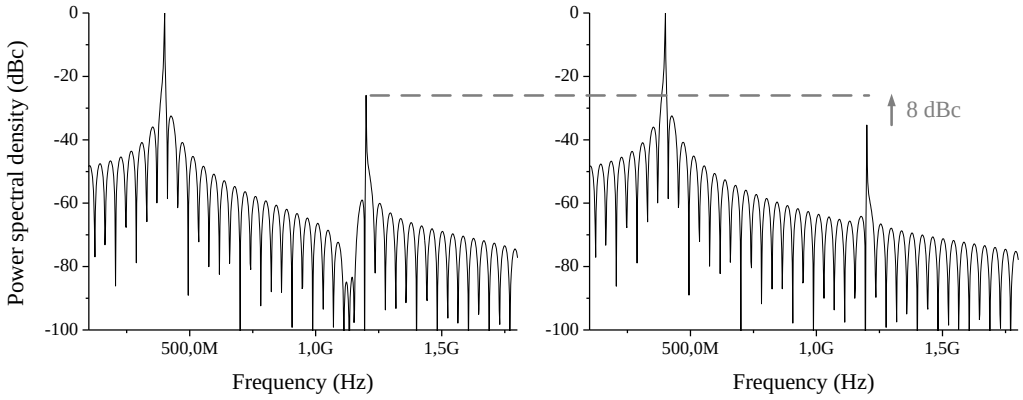

Figure 4.11: Variation of the oversampling factor r - theoretical spectra

The theoretical impact of the oversampling factor is an improvement of 9 dB of the SNR per doubling of the OSR, which also translates into a 9 dB decrease of the quantization noise floor in the spectrum. Among those 9 dB, 6 dB are related to the differential coding and the associated reduction of the quantization error, while the extra 3 dB are related to the spreading of the noise floor. This last effect is valid only when the quantization error is random enough to be considered as a quantization noise with a uniform spectral distribution. The generated signal is defined by a 40-bit pattern, and its frequency has an integer relationship with the working frequency f_s. As a consequence, all the power of the quantization error is located in the harmonics of the generated signal. The SNR is thus related to harmonic distortion.

In the present case, the third harmonic is the main contributor in the noise power. The third harmonic level is reduced by 8 dB while the oversampling factor goes from 2 to 3.32. It corresponds to a dependence in 6r in the SNR, which is consistent with the theory. The same signals have been generated by the actual circuit, measured and presented in Fig. 4.12. The level of the third harmonic with respect to the fundamental tone is reported and compared to the theoretical signals in Table. 4.4.

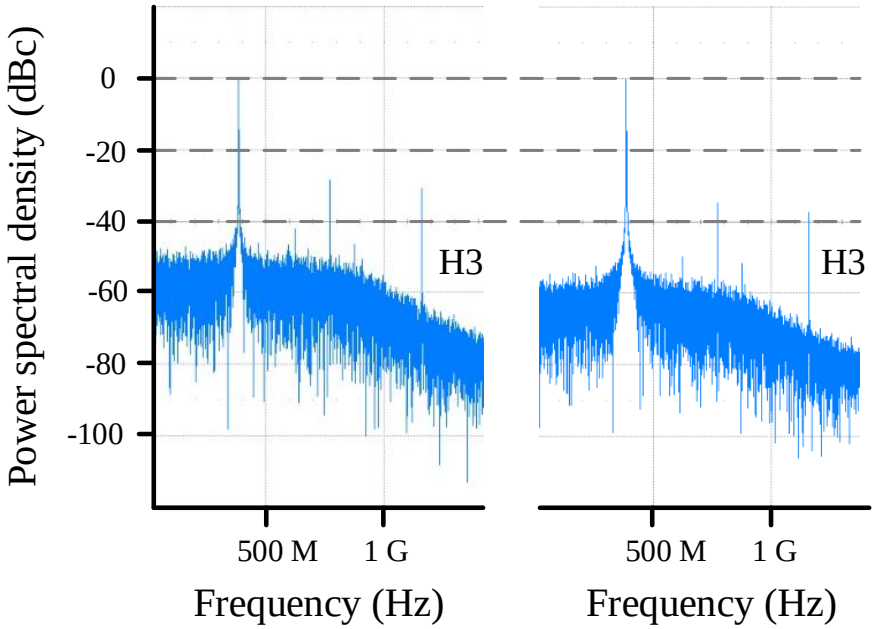

Figure 4.12: Variation of the oversampling factor r - measured spectra

Table 4.4: Third harmonic level - measurements versus theory.

$f_{max}(GHz)$	**Oversampling factor r**	**Theoretical signal (Matlab)**	**Measured signal**
0.4	3.32	-35 dBc	-38 dBc
1	2	-27 dBc	-30 dBc
		$\Delta : 8dBc$	$\Delta : 8dBc$

The measured levels appear to be lower than the theoretical ones because of the low-pass filtering behavior of the analyzer inputs. However, the relative levels are consistent with the theory and validate the impact of the oversampling factor r. One can notice the presence of the second harmonic in the measured signals whereas it should not appear theoretically. It is due to a mismatch between the two differential outputs.

The measurements on the standalone pump are restricted in frequency and configuration of input signals because of the measurement setup. However, major characteristics have been extracted and validated:

- **DAC features:** static linearity and high speed operation with low power consumption.
- **Architecture features:** impact of the OSR, carrier aggregation.

4.1.2.2 Autonomous pump measurements

The second circuit to be tested is the autonomous pump. This circuit is made of an integrated digital pattern generator with 8-bit depth on each of the 3 channels, a Riemann Pump, and a pre-power amplifier which acts as the capacitive load of the pump.

Test bench

The autonomous pump is controlled thanks to a custom 3 bit serial interface driven by an Arduino (Fig. 4.13). The communication protocol is depicted in Annex (Fig. 5.11). The 3x8 bits are pushed in the CKT4 FIFO and stored in latches. They are addressed sequentially at a rate given by the internal oscillator whose frequency is controlled by a voltage V_{tune}. The resulting signal is generated by the Riemann Pump and monitored on the data analyzer. The inputs of the analyzer are set to 50 Ω because the output PPA is able to drive such loads.

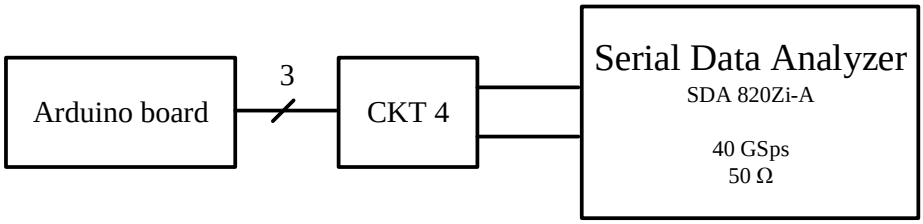

Figure 4.13: Test bench of the autonomous pump

Power consumption

Table 4.5: Autonomous pump operating current.

Supply voltage	1.2 V
Measured operating current	48 mA

The consumption of the core pump is negligible in the front of the digital interface and the PPA, which draw approximately 20 mA each for a total power consumption of 58 mW.

Triangle waveform generation

The 8-bit patterns enable the generation of simple waveforms. The chosen signal is a triangle wave made of 8 slopes, to evidence the integration of the switched currents into the capacitive input impedance of the PPA. The signal is programmed in the Arduino, sent to the CKT4 serial to parallel digital interface and then loaded in the internal latches. The signal obtained at the output is depicted in Fig. 4.14, both in the time and the frequency domain. Table. 4.14 gathers

the level of the first two harmonics and compares it with simulation results.

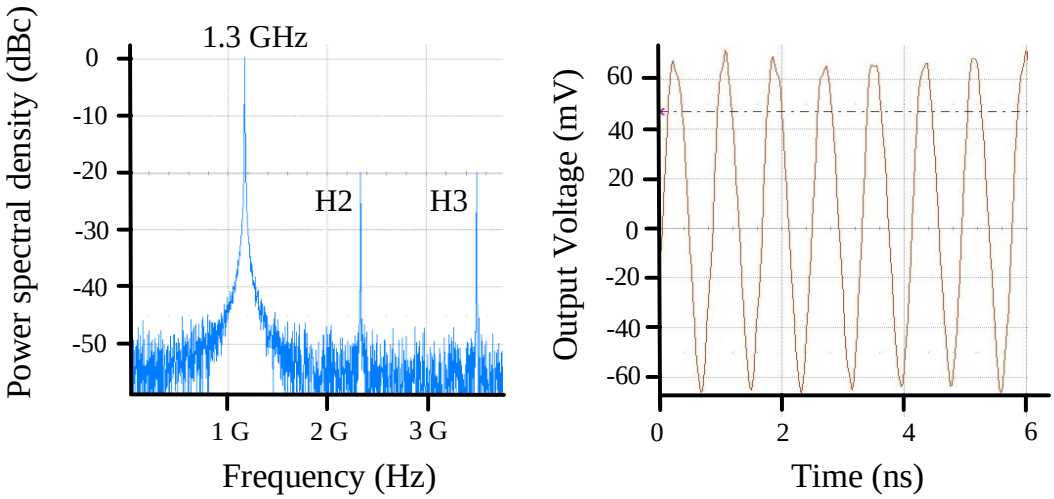

Figure 4.14: Triangle signal spectrum and waveform

Table 4.6: Triangle signal harmonic level.

	Simulation - single	**Simulation - differential**	**Measurement - differential**
H2	-15 dBc	< -60 dBc	-20 dBc
H3	-20 dBc	-20 dBc	-20 dBc

A 1.3 GHz triangle wave is generated across the 50 Ω loads with 125 mV_{pp} amplitude. The power spectral density underscores the presence of the second and third harmonics both at -20 dBc. The level of the third harmonic is the same as the one of the signal generated with Matlab. Nevertheless, in a similar way as the previous circuit measurements the second harmonic is present and reflects a mismatch in the differential architecture. The signal waveforms obtained on single output branches with schematic simulations exhibit second harmonics with a -15 dBc level but the differential recombination cancels it properly. In the actual measurements, the level of this second harmonic equals -20 dBc in differential mode, which corresponds to a decrease with respect to the single branches, but not a complete cancellation. It could be related both to the circuit operation and the channel mismatches (including bondings, package, PCB traces, connectors and coaxial cables).

Pattern generator operating frequency

The internal oscillator frequency is tunable through an external voltage. The same triangle

signal is generated while the frequency tuning voltage is swept from 200 mV to 700 mV. The frequency of the oscillator equals 8 times the frequency of the output triangle. The obtained frequencies are presented in Fig. 4.15, together with the schematic and post-layout simulations.

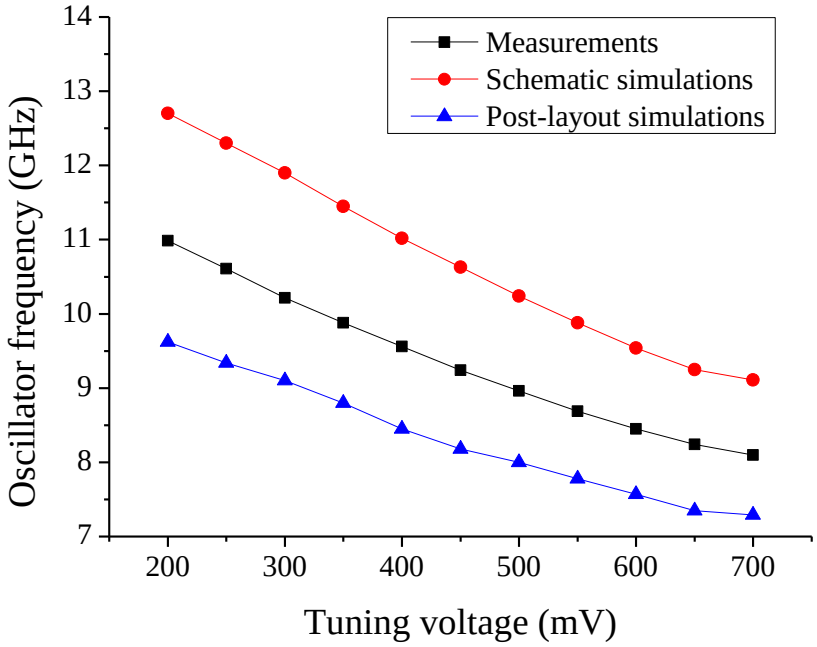

Figure 4.15: Oscillator frequency versus tuning frequency

The operating frequency of the pattern generator decreases as the tuning voltage increases. The tendency observed in measurements is similar to the simulations, but a frequency shift is observed. The actual oscillator is slower than targeted with schematic simulations, but faster than expected after parasitic extractions. The implemented topology is an 8-stage differential ring oscillator made of differential CMOS inverters. The running frequency is not locked and it is substantially dependent on the transit time of the inverters, the capacitive parasitic elements and the temperature. The obtained frequencies remain in the targeted range of 10 GHz, with a tuning interval of almost 3 GHz. The measurements of the autonomous pump validates the compatibility of the Riemann Pump with a complete transmission chain:

- The co-integration with an uphill high speed digital conditioning block.
- The direct interfacing with a downhill capacitive power amplification stage.

4.2 Prospects

4.2.1 Complete transmitter architecture

The realization of a complete transmitter based on the Riemann Pump requires a digital processing core and a power amplification stage (Fig. 4.16).

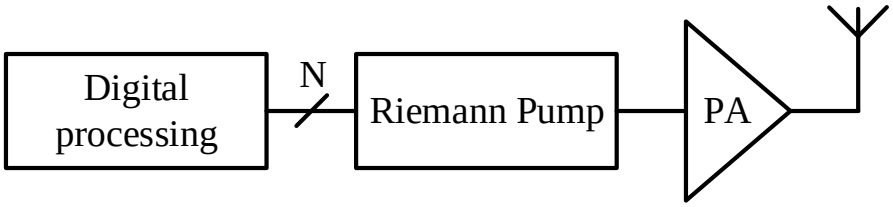

Figure 4.16: Complete transmitter based on the Riemann Pump

Digital processing co-integration and optimizations

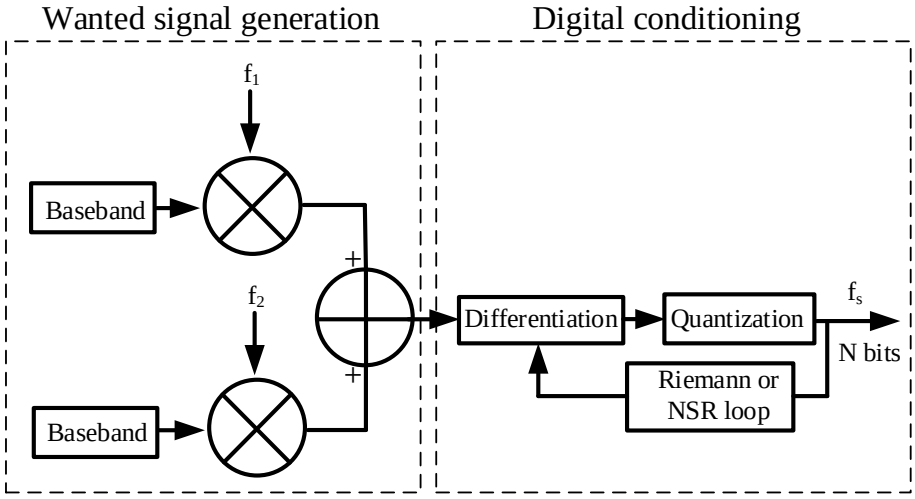

Figure 4.17: Digital processing and conditioning stage (concurrent generation of 2 channels)

The digital processing core basically handles the baseband signal generation, the up-conversion to carrier frequencies, the signals combination, and the Riemann or NSR conditioning (Fig. 4.17) The overall working frequency of the system is limited by the digital signal processing stage and the interconnections with the Riemann Pump. A development and co-integration of the digital blocks and the Riemann Pump in an ASIC would enable to optimize the working frequency and the consumption of the overall system. The target technologies are the most advanced CMOS nodes which favor digital signal processing performances.

The potential development of the Riemann Pump in the 28 nm CMOS FDSOI technology from ST Microelectronics has been assessed. A schematic version of the Riemann Pump and an associated high speed digital interface have been designed. The estimated potential working frequency is 40 GHz for the Riemann Pump and its high speed serial interface. The back gate control on transistors allows to either improve their speed or cut down their leakage current. This additional lever significantly improves the performances of digital circuits in terms of working frequency and consumption.

The very high flexibility of the proposed transmitter architecture induces constraints on the digital calculation core which deals with a lot of data volume because of the high speed processing. Smart algorithms should be used to alleviate the calculations, especially for real-time applications. Several of the envisioned techniques are listed below:

- **Time interleaving**: the high speed interface between the digital computing core and the Riemann Pump can suffer from low pass effects of parasitic elements. Time interleaving could relax the sampling rate by splitting the input bit streams of the Riemann Pump and combining them with an adequate phase shift.

- **Parallel computing**: the frequency of the high speed bit streams generated to control the Riemann Pump switches is too high for the whole calculation chain. Parallel calculations and serialization of the data in a final stage allow to reach the required speed.

- **Modular arithmetic**: the up-conversion step in the digital processing core consists in carrying baseband signals at a wanted frequency. The generation of a given frequency f_1 with a fixed working frequency f_s involves modular arithmetic. The primality relationship between the frequencies and the associated time periods plays a role on the potential complexity of the calculations. Smart algorithms are needed to optimize the computational requirements.

- **Redundancies simplification**: a modulated signal corresponds to a symbol sequence carried at a specific frequency. For the most common modulation schemes, a given symbol sequence can be associated to its temporal waveform (which solely depends on the carrier phase at the origin) and hence its Riemann or NSR slope sequence. The up-conversion operation is thus highly redundant. Several waveform samples corresponding to symbol sequences should be calculated only once, stored in memories, and addressed by the baseband symbol stream. It would result in a substantial relief of the calculations.

Power amplification stage

The Riemann Pump architecture is able to generate signals over a wide frequency range. A complete transmitter requires a broadband power amplifier to reach the required output power. As far as handset devices are concerned, the PA is subject to a trade-off between bandwidth, linearity and efficiency. Depending on the applications, the overall transmitter architecture can include a single wideband PA or several narrowband PAs with a suitable recombination (Fig. 4.18).

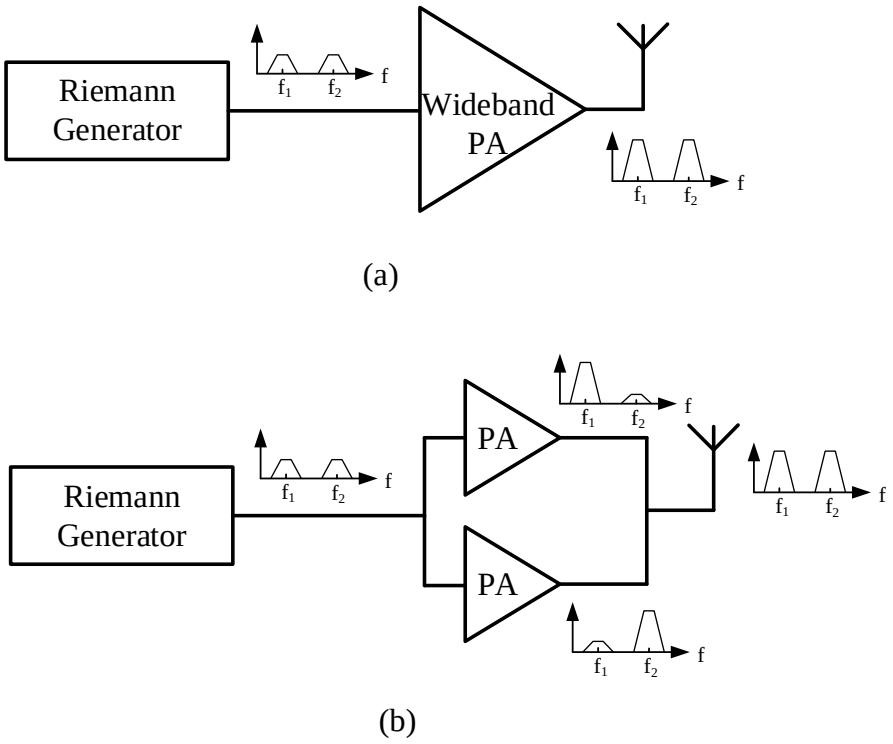

Figure 4.18: Power amplification stage topology (a) single wideband PA (b) multiple-path PA

The PA has a preponderant role in the transmitter power budget. The stringent requirements in terms of efficiency could result in a degraded linearity. The waveform generated at the input of the PA is completely determined by software because the only analog front-end stage in the Riemann Pump. Hence, the PA non-linearities can be characterized and compensated thanks to digital pre-distortion. This computation step should be inserted within the digital calculation chain.

4.2.2 Riemann receiver

The principle exposed and exploited all along this manuscript is applied to the transmitter side of a transceiver. All the exposed theoretical features concerning the DA conversion schemes are compatible with the receiver side, where is becomes AD conversion. The variations of a received signal are quantized and sampled instead of its absolute value. The corresponding architecture is depicted in Fig. 4.19.

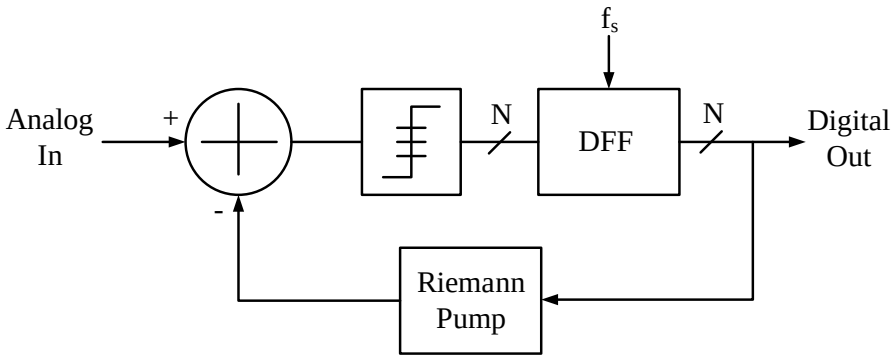

Figure 4.19: Differentiating receiver based on the Riemann Pump

A delayed reconstructed version of the analog signal is subtracted to himself, so as to qantize its derivative. The reconstructed version is generated thanks to a Riemann Pump which performs the integration of the quantized derivative. The digital output is representative of the derivative of the analog input signal, clocked at the sampling frequency f_s.
Such a receiver alleviates the AD conversion cost and leads to the development of a software radio receiver. It is an axis of research to develop a full software radio transceiver base on differentiating conversion schemes, both in the transmitter and the receiver path.

4.3 Conclusion

The characterization of PAULINA validates the principle of an RF transmitter based on the Riemann Pump. The standalone pump circuit is a kind of RF-DAC. Table. 4.7 compares the Riemann Pump with the state-of-the-arf RF-DACs. The figure of merit chosen to compare the DACs is the energy cost of the conversion step (in fJ/conv):

$$FOM = \frac{Power}{2^{ENOB}.BW} \tag{4.1}$$

Table 4.7: State-of-the-art of RF-DACs.

Reference	**ENOB***	**BW* (GHz)**	**Consumption (mW)**	**Process**	**Active area** (mm^2)	**FOM** ($fJ/conv$)
[33]	6	14	2250	90 nm CMOS	0.28	2511
[37]	9	2.5	375	40 nm CMOS	1.65 (chip)	293
[34]	14	3.6	3600	BiCMOS	112	78
[32]	12	1.45	188	65 nm CMOS	0.31	31.6
[35]	14	3	600	180 nm CMOS	28.5	12.2
[36]	13	4.5	360	28 nm CMOS	1.16	9.7
Riemann Pump - NSR conversion	5.4	3.125	0.68	65 nm CMOS	0.2	5.1

* *Measured values are not available for all the references. The ENOB and bandwidth are the nominal theoretical values.*

The Riemann Pump associated with the NSR coding scheme exhibits the best figure of merit, with 5.1 fJ per conversion step. Furthermore, the active area of the presented circuit is the smallest of the reported chips. It highlights the potential of the presented topology to develop a low power and low cost software radio transmitter for the next generation of wireless communications.

Conclusion

The conversion between the digital data and the analog signal suited for radio transmission is a key enabler for the development of wireless technologies. A lot of researches deal with next generation converters. It mostly involves classical data conversion schemes implemented in recent silicon technologies. This approach is not able to address the stringent expectations of forthcoming standards.

This thesis proposes a disruptive architecture of transmitter that operates the conversion via the derivative of the signal before an integration in the analog domain performed by a DAC named the Riemann Pump. The underlying conversion scheme benefits from the OSR to improve the SNR; a doubling of the sampling frequency results in a 9 dB increase, plus an additional 6 dB with the insertion of a 1st order noise shaping loop within the quantization block.

The design of the Riemann Pump in a 65 nm silicon technology from TSMC underlines its high speed operation capability, with digital command up to 25 Gbps, and its sub-mW consumption. The resulting ENOB is approximately 5.4 bits for an output bandwidth larger than 3 GHz. The energy cost of the developed circuit is better than the state-of-the-art RF-DACs, with an energy cost of approximately 5 fJ/conv. step.

A demonstrator of the Riemann Pump has been sent to foundry and characterized. The obtained results bring a proof of concept. The co-integration with a digital processing block and an output amplifier are also demonstrated. Virtually unlimited user defined patterns, very high frequency operation and real-time signal generation are still to be developed in the test bench to go further in the characterization of the prototyped chip.

Next generation wireless communication standards are expected to meet unrealistic specifications, with a factor of 10 improvement in all the key performances (including data rate and power consumption). It would require a breakthrough in the reduction of the cost of information in terms of energy. The implementation of classical architectures in the most recent technologies will not be sufficient to meet such goals.

The approach developed in this thesis is in the trend of Design by Mathematics philosophy. It proposes to develop disruptive circuits and systems thanks to the adequacy between mathematical principles and their electronical implementation.

Publications and communications

Patents

[P1] Y. Veyrac, F. Rivet, Y. Deval, P. Garrec, R. Montigny, "Dispositif de génération de signaux analogiques et utilisation associée", Patent Pending 1502176.

Journals

[R1] Y. Veyrac, F. Rivet, Y. Deval, D. Dallet, P. Garrec, R. Montigny, "A 65 nm CMOS DAC Based on a Differentiating Arbitrary Waveform Generator Architecture for 5G Handset Transmitter", *in IEEE Transactions on Circuits and Systems II (TCAS-II)*, 2015.

[R2] F. Rivet, Y. Veyrac, Y. Deval, P. Garrec, "Adaptive Interference Cancellation using a Sampled Analog Signal Processor", *in IET Radar, Sonar & Navigation*, 2015.

International conferences

[C1] Y. Veyrac, F. Rivet, Y. Deval, D. Dallet, P. Garrec, R. Montigny, "The Riemann Pump: a Concurrent Transmitter in GaN Technology", *in IEEE International Conference on Circuits and Systems (ICECS)*, Marseille, France, December 7-10, 2014.

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Chapter

5

Annexes

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5.1 Distribution of the slopes set

Fig. 5.1 depicts the principle of signal reconstruction. The wanted signal is represented in solid line.

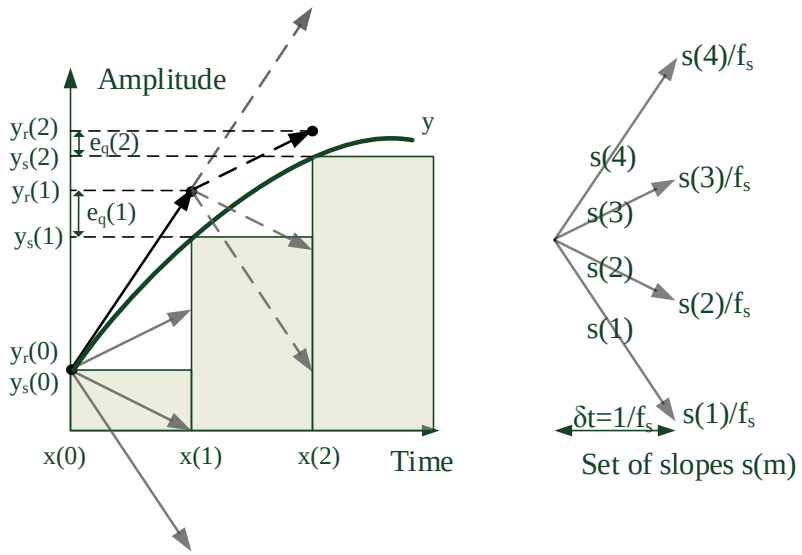

Figure 5.1: Riemann reconstruction process

For our purpose, we will consider zero-mean signals that cover a significant part of the dynamic range [-V, +V], with high enough frequency components. It is generally the case for modulated signals. Under this assumption, starting from any step of index k, the next targeted point $y_s(k+1)$ could be situated anywhere in the interval delimited by the steepest positive slope $s(2^N)$ and the steepest negative slope $s(1)$, with the same probability. The quantization error $e_q(k+1)$ is thus calculated as the minimum distance between the aim $y_s(k+1)$ and each reachable point $y_r(k) + \frac{s(l)}{f_s}$, where l belongs to [1, 2^N]; the point that achieves this minimum, chosen as $y_r(k+1)$.

The example given (Fig. 5.2) corresponds to N=2, with any distribution of the slopes. The dashed line represents the probability density of $y_s(k+1) - y_r(k) = \Delta y$; the above assumption leads to a constant value for this function over the interval delimited by the extreme slopes $s(1)$

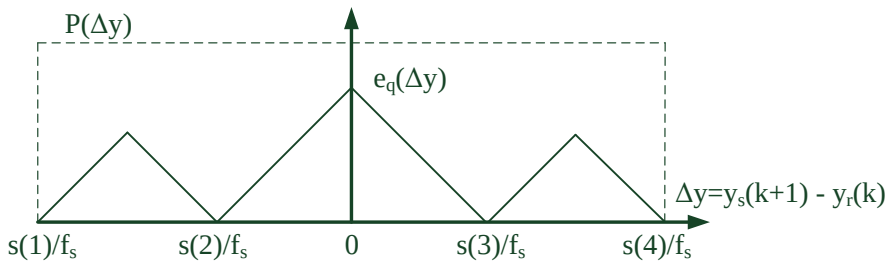

Figure 5.2: Quantization error versus the relative position of the next targeted point (Δy)

and $s(2^N)$. This value equals $\frac{f_s}{[(s(4)-s(1)]}$ so that its integral over the whole interval is one. The quantization error e_q produced is plotted (solid line) versus Δy. This error can be expressed as a quantization noise; the distribution of slopes that produces the minimum quantization noise power has then to be determined. This power can be expressed as:

$$\sigma_e^2 = \int_{s(1)}^{s(2^N)} e_q^2(\Delta y).p(\Delta y)d\Delta y = \sum_{m=1}^{2^N-1} \int_{s(m)}^{s(m+1)} e_q^2(\Delta y).p(\Delta y)d\Delta y \tag{5.1}$$

Let us note $I_m = [\frac{s(m)}{f_s}; \frac{s(m+1)}{f_s}]$ of length $J_m = \frac{s(m+1)-s(m)}{f_s}$, and $J_{tot} = \frac{s(2^N)-s(1)}{f_s}$.

The function e_q over each interval I_m is a triangular shaped function with unity slope with respect to Δy. The power of the quantization noise integrated over any interval I_m is thus:

$$\int_{I_m} e_q^2(\Delta y).p(\Delta y)d\Delta y = \frac{1}{I_{tot}}.2.\int_o^{\frac{J_m}{2}} \Delta y^2.d\Delta y = \frac{2}{I_{tot}}[\frac{\Delta y^3}{3}]_0^{\frac{J_m}{2}} = \frac{{J_m}^3}{12.I_{tot}} \tag{5.2}$$

It gives a total power of:

$$\sigma_e^2 = \frac{1}{12.I_{tot}} \sum_{m=1}^{2^N-1} {J_m}^3 \tag{5.3}$$

Previous problem is equivalent to finding the interval subdivision that minimizes the sum: $\sum_{m=1}^{2^N-1} {J_m}^3$, for any N. Let us demonstrate a first lemma:

***Lemma 1**: Given any real interval I of length J, the subdivision in two intervals I_1 and I_2 of respective length J_1 and J_2 that minimizes the quantity $J_1^3+J_2^3$ is the uniform subdivision, such that $J_1 = J_2$.*

Demonstration:
Let x be a real such that $J_1(x) = x$, and $J_2(x) = J - x, x \in [0, J]$. The quantity of interest is:

$$S(x) = J_1(x)^3 + J_2(x)^3 = x^3 + (J - x)^3 \tag{5.4}$$

The calculation of the derivative gives:

$$S'(x) = 3x^2 - 3(J - x)^2 \tag{5.5}$$

$$S''(x) = 6x + 6(J - x) = 6J \tag{5.6}$$

The first derivative vanishes for:

$$x^2 = (J - x)^2 \tag{5.7}$$

Provided $J \neq 0$, the unique solution of the equation gives $x = \frac{J}{2}$, that corresponds to an extremum of the function S; this extremum being a minimum since the second derivative of S is always positive. The quantity $J_1^3 + J_2^3$ is thus minimized when $J_1 = J_1 = \frac{J}{2}$, i.e. for a uniform subdivision.
Let us now demonstrate the following proposition.

***Proposition:** Given any real interval I of length J, the subdivision in M intervals $I_1, ..., I_M$ of respective length $J_1, ..., J_M$ that minimizes the quantity $J_1^3 + ... + J_M^3$ is the uniform subdivision, such that $J_1 = ... = J_M$.*

***Demonstration** (reduction ad absurdum):*
Let us assume the subdivision that minimizes the quantity $S = J_1^3 + ... + J_M^3$ is not the uniform subdivision. Let $(I_1, I_2, ..., I_M)$ of respective length $(J_1, J_2, ..., J_M)$ be this subdivision; it thus provides a minimal S. Two integers j and k exist such that $J_j \neq J_k$.

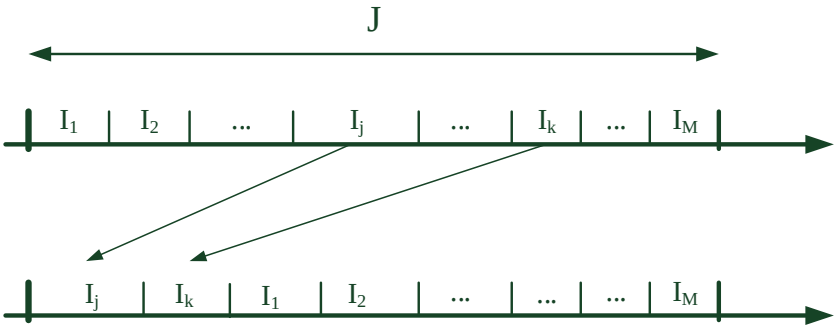

Figure 5.3: Intervals re-arrangement

It is always possible to rearrange the intervals such that I_j and I_k become contiguous. The process described in Fig. 5.3 presents a method to obtain that kind of subdivision. The intervals I_j and I_k are moved toward the first two positions of the global interval I, while all the others are pushed upward accordingly. The length of every interval remains unchanged and the quantity S too. It is now possible to consider the interval I_{jk} of length J_{jk} that is the union of the intervals I_j and I_k. The quantity S can be expressed as:

$$S = \sum_{m=1}^{M} J_m^3 = J_j^3 + J_k^3 + \sum_{m \in [1;M] \setminus \{j,k\}} J_m^3 \tag{5.8}$$

(I_j, I_k) represents a subdivision of the interval I_{jk}, which is not uniform since $J_j \neq J_k$. The lemma 1 states the uniform subdivision that cleaves the interval I_{jk} into two intervals (I'_j, I'_k) of length $J'_j = J'_k = \frac{J_{jk}}{2}$ verifies:

$$J'_j{}^3 + J'_k{}^3 < J_j{}^3 + J_k{}^3 \tag{5.9}$$

Let us consider the subdivision that replaces the intervals I'_j and I'_k by the interval I'_j and I'_k. This subdivision is noted $(I'_j, I'_k, I'_1, I'_2, ..., I'_M)$, with respective length $(J'_j, J'_k, J'_1, J'_2, ..., J'_M)$. The calculation of the quantity S' gives:

$$S' = \sum_{m=1}^{M} J'_m = {J'_j}^3 + {J'_k}^3 + \sum_{m\in[1;M]\setminus\{j,k\}} {J_m}^3 < {J_j}^3 + {J_k}^3 + \sum_{m\in[1;M]\setminus\{j,k\}} {J_m}^3 \tag{5.10}$$

i.e:

$$S' < S \tag{5.11}$$

The starting assumption is then false and it is demonstrated that the subdivision that minimizes the quantity $S = J_1^3 + ... + J_M^3$ is the uniform distribution.

5.2 Digital circuits details

5.2.1 CKT2: re-clocked pump

The synchronization of input data streams is performed thanks to a reference clock coming from the same bit streams generator. A frequency doubler is designed (Fig. 5.4), based on a combination of the input signal and a delayed version (in quadrature). The generated clock is used to synchronize the data streams thanks to dynamic delay flip-flops (Fig. 5.5).

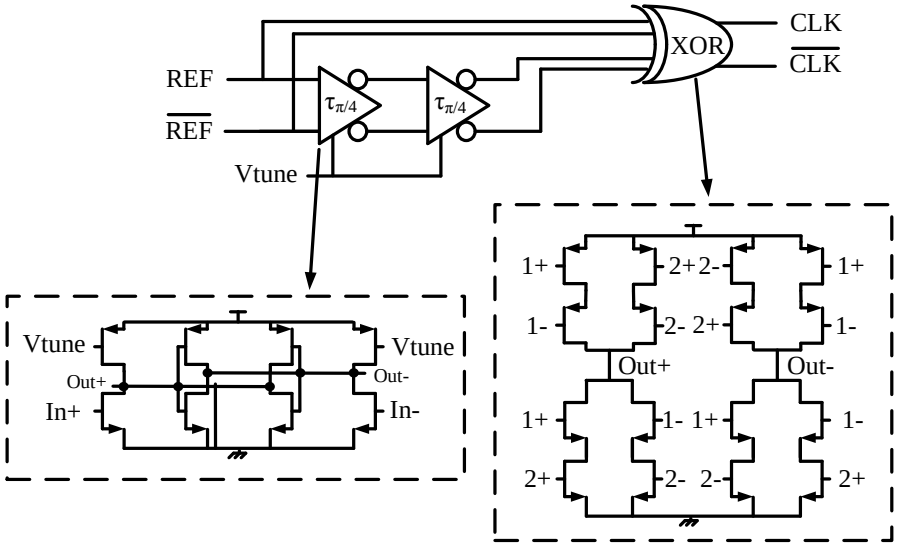

Figure 5.4: Frequency doubler block diagram

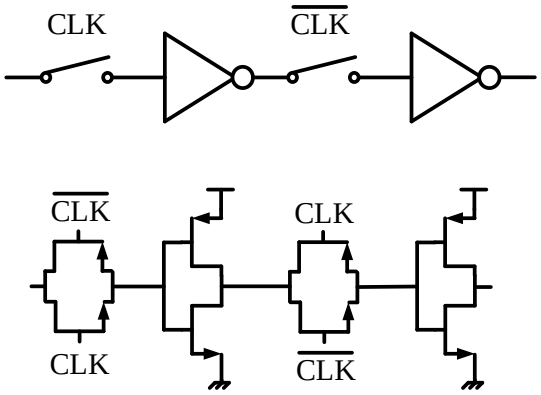

Figure 5.5: Dynamic flip flops schematic

The resynchronization of the 3 input signals is depicted in Fig. 5.6. The generated clock signal captures the values of the input signals and releases them at the same time, after a delay. The layout of the whole resynchronization block is displayed in Fig. 5.7.

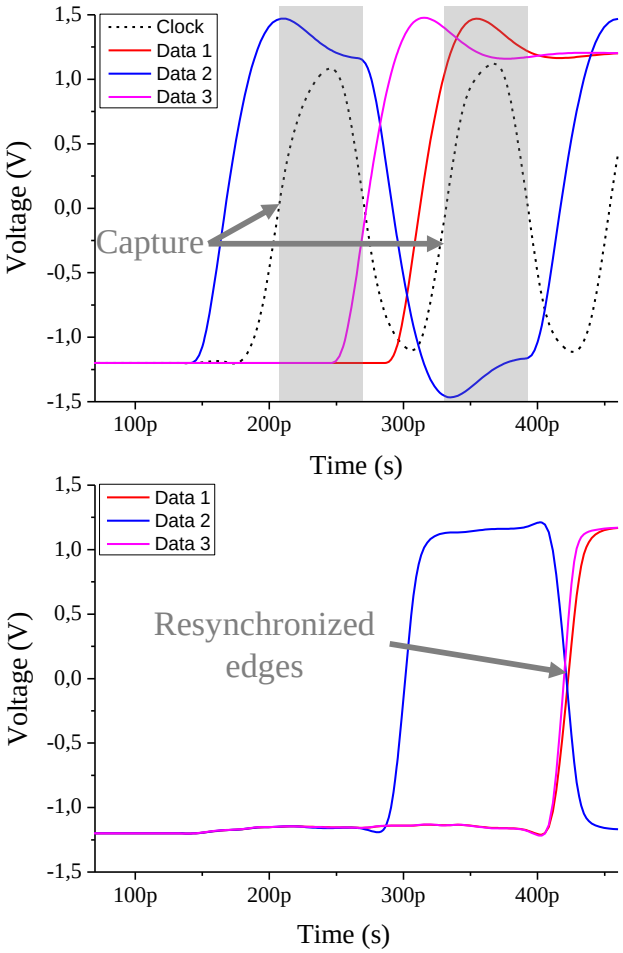

Figure 5.6: Re-synchronization process

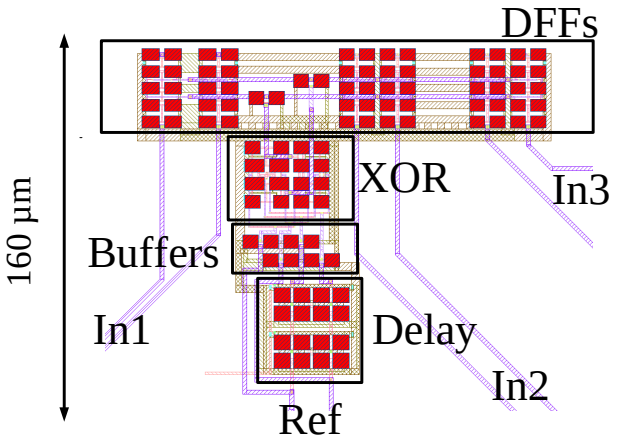

Figure 5.7: Layout of the re-synchronization block

5.2.2 CKT4: autonomous pump

A digital pattern generator is implemented to feed the Riemann Pump with 8 bit depth periodic streams (Fig. 5.8). This generator receives the wanted bits from an external generator operating at low frequency, through a FIFO. The received data are then loaded in parallel into latches. The 8 stored bits are sequentially outputted to the Riemann Pump input switches, thanks to a pulse generator (Fig. 5.9).

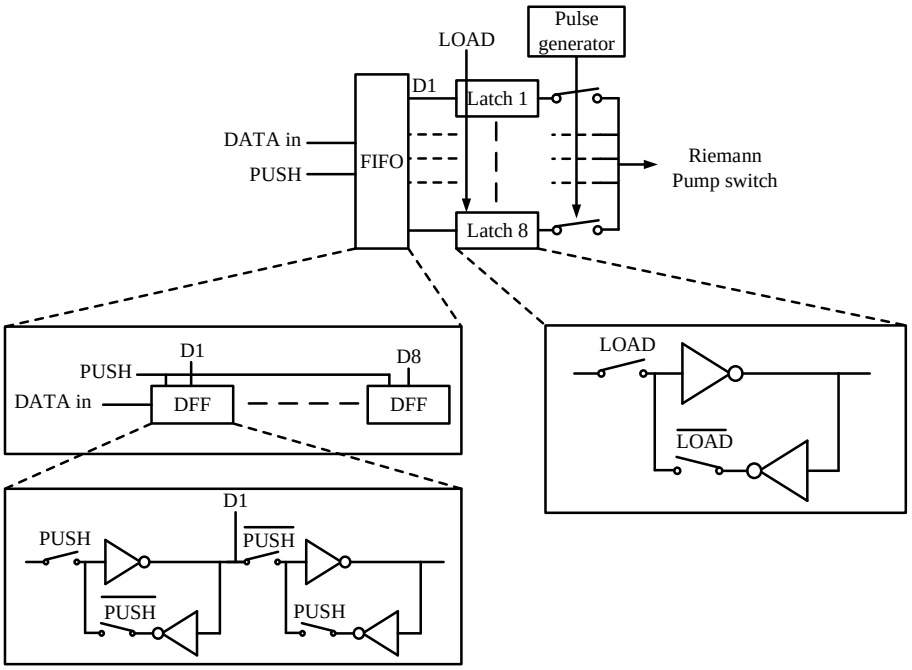

Figure 5.8: Block diagram of the pattern generator

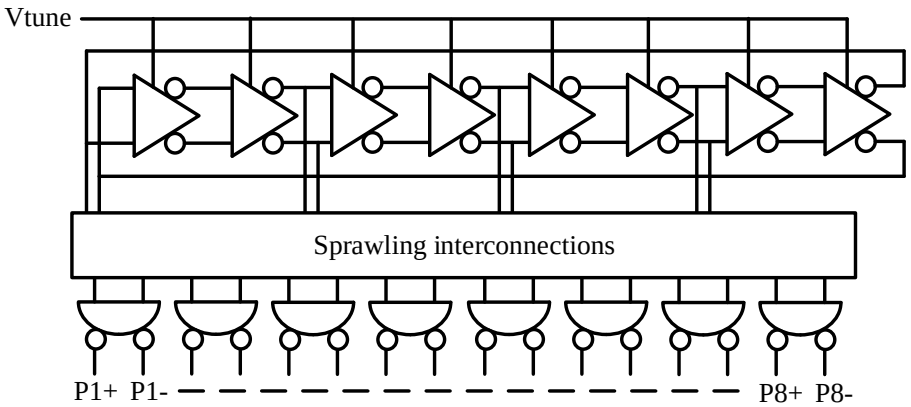

Figure 5.9: Block diagram of the pulse generator

The generation of pulses is illustrated by a timing diagram resulting from a PLS simulation (Fig. 5.10). 8 pulses are generated sequentially to address the 8 stored bits.

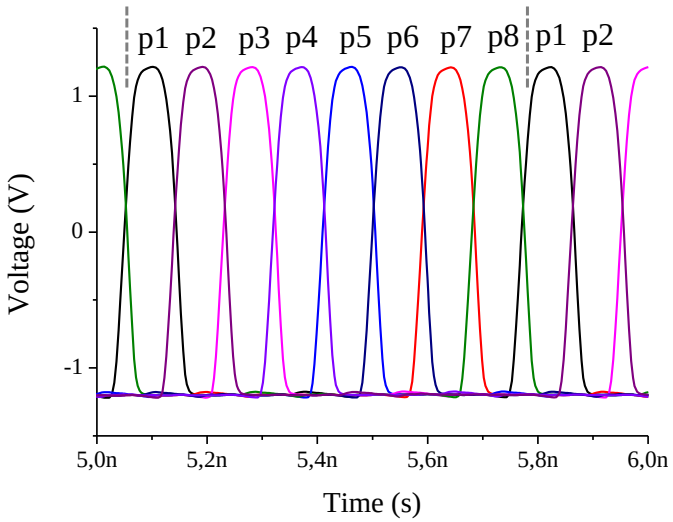

Figure 5.10: Generation of the pulses - PLS

The operation of the whole digital pattern generator is depicted in Fig. 5.11. The first step consists in pushing the data into the FIFO thanks to a serial interface. Once the FIFO is full, all the bits are loaded into the latches. The loaded pattern is then outputted endlessly, at a frequency fixed by the pulse generator. When the bit streams are generated, the output voltage of the Riemann Pump is representative of the reconstruction of the corresponding analog signal.

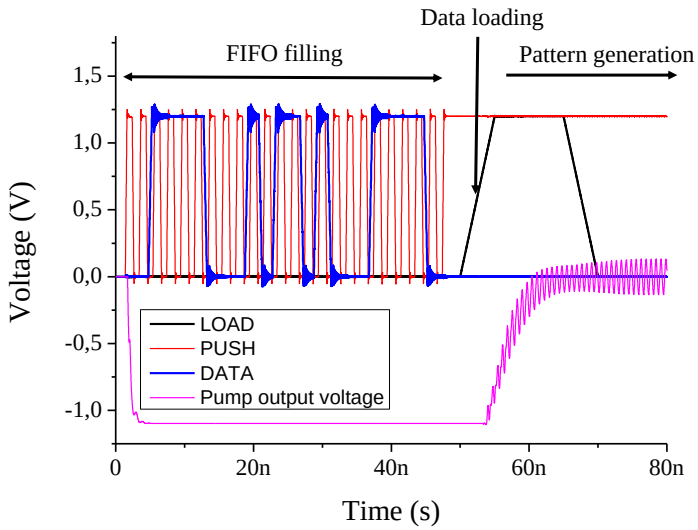

Figure 5.11: Loading of the pattern data

Fig. 5.12 represents the layout of the overall pattern generator.

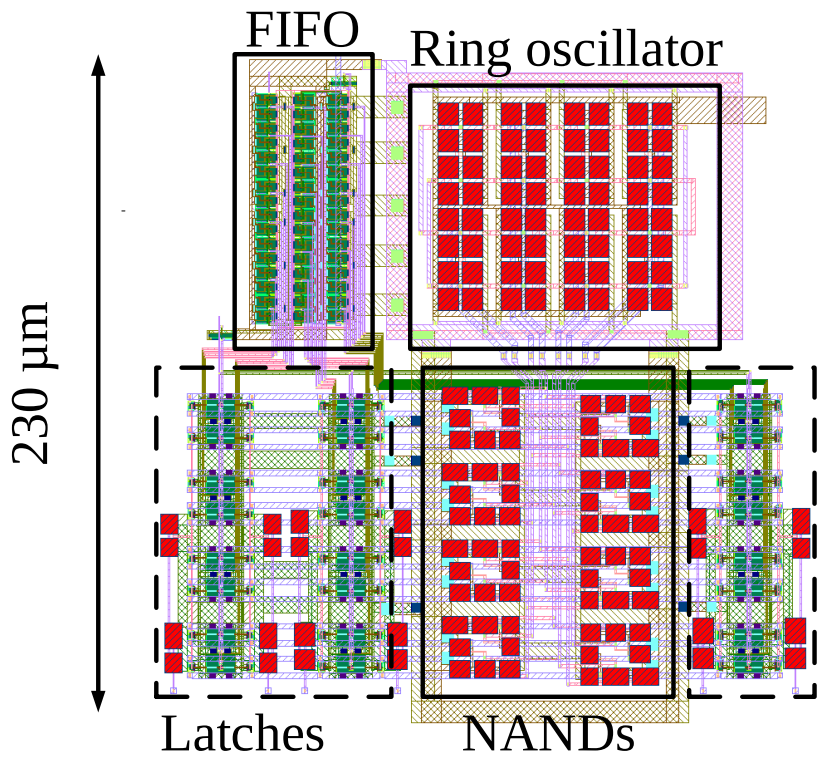

Figure 5.12: Layout of the pattern generator

Design of an analog waveform generator dedicated to software radio transmission.

Abstract: The increasing density of wireless devices and the associated communication flows sharing the same air interface will require a smart and agile use of frequency resources. This thesis proposes a flexible, low cost and low power disruptive transmitter architecture. It uses a differentiating coding scheme which leverages a mathematical and technological reduction of the energy cost of information conversion. The design of a DAC suited to this architecture is developed and its performances are assessed toward RF signal generation. The measurements of a demonstrator designed in 65 nm CMOS technology bring a proof of concept.

Index terms: Digital to analog converter, Waveform generator, Software radio.

Contribution à l'étude et à la réalisation d'un générateur de signaux radiofréquences analogiques pour la radio logicielle intégrale

Résumé: Une utilisation intelligente de l'espace Hertzien sera nécessaire pour permettre au nombre croissant d'objets sans-fil connectés de communiquer dans le même espace de propagation. Ces travaux de thèse proposent une architecture d'émetteur radiofréquence flexible, faible coût et faible consommation, en rupture avec les techniques conventionnelles. Cet émetteur est fondé sur un encodage de la dérivée du signal à générer, ce qui permet de réduire le coût énergétique de la conversion de l'information. Un convertisseur numérique analogique compatible avec cette architecture est présenté et ses performances sont évaluées dans le cadre de la génération de signaux radiofréquence. Les résultats de mesures obtenus avec un prototype réalisé en technologie CMOS 65 nm apporte la preuve du concept.

Mots clés: Convertisseur numérique-analogique, Générateur de signaux, Radio logicielle intégrale.

Résumé étendu

L'espace Hertzien qui relie les terminaux connectés au réseau filaire est régulé par de nombreux standards. La prochaine génération de communications sans-fil requiert une utilisation intelligente et flexible des ressources spectrales afin d'augmenter la capacité de trafic de données du réseau. Cette tendance impose des contraintes sévères sur la conception des émetteurs/récepteurs mobiles. Ils doivent supporter des débits de données élevés, des larges gammes de fréquences et des schémas de modulations variés, tout en arborant une consommation réduite en accord avec les faibles quantités d'énergie stockées dans les terminaux mobiles.

Le **chapitre 1** expose le paradigme des communications radio et l'évolution des architectures d'émetteurs/récepteurs. Il souligne la tendance à améliorer la flexibilité des émetteurs sans-fil par le biais d'une utilisation accrue de l'électronique numérique, selon le principe de la radio logicielle. Le gain de flexibilité important est modéré par la consommation énergétique trop élevée, en particulier en ce qui concerne l'opération de conversion numérique/analogique. Les schémas classiques de conversion de données sont étudiés et leurs limites sont abordées.

Le **chapitre 2** propose l'étude théorique de schémas de conversion en rupture avec les méthodes traditionnelles, ainsi que celle d'une topologie de convertisseur numérique/analogique adapté. Ces techniques de conversion sont fondées sur le principe de la modulation Delta, mise en jeu dans certains systèmes de compression des données. Le processus de conversion traite les variations temporelles du signal, grâce à un codage numérique différentiateur qui permet d'améliorer l'efficacité de conversion de manière significative. La reconstruction du signal est réalisée grâce à un convertisseur numérique/analogique intégrateur sur mesure, que l'on appelle la Pompe de Riemann. Les performances du système proposé sont évaluées vis-à-vis de la génération de signaux radiofréquences.

Le **chapitre 3** décrit la conception de la Pompe de Riemann dans deux technologies intégrées. La première est une technologie GaN dédiée aux applications militaires. La seconde est une technologie silicium 65 nm adaptée au marché de l'électronique grand public. La conception de deux circuits est détaillée, et des simulations post-routage sont présentées. Elles valident la compatibilité de l'architecture proposée avec les technologies ciblées, et permettent d'en estimer les performances.

Le **chapitre 4** présente les mesures menées sur le démonstrateur réalisé en technologie silicium 65 nm. Les résultats réalisés apportent la preuve du concept. Une amélioration des capacités du banc de test est requise pour aller plus loin dans la caractérisation des prototypes. Des pistes sont proposées pour développer un émetteur complet autour de la Pompe de Riemann.

Résumé du chapitre 1

La convergence technologique, les habitudes des utilisateurs et la densité des appareils connectés impliquent une augmentation massive du volume de données sans-fil. La structure du réseau doit changer significativement pour assumer cet afflux de données. Les émetteurs/récepteurs de terminaux mobiles doivent satisfaire 3 contraintes majeures afin d'assurer leur compatibilité avec un réseau qui sera hétérogène :

- **Bas coût** : une solution peu onéreuse est nécessaire pour s'adresser à un marché de masse. La technologie la plus approprié est le CMOS
- **Faible consommation** : les systèmes de communications doivent assurer un fonctionnement à faible puissance, pour sauvegarder la durée de vie de la batterie
- **Bande passant large** : les débits de données mis en jeu seront très important, il faut donc assurer une large bande passante

Les émetteurs radio logicielle fondés sur la conversion directe de larges bandes de fréquence semblent être de bons candidats pour fournir une flexibilité absolue. En revanche, la consommation importante des convertisseurs radiofréquences les rend difficilement intégrables dans les appareils mobiles. La réalisation d'un émetteur qui serait compatible avec les contraintes de consommation nécessite une approche de conversion en rupture avec les architectures conventionnelles, afin d'améliorer l'efficacité de conversion et de passer outre cette pierre d'achoppement majeure. Nous proposons d'explorer une approche innovante de conversion numérique/analogique, qui concerne à la fois le schéma de codage employé et la topologie sur mesure du convertisseur qui lui est associé.

Résumé du chapitre 2

Une conversion numérique/analogique efficace fondée sur des codages différentiateurs est exposée. Ils bénéficient du codage de la dérivée, éventuellement associé à une mise en forme du bruit de quantification, pour améliorer leurs performances de conversion. Cela mène à un compromis entre la complexité du système et les performances de conversion qui est meilleur que celui des schémas de conversion classiques implémentés dans les convertisseurs numérique/analogique rencontrés dans l'état de l'art. La théorie sous-jacente a été développée et validée grâce à des simulations du système. Cela permet de régler le jeu de paramètres du système, à savoir le nombre de bits N utilisés dans la conversion, ainsi que le facteur de sur-échantillonnage, en fonction de l'application visée.

Le système a été évalué pour les contraintes rudes attendues pour le standard 5G. La génération de 10 porteuses agrégées et intrinsèquement synchronisées, avec une dynamique de 60 dB, peut être effectuée avec les caractéristiques suivantes :

- **Schéma de conversion** : conversion de Riemann avec mise en forme du bruit
- **Nombre de bits N** : 6
- **Fréquence de conversion** : f_s=40 GHz

Ces caractéristiques peuvent être compatibles avec les dernières technologies CMOS. Cependant, notre objectif est d'apporter une preuve du concept. Le chapitre 3 expose le flot de conception des démonstrateurs de la Pompe de Riemann dans plusieurs technologies. Il présente les schémas électriques et les plans de routage, ainsi que les résultats de simulation associés.

Résumé du chapitre 3

La Pompe de Riemann a été conçue dans deux technologies complètement différentes, pour des applications différentes. Des applications RADAR sont envisagées avec le circuit an GaN, avec de fortes puissances et une grande robustesse. Le circuit en CMOS cible le marché des communications sans-fil. Grâce à sa faible consommation, sa grande bande passante et sa petite taille, il est en adéquation avec les contraintes de la prochaine génération des terminaux mobiles. De nombreuses techniques ont été utilisées lors de la conception des deux puces, relevant à la fois du domaine analogique et du domaine numérique. Les simulations post-routage mettent en évidence un impact réduit de l'implémentation physique, en ce sens que les performances ne sont pas dégradées de manière significative par rapport à la théorie. Cela confirme l'adéquation entre l'architecture proposée et son implémentation électrique. Cela suggère également que des versions plus complexes de la Pompe de Riemann peuvent être conçues dans les technologies utilisées, avec un nombre de bits plus élevé afin d'améliorer les performances et de pouvoir s'adresser aux standards de nouvelle génération. Parmi les deux puces développées, seule la version en CMOS a été fondue. Le chapitre 4 présente les résultats de mesure obtenus avec la puce baptisée PAULINA.

Résumé du chapitre 4

La caractérisation de la puce PAULINA valide le principe d'un émetteur radiofréquence fondé sur le principe de la Pompe de Riemann. Le circuit caractérisé peut être vu comme un CNA radiofréquence. Le facteur de mérite (FdM) choisi pour évaluer ce convertisseur est le coût énergétique de la conversion (en picojoule par pas de conversion).

$$FdM = \frac{P}{2^{Rés}.BP} \tag{5.12}$$

Avec: **P** la puissance consommée, **Rés** la résolution en nombre de bits effectifs, et **BP** la bande passante du convertisseur

La Pompe de Riemann, associée à un schéma de codage avec mise en forme du bruit de quantification, permet d'obtenir une efficacité de conversion de 5.1 fJ par pas de conversion. De plus, la surface active du circuit est restreinte, avec 0.2 mm^2 pour le prototype réalisé. Cela met en lumière le potentiel de la technologie présentée, dans le cadre du développement d'un émetteur radio logicielle bas coût et basse consommation pour les prochaines générations de communications sans-fil.

Conclusion

La conversion entre les données numériques et les signaux analogiques mis en œuvre pour les émissions radio est un point clé du développement des technologies sans-fil. De nombreuses recherches traitent des convertisseurs de nouvelle génération. Ils emploient principalement des schémas de conversion classiques, implémentés dans des technologies silicium récentes. Cette approche n'est pas à même de répondre aux attentes exigeantes des standards à venir. Ce travail de thèse présente une architecture originale d'émetteur, qui opère la conversion via la dérivée du signal avant une intégration dans le domaine analogique réalisée grâce à un CNA que l'on baptise la Pompe de Riemann. Le principe de conversion sous-jacent tira avantage du sur-échantillonnage pour améliorer le rapport signal sur bruit. Un doublement de la fréquence d'échantillonnage permet d'améliorer le rapport signal sur bruit de 9 dB, et de 6 dB supplémentaires grâce à l'insertion d'une boucle de mise en forme du bruit de quantification du premier ordre. La conception de la Pompe de Riemann en technologie silicium 65 nm souligne sa propension à travailler à haute fréquence, avec une commande numérique pouvant aller jusqu'à 25 Gbps, et sa consommation inférieure au milliwatt. La résolution qui en découle vaut 5,4 bits effectifs, pour une bande passante supérieure à 3 GHz. Le coût énergétique de conversion du circuit développé se classe dans les meilleurs de l'état de l'art des convertisseurs radiofréquences, avec une efficacité de 5 fJ par pas de conversion. Un démonstrateur de la Pompe de Riemann a été fabriqué puis caractérisé. Les résultats obtenus apportent une preuve du concept. La co-intégration avec un bloc de calcul numérique et un amplificateur en sortie est également démontrée. Les prochaines générations de standards de communication sans-fil seront censées regrouper des spécifications techniques irréalistes, avec une amélioration d'un facteur 10 dans toutes les performances clés (dont le débit de donnée et la consommation). Cela va nécessiter de véritables percées dans la course à la réduction du coût de l'information en termes d'énergie. L'implémentation d'architectures classiques dans les technologies les plus avancées ne sera pas suffisante pour atteindre de tels objectifs. L'approche développée dans thèse s'inscrit dans la tendance du « Design by Mathematics ». Elle propose de développer des circuits et systèmes originaux grâce à l'adéquation entre des principes mathématiques et leur implémentation électronique.