# Silicon nanowires synthesized by VLS growth mode for gas sensing applications

Liang Ni

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# Liang Ni

préparée à l'IETR UMR CNRS 6164
Institut d'Electronique et de Télécommunications de Rennes
UFR Informatique - Electronique


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devant le jury composé de :

**Antoine GOULLET**
Professeur à l'université de Nantes / rapporteur

**Gael GAUTIER**
Maître de conférences HDR à l'université de Tours / *rapporteur*

**Jean-Marc ROUTOURE**
Professeur à l'université de Caen / Examinateur

**Vincent THOMY**
Maître de conférences HDR à l'université de Lille 1 / *examinateur*

**Laurent PICHON**
Professeur à l'université de Rennes 1 / *directeur de thèse*

**Anne-Claire SALAUN**
Maître de conférences HDR à l'université de Rennes 1 / co-directrice de thèse

**Régis ROGEL**
Membre invité

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# General introduction

In recent decades, the unceasing reduction of characteristic dimensions for integrated circuits has enabled the microelectronics industry to realize a great technological development and real economic success, which gradually transformed our lifestyles and productions to the "all-electronic".

The microelectronics industry and its numerous applications (information industry, mobile phones, etc.) are based on the basic unit: transistor, where the continuous miniaturization in recent decades has exponentially increased integration density following law's Moore, and undoubtedly improved performance of productions. Indeed, this has significantly increased performances in terms of speed and complexity of realized functions. Thus, the micro-devices embedded in consumer electronics have the growing potential with remarkable performances consistent with the "microsources" of energy (battery) and an ability to communicate with various peripherals and accessories (image, sound, video) that have literally invaded our daily lives. In addition, information technology and communication are not the only fields of applications of integrated circuits. In fact, for the last fifteen years, we have been witnessing many technological advances in biotechnology, photonics, solar energy, automotive, etc…

Currently, the microelectronics industry comes to a double limit, technological and financial. For technological limit, on the one hand, the miniaturization leads the devices to be sensitive to phenomena which degrade the performances (short channel effect, decreased compared On/Off state current... for MOS technologies). On the other hand, the continuing miniaturization requires the development of used manufacturing methods, particularly in terms of lithography, as evidenced by developments in deep UV optical lithography, immersion lithography or e-beam lithography. These extremely expensive techniques oppose the low-cost principle for fabrication of integrated circuits.

To overcome these technological barriers, scientific researches in the field of integrated electronics tend more and more to nanoscience. This science has been recently studied and developed in depth on the physical and chemical properties of materials at very small scale (nanometer). Indeed, the nanoscience permits to reveal and highlight several potentials in terms of physical and electronic phenomena to exploit materials, especially semiconductors. They have shown a remarkable ability in terms of compatibility with the integration of electronic circuits as well as in terms of performances achieved at nanoscale.

Nowadays, innovation of future integrated circuits is based on nanotechnology to produce nano-structures using two approaches: bottom-up and top-down (see Chapter I).

Many elaborated techniques in nanotechnology permit to perform various forms of structures such as nanotubes, nanoparticles and especially nanowires, which open the way for the manufacture of electronic devices with enhanced and/or innovative electronic properties. However, most of the associated technologies are still at an experimental stage. They are difficult to be implemented (due to expensive equipment) and they are not reliable for realizing circuits in mass production. Nevertheless, the specific electronic properties of nano-objects based on semiconductors used as active elements in electronic devices, suggest their great potential for new applications in many fields (chemistry, biology, mechanics ....).

In particular, many research activities focus on the synthesis of silicon nanowires and their applications in innovative micro-nano-systems. Indeed, the synthesis of silicon nanowires is associated with both i) the miniaturization of components in order to improve their electronic performances, and ii) the development of nano- and micro-devices with new features based on elementary components (resistors, transistors ...). Therefore, since 2007 the "Département Microélectronique et Microcapteurs of the Institut d'Electronique et de Télécommunications de Rennes" (DM2-IETR) launched research themes about synthesis of silicon nanowires (SiNWs) and components based on SiNWs for sensors applications. Many advantages of silicon nanowires are considered: i) compatibility with silicon manufacturing, ii) a high surface/volume ratio (useful for applications such as chemical sensors), iii) a giant piezoresistivity (for NEMS Nano-Electro-Mechanical Systems) and iv) the possibility of surface functionalization of the nanowires (intended applications: bio-chemical sensors).

This research work is to fabricate microelectronic devices (resistors and transistors) from silicon nanowires synthesized by VLS (Vapor-Liquid-Solid) method. The growth of these nanowires is carried out by LPCVD (Low Pressure Chemical Vapor Deposition) technique using a metal catalyst (gold). The objective of this work is to highlight the potential applications of these devices as a chemical sensor with high sensitivity.

The thesis will be divided into four chapters. Some additional information will be detailed in the annex.

The first chapter presents state-of-the-art of silicon nanowires synthesis. Two main synthesis methods, bottom-up and top-down are presented. The key VLS mechanism of

synthesizing our NWs is explained in detail. The potential applications of the silicon nanowires in electronic devices are also introduced.

In the second chapter, we have presented state-of-the-art of silicon nanowires based sensors which have various applications as mechanical, chemical and biological sensors. Progresses are presented in various application areas such as mechanical, chemical and biological sensors based on silicon nanowires. Indeed, due to their large surface to volume ratio and their diameters of a comparable size to those of chemical and biological species to detect, SiNWs are good candidates as sensitive units for nano-sensors in areas of biology and chemistry.

In the third chapter, the main materials and related techniques used in the manufacturing process of SiNWs based structures are presented. A brief description of the methods for obtaining each material used is given. The standard procedures of fabrication for both inter-digital comb-shaped structure and the V-shaped groove structure are presented in detail.

Finally, in the last chapter, we study the electrical properties of the VLS SiNWs by means of the inter-digital comb-shaped resistor. Temperature dependence and *in-situ* doping control are studied. The silicon nanowires based resistors are also electrically characterized as chemical sensors under exposure to ammonia and smoke due to ambient charged species detection. Both qualitative (smoke) and quantitative ($NH_3$) measurements have been performed and their performances are discussed and analyzed in detail.

# Chapter I

# State-of-the-art of silicon nanowires synthesis

# I Introduction

One of today's major trends in the semiconductor technology domain is a way of miniaturization. Since the beginning of the microelectronics era, the smallest line width or the minimum feature length of an integrated circuit (IC) has been reduced at a rate of 13% per year [1]. But this trend is not formed by sacrifice of high performance of an IC. By contraries, device miniaturization results in the development of nano-scale devices with the same objective to reduce unit cost and power consumption per circuit function and enhance the performance. Obviously, the integration density has also been improved enormously according to the miniaturization tendency. In the process of miniaturization, semiconductor nanowires have played a very important role and opened up substantial opportunities for novel nano-scale photonic and electronic devices through well-controlled growth and organization of the nanowires.

Since the first 1-D carbon nanotubes (CNTs) were discovered by Iijima in 1991[2], researchers have showed great interest in the synthesis and characterization of 1-D nano-scale structures, especially of nanowires. The key advantage of semiconductor nanowires over carbon nanotubes is the possibility of controlling the conductivity and carrier type by adding impurities. Thus the transistors could be fabricated. A semiconductor nanowire is a one-dimensional (1-D) solid rod with a diameter less than 100 nm which can be fabricated from a variety of semiconductor materials (silicon, germanium, oxides…). Among these semiconductor materials, silicon nanowires (SiNWs) have been widely used because of their relatively low price, easy and compatible semiconductor fabrication methods, and convenient integration for devices in the existing silicon electronic industry. Furthermore, silicon nanowire has many interesting properties that we cannot find in bulk silicon materials:

- Giant piezo-resistivity,
- Thermal electricity,
- High surface area to volume ratio,
- Field emission,
- Higher integration density (smaller feature size),
- Possibility of surface functionalization.

These properties allow realizing electronic devices for new applications (optoelectronics, gas sensors, bio-chemical sensors ...).

The silicon nanowires can be synthesized by many different techniques, most of which can be classified into two categories: 1) “top-down” method which realizes nanowires from big dimension to small and 2) “bottom-up” method which builds nanowires from atoms or molecules via self-organization. The detailed principles of these two strategies will be explained in the following sections.

A vast of exciting and potential applications are expecting on silicon nanowires. They can be used as active parts of components because of their semiconductor properties and integrated into a lot of domains, such as electronics, optoelectronics, sensors, mechanics…

In this first chapter, the different synthesis methods, especially Vapor-Liquid-Solid (VLS) method, and the various potential applications of silicon nanowires will be introduced in the field of nanotechnology.

# II Synthesis methods of nanowires

Although the nanowires have so many attractive advantages and potential applications, they have not been standardized and engaged in mass production in modern semiconductor industry yet. One of the important reasons is that the nanowires have too many various methods of synthesis. Not even one standard method of synthesis has been widely accepted. As previously mentioned, the main growth methods of nanowires can be divided into two strategies: the top-down approach and the bottom-up approach. These two approaches have been widely used to realize nano-structural object, however the two ways of realization are totally different. Both of them have their individual advantages and drawbacks.

## II.1 Top-down approaches

The principle idea of the “top-down” method is to pattern a macroscopic object into a nano-scale object. The lithography and etching techniques permit creating the micro or nano patterns in order to realize the nanowires. However, a very important factor, the wavelength used by lithography limits the scale-down trend. Most of the optical lithography methods can only achieve at 50-100 nm. As a result, a lot of other techniques are used to fabricate the

nanowires with smaller dimension, for example, the nano-imprint lithography, the electronic lithography, the sidewall spacer technique …

## II.1.1 Nano-imprint lithography method

Nano-imprint lithography (NIL) is a method of fabricating nano-scale objects which creates patterns using a mold by mechanical deformation of imprint resist. The whole processes can be considered as affixing a stamp on paper. When the mold is pressed on the substrate covered with resist, the covered rein will be squeezed into the caves of the mold. Then a reverse pattern will be transferred to the substrate. The most commonly used imprint resist is poly-dimethyl siloxane (PDMS) or poly-methyl methacrylate (PMMA). The mold patterns are fabricated by conventional techniques electron-beam lithography (EBL) and reactive ion etching (RIE) which determines the final scale of the products. The reusable property of the mold permits a mass production at low-cost that makes the nano-imprint lithography be a popular technique in semiconductor industry.

The nano-imprint lithography method consists of two main steps (figure 1): imprinting the patterns from the mold to the substrate covered by resist, and a RIE process after the proper release between the resist and the mold. The RIE allows the removal of the unwanted resist to optimize the transfer of the pattern on the substrate.

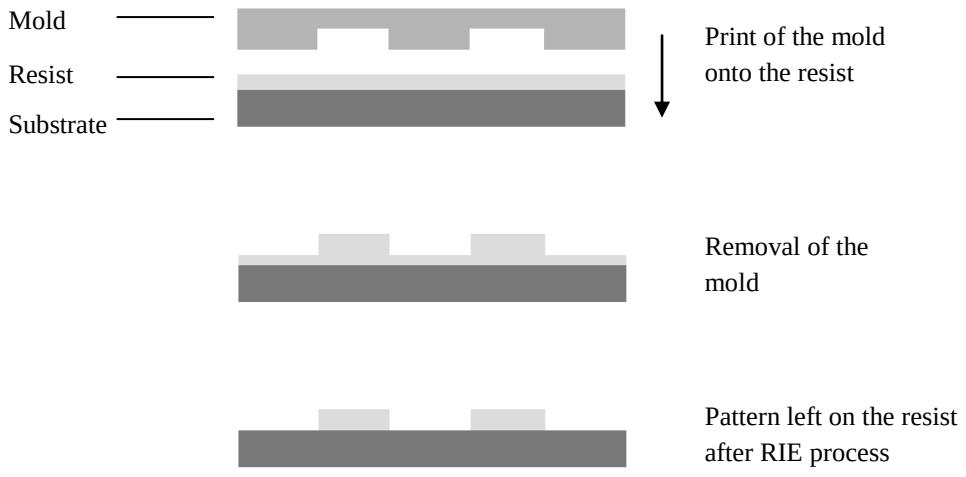


Figure 1: A schematic of NIL technique.

Many different types of nano-imprint lithographies have been proposed in which the thermoplastic nano-imprint lithography (T-NIL) and photo nano-imprint lithography (P-NIL) are the most important. Thermoplastic nano-imprint lithography is the most widely studied method in recent years. It is the earliest nano-imprint lithography developed by S.Y. Chou in 1996 [3]. The special resist PMMA is pressed together with the mold under a certain pressure ($13\times10^6$ Pa) and meanwhile the temperature (200 °C) is heated up [3]. The pattern on the mold can be pressed into the softened resist film until they reach a certain high temperature. When the temperature cools down, the mold is separated with the resist and the pattern of the mold is left onto the underneath material (figure 2-a). The photo nano-imprint lithography works almost under the same principle. The difference between them is that it uses a liquid resist which is cured in the UV light. After an exposure of UV light, the resist becomes solid. Then the mold is released from the resist (figure 2-b).

The imprint process is commonly performed by the following 3 steps:

- Compression between the mold and the resist,

- cure of the resist (T-NIL cured by heating and P-NIL cured by UV light),

- Removal of the mold.

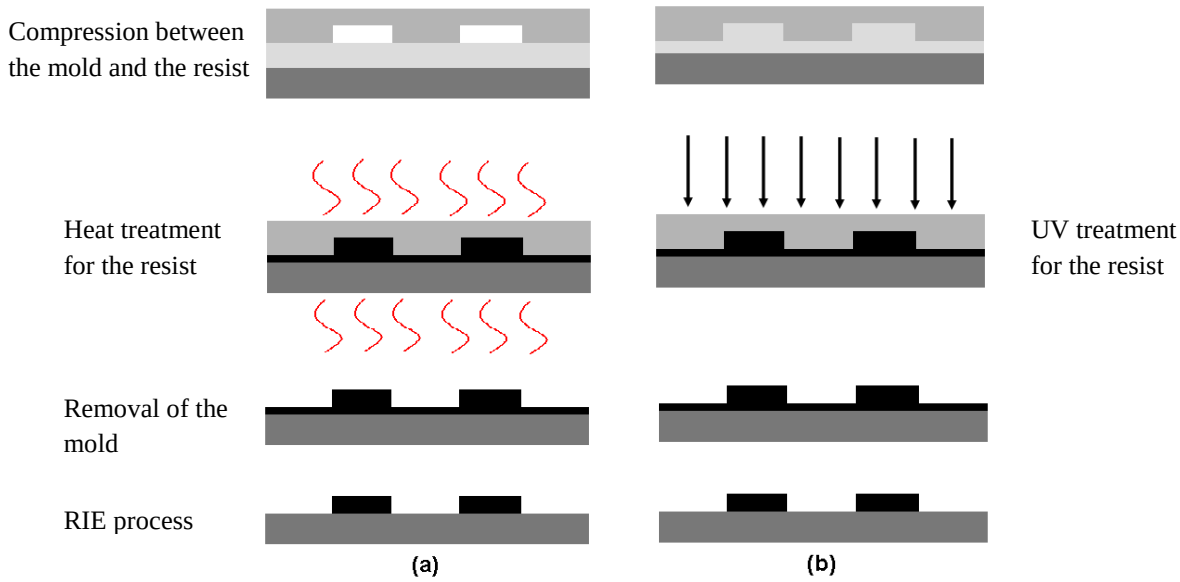


Figure 2: A schematic of (a) T-NIL and (b) P-NIL

The figure 3 shows an example that uses the T-NIL technique to realize silicon nanowires on SOI substrate [4]. A T-NIL is performed to obtain wide thin resist lines (100 nm) on the surface of a 100 nm thick monocrystalline silicon layer. These are subsequently used as a mask for plasma etching under $Cl_2$/HBr to get silicon nanowires.

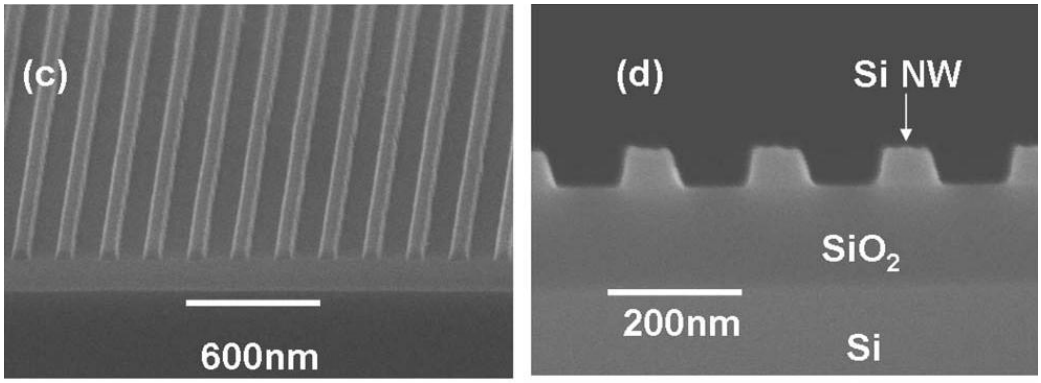


Figure 3: Cross sectional SEM images of silicon nanowires realized by T-NIL [4].

## II.1.2 Electron Beam Lithography method

Electron beam lithography (EBL) refers to a lithographic process that uses a focused beam of electrons to precisely define the resist patterns. Thanks to its short wavelength (≤ 1 µm) exhibited by the electrons in the energy range, EBL offers higher patterning resolution, which can reach nano-scale more easily, than optical lithography whose resolution is limited by diffraction. But the "serial" manner in producing the resist pattern makes the EBL systems less efficient compared with optical systems, which strongly restricts the mass-production in semiconductor industry. Another disadvantage of this method is that EBL systems are generally expensive and highly complex which requires substantial maintenance.

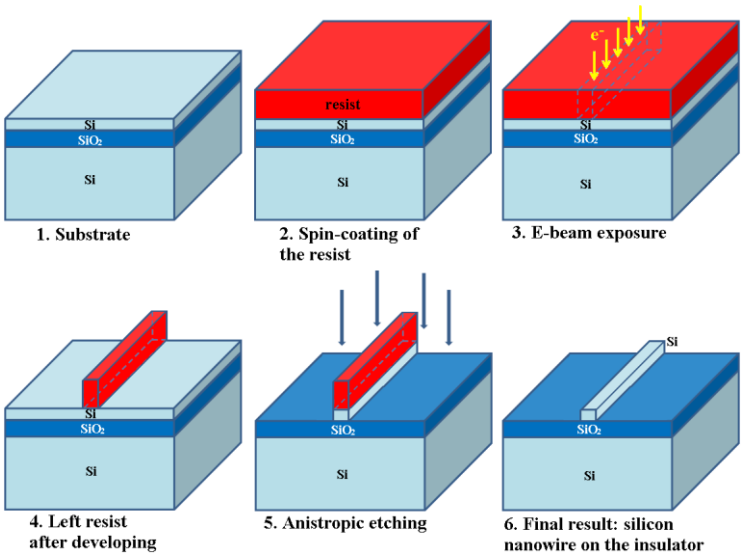


Figure 4: Schematic of silicon nanowires patterning by EBL method.

In practice, the EBL is used to create patterns on a resist material which is sensible to the electrons. The figure 4 shows the technological steps to realize silicon nanowires. An ultra-dense array of vertical silicon nanowires realized via EBL method is illustrated in figure 5 from reference [5].

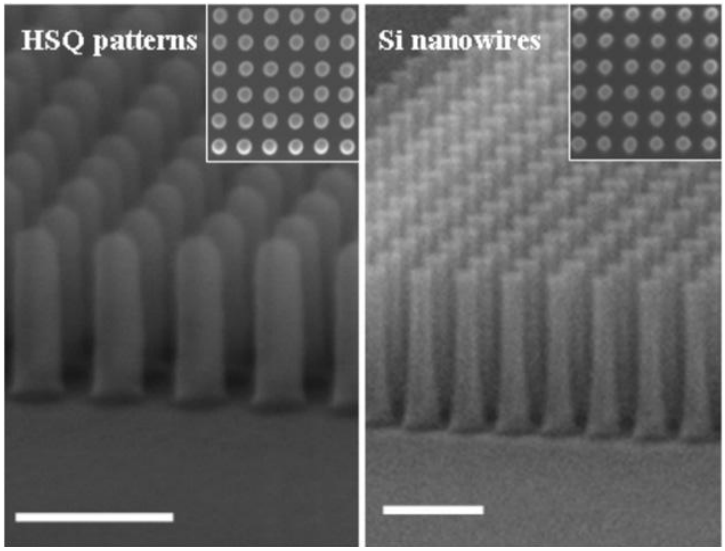


Figure 5: SEM image in tilted view of (left) dense hydrogen silsesquioxane (HSQ) resist patterns (diameter= 27 nm, height = 120 nm) and (right) vertical SiNW arrays after HSQ mask transfer by RIE (NW diameter = 19 nm; array density = 4 $\times 10^{10}$ NWs/cm$^2$). In inset, the top view SEM picture. Scale bar is 100 nm [5].

## II.1.3 Spacer optical lithography method

Although the use of advanced lithography tools like EBL has so many advantages such as high pattern ability, good reproducibility and control of the nanowires (position and diameter), its high-cost disadvantage restricts the mass-production in semiconductor industry. Therefore, a simple and low-cost method, employing sidewall spacer method (figure 6) catches technologists' interests. The sidewall spacer method enables fabricating nano-scale objects via using the classical techniques (optical lithography, chemical vapor deposition (CVD) and Reactive Ion Etching (RIE)). Previously, this sidewall spacer formation technique has been proposed to define the nano-scale hardmask itself. H.-C. Lin et al. [6] proposed this technique to directly define the nano-scale silicon lines that serve as the device channels. After a nano-scale thin film poly-silicon deposition on a dielectric film ($SiO_2$, $Si_3N_4$) previously patterned with vertical sidewalls, a anisotropic dry etching is carried out (see figure 6). Taking advantages of the anisotropic etching property and the height difference at the spacer sidewall, the etching process results in a line structural residue. This line residue is just the nanowire channel serving for TFTs (figure 7). Feasibility of such poly-silicon nanowires as well as their integration into electronics devices was demonstrated by the Groupe Microélectronique [7, 8].

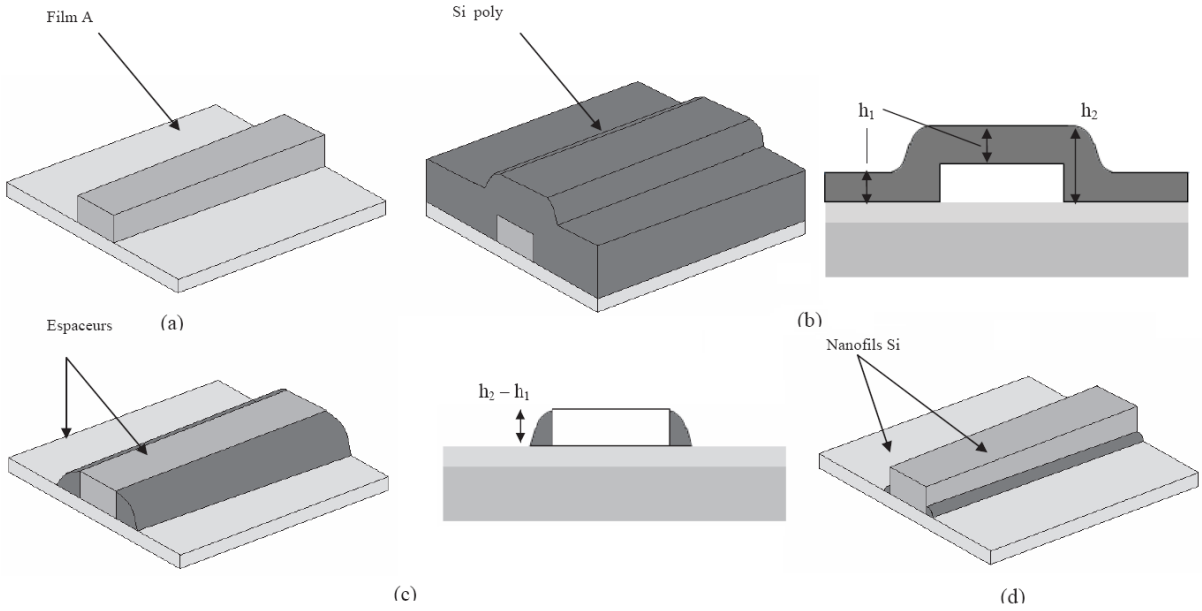


Figure 6: (a)-(d) Schematic of silicon nanowires patterning by sidewall spacer method [7].

This technique provides a low cost method to fabricate a large quantity of parallel nanowires on a large area substrate, thus it enables the integration in mass manufacturing.

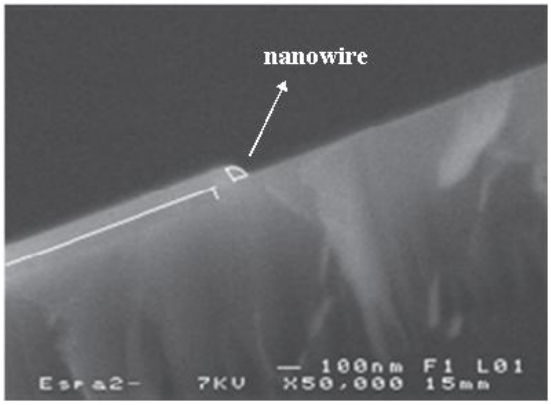


Figure 7: SEM cross-sectional view of silicon nanowire with 50 nm curvature radius [7].

## II.2 Bottom-up approaches

"Bottom-up" approach is an inverse synthesis method compared with the "top-down" approach. The "bottom-up" seeks to have smaller components built up into more complex objects via self-assembly process. The concept of self-assembly is to create the nano-scale objects by self-organizing an enormous number of single atom or molecule. Today, the main self-assembly methods to fabricate silicon nanowires are: Solid-Liquid-Solid (SLS) method, porous template method and Vapor-Liquid-Solid (VLS) method.

### II.2.1 Solid-Liquid-Solid growth method

One useful mode of SiNWs synthesis, using metal catalysts is the Solid-Liquid-Solid (SLS) mechanism [9]. In this case, the SLS mechanism, the metal-rich catalyst remains on the surface of the silicon substrates during the entire process and the substrate itself serves as a silicon source without any additional source from outside.

Recently, an IPSLS (In-Plane Solid-Liquid-Solid) growth mode was proposed and developed by L. Yu and P. Roca [10, 11] for obtaining an in-plane growth of SiNWs. The SiNWs synthesis are realized by the catalytic indium droplets embedded into hydrogenated

amorphous silicon (a-Si:H) matrix, which consumes and transfers a-Si:H into crystalline SiNW during the annealing process. Two different growth modes for the IPSLS SiNWs were found: the GG (grounded-growth) in which the produced SiNWs are attached to the substrate surface and the SG (suspended-growth) in which the produced SiNWs are suspended and carried by the catalyst droplet during its movement (figure 8). The authors have found that the diameter and the growth rate of SiNWs are proportional to the diameter of the catalyst droplet. They have also demonstrated three different methods to guide the growth of SiNWs in an in-plane surface.

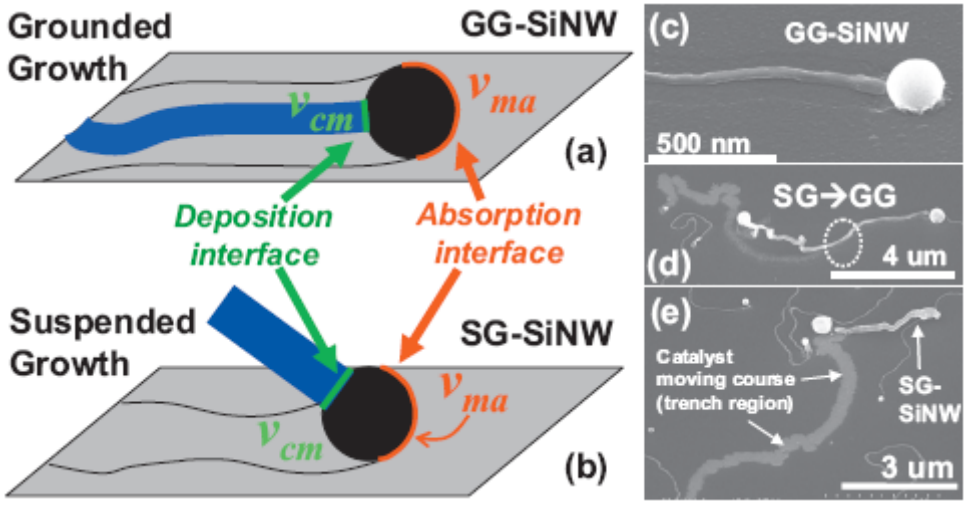


Figure 8: Schematic illustrations of the two different growth modes for the growth of IPSLS SiNWs: (a) the GG mode and (b) the SG mode. (c) and (e) present the corresponding SEM pictures of the GG-SiNWs and SG-SiNWs, respectively. (d) A transient case, from the initial SG mode to the final GG mode during the growth [11].

## II.2.2 Porous template method

The objective of this method is to synthesize oriented nanowires with uniform diameter by using template (for example, the anodic aluminum oxide (AAO) or porous anodic alumina (PAA)) [12-14].

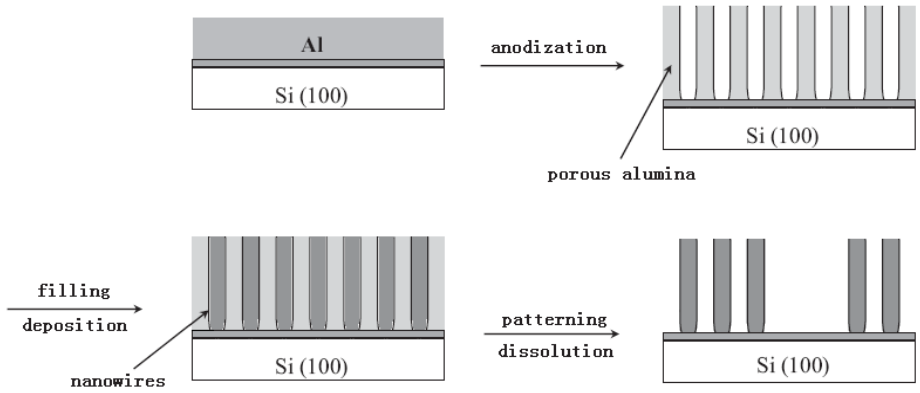


Figure 9: Schematic representation of the PAA films fabrication and nanowire arrays on silicon wafer.

Figure 9 is a schematic representation of this method. The main procedure is divided into three steps. The first step is to fabricate an ordered porous anodic alumina film on the substrate. The diameter and the length of the nanopores can be controlled from a few nanometers to several hundred nanometers and several micrometers, respectively. The second step is to fill the pores of the template with certain materials which could be silicon or metal materials. The filling step can be achieved through different ways: electrochemical, high-pressure injection or evaporation. In addition, the VLS growth method is also commonly used to fill the porous network (figure 10). The last step is to remove the template via selective chemical etching. After the separation or dissolution of the template, a high density array of nanowires would be obtained.

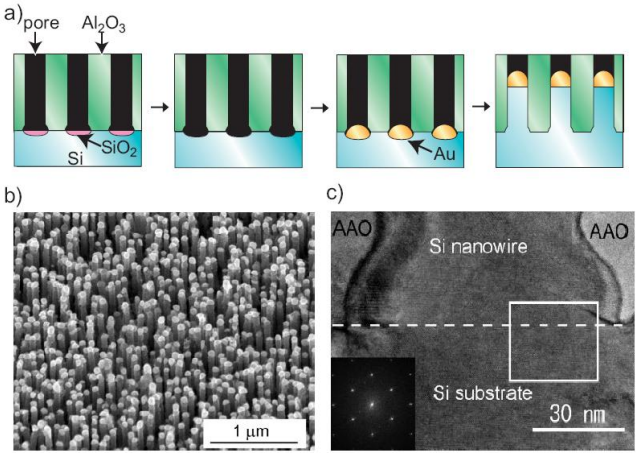


Figure 10: a) Schematic cross-sectional drawing of the growth of Si nanowires in AAO nanopores using VLS method. b) Top-view SEM image of Si nanowires after selective etching of the AAO template. c) Cross-sectional TEM image of lower part of the Si nanowire in the AAO template [12].

### II.2.3 Vapor-Liquid-Solid growth method

The name Vapor-Liquid-Solid (VLS) refers to the fact that the precursor in the vapor phase passes through a liquid droplet and finally ends up as a solid. A metal catalytic film is introduced into the reactor to form liquid nano-droplets on the substrate surface. These nano-droplets can adsorb a vapor to achieve the supersaturation at the back interface of the nano-droplets inducing growth of the nanowires on the substrate surface, usually in a three-dimensional (3D) configuration.

Otherwise, this technique permits doping the nanowires via simultaneously introducing some certain doping gas (the phosphine for N-type doping and the diborane for P-type doping) with precursor gas during the growth process. The most popular technique we use today is Chemical Vapor Deposition (CVD). The involvement of doping changes the conducting property of nanowires which enables the nanowires be integrated in many devices such as FET (Field Effect Transistor), biosensors, solar cells …

The studies of feasibility and sensitivity to certain gas will be demonstrated in this thesis by fabricating an electronic resistor gas sensor based on nanowires via VLS technique using Low Pressure Chemical Vapor Deposition (LPCVD) [15, 16]. And recently we have succeeded in doping the N-type nanowires in different doping concentrations which is rarely cited in the literatures. The details about the LPCVD-VLS growth and doping method will be introduced in chapter 3.

## III VLS mechanism

The VLS mechanism was firstly proposed by Wagner and Ellis in 1964 [17, 18]. Two important phenomena were observed during the silicon wires growth process: an impurity is essential for the growth and a small droplet is present at the tip of the silicon wires. Therefore, they deduced that the role of the metal impurity including Au, Ag, Pt, Al… is to form a liquid droplet with relatively low temperature. The liquid droplet is a preferred site for deposition of silicon induced by the supersaturation of the alloy droplet from the vapor source (precursor gas). Up to now the VLS is still a key and popular mechanism for silicon nanowires growth. However, much smaller metal clusters (nanoclusters) are employed as catalysts for realizing

SiNWs because the initial size of the metal droplets will define the diameter of the SiNWs which varies from tens of nanometers to several microns [19]. In the process, the metal nanoclusters are heated above the eutectic temperature, for example, gold whose eutectic temperature is 363°C. Small Au-Si alloy droplets will form on the substrate surface. When the substrates are exposed in the precursor gas, such as silicon tetrachloride ($SiCl_4$), silane ($SiH_4$) or disilane ($Si_2H_6$), precursor molecules will crack on the surface of the Au-Si alloy droplets and meanwhile the silicon source decomposed from precursor gas is incorporated into the droplets. The sufficient Si incorporation results in the supersaturation of the alloy droplets which leads to a nucleation of the solid silicon. The continuation of this process realizes the synthesis of SiNWs with the alloy droplets riding on the tops (figure 11).

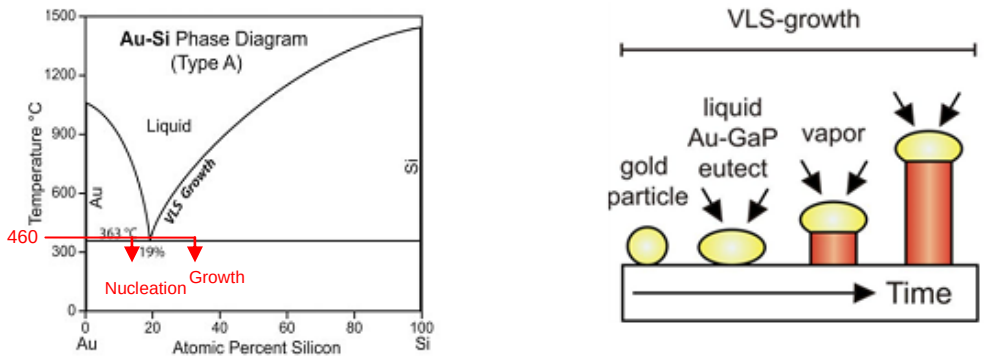


Figure 11: a) A schematic of the Au–Si binary phase diagram (PD); b) A schematic of silicon nanowire growth (using gold as catalyst) [7].

## III.1 Gold as catalyst

In the VLS growth process, a lot of metals have been reported as catalysts including Au, Fe, Ag, Zn and so on [17, 20, 21]. However, gold is always the most frequently used metal catalyst material because it has so many interesting advantages listed below:

- Availability. Gold is widely used for electrical contacts and the machine equipped for depositing a thin film, for example evaporation system, is also easily found in most semiconductor research center.
- Nontoxic that means few safety requirements is needed.

- High chemical stability. It is barely oxidized in air.
- Relatively low eutectic temperature while high Si solubility. The eutectic point of Au-Si is at a concentration of 19% Si and at the temperature of 363°C which is much lower than the melting temperature of pure Au or pure Si.
- Low vapor pressure at high temperature. This feature avoids an unwanted evaporation of gold.

Although gold has such a lot of impressive advantages, one serious drawback is that it is known as impurity in nanowire which restricts its compatibility in semiconductor electronic production standards.

## III.2 Generation of gold particles

Gold, as the widely used and well controlled metal catalyst in VLS mechanism, can be generated and deposited by various methods, including thermal evaporation, sputtering deposition, electron beam evaporation, colloidal gold, laser ablation… [22]. Their common objective is to realize appropriate nano gold particles whose size, position, surface density and cleanliness requirements are satisfied as the catalyst, which supports the subsequent VLS growth process. Here, we introduce two mostly used methods for generating gold nano particles:

1) Thin film annealing: The particles generated from thin film annealing method begin from a thin film deposition of gold on the substrate prepared by thermal evaporation system or sputter systems. The thickness of the thin film ranges from several nanometers to tens of nanometers. Then, the substrate with gold film will be transferred into the reactor chamber where the gold thin film will split up into gold particles during an annealing step up to 600°C for several minutes. The particles size depends mainly on the thickness of the catalyst film deposited [23]. A relatively long annealing time (20-30 minutes) allows for more homogeneous droplets spreading on the substrate [24]. It supplies us a simple, low cost and high throughput gold deposition method, however, the difficulties exist in the control of position, diameter and density controls.

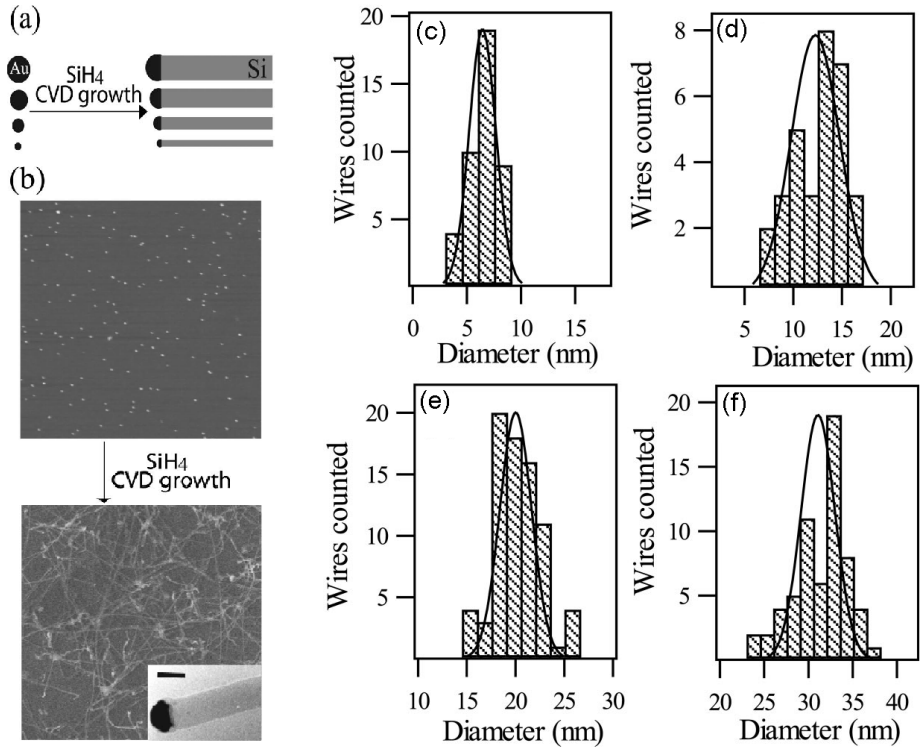


Figure 12: (a) Schematically illustrating the size-controlled synthesis of SiNWs from Au-nanoclusters. (b) AFM image of 10 nm Au-nanoclusters dispersed on the substrate (top). Field Emission Scanning Electron Microscopy (FESEM) image of SiNWs grown from the 10 nm nanoclusters (bottom). The sizes of both images are 4µm. The inset in the bottom image is a TEM micrograph of a 20.6-nm-diam SiNW with a gold catalyst at the end. The scale bar is 20 nm. (c-f) Histograms of SiNW diameters grown from 5-, 10-, 20-, and 30-nm-diam Au-nanoclusters [19].

2) Colloidal gold particle deposition: Colloid particles (colloidal solution) with well defined gold diameters (2 nm to 30 nm) are commercially available and do not suffer from the same diameter controllability problems as in the thin film annealing method. The substrate is prepared via spin-coating using a negatively charged droplet of colloidal solution on a positively charged layer made up of a 0.1 % poly-L-lysine (PLL) solution which ensures the adhesion of the gold particles to the substrate by electrostatic interactions [25]. Using this method, Y. Cui et al [19] succeeded in obtaining 5-, 10-, 20- and 30-nm-diam Au-nanoclusters and nanowires with average 6.4-, 12.3-, 20-, and 31.3-nm-diam were fabricated respectively, which demonstrated that the size of the metal catalysts determines the diameter of the formed nanowires (figure 12). This method has improved a lot in

the problem of diameter controllability, but its position control is not solved as well as thin film annealing method. In addition, it brings us a new contamination problem induced by PLL.

## III.3 Chemical Vapor Deposition

In VLS-based nanowires growth, many different growth methods have been used, including laser ablation [21], molecular beam epitaxy (MBE) [26] and Chemical Vapor Deposition (CVD). The most popular method for growing silicon nanowires is CVD that generates the gaseous semiconductor reactant source by the decomposition of precursor gas such as silane ($SiH_4$) [27, 28], disilane ($Si_2H_6$) [29], silicon tetrachloride ($SiCl_4$) [17, 30, 31]. This decomposition process can be obtained either by plasma (PECVD) or thermal energy (APCVD, LPCVD…). The decomposed Si molecules will be transported into the catalyst droplets and cracked into its constituents (figure 13).

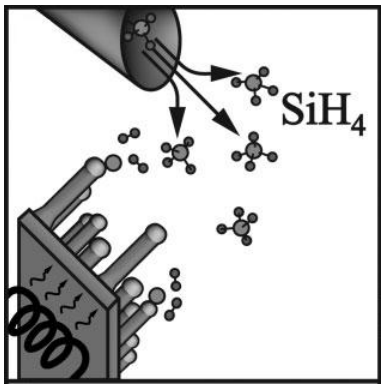


Figure 13: Schematic of experimental setups for silicon nanowires growth by CVD [17].

Advantages of CVD nanowires growth:

- The length and diameter configurations of nanowires growth can be controlled. (Such configurations of NWs realized by LPCVD will be discussed in chapter 2.)
- Offering an opportunity of a well-controlled doping by intentionally employing additional doping precursor at the same time as the silane precursor gas, so called "*in-situ* doping", and additional step for doping is not needed.

Drawbacks of CVD growth of nanowires:

- The silicon nanowires grown by CVD exhibit a certain variation of the growth direction [32, 33].
- The precursor gases, doping gases and the reaction products are often toxic and explosive which requires strict safety consideration.

## III.4 *In-situ* doping for silicon nanowires

One of the main reasons that make silicon nanowire superior to carbon nanotube is the possibility of better controlling the conductivity and carrier type by adding impurities. Silicon nanowires are generally doped by pentavalent elements (P, As, Sb…) to conduct with negative electrons (n-type) or trivalent elements (B, In…) to conduct with positive holes (p-type). This creates a number of potential applications for silicon nanowires such as field effect transistor (FET), biosensor, memory, solar cells…*In-situ* doping is such a good method that succeeds in doping the silicon nanowires. It injects the mixture of the dopant gas and the precursor gas into the reactor chamber at the same time which means the impurity atoms are being introduced into the crystal lattice in the silicon nanowires cores while the silicon nanowires are growing [34-36].

### III.4.1 N-type doping by phosphine

The most familiar gas used for the n-type doping is phosphine ($PH_3$) which is injected at the same time with the silane during the growth of silicon nanowires. To avoid deposition of silicon everywhere on the substrate, the substrate coated with gold catalyst is heated to a lower temperature of precursor gas molecules cracking (approximately <500°C) under the precursor atmosphere ($SiH_4$ combined with $PH_3$), and meanwhile the decomposited gas-phase phosphorus will be cracked into the Au-Si droplet to realize the doping. According to G. F. Zheng [34] and Y.F. Wang [37], they have demonstrated that phosphorous dopant concentration can be readily controlled by varying the ratio of $PH_3$ and $SiH_4$ ([P:Si]) grown on a <111> oriented silicon substrate. Figure 14(a) shows a plot of SiNW resistivity and carrier type as a function of [P:Si]. Significantly, when the ratio [P:Si] is increased, the resistivity is

correspondingly decreased. They have also found out that the majority of the phosphorus-doped SiNWs imaged (figure 14 (b-c)) were single crystal with a <111> growth direction, a smaller fraction of SiNWs were bicrystals with a <112> growth direction and the homogeneous deposition of Si/P doesn't occur during axial elongation (figure 15 (a-b)).

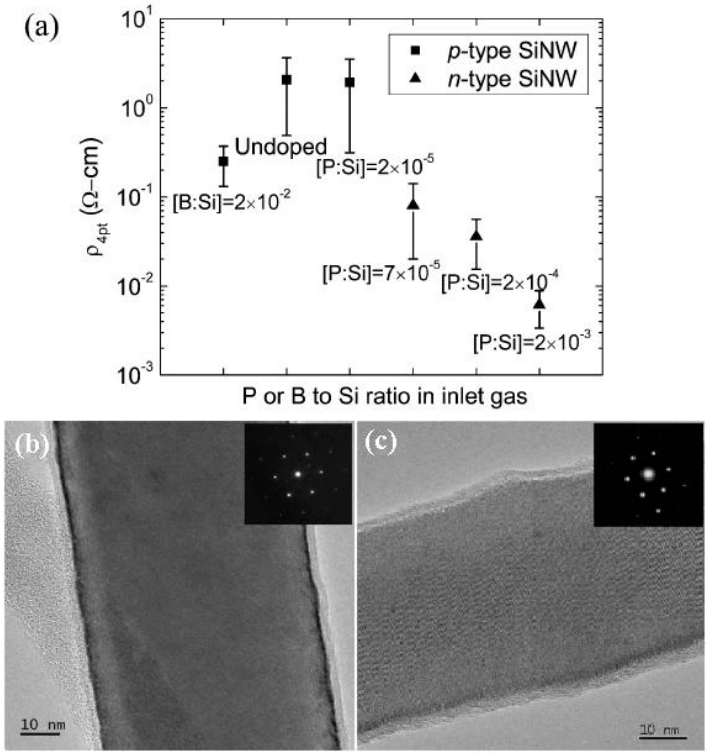


Figure 14: (a) Four-point resistivity of SiNWs grown using [B:Si]=$2\times10^{-2}$, [P:Si]=0, $2\times10^{-5}$, $7\times10^{-5}$, $2\times10^{-4}$ and $2\times10^{-3}$; TEM images of phosphorus-doped SiNWs: (b) with [P:Si]=$2\times10^{-5}$,(c) with [P:Si]=$2\times10^{-3}$ [37].

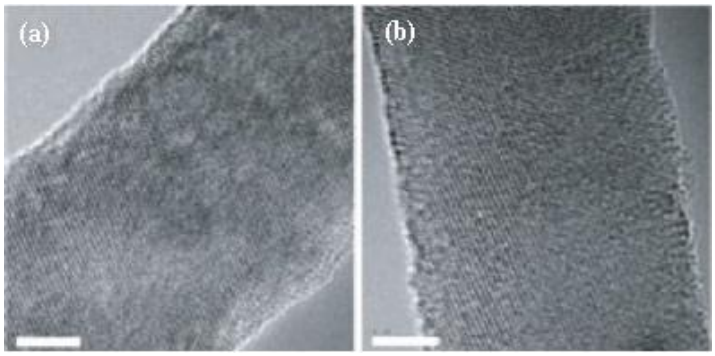


Figure 15: (a) and (b) TEM images of two opposite ends of one 22 nm diameter SiNW; the scale bar is 5 nm [34].

## III.4.2 P-type doping by diborane

Diborane ($B_2H_6$) is widely used as the p-type dopant gas [32, 33, 38, 39] while the trimethylboron (TMB-$C_3H_9B$) is also used to synthesize silicon nanowires [33]. Compared with n-type doping, p-type doping has been studied much more deeply because the experimental configurations will directly affect the morphology and the quality of the p-doped silicon nanowires. L. Pan et al [32] have studied the effect of diborane on the microstructure of SiNWs. Figures 16 (a-b) show us the SEM images of the lightly doped SiNWs using $B_2H_6$ as the doping gas, and figure 16 (c)-(e) show us two SEM and one TEM images of the highly doped SiNWs [32]. We can observe that the highly doped SiNWs are curved and kinked with an average length of approximately 8.5 µm (figure 16 (d)) and a shell of amorphous silicon is deposited outside of the doped nanowire (figure 16 (e)). This result is due to the low dissociation energy of $B_2H_6$ which is about 27 kcal/mol [40]. The $B_2H_6$ reacting with $SiH_4$ leads to an increase in µSi growth which is believed to be responsible for the formation of the amorphous Si surrounding the $B_2H_6$-doped nanowires. K-K. Lew et al [33] have investigated the use of TMB as p-type dopant gas and succeeded in doping the nanowires whose boron concentration measured can range from $1\times10^{18}$ to $4\times10^{19}$ $cm^{-3}$ [figure 17(a)]. Figure 17(b) shows a High-Resolution Transmission Electron Microscopy (HRTEM) image of TMB-doped SiNW with [111] growth orientation [33]. The dissociation energy of TMB is approximately 87 kcal/mol which leads to an increased thermal stability compared with $B_2H_6$. This enables the highly B-doped SiNWs by TMB without a thick amorphous Si coating.

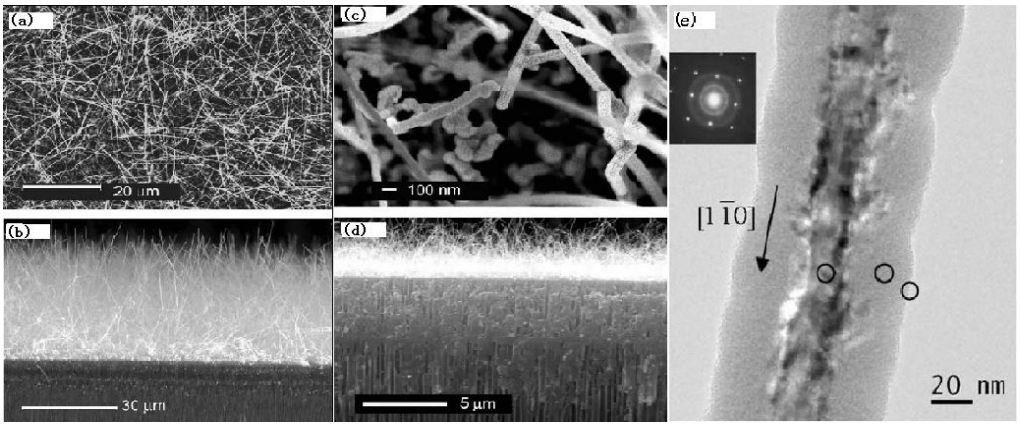


Figure 16: (a-b) SEM images of the top view and cross-sectional view of the $B_2H_6$ lower-doped SiNWs; (c-d) SEM images of highly doped SiNWs; (e) Bright-field TEM image of a typical $B_2H_6$ highly doped SiNW, showing the core-shell structure. The inset is the corresponding diffraction pattern [32].

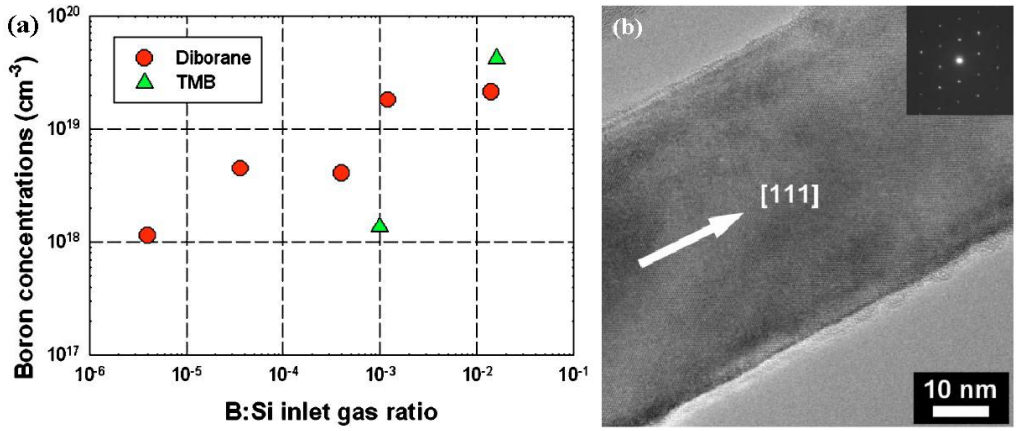


Figure 17: (a) Boron concentration in SiNWs obtained by secondary ion mass spectrometry (SIMS) measurements as a function of the [B:Si] ratio in the inlet gas.; (b) HRTEM image of TMB-doped SiNW with [111] growth orientation. A thin oxide layer was observed on the outer surface [33].

# IV Electronic devices based on silicon nanowires

During the last half century, a drastic scale-down tendency of electronics has taken place, and the industry expects to continue the miniaturization for at least next ten years. Silicon nanowires are considered as such promising materials or components that they would have a great impact in the future CMOS technology. However, before massive integration into the technology, individual electronic device with excellent performance should be realized. Fortunately, a lot of amazing electronic devices based on silicon nanowires have already been realized such as vertical nanowire field effect transistors (NWFETs), logic gates, solar cells… Although a great number of potential applications are discovered, much further work should be carried out before achieving the mass production in semiconductor industry.

## IV.1 Vertical nanowire FET

The use of nanowires in electronics enables new gate architectures for a transistor. An evolution of the field-effect-transistor is showed in figure 18. Their field effects differ from each other via different gates' surrounding structures. Obviously, the vertical NWFET has a complete and uniform wrap-around effect which depletes the channel region and that will greatly improve the performance of the transistor.

Some advantages of such structures are:

- Conduction in the whole bulk of the nanowire,
- No parasitic capacitance at the source/drain regions.
- Low leakage current.

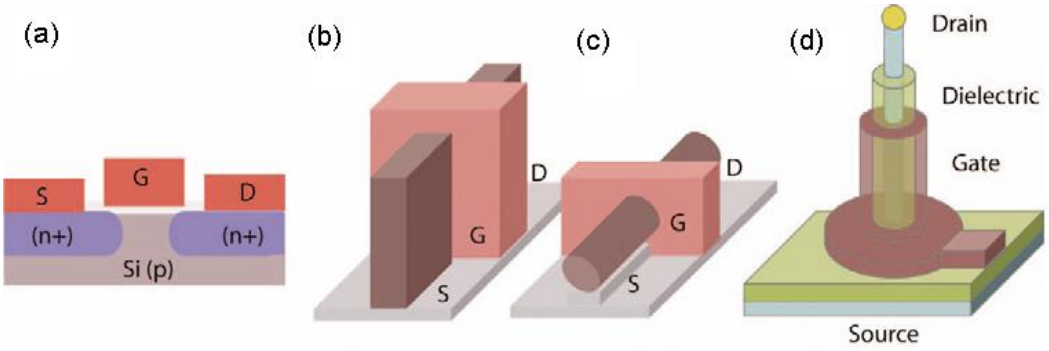


Figure 18: Field-effect-transistors, (a) MOSFET, (b) FinFET, (c) lateral NWFET, and (d) vertical NWFET [41].

Figure 19 and 20 show an example of a vertical nanowire transistor based on a 60-nm-diam, 2-µm-length silicon nanowire and its corresponding electrical characteristics. The vertical silicon nanowires are synthesized by VLS method. A 25-nm-thick $SiO_2$ gate dielectric is deposited around the nanowires and a 100-nm-thick aluminum is deposited as gate electrode. Subsequent optical lithography and wet etching will realize patterning of the gates. Finally, a top Ni contact is defined using resist as etching mask. The processing details can be acquired from the reference [42].

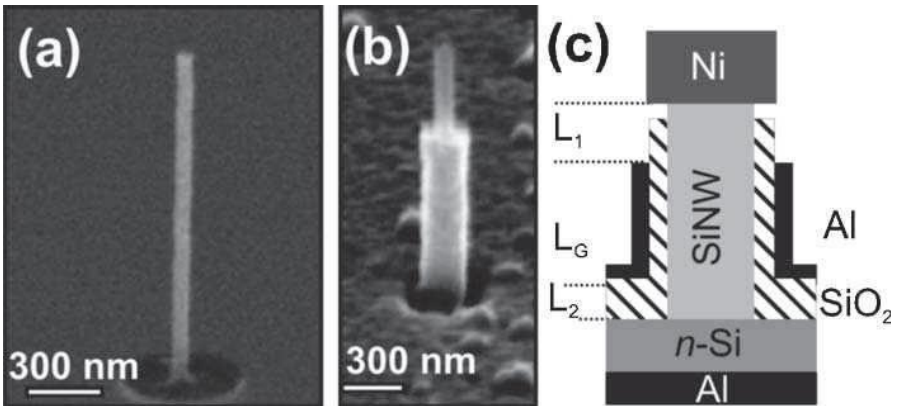


Figure 19: (a) 60-nm-diameter SiNW covered with 25 nm $SiO_2$ gate dielectric, (b) SiNW with gate length defined by etching of Al, (c) schematics of the surround-gated transistor displaying the gate length $L_G$ and ungated regions $L_1$ and $L_2$ [42].

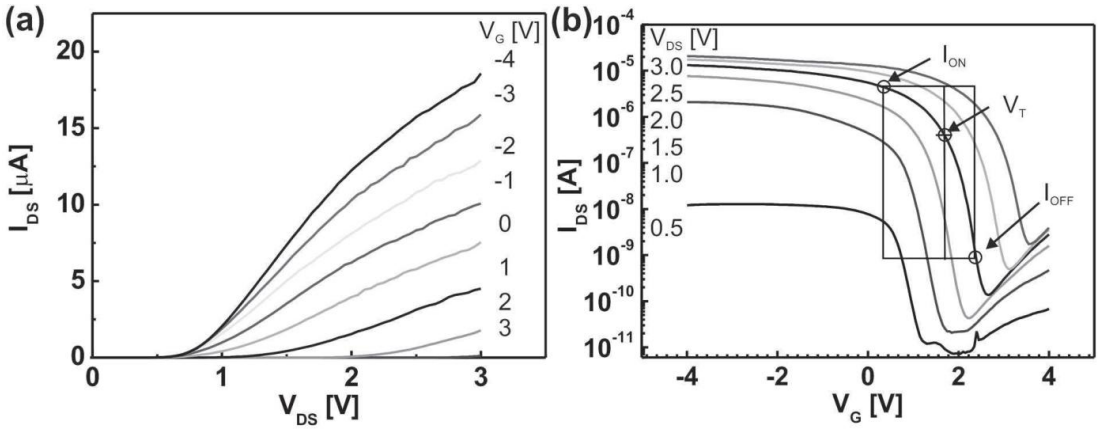


Figure 20: (a) output and (b) transfer characteristics of the vertical NWFET represented in figure 19 [42].

## IV.2 Crossed silicon nanowire-based logic gates

The crossed nanowire (cNW) architecture [43] is a powerful strategy for memory and logic devices in which the key device features can be defined during the synthesis of nanowire building blocks and their subsequent assembly. Based on cNW structure, the most important elements for logic gates, diodes and transistors [44-46], can be fabricated. The electronic characteristics of the functional elements are achieved by the two crossed nanowires which could be a p-type nanowire and an n-type nanowire. An example of a crossed SiNW p-n junction is shown in figure 21 [44]. The crossed SiNW p-n junction is assembled from two 20 nm diameter p- and n-type SiNWs.

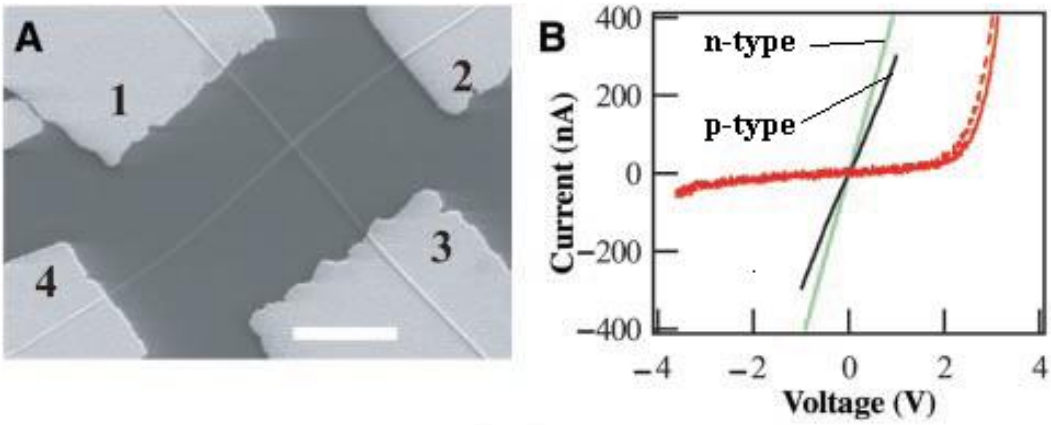


Figure 21: A) Typical Field Emission Scanning Electron Microscopy (FESEM) image of a crossed SiNW junction. The scale bar is 2 μm. B) The black and green curves correspond to the I-V behavior of individual p- and n-type SiNWs, respectively. The solid red line corresponds to voltage drop measured between 3 and 4, and the dashed red line to voltage between 3 and 2 [44].

Via the development of this assembly approach, a lot of crossbar devices can be easily fabricated, such as logic gates, decoders [47, 48]… Figure 22 shows a logic NOR gate realized by using a p-type silicon nanowire as channel unit and three n-type gallium nitride (GaN) nanowires as gates [45]. The single-crystal p-Si and n-GaN NWs are synthesized by nanocluster-catalyzed methods and have diameters of 10 to 25 and 10 to 30 nm, respectively.

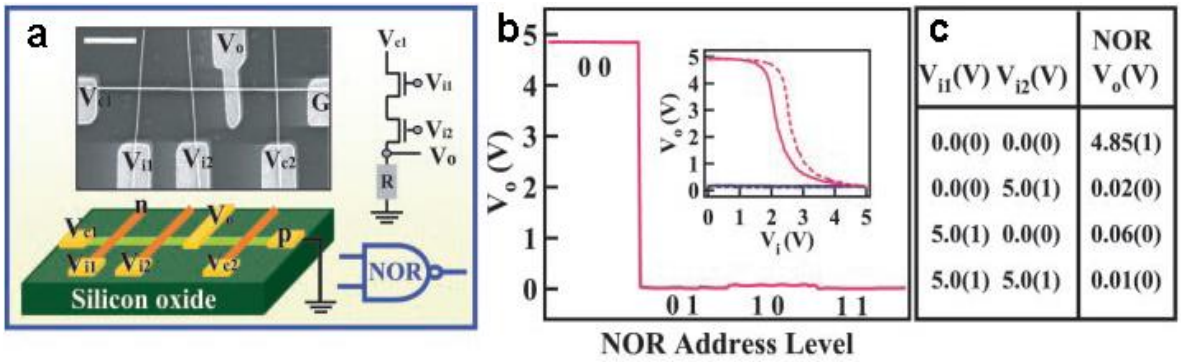


Figure 22: a) Schematic of logic NOR gate constructed from a 1 p-type silicon nanowire by 3 crossed n-type GaN nanowires junction array. b) The output voltage versus the four possible logic address level inputs. c) The measured truth table for the NOR gate [45].

## IV.3 Solar cells

With the industrial development, a large abundance of natural resources such like fossil fuel have been consumed. Therefore, the alternative renewable clean energy sources are severely in need for the future. Among various green natural energy sources, the solar energy is the most efficient and technologically potential. The energy from sunlight striking earth in an hour can meet the whole energy consumption by humans in an entire year. To make full use of solar energy, an efficient device that can capture, convert and store solar energy should be fabricated. Since the invention of Si solar cell 50 years ago [49], the Si photovoltaic solar cell devices remain the basis of the solar energy converters due to the abundance of silicon materials and the high reliability and high efficiency of silicon photovoltaic devices. Recently, the progressive developments in nanotechnology make SiNWs photovoltaic devices [50-54] become a promising candidate for building photovoltaic devices because of the following advantages:

- Simple and low-cost fabrication of large-area dense arrays of SiNWs (for example, via VLS method).
- The as-prepared SiNWs don't peel of the substrate since the as-prepared SiNWs are an integral part of the Si wafer substrate.
- The rough surfaces of the SiNWs enable almost nonreflective property due to strong light scattering and absorption.
- Good compatibility with other current Si-based microelectronics.

Here, figure 23 shows us a photovoltaic device based on a single p-type/intrinsic/n-type (p-i-n) coaxial SiNW [54]. In the radial p-n junction geometry, the single nanowire synthesized by VLS-CVD method consists of a p-type SiNW encased in intrinsic polycrystalline silicon with a further layer of n-type polycrystalline silicon. When the single p-i-n coaxial SiNW is exposed to the sunlight, the photo-carriers absorbed along the SiNW will be transferred through the short travel distances between the absorbing surfaces to the collection electrodes. An overall power conversion efficiency of 3.4% has been achieved by this solar cell which can serve as robust power sources.

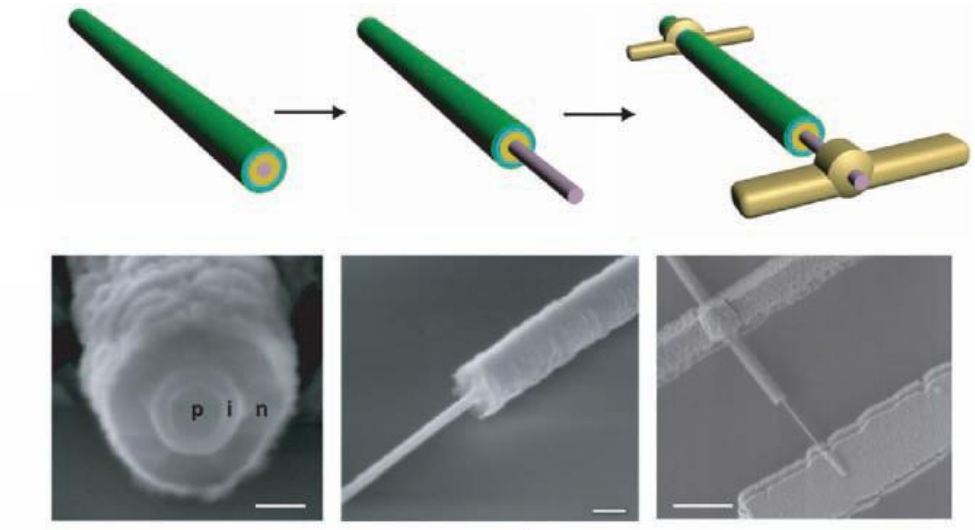


Figure 23: Schematics of a single p-i-n coaxial SiNW solar cell and corresponding SEM images [54].

## IV.4 Silicon nanowire sensors

Besides the above mentioned applications of SiNWs, devices based on silicon nanowires have many other important and promising applications especially as sensors.

Taking advantage of their small size, giant piezoresistance and large surface-to-volume ratio properties, SiNWs can be developed for various applications as sensors, such as mechanical sensors, biosensors and gas sensors… These sensors are mostly based on the transistor principle, especially field-effect transistors. The details about the mechanisms, assembly technologies and working performance will be introduced in chapter 2.

# V Conclusion

In this chapter, the nanowire growth strategies and some growth methods are firstly introduced to help us to understand the main synthesis methods. Then, the key VLS mechanism of synthesizing our NWs is explained in detail. Catalysts, reactors and doping methods are discussed, which will directly affect the quality of silicon nanowires.

In fact, the objective in our work is to realize reasonable doping concentrations and the subsequent characteristics as a sensor.

The objective of this research work is to realize microelectronic silicon nanowires based devices synthesized via the Au-catalyst VLS method. The objective of this work is to study the potential applications of these devices as chemical sensors with high sensitivity.

# Chapter II

# State-of-the-art of silicon nanowires based sensors

# I Introduction

Rapid progress in materials science and nano technologies has led to the development of electrical devices whose working performance has partially achieved specific detection functions (mechanical, electrical…) and biochemical diagnosis functions as well as human's components of organs or live cells. Today's visual technologies have already surpassed the capability of the human brain in many aspects. However, some functions of the human like olfactory system has not been achieved yet. The conventional sensors may hold some of these gas sensing problems and recently-developed nanoscale sensors based on nanowires provide a wider range of applications in pressure measuring, explosive detection, clinical assaying, working environment hazard monitoring…

The conventional biochemical sensors realize their function via adsorption of target molecules and changing the electronic states of the atoms at the reacting surface. The electrical transport characteristics will be changed directly. Most popular form of sensors is transistor which has been used to detect different analytes, because the gate effect of the transistors can increase the modulation of the channel conduction. Top suspended gate and back gate are usually used in order to avoid encapsulating the reacting surface and ensure the reacting surface having direct contact with the analytes. When a gate voltage is applied, the gate voltage will enhance or reduce the molecule adsorption on the transistor surface [55, 56, 57].

Nanoscale sensors based on nanowires used as sensitive unit follow nearly the same principle as the conventional sensors. However, they are expected to be more promising and have more significantly enhanced performance due to the following advantages:

1) Small size with dimensions on the sub-100 nm scale. The interacting biological molecules and other species of interest are also at the nanometer size scale which improves the selectivity of the sensors.

2) Large surface-to-volume ratio of one-dimensional nanowires which provides high-efficiency surface modification and then increases the sensitivity of the sensors when compared to a conventional sensor.

3) The specific properties of SiNWs like giant piezoresistivity and thermal electricity enable sensors based on silicon nanowires to transform many environmental

quantities (slight deformation, a thermal signal…) to an electrical signal with relatively high sensitivity and low power consumption.

The synthesis methods for silicon nanowires have been introduced in the previous chapter. However, for sensors based on these nanowires, the assembly modes are much more important. In order to realize the functions of sensors, the nanowires should be widely opened (noncapsulated) when the sensors are exposed to the sensing targets or modified by bioaffinitive agents. There are two most commonly used sensor structures. The first one is single nanowire sensor (figure 24). The single nanowire is the only transmission channel between the two electrodes. This kind of sensor can be fabricated by many different ways (pick-and-place approach [35, 58], the superlattice nanowire pattern transfer (SNAP) approach [59] and so on) whose objective is to locate a single nanowire on a certain position. The metal electrodes could be pre-patterned on the substrate before placing the nanowire or be defined at both ends of the single nanowire after. However, in most cases, due to the difficulty with precise positioning, size control and self orientation (especially in planar configuration) of the silicon nanowires after synthesis, post positioning methods are usually used for addressing silicon nanowires. Although these methods are feasible to realize the single nanowire sensor, the drawbacks such as device-to-device non-uniformity, time-consuming and unsuitable for large-scale manufacturing, are evident.

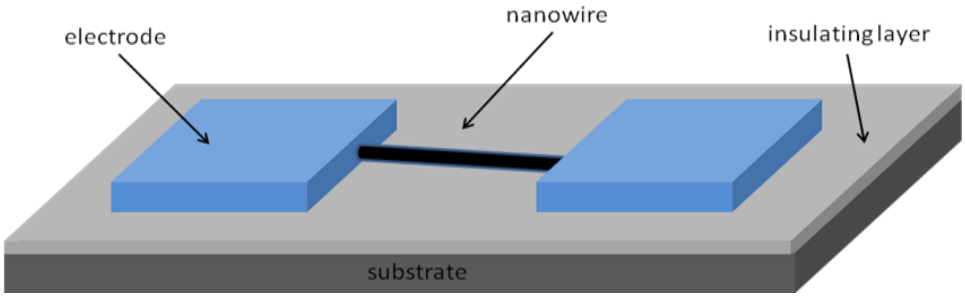


Figure 24: a schematic of a single nanowire sensor.

The second sensor structure is based on bundles (carpet) of nanowires (figure 25) and is generally used as a resistive nanowires sensor. The electrical conduction between source and drain is transferred through the whole nanowires network. The electrodes can be interdigitated to increase the active sensor area and the separation of the electrodes can be longer than the single nanowire sensor (see chapter 3). Nanowires electrical addressing does

not need additional transfer step for nanowires. In this case, the bundles of nanowires can be prepared directly on the substrate by most of main synthesis methods like VLS or SLS.

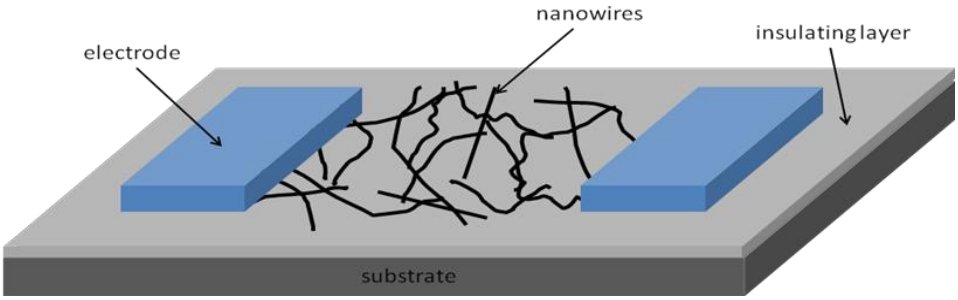


Figure 25: a schematic of a carpet nanowires sensor.

Compared with the single nanowire sensor, the fabrication method of the bundles of nanowires sensor is much easier and more efficient, but the response speed becomes slower because of the longer transmission distance.

## II Silicon nanowires based mechanical sensors

Since 1954, C.S. Smith et al. have studied the various effects of strain on silicon [60]. It is recognized that the resistance changes not only due to the change in geometry but also due to the resistivity of the material. The piezoresistive effect of semiconductor materials can be several orders of magnitudes larger than the geometrical effect in metals. So semiconductor materials, and in particular silicon, can be used to create a sensitive mechanical sensor and almost every semiconductor manufacturer has announced their version of strained CMOS [61].

Recently, with the rapid development of nano technology, the silicon nanowire has been studied experimentally and theoretically as a particular attractive candidate material to realize nanoelectromechanical systems (NEMS). R. He and P. Yang [62, 63] have reported that silicon nanowires possess an unusually large piezoresistance effect compared with bulk. The relationship between conductivity/resistivity and stress/strain is given by:

$$\pi_l^{\sigma} = \frac{1}{X}\frac{\Delta\sigma}{\sigma_0} \quad (1)$$

where $\sigma_0$ is the conductivity under zero stress and X is the stress. The longitudinal piezoresistance coefficient [64] along the <111> direction for p-type Si nanowires can reach 37 times larger than the piezoresistance coefficient for bulk. Such giant piezoresistance effect in silicon nanowires can be used to realize a more efficient sensitive nano-mechanical sensor.

Figure 26-(a) shows a nano-mechanical sensor based on one single nanowire [62, 63]. Most of such single nanowire-based devices are fabricated by the pick-and-place approach to realize FETs and chemical sensors. Here, the suspended 2 µm length p-type Si nanowires have been grown laterally via gold catalyst VLS-CVD method. Si nanowires grow preferentially along <111> direction from vertical <111>-oriented faces pre-patterned microtrenches on a <110>-oriented SOI substrate (figure 26-(b)). The advantages of this method over the pick-and-place approach are that the nanowire synthesis and device fabrication can be achieved simultaneously, and the length of nanowires can be well controlled during the self-assembly process. When the nanowires were over grown, which means the length of the nanowires exceeded the widths of the trenches, a self-welding connection was achieved. As shown in figure 26-(b), the backward growth of nanowire directly indicates that nanowire should be self-welded with the opposite sidewalls and should form solid connections, which is very important for a mechanical sensor to avoid the fracture between the nanowires and the sidewalls.

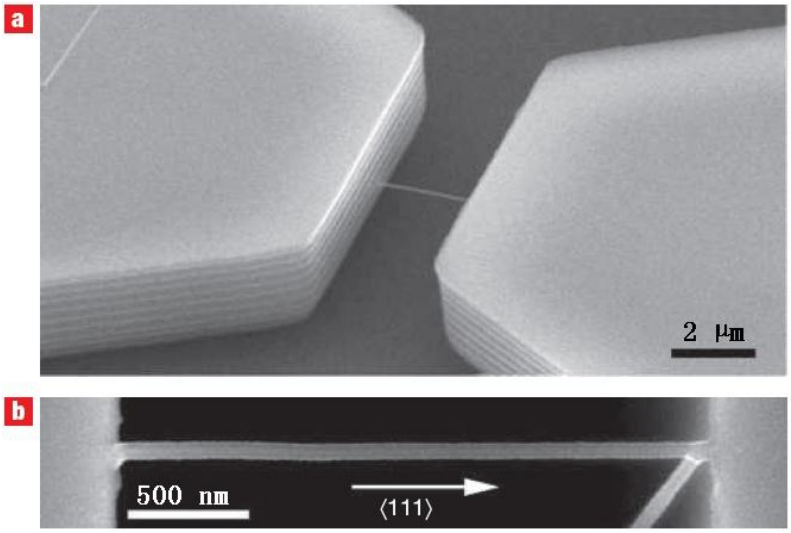


Figure 26: (a) SEM image of a <111>-oriented nanowire grown in trench on <110>-oriented silicon-on-insulator (SOI) wafer, (b) an enlarged image of the bridged nanowire which finally grew backwards after self-welding into the sidewall. The scale bars in (a) and (b) are 2 µm and 500 nm, respectively [63].

Uniaxial stresses were applied on Si nanowire along its length by the four-point bending method. A schematic for the four-point bending setup is shown in figure 27-(a) and the details about the method can be acquired in reference [65]. The I-V characteristics curves (figure 27-(b)) and the uniaxial stresses were performed simultaneously. The conductance of the nanowire (70 nm × 1.2 µm) increases under compressive stresses and decreases under tensile stresses. Relative changes in conductivity $\Delta\sigma/\sigma_0$ for this nanowire can be calculated from the curves of figure 27-(b) and the piezoresistance coefficient $\pi^{\sigma}_{<111>}$ can be deduced according to the equation (1) at the same time. The relationships between $\Delta\sigma/\sigma_0$ and stress X

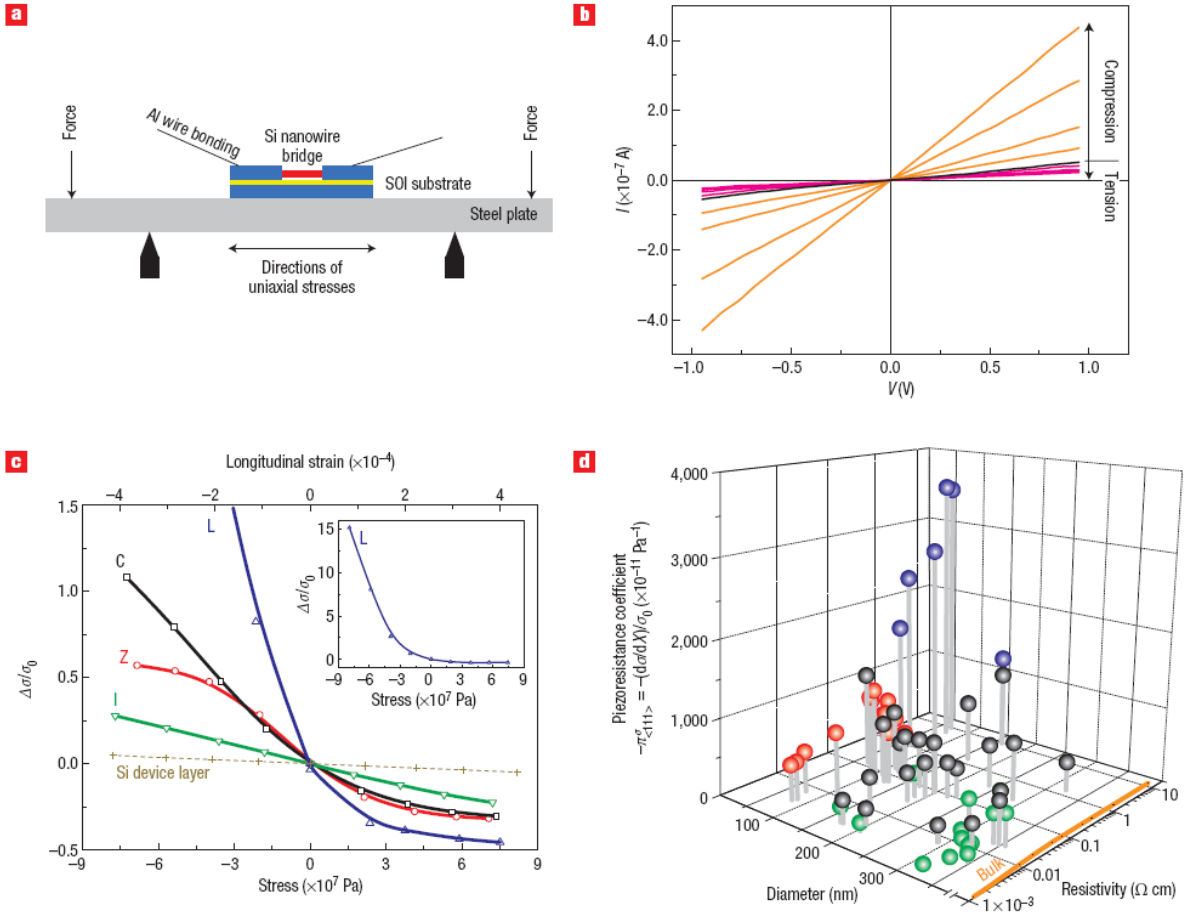


Figure 27: (a) Schematic diagram for the four-point bending setup; (b) I-V characteristics curves of a p-type <111>-oriented nanowire (70 nm × 1.2 µm) under compressive and tensile stresses; (c) Relationships between the relative change in conductivity $\Delta\sigma/\sigma_0$ and stress/longitudinal strain. Four types of nonlinear behaviours of nanowires are shown, labeled with letters I, C, L and Z. The inset shows the overview for L. (d) First-order longitudinal piezoresistance coefficient of p-type Si nanowires and its dependence on diameter and resistivity [63].

and the statistical piezoresistance coefficients $\pi^{\sigma}_{<111>}$, from nanowires with different diameters and resistivities, including bulk Si whose resistivity is 1 Ω·cm as reference, were plotted in figures 27-(c) and (d).

The $\pi^{\sigma}_{<111>}$ for p-type Si nanowires can reach as high as -3,550×$10^{-11}$$Pa^{-1}$, while the piezoresistance coefficient for bulk has only -94×$10^{-11}$$Pa^{-1}$. They have deduced that the piezoresistance coefficient increases with decreasing nanowire doping level and diameter of the nanowire. Thanks to the 1-D nano-structure and the giant piezoresistance coefficient, p-type <111>-oriented Si nanowires enable many applications in flexible electronics and nanoelectromechanical systems. Compared with bulk Si or conventional mechanical sensor, the SiNW sensor is more sensitive and has more efficient performances.

# III Silicon nanowires based chemical and biological sensors

Today, chemical or biological sensors are widely used in many domains such as medicine, diet, environmental security… But at the same time, the requirements on the sensors become more and more strict. Thanks to their high surface area to volume ratio and diameters comparable to those of the chemical and biological species being sensed, the 1-D nanowires can be used as nano sensors with a high sensitivity in both chemical and biological domains. The details about the mechanisms, assembly technologies and working performance for different sensors will be presented in the following sections.

## III.1 Silicon nanowires based gas sensors

Silicon gas sensors are very attractive because of their interesting properties such as high sensitivity, compatibility with classical silicon technology, low cost and low power consumption. They are usually used for detecting the oxidizing gas like nitrogen dioxide ($NO_2$) and the reducing gas like ammonia ($NH_3$). The detection of $NO_2$ is important for monitoring environmental pollution resulted from automotive emissions [66] and the detection of $NH_3$ is needed in industrial and medical environments [67]. Recently, the SiNW gas sensors (porous SiNWs [68], SiNWs bundles [69], SiNWs arrays [70]…) become more

and more popular than silicon film gas sensors, because their surface conductivity and surface potential are easier to be affected due to the large surface to volume ratio.

### III.1.1 Suspended Gate Field Effect Transistor gas sensor

Previous studies in DM2-IETR have demonstrated a successful suspended-gate field effect transistor (SGFET) which has application in gas detection. The structure of the SGFET is shown in figure 28 [71]. The key steps of the procedure are introduced briefly as below. A layer of undoped polycrystalline silicon and a layer of heavily doped polycrystalline silicon are etched successively to define channel zone, source and drain regions, respectively. Then, a 500 nm thick sacrificial layer of germanium is deposited and patterned to form the bridge anchors. The thickness of the sacrificial layer is the exact height of the air-gap. After definition of gate, source and drain contacts, the last step is to remove the sacrificial layer via wet etching using hydrogen peroxide ($H_2O_2$).

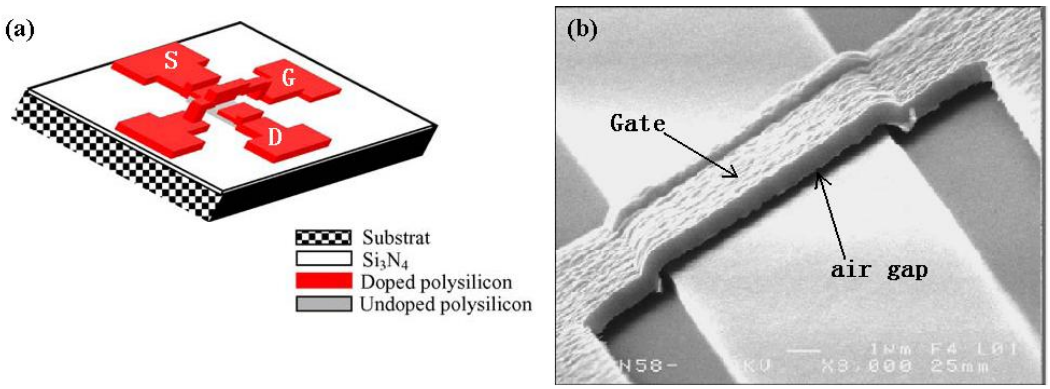


Figure 28: (a) A 3-D schematic of an SGFET, (b) SEM image of a top view for SGFET [71].

The transfer characteristic of SGFET under $NO_2$ and $NH_3$ are shown in figure 29 and 30. Before exposure to $NO_2$ at 10% relative humidity (RH), the reference curves are measured in air with the same conditions. We can observe that the $I_{on}$ decreases systematically as a result of the introduction of $NO_2$ (figure 29-(a)), because the molecules of $NO_2$ act as acceptor centers (known as oxidizing agent [72]) and create negative ions $NO_2^-$. Once these ions have been adsorbed on silicon surface, the free carriers (electrons) concentration in silicon would be decreased. In other words, negative ions $NO_2^-$ adsorbed on the surface of active layer

(channel zone) act as negative charges $-Q_{ss}$ in gate insulator, thus explaining threshold voltage increasing for N-type channel transistor (figure 29-(b)).

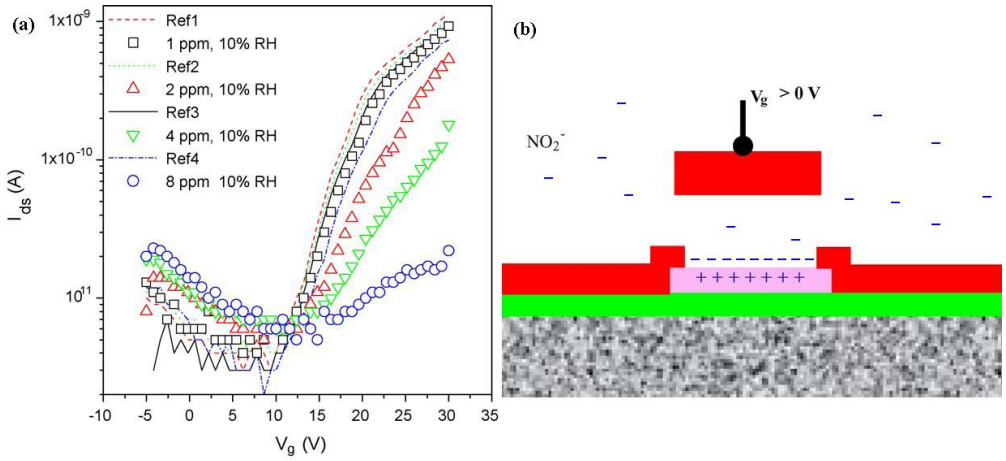


Figure 29: (a) Transfer characteristics of N-type SGFET under different $NO_2$ contents in parts-per-million (ppm) at 10% relative humidity (RH) synthetic air, (b) Negative charges $-Q_{ss}$ due to $NO_2$ adsorption on channel surface [71].

Contrary to $NO_2$ effect, the $NH_3$ effect is exactly inverse (figure 30). The reducing character of $NH_3$ leads to the negative shift of the threshold voltage. Indeed, the molecules of ammonia act as donor centers (reducing agent). Once they have been adsorbed on silicon surface, positive ions $NH_3^+$ act as positive charges $+Q_{ss}$ thus explaining threshold voltage decreasing.

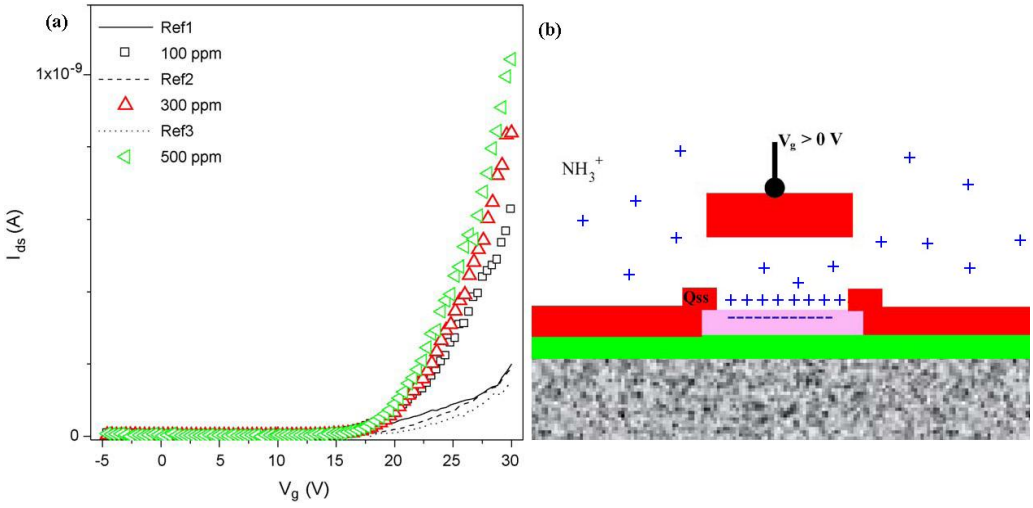


Figure 30: (a) Transfer characteristics of N-type SGFET under different $NH_3$ content in ppm or under dry synthetic air, (b) Positive charges $+Q_{ss}$ due to $NH_3$ adsorption on channel surface [71].

The threshold voltage $V_{th}$ of SGFET can be expressed by:

$$V_{th} = \frac{\Phi_M - \Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\emptyset_f \quad (2)$$

where $\Phi_{MS}$ is the difference between the work functions of the gate material and the semiconductor, $\varphi_F$ the Fermi level position in the semiconductor versus the mid-gap, $Q_{SC}$ the space-charge in the semiconductor, C the total capacitance between the gate material and the semiconductor, $e_{ox}$ the thickness of the insulator, $\rho(x)$ is the charge in the insulator at a distance of $x$ from the gate, $Q_{ss}$ is the charges on the surface of active layer (channel zone) which is equal to $\int_0^{e_{ox}} x\rho(x)dx$. Usually only the last variation $-\frac{Q_{ss}}{Ce_{ox}}$ is considered in this SGFET which influences the final $V_{th}$, because the charges in the ambience directly lead to the variation of $\rho(x)$ in case of a high field due to a very low gap. This property enables the SGFET being used as an excellent gas sensor.

## III.1.2 Silicon nanowires gas sensors

Researchers have made great efforts to develop a gas sensor which can sense gases (for example, $NO_x$) at room temperature for a long time. In the last few decades, one of the most important gas sensors is made of metal oxides (ZnO, $In_2O_3$…) [73-75]. However, the metal oxide based sensors can generally only be operated above 200°C [66, 76]. So, a sensor based on other materials should be realized to achieve the detection function at room temperature. In particular, silicon nanowire is just such material that could be used because it is a highly resistive material for exchanging with oxidizing and reducing gases at room temperature.

### III.1.2.1 $NO_2$ effect

J.R. Heath et al. [59, 77, 78] have realized a gas sensor based on SiNW arrays on flexible plastics, which is suitable for sensing gaseous nitrogen oxide ($NO_2$) at room temperature. The highly regular p-type SiNWs arrays were firstly realized by the superlattice

nanowire pattern transfer (SNAP) approach [59] on a SOI substrate, and then transferred on the plastic substrate by a dry-transfer method described in reference [77]. After transferring of the SiNWs on plastic substrate, two titanium (Ti) electrodes were patterned on the surface of the as-prepared SiNWs samples. The schematic of the SiNWs gas sensor and the measuring installation are illustrated in figure 31 [78].

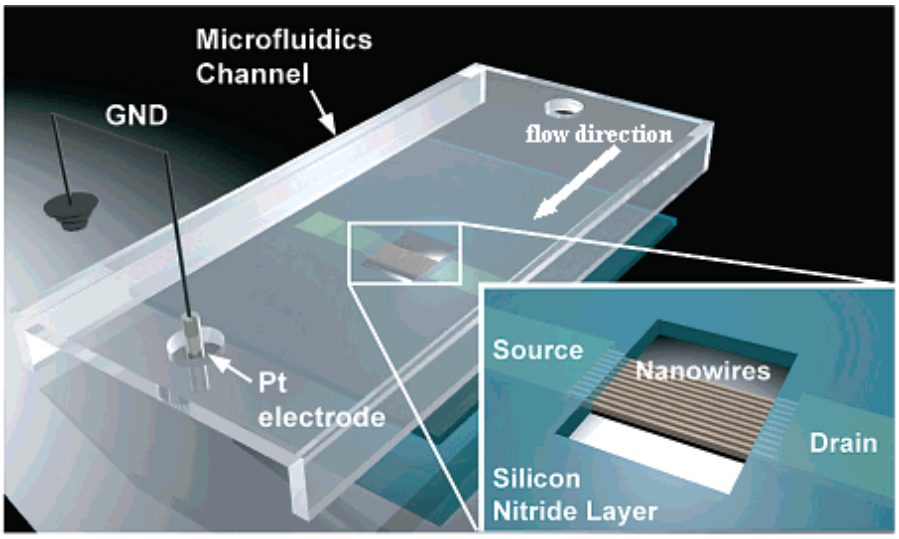


Figure 31: Schematic of the SiNWs arrays $NO_2$ gas sensor and the measuring installation [78].

The sensor device was placed in a test chamber where a continuous flow of $NO_2$ diluted in $N_2$ passed through. The gas sensing measurements were performed by monitoring the resistance of the SiNW array under different $NO_2$ concentrations at room temperature. In the figure 32, we can observe the variation of the resistance before and after $NO_2$ exposure when the $NO_2$ concentration is regulated from 20 parts-per-million (ppm) to 20 parts-per-billion (ppb). When the sensor device was exposed to the 20 ppm $NO_2$, the current was increased about 3000% after only 1.25 min. Although the response time under 20 ppb is much longer than the measurement under 20 ppm $NO_2$, the sensor device succeeded in detecting concentrations down to 20 ppb of $NO_2$ as showed in figure 32-inset. The author suggests that the increase in current after exposure to $NO_2$ should be the strong electron-withdrawing capabilities of $NO_2$, which have the equivalent effect of hole carrier injections into the p-type SiNWs.

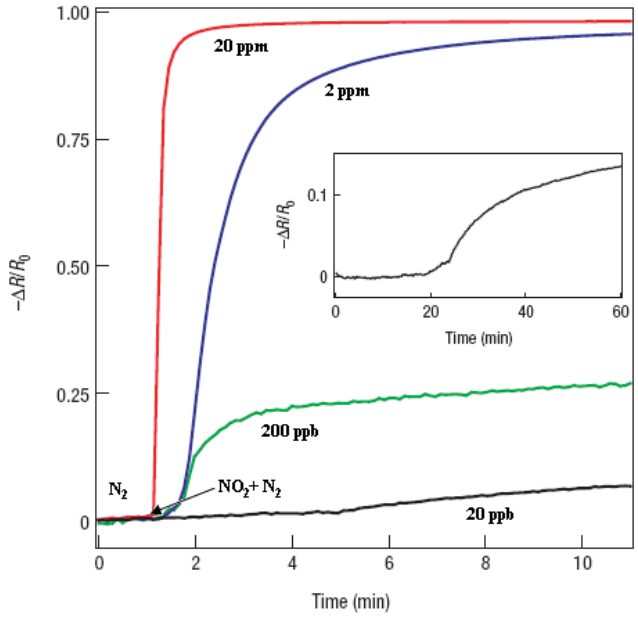


Figure 32: Electrical response of a nanowire sensor to 20 ppm, 2 ppm, 200 ppb and 20 ppb $NO_2$ diluted in $N_2$ at room temperature. Inset: an extended response of the sensor to 20 ppb $NO_2$. $-\Delta R/R_0 = -(R - R_0)/R_0$ where $R_0$ and R denote the SiNWs resistance before and after $NO_2$ exposure, respectively [77].

## III.1.2.2 $NH_3$ effect

X.T. Zhou et al. [69] have realized a gas sensor made by a bundle of SiNWs which exhibits a fast response, high sensitivity and reversibility upon exposure to ammonia gas at room temperature. These SiNWs are produced in large quantity by oxide-assisted growth method following a process described in reference [79]. Before the bundles of SiNWs were pressed at about 0.4 mg in weight onto the surface of insulating glasses, the amorphous silicon oxide was etched by 5% hydrofluoric acid (HF) solution for 2 min. Then, two droplets of silver glue were deposited on the ends of the bundles of SiNWs as electrodes. The schematic of the bundles of SiNWs sensor is shown in figure 33.

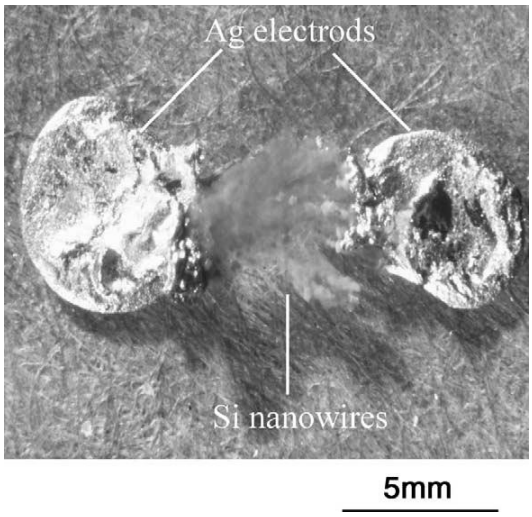


Figure 33: Optical micrograph of a silicon nanowire $NH_3$ sensor [69].

The sensing measurements were carried out in a vacuum chamber which can be pumped by a mechanical pump. A dc source was connected between the two silver electrodes, and the voltage of the dc source was fixed at 10 V. The sensitivity of the sensor was demonstrated by monitoring the variation of the resistance before and after exposure under diluted $NH_3$ in $N_2$ at room temperature. When the mixture of $N_2$ and $NH_3$ (flowrates of $N_2$ and $NH_3$ were 1000 sccm and 1 sccm, respectively) was introduced into the vacuum chamber, we can observe that the resistance of the SiNWs had a four orders of magnitude decreases after the exposure (figure 34-(a)). However, it should be noticed that the pressure inside the reaction chamber was changed after introducing gases. In order to eliminate the influence of the pressure, the same measuring process was repeated by introducing pure $N_2$. Compared with the mixture $NH_3/N_2$, there is only one order of magnitude decrease in the resistance of the same sample, which means that the variation of the resistance of bundle of SiNWs is extremely sensitive to $NH_3$. The sensing protocol can also be performed inversely and the results are illustrated in figure 34-(b).

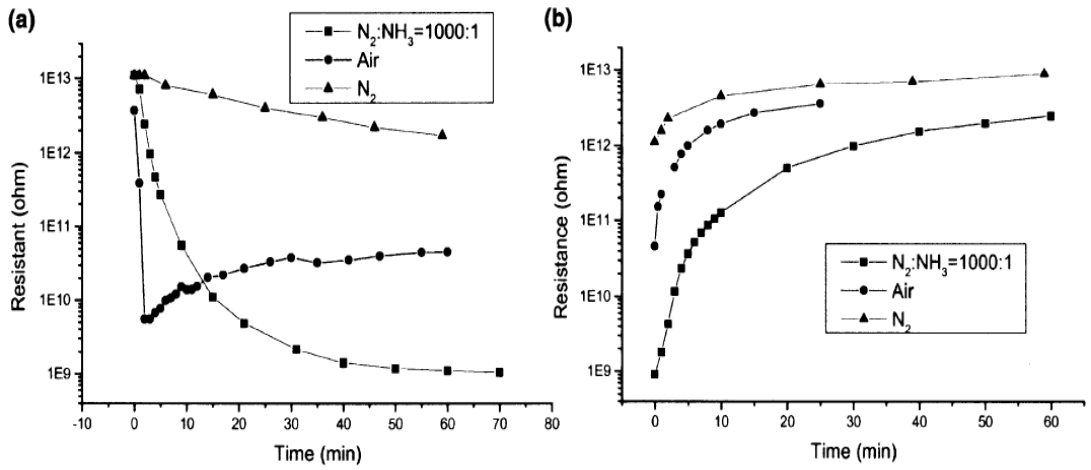


Figure 34: Electrical responses of the Si nanowires bundle under exposure to $N_2$, a mixture of $N_2$, $NH_3$ ($NH_3$ concentration: 1000 ppm), and air with a relative humidity of 60%; (a) when the gases are introduced into the chamber, (b) when the gases are pumped away [69].

The author deduced two possible explanations. One is that the $NH_3$ molecules adsorbed on the surface of the SiNWs through the charge exchange $NH_3 \rightarrow NH_3^+ + e^-$ could directly inject electron carriers into the SiNWs, thus decreasing the resistance. The other is that the adsorbed gas molecules, $NH_3^+$, may act as a chemical gate, which shifts the Fermi level of the SiNWs in the upper part of the band gap and reduces the resistance of the sample.

## III.2 pH sensors

Among the variety of semiconductor sensors, pH sensor is closely related to our daily life. The pH sensor is widely used in monitoring environmental conservation, chemical and food industries. As an important representative of the pH sensor, ion sensitive field-effect transistor (ISFET) has been researched and developed for more than 40 years. However, recent ten years' research on pH sensor based on SiNWs has already revealed excellent performance and application prospect although they have not a research history as long as ISFET pH sensor. In this section, an ISFET pH sensor and a SiNW pH sensor will be introduced.

### III.2.1 ISFET pH sensor

The ion sensitive field-effect transistor (ISFET) was firstly introduced by P. Bergveld in 1970 [80]. The devices can be used as pH sensor via measuring the ion concentrations in solution. The ISFET is in fact nothing else than a MOSFET whose principle is to control the current transferring between the source and drain zones by applying a gate voltage, whereas the physical gate of MOSFET is replaced by a reference electrode inserted in an aqueous solution (see figure 35). The reference electrode is encapsulated by an insulating membrane which is sensible to the variation of ions concentration. The membrane of the ISFET can be $SiO_2$, $Al_2O_3$ [81], $Si_3N_4$ [82].

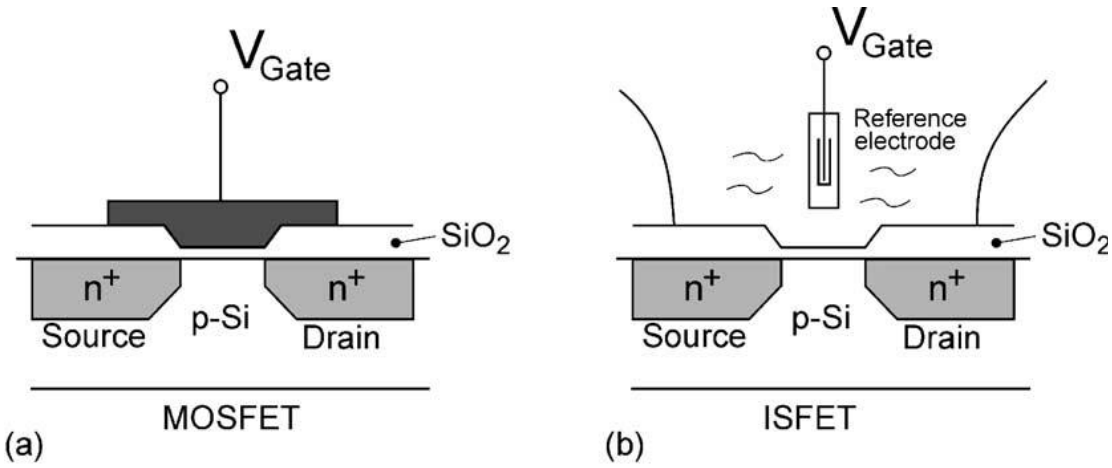


Figure 35: Schematic representation of MOSFET (a) and ISFET (b) [83].

In this case, the threshold voltage of MOSFET is expressed as:

$$V_{th} = \frac{\Phi_M - \Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\emptyset_f \qquad (3)$$

where the first term reflects the difference in work function between the gate metal $\Phi_M$ and the silicon $\Phi_{Si}$, $Q_{ox}$, $Q_{ss}$ and $Q_B$ represent respectively the accumulated charge in the oxide, at the oxide-silicon interface and the depletion charge in the silicon. The last term determines the onset of inversion depending on the doping level of the silicon. A schematic band diagram of MOSFET is illustrated in figure 36.

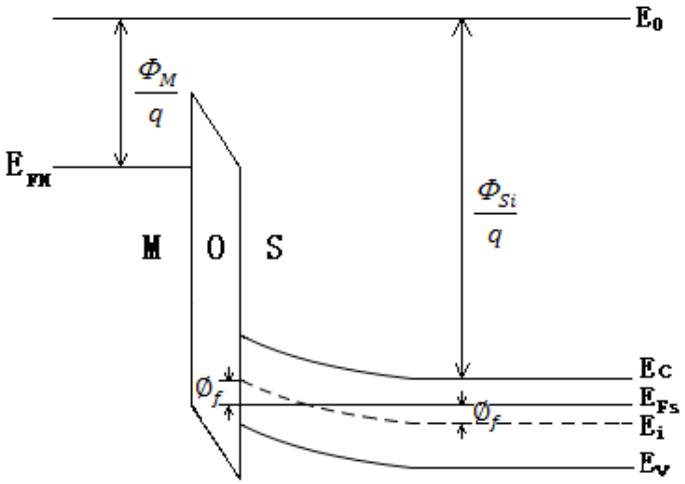


Figure 36: A schematic band diagram of MOSFET.

In the case of ISFET, the above equation becomes:

$$V_{th} = E_{ref} - \Psi + \chi^{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ox}+Q_{ss}+Q_B}{C_{ox}} + 2\emptyset_f \quad (4)$$

$$\Psi = 2.3\frac{KT}{q}\frac{\beta}{\beta+1}(pH_{pzc} - pH) \quad (5)$$

In the equations (4), $E_{ref}$ represents the potential of the reference electrode, the chemical potential $\Psi$ is a function of pH (equation 5) and $\chi^{sol}$ is a constant parameter representing the surface potential of the solvent. In the equation (5), $\beta$ is the significant factor in the quality of the interface insulator/electrolyte. $pH_{pzc}$, called “pH point of zero charge”, is a particular pH for which the surface of the membrane has a zero charge.

The principle of ISFET chemical sensor is based on the trapping of ions at the sensitive layer. The trapped charges induce a change in chemical potential $\Psi$ and thus changing the threshold voltage $V_{th}$ of the transistor.

The sensibility of the ISFET is expressed as:

$$S = \frac{d\Psi}{dpH} = 2.3\left(\frac{KT}{q}\right) * \frac{\beta}{\beta+1} \quad (6)$$

For an excellent insulator ($\beta \gg 1$), the sensibility obeys the Nernst's law which can reach 59.2 mV/pH.

When the reference electrode is connected to the source (Vgs = 2 V), the Id-Vds curves can be modulated by changing the pH values of the solution (figure 37-(a)). It is just the modulation property which enables the ISFET acting as a pH sensor. The $SnO_2$/Al gate ISFET has a linear pH sensitivity of approximately 58 mV/pH in the concentration range between pH 2 and 10 as shown in figure 37-(b) [84].

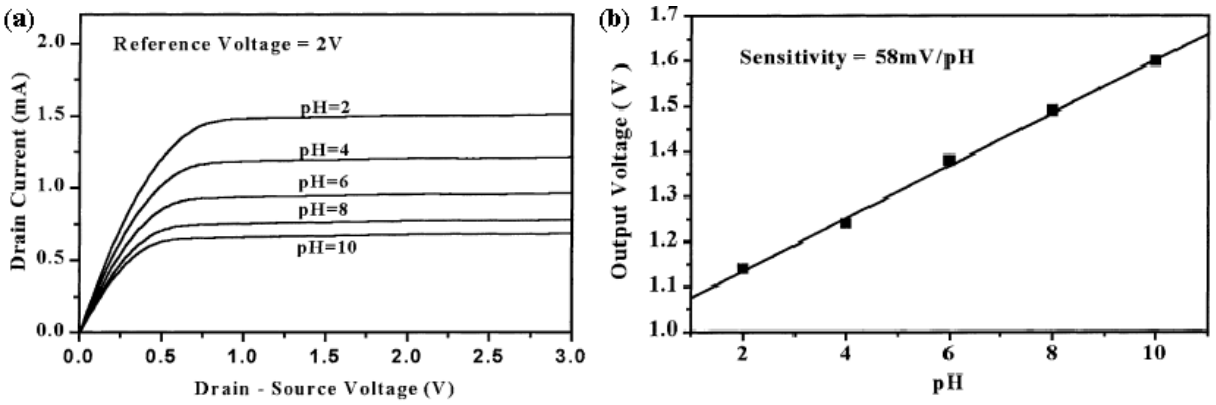


Figure 37: (a) Id (Vds) characteristics of ISFET when Vref = 2 V for different pH values, (b) plots of the output voltage versus pH values [84].

## III.2.2 SiNW pH sensor

The first pH sensor based on SiNW FET was proposed in 2001 by the group of Lieber [85]. The silicon oxide surface on the substrate is modified by 3-aminopropyltriethoxysilane (APTES) acting as silylation reagent for coating silica surfaces to add primary amines, which can be used to crosslink and immobilize proteins and other molecules. In this case, it undergoes protonation (addition of a positive hydrogen ion $H^+$) and deprotonation, where the changes of charges in the surface can chemically gate the SiNW. The single-crystal (boron-doped) SiNW was prepared by a nanocluster-mediated VLS growth method. The nanowire

was located on oxidized silicon substrate by flow aligning described in [86] which flew a suspension of NW into the channel of a PDMS mold (figure 38).

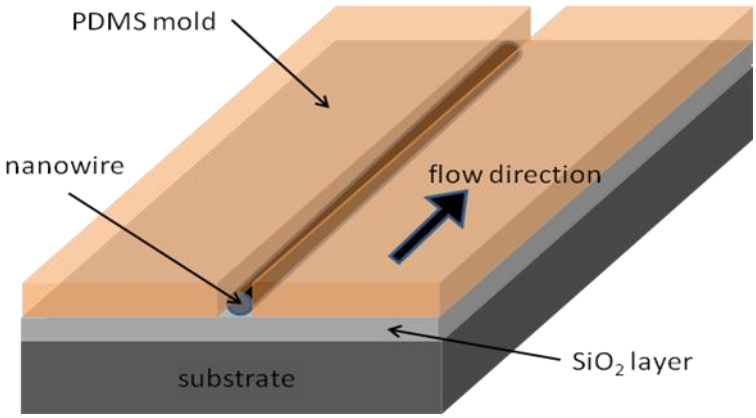


Figure 38: Schematic of a channel formed when the PDMS mold was brought in contact with a flat substrate.

After removal of the mold, the electrodes were defined by EBL to the NW ends (figure 39-(a)). The ohmic SiNW-metal contacts ensure a linear I-V behavior and a stepwise increase conductance (dI/dV) with discrete changes of gate voltage from 10 to -10 V (figure 39-(b) insets). When a continuous flow of controllable pH solution flew along the microfluidic channel, the conductance as a function of time and pH solution demonstrated a similar stepwise increase with discrete changes in pH from 2 to 9. Such behavior suggests that the different ranges of pH solution could replace the gate effect for the SiNW FET, and the modified SiNWs FET could function as nanoscale pH sensor (figure 39-(b)). Y. Cui et al have explained that this behavior was due to covalently linking APTES to SiNW oxide surface which resulted in a surface terminating in both $-NH_2$ and -SiOH groups (figure 39-(a)). The $-NH_2$ group is protonated to $-NH_3^+$ [87] and acts as a positive gate at low pH, which decreases the conductance. The -SiOH is deprotonated to $-SiO^-$ and acts as a negative gate at high pH, which correspondingly causes an increase in conductance.

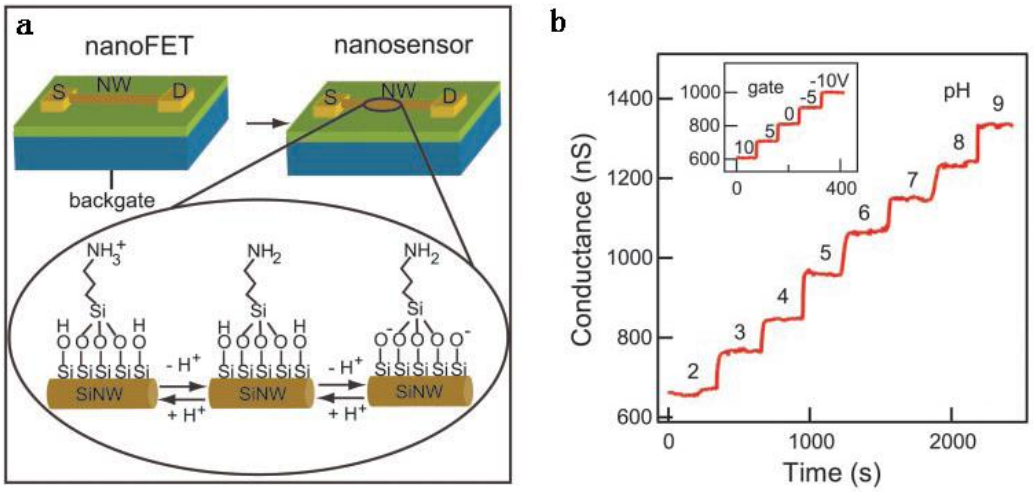


Figure 39: (a) Schematic illustrating the conversion of a NW FET into NW nanosensors for pH sensing. Zoom of the APTES-modified SiNW surface illustrating changes in the surface charge state with pH; (b) Real-time detection of the conductance for an APTES-modified SiNW for pHs from 2 to 9; (inset) Plot of the time-dependent conductance of a SiNW FET as a function of the back-gate voltage [85].

Compared with the ISFET, whose theoretical best sensitivity can reach at about 59.2 mV/pH predicted by Nernst's law, the SiNW pH sensor introduced here has a much better sensitivity about 100 ns/pH (4.7 V/pH after conversion). However, the drawbacks of the SiNW pH sensor are also evident as time-consuming for fabrication and device non-uniformity while the ISFET has already gone into mass-production.

## III.3 Biological sensor: example of DNA hybridization

The group of C.M. Lieber in Harvard University has also fabricated a high sensitive DNA sensor based on nanowires [88]. Figure 40-(a) shows schematic of the sensor device consisting of a SiNW and a microfluidic channel, where the arrows indicate the direction of sample flow.

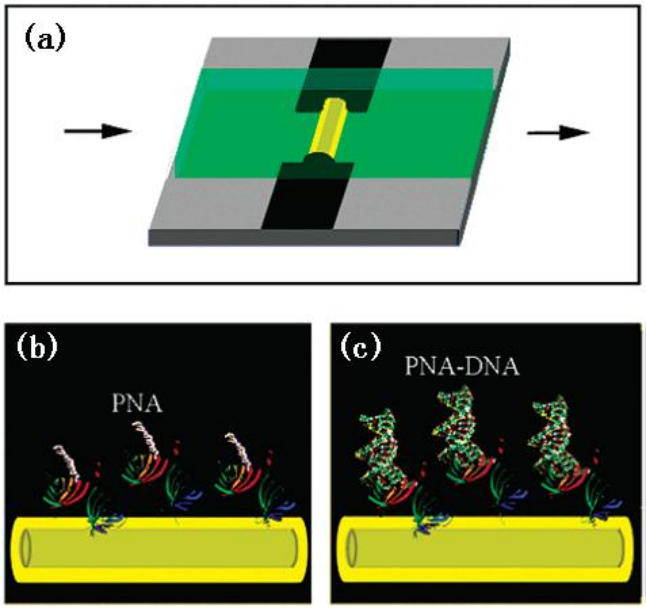


Figure 40: (a) Schematic of the nanowire sensor, (b) The SiNW surface with PNA receptor, (c) PNA-DNA duplex formation [88].

This sensor is fabricated by the pick-and-place approach. The p-type SiNWs were synthesized using a gold cluster catalyzed CVD method. The average diameter of the SiNWs is 20 nm. Electrical contacts were made to nanowire ends using Electron Beam Lithography followed by Ti/Au (50/50 nm) metallization.

The hybridization mechanism is the property of single strand peptide nucleic acid (PNA) to recognize its complementary strand deoxyribonucleic acid (DNA). The PNA probe is chosen as a recognition sequence because it has great affinity and stability to bind to mutant DNA sequences [89]. The PNA receptor coat was firstly immobilized on the surface of nanowire (figure 40-(b)). When the PNA probes and DNA targets are complementary, the molecular hybridization occurs and the negative charges brought by phosphate groups of DNA strand are adsorbed on the nanowire surface (figure 40-(c)). As a result, the cross-sectional conduction of the nanowire is affected, and a variation of conductance of this sensor can be observed in figure 41-(a). The figure 41-(b) has shown a capacity of detecting concentration as low as 10 femto-molar (fM) DNA.

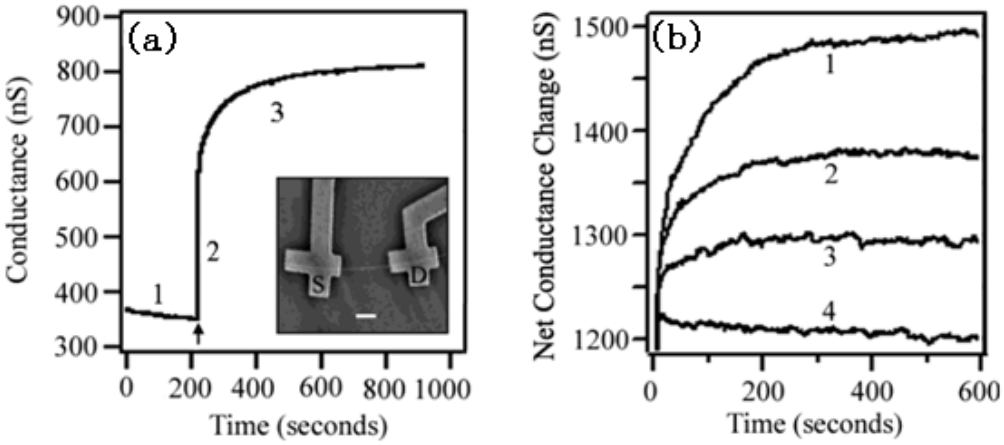


Figure 41: (a) Real-time conductance response from a SiNW device functionalized with PNA receptor. The arrow marks the point in time when the 60 fM DNA sample was added. The inset shows a SEM image of a typical SiNW device with source (S) and a drain (D) indicated; scale bar is 1 μm, (b) Net conductance changes versus time for 100 fM (1), 30 fM (2), 10 fM (3) and 1 fM (4) DNA samples [88].

Such feature with high sensitivity detection of charged carriers via binding a charged bio-molecule at the surface of a modified SiNW (coated by a layer of receptor materials) can also be used for detection of cancer markers protein and virus particles by antibody-modified SiNW FET sensors [90, 91]. The schematics of these two sensors are shown in figures 42 and 43. It suggests also great potential of nanowire sensors for drug discovery via detection of adenosine triphosphate and the drug Gleevec by tyrosine kinase linked nanowire [92].

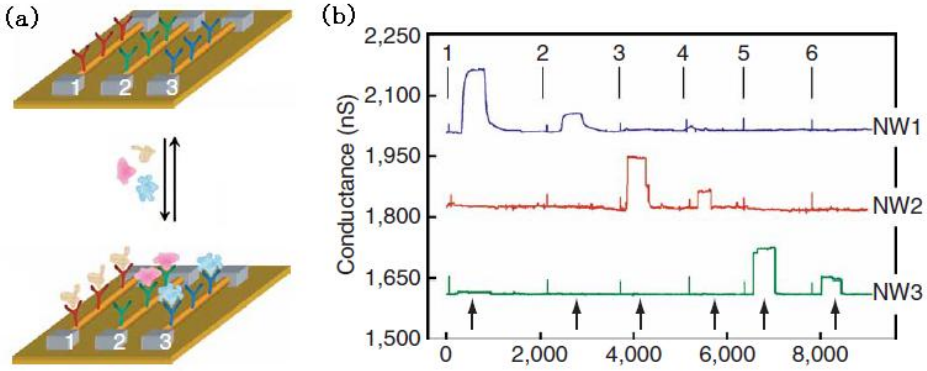


Figure 42: (a) A schematic illustrating multiplexed protein detection by three silicon nanowire devices in an array, (b) conductance response for three different cancer markers [90].

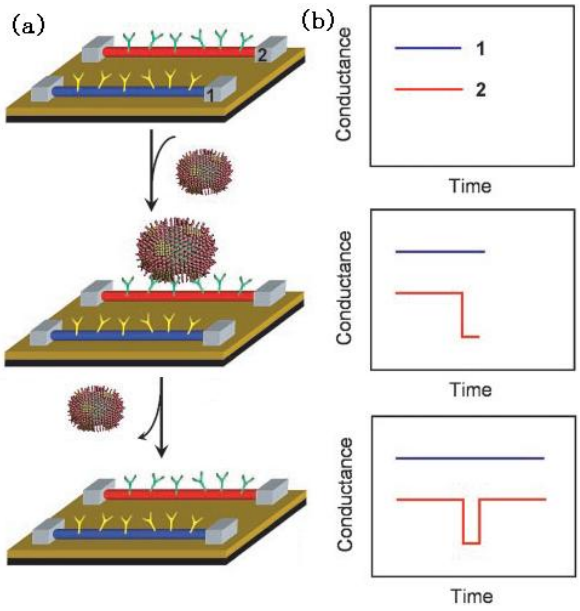


Figure 43: (a) Schematic shows two nanowire devices, 1 and 2, where the nanowires are modified with different antibody receptors, (b) conductance responses to the surface charge when a single virus is bind or unbind to the receptors on nanowire 2 [91].

# IV Conclusion

In this chapter, we have presented sensor devices based on SiNWs which have mechanical, chemical and biological applications, comparing with SGFET, ISFET and their respective applications as gas and pH sensor. Thanks to the nanostructure and the giant piezoresistance, SiNW mechanical sensor has shown a good performance over bulk silicon sensor. For the chemical and biological sensors, the large surface-to-volume ratio enables SiNWs sensors to have promising performances. The mechanism of such sensors is explained in two main theories, which are charge exchanging effect and chemical gating effect. The charge exchanging effect is that there are direct charges exchange between the adsorbed molecules and the SiNWs. The chemical gating effect is considered to shift the Fermi level of the SiNWs to change the conducting property. Both of these two theories are commonly accepted, but no researchers could say which one is dominant. However, it is admitted that silicon nanowire is a potentially good candidate for gas sensing application which warrants further exploration.

One of the main research subjects of the DM2-IETR, is the synthesis and the applications of SiNWs in the field of electronic devices for gas or biochemical sensors. Such devices based on SiNWs will be presented in the following chapter.

# Chapter III

# VLS silicon nanowires devices fabrication and related techniques

# I Introduction

The purpose of this chapter is to introduce the processing technologies for two kinds of devices based on VLS SiNWs, i.e., the inter-digital comb-shaped structure and the V-shaped groove structure, in the DM2-IETR.

In the first part of this chapter, the main materials and related techniques used in the manufacturing process will be presented. A brief description of the methods for obtaining each material and their characteristics will be given.

Then, the standard procedures of fabrication for both inter-digital comb-shaped structure and the V-shaped groove structure will be detailed.

In the end of this chapter, the technical problems for the V-shaped groove structure, such as the spin-coating problem and a photolithography precision problem will be described thoroughly.

# II Materials and related techniques used for realization of SiNWs devices

## II.1 Silicon dioxide via thermal oxidation

The silicon dioxide is mostly used as a barrier layer against diffusion at the substrate-silicon interface and as gate insulator. The thermal oxide should be realized at a very high temperature (> 1000 °C). When the surface of the silicon layer is exposed to an oxidizing atmosphere, the oxygen molecules will be absorbed and react with the silicon. Then the silicon dioxide and a $Si/SiO_2$ interface will be formed at the same time. With the continuous supply of oxygen, the oxygen molecules will pass through $SiO_2$ to react with the silicon underneath the interface $Si/SiO_2$ which has such an effect that the interface will displace deeper inside the wafer.

This type of oxidation can be carried out under dry atmosphere or under wet atmosphere. The oxidation rate under wet atmosphere is much higher than under dry atmosphere. The thickness of the silicon dioxide can reach at 70 nm under dry atmosphere

(1059 °C for 30 minutes) and at 1.2 µm under wet atmosphere (1175 °C for 90 minutes) [93]. However, the quality of the silicon dioxide produced by dry oxidation is better than that obtained by wet oxidation. The active interface of the dry oxidation has fewer defects, and the insulation characteristic is better. Therefore, during our studies, the dry oxidation is often used as gate oxide and the wet oxidation is used as hard mask for bulk wet etching of silicon using Tetra-Methyl Ammonium Hydroxide (TMAH) which will be introduced later [94].

## II.2 Polycrystalline silicon

Solids can exist in two extreme forms: the crystalline or the amorphous form. In the crystalline form, the atoms are arranged in a periodic array, i.e., there is long range order in the system. In the amorphous form, the atoms are arranged randomly, i.e., there is no long range order. Between these two forms, we can imagine that there is the third intermediate form with short or medium range order, or mixed phases consisting of several of these states. On this basis, we can define the solid-state silicon in three types: the monocrystalline silicon, the amorphous silicon and the polycrystalline silicon.

The monocrystalline silicon is characterized by an arrangement of the silicon atoms in an ideal crystal according to the diamond structure. The amorphous silicon consists of random stack of silicon atoms, whose atomic order is limited to short range order only. As we have mentioned, the polycrystalline silicon is the intermediate form between these two extreme forms. Particularly, it can exist the phases consisting of both crystalline form and amorphous form. We can define the polycrystalline silicon as consisting of monocrystalline grains separated by disordered areas rich in crystal defects. This disordered area seems like the amorphous silicon and we can call it the grain boundary. Each of these two components of polycrystalline silicon, grains and grain boundaries, has features that we briefly recall:

- The grain can be defined by its size and its crystalline quality. In fact, we can find out that the real process for obtaining silicon by CVD does not permit depositing high-quality crystalline silicon which is free of defects. The density of the defects will determine the quality of the grain.

- The essential characteristics of the grain boundary are its dimensions, ie., its thickness and its defect density.

Talking about a unique type of polycrystalline silicon would be a mistake and that is why it is always necessary to define the polycrystalline silicon according to certain criteria that can be summarized as follows:

- Texture and grain size.
- Densities of intragranular defects and intergranular defects.
- Ratio of the crystalline volume to the amorphous volume.
- Porosity.

## II.2.1 The principle of the LPCVD method

Among the deposition techniques of thin film silicon, the most common technique today in the microelectronics industry is the LPCVD, which is also one of the most important synthesis methods for VLS silicon nanowires. The LPCVD technique presents at least two essential advantages. Thanks to the low working pressure, it provides good uniformity (the variations are obtained routinely less than 5%) in both axial and radial directions, even when a dopant gas is injected for an *in-situ* doping (except the diborane for p-type doping. The reason will be presented in the following section). On the other hand, the fact that the low flow rate is used and a large number of large area substrates can be used with uniform deposition in a same deposition period, reduce the manufacturing cost, which makes it very attractive from the industrial point of view.

A simplified diagram of the LPCVD reactor used in the laboratory is shown in figure 44. It is a horizontal tubular reactor with hot wall constituted with a quartz tube. A heating resistor consisting of three independent heating elements is placed around the tube and regulated by the thermocouples. An introducing chamber is located in the front of the furnace, which permits to isolate the reactor from the atmosphere of the room permanently. The vacuum established in the deposition chamber is never broken, resulting in a lower pollution levels. To obtain a good vacuum of about $3.10^{-5}$ Pa in the reactor, a primary pump coupled to a secondary turbo-molecular pump is required. A gas distribution system allows using several gaseous precursors simultaneously ($SiH_4$, $PH_3$, $N_2$, He and $B_2H_6$).

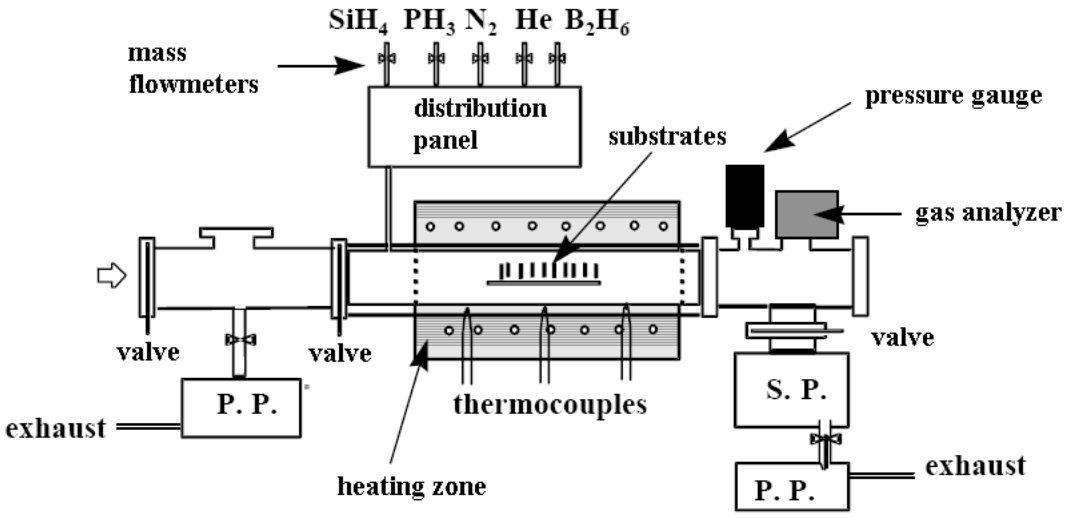


Figure 44: A schematics of the reactor of LPCVD.

Several research topics have been conducted on the mechanisms for deposition of silicon by LPCVD process. Two basic types of chemical reactions are to be considered. On the one hand, the reactions involved in the gas phase, are termed homogeneous. On the other hand, the reactions, which occur in the substrate surface, are referred to heterogeneous. These reactions are governed by different kinetics, which will depend on the deposition conditions, especially temperature, gas pressure and flow.

The overall reaction of silicon deposition from silane is:

$$SiH_{4g} \longrightarrow Si_s + 2H_2$$

For the gas-phase reactions, several cases should be considered. At the usual operating temperature (about 550 °C), the silane decomposes pyrolitically to release silylene according to the reaction formula:

$$SiH_4 \longleftrightarrow SiH_2 + H_2$$

It follows the chain reactions to produce higher order of silanes.

$$SiH_2 + Si_nH_{2n+2} \longleftrightarrow Si_{n+1}H_{2n+4}$$

The reaction involved in the LPCVD reactor decomposes the silane into silicon atoms, which will contribute to the growth. As we have noted earlier, these reactions are balanced by the temperature, pressure and gas flow. The results reported in the literature vary widely because of explorations in different experimental conditions.

## II.2.2 Thin film polycrystalline silicon deposited by LPCVD

The purpose of the studies on the polycrystalline silicon is to obtain the material with best electrical properties, i.e., whose characteristics are as close as possible to those of monocrystalline silicon. The silicon deposited by LPCVD has a "crystal" structure after deposition, which can range from amorphous state to polycrystalline state. The crystalline nature of the films deposited from silane has been studied for a long time depending on the conditions of pressure and temperature. P. Joubert [95] has summarized numerous studies and displayed the changes in the structure of the silicon layers as a function of pressure and deposition temperature (Figure 45). We can observe that for a given deposition temperature, there is a pressure below which the material is deposited in a crystalline state and beyond which it is deposited in an amorphous state. T. Kretz [96] has also concluded that the polycrystalline silicon obtained by solid phase crystallization from amorphous silicon has much bigger grains than that obtained by direct crystallized polysilicon deposition. As previously observed [97], the work performed in our laboratory has also confirmed that polycrystalline silicon obtained by crystallization from amorphous silicon has better electrical properties than as-deposited silicon.

Following these previous studies, the growth conditions of the thin film polycrystalline silicon used in our lab are set at 550 °C and 90 Pa, where silicon is deposited in the amorphous state, and then crystallized by a thermal annealing under vacuum at 600°C during 12 hours. In this case, the crystallization process provides enough energy to the atoms of the deposited layer so that they can be arranged according to the crystal lattice of silicon, which transforms the deposited silicon layer from the metastable amorphous state to the stable crystalline state.

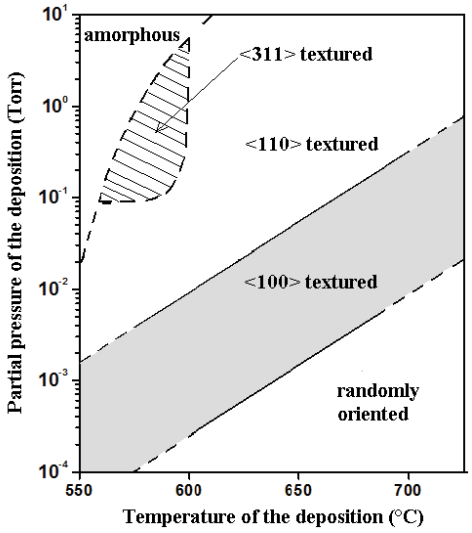


Figure 45: A diagram of pressure-temperature for silicon layers deposited by LPCVD using silane as precursor [95].

## II.2.3 Polycrystalline silicon nanowires synthesized via VLS using LPCVD

As we have presented in chapter 1, the most popular technique we use today to synthesize silicon nanowires via VLS mechanism is Chemical Vapor Deposition. Moreover, the rich experiences accumulated by the DM2-IETR in using LPCVD during the last twenty years enable to realize the silicon nanowire growth via VLS technique.

In our process, silane is used as the precursor gas and the metal catalytic film is gold. When the gold nano-clusters are heated above the Au-Si alloy eutectic temperature (363 °C), the liquid gold droplets will form on the substrate surface. The silane molecules will crack on the surface of the gold droplets and meanwhile the silicon source decomposed silane will be incorporated into the droplets. The sufficient Si incorporation results in the supersaturation of the alloy droplets which leads to a nucleation of the solid silicon. The continuation of this process realizes the synthesis of SiNWs. A VLS silicon nanowire with a gold alloy on the top is shown in the figure 46, which has a 150-nm-diam. In fact, the diameter of the nanowire synthesized by VLS depends on the initial size of the gold droplet. The condition of the growth is set to 40 Pa and 460 °C, which insures a proper growth rate and avoids amorphous silicon deposition on areas uncovered with gold droplets. For example, the length of the

nanowire can exceed 20 µm by means of controlling the growth duration (2 hours). However, in some cases the length depends also on the thickness of the gold film.

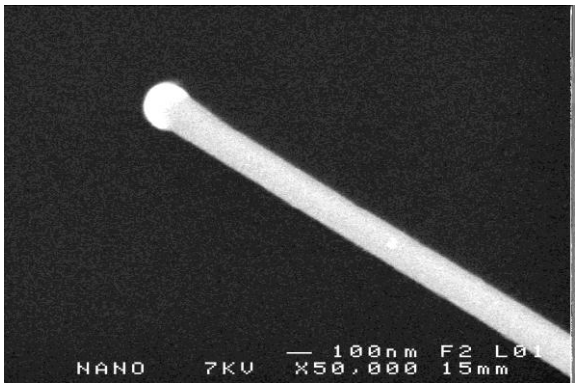


Figure 46: An SEM photo of a single VLS silicon nanowire whose growth conditions are 40 Pa and 460°C.

## II.3 The *in-situ* doping for polycrystalline silicon

The *in-situ* doping using LPCVD consists in injecting a dopant gas into the reactor together with the precursor gas (silane).

### II.3.1 *In-situ* doping for silicon thin film

The most commonly used gas for the N-type doping is phosphine ($PH_3$), which is injected with the silane under normal conditions of temperature (550 °C – 650 °C) for thin film deposition of polycrystalline silicon. According to previous studies [98-100], the gaseous $PH_3$ molecules will be adsorbed and then decomposed on the surface following the reactions below:

$$PH_{3g} \longrightarrow PH_{3s}$$

$$PH_{3s} \longrightarrow P_s + \frac{3}{2}H_2$$

Most of the literatures about P-type *in-situ* doping for polycrystalline silicon report the use of diborane $B_2H_6$ as dopant gas. Sanganeria et al [101], studying the $Si_2H_6$-$H_2$-$B_2H_6$

system, have come to the conclusion that the doping is effected by adsorption of $BH_3$ following:

$$B_2H_{6g} \longrightarrow 2BH_{3g} \longrightarrow 2BH_{3s}$$

$$BH_{3s} \longrightarrow B + \frac{3}{2}H_2$$

The doping level is defined by the molecular ratio Γ:

$$\Gamma = \frac{flow\ of\ dopant\ gas}{flow\ of\ reactive\ gas} = \frac{\Phi_{dopant}}{\Phi_{reactive\ gas}}$$

The previous work conducted in the DM2-IETR [102] has shown that it is possible to achieve the N-type doping range from $10^{16}$ at.cm$^{-3}$ to $2.10^{20}$ at.cm$^{-3}$ and the P-type *in-situ* doping range from $10^{16}$ at.cm$^{-3}$ to $5.10^{19}$ at.cm$^{-3}$ by means of control the molecular ratio Γ.

In this thesis, only the most heavily doped polycrystalline silicon is required to act as conducting electrodes.

## II.3.2 *In-situ* doping for VLS silicon nanowires

The doping process for VLS SiNWs follows the same principle of *in-situ* doping for the silicon thin film using phosphine and diborane as dopant gas for N-type and P-type doping, respectively, except that the normal condition temperature is set at 460 °C. The doping level is also defined by the molecular ratio Γ. An appropriate selection of the LPCVD parameters (pressure and temperature) can avoid silicon deposition on areas uncovered with Au droplets.

When the phosphine is injected into the reactor at the same time with the silane, the decomposed phosphorus molecules will be incorporated into the Au-Si droplet as well as the decomposed silicon source. Such effect will last for the whole growth process of the silicon nanowires, which realizes the N-type *in-situ* doping for VLS silicon nanowires.

We have achieved the N-type doping range from $2.10^{16}$ at.cm$^{-3}$ to $2.10^{20}$ at.cm$^{-3}$. However, the P-type doping control failed. We suggest that a thin film of doped amorphous silicon should be deposited during the growth process on the whole surface of the substrate

(figure 47), which means the synthesized silicon nanowires will have a parallel connection with this doped film (short circuit effect). It is because the dissociation energy of silane changes from 238 kJ/mol without diborane to 84 kJ/mol with diborane [103, 104]. So far we haven't found a solution to solve this problem as we have only diborane as dopant gas for p-type doping.

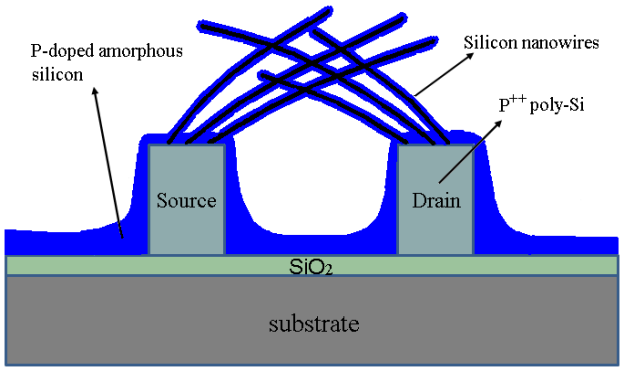


Figure 47: A cross-sectional schematic of a resistance based on P-doped SiNWs.

The details about the doping effect and the electrical properties for N-type doping will be presented in the chapter 4.

## II.4 Etching methods

Etching, as an indispensable step of the photolithography, plays an important role during our processes. As we all know, the etching methods fall into two categories according to the state of the etchant: dry etching and wet etching. They are used mainly for shaping, polishing, cleaning … In the part of our studies, a typical dry etching method, reactive ion etching (RIE), and a wet etching using TMAH etchant are used.

### II.4.1 Dry etching RIE

RIE is an etching technique using reactive ion plasma which involves both physical effect and chemical effect: the ion bombardment by mechanical impact and chemical attack in the vapor phase from fluorinated gases (etching materials based on silicon) or chlorinated gases (etching metals). The physical effect results in an anisotropic etching profile while the chemical effect leads to an isotropic etching profile. It means that the etching rate could be

controlled and a certain ratio of vertical sidewall could be obtained by adjusting the power of the plasma, the pressure and the gas flow. $SF_6$ is used as etchant in our laboratory.

## II.4.2 Wet etching in TMAH

Tetra-methyl ammonium hydroxide (TMAH) is a typical etchant for anisotropic wet etching which is alkali hydroxide base. Compared with dry etching, the wet etching of silicon in TMAH provides a much faster etching rate and a higher degree of selectivity. The reaction formula is the following:

$$Si + 2OH^- + 2H_2O \longrightarrow Si(OH)_2^{2-} + 2H_2$$

The silicon atoms are firstly oxidized by $OH^-$ and then removed from the substrate. If we change the concentration of $OH^-$, the etching rate could be adjusted. The etching rate of the TMAH solution used in our laboratory is about 0.8 µm/min.

The selectivity of the anisotropic wet etching is achieved by the difference of etching rate in each crystallographic direction which means that the etching rate is much faster in certain direction ((100) plane) than in others ((111) plane). To better understand the selectivity, the etching rate dependence on orientation should be explained by the crystal structure of silicon (figure 48).

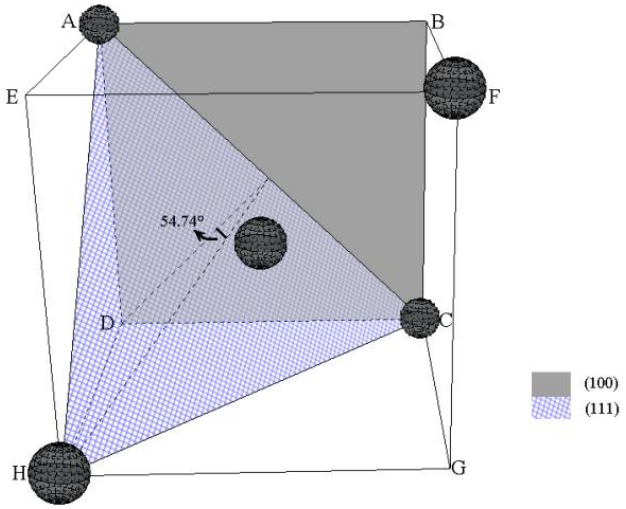


Figure 48: Crystal structure of silicon.

As we have observed in figure 48, the plane ABCD ((100) plane) makes an angle of 54.74° to the plane ACH ((111) plane). The wafers that we use are <100> oriented wafers whose surface is corresponding to the (100) plane. Figure 49 shows a diagram of a sample etched in TMAH with a square opening. When the sample is immersed in the TMAH solution, the (100) will be etched fast inside the wafer. However, the (111) plane which is the slowest etching crystal plane, will be exposed as etching time progresses. The (111) plane is just corresponding to the tilted sidewall of the structure in figure 49. If the etching time is short, a small square ((100) plane) will be left at the bottom. If the etching time is long enough, an inverted pyramid structure can be created.

This anisotropic wet etching method helps us to realize a V-shaped groove upon where we will fabricate devices based on VLS silicon nanowires.

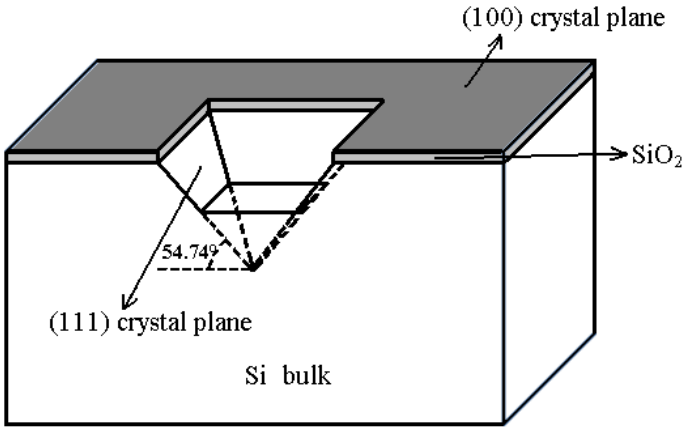


Figure 49: A diagram for TMAH etching.

## II.5 Evaporation system for deposition of thin film gold catalyst

Before the synthesis of SiNWs by VLS method, a thin film of gold (< 5 nm) is deposited on the substrate via thermal evaporation system, which will be used as metal catalyst. The deposition is carried out in vapor phase in a chamber whose pressure is controlled at $10^{-6}$ mbar level. When the current between the ends of the filament is loaded to a high level, the gold wires around the filament is evaporated and deposited on surfaces of the substrates. It should be noticed that the current must be adjusted slowly enough in order to get such a uniformly thin film of gold. The thickness of the gold is detected by a quartz oscillator.

## II.6 Lift-off technique

Lift-off technique is a method to pattern a target material on the surface of a substrate using a sacrificial layer. The dimension of the structure to be defined can achieve to nanoscale. The main steps of this technique are illustrated as following:

1) A sacrificial layer (for example: photoresist) is deposited and an inverse pattern is created on the surface of the substrate by photolithography (figure 50-(a)).

2) A thin film of target material is deposited over the whole sample. In the opening region where the substrate is uncovered by the sacrificial layer, the target material succeeds reaching the surface of the substrate (figure 50-(b)).

3) The sacrificial layer is removed by a solvent meanwhile the target material on the sacrificial layer is washed away. The target material having a direct contact with the substrate will be remained which creates the final pattern (figure 50-(c)).

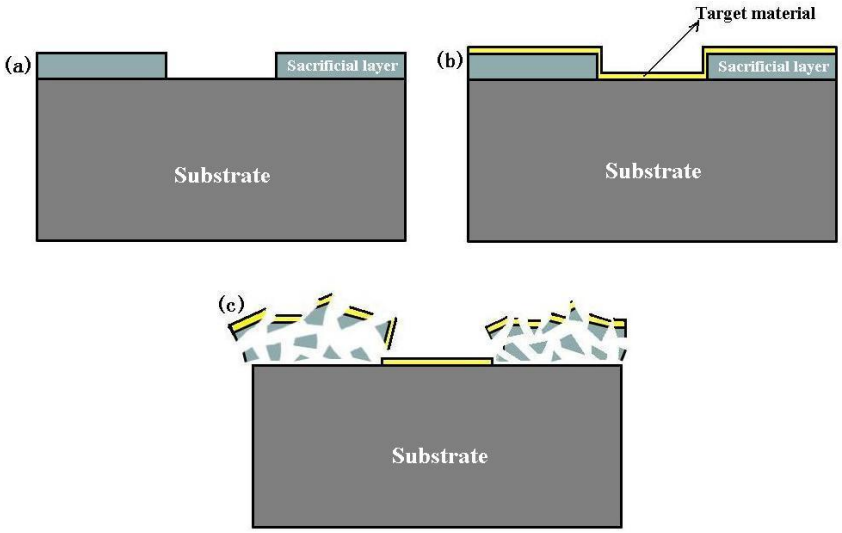


Figure 50: Schematics of the lift-off technique, (a) patterning of the sacrificial layer, (b) deposition of target material, (c) removal of the sacrificial layer and part of target material.

In our studies, the sacrificial layer used is photoresist UV210 and the target material is a thin film of gold whose thickness is less than 5 nm. This method helps us to define the precise locations where should be covered by thin film of gold.

# III Realization of inter-digital comb-shaped devices based on VLS SiNWs

As we have mentioned before, the objective of our research is to realize silicon nanowires based devices and study their potential applications as chemical sensors with high sensitivity. The geometry of the phosphorus heavily *in-situ* doped polysilicon inter-digital comb-shaped structures (also used as electrodes) will increase the possibility of interconnection for silicon nanowires. The tangled Au-catalyst VLS SiNWs will increase the exchanging surface between the active layer (surface of the SiNWs) and the ambient environment which plays a decisive role for the sensitivity. In the following section, we will discuss in detail the steps of fabricating inter-digital comb-shaped devices.

## III.1 choice of substrates

Two kinds of N-type (phosphorus-doped) silicon <100> oriented wafers are used in this chapter whose dimensions are 2-inch and 255-305 μm thick. The resistivity of these two kinds of substrates is guaranteed by the supplier at 1-10 mΩ.cm and 0.001-0.1 mΩ.cm respectively. The former is used to fabricate a resistor based on SiNWs and the latter heavily doped substrate is used to realize a transistor based on SiNWs. The difference between these two devices is that the heavily doped substrate will act as a gate electrode.

## III.2 Procedure of fabrication

The fabrication process of the inter-digital comb-shaped SiNWs based devices includes 2 photolithographic steps. Before any technological steps, a standard RCA cleaning is carried out to remove organic and metal compounds on the surface of silicon wafer. After RCA cleaning, a dry thermal oxidation is realized to insulate the substrate (silicon wafer), which functions also as a gate oxide (70 nm). Then, a heavily phosphorus *in-situ* doped amorphous silicon layer is deposited by LPCVD at 550°C and 90 Pa. Subsequent solid phase crystallization is performed at 600°C under vacuum to activate dopants and leads to the formation of a polycrystalline silicon film. This film is then patterned (by photolithography 1) and dry etched to define the geometry of the comb-shaped electrodes (inter-digital structure

shown in Figure 51-(a)). Here, the dry etching RIE is carried out by the machine NEXTRAL NE 110 to shape inter-digital comb electrodes. The sample is placed into a low pressure chamber (30 mTorr). 5 sccm sulfur hexafluoride ($SF_6$) is driven into the chamber under the plasma phase. The power of the plasma is set at 30 watts. In such condition, the physical effect is predominant so that the lateral etching is relatively weak and the profile is close to vertical. The Au thin film is deposited by thermal evaporation and locally removed using a lift-off technique in order to define precise locations (by photolithography 2) for silicon nanowires synthesis (Figure 51-(b)). Finally, SiNWs are grown in a hot wall LPCVD reactor using silane as precursor gas. Deposition temperature and pressure are respectively 460°C and 40 Pa. This synthesis results in a tangled growth of SiNWs insuring electrical contact between the two doped electrodes (Figure 51-(c)). Different inter-digital structures can be achieved by varying number of teeth and the space between the teeth, which will be introduced in detail in the chapter 4. This fabrication process can be achieved either on silicon wafer or on other substrate (glass) compatible with the maximum process temperature (600°C).

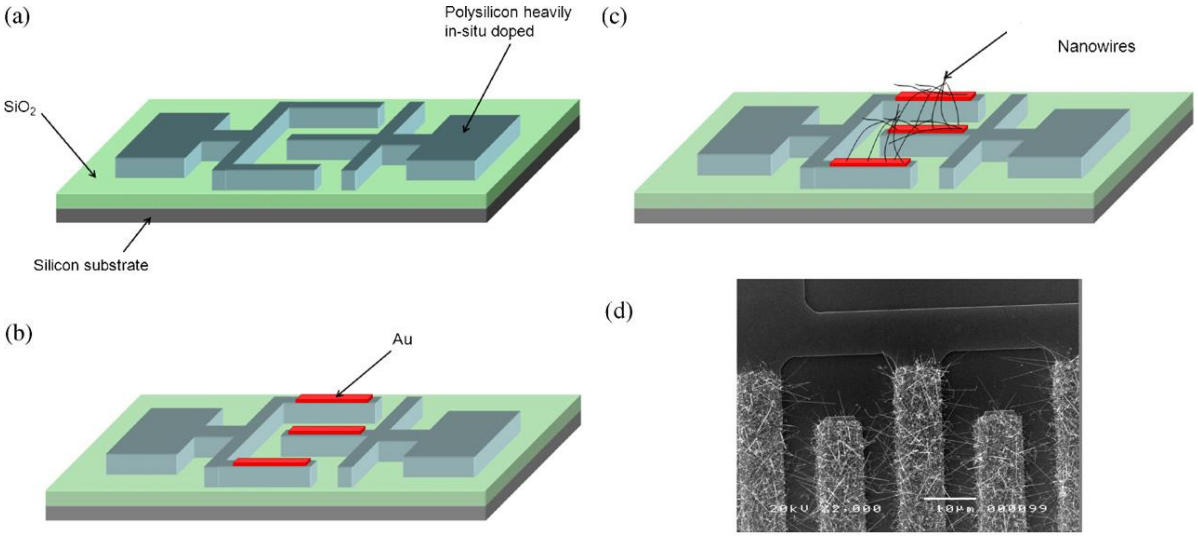


Figure 51: Key device fabrication steps of the inter-digital comb-shaped devices based on VLS SiNWs, a) definition of the comb-shaped electrodes geometry on a $SiO_2$ capped substrate, b) thin film Au local deposition after lift-off technique, c) growth of SiNWs by LPCVD, d) SEM top view observation of VLS SiNWs based device.

It should be noticed that the oxide on the back side of the wafer should be removed after the dry oxidation if a heavily doped substrate is used as back gate to realize a transistor. Otherwise, the back gate will be covered by silicon oxide and isolated.

# IV Realization of V-shaped groove devices based on VLS SiNWs

Beside the inter-digital comb-shaped device, another V-shaped groove device based on VLS SiNWs is also realized to study the potential applications as chemical sensors with high sensitivity. The unique feature of this structure is its V-shaped groove in which the VLS SiNWs are synthesized. The advantage of this structure is that the etched groove channel can confine the analytes (especially for the liquid-state analytes) and ensure all the exchanging reactions taking place inside the groove. The details about the procedure will be discussed in the following sections.

## IV.1 choice of substrates

The same kind of <100> oriented silicon wafers are used for realization of V-shaped groove devices based on VLS SiNWs. Here, the orientation of the wafers is so important for this process because the TMAH etchant for anisotropic wet etching will directly determine whether we can realize the V-shaped groove.

## IV.2 Procedure of fabrication

The principle of the anisotropic wet etching using TMAH has already been explained previously. Here, we present the practical operating steps in detail.

Firstly, the <100> oriented silicon wafer is capped with a 1-µm-thick $SiO_2$ by wet oxidation. After the first photolithography procedure, an opening is created on the $SiO_2$ which acts as a hard mask (figure 52-(a)). The $SiO_2$ layer in the backside prevents the wafer being etched during the wet etching. The normal experimental condition for the anisotropic etching used in our laboratory is 50% TMAH at 80°C, which determines the etching rate of (100) plane at about 0.8 µm/min. Although the etching rate is known, it is still hard to estimate the accurate etching time, because the etching rate is hard to keep constant during the whole processing time. To confirm the etching state and avoid the over etching, we can observe the (100) plane inside the groove through the optical microscope in the last few minutes of the estimated time (figure 52-(b)). When the plane disappears, it means that the groove is etched

to the end (figure 52-(c)). Finally, another wet etching (HF) is carried out to remove the $SiO_2$ layers on both sides of the substrates and then the V-shaped groove is realized (figure 52-(d)).

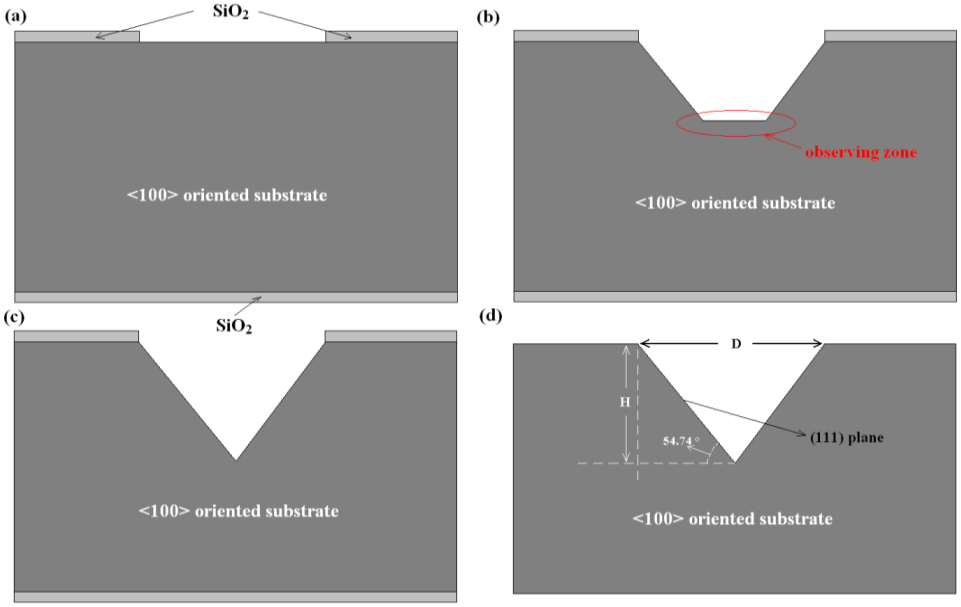


Figure 52: Schematics of wet etching by TMAH, (a) creating an opening on $SiO_2$ layer, (b) partial etching structure, (c) V-shaped groove at the end of etching, (d) final structure after removal of the $SiO_2$.

As we know that the (111) plane makes an angle of 54.74° to the (100) plane (figure 52-(d)), the relationship between the depth (H) and the width (D) can be found out as following formula:

$$H = \frac{D}{2} \times \tan 54.74° \tag{7}$$

According to this formula, we can calculate the depth of the V-shaped groove.

The following procedure of the fabrication is almost the same as that of the inter-digital comb-shaped structure. After the RCA cleaning, the substrate with V-shaped groove is covered by a layer of $SiO_2$ and a layer of heavily doped polycrystalline silicon successively. Then, the polysilicon film is patterned (photolithography 2) and dry etched to define the geometry of the electrodes (figure 53-(a)). Au thin film is then deposited and locally removed using a lift-off technique in order to define precise locations (photolithography 3) for silicon

nanowires synthesis (figure 53-(b)). Finally, SiNWs are grown to link together the two electrodes on the slopes of the V-shaped groove (figure 53-(c)).

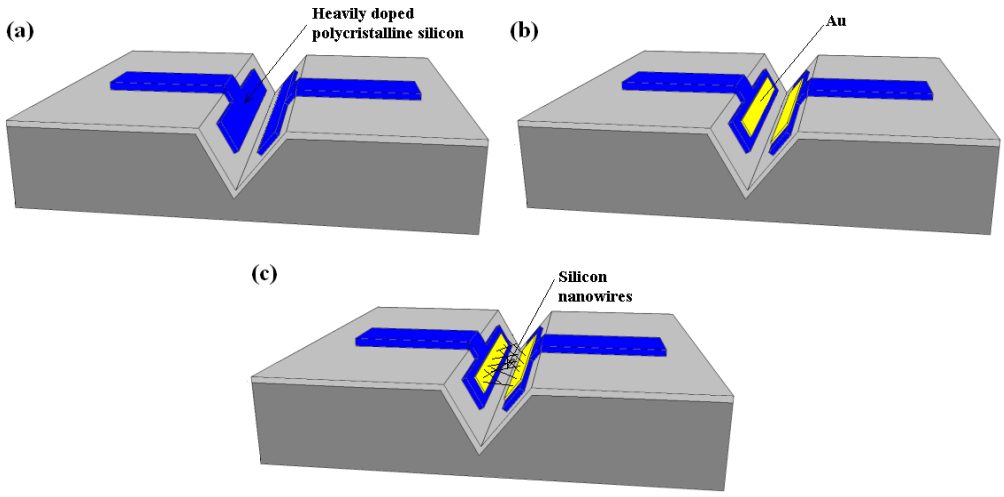


Figure 53: Key fabrication steps of the V-shaped groove devices based on VLS SiNWs, (a) definition of the electrodes on a $SiO_2$ capped substrate with V-shaped groove, b) thin film Au local deposition after lift-off technique, c) growth of SiNWs by LPCVD.

## IV.3 Technical problems for V-shaped groove devices based on VLS SiNWs

### IV.3.1 Spin-coating problem for V-shaped groove devices

During the process, there is a spin-coating problem which hinders the realization of V-shaped groove devices. Because of the difference in height (depth) for the V-shaped groove structure, the risk of spin-coating the photoresist non-uniformly is possible. Three V-shaped grooves with different dimensions, coated by photoresist after development, are shown in the figure 54. Although a specific spin-coating procedure (the classical and the specific spin-coating procedures are illustrated in the annex 1) is performed to ensure proper adhesion of the photoresist to the surface, we can observe that for the groove whose width is equal or larger than 20 µm, no photoresist can protect the zone 1 on the grooves (figure 54 (b-c)) and for the groove whose width is 30 µm, the undeveloped photoresist is left at the bottom of the

cavity in zone 2 (figure 54 (c)). Since the depth of the 30-µm-wide groove is too deep to achieve a good coating of photoresist, we abandoned it and concentrated in optimizing the other smaller grooves (with widths of 10 µm and 20 µm).

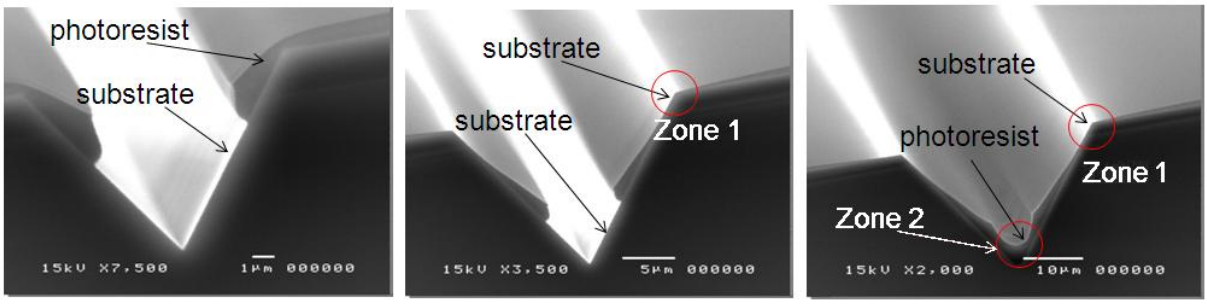


Figure 54: SEM observations of the coating states on the V-shaped groove after development step, (a) a 10 µm width V-shaped groove, (b) a 20 µm width V-shaped groove, (c) a 30 µm width V-shaped groove.

After synthesis of the SiNWs, the SEM photos have been taken again to observe the surface state of the V-shaped groove structural devices (figure 55). We can observe that the electrodes on the 10 µm width groove are continuous (figure 55-(a)) while the electrodes on the 20 µm width groove are cut off (figure 55-(b)). It is because there is no photoresist which covers the zone 1 of the V-shaped groove, thus the heavily doped polysilicon electrodes on the zone 1 was exposed and etched by RIE.

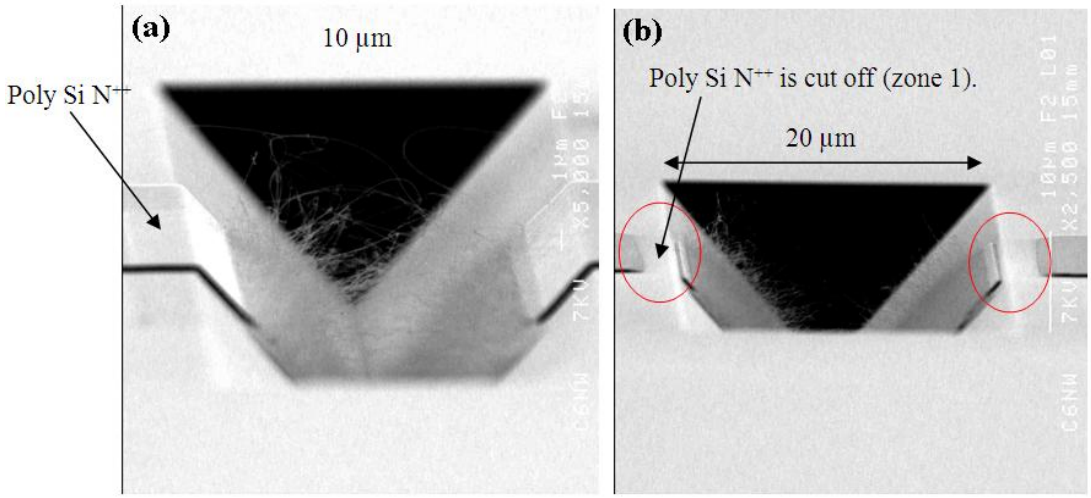


Figure 55: SEM photos of V-shaped groove SiNWs samples, (a) a 10 µm width sample, (b) a 20 µm width sample.

In fact, we can stop TMAH etching prematurely to allow the presence of the flat bottom in the groove (see figure 56). This can decrease the difference in height for the V-shaped groove and improve the spin-coating effect. The SEM photos of the 20 µm width sample after optimization procedure have been shown in figure 57 (c-d).

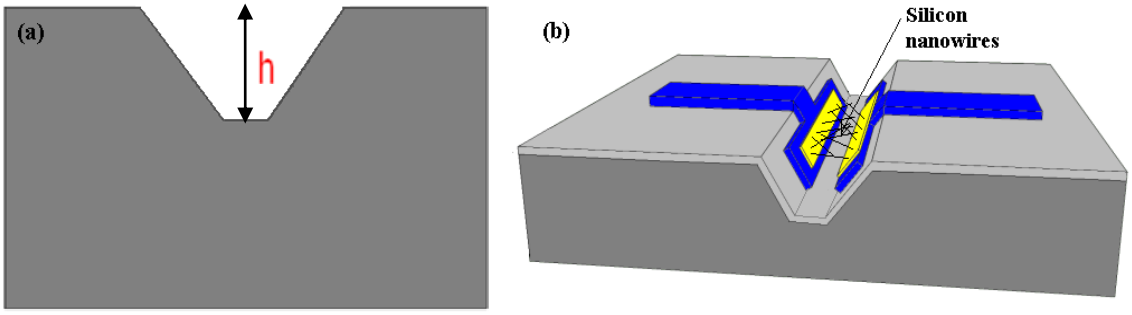


Figure 56: (a) A schematic of a silicon substrate etched by TMAH with a flat bottom (20-µm-wide), (b) a schematic of an optimized V-shaped groove SiNWs device (20-µm-wide sample) after growth of SiNWs.

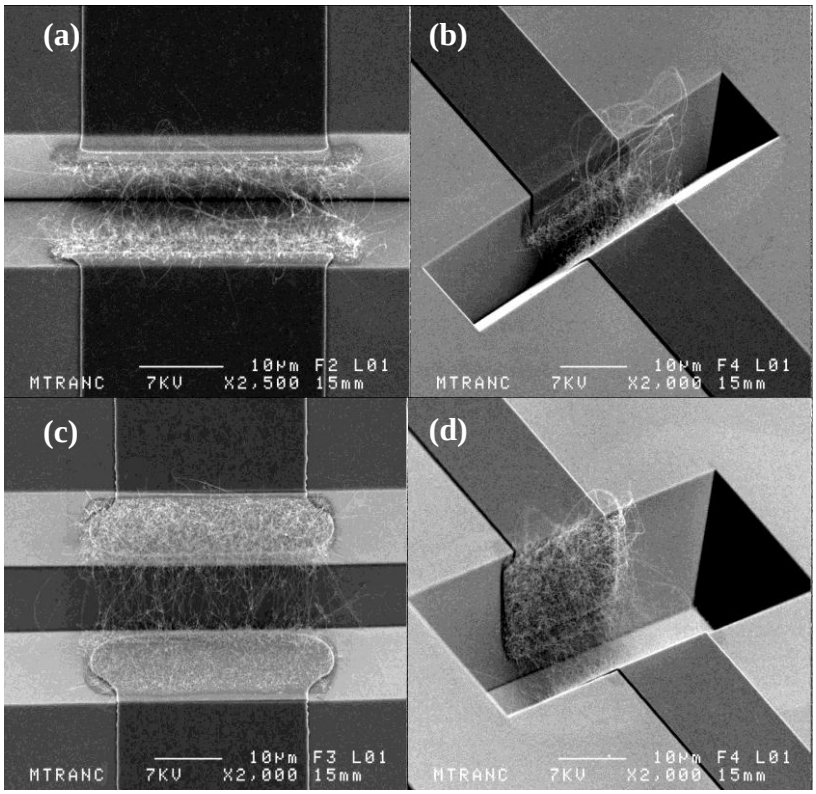


Figure 57: SEM top and 45° view observations of V-shaped groove VLS SiNWs based devices: (a-b) a 10 µm width sample, (c-d) a 20 µm width sample.

### IV.3.2 Photolithography precision problem for the V-shaped groove devices

The other problem for the V-shaped groove process is related to the photolithography precision. When the UV light illuminates through the opening of the mask, a very small deflexion angle appears, which expands the exposure region from designing width Wd to a real width Wr (figure 58). For example, a 10 µm width V-shaped groove, the Wd is 3 µm, but the Wr reaches 5 µm. This precision error is due to the large difference in height for the V-shaped groove. When the separation distance between the mask and the surface is smaller, the Wr will be closer to the Wd. Unfortunately, this precision error for heavily doped polysilicon and gold patterning could not be avoided.

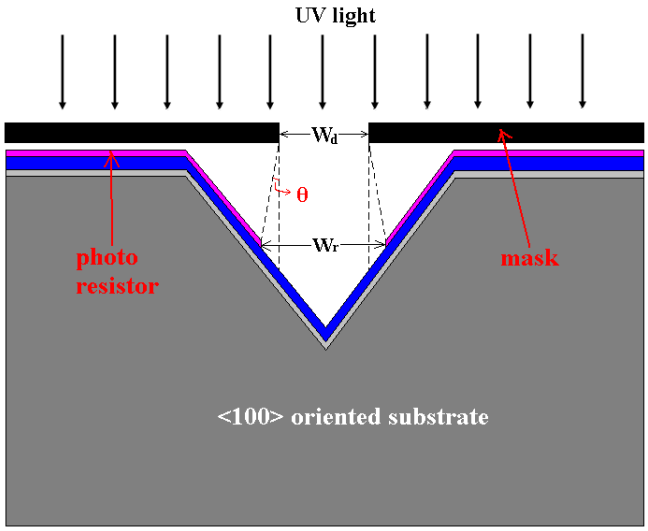


Figure 58: A schematic of simulating photolithography result on V-shaped groove.

## V Conclusion

This chapter aims to present the procedures of fabrication in details for the inter-digital comb-shaped and the V-shaped groove devices based on Au-catalyst SiNWs. For the inter-digital comb-shaped device, both of the geometry of the inter-digital comb-shaped structure and the tangled Au-catalyst VLS SiNWs can increase the exchanging surface between the active layer (surface of the SiNWs) and the ambient environment which enables to raise the sensitivity. The advantage of V-shaped groove devices is that the etched groove channel can lock the analytes (especially for the liquid-state analytes) and ensure all the exchanging reactions taken place inside the groove, which will highlight the sensing efficiency of the

nanowires inside the V-shaped groove. In addition, V-shaped groove offers the possibility to fabricate VLS SiNWs based devices in planar configurations.

The materials used and the related techniques have been also introduced, especially the VLS approach by LPCVD.

Three technical problems during the process, P-type doping problem for VLS SiNWs, spin-coating and photolithography precision problems for the V-shaped groove devices have been discussed, analyzed and solved, which will be necessary for the optimization of our devices based on VLS SiNWs.

# Chapter IV

# Electrical properties of VLS SiNWs and gas sensors applications

# I Introduction

In the third chapter, two different structural devices based on VLS SiNWs, inter-digital comb-shaped devices and V-shaped groove devices, have been introduced. In the first part of this chapter, we will study the electrical properties of the VLS SiNWs in terms of the inter-digital comb-shaped resistor. The current measurements as a function of temperature are carried out, which permit us to understand the electrical behaviors of VLS SiNWs and the effect of *in-situ* doping for VLS SiNWs.

In the second part, the silicon nanowires based resistors are electrically characterized as chemical sensors under exposure to ammonia and smoke to detect ambient charged species. Both qualitative (smoke) and quantitative ($NH_3$) measurements have been performed and their performances are discussed and analyzed in detail.

# II Electrical properties of the SiNWs based devices

The electrical characterizations of the nanowires are performed by measuring the inter-digital comb-shaped resistance based on silicon nanowires. Measurements of electrical current as a function of temperature and doping have been also carried out.

First of all, we should verify the ohmic behavior of the resistance by measuring current between -1 V and 1 V at room temperature. The measurements are carried out by using a probing tester and Agilent Technologies B1500A semiconductor device analyzer. The following schematic shows the assembly for the measurements (figure 59).

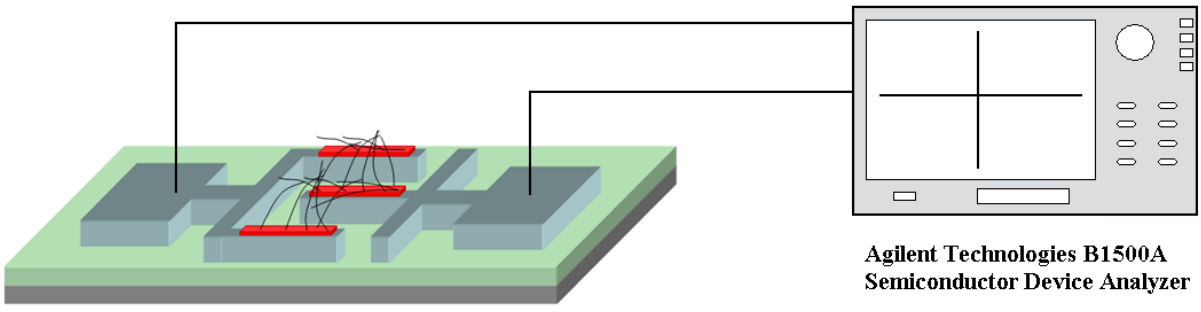


Figure 59: Schematic of I-V characterization for a resistor based on VLS SiNWs.

## II.1 Analysis of the growth duration for the SiNWs electrical properties

As we had no experiences about the growth of nanowires such as the growth rate and the quantity of Au catalyst should be deposited, a lot of trial growth tests have been carried out. The purpose of these tests is to synthesize silicon nanowires long enough by VLS method using Au catalyst nano-droplets to realize a tangled network on the inter-digital comb-shaped electrodes. Therefore, at the beginning of these tests we have deposited a 5-nm-thick gold layer on the substrate. Four different growth durations (10 min, 30 min, 1 hour and 2 hours) by LPCVD have been studied. Figure 60 shows SEM photos which illustrate the growth states of the SiNWs for different growth durations.

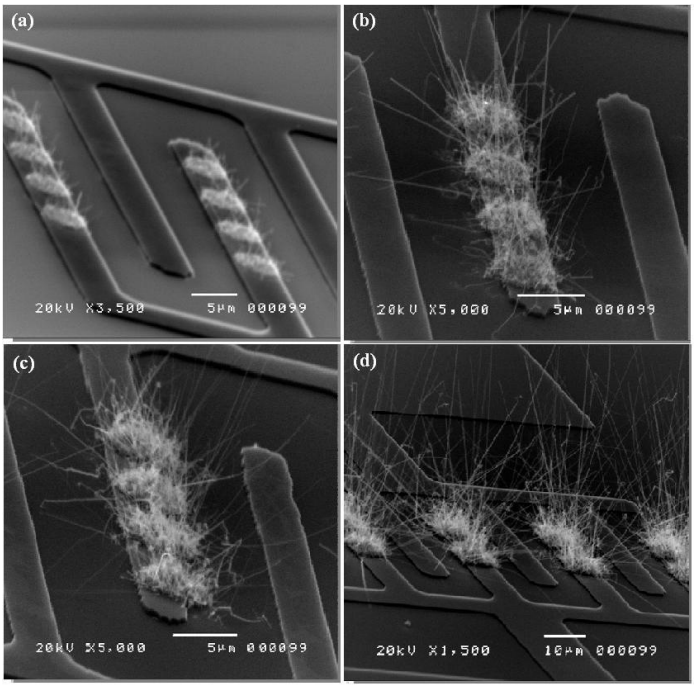


Figure 60: SEM photos of the VLS SiNWs growth state for different durations, (a) 10 min, (b) 30 min, (c) 1 hour, (d) 2 hours.

From the SEM photos, we can find the gold plots deposited on half teeth of the comb-shaped electrodes, which helps us to observe the orientation and the length of the VLS silicon nanowires more clearly. In fact, the orientation of the VLS nanowires cannot be controlled during our process. The randomly oriented nanowires synthesized from the gold plots look like tufts grass, which is strongly dependent of the heavily doped polysilicon texture. With

extension of the growth duration, the length and the density of the nanowires are increased accordingly. In figure 60-(d), we can see that the nanowires are dense enough and most of the nanowires can reach at least 10 µm. The space between two teeth does not exceed 10 µm. Therefore, it results in a tangled silicon nanowires network which insures the interconnection between the comb-shaped teeth. The real structure of the inter-digital comb-shaped resistance based on VLS SiNWs and a corresponding I-V characteristic for three growth durations are shown in figure 61.

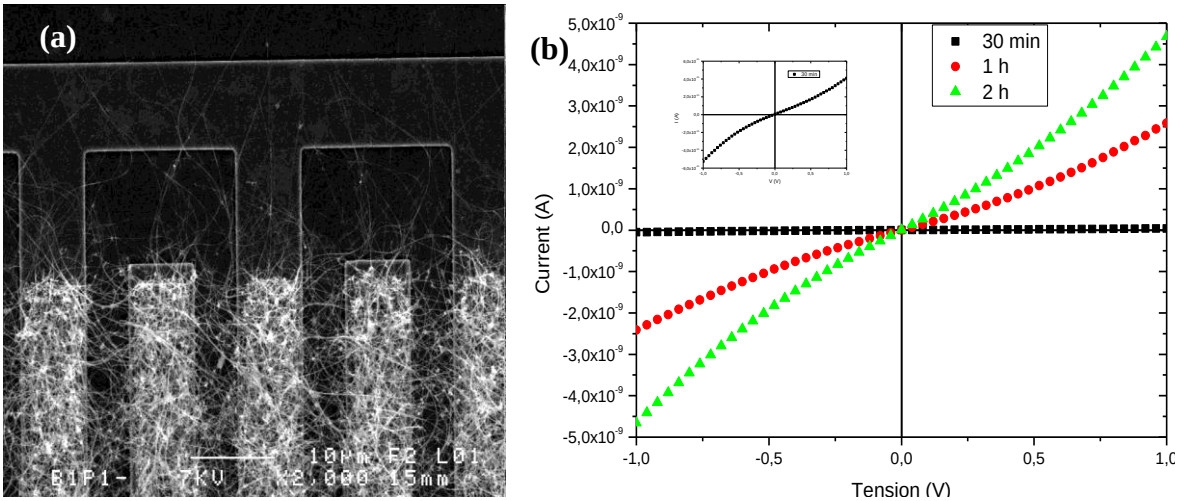


Figure 61: (a) SEM photo of an inter-digital comb-shaped device based on VLS SiNWs (growth for 2h), (b) I-V characteristics for the inter-digital comb-shaped devices which have different durations of growth, (inset) I-V characteristic for the 30 min sample whose current scale is from $-6\times10^{-11}$ A to $6\times10^{-11}$ A.

The figure 61 further confirms that the longer the VLS SiNWs are synthesized, the higher the current level can be obtained. When the geometry of the inter-digital comb-shaped structure is fixed (the space between teeth doesn't change), the longer SiNWs enable to increase the possibility of the interconnection between two adjacent teeth, which decreases the total resistance of the SiNWs device. Thus, the current level of the sample synthesized for 2h is higher than those synthesized for 30 min and 1h.

## II.2 Analysis of each key designing parameter and their influences on current-voltage electrical characteristics

### II.2.1 Inter-digital comb-shaped SiNWs devices

During our studies, two sets of masks have been designed for the inter-digital comb-shaped devices to realize the devices. Besides the thickness of the Au catalyst and the growth duration, the designing parameters of the mask are also very important for the electrical properties of the devices based on SiNWs. By means of analyzing the influence of each key parameter, a suitable combination of the parameters could be found to fabricate an inter-digital comb-shaped device based on SiNWs for the applications as sensors.

As we have mentioned before, the process of inter-digital comb-shaped devices includes two masks. The first mask is to form the geometry of the inter-digital comb-shaped electrodes as shown in figure 62. Two parameters are essential for this mask. One is the number of the teeth on the right side (n) which has two different values, 4 and 8 (For example, the n equals to 8 in figure 62). The other parameter is the distance between two teeth (w) which has also two values, 5 µm and 10 µm. The second mask is used to create the openings which define the regions where should be deposited Au catalyst. There are two different patterns in the second mask (figure 63). The pattern in figure 63-(a) is for the real device while the patterns in figures 63-(b), which create plot openings on half teeth, is only used to facilitate the subsequent SEM observations after the growth of nanowires.

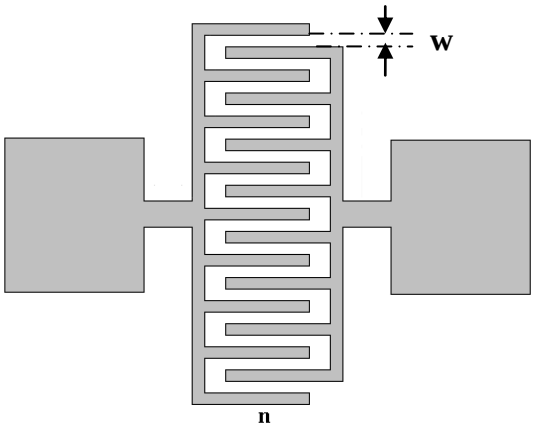


Figure 62: The first mask for defining the geometry of the inter-digital comb-shaped electrodes.

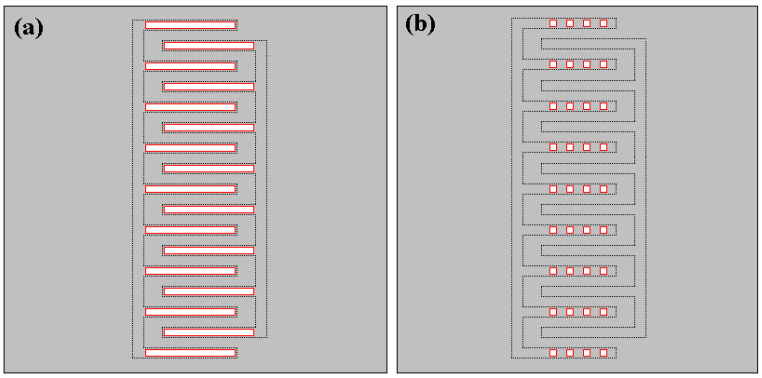


Figure 63: Two different patterns in the second mask, (a) stripe openings on each tooth, (b) plots of openings on half teeth.

Figure 64 shows the I-V characteristics of the inter-digital comb-shaped structure after localized SiNWs synthesis. As a reference, I-V characteristic before SiNWs growth was also plotted in order to insure initial electrical insulation between the two electrodes. This set of measurements highlights a good correlation between current levels measured and parameters as space between teeth (w) and the number of teeth on the right side of the comb resistor (n). Indeed, we can observe that the current (resistance) increases (decreases) as space between teeth (w) decreases and number of teeth increases.

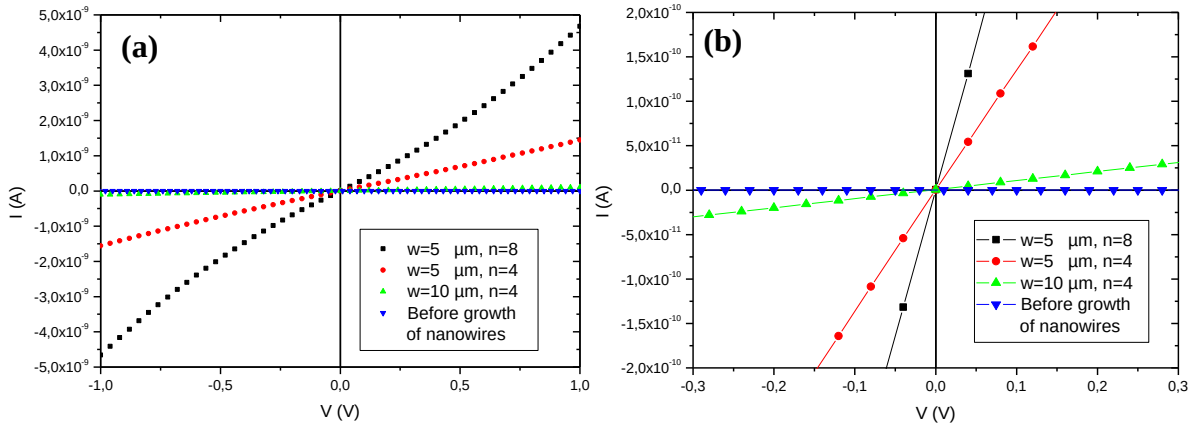


Figure 64: I-V characteristics of SiNWs comb-shaped resistors depending on the space between teeth (w) and the number of teeth (n), (a) bias voltage from -1 to 1 V, (b) bias voltage from -0.3 to 0.3 V.

This result is determined by our inter-digital comb-shaped structure based on SiNWs which is regarded as a series of elementary resistance $R_0$ (formed by the interconnected

SiNWs between two adjacent teeth) connected in parallel (see figure 65). Here, the possibility of nanowires interconnection depends on the space between two adjacent teeth w. It is evident that when the w is larger, there will have less possibility of interconnection for the nanowires (see figure 65) and thus the $R_0$ will become larger (w > w' → $R_0 > R_0$').

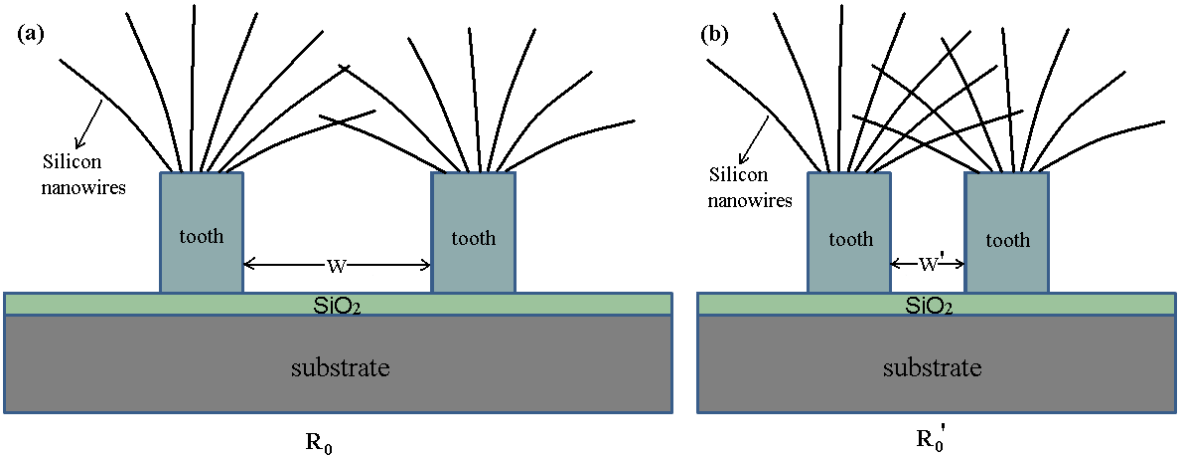


Figure 65 (a-b): Schematics of two resistors with different distance between two teeth (w > w').

Even the space between teeth w can be fixed, the number of interconnected nanowires between two adjacent teeth is different, which means the elementary resistance $R_0$ does not always have the same value. In order to simplify the calculation of the comb-shaped total resistance, we hypothesize that the elementary resistances $R_0$ should be identical. When the right electrode has n teeth, there are 2n elementary resistances for the whole resistor (figure 66). Therefore, the total resistance of this circuit can be expressed as the following formula:

$$R = \frac{R_0}{2n} \tag{8}$$

where $R_0$, R and n represent the elementary resistance between two teeth, the total resistance and the number of teeth on the right side. According to the Ohm's law, we can deduce a formula expressing the current of our comb-shaped resistor as following:

$$I = \frac{2nU}{R_0} \tag{9}$$

Since the voltage (U) is constant, the current of the resistor (I) is proportional to n, and inversely proportional to the elementary resistance $R_0$. In this case, the value of $R_0$ were deduced from current measurements plotted in the figure 64 and reported in the table 1, as well as the average values of elementary resistance ($\overline{R_0}$). The calculated $\overline{R_0}$ highlights the same or close enough values. However, it is really difficult to make a fair performance comparison between comb-shaped devices because the number of participating nanowires can be slightly different.

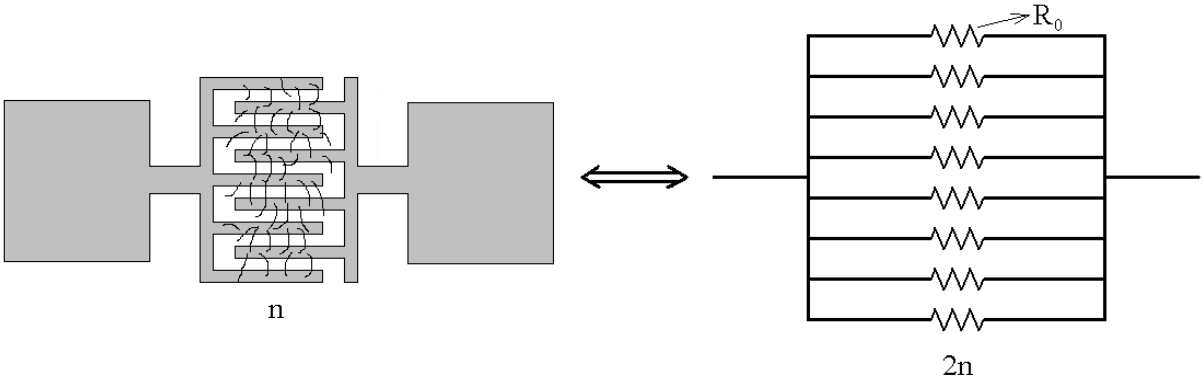


Figure 66: A schematic of an inter-digital comb-shaped resistor and its corresponding circuit diagram.

| U (V) | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 | |
|---|---|---|---|---|---|---|
| $R_0$ (Ω) (n=4) | $5.936\times10^9$ | $5.944\times10^9$ | $5.872\times10^9$ | $5.88\times10^9$ | $5.8\times10^9$ | $\overline{R_0}=5.886\times10^9$ (n=4) |
| $R_0$ (Ω) (n=8) | $4.752\times10^9$ | $4.624\times10^9$ | $4.416\times10^9$ | $4.288\times10^9$ | $4.096\times10^9$ | $\overline{R_0}=4.435\times10^9$ (n=8) |

Table 1: Calculated $R_0$ values deduced from (9) for two values of n.

## II.2.2 V-shaped groove SiNWs devices

The process of V-shaped groove SiNWs devices includes 3 masks (see chapter 3). The first mask helps to etch the V-shaped grooves with two different dimensions (10-µm-wide groove and 20-µm-wide groove with a flat bottom). The second mask is to form the geometry of the electrodes. The third mask contributes to define the locations and the size of the

locations where will be deposited by Au catalyst. The size of the area will be essential for the electrical characteristic of the V-shaped groove SiNWs devices.

Figure 67 shows the SEM photos of the V-shaped groove devices. The bigger the area is deposited by Au catalyst, the more nanowires will interconnect. Thus the current level of the 20-µm-wide groove resistor becomes higher than that of the 10-µm-wide groove resistor (figure 68).

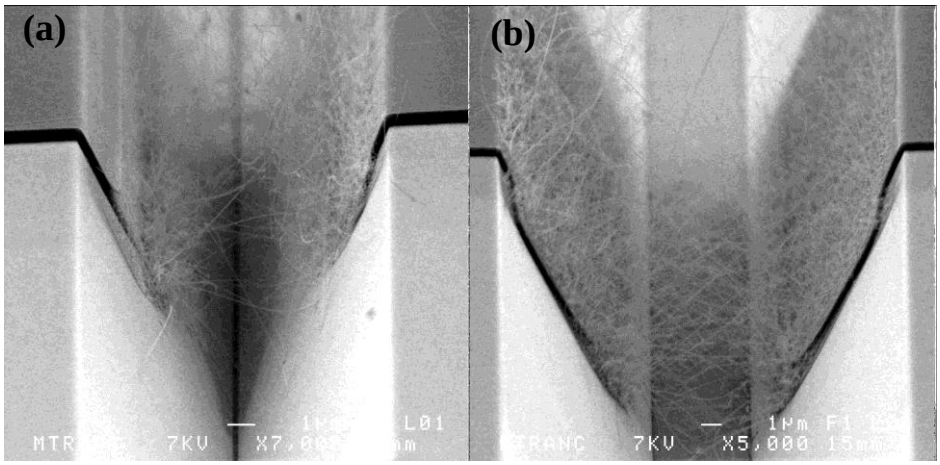


Figure 67: SEM photos of resistors: a) a 10-µm-wide groove resistor and b) a 20-µm-wide groove resistor with a flat bottom.

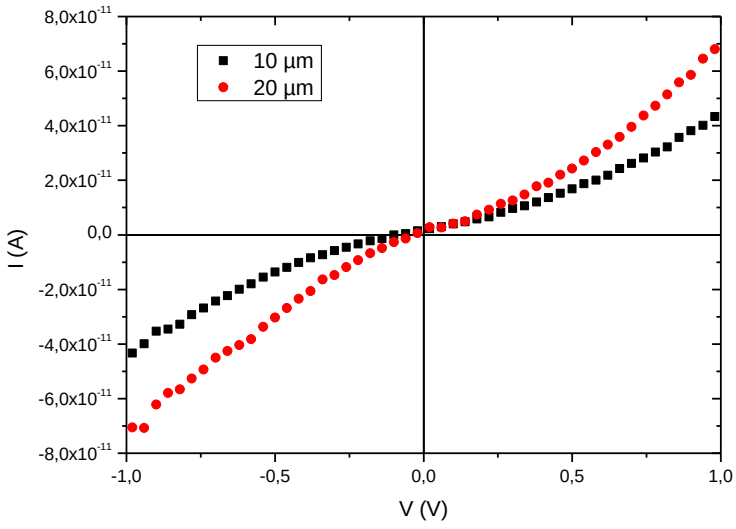


Figure 68: I-V characteristics of V-shaped groove resistors, (a) a 10-µm-wide groove resistor and b) a 20-µm-wide groove resistor with a flat bottom.

## II.3 Studies of the *in-situ* doping for SiNWs

One of the main reasons for the usefulness of semiconductors in electronics is the possibility of controlling the conductivity and carrier type by introducing impurities into an intrinsic semiconductor. In this way, the semiconductor materials can be doped to N-type or P-type, enabling to realize transistors. However, up to now it is not yet fully understood how dopants are incorporated in particle-assisted growth of nanowires, and how the presence of dopants affects wire growth.

In this section, we have tried to use *in-situ* doping method for the purpose of modulating the VLS silicon nanowires electrical properties. The phosphine is chosen as the dopant gas for N-type doping and the doping level is defined by the molecular ratio Γ (phosphine/silane). Once the semiconductor materials have been successfully doped, assumed without any contaminating impurity or crystal defect, the Fermi level will shift from the middle of bandgap to the band edges depending on the incorporated doping level. The corresponding energy needed for a free electron or hole to cross the potential barrier from the Fermi level to the conduction band or valence band is called activation energy, Ea. In this way, a current measurement as a function of temperature permits to obtain the $E_a$ value depending on the doping level of the VLS SiNWs.

The current measurements as a function of temperature are carried out on the inter-digital comb-shaped nanowires resistor, using a cryostat containing a temperature-controlled substrate holder. The diagram of the experimental system for measurement is shown in the following figure 69.

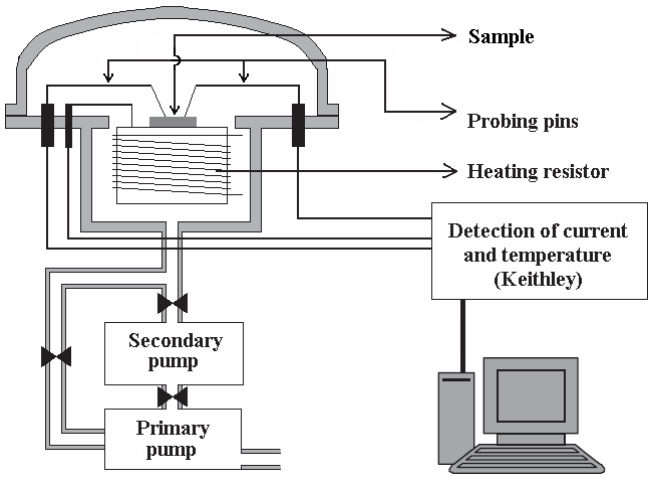


Figure 69: The schematic of system for current-temperature measurements (cryostat).

The current measurements are performed under vacuum (≈ $10^{-5}$ mbar) after degassing the sample at 200 °C for one hour, which permits to eliminate the impurities adsorbed at the nanowires surface that will influence the conductivity. The Keithley 617 whose accuracy of the measurement can reach as low as 1 pA, is used to detect the variation of the current.

The measuring procedure is controlled by a computer system (developed by our laboratory) which allows setting a bias voltage, raising temperature by a constant heating rate (3.7 °C/min), and recording the values of current and temperature during the whole manipulation. The resistors that we have characterized are biased to 1 V for a temperature range between -100 °C and 200 °C. Figure 70 shows the Arrhenius diagram (current as a function of the inverse temperature) for a resistor based on undoped VLS SiNWs.

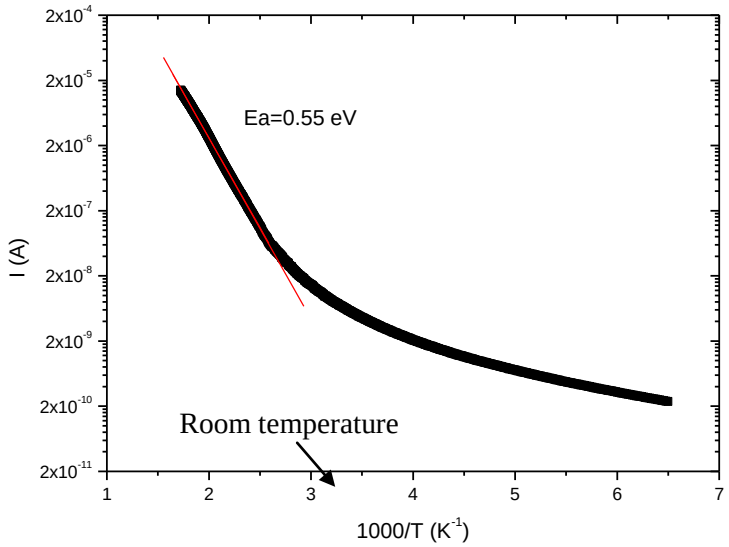


Figure 70: Arrhenius diagram (current as a function of the inverse temperature) of SiNWs based devices

For a semiconductor material, the Arrhenius law obeys the following equation:

$$I = I_0 \exp\left(-\frac{E_a}{kT}\right) \quad (10)$$

where Ea represents the activation energy of carriers in the semiconductor material, which can be calculated according to the slope of the linear part for the curve displayed in semi logarithmic scale.

In the case of undoped silicon, the Fermi level is near the middle of the bandgap (0.56 eV). The measured activation energy value of the resistor based on undoped VLS SiNWs is about 0.55 eV which corresponds to the undoped silicon activation energy. This illustrates that measuring current as a function of temperature and calculating the $E_a$ can indicate the electrical properties of the VLS SiNWs.

By means of adjusting the molecular ratio Γ (phosphine/silane), we have synthesized several VLS SiNWs samples with different *in-situ* doping levels. The concentrations of the phosphorous atoms ($C_p$) for VLS SiNWs derive from an experimental curve of $C_p$ as a function of Γ which is previously established at DM2-IETR [102], concerning *in-situ* doping study on polysilicon layers (figure 71). In this way, $C_p$ may not precisely reflect the doping concentrations in crystalline silicon.

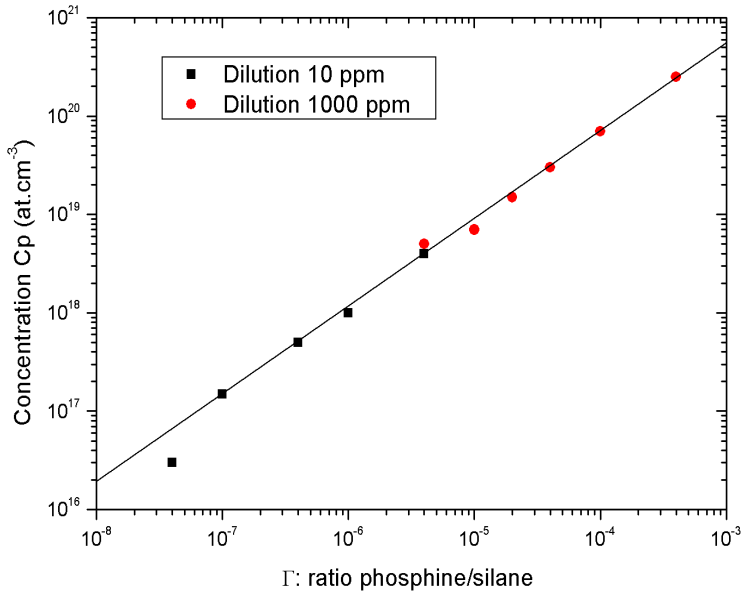


Figure 71: Variation in the concentration of phosphorus atoms versus the molecular ratio Γ[102].

Then, the activation energies deduced from the Arrhenius diagrams for each doping level are plotted as a function of the doping concentration $C_p$ in figure 72. We can notice that when the doping concentration is lower than $2\times18$ at.cm$^{-3}$ the activation energy is quasi constant. Once the doping concentration exceeds $2\times18$ at.cm$^{-3}$, the activation energy decreases significantly. The more interesting point is that the variation of the activation energy seems to be linear between a range of $2\times18$ at.cm$^{-3}$ to $2\times20$ at.cm$^{-3}$. This effect

demonstrates that the *in-situ* doping for the VLS SiNWs could be realized and efficient enough, and the doping level could be well controlled. In order to verify the results of the *in-situ* doping for VLS SiNWs, XPS (X-ray Photoelectron Spectroscopy) analysis is underway.

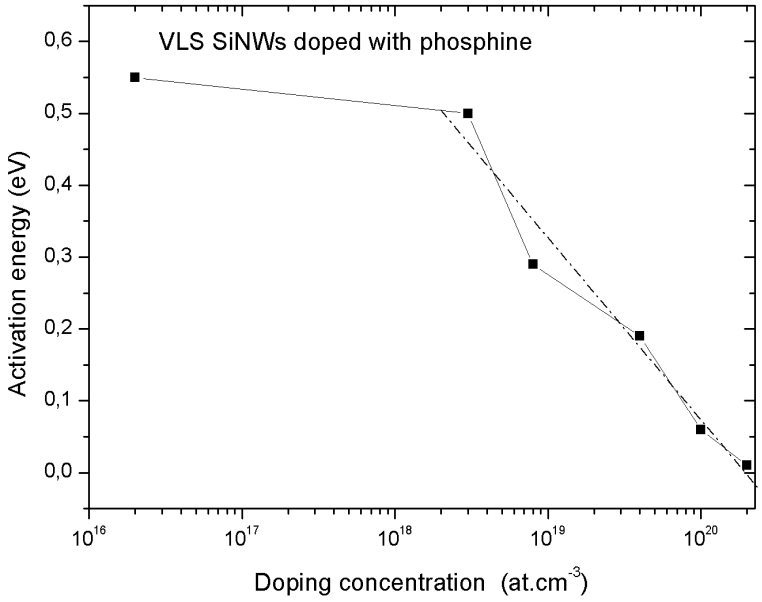


Figure 72: Activation energy of VLS SiNWs as a function of doping concentration.

However, these results cannot significantly be related to the expected activation energy $E_a=E_C-E_F$ resulting from Fermi level shift with the doping concentration for the N-type doped crystalline silicon, because of two main reasons. The first one is that the doping concentration $C_P$ deduced from figure 71 does not correspond to the real doping concentration in the SiNWs. The second one is likely due to the P-type doping effect of the gold catalyst in the nanowire. In this last case, it appears that N-Type doping effect of the phosphine is effective at high $C_P$ values ($>2\times10^{18}$ at.cm$^{-3}$).

## II.4 Electrical characteristics of transistors

After the study of the electrical properties of VLS silicon nanowires, we tried to realize a transistor using nanowires as channels. We hope that the transistor with nanowires channels could increase the sensitivity of detection of charged species.

In the previous section, we have presented the method to realize a transistor based on VLS silicon nanowires. Highly doped silicon substrate is used as gate electrode (figure 73). It is a transistor with a bottom gate and the gate insulator used is a 70-nm-thick silicon dioxide grown by dry oxidation at 1100 °C. The output characteristics $I_{DS}$-$V_{DS}$ and transfer characteristics $I_{DS}$-$V_{GS}$ are shown in figure 74.

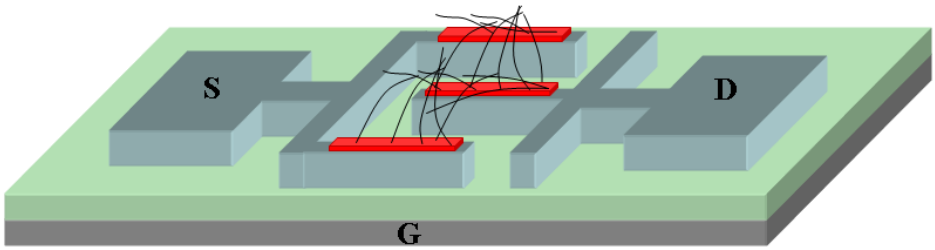


Figure 73: Schematic of a transistor based on VLS SiNWs.

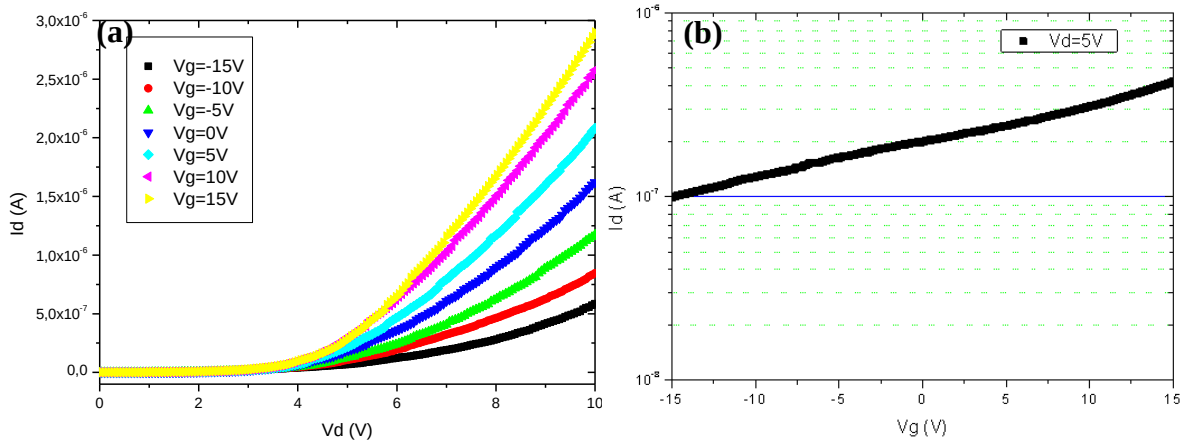


Figure 74: Characteristics for an inter-digital comb-shaped transistor based on VLS SiNWs, (a) output characteristic $I_{DS}$-$V_{DS}$, and (b) transfer characteristic $I_{DS}$-$V_{GS}$.

Comparing with a classical FET, we can observe that the output characteristics plot doesn't exhibit a saturation region even extending the drain-source voltage to the breakdown value (≈ 15V) and the modulation effect is not strong in terms of different gate biases. The weak modulation effect is assumed to be due to the air dielectric between nanowire channel and gate oxide (see figure 75), because air has a better insulation effect than silicon dioxide and the air dielectric thickness is more than 300 nm. In addition, such field effect occurs for

both negative and positive gate biases. This may be attributed to negatively or positively charged species in the air acting as chemical gates.

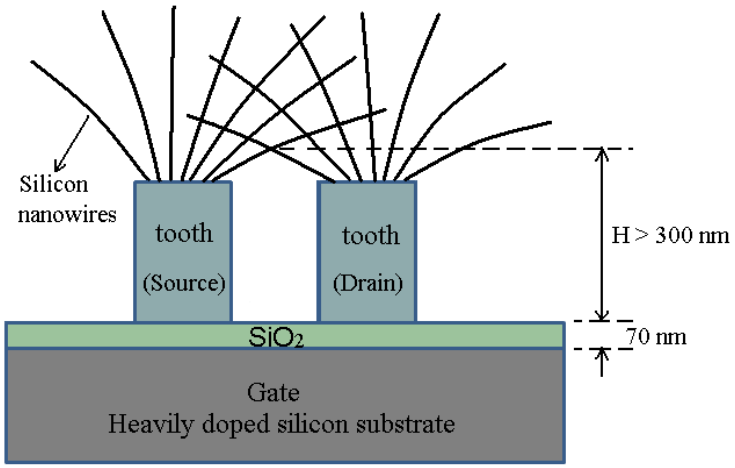


Figure 75: A schematic of inter-digital comb-shaped SiNWs based transistor.

Although the modulation effect of the first transistor is not good enough, the feasibility of such back-gate transistor based on VLS SiNWs has been demonstrated. For development of new sensing applications, the air dielectric may be replaced by liquid (with capped SiNWs). In addition, this method may enhance the field effect and be interesting to the future applications for biological sensors.

# III Electrical measurements and sensor performances

## III.1 Protocols of gas measurements

In order to study and analyze the sensitivity of the devices based on VLS SiNWs as gas sensors operating at room temperature, an optimal procedure of gas measurement should be adopted. In fact, the procedure simulates and defines the working environment of our nanowires devices.

A schematic of the measurement system used for gas detection is shown in figure 76. The sample is placed inside a chamber. A primary pump followed by a secondary pump permits to evacuate most of the chemical species inside the chamber. Two flowmeters can

function separately or simultaneously to control the gases concentration injected into the chamber. The pressure can be regulated by adjusting the valve of primary pump meanwhile the secondary pump is stopped and the gas is injected continuously. The computer system can record the values of current and temperature during the whole manipulation. Two major protocols of the measurement, static and dynamic measurements, will be introduced in detail in the following sections.

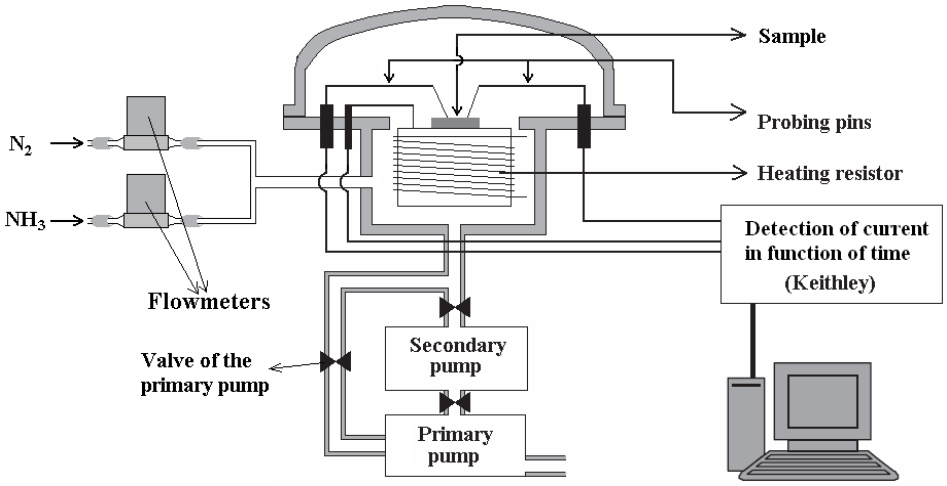


Figure 76: The schematic of measurement system for gas detection (cryostat).

## III.1.1 Electrical response of the sensor

The potential usage of SiNWs as sensitive units for gas detection was checked by measuring the chemical species detection response, $S_g$, which is defined as:

$$S_g = \left|\frac{R_g - R}{R_g}\right| = \left|\frac{I - I_g}{I}\right| \quad (11)$$

where R (I) and $R_g$ ($I_g$) are the resistance (current) values for devices under vacuum and reactive ambient respectively.

## III.1.2 Static measurement

The first protocol is a static measurement for sensors based on VLS SiNWs carried out at room temperature. The chamber holding the sensor is closed and there is no pressure regulation. A flow of nitrogen ($N_2$) gas and a flow of ammonia ($NH_3$) gas are injected into the chamber simultaneously and the ratio of these two gases is controlled by two flowmeters.

The main steps of this protocol for a cycling test are listed as following:

- A primary pump and a secondary pump permit to evacuate most of the chemical species presented inside the chamber. When the vacuum reaches $10^{-5}$ mbar, the pumps are stopped (the chamber is closed).
- Then, we determine the desired ratio of $NH_3/N_2$ (for example: to obtain a ratio of 350 ppm between $NH_3/N_2$, the flowmeter of ammonia is set at 2.84 $cm^3$/min and the flowmeter of nitrogen is set at 8000 $cm^3$/min) and charge the chamber. The charging time depends on the chosen working pressure.
- Once the desired pressure is obtained, the gas flow is cut off and the measurement is started (the chamber is always closed).
- When the desired exposure time is over, the primary and secondary pumps will restart to evacuate the mixture gases of $NH_3/N_2$ in order to return to the initial state.

For the static protocol, the chamber is always closed, so the pressure of the detecting environment completely depends on the charging time. The longer the mixture gases are injected, the more ammonia gas molecules are contained inside the chamber because the ratio of $NH_3/N_2$ is fixed. This means that the static protocol is appropriate to detect a certain quantity of sensing target in a confined space.

## III.1.3 Dynamic measurement

The second protocol is a dynamic measurement of the sensors based on VLS SiNWs for ammonia response. Measurements are carried out at room temperature, and the pressure remains constant. A valve of the primary pump can regulate the working pressure regardless of the flow of gas injection.

The main steps of this protocol for a cycling test are listed as following:

1) When the vacuum reaches $10^{-5}$ mbar, the pumps are stopped.
2) A flow of nitrogen is injected continuously into the chamber and once the desired pressure reaches, the primary pump is activated again and the valve of primary pump enables us to stabilize the pressure (for example: 500 mbar).
3) A current measurement as a function of time is started. After the current stabilizes, a flow of ammonia is injected with the chosen ratio of $NH_3/N_2$.
4) After a certain period of exposure time, the gases are cut off. Then the pumps are turned on again to evacuate the mixture gases of $NH_3/N_2$ and return the detecting environment to the initial state.

For the dynamic protocol, the environment pressure can always be regulated by the valve of the primary pump regardless of the ratio of $NH_3/N_2$. Normally, the pressure is fixed at 500 mbar, because it is the value the closest to the atmosphere pressure that we can adjust by controlling the valve of the primary pump. During the whole period of measurement, the mixture of gases $NH_3/N_2$ is exchanged all the time whereas the concentration of the gases doesn't change as a function of time. This means that the dynamic protocol is suitable to detect a certain concentration of gases in a flowing space.

Both of these two protocols have their own characteristics and applicable environments. The objective of our work is to study the potential applications of the devices based on SiNWs as a chemical sensor with high sensitivity thanks to the large exchange surface between the active layer and the ambient environment. However, flow exchange exists in most of the actual application environments. Therefore, the dynamic protocol is more appropriate to our purpose. It will be adopted to detect the sensitivity of our devices based on VLS SiNWs.

## III.2 Effect under smoke exposure

In this section we study the effect of smoke as a source of pollution upon the inter-digital comb-shaped resistor. For this purpose, the resistor was characterized as a result of an increasing amount of smoke. The smoke source was a stick of incense which was located inside a chamber where held the resistor. The electrical measurements were carried out at

room temperature with an all-or-nothing protocol which is close to the static protocol that we have presented. It means after evacuating the chamber ($P=10^{-5}$ mbar) for a long time, the chamber is back to the atmospheric air. Then smoke of a burnt incense stick was introduced. Following this protocol, flow and gas pressure dependences were not monitored, and smoke pressure in the chamber during SiNWs based resistors exposure is 1 bar.

In this way, a variation of the current in terms of time under the effect of an increasing amount of smoke was monitored as shown in figure 77.

Under incense smoke exposure, the cycling tests show a decrease of the electrical resistance (figure 77), which shows that chemical species adsorbed at the SiNWs surface mostly act as reducing agents. This may be related to the chemical species contained in the incense smoke. Indeed, the gas products from burning incense include CO, $CO_2$, $NO_2$, $SO_2$, etc. with exact ratio of species that are difficult to estimate. The very high value of $S_g$ ($\approx 2\times10^4$ %) may be related to the very high concentration of chemical species brought into the chamber.

This qualitative result shows the potential use of the VLS silicon nanowires as sensitive units for high sensitive gas sensor application operating at room temperature. This first demonstration serves only as a proof-of-concept.

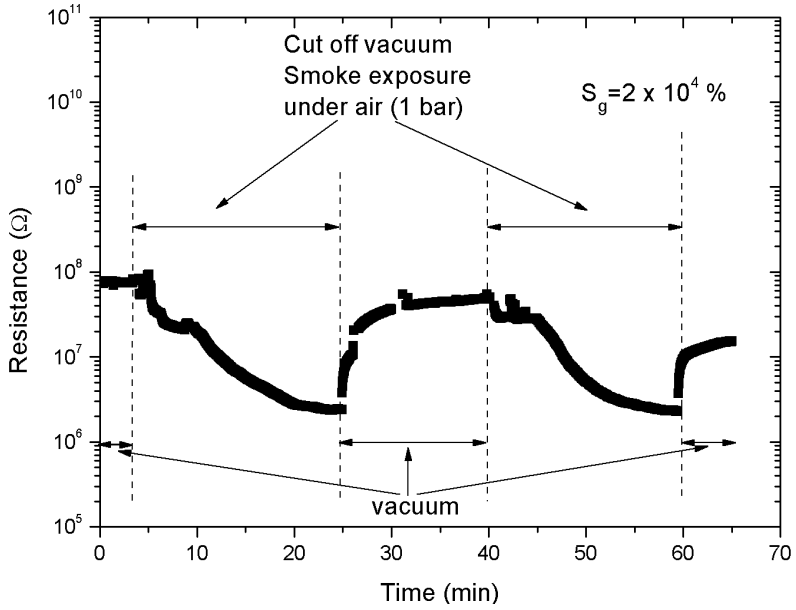


Figure 77: Current response of the device as a function of time upon exposure to smoke.

## III.3 Effect under vacuum or nitrogen exposure

In this section, we study and analyze the effect under vacuum or under nitrogen. Figure 78 shows the curves of I-V characteristics for the comb-shaped resistor in different conditions. After characterizing the resistor in the air (1 bar), the chamber holding the resistor was evacuated to vacuum ($10^{-5}$ mbar) by the primary pump and secondary pump. We can observe that the current decreased after the evacuation of the air. Besides elimination of the species adsorbed on the SiNWs surface, the variations of the pressure and the humidity may also affect the current level.

Then the pumps are stopped, a flow of nitrogen is injected continuously into the chamber. Once the desired pressure reaches, the primary pump is activated again and the valve of primary pump enables us to stabilize the pressure (500 mbar). Compared with the curve under vacuum, the current in nitrogen ambiance at 500 mbar increased a little bit. As we all know, the nitrogen is neutral gas which doesn't react with the silicon nanowires. We suppose that the variation of pressure and limited variation of humidity have only a little influence on the change of the current.

After cutting off the flow of nitrogen, a flow of air was injected into the chamber. In this case, the pressure is always fixed at 500 mbar. Assuming that the difference in humidity between air and nitrogen is negligible, it can be considered that the variation of the current is due to the components under air exposure.

In the end, the resistor was characterized for a second time in the atmospheric air (1 bar). The current is almost back to the initial state.

The objective of this test is to illustrate that the variation of the current or resistance is mainly due to the changes of pressure and different components of gases. When the pressure is fixed to 500 mbar, we think that the resistor based on silicon nanowires is principally sensitive to the change of the gases.

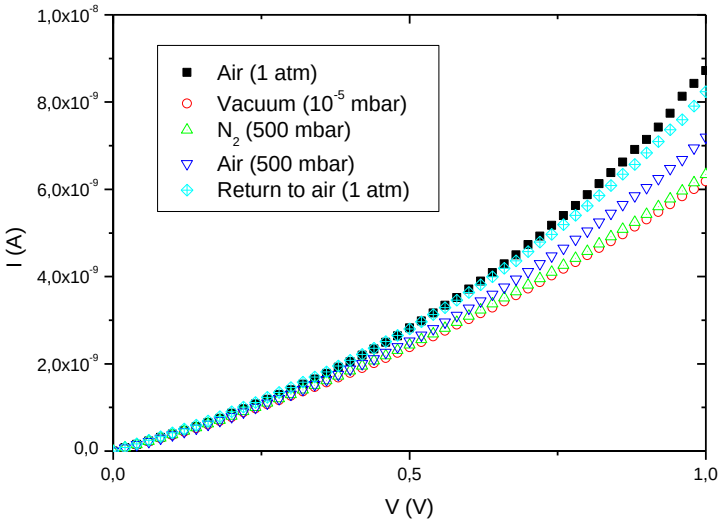


Figure 78: Evolution of I-V characteristics of a comb-shaped SiNWs based resistor in different test conditions.

## III.4 Effect under ammonia exposure

In this section, the measurements strictly following the dynamic protocol under ammonia gas ($NH_3$) will be introduced in detail. Both of the inter-digital comb-shaped SiNWs resistor and the V-shaped groove SiNWs resistor have been characterized at a fixed concentration of ammonia (350 ppm).

Before starting up the sensing measurement, a degassing process was carried out under vacuum. The resistor was heated to T = 200 °C for one hour to ensure the evacuation of most species in the chamber and on the surface of nanowires. The sample is then cooled to room temperature before injection of the gas. The measurements of the change in current through the resistor are performed in function of time.

### III.4.1 Inter-digital comb-shaped SiNWs resistor

Figure 79 shows the evolution of the electrical resistance deduced from the measurement of current with a bias voltage of 1 V at room temperature. Two cycles of exposure to ammonia have been monitored. The time dependent change of the electrical resistance is found to indicate a quasi reversible trend, which suggests that SiNWs could be

reusable after exposure to a low ratio of mixture gas $NH_3/N_2$ (350 ppm). The sensitivity of this resistor, $S_g$, can reach 740 %.

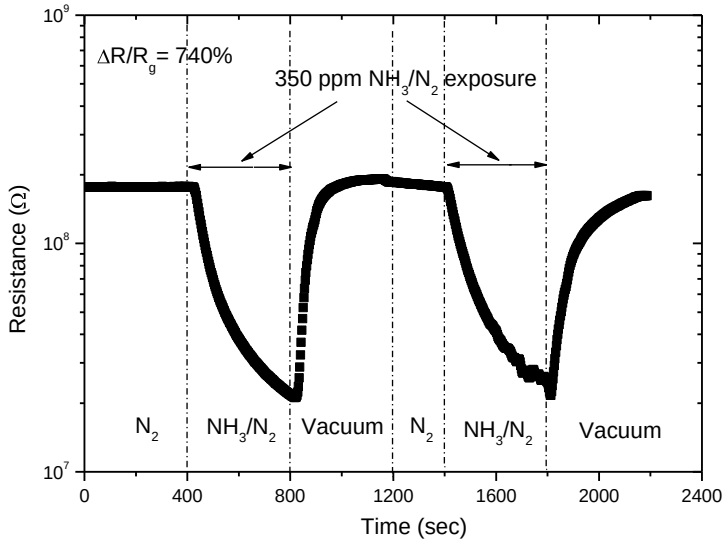


Figure 79: Electrical resistance variations versus time under 350 ppm ammonia exposure cycling test upon inter-digital comb-shaped SiNWs resistor.

## III.4.2 V-shaped groove SiNWs resistor

The same measurement was carried out on the V-shaped groove resistor. Figure 80 shows the electrical resistance variation versus time under 350 ppm $NH_3/N_2$ exposures. For the first cycle, the sensitivity can reach 460 %. However, the reversibility is not effective because the sensitivity, $S_g$, is lower for the second cycle. The lower value observed for the SiNWs based resistors after the second cycle suggests that some of the ammonia gas molecules might not be desorbed after exposure.

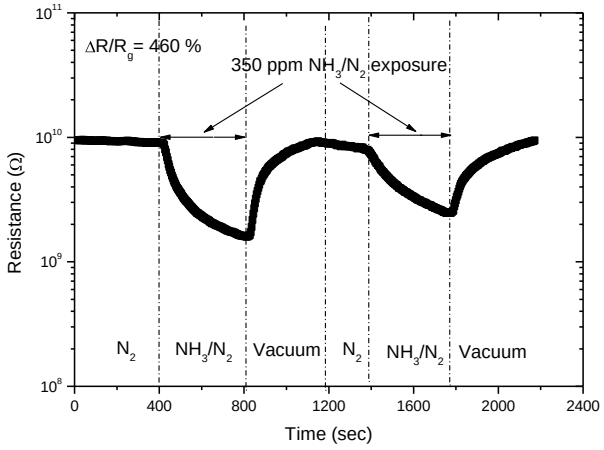


Figure 80: Electrical resistance variations versus time under 350 ppm ammonia exposures cycling test for V-shaped groove SiNWs resistor.

For the two kinds of VLS SiNWs based resistors, as the ammonia gas molecules (acting as donor of electrons or reducing agents) adsorption occurs at the SiNWs surface, electrons are transferred to the SiNWs crystal core. Such interactions induce significant changes in the carriers transport along the nanowires and thus for SiNWs electrical resistance in different possible cumulative ways. First, as the SiNWs conductance can be modulated by an applied voltage [105, 106], positively charged gas molecules (electron donors) bound on SiNWs surface can modulate their conductance by changing the volume of the conductive layer. In this case, ammonia may act as chemical gates. In other words, it means that the Fermi level of the Si nanowires is shifted, which reduces the sample electrical resistance. Moreover, carrier transport strongly depends on structural nanowires defects. So, we have to consider contact resistance between VLS nanowires. Through charge exchange, gas molecules adsorbed may play a significant role in decreasing the potential barrier height at the tunnel junction of two crossed SiNWs. In this case, adsorbed gas molecules passivate defects like dangling bonds and thus lead to an increase of current [107].

However, gold impurities mainly located on the surface of the NWs may act as recombination centers, and therefore they could be responsible of a lowering of the electrons transfer effect related to chemical species detection. Therefore, higher response for further VLS SiNWs based resistors could be expected by using specific etching process of gold.

# IV Conclusion

In this chapter, we have electrically characterized the VLS silicon nanowires and studied their electrical behaviors as a function of *in-situ* doping and temperature. It is demonstrated that the phosphorus *in-situ* doping for the VLS SiNWs could be realized and efficient enough, and the doping level could be well controlled.

Two main protocols for detecting gas responses of the SiNWs sensors are introduced. The first quasi static measurements for the SiNWs based resistor showed their sensitivity under exposure to smoke due to ambient charged species detection. It serves as proof-of-conception for a new kind of SiNWs based devices. Then, the quantitative dynamic measurements under exposure to a low concentration of ammonia gas (350 ppm $NH_3/N_2$) were carried out, which demonstrated high performance of the SiNWs based resistors as high sensitivity sensors. Two main theories, chemical gating effect and charge exchanging effect, were proposed to explain the variation of the resistance under exposure to ammonia gas. It enables to understand the mechanism of conductions for the SiNWs as high sensitivity sensors.

The above results present the potential applications in the field of chemical sensors (gas) for our VLS SiNWs based devices as promising room temperature chemical sensors compatible with classical integrated silicon technology.

# Conclusions and perspectives

The purpose of this research was to realize microelectronic devices (resistors and transistors) based on silicon nanowires synthesized by VLS method. The growth of these nanowires was carried out by LPCVD by using a metal catalyst (gold). The objective of this work was to highlight the potential applications of these devices as a chemical sensor with high sensitivity.

Two different devices based on silicon nanowires were performed: inter-digital comb-shaped and V-shaped groove devices. For the inter-digital comb-shaped device, both of the geometry of the inter-digital comb-shaped structure and the tangled Au-catalyst VLS-SiNWs can increase the exchanging surface (thanks to a high effective surface of the SiNWs) with the ambient environment which enables to raise the sensitivity.

Besides fabricating the devices based on SiNWs, we have also electrically characterized electrically the VLS silicon nanowires and studied their electrical behaviors as a function of *in-situ* doping by phosphine and temperature. It is demonstrated that the phosphorus *in-situ* doping for the VLS SiNWs could be controlled and efficient enough by LPCVD. This can be useful for optimizing the electronic performance of devices based on VLS SiNWs and the future application as transistor.

For detecting gas responses of the SiNWs sensors, two mains protocols: static measurement and dynamic measurement were introduced in this thesis. The first static measurements upon the SiNWs based resistor showed their sensitivity under exposure to smoke due to ambient charged species detection, which serves as proof-of-conception. Then the quantitative dynamic measurements under exposure to a low concentration of ammonia gas (350 ppm $NH_3/N_2$) were carried out, which demonstrated high performance of the SiNWs based resistors as high sensitivity sensors (the relative sensitivity, $S_g$ can reach 740 %). Two main theories, chemical gating effect and charge exchanging effect, were proposed to explain the variation of the resistance under exposure to ammonia gas. The charge exchanging effect is believed that there is a direct charges exchange between the adsorbed molecules and the SiNWs. The chemical gating effect is considered to shift the Fermi level of the SiNWs to change the conducting property. Both of these two theories help to understand the mechanism of conductions for the SiNWs as high sensitivity sensors.

The results obtained during our research are consistent with the desired objective, which permit to validate the feasibility of electronic devices based on VLS SiNWs

synthesized by LPCVD using silane as precursor gas, and the potential applications in the field of chemical sensors (gas) operating at room temperature chemical sensors. Although the first results are encouraging, a lot of studies of optimization could improve the electrical performance for components or sensors based on VLS SiNWs.

The first point to be improved is the contamination of the gold. The gold is known as impurity in nanowire which restricts its compatibility in semiconductor electronic production standards. A gold etching solution (for example, $I_2$/KI [108]) will be tried to remove the gold left on the VLS SiNW surface after growth, and gold impurities effects on electrical performances of devices will be studied.

Although the p-type doping with diborane gas has not been achieved in this thesis, a thin film of doped amorphous silicon has been deposited during the SiNWs growth process on the whole surface of the substrate because of low dissociation energy (silane with participation of diborane). Another doping gas TMB (trimethylboron-$C_3H_9B$) is worth trying to realize the p-type doping effect. For the existing n-type doping SiNWs, an XPS (X-ray Photoelectron Spectroscopy) analysis will be carried out to verify the results of the phosphorus *in-situ* doping for VLS SiNWs which permits to give a more precise value about the doping concentration. Then the relationship of activation energy of VLS SiNWs versus doping concentration enables to understand the phosphorus *in-situ* doping effect of VLS SiNWs.

On the application of undoped SiNWs based devices as gas sensor at room temperature, it is essential to continue the measurements under controlled flow of gas ($NH_3$) with very low concentrations (<1ppm) and start the measurements under oxidizing gas ($NO_2$). A further study on gas sensing effects for devices based on SiNWs with different doping concentrations will also be carried out under both reducing gas and oxidizing gas.

The advantage of V-shaped groove devices is that the etched groove channel can confine the analytes (especially for the liquid and gas analytes) and ensure all the exchanging reactions taking place inside the groove, which would highlight the sensing efficiency of the nanowires inside the V-shaped groove. In this way, a capping PDMS mold is necessary to be assembled on the V-shaped groove device, which could capture the analytes inside a limited space with high density SiNWs. Such a device is expected to enhance the sensitivity of the SiNWs sensor for the chemical or biological applications. In this case, study of SiNWs

surface functionalization will be useful to study sensor selectivity. In addition, novel devices designs will be considered for measurements in aqueous ambience with reported electrical addressing pads.

# Annex 1: Spin-coating procedures

In our process, the spin coating parameters are very important, because they directly determine the coating quality of the photoresist. For example, it is really difficult to coating the photoresist on the places where the difference in height is larger than 2 µm, using the classical set of parameters which will be introduced in the following section in details.

First of all, the photoresist used in this thesis is always UV-210 because it allows defining submicronic patterns (resolution limitation: 130 nm) via photolithography system MA6 from SUSS MicroTech (wavelength of DUV: 248 nm). For different kinds of photoresist, it is obvious that the spin-coating parameters used are not identical because of the differences in fluidity and viscosity. For the process of inter-digital comb-shaped devices, the difference in height is less or equal to 300 nm, thus the basic steps and classical spin-coating parameters are adopted (shown in table 2). It enables to spin-coat a layer of photoresist (UV-210) on the whole substrate uniformly.

| Basic steps | Descriptions |
|---|---|
| Prebake | 120 °C, > 2 min |
| Spin-coating | Acceleration: 5000 r/min/sec, speed: 4200 r/min, time: 30 s |
| Soft bake | 140 °C, 3 min 30 s. |
| Alignment and exposure | Exposure time: 7 s |
| Hard bake | 140 °C, 1 min 30 s. |
| Development | Time: 35 s |

Table 2: Basic steps and spin-coating parameters used for process of inter-digital comb-shaped devices.

For the V-shaped groove structure, we also use the UV-210 photoresist. However, the large difference in height (H > 7.07 µm) prevents a good spin-coating of the photoresist (figure 54). So a modification of the basic steps and the spin-coating parameters has been carried out to solve this problem. It enables to realize a good coverage of the photoresist, even on the edges of the grooves. However, once the spin parameters are modified, the thickness of the photoresist is changed simultaneously. On the flat surface, the thickness of photoresist spin-coated by the new parameters is 1.2 µm while the thickness of photoresist spin-coated by

the classic parameters is 0.6 µm. At the bottom of the groove, the thickness of the photoresist is much larger than that on the flat surface. Therefore, exposure time and developing time should be extended. The modified steps and parameters are shown in table 3.

| Basic steps | Descriptions |
|---|---|
| Prebake | 120 °C, > 2 min |
| First spin-coating | Acceleration: 500 r/min/sec, speed: 1000 r/min, time: 30 s |
| First soft bake | 140 °C, 2 min 30 s |
| Second spin-coating | Acceleration: 500 r/min/sec, speed: 1000 r/min, time: 30 s |
| Second soft bake | 140 °C, 3 min 30 s |
| Alignment and exposure | Exposure time: 45 s |
| Hard bake | 140 °C, 1 min 30 s |
| Development | Time: 1 min 30 s |

Table 3: Basic steps and spin-coating parameters used for process of V-shaped groove devices.

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