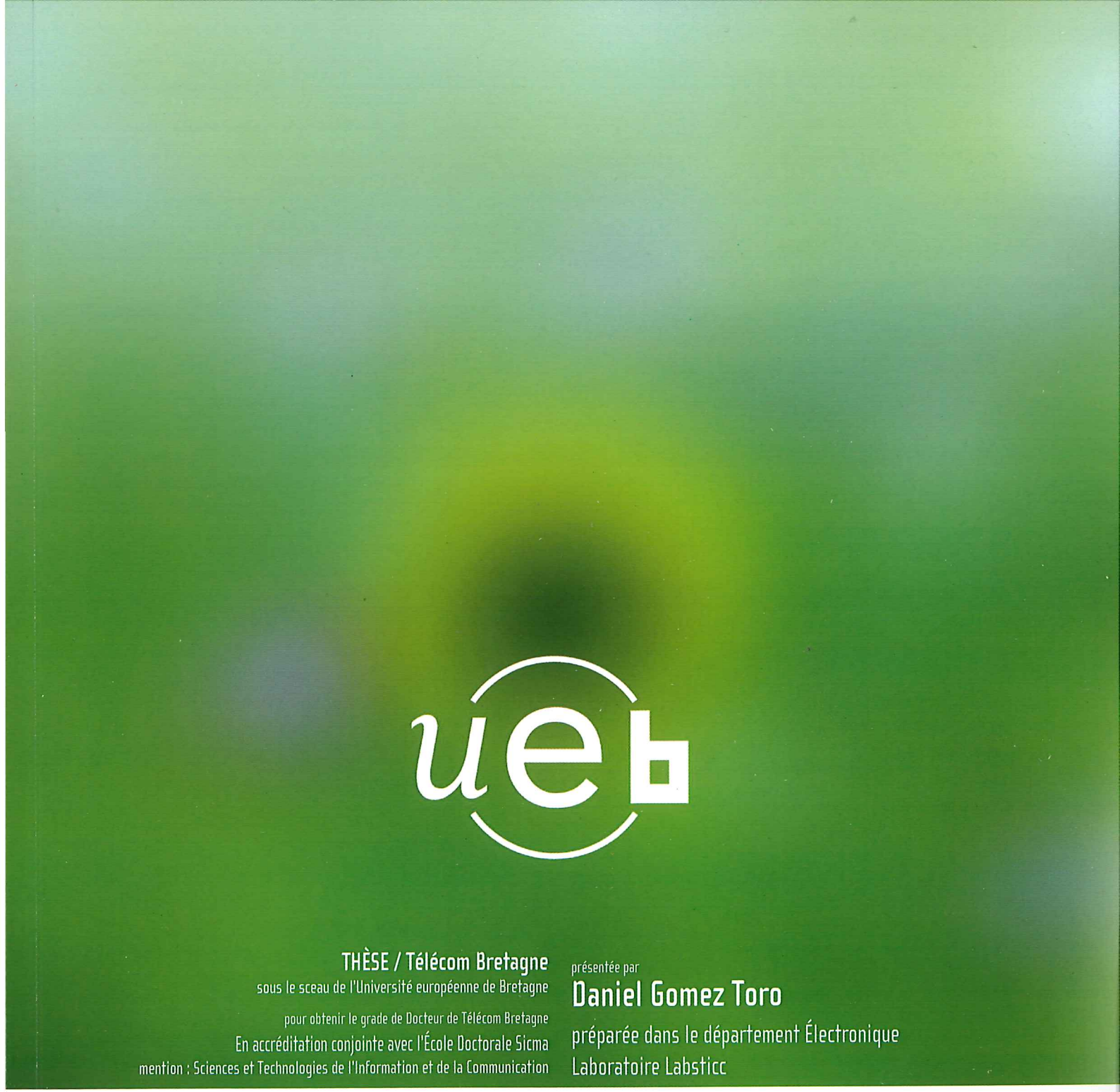
Temporal Filtering with Soft Error Detection and Correction Technique for Radiation Hardening Based on a C-element and BICS

Daniel Gomez Toro



THÈSE / Télécom Bretagne
sous le sceau de l'Université européenne de Bretagne

pour obtenir le grade de Docteur de Télécom Bretagne
En accréditation conjointe avec l'École Doctorale Sicma
mention : Sciences et Technologies de l'Information et de la Communication

présentée par
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préparée dans le département Électronique
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Thèse soutenue le 12 Décembre 2014
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N^{O} d'ordre : 2014telb0344

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Thèse de Doctorat

Mention : « Sciences et Technologies de l'Information et de la communication (STIC) »

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Ce n'est pas assez d'avoir l'esprit bon, mais le principal est de l'appliquer bien. Les plus grandes âmes sont capables des plus grands vices aussi bien que des plus grandes vertus; et ceux qui ne marchent que fort lentement peuvent avancer beaucoup davantage, s'ils suivent toujours le droit chemin, que ne font ceux qui courent et qui s'en éloignent.
Discours de la méthode, René Descartes.

The greatest enemy of knowledge is not ignorance, it is the illusion of knowledge.
Stephen Hawking

La creación intelectual es el más misterioso y solitario de los oficios humanos.
Gabriel García Marquez

Remerciements

Je tiens a remercier Michle Jézéquel et Patrick Adde pour m'avoir ouvert les portes de Télécom Bretagne et de m'avoir donné l'opportunité de réaliser mon doctorat au sein du département électronique. Je remercie également le soutient de PRACOM pour mon projet de thèse. Je remercie mes encadrants, Matthieu Arzel et Fabrice Seguin, pour leur engagement et leur soutient dans cette thèse.

Tout au long de ce travail et de cette aventure en France, j'ai eu le soutient de ma famille et de mes proches, qu'avec Joie et Harmonie m'ont donné des forces et des conseils pour surmonter les différents obstacles. Gracias a todos.

J'ai de la gratitude aussi pour mes collègues Ronald, Oscar, Dani, Javier, Andrea, Sandra, Juan David, Cristina et Soraya pour les bons moments à Télécom et pour mes collegues du groupe de recherche non-académique TIM.

Je veux aussi remercier les jurys de cette thèse pour leur participation dans ma soutenance et l'intérêt porté sur mes travaux.

ABSTRACT

Temporal Filtering with Soft Error Detection and Correction Technique for Radiation Hardening Based on a C-element and BICS

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The higher density of integration and lower supply voltage have led to lower noise margins and a smaller amount of charge representing a bit of information. The International Technology Roadmap for Semiconductors (ITRS) stated that below 65 nm CMOS Technology soft errors impact field-level circuit reliability, not only for embedded memories, but for logic and latches as well. Soft errors are nondestructive functional errors, in contrast to hard errors that induce destructive effects. They are induced by an energetic ionized particle striking a MOS transistor. Those particles have their main origins in cosmic radiation and radioactive package impurities. The strike of an ionized particle on a MOS transistor creates a transient current between the substrate and the drain causing a voltage spike on the drain. That is a single-event transient (SET). If an SET is latched it becomes a single-event upset (SEU). It is important to model the phenomenon in order to understand and simulate its effects on the integrated circuit that need hardening. For that the charge collection model helps determining the amount of charge collected on a drain surface given the geometry of an ionization track and the position of the drain. Thanks to this model the parasitic current can be estimated. This modeled current can be introduced in CADENCE's electrical simulator SPECTRE as a bulk-drain current source to simulate its effects. This simulation methodology can be used on a target system to determine the sensitivity of a particular circuit to SETs. As a case study a low power 8-bit successive-approximation-register (SAR) analog-to-digital converter (ADC) implemented in ST 65nm CMOS technology has been chosen. This ADC is composed of several blocks, combining analog, digital synchronous and asynchronous logic. This diversity of circuits leads to different soft error outcomes. Among those circuits, a particular combinatorial function that generates an internal clock signal has been selected for hardening for its importance in the conversion cycle. Thanks to the simulation methodology, a study of the electrical, geometrical and temporal sensibilities is conducted to show the vulnerability issues of the function. It is concluded that an external circuit should be placed outside the combinatorial function to harden the function without being exposed to the same vulnerabilities. To counter the effects of SETs several technological and by design techniques exist. This work focuses on radiation hardening by design (RHBD) techniques since those techniques can be applied whiteout any additional technological cost. Many conventional RHBD techniques exist for different abstraction levels. For example, for a transistor level exist the transistor sizing and transistor folding techniques. For a combinatorial level logical masking is used. On a system level three main redundancy techniques exist: Hardware, information and temporal redundancy. Those techniques focus on hardening the system either by hardening the transistors or the output of the system without changing the system itself. The extra hardware used for hardening brings important power, propagation delay or area overheads. Additionally, this hardware is not self hardened and if soft errors take place they can affect the whole system. Hence the question: *who guards the guardians?* This work proposes a system that acts as an SET temporal filter, with self-healing properties to prevent SET propagation, thanks to feedback. The system can also indicate through its output signals if the transistors were hit.

Keywords: Cosmic rays, Soft Error, SET, SEU, Charge Collection Model, Critical Charge, SAR ADC, Radiation Hardening by Design, Temporal Filtering, C-element, BICS.

RÉSUMÉ

Temporal Filtering with Soft Error Detection and Correction Technique for Radiation Hardening Based on a C-element and BICS

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12 Décembre 2014

L'augmentation de la densité d'intégration et la baisse de la tension d'alimentation ont amené une baisse de la marge du bruit et de la quantité de charges qui représentent un bit d'information. L'International Technology Roadmap for Semiconductors (ITRS) indique qu'en dessous de la technologie CMOS de 65 nm les erreurs soft ont un impact plus important sur la fiabilité des circuits au sol, non seulement sur les mémoires embarquées, mais aussi pour la logique et les verrous. Les erreurs soft sont des fautes fonctionnelles non destructives, à la différence des erreurs hard qui induisent des effets destructifs. Ils sont induits par des particules ionisantes très énergétiques qui frappent un transistor MOS. Ces particules ont pour origines principales la radiation cosmique et des impuretés radioactives dans le boîtier du circuit intégré. L'impact d'une particule ionisante sur un transistor MOS crée un courant parasite entre le substrat et le drain créant ainsi un pic de tension sur le drain. Il s'agit là d'un événement transitoire singulier (SET sigles en Anglais). Si un SET est verrouillé on parle alors d'événement singulier perturbateur (SEU sigles en Anglais). Il est important de modéliser le phénomène pour comprendre et simuler ses effets sur les circuits intégrés qui doivent être durcis. Pour cela le modèle dit "de collection de charge" permet de déterminer la quantité de charges collectées par un drain grâce à la géométrie d'une trace d'ionisation et de la position du drain. Grâce à ce modèle le courant parasite peut être estimé. Ce courant modélisé peut être intégré dans le simulateur électrique SPECTRE de CADENCE comme une source de courant entre le substrat et le drain pour simuler ses effets. Cette méthodologie de simulation peut être utilisée sur un système cible pour déterminer la sensibilité aux SET d'un circuit en particulier. Un convertisseur analogique numérique (CAN) d'approximations successives (SAR en Anglais) et de basse consommation a été choisi comme cas d'étude. Ce CAN est composé de différents blocs, combinant ainsi des circuits analogiques, numériques synchrones et asynchrones. Cette diversité de circuits peut donner lieux à différents résultats causés par des erreurs soft. Parmi ces circuits, une fonction combinatoire particulière qui génère une horloge interne a été choisie afin d'être fiabilisée, en raison de son importance dans le cycle de conversion. Grâce à la méthodologie de simulation, une étude de sensibilité est faite au niveau électrique, géométrique et temporel pour déterminer les vulnérabilités de la fonction. Il est conclu qu'un circuit supplémentaire devrait être placé à l'extérieur de la fonction combinatoire pour la durcir sans que le durcissement soit affecté par les mêmes vulnérabilités. Pour contrer les effets des SET plusieurs techniques technologiques et de conception existent. Ce travail se focalise sur les techniques de durcissement contre les radiations par conception (RHBD en Anglais), puisqu'elles peuvent être appliquées sans un coût technologique additionnel. Plusieurs techniques RHBD existent pour différents niveaux d'abstraction. Par exemple, au niveau transistor existent les techniques de dimensionnement et de format. Au niveau combinatoire le masquage logique est utilisé. Au niveau système trois techniques de redondance existent: la redondance matérielle, la redondance d'information et la redondance temporelle. Le matériel ajouté pour le durcissement peut entrainer des coûts supplémentaires en consommation de puissance, en délai de propagation et en surface de circuit. De plus, ce matériel n'est pas lui même durci et si des erreurs soft ont lieu, ils peuvent affecter le reste du système. D'où la question *qui garde les gardiens?* Dans cette thèse nous proposons un système qui agit comme un filtre temporel de SET, avec des propriétés d'auto régénération pour éviter la propagation de SET, à l'aide d'une rétroaction. Le système peut aussi indiquer à travers de ses signaux de sortie si les transistors ont été touchés.

Mots-clés: Rayon cosmique, Erreur soft, SET, SEU, Modèle de Collection de Charge, Charge Critique, CAN SAR, Durcissement contre les Radiations par Conception, Filtrage Temporel, C-element, BICS.

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Accronyms

ACU Algorithm Control Unit.

ADC Analog-to-Digital Converter.

CAD Computer-Aided Design.

CC Critical Charge.

CMOS Complementary Metal–Oxide–Semiconductor.

CPLD Complex Programmable Logic Device.

DAC Digital-to-Analog Converter.

DD Displacement Damage.

DICE Dual Interlocked storage CEll.

DNL Differential Nonlinearity.

ECD Error Correction using Duplication.

ELT Enclosed Layout Transistors.

FPGA Field-Programmable Gate Array.

HVT High Threshold Voltage (Vt) Transistors.

INL Integral Nonlinearity.

JEDEC Joint Electron Device Engineering Council.

LET Linear Energy Transfer.

LVT Low Threshold Voltage (Vt) Transistors.

MBU Multi Bit Upset.

MCU Multi Cell Upset.

MOS Metal–Oxide–Semiconductor.

RAM Random Access Memory.

RAM Static Random Access Memory.

RHBD Radiation Hardening by Design.

SEB Single Event Burnout.

SEE Single-Event Effect.

SEFI Single Event Functional Interrupt.

SEGR Single Event Gate Rupture.

SEL Single event Latchup.

SER Soft Error Rate.

SES Single Event Snapback.

SET Single Event Transient.

SEU Single Event Upset.

SHCN Sample and Hold Capacitor Network.

SHE Single Hard Error.

SOI Silicon On Insulator.

SOS Silicon On Sapphire.

SVT Standard Threshold Voltage (Vt) Transistors.

TB Test Bench.

TCAD Technology Computer-Aided Design.

TID Total-Ionizing Dose.

TMR Triple Module Redundancy.

Notations

AL_e Electron absorption length.

AL_n Neutron absorption length.

AL_x Absorption length.

$A_{Location}$ Location altitude.

AL_μ Muon absorption length.

$AL_{p,\pi}$ Proton and Pion absorption length.

B_{si} Silicon constant.

Dn Diffusion coefficient for electrons.

Dp Diffusion coefficient for holes.

D Ambipolar diffusion coefficient.

δ Delay.

E_G Energy gap.

E_{pair} Energy to create an electron-hole pair in silicon.

E Electric field.

ε_0 Vacuum permittivity.

ε_{si} Silicon permittivity.

F_0 Reference flux.

$F_{Location}$ Location flux.

g Generation function.

H_0 Pressure equivalent of the reference altitude A_0.

$H_{Location}$ Pressure equivalent of the location altitude $A_{Location}$.

I_{max} Peak current at t_{max}.

K Coefficient for the diffusion concentration calculation.

k Boltzman constant.

μ_n Electrons mobility.

μ_p Holes mobility.

$N+$ Extrinsic silicon with n-type doping.

N_0 Initial concentration of electron-hole pairs along an ionized track.

N_A p-type doping concentration.

N_D n-type doping concentration.

n Majority carrier concentration.

ν_c Average collection velocity.

$P+$ Extrinsic silicon with p-type doping.

Q Total deposited charge in the ion track.

q Electron charge.

ρ_{Si} Silicon density.

ρ Element density.

σ_{SAT} Soft error cross section saturation.

$\sigma_{soft-error}$ Soft error cross section.

T Temperature in Kelvin.

τ_{Auger} Auger recombination time.

τ_{Rad} Radiative recombination time.

τ_{SRH} Schockley-Read-Hall recombination time.

$\tau_{Surface}$ Surface recombination time.

τ_{α} Collection time.

τ_{β} Time of establishment of the ion track.

τ Majority carriers lifetime.

t_{max} Time when the peak I_{max} takes place.

V_0 Applied voltage.

V_T Threshold voltage.

W_{dep} Depletion region width.

Résumé en français

Introduction Au temps de l'ENIAC et du Hardvard Mark vers la fin des années 1940, les erreurs matériels des ordinateur étaient généralement causés par des brûlures de tubes à vide ou par des courts circuits causés par des insectes d'où l'utilisation du terme "bug" (insecte en anglais) en informatique et en électronique. Depuis ce moment la fiabilité du matériel a été un soucis. A ce moment là, un tube à vide tombait en panne tous les deux jours et devait être remplacé. De nos jours, si une erreur survient il est impossible de remplacer un transistor dans un circuit imprimé. D'où le besoin de stratégies locales de durcissement des circuits. Les sources des erreurs ont changé depuis la fin des années 1940, en passant des bugs et des brûlures de tube à des radiations ionisantes. La radiation peut causer des erreurs transitoires (erreurs soft) comme aussi des erreurs permanentes (erreurs hard) sur les composants. L'International Technology Roadmap for Semiconductors (ITRS) indique, qu'en dessous de la technologie CMOS de 65 nm, la fiabilité des circuits et sérieusement menacée.

Beaucoup de stratégies de durcissement contre les radiations ont été développées au fil des années. Certaines se focalisent sur le durcissement technologique, tandis que d'autres se centrent sur le durcissement par conception. Le durcissement technologique s'applique pendant le processus de fabrication des circuits intégrés pour durcir les propriétés physiques des transistors contre les radiations ionisantes. Ce type de durcissent est coûteux. Une alternative au coût de cette technique est le durcissement par conception. Dans ce type de durcissement, les circuits sont conçus pour supporter un certain niveau de ionisation sans besoin de faire un changement dans le processus de fabrication. En général, cette technique place des circuits additionnels pour ajouter de la redondance dans le but de protéger de l'information. Puisque ces "circuits gardiens" sont fait de la même technologie que le reste du circuit, ils peuvent à leur tour être victimes de la radiation ionisante. Dans ces conditions on peut se poser la question *qui garde les gardiens?*

Ce travail veut apporter une réponse à cette question. Dans cette optique, le

premier pas est de connaître les origines de cette radiation ionisante et des mécanismes qui peuvent causer des erreurs dans les circuits. Aussi, pour être capable de simuler et valider une future solution, un modèle d'impact de radiation doit être établi. Ce modèle doit donner une représentation réaliste du phénomène. Ces aspects sont traités dans le Chapitre 1.

Le Chapitre 2 met en contexte un impacte de radiation avec un système électronique. Dans ce cas il s'agit d'un convertisseur analogique numérique (CAN) de type SAR. Ce type de système mélange des circuits analogiques, numériques synchrone et asynchrones. Cette diversité permet d'observer une variété d'effets dans un seul système. Un autre aspect à prendre en compte est le fait que le convertisseur est conçu pour des applications de basse puissance, et la basse puissance est un des défis les plus importants dans l'industrie de l'électronique. Ce chapitre explorera la vulnérabilité d'un tel système et déterminera un circuit potentiellement critique. En utilisant le modèle d'impact de radiation du Chapitre 1, une méthodologie de simulation électrique sera établie pour étudier la sensibilité aux radiations du circuit critique sous trois aspects. Le premier sera de déterminer la sensibilité électrique, en utilisant le concept de charge critique. Le deuxième sera d'étudier la sensibilité géométrique, utilisant le concept de section critique (ou surface sensible). Finalement la sensibilité temporelle permettra d'observer si un état logique est plus sensible qu'un autre au fil du temps. L'étude complète donnera un cahier de charges qu'une solution de durcissement devra être capable d'accomplir pour cette étude de cas.

Après avoir choisi un circuit qui nécessite un durcissement, il sera impératif d'explorer les solutions existantes pour cela un état de l'art des techniques de durcissement contre les radiations sera établi. Ceci fera part du Chapitre 3. Il montrera les différence entre les techniques de durcissent technologique et par conception. Grâce à cet état de l'art, une discussion aura lieu sur les enjeux pour une solution de durcissement contre les radiations qui peut répondre à la question *qui garde les gardiens?* dans le contexte du CAN SAR de basse puissance. Cette discussion soulignera une stratégie de durcissement particulièrement intéressante appelée filtrage temporel. Le concept de rétroaction est utilisé par certains filtres temporels pour arriver à un certain degré d'auto durcissement, mais ceci reste limité.

La solution proposée dans cette thèse, le filtre temporel avec un C-élément avec Détection et Correction (CDC), sera présentée dans le Chapitre 4. L'architecture du CDC sera utilisée pour durcir un filtre temporel lui même avec l'idée de l'auto compensation en utilisant la rétroaction. Cette solution prendra les avantages des propriétés de filtrage et ajoutera la détection d'impacts ionisants, l'auto compensation par rétroaction et la possibilité de coder l'information du filtre pour plus de durcissement. Le CDC sera simulé et comparé aux autres filtres temporels de l'état

de l'art avec des circuits sans parasites. Cette comparaison utilisera des métriques de performance qui prendront compte ce qui doit être investi en termes de surface de circuit et de consommation de puissance pour atteindre le durcissement.

Finalement, le Chapitre 5 se focalisera sur la faisabilité du CDC et de l'impact des parasites extractés dans sa performance. Une discussion sur comment la solution CDC peut être implémentée sur layout débouchera sur différentes options de conception. Pour choisir l'option la plus appropriée les circuits extractés avec parasites seront comparés. Ensuite, la performance du circuit extracté choisi sera comparé ultérieurement avec celle des autres filtres de l'état de l'art avec les métriques expliquées auparavant.

La conclusion finale résumera les contributions de ce travail et proposera les perspectives

Chapitre 1 Radiation cosmique et impact sur les circuits intégrés Les rayons cosmiques sont des radiations de haute énergie dont leur origine est extérieur au système solaire. On appelle rayons cosmiques primaires qui entrent en contact avec l'atmosphère. Ces rayons génèrent des sous produits lorsqu'ils réagissent avec les particules de l'atmosphère on les appelle rayons cosmiques secondaires. Ils sont responsables des réactions en cascade qui vont finalement aboutir aux rayons cosmiques terrestres. Ces derniers sont les particules énergétiques qui peuvent être retrouvées au niveau de la mer. Ces rayons peuvent donc toucher des circuits électroniques depuis l'espace jusqu'au niveau de la mer. Dans l'espace la particule la plus présente dans le flux de rayons cosmiques est le proton. Au niveau terrestre la particule la plus présente après les réactions en cascades est le neutron. Le principal problème lorsque ces particules (ou autres particules ionisantes) entrent en contacte avec les transistors est le courant parasite induit par l'ionisation du silicium. Le silicium peut être ionisé par un proton ou par une particule α mais pas par un neutron. Le neutron ionise de manière indirecte le silicium par des sous produits ionisants de la réaction entre lui et le silicium. Le passage d'une particule ionisée de haute énergie, crée des pairs électron-trou le long de son parcours. Le courant parasite qui s'entraine est établit entre le substrat et le drain d'un transistor. Trois composantes définissent le courant: le courant de dérive (drift), le courant par effet d'entonnoir (funneling) et le courant de diffusion. Ce courant parasite peut engendrer des erreurs destructives permanentes sur les composants (Hard errors), des erreurs transitoires d'état logique (Soft errors) et la dégradation des composants avec le temps.

Le courant d'ionisation peut être modélisé pour la simulation électrique de circuits. Plusieurs modélisations existent comme la somme de deux exponentielles avec des paramètres de temps de collection de charges, ou le produit d'exponentielles

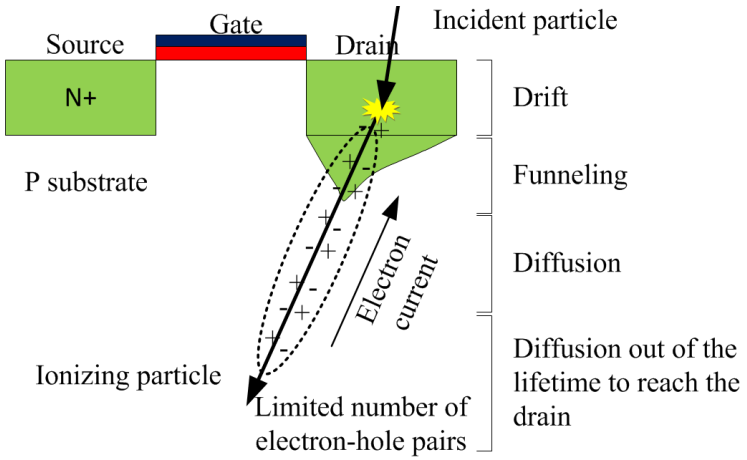


Figure 1: Ionization by a particle strike on an NMOS transistor.

en fonction du pic de courant. Le modèle de collection de charges permet d'avoir une approche plus réelle puisqu'il tient compte des paramètres géométriques et physiques du transistor et de la trace ionisante. Grâce à ce modèle on peut aussi estimer la section critique, qui est la surface sensible dans laquelle si un événement ionisant se produit il peut engendrer un changement d'état logique. Cette surface est limitée par la durée de vie des porteurs de charge majoritaires et par le nombre limité de pairs électron-trou possibles de générer lors de l'ionisation.

Chapitre 2 Etude de l'impact de radiation sur un CAN SAR Dans le but de comprendre les effets des radiations sur un système complexe il serai préférable d'avoir un système qui puisse combiner différent types de circuits pour avoir un vue d'ensemble des différents effets produits. Pour ce faire, un convertisseur analogique numérique asynchrone de type SAR a été choisi. De plus le CAN choisi a été conçu pour une basse consommation et permet de faire une conversion sur 8 bits à 10 MHz. Par rapport à d'autres CAN de l'état de l'art, les convertisseur de type SAR ont un bon compromis entre vitesse de conversion, consommation de puissance, précision et latence. De plus le SAR choisi de Harpe et al. [HZB+11] est très orienté vers la basse consommation et ceci est un des enjeux les plus importants de l'industrie électronique d'aujourd'hui. Ce CAN initialement conçu en technologie CMOS de 90 nm été adapté à la technologie CMOS 65 nm de ST Microelectronics, utilisée dans ce travail. Pour pouvoir faire une analyse de sensibilité aux radiations il est plus judicieux de commencer par une partie critique, au lieu d'analyser tout le circuit au même temps. Une fonction combinatoire en particulier est très critique, la CLK Generator, puisqu'elle génère le signal *Internal CLK* qui contrôle le comparateur du CAN. Ce comparateur est le responsable de décider la valeur des bits pour la

conversion, et il ne s'active que sous l'ordre du CLK Generator. Une erreur de la part de ce signal peut activer le comparateur à un mauvais moment et indiquer une valeur erronée de bit. Pour son rôle de contrôle du signal d'activation, la fonction CLK Generator est choisie pour l'étude de sensibilité. L'étude de sensibilité est fait à trois niveaux pour voir l'impact d'événements transitoires non destructifs (SET) une sous catégorie d'erreurs soft. Dans un premier temps, une étude de charge critique permet d'évaluer la sensibilité électrique des transistors aux SET. La charge critique est la charge qu'il faut modifier sur un nœud électrique pour modifier son état logique. Puis une étude de sensibilité géométrique montre les surfaces sensibles, dans lesquelles si un impacte a lieu peut entrainer un SET. Finalement une étude temporelle permet de montrer si un état logique est plus sensible qu'un autre pendant le cycle de conversion. Au niveau transistor il a été conclu que les transistors PMOS sont moins sensibles que les NMOS. Aussi les transistors de type LVT sont moins sensibles que les SVT et HVT, les HVT étant les plus sensibles. L'étude sur des fonctions NOR2 et NOR8, composantes de la fonction combinatoire CLK Generator, ont montré que plus un nœud a des transistors en parallèle plus il est sensible. De plus, des transistors en série sont sont de plus en plus robustes au fur et à mesure qu'ils sont placés loin du nœud de sortie de la fonction. L'étude géométrique a montré que l'état logique "1" à la sortie de la fonction est le plus sensible car les sections critiques (surfaces sensibles) qui peuvent entrainer un SET sont plus importantes lors de cet état logique comme peut être aperçu dans la figure ci-dessous.

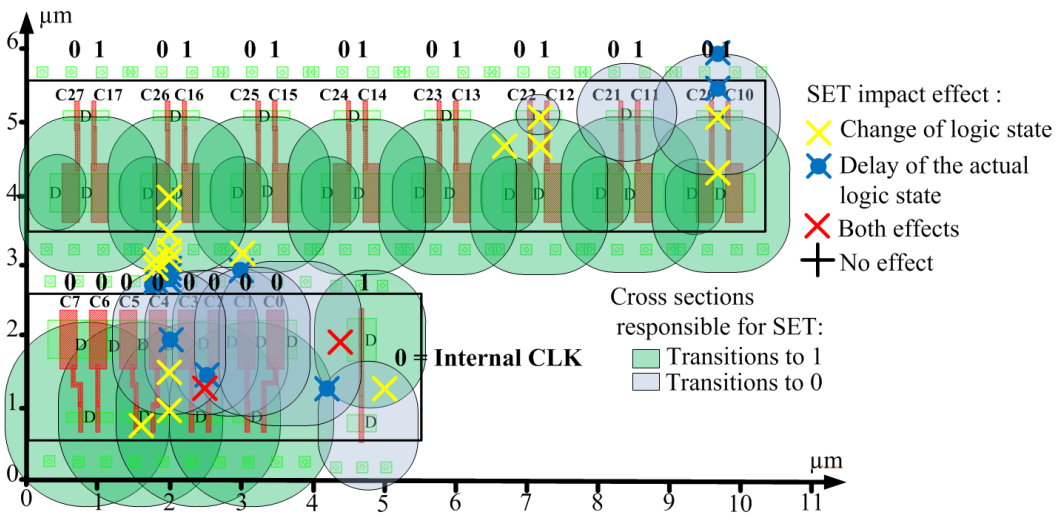


Figure 2: Cross sections and SET effects depending on the location of the impacts for the last iteration when *Internal CLK* is "0".

L'analyse temporelle a montré deux choses. La première est que l'état "1" est aussi le plus sensible dans le temps. Et l'autre est que le 19% du temps du cycle de

conversion est sensible à l'apparition d'effet prolongés de changement d'état qu'on appelle SEU. Un SEU est un SET qui a été verrouillé par un élément mémoire et donc une erreur que dure au moins le temps d'un cycle d'horloge.

Cette étude montre les différents aspects à prendre en compte et qui compliquent le durcissement de la fonction elle même. Dans l'idéale une option pour durcir la fonction combinatoire sera un circuit qui puisse être placé en aval, dont les sections critiques ne peuvent pas d'intercepter avec celles du CLK Generator et qui n'entrainerai pas de surcoût en terme de délai de propagation, de consommation de puissance et de surface.

Chapitre 3 Techniques de durcissement contre les radiations Les techniques de durcissement contre les radiations peuvent se classifier sous deux grandes familles: le durcissement technologique et le durcissement par conception. Ceci est montré dans la figure ci-dessous.

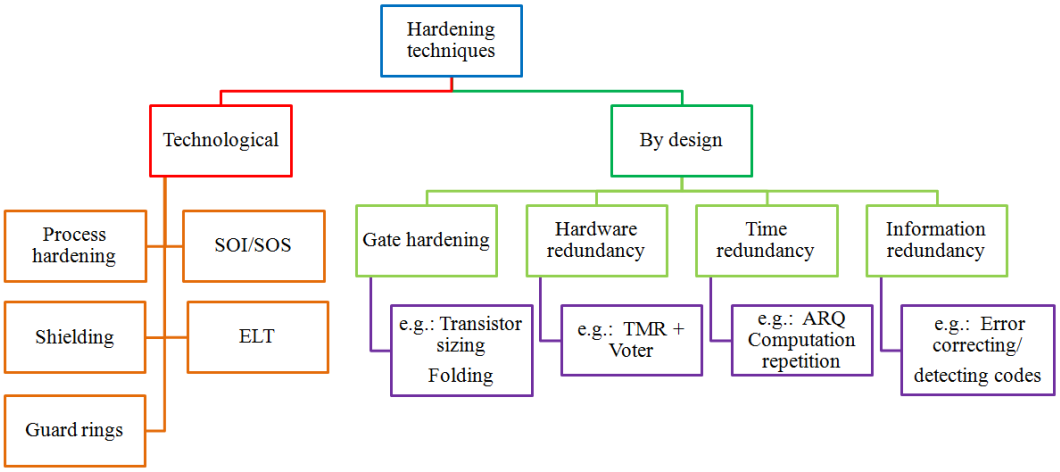


Figure 3: Classification of the hardening techniques.

Les techniques de durcissement technologique se centrent dans le durcissement contre la détérioration par dose de radiation et contre l'activation du transistor BJT parasite intrinsèque à la technologie CMOS. Ces techniques se focalisent dans l'évitement des fautes (Hard ou Soft) Ces techniques emploient des stratégies de purification de processus de fabrication, d'implantation de silicium sur isolant (SOI), d'ajout de couches protectrices (Shielding), de redesign de transistors (ELT) et des anneaux de garde. Ces techniques entrainement un surcoût de la manufacture des circuits imprimés. Ce surcoût peut aller du 10 % du prix initial jusqu'à 50% de plus. L'alternative à ce type de durcissent sont les techniques de durcissement par conception. Ces dernières se centrent dans la protection contre les erreurs soft et peuvent être appliquées dans des technologies CMOS traditionnelles sans besoin

du surcoût du durcissement technologique. Le durcissement par conception peut intervenir tout autant au niveau transistor qu'au niveau système, en passant par le niveau fonctionnel. Les différentes stratégies doivent faire des compromis entre des surcoûts de délai de propagation, consommation de puissance et de surface. Pour des stratégies au niveau transistor un surcoût de surface est à prévoir. Dans le cas des techniques de redondance matérielle il y a un surcoût de surface et de puissance de consommation. Les techniques de redondance d'information entrainent des surcoûts de surface, de délai de propagation et de consommation de puissance. Finalement les techniques de redondance temporelle échangent le surcoût de surface par le délai de calcul.

Pour apporter une solution de durcissement à la fonction combinatoire de départ les techniques de durcissement par conception semblent une alternative intéressante pour éviter le surcoût d'une technique de durcissement technologique. Malgré le durcissement apporté par ces techniques la plupart d'entre elles ne sont pas auto-immunes contre les effets des radiations, et vu que les SET se manifestent plus la technologie CMOS est réduite ceci est un souci.La question *Qui garde les gardiens?* se pose donc. La seule technique complètement auto-immune est la triple redondance matérielle avec redondance triple de voteur. Malheureusement cette technique requiert la triplication de fonctions ou de systèmes, ce qui entraine la triplication de la surface et de la consommation de puissance. Il serait donc judicieux de trouver une alternative. La stratégie de filtrage temporel, sous catégorie de la redondance temporelle, consiste à placer un filtre de SET entre une fonction combinatoire et un élément séquentiel ou une autre fonction combinatoire. Ce filtre est constitué par un C-element et un buffer de délai (voir figure suivante).

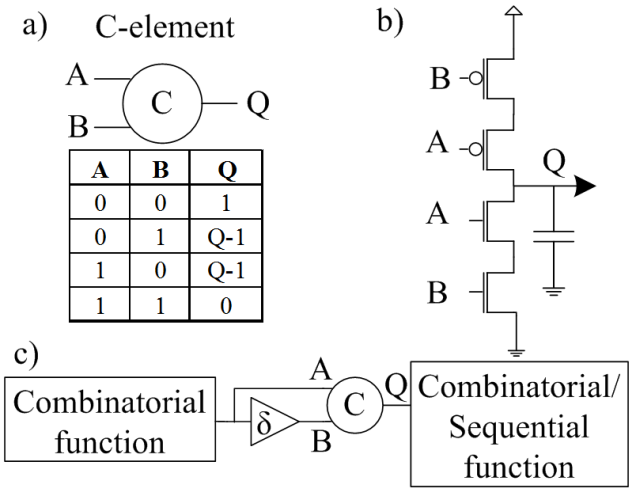


Figure 4: a) C-element symbol and truth table, b) C-element structure, c) Temporal filter structure in a system.

Le C-element a la particularité de se comporter en inverseur lorsque ses entrées sont identiques et en élément mémoire lorsque ses entrées sont différentes, préservant ainsi le dernier état logique. Le buffer de délai est placé en amont du C-element, sur une des ses entrées. Il existera ainsi un décalage du temps de délai entre les deux entrés. De cette façon sont filtrés les perturbations qui ont une durée inférieure à celle du délai du buffer. Cette solution requiert très peu de surface et consomme très peu de puissance du fait de la petite quantité de transistors. La seule contrainte est que le C-element lui même n'est pas durci et si un impacte de radiation survient une erreur peut se propager.

Chapitre 4 L'approche du C-élément avec Détection et Correction (CDC)
Dans le but de durcir le filtre temporel à base de C-element, l'architecture de détection et correction (CDC) a été développée. Cette architecture est montrée sur la figure suivante.

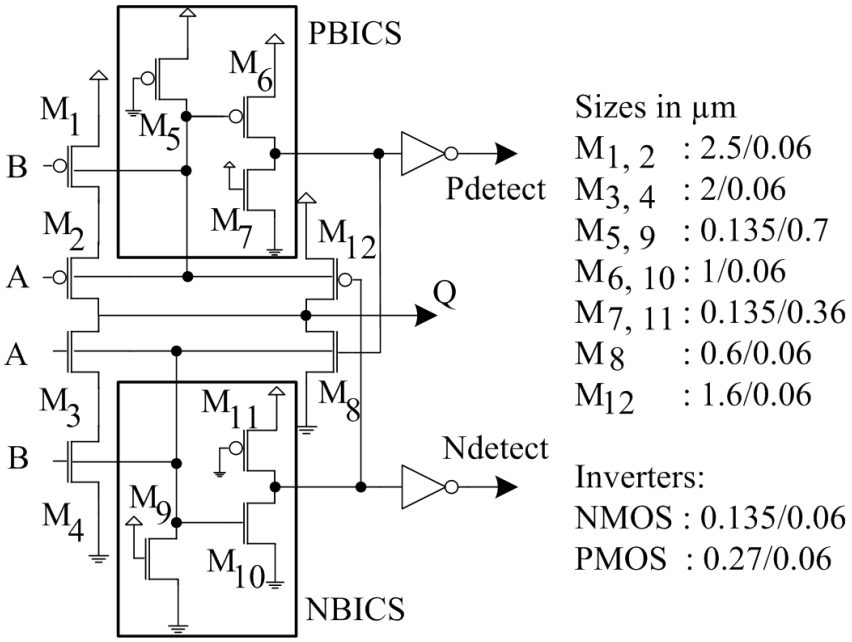


Figure 5: C-element with an SET detection and correction (CDC) feedback control system.

L'architecture du CDC durci le C-element du filtre en ajoutant des capteurs BICS et des transistors de compensation. Les BICS, détectent un changement d'état logique à cause d'un impacte de radiation. Ils sont connectés de façon a capter un courant parasite dans le substrat. Il s'ensuit une rétroaction pour compenser ce changement d'état logique par les transistors de compensation. Cette compensation

rapide évite la propagation de l'erreur. Ces transistors sont taillés de manière que s'ils sont activés par erreur ils ne changent pas l'état logique. Avec le CDC on protège directement le nœud de sortie du C-element. Un grand avantage de cette architecture est que les transistors ajoutés au C-element ne s'activent que lorsqu'un impacte de radiation a lieu, permettant ainsi d'économiser de l'énergie. De plus, les signaux des BICS pour la rétroaction, accompagnés par le signal de sortie, peuvent être utilisés pour l'encodage d'information pour plus de durcissement. La logique de décodage doit être implémentée sur l'élément séquentiel suivant et peut entrainer un coût supplémentaire de conception.

Le filtre CDC a été comparé avec d'autres filtres de l'état de l'art. Pour faire une comparaison de différents circuits des métriques ont été établies pour estimer le gain en robustesse par rapport à ce qui doit être payé en terme de Surface, Surface de Drain Sensible et consommation de Puissance. La comparaison de performances des différents circuits en schématique a montré l'efficacité du CDC vis à vis de la consommation de puissance et de la robustesse apportée au mode mémoire.

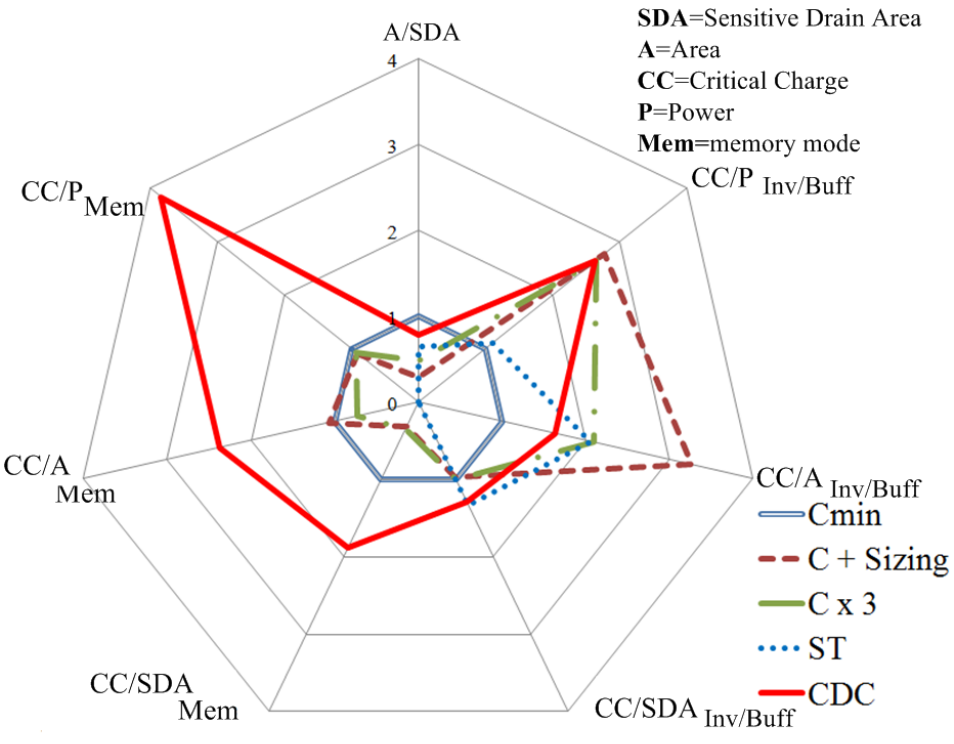
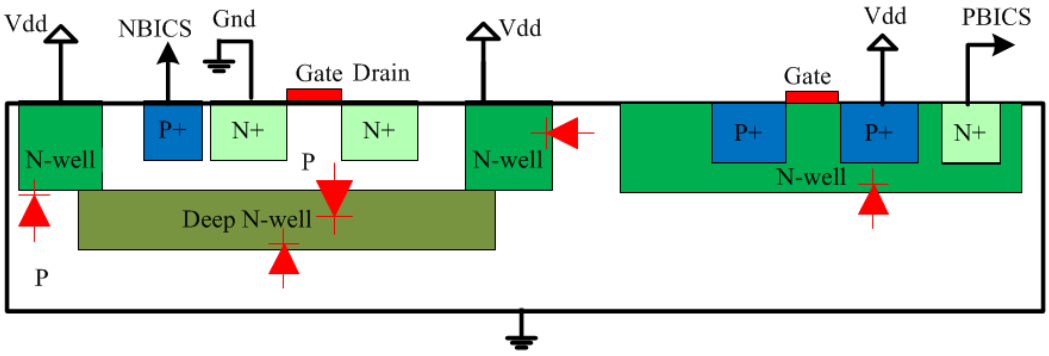


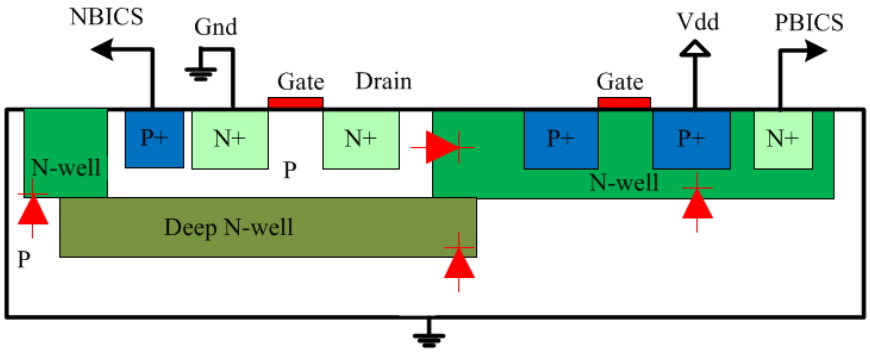
Figure 6: Performance metrics for the different hardening techniques.

Chapitre 5 Vers une implémentation sur silicium du C-élément avec Détection et Correction (CDC) Une analyse électrique basé sur les représenta-

tions schématiques des circuits n'est pas suffisante, car lors de l'implémentation sur silicium plusieurs effets parasites peuvent intervenir. Il faut donc étudier la faisabilité de l'architecture CDC. Pour conception du layout il faut tenir en compte l'isolation des substrats qui sont captés par les BICS des circuits environnants. Les transistors PMOS sont par défaut isolés grâce au caisson N-well qui les contient. Pour les transistors NMOS il faut donc créer un caisson de substrat P isolé du reste, pour cela il faut créer un caisson avec un deep N-well comme le montre la figure suivante. Ce caisson introduit une diode parasite qui devient inhérente à l'implémentation en technologie CMOS. De plus les contraintes de conception d'un caisson avec deep-N Well génèrent un importante surface de circuit additionnelle.



a) Separation between the NMOS bulk and the PMOS bulk



b) Contact between the NMOS bulk and the PMOS bulk

Figure 7: Deep N-well diode connections between two configurations of enclosure for an NMOS transistor.

Cette conception a in profond impact sur la performance du circuit et il faut donc faire des modifications pour arriver au mieux aux performances envisagées. Le circuit extracté du CDC initialement conçu possède un temps de réponse beaucoup trop lent, et n'arrive pas a corriger les SET à temps. Deux causes sont les

responsables de ce soucis: les charges parasites ne sont pas évacuées rapidement et le BICS est activée trop longtemps, et le temps d'activation du signal de rétroaction est beaucoup trop long. Pour cela les transistors des BICS ont été modifiés pour permettre une évacuation plus rapide du courant parasite vers la source est la masse et une réponse plus rapide de la rétroaction même sous l'effet des condensateurs parasites.

Le filtre CDC avec ls modifications liées au layout a été comparé en extracté avec les autres filtres de l'état de l'art. Par sa construction le CDC est la solution qui a la plus petite surface sensible de drain par rapport à la surface totale de circuit. De plus c'est aussi la solution avec un buffer en entrée qui introduit le moins de délai de propagation pour la robustesse apportée. En termes de charge critique et de consommation de puissance sa performance est comparable à la technique de format (Cx3). Aussi en mode inverseur, le CDC propose une performance comparable aux autres techniques pour la métrique de charge critique par rapport a la surface de drains sensibles. Si bien l'augmentation de surface es conséquente en relation aux autres filtres temporels de l'état de l'art, sa surface reste néanmoins insignifiante par rapport à la surface du convertisseur.

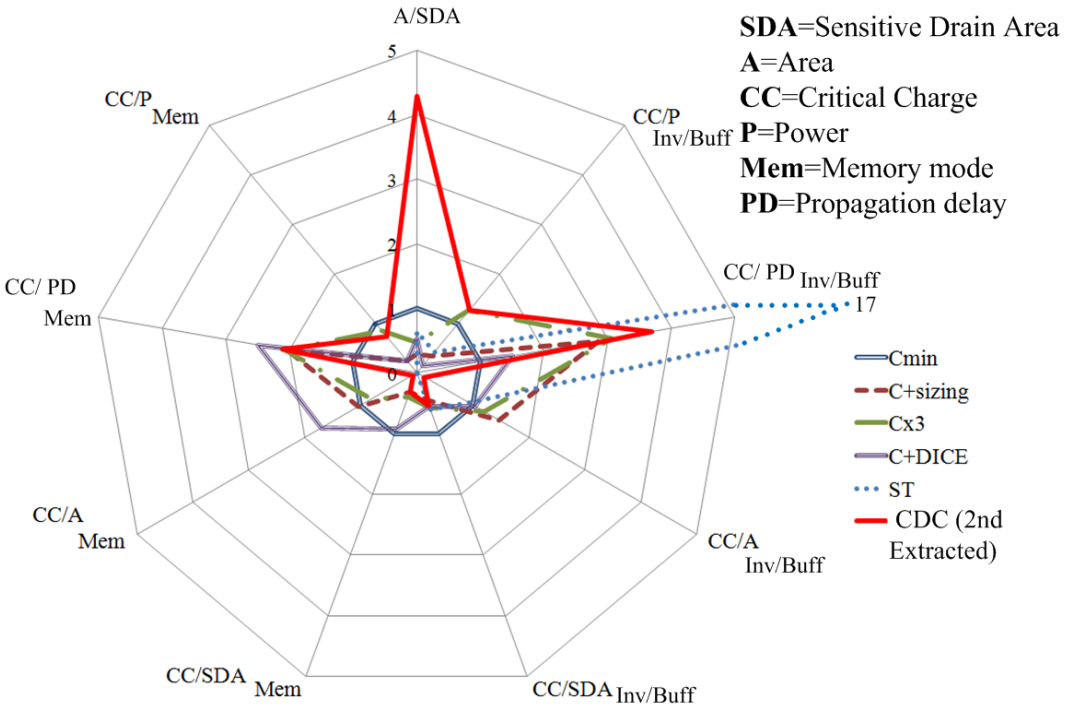


Figure 8: Performance metrics for the different hardening techniques based on their layout's extracted circuits.

A cause du l'augmentation de la taille du CDC par son layout, on peut se demander si la surface est comparable a une technique de redondance matérielle. L'utilisation du CDC pour le cas de la fonction combinatoire étudiée comme moins de puissance et nécessite moins de surface qu'une triple redondance matérielle.

Conclusions Le but de cette thèse est de répondre à la question *Qui garde les gardiens?* dans le contexte des techniques de durcissement par conception contre les radiations. Dans le premier chapitre nous avons exposé les origines des radiations cosmiques et des erreurs soft et nous avons obtenu un modèle pour la simulation de l'impacte de radiations ionisantes sur les transistors. Dans le chapitre 2, nous avons choisi un CAN SAR de basse consommation comme circuit d'étude. Nous avons pu voir la complexité des mécanismes structurels qui génèrent des SET nous avons conclu qu'au lieu de re-concevoir notre fonction combinatoire d'étude il était plus judicieux d'opter pour une option en aval de cette fonction. Le chapitre 3 expose un état de l'art des techniques de durcissement contre les radiations et a montré que des techniques de durcissement par conception peuvent être utilisées comme alternative aux techniques de durcissement technologiques, plus chères. Par contre les techniques de durcissement par conception, si bien augmentent la fiabilité du système sont sensibles aux radiations à leur tour et donc la question *Qui garde les gardiens?* se pose. Le chapitre 4 expose la solution apportée dans cette thèse avec l'architecture de filtre à SET (Filtre temporel) appelée CDC pour C-element avec détection et correction. Cette architecture permet de detecter le courant parasite causé par une ionisation dans le substrat des transistors MOS et déclencher une rétroaction pour compenser la perturbation avant sa propagation. Cette architecture permet aussi l'encodage d'information pour plus de robustesse. En comparaison avec d'autres filtres de l'état de l'art, le CDC a l'avantage de la faible consommation de puissance pour la robustesse apportée. Le chapitre 5 se centre dans la faisabilité de la solution et propose un layout pour l'implémentation de silicium. Le circuit extracté du layout doit tenir compte de changements pour compenser les effets parasites pour s'approcher des performances du circuit en schématique. Malgré ces parasites, le CDC conserve son avantage en terme de consommation de puissance et de court temps de propagation face aux autres architectures de l'état de l'art.

Introduction

During the times of the first digital computers, the ENIAC and the Harvard Mark, in the late 1940's, the hardware errors of the computers were generally caused by vacuum tubes burns and by insects that could cause shorts in the circuitry; giving the origin of the use of "bug" in informatics and electronics. Since then, the reliability of hardware has been a concern. At that time a vacuum tube failed about every two days and had to be replaced [ENI06]. Nowadays, if an error occurs it impossible to replace an integrated transistor inside a chip. So there is a need for local strategies for circuit hardening. Also the sources of those hardware errors have changed from bugs and tube burns to ionizing radiation, electronic noise, electrostatic discharges among others. Radiation can cause either transient errors (soft errors) or permanent component failures (hard errors). The International Technology Roadmap for Semiconductors (ITRS) stated that, below 65nm CMOS Technology [Int11], the reliability of the electronic circuits is seriously threatened. The soft error susceptibility increases exponentially as the supply voltage decreases. Also the susceptibility decreases linearly as the area of transistors decreases. [DW11]. Studies have shown that the soft error rate (SER) for 40nm SRAMS's cmos bulk technology is 30 % higher than the 65nm SRAM and almost the same as 90nm SRAM [DW11]. But not only memory cells and sequential logic si affected, the increase of operating frequencies increases the vulnerability of combinatorial logic [BBB$^+$97]. For recent technologies the combinatorial SER can be anywhere between 20 to 30% of the latch SER at 500MHz. For higher frequencies the combinatorial logic can be comparable or can even exceed that of the larch [MGA$^+$14].

Many radiation hardening strategies have been developed over the years. Some of them are focused on technological hardening, and others on hardening by design. The technological hardening is applied during the integrated circuit's fabrication process to harden the physical properties of transistors against ionizing radiation. This type of hardening is expensive an contributes from 10 to 15% of the manufacturing cost [WN01]. An alternative to the cost of such hardening, is the hardening by design. In this type of hardening, the circuits are created to withstand some

level of ionization without the need to change the fabrication process. In general, this technique places additional circuitry to add redundancy to protect information. Since those "guardian circuits" are made of the same technology as the rest of the circuit, they can be victims of the same threat that is ionizing radiation. Given that condition the question *who guard the guardians ?* can be asked.

This work wants to give an answer to that question. With that purpose in mind, the first step will be to know the origins of these ionizing radiations and the mechanisms that cause the failures in the circuits. Also, to be able to simulate and validate the future solution, a model for the radiation impact will be established. This model will provide a realistic representation of the phenomenon. Those aspects are treated in Chapter 1.

Chapter 2 will focus on putting into context a radiation impact with an electronic system. In this case it will be a low power SAR analog to digital converter (ADC). This type of system mixes analog, synchronous and asynchronous circuits in one system. This diversity can give rise to variety of outcomes in one single system. Another aspect to take into account is that the circuit is conceived for low power applications, and low power is one of the most challenging aspects in the electronic industry. This chapter will explore the vulnerability of such a system and will determine a potential critical circuit. Using the radiation impact model from Chapter 1, an electrical simulation methodology will be established to study the sensitivity to radiation impacts of that critical circuit under three aspects. The first will be determining the electrical sensitivity, using the concept of critical charge. The second will be studying the geometrical sensitivity, using the concept of cross section (or sensitive area). And finally will be analyzing the temporal sensitivity to determine if a logic state is more sensitive than the other over time. The whole study will give the criteria that a hardening solution will have to fulfill in this case study.

After having selected a target circuit that needs hardening, it will be imperative to explore the existent solutions and thus a state of the art of radiation hardening techniques will be exposed. This will be part of Chapter 3. It will show the differences between the technological hardening and the radiation hardening by design. Thanks to this state of the art, a discussion about the stakes for a radiation hardening solution that can answer the question *who guards the guardians ?* in the context of the low power SAR ADC will take place. This discussion will highlight a particularly interesting hardening strategy called temporal filtering. The feedback concept is used by several temporal filters to achieve some degree of self-hardening, but it still has its limitations.

The solution given in this work, the filter with C-element with Detection and

Correction (CDC), will be presented in Chapter 4. The CDC's architecture will be used to harden a temporal filter itself with the idea of a self-healing system using feedback. This solution will take the advantage of the filtering properties, but will add the detection of the ionizing impacts, a feedback compensation and the possibility to encode the information of the filter for further hardening. The CDC will be simulated and compared to other state of the art temporal filters initially based on parasitics free circuits. This comparison will use performance metrics that will take into account what has to paid in circuit area and power consumption to achieve the hardening.

Finally, Chapter 5 will focus on the feasibility of the CDC and the impact of the extracted parasitics in its performance. A discussion on how the CDC solution can be implemented on a layout will lead to several options of design. To choose the most appropriate layout the parasitics extracted circuits will be compared. The performance of the chosen layout's extracted circuit will be compared afterwards to that of the other state of the art filters using the metrics explained before.

The final conclusion will summarize the contributions of this work and will discuss perspectives and future work.

Chapter 1

Cosmic radiation and impact on integrated electronic circuits

In electronics, cosmic radiation can induce, directly or indirectly localized ionization events on circuits capable of upsetting internal data states. Those random errors can be soft or hard errors. If a data error takes place without hardware damage, then this event is called a soft error. If the data error is accompanied by hardware damage then this event is considered as a hard error. The most well known soft error types are Single Event Transient (SET) and Single Event Upset (SEU). A Single Event Transient is a voltage spike, at a given node of an electronic circuit, which can induce a change in the logic state. A Single Event Upset is a latched SET.

To comprehend the origin of those effects an explanation of the cosmic radiation phenomenon will be done. Then the different of this radiation on transistors will be explained. Finally the modeling of the interaction between an ionizing particle and silicon will be detailed followed by a discussion on the soft error cross section.

1.1 Cosmic ray phenomenon

In order to appreciate the importance of the impact of cosmic radiation on electronic circuits a brief summary of cosmic radiation in history will be presented. A description of the phenomenon will follow along with an example of calculation of the soft error rate using the cosmic rays flux. Then the effects of the ionizing radiation caused by α particles and cosmic rays will be exposed.

1.1.1 Cosmic radiation in history

After the discovery of radiation by Henry Becquerel in 1896, it was generally accepted that the ionization in the air was generated by radiation sources on the ground. Nevertheless, during the following two decades experiments of ionization

measurements showed that air ionization increased with altitude. In 1909, Theodor Wulf fabricated an electrometer to measure the levels of ionization created by radiation. He used it to measure the difference of radiation between the top and the bottom of the Eiffel Tower [Hö13]. In 1912 and 1913, Victor Hess (1936 Nobel Prize in Physics) and Werner Kolhöster did measurements at higher altitudes. This led to the cosmic origin of those radiations and the Sun was proposed as one of the radiation sources, after measurements done during an almost complete solar eclipse. In 1925 the terms "cosmic rays" were employed for the first time by Robert Millikan, who confirmed their extraterrestrial origin.

In 1954 soft and hard errors made their appearance in electronic equipment for surveillance of nuclear tests. Also during the space programs of the 60's those anomalies were observed. Nevertheless, the origin of those anomalies was uncertain. Series of studies took place to determine the cosmic ray flux, their composition and the damage they can cause in circuits. At the end of the 70's Timothy C. May and M.H. Woods studied the influence of α particles in circuits [MW79]. James Ziegler studied the influence of cosmic rays [ZL79]. Their works are the basics of the recent studies on the subject of soft errors.

1.1.2 DESCRIPTION OF THE COSMIC RAY PHENOMENON

James Ziegler explained intensively the cosmic ray phenomenon in [Zie96]. His work will be the base for the description that will follow. Cosmic rays are very high energy particles created in space by nuclear reactions in stars, in supernovas, in pulsars and explosions in the galactic nucleus. There are different types of cosmic rays and they are categorized as follow:

- **Primary cosmic rays**: galactic particles that enter the solar system and can hit the Earth. Solar cosmic rays, the particles generated by the Sun and contained in the solar wind, are considered as primary cosmic rays.
- **Secondary cosmic rays**: particles in the Earth's atmosphere and produced by the interaction between primary cosmic rays and the atoms in the atmosphere as illustrated in Figure 1.1. Those interactions create cascade reactions and generate more particles (e.g. neutrons, neutrinos, electrons).
- **Terrestrial cosmic rays**: Particles that finally hit the Earth. Less than 1% of the terrestrial particles are primary cosmic rays. The other 99% of particles is mostly composed of third to seventh generation particles.

In our galaxy, the cosmic rays mean lifetime is about 200 million years. They are considered isotropic and they are composed of 92% of protons, 6% of α particles

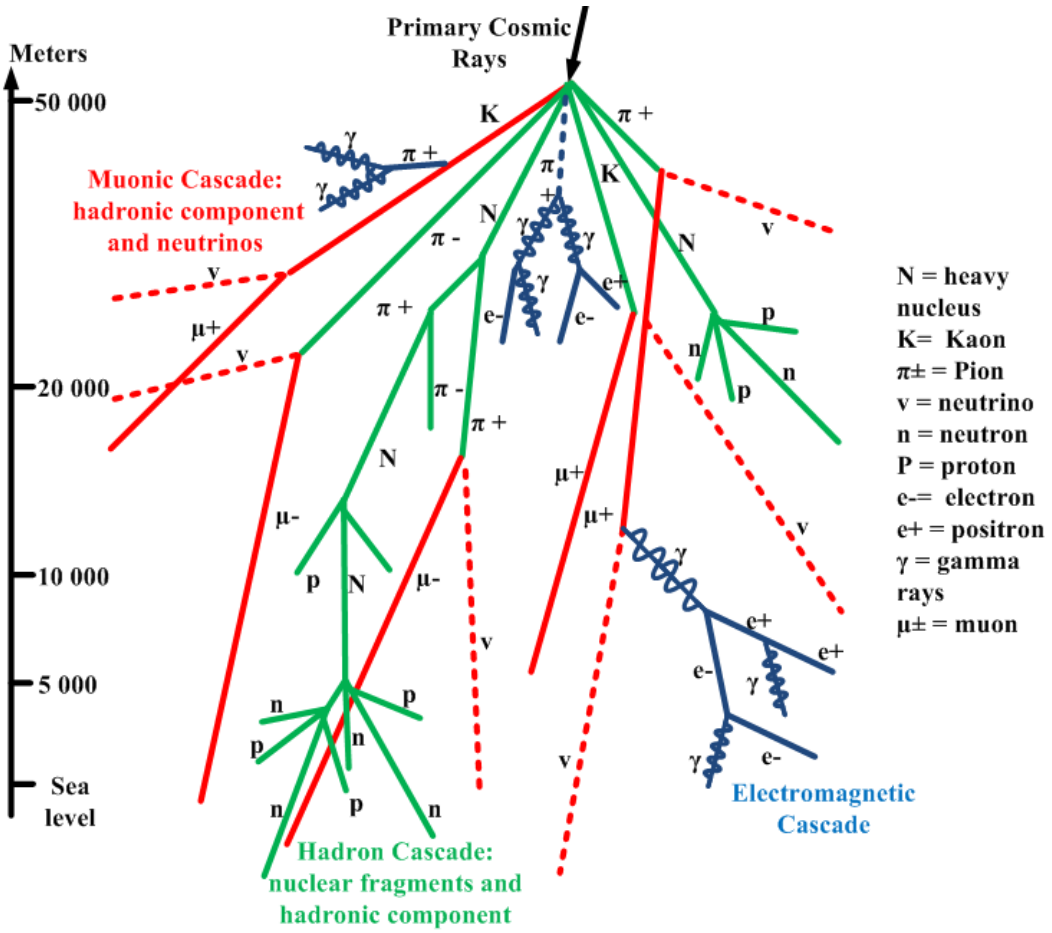


Figure 1.1: Showers of cosmic ray reactions with particles of the atmosphere [Clo02].

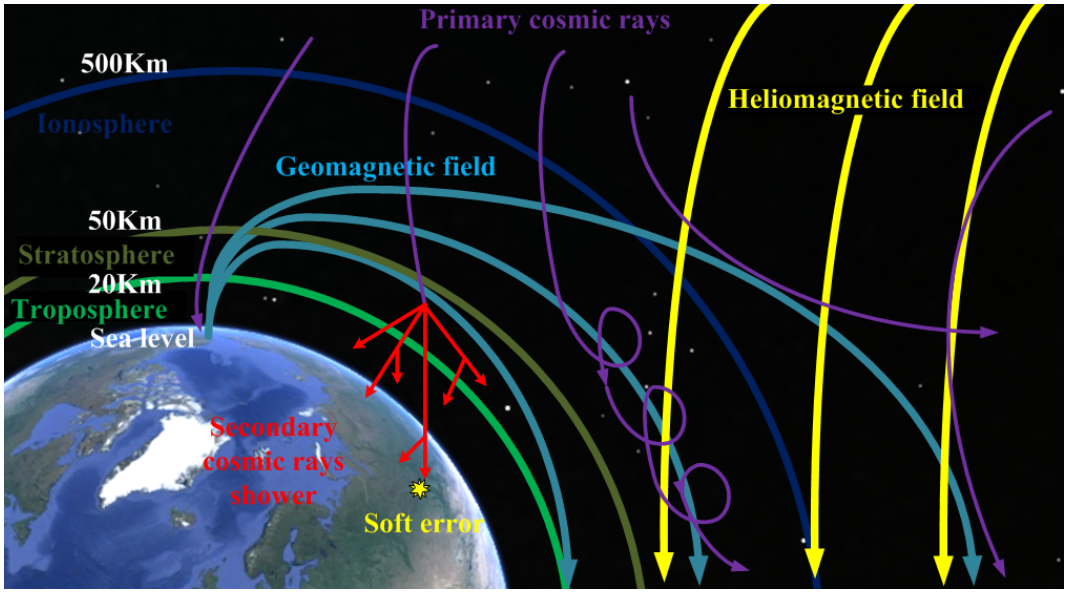


Figure 1.2: Macroscopic mechanism to generate a soft error [Nak08].

and 2% of heavy atomic nuclei. The mean galactic flux is 100 000 $particles/m^2s^{-1}$. In contrast, the flux at sea level is only 360 $particles/m^2s^{-1}$. Many of the cosmic rays from outside of our solar system are kept away by the Sun's magnetosphere, also called heliosphere as shown in Figure 1.2. But most of the primary cosmic rays are deflected by the Earth magnetosphere. The ones that are not deflected enter the ionosphere and wander in the Van Allen belts [Nak08]. Some very energetic primary cosmic rays may enter to the Earth's stratosphere and troposphere.

Cascade reactions begin at 50 km of altitude with particles entering the stratosphere with an energy over 1 GeV, and the maximum density of reactions is reached around 18 km at Pfotzer maximum [Nor96]. After all these cascades, sea level cosmic rays are composed of 94% of neutrons, 4% of pions and 2% of protons. Actually muons are the most abundant particles but they are unstable and only have a lifetime of 2μs. The neutrons originated in the atmosphere are created by two mechanisms [HCL61]. The first is the direct collision between cosmic rays and particles in the atmosphere; they produce neutrons with energies between 1 MeV and 1 GeV. The second is the emission of a neutron by de-excitation of previously excited atmosphere atom. Figure 1.3 shows the spectrum of terrestrial cosmic rays at sea level at New York city [Zie96]. The flux is called differential because it is calculated based on the difference of altitude between the wanted place and a reference known location flux. In Figure 1.3, the neutron's spectrum is the largest, and they are the most common particle at low energies. For higher energies the flux of muon can be greater than

that of the neutrons. Protons and Pions appear in the spectrum for energies higher than 100 MeV and their flux is smaller than that of neutrons. For particle energies around 1000 MeV the flux of protons and neutrons is very similar.

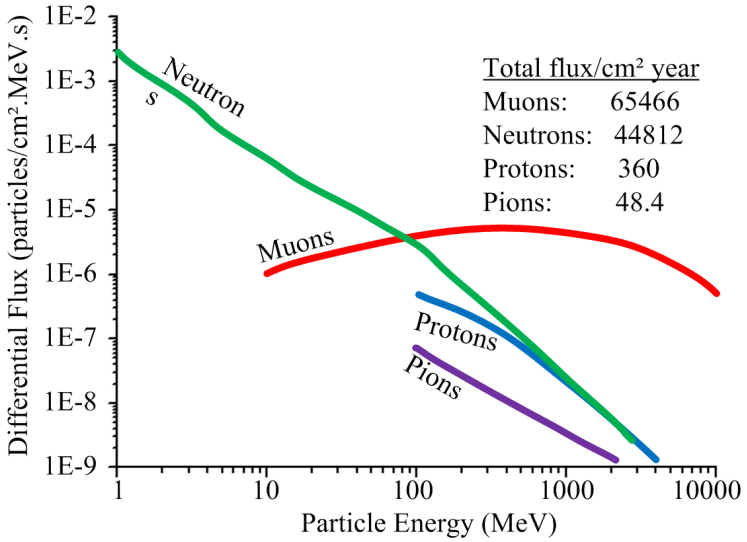


Figure 1.3: Theoretical spectrum of cosmic rays at sea level at New York city [Zie96].

Since electronic circuits can be present at any altitude and location, it is important to know the flux of neutrons, because they are the dominant particle to cause soft errors. The flux of terrestrial cosmic rays varies depending on the Sun cycle and the shape of the Earth's magnetic field. The Sun's cycle is the periodic change of the Sun's activity, which has an average duration of 11 years. Since the Sun's intensity over time has a sinusoidal shape, the peak of intensity is called *Active Sun* and the minimum intensity is called *Quiet Sun*. During the period of Quiet Sun, the number of sunspots is higher than during the Active Sun period. The impact in the flux of cosmic rays is a variation of 20% between a Quiet Sun and an Active Sun. When the Sun is Active the Sun's magnetic field is increased, shielding the Earth against intra-galactic cosmic rays. During this period the flux at sea level can be reduced by almost 30 %.

The terrestrial cosmic ray flux varies not only with altitude but also with latitude [NB93]. Figure 1.4 shows those variations of flux. As the latitude is concerned, the flux is more important at the poles (actually at the magnetic poles) than at the Equator. That is why Auroras are observed near the poles.

All the information above is useful to establish the Soft Error Rate (SER) of a circuit. The SER is the rate at which a device encounters soft errors. It is usually

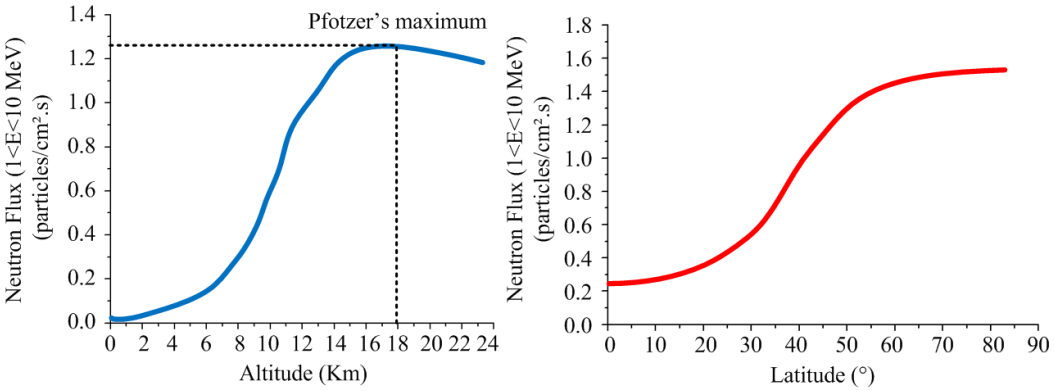


Figure 1.4: Neutron's flux variation in altitude (left) and latitude (right) for neutrons with energies between 1 and 10 MeV. On the left, the neutron flux is based on aircraft and balloon measurements [Nor96]. On the right, neutron flux based on aircraft measurements and the vertical rigidity cutoffs of Smart and Shea [SS84] and [NB93].

expressed in terms of failures in time (FIT).

1.1.3 Soft Error Rate calculation based on the particle flux

The following explanation is based on Ziegler's works [Zie96]. To calculate the SER at a given location, the first step is to know the neutron flux at that location. The flux can be calculated thanks to a measured flux at another altitude. The calculation of the flux change for a given particle with altitude is the Equation 1.1:

$$F_{Location} = F_0 \exp\left(\frac{H_0 - H_{Location}}{AL_x}\right) [particles/s.cm^2.MeV] \quad (1.1)$$

Where F_0 is the reference flux at a given altitude (or air pressure) H_0, and $F_{Location}$ is the wanted flux at an altitude $H_{Location}$. The AL_x parameter corresponds to the particle mean free path or absorption length.

- Muons: $AL_\mu = 520\ g/cm^2$
- Neutrons: $AL_n = 148\ g/cm^2$
- Protons and Pions: $AL_{p,\pi} = 110\ g/cm^2$
- Electrons: $AL_e = 100\ g/cm^2$

Altitudes have to be expressed in terms of pressure H in g/cm^2 using Equation 1.2:

$$H(A_{Location}) = 1033 - (0.11119 \times A_{Location}) + (4.26 \times 10^{-7} \times (0.3048 \times A_{Location})^2) \quad (1.2)$$

Where $A_{Location}$ is the altitude in meters.

It is possible to find a calculation of the flux, according to the different geographical parameters. For instance, the results of different published work that led to the creation of the web tool *Soft error testing resources* [SEU] thanks to collaborative efforts. The supporting works for those results can be found in these articles: [NSMM89], [MAS], [SS07], [CD00] and [GGR$^+$04]. The results from this tool are compatible with the Joint Electron Device Engineering Council (JEDEC) standard JESD89 [JED06].

When the flux is established, the next step is to estimate the number of errors likely to take place given the surface of a circuit. This is done with Equation 1.3.

$$Soft\,errors/year = (Soft\,Error\,Cross\,Section) \times (Nucleon\,Flux) \times (Unit) \quad (1.3)$$

Where the soft error cross section is the number of events per unit of flux [JED06].

For a device soft error cross section, the dimensions are area per device. The soft error cross section is an intrinsic parameter of a circuit that specifies its response to a particle species (e.g. neutron, proton, pion, heavy ion, etc.). It is measured using a beam of particles produced in an accelerator. In general, the cross section depends on the particle type and energy. It can also be associated to a function of the operating conditions of the irradiated chip (e.g., applied voltage, temperature, etc.). The units commonly used to express a cross section are cm^2/bit, cm^2/Mb or $cm^2/device$.

The nucleon flux is the flux of all the particles that is determined at the location (*cf.* 1.1). The unit factor has to be in relation to the soft error cross section. If the cross section is for example in cm^2/bit then the unit is bit. It depends on the kind of circuit that was tested to obtain the soft error cross section.

A macroscopic view of the cosmic ray phenomenon was presented from the creation of cosmic rays to their arrival on Earth. Now is possible to enter a more microscopic view related to the interaction between ionizing radiation, from cosmic rays, and silicon.

1.1.4 IONIZING RADIATION EFFECTS ON SILICON

In the electronics circuits industry, soft errors have to be cared about, because they have an influence on the reliability of the systems. In addition, with the transistor's integration following Moor's law, circuit's reliability to radiation is diminishing. Where only one transistor was affected by a radiation strike, now several transistors can suffer from one single strike. Soft errors can be generated by alpha particles emitted from radioactive impurities in materials of the packaging, or during the foundry process. Another source of ionization comes from highly ionizing secondary particles produced from the reaction of both thermal and high-energy neutrons with silicon [Bau01].

All along the evolution of circuit's integration, the main sources of soft errors have changed. During the 80's decade, α particles from the radioactivity of the packaging impurities were the main cause of soft errors [MW78]. Figure 1.5 shows the three steps of the interaction of α particles and a PN junction. When α particles penetrate into silicon, they generate an ionization track of electron-hole pairs. This is called direct ionization. Once the ion track is created a parasitic current appears along with the funneling of the space charge region. Finally the remaining charges diffuse to create a current by diffusion. This current is the source of a soft error.

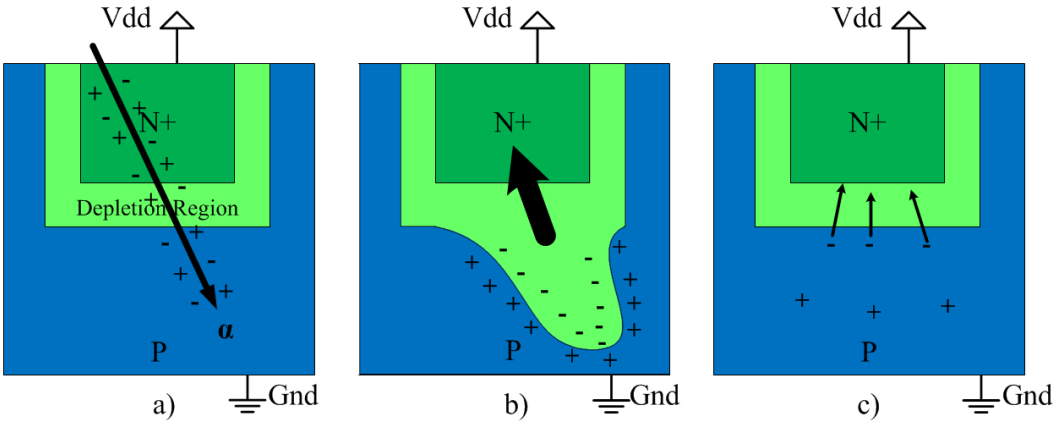


Figure 1.5: Effects of alpha radiation on a PN junction. a) Ionization, b) leakage current and funneling, c) charge collection by diffusion.

Since the 80's, efforts were done to reduce radiation impurities in the packaging materials, and during the 90's the major cause was the reaction between a low energy neutron (thermal neutron) and a ^{10}B boron isotope. Boron is used as a p-type doping and implants species in silicon and was also used in the formation of BPSG (borophosphosilicate glass) dielectric layers. ^{10}B boron isotope is unstable and has a high thermal neutron capture cross section. If a thermal neutron hits the isotope

and it is absorbed, the nucleus fissions, releasing an excited recoil of ^{10}Li lithium nucleus and an α particle as depicted in Figure 1.6 a). A γ photon is emitted from the lithium recoil soon after fission occurs. In this case the ionization is caused by the products of the reaction, thus it is an indirect ionization.

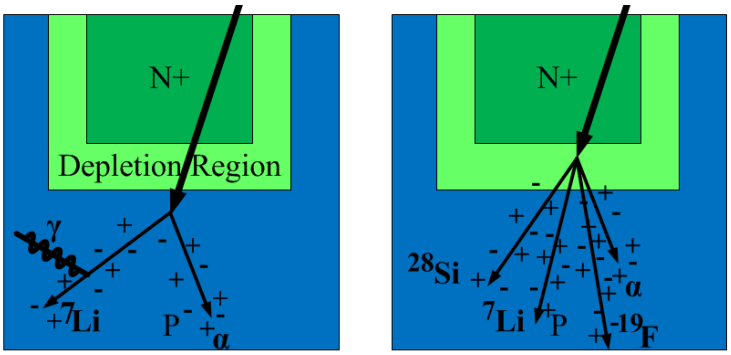


Figure 1.6: Effects of neutron radiation on a PN junction. a) Products of the reaction between a cosmic ray neutron and ^{10}B boron isotope, b) Products of the reaction between a cosmic ray neutron and a silicon nucleus.

Nowadays, the main cause for ionizing soft errors are high energy neutrons (>MeV) [Bau01]. When a high energy neutron collides with a silicon nucleus and breaks it expels different kinds of ionized particles, those particles travel though the silicon lattice, creating electron-hole pairs on a track before they are stopped (*cf.* Figure 1.6 b)). This is another example of indirect ionization. Those ion fragments are from different elements (H, He, Li, Be, B, C, N, O, F, Ne, Na, Mg, Al, Si) [ZBZ13].

The deposited charge by ionization can be calculated from the Linear Energy Transfer (LET). The LET is the energy transferred by an incident particle for the ionization of a material. It is defined as the loss of energy per distance as for a particle with density ρ:

$$LET = -\frac{1}{\rho}\frac{\Delta E}{\Delta x}\ [MeV/(mg/cm^2)] \tag{1.4}$$

The LET can also be expressed in terms of charge deposited along the penetration range. For silicon the conversion factor is:

$$1fC/\mu m = 0.0969 MeV/(mg/cm^2) \tag{1.5}$$

This charge per distance unit was used to compare the influence of α particles and cosmic ray neutrons on the SER.

The influence of α particles and cosmic rays neutron on the SER was studied by Kobayashi et al. [KKKS09]. The results of this work showed that under the technology node of 65nm the α-SER is less significant than n-SER. In addition to that the n-SER is increasing with each new technology node. The average energy of protons generated by the nuclear reaction between cosmic ray neutrons and Si nuclei is approximately 5 MeV. The range of penetration of a proton for this energy is larger than that of an α particle. For instance, an α particle of 5 MeV has a range of 24μm, while that of a proton with the same energy is 200μm. Since the silicon-neutron interaction can produce several protons, and high energy protons traveling further in the silicon lattice can deposit more charge in the material, then those aspects give the advantage to the silicon-neutron interaction over the α-silicon.

One last question remains, what happens with pions and muons? As far as the pions are concerned, they are unstable particles with a lifetime of 26ns and a mass 200 times of the electron. Their flux is about 450 pions/cm^2 and they caused 0.0003 SEU/chip/year in 2004 [ZP04]. Pions do not react much with silicon. Negative pions may react in what is called a pion capture. This takes place when a pion interacts with matter. The negative pion gives his kinetic energy end attaches itself to the nearest nucleus and starts orbiting like an electron. But a pion does not respect Pauli's exclusion principle. This principle says that two fermions (half-integer spin particles like electrons, quarks or neutrinos) cannot share the same quantum state simultaneously. The negative pion has a spin of 0. The pion starts getting closer to the nucleons, by changing its orbital and liberating X radiation. When he is at the fundamental orbital 1-s, because of its mass and the strong interaction he couples with a nucleon. This creates instability and the nucleus fissions itself into high energy fragments. At sea level, the pions capture rate is 8.5pions/cm^3/year, and is estimated that even if all the pions are captured that would only cause 0.05 SEU/year. Their flux is about 100 times smaller than that of the neutrons and their importance in the SER is negligible [Zie96].

Muons are relativistic particles with a mean lifetime of 2 μs, and their number exceeds by 100 times the presence of any other subatomic particle from cosmic radiation at sea level. Muons have two effects on circuits. The first is the muon capture, like pion capture. But in this case when the muon is at the fundamental 1-s orbital, it combines itself with a proton. The nucleus gives then a neutron and a neutrino. The neutron can interact with the nucleus causing secondary reactions. Muon's capture at sea level takes place 510/cm^3/year. The generation of an α particle is about 15/cm^3/year and for heavier fragments is 1/cm^3/year. They cause 0.0006SEU/year [ZP04]. The other effect of the interaction between a muon and silicon is the electrostatic scattering. Muons can cause a nuclear recoil of a

target atom, which generates an ionization. This phenomenon happens at a rate of $7/cm^3/year$ for important charges able to cause SEUs (>100 fC) [Zie96]. Muons can generate more SEUs than pions, but their contribution to the SER is also negligible in comparison with the neutrons.

The parasitic current caused by the ionization being the main phenomenon, is what affects transistors. Keeping that in mind, transistors respond in different ways to this ionization. The induced errors can degrade the transistor performance permanently or temporarily. A classification of the errors is important to confine the research to propose a solution.

1.2 CLASSIFICATION OF THE EFFECTS ON TRANSISTORS

The purpose of this discussion is to give an idea of the types of consequences of radiation on CMOS transistors. Soft errors are only a subset of Single Event Effects (SEE). They are any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike [JED06]. First, destructive SEEs, hard errors will be presented followed by the nondestructive ones, soft errors. The discussion will conclude with the degradation mechanisms caused by radiation.

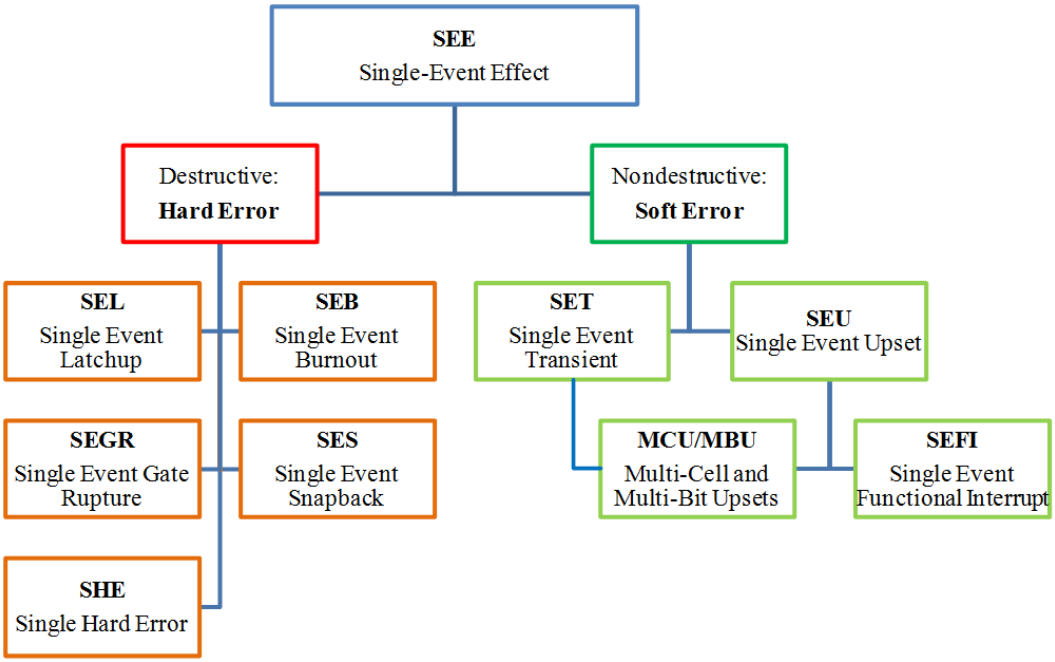


Figure 1.7: Classification of Single Event Effects (SEE) [Lad07].

1.2.1 HARD ERRORS

This type of SEE is an irreversible change in operation of a circuit or a device. This translates into permanent damage to one or more elements of the circuit or the device (gate oxide rupture, destructive latch-up events). This type of error is called hard because there is a permanent loss of data and the component no longer functions properly, even after power reset and re-initialization. Next are going to be presented the different hard errors in CMOS technology.

1.2.1.1 SINGLE EVENT LATCHUP (SEL)

An SEL is a high-current state in a device caused by the passage of an energetic particle near two neighboring PMOS and NMOS transistors. It can activate the parasitic PNPN thyristor structure (*cf.*Figure 1.8) formed by the NMOS-PMOS pair shorting the power to ground. This mechanism can amplify currents to the point where the device fails due to thermal stress. If the effect is not permanent, turning off the power supply disables the thyristor. The channel length and the epitaxial layer thickness play a dominant role on the SEL susceptibility. With the gradual decrease of transistor size new technologies are more vulnerable to this effect [BP96]. In addition to that, there is an increase of SELs at high temperatures [JHBP91].

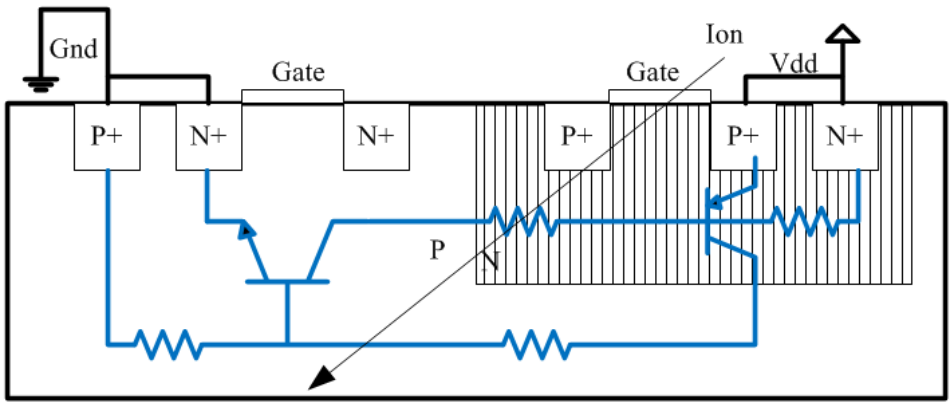


Figure 1.8: Parasitic PNPN structure formed by an energetic particle during an SEL.

1.2.1.2 SINGLE EVENT BURNOUT (SEB)

Mainly affecting high-power MOS transistors, like Vertical Diffused MOS (VDMOS), an SEB takes place when an ion strike turns on the parasitic BJT structure (*cf.*

Figure 1.9), usually in n-channel MOSFETs. The resulting breakdown causes a high-current state and can cause thermal failure of the device [WCHS85]. Those transistors are only vulnerable to SEB when they are in their OFF state, and only when the applied voltages (VDS and VGS) are outside of the normal and safe operating region. When a particle hits, it can creates a high density current. If the voltage decreases in the base-emitter junction of the parasitic bipolar transistor, the transistor is turned on. This happens because of the avalanche current of the collector of the BJT. This can create excessive heating in the junction that can lead to the transistor's burnout.

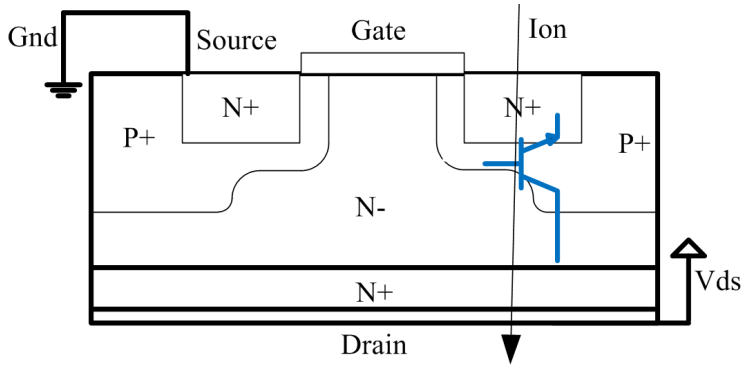


Figure 1.9: Parasitic BJT transistor structure formed by an energetic particle impact in a power VDMOS transistor during an SEB.

1.2.1.3 Single Event Gate Rupture (SEGR)

Like SEB, SEGR mainly affects power MOSFETs. When an ion strikes near the Si/SiO_2 interface of the gate, holes from the ion strike pile up under the gate (*cf.* Figure 1.10). The electric field across the MOSFET gate oxide is increased to its dielectric breakdown. The resulting leakage current can also cause a thermal failure of the gate oxide [TWVT$^+$98].

1.2.1.4 Single Event Snapback (SES)

A single event snapback occurs mainly in NMOS transistors when an ion injects enough current in the drain junction to create an avalanche effect [KK89](*cf.* Figure 1.11). After the passage of an ion through the depletion region, the electron-hole pairs start moving along the field lines. Electrons tend to travel to the drain, and the holes tend to move to the source. However, some holes travel through the p-doping region to the ground. At this moment the parasitic bipolar transistor is turned on.

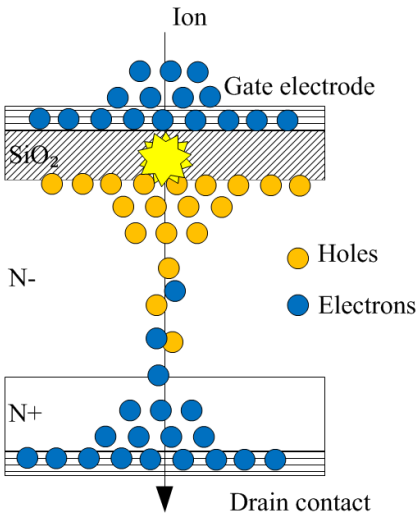


Figure 1.10: Accumulation of charges during an SEGR under the gate of a VDMOS transistor.

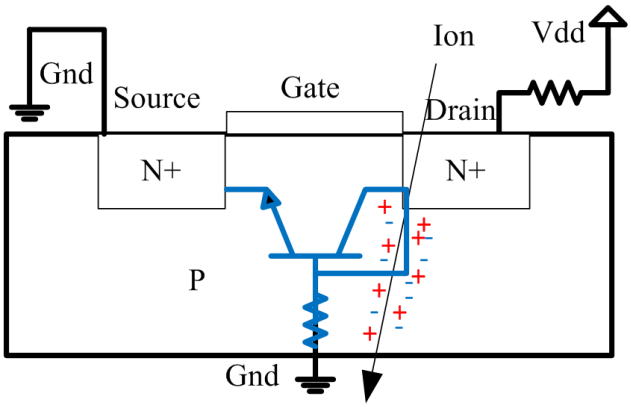


Figure 1.11: Snapback phenomenon activated by the ion track of a high energy particle strike.

An SES can be a regenerative effect but if the phenomenon is sustained by an external current source the excess of current can damage the device. This phenomenon affects MOS transistors and even SOI technologies, which are more radiation resistant [SFCS+03].

1.2.1.5 Single Hard Error (SHE)

In RAM memories, a high energy particle passing through the transistor's gate can leave a dense local deposit of trapped charge that induces a variation in the threshold voltage. This prevents the writing process leaving the SRAM with a stuck bit [DGC+92].

1.2.2 Soft errors

Soft errors are nondestructive functional errors induced by energetic ion strikes. Transistor scaling and lower supply voltage have led to lower noise margins and a smaller amount of charge representing a bit of information. This is expressed in terms of Critical Charge (CC) which is the amount of charge required to change the logic state when the voltage becomes equal to the half of the supply voltage. This scaling trend has increased the susceptibility to soft errors [DSSF10]. The International Technology Roadmap for Semiconductors (ITRS) stated that, below 65nm CMOS Technology, soft errors impact field-level product reliability, not only for embedded memories, but for logic and latches as well [Int11]. The stakes for soft error protection are high for actual and future technologies. Now, the different soft errors in CMOS technologies will be presented.

1.2.2.1 Single-Event Transients (SET)

A Single Event Transient is a voltage spike in a MOS transistor's drain, caused by the charge collection mechanism after a high energy particle creates an ionization track [MW78]. This affects combinatorial logic circuits. As depicted in Figure 1.12, the voltage spike will then propagate through the logic and if the spike is important enough to avoid an electrical masking it can reach a memory element (latch, flip-flop). Since the scaling of technology has increased the sensitivity of CMOS circuits to SETs [DSSF10] is has become a major issue.

1.2.2.2 Single Event Upset (SEU)

Single event upset differ from SET in their affected target and their duration in time. An SEU takes place in a memory element (e.g. latch, flip-flop, RAM cell,

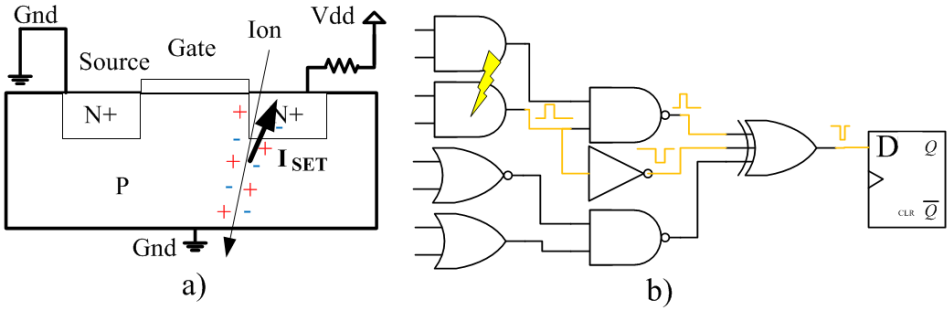


Figure 1.12: a) Ionization current generated by a high energy particle on a NMOS transistor b) Propagation of an SET through combinatorial gates from a single hit on a NAND gate.

asynchronous memory logic) as a consequence of either latching an SET or an ionizing strike hitting the memory element (*cf.* Figure 1.13). Since an SEU is stored in a memory element, the error is no longer transient, and the error can remain several clock cycles, for synchronous logic, or until the next transition edge of an input signal in asynchronous logic.

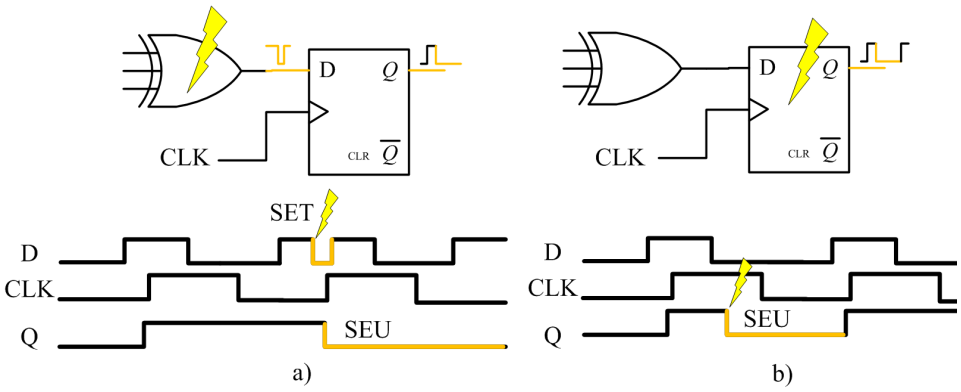


Figure 1.13: a) SEU as a consequence of a latched SET from a combinatorial stage b) SEU as a consequence of an ionization of the memory element.

1.2.2.3 Single Event Functional Interrupt (SEFI)

The SEFIs are a subcategory of SEU errors. This type of error concern not only high-density programmable devices (CPLDs and FPGAs) but also microprocessors, digital signal processors (DSPs), electrically erasable programmable read only memories (EEPROMs), dynamic random access memory (DRAM), and synchronous DRAMs.

A SEFI is a system wide failure [Ini11]. An example of SEFI could be when the Power-On-Reset (POR) is hit by an SEU, which causes the FPGA to reset. This problem is easily solved by touring off and back on the power supply [NS01].

1.2.2.4 Multi-Cell and Multi-Bit Upsets (MCU) and (MBU)

As CMOS technology shrinks, transistors are not only smaller but closer. Due to this trend multiple bits in combinatorial logic and multiple memory cells (e.g. RAM cells) can be affected by one single ionizing event. The charge collection mechanism takes place for the drains near to the impact. As the technology becomes smaller, MBU and MCU rates are increasing [WPC+01].

1.2.3 Degradation Mechanisms

Unlike the hard and soft errors explained earlier, radiant environments create cumulative effects, that gradually degrade the parameters of the transistors instead of an abrupt failure. Two main mechanisms arise, the Total-Ionizing Dose (TID) and the Displacement Damage (DD).

1.2.3.1 Total Ionizing Dose (TID)

Like SEGR, but without the abrupt rupture of the gate, ionizing radiation generates trapped charge in CMOS transistor dielectrics. These trapped charges disturb the threshold voltage. For NMOS transistors the threshold voltage decreases and for PMOS increases. Those trapped charges drive an increase of leakage currents and a degradation of the switching performance leading to a degradation of the lifetime of the device [SSF+08]. Unlike SEE, devices are vulnerable to TID whether or not they are in use.

1.2.3.2 Displacement Damage (DD)

In subsection 1.1.4, was explained the effects of neutrons colliding with silicon, and illustrated in Figure 1.6 b). Results of such collisions are displacement of silicon nuclei and creation of different types of ions. Repeated collisions over time decrease the device performance. The displacements create density defects on the crystal structure of silicon and the ions in the lattice create impurities. Those mechanisms reduce the carrier's lifetime, the carrier mobility and there is even carrier removal. In addition they can increase the leakage current and generate thermal charge [Lad07].

This exhaustive list of effects shows the diversity of errors caused by ionizing radiation and that is why the research in radiation hardening is important for actual

and further transistor technologies. As a starting point, an ionization model has to be established to be able to simulate SEE in CAD tools.

1.3 Modeling the ionization process in CMOS technology

Since ionization is the cause of the SEEs, it is important to know how a device behaves when an ionized particle hits to comprehend the phenomenon, before being able to propose a hardening strategy later. In this section will be presented a methodology for introducing the parasitic current that creates SEEs. Then will be explained the model used in this work to recreate this parasitic current. An application example will be provided. Finally the concept of soft error cross section will be presented along with its saturation property.

1.4 Electric modeling of the ionization process in CMOS technology

The charge collection mechanism explains how an ionizing strike affects the drain of a transistor [MW78]. This mechanism is modeled by the charge collection model introduced in 1978 with Kirkpatrick's work [Kir79]. The objective is to have a simple quantitative model for ionizing particle interaction with silicon, and thanks to this model be able to simulate the parasitic current on the drain of a CMOS transistor. This can be useful for further circuit analysis.

In order to electrically simulate the ionizing phenomenon, an ideal current source with a model of the parasitic current can be used [CP93]. The current source must be connected between the drain and the bulk of each type of transistor to represent the phenomenon (*cf.* Figure 1.14 a)). In addition, the direction of the current must be respected to create the correct transitions (*cf.* Figure 1.14 b) and c)).

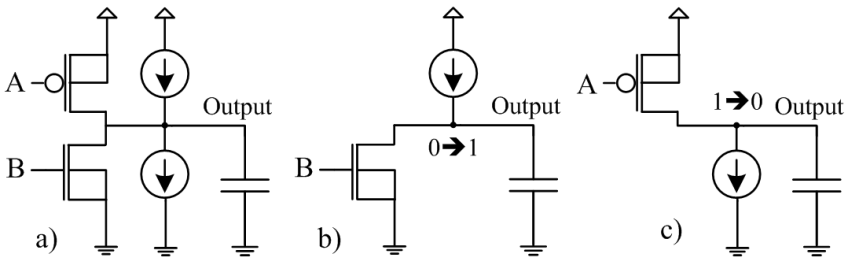


Figure 1.14: a) Placement of current sources to induce SETs for electric simulations, b)Transition from 0 to 1 when the PMOS transistor is OFF, c)Transition from 1 to 0 when the NMOS transistor is OFF.

The charge collection model determines the amount of charge collected on a drain surface given an ionization track and the parasitic current can be deduced. Like α particles ionizing the silicon in Figure 1.5, when an ionizing particle hits the space charge region of a PN junction three stages occur (*cf.* Figure 1.15). At first, the hit creates a track of electron-hole pairs before stopping. Then, a funnel is created. Finally the charged particles diffuse and generate a parasitic current depending on the polarization of the transistor. The resulting current has three components: the current during the funnel creation, the current during the established funnel, and the current of the remaining diffusing charges.

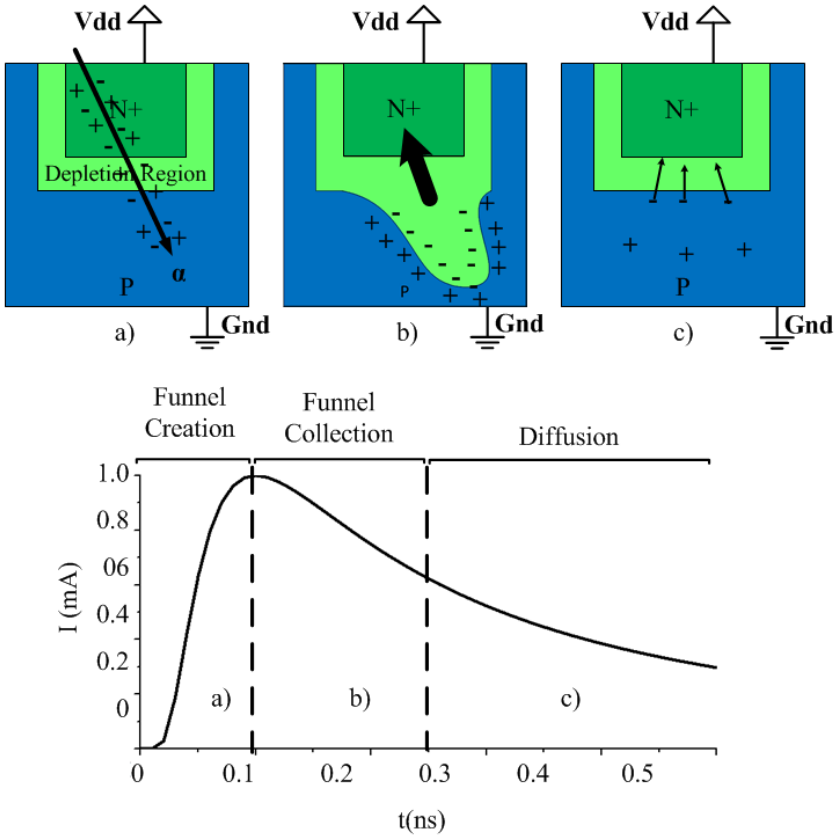


Figure 1.15: Resulting current of an ion passing through the space charge region of a PN junction. a) Ionized track creation, b) Funneling, c) Diffusion of the remaining charges.

Simple current models exist for electrical simulation. As an example the simplified model of C.G. Messenger [Mes82], which gives the current as function of time by:

$$I(t) = I_0 \left(\exp\left(\frac{-t}{\tau_\alpha}\right) - \exp\left(\frac{-t}{\tau_\beta}\right) \right) \tag{1.6}$$

Where $I_0 = \frac{Q}{\tau_\alpha - \tau_\beta}$ is the initial current, with Q the total charge of the ion track, τ_α the collection time of the PN junction and τ_β the time of establishment of the ion track.

Another example, using the I_{max}-t_{max} criterion, is proposed in Merelle *et al.* work [MCP+05]:

$$I(t) = I_{max} \exp(1) \left(\frac{t_{max}}{t}\right)^{\frac{3}{2}} \exp\left(\frac{-3t_{max}}{2t}\right) \tag{1.7}$$

Where I_{max} is the peak of the current and t_{max} is the time to reach the peak.

Even if those models have interesting parameters, that let us simulate the duration and magnitude of the transient current, they lack of the geometric aspect of the phenomenon. With those models it is impossible to see what happens to the current with respect to the distance of the hit, or the orientation of the ion track. It is also impossible to see what happens if two drains or more are affected by the same impact. In order to have a more realistic but simple model of the ionization phenomenon, a model in three dimensions is required.

1.4.1 THEORY OF THE CHARGE COLLECTION MODEL

The charge collection model that will be presented comes from the work of Edmonds [Edm01] and the Diffusion-Collection model used in several works such as Palau et al. [PHC+01]. This model has been coded in MATLAB for simulations. The units of all the physical quantities are shown because they are very important to illustrate the meaning of each quantity.

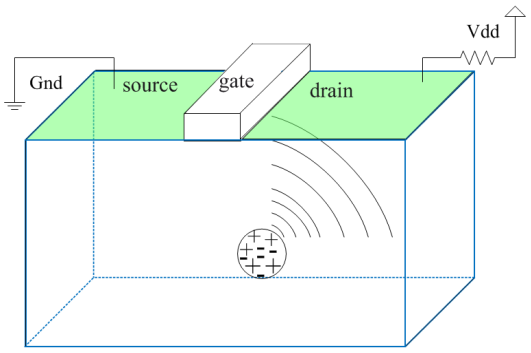


Figure 1.16: Charges diffusing from an ion sphere to the drain.

The first step is to determine the diffusion equation in one point. The diffusion

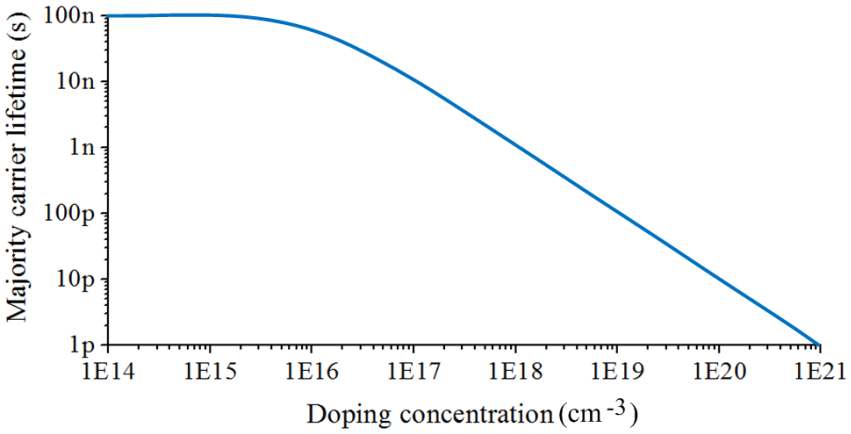


Figure 1.17: Majority carrier's lifetime as a function of the doping concentration.

equation is the solution, for a three dimension case, of the diffusion differential Equation 1.8. The theory behind is not explained in this work but is extensively explained in Lambert's thesis [Dam06].

$$\frac{\partial n}{\partial t} = D.\Delta n + \frac{n - N_0}{\tau} + g \tag{1.8}$$

Where n is the carrier concentration (cm^{-3}), D is the diffusion coefficient ($cm^2.s^{-1}$), N_0 is the initial concentration of carriers at t=0 (cm^{-3}), τ is the carrier's lifetime, and g is the generation function ($cm^{-3}.s^{-1}$).

Carrier's lifetime can be obtained by the experimental work from A. Torres and exposed in Lambert's thesis [Dam06] (*cf.* Figure 1.17). Carrier's lifetime depends mainly on four recombination mechanisms: Radiative Recombination (τ_{Rad}), Auger Recombination (τ_{Auger}), Shockley-Read-Hall (SRH) Recombination (τ_{SRH}) and Surface Recombination ($\tau_{Surface}$). The effective lifetime is obtained from recombination times for each mechanisms following the expression 1.9, as seen in works such as Mohammad Ziaur Rahman [ZR12] and in the thesis of Peter D. Bradley [Bra00].

$$\frac{1}{\tau} = \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Surface}} \tag{1.9}$$

The solution for Equation 1.8 is the diffusion equation for charges diffusion relative to a sphere:

$$n(r,t) = N_0 \frac{exp\left(\frac{r^2}{4.D.t} - \frac{t}{\tau}\right)}{(4.\pi.D.t)^{\frac{K}{2}}} \text{ in } (cm^{-3}) \tag{1.10}$$

Where:

- N_0 is the initial number of electron-hole pairs along the track (cm^{-1}):

$$N_0 = \frac{LET.\rho_{Si}}{E_{pair}} \text{ in } (cm^{-1}) \tag{1.11}$$

  - LET (*cf.* Equation 1.4) is the linear energy transfer of the strike ($MeV.mg^{-1}.cm^2$)).
  - ρ_{Si} is the silicon density(2329 $mg.cm^{-3}$).
  - E_{pair} is the energy to create an electron-hole pair in silicon (3.6 eV).

- r is the distance between the center of the sphere and a point in space (cm).

- τ is the carrier's lifetime (s).

- K=3 in the case of a sphere with radius r(this work), or K=2 in the case of a cylinder with the same radius.

- D is the ambipolar diffusion coefficient ($cm^2.s^{-1}$). It is obtained using the mobility of carriers (μ_n for electrons and μ_p for holes) by the diffusion of carriers thanks to Einstein's relation for diffusion of charged particles.

$$D = 2\frac{D_n D_p}{D_n + D_p} \text{ in } (cm^2.s^{-1}) \tag{1.12}$$

$$D_n = \frac{k.T.\mu_n}{q} \text{ and } D_p = \frac{k.T.\mu_p}{q} \text{ in } (cm^2.s^{-1}) \tag{1.13}$$

  Dn is the diffusion coefficient of electrons and Dp is that of holes. k is Boltzman constant ($1.381 \times 10^{-23} J.K^{-1}$), q is the electron charge ($1.602 \times 10^{-19} C$) and T is the temperature in Kelvin. μ_n is the electrons mobility and μ_p is the holes mobility in $cm^2.V^{-1}.s{-}1$. The mobilities are obtained following Massetti et al work [MSS83]. The method is explained in Appendix A.

So far the diffusion equation was established for a punctual charge diffusing in silicon. The next step is to establish a line from where the charges diffuse.

Following Figure 1.18, Equation 1.10 has to be integrated with respect to L from point A to B. A symbolizes the starting point for the ionization, B is where the particle stops, L is the total length of the line and r is the distance between the line and a point Ω, r varies between A and B. The integral of $n(r,t)$ is:

$$N(l,t) = \int_A^B N_0 \frac{exp\left(\frac{-r(l)^2}{4.D.t} - \frac{t}{\tau}\right)}{(4.\pi.D.t)^{\frac{3}{2}}} dl \ (cm^{-3}) \tag{1.14}$$

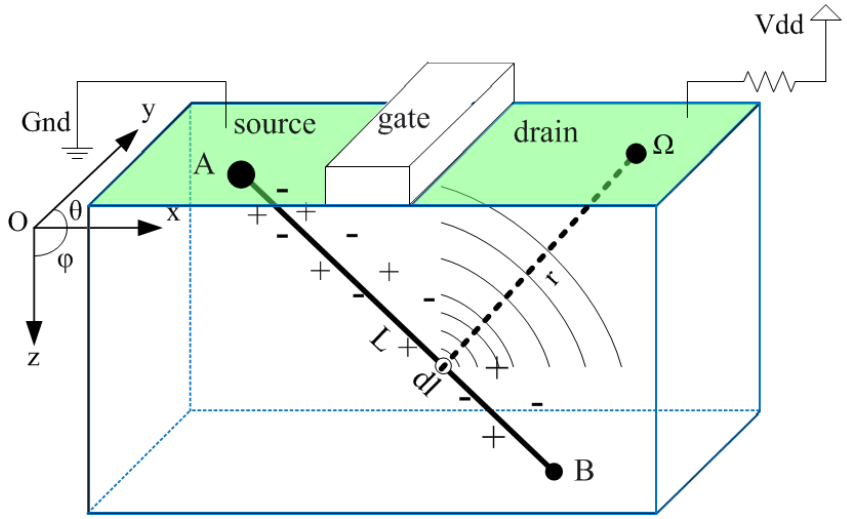


Figure 1.18: Charges diffusing from an ion track to the drain.

The solution to this integral is given in Appendix B.

As stated previously, the LET of a particle is related to the energy of the particle and the length of the trajectory. For simplicity of the model, only straight line trajectories are considered. In order to have a realistic value of LET and L, Ziegler's SRIM program is a good alternative to particle accelerator testing. It provides an estimation of the range of penetration and LET of ions in silicon relative to their initial energy. 86 % of the data from the program is within 10% of accuracy [ZBZ13].

The final step is to determine the total number of charges on the drain at a given moment. The total charge from the ion track collected at the circuit's drain is obtained by integrating the concentration of carriers (N(l,t)) on the drain surface. To obtain the current, N(l,t) must be multiplied by the elementary charge q and by the average collection velocity ν_c via space charge region of the reverse-biased drain.

Thus the current has the following expression:

$$I(t) = \int_{x_{\Omega_0}}^{x_{\Omega_0}+L_{drain}} \int_{y_{\Omega_0}}^{y_{\Omega_0}+W_{drain}} N(l,t) \times q \times \nu_c \; dydx \; (A) \tag{1.15}$$

- $\Omega_0(x_{\Omega_0}; y_{\Omega_0})$ is the initial point of integration with coordinates.
- q $= 1.602 \times 10^{-19} C$
- ν_c is the average collection velocity via space charge region of the reverse-biased drain. It is defined as:

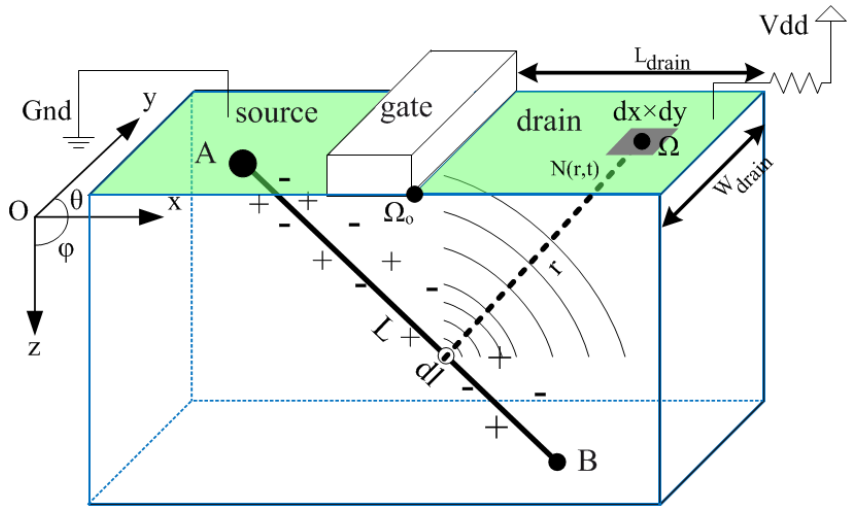


Figure 1.19: Representation of the principle for the calculation of the current based on the number of diffused carriers from an ion track.

$$\nu_c = \mu.E = \mu \frac{V_0}{W_{dep}} \ (cm.s^{-1}) \tag{1.16}$$

Where E is the applied electric field in the depletion region with a width W_{dep} and applied voltage V_0. μ is the mobility of the concerned carriers. In a PMOS transistor the mobility is that of holes μ_p and in a NMOS is that of the electrons μ_n.

$$W_{dep} = \sqrt{\frac{2\varepsilon_{si}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 + V_{drain})} \ (cm) \tag{1.17}$$

V_{drain} is the applied voltage of the drain. The permittivity of silicon is ε_{si} =11.7 ε_0 with $\varepsilon_0 = 8.854 \times 10^{-14} (F.cm^{-1})$.

The built-in junction voltage is expressed as:

$$V_0 = V_T.ln\left(\frac{N_D.N_A}{n_i^2}\right) \ (V) \tag{1.18}$$

The threshold voltage is defined as $V_T = k\frac{T}{q}$ in volts. N_D and N_A are the doping concentration in n-type and p-type silicon in cm^{-3}. n_i in cm^{-3} is the carrier's concentration in intrinsic silicon and is defined as:

$$n_i^2 = B_{si}.T^3 exp\left(\frac{-E_G}{k.T}\right) \tag{1.19}$$

The silicon constant is $B_{si} = 5.4 \times 10^{31}\ K^{-3}.cm^{-6}$. The energy gap is $E_G = 1.12eV$. This time Boltzmann constant is expressed as $k = 8.62 \times 10^{-5} eV.K^{-1}$. Finally T is the temperature in Kelvin.

This model is coded in MATLAB in order to create text files with the information of the current as a function of time for a specific hit. In order to make electrical simulation in CADENCE, the text file of the current is associated with a current source that is connected between the drain and the bulk of a transistor. In this way the electrical simulation can have the geometrical aspects of the ionization strike.

1.4.2 APPLICATION OF THE CHARGE COLLECTION MODEL TO THE CMOS 65NM TECHNOLOGY

In order to put the model in context some examples of situations are going to be presented. For this, the technological parameters were taken from the 65nm CMOS technology kit from ST Microelectronics for the CADENCE simulator. The donors concentration N_D is $10^{20}\ cm^{-3}$ and the acceptors concentration N_A is $6 \times 10^{16}\ cm^{-3}$ for an NMOS transistor. The electron mobility μ_n is 278 $cm^2.V^{-1}.s{-}1$ and the hole mobility is μ_p is 126.8 $cm^2.V^{-1}.s{-}1$. The temperature was chosen as 300 K and the carriers lifetime is set to 1 μs. The LET is considered constant along the track and is set to 0.677 $MeV.mg^{-1}.cm^2$ and the trace length L is 18.95 μm. In order to validate this model, it will be compared to the one in the work of Autran et al. [AUM+10]. This last one is used as reference. The model of current from Equation 1.7 [MCP+05] is also presented and is used as the estimation model. Three impacts were simulated for the situation illustrated in Figure 1.20, each impact has an ionization track of length L. The first one is a vertical trajectory, the second has an inclination of 45◦ relative to the vertical and the third has the initial point at a depth of 1μm and inclinations of 45◦ relative to the vertical and the x axes.

In Figure 1.21 the model presented in the works of Autran et al. [AUM+10] and this work are coherent. The estimated current reaches the maximum thanks to the Imax and Tmax criterion. The trajectory 2) injects more current than the other two in the drain because the whole track is closer to the drain. As the whole track goes far from the drain, the collected current decreases. So an ionization track has to be in a certain range of the drain to cause a voltage spike. This means that a threshold distance exist for the creation of SETs depending on the LET of the particle strike.

With Figure 1.22, is possible to see how the concentration of charges changes with the geometry of the strike. For the impact 1 the diffusion is perfectly circular, but for the second the form is a little stretched to the right. For the impact 3, the

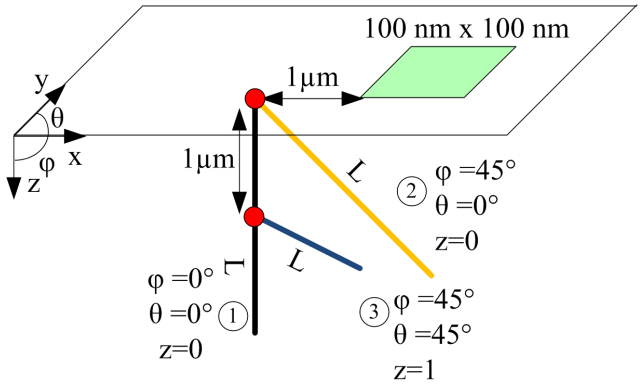


Figure 1.20: Ionization situation for three strikes. 1) Vertical trajectory, 2) Trajectory with inclination of 45◦ relative to the z axis, 3) Trajectory beginning a depth of 1μm with inclinations of 45◦ relative to the z axis and the x axis.

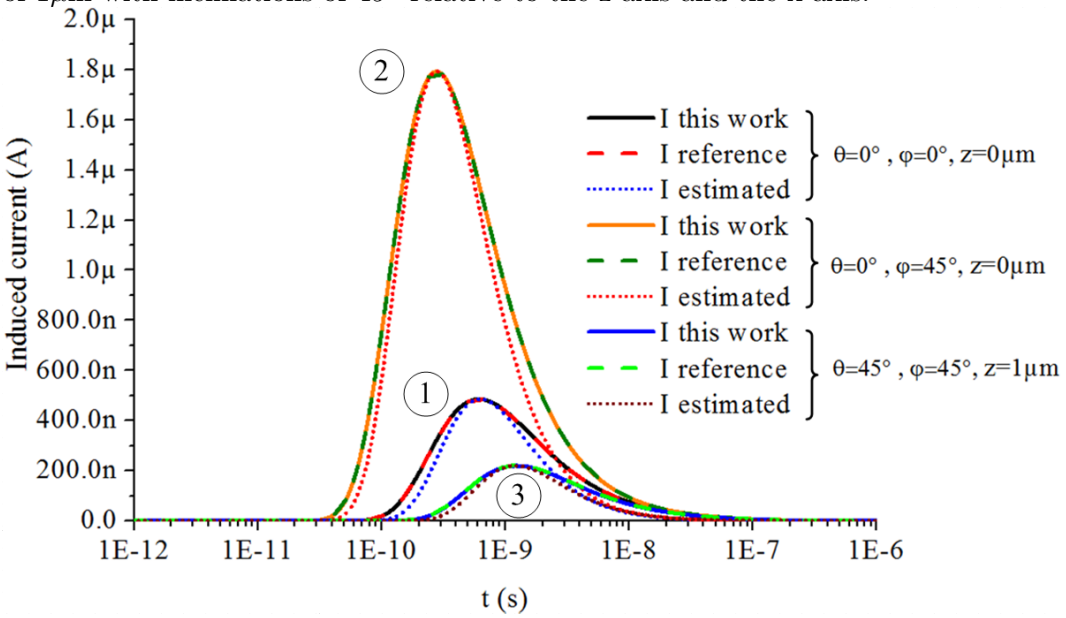


Figure 1.21: Currents from the three ionization situations, from this work, the reference model [AUM+10] and the estimated model [MCP+05].

45◦ deviation can be seen. For this last impact, the carriers take more time to reach the surface because of the depth. That is why for the initial time there is no diffusion form on the surface. The peak of collected current is different for each impact case, thus the concentration of charges at the peak time is different being the highest for the impact 2. The evolution of the charges concentration supports the idea of this threshold of distance between an ion track and the drain. To go further with the idea of the threshold distance, this implies that there is a threshold area. This threshold

area delimits the surface where a drain is sensitive to ionization. This sensitive area is also known as the cross section.

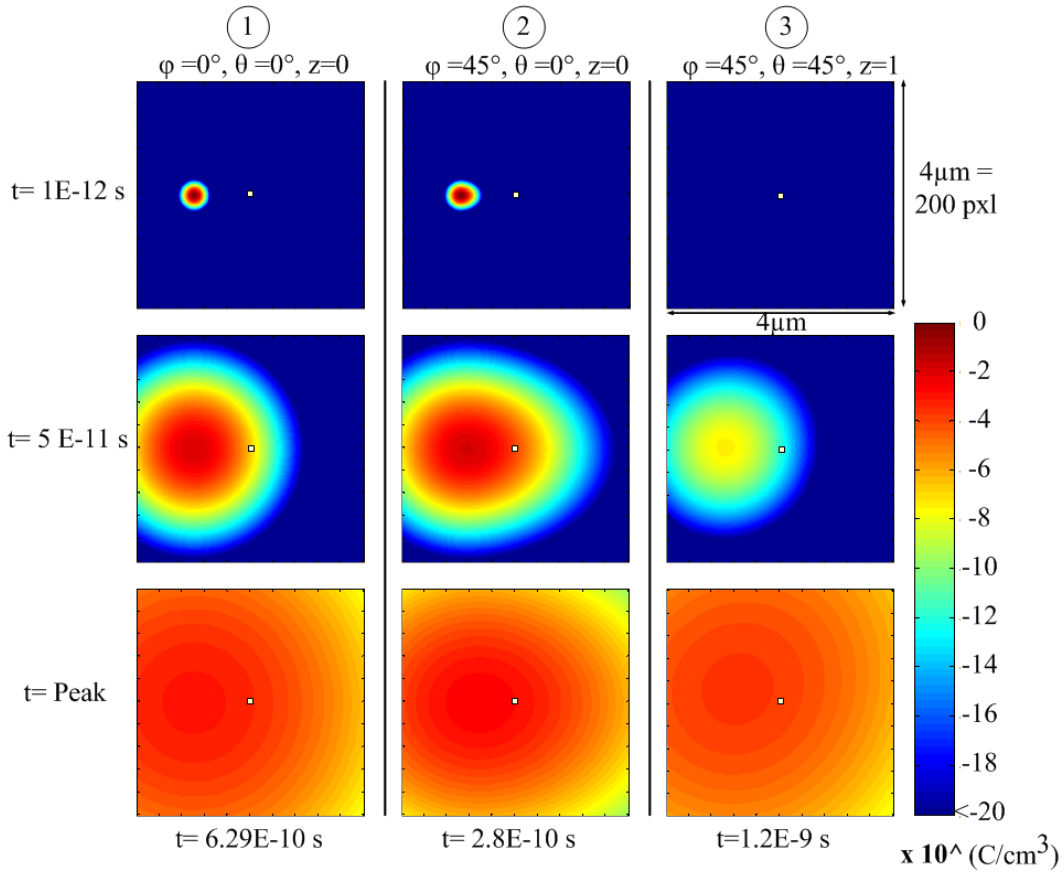


Figure 1.22: Diffusion of charges for the three scenarios of Figure 1.20 seen for a surface of 4 μm x 4 μm. The white square is the drain surface (0.1 μm x 0.1 μm) that collects current.

1.4.3 Cross section definition

The soft error cross section $\sigma_{soft-error}$ is a measure of probability that a collision process will result in a soft error. Along with the soft error rate, the soft error cross section is the most important parameter for circuit reliability and is used to calculate the soft error rate. It is expressed by the effective area in cm^2 of a target for the incident particle. In other words, the cross section is the effective area where an impact (of enough energy) can cause a soft error. It is common to evaluate the cross section as a function of the linear energy transfer (LET). Experimental results of soft error cross section are usually fitted with the Weibull cumulative distribution. The typical curve of cross section relative to the LET has the shape as shown in Figure 1.23.

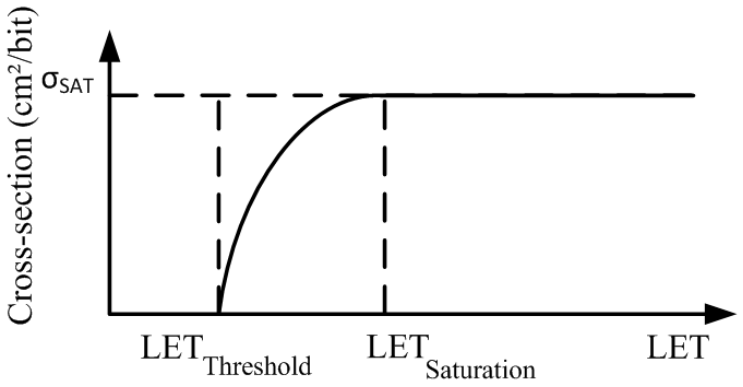


Figure 1.23: SEU cross section typical curve.

This shape shows three important parameters: the LET threshold and saturation and the cross section saturation σ_{SAT}. The first indicates the LET from which an SEU takes place. The second is the LET from which the saturation of the cross section takes place. The last one, σ_{SAT} indicates the upper limit of cross section area.

The cross section is measured using a beam of particles produced in an accelerator. The beam is moved in order to have a surface sweeping and detect when and where an SET takes place. In a more theoretical approach some TCAD simulation tools, such as Cogenda, Sentaurus from Synopsys or TFIT from Iroctech give results based on Monte-Carlo simulations [UGR+10].

As an indicator of the cross section of a drain, it is possible to use a simplification. Let us consider a vertical impact, like case 1 in Figure 1.22. The SET takes place if the charge brought to the drain is more important than the critical charge. The critical charge is the minimum charge required to change the logic state at the drain of a transistor. Hits at different distances from the drain induce different

amounts of charge, thus some will induce SET and other do not (cf. Figure 1.24 a)). If the distance between the impact and the drain is the maximum distance that an impact of such LET induces an SET (cf. Figure 1.24 c)), then is possible to establish an area, surrounding the drain area like in Figure 1.24 b). This area determines the surface in which if an impact occurs is possible to have en SET on the drain. Then is possible to calculate the estimated cross section surface of the drain using Equation 1.20. This simplification can be discretized and applicable to the model presented in Section 1.3.

$$S = W \times Ld + 2(W \times L_{LET-Sat}) + 2(L_{LET-Sat} \times Ld) + \pi \times L^2_{LET-Sat} \ (cm^2) \quad (1.20)$$

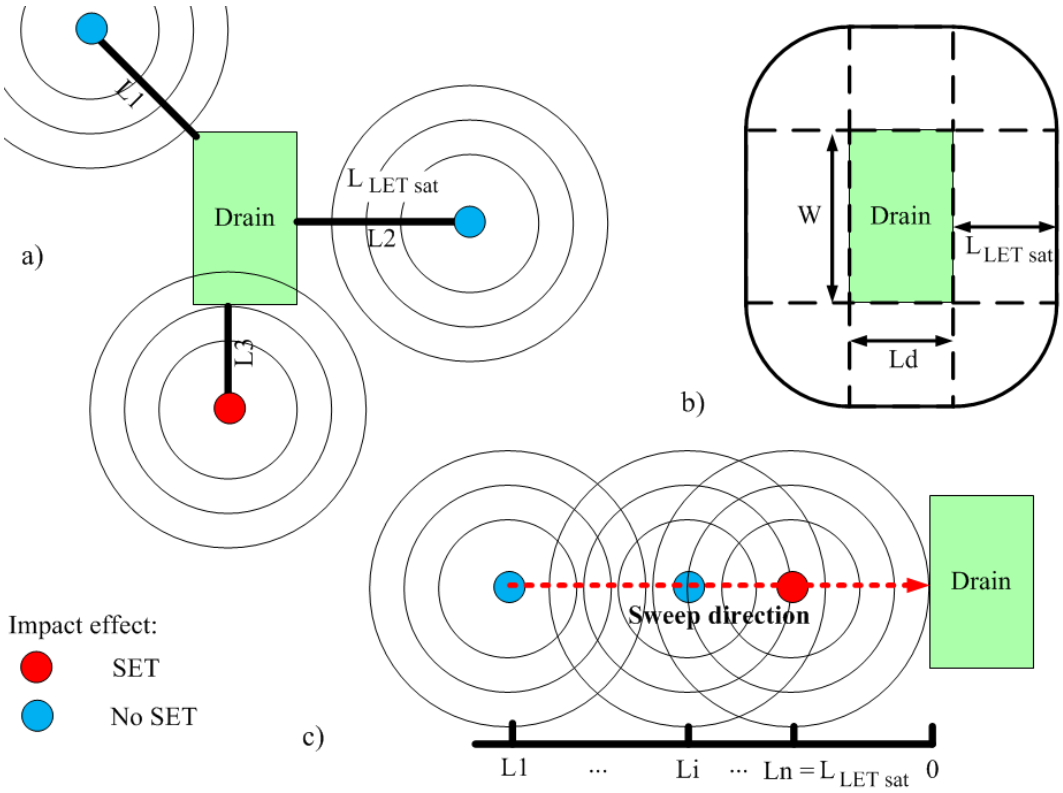


Figure 1.24: a) First approach to determine the cross section area for a drain, using several impact simulations. b) Simplified shape of the cross section given the technological parameters of the drain W and Ld c) Unidirectional sweep to determine the $L_{LET-sat}$ distance.

1.4.4 THE CROSS SECTION SATURATION

The saturation of the cross section indicates that the circuit has a limited sensitive area regardless the values of LET above a certain limit. To understand the causes for the cross section saturation, it is pertinent to look at the atomic level. In nuclear physics, the cross section is a measure of the probability that an encounter between particles will result in the occurrence of a particular atomic or nuclear reaction. It is also called collision cross section. Statistically, the centers of the atoms in a thin foil can be considered as points evenly distributed over a plane. The center of an atomic projectile striking this plane has geometrically a definite probability of passing within a certain distance r of one of these points. In fact, if there are n atomic centers in an area A of the plane, this probability is $(n\pi r^2)/A$, which is simply the ratio of the aggregate area of circles of radius r drawn around the points to the whole area. So there is a finite area of interaction.

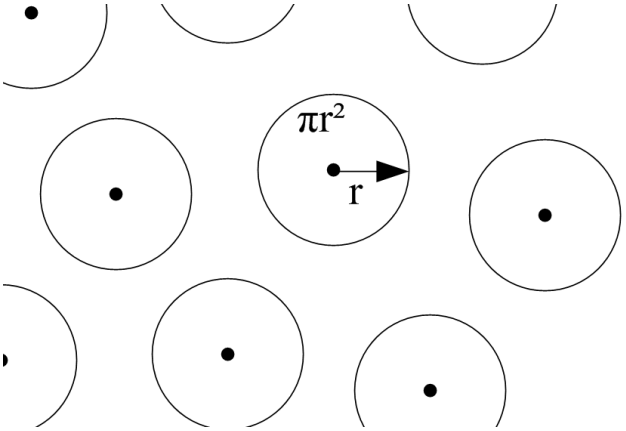


Figure 1.25: Discs of interaction.

For now the concept of a finite interaction surface has been explained, but this work deals with ion interaction with transistors. Thus the concept of cross section has to be taken to the transistor level. Since a soft error caused by an ionizing particle is a phenomenon that takes place in a volume, it is important to look at other parameters such as the LET of the secondary particles, and the carrier's lifetime to understand the cross section saturation at this level.

It was already explained that when a neutron collides with a silicon nucleus and breaks it expelling different kinds of ionized particles, those particles travel though the silicon lattice, creating electron-hole pairs, for a distance before they are stopped or passed through the material (*cf.* Figure 1.26). Since carriers have a finite lifetime, some of the electrons will not be able to diffuse to the drain. Recombinations take place between the ion track and the drain. Thus if the distance is too large a lot

more recombinations take place and then less current will arrive at the drain to be able to create en SET. It is important to note that along the ionization track there are a limited number of electron-hole pairs that can be created. Hence, if the incident particle energy is increased above a certain limit, there will not be more electron-hole pairs that can be created. Carrier's lifetime and the limit of electron hole pairs contribute to the saturation of the soft error cross section.

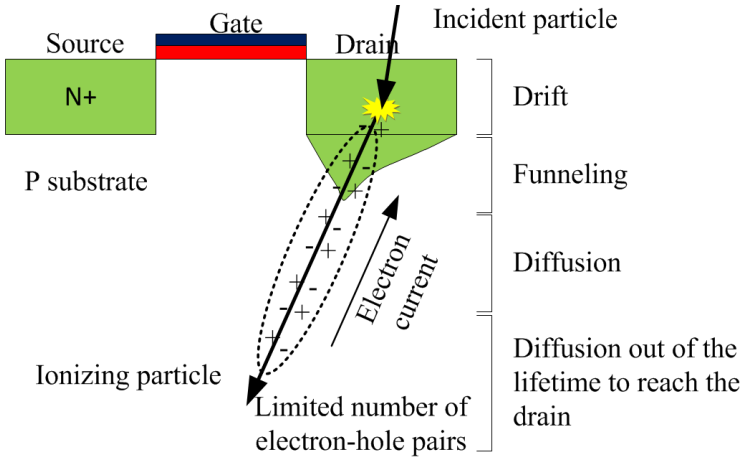


Figure 1.26: Ionization by a particle strike on an NMOS transistor.

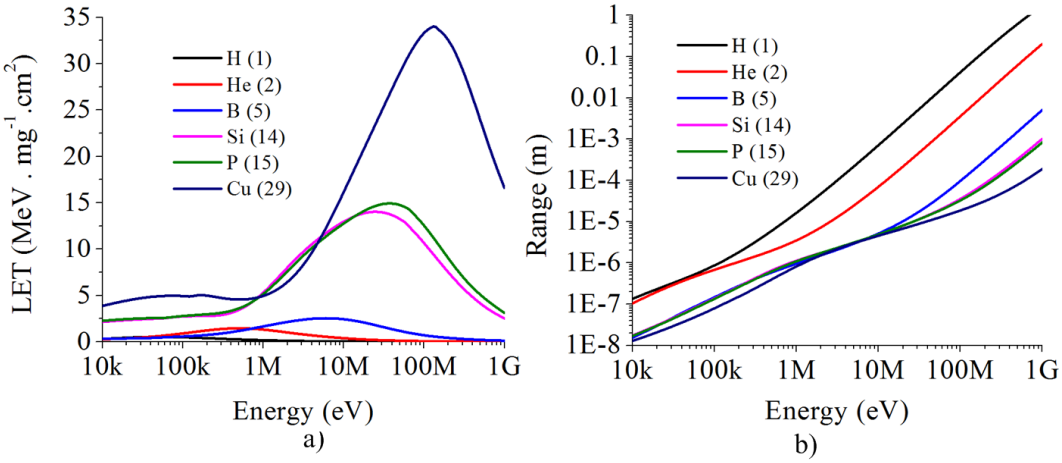


Figure 1.27: a) LET relative to the incident energy of the ions, b) Range of the particle in a block of Silicon relative to the incident energy. Data were obtained using SRIM [ZBZ13].

A final comment refers to the amount of charge created by ionization. LET

units can be converted to $fC/\mu m$, which represent a charge deposited by length. Intuitively the more an incident particle has energy the more electron-hole pairs will be created (more deposited charge) and the longer the ionization track is. But in Figure 1.27 it is pointed out that the LET of a particle depends not only on its incident energy but also on its nature. Figure 1.27 a) shows that the higher the atomic number the higher the LET. Figure 1.27 b) shows that the lower the atomic number the higher the range. Indeed a larger ion like Copper (1.28 c)) may collide with more atoms in matter creating more recoils than a small one like Hydrogen or Helium (Figure 1.28 a) and b)). The small one will reach a longer distance in the material than the bigger one for the same incident energy. In fact since Cu can interact more with silicon, it can deposit more charge than H in a shorter distance. But the fact that the small one reaches a longer distance does not mean that it can create more parasitic current, because even if more electron-hole pairs are created with the distance, electrons and holes may recombine and less current will be induced. The cross section may vary with the type of incoming particle, but the saturation effect will prevail. Either the range is important but the ionization not important or the range is small and the ionization is important.

1.5 Conclusions

This chapter showed the importance of the high energy neutrons in the soft error phenomenon; they are considered as the main source of soft errors. Those soft errors are caused by the ionization current created in the bulk of the CMOS transistors. When an ionized particle hits, the charges diffuse to the drain creating the parasitic current between the bulk and the drain. This current can be electrically simulated introducing a current source between the drain and the bulk of a transistor. This model is coded in MATLAB in order to create text files with the information of the current as a function of time for a specific hit. In order to make electrical simulation in CADENCE. In this way the electrical simulation can have the geometrical aspects of the ionization strike. The current source introduces the values of current relative to time given by the charge collection model. This fault injection methodology of simulation will be used subsequently. The model explained in this chapter uses geometrical parameters to give a more realistic behavior of the current. The realistic values of LET can be obtained thanks to SRIM simulation. This model was compared with state of the art models and is in accordance with them. This model will be useful in the electric simulation methodology for subsequent circuit reliability analysis. Finally, the discussion on the soft error cross section for a drain showed that there is a limit for this sensitive area. And thanks to the simplification for determining the cross section, an approximation of this sensitive surface can be found with the MATLAB model explained in this chapter. In a preliminary analysis,

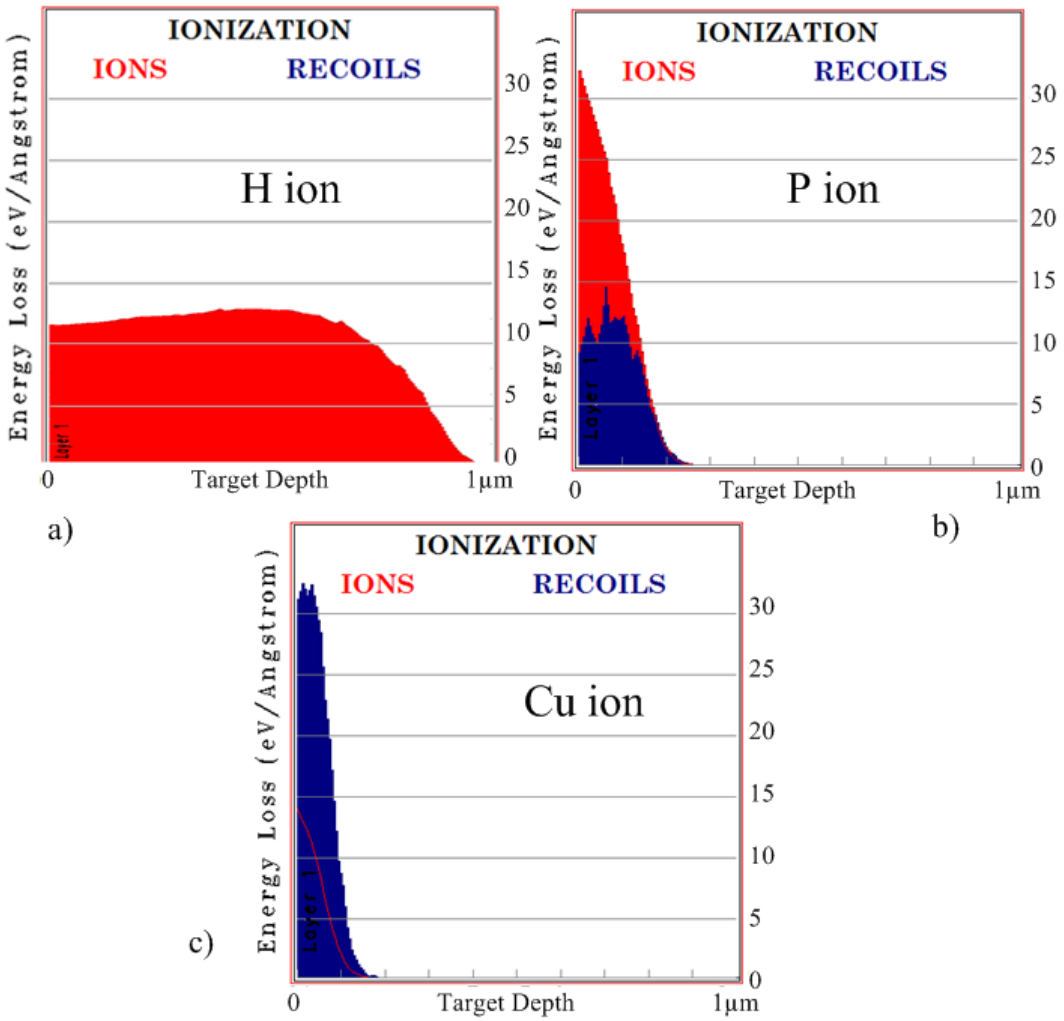


Figure 1.28: Comparison of the ionization expressed in energy loss per Angstrom for an incident energy of 100 keV for different ions. a) Hydrogen, b) Phosphorous, c) Copper. Data were obtained using SRIM [ZBZ13].

this avoids the cost of heavy ion testing. Having realistic parameters in the model, and an approximation of the cross section are keys aspects that are useful in the study of vulnerability for a system in need of a hardening technique.

Chapter 2

Study of a radiation impact on a SAR ADC

In the previous chapter, the effects of radiation on integrated circuits were exposed. It was previously mentioned that CMOS technologies are becoming more sensitive to single event effects, especially 65nm and subsequent technologies. In this chapter, in order to comprehend the effects of SETs on a complex system a vulnerability study will be done. The first step in the study will be to select an appropriate system, for this work a SAR analog-to-digital converter (ADC) will be chosen. This type of circuit mixes analog, synchronous and asynchronous circuits in one system. The next step, will be to select a potentially critical part of this system. Then the fault injection methodology, described in Chapter 1, will be implemented into the CADENCE simulator to make the analysis of the behavior of the system facing SETs. The analysis will show the sensitivity to SETs on three aspects of the critical circuit. The first will be the analysis of the critical charge of the critical circuit. The second will be the influence of the position of the particle hit taken into account the geometric aspects of the layout of the circuit. Finally, the temporal sensitivity of the circuit and the SAR reaction to the errors that took place on that critical part will be analyzed.

2.1 Case study: Combinatorial function within an 8 bit SAR ADC

The effects of radiation on a transistor scale were exposed previously, and it would be interesting to see what happens on a system scale. This information can be useful to determine a hardening strategy. To begin the study a system has to be chosen. Analog to digital converters seem very interesting systems and SAR ADC in particular. A SAR ADC will be explained and then the vulnerability will be exposed.

2.1.1 Motivations for the case study of a SAR ADC

Keeping in mind the diversity of electronic circuits (*i.e.* analog, digital, synchronous, asynchronous, combinatorial), a circuit application combining all these aspects is preferred because of the diversity of outcomes. This diversity can be found in the analog-to-digital converters. Another aspect to take into account is that the circuit has to be conceived for low power applications, since it is one of the most challenging aspects in the electronic industry. An interesting comparison was made for the general tendencies for different types of ADC in Bernal's thesis [Ber06]. In order to pick an ADC a small description of each ADC will be now presented and then will be presented a qualitative comparison.

The Flash ADC has the fastest conversion time, and the digital code can be obtained after one single clock cycle. The flash conversion used 2^N- 1 comparators in parallel to compare the input signal level with all the 2^N- 1 quantization levels. The price to pay for such a rapid response is a rather complex circuit.

In order to diminish the complexity of a Flash ADC, the number of comparators can be reduced and the conversion can be done in two steps. That is the idea of the Multi-Flash architecture. The first one does the conversion for the MSB, then the digital result is converted to an analog signal. This analog signal will be subtracted from the input signal. The resultant analog signal is sent to a second Flash converter.

The Pipeline converter is another type of multiple Flash stages converter. The architecture of this ADC is divided in several small Flash stages (of 1 to 3 bits). Every stage has its own sample and hold circuit to sample the residue signal from the previous stage. This feature allows each stage to sample a new signal once the residue is already sample by the next stage. The sample speed of the converter is independent of the number of stages. The latency between the moment a signal enters the ADC and the whole code is obtained is proportional to the number of stages.

The SAR ADC uses a DAC to generate a signal that approximates the input analog signal. The DAC is driven by a logic that implements a successive approximation algorithm. The main advantage of this architecture is that only requires one comparator and one DAC, unlike the previous exposed ADCs. This makes the architecture very simple. The main drawback of this type of ADC is that needs the same amounts of clock cycles as bits of its digital code. This ADC is precise but slow.

A Cyclic ADC is a Pipeline ADC with only one conversion stage with a feedback on itself. The latency between the input and the output is the same as the Pipeline ADC , but the sample speed is divided by the number of cycles to digitize

a sample. Its simple architecture consumes less power than the Pipeline one.

The principle of the Sigma-Delta ADC is to oversample the desired signal by a large factor and filter the signal band. It uses a Sigma-Delta modulator to sample the residue error between the input signal and the estimated value of the input signal. Then, the modulator is followed by a Flash ADC that gives a quantization with one or more bits per clock cycle. Thanks to the oversampling the quantization and noise errors are diminished but the conversion time is the most significant above the other architectures explained before.

Table 2.1 summarizes the characteristics of the ADC and shows a qualitative comparison of the different ADC architectures. The SAR and the cyclic architectures have interesting agreements between the power consumption, precision and latency. The disadvantage is the speed they can reach.

Type of ADC	Flash	Multi-Flash	Pipeline	SAR	Cyclic	Sigma-Delta
Speed	$+++$	$++$	$+$	$--$	$--$	$---$
Power consumption	$---$	$--$	$-$	$++$	$++$	$+$
Precision	$---$	$--$	$+$	$++$	$++$	$+++$
Latency	$+++$	$++$	$+$	$+$	$+$	$--$

Table 2.1: Qualitative evaluation of different ADC architectures [Ber06].

An interesting SAR ADC is the one from Harpe et al. work [HZB+11], because the power consumption of the SAR architecture is reduced using asynchronous logic and a stand-by mode. For those reasons the selected system to be studied is the 26 μW 8 bit 10 MS/s asynchronous SAR ADC [HZB+11]. The circuit was originally designed for 90 nm CMOS technology. Based on Harpe's et al. paper the circuit was scaled using CADENCE with the 65 nm CMOS technology kit.

In order to verify the performance of the 65 nm technology version relative to the 90 nm one, the Differential Nonlinearity (DNL) and the Integral Nonlinearity (INL) were calculated. The DNL and the INL quantify the precision of an ADC. They are indicators of the deviation between an ideal ADC transfer function and the actual transfer function. Figure 2.1 shows an ideal and a real transfer function for a 3 bit ADC. Vtr indicates the voltage at which a transition takes place and V_{LSB} is the quantification voltage for an LSB.

The DNL quantifies the deviation of the step width. A DNL error of less than or equal to 1 LSB guarantees a monotonic transfer function with no missing codes. The DNL is defined as follows:

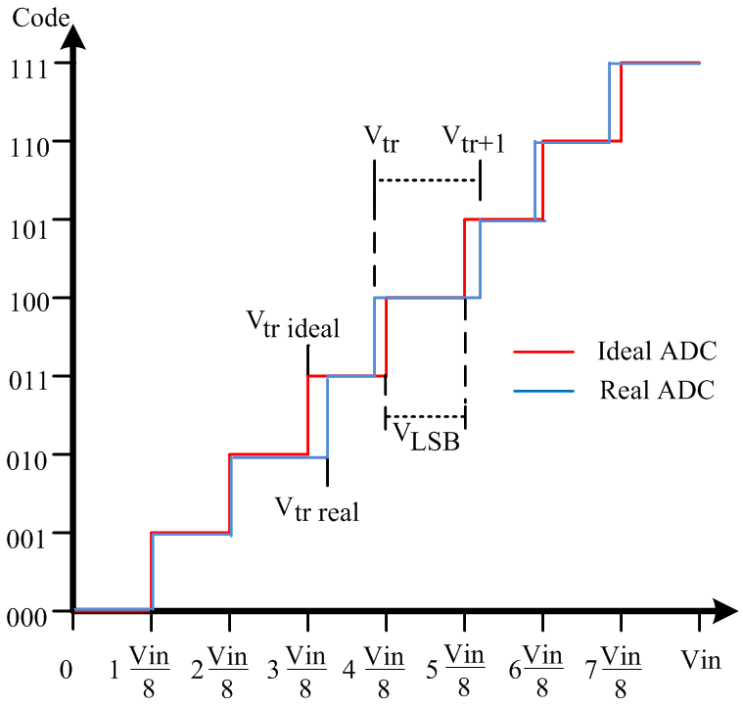


Figure 2.1: Ideal and real transfer function for a 3 bit ADC.

$$DNL = \frac{V_{tr+1} - V_{tr}}{V_{LSB}} - 1 \text{ (LSB)} \tag{2.1}$$

The INL quantifies the deviation of the transition between the real and the ideal transfer function. An INL error of less than or equal to 1 LSB guarantees a low offset between the real and the ideal ADC transfer function. The INL is defined as follows:

$$INL = \frac{V_{tr\ real} - V_{tr\ ideal}}{V_{LSB}} \text{ (LSB)} \tag{2.2}$$

Figures 2.2 and 2.3, show the DNL and the INL for both versions of the same ADC [HZB+11]. In both cases the values are under an LSB and under the range of the reference values. The DNL and INL for the 90 nm version come from Harpe et al [HZB+11]. work. On the other hand the values for 65 nm version were determined by CADENCE simulation. Those values of DNL and INL ensure that the 65 nm version is functional and realistic.

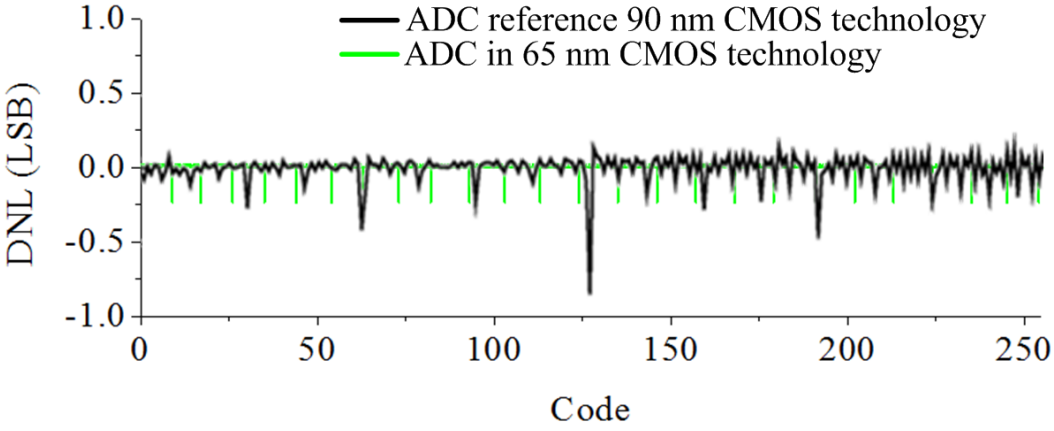


Figure 2.2: DNL for the reference ADC [HZB+11] and the 65 nm version.

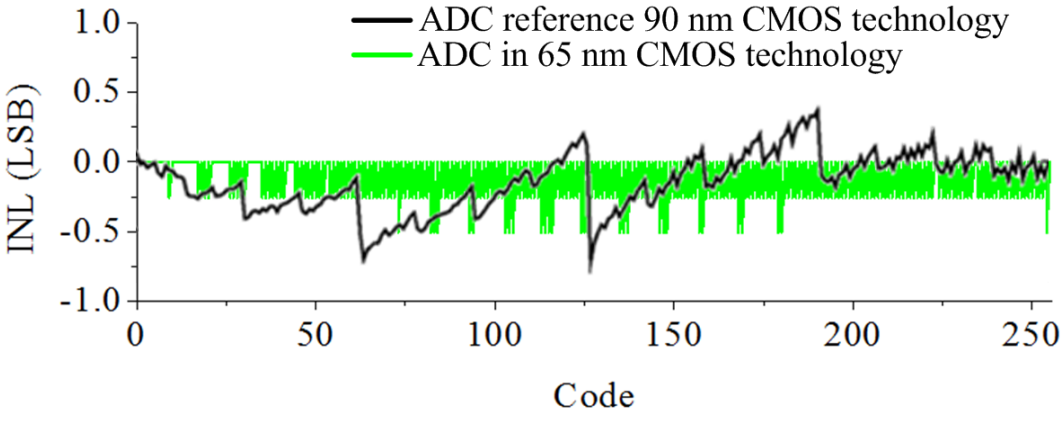


Figure 2.3: INL for the reference ADC [HZB+11] and the 65 nm version.

2.1.2 Operation of the SAR ADC

The SAR ADC uses the binary search algorithm to convert the analog input into an 8-bit code. Figure 2.4 illustrates how the algorithm works. The ADC compares the input voltage (Vin) to the reference voltage which is the power source voltage (Vdd). Thanks to a switched capacitor network composed of weighted capacitances (proportional to powers of 2), the input voltage is compared to fractions of Vdd (V_{Ci}) in eight iterations. At the beginning of the algorithm Vin is compared to V_{C0} with a value of Vdd/2. If Vin is bigger than Vdd/2 the initial MSB bit is set to 1, if it is smaller (this example) the bit is set to 0. The next iterations follow this logic:

$$\begin{cases} V_{Ci+1} = V_{Ci} - \frac{Vdd}{2^{i+1}}, & \text{if previous bit SET to 0} \\ V_{Ci+1} = V_{Ci} + \frac{Vdd}{2^{i+1}}, & \text{if previous bit SET to 1} \end{cases} \tag{2.3}$$

So for the next iteration $V_{C1} = V_{C0} - Vdd/4$. Vin voltage is now compared to 1/4 Vdd. In this case, Vdd is higher then the bit is set to 1 and $V_{C2} = V_{C1} + Vdd/8$. The algorithm goes on until it reaches the eighth iteration. This algorithm has a precision of 1 LSB, that is $Vdd/2^8$ V.

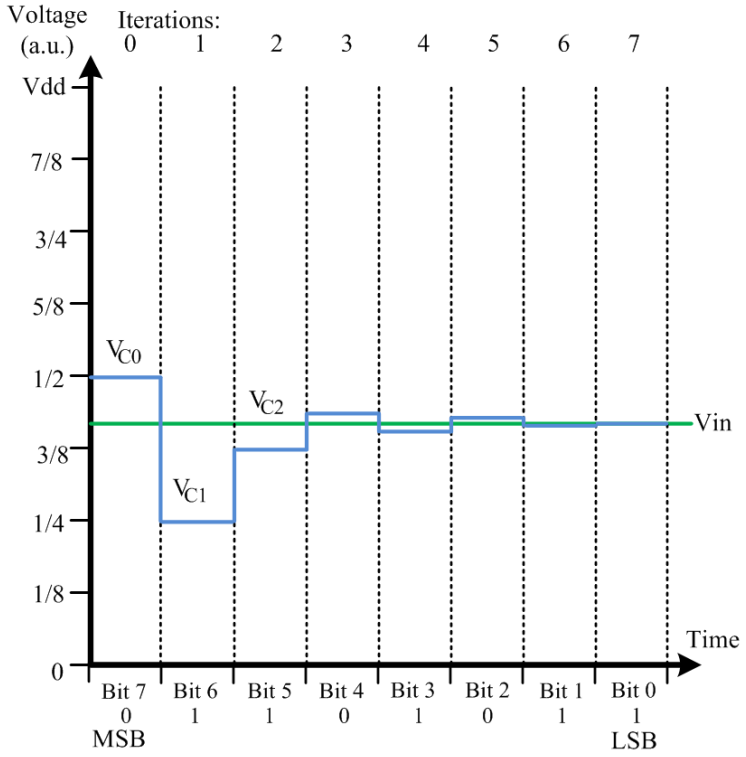


Figure 2.4: Example of the algorithm for 8 bits.

This 8-bit ADC has four main parts [HZB+11] as illustrated in Figure 2.5: The sample and hold capacitor network (SHCN), the comparator, the asynchronous logic and the standby control. The first part implements the sampling, the feedback digital-to-analog converter (DAC) and the summation node. It adds the input voltage with the voltage obtained from the DAC. This is implemented with two charge-redistribution capacitor network with weighted capacitances and an input switch.

The second part makes a clock triggered comparison of the result of the summation and decides which of the differential inputs is the greatest. The result of the comparison is given by *Comp out* and the indication that the comparison is ready is given by *Comp Rdy*. The comparator is sequenced by the *Internal CLK* signal generated by the asynchronous logic.

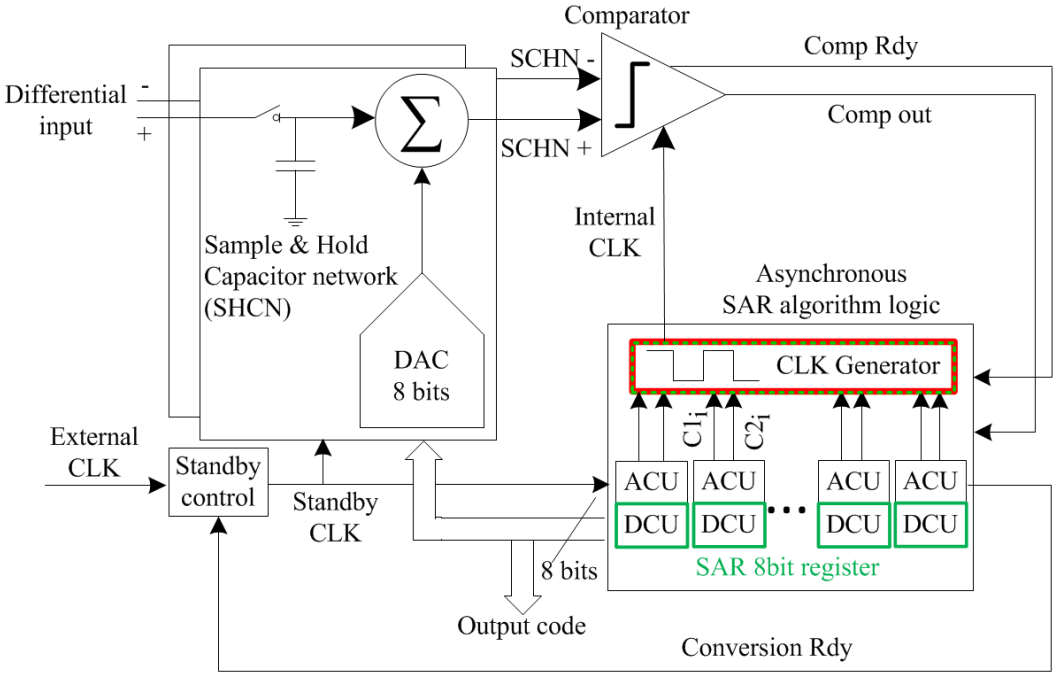


Figure 2.5: Asynchronous SAR ADC Architechture [HZB+11].

The third part, the asynchronous logic, implements the successive approximation algorithm. This 8-bit binary-search algorithm is performed thanks to the feedback loop to the SHCN part, with the information given by the comparator, to obtain the digital output code. The asynchronous logic is implemented by eight pairs of unit blocks. One block is the Algorithm Control Unit (ACU) that is responsible

for the progress of the SAR algorithm. The other block is the DAC Control Unit (DCU) that stores one bit of the code in one bit cycle. This stored bit comes from the comparator result. Both ACU and DCU implement state machines. The eight DAC control units form the SAR register. Each ACU communicates with its pair DCU with two signals $C1_i$ and $C2_i$. These signals control the combinatorial function (CLK Generator) that generates Internal CLK. When the conversion is completed the asynchronous logic sets the conversion ready signal (*Conversion Rdy*) to "1".

The last part is the standby control. This part synchronizes the ADC to an *External CLK* signal as depicted in Figure 2.6. This signal is responsible of the beginning and the end of the conversion cycle. When *External CLK* becomes "1" , *Standby CLk* becomes also "1" and then the conversion begins with the activation of the *Internal CLk* while *Standby CLk* is "1". The standby control also takes into account the completion of the algorithm and disables the *Standby CLk* signal. By turning off the *Standby CLk* when the conversion is finished (*Conversion Rdy* = "1"), regardless of the external clock frequency, the standby control maximizes the standby time and reduces the leakage current. The effect of this mechanism is the reduction of the power consumption for low operation frequencies.

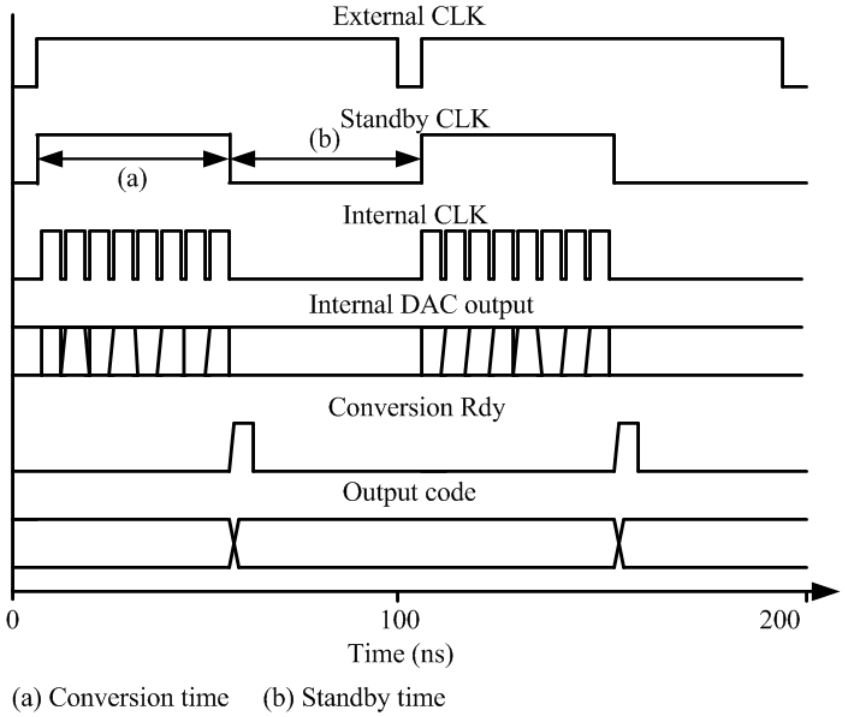


Figure 2.6: Simplified timing diagram of the asynchronous logic [HZB+11].

2.1.3 Choosing a circuit for analysis

2.1.3.1 Relations between blocks and error propagation

The ADC has different types of circuits and it would be complicated to analyze the whole ADC at the same time. Furthermore the objective is to analyze a function of the ADC that can potentially affect the ADC conversion by introducing an SEU in the SAR register. Figure 2.7 shows the possible error propagation paths between blocks.

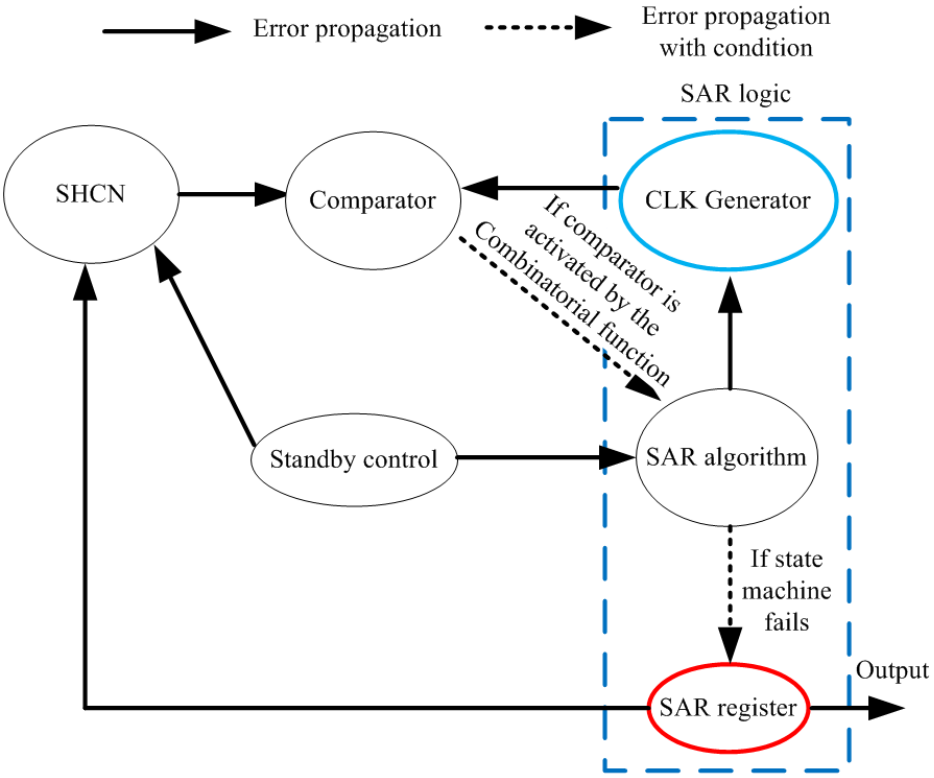


Figure 2.7: Paths for error propagation between blocks in the SAR ADC.

The Standby control block is essentially a toggle flipflop with combinatorial logic. A radiation affecting the Standby control can cause undesired transitions of the *Standby CLK* can reset the conversion before the end. This causes direct problems at the output of the system because the initial differential voltage changes and a wrong binary code is obtained at the end. This is a potentially sensitive part. So this block can affect directly the SHCN and the SAR algorithms blocks.

The SHCN is essentially made of metal-plate capacitors. To our knowledge ionizing radiation does not have an impact on this type of capacitors. In addition, the switch could be considered as critical, but it represents only 0.7 % of the total SHCN surface and the probability to be hit by radiation is smaller in comparison to other more complex circuits in the ADC. The DAC is implemented by the action of inverters that serve as switches in the charge-redistribution capacitor network. Those inverters are driven by the SAR logic and are also quite small.

Supposing an error occurs in the SHCN, the only way an error can propagate to the SAR register is if the comparator and the SAR logic is active. So the influence of the SHCN is restrained. For an error from the SHCN to propagate, *Internal CLK* must be "1" so the comparator can act and activate the *Comp Rdy* signal so that the SAR logic will be disturbed. But the comparator's activation depends on the CLK generator function that generates *Internal CLK*.

In the case of the comparator, if its output signals *Comp Rdy* and *Comp out* have glitches, they can affect the SAR logic by affecting the state machines. The comparator is the link between the analog and the digital part of the circuit. Its output is digital and the output is valid only when it is activated by *Internal CLK*. It is also a potential critical circuit but its errors can be logically masked by the logic from the SAR algorithm blocks that drive the combinatorial function that then drives *Internal CLK*.

The Combinatorial function that generates *Internal CLK*, is the feedback link between the SAR algorithm and the comparison process. Thus an error in this block can cause a bad comparison, or turn the comparator off. This can cause subsequently errors in the logic of the algorithm.

The SAR algorithm block (made by the ACUs) manage the signals state to ensure the process of conversion with the state machines. It is the last block before the register. It is essentially made by flip flops including logic. An error in this part can cause a change of state in the register and affect the SCHN capacitor network subsequently.

Finally the SAR register block (made by the DCUs) is always sensitive to radiation because a direct impact can change the logic state through out the whole conversion cycle an change the value of a bit. An error at this register changes the output but also the error can cause bad charge-redistribution in the SCHN.

As a summary, three blocks seem to be the most relevant: The Stanby control, the SAR algorithm with the ACUs array, and the Combinatorial function. The first two are made of flip flops and the last one completely made of combinatorial circuits.

Soft errors in flip flops and memories have been traditionally a more wide subject of study than soft errors in combinatorial circuits. Soft errors in memorization circuits have been a greater concern because they have a largest number and density of bits susceptible to particle strikes. In recent years, the International Technology Roadmap for Semiconductors (ITRS) stated that, below 65nm CMOS Technology, soft errors impact field-level product reliability, not only for embedded memories, but for logic and latches as well [ITR11]. For this reason and the influence of the Combinatorial function on the circuit , this function is chosen to be analyzed.

2.1.3.2 THE CRITICAL FUNCTION

The asynchronous logic is the core of the circuit and it is the most important part of the system. The *Internal CLK* signal, being the internal sequencer, links the SAR algorithm with the analog part of the circuit. This signal is critical because it can trigger a comparison when it is not requested and thus this can induce errors in the output code. Those errors have different weights, if the error occurs for the most significant bits (MSB) then the value will have a large error, but if the less significant bits (LSB) are affected the error will be small. The study is centered on the CLK generator.

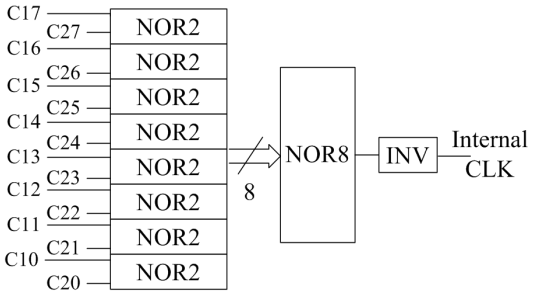


Figure 2.8: CLK generator function for *Internal CLK* generation scheme.

The combinatorial sequencer function scheme is shown on Figure 2.8. This function is composed of eight two-input nor gates (NOR2), one eight-input nor gate (NOR8), and an inverter. The combinatorial logic function associated with this architecture is:

$$InternalCLK = \sum_{i=0}^{7} \overline{C1_i} \cdot \overline{C2_i} \tag{2.4}$$

This critical function controls the comparator and it is crucial to activate the comparator at the right time to obtain a correct bit code. Otherwise the comparator will be activated at en undesired time and compared two non stable signals. The

function has to reach a high state of the *Internal CLK* when $C1_iC2_i$ ="00", according to the state machines. This state generates an output of "1" and activates the comparator. The state "00" means that the result of the comparison is needed to make a decision on the bit in the digital code. This state is generated eight times, once per bit cycle.

The critical function being set, the efforts are going to be concentrated to understand how ionizing radiation can affect this function and how an error occurring in it affects the output of the ADC.

2.2 ELECTRICAL SENSITIVITY

The critical charge study focuses on understanding the electrical sensitivity of a combinatorial gate. The aim of this study is to show the behavior of an SET current injected in a node of the gate. This will give a full understanding of how a soft error is created at the output of a gate. The electrical sensitivity of a given node in the circuit can be expressed in terms of critical charge (CC). The CC is the minimum charge required to change the logic state. This study is done by CADENCE simulations with ST 65nm CMOS technology using the model explained in Chapter1 Section 1.3. Current sources were connected between the drain of the transistors and the bulk as depicted in Figure 1.14.

The CC will be determined for the three components of the combinatorial function (Figure 2.8), the inverter, the NOR2 and the NOR8. This CC will be estimated when a state change occurs on the *Internal CLK* signal. Since the CLK generator function has several stages of functions, an SET occurring on the NOR2 might be electrically masked while traveling through the whole structure. To ensure that an SET arrives to the comparator of the ADC the logic change caused by an SET has to be detected on *Internal CLK*.

2.2.1 CRITICAL CHARGE OF THE INVERTER

In order to understand the behavior of the critical charge in circuits a simple inverter is analyzed in the first place. The study begins with an inverter with same size transistors with a variation of a capacitor load. Then the influence of the size of the transistors with a fixed load will be analyzed. Finally the influence of the type of transistor (SVT ,HVT, LVT) will be investigated.

Figure 2.9 shows the test bench used for the study and the evolution of the critical charge relative to the capacitance. In the test bench scheme the source I_{SET} Up simulates an ionization impact on the PMOS transistor that generates a transition from "0" to "1". I_{SET} Down simulates the impact on the NMOS and a transition

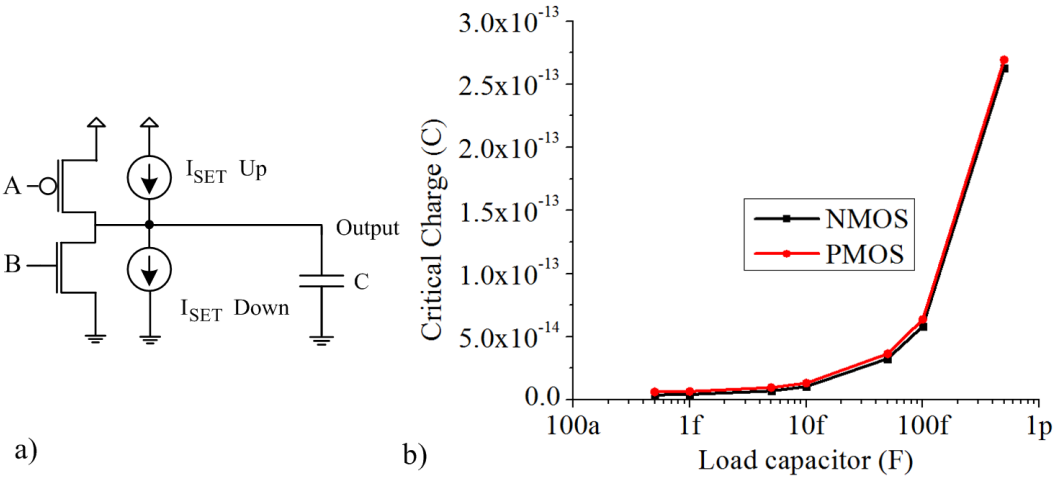


Figure 2.9: a) Test bench, b)Critical charge relative to the load capacitance for same size (W/L=0.135μm/0.06μm) NMOS and PMOS transistors of 65 nm Technology.

from "1" to "0". As far as the CC is concerned there is an increase if the capacitance on the output increases. On the figure, the CC of the PMOS is slightly larger than that of NMOS. This shows the effect of the mobility of the majority carriers. In NMOS transistors the mobility of electrons is higher than the one of holes in PMOS transistors. For this reason the carriers move more easily in NMOS transistors than in PMOS ones, easing the flow of current.

Now, the load is fixed at 0.33fC, which is the minimal capacitance for a metal capacitor in the 65nm technology kit. Choosing the minimal capacitance will show the minimum estimated CC of the technology. Figure 2.10 shows the difference between the critical charges of an inverter with same sizes NMOS and PMOS (0.135/0.06) transistors and larger ones ((0.24/0.06) for NMOS and (0.6/0.06) for PMOS). The larger ones correspond to the actual size of a transistor in the design of the combinatorial function. As the transistor size increases the critical charge increases as well.

At first sight for same size transistors PMOS are less sensitive to ionization than NMOS, since their CCs are larger, as it was explained before. When the size is increased the output node capacitance increases because of the parasitic capacitances of the transistors, thus both transistors become less sensitive. But since the PMOS transistor is larger than the NMOS transistor in this inverter, the PMOS transistor becomes more sensitive than the NMOS. To explain the mechanism behind this effect, in Figure 2.11 a) simplified models of the behavior of MOSFET transistors are exposed. Conducting and non-conducting states are represented by diodes and

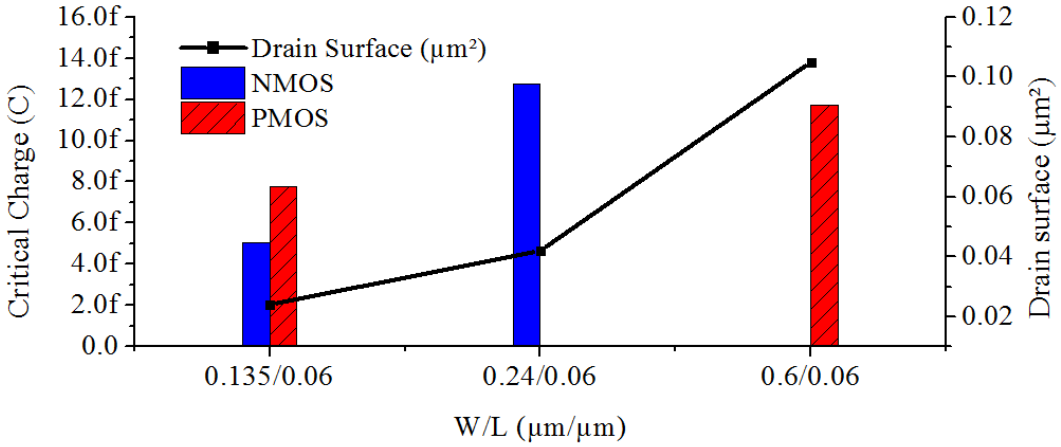


Figure 2.10: Critical charges relative to the transistor size.

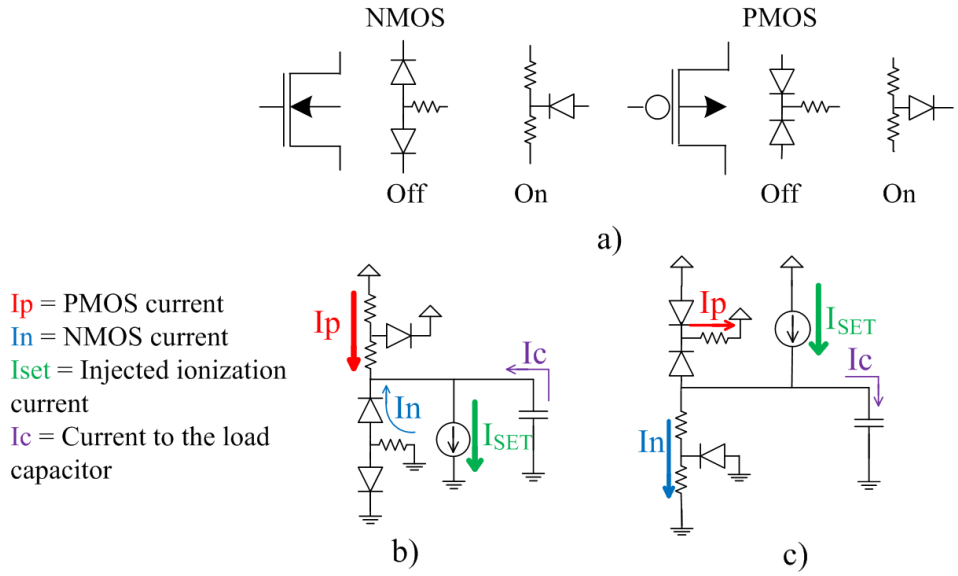


Figure 2.11: a) Simplified models for the "On" and "Off" states of MOS transistors, b) Fault injection on the NMOS when the inverter output is 1, c) Fault injection on the PMOS when the inverter output is 0.

resistors. Those simplified models are used in the two inverter states in Figure 2.11 b) and c).

When the output of the inverter is 1 (Figure 2.11 b)), only the PMOS transistor is on. Since the PMOS transistor is larger than the NMOS, its resistance is lower even if the mobility of the carries in the PMOS is larger than the NMOS. If an

impact occurs, there are charges from the capacitor that will leave. The PMOS can compensate rapidly the I_{set} current thanks to its low resistance. This makes the NMOS less sensitive to ionization. Because of Kirchhoff law there is a small current from the NMOS bulk, validating the bulk drain phenomenon of ionization. On the other hand, when the output of the inverter is 0, charges enter the capacitor (Figure 2.11 c)), since the NMOS transistor is smaller than the PMOS, its resistance is larger. In this case, it is more difficult to evacuate the I_{set} current through the NMOS transistor making the CC of the PMOS transistor smaller.

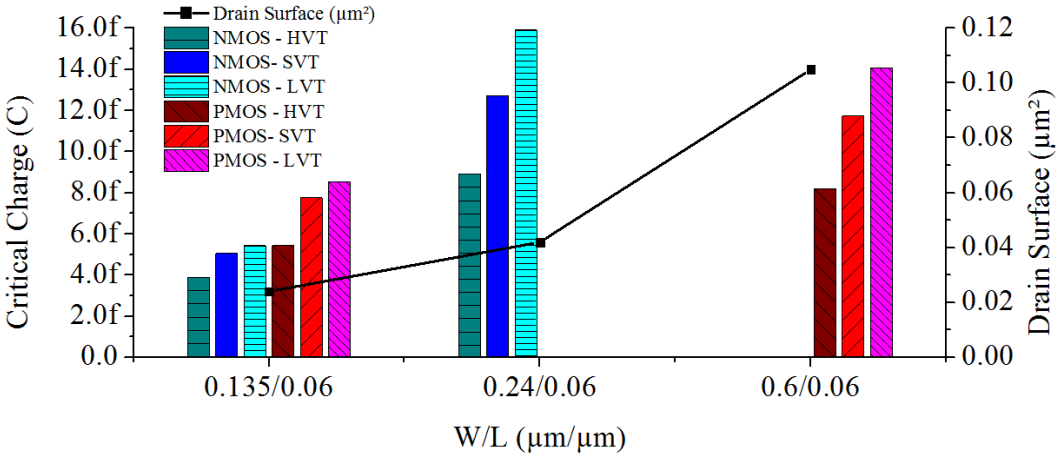


Figure 2.12: Critical charges relative to the transistor size.

One last aspect to consider is the transistor type. For the previous analysis standard voltage threshold (VT) transistors (SVT) were used. Two other types exist: High-Vt (HVT) and Low-Vt (LVT). HVT transistors need less current than SVT to be turned on, whereas LVT transistors require more current than SVT to be on. That is why Figure 2.12 completes Figure 2.10 with the critical charges depending on the transistor type. Figure 2.12 shows that HVT transistors reduce by nearly a third the value of the CC in relation to SVT transistors of the same size because less current is needed to turn them on, in contrast to LVT transistor which need more current though their CC is greater. LVT transistors can be a good option to diminish the sensitivity, but they have a high drain-source leakage current and they are not suited for low power applications.

2.2.2 CRITICAL CHARGE IN NOR FUNCTIONS

The previous part was focused on an inverter. In this part the complexity is increased and NOR functions are going to be analyzed. In the first place a NOR2 function

is studied followed by a NOR8. The general form of a multiple input NOR-gate is shown in Figure 2.13, with NMOS transistors with a drain size of 0.024 μm^2 (W/L = 0.135/0.06, minimal size of the technology) and 0.095 μm^2 (W/L = 0.54/0.06) for PMOS drains. The analysis was made for the worst case scenario in relation to how the function works during an ADC cycle. During the operation of the ADC, this function has two states at its inputs. The first state consists in "0" in all inputs during the standby time. This state is used to measure the CC for the NMOS transistors. In the second state, during the operation time, only one input is "1" and all the others are "0". This state is used to measure the CC for the PMOS. In addition to that, when an input C_i is set to 1 the SET is introduced at node N_i (see Figure 2.13). This introduces a new node voltage which modifies the nearby transistors polarization and can turn on the off ones. Most of the I_{SET} current runs to the bulk of the transistors connected to the same node, but if around 50 μA manage to reach the output node N_0 through the on-transistors (in ohmic mode), the logic state at N_0 can change and change the state of *Internal CLK*.

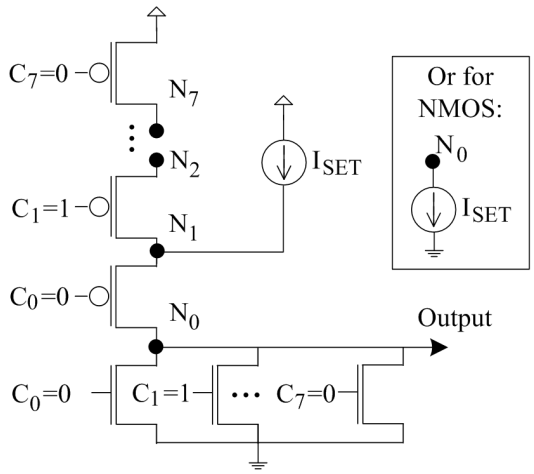


Figure 2.13: Architecture of a NOR gate with multiple inputs, and fault injection during the functioning cycle.

Figure 2.14 shows the CC in the NOR2, for the transistors in each node for the switching configurations cited before. As it was previously done for the inverter, the results from Figure 2.14 are analyzed with a simplified scheme as shown in Figure 2.15.

When an SET is injected, currents from the neighboring lines bring currents to assemble this SET current by Kirchhoff law. This can be seen as the current has to be evacuated by as many paths as possible. With this in mind, when an NMOS is hit, in the situation illustrated in Figure 2.15 a), the I_{SET} current is mainly composed

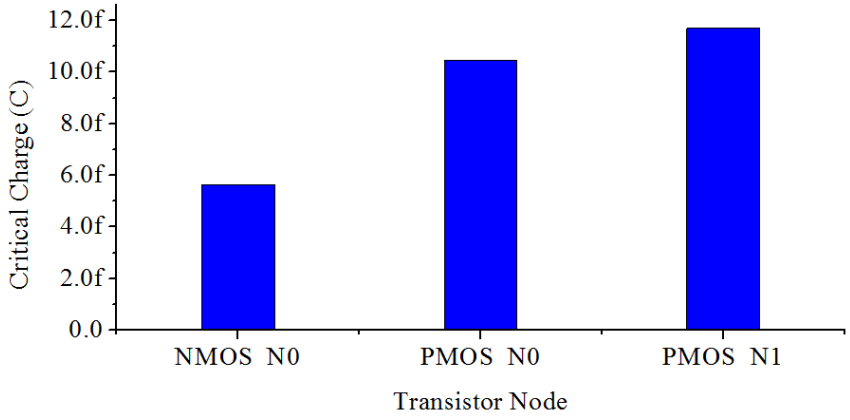


Figure 2.14: Critical charges for the NOR2 gate.

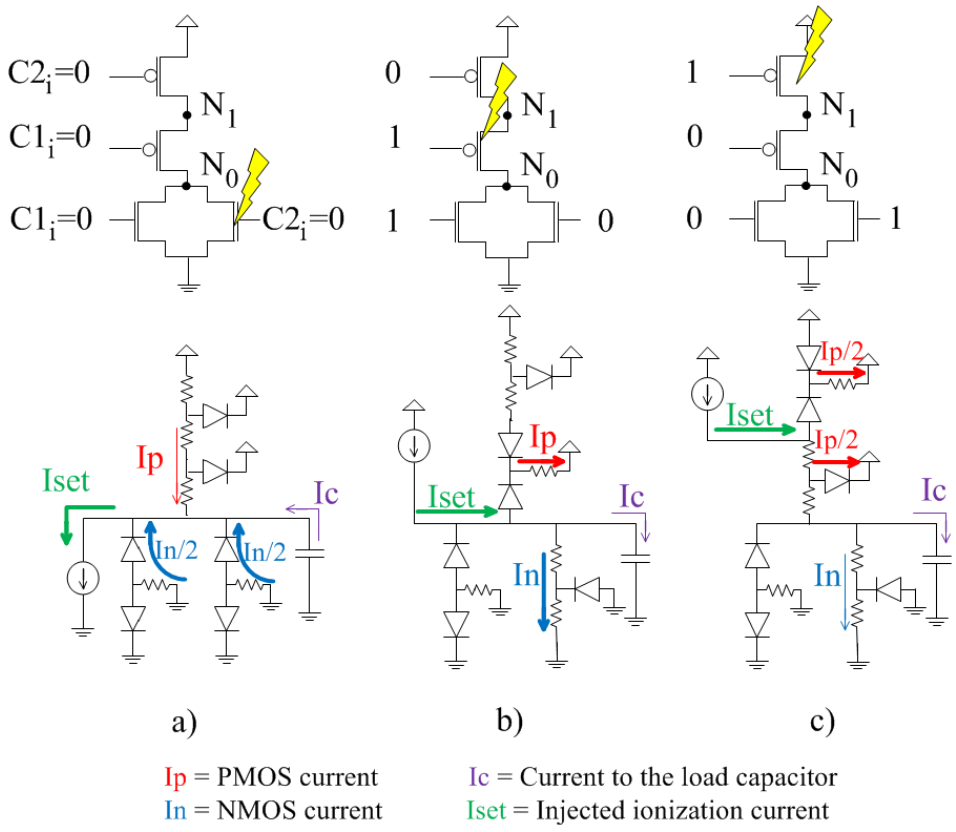


Figure 2.15: a) Fault injection on one of the NMOS when the NOR2 output is 1, b) Fault injection on node N_0 when the inverter output is 0, c) Fault injection on node N_1 when the inverter output is 0.

of currents from the bulk of the NMOS transistors going directly to the node N_0. The difference of critical charge with the situation in Figure 2.15 b) comes from the fact that a part of the SET current is evacuated through the PMOS bulk, bringing less current to load the output capacitance. That is why the parallel NMOS are more sensitive than the PMOS in node N_0. Now for the PMOS on node N_1 (Figure 2.15 c)), the critical charge of this node is larger than that of N_0, because I_{SET} can be mainly evacuated by the two neighboring paths to the bulk of the PMOS transistors. Thus a greater I_{SET} current is needed to upset the output node. Those mechanisms are also observable in a NOR8 gate.

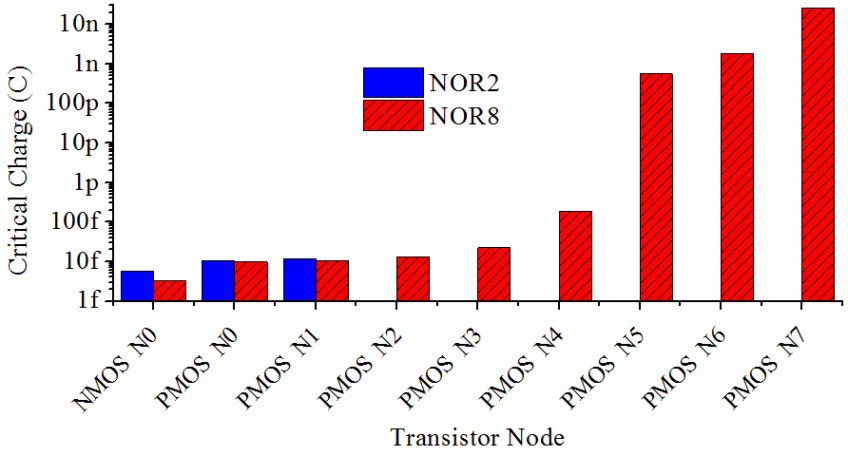


Figure 2.16: Critical charges for the NOR2 and the NOR8 gate.

Figure 2.16 shows the CC for all transistors in the NOR2 and NOR8 structure. A first observation is that in relation to the NMOS in the NOR2, the CC of the NMOS in the NOR8, has been divided by two. The only difference at N0 between a NOR8 and a NOR2 is that in the NOR8 eight NMOS transistors are in parallel instead of two. As illustrated in Figure 2.17, it is clear that this parallelism has weakened the node because the equivalent resistance of the off-NMOS transistors diminished with the number of parallel transistors easing the flow of current.

On the other hand, for nodes N0 and N1, PMOS are not affected by the NMOS parallelism and they keep almost the same CC. For nodes after N2 the CC increases. For N4, the CC is about 50 times that of N0 and for nodes after N4 CC has increased over 100 000 times. CC values for N5 to N7 show that LET has to be incredibly high. If such LET is reached the circuit will be damaged. As depicted in Figure 2.18, serialization of the transistors brings hardening to the architecture brings several paths for the evacuation of the SET current before arriving to the output node. This makes more difficult the propagation of the current to the output node.

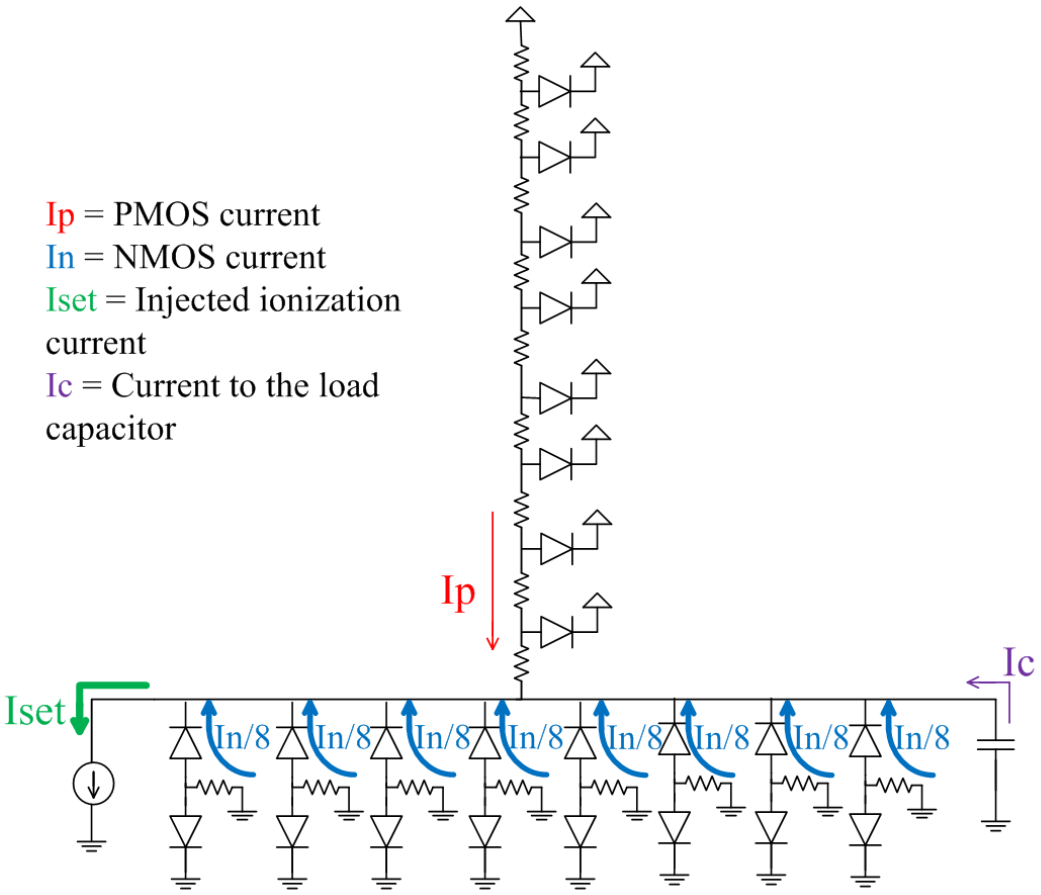


Figure 2.17: Fault injection in a NMOS transistor in the NOR8 gate.

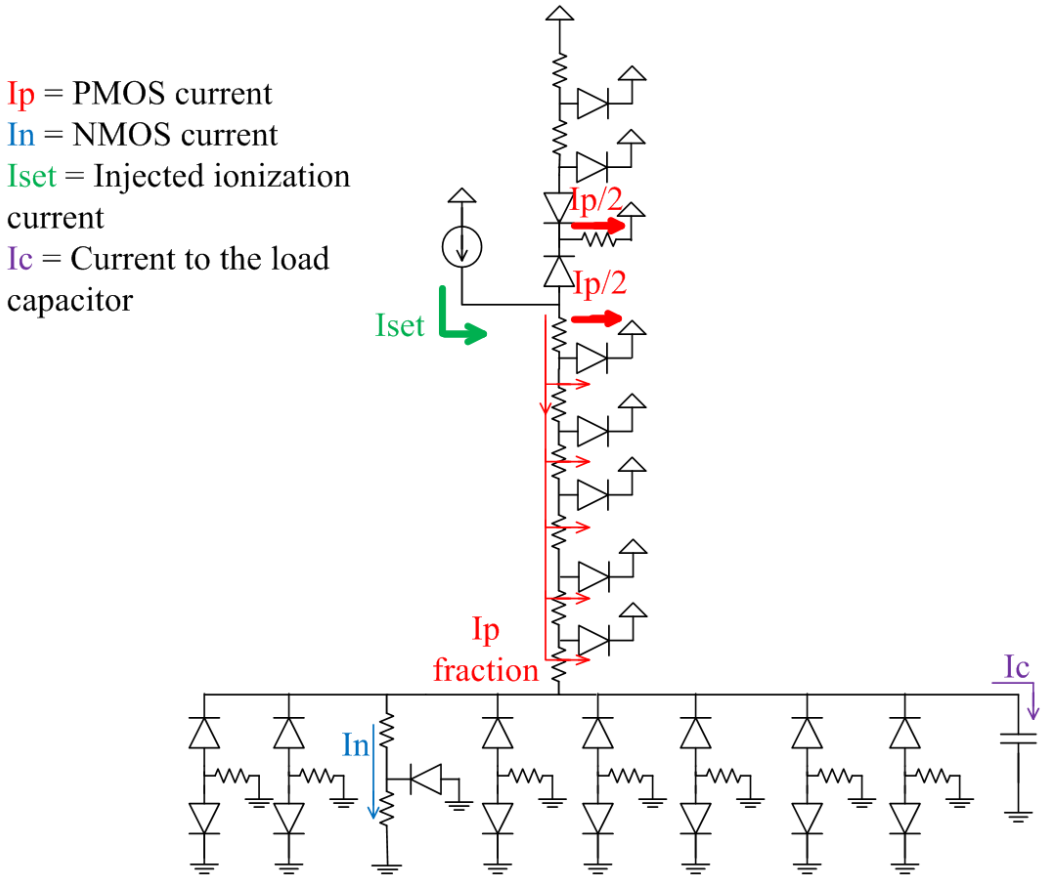


Figure 2.18: Fault injection in a PMOS of en elevated node in the NOR8 gate.

This ends the critical charge analysis of the three components of the combinatorial function of the SAR ADC: the inverter, the NOR2 and the NOR8 gates. This part exposed the electrical part of the analysis, on the next part the combinatorial CLK generator function is going to be studied in a geometrical point of view.

This electrical sensitivity study has shown that the CC increases with the capacitor load of a node. Also that the CC increases as the size of transistors increase. LVT transistors have a greater robustness against SETs than SVT and HVT transistors, HVT being the most sensitive of the three. The leakage current of the LVT transistor is a major drawback if low power applications want to be hardened by those transistors. As far as the structure of the gates is concerned the CC increases with serialization and CC decreases with parallelism in a node. The most sensitive node of the gate is clearly the output node, but in a series structure, nodes close to the output (e.g. nodes N_1, N_2, N_3 in Figure 2.16) have a sensitivity

close to that of the output node. This shows that SET at the output are not only caused on particle hits on the transistors of the output node but also if those hits strike other parts of the structure. With that observation, the geometry of the gate comes to mind, and the next question would be if the geometry of a function on the layout has an impact on the soft errors generation.

2.3 GEOMETRICAL SENSITIVITY

In this section is wanted to study the effect of the radiation strike location on the layout of the CLK generator using the concept of cross sections. The cross section concept was described in Chapter 2 Section 1.4.3. In that section a simplification of the cross section determination was given. Based on that method and using the collected charge model, a study of the cross-section is going to be conducted for the CLK generator function of the SAR ADC. The critical charges determined before will be used.

2.3.1 CRITICAL CHARGE ACTION RADIUS

The CC analysis allows calculating the minimum distance, from the impact to a transistor's drain, required to cause a state change at the output of the function. In this section, it was determined for the smallest sensitive drain surface (0.175 x 0.135 μm^2), in the ST 65nm CMOS technology. Figure 2.19 shows the collected charge as a function of the radius from the impact center to the drain.

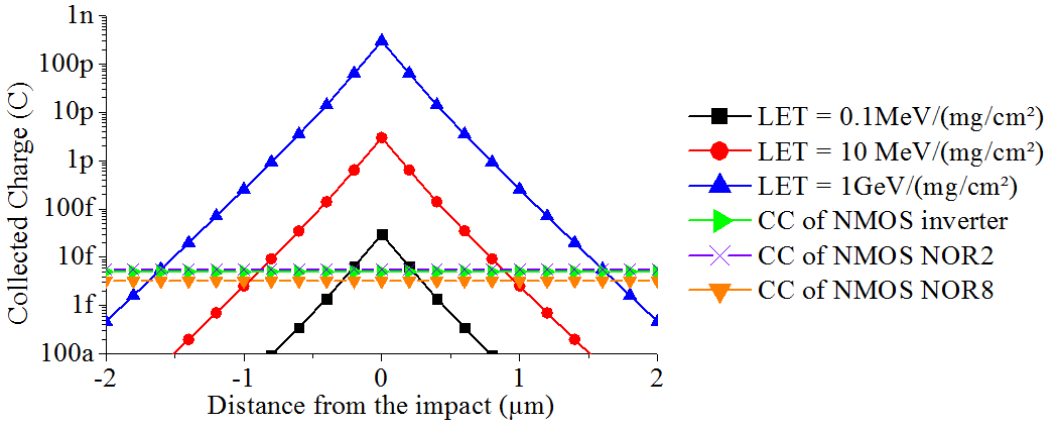


Figure 2.19: Collected charge by the smallest 65nm CMOS technology drain surface relative to the distance of the center of the hit for different LET values.

The CC of the drains of the NMOS transistors will determine the threshold of the action radius of the particle hit. This distance varies depending on the particle

energy until it reaches saturation. For example, a particle hit with an LET of 10MeV can affect the NMOS drains at a distance of nearly 1 μm. This means that any drain of the combinatorial function located at less than 1 μm will collect enough charge to induce an SET. In addition, increasing 100 times the LET increases the radius in about 0.5 μm.

2.3.2 CLK GENERATOR FUNCTION LAYOUT

In previous sections, the effect of a radiation impact was presented for one drain at a time. In this part the objective is to see the cross sections and the influence of the geometrical repartition of the transistors on the layout. This study is done for each drain in the combinatorial function which creates the *Internal Clock*. Another aspect to take into account is the logic state of the function. Indeed some transistors are going to be active and others are not and this inherently will show the difference of sensitivity relative to the logic state of the function.

The set up for the simulations is the one presented in [GTSAJ13]. Different impact points were chosen to highlight the different effects taking place on different zones of the circuit during an *Internal Clock* cycle. In [GTSAJ13] was introduced the concept of action radius, which defines the maximum distance between an ionization impact and the drain of a transistor in which the collected charge can reach the critical charge. This allows the generation of the SET cross-sections for the drains or in other words the sensitive areas of each drains critical charge. Those cross-sections were determined for individual drains. Ground and source connectors gather the charge deposited near them. That is why a final consideration was made by avoiding the influence of the source and ground connectors to observe the interaction with the different sensitive zones of the drains. For this geometrical study a layout of the combinatorial function was created. For the simplicity of the study, the layout shown in Figure 2.20 sketches only the n-type and p-type diffusions, and the gate oxide layer. The drains are indicated by a D.

In order to show the cross sections, an LET = 10 MeV.mg^{-1}.cm^2 is chosen as an example. For an LET of such magnitude, for the 65nm technology, the cross section can show saturation, as it is shown in Roche *et al.* work [RGU$^+$10]. This may vary and here the value is just used to study the variation of the cross section as an example. The most accurate value can be given by SEU testing with laser or in particle accelerators.

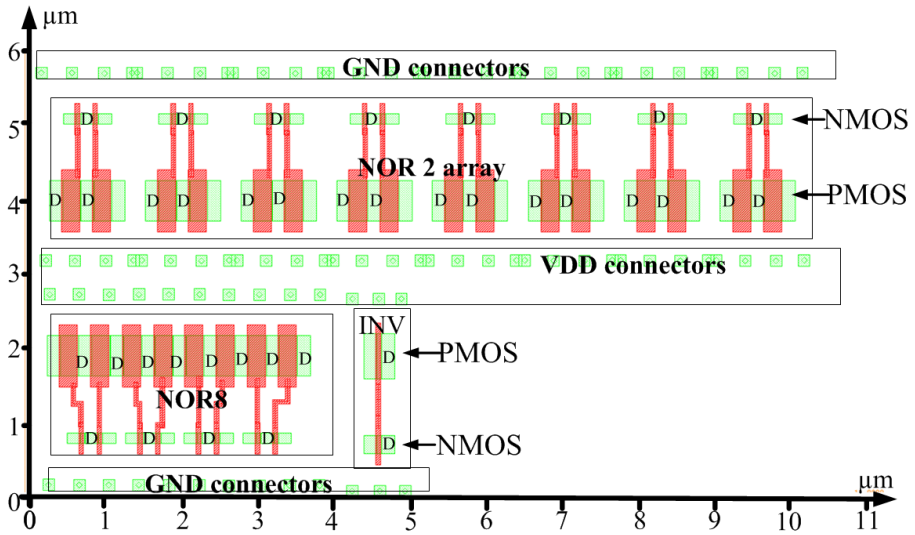


Figure 2.20: Layout of CLK generator function controlling the *Internal Clock* signal.

2.3.3 Logic states and cross section

The cross sections of the transistors where an SET can take place are going to be independently studied depending on the combinatorial state. The cross sections were determined using the model explained in Chapter 2 in Section 1.4.1 and the approximation explained in Section 1.4.3. The critical charges obtained in the study of Section 2.2 were used to determine the action radius in Section 2.3.1. The action radius is the distance between the drain and the external border of the surrounding sensitive area.

The combinatorial function has eight pairs of $C1_iC2_i$ inputs, with 'i' noted from 0 to 7. When the cycle begins, the input pairs are $C1_iC2_i$ = "01" and *Internal CLK* is "0". Figure 2.21 shows the zones where a particle with an LET less or equal to 10 MeV.mg^{-1}.cm^2 can generate an SET in the *Internal CLK* signal. Those zones surround the active transistors drains. The black lined rectangles delimit the area where no contacts to the ground or the source are present. The total sensitive areas seem to cover almost the whole circuit.

In the first iteration the pair $C1_0C2_0$ switches to "00" and the rest remain the same, making *Internal CLK* equal to "1". Figure 2.22 shows a completely different figure compared to the previous one. In this case, the cross sections that can induce an SET able to generate a "0" at the output are shown. At the end of the first

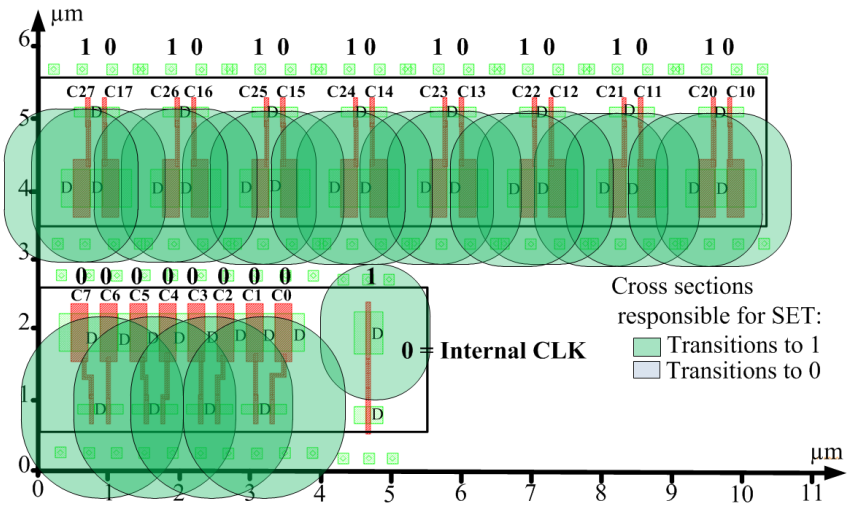


Figure 2.21: Cross sections of transistors at the beginning of the cycle.

iteration $C1_0C2_0$ finally switches to "10", making *Internal CLK* equal to "0" again. Then the same process happens successively to the other pairs. At the end of the cycle all pairs $C1_iC2_i$ are "10". Figure 2.23 shows a similar situation as showed in Figure 2.21. The only difference is on the cross section of the PMOS transistor associated to the C20 input, but the general shape of the sensitive area does not change.

The Figures 2.21 and 2.22 highlight the fact that the cross section shape of the transistors may change depending on the logic state. The Figure 2.24 illustrates the remaining states during the iterations of the cycle making *Internal CLK* "1". An evolution is observable. For the transistors in the array of NOR2 gates the cross section fades away as the cycle moves forward. And on the contrary for the NOR8 gate the cross section becomes larger. For the last three iterations the cross section for the PMOS transistors on the NOR8 gate does not change. This stability is caused by the high critical charge of those drains. That result is in perfect concordance with the critical charges of the NOR2 and NOR8 of Figure 2.16. The only aspect that all the cross section figures presented in this section have in common is that most of the cross sections intersect with neighboring ones. This reveals the possibility of MBUs in the CLK generator.

2.3.4 Combined cross sections and combined SET effects

Taking into account that neighboring transistors can be hit at the same time and their effects can be superposed. Here the cross-sections of all the drains were super-

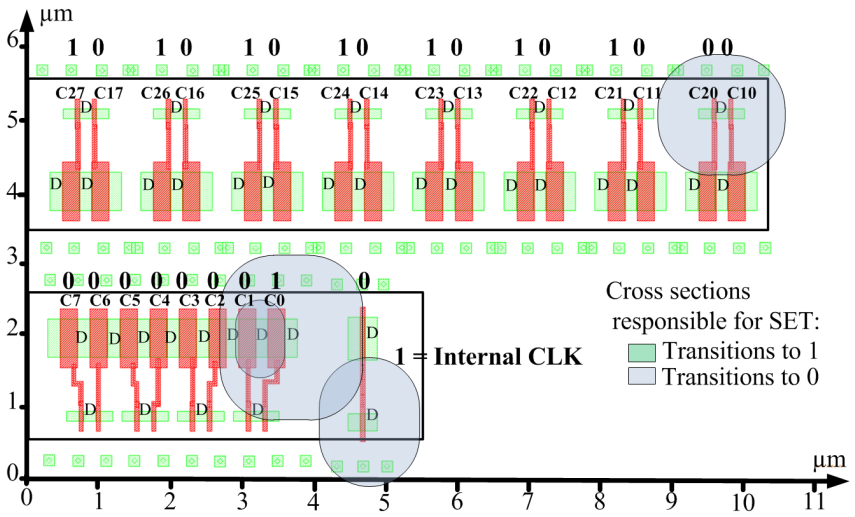


Figure 2.22: Cross sections of transistors at the first iteration of the cycle.

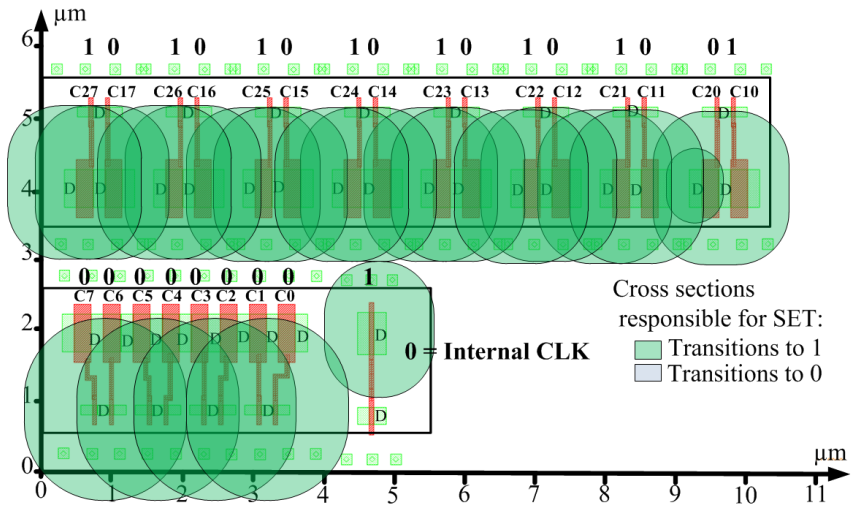


Figure 2.23: Cross sections of transistors at the end of first iteration of the cycle.

posed for the last iteration of the CLK generator logic function. A cartography of SET is going to be presented.

This study focuses on observing the effects of the SET when all the drains are taken into account and several impact simulations were made. The study concentrates on thirty interesting impacts. The impacts where chosen to see the interaction between NMOS and PMOS transistors.

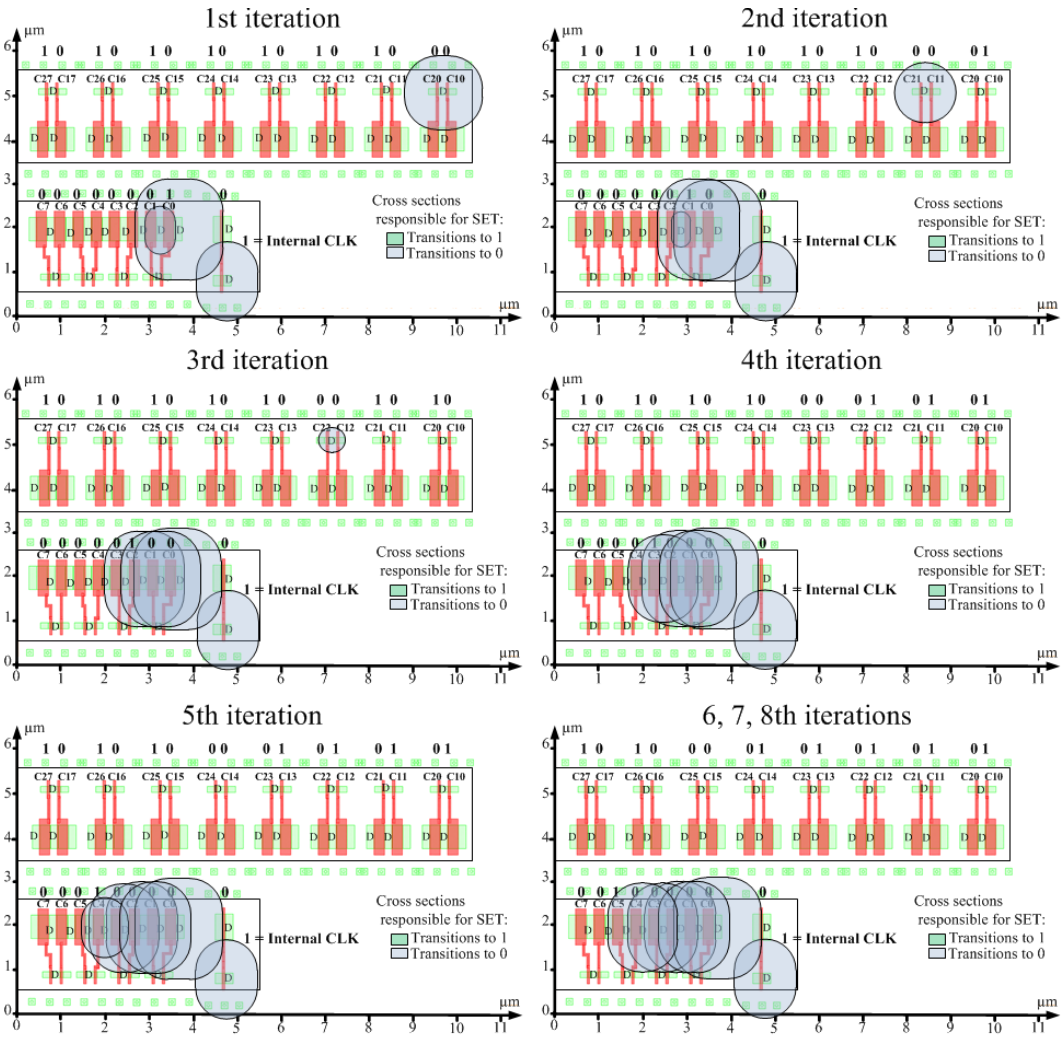


Figure 2.24: Evolution relative to the iteration of the cross section of the drains able to induce a transition to 0 when *Internal CLK* is "1".

Figures 2.25 and 2.26 show all the cross sections and the effects of the chosen impacts. Four situations for an impact can arise. The impact can change the logic state, it can just extend the actual state, it can change and extend the state, or it has no effect. the figures show the effects of the set of thirty impacts in two different logic state. Those figures show that they are the negative of the other for the change

of state and delay effects of SETs. The first remark from those figures is that if same color cross sections intersect each other the effect of an SET is the one expected. For instance in Figure 2.25, an SET hitting a full transition to 1 zone (green zone) the expected effect is that there will be an extension of the same logic state. Here state "1" will be longer. On the other hand if two different cross sections superpose the frontier that defines the final effect changes. This can be seen between the coordinates $2 < x < 3$ and $1 < y < 2$ and $4 < x < 5$ and $1 < y < 2$. In these zones where a transition to 1 is supposed to happen a transition to 0 was observed and vice versa. Even in some punctual intersections both effects can take place. A final remark is that the change of state SET is preponderant when the state of *Internal CLK* is "0" than the opposite. Indeed the geometrical repartition of change of logic state impacts (red crosses) is larger in Figure 2.26 than in Figure 2.25. The conclusion to this fact is that geometrically a transition to 1 is more possible than a transition to 0. Thus a logic state of the combinatorial function is more sensitive than the other.

What should be noted from this study is that the pull-up and pull-down parts of a combinatorial function try to compensate the SET effect if the impact happens on the superposition of two different transition cross sections. This reduces the effective area where an SET can take place. But of course this is not enough to avoid or even mask all the SETs. This points-out the complexity of the relations between the zones. Near the output node, the sensitive areas from the NOR8 gate and the INV gate meet and in this zone can take place an SET whatever the output state is. In addition to that complexity, it should not be forgotten the MBU sensitivity caused by the intersection of cross sections. The electrical and geometrical sensitivities were exposed showing the complex relation between a combinatorial function and its sensitivity to SETS, the remaining aspect is what happens over time for the complete ADC system. This is the subject of the next section.

2.4 TEMPORAL SENSITIVITY

The study of the CLK generator in the SAR ADC will show the consequences of the effects of an SET occurring in this function. This combinatorial function is in a feedback loop between the SAR asynchronous logic and the comparator. A soft error in the CLK generator function can affect directly the comparator and indirectly the SAR logic. In the first place is going to be presented how the ADC stores the bits for the output code during one bit cycle. Then, are going to be exposed the effects of SETs in the memorization process of the SAR logic. Finally temporal analysis results are drawn.

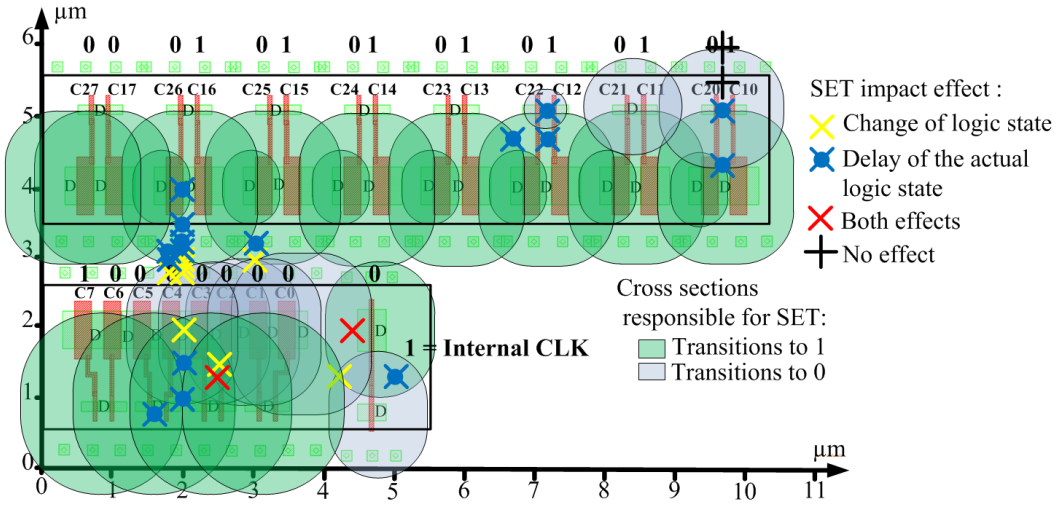


Figure 2.25: Cross sections and SET effects depending on the location of the impacts for the last iteration when *Internal CLK* is "1".

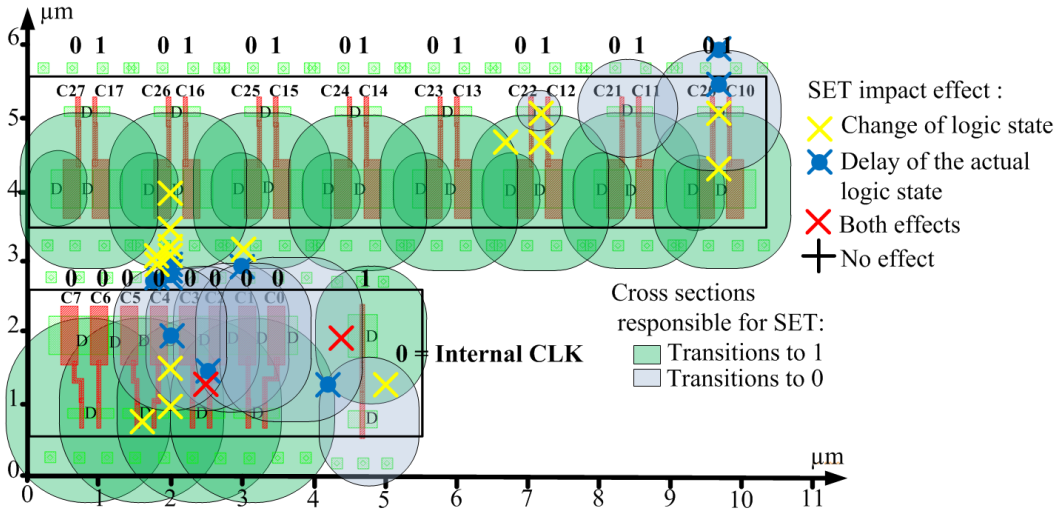


Figure 2.26: Cross sections and SET effects depending on the location of the impacts for the last iteration when *Internal CLK* is "0".

2.4.1 THE BIT CYCLE

The bit cycles is organized by the asynchronous logic. The state machine with the ACU and the DCU block orders the process. The scheme for the couple ACU and DCU is illustrated in Figure 2.27. Figure 2.28 a) shows the state machine associ-

ated to ACU and DCU. The process begins when *Bit-set* is set to "0", this is the initialization. Then when *Bit-set* = "1" (T0 on the timing diagram Figure 2.28 b)) the state $C1_iC2_i = 00$ is reached, the combinatorial function has to activate the comparator by setting *Internal CLK* signal high. When the comparator is ready (at T1) $\overline{CompRdy}$ is "0" and the value of *Comp out* is loaded in the DCU to set *Bit-rdy*, this is the memorization process. The cycle ends when the value is stored and the signal *Next-bit-set* is set to "1" to activate the next ACU and DCU pair (at T2).

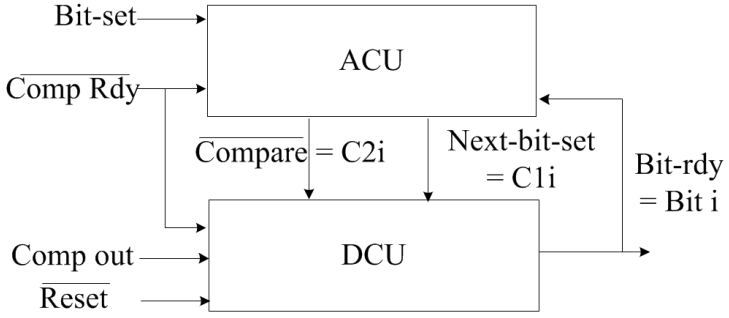


Figure 2.27: ACU and DCU interconnections [HZB+11].

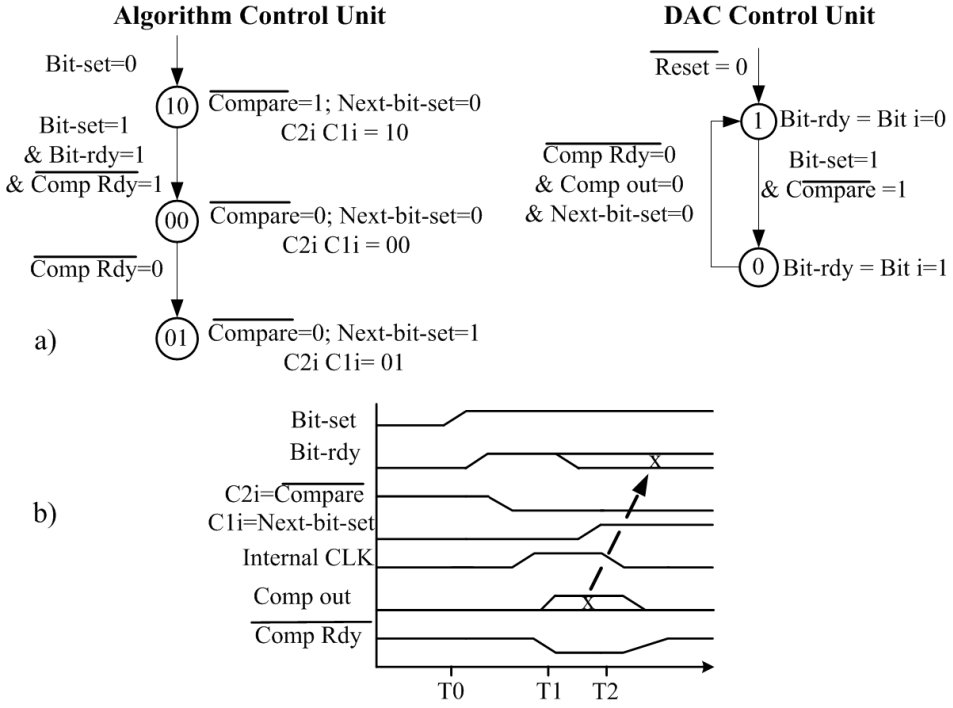


Figure 2.28: a) States machines of ACU and DCU, b) Timing diagram for one bit cycle [HZB+11].

2.4.2 THE SET EFFECTS

The normal functioning cycle being exposed, the study moves on to the effects of an undesired transition of *Internal CLK* signal. If a glitch occurs on this signal out of the memorization process, the comparator will be activated before the logic demands it and $\overline{CompRdy}$ will be "0" before it is required. In this case the SET propagates only to the comparator, but without consequences for the output code. On the other hand if the SET takes place during the memorization process two effects take place during the simulations.

The first one illustrated in Figure 2.29 shows when the *Internal CLK* is "1" the comparator returns the result of the comparison and if *Internal CLK* is "0" the comparator output is systematically "0". $\overline{CompRdy}$ will become "0" when the comparison is ready after *Internal CLK* is "1". If *Internal CLK* suddenly becomes "0" between T1 and T2, a "0" might be stored (*Bit-rdy* = "0"). If the transient effect finishes before T2, the correct value will regenerate and the correct value will be stored. If the soft error happens for an LSB, the error is in the tolerance zone, but if this happens for an MSB then the error can be in the worst case of 50%. This means that some output codes can be less harmed than others. In order to make a link with the geometrical approach, the soft error described here can happen during the situation described by Figure 2.25.

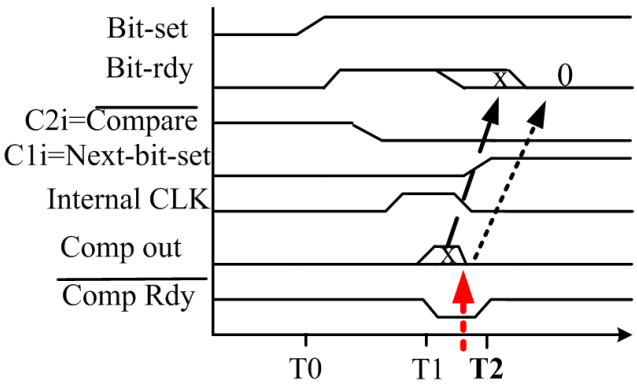


Figure 2.29: Timing diagram of an SET causing an anticipated transition to 0 of *Internal CLK* during the memorization process.

The second effect is illustrated in Figure 2.30. The error takes place when two *Internal CLK* pulses are too close in time. The causes can be either an undesired transition to "0" while *Internal CLK* is "1", or a transition to "1" just after *Internal CLK* went to "0". This is understood by the logic as two bit cycles, where in reality there is only one. In Figure 2.30 when the SET takes place, *Internal CLK* is "0". The state machine considers that the cycle is over ("T2") and the state machine of

the next pair ACU-DCU has to be activated (*Next-bit-set* is set to "1"). In the same moment an indetermination state occurs in $\overline{Compare}$ signal causing the bit to be set at "1". Since the SAR logic has already begun the next cycle and the result cannot be corrected. In order to make a link with the geometrical approach, the soft error described here can most likely happen during the situation described by Figure 2.26.

Those two effects show how an SET generated on the CLK generator function can cause SEUs on the DCUs modules. By the two types of effects it is clear that the memorization time, between T1 and T2 is the most vulnerable moment of the cycle. An error may cause the rest of the code to be false. During the whole SAR cycle, the most significant bits (MSB) are the ones that can change the output code dramatically.

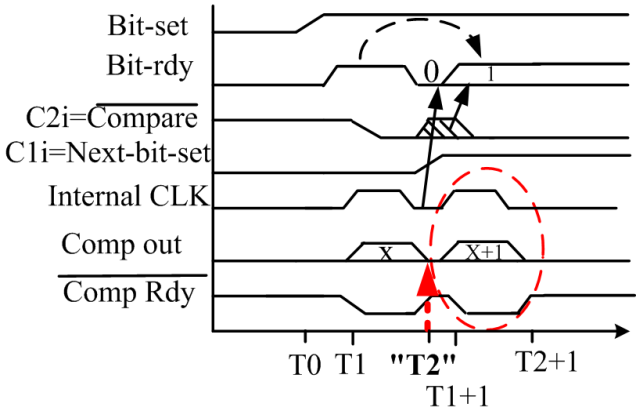


Figure 2.30: Timing diagram of an SET causing an anticipated transition to 1 of *Internal CLK* during the memorization process.

2.4.3 TEMPORAL SENSITIVITY RESULTS

Based on the effects shown before, the idea is to determine the time windows where those errors can take place. A summary of the effects is depicted in Figure 2.31. There are SETs that only extend the same state (as shown by the SETs a) and c)) and only generate a small delay for the end of the cycle. SETs b) and d) cause SEUs in the DCU modules and caused by the effects explained on the previous section. The SET in b) corresponds to a transition to from "1" to "0" (see also Figure 2.25), and The SET in d) corresponds to a transition to from "0" to "1" (see also Figure 2.26).

In order to evaluate the temporal sensitivity to SEUs (TSS), the latching window in which the SEU can take place is compared to the whole ADC cycle (*cf.*

Equation 2.5). The latching windows where determined using CADENCE simulation. The results are that for every bit cycle a transition from "0" to "1" with an SEU has a latching window of 0.6 ns. For the transition from "1" to "0" with generation of an SEU has a latching window of 0.25 ns. The functioning cycle period of the simulated ADC is 35.9 ns, and the latching windows occur 8 times in one functioning cycle. This means that the transition from "0" to "1" is not only predominant in a geometrical point of view but also in terms of time. The TSS is reported on Table 2.2.

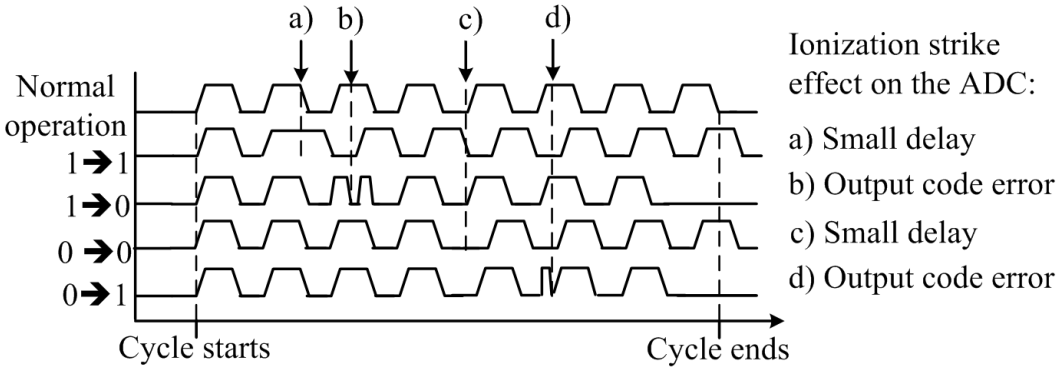


Figure 2.31: Timing diagram of the *Internal CLK* possible soft errors and their effect on the ADC during a complete functioning cycle.

$$Temporal\ sensitivity\ to\ SEU\ (TSS) = \frac{Latching\ Window \times 8}{Cycle\ period} \times 100 \qquad (2.5)$$

Transition	**Latching window**	**TSS**
"0" to "1"	0.6ns	13.4%
"1" to "0"	0.25ns	5.57%

Table 2.2: TSS for the latching windows

2.5 CONCLUSIONS

In order to study the sensitivity of a system to ionizing radiation, a low power SAR ADC was chosen. This complex system can show the consequences of SET on a whole system. The SAR ADC was adapted to the ST Microelectronics 65 nm

CMOS technology kit and a particular combinatorial function reveled to be critical for ADC.

The study presented in this chapter showed three analysis of sensitivity for the CLK generator function that were presented at the international conference IEEE MWSCAS in august 2013 [GTSAJ13]. First an electrical analysis was done with the critical charge criteria. It was found that the CC increases with the load and with the size of the transistors. Also PMOS transistors are slightly more inherently hardened than NMOS, because of its lower carriers mobility, and LVT are less sensitive than SVT and HVT. Finally thanks to the study of the NOR2 and NOR8 functions, it was determined that the parallelism of transistors in an output node decreases the CC, while the CC of series nodes increases with serialization.

The second analysis was focused on a geometrical point of view. The soft error cross section showed a variability depending on the logic state, thus over time. It was showed that an SET that causes a transition to "1" was more likely to happen because of the size of the cross sections where such an event can be generated.

The last analysis was done over the sensitivity of the ADC cycle to SETs that are generated in the combinatorial function and propagate to finally generate an SEU on the DCU modules that make the SAR register. It was showed that 19% of the whole cycle is sensitive to SEUs and an SEU is most likely to happen when a transition to "1" occurs because of an SET on the CLK generator.

Finally, the exhaustive study presented in this chapter highlights the issues of the ionizing radiation on a critical function and how SETs propagate to disturb other parts of the ADC. For the 65 nm technology, an ADC circuit is vulnerable to SETs. The study conducted on the state machine of a digital asynchronous state machine can be applicable to digital circuits in general and shows the necessity for an SET compensation. The results from the three different points of views show that determining the sensitivity of a function is complex, and involves taking care of electrical, geometrical, and temporal aspects. With the intention of hardening this function against radiation, a radiation hardening technique has to be chosen. Different approaches exist and they are going to be presented in the next chapter. It could be interesting to apply a hardening technique that does not require much power, area and time overhead. Another aspect that would be practical is to apply the hardening without modifying the function that is wanted to harden, so the hardening design process can be brief. Ideally, this hardening should be placed at the output of the function in order to stop SETs so that the cross sections of the hardening and the function do not intersect avoiding MBUs in the function and the hardening.

Chapter 3
Radiation hardening techniques

Since the reliability issue affects electronic systems not only in space but also on a terrestrial level, it is imperative to have radiation hardening strategies for systems. To counter those effects many radiation hardening techniques exist. Some are technological and others by design. In this chapter the different radiation hardening techniques will be reviewed. Afterwards a qualitative comparison will be drawn for those techniques. Considering the results from the study of the SAR ADC under the effects of radiation and the information from the radiation hardening strategies, a discussion over the stakes for radiation hardening by design strategies will take place. Based on that reflection, a particular temporal redundancy technique, the temporal filtering, will show its advantages in relation to other techniques. It has interesting features like low area, and low power overhead but with an increase in the propagation delay.

3.1 Radiation hardening classification

Radiation hardening techniques are categorized in two families: the technological hardening and hardening by design (*cf.* Figure 3.1). Technological hardening is applied in the fabrication process and uses the physical properties of materials to harden the integrated circuits. The other type of hardening is by design. This kind of hardening is applied during the circuit design process, and is more flexible than the technological approach. Indeed, hardening by design is applied at different abstraction levels in circuit design. From a transistor level up to a system level, design techniques adapt to the application requirements. Gate level techniques tend to increase the critical charge of the gate, function and system level techniques use redundancy to increase the reliability. Both families of hardening techniques are going to be presented in detail in the next two sections.

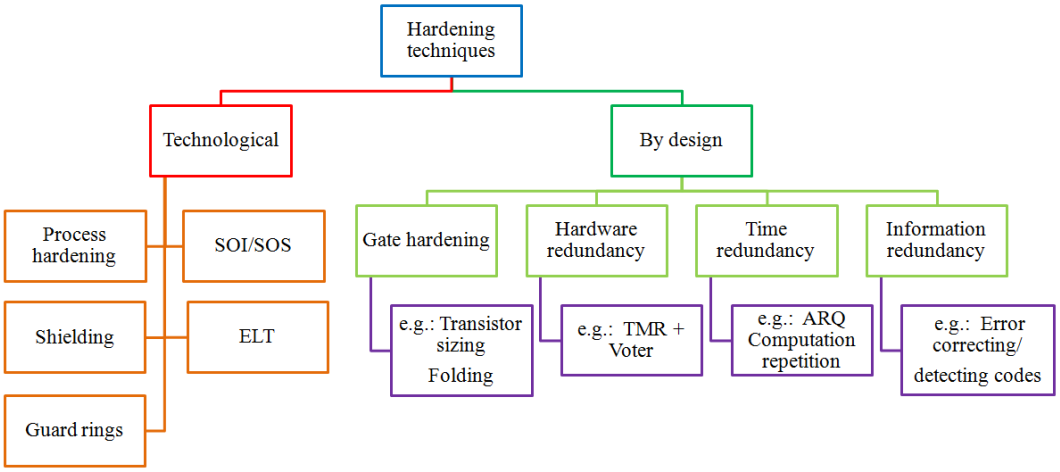


Figure 3.1: Classification of the hardening techniques.

3.2 TECHNOLOGICAL HARDENING TECHNIQUES

Technological hardening techniques for CMOS technology are applicable during the integrated circuits fabrication process. The main goal of technological hardening strategies is to use physical principles of materials to enhance the tolerance against SEEs and the degradation mechanisms such as the Total-Ionizing Dose (TID). Here will be presented the different techniques.

3.2.1 PROCESS HARDENING

Hardening against the degradation mechanisms implies to minimize the trapped charges in the transistor's dielectrics that disturb the threshold voltage. A large volume of silicon oxide favors the accumulation of holes [HSA02]. This causes a variation of the threshold voltage in relation to the silicon oxide thickness. Therefore, radiation hardened devices should have a silicon oxide layer as thin as possible. A thin oxide layer allows the trapped holes to annihilate by electron tunneling from polysilicon and silicon oxide interface [MA92].

The removal of impurities during the preparation and cleaning process of the gate oxide helps to improve the TID tolerance. Organic and inorganic contaminants might be present along with silicon dislocations. Those impurities affect not only transistor performance but also the radiation tolerance. Mechanical and chemical treatments help to remove the impurities cited before [HSA02]. Another type of purification process is the depleted boron in the borophosphosilicate glass (BPSG) passivation layer. BPSG is used for insulating protection for the integrated circuits.

The BPSG layer is depleted of the ^{11}Boron isotope because it can easily capture neutrons and induce an α particle decay generating soft errors [Bau01].

3.2.2 Silicon On Insulator (SOI), Silicon On Sapphire (SOS)

The SOI technology is characterized by an insulator layer between the silicon wafer substrate and the silicon layer with the PN junctions [CC03], as illustrated in Figure 3.2 b). The insulator layer is typically made of silicon dioxide or sapphire. Thanks to the isolation between n and p-wells SOI is SEL tolerant because there is no direct contact between the two types of transistors. The isolation benefits also to the power efficiency by reducing the leakage current. This technology is inherently radiation hardened because it significantly reduces the sensitive volume to ionization in relation to a classic Bulk technology as illustrated in Figure 3.2. A smaller sensitive volume decreases the charge collection mechanism because the ion tracks that can be created are shorter than those in Bulk technology. This reduces the transient induced current responsible for the soft errors. The main drawback of this technology is the increase in substrate cost, which contributes an estimated 10–15% increase to the total manufacturing costs but it is considered as a more than Moore promising technology [WN01].

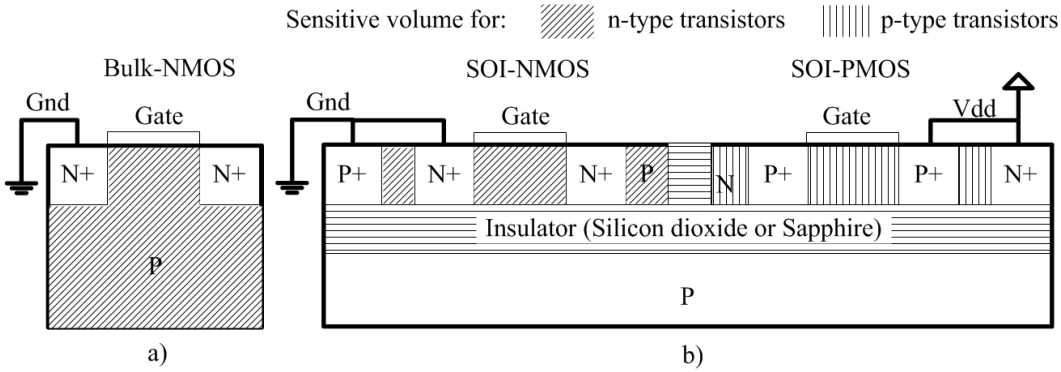


Figure 3.2: Difference of the sensitive volume between a Bulk NMOS transistor and a SOI NMOS transistor. a) Bulk NMOS transistor, b) SOI NMOS and PMOS transistors.

3.2.3 Shielding

Radiation shielding prevents SEEs by putting a physical barrier between the integrated circuits and the environment. Shielding for space microelectronics needs to

provide an acceptable ionizing protection with minimum shield mass. In general, the approach is to use a graded-Z shield to protect against charged particles and gamma rays. A graded-Z shield uses elements with high atomic number (high Z) like tantalum (Z=73). The idea is to have a high-Z layer between two low-Z materials, for instance a tantalum layer between two layers of aluminum (Z=13). A graded-Z shield reduces the electron dose rate by more than sixty percent. For protons, the optimal shield consists of a single low-Z material layer [FDRS96].

Electron transport in matter is a complicated phenomenon of several physical processes. Three of them are important for shielding space electrons: 1) inelastic scattering from atomic electrons, 2) elastic scattering from nuclei, and 3) the production of Bremsstrahlung photons. Protons are also a concerned for space applications since they are the most common particles in the primary cosmic ray flux. For proton shielding the optimal solution is a low-Z material, thus for both protons and electrons the three intercalate layer is still the best approach as illustrated in Figure 3.3.

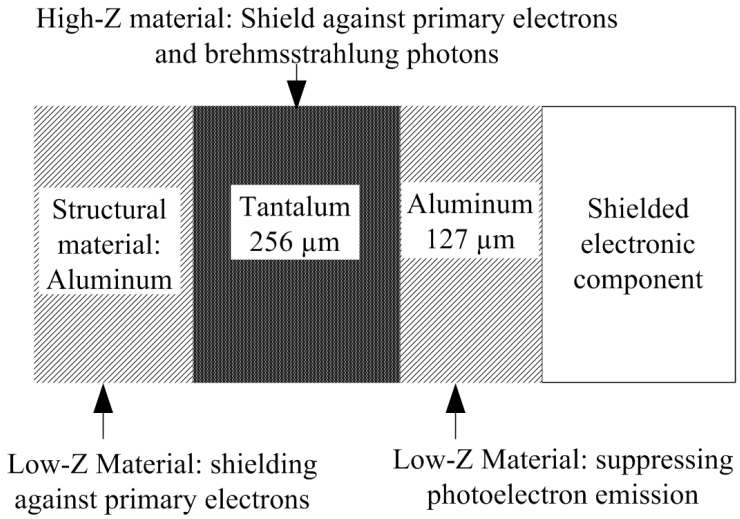


Figure 3.3: Cross-section of the shielding using intercalated low-Z layers with a high-Z layer.

For more terrestrial applications where neutrons are the main constituents of terrestrial cosmic rays, neutron shielding consists of three parts: Slowing down fast high-energy neutrons, absorbing the slowed down neutrons and attenuating the gamma radiation resulting of the scattering with the shielding material. In this case materials with high atomic number are not the most suited because neutrons can easily penetrate in those materials. The best are the hydrogen-rich (*e.g.* water, con-

crete) and hydrocarbons materials (*e.g.* plastic, paraffin), because the constituent particles have similar mass to that of neutrons (*e.g.* protons in hydrogen nuclei). Materials containing boron and cadmium are also good boron absorbers [MA92]. For this kind of radiation, not only an area overhead is expected but also a weight one because of the density of the shielding materials.

3.2.4 Enclosed Layout Transistors (ELT)

The Enclosed Layout Transistors technique focuses on radiation hardening against Total Ionizing Dose (TID) effects. The countered effects are the parasitic edge leakage currents between the drain and the source of a standard CMOS transistor [MOM87], and the field oxide leakage between adjacent transistors [BT84] (*cf.* Figure 3.4 a)). This technique is a layout approach that encloses the drain of a transistor by the gate and the source as illustrated in Figure 3.4 b). They are the best solution against TID, because they combine effectiveness and compatibility with commercial processes [MA97]. This technique has two main drawbacks. The first one is the difficulty in modeling an ELT. Indeed the W/L ratio is not straightforward and the gate and drain/source capacitances are larger than in the standard transistors. The second is the area overhead because of the enclosure. This area penalty factor is between 1.5 and 3.5 [ACD+99].

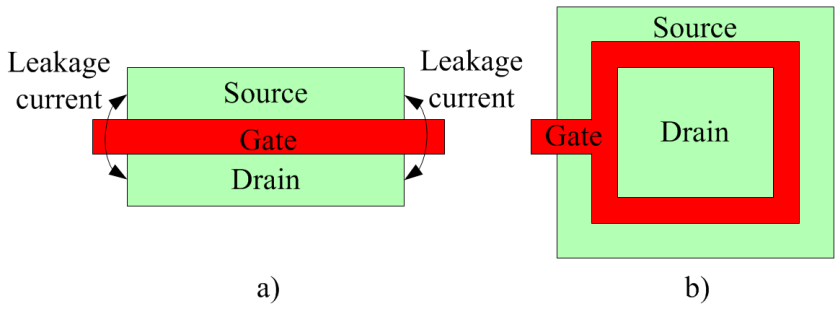


Figure 3.4: a) Standard CMOS structure, with leakage currents caused by TID, b) ELT structure.

3.2.5 Layout Guard Rings

Guard rings reduce the risk of SEL and intra-device leakage by providing electrical and spatial isolation [MA97]. As illustrated in Figure 3.5, each type of transistor can be surrounded by a protection ring: NMOS transistors by a P+ ring and PMOS transistors by a N+ one. The latch-up protection comes from the fact that the gain of the parasitic NPN transistor is significantly decreased by the P+ guard ring and

the gain of the PNP bipolar by the N+ guard ring. The price that has to be paid is of course an area overhead of around 8%[PSPL13]. The guard ring technique can be implemented along with the ELT technique to harden transistors against both SEL and TID [ACD+99] [MA97].

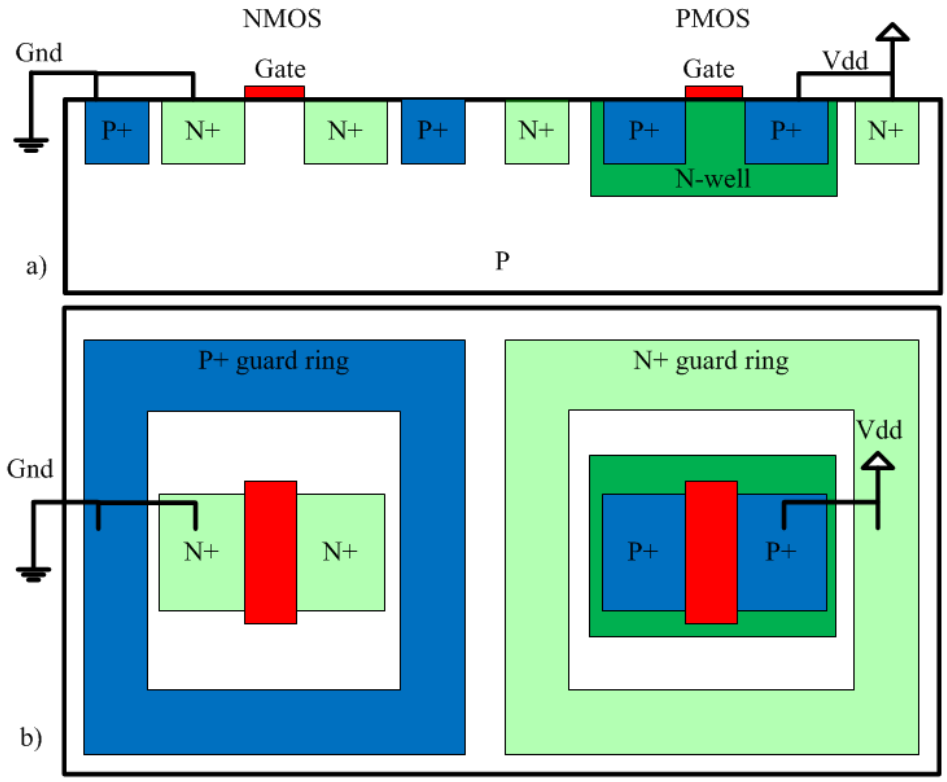


Figure 3.5: a) Cross section of an NMOS and a PMOS transistors with their respective guard ring, b) Top view of the NMOS and the PMOS with their guard ring.

3.2.6 Summary

Technological hardening techniques focus mainly on hardening against the radiation dose deterioration (*e.g.* TID), and against the effects of the parasitic BJT transistor in the CMOS technology (*e.g.* SEL). Techniques such as SOI, shielding and boron depletion from the BPSG passivation layers help reducing the possibility of interaction between ionized particles and silicon that can induce SETs. Nevertheless, a weight and an area overhead are expected from those techniques along with an important production price. According to Multi Project Circuits (CMP in french)

price list for 2014 the difference in price between bulk CMOS and SOI technologies can be up to 50%. CMP is a service organization in ICs and MEMS for prototyping circuits. However, it is expected that SOI catches up with the price of bulk CMOS for 28 nm and subsequent technologies [Jon12]. Radiation hardening by design is an interesting alternative to technological hardening because they can be applied in classical bulk CMOS technology without any technological additional cost. But it can also be use as a complement to technological hardening.

3.3 Radiation Hardening by Design techniques (RHBD)

Radiation hardening by design techniques focus on hardening against soft errors and are application dependent. (RHBD) techniques intervene at several levels of abstraction. They can be applied at a transistor or gate level with a gate hardening approach, or in a function or system level with redundancy techniques. This section will present the different hardening by design techniques.

3.3.1 Transistor sizing

On a transistor level, one of the simplest strategies for SET mitigation is the transistor sizing. The idea is to increase the capacitance so that the charge required to generate an SET has to be more significant, this is an increase of the critical charge [ZM04]. To this aim, the W/L parameters are adjusted to the desired values. As an example doubling W/L decreases the SET voltage amplitude by a half [ZM04]. It is important to avoid increasing L because the speed gained by scaling will be deteriorated by the resistive effect of a large gate. Nevertheless, increasing the capacitance of a sensitive node increases the response time adding propagation delay to the response. This technique was suitable for older technologies since the stored charge at a node was higher than some fC. But for recent technologies, where capacitance is between aF and fF, the capacitance to attenuate an SET has become prohibitively high. This high capacitance can increase the delay propagation of the gates affecting the frequency response of the gate by 3% [KAR$^+$09] [MZS$^+$06].

3.3.2 Transistor folding

The transistor folding technique is used to divide the sensitive node of a transistor into several nodes according to the number of parallel folded transistors [KAR$^+$09] (*cf.* Figure 3.6 a)). This folding creates replicas of the gate as shown in the example of an inverter in 3.6 a). This local redundancy helps to keep the logic state in case of one of the replicas is hit by ionization. On the layout a large transistor is divided in smaller ones, 4 in the example of Figure 3.6. Those smaller transistors are grouped

to share the drain, and the source. In this case two pairs of transistors share the drain, in this way the size of the drain is reduced by a half. Reducing the size of the drain reduces the change of being hit by ionization.

The main drawback of this technique is that if a big transistor is folded the smaller transistors have a smaller critical charge. In addition, in Chapter 2 was demonstrated that a parallel configuration of transistors reduces the critical charge. Thus if the folded transistors are too small the sensitive area can become greater than that of the initial large transistor [KAR+09]. This phenomenon can be observed with the NOR8 gate in Chapter 2 2.3.3. An extra hardening can be applied to this technique using transistor sizing. The increase of the transistor size will increase the critical charge of the output node.

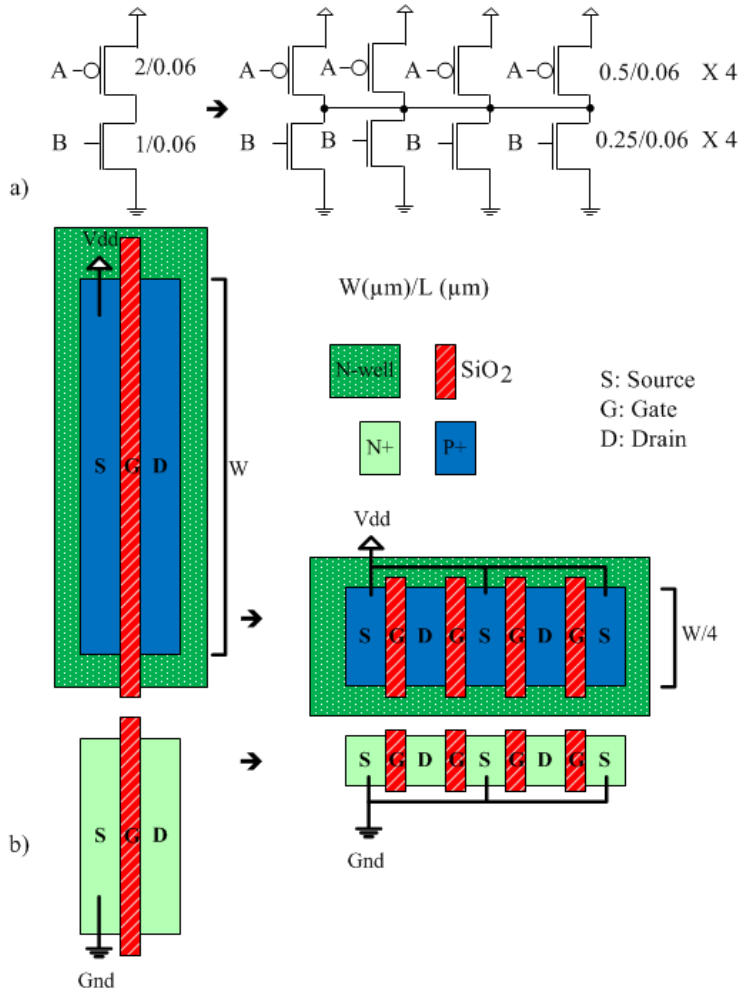


Figure 3.6: a) Electric scheme of a single inverter and its four time folded version, b) Simplified layout of a single inverter and its folded version.

3.3.3 HARDWARE REDUNDANCY

Hardware redundancy is one of the most common techniques and is known not only for its simplicity of implementation and its scalability but also for its area and power overhead. However there is just a small propagation delay overhead caused by that of the voter but it does not affect significantly the frequency response. Hardware redundancy generally means replicating a functional module (*e.g.* a gate, a function, a system) a number of times and providing a voting circuit that determines by majority vote the correct output, based on the replicated modules output [SSL11]. The reliability is increased with this technique because if one of the replicated modules fails the others will provide the right output and thanks to the voter the error will be logically masked.

A first technique is Error Correction using Duplication (ECD) [MZW+06]. As illustrated in Figure 3.7, the idea of this technique is to duplicate a combinatorial module, and let a decision gate decide the correct value of the output. The decision gate can be implemented by a Müller c-element. This gate acts as an inverter if the inputs are the same, and if the inputs are different the output remains the same. The drawbacks of this technique is of course that the size is doubled but also that the c-element is not hardened and if it is impacted by radiation an SET will propagate.

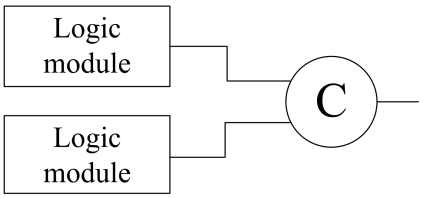


Figure 3.7: Error correction using duplication (ECD).

The most well known hardware redundancy technique is Triple Module Redundancy (TMR), shown in Figure 3.8 a). This technique has the inherent problem that is the lack of hardening of the voter and if a soft error occurs in this circuit the error will propagate. In order to mitigate this issue, the voter is also replicated and the module outputs are connected to all the voters as illustrated in Figure 3.8 b). This configuration is known as distributed voting [AS74]. Finally, another approach is Cascaded TMR (CTMR) where the outputs of TMR redundant modules are compared by a voter as depicted in Figure 3.8 c). Voting levels can be cascaded that way. However, the reliability of the final system does not necessarily increase with the cascading order number [SSL11]. Due to the area and delay propagation overheads associated with this technique, the replicated units in CRMR with a multi-layer voting scheme are normally functional units or logic blocks, not single gates.

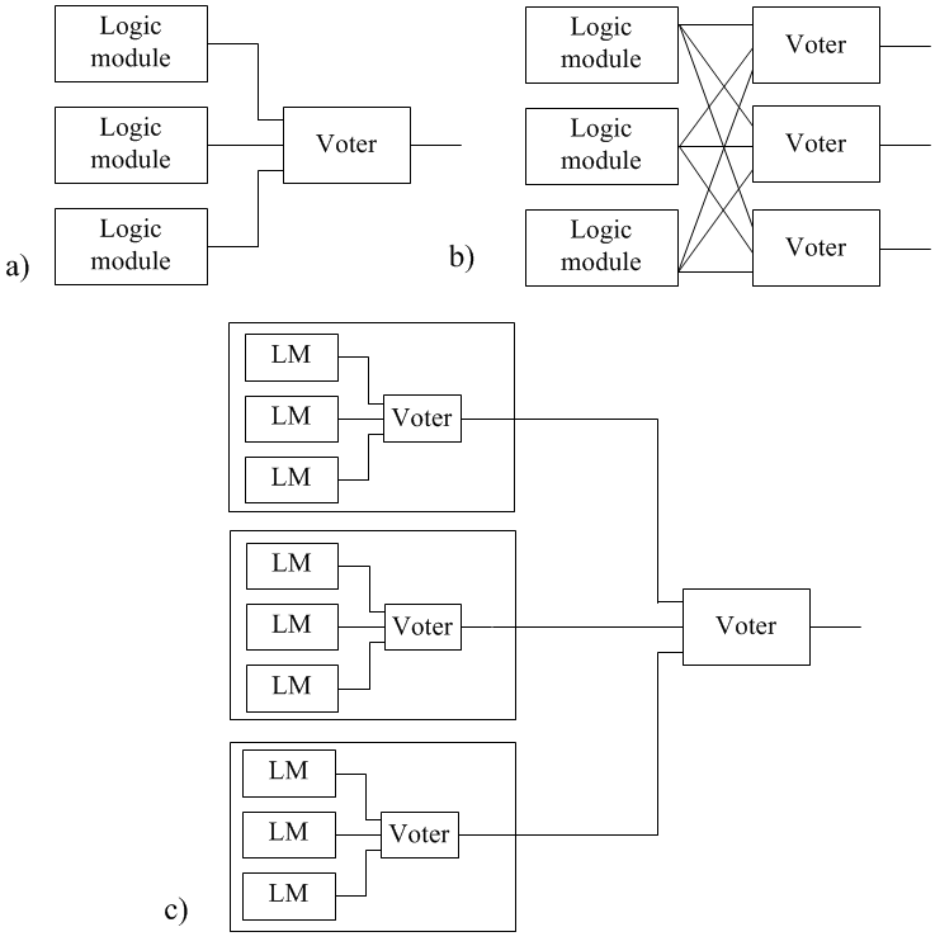


Figure 3.8: a) Triple Module Redundancy (TMR), b) TMR with distributed voting, c) Cascaded Module Redundancy (CMR).

In recent years, efforts are being made to reduce the area overhead of TMR focusing on a more local modular redundancy called logical masking. On a function level, this technique intends to avoid the propagation of SET through a combinatorial structure by hardening the most sensitive nodes. With this concept in mind, approximate logic circuits were proposed. They are circuits that perform a slightly different but closely related logic function, so that it can be used for error detection or error masking where it overlaps with the original circuit [SCEGVLO12]. An example of such technique is shown in Figure 3.9. This masking technique can be used for error detection and correction. An area overhead of between 50% and 70% have to be expected. The power of an approximated logic circuit is considered to be smaller or at least equal to that of the original circuit.

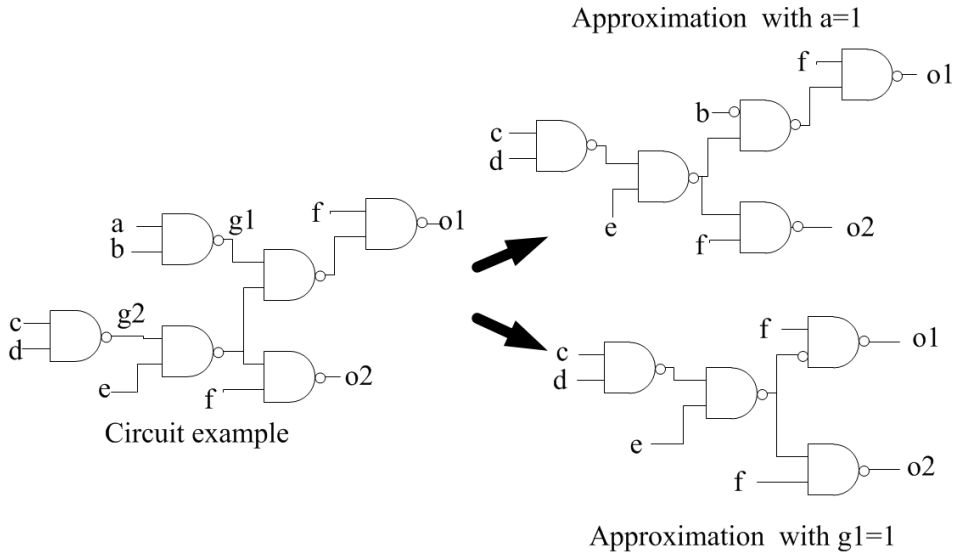


Figure 3.9: Approximate circuits obtained by the algorithm proposed in Sanchez *et al.* work[SCEGVLO12].

Probabilistic approaches are also being investigated. The idea is to use a mathematical model for estimating gate failure more accurately and evaluating reliability and fault tolerant designs. The work from Ban *et al.* [BWAN13] shows how to detect the less reliable components of a logic gate through a probability analysis. The probability of failure of a transistor is first determined, then that of a logic gate, and finally that of the whole combinatorial function. The proposed example uses locally TMR on those less reliable gates. This method proved to increase the reliability of the combinatorial function of 17%. The issue that remains is that even if an unreliable gate is hardened, nothing prevents SET from propagating from the other gates.

3.3.4 Information redundancy

The aim of this technique is to provide extra information used in applications related to error detection and error correction to increase the reliability. Information redundancy is widely used in memories to recover information corrupted by SEUs and in telecommunications for reliable data transmissions. There are also applications of this technique for combinatorial functions.

The most basic error detection technique is the parity bit. The obvious drawback is that an error correction is not possible, as there is no way to determine which particular bit is corrupted or even if there are several corrupted bits. An-

other error detection technique is the cyclic redundancy check (CRC). It is an easily implemented technique to obtain data reliability based on a hash function used to produce a checksum to validate the result. Redundant information is provided by the checksum about the block of data that helps the recipient detect errors. CRC is computed before and after transmission or memorization to confirm that the information is reliable. It is one of the most widely used techniques for error detection in data communications. It is usually associated with an Automatic Repeat reQuest (ARQ) protocol.

As far as the error correcting techniques are concerned error correcting codes are the main solution in communications and memories. An example of application is illustrated in Figure 3.10. A block of information x is encoded by the generator function G to encode the syndrome thanks to the information x. This syndrome contains redundant information of x. Both x and the syndrome G(x) are stored in a memory block. Assuming an SEU took place in the memory block, the information from x is distorted. Thanks to x and the syndrome, the validity of x can be checked. If errors are found and the code is powerful enough the original x block can be decoded. This allows detecting and correcting the bits of information that have been changed due to soft errors. It must be clarified that the number of errors that can be corrected depends on of the power of the code.

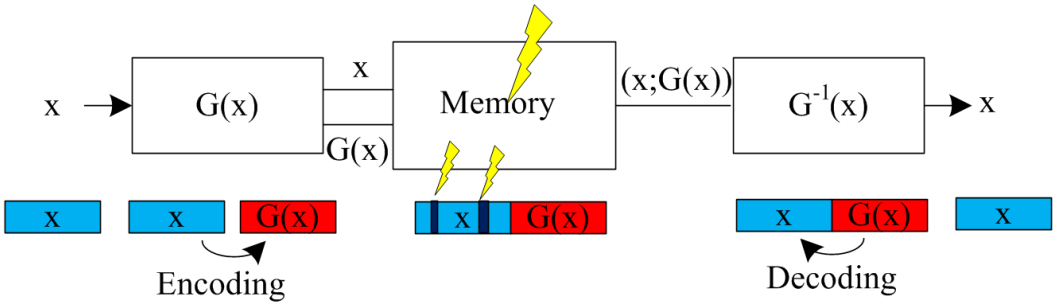


Figure 3.10: Error correcting codes in a memory application, with the encoding and decoding operations.

Some error correcting codes that are used for circuit reliability are: hamming codes [BAS05] and BCH codes [BPP+13] for RAM applications, LDPC codes [WH09], for on-line correction of functions results. Arithmetic AN codes are also used for on-line detection and correction [Muk08]. The issues with those error detecting/correcting techniques are the limited power of correction and the important area overhead associated with the implementation of the coding and decoding operations. The area overhead is related to the size and the type of the code as can be seen in the work of Adde *et al.* [AGTJ12]. In addition the coder and the decoder

can be hit by radiation and they are not self hardened.

On a gate level, there are architectural approaches of information redundancy based on keeping a redundant copy of data. This principle not only provides the correct data after a particle strikes but also helps the upset section recover from the SEU thanks to feedback. Two examples of such a technique for memory cells are the radiation-hardened latch with cross-coupled inverters[Roc88] and the Dual Interlocked storage CElls (DICE) [CNV96] (*cf.* Figure 3.11).

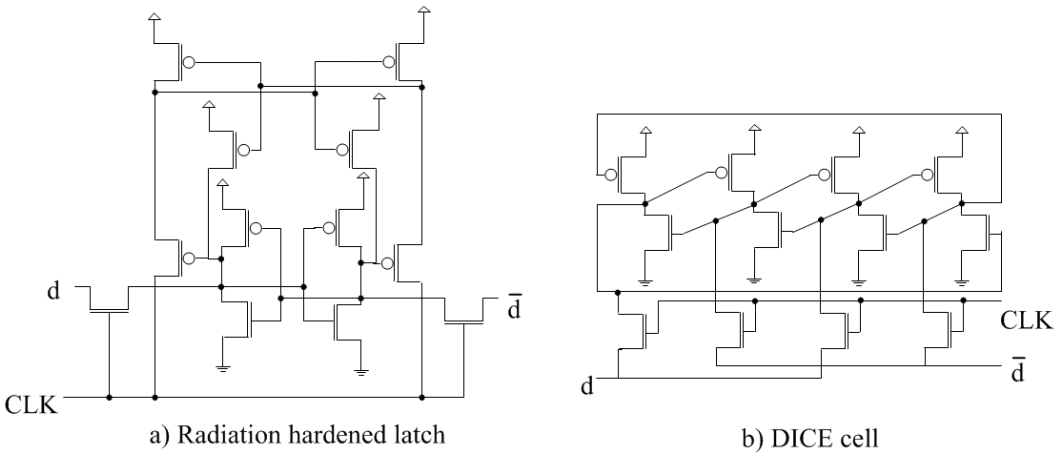


Figure 3.11: Hardened memory cells.

The latch cell hardening (Figure 3.11 a)) adds at most 40 % complexity and reduces the read and write time of the cell by 7 in relation to a hardening technique using resistors. But the read and write time can double in relation to the unhardened cell. DICE cells (Figure 3.11 b)) have a redundant copy of the output d and $\bar{d}$ in two different nodes. This keeps the logic state if one of the nodes is hit. One drawback of this technique is that the cell can increase the size of a typical CMOS RAM cell by 1.7 to 2 times [CNV96]. Another issue is that this cell can only handle an SET in one single node of the interlocked inverters. If two nodes are hit the state cannot be recovered.

3.3.5 Temporal redundancy

Time redundancy trades the area overhead, used in hardware redundancy, for time overhead. This time overhead is used in a gate level for delay buffers to create temporal filters, or in repeating the same computation in a system level. The idea of the first technique is to filter the SETs considering them as glitches. A filter is to be set between two functions, so the SET cannot propagate. For example between a combinatorial function and a flipflop as illustrated in Figure 3.12. The filter is

composed of several delay buffers (δ) and a voter. The output signal of the combinatorial function is divided into a direct signal and delayed ones. The signals are redundant, but thanks to the delays the voter decides the correct value of the signal stopping the SET propagation [SK12]. Finally, this technique does not require much area overhead compared to that of a complex system, but it ads latency in a pipeline structure because of the delays.

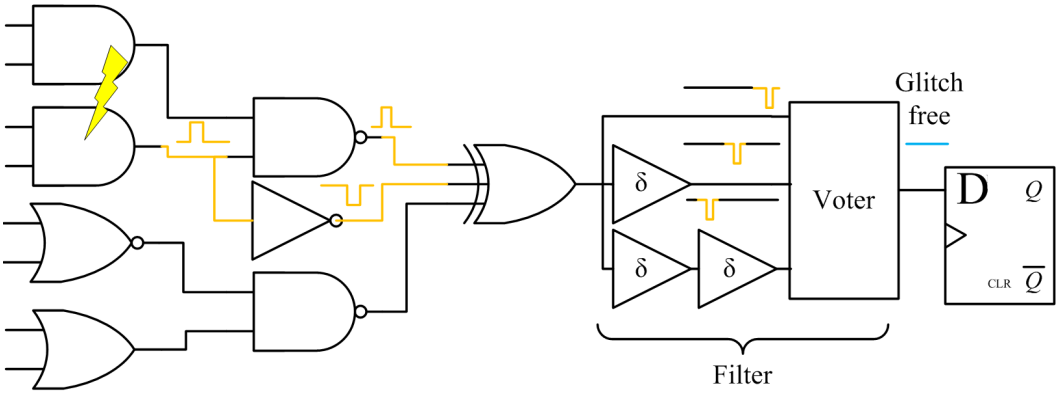


Figure 3.12: Temporal SET filter placed between a combinatorial function and a flipflop.

Computation repetition is a system level approach for temporal redundancy. In this case the idea is to realize a computation several times, and compare the results of the computation to then transmit the result obtained by a majority vote. If a computation is done three times, the most recurrent result will be considered as valid. Another approach is to use some kind of error detection technique (*e.g.* parity codes, AN codes, voters) to determine if a soft error occurred and order a re-execution of the computation. This technique is called the Automatic Repeat reQuest (ARQ) protocol as depicted in Figure 3.13 and an example can be found in Balaji et Rafay work [BR13].

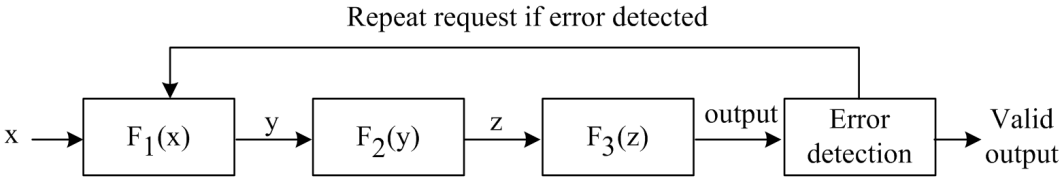


Figure 3.13: ARQ protocol principle.

Although ARQ avoids SET propagation, it can be very time consuming and power consuming. Even if the ARQ protocol could be more energy efficient than just the repetition of the computation with the voting process at the end, a whole re-

computation process has to take place. A final comment is that the error detection block for the ARQ system has to be self hardened otherwise there is a risk of SET propagation from there.

3.3.6 SUMMARY

Unlike technological hardening, hardening by design focuses only on hardening against soft errors and can be applied to conventional bulk CMOS technology avoiding the extra cost of technological hardening. If the additional cost can be paid, technological hardening and RHBD techniques can be applied in a same circuit. Hardening by design can be applied at different abstraction levels, from gates to whole systems. In the different strategies a trade-off between area, delay and power overhead has to be made. For strategies at a transistor level a size overhead is expected. For hardware redundancy an area and power overhead is expected with not much consequence in terms of propagation delay. For information redundancy, the encoding of information preserves the information from errors but requires some degree of complexity so that an area overhead is expected. The encoding takes time and consumes energy so a delay and power overhead are to be taken into account. Finally temporal redundancy trades area for time overhead. Even if less additional components are required a power overhead is expected due to re-computation process and delays.

3.4 STAKES OF RADIATION HARDENING BY DESIGN STRATEGIES

Radiation hardening is one of the challenges of integrated circuits. Because of the high cost of technological hardening, the RHBD techniques are an interesting alternative. Those techniques have to deal with trade-offs between area, propagation delay and power depending on the application. A comparative evaluation has been constructed in Table 3.1 to summarize the main characteristics of the RHBD techniques. This Table is based on the publications cited for each technique and the comparisons made in the works of Mitra et al. [MZS+06], Baze et al.[BKPS02], Velazco [Vel11], Lazarri [Laz07] and Katensmidt [KNCR04]. Based on the study made in Chapter 2, the hardening solution for the CLK Generator should satisfy several aspects. Ideally the hardening has to meet low power, low area and low time overheads. In addition to that, it would be interesting to apply the hardening without modifying the function so the hardening design process can be brief. Moreover, this hardening should be placed at the output of the function in order to stop the propagation of SETs. The final requirement is that that the hardening technique as to be the self-hardened, otherwise the hardening itself can be a source of soft errors. The question *who guards the guardians?* needs to be answered.

Haredening Category	Hardening Technique	Advantages	Drawbacks	Desing Considerations	SET/SEU Hardening Approach	Self-hardening
Gate level	**Transistor Sizing**	●Local hardening ●Small area overhead (less than ECD)	Limited hardening	●Locate the sensitive parts ●Optimal W/L	SET avoidance	no
	Transistor Folding	● Area reduction ●Can be used with transistor sizing	● Risc of critical decrease ●Limited hardening	Search for the optimal W/L	SET avoidance	no
Hardware Redundancy	**ECD**	Simple design, no delay impact	Duplicates power consumption and circuit area	Not particularly	Detection and Correction	no
	TMR	●Simple design ●No delay impact	Tripicates power and circuit area	Not particularly	Detection and Correction	no
	TMR with Distributed Voting	●Simple design ●No delay impact	Tripicates power and circuit area	Logic after the voters	Detection and Correction	yes
	Aproximated circuits	Less area and power overhead in relation to TMR and EDC	Determination of the approximated circuit	Most fitting approximated circuit	Detection and Correction	no
	Hardening based on Probability	Less area and power overhead in relation to TMR and EDC	Complexity of probability analysis.	Probability analysis	SET avoidance	no
Information Redundancy	**Error Detecting Codes**	On-line error detection	Unknown error Delay overhead caused by the logic	●Detection power ●Delay for the detection	Detection	no
	Error Correcting Codes	On-line error detection and correction	Coder and decoder complexity relative to the code lenght.	●Type of code ●Correction ●Delay of Coding/decoding	Detection and Correction	no
	Rad-hard Cross Inverters	Local redundancy, uses feedback to recover from an error	●No error detection. ●No correction if two transistors are ●Cell area x 1.4	Analog desing	Feedback correction	For 1 bit upset
	DICE	Local redundancy, uses feedback to recover from an error	● No error detection. ● No correction if two transistors are ●Area x 2	Analog design	Feedback correction	For 1 bit upset
Time Redundancy	**SET Filtering**	●Stops SET ●Very small area and power overhead. ●Easy to implement	Inherent delay (betwee some ps and ns)	Buffer delay time according to SET pulse width	●Detection and Correction ●Stops SET propagation	no
	ARQ	Data verification	If error detected, a whole process has to be repeated.	Atomatic request protocol	Detection and Correction	no

Table 3.1: Comparative table of the RHBD techniques.

One of the first remarks is that all the hardening by design techniques need a certain amount of area overhead. Gate hardening techniques have to be applied locally otherwise the whole size of the circuit increases. Without a doubt, hardware and information redundancy techniques have the most significant area overheads. Either by the replication of a circuit or by the arithmetic of the coding and decoding processes. Time redundancy techniques trade area for operating time and are very interesting for low area overhead especially the SET filters.

As far as the power consumption is concerned, hardware and information redundancy have the highest power consumption in relation of the size of the circuits. In this case gate level and time redundancy techniques have the advantage.

In terms of propagation delay, information redundancy is the most time consuming technique, specially error detecting/correcting codes. For example, in a pipeline structure, the number of clock pulses required to decode a message can be equal to the number of bits in the message. Time redundancy techniques either have to order a re-computation (only if an error is detected), or add a delay buffer of some nanoseconds at most. By increasing the size of the transistors gate level technique adds parasitic capacitances that can slow down the circuit, but this is not as dramatic as information redundancy techniques. Finally hardware redundancy has the advantage; the parallelism has no or little impact in the propagation delay.

Another parameter to take into account is the easiness of design of RHBD techniques. Time is money and the time spent in design generates cost for companies. Some techniques are very easy to apply to a circuit like transistor sizing, ECD, TMRs and SET filtering. Transistor sizing is quite easy to apply because only the size of the transistor has to be increased. But because of the small scale of this technique, increasing the size of all transistors in a circuit can generate a very important and unnecessary power consumption. To avoid this power overhead, sensitivity analysis have to be made requiring more design time. Hardware redundancy techniques like approximated circuits an hardening by probability require complex analysis. Other techniques like Error Detecting and Correcting codes require an extensive theoretical study to prove their effectiveness. For the time redundancy techniques, a system with ARQ needs a certain control system that adds complexity to the system. Unlike ARQ, an SET filter is a simple circuit that only requires a delay buffer design according to the intensity of SETs that is wanted to filter. Also an SET filter can be easily placed at the output of a combinatorial function.

As far as their action against SETs and SEUs is concerned, three hardening approaches lead the way: SET avoidance, SET/SEU detection/correction and the feedback correction. None of the SET avoidance technique are self hardened, so

there is still a risk of SETs. Of course the risk is less important than without any hardening but if an SET occurs nothing detects its occurrence. The SET/SEU detection and correction techniques generally hardened a circuit or a function, but they are not self hardened. Only TMR with distributed voting can be considered as self hardened. An interesting aspect is the feedback correction. Both techniques that use that principle (Rad-hard Cross inverters and DICE) are self-hardened for one bit upsets.

One technique seems to fulfill most of the criteria proposed at the beginning of this discussion. Indeed an SET filter is a small circuit, low power consuming, with SET detection and correction capabilities and can be placed after a sensitive function. The only limitations are the inherent delay that suggests a frequency restriction and the lack of self hardening. If the frequency restriction is considered as application-dependent, then an SET filter with self healing properties can be an interesting solution. The next section will detail the current SET filters that integrate the concept of feedback to harden the filter itself.

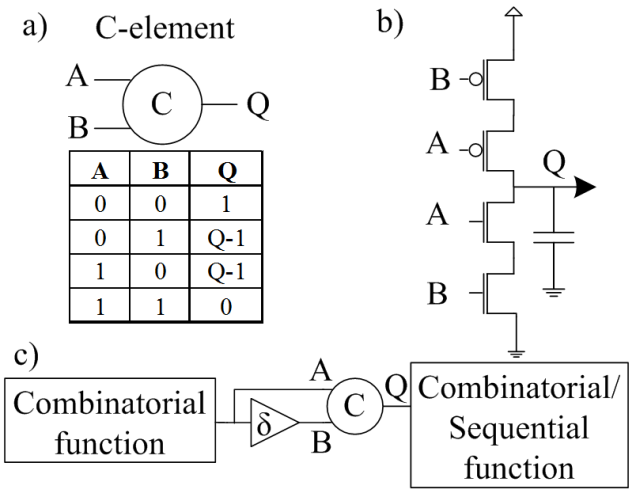
3.5 TEMPORAL FILTERING HARDENING AND FEEDBACK

As stated previously, the idea of temporal filtering (or SET filtering) is to stop the SETs coming from previous stages before they are latched, considering them as glitches. The filters are placed after a combinatorial function and before a memory element. A simple approach is to add a down-sized latch at the input of a sequential element to slow down the data transitions and as a result to filter out SET pulses that are faster than its propagation delay [HD11]. Another technique is to use the hysteresis property of the Schmitt trigger at the output of a combinatorial function. This makes harder for an SET to change the logic state because more charge is needed to make the change [SNI06]. In the previous Section 3.3.5 a filter with several delays was exposed. This section will expose a simplified version of that filter that requires only one delay and a voter. Then the hardening strategies for that kind of filters are going to be shown.

3.5.1 TEMPORAL FILTERING WITH C-ELEMENTS

A simplified alternative to filter shown in Section 3.3.5 is to build a low-pass filter [UTTS08] which can be achieved with a C-element preceded by one delay buffer at one of the inputs as illustrated in Figure 3.14 c). Then the C-element feeds a latch or even a parasitic capacitance as illustrated in Figure 3.14 b). The main advantage of using a C-element is that it is very simple to design. The C-element keeps the last output if the inputs are not the same, as a memory, or acts as an inverter when the inputs are equal. The C-element may be used as a filter between two functions as

shown in Figure 3.14. This SET filter can feed a hardened latch [GCG+13a][XLT13] so that combinatorial and sequential units are both radiation-hardened. If the logic requires, an inverter should be placed between the output of the combinatorial and the filter, in this way the inversion logic of the filter is compensated.



A	B	Q
0	0	1
0	1	Q-1
1	0	Q-1
1	1	0

Figure 3.14: a) C-element symbol and truth table, b) C-element structure, c) Temporal filter structure in a system.

If a glitch appears at the output of the combinational function and lasts less than the delay on input A, then inputs A and B will differ and the glitch will be filtered by the C-element. Designing the delay element requires knowing the expected SET pulse-widths that a circuit will encounter. As reported in [NBS+07], there has been no consensus on the expected SET pulse-widths for recent technology nodes. In [NBS+07] the authors also mention that values of SET pulse-widths can reach values as large as a few ns and depend not only on the Linear Energy Transfer (LET) of the striking ions but also on the considered technology (130nm vs. 90nm, for instance). Moreover, SET pulse-widths depend also on the circuit temperature as shown in [GAB+10]. Therefore, a maximal SET pulse-width has to be considered depending on the operating conditions and the targeted robustness to design an appropriate delay element.

The main advantage of this filtering technique is that the propagation of an SET glitch, with a pulse-width shorter than the designed delay, is stopped and the right value propagates after the filter. This enables the reliability problem to be solved by the filter and not in the possibly complex combinatorial function preceding the filter. The reliability issue is then set only on the filter, reducing considerably the area that is wanted to harden. The probability of an impact, taking into account the surface, is smaller in a small filter than in a larger and more complex combina-

torial function. The drawbacks are that these techniques require a delay to operate and they have no self healing properties if the filter is hit.

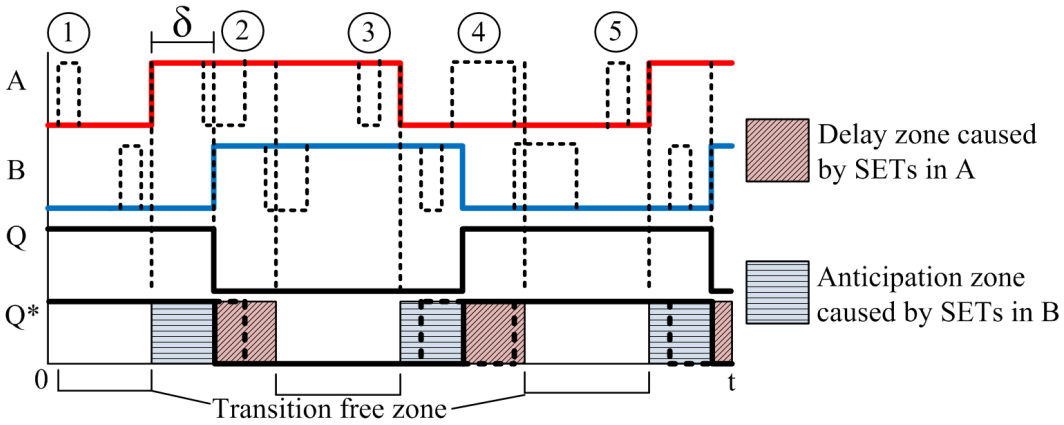


Figure 3.15: Filters behavior depending of the moment of occurrence of SETs. A and B are the inputs, Q is the ideal output, Q* is the real output with the delays or anticipation zones.

When the time delay (δ) is fixed it is important to keep in mind that depending on the moment when an SET enters the filter the output Q will react differently, anticipating or delaying the Q signal but filtering the glitch. Figure 3.15 shows input signals A and B disturbed by SETs (in dotted line). The output Q show the control response without SETs and the signal Q^* is representing the output Q signal with the effects of the numerated events with a dotted line. Depending on the moment when an SET occurs the output of the function can anticipate or delay the logic state. For example SET number 1 has no effect but SETs 2 and 4 cause a delay because the logic of the C-element states that when the inputs are different the output must be maintained. SETs 3 and 5 cause an anticipation of the change of logic state because the delayed SET in input B has the same logic state as input A. The delay and anticipation zones have a maximum time width of the delay δ. Passing that time the output is transition free. This phenomenon must be taken into account for the frequency of operation of the system so the transition free zones are more important.

The C-element based filter has been explained, but the issue of its own reliability is still at stake so the hardening strategies used in the literature for hardening C-elements are going to be explained next.

3.5.2 State of the art for SET filter Hardening

In the case of a C-element, the vulnerability comes from the low critical charge at the output node and the memorization state when both inputs are different. If the

C-element is hit during the memorization state the information is corrupted and an SET will propagate. That is why to reduce the vulnerability the memory mode has to be shorter than the inverter mode. The reliability issue on the filter has been the object of several designs in bulk CMOS technology.

The C-element is a small and simple gate and those hardening strategies can be easily applied to it. The design solutions are illustrated in Figure 3.16. The only one that is not shown in the figure is the sizing technique because the structure remains the same, only the size of the transistors is increased in order to increase the output capacitance and by that increase the critical charge at the output or the gate. The critical charge of the output can be increased with a simple folding of the C-element as shown in Figure 3.16 a). Otherwise, the C-element can be hardened thanks to additional cells. As proposed in [Mar90], a C-element can be followed by a well-designed latch (Figure 3.16 b)) so that the output of the C-element benefits from the latch stability to erase short glitches. A C-element can also be designed with Schmitt trigger capabilities by using a CMOS Schmitt trigger [KS92] but changing the connection of the inputs, as shown in Figure 3.16 c). This allows the gate to have a high threshold voltage for a transition from "0" to "1" and a low one for transitions from "1" to "0". In Figure 3.16 d), a C-element is strengthened thanks to the technique provided by [CAR13]. This technique combines function duplication with feedback, to activate a copy of the C-element gate, when an undesired state change occurs. This technique can also benefit from an additional Schmitt trigger as described in Figure 3.16 e). A DICE [CNV96] can also be used to strengthen the C-element output as shown in Figure 3.16 f). This technique uses the principle of the latch but with a hardened one. This hardened latch have copies of the state in the nodes of their cross-coupled inverters that can reestablish the correct value if one of the nodes is hit. This solution was compared to other ones in [VXVZ06] and selected as the best one to mitigate SETs. Finally, the Schmitt trigger (ST) circuit proposed in [SNI06] and illustrated in Figure 3.16 g) is also a filtering solution which has to be considered of interest. Even though is not C-element based it is considered as a temporal filtering solution. This gate uses a pass-gate to attenuate the voltage magnitude of incoming SETs by a resistive effect, and then the inverter and the latch serve as Schmitt trigger to add the hysteresis effect. This effect is obtained by changing the size of the transistors from the inverter after the pass-gate and the feedback inverter. The transistor sizes for each filter can be found in Appendix E.

As integration technology shrinks, the critical charges of the nodes become smaller. Solutions that rely exclusively on the increase of critical charge are still unreliable because if an SET manages to take place there is no other mechanism preventing the SET to propagate. This is the case of the folding (Cx3), the strengthening (C+Str), and Schmitt trigger techniques (C+ST, C+ST+Str, ST). The tech-

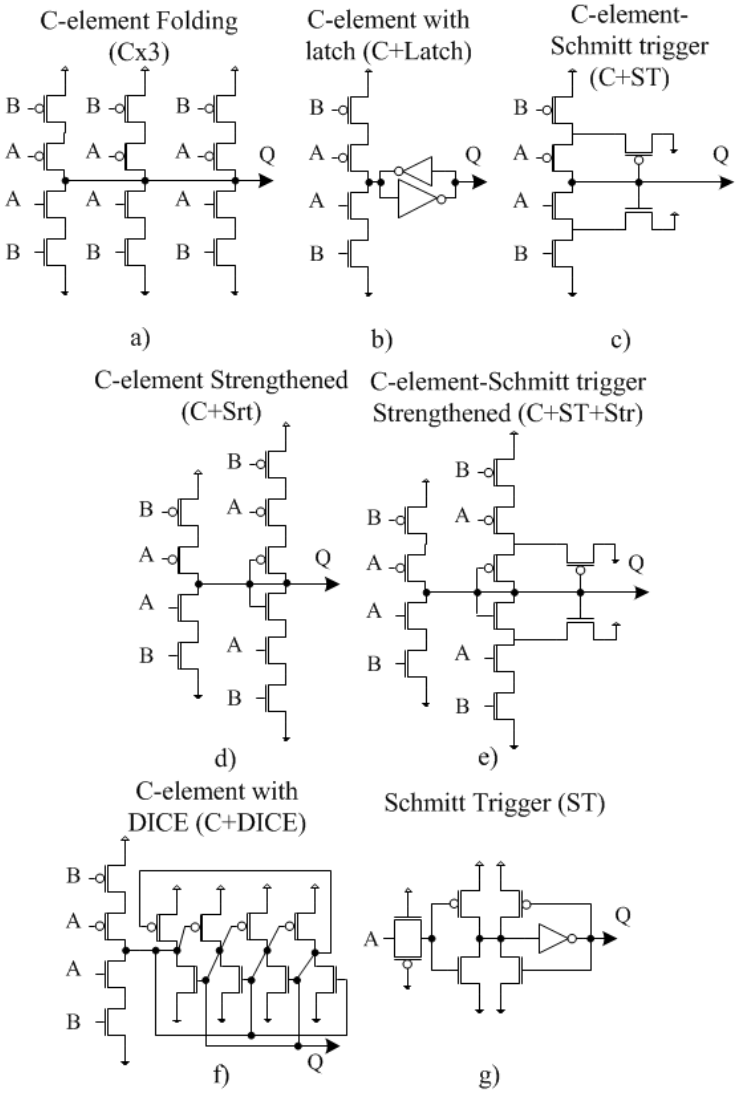


Figure 3.16: a) C-element hardened by folding technique [KAR+09] (C x 3); b) C-element with latch (C+latch) [Mar90]; c) C-element based on a CMOS Schmitt trigger[KS92]; d) C-element hardened by strengthening technique [CAR13] (C+Str); e) C-element as a Schmitt trigger hardened by strengthening technique [CAR13] (C+ST+Str); f) C-element hardened by a DICE cell [CNV96] (C+DICE); g) Schmitt trigger (ST) [SNI06].

niques using a latch (C+Latch, C+DICE) prevent SETs from the C-element to propagate; nevertheless an SET that takes place on the latch will propagate. In the case of a DICE latch a single SET might not affect the circuit but. Because of the size of the technology and the trends not only SETs affect integrated circuits but one single ionizing strike can generate multiple bits upsets (MBUs). If the DICE

is disturbed by MBUs, unfortunately the feedback action will not be enough, because the copies of the state will also be corrupted. Indeed those techniques reduce the reliability issue even more but they still have weaknesses, and the question *who guards the guardians?* is still open. Chapter 4 will expose a strategy that wants to overcome those weaknesses.

3.6 Conclusions

This chapter presented a state of the art of radiation hardening techniques. Technological hardening techniques focus on avoiding radiation effects by modifying the fabrication process and using the physical properties of materials to harden the integrated circuits. Radiation hardening by design is an interesting alternative to technological hardening because they can be applied in classical bulk CMOS technology without any technological additional cost. RHBD techniques can be applied at different abstraction levels, from gates to whole systems. In the different strategies a trade-off between area, delay and power overhead is made.

This state of the art brought a discussion over the stakes for a hardening by design technique. Focusing on a low cost solution, it was pointed out that there is a need to harden the hardening. An ideal radiation hardening by design technique should incorporate low area, low power and low delay overhead. Also that solution has to be independent from the function that is wanted to harden to avoid that an SET affecting the function affects also the hardening. A final consideration is that the hardening technique had to have self-healing properties to counter SET occurring at its output.

For those criteria the temporal filtering is promising, on the condition that a delay is used and if it could be hardened. Several hardening strategies were presented for temporal filters based on C-elements, but the question *who guards the guardians?* is still open.

Chapter 4

The C-element with Detection and Correction (CDC) approach

The previous chapter explored the different hardening solutions and discussed the necessity to answer the question *who guards the guardians?* To avoid the additional cost of technological hardening, hardening by design seems to be an interesting alternative, especially the temporal hardening. This technique aims at gathering aspects such as low area overhead, low power overhead, with a reasonable delay overhead and easy placement on the circuit. The SET filters exposed in Chapter 3 Section 3.5.2 showed weaknesses, even if they are able to block SETs. The problem is that they are not completely self hardened and if they fail there is no indication of the error. In order to propose a solution three aspects are considered. The first one is to block the propagation of SETs. The second is to improve the self hardening to avoid the SET propagation. The last aspect is to consider the case that the filter can fail. Those aspects can be covered by a detection and correction architecture on an SET filter. The filter alone stops SETs, a detection mechanism indicates that an SET took place, and using a feedback signal, from the detection, a correction can be done. A bulk CMOS solution that combines detection and correction of SETs is going to be presented. The properties of this solution will be explained at first, then an electrical characterization of those properties will be done. Finally a comparison of that solution with other state of the art SET filters will be made.

4.1 CDC Properties

Inspired by the temporal filtering (or SET filtering) and the feedback action of some hardening techniques like those presented in Chapter 3 Section 3.5 Figure 3.16, a C-element based filter is going to be presented. The main idea is to detect the parasitic current using Built-In Current Sensors (BICS), and to effectuate a feedback compensation to counter an SET. The approach, called CDC for C-element with Detection and Correction, has three properties that are going to be explained. The first is the SET detection, the second is the feedback correction and the last one is

the possibility of encoding information.

4.1.1 SET DETECTION WITH BICS

The SET detection principle is based on how ionizing radiation affects silicon. In Chapter 1 Section 1.1.4 was exposed that a parasitic current between the bulk and the drain was generated from an ion strike. Based on that current flow the SET detection is achieved by bulk built-in current sensors (BICS) [NRV+06]. Dedicated BICS have to be implemented for each type of well, an NBICS and a PBICS are required. Figure 4.1 shows how the BICS are connected to a C-element. The PBICS and NBICS detect the ionization current in the bulk by sensing the current through M_5 and M_9, respectively. Those transistors are always active and serve as sensing resistors to use the voltage difference to activate transistors M_6 and M_{10}. Small amplifiers made by M_6 and M_7 for the PBICS and M_{10} and M_{11} for the NBICS, amplify the sensing voltage to indicate that a logical change of state took place. The PBICS detects output transitions from 0 to 1 and the NBICS detects transitions from 1 to 0.

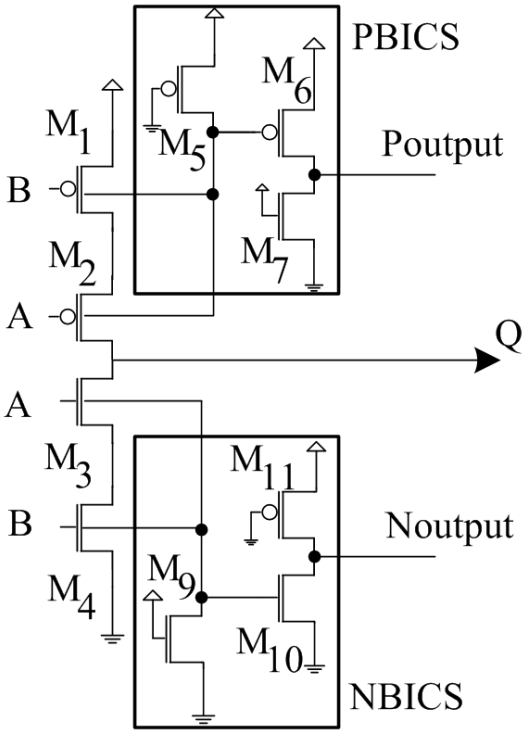


Figure 4.1: C-element with an SET detection using BICS.

4.1.2 CORRECTION WITH FEEDBACK

The output signal from the BICS can be used not only as detection, but also as a feedback signal to activate a compensation mechanism. The correction part compensates the SET's voltage glitch by using the detection signal from the sensor to activate the feedback transistors M_8 or M_{12} so that the right state is recovered. The idea is to have a quick response so a transition can be compensated before the next circuit, after the filter, has the time to acknowledge the transient change of state. If an undesired transition to 1 occurs then M_8 will be activated. On the contrary if a transition to 0 takes place M_{12} is turned on. The fact that BICS and feedback transistors are only active when an SET occurs avoids a dynamic power overhead. This is why the architecture is called C-element with Detection and Correction (CDC). Supposing an SET in the NBICS is detected when the output Q is "0", this means only that the value "0" is maintained. The feedback transistors have to be well sized so that the state does not change when the feedback indicates that an SET took place. The same situation can happen with the PBICS when the output Q is "1".

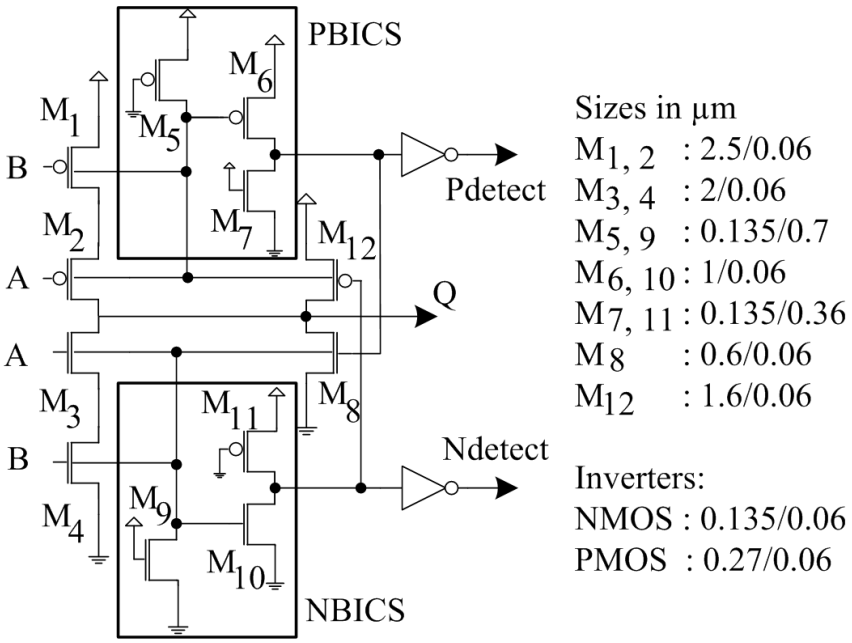


Figure 4.2: C-element with an SET detection and correction (CDC) feedback control system.

Supposing the compensation is not enough and the glitch cannot be compensated in time, at least there is an indication that an error has occurred with the

output of the BICS. Inverters can be placed after those outputs to deal with the fan-out. Additionally, this ensures that the switching of the feedback signal is done as quickly as possible because there is no additional charge. Thus the BICS are design based on the size of the feedback transistors, the inverters and the BICS output. Finally, the detection signals are *Pdetect* and *Ndetect* as shown in Figure 4.2. The feedback signal feeding M_8's gate can be considered as $\overline{Pdetect}$ and the signal feeding M_{12}'s gate can be considered as $\overline{Ndetect}$. The symbol for the CDC is depicted in Figure 4.3 and will be used in the rest of this work.

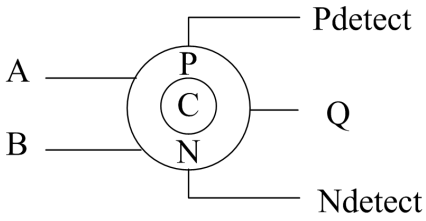


Figure 4.3: CDC symbol.

Design considerations must be taken into account to ensure the normal functioning of the CDC:

1. For an easy placement and avoid further logic concerns an inverter should be placed upstream to feed the direct input of the CDC and the delay buffer, because the CDC alone acts as an inverter.

2. All the transistors should be designed for low power applications, to minimize the power overhead.

3. M_1, M_2, M_3 and M_4 must have a large W/L ratio to benefit from transistor sizing and increase the critical charge of the output node.

4. M_5 and M_9 should have a small W/L ratio ($M_{5,9}(W/L) = 0.135/0.7$) because the resistance of the channel will be used as current sensor.

5. M_6 and M_{10} must have a large W/L ratio ($M_{6,10}(W/L) = 1/0.06$) to act as a voltage amplifier to detect as soon as possible a change of voltage at the bulk. In order to switch even faster, those transistors can have a low voltage threshold (LVT).

6. M_7 and M_{11} must have a small W/L ratio ($M_{7,11}(W/L) = 0.135/0.36$) to enable a quick change of state at their drains. This helps with the action of M_6 and M_{10}.

7. M_8 and M_{12} must have a large W/L ratio and depend on the size of M_1, M_2, M_3, M_4 to avoid false errors when the feedback is activated ($M_8(W/L) = 0.6/0.06$, $M_{12}(W/L) = 1.6/0.06$).

8. Output inverters for *Ndetect* and *Pdetect* signals help with the fanout ($PMOS(W/L) = 0.27/0.06$, $NMOS(W/L) = 0.135/0.06$) and isolate the feedback signal from other subsequent circuits.

4.1.3 Encoding and Decoding capabilities

One last aspect of this hardening strategy is that the output information can be encoded by 3 bits in real time. During the normal operation, signal *Output* changes from 0 to 1 or vice-versa, but *Pdetect* is 1 and *Ndetect* is 0. If the PBICS detects an SET, *Pdetect* becomes 0 during this event. If an SET is detected by the NBICS, *Ndetect* becomes 1 during this event. Every change of state will be considered as an error. Table 4.1 shows that other states than *Normal* are unreliable, and the correct output value is decoded as the previous one *Q-1*. This information is useful when the feedback system is not able te compensate in time a transition caused by a very energetic strike or in case of one hit affecting various transistors at the same time. The decoder logic is implemented by the circuit on Figure 4.4. This circuit is based on a C-element with the logic from Table 4.1. The $\overline{Ndetect}$ and $\overline{Pdetect}$ signals can be obtained from the signal to the feedback transistors, so no other logic gates are needed. This decoding logic could be placed at the input of a hardened latch or Flip-flop cells. It can be applied to C-element-based hardened flipflops such as those from Devarapalli *et al* [DZHS10], Glorieux *et al* [GCG+13b] and Gang *et al* [CGG13].

Output	**Pdetect**	**Ndetect**	**Description**	**DecOutput**
0	0	0	PBICS hit	Q-1
0	0	1	PBICS and NBICS hit	Q-1
0	1	0	Normal	0
0	1	1	Transition to 0	Q-1
1	0	0	Transition to 1	Q-1
1	0	1	PBICS and NBICS hit	Q-1
1	1	0	Normal	1
1	1	1	NBICS hit	Q-1

Table 4.1: Description of the output code states and decoding

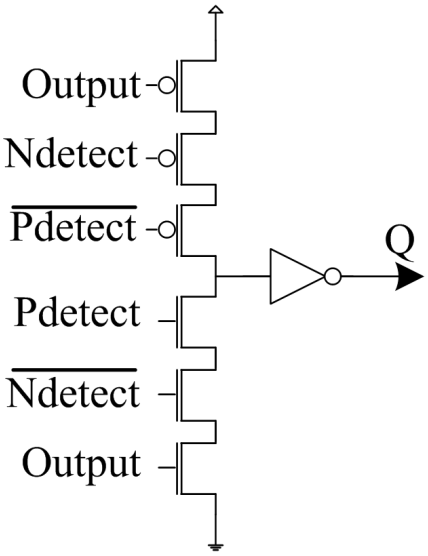


Figure 4.4: Decoder logic based on Table 4.1.

4.2 CDC CHARACTERIZATION

The CDC solution makes a trade-off between time, for the filter's delay buffer, and low area and power overhead. In addition the CDC architecture enables SET detection and correction on the C-element so the filter itself is hardened. Those characteristics have limits, which will be discussed in this section. To give the characteristics of the CDC solution, electrical simulations are done using the CADENCE kit for 65 nm CMOS Technology to study the behavior of the CDC. In the first place, the study will focus on the CDC properties of filtering, then the self-healing and finally the encoding. The validation of the CDC will be exemplified using the SAR ADC and different test benches that will be specified for each property. The CDC will provide the hardening for the CLK generator. The set up for the validation simulations uses the 65 nm version of the SAR ADC placing the CDC between the CLK generator function that creates the Internal CLK signal and the comparator as shown in Figure 4.5. An inverter upstream the filter is omitted because the logic of the comparator compensates the inversion of the filter. It is important that when the CDC is tested in the SAR ADC the operating sample frequency of 10 MHz is respected.

4.2.1 FILTERING

The first property of the CDC is the filtering. To demonstrate the filtering capabilities the simple set up shown in Figure 4.6 is used. A pulse generator will provide the

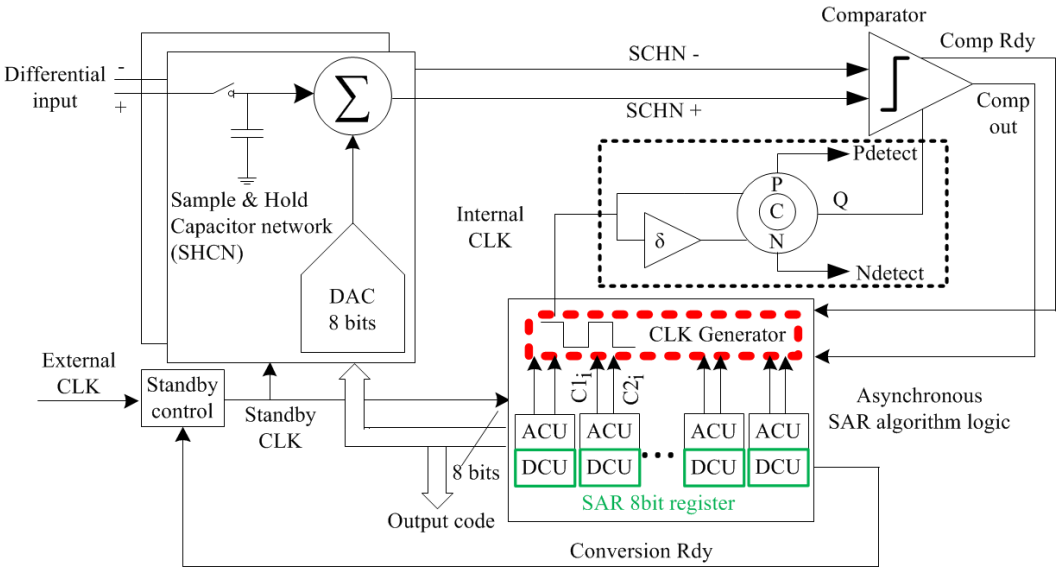


Figure 4.5: SAR ADC with the CDC temporal filter after the CLK generator function.

SET pulses with variable width. Here the pulses are defined as step signals from 0 to 1.2 volts. Low power CMOS transistors are used because of the low power requirement of the SAR ADC. For such transistors, 1.2 volts is the required supply voltage in 65 nm technology for the ST Microelectronics kit. The CDC with the delay buffer will filter those pulses and the Q output will reflect the filtering process by charging or discharging the capacitor C. The capacitance is 0.33fC, this corresponds to the minimal capacitance of the smallest capacitor (metal plates) in the CMOS 65 nm technology kit. This scenario guarantees the lowest output charge for the CDC and can show the slightest variation of the output state.

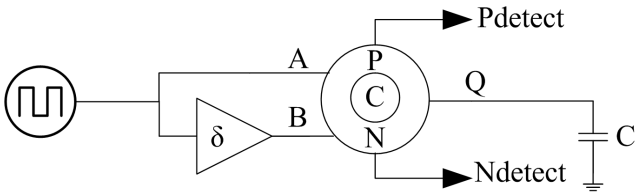


Figure 4.6: Test bench for the filtering simulation.

As reported in [NBS+07], there has been no consensus on the expected SET pulse-widths for recent technology nodes. In [NBS+07] the authors also mention that values of SET pulse-widths can reach values as large as a few ns and depend not only on the Linear Energy Transfer (LET) of the striking ions but also on the considered technology (130nm vs. 90nm, for instance). Moreover, SET pulse-widths depend also on the circuit temperature as shown in [GAB+10]. Therefore, a max-

imal SET pulse-width has to be considered depending on the operating conditions and the targeted robustness to design an appropriate delay element. The delay time δ is fixed at 0.9 ns to be in the order of magnitude of powerful SET pulse widths.

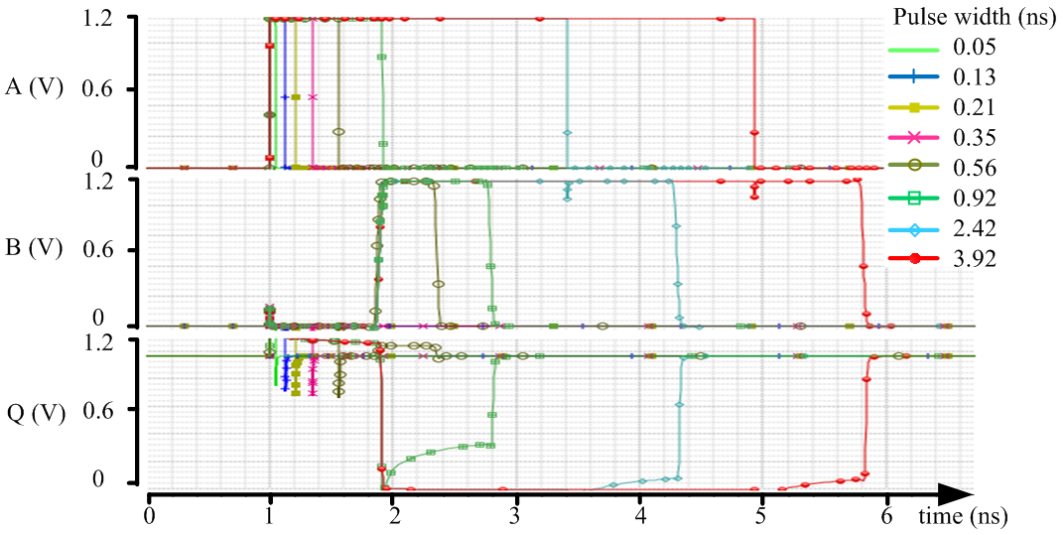


Figure 4.7: Commutation to "0" of the ouput Q of the temporal filter CDC depending on the width of the pulse at the input.

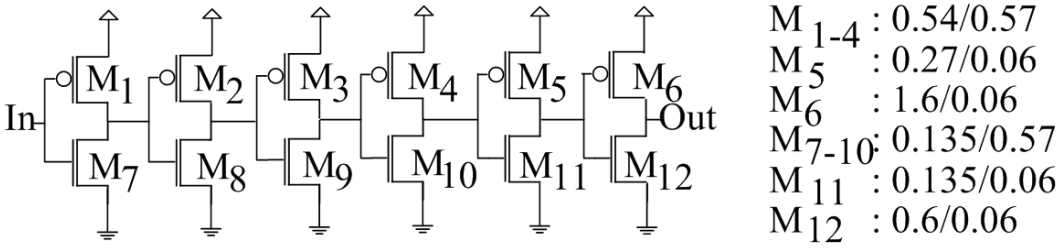


Figure 4.8: Buffer delay. The transistor sizes of W/L are in μm.

Figure 4.7 shows different pulses with different pulse widths and their effects on the filter. The pulses whose width is above the delay time $\delta = 0.9$ ns are the only ones that can make the filter switch the logic state at the output Q. Another effect less clear is the electrical masking of the buffer. The signal B, the output of the buffer, does not show the pulses whose width is below 0.56 ns. The buffer is made by a succession of 6 inverters as depicted in Figure 4.8. The delay buffer was constructed to reach the 0.9 ns delay without having to enlarge the gate length, which adds resistive effects. In addition the output transistors of this buffer are larger to preserve the shape of the input pulse. This succession of inverters attenuates a very rapid glitch because all the six inverters cannot switch as quickly as the glitch.

Figure 4.9 shows the pulse width from which the buffer switches. This threshold width is 0.85 ns.

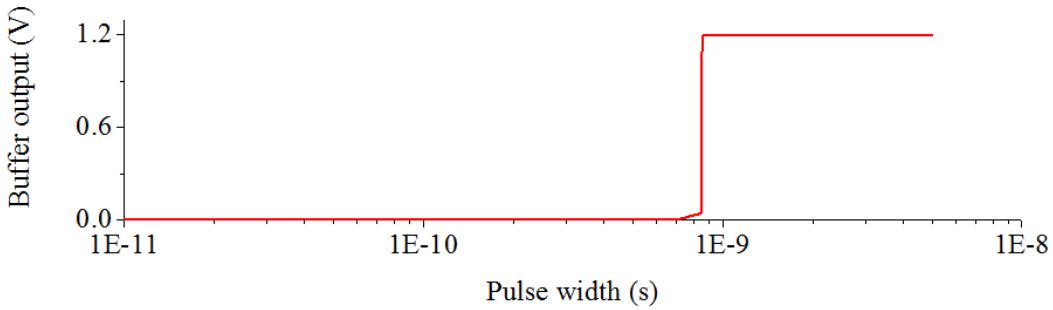


Figure 4.9: Buffer output magnitude relative to the pulse width at the input of the filter for a 1.2 V magnitude pulse.

A similar figure can be shown for the CDC. Since it works as an inverter Figure 4.10 shows the switching to "0" when the threshold of the delay is reached. A complementary figure can be drawn for the transition to "1" and the threshold will be the same. The filter can be adjusted to filter glitches by just changing the propagation delay of the buffer.

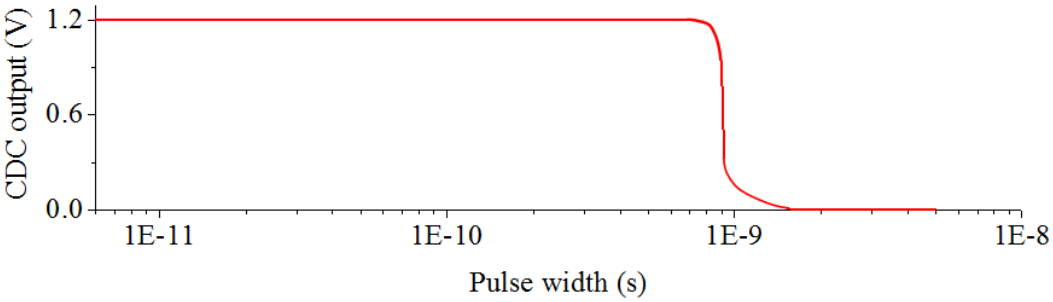


Figure 4.10: CDC output magnitude relative to the pulse width at the input of the filter for a 1.2 V magnitude pulse.

To see the filtering effect on the SAR ADC, the CDC filter is placed between the CLK generator and the comparator as illustrated in Figure 4.11. SETs coming from the CLK generator are simulated using current sources that inject the parasitic modeled current.

Figure 4.12 shows the filter in action. Two cases are depicted, the first one uses pulses whose width is under the delay value of the buffer (0.9 ns) and the second case uses SET pulses whose widths are larger than the delay. In the first case the pulse width is 0.3 ns and in the second case 1 ns. The represented signals are *Internal*

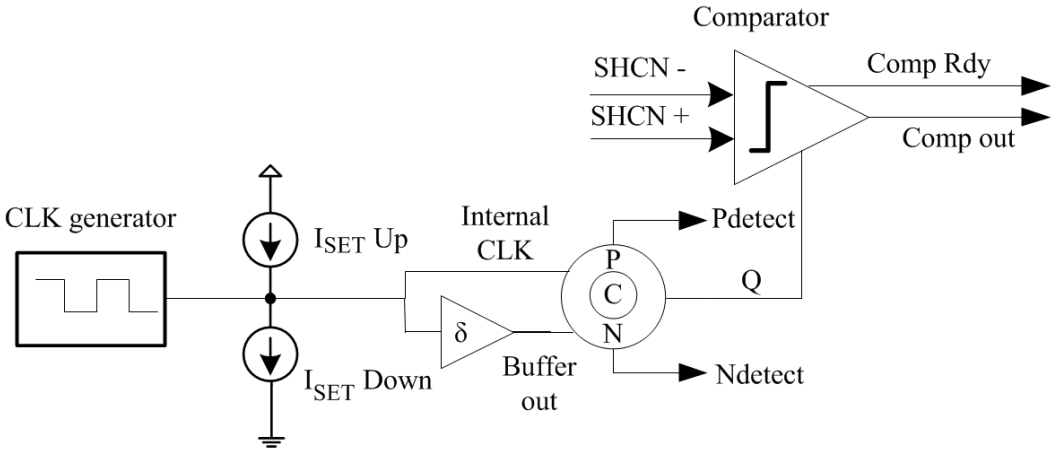


Figure 4.11: Test bench to simulate the filtering capabilities of the solution.

CLK, *Buffer out*, *Q*.

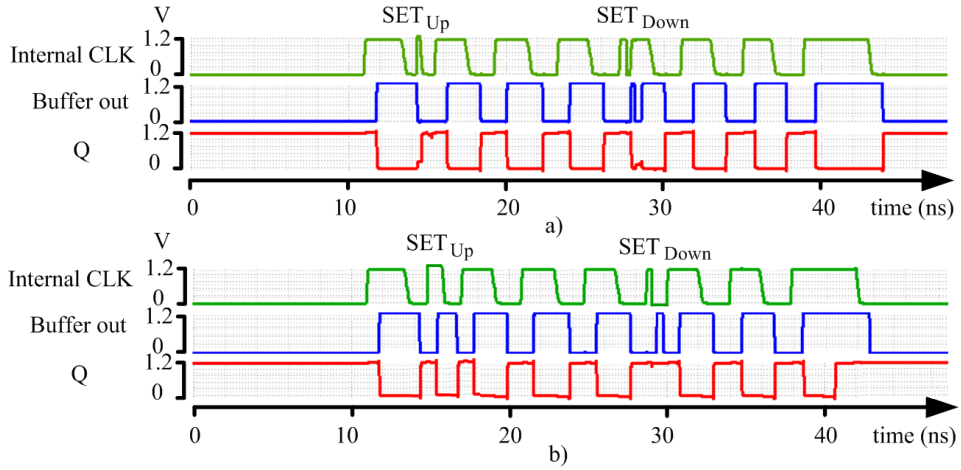


Figure 4.12: a) Filtering SETs with pulse width of 0.3 ns b) filtering SETs with pulse of 1 ns.

In Figure 4.12 a), the SET pulses have a small width (0.3 ns) and by the action of the delay buffer the glitch is filtered, so the output signal is unchanged. In Figure 4.12 b), the pulses have a width of 1 ns which is larger than δ. Since the pulse lasts longer than the 0.9 ns delay of the buffer, the SET_{up} pulse of *Internal CLK* and the pulse transmitted through the buffer make the inputs of the C-element coincide. Two outcomes can take place. The first is that the state can change suddenly, like Q when SET_{up} takes place. The other is that the logic state is kept longer than normal

like when SET_{down} takes place. The anticipation and the delay of a logic state can cause errors of logic in asynchronous and synchronous circuits as well. So the longer the delay of the buffer the better, but this has a propagation delay cost so a trade-off can be done. The higher energy strikes the rarer they are. Thus, depending if the environment has a high or a low radiation flux, a large or a short delay can be chosen.

With this simulation, has to be noted that the use of the delay buffer does not affect the frequency response of the SAR ADC because the conversion cycle with the buffer lasts around 40ns, and the ADC cycle is 100ns. The 10MHz of sampling rate can still be fulfilled.

4.2.2 SELF-HEALING

In order to show the self healing properties of the CDC, the same test bench as illustrated in Figure 4.11 is used, but in this case the current sources simulating SETs taking place on the filter will be placed at the output Q as depicted in Figure 4.13. To demonstrate the self-hardening effect the CDC is compared to another CDC whose feedback transistor gates are disconnected from the feedback signal. The gate of the PMOS feedback transistor is connected to the Vdd source and the the gate of the NMOS one is connected to the ground. This keeps the same load at the output of the CDCs so the comparison is made with the same output charge.

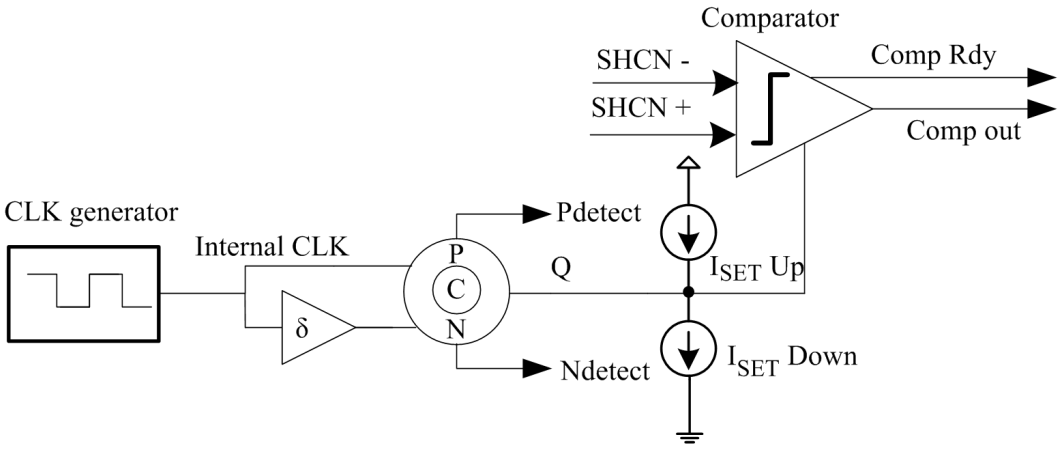


Figure 4.13: Test bench to simulate the self-healing properties of the CDC.

Figure 4.14 shows the simulation of the CDC with and without feedback connection. *Q Control* signal is the output of the CDC without SETs. I_{SET} is the magnitude of the current of the SETs. In this figure the maximum current pulses depending on the functioning mode for CDC are illustrated. In inverting mode the peak can reach 1 mA (a critical charge (CC) of 95.5 fC)), but in the memory mode the peak can only reach 324 μA (a CC of 37.6 fC). This decrease of CC shows the

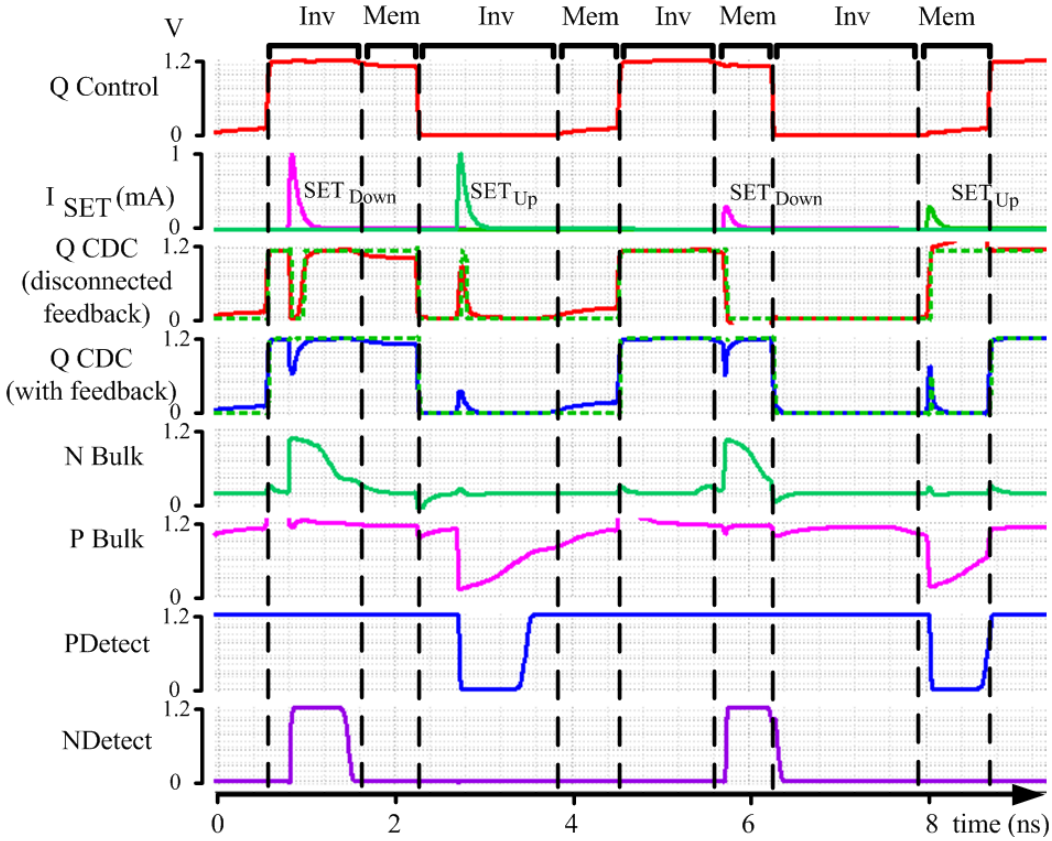


Figure 4.14: Difference between a CDC that uses feedback for correction and another that does not when state changing SETs occur.

vulnerability of the memory mode. *Q CDC* with and without feedback signals show the output Q in solid line and in dotted line the logic state detected by the comparator. The signal *Q CDC disconnected feedback* has glitches able to change the logic state. For the SETs in the memory state the information is completely lost. In this case the critical charges for the inverter mode is 80 fC and 12 fC for the memory mode. The signal *Q CDC with feedback* has smaller and quicker glitches than *Q CDC disconnected feedback*. Those glitches are small because of the feedback transistors compensation. The activation of the feedback transistors takes place 6 ps after the SET is detected. The output Q can reach the switching voltage, but since the compensation acts so rapidly the next gate does not have enough time to react. This makes the signal *Q CDC with feedback* resemble to *Q Control*. *N bulk* and *P bulk* show the effect of an SET on the voltage of the bulk of the CDC. This voltage variation is detected by the BICS to generate the feedback signal and then indicate the SETs with the *P Detect* and *N Detect* signals.

Figure 4.15 shows the same simulation as in Figure 4.14 but this time the SETs

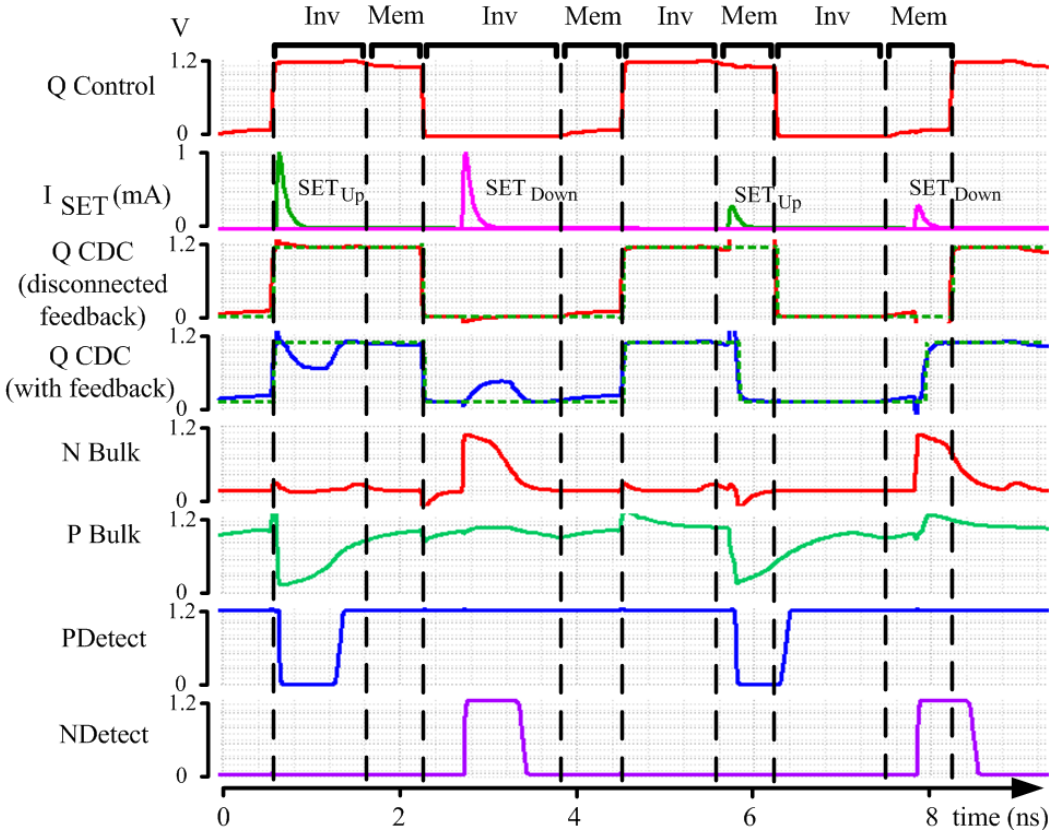


Figure 4.15: Difference between a CDC that uses feedback for correction and another that does not when same state SETs occur.

are not supposed to cause a change of logic state but maintain it. The *Q CDC disconnected feedback* signal resembles the *Q Control* one. On the other hand some variations can be observed in the *Q CDC with feedback* signal. Concerning the inverter mode, when a non-changing state SET takes place, the BICS detect this event and activate the feedback signal anyway. This is the case if SET_{Up} (resp. SET_{Down}) occurs when the output is "1"(resp. "0"). Since the logic of the CDC is very simple, to avoid a complexity overhead, the feedback transistors are sized in order to avoid a change of state in this case. That is why they are activated, but their action is not enough to change the state and generate an error. That is the reason for the curves on signal *Q CDC with feedback*. Since they do not reach the threshold 0.6 volts the logic state remains. In the case of the memory mode the C-element relies on the output capacitance to keep the logic state. Unfortunately this capacitance alone is not enough to counteract the effect of the feedback transistors that generate change of state anticipating the next logic state. This action of the feedback

transistors indeed anticipates the next transition but avoids any glitch at the output.

Three remarks can be drawn from Figures 4.14 and 4.15. The first is that, in the four cases of impacts (two in inverter mode and two in memory mode), the CDC is efficient to counteract the SETs in 3 out of 4 cases, and gives an indication that such event took place in all of them. The second one is that the remaining case, when a non-changing state SET occurs during the memory mode, has a less probability of occurrence. Since the memory time corresponds to the delay δ, and this time is necessarily shorter than the inverter mode, an SET is more likely to take place during the inverter mode. The last remark is that for the tolerated critical charges the CDC does not generate any glitch caused by SET current pulses.

4.2.3 ENCODING AND DECODING

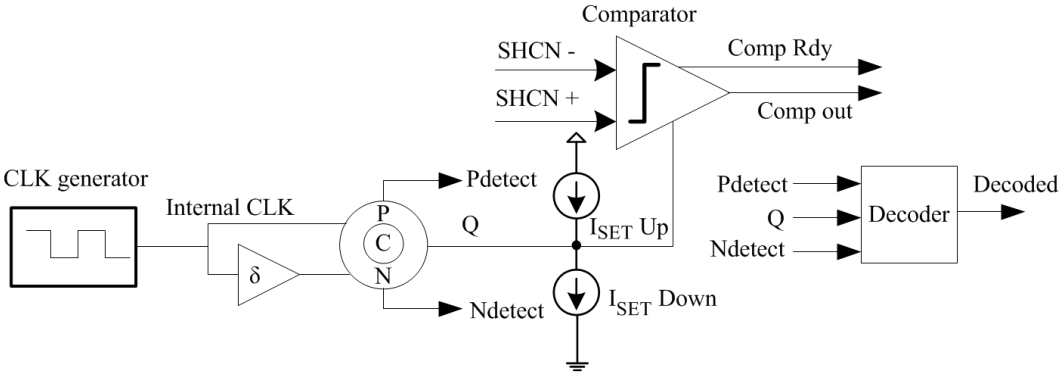


Figure 4.16: Test bench to simulate the recovery of information thanks to the encoding provided by the CDC.

A question remains and is what happens when an SET is powerful enough to create a glitch at the output if the critical charge is exceeded. The solution to this problem is given thanks to the encoding of the information by the three outputs of the CDC: Q, Pdetect and Ndetect. Following the logic Table 4.1 a decoder was proposed and illustrated in Figure 4.4. Using that decoder at the outputs of the CDC as depicted in Figure 4.16 a comparison between the disturbed Q signal and the decoded one can be shown. For that purpose a simulation was carried out and is shown in Figure 4.17.

Figure 4.17 shows a Q signal disturbed by glitches in comparison to the glitch free signal *Q Control*. The injected currents have a peak of 1.8 mA. This value is

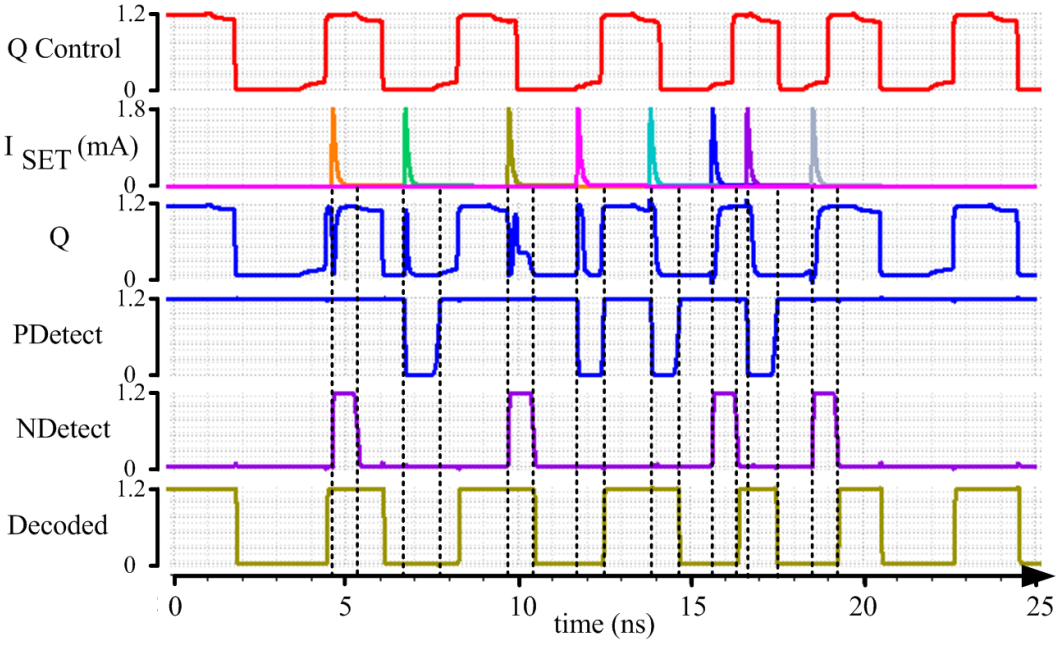


Figure 4.17: Recovery of information thanks to the encoding provided by the CDC.

above the limits of the CDC. Thanks to the *P Detect* and *N Detect* signals, the decoder can recover the state and produce a glitch free *Decoded* signal.

Supposing that a particular application requires a hardening above the one offered by the correction with feedback, this encoding characteristic can be useful. Nevertheless the encoding requires an extra implementation of the decoding logic and implies additional complexity in relation to the correction solution. The decoder uses the logic of a C-element but with three inputs (cf. Figure 4.4 Chapter 3 Section 4.1.3), thus it can be applied to C-element-based hardened flipflops such as those from Devarapalli *et al* [DZHS10], Glorieux *et al* [GCG+13b] and Gang *et al* [CGG13]. The decoder can be placed as the input logic of an SEU hardened memory cell.

This concludes the electrical simulations of the three properties of the CDC solution. The next section will compare the performance of the CDC to that of other SET filters to show the advantages and drawbacks in relation to other state of the art solutions.

4.3 COMPARISON WITH OTHER SET FILTERS

The properties of the CDC solution being exposed, this section continues by comparing them to that of the other SET filters illustrated in Figure 3.16 of Chapter 3 Section 3.5.2. For easiness those architectures are recalled in Figure 4.19 of this section. First, the test bench will be established and then electrical simulations will be exposed to illustrate the behavior of each solution to the same SET impact. Afterwards a critical charge, area, power and sensitive drain area analysis will be done on every solution. This section will conclude by a performance comparison. The work in this section was published in the IEEE TCASII journal [GTASJ14].

4.3.1 TEST BENCH

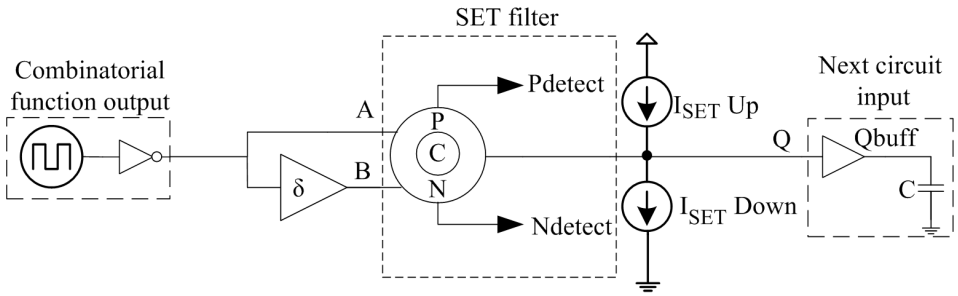


Figure 4.18: Test bench for simulation.

To compare the behavior of the CDC architecture with other filters, the test bench in Figure 4.18 is used for simulation with CADENCE tools for the ST Microelectronics 65nm bulk CMOS technology. A pulse generator followed by an inverter will provide a realistic signal before the SET filter. Then the filter is placed with the same delay buffer for all the filters. Inside the dotted line box is located the C-element with the hardening. This is where the different filters are placed for simulation. The output Q of the filter is where the SETs will take place, and in order to determine its propagation a buffer followed by a capacitor load will serve as next circuit input. The tests focus on the response of the output Q when SETs take place. The SETs are modeled by current sources $I1_{SET}$ and $I2_{SET}$ that inject a transient current between the bulk and the drain of the transistors at the output of the filter. The current has a peak of 324 μA after 0.4 ps, then it decreases exponentially during 2 ns. This current brings the minimum critical charge to the CDC in the memory mode, as was presented in the previous section. The current model was used in a previous work [GTSAJ13]. The same set up used in Section 4.2 is used here. The supply voltage is 1.2V, the delay δ of the buffer is 0.9

ns and the final output capacitance is 0.33fC that represents the load after the buffer.

4.3.2 ELECTRICAL SIMULATION OF SET IMPACTS ON DIFFERENT FILTERS

To compare the properties of the proposed C-element with detection and correction (CDC) and challenging architectures, results of the simulations are shown in Figure 4.20. The simulations compare the responses of a C-element without any hardening, of a C-element with a CDC and the solutions illustrated in Figure 4.19. These cells have all same inputs A and B which are stimulated by periodic square signals. When A and B are different, all the architectures are supposed to be in a memorization mode, otherwise they act as inverters (C-element,CDC, Cx3, C+ST, C+Str, C+ST+Str) or buffers (C+Latch, C+DICE and the Schmitt trigger).

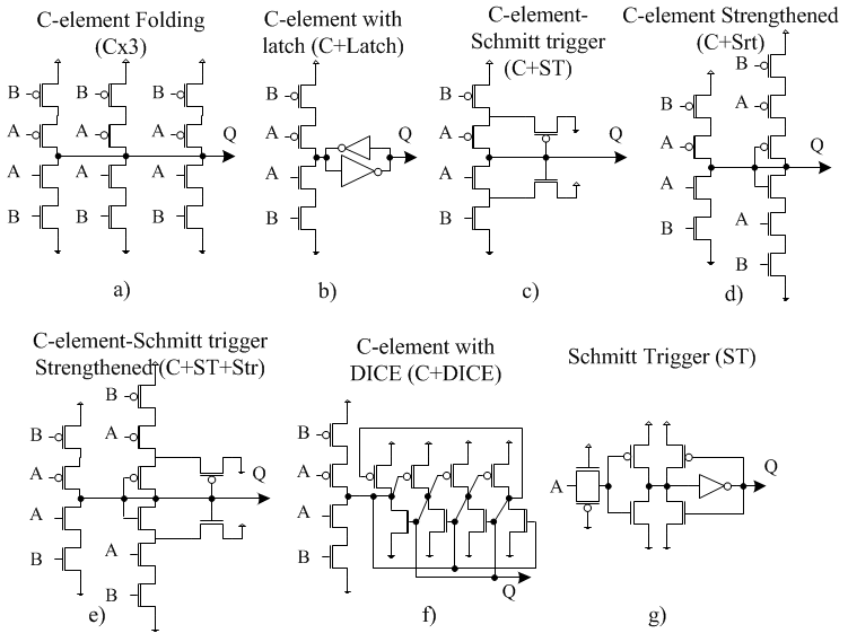


Figure 4.19: a) C-element hardened by folding technique [KAR+09] (C x 3); b) C-element with latch (C+latch) [Mar90]; c) C-element based on a CMOS Schmitt trigger[KS92]; d) C-element hardened by strengthening technique [CAR13] (C+Str); e) C-element as a Schmitt trigger hardened by strengthening technique [CAR13] (C+ST+Str); f) C-element hardened by a DICE cell [CNV96] (C+DICE); g) Schmitt trigger (ST) [SNI06].

In Figure 4.20, signals A and B refer to the inputs, Q *Control* is the control

signal for the output of a C-element which is not hit by SETs. I_{SET} shows the SET current (324 μA) injected at the output node. SETs from (1) to (4) change the logic state, (5) and (7) maintain the same logic state and (6) and (8) is a combination of the two. In (6) I_{SET} Up is twice as large as I_{SET} Down and in (8) is the opposite. Solid lines represent the output Q. The dotted lines represent the signal *Qbuff* at the output of the buffer. *Q Cmin* is the output of the minimal C-element of the 65 nm CMOS technology. *Q C + Sizing* is the output signal of the C-element in the CDC, but without hardening. The outputs of the challenging solutions are *Q Cx3* (Figure 4.19 a)), *Q C+Latch* (Figure 4.19 b)),*Q C+ST* (Figure 4.19 c)), *Q C+Str* (Figure 4.19 d)), *Q C+ST+Str* (Figure 4.19 e)), *Q C+DICE* (Figure 4.19 f)) and *Q ST* (Figure 4.19 g)). *Q CDC* is the output of this work's solution. *Pdetect* and *Ndetect* are the detection signals from the BICS of the CDC.

Figure 4.20 shows that there is not a significant difference of propagation delay between the C-element based filters and the *Control* output, thanks to the absence of a significant amount of hardware at the output node Q. This figure also illustrates the effects of eight impacts on every challenging hardening architecture. When in inverter (or buffer) mode and memory mode, all signals but *Q CDC* show glitches and loss of information. This can be seen by the unexpected glitches and unwanted transitions in relation to *Q control*. The unwanted transitions are seen in the memory mode. If *Q C + Sizing* and *Q CDC* are compared, it is clear that the hardening technique helps correcting the error as soon as it takes place. The CDC benefits from signals *Pdetect* and *Ndetect* which are activated when the respective transition happens activating the respective feedback transistor for compensation. Thus the output of the CDC circuit is the most similar to the reference output *Q Control*. An interesting aspect is shown by the buffer output *Qbuff*, represented as a dotted line and superposed over the *Q CDC* curve. The changes of logic state happen too fast for the buffer to detect them generating a glitch-free buffered signal. If the current is intense enough, the correction system is not able to compensate and glitches can appear. In that situation, at least *Pdetect* and *Ndetect* indicate that a problem happened and, using the decoder, the information can be retrieved, as illustrated by signal *Decoded*. The events at 7.8 ns (5) and 11 ns (7) show that I_{SET} Up induces a "1" and I_{SET} Down induces a "0". The induced state is the same as the state of the output, and so, no feedback should be applied to correct the state because the state is correct. Of course *Pdetect* and *Ndetect* indicate that the event happened but thanks to the sizing of the feedback transistors of the CDC the logic state does not change. This voltage variation happens because of the difference of potential with the active transistors of the C-Element. One final situation is the multiple SET at 9.4 ns (6) and 12.4 ns (8). At (6) the intensity of I_{SET} Up is lower than that of I_{SET} Down the resulting effect is a transition to 1 because of the sizing of the feedback transistors. At (8) the intensity of I_{SET} Up is higher than that of I_{SET}

Down and the resulting effect is a transition to 1. As a consequence, a glitch takes place because a double SET is detected and both feedback transistors are activated. In the case of a double error, the indication is given by the detectors and for further hardening the decoder can recover the state.

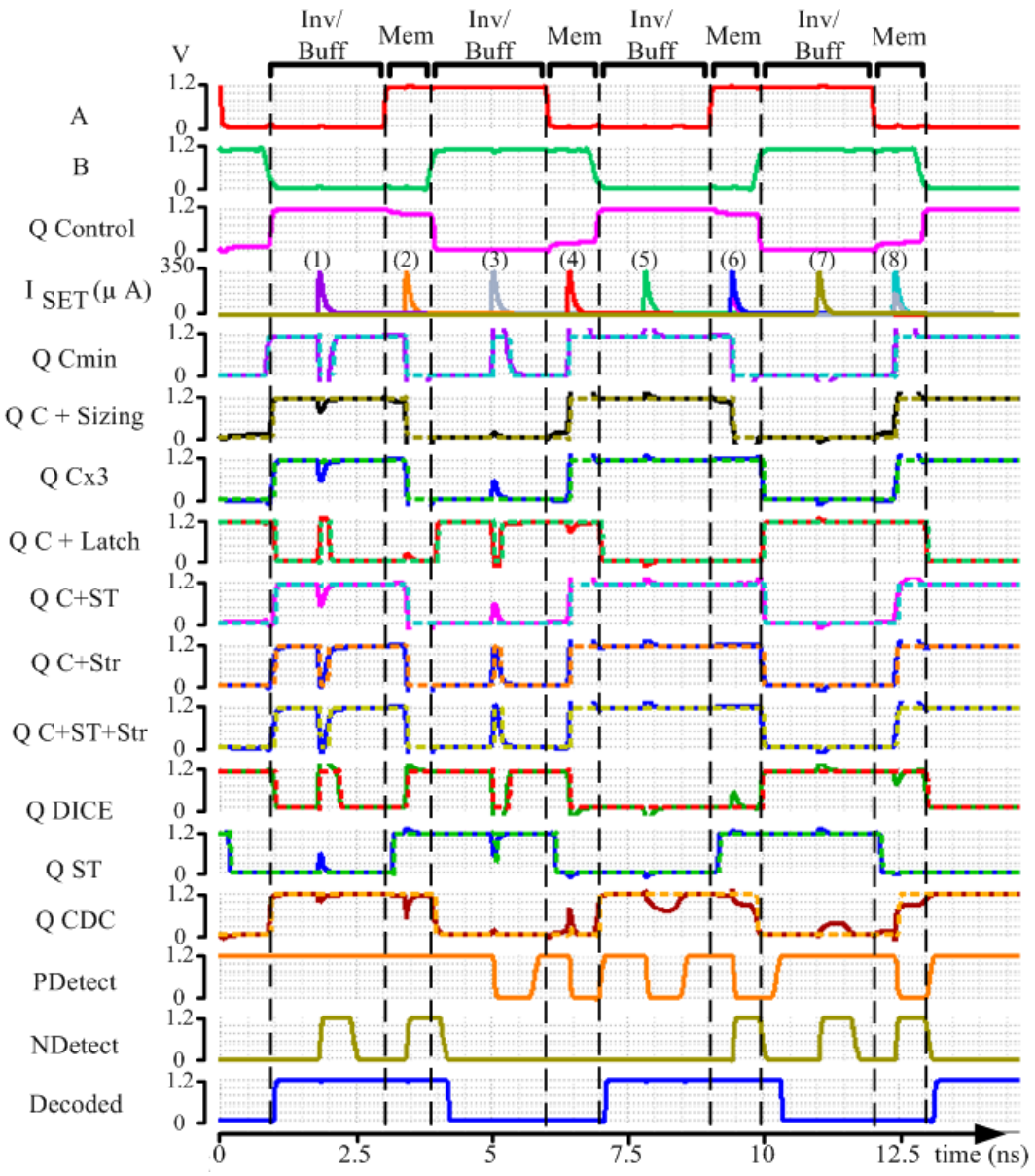


Figure 4.20: Filters response to SET effects during the inverter/buffer and memory modes.

4.3.3 Performance parameters of SET filters

The performance of the circuit was evaluated by electrical simulations with CADENCE. To determine the propagation delay and power consumption, the circuit was simulated into the low power asynchronous SAR ADC. The propagation delay of the CDC with a delay buffer of 0.88 ns is 0.95 ns. The power consumption of the CDC is 1.58 μW in a normal conversion cycle at the sampling rate of 10 MHz. The buffer delay can be implemented in various ways, given the buffer architecture used in this work its power consumption is 2.8 μW. The minimal current detectable by the sensors is 55 μA (obtained by electrical simulations). The critical charge of the output node for the inverter mode is 95.5 fC and for the memorization mode is 37.6 fC. The CDC surface (19.5 μm^2) is obtained by assembling the transistors together for an estimation of the area of a compact layout (*cf.* Appendix F Figure F.4 b)). This is taken as a reference for the minimal size of integration for the circuit in silicon. The simulations on this section do not take into account the parasitics from the layout implementation. This matter will be treated in Section 5.1.

In order to present a comparison as fair as possible, the CDC is compared to the other types of filters presented in Figure 4.19, including the smallest C-element of the technology (Cmin) and a 2.6 times larger C-element (C+Sizing). The comparison is made in terms of critical charge (CC), area (A), Sensitive Drain Area (SDA) and dynamic power consumption (P). Those aspects are shared by the other solutions. The propagation delay of the filters is not taken into account in this electrical comparison, because the simulations did not showed a substantial difference between the delays as was observed in Figure 4.20. The propagation delay of the filters will be taken into account for the study of the layout's extracted circuits in Chapter 5 Section 5.4. The CC is calculated as the charge inserted by the SET current. The layout of each filter is shown in Appendix F. The SDA was chosen instead of the cross section parameter because it is simpler to obtain, and the cross section is linked inherently to the size of the drains. The SET detection and the encoding of information in temporal filters is a novelty and thus is an additional aspect aside of the comparison.

Figure 4.21 shows the area (A), the Sensitive Drain Area (SDA) and the dynamic power consumption (P) of each circuit compared. The area of each circuit was obtained from the layouts done in CADENCE, and the sensitive area is the area of all the drains that can contribute to the disturbance of the output. As exposed in Chapter 2 Section 2.2.2 the drains that, most likely, can contribute to cause SETs at the output of a function are the three in series from the output. For the CDC this area is only the sum of the drains in the C-element and the feedback transistors, because the other transistors cannot induce an SET at the output. Among the circuits

the CDC solution has the largest area. But the SDA represents only 9.3% of the total area. This SDA/A ratio is the smallest of all the other hardening techniques. Furthermore, a closer look on the power shows that the CDC solution consumes less power than the average of the other circuits. In comparison to the others it is very energy efficient since only the C-element (4 transistors) in the CDC structure switches in normal operation. In the other circuits, either the transistors are larger or their number is up to 12. This makes their consumption larger because those transistors switch continuously, or in the case of C+ST, the feedback transistors are constantly on.

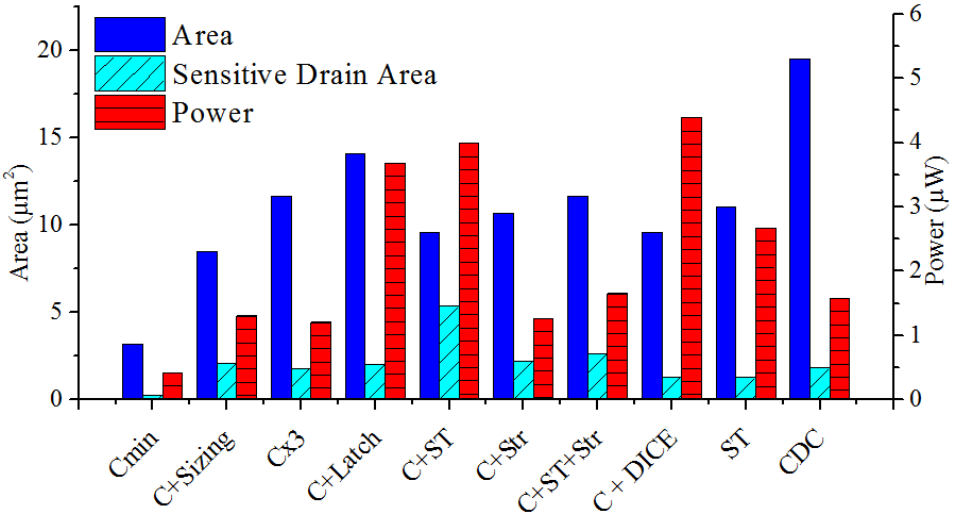


Figure 4.21: Area, Sensitive Drain Area (SDA) and dynamic power consumption for the different techniques.

Figure 4.22 shows the critical charge for each filter in the inverter/buffer mode and in the memorization mode. The interest of designing using a hardening technique is shown by the increase of the critical charges between the simplest C-element (Cmin) and the other circuits for the inverter/buffer mode. Only the C+Latch, the C+DICE and the CDC increase significantly more the critical charge for the memory mode. In terms of temporal sensitivity, the memorization mode is more vulnerable because of the low critical charge, but its duration in time is smaller than the inverter/buffer mode. This makes the inverter/buffer mode the most vulnerable in time. The Schmitt trigger (ST) has the advantage to have only the buffer mode, and being equally robust in time. But its drawback is that it relies on the filtering capabilities of its output latch. It only filters SETs coming before the output latch and with duration smaller than the propagation delay of the latch (48ps in this case). Thus if an SET occurs at the output it will propagate.

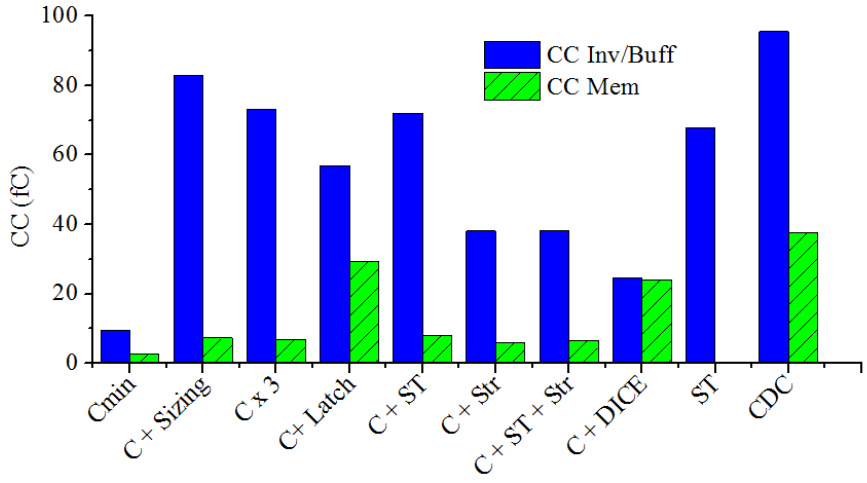


Figure 4.22: Critical Charges of the different RHBD techniques during inverter/buffer mode and the memorization mode.

4.3.4 Synthesis

To give an index of performance is quite complicated because it is application dependent. For example, some applications favor low power consumption over area, others favor small circuit areas at the price of a high power consumption, but they all want reliability. In order to compare the performance of the circuits, seven metrics where established. Those metrics are expressed in relation to the smallest C-element in the 65nm technology. This means that if the metric is bigger than 1, there is a gain in performance, on the other hand if the metric is less than 1 there is a loss. The metrics express the gain in robustness, given by the critical charge, over what has to be paid in power ($CC/P_{Inv/Buff}$), in total area ($CC/A_{Inv/Buff}$), or in sensitive drain area ($CC/SDA_{Inv/Buff}$). Those metrics where evaluated for the inverter/buffer mode and have counterparts for the memorization mode (CC/P_{Mem}, CC/A_{Mem}, CC/SDA_{Mem}). Finally the last metric compares the ratios A/SDA of the minimal C-element and that provided by the hardening techniques to see the price that has to be paid sensitive drain area for the whole area of the circuit.

For simplicity of the Figure 4.23, only the circuits whose metrics outperform the CDC ones are shown. The CDC solution has a remarkable performance in the memorization mode for the three metrics. In the inverter/buffer mode it stays behind for $CC/A_{Inv/Buff}$, in which the sizing technique (C+Sizing) has the maximal optimization in terms of total area in the layout. For $CC/P_{Inv/Buff}$ the CDC is nearly as good as the sizing technique. In terms of $CC/SDA_{Inv/Buff}$ performance it is as good as the Schmitt trigger (ST). Finally, for the ratio A/SDA, the CDC

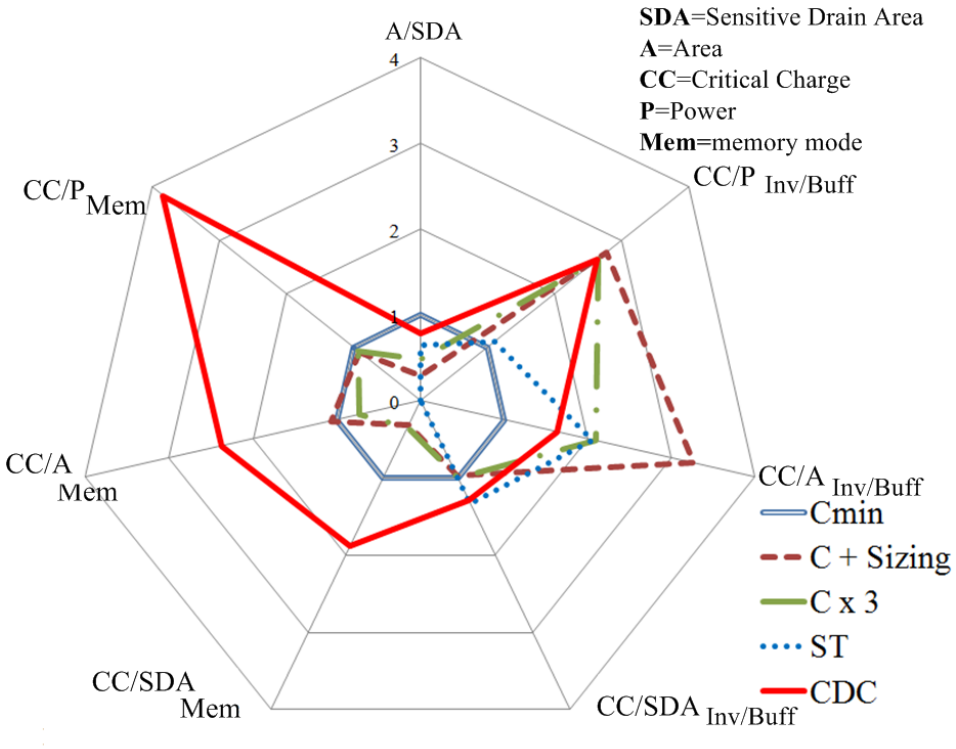


Figure 4.23: Performance metrics for the different hardening techniques.

architecture is the closest to the minimal ratio set by the minimal C-element. The CDC regroups in one circuit, various performances of the other techniques and improves significantly the robustness of the memorization mode for all the metrics by paying the price of an area overhead.

This section explained the characteristics of the architecture of a C-element with Detection and Correction (CDC) capabilities. Thanks to the BICS sensors and the feedback transistors, a simple C-element can be hardened. It can achieve self healing capabilities and can give extra information about the output via *Ndetected* and *Pdetected* signals. Its low power consumption is a good advantage for low power applications such as the SAR ADC. The price to pay is an area overhead because of the BICS and the size of the feedback transistors. The CDC architecture offers a check point from which reliable information can be expected, for the critical charge that it tolerates. The use of this architecture can be an alternative to the use of redundant hardening strategies (TMR), which have a significant area and power.

4.4 Conclusions

The CDC solution offers low power overhead and high robustness, easy placement on the SAR ADC in exchange of reasonable propagation delay overhead. An area overhead in relation to the other filters is expected. In this chapter the architecture of the C-element with Detection and Correction was presented. The performance aspects are accomplished with a combination of a C-element based SET filter with BICS and feedback transistors. The main idea is to mitigate an SET as soon as possible to prevent a wrong logic state reading for the next circuit after the CDC.

This chapter also explored the electrical characteristics of the CDC through simulations. The CDC solution is able to stop the propagation of SETs thanks to the action of the delay buffer and the logic of the C-element. The CDC has self-healing that helps recovering the C-element itself from SETs. This is achieved with Built-In Current Sensors (BICS) and feedback transistors. Also, the CDC has the possibility of encoding information on-line, thanks to the signals of the CDC output signals. It is the first design of its kind using BICS and feed back transistors to create a micro-feedback-controlled system. This work was published in the IEEE TCAS II journal in September 2014 [GTASJ14]. The CDC proved to have a high efficiency of power consumption relative to the hardening when compared to other state of the art filters. It was also predicted to be efficient towards the sensitive drain area relative to the total area of the circuit. In addition, it proved to be strong for the memory mode above the other solutions. Thanks to its detection abilities if an ionizing hit is too strong for the feedback, at least a detection signal indicates that an impact took place. Finally the coding possibility can increase the hardening when a decoding circuit is placed on subsequent stages after the CDC. After the parasitics free analysis in this chapter, Chapter 5 will focus on the layout implementation of the CDC and the impact of the parasitics extraction on the performances.

Chapter 5

Towards the silicon implementation of a C-element with Detection and Correction (CDC)

The previous chapter exposed the C-element with Detection and Correction (CDC), a hardening architecture for a C-element based SET filter. The CDC can filter SETs, detect ionizing impact on its C-element, and can auto-compensate an SET at its output (for the critical charge it tolerates). An additional feature is the encoding of information thanks to the three outputs. This solution was compared to other state of the art SET filters, and showed interesting performances in robustness in relation to power consumption and small sensitive drain areas and the memory mode. This chapter focuses on the layout implementation issues and the impact of the extracted parasitics on the CDC performances. The technology used is the 65 nm CMOS from ST Microelectronics. The first section will explore the issues of the layout design. The second section will compare different layouts and their extracted performances to chose the most appropriate CDC. The third section will show the encoding capabilities of the extracted CDC. Finally, the performance of the chosen CDC is going to be compared to that of the extracted circuits of the other state of the art filters. This will show the difference of the extracted performance in relation to the performances exposed in the previous chapter.

5.1 Layout design considerations

The architecture of the CDC requires the sensing of the bulks of the N-type and P-type transistors to activate the feedback if an ion strikes. This sensing has to be exclusively done in the bulks of the C-element, otherwise hits of other cells will be sensed. That is why the layout design has several considerations to take into account. This section will start with the layout considerations of the exclusive sensing of the bulks. Then the performance degradation of the extracted circuit in relation to the parasitics free circuit will be discussed. Finally, to improve the layout performance

two solutions will be given to speed up the response.

5.1.1 EXCLUSIVE BULK SENSING AND PARASITIC DIODE

A compact approximated layout of the CDC has been used previously to estimate the layout's surface in Chapter 4 Section 4.3.3. This was an approximation of what the ideal layout should be like if the CDC could be implemented in such a compact way. However, the sensing of the current of the C-element's bulk has a particularity. That current has to be the only one sensed by the BICS, excluding that of any neighboring circuits. The PMOS transistors benefit from an exclusive N-well. But the NMOS transistors share the bulk of P-substrate with all the NMOS transistors of all the other functions. To ensure that those NMOS transistors have an isolated bulk, an enclosure has to be created using classical N-wells and a deep N-well connected as suggested in Simionovski's work[SW14]. This is illustrated in Figure 5.1. This N-well enclosure demands an area overhead that is dictated by the manufacturer's rules for the layout. Indeed, the perimeter of a deep N-well has to be surrounded by an N-well to complete the enclosure. On each side of the perimeter border the N-well has to be 1 μm wide. That makes an addition of 2 μm of N-well on each direction.

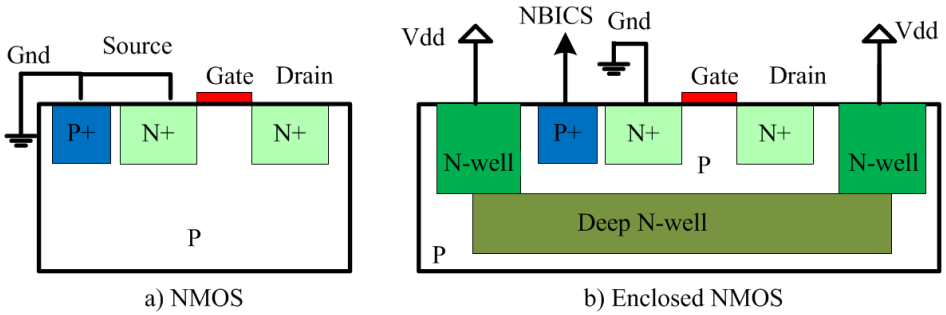
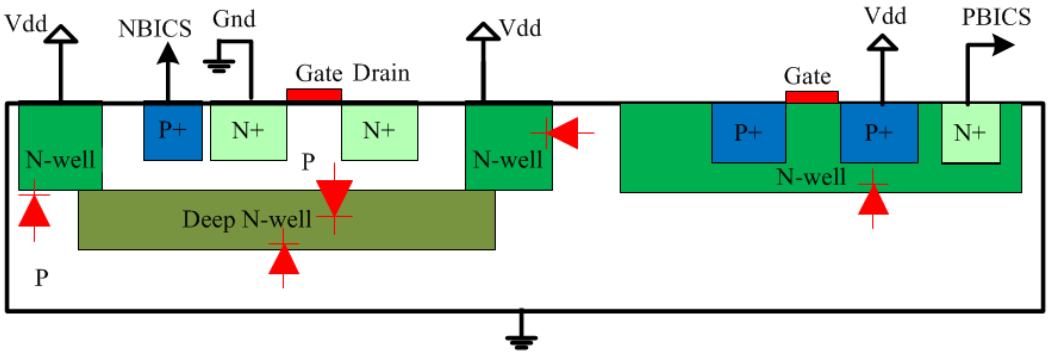


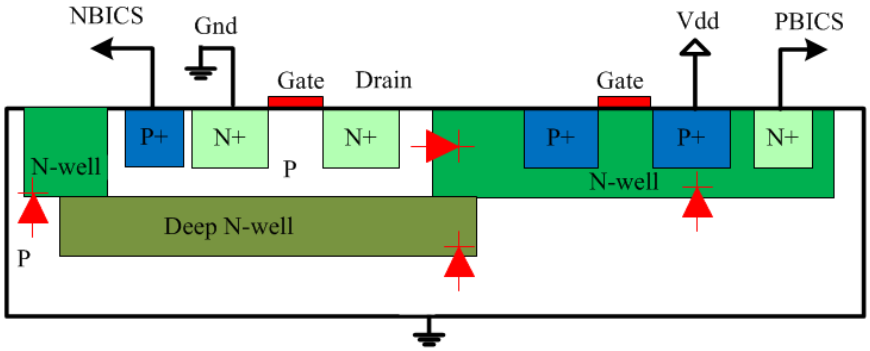
Figure 5.1: Deep N-well enclosure for an NMOS transistor.

The introduction of a deep N-well adds a parasitic diode that connects the bulk of the NMOS transistors to the N-well enclosure. Additional diodes exist inherently because of the PN junctions between the P-substrate and the N-wells. Usually those diodes have not a significant effect on the transistors functioning because they are connected in reverse bias. In addition to that, the fact that the N-well requires a significant area overhead poses a dilemma for the layout. On one hand, the wells can be completely separated ensuring the closest representation of the schematic circuit as represented in Figure 5.2 a). The problem is that this will require additional area because of the bulk separation. On the other hand, the N-well of the PMOS transistors can be part of the enclosure of the NMOS ones as illustrated in Figure

5.2 b). This reduces the area of the circuit taking advantage of the N-well for the enclosure. The only issue is that this option links by a diode both of the bulks and two parasitic diodes (a deep N-well diode and an N-well diode) are linked to the input of the PBICS and not to a source.



a) Separation between the NMOS bulk and the PMOS bulk



b) Contact between the NMOS bulk and the PMOS bulk

Figure 5.2: Deep N-well diode connections between two configurations of enclosure for an NMOS transistor.

However, those diodes are polarized in reverse bias thus there is no a risk of charge sharing during normal operation. Actually the diode linking the NMOS transistors bulk (N-bulk) and the PMOS's (P-bulk), can be used as an additional path of evacuation of the parasitic current in the N-bulk. As far as the BICS connection is concerned, each BICS can be placed on each concerned bulk. This avoids further area overhead, because if the BICS are placed outside the wells an additional distance between the wells has to be respected for the layout. In this case the distance between a new N-well and the deep N-well has to be 2.5 μm. A first layout version can be seen in Appendix F Figure F.5.

To understand the effect of the presence of this diode and what to expect for the

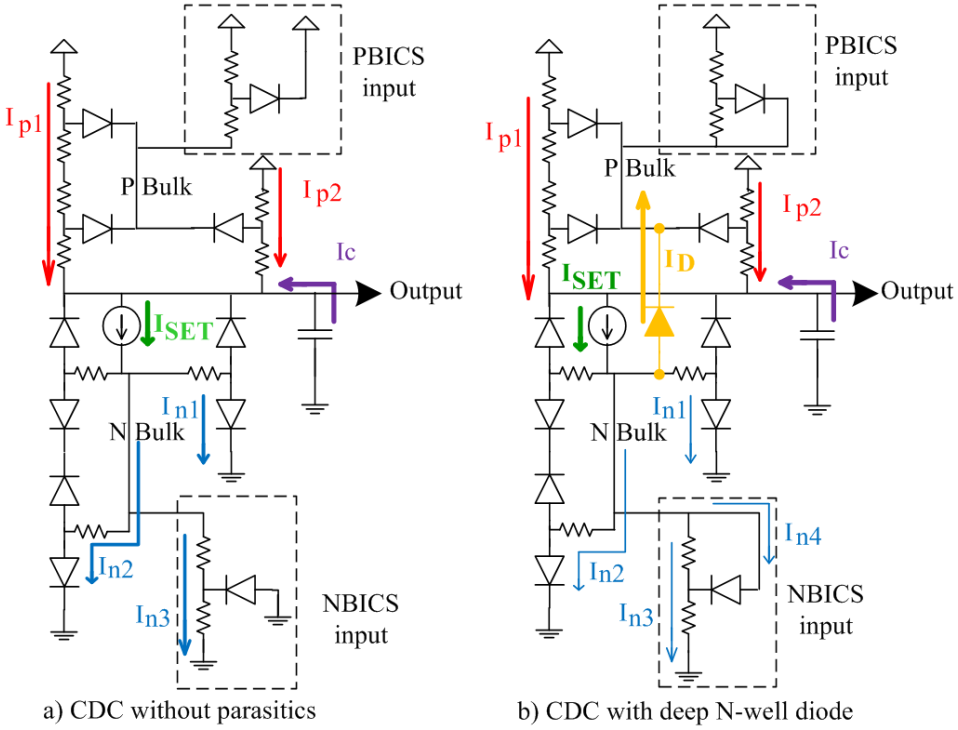


Figure 5.3: Currents behavior in a parasitics free CDC (a) and a CDC with the parasitic deep N-well diode (b).

robustness of the circuit, the CDC without the diode will be compared to the CDC with the diode. The situation represented in Figure 5.3 shows the PMOS transistors of the C-element in active mode and the NMOS in off mode. The PMOS transistors of the C-element and the PMOS feedback transistors are active to compensate the current I_{SET} with currents I_{p1} and I_{p2}. On the N-bulk side the currents I_n dissipate the added charges to the ground. With the I_{n3} going through the input transistor of the NBICS, SET is sensed by the resistors. In Figure 5.3 b) two connections are different. First a diode connects the two bulks, and second the NBICS sensing transistor's bulk is connected to the N-bulk instead of the ground. Those two changes create two new paths for the dissipation of the I_{SET} current. Since the diode has a large area it can let pass a large amount of current, thus I_n currents will be smaller than for the situation in Figure 5.3 a). This means that the sensing current I_{n3} will be smaller and probably a compensation has to be done, this will be the subject of further analysis in subsection 5.1.3. A smaller value of I_{n3}'s magnitude means also that the extracted representation of the CDC will certainly have a decrease of robustness. The cause is that the BICS will be activated slower than predicted, the feedback transistors will be activated with a certain delay and that lets time to an ion strike to act more. This decrease of robustness is translated in a decrease of the critical charge of the extracted version of the CDC in relation to the schematic.

5.1.2 DIFFERENCE OF PERFORMANCE BETWEEN THE SCHEMATIC AND THE EXTRACTED VERSION OF THE CDC

To illustrate the difference of the behavior between the schematic design of the CDC, which is parasitics free, and the extracted a simulation was made. The schematic described in Figure 4.2 of Chapter 4 Section 4.1.2 is used for the CDC without parasitics. For the extracted CDC the circuit comes from the first layout attempt (*cf.* Appendix F Figure F.5). The simulation uses the same test bench presented in Figure 4.18. To give a more realistic approach the test bench uses the circuit extractions of its components to simulate parasitics. This gives at the output of the CDC a more realistic load. Figure 5.4 shows the response of both circuits to the I_{SET} current for the parasitics free critical charge of the combinatorial mode (173 fC). The critical charge increases from that of the test bench without parasitics (95 fC). Dotted lines show the parasitics free circuit behavior and solid lines that of the extracted.

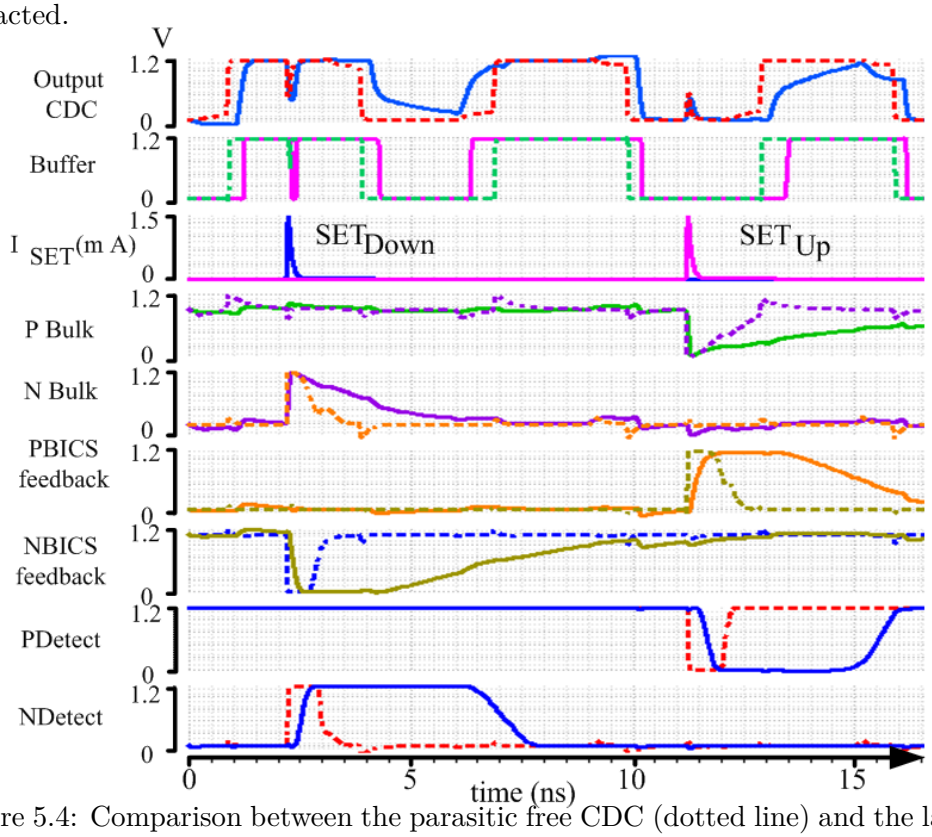


Figure 5.4: Comparison between the parasitic free CDC (dotted line) and the layout extracted version (solid line).

In Figure 5.4 the decrease of robustness can be clearly seen for the *Buffer* signals. For the first extracted version of the CDC the state has already changed (solid line) instead of being in the threshold like the CDC without parasitics version (dotted line). Also an important distortion of the *Output* signal can be observed and can be explained through the behavior of the bulk, the BICS feedback, and detection signals. As far as the bulk is concerned, the extracted circuit shows that the effect of the ionizing hit lasts longer than the parasitic free case. A parasitic RC effect prevents the bulk current to be evacuated as soon as possible. This effect causes that the feedback transistors are active more time than needed, which drives the distortion of the output signal. Another consequence of that is that the *PDetect* and *NDetect* will be active more time than expected. Nevertheless, this alone does not explain the robustness decrease. The basic principle of the CDC action is a quick response to an SET. In the first extracted version, the RC parasitics generate a delay in the response. The feedback signals of the BICS to the transistors have increased their switching time. This delays the activation of the feedback transistors to compensate the SET, explaining the diminution of the critical charge to 125 fC, which compared to the CDC without parasitics, is a decrease of 28 % of critical charge.

Characteristics	**CDC without parasitics**	**1st Extracted**
Critical charge Inv mode	172 fC	125 fC
Critical charge Mem mode	108 fC	71.4 fC
Power	1.58 μW	6.89 μW
Area	19.5 μm^2	103 μm^2
Sensitive Drain Area	1.82 μm^2	1.82 μm^2
Feedback response delay	6 ps	140 ps
Gate delay (with 0.9 ns delay buffer)	1.06 ns	1.2 ns

Table 5.1: CDC characteristics of the parasitics free and the first extracted version.

To quantize the differences between the CDC without parasitics design and the first extracted CDC, Table 5.1 shows the key characteristics. As expected the critical charge diminished. The decrease is about 30 % for both modes. The power consumption increased. Also the first extracted CDC is less sensitive since it starts detecting parasitic current from 377 μA. Finally the activation of the feedback increases significantly to 0.14 ns. Those changes are linked to the addition of the parasitic capacitances of the wires and resistances of the contact vias. The signifi-

cant increase of the size of the circuit is a consequence of the conception rules for using a deep N-well in the design. The latency in the extracted version has only increased 0.18 ns.

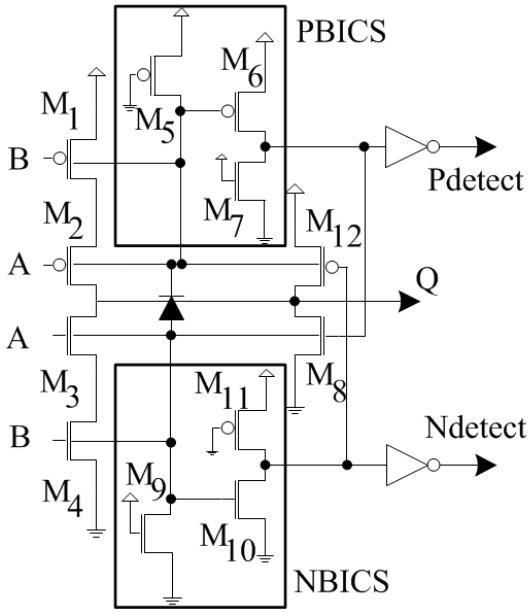
The performance of the parasitics free circuit is difficult to reach because of the real switching time of transistors. The CDC circuit without parasitics has a feedback response in 6 ps, and the extracted can only reach 140 ps. The correction abilities of the CDC rely on a rapid activation of the feedback transistors and the rapid evacuation of the bulk parasitic current. The performance of the circuit can be improved if the bulk current can be evacuated more rapidly and if the feedback response is accelerated. To improve those aspects some layout modifications have to take place.

5.1.3 DESIGN SOLUTIONS

Two issues were previously pointed out, the evacuation of the SET current in the bulk needs to be more efficient, and the speed of the feedback response needs to be increased. To accelerate the evacuation of the bulk current, the resistance of the evacuation paths has to be diminished. The evacuation paths are no other than the PN junctions of the transistors that connect the bulk to the source and the deep N-well diode. A simple approach, without redesigning the C-element or the feedback transistors, consists in reducing the resistance of the sensing transistor (M_5 and M_9 in Figure 5.5). For that, not only the width can be increased, but also the number of contact vias of the transistor. One contact has a resistance of 37 ohms. In Simionosvski's work [SW14] the sensing transistor has only one contact via but the timing of the application is between 50 ns to hundreds of nanoseconds.

In the case of the CDC solution for the SAR, the internal clock has a period of around 6 ns and the action of the CDC requires a high speed feedback compensation. As shown previously, the CDC feedback response has to happen in a small fraction of a nanosecond. If the number of contacts is doubled the resistance is only the half and the current is doubled. This increase of the current's magnitude helps accelerating the detection. This can be seen in Figure 5.6 for the currents of NBICS. This figure shows the I_{SET} current injected between the output of the CDC and the N-bulk. The currents in dotted lines are from the first extracted version and in solid line the currents of the improved version. This is the second extracted version which has the wells joined by a deep N-well diode. The first version has also its wells joined. In the figure, the diode current (I_{Diode}) does not change much because the size of the deep N-well diodes do not change much because the layout redesign avoided a significant area overhead. But the current evacuated through the NBICS doubled with this redesign, accelerating the detection. The feedback current

($I_{Feedback\ NMOS}$) is activated quicker than before, and the feedback action happens closer to the SET. In the previous case (dotted line), the feedback transistor is active much more time, having the risk of injecting current when it is no longer needed.



Transistor	1st Extracted	2nd Extracted
M1	2.5/0.06	2.5/0.06
M2	2.5/0.06	2.5/0.06
M3	2/0.06	2/0.06
M4	2/0.06	2/0.06
M5	0.137/0.7	0.5/1.4*
M6	1/0.06	3.6/0.06*
M7	0.135/0.36	0.4/0.1*
M8	0.6/0.06	0.6/0.06
M9	0.135/0.7	4/1*
M10	1/0.06	3.6/0.06*
M11	0.135/0.36	0.4/0.06*
M12	1.6/0.06	1.6/0.06
DNW Diode	3.6/4.5	4/4.5

* Modified transistors

Figure 5.5: W/L of the transistors and diode size for the first and second extracted versions. Units are in μm.

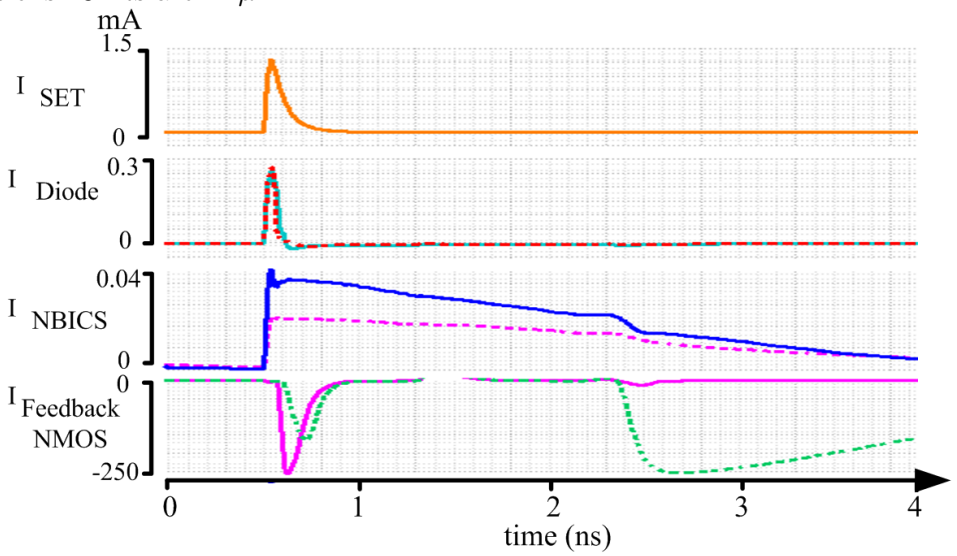


Figure 5.6: Behavior to an SET of the currents of the diode, the NBICS sensor transistor and feedback NMOS. Dotted lines are for the 1st extracted and solid lines for the 2nd extracted.

As far as accelerating of the feedback response is concerned, the only way is to increase the gain of the voltage amplifier in the BICS. For that the transistors M_6 and M_{10} have their width increased and M_7 and M_{11} have their width increased and the length decreased. This redesign also contributes to the increasing of the speed of the feedback response observed with ($I_{Feedback\ NMOS}$) in Figure 5.6.

The benefits from the better evacuation of the current and the acceleration of the feedback response can be seen in Figure 5.7. The figure shows that the second extracted circuit of the CDC gained robustness. The critical charge is now 140 fC instead 128 fC. The *Buffer* signal for the modified CDC reaches the switching threshold whereas the previous version switched totally and the voltage peak reaches 0V. The current evacuation and the amplification accelerate the healing process, activating the feedback signals quicker than before. The feedback signals are activated in 30 ps instead of 140 ps. Finally the detection signals indicate the soft error during less time than before avoiding on one hand further power consumption, and on the other hand further distortion of the output signal.

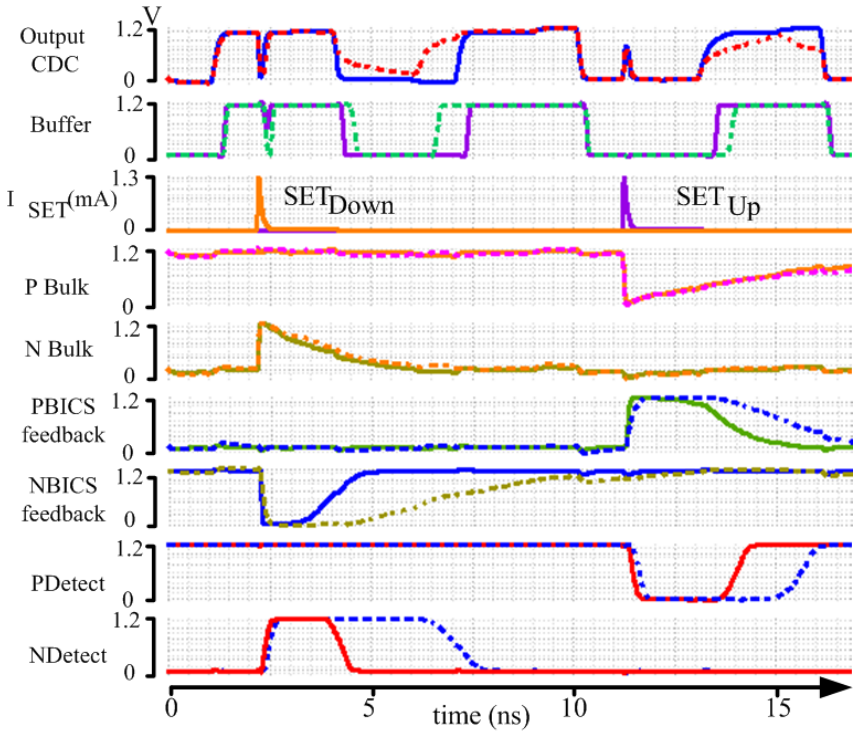


Figure 5.7: Comparison between the first extracted circuit of the CDC (dotted line) and the second one (solid line).

The layout implementation had an important impact on the CDC architecture, and since a more real circuit has been reached, only layouts with joined wells were studied. But the modifications cited before can also be implemented with a layout with separated wells. A performance comparison has to be made between the extracted versions of the CDC presented until now and an extracted version using the separated wells layout implementation. With that information the most appropriate layout can be chosen.

5.2 CHOOSING THE CDC'S LAYOUT

The rapid evacuation of the SET current and the acceleration of the feedback response can be implemented with different layouts. It was stated before that separating the wells for the sensing increases the area of the circuit. But that is not the only parameter that influences the performance. And by a performance analysis can be decided the most suitable implementation of the CDC for the SAR ADC. This means that the power of the CDC has to be as low as possible, as well as the area and the propagation delay. Using the scaling factor α (90/65) [Cri99] [FDN$^+$01], from CMOS 90 nm to 65 nm, the SAR ADC should ideally consume 35.88 μW, with a target sample frequency of 10 MHz and a total core area of 65.2 $\times$ 165.2 μm. The increase of power consumption is caused by the fact that the SAR ADC [HZB$^+$11] has a 1 volt voltage supply (under the 1.8V normally used for the CMOS 90 nm technology), and the CMOS 65 nm technology used in this work uses a voltage source of 1.2V. This sections will focus on a performance comparison of the extracted versions to chose the most appropriate one. First the electrical characteristics are going to be compared and then a performance synthesis will determine te best of them.

5.2.1 CHARACTERISTICS COMPARISON

This subsection compares the electrical characteristics of the CDC circuit without parasitics (*cf.* Figure 4.2 of Chapter 4 Section 4.1.2), used as reference, with those of the first and second extracted versions (*cf.* Figure 5.5). The extracted circuit for the separated wells implementation of the CDC layout is also considered. This circuit will be called third extracted and the only difference with the second extracted is that this one does not have a Deep N-well connected between the wells but directly to the supply voltage. The schematic of that extracted can be seen in Figure E.1 of Appendix E. The different layouts of the three extracted versions can be found in Appendix F. For the first extracted circuit see Figure F.5, second extracted refer to Figure F.6 and the third extracted with separated wells is illustrated in Figure F.7. The four circuits (CDC parasitics free and the three extracted circuits versions) are simulated with the same test bench and the same procedure to obtain the power

consumption as in Chapter 4 Section 4.3. Each circuit is tested with the parasitics free and the extracted versions of this test bench (TB) to see the influence of the parasitics on their performance. The extracted version of the test bench uses the extracted of the circuits composing it to simulate the parasitics. First the power consumption is analyzed, then the critical charge in inverter mode, followed by the CC in memory mode. Finally the area, the sensitive drain area and the propagation delay are going to be discussed.

5.2.1.1 Power consumption comparison

Figure 5.8 shows the difference between the power consumption in a conversion cycle in the SAR ADC for each version of the CDC. In the parasitic free test bench for the 2nd and 3rd extracted circuits a power increase was expected in relation to the CDC without parasitics and the 1st extracted. The parasitics versions show a significant increase of power consumption. However, a decrease of power can be observed between the first extracted and the 2nd and 3rd versions. The power efficiency is enhanced thanks to the improvements on the layout such as the increase of the number of contact vias. Also, the 3rd extracted design has less parasitics that consume power and a smaller deep N-well diode; that is why it is the best layout representation for a low power consumption point of view.

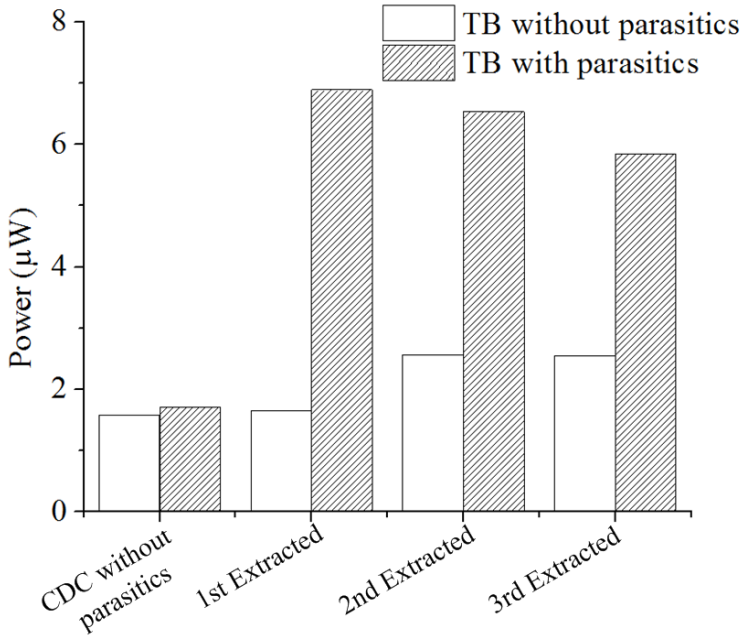


Figure 5.8: Comparison of the power consumption of the CDC versions with and without parasitics.

5.2.1.2 Critical charge comparison for the Inverter mode

In terms of critical charge of the inverter mode, Figure 5.9 shows that the parasitics free CDC has the most important critical charge relative to the others because the feedback action takes place quicker. This trend is preserved in with the parasitic cases. Nevertheless the 2nd and 3rd extracted circuits surpass the first extracted with parasitics. It is the opposite when the critical charge is estimated without parasitics. This proves that the layout oriented modifications that were applied in the 2nd and 3rd extracted worked as intended. The increase of critical charge observed in the parasitics test benches have two the causes for this effect. The first is the additional capacitors and resistance of the transistors of the c-element and feedback. The other is the parasitics of the load (the buffer) at the output of the CDCs. The 2nd and 3rd extracted circuits have almost the same amount of CC. The 3rd extracted circuit, coming from the separated wells layout, has a small advantage because more parasitic capacitances are added at the output because of the separation. So the 3rd extracted circuit is the one that gets closer to the CDC without parasitics.

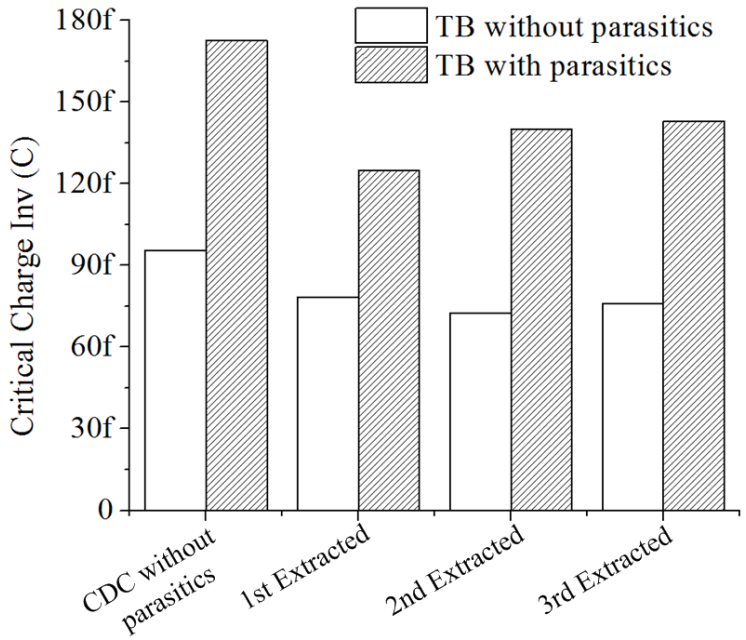


Figure 5.9: Comparison of the critical charge for the inverter mode of the CDC versions with and without parasitics.

5.2.1.3 Crtitical charge comparison for the Memory mode

An opposite trend of that described for the critical charge for the inverter mode occurs for the critical charge in the memory mode (*cf.* Figure 5.10). The way the CDC is constructed, the critical charge of the memory mode is inherently smaller than that of the inverter mode. The charge from the capacitor load can be extracted more easily than in the inverter mode. This mode has more evacuation paths than the inverter mode. And also in the extracted circuits a parasitic diode appears. An example is illustrated by Figure 5.11. The situation shows a strike that hits the NMOS transistors and the action of the feedback PMOS transistor. In the CDC without parasitics a deep-N well diode does not exist and the feedback response is quicker. Also the resistance R of the sensing transistor is smaller in the 2nd and 3rd extracted circuits than in the 1st extracted, thus the decrease of critical charge in those cases. The 3rd extracted circuit (from separated wells layout) suffers from the delay of activation of the feedback transistors because of the distance between the BICS and the feedback transistors. Along the distance separating BICS and feedback transistors, many parasitic capacitors are added, delaying the feedback action. In this case the 1st extracted circuit is closer to the CDC without parasitics because it is the one that has the largest resistance in evacuation paths, preventing the charge of the memory state to leave the circuit.

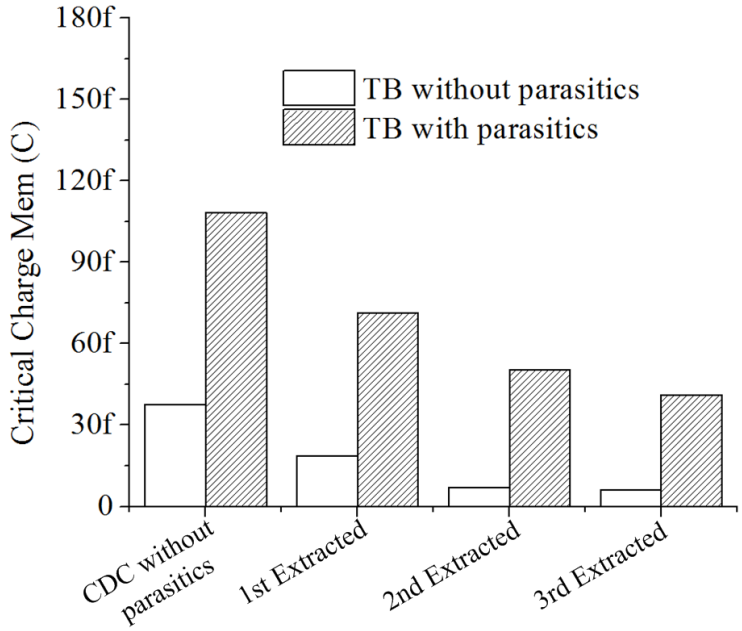


Figure 5.10: Comparison of the the critical charge for the inverter mode of the CDC versions with and without parasitics.

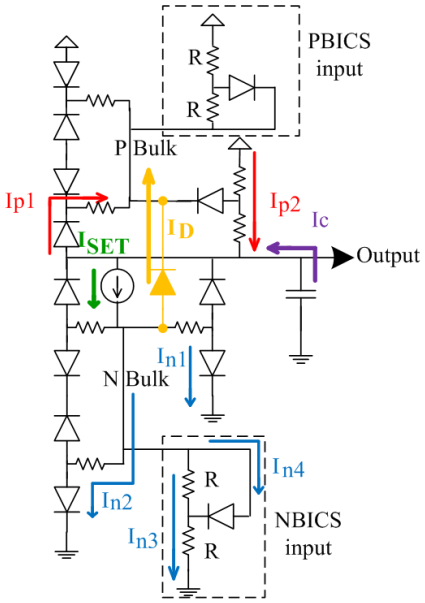


Figure 5.11: Current evacuation paths for the memory mode.

5.2.1.4 Area, Sensitive Drain Area, and propagation delay comparison

The area and the sensitive drain area are directly obtained from the layouts, but the propagation delay is obtained by simulation in the test bench with parasitics. As far as the area is concerned, the 3rd extracted has the most significant area overhead. The separation of wells increases dramatically the size, of what is already a large area implementation in relation to the estimation of the CDC without parasitics. The 1st and 2nd extracted versions of the CDC have almost the same area. What is remarkable of the CDC design is that the sensitive drain area remains the same for any implementation, as long as the transistors of the C-element and feedback are unchanged.

One last aspect is the propagation delay of the CDC. This delay does not vary significantly among the extracted circuits. Using a buffer delay of 1 ns, the CDC without parasitics has a propagation delay of 1.06 ns. For the 1st extracted circuits the delay is 1.2 and 1.13 for the 2nd and 1.14 ns for the 3rd extracted. It is possible to assure that in terms of propagation delay and area overhead the 2nd extracted can be chosen. The different circuits excel for different characteristics so to select the best option the performance will be compared using the metrics of Chapter 4 Section 4.3.4. This will determine the most robust solution for the low area, low

power, and low propagation delay that are required.

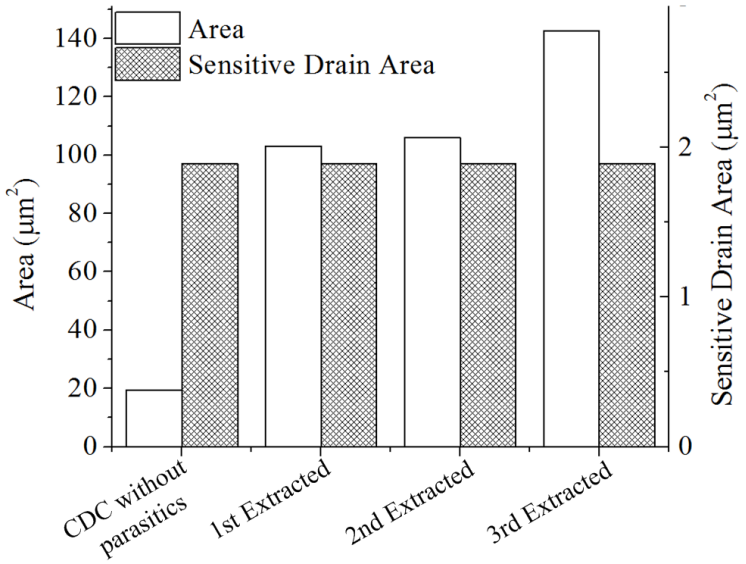


Figure 5.12: Comparison of the area and the sensitive drain area of the CDC versions with and without parasitics.

5.2.2 PERFORMANCE COMPARISON

Finally, to compare the performance of the different layout extracted circuits to that of the CDC without parasitics, the metrics used in Chapter 4 Section 4.3.4 are employed. An additional metric is the critical charge relative to the propagation delay of the circuit. This metric will also be used when the selected extracted CDC will be compared to the other SET filters. It indicates what is gained in robustness at the expense of propagation delay. For Figure 5.13 the layout extracted circuit of the minimal C-element (*Cmin*) is used as reference. The performance of the CDC obtained in Section 4.3.4 is shown for comparison (*CDC ref*). The *CDC without parasitics* curve shows the performance if the reference CDC was perfectly implemented on layout. The other layout extractions of the CDC are also displayed.

The increase of the critical charge and circuit area, in addition to the slower feedback response have changed the shape of the performance curve in relation to the reference CDC (*CDC ref*). An important aspect is that the performance of the Cmin changed, because its critical charge increased with the layout version. This also changed its performance. In terms of critical charge relative to the area (CC/A_{Inv} and CC/A_{Mem}) or the sensitive drain area (CC/SDA_{Inv} and CC/SDA_{Mem}), even the CDC without parasitics cannot have a better performance than the minimal

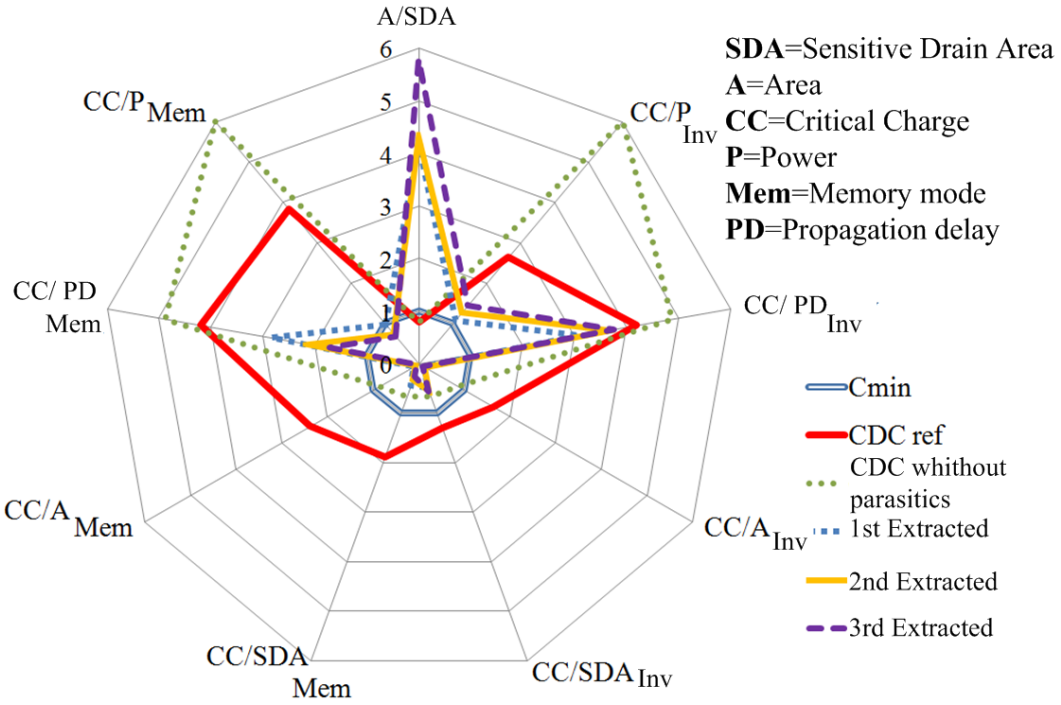


Figure 5.13: Performance evaluation of the different versions of CDC.

C-element. What is gained by the CDC in all its versions is an important efficiency between the robustness and the propagation delay (CC/PD_{Inv}). Another strong point is the performance relative to the power (CC/P_{Inv}) in the inverter mode. The layout's extracted versions are not as strong as the parasitics free or the reference ($CDC\ ref$) versions, but they are more efficient than Cmin. For the memory mode (CC/P_{Mem}) they have a similar performance to that of$Cmin$. The peak of the A/SDA criteria is not a surprise because on the layout versions keep the sensitive drain area unchanged but their effective area increased because of the deep N-well.

The 3rd extracted increased the A/SDA ratio even more in relation to the 2nd extracted, but the other parameters decreased. Only on the CC/P_{Inv} a slight increase in relation to the 2nd extracted. On the other hand the 2nd extracted circuit achieves the most robustness with less area and has the best trade-off of CC per propagation delay (CC/PD) for the inverter and the memory mode. It is the one that reaches the best power, propagation delay, and area performance relative to the critical charge with less circuit area. For that reason is the selected circuit. As a reminder the 2nd extracted version of the CDC comes from the layout of Figure F.6 on Appendix F. In comparison to the CDC of reference, the parasitics and the deep N-well diode affected the robustness in both modes. Also the increase of the layout

area because of the enclosure penalizes the robustness in relation to the area. And finally the increase of the power consumption diminished the performance of the robustness in relation to the power consumption. This analysis will be deepened, with the comparison between the selected extracted CDC's performance and that of the other filters extracted. This will be treated in Section 5.4.

The comparative Table 5.2 shows the characteristics of the selected circuit in comparison to that of the CDC without parasitics and the first extracted circuit. What must be retained is that the critical charge was increased by 10% for the inverter mode in relation to the 1st extracted. The power was also slightly diminished, but more important the feedback reaction time was accelerated 4.3 times.

Characteristics	**CDC without parasitics**	**1st Extracted**	**2nd Extracted (selected)**
Critical charge Inv mode	172 fC	125 fC	140 fC
Critical charge Mem mode	108 fC	71.4 fC	50.5 fC
Power	1.58 μW	6.89 μW	6.53 μW
Area	19.5 μm^2	103 μm^2	105 μm^2
Sensitive Drain Area	1.82 μm^2	1.82 μm^2	1.82 μm^2
Feedback response delay	6 ps	140 ps	30 ps
Gate delay (with 0.9 ns delay buffer)	1.06 ns	1.2 ns	1.13 ns

Table 5.2: CDC characteristics comparison with the chosen layout (of 2nd Extracted).

A final consideration, concerns the delay buffer *cf.* Figure 4.8 of Chapter 4 Section 4.2. The extracted circuit of the layout of this circuit introduces significant parasitics, delay (3 ns), and power overhead. That is why a simpler version is used as depicted in Appendix F Figure F.9 to reach the 1 ns delay used in this work. It is made of two inverters (PMOS (W/L): 0.27/0.135 and NMOS (W/L): 0.135/0.135).

One last aspect concerns the CDC in the SAR ADC. The size of the CDC's layout has been discussed extensively but it is important to compare it to the size of the SAR ADC. The SAR ADC was not implemented in layout for the 65 nm CMOS technology, but an estimation can be done using the scaling parameter α [Cri99] [FDN$^+$01]. This parameter can be defined as the ratio between the channel length of the former CMOS technology and the target technology. In this case $\alpha = 90/65 = 1.38$. In the 90nm CMOS technology, the core of the ADC measures 20520 μm^2

($90 \times 228\ \mu m^2$ [HZB+11]). Thus the estimation is $20520/\alpha^2 = 10703\ \mu m^2$. Given this estimation the area of the 2nd extracted layout represents only around 1 % of the SAR ADC's area. Thus the CDC does not have much impact on the silicon cost of the initial ADC.

5.3 CDC COUPLED WITH THE DECODER

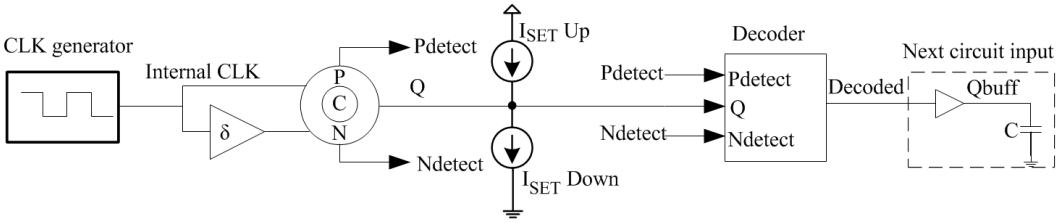


Figure 5.14: Simulation test bench for the couple CDC-decoder.

This subsection will show the simulation of the selected extracted CDC coupled with the decoder presented in Chapter 4 Section 4.1.3. For that the test bench of Figure 5.14 was created. The decoder was proposed as the input logic for a hardened memory element. The decoder combinatorial function needs the outputs *Ndetect* and *Pdetect* and the inverted signals $\overline{Ndetect}$ and $\overline{Pdetect}$. To avoid adding inverters the inverted signals of *Ndetect* and *Pdetect* are taken from the feedback signals in the CDC. The voltage signals of the bulks could be used instead of *Ndetect* and *Pdetect*, because they have the same information, but the capacitance added can change the response of the CDC. So to ensure the feedback signals isolation and an easier adaptation to the decoder the inverters that generate *Ndetect* and *Pdetect* are kept in the design (*cf.* Figure 5.5).

Figure 5.15 shows the simulation of the layout extraction of the test bench. To show the unique feature of this couple CDC-decoder, the SET current is set to a peak of 3.6 mA. That is four times that of what the CDC can resist alone. The signal *Control CDC* serves as a control and shows what happens to the output *Q* (solid line) with such current spikes, as well as the buffer's output (dotted line) if placed right after *Q*, if no decoder is used. It is possible to observe the SETs caused by the currents. *Q* shows the output of the test bench that is connected to the decoder. As *Control CDC*, *Q* is distorted by the SETs. The *Decoded* signal shows the signal at the decoder's output (solid line) and after the load buffer (dotted line). This signal illustrates the behavior of the C-element like logic function of the decoder. Thanks to the transistor's sizing the *Decoded* signal does not change its logic state when an SET takes place. This function uses the signals *Ndetect*, *Pdetect*, and its negated to work.

This simulation demonstrates the utility of using the coding properties of the CDC to have safe information. As predicted in the parasitics free simulations, the use of a decoder increases the range of action of the CDC. This simulation illustrates a hardening far beyond the other state of the art solutions, thanks to this encoding particularity. However a precision has to be made. This study covers only the encoding, and not the radiation hardening of the decoder itself. The idea is to place the decoder at the input of a self hardened C-element based memory cells like those from Devarapalli *et al* [DZHS10], Glorieux *et al* [GCG+13b] and Gang *et al* [CGG13].

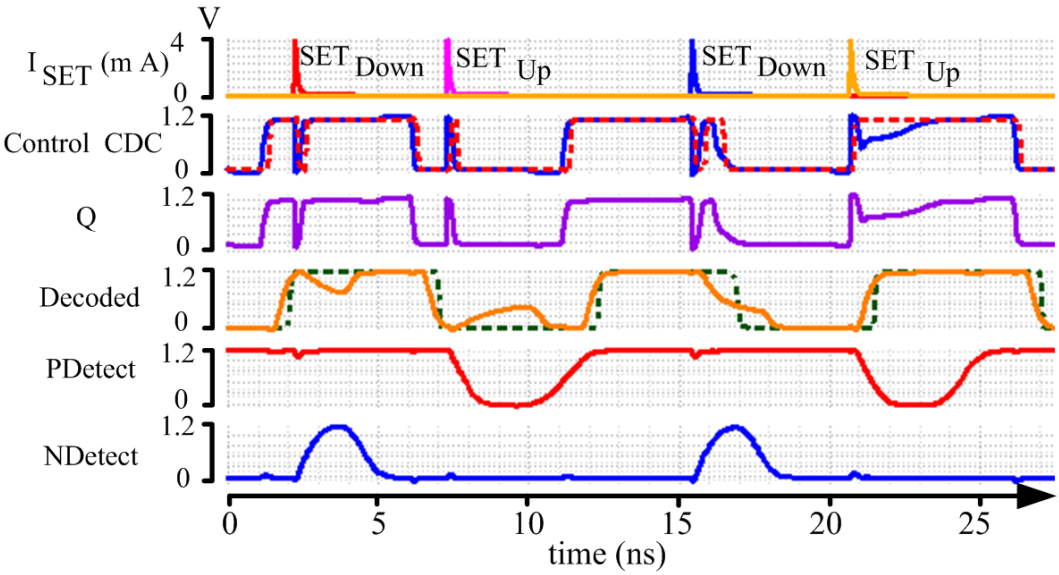


Figure 5.15: Simulation of the encoding and decoding capabilities of the couple CDC-decoder.

Now that a CDC layout has been chosen, thanks to its extracted layout performance, and its encoding property has been verified in the parasitics test bench, the performance of the CDC can be compared to that of the other filters with their extracted circuits.

5.4 Extracted CDC comparison with other SET filters

The parasitics extracted from the layout can modify the power consumption, critical charge of the circuits but also their propagation delay. This section will compare the electrical characteristics of the state of the art filters with the chosen extracted CDC. This will lead to the performance comparison using the metrics explained in Section 5.2.2. This section will end with a discussion on hardware redundancy

techniques and the CDC.

5.4.1 CHARACTERISTICS COMPARISON WITH THE OTHER SET FILTERS

Following the same methodology of analysis done in Section 5.2.1, the characteristics of the different filters in their layout's extracted versions is going to be compared using the tests benches with and without parasitics. The layout of each filter can be found in Appendix F. The comparison of the sensitive drain area and the area of the circuits is omitted because the sensitive drain area has not changed and the area of the CDC is considerably larger than any other SET filter's one because of the N-well enclosure. First the power consumption is analyzed, then the propagation delay, followed by the critical charge in inverted mode, and finally the CC in memory mode.

5.4.1.1 POWER CONSUMPTION COMPARISON

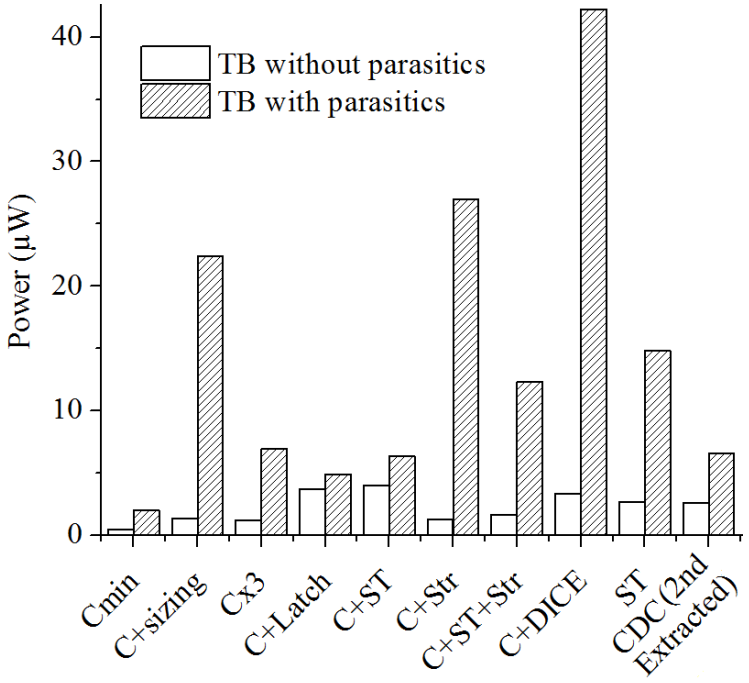


Figure 5.16: Comparison of the power consumption between the filters for the test benches with and without parasitics.

Figure 5.16 shows the difference of power consumption for the filters with the test benches with and without parasitics. In general, the power of the extracted

circuits is larger that determined with the parasitics free test bench. However, the sizing (C+sizing), the strengthening (C+Str) and the DICE (C+DICE) techniques have increased their power consumption significantly. Those layouts have large transistors, which enable a large flow of current, and make the power consumption increase. In the case of the DICE, an additional aspect makes its power increase. Its interlocked latch at the output adds complexity at the output, and this latch switches constantly generating a considerable power overhead in the extracted circuit. The extracted CDC keeps a reasonable power consumption as do the folding (Cx3), the latch (C+Latch) and the C-element with Schmitt trigger (C+ST). The last two are those whose power in the parasitic test bench are closer to that of the parasitics free test bench.

5.4.1.2 Propagation delay overhead comparison

The Schmitt trigger solution has the smallest propagation delay (*cf.* Figure 5.17) because it does not need to be preceded by a delay buffer (1 ns). The increase of delay in the test bench with parasitics in relation to the parasitics free one has its explanation on the increase of the charge capacitance at the output node and the parasitics associated to the switching time of its output latch. The filters with less delay overhead are the basic C-element filter (Cmin), the C-element with latch (C+Latch) and with Schmitt trigger capabilities (C+ST). The chosen CDC's extracted circuit keeps almost the same propagation delay as predicted with the parasitics free test bench. It has also about the same propagation delay as the fastest filters. The DICE technique requires the most propagation delay. The interlocked latch at the output adds around a nanosecond to the response of the circuit.

5.4.1.3 Critical charge comparison for the Inverter/Buffer mode

As far as the critical charge of the inverter/buffer mode is concerned, almost all the techniques took advantage of the increase of the output capacitance as can be observed in Figure 5.18. The less impressive increase is that of the C-element with latch (C+Latch). But definitely the technique that took the most advantage is the DICE. The critical charge in the parasitics test bench is 4 times larger than that of the parasitics free one. The propagation delay caused by the interlocked inverters prevents the propagation of an SET. The switching time is to slow for the rapid SET glitch to affect the output. This of course the frequency operation range of the DICE is more limited. Among the filters, only the folding technique (Cx3) can reach a slightly higher critical charge than the CDC.

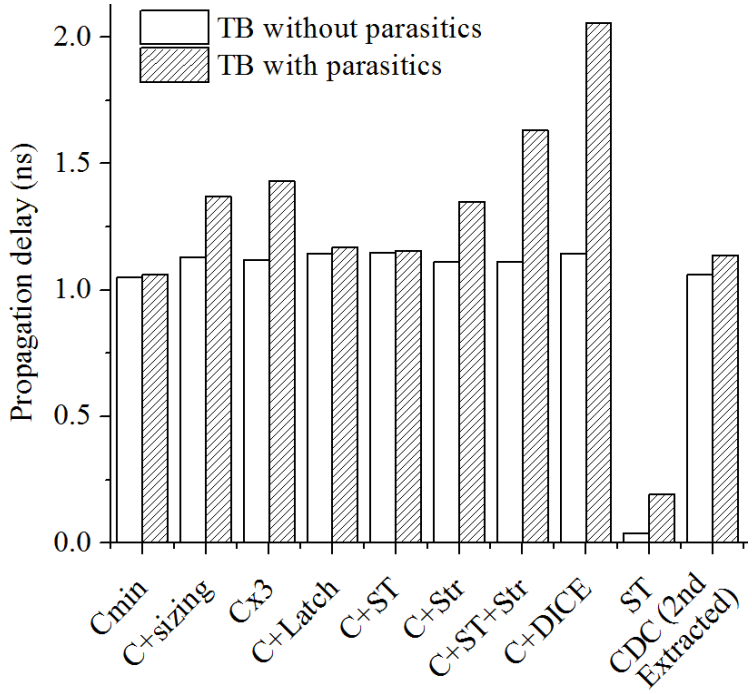


Figure 5.17: Comparison of the propagation delay between the filters for the test benches with and without parasitics.

5.4.1.4 CRITICAL CHARGE COMPARISON FOR THE MEMORY MODE

Finally, Figure 5.19 shows the critical charge for the memory mode. The remarkable increase of the DICE technique can be seen also for this mode. The value of the critical charge is maintained almost intact for the memory mode in relation to the buffer mode. Then follows the folding (cx3), the sizing (C+sizing), the combined strengthening with Schmitt trigger (C+Str+ST) and the extracted CDC. They have comparable critical charge in this mode but still are less robust than the DICE.

5.4.2 PERFORMANCE COMPARISON TO OTHER SET FILTERS

The CDC has its strong points in power consumption, small propagation delay and high critical charge for its inverter mode. In the previous analysis there is no consensus on which filter is the best. To position the CDC's performance in relation to the others, a comparison is made using the metrics used before in Section 5.2.2. This gives the performance relative to a possible application. This can give a better idea of the filters performance, because the constraints of power consumption, area, and latency vary with the application. For the clarity of the figure, only the filters that have the best performance in a metric or have a metric comparable to that of the CDC were taken into account. By comparison to the same figure but without parasitics of the circuits (*cf.* Chapter 4 Section 4.3.3 Figure 4.23), the DICE tech-

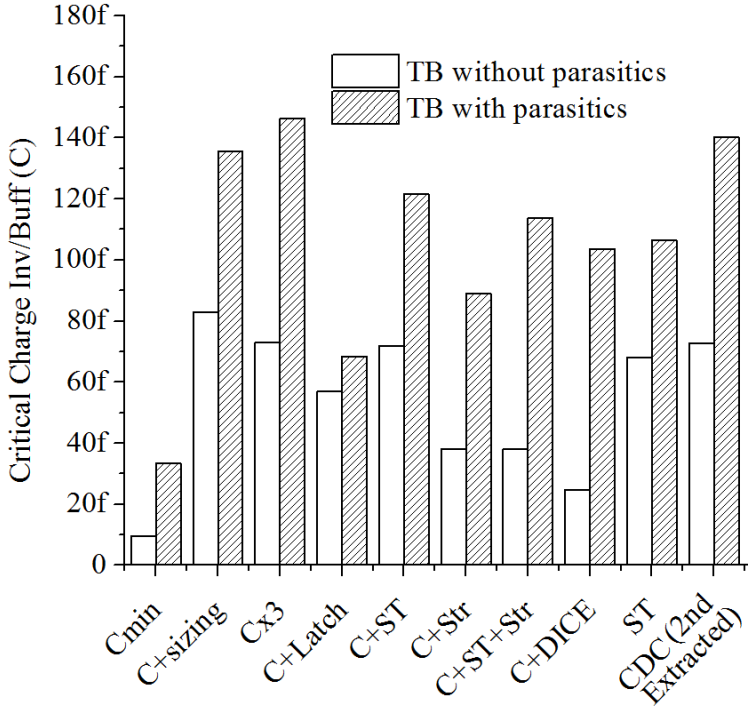


Figure 5.18: Comparison of the critical charge between the filters for the Inverter/Buffer mode for the test benches with and without parasitics.

nique was added.

The first remark concerns the A/SDA metric. Because of the large size, the CDC solution is the only that can reach such a gain. Of course this will be paid on the other metrics that depend on the circuit area. In terms of robustness and power for the inverter mode ($CC/P_{Inv/Buff}$) the folding and the CDC have comparable performance. The other solutions have a degradation of performance relative to the minimal C-element ($Cmin$). Continuing clockwise, in what has to be paid in the filter's propagation delay for robustness ($CC/PD_{Inv/Buff}$), the Schmitt trigger (ST) has no match because of his lack of delay buffer; its gain is up to 17. For the solutions that require this buffer, the CDC has a real advantage. In terms of $CC/A_{Inv/Buff}$ the sizing (C+Sizing) technique has the best performance in the inverter mode. Surprisingly, all the filters have comparable performance for what has to be paid in sensitive drain area ($CC/SDA_{Inv/Buff}$). The increase of the critical charge has placed almost every solution at the same level. But it should be pointed out that they are all less efficient than the minimal C-element for that metric.

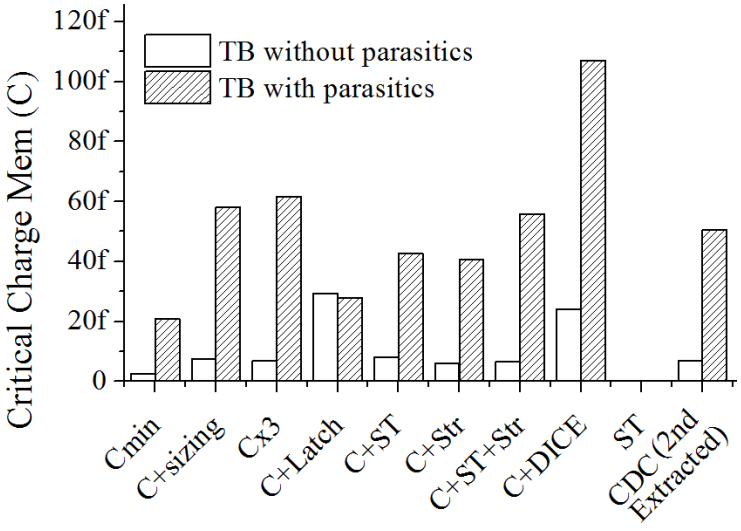


Figure 5.19: Comparison of the critical charge for memory mode between the filters for the test benches with and without parasitics.

As far as the metrics for the memory mode are concerned, the DICE has a predominant role in all of them except for the power and the propagation delay. For the delay (CC/PD_{Mem}) the DICE is followed by the CDC and for the power (CC/P_{Mem}) the advantage is for the minimal C-element. Among the hardening techniques only the CDC and the folding technique have the best efficiency.

In summary, the circuit with the best robustness in relation to the area is the sizing technique (C+sizing). In the memory mode the dominant technique is the DICE. The CDC is predominant for its small sensitive drain area, in relation to its whole area. It also has the best performance in relation to power and propagation delay for the inverter mode. In relation to the performances of the parasitics free (cf. Chapter 4 Section 4.3.4), the CDC maintained its dominance for the robustness in relation to power consumption($CC/P_{Inv/Buff}$) and the A/SDA ratio. It continues to have a comparable $CC/SDA_{Inv/Buff}$ to the other filters. The impact of the parasitic diode changes its dominance in the memory mode, and places the DICE solution in a better position. However, the extracted showed that the DICE solution has 1 ns more propagation delay than the CDC and this restricts the frequency response of the DICE solution.

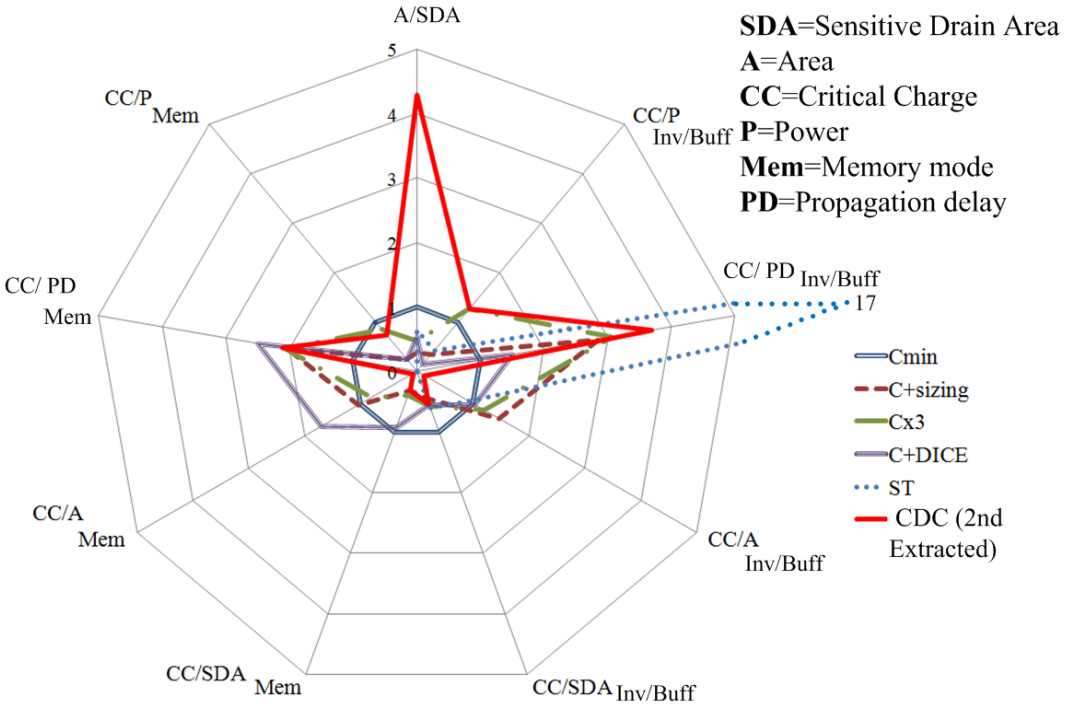


Figure 5.20: Performance metrics for the different hardening techniques based on their layout's extracted circuits.

5.4.3 CDC AND HARDWARE REDUNDANCY TECHNIQUES

The extracted CDC solution is more efficient for applications involving low power consumption, like the SAR ADC in the study case, and applications with a frequency of operation up to 442 MHz. This frequency is the limit where the memory mode lasts more than the inverter mode This is the frequency for two times the propagation delay of 1.13 ns. Also the total area of the CDC is 1% of that of the SAR ADC. Those characteristics match perfectly the low power and frequency (10 MHz) requirements of the SAR ADC application. A way to increase the frequency of operation, avoiding the delay buffer, can be a double redundancy (*e.g.* ECD) of the combinatorial function preceding the CDC, and use the CDC as a voter. In this case the area is sacrificed for the benefit of a much higher frequency of operation. That frequency could reach the order of GHz because the delay buffer is eliminated.

The area of the CDC is clearly larger than that of the other filters. Because of the size, that is larger than that of the CLK generator, it could be tempting to use hardware redundancy techniques instead of the CDC in this case. To put into

the context of the SAR ADC, the combinatorial function that is wanted to harden has an area of 66 μm^2 (*cf.* Appendix F.10) and the extracted consumes 21.2 μW. The selected CDC has an area of 105 μm^2 (*cf.* Appendix F.6), and the extracted model consumes 6.53 μW. The delay buffer that precedes the CDC adds an area of $4.5\mu m^2$ and consumes 9.53 μW. It is possible to compare the CDC solution to other redundancy techniques that require a significant area overhead like Error Correction using Duplication (ECD) and Triple Module Redundancy (TMR) (cf. Chapter 3 Section 3.3.3). Table 5.3 shows the overheads of area and power if hardware redundancy techniques were applied to harden the CLK generator function of the SAR ADC. The table shows the overheads if the CDC filter is applied directly to the CLK generator and if the duplication technique is associated with the CDC as voter.

Fonction	**CLK generator**	**TMR**	**ECD**	**CLK generator + CDC**	**ECD + CDC**
Area (μm^2)	66	201.2	135.2	175.5	237
Power (μW)	21.2	65.6	44.4	37.3	48.9

Table 5.3: Area and power comparison between the CDC filter and Triple Module Redundancy (TMR) and Error Correction using Duplication (ECD).

In terms of area, the CDC solution applied in the SAR ADC to harden the CLK generator has an area between that of ECD and TMR, but is the solution that consumes less power. The surface of the hardening with CDC is 12.8 % smaller than that of TMR, whereas it is 29.8 % larger than ECD. For the power consumption the solution with a CDC requires 46 % less power than TMR and 16.1 % less than ECD. Supposing another application does not allow the use of the delay buffer and requires a lower power consumption than TMR, a double redundancy (ECD) coupled with a CDC can be a solution. In this case the area will be 17.8 % larger than TMR, but the power consumption will be 25.4 % smaller than TMR. It will consume almost the same amount of power as an ECD technique, but the voter will be hardened and the information can be encoded for further hardening.

This modularity of the CDC architecture makes possible to couple the BICS and the feedback transistors to other architectures of filters to increase the critical charge. It can be easily done with the folding technique for example. In addition to this flexibility the decoding capability can be taken into account.

5.5 Conclusions

In this chapter the silicon implementation is considered. The CDC layout implementation needs isolated wells to sense effectively the NMOS and PMOS transistors of the C-element. Even if the wells are put together, the area of the circuit increases relative to that initially predicted. However, in terms of power consumption and latency the CDC proved its strong points against the other state of the art filters. It has to be noted that further improvements on the layout can increase even more the critical charge. If the feedback response is accelerated the self healing recovers more quickly the C-element from an SET. The layout's first extracted circuit showed that parasitic phenomena have an impact on the circuit's performance. The parasitics phenomena are caused by the capacitances between every metal wire and other metals as well as between the metal and the substrate. Resistances created by the contact via size, the polysilicon gates, and the length/width of wires contributes to the parasitics phenomena. Layout improvements showed an increase of the extracted circuit's performance, but without reaching that of the parasitic free CDC. However, between three extracted circuits related to layouts designs, the 2nd extracted circuit was chosen for having the best performance with less area. The speed factor is of course limited by the parasitics linked to the technology. As the CMOS technology shrinks and the switching times accelerate the CDC architecture can also gain in speed of feedback response. The sensitive drain surface of this solution represents only 1% of the total CDC layout surface. The CDC solution has equal performance with the folding (Cx3) in terms of robustness in relation to the power consumption (CC/P). This parameter is three times more significant for the inverter mode than the other techniques. Another improvement to the single CDC was the couple CDC-decoder that proved a significant increase of the hardening. This requires including the decoder logic in a memorization module after the CDC. The layout implementation required more area than expected, but this does not prove to be problematic for the hardening of the CLK generator of the SAR ADC compared to the size of the converter. The modularity of the CDC solution can be applied to double or triple modular redundancies to eliminate the delay buffer if needed. It can also be applied to other SET filters like the one using folding to increase the critical charge.

Conclusion

The purpose of this work is to answer the question *who guards the guardians?* in the context of what happens if the radiation hardening by design fails in a circuit because of an SET. To reach an answer to that question the bases for the research had to be set in Chapter 1. The cosmic origin of the ionization impacts was explained. Then it was shown that the main issue in transistors is the parasitic current between the bulk and the drain of a transistor that causes a change of logic state after an ion strike. That parasitic current can generate hard errors, soft errors and degradation of transistors in time. So this current is the major concern. To understand and simulate how a transistor is affected by this current a model was made using the collecting charge model. This model provided a physical and geometrical approach to an electrical simulation in CADENCE.

With the primary bases set, the next step was to choose a case study to understand the behavior of soft error sensitivity in a complex system. This was done in Chapter 2. A SAR ADC was chosen for its multiplicity of circuits (analog, synchronous and asynchronous digital). From this system a particular combinatorial function was found critical and was chosen to be hardened. After a critical charge, geometrical and temporal sensitivity study using the collecting charge model several conclusions were reached. The first was that the structure of a combinatorial function is linked to the circuit's sensitivity. The parallelism of transistors decreases the sensitivity, while the serialization increases it. The second is that, from a geometrical point of view, the sensitive area of the circuit varies depending on the logic state. The most sensitive state is when the output is "1". The final conclusion is that temporarily a transition to "1" is much more sensitive and is more likely to generate SETs that can become SEUs in the memory register of the SAR ADC. Those sensitivity aspects showed that it would be easier to implement a hardening out of the function. Otherwise the function would have to be redesigned. Placing the hardening outside the function helps to harden all the states all the time. Also, the sensitive areas of the hardening wont be near the sensitive areas of the function. Moreover, given the context of the low power ADC and lowering the cost of the

hardening, the solution would have to balance low power, small area overhead and a low propagation delay overhead. This work was published as a conference paper for the IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS) in August 2013 [GTSAJ13].

An extensive state of the art was built in Chapter 3 to determine the technique that would fit the requirements of area, propagation delay and power stated before. Additionally, the context required a hardening strategy against soft errors at a lower cost than the technological hardening ones. A hardening strategy called temporal filtering seems to fit most of the criteria. A temporal filter (or also SET filter) is placed after a combinatorial function and before a memory element. It is composed of a delay buffer that precedes a two input voter. The voter decides between the delayed and non delayed input using a C-element. With its low number of elements the probability of ionizing hit is lower than if the filter was more complex. This element has the property to have an inverter mode when the inputs are the same, and a memory mode when they are different to keep the last output. This stops the propagation of soft errors. This technique requires a small area, it is very power efficient and only requires a certain propagation delay. It is also easy to implement. The only problem that remains is that it is not self hardened.

Chapter 4 presents the architecture of the SET filter with C-element with Detection and Correction (CDC). The proposed solution has an innovative architecture, which hardens the C-element of the filter by using BICS (Built-In Current Sensors) to detect that an impact took place. Then the sensor will engage a feedback compensation to recover the right logic state, by activating what are called feedback transistors. Finally, the sensors will indicate through two outputs if either the NMOS or the PMOS transistors were hit (or both). Those outputs, in addition to the output of the C-element, can encode the information in real-time, and in case of error the information can be recovered thanks to a decoder. Electrical simulations demonstrated the filtering, the self-healing and the encoding properties. Then a comparison to other state of the art temporal filters was done to show the strong points of this technique, which are the elevated critical charge, the low power consumption and a small area of sensitive drains relative to the area of the CDC. In addition, it proved to be strong for the memory mode above the other state of the art SET filtering solutions. This work was published in the IEEE Transactions on Circuits and Systems II: Express Briefs in September 2014 [GTASJ14].

With the architecture of CDC being defined and verified by simulation, a study of feasibility was done in Chapter 5. The layout implementation showed the need of a deep N-well to isolate the NMOS transistors from the whole P-substrate. The layout's parasitic extraction also showed that parasitics phenomena have an impact

on the circuit's performance but with small changes the CDC was enhanced. A study of the parasitics impacts on the extracted circuits of different layouts helped to determine the most appropriate one. This selected circuit proved to have low power and propagation delay overhead and also proved its efficiency on those aspects against the other state of the art filters. A final enhancement is the coupling with the decoder logic that can be placed as the input of a hardened memory element. The coding and decoding of information increases the robustness by stopping eventual SET propagation, in case of a very energetic ion strike on the CDC.

As far as the hardening of the CLK generator within the SAR ADC is concerned, the CDC filter also proved to be less power consuming than the hardware redundancy techniques for this specific case. The modularity of the CDC solution proved its adaptability to the needs of different applications since it can be applied to double or triple modular redundancies to eliminate the delay buffer if needed. It can also be applied to other SET filters like the one using folding to increase the critical charge.

Further work can follow two main research axes: design and implementation. There are three main tasks when designing a CDC. The first is considering the CDC as a dynamical system with feedback to establish a transfer function for a mathematical model. This will help to optimize the action of the CDC depending on the load and the parasitic SET current. This can also help to fix the transistor sizes for a rapid response. The other design task is to implement a layout using more recent CMOS technology such as the SOI 28 nm from ST Microelectronics. This technology is directly being manufactured only in SOI. Using this technology the CDC can benefit from the small scale and the switching time but also from the SOI structure. With the SOI technology, the transistors are isolated from the bulk thanks to an oxide layer, and this can probably eliminate the deep N-well reducing considerably the circuit area. Also, it is expected that SOI catches up with the price of bulk CMOS for 28 nm and subsequent technologies so SOI technology can be more affordable [Jon12]. The last design task is to see the applicability of the CDC structure in memory elements to detect and recover in-situ the information if a soft error occurs.

The other axis is more linked to the silicon implementation of the CDC. The first one is to analyze the sensitive area (or cross section) of the CDC. This can be done by simulation using cross section prediction software like technology CAD (TCAD) based software such as Cogenda, Synopsys Sentaurus, Silvanco or TFIT from Irochtech. The cross section can also be analyzed in laboratory with soft error testing facilities using laser testing or particle accelerator testing. And of course the final work is to have the CDC implemented on silicon in a system for hardening.

This requires the design of the input/output ring for the integrated circuit and the manufacturing so the CDC can be physically tested.

Contributions to the literature

Conference papers

Daniel Gomez Toro, Fabrice Seguin, Matthieu Arzel, and Michel Jezequel. Study of a cosmic ray impact on combinatorial logic circuits of an 8bit SAR ADC in 65nm CMOS technology. In 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), pages 241–244, August 2013.

Journal papers

Daniel Gomez Toro, Matthieu Arzel, Fabrice Seguin, and Michel Jezequel. Soft error detection and correction technique for radiation hardening based on c-element and BICS. IEEE Transactions on Circuits and Systems II: Express Briefs, September 2014.

P. Adde, D. Gomez Toro, and C. Jego. Design of an efficient maximun likelihood soft decoder for systematic short block codes. , IEEE Transactions on Signal Processing, PP(99):1, 2012.

Appendices

Chapter A
Mobilities based on Massetti et al model

The mobilities can be obtained by the Equations A.1 and A.2 [MSS83]. N/P_{doping} represent the concentration of the doping element in cm^{-3}. The curves of mobility for electrons and holes are represented in Figure A.1.

For Arsenic and Phosphorus doping:

$$\mu = \mu_0 + \frac{\mu_{max} - \mu_0}{1 + \left(\frac{N_{doping}}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_{doping}}\right)^{\beta}} \text{ in } (cm^2.V^{-1}.s{-}1) \tag{A.1}$$

For Boron:

$$\mu = \mu_0 \exp\left(\frac{-p_c}{P_{doping}}\right) + \frac{\mu_{max} - \mu_0}{1 + \left(\frac{P_{doping}}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{P_{doping}}\right)^{\beta}} \text{ in } (cm^2.V^{-1}.s{-}1) \tag{A.2}$$

Parameters	Arsenic	Phosphorus	Boron
$\mu_0(cm^2.V^{-1}.s^{-1})$	52.2	68.5	44.9
$\mu_{max}(cm^2.V^{-1}.s^{-1})$	1417	1414	470.5
$\mu_1(cm^2.V^{-1}.s^{-1})$	43.4	56.1	29.0
$C_r(cm^{-3})$	9.68×10^{16}	9.20×10^{16}	2.23×10^{17}
$C_s(cm^{-3})$	3.43×10^{20}	3.41×10^{20}	6.10×10^{20}
α	0.68	0.711	0.719
β	2.00	1.98	2.00
p_c	-	-	9.23×10^{16}

Table A.1: Fitting parameters for Equations A.1 and A.2 [MSS83]

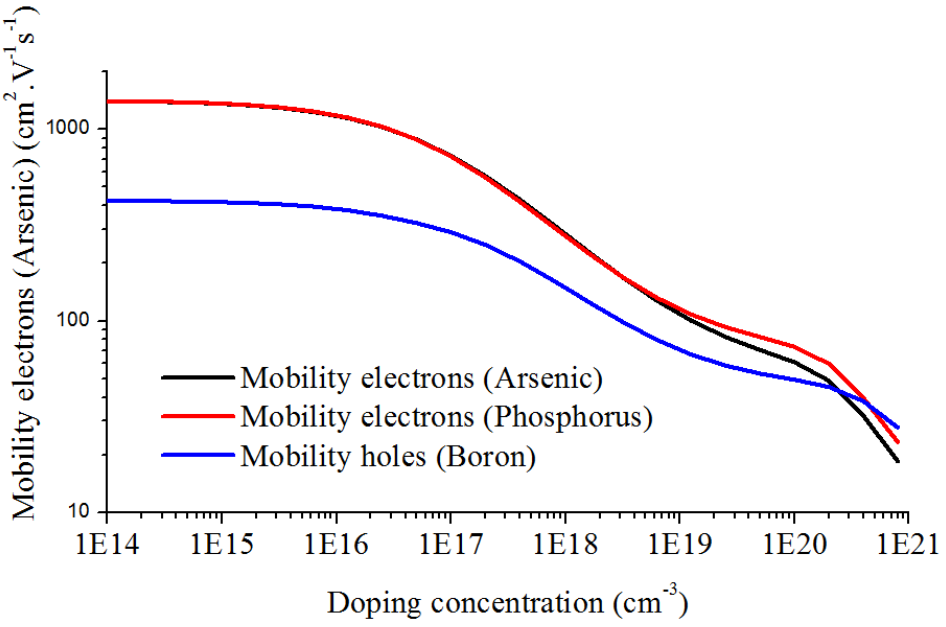


Figure A.1: Mobilities of electrons and holes for the variation of concentration of doping with Arsenic, Phosphorus and Boron at 300K.

Chapter B

Solution to N(l,t)

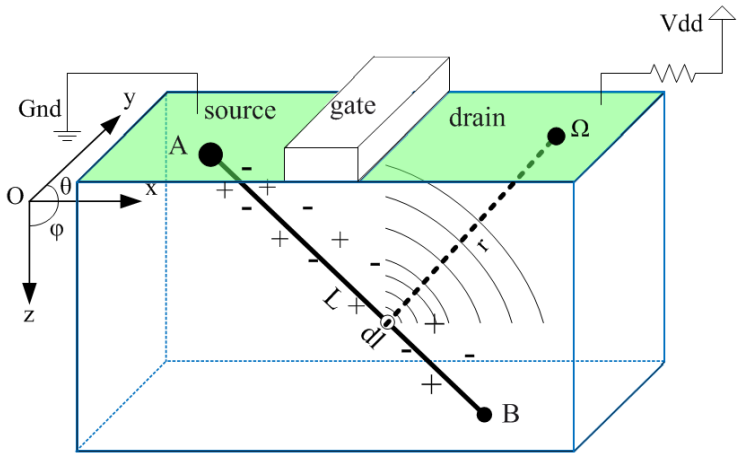


Figure B.1: Charges diffusing from an ion track to the drain.

For the integral , the segment AB has to be set with A and B defined with coordinates (x_A, y_A, z_A) and (x_B, y_B, z_B).

$$N(t) = \int_A^B N_0 \frac{exp\left(\frac{-r(l)^2}{4.D.t} - \frac{t}{\tau}\right)}{(4.\pi.D.t)^{\frac{3}{2}}} dl \ (cm^{-3}) \tag{B.1}$$

Since the ionization phenomenon has a vertical component (excepting a perfectly horizontal strike), the parametrization of the AB segment will use a λ parameter.

$$\begin{cases} x = a \times \lambda + b, & \text{with } a = \dfrac{x_B - x_A}{z_B - z_A},\ b = x_A - z_A \times a \\ y = c \times \lambda + d, & \text{with } c = \dfrac{y_B - y_A}{z_B - z_A},\ d = y_A - z_A \times c \\ z = \lambda, & z_A \leq \lambda \leq z_B \end{cases} \tag{B.2}$$

Thus:

$\frac{dl}{d\lambda} = \sqrt{\left(\frac{dx}{d\lambda}\right)^2 + \left(\frac{dy}{d\lambda}\right)^2 + \left(\frac{dy}{d\lambda}\right)^2}$
that is:

$dl = d\lambda \times \sqrt{\left(\frac{dx}{d\lambda}\right)^2 + \left(\frac{dy}{d\lambda}\right)^2 + \left(\frac{dy}{d\lambda}\right)^2}$
using x, y and z definitions in B.2:

$dl = d\lambda \times \sqrt{1 + a^2 + c^2}$

r has to be set as a function of the AB segment because it changes with the trajectory L. r can be defined from a point (x,y,z) in the AB segment to the Ω point with coordinates $(x_\Omega, y_\Omega, z_\Omega)$. First is presented the parametrization for the normal case and then for the horizontal case:

r is defined as:

$$r = \sqrt{(x - x_\Omega)^2 + (y - y_\Omega)^2 + (z - z_\Omega)^2} \tag{B.3}$$

replacing x,y and z by the parameter λ:

$$r(\lambda) = \sqrt{(a\lambda + b - x_\Omega)^2 + (c\lambda + d - y_\Omega)^2 + (\lambda - z_\Omega)^2}$$

Developing the expression:

$$r(\lambda)^2 = \lambda^2 a^2 + \lambda 2a(b - x_\Omega) + (b - x_\Omega)^2 + \lambda^2 c^2 + \lambda 2c(d - y_\Omega) + (d - y_\Omega)^2 + \lambda^2 - \lambda 2z_\Omega + z_\Omega^2$$

Reorganizing:

$$r(\lambda)^2 = \lambda^2(a^2 + c^2 + 1) + \lambda 2(a(b - x_\Omega) + c(d - y_\Omega) - z_\Omega) + (b - x_\Omega)^2 + (d - y_\Omega)^2 + z_\Omega^2$$

To simplify the writing:

$\alpha = a^2 + c^2 + 1$
$\beta = 2(a(b - x_\Omega) + c(d - y_\Omega) - z_\Omega)$
$\gamma = (b - x_\Omega)^2 + (d - y_\Omega)^2 + z_\Omega^2$

Finally:

$$r(\lambda)^2 = \lambda^2\alpha + \lambda\beta + \gamma \text{ and } dl = d\lambda\sqrt{\alpha} \tag{B.4}$$

In order to avoid indetermination when the AB segment is horizontal($z_A = z_B$), the parametrization has 2 cases:

Parametrization if: $x_A \neq x_B$ and $z_A = z_B$

$$\begin{cases} x = \lambda, & x_A \leq \lambda \leq x_B \\ y = a \times \lambda + b, & \text{with } a = \dfrac{y_B - y_A}{x_B - x_A},\ b = y_A - x_A \times a \\ z = z_A \end{cases} \tag{B.5}$$

In this case we have:

$\alpha = 1 + a^2$
$\beta = 2(a(b - y_\Omega) - x_\Omega)$
$\gamma = x_\Omega^2 + (b - y_\Omega)^2 + (z_A - z_\Omega)^2$

And if $x_A = x_B;\ y_A \neq y_B\ ;\ z_A = z_B$

$$\begin{cases} x = x_A \\ y = \lambda, & y_A \leq \lambda \leq y_B \\ z = z_A \end{cases} \tag{B.6}$$

In this case we have:

$\alpha = 1$
$\beta = -2y_\Omega$
$\gamma = (x_A - x_\Omega)^2 + y_\Omega^2 + (z_A - z_\Omega)^2$

In order to simplify the integral, $r(\lambda)^2$ can be expressed like a perfect square polynomial:

$$r(\lambda)^2 = \lambda^2\alpha + \lambda\beta + \gamma = \alpha(\lambda - H)^2 + K, \text{ with } H = \frac{-\beta}{2\alpha} \text{ and } K = \alpha H^2 + \beta H + \gamma \tag{B.7}$$

Now, returning to the first parametrization situation (*c.f.* B.2) if r^2 is replaced, the integral is:

$$N(t) = \int_{z_A}^{z_B} N_0\sqrt{\alpha}\frac{exp\left(-\frac{\alpha(\lambda - H)^2 + K}{4.D.t} - \frac{t}{\tau}\right)}{(4.\pi.D.t)^{\frac{3}{2}}}d\lambda \tag{B.8}$$

The integral is set from z_A to z_B. This corresponds to an incident particle with a trajectory angle other than 0° with respect to the horizontal. This case covers most of the situations.

$$N(t) = \frac{N_0\sqrt{\alpha}}{(4.\pi.D.t)^{\frac{3}{2}}} exp\left(-\frac{t}{\tau} - \frac{K}{4.D.t}\right) \int_{z_A}^{z_B} exp\left(-\frac{\alpha(\lambda - H)^2}{4.D.t}\right) d\lambda \tag{B.9}$$

Concentrating on the integral, a variable change can be done:

$$I = \int_{\mu(A)}^{\mu(B)} \sqrt{\frac{4Dt}{\alpha}} exp\left(-\mu^2\right) d\mu \text{ with } \mu(\lambda) = \frac{\lambda - H}{\sqrt{\frac{4Dt}{\alpha}}} \text{ and } d\mu = \frac{1}{\sqrt{\frac{4Dt}{\alpha}}} d\lambda \tag{B.10}$$

$$I = \int_{\mu(A)}^{\mu(B)} \sqrt{\frac{4Dt}{\alpha}} \times \frac{\sqrt{\pi}}{2} \times \frac{2}{\sqrt{\pi}} exp\left(-\mu^2\right) d\mu \tag{B.11}$$

In addition, it is known that:

$$\int_a^b exp(-x^2)dx = \frac{\sqrt{\pi}}{2} \times (erf(b) - erf(a)) \tag{B.12}$$

The integral I is:

$$I = \sqrt{\frac{4Dt}{\alpha}} \times \frac{\sqrt{\pi}}{2} \times (erf(\mu(B)) - erf(\mu(A))) \tag{B.13}$$

And finally the diffusion equation as a function of time t and a point $\Omega(x_\Omega, y_\Omega, z_\Omega)$:

$$N(t,\Omega) = \frac{N_0\sqrt{\alpha}}{(4.\pi.D.t)^{\frac{3}{2}}} exp\left(-\frac{t}{\tau} - \frac{K}{4.D.t}\right) \sqrt{\frac{4Dt}{\alpha}} \times \frac{\sqrt{\pi}}{2} \times \left(erf\left(\frac{z_B - H}{\sqrt{\frac{4Dt}{\alpha}}}\right) - erf\left(\frac{z_A - H}{\sqrt{\frac{4Dt}{\alpha}}}\right)\right) \tag{B.14}$$

And simplifying:

$$N(t,\Omega) = \frac{N_0}{8.\pi.D.t} exp\left(-\frac{t}{\tau} - \frac{K}{4.D.t}\right) \left(erf\left(\frac{z_B - H}{\sqrt{\frac{4Dt}{\alpha}}}\right) - erf\left(\frac{z_A - H}{\sqrt{\frac{4Dt}{\alpha}}}\right)\right) \tag{B.15}$$

Chapter C

Solution to N(l,t) in polar coordinates

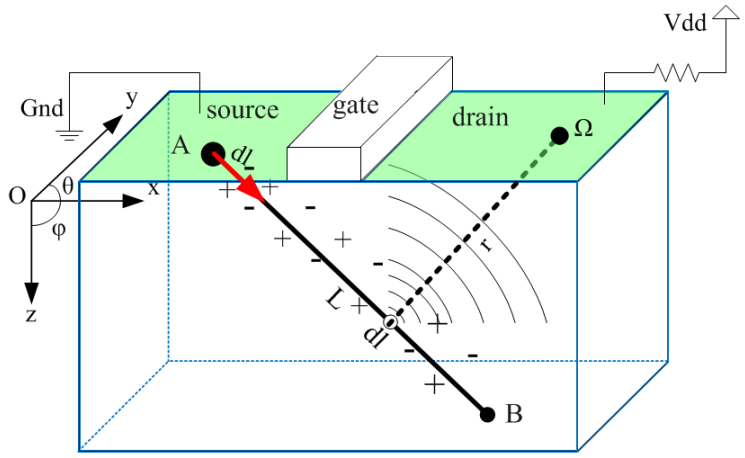


Figure C.1: Charges diffusing from an ion track to the drain.

For the integral , the segment AB has to be set with A and B defined with coordinates (x_A, y_A, z_A) and (x_B, y_B, z_B).

$$N(t) = \int_0^L N_0 \frac{exp\left(\frac{-r(l)^2}{4.D.t} - \frac{t}{\tau}\right)}{(4.\pi.D.t)^{\frac{3}{2}}} dl \tag{C.1}$$

The parametrization of the AB segment will use a l parameter. Let be θ the azimuthal angle of trace in the XY plane from the X axis to the Y axis; and φ the azimuthal angle of trace in the XZ plane from the Z axis to the X axis. A point of the AB trace has coordinates (x_i, y_i, z_i) defined as:

$$\begin{cases} x_i = lsin(\varphi)cos(\theta) + x_A, & \text{with } 0 \leqslant l \leqslant L \\ y_i = lsin(\varphi)sin(\theta) + y_A \\ z_i = lcos(\varphi) + z_A \end{cases} \tag{C.2}$$

r has to be set as a function of the AB segment because it changes with the trajectory L. r can be defined from a point (x_i, y_i, z_i) in the AB segment to the Ω point with coordinates $(x_\Omega, y_\Omega, z_\Omega)$.

r is defined as:

$$r(l) = \sqrt{(x_i - x_\Omega)^2 + (y_i - y_\Omega)^2 + (z_i - z_\Omega)^2} \tag{C.3}$$

replacing x_i, y_i and y_i by their equivalent:

$$r(l) = \sqrt{(lsin(\varphi)cos(\theta) + x_A - x_\Omega)^2 + (lsin(\varphi)sin(\theta) + y_A - y_\Omega)^2 + (lcos(\varphi) + z_A - z_\Omega)^2}$$

Developing the expression:

$$r(l)^2 = l^2\left(sin^2(\varphi)\left(cos^2(\theta) + sin^2(\theta)\right) + cos^2(\varphi)\right) + 2lsin(\varphi)cos(\theta)(x_A - x_\Omega) + 2lsin(\varphi)sin(\theta)(y_A - y_\Omega) + 2lcos(\varphi)(z_A - z_\Omega) + (x_A - x_\Omega)^2 + (y_A - y_\Omega)^2 + (z_A - z_\Omega)^2$$

To simplify the writing:

$$\alpha = \left(sin^2(\varphi)\left(cos^2(\theta) + sin^2(\theta)\right) + cos^2(\varphi)\right) = 1$$
$$\beta = 2lsin(\varphi)cos(\theta)(x_A - x_\Omega) + 2lsin(\varphi)sin(\theta)(y_A - y_\Omega) + 2lcos(\varphi)(z_A - z_\Omega)$$
$$\gamma = (x_A - x_\Omega)^2 + (y_A - y_\Omega)^2 + (z_A - z_\Omega)^2$$

Finally:

$$r(l)^2 = l^2\alpha + l\beta + \gamma \tag{C.4}$$

In order to simplify the integral, $r(l)^2$ can be expressed like a perfect square polynomial:

$$r(l)^2 = l^2\alpha + l\beta + \gamma = \alpha(l - H)^2 + K, \text{ with } H = \frac{-\beta}{2\alpha} \text{ and } K = \alpha H^2 + \beta H + \gamma \tag{C.5}$$

Now, if $r(l)^2$ is replaced, the integral is:

$$N(t) = \int_0^L N_0 \frac{exp\left(-\frac{\alpha(\lambda - H)^2 + K}{4.D.t} - \frac{t}{\tau}\right)}{(4.\pi.D.t)^{\frac{3}{2}}} dl \tag{C.6}$$

$$N(t) = \frac{N_0}{(4.\pi.D.t)^{\frac{3}{2}}} exp\left(-\frac{t}{\tau} - \frac{K}{4.D.t}\right) \int_0^L exp\left(-\frac{\alpha(\lambda - H)^2}{4.D.t}\right) d\lambda \tag{C.7}$$

Concentrating on the integral, a variable change can be done:

$$I = \int_{\mu(0)}^{\mu(L)} \sqrt{\frac{4Dt}{\alpha}} exp\left(-\mu^2\right) d\mu \text{ with } \mu(\lambda) = \frac{\lambda - H}{\sqrt{\frac{4Dt}{\alpha}}} \text{ and } d\mu = \frac{1}{\sqrt{\frac{4Dt}{\alpha}}} d\lambda \tag{C.8}$$

$$I = \int_{\mu(0)}^{\mu(L)} \sqrt{\frac{4Dt}{\alpha}} \times \frac{\sqrt{\pi}}{2} \times \frac{2}{\sqrt{\pi}} exp\left(-\mu^2\right) d\mu \tag{C.9}$$

In addition, it is known that:

$$\int_a^b exp(-x^2)dx = \frac{\sqrt{\pi}}{2} \times (erf(b) - erf(a)) \tag{C.10}$$

The integral I is:

$$I = \sqrt{\frac{4Dt}{\alpha}} \times \frac{\sqrt{\pi}}{2} \times (erf(\mu(B)) - erf(\mu(A))) \tag{C.11}$$

And finally the diffusion equation as a function of time t and a point $\Omega(x_\Omega, y_\Omega, z_\Omega)$:

$$N(t,\Omega) = \frac{N_0}{(4.\pi.D.t)^{\frac{3}{2}}} exp\left(-\frac{t}{\tau} - \frac{K}{4.D.t}\right) \sqrt{\frac{4Dt}{\alpha}} \times \frac{\sqrt{\pi}}{2} \times \left(erf\left(\frac{L - H}{\sqrt{\frac{4Dt}{\alpha}}}\right) - erf\left(\frac{0 - H}{\sqrt{\frac{4Dt}{\alpha}}}\right)\right) \tag{C.12}$$

Simplifying and replacing α by its value 1:

$$N(t,\Omega) = \frac{N_0}{8.\pi.D.t} exp\left(-\frac{t}{\tau} - \frac{K}{4.D.t}\right) \left(erf\left(\frac{L - H}{\sqrt{4Dt}}\right) - erf\left(\frac{-H}{\sqrt{4Dt}}\right)\right) \tag{C.13}$$

Chapter D
Demonstration Autran

Pour résoudre l'integrale et l'amener à ressembler à l'integrale de $exp(-x^2)$ on passe par l'expression d'un polynome parfait au carré.

$$r(l)^2 = l^2\alpha + l\beta + \gamma = \alpha(l-P)^2 + Q, \text{ avec } P = \frac{-\beta}{2\alpha} \text{ et } Q = \alpha P^2 + \beta P + \gamma \quad \text{(D.1)}$$

dans ce cas: $r(\eta)^2 = \eta^2 + K\eta + l_0^2$

$r(\eta)^2 = (\eta - P)^2 + Q$ avec $P = -K/2$ et $Q = P^2 + KP + l_0^2$
d'où $r(\eta)^2 = (\eta - \frac{-K}{2})^2 + \left(\frac{-K}{2}\right)^2 + K\frac{-K}{2} + l_0^2 = (\eta + \frac{K}{2})^2 + \frac{K^2}{4} + \frac{-K^2}{2} + l_0^2$
$r(\eta)^2 = (\eta + \frac{K}{2})^2 - \frac{K^2}{4} + l_0^2$

du coup si j'introduis cela dans lintégrale:

$$N(t) = \int_0^L N_0 \frac{exp\left(-\frac{r(\eta)^2}{4.D.t} - \frac{t}{\tau}\right)}{(4.\pi.D.t)^{\frac{3}{2}}} d\eta = \int_0^L N_0 \frac{exp\left(-\frac{(\eta+\frac{K}{2})^2 - \frac{K^2}{4} + l_0^2}{4.D.t} - \frac{t}{\tau}\right)}{(4.\pi.D.t)^{\frac{3}{2}}} d\eta \quad \text{(D.2)}$$

$$N(t) = \frac{N_0}{(4.\pi.D.t)^{\frac{3}{2}}} \times exp\left(-\frac{t}{\tau}\right) \times exp\left(-\frac{-\frac{K^2}{4} + l_0^2}{4.D.t}\right) \times \int_0^L exp\left(\frac{(\eta + \frac{K}{2})^2}{4.D.t}\right) d\eta \quad \text{(D.3)}$$

$$N(t) = \frac{N_0}{(4.\pi.D.t)^{\frac{3}{2}}} exp\left(-\frac{t}{\tau}\right) exp\left(-\frac{l_0^2}{4.D.t}\right) exp\left(\frac{K^2}{16.D.t}\right) \int_0^L exp\left(\frac{(\eta + \frac{K}{2})^2}{4.D.t}\right) d\eta \quad \text{(D.4)}$$

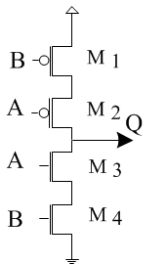
$$N(t) = \frac{N_0}{8.\pi.D.t} exp\left(-\frac{t}{\tau}\right) exp\left(-\frac{l_0^2}{4.D.t}\right) exp\left(\frac{K^2}{16.D.t}\right) \left[erf\left(\frac{L + \frac{K}{2}}{\sqrt{4.D.t}}\right) - erf\left(\frac{0 + \frac{K}{2}}{\sqrt{4.D.t}}\right)\right] \quad \text{(D.5)}$$

Chapter E

Transistor sizes of the SET filters

The following figures indicate the sizes or the transistors used for each filter.

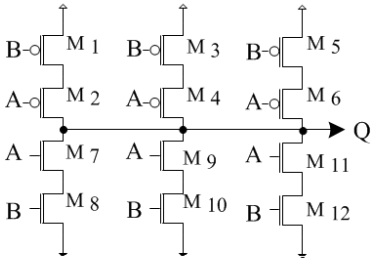
C-element (Cmin and C+ Sizing)



Sizes in µm
Cmin:
$M_{1,2}$: 0.54/0.06
$M_{3,4}$: 0.135 /0.06

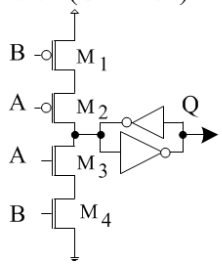
C+Sizing:
$M_{1,2}$: 4/0.06
$M_{3,4}$: 2/0.06

C-element Folding (Cx3)



Sizes in µm
$M_{1\text{ to }6}$: 1.14/0.06
$M_{7\text{ to }12}$: 0.57/0.06

C-element with latch (C+Latch)

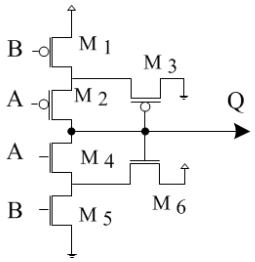


Sizes in µm
$M_{1,2}$: 2.4/0.06
$M_{3,4}$: 1.4/0.06

Small inverter:
NMOS : 0.8/0.06
PMOS : 0.4/0.06

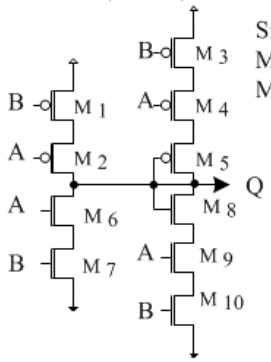
Large inverter:
NMOS : 1.8/0.06
PMOS : 0.9/0.06

C-element-Schmitt trigger (C+ST)



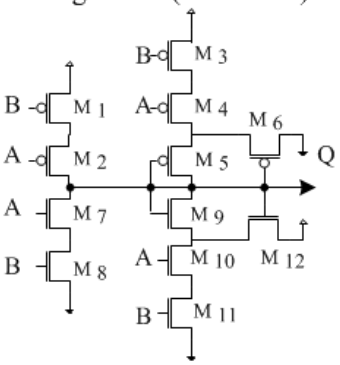
Sizes in µm
$M_{1\text{ to }3}$: 3.4/0.06
$M_{4\text{ to }6}$: 1.7/0.06

C-element Strengthened
(C+Srt)



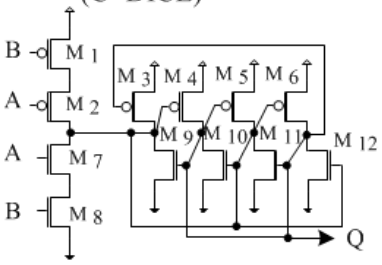
Sizes in µm
$M_{1\text{ to }5}$: 1.66/0.06
$M_{6\text{ to }10}$: 0.83/0.06

C-element-Schmitt trigger
Strengthened (C+ST+Str)



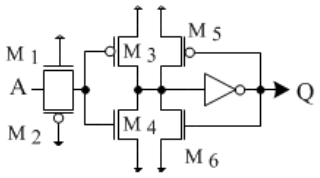
Sizes in µm
$M_{1\text{ to }6}$: 1.66/0.06
$M_{7\text{ to }12}$: 0.83/0.06

C-element with DICE
(C+DICE)



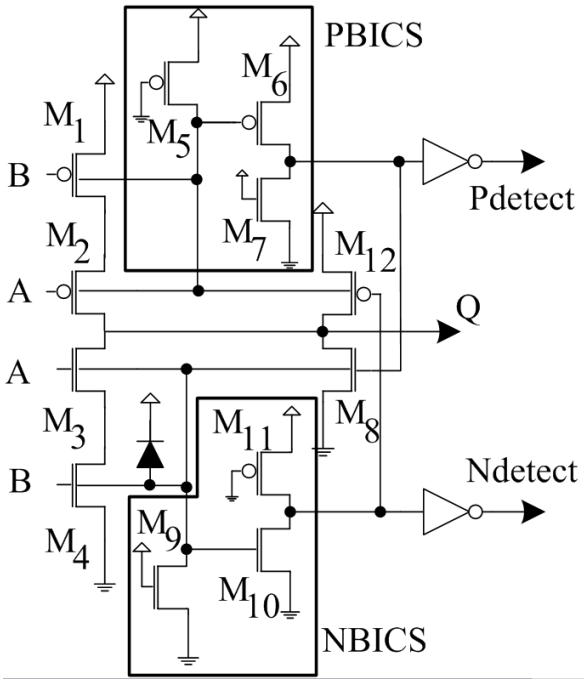
Sizes in µm
$M_{1,2}$: 1.4/0.06
$M_{3,4}$: 1/0.06
$M_{3\text{ to }6}$: 0.27/0.06
$M_{9\text{ to }12}$: 0.135/0.06

Schmitt Trigger (ST)



Sizes in µm
$M_{1,4}$: 1.2/0.06
$M_{2,4}$: 2.2/0.06
M_5 : 0.27/0.7
M_6 : 0.135/0.06

Inverter:
NMOS : 2.2/0.06
PMOS : 1.2/0.06



Transistor	3nd Extracted
M1	2.5/0.06
M2	2.5/0.06
M3	2/0.06
M4	2/0.06
M5	0.5/1.4
M6	3.6/0.06
M7	0.4/0.1
M8	0.6/0.06
M9	4/1
M10	3.6/0.06
M11	0.4/0.06
M12	1.6/0.06
DNW Diode	1.76/4.1

Figure E.1: Transistor sizes for the third extracted circuit from the separated wells layout of Figure F.7

Chapter F
Layouts of the SET filters

The following figures illustrate the layouts of the studied circuits. The measures shown in the figures indicate the width of the circuit with and without the source rails because the positioning of those rails depend on the placement in a particular layout. The measures of the circuit area were made without the source rails.

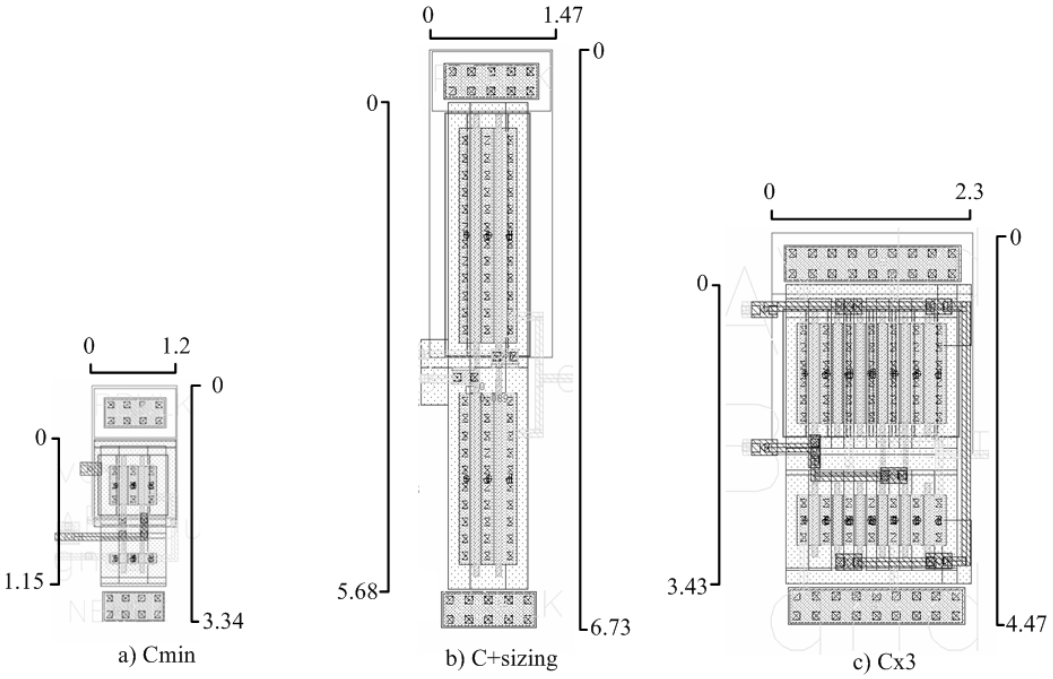


Figure F.1: a) Minimal size C-element (Cmin), b) Minimal C-element sized by a factor of 2.6 (C+Sizing), c) C-element folded three times (Cx3) (Units in μm)

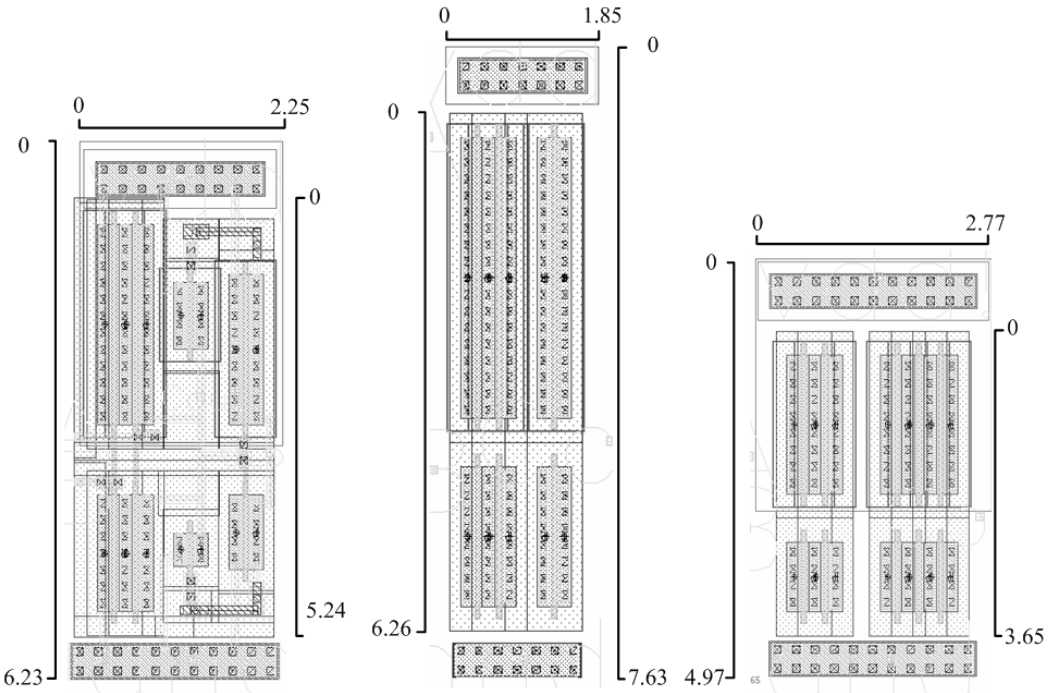


Figure F.2: a) C-element with latch (C+Latch), b) C-element-based Schmitt trigger (C+ST) , c) C-element with strengthening (C+Str)(Units in μm)

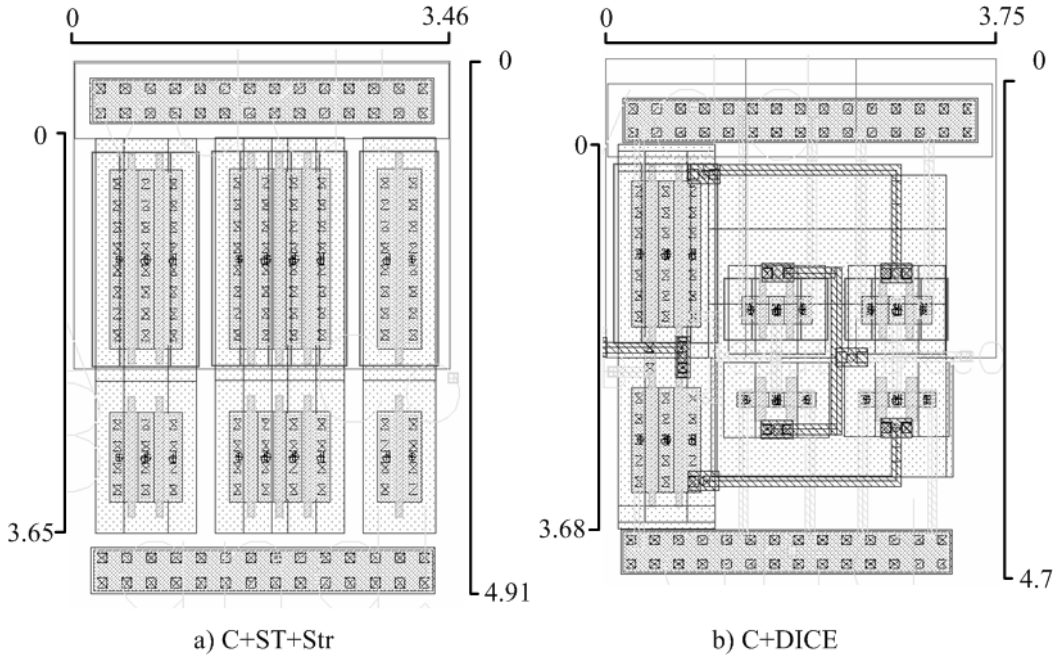


Figure F.3: a) C-element-based Schmitt trigger with strengthening (C+ST+Str), b) C-element with DICE (C+DICE) (Units in μm)

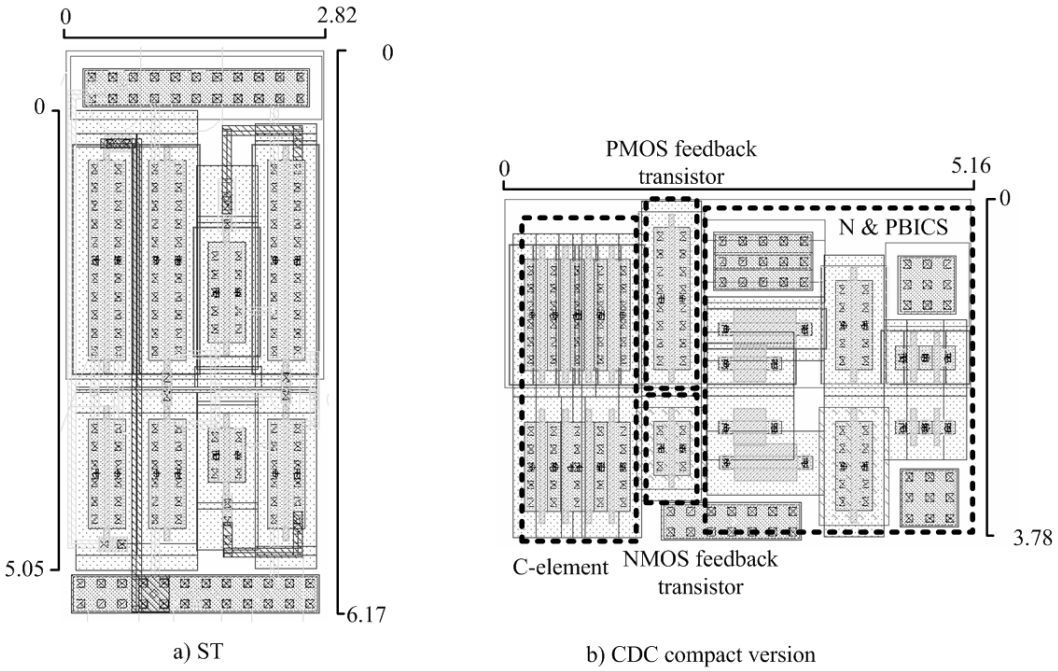


Figure F.4: a) Schmitt trigger, b) CDC ideal compact layout version (Units in μm)

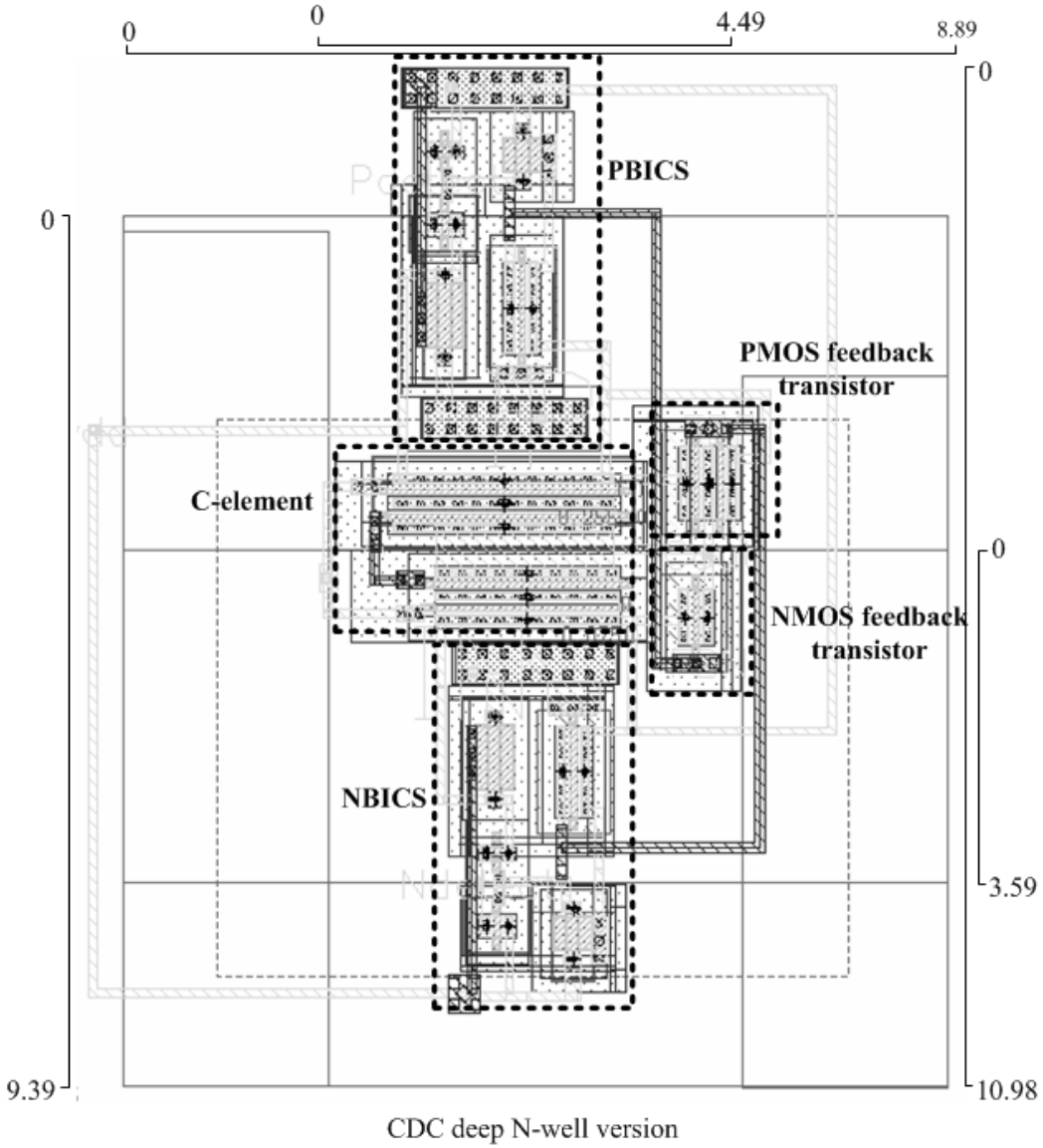


Figure F.5: CDC with deep N-well version(Units in μm)

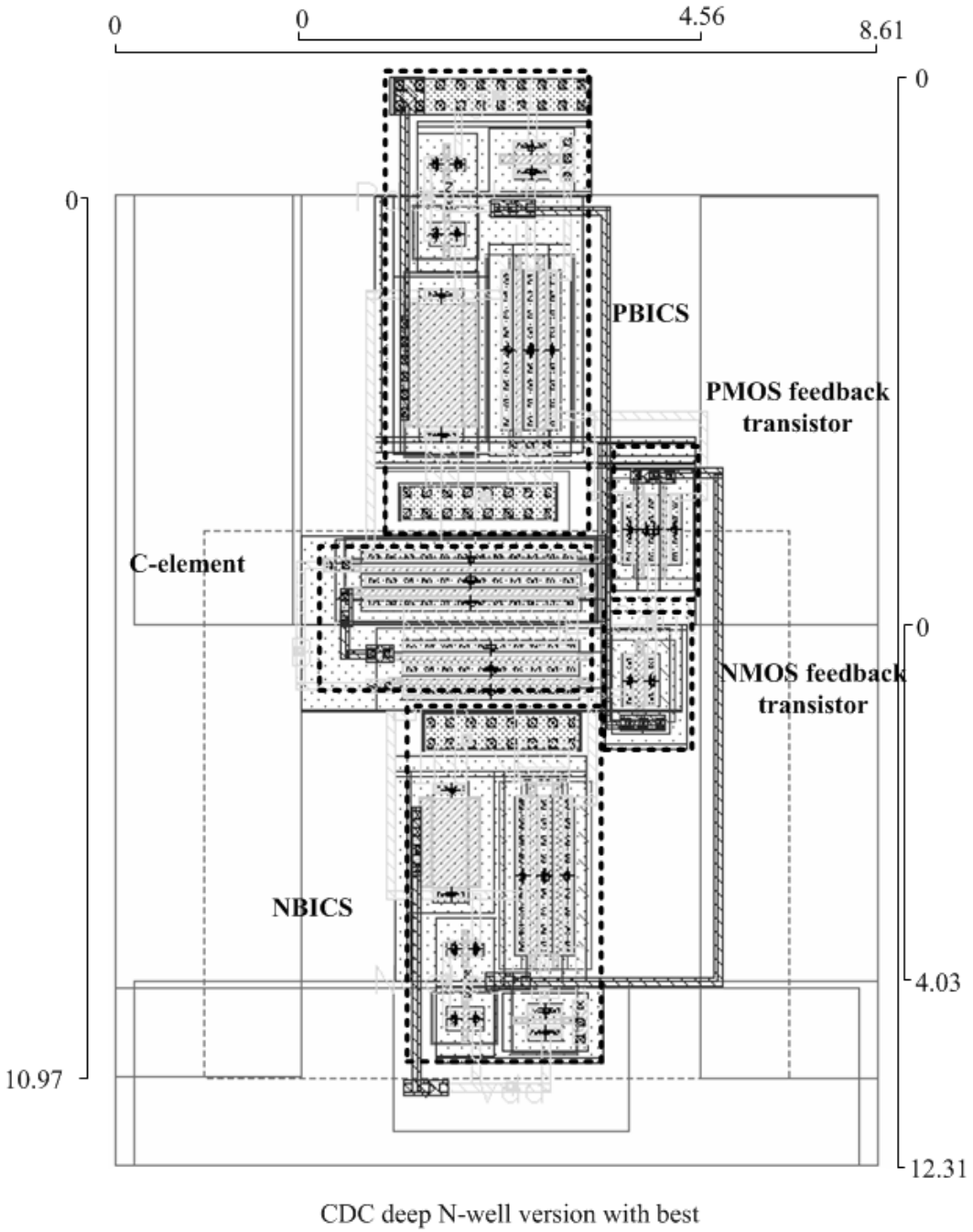


Figure F.6: CDC with deep N-well closest version to the theoretical performances (Units in μm)

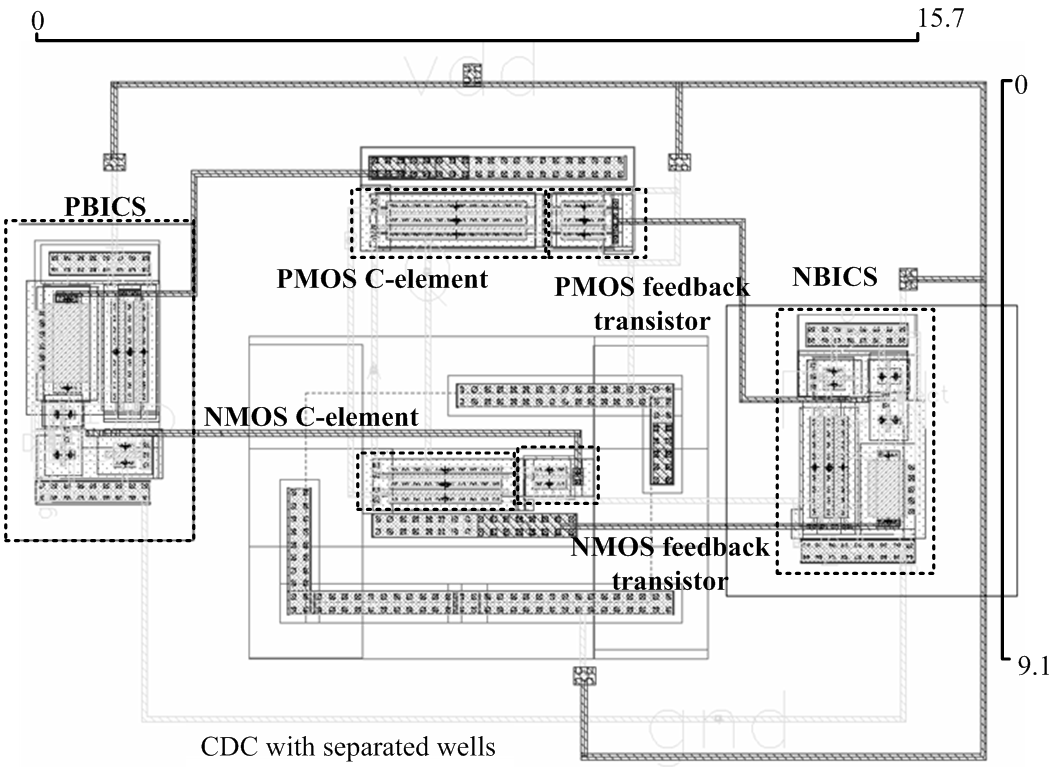


Figure F.7: CDC with well separation (Units in μm)

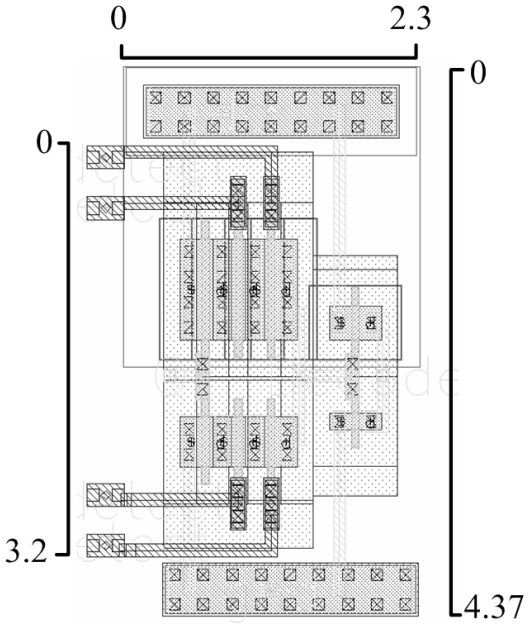


Figure F.8: The decoder (Units in μm)

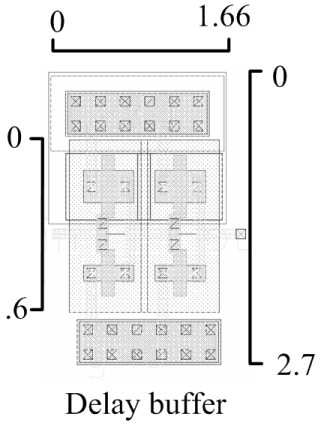


Figure F.9: The delay buffer (1 ns delay) (Units in μm)

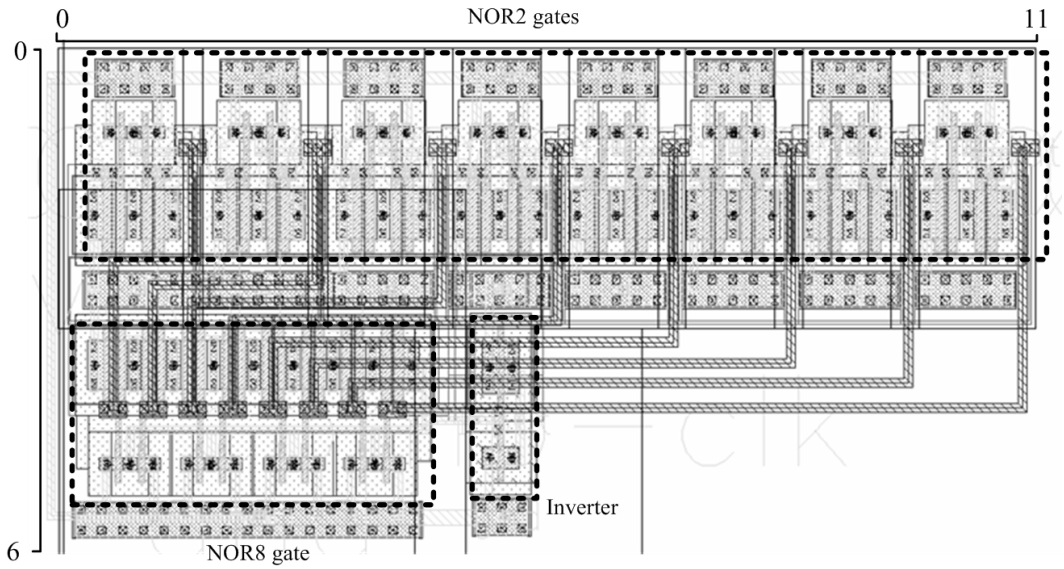


Figure F.10: The CLK generator function (Units in μm)

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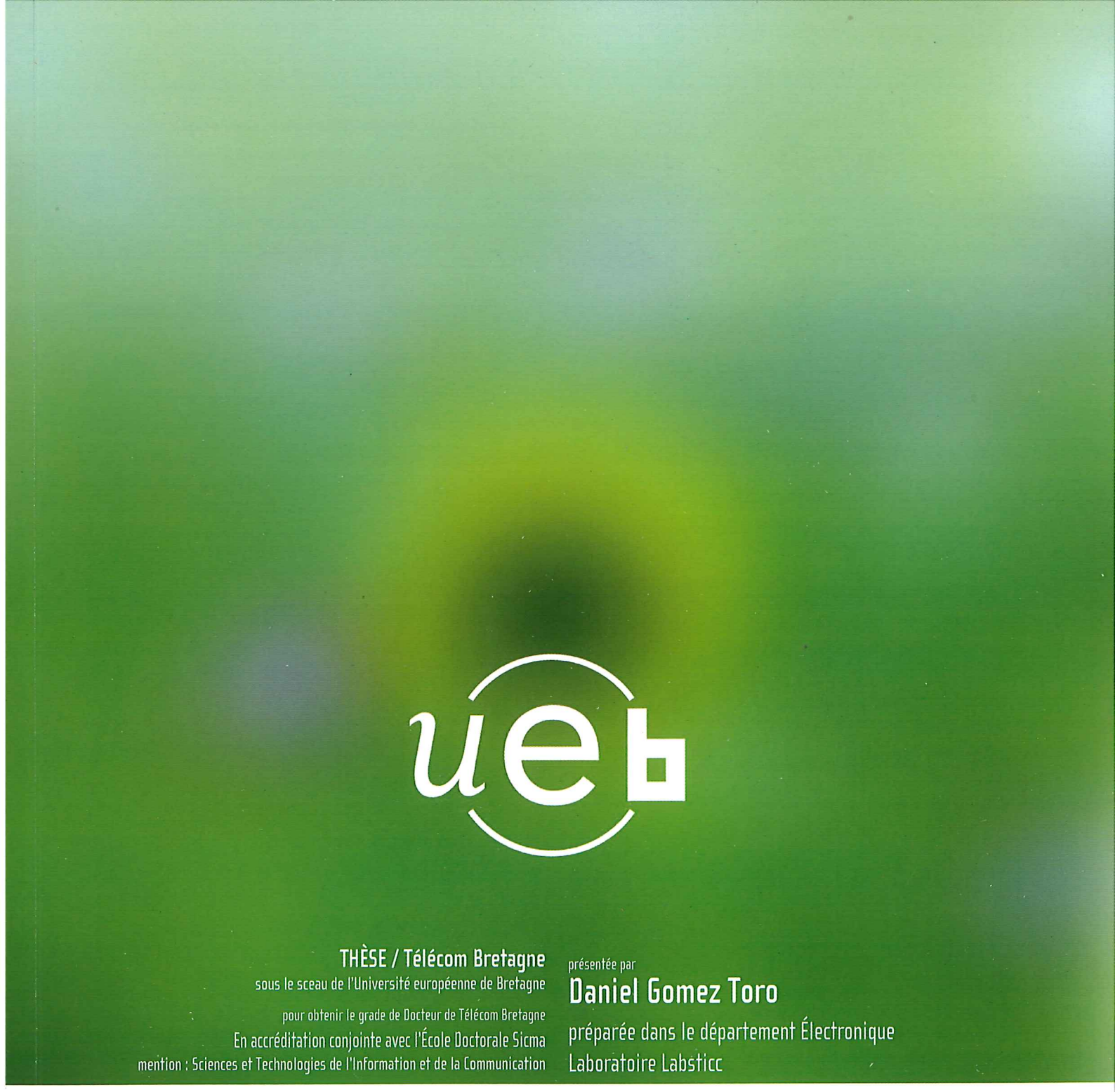

THÈSE / Télécom Bretagne
sous le sceau de l'Université européenne de Bretagne

pour obtenir le grade de Docteur de Télécom Bretagne
En accréditation conjointe avec l'École Doctorale Sicma
mention : Sciences et Technologies de l'Information et de la Communication

présentée par
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Temporal Filtering with Soft Error Detection and Correction Technique for Radiation Hardening Based on a C-element and BICS

Thèse soutenue le 12 Décembre 2014
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Résumé

L'augmentation de la densité d'intégration et la baisse de la tension d'alimentation ont amené une baisse de la marge du bruit et de la quantité de charges qui représentent un bit d'information. L'International Technology Roadmap for Semiconductors (ITRS) indique qu'en dessous de la technologie CMOS de 65 nm les erreurs soft ont un impact plus important sur la fiabilité des circuits au sol, non seulement sur les mémoires embarquées, mais aussi pour la logique et les verrous. Les erreurs soft sont des fautes fonctionnelles non destructives, à la différence des erreurs hard qui induisent des effets destructifs. Ils sont induits par des particules ionisantes très énergétiques qui frappent un transistor MOS. Ces particules ont pour origine principal la radiation cosmique. L'impact d'une particule ionisante sur un transistor MOS crée un courant parasite entre le substrat et le drain créant ainsi un pic de tension sur le drain. Il s'agit là d'un événement transitoire singulier (SET en Anglais). Si un SET est verrouillé on parle alors d'événement singulier perturbateur (SEU en Anglais). Il est important de modéliser le phénomène pour comprendre et simuler ses effets sur les circuits intégrés qui doivent être durcis. Pour cela le modèle dit «de collection de charges» permet de déterminer la quantité de charges collectées par un drain grâce à la géométrie d'une trace d'ionisation et de la position du drain. Grâce à ce modèle le courant parasite peut être estimé. Ce courant modélisé peut être intégré dans le simulateur électrique CADENCE comme une source de courant entre le substrat et le drain pour simuler ses effets. Cette méthodologie de simulation peut être utilisée sur un système cible pour déterminer la sensibilité aux SET d'un circuit en particulier. Un convertisseur analogique numérique (CAN) d'approximations successives a été choisi comme cas d'étude. Ce CAN est composé de circuits analogiques, numériques synchrones et asynchrones. La fonction combinatoire qui génère l'horloge interne est sélectionnée pour être durcie en raison de son importance pour un cycle de conversion. Grâce à la méthodologie de simulation, une étude de sensibilité est faite au niveau électrique, géométrique et temporel pour déterminer les vulnérabilités de la fonction. Il est conclu qu'un circuit supplémentaire devrait être placé à l'extérieur de la fonction combinatoire pour la durcir sans que le durcissement soit affecté par les mêmes vulnérabilités. Ce travail propose l'utilisation d'un filtre temporel durci dans le but d'arrêter des SET et éviter leur propagation si le filtre est touché. Le durcissement est réalisé avec des capteurs de courant intégrés sur le bulk (BICS en Anglais) pour détecter le courant parasite causé par l'impacte d'une particule ionisante. Une fois détecté l'effet transitoire à la sortie du filtre est compensé par des transistors de feedback pour éviter la propagation des SET.

Mots-clés : Rayon cosmique, Erreur soft, SET, SEU, Modèle de Collection de Charge, Charge Critique, CAN SAR, Durcissement contre les Radiations par Conception, Filtrage Temporel, C-élément, BICS.

Abstract

The higher density of integration and lower supply voltage have led to lower noise margins and a smaller amount of charge representing a bit of information. The International Technology Roadmap for Semiconductors (ITRS) stated that below 65 nm CMOS Technology soft errors impact field-level circuit reliability, not only for embedded memories, but for logic and latches as well. Soft errors are nondestructive functional errors, in contrast to hard errors that induce destructive effects. They are induced by an energetic ionized particle striking a MOS transistor. Those particles have their main origins in cosmic radiation and radioactive package impurities. The strike of an ionized particle on a MOS transistor creates a transient current between the substrate and the drain causing a voltage spike on the drain. That is a single-event transient (SET). A latched SET becomes a single-event upset (SEU). It is important to model the phenomenon in order to understand and simulate its effects on the integrated circuit that need hardening. For that the charge collection model helps determining the amount of charge collected on a drain surface given the geometry of an ionization track and the position of the drain. Thanks to this model the parasitic current can be estimated. This modeled current can be introduced in CADENCE's electrical simulator SPECTRE as a bulk-drain current source to simulate its effects. This simulation methodology can be used on a target system to determine the sensitivity of a particular circuit to SETs. As a case study an 8-bit successive-approximation-register (SAR) analog-to-digital converter (ADC) implemented in ST 65nm CMOS technology has been chosen. This ADC is composed analog, digital synchronous and asynchronous logic circuits. This diversity of circuits leads to different soft error outcomes. Among those circuits, a particular combinatorial function that generates an internal clock signal has been selected for hardening for its importance in the conversion cycle. Thanks to the simulation methodology, a study of the electrical, geometrical and temporal sensibilities is conducted to show the vulnerability issues of the function. It is concluded that an external circuit should be placed outside the combinatorial function to harden the function without being exposed to the same vulnerabilities. To counter SETs several technological and by design techniques exist. This work focuses on radiation hardening by design (RHBD) techniques since those techniques can be applied whiteout any additional technological cost. This work proposes a hardened temporal filter solution, which benefits from low power and low area overhead. The hardening is achieved using Built-In Current Sensors (BICS) to detect the parasitic current in the bulk caused by an ion strike and feedback transistors that are activated to compensate the effect at the output of the filter before the propagation of the SET.

Keywords : Cosmic rays, Soft Error, SET, SEU, Charge Collection Model, Critical Charge, SAR ADC, Radiation Hardening by Design, Temporal Filtering, C-element, BICS.

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