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► **To cite this version:**

B. Szelag, F. Balestra, G. Ghibaudo, M. Dutoit. Gate and Substrate Currents in Deep Submicron MOSFETs. Journal de Physique IV Proceedings, 1996, 06 (C3), pp.C3-61-C3-66. 10.1051/jp4:1996309 . jpa-00254227

HAL Id: jpa-00254227

<https://hal.science/jpa-00254227>

Submitted on 4 Feb 2008

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Gate and Substrate Currents in Deep Submicron MOSFETs

B. Szelag, F. Balestra, G. Ghibaudo and M. Dutoit*

LPCS/ENSERG-INPG (URA CNRS), BP 257, 38016 Grenoble, France

** IMO, EPFL, 1015 Lausanne, Switzerland*

1. INTRODUCTION

The study of hot carrier effects, mainly the substrate and gate currents, is of great interest for the prediction of the long term reliability of MOS devices. It has been shown that, although the substrate current and impact ionization rate are increased in the deep submicron range, they can be reduced at low temperature in the low drain voltage range ($V_d < 2V$) [1-3], this behavior being enhanced with reducing the channel length [4]. The gate current is supposed to be strongly correlated with the substrate current [5]. Simultaneous measurements of the substrate (I_b) and gate (I_g) currents have been recently reported for long channels (0.7 to 0.9 μm [6]). In this previous work, the results indicate that I_b and I_g exhibit opposite temperature dependence at low V_d , thus raising new questions on the interpretation of the so called crossover effect. However, no detailed investigation has been proposed for the gate current in a wide temperature range for deep submicron MOSFETs. The aim of this paper is to give a thorough analysis of the gate and substrate currents in a wide range of temperatures (down to near liquid helium), voltages (drain, gate, substrate) and channel lengths (down to 0.1 μm).

2. EXPERIMENTAL DETAILS

The devices used in this study are conventional silicon N MOS transistors fabricated with electron beam lithography and having a gate oxide thickness of 5 nm. The gate lengths range from 0.8 μm down to 0.1 μm . The channel doping of the order of $3 \cdot 10^{17} / cm^3$ is high enough in order to significantly reduce short channel effects. Shallow source and drain extension have been realised by arsenic implantation ($2 \cdot 10^{15} / cm^2$, 20keV).

The electrical characteristics were measured with a semiconductor parameter analyser HP4155A. The devices mounted in a 24 pin dual-in-line package were placed in a cryostat from CTI-Cryophysics allowing the temperature to be varied from 20 up to 300K.

3. RESULTS AND DISCUSSION

Fig. 1 shows the normalized variations of the maximum substrate current ΔI_{bmax} ($= (I_{bmax}(T) - I_{bmax}(300K)) / I_{bmax}(300K)$) as a function of temperature and channel length. For the 0.8 μm MOSFET (Fig. 1a), I_{bmax} decreases at low temperature only for the lowest drain bias ($V_d = 2V$). However, for the

0.1 μ m MOSFET (Fig. 1b), this reduction is observed for a drain bias up to 3V, showing the extension of this interesting property for a large range of Vd in the deep submicron range. Furthermore, the impact ionization rate (Ib/I_d) is reduced with decreasing the temperature for a drain voltage below 3.5V and increases above this bias for the 0.8 μ m MOSFET (fig 2a), whereas the reduction of Ib/I_d with the temperature occurs for drain bias up to 4V for the 0.1 μ m MOSFET (fig 2b). It is worth noticing that, in the previous works, such a reduction of hot carrier effects has only been obtained for Vd lower than 2V. This behavior has been associated with the substantial non-stationary effects in ultra-short channel MOS transistors at low temperature which seems to be strongly enhanced in our devices.

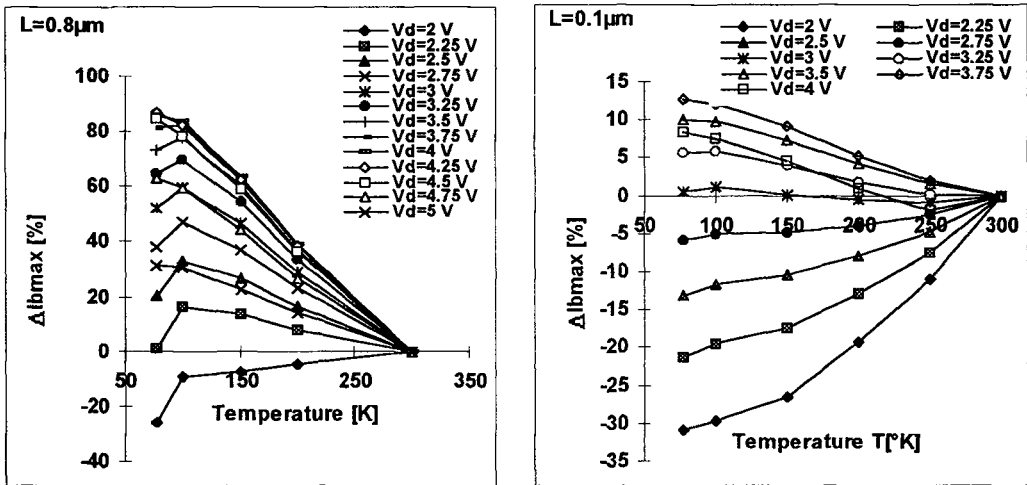


Fig.1: Normalized variations of the maximum substrate current as function of temperature with various drain voltage for (a) 0.8 μ m and (b) 0.1 μ m MOSFETs.

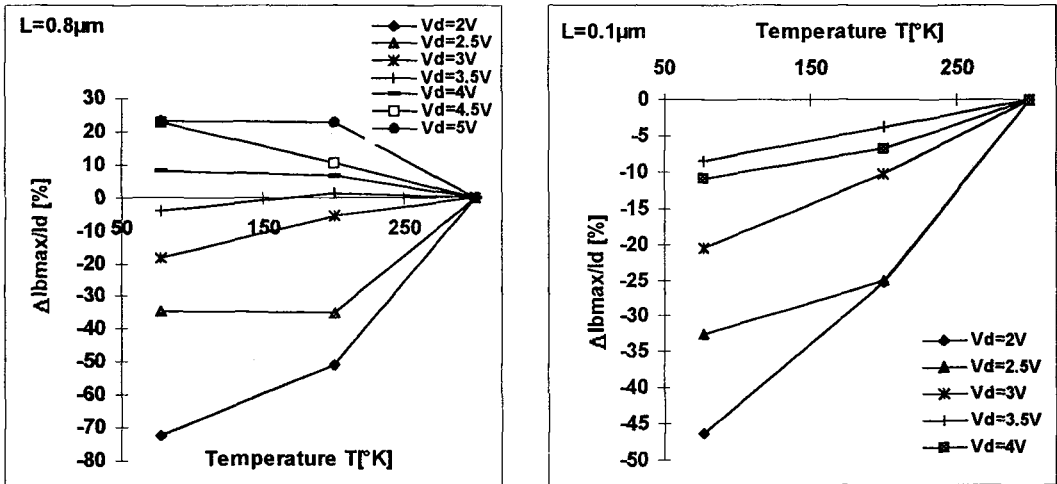


Fig.2: Normalized variations of I_{bmax}/I_d as function of temperature with various drain voltage for (a) 0.8 μ m and (b) 0.1 μ m MOSFETs.

Fig. 3 presents the variations of the gate current for the same devices in a wide temperature range. The gate current is substantially enhanced at low temperature (77K) in the 0.8 μ m MOSFET (Fig. 3a). A

maximum can also clearly be seen in these curves for intermediate values of gate biases. A very different behavior is obtained for a $0.1 \mu\text{m}$ device (Fig. 3b). In this case, a very small increase of gate currents is observed at low temperature. For low drain voltages, I_g is almost constant. Moreover, the gate current does not show a bell-shaped curve for both temperatures whatever V_d is [7]. It is worth noting that no reduction of I_g is obtained at low temperature, unlike the case of $I_{b\text{max}}$ variations (Fig. 1). In these results, the differences between the substrate and gate currents, on one hand, and between long and very short channels, on the other hand, are highlighted. The increase of I_g vs V_g for the $0.1 \mu\text{m}$ MOSFETs shows that the high field regions leading to the substrate and the gate currents are not the same. The physical mechanisms will be thoroughly investigated below.

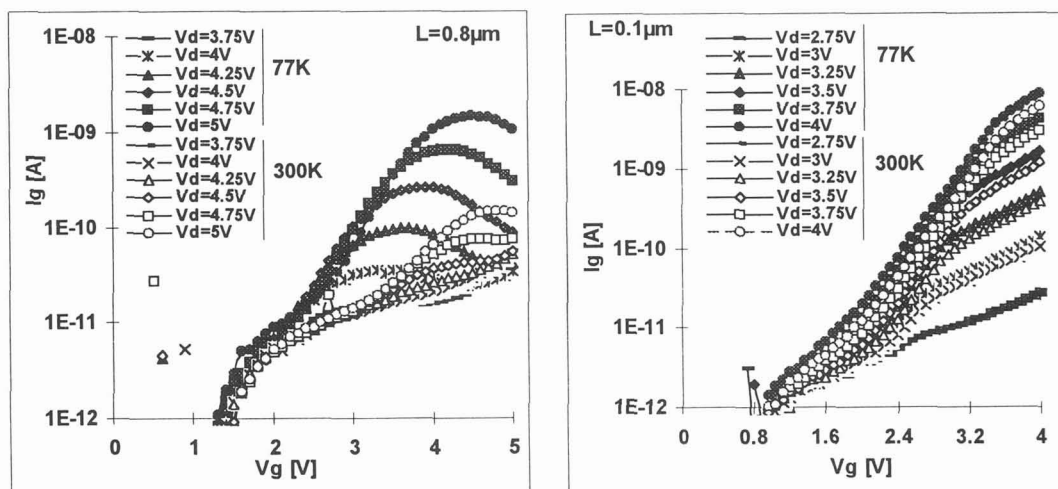


Fig 3: Gate current versus gate voltage for various drain biases and temperatures for (a) $0.8 \mu\text{m}$ and (b) $0.1 \mu\text{m}$ MOSFETs.

In Fig. 4 are shown the variations of the maximum transconductance for $0.1 \mu\text{m}$ and $0.8 \mu\text{m}$ MOS transistors in linear operation versus V_{sb} for various temperatures. An original behavior is highlighted in this figure for deep submicron MOSFETs. A conventional reduction of $G_{m\text{max}}$ is observed at 300K, similar to that obtained in the case of a $0.8 \mu\text{m}$ device, but a significant increase of $G_{m\text{max}}$ is underlined for temperatures lower than 200K. It is worth noticing that this feature is not obtained for high drain biases in saturation.

The influence of the substrate bias for hot carrier effects is exemplified in Fig. 5. An enhancement of the maximum substrate current is obtained with increasing V_{sb} for the $0.1 \mu\text{m}$ MOSFET, whereas a reduction of $I_{b\text{max}}$ is observed for the $0.8 \mu\text{m}$ transistor. The decrease of the temperature induces an increase of the variation of $I_{b\text{max}}$ with the substrate bias for $0.1 \mu\text{m}$ device. In both case, the variation of the maximum of the substrate current versus V_{sb} becomes temperature independent below 77K. These plots also underline the special mechanisms occurring in deep submicron devices.

Fig 6 presents the conventional $I_b(V_g)$ bell-shaped curves at the liquid nitrogen temperature for the $0.8 \mu\text{m}$ (fig. 6a) and the $0.1 \mu\text{m}$ (fig. 6b) MOSFETs, the substrate bias being the parameter. The shift of the curves is due to the augmentation of the threshold voltage with V_{sb} . For constant $(V_g - V_t)$, we can clearly see that I_b always increases with V_{sb} for the deep submicron device, whereas for the long channel MOSFET, I_b decreases for V_{sb} below 2V and increases above this voltage. It is worth noticing that, at room temperature for the $0.8 \mu\text{m}$ device, we have the same behaviour but the final increase is reduced compared with low temperature operation.

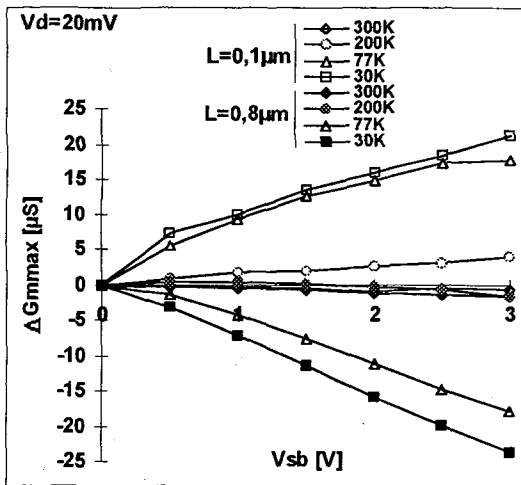


Fig. 4 : Maximum transconductance vs source-substrate voltage for various temperatures.

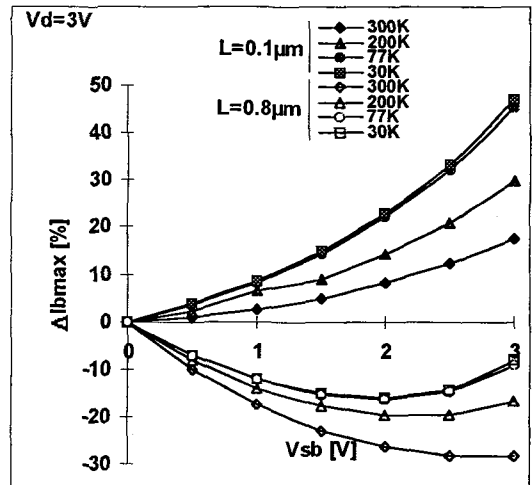


Fig.5 : Normalized variations of the maximum substrate current as a function of the source-substrate voltage for various temperatures and gate lengths.

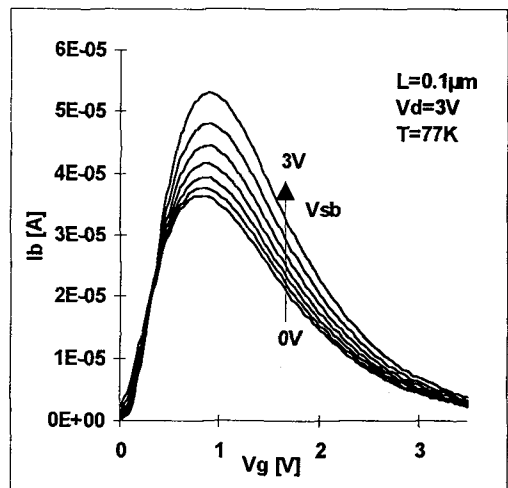
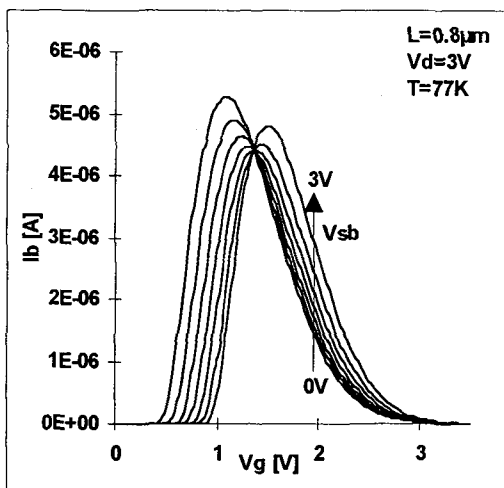


Fig 6 : Variations of the substrate current with the gate bias at 77K for various substrate biases for (a) 0.8 μm and (b) 0.1 μm MOSFETs.

We now consider the influence of the substrate bias on the gate current. Fig 7 presents the variations $I_g(V_g)$ for various V_{sb} at 77K and at 300K for the 0.8 μm (fig. 7a) and the 0.1 μm (fig. 7b) MOSFETs. On these curves, substantial increase of the gate current at low temperature is observed. We can also see that the gate current variations with the substrate bias are increased at 77K, these variations reaching their maximum for the medium gate biases and being reduced for high V_g . By comparing figures 6 and 7, it appears that the substrate bias has a larger influence on the gate current.

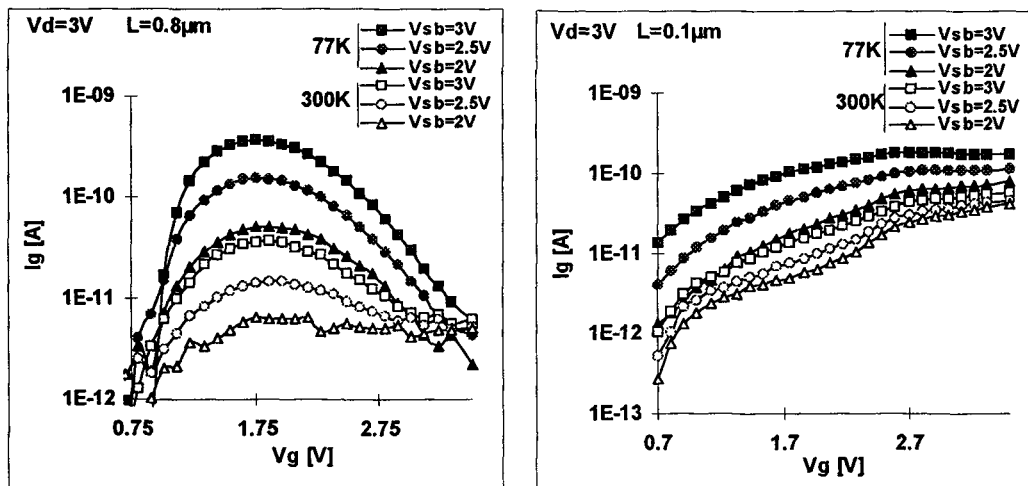


Fig 7 : Variations of the gate current with the gate bias at 77K and 300K for various substrate biases for (a) $0.8\mu\text{m}$ and (b) $0.1\mu\text{m}$ MOSFETs.

Fig 8 summarizes the different effects shown previously. Relative gate current I_g/I_d versus relative substrate current I_b/I_d is presented for a $0.8\mu\text{m}$ gate length device at 300K and 77K (fig. 8a and 8b respectively) and for a $0.1\mu\text{m}$ gate length at 300K and 77K (fig. 8c and 8d respectively). At a given gate bias, I_g increases exponentially while I_b increases only linearly versus V_{sb} , so I_g is a strong function of the substrate bias. The differences between very short devices and longer devices are also highlighted as a function of the gate bias. Indeed, I_g and I_b vary in the same way for the $0.8\mu\text{m}$ MOSFET, whereas for the $0.1\mu\text{m}$ MOSFET these two currents present opposite variations versus V_g . The variations of I_g with V_{sb} at a given V_g increase at low temperature.

This V_{sb} dependence shows that various mechanisms are involved in the variations of the gate and substrate currents. These behaviors are explained in terms of impact ionization feedback [8] caused by the secondary electron-hole pairs. In fact, the substrate current is created by low energy carriers heated by the pinch-off electric field, whereas the gate current is created by high energy carrier induced by the secondary heating at the drain-substrate junction, especially for deep submicron devices, explaining these original features. A thorough understanding of the temperature variations need further investigations.

4. CONCLUSION

The behaviors of the substrate and the gate current have been investigated in wide temperature, voltage and channel length ranges. For the deep submicron devices, a reduction of the maximum substrate current has been obtained at the liquid nitrogen temperature for drain bias up to 3V, which extends the previous range of observation of the crossover effect. Substantial differences between the temperature and bias dependences of the gate and the substrate currents have also been highlighted. These observations show that the high field region inducing I_b and I_g are not the same, especially for deep submicron devices. The substrate current depends mainly on the pinch-off region whereas the gate current is mainly correlated with the drain-substrate junction.

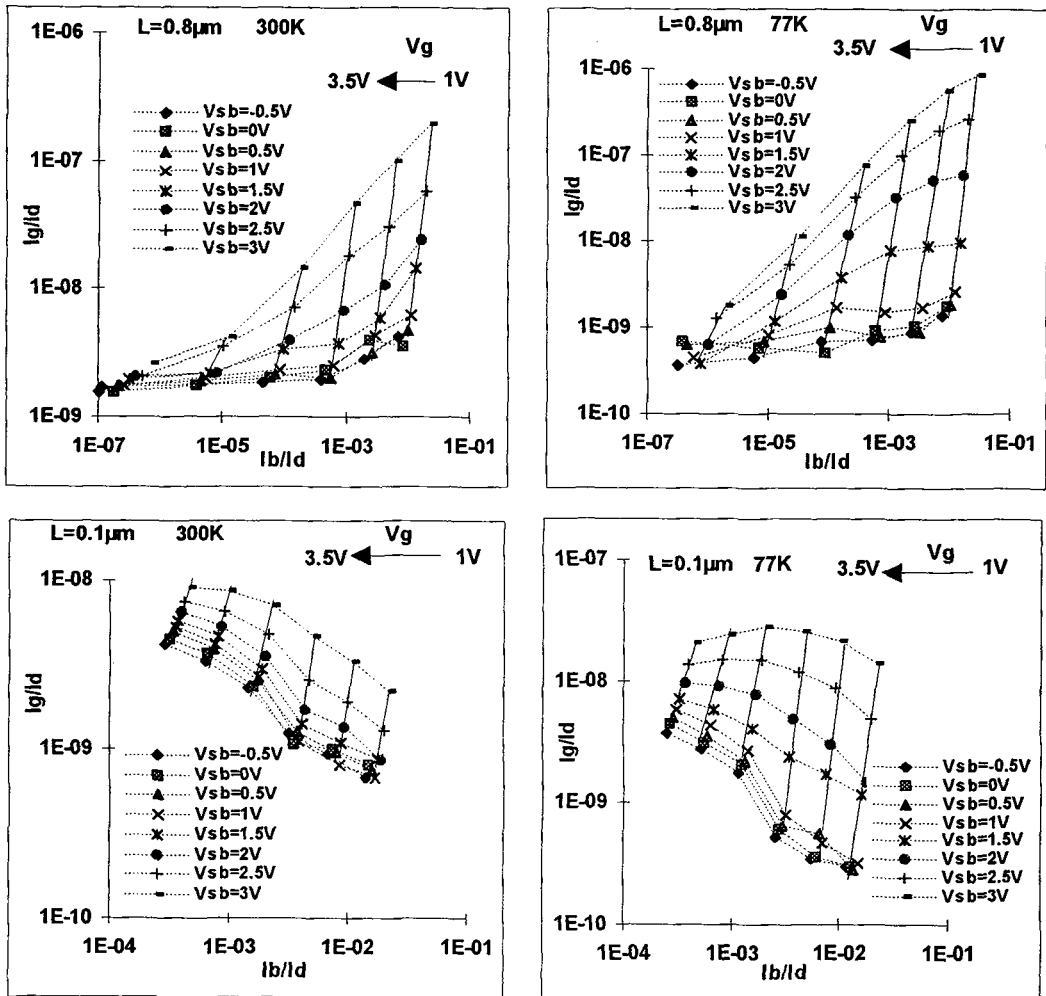


Fig. 8: Relative gate current vs relative substrate current for (a) $L=0.8\mu\text{m}$ at 300K, (b) $L=0.8\mu\text{m}$ at 77K, (c) $L=0.1\mu\text{m}$ at 300K and (d) $L=0.1\mu\text{m}$ at 77K

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