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## Characterization and Modeling of Silicon CMOS Transistor Operation at Low Temperature

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**Abstract :** A brief review of the main physical results about the low temperature characterization and modeling of Si CMOS devices is presented. More specifically, the carrier mobility law, the saturation velocity, the short channel effects, the impact ionization phenomenon, the hot carrier effects or the parasitic leakage current are physically discussed.

### 1. INTRODUCTION

Low temperature operation of Silicon CMOS transistors is a promising way to improve the circuit performance. The temperature reduction allows the increase of the carrier mobility and saturation velocity, better turn-on capabilities, latch-up immunity, reduction in activated degradation processes, lower power consumption, decrease of leakage current, reduced thermal noise, increased thermal conductivity, ... [1-12]. Nevertheless, the low temperature operation leads to specific problems related to the cryogenic condition. For instance, the impurity freeze-out, kink phenomenon, series resistance effects, transient behavior, changes in mobility laws make it difficult the physical understanding and modeling of the MOS device operation at low temperature (4.2-300K).

In this paper, a brief review of the main physical properties of Si CMOS devices operated at low temperature is presented. More specifically, various models for the low field and high field mobility are described. The saturation velocity and related non stationary transport phenomena observed at low temperature and for very short channel devices are analyzed. The influence of the impurity freeze out on the device operation via the kink effect and transient behavior is discussed. The parasitic leakage currents due to the impact ionization and gate induced drain leakage near drain are outlined. The short channel effects such as charge sharing, drain induced barrier lowering or punch through are also emphasized. The specific results recently obtained for hot carrier effects in sub 0.1 $\mu$ m MOS transistors are also addressed.

### 2. MOBILITY AND VELOCITY MODELING

#### 2.1. Low field mobility

The modeling of the mobility in Si CMOS devices has been the subject of much work during the past years [7,13,14]. The knowledge of the effective mobility law is of major importance for the modeling of the transfer and output characteristics of the MOS devices. The room temperature mobility law is well established for many years and has been ascribed to various physical mechanisms such as surface roughness scattering, surface phonon interaction or inversion layer degeneracy [7,13-15]. As the temperature is reduced, the mobility law is modified with a strong departure from the room temperature law.

A generalized mobility law has been proposed for a temperature range 4.2K-300K valid for strong inversion i.e. above threshold [15]. Using specific extraction method, the effective mobility has been shown to be an empirical function of the inversion charge  $Q_i$  or gate voltage  $V_g$  as [15,16]:

$$\frac{1}{\mu} = \frac{A}{Q_i^{n-2}} + B Q_i \quad \text{and} \quad \mu = \mu_m \frac{[\theta(V_g - V_t)]^{n-2}}{1 + [\theta(V_g - V_t)]^{n-1}} \quad (1)$$

where A and B are constants depending on the strength of the Coulomb and surface roughness scattering intensities,  $\mu_m$  is proportional to the maximum mobility,  $\theta$  is the mobility attenuation factor,  $V_t$  is the threshold voltage, and, n is an exponent coefficient which varies from 2 to 3 as the temperature is reduced from room to near liquid helium temperature.

Figs. 1-2 show typical variations of the maximum mobility and of the exponent n as a function of temperature as obtained on N channel devices. It is generally found that the ambient mobility law (n=2) is valid for P channel down to 20-25K whereas for N channel devices, the room temperature law applies down to 100-150K. The variation of the mobility law with

temperature can be interpreted by the combined contribution of two main scattering processes i.e. Coulomb scattering at low inversion charge and surface roughness at higher gate voltage. This analysis has been inferred by studying the influence of the substrate bias and of the fixed oxide charge near the channel [16]. As a matter of fact, the increase of the absolute substrate bias allows the carriers to be pushed towards the interface while the increase of the interfacial charge after Fowler-Nordheim gate stress enables to change the Coulomb scattering rate.

The mobility law of Eq. 1 can be used to explain quantitatively the evolution of the maximum mobility and attenuation coefficient with only one more parameter controlling A or B [16]. The change of the reciprocal mobility with the oxide charge  $Q_t$  indicates that, independently of the temperature, the Coulomb scattering coefficient  $\alpha_c = \Delta(1/\mu)/\Delta Q_t$  lies around 12000Vs/C and 3500Vs/C for electron and holes, respectively.

The mobility law of Eq. 1 is indeed valid up to intermediate electric field values (3-4MV/cm). Above this limit, strong electric field effects arise leading to the onset of negative transconductance phenomenon. This behavior can be interpreted as being the result of a higher order term in the denominator of Eq. 1b such as [17]:

$$\mu = \mu_m \frac{[\theta(V_g - V_t)]^{n-2}}{1 + [\theta(V_g - V_t)]^{n-1} + [\theta_2(V_g - V_t)]^n} \quad (2),$$

where  $\theta_2$  is a second order mobility attenuation factor.

It has been found that these mobility attenuation coefficients are nearly proportional to each other. This has been interpreted using a new surface roughness mobility model based on an appropriate spatial mobility profile within the inversion layer [18].

For a room temperature like mobility law i.e.  $n=2$ , the effective mobility is classically assumed as being an explicit function of the effective electric field in the inversion layer defined as:

$$E_{\text{eff}} = \frac{\eta Q_i + Q_d}{\epsilon_{\text{si}}} \quad (3),$$

where  $\eta$  is the inversion to depletion charge weighting factor,  $Q_d$  is the depletion charge. The parameter  $\eta$  is generally found around 1/2 (resp. 1/3) for N (resp. P) type devices [13,14,19].

A direct method for the extraction of  $\eta$  consists of measuring the sensitivity of the mobility with respect to the gate and substrate voltages such that [19]:

$$\eta = \frac{R}{1+R} \quad \text{with} \quad R = \frac{C_d}{C_{\text{ox}}} \frac{\partial \mu / \partial V_g |_{V_b}}{\partial \mu / \partial V_b |_{V_g}} \quad (4),$$

where  $C_d$  and  $C_{\text{ox}}$  are the depletion and gate oxide capacitances,  $V_b$  the substrate bias.

Fig. 3 shows an example of the temperature dependence of  $\eta$  as obtained using this method. As can be seen from this figure,  $\eta$  is well defined for holes and close to 1/3 for almost the whole temperature range, whereas for electrons it is only nearly constant above 250K ( $\approx 1/2$ ). Otherwise,  $\eta$  is found to strongly increase as the temperature is reduced due to the fact the mobility law deviates significantly from the room temperature one ( $n \neq 2$ ). These features indicate that the mobility is not in general a simple function of an effective electric field but depends in a complicated manner of two variables i.e. the inversion and depletion charges [19].

## 2.2. High field mobility

As the longitudinal electric field increases, hot carrier effects are emphasized giving rise to pronounced non ohmic behavior [1]. As a result, the drift velocity is no longer proportional to the applied electric field, making obsolete the concept of constant mobility. Instead, for high electric field ( $10^3$ - $10^4$ V/cm), velocity saturation due to intervalley and/or optical phonon scatterings leads to a strong decrease of the mobility whatever the temperature is [1,20].

The high field mobility is a function of the saturation velocity  $v_{\text{sat}}$  and low field mobility  $\mu_0$  by an empirical relation of the electric field  $E$  as [20]:

$$\mu = \frac{\mu_0}{\left[ 1 + \left( \frac{\mu_0 E}{v_{\text{sat}}} \right)^a \right]^{1/a}} \quad (5),$$

where  $a$  is an exponent varying between 1 and 5.

Based on Eq. 5, the saturation velocity can be extracted after plotting the drift velocity near source  $v_{\text{ds}}$  as a function of the source electric field  $E_s$  [21]. The source velocity  $v_{\text{ds}}$  is deduced from the drain current  $I_d$  as,

$$v_{\text{ds}} = \frac{I_d}{WC_{\text{ox}}(V_g - V_t)} \quad (6),$$

where  $W$  is the channel width.

The source electric field is given by [21]:

$$E_s = I_{d0} / (LG_d) \quad (7),$$

where  $I_{d0}$  is the drain current in the absence of saturation velocity and  $G_d$  the ohmic conductance. As at strong inversion, the drain current is a function of  $(V_g - V_t)$ , so that  $I_{d0}$  can be calculated from the ohmic transfer characteristics as [21],

$$I_{d0} = \int_0^{V_d} G_d (V_g - u) du \quad (8)$$

Otherwise, the conventional method for the extraction of the saturation velocity uses the saturation drain current given by,

$$I_{dsat} = WC_{ox} v_{sat} (V_g - V_t - V_{dsat}) \quad (9)$$

where  $V_{dsat}$  is the saturation drain voltage.

The saturation velocity and the exponent  $a$  have been extracted after applying Eq. 5 to the  $v_{ds}(E_s)$  characteristics for different temperatures and channel lengths. Fig. 4 shows the variation of the saturation velocity with temperature as obtained using this method and the conventional one. A significant increase of the saturation velocity can be noticed as the temperature is reduced. A strong increase of the saturation velocity as the channel length is reduced below  $0.2-0.25\mu\text{m}$  has also been observed and is possibly attributed to the onset of velocity overshoot resulting from non stationary transport at short channel length [21-23]. After extracting the velocity saturation from Eq. 5, values for the exponent  $a$  have been found in the range 4-6 in agreement with results obtained at room temperature on resistive gated MOS transistors [20].

### 3. INFLUENCE OF IMPURITY FREEZE OUT

Impurity freeze-out becomes a major issue for temperature below 150K in devices with usual doping concentration and elements (B, P, As, ..). At 77K, the freeze out effect is not very pronounced but could lead to an increase of the parasitic series resistance in MOS devices with Lightly Doped Drain (LDD) structures. At lower temperatures where strong freeze out happens, kink effect as well as transient phenomena may be a serious concern.

#### 3.1. Impact of LDD structures

As the temperature is reduced, the impact of LDD's on the operation of MOS transistors becomes critical due to the impurity freeze out in the LDD regions [24]. The presence of LDD's considerably affects the static characteristics of MOS devices operated in the linear region at low temperature ( $T < 100\text{K}$ ). The LDD series resistance has been shown to increase dramatically at low temperature due to the non degenerate doping level in the LDD regions, resulting in the de-activation of the channel [24]. However, it has also been demonstrated that, at high enough drain and gate voltages, a sufficiently high field assisted impurity ionization occurs, which allows a strong reduction of the series resistance with biasing. The presence of LDD's leads to a strong degradation of the drain current in ohmic region but does not alter the saturation current.

Thanks to a simple analysis taking into account the pseudo ohmic part of the output characteristics, it has been possible to evaluate the LDD series resistance  $R_{sd}$  as a function of the electric field across the LDD region,  $E_{LDD}$ , for various experimental conditions [24]. In Fig. 5 are reported typical variations of the LDD resistance with the electric field for various temperatures. This peculiar behavior for the series resistance has been found independently of the gate bias and LDD implantation dose. This phenomenon has been quantitatively interpreted by field assisted shallow level impact ionization [24]. The series resistance in the LDD region can therefore be expressed as:

$$R_{sd} = R_0 (N_d / N_d^+) \quad (10)$$

where  $N_d^+ / N_d$  is the fraction of ionized impurities and  $R_0$  is the minimum LDD resistance when no freeze out effect occurs.

For shallow level impact ionization, the fraction of ionized impurities reads,

$$N_d^+ / N_d = 1 + \frac{N_{d0}^+ / N_d - 1}{1 + \gamma} \quad (11)$$

where  $N_{d0}^+ / N_d$  is the thermal equilibrium ionization rate and  $\gamma = \gamma_0 \exp(-B/E_{LDD})$  is the Chynoweth-like formula for the ratio between the impurity ionization cross section and the impurity capture cross section [24].

#### 3.2. Kink phenomena

It is well known that at low temperature ( $T < 30\text{K}$ ), enhancement-mode MOS devices suffer from the presence of a kink effect in the saturation region (see Fig. 6) [8,9]. This phenomenon, which is similar to the so called "kink" in SOI devices, is attributed to the self polarization of the bulk due to majority carriers flowing from the body to the source. At low temperature, the impurity freeze out in the substrate results in a strong increase of the back resistance which reduces the evacuation of the impact ionization current via the body electrode. This phenomenon gives rise to the self biasing of the substrate and in turn to the forward polarization of the source-substrate diode. The shift in the bulk bias  $V_b$  induces a further change of the threshold voltage which explains the increase of the drain current in saturation [8-10,25].

The excess drain current due to the parasitic biasing of the body can approximately be modeled by the formula [25]:

$$\Delta I_d = g_b V_b \quad (12)$$

where  $g_b$  is the body transconductance which is related to the gate transconductance as  $g_b = (C_d / C_{ox}) g_m$ .

The change in the internal substrate bias is calculated from the substrate current crossing the forward-biased source-substrate junction by a classical diode formula extended to the case of low temperature condition [25]. The impact ionization substrate current is evaluated using the usual expression given below (see section 4.1). This approach gives a satisfactory

description of the kink effect for temperatures down to 25K [25] and can also be applied to explain the reduction of the kink effect in short channel MOS devices due to the combined effects of charge sharing and velocity saturation with temperature [10].

### 3.3. Transient effects

In the deep freeze out regime for very low operation temperatures ( $T < 30K$ ), the frozen-out impurities do not ionize enough rapidly [26]. As a result, for small electric field, the ionization by carrier emission from the trap should take an infinitely large time to occur. The application of a large enough electric field allows field assisted ionization to take place and in turn the formation of the depletion layer in the silicon substrate. This phenomenon leads to transient behaviors in the drain current when a pulse is applied to the MOS device terminals [4,5].

Three mechanisms are mainly involved in the field assisted impurity ionization at low temperature [26,27]. The first one is the well known Poole-Frenkel ionization where the emission barrier is reduced by the voltage bias. The second possible process is the tunnel assisted field ionization. This mechanism is likely more efficient at higher electric fields. The third one is the shallow level impact ionization discussed previously in section 2.2 [27].

The non instantaneous response of the depletion layer formation is at the origin of the drain current transient. As a consequence, the temperature lowering leads to a strong increase of the transient time. The time constant of the drain current transient is also found to depend significantly on the gate and drain biases as reported in Fig. 7.

## 4. PARASITIC LEAKAGE CURRENTS

In this section the temperature dependence of the main parasitic leakage currents arising at high voltages is illustrated. Among these currents are the substrate current due to the impact ionization happening near the drain and the gate induced drain leakage (GIDL) current which results from band to band tunneling in the drain to gate overlapped region.

### 4.1. Impact ionization substrate current

The characterization of the substrate current due to the impact ionization near the drain is a key issue for the kink effect and hot carrier degradation processes. A study of the substrate current in a MOS transistor is thus mandatory for the qualification of CMOS technology for cryogenic operation. In this section, some results about the temperature dependence of the impact ionization current in MOS devices are presented. According to our findings, the classical substrate current model is found to be applicable down to near liquid helium temperature [28].

The substrate current is found to be much higher in N channel transistors (by about 3 orders of magnitude) than in P type structures. This feature is obviously attributed to the higher mobility and higher impact ionization rate for electrons than for holes. After extraction of the saturation voltage  $V_{dsat}$ , the multiplication factor  $I_{sub}/I_d$  has been plotted versus  $1/(V_d - V_{dsat})$  and found to vary linearly over the whole temperature range (20-300K). This feature demonstrates that the substrate current can be well modeled by the conventional relation [28-31]:

$$I_{sub} = A I_d \exp[-B / (V_d - V_{dsat})] \quad (13),$$

where A and B are empirical constants linked to the impact ionization law coefficients as  $A = a_i l$  and  $B = b_i l$  with l being the effective ionization length near drain.

The coefficients A and B have been extracted for various temperature and are given in Fig. 8. The interesting result is that the coefficient B is found to be almost constant with temperature (close to 30 and 50 V) whereas the coefficient A is monotonically increasing as the temperature is reduced [28]. Since  $b_i$  is weakly temperature dependent, this means that l should also be temperature independent. Instead, the temperature dependence of the substrate current is thought to stem essentially from that of the coefficient A. This feature could be justified by the temperature dependence of the pre-exponential factor of the impact ionization rate, which is physically not very well understood [30].

### 4.2. Gate Induced Drain Leakage

Gate induced drain leakage (GIDL) constitutes a major concern as regard to the off-state current in scaled down MOS devices [32,33]. This section summarizes the GIDL results obtained in MOSFETs operated under cryogenic condition. To this purpose, the GIDL phenomenon has been investigated as a function of temperature (20-300K) on CMOS transistors issued from various technologies with and without LDD's [34].

The GIDL is mainly due to the band to band tunneling which occurs in the drain to gate overlapped region at high drain voltage while biasing the device in strong accumulation.

The onset of GIDL depends strongly on the gate-to-drain overlap and on the drain doping concentration. It has been found that the GIDL is significant for devices without LDD and with LDD doped at sufficiently high doses [34].

It is generally found that the GIDL current decreases substantially (by almost one order of magnitude) as the temperature is reduced. This feature opposes the usual argument according to which band-to-band tunneling is temperature independent. At sufficiently high gate-to-drain field, the GIDL current varies almost linearly with the reciprocal potential across the oxide. This suggests that band-to-band tunneling is the dominant process down to 20K [34]. This behaviour can be interpreted by the classical GIDL model [32-34]:

$$I_d = W A^* E_{ox} \exp(-B^* / E_{si}) \quad (14)$$

where  $E_{Si} = (V_g - V_d - 1.2) / (3t_{ox})$  is the surface silicon electric field,  $B^*$  is an exponential coefficient proportional to the silicon gap to the power 3/2 and  $A^*$  is a constant proportional to the squared energy gap.

Fig. 9 shows typical variations with temperature of the GIDL coefficients  $A^*$  and  $B^*$ . The exponential coefficient is nearly constant with temperature and close to the theoretical value (30-40MV/cm) [34]. In contrast,  $A^*$  is found to decrease monotonically as the temperature is reduced. The change of the silicon energy gap with temperature (5% over the whole temperature range) cannot be advanced to explain this temperature dependence. This implies that another mechanism or a better modeling of the band-to-band tunneling process could be considered to explain such a behavior.

## 5. SHORT CHANNEL EFFECTS

In this section we review the temperature dependence of the main short channel effects such as charge sharing, drain induced barrier lowering (DIBL) and punch-through.

### 5.1. Charge sharing

It is well known that as the MOS devices are scaled down, there is a critical roll-off of the threshold voltage at zero drain bias for short gate lengths. This feature is attributed to the so-called charge sharing effect [35]. Since charge sharing depends essentially on the depletion layer thickness in the substrate and at the source-drain ends, it is expected to vary slightly with temperature. Indeed, this has been observed on submicronic MOS devices operated at 77K [6].

More recent results demonstrates that this behavior is also true for deep submicron N MOS transistors as exemplified in Fig. 10. In this figure, one can see a strong roll-off of the threshold voltage below 0.2 $\mu$ m independently of temperature down to 25K.

### 5.2. Drain Induced Barrier Lowering

Drain Induced Barrier Lowering (DIBL) is a serious constraint for deep submicrometer device operation [36,37]. For this reason, the temperature dependence of the DIBL effect is an important issue to be addressed for cryogenic applications.

The DIBL effect has been thoroughly investigated as a function of temperature on deep submicron MOS devices between room and near liquid helium temperatures [38]. To this end, a new method for the extraction of the DIBL coefficient has been used. The DIBL leads to a linear decrease with drain voltage of the threshold voltage such that  $V_t = V_{t0} - \lambda V_d$  [36,37]. Since the drain current depends essentially on the gate voltage drive from weak to strong inversion, it is easy to show that in the saturation region the output conductance to gate transconductance ratio provides the DIBL parameter as [38]:

$$\lambda = g_{dsat} / g_{msat} \quad (15)$$

This method has been employed on deep submicron N MOS transistors with 55Å gate oxide thickness and channel lengths ranging between 0.1 and 2 $\mu$ m. The values of  $\lambda$  have been extracted using Eq. 15 from the minimum of the  $g_d/g_m(V_d)$  characteristics for all the geometries and temperatures [38].

Fig. 11 shows the variations of the DIBL coefficient as a function of channel length for various temperatures between 50K and 300K. As expected from the simple theory [36],  $\lambda$  is found to vary almost linearly with the reciprocal channel length and to be nearly temperature independent.

This last feature clearly emphasizes the fact that the DIBL effect does remain a serious constraint even for low temperature operation, since it cannot be remedied by a cryogenic operation.

### 5.3. Punchthrough

Unlike charge sharing effect, the punchthrough current which is the leakage from source to drain via the silicon substrate is significantly reduced by the temperature lowering [6]. This is due to the fact that the punchthrough current is mainly governed by the thermoionic emission over the barrier between source and drain [6]. The punchthrough current can therefore be expressed as [6,11]:

$$I_d = I_0 \exp\left(-\frac{\Phi}{kT}\right) \quad (16)$$

where  $\Phi$  is the source-to-drain barrier height. Thus, the punch through current is thermally activated and by turn strongly reduced at low temperature. This phenomenon is critical in the subthreshold region where the presence of low amplitude leakage currents is easily observable. This feature demonstrates that the operation at low temperature is an effective way to reduce the parasitic punchthrough leakage current in MOSFETs even though their operation is not well optimized at room temperature.

### 5.4. Specific behavior for sub 0.1 $\mu$ m devices

Original behaviors have been recently observed for hot carrier effects in deep submicron MOSFETs. In Fig. 12 are shown the variations of the substrate current with gate voltage as a function of  $V_d$  for 300 K and 77 K in the case of a 0.07  $\mu$ m gate length MOS device. As illustrated in Fig. 12a for 300K, the substrate current peak is obtained for a  $V_g$  value ( $V_{gmax}$ ) which is almost independent of drain voltage, unlike for long channel MOSFETs for which a strong decrease of  $V_{gmax}$  is obtained with reducing  $V_d$ . On the other hand, at 77 K (Fig. 12b),  $V_{gmax}$  substantially increases when  $V_d$  is reduced, emphasizing an original behavior for these deep submicron MOS transistors. A similar trend has been found for various MOSFETs fabricated with different technologies [39-43]. It is worth noting that, in Fig. 12b, the maximum substrate

current is obtained for a gate voltage which is almost two times higher than the drain bias for the lowest  $V_d$  at 77 K, which is different from the conventional  $V_g=V_d/2$  observed for long channel MOS devices. These phenomena will be very important for the aging conditions of sub-0.1  $\mu\text{m}$  devices, and a degradation for  $V_g=V_d/2$  will not lead to the maximum substrate current conditions. These features are associated with the variations of the impact ionization rate  $M (=I_p/I_d)$ . The slopes of the  $M(V_g)$  and  $M(1/(V_d-V_{dsat}))$  characteristics have been found to decrease with reducing the gate length in the sub-0.1  $\mu\text{m}$  range. Furthermore, for 0.07  $\mu\text{m}$  devices,  $M$  shows the most gentle slope with  $V_g$  for low  $V_d$  and at low temperature [39]. This low reduction of the impact ionization rate with increasing the gate bias leads to an enhancement of the substrate current until high  $V_g$  and induces a substantial shift of the substrate current peak.

The substantial increase of the impact ionization rate when the devices are scaled down has been attributed to the reduction of the effective pinch-off length, associated with the high lateral electric field region, which is limited by the channel length in deep submicron devices (see Fig. 13). Indeed, the effective channel length for the 0.07  $\mu\text{m}$  MOSFETs is in the sub-50nm range. Furthermore, the theoretical pinch-off length for these devices, which depends on the gate oxide thickness and junction depth [44], is around 70nm. Therefore, it is clear that the effective pinch-off length is reduced in the sub-0.1  $\mu\text{m}$  transistors compared with that obtained in long channel devices. This behavior can also explain the reduction of the slope of the  $M(V_g)$  characteristics with reducing the gate length, this slope being proportional to the pinch-off length of the devices [39]. On the other hand, it has been found that, at low temperature, a significant decrease of the ionization rate is obtained with reducing the pinch-off length, and over a length of 100 nm the energy distribution of hot carrier has not reached a stationary state [45]. Therefore, at low temperature, the significant enhancement of non-stationary effects for very short high field regions, together with the lower electron energy in the initial energy distribution which gives rise to a reduction in the number of high energy electrons for low drain bias and electric field, lead to a substantial reduction of the impact ionization rate observed in the case of the shortest devices (sub 0.1  $\mu\text{m}$ ) and the lowest drain voltage (see Fig.13).

## 6. CONCLUSION

A brief review of the electrical properties of Silicon CMOS devices operated from room down to liquid helium temperature has been presented. First, typical results and models for the low field mobility and saturation velocity have been given. The strong modification of the mobility law at low temperature has been underlined. The observation of velocity overshoot as the device are scaled down has been illustrated for 0.1 $\mu\text{m}$  N MOS devices. The influence of the impurity freeze out which occurs at low temperature, has also been discussed. The impact of LDD's on the performance of MOSFETs has been emphasized. The onset of a kink effect in the output characteristics in the saturation region has been addressed. The presence of drain current transients for MOSFETs operated at low temperature has been illustrated. The parasitic leakage currents such as the impact ionization substrate current and gate induced drain leakage have been analyzed as a function of temperature. Finally, the impact of temperature on various short channel effects such as charge sharing, drain induced barrier lowering and punchthrough has also been presented. The specificity of hot carrier effects in sub 0.1 $\mu\text{m}$  devices has also been discussed.

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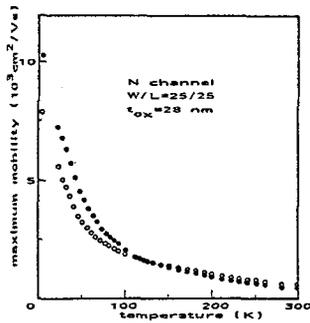


Fig. 1: Typical variations of the maximum effective (o) and field effect (•) mobilities with temperature [15].

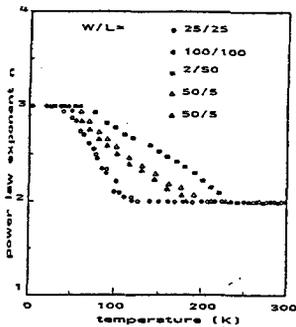


Fig. 2: Typical variations of the power law parameter n with temperature as obtained on N channel devices [15].

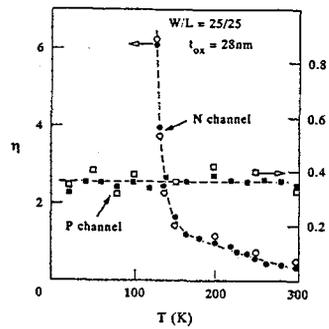


Fig. 3: Typical variations of the parameter  $\eta$  with temperature as obtained for P and N channel devices [19].

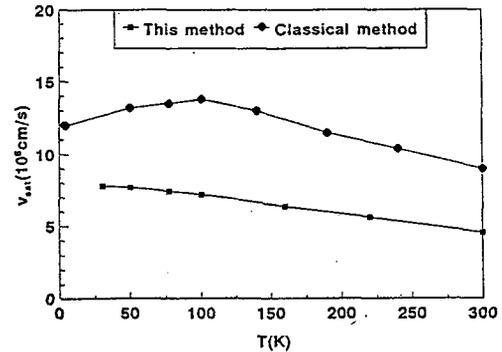


Fig. 4: Variation of the saturation velocity with temperature as obtained from various methods [21].

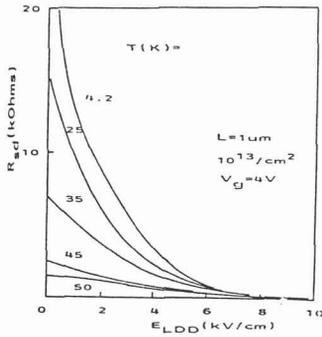


Fig. 5: Typical variations of the LDD series resistance with LDD electric field for various temperatures [24].

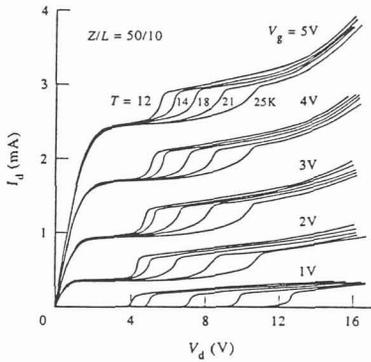


Fig. 6: Typical drain current output characteristics illustrating the onset of the kink effect in saturation at low temperature [8].

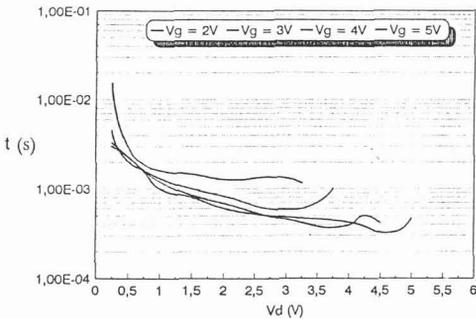


Fig. 7: Variation of the transient time with drain voltage as measured after pulsing the gate with various biases.

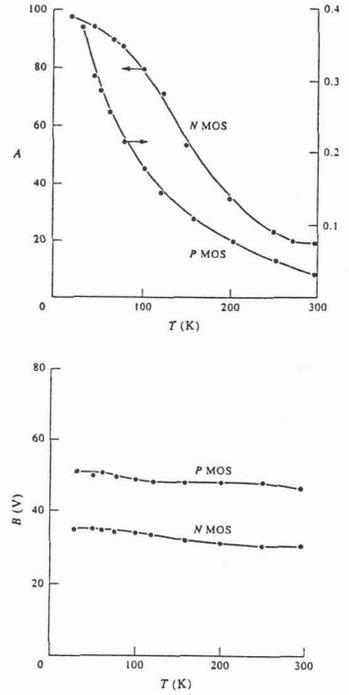


Fig. 8: Variations of the A and B coefficients with temperature as obtained for N and P channel devices [28].

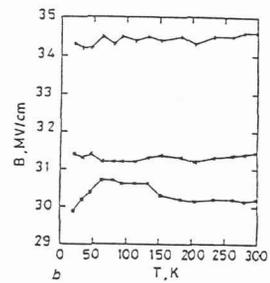
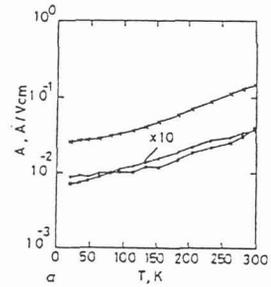


Fig. 9: Variations of the GIDL coefficients  $A^*$  and  $B^*$  with temperature for all device types ( $\times$  pMOS without LDD,  $\blacksquare$  pMOS with LDD and  $+$  nMOS with LDD) [34].

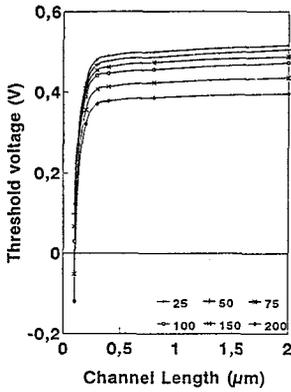


Fig. 10: Variation of the threshold voltage with channel length as obtained on submicron MOS devices for various temperatures.

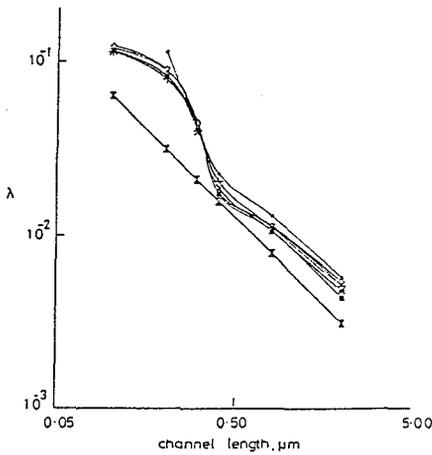


Fig. 11: Variations of the DIBL parameter with channel length as obtained for several temperatures [38].

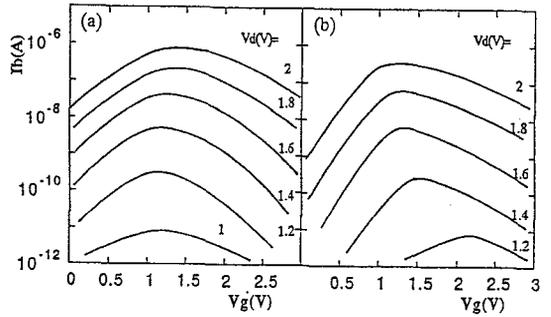


Fig. 12 : Substrate current - gate voltage characteristics for a 0.07 μm gate length MOSFET's for (a) 300K, and (b) 77K [39].

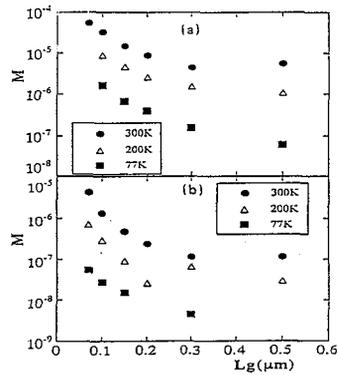


Fig. 13 : Variations of the impact ionization rate ( $M=I_b/I_d$ ) as a function of  $L_g$  for a constant ( $V_g-V_t$ ) value ( $V_g-V_t=1.2$ V) at 300, 200 and 77 K; (a)  $V_d=1.8$ V and (b)  $V_d=1.5$ V [43].