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Several alternative approaches to the manufacturing of HTS Josephson junctions

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In this work we describe comparatively the fabrication and the characterization of various types of HTS Josephson junctions manufactured using different processes: grain boundary junctions have been studied both by the way of junctions on bicrystal substrates and of bi-epitaxial junctions. Ramp-edge types have been elaborated and characterized using mainly N-YBaCuO thin film as a barrier while the trilayer approach has been investigated through a-axis structures. YBaCuO or GdBaCuO superconductive films, insulator layers, barriers, buffer and seed layers are deposited using inverted cylindrical magnetron (ICM) sputtering or pulsed laser deposition (PLD) techniques. Most of these junction configurations have been improved either on SrTiO₃, MgO, LaAlO₃ or on more conventional R-plane sapphire substrates. Technology process involving optical lithography and Ar ion beam milling are used up to two inch wafers (sapphire). Emphasis has been put on the optimization of the device processing procedures and their reliabilities in the aim of high temperature superconducting electronics.

Structural and morphological characterizations, SEM and TEM observations have been realized in order to improve the junction processes. All the obtained devices were electrically and optically tested including under applied microwaves (Shapiro steps), magnetic field diffraction and light irradiation (infrared detection). Most of the results evidence a resistively-shunted junction (RSJ) behaviour up to ≈ 77 K (except for very high current density values). Potentiality of each HTS thin film device structure will be comparatively discussed.