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Collapse and large signal modelling of GaAs field effect transistors at 77 K

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Abstract- A complete electrical characterization of different types of GaAs field effect transistors at liquid nitrogen temperature is performed. The trapping-detrapping mechanisms on deep levels are particularly addressed and a method is proposed to circumvent the collapse phenomenon which otherwise limits the electrical performances. From these measurements a HEMT non-linear model is extracted and is found efficient for the prediction of the large signal power out versus power in characteristic of a cooled HEMT. A further application could be the optimized design of a cooled low phase noise oscillator.

1-Introduction

The sharing of the microwave bandwidth for telecommunication applications has enhanced the need for high spectral purity microwave sources. Cryogenically cooled microwave oscillators [1] could be an answer to this problem thanks to the availability of very high quality factors resonators at low temperatures, such as sapphire-superconductor resonators [2]. However the optimized design of such an oscillator requires a non-linear model of the cooled active microwave device which is not available yet. FET's show enhanced electrical performance under cooling and therefore are thought to be the best devices for such an application. However they are subject to trapping-detrapping phenomena on deep levels which may considerably degrade the expected performance. This phenomena must be considered at the time of modelling and this paper deals with this type of modelling performed on different commercial FET devices at liquid nitrogen temperature.

2- Collapse Preventing for Low Temperature Electrical Characterization

The different devices under test, a conventional GaAs MESFET, two AlGaAs/GaAs HEMT and two AlGaAs/InGaAs pseudomorphic HEMT, are placed into a 50 Ω microstrip chip carrier. These devices are characterized at 77 K with respect to their DC and pulsed drain current characteristics and microwave small signal S parameters. As shown on Figure 1, in complete darkness, the DC analysis demonstrates that the HEMT device is dramatically affected by the temperature : at drain to source voltages less than about 1 V a typical collapse of *I-V* characteristics occurs [3,4,5]. This anomalous behaviour disappears under conditions of white light illumination [4]. Many authors have reported that the collapse strongly depends on the bias history at low temperature and that the effect of a drain stress is predominant [5,6]. On Figure 1, the DC

characteristics in the dark have been obtained after an initial plot at $V_{gs} = 0V$ sweeping the drain voltage from $0V$ to $V_{dmax} = 2.5V$. It can be observed that such a stress induces a severe collapse.

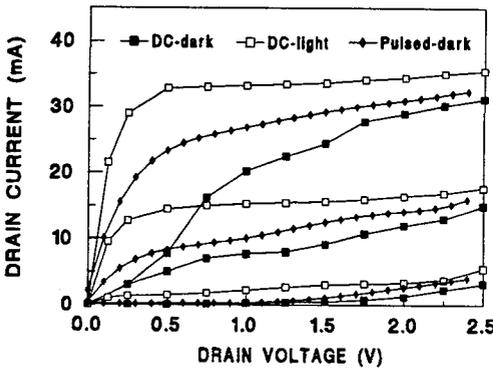


Figure 1 : HEMT Drain current curves for V_{gs} values of $0V$, $-0.2V$ and $-0.4V$ at low temperature ($77 K$)

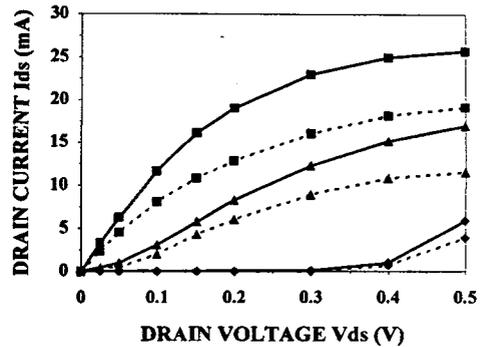


Figure 2 : HEMT current-voltage curves at $V_{gs} = 0V$ (solid line) and $V_{gs} = -0.1V$ (dashed line). Bias stress : \blacksquare - $V_{ds} = 3V$, $V_{gs} = 0V$; \blacktriangle - $V_{ds} = 2V$, $V_{gs} = 0V$; \blacklozenge - $V_{ds} = 1V$, $V_{gs} = 0V$. Stress time : five minutes.

On Figure 2, the stress conditions are varied, the drain voltage is maintained at a value V_{stress} ($V_{stress} = 1V$, $2V$ or $3V$) during a stress time of $5mn$. The corresponding drain current characteristics in the ohmic region are shown in Fig. 2 for these three different stress. The device exhibits severely distorted $I-V$ characteristics mainly if the stress drain voltage is $1V$. On the contrary for a drain bias stress equal or higher than $3V$ a total collapse-recovery phenomenon is clearly observed. As extensively described by *Hori et al* [6], the collapse state and the recovery state can be switched to each other simply by changing the value of the stress drain voltage. Figure 3 shows the collapse enhancement versus stress time ($V_{stress} = 1V$, $V_{gs} = 0V$). The collapse is evaluated through the drain current amplitude measured at a fixed drain voltage of $40 mV$. This drain current dramatically decreases (Fig. 3) as the stress time increases and a full collapse is observed for a stress time in excess of $2 mn$. On the contrary a DC stress of $V_{stress} = 3V$, ($V_{gs} = 0V$) induces quite immediately the recovery. We have also observed a similar behaviour in some pseudomorphic HEMTs (PHEMTs). Figure 4 represents the drain current characteristics (V_{gs} varied from $0V$ to $-0.3V$, step $0.1V$) for a PHEMT device after an initial bias stress ($V_{ds} = 1V$, $V_{gs} = 0V$) applied during a stress time of $5mn$. However two important features must be noticed :

- In PHEMTs the collapse is much less pronounced and only appears if the stress drain and gate voltages are chosen at around $1V$ and $0V$, respectively (as an example, see the first curve $V_{gs} = 0V$).
- If V_{dmax} is above the kink voltage value which can be evaluated from the $I-V$ characteristics to be about $V_{kink} = 1.5V$ (Figure 4) no significant further collapse can be observed (curves $V_{gs} = -0.1V, -0.2V, -0.3V$).

The origin of the collapse is generally attributed to the existence of electron trapping on the DX centers which are deep donor levels located in the n-AlGaAs layer. The recovery phenomenon has been presented as the result of an impact ionization process [6,7]. Following, this hypothesis, when the electric field is sufficiently high, an impact ionization of hot electron occurs in the high-field channel region and generates holes which flow along the electric field lines and are collected at the

gate electrode. Consequently, a dramatic enhancement in the gate current is expected. This expectation has been verified on each of the devices under test and an example of gate current variation versus drain to source voltage V_{ds} is illustrated in Figure 5 for pseudomorphic HEMT's. The enhancement in the gate current at around $V_{ds} = 1.5V$ clearly indicates that the most of holes generated by impact ionization are swept towards the gate. Since the hole concentration increases rapidly and the hole capture cross section of DX center being about several orders of magnitude larger than the electron capture cross section of DX center [8], the traps ionization probably results from this hole current.

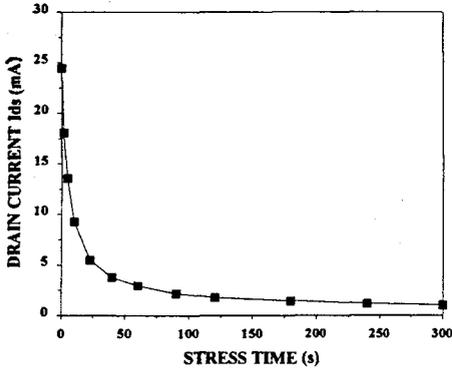


Figure 3 : Drain current I_{ds} versus stress time for HEMT device. Bias stress : $V_{ds} = 1 V$, $V_{gs} = 0 V$

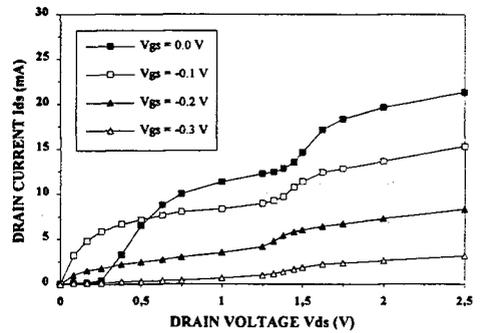


Figure 4 : PHEMT current-voltage characteristics at low temperature (77K)

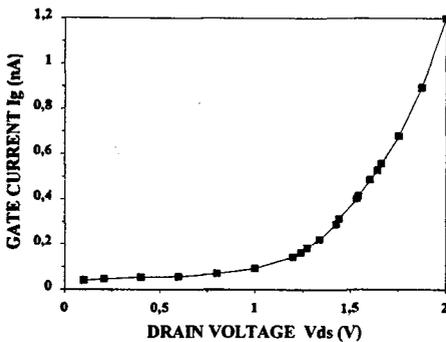


Figure 5 : Gate current versus drain-source voltage V_{ds} for a V_{gs} value of $-0.3 V$ at 77K

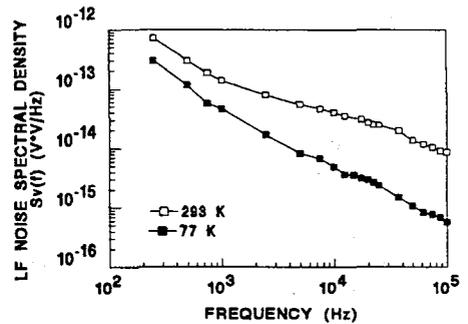


Figure 6 : HEMT input LF voltage noise generator. DC bias : $V_{ds} = 2V$, $V_{gs} = -0.1V$

Finally some practical essential consequences must be inferred from the previous results. Firstly the quiescent point (V_{ds} , V_{gs}) of any cooled device operated in a non-linear circuit must be carefully chosen so that V_{ds} is well above the kink voltage ($V_{kink} \cong 1.5V$, $V_{ds} > 2V$ or $3V$ in HEMTs, $V_{ds} \geq 2V$ in PHEMTs). Secondly the non linear modelling of this device has to be performed from I - V pulsed characteristics i.e by superimposing pulses on the DC bias.

Indeed the pulsed drain current characteristics of the HEMT device (obtained in the dark with a pulse width of 500 ns and a DC bias of $V_{ds} = 2V$, $V_{gs} = -0.1V$) reported on Figure 1 shows that a drain bias of 2V is sufficient to prevent any persistent collapse. Moreover, the pulse width does not affect the measurement since no change is observed on the curves with pulse width ranging from 500 ns to 10 ms. At ambient temperature, the low frequency dispersion phenomena are linked to the trapping/detrapping processes. At low temperature, this parasitic behaviour is largely reduced and if the collapse can be avoided, the trapping is no longer a problem. Consequently such devices are well suited for a high frequency use at low temperature, even in the dark.

The same behaviour is observed in PHEMTs. However, in these devices the recovery is complete at 2V and no further increase of the current is observed beyond that point. This is the major difference with AlGaAs/GaAs HEMTs where the recovery is often incomplete until much higher drain voltages such as 3V or 4V. However, in both cases, a quiescent point chosen above the kink effect leads to steady pulsed characteristics and a complete modelling of the device can be performed.

3- High frequency and noise 77K measurements

The high frequency measurements performed on one of the HEMT devices have shown good performance at low temperatures : a 20% increase of the transconductance parameter and 30% increase of the current-gain cutoff frequency were observed when cooling the device from 300 K to 77 K. The first PHEMT we studied at high frequency has demonstrated a lowering of the small signal gain, but this must not be seen as a general behaviour especially for more recent devices. With regard to the MESFET, even if better performance is obtained at cryogenic temperature, the measured cutoff frequency is not as large as for the HEMT's. For these reasons a HEMT device has been selected for further investigations.

Since the phase noise of a transistor oscillator largely depends on the device low frequency noise, the assessing of this noise is a prerequisite before any design. Therefore the frequency dependence of the input referred LF noise voltage generator at 300 K and 77 K for the same DC bias than used for the pulsed measurement is displayed on Figure 6. It is clearly seen from our experimental results that the LF input noise voltage is sensibly reduced in the upper frequency range (-11 dB at 100 kHz) when cooling the device. Indeed, the trap time constants greatly increase with decreasing temperature and produce a shift of the generation-recombination noise bulge toward the low frequency range [1]. Additionally we expect that the excess input referred current noise produced by impact ionization and the related gate current in the nA range will not influence the overall noise performance but this point will have to be further investigated.

Finally, these results demonstrate that this HEMT device could be well suited for a low phase noise oscillator design at low temperatures when an accurate large signal model is available.

4 Large signal device modelling

The large signal model of the HEMT device at cryogenic temperature has been successfully obtained from the pulsed I - V measurement using the fitting facilities of the HP-MDS simulator software.

Three essential nonlinearities have been considered in this model :

- The drain current generator described by TAJIMA's expressions [9].
- The gate diode current and its effect on the maximum gate voltage excursion.
- The gate capacitance nonlinearity.

However, this model is not appropriate to describe the decrease of the transconductance observed beyond $V_{gs} = 0$ V. Consequently, we have modified the TAJIMA's model using a polynomial function of V_{gs} which overcomes this drawback. A comparison between measured and modelled current voltage curves is shown on Figure 7 for this model.

Measured and modelled output power variations versus input power at 4 GHz frequency are displayed on Figure 8. A good agreement is observed between the modelled and the measured data both at 300 K and 77 K.

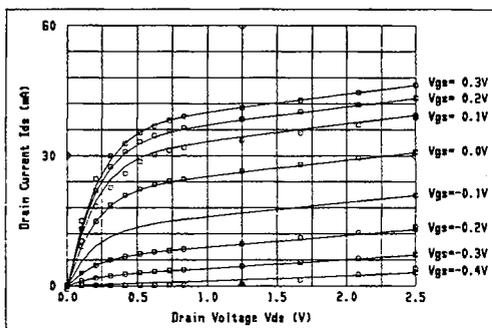


Figure 7 : Pulsed I - V measured and modelled data for a DC bias of $V_{ds} = 2$ V, $V_{gs} = -0.1$ V at low temperature

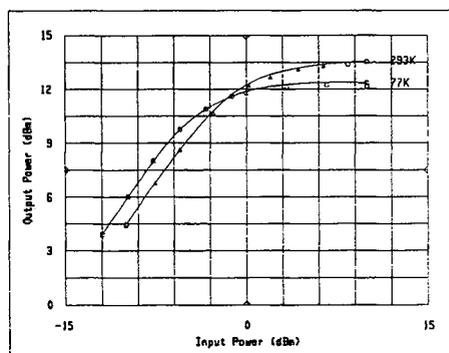


Figure 8 : HEMT output power versus input power at 293 K and 77 K at 4 GHz. DC bias : $V_{ds} = 2$ V, $V_{gs} = -0.1$ V. Measured (dots) and modelled (lines) data.

5- Conclusion

We have reported that the commonly observed collapse which limits cooled heterojunction FETs devices electrical performance can be prevented, even in the dark, using appropriate bias conditions corresponding to a drain voltage V_{ds} beyond the kink voltage. As an illustration a large signal model of AlGaAs/GaAs HEMT's has been successfully implemented from pulsed measurements performed at liquid nitrogen temperature and in darkness. The good agreement observed between power out versus power in simulated and measured data substantiates our findings. Finally, such a model will be used for microwave cryogenic circuits CAD and, together with low frequency noise data reported in this paper, will help to understand of noise conversion processes in oscillators.

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