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On the determination of the effective channel length of MOSFETS

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ABSTRACT: The conventional method used to determine ΔL , the processing induced channel length shortening in MOSFETs at room temperature gives invalid results at 77 K. This error is found to result from the incorrect assumption that the channel resistance is a linear function of effective channel length for the values of gate overdrive normally used for the extraction of ΔL . By restricting gate voltages to the range where this assumption is shown experimentally to be valid, values of ΔL extracted at 77 K are smaller than those extracted at room temperature. This attributed to the reduced source-channel and drain-channel depletion region widths at 77 K at and above threshold.

1. INTRODUCTION

While procedures have been developed to measure ΔL , the difference between the drawn or mask length L_m and the effective channel length L at room temperature, at 77 K the data are scattered, often with a negative ΔL extracted. This result is physically unreasonable since it implies that L is greater than L_m . The value of ΔL is extracted from a comparison of measurements with the expression for channel current I_D , which is assumed to be valid in the limit of small drain-source voltage V_D (linear region) for $V_G > V_T + V_D/2$

$$I_D = \frac{WC_{ox}\mu_f}{L}(V_G - V_T - \frac{V_D}{2})(V_D - I_D R_T) \quad (1)$$

where W is channel width, C_{ox} is gate oxide capacitance per unit area μ_f is average channel carrier mobility at low channel fields, L is channel length, V_G is gate-source voltage, V_T is threshold voltage and $R_T = R_S + R_D$, with R_S assumed equal to R_D as expected from symmetry.

From (1) the total device resistance $R_m = V_D/I_D$ for a device of mask length L_m can be written.

$$R_m = R_T + \mathcal{F}(L_m - \Delta L) \quad (2)$$

where for a given (small) V_D ,

$$\mathcal{F} = [WC_{ox}\mu_{if}(V_G - V_T - \frac{V_D}{2})]^{-1} \quad (3)$$

with W , C_{ox} and μ_{if} assumed to be independent of channel length. The dependence of V_T on L is taken into account by measuring the threshold voltage for each device. The function \mathcal{F} then for a fixed V_D is assumed to be independent of L and a function of only gate overdrive ($V_G - V_T$).

To determine R_T and ΔL , which are assumed to be independent of L_m for a given technology, plots of R_m as functions of L_m for constant W and V_D are made for given values of ($V_G - V_T$), well above threshold (to reduce any errors in the extraction of V_T). We see then from (2), that these plots are expected to be straight lines that intersect at $R_m = R_T$ and $L_m = \Delta L$, [1-3]. This method, appears to give reliable values of R_T and ΔL at room temperature for devices with channel lengths greater than about one μm . At low temperatures, however, the $R_m - L_m$ plots do not intersect at a single point. If an average value of the intersections is taken, the value of ΔL extracted is often negative, implying that the actual channel length is greater than the mask length [4,5], a result that is difficult to explain physically. In this paper we refer to the above technique to determine ΔL and R_T as the conventional method.

It has been suggested that the failure of the conventional method at 77 K results from an inaccuracy in the determination of V_T by the maximum slope method [6]. The error is thought to result from the large dependence of μ_{if} on V_G and the relatively large influence of R_T on the $I_D - V_G$ curves. To overcome this potential problem, a shift and ratio (S&R) method was developed [5]. If R_T is independent of V_G , taking the derivative of (3) with respect to V_G gives for a device i

$$S_i = \frac{\partial R_{mi}}{\partial V_G} = 0 + \frac{\partial \mathcal{F}}{\partial V_G} (L_{mi} - \Delta L) \quad (4)$$

where $\partial \mathcal{F} / \partial V_G$ is a general function of gate overdrive common to all devices on the test chip. Using a long channel device as reference such that $L_{mo} \gg \Delta L$, S_i can be shifted in V_G (to compensate for the difference in V_T) until the ratio of S_i/S_o is constant. Here S_o and L_{mo} refer to the reference device. Then from (5) ΔL is obtained

$$\Delta L = L_{mi} - L_{mo} \left(\frac{S_i}{S_o} \right) \quad (5)$$

We have modified the S&R method such that a long channel reference device, while convenient, is not required. We also plot the data somewhat differently such that a better physical insight can be obtained, especially in the region well above threshold where the conventional method is used. Plots of S_i are moved horizontally and vertically with respect to S_o until S_i and S_o coincide. The horizontal displacement is then equal to the difference in V_T of the two devices while the vertical displacement (log scale) gives the ratio of S_i/S_o . Then for coincidence,

$$\frac{S_i}{S_o} = \frac{L_{mi} - \Delta L}{L_{mo} - \Delta L} \quad (6)$$

For a given reference device, $(L_{mo} - \Delta L)$ is a constant and a plot of S_i/S_o against L_{mi} gives a straight line. Extrapolating to $S_i/S_o = 0$ gives $L_{mi} = \Delta L$. These results are then checked by plotting $(L_{mo} - \Delta L) S_i/S_o$ vs. L_{mi} to verify that the slope of this graph is a straight line of unity slope as expected (Eq. 6).

2 EXPERIMENT

The devices used in this study were fabricated with CMOS technology for room temperature operation. The average net doping in the channel region is about 10^{17}cm^{-3} . The source and drain junctions are abrupt (non-LDD) and thus the variation of R_T on V_G is expected to be negligible. The gate material is n^+ polysilicon which results in "buried channel" PFETs. Because of the freezeout of channel holes onto the acceptors implanted for threshold control, the electrical characteristics are not given by (1) at 77 K. Thus only NFETs are discussed here. In this work devices with mask width of $20\ \mu\text{m}$ were used. Mask channel lengths of $0.6\ \mu\text{m}$ to $20\ \mu\text{m}$ were tested and nominal gate oxide thickness is $15\ \text{nm}$.

Data were taken at room temperature and at 77 K (immersed in liquid nitrogen) with the aid of a computer-controlled Hewlett Packard Transistor Parameter Analyzer model 4145A. Plots of S_i vs. V_G were made using similar vertical scales (decades/cm) and horizontal scales (V/cm) such that they could be moved horizontally and vertically with respect to each other to obtain coincidence.

3. RESULTS

Figure 1 shows the room temperature S_i data as a function of V_G shifted to obtain coincidence for the longest ($L_m = 20\ \mu\text{m}$) and shortest ($L_m = 0.6\ \mu\text{m}$) n-channel devices. Reasonable coincidence occurs for the range of V_G from about 0.4 V above threshold to about 5 V. The range of coincidence extends to lower values of V_G as the channel lengths approach each other.

Similar plots are shown for these same NFETs at 77 K in Figs. 2. We can see that coincidence is obtained from just below threshold to about 1.1 V above threshold. We can also see that with increasing gate overdrive the deviation from coincidence becomes larger.

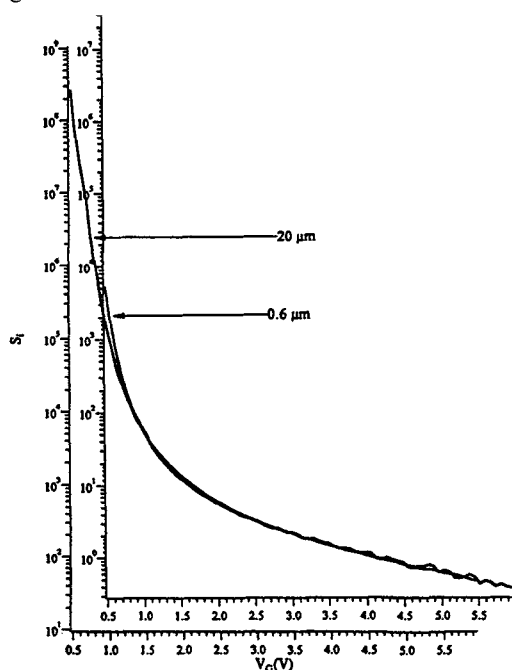


Fig. 1. Plot of S_i as functions of V_G for n-channel devices with mask lengths of 0.6 and $20\ \mu\text{m}$: The plots are shifted horizontally and vertically to obtain coincidence.

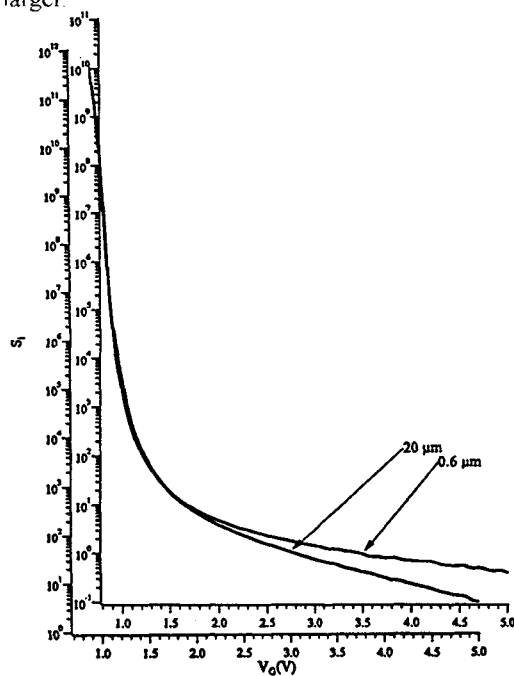


Fig. 2. Plots S_i vs. V_G at 77 K for the devices of Fig. 1.

A plot of S_i/S_0 for n-channel devices in the region of coincidence using the $20\ \mu\text{m}$ device as

reference is plotted in Fig. 3 for room temperature. A least-square fit to a straight line gives $\Delta L = 0.36$ V. This is close to the value of 0.32 V obtained by the conventional method.

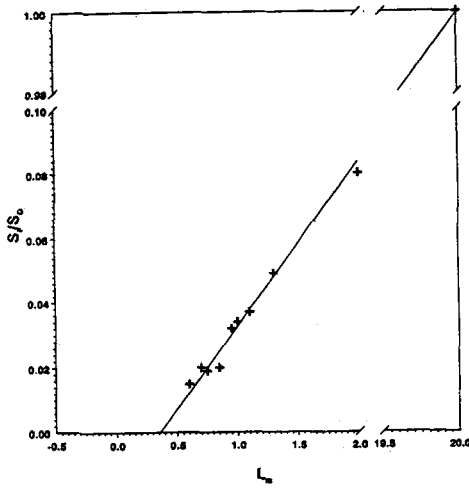


Fig. 3. Plot of S/S_0 vs. L_m with $L_m = 20 \mu m$ as reference. The L_m intercept is the extracted value of ΔL .

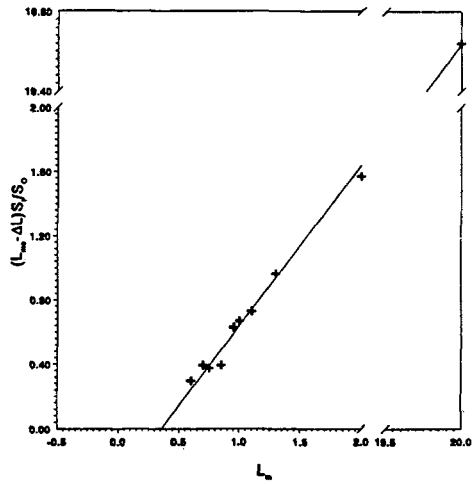


Fig. 4. Plot of $(L_{m0} - \Delta L) S/S_0$ vs. L_m for room temperature. The L_m intercept indicates ΔL . The slope is near-unity as expected.

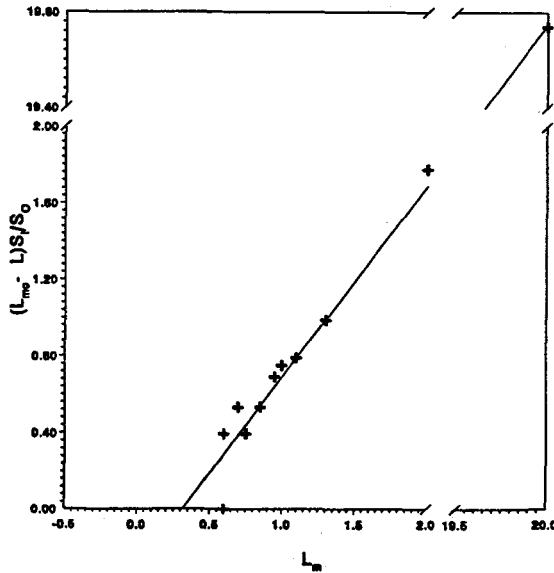


Fig. 5. Plot of $(L_{m0} - \Delta L) S/S_0$ vs. L_m for 77 K. As for room temperature, the L_m intercept yields ΔL and the slope is close to unity.

Figure 4 shows the room temperature plot of $(L_{m0} - \Delta L) S_i/S_o$ as a function of L_m . The slope is 1.01, close to the expected value of unity. A similar plot at 77 K is shown in Fig. 5 yielding $\Delta L = 0.32 \mu\text{m}$ and a slope within one percent of unity. We note that this value is 0.04 V less than at room temperature. We also note that the conventional method for this case did not give meaningful results because the plots of R_m vs. L_m for different gate overdrive of 1, 2, 3, and 4 V did not intersect at believable values of R_T and ΔL .

4. DISCUSSION AND CONCLUSIONS

Both the conventional and S&R methods of ΔL extraction depend on the function \mathcal{F} and thus $\partial\mathcal{F}/\partial V_G$ being a general function of gate overdrive common to all devices of a given technology and independent of channel length, and R_T being independent of gate voltage. These assumptions are clearly valid at room temperature for the devices tested for $V_G > V_T$ as can be seen from Fig. 1. Thus both methods are expected to be valid. The values of ΔL extracted, 0.36 and 0.32 μm respectively for the S&R and conventional methods respectively are within experimental accuracy of each other.

We see then from Fig. 2 however, at 77 K coincidence can not be obtained for NFET's in the region appreciably above threshold indicating that $\partial\mathcal{F}/\partial V_G$, and thus \mathcal{F} , are not independent of channel length as assumed, at least at these values of V_G . Since the conventional method relies on data from this range of V_G , it is not surprising that it fails at this temperature. The extracted value of ΔL is 0.04 μm less at 77 K than at room temperature. This is in good agreement with the value of 0.045 μm calculated considering the reduced source-channel and drain channel depletion regions at and above threshold [7].

Both the conventional and shift and ratio methods are valid at room temperature for the measurement of ΔL . It is found that the failure of the conventional method at 77 K results from the assumption that the channel resistance per unit channel length is a unique function of overdrive and independent of channel length. This assumption is shown to be incorrect in the region of overdrive voltage which is normally used in this method. The S&R method is valid at this temperature because it is restricted to gate overdrive values where the above assumption is shown experimentally to be valid.

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References:

- [1] Ng K. K. and Brews J. R., Circuits and Devices, (1990) pp. 33 - 38.
- [2] Terada K. and Muta H., Jap. J. Appl. Phys. **18** (1979) pp. 953-959.
- [3] Chern J. G. J. et al, IEEE Electron Device Lett. **EDL 1** (1980) pp. 270-274
- [4] Garcia M. et al, "Parameter extraction at liquid nitrogen temperature on short channel PMOS devices" Anais da VIII Congresso da Sociedade Brasileira de Microeletronica (1993) pp. VI.7-VI-12.
- [5] Taur Y. et al, IEEE Electron Devices Lett. **13** (1992) pp. 267-269
- [6] Jain S. Proc. Inst. Elec. **135-1** (1988) pp. 162-
- [7] Kamgar A, "Si MOS Devices at Low Temperatures", Proceedings of the Cold Electronics Workshop, Pasadena 4-5 October 1984 pp 83-91.