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Study of saturation velocity overshoot in deep submicron silicon MOSFETS from liquid helium up to room temperature

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Abstract : The electron saturation velocity in Silicon MOS transistors with channel lengths in the range 0.1–0.8 μm is studied for temperatures between 4.2K and 300K. A new method for the evaluation of the saturation velocity in a MOS transistor is presented. This method enables the drift velocity at source end of the device to be determined as a function of the corresponding electric field. The results obtained by this new method are compared to the ones obtained by classically used techniques and to literature data collected on resistive gated MOS devices.

1. INTRODUCTION

As the scaling down of Si MOS transistors proceeds, the device performance becomes more and more dominated by the carrier velocity saturation phenomenon [1-2]. Moreover, for very short channel devices, electron velocity overshoot is expected to take place for channel length below 0.1 μm [1,2].

In this work, the electron saturation velocity is investigated in Silicon MOS transistors with channel lengths in the range 0.1-0.8 μm for temperatures between 4.2K and 300K. For this purpose, a new method for the evaluation of the saturation velocity in MOS transistors is worked out. This procedure enables the drift velocity at source end to be determined as a function of the corresponding electric field.

2. SATURATION VELOCITY EXTRACTION METHOD

The drift velocity near source can be calculated from the $I_d(V_d)$ output characteristics measured at strong inversion after dividing the drain current by the inversion charge at source end such as :

$$v_{ds} = \frac{I_d}{W C_{ox} (V_g - V_t)} \quad (1),$$

where W is the channel width, C_{ox} is the gate oxide capacitance and V_t is the charge threshold voltage at source end (supposed to be independent of drain voltage).

The corresponding longitudinal electric field E_s at source end is obtained within the gradual channel approximation according to

$$E_s = I_{d0} / (L G_d) \quad (2),$$

where G_d is the ohmic conductance, L the channel length and $I_{d0}(V_d)$ is the drain current of the device in the absence of velocity saturation effect.

Noticing that the drain current in strong inversion is a function of the gate voltage drive $V_g - V_t$, the drain current in the absence of velocity saturation effect can be calculated from the experimental ohmic conductance transfer characteristics as

$$I_{d0}(V_d) = \int_0^{V_d} G_d(V_g - \Phi) d\Phi \quad (3).$$

Using this method, it is therefore possible to assess the variation of the source drift velocity as a function of the corresponding electric field after changing the drain voltage from linear to saturation regions.

The saturation velocity is then extracted as is usual from the non linear behavior of the drift velocity with electric field employing the empirical fitting expression [3] :

$$v_{ds} = \frac{\mu E_s}{[1 + (E_s/E_c)^\alpha]^{1/\alpha}} \quad (4),$$

where μ is the low field mobility, E_c is a critical field and a α fitting exponent generally ranging between 2 and 5. The saturation velocity v_{sat} is then deduced from the critical field as $v_{sat} = \mu E_c$.

Our method is therefore well different from the classical procedures which are based on the MOSFET saturation parameters such as the transconductance g_{msat} , the saturation drain current I_{dsat} and the saturation drain voltage V_{dsat} using the following relations [1,4,7] :

$$g_{sat} = W C_{ox} v_{sat} (1 - dV_{dsat}/dV_g) \quad (4a),$$

and

$$I_{dsat} = W C_{ox} v_{sat} (V_g - V_t - V_{dsat}) \quad (4b).$$

It should be noted that, with our procedure, the saturation velocity in an actual short channel MOSFET is extracted as in the case of resistive gated MOS devices [3,6].

3. RESULTS AND DISCUSSION

The devices used in this study are conventional Silicon N MOS transistors fabricated with electron beam lithography and having a gate oxide thickness of 50Å. The channel doping of the order of $3 \times 10^{17}/\text{cm}^3$ is high enough in order to prevent short channel effect. Shallow source and drain extensions have been realized by Arsenic implantation ($2 \times 10^{15}/\text{cm}^2$, 20keV).

The static drain current characteristics were measured with a Keithley 236 system while the devices mounted in 24 pin dual-in-line package were placed into a liquid helium cryostat from Lakeshore-Cryophysics.

Fig. 1 shows typical variations of the drift velocity v_{ds} with the electric field at source end while varying the drain voltage from linear to saturation region for various gate lengths. Note the increase of the velocity for the shortest device.

Rel. 4 has then been used to extract the saturation velocity. For that, the best fitting parameters E_c and α have been obtained by plotting the quantity $Y = (E_s/V_{ds})^\alpha$ as a function of E_s^α . Fig. 2 gives an example of such characteristics for various temperatures. The values of α have been found in the range 4-6 in agreement with data obtained at room temperature on resistive gated MOS devices [5,6].

In Fig. 3 are reported typical variation of the saturation velocity v_{sat} with temperature for the case of "long" channel device ($L=0.8\mu\text{m}$). Note the increase of the saturation velocity as the temperature is lowered. For comparison purpose, the results obtained by Fang and Fowler [4] and Takagi and Toriumi [3] are also displayed.

In Fig. 4 are presented the variation of the saturation velocity v_{sat} as a function of channel length for several operation temperatures. Note the substantial increase of the saturation velocity as the device are scaled down. For the shortest device ($L=0.1\mu\text{m}$), the saturation velocity can exceeds 10^7cm/s . This could be attributed to the velocity overshoot effect resulting from non stationary transport at very short channel length [1,2]. Nevertheless, it should be noted that the maximum saturation velocity values found here are somewhat lower than those reported by Shahidi et al [1] (see Fig. 5 for comparison).

In Fig. 6 are also given for comparison the saturation velocity v_{sat} versus temperature as obtained from our procedure and using the classical method based on the exploitation of the MOSFET saturation parameters (Rels. 4). As is clear from this figure, the classical method does overestimate the saturation velocity and even provides incorrect trend at low temperature. This could be due to the inadequacy of the saturation MOSFET equations employed for extracting the velocity saturation. In our case, only the source parameters are used and are therefore much less subjected to inaccuracy than the corresponding drain ones.

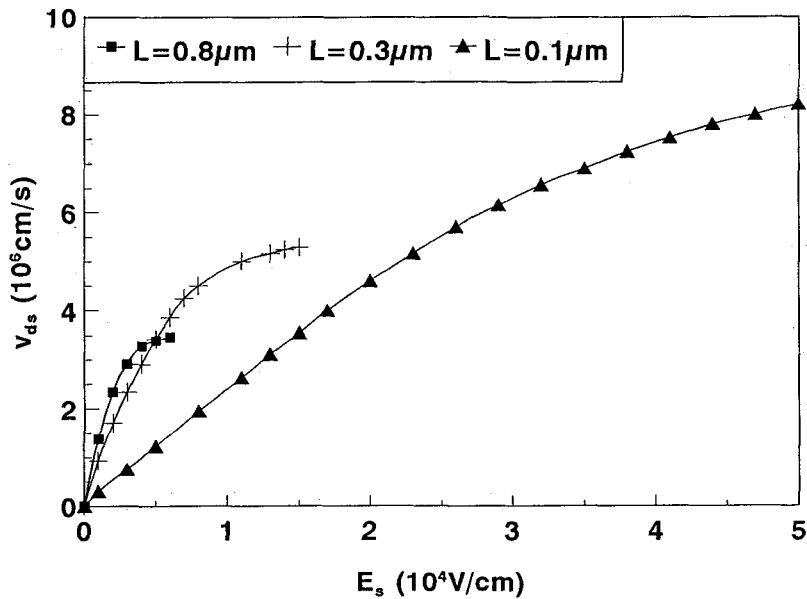


Fig. 1 : Variation of drift velocity versus electric field at source ($T=300\text{K}$).

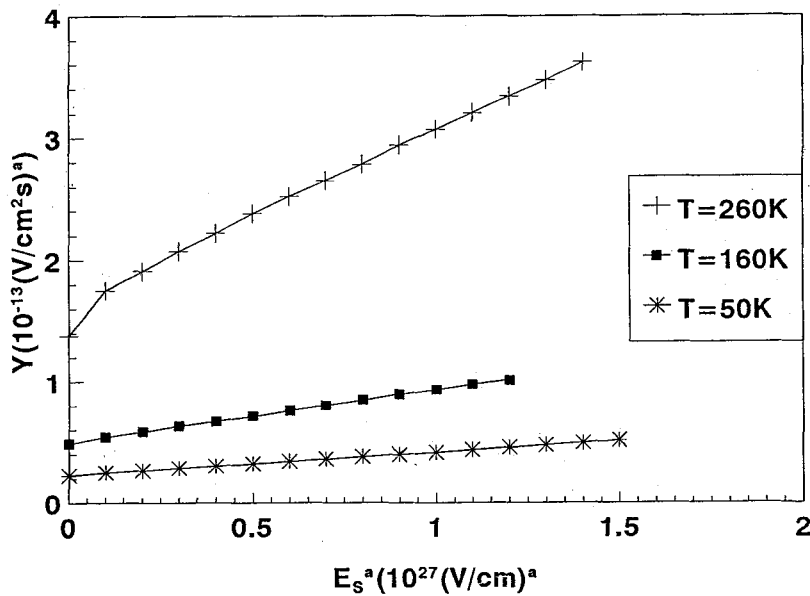


Fig. 2 : Variation of the function $Y=(E_s/V_{ds})^a$ with E_s^a for various temperatures ($V_g=2\text{V}$, $L=0.3\mu\text{m}$).

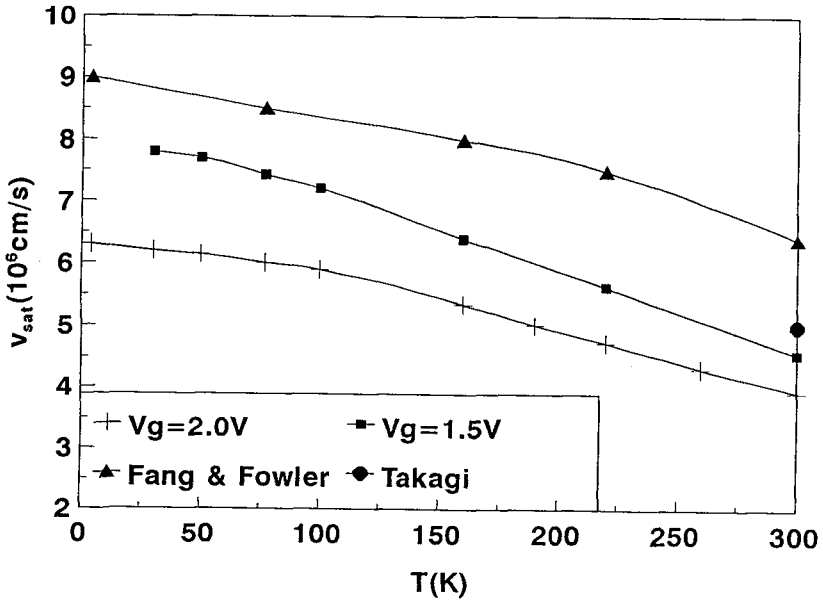


Fig. 3 : Variation of the saturation velocity with temperature as obtained for two gate voltages ($L=0.8\mu m$). Results obtained by Fang and Fowler [4] and Takagi and Toriumi [3] are also shown.

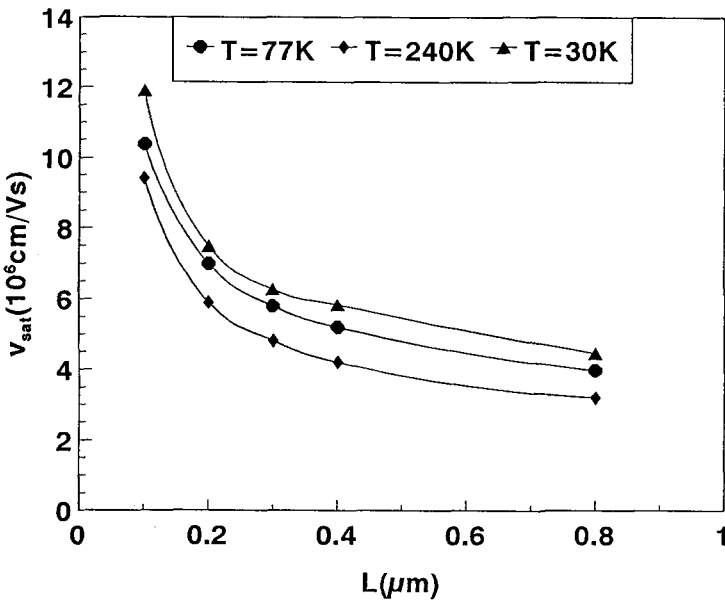


Fig. 4 : Variation of the saturation velocity with channel length for several temperatures as obtained by our method ($V_g=1.5$ V).

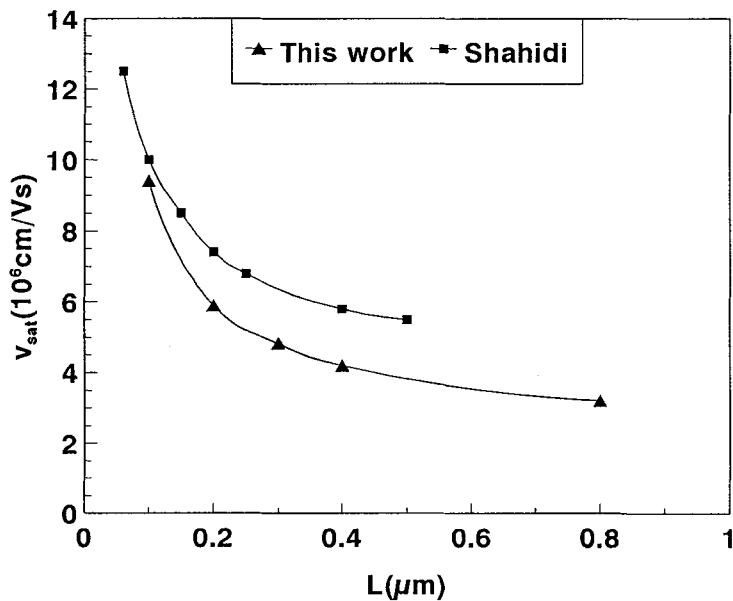


Fig. 5 : Variation of the saturation velocity with channel length as obtained on our devices and after Shahidi et al [1] at room temperature.

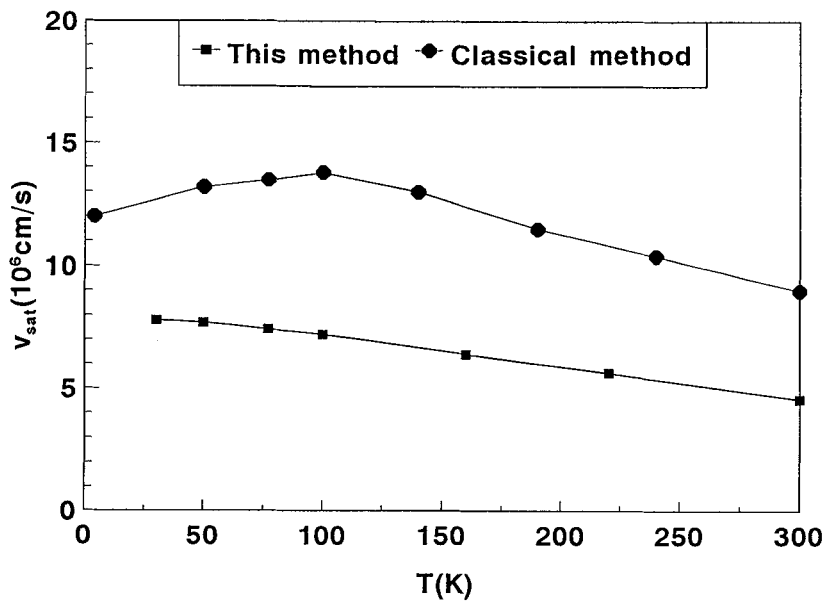


Fig. 6 : Variation of the saturation velocity with temperature as obtained with our procedure and using the classical method based on Rel. 4 ($L=0.3\mu\text{m}$, $V_g=1.5\text{V}$).

4. CONCLUSION

The electron saturation velocity in Silicon MOS transistors with channel lengths in the range 0.1-0.8 μm has been studied for temperatures between 4.2K and 300K. A new method for the evaluation of the saturation velocity in a MOS transistor has been worked out. This procedure enables the drift velocity at source end of the device to be determined as a function of the corresponding electric field. The results obtained by this new method have been compared to the ones obtained by classically used techniques and inferred by the comparison to literature velocity saturation data collected on resistive gated MOS devices.

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