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Performances and physical mechanisms in sub-0.1 μm gate length LDD MOSFETs at low temperature

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Abstract: The electrical properties of sub-0.1 μm gate length LDD devices are investigated between room and liquid helium temperatures. The strong impact of gate overlapping effects on LDD resistance is shown for these ultra-short channel MOSFETs in a wide temperature range. It is experimentally demonstrated that these mechanisms lead to a substantial enhancement of the driving current when the devices are scaled down, and induce an additional improvement in the case of low temperature operation. Furthermore, the performances of these transistors with LDD structure at low temperature are also discussed in terms of field assisted impurity ionization in the LDD's.

1. INTRODUCTION

LDD structures are very useful for deep submicron devices due to their capability of decreasing short channel and hot carrier effects. However, the series resistances associated with the LDD regions can be relatively large and harmful for very short channel MOSFET's, and thus can decrease substantially the driving current [1]. On the other hand, low temperature operation is very attractive in order to improve the device performances [2]. Nevertheless, freeze-out effects in the LDD's are supposed to alter significantly the benefits of a reduction of temperature, and very poor properties are expected for LDD MOS transistors at very low temperature. A recent study has shown that a satisfactory low temperature operation can be obtained for long channel LDD transistors due to field assisted impurity ionization in the LDD's [3].

Therefore, it is very valuable to evaluate the performances of very short channel devices as a function of temperature. We show in this paper that low temperature operation is very promising for the optimization of the electrical properties of sub-0.1 μm gate length LDD MOSFETs. A detailed study of the electrical characteristics between room and liquid helium temperature allow us to gain insight in the various physical mechanisms involved in the strong improvement of the performances of these devices in various temperature ranges.

2. RESULTS AND DISCUSSION

LDD MOSFETs with gate length ranging from 0.5 to 0.07 μm , fabricated according to a conventional NMOS process in conjunction with a direct write EB lithography and a two step ECR plasma etching, are studied in this work. Poly-Si side wall spacers have been used for these devices. The gate oxide thickness is 50 Å. Further details for the fabrication of these MOS transistors can be found in [4].

Figure 1 shows the $I_d(V_d)$ characteristics of 0.07 and 0.1 μm MOSFETs between 300 K and 20K. As exemplified in this figure, a substantial increase of the drain current is obtained by decreasing the temperature for gate voltages sufficiently high compared with the threshold voltages. It is worth noticing that these comparisons between room and low temperature are achieved for a constant gate bias, and, thus, the low temperature improvement would be even higher for a given $(V_g - V_t)$ due to the shift of the threshold voltage. On the other hand, a significant kink effect, which increases for the shortest device, can be clearly seen on these curves whatever the temperature is. The kink effect, very well known for SOI devices, has

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also been previously shown in the case of long channel bulk Si devices operated at very low temperature (≤ 40 K) in the strong freeze-out regime due to the high substrate resistance [5]. Recently, a kink effect has also been reported for single drain MOS devices in the $0.1 \mu\text{m}$ range for temperature as high as 77 K [6]. In our results, the kink effect is obtained even at room temperature for a drain bias lower than 2V , in particular for the $0.07 \mu\text{m}$ MOSFET's, highlighting the increase of the forward biasing of the source/substrate junction in the deep submicron regime.

In figure 2 are presented the transfer characteristics in linear operation for various channel lengths. A strong increase of drain current is obtained in the high gate voltage region, mainly for $T \leq 150$ K in the case of $0.1 \mu\text{m}$ gate length, and even at 300 K for the $0.07 \mu\text{m}$ gate length transistor. It is worth noticing that this behavior is also observed in the liquid nitrogen temperature range in the case of longer devices (between $0.15 \mu\text{m}$ and $0.5 \mu\text{m}$ in this study). Therefore, the excess drain current is enhanced and is obtained for higher temperature for the shortest devices.

Fig. 3a exemplifies the $I_d(V_g)$ characteristics for high drain bias in the case of the $0.07 \mu\text{m}$ MOSFET's. Similar behaviors as those for linear operation have been obtained as a function of gate voltage and temperature. In addition, the influence of V_d in the saturation regime is reported in figure 3b in the case of liquid nitrogen operation for the $0.07 \mu\text{m}$ MOSFET's. With increasing the drain voltage, a very sharp transition is obtained for lower gate bias. This phenomenon, which is also observed for V_d lower than 1.4V for which no kink is observed in the $I_d(V_d)$ characteristics, and even in linear operation, cannot be attributed to the kink effect. In fact, this original behavior is explained in terms of LDD accumulation and impact ionization phenomena. Indeed, fringing fields seem to be very important for these transistors with polysilicon spacers. Therefore, the gate induces a strong accumulation of the LDD regions, which can be observed even at 300 K for the shortest device for which the influence of the series resistances is very high. At low temperature, due to impurity freeze-out in the LDD's and thus to the increase of the series resistance R_{sd} , this effect can also be seen for longer devices. Furthermore, the gate voltage at which an excess I_d is obtained is shifted to higher values when the temperature is reduced due to the large change in the threshold voltage of the LDD's associated with the thick gate insulator under the polysilicon spacers (about 3 times the gate oxide thickness). On the other hand, by increasing V_d , a stronger field assisted ionization is obtained in the LDD regions which enhances the ionized impurity density and reduces the threshold voltage of the LDD's, inducing an excess current at lower V_g (Fig. 3b). This field assisted ionization can be attributed to shallow level impact ionization or/and Poole-Frenkel processes. Nevertheless, due to the strong dependence of the ionization on the drain current, as it will be shown below, we think that the main phenomenon is the shallow level impact ionization process.

These results show the strong impact of gate overlapping effects on the LDD resistance for MOSFET's in the sub- $0.1 \mu\text{m}$ gate length range. These mechanisms lead to a substantial enhancement of the driving current when the devices are scaled down, and induce an additional improvement in the case of low temperature operation.

Some transient and hysteresis effects, have also been observed in the case of low temperature operation. Figure 4 shows the $I_d(V_g)$ characteristics for a $0.1 \mu\text{m}$ MOS transistors in linear operation (Fig. 4a) and saturation (Fig. 4b) at 77 K. The various curves have been obtained for forward- and reverse- V_g -scans and for different integration times (medium, with an average value of 16 samples taken during 1 line frequency period, and long, with an average value of 256 samples taken during 16 line frequency periods, integration times of the HP 4145B, which leads to various acquisition times for each measured point). For both V_d values, a significant hysteresis effect is observed with a suppression of the sharp transition in the case of the reverse- V_g -scan. On the other hand, by using a medium integration time, a significant reduction of the drain current is obtained for a forward- V_g -scan, in particular at high drain biases, highlighting a substantial transient effect. The effect of integration time is very low for a reverse- V_g -scan.

It should be mentioned that significant transient effects have been reported previously for MOS devices operated in the liquid helium temperature range [7,8], but these effects are supposed to be very low at liquid nitrogen temperature, and no transient effect have been shown up to now in this temperature range. The previous drain current transients, shown for temperatures between 4.2K and 25K [7,8], have been attributed to the time required for the formation of the depletion region under the gate with strongly frozen-out impurities. An excess drain current has been obtained for these kinds of transients [7,8].

In this work, during the transient, the drain current is lower than the equilibrium value. This phenomenon is in fact attributed to the complex ionization processes of the frozen-out impurities in the LDD regions. With increasing the gate voltage, the LDD's are progressively accumulated, which induces a significant enhancement of the drain current. The increase of I_d and the decrease of the source-drain series resistance

which enhances the lateral electric field lead to a substantial ionization of the frozen-out impurities in the LDD's. This sole phenomenon should not give a significant transient time. However, another effect seems also to be important. In fact, the LDD regions behave like two accumulation-mode transistors near the source and the drain in series with the channel. For these accumulation-mode MOSFETs, it has been previously reported [9] that a strong impurity freeze-out can be induced at the Si/SiO₂ interface at 77K by increasing the gate bias. Therefore, various conflicting ionization and freeze-out effects occur in the LDD's at low temperature by increasing V_g . The surprising transient behavior in this temperature range are certainly due to these original low temperature features.

On the other hand, in the case of a reverse- V_g -scan, the impurities inside the LDD's, which are ionized at high gate voltages (the percentage of ionized impurities depending on V_d , but a large number of impurities being ionized even for low drain voltage for strong gate bias and drain current), are not frozen-out until very low gate voltage for both integration times. Therefore, a situation similar to the case of 300 K is observed in the LDD regions, with a very low threshold voltage. The hump in the $I_d(V_g)$ characteristics is thus suppressed, as in the case of room temperature operation for the 0.1 μm device.

In figure 5 are shown the output $I_d(V_d)$ characteristics for a 0.07 μm gate length MOSFET's at 77K obtained with long and medium integration times. A substantial transient effect is also observed in this figure. This transient is associated to the decrease of the source-drain series resistance which leads also to an enhancement of the effective gate voltage, which is similar to the case of the transient effect observed in the $I_d(V_g)$ characteristics. A higher drain current is obtained with long integration time, in particular for low gate bias. A double kink effect can also be clearly seen for low gate voltages. The second kink, which is the conventional kink due to the forward biasing of the source-substrate diode, was already observed in the case of medium integration time. The first kink is in fact attributed to the strong ionization of the LDD's when V_d is increased, which leads also to a larger slope in saturation. This ionization of LDD impurities is also underlined by the non-linear behavior of the curves at low drain voltage. For high gate voltage (3V) the transient effect is almost suppressed and the slope in saturation is rather low even for long integration time. This phenomenon is due to a strong ionization at lower drain voltages associated with the higher drain current at high V_g . It is also worth noticing that the transient effect is reduced for strong V_d .

Figures 6 and 7 present the hysteresis effects in the cases of reverse- V_g - and - V_d -scans, respectively. For a reverse- V_g -scan, a substantially higher drain current together with a reduction of the slopes of the $I_d(V_d)$ characteristics in saturation are obtained. The first kink is also significantly reduced. These effects are due to a strong ionization of the LDD's in the case of a reverse- V_g -scan until low gate voltages, and are correlated with the hysteresis observed in the $I_d(V_g)$ characteristics. At high gate or drain biases, these hysteresis effects are suppressed due to a strong ionization of the impurities inside the LDD's in both cases. In the case of a reverse- V_d -scan, similar behaviors as in the reverse- V_g -scan characteristics are obtained, with, in particular, a suppression of the first kink.

It should also be mentioned that, in the case of a reverse- V_d -scan in the $I_d(V_d)$ characteristics and in the case of a reverse- V_g -scan in the $I_d(V_g)$ characteristics, negative resistances are obtained for the first current points due to some transient effects which are reduced for long integration time.

For low gate voltage (2V), the non-linear variation at low V_d is suppressed because the current is not sufficiently high for the impact ionization process, but a strong slope is obtained in saturation for higher I_d and V_d associated with the beginning of the impact ionization process (Fig. 8). The strong kink effect observed for V_d higher than 1V is not a conventional kink for such a low drain voltage because the substrate current is almost equal to zero, but is in fact associated with a significant shallow level impact ionization of the LDD dopant impurities. For lower V_g (1.5V), this large slope in saturation is substantially reduced due to the further reduction of the drain current and thus of the ionization process in the LDD's (Fig.8).

Finally, it is worth noting that similar transient and hysteresis phenomena have been obtained in the liquid helium temperature range, with a magnification of the non-linear variation of the drain current for low drain voltage in the $I_d(V_d)$ characteristics. On the other hand, these effects are progressively suppressed when the temperature increases, and are strongly reduced for $T=150\text{K}$. These phenomena have not been observed at room temperature due to the full suppression of the freeze-out effects.

Furthermore, we have recently shown that the substrate current and the impact ionization rate are substantially reduced for these LDD devices operated at liquid nitrogen temperature [10]. Therefore, liquid nitrogen operation seems to be a very good candidate for the optimization of the electrical properties of sub-0.1 μm MOSFETs.

3. CONCLUSION

The electrical properties of sub-0.1 μm gate length LDD devices have been investigated from room to liquid helium temperatures. The dramatic impact of gate overlapping effects on LDD resistance has been shown for these ultra-short channel MOSFETs in a wide temperature range. It has been experimentally demonstrated that these mechanisms lead to a substantial enhancement of the driving current when the devices are scaled down, and induce an additional improvement in the case of low temperature operation. Furthermore, field assisted impurity ionization in the LDD's has been shown to increase significantly the performances of these transistors at low temperature. Moreover, transient and hysteresis phenomena, observed in a wide temperature range and associated with the ionization and freeze-out effects, have been highlighted.

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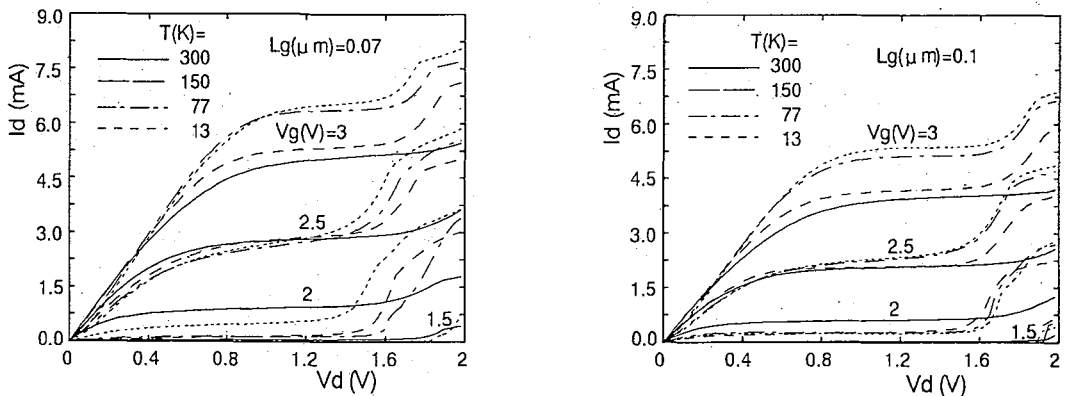


Fig. 1 : Drain current - drain voltage output characteristics for (a) a 0.07 μm MOSFET's and (b) a 0.1 μm MOSFET's in a wide temperature range.

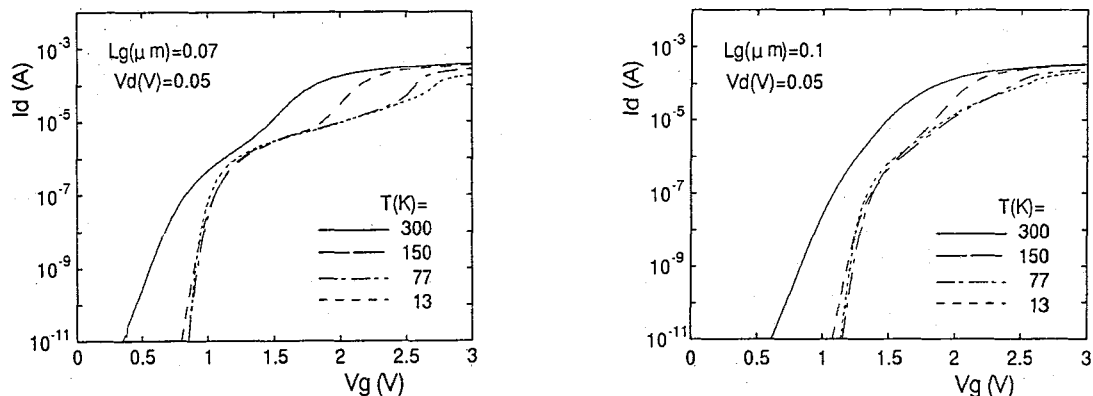


Fig. 2 : Drain current - gate voltage transfer characteristics for (a) a $0.07 \mu\text{m}$ and (b) a $0.1 \mu\text{m}$ MOSFETs in linear operation ($V_d=50\text{mV}$) as a function of temperature.

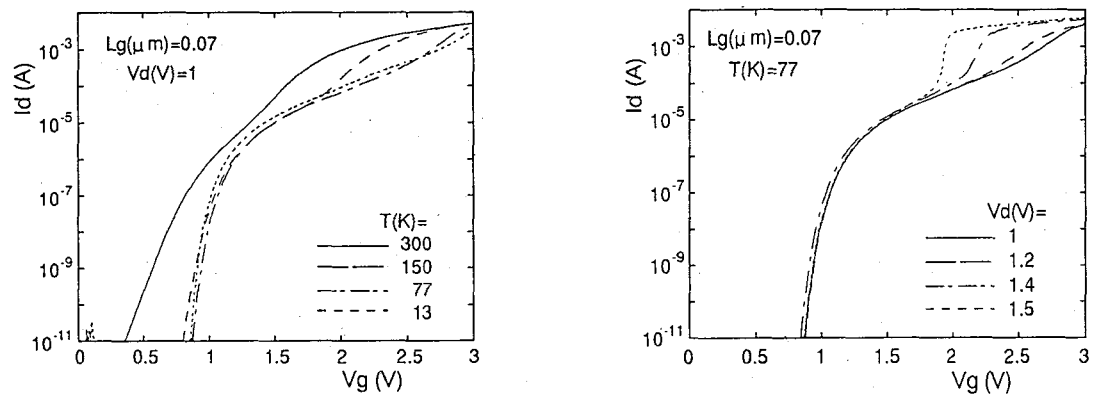


Fig. 3 : Transfer characteristics for the $0.07 \mu\text{m}$ gate length device (a) for various temperatures in the case of high drain bias ($V_d=1\text{V}$) and (b) for different drain voltages at 77K .

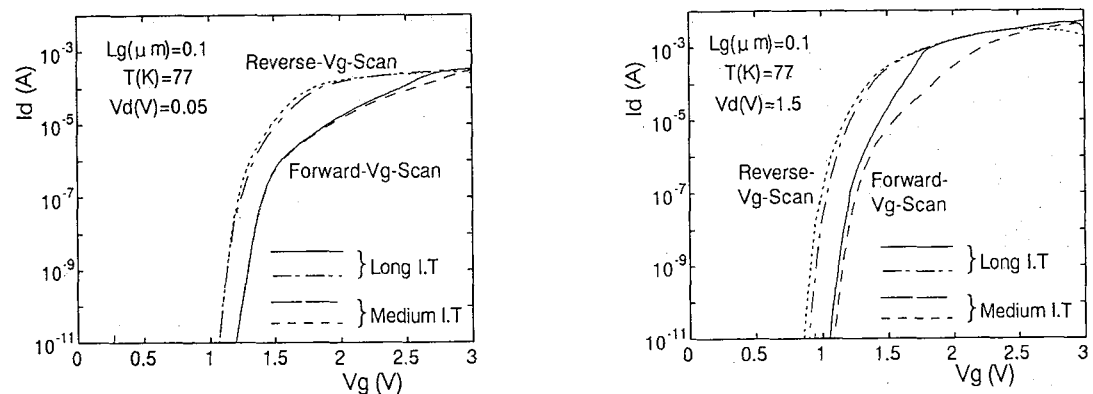


Fig. 4 : Drain current - gate voltage characteristics for a $0.1 \mu\text{m}$ gate length MOS device at 77K showing the transient and hysteresis phenomena, in the cases of (a) linear operation ($V_d=50\text{mV}$) and (b) saturation ($V_d=1.5\text{V}$).

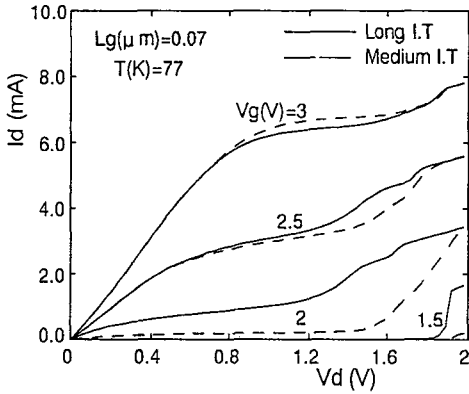


Fig. 5 : Drain current - drain voltage characteristics for a $0.07 \mu\text{m}$ MOS device at 77 K showing the transient phenomena.

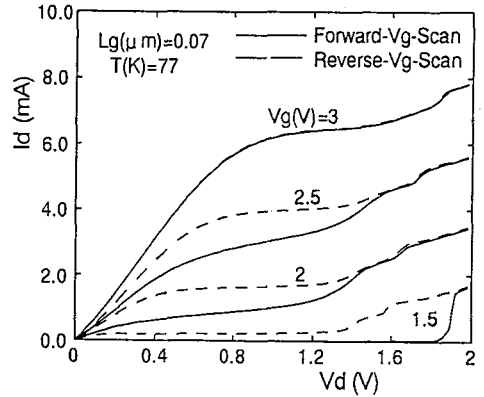


Fig. 6 : Drain current - drain voltage characteristics for a $0.07 \mu\text{m}$ MOS device at 77 K showing the hysteresis phenomena in the case of forward- and reverse- V_g -scans (These curves have been obtained with a long integration time).

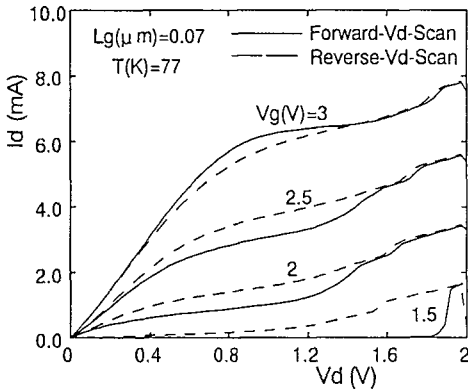


Fig. 7 : Drain current - drain voltage characteristics for a $0.07 \mu\text{m}$ MOS device at 77 K showing the hysteresis phenomena in the case of forward- and reverse- V_d -scans (These curves have been obtained with a long integration time).

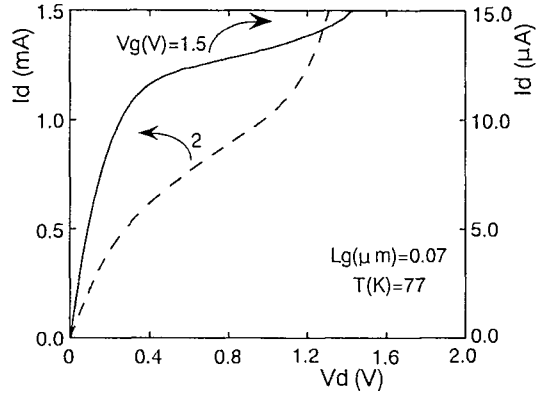


Fig. 8 : Drain current - drain voltage characteristics for a $0.07 \mu\text{m}$ gate length MOSFET's at 77 K for low gate biases.