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Non-Destructive Techniques for Identification and Control of Processing Induced Extended Defects in Silicon and Correlation with Device Yield

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Abstract. — The possibilities and limitations of non-destructive extended defect characterization techniques, *i.e.* X-ray topography, carrier recombination imaging and laser scattering tomography are illustrated by a case study whereby a dislocation problem occurred during the local isolation step of a CMOS compatible diode process. It is shown that the diode yield is correlated with the presence of dislocations observed after the full process. The “in process” application of the techniques is illustrated by investigating defect formation after different local isolation processes.

1. Introduction

It has been known since the beginning of the microelectronics era that extended lattice defects change the electronic properties of silicon and can thus influence the characteristics of devices. The establishment of a direct correlation between the presence of defects *e.g.* in a single diode and the diode characteristics is however not that straightforward. The (beneficial or) detrimental effect of a lattice defect depends indeed strongly on its exact location in the active device area and not the least also on the degree of metallic decoration of the defect. For that reason this kind of “microscopic” studies looking at single devices has not been too successful.

To be useful for process and yield control, defect characterization tools should be used which are non-destructive and allow rapid inspection of the wafer during different stages of the process. Few techniques are available to do this and are mainly based on the use of

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X-rays (X-ray topography) [1, 2], optical beams (*e.g.* photoluminescence [3, 4], IR microscopy, interferometry and tomography [5–7]) or microwave absorption for lifetime mapping [8, 9].

In the present paper an approach is illustrated whereby the device yield on wafer level is correlated with defect studies on macroscopic level. The possibilities and limitations of non-destructive techniques are illustrated by a case study whereby a dislocation problem occurred during the local isolation step of a CMOS compatible diode process. It is shown that the diode yield is correlated with the presence of dislocations observed after the full process.

The use of these non-destructive techniques has the advantage that an extended defect problem can be detected and identified early in the process so that appropriate measures can be taken. This is illustrated by studying dislocation distributions just after the local isolation step using different isolation stacks and ramping conditions.

2. Materials and Characterization Techniques

In the present study two types of samples have been studied. First arsenic implanted n^+ diodes were fabricated on 150 mm (001) Cz wafers both on p-type substrates and on substrates with a p-well. An advanced 0.35 μm CMOS compatible process was used including a split with two different local isolation technologies, *i.e.* conventional LOCAL isolation Of Silicon (LOCOS) and Poly Buffered LOCOS (PBL) both with a range of different isolation stacks. The diodes were contacted using metal contacts. To allow separation of perimeter effects from bulk contributions a special test structure was used with different sizes of square diodes (“area” diodes) and with meander diodes having a large perimeter to area ratio. The diode current/voltage characteristics distribution over the processed wafers were measured with an automated wafer probe station and a HP4145 parameter analyser. All measurements were performed between a top junction contact and a bottom Ohmic contact so that the current flow is forced through the substrate. During the measurement, nitrogen is flushed continuously over the wafer to avoid surface charging and leakage effects. After full electrical characterization of the diodes, which revealed in some cases significant yield differences between the two isolation approaches, the covering layers were etched off and the substrates were investigated using a variety of non-invasive defect characterization tools as discussed further.

In a second case, the possibility to detect in a non-invasive way a dislocation problem in an early stage of the device processing is illustrated by investigating wafers after the local isolation step without removal of the oxidation mask and grown thick field oxide. Again LOCOS was compared with PBL using a stack of 15 nm pad oxide and 150 nm Si_3N_4 and a stack of 20 nm pad oxide, 50 nm amorphous Si and 200 nm Si_3N_4 , respectively. A 600 nm field oxide was grown in wet oxygen at 975 °C using different temperature ramping-up and down rates. A correlation was also made with results obtained by preferential etching after cleavage of the wafers.

X-ray topography analyses were performed at the ID19 beam-line of the European Synchrotron Radiation Facility in Grenoble (France). The topographs were taken in transmission (Laue) mode with white beam on a diffractometer 145 m far from the source. The beam size was limited by slits to fully illuminate one device of the periodic array of diodes fabricated on the silicon wafers. The Laue patterns obtained consisted of several spots, each of them being an X-ray image of the probed surface. These patterns were indexed by a suitable computer program which enabled the identification of the diffraction vectors and, from geometrical considerations, the beam energies corresponding to the different images. 220 transmission images, produced by lattice planes perpendicular to the sample surfaces and by energies of the beam around 20 keV, were used to fully characterize the extended defects.

Plan view Laser Scattering Tomography (LST) images were obtained in the Brewster angle mode using a MILSA IRHQ-2 instrument of Ratoc equipped with a semiconductor laser (870 nm wavelength) for near surface inspection. The depth penetration of this mode of operation is about 15 μm . Images obtained with reflected visible light and scattered laser light were compared to eliminate artefacts due to surface effects.

Plan view carrier recombination imaging was performed at room temperature using a new non-contacting tool developed at Bio-Rad Micromeasurements Ltd [10] with a probing depth of 0.2–1 μm depending on wavelength, excitation level and surface passivation. A localised recombination image is obtained which reveals areas of enhanced non-radiative recombination. The recombination images are compared with reflected light images from the same sample area to separate bulk recombination centres from particles and surface contamination or damage.

3. Results and Discussion

3.1. CORRELATION BETWEEN DIODE YIELD AND EXTENDED DEFECTS. — In Figure 1 the cumulative probability of the leakage current at a reverse bias of 5 V is shown both for large square diodes and meander diodes on a “relaxed” LOCOS (60 nm pad oxide/120 nm Si_3N_4) and on a PBL wafer (20 nm pad oxide/50 nm a-Si /200 nm Si_3N_4). Both diode wafers are without p-well and with metal contacts. A clear difference in leakage current distribution is observed for these two extreme cases. The “relaxed” LOCOS wafer has a yield close to 100% while the PBL wafer only yields about 60%. Detailed analyses of the different contributions to the leakage current showed that in both cases the leakage current is mainly originating from the perimeter of the diodes already suggesting the possibility of a local isolation related problem. This is confirmed by X-ray topography and contactless carrier recombination imaging as illustrated in Figures 2 and 3 which are obtained after removal of the different layers from the silicon substrate. In the LOCOS wafer no extended defects were observed.

Figure 3 shows a low and high resolution image of a diode structure for which PBL isolation was used. The top image reveals two of the isolation lines which have a strong dark contrast due to enhanced carrier recombination. The defect density is so high that no individual dislocations are resolved. Zooming in and using higher resolution allows, however, to image also individual dislocations which are running parallel to the film edge and extend under the field oxide as shown in Figure 3b. This illustrates that a very localised image is obtained with high spatial resolution in contrast to many of the other techniques which are based on recombination imaging. It should be mentioned that in the present experiment no intentional metal contamination has been introduced and that all processing was performed under (ultra) clean conditions. The excellent leakage current values for the non-dislocated diodes also confirm that metal contamination levels after processing are extremely low. This illustrates that the room temperature carrier recombination imaging technique is sensitive for very low levels of metal contamination.

A more detailed report on the diode performance for the different isolation stacks and thermal treatments and their correlation with the presence of extended defects will be published elsewhere [11]. A similar impact on diode characteristics of “clean” dislocations but originating from the substrate itself due to interstitial oxygen precipitation was recently observed and studied in detail using a variety of complementary characterization tools [12, 13].

In view of the success of the mentioned non-invasive techniques to reveal the defects causing the diode leakage problem after the full diode process, the next step was to evaluate the possibility to use these techniques to detect the defects in an early stage of the device processing so that they might also be used for process control.

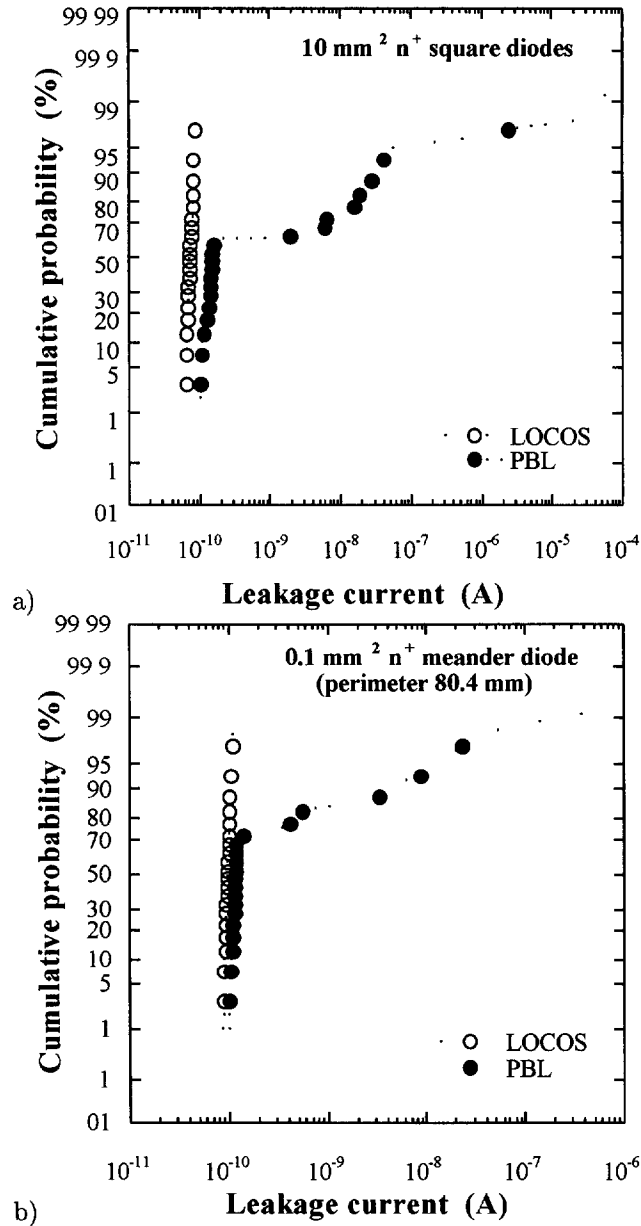


Fig. 1. — a) Cumulative probability of the leakage current for large n⁺ square diodes with a LOCOS and PBL isolation technology. 98 diodes on each wafer were measured. The PBL wafer has a poor yield of only 60%. b) A similar behaviour is observed for the meander diodes.

3.2. IN PROCESS NON-DESTRUCTIVE DETECTION AND CHARACTERIZATION OF EXTENDED DEFECTS. — The results reported in the previous section strongly suggest that the observed leakage current problem is related with dislocation generation during the local isolation process. For that reason wafers were prepared with similar isolation structures as used in the diode structures and characterized after the growth of the field oxide without any removal of the optically transparent layers.

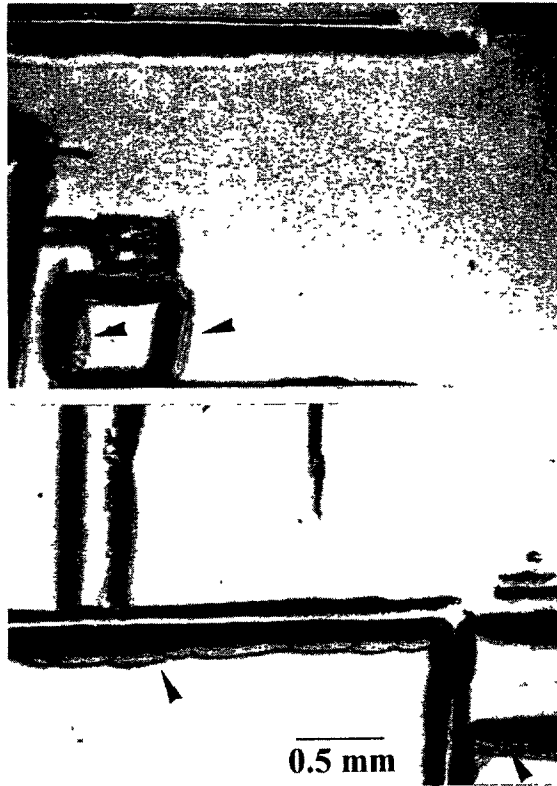


Fig 2 — X-ray topography images of the diode wafer with PBL isolation of Figure 1 after removal of all device layers. Dislocations can clearly be observed at the edges of the active device areas which correspond with the field oxide edges (arrows).

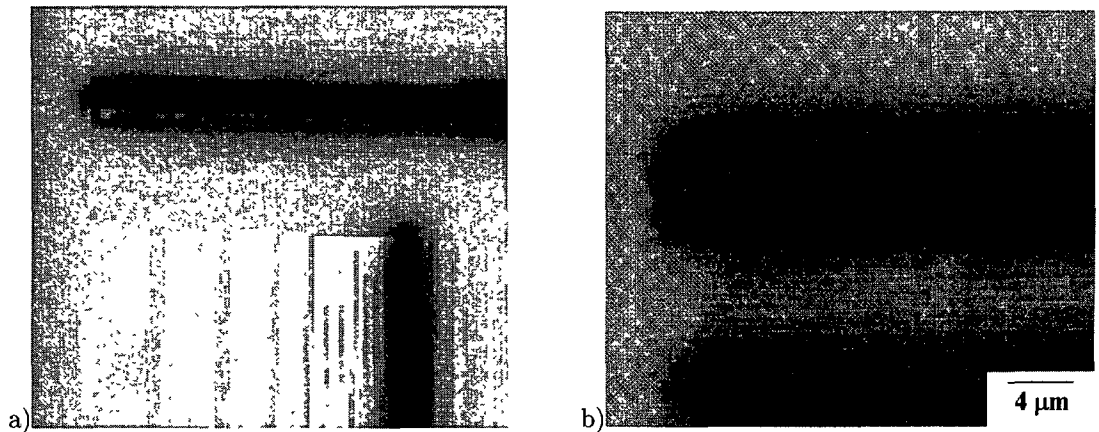


Fig. 3. — Carrier recombination images revealing the presence of extended defects at local isolation edges of diode structures. The low magnification image in (a) shows two isolation stripes in perpendicular directions which contain both a large density of dislocations. The high resolution image in (b) reveals individual dislocations extending into the field oxide area. All device layers were etched off before the analysis. The marker is 4 μm

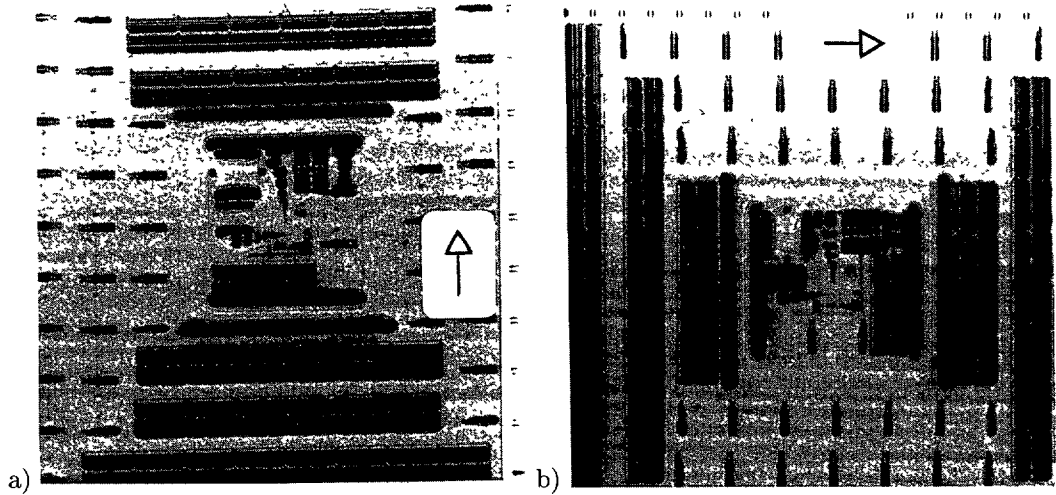


Fig 4. — Transmission X-ray images taken with two perpendicular $\langle 220 \rangle$ diffraction vectors (arrows) parallel to the LOCOS sample surface. The lengths of the diffraction vectors correspond to 1 mm on the sample. The oxide and nitride layers were not removed. No dislocations are observed but the localised strain fields at the LOCOS edges are clearly revealed.

Figures 4a and 4b show diffraction contrast coming from the distortion fields in the silicon substrate at the boundaries of the overlayer stripes in the LOCOS structure. The stripes are aligned along the $\langle 220 \rangle$ directions parallel to the sample surface. The vanishing of the contrast due to the stripe boundaries parallel to the diffraction vector indicates that the displacement vectors \mathbf{R} associated with them are parallel to the surface and perpendicular to the stripe edges. This observation illustrates the possibility of X-ray topography to obtain also information on local strain fields in semiconductor structures. No extended substrate defects are seen in the figures and were also not observed in other areas of the sample.

The information contained in Figures 5a and 5b, obtained on a diode wafer with PBL isolation, is quite different. In addition to the contrast given by the discontinuities of the surface stripes, dislocation lines are present at the stripe edges and roughly parallel to the stripes themselves. Figure 5b shows a higher magnification of the central region of the structure. The dislocation lines are clearly seen and are easily distinguishable from the strain contrast at the stripe edges.

Unlike the contrast due to the stripe edges, the dislocation contrast does not vanish with the operating diffraction vectors. This observation implies that the Burgers vectors $b = a/2\langle 110 \rangle$ of the dislocations are not perpendicular to the lines (*i.e.* they are not of the edge type) but that they are of 60 degree type with \mathbf{b} inclined to the sample surface. This is in full agreement with previous TEM analyses of dislocations formed at $[110]$ oriented film edges on (001) substrates [14].

It was recently demonstrated that LST is a technique which not only allows to detect scattering inclusions but also dislocations and stacking faults in bulk silicon [7, 15] when the appropriate imaging conditions are used. The present study reveals that it is also possible to detect processing induced near surface dislocations through optically transparent capping layers. Typical results are seen in Figures 6a and 6b, showing plan view scattering and reflection images obtained on the same LOCOS and PBL samples as in Figures 4 and 5, respectively.

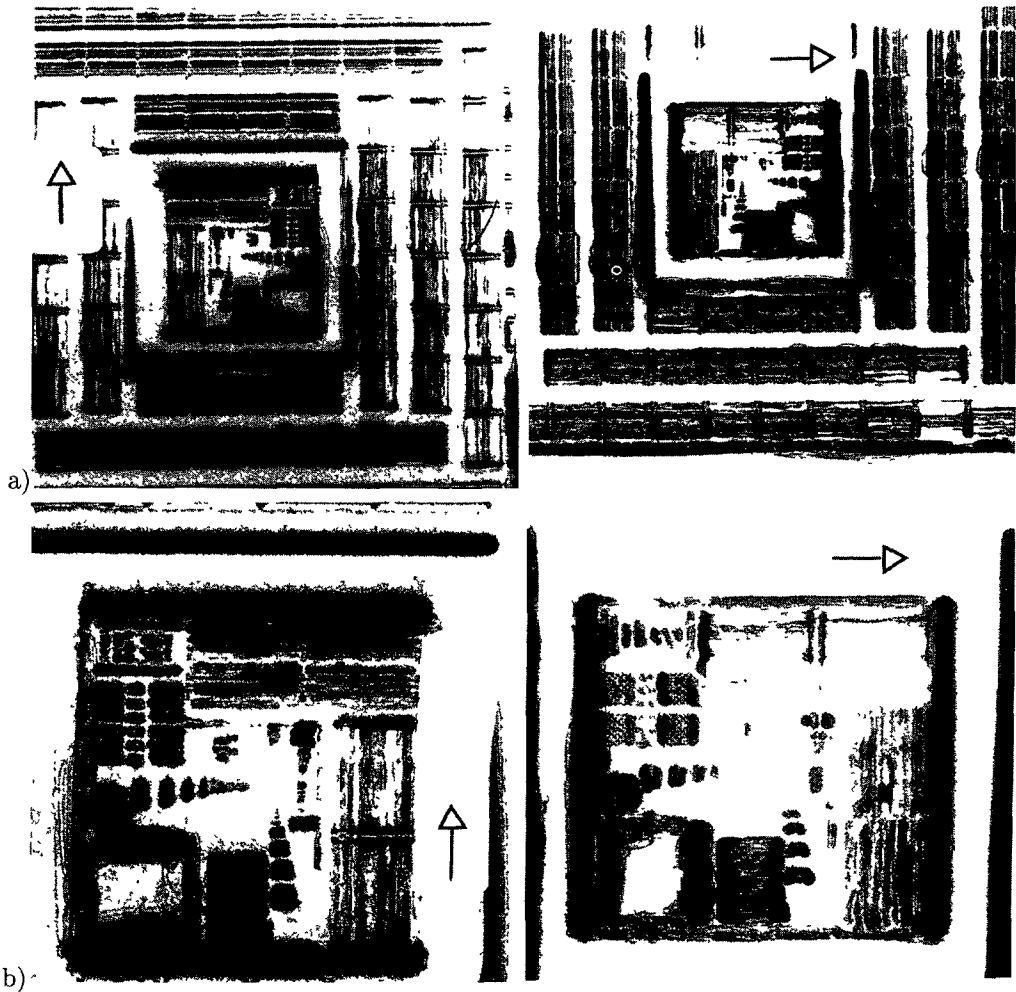


Fig. 5 — a) Transmission X-ray images taken with two perpendicular $\langle 220 \rangle$ diffraction vectors (arrows) parallel to the PBL sample surface. The lengths of the diffraction vectors correspond to 1 mm on the sample. The oxide, polysilicon and nitride layers were not removed. b) Higher magnification transmission X-ray images of the same area. Dislocations penetrating in the silicon substrate below the field oxide are clearly observed at the left side. The lengths of the diffraction vectors correspond to 0.5 mm on the sample.

In the LOCOS sample no defects are observed while in the PBL sample a large density of dislocations is present as confirmed by preferential etching of cleavage planes obtained through the structures.

4. Conclusions

It is shown that (clean) dislocations close to active areas of devices have a strong impact on the device performance and yield. In view of the increased sensitivity of deep submicron technologies for single substrate defects there is a strong need for non-destructive large area

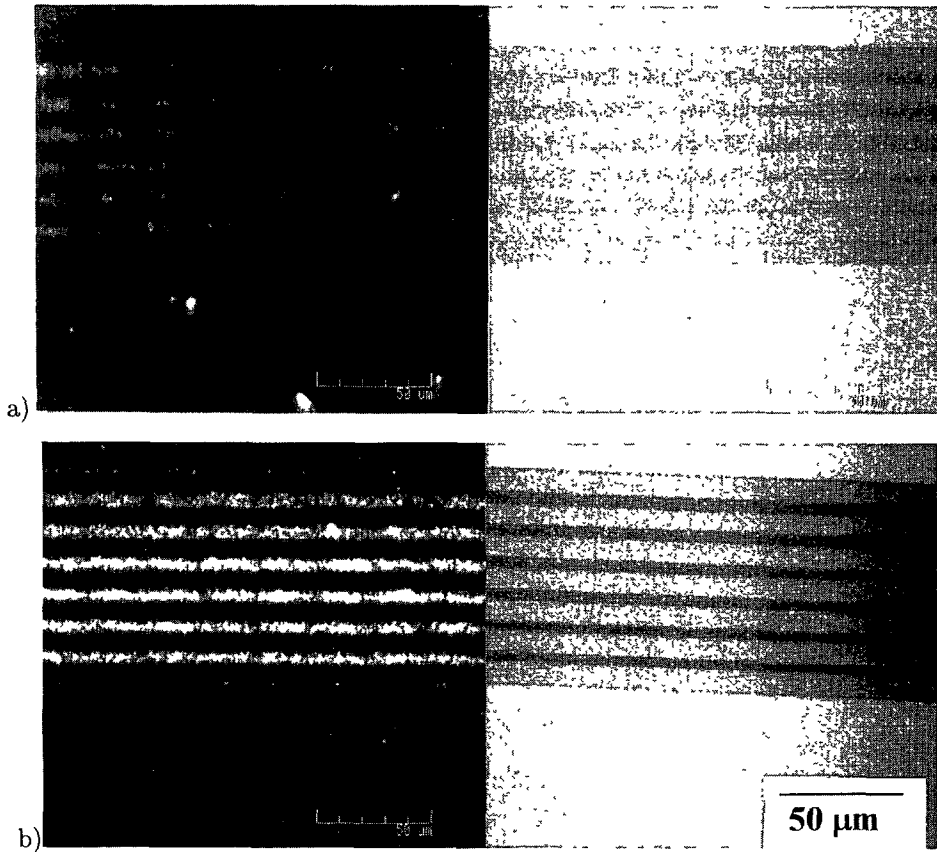


Fig. 6. — Plan view Brewster angle LST images (left) of a LOCOS (a) and a PBL (b) structure consisting of a periodic pattern of parallel lines. The presence of dislocations in the PBL structure is clearly revealed by the strong scattering in the field oxide regions in between the active area stripes. The oxide, polysilicon and nitride layers were not removed. The images at the right are reflected visible light images showing the test structure.

techniques allowing to detect defect related problems in an early stage of device processing. Three possible candidates, *i.e.* X-ray topography, carrier recombination imaging and LST, each yielding complementary information on the nature and presence of extended substrate defects have been presented.

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