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Numerical and Analytical Investigations on IGBTs Thermal Behaviour

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Abstract. — Power devices such as IGBTs (Insulated Gate Bipolar Transistors) operate within a large temperature range. Therefore, it is really important to understand the relationship between the device temperature and its electrical characteristics. From this viewpoint, the authors have studied the influence of the IGBT technology (Punch-Through PT or Non-Punch-Through NPT) on its thermal and electrical behaviours. This work points out that the variations with temperature of the stored charge in the IGBT base depend on the device technology. Using two-dimensional device simulations coupled with an analytical modelling, the authors show that the stored charge in PT devices is more temperature sensitive than in NPT devices. The modelling of the stored charge function of the current density and the device description proves that the concept of the charge injection control influences the temperature dependence. Consequently the static and dynamic IGBT characteristics are temperature sensitive. The voltage rise in hard switching mode (turn-off phase) is related to the temperature dependence of the stored charge.

Résumé. — Les composants de puissance comme les IGBTs (Transistors Bipolaires à Grille Isolée) fonctionnent sur une large gamme de température. Il apparaît alors important de comprendre les relations entre la température du composant et ses caractéristiques électriques. Dans cette problématique, les auteurs ont étudié l'influence de la technologie de l'IGBT (Punch-Through PT ou Non-Punch-Through NPT) sur son comportement électrique et thermique. Ce travail révèle que les variations en température de la charge stockée dans la base de l'IGBT dépendent de la technologie du dispositif. En utilisant des simulations en deux dimensions couplées avec une modélisation analytique, les auteurs montrent que la charge stockée dans les composants PT est plus sensible à la température que dans les composants NPT. La modélisation de la densité de courant en fonction de la charge stockée prouve que le contrôle de l'injection de charges influence la dépendance en température. En conséquence, les caractéristiques statiques et dynamiques de l'IGBT sont sensibles à la température. La montée de la tension en commutation dure à l'ouverture est reliée à la dépendance en température de la charge stockée.

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1. Introduction

IGBT (Insulated Gate Bipolar Transistor) is one of the most attractive power devices due to its good electrical characteristics and to its easy gate drive (and low cost). It generally operates within a large temperature range [1] therefore, it is really important to understand the relationship between the device temperature and its electrical characteristics. Previous articles have pointed out different thermal behaviour between the two IGBT families: Punch-Through PT and Non-Punch-Through NPT [2–7]. This paper investigates the influence of the IGBT technology on the stored charge in the device base. The purpose is to understand the influence of physical or technological parameters on the electro-thermal IGBT characteristics. We have especially studied the variations of the IGBT stored charge function of device technology and temperature. This is achieved with different steps. Firstly, we present the technological concepts of PT and NPT IGBTs. These considerations may be well known by most of the readers, but it is essential to understand the technology concepts which are connected to the semiconductor physics. Furthermore, these technological aspects will be used in the following part concerning the two-dimensional device simulation. Afterwards, we develop a simple modelling of the current density function of the main technological or physical parameters. This analytical approach allows to study the influence of several variables as the layer widths, the carrier lifetime and its temperature sensitivity. Moreover, calculation durations using the analytical approach are reasonable so that we could study the influence of various parameters. Finally, the temperature dependencies of measurable electrical characteristics such as the voltage rise in hard switching mode (turn-off phase) is related to the device technology.

2. PT and NPT IGBT Technologies

The main difference between these two technologies is the initial substrate used by the manufacturers. PT IGBT (Fig. 1a) is built on a thick P^+ substrate ($300\ \mu\text{m}$). The high resistivity layer is processed by a silicon epitaxial growth with two doping levels to create firstly, the N^+ buffer layer, and secondly, the N^- layer (IGBT base). The trade-off between low on-state voltage ($V_{ce(sat)}$) and high switching speed is achieved by adjusting the buffer layer geometry and the carrier lifetime. The N^+ buffer layer geometry (doping level, width) is adjusted with epitaxial process parameters. The goal of the buffer layer is to reduce the emitter efficiency and therefore, to reduce the hole carrier injection from the emitter P^+ towards the base N^- . The carrier lifetime can be reduced and controlled by an irradiation process [8–10]. As the temperature increases, the carrier lifetime in the base region has been found to increase [8, 11, 12].

The NPT technology (Fig. 1b) is basically different. In this case, the original substrate is the N^- layer. Its width is about $220\ \mu\text{m}$ which allows sufficient mechanical properties. Then manufacturers diffuse a P^+ layer in the back side of the die. This P^+ layer geometry is adjusted to provide the Charge Injection Control (C I C.) in the IGBT base [13]. The next technological steps concern the MOSFET part of the device and are identical to the power VDMOS technology.

3. Two-Dimensional Numerical Device Simulation

The two-dimensional MEDICI software [14] solves carrier transport equations. The technological parameters (cellular geometry, doping profiles, layer width...) have been obtained with reverse engineering techniques such as microscopic examination and spreading resistance probe. From these technological parameters, we have created MEDICI input file using several physical models (carrier mobility, carrier generation-recombination, *etc*). The simulation results can

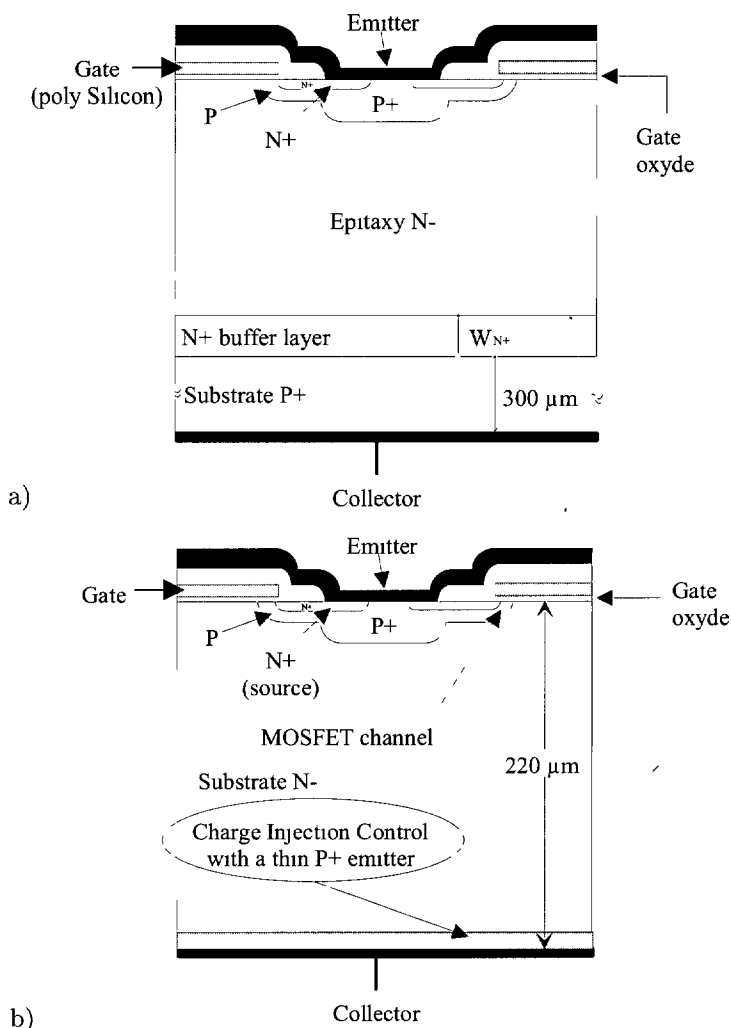


Fig 1. — IGBT cross-section. a) PT technology, b) NPT technology.

be used to investigate the influence of technology on electrical behaviour. Firstly, we have to verify that measurements and simulations are in agreement. Thus we simulate $I-V$ curves with gate voltage and temperature as parameters (Figs. 2a and 2b).

The MEDICI simulator reproduces correctly the steady-state behaviours of PT and NPT IGBT with different lattice temperatures. Then we have analyzed the carrier distribution into the structure. Figure 3 shows the static hole carrier distribution in the high resistivity layer (base) with a constant current density of 100 A cm^{-2} and the temperature increasing in the range $27 \text{ }^\circ\text{C}$ to $150 \text{ }^\circ\text{C}$ (Fig. 3a for the PT device and Fig. 3b for the NPT device). The high resistivity layer is always in quasi-neutral state, *i.e.*, hole and electron concentrations are equal. We observe from Figures 3a and 3b that, in the NPT technology device, the carrier profile and the stored charge remain constant when temperature increases. On the other hand, the stored charge in the PT device considerably increases (Fig. 3a).

The simulation of the NPT device shows that the injection level at the emitter-base junction of the internal PNP transistor is constant during the temperature rise ($J_T = 100 \text{ A cm}^{-2}$).

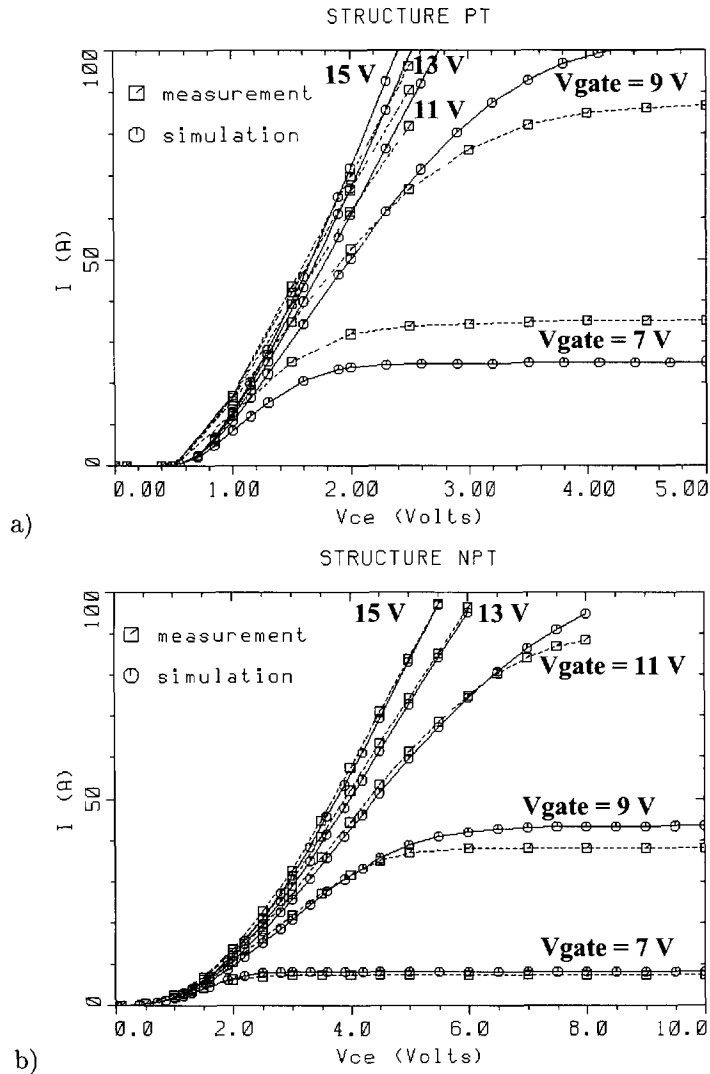


Fig. 2. — $I_c = f(V_{ce})$, $T = 150^\circ\text{C}$. a) PT device, b) NPT device

The thin emitter geometry in a NPT structure controls the injection level in the IGBT base. The charge injection control does not occur in a PT device because of the classic emitter (emitter width equals $300\ \mu\text{m}$). In the next part, we propose a simple steady-state modelling taking into account the emitter geometry.

4. Analytical Device Modelling

4.1. CURRENT DENSITY MODELLING — The purpose of this section is to develop a simple model which may provide acceptable results in short calculation durations. Therefore, we will be able to study the effect of various technological or physical parameters.

From the ambipolar transport equation in the base, we express the static current density

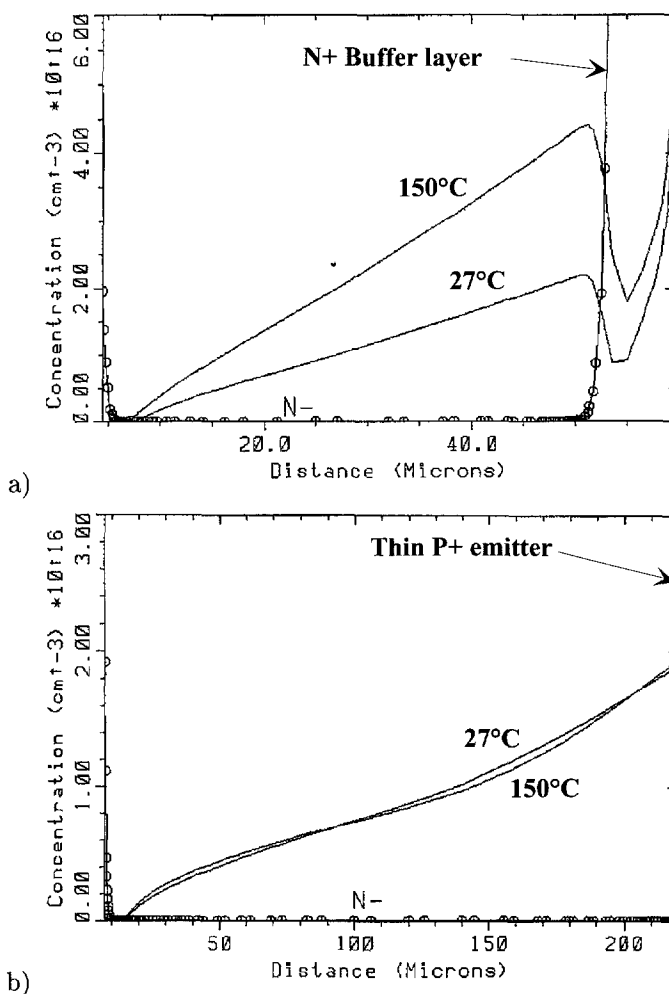


Fig. 3. — Net doping and hole carrier profiles in the base (in 10^{16} cm^{-3}), $J_T = 100 \text{ A cm}^{-2}$, $V_g = 15 \text{ V}$, $T = 27 \text{ }^\circ\text{C}$ and $150 \text{ }^\circ\text{C}$. a) PT device, b) NPT device.

function of injection level in the base and physical or geometrical parameters. The following model is based on bipolar transistor current (Fig. 4). As we are mainly interested in the variations of the stored charge *versus* temperature, the model does not take into account the N^+ buffer layer (PT technology). We assume that firstly, the hole concentration equals zero at the edge of the depletion layer, secondly, the depletion layer width is negligible in comparison to the base width. The electron current density in the high-level injection base can be given as follows [15]:

$$J_{nB}(x) = \frac{b}{1+b} J_T + qD \frac{dp(x)}{dx} \tag{1}$$

with b : electron mobility to hole mobility ratio in the base region, J_T : total current density, q : electron charge, $p(x)$: hole concentration in the base region, D : ambipolar diffusion coefficient in the base region.

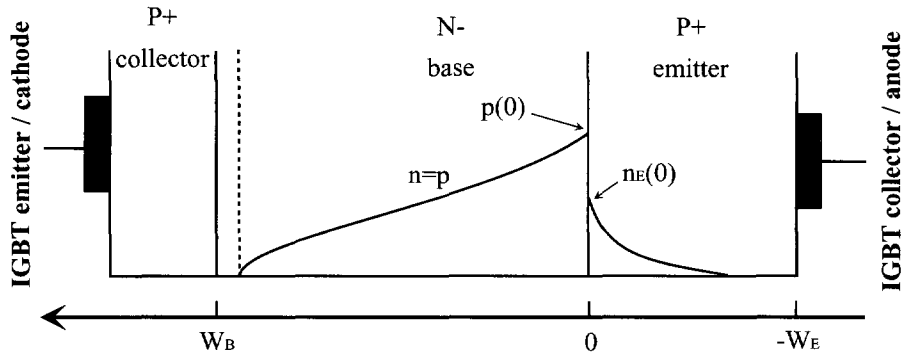


Fig 4. — Bipolar transistor part of IGBT

D is defined as follows:

$$D = 2 \frac{D_n D_p}{D_n + D_p} \quad (2)$$

where D_n , D_p are respectively the electron and hole diffusion coefficients [16].
 D_n , D_p are defined by the Einstein relationship:

$$D_n = \frac{kT}{q} \mu_n \quad (3)$$

$$D_p = \frac{kT}{q} \mu_p \quad (4)$$

with k : Boltzmann's constant, μ_n : electron mobility and μ_p : hole mobility.

In the base region, we consider that the ambipolar diffusion length and the base width are in the same order of magnitude. Therefore, the hole carrier profile may be expressed with hyperbolic function:

$$p(x) = p(0) \frac{\text{sh}\left(\frac{W_B - x}{L}\right)}{\text{sh}\left(\frac{W_B}{L}\right)} \quad \text{where } 0 \leq x \leq W_B \quad (5)$$

with $p(0)$: hole concentration at the emitter-base junction (Fig 4), W_B : base width, L : ambipolar diffusion length.

L is given by the following equation:

$$L = \sqrt{D\tau_{HL}}, \quad (6)$$

τ_{HL} corresponds to the carrier lifetime in high injection level condition.

τ_{HL} is yielded by [8]:

$$\tau_{HL} = \tau_n + \tau_p, \quad (7)$$

τ_n , τ_p are respectively the electron and hole lifetimes.

In the emitter region, the electron carrier concentration can be expressed as follows:

$$n(x) = n_E(0) \frac{\text{sh}\left(\frac{W_E + x}{L_n}\right)}{\text{sh}\left(\frac{W_E}{L_n}\right)} \quad \text{where } -W_E \leq x \leq 0 \quad (8)$$

with $n_E(0)$: electron carrier concentration at the emitter-base junction (Fig. 4), W_E : emitter width, L_n : electron diffusion length in the emitter.

The electron current density in the emitter is given by:

$$J_{nE}(x) = qD_n \frac{dn(x)}{dx} = q \frac{D_n}{L_n} n_E(0) \frac{\text{ch}\left(\frac{W_E + x}{L_n}\right)}{\text{sh}\left(\frac{W_E}{L_n}\right)}. \tag{9}$$

At the emitter-base junction, we assume [17]:

$$n_E(0)N_{AE} = p(0)^2, \tag{10}$$

where N_{AE} is the emitter doping level.

$$J_{nE}(0) = J_{nB}(0). \tag{11}$$

Equation (11) corresponds to the continuity of the electron current density at $x = 0$ (emitter-base junction).

Finally, equations (1, 5, 9, 10, 11) lead to the current density expression in the PT structure:

$$J_T = q \frac{1+b}{b} p(0) \left[\frac{D}{L} \coth\left(\frac{W_B}{L}\right) + \frac{p(0)}{N_{AE}} \frac{D_n}{L_n} \coth\left(\frac{W_E}{L_n}\right) \right]. \tag{12}$$

In NPT structure, the carrier lifetime is large so that, the carrier profiles are quasi-linear in the base and in the emitter. Therefore, the electron current density in the base can be written as follows.

$$J_{nB}(x) = \frac{b}{1+b} J_T - qD \frac{p(0)}{W_B}, \tag{13}$$

and the electron current in the emitter:

$$J_{nE}(x) = qD_n \frac{n_E(0)}{W_E}. \tag{14}$$

With the same assumptions (Eqs. (10) and (11)), we obtain the total current density in a NPT technology.

$$J_T = q \frac{1+b}{b} p(0) \left[\frac{D}{W_B} + \frac{D_n p(0)}{N_{AE} W_E} \right]. \tag{15}$$

Equation (15) corresponds to equation (12) applied to the NPT technology assuming that the carrier diffusion lengths are much larger than the widths of the base and emitter layers.

In equation (12), the physical parameters b , D , D_n , L , L_n are temperature sensitive. These variables are calculated from the carrier mobility and lifetime. The carrier mobility and lifetime models are chosen from [7, 18, 19]:

$$\text{electron mobility} \Rightarrow \mu_n = \frac{1429.23 \times \left(\frac{T}{300}\right)^{-2.3} - 55.24}{1 + \left(\frac{T}{300}\right)^{-3.8} \left(\frac{N_t}{1.072 \times 10^{17}}\right)^{0.73}} + 55.24 \tag{16}$$

$$\text{hole mobility} \Rightarrow \mu_p = \frac{479.37 \times \left(\frac{T}{300}\right)^{-2.2} - 49.70}{1 + \left(\frac{T}{300}\right)^{-3.7} \left(\frac{N_t}{1.606 \times 10^{16}}\right)^{0.70}} + 49.70 \tag{17}$$

Table I. — *Physical and geometrical parameters.*

	PT device	NPT device
N_B (cm ⁻³)	10 ¹⁴	
W_B (μm)	50	200
N_{AE} (cm ⁻³)	10 ¹⁷	
W_E (μm)	300	1
$\tau_{n0} = \tau_{p0}$ (μs)	0.1	20
$\alpha_n = \alpha_p$	1.5	
N_{REF} (cm ⁻³)	10 ²⁰	

where T represents the temperature (K) and N_t (cm⁻³) the doping level of the layer ($N_t = N_{AE}$ in the emitter side or $N_t = N_B$ in the base)

The carrier lifetime model is [7, 18]:

$$\text{electron lifetime} \Rightarrow \tau_n = \frac{\tau_{n0}}{N_t} \left(\frac{T}{300} \right)^{\alpha_n}, \quad (18)$$

$$1 + \frac{N_{REF}}{N_t}$$

$$\text{hole lifetime} \Rightarrow \tau_p = \frac{\tau_{p0}}{N_t} \left(\frac{T}{300} \right)^{\alpha_p}, \quad (19)$$

$$1 + \frac{N_{REF}}{N_t}$$

where τ_{n0} and τ_{p0} represent the electron and hole carrier lifetimes at 300 K in a high resistivity layer, respectively, α_n and α_p are the temperature sensitivities and N_{REF} is a parameter [18].

4.2. INJECTION LEVEL $p(0)$ FUNCTION OF TEMPERATURE. — From equations (2-4, 6, 7, 12, 16-19), we calculate the injection level $p(0)$ function of temperature with a constant current density of 100 A cm⁻². We illustrate the modelling with two different examples: one for each technology. Table I presents the physical and geometrical parameters.

We consider that the base doping concentration (N_B) is 10¹⁴ cm⁻³. For the PT device, we have chosen the base width equals 50 μm because it corresponds to a 600 V device with a N⁺ buffer layer. For the NPT device, the base width equals 200 μm. The emitter doping concentration (IGBT collector) is 10¹⁷ cm⁻³ whatever the technology is. This value is typical of NPT devices, while for PT devices, it is quite low. As we omitted to take into account the buffer layer in the PT device modelling, we consider that this low emitter concentration reduces the injection efficiency instead of the buffer layer. The NPT device presents a thin emitter: 1 μm. In PT technology, the emitter is the substrate. Therefore, we consider that its width equals 300 μm. The carrier lifetime for the PT device is 0.1 μs, while for the NPT device, the carrier lifetime equals 20 μs. In references [8, 11, 12], the carrier lifetime in the base region has been reported increasing with temperature. For this reason, we propose $\alpha_n = \alpha_p = 1.5$ (Eqs. (18, 19)). This leads to a carrier lifetime increase of 67% when temperature rises from ambient to 150 °C. Next, we assume that the carrier lifetime does not depend on the layer concentration ($N_{REF} = 10^{20}$ cm⁻³). This is assumed in PT technology because the carrier lifetime is reduced by a specific process such as electron irradiation [8-10]. Therefore, the carrier lifetime is not related to the doping concentration. In NPT case, it has been found afterwards that the parameter N_{REF} does not influence the calculated results.

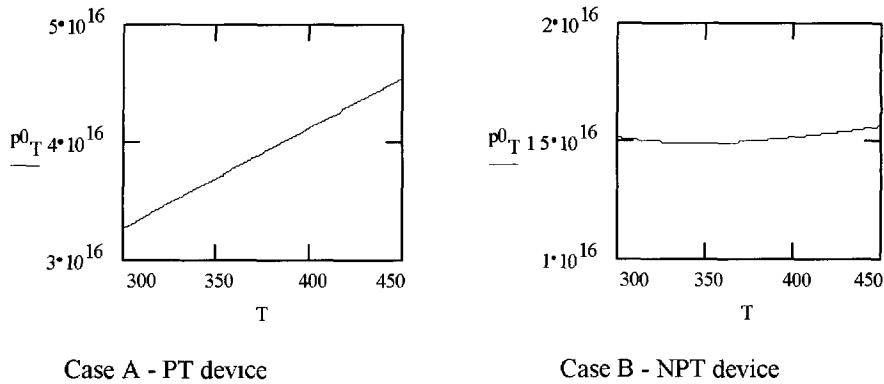


Fig. 5. — Carrier injection level $p(0)$ (in cm^{-3}) function of temperature T (in K) at 100 A cm^{-2} (calculated from Eq (12))

From equation (10) and using the parameters presented in Table I, we extract the injection level $p(0)$ function of temperature for a given current density (Fig. 5).

From Figure 5, we observe firstly that the carrier injection level $p(0)$ is smaller in NPT device than in PT device. This is due to the carrier injection control with a thin emitter in NPT IGBT [13]. Secondly, we note that $p(0)$ rises sharply with temperature in the PT technology and remains nearly constant in the NPT technology.

In NPT device, the emitter width is shorter than the electron diffusion length. Furthermore, the electron diffusion coefficient D_n remains almost constant when temperature rises. Therefore, equation (15) does not depend on temperature. As a result, the emitter injection efficiency is temperature-independent in NPT device. In contrast for PT device, we have to consider equation (9) instead of equation (14) because the electron diffusion length is shorter than the emitter width. As the carrier lifetime and the electron diffusion length rise with temperature, the emitter injection efficiency of PT device increases with temperature.

Finally we note that the results using the simple model are in agreement with the two-dimensional device simulations (Figs. 3a and 3b).

4.3. STORED CHARGE FUNCTION OF TEMPERATURE. — The stored charge in the IGBT base can be calculated as follows:

$$Q = qS \int_0^{W_B} p(x) dx \quad (20)$$

where S is the device area, $p(x)$ is defined by equation (5).

Figure 6 presents the variations of the stored charge in the IGBT base *versus* temperature ($J_T = 100 \text{ A cm}^{-2}$).

We note that, due to a constant injection level in the base, the stored charge in the NPT device is not temperature sensitive. On the other hand, the stored charge in PT device increases with temperature. The stored charge rises because of firstly, the increase of the carrier injection level $p(0)$ secondly, the increase of the carrier lifetime (α_n and $\alpha_p > 1$, Eqs. (18, 19)) and consequently of the carrier diffusion length (Eq. (6)).

The stored charge in the base region is related to two main electrical characteristics: the on-state voltage and the current tail occurring during turn-off phase.

The forward voltage drop may be divided into three parts: the voltage drops in the channel, in the base layer and in the $P - N_{\text{base}}$ junction. Only the second one is influenced by the stored

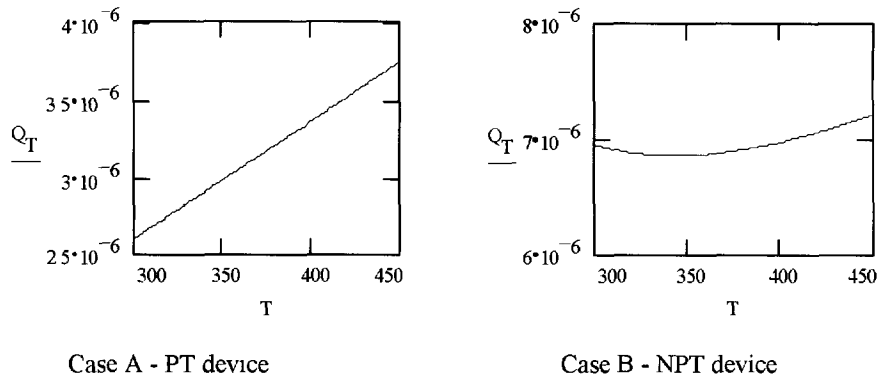


Fig. 6 — Variation of the stored charge in the IGBT base (in C) function of temperature T (in K) at 100 A cm^{-2} (calculated from Eq (20)).

charge For a constant current density, decreasing the stored charge by means of the buffer layer and emitter geometries or carrier lifetime reduction leads to an increase of the base region voltage drop.

During turn-off phase, IGBT behaves as a bipolar transistor with the unconnected base. Therefore the stored charge removal by recombination or by extraction towards emitter and collector results in a current tail [8]. It is quite difficult to express analytically the current tail function of time. Nevertheless it is clear that the current tail and the stored charge removal are strongly related. Smaller is the carrier lifetime, shorter will be the current tail.

Lefebvre *et al.* [3, 6] have measured the recovery charge function of temperature in Zero Current Switching (ZCS) mode. Figure 7 extracted from [6] reveals that the stored charge increases drastically with temperature in the PT device. These results are in agreement with those presented in this section.

Turn-off losses due to the current tail limit the frequency range of their applications. PT IGBTs can be optimised for low transient losses using a low carrier lifetime [8–10]. Consequently, the carrier injection level $p(0)$ and the stored charge are reduced. Nevertheless, as shown in this section, the device temperature rise leads to increase the stored charge and therefore to increase the transient losses [8]. Thermal instability using PT device in a Zero-Current-Switching (ZCS) application has been observed [3]. NPT IGBTs do not present such a behaviour because the stored charge is less temperature sensitive.

4.4. dV/dt FUNCTION OF TEMPERATURE IN HARD SWITCHING MODE (TURN-OFF PHASE)

In an inductive buck-chopper (Fig. 8), it is important to note that the collector-emitter voltage rise (dV/dt) during turn-off phase of the IGBT is also temperature sensitive. We have observed that the IGBT forces the dV/dt slope [5] (Fig. 9). The value of this dV/dt slope depends on the experimental conditions (current, junction temperature, gate resistance) and the device technology (NPT or PT, high switching speed or low $V_{ce(sat)}$). From Figure 9, we observe that the gate voltage is negative before the collector-emitter voltage (V_{ce}) starts to rise. From numerical simulations of PT and NPT device transient phase, we can observe that the expansion of the depletion layer in the N^- base allows to eliminate a part of the stored charge (Figs. 10 and 11). The hole carrier profile close to the P^+ emitter and the injection level $p(0)$ do not change during the V_{ce} rise [20]. The V_{ce} rise creates an instantaneous current due to the removal of a part of the stored charge (Q^*) in the IGBT base during the depletion layer

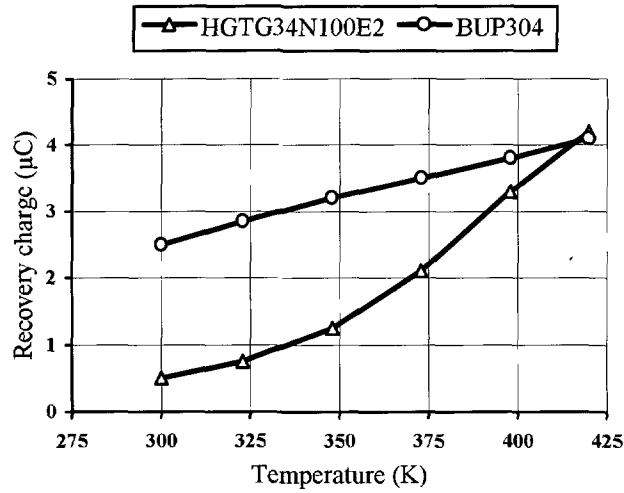


Fig. 7. — Recovery charge (μC) function of temperature (K) in ZCS mode (PT device HGTG34N100E2, NPT device: BUP304, $I = 25 \text{ A}$, $di/dt = 20 \text{ A}/\mu\text{s}$).

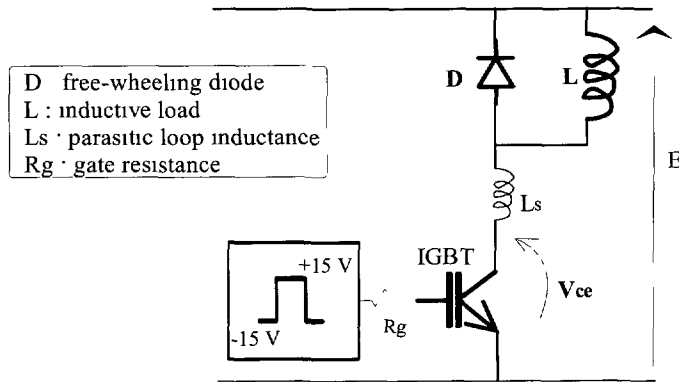


Fig 8 — Buck-chopper test circuit.

expansion (Fig 12). The instantaneous current substitutes the MOSFET electron current and allows the IGBT to provide the whole load current until V_{ce} equals the supply voltage E

The IGBT current starts to decrease when the V_{ce} voltage across the IGBT equals the dc line voltage E and the anti-parallel diode turns-on (Fig. 9). During the V_{ce} rise, the instantaneous current can be related to the dV/dt as follows [5]:

$$i \approx \frac{dQ^*}{dt} = \frac{dQ^*}{dx(t)} \frac{dx(t)}{dt} = \frac{dQ^*}{dx(t)} \frac{d(-W_{DZ}(t))}{dV(t)} \frac{dV(t)}{dt} \tag{21}$$

where Q^* represents the part of the stored charge removed during the expansion of the depletion layer (Fig. 12):

$$Q^* \cong qS \int_{x^*=W_B-W_{DZ}}^{W_B} p(x)dx. \tag{22}$$

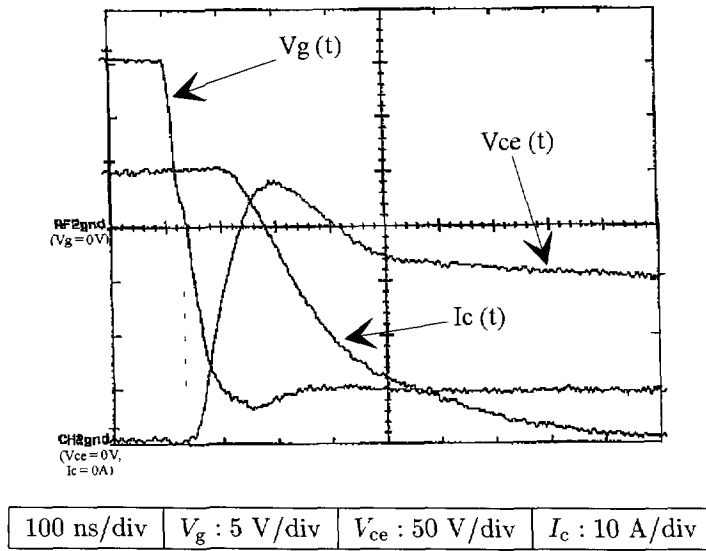


Fig. 9. — Measured turn-off waveforms $I_c = f(t)$, $V_g = f(t)$, $V_{ce} = f(t)$, $T = 27 \text{ }^\circ\text{C}$, $R_g = 4.7 \text{ } \Omega$ (PT device: IRGPC50F)

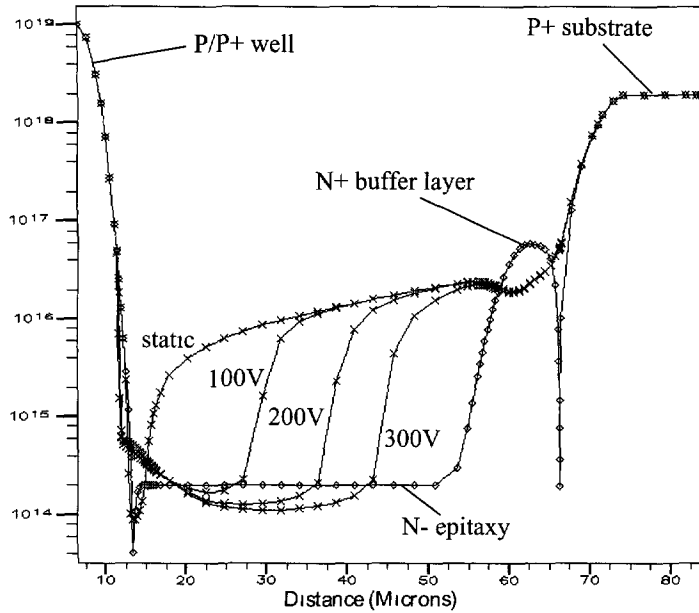


Fig. 10. — Net doping and hole carrier profiles (in cm^{-3}) during the depletion layer expansion (PT device), $T = 27 \text{ }^\circ\text{C}$, $R_g = 4.7 \text{ } \Omega$, $J_T = 100 \text{ A cm}^{-2}$.

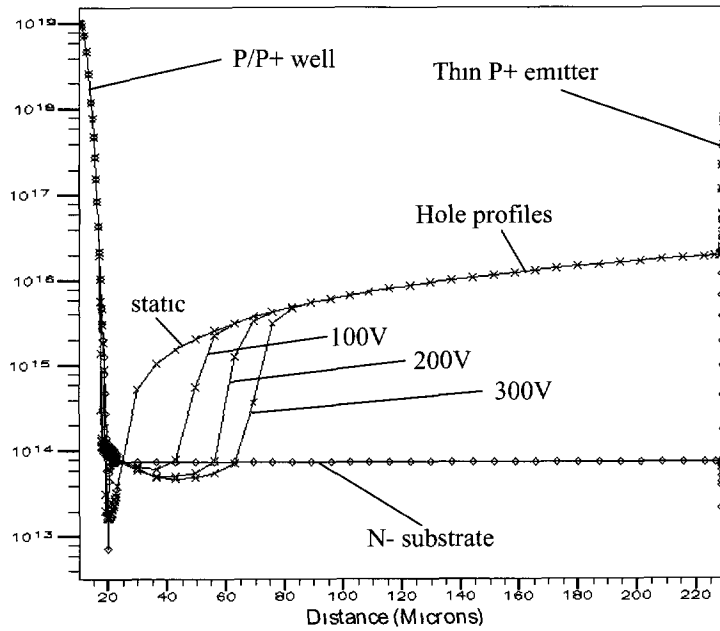


Fig. 11. — Net doping and hole carrier profiles (in cm^{-3}) during the depletion layer expansion (NPT device), $T = 27\text{ }^\circ\text{C}$, $R_g = 4.7\ \Omega$, $J_T = 100\ \text{A cm}^{-2}$.

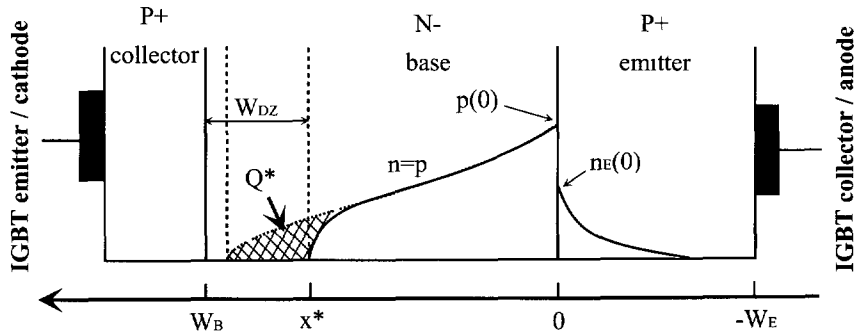


Fig. 12. — Simplified hole profile during the depletion layer expansion

The depletion layer width can be written:

$$W_{DZ}(t) = W_B - x^*(t) = \sqrt{\frac{2\epsilon V(t)}{q(N_B + p)}} \tag{23}$$

V represents the voltage applied to the device, ϵ : the dielectric constant of silicon, N_B : the base doping level, p : the hole concentration in the depletion layer.

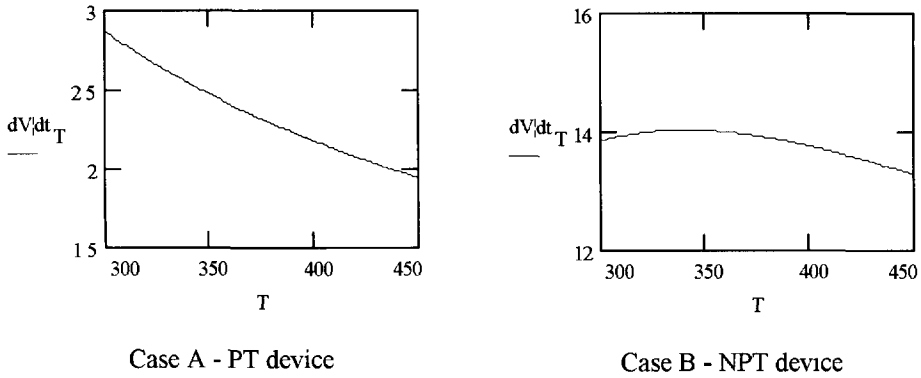


Fig 13 — Voltage slope dV/dt (in $kV \mu s^{-1}$) function of temperature T (in K) (calculated from Eq. (25)) $V_{ce} = 100 V$, $J_T = 100 A cm^{-2}$

The hole concentration p can be calculated:

$$p = \frac{J_T}{qv_{sat(p)}}, \quad (24)$$

where $v_{sat(p)}$ is the hole saturation velocity

Finally, the expression of the instantaneous current is:

$$i \approx p(0)Sq \frac{\text{sh} \left(\frac{1}{L} \sqrt{\frac{2\epsilon V(t)}{q \left[N_B + \frac{J_T}{qv_{sat(p)}} \right]}} \right)}{\text{sh} \left(\frac{W_B}{L} \right)} \sqrt{\frac{\epsilon}{2q \left[N_B + \frac{J_T}{qv_{sat(p)}} \right]}} \frac{1}{\sqrt{V(t)}} \frac{dV(t)}{dt}. \quad (25)$$

Using equation (25) and assuming that the instantaneous current is half of the total constant current, *i.e.*, the PNP transistor current gain equals 1, we calculate the voltage slope (dV/dt) function of temperature (Fig. 13).

For a constant current, the dV/dt slope depends on the stored charge and the hole profile. If we suppose a wide base coupled with a very flat hole profile (NPT technology), the dV/dt has to be very high to remove a sufficient part of the stored charge and to create a suitable instantaneous current (Fig. 13 - Case B). Consider PT technology, the dV/dt slope is higher for high switching speed devices than for low voltage drop devices because the stored charge is smaller in fast IGBT [5]. In PT IGBT, we have already observed that the stored charge in the base increases with the temperature (for a constant current). Then the dV/dt slopes of PT devices decrease with the temperature (Fig 13). The NPT devices are not so much temperature sensitive.

Figures 14 and 15 present the measured dV/dt slopes for PT and NPT devices. Firstly, we observe that the dV/dt values are larger for NPT device as already shown by the analytical model. Secondly, the dV/dt slopes decrease with temperature (as explained previously). The dV/dt slopes measured on the NPT device (Fig. 15) seem to be less temperature sensitive. This point is quite hard to verify due to the difficulty in measuring so large dV/dt ($> 10 kV \mu s^{-1}$). Nevertheless, the measurements are in agreement with the device behaviour analysis.

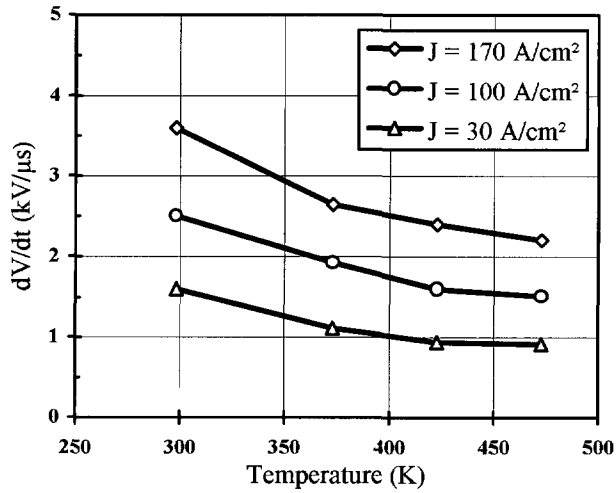


Fig. 14. — Measured dV/dt versus temperature for different current densities, $R_g = 4.7 \Omega$ (PT device: IRGPC50F)

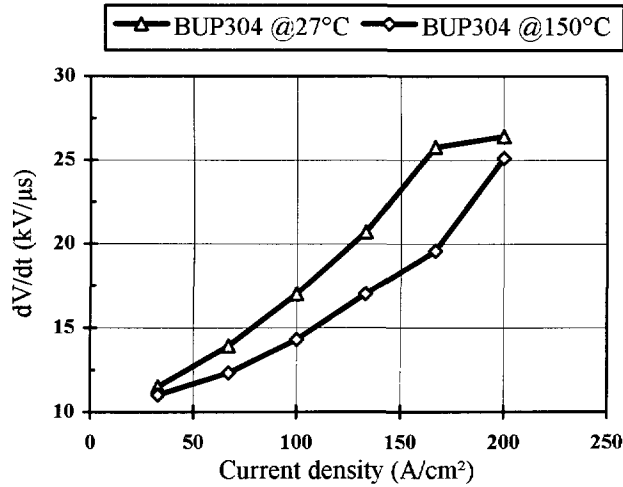


Fig. 15. — Measured dV/dt versus current density ($R_g = 4.7 \Omega$, $T = 27^\circ C$ and $150^\circ C$, NPT device: BUP304).

5. Conclusion

This paper investigates the thermal behaviour of PT and NPT IGBTs. Using two-dimensional device simulation and analytical modelling, this study points out the influence of technological and physical parameters on the temperature dependence of the device characteristics. We show that the charge injection control with a thin emitter allows the stored charge in the NPT IGBT base to be nearly temperature insensitive. In contrast, the stored charge in PT device increases with temperature. The calculated stored charges are quite in agreement with the measured recovery stored charge in zero current switching mode.

The IGBT voltage rise at turn-off in an inductive chopper (hard switching mode) depends on the temperature through the stored charge variations. We have observed that the IGBT forces the dV/dt slope. The V_{ce} rise and the depletion layer expansion create an instantaneous current due to the removal of a part of the stored charge in the IGBT base. This internal transient current substitutes the MOSFET electron current and allows the IGBT to provide the load current during the V_{ce} rise. For a constant current density, the dV/dt slopes measured on PT devices decrease with temperature due to the increase of the stored charge. The dV/dt slopes are much larger with NPT than with PT IGBTs because of the flat hole carrier profile in NPT device base. We note also that the dV/dt slopes measured on NPT devices are less temperature sensitive.

Finally, the new considerations introduced in this study may give the users a better understanding of the IGBT thermal behaviour.

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