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Monte Carlo study of 50 nm-long single and dual-gate MODFETs : suppression of short-channel effects

P. Dollfus, P. Hesto, S. Galdin and C. Brisset

Institut d'Electronique Fondamentale, CNRS URA22, Université Paris XI, Bâtiment 220, 91405 Orsay Cedex, France

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Résumé. — Nous présentons une étude théorique, à partir de simulations Monte Carlo, de MODFETs à simple et double grille de 50 nm de longueur. L'introduction d'une seconde grille située entre la grille de commande et le drain et dont le potentiel est fixé à une valeur positive permet de s'affranchir des effets de canal court qui apparaissent dans les MODFETs à très courte longueur de grille. Nous décrivons le fonctionnement physique de ces dispositifs et en particulier le rôle de la seconde grille. Le MODFET bi-grille présente d'excellentes caractéristiques de drain en saturation tout en offrant des valeurs élevées de transconductance g_m et de fréquence de coupure f_T . Il en résulte une amélioration importante du rapport g_m/g_D .

Abstract. — A theoretical study of 50 nm-Single and Dual-Gate MODFETs using Monte Carlo simulation is reported. The introduction of a second gate, whose potential is fixed to a positive value, between the control-gate and the drain allows to efficiently provide against short-channel effects that occur in ultra-short single-gate MODFET. We describe the physical operating of these devices and especially the role of the second gate. The dual-gate MODFET exhibits an excellent saturation behaviour compared with single-gate MODFETs together with high values of transconductance g_m and current gain cutoff frequency f_T . This is resulting in a large improvement in the g_m to g_D ratio.

1. Introduction.

Performance improvements of Modulation-Doped Field-Effect Transistors (MODFETs) are mainly achieved by scaling down dimensions using high resolution electron beam lithography. But this trend towards the reduction of gate length seemed to have been stopped for a few years. The limitation is not only related to technological difficulties but above all to short-channel effects that occur at gate length less than $0.1 \mu\text{m}$ to the detriment of saturation behaviour. Indeed, these short-channel effects lead to a high drain conductance g_D , which prevents the pinchoff and results in a shift in threshold voltage that is then dependent on drain voltage [1-3]. Recently, 50 nm gate pseudomorphic MODFETs have been fabricated using a self-aligned-gate technique [4]. A very high value of extrinsic transconductance

($g_m = 1\,740$ mS/mm) has been achieved but in return the drain conductance g_D was very high too, leading to a poor g_m/g_D ratio of 6.5 that is sufficient for most microwave applications but not at all for logic applications.

To provide against short-channel effects with keeping advantage of a high overshoot velocity due to ballistic transport [1], we propose a dual-gate (DG) AlGaAs/InGaAs/GaAs MODFET with gates 50 nm long. The gate closer to the source (G1) is used to modulate the electron injection in the channel, as in a single-gate (SG) transistor, while the gate closer to the drain (G2) is biased to a constant voltage V_{G2S} always more positive than V_{G1S} . The role of the second gate is to create a slightly depleted region in the channel. As soon as the charge domain is forming between the two gates, this region becomes so resistive as to absorb the additional drain voltage. In this way, the electron injection in the active zone is only controlled by the first gate voltage V_{G1S} and is not influenced by the drain voltage. This configuration allows to spectacularly improve the saturation behaviour.

In this work, we have thus investigated the saturation mechanisms that occur in SG-MODFET and DG-MODFET. Both devices have been simulated with 50 nm gate lengths using two-dimensional Monte Carlo model that is actually the most accurate method to take into account the nonstationary transport that predominates in such short heterostructures [5]. The simulated SG-MODFET has the feature to present a quite good saturation behaviour at high gate voltage, i.e., in open-channel range of operation, and a poor one near the pinchoff. We have studied these two different regimes whose description is a necessary introduction to facilitate the analysis of DG-MODFET operation. The latter device exhibits an excellent saturation behaviour on the entire range of gate voltage leading to very good values of g_m/g_D ratio.

Section 2 describes the simulated structures. Sections 3 and 4 report respectively the physical operating of SG-MODFET and DG-MODFET. Section 5 presents the comparative device performances. In last section, section 6, we synthesize the results of this work and we present suggestions for future applications.

2. The simulated structures.

The device structures (Fig. 1) consist of an undoped GaAs buffer layer, on which are grown a non-intentionally doped 15 nm thick strained $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer (the channel), a 5 nm thick spacer layer (undoped $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$) and a N^+ -doped AlGaAs layer ($N_D = 2 \times 10^{18} \text{ cm}^{-3}$). The source and drain N^+ contact regions are doped to $2 \times 10^{18} \text{ cm}^{-3}$. The total thickness of AlGaAs layers in all gated regions is 22 nm, including the spacer. The source-gate distance L_{SG} is 0.1 μm in each device and in the SG-MODFET the gate-drain distance L_{GD} is 0.5 μm . In the DG-MODFET, the gate-to-gate separation is 0.1 μm and the second gate to drain distance is 0.35 μm . The gated regions of the channel are named respectively control-zone (under G1) and screen-zone (under G2), which will be justified further on. The Schottky-barrier height Φ_B is assumed to be 0.75 eV.

Our two-dimensional particle Monte Carlo model has been described in details elsewhere [1, 6]. At every metal-semiconductor surface the boundary conditions fix the electrostatic potential, when in the cells adjacent to the ohmic contacts the equilibrium electron concentration is assumed to be recovered ($n = N_D$). This last boundary condition is thus the condition of injection of carriers whose initial energy and momentum are specified by a Maxwellian distribution. A large number of particles, typically here 25 000, is initially implanted in the device. It is worth noting that the two-dimensional quantization of electron energy states in the quantum well is not accounted for in our 2DG program: the low-field carrier velocity is not much affected by such a simplification, at least at room temperature, as was shown both experimentally and theoretically [7-9]. Band structure and main scattering

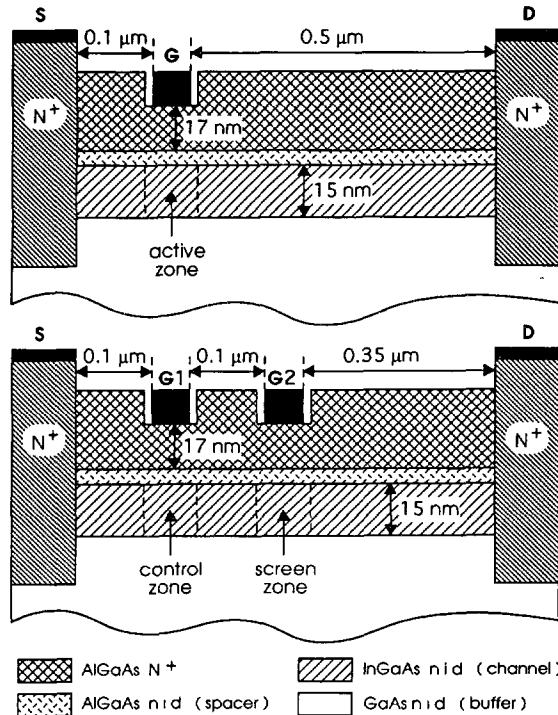


Fig. 1. — Schematic cross section of simulated SG-MODFET and DG-MODFET.

parameters in strained InGaAs such as the effective mass m^* in Γ -valley, the energy of polar optical phonon $\hbar\omega_0$ and the conduction band discontinuity ΔE_c with AlGaAs are taken from relevant experimental measurements reported in the literature [10-12]. Other parameters that are not available from experimental measurements were extrapolated from well known bulk material parameters.

3. Single-gate MODFET operation.

Figure 2 shows the drain current characteristics $I_D(V_{DS})$ of the SG-MODFET. At high gate bias voltages, i.e., in open-channel range of operation, the drain current is quite well saturated as soon as the drain voltage is reaching about 0.5 V. But at low V_{GS} , i.e., in pinchoff range of operation, the drain current increases almost exponentially with V_{DS} and seems to saturate only at high V_{DS} . This is resulting in a high drain conductance g_D , which is detrimental for high frequency applications because of the decrease of the maximum oscillation frequency, and for logic operation because of the imprecise definition of the low-state logical level.

The saturation of the drain current generally requires the existence of two zones in the channel between source and drain: a gate-controlled zone along which is dropped the saturation drain voltage V_{Dsat} and a space charge layer (SCL) which is supporting any further increase of bias drain voltage. The SCL acts as a screen for the active zone against the variations of drain voltage: the conditions of electron injection in the active zone become independent on V_{DS} .

The saturation behaviour, depending on gate voltage, is well illustrated in figure 3 where we have plotted the profile of the bottom of the conduction band along the channel for two drain

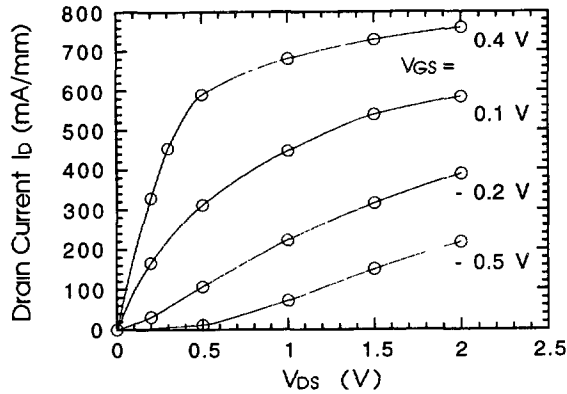


Fig. 2. — Drain characteristics of SG-MODFET.

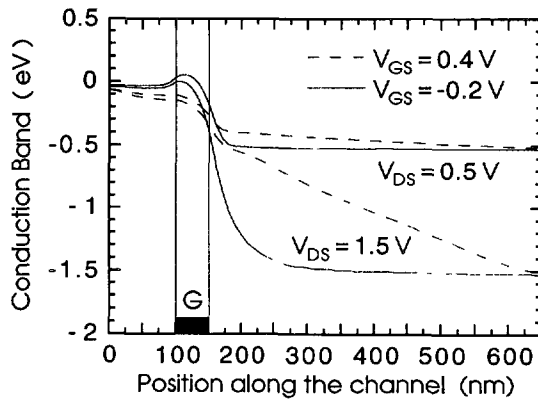


Fig. 3. — Profile of bottom of conduction band along the channel in SG-MODFET in open-channel operation ($V_{GS} = 0.4$ V), and in pinchoff operation ($V_{GS} = -0.2$ V), for two different drain voltages.

voltages, in both cases of open channel operation ($V_{GS} = 0.4$ V, dashed lines) and pinchoff operation ($V_{GS} = -0.2$ V, solid lines). At high V_{GS} , beyond the onset of saturation ($V_{DS} \geq 0.5$ V), the conduction band is nearly fixed at the end of the gate and the additional drain voltage is dropped between the gate-end and the drain. The gated region, i.e., the active zone, seems to be screened from drain potential variations. On the opposite, in pinchoff operation the whole drain voltage is applied across the active zone that is to say the longitudinal component of the electric field goes on increasing dramatically as V_{DS} does.

These variations in conduction band profiles have direct consequences on the electron density in the active zone. In figure 4 the minimum value of electron density n_s in the gated-zone of the channel is plotted as a function of V_{DS} . In open channel operation ($V_{GS} = 0.4$ V, dashed lines), an increase in V_{DS} tends first to deplete the active zone (for $V_{DS} < 0.5$ V) and the previously described screening effect shows itself in the saturation of the curve of n_s against V_{DS} . But in pinchoff operation ($V_{GS} = -0.2$ V, solid lines), the electron density in the active zone increases as drain voltage is increased. As a matter of fact, at this gate voltage the electron injection from source side is controlled by a potential barrier and this one is modulated by variations of drain potential, which prevents the current saturation.

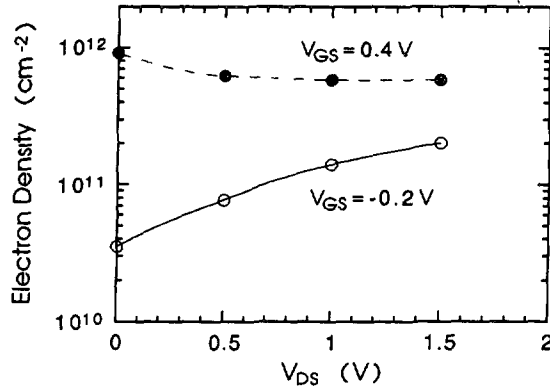


Fig. 4. — Minimum electron density in the gated-zone of the SG-MODFET channel versus V_{DS} for two V_{GS} .

The physical mechanisms that lead to these different behaviours according to the gate voltage can be described as follows. Since most electrons cross the active zone ballistically [1], their momentum is parallel to the interface and they cannot easily transfer to the high bandgap material. But as soon as they have a sufficient energy ($\epsilon_{\Gamma L} = 0.36$ eV), they have a great probability to transfer in the lateral valleys and to initiate the arising of an accumulation of slow electrons (a charge domain) just beyond the gate-end. The effect of intervalley scattering is to randomize the electron velocities and to increase the electron effective masses, which leads to considerably reduce the average electron drift velocity. At high V_{GS} , the charge domain grows easily. It is pointed out in figure 5a that is a plot of the spatial distribution of

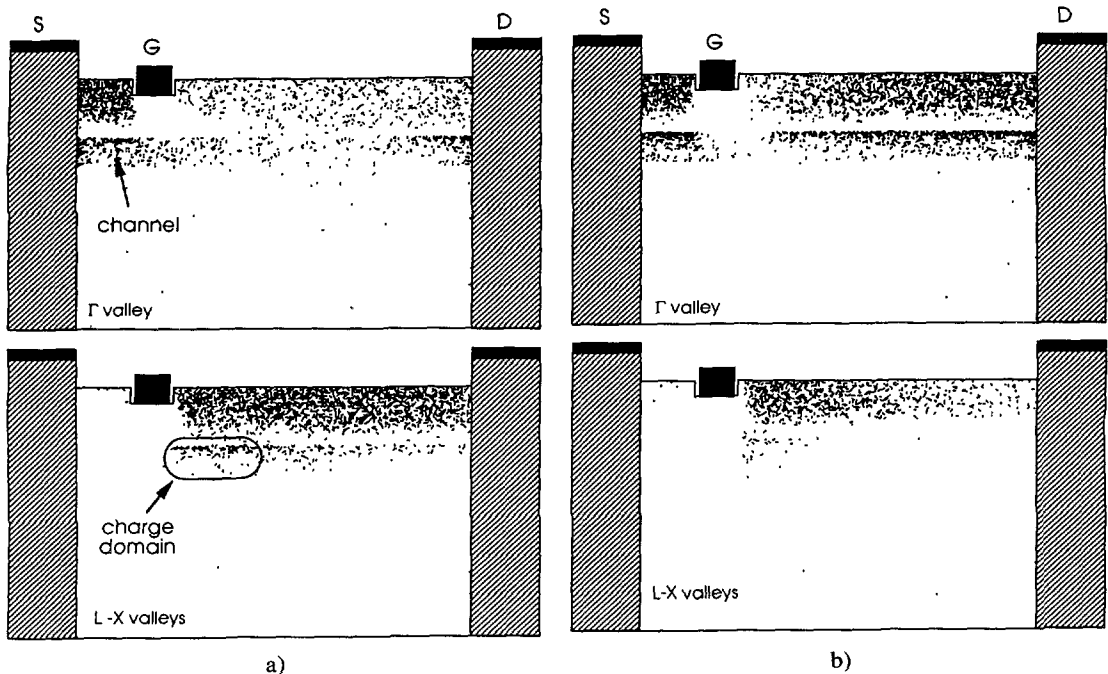


Fig. 5. — a) Electron repartition in SG-MODFET for $V_{DS} = 1$ V in open-channel operation ($V_{GS} = 0.4$ V). b) Electron repartition in SG-MODFET for $V_{DS} = 1$ V in pinchoff operation ($V_{GS} = -0.2$ V).

electrons in the device at $V_{DS} = 1$ V and $V_{GS} = 0.4$ V. The gate-to-drain region of the channel is then supplied with a great amount of heated and very little mobile electrons. It becomes more resistive than the active zone and tends to be depleted with absorbing the increase in drain potential. The entity « accumulation-depletion » constitutes the SCL that is necessary for the current saturation. At low V_{GS} , the amount of k -space transferred electrons beyond the gate-end is smaller are shown in figure 5b that is a plot of the spatial distribution of electrons at $V_{DS} = 1$ V and $V_{GS} = -0.2$ V. This is not enough to initiate the previously described screening effect. The entire further drain potential remains applied to the active zone, which lowers the potential barrier at the gate entrance of the channel and increases the electron injection. This additional injection does not favour a lot the charge domain growth because it is concomitant with an increase of electric field. Electrons, which are mainly ballistic under the gate, reach then such an energy that, after experiencing an intervalley scattering, many of them easily transfer into the very conductive AlGaAs upper layer and escape from charge domain.

The introduction of a second gate in the gate-to-drain region has been thought up to improve the charge domain growth and the screening effect, which is necessary for a good saturation behaviour on the full range of gate voltage.

4. Dual gate MODFET operation.

The gate closer to the source (G1, the control-gate) is used to modulate the electron injection in the channel, as in a single-gate FET, and the gate closer to the drain (G2, the screengate) is biased to a constant voltage V_{G2S} always more positive than V_{G1S} . The role of the second gate is to create a slightly depleted region in the channel, so that, as soon as the charge domain is forming between the two gates, this region becomes so resistive as to absorb the additional drain voltage.

Figure 6 shows the drain current characteristics $I_D(V_{DS})$ of the DG-MODFET. The screengate to source voltage V_{G2S} was fixed to 0.6 V. To describe the device operation we will consider the single case of pinchoff gate voltage ($V_{GS} = -0.2$ V) at which the improvement of the saturation is specially obvious compared to the SG-MODFET (Fig. 2).

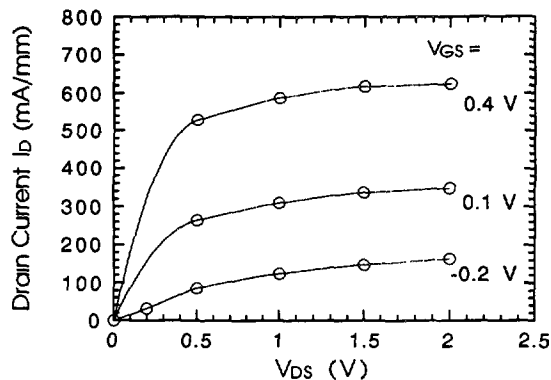


Fig. 6. — Drain characteristics of DG-MODFET for $V_{G2S} = 0.6$ V.

The respective role of the two gates in the control and the saturation of the current is well demonstrated by the conduction band profiles along the channel at two V_{DS} (Fig. 7, dashed lines) in comparison with the same profiles of the SG-MODFET (solid lines). Below 0.5 V drain voltage, i.e., before the current saturation, the profiles of conduction band are nearly the

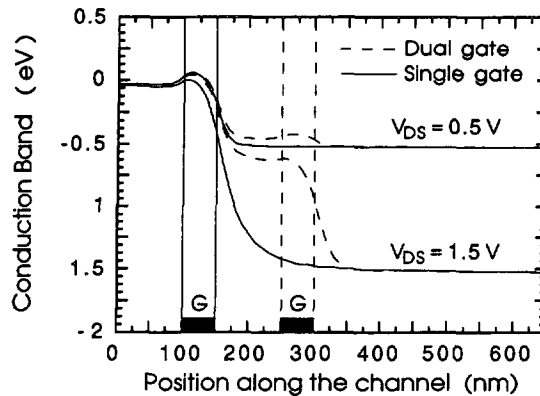


Fig. 7. — Profile of bottom of conduction band along the channel in SG-MODFET (solid lines) and DG-MODFET (dashed lines) in pinch-off operation, for two different drain voltages.

same in both devices. The drain-to-source potential is entirely absorbed in the less dense region of the channel that is to say under the control-gate. In this drain voltage range, the screen-gate of DG-MODFET has no influence of the device operating and current values are very close in both DG-MODFET and SG-MODFET. Beyond 0.5 V drain voltage, the situation is very different according to the device. Contrary to the case of the SG-MODFET, the additional drain voltage applied to the DG-MODFET is not absorbed under the control-gate but under the second gate that screens the first gated-region from drain potential variations. The electron injection is then well commanded by the control-gate and the current saturates. This justifies the names of control-gate (G1) and screen-gate (G2) used in this paper.

This is well confirmed by the evolution of the minimum value of electron density n_s in the first gated zone of the channel (named control-zone) with drain voltage (Fig. 8). Beyond 0.5 V drain voltage, n_s tends to become independent of V_{DS} in DG-MODFET (dashed line) contrary to the case of SG-MODFET (solid line).

The screening mechanism occurring in the DG-MODFET can be described as follows. At low V_{DS} the longitudinal electric field builds in the less resistive zone of the channel, i.e., in the control-zone. When V_{DS} is high enough, the charge domain of k -space transferred electrons

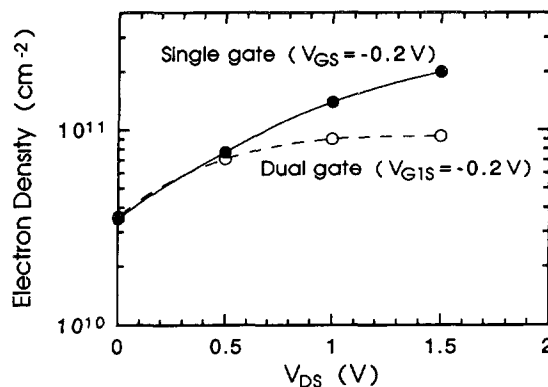


Fig. 8. — Minimum electron density in the control-zone of SG-MODFET (solid lines) and DG-MODFET (dashed lines) in pinch-off operation versus V_{DS} .

grows just behind the control-gate. In this case, the charge domain is well trapped inside the channel, between the two gates, since the presence of a second gate, under which the large band gap layer is entirely depleted, forces the electrons that spatially transfer into the upper AlGaAs layer to come back in the channel. The charge domain is pointed out in figure 9 that is a plot of the spatial distribution of electrons in the device at $V_{DS} = 1$ V, $V_{G1S} = -0.2$ V, and $V_{G2S} = 0.6$ V. The screen zone is then supplied with heated and very little mobile electrons. It becomes more resistive than the region under the control-gate and absorbs the additional drain potential. The entity « charge domain — screen-zone » constitutes the SCL, which is necessary for the current saturation.

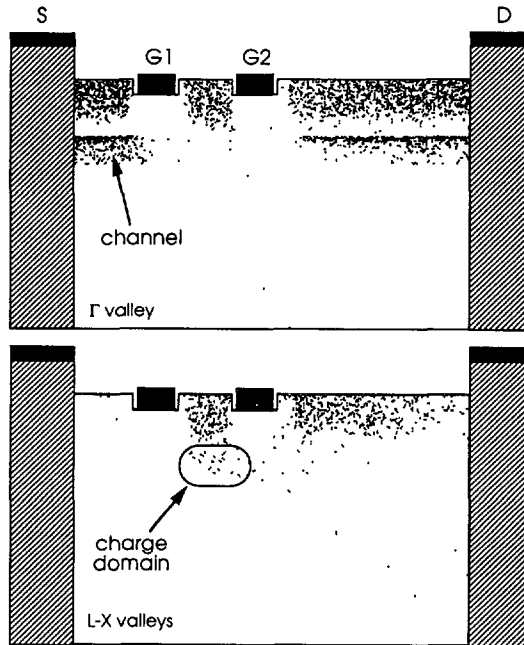


Fig. 9. — Electron repartition in DG-MODFET for $V_{DS} = 1$ V in pinchoff operation ($V_{G1S} = -0.2$ V, $V_{G2S} = 0.6$ V).

Thus, the following gate-bias conditions must be respected for a good device operating of the DG-MODFET :

- 1) V_{G1S} changes parametrically to modulate the electron injection and V_{G2S} is fixed ;
- 2) V_{G1S} have to be less than V_{G2S} for the control-region to be initially more resistive than the screen-region. The electrons must be first accelerated under the control-gate and the screen-gate must have no influence on the electron transport as long as the k -space transfer is not occurring ;
- 3) V_{G2S} have to be chosen not too high for the channel electron density and the conductivity under the screen-gate to be less than in the ungated regions. As soon as the charge domain is growing, the screen region must be the more resistive region of the channel to be able to absorb the entire additional drain voltage.

5. Device performances.

In consideration of the greater complexity of a dual-gate device compared with a single-gate one, the utilization of the DG-MODFET is justified only if it offers advantages over all SG-MODFETs fabricated by the same technological processing. Thus, to show off the advantages of DG-MODFET we now compare the performances of the simulated DG device with those of two SG-MODFETs having the same vertical geometry but with respective gate lengths of 50 and 100 nm. We have considered three factors of merit, i.e., the transconductance g_m , the current gain cutoff frequency f_T , and the g_m/g_D ratio that is an important parameter in view to logic applications.

The microwave performances of transistors can be very well determined using high frequency small-signal Monte Carlo simulations [13]. This specific approach requires large computer time to extract Fourier coefficients of terminal currents with a good precision. We have used here a simpler approach using steady-state Monte Carlo simulations, which has been justified for this kind of devices. The electrical parameters, such as transconductance, gate capacitance C_G and drain conductance, are derived from steady-state values of drain current I_D and total electron charge Q_i inside the device. Assuming impurities to be fully ionized, the total gate capacitance C_G is given by the slope of Q_i against the control-gate voltage, i.e., V_{GIS} in case of dual-gate device. The current gain cutoff frequency can be then determined using the classical formula $f_T = g_m/2\pi C_G$ that has been proved correct, in a first approach, for single-gate MODFETs [13].

The devices' characteristics calculated at $V_{DS} = 1.5$ V are sum up in table I. The 50 nm SG-MODFET exhibits a quite low maximum g_m (760 mS/mm). Short channel effects are responsible for this : as shown in figure 2, if g_D is quite low in open-channel regime it is very high near the pinchoff, which then affects the variation of I_D per V_{GS} swing. Short-channel effects are much less important in the 100 nm SG-MODFET that exhibits a higher maximum g_m (975 mS/mm) despite the longer gate. The DG-MODFET, that offers an excellent saturation behaviour on the full range of control-gate voltage, produces a slightly better g_m (990 mS/mm) than the latter. The 50 nm SG-device takes advantage of a lower gate capacitance to reach the best maximum f_T (335 GHz). But the DG-MODFET, that is not affected by short-channel effects and is then very well commanded by the control-gate, exhibits a very high g_m/g_D ratio (27) than SG-MODFETs (5.8 and 11.6). This is of great interest for many applications, especially for high speed logic applications.

Table I. — *Best value of device characteristics calculated at $V_{DS} = 1.5$ V.*

Device	50 nm SG	100 nm SG	DG
g_m (mS/mm)	760	975	990
f_T (GHz)	335	270	285
g_m/g_D	5.8	11.6	27

6. Conclusions.

The dual-short-gate MODFET allows to provide against short channel effects and then to obtain an excellent saturation behaviour on the entire range of gate voltage, while achieving very good values of intrinsic transconductance and cutoff frequency. If this improvement is not

deciding in view of microwave applications, such a dual-gate structure could be a good potential candidate for very high speed logic applications. This study has shown off the principles of both single-gate and dual-gate MODFET operation but it should be noted that the simulated DG-device was not optimized and it may be still improved with modifying the gate-to-gate separation or the screen-gate length. A deciding improvement of MODFET performances could be obtained by fabricating a 50 nm DG structure using, if possible, a self-aligned-gate technology. Such a configuration should allow to achieve very high g_m , f_T and f_{max} values while providing against short-channel effects and then achieving excellent g_m/g_D ratios.

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