



HAL
open science

Electrical properties of thin anodic silicon dioxide layers grown in pure water

François Gaspard, A. Halimaoui, Gérard Sarrabayrouse

► To cite this version:

François Gaspard, A. Halimaoui, Gérard Sarrabayrouse. Electrical properties of thin anodic silicon dioxide layers grown in pure water. *Revue de Physique Appliquée*, 1987, 22 (1), pp.65-69. <10.1051/rphysap:0198700220106500>. <jpa-00245516>

HAL Id: jpa-00245516

<https://hal.science/jpa-00245516v1>

Submitted on 4 Feb 2008

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

Classification

Physics Abstracts

73.40Q — 73.60H — 81.15

Electrical properties of thin anodic silicon dioxide layers grown in pure water (*)

F. Gaspard, A. Halimaoui and G. Sarrabayrouse (+)

Laboratoire de Spectrométrie Physique associé au CNRS, Université Scientifique, Technologique et Médicale de Grenoble, B.P. 87, 38402 St Martin d'Hères Cedex, France

(+) LAAS CNRS, 7, avenue Colonel Roche, 31077 Toulouse Cedex, France

(Reçu le 4 juin 1986, révisé le 1^{er} septembre, accepté le 30 septembre 1986)

Résumé. — Des couches très minces de SiO₂ (40-100 Å) peuvent être obtenues très simplement par oxydation électrochimique du silicium dans l'eau pure. Un contrôle très précis de l'épaisseur est possible par simple coulométrie. Les couches de SiO₂ sont très homogènes en épaisseur et dépourvues d'effets de bord et de défauts du type « pinholes ». Les propriétés électriques des oxydes ainsi que celle de l'interface Si/SiO₂ ont été étudiées en réalisant des structures métal-oxyde anodique-semiconducteur ; le métal étant soit le chrome, soit l'aluminium. Les résultats de cette étude montrent que ces oxydes présentent une faible densité de charge à l'interface Si/SiO₂ ($\leq 10^{11} \text{ cm}^{-2}$), une densité d'états d'interface comparable à celle obtenue avec des oxydes thermiques de même épaisseur ($\sim 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) et des champs de claquage particulièrement élevés (11 à 14 MV cm⁻¹). Il apparaît ainsi qu'aucune pollution des couches d'oxyde ne se produit pendant l'électrolyse. L'étude de l'injection Fowler-Nordheim conduit, par ailleurs, à des hauteurs de barrière métal-oxyde très satisfaisantes (2,5 à 2,8 eV) même pour un oxyde aussi mince que 44 Å.

Abstract. — Thin silicon dioxide layers (40-100 Å) can be successfully produced by anodization of silicon in pure water. The resulting layers are very homogeneous and pinhole free. The monitoring of the SiO₂ thickness is accurately achieved by simple coulometry. The electrical properties of the oxide layers and the associated Si/SiO₂ interface have been investigated by forming metal-oxide-semiconductor (MOS) capacitors using the anodically grown oxide as the dielectric and aluminium or chromium as the metal. This investigation shows a low charge density at the Si/SiO₂ interface ($\leq 10^{11} \text{ charges} \cdot \text{cm}^{-2}$) and an interface states density comparable to that obtained with thermally grown SiO₂ ($10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$). The dielectric breakdown occurs at high fields (11 to 14 MW . cm⁻¹). These results show that there is no pollution during the electrolysis. Furthermore, the metal to oxide barrier heights remained high (2.5 to 2.8 eV) even for thin (44 Å) SiO₂ layers.

1. Introduction.

Very thin silicon dioxide layers (20-200 Å) have attracted wide interest in many applications such as short channel MOSFET and EPROMS. Until now, the most commonly used technique for the fabrication of the SiO₂ films in MOS device is the thermal oxidation of silicon.

On the other hand, oxide films can be grown on

silicon by an electrochemical process [1-5]. Silicon dioxide layers with good electrical properties are obtained when the anodization is performed in pure water at low current density ($10 \mu\text{A}/\text{cm}^2$) [6].

The electrochemical process of oxidation has some advantages over the thermal process :

1) Accurate control of the oxide thickness, especially in the 20-30 Å thickness range, is easily obtained.

2) As most anodic oxides, the rate of growth and the electric field across the SiO₂ films are exponentially dependent [7]. Consequently, the layers are very homogeneous and pinhole free.

(*) Work supported by « Groupe circuits intégrés au silicium » (G.C.I.S.).

In this paper, the electrical properties (interface charges, oxide charges, interface states, electrical conduction and dielectric breakdown) of thin anodic SiO_2 layers grown in pure water are investigated using MOS capacitors.

2. Experimental procedure.

Monitoring of the oxide thickness is achieved by coulometry using the calibration curve given in figure 1, where Q is the total charge passed through the electrochemical cell (the time integral of the current) and d_{ox} is the oxide thickness, determined by ellipsometry. For an imposed current density of $10 \mu\text{A} \cdot \text{cm}^{-2}$ and for thicknesses less than about 25 \AA the potential of the silicon anode remains lower than the oxidation potential of water. As a result, the silicon is oxidized with an electrolysis efficiency of 100 %. For thicknesses greater than 25 \AA the anode potential becomes higher than the decomposition potential of water ; both silicon and water are oxidized and the efficiency in SiO_2 formation drops to about 17 %.

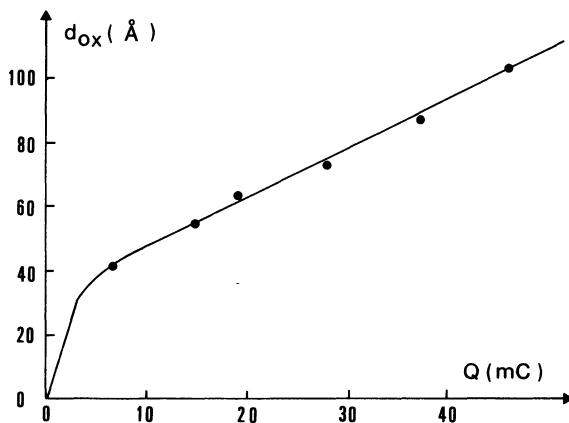


Fig. 1. — Oxide thickness versus total charge passed through the electrochemical cell. Current density : $10 \mu\text{A} \cdot \text{cm}^{-2}$; area : 0.75 cm^2 .

Metal-oxide-semiconductor (M.O.S.) capacitors have been fabricated on $5 \Omega \cdot \text{cm}$ p-type $\langle 100 \rangle$ oriented silicon wafer. After a standard cleaning the wafers (38 mm diameter) were oxidized at 1050°C in dry O_2 during four hours. Windows have been opened by oxide etching, and the freshly etched silicon surface (total area = 1.7 cm^2) is anodically oxidized in pure water (the water resistivity is about $18 \text{ M}\Omega \cdot \text{cm}$ at 20°C) using constant current density ($10 \mu\text{A}/\text{cm}^2$). A post oxidation anneal is performed at 700°C in N_2 during one hour. Then 3000 \AA thick square chromium (wafer 1 and wafer 3) or aluminium (wafer 2) dots were evaporated onto the oxide films (dots area : $300 \times 300 \mu\text{m}^2$, $100 \times 100 \mu\text{m}^2$ and $40 \times 40 \mu\text{m}^2$).

When aluminium is used (wafer 2) a post metallization anneal is performed at 450°C in N_2 during half an hour. Electrical measurements have been made using the apparatus previously described [11]. For each capacitor, high (1 MHz) and low (1 kHz) frequency capacitance-voltage measurements ($C-V$) were recorded, followed by current-voltage measurements ($I-V$). The $I-V$ has been recorded up to dielectric breakdown.

For some samples, thermal stress has been applied under bias, followed by $C-V$ measurements in order to measure the mobile charges density.

All the tested capacitors have been found defect free.

3. Experimental results and discussion.

3.1 LAYER HOMOGENEITY. — The oxide thickness, measured using the $C-V$ technique [8], was found to be in good agreement with the coulometric method.

For a given wafer (38 mm diameter) the oxide thickness is homogeneous ; as shown in figure 2a and b, where d_{ox} is the oxide thickness and N the number of tested capacitors, the thickness was found to be $96 \pm 3.5 \text{ \AA}$ for wafer 1 and $44 \pm 3.5 \text{ \AA}$ for wafer 3 ($3.5 \text{ \AA} \approx 1$ monolayer).

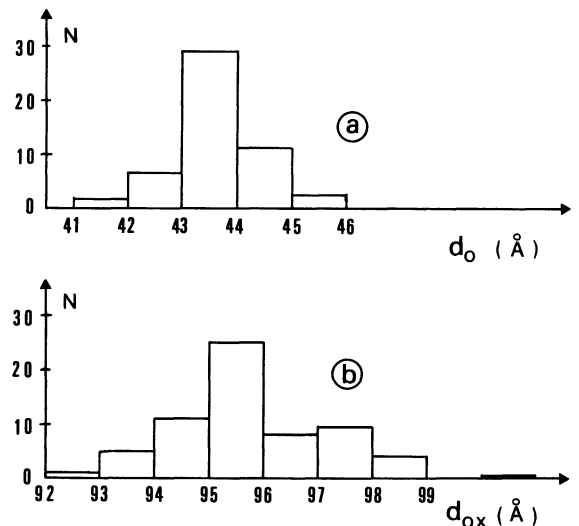


Fig. 2. — Layers homogeneity. a) wafer 3 (44 \AA) ; b) wafer 1 (96 \AA).

3.2 INTERFACE FIXED CHARGE. — The total amount of fixed charge at the Si/SiO_2 interface is determined using the shift of the flat-band voltage :

$$N_{\text{FC}} = \frac{V_{\text{FB}}^{\text{M}} - V_{\text{FB}}^{\text{C}}}{q} \cdot C_{\text{ox}} \text{ (charges} \cdot \text{cm}^{-2}\text{)}$$

C_{ox} is the oxide layer capacitance per unit area. V_{FB}^{M} is the measured flat-band voltage (Fig. 3) deduced from the theoretical flat-band capacitance $C_{\text{FB}} =$

$\epsilon_i / \left[d_{\text{ox}} + \frac{\epsilon_i}{\epsilon_s} \left(\frac{kT\epsilon_s}{pq^2} \right)^{1/2} \right]$ [9], where ϵ_i and ϵ_s are the permittivities of the insulator and the semiconductor respectively, and p is the bulk hole density.

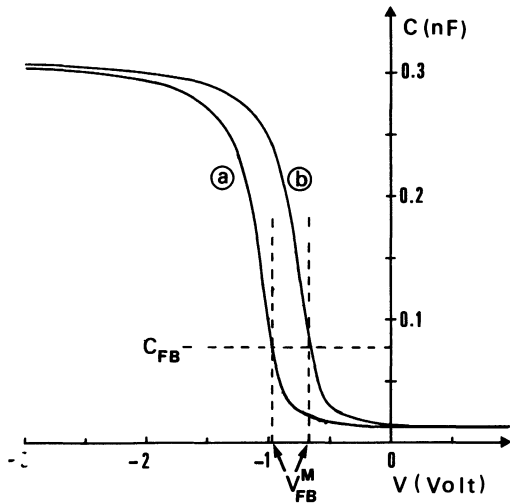


Fig. 3. — Typical capacitance-voltage curves. Device area = $9 \times 10^{-4} \text{ cm}^2$; $d_{\text{ox}} = 98 \text{ \AA}$. a. Aluminium gate; b. Chromium gate.

V_{FB}^{C} is the flat-band voltage calculated from the relation :

$$V_{\text{FB}}^{\text{C}} = \frac{1}{q} \left(\phi_m - \chi - \frac{\epsilon_g}{2} - kT \ln \frac{p}{n_i} \right)$$

where $\phi_m - \chi$ is the metal to semiconductor barrier height and ϵ_g the energy band gap of the semiconductor. Assuming an aluminium to silicon barrier height equal to -0.11 eV [10], the maximum shift of the flat-band voltage is found to be about 0.02 V . As this value is in the range of the inaccuracy in V_{FB}^{C} ($\pm 0.040 \text{ V}$), no accurate value of the total amount of fixed charge near the Si/SiO₂ interface can be deduced from these measurements.

However, as a charge density of $10^{11} \text{ charges} \cdot \text{cm}^{-2}$ gives rise to a flat-band shift of about 0.05 V , this value can be taken as an upper limit of the charge density. Moreover recent results obtained with thicker anodic oxide (900 \AA) grown in the same conditions lead to a charge density near the Si/SiO₂ interface in the range $1.3 \times 10^{10} \text{ charges} \cdot \text{cm}^{-2}$. In the case of a chromium gate, the assumption of a barrier height of -0.06 eV [10] leads to a shift of the observed flat-band voltage, corresponding to a negative charge of $5 \times 10^{11} \text{ charges} \cdot \text{cm}^{-2}$. However, the existence of such a charge is questionable because the same shift of the flat-band voltage has been observed with thermal SiO₂ [11].

3.3 MOBILE IONIC CHARGE. — The C-V method has been used to measure mobile ionic charge density [12] for wafer 1 and 3 (chromium gate).

First, a high frequency (1 MHz) C-V curve is recorded. The MOS capacitor is then heated to $200 \text{ }^\circ\text{C}$ during half an hour under high electric field ($\pm 4 \text{ MV} \cdot \text{cm}^{-1}$). Finally, the MOS capacitor is cooled back to room temperature and another C-V curve recorded.

For all the samples, positive mobile charge density between 1 to $3 \times 10^{11} \text{ charges} \cdot \text{cm}^{-2}$ has been measured. The origin of this positive charge is at this time unclear. It could be related to protons formation during electrolysis [6].

3.4 INTERFACE STATES. — Typical high (1 MHz) and low (1 kHz) frequency capacitance-voltage curves are shown in figure 4.

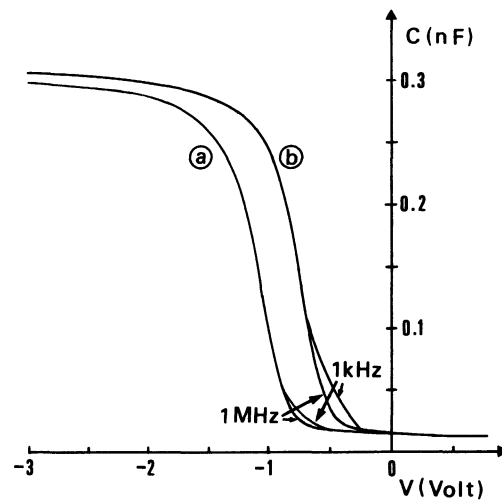


Fig. 4. — High and low frequencies capacitance-voltage curves. Device area = $9 \times 10^{-4} \text{ cm}^2$. a. Aluminium gate, $d_{\text{ox}} = 99 \text{ \AA}$; b. Chromium gate, $d_{\text{ox}} = 97 \text{ \AA}$.

The surface states density is extracted from the difference between the H.F. and L.F. capacitance-voltage curves. Figure 5 shows plots of the surface states density N_{ss} as a function of the energy within the forbidden gap referred to the valence band ϵ_v . The density peak is in the range 1 to $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Furthermore the shape of the density peak, its location near the valence band and its value are in agreement with results obtained with thermally grown oxides [11].

3.5 CURRENT-VOLTAGE CHARACTERISTIC. — Figure 6 shows typical I-V curves corresponding to electron injection from the metal.

The current is found to be proportional to the device area. This means that there is not thinning of the anodic oxide near the edge of the isolation oxide, contrary to

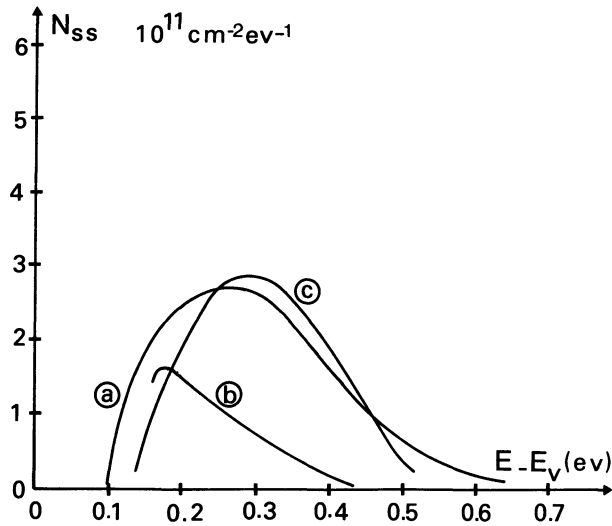


Fig. 5. — Energetic distribution of interface states. a. Chromium gate, $d_{ox} = 44 \text{ \AA}$; b. Aluminium gate, $d_{ox} = 97 \text{ \AA}$; c. Chromium gate, $d_{ox} = 97 \text{ \AA}$.

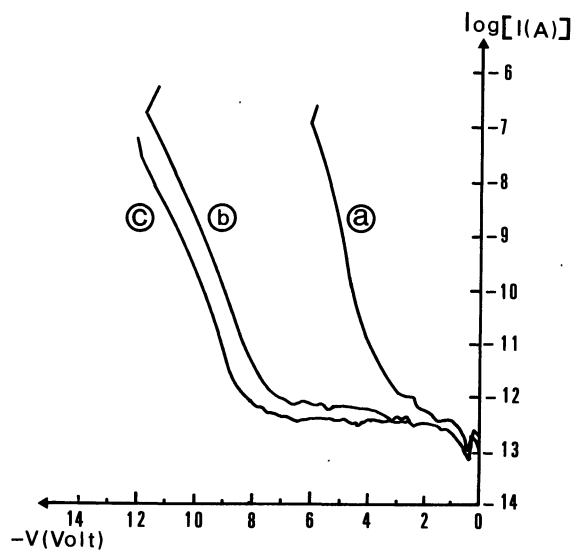


Fig. 6. — Current-voltage curves. a. Chromium gate, $d_{ox} = 44 \text{ \AA}$; b. Chromium gate, $d_{ox} = 95 \text{ \AA}$; c. Aluminium gate, $d_{ox} = 95 \text{ \AA}$.

some observations with thermal SiO_2 [13]. The classical Fowler-Nordheim formula is given by [14]:

$$j/\epsilon_{ox}^2 = C \exp\left(-\beta/\epsilon_{ox}\right)$$

ϵ_{ox} being the electric field across the oxide. The relationship between the slope β and the metal to oxide barrier height ϕ_0 , expressed in eV, assuming $m_{ox}/m = 0.5$ [15] is given by:

$$\phi_0 = (\beta/4.83 \times 10^7)^{2/3}.$$

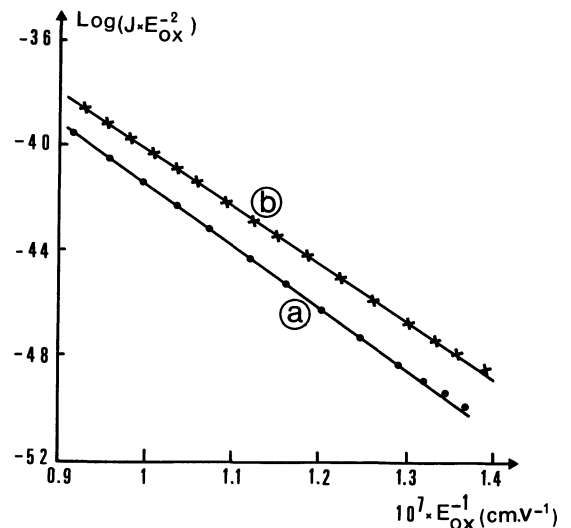


Fig. 7. — Current density versus electric field in Fowler-Nordheim graph. a. Aluminium gate, $d_{ox} = 95 \text{ \AA}$; b. Chromium gate, $d_{ox} = 95 \text{ \AA}$.

The plot of j/ϵ_{ox}^2 vs. $1/\epsilon_{ox}$ (Fig. 7) is linear within a large current range for the thicker oxide (95 \AA). For the thinner one (44 \AA), direct tunnelling is observed below electric fields of about $8 \text{ MV} \cdot \text{cm}^{-1}$.

The metal to oxide barrier height can be calculated from the slope of those curves. The results are given in table I and show satisfactory agreement with measurements obtained on thermally grown oxide.

Table I.

d_{ox} (Å)	Metal	ϕ_0 (eV)	Reference
44	Cr	2.47 (*)	this work
72	Cr	2.90	[11]
90	Cr	2.76	[11]
98	Cr	2.68	this work
98	Al	2.82	this work
200-1 000	Al	3.13 (**)	[16]
200-1 000	Cr	2.96	[16]

3.6 BREAKDOWN ELECTRIC FIELD. — A statistical study of the dielectric breakdown has been done for all samples. The breakdown occurs for electric field between 12 and 14 $\text{MV} \cdot \text{cm}^{-1}$ for the thin oxide (44 \AA) and between 11 and 13 $\text{MV} \cdot \text{cm}^{-1}$ for the thicker one (95 \AA).

(*) This value must be taken with caution owing to the possibility of direct tunnelling.

(**) Average of 23 °C and 100 °C results. All other results in this table are given for room temperature.

4. Conclusion.

The electrochemical oxidation of silicon in pure water leads to very homogeneous SiO₂ layers, with a low fixed charge density ($\leq 10^{11} \text{ cm}^{-2}$) and high breakdown electric fields (11 to 14 MV . cm⁻¹). The surface states density is comparable to that obtained with thermal SiO₂, and the metal to oxide barrier heights remained high even for very thin samples. All these properties have been found to be very reproducible from device to device and stable after ten months.

Beside these results, the most interesting features of the process are probably its ability to give very homogeneous SiO₂ layers totally free of pinholes and defects, and the easiness to obtain accurately very thin oxide layers.

Owing to the difficulties encountered in the preparation of such oxides by the thermal process, the electrochemical oxidation of silicon in pure water could appear a very attractive method especially in the 20-100 Å thicknesses.

References

- [1] SCHMIDT, P. F. and MICHEL, W., *J. Electrochem. Soc.* **104** (1957) 230.
 - [2] DUFFEK, E. F. *et al.*, *Electrochem. Technol.* **3** (1965) 75.
 - [3] JAIN, G. C. *et al.*, *J. Electrochem. Soc.* **126** (1979) 89.
 - [4] REVESZ, A. G., *J. Electrochem. Soc.* **114** (1967) 629.
 - [5] BEYNON, J. D. E. *et al.*, *Solid State Electron.* **16** (1973) 309.
 - [6] GASPARD, F. and HALIMAOU, A., *Proc. Int. Conf. INFOS 85*, Toulouse, France (North Holland) 1986, p. 251.
 - [7] CABRERA, N. and MOTT, N. F., *Repts. Progr. Phys.* **12** (1948-49) 163.
 - [8] MASERJIAN, J., *J. Vacuum Sci. Technol.* **20** n° 6 (1974) 996.
 - [9] SZE, S. M., *Physics of Semiconductor Devices* (J. Wiley, New York).
 - [10] KAR, S., *Solid State Electron.* **18** (1975) 169.
 - [11] CAPILLA, J. and SARRABAYROUSE, G., *Revue Phys. Appl.* **19** (1984) 343.
 - [12] SNOW, E. H. *et al.*, *J. Appl. Phys.* **36** (1965) 1664.
 - [13] SHENG, T. T. *et al.*, *J. Electrochem. Soc.* **125** n° 3 (1978) 432.
 - [14] LENZLINGER, M. and SNOW, E. H., *J. Appl. Phys.* **40** (1969) 278.
 - [15] WEINBERG, Z. A., *J. Appl. Phys.* **53** n° 7 (1982) 5052.
 - [16] OSBURN, C. M. and WEITZMAN, E. J., *J. Electrochem. Soc.* **119** (1972) 603.
-