



HAL
open science

Silicon wafers for integrated circuit process

B. Leroy

► **To cite this version:**

B. Leroy. Silicon wafers for integrated circuit process. *Revue de Physique Appliquée*, 1986, 21 (8), pp.467-488. 10.1051/rphysap:01986002108046700 . jpa-00245465

HAL Id: jpa-00245465

<https://hal.science/jpa-00245465>

Submitted on 4 Feb 2008

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Classification

Physics Abstracts

81.10F — 81.40 — 61.70 — 62.20F

Silicon wafers for integrated circuit process

B. Leroy

Compagnie IBM France, Dept. 1817/14 E, B.P. 58, 91102 Corbeil Essonne Cedex, France

(Reçu le 12 février 1986, révisé le 28 avril, accepté le 6 mars 1986)

Résumé. — Le marché des circuits intégrés sera dominé pendant encore plusieurs années par des circuits réalisés sur des substrats de silicium. D'abord nous passons en revue comment les procédures de tirage du cristal impactent la qualité du silicium. Ensuite nous étudions comment les traitements thermiques affectent le comportement de l'oxygène et du carbone, et comment il en résulte une évolution de la qualité des tranches de silicium. En conclusion nous détaillons les exigences que les tranches doivent satisfaire à l'inspection de réception par l'utilisateur.

Abstract. — Silicon as a substrate material will continue to dominate the market of integrated circuits for many years. We first review how crystal pulling procedures impact the quality of silicon. We then investigate how thermal treatments affect the behaviour of oxygen and carbon, and how, as a result, the quality of silicon wafers evolves. Gettering techniques are then presented. We conclude by detailing the requirements that wafers must satisfy at the incoming inspection.

1. Which substrates for integrated circuits ?

The integration of many electronic components on the same substrate was achieved during the 1960's, as the replacement of germanium substrates by silicon substrates allowed to use planar process. Since this date, nearly all the integrated circuits (I.C.) in the world are built on silicon substrates. One of the reasons is the possibility to manufacture large dislocation free monocrystalline wafers.

This article explains first why silicon is still the most commonly used material in I.C. manufacturing. Then the requirements for the specifications and the quality of silicon wafers are presented, with a discussion of the technologies involved.

1.1 THE CHALLENGES FACING THE I.C. MANUFACTURING. — The I.C. industry is facing three major challenges :

— Increase the number of operations per second in the computer, the complexity of these operations, by decreasing the delays in the devices and in the packaging.

— Decrease the cost per operation at the machine level, by an increase in productivity especially by using larger wafer and by a larger integration of the circuits. Figure 1 gives the evolution of the number of logic circuits per chip and per module. This number doubles every year. The reduction of the cost of packaging needs a lower heat generation of the circuits.

— Decrease the failure rate at the chip and the packaging level, by the use of redundant circuits, a drastic control of cleanliness during manufacturing operations, the use of new materials for interconnections, and a reduction of the current densities involved.

1.2 PROGRESS IN I.C. ON SILICON SUBSTRATES. — The two main causes of progress in I.C. on silicon substrates are the reduction of the dimensions of the circuits, and the introduction of new types of circuits.

1.2.1 Scaling down. — The main laws of scaling down FET devices were developed by Dennard [1, 2]. He pointed out that one can reduce by an identical ratio all the length, the widths and the thicknesses, and by an other ratio the applied voltage or the dopant concentrations. This induces smaller delays and/or reduces heat generation. He showed that scaling reaches limits only for very small dimensions (fraction of a micron). In the interconnections, a smaller delay needs no or small reduction of the thicknesses, compared to lengths and widths ; but the main progresses are due to the change in the nature of the wires : more complex circuits, reduction of cables, change in the modules and in the cards. Figure 2 compare the system delay between 3033 and 3081 technologies. The improvements due to progresses in packaging was larger than what would be obtained by reducing the chip delay alone, for instance by using circuits in gallium arsenide. Chips and packaging improvements must progress at a similar rate.

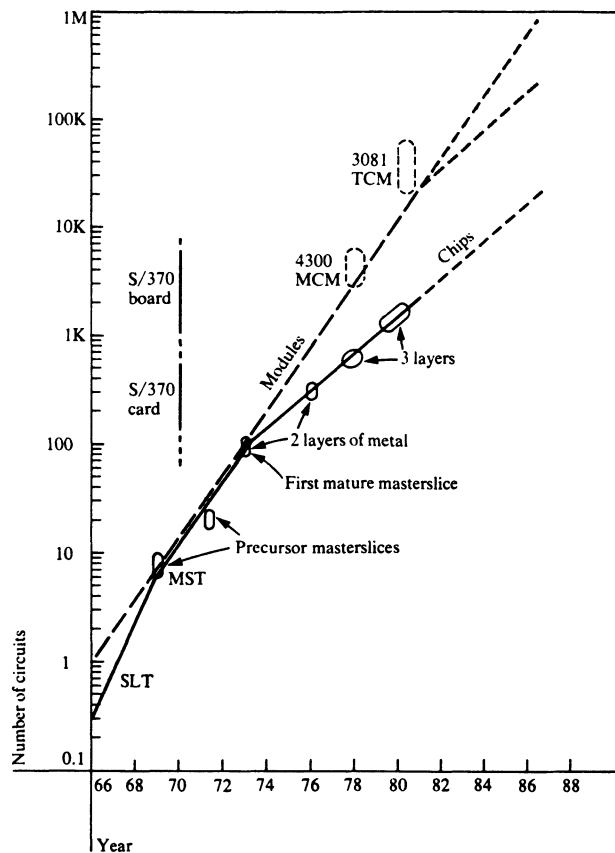


Fig. 1. — Evolution of the number of logic circuits on a single chip (full line) and on modules (dotted line) in IBM computers; MCM and TCM are multi layer ceramic modules.

From RYMASZEWSKI, E. J. *et al.*, *IBM J. Res. Dev.* **25** (1981) 606. Copyright 1981 by IBM Corporation; reprinted with permission.

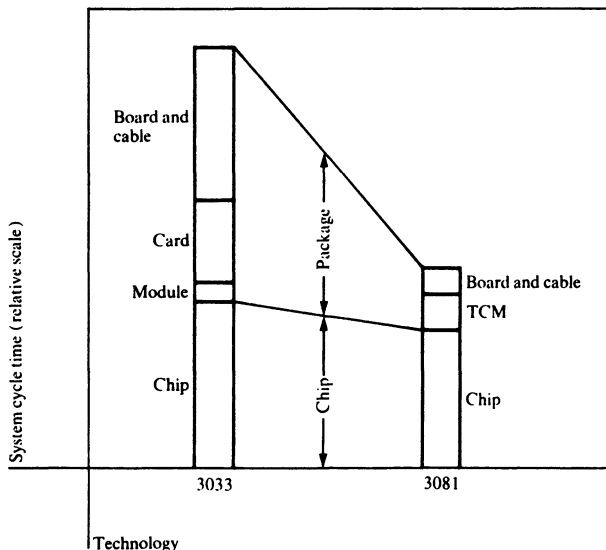


Fig. 2. — Comparison of system delay distribution of 3033 and 3081 technologies.

BLODGETT, A. J., *IBM J. Res. Dev.* **26** (1982) 30. Copyright 1982 by IBM Corporation; reprinted with permission.

Scaling down is possible because of the introduction of new technologies : low pressure or plasma enhanced chemical vapour deposition, ion implantation, metallic silicides technologies, exposure of resists by electrons, directionnal plasma etch. These technologies lead to a better design of devices, for instance smaller isolation areas for bipolar circuits.

Scaling down leads to drastic changes in the types of encountered defects : bulk defects have a smaller impact, but devices are very sensitive to the surface defects, to traces of contaminations, to electrostatic defects and to charges generated by α particles.

Scaling down increases the importance of edges. Computer simulation of the various steps of the process involves using two or three dimensionnal programs, instead of one dimension.

1.2.2 Designing new types of circuits. — New types of circuits were developed to increase the speed, to reduce the delay and the power, to allow more complex circuits by the multiplicity of connections. A better control of photolithography process was the condition to introduce C MOS and MTL families of circuits, because they are based on the injection of carriers by a lateral PNP transistor. The C MOS technology needs very specific wafers, for instance highly boron doped (2×10^{19} at/cm³) and covered by a 10 μ m thick epitaxy with a low doping (10^{15} at/cm³). Stresses generated in this type of substrate will be investigated in § 3.4.3.

Polysilicon and sidewall technologies for bipolar transistors allowed to manufacture a dual base (NEC 1979) : one very thin, weakly doped base in the active part of the transistor, and one highly doped base which provides the holes. Such bipolar transistors operate at very high speed, consume little power and have a high gain due to a small base resistance.

1.3 USING NEW MATERIALS.

1.3.1 Silicon on insulator. — Circuits implanted in a silicon layer grown epitaxially on an insulating substrate (sapphire in nearly all cases) display many advantages : high speed (reduction of substrate capacitances), higher density (no isolations), and better electrical behaviour (less carriers injected in SiO₂; « latch up » free; better control of the threshold voltage; better resistance to radiations).

75 mm diameter wafers of sapphire are presently being used; but the quality of the epitaxy is poor : dislocations and grain boundaries are present. This limits applications to circuits employing only majority carrier devices (custom logics, C MOS static RAM and ROM).

In spite of their advantages, these circuits are produced only for military applications.

1.3.2 III-V compounds. — The lattice of III-V compounds is made up by assembling one atom of the third column of Mendeleiev's table with one of the fifth column. The most commonly used are GaAs

and InP. Their main characteristics are :

- A band gap larger than that of silicon (GaAs : 1.42 eV; InP : 1.28 eV). No isolation is needed; circuits can work at higher temperature (300 °C for GaAs).

- The possibility to vary the gap by substituting one type of atom : Al instead of Ga (GaAlAs); Ga instead of In (GaInP or GaInAs). This allows multi-layer structures.

- A direct band to band transition : this material is convenient for optoelectronic.

- The possibility of achieving a reproducible doping.

- Large carrier mobilities (GaAs : 8 600 cm²/s; InP : 4 600 cm²/s at 300 K).

- The possibility of very fast transport in bidimensionnal layers at the GaAs-GaAlAs interface.

- The possibility of nearly ballistic electron injection for small devices.

- A negative differential mobility for high electric fields (GUNN diodes).

GaAs devices are able to dominate two markets :

- Very fast devices : GaAs-GaAlAs heterostructures in bipolar devices allow a 0.05 ns delay; in MESFET devices, the delay is 0.1 ns for a 1 mW dissipation. In TEGFET devices, a bidimensionnal layer of electrons is confined at the GaAs-GaAlAs interface. In the device proposed by Thomson-CSF in 1982, a delay of 20 ps was achieved with a 1 mW dissipation.

- Optoelectronics : III-V compounds make good photodiodes. Laser effect is efficient in heterostructures. The integration of a photodiode and of a transistor gives rise to a new device, the phototransistor; integrated with a laser, all the functions for optical communications become available : reception of the light, transformation in an electric signal, computation in the device and emission of an optical signal.

But the technology of III-V compounds needs large improvements :

- Substrate quality : the largest wafers used in manufacturing have a diameter of 100 mm and a density of dislocations 10⁴/cm². The addition of indium during pulling reduces this density to less than 10²/cm² for an In concentration of 10¹⁹ at/cm³.

- Passivation : the native oxide is poor and only deposited insulating layers are used. The density of surface states is high.

- The adjustment of the threshold voltage is difficult and imprecise.

- The technologies for epitaxy (Molecular Beam Epitaxy and Metal-Organic Chemical Vapour Deposition) have to be improved.

- The outdiffusion of arsenic at high temperature is also a concern.

Until now, the industrial production of very dense integrated circuits (VLSI) is not defect free. But

obviously these families of circuits will have a wide application in the future, especially in the field of telecommunications, for microwave devices.

1.3.3 Josephson circuits. — A Josephson junction consists of two supraconductive layers separated by a very thin (2 nm) insulating layer. Josephson devices display three characteristics : fast switching (10 to 20 ps), low power dissipation (1 μW per circuit) and operation at a very low temperature (4 K). But the manufacturing technology is very difficult; the reliability of the circuits is poor due to the difference of thermal expansion between various materials; the delays of commutation vary widely on the same chip. The Josephson device remains until now a laboratory product.

1.3.4 Magnetic bubbles. — Magnetic bubbles are magnetic domains, some μm wide, which can be magnetized only in one direction by a signal driven by a magnetic metal, for instance permalloy (Fe + Ni). Since the access time is about 1 ms, they are used in mass memories, between the disks and the central memory of the computer. The main qualities are : non volatility, less errors than in MOS memories (10⁻¹² compared to 10⁻¹⁰ in 1983).

But the drastic reduction in the price of MOS devices and the better performances of memory disks has reduced the interest of this technology.

1.3.5 Conclusion. — The I.C. industry will continue to use silicon substrates in the next years for nearly all the productions. Other substrates will have only very specific markets : military, due to the resistance to the radiations for silicon on insulator substrates; non volatil mass memories for the magnetic bubbles; high frequency and optoelectronic application for the III-V compounds.

2. The pulling of silicon crystals.

The main requirements for wafers are :

- A large diameter to achieve high productivity. The evolution of the size of silicon and gallium arsenide single crystals is shown in figure 3.

- No crystalline defects in the part of the wafer where circuits are implanted : a dislocation free monocrystal is necessary.

- Gradients and fluctuations of dopant concentration as small as possible.

- A good resistance to plastic deformation.

- A low sensitivity to contamination, i.e. the ability to getter defects out of the circuits zone : backside gettering, or intrinsic gettering by defects in the bulk, when a defect free zone (DFZ) underneath the active surface is possible.

2.1 THE SEQUENCE OF OPERATIONS. — Very pure silica is reduced by carbon in an arc furnace to obtain metallurgical grade polysilicon. This material is converted into chlorinated compounds (SiHCl₃, or SiCl₄, or SiH₂Cl₂) by a reaction with HCl at 300 °C;

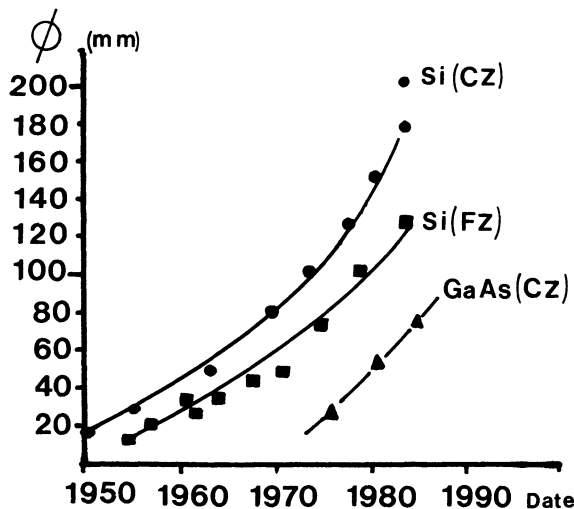


Fig. 3. — Diameter of the largest crystals used by the industry of integrated circuits function of the date.

pure polycrystalline silicon rods (less than 1 ppmA of impurities) are then obtained by reduction of these gazes by hydrogen.

This rod is melted and a cylindrical monocrystal is pulled. Two main pulling techniques are used : Czochralski (CZ) (bibliography in Rosenberger [3] and Zulehner [4]), and Float Zone (FZ) (bibliography in Dietze [5]).

Wafers are obtained from the monocrystal by a series of mechanical operations : grinding, sawing, lapping, chamfering, polishing, cleaning.

Thermal treatments, or gettering operations performed at the back of the wafer (grinding, ion implantation, deposition of polysilicon or silicon nitride layers, doping) can be added. Their goal is to improve the quality of the wafers before the manufacturing process which will lead to the production of integrated circuits, starts.

2.2 THE PULLING OF MONOCRYSTALS. — Monocrystals are obtained by letting a pure silicon melt solidify on a monocrystalline oriented seed.

2.2.1 The Czochralski process (CZ). — Polycrystalline silicon material is first melted in a crucible heated by a resistor or by RF currents. Following the process designed by Dash [6], a seed is dipped into the melt, and begins to melt. The power is then reduced and the seed is slowly withdrawn ; the crystal and the crucible rotate in opposite directions. By controlling power and acting on the speed of the seed, the crystal diameter is adjusted. This process is illustrated in figure 4.

Chemical reactions between melted silicon and the crucible play a very important part : using a silica crucible, a large amount of oxygen is incorporated in the melt and part of it (10^{18} at/cm³) gets into the monocrystal. Other types of crucible may be used if a reduction in oxygen concentration is wanted, e.g. graphite, SiC, nitride (Si₃N₄)...

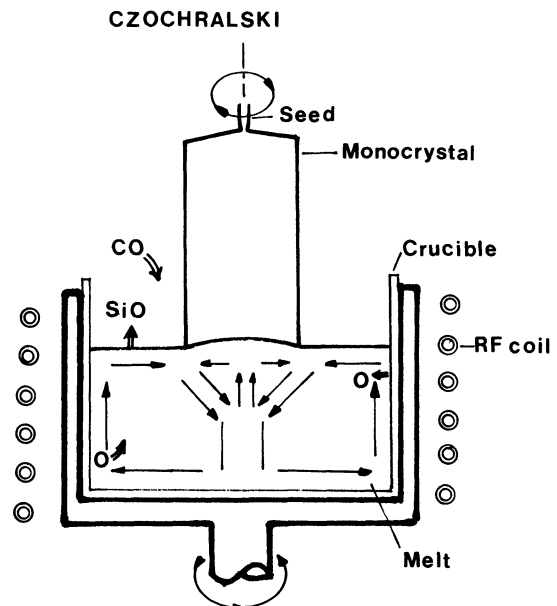


Fig. 4. — Czochralski single crystal pulling. Arrows indicate the flows in the liquid when the crystal and the crucible are counterrotated. Note the incorporation of oxygen in the melt and the presence of SiO and CO in the atmosphere.

Gradients and fluctuations of dopant and defect concentrations are explained by the convections in the melt (Fig. 4), due to thermal gradients (from the edge to the centre) and to the rotations (from the centre to the edge, under the crystal).

2.2.2 The float zone process (FZ). — A polysilicon rod in vertical position is melted at its lower end. A seed is introduced in the melt and the float zone slowly passes through the rod from the bottom to the top. The seed and the rod are rotated in opposite directions (Fig. 5). In this technology, there is no contact with a crucible and the only possible contamination comes from gazes (outgazing of the equipment).

The « Pedestal » technology is identical except that the seed is introduced at the upper end of the rod.

2.3 CRYSTAL DOPING. — The growing crystal incorporates impurities of the melt ; but the impurity concentration in the solid C_s differs from the concentration C_l in the liquid, just at the interface. The ratio $k = C_s/C_l$ is called the segregation coefficient, it is characteristic of the impurity and of the melt. Table I gives the value of k , of the diffusion coefficient D and of the covalent radius r_c for several elements in a silicon melt (see Trumbore [7] and Zulehner [4]). Figure 6 gives the limit of solubility of impurities in lightly doped solid silicon. k is smaller than 1 for all the elements except oxygen. For metals, k is about 10^{-5} , which means that a drastic purification of silicon results from crystal pulling.

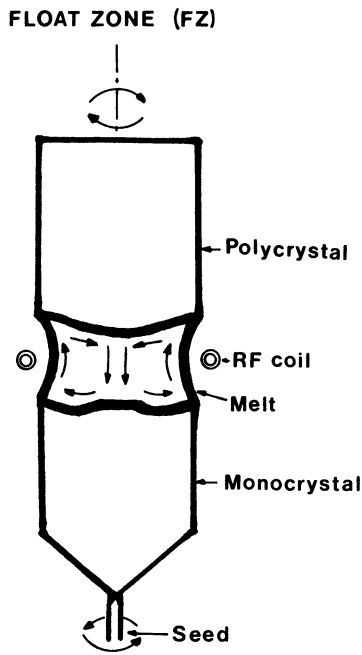


Fig. 5. — Float zone single crystal pulling. Arrows indicate the flows in the liquid. For large crystals, the diameter of the coil can be smaller than the diameter of the crystal.

Dopant	<i>k</i>	<i>D</i> (10 ⁻⁴ cm ² /s)	<i>r_c</i> (Å)	Metals <i>k</i> (10 ⁻⁶)
B	0.8	2.4	0.88	Li 10 ⁴
Al	0.002	7	1.26	Ti 9
Ga	0.008	4.8	1.26	V 10
In	0.0004	6.9	1.44	Ta 0.1
Th	0.00017	7.8	1.47	Cr 28
C	0.07	2	0.77	Mo 0.05
Ge	0.33		1.22	Mn 10
Sn	0.016		1.40	Fe 8
				Co 8
N	0.0007		0.70	Ni 30
P	0.35	2,3	1.10	Cu 400
As	0.3	3.3	1.18	Ag 1
Sb	0.023	1.5	1.36	Au 25
Bi	0.0007		1.46	Zn 10
				Cd 1
O	1.3	3.3	0.66	
S	10 ⁻⁵	2.4	1.04	

k : segregation coefficient; *D* : coefficient of diffusion in liquid silicon;
r_c : covalent radius.

Figure 7 represents a typical concentration profile of an impurity near the interface, along the axis of rotation; for *k* < 1, freezing rejects the impurity in the melt.

At steady state, Fick's law gives :

$$D \frac{\partial^2 C}{\partial z^2} + V \frac{\partial C}{\partial z} = 0$$

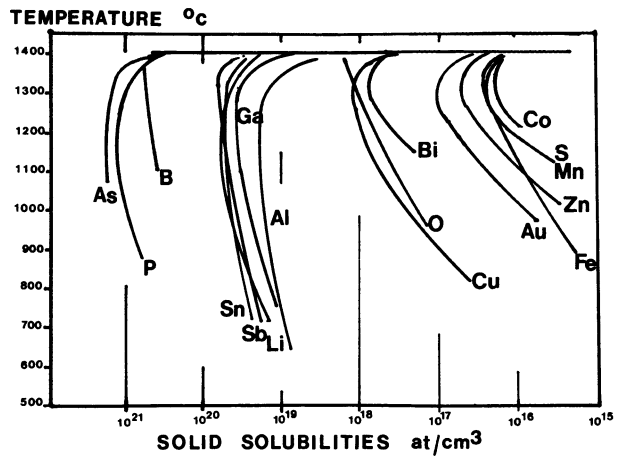


Fig. 6. — The limit of solubility of impurities in solid lightly-doped silicon is plotted as a function of the temperature. From Trumbore [7].

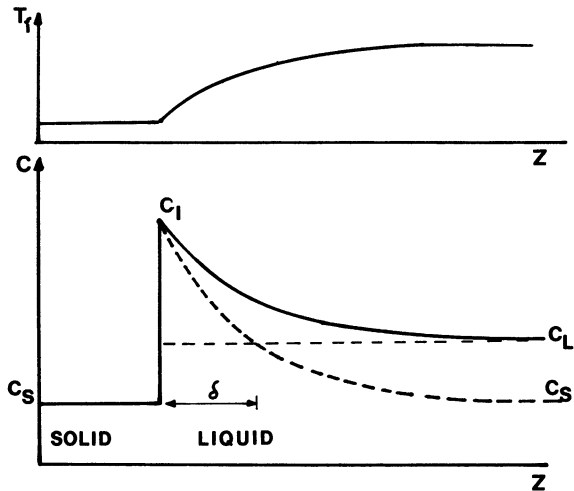


Fig. 7. — The axial distribution of the concentration *C* of an impurity near the crystal-melt interface is plotted. The corresponding profile of the freezing temperature *T_f* is presented. The definition of δ is illustrated by the intersection of the horizontal $C = C_L$ with the dotted line

$$C - C_s = (C_1 - C_s) \exp - \frac{Vz}{D}$$

and the conservation of matter at the interface yields :

$$(C_1 - C_s) V + D \left(\frac{dC}{dz} \right)_{z=0} = 0$$

If the diffusion in the solid is neglected, *C* is the concentration in the melt, *D* the coefficient of diffusion in the melt, *V* the rate of freezing, *C_s*, *C₁*, *C_L* the concentrations in the solid, in the liquid at the interface and far from the interface respectively.

The solution is :

$$\frac{C - C_s}{C_1 - C_s} = \exp - \left(\frac{Vz}{D} \right)$$

The thickness δ of the interface layer is defined by :

$$\frac{C_L - C_s}{C_L - C_s} = \exp - \left(\frac{V\delta}{D} \right)$$

$$\frac{C - C_s}{C_L - C_s} = \exp \frac{V}{D} (\delta - z)$$

δ varies with the conditions of convection in the melt.

Ratio $k_e = C_s/C_L$ is called the effective segregation coefficient

$$k_e = \frac{k}{k + (1 - k) \exp \left(- \frac{V\delta}{D} \right)}$$

Fluctuations of the concentration of impurities are observed when $V\delta$ varies rapidly.

Impurities rejected in the melt increase slowly C_L , and then C_s , as pulling proceeds. Figure 8 gives the value of k_e versus $V\delta/D$, and the ratio of C_s/C_0 (C_0 , the initial concentration in the melt) versus the fraction of the melt solidified, g , for various k_e ($C_s/C_0 = k_e$ for $g = 0$).

$$C_s/C_0 = k_e(1 - g)^{k_e - 1}$$

when there is no exchange of impurity with the atmosphere.

2.3.1 Reduction of the axial concentration gradients. —

It is obvious that the axial concentration gradient is reduced when k_e increases, for instance when pulling occurs at higher pulling rates from a melt possessing a larger C_0 . The resistivity of the crystal decreases from the seed end to the tail end, as the concentration of dopant increases.

To achieve a constant C_s along the crystal axis, one can use a small melt continuously fed by liquid silicon doped at C_s . The concentration in the melt is maintained at the value C_s/k_e when the volume of the melt is kept constant. Various geometries have been proposed : double crucible, fusion of a polycrystal during the pulling. See for instance Rosenberger [3].

2.3.2 Supercooling. — The freezing temperature T_f varies with the concentration of dopant C (in at/cm³) as shown in figure 7. For silicon :

$$T_f(C) - T_f(C_L) = 0.93 \times 10^{-20} (C - C_L)(k - 1) \text{ (}^\circ\text{C)}.$$

When the temperature gradient $\partial T/\partial z$ is large enough in the melt, freezing occurs only at the interface, layer after layer. But if $\partial T/\partial z$ is too small (this can only be the case for high doping of the melt, above 10^{19} at/cm³), the temperature is smaller than T_f in a thin layer of the melt, giving rise to supercooling. In some cases massive freezing occurs, and the pulled solid becomes polycrystalline.

2.4. HEAT AND MELT FLOWS IN CZOCHRALSKI CRYSTAL PULLING.

2.4.1 Heat flows. — Figure 9 represents the heat flows and the corresponding curves of constant temperature in the CZ process.

— *The interface* between the crystal and the melt remains at a constant temperature, T_f .

— *In the melt*, heat is generated by the RF currents, and the crystal behaves as a sink for heat. The temperature gradients ∇T induce convective flows, ascending near the crucible and descending under the

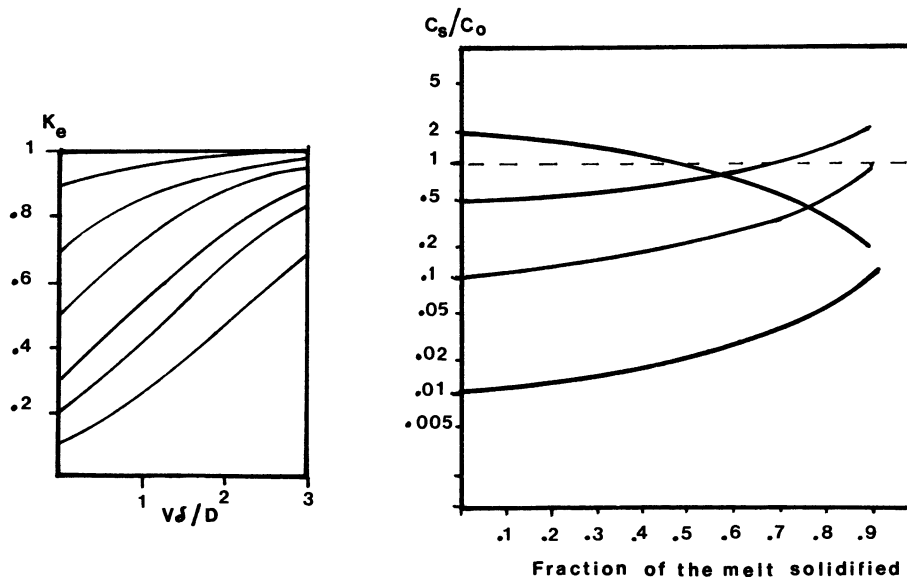


Fig. 8. — Left : effective segregation coefficient k_e of an impurity function of $V\delta/D$ (V freezing rate, δ diffusion layer thickness, D diffusion coefficient of the impurity in the melt). Right : C_s/C_0 function of the fraction of the melt solidified g , for various k_e ; C_s is the concentration in the crystal, C_0 the initial concentration in the melt; no exchange with the atmosphere is supposed, k_e is the value of C_s/C_0 for $g = 0$.

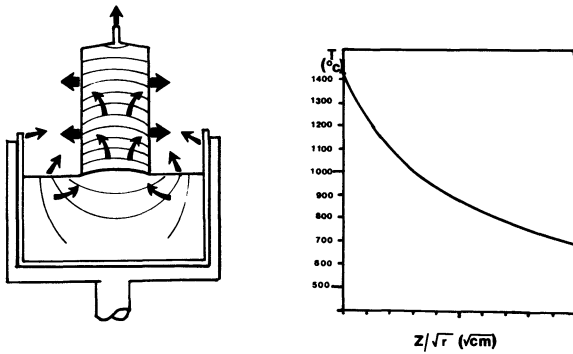


Fig. 9. — Left : heat flows during CZ pulling and shape of the isotherms. Right : axial distribution of the temperature in the crystal (r : radius of the crystal; z axial distance from the melt).

crystal; these flows are characterized by the number of Grashof, N_{Gr} , which is the ratio of forces due to the change in density to the forces of viscosity. For silicon :

$$N_{Gr} = 15\,600 R^4 \nabla T \quad (R \text{ in cm, } \nabla T \text{ in } ^\circ\text{C/cm})$$

R is the radius of the crucible.

In the melt, heat is also dissipated by irradiation or convection at the interface between the melt and the atmosphere.

— *The crystal gets heat from many sources* : the melt; the latent heat of freezing of silicon; radiative heat from the liquid surface, from the emerged part of the crucible and the walls of the equipment. It dissipates heat by irradiation and convection along its cylindrical lateral surface and through the head, and by conduction through the seed. See Rosenberger [3], Rea [8], Ramachandran [9].

The interface is convex when the heat sink is very efficient (pulling of the head, or high contribution of the convection of the gaz), and concave in the other case. Convex or concave refer to the shape of the solid side.

Figure 9 represents a typical axial distribution of temperatures. When the radius is constant, the pulling rate and the RF power are adjusted, but the distribution of temperature is not a function of this adjustment : the temperature is inversely proportionnal to the square root of the radius and independent of the pulling rate.

Thermal history of the wafers. — Depending on where inside the crystal the wafers come, their thermal history varies greatly : seed end wafers have been rapidly cooled through the head of the crystal ; middle end wafers have been slowly cooled, and tail end wafers have been first slowly cooled at high temperature and then fast cooled at the end of the pulling process. Typical values of this kinetic are given in figure 10, for 85 mm diameter crystal, from Leroy [10]. The time coordinate is the ratio of the distance by the pulling rate.

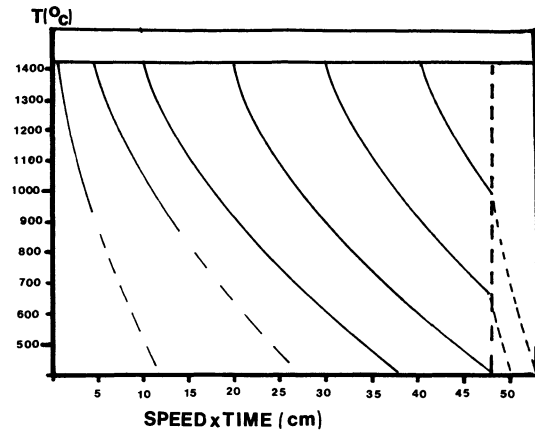


Fig. 10. — Kinetics of cooling of a silicon layer. Its distance to the seed is the distance at 1 415 °C. The time spent between two temperatures is measured on the horizontal scale, multiplied by the pulling rate.

2.4.2 Melt flows.

Forced convection. — A liquid, near a rotating disk, moves about through friction, creating a centrifugal flow in a δ_0 -thick layer fed by a vertical flow. For an infinite disk, Cochran [11] showed that δ_0 does not depend on the distance to the axis and

$$\delta_0 = 4\sqrt{\nu/\omega}$$

where $\nu = 3 \times 10^{-3} \text{ cm}^2/\text{s}$ is the kinematic viscosity of the melt and ω (rad/s) the angular velocity of the disk. For $\omega = 2 \text{ rad/s}$ (20 rpm), $\delta_0 = 1.4 \text{ mm}$.

For a finite disk of radius r , this convection is characterized by the number of Reynolds N_{Re} , which is the ratio of the inertial force to the viscous force.

$$N_{Re} = \omega r^2/\nu. \quad \text{Then} \quad N_{Re} = 16 r^2/\delta_0^2.$$

Proudman [12] and Taylor [13], proved that the steady state of a liquid rotated in a crucible was bidimensional, i.e. without vertical component. The case in which a crystal is put in contact with the liquid and rotated around the same axis, but with a different velocity, is illustrated in figure 11. Proudman and Taylor showed that the melt was divided in large cylindrical cells, where the liquid rotates with a constant angular velocity, separated by small layers where the angular velocity varies. Carruthers [14] made an extensive study of the various configurations corresponding to the various rotation rate of the crystal and of the crucible. Each cell displays a radial and an axial velocity, consistent with the study of Cochran, illustrated in figure 11. An illustration of these nonmixing cells is also presented.

When a fast change in the crucible speed is imposed, the angular velocity in the cells does not remain constant, and an helicoidal flow, with shear components, results : it is the Ekman flow. The cells change their shape, and there is some mixing of the melt.

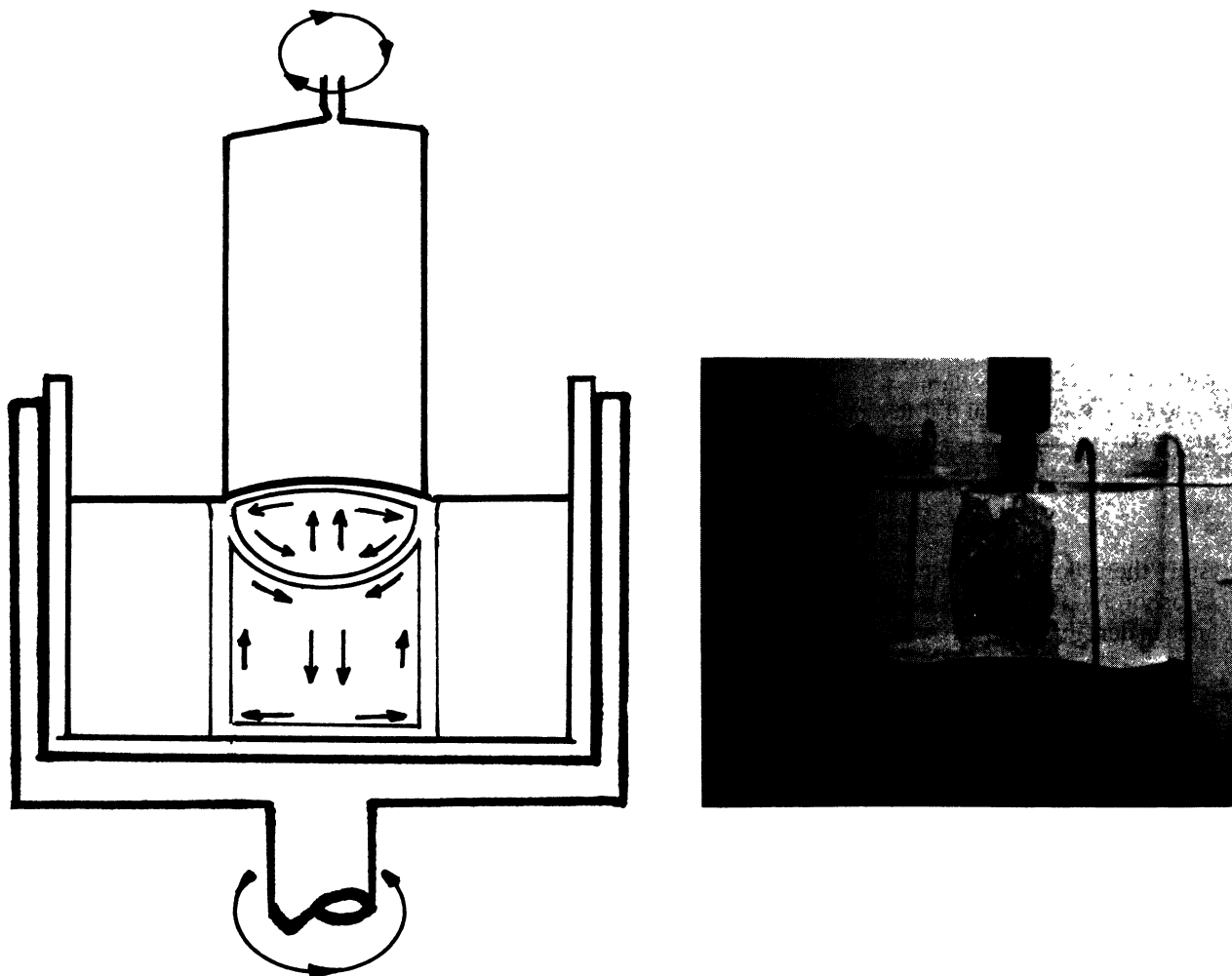


Fig. 11. — Forced convection in the melt : left ; Proudman-Taylor cells, shear layers, and convection currents when the crystal and the crucible are rotated in the opposite directions. Right : illustration of one cell : crystal : rotation + 22 rpm ; crucible : - 22 rpm ; liquid : glycerine/water ; room temperature. Westdorp, private communication.

Dominant convection. — Murgai [15] pulled crystals from melts highly doped with antimony (1.22×10^{20} at/cm³), with its crucible off-centred to have a strong lateral gradient of temperature. At the beginning of the pulling, a very regular pattern of dopant concentration fluctuations was observed, due to a forced convection dominant flow. When part of the melt was frozen, thermal convection dominated, inducing a very irregular microsegregation. The correlation between the dopant concentration and the microscopic growth rate revealed a periodic remelt of the crystal during the thermal convection.

Carruthers [16] and Kobayashi [17] characterized the dominant flow by ratio N_{Gr}/N_{Re}^2 . This ratio increases with the crystal diameter.

When this number is very small, less than 10^{-3} , forced convection dominates in the whole melt. When it is very large (more than 10^2), thermal convection dominates. Between these two values, forced

convection predominates near the crystal and thermal convection near the crucible, as shown in figure 4.

Typical values :

$$R = 10 \text{ cm}, \quad r = 5 \text{ cm}, \quad \Delta T = 50 \text{ }^\circ\text{C}, \quad \omega = 1 \text{ rad/s}$$

$$N_{Gr} = 7.8 \times 10^8; \quad N_{Re} = 0.83 \times 10^4;$$

$$N_{Gr}/N_{Re}^2 = 11.3.$$

Interface layer. — Just under the freezing interface, one can define three layers with three characteristic thicknesses (see Rosenberger, (1979)).

- 1) A δ thick layer where the impurity concentration varies.
- 2) A δ_0 thick layer where the radial velocity of the liquid change.
- 3) A δ_T thick layer, where the temperature gradient is large.

During the CZ pulling of silicon crystals, we can

write :

$$\delta_0 = 4\sqrt{v/\omega}; \quad \delta = \delta_0 0.4(v/D)^{-1/3} = 1.6 D^{1/3} v^{1/6} \omega^{-1/2}$$

$$\delta_T = \delta_0(v/\lambda)^{-1/3} \simeq 2 \delta_0.$$

λ is the thermal conductivity of the melt, and $v/\lambda = 0.06$ for Si. For the majority of dopants, $5 < v/D < 30$ so that $\delta \simeq \delta_0$.

Radial gradients of concentration. — The radial distribution of the concentration of impurities exhibits a maximum on the axis of rotation and a minimum at the lateral surface. This difference is larger for phosphorus than for boron, and for an (111) oriented substrate than for a (100) one. It is reduced by an increase of the rotation rate, which accelerates the circulation of the melt (larger speed, smaller interface layer, more importance to the forced convective flows).

Out diffusion of antimony from the bath can reduce its concentration close to the lateral surface of the crystal. Oxygen can outdiffuse from the crystal during cooling, creating an oxygen poor layer (typically 1 mm thick).

A control of the resistivity gradients is a key parameter in the quality of wafers for integrated circuits technology.

2.4.3 Striations. — Many properties of the crystal exhibit fluctuations on a microscopic scale : concentration of dopants, oxygen, carbon; density of small defects, revealed by chemical etching or decoration with copper; nuclei for oxygen precipitation; type of

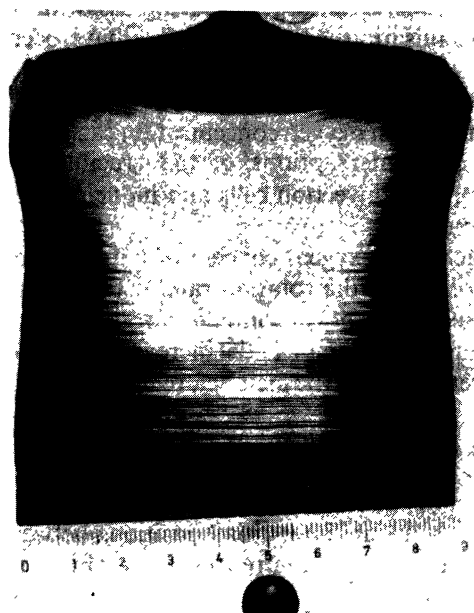


Fig. 12. — Longitudinal cross section of a 85 mm diameter CZ crystal showing striations (periodicity 400 μm). Defects have been decorated by copper diffusion and revealed by Jenkins-Wright etch.

oxide precipitates after a high temperature thermal treatment (see § 3) (Fig. 12).

A regular striation appears when the distribution of temperature in the melt has not radial symmetry, i.e. when there is a small lateral gradient : the interface layer thickness δ , the rate of freezing V and the effective coefficient of segregation k_e vary during one rotation of the crystal relative to the melt. If \bar{v} is the average pulling rate, ω_C and ω_M the rotation rate of the crystal and of the crucible, the thickness of silicon layer frozen during such a rotation is $\Delta z = \bar{v}/(\omega_C - \omega_M)$ which is the axial periodicity of the striation. But the real shape of the maximum of concentration is an helicoidal surface.

Figure 13 represents a typical example of axial fluctuations of boron and oxygen concentrations irregular fluctuations superpose to regular striations. They are due to thermal fluctuations (order of magnitude : less than 1 °C).

Pulling under a magnetic field (5 000 Gauss) is used to reduce the se fluctuations by blocking the convective flows. See Feigl [18].

Neutron transmutation doping was also used to superpose an homogeneous doping to the intrinsic doping for phosphorus doped wafers.

3. Oxygen and carbon in silicon crystals.

Oxygen is the most important contaminant in CZ crystals. Its concentration is sometimes larger than 30 ppmA. The concentration of carbon is generally around 1 ppmA, but can reach 8 ppmA in tail end wafers.

In FZ crystals, pulled under vacuum, the contamination by oxygen is drastically reduced, between 0.1 and 0.01 ppmA, but the concentration of carbon remains between 0,1 to 5 ppmA.

3.1 INTRODUCTION OF OXYGEN AND CARBON DURING CZ PULLING. — The melt and the silica crucible react, which yields oxygen :

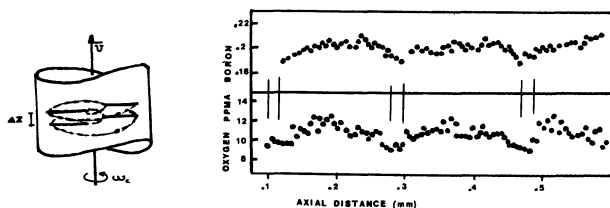
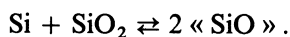
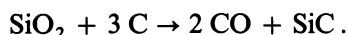


Fig. 13. — Left : perspective showing the helicoidal shape of the striations Right : oxygen and boron axial concentration : a remelt occurs every 200 μm, with a minimum in concentrations. The maximum occurs just before the remelt for boron, just after for oxygen. From Murgai (private communication).

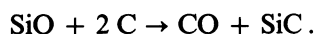
The chemical nature of « SiO » in the melt is not known, but the limit of solubility of oxygen in the melt at the freezing temperature is 25 ppmA, and in solid silicon, 35 ppmA. The dissolution rate of the crucible is about 10 $\mu\text{m}/\text{h}$. It increases when the temperature increases, when the pressure decreases; the roughness of the crucible, the impurities in the crucible and in the melt, and the melt flows near the crucible are key parameters. See Zulehner [4].

During the thermal convection, part of the « SiO » evaporates, as the SiO equilibrium vapour pressure is 12 mbar at 1 420 °C. Two chemical reactions generate carbon monoxide, from those parts of the equipment made of graphite :

Reaction between crucible and graphite susceptor :



Reactions in the gaz



CO dissolves in the melt, especially during the melting of polycrystalline silicon or a remelt of a crystal, and the exchanges of CO between the melt and the atmosphere are very small during pulling (Compain, [9]).

Oxygen and carbon dissolved in the melt diffuse from the thermal convection cell to the forced convection cell (Fig. 4) and reach the freezing interface.

3.1.1 Axial concentration. — The concentration of oxygen in the melt is due to two competitive processes : incorporation is proportionnal to the surface of contact between the crucible and the melt, and is reduced when the level of the melt decreases. The evaporation occurs through a constant surface. The concentration of oxygen in the melt decreases during the pulling process, and in the crystal from the seed end to the tail end. This is not true at the very end of the pulling, when the forced convection cell reaches the crucible : oxygen is then directly incorporated under the crystal-melt interface, and the oxygen concentration increases (Fig. 14). See Murgai [15]; Carlberg [20].

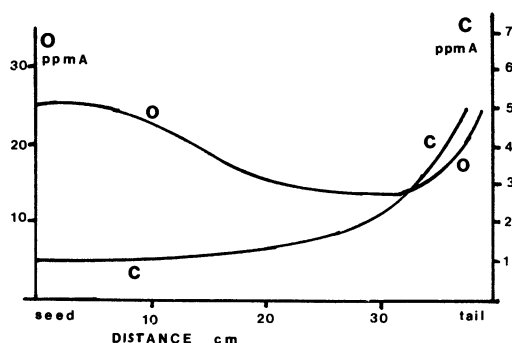


Fig. 14. — Typical axial distribution of oxygen and carbon in a CZ crystal. Two types of wafers have the same concentration of oxygen : seed end, with a low carbon concentration, and tail end with a large amount of carbon.

The axial concentration of carbon increases from the seed end to the tail end : the segregation coefficient of carbon in silicon is 0.07 (Nozaki [21], Compain [19]), and the exchanges of carbon between the melt and the atmosphere are very small during the solidification (Fig. 14).

3.1.2 Radial concentration. — The concentration of oxygen is larger in the centre of the crystal, where it is provided by the forced convection flows, than near the lateral surface. This gradient is reduced by increasing the crystal rotation rate.

3.1.3 Fluctuations. — Thermal fluctuations induce fluctuations of the freezing rate (§ 2.4.3), and of the concentrations of dopants, oxygen and carbon (Fig. 13), the maximum for the oxygen ($k = 1.3$) being the minimum for carbon and dopants ($k < 1$) (Hu, [22]). Similar fluctuations are observed for clusters of point defects called Swirls because of their helicoidal pattern (§ 2.4.3), (de Kock, [23, 24]).

In further thermal treatments, oxygen will precipitate in helicoidal patterns, which appear as eccentric rings in X rays topographs when the wafers are cut aslant (Fig. 15).

A large bibliography is available; see Murgai [15], Abe, [25, 26]; Leroy [27].

3.1.4 How to reduce oxygen and carbon concentrations. — A reduction of the oxygen level is achieved by pulling under a magnetic field, thus reducing the convective flows (see Feigl [18]), or by using materials without oxygen for the crucible : vitreous carbon, SiC, Si_3N_4 . But the dissolution of these materials provide high concentrations of carbon or nitrogen at the melt-solid interface. The risk of precipitation of SiC or Si_3N_4 is large, inducing dislocations and polycrystallisation. Alumine crucible have been used, but they induce a high aluminium contamination (more than 10^{17} at/cm³).

An increase in oxygen concentration can be achieved by periodic interruptions of the crucible rotation, breaking the convection cells and inducing a mixture of the melt.

To achieve oxygen concentration constant, one needs to change the rotation rate or the pulling rate.

The reduction of carbon concentration is achieved by pulling under vacuum; the increase is obtained by a long overheating of the melt before pulling.

3.2 MEASUREMENT AND PROPERTIES.

3.2.1 Infrared absorption. — In silicon, oxygen atoms are mainly in an interstitial position, between two silicon atoms (bond centred position) (Fig. 16). This configuration allows three main modes of vibration, and one can observe three characteristic absorptions of infrared light, at $1\,206\text{ cm}^{-1}$, $1\,106\text{ cm}^{-1}$ and 517 cm^{-1} at room temperature. At low temperature (23 °K, 6 °K), the $1\,106\text{ cm}^{-1}$ absorption shifts and divides in six rays centred at $1\,130\text{ cm}^{-1}$, due to isotopic effects of

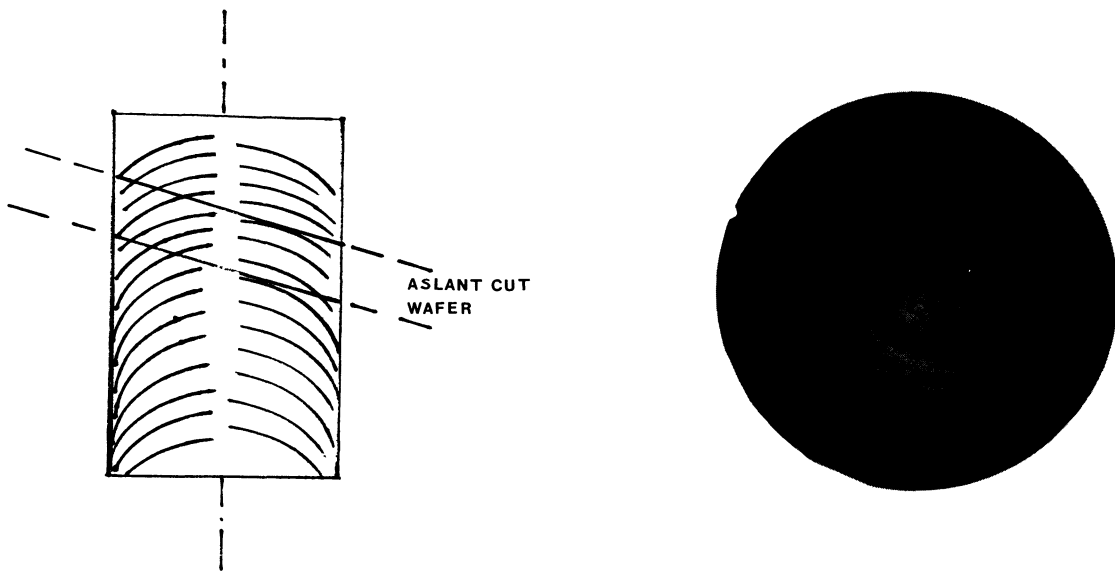


Fig. 15. — Rings of oxygen precipitates in a wafer cut aslant and annealed 20 hours at 1 000 °C : rings are eccentred in the wafer, as they are a memory of the radial symmetry of the crystal.

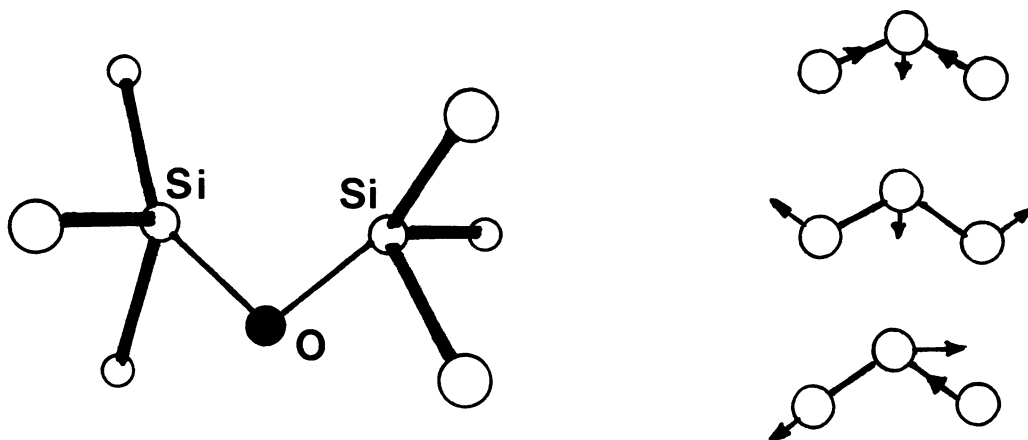


Fig. 16. — Left : position of interstitial oxygen between two silicon atoms; Right : modes of vibrations of this « quasi molecule », and wave numbers associated.

oxygen (^{16}O and ^{18}O) and of silicon (^{28}Si , ^{29}Si , ^{30}Si) (Pajot [28]).

The determination of interstitial oxygen content $[O]$ by measuring one infrared absorption α requires a calibration.

- Absorption at $1\,203\text{ cm}^{-1}$ yields a small signal and it not used.

- Absorption at 517 cm^{-1} was used by Compain [19], but only in differential measurements (compared to a standard) because of the high absorption of silicon at this wavelength.

- Absorption at $1\,106\text{ cm}^{-1}$ at room temperature is used. It gives only the concentration of interstitial oxygen. But an absorption of oxygen precipitates at $1\,080\text{ cm}^{-1}$ imposes corrections after thermal treat-

ments between 600 °C and 900 °C . Calibrations by various methods were discussed by Pajot [29]. The actual ASTM standard is : $[O]/\alpha = 4.9\text{ ppm}\cdot\text{A}\cdot\text{cm}$ but an old one, $[O]/\alpha = 9.63\text{ ppm}\cdot\text{A}\cdot\text{cm}$ was (and is still) used in the literature. This calibration coefficient has to be precised to compare various publications.

Various complexes of oxygen with carbon or point defects were identified after irradiation and their infrared absorbances determined. See Corbett [30], BreLOT [31], Compain [19].

The concentration of substitutional carbon is measured from the change in infrared absorption at 604 cm^{-1} at room temperature, with the calibration of Newman [32] :

$$[C]/\alpha = 2.2\text{ ppm}\cdot\text{A}\cdot\text{cm} .$$

3.2.2 Diffusion data. — The best fitting of all the data relative to interstitial oxygen diffusion between 350 °C and 1 300 °C is obtain with the formula of Watkins [33]

$$D_0 = 0.23 \exp(-2.561 \text{ eV}/kT) \text{ (cm}^2/\text{s)}.$$

However, to explain the kinetics of donor formation, Ourmazd [34] introduced an increase of the low temperature effective diffusivity of oxygen with the concentration of silicon self interstitials.

The enthalpy of capture of oxygen in highly dislocated areas is 0.95 eV (Hrostowski, [35], Magee, [36]).

The diffusion coefficient of substitutional carbon in silicon measured by Newman [37] is :

$$D_C = 0.33 \exp(-2.92 \text{ eV}/kT) \text{ (cm}^2/\text{s)}.$$

3.2.3 Limit of solubility. — Figure 17 represent the behaviour of oxygen during thermal treatments (left) and the equilibrium SiO_2 phases with respect to pressure and temperature. Values of the solubility limit in solid silicon found by various authors vary widely within a factor 10, see Leroy [27], partly because the nature of the SiO_2 phase in equilibrium with silicon is involved ; it can be cristalline or amorphous, oxide layer or precipitates ; the role of point defects is also important, so that measured values are sometimes non equilibrium values. Stresses play an important role in oxygen precipitation (see § 3. 3). In figure 17, values are reported for $[\text{O}]/\alpha = 5.6 \text{ ppmA} \cdot \text{cm}$. This gives a good idea of the quantity of interstitial oxygen in equilibrium with an oxide layer. Even during an oxidation at high temperature (1 000 °C), oxygen can outdiffuse from the wafers if its concentration is larger than the limit of solubility.

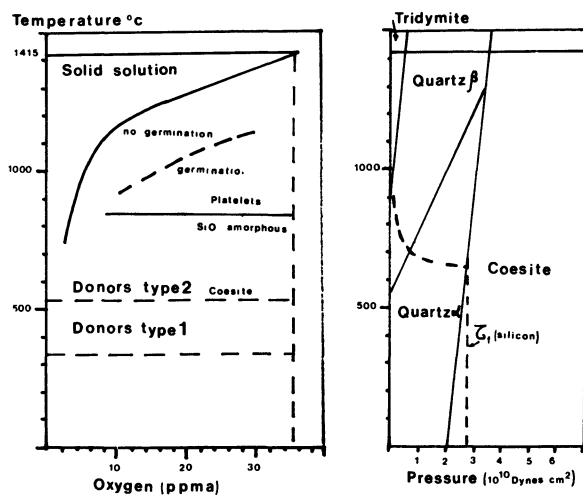


Fig. 17. — Left : behaviour of oxygen during isothermal annealings, from Cazcarra (41); Right : equilibrium SiO_2 phase function of the temperature and the pressure, from Pascal (nouveau traité de chimie minérale). Dotted line : pressure inducing the critical shear stress τ_f in silicon (see Fig. 19). Coesite can exist only at a temperature smaller than 700 °C.

The limit of solubility of carbon in silicon is 8 ppmA at 1 400 °C, 2 ppmA at 1 250 °C, 5 ppmA at 1 100 °C (Bean, [38]). But SiC does not precipitate in CZ crystals because of the strong interaction between carbon and oxygen.

3.3 CLUSTERING AND PRECIPITATION DURING ANNEALINGS. — A large bibliography on oxygen and carbon clustering and precipitation in silicon during annealings is available ; see Patel [39, 40], Cazcarra [41, 42], Claeys [43, 44], Leroy [27], Bourret [45, 46].

3.3.1 Stresses. — The agglomeration of oxygen atoms requires that the matrix expand, 35 % in volume for coesite, 120 % for amorphous silica. Stresses around the precipitates give rise to lattice strains, to the generation of dislocations and of silicon interstitials.

At low temperature, strains dominate, and precipitates lie in (001) planes, easier to separate due to the anisotropy of the matrix. Coesite and amorphous silica are observed. (Bourret, [46]). Small clusters are characterized by donor states. Emission of silicon interstitials relax 80 % of the stresses (Ourmazd [34]), but is very slow.

At larger temperature (more than 700 °C), stresses can be relaxed by the emission of dislocations and amorphous silica platelets dominate. But more massive precipitates are observed, surrounded by an extrinsic stacking fault, which emits vacancies and captures interstitials.

At temperature above 1 150 °C, precipitates are « quasi spherical », with or without stacking faults and dislocations surrounding them : relaxation of stresses by emission of interstitials dominates.

Figure 17 (right) indicates the crystalline SiO_2 phase stable with respect to the temperature and the pressure. The pressure for which dislocations are generated is also represented, in dotted lines (Leroy [27]). Coesite exists only at temperatures below 700 °C, but for higher temperatures, the interface energy between silica and silicon must be taken into account, explaining the amorphous nature of silica films or precipitates.

3.3.2 Generation and annihilation of donor states. *First type of donors.* — A first type of oxygen related donor states was observed by Fuller [47] and Kaiser [48]. They possess the following characteristics :

- Generation occurs between 400 °C and 520 °C.
- The initial rate of donor formation, maximum at 450 °C, is proportionnal to the fourth power of the interstitial oxygen concentration $[\text{O}]$ (in at/cm^3).

$$dN_N/dt = K [\text{O}]^4 / 10^{60} \text{ (Fuller [47], Kaiser [48])}.$$

— $[\text{O}]$ is reduced during the generation of donor states.

— This generation is inhibited by carbon (Bean [38]; Lerouelle [49]). $K = 1$ for Kaiser [48]; $K = 0.5$ for Cazcarra [42]. The concentration of substitutional

carbon is reduced during the generation of donor states.

— At least 10 different double donors were identified by infrared spectroscopy in liquid helium (Compain [19], Pajot [50]) and labelled A to I. The ionization energies for the neutral species vary from 69 meV (A^0) to 53 meV (I^0) and from 156 meV (A^+) to 117 meV (I^+) for the singly ionized species.

— During an isothermal annealing, all species have the same type of evolution : they appear, their concentrations reach a maximum, and then decrease. This occurs successively in the order A to I, the same order as the order of decreasing ionisation energies. Species D and E reach the higher maximum (Compain [19], Ourmazd [34]).

— The defect symmetry is C_{2v} or $mm2$.

— Donor states are destroyed at temperature above 500 °C, with an enthalpy of activation of 2.6 eV (Fuller [47]).

— Donor states are not nuclei for oxygen precipitation during later thermal treatments, but clusters containing carbon are nuclei.

Many models were proposed (see Bourret [45]), but the best fitting with all the observations is due to the model of Ourmazd [34] : donor states are clusters of oxygen atoms; each one changes into the next labelled by the following letter one by adjunction of 2 oxygen atoms (symmetry C_{2v}). The double donor nature is due to one silicon atom moved to a quasi interstitial position and bonded with only 2 oxygen atoms. The first electrically active specie (A) contains 5 oxygen atoms.

Annealing of donor states generated during pulling. — During pulling, the silicon remains roughly 1 hour between : 500 °C and 400 °C. A large amount of oxygen donors are created for wafers with a high oxygen content, and p doping (10^{15} at/cm³ for $10\Omega \cdot \text{cm}$ wafers) can be overcompensated (more than 10^{15} donors for concentration of oxygen above 20 ppmA). To know the resistivity and the doping content, it is necessary to redissolve the donor states. This is achieved by a 650 °C annealing on the crystal, during 1/2 to 2 hours. But nuclei for later oxygen precipitation are then created.

Second type of donors.

• They are created between 550 and 900 °C (Bean [38], Capper [51], Cazcarra [42]).

• The kinetic is accelerated by the presence of carbon (Lerouelle [49]) or a 450 °C preannealing (Kanamori [52]). Its enthalpy is 1.9 eV.

• It correlates with a reduction of infrared absorption of interstitial oxygen and substitutional carbon (Bean [38], Cazcarra [42], Lerouelle [49]).

• Ionization levels vary with temperature between 0.05 eV and 0.3 eV.

• Annihilation occurs at temperature above 900 °C, but without increase of the concentration of interstitial oxygen (Cazcarra [42]). This is interpreted as a

loss of the donor nature of oxygen-carbon complexes by adjunction of oxygen atoms.

• The number of donor states correlates with the number of nuclei for later oxygen precipitation (Cazcarra [42]).

These donor states are interpreted as traps at the interface between silicon and silica for very small precipitates.

3.3.3 Precipitation of oxygen.

Absorption of infrared light by the precipitates. —

Three types of infrared absorptions by oxide precipitates were identified by Tempelhoff [53], Hu [54], and Compain [19]. They exhibit the following characteristics after isothermal annealings lasting 24 hours :

— 850 cm^{-1} absorption : the number of precipitates is maximum between 700 °C and 900 °C; it is proportionnal to the carbon concentration; interstitial oxygen has no influence.

— 1 080 cm^{-1} absorption : the number of precipitates is proportional to the oxygen concentration; carbon has no influence; the density is maximum between 850 °C and 1 050 °C.

— 1 230 cm^{-1} absorption : the density of precipitates is maximum between 900 °C and 1 000 °C, increases with oxygen content or with the decrease of carbon content.

Tempelhoff [53] gave an interpretation of these absorptions by the nature of the phase precipitated, Hu [54] by its shape.

The absorption at 1 080 cm^{-1} induces a « noise » in the interstitial oxygen absorption at 1 106 cm^{-1} , difficult to take into account. It is thus better, in the case of wafers with high oxygen precipitation, to measure the concentration of oxygen by the absorption at 517 cm^{-1} .

Low temperature precipitates. — The nature of precipitates created between 600 °C and 750 °C was determined by Bourret [45] : 80 % of the oxygen is in small platelets of amorphous silicas 20 % is in « ribbon like defects » oriented (011) and made up of small ribbons of coesite (8 Å thick in the (100) direction and 70 Å wide) followed by dipoles of dislocations with a burgers vector $b = \pm (110)$. 80 % of the stresses around precipitates are relaxed by emission of interstitials. No punch out dislocations are observed, i.e. the pressure is large enough to create coesite, but is lower than the silicon critical resolved shear stress at this temperature (Fig. 17, see Leroy [27], Bourret [45]).

High temperature precipitates. — A very large bibliography exists : see Patel [40], Claeys [43, 44], Leroy [27].

At a temperature above 750 °C, there is no longer a coesite phase, but only amorphous silica. But precipitates punch out dislocations (Fig. 18).

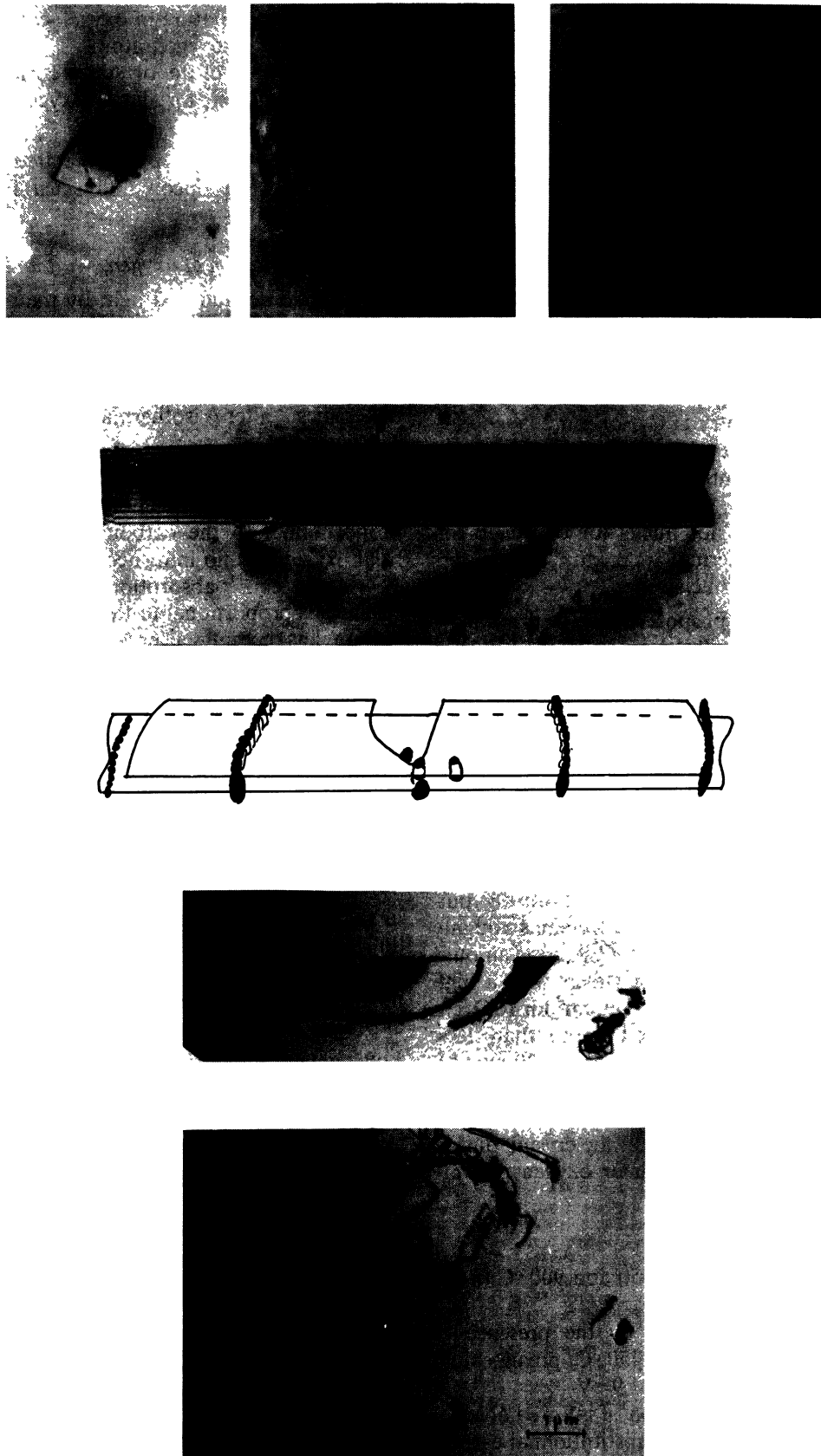


Fig. 18. — Up : Amorphous SiO_2 platelets, with punched out dislocations loops, and a circular stacking fault with a quasi spherical precipitate in its middle (annealing at 900°C) ; Middle : ring shaped stacking fault after 4 thermal treatments 100 mn at $1\,100^\circ\text{C}$ (see Plougonven [56], Leroy [27]). Down : very complex defects due to a succession of thermal treatments between 925°C and $1\,000^\circ\text{C}$, very efficient for gettering ; All the TEM photos are from P. Beaufrère.

Tan [55] made an extensive study of dislocation loop columns punched out by square, (001) oriented platelets of amorphous silica. Dislocations have $a[a/2.(011)]$ Burgers vector and have a square shape, gliding in (101) family planes. Eight columns of dislocations can be generated by a single precipitate.

Punched out dislocations can transform by glide into extrinsic stacking faults, centred on a precipitate, and growing by capture of the interstitial of silicon emitted during the growth of the precipitates.

During cooling, a small precipitation occurs in the core of dislocations, inducing very complex defects : ring shaped stacking faults (Plougonven [56]) and various type of defects as shown in figure 18.

The growth kinetics of the platelet like precipitates was studied by Wada [57], between 750 °C and 850 °C. He showed that the thickness remained constant (near 8 nm) and that the edge of the square grew with time t at rate $Kt^{3/4}$. This kinetics corresponds to the rate of diffusion of oxygen to the precipitate.

The growth kinetics of the stacking fault in the 900 °C-1 150 °C range shows the same type of law, i.e. radius proportionnal to time exponent 3/4, either for single stacking faults (Patel [40] or for ring shaped stacking faults (Plougonven [56])). Leroy [27] showed that this law was due to the kinetics of capture of the interstitials by the stacking fault when the number of oxide precipitates was large compare to the number of stacking faults, and due to the oxygen diffusion in the other case. Clàeys [44] showed a reduction of the SF radius near the interface under a neutral or a chlorinated atmosphere, i.e. when the surface was a sink for interstitials.

When the annealing occurs at temperature higher than 1 100 °C the proportion of platelets decreases and the majority of the precipitates are quasi-spherical (sometimes (111) type faces).

Nucleation of precipitates. — Small precipitates grow at high temperature only if their size is larger than a critical size. Cazcarra [41], figure 17 determined a domain where nucleation of new precipitates occurs, under a critical temperature increasing with the oxygen and the carbon content. The enthalpy of activation of the nucleation is around 2.3 eV. Inoue [58] made a simple model showing a maximum in nuclei generation around 700 °C and the suppression between 900 °C and 1 000 °C. Interstitials provided by an oxidation increase the dissolution rate of nuclei.

Thermal history of the wafers. — When wafers are submitted to thermal treatments at temperatures above 900 °C, the precipitation of oxygen occurs on nuclei function of the thermal history :

It is clear in figure 15 that the number of oxygen precipitates follows the fluctuations of the pulling conditions, i.e. fluctuations in oxygen, carbon and clusters of point defects concentration, through the number of nuclei generated during cooling of the crystal, and during the process.

One can remove this type of memory effect in two ways : a thermal treatment at very high temperature (above 1 280 °C) dissolves the precipitates and all the nuclei (Compain [19]) changing the density and the nature of the precipitates during following thermal treatments. There is a high risk of contamination in annealing at such elevated temperature. An annealing at 750 °C induces a quasi homogeneous distribution of small precipitates.

3.3.4 Defect free zone (DFZ). — It is well known that a thin layer free of oxygen precipitates exists at the surface of the wafer, at the place where the circuits are implanted. Hu [59] performed a detailed study of this phenomenon :

At the surface is a thin layer from which oxygen has outdiffused preventing its precipitation.

In the bulk all oxygen has precipitated.

In between is a zone where oxygen has only partially precipitated on very few nuclei ; the pattern of this zone is a memory of the pulling conditions for 1 000 °C thermal treatments.

For 800 °C thermal treatment, the nucleation of precipitates in that zone seems slower than in bulk silicon, even if the concentration of oxygen has not decreased : a large importance of point defects in nucleation is then demonstrated.

As the thickness of this Defect Free Zone (DFZ) plays a key role in wafer quality, it is of interest to trigger a large outdiffusion of oxygen without nucleation of precipitates before or at the beginning of the integrated circuit process (by annealing the wafers at temperatures above 1 000 °C for several hours).

3.3.5 Impact of precipitation on the quality of the wafers. — Oxygen precipitation induces first an increase in the concentration of interstitials : this can accelerate diffusions and make oxidation stacking faults grow.

Second, precipitates generate dislocations. Wafers are more sensitive to stresses (see next §) by reducing the critical shear stress of silicon. However precipitates have a very positive effect in gettering metallic impurities (§ 4.2).

It is necessary to program the thermal treatments to achieve a large defect free zone.

3.4 STRAINS, STRESSES AND DISLOCATIONS.

3.4.1 Critical shear stress. — Stresses can generate dislocations lying in (111) type planes, with $a/2$ (110) type of Burgers' vector in silicon. Dislocations are generated when the resolved shear stress τ exceeds a critical value τ_c , and they move as long as $\tau > \tau_m$ (τ_m , critical shear stress for glide, is smaller than τ_c , critical shear stress for generation of a dislocation).

At any given time there is a superposition of various types of stresses : imposed stresses (applied stresses, thermal stresses due to temperature gradients, stresses due to the films deposited on the wafers, stresses at the edge of films), and stresses around precipitates or cracks.

The apparent critical shear stress, τ'_c (or τ'_m), is the imposed shear stress necessary to induce plastic deformation, i.e. τ_c or τ_m minus the shear stresses due to precipitates or cracks.

Cracks are due to scratches or to edge shipping. Scratches are deactivated by a chemical etching in an HNO_3/HF solution, and edge shipping reduced by chamfering of the edge of the wafer.

τ'_c and τ'_m are determined by studies of pulling or bowing strains (Patel [39, 40]), or of the pattern of dislocations due to a well known distribution of stresses, around an indentation rosette (Hu [60]) or during cooling a row of wafers (Leroy [61]). These values were discussed by Leroy [27].

τ'_c is stable at low temperature, its value is 2.5×10^8 Pa. For that stress, fracture occurs. At a temperature above 600°C , dislocations are emitted. τ'_c decreases with increasing temperature :

$$\text{Log}_{10} \tau'_c(T)/\tau'_c(T') = (T' - T)/250^\circ\text{C}.$$

The reduction of τ'_c due to the precipitates is nearly proportionnal to the quantity of oxygen precipitated (Leroy [61]), but is larger for large precipitates grown at 1000°C than for small precipitates generated at 800°C (see Leroy [27]). Figure 19 gives typical values of τ'_c compatible with the experiments of Leroy [27] for (100) wafers.

It seems that interstitial oxygen increases the resistance to the generation of dislocations (Sumino

[62, 63]), or their migration (Hu [60]). It follows that FZ wafers with small oxygen concentration, are more sensitive to stresses than CZ wafers.

3.4.2 Generation of dislocations by thermal gradients. — Inserting or pulling a row of wafers out of a furnace induces on the wafers temperature gradients which possess a radial symmetry; these gradients, larger during wafer removal than during insertion, generate stresses, compressive in the centre and tensile at the edge of the wafer during removal (it is the contrary during insertion).

Thermal stresses acting on flat wafers have only two stress components, σ_{rr} (radial) and $\sigma_{\phi\phi}$ (tangential). They vary with the distance r to the centre, but not along the wafer thickness z .

When the wafer is not flat, this bow induces a difference in substrate strains, and thus in substrate stresses between the convex side and the concave side. Consequently, in a bowed wafer, σ_{rr} and $\sigma_{\phi\phi}$ vary with z : they are more compressive at the centre of the concave side, and less compressive (or tensile) at the centre of the convex side. Figure 20 give typical values of these stresses along the radius of the wafer. See Leroy [61, 27].

Thermal stresses can generate dislocations when the resolved shear component τ in a (111) plane along a (101) direction is larger than τ'_c , which varies with the temperature and the oxygen precipitation (see § 3.4.1). One must compare τ'_c of figure 19 with τ at the centre

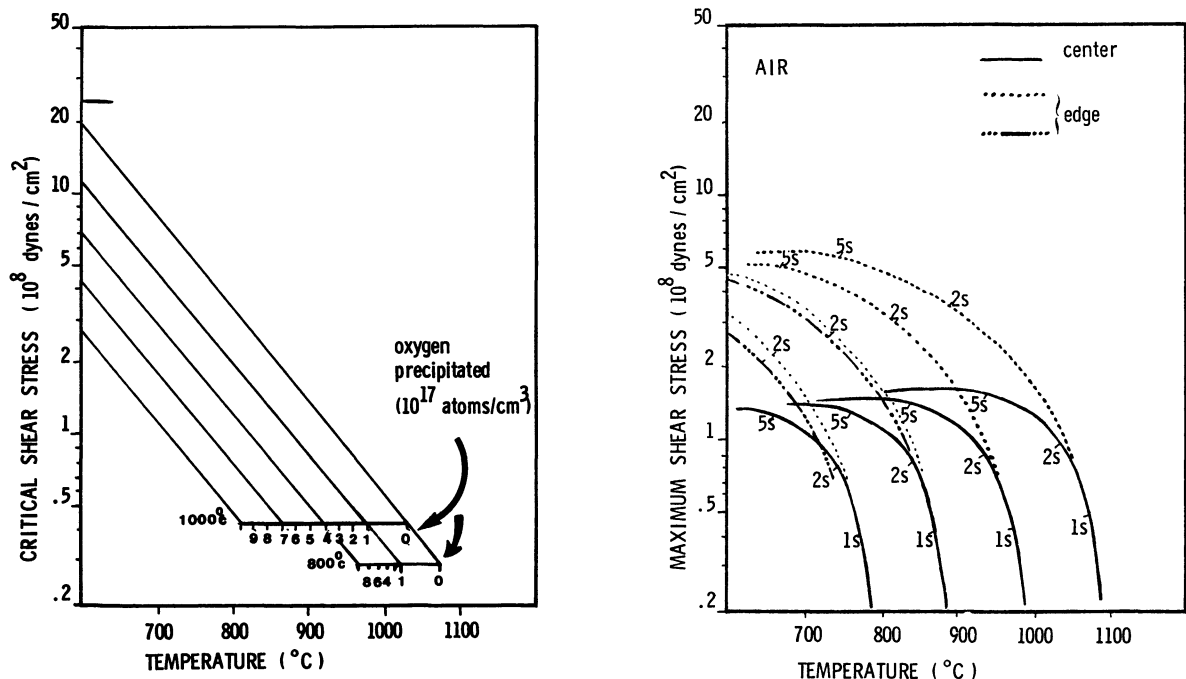


Fig. 19. — Left : critical shear stress in silicon function of the temperature, for two modes of precipitation of oxygen : large number of small precipitates at 800°C , small number of large precipitates at 1000°C . Quantity of oxygen precipitated in 10^{17} at/cm³, from Leroy [61]. Right : maximum resolved shear stress at the center and at the edge of the wafer function of the temperature, during cooling a row of wafers; furnace temperature : 800°C , 900°C , 1000°C , 1100°C . On the curves, numbers indicate time in seconds from the beginning of the cooling — $1\text{ Pa} = 10\text{ dynes/cm}^2$.

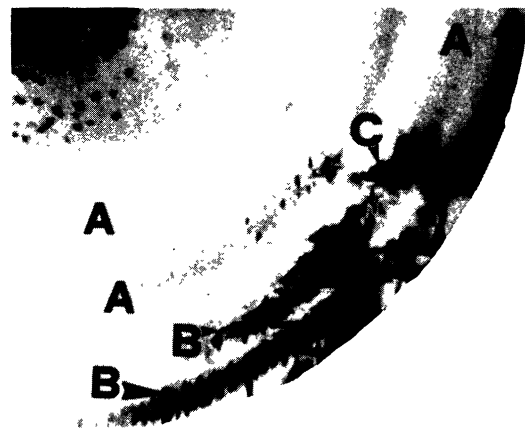
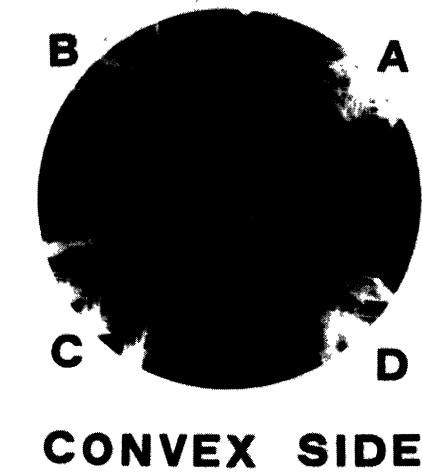
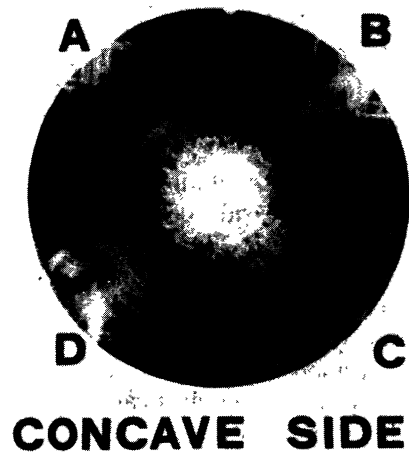
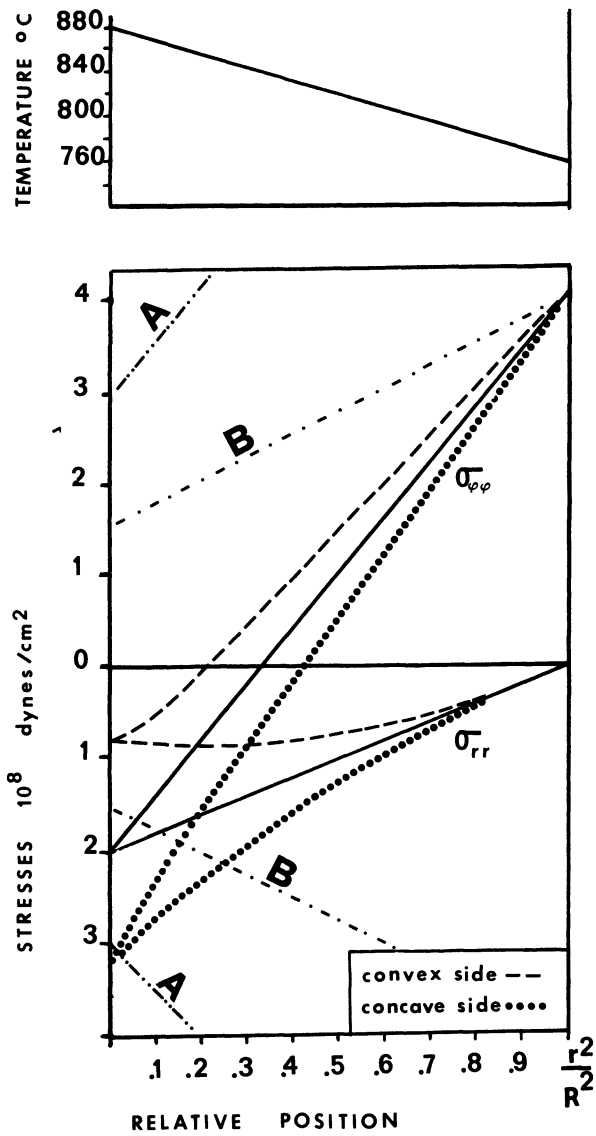


Fig. 20. — a) The radial and tangential components of stresses induced by the cooling of a row of wafer σ_{rr} and $\sigma_{\phi\phi}$ are plotted as a function of $(r/R)^2$. r is the distance to the centre and R is the wafer radius — 1 Pa = 10 dynes/cm². Stress values are plotted for the concave side (. . .), for the neutral fiber (—), and for the convex side (— . —). The temperature gradient is shown in the above insert. b) Zones of dislocations, generated on the concave and convex sides have been revealed by using a Jenkins-Wright etch. c) X-rays topograph shows dislocations (slip lines) are generated in the rings with oxygen precipitates (Leroy [61]).

and at the edge, where they are maximum. Typical values of τ at the centre and at the edge were determined by Hu [64, 60] and Leroy [61], for flat wafers and by Leroy [61, 27] for bowed wafers. See figure 19. It is clear that τ'_c is reached nearly at the same time at the centre and at the edge, but always first in areas with high oxygen precipitation, and always at the centre of the concave side before the centre of the convex side (Leroy [61, 27]). The critical parameter is then the direction of the bow and not its absolute value. As small a bow as $3 \mu\text{m}$ is sufficient in 100 mm diameter wafers to impose this direction (Leroy [27]). Figure 20 is a good illustration of these facts.

During the process, the films can induce a change of bow at high temperature, different from the bow measured at room temperature; see Leroy [65].

Critical temperature for pulling a row of wafers. —

The critical temperature T_c for pulling a row of wafers out of a furnace is defined by the following process: the row of wafer is pulled in less than 2 seconds from the furnace temperature T to room temperature. Warpage is measured, and wafers are reinserted in the furnace, but at temperature $T + \Delta T$. T_c is the first temperature for which a plastic deformation occurs. Figure 21 give the value of T_c for two modes of oxygen precipitation and the values calculated

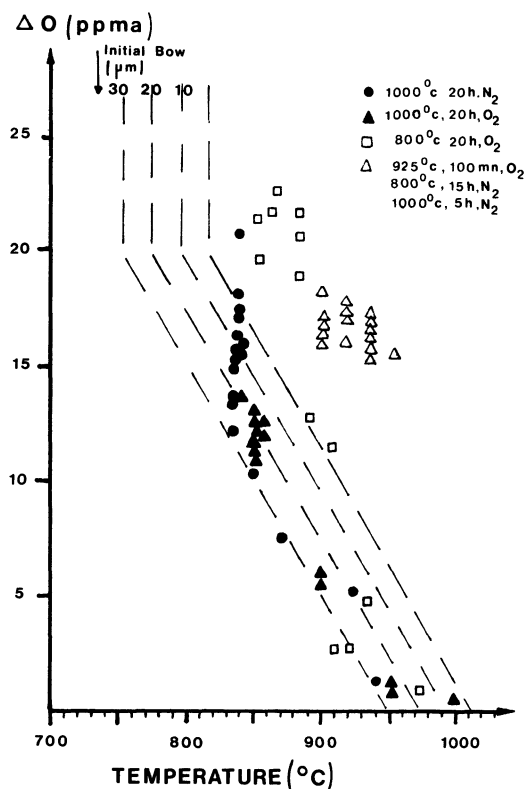


Fig. 21. — Critical temperature for pulling a row of $400 \mu\text{m}$ thick, 82 mm diameter wafers, out of a furnace; experimental points reference the thermal treatment of oxygen precipitation. Dotted lines are calculations with values of figure 19 for an annealing at $1000 \text{ }^\circ\text{C}$, and take the bow into account.

by Leroy [27]. These values remain the same when the thickness, the diameter, the distance are multiplied by the same number.

Specifications. — To reduce the risks of plastic deformation, a maximum of oxygen concentration is imposed, and the edge of the wafers is chamfered. To reduce the yield loss due to the plastic deformation, a specification of convexity and of maximum bow must be added to incoming inspection.

The stresses due to bow are proportionnal to the square of the ratio of radius R to thickness h (Leroy [61, 27]). Specifications have to maintain this ratio smaller than 120, i.e. increase h with R .

To reduce thermal stresses, the furnace temperature is slowly reduced (3 to $6 \text{ }^\circ\text{C}/\text{min}$), to a temperature near $850 \text{ }^\circ\text{C}$ at the beginning of the I.C. manufacturing process (for a small oxygen precipitation), and to between $750 \text{ }^\circ\text{C}$ and $800 \text{ }^\circ\text{C}$ at the end. This type of cooling is called ramping.

3.4.3 C MOS wafers. — Wafers used for C MOS circuits are made of highly boron doped substrates ($1.5 \times 10^{19} \text{ at}/\text{cm}^3$) covered by a lightly boron doped epitaxy ($7 \times 10^{14} \text{ at}/\text{cm}^3$), $12 \mu\text{m}$ thick. Boron induces a large retraction of the crystalline parameter, $\Delta l/l = 0.2 [B]/5 \times 10^{22}$ where $[B]$ is the concentration of boron in at/cm^3 . Strains and stresses are present in the wafer thickness, but they are independent of the radial position. $\sigma_{rr} = \sigma_{\varphi\varphi} = \sigma$ varies only with z ; it is proportionnal to the difference between the concentration $C(z)$ and the average concentration in the whole wafer.

Typical values of concentration and stresses are given in figure 22 (Leroy [10]). These measurements were done after annealings inducing a redistribution of the dopant. The wafer was $600 \mu\text{m}$ thick, but a change in the wafer thickness h introduces no change for the stresses in the epitaxy, but only in the stresses in the substrate (σ_s is inversely proportionnal to h). Stresses are compressive in the epitaxy, they are proportionnal to the concentration of the substrate, and they induce a convex bow independent of the temperature. The resolved shear component, maximum at the surface, is $\tau = \sigma/\sqrt{6} = 0.4 \times 10^8 \text{ dynes}/\text{cm}^2$ in the example. Comparing figure 19 it is clear that dislocations are generated at temperature above $1025 \text{ }^\circ\text{C}$, since there is no oxygen in the epitaxy. Dislocations, with a Burgers' vector $a/2 (101)$ glide in the (111) type planes, downwards until $\tau = \tau_m$ (and then they stop) and along the $(\bar{1}\bar{1}0)$ direction, with a constant velocity ($0.02 \text{ cm}/\text{s}$). They thus reach the edges of a 100 mm in diameter wafer in less than 10 min at $1025 \text{ }^\circ\text{C}$. There is no emergence of these dislocations in the active zone of the wafer and thus is no yield loss. Figure 22 shows a pattern of such dislocations on wafers with and without oxygen precipitation. Comparing the values of $\tau(z) = \sigma(z)/\sqrt{6}$ and the depth of the horizontal part of the dislocation is a fine way to measure $\tau_m(T)$.

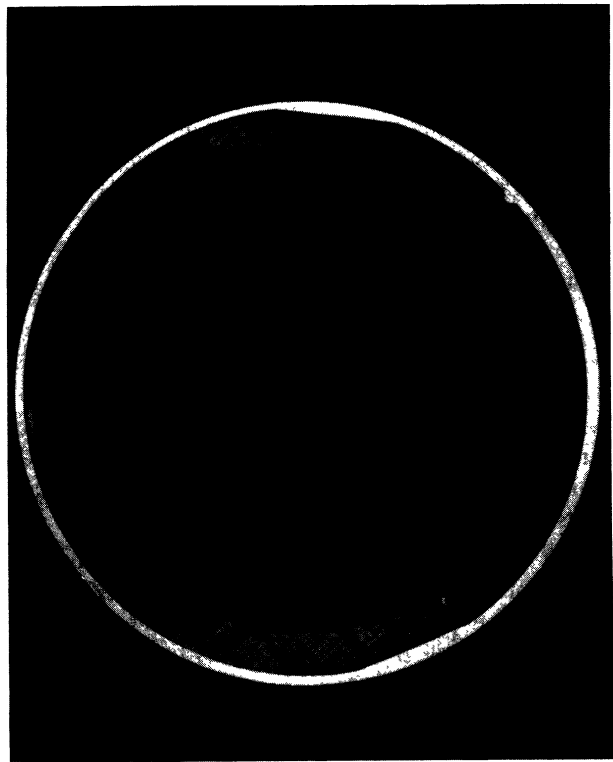
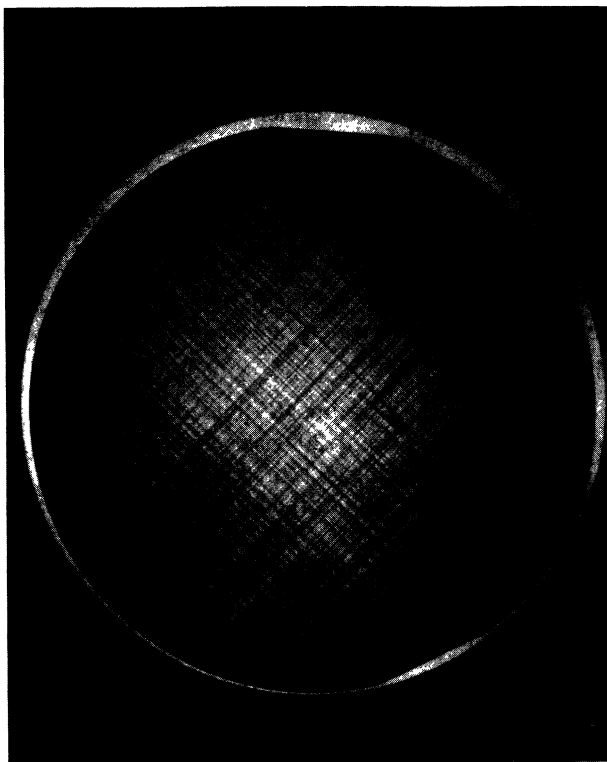
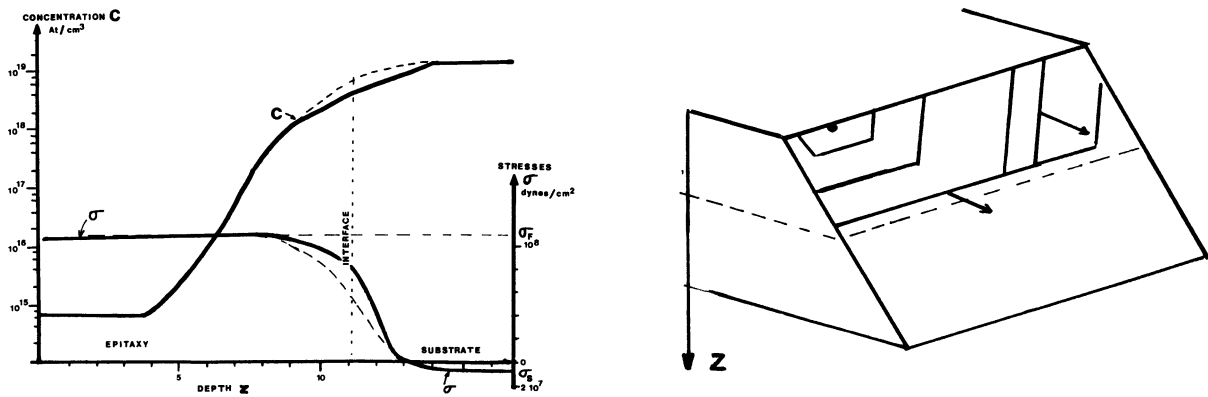


Fig. 22. — Up, left : distribution of the boron concentration in the epitaxy and in the substrate, and stresses associated, in a C MOS wafer, after annealings (1 Pa = 10 dynes/cm²). Up, right : migration of dislocations gliding in a (111) plane. Down : typical patterns of dislocations after a 1 140 °C thermal treatment : Left : no oxygen precipitated ; right : large precipitation of oxygen.

These dislocations relax the stresses and change the bow of the wafer. A complete relaxation occurs when d , the distance between the dislocations, is :

$$d = \frac{5 \times 10^{22}}{[B]} \frac{5.43 \times 10^{-4}}{0.4} = 4.5 \mu\text{m}.$$

These dislocations have no detrimental effects on the circuits (no emergence except at the edge of the wafer), but a very benefit role : they act as gettering centres for metallic impurities (see § 4).

4. Gettering.

4.1 CONTAMINATION INTRODUCED DURING HIGH TEMPERATURE PROCESS STEPS. — The process steps at which contamination occurs are : at room temperature, wafer polishing (however the level introduced by that process step is now very low), wafer handling (the use of metallic tweezers is now forbidden in manufacturing lines), wafer cleanings, chemical etches, or in ionic implanters ; at high temperature, from and through quartz tubes, from quartz wafer-carrying boats or through gases.

Li, Na, K, Cs, Ca segregate in insulating layers, and their role in silicon is not very important.

Cu, Ag, Au were the first metallic contaminants studied, during the 1960's, but their level has decreased during the 1970's following progresses in process control. Fe and Ni, two elements found in stainless steel, play the most important part in the fabrication technology, because they cause a catastrophic degradation of integrated devices, even at very low concentrations (a few ppb in the bulk).

The migration of metal atoms in silicon is due to an interstitial mechanism : the diffusion coefficient is large ($10^{-7} < D < 10^{-4}$ cm²/s) and the activation energy low (0.2 to 1 eV). Thus a small amount of contaminant can easily diffuse through the entire substrate thickness during a high temperature step.

The solubility limit of metals in intrinsic silicon (doped with less than 10^{18} at/cm³) decrease very quickly with temperature (Fig. 6). Thus reactions of precipitation are induced by a slow decrease of temperature, especially near the surfaces where the concentration of vacancies and interstitials changes quickly.

Dislocations are very efficient sinks for metallic atoms, and precipitates are mainly located on dislocations. This allow gettering.

4.2 GETTERING TECHNIQUES. — The role of gettering techniques is to trap atoms of metal and/or silicon interstitials in excess in the inactive parts of the wafer. The net result is to empty the rest of the wafer of its contaminants.

4.2.1 Intrinsic gettering. — Complexes formed of oxide precipitates and dislocations in CZ grown crystals can capture atoms of metal. This cleaning occurs all along the process and is beneficial to the circuits (Tice [66]).

Dislocations located between a substrate and an epitaxial layer are also gettering centres. In C MOS wafers one thermal treatment at 1 100 °C is enough to generate them (§ 3.4.3). Salih [67] proposed to introduce misfit dislocations by starting the epitaxial growth in a mixture of SiCl₄ and GeH₄; the germanium atoms present in silicon reduce the crystalline parameter.

4.2.2 Gettering by backside defects. — Dislocations introduced at the rear side of the wafer, before or during the process, can capture atoms of metal; many method have been proposed :

- Sand blasting (Metz [68]), sound stressing (Yang [69]), or other types of mechanical damage.
- Ion implantations (Cullis [70]), especially of argon (Nassibian [71]) can introduce a well controlled amount of defects. Their efficiency, however, decreases during subsequent treatments because they are annealed out.
- Laser damage was also used.
- The deposition of a polysilicon film at the back

of the wafer is also efficient as it introduces many grain boundaries rich in dislocations.

4.2.3 Gettering by stresses. — Gettering can also occur in highly stressed areas, either on dislocations, or because of stress gradients. The deposition of a nitride or of a silicide layer at the back of the wafer is used for this purpose.

4.2.4 Gettering by diffusions. — High concentrations of dopant getter by two mechanisms :

First, they introduce misfit dislocations.

Second, the electric field at the periphery of the diffused areas capture isolated atoms of metal (interstitial atoms with a positive charge), such as Cu⁺, Au⁺... in boron doped areas, substitutionnal atoms with a negative charge in phosphorus doped areas, such as Au⁻.

Third, the limit of solubility is higher in highly doped areas, for all the metals.

This gettering is used either in backside diffusions, or in isolation areas used for bipolar circuits.

5. Conclusion : what is a silicon wafer for integrated circuits process ?

5.1 SPECIFICATIONS. — Listed below are the requirements for silicon wafers specifications.

5.1.1 Shape.

— Ratio R/h , i.e. radius R divided by thickness h , should be smaller than 120 (risk of warpage, § 3.4.2).

— Edge chamfering (slip lines, § 3.4.1).

— No active scratches (generation of dislocations, § 3.4.1).

— Initial bow convex, between 0 μm and 30 μm (warpage, § 3.4.2).

— Flatness better than 9 μm (photolithography, § 1.2).

— Wafer cut aslant 1° to 2° from the crystallographic direction (100) or (111), to have a better control of the shape of surface steps during epitaxy (no « wash out », control of the « epi shift »), and to reduce the oxidation enhanced diffusion of dopants (see Fig. 15).

5.1.2 Doping.

— Resistivity between two values ($RS_1 < RS < RS_2$).

— Limitation of the radial gradient (15 %) (§ 2.4.2).

— Limitation of the fluctuations (15 %) (§ 2.4.3).

5.1.3 Surface quality. — Hydrophilic/hydrophobic : the contamination is larger on hydrophobic surfaces, i.e. with a thicker native oxide.

5.1.4 Oxygen/gettering.

— Maximum of oxygen concentration, depending on the I.C. process, from 18 ppmA to 22 ppmA (plastic deformation, § 3.4).

— Either external gettering (FZ wafers) or specification of a minimum for oxygen concentration (12-14 ppmA) for internal gettering (§ 4.2). In order

to reach a suitable quantity of oxygen precipitated in small precipitates at the end of the I.C. process (gettering/plastic deformation) either a specification of a minimum for the number of nuclei for oxygen precipitation, or a specification mini/maxi for carbon content (§ 3.3 and 3.4).

5.2 ADDITIONAL STEPS.

5.2.1 Thermal treatments prior to I.C. manufacturing. — To achieve a large defect free zone at the end of the process, and the right number of nuclei for oxygen precipitation, one can add thermal treatments before the I.C. process (see for instance Borland [72]).

Thermal history of the wafers is illustrated in figure 23.

- Kinetics of cooling of the crystal during pulling, with differences between seed, middle and tail end wafers (§ 2.4.1).

- Dissolution of donor states (the whole crystal annealed at 650 °C, 1 to 2 hours), with induction of small nuclei (§ 3.3.2).

- Slicing of the crystal and polishing of the wafers.

- Defect free zone constitution by a high temperature annealing (1 100 °C-1 150 °C, 1-3 hours, N₂ atmosphere). The duration of this annealing is limited by the reduction of the critical shear stress τ_c due to the precipitation of oxygen in the bulk, correlated with oxygen and carbon content (seed/tail end wafers) (§ 3.3 and 3.4). An increase in the number of nuclei can be achieved by a slow heating from 700 °C to 850 °C and then a fast heating to 1 100 °C.

- Germination of nuclei by an annealing between 700 °C and 800 °C, 2-10 hours, especially for wafers pulled in the vacuum (no carbon); duration depends on the position of the wafer in the crystal.

- Growth of precipitates by an annealing at 1 000 °C-1 050 °C, 2-10 hours, to insure a good gettering capacity at the beginning of the I.C. process.

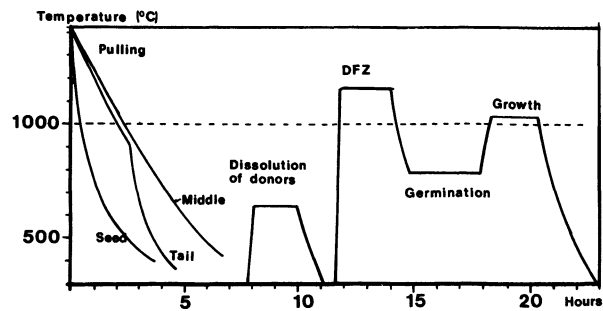


Fig. 23. — Typical thermal history of the wafer : left : cooling of the crystal for seed, middle and tail end wafers; middle : 650 °C annealing of the crystal to dissolve donor states; right ; typical annealings to induce a defect free zone, to nucleate a large number of precipitates, and to induce oxygen precipitation for internal gettering.

Note that, because CZ wafers have a higher critical shear stress than FZ wafers at the beginning of the I.C. process (before oxygen precipitation), they are preferred, especially when high temperature thermal treatments (above 1 000 °C) occur only during this beginning.

5.2.2 Gettering. — An additional operation to increase the gettering efficiency can be selected in those listed in § 4.2.

When all these specifications are met, and all the thermal and gettering treatments achieved, the silicon wafer is ready to be used in an integrated circuit process.

Appendix. — Very recent developments on Silicon Material Science and technology were published in references [73 to 75].

Acknowledgments.

The author wants to thank G. Barbottin, P. Beaufrère, J. Lerouelle and M. Rivier for helpful discussion of the article.

References

- [1] DENNARD, R. H., GAENSSLEN, F. H., YU, H. N., RIDEOUT, V. L., BASSOUS, E. and LE BLANC, A. R., *IEEE J. Sol. St. Circuits* **SC 9** (1974) 256.
- [2] DENNARD, R. H. and WORDEMAN, M. R., *Physica* **129B** (1985) 3.
- [3] ROSENBERGER, F., *Fundamentals of crystal growth 1*, Solid State Science 5 (Springer-Verlag) 1979.
- [4] ZULEHNER, W. and HUBER, D., *Czochralski grown Silicon in Crystals 8* (Springer-Verlag) 1982.
- [5] DIETZE, W., KELLER, W. and MUHLBAUER, A., *Float zone grown silicon in Crystals 5*, Springer-Verlag 1981.
- [6] DASH, W. C., *J. Appl. Phys.* **30** (1959) 459.
- [7] TRUMBORE, F. A., *The Bell System Tech. J.* (1960) p. 205.
- [8] REA, S. N., *J. Crystal Growth* **54** (1981) 267.
- [9] RAMACHANDRAN, P. A. and DUDUKOVIC, M. P., *J. Crystal Growth* **71** (1985) 399.
- [10] LEROY, B., unpublished result (1985).
- [11] COCHRAN, W. G., *Proc. Camb. Philos. Soc.* **30** (1934) 365.
- [12] PROUDMANN, J., *Proc. R. Soc. A* **92** (1916) 408.
- [13] TAYLOR, G. I., *Proc. R. Soc. A* **93** (1916) 99 ; **100** (1921) 114 ; **102** (1922) 180 ; **104** (1923) 213.
- [14] CARRUTHERS, J. R. and NASSAU, K., *J. Appl. Phys.* **39** (1968) 5205.
- [15] MURGAI, A. et al. *J. Electrochem. Soc.* **123** (1976) 224 ; **126** (1979) 2240 ; in *Semiconductor Silicon 1977*, p. 72 and 83 ; in *Semiconductor Silicon 1981*, p. 113.
- [16] CARRUTHERS, J. R., *J. Crystal Growth* **36** (1976) 212.
- [17] KOBAYASHI, N., *J. Crystal Growth* **52** (1981) 425.

- [18] FEIGL, G., *Solid State Technol.* (1983) 121.
- [19] COMPAIN, H., Thesis, Paris (1982).
- [20] CARLBERG, T., KING, T. B. and WITT, A. F., *J. Electrochem. Soc.* **129** (1982) 189.
- [21] NOZAKI, T., YATSURUGI, Y. and AKIYAMA, N., *J. Electrochem. Soc.* **117** (1970) 1566.
- [22] HU, S. M., *J. Vac. Sci. Technol.* **14** (1977) 17.
- [23] DE KOCK, A. J. R. in *Handbook on semiconductors* 3 (1980) 247.
- [24] DE KOCK, A. J. R. and VAN DE WIJGERT, W. M., *J. Crystal Growth* **49** (1980) 718; *Appl. Phys. Lett.* **38** (1981) 888.
- [25] ABE, T., KIKUCHI, K. and SHIRAI, S., in *Semiconductor silicon 1977*, p. 95.
- [26] ABE, T., KIKUCHI, K., SHIRAI, S. and MURAOKA, S. in *Semiconductor silicon 1981*, p. 54.
- [27] LEROY, B., Thesis, Paris VII university (1983).
- [28] PAJOT, B. and DELTOUR, J. P., *Infrared Phys.* **7** (1967) 195.
- [29] PAJOT, B., *Analisis* **5** (1977) 293.
- [30] CORBETT, J. W., WATKINS, G. D. and MAC DONALD, R. S., *Phys. Rev.* **135A** (1964) 1381.
- [31] BRELOT, A., Thesis, Paris VII university (1972).
- [32] NEWMAN, R. C. and WILLIS, J. B., *J. Phys. Chem. Solids* **26** (1965) 373.
- [33] WATKINS, G. D., CORBETT, J. W. and MAC DONALD, R. S., *J. Appl. Phys.* **53** (1982) 7097.
- [34] OURMAZD, A., SCHROTER, W. and BOURRET, A., *J. Appl. Phys.* **56** (1984) 1670.
- [35] HROSTOWSKI, H. J. and KAISER, R. H., *J. Phys. Chem. Solids* **9** (1959) 214.
- [36] MAGEE, T. J., LEUNG, C., KAWAYOSHI, H., FURMAN, B. K. and EVANS Jr., C. A., *Appl. Phys. Lett.* **38** (1981) 891.
- [37] NEWMAN, R. C. and WAKEFIELD, J., *J. Phys. Chem. Solids* **19** (1961) 230.
- [38] BEAN, A. R. and NEWMAN, R. C., *J. Phys. Chem. Solids* **32** (1971) 1211; **33** (1972) 255.
- [39] PATEL, J. R. and CHAUDHURI, A. H., *J. Appl. Phys.* **34** (1963) 2788.
- [40] PATEL, J. R., *Discuss. Farad. Soc.* **38** (1964) 201; in *Semiconductor Silicon 1977*, p. 521; in *Semiconductor Silicon 1981*, p. 189.
- [41] CAZCARRA, V., *Inst. Phys. Ser. Conf.* **46** (1978) 303.
- [42] CAZCARRA, V. and ZUNINO, P., *J. Appl. Phys.* **51** (1980) 4206.
- [43] CLAEYS, C. L., *Anais Oficina Brasil. Microelectron.* (1981) 193.
- [44] CLAEYS, C. L. et al. *Physica* **116B** (1983) 148.
- [45] BOURRET, A. in *Proceedings of the 13th international conference on defects in semiconductors*, Coronado (1984).
- [46] BOURRET, A., THIBAUT-DESSEAUX, J. and SEIDMAN, D. N., *J. Appl. Phys.* **55** (1984) 825.
- [47] FULLER, C. S. and LOGAN, R. A., *J. Appl. Phys.* **28** (1957) 1427.
- [48] KAISER, W., FRISCH, H. L. and REISS, H., *Phys. Rev.* **112** (1958) 1546.
- [49] LEROUILLÉ, J., *Phys. Status Solidi (a)* **67** (1981) 177.
- [50] PAJOT, B., COMPAIN, H., LEROUILLÉ, J. and CLERJAUD, B., *Physica* **117B** and **118B** (1983) 110.
- [51] CAPPER, P., JONES, A. W., WALLHOUSE, E. J. and WILKES, J. G., *J. Appl. Phys.* **48** (1977) 1646.
- [52] KANAMORI, A. and KANAMORI, M., *J. Appl. Phys.* **50** (1979) 8095.
- [53] TEMPELHOFF, K. and SPIEGELBERG, F. in *Semiconductor Silicon 1977*, p. 585.
- [54] HU, S. M., *J. Appl. Phys.* **51** (1980) 5945.
- [55] TAN, T. Y. and TICE, W. K., *Philos. Mag.* **34** (1976) 615.
- [56] PLOUGONVEN, C., LEROY, B., ARHAN, J. and LECUILLIER, A., *J. Appl. Phys.* **49** (1978) 2711.
- [57] WADA, K., INOUE, N. and KOHRA, K., *J. Crystal Growth* **49** (1980) 749.
- [58] INOUE, N., WADA, K. and OOSAKA, J. in *Semiconductor Silicon 1981*, p. 282.
- [59] HU, S. M., *J. Appl. Phys.* **52** (1981) 3974.
- [60] HU, S. M., *J. Appl. Phys.* **46** (1975) 1465, 1470 and 1869; *Appl. Phys. Lett.* **31** (1977) 53 and 139.
- [61] LEROY, B. and PLOUGONVEN, C., *Electrochem. Soc. Meeting Ext. Abstracts*, Philadelphia (1977). *J. Electrochem. Soc.* **127** (1980) 961.
- [62] SUMINO, K. and YONENAGA, I., *Japan. J. Appl. Phys.* **19** (1980) L49 and L763.
- [63] SUMINO, K. in *Semiconductor Silicon 1981*, p. 208.
- [64] HU, S. M., *J. Appl. Phys.* **40** (1969) 4413.
- [65] LEROY, B., *Passivation induced phenomena in silicon substrates* in «Instabilities in silicon devices» (North Holland) 1986.
- [66] TICE, W. K. and TAN, T. Y., *Appl. Phys. Lett.* **28** (1976) 564.
- [67] SALIH, A. S. M., KIM, H. J., DAVIS, R. F. and ROZGONYI, G. A. in *Semiconductor processing*, ASTM, p. 272 (1984).
- [68] METZ, E. J., *J. Electrochem. Soc.* **112** (1965) 420.
- [69] YANG, K. H., KAPPER, H. F. and SCHWUTTKÉ, G. H., *Phys. Status Solidi (a)* **50** (1978) 221.
- [70] CULLIS, A. G., SEIDEL, T. E. and MEEK, R. L., *J. Appl. Phys.* **49** (1978) 5188.
- [71] NASSIBIAN, A. G. et al. *J. Appl. Phys.* **47** (1976) 992; *IEEE Solid State Elect. Dev.* **3** (1979) 127.
- [72] BORLAND, J. O., KUO, M., SHIBLEY, J., ROBERTS, B., SHINDLER, R. and DALRYMPLE, T. in *Semiconductor Processing*, ASTM, 1984, p. 49.
- [73] VLSI Science and Technology, 1985, Electrochemical Society, Pennington, N.J. (1985).
- [74] Extended Abstracts, ECS Meeting, 86-1 Boston-Electrochemical Society, Pennington (1986).
- [75] Proceedings of the fifth international Symposium on Silicon Materials Science and Technology, Electrochemical Society Pennington, N.J. (1986).