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A complete dry etching process for MOS FET's with submicron gate length

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Résumé. — Un procédé de gravure sèche a été mis au point pour la fabrication de transistors MOS submicroniques en technologie canal N grille silicium. La gravure ionique réactive a été utilisée pour graver le Si_3N_4 , le silicium polycristallin et le SiO_2 déposé dopé au phosphore (PSG). L'aluminium a été gravé par plasma. Le procédé fournit une gravure en pente des trous de contact dans le PSG et une surface aplanie du PSG, ceci pour améliorer la couverture aux marches de la métallisation et pour faciliter la gravure de l'aluminium. Des transistors MOS ayant des longueurs de grilles de $0,6 \mu\text{m}$ ont été fabriqués avec succès selon ce procédé.

Abstract. — An anisotropic dry etching process for submicrometer silicon gate N channel MOS technology has been developed. Reactive ion etching was used for Si_3N_4 , polysilicon and phosphosilicate glass (PSG). Aluminum was plasma etched. The process includes tapered etching of contact holes in PSG and planarization of PSG to improve step coverage of metallization and to facilitate aluminum etching.

MOS devices with gate length as small as $0.6 \mu\text{m}$ have been successfully fabricated with this process.

1. Introduction. — The developments towards higher complexity of integrated circuits have been achieved by progressive reduction in size of the devices. For future increase in integration density, one micron and even submicron geometries will be needed. Besides the lithography techniques, capable of producing features in the one micron range with high yield, the etching of the different layers, with precise linewidth control, is the most important problem to be solved. Only anisotropic dry etching techniques can provide the desired dimensional control for future technologies. In addition to this requirement, any etching process must also have adequate selectivity. That is, the film etch rate must exceed mask and substrate etch rates by an acceptable amount determined by process conditions.

In this paper, we will present a complete anisotropic dry etching process for silicon gate N channel MOS fabrication. Besides the required anisotropy and selectivity for submicron technologies, this process includes tapered etching [1] of contact holes in PSG and surface leveling or planarization of PSG [2] with the purpose of providing smooth surfaces to improve step coverage of metallization, and to facilitate resist patterning and etching at the metallization level.

2. Process description. — The complete process is given in table I and is illustrated in figure 1. It is a

Table I

PROCESS DESCRIPTION
Silicon wafers: Ø 3" p type <100> 6 - 8 ohm.cm Thermal oxidation 70 nm Si_3N_4 deposition 80 nm Masking level 1 (active area definition).
Si_3N_4 etching (RIE)
Boron implantation 2×10^{12} 140 Kev Field oxidation 600 nm Si_3N_4 and 70 nm SiO_2 removal Gate oxidation 40 nm Boron implantation (channel) Polysilicon deposition 400 nm Masking level 2 (gate oxidation).
Polysilicon etching (RIE)
Arsenic implantation (source, drain) 5×10^{15} 130 Kev PSG deposition 800 nm Anneal PSG reflow Masking level 3 (contact holes).
PSG tapered etching and planarization (RIE)
Al deposition 1000 nm (interconnexions) Masking level 4.
Al etching (plasma)

PROCESS DESCRIPTION

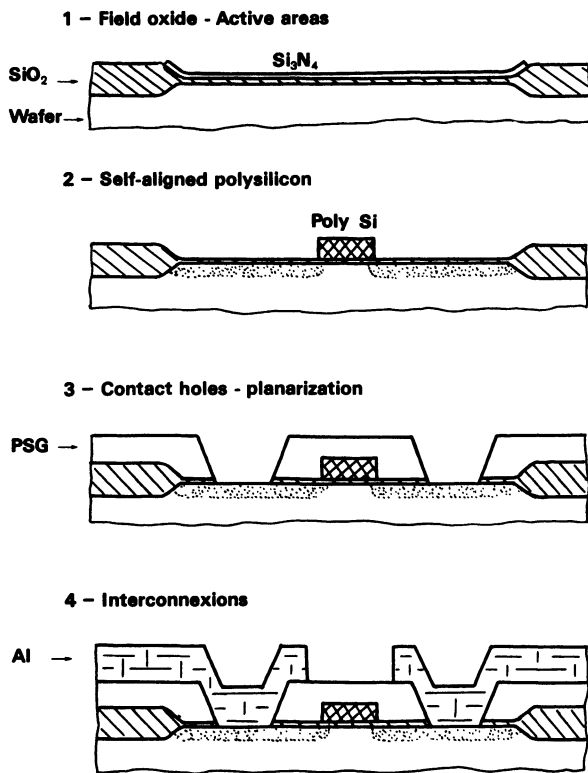


Fig. 1. — Fabrication steps of a silicon gate N channel MOS transistor.

standard LOCOS oxidation silicon gate N channel MOS process. The wafers were masked with Waycoat HPR 204 photoresist. The patterns were defined into the resist using hard contact printing machine (karl Süss MJB 3). The etching of Si_3N_4 , polysilicon and PSG was achieved by reactive ion etching, performed in a commercially available r.f. diode sputter system (DION 300 ALCATEL). The aluminum interconnecting layer was etched in a parallel-plate-plasma reactor built in the laboratory [3].

2.1 SILICON NITRIDE ETCHING. — The thin (80 nm) layer of Si_3N_4 is uniformly deposited onto a flat surface of SiO_2 and no submicron resolution is needed. Therefore, the first etching step is the less critical one. SF_6 was used as an etchant for reactive ion etching of Si_3N_4 . The parameters and results of the etching are given in table II. The corresponding etch profiles are anisotropic. The Si_3N_4 to SiO_2 etch rate ratio is 2 to 1.

2.2 POLYSILICON ETCHING. — This is the most critical step in the whole process. The polysilicon gate etching requires ultimate resolution and therefore no or well controlled undercutting. At the same time, the underlying thin gate oxide calls for high selectivity.

A common approach to anisotropic polysilicon

Table II

Material	Si_3N_4 80 nm	PolySi 400 nm	PSG 600 nm	Al 1 μm
Substrate	SiO_2 70 nm	SiO_2 40 nm	Si; SiPoly 400 nm	SiO_2 600 nm
Etching mode	RIE	RIE	RIE	parallel plates reactor
Gas	SF_6	SF_6	CHF_3	CCl_4
Pressure (mtorr)	10	10	12	200
Power density (W/cm^2)	0,19	0,19	0,4	0,4
Etch rate (nm/min)	85	165	45	90
Selectivity	2	10*	20	10
Uniformity on 3" wafers	3%	5%	1%	5%

* effective selectivity at the end of etching

etching is the use of chlorinated compounds which lead to sidewall recombination of active species avoiding lateral etching [4]. We propose to use SF_6 as an etchant for polysilicon reactive ion etching. The etching can be selective because no recombination process limits the etching reaction as in the case of CF_4 [5]. The polysilicon etch rate in SF_6 is much higher than in CF_4 [6]. It is only limited by the generation rate of active fluorine in the glow discharge.

Reactive ion etching of polysilicon in SF_6 results from the contribution of neutral active species, i.e. fluorine, responsible of isotropic etching and from ion-assisted-chemical etching, responsible of directional etching [6]. To obtain anisotropic etching, it is necessary to reduce the working pressure and thereby enhance the role of ions. As a result, isotropic action of fluorine is reduced. The etching not only becomes more directional but also less selective. Therefore, the optimization of polysilicon gate etching requires a careful balance between these two contributions.

2.2.1 Loading effect and selectivity. — With a SiO_2 cathode, polysilicon etching exhibits a loading effect (Fig. 2) : the etch rate decreases with increasing the area to be etched. Since the SiO_2 etch rate shows no loading effect, the selectivity of polysilicon etching increases with decreasing area. This fact must be taken into account to evaluate selectivity. For example, when polysilicon patterns have to be produced across relief structures, an overetch time is necessary to remove the remaining polysilicon at the steps. This remaining polysilicon has a very small area, so the etching is completed at a maximum etch rate corresponding to A close to zero. The effective selectivity is the ratio of the polysilicon etch rate for $A = 0$ to the SiO_2 etch rate [6].

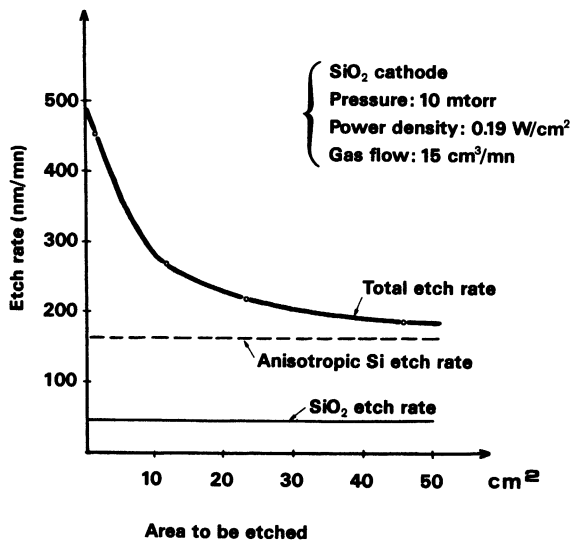


Fig. 2. — Polysilicon etch rate versus area to be etched with a SiO_2 cathode, polysilicon etching exhibits a loading effect.

2.2.2 *Loading effect and anisotropy.* — Besides the loading effect, figure 2, also shows the contribution to the total etch rate of the ion-assisted-chemical etch rate, responsible of directional etching. At

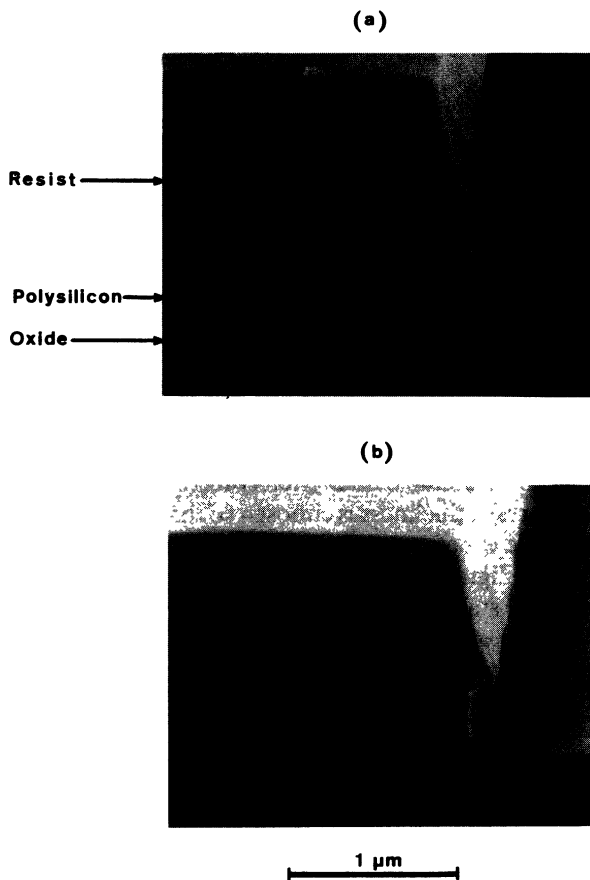


Fig. 3. — SEM micrographs of reactively ion etched polysilicon. Cathode SiO_2 : SF_6 pressure : 10 mtorr. Power density : 0.19 W/cm^2 . Gas flow : $10 \text{ cm}^3/\text{min}$. a) Polysilicon etch time : 2 min. Anisotropic etching. b) Etch time : 3 min. Undercutting appears with an overetch.

10 mtorr pressure, this directional etching is dominant for area greater than 20 cm^2 . Thus, as it is illustrated in figure 3a, the polysilicon etching is quite anisotropic. However, if an overetch time is applied, as illustrated in figure 3b for 1 min. overetch time, undercutting appears. When the etching is complete, the polysilicon area to be etched, area of sidewalls of the etched patterns, is close to zero. So, we are under low loading conditions : a high polysilicon etch rate due to fluorine action leads to undercutting. The previous vertical etch profile moves under the mask, at a rate of 200 nm/min . in our experiment, with no alteration in its shape [6].

2.2.3 *Experimental results.* — Since there are no steep steps after the LOCOS oxidation (Fig. 1), we can obtain anisotropic etching for polysilicon at 10 mtorr working pressure, because no excessive overetch time is required to complete the etching. Figure 4 shows a $0.6 \mu\text{m}$ wide polysilicon gate reactively ion etched using SF_6 at 10 mtorr. The other experimental conditions are summarized in table II. Note that in this experiment 20 s overetch time was applied with no significant undercutting. There is no change in linewidth, the linewidth at the bottom of the etched pattern being equal to the linewidth of the resist at the top of the polysilicon gate (Fig. 4a).

2.3 PHOSPHOSILICATE GLASS (PSG) ETCHING. — Typical parameters for PSG reactive ion etching are given in table II. High selectivity against silicon and perfectly anisotropic etch profiles are obtained [7]. The main problem with this contact hole anisotropic etching comes from the vertical etch profiles which may cause metallization failures. To overcome this problem we propose a new process producing tapered contact holes and a planarized PSG surface before metallization.

2.3.1 *Planarization process.* — Planarization is a dry etching process which suppresses topology variations of PSG layer [2]. Figure 5 illustrates the sequence of the planarization technique. A resist film is coated on the wafer. This film conforms to topology variations and produces a planar surface at the resist top. By etching the structure using conditions that etch the resist and the PSG at the same rate, the flat surface of the resist top is replicated into the PSG. Figure 6 shows the structure during planarization (Fig. 6a) and after the planarization process is complete (Fig. 6b).

2.3.2 *Tapered contact hole.* — Anisotropic etching can lead to tapered etch profile because during etching not only the mask thickness changes due to resist erosion but also its lateral dimension. The etching produces a slope into the resist mask and this slope is transferred into the etched layer via the resist to layer etch rate ratio.

If we have the same etch rate for resist and PSG, as it is the case in the planarization process, the resist profile will be exactly replicated into the PSG layer

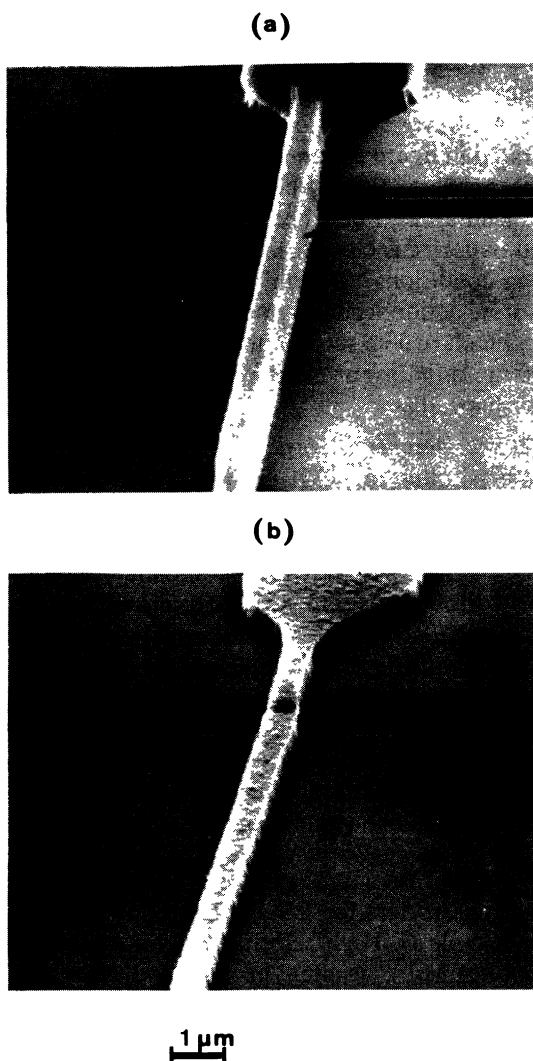


Fig. 4. — SEM micrographs of reactively ion etched MOS transistor polysilicon gates. Cathode $\text{SiO}_2 : \text{SF}_6$ pressure : 10 mtorr. Power density : 0.19 W/cm^2 . Gas flow : $15 \text{ cm}^3/\text{min}$. Etch time : 2 min. 15 (overetch time 20 s). *a*) Sample after etching. 20's overetch time gives rise to insignificant undercutting. *b*) Sample after resist stripping. Gate length : $0.6 \mu\text{m}$.

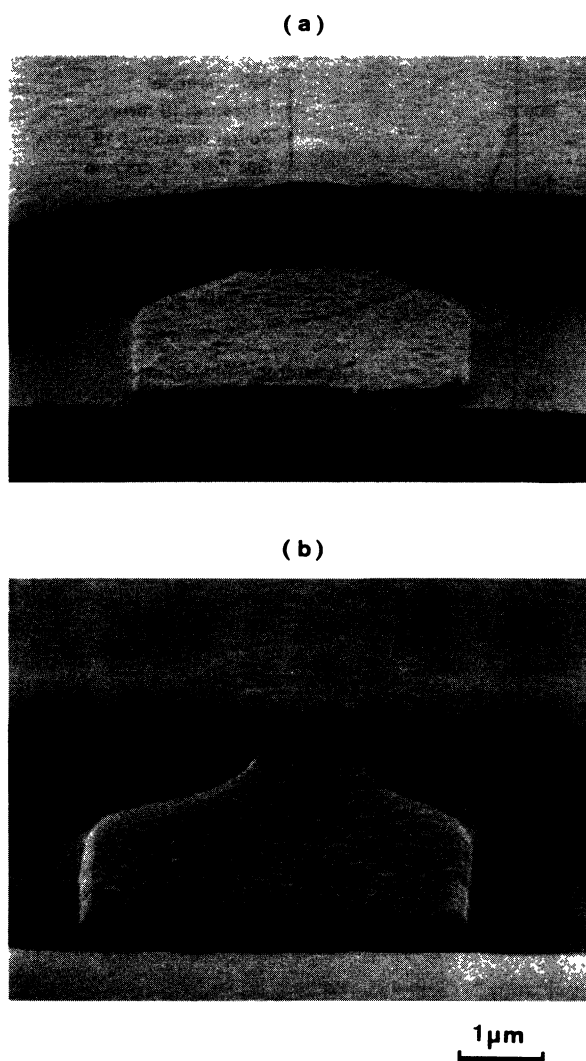


Fig. 6. — SEM micrographs of the planarization process : *a*) During planarization. The top resist is flat. PSG after reflow appears as a wave on the polysilicon gate. *b*) After planarization. The flat resist top has been replicated into PSG.

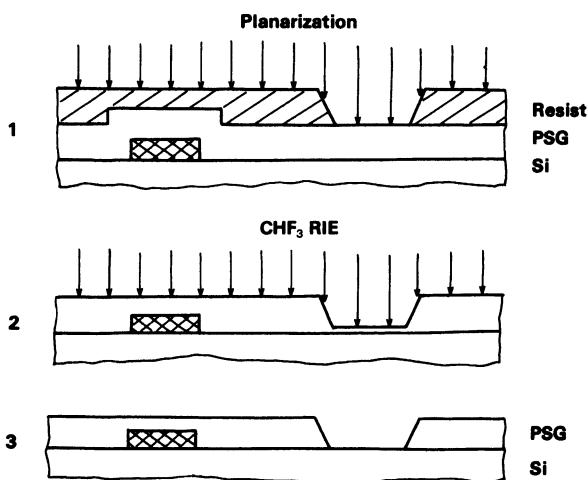


Fig. 5. — Schematic presentation of the various steps required for planarization and tapered contact hole etching.

as shown in figure 7*a*. Figure 7*b* shows the tapered profile of a contact hole after complete etching.

If the resist thickness is chosen so that planarization is complete before the contact holes are opened, as shown in figure 5, the etching can be continued using CHF_3 in standard conditions (see table II) to take advantage of its high selectivity over silicon. Figure 8 displays the resulting MOS structure after planarization and tapered etching of contact holes.

2.4 ALUMINUM ETCHING. — Anisotropic etching of aluminum is performed using CCl_4 as an etchant in a parallel-plate reactor [3]. With reactive gas containing chlorine as CCl_4 the anisotropy results from recombination of radicals and Cl atoms on the sidewalls leading to polymer formation which impede lateral etching [4]. This recombination process occurs at any steep topology variation of the wafer, so that it is extremely difficult to etch the aluminum closest

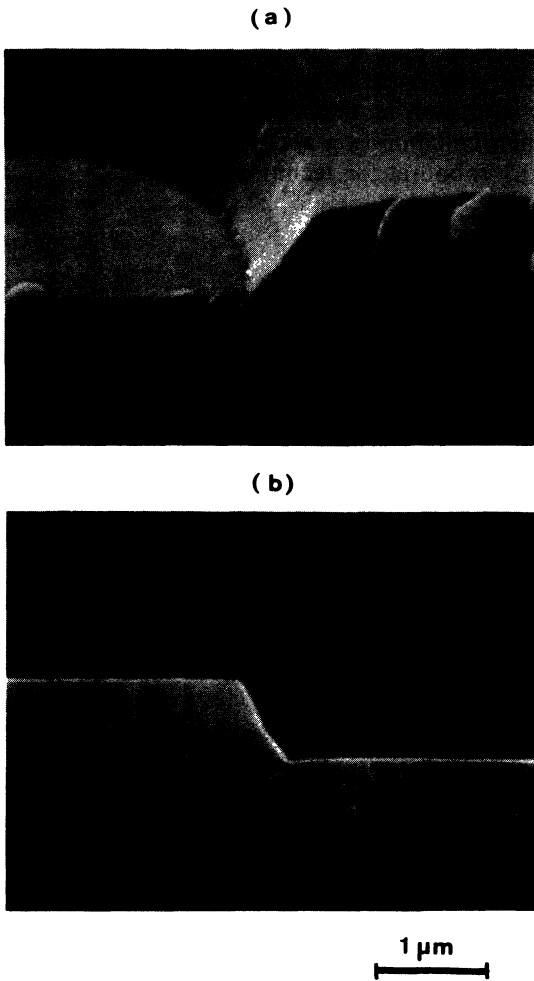


Fig. 7. — SEM micrographs of tapered etching : a) The resist profile is replicated into PSG. b) The tapered profile of a contact hole after complete etching.

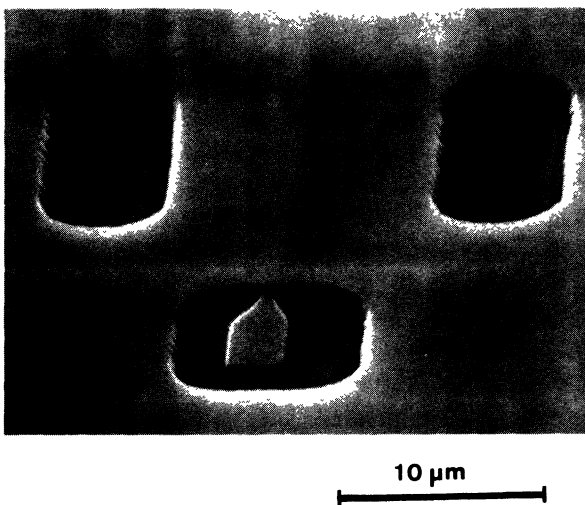


Fig. 8. — SEM micrograph of the MOS structure after planarization and tapered etching of contact holes.

to the step [8]. Since in our process the PSG is planarized, aluminum is deposited on a flat surface. As a result, aluminum etching can be performed with no

problem. The etching conditions and features are summarized in table II. Figure 9 shows the fabricated MOS transistor after aluminum etching.

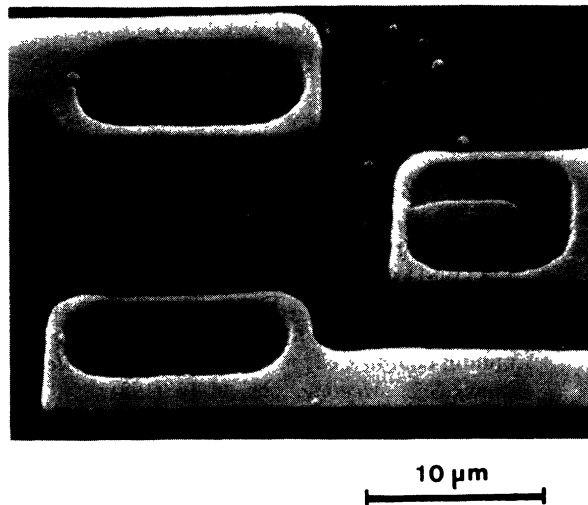


Fig. 9. — SEM micrograph of the MOS device after aluminum etching.

3. Electrical measurements. — The devices fabricated with the described process have different gate lengths down to 0.5 μm. A typical short channel (0.55 μm) $I_D(V_D)$ characteristic is presented on figure 10. The threshold voltage variation as a function of channel length, doping level, bulk and drain voltages are presently investigated for these devices, with the purpose of studying short channel effects in MOS transistor modelling.

4. Conclusion. — We have described a complete anisotropic dry etching process which meets the requirements of submicron N channel technology. That is, precise linewidth control and selectivity especially for polysilicon etching in order to protect the underlying thin gate oxide. Besides these features,

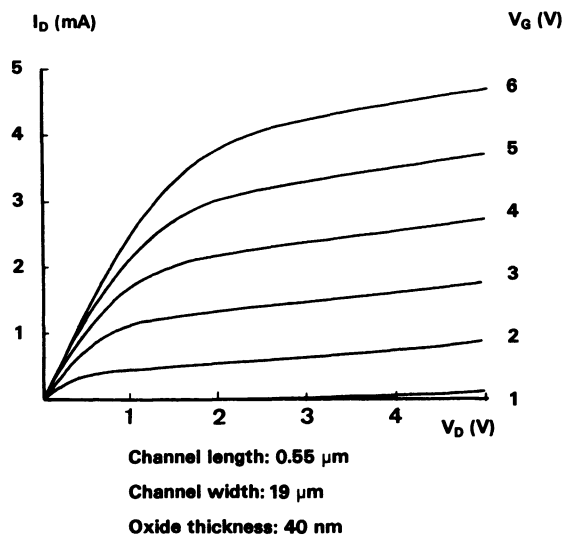


Fig. 10. — MOSFET characteristics $I_D(V_D)$.

the process offers a planarized surface and tapered contact holes. As a result resist patterning and aluminum etching are facilitated. On the other hand, metallization failures due to incomplete metal coverage over PSG steps are drastically reduced giving rise to higher reliability.

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