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SUBSTRATE AND INTERFACE EFFECTS IN GaAs FET'S ⁽¹⁾

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Résumé. — Dans cette communication on décrit l'effet de la polarisation du substrat sur les caractéristiques électriques du transistor à effet de champ à l'arseniure de gallium, réalisé à partir d'une couche N épitaxiée sur substrat semi-isolant compensé au chrome. Une analyse basée sur l'existence d'une double charge d'espace à l'interface semiconducteur-semi-isolant, est proposée et appliquée à la détermination des paramètres de la couche active et des paramètres de l'interface. Les propriétés des caractéristiques de courant de drain aux basses températures et celles de l'admittance de sortie en basses fréquences, sont attribuées à la réponse dynamique de cette double charge d'espace.

Abstract. — In this paper, the experimental results describing the substrate bias effect on the Schottky gate capacitance-voltage and the DC current-voltage characteristics of GaAs FET's (N-type epilayer on semi-insulating Cr-doped substrate) are reported. These results are accounted for by the formation of a double space-charge in the N-layer and in the S.I. substrate in the vicinity of the interface. A theoretical analysis is proposed and appropriate methods for obtaining both the N active layer and the interface parameters (fixed interface charge value, deep centers density in the S.I. GaAs) are shown. The deep level charge effect on the low temperature drain current-drain voltage characteristics, is described.

Introduction. — In gallium arsenide Schottky barrier field-effect transistors, made from N-type epilayer on semi-insulating substrate, it is found that the interface characteristics strongly influence the electrical properties : low-frequency drain current relaxation phenomenon, R.F. and noise performances [1]. In this paper, the experimental results describing the substrate bias effect on the Schottky gate capacitance-voltage and the DC current-voltage characteristics will be reported. It will be shown that a space-charge appears in the N-layer in the interface vicinity. Its properties depend on the interface parameters, i.e. fixed interface charge, deep centers charge in the S.I. A theoretical analysis of the drain current variations will be proposed and applied to the N active layer (thickness, effective doping concentration, carrier mobility) and interface (fixed interface charge value, deep centers concentration in the S.I.) parameters determination.

1. Experimental results. — The studied structures are made from an N-type Ge-doped GaAs layer of thickness d between 0.2 and 0.5 μm . This epilayer

is obtained by a low pressure organo-metallic compounds cracking [2] directly on Cr-doped semi-insulating substrate of thickness D equal to 400 μm . The Schottky gate ($L = 1 \mu\text{m}$ or 50 μm , $Z = 300 \mu\text{m}$) is made from an Au-Pt-Ti metallization. The lateral Au-Ge alloyed ohmic contacts are the source and the drain electrodes and, the ohmic contact (Au-Ge) on the S.I. bottom is called the substrate electrode (Fig. 1).

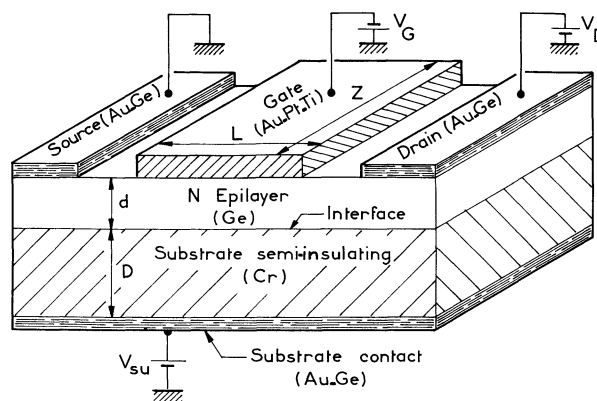


FIG. 1. — Configuration of the device. Definition of the bias voltages.

⁽¹⁾ Preliminary results concerning this communication have been previously accepted for publication (in French) in the Revue de Physique Appliquée.

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1.1 CAPACITANCE-VOLTAGE CHARACTERISTICS. — At given substrate bias V_{su} , the characteristic (Fig. 2) is clearly defined in three parts : (i) a slow variation for $0 < V_G < V_{TC}$, (ii) an abrupt decrease between V_{TC} and V_C , (iii) a third region where the capacitance tends towards the null value. The characteristic translates with a change of V_{su} . Thus, the variations of the quantity $-\frac{C^{*3}}{q\epsilon_0\epsilon_s}\left(\frac{\partial C^*}{\partial V_G}\right)^{-1}$ as a function of $\frac{\epsilon_0\epsilon_s}{C^*}$, usually identified to the donor distribution, where C^* is the capacitance by area unit, will also translate and strongly depend on the substrate bias.

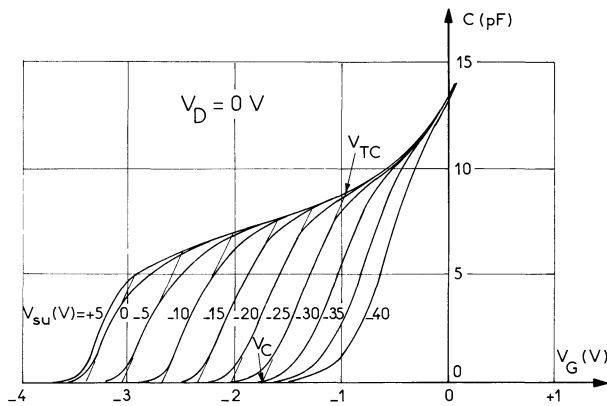


FIG. 2. — Experimental variations of the Schottky gate- (source drain) capacitance as a function of the gate voltage. Substrate voltage as parameter.

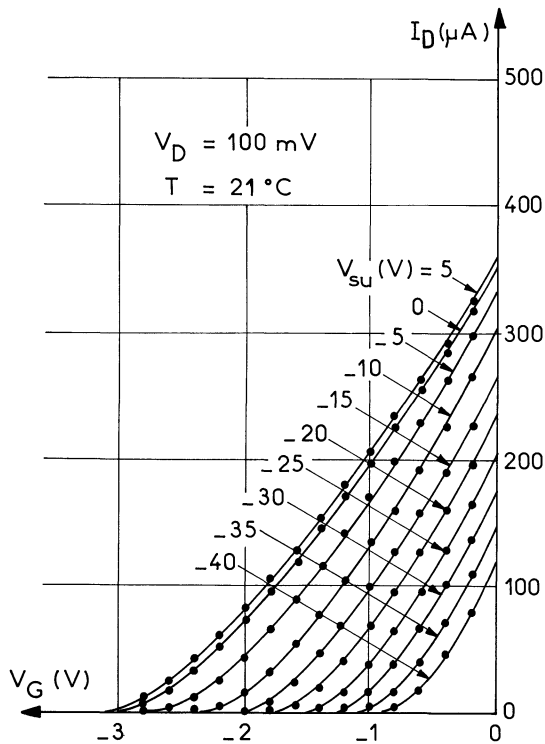


FIG. 3. — Experimental variations of the DC drain current as a function of the gate voltage. Substrate voltage as parameter.

1.2 CURRENT-VOLTAGE CHARACTERISTICS. — The drain current-gate voltage characteristic (Fig. 3), as a function of the substrate bias, translates vertically. At fixed gate bias V_G , the drain current I_D (Fig. 4) decreases only when the substrate bias is lower than a negative threshold value noted V_{SUL} .

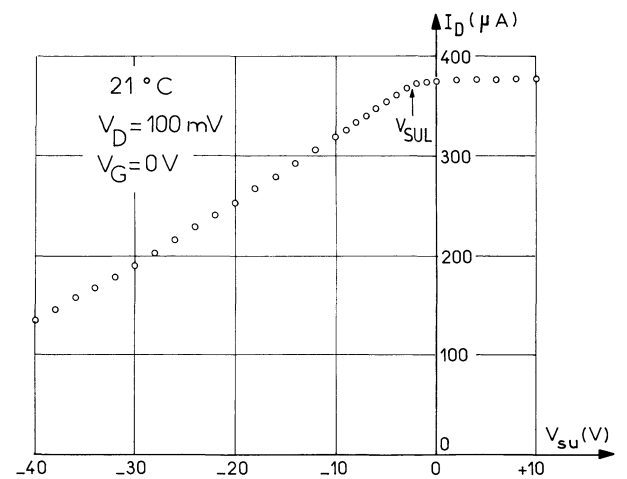
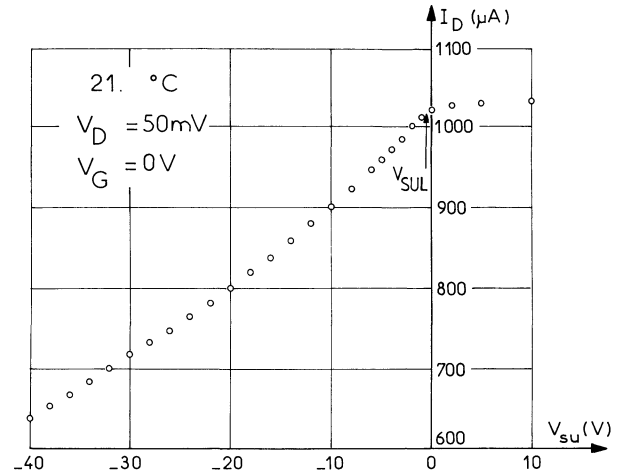


FIG. 4. — Experimental variations of the DC drain current as a function of the substrate voltage. 4.1 : Structure T317 N° 2 ($L = 1 \mu m$). 4.2 : Structure T317 N° 3 ($L = 50 \mu m$).

2. Analysis of the results. — From the observed experimental properties and published former studies [3-6], the retained mechanisms are : (i) a depleted space-charge of width W under the gate electrode, (ii) a fixed positive charge σ_{ss} at the semiconductor-semi-insulating interface, similar to that observed in the semiconductor-insulating interface, (iii) at both sides of the interface may exist two space-charges, the negative one in the S.I. is related to a deep centers density N_t , whose energy level is several kT above the Fermi level and, the positive one in the semiconductor to the donor density N_D .

The energy level diagrams and the charges distributions are : (i) $V_{su} > 0$: the structure behaves as a semiconductor-insulating structure, (ii) $V_{su} = 0$: there is a negative charge build-up in the S.I., (iii) $V_{su} = V_{SUL}$, the energy levels in the semiconductor become flat in the interface vicinity, (iv) $V_{su} < V_{SUL}$: there is a double space-charge build-up : a positive one in the semiconductor and a negative one in the S.I. (Fig. 5). Thus the effective channel conduction thickness is reduced to $d - (W + x_d)$.

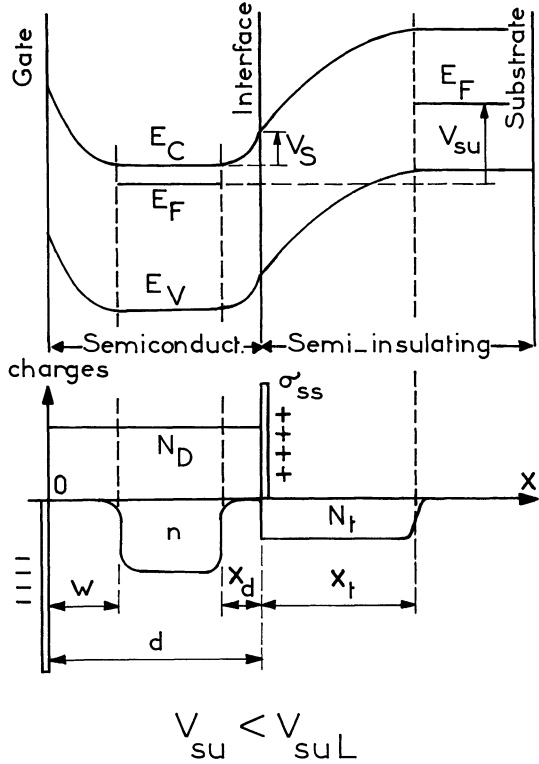


FIG. 5. — Band diagram and charge distribution in a cross-section of the structure.

In this case, the gate threshold voltage V_T , defined by the existence of a single point of the semiconductor showing a carrier density n equal N_D , is :

$$V_T = V_{bi} - \frac{qN_D}{2\epsilon_0\epsilon_s} \times \left[d - \left(\sqrt{\frac{2\epsilon_0\epsilon_s}{qN_D} \frac{N_t}{N_D} (\phi_D - V_{su}) - \frac{\sigma_{ss}}{qN_D}} \right)^2 \right] \quad (1)$$

where V_{bi} and ϕ_D are respectively the gate — N layer and the N layer — S.I. built-in potentials.

The drain current at low drain voltage V_D , for the ranges $V_{su} \leq V_{SUL}$ and $V_T \leq V_G \leq V_{bi}$, in the hypothesis of an abrupt space charge-electrically neutral channel boundary, is :

$$I_D |_{V_D \rightarrow 0} = qN_D \mu_0 \frac{Zd}{L} \times$$

$$\times V_D \left[1 - \frac{1}{d} \left(\sqrt{\frac{2\epsilon_0\epsilon_s}{qN_D} \frac{N_t}{N_D} (\phi_D - V_{su}) - \frac{\sigma_{ss}}{qN_D}} \right) \right] \times \left[1 - \sqrt{\frac{V_{bi} - V_G}{V_{bi} - V_T}} \right] \quad (2)$$

In the cases (i, ii, iii), this relation is reduced to ($V_{TL} \leq V_G \leq V_{bi}$) :

$$I_{DL} |_{V_D \rightarrow 0} = qN_D \mu_0 \frac{Zd}{L} V_D \left[1 - \sqrt{\frac{V_{bi} - V_G}{V_{bi} - V_T}} \right] \quad (3)$$

with

$$V_{TL} = V_{bi} - \frac{qN_D d^2}{2\epsilon_0\epsilon_s} \quad (4)$$

In the four cases, the gate capacitance expression ($V_G > V_{TL}$ or $V_G > V_T$) is :

$$C = ZL \sqrt{\frac{q\epsilon_0\epsilon_s N_D}{2(V_{bi} - V_G)}} \quad (5)$$

3. Application to the determination of the parameters. —

(i) The built-in potential V_{bi} and the donor concentration N_D are deduced from the variations of $1/C^2$ as a function of V_G , for $V_G > V_{TL}$ or $V_G > V_T$.

(ii) The variations of I_D as a function of $\sqrt{V_{bi} - V_G}$, for a given value V_{su} , is linear with a slope equal to $k\mu_0\sqrt{N_D}$ and a X axis intersection equal to $\sqrt{V_{bi} - V_T}$.

(iii) The variations of the quantity $\sqrt{V_{bi} - V_T}$ as a function of $\sqrt{\phi_D - V_{su}}$ (Fig. 6) present two linear regions and give the quantities

$$\sqrt{\frac{N_t}{N_D}}, \quad \frac{qN_D d^2}{2\epsilon_0\epsilon_s}, \quad \frac{\sigma_{ss}}{\sqrt{2qN_D\epsilon_0\epsilon_s}}$$

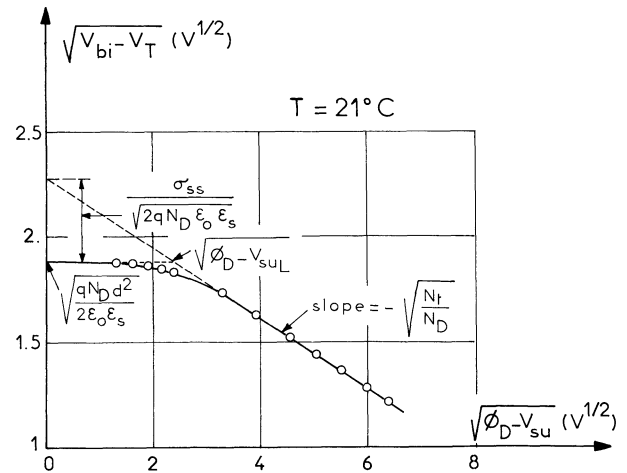


FIG. 6. — Experimental variations of the square-root of $(V_{bi} - V_T)$ as a function of the square-root of $(\phi_D - V_{su})$. Application to the parameters determination. Structure T317 N° 2 ($L = 50 \mu\text{m}$).

An example of the parameters values calculated from these quantities (Thomson CSF 310-6 layer) is : $N_D = 7.6 \times 10^{16} \text{ cm}^{-3}$, $V_{bi} = 0.75 \text{ V}$, $d = 0.25 \mu\text{m}$, $\mu_0 = 3900 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{S}^{-1}$, $N_t = 1.9 \times 10^{15} \text{ cm}^{-3}$, $\sigma_{ss} = 6 \times 10^{-4} \text{ cb} \cdot \text{cm}^{-2}$.

4. Effects on the FET electrical characteristics. — The time response of the space-charge in the S.I. is responsible for the low-frequency output admittance relaxation phenomenon [7]. One of the most important

effects of this space-charge is the current-voltage characteristic looping and bumping. An example, at nitrogen liquid temperature, is given (Fig. 7.1). The curve 1 corresponds to the first drain voltage increase and to the build-up of the space-charge in the S.I. and its image space-charge in the semiconductor. The frozen space-charge acts as a fixed charge and controls the following increasing and decreasing drain voltage characteristics (curves 2 and 3). These effects are greatly reduced in FET with a high-resistivity buffer layer [8] (Fig. 7.2). But, due to leakage in the buffer layer, these FETs present high subthreshold current [9] (Fig. 8).

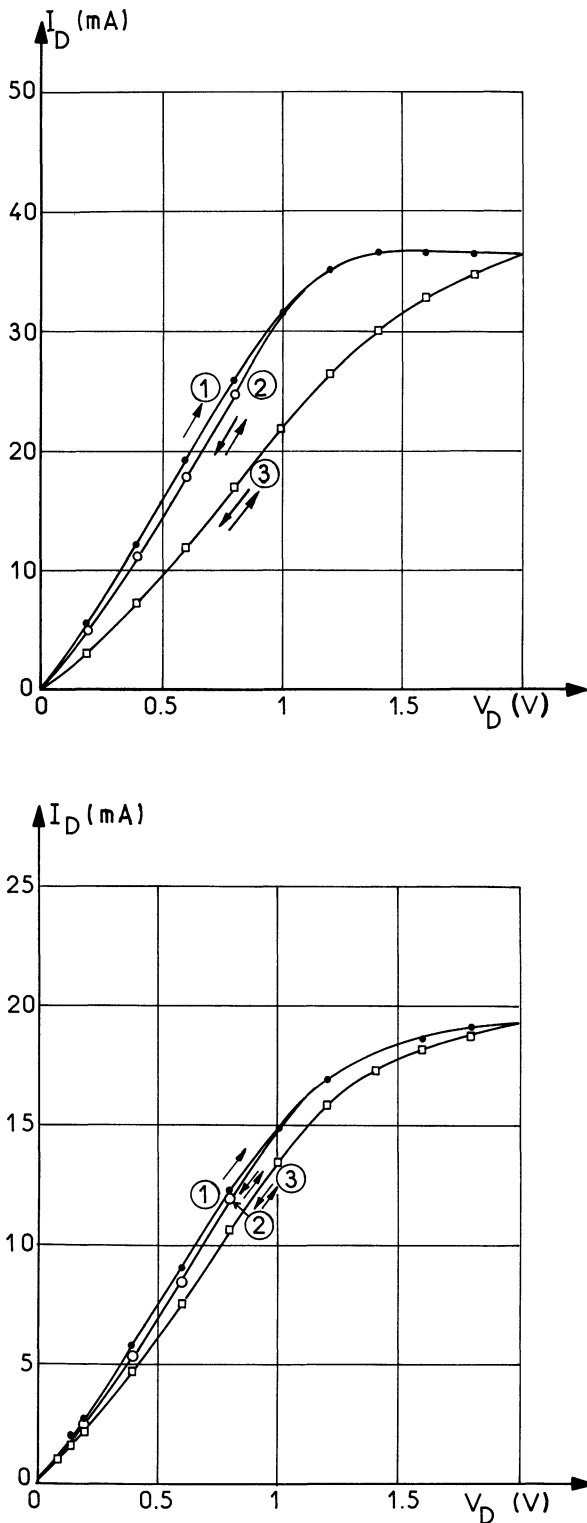


FIG. 7. — Low temperature DC drain current as a function of the drain voltage $T_a = -196\text{ }^\circ\text{C}$. 1 : initial drain voltage increase; 2, 3 : two following decrease and increase of drain voltage (depending on V_D max reached during 1) 7.1 : Unbuffered device. 7.2 : Buffered device.

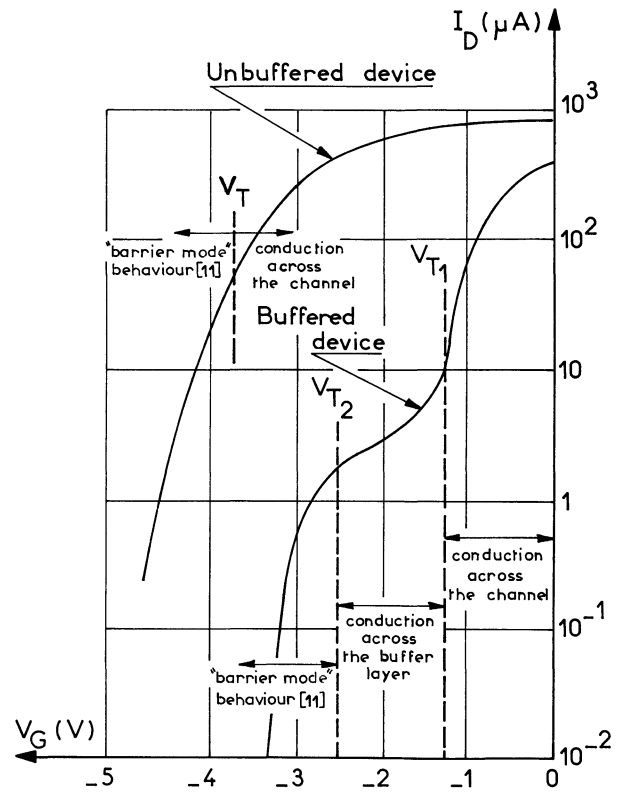


FIG. 8. — Classical and subthreshold drain currents in a buffered and an unbuffered devices showing the current leakage effect through the buffer layer.

Thus, though the multi-layer technology improves the RF performances, it must be forbidden in high-speed switching logic circuits which need good blocking characteristics.

5. Conclusion. — A way to determine the parameters of N^+ epilayer on semi-insulating substrate is proposed. It consists in a substrate bias which acts on the electrostatic configuration of the semiconductor-semi-insulating interface. The physical origin of the deep centers N_t and the interface charge σ_{SS} are unknown though these deep centers are related to chromium [10]. The current-voltage characteristic looping and the low-frequency relaxation phenomenon are finally related to the semi-insulating space-charge.

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