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TRAP CHARACTERIZATION IN S. O. S. - M. O. S. TRANSISTORS USING NOISE MEASUREMENTS (*)

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Résumé. — On a mesuré le bruit des transistors M. O. S.-S. O. S. à canal n et p à la température ambiante dans la bande de fréquences 1 kHz-1 MHz. Le comportement du bruit a été relié au dopage de la couche de silicium épitaxié ainsi qu'à l'effet de sa polarisation. Les dispositifs n et p à assez forte concentration d'impuretés montrent des spectres de bruit en $1/f$ tendant vers le niveau thermique théorique en hautes fréquences. Le comportement de ce bruit est dû principalement aux niveaux d'interface Si-SiO_2. Pour les dispositifs à canal p, où la couche de silicium est entièrement déplétée, on obtient des spectres de bruit composés de trois bosses venant se superposer au $1/f$ résiduel. Ces différentes bosses sont associées à trois niveaux de pièges situés dans la zone de déplétion proche de l'interface Si-Saphir. A partir de simples hypothèses tenant compte de la théorie du bruit de Génération-Recombinaison, on trouve des densités de pièges de l'ordre de 10^{11} cm^{-2} pour chacun des niveaux. Ces mesures de bruit corrélées aux mesures de tension de seuil confirment la déplétion complète de la couche de silicium.

Abstract. — The noise of n- and p-channel S. O. S.-M. O. S. transistors has been measured at room temperature in the range of 1 kHz-1 MHz. Its behaviour has been related to the doping of the silicon film and to the effect of the bulk silicon layer bias. n-channel devices and p-channel ones, with a high enough doping concentration, exhibit $1/f$ noise which tends to the theoretical thermal level at higher frequencies. This noise is thought to be due to the Si-SiO_2 interface levels. p-channel devices with a fully depleted silicon film present bumps in the noise spectra which are superposed on a $1/f$ background. They are associated with three different levels in the depletion zone and also near the lower interface. Making simple assumptions in the theory of G. R. noise in M. O. S. transistors, a density of traps of about 10^{11} cm^{-2} for each level has been found. These noise measurements have been made in connection with threshold voltage measurement, the variation of which confirms the complete depletion of the silicon film.

1. **Introduction.** — The purpose of this work is the investigation of the influence of the silicon-sapphire interface on the behaviour of the noise of Silicon-On-Sapphire M. O. S. transistors.

The experimental results (which include threshold voltage measurements) have pointed out the important role played by the bias of the silicon bulk.

2. **Description of the device.** — The transistors have been provided by LETI-MEA (C. E. N. Grenoble). They are designed on insulating substrates from Union Carbide and Inselek. They are represented on figure 1.

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The same mask has been used for the three kinds of transistors. Both n- and p-inversion-channel transistors have been studied. The dimensions of these devices are given on figure 1. The transistors have been labelled in the following mode :

i) p-channel with
$N_D = 2$ to 5×10^{15} cm^{-3} → transistor S_1 ;
ii) p-channel with
$N_D = 1$ to 2×10^{16} cm^{-3} → transistor S_2 ;
iii) n-channel with
$N_A = 5 \times 10^{15}$ to 10^{16} cm^{-3} → transistor S_3 .

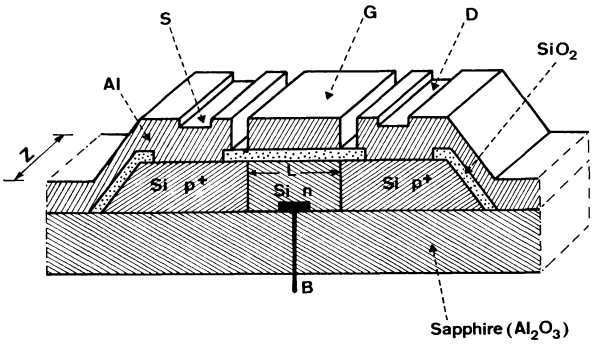

FIG. 1. — Description of the p-channel inversion-type S. O. S. transistors.

d_{ox} ≃ 0.1 µm	
d_{si} ≃ 0.8 µm	p-Channel N_D : 2—5 × 10^{15} cm^{-3} « S_1 »
$d_{Al_2O_3}$ ≃ 250 µm	p-Channel N_D : 1—2 × 10^{16} cm^{-3} « S_2 »
Z/L = 16/8	n-Channel N_A : 5 × 10^{15}—10^{16} cm^{-3} « S_3 »

The substrates of the transistors S_1 and S_2 were provided by Union Carbide and those of the S_3 transistors by Inselek.

An electric contact on the silicon layer is represented by the letter B on figure 1. This electrode enables one to control the bias of the silicon bulk, this bias is always referred to the source. Furthermore, when this electrode is not used, it is kept grounded to avoid the kink effect on the drain current.

The chosen values for I_D, V_{DS} and V_{GS} keep the transistor in the ohmic regime of the $I_D - V_{DS}$ characteristics : the main advantages of these biasing conditions are a uniform inversion layer and a low channel impedance to make easier measurements of the channel noise current.

3. **Drain characteristics.** — The bulk of the epitaxial silicon layer has been reverse biased with respect to the source. The effect of this bulk-source bias V_{BS} has been studied on bulk silicon M. O. S. transistors : its influence is such that the drain current I_D diminishes when increasing V_{BS}, (V_{GS} being kept constant).

For the three devices, the variation of the threshold voltage has been measured. S_2 and S_3 present a uniform variation of V_T with V_{BS}, whereas V_T in the case of S_1 is made more negative, and saturates. These results are plotted on figure 2 for S_1 and S_2.

This different behaviour can be correlated with the magnitude of the doping concentrations of S_1 and S_2.

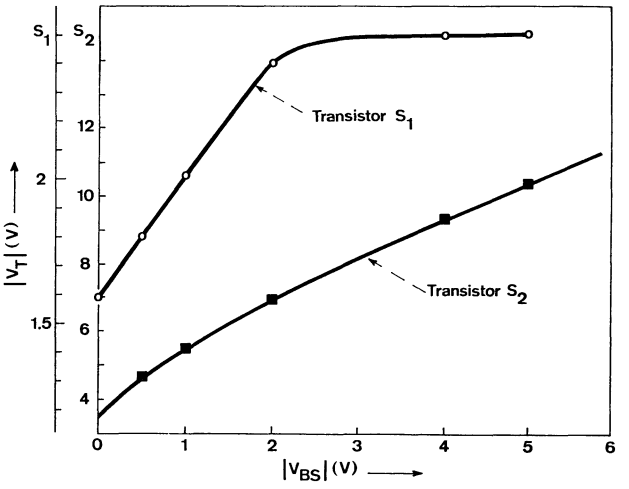

FIG. 2. — Variation of the threshold voltage V_T *vs.* the bulk-source bias V_{BS}.

The value of V_{BS} (of up to 3 volts) applied to S_1 is sufficient to create a depletion layer which extends to the Si-Al_2O_3 interface. Fixed charges included in the sapphire or trapped in interface levels give values of V_T reaching saturation.

When the doping of the epitaxial layer is higher, the saturation may not be observed because the depleted zone cannot reach the lower interface. This is the case in the S_2 devices.

If we assume that most of ΔV_T is due to the fixed charge $Q_{Al_2O_3}$ at the Si-Al_2O_3 interface and in the Al_2O_3 substrate, we can obtain its numerical value. For a ΔV_T of 0.9 V, we find a positive charge $Q_{Al_2O_3} \simeq + 6 \times 10^{10}$ e/cm^2. The values of $Q_{Al_2O_3}$ ranged from 6×10^{10} e/cm^2 to 4×10^{11} e/cm^2 for different devices S_1.

Similar orders of magnitude and sign of this charge are reported in the literature [1], [2]. For the S_3 devices, no saturation of V_T was observed ; this behaviour cannot be explained only by the order of magnitude of the doping concentration, because these devices have been realized on a different substrate (Inselek) and by different technological steps, which may modify the Si-Al_2O_3 interface, and may also compensate or screen the effect of the interface charge.

4. **Results on the channel noise.** — The experimental set-up used in the range of frequencies (1 kHz-1 MHz) is described in figure 3 : a white noise generator is used as a noise standard ; the channel noise current $i_c(t)$ is amplified and filtered by a wave analyzer which performs its spectral analysis.

At the output of the transistor, the noise associated with the drain current was measured. These measurements lead to the spectral intensity of the channel noise current $i_c(t)$. The equivalent noise circuit is represented on figure 3. There, the transistor is reduced to its channel impedance $R_c = \partial I_D/\partial V_{DS}$ in parallel with the drain load resistor R_L.

All noise measurements were made at room tempe-

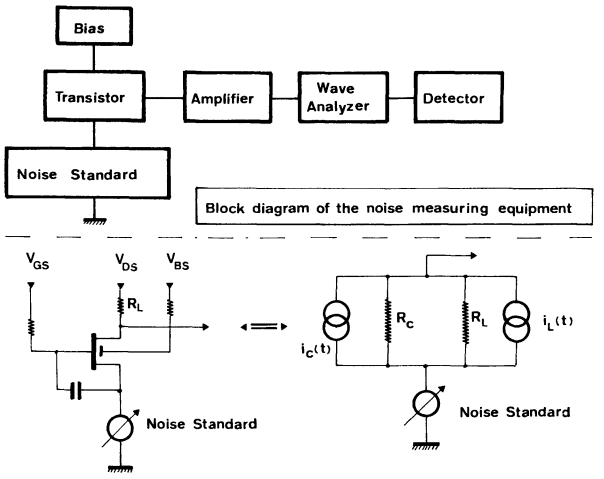

FIG. 3. — Block diagram of the noise measuring equipment and equivalent noise circuit of the transistor.

rature (300 K). Two kinds of curves represent the noise : i) noise spectra $S_i(f)$ *vs.* frequency for several values of V_{BS} ; ii) the spectral intensity $S_i(f)$ *vs.* V_{BS} at several frequencies of analysis.

a) Let us consider first the noise spectra of the n-channel transistor S_3 plotted in figure 4. They exhibit

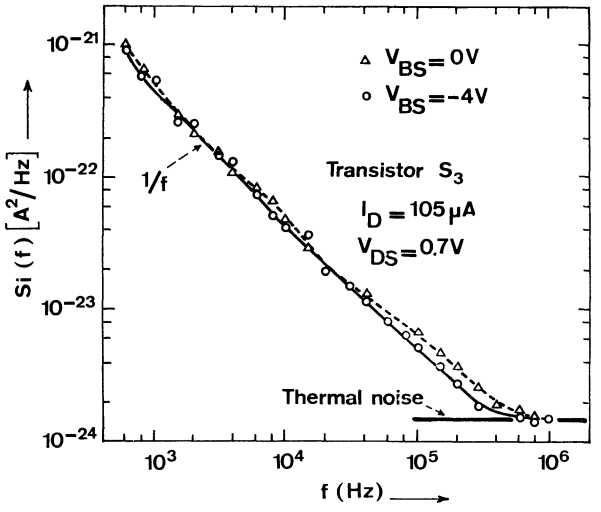

FIG. 4. — Noise spectra of transistor S_3 $\begin{cases} \triangle\ V_{BS} = 0\ \text{V}, \\ \bigcirc\ V_{BS} = -4\ \text{V}. \end{cases}$

a uniform $1/f$ law and tend to the theoretical level of the thermal noise which can be easily calculated in the ohmic regime of the drain characteristics by putting

$$S_i(f) = \gamma\, 4\, kT \frac{\partial I_D}{\partial V_{DS}}, \quad [3], [4]$$

with $\gamma \simeq 1$ as the device is biased with $V_{DS} \to 0$. The calculation results in $S_i(f) = 1.33 \times 10^{-24}$ A²/Hz. There is a good agreement between the experimental values at high frequencies and the calculated level.

The $1/f$ portion of the noise spectrum is due to surface noise caused by the interactions between the channel carriers and the Si-SiO_2 interface levels. This noise has been extensively studied on bulk M. O. S. transistors and is very well known.

No influence of the bulk-source bias V_{BS} was noticed on the $S_i(f)$ level.

The variation of $S_i(f)$ *versus* V_{BS} at frequencies of 800 Hz and 20 kHz is plotted on figure 5 ; it confirms the results of the noise spectra when varying V_{BS}.

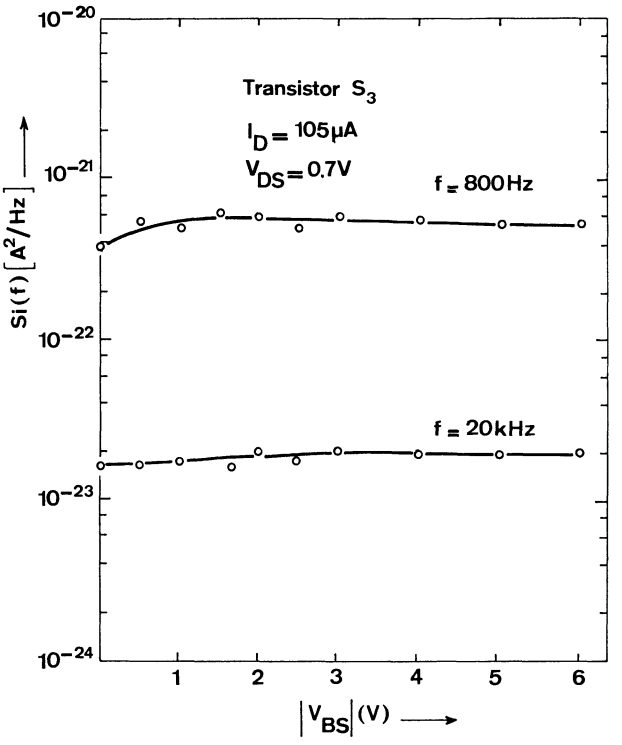

FIG. 5. — Variation of $S_i(f)$ *vs.* V_{BS} for transistor S_3.

Hsu reported elsewhere [5], [6] the presence of G-R mechanisms in n-channel S. O. S.-M. O. S. transistors. We did not verify these results. This is due to the different types and technologies of the tested devices. Indeed the S. O. S.-M. O. S. studied by Hsu present a silicon film completely depleted at $V_{BS} = 0$ V.

b) The noise spectra of S_2 and S_3 are similar. They display a uniform $1/f$ law and no influence of V_{BS}, as is shown on figure 6. This can be correlated with the variation of V_T *vs.* V_{BS} (see figure 2). The doping of the silicon film of S_2 is so high that values of V_{BS} of up to 4 V have little effect on V_T and do not deplete completely the silicon ; so a neutral silicon layer screens the effect of levels near the lower interface.

Only Si-SiO_2 interface levels contribute to that noise.

c) $S_i(f)$ has been plotted *versus* frequency for S_1 (Fig. 7). When keeping $V_{BS} = 0$, the noise follows a $1/f$ law (curve A) and tends to reach the theoretical thermal level (1.2×10^{-24} A²/Hz). The behaviour of this noise can be compared to the one of S_2 and S_3, where the silicon-dioxide interface mainly contributes to the noise. When increasing V_{BS} to 3.5 V a $1/f^2$ slope and bumps appear in the noise spectrum (curve B). This curve has been computed by adding elementary G-R noise components which are defined by a noise spec-

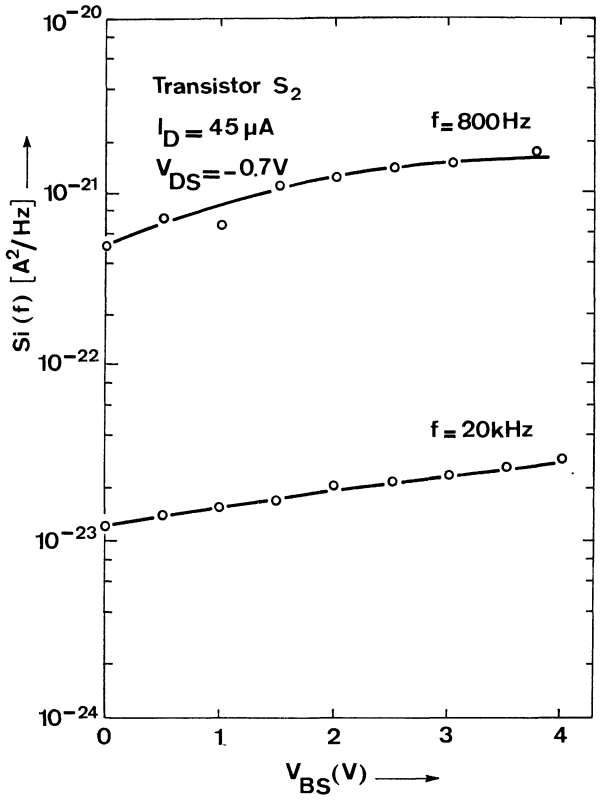

FIG. 6. — Variation of $S_i(f)$ *vs.* V_{BS} for transistor S_2.

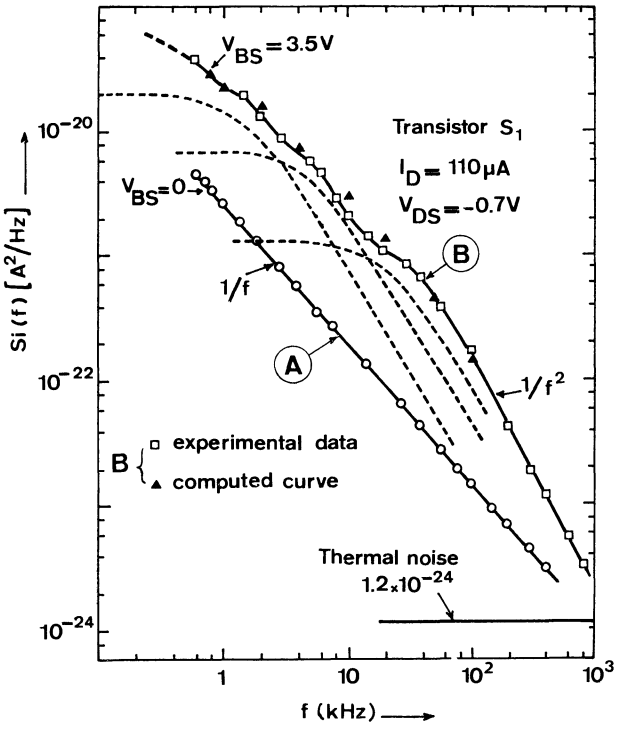

FIG. 7. — Noise spectra of transistor S_1. Curve A : ○ $V_{BS} = 0$.
Curve B : { □ $V_{BS} = 3.5$ V
▲ Superposition of three G-R noise components.

trum $S_i(f)$ proportional to $\tau/(1 + \omega^2 \tau^2)$ where τ is a relaxation time constant and $\omega = 2\pi f$. From the *plateau* level and the roll-off frequency (where the magnitude of the noise is 3 dB below the *plateau*), one can approximate the density N_T of the traps per unit of surface involved in each elementary G-R process, by assuming a uniform spatial distribution through the silicon film in the depletion region. The position of the G-R levels has been determined with a precision of about 20 %.

From the determination of the device transconductance (g_m), the gate geometry (Z, L), the thin oxide capacitance (C_0) and the fractional occupancy of traps (f_t) [the product $f_t(1 - f_t)$ is approximated to 0.25], one can obtain [7], [8] :

$$S_i(f) = \frac{4\,q^2\,g_m^2}{C_0^2\,ZL} N_T\,f_t\,(1 - f_t)\,\frac{\tau}{1 + \omega^2\tau^2}\,.$$

The values obtained for each level are :

$$N_T = 9.8 \times 10^{10}\ \text{cm}^{-2}\,,$$
$$N_T = 1.1 \times 10^{11}\ \text{cm}^{-2}\,,$$
$$N_T = 1.27 \times 10^{11}\ \text{cm}^{-2}\,.$$

These levels are related to the large density of defects in the silicon film near the silicon-sapphire interface. The orders of magnitude found are similar to those reported in the literature [6], [9].

As the value of V_{BS} has been chosen such that V_T saturates (Fig. 2), the silicon film is completely depleted and the depletion layer traps, including the crystal defects near the Si-Al_2O_3 interface, become active. The depleted silicon layer couples electrically the active channel and those levels.

This assumption agrees with the fact that the tran sistor S_2 shows only a $1/f$ noise. For fixed frequencies (800 Hz, 4 kHz, 40 kHz) we have plotted $S_i(f)$ *versus* V_{BS} for the transistor S_1. Around $V_{BS} = 2$ V, an increase is observed in the noise (see figure 8) ; this

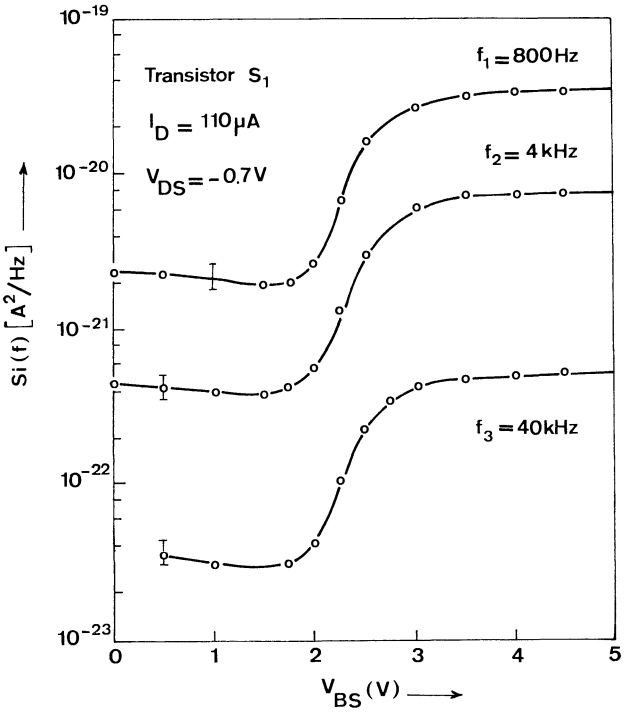

FIG. 8. — Variation of $S_i(f)$ *vs.* V_{BS} for S_1.

happens when the depletion layer reaches the lower interface and when traps become active. The behaviour of this noise is quite similar to that of V_T *vs.* V_{BS}, as can be seen on figure 2.

5. **Conclusion.** — We have shown that noise measurements together with first order measurements (V_T) are a powerful means of characterization of S. O. S. devices. The influence of V_{BS} has been pointed out : the depletion layer caused by this bias is such that trapping levels in this zone may become active, and considerable noise levels are due to trapping. This effect on the noise is thought to be related with the variation of the carrier mobility near the interface, and with the origin of the leakage currents arising from states near the silicon-sapphire interface [10], [11]. Noise measurements *versus* the device temperature will be made : they will bring more informations about the location of the energy levels in the silicon gap and their capture cross sections.

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