



HAL
open science

An application of physical methods to the computer aided design of electronic circuits

P. . Siarry, G. Dreyfus

► **To cite this version:**

P. . Siarry, G. Dreyfus. An application of physical methods to the computer aided design of electronic circuits. Journal de Physique Lettres, 1984, 45 (1), pp.39-48. 10.1051/jphyslet:0198400450103900 . jpa-00232306

HAL Id: jpa-00232306

<https://hal.science/jpa-00232306>

Submitted on 4 Feb 2008

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Classification
Physics Abstracts
05.90 — 85.40

An application of physical methods to the computer aided design of electronic circuits

P. Siarry and G. Dreyfus

Ecole Supérieure de Physique et de Chimie, Laboratoire d'Electronique,
10, rue Vauquelin, 75231 Paris Cedex 05, France

(Reçu le 4 juillet 1983, révisé le 29 septembre, accepté le 4 novembre 1983)

Résumé. — Certaines méthodes et algorithmes utilisés dans les simulations de phénomènes physiques sont appliqués à la conception automatisée des circuits intégrés ou imprimés. Des exemples de résultats obtenus à l'aide de ces algorithmes sont présentés. Ils montrent que l'arrangement des composants et des connexions d'un circuit intégré peut être considéré comme le passage d'un état désordonné à un état partiellement ordonné; cette comparaison conduit à une méthode efficace qui permet d'obtenir un placement optimum des composants et un tracé des connexions.

Abstract. — Methods and algorithms used in simulations of physical phenomena are applied to the automated design of integrated or printed circuits. Representative results, obtained by these algorithms, are presented. They show that the design of the layout of an integrated circuit may be viewed as a transition from a disordered state to a partially ordered state; this comparison leads to an efficient method allowing an optimum placement of the components and a routing of the connections.

1. Introduction.

The design of integrated circuits or of printed circuits is an increasingly difficult task because of the number and complexity of the components. The million-transistor chip being now in view, the availability of efficient computer-aided design tools is of utmost importance. A large amount of work has been devoted to algorithms for designing printed circuit boards or integrated circuits. The problem, however, remains open since no method has proved completely satisfactory [1]. Moreover, the development of powerful integrated chips leads to attempts at building small computers specifically aimed at the C.A.D. of electronic circuits; therefore, algorithms which were satisfactory when running on large, expensive, general-purpose computers turn out to be poorly adapted to smaller machines. Therefore, more research in this area is still needed [2].

Many attempts have already been done for applying the methods developed for the purpose of physics to other fields, such as computer operation [3], optimization [4], neural networks [5], etc... While the manuscript of this paper was being prepared, an analogy between optimization and annealing in solids was published [6], and the idea was applied to the design of large computers.

The basic idea in this paper is the following: the design of an integrated or printed circuit may be viewed as a transition between a completely disordered state and a partially ordered state (Fig. 1). Assume that a circuit is defined by its components, that is, a set of rectangular boxes, and the

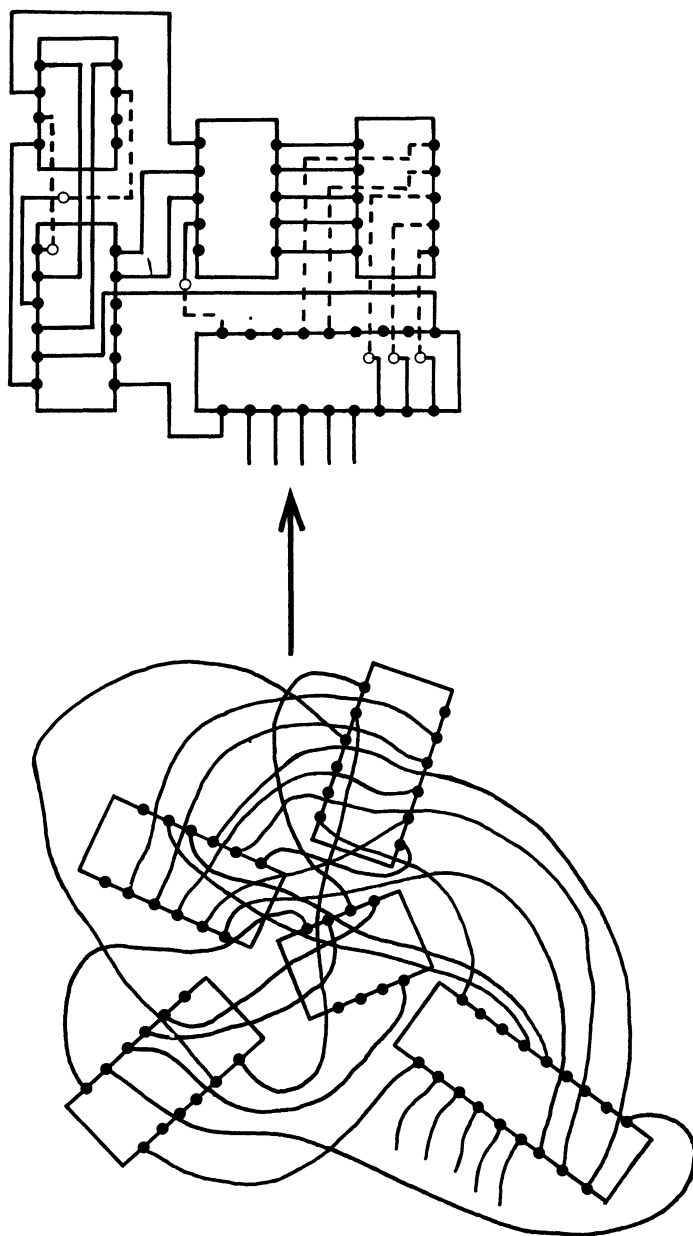


Fig. 1. — The design of an electronic circuit viewed as a disorder-order transformation.

connections between them. Ideally, a C.A.D. program should start from a « liquid of components » and reach an ordered state in which all the elements are arranged regularly with connection paths as simple as possible. Such a transformation occurs spontaneously in many familiar physical or chemical systems. Therefore, the techniques which have been used for many years by physicists to simulate phase transitions on computers can be relevant to some problems occurring in the C.A.D. of integrated or printed circuits. Classically, the design is done in two major phases : first, the components are placed so as to optimize a criterion or a given set of criteria. In a second

step, the connections between the components are routed. In the analogy between C.A.D. and a disorder-order transformation, a global approach seems attractive. However, in view of the complexity of the problem, we have separated the two operations in the first attempt described here ; they will be discussed separately and representative results will be presented. In the design of large systems, an intermediate step, called global wiring, is added. In reference 6, the placement of components and the global wiring are treated by methods of statistical physics ; the real, detailed routing of the connections is not considered. Since we aim at the design of medium-size printed or integrated circuits, we have skipped the global routing step but we have treated the problem of detailed wiring. Therefore, the two approaches are complementary.

2. Placement of components.

The components are to be placed in a plane and connections may be routed on two or more levels. Each component has a fixed set of pins (for discrete components) or of pads (for elements of an integrated circuit), and the designer decides which pin is to be connected to which pin. The connections must be as short and straight as possible. Two electrically independent connections must not cross on the same level. Therefore, the components should be placed in order to allow, in the subsequent routing step, straight, short and simple paths to be designed. Two criteria are generally used : either the total wire length, or the number of wire crossings, must be minimum.

In our approach, components are viewed as particles which interact through the connections. A conformational energy is defined as a linear function of the wire length, or of the crossing count (or of both). Therefore, the transition which will take place in the algorithm will attempt to minimize this energy, just as a natural transition will drive a physical system to a state of minimal energy, or to one of several states of comparably small energies [6].

In analogy with the simulation of physical phenomena, a classical Monte-Carlo method is used, using the Metropolis algorithm [7, 8]. A « temperature » is defined, in the same units as the conformational energy ; starting from a temperature which is high enough to allow the system to evolve, the algorithm drives the system to a stable state when the temperature is lowered. The evolution of the system is allowed by the fact that a new configuration is accepted either if its energy is lower than the previous one, or, with a probability $\exp(-E/T)$, if its energy is higher than the previous one.

The procedure which is used here is similar to that described in reference 6. Starting from a given configuration (chosen, for instance, at random), a new configuration is obtained by exchanging two components labelled n and m . The new energy is computed, and the configuration is accepted or rejected according to the above criterion. A new attempt is made to exchange component $n + 1$ with another component p chosen at random, and the process is repeated. If the number of accepted exchanges reaches a preset limit (depending on the number of components) or if the number of attempted exchanges exceeds a preset limit, the system is considered to be in a stable state at the given temperature ; the temperature of the system is subsequently decreased. The algorithm is terminated when no exchanges are accepted within the above limits. If the starting temperature is zero, the method is identical to classical optimization algorithms ; it yields local energy minima.

Figure 2 shows the effect of the algorithm on a collection of twelve boxes at predetermined locations with $N = 123$ connections. The starting configuration (a) was chosen randomly. The Manhattan length L_i of a wire starting at location (x_1^i, y_1^i) and reaching location (x_2^i, y_2^i) is defined as :

$$L_i = |x_2^i - x_1^i| + |y_2^i - y_1^i|.$$

The energy of the system was defined as the average Manhattan length of all the wires :

$$E = \frac{1}{N} \cdot \sum_{i=1}^N L_i.$$

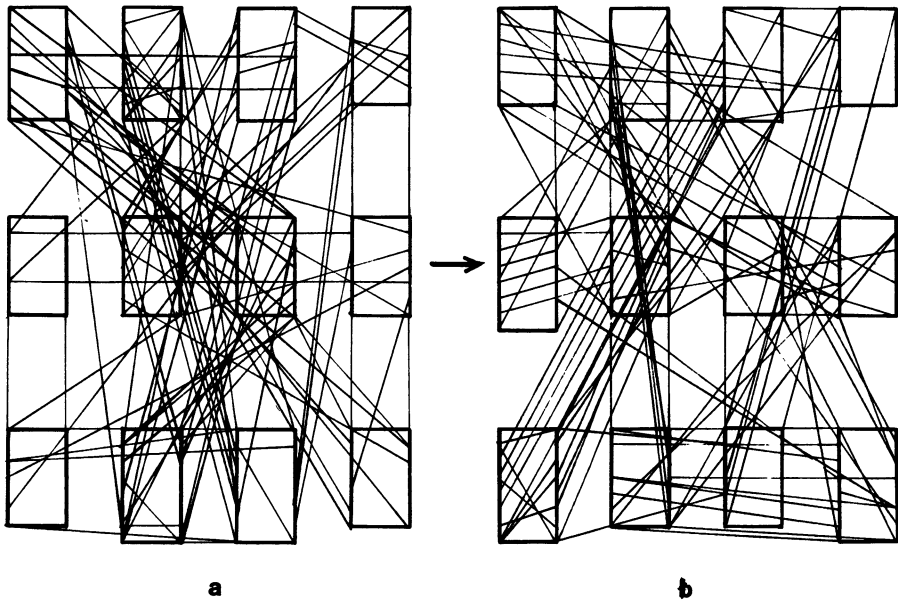


Fig. 2. — Placement of twelve components by minimizing the wire length. *a*) Initial placement (chosen at random). *b*) Final placement.

For clarity, the wires are shown as straight lines, which is, of course, unrealistic, but the length chosen in the algorithm is the Manhattan length, which is the minimum realistic length of a wire. The starting energy was $E = 467$. The final configuration (*b*) has approximately half the initial configuration energy. Obviously, the final circuit is much less congested than the initial one. Therefore, the subsequent wiring step is easier for the final configuration than for the initial one.

The computational effort required is measured by the number of attempted exchanges. In this case, about 2.15×10^4 exchanges were attempted, whereas the total number of possible configurations is approximately 4.8×10^8 . In order to follow the evolution more closely, figure 3 shows the average energy and the minimum energy as a function of temperature. The curves meet at low temperatures, showing that the algorithm reaches a solution. It can be seen that the final state is not exactly the best configuration found. This is the price that we have to pay for not testing all the possible configurations. Since, however, it is very easy to keep in memory the optimal solution found at each temperature, this price is moderate.

As expected, the « heat capacity » of the system is shown on figure 4 to increase sharply as T reaches its final value. The originality of the Metropolis approach, as compared to classical minimization methods, is that exchanges leading to configurations of higher energy are allowed. The ratio of the number of such exchanges to the total number of attempted exchanges is plotted *versus* temperature on figure 5. In a « zero-temperature » method, this ratio would be zero. In the present case, it starts at 0.5, thereby showing that the initial temperature is so high that almost all exchanges are accepted. The ratio drops to zero as the temperature is decreased.

In this example, all circuits are considered to be equivalent, which may not be the case if, for instance, thermal dissipation problems are encountered. In digital electronics, however, such problems tend to disappear with the advent of CMOS technologies. Gate arrays also provide a good example of sets of equivalent cells. The method, therefore, is widely applicable.

It must be pointed out that if the process is started at zero temperature, the final situation is a local minimum with, in this case, an energy of about 300.

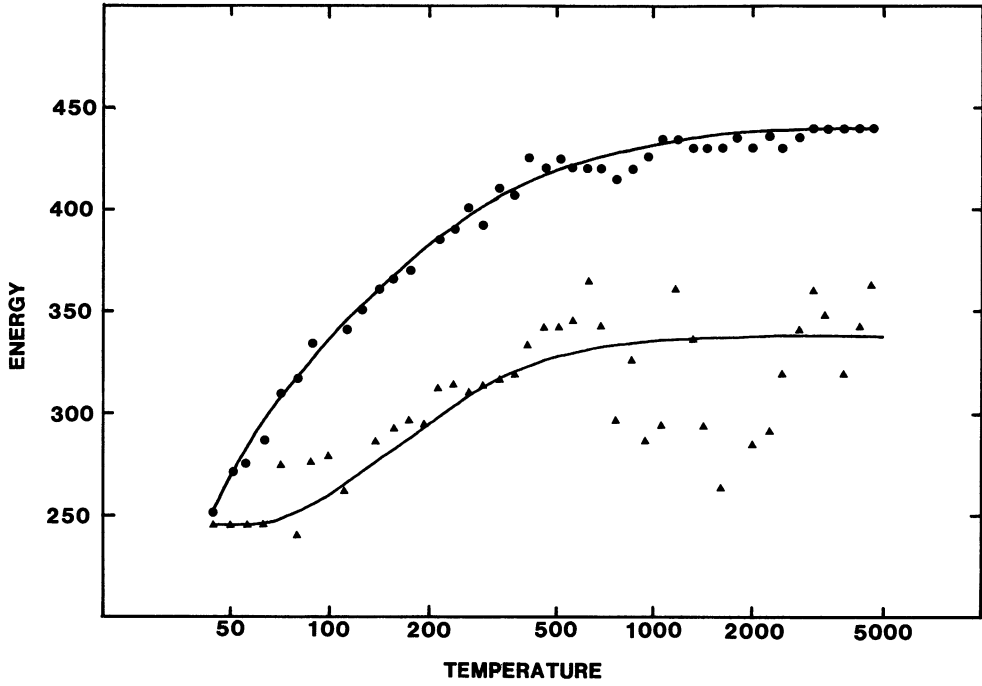


Fig. 3. — Plot of the average energy (dots) and minimum energy (arrows) *versus* temperature.

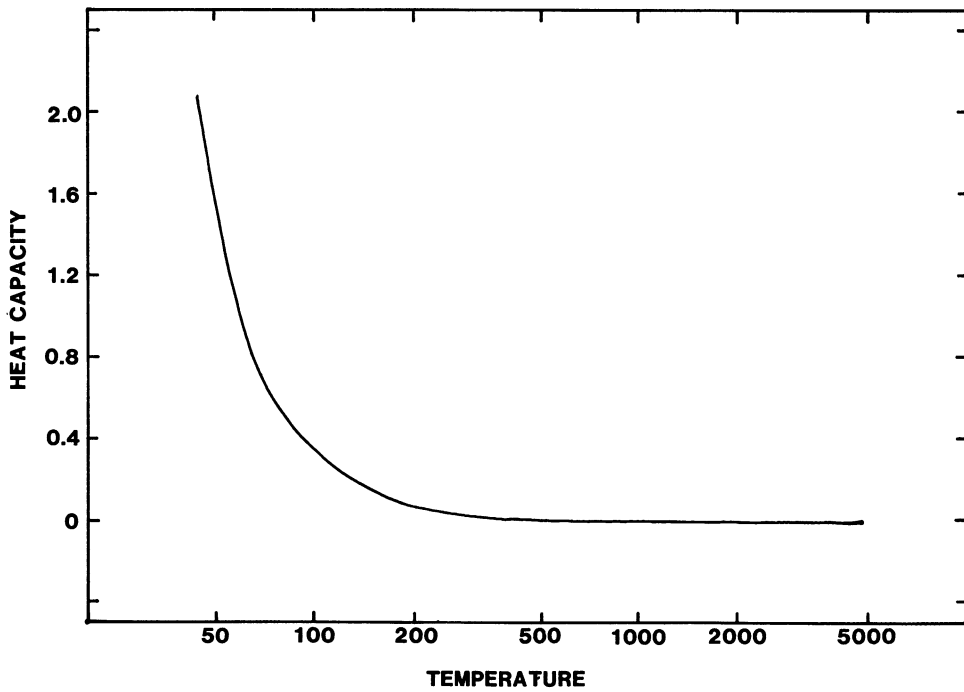


Fig. 4. — Specific heat as a function of temperature.

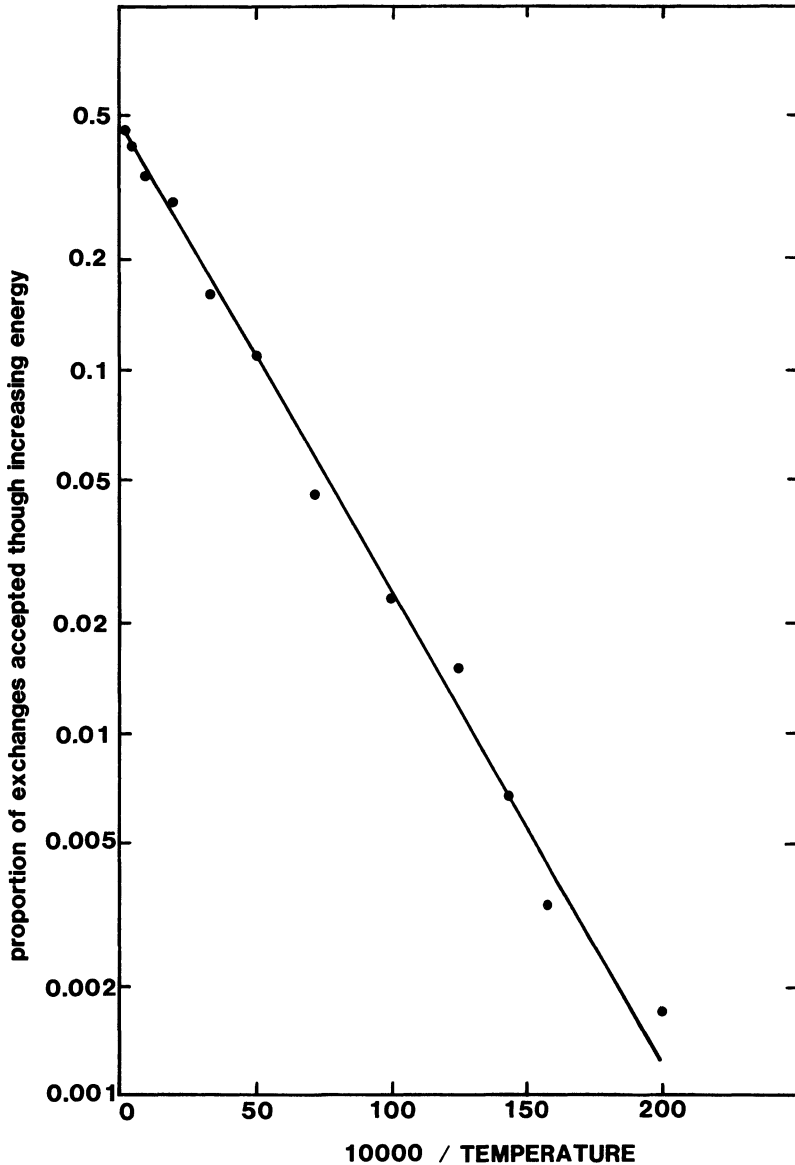


Fig. 5. — Ratio of the amount of accepted configurations leading to an increased energy to the total number of exchanges attempted at each temperature.

In this section, we have shown that it is possible to view the placement problem as a transition from a disordered state to a state of minimum energy when the temperature is decreased. In the example studied here, the interactions between the « particles » are done through the connections which must be as short as possible; the energy could be somewhat improperly termed an elastic energy (the energy chosen in this case was linear with the length instead of quadratic). The method is shown to be more efficient than classical minimization methods because it prevents the system from getting trapped in a local minimum.

3. Routing of connections.

We are now interested in finding the detailed wiring of a printed circuit or of an integrated circuit. Usual routers, such as the Lee algorithm [9, 10], implement connections one by one, in a sequential manner that is apt to crowd certain areas before all connections are completed. Therefore we propose to try to route all connections simultaneously, by treating this problem in analogy with physical systems.

The basic idea is the following : each connection is envisioned as a particle subjected to various attractive or repulsive potentials. For finding its path, it is necessary to define a kind-of « free energy » that we shall endeavour to minimize. To that energy will contribute the « elasticity » of connections (these must be as short as possible), their « rigidity » (we have to minimize the number of elbows and the passages from one side to the other), a repulsive potential at short range between connections, and an attractive potential at long range between a path and its target. It is the competition between all these contributions that will allow to find a configuration of connections.

Practically, we consider the case of double sided printed circuit boards. The algorithm works as follows : the two sides of the board are divided into small squares, the side of which constitute one elementary step in vertical or horizontal direction ; each connection in turn takes one single step forward, so that we may consider that all connections are grown simultaneously. At each step, for choosing among the five possibilities — forward, backward, right, left, through — the program computes the contributions to the potential and adopts the step which gives the lowest resulting potential.

It is clear that the method admits several parameters, the value of which must be chosen heuristically. Therefore, the algorithm was first perfected by connecting only two boxes made up of eight pins. The algorithm was tested by considering more than four hundred examples of circuits comprising eight connections. The results that have been achieved so far are encouraging, since about 97 % of the connections ended without a problem. Two extra parameters were introduced ; first, a repulsive potential between connections running along the same path on both levels : indeed, long superposed wires on different sides of the board must be avoided, because they make easier the building of walls around the targets of connections (which, consequently, cannot come to an end) and, electrically, create capacitance problems ; secondly, a repulsive potential between parts of the same connection, thereby preventing loops to occur.

To illustrate our results, an example of a circuit made up of eight connections routed by our algorithm is presented in figure 6. In order to show the effect of each parameter, we consider the deformation of one of these connections, resulting from the modification of various parameters such as attraction, repulsion and rigidity ; we start in (a) with a predetermined set of values for the parameters.

In figure 6b, a weaker attractive potential is used : the thick connection, weakly attracted by its target, wanders a little before concluding ; in figure 6c, a higher repulsive potential is introduced : the thick connection, highly repelled by other connections and pins, takes a by-way to avoid the overcrowded zone ; if the connections can bend freely in the plane (Fig. 6d) seven bends are observed (instead of four, in the standard case) for the thick connection ; on the other hand, if the connection is very rigid with respect to bending in the plane, the thick connection has no more than three bends (Fig. 6e). In figure 6f, the connections are given a high rigidity with respect to bending perpendicularly to the plane : the thick connection, unwilling to increase the energy by changing its level, does it only when other solutions cannot be obtained. If a high repulsive potential between superposed lines is introduced (Fig. 6g), the thick connection takes a long way round in order to find a zone free on the two sides of the board ; finally, figure 6h shows the situations in which there is no loop repulsion : the thick connection steps backward to its starting point, before starting again forward on the other side of the board. Figure 7 shows an example of a circuit comprising twelve boxes and a hundred and thirty connections (it is approximately the same example as that used for studying the optimal placement of components). The computation time,

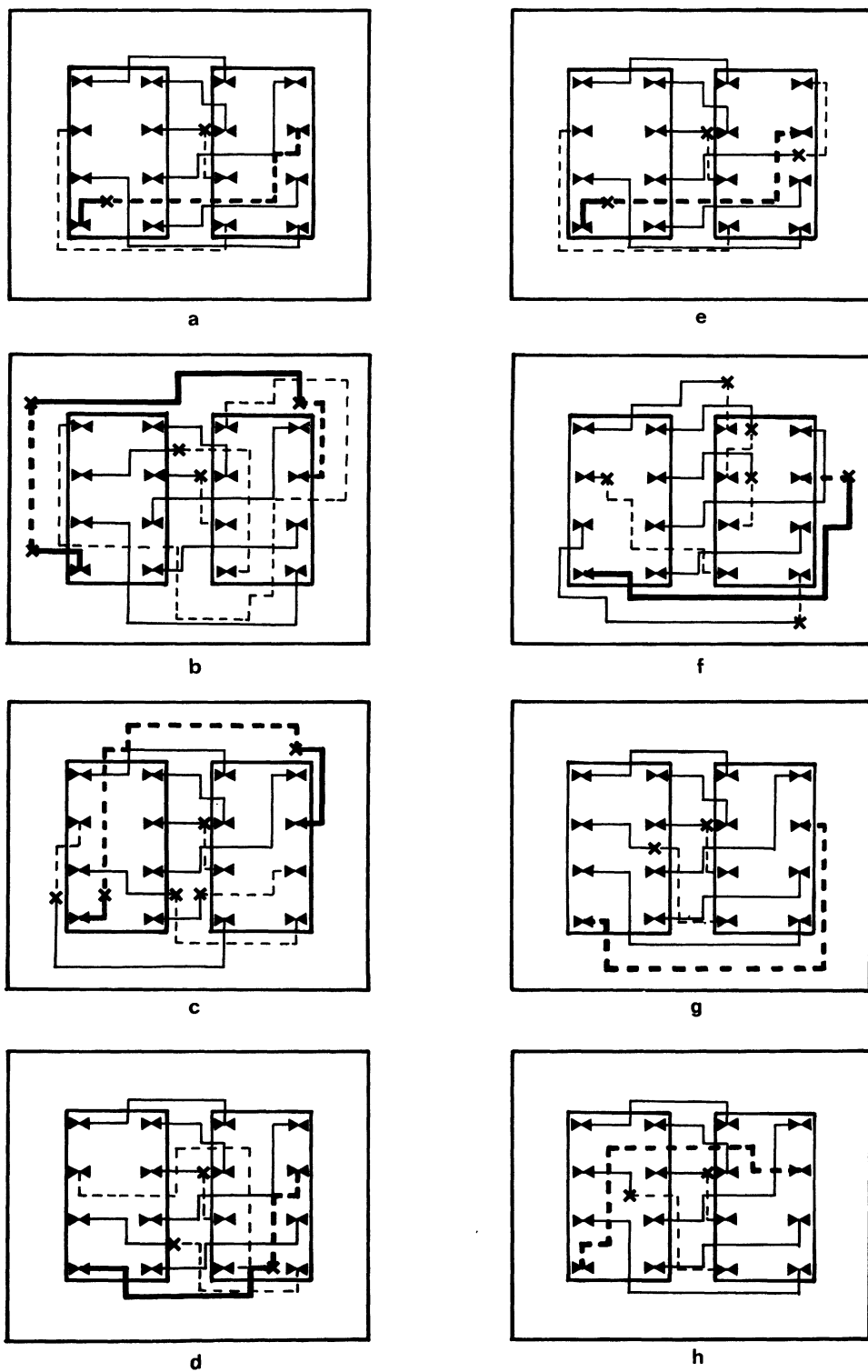


Fig. 6. — Various connection styles corresponding to various values of the potentials and of the rigidity of the connections.

with a IBM 370 computer, is about forty seconds; no intervention is necessary once the list of the connections has been given.

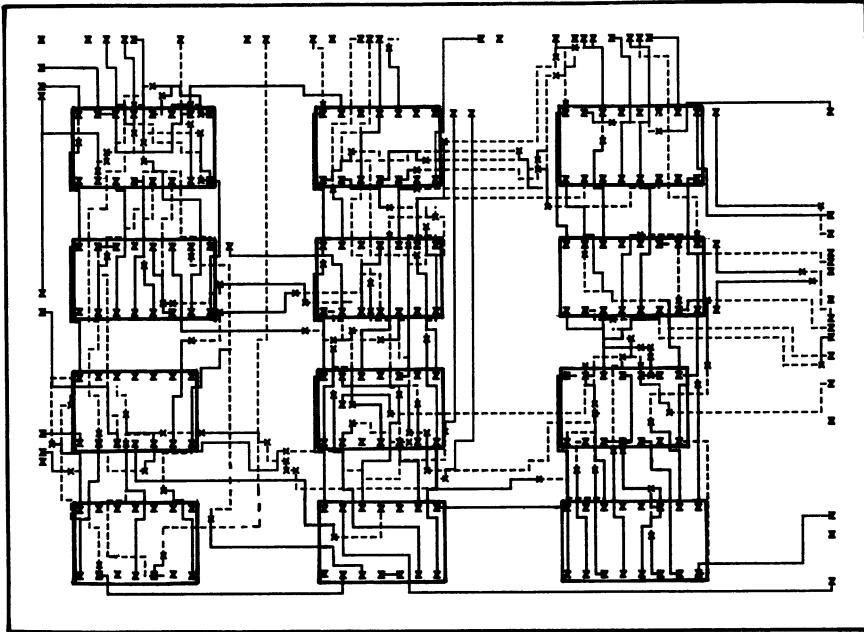


Fig. 7. — Routing of a circuit with twelve components (130 connections).

4. Conclusion.

In this paper, physical methods have been used to carry out the design of electronic circuits, such as printed boards or custom integrated circuits. Considering C.A.D. as a transition from a disordered state to a partially ordered state, it has been shown that a complete design can be achieved by using a Metropolis algorithm together with an algorithm that grows all connections in parallel and computes the energy of the system. Real examples have been treated by this method and further developments are under way. Although these algorithms can certainly be refined to a considerable extent, the results presented here show the viability of the method.

Acknowledgments.

The authors wish to thank Professor P. G. de Gennes and Professor J. P. Hansen for helpful encouragement and support. They are grateful to P. Audrain and Y. Guern for their efficient assistance in writing the computer programs.

References

- [1] SOUKUP, J., *Proc. IEEE* **69** (1981) 1281.
- [2] HONG, S. J. and NAIR, R., *Proc. IEEE* **71** (1983) 57.
- [3] VOLDMAN, J., MANDELROT, B., HOEVEL, L. W., KNIGHT, J., ROSENFELD, P., *IBM J. Res. Dev.* **27** (1983) 164.

- [4] KIRKPATRICK, S., *Disordered Systems and Localization* (Springer-Verlag) 1981, p. 280.
- [5] HOPFIELD, J. J., *Proc. Natl. Acad. Sci.* **79** (1982) 2554.
- [6] KIRKPATRICK, S., GELATT, C. D. Jr., VECCHI, M. P., *Science* **220** (1983) 671.
- [7] METROPOLIS, N., ROSENBLUTH, A. W., ROSENBLUTH, M. N., TELLER, A. H., TELLER, E., *J. Chem. Phys.* **21** (1953) 1087.
- [8] BINDER, K., *Monte Carlo Methods in Statistical Physics* (Springer-Verlag) 1979, p. 1.
- [9] LEE, C. Y., *IRE Trans. Electron. Comput.* **10** (1961) 346.
- [10] RUBIN, F., *IEEE Trans. Comput.* **23** (1974) 907.
-

Commission paritaire N° 59.024