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Chip verification and failure analysis during the design evaluation of very large scale integrated (VLSI) devices call for highly accurate internal analysis methods. After having characterized the first silicon by automated functional testing, classification and statistical analysis can be carried out: In this way a rough electrical evaluation of the material under investigation can be made. Further clues to a faulty device behavior can only be obtained by internal measurements. Serious malfunctions of circuit blocks and internally traced signals can easily be detected by scanning electron beam operation, making use of the qualitative voltage contrast; several individual modes of operation are known, such as voltage coding, logic-state mapping and frequency tracing and mapping, for example [1]. While electron beam testing is indispensable for nondestructive and nonloading measurements on submicron interconnection lines [2] mechanical probing can be used for waveform measurements on less critical geometries, too [3]. Hot spot detection (liquid crystal thermography) can be a very helpful and also nondestructive analysis tool for localization of defective areas [4]. Areas of high power dissipation on the chip can easily be located, because they appear as black spots when the IC-surface is viewed through crossed polarizers in the optical microscope. In situations where there does not appear to exist a direct link between the occurance of hot spots and the actual defective area, the laser is a powerful tool, solving this problem by subsequent cutting of metallization lines [5]. Additionally defect identification often calls for destructive methods like wet chemical and plasma etching followed by light or SEM inspection.

In an extreme case of **failure analysis** the storage function of a memory device was crippled by systematic defects inside the chip's periphery which could be observed, localized and identified. A further step taken was laser manipulation at the chip level, which restored the chip's functionality [6] The comprehensive analysis strategy used here places a greater emphasis on verifying the failure cause through chip manipulation, resulting in a steeper learning curve during the product development.

Internal measurements on submicron interconnection lines for **chip verification** call for a highly accurate electron-beam tester. The system performance requirements for CMOS circuits in the sub-µm regime are: a 0.1 µm spatial resolution at a low electron acceleration voltage of 1 kV, and a probe current of more than 1 nA, a temporal resolution of approximately 500 ps, and a voltage resolution of about 20 mV. To fulfill these requirements a new electron optical column has been developed in collaboration with Integrated Circuit Testing GmbH [7]. The main feature of a low-aberration compound spectrometer objective lens is the suppression of line-to-line voltage coupling to less than 2 %. Some examples illustrate that the newly developed electron optical column satisfies all the requirements for internal measurements on VLSI circuits.

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