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LPCVD SILICON FOR ACTIVE DEVICES

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Résumé - Dans cet article, nous examinons différentes possibilités offertes par la technique LPCVD pour déposer des couches minces de silicium polycristallin non dopé et dopé bore in-situ sur des substrats amorphes. Deux techniques sont envisagées pour le dépôt de couches minces de silicium non dopé: (i) les couches sont déposées à une température supérieure à 580°C et sont polycristallines. Leur micro-structure qui dépend de la température de dépôt et de la pression de silane, est inhomogène en épaisseur, (ii) les couches sont déposées à une température inférieure à 580°C et sont amorphes. La cristallisation par un recuit thermique à basse température ($T_{\text{recuit}} \leq 600^\circ\text{C}$) de ces couches permet d'obtenir des couches de silicium polycristallin dont la taille de grain peut excéder $0,5 \mu\text{m}$ et qui dépend peu de l'épaisseur. L'addition de diborane ($\text{B}_2\text{H}_6/\text{SiH}_4 = 5 \cdot 10^{-3}$) modifie la micro-structure des couches. La diminution de la pression pendant le dépôt a pour effet d'augmenter l'incorporation du bore et de diminuer la résistivité des couches déposées à 625°C à une valeur limite d'environ $2 \cdot 10^{-3}$ ohm.cm sans recuit. Des Transistors Couches Minces ont été réalisés en utilisant ces différents types de films, leurs caractéristiques électriques sont présentées.

Abstract - In this paper, we review some possibilities given by the LPCVD technique to deposit undoped and in-situ doped silicon films on amorphous substrates. To deposit undoped silicon films, two main techniques can be investigated: (i) the silicon films are deposited at temperature higher than 580°C and are polycrystalline. However, their grain size which depends on the deposition parameters, is also dependent on their thickness. (ii) The silicon films are deposited at temperature lower than 580°C and are amorphous. When these films are thermally crystallized at low temperature ($T_{\text{anneal}} \leq 600^\circ\text{C}$), the grain size may exceed $0.5 \mu\text{m}$ and does not depend on the thickness of the silicon films. When diborane is added ($\text{B}_2\text{H}_6/\text{SiH}_4 = 5 \cdot 10^{-3}$), the micro-crystalline of the silicon films is strongly modified. The decrease down to 10 mTorr of the gas pressure during the deposition process results in the increase of the boron incorporation and in the decrease of the resistivity to $2 \cdot 10^{-3}$ ohm.cm, without any annealing for the films deposited at 625°C. TFT's have been fabricated with these undoped silicon films and their electrical characteristics are presented.

1. INTRODUCTION

Polycrystalline silicon (Polysilicon) is a material becoming more widely used in microelectronics. Indeed, this material exhibits various structural and electrical properties such as a large range of resistivity which makes it suitable for the realization of passive and active components.

High resistivity polysilicon (i.e. undoped or lightly doped polysilicon) is used for the realization of resistors for Random Access Memory (RAM) [1] circuits, of sensors,

and of micromechanisms [2,3] and for also the realization of the active channel of the Thin Film Transistors (TFT) [4,5].

Low resistivity polysilicon (i.e. heavily doped polysilicon) is used for interconnections in integrated circuits, as a source of diffusion of doping species, for gates in the MOS technology [6] and for contacts for TFT's [7,8]. Some of these uses can be combined such as in the BICMOS technologies under development which require polysilicon films to act as a collector contact and as a diffusion source for the emitter realization [9].

Therefore, most of these applications requires polysilicon films with specific structural and electrical properties. For instance, the electrical behaviour of polysilicon TFT's is strongly dependent on the structure of the polycrystalline silicon films [5,10,11]. Therefore correlations between the deposition process of the polysilicon films and their structural and electrical properties must be established.

To fulfil these requirements, several techniques of deposition of polysilicon films such as evaporation, sputtering or CVD (Chemical Vapor Deposition) are available. Low Pressure Chemical Vapor Deposition (LPCVD) is the most widely used deposition technique for polysilicon films. This technique has proved to be cost effective as it offers a high throughput (batch process) and a high reliability within the physical properties of the deposited polysilicon films. Moreover, the LPCVD process is a thermally activated process, therefore there is no energetic and charged particle which can create defects in the semiconductor.

In this paper, we will point out the influence of deposition parameters, in particular, the silane pressure and the temperature during the deposition process on the structure of the LPCVD undoped and on the electrical properties of in-situ boron-doped silicon films. Moreover, the crystallization of the silicon films deposited in the amorphous state will also be presented, especially as a function of the nature of the substrate. Finally, comparison of TFT results obtained with as-deposited and crystallized silicon films will be reported.

2. UNDOPED POLYSILICON

The crystalline structure of the polysilicon films deposited by the LPCVD technique is extremely dependent on the temperature and the pressure during the deposition process. Indeed the structure of the silicon films can be either polycrystalline or amorphous according to the deposition parameters. Therefore, two techniques to deposit polycrystalline silicon can be considered: (i) where the silicon films are directly deposited into the polycrystalline structure, these films are the so-called as-deposited polysilicon films, (ii) where the silicon films are deposited into the amorphous state and are, then thermally crystallized.

2.1. As-deposited polysilicon

The new trends for the use of the polysilicon films for the realization of active components such as the Thin Film Transistors (TFT), have induced investigations on the LPCVD process in order to fit the structural and electronic properties of the polysilicon films with the realization of active devices [12,13].

The cross-sectional Transmission Electron Microscopy (TEM) micrograph of a 0.9 μm -thick polysilicon film (see Fig.1) shows a typical columnar structure of a LPCVD silicon film deposited on an amorphous substrate (i.e. glass substrate or silicon dioxide).

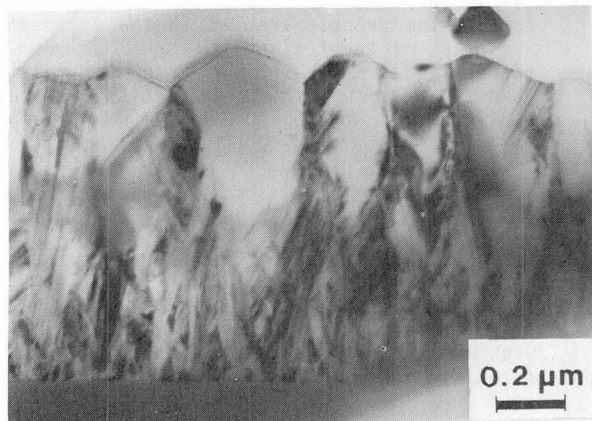


Fig.1. Cross-sectional TEM micrograph of a 0.9 μm thick polysilicon film deposited at 700°C (From ref.13)

The typical features of these films are:

- non-homogeneous structure through the film thickness
- rough surface of the silicon film
- lateral grain size of the silicon films which depends on the thickness of the films

However, the relative importance of these features depends strongly on the pressure-temperature parameters during the deposition process. A systematic investigation has been made on the structure of undoped silicon films deposited by thermal decomposition of

silane diluted into hydrogen (10% SiH₄ - 90% H₂) in a hot-wall LPCVD reactor, described in ref.13, in the temperature range of 580°C-700°C and in the silane pressure range of 2 · 10⁻⁴ - 1 Torr.

The crystallite size of the 1 μm thick silicon films, as determined by x-ray diffraction measurements, increases when the temperature increases and decreases when the silane pressure increases (as indicated by table.1). However, the silicon films deposited at low temperature (580°C) and at high silane pressure (1 Torr) are amorphous.

Table.1. Crystallites size determined from (220) X-Ray diffraction peak on 1 μm-thick poly-Si film deposited with a 40 sccm gas flow (10 sccm at 2.10⁻³ Torr) at five different gas pressures (10% SiH₄ - 90% H₂)

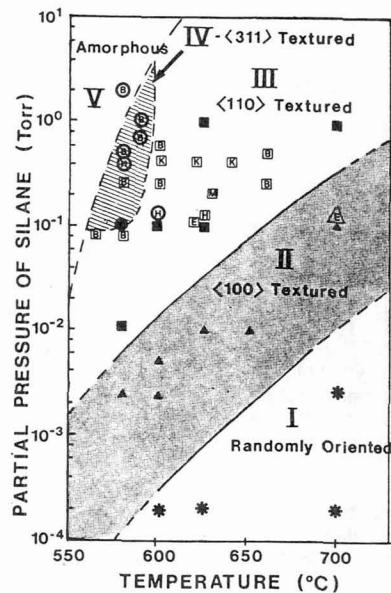
Temperature °C	XRD crystallite size (nm)				
	0.002 Torr	0.02 Torr	0.1 Torr	1 Torr	10 Torr
580	--	82	60	39	Amorphous
625	120	110	116	92	62
700	102	138	136	105	--

The temperature and the silane pressure have not only an effect on the grain size of the deposited silicon films but also on their texture. The orientation factor O_{hkl} of the silicon films, determined by x-ray measurements, corresponds to the volume fraction of material oriented in the <hkl> direction normal to the surface of the silicon film. The published experimental results on the subject of the dominant texture of LPCVD silicon films as a function of the deposition parameters (i.e. temperature and partial silane pressure) have been summarized with our own results in Fig.2.

The diagram shown in Fig.2 can be divided into five zones:

- Zone 1: at very low silane pressure, the silicon films are randomly oriented.
- Zone 2: at higher pressure, the layers are <100> textured.
- Zone 3: the layers are <110> textured. This part of the diagram corresponds to the experimental set of deposition parameters used in the classical LPCVD apparatus and therefore this is the zone where most of the experimental results are available.
- Zone 4: In a narrow zone, at temperature lower than 600°C and silane pressure higher than 0.1 Torr, the layers are <311> textured.
- Zone 5: here for the temperature lower than 580°C and pressure higher than 1 Torr, the silicon films are amorphous.

Fig.2. Dominant texture observed on LPCVD silicon films as a function of the temperature and the silane pressure (deposited with several gas mixtures). (Ref.13) Our measures (closed symbols: *, untextured; ▲, <100> textured; ■, <110> texture; ●, <311> texture; open symbols: B=Bisaro et al in Ref.(14); E=Kimura et al in ref.(15); H=Harbeke et al in ref.(16); K= Kamins in ref.(17); M=Meakin et al in ref.(12).



The nature of the diluting gas or the dilution ratio does not seem to have a significant effect on the texture of the layers since experiments have been performed with different gas mixtures (90% H_2 - 10% SiH_4 , 99% H_2 - 1% SiH_4 , 95% He - 5% SiH_4) and the texture of films obtained is very similar for the films deposited at the same temperature and the same partial silane pressure.

Similarly, the surface roughness of the deposited silicon films, investigated by Scanning Electron Microscopy (SEM), depends also on the silane pressure and the deposition temperature. The SEM micrograph reported in Fig.3.a shows that the surface of an untextured layer is rather smooth, whereas the surface roughness increases when the silane pressure increases. A strong <100> orientation is always characterized by a faceted grain relief as shown in Fig.3.c.

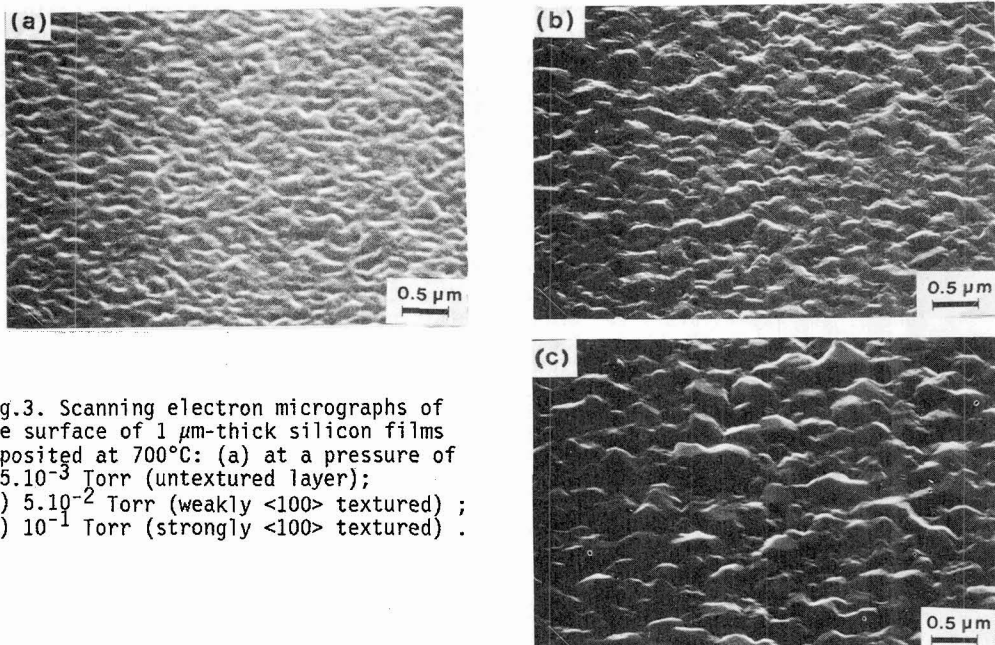


Fig.3. Scanning electron micrographs of the surface of 1 μm-thick silicon films deposited at 700°C: (a) at a pressure of $2.5 \cdot 10^{-3}$ Torr (untextured layer); (b) $5 \cdot 10^{-2}$ Torr (weakly <100> textured); (c) 10^{-1} Torr (strongly <100> textured).

2.2 Crystallised silicon

The electronic properties i.e. the field-effect mobility, the leakage current and threshold voltage of the Thin Film Transistors (TFT) realized with polysilicon films depend strongly on the grain size of the polysilicon. Moreover, it has been shown that TFT's with high field-effect mobility and low leakage current could be realized by using very thin polysilicon films (thickness < 100 nm) [18,19]. In this case, the devices are realized with the part of the silicon layer which is close to the substrate, hence with the strongly disturbed part of the as-deposited polysilicon layer as shown in Fig.1.

The thermal crystallization of amorphous silicon films is an alternative technique to obtain polysilicon with large grains at low temperature, regardless of the thickness of the silicon layer.

As previously shown in Fig.2, LPCVD silicon films deposited at a temperature lower than 580°C and a pressure higher than 0.1 Torr, are amorphous, whereas those deposited at a higher temperature, are polycrystalline. Moreover, amorphisation of LPCVD deposited polycrystalline silicon by self-implantation of Si-ions has been shown to be an alternative technique to produce amorphous silicon films [20,21].

These amorphous silicon films become polycrystalline after annealing at temperatures higher than 500°C. The crystallization process depends however on the thermal annealing process, the nature of the substrate, the deposition temperature and the post-deposition treatment of the silicon films [11,21,22,23,24].

The final grain size of the crystallized amorphous LPCVD silicon films may depend on the nucleation rate which is related to the deposition conditions (i.e. temperature, pressure, carrier-gas ..), the annealing temperature and duration, and the substrate nature.

It has been shown that the grain size of the thermally crystallized silicon films is maximised for the films deposited at temperatures around 550°C [11,23,25] and increases when the annealing temperature decreases [11,26]. In these conditions the annealing time needed to crystallize all the layer was found to be very long (>20 hours).

Transmission Electron Microscopy (TEM) were conducted on crystallized films. Fig.4.a shows top view of a silicon film deposited at 550°C on silicon dioxide substrate and annealed at 600°C for 15 hours. In contrast to the as-deposited polysilicon, the film exhibits a dendritic grain-like structure (Fig.4.a) with a large mean grain size (about 0.5 μm) in accordance with the previously published observations [11,21]. Furthermore, in all cases the crystallized Si films have smooth surfaces (Fig.4.b) even if the film is textured, whereas in the as-deposited polysilicon the surface roughness increases with the film texture due to the columnar nature of the grains. Moreover, the lateral size of the silicon grains do not change within the depth of the silicon film as shown in Fig.4.b.

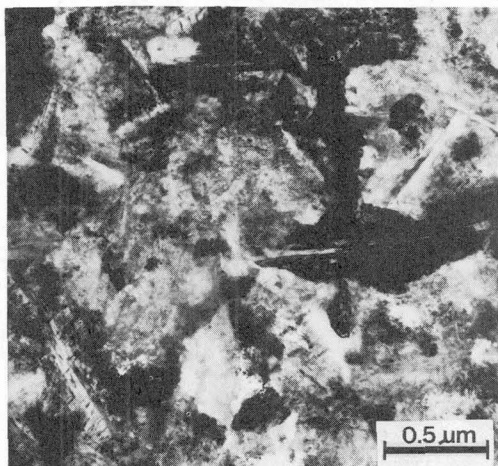


Fig.4.a. TEM top view of a crystallized silicon film.

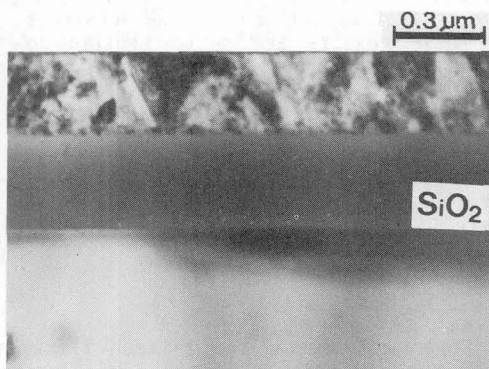


Fig.4.b. TEM cross-sectional observation of a crystallized silicon film.

Moreover, the polysilicon devices are fabricated on various substrates (glass, silicon dioxide,...) and it is necessary to determine the influence of the nature of the substrate on the crystallization process. To our knowledge, there is no comparative investigation of this effect on the crystallization process of amorphous LPCVD silicon films. We have undertaken investigations on the influence of the substrate nature on the crystallization of 0.5 μm -thick LPCVD amorphous silicon films deposited at 550°C on different types of substrates. The annealing process at 600°C was carried out under argon and the x-ray diffraction technique was chosen, from amongst other methods (Raman scattering, conductivity), to study the crystallization kinetics. The integrated x-ray intensity of the (111) diffraction peak was recorded after each step of annealing time and reported in Fig.5, for three types of substrates.

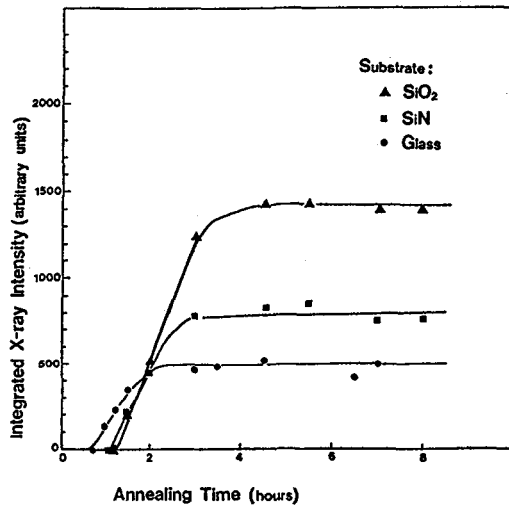


Fig.5. Effect of the nature of the substrate on the crystallization process of 0.5 μm -thick amorphous LPCVD silicon films.

From these curves, three points can be deduced: i) the incubation time, ii) the crystallization rate and iii) the full crystallization time of the <111> oriented grain. It has been found that the incubation time is minimized in the case where the glass substrate is used. This suggests that the nucleation rate is faster on glass substrate than on silicon nitride covered glass or silicon dioxide substrates. This, in turn, influences the final grain size, since the higher is the nucleus density, the smaller is the grain size. In addition, if we assume the crystallized volume (V_{111}) of <111> oriented grains to be proportional to the integrated intensity of the (111) diffraction peak, we found that V_{111} on SiO_2 is three times greater than that on glass and twice the volume of that on silicon nitride substrate.

These results are quite similar to those obtained in the case of solid phase crystallization of self-implanted amorphous silicon films [22]. In this technique, when the amorphous silicon film is Si-implanted near the film/substrate interface, a strong enhancement of the grain size of the crystallized LPCVD silicon film is observed. This effect has been attributed to a delay of the nucleation process [22].

The thermal annealing of the amorphous LPCVD silicon films provides silicon films with larger grain size and smoother surface than the as-deposited polycrystalline silicon films. However, the crystallization of the amorphous films requires a long duration (> several hours) in order to fully crystallize the silicon films.

3). DOPED SILICON

Doped polycrystalline silicon films are normally deposited undoped and then the dopants are added later by ion implantation or by diffusion from doped sources. These techniques require high temperature annealing processes to achieve full dopant activation. In-situ doping is an attractive alternative to these processes since extra steps are suppressed and lower cost of fabrication is expected.

However, investigations on the in-situ doping LPCVD process in a conventional hot-wall apparatus with phosphine (PH_3) for deposition of phosphorus doped polysilicon films have shown that the addition of Phosphine to the silane, drastically decreases the growth rate of the silicon films and induces a strong nonuniformity of the film thickness across the wafers [27,28,29,30]. On the contrary, the addition of diborane (B_2H_6) to the silane

induces variations on the growth rate of the silicon films especially in the low temperature range ($T_d \leq 580^\circ\text{C}$) where the addition of diborane to the silane increases the growth rate of the silicon films [30,31,32].

The investigations [33,34] on the doping process of the silicon films deposited on amorphous substrate with diborane added to the silane have shown that the texture of the deposited silicon films is strongly modified by the addition of diborane to the silane. Fig.6 reports the texture of the silicon films as a function of the deposition temperature and the silane pressure. The films were deposited with the same conditions as previously reported [13,31] for the undoped silicon except diborane was added to the silane ($\text{B}_2\text{H}_6/\text{SiH}_4 = 5 \cdot 10^{-3}$). As shown on this figure, the texture of the boron doped silicon films can be controlled by adjusting the deposition temperature and/or the Silane pressure. On the contrary to the undoped silicon films, the silicon films deposited at very low silane pressure are $\langle 100 \rangle$ textured when they are deposited at temperature higher than 550°C . There is no randomly oriented boron-doped silicon films. However, at lower temperature there is formation of an amorphous Si-B compound which is characterized by a very high boron concentration ($\geq 2 \cdot 10^{21} \text{ cm}^{-3}$).

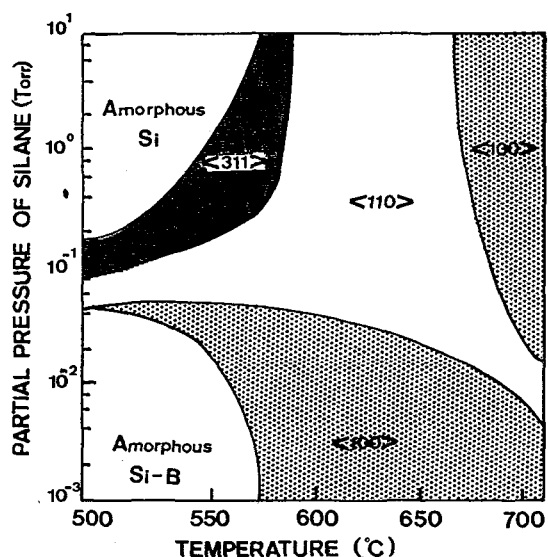


Fig.6. Texture as a function of the deposition parameters for $1 \mu\text{m}$ -thick boron-doped silicon films

The incorporation of the boron inside the silicon is also dependent on the deposition parameters as reported in Fig.7. One of the main results of this investigation is the strong effect of the silane pressure on the boron incorporation rate. Indeed, the concentration of boron inside the silicon films increases by a factor one hundred when the silane pressure decreases from 0.1 Torr down to 0.01 Torr and continuously increases when the deposition temperature decreases. Similar behaviour has been reported in the case of the use of disilane instead of silane and has been attributed to a surface reaction phenomena due to the incorporation of boron at the surface of the growing silicon film [35]. This assumption is supported by the very high concentration of boron in the silicon films deposited at very low silane pressure (Fig.7) whereas the gas-phase reactions are very unlikely.

The resistivity of these un-annealed films (Fig.8) will depend on their structure (as reported in Fig.6) and the boron concentration (as reported in Fig.7). For example, the films deposited at low pressure ($P_{\text{silane}} < 0.01 \text{ Torr}$) exhibit a resistivity about $2 \cdot 10^{-3} \text{ ohm-cm}$ when they are deposited at a temperature higher than 590°C whereas the films deposited in the same range of pressure but at lower temperature exhibit a resistivity higher than 1 ohm-cm . This variation of resistivity is directly connected to the variation of structure of silicon films as illustrated in Fig.6 where the films deposited in the high temperature range are fully crystalline whereas the films deposited in the low temperature range are amorphous. It should be noticed that such a low value of

the resistivity can be obtained for the films deposited at 625°C without any thermal annealing.

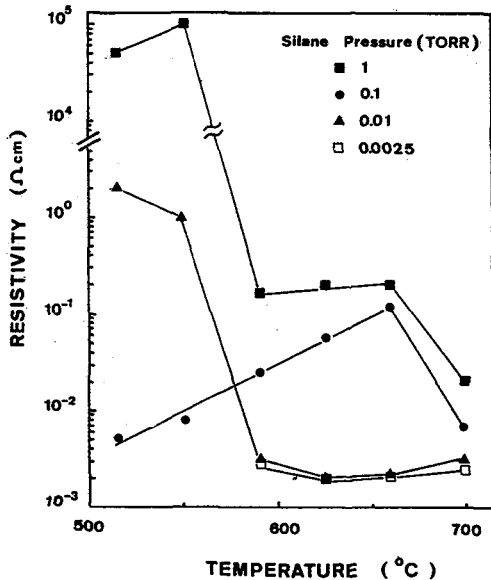


Fig.7. Boron concentration versus deposition temperature for various silane pressure

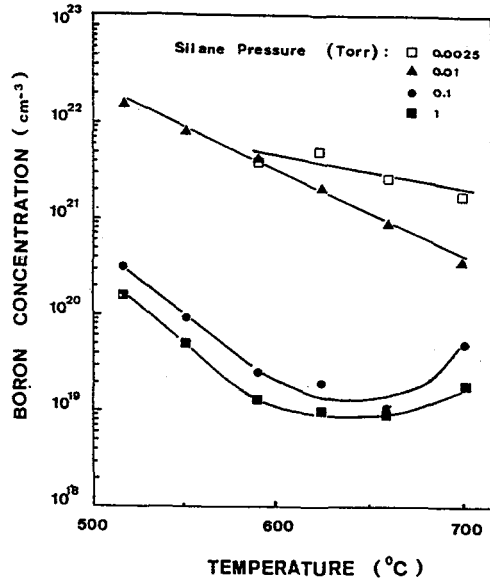


Fig.8 Resistivity of the 1 μm -thick boron-doped silicon films as a function of the silane pressure and temperature

4. ACTIVE DEVICES

The main applications of the polysilicon Thin Film Transistors (TFT) are the Three-Dimensional (3D) integration of active devices for high density memories [36] and the realization of large area devices such as display [37,38,39] or smart sensors[40]. The Active Matrix Liquid Crystal Display (AMLCD) technology plays a key role for the realization of large area displays. This technology is based on the use of TFT's at each intersection of the lines and of the columns to switch off or on the liquid crystal cell according to the video signal.

The polysilicon TFT's are good candidates to realize these switching devices since their switching capability ($I_{\text{on}}/I_{\text{off}}$ ratio) are compatible with the electrical specifications of the AMLCD's. They also offer a potential high field-effect mobility [22,41,42] and therefore the capability for drive circuits integration [25,43].

However, these displays must be realized on low cost, transparent substrates and their viewing area should be close to the full-page size. Therefore the objective is to realize a large size, low cost device on a glass substrate at low temperature to avoid any degradation of the glass substrates ($T_{\text{process}} \leq 600^\circ\text{C}$) which may contain several hundreds of thousands of TFT's.

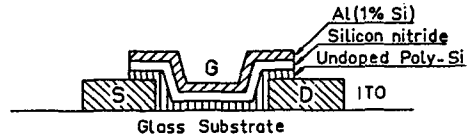
Numerous low temperature technologies realizing these TFT's on glass substrates are under development [39] and use as-deposited [38,39,44] or crystallized [25,26,43,45] LPCVD silicon films. The TFT's based on the crystallized silicon films usually exhibit a high field-effect mobility and therefore can be used for the realization of the AMLCD's with integrated drivers [25,43]. The TFT's based on the as-deposited polysilicon usually exhibit a lower field-effect mobility but offer the advantage of avoiding the long thermal annealing necessary for the crystallization of the amorphous films.

Besides the electrical requirements of TFT's for display realization, the complexity of the fabrication process of TFT's has to be very low to achieve high production yield and low cost, especially for the large area displays. To fulfil these requirements,

specific design for the AMLCD's realization has been used which necessitates a low number of photolithographic levels for TFT realization [40,44].

The design of TFT's based on a shortened process which needs only two photolithographic steps is reported in Fig.9 [44]. The starting substrate is an alkali-free glass substrate covered with an Indium Tin Oxide (ITO) layer which is etched to form the contacts (source and drain) of the TFT. The following are then deposited: an undoped silicon film by LPCVD, a silicon nitride layer by Plasma Enhanced Chemical Vapor Deposition (PECVD) and finally a 300 nm-thick layer of Al(1%Si) by e-gun evaporation. The second photolithographic step is used to form the gate structure.

Fig.9. Cross-sectional representation of poly-Si TFT



In Fig.10, the drain current I_d versus the gate voltage V_g is reported for two types of TFT's realized with the same structure but the silicon films were deposited by the two different LPCVD processes previously reported. The 40 nm-thick as-deposited polycrystalline silicon film were deposited at 590°C at low silane pressure whereas the 50 nm-thick amorphous silicon films were deposited at 570°C and thermally annealed at 595°C. The TFT's behave very similarly as n-channel enhancement types but as expected, for high gate voltage ($V_g = 20$ V), the I_{on} -current I_d is higher in the case of the crystallized silicon than in the case of the as-deposited silicon film. This increase of the I_{on} -current is directly correlated to the larger crystallite size of the crystallized silicon films. Indeed, the increase of grain size results in the increase of the field-effect mobility [11,18]. Moreover, it should be noticed that the I_{off} -current I_d ($V_g = -3$ V) of both TFT's are similar and lower than 10^{-11} A. The I_{on}/I_{off} ratio of the crystallized silicon TFT is of the order of 10^6 and therefore the electrical properties make these TFT's compatible with the realization of AMLCD's.

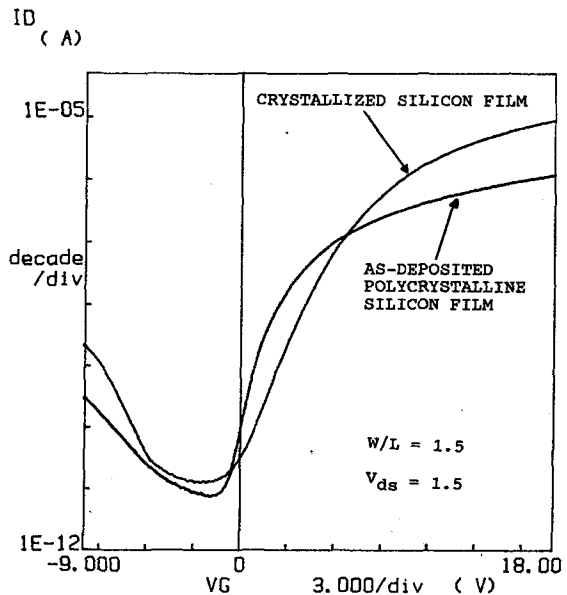


Fig.9. Subthreshold characteristics of TFT's realized with as-deposited polycrystalline silicon film and with crystallized silicon film

5. CONCLUSION

In this paper, we attempted to point out the effects of the deposition parameters on the structure and the electrical properties of the LPCVD silicon films. The decrease of the gas pressure during the deposition process appears to be the main factor involved in the improvement of the micro-structure of the as-deposited polycrystalline silicon films and in the decrease of the resistivity of the boron-doped silicon films. Moreover, the thermal crystallization of the amorphous silicon films offers the potential advantage of yielding large grains polycrystalline silicon films at low temperature, compatible with the use of glass substrates. These types of polysilicon films have been shown to be useful in the fabrication of high field effect mobility TFT's. However, this last technique necessitates long annealing times which are not always compatible with industrial processes.

The LPCVD technique has been shown to be a versatile tool which can be used in the domain of standard microelectronics as well as in large area microelectronics. New types of LPCVD apparatus are becoming available which can be used in the very low silane pressure to deposit large grains polysilicon films at low temperature and which can handle substrates which size up to 300*300 mm².

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REFERENCES

- /1/ Mahan J.E., Newman D.S. and Gulett M.R., IEEE Trans. Electron.Dev.ED-30(1983)45
- /2/ Howe R.T., "Polysilicon Films and Interfaces", (ed.Wong.C.Y,Thompson C.V and Tu K.N) M.R.S Proceedings, (1988)213
- /3/ Mehregany M., Gabriel K.J. and Trimmer W.S.N., IEEE Trans. Electron.Dev.ED - 35(1988)719
- /4/ Bartelink D .J , "Grains Boundaries in Semiconductors", Elsevier Science publishing company, (1982)249
- /5/ Kung K.T.Y , and Reif R , J.Appl.Phys. 61(1987)1638
- /6/ Adams A.C , "VLSI Technology", (ed.Sze S.M), McGraw-Hill(1983)
- /7/ Hawkins W.G , IEEE Trans. Electron.Dev.ED-33(1986)477
- /8/ Ahmed S.S , Kim D.M, Shichijo H., IEEE Trans. Electron.Dev.ED-33(1986)973
- /9/ Gerodolle A., Giroult G., Martin S., and Nouailhat A., "ESSDERC Proceedings", (ed.Nougier J.P and Gasquet D.) Les Editions de Physique, (1988)109
- /10/ Migliorato P, Meakin D.B., Appl. Surf. Science, 30(1987)353
- /11/ Hatalis M.K and Greve D.W., J.Appl.Phys., 63(1988)2260
- /12/ Meakin D., Stoemenos J., Migliorato P. and Economou N.A., J.Appl.Phys.61(1987)5031
- /13/ Joubert P., Loisel B., Chouan Y., and Haji L., J.of Electrochem. Soc. 134(1987)2541
- /14/ Bisaro B., Magarino J., Proust N. and Zellama K., J.Appl.Phys., 59(1986)1167
- /15/ Kimura M. and Egami K., Appl. Lett., 44(1984)420
- /16/ Harbeke G., Krausbauer L., Steigmer E.F., Widmer A.E., Kappert H.F. and Neugebauer G., J.of Electrochem. Soc. 131(1984)675
- /17/ Kamins T.I., Mandurah M.M. and Saraswat K.C., J.of Electrochem. Soc. 125(1978)927
- /18/ Morozumi S., Araki R., Oshima H., Matsuo M., Nakazawa and Sato T., Proceedings "Japan Display'86" (1986)196
- /19/ Hayashi H., Noguchi T. and Oshima T., Jap.J.of Appl.Phys., 23(1984)L819
- /20/ Kung K.T.Y , and Reif R., J.Appl.Phys. 59(1986)2422
- /21/ Noguchi.T., Hayashi H. and Ohshima T., J.of Electrochem. Soc. 134(1987)1771.
- /22/ Chiang A., Huang T.Y., Wu I.W. and Zarzicki M.H., Polysilicon Films and Interfaces, M.R.S Proceedings,(1988)305
- /23/ Panwar O.S., Moore R.A., Mitchell N.J.S., Gamble H.S and Armstrong B.M., Appl. Surf. Science, 36(1989)247
- /24/ Harbeke G., Krausbauer L., Steigmeier E.F., Widmeier A.E., Kappert H.F. and Neugebauer G., Appl. Phys. Lett. 42(1983)249
- /25/ Mimura A., Konishi N., Ono K., Ohwada J., Hosokawa Y., Ono Y.A., Suzuki T., Miyamata K. and Kawakami H., "Proceedings IEDM"(1987)436
- /26/ Loisel B., Haji L., Joubert P. and Guendouz M., To be published in "Proceedings Polyse'88",(ed. Moller H.J., Strunk H.P. and Werner J.H.), Springer-verlag

- /27/ Hitchman M.L and Ahmed W., Vacuum 34(1984)979
- /28/ Meyerson B.S. and Olbricht W., J.of Electrochem. Soc., 131(1984)2361
- /29/ Learn A.J.and Foster D.W.,J.Appl.Phys.61(1987)1898
- /30/ Eversteyn F.C.and Put B.H., J.of Electrochem. Soc. 120(1973)106
- /31/ Joubert P., Sarret M.,Haji L., Hamedi L. and Loisel B., To be published
- /32/ Mercadere L., Thesis Toulouse (1988)
- /33/ Haji L., Hamedi, Rupert A., Loisel B. and Joubert P., To be published Proceedings Polyse
- /34/ Bielle-Daspert D. et al, Thin Solid Films,150(1987)69
- /35/ Nakayama S., Kawashima I. and Murota J., J.of Electrochem. Soc. 133(1986)1721.
- /36/ Maihi S.DS., Shichijo H., Banerjee S.K., Sandaresan R., Elahy M., Pollack G.P., Richardson W.F., Shah A.H., Womack R.H., Chatterjee P.K. and Lam H.W., IEEE Trans. Electron.Dev., ED-32(1985)258
- /37/ Sasaki A. and Uchida T., Proceedings Japan Display (1986)63
- /38/ Oshima H., Nakazawa T., Shimobayashi T., Ishiguro H. and Morozumi S., SID Technical digest (1988)408
- /39/ Migliorato P., Seminar Lecture Notes, Proceedings SID I (1988)5.2
- /40/ Morozumi S., Hurihara H., Oshima H., Takeshita T.and Hasegawa K., Proceedings conference on Solid State Devices and Materials , Kobe, (1984)559
- /41/ Oshima T., Noguschi T. and Hayashi H., Jpn. J. Appl. Phys., 25(1986)L291
- /42/ Hawkins W.G., IEEE Trans. Electron.Dev., ED-33(1986)477
- /43/ Ipri A.C. and Stewart R.G., "Proceedings Eurodisplay'87" (1987)188
- /44/ Loisel B., Haji L., Sangouard P. and Sarret M., Electronics Lett. 24(1988)156
- /45/ Hseih B., Hatalis M.K and Greve D.W.,IEEE Trans. Electron.Dev., ED-35(1988)1842