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RAPID THERMAL ANNEALING OF TiW SCHOTTKY CONTACTS ON GaAs

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1 INTRODUCTION

Recently, there has been an increasing interest in the application of refractory gate metals in a self-aligned GaAs metal-semiconductor field-effect transistor (MESFET) technology. The processing requires the gate material to maintain a good rectifying contact with low leakage current and high breakdown voltage when subjected to high temperature annealing (~900°C) necessary to activate the n⁺ implant. The refractory metal/GaAs interface has to be mechanically, chemically and electrically stable. Most problems are related with peeling off, chemical reaction and interdiffusion. Although TiW and TiW-based alloys have been frequently considered as appropriate candidates /1,2,3/, the stability of TiW during rapid thermal annealing (RTA) has not yet been ascertained. In this contribution we report an extensive study of the TiW/GaAs interface after RTA.

2 EXPERIMENTS

After degreasing and in situ Ar sputtercleaning, thin films (50nm-200nm) of TiW were deposited on Si-doped GaAs wafers (n ~ E17/cm³) by dc magnetron sputtering from a 30%Ti/70%W compound target. The Ar pressure was optimized to obtain minimum film stress conditions. The composition of the deposited TiW films was determined by RBS as 25%Ti/75%W. The samples were subjected to RTA in forming gas ambient at 700°C-1050°C, 10s. Electrical measurements were performed on 90µm×90µm Schottky diodes patterned by standard lithography. Alloyed AuGe/Ni was used as backside contact. In order to avoid diode leakage at the edges about 200nm of GaAs was etched away in H2SO4:H2O2:H2O before measurement.
Fig. 1 - High resolution cross-sectional TEM image of the TiW/GaAs interface after annealing at 900°C, 10s.

Fig. 2 - Auger depth profiles of Ti, W, Ga, As and O of as-deposited and annealed (880°C, 10s) TiW films on GaAs.

Fig. 3 - SIMS depth profiles of Ti, W, Ga and As of as-deposited and annealed (950°C, 10s) TiW films on GaAs.
3 RESULTS AND DISCUSSION

All the films examined showed good adherence even after annealing at the highest temperatures. XRD analysis showed a clear W α-phase spectrum. After annealing, the peaks showed a reduction of the halfwidth, which can be attributed to grain size growth. High resolution cross-sectional TEM examination (fig.1) showed good TiW/GaAs interface stability. However, local island growth of epitaxial phases induced by RTA were found. No clear morphologic structure in the TiW film could be detected by TEM, due to the very strong absorption of the electron beam by the metal. Auger (fig.2), SIMS (fig.3), RBS (fig.4) and EDS show significant motion of the Ti resulting in surface accumulation as well as Ti diffusion into the GaAs substrate. The W/GaAs interface however remains stable for temperatures up to \( \sim 1000^\circ\text{C} \).

Forward and reverse current-voltage characteristics of as-deposited and annealed TiW Schottky contacts are shown in fig.5. They show a continuous increase in both the ideality factor and the Schottky barrier heights extracted from IV- and CV-data (fig.6). Diodes annealed at 950°C have a barrier height as high as 0.95eV (IV-value), which is considerably higher than the value of 0.70eV obtained for nonannealed diodes. Significant degradation of the diodes occurs after annealing at temperatures higher than 1000°C, coinciding with the onset of W/GaAs interdiffusion.

Breakdown characteristics of as-deposited and annealed TiW/GaAs contacts are depicted in fig.7. Unannealed diodes show a soft turn-on of the breakdown, which is characteristic for Schottky diodes. After annealing the breakdown voltage increases and the characteristics become avalanche-like. Measurements at higher temperatures show an increase in breakdown voltage, which confirms avalanche being the breakdown mechanism.

The RTA-induced properties of the contacts are consistent with the Shannon contact structure /4/ (metal/p+-GaAs/n-GaAs). The p+-formation is attributed to the indiffusion and activation of Ti which is known to have acceptor levels in GaAs /5,6/. Due to the p+-layer formation a barrier height enhancement occurs. With increasing annealing temperature the p+-layer becomes thicker and/or more highly doped. This explains the steady increase of the barrier height with annealing temperature. It is estimated that a 1.E18/cm³ p+-layer of 200Å thickness can account for the 250meV difference in the barrier height between the as-deposited and 950°C annealed diodes. The avalanche breakdown behaviour of the annealed diodes is consistent with the formation of a p+-layer between the metal and the n-GaAs substrate. Breakdown will be initiated by avalanche multiplication at the p+/n junction.

Our observations show that rapid thermal annealed TiW/GaAs contacts, and Shannon contacts in general, can have advantageous properties for application in a self-aligned MESFET technology.

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Fig. 6 - Ideality factors and barrier heights for TiW/GaAs contacts annealed at different temperatures.

Fig. 4 - RBS spectra of TiW/GaAs samples annealed at different temperatures.

Fig. 5 - Forward and reverse current-voltage characteristics for TiW/GaAs contacts annealed at different temperatures.

Fig. 7 - Reverse leakage current versus reverse applied voltage of as-deposited and annealed (950°C, 10s) TiW/GaAs contacts.