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RAPID THERMAL PROCESSING OF ARSENIC-IMPLANTED POLYSILICON ON VERY THIN OXIDE

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Résumé - Dans le cadre d'un procédé CMOS à grilles en silicium polycristallin (n^+ et p^+), le recuit thermique rapide a été utilisé avec succès pour une grille en silicium polycristallin implanté avec de l'arsenic et déposé sur 7 nm de SiO_2 . Le travail de sortie de la grille que nous avons obtenu correspond à la valeur théorique attendue. Les états d'interface et les charges fixes dus au recuit rapide peuvent être éliminés par un recuit à 500°C sous forming gas. Les mesures de tensions de claquage aussi bien instantanées qu'en fonction du temps montrent que l'intégrité de l'oxyde de grille (7 nm) est préservée après le recuit rapide. La diffusion de l'arsenic dans le silicium polycristallin lors du recuit rapide est en accord avec les résultats de la littérature pour des recuits conventionnels.

Abstract - We demonstrated the feasibility and advantages of using rapid thermal annealing (RTA) to achieve a proper work function for arsenic-implanted polysilicon gate on 7 nm SiO_2 in a dual work function (n^+ and p^+) poly-gate CMOS process. Interface states and fixed oxide charge due to RTA can be annealed out at 500°C in forming gas. Time-zero and time-dependent breakdown results show that the integrity of 7 nm gate oxide can be preserved after RTA. The diffusivity of arsenic in polysilicon under RTA is found to be consistent with literature data from conventional furnace anneals.

1 - INTRODUCTION

Doping of the polysilicon gate by using the source/drain ion implantation step for a dual work function (n^+ and p^+) poly-gate CMOS process is desirable and challenging under reduced implant dose and thermal budget for future sub-micrometer CMOS VLSI applications /1/. Recently rapid thermal processing (RTP) or annealing (RTA) has been studied as an alternative or supplement to the conventional furnace annealing for minimizing the heat treatment necessary to diffuse and activate dopants. It has also been explored for silicide, glass reflow, oxidation and nitridation processes /2/. In this paper we report the results of a comprehensive study on the rapid thermal annealing of arsenic-implanted polysilicon gate electrode on 7 nm gate oxide. It is demonstrated that RTA is required for the activation of arsenic to get a degenerately doped n^+ polysilicon, while maintaining shallow source and drain junctions in a dual work function poly gate CMOS process. SIMS profile (chemical concentration) should be supplemented with carrier concentration profile to investigate the dependence of gate work function on arsenic dose and annealing conditions. The effective diffusivity of arsenic in polysilicon under RTA conditions is extracted. The effects of RTA on the quality and integrity of the underlying 7 nm thin gate oxide have been identified and methods to anneal out RTA induced damage are reported.

2 - EXPERIMENTAL

Aluminum contacted polysilicon-gate capacitors were fabricated on 1 $\Omega\text{-cm}$ (100) p-type Si wafers. Immediately after 7 nm dry oxide was grown, 250 nm polysilicon was deposited at 610°C by low pressure chemical vapor deposition (LPCVD). The polysilicon gate was doped by arsenic ion implantation (2×10^{15} or $4 \times 10^{15} \text{cm}^{-2}$) through 10nm screen oxide at 30 KeV. Different combinations of furnace annealing and RTA (AG-2146) in nitrogen were performed to redistribute and activate arsenic. Splits in RTA gas atmosphere (N_2 , Ar, and forming gas) and ramp rate conditions have been included. No post-aluminum annealing was performed. The flat band voltage (V_{FB}) and interface states density D_{it} were obtained by using high-frequency (HFCV) and quasi-static C-V (QSCV) measurements. Arsenic concentration was measured by SIMS. Carrier concentration and mobility were determined by Hall effect and resistivity measurements using a Van der Pauw geometry fabricated on polysilicon. Time zero oxide breakdown (TZBD) was measured by ramping the current and recording the snap-back voltage. Time dependent breakdown (TDBD) measurements were performed by constant current stress.

3 - ARSENIC DIFFUSION AND ACTIVATION

The difficulty of using conventional furnace annealing to achieve degenerately doped n-type polysilicon with reduced implant dose and annealing temperature is illustrated in Fig.1, case A, where the chemical (SIMS, solid line) and carrier concentration (dots) profiles of As implanted ($2 \times 10^{15} \text{cm}^{-2}$ dose) 250 nm polysilicon are shown after furnace annealing at 850°C for 30 min. High diffusivity of As along the grain boundaries /3/ at 850°C gives a high concentration of As (about $2 \times 10^{19} \text{cm}^{-3}$) at the gate oxide interface. However, the carrier concentration profile in Fig.1, case A, clearly shows low activation of As (4.2% of the implant dose) due to severe As segregation into the grain boundary at low temperature /4/. A high-resistivity polysilicon layer exists near the gate oxide interface due to limited dopant activation and low carrier mobility. The work function of this polysilicon deviates from that of a degenerately doped n⁺ polysilicon as indicated by the measured value of V_{FB} (-0.6V) which is more positive than the theoretical value (-0.92V) for n⁺ polysilicon on 7 nm oxide and $2 \times 10^{16} \text{cm}^{-3}$ boron-doped substrate. Moreover, a reduction of MOSFET transconductance can result from the formation of a depletion layer near the polysilicon/oxide interface under positive gate bias due to low active As concentration.

SIMS profile (solid line) of Fig.1, case B, shows that an additional RTA at 1100°C for 10 sec in N_2 re-distributes As uniformly across the 250 nm polysilicon film. The nearly flat carrier concentration profile (dots) with an average value of $1.7 \times 10^{19} \text{cm}^{-3}$ clearly demonstrates the effectiveness of the additional RTA (high temperature, short time) in activating a large amount of As, up to 21% of the implant dose.

Fig.2 shows the As concentration (solid lines) and the carrier concentration (dashed lines) in polysilicon as a function of RTA temperature without any prior furnace anneals. RTA at 1100°C for 10 sec is necessary to distribute As uniformly throughout the 250 nm polysilicon film as indicated by curve C. The redistribution of As in 250 nm polysilicon is incomplete at lower RTA temperatures as evidenced by curve B (1050°C) and curve A (1000°C), where a considerable amount of As remains near the top surface of the polysilicon film. It is worth noting that the arsenic concentration increases towards the polysilicon-oxide interface after RTA at 1100°C as seen in the SIMS profiles of Fig.2, case C, and Fig.1, case B. This effect is due to the grain structure of the polysilicon. Cross sectional TEM reveals columnar grains with high density of smaller grains near the polysilicon/oxide interface, meaning increased grain boundary area toward that interface. This results in an increased amount of arsenic confined at or near the grain boundary and therefore an increase in total arsenic (SIMS) concentration toward the polysilicon/ SiO_2 interface.

The average carrier concentrations are $0.9 \times 10^{19} \text{cm}^{-3}$, $1.1 \times 10^{19} \text{cm}^{-3}$, and $1.8 \times 10^{19} \text{cm}^{-3}$ after RTA at 1000°C , 1050°C and 1100°C , respectively. Although the average carrier concentrations are within a factor of two for the three RTA temperatures, the carrier concentration profile depends strongly on RTA temperature. As shown in Fig.2, RTA at 1100°C is required to activate a large amount of arsenic close to the oxide interface. The carrier concentration after RTA at 1000°C is high at the surface ($\approx 4 \times 10^{19} \text{cm}^{-3}$), but falls off sharply beyond a depth of 50 nm from the polysilicon surface, consistent with measured SIMS As concentration, grain size, and the segregation effect. It is therefore clear that neither SIMS profile nor average carrier concentration is sufficient, and they must be supplemented with carrier concentration profile measurements in order to investigate the dependence of polysilicon work function on implant dose and annealing conditions, even in the case of RTA.

The effective diffusivity of As along the polysilicon grain boundary was extracted from SIMS profiles using a large grain (200-300 nm) polysilicon film /5/ so that only a very small fraction of the implanted arsenic impurities near the surface, i.e. those within a diffusion length of the grain boundary can reach the grain boundary and diffuse rapidly through it. In such a case a simple one dimensional limited-source diffusion model applies, and the tail part of the SIMS profile fits well to a Gaussian curve. The RTA and furnace diffusivity data obtained in this way are plotted in Fig.3 together with some published data of arsenic in polysilicon /3,6/. The diffusivity data spreads at least over two orders of magnitude due to the strong dependence of grain boundary diffusion on grain structure and impurity or dopant content. Our data from either furnace annealing or RTA is within the spread. The activation energy calculated from our limited data is 3.5 eV, consistent with reported values /3,6/, suggesting that the diffusion of arsenic under RTA and furnace annealing follow the same physical mechanism. The broadening of the arsenic peak in the SIMS profile at the surface of the same large grain (200-300 nm) polysilicon after RTA, mainly due to the movement of the dopant inside the grain, may be used to estimate the diffusion length of high concentration of arsenic in single crystalline silicon. A value of 15 nm for \sqrt{Dt} under 1100°C 10 sec RTA was obtained, which agrees with extrinsic arsenic diffusivity data /7/. This is evidence that dopant redistribution in the substrate is very little during such polysilicon RTA processes.

4 - INTERFACE STATES AND OXIDE CHARGE

There is an increase in interface states density after RTA in N_2 as shown in Fig.4. Two peaks have been

observed in both poly and Al gate capacitors, one located at roughly 0.1eV above midgap energy with a density of 10^{13} eV⁻¹cm⁻² and the other at 0.35eV below midgap with a density of 2×10^{12} eV⁻¹cm⁻². This increase in D_{it} is consistent with published data on post oxidation furnace annealing in nitrogen /8/. It has little dependence on RTA temperature above 800°C, gate material, or RTA temperature ramp rates. There is no D_{it} increase if RTA is performed in forming gas. The RTA induced interface states may be explained in terms of the reduction of the concentration of water related groups and the increase of the density of Si dangling bonds at the SiO₂/Si interface during RTA in inert gas ambient. These interface states persisted after 400°C 30 min anneal in forming gas. They are completely annealed out after a 500°C pre-aluminum FG anneal for 30 min.

RTA also induced a positive V_{FB} shift that can be attributed to changes in the density of interface states and fixed oxide charge. A reduction in positive fixed oxide charge after high temperature anneal in an inert ambient was reported previously /9,10/. The change in fixed oxide charge is further confirmed by performing RTA in forming gas, where positive shift is observed without any increase in D_{it} . Another evidence of the change in fixed oxide charge is that D_{it} increase is independent of the RTA temperature ramp rate while V_{FB} shift is bigger for higher ramp rate. Our data shows that the positive V_{FB} shift can be completely recovered after a pre-metallization FG anneal at 500°C for As-doped n⁺ polysilicon-gate capacitors.

Fig.5 shows V_{FB} and carrier concentration data as a function of thermal process. The first case (850°C 30 min) corresponds to case A of Fig.1 where the low (-0.6 V) V_{FB} value is due to low carrier concentration at the polysilicon-oxide interface. The second and third case correspond to RTA at 1100°C with or without a prior furnace anneal. In these cases the carrier concentration at the interface is high enough for degenerately doped polysilicon conditions but V_{FB} is still low, which is due to RTA induced changes in oxide charge and interface states. An ideal V_{FB} value (-0.92V) is achieved if an additional anneal is done after RTA, i.e., at 500°C for 30 min in forming gas (the one to anneal out interface states) or at 800°C for 15 or 60 min in N₂. In spite of the decrease of carrier concentration after 800°C furnace annealing, the V_{FB} is still the expected one, suggesting that the polysilicon is degenerately doped from V_{FB} point of view if carrier concentration at the oxide interface is at least 10^{19} cm⁻³.

5 - INTEGRITY OF 7 nm GATE OXIDE

Fig.6 shows that RTA at 1100°C for 10 sec in N₂ increases the average time-zero oxide breakdown field by roughly 0.4 MV/cm. Additional anneal at 800°C for 1 hr in N₂ has no extra effect on the breakdown strength. Fig.7 shows little change in the oxide breakdown charge density after RTA at 1100°C under constant current (Fowler-Nordheim tunneling) stress measurements. The improvement in breakdown strength is consistent with published data on post-oxidation annealing effects using conventional furnaces /8/. which can be attributed to the reduction of water-related groups and the modification of sub-oxide charge state concentration /8/.

6 - CONCLUSION

In conclusion, we demonstrated the need, feasibility, and advantages of using rapid thermal annealing to achieve a proper As-doped n⁺ polysilicon work function on very thin gate oxide with little dopant redistribution in the substrate. The importance of carrier concentration data to supplement SIMS data has been demonstrated. Diffusivity data of arsenic in polysilicon for furnace annealing and RTA has been extracted. The effects of RTA on the interface states, fixed oxide charge, and breakdown strength have been identified. The integrity and quality of 7 nm gate oxide after RTA of the polysilicon gate can be preserved by means of a suitable low temperature furnace anneal.

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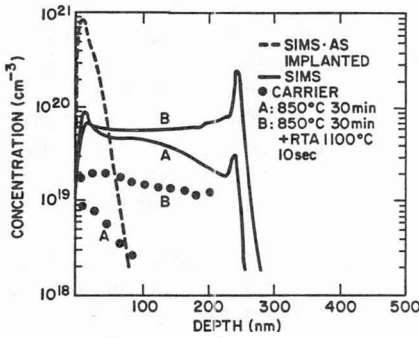


Fig. 1: SIMS (solid lines) and carrier concentration (dots) profiles of As in 250 nm polysilicon on top of 7 nm gate oxide after 850°C 30 min furnace anneal (A) and additional RTA at 1100°C for 10 sec (B). Dashed curve represents the as-implanted As profile ($2 \times 10^{15} \text{As/cm}^2$, 30 KeV)

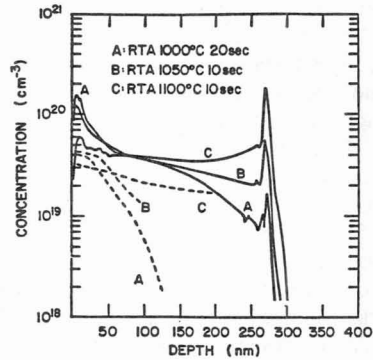


Fig. 2: SIMS (solid line) and carrier (dashed line) concentration profiles of As after 1000°C (A), 1050°C (B), and 1100°C RTA (C) without any prior furnace anneal. 250 nm polysilicon; $2 \times 10^{15} \text{As/cm}^2$, 30 KeV.

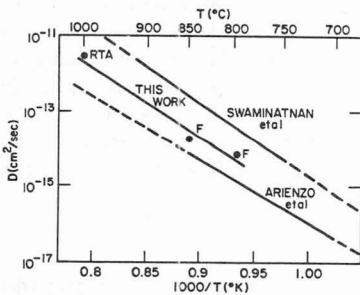


Fig. 3: Effective diffusivity of As along the polysilicon grain boundary.

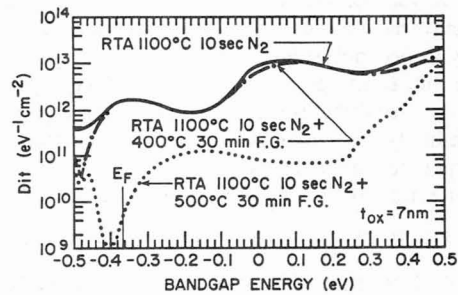


Fig. 4: Interface state density after RTA and the effects of subsequent pre-aluminum anneals in forming gas.

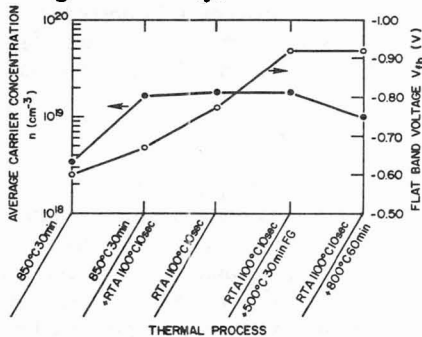


Fig. 5: Flatband voltage and average carrier concentration vs. thermal process. 250 nm polysilicon; $2 \times 10^{15} \text{As/cm}^2$, 30 KeV.

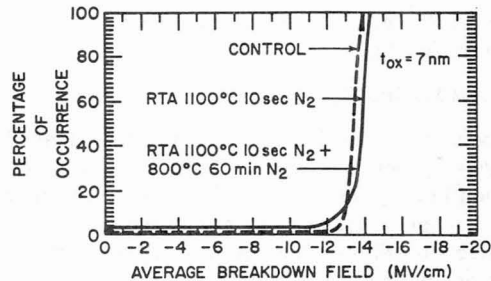


Fig. 6: Time-zero oxide breakdown statistics as a function of thermal process history. The polysilicon of control devices was doped degenerately with $4 \times 10^{15} \text{As/cm}^2$ at 30 KeV and 950°C annealing for 30 min in N_2 .

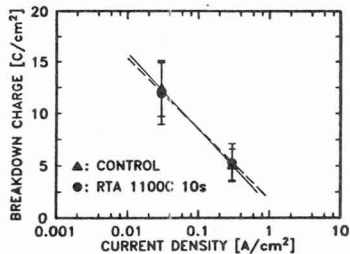


Fig. 7: Breakdown charge density vs. stress current for the control and RTA samples of Fig. 6.