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A MOBILITY MODEL FOR MOSFET DEVICE SIMULATION

A. J. WALKER and P. H. WOERLEE

Philips Research Laboratories, NL-5600 JA Eindhoven, The Netherlands

Abstract The device characteristics of sub-micron MOS transistors depend strongly on the mobility of the charge carriers in the inversion layer. A new low lateral field mobility model for the normal field dependence will be presented. Good agreement was found between the predicted and measured mobilities for a large variety of samples. The model was successfully incorporated into a two - dimensional device simulation program which gave predictions agreeing well with experimental data.

1. INTRODUCTION

The importance of sub - micron silicon MOS transistors in future generations of memory and logic circuitry has led to intense interest in the accurate modelling of these devices with particular attention being paid to the mobility of the charge carriers in the inversion layer. Scaling the transistors into the sub - micron regime demands the use of thinner gate oxides and higher substrate doping densities. The influence that these changes have on the mobility must be built into any model if accurate predictions are to be made about device performance.

This paper presents a new physically - based model for the normal effective field dependence of the electron and hole mobilities in silicon inversion layers at low lateral fields. Recent results of an investigation into the application of this model to measurements carried out on MOS devices with gate oxide thicknesses and surface doping densities scaled for process generations down to $0.25\mu\text{m}$ are given. Furthermore, for the first time such a model was incorporated in a two - dimensional device simulation program and comparisons between predictions from this program and measurements on sub - micron transistors are presented.

2. MODEL

It has been shown elsewhere that the electron [1] and hole [2] mobilities follow universal curves when plotted as functions of an effective normal field, E_{eff} , given by

$$E_{eff} = \frac{1}{\epsilon_{si}}(Q_{dep} + \eta Q_{inu}) \quad (1)$$

with $\eta = 1/2$ for electrons and $1/3$ for holes and where Q_{dep} and Q_{inu} are the depletion and inversion layer charges per unit surface area respectively.

In this new model a semi - empirical approach was taken to model the mobility - E_{eff} curves. It was assumed that the room temperature inversion layer mobility is dominated by three scattering mechanisms [3], namely Coulomb, carrier-phonon and surface roughness, each with its own contribution to the net mobility. These contributions are designated by μ_c , μ_{cp} and μ_{sr} respectively. Actual modelling of scattering processes in inversion layers is very complex due to the quantum mechanical nature of these processes and the fact that at temperatures above absolute zero more than one sub - band is filled. Therefore, a simplified semi - empirical approach was adopted.

To obtain a simple first order expression for carrier mobility due to screened Coulomb scattering, the Brooks - Herring formula was adopted [4]:

$$\mu_c = \frac{CT^{1.5}}{\ln(1+b) - b/(1+b)} \cdot \frac{1}{N_I} \quad (2)$$

where $b = (24m^* \epsilon_{Si} k^2 T^2) / (\hbar^2 q^2 N_o)$, N_I is the charged impurity density, N_o is the mobile carrier density, C is a constant, ϵ_{Si} is the dielectric constant of silicon and the other symbols have their usual meanings.

The following modifications were made for the inversion layer :

$$N_o = n_{inv} / \langle z \rangle \quad N_I \longrightarrow N_I + N_{ox} / \langle z \rangle$$

where n_{inv} is the number of mobile carriers per unit surface area, $\langle z \rangle$ is the average distance of mobile carriers from the Si/SiO_2 interface and N_{ox} is the fixed oxide charge per unit surface area.

As a result of numerical calculations [5], $\langle z \rangle$ can be given as a function of the mobile inversion charge number density per unit surface area, n_{inv} , and therefore as a function of E_{eff} .

As was given elsewhere [6], the mobility μ_{cp} due to carrier - phonon scattering and the mobility μ_{sr} due to surface roughness scattering can be approximately given by

$$\mu_{cp} = k_{cp} T^{-1} E_{eff}^{-1/3} \quad (3)$$

$$\mu_{sr} = k_{sr} E_{eff}^{-2} \quad (4)$$

where k_{cp} and k_{sr} are constants.

The net mobility μ was calculated using Matthiesen's rule. i.e.

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{cp}} + \frac{1}{\mu_{sr}} \quad (5)$$

with μ_c , μ_{cp} and μ_{sr} given in equations 2, 3 and 4 respectively with the constants C , k_{cp} and k_{sr} as fitting parameters.

The above equations were incorporated into a two - dimensional device simulation program, CURRY [7], in which the effective field at any point from source to drain was calculated by averaging the normal field in the depth direction over the inversion layer or surface accumulation layer at that point. The model is therefore a non - local one with the mobility at any point dependent on the values of the normal electric field at other points.

3. EXPERIMENTAL

To measure the mobility, a set of devices was fabricated which included both n- and p-type transistors and associated capacitors. The devices were all made on (100)-oriented p-type Si wafers with a resistivity of 20 Ω .cm. An n-well was formed using high energy phosphorus and arsenic implants while the p-substrate was implanted with high energy boron for the n-type devices. Gate oxides of thickness between 10nm and 23nm were thermally grown at 900°C in an oxygen/nitrogen mixture (10% oxygen by volume). Polysilicon gate electrodes were used and doped with phosphorus. Capacitor gate electrodes had areas of up to $3.3 \times 10^{-4} \text{cm}^2$ with transistor gate areas up to $4 \times 10^{-4} \text{cm}^2$. Gate oxide fixed charge and interface state levels of below $1 \times 10^{11} \text{cm}^{-2}$ were measured in the devices.

The effective inversion layer mobility, μ , was extracted from conductance measurements in the linear region on $200\mu\text{m} \times 200\mu\text{m}$ MOS transistors. The mobile inversion charge per unit surface area, Q_{inv} , was measured on the capacitor structures [8]. The sub - micron transistors were fabricated using electron beam lithography. The n-MOS device had a gate length of $0.53\mu\text{m}$ and width of $3.9\mu\text{m}$. Its gate oxide was 12.5nm thick. The p-MOS device had a gate length and width of $0.60\mu\text{m}$ and $4.2\mu\text{m}$ respectively with a 10nm thick gate oxide.

4. RESULTS AND DISCUSSION

The results from mobility measurements on the large n- and p-MOS devices are given in Fig.1 and 2 respectively in which mobility is plotted as a function of normal effective field. The surface doping density, N_s , and gate oxide thickness, t_{ox} , are also shown in the figures. The points are the experimental data with the

solid lines being the fits of the model to these data. Fig.1 shows that the electron mobility in the inversion channel is almost independent of surface doping density at high effective fields but depends strongly on the doping at lower fields. In the case of the pMOS devices, different boron implants had been introduced into the originally n-type channel but it was not clear as to what the actual density of charged impurities would be since the impurities are not completely ionized.

It was apparent in the model for electrons that the same values for C (equ.2), k_{cp} (equ.3) and k_{sr} (equ.4) could be used for all samples provided that the surface doping density, N_I , and the oxide fixed charge, N_{ox} , were known. The values used in Fig.1 were $C = 2.63 \times 10^{17}$, $k_{cp} = 1.35 \times 10^7$ and $k_{sr} = 7.0 \times 10^{14}$ all expressed in cgs units.

In the model for holes, the value of N_I was unknown. Therefore a fit was carried out to find the optimum value of $C/(N_I + N_{ox}/\langle z \rangle)$ using fixed values of k_{cp} and k_{sr} . This was 0.225 for $k_{cp} = 3 \times 10^6$ and $k_{sr} = 2.22 \times 10^{14}$ all in cgs units. This is the solid line in Fig.2.

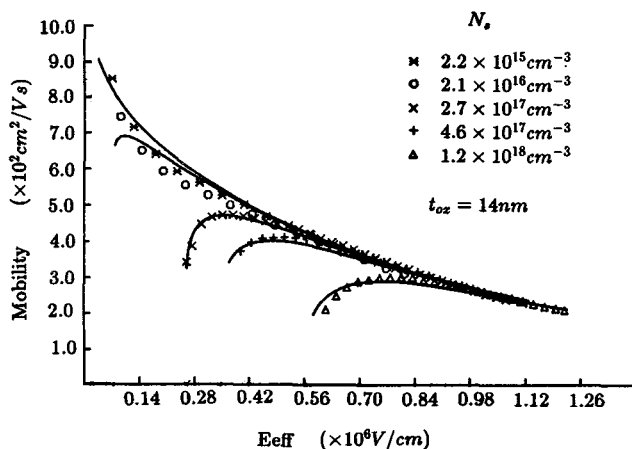


Fig.1 . The low lateral field electron mobility versus the normal effective field for samples with gate oxide thickness and surface doping density as given in the insert. The points are the experimental values while the solid lines are the fits of equation 5 with μ_c , μ_{cp} and μ_{sr} as given in equations 2, 3 and 4.

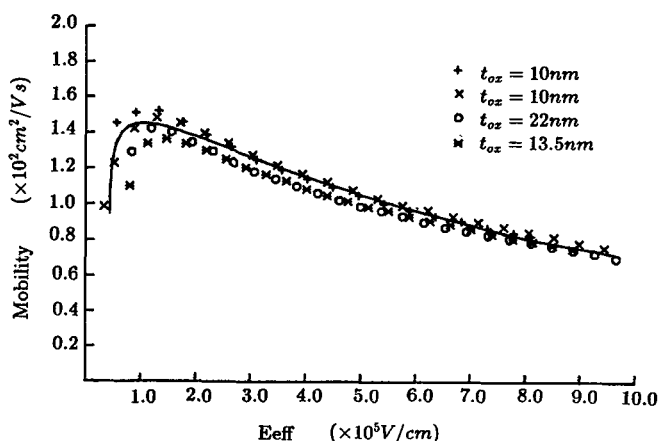


Fig.2 . The low lateral field hole mobility versus the normal effective field for samples with gate oxide thickness as given in the insert. The points are the experimental values while the solid line is the fit of equation 5 with μ_c , μ_{cp} and μ_{sr} as given in equations 2, 3 and 4.

In Fig.3, simulations of a half - micron n-MOS transistor together with experimental data are shown. Good agreement between the calculated and experimental data is observed. Similar data for a buried channel p-MOS transistor are shown in Fig.4. The $I_{ds} - V_{gs}$ characteristics at low V_{ds} are modelled well but systematic deviations in the $I_{ds} - V_{ds}$ characteristics at high lateral fields suggest that the lateral - field model for holes is not accurate at high lateral fields.

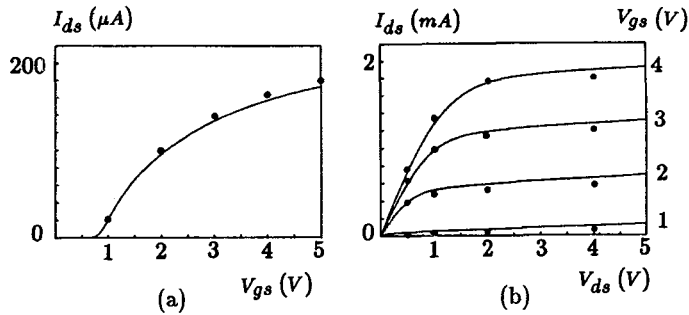


Fig.3. (a) $I_{ds} - V_{gs}$ ($V_{ds} = 0.1V$) and (b) $I_{ds} - V_{ds}$ characteristics of an n-MOS lightly-doped drain transistor with a gate length of $0.53\mu m$ and width of $3.9\mu m$ and gate oxide thickness of $12.5nm$. The dots are calculated data points using the device simulation program.

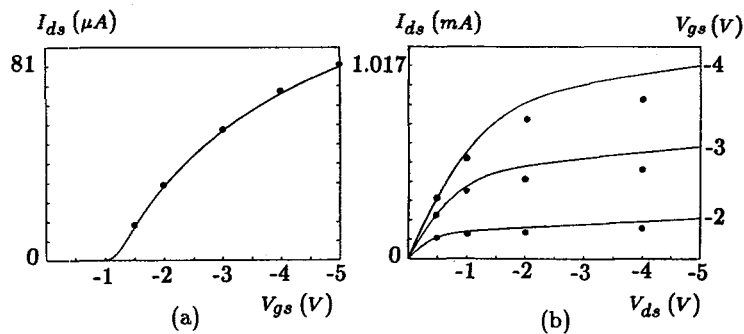


Fig.4. (a) $I_{ds} - V_{gs}$ ($V_{ds} = -0.1V$) and (b) $I_{ds} - V_{ds}$ characteristics of a p-MOS buried channel transistor with a gate length of $0.60\mu m$ and width of $4.2\mu m$ and gate oxide thickness of $10nm$. The dots are calculated data points using the device simulation program.

5. CONCLUSIONS

It appears that a simple mobility model with three parameters can describe a large amount of experimental data. The model was successfully incorporated into a two - dimensional device simulation program which subsequently predicted $0.5\mu m$ MOS transistor behaviour in good agreement with experiment

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