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THE SERIES RESISTANCE OF SUBMICRON MOSFETs AND ITS EFFECT ON THEIR CHARACTERISTICS

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Résumé - Une formule de modèle, liée au procès, pour les résistances série des MOSFETs est présentée, en supposant un profil de dopage linéaire pour des jonctions graduelles. La variable la plus importante du procès est le gradient de dopage latéral, tandis que la dose du drain légèrement dopé n'a pas beaucoup d'influence. Les valeurs calculées des résistances correspondent bien avec les valeurs mesurées, qui ont été extraites des paramètres d'un nouveau modèle de circuit pour des MOSFETs. Dans ce modèle le courant et la tension de saturation sont exprimés explicitement en termes des résistances série.

Abstract - A process-related design formula for the MOSFET series resistances is discussed, assuming a linear doping profile for graded junctions. The main process variable is the lateral doping gradient, whereas the LDD-dose has little effect. Calculated resistance values agree well with measured data, which have been extracted from the parameters of a new MOSFET circuit model. In the latter model the current and saturation voltage are expressed explicitly in terms of the series resistances.

1 - Introduction

In order to maintain a 5.5 Volt power supply in (sub)micron-size MOSFETs, graded source/drain junction profiles are widely used. Although the required reduction of hot carrier effects by this approach has been discussed extensively, little attention is paid to the associated effect of increased series resistance. In graded junctions the largest contribution to R_s arises from current crowding at the channel side (compare Fig. 1). However, when using implicit relations (derived for conventional junctions [1, 2]), to calculate this effect in LDD devices, large deviations from experimental data are found (compare Fig. 2). In this contribution a new process-related design formula for this resistance has been derived, which is based on the assumption of a linear lateral doping profile, in agreement with 2-D process simulation results. Furthermore its effect on the transistor characteristics and performance are discussed.

2 - Calculation of the LDD-MOSFET series resistance

According to the schematic representation of the current pattern of fig. 1, the source/drain series resistance of a MOSFET consists of four components: a contact resistance below the contact window, a sheet resistance, where the current flows along parallel lines, a spreading resistance due to current crowding at the vicinity of the channel end and an accumulation layer resistance owing to gate overlap. The contact resistance R_{co} has been calculated applying a transmission line model to the interface between the metal and the semiconductor [3]. Usually its value and that of the second component are much smaller than the spreading resistance. Using the assumption (based on numerical simulation) that the current converges within an angle of 1 radius from the full junction depth (y_j) to the thin accumulation sheet (thickness y_c), the latter resistance is given by

$$R_{sp} = 0.64 \int_{\cdot 64 y_c}^{\cdot 64 y_j} \frac{\rho dx'}{x'W}, \quad (1)$$

where the constant of 0.64 comes from $1/tg1$. The above integral has been evaluated in case of a uniform junction doping [1] and an exponential profile at the vicinity of the channel [2]. However even in the latter case, for LDD-type devices large deviations from experimental data are found (compare fig. 2). In fact, according to 2-D process simulation and experimental data [4], for the tail of graded junctions a far more linear doping profile applies.

Assuming an accumulation layer to be present between the undepleted junction end ($x = 0$) and ($x = -x_a$) (compare fig. 1), its resistance is simply given by

$$R_{ac} = \frac{x_a}{\mu_{ac}qN_{ac}W}, \quad (2)$$

where qN_{ac} and μ_{ac} are the charge and mobility of this layer, respectively and W is the channel width. Defining a doping profile $N = N_0 - kx$, where k is the lateral doping gradient, according to (1) the spreading resistance is given by

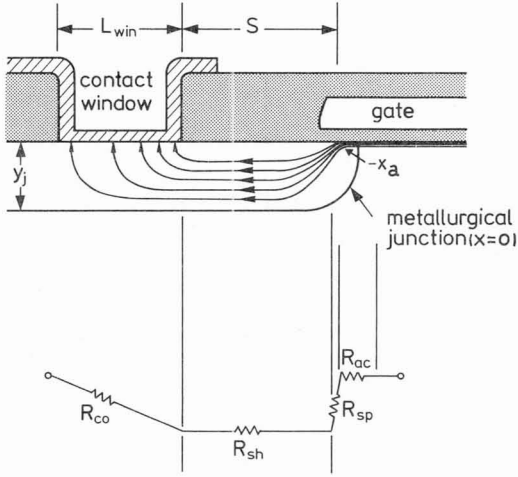


Fig. 1. Schematic diagram showing current pattern in the source region and its associated resistance components.

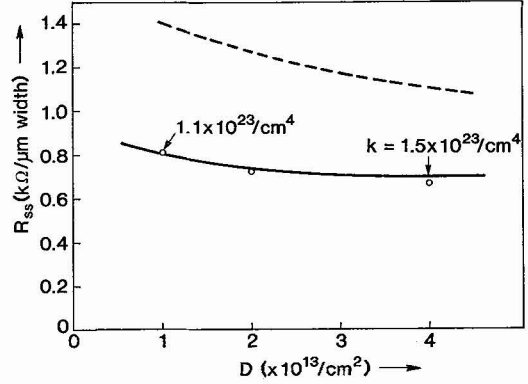


Fig. 2. Source series resistance vs LDD implantation dose. Dots are measured values, lines are calculated values (— = model, - - = ref. 2).

$$R_{sp} = \frac{0.64}{q\mu_s(N_0 + kx_a)} \ln \left[\frac{y_j(N_0 + kx_a)}{y_c(N_0 + kx_a + .64 ky_j)} \right], \quad (3)$$

where μ_s is the average bulk mobility in the tail of the graded junction.

Considering that the total series resistance is determined by the minimum of the sum of R_{sp} and R_{ac} , x_a follows from the condition $d(R_{sp} + R_{ac})/dx_a = 0$. This procedure yields

$$x_a = k^{-1} \left[\{ 0.64(\mu_{ac}/\mu_s) N_{ac}kc \}^{1/2} - N_0 \right], \quad (4)$$

where

$$c = \ln \left[\frac{y_j(N_0 + kx_a)}{y_c(N_0 + kx_a + 0.64 ky_j)} \right].$$

Substituting the latter value in (3), we finally obtain

$$R_{sp} = \frac{0.80c^{1/2}}{qW(\mu_{ac}\mu_s)^{1/2} (N_{ac}k)^{1/2}}. \quad (5)$$

From this result we conclude that the main process variable, affecting the LDD series resistance, is the lateral doping gradient $k = d N_j/dx$, whereas the implant dose has only indirectly little effect. This is shown in fig. 2, where the calculated source series resistance has been plotted. The values of k have been obtained from process simulation. In addition, since μ_{ac} decreases with N_{ac} (V_{GS}), R_{sp} decreases slowly with gate bias [2]. For instance, when V_{GS} is decreased from 4 to 2 Volts, the resistance values of fig. 2 increase by 25%.

3 - Effect of series resistances on the transistor characteristics

Starting from the well-known model equation for a short-channel MOSFET [5], the effect of a source (R_{ss}) and drain resistance (R_{sd}) on the characteristics can be calculated by taking into account the Kirchhoff relations

$$\left. \begin{aligned} V'_{DS} &= V_{DS} - I_D(R_{ss} + R_{sd}) \\ V'_{GS} &= V_{GS} - I_D R_{ss} \end{aligned} \right\} \quad (6)$$

In the above relations V_{DS} and V_{GS} are the external drain-source and gate-source bias. Using the above relations and assuming that for a practical device

$$\beta(R_{ss} + R_{sd}) < 0.50 ,$$

in which $\beta = \beta_0 W/L$ is the MOSFET gain constant, the current equation can be rewritten into

$$I_D = \beta \frac{(V_{GS} - V_T) V_{DS} - \frac{1}{2}(1 + \delta) V_{DS}^2}{1 + \theta_A(V_{GS} - V_T) + \theta_B V_{SB} + \theta_C V_{DS}} \quad (7)$$

In this equation V_T is the threshold voltage, δ is a factor representing the substrate backgate effect and θ_B is a mobility degradation parameter. However compared to the previous model [5] two parameters are present, which are generalisations of the mobility degradation (θ_0) and velocity saturation effect (θ_{co})

$$\theta_A = \theta_0 + \beta(R_{ss} + R_{sd}) , \quad (8a)$$

$$\theta_C = \theta_{co} - \frac{1}{2}\theta_0 - \beta R_{sd} . \quad (8b)$$

Furthermore from the internal saturation condition $d I_D / d V_{DS}' = 0$, the external saturation voltage can be calculated. In this way we obtain

$$V_{DSS} = \frac{2(V_{GS} - V_T)}{1 + \delta} \left[\left\{ 1 + \frac{2\theta_C(V_{GS} - V_T)}{(1 + \delta) [1 + \theta_A(V_{GS} - V_T) + \theta_B V_{SB}]} \right\}^{\frac{1}{2}} + 1 \right]^{-1} . \quad (9)$$

Generally, owing to the presence of R_{ss} and R_{sd} , under the same bias conditions the current is reduced, but the saturation voltage increases.

In principle the model parameters V_T , δ , β , θ_A , θ_B and θ_C can be determined from a comparison between the measured transistor characteristics and calculated model data. Usually V_T and δ are expressed in terms of the zero-bias threshold voltage V_{T0} and a threshold slope factor γ [5]. In addition for a short-channel transistor a drain feed-back effect $V_T = V_{T0} - fV_{DS}$ has to be taken into account. From measuring the characteristics of devices with different gate lengths, according to relations (8a) and (8b) R_{ss} and R_{sd} can be obtained from the slope of θ_A vs β and θ_C vs β plots. However since $\theta_{co} = (L E_c)^{-1}$, where E_c is the velocity saturation field, in the latter case the value of the parameter E_c is required.

4 - Comparison with experimental results

Generally the model equations (7) and (9) represent well the characteristics of MOSFETs with graded junctions. Fig. 3 shows a good fit to the measured characteristics of a device with a $0.5 \mu\text{m}$ gate length. Corresponding values of major parameters are given in the subscript. Next figs. 4 and 5 give the parameters θ_A and θ_C as a function of the gain constant β . The latter has been varied by taking devices with different gate length (compare the insets). In agreement with eqs. (8) a linear dependence is observed. From the slope value and the indicated value of E_c (obtained from non-LDD devices), a value $R_{ss} = 680 \Omega$ and $R_{sd} = 560 \Omega$ per μm gate width has been obtained. Unfortunately owing to additional effects, the accuracy of the above model is not sufficient to provide the gate bias dependence of the series resistances. Therefore the given data has to be considered as an average. However, if the resistance values are determined from the characteristics at low drain bias, a slightly larger value for R_{sd} is observed. This is due to the absence of an accumulation layer at large drain bias.

Following the above procedure, the resistance value has been measured as a function of the LDD-implantation dose. The results for the source resistance are given in fig. 2. Not only agree the measured data well with values calculated according to eqs. (3), (4) and (5), but the weak dependence on the dose D is confirmed too.

Finally fig. 6 gives the decrease in drive current of an optimized LDD-device compared to a conventional type. Owing to compensating effects (a decrease of θ_C and an increase of V_{DSS}) this decrease is less than the direct change in θ_A and θ_C .

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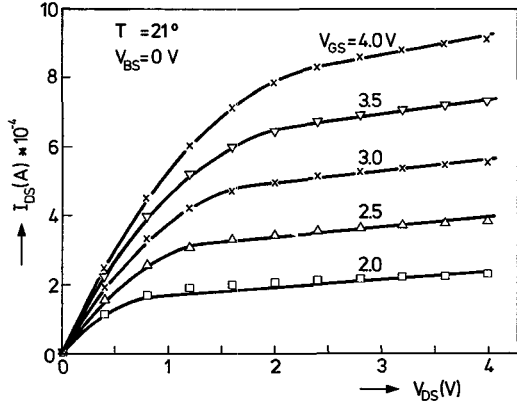


Fig. 3. Measured and calculated characteristics of a 0.5 μm MOSFET. $V_{T0} = 0.70\text{ V}$, $\gamma = 0.10\text{ V}^{1/2}$, $\beta = 1.48\text{ mA/V}^2$, $\theta_A = 0.56\text{ V}^{-1}$, $\theta_c = 0.22\text{ V}^{-1}$, $f = 0.13$.

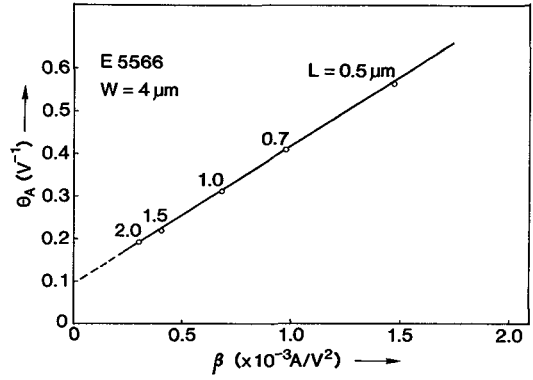


Fig. 4. Model parameter θ_A vs gain factor. The slope yields the value of $(R_{ss} + R_{sd})$.

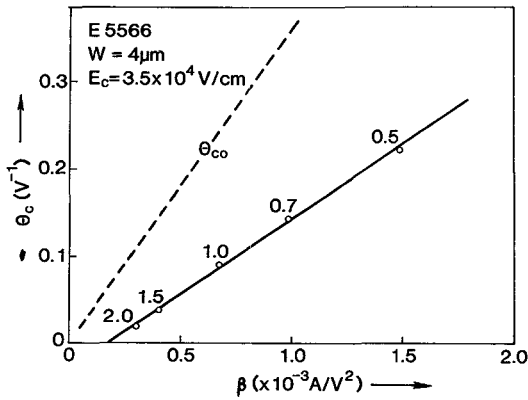


Fig. 5. Model parameter θ_c vs gain factor. From the slope and the velocity saturation field (E_c) the value of R_{sd} is obtained.

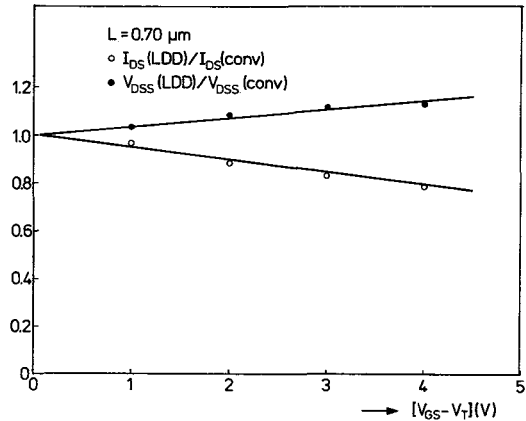


Fig. 6. Change in drain current and saturation voltage of a 0.7 μm - LDD MOSFET compared to a conventional device.