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## TRENDS IN INDIUM PHOSPHIDE MICROELECTRONICS

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**RESUME** - Parallèlement à l'optoélectronique 1,3 - 1,5  $\mu\text{m}$ , et grâce à des propriétés de transport électroniques remarquables, une microélectronique sur les matériaux à base de InP se développe actuellement. Après quelques rappels sur les propriétés des matériaux InP et GaInAs, les diverses structures de transistors actuellement étudiées sont décrites, avec leurs mérites respectifs. Une analyse est ensuite présentée, portant sur les évolutions technologiques et les domaines d'application.

**ABSTRACT** - Together with 1,3 - 1,5  $\mu\text{m}$  optoelectronics, a microelectronic technology is presently developing on InP-based materials, owing to their remarkable transport properties. After general considerations on InP and GaInAs properties, various transistor structures are presented and their comparative merits discussed. This is followed by an analysis of current trends in technology and fields of applications.

### 1 - INTRODUCTION

In the past 15 years, a large interest has concentrated on gallium arsenide (GaAs) devices for both microelectronic (GaAs MESFETs) and optoelectronic applications (AlGaAs/GaAs lasers and LEDs). This technology is now rather well-established, even if digital applications of GaAs MESFETs are unrestly facing progresses in silicon technology. More recently, another III-V material, InP, exhibiting similar potentialities in the fields of optoelectronics and microwave or high-speed applications, has experienced a renewed interest, mainly because of the shift in interest towards higher wavelengths for optical fiber transmissions. In spite of a higher susceptibility of the material to technological treatments than GaAs, InP-based optoelectronic devices are now fabricated and are commercially available. Conversely, no InP-based transistor has established itself as the plow-horse of an InP-based microelectronic technology, although a large research effort is building up worldwide in the investigation of various structures of field effect or bipolar transistors. This should soon result in reliable high-performance devices taking advantage of the attractive electronic transport properties of InP and of GaInAs, a ternary compound which, lattice-matched to InP, exhibits a mobility of more than 10000  $\text{cm}^2/\text{Vs}$ .

### 2 - ELECTRONIC TRANSPORT IN InP AND GaInAs

Like in GaAs, electron mobility in InP and GaInAs is much higher than hole mobility, which favors n-channel FET or npn bipolar structures. With drift mobilities of 4000 and 10000  $\text{cm}^2/\text{Vs}$ , respectively at room temperature, both materials exhibit a similar high drift velocity, of the order of  $2.5 \cdot 10^7$   $\text{cm/s}$  for 1  $\mu\text{m}$  long gate devices (Fig1). This value, somewhat higher than in GaAs, mostly results from the larger separation between  $\Gamma$  and L valleys in the conduction band, confining electrons in the high mobility  $\Gamma$  valley till they gain an energy larger than about 0.5 eV from the electric field. Even for transistors with submicron gate length, this superiority of InP and GaInAs over GaAs is expected to remain valid [1]. Also related to the higher  $\Delta E_{\Gamma L}$  value is the more pronounced negative resistance behaviour used in Transferred Electron (Gunn) Devices (TEDs).

In table I, some parameters of interest regarding electronic properties of InP, GaInAs and AlInAs are given. This third compound is increasingly being used as a high bandgap material to confine electrons in the channel of GaInAs FETs, thanks to the large conduction band discontinuity with GaInAs. Unfortunately good quality AlInAs is difficult to grow by MBE or MO-VPE, with usual mobility in the 1000-2000  $\text{cm}^2/\text{Vs}$  range. Recently figures between 3000 and 4000  $\text{cm}^2/\text{Vs}$  have been reported with both growth techniques; This illustrates the rapid improvement currently experienced in the epitaxial growth of InP-based material. It is also important to emphasize in table I, the small bandgap of GaInAs resulting in its high mobility but also in a low bulk resistivity, high temperature sensitivity and large impact ionization coefficients (fig. 2).

Table 1: Physical parameters of InP and lattice-matched GaInAs and AlInAs.

	InP		GaInAs		AlInAs
$E_G$ (eV)	1.35		0.75		1.45
MOBILITY ( $cm^2/Vs$ )	4000		10000		3500
$\Delta E_{rl}$ (eV)	0.6		0.55		0.61
DRIFT VELOCITY ( $10^7$ cm/s)	2.5		2.5		
BULK RESISTIVITY ( $\Omega cm$ )	$10^8$		$2 \cdot 10^3$		
BARRIER SCHOTTKY HEIGHT $\phi_{Bn}$ (eV)	0.4		0.2		0.6/0.8
$\Delta E_C$ (eV)		0.2		0.55	

3 - KEY ASPECTS OF AN InP-BASED MICROELECTRONIC TECHNOLOGY

While  $n^+$  doped substrates with a very low dislocation density are now available for optoelectronic devices, high quality semi-insulating (S.I.) substrates are not yet available. Because of an insufficient purity of starting materials, the resistivity of undoped crystals is usually only marginal (residual doping : a few  $10^{15} cm^{-3}$  - n type). Semi-insulating material ( $10^7$ - $10^8 \Omega cm$ ) is obtained by compensation of residual donors by Fe atoms with a concentration which increases from seed to queue of the ingot (for instance  $10^{16}$  -  $10^{17} cm^{-3}$ ). Like in Cr doped GaAs, Fe atoms tend to redistribute under annealing, resulting in thermal instability. Moreover a reproducible process for surface preparation (polishing) is not yet perfectly established. Obviously more work is necessary before S.I. substrates of adequate quality becomes available.

Actually most devices are fabricated from epitaxial layers, generally grown on a buffer layer preventing detrimental pollution from the substrate. VPE but more often MO-VPE or MBE are presently used for the growth of these structures. A good homogeneity of the grown layers (composition thickness, doping level) is then necessary not only to maintain the lattice matching condition in the case of heterostructure - which is not critical in the AlGaAs-GaAs system- but mainly to provide a small dispersion in threshold voltage. Very encouraging results have already been obtained in that respect [2] : a deviation of only  $\pm 1.5 \%$  over 2 inch substrates of the sheet carrier concentration.

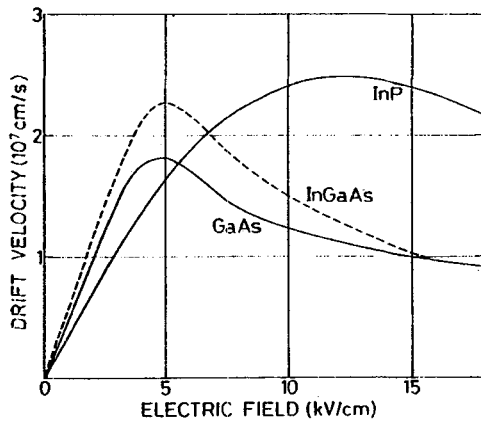


Figure 1: Drift velocity of InP and GaInAs under static electric field.

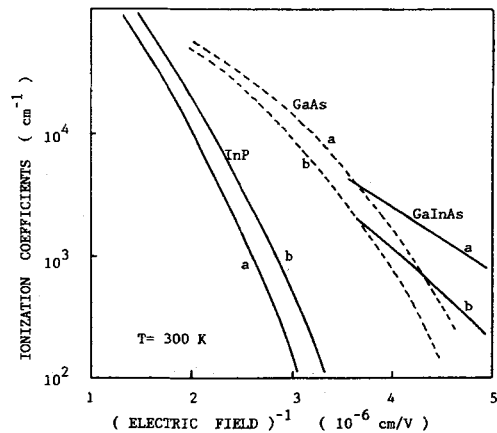


Figure 2: Ionization coefficients for holes(b) and electrons(a) in InP and GaInAs with reference to GaAs

Another important point which illustrates the difficulty faced in establishing an InP microelectronic technology is the material fragility : not only InP is more brittle than GaAs, making the handling of 2 or 3 inch wafers more critical, but also InP, and GaInAs as well, are quite sensitive to bombardment by energetic species as found in usual plasma etching or deposition systems. For instance Ar ion milling of InP surfaces even at low energy (300 V) degrades the material quality and results in the formation of an In rich surface layer unless special care such as cooling the slice at liquid nitrogen temperature is taken /3/. InP, and to a lesser extent GaInAs, also tends to decompose at relatively low temperature with preferential evaporation of the group V element (around 350°C under ultrahigh vacuum for InP /4/). Although this phenomenon can be fought by encapsulation, or phosphorus or arsenic overpressure, it obviously requires adjustments in the processing techniques previously developed for GaAs devices and circuits. Satisfactory techniques for surface protection are now available for diffusion and implantation annealing.

Related to its surface instability, passivation is a very important issue for the reliability of InP-based devices : it is well-known that reverse biased GaInAs p-n junctions, when exposed to atmosphere, tend to degrade with conductive paths appearing at the surface, possibly associated with the formation of an In<sub>2</sub>O<sub>3</sub> conductive layer. This problem has so far received limited answers. Only the development of suitable passivation schemes (PECVD SiN for instance in the case of GaInAs PIN or avalanche photodiodes /5/) allows the developemnt of stable devices. This passivation issue, which also hampered for quite a while the development of a viable GaAs MESFET technology, is now well addressed, partly due to the large interest in establishing a MISFET technology on InP and GaInAs, motivated by the attractive low surface state density observed on these materials.

To conclude this paragraph, a few considerations on metal-semiconductor contacts are now given : with most metals, InP and GaInAs surface tend to be pinned quite close to the conduction band. This has so far hampered the development of a MESFET technology on these materials. It has also partly motivated the use of AlInAs in various FET structure, owing to a larger Schottky barrier height, between 0.6 and 0.8 eV (see Table I). This Fermi level pinning at the surface is also put forward to explain the low and high resistivity of contact on n-type and p-type materials respectively, with some recent improvement in the latter case /6/,/7/. A technology for InP-based microelectronics is still far from being fully established ; but important progress is continuously being made. Such progress is best illustrated by the increase in performance of the various transistor structures presently investigated.

#### 4 - InP FETs

First attempts to develop an InP MESFET technology have met limited success, due to the low Schottky barrier height. Since then, different schemes have been proposed to overcome this situation : for instance by adding a thin dielectric layer between the semiconductor surface and the gate metallization /8/ or more recently by use of a shallow diffusion converting a thin surface layer - completely depleted of carriers in actual operation - to p-type /9/. It has also been shown that by a suitable choice of the gate metal (Cd), a larger Schottky barrier appears /10/. None of these approaches has already established itself as a viable process so far, even though such a technology has been used in the fabrication of a monolithic laser-FET device /11/.

InP junction FETs have also been investigated, in particular with fully ion-implanted structures /12/. A major achievement has been the control of a shallow, abrupt p<sup>+</sup>n gate junction, thanks to a co-implantation process. Submicron gate planar structures are difficult to fabricate, with the requirement of aligning the metal gate onto the p<sup>+</sup>n region. This can be overcome by subsequent etching with the gate metal as a mask. More investigations are still needed to ascertain the viability of this structure (gate contact resistivity, mesa gate passivation) but promising results have already been obtained /13/. It is worth illustrating the potential of InP JFETs by noting that the monolithic receiver with the best sensitivity at 1.3 μm (-36.5 dBm at 200 Mbit/s) has been fabricated with InP JFETs /14/.

However most of the research devoted to InP FETs has so far focused on MISFETs : it was recognized quite early that the interface state density of insulator/InP could be very low, below 10<sup>12</sup>/cm<sup>2</sup> eV, in contrast to the situation with GaAs. Moreover in the prospect of a power transistor, a MISFET structure appears quite attractive. This was actually clearly demonstrated by the excellent results reported on a SiO<sub>2</sub> gate power MISFET : 3 W/mm /15/.

Unfortunately InP MISFETs are prone to large threshold voltage drift, in operation, due to instability of the insulator-semiconductor interface. InP native oxydes, as usually grown exhibit poor dielectric properties. Good characteristics were reported however, with the oxidation of InP through an Al<sub>2</sub>O<sub>3</sub> film /16/. This oxidation scheme leads to the formation

of a polyphosphate insulator, as recently identified. The direct formation of such an insulator by other means is obviously a promising technique /17/. As an alternative to oxidation, both nitridation and sulfidation have been investigated. In spite of an excellent effective mobility ( $3500 \text{ cm}^2/\text{Vs}$ ) characteristic of a low density of fast interface states, the dielectric quality of the thermally grown sulfide insulator doesn't allow the fabrication of transistors with low current drift /18/. Actually it is a second approach to the realization of MISFETs that has received most of the attention : that is the deposition of a dielectric film ( $\text{SiO}_2$ ,  $\text{SiN}$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{PN}$ , ...) using a large number of techniques, from e-beam evaporation to CVD. Most of them lead to a low density of interface states, and then acceptable mobility. However, drain current drift in CW operation, due to trapping and evidenced by hysteresis of C-V MIS diodes characteristics, remains a major obstacle to the development of an InP MISFET technology /19/.

Several criteria to be fulfilled in order to obtain an acceptable MIS structure are now well accepted : a good stoichiometry of the very first atomic layers of the InP surface, implying no high-temperature treatment or surface bombardment creating P vacancies ; a very thin interface layer, requiring in situ etching /20/, possibly As passivation /21/ ; a high quality dielectric. Simultaneous obtention of those characteristics is a real challenge : conventional CVD, indirect PECVD /22/, UV enhanced CVD /23/, flash CVD /24/, have in particular shown much promise in that respect, as evidenced by the reasonable drift behaviour reported with such techniques /25/. Obviously real progress has been made in recent years in the understanding and control of InP MISFETs drift behaviour. Although this problem has not yet received a fully satisfactory answer, continuous improvement is observed (fig.3), opening the door to a MISFET technology, which would be a major breakthrough in III-V microelectronics.

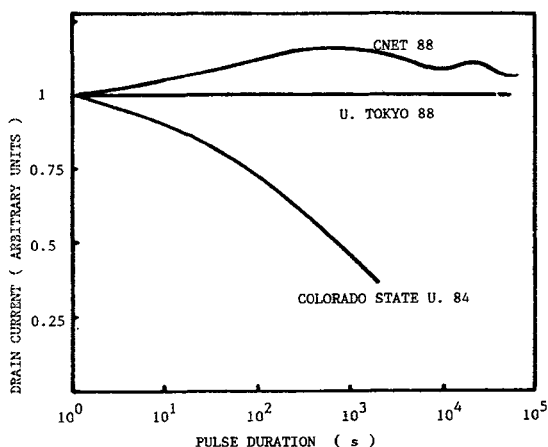


Figure 3: Drift behaviour of the drain current of enhancement-mode InP MISFETs after a 2V step is applied on the gate.  $V_{ds} = 0.1\text{V}$ .

##### 5 - GaInAs FETs

$\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$  lattice-matched to InP is a very promising material, with a high mobility and high saturation velocity. Moreover with a low-bandgap, it is particularly suited for the absorption of light at wavelength of 1.3 and 1.55  $\mu\text{m}$ . For these reasons, GaInAs transistors have received much attention in recent years. But which FET structure is the best is not clear yet, with continuous improvements being reported for the various structures (fig. 4). This progress can be clearly associated to the better quality of material grown by MBE or MOVPE including more efficient buffer layers at the substrate interface. As with InP, GaInAs MESFETs have not received much attention, due to the low Schottky barrier height. A few attempts have been reported recently aiming at artificially increasing the barrier height by inserting a thin insulating layer between the metal gate and the GaInAs channel or by the use of a Cd gate electrode .

The most popular GaInAs structure has long been the homojunction FET (JFET). Many different approaches have been reported for defining the gate : blanket p diffusion or implantation followed by gate layer etching, p-n junction epitaxial growth, selective diffusion or implantation,...with compromise to be found between gate length reduction and gate junction passivation. While selectively diffused or ion-implanted gate may be naturally passivated by the diffusion or implantation mask /26/ /27/, no efficient scheme has yet been reported for mesa etched gate. Better performance can be obtained with

heterojunction FETs (HJFETs) : selective etching of a p<sup>+</sup> InP gate layer down to a gate length of 0.5 μm has already been reported with a f<sub>max</sub> of 60 GHz /28/, but the critical passivation problem has still to be solved.

GaInAs MIS structures, like InP ones, are characterized by a low interface state density (> 10<sup>12</sup> cm<sup>-2</sup> eV<sup>-1</sup>) allowing the fabrication of MISFETs. Moreover, and this is probably attributable to the better surface stability of GaInAs, several Laboratories have already reported a quite acceptable drain current drift behaviour /29/. For instance with a self aligned structure with a SiO<sub>2</sub> UVCVD gate dielectric, a drain current drift of only 2 % in 70 hours has been mentioned /30/, allowing the fabrication of test circuits and microwave transistors with a 45 GHz f<sub>max</sub>. Similar results (3 % in 30 hours) have since been reported on depletion mode GaInAs transistors with SiN gate dielectric deposited in a multipolar plasma after in situ native oxide removal /31/. The MISFET technology, only scarcely addressed till now, obviously offers much promise, in particular for logic applications and optoelectronics.

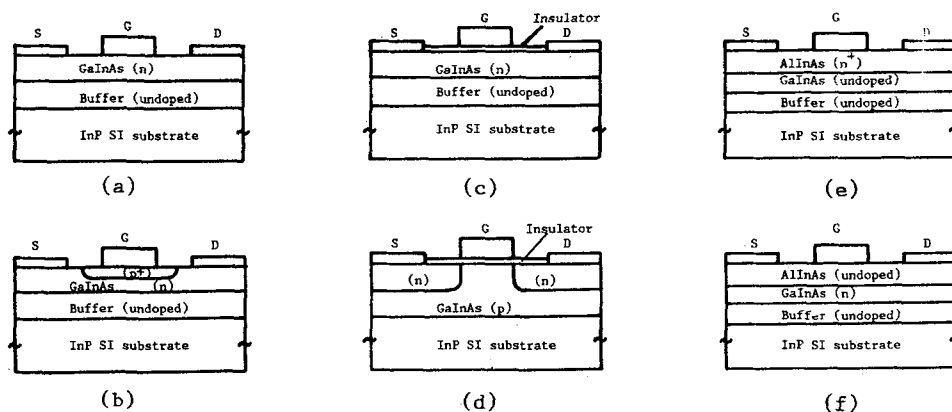


Figure 4: Schematic GaInAs FET structures

- (a): MESFET (c): Depletion-mode MISFET (e): MODFET  
 (b): JFET (d): Inversion-mode MISFET (f): "MIS"FET

In the last 10 years AlGaAs/GaAs heterostructure FETs have been widely studied as an alternative to conventional GaAs MESFETs. Known in their original design as TEGFETs, MODFETs or HEMTs, they showed superior performances in terms of transconductance, cut-off frequency and noise figure. A parallel development has been experienced very recently with AlInAs/GaInAs heterostructure FETs, which offer a major advantage over their GaAs-based counterparts : the conduction band discontinuity, close to 0.55 eV (0.25 eV for usual AlGaAs/GaAs MODFETs) allows a much higher electron sheet concentration (about 3.10<sup>12</sup> cm<sup>-3</sup>) while preventing a parasitic channel to appear in the AlInAs barrier over a wider range of bias condition ; only drawbacks : a slightly lower Schottky barrier height (0.6-0.8 eV depending on AlInAs quality) and a material which has not yet reach the quality of AlGaAs. Several Laboratories have developed such heterostructure FETs which already outperform their GaAs counterparts of comparable gate length /32/. Since the report by NEC of a transistor with a transconductance of 440 mS/mm at room temperature, progress has been very fast, in particular with respect to high frequency performances (fig. 5). Recently devices with 1080 mS/mm transconductance and 175 GHz transition frequency for 0.1 μm gate length, with a minimum noise figure of 0.8 dB at 63 GHz (AG : 8 dB) for 0.2 μm gate length were reported /33/.

While the MODFET structure uses a doped barrier, which can act as a parasitic channel and be responsible for a high gate leakage current, other designs have been studied, directly derived from the AlGaAs/GaAs experience, with an undoped barrier, such as the inverted MODFET and the "MISFET". Such structures usually exhibit lower gate current, lower transconductance and gate capacitance than conventionnal MODFETs. Still their high frequency performance remains very attractive, as illustrated by the 100 GHz f<sub>max</sub> reported by Bendix for a 0.7 μm long gate structure with a 200 Å thick channel doped to 4.10<sup>18</sup> cm<sup>-3</sup> /34/. With a more conventionnal channel (1000 Å with 2.10<sup>17</sup> cm<sup>-3</sup> doping) a 40 GHz f<sub>max</sub> was obtained at CNET-Bagneux on 1 μm gate length devices /35/. Moreover a very good uniformity is expected for undoped barrier FETs with a conduction band discontinuity close to the Schottky barrier height ; this is an important point for circuit

applications. Worth mentioning in the prospect of circuits are the 280 mS/mm transconductance and near-zero threshold voltage reported by Sony on self-aligned refractory gate devices with 5  $\mu\text{m}$  gate length /36/.

While improvement in AlInAs/GaInAs heterostructure FETs growth and processing is continuing, first promising results were reported recently with identical structures but for an InP channel : on 1  $\mu\text{m}$  gate devices with a doped channel a transconductance of 155 mS/mm was measured and an  $f_{\text{max}}$  of 42 GHz inferred from S parameters measurements /37/. With pseudomorphic AlGaAs/GaInAs, heterostructure FETs as an example, pseudomorphic AlInAs/GaInAs, AlInAs/InP, AlGaAs/InP, GaInP/GaInAs have also been investigated; No clear improvement in performance as compared to lattice-matched devices has been demonstrated so far.

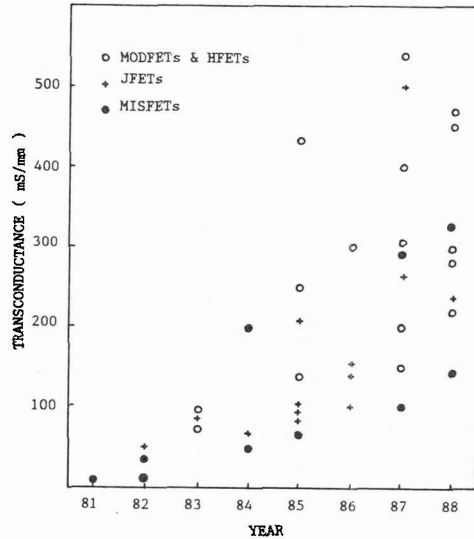


Figure 5: Increase in transconductance over the years illustrating the improvement in material quality. Only FETs with gate length  $>0.5$  micron have been considered.

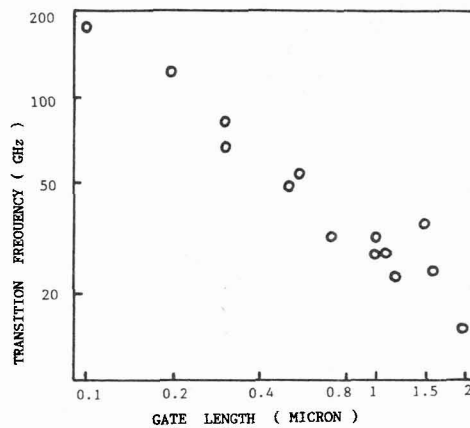


Figure 6: Variation of the transition frequency of GaInAs FETs with different structures versus gate length.

## 6 - GaInAs HETEROJUNCTION BIPOLAR TRANSISTORS

Bipolar transistors can also be fabricated from InP-based materials : as in Si or GaAs, they offer potential improvement over FETs in terms of drive capability, threshold voltage homogeneity, at the expense of a more complex processing technology. While the AlGaAs/GaAs HBT technology is now developing rapidly, the same HBT technology can also be envisioned on InP-based materials, with the associated advantages : low base sheet resistance, low emitter capacitance. With different material combinations available for the fabrication of HBTs, most investigations have rapidly concentrated on npn structures with a GaInAs base, and either GaInAsP or AlGaInAs emitter. These bipolar transistors have very interesting potentialities ; actually recent developments in the AlGaAs/GaAs HBT technology have shown that the device speed is now approaching a limit set by the transit time of electrons through the base and collector. The superior transport properties of InP-based materials could then allow an extension of the frequency range of operation of HBTs, with the additional advantage for circuit applications of a lower emitter-base voltage. Also of interest are the better behaviour of InP/GaInAs HBTs at low current density, resulting from the lower surface recombination velocity. This, as well as the invertibility of wide-bandgap emitter and collector, may be especially interesting in I<sup>2</sup>L circuits.

However, the HBT technology is far more complex than the FET's one, and many technological problems have to be solved before a viable technology is established : abrupt p-n junctions, graded heterojunctions, isolation, passivation, non-diffusing contacts, ... Very promising results have already been obtained, in particular InP/GaInAs DHBTs grown by gas source MBE with a transition frequency of 18 GHz for 5 μm emitter stripe width /38/, and devices grown by MOVPE with a current gain of 11000 /39/. In the AlGaInAs/GaInAs system, a current gain of 1200 and a transition frequency of 1.7 GHz for devices with 20 μm emitter stripe width have been measured /40/. Undoubtedly, these characteristics will soon be improved, taking into account the general improvement of the technology of InP-based materials.

## 7 - FROM DEVICES TO CIRCUITS

An important point has to be made : no InP-based microelectronic device or circuit, with the exception of microwave Gunn diodes, has yet been developed, sold or used in systems, although a few companies intend to do so shortly. For the time being, most efforts are devoted to the demonstration of the feasibility of transistors or circuits. Low complexity circuits have been fabricated for demonstration of either logic or optoelectronic functions. Between 1980 and 1984 several InP MISFET ICs have been reported in the United States under Navy funding /41/. Such circuits were not able to operate DC, because of the drift in transistor characteristics. More recently GaInAs FET ICs have also been reported (GaInAs MISFET ring oscillator with a propagation delay time of 50 ps/gate /42/, GaInAs JFET base band amplifier). Most attention is presently focusing on using AlInAs/GaInAs heterostructure FET for digital ICs. In spite of a report by NEC on the dispersion of the sheet carrier concentration over a 2 inch wafer, almost no data is presently available on the threshold voltage dispersion of processed transistors. The quality of AlInAs material for instance is probably not yet sufficient to allow a reproducible threshold from wafer to wafer. A larger number of reports is now available on the use of InP-based transistors in optoelectronic circuits. Since the first demonstration in 1979 of an IC associating one GaInAs PIN and one FET /43/ a large interest has developed in the area of InP-based OEICs, particularly in Japan. A variety of InP and GaInAs FETs, and even bipolars, have been used in the fabrication of laser drivers or photodetector amplifiers. This large interest originates mainly from the expected improvement in performances, resulting from the reduction of interconnection reactances, as well as in cost and compacity. However the fabrication of high performance OEICs has so far been hampered by the necessary compromising for integrable structures of optoelectronic and microelectronic devices. Very significant achievements have been reported however, on either simple receiver circuits associating a photodiode and a transistor /44/ or even more complex circuits as recently reported by ATT Bell (GaInAs PIN plus 8 InP JFET amplifier /14/). Very informative is the analysis of the current trend in the increase in performance of monolithic photoreceivers : the sensitivity is steadily improving by about 2.5 dB/year since a few years and within 2 years from now, monolithic receivers should surpass their hybrid counterparts. Quite interestingly, a parallel evolution is presently observed with GaAs OEICs, with the recent report of a GaAs receiver exhibiting a sensitivity of -39 dBm at 250 Mbit/s, equivalent to the one of non-avalanching diode hybrid receivers at 0.85 μm wavelength /45/.



A similar evolution is observed with monolithic transmitters for which increasing bandwidths are being reported /11/. The variety of transistors, with InP or GaInAs channel used in these demonstration circuits still illustrates clearly the current uncertainty as to which transistor structures are the more promising.

#### 8 - PROSPECTS FOR AN InP-BASED MICROELECTRONICS

The InP-based microelectronics is still in its infancy, but it is rapidly maturing as evidenced by the improvement in basic characteristics such as transconductance and bandwidth. Most recent reports refer to GaInAs channel FETs which benefit from simultaneous developments of high quality epitaxial growth techniques required for optoelectronic devices and of a mature AlGaAs/GaAs Schottky gate technology. Actually, for many years, and in spite of the known promising characteristics of InP, the motivation for developing an InP-based microelectronics was not strong enough to allow a sensible development. Only with the advent of 1.3 - 1.5  $\mu\text{m}$  optoelectronics did InP-based microelectronics experience a real development. Also very important is the fact that the GaAs microelectronics expertise can quite directly be used for InP compounds /46/.

Thus supported by optoelectronics and GaAs technology, InP-based microelectronics is still facing specific problems : In the area of technology, several points still require particular attention, such as high quality (undoped ?) semi-insulating substrates, low temperature, low energy processing techniques, passivation ; but most importantly it will be necessary to concentrate future development on a limited number of transistor structures. In that respect more work has still to be done to ascertain the viability of structures with a GaInAs channel under operating conditions of real circuits; Beyond that point, the choice of the best structure is still an open question. For InP and GaInAs MISFETs, experiencing a real improvement of the stability of their threshold voltage, the prospects now look better, but much time is still necessary before a reproducible, industrial processing technology is established. Presently JFETs are quite appealing because of their simplicity. Good results have already been reported, and small complexity circuits have been fabricated. Heterostructure gates can possibly improve JFETs performances ; however heterostructure FETs of the MISFET type, or MODFETs, are more likely to become the preferred transistors either with InP or GaInAs channels. HBTs are also very attractive, but since they require an involved processing technology, it will take much time before they begin to challenge their AlGaAs/GaAs counterparts.

Optoelectronic integration is obviously a promising field of application for InP-based microelectronics. Fabrication of OEICs with acceptable yield will require adjustments in transistors structures and processing to ease integration with optoelectronic devices /47/. Competition might come from mis-matched epitaxy approaches, illustrated by the realization of GaAs/InP transmitters and receivers by NEC /48/. In the field of microwave applications, two areas of interest have to be considered : for low-noise amplification, AlInAs/GaInAs MODFETs already begin to challenge their AlGaAs/GaAs counterparts and will continue to do so, with industrial development likely to appear soon. For power microwave amplification, InP has already shown its potentialities. Unfortunately InP MISFETs used for such demonstration suffered from threshold voltage drift. While some progress is now observed on this point, other structures (JFETs and even MESFETs) are also investigated as alternatives, with the same potential for high power although probably with inferior performance in linearity. Finally one should not forget the excellent negative resistance properties of InP and GaInAs and of AlInAs/GaInAs barriers which may in the future allows new development in microwaves or digital applications /49/, /50/.

#### 9 - CONCLUSION

Transistors made from InP compounds have already shown very attractive performances, mainly for microwave and optoelectronics applications. Still some basic work has to be carried on to establish suitable technologies and even to define device structures. Using the same tools as developed for GaAs ICs and for 1.3 - 1.5  $\mu\text{m}$  wavelength optoelectronic devices, InP-based transistors are now able to enter the world of applications in both microwaves and optoelectronics. A few laboratories, in particular in Japan, are even already addressing the question of digital applications of GaInAs FETs. In Europe, several Laboratories are also engaged in research programmes, partly under EEC funding, aiming at establishing a viable InP-based microelectronics technology.

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