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ELECTRICAL PERFORMANCES COMPARISON OF SEMI AND FULLY RECESSED ISOLATION STRUCTURES

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Résumé - Les caractéristiques de structures d'isolation LOCOS semi-enterré et LOCOS enterré ont été analysées. En particuliers, les simulations bidimensionnelles couplées de technologie et de dispositif, réalisées avec le logiciel IMPACT, ont démontré l'influence de l'interface Si/SiO₂ sur les performances d'isolation. Un excellent accord simulation-expérimentation a été trouvé pour les structures étudiées.

Abstract - Electrical characteristics of semi-recessed and fully-recessed LOCOS isolation techniques are analyzed. Two-dimensional process/device simulations, performed with the IMPACT package, have demonstrated the effect of the Si/SiO₂ interface shape on isolation efficiency. An excellent agreement has been found between simulations and measurements for the studied structures.

I - INTRODUCTION

Device isolation presents critical aspects for circuit packing density in VLSI. LOCAL Oxidation of Silicon (LOCOS) is classically limited by the bird's beak extension and lateral diffusion of the channel stop region into active transistor area. Several technological alternatives were proposed to control lateral growth of oxide, such as SILO technique (Sealed Interface Local Oxidation) by using successive silicon nitride and deposited oxide layers /1,2/. In order to evaluate a new isolation process, numerous technological and device physics aspects have to be investigated to clarify important two dimensional (2D) parasitic effects /3/. So the use of coupled process/device simulations is of prime necessity. This paper proposes a comparison of electrical performances for both semi and fully-recessed isolation structures by means of process-device simulations and experimental results. A special attention has been devoted to the bird's beak shape description to demonstrate the electrical implications induced by geometrical effects. An advanced version of the IMPACT3 device simulator extended for isolation structure modeling linked to the IMPACT2 /4/ process simulator was extensively used for two dimensional electrical analysis.

II - PROCESS DESCRIPTION

Table I outlines the main characteristics of the isolation structures that has been investigated. SEM cross-sectional views of both structures are shown in figure 1. For each of them, two versions have been fabricated:

- an aluminium gate version for which a 0.5 micron poly-silicate-glass (PSG) layer was deposited prior the aluminium level. (figure 2)

- a polysilicon gate version. In this case, the n⁺ diffusion regions are self-aligned to the polysilicon. A 550 Å thick oxide layer of about 3 microns long exists between the field oxide mask and the edge of the poly mask. (figure 3)

III - ISOLATION PROPERTIES

The major difference between the semi-rox and the full-rox structure is the bird's beak shape. Because the junctions are shallower than the planar part of the

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Si/SiO₂ interface, the oxide corners are incorporated into the channel region. Figures 4 and 5 show the potential variations along the interface for both structures with a polysilicon gate. Different barrier deformations are observed when the gate bias affects sufficiently the interface potential distribution. Indeed, the potential barrier of the fully-recessed structure is then located under each bird's beak corner, but remains spread over the whole field oxide interface in the case of the semi-recessed structure. Because the current in the overall structure is controlled by electron emission over the potential barrier at the source side, the fully-recessed device shows better isolation properties than the semi-recessed one. This point is illustrated by the ID-VG characteristics for both aluminium and polysilicon gates (resp. figures 6 and 7). Notice that an excellent agreement is found between measured and calculated drain currents that validates the simulation approach.

Further simulations have been carried out on 2 and 7 microns long aluminium gate devices without the PSG layer, for a 5 volts drain bias condition. Characteristics plotted in figure 8 demonstrates the sensitivity of the semi-recessed isolation structure to the n⁺ to n⁺ spacing (L). By opposition, the fully-recessed structure does not reveal this typical 1/L dependence in the subthreshold mode of operation. Indeed, the effective channel length is in this case reduced to the curved part of the field oxide interface and makes the whole parasitic transistor dominated by the two corner devices.

IV - SENSIBILITY TO DIBL EFFECT

The simulations performed on a 2 microns long device have allowed to analyze the effect of Drain Induced Barrier Lowering (DIBL) combined to the corner effect. The drain bias modulates the potential distribution around the n⁺ diffusion and first affects the potential barrier in the corresponding region. As the curved part of the interface located on the drain side requires more band bending to invert because of the influence of the drain controlled depletion region, the channel is firstly formed in the source region (figure 9). Figure 10 illustrates the potential distribution along the interface for gate bias varying from 0 to 15 volts. This result shows, once again, how the newly located potential barrier leads to a better immunity against the DIBL effect, for the full-rox isolation structure.

CONCLUSION

The presented results obtained from coupled process-device analysis have outlined the sensitivity of isolation structure to the field oxide shape. As the corner effect provides better characteristics for threshold voltage, subthreshold slope and drain voltage dependence, buried oxide isolation structures with sharpened corners appear as a valuable solution for micron and submicron technologies. Moreover, the experimental characteristics of the studied structures have revealed to be in good agreement with two dimensional numerical modeling, and have proved the capabilities of the IMPACT simulation tool to investigate physics of new isolation structures.

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FIGURE 1 : SEM CROSS-SECTIONAL VIEWS OF THE FIELD OXIDE EDGE
SEMI-RECESSED STRUCTURE FULLY-RECESSED STRUCTURE

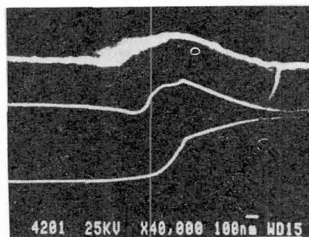
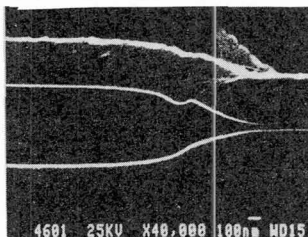


TABLE I

	Semi-Rox Structure	Full-Rox Structure
Field Implant	2 10 ¹³ cm ⁻² at 25 Kev	2 10 ¹³ cm ⁻² at 25 Kev
Field Oxidation	1000° C 220 mn	950° C 370 mn
Oxide thickness	716 nm	735 nm
S/D implant	5 10 ¹⁵ cm ⁻² at 140 Kev	5 10 ¹⁵ cm ⁻² at 140 Kev
Annealing	950° C 45 mn	950° C 45 mn

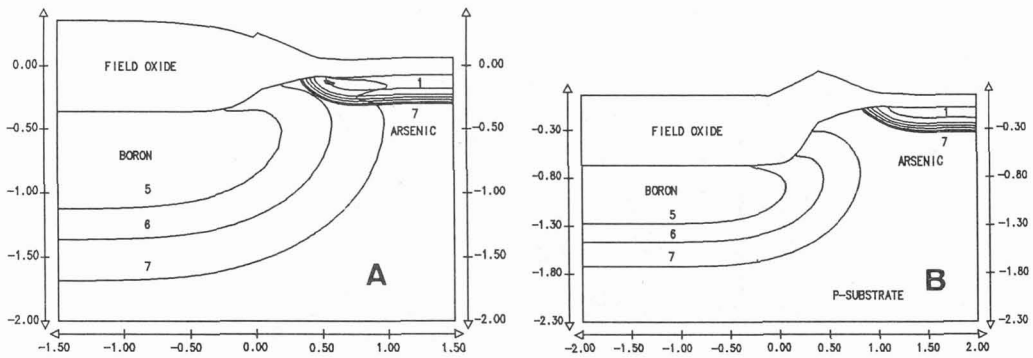


FIGURE 2 : ALUMINIUM GATE STRUCTURES 2-D IMPURITIES EQUI-CONTOURS LINES
 (A) SEMI-RECESSED STRUCTURE (B) FULLY-RECESSED STRUCTURE

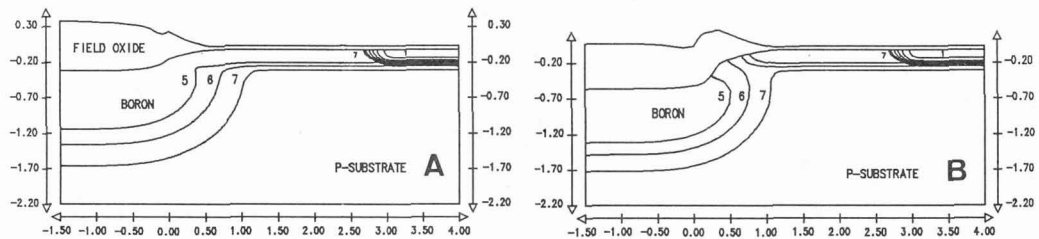


FIGURE 3 : POLYSILICON GATE STRUCTURES 2-D IMPURITIES EQUI-CONTOURS LINES
 (A) SEMI-RECESSED STRUCTURE (B) FULLY-RECESSED STRUCTURE

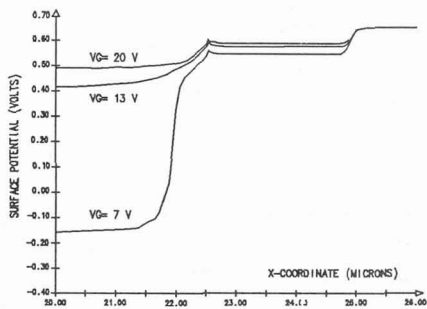


FIGURE 4 : SEMI-ROX STRUCTURE INTERFACE POTENTIAL DISTRIBUTION FOR POLYSILICON GATE DEVICES ON DRAIN SIDE
 $V_{\text{drain}} = 50 \text{ mVolts}$, $V_{\text{bulk}} = 0 \text{ Volt}$, $V_{\text{source}} = 0 \text{ Volt}$, $W/L = 100/20$

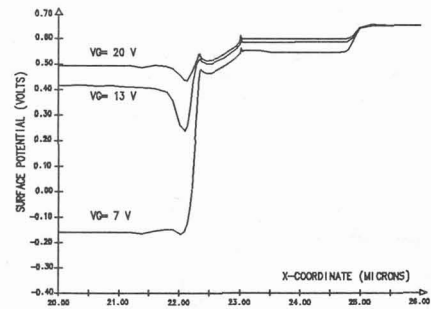


FIGURE 5 : FULL-ROX STRUCTURE INTERFACE POTENTIAL DISTRIBUTION FOR POLYSILICON GATE DEVICES ON DRAIN SIDE
 $V_{\text{drain}} = 50 \text{ mVolts}$, $V_{\text{bulk}} = 0 \text{ Volt}$, $V_{\text{source}} = 0 \text{ Volt}$, $W/L = 100/20$

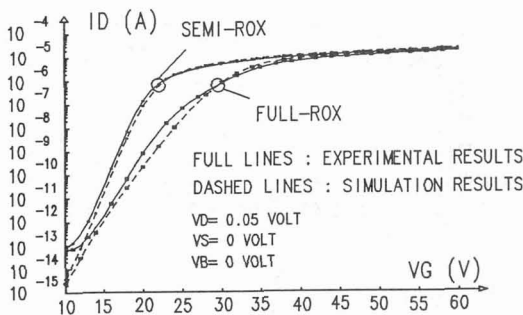


FIGURE 6 : ALUMINIUM GATE VERSION SIMULATED AND MEASURED I_D - V_G CHARACTERISTICS
 $W/L = 100/20$

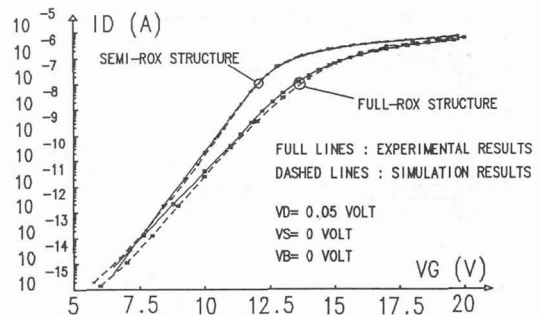


FIGURE 7 : POLYSILICON GATE VERSION SIMULATED AND MEASURED I_D - V_G CHARACTERISTICS
 $W/L = 100/20$

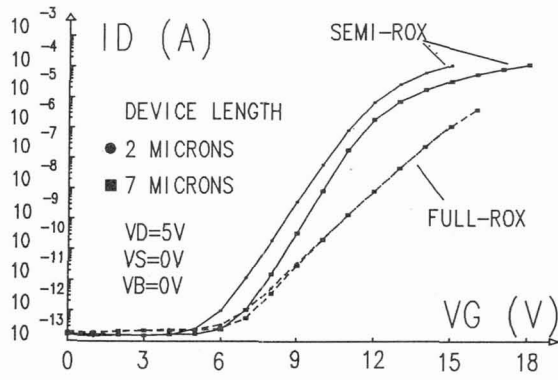


FIGURE 8 : CALCULATED ID-VG CURVES FOR DIFFERENT DEVICE LENGTHS
 $V_{source} = 0$ Volt , $V_{bulk} = 0$ Volt , $V_{drain} = 5$ Volts
 $W = 100$ Microns

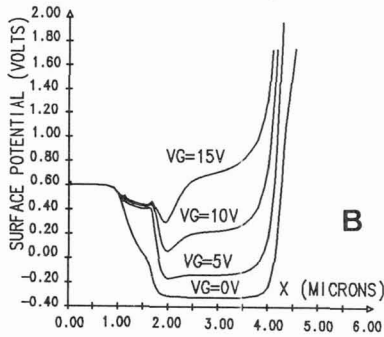


FIGURE 9 :
 POTENTIAL DISTRIBUTION
 ALONG THE INTERFACE

$V_{source} = 0$ VOLT
 $V_{bulk} = 0$ volt
 $V_{drain} = 5$ volts
 $V_{gate} = 0,5,10,15$ volts
 $L = 2$ microns

(A) SEMI-ROX STRUCTURE
 (B) FULL-ROX STRUCTURE

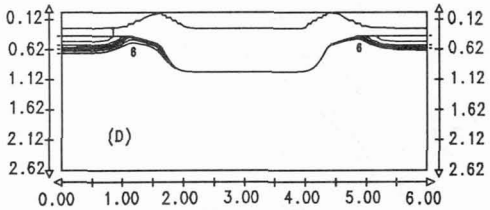
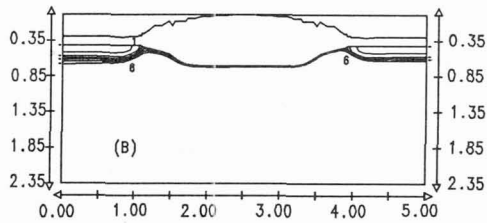
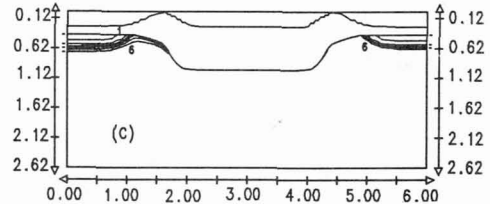
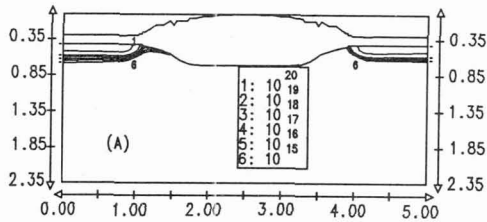
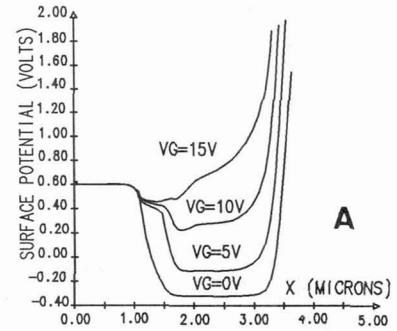


FIGURE 10: ELECTRON DENSITY DISTRIBUTION DURING CHANNEL FORMATION

$V_{source} = 0$ volt , $V_{bulk} = 0$ volt , $V_{drain} = 5$ volts

SEMI-ROX STRUCTURE : (A) $V_{gate} = 5$ volts , (B) $V_{gate} = 15$ volts
 FULL-ROX STRUCTURE : (C) $V_{gate} = 5$ volts , (D) $V_{gate} = 15$ volts