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HOT CARRIER SENSITIVITY OF MOSFET'S EXPOSED TO SYNCHROTRON-LIGHT

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<u>Abstract</u> - The influence of synchrotron-light irradiation for p- and n-channel MOSFET's on their sensitivity to hot carrier degradation was investigated. The radiation induces additional interface states and a positive oxide charge. Annealing at 450°C reduces the interface state density to its initial value but not the oxide charge. A hot carrier stress can compensate this remaining charge by trapping electrons. This effect produces an enhanced shift of the threshold voltage compared to non-irradiated devices. After compensating all of the charge due to the irradiation the devices have a degradation behavior comparable to the non irradiated ones.

1 - INTRODUCTION

X-ray lithography is expected to become important for the realization of MOSFET's with submicron channel lengths. X-rays however are damaging the oxide by the generation of interface states and positive oxide charges. An complete annealing is possible only at elevated temperatures. Yet after the metallization of the wafer with aluminum the highest applicable temperature is 450°C. Using X-ray lithography for structuring the aluminum, an annealing of the irradiation at a subsequent temperature step of less than 450°C is often incomplete. The amount of the remaining positive oxide charge proves different for various technologies.

A highly detrimental behavior of short channel MOSFET's is the effect of degradation by hot carriers, which has been proven to be enhanced for devices exposed to ionizing radiation. This correlation was recently shown for n-channel MOSFET's, which were irradiated by a 10 KeV-X-ray source /1/.

In our experiments the degradation of hot carrier stress for p- and n-channel MOSFET's exposed to synchrotron-light was investigated. The wavelengths of the radiation facility at the BESSY laboratory IMT in Berlin are ranging between 0.3 and 1.5 nm. The temperature at the subsequent annealing process was 450°C, the highest permitted value for a fully processed wafer. The stress behavior of these MOSFET's was compared to devices, which were not subjected to the radiation and annealing procedure.

2 - DEVICE PREPARATION AND MEASUREMENTS

An overview of the whole experimental procedure is given in Fig. 1. The test devices are available on a 4"-wafer. The interface trap density was determined by the charge pumping technique. The single steps of irradiation, annealing and hot carrier stress are described in the next sections:

i. Irradiation

The conditions at the radiation process were chosen to be comparable to a usual exposure step for X-ray resists (e.g. power, time, geometry).



Fig. 1: Flowchart and parameter of the experimental procedure

In Fig. 2 the transfer characteristics of the p- and n-channel devices before and after irradiation with synchrotron-light are given. The shift of the threshold voltage is the same for both p- and n-channel devices. The increase of the interface state density can be deduced from the change of the subthreshold slope.



Fig. 2: Transfer characteristics of p- and n-channel MOSFET's before and after irradiation with synchrotron light

ii. Annealing

The annealing of the radiation damage was carried out at 450 °C in N₂ ambient for 15 min. The density of the interface traps reaches the initial value. For a lot² of the devices the positive oxide charge was not completely reduced.



The stress condition for the p-channel MOSFET was V_G = - 2.5V at a drain current of I_D = -40mA. The n-channel device was stressed at V_G = + 4V and I_D = 40mA. The duration of the stress was 1 min for both MOSFET-types.

3 - RESULTS AND DISCUSSION

In table I the values for the threshold-voltages ${\rm V}^{}_{\rm T}$ and interface trap densities ${\rm D}^{}_{\rm it}$ are listed.



Table I: Average values of threshold voltage V_T and interface traps density D_{it} after different treatment (referring to one wafer each).

Fig. 3 schematically displays the course of the threshold voltage $V_{\rm T}$ during the experimental procedure. The lower curve of both devices applies to hot-carrier-stress with preceding irradiation/annealing treatment, the upper ones apply to hot carrier stress only.



Fig. 3: Threshold voltage after different treatment

After annealing the threshold voltage tends towards the preradiation value. The amount of this change depends on the time and temperature of the annealing step. Often there is no complete reduction of the positive oxide charge producing a threshold voltage more negative than the initial value. A subsequent hot carrier stress gives rise to a neutralisation of the residual charge. Therefore the threshold voltage shift is enhanced within the initial phase of stressing. Because of the different threshold voltages at the beginning of the stress the effective gate voltage was adjusted according to equivalent hot electron stress conditions.

Fig. 4 displays the shift ΔV_T stress after a hot electron stress of 1 min as a function of ΔV_T anneal, which is the difference between the threshold voltage after annealing and the pre-irradiation value and an indication for the quality of the annealing process.



Fig. 4: Threshold voltage shift ΔV_{T} , stress after a hot electron stress versus the difference ΔV_{T} , anneal between the threshold voltage after annealing and the pre-irradiation value. ΔV_{T} , anneal results from the remaining positive charge after irradiation and annealing.

From Fig. 4, it is apparent that devices with a higher amount of residual positive charge have a higher shift in threshold voltage for the same stress conditions. After neutralisation of this charge the MOSFET will show a stress behavior equal to a non-irradiated MOSFET. This fact can be taken from the time dependence of threshold voltage during hot electron stress given in Fig. 5.





4 - CONCLUSION

An enhanced sensitivity to hot electron stress for devices priorly exposed to synchrotron light was observed. This effect is caused by a positive charge generated by irradiation and remaining in the device after an incomplete annealing process at 450°C. This charge will be compensated by the hot electrons injected into the oxide resulting in a significantly higher threshold shift at the starting phase of stressing. This phenomenon was observed for both pand n-channel MOSFET's. A complete annealing procedure at temperatures applicable to fully processed wafers can overcome this enhanced stress effect.

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