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POWER MOS FET MODELS FOR "SWITCHING" CIRCUITS

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RESUME: Un modèle compact du transistor VDMOS de puissance, compatible avec le logiciel "SPICE2", est proposé. En tant qu'applications, le transistor est "simulé" en régime de commutation sur des charges résistives et inductives et les résultats obtenus sont validés par des mesures expérimentales.

ABSTRACT: A compact model of the Power VDMOS Transistor compatible with the circuit simulator "SPICE2" is described in this article. This model is applied to the simulation of switching circuit with resistive and inductive loads; comparisons with experimental results are presented.

I. INTRODUCTION:

In the Power Mosfet area, several suggestions on equivalent circuit have been recently published by International Rectifier [1], Motorola, RCA [2] Siemens [3] and the Washington University [4]. It consist in rather specific models obtained by identification of some electrical characteristics: for a given model, the application domain is not valid simultaneously for DC and dynamic operation, as well as for resistive and inductive loads. These models can use two active components from the SPICE library which are the MOS and the JFET; the use of the later for simulating the "quasi-saturation" phenomenon [5, 6] is no more useful, today, for the modeling as actual structures are optimized in which this phenomenon now appears only for drain current level over the nominal current rating.

In this paper, we describe a basic but accurate model for switching circuits with resistive and inductive loads. This model is compatible with the well known "SPICE" software. It works as well as with low voltage structures (one hundred of volts) of both standard and Logic Level (L^2 FET [5] with a nominal gate source voltage of 5 volts) types, with medium voltage (100 - 500 volts) and high voltage devices (>500 volts). Its configuration is based on a more complete but also more difficult to handle model [8-10] whose parameters are all related to the physical properties and topology of the VDMOS transistor. Their values can be obtained from datasheets and thanks to some "classic" measurements. It must be pointed out that this model takes into account the high degree of non linearity of the gate-drain and drain-source capacitors and also some short channel effects (variable mobility, etc...) which mainly prevail in the low and medium voltage structures.

II - DESCRIPTION OF THE VDMOS TRANSISTOR MODEL:

II-1 - VDMOS'T structure and model topology:

The model structure is directly related to the power VDMOS geometrical topology (see Fig.1). We can notice on the schematic: i) the intrinsic transistor (conduction channel) represented by the current generator J_d , ii) the n-type layer between the p wells with the access resistance R_a to the channel and the highly non linear gate-drain capacitor C_{gd} , i.e. the depletion capacitor C_d in series with the thin gate oxide capacitor C_{gdmax} , iii) the low doped n-type epitaxial bulk accounted for by the drift resistance R_d , the pn junction capacitor C_{ds} with the p well and the internal body diode D_{body} , iv) the gate metallization covering over the N^+ source diffusion which creates, through the thin and thick oxide, a constant parasitic capacitor C_{gso} . When the MOS transistor goes through a switching phase, all the three different modes: Blocked, Ohmic and Saturation, are involved. The model (see Fig. 2) takes into account these three functioning modes. In the figure 2, the conduction channel under the gate, i.e. the intrinsic transistor, is described by the current generator J_d and the non linear capacitors C_1 and C_2 .

In the "Ohmic" mode (i.e. $V_d < V_p$), the current J_d as approximated from the general formulation , is given by:

$$(1) \quad J_d = \frac{K_p}{(1+(V_g-V_T)/\psi_i)(1+V_d/L.EO)} ((V_g-V_T)V_d - 0.5 V_d^2)$$

with $K_p = \mu_0(Z/L).C_{ox}$, where μ_0 is the carrier mobility at low electric field level, Z the channel perimeter, L the channel length, C_{ox} the gate oxide capacitor per unit area, V_g and V_d the gate-source and drain-source potentials, V_T the threshold voltage. " ψ_i " and $L.EO$ are the potentials related to the effect of the transverse and longitudinal electric fields on the carrier mobility in the channel (i.e. transverse roll-off limitation and longitudinal velocity saturation). The capacitors C_1 and C_2 can be considered as equal and are approximated to $(C_{ox}.Z.L)/2$ [10].

In the "Saturation" mode (i.e. $V_d \geq V_p$), the drain voltage V_p corresponding to the onset of the channel pinch-off, assuming a perfect current saturation i.e. there is no effect of channel length modulation [11], is given by:

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$$(2) V_p = L \cdot E_O \left(\left(1 + 2 \frac{V_g - V_T}{L \cdot E_O} \right)^{1/2} - 1 \right)$$

In that mode, the channel is pinched and "disappears" on the drain side, so does the capacitor C1, and C2 takes a value close to 2/3 Cox.Z.L [8,9].

In the "Blocked" mode (i.e. $V_g < V_T$), the drain current will theoretically be null as the "subthreshold" current is neglected, and the intrinsic transistor is reduced to one element: the oxide capacitor Cgsb. Although this is a distributed capacitor over the whole P region, we suppose it, for the model, located between the gate and source electrodes ($C_{gsb} = C_{ox} \cdot Z \cdot L$).

We complete the model with the source inductance Ls which can induce an important feed-back effect from the output to the input. The static parameters are Kp, VT, psi, L.EO, Ra and Rd; they can be obtained by a classical way with low and high level drain voltage measurements [12]. The dynamic parameters are Rg, C1, C2, Cgso, Cgsb, Cgd, Cds and Ls, they can be partially obtained with an original method developed previously [10], based on the constant current gate charge relation.

II-2- Implantation of the model for SPICE program:

This VDMOS transistor model cannot be described by a single component of the SPICE library so it is necessary to build a macro-component (sub-circuit) in which each element (non linear capacitor, current generator, etc.) is a part of this library. Then the current generator Jd is represented by the MOS model level 1 or 3, and the non linear capacitors Cds and Cd thanks to the transition capacitances of the diode model. The elements Cgsb, Cgso, C2 are represented by an unique capacitor Cgs; this one is constant in a first order approximation as for Ra and Rd too. The capacitor C1 acts-only in the "ohmic" mode so it can be neglected for the purpose of simulation. The remaining SPICE parameters are defined as: $V_{MAX} / \mu O = E_O$ and $\theta = 1/\psi$. The macro model obtained is shown in Fig. 3. We propose two solutions: i) the first one is what we call the "Switch Solution" because in order to simulate the non linearity of the Miller capacitance Cgd, we use alternately two components: a diode Cd* and a capacitor Cgdmax which are switched thanks to two transistors M2,3 of the model level 1, ii) the second one requires less components but an initialization procedure to set up the static bias of the middle node of the two capacitors in series Cgdmax and Cd. This second model is much faster in CPU time than the first one as the transistor number is decreased by a three fold, but because of its initialization step, it cannot be set up as a "black-box" sub-circuit. The related listings can be supplied by the authors.

III. APPLICATION OF THE MODEL IN A SWITCHING CONFIGURATION:

III-1- Basic considerations on the device operation:

Beside the direct mode, the model takes account of the behaviour of the device within the third quadrant of the output electrical characteristics (Fig.4); this operating mode is useful for the modeling of applications such as synchronous rectifiers, power energy converters and controls, in particular, those without "free-wheeling" diodes. In this case, the current is shared by both the MOS conduction channel and the "body" diode. It is worthy to notice that, at "low level" current (i.e. compared to the device rated continuous current), the channel contribution decreases noticeably the conduction losses whereas, at higher level, the resistivity modulation of the drain epilayer by the diode holes injection allows an overall series resistance noticeably lower than the MOS on-state resistance RON from a 1:2 to 1:20 factor for 60V to 1000V device voltage ratings. Thus the "body" diode is differentiated from the element Cds in the model.

III-2- Switching operation:

We use here our model in a switching configuration (see Fig.5) and look at the gate-source VGS, drain-source VDS voltages and drain current ID. The electrical characteristics are simulated under SPICE "transient analysis" option, and compared to experimental temporal waveforms, as well as for low voltage products (MTP25N06L - 60 volts) and for high voltage ones (MTH5N100 -1000 volts).

III-2-1- Resistive switching (LD=0):

As one can see on the figure 6, the simulation waveforms agree well with experimental results. If we look closer at the switching times ton and toff, we notice a difference less than 10% between the measured and simulated values for all the different devices studied.

III-2-2- Inductive switching (RD=0):

This test is more realistic since it covers a lot of applications : motor drive, converters etc... The obtained waveforms are quite different from those studied previously on resistive loads and depend on how big the time constant $LD/(RD + RON)$ is. Furthermore, as the inductive load LD on the transistor drain can induce very high voltage spikes at turn off, the transistor is usually clamped by several different ways : "free wheel" diode, SNUBBER, Zener clamp etc...

At first, we have verified that the model, without any protection on the drain, allows to forecast the voltage spike value on the drain. But usually the device is protected by a clamp between drain and source, so the overvoltage is limited to a value below the breakdown voltage of the MOS'T. The waveforms we got in this configuration are shown in Fig.7a. Fig.7b demonstrate the good precision of the simulation for both the voltage-current values and waveforms. The overvoltage is accounted for by the transient factor $LD \cdot dI/dt$ which can be very high. The drain voltage remains equal to Vclamp as long as there is energy to dissipate in the load LD. As soon as it reaches its clamping value, the drain current falls very sharply . The time needed for this current to fall to zero (as it is setting up in the clamp) depends on the device characteristics (mainly its source inductance Ls), on the initial peak value of the current and on the clamp used. Depending on how big the overvoltage is, we can notice some oscillations of the drain voltage whose period is related to the RLC series circuit elements: the load LD, the drain-source Cds and gate-drain Cgd capacitors, the damping resistances RD, RON and RG.

From a practical point of view, it is important to notice that a transient current flows into the gate resistance RG; the current value is proportional to dV_{DG}/dt . Thus a transient gate voltage is set up by the ohmic drop through RG. Particularly, if the RG

resistance has a rather big value, the oscillations can bring a too high (dangerous) gate voltage well beyond the absolute ratings of the transistor.

IV. CONCLUSION:

We have shown here a model for VDMOS power transistors (working in switching mode) applicable to the analog circuit simulator U.C. Berkeley's SPICE2; it is obtained from a previous and more complete model [8-10]. The SPICE macro-component requires five static "elements": $M1(J_d)$, D_{body} , R_d , R_a , R_s , and six dynamic ones: C_{gdmax} , C_d , C_{gs} , C_{ds} , R_g , L_s . The way of determining them is explained in the several reports noted in the references.

The future work will consist in: i) extending these results to other Power Mosfets devices from the Motorola TMOS™ family (actually -june 1988- a preliminary library can be furnished on request), ii) taking into account the thermal effects (at least a global manner), iii) to transfer these results to end users to check if this model feeds their needs, iv) finally, to compare this model with those existing from other laboratories: especially for implantation method, parameters extraction, accuracy, calculation speed. About this last criteria, some comparisons, even if not systematic, have been performed and show that our model is better with a factor varying from 30 to 80% compared to other proposed configurations.

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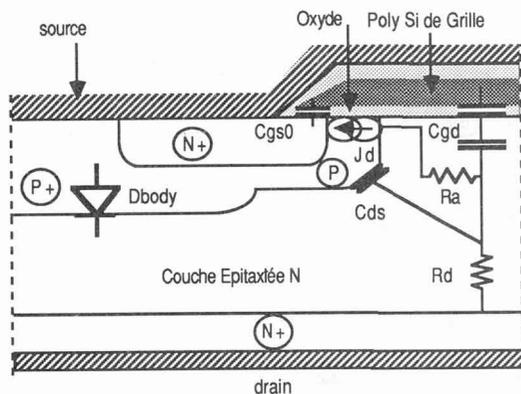


Figure 1: Cross section of the VDMOS power transistor. Localization of the simplified model elements .

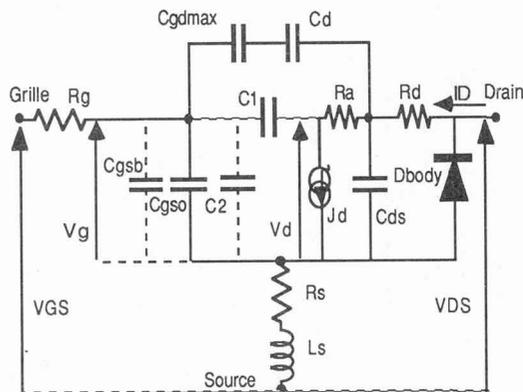


Figure 2: Simplified model of the VDMOS power transistor in conduction (in blocked mode, C_{gsb} is paralleled to C_{gs0}).

